

AMCC 405GP
PowerPC

Document Issue 1.00

September 2004

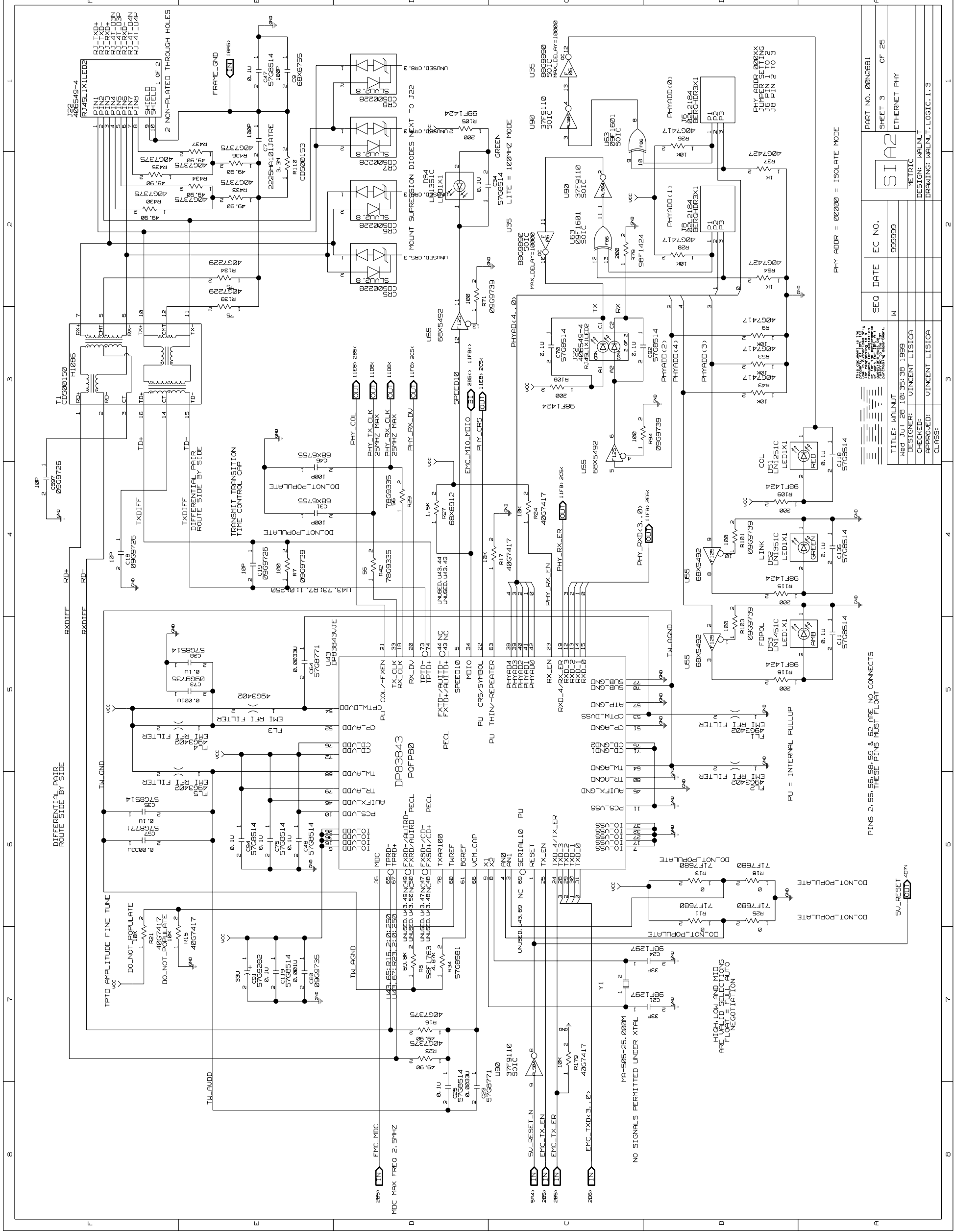
PPC405GP Embedded Processor Schematic

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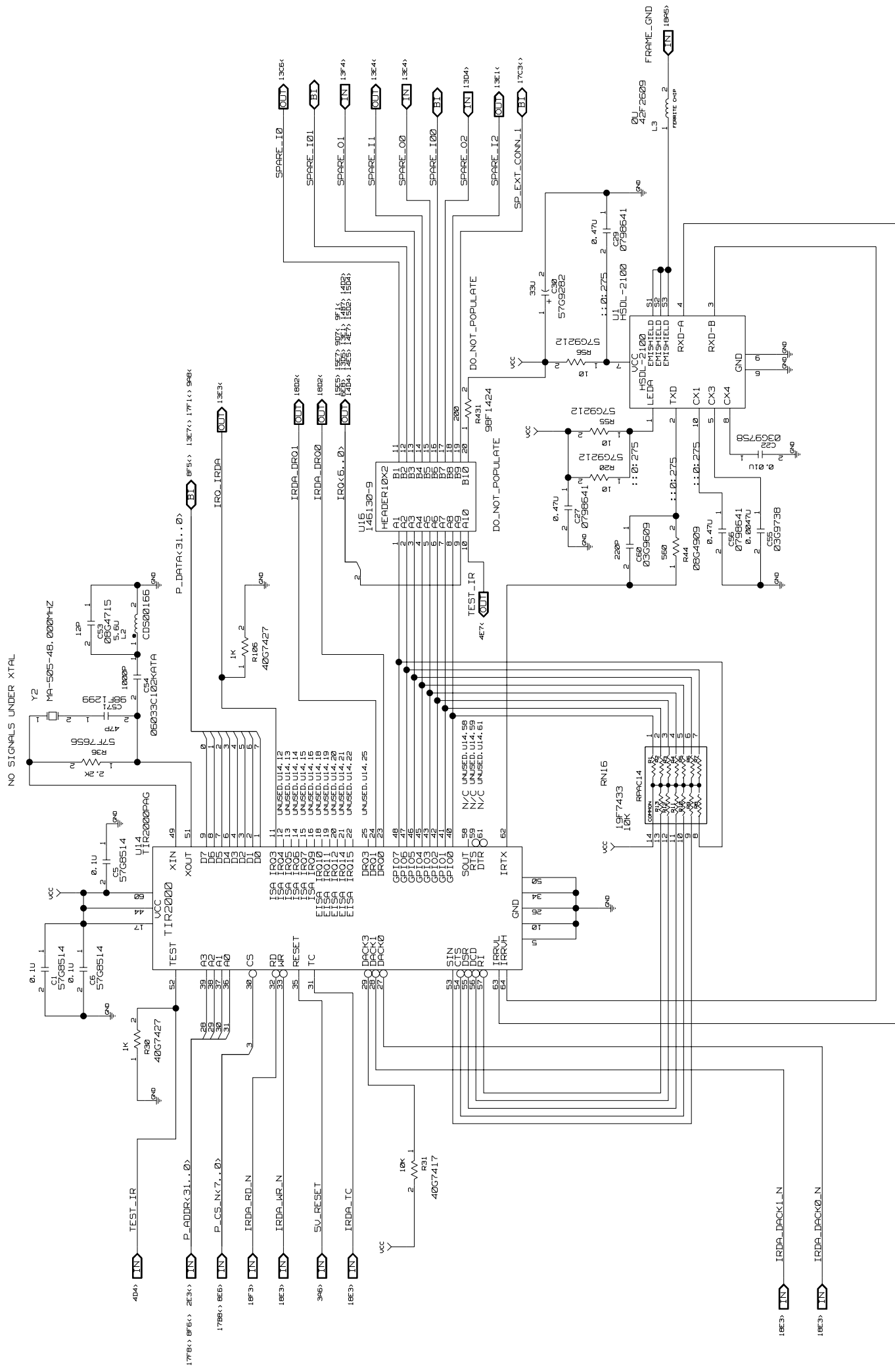
		PART NO. 00N2661 SHEET 3 OF 25
TITLE: WALNUT WED JUL 28 10:35:38 1999	EC NO. 999999	ETHERNET PHY
DESIGNER: VINCENT LISTICA CHECKED: VINCENT LISTICA	METRIC	DRAWING: WALNUT.LOGIC.1.3
APPROVED: VINCENT LISTICA CLASS:	PHY ADDR = 00000 = ISOLATE MODE	

THIS DRAWING IS THE PROPERTY OF SIA2. IT IS TO BE USED ONLY FOR THE PROJECT AND FOR THE BOARD FOR WHICH IT WAS DESIGNED. IT IS NOT TO BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.

PINS 2, 55, 56, 59, & 62 ARE US. CONNECTS THESE PINS MUST FLOAT

HIGH, LOW, AND MID ARE VALID ELECTRONS NEGOTIATION

NO SIGNALS PERMITTED UNDER XTAL

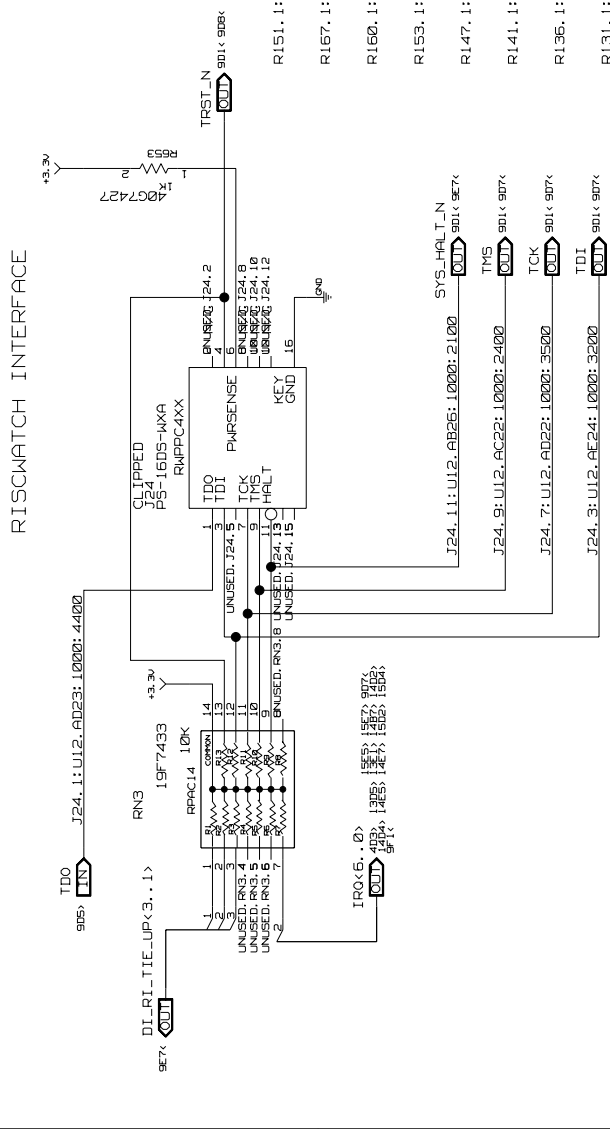


- CONTROLLER MODES:
- 1) FAST IRDA - FIR
 - 2) MEDIUM IRDA - MIR
 - 3) SLOW IRDA - SIR
 - 4) SHARP INFRARED - IR
 - 5) TV MODE
 - 6) UART MODE - NOT AVAILABLE

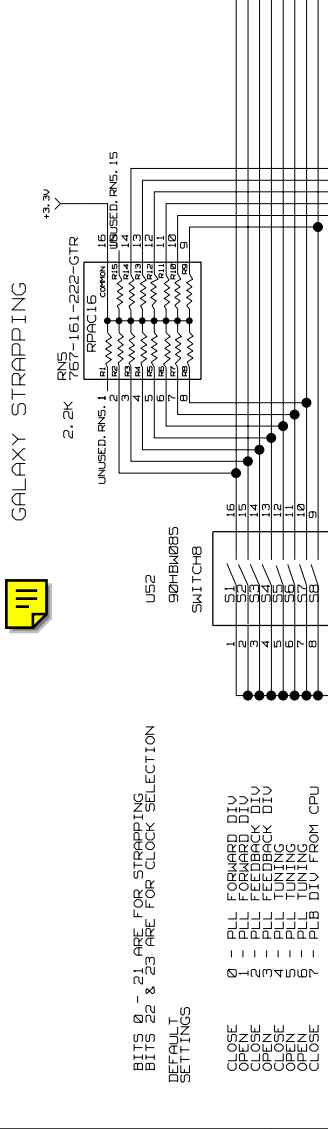
TITLE: WALNUT		DESIGNER: VINCENT LISTICA
MFG: JUN 28 10:35:48 1999		CHECKED: VINCENT LISTICA
CLASS:		APPROVED: VINCENT LISTICA

SEQ	DATE	EC NO.	PART NO. 00N2661
W		999999	SHEET 4 OF 25
SIA2			IRDA INTERFACE
METRIC			
DESIGN: WALNUT			
DRAWING: WALNUT.LOGIC.1.4			

RISCVATCH INTERFACE



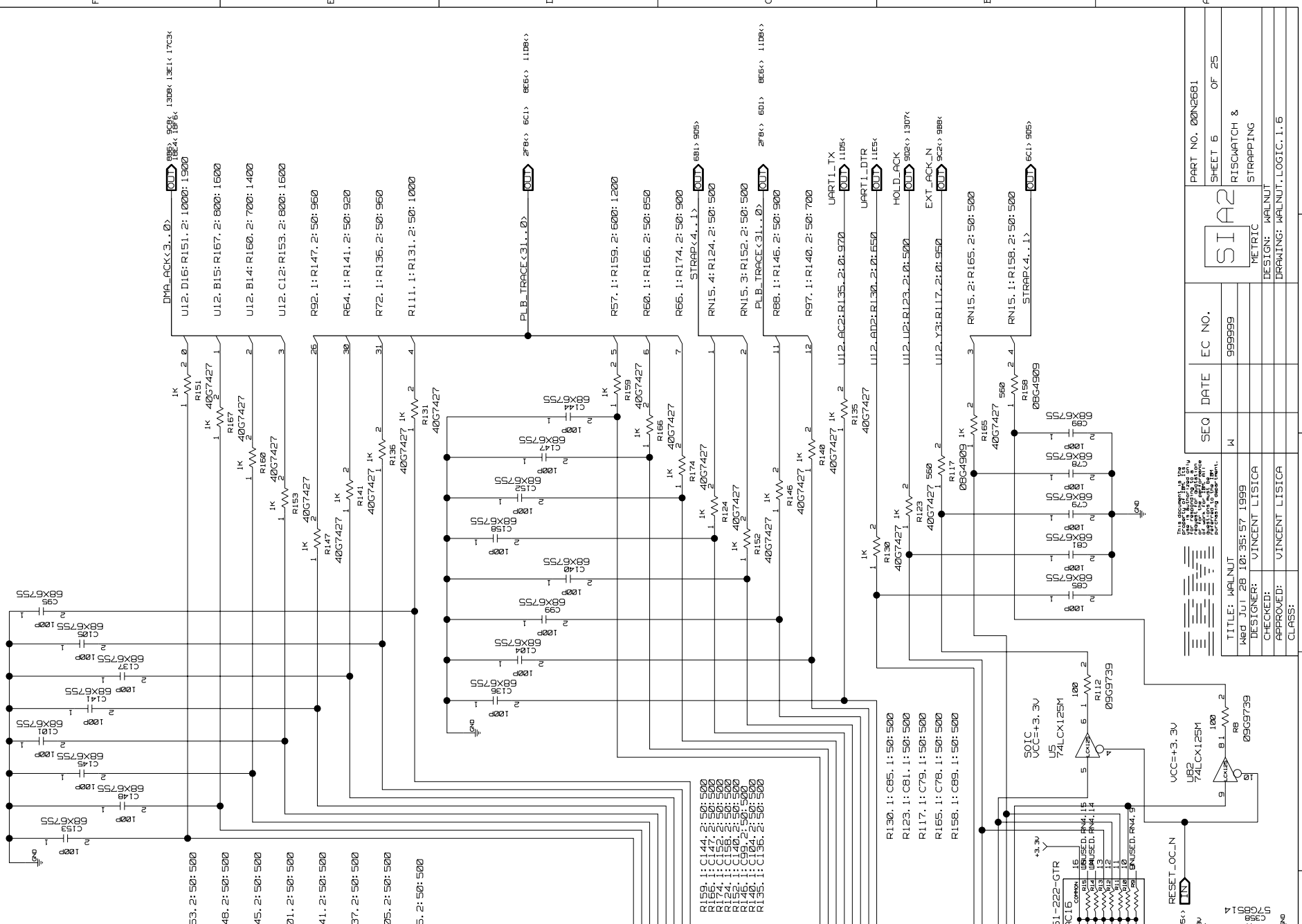
GALAXY STRAPPING



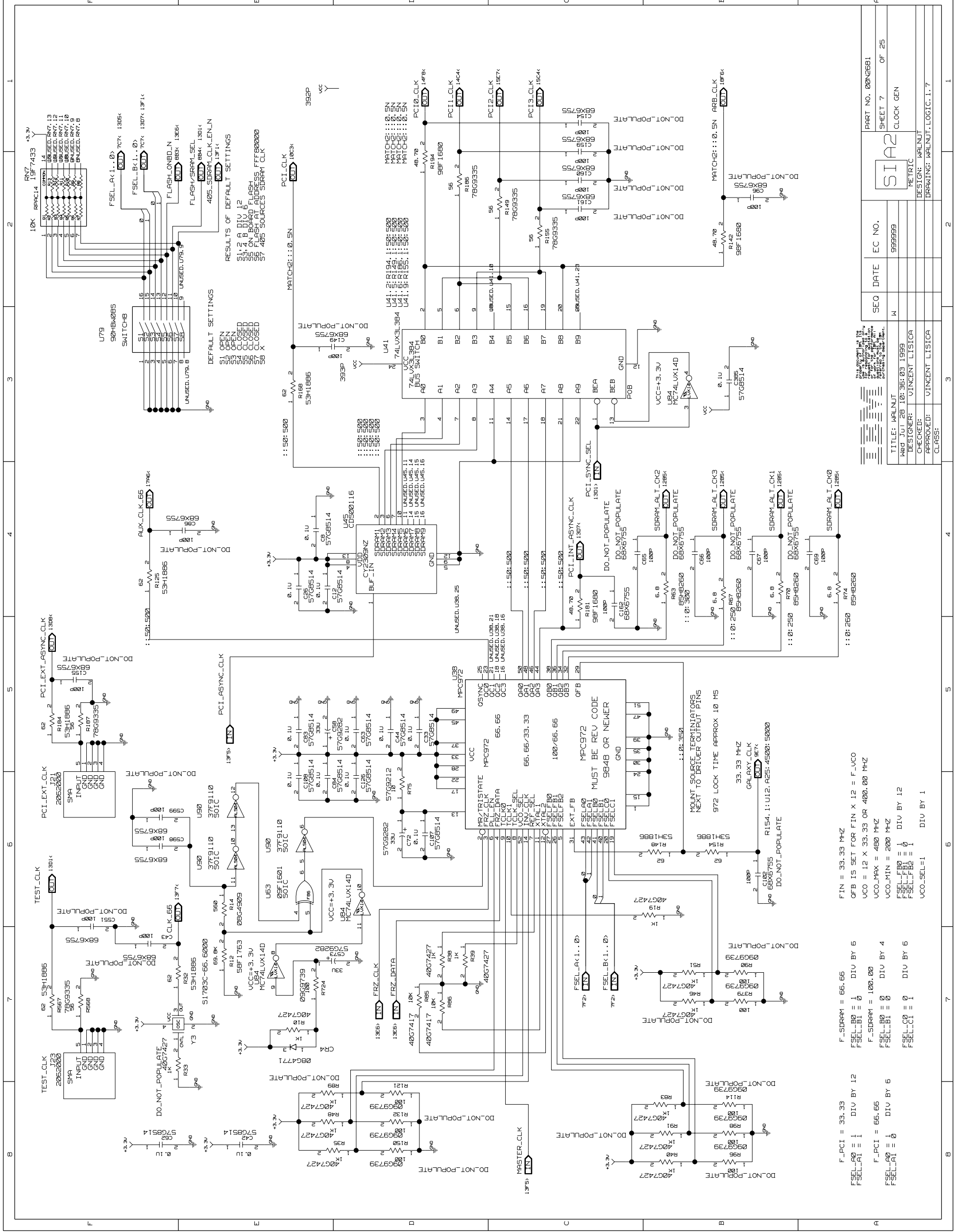
BITS 0 - 21 ARE FOR STRAPPING
 BITS 22 & 23 ARE FOR CLOCK SELECTION
 DEFAULT SETTINGS
 0 - PLL FORWARD DIV
 1 - PLL FORWARD DIV
 2 - PLL FEEDBACK DIV
 3 - PLL FEEDBACK DIV
 4 - PLL TUNING
 5 - PLL TUNING
 6 - PLL TUNING
 7 - PLL TUNING
 8 - PLL DIV FROM CPU
 9 - OPB DIV FROM PLB
 10 - OPB DIV FROM PLB
 11 - OPB DIV FROM PLB
 12 - PCT DIV FROM PLB
 13 - PCT DIV FROM PLB
 14 - EXT BUS DIV FROM PLB
 15 - ROM ADDR DIV

16 - ROM WIDTH
 17 - ROM LOCATION
 18 - PC SELECT MODE ENABLE
 19 - PC SELECT MODE ENABLE
 20 - ECC MODE ENABLE
 21 - PCT ABLETTOR ENABLE
 22 - SCLK-SRC
 23 - SCLK-SRC

RESULTS OF SETTINGS
 FORWARD DIV = 2
 PLL FEEDBACK DIV = 2
 PLL FEEDBACK DIV FROM PLB = 2
 PCT DIV FROM PLB = 2
 PCT DIV FROM PLB = 2
 ROM WIDTH = 8 BITS
 ROM LOCATION IS PERIPHERAL ATTACH
 PCT IN-TURNAL ARB IS ENABLED
 PCT IN-TURNAL ARB IS SELECTED (FROM 66.66 MHZ OSC)
 CPU = 400 MHz
 OPB = 600 MHz
 PCT = 600 MHz
 PCT_LASTING = 1 = VCC



	PART NO. 080N2681 SHEET 6 OF 25
TITLE: WALNUT DESIGNER: VINCENT LISTICA CHECKED: VINCENT LISTICA APPROVED: VINCENT LISTICA CLASS:	EC NO. 999999 RISKWATCH & STRAPPING METRIC DESIGN: WALNUT DRAWING: WALNUT.LOGIC.1.6



FPC1 = 33.33
 FSEL_A0 = 1 DIV BY 12
 FSEL_A1 = 1
 F_SDRAM = 66.66
 FSEL_B0 = 1 DIV BY 6
 F_SDRAM = 100.00
 FSEL_B1 = 0 DIV BY 4
 FSEL_C0 = 0 DIV BY 6
 FSEL_C1 = 1 DIV BY 6
 F_IN = 33.33 MHz
 OFB IS SET FOR FIN X 12 = F_VCO
 VCO = 12 X 33.33 OR 400.00 MHz
 VCO_MAX = 480 MHz
 VCO_MIN = 200 MHz
 FSEL_FB0 = 1 DIV BY 12
 FSEL_FB1 = 1
 VCO_SEL = 1 DIV BY 1

MOUNT SOURCE TERMINATORS NEXT TO DRIVER OUTPUT PINS
 972 LOCK TIME APPROX 10 MS
 33.33 MHz GALAXY-CLK
 R154.1:U12.A25:4500:5000
 DO_NOT_POPULATE

MATCH=2: 0:5N
 MATCH=3: 0:5N
 MATCH=4: 0:5N
 MATCH=5: 0:5N
 MATCH=6: 0:5N
 MATCH=7: 0:5N
 MATCH=8: 0:5N
 MATCH=9: 0:5N
 MATCH=10: 0:5N
 MATCH=11: 0:5N
 MATCH=12: 0:5N
 MATCH=13: 0:5N
 MATCH=14: 0:5N
 MATCH=15: 0:5N
 MATCH=16: 0:5N
 MATCH=17: 0:5N
 MATCH=18: 0:5N
 MATCH=19: 0:5N
 MATCH=20: 0:5N
 MATCH=21: 0:5N
 MATCH=22: 0:5N
 MATCH=23: 0:5N
 MATCH=24: 0:5N
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 MATCH=95: 0:5N
 MATCH=96: 0:5N
 MATCH=97: 0:5N
 MATCH=98: 0:5N
 MATCH=99: 0:5N
 MATCH=100: 0:5N

RESULTS OF DEFAULT SETTINGS
 S1 OPEN
 S2 OPEN
 S3 OPEN
 S4 OPEN
 S5 OPEN
 S6 OPEN
 S7 OPEN
 S8 OPEN
 S9 OPEN
 S10 OPEN
 S11 OPEN
 S12 OPEN
 S13 OPEN
 S14 OPEN
 S15 OPEN
 S16 OPEN
 S17 OPEN
 S18 OPEN
 S19 OPEN
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 S86 OPEN
 S87 OPEN
 S88 OPEN
 S89 OPEN
 S90 OPEN
 S91 OPEN
 S92 OPEN
 S93 OPEN
 S94 OPEN
 S95 OPEN
 S96 OPEN
 S97 OPEN
 S98 OPEN
 S99 OPEN
 S100 OPEN

TITLE: WALNUT
 DESIGNER: VINCENT LISTICA
 CHECKED: VINCENT LISTICA
 APPROVED: VINCENT LISTICA
 CLASS:

PART NO. 00N2661
 SHEET 7 OF 25
 CLOCK GEN

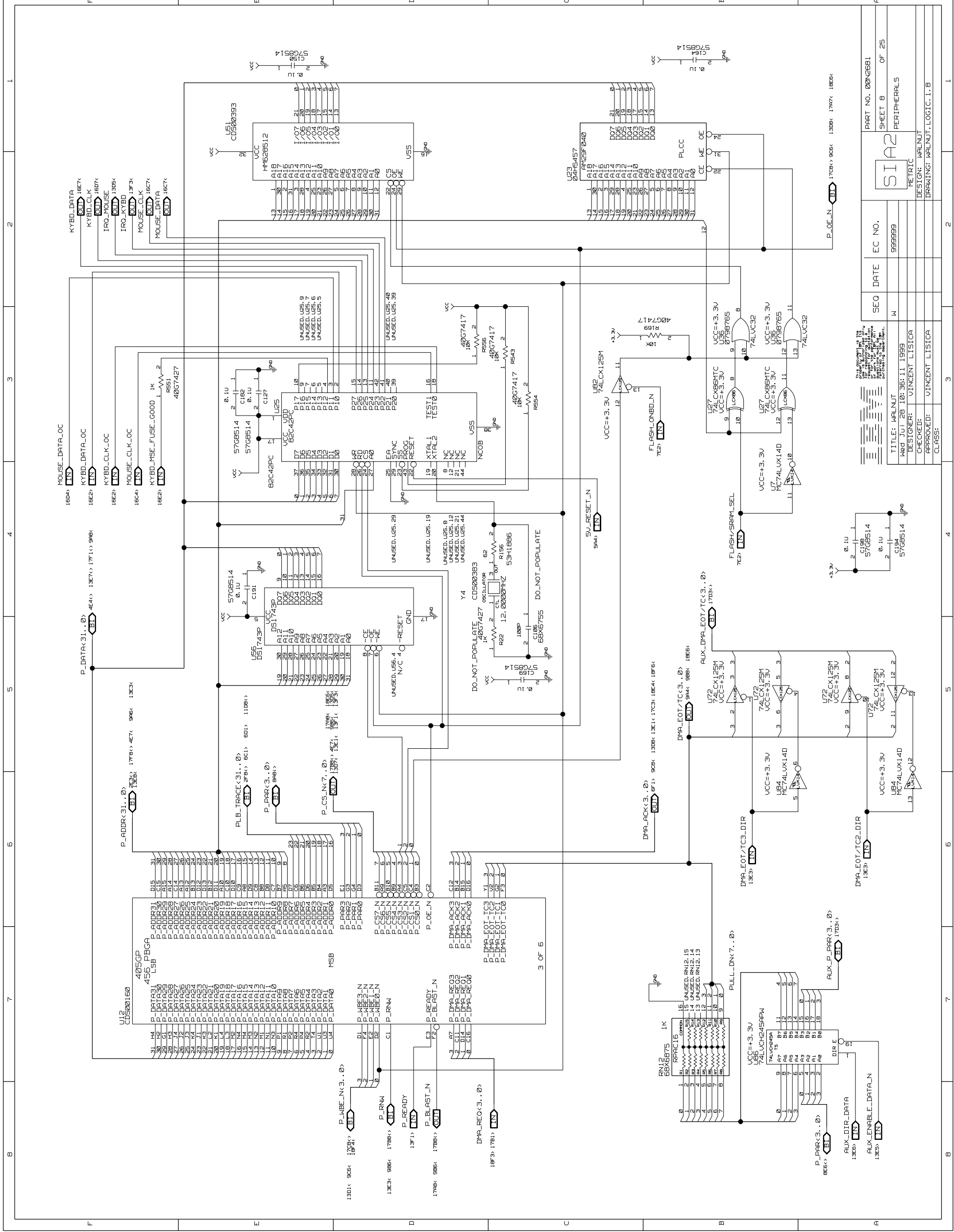
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 METRIC
 DESIGN: WALNUT
 DRAWING: WALNUT.LOGIC.1.7

SEQ DATE EC NO.
 W 999999

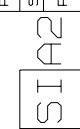
MFG JUL 28 10:36:03 1999
 TITLE: WALNUT
 DESIGNER: VINCENT LISTICA
 CHECKED: VINCENT LISTICA
 APPROVED: VINCENT LISTICA
 CLASS:

PART NO. 00N2661
 SHEET 7 OF 25
 CLOCK GEN

SIA2
 METRIC
 DESIGN: WALNUT
 DRAWING: WALNUT.LOGIC.1.7



TITLE: WALNUT		DESIGNER: VINCENT LISTICA	DATE: JUN 28 10:36:11 1999	EC NO.:	999999	SEQ DATE:	14	EC NO.:	999999	SHEET 8	OF 25
DRAWING: WALNUT.LOGIC.1.8		CHECKED:	APPROVED:	CLASS:						PART NO. 08N2681	
DRAWING: WALNUT.LOGIC.1.8		CHECKED:	APPROVED:	CLASS:						PERIPHERALS	



METRIC

DESIGN: WALNUT

DRAWING: WALNUT.LOGIC.1.8

CLASS:

APPROVED:

CHECKED:

DESIGNER: VINCENT LISTICA

DATE: JUN 28 10:36:11 1999

EC NO.:

999999

SEQ DATE:

14

EC NO.:

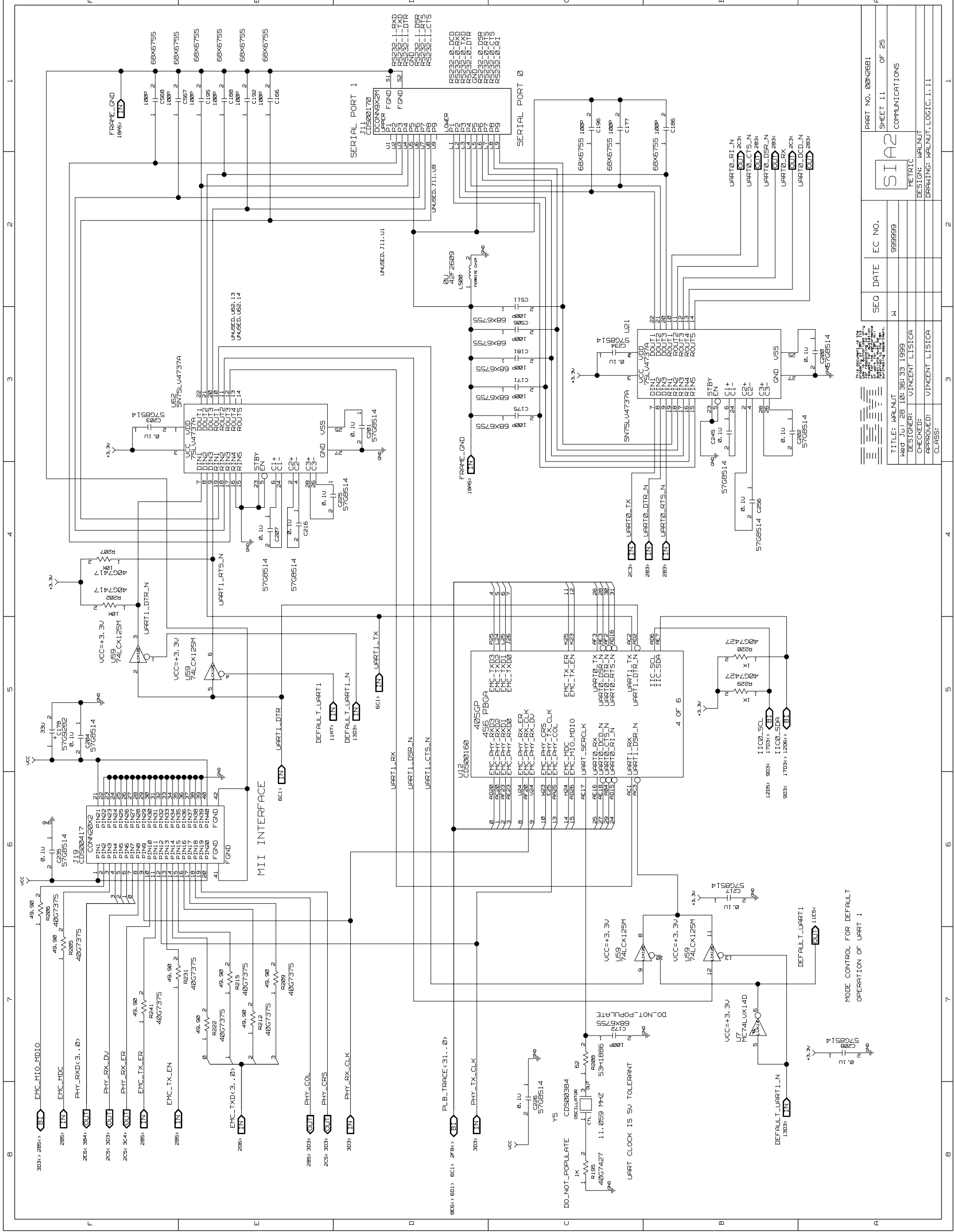
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SHEET 8

OF 25

PERIPHERALS

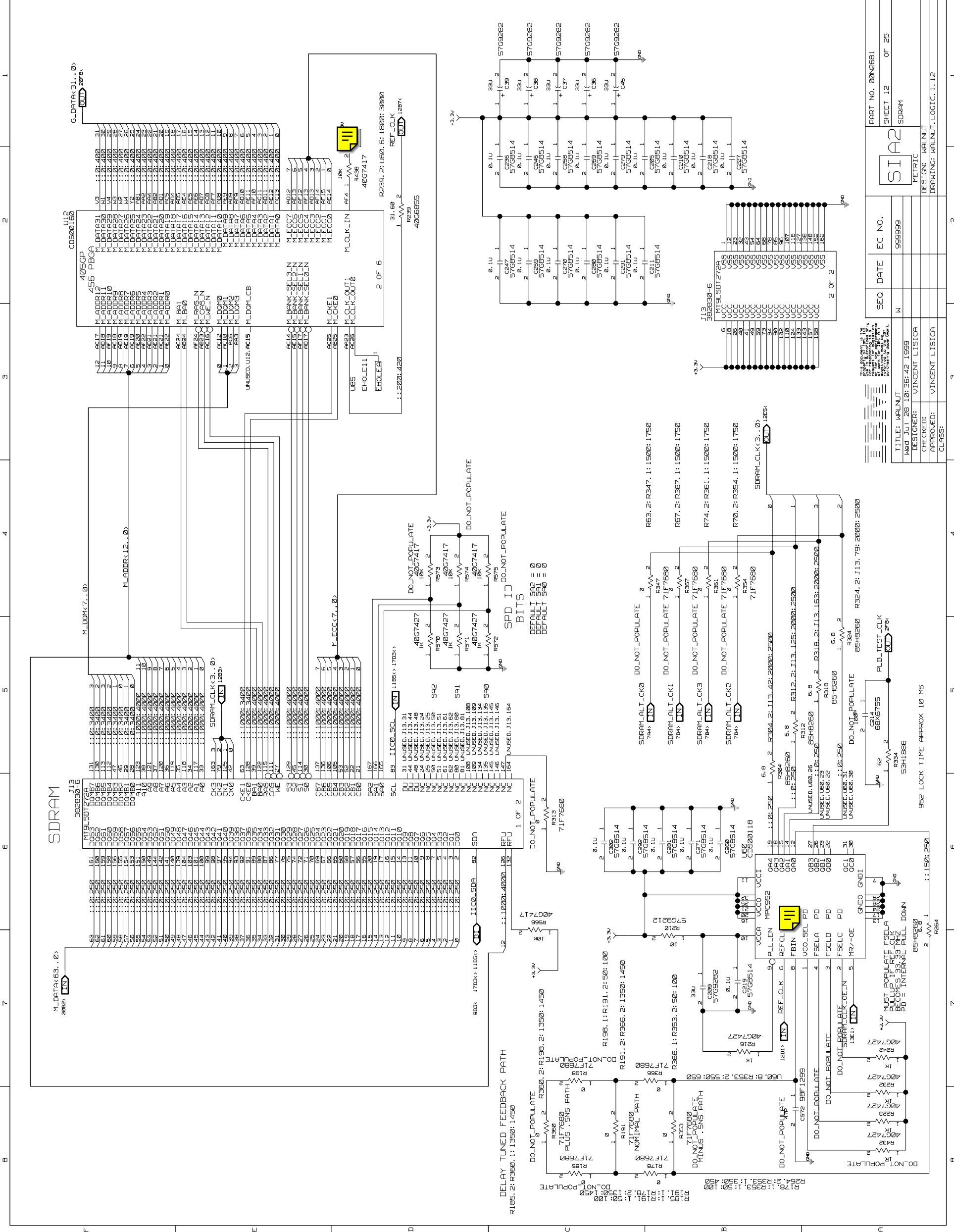
PART NO. 08N2681



PART NO. 00N2661	
SHEET 11 OF 25	
COMMUNICATIONS	
SIA2	
SEO DATE	EC NO.
W	999999
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CHECKED: WALNUT	DESIGN: WALNUT
APPROVED: VINCENT LISTICA	DRAWING: WALNUT.LOGIC.1.11
CLASS:	

TITLE: WALNUT
 WED JUL 28 10:36:33 1999
 DESIGNER: VINCENT LISTICA
 CHECKED: WALNUT
 APPROVED: VINCENT LISTICA
 CLASS:

MODE CONTROL FOR DEFAULT OPERATION OF UART 1



REV	DATE	BY	CHKD	DESCRIPTION
1	10/11/00	W	W	INITIAL DESIGN
2	10/11/00	W	W	REVISED FOR MANUFACTURING
3	10/11/00	W	W	REVISED FOR MANUFACTURING
4	10/11/00	W	W	REVISED FOR MANUFACTURING
5	10/11/00	W	W	REVISED FOR MANUFACTURING
6	10/11/00	W	W	REVISED FOR MANUFACTURING
7	10/11/00	W	W	REVISED FOR MANUFACTURING
8	10/11/00	W	W	REVISED FOR MANUFACTURING

TITLE: WALNUT	DESIGNER: VINCENT LISTICA
WED JUL 28 10:36:42 1999	CHECKED: VINCENT LISTICA
	APPROVED: VINCENT LISTICA
	CLASS:

SEQ	DATE	EC NO.
W	999999	

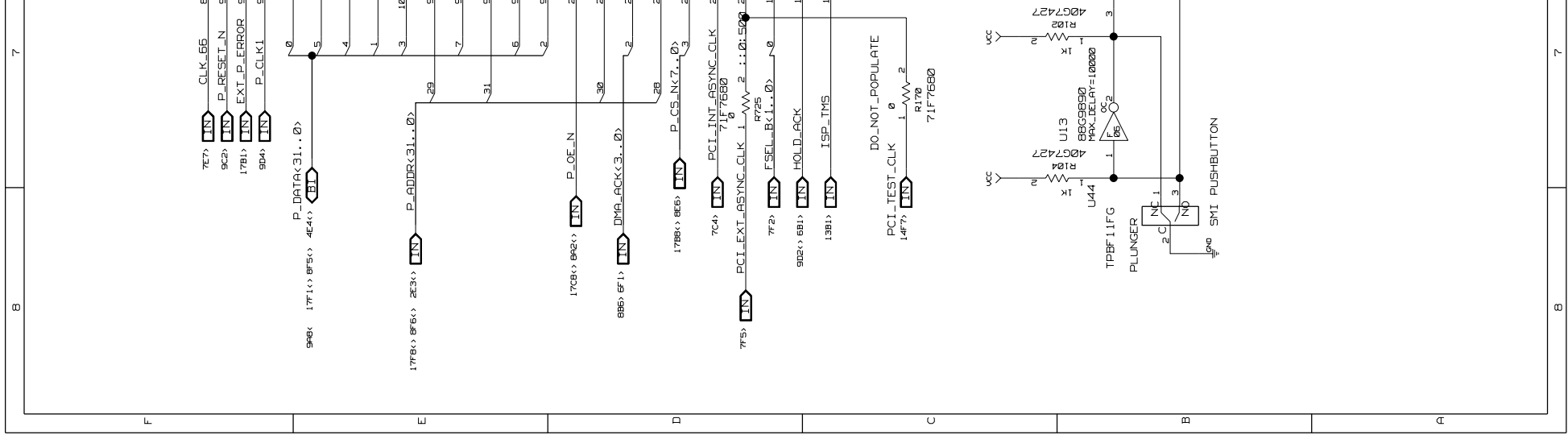
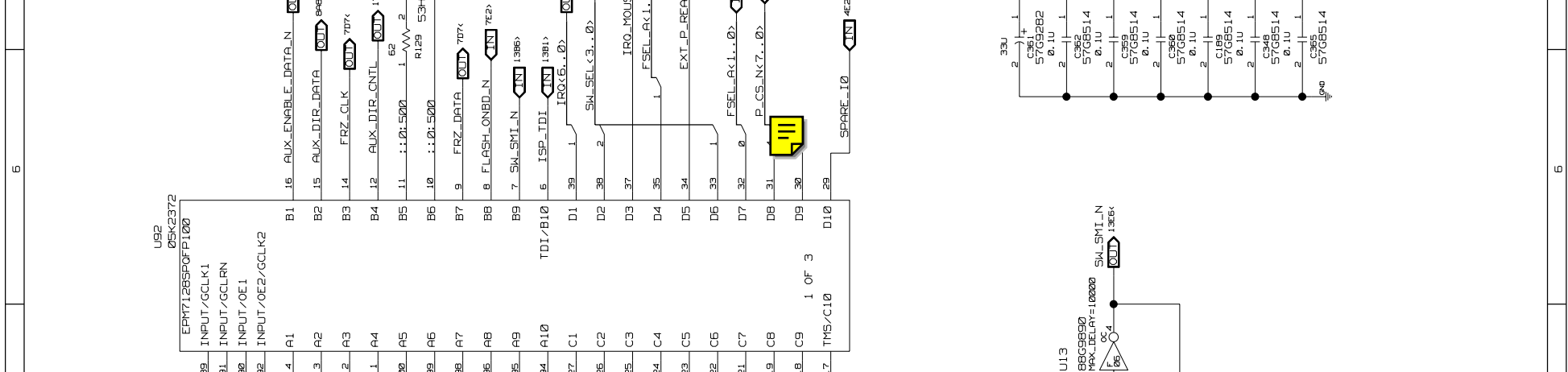
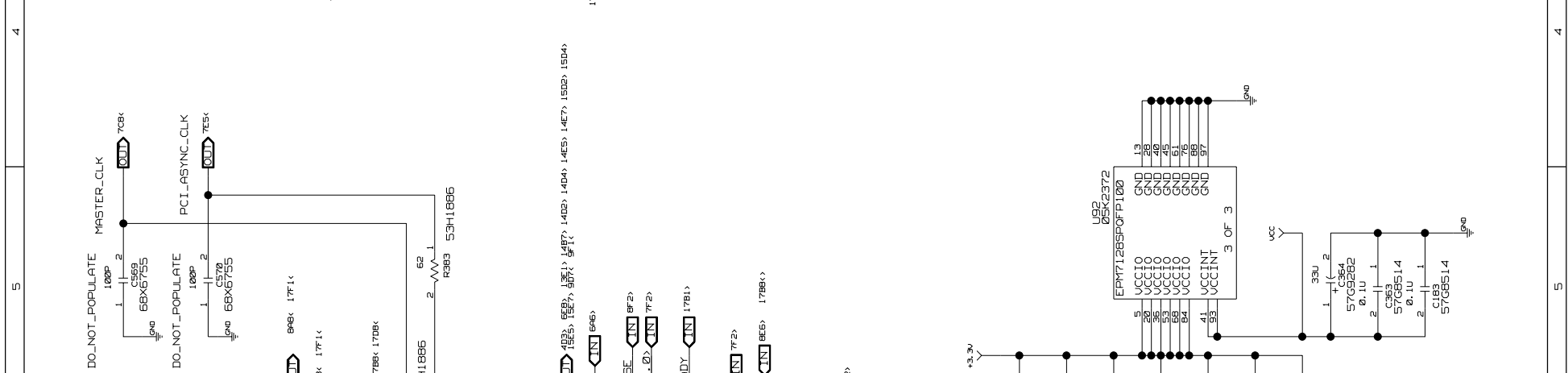
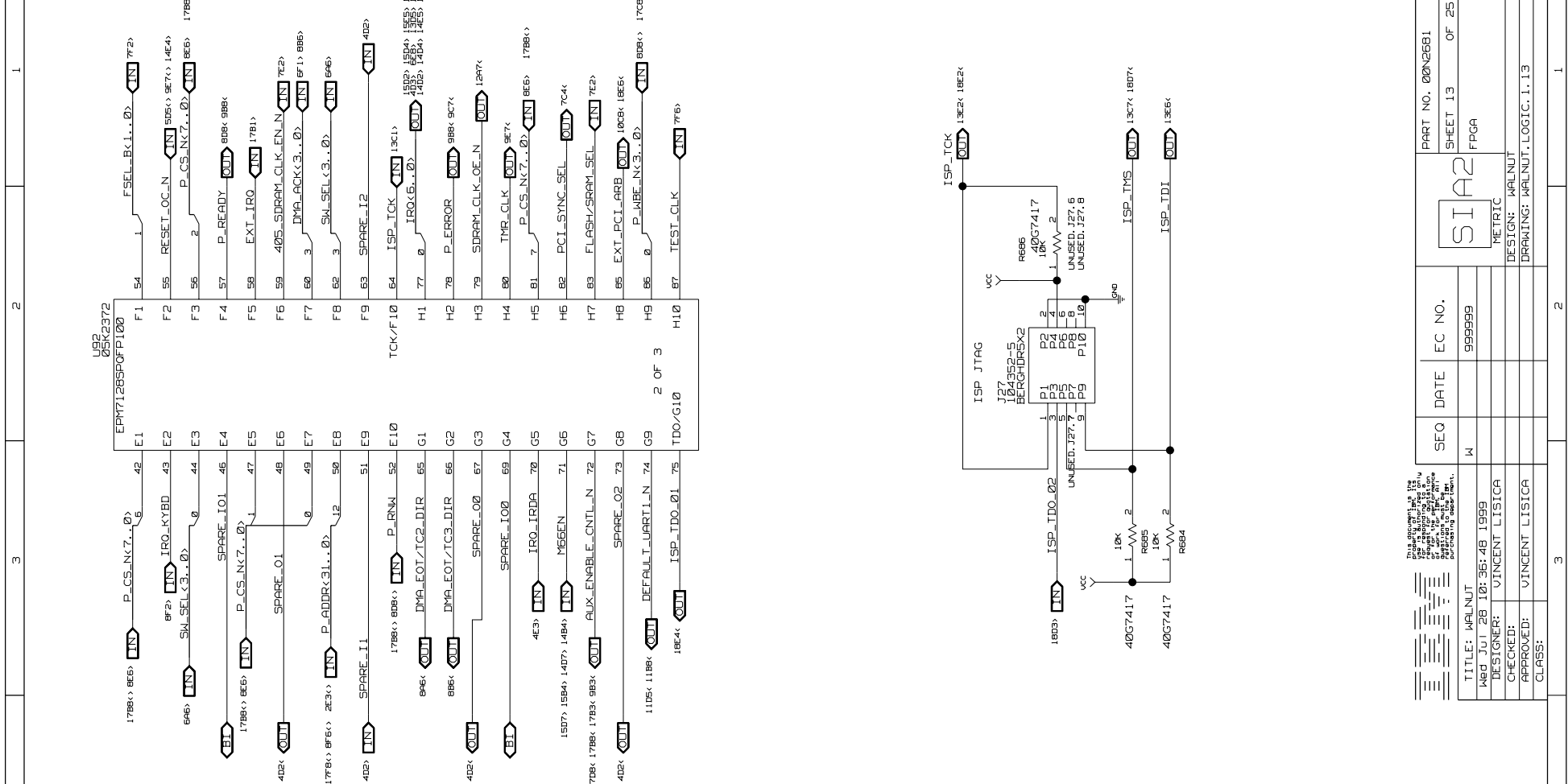
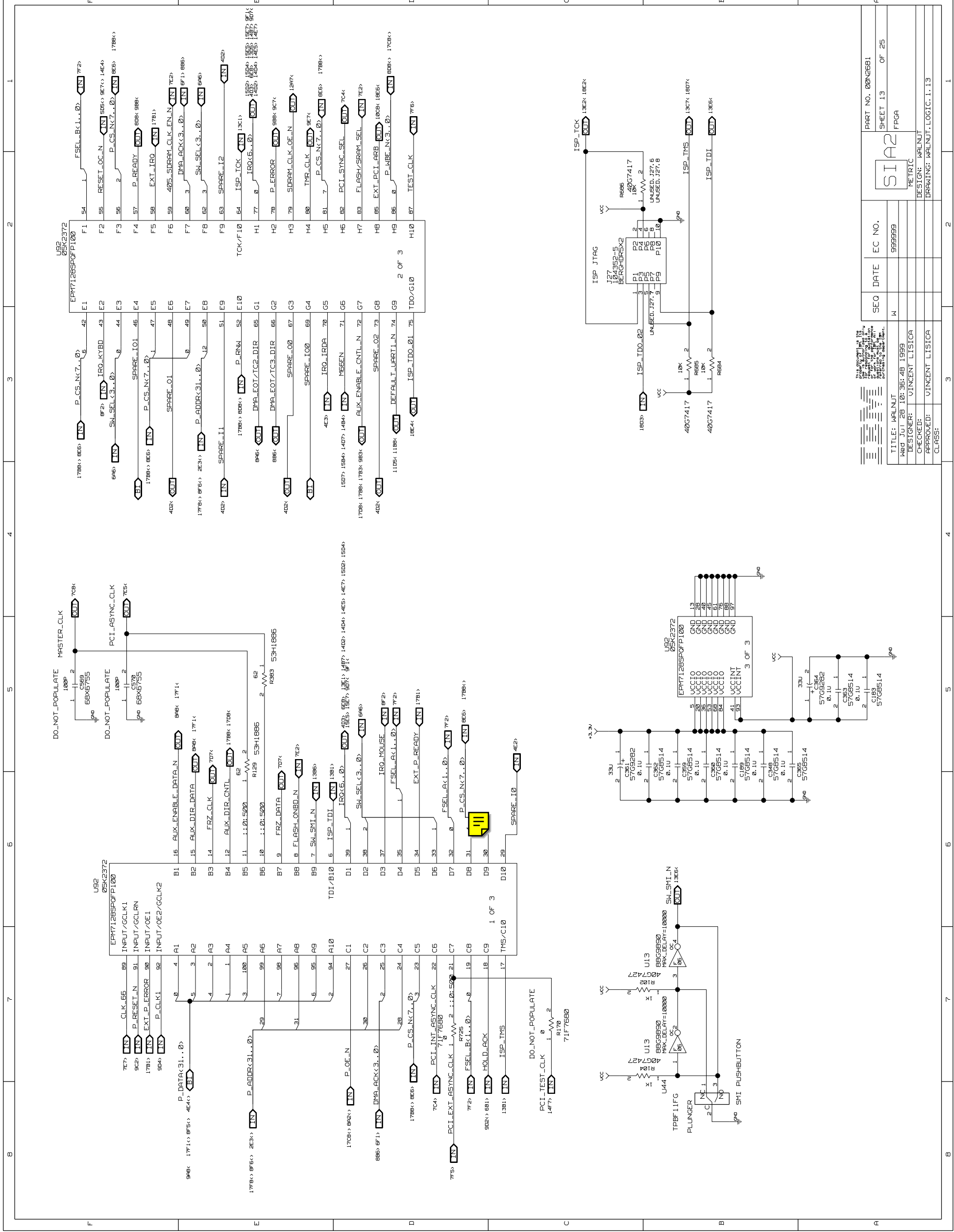
PART NO. 00N2681	SHEET 12 OF 25
SDRAM	

SIA2	
METRIC	
DESIGN: WALNUT	
DRAWING: WALNUT.LOGIC.1.12	

952 LOCK TIME APPROX 10 MS

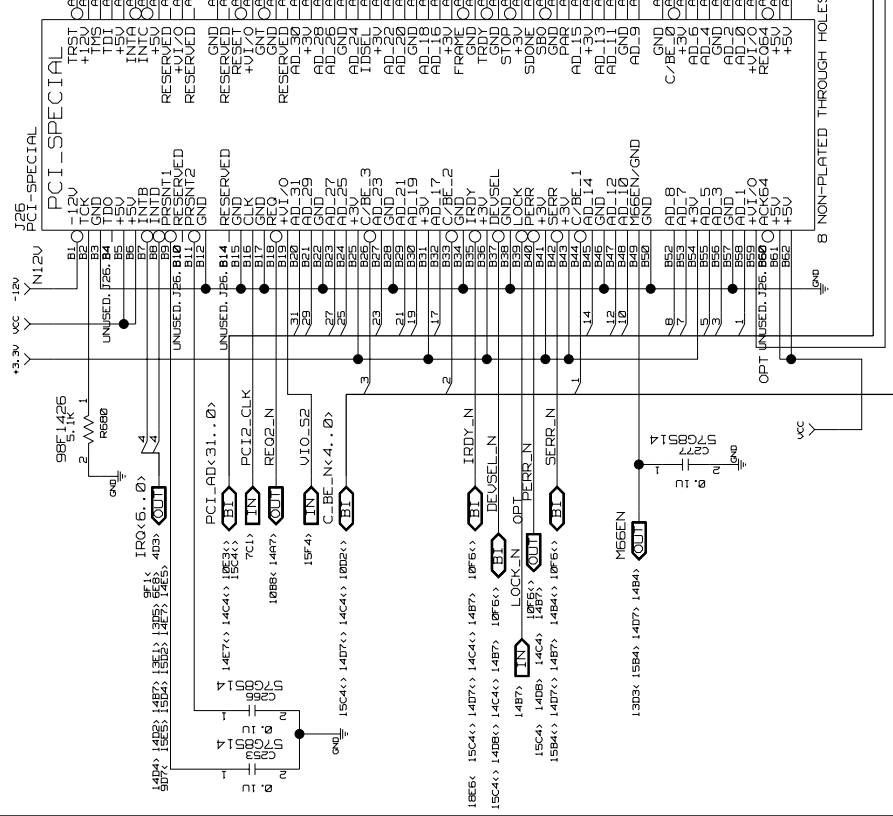
53H1886

53H1886



PCI SLOT2
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

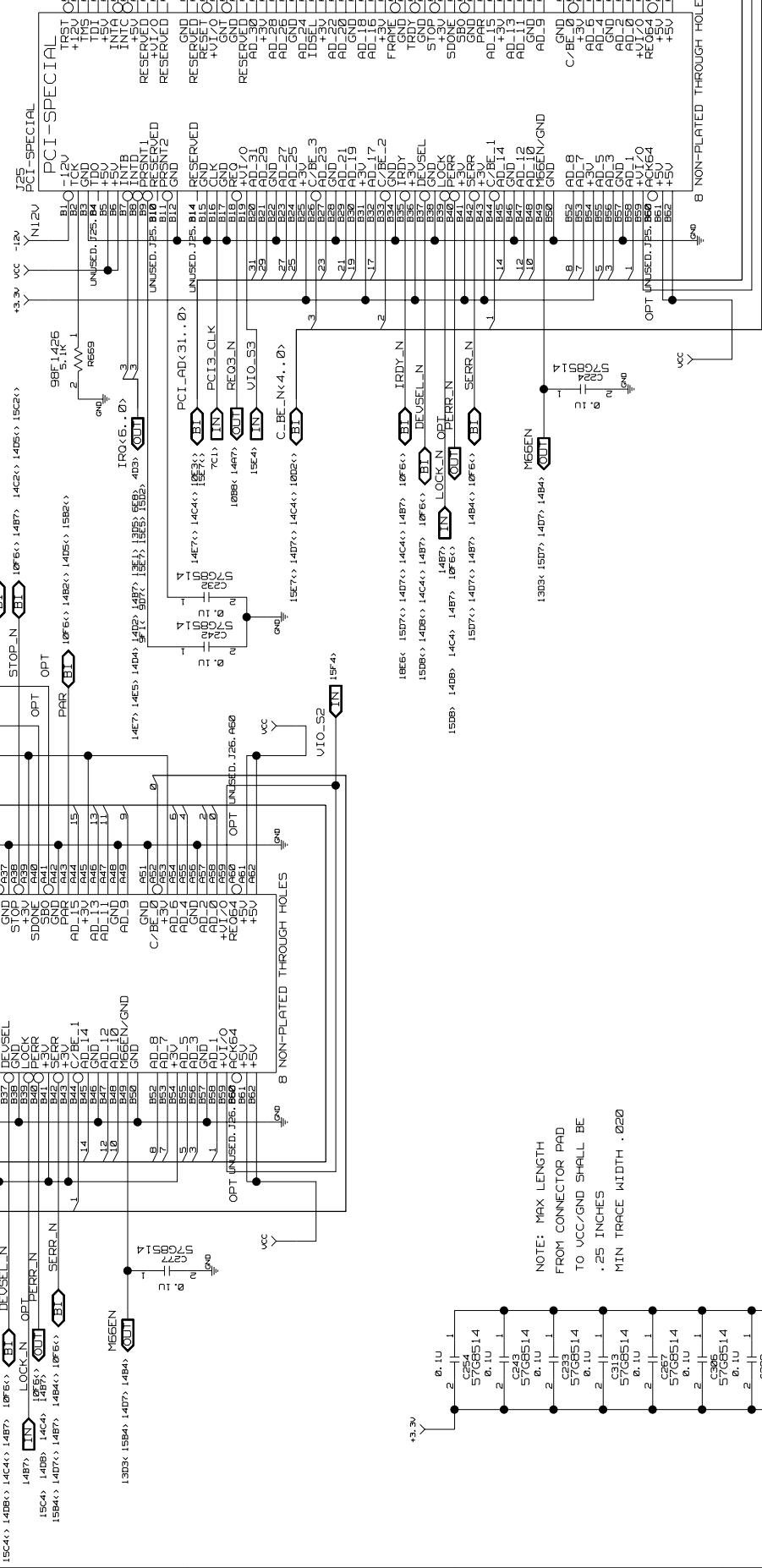


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT3
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

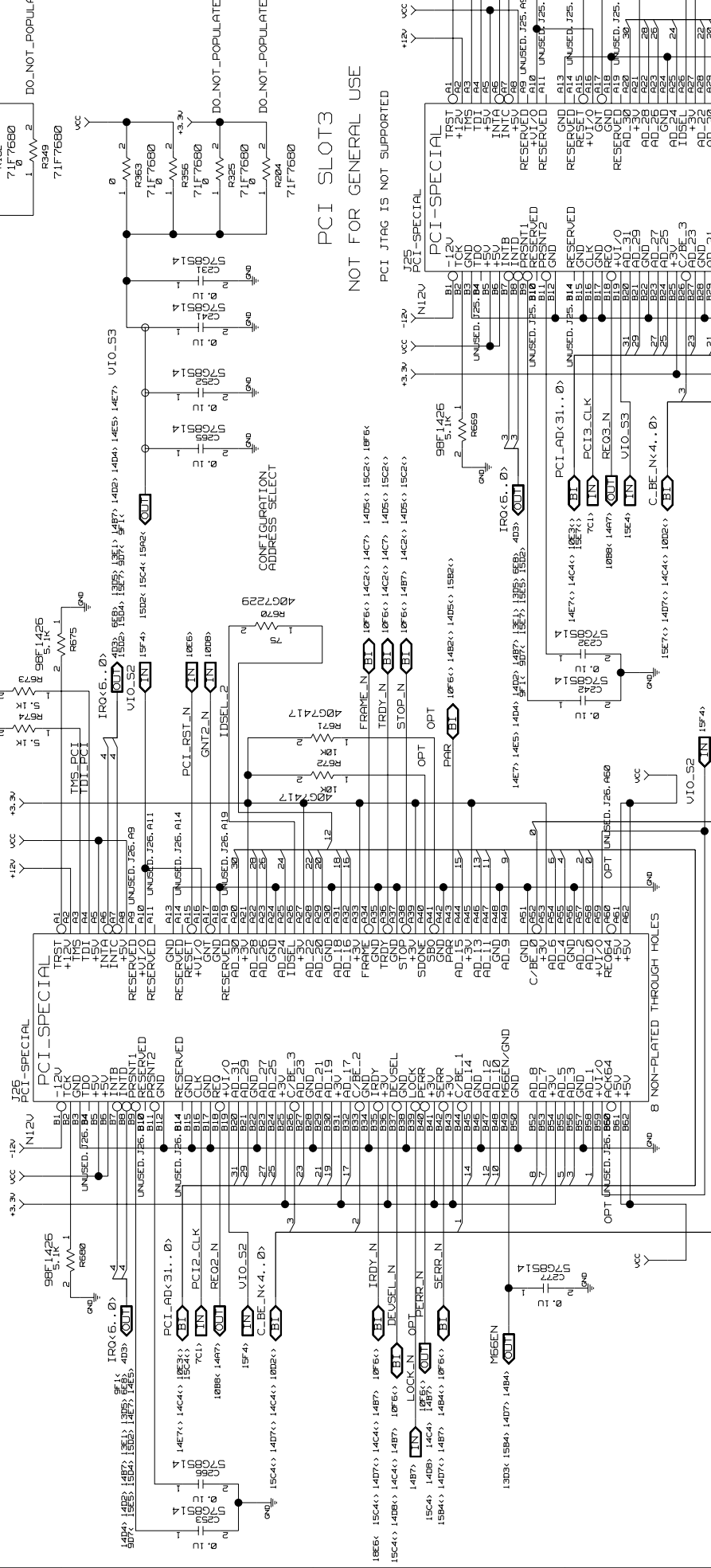


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT4
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

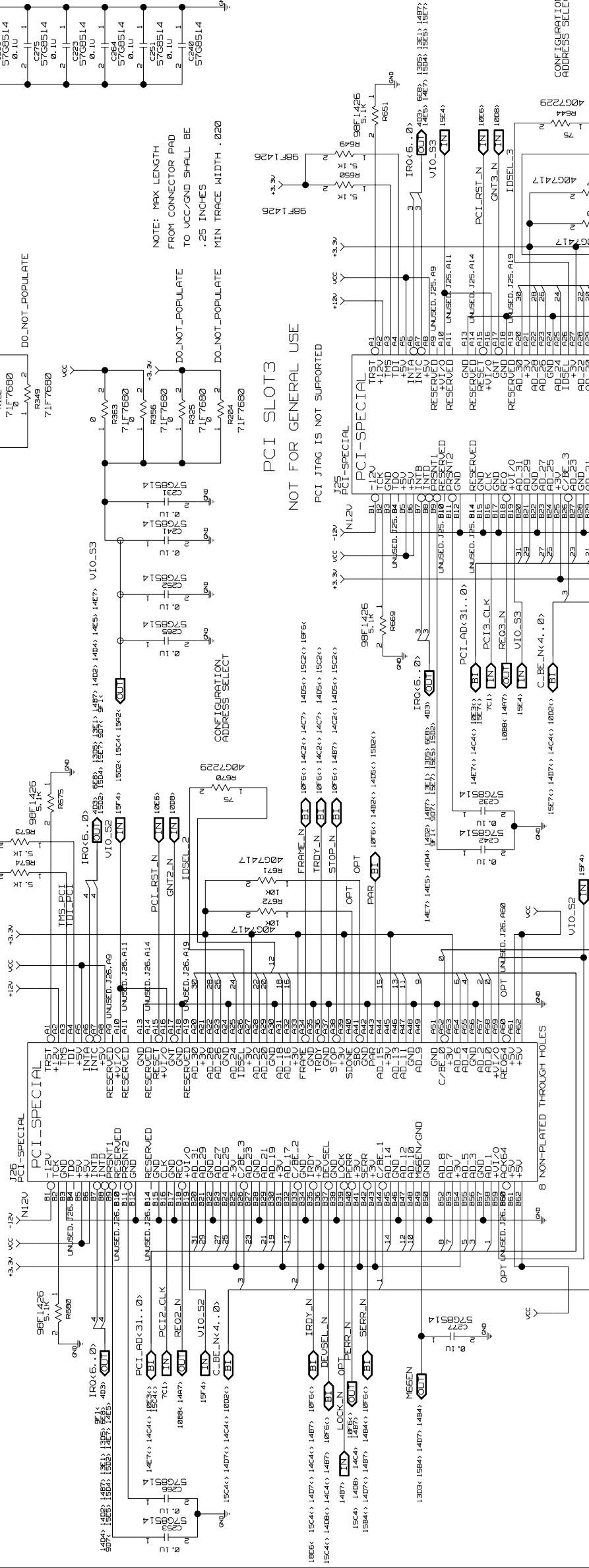


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT5
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

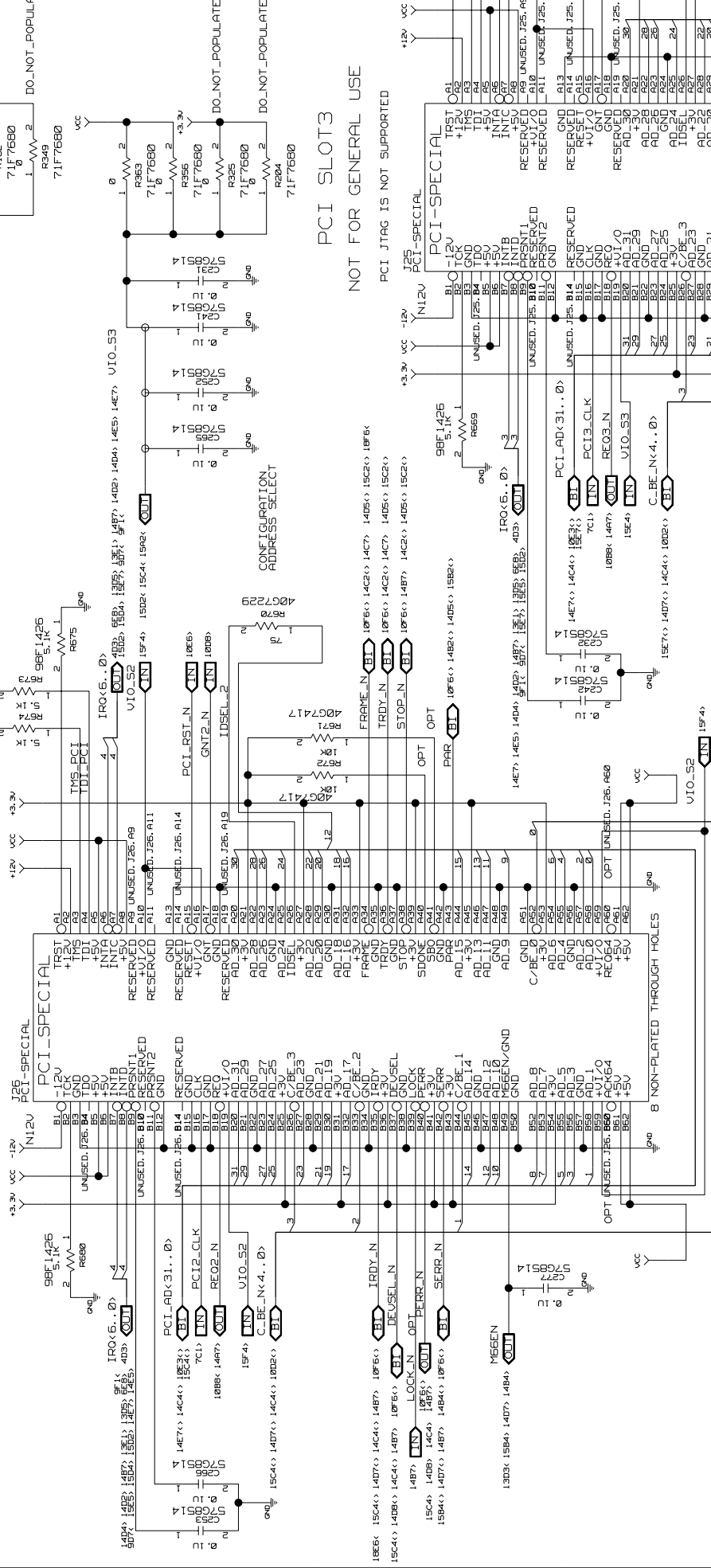


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT6
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

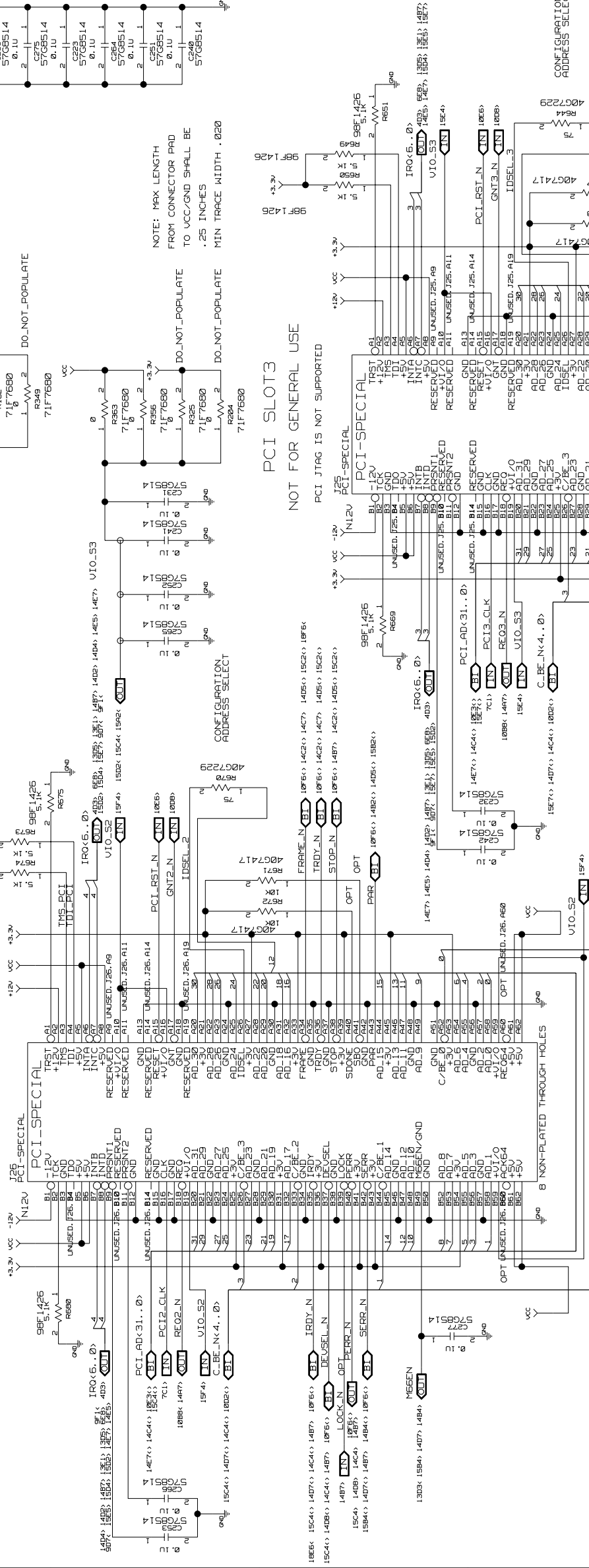


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT7
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED

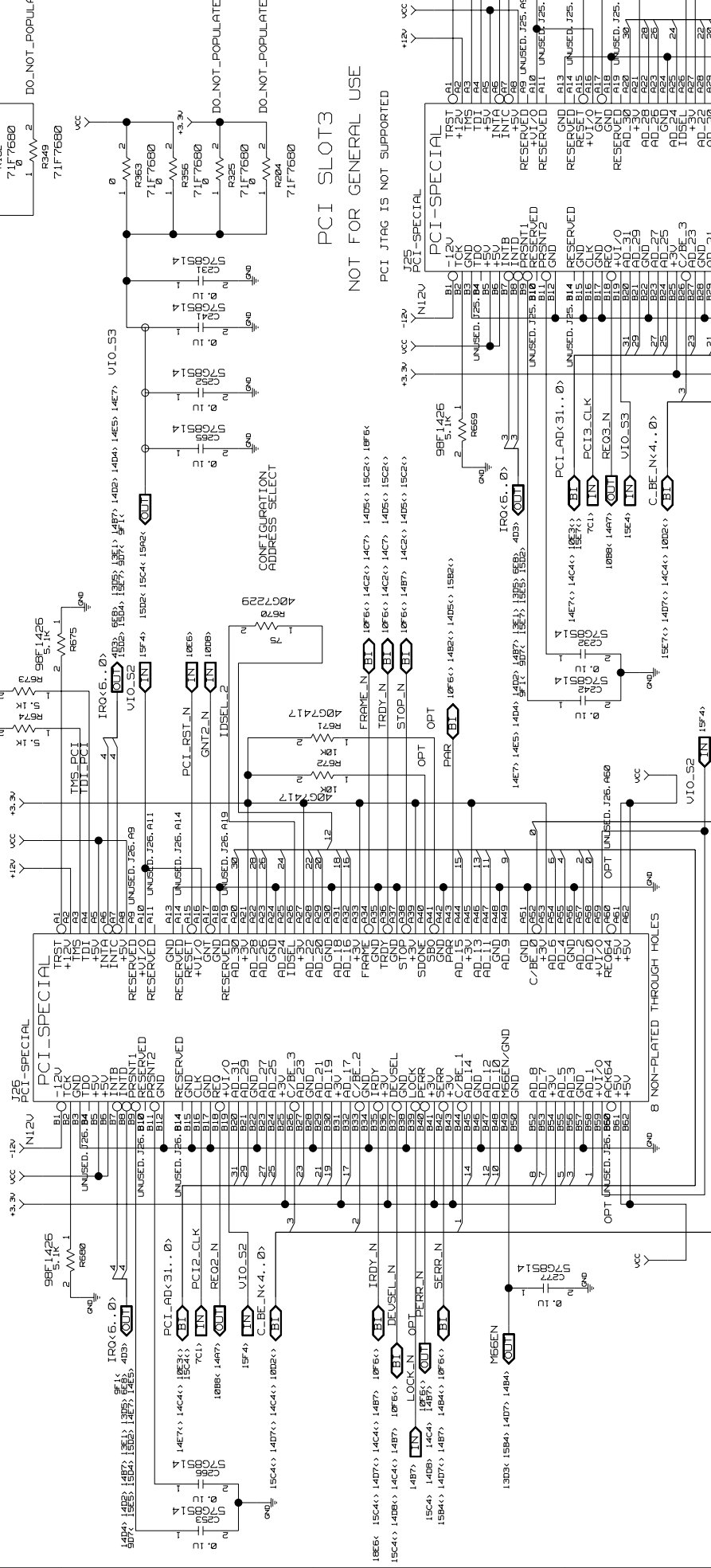


NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

PCI SLOT8
NOT FOR GENERAL USE

PCI JTAG IS NOT SUPPORTED



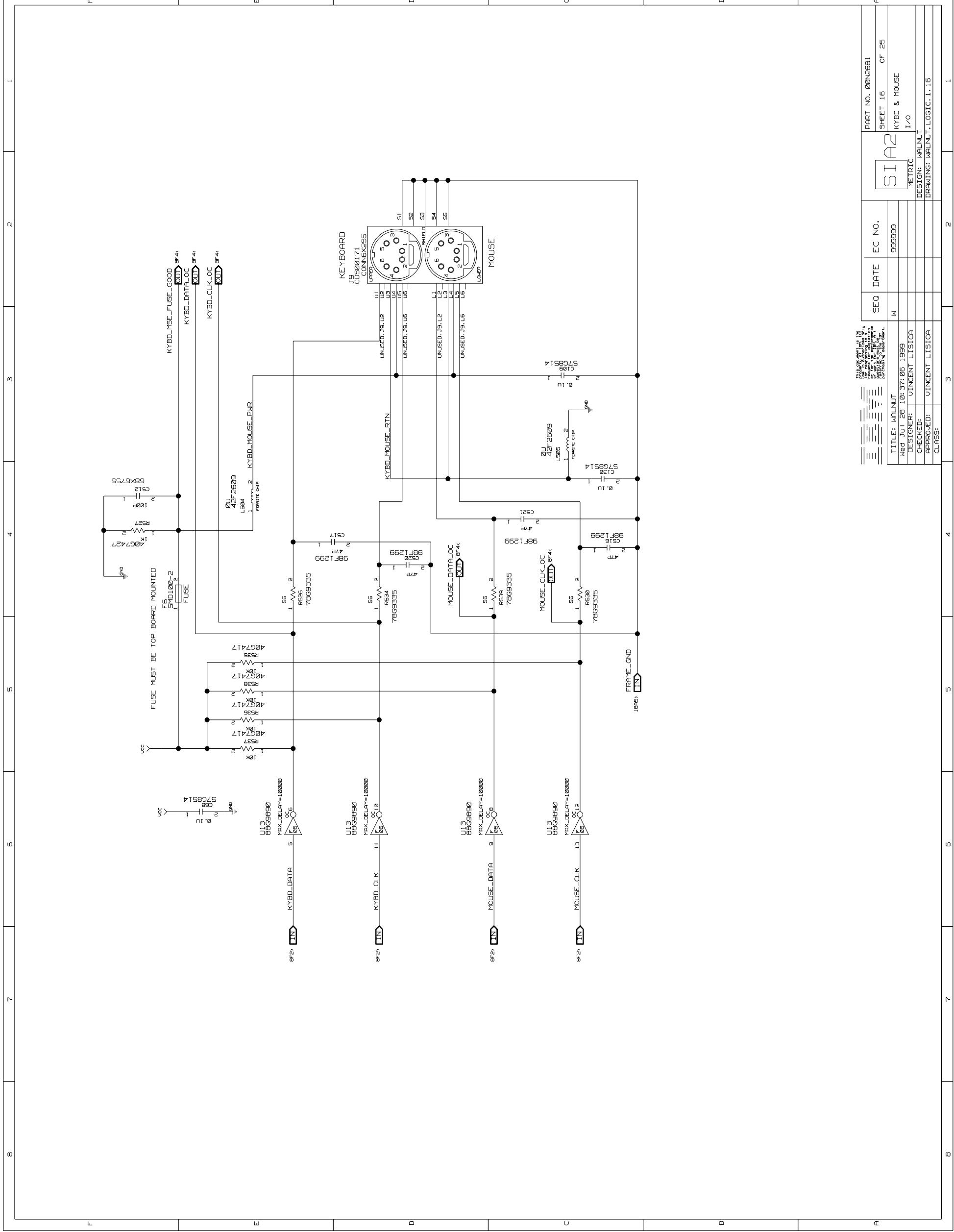
NOTE: MAX LENGTH
FROM CONNECTOR PAD
TO VCC/GND SHALL BE
.25 INCHES
MIN TRACE WIDTH .020

12 CAPS TO BE EVENLY SPACED
AT PCI CONNECTOR

TITLE: WALNUT		DESIGN: WALNUT
DESIGNER: VINCENT LISTICA		CHECKED: VINCENT LISTICA
APPROVED: VINCENT LISTICA		CLASS:
MBO JUN 28 10:37:02 1999		
PART NO. 00N2681		
SHEET 15 OF 25		
PCI SLOTS 2 & 3		



METRIC
DRAWING: WALNUT.LOGIC.1.15

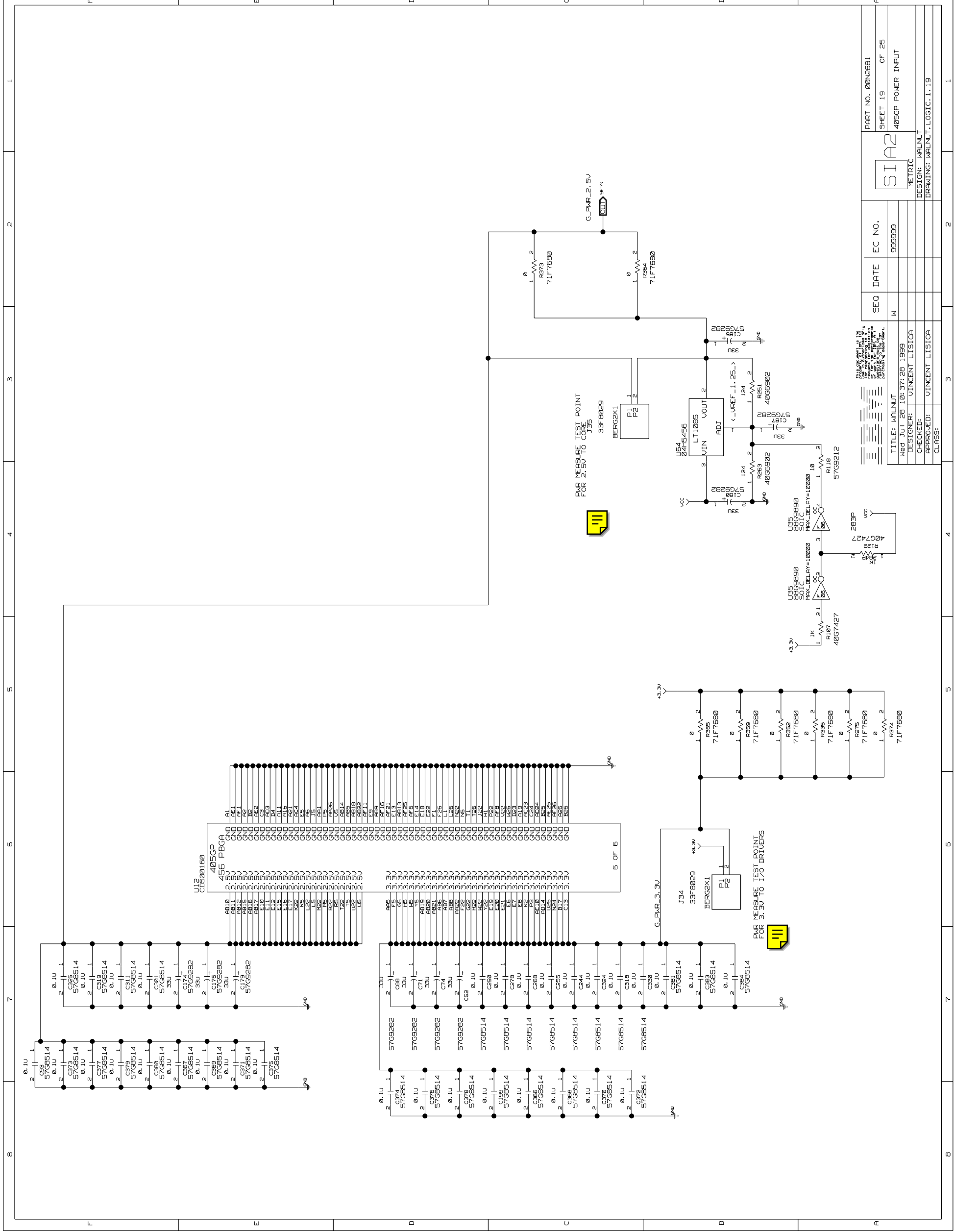


TITLE: WALNUT
 WED JUL 28 10:37:06 1999
 DESIGNER: VINCENT LISTICA
 CHECKED: VINCENT LISTICA
 APPROVED: VINCENT LISTICA
 CLASS:

SEQ	DATE	EC NO.	DESCRIPTION
W		999999	

SIA2
 METRIC
 DESIGN: WALNUT
 DRAWING: WALNUT.LOGIC.1.16

PART NO. 00N2661
SHEET 16 OF 25
KYBD & MOUSE
I/O



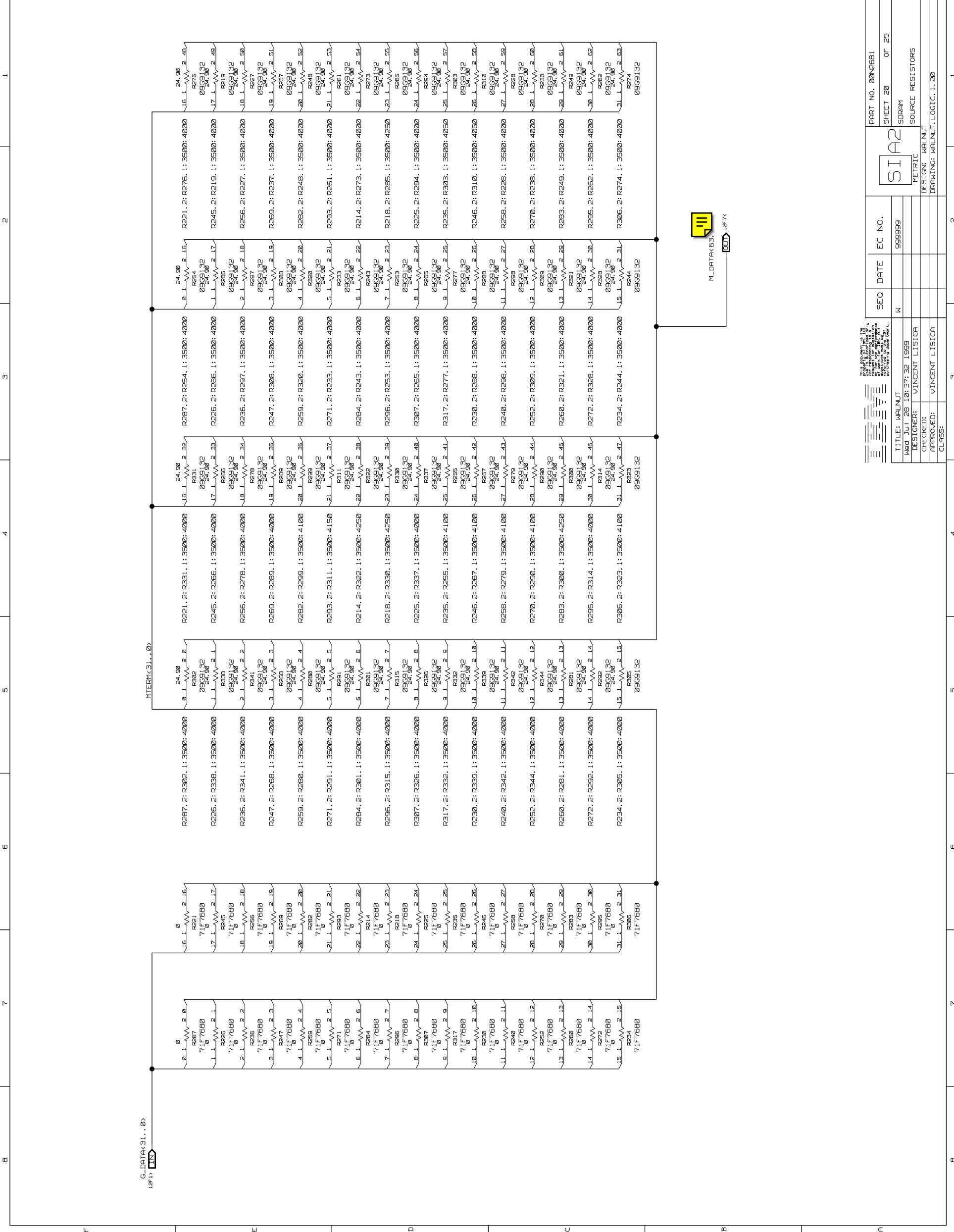
PMR MEASURE TEST POINT
FOR 2.5V TO CORE
J35

PMR MEASURE TEST POINT
FOR 3.5V TO I/O
DRIVERS
J34

U12 405GP
456 PBGA

SIA2

SEQ	DATE	EC NO.	PART NO.
1	14060728	999999	00N2681
TITLE: WALNUT			SHEET 19 OF 25
DESIGNER: VINCENT LISTICA			405GP POWER INPUT
CHECKED: VINCENT LISTICA			METRIC
APPROVED: VINCENT LISTICA			DRAWING: WALNUT.LOGIC.1.19
CLASS:			



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 1ap15

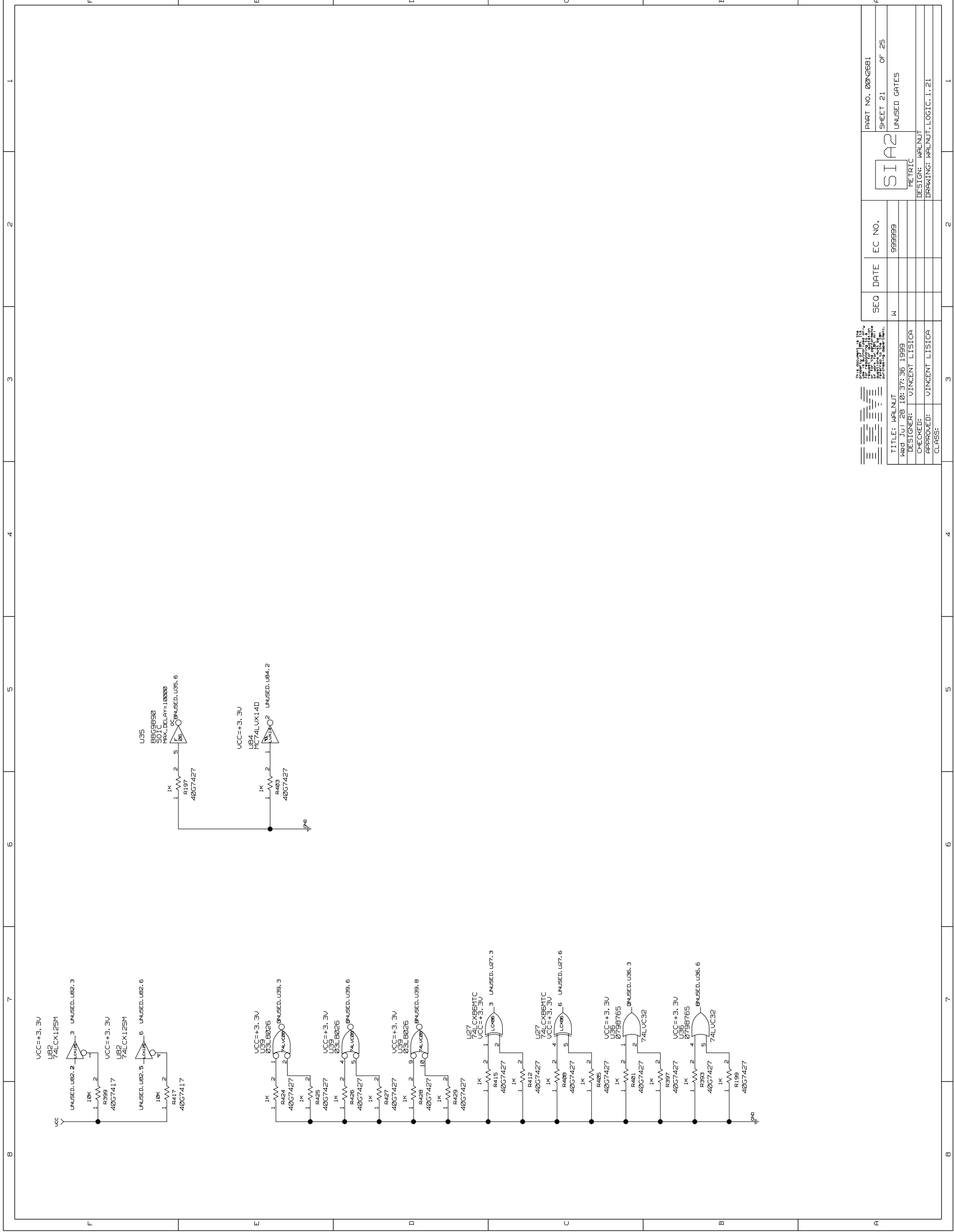
MTERM<31...0>

M-DATA<63...
 1ap74



TITLE: WALNUT
 WED JUN 28 10:37:32 1999
 DESIGNER: VINCENT LISTICA
 CHECKED:
 APPROVED: VINCENT LISTICA
 CLASS:

SEQ	DATE	EC NO.	SIA2	PART NO. 08N2661
W		999999		
			METRIC	SOURCE RESISTORS
			DESIGN: WALNUT	
			DRAWING: WALNUT.LOGIC.1.20	



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TITLE: WALNUT
 WED JUL 28 10:37:36 1999
 DESIGNER: VINCENT LISTICA
 CHECKED: WALNUT
 APPROVED: VINCENT LISTICA
 CLASS:

SEQ	DATE	EC NO.	DESCRIPTION
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2			
3			
4			
5			
6			
7			
8			
9			
10			

SI A2

METRIC

DESIGN: WALNUT
 DRAWING: WALNUT.LOGIC.1.21

PART NO. 00N2681
 SHEET 21 OF 25
 UNUSED GATES

F E D C B A

1 2 3 4 5 6 7 8

F E D C B A

UNSEED.U65.11 7F2<
 UNSEED.U65.12 7F2<
 UNSEED.U65.13 7F2<
 UNSEED.U70.1 17C7<
 UNSEED.U70.2 17C7<
 UNSEED.U70.3 17C7<
 UNSEED.U70.12 17C7<
 UNSEED.U70.13 17C7<
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 UNSEED.U82.6 21F7<
 UNSEED.U84.2 21E5>
 UNSEED.U83.9 17B5<>
 U10.S0 14E7< 14E7< 14F5<
 U10.S1 14E7< 14E7< 14F5<
 U10.S2 15E4< 15E4< 15E4< 15E7<
 U10.S3 15E4< 15E4< 15E4< 15E7<
 -SVALTS.NEG 50B> 5B1< 17C3<

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