Am79C900
Integrated Local Area Communications Controller™ (ILACC™)

Advance Information

Am79C900

Integrated Local Area Communications Controller™ (ILACC™)

Advanced Micro Devices

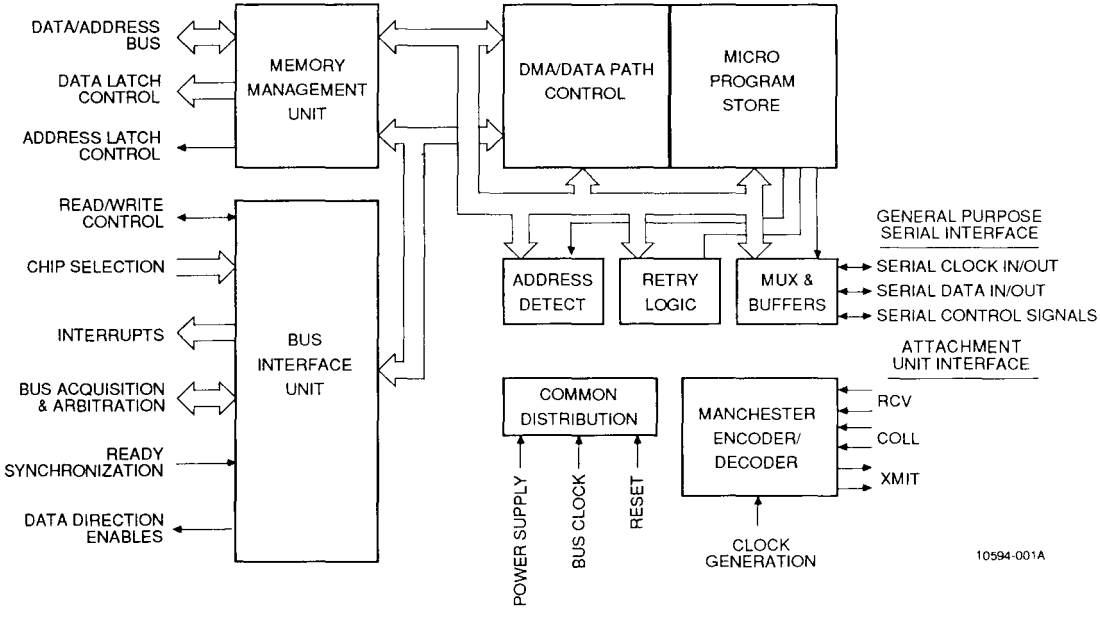
DISTINCTIVE CHARACTERISTICS

- Integrated Ethernet controller and Serial Interface Adapter.
- 32-bit bus interface with programmable capability for easy interface to popular bus architectures such as: 29000, 80X86, 680X0.
- Compatible with Ethernet and ISD 8802-3 ANSI/ IEEE Std. 802.3 10BASE-5, 10BASE-2, 10BASE-T and 10BASE-F.
- On board 48-byte FIFO, DMA controller, and advanced buffer management scheme.
- Split bus and network clock signals supporting 1-10 Mbit/s networks.
- Extensive network diagnostics capabilities including: CRC, loop back, collision retry/runt packet counters, and TDR.
- State of the art CMOS technology and surface mount packaging.

GENERAL DESCRIPTION

The Am79C900 Integrated Local Area Communications Controller (ILACC) is a second generation Ethernet/ 802.3 integrated controller and serial interface encoder/ decoder. The ILACC has been designed to easily interface to popular microprocessor bus architectures through its programmable bus interface. The ILACC's on board DMA controller and its sophisticated buffer management scheme allows the system designer to achieve maximum performance in tightly coupled systems such as PC mother board applications and node processor based adapter cards. In open bus architectures such as personal computer add-on LAN cards the ILACC gives the system designer the flexibility to chose the optimal cost-performance ratio by allowing both inexpensive bus master and shared memory applications. The ILACC will through its AUI interface in conjunction with an external transceiver chip support thick coax, thin coax, twisted pair and fiber optic cable, networking schemes, such as Ethernet and ISO 8802-3 ANSI/IEEE Std. 802.3 10BASE-5, 10BASE-2, 10BASE-T and 10BASE-F.

BLOCK DIAGRAM



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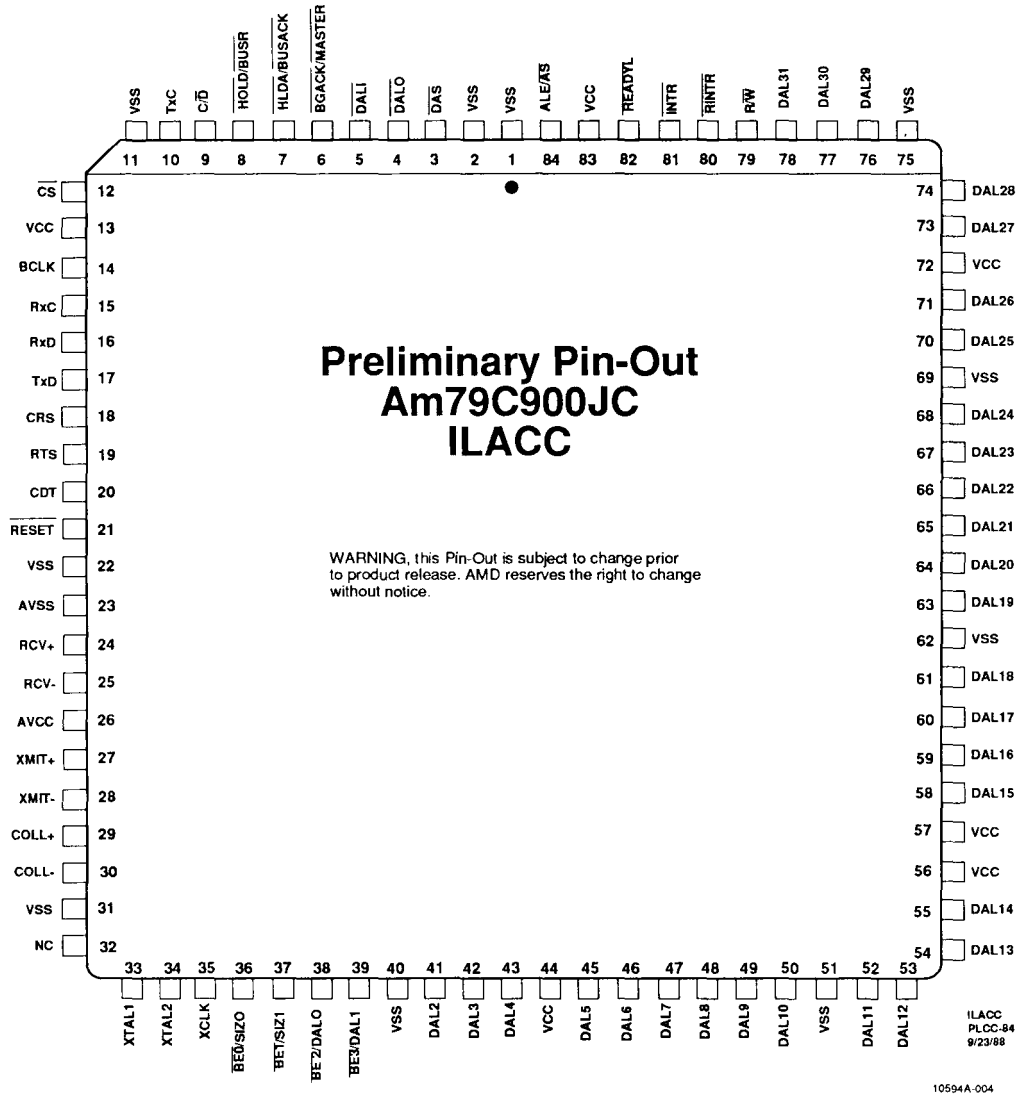
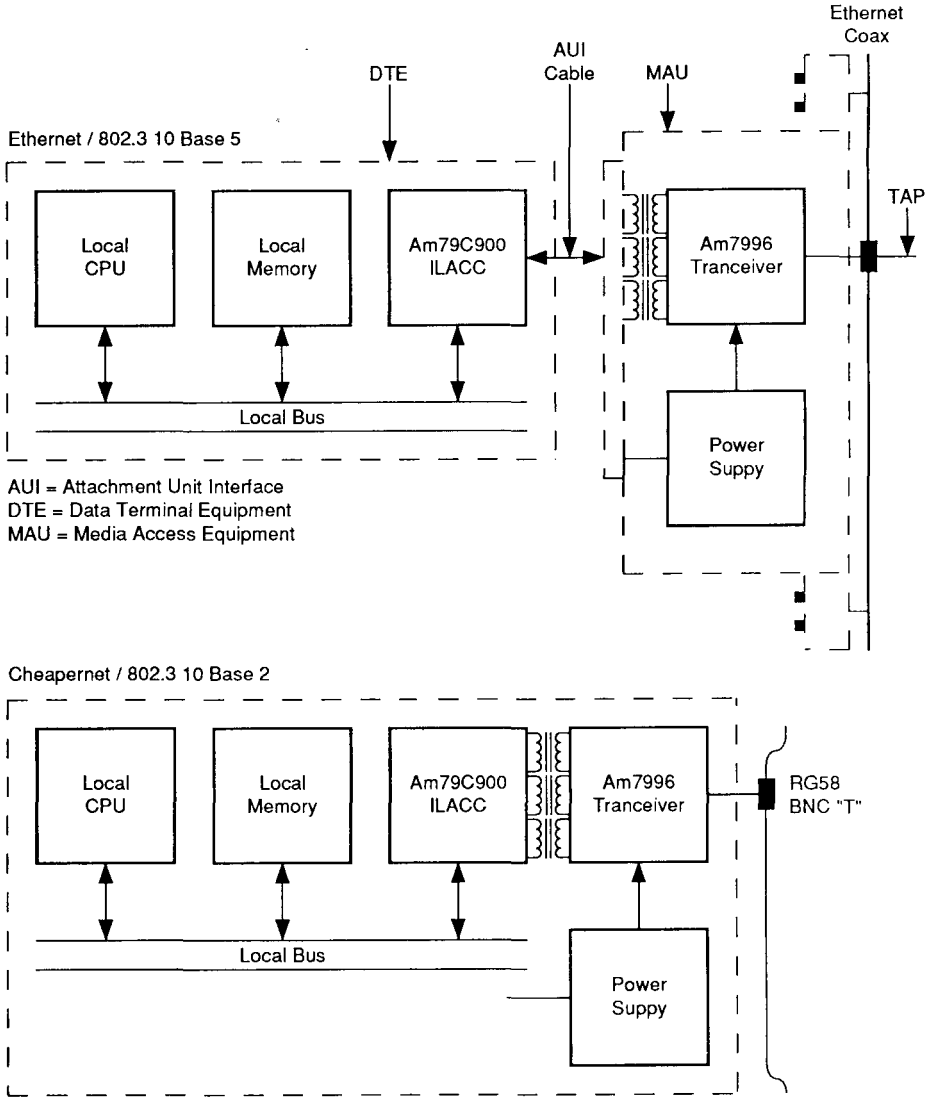
CONNECTION DIAGRAM
Am79C900JC



TYPICAL ETHERNET NODE

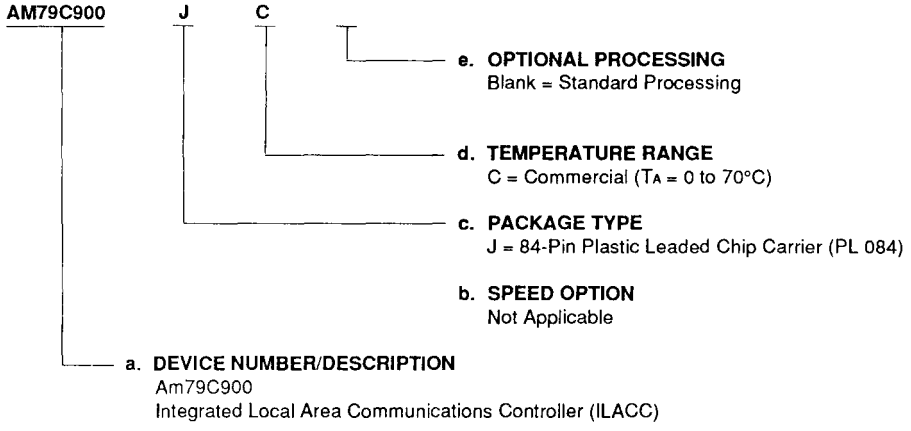


ORDERING INFORMATION

Standard Products

AMD standard products are available in several Packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C900	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

ALE,$\overline{AS}$
Address Latch Enable/Address Strobe (Input/Output, High Impedance)
Used to demultiplex the DAL bus and define the address portion of the memory cycle. $\overline{AS}$ is the logical inversion of ALE. The polarity of the pin is programmable through ACON (CSR3 bit 1) as follows:

ACON = 0: ALE (falling edge latches address).
ACON = 1: $\overline{AS}$ (rising edge latches address).

Used as input during bus arbitration, to detect completion of previous bus master transactions.

BCLK
Bus Clock (Input)
BCLK determines the operating clock rate for the microprocessor interface. The minimum permitted frequency for BCLK must be at least 1.2 times the network data rate, within the range of 2 to 20 MHz. When using the internal SIA, this correlates to 0.6 times the frequency provided at XTAL1/2 (i.e., for a network data rate of 10 Mbits/s, XCLK = 20 MHz, BCLK (min) = 12 MHz, BCLK (max) = 20 MHz).

$\overline{BGACK}$, $\overline{MASTER}$
Bus Grant Acknowledge (Input/Output, Open Drain)
Bus Grant Acknowledge indicates the current bus master (BACON = 01). If the ILACC has requested the bus (asserted $\overline{BUSREQ}$), it must wait until $\overline{BUSACK}$ becomes asserted (indicating the current master will relinquish the bus on completion of its transaction), at which time the ILACC will sample $\overline{BGACK}$, $\overline{DAS}$ and ALE/$\overline{AS}$. If they are in their inactive state (indicating the current master has completed its last cycle and no other device is claiming bus mastership), the ILACC will assert $\overline{BGACK}$. Bus Grant Acknowledge must remain asserted as long as the ILACC remains bus master. Used with 680X0 family of processors.

Master (Output, Open Drain)
Asserted when ILACC is the bus master (BACON=00) to enable data/address bus drivers.

C/$\overline{D}$
Control/Data Select (Input)
Used during slave cycles to determine if the current I/O transaction is transferring control or data information.

C/$\overline{D}$ = 0: Data Port select.
C/$\overline{D}$ = 1: Register Address Port select.

The input is ignored when the ILACC is a bus master.

CDT
Collision Detect (Input)
When asserted, indicates that there is more than one node transmitting on the medium concurrently. CDT is only required when using the general purpose serial interface. CDT should be tied low when using the internal SIA (PORTSEL = 0, CSR15 bit 8).

COLL+
COLL-
Collision Detect (Input)
A differential line input signaling that there is a collision, when operating the integrated SIA. Used in Ethernet/802.3 applications. Operates at pseudo-ECL levels. When using the general purpose serial interface (PORTSEL = 1, CSR15 bit 8), COLL+/- should be tied to ground.

CRS
Carrier Sense (Input)
CRS must be asserted when valid data is being received by an external transceiver connected via the general purpose interface port. CRS is only required when using the general purpose serial interface. CRS should be tied low when using the internal SIA (PORTSEL = 0, CSR15 bit 8).

$\overline{CS}$
ChipSelect(Input)
Used to access the ILACC internal registers, in conjunction with C/$\overline{D}$. Ignored during bus mastership cycles.

DAL_0–DAL_1, $\overline{BE_2}$–$\overline{BE_3}$
Data/Address/Byte enable lines (Input/Output, High Impedance)
For BACON = 00. In master cycles, during the address portion of a memory transfer, the pins function as $\overline{BE_2}$–$\overline{BE_3}$, the memory bank selected signals for an 80X86-type environment. During the data portion of the memory transfer, DAL_0–DAL_1 contain the read or write data, depending on the type of transfer. In slave cycles, these lines operate as data/address lines.

Data/Address lines (Input/Output, High Impedance)
For BACON = 01. In master cycles, during the address portion of a memory transfer, the pins function as A_1 and A_0, the byte offset signals for a 680X0-type environment. During the data portion of the memory transfer, DAL_{0-1} contain the read or write data, depending on the type of transfer. In slave cycles, these lines operate as data/address lines.

DAL_2–DAL_{31}
Data/Address Lines (Input Output, High Impedance)
During the address portion of a memory transfer DAL_2–DAL_{31} contain memory address information. During the data portion of the memory transfer DAL_2–DAL_{31} contain the read or the write data depending on the type of transfer.

$\overline{DALI}$
Data/Address Line In (Output)
An external bus transceiver control line, used to enable the data path into the ILACC. Active in both master and slave cycles.

PIN DESCRIPTION

ALE,$\overline{AS}$
Address Latch Enable/Address Strobe (Input/Output, High Impedance)
Used to demultiplex the DAL bus and define the address portion of the memory cycle. $\overline{AS}$ is the logical inversion of ALE. The polarity of the pin is programmable through ACON (CSR3 bit 1) as follows:

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The input is ignored when the ILACC is a bus master.

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Collision Detect (Input)
When asserted, indicates that there is more than one node transmitting on the medium concurrently. CDT is only required when using the general purpose serial interface. CDT should be tied low when using the internal SIA (PORTSEL = 0, CSR15 bit 8).

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A differential line input signaling that there is a collision, when operating the integrated SIA. Used in Ethernet/802.3 applications. Operates at pseudo-ECL levels. When using the general purpose serial interface (PORTSEL = 1, CSR15 bit 8), COLL+/- should be tied to ground.

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ChipSelect(Input)
Used to access the ILACC internal registers, in conjunction with C/$\overline{D}$. Ignored during bus mastership cycles.

DAL_0–DAL_1, $\overline{BE_2}$–$\overline{BE_3}$
Data/Address/Byte enable lines (Input/Output, High Impedance)
For BACON = 00. In master cycles, during the address portion of a memory transfer, the pins function as $\overline{BE_2}$–$\overline{BE_3}$, the memory bank selected signals for an 80X86-type environment. During the data portion of the memory transfer, DAL_0–DAL_1 contain the read or write data, depending on the type of transfer. In slave cycles, these lines operate as data/address lines.

Data/Address lines (Input/Output, High Impedance)
For BACON = 01. In master cycles, during the address portion of a memory transfer, the pins function as A_1 and A_0, the byte offset signals for a 680X0-type environment. During the data portion of the memory transfer, DAL_{0-1} contain the read or write data, depending on the type of transfer. In slave cycles, these lines operate as data/address lines.

DAL_2–DAL_{31}
Data/Address Lines (Input Output, High Impedance)
During the address portion of a memory transfer DAL_2–DAL_{31} contain memory address information. During the data portion of the memory transfer DAL_2–DAL_{31} contain the read or the write data depending on the type of transfer.

$\overline{DALI}$
Data/Address Line In (Output)
An external bus transceiver control line, used to enable the data path into the ILACC. Active in both master and slave cycles.

DALO
Data/Address Line Out (Output)
An external bus transceiver control line, used to enable the data path away from the ILACC. Active in both master and slave cycles.

DAS
Data Strobe (Input/Output, High Impedance)
Defines the data portion of the bus transfer. Input during bus slave, output during bus master cycles.

HLDA,BUSACK
Hold Acknowledge (Input)
Response from other potential bus masters to indicate they have relinquished bus mastership, in an 80X86-type processor environment (BACON = 00). Any host which allows preemptive DMA may deassert Hold Acknowledge at any time, requiring the ILACC to deassert HOLD .

Bus Acknowledge (Input)
This signal is asserted by the host in response to a Bus Request. When Bus Acknowledge is received in response to the chip's assertion of Bus Request, the ILACC becomes the bus master after ALE/AS, DAS and BGACK are sampled inactive. Intended for use in 680X0-type processor environments (BACON = 01).

HOLD,BUSREQ
Hold (Output, Open Drain)
Asserted by the ILACC to request bus mastership in 80X86 processor configurations. The output can be wire-ORed with other potential bus masters. HOLD will be deasserted by the ILACC within a maximum of five bus cycles, if another master preempts the ILACC (removes HLDA).

Bus Request (Output Open Drain)
Bus Request is asserted when the chip requires the bus for direct memory transfer in 680X0-type processor configurations. The output may be wire-ORed with other potential bus masters.

INTR
Interrupt (Output, Open Drain)
An attention signal that indicates that one or more of the following status flags are set: BABL, MERR, MISS, TINT, IDON (all in CSR0), TXSTRT or LBD (in CSR4). INTR is enabled by IENA = 1 (CSR0 bit 6).

NC
No Connection
Do not connect.

RCV±
Receive Data (Input)
A differential line input to the integrated SIA, for receiving Manchester encoded data from the network. Operates at pseudo-ECL levels. When using the general purpose serial interface (PORTSEL = 1, CSR15 bit 8), RCV ± should be tied to ground.

R/W
Read/Write (Input/Output, High Impedance)
Indicates the direction of data flow to or from the ILACC. An output during bus master cycles, an input during slave cycles.

READYL
Ready Low (Input/Output Open Drain)
When the ILACC is a bus slave, READYL is the output used to request wait states to be inserted in host read/write operations. When the ILACC is a bus master, READYL is the input acknowledge from target memory to indicate it will accept data in a write cycle, or that valid data is available on the DAL bus in a read cycle.

RESET
System Reset (Input)
Reset clears the internal logic. All outputs go to their high impedance state or are driven inactive. All bus-related outputs are high impedance until the Initialize command is given by the host.

RINTR
Receive Interrupt (Output, Open Drain)
When active, indicates that RINT in CSR0 is set (bit 10). RINTR is enabled by INEA (CSR0 bit 6). Receive interrupts can be masked by setting the mask bit RINTM in CSR3 (bit 7). RINTR will remain asserted until RINT is cleared, RINTM is set, or INEA is cleared. RINT set in CSR0 does not cause the external INTR to become asserted, although the INTR summary bit in CSR0 will be set, providing RINTM in CSR3 is clear.

RTS
Request To Send (Output)
RTS is asserted when the chip wishes access to the channel. RTS remains asserted during the transmission cycle. RTS will only be activated by the ILACC if the general purpose serial interface has been selected. RTS should be left unconnected if the integral SIA has been selected (PORTSEL = 0, CSR15 bit 8).

RxC
Receive Clock (Input)
The receive data clock; operates at the network data rate. Only required if the general purpose serial interface has been selected. Input frequency range from 1 to 10 MHz is permitted. RxC should be tied low if the internal SIA has been selected (PORTSEL = 0, CSR15 bit 8).

RxD
Receive Data (Input)
The receive serial data path to the general purpose serial interface. Serial data presented on this input will be clocked into the ILACC by the positive edge of the RxC. RxC should be tied low when using the internal SIA (PORTSEL=0, CSR15 bit 8).

SIZ_0–SIZ_1, $\overline{BE_0}$–$\overline{BE_1}$
Size (Output, High Impedance)
With BACON = 01, SIZ_0 and SIZ_1 are produced for 680X0 or Am29000 environments.

Byte Enable (Output, High Impedance)
With BACON = 00 , these lines become $\overline{BE_0}$ and $\overline{BE_1}$ (DAL_0 and DAL_1 become BYTE ENABLE 2 and 3 respectively). These signals are used for the 80X86 interface.

TxC
Transmit Clock (Input)
The transmit data clock, operates at the network data rate. Only required if the general purpose serial interface has been selected. Input frequency range from 1 to 10 MHz is permitted. TxC should be tied low if the internal SIA has been selected (PORTSEL = 0, CSR15 bit 8).

TxD
Transmit Data (Output)
The transmit serial data path. Only activated by the ILACC if the general purpose serial interface has been selected. The ILACC will clock out serial data onto TxD on the positive edge of TxC. TxD should be left unconnected if the internal SIA has been selected (PORTSEL = 0, CSR15 bit 8).

VCC
Power supply (6 pins)
+5 V supply for internal interface logic and I/O pin driver functions.

VSS
Ground (10 pins).
0 V reference for internal interface logic and I/O pin driver functions.

AVCC
Analog Power supply
+5 V supply for the analog functions of the internal SIA. This supply should be separated from the digital V_{CC} supplies as far back to the system power supply as practical.

AVSS
Analog Ground Reference
0 V reference for the analog functions of the internal SIA. This ground reference should be separated from the digital V_{SS} supplies as far back to the system power supply as practical.

XCLK
Clock (Output)
XCLK is derived from the crystal oscillator. It can be used as the input to BCLK. Frequency range for XCLK is 2 to 20 MHz.

XMIT+
XMIT-
Transmit Data (Output)
A differential line output for transmitting Manchester encoded data from the integrated SIA. Operates at pseudo-ECL levels. When using the general purpose serial interface port (PORTSEL = 1, CSR15 bit 8), XMIT+ should be left unconnected.

XTAL1
XTAL2
Crystal Oscillator (Input)
The crystal frequency determines the network data rate. When using an external crystal, two 100-pF capacitors are required, between XTAL1 and ground and XTAL2 and ground. XTAL1 may be driven from an external source, in which case XTAL2 must be left floating. Frequency range is 2 to 20 MHz. When using the internal SIA, the network data rate will be one half of the external crystal frequency. The frequency at XTAL1 cannot run faster than 1.67 times the frequency at BCLK.

FUNCTIONAL DESCRIPTION

General

The Am79C900 (ILACC) is designed to operate in an environment that allows close coupling with a local memory and/or microprocessor (host), or alternately it can reside on a system bus and act as an intelligent bus master device.

The ILACC is programmed by a combination of registers resident within the chip, and data structures located in user memory. There are 59 user-accessible Control and Status Registers (CSRs) within the chip. The host is responsible for initial programming of a small subset. Once enabled, the ILACC accesses memory directly to acquire additional operating parameters.

The Am79C900 has the ability to perform independent buffer management as well as transfer data packets to and from the network. There are three memory structures accessed by the chip:

1. **Initialization Block** – Seven 32-bit entries in memory starting on a long word boundary. It contains the parameters necessary for device operation. The Initialization Block is comprised of:
   - Mode of Operation
   - Physical Address
   - Logical Address Filter
   - Pointers to Receive and Transmit Descriptor Rings
   - Number of Entries in Receive and Transmit Descriptor Rings
2. **Receive and Transmit Descriptor Rings** – Two contiguous ring structures in memory, for control of Receive and Transmit packets. The descriptor rings are comprised of:
   - The address of a data buffer
   - Status and error information associated with the buffer
   - The length of the data buffer
3. **Data buffers** – Area(s) of memory reserved for packet buffering. Data buffers may begin on arbitrary word boundaries. Each buffer must be contiguous in memory, although multiple buffers can be located anywhere in addressable memory.

   In general the programming sequence of the ILACC may be summarized as:

1. Program the ILACC's CSRs to locate the Initialization Block in memory. The byte control, byte addressing, address latch enable and bus arbitration modes are also defined.
2. Define the byte control, byte addressing, address latch, and bus arbitration.
3. Fetch the Initialization Block via DMA.
4. Access the descriptor rings and data buffers for packet handling.

The parallel interface of the ILACC has been designed to be easily interfaced to a variety of popular 32-bit microprocessor buses; examples include the 80X86, 680X0 and AMD 29000 series. The ILACC is user-configurable so that it directly interfaces to the bus arbitration schemes of the above architectures.

The ILACC has a 32-bit wide linear address space when acting as Bus Master, allowing it to DMA directly into the entire address space of the above microprocessors and system buses.

Interrupts to the processor are generated by the ILACC upon:

1. Completion of ILACC's Initialization routine
2. The reception of a packet
3. Start of transmit packet
4. Completion of transmit activity
5. A transmitter time-out error
6. A missed packet
7. A memory error
8. Completion of a loopback test

The cause of interrupt is determined by reading CSR0 and/or CSR4. Bit 6 of CSR0 (INEA) enables or disables interrupts to the host. In systems where polling is used in place of interrupts, bit 7 of CSR0 (INTR) indicates an interrupt condition.

The basic operation of the ILACC consists of two distinct modes: transmit and receive. In the transmit mode, the ILACC directly addresses data in a transmit buffer in memory. It prefaces the data with a preamble and synchronization pattern, and calculates and appends a 32-bit CRC. This packet is then Manchester encoded by the internal SIA, or sent out in NRZ format with clock, depending on which transceiver port is selected.

In the receive mode, packets are received via the external transceiver and passed to either the SIA port or the general purpose serial interface of the ILACC. If the internal SIA is used, clock and data separation occur and the packet is loaded into buffer memory. If the general purpose interface is used, clock and data separation must occur externally. A CRC is calculated for the received packet and compared with the CRC appended to the data packet. If the calculated CRC does not agree with the packet CRC, an error bit is set.

ILACC Bus Configurations

The ILACC supports a 32-bit data and address bus. Memory byte selection during ILACC bus mastership can be software-programmed according to the target microprocessor using the BACON bits. Arbitration schemes for 80X86 and the 680X0 are supported.

Bus Cycles

Depending on the operation, the ILACC can function as a bus slave (memory or I/O mapped) or as a bus master (DMA) device.

BUS SLAVE CYCLES

Slave cycles are executed by the host system on the ILACC, to program the initial conditions of the device or to examine its state during operation.

The host can gain read or write access to the ILACC's internal Control and Status Registers (CSRs) by asserting the $\overline{CS}$ line ($\overline{CS}$ = 0), causing the ILACC to enter the bus slave mode. The CSRs are accessed in a two-stage process. The host must first write the address of the register to be accessed into the Register Address Pointer (RAP). The host can subsequently perform read or write operations on the register addressed by the contents of RAP by accessing the Data Port.

RAP or Data Port selection is performed using the C/$\overline{D}$ input pin (C/$\overline{D}$ = 1 for RAP access). For more details, see the heading "User Programmable Registers."

All slave accesses to/from the ILACC's internal CSRs take place over DAL_{0-15}. The high order address and data bus lines (DAL_{16-31}) are undefined during slave operation.

Read Sequence

At the beginning of the read cycle, $\overline{CS}$, C/$\overline{D}$ and R/$\overline{W}$ are asserted by the host. The host will assert $\overline{DAS}$, which will latch both the read request and the state of C/$\overline{D}$ within the ILACC. R/$\overline{W}$ and C/$\overline{D}$ need not be active for the remainder of the cycle. The ILACC will subsequently assert $\overline{DALO}$ to enable the external output bus transceiver(s). If C/$\overline{D}$ was latched as a "1", the contents of RAP will be placed on the DAL bus. If C/$\overline{D}$ was a "0", the contents of the CSR addressed by RAP will be placed on the DAL bus. After the data on DAL_{0-31} becomes valid, the ILACC asserts $\overline{READYL}$, signalling the host to strobe in the data using the rising edge of $\overline{DAS}$, and relinquish $\overline{CS}$. The ILACC subsequently releases $\overline{DALO}$, $\overline{READYL}$ and the DAL bus. $\overline{CS}$ and $\overline{DAS}$ must be valid during the entire slave read cycle.

Write Sequence

At the beginning of the write cycle, $\overline{CS}$, C/$\overline{D}$ and R/$\overline{W}$ are asserted by the host. The host will assert $\overline{DAS}$, which will latch both the write request and the state of C/$\overline{D}$ within the ILACC. R/$\overline{W}$ and C/$\overline{D}$ need not be active for the remainder of the cycle. The ILACC will subsequently assert $\overline{DALI}$ to enable the external input bus transceiver(s). The host will output the write data on DAL_{0-31}. If C/$\overline{D}$ was latched as a "1", the contents of the DAL bus will be written to RAP. If C/$\overline{D}$ was a "0", the contents of the DAL bus will be written to the CSR addressed by the RAP. When the ILACC asserts $\overline{READYL}$, the host strobes the data into the ILACC using the rising edge of $\overline{DAS}$, and subsequently releases the $\overline{CS}$ line and the DAL bus. The ILACC will deassert $\overline{DALI}$ and $\overline{READYL}$ in response to $\overline{DAS}$ going inactive. $\overline{CS}$ and $\overline{DAS}$ must be valid during the entire slave write cycle.

BUS ACQUISITION

The ILACC bus acquisition mechanism can be optimized to suit common two- or three-wire bus arbitration schemes, using the Bus Acquisition Control (BACON) bits in CSR4, as defined below:

BACON	Bus Configuration
00	80X86
01	680X0
10	RESERVED
11	RESERVED

For 80X86-type processors, bus acquisition is controlled with a two-wire handshake of $\overline{HOLD}$ (HOLD REQUEST) and $\overline{HLDA}$ (HOLD ACKNOWLEDGE). If BACON = 00 (80X86 operation), the burst transfer may be preempted by the host or system arbiter deasserting the $\overline{HLDA}$ line. The ILACC will complete its current bus transaction before relinquishing the $\overline{HOLD}$ request.

For 680X0-type processors, bus acquisition is controlled with a three-wire handshake of $\overline{BUSREQ}$ (BUS REQUEST), $\overline{BUSACK}$ (BUS ACKNOWLEDGE) and $\overline{BGACK}$ (BUS GRANT ACKNOWLEDGE). Preemption is not supported in this configuration.

The ILACC will request the bus to enable the movement of a receive packet into the receive buffer area, or to check for the presence of a transmit message and to move it from the transmit buffer area if required.

If there are 16 bytes or more empty in the FIFO in transmit mode, or at least 16 bytes of data in the FIFO in receive mode, when the ILACC releases the bus ($\overline{HOLD}$ or $\overline{BGACK}$ deasserted), it will request the bus again within 4 bus clock periods for receive, or 10 bus clock periods for transmit.

BUS MASTER CYCLES (ILACC DMA TRANSFERS)

The ILACC will initiate DMA transfers according to the type of operation being performed. All DMA transfers will fall into the following catagories:

- Single-cycle DMA
- Dua-cycle DMA
- Burst-cycle DMA

Single-Cycle DMA Transfers

Once the ILACC has been granted bus mastership, it will issue a single long-word memory address, and perform the read or write operation on the location, with appropriate output signals to indicate selection of the active data bytes during the transfer. On completion of the transfer, the ILACC will relinquish bus mastership.

Dual-Cycle DMA Transfers

Once the ILACC has been granted bus mastership, it will perform two data transfer cycles before relinquishing the bus. It will issue the long-word memory address of the first location, and perform the read/write operation, supplying appropriate output signals to indicate selection of the active data bytes before executing the second transfer in a similar manner and relinquishing the bus. The two transfers within the mastership period will always be of the same type (either both read or both write), but may or may not be to contiguous addresses. Dual-cycle DMA transfers cannot be preempted.

Burst-Cycle DMA Transfers

Once the ILACC has been granted bus mastership, it will perform a series of consecutive data transfer cycles before relinquishing the bus. Each data transfer will be performed sequentially, with the issue of the long-word address, and the transfer of the data with appropriate output signals to indicate selection of the active data bytes during the transfer. All transfers within the mastership cycle will be either read or write cycles, and will be to contiguous long-word addresses. The number of data transfer cycles within the burst is dependent on the programming of the DMAPLUS option (CSR4, bit 14). If DMAPLUS = 0, a maximum of four transfers will be performed. If DMAPLUS = 1, the burst will continue until the FIFO is filled to its high threshold (transmit operation) or emptied to its low threshold (receive operation). The exact number of transfer cycles in this case will be dependent on the latency of the system bus to the ILACC's mastership request ($\overline{HOLD}$/BUSREQ to $\overline{HLDA}$/$\overline{BGACK}$ delay) and the speed of bus operation. The burst cycle may be preempted when using the 80X86 mode of operation by removing the mastership privilege ($\overline{HLDA}$ = HIGH). The ILACC will complete the current read or write cycle before returning the mastership request inactive ($\overline{HOLD}$ = HIGH).

BUS MASTER TRANSACTIONS

Transactions during ILACC bus mastership consist of use of the allowable DMA cycle types as previously defined and the type of memory transaction being performed. Bus transactions fall into one of the following three catagories :

- Initialization block read access
- Descriptor read/write access
- Data buffer read/write access

Initialization Block Access

This transaction reads all 7 long-words (28 bytes) of the Initialization Block.

Data is read from the Initialization Block as a sequence of four separate arbitration/relinquish cycles. The first three exchanges will be performed as dual-cycle DMA transfers, performing two contiguous long-word reads, commencing at the base address programmed in CSR1 and CSR2. This sequence continues until the fourth cycle, which will perform a single-cycle DMA transfer, to read the last long-word entry in the Initialization Block. The time between each mastership cycle may vary if another device is also contending for bus mastership during the initialization sequence. The ILACC will always complete the 2 long-word read operations within the bus mastership period, even if preempted.

Initialization Block entries are not byte-swapped, regardless of target configuration. The internal ILACC registers read in the memory-based initialization parameters on the basis that bit 31 of the memory location is the high order bit of the word.

The base location of the Initialization Block is constrained to be on an even word boundary. Bits 0 and 1 of CSR1 must be zero.

Descriptor Access

These transactions read and write the appropriate entries of the transmit and receive descriptor rings to manage the transfer of transmit buffers to the network and messages from the network to the receive buffers.

Accesses to descriptor entries are performed by only two methods:

1. A single-cycle DMA transfer is used to examine the OWN bit or modify the status in the transmit or receive descriptor (TMD1[31-24], RMD1[31-24]). If ownership is established, a separate single-cycle DMA transfer will be used to read the address of the buffer (TMD2 or RMD2).

   For chained buffers (multiple descriptors/buffers containing a single message), a single-cycle write will be used to update the transmit or receive descriptor status (TMD1 or RMD1) of all but the last descriptor in the chain.

2. A dual-cycle DMA transfer will be performed on a transmit descriptor, if a condition is detected which requires both status (TMD1) and error (TMD2) conditions to be reported. Transmit descriptors will only be updated with a dual-cycle DMA transfer if an error condition is reported and the descriptor is the last or only entry in the transmit chain.

   A dual-cycle DMA write will be used on receive descriptors on completion of the receive packet to update the status (RMD1) and report the message length (RMD2) and/or error conditions. Receive descriptors will only be updated with a dual-cycle DMA transfer, if the descriptor is the last or only entry in the receive chain.

Note that during all descriptor read operations, the entire data bus will be activated, as if a full long-word data fetch were being performed. The ILACC will internally route and use only the required data, and discard any superfluous information fields. For write cycles, only the appropriate data bus bytes are activated, to ensure adjacent memory locations are not corrupted.

Descriptor entries are not byte swapped, regardless of target configuration. The internal ILACC registers read in the memory-based initialization parameters on the basis that bit 31 of the memory location is the high order bit of the word.

Descriptors must be constrained to be on 16-byte boundary, as defined by the TRANSMIT/RECEIVE DESCRIPTOR RING ADDRESS fields (TDRA and RDRA), within the Initialization Block (TDRA[3-0] = 0, RDRA[3-0] = 0). Hence all descriptor entries will appear on long-word boundaries to the ILACC.

Data Buffer Access

Burst-cycle DMA is used to read transmit buffer information and transfer it to the FIFO, or to write receive message information from the FIFO to the receive buffer area.

Accesses to buffer entries are performed by only two burst mechanisms:

1. If DMAPLUS = 0 (CSR4, bit 14), the burst transfer will consist of up to four read/write cycles, providing the ILACC is not preempted (applicable to 80X86 mode only). If the ILACC is preempted, it will complete its current read/write transfer, before relinquishing mastership.

2. If DMAPLUS = 1, burst transfers continue until the FIFO is filled to its high threshold, or emptied to its low threshold, within a single DMA burst cycle (unless preempted). If the ILACC is preempted, it will complete its current read/write transfer, before relinquishing mastership.

To maximize system bus bandwidth, the ILACC will always use its first DMA transfer to or from a buffer, to long-word align its remaining transfers. For example, if the buffer is located on an odd-word boundary (A1 = 1, A0 = 0), the first DMA transfer will read or write 1 word (2 bytes) of data. Subsequent cycles will DMA long-word data (4 bytes) since the addresses will now be long-word aligned (A1 = 0, A0 = 0); until the burst is complete, or less than 4 data bytes remain to be DMAed.

In the case where less than 4 bytes remain to be transferred to/from a buffer, the ILACC will read data from or write data to the appropriate bytes of the data bus, in accordance with the relevant host processor addressing convention.

Note that during all buffer read operations, the entire data bus will be activated, as if a full long-word data fetch were being performed. The ILACC will internally route and use only the required data, and discard any superfluous information fields. For write cycles, only the appropriate data bus bytes are activated, to ensure adjacent memory locations are not corrupted.

Buffer data will be byte swapped according to the target memory architecture, due to the byte orientation of the 802.3 protocol ("little-endien"). Data is transferred across the network in byte-ascending order (i.e., starting with byte 0, then byte 1, 2, 3, etc.).

There are a number of additional restrictions which apply to transmit and receive buffers:

1. Buffers must commence on word boundaries (A0 = 0), as defined by the transmit/receive message buffer pointer (ADR[0] = 0 in TMD0 or RMD0).

2. The BUFFER BYTE COUNT for receive buffers should always be an even number of bytes (BCNT in RMD1), and must be a minimum of 64 bytes.

3. The MESSAGE BYTE COUNT for receive buffers (MCNT in RMD2) will contain the exact number of bytes received in the packet, and is written by the ILACC in the last receive descriptor table entry (DTE) for the message (valid where the ENP bit is set in RMD1, and assuming ERR is clear).

4. The BUFFER BYTE COUNT (BCNT in TMD1) for the first buffer in a chained transmit packet must be a minimum of 116 bytes if DMAPLUS (CSR4[14]) is set, or 100 bytes minimum if DMAPLUS is reset. Note that BCNT should be an even number of bytes, except in the case where it refers to the last, or only, buffer in a chain.

Note that 80X86 type processors have bus transfer restrictions, namely:

(i) that a single 3-byte transfer will not be observed, without an accompanying byte cycle either before or after.

(ii) misaligned transfers will move the data at the high addressed long-word location first, then decrement to the previous long-word location to complete the transfer.

These restrictions do not apply to the ILACC even when configured for the 80X86 interface. 3-byte cycles can be observed (i.e., at the end of a buffer), and the ILACC will transfer data logically, incrementing to each long word location, and performing the appropriate transfer.

Detailed Description of Bus Signals

Bus Acquisition

All data transfers from the ILACC during bus mastership are timed by ALE/$\overline{AS}$ or $\overline{DAS}$, and $\overline{READYL}$. The automatic adjustment of the ILACC cycle by the $\overline{READYL}$ signal allows synchronization with variable cycle time memory. Bus cycles are a minimum of $4.T_{BCLK}$ cycles and can be increased in $1.T_{BCLK}$ increments.

$\overline{DALI}$ and $\overline{DALO}$ are used to control external bus transceivers. $\overline{DALI}$ is used to enable the data path toward the ILACC, $\overline{DALO}$ to enable the data path away from the ILACC.

Read Sequence

The read cycle is commenced by placing valid addresses on DAL_{0-31} for the 680X0 mode, or DAL_{2-31} for the 80X86 mode. The appropriate byte transfer signals (A_{0-1} and SIZ_{0-1} for the 680X0 mode; $\overline{BE}_{0-3}$ for the 80X86 mode) are asserted to indicate the active data bus width. The R/$\overline{W}$ signal is driven HIGH to indicate a read cycle. The ALE/$\overline{AS}$ pulse allows the external latch to load and store the long-word address. The DAL lines go into a high impedance state and $\overline{DAS}$ falls low to signal the start of the memory access. $\overline{DALI}$ is activated by the ILACC to enable the external input bus transceiver(s). The memory responds by asserting the $\overline{READYL}$ input to the ILACC, to indicate that DAL_{0-31} have valid data. The ILACC latches the memory data on the rising edge of $\overline{DAS}$, which in turn ends the memory cycle.

Write Sequence

The write cycle is very similar except the write transfer is indicated by R/$\overline{W}$ being driven LOW. The DAL_{0-31} lines change from containing addresses to data after ALE/$\overline{AS}$ goes inactive. $\overline{DALO}$ is used to enable the ILACC data onto the data bus. Data to memory is held valid after $\overline{DAS}$ goes inactive.

SUMMARY OF 32-BIT MEMORY TRANSFERS

From the cases outlined previously, the following set of 32-bit bus transfer conditions are required.

Initialization Block :

LONG-WORD TRANSFER FROM EVEN-WORD ADDRESS

Example: Normal 32-bit Initialization Block entry read.

680X0: SIZ1=0, SIZ0=0, A1=0, A0=0

MS	byte	from	DAL <31:24>
	byte	from	DAL <23:16>
	byte	from	DAL <15:08>
LS	byte	from	DAL <07:00>

80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0

MS	byte	from	DAL <31:24>
	byte	from	DAL <23:16>
	byte	from	DAL <15:08>
LS	byte	from	DAL <07:00>

Transmit/Receive Descriptors :

LONG-WORD TRANSFER TO/FROM EVEN-WORD ADDRESS

Example: Normal 32-bit descriptor access.

680X0: SIZ1=0, SIZ0=0, A1=0, A0=0

MS	byte	to/from	DAL <31:24>
	byte	to/from	DAL <23:16>
	byte	to/from	DAL <15:08>
LS	byte	to/from	DAL <07:00>

80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0

MS	byte	to/from	DAL <31:24>
	byte	to/from	DAL <23:16>
	byte	to/from	DAL <15:08>
LS	byte	to/from	DAL <07:00>

BYTE TRANSFER FROM EVEN-WORD ADDRESS

Example: Read status from RMD1/TMD1.

680X0: SIZ1=0, SIZ0=0, A1=0, A0=0

MS byte from DAL <31:24>

80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0

MS byte from DAL <31:24>

Note: Although all bytes are active, only required bytes are used internally.

BYTE TRANSFER TO EVEN-WORD ADDRESS

Example: Write status to RMD1/TMD1.

680X0: SIZ1=0, SIZ0=1, A1=0, A0=0

MS byte to DAL <31:24>

80X86 : #BE3=0, #BE2=1, #BE1=1, #BE0=1

MS byte to DAL <31:24>

Transmit/Receive Buffers :

LONG-WORD TRANSFER TO/FROM EVEN-WORD ADDRESS

Example: First, last or only 4 bytes in buffer on even-word address.

680X0: SIZ1=0, SIZ0=0, A1=0, A0=0

FIFO	byte n	to/from	DAL <31:24>
FIFO	byte n + 1	to/from	DAL <23:16>
FIFO	byte n + 2	to/from	DAL <15:08>
FIFO	byte n + 3	to/from	DAL <07:00>

80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0

FIFO	byte n	to/from	DAL <07:00>
FIFO	byte n + 1	to/from	DAL <15:08>
FIFO	byte n + 2	to/from	DAL <23:16>
FIFO	byte n + 3	to/from	DAL <31:24>

3-BYTE TRANSFER FROM EVEN-WORD ADDRESS

Example: Last or only 3 bytes in transmit buffer.

680X0: SIZ1=0, SIZ0=0, A1=0, A0=0

FIFO	byte n	from	DAL <31:24>
FIFO	byte n + 1	from	DAL <23:16>
FIFO	byte n + 2	from	DAL <15:08>

80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0

FIFO	byte n	from	DAL <07:00>
FIFO	byte n + 1	from	DAL <15:08>
FIFO	byte n + 2	from	DAL <23:16>

Note: Although all bytes are active, only required bytes are used internally.

3-BYTE TRANSFER TO EVEN-WORD ADDRESS

Example: Last or only 3 bytes in receive buffer.

680X0: SIZ1=1, SIZ0=1, A1=0, A0=0

FIFO	byte n	to	DAL <31:24>
FIFO	byte n + 1	to	DAL <23:16>
FIFO	byte n + 2	to	DAL <15:08>

80X86: #BE3=1, #BE2=0, #BE1=0, #BE0=0

FIFO	byte n	to	DAL <07:00>
FIFO	byte n + 1	to	DAL <15:08>
FIFO	byte n + 2	to	DAL <23:16>

WORD TRANSFER FROM EVEN-WORD ADDRESS
Example: Last or only 2 bytes in transmit buffer on even-word address.
680X0: SIZ1=0, SIZ0=0, A1=0, A0=0
FIFO byte n from DAL <31:24>
FIFO byte n + 1 from DAL <23:16>
80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0
FIFO byte n from DAL <07:00>
FIFO byte n + 1 from DAL <15:08>
Note: Although all bytes are active, only required bytes are used internally.

WORD TRANSFER TO EVEN-WORD ADDRESS
Example: Last or only 2 bytes in receive buffer on even-word address.
680X0: SIZ1=1, SIZ0=0, A1=0, A0=0
FIFO byte n to DAL <31:24>
FIFO byte n + 1 to DAL <23:16>
80X86: #BE3=1, #BE2=1, #BE1=0, #BE0=0
FIFO byte n to DAL <07:00>
FIFO byte n + 1 to DAL <15:08>

WORD TRANSFER FROM ODD-WORD ADDRESS
Example: First or only 2 bytes in transmit buffer on odd-word address.
680X0: SIZ1=0, SIZ0=0, A1=0, A0=0
FIFO byte n from DAL <15:08>
FIFO byte n + 1 from DAL <07:00>
80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0
FIFO byte n from DAL <23:16>
FIFO byte n + 1 from DAL <31:24>
Note: Although all bytes are active, only required bytes are used internally.

WORD TRANSFER TO ODD-WORD ADDRESS
Example: First or only 2 bytes in receive buffer on odd-word address.
680X0: SIZ1=1, SIZ0=0, A1=1, A0=0
FIFO byte n to DAL <15:08>
FIFO byte n + 1 to DAL <07:00>
80X86 : #BE3=0, #BE2=0, #BE1=1, #BE0=1
FIFO byte n to DAL <23:16>
FIFO byte n + 1 to DAL <31:24>

BYTE TRANSFER FROM EVEN-WORD ADDRESS
Example: Last or only byte in transmit buffer on even-word address.
680X0: SIZ1=0, SIZ0=0, A1=0, A0=0
FIFO byte n from DAL <31:24>
80X86: #BE3=0, #BE2=0, #BE1=0, #BE0=0
FIFO byte n from DAL <07:00>
Note: Although all bytes are active, only required bytes are used internally.

BYTE TRANSFER TO EVEN-WORD ADDRESS
Example: Lastor only byte in receive buffer on even-word address.
680X0: SIZ1=0, SIZ0=1, A1=0, A0=0
FIFO byte n to DAL <31:24>
80X86: #BE3=1, #BE2=1, #BE1=1, #BE0=0
FIFO byte n to DAL <07:00>

BYTE TRANSFER FROM ODD-WORD ADDRESS
Example: Last or only byte in transmit buffer on odd-word address.
680X0: SIZ1=0, SIZ0=0, A1=0, A0=0
FIFO byte n from DAL <15:08>
80X86 : #BE3=0, #BE2=0, #BE1=0, #BE0=0
FIFO byte n from DAL <23:16>
Note: Although all bytes are active, only required bytes are used internally.

BYTE TRANSFER TO ODD-WORD ADDRESS
Example : Last or only byte in receive buffer on odd-word address.
680X0: SIZ1=0, SIZ0=1, A1=1, A0=0
FIFO byte n to DAL <15:08>
80X86: #BE3=1, #BE2=0, #BE1=1, #BE0=1
FIFO byte n to DAL <23:16>

FIFO Operations

The FIFO provides temporary buffer storage for data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the FIFO is 48 bytes.

Transmit

Data is loaded into the FIFO under internal micro-program control.

The FIFO must be more than 16 bytes empty before the ILACC requests the bus ($\overline{\text{HOLD}}$/$\overline{\text{BUSREQ}}$ is asserted). The ILACC will start sending the preamble (if the line is idle) as soon as there is one byte loaded into the FIFO. Should the transmitter be required to back off, there will be up to 32 bytes of data in the FIFO ready for transmission. Reception has priority over transmission during the time that the transmitter is backing off.

Receive

Data is loaded into the FIFO from the serial input shift register during reception and leaves the FIFO under microprogram control. The ILACC microcode will wait until there are at least 16 bytes of data in the FIFO before initiating a DMA burst transfer. Preamble (including the synchronization bits) is not loaded into the FIFO.

Serial Interface

The ILACC has two serial interfaces:

- General Purpose Serial Interface
- IEEE 802.3 Attachment Unit Interface (AUI)

GENERAL PURPOSE SERIAL INTERFACE

This is provided to allow alternate clock/data encoder transceivers. When the GPSI port is not in use (PORTSEL = 0, CSR15 bit 8), all inputs should be tied low and when all outputs are not in use, it should be left floating.

SERIAL INTERFACE ADAPTER

This is a Manchester Encoder/line driver in the transmit path, a Manchester Decoder with noise filtering and quick lock-on characteristics in the receive path, and a signal detect/converter in the collision path. In addition, the integral SIA provides the interface between the CMOS logic environment of the controller and the differential signaling environment of the transceiver.

SIA-Controller Interface

Since the ILACC incorporates the facilities of both the LANCE (Am7990) and SIA (Am7992A), the interface signals which previously appeared as hardwired pins are now internal.

To more easily understand the operation of the ILACC, this internal interface is described as a set of signals, defined as follows:

Internal Receive Enable (IRENA) – Analogous to the externally available Carrier Sense (CRS) signal. An output from the SIA to the controller to indicate carrier presence. IRENA goes active when there is a negative transition on RCV+/RCV- that is more negative than the amplitude "Squelch Limit" and meets the pulse width requirements of the input filtering. IRENA goes inactive within 2 bit times of the last positive transition at RCV+/RCV-.

Internal Receive Clock (IRCLK) – The recovered clock from the differential input at RCV+/RCV-. An output from the SIA block to the controller, to clock in the serial bit stream. IRCLK is activated 1/4 bit time after the second negative Manchester preamble clock transition at RCV+/RCV-, and remains active until the end of message.

Internal Receive Data (IRXD) – The recovered serial data stream from the SIA block to the controller section of the ILACC. When IRENA is active, signals at RCV+/RCV- meeting threshold and pulse width requirements will be clocked in by IRCLK and passed to the controller portion of the ILACC.

Internal Transmit Enable (ITENA) – Identical in function to the RTS output. It is asserted (high) by the controller portion to indicate that serial data is available for encoding and driving XMIT+/XMIT-.

Internal Transmit Clock (ITCLK) – An output from the SIA block to the controller, to clock out the serial bit stream and permit output data to be encoded.

Internal Transmit Data (ITXD) – The serial bit stream output from the controller section. When ITENA is active, signals at ITXD will be clocked out by ITCLK and appear as Manchester encoded data at the XMIT+/XMIT- outputs.

Internal Collision Detect (ICLSN) – Identical in function to the externally available CDT input to the ILACC. ICLSN is an output from the SIA block to the controller. When signals at the COLL+/COLL- differential inputs are driven by an external transceiver to indicate a collision, ICLSN will go high.

Transmit Path

The transmit section encodes separate clock and NRZ data input signals into a standard Manchester serial bit stream. The transmit outputs (XMIT+/XMIT-) are designed to operate into terminated transmission lines. When operating into a 78-ohm terminated transmission line, signaling meets the required output levels and skew for Cheapernet, Ethernet and IEEE-802.3.

Transmitter Timing and Operation

A 20-MHz fundamental mode crystal oscillator provides the basic timing reference (XCLK) for the SIA portion of the ILACC. It is divided by two, to create the internal transmit clock reference (ITCLK). Both XCLK and ITCLK are fed into the SIA's Manchester Encoder to generate the transitions in the encoded data stream. ITCLK is used by the SIA to internally synchronize the Internal Transmit Data (ITXD) from the controller and Internal Transmit Enable (ITENA). ITCLK is also used as a stable bit rate clock by the receive section of the SIA and controller.

The oscillator requires an external 0.005% crystal, or an external TTL-level input as a reference. Transmit accuracy of 0.01% is achieved (no external adjustments are required).

Transmission is enabled by the controller. As long as the ITENA request remains active, the serial output of the controller will be Manchester-encoded and appear at XMIT+ and XMIT-. When the internal request is dropped by the controller, the differential transmit outputs go to one of two idle states, dependent on TSEL in the Mode Register (CSR15, bit 9):

1. TSEL LOW: The idle state of XMIT+/XMIT- yields "zero" differential to operate transformer-coupled loads.
2. TSEL HIGH: In this idle state, XMIT+ is positive with respect to XMIT- (logical HIGH).

SIA Oscillator

External Crystal Characteristics

When using a crystal to drive the oscillator, the following crystal specification should be used to ensure a transmit accuracy of 0.01%:

	Min	Nom	Max	Units
1. Parallel Resonant Frequency	2		20	MHz
2. Resonant Frequency Error (CL = 50 pF)	−50	0	+50	PPM
3. Change in Resonant Frequency With Respect To Temperature (CL = 50 pF)	-40		+40	PPM
4. Motional Crystal Capacitance (C1)		0.022		pF
5. Series Resistance			35	Ω
6. Shunt Capacitance			7	pF
7. Drive Level			5	mW

External Clock Drive Characteristics

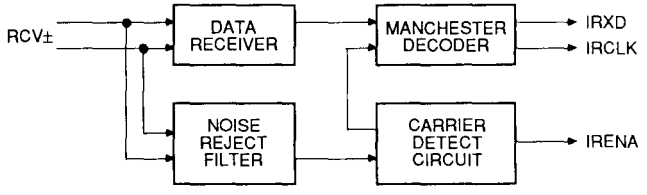
When driving the oscillator from an external clock source, XTAL2 must be left floating (unconnected). An external clock having the following characteristics must be used to ensure less than ±0.5 ns jitter at XMIT+/ XMIT-.

Clock Frequency:	2-20 MHz +0.01%
Rise/Fall Time (tR/tF):	< 2 ns from 0.8 V to 2.0 V
XTAL1 HIGH/LOW Time (tHIGH/tLOW):	40 - 60% duty cycle
XTAL1 Falling Edge to Falling Edge Jitter:	< +0.2 ns at 1.5 V input

Receiver Path

The principle functions of the Receiver are to signal the ILACC that there is information on the receive pair, and separate the incoming Manchester encoded data stream into clock and NRZ data.

The Receiver section (see Receiver Block Diagram) consists of two parallel paths. The receive data path is a zero threshold, wide bandwidth line receiver. The carrier path is an offset threshold bandpass detecting line receiver. Both receivers share common bias networks to allow operation over a wide input common mode range.



Receiver Block Diagram 10594-006A

Input Signal Conditioning

Transient noise pulses at the input data stream are rejected by the Noise Rejection Filter. Pulse width rejection is proportional to transmit data rate. DC inputs more positive than minus 100 mV are also suppressed.

The Carrier Detection circuitry controls the stop and start of the phase-locked loop during clock acquisition. Clock acquisition requires a valid Manchester bit pattern of 1010 to lock onto the incoming message (see Receive Timing – Start of Reception Clock Acquisition waveform diagram).

When input amplitude and pulse width conditions are met at RCV+/RCV–, the internal enable signal from the SIA to controller (IRENA) is asserted and a clock acquisition cycle is initiated.

Clock Acquisition

When there is no activity at RCV+/RCV- (receiver is idle), the receive oscillator is phase locked to ITCLK. The first negative clock transition after IRENA is asserted interrupts the receive oscillator. The oscillator is then restarted at the second Manchester "0" (bit time 4) and is phase locked to it. As a result, the SIA acquires the clock from the incoming Manchester bit pattern in 4 bit times with a "1010" Manchester bit pattern.

IRCLK and IRXD are enabled 1/4 bit time after clock acquisition in bit cell 5. IRXD, is at a HIGH state when the receiver is idle (no IRCLK). IRXD, however, is undefined when clock is acquired and may remain HIGH or change to LOW state whenever IRCLK is enabled. At 1/4 bit time through bit cell 5, the controller portion of the ILACC sees the first IRCLK transition. This also strobes in the incoming fifth bit to the SIA as Manchester "1". IRXD may make a transition after the IRCLK rising edge in bit cell 5, but its state is still undefined. The Manchester "1" at bit 5 is clocked to IRXD output at 1/4 bit time in bit cell 6.

PLL Tracking

After clock acquisition, the phase-locked clock is compared to the incoming transition at BCC and the resulting phase error is applied to a correction circuit. This circuit ensures that phase-locked clock remains locked on the received signal. Individual bit cell phase corrections of the V_{CO} are limited to 100% of the phase difference between BCC and phase-locked clock. Hence, input data jitter is reduced in RCLK by 10 to 1.

Carrier Tracking and End of Message

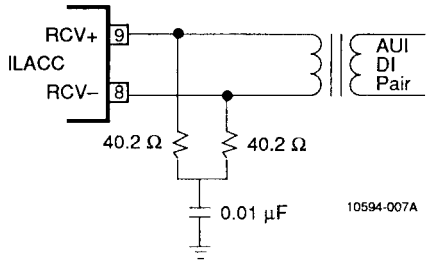
The carrier detection circuit monitors the RCV+/RCV- inputs after IRENA is asserted for an end of message. IRENA deasserts 1 to 2 bit times after the last positive transition on the incoming message. This initiates the end of reception cycle. The time delay from the last rising edge of the message to IRENA deassert allows the last bit to be strobed by IRCLK and transferred to the controller section, but prevents any extra bit(s) at the end of message. When IRENA deasserts (see Receive Timing-End of Reception (Last Bit = 0) and Receive Timing-End of Reception (Last Bit = 1) waveform diagrams) an IRENA hold off timer inhibits IRENA assertion for 1 to 2 bit times.

Data Decoding

The data receiver is a comparator with clocked output to minimize noise sensitivity to the RCV+/RCV- inputs. Input error is less than +/- 35 mV to minimize sensitivity to input rise and fall time. IRCLK strobes the data receiver output at 1/4 bit time to determine the value of the Manchester bit, and clocks the data out on IRXD on the following IRCLK. The data receiver also generates the signal used for phase detector comparison to the internal SIA voltage controlled oscillator (VCO).

Differential Input Termination

The differential input for the Manchester data (RCV+/RCV-) is externally terminated by two 40.2 ohm +1% resistors and one optional common-mode bypass capacitor, if direct coupling is used (as shown in the Differential Input Termination diagram below). The differential input impedance, Z_{IDF}, and the common-mode input impendance, Z_{ICM}, are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The COLL+/COLL- differential inputs are terminated in exactly the same way for the AUI DI pair.



Differential Input Termination

Collision Detection

A transceiver detects the collision condition on the network and generates a differential signal at the COLL+/COLL- inputs. This collision signal passes through an input stage which detects signal levels and pulse duration. When the signal is detected by the SIA it sets the ICLSN line HIGH. The condition continues for approximately 1.5 bit times after the last LOW-to-HIGH transition on COLL+/COLL-.

Jitter Tolerance Definition

The Receive Timing-Start of Reception Clock Acquisition waveform diagram shows the internal timing relationships implemented for decoding Manchester data in the SIA module. The SIA utilizes a clock capture circuit to align its internal data strobe with an incoming bit stream. The clock acquisition circuitry requires four valid bits with the values 1010. Clock is phase locked to the negative transition at the bit cell center of the second "0" in the pattern.

Since data is strobed at 1/4 bit time, Manchester transitions which shift from their nominal placement through 1/4 bit time will result in improperly decoded data. With this as the criteria for an error, a definition of "Jitter Handling" is:

The peak deviation approaching or crossing 1/4 bit cell position from nominal input transition, for which the SIA will properly decode data.

Data Flow Overview

DESCRIPTOR RING ACCESS MECHANISM – DETAILED DESCRIPTION

At initialization, the ILACC will have read the base address of both the transmit and receive descriptor rings. These will be stored in CSRs for use by the ILACC during subsequent operation (CSR24 = Base Address of Rx Ring, CSR30 = Base Address of Tx Ring).

With the ILACC started, and the transmit and receive functions enabled, the base address of each ring will be loaded into the current descriptor address registers (CSR28 = Current Address of Rx Ring, CSR34 = Current Address of Tx Ring).

The address of the next descriptor in the transmit and receive rings will be computed (current ring address + descriptor table entry length) and loaded into CSR26 (Next Address of Rx Ring) and CSR32 (Next Address of Tx Ring).

TRANSMIT DESCRIPTOR TABLE ENTRY (TDTE)

When there is no channel activity, the ILACC will use the current descriptor address stored internally, to vector to the appropriate TDTE. It will subsequently poll the entry, awaiting the host to set the OWN bit (in TMD1). This will be set by the host to signal that a buffer has been queued for transmission. The poll time is a function of BCLK. The descriptor will be polled at intervals of 32 768x T_{BCLK} (BCLK period).

If the OWN and start of packet (STP) bits are set, the ILACC will save the status bits, and any address information within TMD1, and subsequently read TMD0 to obtain the full address of the data buffer. This will be saved in the Current Tx Buffer Address (CSR20) location. The length field will be read from TMD1 and saved in the Current Tx Byte Count (CSR42) location. Each of these memory reads is performed separately with a new arbitration cycle for each transfer.

If the OWN bit was set, but STP = 0, the ILACC will reset the OWN bit and move to the next transmit descriptor in the ring.

If the transmit buffers are data chained (ENP = 0), the ILACC will look ahead to the next transmit descriptor in the ring, before transferring the first data burst for the current data buffer to the FIFO. This lookahead operation is performed only once.

If the ILACC does not own the next TDTE (i.e., the second TDTE for this packet), it will complete transmission of the current buffer, and update the status of the current (first) TDTE by setting the BUFF bit. This will cause the transmitter to be disabled (CSR0, TXON = 0). The ILACC will have to be re-initialized to restore the transmit function.

If the ILACC owns the second TDTE, it will also read the buffer address and byte count entries. The information read from the next buffer in the chain is saved by the ILACC in the Next Rx/Tx Buffer Address (CSR22), the Next Rx/Tx Byte Count (CSR44), and the Next Rx/Tx Status (CSR54) locations. Once the ILACC has completed emptying the current buffer, it will clear the OWN bit, overwrite all "current" descriptor and buffer entries with "next" entries in the appropriate CSR locations, and immediately start loading data from the second buffer.

Between DMA bursts, starting from the second buffer, the ILACC again performs the lookahead operation, to check for ownership of the next (third) buffer. This sequence will continue, until a TDTE indicates the end of the packet (ENP =1). When all data from the packet has been transmitted from the FIFO to the channel, the ILACC will update the status bits in TMD1 and write the Transmit Collision Count (TMD2). If there were errors, TMD2 will be updated, prior to the ILACC relinquishing ownership of the last buffer. The ILACC will subsequently inspect the next buffer for ownership (first buffer in next packet), to guarantee back-to-back packet transmission.

If the next buffer is not owned by the ILACC, then it will continue to poll the TDTE every 1.6ms (BCLK = 20 MHz), until the host toggles the state of the OWN bit.

If an error occurs before all buffers are transmitted (i.e., RTRY or LCOL), the ILACC will stop the current packet transmission, reset the OWN bit in TMD1, and set the TINT bit in CSR0, causing an interrupt if IENA = 1. The ILACC will not transmit the remaining buffer(s) in the packet. Instead, it will reset the OWN bit and update the error flags (TMD2) in the current TDTE. The ILACC will subsequently reset the OWN bit in each TDTE it polls, until it locates a TDTE with both OWN and STP set, indicating the first buffer of a new packet.

When the transmit buffers are not chained (ENP = 1), indicating a single buffer packet or the last buffer in a multi-buffer packet, the ILACC does not perform the lookahead operation. It will transmit the current buffer, update TMD2 if an error occurred, update the status and reset the OWN bit in TMD1, and overwrite CSR34 (Current Address of Tx Ring) with the contents of CSR32 (Next Address of Tx Ring). The ILACC will then immediately check the current TDTE for ownership. If the ILACC owns the descriptor, it will read the other entries in the descriptor table, and save them in the "current" data buffer locations. Transfer of the data to

the FIFO for transmission, lookahead operation and update of the CSR locations will then follow the sequence as described. If the ILACC does not own the descriptor, it will poll the descriptor entry every 1.6ms (BCLK = 20MHz) until the host toggles the state of the OWN bit. The host may set the TDMD bit in CSR0 once it has passed ownership of the buffer to the ILACC. This will force the ILACC to check the OWN bit of the "current" TDTE, without waiting for the poll time to elapse.

RECEIVE DESCRIPTOR TABLE ENTRY (RDTE)

Receive ring access is similar to that of the transmit ring. Once the receiver is enabled, the ILACC will check for ownership of the receive descriptor designated as "current" (as defined in the Current Rx Buffer Address in CSR18). With no incoming messages, and the OWN bit clear, the ILACC will poll RMD1 every 1.6ms (BCLK = 20MHz) until the host relinquishes ownership. Once the ILACC owns the buffer, it will read the buffer address and length, updating the "current" CSR entries.

When a packet is received from the channel, the ILACC will first check that it owns a receive buffer. If it does not, it will poll the receive descriptor once more to determine if the host has relinquished ownership. If ownership remains with the host, the ILACC has no receive buffer in which to dump the incoming packet data. It will set the MISS error in CSR0 (generating an interrupt if INEA is set), and will not poll the RDTE until the packet has completed.

If the ILACC owns a receive buffer when a packet is received, it will interleave a lookahead operation while dumping the receive data into the buffer. This lookahead operation will consist of a single DMA read of the next RDTE status (RMD1), if ownership of the buffer remains with the host. If the OWN bit is set, the lookahead will consist of two separate DMA read operations, as the address and length fields of the buffer are also read from the DTE. The "next" fields in the CSR locations will be updated with the information from the lookahead. Either lookahead operation is performed only once.

Regardless of ownership of the second receive buffer, the ILACC will complete the received data transfer from the FIFO to the first receive buffer, under burst-mode DMA.

If the packet length exceeds the length of the first buffer and requires buffer chaining, and the ILACC does not own the second buffer, it will update the current descriptor status in RMD1 with the BUFF and possibly OFLO bits set, toggle the OWN bit, and overwrite the Current Address of Rx Ring (CSR28) with the Next Address of Receive Ring (CSR26). If the ILACC does own the second buffer, it will relinquish the current buffer, overwrite all "current" descriptor and buffer entries in CSRs with "next" entries (as read in the previous lookahead), and commence unloading the FIFO to the second buffer in the chain. Between DMA bursts to unload the FIFO, the ILACC will perform the next lookahead operation to check for ownership of the next (third) RDTE. If it does own the descriptor, it will again read the address and length fields and update the "next" buffer locations in the appropriate CSRs.

This activity continues until the ILACC recognizes the completion of the packet (channel becomes idle). The ILACC will subsequently update the current RDTE status with the end of packet (ENP) indication set, write the message byte count (MCNT) for the complete packet into RMD2, and overwrite the "current" entries in the CSRs with the "next" entries.

If after receive completion, the packet is detected as a runt, the "current" buffer address and status in the RDTE are not updated, and the internal CSRs are also not updated. The runt packet data buffer will be overwritten by the next received message data.

At this stage, dependent on ownership during the previous lookahead operation, the "next" CSR locations associated with the data buffer status, address and length, may or may not contain the next data buffer to be used. The "current" CSR locations associated with the RDTE will contain the information necessary to poll the next descriptor in the ring if necessary.

SERIAL TRANSMISSION

Serial transmission consists of sending an unbroken bit stream from either the TxD output or XMIT+/XMIT- pair consisting of:

1. Preamble/Start Frame Delimeter (SFD): 56 bits (7 bytes) of alternating ONES and ZEROES terminating with the 8-bit (1-byte) SFD sequence of 10101011.
2. Data: The serialized byte stream from the FIFO shifted out with the LSB first.
3. CRC: The inverted 32-bit polynomial calculated from the data, address, and type fields, shifted out with the MSB first. The CRC is not transmitted if:
   a. Transmission of the data field is truncated for any reason.
   b. CDT or COLL+/- becomes active at any time during transmission.
   c. DTCR = 1 (CSR15, bit 03) in a normal or loopback transmission mode.

The transmission is indicated at the general purpose serial interface by the assertion of RTS with the first bit of the preamble and the negation of RTS after the last transmitted bit.

The ILACC starts transmitting the preamble when the following are satisfied:

1. There is at least 1 byte of data to be transmitted in the FIFO.
2. The interpacket gap time (IPG) has elapsed.
3. The backoff interval has elapsed, if a retransmission is required.

SERIAL RECEPTION

Serial reception consists of receiving an unbroken bit stream on the RxD input or RCV+/RCV- pair consisting of:

1. Preamble/SFD: The two consecutive ONES of the SFD, occurring a minimum of 8 bit times after the carrier is detected (assertion of internal or external Carrier Sense), commence the serial to parallel conversion process, and movement of the receive bit stream into the FIFO.
2. Data: The serialized byte stream following the Destination Address. The last four complete bytes of data are the CRC. The Destination Address and the Data are framed into bytes and enter the FIFO. Source Address and Length/Type field are part of the data which are transparent to the ILACC.

Reception is indicated at the general purpose serial interface by the assertion of CRS and the presence of clock on RxC while RTS is inactive. The ILACC does not sample the received data until about 8 bit times (800 ns for 10-MHz operation) after CRS goes high. Note that the receive process will be aborted if two consecutive ZEROES occur during the preamble/SFD sequence, prior to the two ONES pattern within the SFD.

FRAME FORMATTING

The ILACC performs the encapsulation/decapsulation function of the data link layer (2nd layer of ISO model) as follows:

Transmit

In transmit mode, the user must supply the Destination Address, Source Address, and Length/Type fields, as part of the data field in the transmit buffer memory. The ILACC will append the preamble, SFD (or synchronization bits), and CRC (Frame Check Sequence) to the frame as is shown in the figures below.

Receive

In receive mode, the ILACC strips off the preamble and SFD (or synch bits) and transfers the rest of the frame, including the four CRC bytes, to the memory. The ILACC will discard packets with less than 64 bytes (runt packet) and will reuse the receive buffer for the next packet. This is the only case where the packet data is discarded. A runt packet is normally the result of a collision.

Error Reporting and Diagnostics

Extensive status reporting and diagnostics are provided by the ILACC.

Error Reporting

Error conditions reported relate either to the network as a whole or to the individual node. Network error and status information is reported in the ILACC internal CSRs, and also within the message buffer descriptors passed between the ILACC and the host or user.

Node Errors Include:

Babbling Transmitter – Transmitter attempting to transmit more than 1518 data bytes.

Collision – Collision detection circuitry nonfunctional.

Missed packet – Insufficient buffer space.

Memory time-out – Memory response failure.

Overflow – The receiver has lost all or part of the incoming packet due to overflow of internal FIFO.

Buffer error – The receiver does not own the next buffer when data chaining.

Underflow – When transmitting, the FIFO has emptied before the end of the packet was loaded into the ILACC.

Network Related Errors:

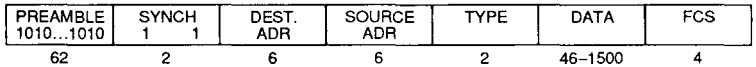
Framing – Packet did not end on a byte boundary.

CRC – A CRC error was detected on the incoming packet.

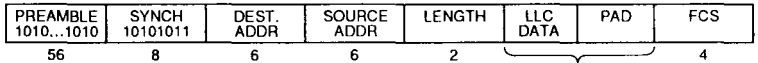
Receive Collision Count – Counts collisions on the network between any two receive packets.

Runt Packet Count – Counts undersize packets on the network between any two received packets.

Transmit Collision Count – Counts the number of retrys to send an individual packet.



Ethernet Frame Format



IEEE 802.3 MAC Frame Format

10594-009A

The ILACC performs several diagnostic routines which enhance the reliability and integrity of the system. These include a CRC logic check and two loopback modes (internal/external). Errors may be introduced into the system to check error detection logic. A Time Domain Reflectometer is incorporated into the ILACC to aid the location of cable faults. Short or open circuit conditions manifest themselves in reflections which are sensed by the TDR.

FRAMING ERROR (DRIBBLING BITS)

The ILACC can handle up to 7 dribbling bits when a received packet terminates. During the reception, the CRC is generated on every serial bit (including the dribbling bits) coming from the cable, although the internally saved CRC value is only updated on the eighth bit (on each byte boundary). The framing error is reported to the user as follows:

1. If the number of the dribbling bits are 1 to 7 and there is no CRC error, then there is no Framing error (FRAM = 0).
2. If the number of the dribbling bits are less than 8 and there is a CRC error, then there is also a Framing error (FRAM = 1).
3. If the number of the dribbling bits = 0, then there is no Framing error. There may or may not be a CRC error.

LOSS OF CARRIER

After the ILACC initiates a request for transmission (either internally to the embedded SIA, or externally via the RTS output), it will expect to see a "carrier sense" returned from the internal SIA or the external transceiver (CRS should become active when the general purpose serial interface is used). The "carrier sense" signal must be asserted during the time that the request to send is active. If "carrier sense" does not become active in response to the request or becomes inactive before the end of transmission, the LCAR (loss of carrier) error bit will be set in TMD2 after the packet has been transmitted.

DIAGNOSTICS

Loopback

The normal operation of the ILACC functions as a half-duplex device. However, a pseudo-full duplex mode is provided for on-line operational test of the ILACC. In this configuration, simultaneous transmission and reception of a loopback packet is enabled with the following constraints:

1. The packet length must be no longer than 42 bytes with DTCR=0 and 46 bytes with DTRC=1. If the transmit packet size exceeds the recommended length, LBE is set to indicate an overflow in the FIFO.
2. Serial transmission does not begin until the FIFO contains the entire output packet.
3. Moving the input packet from the FIFO to the memory does not begin until the serial input bit stream terminates.
4. The CRC may be generated and appended to the output serial bit stream or may be checked on the input serial bit steam, but not both in the same transaction.
5. The packets should be addressed to the node itself.
6. During normal loopback, all address schemes remain valid.
7. Multicast addressing can be used only when DTCR = 1 (CSR15 bit 3). In this case, the user needs to append the CRC bytes.
8. Ordinary receive activity will be ignored.

Loopback is controlled by INTL, DTCR, and LOOP (CSR15 bits 6, 3, 2).

Loop	INTL	Function
0	X	No loopback, normal operation
1	0	External loopback
1	1	Internal

Interpacket Gap Time (IPG)

General Purpose Serial Interface

The IPG time is 96 network data bit times. The interpacket gap time for back-to-back transmission is 9.6 to 10.6 microseconds (for a 10-MHz network data rate), including synchronization. The interpacket delay interval begins immediately after the negation of the CRS signal. During the first 64 clock cycles of the IPG, CRS activity is internally masked in the ILACC.

Following a receive packet, if CRS is asserted and remains asserted during the first 64 clock cycles of IPG, the ILACC will ignore the packet, and the IPG timer will not recommence until CRS goes inactive.

Following a transmit packet, if CRS is asserted during, and remains asserted after, the 64 clock-period window, the ILACC will start to look for the synch bits (011) about 8 bit times (800 ns for 10-MHz data rates) after the 64 clock-period window has elapsed. Therefore, the packet may be received correctly if at least 8 bits of the alternating ONES and ZEROES sequence are left following the 64 clock-period window. The received packet may contain a CRC error, if insufficient preamble bits remain, and the ILACC looks for and detects the SFD within the data field. Alternatively, the receive process may be terminated, due to the detection of two consecutive ZEROES while awaiting the SFD. In this case, the full interpacket delay will not recommence until the receive bit stream completes (CRS goes inactive). Finally, the received packet may be discarded due to runt packet detection, indicating excessive data loss during the 64 clock-period window.

If CRS is asserted after the 64 clock-period window, the ILACC will treat this as the start of a new packet. It will start to look for the synch bits (011) 8 bit times after CRS becomes active.

Whenever the ILACC is ready to transmit (i.e., the FIFO has been loaded with at least one byte of transmit data), and is waiting for the interpacket delay to elapse, it will begin transmission immediately after the interpacket delay interval. If the ILACC has previously deferred a transmission, due to a receive message being detected during the 64 clock-period window, the ILACC will attempt to transmit the packet after the next IPG time elapses, regardless of CRS activity.

Internal SIA Interface

The timing of the integrated SIA is identical to that described above. However, no external signals are available to indicate the start of the IPG time out.

COLLISION DETECTION AND COLLISION JAM

General Purpose Serial Interface

Collisions are detected by monitoring the CDT pin. If CDT becomes asserted during a frame transmission, RTS will remain asserted for at least 32 (but not more than 40) additional bit times (including CDT synchronization). This additional transmission after collision detection is referred to as COLLISION JAM. If collision occurs during the transmission of the preamble, the ILACC continues to send the preamble, and sends the 32-bit JAM pattern following the preamble. If collision occurs after the preamble, the ILACC will send the JAM pattern following the transmission of the current byte. The JAM pattern is any pattern except the CRC bytes.

Internal SIA Interface

When using the SIA interface, collisions are detected by monitoring the differential COLL+/COLL- signals returned from the bus transceiver. JAM is issued the same way as General Purpose Serial Interface.

Receive-Based Collision

If CDT or COLL+/COLL- (serial interface dependent) is asserted during the reception of a packet, the reception is immediately terminated. If a collision occurs within 6 byte times (4.8 ms at 10M bit/s network data rate), the packet will be rejected because of an address mismatch, and the FIFO write pointer will be reset. If a collision occurs within 64 byte times (51.2 ms at 10M bit/s), the packet will be rejected since it is a runt packet. If a collision occurs after 64 byte times (late collision), this will result in a truncated packet being written to the memory buffer, the LCOL bit in the RDTE will be set in RMD1 and the CRC error bit may also be set.

Transmit-Based Collision

When a transmission attempt has been terminated due to the assertion of CDT or COLL+/COLL- (a collision that occurs within 64 byte times), the ILACC will retry the transmission up to a maximum of 15 times. The ILACC does not try to reread the descriptor entries from the transmit TDTE upon each collision. The descriptor entries for the current buffer are internally saved in the CSRs. The scheduling of each re-transmission is determined by a controlled randomized process called the "truncated binary exponential backoff". Upon completion of the COLLISION JAM interval, the ILACC calculates a delay before re-transmitting. The delay is an integral multiple of the SLOT TIME. The SLOT TIME is defined as 512 bit times (64 bytes). If a collision is detected during transmission, the SLOT TIME counter is started at the end of the COLLISION JAM sequence.

The number of SLOT TIMES to delay before the nth re-transmission attempt is chosen as a uniformly distributed random integer "r" in the range of :

$0 < r < 2^k$, where $k = \min(n, 10)$

For example, if this is the third retry :

$n = 3$

$k = \min(3,10) = 3$

$2^3 = 8$

If the number selected is zero ($r = 0$), the ILACC will begin re-transmission at the end of the 96 clock IPG time.

If all 15 retry attempts fail, the ILACC sets the RTRY bit in the current transmit TDTE in host memory (TMD2), gives up ownership (sets the OWN bit to zero) for this packet, and processes the next packet in the transmit ring for transmission.

When there are excessive collisions of any buffer in a multi-buffer packet, the status will be written in the current descriptor. The OWN bit in the subsequent descriptor will be reset until the STP is found.

If there is a late collision (collision occurring after 64 byte times), the ILACC will not retransmit. It will terminate the transmission, note the LCOL error (TMD2), and transmit the next packet in the ring.

Collision-Microcode Interaction

The microprogram uses the time provided by COLLISION JAM, INTERPACKET DELAY, and the backoff interval to restore the address and byte counts internally and starts loading the FIFO in anticipation of retransmission. It is important that the ILACC be ready to transmit when the backoff interval elapses to utilize the channel properly.

Time Domain Reflectometry

The ILACC contains a time domain reflectometry counter. The TDR counter is ten bits wide. It counts at the internal ILACC network crystal frequency (XCLK). It is cleared by the microprogram, and commences counting once the carrier is detected during transmission.

Counting ceases if a collision is detected (CDT or COLL+/COLL-), or the request for transmission (RTS for general interface, internal request for integrated SIA) is dropped. The counter does not wrap around, but will freeze at the maximum count (all ones), until cleared. The value in the TDR is written to the TDTE TMD2 following the transmission of the packet. The TDR is used to determine the location of suspected cable faults.

Heartbeat

General Purpose Serial Interface

During the INTERPACKET DELAY following the negation of RTS, the CDT input is asserted by some transceivers as a self-test. If the CDT input is not asserted within a 20 network bit (2 μs) time period following the completion of transmission (after CRS goes inactive), then the ILACC will set the CERR bit in CSR0. CERR error will not cause an interrupt to occur ($\overline{INTR}$ = 0).

Internal SIA

The integrated SIA within the ILACC performs the self test feature described above invisibly to the user. The SIA will expect the SQE TEST waveform (nominal 10-MHz sequence) to be returned via the COLL+/COLL- pair, by the external transceiver within 20 network bit periods after RCV+/RCV- goes inactive.

Cyclic Redundancy Check (CRC)

The ILACC utilizes the 32-bit CRC function used in the Autodin-II network. Refer to the Ethernet specification (Frame Check Sequence Field and Appendix C: CRC Implementation) or ISO 8802-3 ANSI/IEEE Std. 802-3 can be verified using the LOOP (CSR15 bit 2) and DTCR (CSR15 bit 3) bits. See Frame Check Sequence Field section on page 21 for more detail. The ILACC CRC logic is as follows:

1. **TRANSMISSION – LOOP = 0 (CSR15 bit 2) and DTCR = 0 (CSR15 bit 3).** The ILACC calculates the CRC from the first bit following the Start bit to the last bit of the data field. The CRC value inverted is appended onto the transmission in one unbroken bit stream, with the most significant bit transmitted first.
2. **RECEPTION – LOOP = 0 (CSR15 bit 2).** The ILACC performs a check on the input bit stream from the first bit following the start bit to the last bit in the frame. The ILACC continually samples the state of the CRC checked on framed byte boundaries, and, when the incoming bit stream stops, the last sample determines the state of the CRC error. Framing error (FRAM) is not reported if there is no CRC error.
3. **LOOPBACK – LOOP = 1 (CSR15 bit 2) and DTCR = 0 (CSR15 bit 3).** The ILACC generates and appends the CRC value to the outgoing bit stream as in Transmission, but does not perform the CRC check of the incoming bit stream.
4. **LOOPBACK – LOOP = 1 (CSR15 bit 2) and DTCR = 1 (CSR15 bit 3).** The ILACC performs the CRC check on the incoming bit stream as in Reception, but does not generate or append the CRC value to the outgoing bit steam during transmission.

PROGRAMMABLE RESOURCES

This section defines the control and status registers and the memory data structures required to program the ILACC.

User Programmable Registers

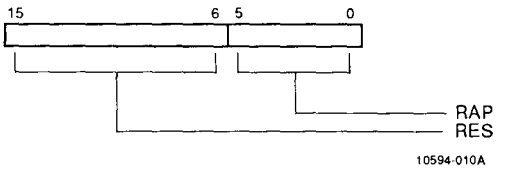
Internal programmable registers are accessed in a two step operation. First, the address of the programmable register is written into the Register Address Port (RAP). Subsequent read or write operations will access the register pointed to by the contents of the RAP. The data will be read from (or written into) the selected Register through the Data Port.

The C/$\overline{D}$ pin permits external selection of either the Data or the Register Address Port as follows:

C/$\overline{D}$	Port
0	Data Port
1	Register Address Port

REGISTER ADDRESS PORT (C/$\overline{D}$ = H)

The high-order 16 bit (i.e., DAL 16-31) are undefined. RAP is defined as follows:



Bit	Name	Description
15-06	RES	Reserved and read as zero.
05-00	RAP	Register Address Port select. Selects the Control and Status Register location to be accessed. RAP is cleared by $\overline{RESET}$.

CONTROL AND STATUS REGISTERS

The Control and Status Registers (CSRs) are internal to the ILACC, and accessed on an individual basis by first writing the appropriate CSR address into the RAP.

Regardless the state of the STOP bit, READ/WRITE access is permitted to CSR0 and CSR3–4. To access CSR1–2, the STOP bit in CSR0 must be set.

All CSR data transfers will take place over the lower 2 bytes (DAL_{15-0}) for all slave operations. DAL_{31-16} are undefined.

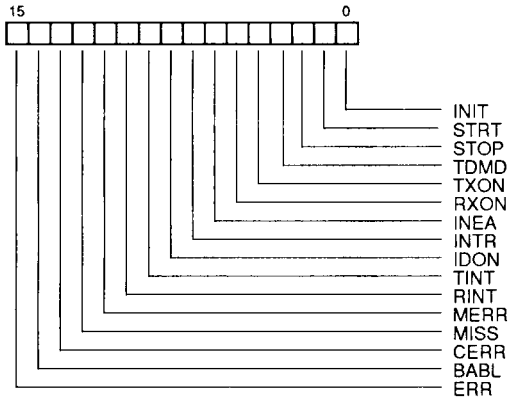
Addresses 5-58 are available as READ ONLY, providing the STOP bit is set. These allow the host to verify data loaded during initialization and/or monitor ILACC functions.

The internal programmable registers are mapped as follows:

RAP	CSR	Contents
00	CSR0	CONTROL AND STATUS REGISTER 0
01	CSR1	CONTROL AND STATUS REGISTER 1
02	CSR2	CONTROL AND STATUS REGISTER 2
03	CSR3	CONTROL AND STATUS REGISTER 3
04	CSR4	CONTROL AND STATUS REGISTER 4
05	CSR5	TRANSMIT COLLISION COUNT
06	CSR6	RX/TX DESCRIPTOR TABLE LENGTH
07	CSR7	RECEIVE COLL./RUNT PACKET CNT.
08	CSR8	LOGICAL ADDRESS FILTER 15-0
09	CSR9	LOGICAL ADDRESS FILTER 31-16
10	CSR10	LOGICAL ADDRESS FILTER 47-32
11	CSR11	LOGICAL ADDRESS FILTER 63-48
12	CSR12	PHYSICAL ADDRESS 15-0
13	CSR13	PHYSICAL ADDRESS 31-16
14	CSR14	PHYSICAL ADDRESS 47-32
15	CSR15	MODE REGISTER
16	CSR16	INITIALIZATION BLOCK ADDRESS 15-0
17	CSR17	INITIALIZATION BLOCK ADDRESS 31-16
18	CSR18	CURRENT RX BUFFER ADDRESS 15-0
19	CSR19	CURRENT RX BUFFER ADDRESS 31-16
20	CSR20	CURRENT TX BUFFER ADDRESS 15-0
21	CSR21	CURRENT TX BUFFER ADDRESS 31-16
22	CSR22	NEXT RX/TX BUFFER ADDRESS 15-0
23	CSR23	NEXT RX/TX BUFFER ADDRESS 31-16
24	CSR24	BASE ADDRESS OF RX RING 15-0
25	CSR25	BASE ADDRESS OF RX RING 31-16
26	CSR26	NEXT ADDRESS OF RX RING 15-0
27	CSR27	NEXT ADDRESS OF RX RING 31-16
28	CSR28	CURRENT ADDRESS OF RX RING 15-0
29	CSR29	CURRENT ADDRESS OF RX RING 31-16
30	CSR30	BASE ADDRESS OF TX RING 15-0
31	CSR31	BASE ADDRESS OF TX RING 31-16
32	CSR32	NEXT ADDRESS OF TX RING 15-0
33	CSR33	NEXT ADDRESS OF TX RING 31-16
34	CSR34	CURRENT ADDRESS OF TX RING 15-0
35	CSR35	CURRENT ADDRESS OF TX RING 31-16
36	CSR36	RUNT BACKUP BUFFER ADDRESS 15-0
37	CSR37	RUNT BACKUP BUFFER ADDRESS 31-16
38	CSR38	RETRY BACKUP BUFFER ADDRESS 15-0
39	CSR39	RETRY BACKUP BUFFER ADDRESS 31-16
40	CSR40	CURRENT RX BYTE COUNT
42	CSR42	CURRENT TX BYTE COUNT
44	CSR44	NEXT RX/TX BYTE COUNT
46	CSR46	POLL TIME COUNT
48	CSR48	HI ADDRESS INIT BLOCK
50	CSR50	CURRENT RX STATUS
52	CSR52	CURRENT TX STATUS
54	CSR54	NEXT RX/TX STATUS
56	CSR56	RUNT BACKUP BYTE COUNT
58	CSR58	RETRY BACKUP BYTE COUNT

CONTROL AND STATUS REGISTER 0 (CSR0). RAP = 0

The ILACC updates CSR0 by logical "ORing" the previous and present values.



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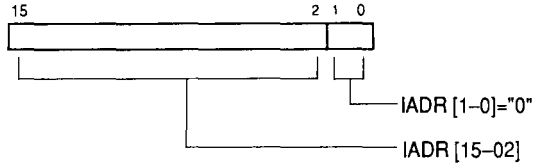
Bit	Name	Description
15	ERR	ERROR summary is set by the "OR" of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only; write operations are ignored.
14	BABL	BABBLE is a transmitter time-out error. It indicates that the transmitter has been on the channel longer than the time required to send the maximum length packet. BABL indicates excessive length in the transmit buffer. It will be set after 1519 data bytes have been transmitted. The chip will continue to transmit until the byte count equals zero. When BABL is set, an $\overline{\text{INTR}}$ interrupt will be generated providing INEA = 1 and the mask bit BABLM (CSR3 bit 14) is clear. BABL is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
13	CERR	COLLISION ERROR indicates that the collision input to the chip failed to activate within 20 network bit times after a chip initiated transmission was completed (20 bit times window commences on the rising edge of CRS). The collision after transmission is a transceiver test feature. CERR will not cause an interrupt to be generated ($\overline{\text{INTR}}$ = 0, $\overline{\text{INTR}}$ line unaffected). CERR is READ/CLEAR only. It is set by the chip, and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the stop bit.
12	MISS	MISSED PACKET is set when the receiver loses a packet, because it does not own a receive buffer and the FIFO has overflowed, indicating loss of data. FIFO overflow is not reported, because there is no receive ring entry in which to write status. When MISS is set, an $\overline{\text{INTR}}$ interrupt will be generated providing INEA = 1, and the mask bit MISSM (CSR3 bit 12) is clear. MISS is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
11	MERR	MEMORY ERROR is set when the chip is the Bus Master and has not received a "ready" indication from memory within 512 XCLK counts (i.e., 25.6µs for 20-MHz network data rate) after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off, and an $\overline{\text{INTR}}$ interrupt will be generated, providing INEA = 1 and the mask bit MERRM (CSR3 bit 11) is clear. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
10	RINT	RECEIVER INTERRUPT is set after the ILACC has completed a received packet and toggled the $\overline{\text{OWN}}$ bit in the last Receive Descriptor Ring in the chain. When RINT is set, the $\overline{\text{RINTR}}$ interrupt will be generated, providing INEA = 1 and the mask bit RINTM (CSR3 bit 10) is clear. The interrupt summary bit, $\overline{\text{INTR}}$, will also be set, but the condition of the external $\overline{\text{INTR}}$ line is unaffected by the state of RINT. RINT is READ/CLEAR ONLY and set only by the chip. It can be cleared by writing a "1" into the bit, (writing a "0" has no effect), by the application of $\overline{\text{RESET}}$ or by setting the STOP bit.
09	TINT	TRANSMITTER INTERRUPT is set after the ILACC has completed a transmitted packet and toggled the $\overline{\text{OWN}}$ bit in the last Transmit Descriptor Ring in the chain. When TINT is set, an $\overline{\text{INTR}}$ interrupt will be generated providing INEA = 1 and the mask bit TINTM (CSR3 bit 09) is clear. TINT is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.
08	IDON	INITIALIZATION DONE indicates that the chip has completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an $\overline{\text{INTR}}$ interrupt will be generated, providing INEA = 1 and the mask bit IDONM (CSR3 bit 8) is clear. IDON is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has not effect. It is also cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

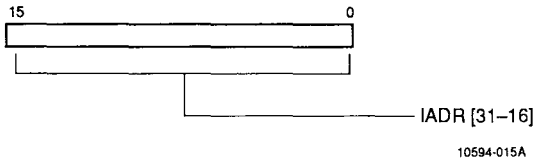
Bit	Name	Description
07	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt-causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON, LBD or TXSTRT; and its associated mask bit is clear. If INEA = 1 and $\overline{INTR}$ = 1, the $\overline{INTR}$ output pin will become active when any one or more of the above interrupt flags is set, with the exception of RINT. $\overline{INTR}$ is READ ONLY; writing this bit has no effect. $\overline{INTR}$ is cleared by $\overline{RESET}$, by setting the STOP bit, or by clearing the relevant interrupt bit(s).
06	INEA	INTERRUPT ENABLE will cause an external $\overline{INTR}$ to be generated for any of the following interrupt bits set in CSR0 (providing the associated mask bit in CSR3 is clear): BABL, MISS, MERR, TINT or IDON, as well as LBE and TXSTRT in CSR4 (providing the mask bits in CSR4 are clear). Note that RINT will not cause the $\overline{INTR}$ line to be asserted. If INEA = 1 and $\overline{INTR}$ = 1 (caused by any interrupt flag except RINT), the $\overline{INTR}$ pin will be low. If INEA = 0, the $\overline{INTR}$ pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE and can be cleared by the host, by $\overline{RESET}$ or by setting the STOP bit.
05	RXON	RECEIVER ON indicates that the receiver is enabled. RXON is set when STRT is set, if DRX = 0 in the MODE register of the initialization block (and the initialization block has been read by the chip by setting the INIT bit). RXON is cleared when IDON is set and DRX = 1 in the MODE register, or if a memory error (MERR) has occurred. RXON is READ ONLY; writing this bit has no effect. RXON is cleared by $\overline{RESET}$ or by setting the STOP bit.
04	TXON	TRANSMITTER ON indicates that the transmitter is enabled. TXON is set when STRT is set if DTX = 0 in the MODE register of the initialization block and the INIT bit has been set. TXON is cleared when IDON is set and DTX = 1 in the MODE register, if a memory error (MERR) has occurred, or if transmitter underflow occurs (UFLO in transmit descriptor entry). TXON is READ ONLY; writing this bit has no effect. TXON is cleared by $\overline{RESET}$ or by setting the STOP bit.
03	TDMD	TRANSMIT DEMAND, when set, causes the chip to access the Transmit Descriptor Ring without waiting for the polltime interval to elapse. TDMD need not be set to transmit a packet, it merely hastens the chip's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by $\overline{RESET}$ or by setting the STOP bit. Writing a "0" in this bit has no effect.
02	STOP	STOP disables the chip from all external activity when set and clears the internal logic. The chip remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set. STOP is READ/WRITE WITH ONE ONLY and set by $\overline{RESET}$. Writing a "0" to this bit has no effect. STOP is cleared by setting either INIT or STRT.
01	STRT	START enables the chip to send and receive packets, perform direct memory access and do buffer management. Setting STRT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first. STRT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. STRT is cleared by $\overline{RESET}$ or by setting the STOP bit.
00	INIT	INITIALIZE, when set, causes the chip to begin the initialization procedure and access the Initialization Block. Setting INIT clears the STOP bit. If STRT and INIT are set together, the INIT function will be executed first. INIT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. INIT is cleared by $\overline{RESET}$ or by setting the STOP bit. The ILACC does not internally clear the INIT bit on completion of the initialization procedure.

CONTROL AND STATUS REGISTER 1 (CSR1).
RAP = 1
READ/WRITE accessible only when the STOP bit in CSR0 is set. Unaffected by $\overline{\text{RESET}}$.



Bit	Name	Description
15-00	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Bits 00 and 01 must be zero. Used with CSR2 to form the base address of the Initialization Block in host memory.

CONTROL AND STATUS REGISTER 2 (CSR2).
RAP = 2
READ/WRITE accessible only when the STOP bit in CSR0 is set. CSR2 is unaffected by $\overline{\text{RESET}}$.

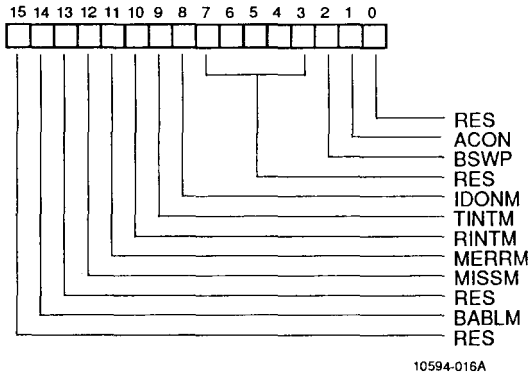


Bit	Name	Description
15-00	IADR	The high order 16 bits of the base address for the Initialization Block in host memory. Used with CSR1 to form the full 32 bit base address of theInitialization Block.

CONTROL AND STATUS REGISTER 3 (CSR3).
RAP = 03
Only accessible when the STOP bit in CSR0 is set. CSR3 is cleared by $\overline{\text{RESET}}$.

CSR3 allows redefinition of the Bus Master interface and masking of selected interrupts.

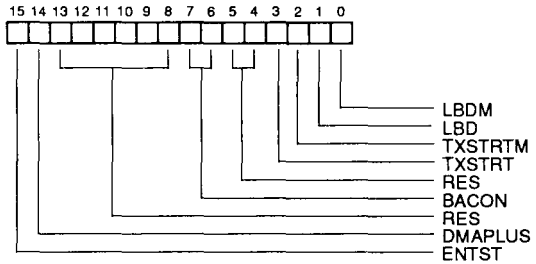
All other bits will be read as zeroes, regardless of data during write operations.



Bit	Name	Description
15	RES	RESERVED and read as zero.
14	BABLM	BABBLE MASK. If BABLM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ will remain inactive, regardless of the state of BABL in CSR0.
13	RES	RESERVED and read as zero in all modes.
12	MISSM	MISSED PACKET MASK. If MISSM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ will remain inactive, regardless of the state of MISS in CSR0.
11	MERRM	MEMORY ERROR MASK. If MERRM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ will remain inactive, regardless of the state of MERR in CSR0.
10	RINTM	RECEIVE INTERRUPT MASK. If RINTM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{RINTR}}$ will remain inactive, regardless of the state of RINT in CSR0.
09	TINTM	TRANSMIT INTERRUPT MASK. If TINTM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ will remain inactive, regardless of the state of TINT in CSR0.
08	IDONM	INITIALIZATION DONE MASK. If IDONM is set, the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ will remain inactive, regardless of the state of IDON in CSR0.
07-03	RES	RESERVED and read as zeroes.
02	BSWP	BYTE SWAP. BSWP is read only and indicates whether the chip is programmed for systems that consider bits 00-07 on the data bus to be the most significant byte. When BSWP = 1, the chip will swap high-order bytes for low-order bytes on DMA data transfers between the FIFO and bus memory. Only data from the FIFO transfer is swapped; Initialization Block data and Descriptor Ring entries are not swapped. Byte swapping and the state of BSWP is controlled by the BACON bits, writing BSWP will have no effect.
01	ACON	ALE CONTROL. Defines the assertive state of ALE/$\overline{\text{AS}}$ when the chip is the Bus Master. ACON = 0: ALE (falling edge latches address). ACON = 1: $\overline{\text{AS}}$ (rising edge latches address). ACON is READ/WRITE and cleared by $\overline{\text{RESET}}$. The state of ACON is unaffected by STOP.
00	RES	RESERVED and read as zero.

CONTROL AND STATUS REGISTER 4 (CSR4).
RAP = 04

CSR4 controls selected diagnostic functions, microprocessor bus acquisition and DMA signaling. CSR4 can be accessed regardless of the state of the STOP bit. CSR4 is cleared by $\overline{\text{RESET}}$.



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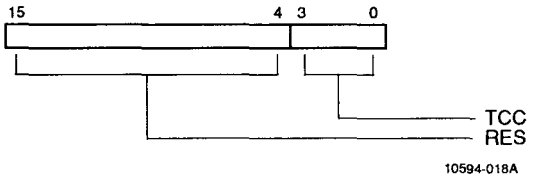
Bit	Name	Description
15	RES	RESERVED. Written and read as zero only.
14	DMAPLUS	DMAPLUS = 1, allows a DMA burst transfer to continue until the internal FIFO is empty or full, or until preempted. When DMAPLUS = 0, the 16-byte burst mode is selected. Cleared by $\overline{\text{RESET}}$, unaffected by STOP. Note that DMAPLUS affects the minimum transmit buffer size, for the first buffer in a chain. The first buffer should be a minimum of 100 bytes with DMAPLUS = 0, and increased to 116 bytes minimum with DMAPLUS = 1. This guarantees the ILACC can retransmit the packet if a collision occurs within the slot time.
13-08	RES	RESERVED and read as zeroes only.
07-06	BACON	BUS ACQUISITION CONTROL is used to optimally mate the ILACC with various microprocessor and system buses.The BACON bits will override the programming of BSWP (see table below). BACON is READ/WRITE and cleared by $\overline{\text{RESET}}$, but unaffected by the STOP bit in CSR0.
05-04	RES	RESERVED and read as zero only.
03	TXSTRT	TRANSMIT START status bit is set each time the ILACC attempts to begin a transmission (at the start of preamble). The $\overline{\text{INTR}}$ bit in CSR0 will be set if TXSTRTM is clear, and an $\overline{\text{INTR}}$ interrupt will be generated if INEA is set. TXSTRT is cleared by writing a "1" to its bit position, or by activating $\overline{\text{RESET}}$ or STOP. Unaffected by writing a "0".
02	TXSTRTM	TRANSMIT START MASK enables or disables the generation of the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ interrupt associated with TXSTRT. Cleared by $\overline{\text{RESET}}$ or STOP.
01	LBE	Asserted when transmit packet size exceeds the recommended 4-byte limit. In this case, the FIFO will overflow while filling. When LBE is set, STOP and INTR are also set. Cleared by writing a "1" or by hardware reset.
00	LBEM	LOOPBACK DONE MASK enables or disables the generation of the $\overline{\text{INTR}}$ bit and the external $\overline{\text{INTR}}$ interrupt associated with LBE. Cleared by $\overline{\text{RESET}}$ or STOP.

BACON	Bus Configuration	BSWP*
00	32 bit 80X86	0
01	32 bit 680X0	1
10	Reserved	X
11	Reserved	X

** NOTE : BSWP is read only. The swapping function is programmed in accordance with the Bus Acquisition Control (BACON) bits in CSR4.*

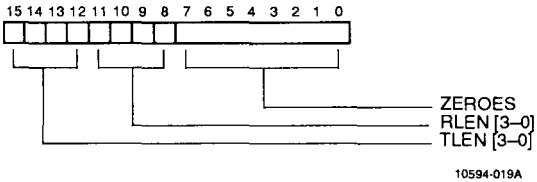
USER READABLE REGISTERS

TRANSMIT COLLISION COUNT (CSR5).
Contains the number of retry attempts to transmit the current buffer. Written into the transmit descriptor table entry when either a successful transmission has been completed, or the transmission was aborted due to excessive retries. Read only access when STOP = 1. See the description of the transmit descriptor table for further details.



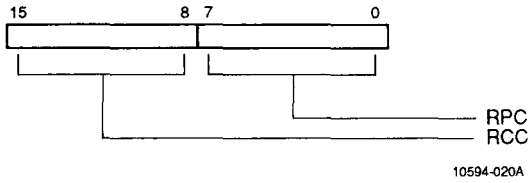
RX/TX DESCRIPTOR TABLE LENGTH (CSR6).
Contains a copy of the RLEN and TLEN bits, read from user memory during the initialization sequence. Read only access when STOP = 1.

See the description of the Initialization Block for further details.

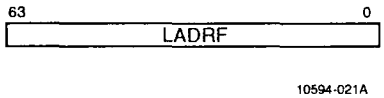


RECEIVE COLLISION/RUNT PACKET COUNT (CSR7)
The Receive Collision Count indicates the number of collisions detected on the network since the last received packet. The value is written into the receive descriptor table entry when a successful reception has been completed. The RCC will be reset immediately after the OWN bit for the descriptor is cleared by the ILACC, or upon a host read. Read only access when STOP = 1. See the description of the receive descriptor table entries for further details.

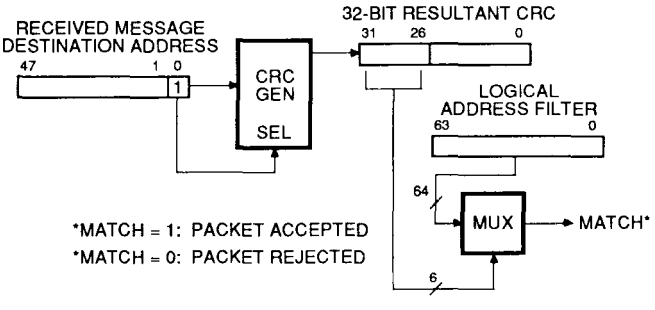
The Runt Packet Count indicates the number of runt packets (less then 64 bytes) addressed to the node since the last successfully received packet. The value is written to the receive descriptor table entry when a successful reception has been completed. The RCC will be reset immediately after the OWN bit for the descriptor is cleared by the ILACC, or upon a host read. Read only access when STOP = 1. See the description of the receive descriptor table entries for more details.



LOGICAL ADDRESS FILTER (CSR8-11)
READ ONLY access, when the STOP bit is set.



Bit	Name	Description
63-00	LADRF	The 64-bit mask that is used to accept incoming Logical Addresses. The Logical Address Filter is a read only copy of the entry of the same name in the Initialization Block. The value is updated only when the Initialization Block is read (INIT = 1). If the least significant address bit of a received message is set (PADR bit 00 = 1), then the address is deemed logical, and passed through the CRC generator. After processing the 48-bit destination address, a 32-bit resultant CRC is produced and strobed into a register. The high order 6 bits of this resultant CRC are used to select one of the 64-bit positions in the Logical Address Filter (see diagram). If the selected filter bit is a "1," the address is accepted and the packet will be placed in memory.



LOGICAL ADDRESS FILTER OPERATION

The first bit of the incoming address must be a "1" for a logical address. If the first bit is a "0," it is a physical address and is compared against the physical address that was loaded through the Initialization Block.

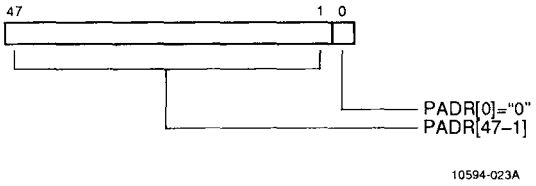
The Logical Address Filter is used in multicast addressing schemes. The acceptance of the incoming frame based on the filter value indicates that the message may be intended for the node. It is the user's responsibility to determine if the message is actually intended for the node by comparing the destination address of the stored message with a list of acceptable logical addresses.

The Broadcast address, which is all ones, does not go through the Logical Address Filter and is always enabled. If the Logical Address Filter is loaded with all zeroes (and PROM = 0), all incoming logical addresses except Broadcast will be rejected.

The multicast addressing in external loopback is operational only when DTCR = 1 in the Mode Register.

PHYSICAL ADDRESS REGISTER (CSR12-14)

READ ONLY access when the STOP bit is set.

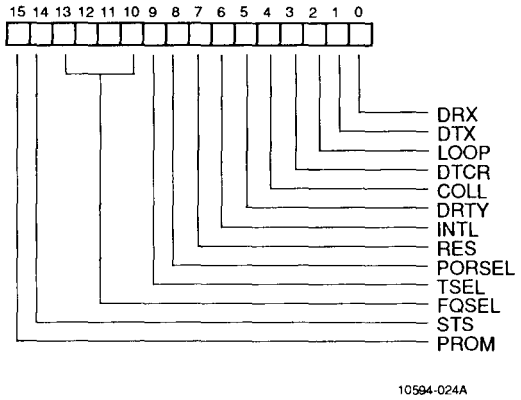


Bit	Name	Description
47-00	PADR	PHYSICAL ADDRESS is the unique 48-bit physical address assigned to the chip. PADR[0] must be zero. The Physical Address value is a read only copy of the entry of the same name in the Initialization Block. This internal copy is updated only when the Initialization Block is read (INIT = 1).

MODE REGISTER (CSR15)

The MODE Register is a read only copy of the entry of the same name in the Initialization Block. This internal copy is updated only when the Initialization Block is read (INIT = 1), and will be cleared by $\overline{\text{RESET}}$.

The MODE Register entry in the Initialization Block (located in user memory) permits alteration of the chip's operating parameters and provides the programming options for the internal SIA and/or general purpose interface port. Normal operation is with the Mode Register clear.



Bit	Name	Description
15	PROM	PROMISCUOUS Mode. When PROM = 1, all incoming packets are accepted.
14-10	RES	RESERVED and read as zero only.
09	TSEL	TRANSMIT MODE SELECT. TSEL = 0: In the idle transmit state, XMIT+ and XMIT- are equal, providing "zero" differential to operate transformer coupled loads. Delay and output return to zero are controlled internally. TSEL High: In Idle transmit state XMIT+ is positive with respect to XMIT-.
08	PORTSEL	PORT SELECT allows the chip to select between the IEEE standard Attachment Unit Interface (AUI) using the internal SIA, or the general purpose serial interface (GPSI) to drive an independent device. When PORTSEL = 1, the general purpose port is selected. During the selection of the internal SIA, the GPSI outputs should be left unconnected and inputs should be tied to ground. Cleared by $\overline{\text{RESET}}$, unaffected by STOP.If Internal Loopback is enabled (MODE Register, bits 2 and 6) the state of PORTSEL is ignored, and the serial bit stream is looped back prior to the Manchester Encoder section of the ILACC.
07	RES	RESERVED. Read as zero.
06	INTL	INTERNAL LOOPBACK (INTL = 1) selects Internal Loopback and is used with the LOOP bit to determine where the loopback is to be done. Internal Loopback allows the chip to receive its own transmitted packet. The condition of PORTSEL does not effect the operation of Internal Loopback and the data stream is looped back prior to the integral SIA. Since this represents full duplex operation, the packet size is limited to 32 bytes. Only packets which the node addresses to itself will be accepted. Packets addressed to the node from other nodes will not be accepted. EXTERNAL LOOPBACK (INTL = 0) permits the ILACC to transmit a packet out to the physical medium, either using the internal SIA, or via the general purpose serial interface (determined by PORTSEL, CSR15 bit 8). If PORTSEL = 0, the internal SIA will used, and the transmit/receive path will be tested to the physical medium (via external transceiver). If PORTSEL = 1, the general purpose interface will be exercised. Multicast addressing in External Loopback is valid only when DTCR = 1 (user must append 4 byte CRC to packet). Packets addressed to the node from other nodes will be accepted. INTL is only valid if LOOP = 1; otherwise it is ignored.
05	DRTY	DISABLE RETRY. When DRTY = 1, the chip will attempt only one transmission of a packet. If there is a collision on the first transmission attempt, a Retry Error (RTRY) will be reported in the TDTE. The RTRY error flag appears in TMD2.
04	COLL	FORCE COLLISION. This bit allows the collision logic to be tested. The chip must be in internal loopback for COLL to be valid. If COLL = 1, a collision willbe forced during the subsequent transmission attempt. This will result in 16 total transmission attempts with a re- try error reported in TMD2.
03	DTCR	DISABLE TRANSMIT CRC. When DTCR = 0, the transmitter will generate and append a CRC to the transmitted packet. When DTCR = 1, the CRC logic is allocated to the receiver and no CRC is generated or sent with the transmitted packet.
02	LOOP	LOOPBACK allows the chip to operate in full duplex mode for test purposes. When LOOP = 1, loopback is enabled. The loopback packet size is user selectable. The CRC is calculated over the entire packet, although only the last 4 to 48 bytes of data from the packet will be returned to user memory. Regardless of the data field length of the received packet, the last 4 bytes will contain the CRC. If DTCR = 0, the 4 byte CRC generated and appended at transmit time, will be stored in user memory after the (0–44 byte) data field. If DTCR = 1, the user-calculated CRC must be contained in the last 4 bytes of the transmit buffer. The receiver will generate a comparison to check against the transmitted CRC, which will be loaded into the last 4 bytes of the received buffer. Transmission in loopback mode begins when the first 16 bytes of data are in the FIFO. Transmit and receive data chaining may be performed in these modes of operation.
01	DTX	DISABLE THE TRANSMITTER causes the chip to not access the Transmitter Descriptor Ring and therefore no transmissions are attempted. DTX = 1 will clear the TXON bit in CSR0 when initialization is complete.
00	DRX	DISABLE THE RECEIVER causes the chip to reject all incoming packets and not access the Receive Descriptor Ring. DRX = 1 will clear the RXON bit in CSR0 when initialization is complete.

INITIALIZATION BLOCK ADDRESS (CSR16-17)
A read only copy of the start address of the Initialization Block located in user memory, as programmed in CSR1 and CSR2.

CURRENT RX BUFFER ADDRESS (CSR18-19)
Contains the current receive buffer address the ILACC will use to dump an incoming packet. If the ILACC was stopped while receiving a packet, it will be the address of the incompleted buffer the ILACC was using. The address is 32 bits wide.

CURRENT TX BUFFER ADDRESS (CSR20-21)
Contains the address of the transmit buffer the ILACC transmitted last. In the event the ILACC was stopped while transmitting, it will contain the address of the incompleted buffer the ILACC was using. The address is 32 bits wide.

NEXT RX/TX BUFFER ADDRESS (CSR22-23)
Since the ILACC can only operate in half duplex, this register is shared depending on the condition of the ILACC at any time (i.e., transmit or receive). When the ILACC is transmitting, the register contains the address of the transmit buffer the ILACC will attempt to transmit next. When the ILACC is receiving, it will contain the address of the next receive buffer in which the ILACC will dump incoming packet data. In both cases, the ILACC will read the value during buffer lookahead, while it is dealing with the current buffer. The address is 32 bits wide.

BASE ADDRESS OF RX RING (CSR24-25)
Contains the base address of the receive descriptor table entries in user memory. The value is a read only copy of the value obtained from the Initialization Block at initialization time. The address is 32 bits wide.

NEXT ADDRESS OF RX RING (CSR26-27)
Contains the address of the next receive descriptor that the ILACC will use. The ILACC will calculate this address based on the current descriptor address and the descriptor entry length. It will poll the next descriptor during lookahead, to determine if a receive buffer is available and its location. The address is 32 bits wide.

CURRENT ADDRESS OF RX RING (CSR28-29)
Contains the address of the receive descriptor that the ILACC will use for the next incoming packet. If the ILACC was stopped during reception, it will contain the descriptor address of the incompleted message. The ILACC uses the address to examine the descriptor, to determine if a receive buffer is available, locate it, and indicate the condition and length of the received data. The address is 32 bits wide.

BASE ADDRESS OF TX RING (CSR30-31)
Contains the base address of the transmit descriptor table entries in user memory. The value is a read only copy of the value obtained from the Initialization Block at initialization time. The address is 32 bits wide.

NEXT ADDRESS OF TX RING (CSR32-33)
Contains the address of the next transmit descriptor that the ILACC will use. The ILACC will calculate this address based on the current descriptor address and the descriptor entry length. It will poll the next descriptor during lookahead, to determine if a transmit buffer is available, and its location. The address is 32 bits wide.

CURRENT ADDRESS OF TX RING (CSR34-35)
Contains the address of the transmit descriptor that the ILACC will use for the next outgoing packet. If the ILACC was stopped during transmission it will contain the descriptor address of the incompleted message. The ILACC uses the address to examine the descriptor, to determine if a transmit buffer is available, locate it, and indicate the condition of the transmitted data. The address is 32 bits wide.

RUNT BACKUP BUFFER ADDRESS (CSR36-37)
Contains a copy of the current receive buffer address. In the event that the receive packet is identified as a runt, the Runt Backup Buffer Address is written back into the Current Rx Buffer Address. The address is 32 bits wide.

RETRY BACKUP BUFFER ADDRESS (CSR38-39)

CURRENT RX BYTE COUNT (CSR40)
Contains a copy of the current receive descriptor byte count as read from the current receive descriptor.

CURRENT TX BYTE COUNT (CSR42)
Contains a copy of the current transmit descriptor byte count as read from the current transmit descriptor.

NEXT RX/TX BYTE COUNT (CSR44)
Since the ILACC can only operate in half duplex, this register is shared depending on the condition of the ILACC at any time (i.e., transmit or receive). During transmission, it contains the transmit buffer byte count as read from the next transmit descriptor entry during lookahead. During reception, it contains the buffer byte count as read from the next receive descriptor entry during lookahead.

POLL TIME COUNT (CSR46)
The Poll Time Count is a copy of the internal roll over counter, which determines the frequency at which the ILACC will inspect the transmit descriptor ring entry.

HI ADDRESS INIT BLOCK (CSR48)
Contains a copy of the contents of CSR2 at initialization time.

CURRENT RX STATUS (CSR50)
Contains a copy of the current receive descriptor status byte as read from the current receive descriptor.

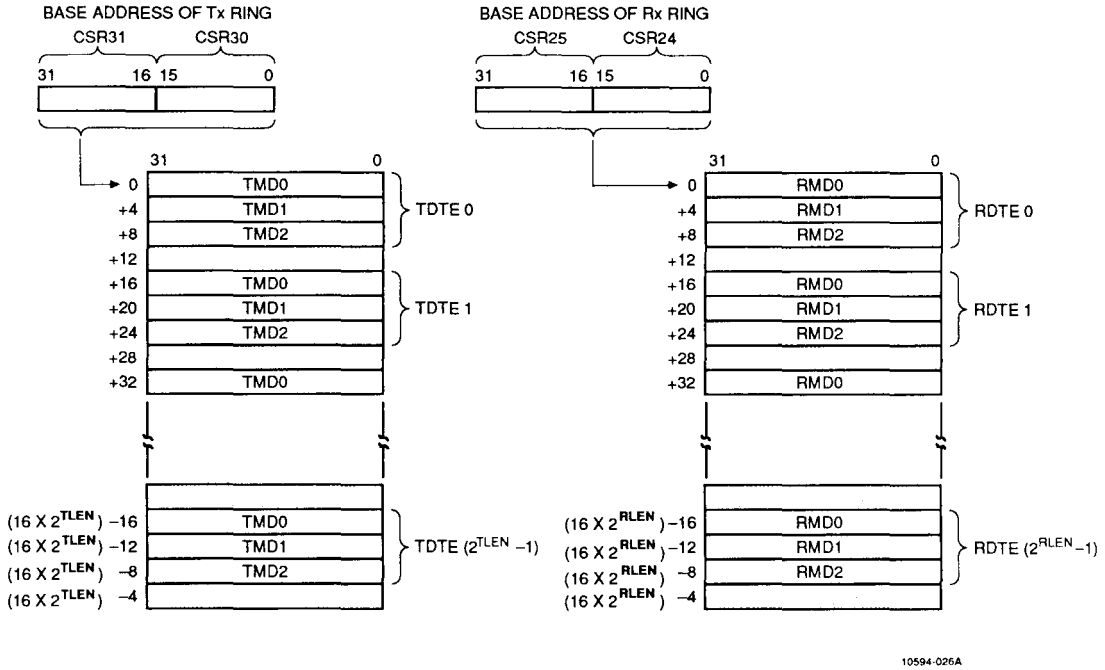
CURRENT TX STATUS (CSR52)
Contains a copy of the current transmit descriptor status byte as read from the current transmit descriptor.

NEXT RX/TX STATUS (CSR54)
Since the ILACC can only operate in half duplex, this register is shared depending on the condition of the ILACC at any time (i.e., transmit or receive). During transmission, it contains the transmit status byte as read from the next transmit descriptor entry during lookahead. During reception, it contains the status byte as read from the next receive descriptor entry during lookahead.

RUNT BACKUP BYTE COUNT (CSR56)
Contains a copy of the current receive buffer byte count. In the event that the receive packet is identified as a runt, the Runt Backup Byte Count is written back into the Current Rx Byte Count.

RETRY BACKUP BYTE COUNT (CSR58)
Contains a copy of the current transmit buffer byte count. In the event that the transmit packet suffers a collision, the Retry Backup Byte Count is written back into the Current Tx Byte Count.

DESCRIPTOR TABLE CONTENT



INITIALIZATION

PROCEDURE AND FLOWCHART

ILACC initialization includes the reading of the initialization block in memory to obtain the operating parameters. The initialization block is read when the INIT bit in CSR0 is set. The INIT bit should be set before or concurrent with the STRT bit to insure correct operation. On completion of the read operation and after internal registers have been updated, the IDON will be set in CSR0, and an interrupt generated if INEA is set.

The Initialization Block is vectored by the contents of CSR1 (least significant word of address) and CSR2 (most significant word of address). The block is resident in host memory, and contains the user defined conditions for ILACC operation, together with the address and length information to allow linkage of the transmit and receive descriptor rings.

MODE REGISTER

The Mode Register defines the transmit/receive operation of the ILACC. At initialization, this user-defined value is stored in CSR15.

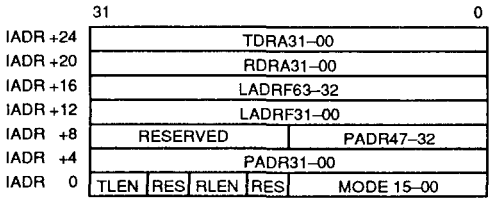
LOGICAL ADDRESS FILTER (LADRF)

The filter value used for multicast addressing. Stored in CSR8-11 during initialization.

PHYSICAL ADDRESS REGISTER (PADR)

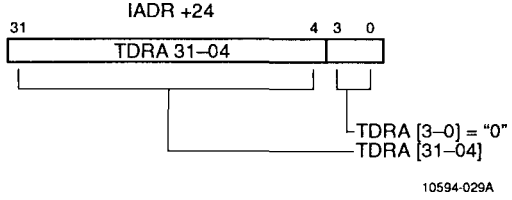
The individual node address assigned to the ILACC, and stored in CSR12-14 during initialization.

INITIALIZATION BLOCK



TRANSMIT DESCRIPTOR RING ADDRESS (TDRA)

The base address (lowest address) of the user area where the transmit descriptor ring is located. This is a full 32-bit address and is stored in the ILACC during initialization.



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The least significant 4 bits of the ring base address must be zero.

TRANSMIT DESCRIPTOR RING LENGTH (TLEN)

TLEN defines the number of TDTEs which will be used in the ring. TLEN is located at the base location of the Initialization Block (IADR + 0) with the Mode Register and the RLEN entry. A maximum of 512 transmit descriptor entries is permitted.

TLEN has a four bit field. The user is free to write any 4-bit code into this field. Binary values greater than 9 (e.g., TLEN = 1111b) will be stored as written, and the ILACC will expect 512 TDTEs.

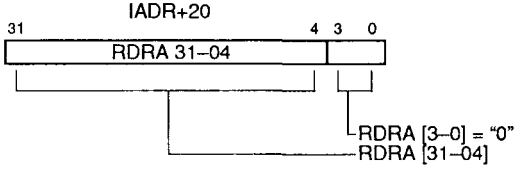
TLEN is expressed as a power of two, as follows:

TLEN				No. of TDTEs
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	512

Note that the field is stored in CSR6 during initialization. For details, refer to the definition within the Description of User Accessible Resources.

RECEIVE DESCRIPTOR RING ADDRESS (RDRA)

The base address of the user area where the receive descriptor ring is located. This is a full 32-bit address, and is stored in the ILACC during initialization.



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The least significant four bits of the ring base address must be zero.

RECEIVE DESCRIPTOR RING LENGTH (RLEN)

RLEN defines the number of RDTEs which will be used in the ring. RLEN is located at the base location of the Initialization Block (IADR+0) with the MODE Register and the TLEN entry. Maximum of 512 transmit descriptor entries are permitted.

RLEN is expressed as a power of two, as follows:

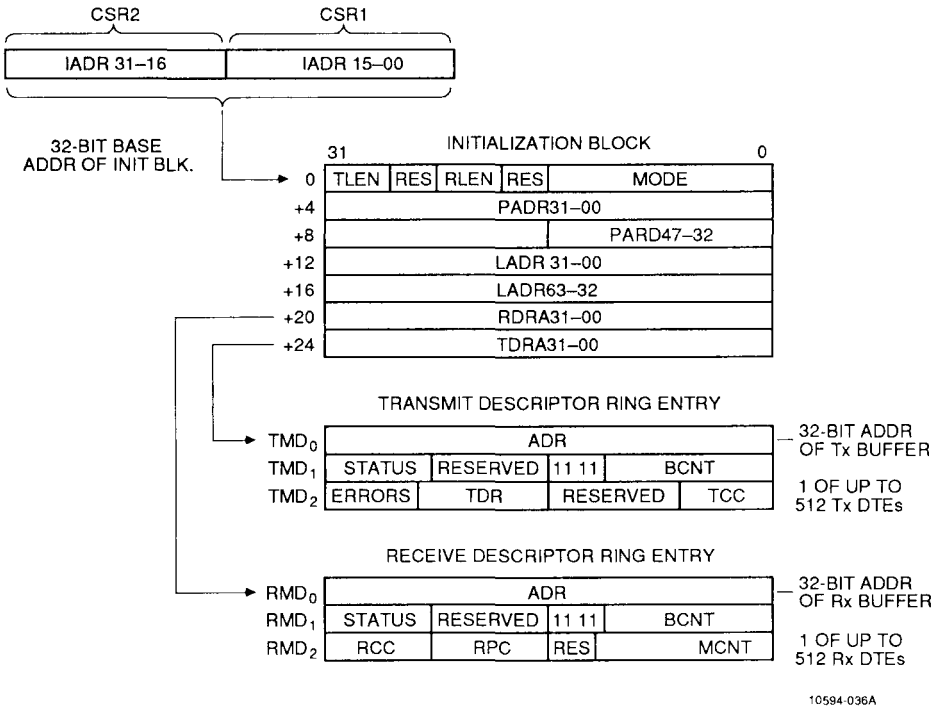
RLEN				No. of RDTEs
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	512

RLEN has a 4-bit field. The user is free to write any 4-bit code into this field. Binary values greater than 9 (i.e., RLEN = 1111b) will be stored as written, and the ILACC will expect 512 RDTEs.

Note that the field is stored in CSR6 during initialization. For details, refer to the definition within the Description of User Programmable Registers.

INITIALIZATION BLOCK LAYOUT

Programmer's Model



Reinitialization

The transmitter and receiver section of the ILACC are turned on via the initialization block (MODE Register: DRX, DTX bits). The state of the transmitter and receiver can be monitored through CSR0 (RXON, TXON bits). The ILACC must be reinitialized if the transmitter and/or the receiver were not turned on during the original initialization, and it is subsequently required to activate them. Alternatively, the ILACC may require reinitialization if either section shuts off due to the detection of an error condition (MERR, UFLO, TX BUFF error). Care must be taken when the ILACC is reinitialized.

Prior to reinitialization of the ILACC, the user must set the STOP bit in CSR0. Subsequently, CSR3 must be reprogrammed since its contents are cleared when the STOP bit is set (software reset). CSR3 programming is not needed when default values for ACON are used. CSR1 and CSR2 are not affected by the STOP bit. However, it is recommended that they be reloaded during the reinitialization procedure. The user should rearrange the descriptors in the transmit or the receive ring prior to re-enabling the transmit/receive functions. This is necessary since the transmit and the receive descriptor pointers are reloaded with their respective base address upon initialization. The ILACC can be reinitialized by setting the INIT bit in CSR0).

An alternate method of starting the ILACC, once it has stopped, is by setting the STRT bit in CSR0. The STRT bit puts the ILACC in operation in accordance with the parameters defined in the MODE register. If DTX and/or DRX are "0" in the MODE register, the transmitter or the receiver will be turned on again when STRT is set.

This approach may appear an easier task than the reinitialization mechanism, where the user is required to rearrange the descriptors in the rings. However, it is not recommended if the ILACC was stopped during the transmission or the reception of a packet or when the buffers are data chained.

Buffer Management

Buffer management is accomplished through message descriptors organized as ring structures in memory. There are two rings, a receive ring and a transmit ring. Each message descriptor entry requires three double words (6 words or 12 bytes).

To simplify the maintenance of pointers for the rings, the space allocated for the transmit/receive descriptor table entries is as follows :

Descriptor Table Entries are 8 words long, located on 16-byte boundaries (bits 0-3 of pointer address must be zero).

Descriptor Rings

Each descriptor ring must be organized in a contiguous area of memory. At initialization time, the ILACC reads the user-defined base address for the transmit and receive descriptor rings, as well as the number of entries contained. Maximum of 512 ring entries is permitted.

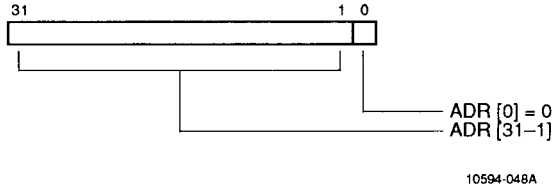
Each ring entry contains the following information:

1. The address of the actual message data buffer in user or host memory
2. The length of the message buffer
3. Status information indicating the condition of the buffer

To permit the queuing and de-queuing of message buffers, ownership of each buffer is allocated to either the ILACC or the host. The OWN bit within the descriptor status information is used for this purpose. "Deadly Embrace" conditions are avoided by the ownership mechanism. Only the owner is permitted to relinquish ownership, or to write to any field in the descriptor entry. A device that is not the current owner of a descriptor entry cannot assume ownership or change any field in the entry.

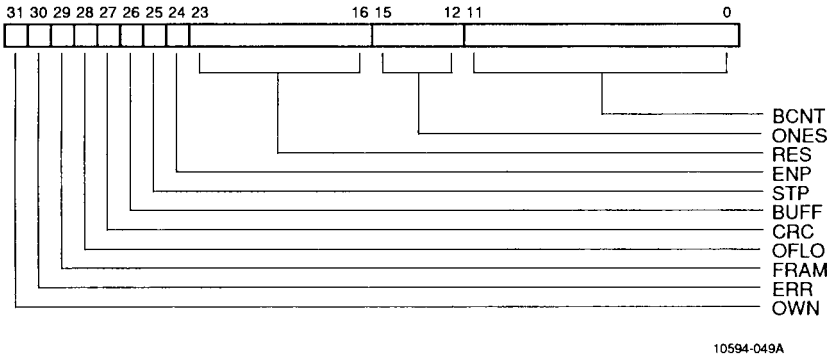
Descriptor Memory Allocation

RECEIVE MESSAGE DESCRIPTOR 0 (RMD0).



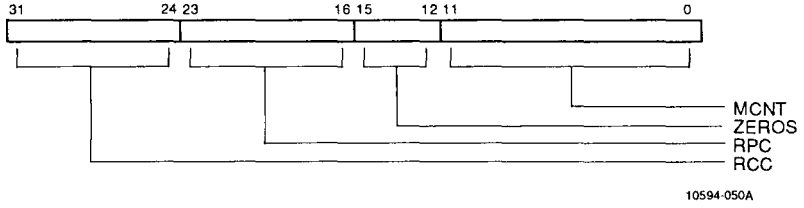
Bit	Name	Description
31-00	ADR	Address of the buffer pointed to by this descriptor. ADR is written by the host and unchanged by the ILACC. The buffer must be located on a word boundary (bit 0 must be zero).

RECEIVE MESSAGE DESCRIPTOR 1 (RMD1).



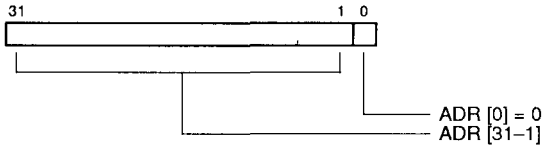
Bit	Name	Description
31	OWN	This bit indicates that the descriptor entry is owned by the host (OWN=0) or by ILACC (OWN=1). The ILACC clears the OWN bit after filling the buffer pointed to by the descriptor entry. The host sets the OWN bit after emptying the buffer. Once the ILACC or host has relinquished ownership of a buffer, it must not change any field in the three words that comprise the descriptor entry.
30	ERR	ERROR summary is the "OR" of FRAM, OFLO, CRC or BUFF. ERR is set by the ILACC and cleared by the host.
29	FRAM	FRAMING ERROR indicates that the incoming packet contained a non-integer multiple of eight bits and there was a CRC error. If there was not a CRC error on the incoming packet, then FRAM will not be set even if there was a non-integer multiple of eight bits in the packet. FRAM is not valid in internal loopback mode. FRAM is valid only when ENP is set and OFLO is not. FRAM is set by the ILACC and cleared by the host.
28	OFLO	OVERFLOW error indicates that the receiver has lost all or part of the incoming packet, due to an inability to store the packet in a memory buffer before the internal FIFO overflowed. OFLO is valid only when ENP is not set. OFLO is set by the ILACC and cleared by the host.
27	CRC	CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is valid only when ENP is set and OFLO is not. CRC is set by the ILACC and cleared by the host.
26	BUFF	BUFFER ERROR is set any time the ILACC does not own the next buffer while data chaining a received packet. This can occur in either of two ways: 1. The OWN bit of the next buffer is zero. 2. FIFO overflow occurred before the ILACC received the next STATUS. If a Buffer Error occurs, an Overflow Error may also occur internally in the FIFO, but will not be reported in the descriptor status entry unless both BUFF and OFLO errors occur at the same time. BUFF is set by the ILACC and cleared by the host.
25	STP	START OF PACKET indicates that this is the first buffer used by the ILACC for this packet. It is used for data chaining buffers. STP is set by the ILACC and cleared by the host.
24	ENP	END OF PACKET indicates that this is the last buffer used by the ILACC for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the ILACC and cleared by the host.
23-16	RES	RESERVED.
15-12	ONES	MUST BE ONES. This field is written by the host and unchanged by the ILACC.
11-00	BCNT	BUFFER BYTE COUNT is the length of the buffer pointed to by this descriptor, expressed as the two's complement of the length of the buffer. This field is written by the host and unchanged by the ILACC. Minimum buffer size is 64 bytes for the first buffer of a packet. The count should be expressed as an even number of bytes.

RECEIVE MESSAGE DESCRIPTOR 2 (RMD2)



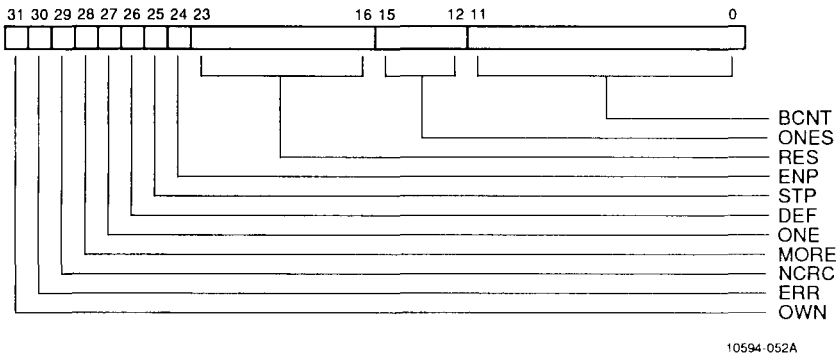
Bit	Name	Description
31-24	RCC	RECEIVE COLLISION COUNT indicates the number of collisions on the network since the last successfully received packet. The internal value of RCC in CSR7 is written to RMD2 (in the last descriptor of the chain) prior to the OWN bit being flipped (i.e., after a successful reception). The collision count in CSR7 is reset immediately after the OWN bit for the descriptor is reset, or upon a host read. The count does not roll over when more than 255 collisions are detected, but will freeze at the maximum count.
23-16	RPC	RUNT PACKET COUNT indicates the number of runt packets addressed to this node since the last successfully received packet. The internal value of RPC in CSR7 is written to RMD2 (in the last descriptor of the chain) prior to the OWN bit being flipped (i.e., after a successful reception). The runt packet counter in CSR7 is reset immediately after the OWN bit for the descriptor is reset, or upon a host read. The count will be frozen at 255 if runt packets in excess of this are detected.
15-12	ZEROS	MUST BE ZEROS. This field is written by the ILACC.
11-00	MCNT	MESSAGE BYTE COUNT is the length in bytes of the received message, expressed as an unsigned binary integer. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by the chip and cleared by the host.

TRANSMIT MESSAGE DESCRIPTOR 0 (TMD0).



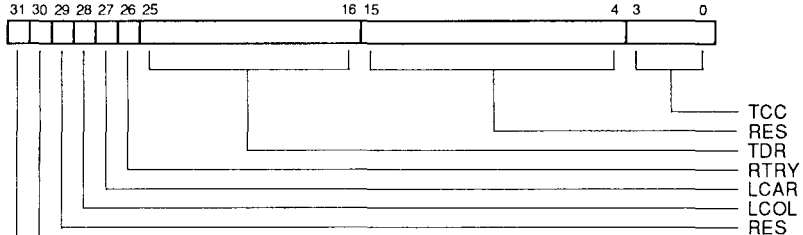
Bit	Name	Description
31-00	ADR	The 32-bit address of the buffer pointed to by this descriptor. ADR is written by the host and unchanged by the ILACC. The buffer must be located on a word boundary (bit 0 must be zero).

TRANSMIT MESSAGE DESCRIPTOR 1 (TMD1).



Bit	Name	Description
31	OWN	This bit indicates that the descriptor entry is owned by the host (OWN = 0) or by the ILACC (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by this descriptor. The ILACC clears the OWN bit after transmitting the contents of the buffer. Both the host and the ILACC must not alter a descriptor entry after relinquishing ownership.
30	ERR	ERROR summary is the "OR" of UFLO, LCOL, LCAR, or RTRY. ERR is set by the ILACC and cleared by the host.
29	NCRC	NO CRC dynamically controls the generation of CRC on a packet by packet basis. It is valid in the last descriptor of the packet to be transmitted. When NCRC=1 CRC generation is inhibited. When NCRC=0, CRC generation is activated. NCRC is set by the host and unchanged by the ILACC.
28	MORE	MORE indicates that more than one retry was needed to transmit a packet. MORE is set by the ILACC and cleared by the host.
27	ONE	ONE indicates that exactly one retry was needed to transmit a packet. The ONE flag is not valid when LCOL is set. ONE is set by the ILACC and cleared by the host.
26	DEF	DEFERRED indicates that the ILACC had to defer while trying to transmit a packet. This condition occurs if the channel is busy when the ILACC is ready to transmit. DEF is set by the ILACC and cleared by the host.
25	STP	START OF PACKET indicates that this is the first buffer to be used by the ILACC for this packet. It is used for data chaining buffers. STP is set by the host and unchanged by the ILACC. The STP bit must be set in the first buffer of the packet, or the ILACC will skip over this descriptor and poll the next descriptor(s) until the OWN and STP bits are set. STP is set by the host and unchanged by the ILACC.
24	ENP	END OF PACKET indicates that this is the last buffer to be used by the ILACC for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the host and unchanged by the ILACC.
23-16	RES	RESERVED
15-12	ONES	MUST BE ONES. Written by host.
11-00	BCNT	BUFFER BYTE COUNT is the usable length of the buffer pointed to by this descriptor, expressed as the two's complement of the buffer byte length. This is the number of bytes from this buffer that will be transmitted by the ILACC. This field is written by the host and unchanged by the ILACC. The first buffer of a packet must be a minimum of 116 bytes (DMAPLUS = 1) or 100 bytes (DMAPLUS = 0) when data chaining, and 64 bytes (DTCR=1) or 60 bytes (DTCR=0) when not data chaining. The count should be an even number of bytes for all but the last buffer in a chain.

TRANSMIT MESSAGE DESCRIPTOR 2 (TMD2).



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Bit	Name	Description
31	BUFF	BUFFER ERROR is set by the ILACC during transmission when the ILACC does not find the ENP flag in the current buffer and does not own the next buffer. This can occur if either: 1. The OWN bit of the next buffer is zero. 2. FIFO underflow occurred before the ILACC was able to read the next STATUS byte. BUFF is set by the ILACC and cleared by the host. BUFF error will turn off the transmitter (CSR0, TXON = 0). If a Buffer Error occurs, an Underflow Error will also occur. BUFF error is not valid when LCOL or RTRY error is set during transmit data chaining. BUFF is set by the ILACC and cleared by the host.
30	UFLO	UNDERFLOW ERROR indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that FIFO has emptied before the end of the packet was reached. Upon UFLO error, the transmitter is turned off (CSR0, TXON =O). UFLO is set by the ILACC and cleared by the host.
29	RES	RESERVED bit. The ILACC will write this bit with a "0."
28	LCOL	LATE COLLISION indicates that a collision has occurred after the slot time of the channel has elapsed. The ILACC does not retry on late collisions. LCOL is set by the ILACC and cleared by the host.
27	LCAR	LOSS OF CARRIER is set when the carrier is lost during an ILACC-initiated transmission. The loss is detected internally if the ILACC's integral SIA isbeing used, or via the CRS line becoming deasserted if the general purpose serial interface is utilized. The ILACC does not retry upon loss of carrier. It will continue to transmit the whole packet until done. LCAR is not valid in Internal Loopback Mode. LCAR is set by the ILACC and cleared by the host.
26	RTRY	RETRY ERROR indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DRTY = 1 in the MODE register, RTRY will set after 1 failed transmission attempt. RTRY is set by the ILACC and cleared by the host.
25-16	TDR	TIME DOMAIN REFLECTOMETRY reflects the state of an internal ILACC counter that counts from the start of a transmission to the occurrence of a collision or loss of carrier. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by the ILACC and is valid only if RTRY is set. TDR will be incremented at the BCLK rate.
15-04	RES	RESERVED
03-00	TCC	TRANSMIT COLLISION COUNT indicates the number of transmit retries of the associated packet. The maximum count is 16. Written by the ILACC into the last transmit descriptor for the message (ENP = 1), and valid only when OWN = 0.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–25°C to +125°C
Power Dissipation	1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolutely maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

COMMERCIAL (C) Devices

Temperature (Ta)	0 to +70°C
Supply Voltage (Vcc)	+4.50 to +5.50 V
Vss	0 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

AC TIMING PARAMETERS

Key: (H↓L) indicates falling edge of signal

(L↑H) indicates rising edge of signal

$\overline{\text{NAME}}$ identifies active low signal

Clock Signals

No.	Description	Min (ns)	Max (ns)
23	Network bit time: BT = 2/XCLK (Hz) (note 3)	100	1000
28	XCLK period : T_{XCLK} (note 3)	50	500
37	TXC period : T_{TXC}	99%*BT	101%*BT
38	TXC low pulse width : T_{TXCL}	45%*BT	55%*BT
39	TXC high pulse width : T_{TXCH}	45%*BT	55%*BT
40	TXC rise time (note 2)		8
41	TXC fall time (note 2)		8
46	RXC period : T_{RXC} (note 4)	85	115
47	RXC high pulse width : T_{RXCH} (note 4)	38	
48	RXC low pulse width : T_{RXCL} (note 4)	38	
49	RXC rise time (note 2)		8
65	RXC fall time (note 2)		8
84	BCLK period : T_{BCLK} <= 0.835*BT (note 3)	50	500
102	BCLK low pulse width : T_{BCLKL} (note 3)	40%*BT	60%*BT
103	BCLK high pulse width : T_{BCLKH} (note 3)	40%*BT	60%*BT

Bus Slave

No.	Description	Min (ns)	Max (ns)
79	Data In valid hold time from $\overline{\text{READYL}}$ (H↓L)	10	
80	$\overline{\text{CS}}$ (H↓L) or R/$\overline{\text{W}}$ setup time to $\overline{\text{DAS}}$ (H↓L)	5	
81	$\overline{\text{CS}}$ hold time from $\overline{\text{DAS}}$ (L↑H)	0	
82	C/$\overline{\text{D}}$ setup time to $\overline{\text{DAS}}$ (H↓L)	5	
83	C/$\overline{\text{D}}$ hold time from $\overline{\text{DAS}}$ (H↓L)	15	
85	R/$\overline{\text{W}}$ hold time from $\overline{\text{DAS}}$ (H↓L)	15	
86	$\overline{\text{DAS}}$ (L↑H) delay to $\overline{\text{DALO}}$ (L↑H)		30
87	$\overline{\text{DAS}}$ (H↓L) delay to $\overline{\text{DALO}}$ (H↓L)		30
88	$\overline{\text{DAS}}$ (L↑H) delay to $\overline{\text{DALI}}$ (L↑H)		30
89	$\overline{\text{DAS}}$ (H↓L) delay to $\overline{\text{DALI}}$ (H↓L)		30
90	$\overline{\text{DAS}}$ (L↑H) delay to $\overline{\text{READYL}}$ (L↑H) (deassertion)		T_{BCLK} + 35
92	$\overline{\text{DAS}}$ (H↓L) delay to $\overline{\text{READYL}}$ (H↓L), (note 1)		5*T_{BCLK}
93	$\overline{\text{DAS}}$ (H↓L) with $\overline{\text{CS}}$ (H↓L) delay to Data In valid		T_{BCLK} −10
94	Data Out valid setup to $\overline{\text{READYL}}$ (H↓L),	30	
95	Data In valid hold time from $\overline{\text{DAS}}$ (L↑H)	0	
96	Data Out valid hold time from $\overline{\text{DAS}}$ (L↑H)	30	2T_{BCLK} +60
97	BCLK (L↑H) delay to $\overline{\text{READYL}}$ (H↓L)	5 (note 6)	30
98	$\overline{\text{DAS}}$ (L↑H) hold time from $\overline{\text{READYL}}$ (H↓L)	0	

Bus Master

No.	Description	Min (ns)	Max (ns)
1	BCLK (H↓L) delay to ALE, $\overline{AS}$, $\overline{DAS}$, $\overline{BE}_0$–$\overline{BE}_{17}$, $\overline{SIZ}_0$–$\overline{SIZ}_{17}$, driver enabled	0	
2	BCLK (L↑H) delay to ALE/$\overline{AS}$ valid		40
3	BCLK (L↑H) delay to address valid	10 (note 6)	40
4	BCLK (L↑H) delay to bus control outputs valid		40
5	Data In valid setup to $\overline{DAS}$ (L↑H)	30	
6	Data In valid hold from $\overline{DAS}$ (L↑H)	0	
7	BCLK (H↓L) to address drive disable		35
8	Address out valid hold from ALE (H↓L)/$\overline{AS}$ (L↑H)	T_{BCLKH}–5	
9	BCLK (H↓L) delay to $\overline{DAS}$, R/$\overline{W}$ (L↑H)	10 (note 6)	30
10	BCLK (H↓L) delay to memory control/address outputs Hi-Z		40
11	BCLK (H↓L) delay to $\overline{DAS}$, (H↓L)	10 (note 6)	30
12	Ready valid setup to BCLK (L↑H)	5	
13	$\overline{DAS}$ (H↓L) delay to $\overline{READYL}$ (H↓L) (no wait states)		$1.5*T_{BCLK}$ –35
14	Ready valid hold from BCLK (L↑H)	5	
15	BCLK (H↓L) delay to $\overline{DALO}$ (H↓L)	10 (note 6)	30
16	$\overline{READYL}$ pulse width	T_{BCLK}	
18	BCLK (L↑H) delay to $\overline{DALI}$ (H↓L)	10 (note 6)	30
19	BCLK (H↓L) delay to Data Out valid		35
20	Data Out valid hold from $\overline{DAS}$ (L↑H)	T_{BCLKL}–5	
21	$\overline{DALO}$ (L↑H) hold time from $\overline{DAS}$ (L↑H)	T_{BCLKL}–5	
22	BCLK (L↑H) delay to $\overline{DALO}$ (L↑H)	10 (note 6)	30
24	BCLK (H↓L) delay to $\overline{DALI}$ (L↑H)	10 (note 6)	30
29	Address out valid setup to ALE (H↓L) / $\overline{AS}$ (L↑H)	T_{BCLK}–10	
30	Data Out valid setup to $\overline{DAS}$ (L↑H)	$2*T_{BCLK}$ –35	
35	Data In valid setup to BCLK (H↓L) (Note 5)	0	
36	Data In valid hold after BCLK (H↓L) (Note 5)	30	

Bus Acquisition

No.	Description	Min (ns)	Max (ns)
50	$\overline{HLDA}/\overline{BUSACK}$ (H↓L) setup to BCLK (H↓L)	15	
51	$\overline{BUSACK}$ (H↓L) delay to $\overline{BUSREQ}$ (L↑H) (deassertion)		T_{BCLK}+30
52	$\overline{BUSACK}$ (L↑H) hold time from BCLK (L↑H)	15	
53	$\overline{BGACK}$ (L↑H) setup to BCLK (H↓L)	15	
55	BCLK (H↓L) delay to $\overline{HOLD}$ (L↑H)		40
60	$\overline{HLDA}$ (L↑H) setup to BCLK (L↑H)	15	
61	BCLK (L↑H) delay to $\overline{HOLD}$ (L↑H)		5 Bus Clock
99	BCLK (H↓L) delay to $\overline{BGACK}$ (H↓L) and $\overline{BUSREQ}$ (L↑H)		40
100	$\overline{HOLD}$ or $\overline{HLDA}$ (L↑H) delay to $\overline{MASTER}$ (L↑H) (Preemption)		30
101	$\overline{HOLD}$ and $\overline{HLDA}$ (H↓L) delay to $\overline{MASTER}$ (H↓L)		30

Serial Timing

No.	Description	Min (ns)	Max (ns)
27	XCLK (L↑H) to XMIT+/- output		100
42	TXC (L↑H) delay to RTS (L↑H) (C_L = 50 pF)		70
43	RTS hold time from TXC (L↑H) (C_L = 50 pF)	5	
44	TXC (L↑H) delay to TXD (C_L = 50 pF)		70
45	TXD hold time from TXC (L↑H) (C_L = 50 pF)	5	
66	RXD rise time (note 2)		8
67	RXD fall time (note 2)		8
68	RXD hold time (RXC to RXD change)	5	
69	RXD setup time (RXD stable to RXC (L↑H))	40	
70	CRS low time	BT+20	
71	CDT high time	T_{TXC}+30	
72	RTS hold time from CDT (L↑H)	32*BT	40*BT
73	CRS hold time from RXC (L↑H)	0	

DC CHARACTERISTICS

Capacitance

Symbol	Description	Typ.	Units
C_{IN}	Input Pins	10	pF
C_{IO}	Bidirectional Pins*	20	pF
C_{OUT}	Output Pins	10	pF

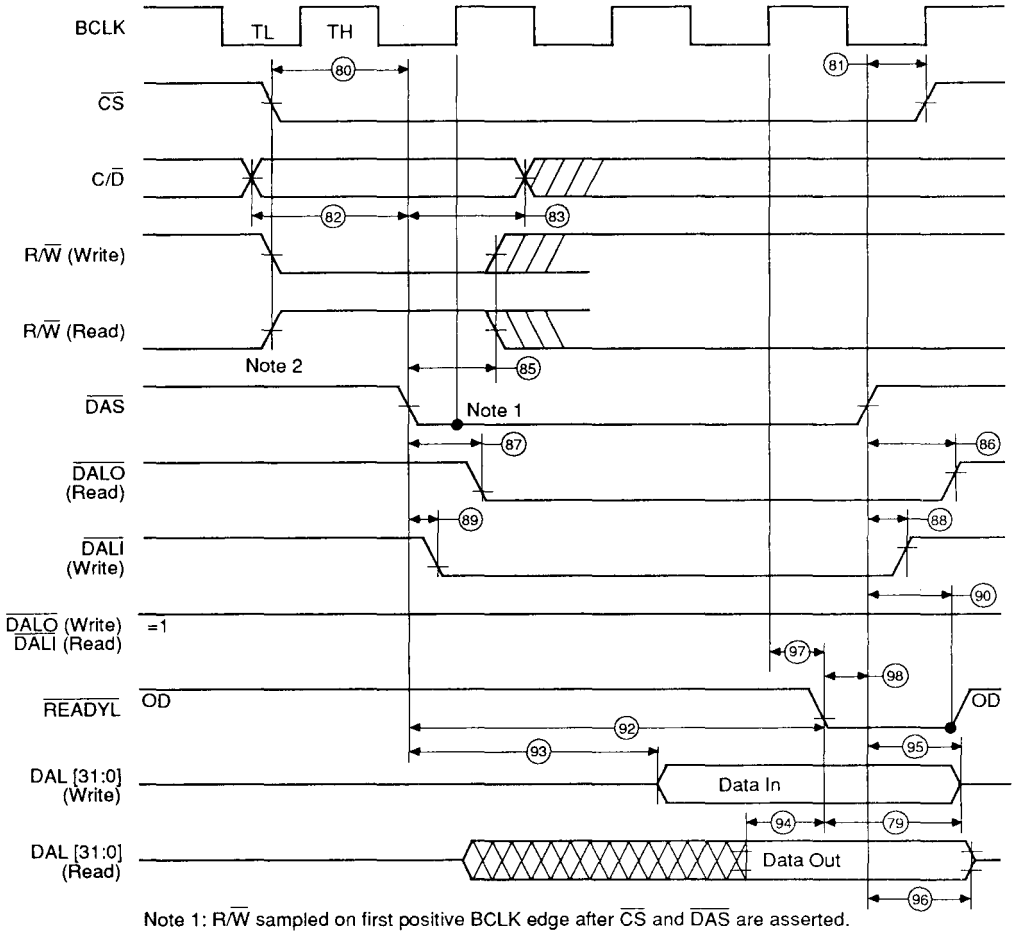
*Note: All output pins, output load capacitance C_L: 100 pF, except (20 mA sink, C_L: 200 pF), RTS (C_L: 50 pF) and TxD (C_L: 50 pF)

Symbol	Description	Test Conditions	Min	Max	Units
V_{IL}	Input LOW voltage			0.8	V
V_{IH}	Input HIGH voltage		2.0		V
V_{OL}	Output LOW voltage	I_{OL1} = 20 mA (Note 7) I_{OL2} = 4 mA		0.4	V
V_{OH}	Output HIGH voltage (note 8)	I_{OH} = -0.4 mA	2.4		V
I_{IX}	Input leakage current (note 9)	0 V<V_{IN}<VCC	–10	10	µA
I_{IXD}	RCV+/- and COLL+/- Input Low Current	VCC = 5 V, V_{IN} = 0 V	–210	–310	µA
I_{IZD}	RCV+/- and COLL+/- Input High Current	VCC = 5 V, V_{IN} = 5 V		120	µA
I_{ILX}	XTAL1 Input LOW Current	V_{IN} = TBD			
I_{IHX}	XTAL1 Input HIGH Current	V_{IN} = TBD			
I_{OZ}	Output Leakage Current (note 10)	0.4 V < V_{OUT} < VCC	–10	10	µA
V_{OD}	Differential Output Voltage: (XMIT+) - (XMIT-)	R_L = 78 Ω VO VO*	 630 –630	 870 +870	 mV mV
V_{ODOFF}	Transmit Differential Output Idle Voltage	R_L = 78 Ω (note 11)	–20	20	mV
I_{ODOFF}	Transmit Differential Output Idle Current	R_L = 78 Ω (note 12)	–325	325	µA
V_{CMT}	Transmit Output Common Mode Voltage	R_L = 78 Ω	2.5	4.2	V

Symbol	Description	Test Conditions	Min	Max	Units
V_{ODI}	Transmit Differential Output Voltage Imbalance	R_L = 78 Ω |VO| – |VO*| (note 11)		20	mV
V_{IRD}	Receive Data Differential Input Threshold		–35	35	mV
V_{IDC}	COLL+/- Differential Input Threshold		–160	–320	mV
V_{IRDVD}	RCV+/- and COLL+/- Differential Mode Input Voltage Range			±1.5	V
V_{ICM}	RCV+/- and COLL+/- Input Bias Voltage	I_{IN} = 0 mA	1.5	4.2	V
V_{ODP}	Undershoot Voltage at zero differential on transmit return to zero (end of message)	(note 13) 27 MHz ±1% and 73Ω or 83Ω ±1% resistive		-100	mV
I_{CC}	Power Supply Current	XCLK = BCLK = 20 MHz		300	mA

NOTES :

1. CSR0, 3 and 4 can be accessed within $5*T_{BCLK}$ periods. All other CSRs take $15*T_{BCLK}$ periods max.
2. Not tested.
3. Not shown on timing diagrams.
4. Characterized at 10-MHz data rate.
5. Asynchronous parameters 5 and 6 must be met. Synchronous parameters 35 and 36 can be violated if parameters 5 and 6 are met.
6. Parameter guaranteed by design—not tested.
7. IOL_1 =20 mA: DAL24–27, DAL30–31, $\overline{BUSRE2}/\overline{HOLD}$, $\overline{DAS}$, $\overline{READYL}$, R/$\overline{W}$
8. IOL_2 =4 mA: DAL0 / $\overline{BE2}$, DAL1 / $\overline{BE3}$, DAL2–23, DAL28, DAL29, ALE / $\overline{AS}$, $\overline{DALI}$, $\overline{DALO}$, $\overline{BE0}$ / SIZ0, $\overline{BE1}$ / SIZ1, $\overline{BGACK}$ / $\overline{INTR}$, $\overline{RINTR}$, XCLK, TXD, RTS, TXC.
9. V_{OH} does not apply to open-drain output pins.
10. I_{IX} applies to all input only pins except RCV+/-, COLL+/-, and XTAL1.
11. I_{OZ} applies to all three-state output pins and bidirectional pins.
12. Tested, but to values in excess of limits. Test accuracy not sufficient to allow screening guardbands.
13. Correlated to other tested parameters - not tested directly.
14. Test not implemented to data sheet specification.

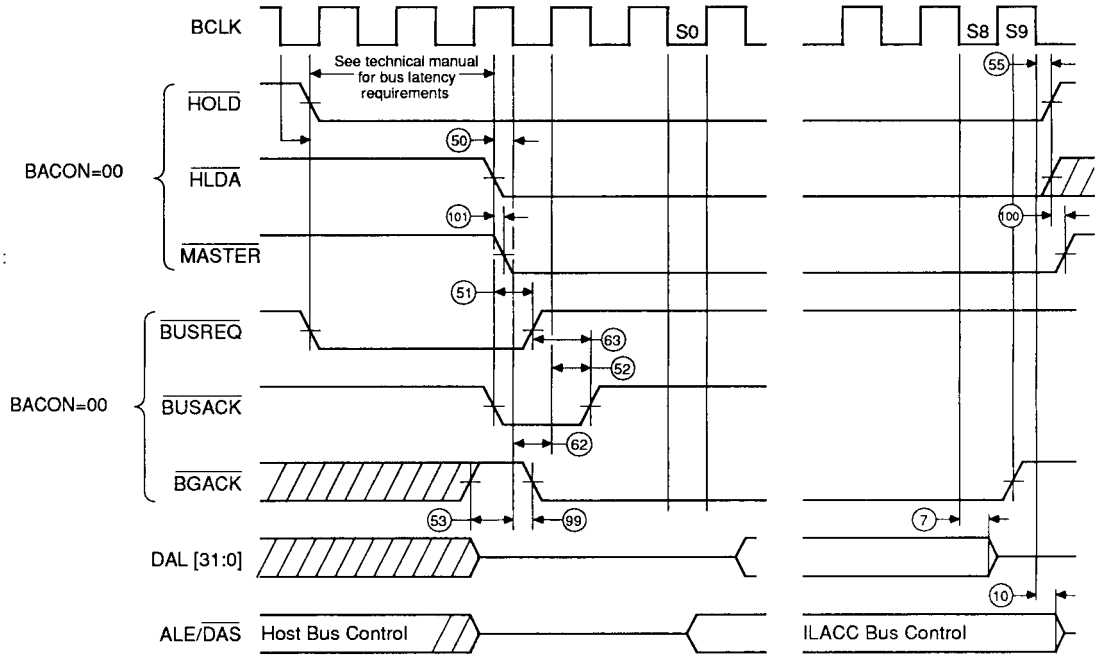


Note 1: R/W sampled on first positive BCLK edge after CS and DAS are asserted.

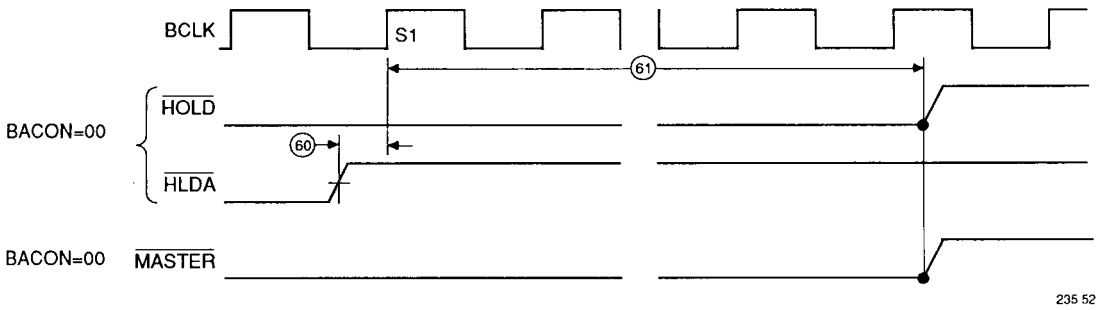
Note 2: Timing refers to assertion of CS.

10594-100A

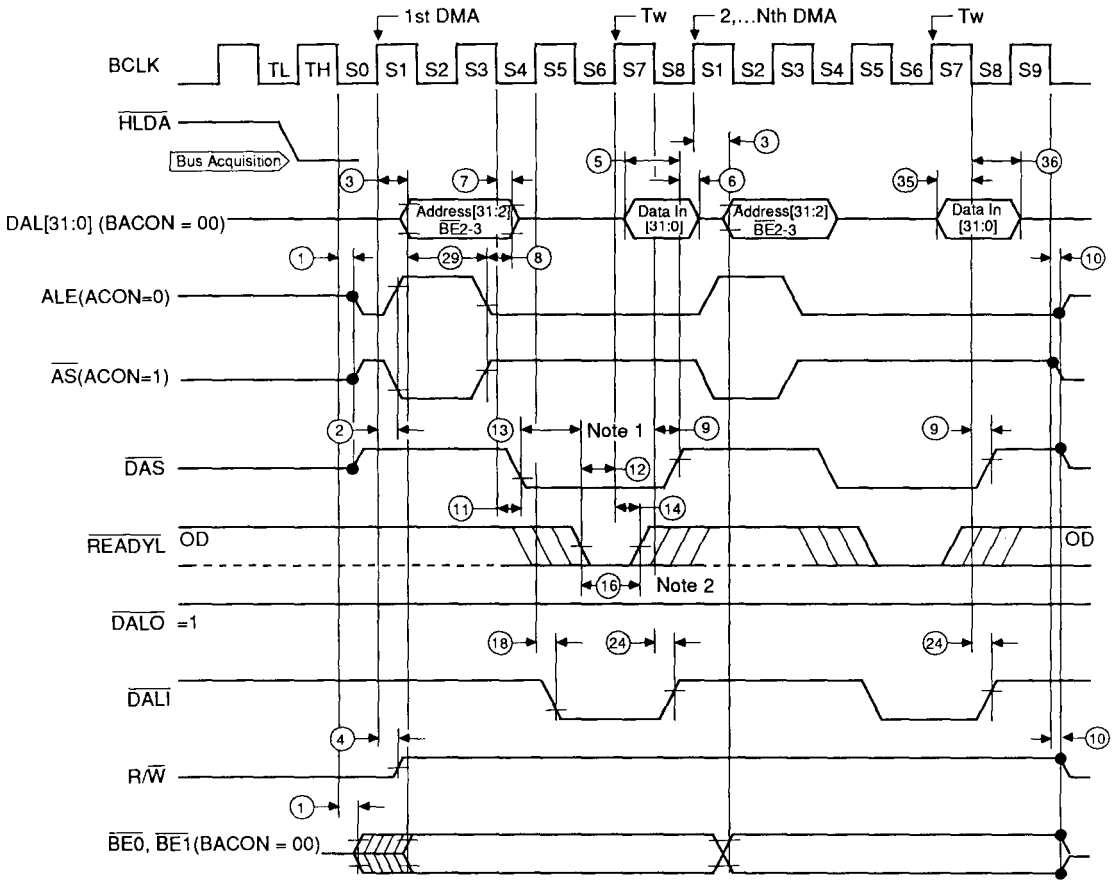
Bus Slave Timing



Bus Acquisition and Relinquish Timing



Bus Pre-emption Timing



Note 1: Timing diagram shows READYL for 0 wait states. For wait states,

$$\min(n_{wait}) = (n_{wait} + 0.5) \cdot T_{BCLK} - (11)_{min}$$

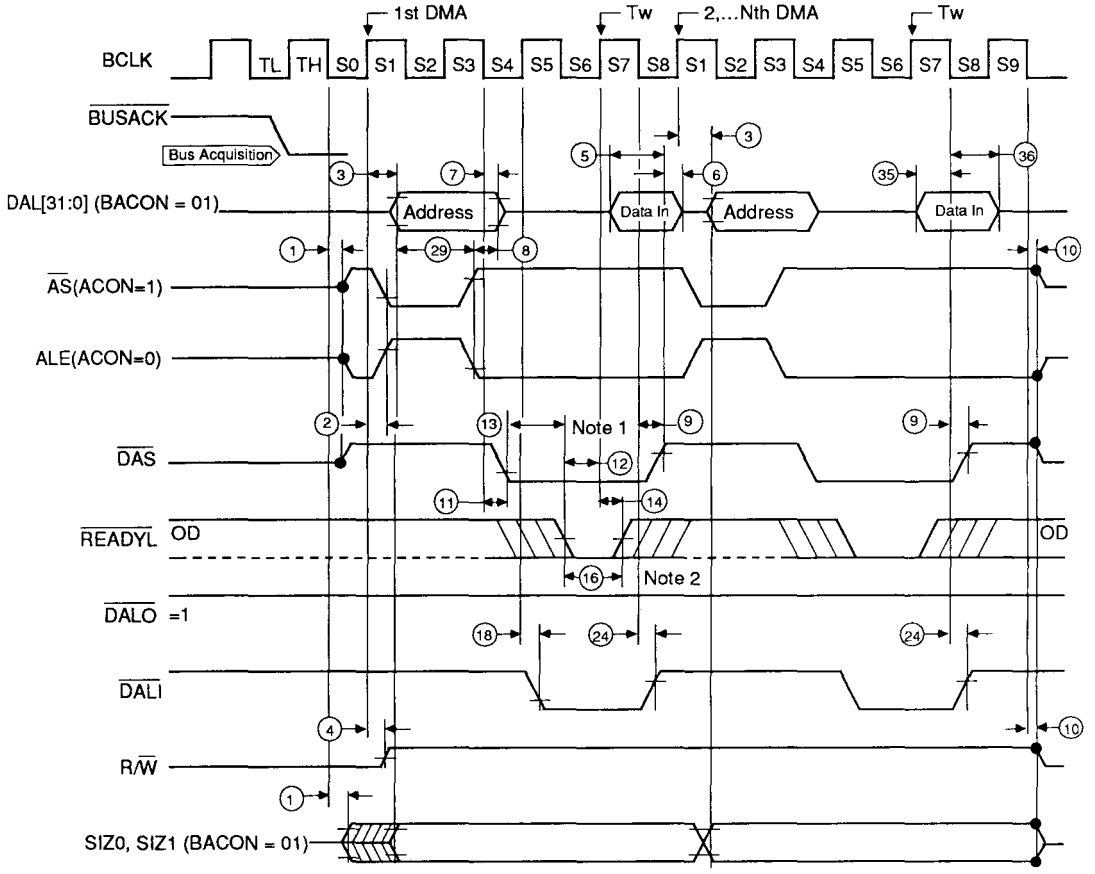
$$\max(n_{wait}) = (n_{wait} + 1.5) \cdot T_{BCLK} - 35\ ns$$

where n_{wait} denotes number of wait states

10594-120A

Note 2: If READYL is not returned high prior to sampling in next DMA cycle, a 0 wait state DMA cycle will occur.

Bus Master Read Timing
(290XX and 680X0)



Note 1: Timing diagram shows READYL for 0 wait states. For wait states,

$\min(n_{wait}) = (n_{wait} + 0.5) \cdot T_{BCLK} - (11)_{min}$

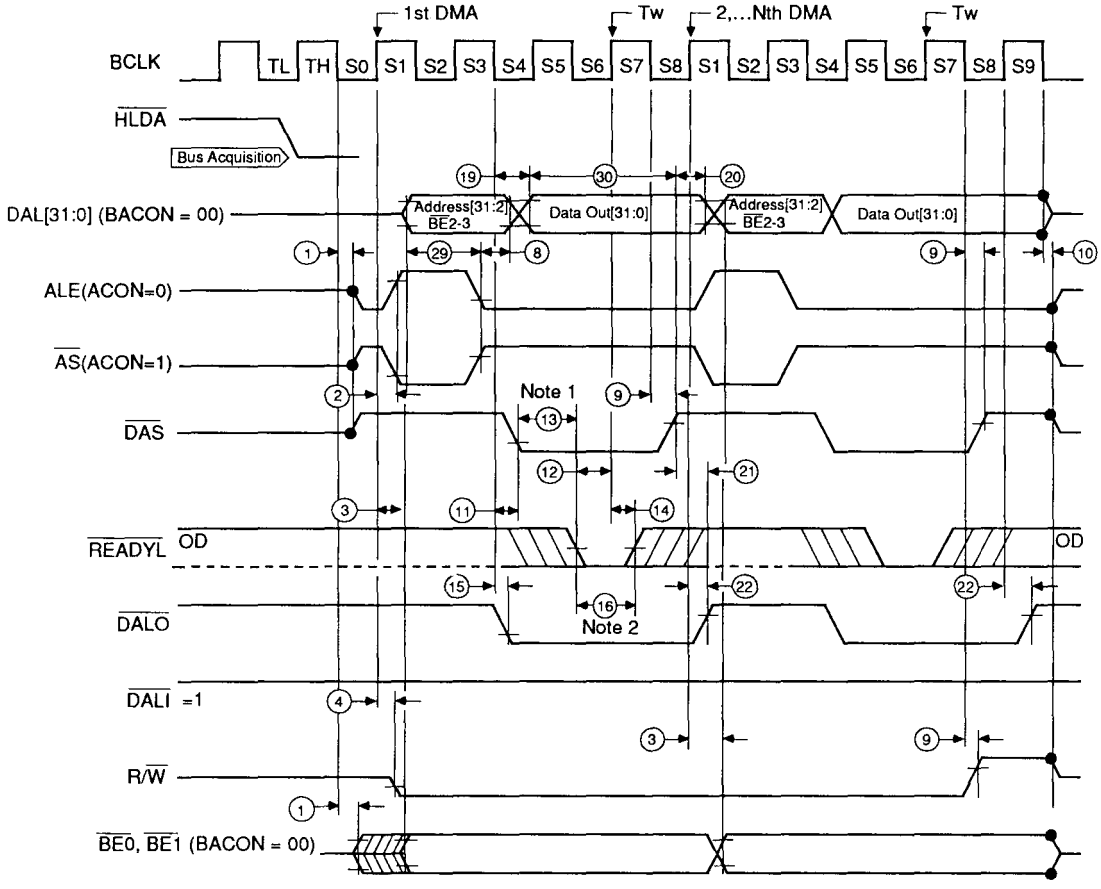
$\max(n_{wait}) = (n_{wait} + 1.5) \cdot T_{BCLK} - 35$ ns

where n_{wait} denotes number of wait states

10594-106A

Note 2: If READYL is not returned high prior to sampling in next DMA cycle, a 0 wait state DMA cycle will occur.

Bus Master Read Timing
(290XX and 680X0)



Note 1: Timing diagram shows READYL for 0 wait states. For wait states,

$\min(n_{wait}) = (n_{wait} + 0.5) \cdot T_{BCLK} - (11)_{min}$

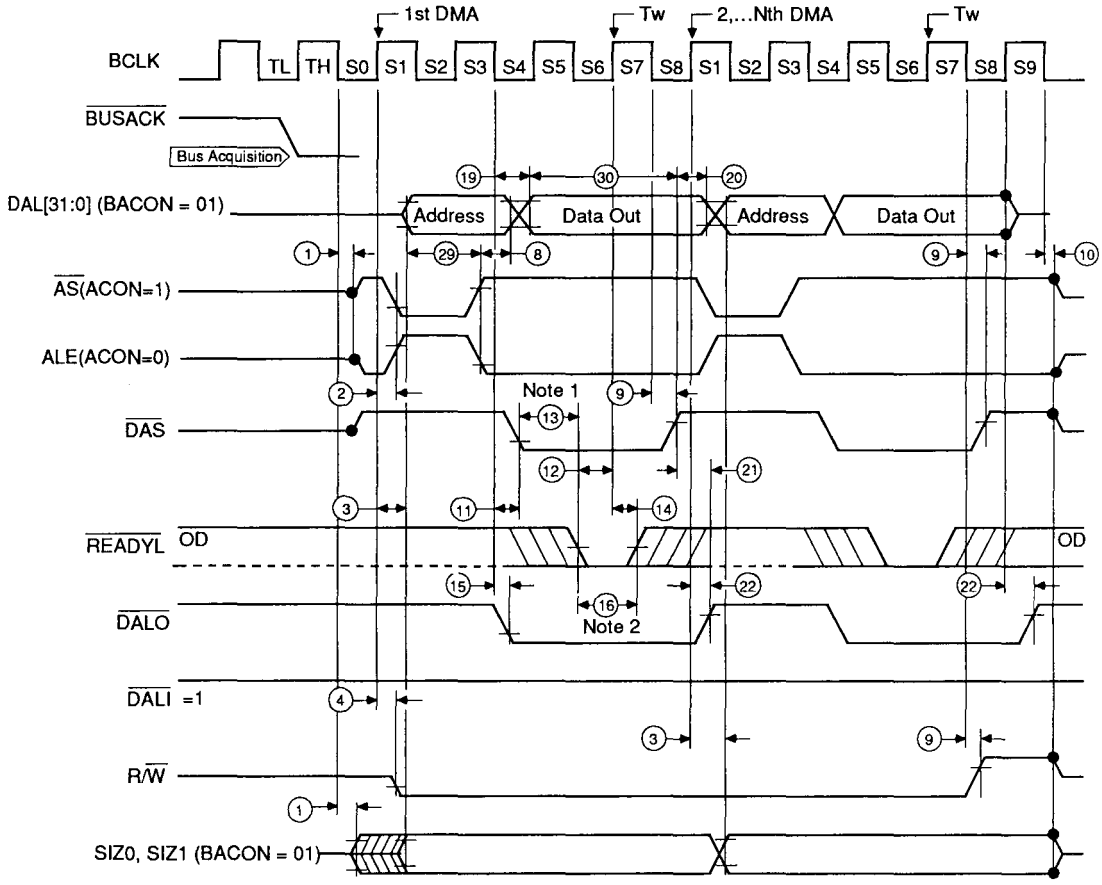
$\max(n_{wait}) = (n_{wait} + 1.5) \cdot T_{BCLK} - 35$ ns

where n_{wait} denotes number of wait states

10594-103A

Note 2: If READYL is not returned high prior to sampling in next DMA cycle, a 0 wait state DMA cycle will occur.

Bus Master Write Timing
(290XX and 680X0)



Note 1: Timing diagram shows READYL for 0 wait states. For wait states,

$\min(n_{wait}) = (n_{wait} + 0.5) \cdot T_{BCLK} - (11)_{min}$

$\max(n_{wait}) = (n_{wait} + 1.5) \cdot T_{BCLK} - 35$ ns

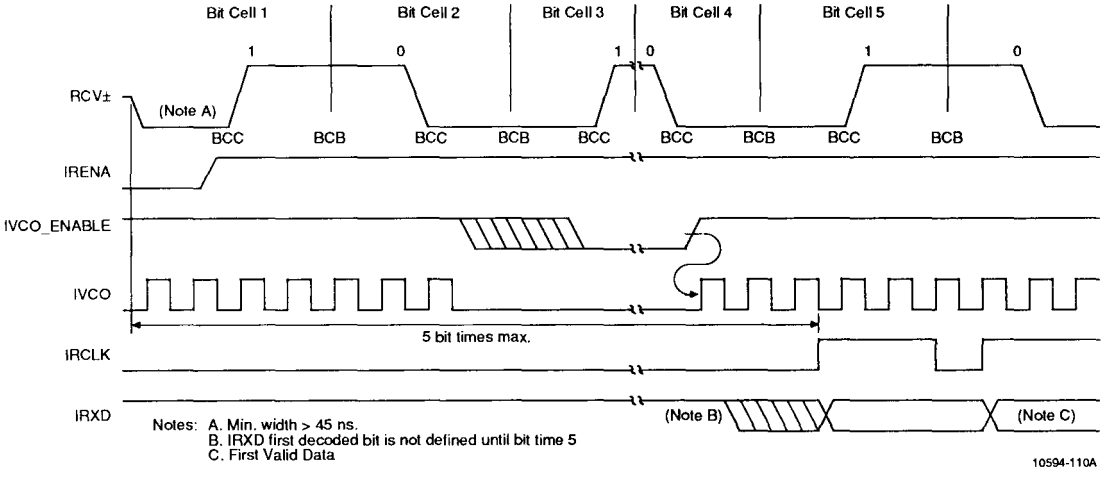
where n_{wait} denotes number of wait states

10594-104A

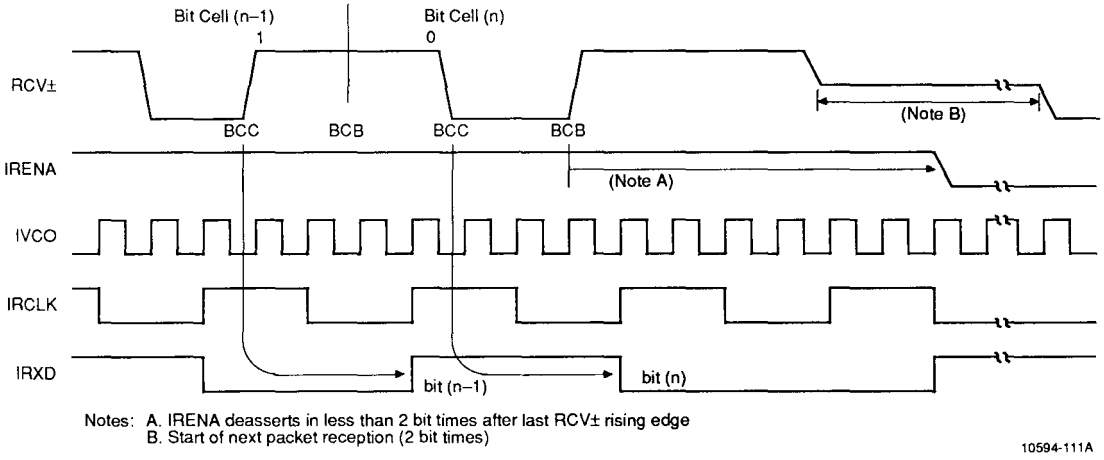
Note 2: If READYL is not returned high prior to sampling in next DMA cycle, a 0 wait state DMA cycle will occur.

Bus Master Write Timing
(290XX and 680X0)

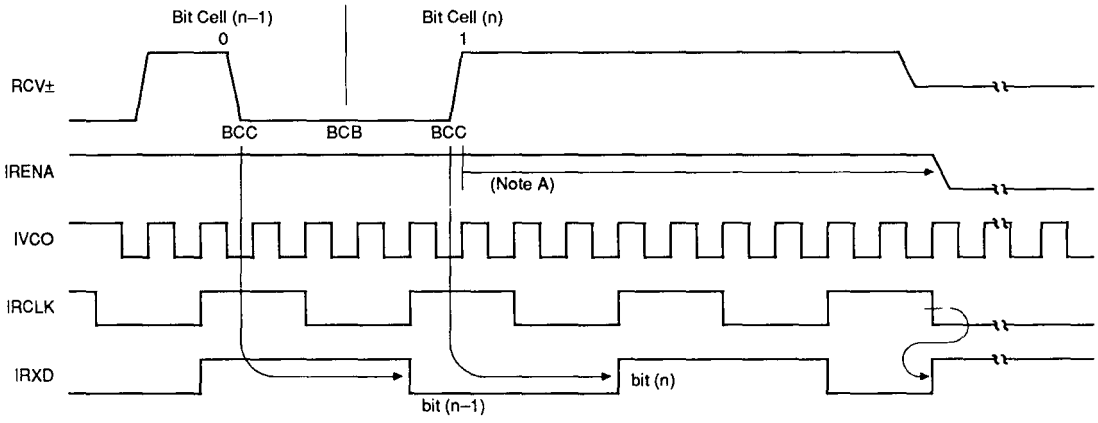
Serial Timing



Serial Receive Timing
Start of Reception & Clock Acquisition



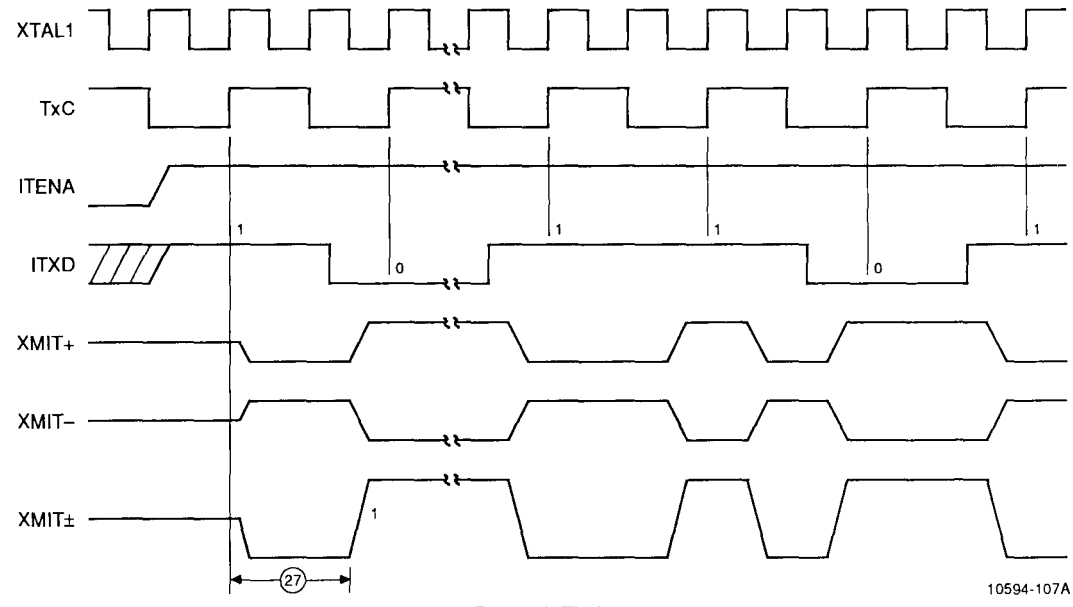
Serial Receive Timing
End of Reception (Last Bit = 0)



Notes: A. IRENA deasserts in less than 2 bit times after last RCV± rising edge

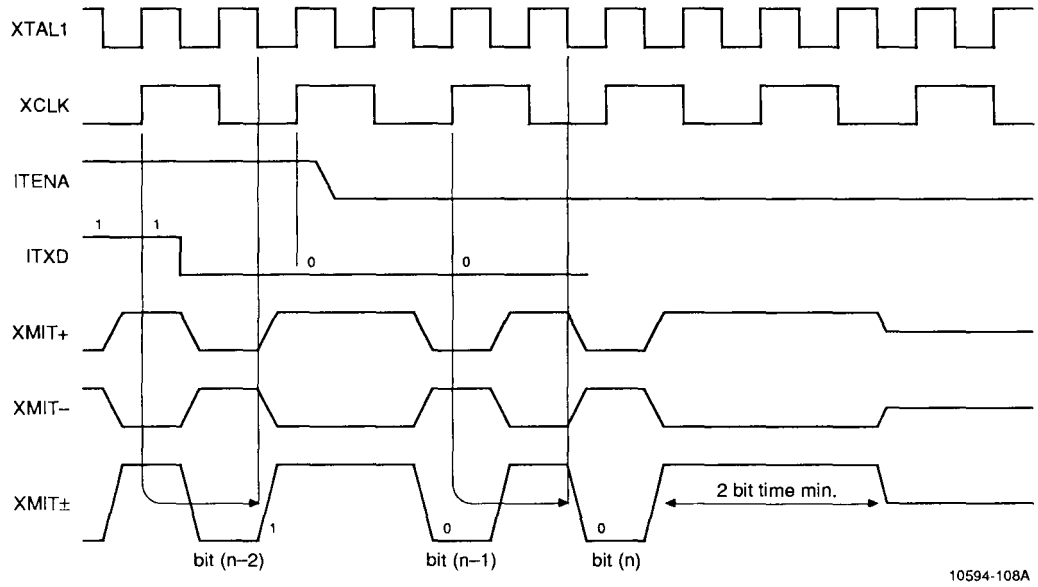
10594-112A

Serial Receive Timing
End of Reception (Last Bit = 1)

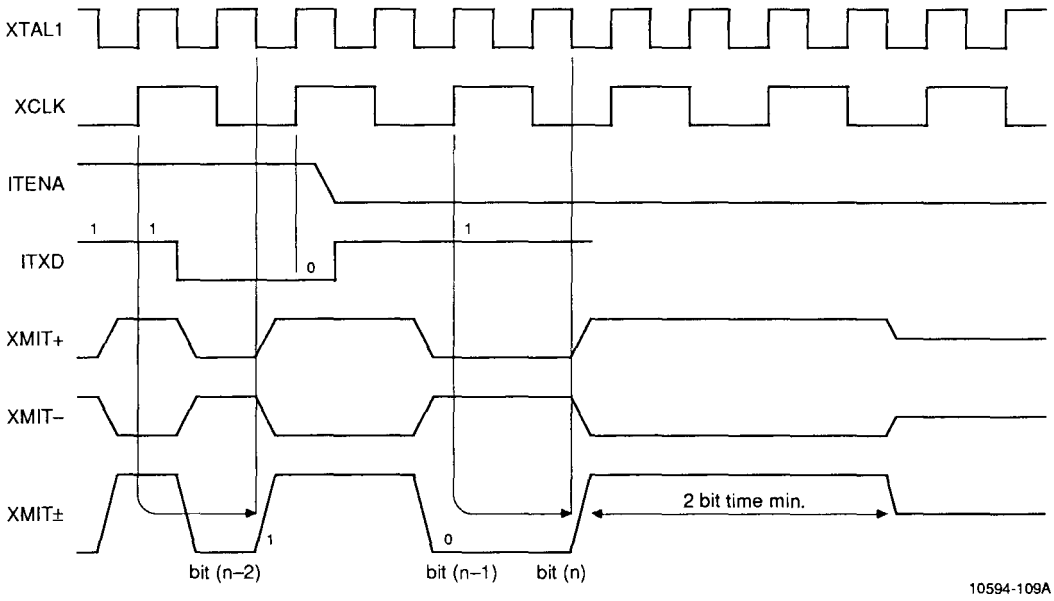


10594-107A

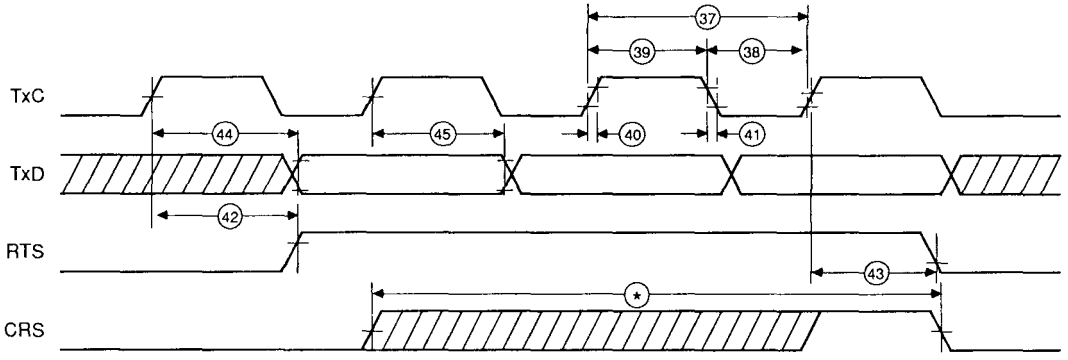
Transmit Timing
Start of Packet



Transmit Timing
End of Packet (Last Bit = 0)



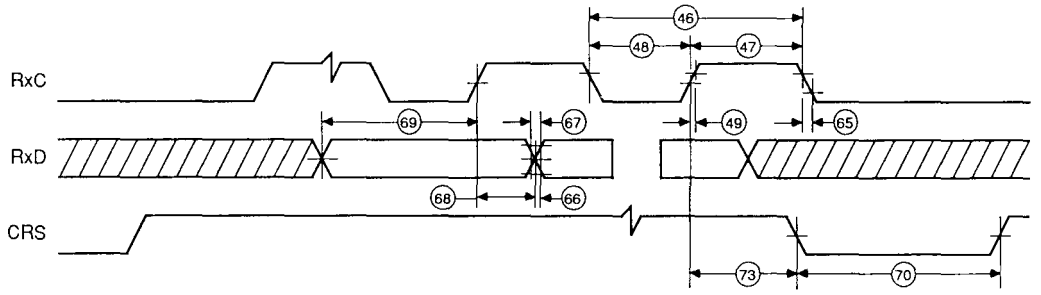
Transmit Timing
End of Packet (Last Bit = 1)



*During transmit, CRS input must be asserted (High) and remain active-high after RTS goes inactive (Low). If CRS is deasserted before RTS is deasserted, LCAR will be reported in TMD2 after the transmission is completed by the ILACC.

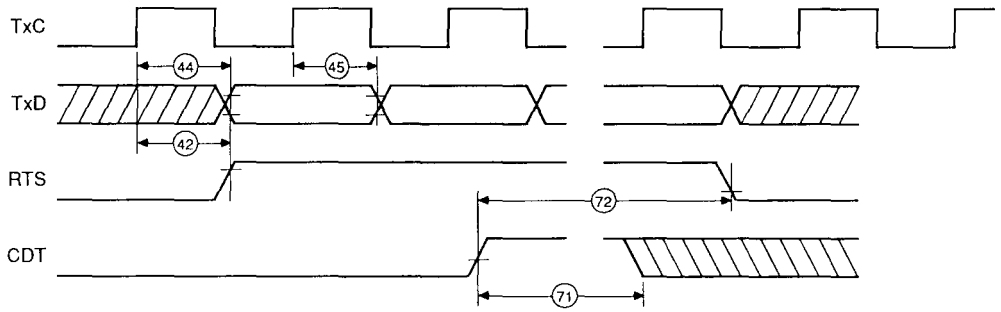
10594-113A

Transmit Timing
General Purpose Serial Interface Port



Receive Timing
General Purpose Serial Interface Port

10594-114A



10594-115A

Transmit Timing During Collision
General Purpose Serial Interface Port

PHYSICAL DIMENSIONS