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analog-digital CONVERSION NOTES

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CONVERSION NOTES

by
The Engineering Staff of
Analog Devices, Inc.

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PREFACE TO THE 1977 SEMINAR EDITION

Analog-Digital Conversion Notes is the first major revision of material previously published in the highly successful *Analog-Digital Conversion Handbook*, first published by Analog Devices, Inc., in 1972 and reprinted in 1976.

This volume contains Parts I and II of that book, updated wherever specific converter products are referred to, in order to reflect the revolution in cost, size and (in some cases) performance brought about by the development of converters in integrated-circuit and hybrid form.

Two entirely new chapters have been added to further reflect changes in the structure of the technological marketplace brought about by the availability of both converters and computers as true components. Chapter II-2 is a consideration of the relationship between processes, configurations, and performance in miniature low-cost converters. Chapter I-4 considers the application of converters with parallel and serial digital interfaces, micro-computers, asynchronous serial data ports, and proprietary integrated data-conversion-subsystem architectures—a natural sequel to the wide-ranging discussion of system considerations in Chapters I-2 and I-3.

As with the earlier volume, it is our hope that this volume will help the purely digital or purely analog designer obtain appropriate practical knowledge of the complementary field and the interface between them, and that it will serve as a useful text and reference source for all designers and users of interface equipment. We will welcome the comments and suggestions of our readers for the benefit of future editions and readers.

March 1, 1977
Norwood, Mass.

D.H. Sheingold

CONTENTS IN BRIEF

Preface to the 1977 Seminar Edition		i
Contents		ii
PART I:	CONVERTERS AT WORK	
Chapter I-1	Data-System Components	1
Chapter I-2	Data Acquisition	7
Chapter I-3	Data Distribution	23
Chapter I-4	Subsystems and Data Communication	31
Chapter I-5	Analog Functions with Digital Components	57
Chapter I-6	Applications of Converter Systems	73
	A. Automatic Testing	
	B. Communications and Signal Analysis	
	C. Displays	
	D. Commerce, Industry, and Elsewhere	
PART II:	CONVERTERS	
Chapter II-1	Understanding Converters	95
Chapter II-2	Converter Microcircuits	127
Chapter II-3	Converter Design Insights	171
Chapter II-4	Testing Converters	191
Chapter II-5	Specifying Converters	217
Chapter II-6	Applying Converters Successfully	237

CONTENTS IN DETAIL

Preface

Contents: In Brief	ii
In Detail	iii

PART I: CONVERTERS AT WORK

Chapter I-1. Data-System Components	1
Sensors; Amplifiers; Common-Mode Problems; Isolation; Function Modules; Multiplexers; Digital Multiplexing; Sample-Hold Circuits; A/D Converters; D/A Converters; Registers; Up-Down Counters; Filters; Comparators; Power Supplies; Digital Panel Meters (and DVM's); Digital Displays; One More Important Element	
Chapter I-2. Data Acquisition	7
Then and Now; Environment and Complexity; Key Factors; Single-Channel Conversion Subsystems; Direct Conversion; Sample-Hold and Conversion; Signal Conditioning; Multi-Channel Conversion; Multiplexing the Outputs of Single-Channel Converters; Multiplexing the Outputs of Sample-Holds; Multiplexing the Inputs of Sample-Holds; Multiplexing Low-Level Data; More than One Tier of Multiplexers; Signal Conditioning; Ratiometric Conversion; Wide Dynamic Ranges; Noise Reduction	
Chapter I-3. Data Distribution	23
Factors Affecting Distribution-System Design; Digital vs. Analog Distribution; Converter-per-Channel Distribution; Simultaneous Updating; Analog Distribution; Acquisition vs. Distribution; Filtering/Smoothing; The Cost Factor; Minimizing Calibration Errors by Servoing; Isolation	
Chapter I-4. Subsystems and Data Communication	31
Subsystems for Interfacing Converters to Analog and Digital Worlds; The AD7550 13-bit converter-on-a-chip; The AD2008 System-Oriented Panel Meter; SERDEX SERIAL Data-EXchange cards; DAS1128 Data-Acquisition Subsystem; RTI-1200 Real-Time Interface; MACSYM ONE, a Compleat System; Interfacing Converters with Microprocessors, Using Parallel Connections; Microprocessor Interfacing, I/O vs. Memory; Interfacing DAS1128 and an 8080; Interfacing AD7550's with μ C's; A Note on Bit-Labeling; Sophisticated Memory-Managed Interfacing with the RTI 1200; Serial Interfacing; V/f Converters; More on SERDEX	
Chapter I-5. Analog Functions with Digital Components	57
Sources; Scale Factors and Modulation; Functional Relationships; Trigonometric Applications; Waveforms; Functions of Time; Digital Servo Devices	

A. Automatic Testing

Uses for Automatic Testing; Ingredients of Test Systems; Converters in Test Systems;

B. Communications and Signal Analysis

Shift-Register Delay Line; Read Out into Memory; Read Out as an Analog Signal; Recirculate; Perform Signal Averaging by Addition; Time Compression by Sampling; Real-Time Correlation; Incremental Delay Line as a Filter; Recursive Filtering

C. Cathode-Ray-Tube Displays

Basic System; Uses of D/A Converters in Displays; Raster Displays; Dot-Matrix Displays; Graphic Displays; Delay-Line Integrator; Vectors and Segments; Differential Linearity and Linearity; Speed and Dynamics

D. Commerce, Industry, and Elsewhere

Automatic Scale Zeroing; Low-Noise Communications; Music-Distribution Systems; Power-Rectifier Monitoring; List of Areas Where A/D and D/A Conversion May Help

PART II: CONVERTERS**Chapter II-1. Understanding Converters**

95

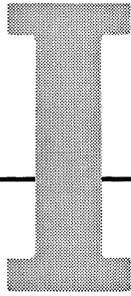
Analog Quantities; Digital Quantities; The Binary Code; Basic Conversion Relationships; Other Codes; Binary-Coded Decimal (BCD); Overranging; 2-4-2-1 BCD; Gray Code; Analog Polarity; Bipolar Codes; Code Conversion; Other Codes; Arbitrary Biasing and Scaling; DAC's as Multipliers and ADC's as Dividers; Ground Rule; Power Supplies; Digital Logic Levels; Control Logic—The Status Output; The Strobe; Analog Signals; D/A Converter Circuits; Resistance Ladders; Switching; References; Bipolar Conversion; Registers on DAC's; A/D Converter Circuits; Successive-Approximations; Integration; Counter Types; Parallel Types

Chapter II-2 Converter Microcircuits

127

Technologies for Converters; Circuit Techniques, Performance, and Applications; The AD7520—A 10-Bit Monolithic CMOS D/A Converter: Early CMOS D/A Conversion; Equivalent Circuit; Applying the AD7520 (Analog Division, Single-Supply Application, Audio-Circuit Applications); The AD7522—A Double-Buffered 10-Bit CMOS Multiplying DAC: Applications; The AD7570—A 10-Bit Successive-Approximations CMOS A/D Converter: Microprocessor Capability; Advantages of CMOS; How the AD7570 Works; Notes on Logic Functions; Applications; AD7550—13-Bit CMOS μ P-Compatible A/D Converter: Microprocessor Compatibility; Applications; How the Quad-Slope Converter Works; The AD562—12-Bit Digital-to-Analog Converter: Circuit Design; Applications; The AD561—High-Accuracy 10-Bit DAC with Built-In Reference: Process Limitations; Buried Reference Diode; Design; Application Features and Circuits; The AD2026 Panel Meter: Design; The I²L Chip; What is I²L? The AD572—12-Bit Successive-Approximation A/D Converter: Design; Theory of Operation; Timing; Digital Output Data; Applications; Conclusion

Chapter II-3. Converter Design Insights	171
<p>Converter Design; Review of D/A Techniques; The Importance of Logic Buffering; Monolithic Components; Component Tolerance; Interquad Divider Reference Loop; Trimming High-Accuracy Converters; Temperature-Variation Effects; Current vs. Voltage Output; Error Budgets; Layout Considerations; Successive-Approximation A/D Converters; The Logic Sequencer; Comparators: The Most Critical Element; Other Considerations in A/D Converter Design</p>	
Chapter II-4. Testing Converters	191
<p>Linearity; D/A Converters; A/D Converters; Gain Calibration; Zero and Gain Calibration; Unipolar DAC; Bipolar DAC Using Offset-Binary or 2's Complement; Temperature Effects; Differential Nonlinearity; Monotonicity; DAC Testing; Dynamic Programming; Bit-Scan Mode; Count Mode, Differential-Linearity Tester; Digital Dither Generator; Settling-Time Measurement; Zero and Full Scale; Comparator Thermal Effects; Alternate Method for Zero and Full-Scale Measurement; Major Carry; ADC Testing; Dynamic Crossplot; Anomalous Errors; Single-Shot Conversion Errors; Semi-Automatic Testing</p>	
Chapter II-5. Specifying Converters	217
<p>Two Basic Factors; Defining the Objectives—Application Checklists; Considerations for D/A Converters; Considerations for A/D Converters; Considerations for Analog Multiplexers and Sample-Holds; Definitions of Specifications; System-Component Selection Process; Typical Converter Classifications; An Example of the Selection and Verification Process; First Approximation; Error Analysis</p>	
Chapter II-6. Applying Converters Successfully	237
<p>Making the Proper System Choices; Data-Acquisition Systems; Three Classes of Converter Specifications; Approaches to Relaxing the Specifications; Logarithmic Compression; Filtering; Sample-Hold; Contributions to Error; Installation and Grounding; Reducing Common-Mode Errors</p>	



Data-System Components

Chapter I-1

This book is basically about A/D and D/A converters: understanding them, applying them, testing them, choosing them, and using them in systems.

When used in systems, they are often accompanied by an impressive panoply of other devices, both analog and digital, to measure input signals and perform intermediate processing with varying degrees of sophistication.

This chapter provides what might be termed a brief biographical “thumbnail” sketch of the main role players. Their general characteristics and aptitudes are summarized, and their roles in further conversion activity are hinted at within the short discussions devoted to each device.

In this book, the reader will quickly find that by far the greater weight of discussion is given to the properties and uses of *analog* circuits and their characteristics in the performance of system functions. The reasons for this lie primarily in the extreme fine-structure and the many degrees of freedom associated with analog circuits. They must labor in the real world, where noise immunity is a function of resolution and signal level, speed is a function of signal level, accuracy is a function of component tolerance and signal level, and the challenges to the designer’s knowledge and ingenuity are many and unrelenting. On the other hand, their basic promise, in favorable environments, is functional simplicity, speed, and overall low cost.

With digital techniques, on the other hand, the principal challenges are to combinational ingenuity, equipment architecture, decreasing the cost and complexity of interconnections, and – in common with analog techniques – anticipating where Murphy’s Law will strike next, and debugging where anticipation has failed. Digital circuits have high noise immunity, no drift, high speed (individually) and low cost (individually), and the rules for using them are few and simple.

With the exception of pre-amplification, a great many of the functions described here in analog form could be performed digitally, after the conversion. That they are not often is (so far) the result of favorable tradeoffs in cost, speed, and complexity. However, reductions in cost of digital integrated circuits and the increase of chip complexity are rapidly making feasible the development of devices that are intended to perform analog functions, but contain digital components. Examples of these include analog function generation with read-only memories (ROM’s) and the universe of arithmetic, logic, and control possibilities with microprocessors.

Figure 1 illustrates the relationships of the principal components of a data system in a “global” perspective. Those to be introduced in this chapter include the following:

- Sensors
- Operational Amplifiers
- Instrumentation Amplifiers
- Isolation Amplifiers

Function Modules
Multiplexers
Sample-Hold Circuits
Analog-to-Digital Converters
Digital-to-Analog Converters
Up-Down Counters
Filters
Power Supplies
Comparators
DPM's
Digital Displays

Rarely will a system use all of the above components; on the other hand, the more-complex systems will often use appreciable quantities of one or another of them. Furthermore, as components shrink in size and cost and become available as integral parts of subsystems with specified performance (and perhaps even a modicum of software), the designer may not even have to think of them as individual components, but rather as sub-blocks in a supplier's diagram (examples may be found in Chapter I-4).

SENSORS

One might imagine that the systems designer has very little say in the choice of sensor, that he accepts whatever data signals exist without protest and gets on with the interface system design without further ado. However, if the systems engineer can have a say in the selection of the original transducer, he can go a long way towards easing his own conversion-design task.

For example, in monitoring or controlling mechanical shafts, the designer may be confronted with signals obtained by three radically-different position-sensing approaches: digital shaft encoders, synchros, and potentiometers, plus variations on all three.

Likewise, temperature measurements may be accomplished with thermocouple and thermistor, while mechanical force may be measured directly by load cells and strain gauges, or obtained indirectly by integrating the output from accelerometers, or even by counting interference fringes in an optical system.

Although it is not our role to recommend any particular type of signal transducer for a particular application, we thoroughly endorse the idea of getting the systems-design engineer into the act before the signal sources are settled upon, instead of later, when it is found that the designer is painted into a corner by the few options allowed.

AMPLIFIERS

If the transducer signals must simply be scaled up from millivolt levels to an A/D converter's typical ± 10 -volt full-scale input, an operational amplifier with appropriate closed-loop gain may be the first choice. Possibly, if the system involves many sources, each transducer can be provided with its own local amplifier so that the low-level signals are amplified before being "shipped" to the data center. Besides scaling, operational amplifiers are used for a host of linear and nonlinear, static and dynamic functions. Specialized amplifiers, such as instrumentation and isolation amplifiers, are always worthy of consideration, because they are frequently the most cost-effective option.

COMMON-MODE PROBLEMS

If analog data must be transmitted over long distances (and often, over quite short distances), differences in ground potential between signal site and data center will add spice to the interface systems design problem. In order to separate common-mode interference from the signal to be recorded or processed, devices designed for the purpose (i.e., instrumentation amplifiers) may be introduced. Typically, an instrumentation amplifier is characterized by good common-mode-rejection capability, high input impedance,

low drift, adjustable gain, and somewhat greater cost than operational amplifiers. They range in form from the monolithic AD521 and hybrid AD522 to potted modules.

ISOLATION

In the event of either very-high common-mode voltage level or the need for extremely-low common-mode leakage current, or both (as might be mandatory for many clinical medical-electronics applications), an *isolation amplifier* is required to interpose a break in the common-mode path from the signal source to the data center. Isolation amplifiers involve optical isolation or transformer-coupled carrier isolation techniques, and (for a given technology) they typically cost about the same as instrumentation amplifiers. Though most-often used for isolating input data from system level, they may also be used for communicating system outputs to devices at other levels.

FUNCTION MODULES

These are special-purpose analog devices and circuits used for a wide variety of signal conditioning operations on signals that are in analog form. Where their accuracy is adequate, they can simply, and at low cost, relieve a processor of an expensive and time-consuming software and computational burden. This category is large and open-ended, but some of the more popular operations performed are multiplication; taking ratios; raising to powers; taking roots; performing special-purpose nonlinear functions such as linearizing transducers; performing rms measurements; computing vector sums; integration and differentiation; current-to-voltage or voltage-to-current transformations, etc. Some of these operations can be purchased in the form of such readily-available devices as multiplier/dividers, log/antilog amplifiers, etc. Others represent but a sampling of the vast potential inherent in operational-amplifier circuitry, available to the designer at low parts cost, and limited only by his ingenuity.

ANALOG MULTIPLEXERS

If data from many independent signal sources must be processed by the same computer or communications channel, a multiplexer is usually introduced to couple the input signals into the A-D converter in some sequence. Additional logic keeps track of which data source is coupled to the converter at any instant.

Multiplexers are also used in reverse. For example, when the converter must distribute analog information to many different channels, the multiplexer, fed by a high-speed output D/A converter, continually refreshes the various output channels with computer-generated information.

DIGITAL MULTIPLEXING

Often, a digital distribution system uses no device that specifically goes under the label of "digital multiplexer." Unlike the comparable process of shunting analog information from computer to many output channels via a single D/A converter, or from many sources to a single A/D converter, the digital multiplexing function is often delegated to the devices being multiplexed, as they share a set of common inputs.

For example, if many digital sources must be multiplexed into a computer or data-transmission channel, they are usually tied to the computer by a common set of parallel "bus" lines.

Commands from the computer then instruct the individual sources which one among them must feed its burden of data into the common bus, thence to the computer. Conversely, if the computer is bent on updating a number of digital output registers (each of which might be connected to a D/A converter), the updating process is accomplished by computer commands that strobe the selected register to accept the data being transmitted over the common output bus lines. Only that register instructed to receive the data can do so; the remaining registers simply ignore the data fed in parallel to their input terminals.

SAMPLE-HOLD CIRCUITS

In many interface systems, the original signal varies quite rapidly, calling for some subtlety in the interface linkage. Because an A/D converter takes a finite time to digitize the input signal, changes in this signal level during the actual conversion process could result in gross errors with some converter types. In any event, the lengthy conversion period would be completed some appreciable time following the conversion command, so that the final digital value would never truly represent the data level prevailing at the instant at which the conversion command was transmitted.

Sample-hold devices are typically introduced into the data link to make a fast "acquisition" of the varying analog signal and "hold" this signal for the duration of the conversion process. Sample-hold circuits are also used in multi-channel distribution installations, where they enable each channel to receive and "hold" its own signal level for activation of different output processes. Usually, a data-acquisition sample-hold circuit must exhibit ultra-fast signal acquisition, with minimal droop for a matter of 1 to 50 microseconds. By contrast, an output data distribution sample-hold circuit can be updated more leisurely, but it is often required to "hold" an analog value for many milliseconds – or even seconds – in the interval between updates.

A/D CONVERTERS

These devices, which may range from monolithic IC's, such as the AD7570, to high performance modules such as the ADC1102, convert analog input data – usually voltage – into its equivalent digital form. Key characteristics of A/D converters may include absolute and relative accuracy, linearity, monotonicity, resolution, conversion speed, stability, and – of course – price. Other aspects open to choice include input ranges, digital output codes, and physical size.

Although the industry tends to converge upon the successive-approximations technique for a very large number of system applications, because of its inherently excellent compromise between speed and accuracy, other popular alternatives include counter-comparator types, and dual-ramp and "quad-slope" approaches. The dual-ramp has been widely used in digital voltmeters. In addition, synchro-to-digital and resolver-to-digital converters are used where data from mechanical shafts must be converted into digital form.

D/A CONVERTERS

These devices "reconstitute" the original data after processing, storage, or even simple transmission from one location to another in digital form. The basic converter consists of an arrangement of weighted resistance values (or divider ratios), each controlled by a particular level or "significance" of digital input data, that develops varying output voltages or currents in accordance with the digital input code.

Although converters have fixed references, for most applications, a special class of D/A converters exists, having a capability of handling variable and even ac reference sources. These devices are termed *multiplying* DAC's, because their output value is the product of the number represented by the digital input code, and the analog reference voltage, which may vary from full scale to zero, and in some cases, even to negative values. In some instances, such as for ac measurements and resolver/synchro conversion, the multiplying converter's weighted divider circuitry is based on tapped transformers, instead of precision resistors, since turns ratios have excellent long-term stability and immunity to temperature effects.

REGISTERS

Digital registers are used to hold information in readiness for passing it along to computers, D/A's, and so forth. For example, a multi-channel interface system using an A/D converter for every input channel would store the digitized values in each converter's output register until called on by the computer to feed the stored value into the common input bus. The converse holds true for output multiplexing, where a number of D/A converters provide different voltage levels for the independent output channels. Each D/A is then fed by a storage register, which "holds" the digital input word until the com-

puter feeds in the new, updating digital value.

Shift registers are used, for example, where the data is transmitted serially over a single pair of wires, instead of as parallel bits over many wires. In this case, the shift register accumulates a serial input word in much the same way that a train and its many carriages (bits) enters a station. When all the bits have entered the shift register, the data bits (passengers) may be read out (detrained) in parallel.

UP-DOWN COUNTERS

These devices, analogous to ramp generators, are quite useful for performing a variety of “tricks” with A/D and D/A converters. Specifically, they are used in forming electronic servo loops for automatic error correcting, offset adjusting, long-termed sample holds, etc.

In electronic servo applications, the up-down counter accumulates pulses representing the variable being controlled, adjusted, or measured, in much the same way that a servo-motor shaft accumulates rotational angle. The counter is often used in conjunction with a D/A converter to develop an analog value proportional to the accumulated count. The process is also used in tracking-A/D converters and resolver/synchro-to-digital converters.

FILTERS

Filters are used on the input side of an A/D converter to remove unwanted components of the input signal. Noise and line-frequency pickup are also attenuated in this way, but at the expense of reduced response to fast input-signal amplitude variations. Filters are also used on the analog output from D/A converters, in order to smooth out the “lumps” created by discrete digital values. Often, the electromechanical device being actuated by a D/A converter (examples include d’Arsonval meters, servo motors, magnet coils, loud-speakers, etc.) acts as a filter in its own right, owing to substantial electrical or mechanical inertia.

In high-speed information-processing systems, “anti-aliasing” low-pass filters are used ahead of A/D and following D/A converters to avoid errors caused by intermodulation of unwanted high-frequency components of the signal (and input noise) with harmonics of the sampling frequency.

COMPARATORS

Conversion systems involve both analog and digital comparators. For example, the A/D conversion process involves balancing the unknown input voltage against some form of internally-produced reference. A comparator responds to the polarity of the inequality between input and reference. More rarely, comparators are used as fast, high-gain (open-loop) amplifiers. Digital comparators, as their name implies, are used on digitized, rather than analog forms of data. For example, a digital comparator might be used in set-point control to provide considerably better accuracy, resolution, and stability, than is possible with an equivalent analog process.

POWER SUPPLIES

Accuracy of interface systems is steadily rising, to the point where 12-bit resolution is quite routine, and 16-bit operation is frequently involved for higher repeatability, resolution, linearity, and accuracy. Consequently, the design of the dc power system is no longer a trivial matter (it never really was!) since errors that remain second-order effects at 8-10 bits become menacing first-order effects at the 16-bit level. In many instances, careful separation of analog and digital grounds is required, demanding, in turn, considerable isolation between the various outputs that modern power supplies provide.

We certainly advocate raising the priority of power-supply engineering from the status of an “afterthought” to that of an item that should be eliminated as a concern early in the design process. Too often, the power supply design (or choice) is left until last, where it is presumed to be able to take up all the slack or tolerances that other design stages create. Instead, at least as much initial attention should be devoted to the power supply as selection of converters, amplifiers, sample-holds, multiplexers, and other devices. A related question is whether to use power supplies and/or regulators in large, medium, or

small "chunks," for major portions of the system, for individual chassis, or perhaps even for mounting on individual boards. The issues involve space, cost, circuit independence vs. excessive lead length and wire size, avoidance of ground loops, allowable local dissipation levels, etc.

If continued operation despite loss of primary power is essential, either from considerations of overall system reliability or because of potential loss of data in volatile memory, the system design should include some arrangement for continuity of supply, for detection when standby power is in use, and for contingency decisions or alarm.

DIGITAL PANEL METERS (and DVM's)

These devices form a kind of self-contained digital processing system all on their own. They can, of course, be used in conjunction with computer or digital recorder, owing to the BCD output that most DPM's provide.

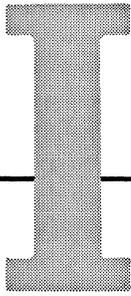
Basically, the DPM may be regarded as an analog-to-digital converter, complete with case, overrange capability, input protection, visual readout, and remote electrical output, usually in BCD format. Thus, the DPM may be used as an A/D converter, complete with visual displays for initial adjustments, in a multi-channel conversion system. Alternatively, it provides a very unambiguous and error-free component for quality-control systems, where human operators use the DPM with high resolution and repeatability in set-point applications for adjusting temperature, pressure, weight, and other industrial variables.

DIGITAL DISPLAYS

Decimal displays are often required in conversion systems for initial setup procedures. Although normal operation of the system involves data rates considerably too fast for the eye to follow, calibration, checkout, and other manual operations nonetheless require a display to be added, often in conjunction with a counter. Thus, manufacturers offer decimal displays in decade increments, and usually with input data compatible with conventional logic levels and prevailing codes.

ONE MORE IMPORTANT ELEMENT

As Figure 1 indicates, there is one additional element that is always present in a data system but seldom shown on a block diagram: *homo sapiens*. These systems are designed, built, programmed, tested, and perfected by humans to serve human purposes; and quite often humans interface with data systems in operation, reading displays and making adjustments—to, and within the system. It is to all these humans that this book is fraternally dedicated.



Data Acquisition

Chapter I-2

Analog data is acquired in digital form for any or all of the following purposes:

Storage

Transmission

Processing

Display

Data may be stored in either raw or processed form; it may be retained for short, medium or long periods. It may be transmitted over long distances (for example, to or from outer space), or short distances (from a lab bench to a minicomputer alongside it). The data may be displayed on a digital panel meter, or as part of a cathode-ray-tube presentation.

Processing can run the gamut from simple comparison to complicated mathematical manipulations. It can be for such purposes as collecting information, converting data to a useful form, using the data for controlling a process, performing repeated calculations to dig out signals buried in noise, generating information for displays, simplifying the jobs of warehouse employees, controlling the color of paint, the thickness of a wrapper, the speed of a subway train.

But it all starts with getting the data in digital form, as rapidly, as accurately, as completely, and as cheaply as necessary.

The basic instrumentality for accomplishing this is the analog/digital converter; it can be a simple shaft digitizer, a DPM with digital outputs, or a sophisticated high-resolution high-speed device. To accommodate the input voltage to the specified conversion relationship, some form of scaling and offsetting may be necessary, performed with an amplifier (/attenuator). To convert analog information from more than one source, either additional converters or a multiplexer may be necessary. To increase the speed with which information may be accurately converted, a sample-hold is desirable. To compress an extra-wide analog signal range, a logarithmic amplifier may be found useful.

The properties of the data-acquisition system depend on both the properties of the analog data itself, and on what is to be done with it.

In this chapter, we shall show some of the configurations that have proven useful and/or popular and discuss some of the considerations involved in the choice of configuration, components, and other elements of the system. Additional information can be found in the chapters on the individual devices.

THEN AND NOW

Two decades ago, A/D converters capable of 0.05% performance and 50,000 sample/second conversion rates, cost about \$8000, consumed about 500 watts, and occupied perhaps one-third of a cubic meter. Today, Analog Devices' AD7570 requires less than 20 microseconds for a 10-bit 0.05% conversion, lists for \$49 in 100's, and is packaged in a 28-pin DIP. And it is designed for easy interfacing with the modern microprocessor.

In the past 20 years, through several "generations" of equipment, data-acquisition hardware has changed radically, thanks primarily to the semiconductor revolution, and prices, have come down to the point where digital, rather than analog, "massaging" of information is a matter of routine, rather than exotic necessity.

What have not changed, however, are the fundamental system problems confronting every digital data-systems designer. Of course, it helps to have small, quiet, low-cost, cool, low-drain components. But (s)he is still up against the laws of Mother Nature, who often seems to prefer to keep her secrets safely obscured by noise, rfi, ground loops, power-line pickup, and transients coupled into signal lines from machinery. Separating the signals from these obscuring effects, then, becomes a matter for ingenuity and imagination, coupled with a great deal of experience; it is not merely a matter of purchasing fast, high-resolution A/D converters. (But having them available at realistic cost provides incentives for giving them useful jobs.)

ENVIRONMENT AND COMPLEXITY

Data-acquisition systems can be separated into at least two basic categories: those suited to favorable environments (electrically quiet laboratories), and those intended for hostile environments (factories, vehicles, military surroundings, and remote installations). The latter group includes industrial process control systems where, for instance, temperature information developed by thermocouples located on tanks, boilers, vats, pipelines, bearings, oil burners, etc., (that are often spread over miles of factory real estate) is fed into a central computer that provides real-time process control. Included are digital control of steel mills, automated production processes, numerically-controlled machine tools. Any or all of these applications may be characterized by the vulnerability of data signals to the phenomena mentioned above and the requirement for almost routine isolation and measurement of off-ground voltages. Also included are *electrically*-noisy environments, such as generating stations, where thermocouples measuring bearing temperatures of rotating machinery are exposed to volts of interference caused by megawatt changes in load; and aircraft control systems, radar stations, etc.

On the other hand, for laboratory-instrument applications, and such test systems as those gathering long-term drift information on arrays of zener diodes undergoing constant-temperature life tests in well-shielded ovens, or gas chromatographs, automatic weighing machines, mass spectrometers, and other sophisticated instruments, the system designer's problems are related more to the performing of sensitive measurements (usually under favorable conditions) than to the gross problems of protecting the integrity of analog data.

Systems existing in hostile environments may require devices capable of wide temperature-range operation, excellent shielding, considerable design effort aimed at eliminating common-mode errors and preserving resolution, conversion at early stages, redundant paths for critical measurements, and (perhaps) considerable processing of the digital data to ensure that it is reliable. Measurements in the laboratory, with narrower temperature ranges and less ambient electrical noise, may be easier to make and communicate, but higher accuracies (or resolutions) may require more-sensitive devices, and a still-considerable degree of effort to preserve appropriate signal/noise ratios.

KEY FACTORS

The choice of configuration and circuit building blocks in data acquisition depends on several critical considerations:

1. Resolution and accuracy
2. Number of analog channels to be monitored
3. Sampling rate per channel
4. Throughput rate
5. Signal-conditioning requirements
6. The cost function

Besides the choice of appropriate component performance levels, careful analysis of the above factors is required to obtain the lowest-cost circuit configuration. Typical configurations include:

1. Single-channel possibilities
 - Direct conversion
 - Preamplification and direct conversion
 - Sample-hold and conversion
 - Preamplification, sample-hold, and conversion
 - Preamplification, signal-conditioning, and any of the above
2. Multi-channel possibilities
 - Multiplexing the outputs of single-channel converters on a processor bus
 - Multiplexing the outputs of sample-holds
 - Multiplexing the inputs of sample-holds
 - Multiplexing low-level data
 - More than 1 tier of multiplexers

Some of the more-interesting signal-conditioning options include

1. Ratiometric conversion
2. Wide-dynamic-range options
 - High-resolution conversion
 - Range biasing
 - Automatic gain switching
 - Logarithmic compression
3. Noise-reduction options
 - Filtering
 - Integrating converters
 - Digital processing

Finally, in evaluating tradeoffs, there are at least three types of “budgets” that should be considered: cost budget, system time budget, and error budget.

SINGLE-CHANNEL CONVERSION SUBSYSTEMS

Direct Conversion

Figure 1 represents the simplest digitizing system, a lone A/D converter, performing repetitive conversions at a free-running internally-determined rate. It has power inputs and an analog signal input. Its outputs are a digital code word, including “over-range” indication, (in parallel or byte-serial form), polarity information (if necessary), plus a “status” output, to indicate when the output digits are valid.

Perhaps the most well-known converter of this kind is the digital panel meter, which consists of a basic A/D converter and a numerical display. For many applications, the sole purpose of digitizing is to obtain the numerical display, i.e., to use the DPM as a meter, rather than as a system component.

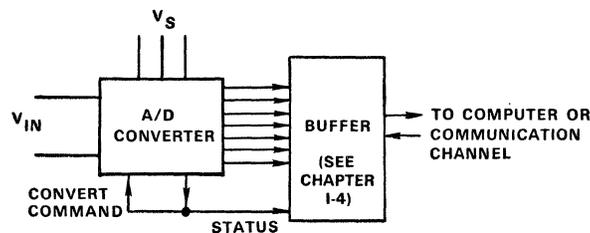


Figure 1. Simplest data-acquisition system configuration.

The DPM, however, is not necessarily the best way to digitize a single channel. Its two major shortcomings are: it is slow, and its BCD digital coding must be changed to binary if its output is to be processed by binary equipment. When free-running, its output is strobed into an available interface register when the data is valid, rather than by an interface command.

Converters designed for system applications (including many DPM's, such as the AD2008) can usually receive external commands to convert or hold. For dc and low-frequency signals, the converter is usually a dual-slope type, which has the advantage that it is inherently a low-pass filter, capable of averaging out high-frequency noise, and nulling frequencies harmonically-related to its integrating period. (For this reason, the integrating period is usually made equal to the period of the line frequency, since the major portion of system interference usually occurs at that frequency and its harmonics.)

If the converter is responding to individually-important samples of the input, the maximum rate of change of the average input for full resolution, and the conversion rate, have the following relationship (binary conversion):

$$\left. \frac{dV}{dt} \right|_{\max} = 2^{-n} V_{FS} / T_{\text{CONVERT}}$$

For example, if $V_{FS} = 10V$, $n = 11$ (1/2048 resolution) and $T_{\text{convert}} = 0.1s$, the maximum rate of change of input is about 1/20 V/s. At faster rates of change, 1 LSB changes cannot be resolved within the sampling period.

If, on the other hand, individual samples are not important, but large numbers of samples are to be dealt with, essentially delineating a stationary process, the only requirement is that the signal be sampled at least twice per cycle of the highest frequency of interest. For this purpose, in the example given above, the maximum signal frequency that can be handled is 5Hz.

So far, the context has been that of the dual-slope integrating A/D converter, which spends about 1/3 of its sampling period performing an integration, and the remainder of the time counting out the average-value-over-the-integrating-period as a digital number, and resetting to initial conditions for the next sample. It should be noted that the dual-slope type will always read out the average value, which results in a valid sample of the input waveform over the integrating "window."

Though it is slow, an integrating A/D converter, such as the quad-slope AD7550, is quite useful for measurements of temperature, battery discharge, and other slowly-varying voltages, especially in the presence of noise.

However, by far the most popular type of converter for system work is the successive-approximations device (described amply in Part II), since it is capable of high resolution (e.g., 16 bits), high speed (e.g., 1 μ s for 10-bit conversion), and quite reasonable cost. In the above example, if T_{convert} , using a successive-approximation converter, is 10 μ s, the maximum allowable dV/dt for maintenance of bit-at-a-time resolution becomes 500V/s, an improvement, but far from sensational.

The successive-approximation converter has the weakness that at higher rates of change, it generates substantial linearity errors, because it cannot tolerate change during the weighting process. The converted value lies somewhere between its values at the beginning and the end of conversion; but the time uncertainty approaches the magnitude of the conversion interval. Figure 2 illustrates this point. Finally, even if the signal is slow enough, noise rates-of-change (perhaps introduced by the signal itself) that are excessively large will cause erroneous readings that cannot be averaged, by either analog or digital means. An external sample-hold can greatly improve matters, as will be shown.

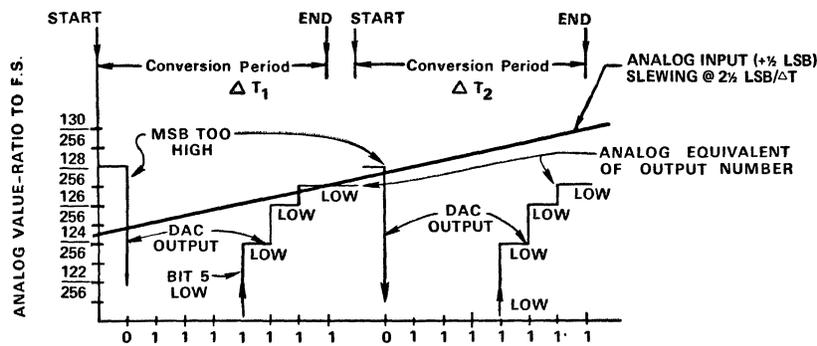


Figure 2. Successive-approximations converter error with fast-changing input ($2\frac{1}{2}$ LSB per conversion interval). Note that output reading of $127/256$ FS is the same for both intervals, though one starts at $124/256$ and the other ends at $129/256$. Error increases with ramp speed.

Direct conversion, especially near the signal source, is most useful if the data must be transmitted through a noisy environment. This can be seen, even in the case of an 8-bit converter ($1/256$ resolution) and a high-level 10V signal, if one considers that bits will be lost if the peak-to-peak noise level induced in the analog signal is greater than 40mV (approximately $10V/256$); the standard TTL digital noise immunity, on the other hand, is 1.2V (or $2.0 - 0.8V$), a gain in signal-to-noise of better than 10:1.

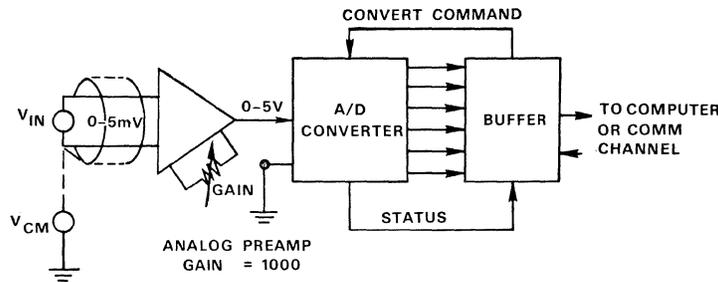


Figure 3. A/D Converter with preamplifier.

Preamplification and Direct Conversion (Figure 3)

Converters designed for OEM system applications are, in most cases* “single-ended” in reference to signal ground, and have normalized analog input ranges of the order of 5 or 10 volts, single-ended or bipolar. It makes sense to scale signal inputs up or down to the standard converter input level, to make fullest-possible use of the converter’s available resolution.

If the signals are of reasonable magnitude (already preamplified or outputs of an analog computer), and already exist within the system, the scaling may be simply accomplished with operational amplifiers in a single-ended or differential configuration. If the signals are from outside the system, or are quite small, or have an appreciable common-mode component, a differential instrumentation amplifier may be profitable used, with characteristics depending on the gain required, the signal level, the needed CMR, bandwidth, impedance levels, and cost tradeoffs.

Finally, if the input signals must be galvanically isolated from the system, a light- or transformer-coupled isolation amplifier must be used to break all conductive signal paths. This kind of isolation is essential in some medical-instrument applications. It is also useful where large common-mode spikes are encountered, for industrial applications requiring *intrinsic safety*, and for all applications in which the signal source is at a high off-ground potential.

*Extremely-high-resolution converters, such as the ADC-16Q, have a high-CMR differential front end. DVM’s, and some DPM’s, also tend to have differential inputs, in consonance with their low full-scale-input levels (e.g., 0.1999V).

Sample-Hold and Conversion (Figure 4)

A successive-approximations converter can be made to operate at considerably-greater accuracies at high speeds, overcoming the weaknesses mentioned above, by introducing a sample-hold at its input. Between conversions, the sample-hold acquires the input signal, and, just before conversion takes place, it is placed in *hold*, where it remains throughout the conversion. It can be seen that, if the S/H responds instantaneously and accurately, the converter can convert changes (from the preceding sample) of any magnitude accurately, at speeds up to the conversion rate. In practical sample-holds, however, there will be acquisition time, tracking delay, and aperture time; typical values of these quantities are $2\mu\text{s}$ to 0.01% , a fraction of a μs , and 25ns , with $2\text{-}3\text{ns}$ uncertainty. If the aperture time and tracking delay compensate one another, or are unimportant as long as they are consistent, the principal source of time error is the aperture *uncertainty*. The relation between aperture uncertainty and maximum rate of change for maintaining resolution in an n -bit system is

$$\left. \frac{dV}{dt} \right|_{\text{max}} = 2^{-n} V_{\text{FS}} / t_{\text{apu}}$$

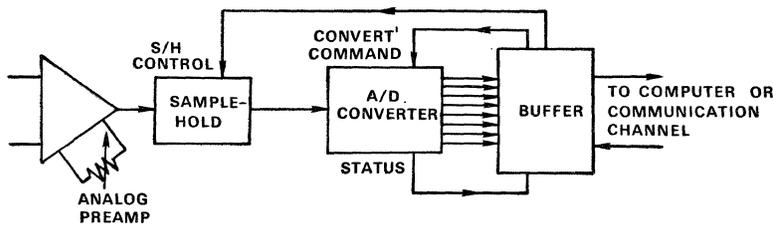
for the example given, ($f_{\text{sample}} = 100\text{kHz}$, $V_{\text{FS}} = 10\text{V}$, $t_{\text{apu}} = 3\text{ns}$)

$$\left. \frac{dV}{dt} \right|_{\text{max}} = 5\text{mV} / 3\text{ns} = 1.67\text{V} / \mu\text{s}$$

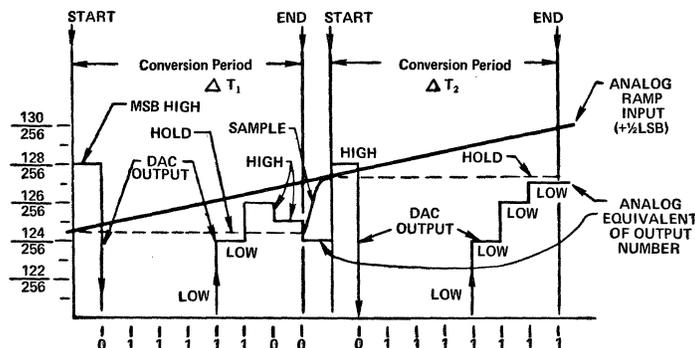
This number is also limited by the *slew rate* specification of the sample-hold.

Figure 4b shows, in contrast with Figure 2, that the successive-approximations converter, with a constant input applied by the S/H, will deliver an accurate digital representation of the beginning input at the end of each conversion interval. Any errors that are functions of time will be due to errors of the sample-hold, including the acquisition errors above, plus droop during the conversion interval, and any linearity, offset, and transient errors. Noise present on the signal, though sampled and converted, may be susceptible to digital averaging by the processor.

Since sample-holds usually operate at unity gain, with errors referred to full-scale (which should be the same as the converter's full scale range), scaling or preamplification should occur before the signal is applied to the sample-hold.



4a. Sample-Hold in single-channel data acquisition.



4b. Successive-approximations converter example of Figure 2, preceded by sample-hold. Digital output is within $\frac{1}{2}\text{LSB}$ of analog input at start of conversion, $124/256$, and $127/256$.

Sample-and-hold devices can be used with other types of converters, to establish precise timing of the signals being sampled, independently of the time required by a given device to complete a conversion. Their utility is especially evident if the conversion time is variable, as in counter types.

Signal Conditioning (Figure 5)

This is a blanket term that includes a wide variety of possibilities. Scaling of input gains to match the input signal to the converter's full-scale range is a simple, obvious example. One might also include dc offset to bias odd ranges, such as 2.5 to 7 volts, to levels more compatible with standard converters. Preamplification, as discussed earlier, is a typical example. Linearizing of data from thermocouples and bridges can be performed by analog techniques, using either piece wise-linear approximations (generated by biased diodes) or smooth series-approximations using low-cost I.C. multipliers; it could be done digitally, after conversion with a microprocessor or by using a ROM to store the inverse function.

Analog differentiation could be used to measure the rate at which the input varies; integration could be used to obtain total dosage from a rate of flow. Either could be used to produce a 90° phase shift; an op amp could be used to provide an arbitrary phase shift. Sums and differences can be used to reduce the number of data inputs (analog data reduction).

Analog multipliers could be used to compute power by squaring voltage or current signals, or by multiplying them together. Analog dividers of various types could be used to compute ratios or the logarithms of ratios, or square roots. Devices that compute $Y(Z/X)^m$ can take ratios over wide dynamic ranges, and perform ideal-gas computations.

Comparators can be used to make decisions based on analog levels (e.g., to convert only when an input exceeds a threshold or is within a "window.") Op amps and diodes may be used to perform simple "ideal diode" functions.

A/d – what seems almost like getting "something for nothing" – logarithmic modules can be used for range compression to permit the conversion of signals having resolutions of 10^6 with 12-bit converters. (This will be discussed later in the chapter.)

Active filters are essential elements to minimize the effects of noise, carriers, and unwanted high-frequency components of the input signal. Their growth of use, and the increase of interest in their design are reflected in the large number of magazine articles and the preponderance of filter discussions in such publications as the *IEEE Transactions on Circuit Theory*, plus a growing number of books on both analog and digital filtering.

One could go on and on, but the basic point should have been made: That in system design, all data-processing need not be digital (with all due respect to the great potential inherent in the use of microprocessors). Analog circuits can perform processing or data reduction effectively, reliably, and economically, and should be considered as alternative ways of reducing numbers of transmission channels, software complexity, noise, and – more often than not – cost.

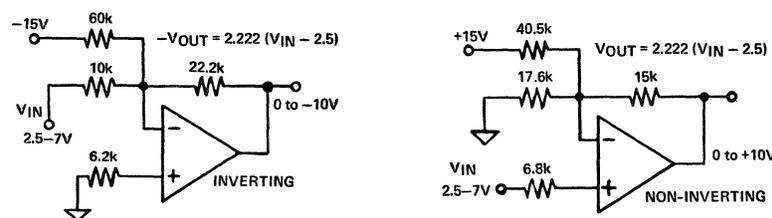


Figure 5a. Op amps used for offset and scaling.

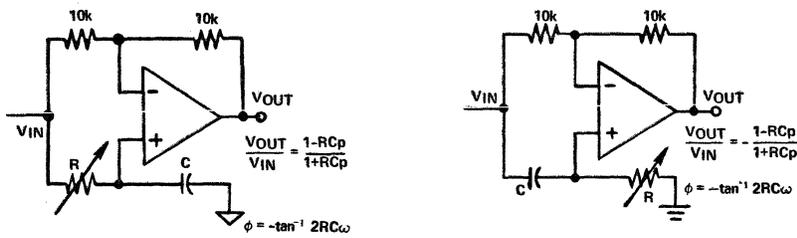


Figure 5b. Op amp to generate arbitrary phase shift, Gain = 1, all-pass.

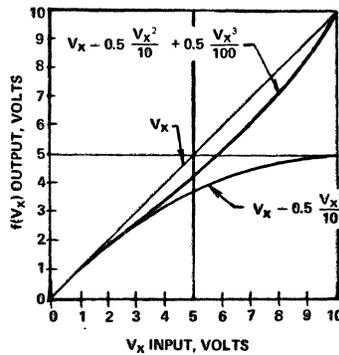
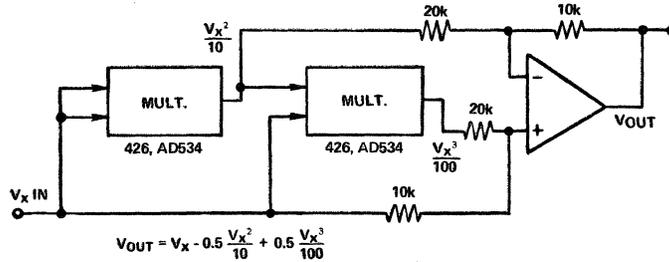


Figure 5c. Using multipliers for nonlinear functional relationships (such as linearization).

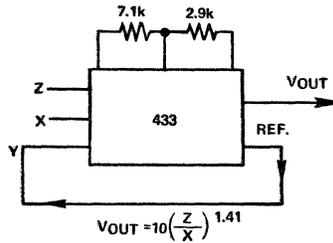


Figure 5d. Ratio of two voltages raised to arbitrary non-integral power.

MULTI-CHANNEL CONVERSION

In multi-channel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system. Large systems may combine several different kinds of multiplexing, as well as cascaded tiers of the same kind.

Multiplexing the Outputs of Single-Channel Converters

Although the conventional way to digitize data from many analog channels is to introduce the time-sharing process, whereby the input of a single A/D converter is multiplexed in sequence among the various analog sources, an alternative parallel conversion approach is becoming increasingly practicable. Cost of A/D converters has dropped radi-

cally during the past decade, and it is now possible to assemble a multi-channel conversion system, with the seeming extravagance of one converter for every analog source, just as economically as the conventional analog multiplexed system. (Figure 6.)

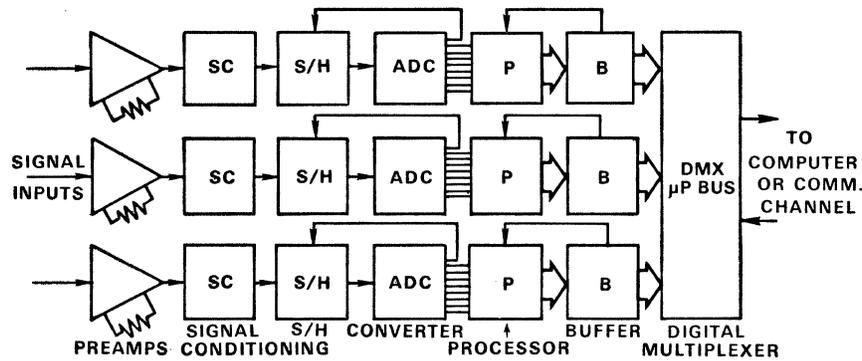


Figure 6a. Basic multi-channel conversion scheme, using digital multiplexing before transmission.

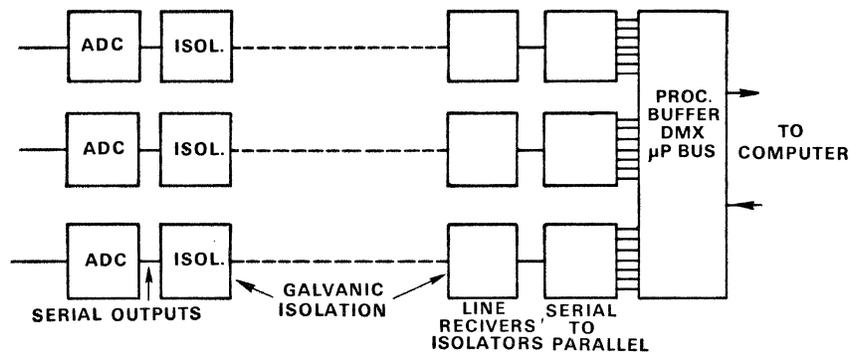


Figure 6b. Multi-channel conversion using remote A/D converters.

There are a number of important advantages to this parallel conversion approach, which, by the way, is virtually standard practice for resolver/synchro conversions beyond about the 10-bit accuracy level. First of all, quite obviously, slower converters may be used to obtain a given digital throughput rate; alternatively, the converter-per-channel may run at top speed, providing a much greater flow of data into the digital interface. For a constant data rate, however, with more channels (and fewer conversions per channel), the reduced conversion speed, plus the fact that each converter is looking at continuously-changing data, rather than jumping from one level to another, may allow the sample-holds to be eliminated, at a cost saving. Fewer conversions also mean that a slower converter might be used, generally resulting in even further cost saving, especially since some channels may not require a great deal of resolution.

The parallel-conversion approach provides a further advantage when applied to industrial data-acquisition systems, where many strain gages, thermocouples, thermistors, etc., are strung out over a large geographical area. In essence, by digitizing the analog signals right at their source and transmitting serial digital data, rather than the original analog signals, back to the data center, a considerably immunity to line-frequency (50-60-400Hz) pickup and ground-loop interference is achieved. Among other factors, the digital signals can be transformer or optically coupled, for example, to gain complete electrical (hence ground loop) isolation. Also low-impedance-digital drive and receiving circuits drastically prune vulnerability to noise.

Not least, among the subtle benefits of digitizing sensor signals at their source, is the ability to perform logical operations on the digitized data before it is fed into the computer. In this way, for example, main-frame involvement with data is streamlined and redundancies are minimized. More-specifically, logic circuits can arrange to access data from slowly-

varying thermocouple sensors less frequently, while reading-in data from critical sources at enhanced speed. In fact, the versatility of a digital subsystem may be exploited to make its own decision as to when a particular data channel should be fed into the computer: if certain signal sources remain constant or within a narrow range for long periods, then change rapidly later in the process, it is possible to ignore these data until the changes occur. (A local microcomputer can store the stationary values and make the decisions).

In summary, a great deal of flexibility and versatility is gained by transferring the interface process from analog multiplexing to digital multiplexing. Logic decision circuits can exercise judgement on when and what data to feed the computer, and, in general, can give the overall interface a much larger measure of autonomy than is possible with an entirely-analog conversion system. (The computer cannot make decisions about the data submitted by an analog multiplexing system until it has received the data upon which to base its judgements...this means that the data have been interfaced before the computer can decide that that particular piece of information is redundant. And there is no guarantee that it will be redundant on the next pass.)

Finally, it should be noted that if the data is being transmitted from a lunar vehicle to Earth, the channel is quite crowded, and the sort of *redundancy-reduction data compression* described above is absolutely essential to make sure that the items of data that get through are those having the highest priorities, by virtue of containing intelligence rather than redundant information.*

For each channel of the digitally-multiplexed system, there could be the array described earlier: preamplifier, signal-conditioning, sample/hold, converter. It is also possible that for one or more of the channels, there are a number of sequentially-multiplexed sub-channels, especially if they are carrying similar information.

Multiplexing the Outputs of Sample-Holds

Working back from the interface (with a minimum number of shared elements) towards the more-conventional situation in which the number of shared elements is maximized, we consider the case of a shared A/D converter, with a multiplexer at its input, switching among the outputs of a number of sample-holds (Figure 7). This configuration is found where sample holds are updated rapidly, even simultaneously, then read out in some sequence. It is generally a high-speed system, in which all items of data delineating the state of the system must do so for the same given instant. Multiplexing may be done

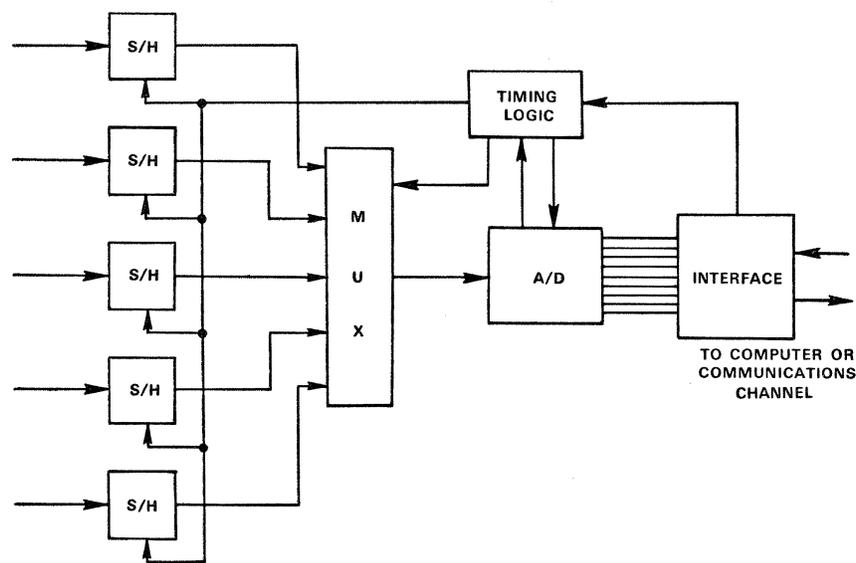


Figure 7. Multiplexed simultaneous sample system.

*"New approaches to Data-Acquisition System Design," by T. O. Anderson, *Analog Dialogue*, Vol. 5, No. 1, January, 1971.

sequentially, or by random addressing. For this kind of operation, the former is more typical. The sample-holds must have sufficient freedom from droop to avoid accumulating excessive error while awaiting readout, which period may be considerably longer than in the case of the converter-per-channel. Increased throughput rate could be obtained by using additional converters, with fewer multiplex switch points and faster update rate.

Applications that might require this approach include wind-tunnel measurements, seismographic experimentation, or in testing complex radar or fire-control systems. Often, the event is a one-shot phenomenon, and the information is required at a critical point during the one-shot event. . .such as, for example, when a supersonic air blast hits the scale model.

Multiplexing the Inputs of Sample-Holds

The next step towards increased sharing is to share the sample-hold as well as the A/D converter. Figure 8 shows the typical system embodying this idea. For most-efficient use of time, the multiplexer is seeking the next channel to be converted, while the sample-hold, in *hold*, is having its output converted. When conversion is complete, the *status* line from the converter causes the S/H to return to *sample* and acquire the next channel. Then, after the acquisition time is completed, either immediately, or upon command, the sample-hold is switched to *hold*, a conversion begins, and the multiplex switch moves on.

This system is slower overall than the previous example, and, since the channels may tend to be diverse rather than identical, the multiplexer could equally well be switching sequentially or in a random-access mode. For some systems, a manual mode, for check-out, may also be desired. In the random-access mode, it is quite possible that some channels (those with more "intelligence", i.e., change/time), will be accessed more frequently).

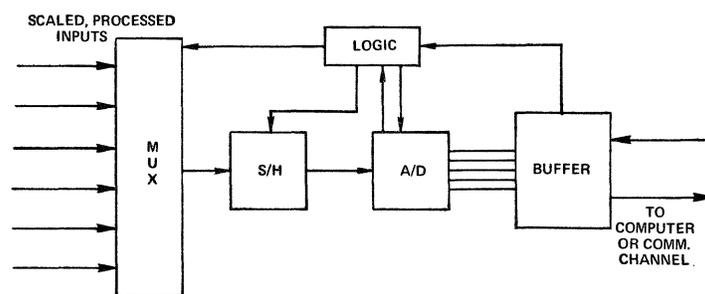


Figure 8. Multi-channel analog multiplexed interface.

Multiplexing Low-Level Data (Figure 9)

The idea here is that, in addition to sharing of the converter and the sample-hold, expensive instrumentation-amplifier capacity must also be conserved. The decreasing cost of instrumentation amplifiers (in fact, of amplifiers of all types), plus the disadvantages of low low speed and the engineering effort involved in ensuring the successful transmission and multiplexing of low-level data, are likely to result in decreasing use of this system approach. Some of the considerations are discussed in the chapter on Multiplexing.*

Low-level multiplexing is often involved with the use of programmable-gain amplifiers, or the even-more-sophisticated automatic range-switching preamps, which combine the use of converters having modest resolution with range-switching controlled from the interface to obtain additional significant bits. (For example, a 12-bit converter, and 32 steps of adjustable gain, can provide 17-bit resolution, assuming — big *if* — that the resolution is actually present in the signal and that the system is capable of handling it without degradation.)

All the difficulties that are inherent in single-channel low-level circuitry are compounded by the addition of low-level multiplexing of n such channels. Not only is guarding necessary, but individual channels should be individually guarded. And, following the principle

*Analog-Digital Conversion Handbook, Analog Devices, Inc., 1976, \$3.95.

that the guard should be present right up to the input of the preamplifier, the guard too must be switched (or else driven from the common-mode level as measured separately at the amplifier*). Not only must the problem of pickup be considered, but the new dimension of crosstalk is added. And not only signal-to-signal crosstalk (not a great problem with small differential signals), but also common-mode-to-signal. Not only must input capacitance be balanced, but it must be balanced in the context of a multiplex switch having at least two circuits.

The saving grace (though perhaps not for some) is that systems of this sort are slow, and a large capacitor across each pair of input leads can reduce capacitive unbalance and high-frequency noise, without slowing-down the system excessively.

The usual low-level problems of thermal unbalance at connectors, lead junctions, and switches (and don't forget kovar-to-copper at IC's), must also be dealt with. All such unavoidable thermocouples should have thermal symmetry.

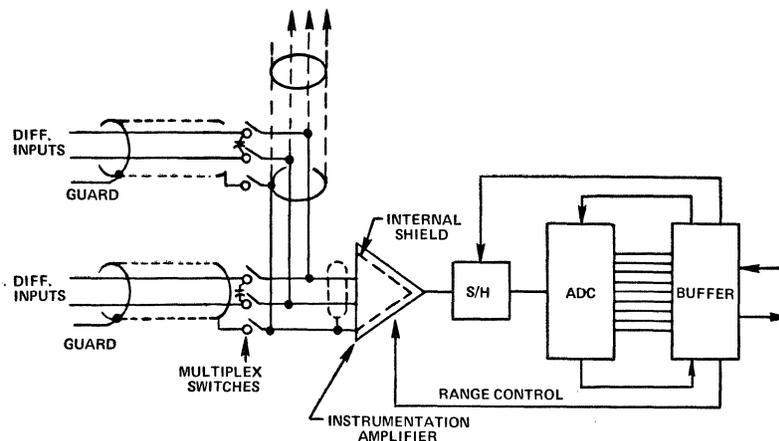


Figure 9. Low-level multiplexing.

More than One Tier of Multiplexers

If there are 64 channels to be multiplexed, the problems of stray capacitance (including capacitive unbalance) are worsened by the parasitic capacitance of the *off* channels on the conducting channel: if there are n channels, the capacitance will be $(n - 1) C_{DGO}$ plus the usual stray wiring capacitance. It is practical to reduce this capacitance by using two tiers of multiplexer. In the above example, with 8 channels per switch, the capacitance is reduced to $14C_{DGO}$ from $63C_{DGO}$.

SIGNAL CONDITIONING

Discussed here are a few topics that keep coming up in connection with data-acquisition systems.

Ratiometric Conversion

Some A/D converters have a *ratiometric*, or "external reference" connection, allowing the output digital number to represent the ratio of the input to an arbitrary (within specified limits) reference input. In effect, the device becomes an analog divider with digital readout.

Devices of this sort are useful in making precision measurements that ignore variation of a device reference. For example, Figure 10 shows how a potentiometer ratio can be measured, independently of variations of the applied voltage, by applying the same voltage to the reference input of the converter.

*The extra switch points can be eliminated by passively summing the voltages at the amplifier inputs, via high-impedance buffers, with two equal resistors, $CMV = \frac{1}{2}(e_1 + e_2)$, and buffering with a simple follower.

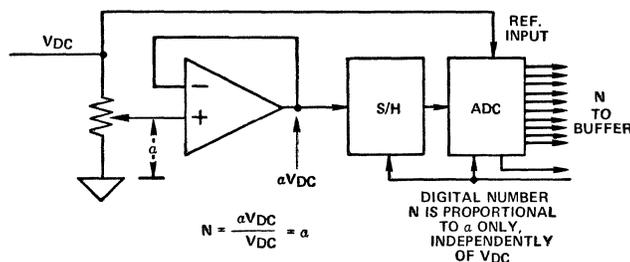


Figure 10. Measuring a potentiometer ratio, independently of the applied voltage, a ratiometric measurement. If the sensor is a bridge, the amplifier could be an instrumentation type instead of a follower.

In a multiplexed system, where measurements may be taken from a number of similar devices, such as strain-gage bridges, the common bridge supply may be used as the converter's reference to eliminate normal-mode gain error caused by supply-voltage variation.

Wide Dynamic Ranges

The need for wide-dynamic-range signal conditioning in a single channel may occur in two basic ways: Either it is necessary to resolve a voltage anywhere in the range to a high degree of accuracy, relative to full scale, (for example in the measurement of position in a follow-up system); or it is sufficient to measure a quantity having a wide range of variation to modest accuracy, relative to actual value (for example, to within 1%, over a 10,000:1 range).

For signals in the first category, a high resolution-and-linearity converter (such as the ADC-16Q) is the simplest answer. Another possibility is the use of a moderate-resolution converter (e.g., 12-bit resolution), preceded by an amplifier with switched gain (Figure 11) controlled from the digital interface. In one form of operation, a trial conversion is performed at the lowest gain; if the MSB is 0, the gain is doubled and another conversion is performed; if the MSB is still 0, the gain is doubled again, etc., until either the MSB is turned on or the top end of the range is reached. Each doubling represents an additional bit of resolution. This scheme may be programmed with the RTI1200 interface (Chapter I-4), for up to 15 bits of resolution (but not accuracy).

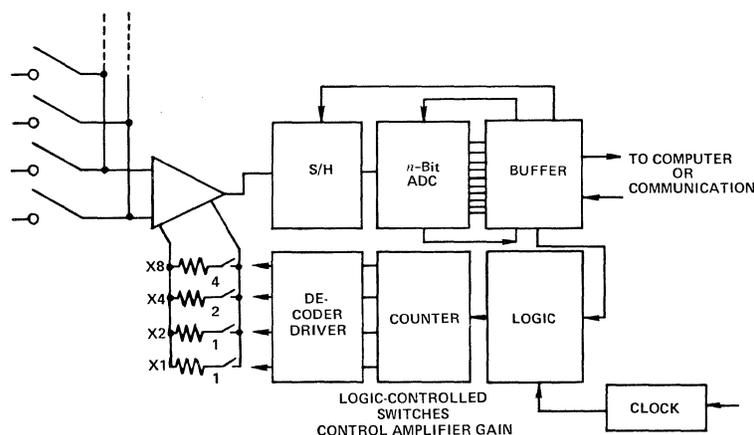


Figure 11. Switched-gain amplifier.

Yet another possibility, when seeking accurate measurements of small variations about a fixed value of voltage, is to sum a voltage equal to the nominal fixed value (and opposite in polarity) and measure the differences. If the voltage is applied (Figure 12) via a high-resolution DAC, the interface can keep track, digitally, of both the initial value and the difference voltage, using an ADC of quite modest performance. (The tradeoff here is the cost of a high-resolution DAC, such as the DAC-1138, plus logic and a modest 8-, 10- or 12-bit ADC, vs. a 16-bit ADC.)

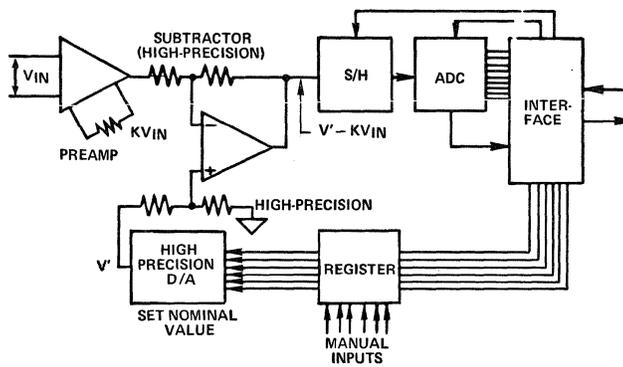


Figure 12. Use of high-resolution DAC to measure small deviations about a precisely-determined value.

In any of these schemes, it is essential to keep in mind that every element in the front end, wiring, preamplifiers, components, references, must be compatible with the resolution and accuracy sought. This also includes the noise level.

For signals in the second category, the switched-gain amplifier is a satisfactory, but slow-and-expensive approach. An intriguing alternative is to use a logarithmic amplifier for for data compression (Figure 13).

The error of a logarithmic amplifier, after calibration, is a *log conformity* error (nonlinearity on a semi-log plot) that is specified in terms of a maximum value at the output, or a maximum ratio to actual input over a specified range. For example, 1% log conformity error means that the error at the output, for 2V/decade* scaling, is 8.6mV, corresponding to an input uncertainty of $\pm 1\%$. Typical input *voltage* range (i.e., for the Analog Devices 755) is 1mV to 10V. The corresponding output-voltage range is $\pm 4V$ (i.e., ± 2 decades at 2 volts per decade, with respect to a 0.1V reference level.) Since an error of 1% referred to the 1mV minimum input signal is $1/10^6$ of full-scale input, and since the corresponding output error of 8.6mV is $0.0086/8 = 1.075 \times 10^{-3}$ of the output swing, the dynamic range of the signal has been compressed by a factor of 1000, as a result of the logarithmic transformation. This means that a 12-bit converter (with suitable scaling) can be used to digitize the log amplifier output, with a quite-comfortable error margin.

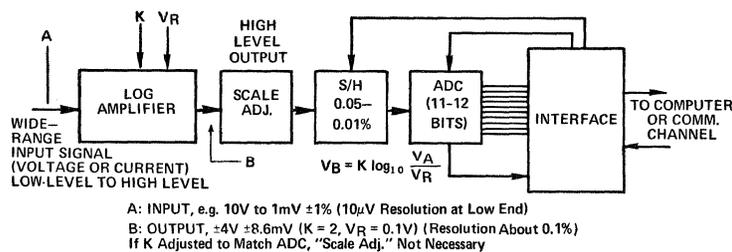


Figure 13. Low amplifier used for range compression in data-acquisition system.

Though it might appear that the representation of data having an inherent 20 bits of resolution ($10^6 \cong 2^{20}$) by a signal having 12-bit resolution is getting "something for nothing," in violation of *some* Natural Law, the scheme really works. There are, however, some points to consider:

1. Compression is achieved by exponentially distorting the relative value of the Least Significant Bit. Thus, for a 10,000-to-1 signal range, represented by $\pm 4V$ output, an LSB (of 12 bits, offset binary, suitably scaled) is worth 23mV at 10V input (i.e., $10 [1 - \log_{10}^{-1} 8/8192]$) and $2.3\mu V$ for 1mV input. Therefore, while the approach is quite useful for compressing data requiring essentially constant *fractional* error (e.g., 1%) anywhere in a

*A decade is a 10:1 range of input voltage or current.

wide range, it is not at all suited to applications requiring high resolution (e.g., 0.01% FS) at any point in the range.

2. Since the digital number is a logarithmic representation of the analog input signal, it must be dealt with as such in the digital process. If the number is to be used in computation, it should be antilogged, using a ROM and/or processor computing capacity, unless of course the computation is facilitated by the availability of a logarithmic relationship. If the data is simply to be stored or transmitted, and eventually returned to analog form unchanged, it does not require any further digital transformation, just an analog antilog operation following the output D/A conversion (unless logarithmic analog data is acceptable).

3. Since a logarithmic function is inherently unipolar (the logarithm is real only for positive values of the argument – positive signals require a 755N, negative signals a 755P), it is far from ideal for signals that are inherently zero-centered. While it may be useful to bias some types of input signals into a single polarity, functions that demand symmetrical treatment may be badly distorted by the wide variation, in both resolution and speed, between zero and full-scale input. Such functions would profit by a type of compression that is symmetrical about zero. An example of an easily-obtained form is a \sinh^{-1} function (Figure 14), which involves two complementary antilog transconductors (752P and 752N) in the feedback path of an op amp. The resulting function is logarithmic for larger values of input, but it passes through zero, essentially linearly (but slowly).

Noise Reduction

Like diseases, noise is never eliminated, just prevented, cured, or endured, depending on its seriousness and the costs/difficulty of treating it.

Noise in data-acquisition systems takes three basic forms, *transmitted noise*, inherent in the original signal, *inherent noise*, generated within the devices used in data acquisition (preamps, converters, etc.) and *induced noise*, “picked up” from the outside world, power supplies, logic, or other analog channels, by magnetic, electrostatic, or galvanic coupling.

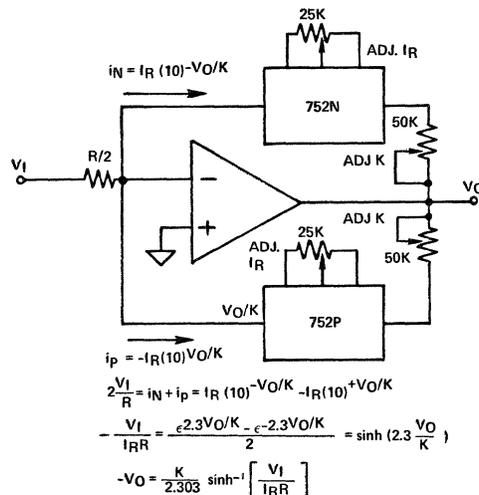
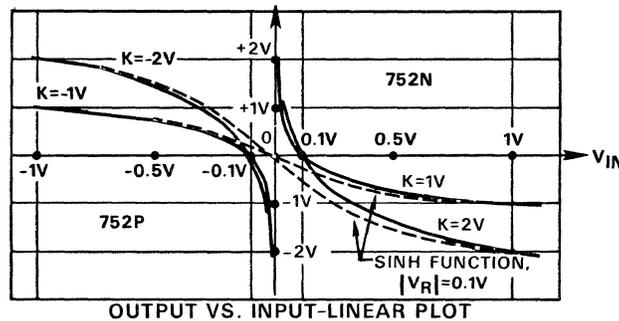


Figure 14. Bipolar signal compression using complementary logarithmic transconductors to synthesize \sinh^{-1} function.

Noise is either *random* or *coherent* (i.e., correlated to some noise-inducing phenomenon within or outside of the system). Random noise is usually generated within components, such as resistors, semiconductor junctions, or transformer cores, while coherent noise is either locally-generated by processes, such as modulation/demodulation (e.g., chopper-stabilization), or coupled-in. Coherent noise often takes the form of “spikes,” although it may be of any shape, including – collectively from many sources – pseudorandom.

Noise is characterized in terms of either *root-mean-square (rms)* or *peak-to-peak* measurements, within a stated bandwidth.* Random noise from a given source, within a given bandwidth, will give consistent *rms* measurements. For a typical gaussian amplitude distribution, and a sufficient number of measurements, one may expect a consistent relationship between the probabilities of obtaining peaks of given size in relation to the rms, as shown in the Tables in Figure 15.

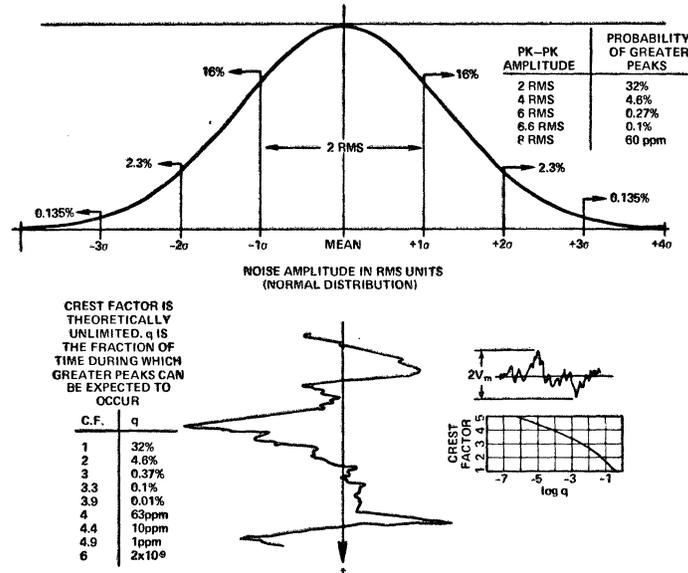


Figure 15. RMS vs. peak-to-peak amplitudes for gaussian noise.

RMS values of noise from uncorrelated sources (e.g., from different devices, or from different portions of the frequency spectrum of the same device) add as the square-root of the sum-of-the-squares. However, if noise is dominated by picked-up spikes, root-sum-of-squares is of small comfort.

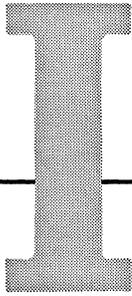
As we have indicated at the beginning of the chapter, there are two basic forms of system-design problem: those involving essentially ordinary signal levels in unfavorable environments, and those involving extremely high-resolution measurements in favorable environments.

For unfavorable environments, where the major source of noise is *induced noise*, the designer must rely on early preamplification and conversion, isolation, shielding and guarding, signal compression and filtering, and – where possible – an information rate (via fast sampling or parallel paths) that has enough redundancy to allow the digital processor to retrieve data via correlation and summation.

In favorable environments, where the measurement process and the processing hardware introduce the major portion of the uncertainty, the emphasis must be placed on measurement techniques, filtering, choice of data-acquisition hardware for best resolution, and – again – the use of high-speed digital processing for signal retrieval, including drift compensation and scale-factor adjustment.

Where noise is likely to have large spikes as a major component, the integrating-type converter (dual-slope) usually provides additional filtering. For random noise, if there are sufficient samples taken of a given signal channel, the statistical properties of the noise are imparted to the digital output, which may be filtered by digital techniques.

*For a useful discussion of the properties of noise, see “Noise and Operational Amplifier Circuits,” in *Analog Dialogue*, Vol. 3, No. 1.



Data Distribution

Chapter I-3

After analog data have been converted to digital form and have been duly stored, transmitted, or processed, the results of this handling, as well as some newly-created digital numbers, may be required once again in the “real world” of phenomena. In analog or digital form, they may be used to drive meters or motors, display information, stimulate devices under test, generate heat or light, modulate waveforms, sound the alarm, or – in short – they are converted from abstract numbers to the manipulation of energy.

The multiplexed digital output words are made available in serial order at an output register, for distribution to their destinations. Though an increasing number of real-world functions, such as numerical displays, stepping motors, printers, and the like, are effected by digital numbers (perhaps with “decoding,” but without the interposition of electronic analog variables), there is still a widespread – and growing – use of electronic D/A converters in distribution systems. This chapter treats of those systems that use D/A converters.

FACTORS AFFECTING DISTRIBUTION-SYSTEM DESIGN

The configuration, choice of components and their specifications, the system timing, and location of multiplexing, depend, as with data acquisition, on

1. Number of channels
2. Settling time per channel
3. Update rate
4. Output resolution
5. Output linearity and accuracy
6. The nature of the loads
7. The cost function

There are a number of areas for decision by the system designer:

Digital signal readout: Serial paths or parallel paths? Serial words or parallel words?

Signal storage between updates: in digital or analog form? Registers or sample-holds? Single-rank or dual-rank? Sample-holds or inertia?

Multiplexing: Digital or analog? If digital, parallel or serial? If analog, with sample/holds or multiplex switching?

Update: Simultaneous, sequential, or random?

Conversion: At computer or at load? Single converter with analog multiplexing, or many converters with digital multiplexing?

Analog output: Voltage or current? Discrete values or smoothed? Permissible level of switching transients? Isolated or galvanically-connected circuitry?

Techniques to reduce costs: Combining sample-hold and multiplexing. Inertial filtering. Using low-precision DAC's in “slave” circuit for standardized calibration.

The systems designer has a choice between feeding data to analog actuating and indicating devices via either a D/A converter (with storage register) for each channel (Figure 1), or a single D/A converter, with a sample-hold circuit for each channel (Figure 2).

Once updated, a D/A converter-with-input-register will store an analog value indefinitely, or at least, for so long as the power is connected. By contrast, a sample-hold circuit, since it holds the analog data on a capacitor, is susceptible to a definite "droop" (positive or negative) in the analog output as the charge on the capacitor changes due to leakage across the switch, from the amplifier's summing point, or from the supplies (or perhaps even due to the capacitor's own leakage resistance or dielectric absorption). Thus, even though the data may not change at all, as is ideally the case for an aircraft simulator's altimeter in "straight & level" flight, it is necessary to update sample-hold circuits periodically to correct for output droop. On the other hand, so long as the data remains unchanged, a distribution system based on D/A converters (with registers) need not be periodically refreshed.

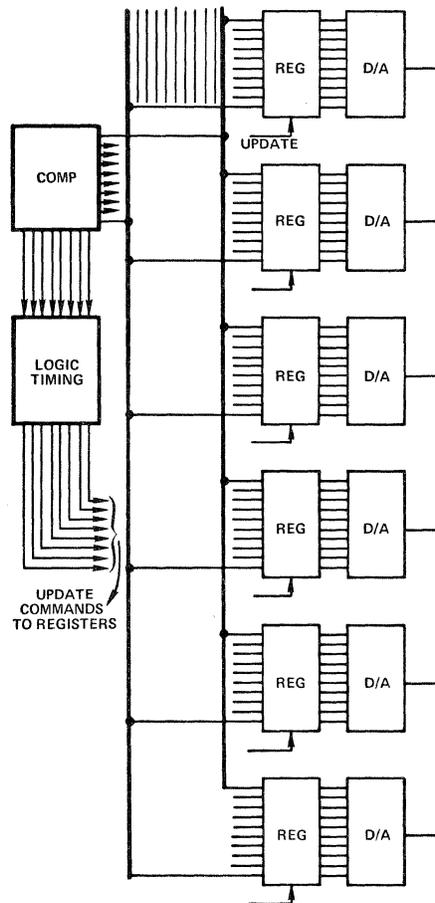


Figure 1. D/A Converter for each channel; parallel-word distribution.

The D/A converter's ability to store without error lays the foundation for an "updating by exception" rule, whereby the data channels are only updated if the *information* changes. Otherwise, the computer leaves the D/A unrefreshed.

A further consideration in the use of D/A converters vs. sample-hold circuits lies in the matter of allowing for acquisition and settling time. The data sheet for a typical data-distribution sample-hold circuit at reasonable cost may call for acquisition periods ranging from $2\mu\text{s}$ to $20\mu\text{s}$ or more. Thus, it is often necessary for the computer to remain connected to each channel for the duration of this acquisition period (unless buffered), which may use up appreciable main-frame time. By contrast, the storage register of a D/A con-

verter can be updated in a fraction of a microsecond, so it is quite conceivable that an entire 10-channel data-distribution system, using one D/A per channel, can be updated in the time required to refresh a single sample-hold circuit.

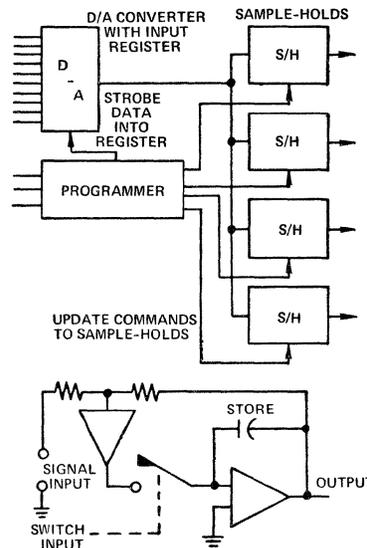


Figure 2. Sample-hold for each channel, with single fast, accurate D/A Converter. Multiplexing occurs by sampling each channel individually as its associated data appears on the input bus.

Offsetting some of the flexibility of the D/A-per-channel data-method is the cost of interconnecting the D/A's to the data source. Parallel data at the 10-bit level requires at least 12 conductors (10 data lines, ground, and command line) from the computer to the D/A converter, which, for fast transmission rates, requires costly multiple twisted pairs. If the D/A's are widely-distributed, as, for example, in a steel rolling mill, installation cost for the cable may easily be the largest single economic factor, far outweighing the cost of the D/A converters. Cable and installation costs can be reduced somewhat by introducing serial, instead of parallel data transmission. However, the penalty now lies in more-involved logic and added updating time (which may not be a problem at all), since each 10-bit channel requires at least 10 times as long to update. (See also SERDEX, in Chapter I-4).

CONVERTER-PER-CHANNEL DISTRIBUTION

Figure 1 illustrates the main ingredients of the distribution approach based on one D/A converter for every channel. Computer data is fed on a parallel bus to all D/A-converter input registers, while an update command is addressed individually to each register. Whenever the computer strobcs a new data word into the data bus, it emits a command signal that causes one of the storage registers to accept this new word. A succession of parallel digital words and update commands then completes the data-refreshing cycle. The converters may be randomly addressed (and with varying numbers of data points per channel) or a computer may program sequential addresses, if the data is programmed to arrive in the same order.

Simultaneous Updating

In some instances – for example, in semiconductor test equipment – it is advantageous to update all analog channels simultaneously, thereby minimizing settling time in both the converter's output amplifiers and the IC device undergoing test. A data-distribution arrangement that eliminates delays caused by sequential refreshing of each D/A converter is shown in Figure 3.

This arrangement (used in the AD7522) interposes an extra digital buffer between the computer's data bus and the D/A converter's input register. The system updates the

buffer registers serially while a previously-programmed semiconductor test takes place; then, as soon as a new set of analog voltage and current values are required, a command signal feeds the new set of digital words from the buffer registers to the input registers. While the device is being tested at these new voltage and current excitation levels, the buffer registers are again loaded sequentially for the following test.

Serial data transmission, to remote DAC's (with or without galvanic isolation) is conducted in much the same way, using two wires for the data, plus an extra conductor for command signals. However, the buffer register in this case is a shift register, accepting the data serially, but passing it on to the converter in parallel. In the AD7522, the buffer registers can be operated in parallel, byte serial, or bit serial.

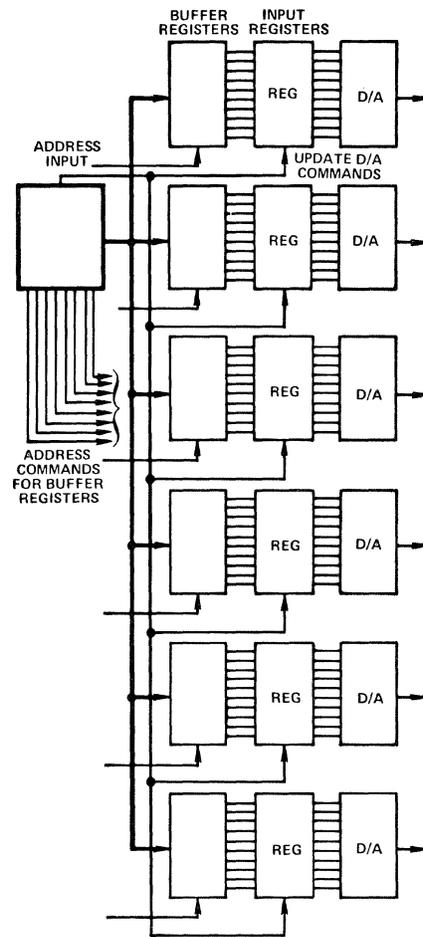


Figure 3. Simultaneous D/A updating.

ANALOG DISTRIBUTION

Two approaches to sample-and-hold-circuit updating are shown in Figures 2 and 4. In Figure 2, analog data is “shipped” over a common cable to all the sample-and-hold circuits. However, each sample-and-hold device, normally in *hold*, remains oblivious to the input data until a command signal connects it momentarily to the data bus (*sample*). On receipt of its update pulse, the sample-and-hold circuit acquires whatever analog information appears on the data line and holds this value until subsequently commanded to acquire a new signal level.

An alternative arrangement, using a modular (de)multiplexer for distribution of analog data among individual channels, is shown in Figure 4. Here, the sample-and-hold circuits respond to whatever signals are presented at their input terminals, and then hold this signal level when the analog input is disconnected. The multiplexer switches serve double duty, both in multiplexing and for charging the *hold* capacitor. Though more subject to leakage and crosstalk than the circuit of Figure 2, this is a simple and low-cost arrangement.

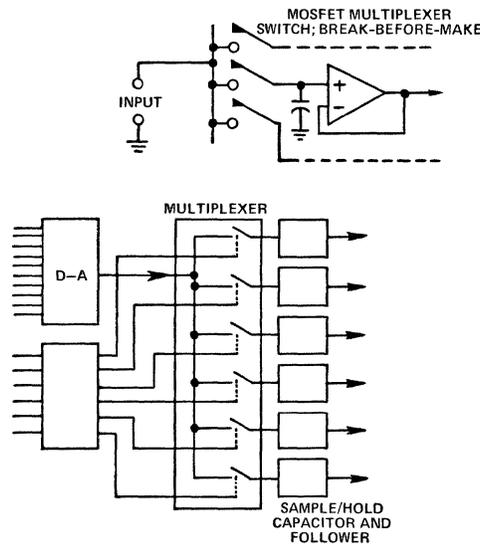


Figure 4. Multiplexing and sample-and-hold using multiplex switches.

A data-distribution arrangement that eliminates sample-and-hold circuitry is presented in Figure 5. Here, the purpose is to utilize the inherent storage capacity of the device being activated. For example, it is possible to distribute data among several d’Arsonval indicators in a utility substation simply by exploiting the natural inertia of the meter movement. So long as the data can be refreshed with sufficient rapidity, the meter’s average response is simply dependent on the “duty cycle” (dwell time at each switch point to refresh period). Thermal ovens can be controlled by pulsing in this way, as can instrument servos and other devices with built-in inertia of one kind or another. For such applications, the converter should have sufficient peak output current-handling capacity and the switches low-enough resistance (perhaps even electromechanical relays) to avoid introducing errors.

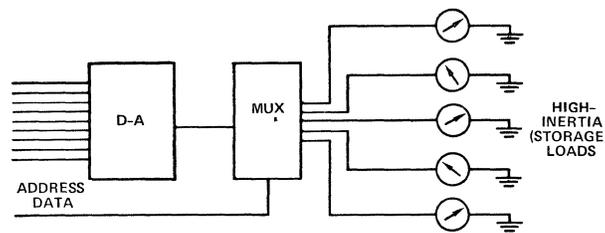


Figure 5. Using output-transducer inertia for averaging and data storage, eliminating per-channel storage (registers or capacitors/op amps).

ACQUISITION vs. DISTRIBUTION

As a rule, data *acquisition* poses more challenging problems than data *distribution*, but some of the problems assume different shapes. Since data distribution can take place at macroscopic power levels (volts and milliamperes), noise is not a great problem (except for *induced* noise in hostile environments). To the contrary, DAC outputs are sometimes boosted, as in programmable power supplies; in such cases, it is useful for the DAC’s output amplifier system to have remote sensing to avoid errors due to voltage drops in the wiring. This may also be the case for high-resolution DAC’s (such as DAC-1138) at more-modest power levels.

Sample-holds used in data acquisition must have short aperture time (or at least small aperture uncertainty) because they must either deal with the “instantaneous” value of a signal, or sample it rapidly at equal time intervals. Their *hold* time need be no longer than is necessary for the ADC to digitize the signal. In short, the emphasis in sample-

hold circuits for data acquisition lies on rapid acquisition, followed by rapid conversion. By contrast, sample-hold configurations used for data distribution usually permit relaxed update timing, but the analog values may have to be preserved for long periods without "droop." Thus, sample-holds for data distribution must have long *hold* times, and short acquisition-and-settling times. Where high resolution (12 bits or better) and large ratios of *hold* to *settling time* are necessary, multiple D/A distribution, with storage in registers becomes preferable; the decreasing cost of IC DAC's makes the choice easy.

FILTERING/SMOOTHING

In data acquisition, the purpose of filtering is to remove (or at least reduce) analog transmitted, inherent, or induced input noise. In distribution, filtering is used to reduce "noise" caused by quantization (finite increments of digital resolution causing discontinuous analog outputs — the obverse side of quantization uncertainty in A/D conversion), and to deal with coupled-in switching transients and "glitches" (which are large spikes caused by intermediate codes introduced by asymmetrical switching times at such transitions as 0111 1111 to 1000 0000.

Discontinuities are often tolerable, especially in DC-value testing, where they occur at the application of test conditions, and readings are not taken until the system has settled. On the other hand, if the converter is producing an analog ramp in discrete steps, the discontinuities may have to be smoothed, and certainly any feedthrough transients and/or "glitches" must be minimized. Linear filtering of glitches is impractical, because they have far from uniform magnitudes and they do not occur at uniform intervals; hence, filtering leads to badly-distorted waveforms. Glitches are minimized at the DAC by very fast switching with the best-possible matching of rise and fall times (to minimize the energy in the pulse), and then plucked out by "degitcher" circuitry, which *holds* the output fixed during switching, then releases it for normal settling. The DAC-10DF is an example of a DAC specifically designed for this purpose.

For reconstructing very coarse sampled data, sophisticated interpolation techniques are used to overcome the limitations of simple filtering. An example is integration of the difference between two adjacent values so that the "points" are connected by straight lines, and the discontinuities become more-easily-filtered changes in slope rather than steps.

THE COST FACTOR

As of this writing, costs of low-resolution monolithic DAC's are very low and still decreasing. For modest-resolution systems (8-10 bits), multiple DAC usage (for example, employ the AD7522, which is double-buffered and even permits serial input, as well as direct interfacing with microprocessors) is competitive with sample-holds, and generally gives better performance, as we have noted. From 10 to 12 bits, sample-holds appear to hold the cost edge. Above 12 bits, it is difficult to obtain sample-holds with adequate resolution and speed because of the problem of obtaining capacitors with decent dielectric absorption characteristics. So, for high resolution, converters-with-registers, though more expensive, must win by default.

MINIMIZING CALIBRATION ERRORS BY SERVOING

Where many low-cost DAC's are used, it is possible to produce outputs that have absolute accuracy limited only by their resolution. This is done by slaving their outputs to that of a high-resolution, accurately-calibrated, temperature-stabilized master DAC (Figure 6).

Figure 6a shows the basic principle, with "master" and "slave" DAC's. In this illustration, computer data fed to D/A(1) is converted and applied to a comparator in which it is compared with the output of the slaved DAC, D/A(2). The comparator's output drives an up/down counter in the appropriate sense to drive the output of the slaved DAC up if it lower than the master and down if it is higher. Thus, at balance, the slaved DAC will hunt between the two values adjacent to the "correct" value. Filtering provides a degree of interpolation.

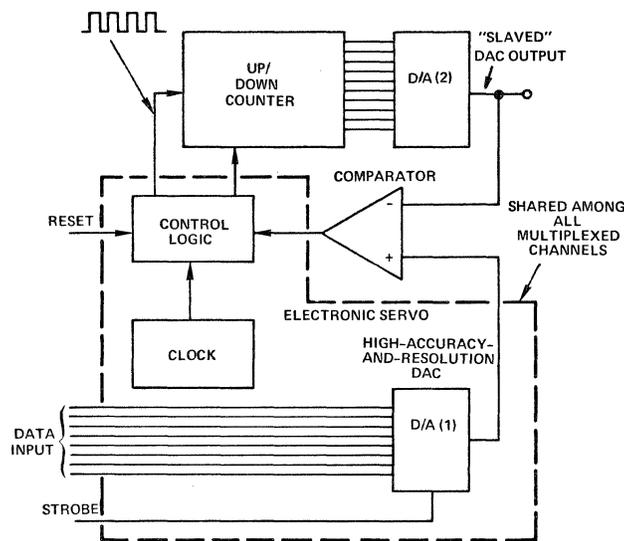


Figure 6a. Controlled-output DAC.

In Figure 6b, this process is extended to multi-channel multiplexing, to update a number of lower-resolution DAC's. Use of feedback as part of the updating process permits an array of low-cost, low-resolution (monotonic) converters to establish precisely-controlled analog output voltages, regardless of calibration drift, but limited by the resolution.

The principal disadvantage of this scheme is its slowness, since the precision DAC must first settle, then the analog output of the DAC being updated must settle to each new trial value before the next clock pulse can be applied to the counter. If the high-precision DAC is a 16-bit unit, (e.g., DAC-1136) with settling-time just under $100\mu\text{s}$, and the DAC's being updated are 12-bit units, with LSB-settling time of $2\mu\text{s}$, each channel can require at least 8ms for updating, but a possible minimum of less than $100\mu\text{s}$. The comparator reversal can be used to signal completed conversion and initiate updating of the next channel, to minimize throughput time per cycle of update.

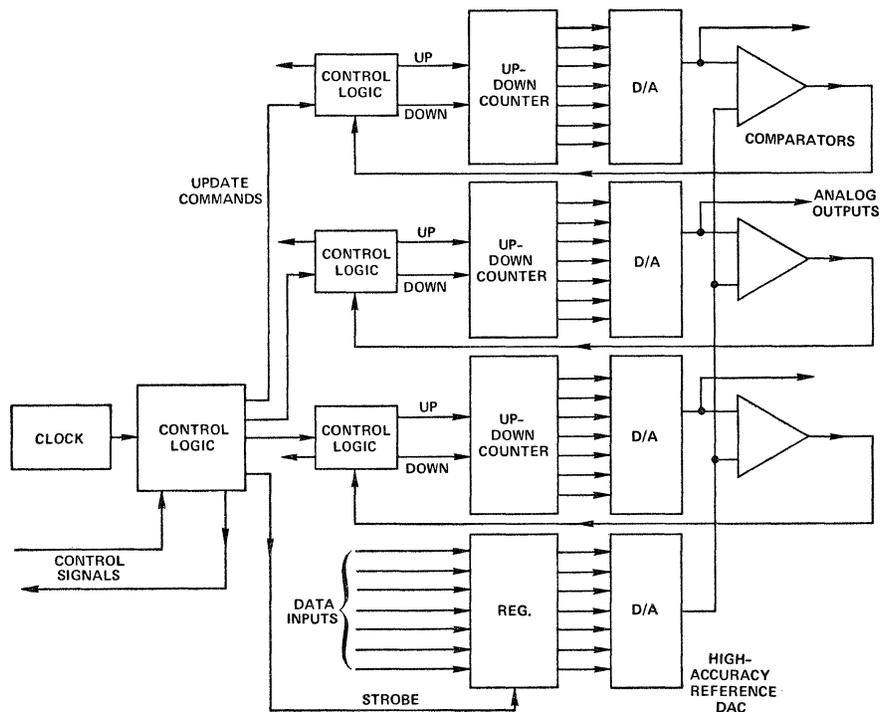
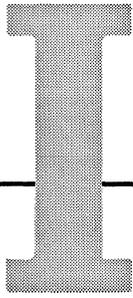


Figure 6b. Low-cost high-accuracy distribution.

ISOLATION

If a data-distribution system is spread over a large geographical area, it frequently becomes necessary to isolate the various analog loads from the digital data source. Otherwise, substantial differences in ground potential at the various locations could cause large ground currents or excessive induced noise. Isolation could be accomplished by transformer or optical coupling, applied either to the digital signals (two-wire line with serial-to-parallel-to-analog conversion at the load), or to the analog signals after conversion, using (for example) isolation amplifiers in the 284 family, which also provide auxiliary floating power for additional remote circuitry, such as low-level preamplifiers.



Subsystems and Data Communications

Chapter I-4

Now that we have seen a number of basic data-acquisition and data-distribution architectures in Chapters I-2 and I-3, it may be worthwhile to pause and consider some forms of system implementation. Areas of contemporary interest include:

1. Proprietary systems, subsystems, and components for interfacing and data communication.
2. Interfacing converters with nearby destinations, such as a microprocessor data bus, using parallel and byte-serial connections.
3. Communicating sensor-based data with distant destinations using serial techniques.

In Chapter I-2, most of the configurations treat parallel data from the converter as an input to a nebulous “buffer” block. This buffer translates the converter’s output into machine data format, monitors the status of conversion, initiates conversions, addresses the multiplexer, initiates sample/hold, gain-ranging, etc. This function is achieved by the purchase of proprietary interface products, ranging from IC’s and modules to complete systems, and integrating them into the user’s overall system.

In this chapter, we shall examine ways in which these forms of interfacing are achieved—first by outlining a number of proprietary systems and subsystems that form a hierarchy, then by a more-detailed consideration of the two basic forms of interfacing—parallel (and byte-serial) and serial.

We must be careful to limit the scope of this discussion, because any one of these topics could itself justify a volume the size of this book for a thorough in-depth treatment of all possible cases. Our method will employ the following techniques: First, this book is oriented primarily towards converters: we shall seek to maintain that focus in this chapter. Second, though we will tend to summarize in somewhat general terms, we will limit much of our discussion to ideas for which concrete embodiments can be found in the Analog Devices product line. This, in turn, permits an abbreviated treatment, with security in the knowledge that the reader who desires greater depth can find substantial amounts of detailed information relating to specific approaches in our published literature (and products available to implement them).

1. SUBSYSTEMS FOR INTERFACING CONVERTERS TO ANALOG AND DIGITAL WORLDS

Briefly summarizing some salient ideas from earlier chapters, data acquisition is the process of transforming electrical voltages or currents, usually transducer outputs, into digital information to be received at some defined destination in a system, for storage, display, processing, or further transmission (Figure 1). The data-acquisition process typically involves these forms of activity:

- Analog signal-manipulation
- Analog-digital conversion
- Digital signal manipulation
- Digital control manipulation

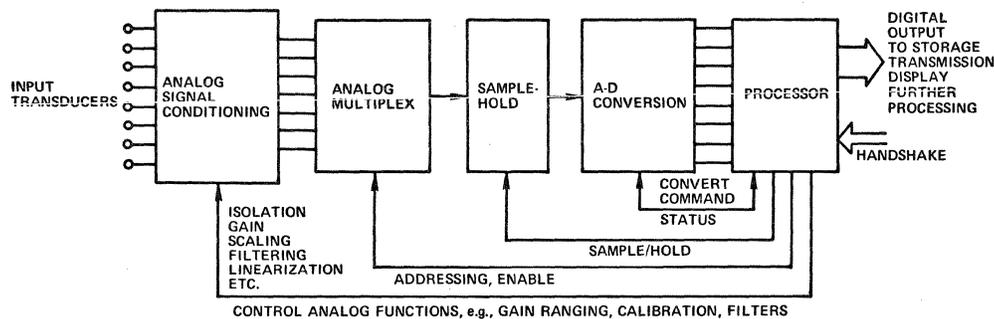


Figure 1. Data-acquisition function.

Analog signal manipulation includes such operations as isolated pre-amplification, gain adjustment, linearization, algebraic functions (perhaps involving other inputs), sample-hold, and analog multiplexing.

An *analog-to-digital converter* produces a parallel or serial digital code that represents the ratio of an analog signal to a reference voltage or current. The digital code is usually—but not always—a binary or binary-coded-decimal number proportional to the ratio.

Digital SIGNAL manipulation might involve multiplexing, various arithmetic and logic operations—e.g., magnitude comparisons, algebraic operations, code or format conversions—storage, transmission to a central or intermediate processor, and deriving control signals for either digital handshaking or for operations on the “real-world” portion of the system.

Digital CONTROL manipulation includes control of all digital operations, programming of analog functions (switching gains or circuit configurations), selection of analog channels, initiation of conversions, etc., and all of the associated software.

A *data-acquisition system* (for our purposes) is a self-contained subsystem, consisting of the conversion function (which involves at least one a/d converter) and some portion of both the analog and the digital manipulation circuitry. This definition is obviously quite flexible, since it permits a full *functional* range from a simple a/d converter (with a given analog span and digital controls) to an “intelligent” multi-channel measurement-and-control subsystem—and a full *physical* gamut from an integrated-circuit chip to a rack (or a room) full of equipment.

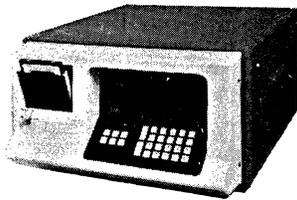
The properties that define a given subsystem are determined by the application; their choice is affected by such factors as resolution, noise levels, system size and complexity, delegation of system tasks, frequency and level of interactions, the physical environment, and (of course) cost—of hardware, of software, of wire, and of system development, prototyping, and manufacture.

When choosing the approach to take in designing a system, one system designer’s component or subassembly may be another designer’s turnkey system. In general, the design problem involves a classical “make-or-buy” situation. The designer will purchase available components or subsystems that reflect the level of integration that is a best compromise between out-of-pocket cost and the many costs—both overt and hidden—of expending design and manufacturing effort in technological areas that are peripheral to one’s primary mission.

The hierarchy of systems integration is especially deep at Analog Devices, ranging as it does from integrated-circuit converter chips to complete processor-based turnkey quality-control systems for the textile industry. As examples of levels of the hierarchy that are relevant for readers of this book, Table 1 lists some specific products that were available from Analog Devices in January, 1977.*

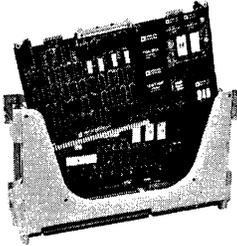
*Since a complete discussion of their properties and applications is beyond the scope of this book, we will discuss several of these products in the context of their role in the conversion system. Complete information is available, ranging from free data sheets and brochures to complete instruction books and software manuals (at reasonable cost). Consult a nearby Analog Devices field office, or write to the address on the flyleaf of this book.

TABLE 1. REPRESENTATIVE EXAMPLES OF DATA-ACQUISITION SYSTEMS, SUBSYSTEMS AND SUBASSEMBLIES MANUFACTURED BY ANALOG DEVICES IN JANUARY, 1977.



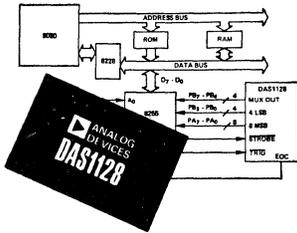
MACSYM ONE Fully Integrated Measurement And Control SYsteM

Macsym One is a processor-based Measurement and Control SYsteM used to automate the measurement, evaluation, and control of real-world events--analog and digital--while interfacing with human operators and other computers. In one compact package, it incorporates a processor, interface modules, an operator's panel, serial data ports and easy-to-use software. It can handle expandably from 8 to 4000 analog or digital input/output signals.



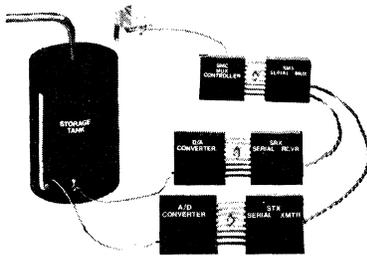
RTI-1200 Analog/Microcomputer Interface Subsystem

The RTI-1200 Real-Time Interface is a complete ready-to-use analog input/output subsystem designed for physical, electrical, and software compatibility with the SBC-80/10 Single-Board Computer--and easy interfacing with any other 8080-based microcomputer having accessible address, data, and control buses. Interfacing as a block of memory locations, it has extraordinary versatility.



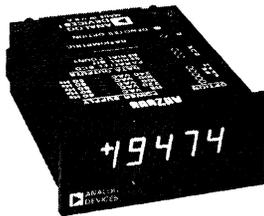
DAS1128 Data-Acquisition Subsystem

The DAS-1128 is a general-purpose 12-bit basic data-acquisition building block that can accept 8 differential or 16 single-ended analog inputs, multiplex them, sample-hold, and convert, with a maximum throughput rate of 35kHz. It can be readily interfaced with microcomputer systems.



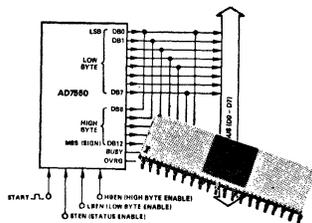
SERDEX SERIAL Data-EXchange Modules

SERDEX modules (and cards) permit easy communication between the parallel-digital-data world of ADC's, DAC's, DPM's and other digital instruments, and the 2-wire ASCII world of teletypewriters and computers. *Transmitters* translate parallel data to asynchronous serial, *Receivers* translate ASCII to parallel, and *Multiplexers* permit operation of a number of modules in a system.



AD2008 Versatile Systems-Oriented Digital Panel Meter

The AD2008 is a 4½-digit line-powered DPM, with a floating opto-isolated front end, designed for making accurate measurements in adverse electrical environments. Besides an easy-to-read display (for the human interface), it has both parallel-BCD and pulse-train options available, and a variety of control facilities, for flexibility in interfacing with local or remote equipment.



AD7550 Single-Chip Microprocessor-Compatible Ratiometric ADC

The AD7550 is a 13-bit analog/digital converter on a single monolithic chip. Its three-state digital data outputs and *select* lines permit direct interfacing with an 8-bit microprocessor data bus in byte-serial format. It can be easily configured for memory-managed I/O. Its "quad-slope" conversion technique provides stabilities to within 1ppm/°C.

We will review briefly the functional repertoire of these products in relation to the conversion interface, starting with the simplest (the AD7550) and working our way up the chain.

THE AD7550 13-BIT CONVERTER ON A CHIP

The AD7550 is a 12-bit-plus-sign 2's-complement ratiometric a/d converter, built on a single monolithic CMOS chip and housed in a 40-pin DIP package. As the block diagram in Figure 2 shows, it is an integrating converter, employing the quad-slope principle (see Chapter II-2), and it requires a reference, three resistors, and a capacitor for normal fixed-reference operation. The data output is available via two sets of three-state latches*, one for the 5 more-significant bits and the other for the 8 less-significant bits. The conversion-status ($\overline{\text{BUSY}}$) and overrange outputs are also three-state; this permits them to be connected to a micro-processor's common data bus and treated as data (as we shall shortly show in Figure 12).

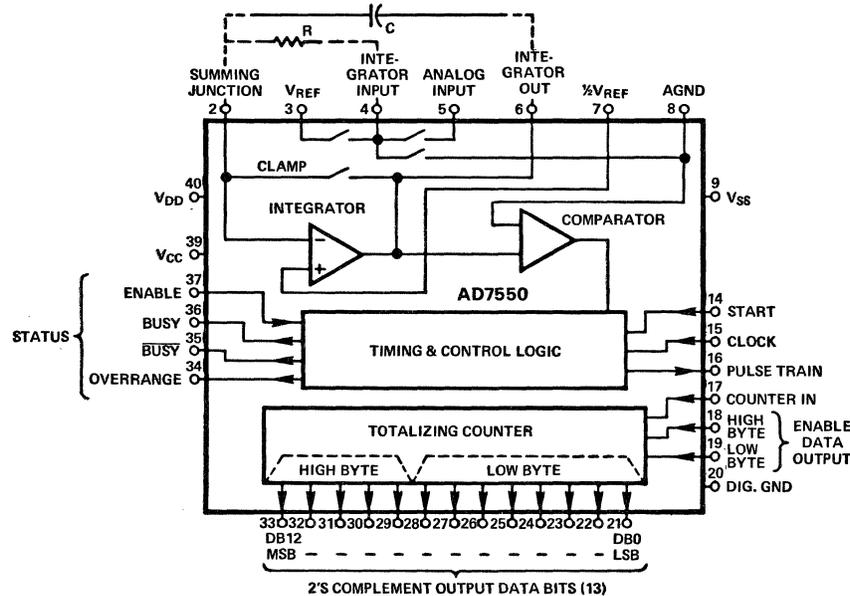


Figure 2. Block diagram of the AD7550 A/D converter.

Thus, the AD7550 can provide either full-parallel 13-bit data output (with both bytes enabled) or byte-serial data output (with both bytes wired to a common bus and enabled at different times). In addition, a pulse-stream output can be used with a remote counter for a kind of serial data transmission.

THE AD2008 SYSTEM-ORIENTED PANEL METER

The AD2008 (Figure 3) is a 4½-digit-plus-sign panel meter designed for flexible system interfacing, as well as for accurate display of input voltage or its ratio to external references. Optional BCD or pulse-train outputs permit either parallel or serial interfacing. Line-powered operation and opto-isolation permit floating measurements to be made in the presence of common-mode voltages as great as 300V rms. In addition to magnitude and sign information, digital outputs also include DATA READY and (for the parallel option) OVERLOAD; control inputs include a 4-mode external TRIGGER-HOLD (2.5 conversions/second, maximum-rate conversion, finish-this-conversion-and-hold, start conversion), and remote display controls (test segments, blank display, blank polarity).

*Three-state latches provide normal "1" or "0" data when enabled; the output floats (open switch) when not enabled. This permits a number of channels to share a common bus (enabled-one-at-a-time).

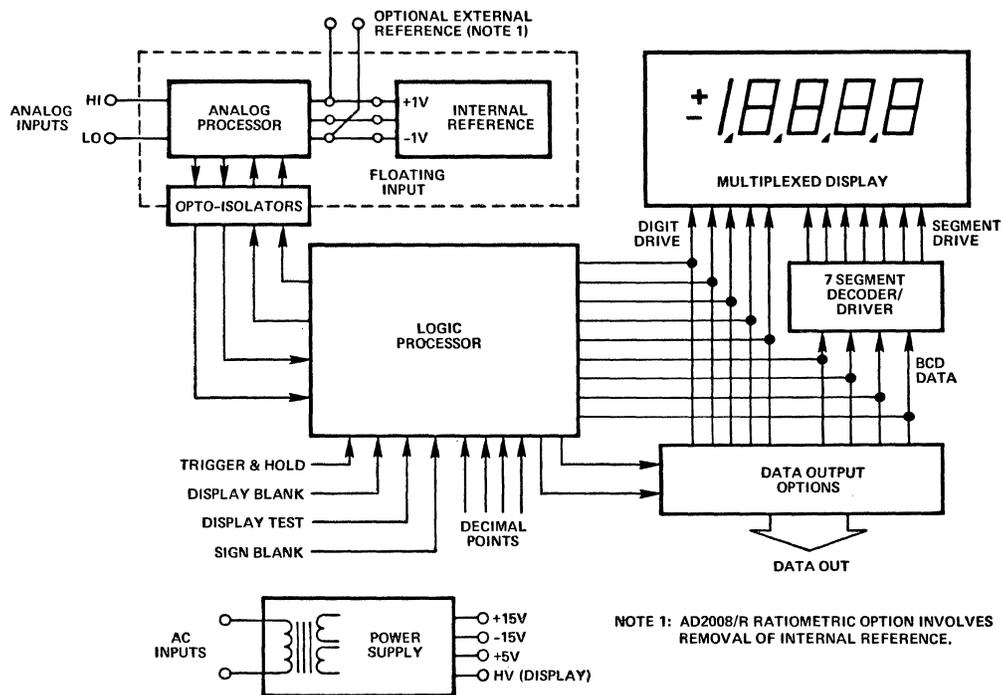


Figure 3. AD2008 block diagram

SERDEX SERIAL DATA-EXCHANGE CARDS

SERDEX (SERial Data EXchange) components are flexible building blocks of systems in which converters and other controlled devices can communicate with remote (up to 3km distant) destinations under remote control, over a single twisted wire-pair, using asynchronous serial ASCII-coded digital information. The three principal components are the STX transmitter, the SRX receiver, and the SMX multiplexer, shown in basic functional block form in Figure 4. A brief example shows how SERDEX works: The asynchronous port, a Teletype machine, transmits the ASCII code for the character "?". Upon receiving it, the STX initiates a conversion. When the conversion has been completed, the STX translates the parallel BCD output of the converter into ASCII format and sends back the numerical magnitude of the converter input for printout, digit by digit. Since the STX ignores alphabetic characters, a printout might look like this:

HOW MANY TONS OF GRAVEL ARE ON THE SCALE? 112

The STX also responds to six characters, in addition to "?", as shown; they can be used to initiate switch closures. For example, the next command might be

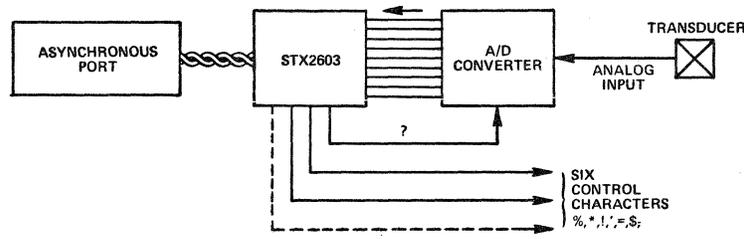
DUMP THE LOAD!

The "!" would initiate a switch closure to carry out the instruction. The SRX receiver communicates with d/a converter, to provide an analog output, in response to a transmitted ASCII number, followed by the symbol "\$"; the SRX will also accept six other control characters, like the STX. For systems involving more than one transmitter and/or receiver, the SMX digital multiplexer sorts out the messages, in response to the character "#" and a numeral. For example,

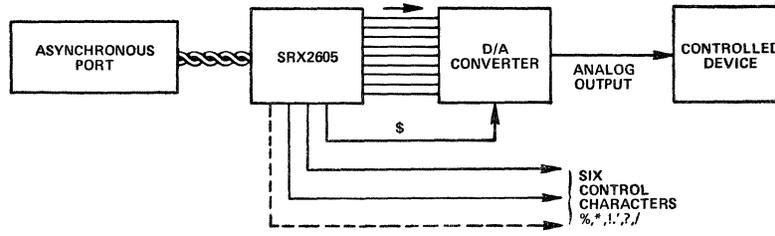
HOW MANY CC OF SOLUTION ARE IN BEAKER #2? 053

causes the multiplexer to select STX number 2; at the same time, the a/d converter associated with the level measurement performs a conversion and sends back its reading, 053.

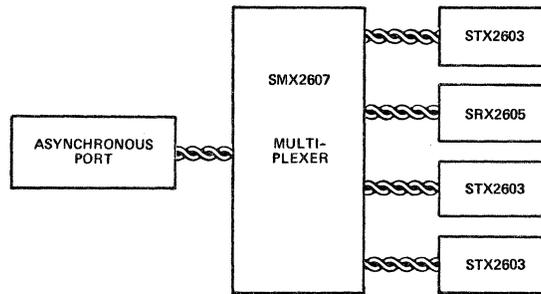
It is not hard to see that pilot measurement-and-control systems of respectable magnitude can be quickly assembled with little software development, using standard Teletype machines or computers of any scope having asynchronous serial data ports. More information on SERDEX and its applications can be found in Section 3 of this chapter.



A. Transmitter (STX2603)



B. Receiver (SRX2605)



C. Multiplexer (SMX2607)

Figure 4. The elements of SERDEX.

DAS1128 DATA-ACQUISITION SUBSYSTEM

Thus far, we have considered two forms of system-oriented converters and a family of system components that are converter-oriented. We now come to a classical data-acquisition subsystem, the DAS1128. It can be seen that its form (Figure 5), resembles the central structure in Figure 1. The DAS1128 comprises an analog-input-signal multiplexer, a sample-hold amplifier, a 12-bit a/d converter, and all of the programming, timing, and control circuitry needed to perform the data-acquisition function and provide a parallel digital output in binary, offset-binary, 1's-complement, or 2's-complement coding.

The user, by choice of external jumpers, can determine whether the device is to accept 8 channels of differential signals, 16 channels of single-ended signals, or 16-channels of "pseudo-differential" input, with a common reference. The multiplexer can be jumpered to scan continuously any number of consecutive channels, from 2 to 16, to scan sequentially on step command, or to select channels as randomly addressed.

The user can also connect the device to establish a variety of full-scale ranges, with either round-number full-scale voltage (e.g., 0 to +10V), or round-number per-bit voltage (LSB = 2.5mV, full scale = 10.24V). Where throughput rate is of prime importance, the device may be connected in an OVERLAP mode, in which the next channel may be selected while a conversion is in process; in addition, the clock frequency may be adjusted for the best conversion-time/accuracy tradeoff, and, finally, the conversion may be short-cycled to the

minimum-acceptable number of bits. The range of throughput rates is from 35,000 12-bit conversions per second for different channels to 200,000 successive 4-bit conversions per second on a single channel.

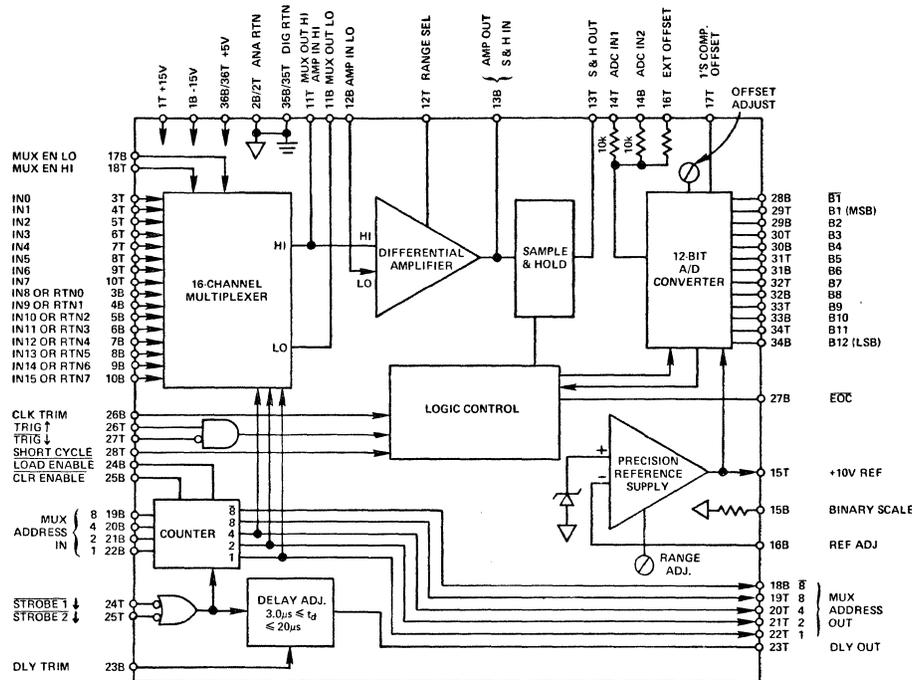


Figure 5. Block diagram of the DAS1128 data-acquisition subsystem.

The DAS1128 can be made to interface with a microcomputer via peripheral interface chips, as you will see in Section 2. However, the burden of interfacing is on the designer of the system. For a subsystem that relieves the system designer of hardware problems relating to the analog-digital-processor interface (and even many of the software considerations), one can turn to the RTI-1200, which is physically, electrically, and software-compatible with a popular single-board microcomputer, the Intel SBC-80/10.

RTI-1200 REAL-TIME INTERFACE

Figure 6 shows the salient electrical features of the RTI-1200 "Real-Time Interface". First of all, the upper central portion of the diagram shows the conventional multiplexer-sample-hold-a/d converter configuration, that is characteristic of data-acquisition systems, and a pair of optional d/a converters, for analog data distribution. At the left are the direct connections to the microcomputer buses: data, control, and address. Other elements of the RTI-1200's optional (*) and inherent hardware features are overvoltage protection at the analog inputs, a programmable-gain amplifier for up to 3 bits of additional dynamic range, 4-20mA current inputs and outputs*, logic drivers for controlling external devices, a dc/dc power converter for deriving all operating voltages from the +5V computer power bus*, a pacer-clock system for relating the computer to real time and for producing repetitive events within the RTI-1200, and a socket for user-installed 1k programmable read-only memory (PROM), which may be used either in relation to tasks involving the RTI-1200 (such as data-linearizing) or simply to add memory capacity within the microcomputer system.

It should be readily apparent that, in hardware alone, the RTI-1200 marshals on one board a fairly complete data-acquisition function. Its software features make that function even more accessible. First, it is designed to appear to the computer as a block of memory locations. This means, for example, that with the appropriate address and a MEMORY WRITE command, an a/d conversion can be initiated or data strobed into one of the d/a converters. Some of the operations that become easy software exercises include:† self-checking, calibration, use of multiple RTI-1200's (with *card select*), improving throughput rates, acquiring

†Techniques for these operations, and more, can be found in the *RTI-1200 User's Guide*, \$5, Analog Devices, Inc., P.O. Box 796, Norwood MA 02062.

data on sequentially numbered channels, automatic gain ranging, end-of-conversion interrupts, pacer-triggered interrupts, etc.

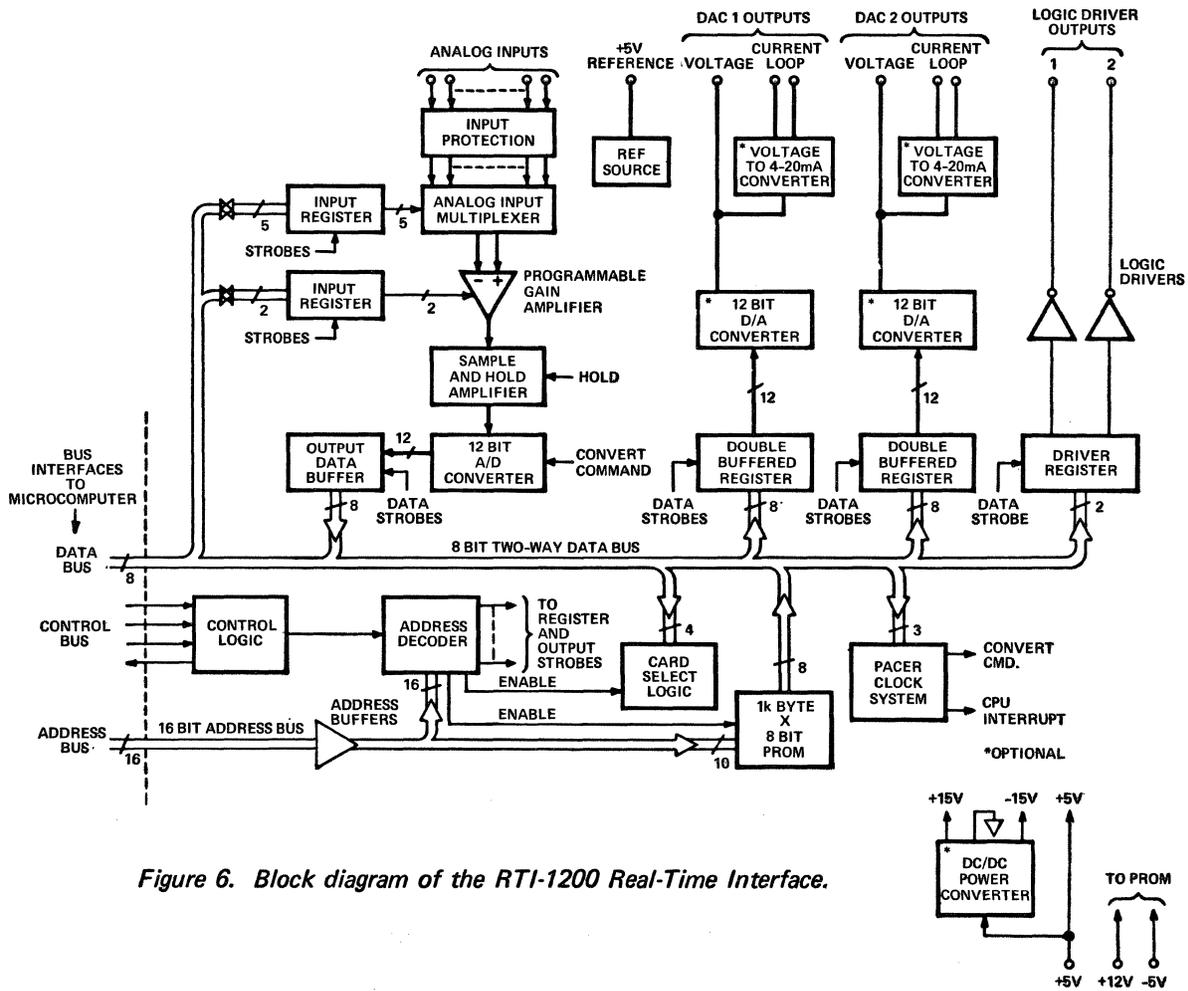


Figure 6. Block diagram of the RTI-1200 Real-Time Interface.

Beyond the RTI-1200, and the limitations of its host computer, the SBC-80/10, one would have to consider a general-purpose integrated Measurement And Control SYstem, processor-based, that could automate the measurement, evaluation, and control of analog and digital real-world events, while interfacing with human operators, other computers, and peripherals. Such a system is Macsym One. As the block diagram in Figure 7 shows, it incorporates a processor, interface modules, an operator's panel, serial data ports. It also includes easy-to-use software involving a sophisticated operating system.

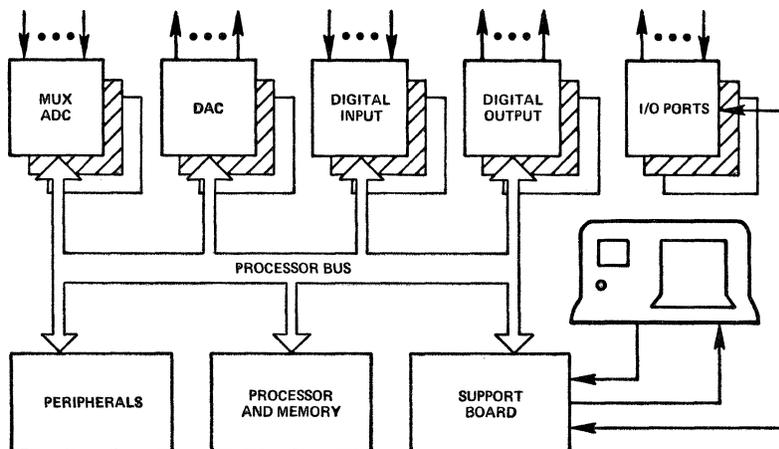


Figure 7. Block diagram of Macsym One system hardware.

MACSYM ONE—A COMPLETE SYSTEM

Macsym One is a fully integrated hardware/software system, easily programmable in a high-level measurement and control language, designed to simplify the application of computing power to “real-world, real-time” measurement and control problems, particularly when computer knowhow, time, money, or staff is in short supply. It can be used as a programmable instrument, programmable controller, programmable data-logger, programmable calculator, and remote network processor.

Its *hardware* consists of a chassis containing a single-board processor with memory, a system-support board, an operator's control panel, and a backplane capable of accepting 16 additional option boards. Systems are configured by plugging standard off-the-shelf boards (as required for a particular application) into the backplane, which serves as a communications and power bus. Expansion chassis are also available. Input/output (I/O) boards provide functional interfaces to analog and digital real-world process signals. A unique “master-slave” expansion concept permits each family of I/O boards to be expanded 16-fold. The system supports a number of standard peripherals, including floppy disk and cassette tape for program and data storage, Tektronix 4006 storage-tube graphic display, and RS232 ports for remote communication and user interfacing via RS232-compatible peripherals.

The supporting *software* greatly simplifies the task of creating and running programs that match the system to the application. The support packages include a high-level language for program development using simple English/algebraic expressions (MacBASIC), an executive program (XMAC) that facilitates the development and manages the running of user programs or subroutines written in high-level or assembly language, and an assembly-language system—for creating assembly-language object code—that may be linked to and called from the high-level language.

This completes the summary of a gamut of proprietary systems, subsystems, and components for interfacing and data communication. It has been intentionally wide-ranging, and if the reader has found it incomplete and somewhat breathtaking, these are perceptions that were by no means lost to the writer. Let us now consider in somewhat greater detail a common application of a number of the devices described, the interfacing of parallel data.

2. INTERFACING CONVERTERS WITH MICROPROCESSORS, USING PARALLEL CONNECTIONS

Microprocessors, because of their low cost and ready availability, have established what will be the prime area for converter interfacing in the future. It therefore makes sense to indicate how the general principles discussed in earlier chapters can be applied in fairly specific ways to microprocessors.

There is plethora of detailed microprocessor architectures and software systems, differentiated by manufacturer, by “generation,” and by degree of integration. It would be futile and well beyond the scope of this chapter to explore even a few of them in detail. Instead, we shall seek to show the elements that most microprocessors have in common and to indicate how some of the conversion and data-acquisition devices mentioned earlier can be interfaced to μP 's. Many of the underlying ideas can be found, with considerably more flesh on them, in volumes of “The Bugbook” series*, which contain a wealth of basic information and sets of microcomputer-interfacing experiments, using 8080-based systems. EDN's Microcomputer Systems Reference Issue is also a useful source.†

A *microcomputer* is a full, operational computer system based on a microprocessor chip. A *microprocessor chip* (packaged integrated circuit) is something less than a microcomputer, and the difference between the two is simply a measure of a continually shrinking technological gap. Figure 8 shows a functional diagram of the connections to an 8080 microprocessor. They include a 16-bit unidirectional latched address bus, which is used to address one eight-bit byte out of a possible 65,536 bytes of (external) memory; an 8-bit bidirectional data bus

* A vintage example is THE BUGBOOK III, by David G. Larsen, Peter R. Rony, and Jonathan A. Titus, 1975, published by E & L Instruments, Inc., 61 First Street, Derby, Connecticut 06418.

†At hand at the time of writing was the 1976 issue (Nov. 20, No. 21), EDN Magazine, Cahners Publishing Co., Inc., Boston.

for transferring data to or from the processor; a set of power-supply terminals; a pair of clock terminals; and a set of incoming and outgoing control lines. The processor itself contains an accumulator, a set of registers, and the operational capability of carrying out up to 256 different instructions, coded in 8-bit words. The instruction groups include data-transfer; arithmetic operations; logic operations; branching operations; and stack, I/O, and machine-control operations.

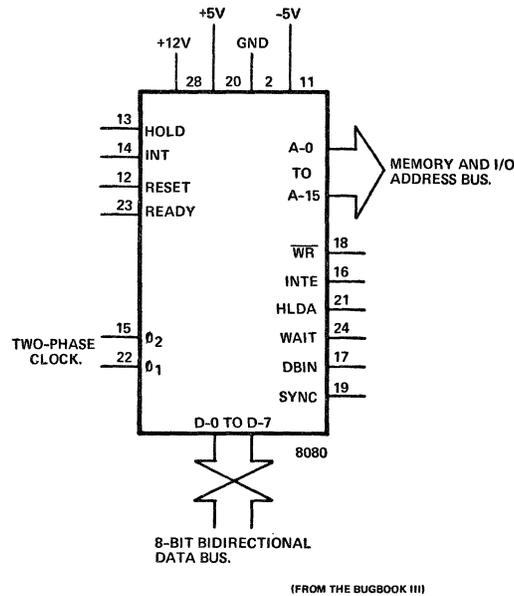


Figure 8. Functional diagram of connections to the 8080 microprocessor.

“Double-precision” operations are inherent: a number of instructions string two 8-bit data bytes together as a 16-bit word. It will be seen that this is a useful feature in dealing with converters.

MICROPROCESSOR INTERFACING, I/O VS. MEMORY

To interface a converter or a data-acquisition system to a microprocessor, a number of requirements must be fulfilled:

It must be possible to address the converter subsystem, and, if a MUX with random addressing is used, it must be possible to address specific analog channels.

The output of the converter must be transformed to a compatible format and to circuitry compatible with three-state bussing.

Suitable software and control signals must be provided to initiate conversion, determine when conversion is complete, and transfer the data appropriately.

There are two common ways of interfacing peripheral devices with microcomputers (Figure 9). One utilizes an area of memory space, usually restricted in extent, set aside for I/O devices; for example, 256 inputs and 256 outputs may be used with the 8080. These inputs/outputs interface with the accumulator via peripheral interface chips, which handle the addressing, the conversion of (say) 12-bit parallel to two three-state \leq 8-bit bytes, and the controls for I/O read/write.

The other approach, memory-managed interfacing, treats the external I/O devices (and their peripheral chips, if necessary) as memory, using the controls for memory read/write. This approach makes available a much larger number of possible addresses and greater freedom over their disposition, as well as the large number of instructions involving memory, including—in the case of the 8080—the double-precision 16-bit memory load-and-store instruction, which becomes directly available for input/output control.

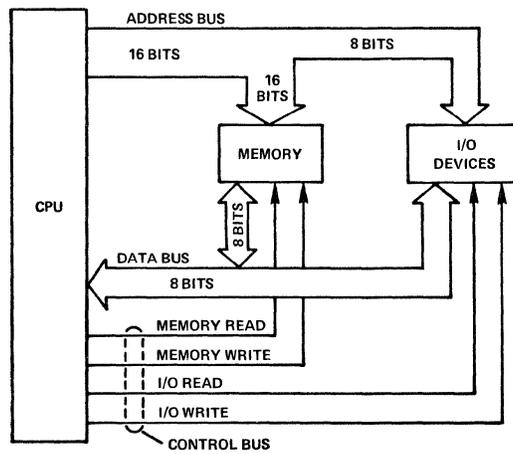


Figure 9. Accumulator (or isolated) I/O vs. memory mapped I/O.

There are some other advantages to memory-managed I/O. Figure 10 shows an interpretation of a microprocessor's principal role (that it has in common with all stored-program digital computers), that of memory controller. Its primary function is to fetch instructions from memory. Time-wasting dislocations caused by the intrusion of the outside world into this satisfying internal game are minimized if the outside world can be made to look like memory. For example, the processor may think it is writing into memory when it is really updating the output voltage of a DAC. Since different microprocessors communicate with memory in essentially the same way, it becomes simpler (for both user and vendor) for a company like Analog Devices to furnish memory-managed I/O devices (especially basic IC chips, such as the AD7550 a/d converter) that will communicate, in concept, with a large majority of available microprocessors, whatever the details of their hardware or software.

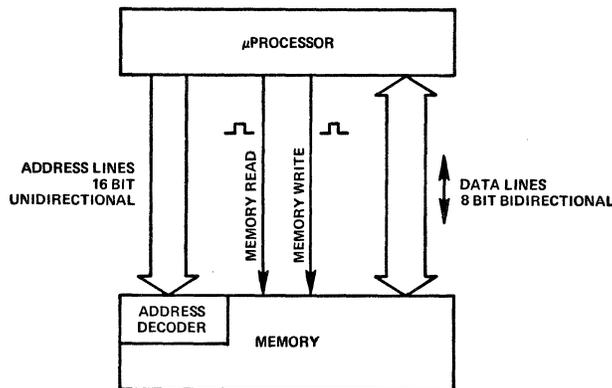


Figure 10. A microprocessor is a memory-controller.

Finally, the use of memory ports for I/O permits the use of "horizontal" memory-managed I/O ("card select" in the RTI-1200). This technique allows the design of highly structured operating-system architectures, which can sidestep the difficulties posed by lack of relative- and index-addressing modes in the 8080.

Concrete examples of some of these concepts can be given in terms of the products mentioned earlier in this chapter.

INTERFACING DAS1128 AND AN 8080

Figure 11 shows how a DAS1128 data-acquisition subsystem might be interfaced with an 8080, using an 8255 peripheral interface chip. A typical sequence of events, slightly simplified, is this:

1. A "setup" byte, addressed to this channel (address decoded), is latched (written) into the 8255. It configures the 8255 as a set of two input ports (8 and 4 bits), which will receive the data from the converter, and one 4-bit output port, which will address

the appropriate MUX channel. (The DAS1128 will have been configured for random addressing.)

2. A MUX-address byte, addressed to this channel (address decoded), appears on the data bus and is latched (written) into the MUX-address input of the DAS1128, causing the multiplexer to switch to the appropriate channel.
3. A conversion command, addressed to this channel (address decoded), is written into the DAS1128's $\overline{\text{STROBE}}$ input and initiates a conversion cycle, starting with sample-hold.
4. At some later time, when the conversion can be expected to have been completed, successive READ pulses, addressed to this channel (addresses decoded), cause data in the 8-bit and 4-bit input bytes of the 8255 to be transferred to the microprocessor. It is also possible (but not shown for the sake of simplicity) for the DAS1128's STATUS (BUSY) line to have triggered an *interrupt* cycle when the converter's output became valid, in order to get fast handling without tying up the processor during the conversion. Interfacing could be either I/O or memory-managed, trading off 8-bit (I/O) vs. 16-bit (memory) addressing for the sake of simpler software (2-byte instructions) and faster machine handling.

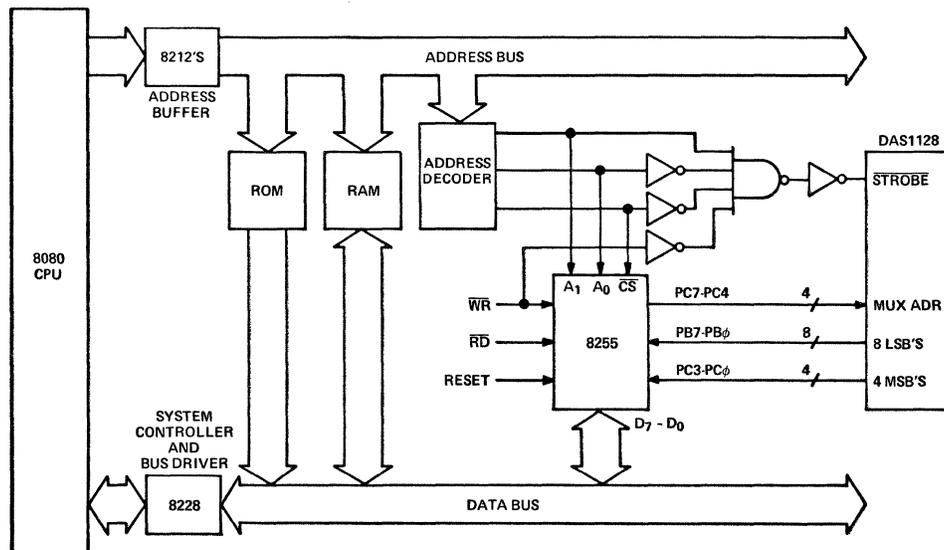


Figure 11. Interfacing a DAS1128 to an 8080 microprocessor.

It is easy to see that essentially the same technique could be used to interface a simple 12-parallel-bit converter, such as the AD572, without the MUX, and with or without a sample/hold. If a separate sample-hold (such as the AD582) were used, an appropriate time delay must be used between the initiating HOLD command and the start of conversion.

INTERFACING AD7550's WITH MICROCOMPUTERS

If the converter has three-state outputs with two separate ≤ 8 -bit bytes that can be individually enabled, the peripheral-interface chip can be eliminated. The AD7550 is a good example of such a converter. Figure 12 shows how the AD7550 may be connected to an 8-bit data bus. The outputs of the AD7550 are arranged in three groups, each having 3-state outputs and independent *select (enable)* lines. The three groups are:

1. Low 8 bits of the data word.
2. High 5 bits of the data word.
3. The "status" bit (busy signal) and the overrange bit.

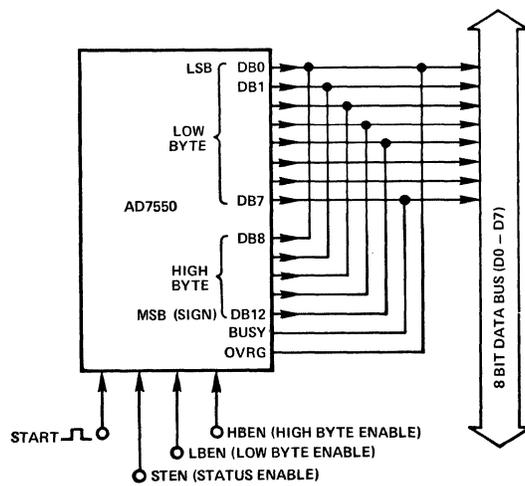


Figure 12. Interfacing the AD7550 to an 8 bit data bus. Coding of AD7550 is 13-bit 2's complement.

When wired as shown, each of the three groups can be selected and enabled (500ns max access time) for transmission on the data bus. A fourth signal, START, is required to initiate conversion.

A NOTE ON BIT-LABELLING

Note that the labelling of the bits differs from the normal bit-labelling used in conversion technology. Elsewhere in this text, the most-significant bit is labelled "Bit 1", and the least-significant bit is "Bit n", corresponding to the *fractional* binary weights, 2^{-j} ; that is, bit 1 has the weight $2^{-1} = 1/2$, and the LSB has weight $2^{-n} = 1/2^n$. This corresponds naturally to the way converters work (full-scale digital output generally corresponds to a unity ratio of analog signal-to-reference). Perhaps unfortunately, microprocessor manufacturers have chosen to use *integer*-binary bit notation, in which the most-significant bit is labelled "Bit n-1" and the least-significant bit is "Bit 0", corresponding to the integer weights, 2^j ; that is, bit (n-1), the MSB, has the relative weight 2^{n-1} , and bit 0, the LSB, has the weight $2^0 = 1$.

The difference in format, for two-byte words, corresponds to the difference between "left-justified" words (integer point at left), e.g., (12 bits)

1	0	1	1	0	1	1	1
---	---	---	---	---	---	---	---

1	1	0	1	X	X	X	X
---	---	---	---	---	---	---	---

 and "right-justified" words (integer point at right), e.g.,

X	X	X	X	1	0	1	1
---	---	---	---	---	---	---	---

0	1	1	1	1	0	1
---	---	---	---	---	---	---

. (For better or worse,) the "first-generation" of μ P-compatible devices discussed here are formatted for ease-of-use with popular microprocessors, rather than for either historical continuity or highest analog accuracy in the single-byte 8-bit mode. Hence, in the AD7550, (and the AD7570 successive-approximations ADC, and the AD7522 multiplying DAC), the low byte has the 8 less-significant bits, the high byte has the (five) more-significant bits, and the bits are labeled from DB_{n-1} (the MSB) to DB_0 (LSB).

Figure 13 shows how two AD7550's, each connected as in Figure 12, could interface to the idealized microprocessor of Figure 10. Since the AD7550 was designed as a compromise for both parallel and byte-serial operation, the external address decoding logic is necessary, as shown. The resulting interface is nevertheless quite simple. The 1:8 decoder identifies 8 different instructions, all implemented as MEMORY READ, including the START CONVERSION, which is implemented with a dummy READ command. Following the START command, the microprocessor can examine the status of conversion at will by reading data from the *status* (BUSY) addresses. When this datum indicates that the conversion process has been completed, a single 16-bit MEMORY READ instruction will provide the 13-bit digital value.

If it is desired that the end-of-conversion (EOC) produce an INTERRUPT request, the *status* line could be wired to an interrupt request line and enabled at the start of conversion. This scheme can be extended to embrace any number of ADC's, or indeed any number of combinations of ADC's and DAC's for an analog in/out subsystem.

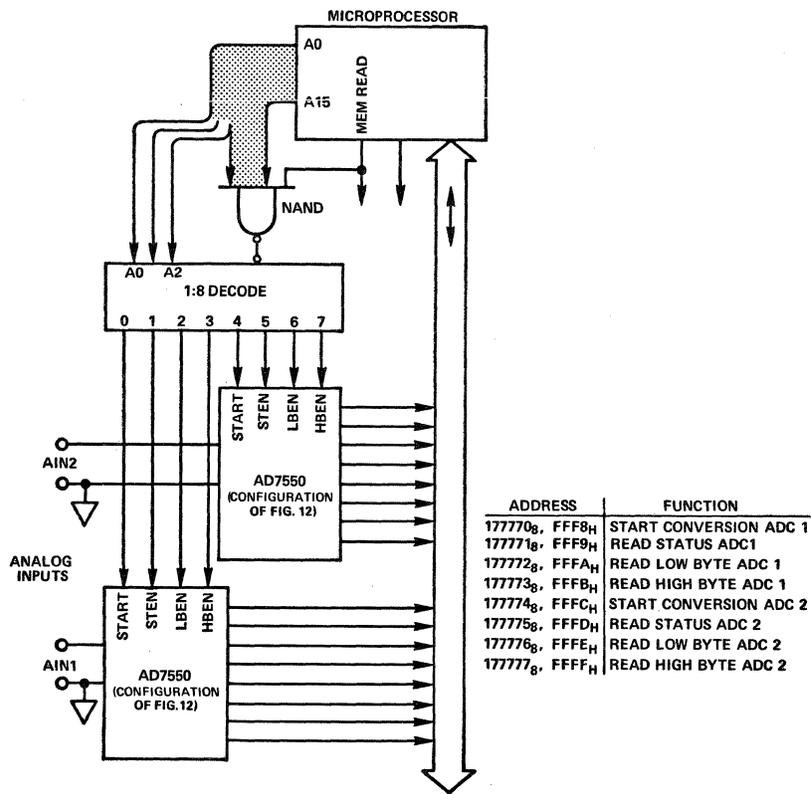


Figure 13. Interfacing multiple AD7550's to a microprocessor.

SOPHISTICATED MEMORY-MANAGED INTERFACING VIA THE RTI-1200

One of the RTI-1200's most important features is the way it interfaces to a microcomputer. It appears as a block of memory locations, using the memory-managed I/O technique; all of the 8080's memory-reference instructions can be used in communicating with the RTI-1200.

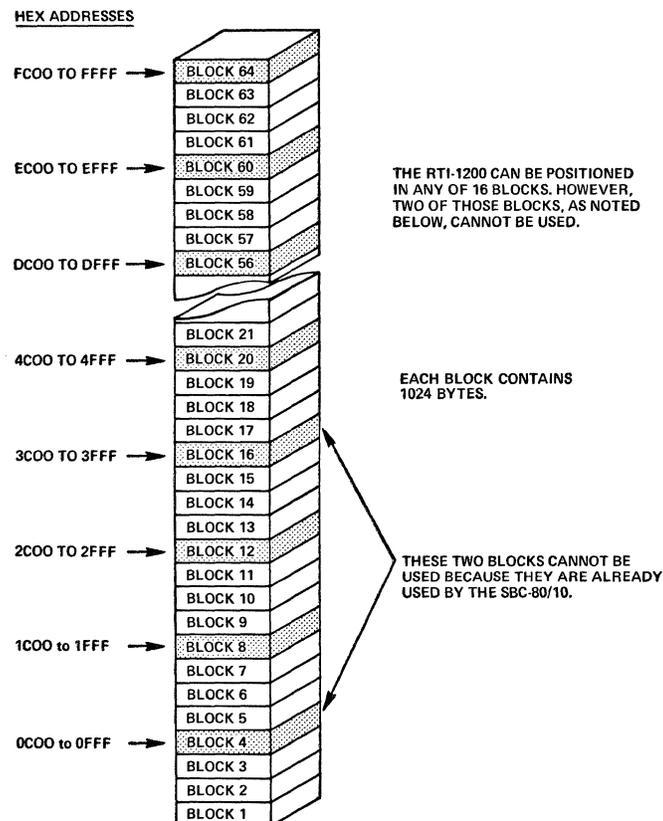


Figure 14. Positioning the RTI-1200 in the SBC-80/10's memory address space.

For example, one of the memory locations used by the RTI-1200 contains the address of the analog-input channel selected by the multiplexer. Stepping from one channel to the next can be accomplished with a single instruction that increments or decrements the contents of a memory location.

A diagram of the RTI-1200's location in memory space is shown in Figure 14. The RTI-1200 occupies a 1k (1024-byte) block, located at any of 14 positions selected by the user. The functions relating to the operation of the RTI-1200 reside in the top 16 locations, the remaining 1008 locations are reserved for use by a 1k programmable read-only memory (PROM) that a user may furnish (and plug in on-board). Such a PROM can be used simply to expand the computer's memory space independently of the RTI-1200's functions. More frequently, it can be used to store subroutines relating to the RTI-1200 (transducer linearizing, for example). This can be especially advantageous if more than one RTI-1200 is used with a single microcomputer.

Figure 15 shows a more-detailed functional view of the memory space utilized by the RTI-1200, and Figure 16, on the next page, is a bit-by-bit memory map. There are a few features of especial interest:

XFF0, the SETUP byte, is instructed as to whether or not the end of conversion will trigger an interrupt. It is also instructed as to which pacer clock will be used, and whether it will be used to trigger conversions or interrupts.

Bytes XFF5 and XFF4, and XFF7 and XFF6 write data into the two (optional) on-board d/a converters, in a "right-justified" 12-bit 2-byte format.

XFF8 provides a/d converter output, with 12-bit accuracy, but truncated to eight bits of resolution.

XFFE and XFFD provide the full 12-bit a/d converter output, in the right-justified 2-byte format.

Two bytes, XFF9 (Gain Select) and XFFA (MUX Address) can be either read or written into. This allows their condition to be determined when gain-ranging or automatically cycled MUX addressing is used.

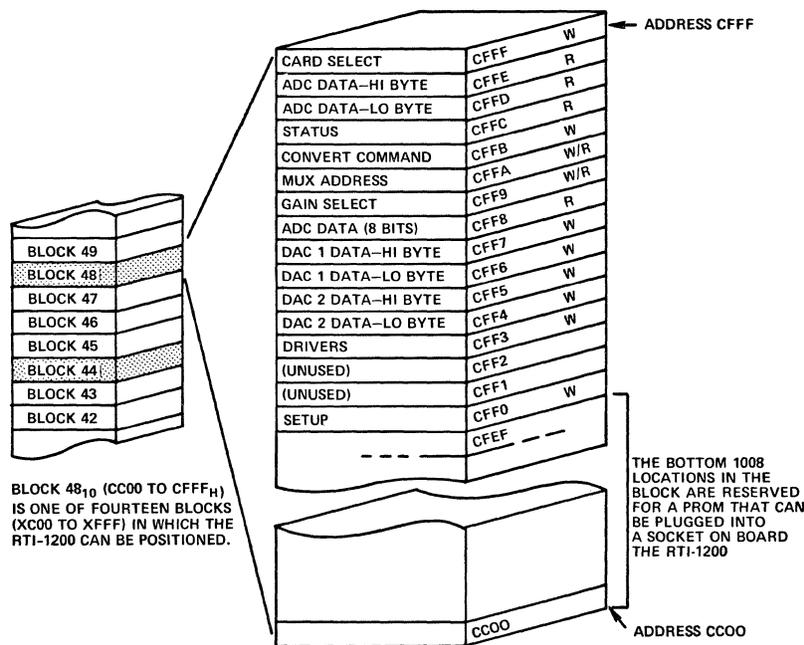


Figure 15. An expanded view of a memory block occupied by the RTI-1200.

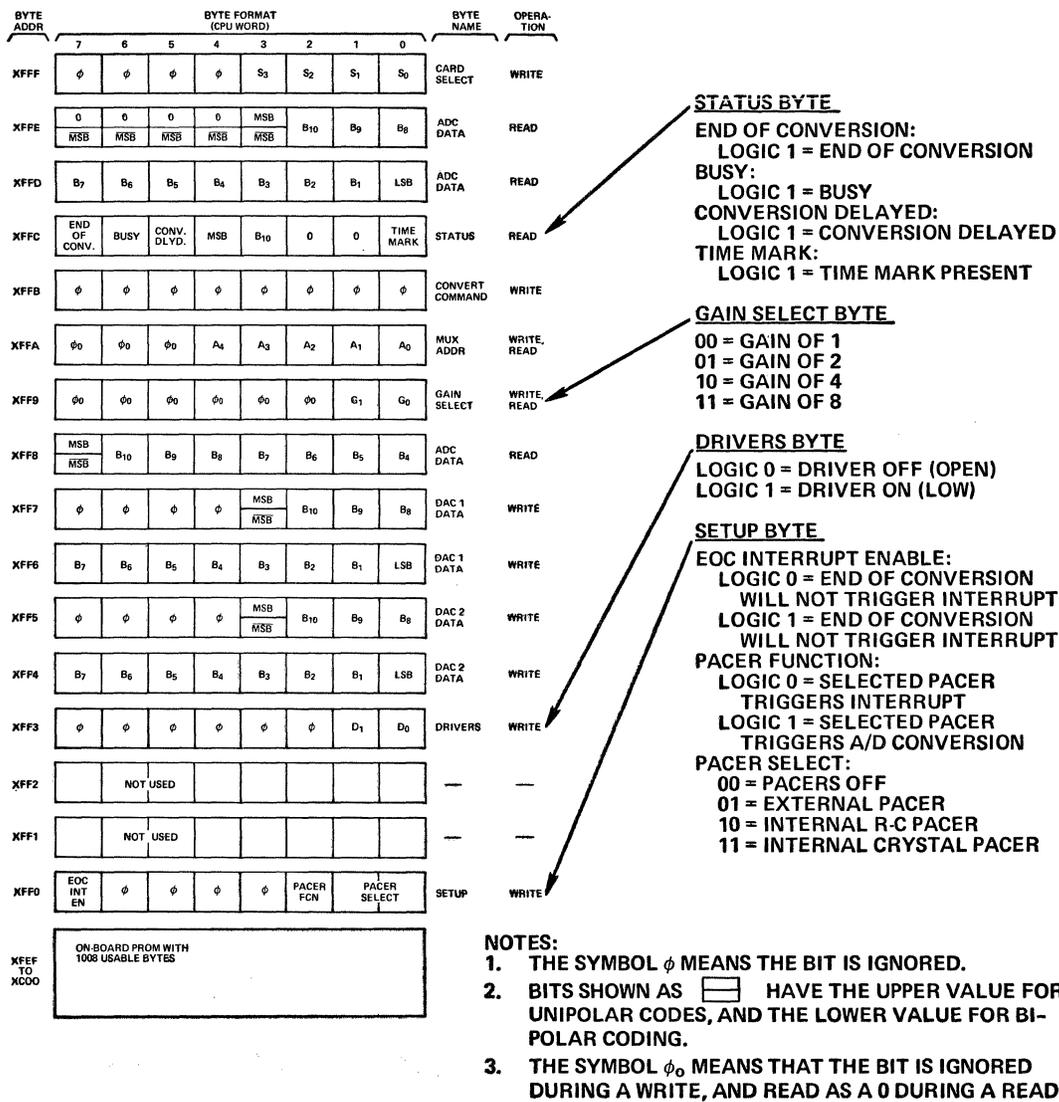


Figure 16. RTI-1200 memory map.

XFFF is a "card-select" (horizontal memory-mapped) byte. This feature permits a number of RTI-1200's to occupy the *same* block of memory interchangeably when addressed (Figure 17).

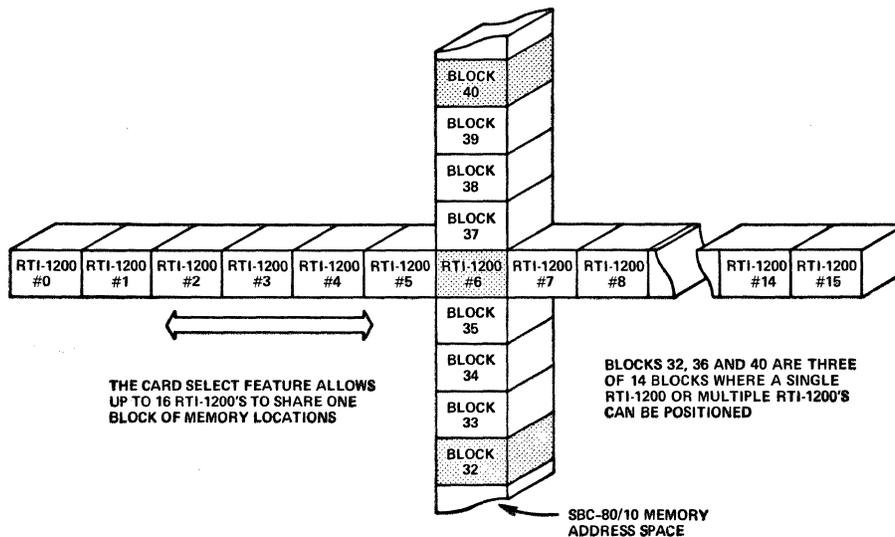


Figure 17. Vertical and horizontal memory-managed I/O as applied to the RTI-1200.

As an illustration of the simplifications afforded by memory-managed interfacing, combined with the advantages of on-board firmware, in the conception and writing of system software, here is the entire (8080 assembly language) program for acquiring a single reading from a single channel:

```

MVI      A,07H
STA      MUXADR      ; SELECT CHANNEL 07H
STA      CNVCMD      ; ISSUE CONVERT COMMAND
LOOP:    LDA      STATUS
RLC
JNC      LOOP        ; CHECK EOC BIT
LHLD     ADCLO       ; READ DATA
HLT

```

This program selects the desired analog channel (07), issues a CONVERT COMMAND, determines when the data is ready, and reads the data. At its conclusion, 12-bit data from the converter will be present in a two-byte register-pair. This program requires only that the desired gain has previously been selected (i.e., the desired data stored in the GAINSEL byte) and that the proper setup data had been written into the SETUP byte. In this case, the correct setup byte would be 00H (00, hexadecimal), which means that the pacers are turned off, and end-of-conversion will not trigger an interrupt.

3. SERIAL INTERFACING

We've shown some of the ways analog information can be handled in its translation to digital and in the interfacing of the digital information with a processor bus. This approach makes the most sense if the source of the analog information is electrically and physically *near* the processor. If, on the other hand, the data must be carried through an electrically noisy environment, and/or over distances greater than a few meters (a task which would become quite expensive for parallel data transmission, because of the high cost of wire and wiring, and the need for more driver power to deal with increased capacitance), immediate conversion to some form of digital or pulse transmission in two-wire serial form is strongly desirable.

V/F CONVERTERS

Perhaps the most-obvious approach is the use of a voltage-to-frequency converter, a device that produces a (usually asynchronous) output train of pulses or square-waves at a frequency proportional to the input voltage or current. V/f converters offer high resolution at low cost, in common with other integrating methods. A V/f converter can continuously track the input signal without the need for clock pulses, convert-command signals, or any form of external logic. The direct count of its output pulses, over a time period (Figure 18), can produce a binary or BCD digital number, which represents the average value of the input during the counting period.

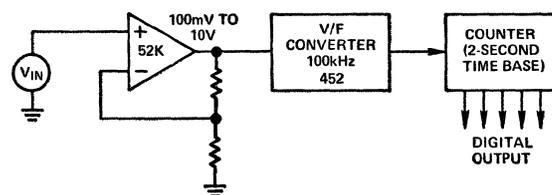


Figure 18. V/f converter used as a nearly 18-bit binary (5½BCD) A/D converter. Resolution is 1 pulse in 200,000, or 0.05% of smallest input signal (or 5ppm of full scale).

The VFC pulses require but a single wire-pair for transmission, unlike parallel converters, which—for n bits—require at least $n+1$ wires, or synchronous serial converters, which require a form of clock signal. The V/f converter may share a local power source with a transducer and may be optically coupled for high common-mode isolation (Figure 19).

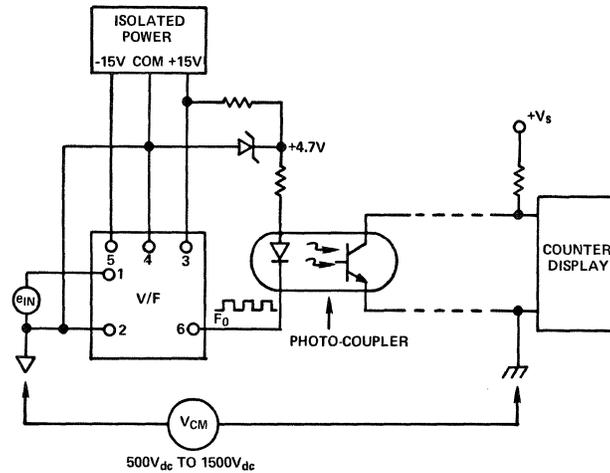
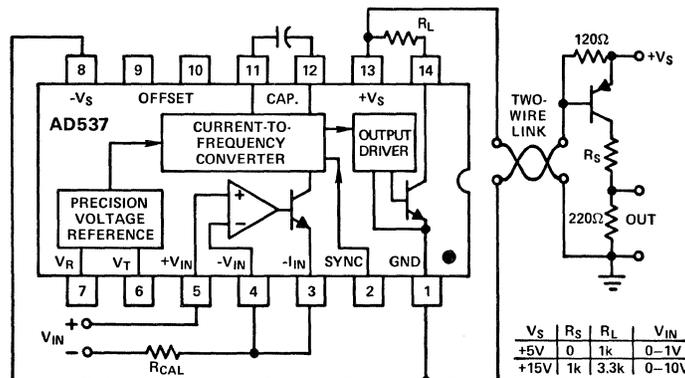


Figure 19. Optically-isolated A-D conversion.

Or a low-power-drain integrated-circuit V/f converter, such as the AD537, can use the two-wire link both to obtain its excitation voltage and to furnish an output-current pulse train, as Figure 20 shows. This avoids the need for local excitation. The current signal is converted to a DTL/TTL or CMOS-compatible signal by the single-transistor termination circuit shown. The excellent supply rejection, high output-drive capability, and square-wave output from the AD537, are all advantageous in this application.

The pulse trains from a number of AD537 VFC's may be multiplexed onto the same counter in random order by connecting their collectors together (sharing a single pullup resistor), and their emitters to the open collectors of a 1:N address decoder. Opening all gates but the one selected will cause its output pulse train to appear at the common collector terminal.

A scheme for building a *synchronous* V/f converter can be found in pages 83-85 of the *NONLINEAR CIRCUITS HANDBOOK*.* Synchronous VFC's produce pulses only when clocked, with a maximum rate related to the clock frequency. By a suitable interleaving of clock phases in relation to a master clock, synchronous VFC's can be multiplexed onto a single line.



THE AD537 CAN BE USED FOR TRUE TWO-WIRE OPERATION, AS SHOWN HERE. THE FREQUENCY INFORMATION IS TRANSMITTED AS A CURRENT SIGNAL ON THE SUPPLY LINE TO THE DEVICE. THE SIGNAL IS CONVERTED TO A DTL/TTL OR CMOS-COMPATIBLE SIGNAL BY THE SINGLE-TRANSISTOR-TERMINATION CIRCUIT SHOWN. THE EXCELLENT SUPPLY REJECTION, HIGH OUTPUT-DRIVE CAPABILITY AND SQUARE-WAVE OUTPUT FROM THE AD537 ARE ALL ADVANTAGEOUS IN THE APPLICATION.

Figure 20. VFC two-wire operation.

*NONLINEAR CIRCUITS HANDBOOK, Edited by D. H. Sheingold, Analog Devices, Inc., 1974 & 1976, P.O. Box 796 Norwood MA 02062, \$5.95.

current for the loop. The current flows through receivers, transmitters, teletype machines, etc., so long as the switches are closed. When any of the devices on the line causes a switch to open, the current stops flowing, and all receivers on the line detect the level change. If a switch opens and closes a number of times, it will transmit a coded message to all enabled receivers; and the code, when decoded, will provide whatever information it represents and will cause whatever subsequent actions are appropriate.

A character in the ASCII format used by SERDEX (Figure 23) consists of a START bit, followed by eight information bits (LSB first) in non-return-to-zero (NRZ) format, and 2 STOP bits. A START signal is given by turning the current off (0). When a START signal is received, the incoming bit stream is sampled at the center of each bit interval, until the character is completed. Since a maximum of 11 bits are involved in a character code, and synchronization is established by the START bit, extremely precise bit-timing is unnecessary. The eighth bit may be used as a parity bit. The STOP bits turn the current on, and it remains on until the next character arrives. Figure 23 shows some examples of ASCII codes used by SERDEX. Since SERDEX transmitters ignore the codes for alphabetic characters, they may be used on printouts to convey background information about the commands or measurements, including units of measurement. All SERDEX cards are pre-programmed (via changeable jumpers) for teletypewriter operation at 110 baud (1.76kHz clock rate). Other data-transfer rates up to 19.2k baud are available by jumpering.

EXAMPLES OF ASCII CHARACTER CODES:

CHARACTER	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1 (LSB)
0	1	0	1	1	0	0	0	0
1	1	0	1	1	0	0	0	1
2	1	0	1	1	0	0	1	0
3	1	0	1	1	0	0	1	1
4	1	0	1	1	0	1	0	0
5	1	0	1	1	0	1	0	1
6	1	0	1	1	0	1	1	0
7	1	0	1	1	0	1	1	1
8	1	0	1	1	1	0	0	0
9	1	0	1	1	1	0	0	1
!	1	0	1	0	0	0	0	1
\$	1	0	1	0	0	1	0	0
%	1	0	1	0	0	1	0	1
.	1	0	1	0	0	1	1	1
/	1	0	1	0	1	1	1	1
=	1	0	1	1	1	1	0	1
?	1	0	1	1	1	1	1	1
*	1	0	1	0	1	0	1	0
#	1	0	1	0	0	0	1	1

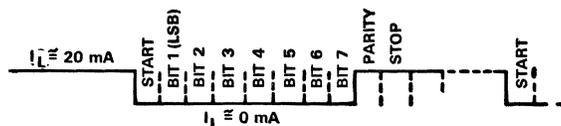


Figure 23. Typical ASCII coding and format.

When an STX serial transmitter receives a control character, an action or a series of actions is initiated. For example, when “%” is received, a pulse is initiated at the appropriate terminal. If a question mark is received (?), an a/d conversion is initiated. When the converter indicates that conversion has ended, the change of state of the *status* line causes the resulting digital data to be transmitted serially back to the control center. As the block diagram in Figure 24 indicates, up to 8 BCD digits can be sent, or up to 24 binary bits (if they are arranged in groups of three for transmission as octal digits). By the use of external shift registers, the STX2603’s word output can be expanded to transmit a string of characters of any desired length, including the outputs of additional a/d converters or such ASCII characters as plus- and minus-signs, decimal point, space, carriage return, and alphabetic characters.

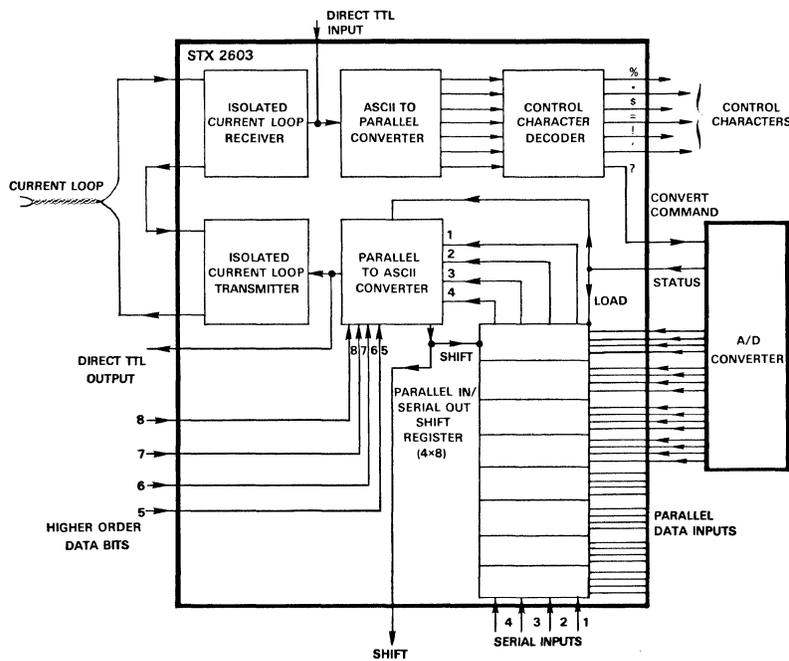


Figure 24. Block diagram of the STX2603 serial transmitter.

The serial output of the STX's parallel-loaded shift register (and any external extensions) is fed to the parallel-to-ASCII converter, where it is transmitted one-character-at-a-time to the teletypewriter of computer.

Figure 25 illustrates a possible application of the STX serial transmitter to control the liquid level in a tank from a teletypewriter. To determine the level in the tank, the operator might type

WHAT IS THE LEVEL IN THE TANK IN CENTIMETERS?

The STX2603 ignores all the alphabetic characters. When it receives the question mark (?), it initiates an a/d conversion and subsequently transmits the data back to the teletypewriter. The STX2603 can recognize and respond independently to 6 other control characters (?, *, \$, !, ', and =) that may be useful for controlling system components, e.g., activating a pump, then turning it off later. Thus, a check-and-fill dialogue might proceed as follows:

WHAT IS THE LEVEL IN THE TANK IN CENTIMETERS? 287

TURN THE FILL PUMP ON%

WHAT IS THE LEVEL IN THE TANK? 496

?575

?681

?760

TURN THE FILL PUMP OFF!

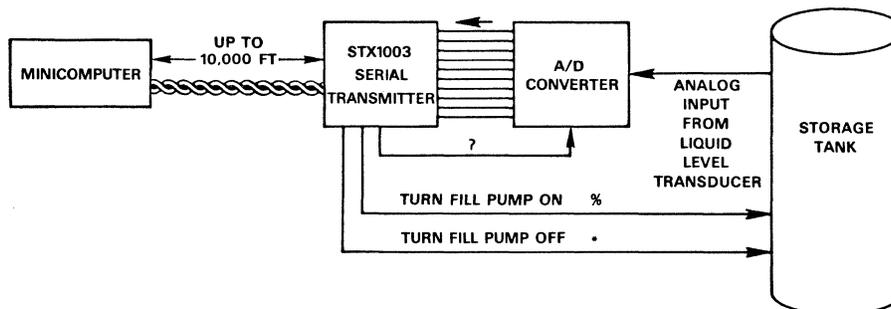


Figure 25. Application of the STX1003 Serial Transmitter.

In this manual system, the operator decides when the tank is sufficiently full and types the turn-off command. Clearly, no significant difficulty is encountered in replacing the teletypewriter with a computer having an asynchronous serial port and a high-level language capability, such as BASIC.

The SRX2605 Serial Receiver (Fig. 26) has a slightly different set of six control characters (% , ? , ! , ' , / , *) to which it responds by emitting a pulse at the proper pin. If it receives an equal sign (=), the internal register and *ready* flip-flop are cleared, and the data characters that follow enter the shift register. When a terminating dollar-sign is received (\$), the *ready* flip-flop is set, data is strobed into the d/a converter (and updates its analog output), and acceptance of additional data is inhibited until the next = arrives. A typical instruction might read

APPLY A NUMBER OF MILLIVOLTS = 3206\$

The alphabetic text is ignored. The equal sign (=) designates that data will follow; 3206 is the BCD number that programs the BCD-coded 4-digit d/a converter. and the \$, indicating end-of-data, strobes the data into the d/a input register.

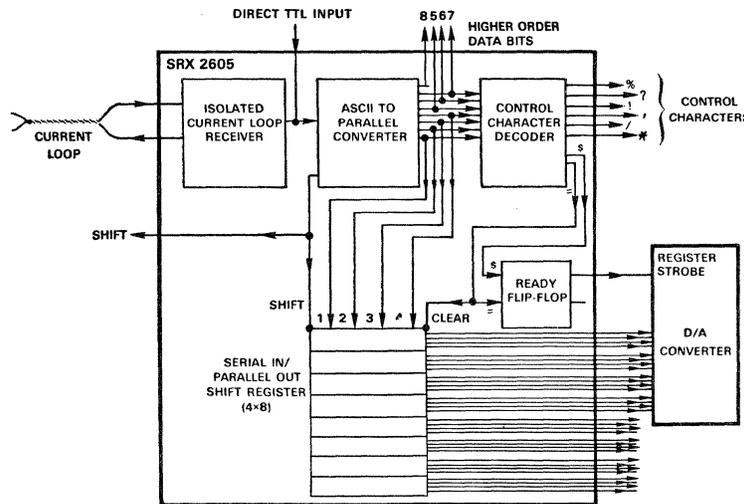


Figure 26. Block diagram of the SRX2605 serial receiver.

The SMX2607 multiplexer (Figure 27) is a bidirectional 8-channel multiplexer for implementing more-elaborate system. For up to 16 channels, an additional multiplexer is used. The first 8 channels (0 to 7) are addressed from the teletypewriter or computer by transmitting the number symbol, #, followed by a digit from 0 (channel 0) through 7; for the second set of 8 channels, # is followed by a letter from P through W, i.e., 8 through 15.

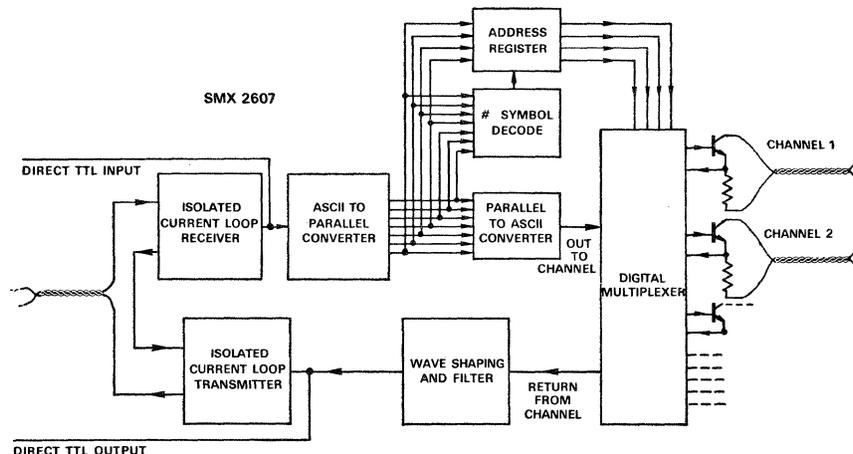


Figure 27. Block diagram of a SMX2607 multiplexer.

Multiple ranking of multiplexers permits communication with an unlimited number of channels. For example, in a dual-rank configuration ($8 \times 8 = 64$ channels), channel 3 of the first rank and channel 6 at the second rank would be addressed if the multiplexers received the characters #36.

Serial data received from the teletypewriter or computer is converted to parallel form, decoded to extract the number symbol and channel address, then converted back to serial data for transmission to the selected channel. Data returning from the remote channel is merely relayed back to the central control station.

Figures 28 through 32 show some additional system applications of SERDEX. Further applications in laboratory instrumentation can be found in AMERICAN LABORATORY, May, 1975. The use of SERDEX with a FIFO (first-in-first-out) serial buffer memory for collecting data in bursts and playing it back at a more-leisurely rate can be found in ANALOG DIALOGUE 8-2. The seminal article describing SERDEX appeared in ANALOG DIALOGUE 7-2. Finally, Figure 33, shows how data converted (and readable) at a remote location by an AD2008/B digital panel meter can be interfaced to a teletypewriter.

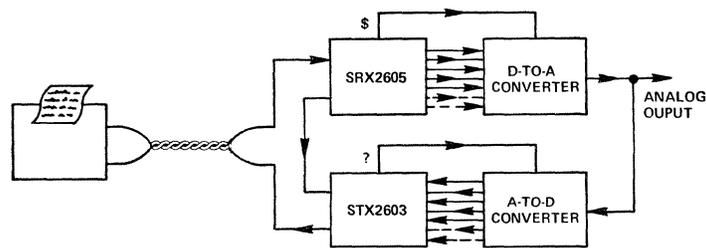
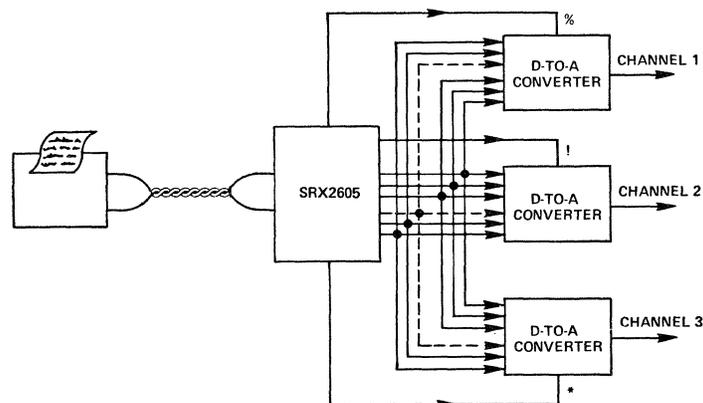


Figure 28. Verification of programmed analog output. An SRX2605 and an STX2603, operating on the same current loop, form a highly-reliable system. When a ? is typed, the D/A converter output is converted to digital and transmitted back to the teletypewriter.



*Figure 29. Self-multiplexed analog output. Several D/A converters are connected in parallel to one SRX2605. The %, !, or * strobes the input register of the desired D/A converter.*

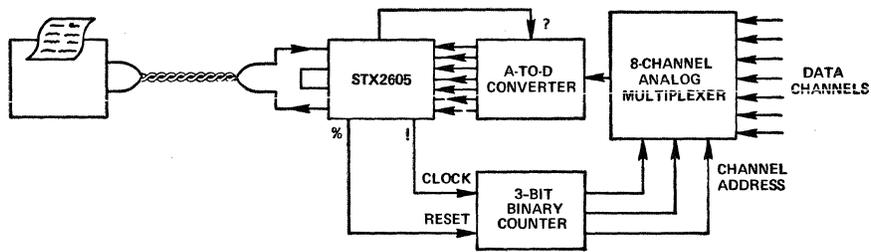


Figure 30. Teletypewriter or computer-controlled n-channel remote analog sequential channel addressing, using binary counter. ! Advances the counter, % resets to first channel, and ? initiates data transmission back to the teletypewriter.

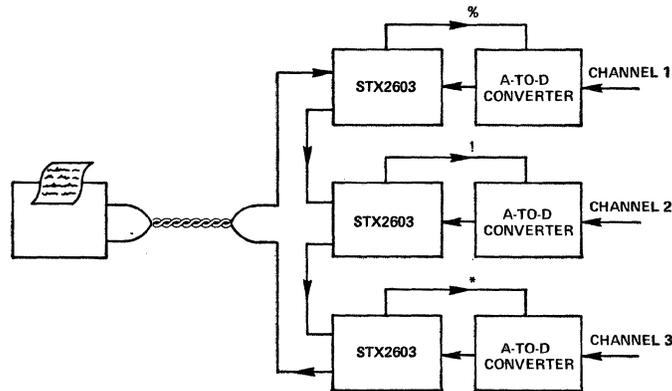


Figure 31. Many transmitters self-multiplexed on one series current loop. %, !, or * interrogates the respective channels and transmits the data to the teletypewriter.

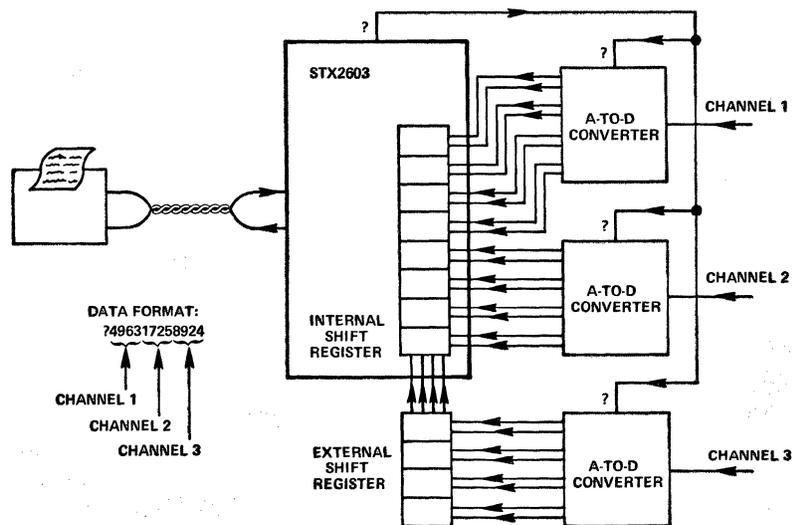


Figure 32. Using external shift register for simultaneous transmission of many channels with only one STX2603.

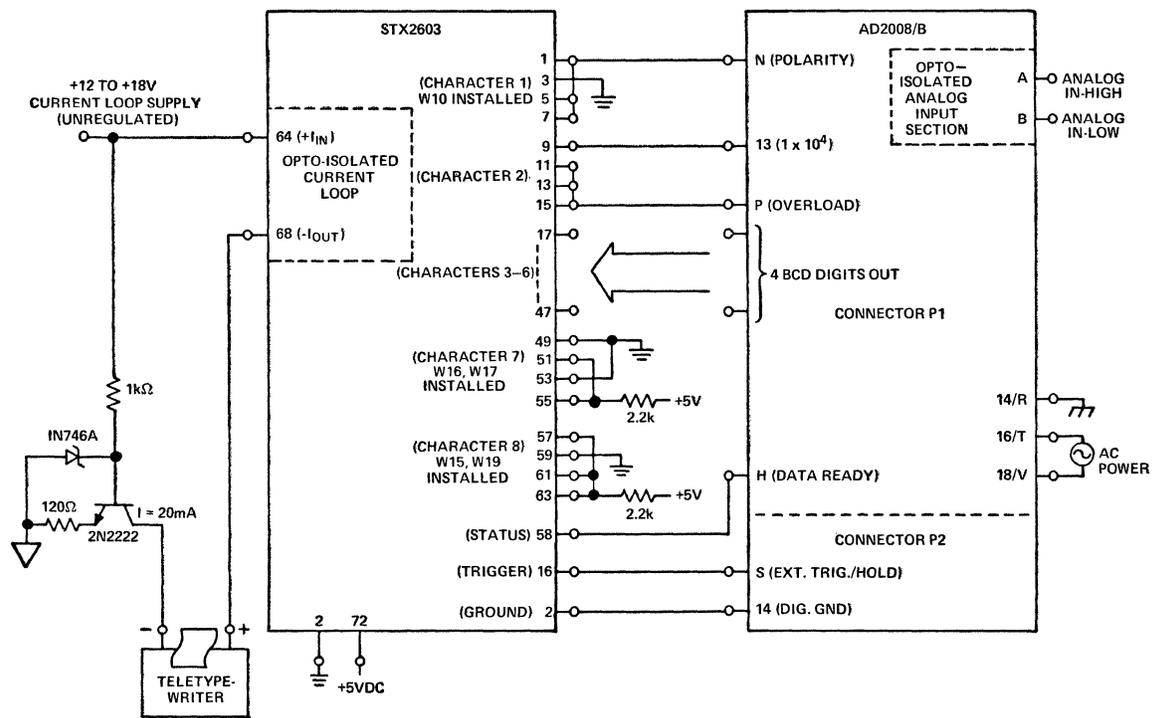
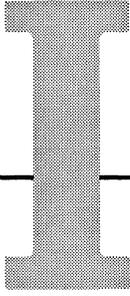


Figure 33. A digital panel meter AD2008/B is interfaced to a teletypewriter through an STX2603 Transmitter Card. Using this hookup, the DPM will convert upon receipt of a "?" typed on the teletypewriter, and transmit the data back after a conversion has been completed. The information will include polarity, overrange, overload, 4 BCD digits, line feed, and carriage return.

CONCLUSION

We have summarized in this chapter a variety of means of implementing converter-interface functions in terms of standard readily available products, at the various levels of system involvement that are likely to concern our readers. More information on any aspect of this discussion is no farther away than the nearest Analog Devices sales office.



Analog Functions With Digital Components

Chapter I-5

ANALOG FUNCTIONS WITH DIGITAL COMPONENTS

The “analog” world has numerous circuit tricks that occur time and again, employing op amps, multiplier/dividers, filters, phase shifters, function generators, etc. The term “analog” commonly has two meanings, *both of which* are intended here: “analog” in the sense of dealing with measurable quantities rather than abstract *digital* numbers, and “analog” in the sense of *continuous* (derivatives existing nearly everywhere), rather than *discontinuous* (quantized).

There have been a few excellent books on the applications of operational amplifiers, fewer on the applications of op amps and analog function modules, and virtually none on the use of digital components (converters, counters, shift registers, etc.) in the service of analog relationships.

There are many excellent auguries favoring an intimate, long, and happy marriage between the two families. Analog devices are cheap, plentiful, and capable of a great deal of functional versatility; digital devices are cheap, plentiful, and capable of a great deal of functional versatility. The reasons there has been little apparent intercourse between them are twofold: Interface devices, such as A/D and D/A converters have heretofore been too expensive to be wasted as components (remember the days of \$227 op amps and \$50 transistors?), and practitioners who volubly embrace the tricks of both trades are either extremely rare or remain well-hidden.

This chapter is in no sense intended as an encyclopedia (in either breadth or depth) of such connubial (i.e., “hybrid”) circuits; that volume is yet to be written. Rather, the few representative items included here are intended to be suggestive of what is possible, and to stimulate the reader to bring his creative faculties to bear on new ways of looking at problems that he may have conceived of as being strictly “analog” or “digital.” For those already laboring in the vineyard, there will be no revelations, but perhaps there is something a little new or different to make a scan worthwhile. The circuits are presented in the form of independent modular panels that stand alone (“bite-size morsels,” to aid digestion). The selected examples are:

SOURCES

- Digitally-Controlled Voltage Source

 - Manual Digital Inputs

 - Thumbwheel BCD switch

 - Toggle-switch register

- Digitally-Controlled Current Sources

 - “Current-output” DAC

 - Current gain: floating load

 - Current gain: buffered load

 - Current to grounded load

SCALE FACTORS AND MODULATIONS

- Digitally-Controlled Direct Gains
- Digitally-Controlled Inverse Gains
- High-Precision Analog Multiplication
- . . . or Division

FUNCTIONAL RELATIONSHIPS

- Analog Functions with Memory Devices
- Arbitrarily Programmable Functional Relationships
- Sinusoidal Input-Output Relationships

TRIGONOMETRIC APPLICATIONS

- Digital Phase Shifter
- Digital/Resolver Converter (Resolver Simulator)
- Resolver (Digital) Control Transformer

WAVEFORMS

- Sawtooth
- Triangular-Wave
- Sinusoidal

FUNCTIONS OF TIME

- Precision Analog Delay Line
- Tapped Delay Line
- Serial Delay Line
- Analog-to-Frequency Converter

DIGITAL SERVO DEVICES

- Tracking Sample-Hold (A/D Converter)
- Digital Pulse Stretcher
- Digital Peak-Follower (with Hysteresis)
- Automatic Zeroing Circuit

DIGITALLY-CONTROLLED VOLTAGE SOURCE

(or Precision Power Supply)

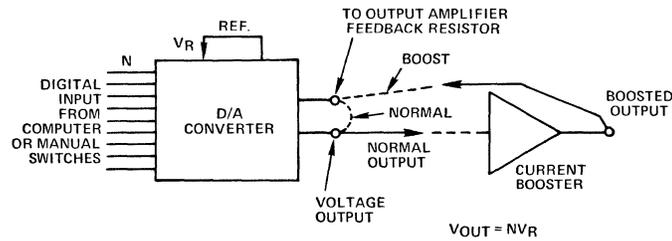
A well-calibrated D/A converter is probably the simplest available source of arbitrary precision voltages. Turn on the power, set the digital input, and expect (and receive) the voltage you asked for. With a 10-bit converter, resolution is 0.1%; with a 12-bit converter, 0.024%; and with a 16-bit converter, 0.0015% (15 ppm).

Let it be driven by a computer, and you have a ready supply of voltage for fast or slow automatic testing. Set it manually (with a "toggle-switch register," or with BCD thumb-wheel switches), and it's a convenient "volt-box," or a handy reference source. Or set it permanently by hard-wiring its logic inputs. No resistors or pots necessary!

If its output op amp doesn't have adequate output current, follow it with an inside-the-loop current booster. Feedback to the built-in amplifier-feedback-resistor will make the output virtually independent of the booster's dc characteristics. It can be followed with an op amp having higher-voltage output and precisely-set fixed gain, if high voltage is needed. Doing this outside the DAC's loop protects the converter's circuitry (including the low-voltage digital components) from accidental exposure to fault voltages.

Because the setting is done digitally with (e.g.) TTL logic levels, the voltage can be set from a distant location, or in the presence of a fair amount of electrical noise, relying on

the inherently-high noise immunity of digital signals (at the cost of additional wire for the parallel circuits). If noise pickup is not a major factor, it is interesting to note that in some cases the switches can be closed "passively," i.e., to the power-supply return for "0", left open for "1".* The double-buffered AD7522, with serial input, may permit remote voltage (or gain) settings, with minimal wiring, when appropriately pulsed.

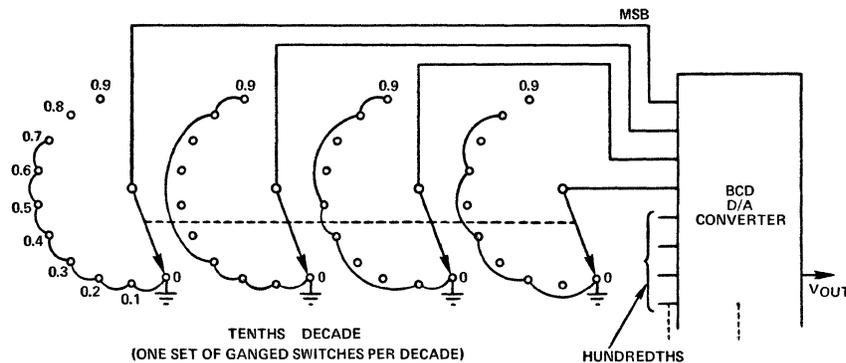


MANUAL DIGITAL INPUTS

All that is needed to obtain a given output voltage from a D/A converter is to close the appropriate switches. Human beings usually prefer base-10 numbers or BCD coding, despite the fact that it throws away inherent binary resolution at the rate of 2-bits-out-of-12 (12BCD = 1/1000, 10BIN = 1/1024).

Thumbwheel-switch Encoder

A thumbwheel-switch encoder is the simplest way for the operator, especially if he is mathematically unsophisticated, since the base-10 number can be set directly, and all the appropriate switches are automatically closed. A D/A converter with BCD coding should be used. The switch points that are "0" (positive true) are connected to ground; those that are "1" are either left open* or connected to +V_S (but be sure to use a break-before-make switch). The wiring for one decade of thumbwheel switchery is shown ("1" open). If the converter has *complementary BCD* coding, the complementary switch connections should be used.

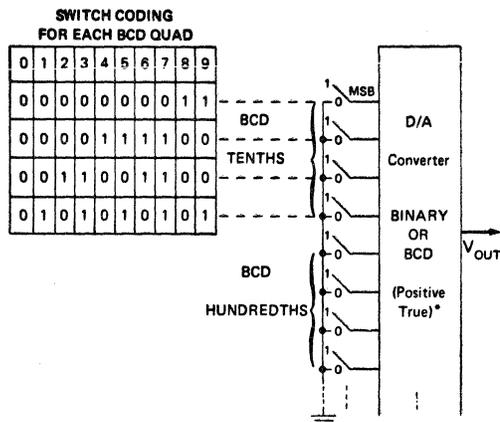


Toggle-Switch Register

The toggle-switch register is physically more elementary, and it may be used with either binary or BCD-coded DAC's. It does require some calculations, though, especially for binary settings. As an aid to calculation, two tables are given, one for BCD (the same code is used for each digit), and one for binary equivalents of representative decimal fractions of full scale. Interpolation is performed by adding or subtracting an appropriate set of terms (binary rules) to form the desired sum. Note that multiplication or division by 2 simply moves a number one place to the left or right: by 4, two places left or right, etc.

*TTL only.

TOGGLE-SWITCH REGISTER



*If converter operates with complementary logic, perform computations the same way, but use complementary switch settings.

For unipolar binary coding, the digits to the right of the “decimal” point form the code, MSB leftmost. For bipolar 2’s complement, divide the magnitude by two for the positive number, then complement all digits and add 1LSB for the negative number. For offset binary, complement the 2’s-complement MSB. (See Chapter 1, Part II, for a more-complete discussion of coding and conversion relationships in bipolar DAC’s.)

BINARY EQUIVALENTS OF DECIMAL FRACTIONS

	MSB				
0.8	0.1100	1100	1100	1101	0
0.5	0.1000	0000	0000	0000	0
0.4	0.0110	0110	0110	0110	1
0.25	0.0100	0000	0000	0000	0
0.2	0.0011	0011	0011	0011	0
0.125	0.0010	0000	0000	0000	0
0.1	0.0001	1001	1001	1001	1
0.08	0.0001	0100	0111	1010	1
0.0625	0.0001	0000	0000	0000	0
0.04	0.0000	1010	0011	1101	0
0.02	0.0000	0101	0001	1110	1
0.01	0.0000	0010	1000	1111	0
0.008	0.0000	0010	0000	1100	1
0.004	0.0000	0001	0000	0110	0
0.002	0.0000	0000	1000	0011	0
0.001	0.0000	0000	0100	0001	1
0.0008	0.0000	0000	0011	0100	1
0.0004	0.0000	0000	0001	1010	0
0.0002	0.0000	0000	0000	1101	0
0.0001	0.0000	0000	0000	0110	1

Converting Base-10 Number to Binary Switch Setting – 2 Examples (12-Bit Conversion)

1. +0.9FS (Note: 0.9 = 0.5 + 0.4)

0.5	0.1000	0000	0000
+0.4	+0.0110	0110	0110
0.9	0.1110	0110	0110

Code: 1110 0110 0110, Straight Binary

2. -0.6FS, 2’s Complement (Note: 0.6 = 0.4 + 0.2)

0.4	0.0110	0110	0110
0.2	+0.0011	0011	0011
0.6	0.1001	1001	1001

Code: 1001 1001 1001, Straight Binary

X ½ 0100 1100 1100 Scale Expansion

Compl. 1011 0011 0011 One’s Complement

+1 LSB 1011 0011 0100, Two’s Complement

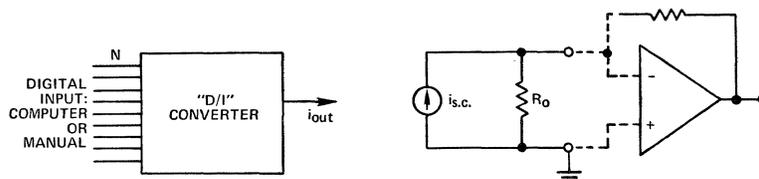
DIGITALLY-CONTROLLED CURRENT SOURCES

Many analog current sources have been developed with the variations that provide such diverse advantages as low cost, simplicity, ability to ground the load, etc. In conventional all-analog circuits, the original controlling input is derived typically from a precision potentiometer, zener diode, or other reference. However, availability of versatile D/A converters now permits convenient digital control of current values, making, for example, programmable current supplies an inexpensive reality. As with voltage sources, the adjustments may be performed by either a computer or a human operator. These are a representative few among the many ways of accomplishing current drive.

“Current-Output” DAC

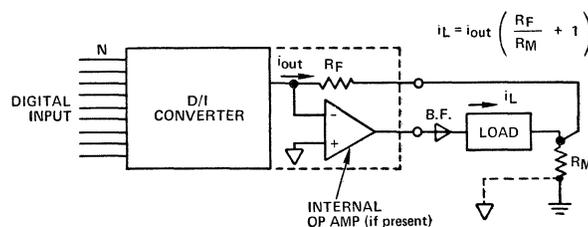
This would appear to be the simplest form of digital-to-current output source. However, it is unsatisfactory, because, except for devices such as the AD561, it generally has appreciable internal admittance “looking back,” and this admittance (and the load) must be included in computations of the share of current reaching the load. For this reason, the principal application of the current-output DAC is to drive inverting-operational-amplifier input terminals, which are normally at zero potential and thus impose negligible loading error. The AD561, however, may be treated as a true current source (Chapter II-2).

The output resistance of these DAC’s is often introduced by the resistive dividers used for attenuation of less-significant-bit currents (as is explained in Chapter 3, Part II). It is feasible, for applications in which a restricted number of discrete values of current (say 16) are required, to construct highly-precise fast current-output converters with high internal resistance, using quad current switches (*ibid.*) without attenuators.



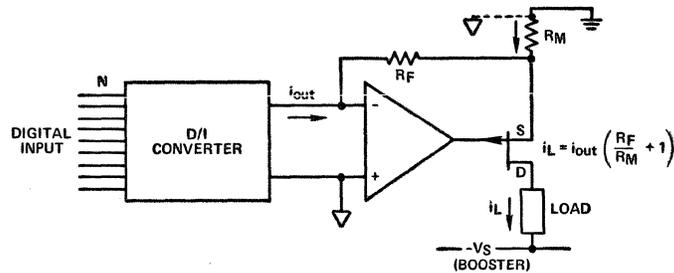
Current Gain – Floating Load

In this application, a load that has both terminals available is connected between the amplifier output terminal and the return lead of the feedback resistor. The attenuation introduced by R_M , if used, produces current gain. If the amplifier’s output current is inadequate, a booster may be used, inside the loop (B.F.). For large currents, a separate booster supply should be used, with only the R_M pickoff point connected to the converter’s analog ground.



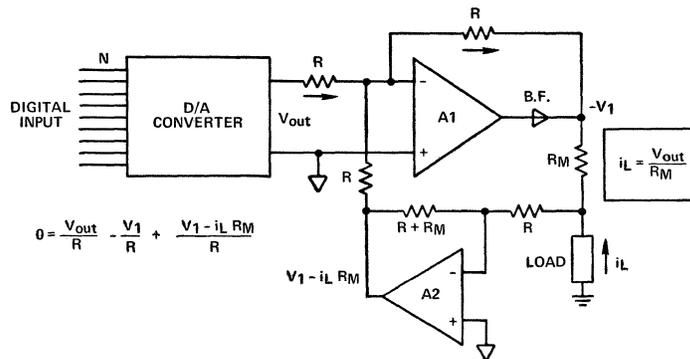
Current Gain – Buffered Load

For applications in which the amplifier’s output range imposes serious restrictions on the kind of load that might be driven, a transistor with the load in its collector (or drain, in the case of FET’s) allows a wide range of voltage swing across the load. Examples of loads that might be driven in this manner are CRT deflection coils, motor windings, chart-recorder pen drives, etc.



Current to Grounded Load

There are a number of ways of driving current to a grounded load, all of which employ both positive and negative feedback to measure and control the current. One example, using a voltage source and two operational amplifiers, is shown here. Amplifier A1 measures the difference voltage across R_M (direct from the top and inverted from the bottom via A2) and sets it equal to the DAC's V_{out} , thus forcing a current V_{out}/R_M through the load. In the general case, the resistor ratios can be adjusted for scaling, the drive could be from a current source, boosters could be used (at point "BF") etc. As with all operational-amplifier circuits having complicated (or even simple) dynamics, attention should be paid to dynamic stability: feedback capacitors may not be as helpful as capacitance shunting the load.



DIGITALLY-CONTROLLED SCALE FACTORS

A D/A converter that accepts variable references (i.e., a *multiplying* DAC) can be thought of as a digitally-controlled potentiometer. As such, it can be used for setting gains, either by a computer or a human operator. Computer-setting might be used, for example, in adaptive control systems; manual setting might be employed where the device being controlled is remote (think of it as a potentiometer with a long shaft).

The multiplying D/A converter can also be thought of as a means of modulating a computer output by an analog signal. For example, if the computer is developing a square wave, the analog signal might be amplitude-modulating it.

The simplest device operates in one quadrant, with either a positive or a negative analog signal and straight binary or BCD coding.

For two-quadrant operations, there are two modes: bipolar analog and bipolar digital. Bipolar analog operation simply requires a bipolar analog input and straight binary or BCD digital coding. It also requires a converter that can accept analog signals of either polarity. Such DAC's as the DAC1125 and AD7520, that use voltage switching and R-2R ladder networks, are capable of this form of operation; current-source DAC's are usually unipolar, though the devices employing monolithic Craven-cell switches, such as the AD561 and AD562 will accept a wide signal range without appreciable degradation of linearity.

Bipolar digital operation can involve offset-binary (or 2's complement) coding, with an inverted version of the analog input applied to the offset reference terminal, or to one

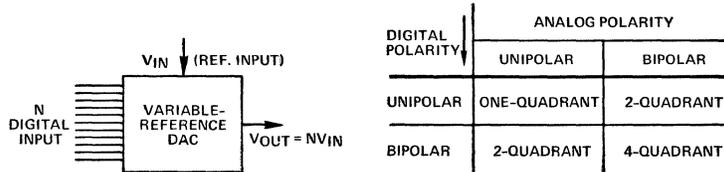
end of an R-2R ladder network; or sign-magnitude coding (unipolar DAC), with the sign bit switching the output polarity.

Four-quadrant operation involves a combination of circumstances: a DAC that can respond to both bipolar analog and bipolar digital inputs in the correct polarity, with appropriate speed and feedthrough performance. "Feedthrough" is the analog output signal that appears when the digital input is calling for zero gain.

Shown here are four ways (among many) that digital gain control can be used to perform useful functions.

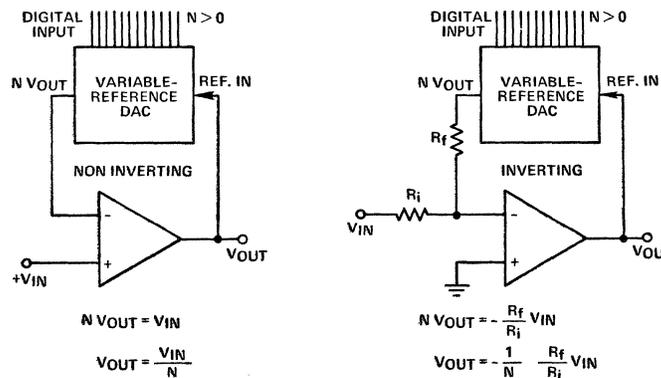
Direct Scale Factor

This circuit provides simple digital scale adjustment, proportional to the digital number. As noted, the digital number can be applied either by a computer signal, or manually.



Inverse Scale Factor

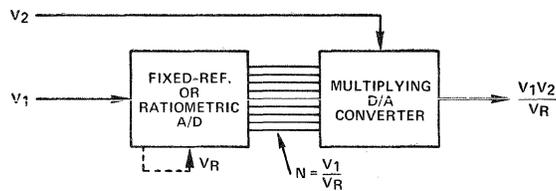
With the DAC in the feedback loop of an operational amplifier, the gain is inversely-proportional to the digital number. As a follower, all gains must be greater than unity, since even full feedback is 1LSB less than unity gain. As an inverter, the resistor ratio can be chosen for attenuation, so that normalized unity gain can occur at a mid-scale value (if $R_f/R_i = 0.1$, nominal minimum gain is 0.1 ($N = F.S.$), and unity gain is at $N=0.1$). But noise-and-error-gain will be $\cong 1/N$. The rules of feedback call for unipolar (positive) feedback gains only (signal may be bipolar).



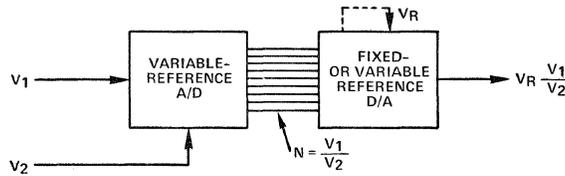
High-Precision Analog Multiplication

Since a 12-bit multiplying DAC develops accuracies to within considerably better than 0.1%, it is possible to make an analog multiplier having excellent accuracy by converting one of the inputs to digital form and using it to control the gain of a multiplying DAC. If the ADC is ratiometric, the output is a function of three variable. (V_R should always be larger than V_1 , or else overrange indication will be necessary).

Since an A/D converter digitizes the ratio of the "input" to the "reference", a D/A converter will convert the ratio back to a voltage. Again, if the D/A is a multiplying type, the output is a function of three variables. For both of these applications, the A/D may be connected for free-running operation, and either the A/D or the D/A should have a register to buffer the D/A from the conversion process and store the previous value.



... or Division



FUNCTIONAL RELATIONSHIPS

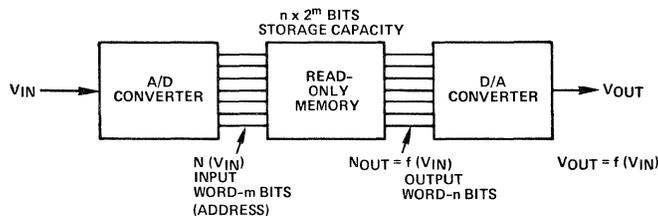
The term “functional relationship” implies a black-box operation, linear or nonlinear, $y = f(x)$, f being any single-valued realizable function. It is distinguished from a “function generator,” which implies a *time function* (i.e., in a function generator, $y = f(t)$). By applying a linearly-increasing function of time to a device having a given functional relationship, one can create a function generator.

In analog circuitry, functions are traditionally embodied in three ways:*

1. Using a natural function (e.g., the inherently logarithmic diode characteristic for log and antilog circuitry, the transconductance relationships of transistors for transconductance multipliers, the ability of a capacitor to store charge for integration).
2. Using diode-resistor networks to form piecewise-linear approximations to a nonlinear function.
3. Using combinations of natural functions to approximate arbitrary relationships, for example, power series using multipliers to generate the x^2 , x^3 , x^4 , etc., terms.

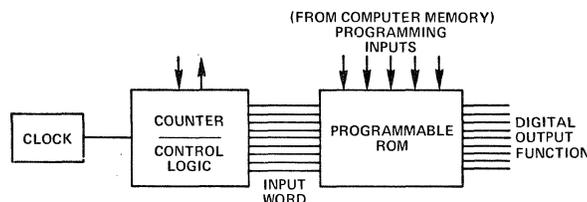
Now that converters and memories are available at low cost, a fourth approach becomes feasible:

4. Using memories (e.g., ROM's singly or in groups) to store a function digitally, and converting-in and -out with A/D's and D/A's, as shown in the illustration. Typical applications already in growing use are trigonometric transformations and thermocouple compensators.



Arbitrarily-Programmable Functional Relationships

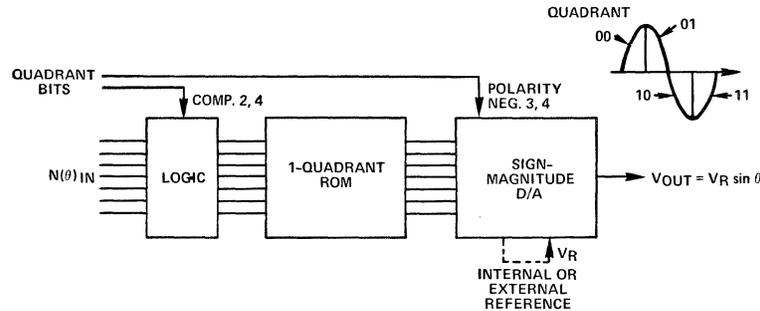
Besides standard functions that can be purchased in ROM's, it is also possible to buy programmable read-only memories, that can be programmed by the purchaser to simulate functional relationships.



*Nonlinear Circuits Handbook, Analog Devices, Inc., 1974 & 1976, has many details of these methods. \$5.95, P.O. Box 796, Norwood MA 02062.

Sinusoidal Input-Output Relationships

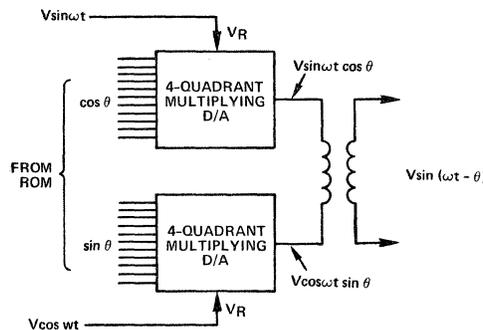
An example of the approach is the use of a read-only memory that has the values of $\sin\theta$ stored in it for $0^\circ \leq \theta \leq 90^\circ$. Two additional digits provide quadrant information, one to complement the input in the even-numbered quadrants, the other to provide the output sign-change for the 3rd and 4th quadrants. The input arrives from an angle-to-digital transducer, the corresponding sinusoidal number values are developed and applied to a D/A converter, and it makes the sine function available as a voltage. If the D/A converter is a multiplying type, computations of the form $R\sin\phi$ are readily performed.



TRIGONOMETRIC APPLICATIONS

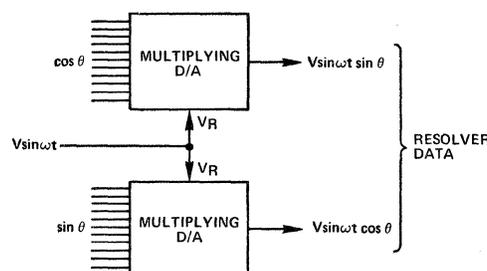
Digital Phase Shifter

The Figure shows two multiplying D/A converters used as digitally-controlled attenuators multiplying the reference signals $V \sin\omega t$ and $V \cos\omega t$ by the vector component of θ . The summed output from the two converters is then the vector $V \sin(\omega t + \theta)$, where the phase angle θ is set by the converter's digital inputs.



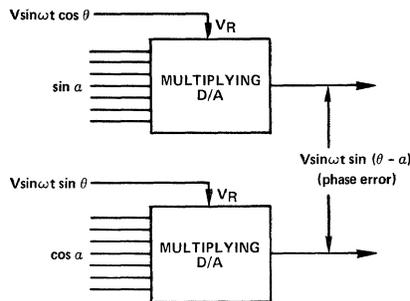
Digital/Resolver Converter (Resolver Simulator)

Similar to the above configuration, but having the common reference input to both multipliers, $V \sin \omega t$, this configuration obtains the two components, $V \sin \omega t \sin \theta$ and $V \sin \omega t \cos \theta$, which express resolver data for angle θ . The resolver data can be converted into synchro format with a Scott-T transformer, or an equivalent network in which operational amplifiers provide the appropriate voltage ratios. This resolver simulator can be enclosed within a feedback loop to operate as a resolver-to-digital converter.



Resolver (Digital) Control Transformer

Using the *actual* resolver line voltages $V \sin \omega t \sin \theta$ and $V \sin \omega t \cos \theta$ as the converter reference inputs, and multiplying by digital equivalents to $\cos \alpha$ and $\sin \alpha$, an output proportional to the angular error, $\theta - \alpha$ (for small angular errors) is developed. Operated in this mode, the configuration simulates a resolver control transformer.

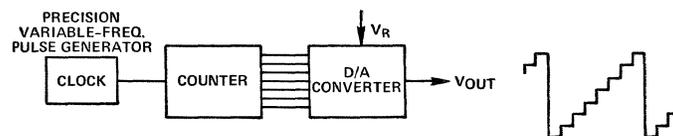


WAVEFORM GENERATION

Linear waveforms are generated digitally by clocks and counters, processed by ROM's or μP 's to obtain arbitrary shapes, and converted to analog functions of time by DAC's¹. As long as the original digital function can be created, then an analog output can be made to follow (within its speed limitations). The ease of manipulation and ability to lock timing operations to precise clocks give the digital approach considerable edge in versatility over many analog alternatives. Deglitching and filtering may be used as (and if) necessary to clean up the waveforms. Arbitrary counts and very-simple DAC's may be used to obtain pulse trains of few-step staircases of arbitrary duty cycle.

Sawtooth Generator

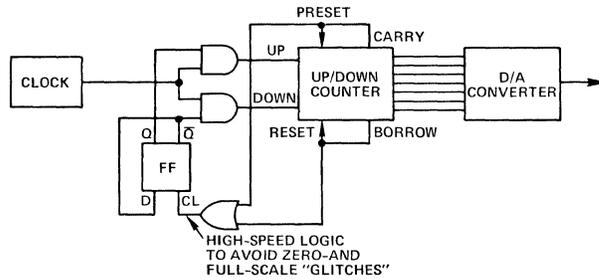
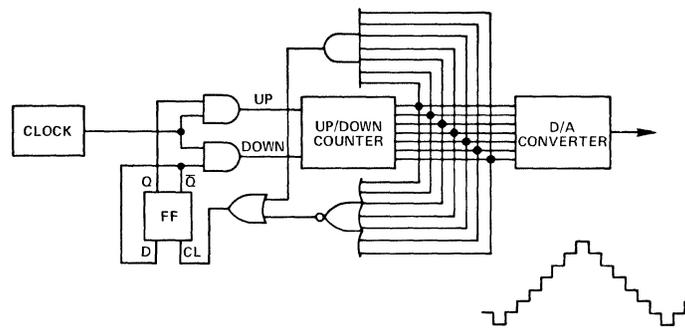
This sweep generator is composed of a digital clock, a counter, and a DAC. The clock pulses increment the counter, and the sequential counter steps increment the DAC output. After the counter is full, it returns to its empty state and starts counting again. Both amplitude and period of the sweep generator are easily and precisely adjustable. The resolution is determined by the number of counts and choice of D/A converter, ranging from the 16-bit DAC1136, with its 65,536 steps, down to 10- or fewer-bit converters with 1,024 steps, and below.



Triangular-Wave Generator

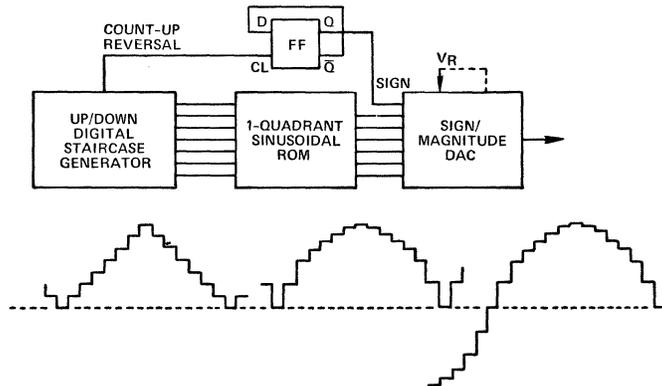
Instead of being allowed to overflow, the counter in this case is an up-down counter that is caused to change direction when it is full and again when it is empty. Two approaches to reversing direction are shown. In one, the reversal is generated during the full (and empty) states; in the other, it is generated by the carry (borrow) occurring at the leading edge of the next pulse. The result, at the DAC output, is essentially a triangular-wave of precise amplitude and frequency. With little additional logic, full-scale dwell (or dwell-and-reversal at any level) provides trapezoidal waveforms.

¹See also Chapter I-6, section B.



Sine-Wave Generator

If the digital count is fed to a sinusoidal ROM, and its output, accompanied by polarity information, is applied to a sine-magnitude-coded DAC, the output of the DAC will be an n-bit quantized sine wave. Its frequency is determined by the clock, and its amplitude can be controlled externally or by the use of a multiplying DAC.



TIME FUNCTIONS

The ability of flip-flops to store information, undegraded by time, and the continually decreasing cost of storage capacity, are strong motivations to seek ways of eliminating capacitor circuits, with their leakage, dielectric hysteresis, and nonlinearity. “Distortionless” time delay, integration, and sample-and-hold are a few targets for such effort.

Precision Analog Delay Line

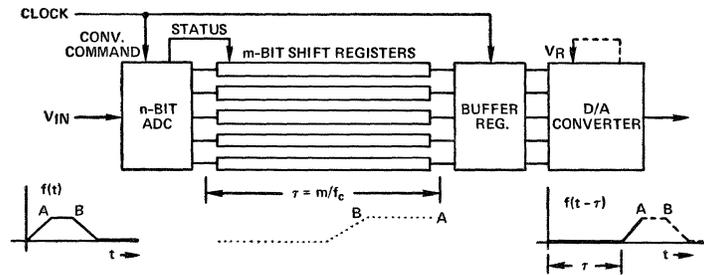
There are interesting applications for good analog delay lines: analog correlation, “distortionless” signal compression or expansion (i.e., “riding the gain” without missing a drumbeat), electronic echo-chamber effects, analog modeling of processes that incorporate pure time delay² for predictive control, design of filters with arbitrary transfer functions, are a few.

But there hadn’t been a decent way of building a practical analog time-delay device that is variable over microseconds to minutes to months, until shift registers became available with many bits at low cost-per-bit. Microprocessors can also perform such functions.

²See also Chapter I-6, section B.

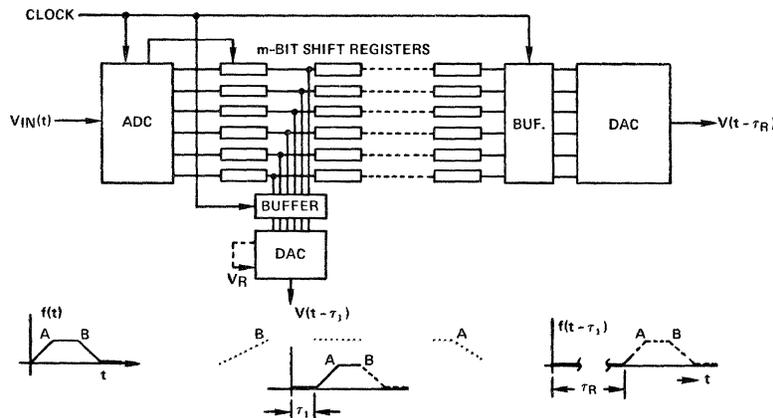
Active or passive filter-type delay lines were seldom “distortionless,” analog “bucket brigades” had excessive leakage errors at low speeds, as well as a resolution-vs.-cost problem (this latter being solved by the new charge-coupled MOS high-speed bucket brigades), tape recording wasn’t efficacious at high speeds, and the use of mainframe memory was too expensive (and bulky for portable instruments).

In the example shown, the delay is produced by shift registers (e.g., 256-bit) for n parallel digital channels, each channel representing 1 bit of converted analog signal. For 10-bit conversion, and 10 delay lines, signals that can be quantized into 1024 discrete levels can be delayed with a resolution of $1/256$ of the delay time (e.g., $1\mu\text{s}$ of $256\mu\text{s}$, $1/16\text{s}$, 1.38° per cycle of a sinusoidal ac signal of period equal to the delay time, etc.).



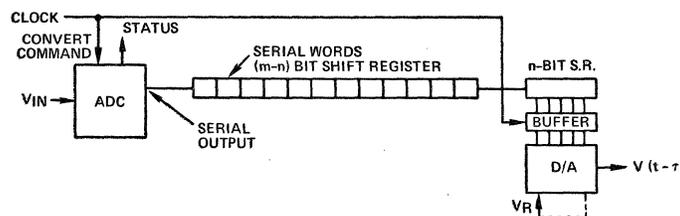
Tapped Delay Line

This device makes a number of points in the history of a waveform available simultaneously. It is simply the delay line with an increased number of discrete “chunks” of delay, and readout via DAC’s at each point. Multiplying DAC’s allow such interesting functions as $f(t) \cdot f(t-\tau)$ to be computed for a variety of values of τ .



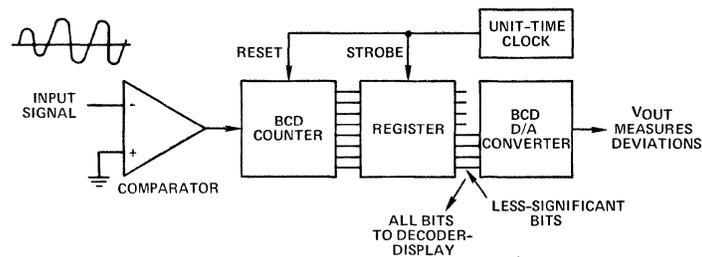
Serial Delay Line

For signals that do not require sampling at top speed, a considerable saving of the cost of delay lines (or increase in the time-resolution of the delay) can be achieved by feeding the converted signal into the line serially, and converting back to parallel information before the D/A conversion. Since the signal is being clocked through the line, a bit-at-a-time, few if any additional bits of shift register capacity are needed.



Precision Average-Frequency-to-Voltage Converter

In this application, the output of a frequency-or analog-event-meter (e.g., 16 bits) is applied to the usual BCD readout. In addition, the 8 (or more) least-significant bits are converted to voltage, providing a very sensitive analog measure of small frequency changes. It is feasible to also convert the top 8 bits, and use a low-cost analog divider, such as the AD534, to get a continuous analog readout of the fractional deviation.

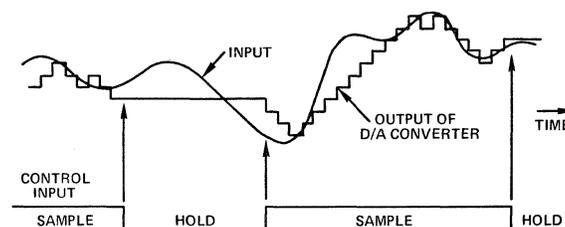
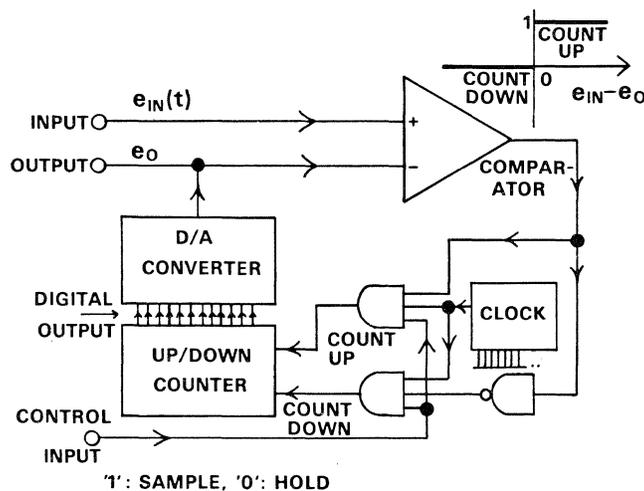


DIGITAL SERVO CIRCUIT

Most A/D converter designs involve feedback. Thus the very means of conversion implies that the combination of analog-digital interaction and the power of feedback can yield quite valuable results. A few examples are sample-and-hold, peak-detecting, and automatic zero-setting.

Tracking Sample-and-Hold (A/D Converter)

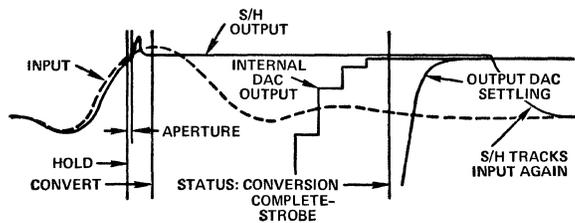
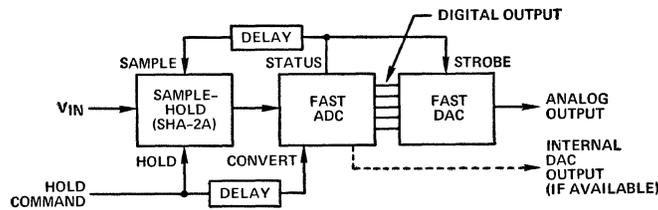
This circuit, also mentioned in the chapter on sample-and-holds, is especially useful as a track-and-infinite-hold device. It can acquire the analog signal within a minimum of 1 count and maximum of 2^n counts, and, upon command, *hold* it indefinitely without degradation, providing both digital and analog readout. Since it uses an up-down counter, it will track the analog signal at a constant rate (2^{-n} FS per count), and “hunt” between the two digital values that straddle the analog value, if it remains constant.



For slowly-varying analog signals, the tracking sample-hold is one of the lowest-cost ways to convert, since it eliminates the need for a sample-hold. However, its conversion time is variable, which introduces timing errors in sampled-data systems, since the most-recently acquired value may represent any value of signal during the interval between interrogations. Also, its response depends to a great extent on the amount and type of noise present.

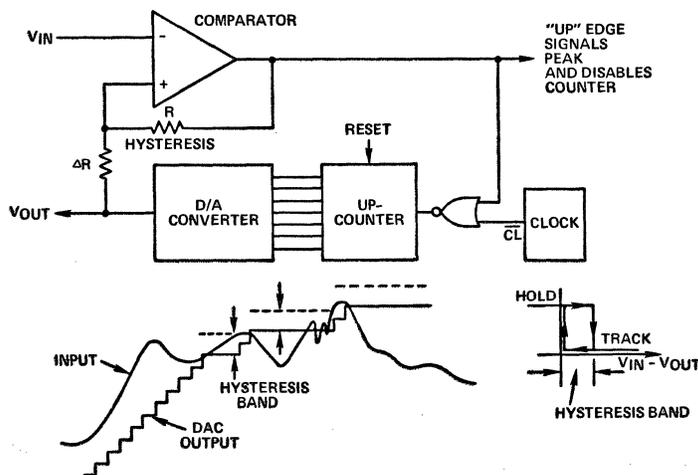
Digital Pulse Stretcher

For extremely-fast acquisition-very-long hold, this circuit, consisting of a fast sample-hold and a fast successive-approximations A/D converter will provide the best results. Both analog and digital outputs are available. If the internal D/A converter's output can be made available without slowing conversion, the output D/A shown in the Figure is unnecessary. The SHA-2A is kept in *sample* at all times except during conversion. When switched to *hold*, it should have a "head start" of about 100ns for its transients to die down before conversion starts. But aperture time is 10ns with 0.25ns jitter.



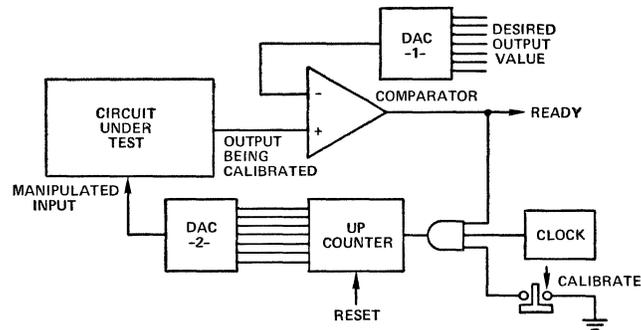
Digital Peak-Follower (with Hysteresis)

Similar to the tracking sample-hold, but using an up-counter (a valley-follower would use a down-counter), this circuit will *hold* the highest value of input that it has been able to track. However, to provide a small measure of immunity to noise, hysteresis makes the circuit insensitive to small changes; in order for the input to be followed, it must be higher than the stored value by a preset amount. A similar circuit can be used for valley following, and two such circuits with an output subtractor will provide peak-to-peak measurement.



Automatic Set-Point Circuit

If a circuit under test is to be calibrated from time to time (e.g., each time some element, perhaps a device under test, is changed), the resetting and the level to which a test value must be reset, may be adjusted digitally. In the example, an output of the circuit must be set to a value equal to a calibrating value set by DAC-1. The values are compared, and a clock increments a counter, which updates a DAC, setting the input that performs the calibrating adjustment. When the comparator changes sign, calibration is complete, and the sign change indicates a “Ready” condition. The calibration value is retained until a new calibration cycle is initiated by resetting the counter and gating the clock.

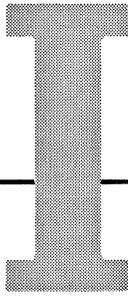


A FINAL NOTE:

SOFTWARE vs. HARDWARE

The examples given here all involve hard-wired analog-digital circuitry. For applications in which microprocessors are available, it should be evident that functions involving memory, control logic, and digital data can often be as well (if not quite as speedily) handled through the writing of appropriate microprocessor programs.

Rather than viewing the techniques as competitive, the designer should consider that the three-way tradeoff between analog, hard-wired, and software approaches provides at least one more degree of freedom for developing cost-effective instruments, apparatus, and systems. The flexible designer will not arbitrarily exclude a given approach; on the other hand, the committed designer should know that other alternatives to his own predilections do exist and may, on occasion, prove available to save the day.



Applications of Converter Systems

Chapter I-6

APPLICATIONS OF CONVERTER SYSTEMS

- A. AUTOMATIC TESTING
- B. COMMUNICATIONS AND SIGNAL ANALYSIS
- C. DISPLAYS
- D. COMMERCE, INDUSTRY, AND ELSEWHERE

Chapters I-5 have introduced the basic hardware elements of systems and equipment that involve converters, shown the basic configurations of data-acquisition and data-distribution systems, and indicated a few examples of the uses of digital and analog elements in intimate combination.

This chapter will illustrate the scope and breadth of systems and equipment that have been conceived of or built involving converters. The examples are drawn from a variety of sources, but they share the ideas, hardware, and circuit structures that have already been touched upon.

The intent is to inform the reader of what has been done, to suggest what can be done, and to arouse thoughts of what *might* be done by adding the conceptual tools described in this volume to the fund of knowledge and experience that he already possesses pertaining to his own field of endeavor.

A. AUTOMATIC TESTING

“Automatic testing of electronic devices has been a major factor not only in the overall improvement of product quality and reliability, but also in the dramatic lowering of product costs.”¹

—Harold T. McAleer, General Radio Company

Although a major (and in some ways an obvious) market for electronic testing equipment, makers and users of electronic devices have not been the only beneficiaries of automatic testing. Anyone who has had his blood tested recently, has flown safely in a 747 jet aircraft, or has contemplated purchasing a new Volkswagen, has been exposed to the potential savings (and not only financial) inherent in automatic testing.

The cost savings, both immediate and long term, result from a number of characteristics of automatic testing:

Human resources are conserved. Fewer persons can conduct more (and more-thorough) tests of high complexity with minimal training.

Volume. Large numbers of tests can be performed in a short time: either many tests on complex devices or fewer tests on large number of devices.

Reliability and consistency. A well-designed test program will perform identical tests leading to consistent results, with no aberrations due to misreading, fatigue, etc. If failure occurs in mid-test and repairs are made, the entire test cycle can be repeated,

¹IEEE Spectrum, May, 1971, “A Look at Automatic Testing”

numerous times if necessary, with full confidence that the most recent test has "cut no corners."

Multiplexing of adjustments and readouts. An instrument designed for use in automatic testing bears little physical resemblance to conventional instruments, since it need have neither binding posts, knobs, readout, nor even "front panel;" it shares the system's readout devices; connections and adjustments are made by the system.

Automatic Calibration. Any necessary calibrations, zero-adjustments, nonlinear-device compensations, or other predicted allowances can be made under system command. Range-changing can also be fully automated.

Measurement statistics. The system can retain in memory the results of all tests, the results of discrepant tests, and/or histograms of specific parameters, and print them out upon request. Yield studies can lead to product improvements, elimination of sources of repeated rejections, and prediction or tracing of future failures.

In short, a well thought-out, designed, and implemented automated test facility can reliably perform large numbers of tests, around the clock, on a "100%" basis, consistently and without tiring, with accuracy and skill, and with feedback to the designer for the next generation of the product. Skilled test personnel can be applied to more-creative pursuits than routine manual testing of the ins-and-outs of complex systems.

Then, as mentioned above, there are the many intangible benefits, that pay off in human values as well as dollars-and-cents: the aircraft engine that didn't fail, the electrical chassis that didn't need field repair, the steel rolling mill that didn't run away, the hospital patient that survived, the vendor whose reputation remained consistently high.

USES FOR AUTOMATIC TESTING

The manufacturer of components, such as integrated circuits, benefits greatly, because testing is a far-from-negligible cost in the integrated circuits business. Besides delivering a higher level of acceptable quality to the customer, he also develops more-accurate knowledge of yields and trends, and can serve needs for specific selection categories. For the producer of high-performance specialty IC's, such as Analog Devices, it is an indispensable tool. Such devices as the laser-trimmed AD510 low-offset op amps and the AD534 monolithic multiplier/divider would be so costly as to be infeasible if manual measurements and adjustments were involved. (Instead, the additional cost is a small fraction of the price of the standard unit.)

The user of large number of identical components can also benefit: He can weed out discrepant units in incoming inspection; measure, select, and grade units for different applications (rather than paying the manufacturer extra to do the same job); and keep comparative statistics from lot-to-lot and vendor-to-vendor. It may be noted, as a matter of perspective, that an average saving of 10¢ on 100,000 units is \$10,000.

The manufacturer of equipment and systems can test subassemblies in-process, or as received from subcontractors; he can also test completed pieces of equipment thoroughly. In both cases, the test system can be programmed for GO/NO at points of discrepancy, and to either reject the device for later evaluation, or branch into a diagnostic mode, to isolate the portion of the circuit (or perhaps even the component or connection) that is faulty. Repaired units can be recycled and subjected to the same battery of tests as the new units.

Highly-complex systems, such as jet aircraft and their various subsystems, can be tested thoroughly on the ground by a small number of persons in a short time, with a high probability of finding any faults, or the discrepancies that might indicate incipient faults. In addition, the on-board test and monitoring system can provide warning to the crew of anomalous subsystem behavior, and, as the electronic portions become increasingly sophisticated, it can perform a degree of diagnostic testing.

INGREDIENTS OF TEST SYSTEMS

For systems that test devices, the test begins with the *unit under test*. It must be handled, maneuvered into place, connected to. Then a *stimulus* is applied, and a *response* must be measured. The response is compared with a set of possible responses, and a *decision* is made (accept, reject, grade-and-sort, perform an adjustment) and communicated (print, store, mark, analyze), and a new instruction is given (next test, next set of connections, next device, wait for manual instruction, etc.). An outline of such a system is shown in the block diagram of Figure 1.

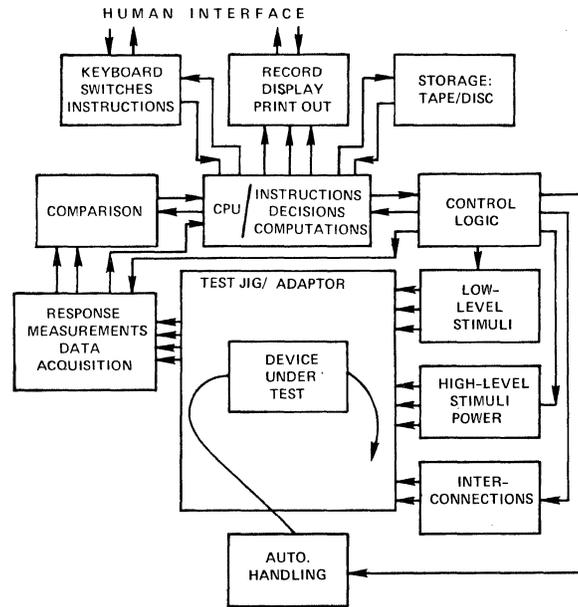


Figure 1. Test system ingredients in typical configuration.

Devices have at least two leads (resistors, capacitors), but they may have many more (op amps have at least six, printed-circuit boards may have 20 or more.) The instructions must call for connecting the appropriate stimulus generators and power sources to the appropriate terminals, and the appropriate measuring devices (bridges, amplifiers, etc.) to *their* appropriate terminals, and making all opens, shorts, “grounds,” links, etc., as required for the test step. Some of these may be hard-wired in the adaptor; others must be called for by software, or manual setting. Minimal noise pickup, interference, and parasitic effects caused by lead resistance, capacitance, and inductance are absolutely essential.

Converters in Test Systems

It may be fairly evident that much of the engineering and hardware cost of test systems goes into fixtures, switching devices, computers, peripherals, displays, wiring, and cabinetry. However, since the stimuli are digitally-controlled, and the responses must be returned to digital form for processing, it should be evident that converters and their accessories play a key role in ensuring test accuracy, speed, and reliability, yet represent but a small fraction of the cost of the system. For this reason, it may be false economy to use conversion devices that are anything but entirely adequate to do the job, or to seek to cut cost corners.

Typical uses of D/A converters in testing include: programmable power supplies, pulse generators, sweep generators, waveform generators (with appropriate digital inputs). They may be used as offset and gain “potentiometers” in calibration loops, as bridge-balancing voltage sources, and as part of A/D converters, sample-holds, peak-followers, etc.

A/D converters, either with multiplexing or per-channel, return the measurements to digital form, after processing by isolation or differential amplifiers, by op amps as electro-

meters, by multipliers, ratio devices, log devices, and all the other paraphernalia mentioned in Chapter 2.

An essential decision that must be made is the degree to which analog data reduction will be used, as compared with the performance of similar functions by digital software. Whatever the realities of the system itself, this consideration depends largely upon the background and experience of the designer; we suggest that analog-oriented designers not overlook the possibilities of software for reliable routine computation, and that digital designers consider the decreasing cost of functions that can be performed with analog modules and linear integrated circuits, and the balance between too much and too little data.

Much that could be said about system optimization, in terms of getting the best-possible interference-free measurements of suitable accuracy, has already been mentioned in several places in this book; and test systems are probably the most representative class of design problems requiring active application of these principles.

In component tests, where the lead-runs to the unit-under-test (UUT) are controllable, as is the local environment, the main sources of interference arise from the proximity of input, output, power, and logic leads in the vicinity of the test adaptor. In large-system testing, long leads, including multiconductor cables and connectors; the presence of electrical noise (RFI, power line and switching-transient spikes); and possibly unfavorable environmental conditions (temperature, humidity, vibration), may all make the measurement problem extremely difficult. It often turns out that, in the design of large systems, self-checking is an effective way of solving the interference problem, using a local μ P-controlled test subsystem that communicates digitally with an external system tester. If this is too ambitious, local digitizing, as an integral part of system design – in anticipation of testing – may provide a large ratio of benefits to cost.

B. COMMUNICATIONS AND SIGNAL ANALYSIS

In this section, we shall discuss briefly the class of converter applications that involve the generation, transmission, recovery, processing, storage, characterization, and synthesis of analog waveforms. Conceivable applications include:

- Time expansion, compression, (relative) advance, and delay
- Transient storage and recording
- Synthesis and analysis of speech and music (and waveforms in general)
- Transfer-function synthesis and analysis
- Convolution
- Digital filtering
- Recovery of signals from noise by correlation techniques and fast Fourier transforms
- Scrambling and unscrambling coded transmissions
- Generation of arbitrary signals and transfer functions

Digital methods, especially with microprocessors, can provide a powerful set of tools for dealing with analog functions and the transfer functions that operate on them in the time and frequency domains, as we have suggested in Chapter 5.

The key that unlocks the door is the A/D converter, which “freezes” a sample of the waveform and makes possible permanent storage without degradation. Thereafter, digital shift registers, binary rate-multipliers, memories, comparators, microprocessors, and control logic can perform a variety of operations entirely in digital format.

Except for errors due to the discrete (in time and amplitude) nature of the sampled signal, and approximations or roundoff errors in computation (where necessary or permitted), there is no loss of information, even though the signal be stored, multiplied, integrated, added, subtracted, correlated, or otherwise manipulated. It can of course be returned to the analog domain, via D/A conversion, and subjected to further processing there, while its attributes are still retained in Memory.

The circuits and ideas that appear here, all variations on the basic theme of the shift register delay line, represent promising areas of application, but they are not necessarily new or original. Their purpose is to unleash the reader's curiosity and creativity, in the field broadly encompassed by the title of this section. We've tried to avoid, except where necessary, mathematical particularities (and the controversies they sometimes engender).

SHIFT-REGISTER DELAY LINE

The basic tool for performing many interesting functions is the shift-register delay line, mentioned briefly in Chapter 4, and shown here again for further discussion.

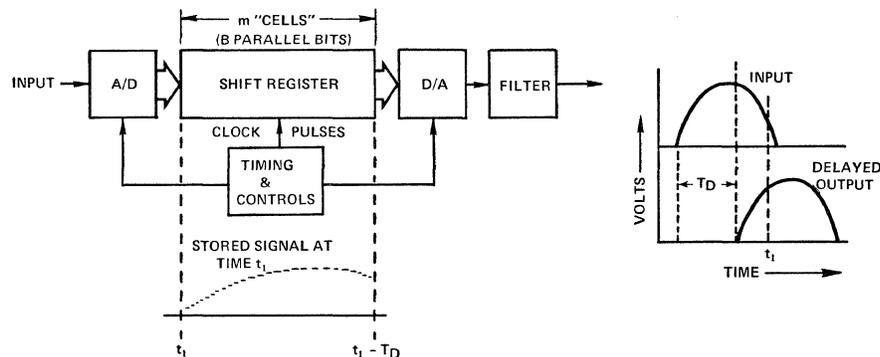


Figure 2. Parallel shift-register delay line.

Suppose the analog signal is a one-shot occurrence, of which m samples have been taken, that the clock has stopped, and the conversions have ceased. The signal is now stored in the delay line in digital form, and it will remain there until it is advanced or cleared or the power has been turned off. A number of interesting things may be done with the stored signal:

Read out into memory

The stored signal can be read out, a word at a time, and stored in memory, while the line awaits another transient (Figure 3).

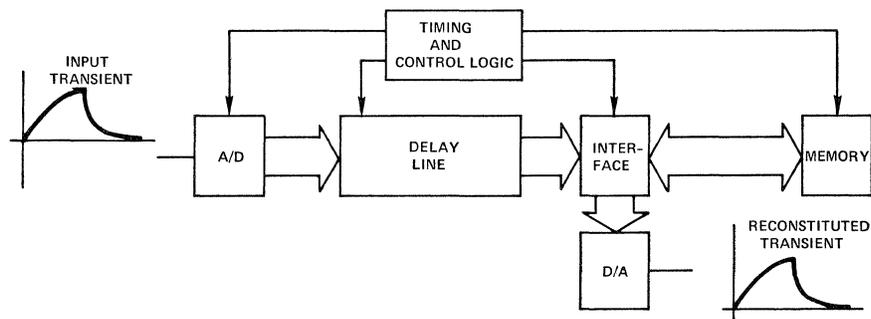


Figure 3. Transient recorder.

Read out as an analog signal

The signal can be read out and converted to an analog signal, each sample in turn, but at a rate arbitrarily determined by the choice of clock frequency. For example, the transient may have been quite rapid, but it is desired to plot it out on a chart recorder. Or, it may have been fed into the line slowly (perhaps even manually as an arbitrary waveform), to be used as a shaped stimulus for an analog process, and is to be discharged at high speed.

Recirculate

If the output end of the line is fed back to the input, it becomes a recirculating delay line (Figure 4). The stored signal will then appear at the end of the line repetitively, al-

lowing the transient to be displayed on an ordinary oscilloscope. By loading, or “charging”, with an arbitrary input signal (either analog or digital), then providing rapid recirculation and D/A conversion, it is possible to create an extremely wide range of arbitrary repetitive analog waveforms, of controllable repetition rate and amplitude.

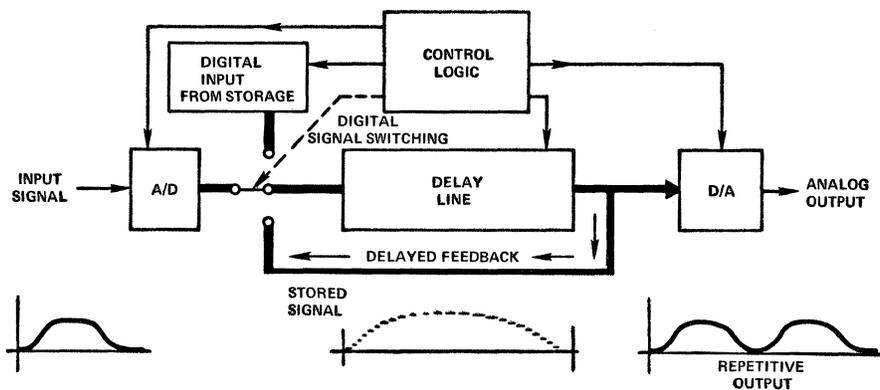


Figure 4. Recirculating delay line.

Perform waveform averaging by addition

If the same message is sent repeatedly but arrives at the converter accompanied by (and perhaps “buried in”) noise, it can be recovered by summing all the versions of the message: the coherent portions will add directly with the number of items summed, while the rms noise will tend to be “averaged out” and will increase only as the square-root of the number of items. For example, with 100 repetitions, the signal will be increased in relation to noise by a factor of 10. This can be accomplished with a delay line by summing each sample increment of the newest message with the sum of the corresponding samples of previous messages, accumulated in the delay line (Figure 5). Thus, when the second message arrives, its first sample is summed with the already-stored sum of the two previous first samples. Since the original messages are presumably identical, while the noise varies randomly, each iteration adds 1 unit of original signal to each sample, while the noise components tend to be averaged out.

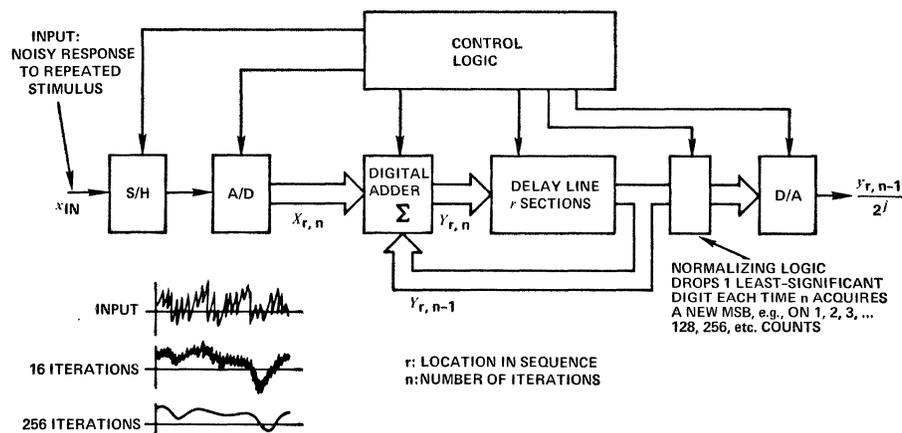


Figure 5. Waveform averaging by addition – basic scheme.

In practice, computing the simple sum

$$Y_{r,n} = Y_{r,n-1} + X_{r,n}$$

where

$Y_{r,n}$ = output of the n th sample at the r th position
 $X_{r,n}$ = input of the n th sample at the r th position

leads to an “open-ended” output amplitude, which is expensive to implement digitally and difficult to display on an oscilloscope during summation. It is a better idea to consider normalizing the output, i.e., dividing it by n , so that its average value tends to be constant. Since dividing digitally is not especially desirable, except for integral powers of 2, we may consider several alternatives based on the error-correcting relationship

$$Y_{r,n} = Y_{r,n-1} + \frac{X_{r,n} - Y_{r,n-1}}{n}$$

The first thing to observe is that as n becomes large, $Y_{r,n}$ and $Y_{r,n-1}$ are very nearly equal, and each additional increment causes little change, because it is divided by n . The second thing to note is that, since both terms of the difference can occur in analog form (the input and the last value of output), the difference could be taken before conversion, substituting an op amp for a digital subtractor (Figure 6). Finally, one might observe that division by n could be performed either as an analog function (counter and DAC supplying reference voltage proportional to n to the ADC), or as a digital approximation using only integral powers of 2, obtained by shifting the ADC output code one bit toward the right (dropping the last bit), as each increasingly-significant bit of n appears on a counter.

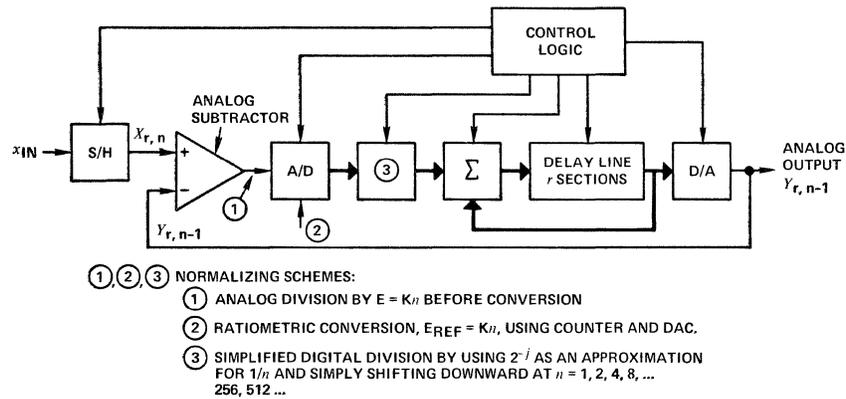


Figure 6. Waveform averaging by addition using normalized variables.

Time Compression by Sampling

In Figure 7, a shift register is advanced at a high frequency, f_c , for example 513kHz. The converter is digitizing a slowly-varying signal at a rate f_s . Suppose that the shift register has 512 steps, and that at a given instant, the 512th sample appears at the output and is fed back to the input. On the next step, starting the m th iteration, the converter output, $X_{1,m}$, is fed into the line to replace the output $X_{1,m-1}$. The line then advances for 512

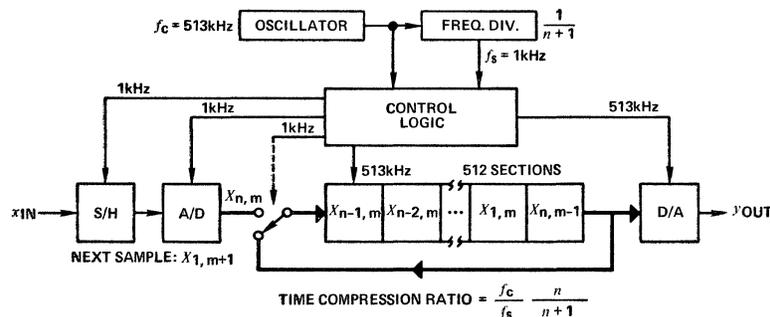


Figure 7. Time compression by sampling. On next count, $X_{n,m}$ is introduced into the line to replace $X_{n,m-1}$. At $n+1$ additional counts, $X_{1,m+1}$ is introduced to replace $X_{1,m}$.

steps. On the 512th step, the input is once again $X_{1,m}$, and $X_{2,m-1}$ appears at the end of the line, while $X_{2,m}$ is ready at the converter output. On the 513th step, the converter output is fed into the line to replace $X_{2,m-1}$. $X_{1,m}$ and $X_{2,m}$ are now indexed down the line, and on the 513th step, $X_{3,m}$ replaces $X_{3,m-1}$. By the time 512 conversions have occurred, in real time, the sampled signal (including new and previous values) has circulated 513 times, thus providing a 512-fold-speeded-up version of the (1.96Hz) analog input waveform at the output of the D/A converter, at the equivalent of 1ms per sample.

If each cycle of the analog waveform is identical to the adjacent ones, and if the clock is synchronized to the analog signal, the output of the DAC, plotted on an oscilloscope screen, swept at 1kHz, will appear to stand still, plotting the low-frequency input, but *with no flicker*. Changes of the input signal, from iteration to iteration, will appear as progressively-appearing changes to the stationary pattern.

Since the compression ratio depends on the time required for each 511 samples, it is proportional to the clock frequency, which can be locked in at any convenient value. A typical application for time compression is in real-time spectrum analyzers.

Real-Time Correlation

For an input function, $f(t)$, the output of the delay line over a complete circulation (in compressed time) is a set of values of $f(t - \tau_i)$. If the successive values are multiplied by the sampled value of another waveform, $g(t)$, which, with $f(t)$, is updated after each circulation, and if each individual product is averaged with its synchronous counterparts from previous circulations, the output of the averager will represent a sample-by-sample cross-correlation of f and g at a real-time rate, delayed by the product of the sampling period and the number of samples circulated (Figure 8).

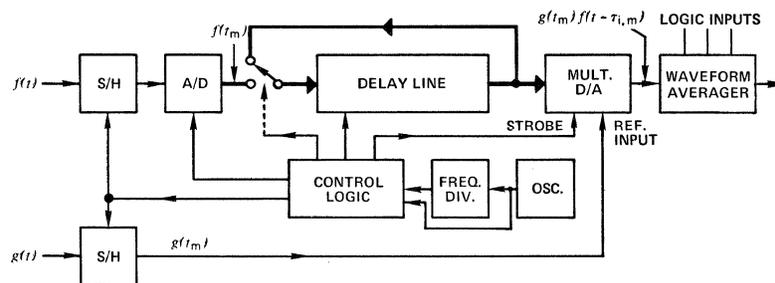


Figure 8. Real-time correlation using delay line.

Incremental Delay Line as a Filter

If the delay line consists of a number of sections, and the outputs at these taps are converted to analog form, and summed, with arbitrary coefficients, it is possible to synthesize arbitrary time-domain responses to steps, pulses, or other waveforms. Since the output bears a linear* relationship to the input, the resulting transfer function may provide amplitude and phase responses to other signal forms (over limited ranges of frequency) that can be expressed by transform integrals but are otherwise formally considered “unrealizable.” In this case, the output is a function of the input only (Figure 9a).

Recursive Filtering

When the output is a function of input only, the number of possible responses is limited, because the output will settle within a finite time after the input has ceased to vary. However, by making the output a function of both output and input, a more-general (and more interesting) set of responses becomes possible.

Recursion may be achieved by feeding back from the output to each tap point (after it has made its contribution); but this requires an A/D converter for each tap. A more economical scheme uses a second tapped delay line, fed back (in sections – if desired) to the output summing amplifier, thus requiring only D/A converters for each tap point (Figure 9b)

*i.e., if the input is doubled, the corresponding output will be doubled.

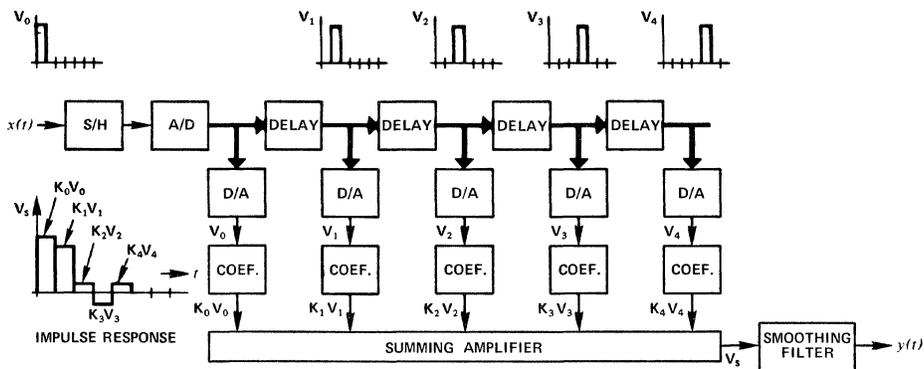


Figure 9a. Delay line as a filter with programmable real-time response. (Small number of sections shown for clarity).

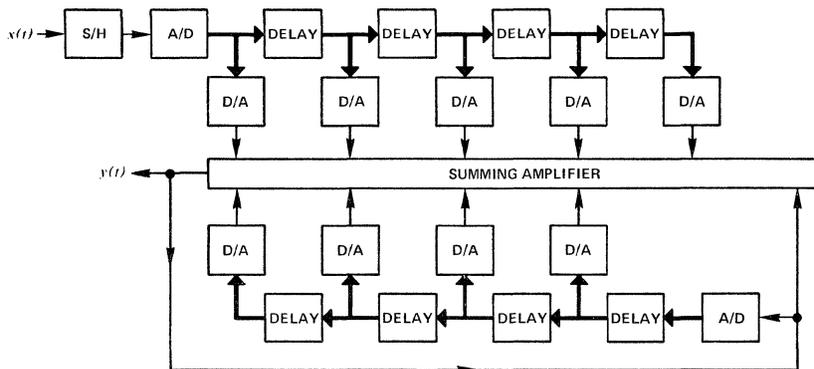


Figure 9b. Delay line in recursive filtering. Coefficients (not shown) can be applied manually or digitally (multiplying DAC's).

CONCLUSION

Though it has been limited in scope, we hope that this section has provided the reader with an awareness of the power of digital techniques in signal processing, just through the use of delay-line storage. There are many more hard-wired processing tricks available, such as the use of binary rate-multipliers for digital frequency modulation of digital signals, counters for converting from frequencies to discrete digital values, and voltage-to-frequency converters for analog modulation of digital signals.

The growing availability of digital components of high complexity (FFT processors), increasing speed, and low cost (microcomputers), plus the possibility of overall control of the processing by CPU's and stored commands, makes the outlook for analog waveform synthesis and processing by digital techniques extremely bright, whatever the source: speech, music, noise, gas chromatographs, electroencephalograms, mechanical vibrations, to mention just a few.

C. CATHODE-RAY-TUBE DISPLAYS

In the industrial and scientific world, the close association of computer and cathode-ray tube provides an unparalleled method for speedy access to stored and real-time data. It simultaneously affords the opportunity for interactive dialogue with the computer for the purpose of actually controlling what the computer does. The recent growth of electron-beam recording (on film negative) poses a serious challenge to the centuries-old tradition of typesetting, while the ability to use computer power to adapt data to the needs of the human operator prior to presentation makes the computer-CRT display a powerful combination indeed.

While systems do exist for the sole purpose of display, the more general application of displays is in connection with data-acquisition systems and systems involving computers. Such systems may be either purely digital in nature (e.g., business systems with punched-card inputs), or they may involve A/D and D/A converters in maintaining input and output contacts with the "real world." Whatever the display's purpose, or the source of the data, many cathode ray displays involve the use of D/A converters for generating sweeps, characters, and vectors, for positioning and intensification, relying on their inherent linearity, reproducibility, and controllability by entirely digital sources of command.

Since we are concerned here primarily with display systems that employ converters – with particular emphasis on the way they are used and the factors of importance in selecting and using them – the number of systems chosen will be limited and system description brief.

In general, a cathode-ray display system consists of a display processor and the display chassis. The processor usually holds the information to be presented for update, the instructions for presenting it, the signals needed to activate the display elements, and the digital-to-analog processing hardware, and may include a *refresh memory*. The display chassis itself contains power supplies, CRT, circuitry for beam positioning intensification, nonlinearity correction, and focus.

Representative display techniques include:

- TV raster (picture and graphic displays)
- Stored-character display, e.g., Monoscope (alphanumerics)
- Dot-matrix (alphanumerics)
- Cursive: stroke and vector generators (alphanumerics and graphics)
- Rotating (PPI)

In addition, electron-beam recording (EBR) is a high-precision technique allied to the TV raster, but capable of considerably greater resolution, because it records on film, without regard for screen persistence or "flicker" problems, and can thus afford considerably greater time-per-frame.¹

BASIC SYSTEM

Figure 10 shows the generalized system outline for an installation capable of accepting, processing, storing, and displaying information on a CRT screen. A purely clerical system would not normally involve sensors and A/D interface systems, but might on the other hand, involve other forms of peripheral data input. An air traffic control system, based on radar data, is an example of current usage of CRT displays for interactive handling and presentation of complex information.

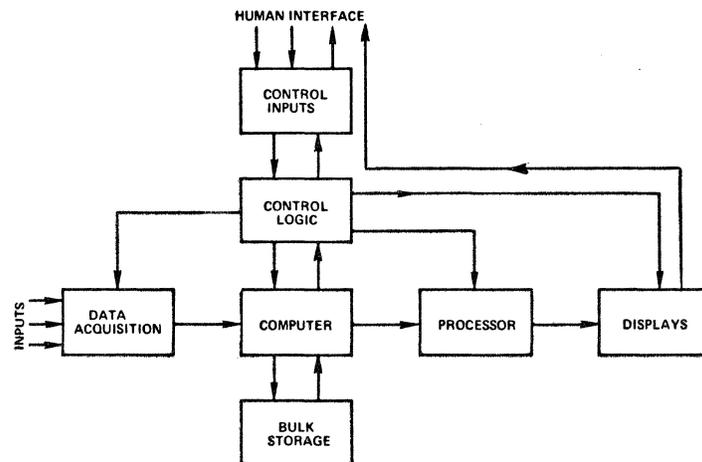


Figure 10. Display system outline.

¹ *Analog Dialogue*, Vol. 6, No. 1, p. 14 "EBR uses 16-Bit DAC"

Further ingredients of the generalized display system are quite straightforward. The manual controls provide human interface, enabling the operator to call for a specific picture (or portion of a picture), to enter new information into the system, to command new modes of operation, and to initiate different data-processing and display functions. Bulk storage forms part of the data-processing capability; further auxiliary storage is often required, in the absence of storage-type CR tubes, for display refreshing at high speed to avoid annoying flicker. Control logic interfaces between computer data and the various peripheral devices, including displays, memories, communications links, the human operator, data-acquisition circuits, etc.

USES OF D/A CONVERTERS IN DISPLAYS

Raster Displays

In Chapter 4, a counter-driven D/A converter was suggested as a sawtooth sweep generator. When used for displays, this scheme can provide highly-repeatable, controllable, and linear sweeps of arbitrary resolution and accuracy.

Rasters conventionally are generated by a fast horizontal scan, that is swept vertically at a slower rate that will allow a given number of lines to be generated during the period for a frame. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace (i.e. time for 1 line) multiplied by the number of lines, plus vertical retrace time.

D/A converters are well-suited to vertical sweeps, for a number of reasons:

- Timing, controlled by a clock and logic, is quite precise and uniform.
- Lines are horizontal (analog sweeps have slight tilt).
- Line-spacing-uniformity depends on linearity, while maximum number of lines depends on DAC resolution. DAC's having 10-bit resolution (1024 lines) and 12-bit linearity (0.0125% linearity error) are readily available. In electron-beam recording, a 16-bit DAC provides 4096 lines with less than 5% spacing error.
- DAC switching transients are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the requirements on DAC's are more severe, and analog sweeps are likely to win the cost tradeoff, in most applications. For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle well within 100ns, and that there be no "glitches." (Even if the display is blanked between horizontal steps, large glitches at major carriers can cause deflection-amplifier transients, which distort the pattern.) While this is feasible (e.g., DAC-10DF), cost is increasing rapidly with resolution.

Raster displays using either analog or internally-synchronized digital sweeps have the weakness that the whole picture must be updated at once: specific portions cannot be singled out for local refreshing. For this reason, plus the low cost of video hardware (if it can be successfully adapted to the use at hand), a major application of raster displays is in multiple or remote monitoring, where no interaction is needed.

However, if it is necessary to update the display in local spots only, or to interact with it (for example, in editing), a form of display that allows access to specific portions of the tube face must be used.

Dot-Matrix Displays

Another name for a display in which each point to be brightened has a definite address is the highly-descriptive one: dot-matrix. While it can take the form of a raster display with both sweeps digital, the speed limitations and memory requirements make a variation of it more useful, especially for alphanumeric: the stored-character dot-matrix.

Each character might be represented by a matrix of points, e.g., 4×7 , with each point that is defined as part of the character intensified, by either a "mini-raster" scan or a character trace. The X and Y coordinates of each point are located at addresses in two ROM's; in character tracing, the point is addressed by a word consisting of a format code for the character (e.g., ASCII) and a number from a counter indicating the order of the point in the writing sequence.

In a typical system using this presentation (Figure 11), two DAC's with outputs that are summed are used for each axis. One set of DAC's, producing sweeps in raster format, locates the index point (i.e., position) of the character. The second set produces a sequential set of outputs that rapidly move the spot from one point to the next, until the character has been traced out.

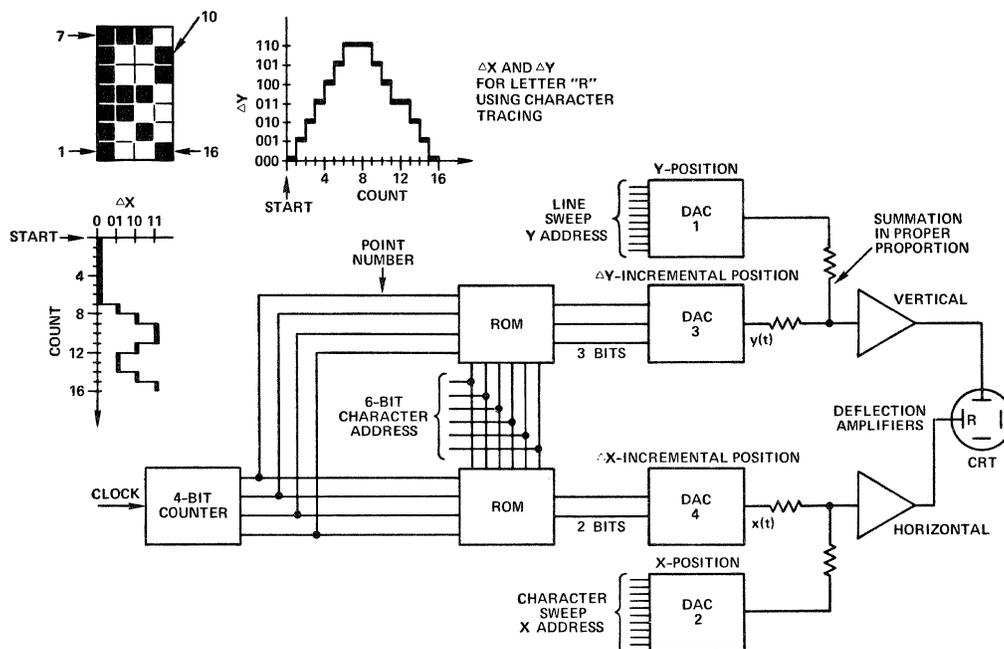


Figure 11. Dot matrix display scheme.

An important advantage of this scheme is that low-resolution (but high linearity) DAC's can be used to locate each character, in the same way that a typewriter indexes across a page, character by character, and down the page, line by line. Glitches are no problem because the trace is blanked in transit. The DAC's that produce the characters need only have fast response, with very modest resolution and accuracy. And the refresh memory needs to store only the character codes, rather than all points for each character.

For a purely alphanumeric display, type "point size" and "leading" could be determined by manual gain controls of the respective DAC's, to the degree allowed by the logic determining the character count per line and the amount of information to be presented in each frame.

Information can be updated incrementally by addressing specific display locations, and grossly by either displaying new frames, or by a "scrolling" or "waterfall" (in reverse) scheme in which data is advanced vertically. Old data disappears at the top as new data appears at the bottom.

Of course, the "typewriter" presentation need not be used at all. For example, in a display that combines graphics and alphanumerics, the X and Y DAC's may be set at the appropriate arbitrary address for each character of a caption, which is then supplied via the ROM. Captions may also be read along vertical lines if axes are interchanged. Although 2 and 3 bits served to display the character adequately in the example, the D/A converter may have many more bits available for handling other forms of additive input. It is important to note, though, that the accuracy and resolution of the positioning DAC

must be such that its errors are less than the relatively-weighted value (taking differing scaling into account) of the least-significant bits of DAC's whose outputs are summed. Otherwise, overlapping or uneven spacing may result.

GRAPHIC DISPLAYS

The general objective in graphic displays is to provide a flickerless presentation of numerical, line-drawing, or pictorial information, with the possibility of editing, changing, storing, or isolating any element of it. If the drawing is synthesized by definable and reproducible computer operations, then any number of schemes may be used for the actual control and interaction, ranging from keyboards to "light pens."

The general problem is to start with the spot at a given point (which may be any point arrived at in the course of plotting the display, or it may be a point that has been recalled for replotting), and proceed by a straight-line increment to another point, using a programmed analog technique. (For better control of spot position, it could be done digitally by closely-spaced dots, perhaps employing a binary rate-multiplier, but, on the other hand, it may be highly desirable to reduce the amount of memory or digital manipulation involved.) It is important to avoid variations of intensity caused by velocity modulation, by either maintaining constant writing speed or by compensating for variable writing speed by appropriate intensity modulation (the former is preferable if it can be accomplished simply).

Delay-Line Integrator

In Figure 12, a single high-resolution converter is used for each coordinate. The outputs of the converters are incremented in small, equal steps of X or Y, whichever is the greater in magnitude. Between the converter output and the deflection amplifier is a "delay-line integrator," essentially a fast analog delay line tailored for step response that has a fixed delay time, and is linear with time from the initial value to the final value. It will then hold the final value until the input changes. Because the maximum input steps are equal, the delay line will maintain a constant maximum writing rate in the X or Y direction (until the other variable becomes greater). Since the larger of the two variables has been chosen, the largest possible vector change (occurring in the case where they are equal) is 1.4 times as great. The range from 1 to 1.4 is sufficiently small that only a few values (if any) of intensity-modulation voltage will be needed to provide adequate correction for changes in writing speed.

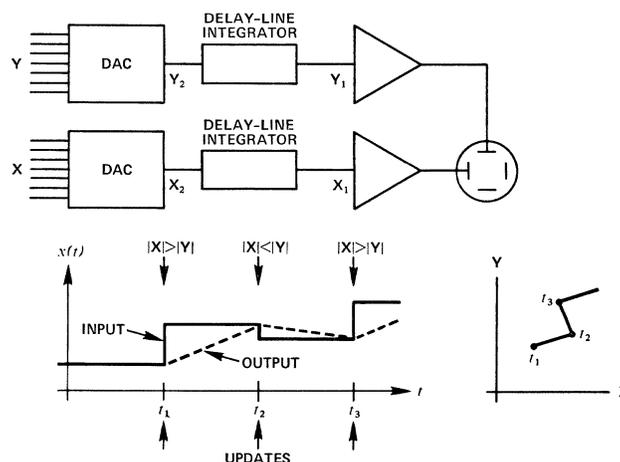


Figure 12. Delay-line integrator. DAC outputs have just switched to new values, X_2 , Y_2 . Delay line outputs X_1 , Y_1 will change to new values linearly.

Vectors and Segments

An obvious way of obtaining a given rate of change of voltage is to feed a constant into an integrator: the rate of change of output is proportional to the input. Thus, starting with an initial position X_0, Y_0 , furnished by a DAC pair, there is added to it the output of a pair of integrators, the inputs of which are slope update outputs from another DAC pair with inputs from the refresh memory. The slope update signals may change during the configuration of a character, or they may allow long uninterrupted straight sweeps. The two major difficulties with this approach are that the integrator must be reset to eliminate drift, and there is no easy way to maintain constant trace brightness.

Another approach uses ramps instead of integrators. In the (perhaps unwieldy) circuit of Figure 13, there are two out-of-phase triangular waves, two high-accuracy DAC's for initial positioning, and four multiplying D/A converters supplying the coordinates of the points to be connected.

Starting from an initial point, determined by the X and Y position DAC's, the rates of change of X and Y are determined by multiplying the digital input values by the ramps and summing the out-of-phase values in the output amplifier, e.g., $(X_2 - X_1)$ and $(Y_2 - Y_1)$ for the positive slope of the synchronous ramp.

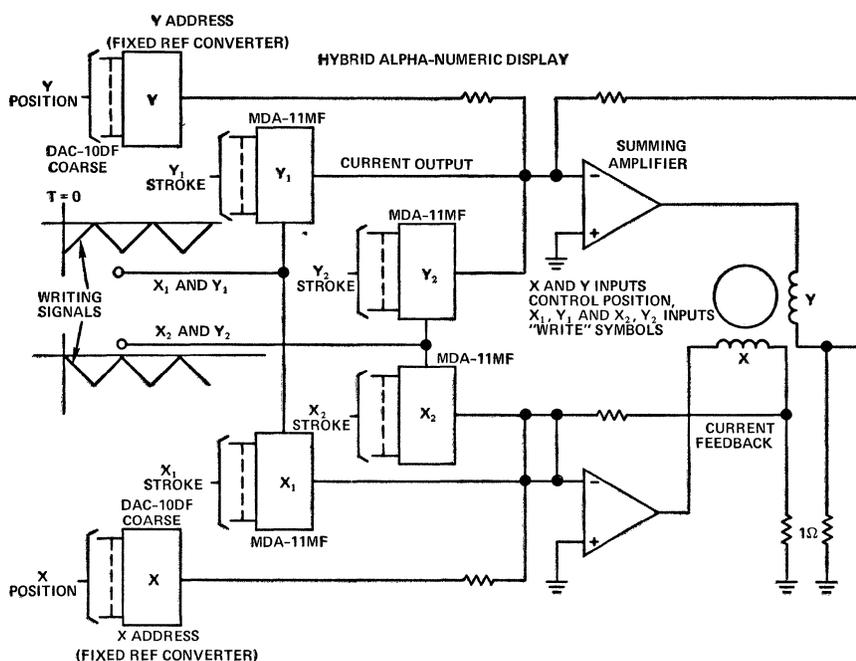


Figure 13. Display system combines fixed-reference converters for coarse positioning, plus multiplying converters for applying "writing" analog signals to the deflection circuits. Method uses common analog triangular waveform for synthesizing all alpha-numeric symbols, instead of using a unique analog waveform for each symbol.

When updating occurs, the ramp at the same time changes slope, and the old value, i.e., X_1, Y_1 is replaced by X_3, Y_3 . The new rates of changes are thus determined by $-(X_2 - X_3)$ and $-(Y_2 - Y_3)$, or $X_3 - X_2$ and $Y_3 - Y_2$. Thus, each new incremental slope is determined by the difference between the new input and the previous input, always in the proper sense.

Unlike the integrator, resetting is not necessary; however, the values of X and Y should be refreshed from time to time, since the net change depends on the ramp amplitude, and tolerances build up. Also, it is necessary for the computer to determine the vector change and modulate the intensity appropriately.

There are many other schemes that could be conceived of, and a number have been described in the literature. In some recent schemes, binary rate-multipliers are used for direct digital multiplication to supplant multiplying DAC's.

D. COMMERCE, INDUSTRY, AND ELSEWHERE

The reader who has arrived at this point (after presumably reading all of the material in Part One) has been exposed to a large variety of circuit configurations and application suggestions. It would not have been difficult for him to have noticed that some of the configurations looked more-or-less alike, though offered from somewhat different viewpoints.

In this section, he will not find anything especially different, from the circuit point of view, but he may find it of interest as a microcosmic glimpse of the applications of conversion devices in the workaday world. We will show here just a few applications, with the descriptive emphasis more on what they *accomplish*, rather than on how their circuits go together.

At the end of this chapter will be found a brief appendix, listing a large number of randomly-aggregated present and possible uses for conversion and the associated analog-digital technology. This list, in no sense complete, and in no wise organized in any rational way, might represent the result of a quick scan of one or two current magazines, and the recesses of one's mind. It will not impress anyone now working in the field. However, for the reader who is unaccustomed to the power of computational techniques, it may be an excellent point of departure for the development of ideas as to how they might help in his own field.

Because A/D and D/A converters were originally developed as computer interfacing devices, used primarily for getting data into and out of digital computers, the casual observer still tends to associate them with computer application alone. In reality, as Chapter 5 has demonstrated, both A/D and D/A converters have followed the operational amplifier out of the computer laboratory and into the industrial world-at-large.

Digital communications is increasingly employed for its noise immunity. Likewise, digital methods are used in testing, controlling, and measuring, owing to their ease of application, and the simplicity with which digital data can be manipulated, stored, processed, addressed, distributed, scaled, and otherwise handled.

One result is an interesting variety of applications for A/D and D/A converters, in which the unit has a life of its own, quite independent of a computer, as a component of a piece of equipment designed for a purpose.

AUTOMATIC SCALE ZEROING

The use of a D/A converter to reset zero in a weighing machine (Figure 14) is typical of a large number of uses for the D/A converter as a long-term sample-hold device, as mentioned in Chapter 5.

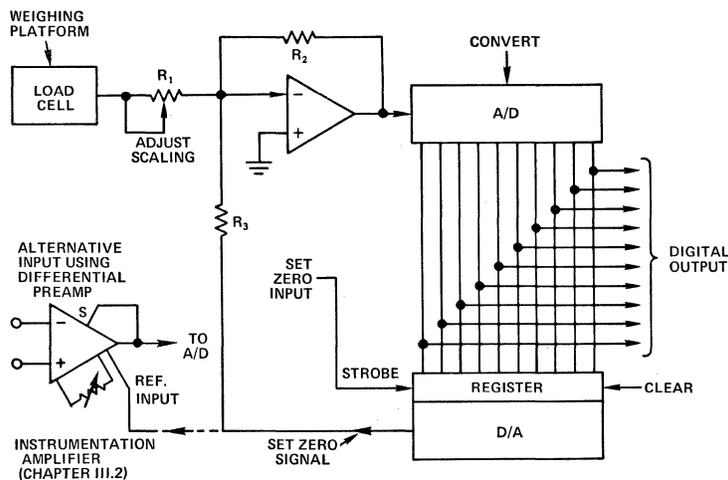


Figure 14. Weighing device with automatic "push-button" tare weight compensation.

The purpose of the arrangement is to measure the container (or “tare”) weight and feed it back to the summing point of an operational amplifier, to produce a null reading, so that when the container is filled, only the weight of the contents is read out.

The procedure is simple: The empty container is placed on the scale, with the D/A output at zero. The voltage representing the container’s weight is converted to digital form by the A/D converter. Then the A/D output is strobed into the D/A converter, producing an output that is equal, but of opposite polarity, to the input, thus zeroing the summing-amplifier output. When the load is applied, another conversion is performed (but does not affect the D/A output), and the weight of the load alone is read out.

The amplifier can be so scaled that the converter (which may be part of a DPM) reads out in engineering units of weight, or some function of weight, such as cost. If the A/D converter is a BCD type, the D/A converter should be similarly coded. If the input range of the A/D converter is similar to the output range of the D/A, $R_2 = R_3$, with R_1 setting the overall gain relationship. If an instrumentation amplifier is used, the DAC adjusts its reference.

The same basic idea is applicable to any situation for which push-button zeroing is desirable, usually when sophisticated equipment is being operated by untrained personnel, or when time is of the essence, as in production-line operations.

LOW-NOISE COMMUNICATIONS

Digital techniques for voice and data transmission¹ are widely used by the common carriers, NASA, the military, railroads, and many more. The purpose is to gain increased immunity to noise and to preserve the fidelity of the transmitted information in the presence of nonlinearities, analog crosstalk, etc.

Low noise communication is possible when a voice signal is converted to digital form before transmission. Analog signals pick up noise, and, though amplified in “repeater” stations along the way, tend to become progressively degraded. But if digital transmission is used, the signal can be restored by reshaping or regenerating the pulses. At the receiving end, a D/A converter reconstructs the original voice signal.

Figure 15 is a simplified diagram of such a system. The analog signal is sampled at regular intervals, converted to digital form in the A/D converter, and transmitted serially, along with the clock pulses. At the receiving end, the signals are assembled in a shift register, kept in step by the clock pulses, and converted back to the original audio signal with the D/A converter.

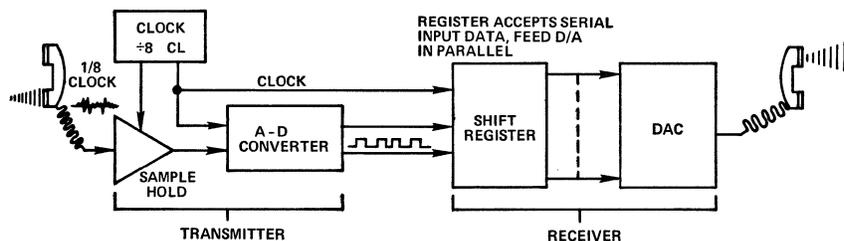


Figure 15. Digital voice communications.

The clock frequency is divided by 8 before being applied to the sample-hold. The A/D converter thus sends one serial 8-bit word for each time the sample-hold circuit is strobed. The shift register at the receiving end assembles the words of eight bits each.

The sampling rate should be at least twice the bandwidth. Thus for 5kHz bandwidth, a 10kHz sampling rate is required. The converters thus should operate on 0.1ms cycle times.

¹This topic and the following one (among others) were described in *Electronics*, October 26, 1970 “Purring D/A Converters to Work. . .” and are still of timely interest.

MUSIC DISTRIBUTION SYSTEMS

Music-distribution systems in commercial aircraft (e.g., the Boeing 747) utilize digital techniques to conserve wiring and economize on weight. As an alternative to piping eight analog channels to each seat, in parallel (with all the wiring involved, as well as the possibilities of crosstalk), the music channels are multiplexed, distributed digitally on one pair of wires, and decoded at the seat.

In Figure 16, the analog music channels are multiplexed into the sample-and-hold circuit. The A/D converter sends out serial words corresponding to each of the eight channels in sequence. A 3-bit address code is added to the 8 bit of analog information, and the complete word is wired to every seat in the plane. At each seat, an address decoder is linked with the channel-selector switch, and the D/A converter operates only on the digital word corresponding to the selected channel.

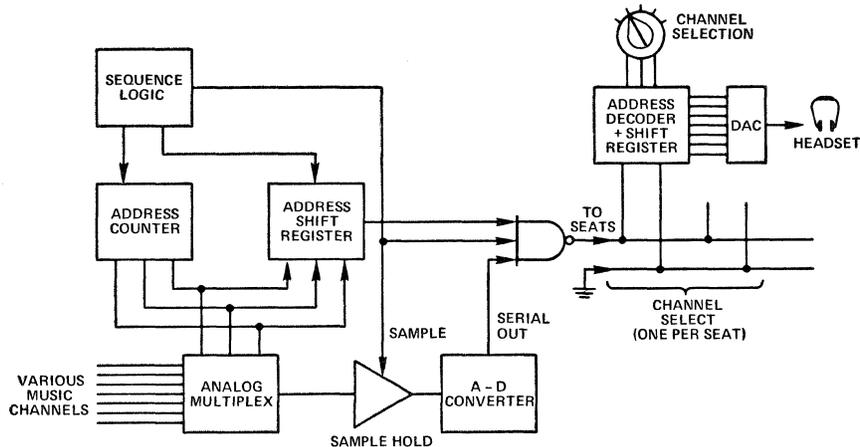


Figure 16. Aircraft music distribution.

As in the previous application, absolute accuracy in the D/A converters is unimportant — all that counts for good sound reproduction is linearity. It's also interesting to note that only 6 bits are required for reasonably satisfactory music reproduction ($6 \times 6 = 36\text{dB}$). ("It's a nice place to visit, but I wouldn't want to live there.")

POWER RECTIFIER MONITORING

Availability of low-cost digital computers and peripheral equipment has opened up a new field in the real-time monitoring of high-power systems, and detecting incipient danger signals in time to protect against (really) catastrophic failure. One can foresee application of the principle to large turbines, generators, engines, pumps, and machine tools, and other equipment where continuous monitoring and comparison of oil pressure, bearing temperature, mechanical stresses, etc., can prevent destruction of expensive (perhaps irreplaceable) equipment and even save human lives.

Digital protection is well-suited to systems that must operate constantly and consistently, but it is perhaps even more advantageous for systems that operate over wide ranges of temperature, pressure, altitude, speed, or must be started and stopped frequently.

The concept of digital protection is exemplified very effectively by a 128-megawatt power-rectifier system used at the Lawrence Radiation Laboratory, Berkeley, California,² for magnet-field control in the Bevatron particle accelerator (Figure 17).

² *Analog Dialogue*, Vol. 5, No. 3, "Protecting a 1/8 Gigawatt Power Supply (8kVA at 16kV) or How Do You Make a 2000A Fuse?"

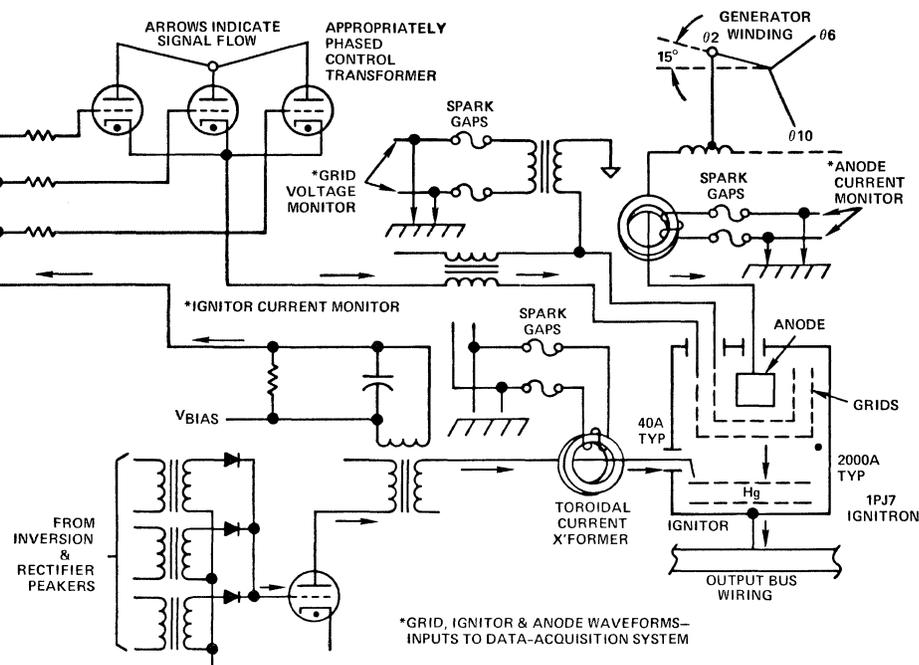


Figure 17a. Ignitron monitoring system.

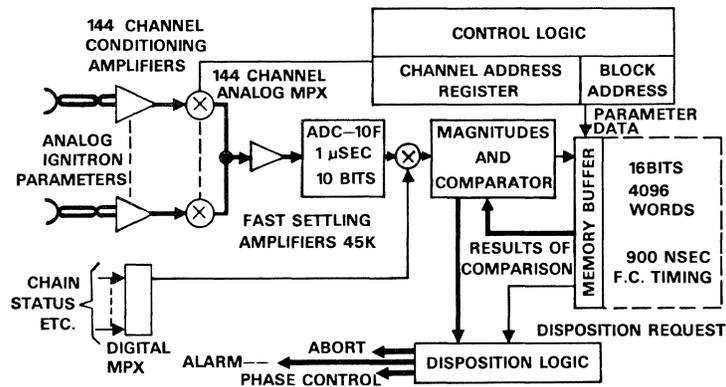


Figure 17b. Data acquisition system.

Figure 17. Bevatron data-acquisition system.

The rectifier system is based on 48 mercury Ignitrons (high-power rectifiers), operating in parallel pairs, each of which handles an anode current of 2000 amperes. Output dc power is controlled SCR-fashion by adjusting the time, within each cycle of the 12-phase 60Hz excitation power, at which the individual ignitrons conduct. Firing control is accomplished by varying the phase of the drive pulses applied to each ignitron's grid. Faulty firing can obviously create havoc within the system, by simply causing one ignitron in a pair to conduct prematurely – or not at all – so that current is unequally distributed between ignitron pairs.

A fast data-acquisition system samples such waveforms as grid voltage, ignitor current, and anode current, for each tube, at a large number of intervals during each cycle and compares them with stored threshold values (perhaps obtained by processing earlier data). Any significant disparities are noted, analyzed, and appropriate action is automatically initiated, ranging from minor adjustments, to a "flag," to shutdown.

Since such anomalies can signal incipient breakdowns, this scheme can prevent the very expensive consequences of losing large amounts of power under fault conditions, even for very short times. The method also allows observation of aging and so can effect parts

replacement at appropriate, rather than arbitrary, intervals. It also provides rather obvious means of feedback of life data to parts manufacturers, who can use the information for product reliability improvement. (It's much harder to diagnose the source of failure by investigation of a hardened puddle of metal and glass, or after an explosion of suddenly-vaporized coolant.)

Although most readers of this book are unlikely to be designers of control systems for Bevatrons, a little thought will show that the monitoring principles applied in this case may prove useful elsewhere for minimizing risks of failure, and for failure analysis, in any system where catastrophic failure should be unthinkable.

APPENDIX TO CHAPTER SIX

A random, incomplete, disorderly, and possibly presumptuous (*but, hopefully, thought-provoking*) list of present and likely areas where A/D and D/A conversion may help.

Accumulated life information
Actuators, displays, indicators
Aircraft hydraulic system testing
Air traffic control system
Angular rate, linear force, swept frequency, programmed temperature, forced vibrations, etc., generated electronically
Architectural work
Automated production processes
Automatic pushbutton zeroing by nontechnical personnel
Automatic scale zeroing
Automatic test system

Bins, putting things into
Blood, automatic chemical testing
Blood pressure monitoring in intensive care

Calibration curves
Chart-recorder overrange
Chemical plants & complexes
"Chirp" radar
Communications signals
Complete testing from several-hundred tests/min
Constant-speed alternator
Continuous blending
Controllers

Depth of cut
Digitally-controlled aircraft simulator
Digital control of steel mills
Digital speech & music transmission, multiplexed
Doppler radar, ignoring returns from stationary objects

Electrical substation
Electronic weighing
Electrochemical analyzer
Electrochemical baths
Emitted energy from bombarded target
Energy level, momentum, light intensity

Factory electrical power demand peaks
Firmware
Flow meter
Fluidic devices
Food processing operations
Foundry operations
Frequency synthesizer

Gas chromatographs
Generate ideas for rectifier improvements
Grading apples
Graphics design

Hangar and airfield testing of aircraft
High-voltage power supplies
High-power systems (real-time monitoring)
Histograms

IC semiconductor test equipment
Industrial, aeronautic, or scientific
Infrared optical pyrometers
Infra-red techniques
Instrument servos

Lasers and optoelectronics
Level indicators
Load cell

Machine shops
Maintenance scheduling
Mass spectrometers
Materials testing
Mechanical handling
Mechanical servos

Metal fabrication
Metal-removing speed
Metalworking
Monitoring oil pressure, bearing temperature, mechanical stress
Motor drive
MPX music distribution systems for passengers in 747's

Nuclear accelerators
Null balance
Numerically-controlled machine tools
N/C positioner

Oceanography
Ocean technology
On-line chemical process

Pharmaceutical plants
Plating plants
Pollution monitoring
Power-rectifier monitoring
Precision 3-phase output (synchronous motor speed control)
Pressure gages
Pressure regulators
Pressure, temperature, seismic, sonar, radar, and other transducers
Printing and graphics
Programmable power supplies
Protects against breakdown
Pulp and paper mills
Pulse-height analysis

Radar or fire-control system
Radar plan-position & moving-target indicators
Real-time process control
Relay testing
Remote or unattended monitoring
RF measurements

Seismographic experimentation
Ship's turbine, widely-differing speeds, temperature, pressure, humidity, shaft speed, torque
Signal processing in radar and sonar systems
Simulator's altimeter
Solenoid valves
Sonar returns
Spectral analysis
Speed control
Steel industry
Steel rolling mill
Stress signals
Sulfur dioxide monitors
Supersonic air blasts
Synchro-resolver

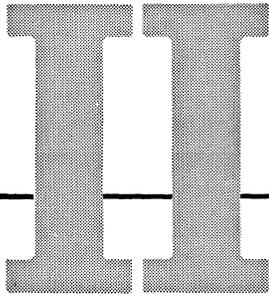
Tachometer signals
Tanks, boilers, vats, pipelines, bearings, oil burners (temperature sensing)
Tare weight compensation
Textile mills
Thermal ovens
Tone generator
Tracked air-cushion vehicle
Training simulators
Turbines, generators, engines, pumps, machine tools
Typesetting

Utility Substation

Valves and Actuators

Weather charts
Weather stations
Weighing machines
Wind tunnel

X-ray dosage



Understanding Converters

Chapter II-1

A/D converters translate from analog measurements, which are characteristic of most phenomena in the “real world,” to digital language, used in information processing, computing, data transmission, and control systems. D/A converters are used in transforming transmitted data or the results of computation back to “real-world” variables for control, information display, or further analog processing.

ANALOG QUANTITIES

Analog input variables, whatever their origin, are most frequently converted by transducers into voltages or currents. These electrical quantities may appear as “dc” continuous direct measurements of a phenomenon, as modulated ac waveforms (using a wide variety of modulation techniques), or in some combination, with a spatial configuration of related variables to represent shaft angles. Examples of the first are outputs of thermocouples, potentiometers on dc references, analog computers; of the second, “chopped” optical measurements, ac strain gage or bridge outputs; and of the third, synchros and resolvers.

The analog variables to be dealt with in this chapter are those involving “dc” voltages or currents representing the actual analog phenomena. They may be either wideband or narrow-band. They may be either scaled from the direct measurement, or subjected to some form of analog pre-processing, such as linearization, combination, demodulation, filtering, sample-hold, etc. As part of the process, the voltages and currents are “normalized” to ranges compatible with assigned converter input ranges. Ways and means of accomplishing appropriate pre-processing are discussed in the chapters on applications and system accessories. Analog output voltages or currents from D/A converters are direct and in normalized form, but they may be subsequently post-processed (e.g., scaled, filtered, boosted, etc.).

Synchro-to-digital and digital-to-synchro converters, while widely-used in some control applications, are not included within the scope of this chapter. Some relevant material on this topic will be found in the applications chapters of Part 1.

DIGITAL QUANTITIES

Digital numbers are represented by the presence or absence of essentially fixed voltage levels referred to “ground,” either occurring at the outputs of logic gates, or applied to their inputs. The digital numbers used are all basically binary. That is, each “bit,” or unit of information has one of two possible states. These states are “off,” “false,” or “0,” and “on,” “true,” or “1.” *Words*, groups of levels representing digital numbers, may appear simultaneously in *parallel*, on groups of gate inputs or outputs, *serially* (or in a time sequence) on a single line,¹ or in a serial-parallel combination (e.g. “*byte-serial*”).

¹In serial data transmission, if the levels return to ground between successive bits, they are denoted RZ (return-to-zero); if they change only when the leading edge of a clock pulse is present, and remain until the next leading edge, they are denoted NRZ (non-return-to-zero).

The most widely-used choice of levels at this writing, applicable to the class of products to which this book is devoted (i.e., converters manufactured by Analog Devices), are those used in TTL (transistor-transistor logic), in which positive true, or “1” corresponds to a minimum output level of +2.4V (inputs respond unequivocally to “1” for levels greater than 2.0V); and false, or “0” corresponds to a maximum output level of +0.4V (inputs respond unequivocally to “0” for anything less than +0.8V). A unique parallel or serial grouping of digital levels, or a *number*, or *code*, is assigned to each analog level which is quantized (i.e., represents a unique portion of the analog range). A typical digital code would be this array:

1 0 1 1 1 0 1 0 1

It is composed of nine bits. The “1” at the extreme left is called the “most significant bit” (MSB, or Bit 1), and the one at the right is called the “least significant bit” (LSB, or bit *n*: 9 in this case). The meaning of the code, either as a number, or as a representation of an analog variable, is unknown until the *code* and the *conversion relationship* have been defined.

THE BINARY CODE

The best-known code is *natural binary*. In a natural binary fractional code having *n* bits, the MSB has a weight of 1/2: (2^{-1}), the second bit has a weight of 1/4: (2^{-2}), and so forth down to the LSB, which has a weight of 2^{-n} . The value of a binary number is obtained by adding up the weights of all non-zero bits. As an example, Table 1 lists the 16 permutations of 4-bits’ worth of 1’s and 0’s, with their binary weights, and the equivalent numbers expressed as both decimal and binary fractions.

Decimal Fraction	Binary Fraction	Code			
		MSB (x1/2)	Bit 2 (x1/4)	Bit 3 (x1/8)	Bit 4 (x1/16)
0	0.0000	0	0	0	0
1/16 = 2^{-4} (LSB)	0.0001	0	0	0	1
2/16 = 1/8	0.0010	0	0	1	0
3/16 = 1/8 + 1/16	0.0011	0	0	1	1
4/16 = 1/4	0.0100	0	1	0	0
5/16 = 1/4 + 1/16	0.0101	0	1	0	1
6/16 = 1/4 + 1/8	0.0110	0	1	1	0
7/16 = 1/4 + 1/8 + 1/16	0.0111	0	1	1	1
8/16 = 1/2 (MSB)	0.1000	1	0	0	0
9/16 = 1/2 + 1/16	0.1001	1	0	0	1
10/16 = 1/2 + 1/8	0.1010	1	0	1	0
11/16 = 1/2 + 1/8 + 1/16	0.1011	1	0	1	1
12/16 = 1/2 + 1/4	0.1100	1	1	0	0
13/16 = 1/2 + 1/4 + 1/16	0.1101	1	1	0	1
14/16 = 1/2 + 1/4 + 1/8	0.1110	1	1	1	0
15/16 = 1/2 + 1/4 + 1/8 + 1/16	0.1111	1	1	1	1

Table 1. Fractional binary codes.

When all bits are “1” in natural binary, the number value is $1 - 2^{-n}$, or normalized full-scale less 1 LSB ($1 - 1/16 = 15/16$ in the example). Strictly speaking, the number that is represented, written with an “integer point,” is 0.1111 (= $1 - 0.0001$). However, it is almost universal practice to write the code simply as the integer 1111 (i.e., “15”) with the fractional nature of the corresponding number understood [“1111” → $1111/(1111 + 1)$, or $15/16$].

For convenience, Table 2 lists bit weights in binary, for numbers having up to 20 bits. The practical range for the vast majority of applications is about 16 bits; for larger numbers of bits than 20, continue to divide by 2.

BIT	2^{-n}	$1/2^n$ (Fraction)	"dB"	$1/2^n$ (Decimal)	%	ppm
FS	2^0	1	0	1.0	100	1,000,000
MSB	2^{-1}	1/2	-6	0.5	50.	500,000
2	2^{-2}	1/4	-12	0.25	25	250,000
3	2^{-3}	1/8	-18.1	0.125	12.5	125,000
4	2^{-4}	1/16	-24.1	0.0625	6.2	62,500
5	2^{-5}	1/32	-30.1	0.03125	3.1	31,250
6	2^{-6}	1/64	-36.1	0.015625	1.6	15,625
7	2^{-7}	1/128	-42.1	0.007812	0.8	7,812
8	2^{-8}	1/256	-48.2	0.003906	0.4	3,906
9	2^{-9}	1/512	-54.2	0.001953	0.2	1,953
10	2^{-10}	1/1,024	-60.2	0.0009766	0.1	977
11	2^{-11}	1/2,048	-66.2	0.00048828	0.05	488
12	2^{-12}	1/4,096	-72.2	0.00024414	0.024	244
13	2^{-13}	1/8,192	-78.3	0.00012207	0.012	122
14	2^{-14}	1/16,384	-84.3	0.000061035	0.006	61
15	2^{-15}	1/32,768	-90.3	0.0000305176	0.003	31
16	2^{-16}	1/65,536	-96.3	0.0000152588	0.0015	15
17	2^{-17}	1/131,072	-102.3	0.00000762939	0.0008	7.6
18	2^{-18}	1/262,144	-108.4	0.000003814697	0.0004	3.8
19	2^{-19}	1/524,288	-114.4	0.000001907349	0.0002	1.9
20	2^{-20}	1/1,048,576	-120.4	0.0000009536743	0.0001	0.95

TABLE 2. Binary bit weights or resolution.

The weight assigned to the LSB is the *resolution* inherent in numbers having n bits. The "dB" column represents the logarithm (base 10) of the ratio of the LSB value to unity (full scale), multiplied by 20, in the popular manner. Each successive power of 2 represents a change of 6.02dB [i.e., $20 \log_{10} (2)$] or "6dB/octave."

In natural binary, the normalized numerical value of the code 1 0 1 1 1 0 1 0 1, a 9-bit code, would be

$$\begin{array}{rcl}
 0.5000 \text{ MSB} & 1/2 & = 256/512 \\
 0.1250 \text{ Bit 3} & 1/8 & = 64/512 \\
 0.0625 \text{ Bit 4} & 1/16 & = 32/512 \\
 0.0312 \text{ Bit 5} & 1/32 & = 16/512 \\
 0.0078 \text{ Bit 7} & 1/128 & = 4/512 \\
 \underline{+0.0020 \text{ Bit 9 (LSB)}} & 1/512 & = \underline{+ 1/512} \\
 0.7285 & & 373/512 = 0.7285
 \end{array}$$

Bit numbering in some purely numerical devices, such as microprocessors, may be based on whole numbers, instead of binary fractions. In such systems, the LSB is always Bit 0 (viz., 2^0), the MSB is always Bit $n - 1$ (viz., 2^{n-1}), and the value of a binary number, normalized to full scale, is the integer value, divided by 2^n . An example of this approach can be found in Chapter I-4, in the section on interfacing converters with microprocessors.

BASIC CONVERSION RELATIONSHIPS

Perhaps the most fruitful way of indicating the relationship between analog and digital quantities involved in a conversion is to plot a graph. Since there are two complementary conversion relationships to be discussed, two graphs must be plotted, one for A/D conversion, the other for D/A conversion.

Figure 1 shows the graph for an ideal 3-bit D/A converter. A 3-bit converter has 8 dis-

crete coded levels, thus a total of 8 different inputs and 8 corresponding outputs, ranging from zero to 7/8 of "ful scale." Since no other levels can exist with this coding, it is plotted as a bar graph.

In practical D/A converters, the zero bar may not exactly zero (offset error). The range from zero to 7/8 F.S. may not be exactly as specified (gain error), the differences in heights of the bars may not be equal or changing uniformly (nonlinearity), and – in fact – if the nonlinearity is great enough, one or more values of analog output may be less than the values corresponding to codes having smaller weight (non-monotonic due to excessive *differential nonlinearity*). These errors (and others), the means of specifying and testing them, and some of the design techniques for keeping them small, are discussed in chapters II-2, II-3, II-4, and II-5.

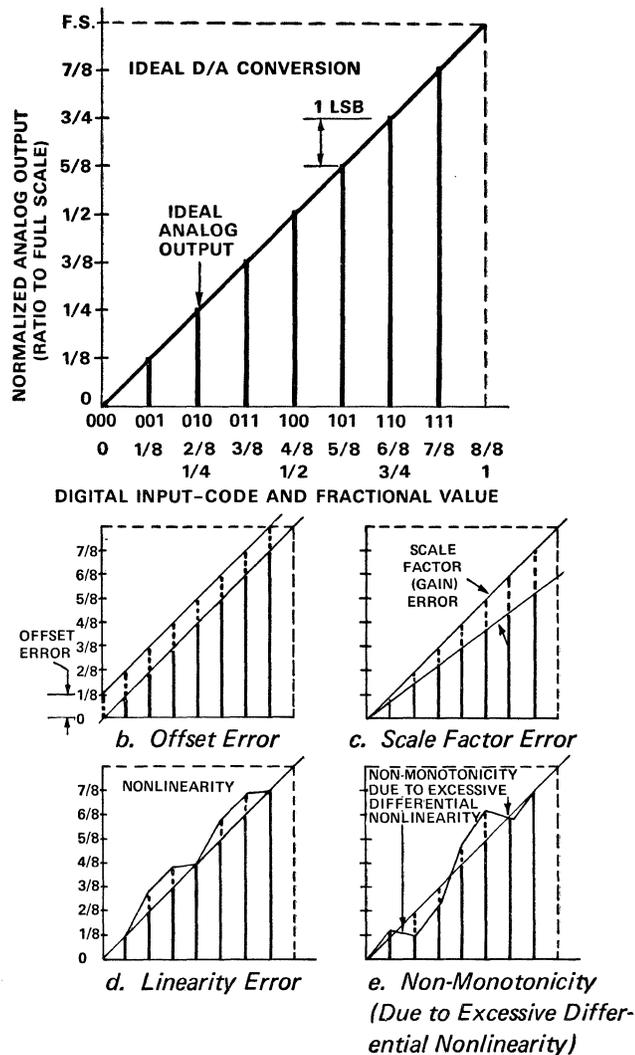


Figure 1. Conversion relationship in a 3-bit D/A converter
 a. Ideal relationship
 b, c, d, e. Typical sources of error

To visualize the ideal performance of converters having larger numbers of bits, one may intensify this pattern by interpolating additional bars between the bars on this graph. For example, a fourth bit would require 8 additional bars with heights halfway between the levels indicated. The value of the LSB would be F.S./16, and the maximum value would be $7/8 + 1/16 = 15/16$ F.S. The next bit would interpolate 16 additional bars, the new LSB would be F.S./32, and the maximum value would be $31/32$, etc. The straight line connecting the tops of the bars is the locus of the *envelope* of the ideal conversion relationship.

Figure 2 shows the graph for an ideal 3-bit A/D converter. Since all values of the analog input are presumed to exist, they must be *quantized* by partitioning the continuum into 8 discrete ranges. All analog values within a given range are represented by the same digital code, which corresponds to the nominal mid-range value. These mid-range values correspond to the bar heights of the D/A converter.

There is, therefore, in the A/D conversion process, an inherent *quantization uncertainty* of $\pm 1/2$ LSB, in addition to the conversion errors analogous to those existing for the D/A converter. The only sure way to reduce this quantization uncertainty is to increase the number of bits. (There are, of course, statistical interpolation tricks that may be performed in the digital processing or in analog filtering following subsequent D/A conversion, which will fill in missing analog values for large, rapidly-varying signals, but they will do nothing to indicate the variations within a quantum for an apparently-constant digital number.)

Since it is easier* to determine the location of a *transition* than it is to determine a mid-range value, errors and settings of A/D converters are defined and measured in terms of the analog values at which transitions occur, in relation to the ideal transition values. Like D/A converters, A/D converters have offset error: the first transition may not occur at exactly $+1/2$ LSB; scale-factor (or gain) error: the difference between the values at which the first transition and the last transition occur is not equal to $(F.S. - 2LSB)$; and *linearity* error: the differences between transition values are not all equal or uniformly changing. If the *differential linearity* error is large enough, it is possible for one or more codes to be missed (the counterpart of non-monotonic D/A conversion).

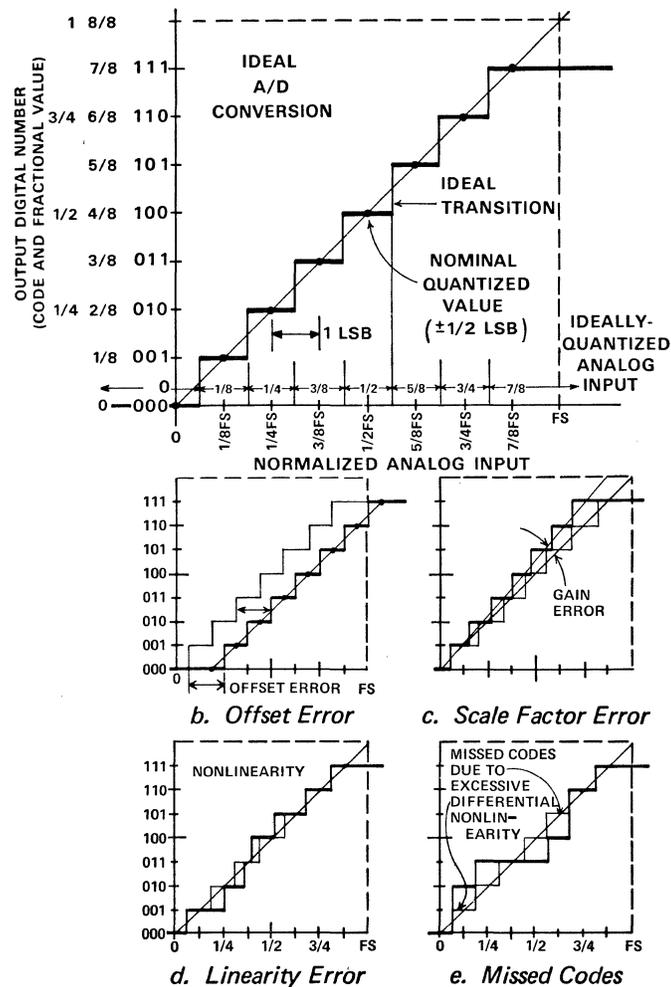


Figure 2. Conversion relationship in 3-Bit A/D converter
a. Ideal relationship b, c, d, e Typical sources of error.

*(using analog techniques)

An important factor in the conversion relationship is the choice of "Full Scale," the LSB magnitude, and the transition points. For a great many converters, full scale is in the vicinity of 10 volts: either exactly 10V or 10.24V. For 10V, the bit values are easily expressed as negative powers of 2, multiplied by 10; for 10.24V, the LSB can be expressed in "round" numbers, being a multiple or submultiple of 10mV.

Table 3 lists the LSB values, the "all 1's" value (i.e., F.S. - 1 LSB), and the A/D converter transition values at 1/2 LSB (for zero adjustment) and all 1's (F.S. - 1/2 LSB, for scale factor adjustment) for resolutions to 2^{-20} , for both 10V and 10.24V full scale. If full scale is 5V (also a popular value), simply divide the appropriate numbers by 2.

No. of Bits <i>n</i>	10V Full Scale				10.24V Full Scale			
	LSB	All 1's (Volts)	A/D Transitions		LSB	All 1's (Volts)	A/D Transitions	
			To LSB (1/2 LSB)(Volts)	To All 1's (Volts)			To LSB (+1/2 LSB)(Volts)	To All 1's (Volts)
1	5V	5.0	2.5V	2.5	5.12V	5.12	2.56V	2.56
2	2.5V	7.5	1.25V	6.25	2.56V	7.68	1.28V	6.40
3	1.25V	8.75	625mV	8.13	1.28V	8.96	640mV	8.32
4	625mV	9.38	312mV	9.07	640mV	9.60	320mV	9.28
5	312mV	9.69	156mV	9.53	320mV	9.92	160mV	9.76
6	156mV	9.84	78.1mV	9.76	160mV	10.08	80mV	10.00
7	78.1mV	9.92	39.1mV	9.88	80mV	10.16	40mV	10.12
8	39.1mV	9.961	19.5mV	9.941	40mV	10.20	20mV	10.18
9	19.5mV	9.980	9.77mV	9.970	20mV	10.220	10mV	10.21
10	9.77mV	9.990	4.88mV	9.985	10mV	10.230	5mV	10.225
11	4.88mV	9.9951	2.44mV	9.9927	5mV	10.235	2.5mV	10.232
12	2.44mV	9.9976	1.22mV	9.9964	2.5mV	10.2375	1.25mV	10.2362
13	1.22mV	9.9988	610μV	9.9982	1.25mV	10.2388	625μV	10.2382
14	610μV	9.9994	305μV	9.9991	625μV	10.2394	312μV	10.2391
15	305μV	9.99970	153μV	9.99955	312μV	10.23969	156μV	10.23953
16	153μV	9.99985	76μV	9.99977	156μV	10.23984	78.1μV	10.23976
17	76μV	9.99992	38μV	9.99988	78.1μV	10.23992	39.1μV	10.23988
18	38μV	9.999962	19μV	9.999943	39.1μV	10.239961	19.5μV	10.239941
19	19μV	9.999981	9.5μV	9.999971	19.5μV	10.239980	9.77μV	10.239970
20	9.5μV	9.999990	4.8μV	9.999985	9.77μV	10.239990	4.88μV	10.239985

Table 3. LSB and (FS - LSB) values for 10V and 10.24V conversion.

OTHER CODES

Although binary is the most commonly-used code, there are a number of other popular codes used at system interfaces, depending on signal range and polarity, conversion technique, specially desired characteristics, and origin or destination of digital information.

BINARY-CODED DECIMAL (BCD)

This is a code in which each decimal digit is represented by a group of 4 binary-coded digits. The LSB of the most significant group, or "quad," had a weight of 0.1, the LSB of the next has a weight of 0.01, the LSB of the next has a weight of 0.001, etc. Each quad has 10 permissible levels with weights 0 to 9. Group values in excess of 9 are not permitted. For example, Table 4 shows BCD coding for a variety of numbers between 0 and 0.99.

A/D converters with the BCD code are used primarily in digital voltmeters and panel meters, since each quad's output may be decoded to drive a numeric display using the familiar decimal numbers. If the display is of a BCD digitally transmitted or processed number, or if the input is via a thumbwheel switch, a D/A converter that responds to BCD may be used to furnish an analog output from the same digital input.

BCD is somewhat wasteful, in the sense that each BCD quad has 10/16 the resolution of a comparable natural binary quad. Table 5 shows the relative resolution capability.

Decimal Fraction	BCD Code	
	MSQ (x1/10)	2nd Quad (x1/100)
	x8 x4 x2 x1	x8 x4 x2 x1
0.00 = 0.00 + 0.00	0 0 0 0	0 0 0 0
0.01 = 0.00 + 0.01	0 0 0 0	0 0 0 1
0.02 = 0.00 + 0.02	0 0 0 0	0 0 1 0
0.03 = 0.00 + 0.03	0 0 0 0	0 0 1 1
0.04 = 0.00 + 0.04	0 0 0 0	0 1 0 0
0.05 = 0.00 + 0.05	0 0 0 0	0 1 0 1
0.06 = 0.00 + 0.06	0 0 0 0	0 1 1 0
0.07 = 0.00 + 0.07	0 0 0 0	0 1 1 1
0.08 = 0.00 + 0.08	0 0 0 0	1 0 0 0
0.09 = 0.00 + 0.09	0 0 0 0	1 0 0 1
0.10 = 0.10 + 0.00	0 0 0 1	0 0 0 0
0.11 = 0.10 + 0.01	0 0 0 1	0 0 0 1
:		
0.20 = 0.20 + 0.00	0 0 1 0	0 0 0 0
:		
0.30 = 0.30 + 0.00	0 0 1 1	0 0 0 0
:		
0.90 = 0.90 + 0.00	1 0 0 1	0 0 0 0
0.91 = 0.90 + 0.01	1 0 0 1	0 0 0 1
:		
0.98 = 0.90 + 0.08	1 0 0 1	1 0 0 0
0.99 = 0.90 + 0.09	1 0 0 1	1 0 0 1

Table 4. Examples of 2-digit BCD weighting.

Number of Bits	Least Significant Bit		Number of Binary Bits Needed For Same Resolution as BCD
	Binary	BCD	
4	0.062	0.1	4
8	0.0039	0.01	7
12	0.00024	0.001	10
16	0.000015	0.0001	14
20	0.000001	0.00001	17
24	0.0000002	0.000001	20

Table 5. Relative resolution of BCD and binary.

OVERRANGING

Many BCD A/D converters have an additional bit with weight equal to full scale, in a position “more significant” than the MSB.

This additional bit provides a maximum of 100% “overrange” capability. Additional “super-significant” bits would provide binary 300% (2 bits) and 700% (3 bits) overrange capability (or extend the range to nearly 800% of the BCD “full scale.”) The overrange bit is most commonly used in digital voltmeters and panel meters to indicate that nominal full scale has been exceeded and that the visual reading may be erroneous.

Overrange bits need not be restricted to BCD. They are useful as “flags” in any conversion process for which an overrange input would give an ambiguous reading, or where an overrange input indicates anomalous analog system behavior. The overrange bit must of course be of suitable accuracy, since it is, in effect, the MSB.

2-4-2-1 BINARY-CODED DECIMAL

This is a code that is still in use, in which the bit in the MSB position in each quad has a weight of 2 instead of the usual 8 that is normal for BCD. It is found, for example, at

the digital output of some older Hewlett-Packard digital voltmeters. The relative weights within a quad are given in Table 6.

	2 [☆] (x2)	4 (x4)	2 (x2)	1 (x1)
0.0	0	0	0	0
0.1 = 0.1	0	0	0	1
0.2 = 0.2	0	0	1	0
0.3 = 0.1 + 0.2	0	0	1	1
0.4 = 0.4	0	1	0	0
0.5 = 0.1 + 0.4	0	1	0	1
0.6 = 0.2 + 0.4	0	1	1	0
0.7 = 0.1 + 0.2 + 0.4	0	1	1	1
0.8 = 0.2 + 0.4 + 0.2	1	1	1	0
0.9 = 0.1 + 0.2 + 0.4 + 0.2	1	1	1	1

Table 6. 2-4-2-1 BCD bit weights within each quad.

This code was more economical to implement in the days before integrated-circuit logic became common, still has the advantages of having all 1's for (full scale – LSB) and requiring a smaller range of resistance in D/A-converter ladder networks based on binary conductance values.

GRAY CODE

This is a binary code in which the bit position does not signify a numerical weighting; however, in converters using it, each code still corresponds to a unique portion of the analog range. It is easily translatable into natural binary (Table7):

Decimal Fraction	Gray Code				Binary Code			
0	<u>0</u>	0	0	0	0	0	0	0
1/16	0	0	0	<u>1</u>	0	0	0	1
2/16	0	0	<u>1</u>	1	0	0	1	0
3/16	0	0	1	<u>0</u>	0	0	1	1
4/16	0	<u>1</u>	1	0	0	1	0	0
5/16	0	1	1	<u>1</u>	0	1	0	1
6/16	0	1	<u>0</u>	1	0	1	1	0
7/16	0	1	0	<u>0</u>	0	1	1	1
8/16	<u>1</u>	1	0	0	1	0	0	0
9/16	1	1	0	<u>1</u>	1	0	0	1
10/16	1	1	<u>1</u>	1	1	0	1	0
11/16	1	1	1	<u>0</u>	1	0	1	1
12/16	1	<u>0</u>	1	0	1	1	0	0
13/16	1	0	1	<u>1</u>	1	1	0	1
14/16	1	0	<u>0</u>	1	1	1	1	0
15/16	1	0	0	<u>0</u>	1	1	1	1

Table 7. Comparison of 4-Bit binary and Gray codes. Underlined bits indicate changes as number increases.

In Gray code, as the number value changes, the transitions from one code to the next involve only one bit at a time. The bits that change as the numbers increase are underlined in the table.

The conversion from binary to Gray code occurs as follows: If the binary MSB is zero, the Gray code MSB will be zero. Then, continuing to read from MSB to LSB, each change produces a "1," each non-change produces a "0." For example, .11 in binary, 1011, becomes 1110 in Gray code (1 → 1, 1-to-0 → 1, 0-to-1 → 1, 1-to-1 → 0). Another example: the 12-bit binary number 101111000101 becomes 111000100111. Fig. 3 shows one way in which binary to Gray code conversion may be mechanized.

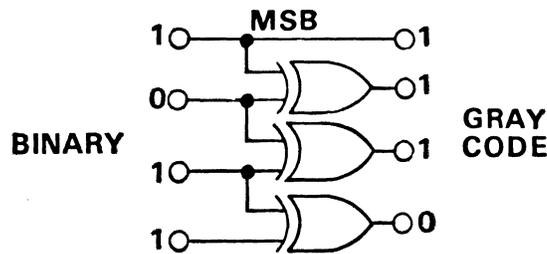


Figure 3. Binary to Gray code conversion using exclusive – or gates.

The conversion from Gray code to binary is just the reverse of the conversion from binary to Gray code: The binary MSB will be the same as the Gray code MSB. Then, continuing to read from MSB to LSB, if the next bit is 1, the next binary bit is the complement of the previous binary bit. For example, if the Gray code is 1110, the corresponding binary is 1011 (1 → 1, 1 → 1-to-0, 1 → 0-to-1, 0 → 1-to-1). Another example, the 8-bit Gray code 01110000 is 01011111 in binary. A mechanization of Gray code-to-binary conversion appears in Figure 4.

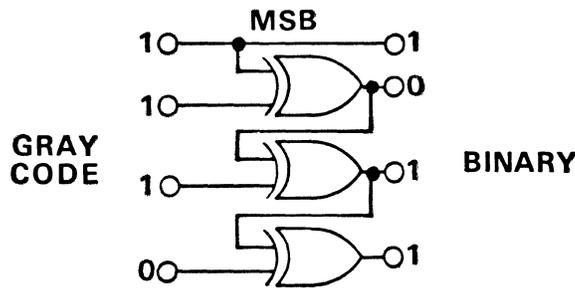


Figure 4. Gray code to binary conversion.

Gray code is useful for shaft encoders (angle-to-digital converters) because the change of only 1 bit for each increment eliminates false intermediate codes that could occur in natural binary conversion. Here, for comparison, are Gray code and binary developed optical shaft encoders for 4-bit resolution.

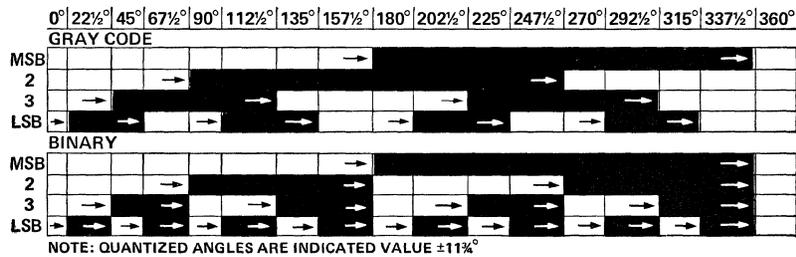


Figure 5. Gray vs. binary encoding.

Note that, with the Gray code converter, there is only one bit-change at each transition. If the edge of a shaded area is slightly out of line, the coding will be in error by a small fraction of an LSB. In the binary converter, *all four bits change at once* at the 180° and 360° transitions. If bit 2's shaded area were to end a little to the left of the 180° transition, the code, in a small region, would be 0011, indicating the 67½° range, or a fictitious progression from 157½° to 67½° to 180°. We leave the catastrophic implications of this to the reader.

The shaft encoder is a *simultaneous* converter: all bits appear at once and can be read in parallel at any time. There is an electrical equivalent form of simultaneous A/D converter having a Gray code output. It employs a chain of biased comparators, the outputs of which provide a quantized indication of the analog input level: all comparators above it

are 0, all comparators below it are 1. Multi-input logic gates then make the decisions necessary to obtain a parallel Gray code output. Such converters are quite fast, some being capable of producing 10M meaningful conversions per second, but they require a number of comparisons that is a geometric function of the required resolution, (i.e., $2^n - 1$), as well as logic gates having large numbers of inputs.

A variation of this scheme, the cyclical converter, which also has Gray code output, uses fewer comparators, with more-accurate output states, but it requires more time to perform the conversion. It continuously tracks the analog input.

The use of Gray code in fast converters that provide continuous conversions has the same rationale as for the shaft encoder. Any Gray code output value that is latched into a register will always be within ± 1 LSB of the correct value, even if the latching occurs just as a bit is switching. With binary, however, where many bits can switch at a single transition, it is possible to latch in mid-flight, and, because of the "skew" between turn-on and turn-off speeds, lock in an utterly false code.

COMPLEMENTARY CODES

The actual mechanization of some forms of converters, (for example, D/A converters using monolithic quad current switches) may require codes, such as natural binary or BCD, in which all bits are represented by their complements. Such codes are called complementary codes.

In a 4-bit complementary-binary converter, 0 is represented by 1111, half-scale (MSB) by 0111, and full scale (less 1LSB) by 0000. It can be easily obtained from the " \bar{Q} " outputs of a register, of which "Q" is the normal output sense.

Similarly, for each quad of a BCD-coded converter, *complementary* BCD is the code obtained by representing all bits by their complements. In complementary BCD, 0 is represented by 1111, and 9 is represented by 0110. As an example, Table 8 lists the equivalents for 1 through 11 in complementary binary and complementary BCD (with overrange bit).

Decimal	Natural Binary	Complementary Binary	Complementary BCD
0	0000	1111	0000
1	0001	1110	0001
2	0010	1101	0010
3	0011	1100	0011
4	0100	1011	0100
5	0101	1010	0101
6	0110	1001	0110
7	0111	1000	0111
8	1000	0111	0100
9	1001	0110	0101
10	1010	0101	1000
11	1011	0100	1001

Conversion Relationship of Ideal 3-Bit Complementary Binary D/A Converter

Table 8. Complementary codes.

If a natural binary input were applied to a D/A converter coded to respond to complementary binary, the output would be in reverse order, i.e., zero output for all 1's, and F.S. - 1 LSB for all 0's.

The complementary codes discussed above involve complementing *all bits*, for convenience in implementing the conversion relationship using certain kinds of switches (i.e., those that respond to complementary logic). We could just as well have left the logic unchanged but redefined it as "negative true." However, for consistency in elucidation, we define all logic in terms of "positive true" TTL (or DTL), as explained at the beginning of the

chapter. It is important to understand that, for purposes of this discussion, these complementary codes have nothing to do with representation of the *analog polarity* relationship, a matter that will be discussed next.

ANALOG POLARITY

So far, the conversion relationships mentioned have been unipolar: the codes have represented numbers, which in turn represent the normalized *magnitudes* of analog variables,² without regard to polarity. A unipolar A/D converter will respond to analog signals of only one polarity, and a unipolar D/A converter will produce analog signals of only one polarity.

The analog signal polarity is determined either by using a converter whose reference and switches (or specifications) are compatible with the desired analog polarity, or (if for reasons of economy or availability, a converter is available having predetermined polarity) by operating on the analog signal before A/D conversion – or after D/A conversion – to invert its polarity, and also perform any necessary scale changes, if range must be adapted too.

BIPOLAR CODES

For conversion of bipolar analog signals into a digital code that retains sign information, one extra bit – the “sign bit” – is necessary. This “most significant bit” doubles the analog range and halves the peak-to-peak resolution. In some cases, the sign bit is provided by re-interpreting the existing MSB, in which event the analog *range* may still be doubled, but the *resolution* is twice as coarse. For example, if a 10-bit converter’s resolution is 1/1024, for the range 0-10V, we may use a bipolar code having 11 bits, with peak-to-peak resolution of 1/2048 and range of ±10V, or retain a code having 10 bits, but “stretch” the range to ±10V, in which case the peak-to-peak resolution remains 1/1024, which doubles the magnitude of the LSB. It must be emphasized that, because the sign digit doubles both the range *and* the number of levels, the LSB’s ratio to full scale in either polarity is $2^{-(n-1)}$, not 2^{-n} .

The most-often-used binary codes in bipolar conversion are: Sign-magnitude (magnitude plus sign), Offset binary, Two’s complement, and One’s complement. Table 9 shows each of these codes expressed for 4 bits (3 bits plus sign).

Number	Decimal Fraction		Sign + Magnitude	Two’s Complement	Offset Binary	One’s Complement
	Positive Reference	Negative Reference				
+7	+7/8	-7/8	0 1 1 1	0 1 1 1	1 1 1 1	0 1 1 1
+6	+6/8	-6/8	0 1 1 0	0 1 1 0	1 1 1 0	0 1 1 0
+5	+5/8	-5/8	0 1 0 1	0 1 0 1	1 1 0 1	0 1 0 1
+4	+4/8	-4/8	0 1 0 0	0 1 0 0	1 1 0 0	0 1 0 0
+3	+3/8	-3/8	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1
+2	+2/8	-2/8	0 0 1 0	0 0 1 0	1 0 1 0	0 0 1 0
+1	+1/8	-1/8	0 0 0 1	0 0 0 1	1 0 0 1	0 0 0 1
0	0+	0-	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0
0	0-	0+	1 0 0 0	(0 0 0 0)	(1 0 0 0)	1 1 1 1
-1	-1/8	+1/8	1 0 0 1	1 1 1 1	0 1 1 1	1 1 1 0
-2	-2/8	+2/8	1 0 1 0	1 1 1 0	0 1 1 0	1 1 0 1
-3	-3/8	+3/8	1 0 1 1	1 1 0 1	0 1 0 1	1 1 0 0
-4	-4/8	+4/8	1 1 0 0	1 1 0 0	0 1 0 0	1 0 1 1
-5	-5/8	+5/8	1 1 0 1	1 0 1 1	0 0 1 1	1 0 1 0
-6	-6/8	+6/8	1 1 1 0	1 0 1 0	0 0 1 0	1 0 0 1
-7	-7/8	+7/8	1 1 1 1	1 0 0 1	0 0 0 1	1 0 0 0
-8	-8/8	+8/8		(1 0 0 0)	(0 0 0 0)	

Table 9. Commonly-used bipolar codes.

²Gray code is an exception. Since it is not quantitatively weighted, it can represent any arbitrary range of magnitudes of any polarity.

Because the analog signal now has a choice of polarity, we must be careful about the relationship between the code and the polarity of the analog signal. "Positive reference" indicates that the analog signal³ increases positively as the digital number increases. "Negative reference," on the other hand, indicates that the analog signal decreases towards negative full scale as the digital number increases. Conversion relationships for bipolar A/D and D/A converters are shown graphically in Figures 6 and 7.

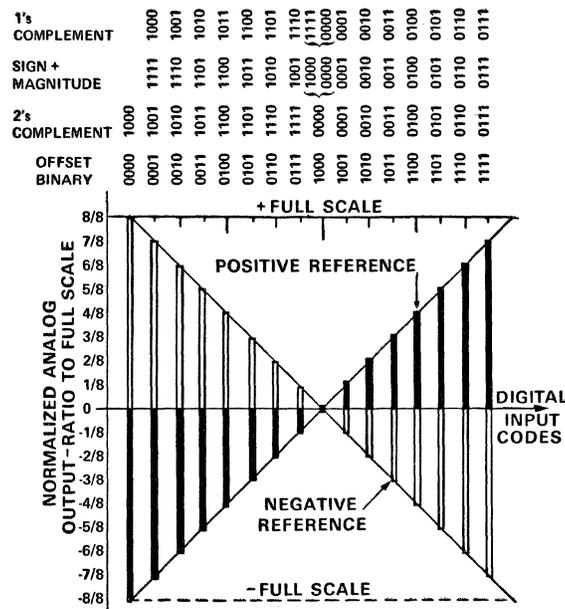


Figure 6. Ideal D/A conversion relationship for 4-bit (3-bit-plus-sign) offset binary, 2's complement, sign-magnitude, 1's complement codes.

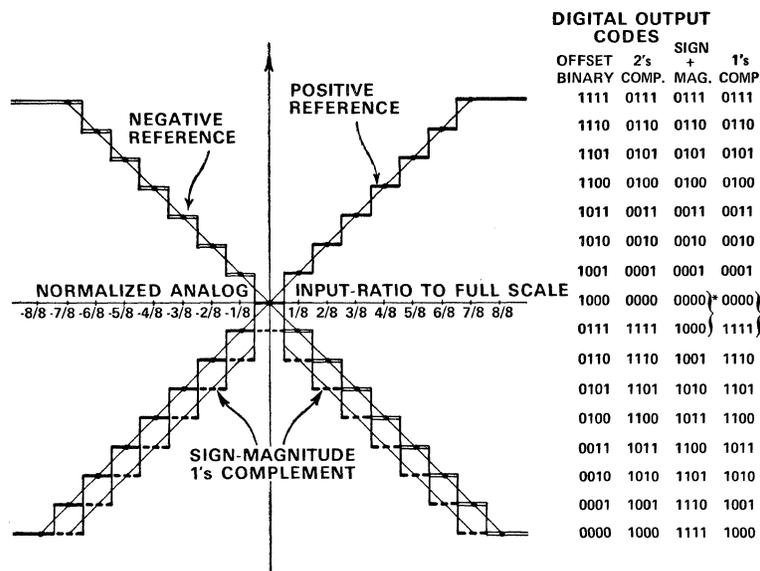


Figure 7. Ideal A/D conversion relationship for 4-bit (3-bit-plus-sign) offset binary, 2's complement, sign magnitude, 1's complement codes.

Sign-Magnitude would appear to be the most straightforward way of expressing signed analog quantities digitally. Simply determine the code appropriate for the magnitude and add a polarity bit. It is used advantageously in D/A converters that operate in the vi-

³A/D converter input or D/A converter output.

*In sign-magnitude and 1's-complement A/D converters, the ambiguous zero must be dealt with. In some units, one of the codes is "forbidden," (DVM's generally read "+0" only), in others, the $\pm 1/2$ LSB zero region is divided into two regions (0 to $+1/2$ LSB, and 0 to $-1/2$ LSB), one of which produces one code, the other the other code. This is a more useful approach in codes having a sequential continuum of numbers, such as a 1's complement.

cinity of zero, where the application calls for smooth and linear transitions from positive small voltages to negative small voltages. As can be seen in the example in the table, it is the only code for which the three magnitude bits do not have a major transition (all 1's to all 0's, or equivalent) at zero. Sign-magnitude BCD is almost universally used for bipolar digital voltmeters (A/D converters).

It does have some shortcomings, though. In data-processing applications, the *other* codes are more-readily usable for computation with a minimum of translation. One of its problems is that it has two codes for zero. For this reason, sign-magnitude is harder to interface with digitally, because it requires either software, or additional equipment. In addition, the converter circuitry for sign-magnitude is usually somewhat more complicated and costly than for some other codes.

Offset binary is the easiest code to embody with converter circuitry. An examination of the offset binary code for three bits plus sign will show that it is really a natural binary code for four bits, except that its zero is at negative full scale, the LSB is 1/16 of the bipolar range, and the MSB is turned on at analog zero. Therefore, to make an offset binary 3-bits-plus sign converter out of a 4-bit D/A converter having 0-to-10V full-scale range, we have only to double its scale factor (20V range), and offset its zero by one half of the full range (-10V), an operation which is neither difficult nor expensive. Similarly, for an A/D converter, one would attenuate the input by one-half, and add a bias of one-half the full range.

Besides its ease of implementation, offset binary has the further advantage that it is compatible with computer inputs and outputs, it is easily changed to the more-computationally useful two's complement (just complement the MSB), and it has a single unambiguous code for zero. The all-zeros negative full scale code (0000), though not used in computing (because $-(F.S. - 1 \text{ LSB})$ is the most negative value defined in computing), is nevertheless useful as a converter checking and adjustment code.

The principal drawback of offset binary is that a major bit transition occurs at 0 (all bits change, from 0111 to 1000). This can lead to "glitch" problems dynamically (the difference in speed between bits turning on and off can lead to large spikes) and to linearity problems statically (the largest linearity errors are most likely to occur at major transitions, because the transition is essentially a difference between two large numbers). Also, in offset binary, zero errors may be greater than with sign-magnitude, because the zero analog level is usually obtained by taking a difference between the MSB ($\frac{1}{2}$ full range) and a bias ($\frac{1}{2}$ full range), again, two large numbers.

Two's complement, for conversion purposes, consists of a binary code for positive magnitudes (0 sign bit), and the two's complement of each positive number to represent its negative. The two's complement is formed arithmetically by complementing the number and adding 1 LSB. For example, the two's complement of 3/8 (0011) would be its complement plus 1 LSB, or $1100 + 0001 = 1101$.

Two's complement is a useful code computationally because it can be thought of as a set of negative numbers. Therefore, addition can be used instead of subtraction. For example, to subtract 3/8 from 4/8, add 4/8 to -3/8, or 0100 to 1101. The result is 0001 (disregarding the extra carry), or 1/8.

If the two's complement code and the offset binary code are compared, it can be seen that the only difference between them is that the MSB of one is replaced by its complement in the other (Nature's way of helping converter manufacturers and users). Since both a digit and its complement are available from most flip-flops, an offset-binary-coded converter may be used for 2's complement, just by using the MSB's complement at the output of an A/D converter or at the output of a D/A converter's input register. And vice versa.

Two's complement has the same disadvantages as offset binary, since the conversion process is identical.

One's complement is a means of representing negative numbers sometimes used by computers. One's complement is obtained arithmetically by simply complementing all of a number's digits. Thus, the one's complement of 3/8 (0011) is (1100). When a number is subtracted by adding its 1's complement, the extra carry (that is disregarded in 2's complement), if present, cause 1 LSB to be added to the total ("end-around carry.") Thus, subtracting 3/8 from 4/8, $0100 + 1100 = 0000 + 0001 = 0001$ (or 1/8). A one's complement code can be formed by complementing each positive value to obtain its corresponding negative value, including - alas - zero, which is then represented by two codes, 0000 and 1111.

Besides its ambiguous zero, another disadvantage of this code in conversion is that it is not as readily implemented as is 2's complement. If it is not converted to 2's complement before a D/A conversion, by adding 1 LSB digitally when the MSB is 1 (indicating a negative number), then the easiest way to implement the conversion is by performing a 2's complement conversion, and adding the *analog* value of 1LSB, if the MSB is 1. Adding the extra analog bit can be done simply and elegantly (if not accurately) by resistively dividing the digital MSB logic level down to the LSB's analog value and summing this attenuated signal.

CODE CONVERSION

Since code conversion may be desirable, either after A/D conversion or before D/A conversion, in order to make it possible to use a converter that produces the best results at the lowest cost, the matrix of Table 10 briefly outlines the relationships among the codes.

To Convert From To ↓	Sign Magnitude	2's Complement	Offset Binary	1's Complement
Sign Magnitude	NO CHANGE	If MSB = 1, complement other bits, add 00 .. 01	Complement MSB If new MSB = 1, complement other bits, add 00 .. 01	If MSB = 1, complement other bits
2's Complement	If MSB = 1, complement other bits, add 00 ... 01	NO CHANGE	Complement MSB	If MSB = 1, add 00 ... 01
Offset Binary	Complement MSB If new MSB = 0 complement other bits, add 00 ... 01	Complement MSB	NO CHANGE	Complement MSB If new MSB = 0, add 00 ... 01
1's Complement	If MSB = 1, complement other bits	If MSB = 1, add 11 ... 11	Complement MSB If new MSB = 1, add 11 ... 11	NO CHANGE

Table 10. Relations among bipolar codes.

OTHER BIPOLAR CODES

The list of bipolar codes mentioned above may seem quite complete and coherent from the tutorial point of view, but it does not fully reflect the ingenuity and diversity of the computer and converter industries. There are a number of variations in more-or-less widespread usage that should be mentioned here because they will inevitably be encountered. Fortunately, they are based on codes we have already discussed and may be easily described.

Modified sign-magnitude: This is a version of sign-magnitude in which the MSB is complemented (1 for positive, 0 for negative).

Modified one's complement: Like modified sign-magnitude, a version in which the MSB is complemented (1 for positive, 0 for negative).

Both of the above codes have polarity bits that are the same as for offset binary – which is the lone standout in Table 9. Since offset binary is popular among converter manufacturers, it stands to reason that other codings should be available with compatible sign bits, for the sake of uniformity, even though they may take us one step away from the basic natural binary rationale.

Complementary everything: All of the above-mentioned codes may be completely complemented to form complementary sign-magnitude, complementary offset binary, complementary 2's complement, and complementary 1's complement. (These are, as explained earlier in this chapter, “negative true” versions.) Such codes, although they made life a little more complex, were necessary to take advantage of some of the best monolithic switching hardware available at one time – quad current switches. Fortunately, A/D converters and D/A converters that are supplied with registers performed the complementarity internally, so that the user wasn't usually aware of the complexities that lay within.⁴ However, users of monolithic and hybrid converters without registers should be prepared to adjust their thinking (and especially their test equipment) to include the possible application of complementary codes.

For the sake of completeness, Table 11 lists the codes mentioned above, for 3-bits-plus-sign.

Number	Modified Sign-Magnitude	Modified 1's Complement	COMPLEMENTARY CODES			
			Comp. Sign-Magnitude	Comp. Offset Binary	Comp. 2's Complement	Comp. 1's Complement
+7	1 1 1 1	1 1 1 1	1 0 0 0	0 0 0 0	1 0 0 0	1 0 0 0
+6	1 1 1 0	1 1 1 0	1 0 0 1	0 0 0 1	1 0 0 1	1 0 0 1
+5	1 1 0 1	1 1 0 1	1 0 1 0	0 0 1 0	1 0 1 0	1 0 1 0
+4	1 1 0 0	1 1 0 0	1 0 1 1	0 0 1 1	1 0 1 1	1 0 1 1
+3	1 0 1 1	1 0 1 1	1 1 0 0	0 1 0 0	1 1 0 0	1 1 0 0
+2	1 0 1 0	1 0 1 0	1 1 0 1	0 1 0 1	1 1 0 1	1 1 0 1
+1	1 0 0 1	1 0 0 1	1 1 1 0	0 1 1 0	1 1 1 0	1 1 1 0
0+	1 0 0 0	1 0 0 0	1 1 1 1	0 1 1 1	1 1 1 1	1 1 1 1
0-	0 0 0 0	0 1 1 1	0 1 1 1	0 1 1 1	1 1 1 1	0 0 0 0
-1	0 0 0 1	0 1 1 0	0 1 1 0	1 0 0 0	0 0 0 0	0 0 0 1
-2	0 0 1 0	0 1 0 1	0 1 0 1	1 0 0 1	0 0 0 1	0 0 1 0
-3	0 0 1 1	0 1 0 0	0 1 0 0	1 0 1 0	0 0 1 0	0 0 1 1
-4	0 1 0 0	0 0 1 1	0 0 1 1	1 0 1 1	0 0 1 1	0 1 0 0
-5	0 1 0 1	0 0 1 0	0 0 1 0	1 1 0 0	0 1 0 0	0 1 0 1
-6	0 1 1 0	0 0 0 1	0 0 0 1	1 1 0 1	0 1 0 1	0 1 1 0
-7	0 1 1 1	0 0 0 0	0 0 0 0	1 1 1 0	0 1 1 0	0 1 1 1
-8				1 1 1 1	0 1 1 1	

Table 11. Modified and complementary bipolar codes.

ARBITRARY BIASING AND SCALING

The conversion relationships discussed so far have been either strictly one-sided (0 to full scale) or symmetrical (\pm full scale). The reason for this emphasis is that most commercially-available converters are built that way – as general-purpose devices.

However, since the principal relationship between the analog variable and the digital number is *proportionality*, the repertoire of codes corresponding to a given resolution may represent any portion of the analog voltage or current range. For example, if one wished to encode the voltage range from 4 to 7 volts in binary, using a 0–10V A/D converter, one could simply apply the voltage without any transformation, using only 0.3 of the available number of bits. However, a more efficient alternative would be to offset the input by 4 volts, amplify by 3.33, and apply the resulting 0–10V signal to the converter,

⁴Since both polarities of logic are usually available, complementary inputs (or outputs) can *simplify* loading, and wiring, and fanout problems. For example, if an A/D converter uses a conversion process involving a complementary-input D/A converter, the complementary logic outputs may be applied to the D/A converter, and the uncomplemented outputs to the outside world.

thereby making use of the entire range of available codes and improving resolution by a greater than 3. In a sense, the conversion relationship between the original input and the digital output is an *offset binary* code. The subsequent digital processing would take this transformation into account via the software.

Another sort of arbitrary scaling might result if the analog signal were proportional to a temperature range of (for example) 0° to 70°C , and one desired a direct readout of temperature on a digital voltmeter. A typical approach might be to scale the voltage directly to the temperature numbers (e.g., $10^{\circ}/\text{V}$) and apply it to a DVM, with the location of the decimal point re-interpreted. The DVM would then provide a readout in *engineering units*.

In offset binary and 2's complement coding, a converter's output is asymmetrical, because a code exists for -F.S. (i.e., -1), but not for +F.S. ($1 - 2^{-(n-1)}$ is maximum). Since a computer will not use the code for -F.S., the remaining codes are symmetrical for computing purposes, and the -F.S. code is unused, and - in effect - lost. For some purposes, such as data transmissions, it may be desirable to retain the information in *all* codes, and achieve full scale and symmetry as well. This can be accomplished by biasing the analog signal by $\text{F.S.}/(2^n - 1)$, and multiplying the reference by $1/(1 - 2^{-n})$.⁵ The only drawback of this scheme is that a D/A converter output, though providing a complete, symmetrical full-scale swing, will not have an analog zero state. (Fig. 8).

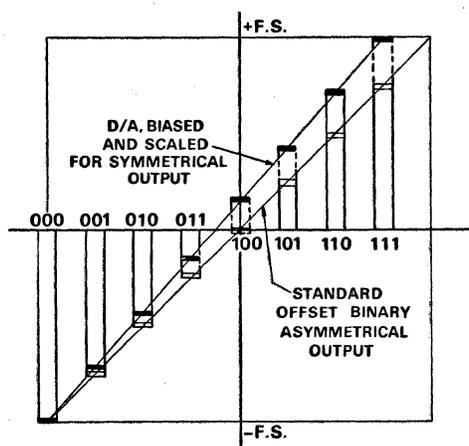


Figure 8. Conversion relationship for a 2-bit-plus-sign D/A converter biased and scaled for symmetrical analog output. Note that there is no code that gives analog zero.

DAC's AS MULTIPLIERS AND ADC's AS DIVIDERS

The D/A converter can be thought of as a digitally-controlled potentiometer that produces an analog output (voltage or current) that is a normalized fraction of its "full scale" setting. The output voltage or current depends on the reference value chosen to determine "full scale" output. If the reference may vary in response to an analog signal, the output is proportional to the product of the digital number and the analog input. The product's polarity depends on the analog signal polarity, and the digital coding and conversion relationship. 4-quadrant multiplication is available if the D/A converter accepts reference signals of both positive and negative polarities, and the digital response is bipolar. A typical conversion relationship for a 4-quadrant multiplying DAC having 3-bit-plus-sign 2's complement coding is shown in Figure 9, interpreting the Multiplying DAC as a digitally-controlled variable-gain amplifier.

In another interpretation, the envelope of the ideal bipolar D/A converter output in Figure 6 could be seen as proportional to the analog signal input, starting from full scale "Positive Reference," being attenuated as the analog signal is reduced, passing through zero, and increasing negatively to the "Negative Reference" envelope.

⁵These are b and m , respectively, in the equation $y = mx + b$.

Multiplying D/A converters may be 4-quadrant, two-quadrant (single polarity of either analog or digital variable), or one quadrant. They may even be fractional-quadrant, if the reference has a limited range of variation.

In analog-to-digital converters, the digital output number depends on the ratio of the quantized input to the "full-scale" reference. If the reference is allowed to change in response to a second analog input, the digital output will be proportional to the ratio of the analog signal to the reference signal. Thus, the "ratiometric" A/D converter can be thought of as an analog divider with digital output.

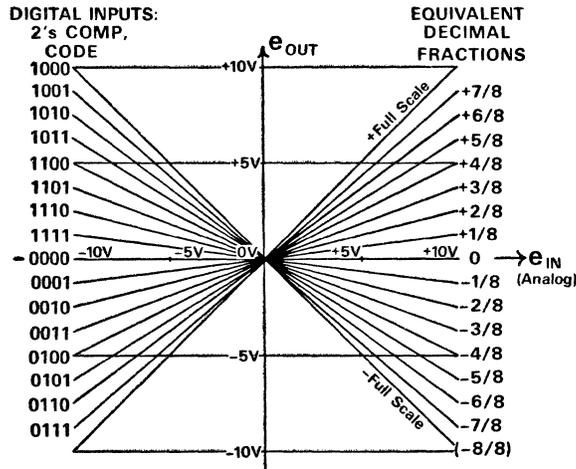


Figure 9. D/A converter as four-quadrant multiplier of analog voltage and 3-bit-plus-sign 2's complement digital number. Analog output vs. analog input as a function of digital input code.

ELECTRICAL INTERFACES WITH CONVERTERS

Converters may have associated with them six families of electrical inputs and outputs: analog signal, digital code, power, control, configuration, and reference. Table 12 indicates some of the properties of these interfaces, and the text that follows adds further detail.

	D/A Converters		A/D Converters	
ANALOG SIGNAL	Output:	Voltage or Current Polarity Magnitude	Input:	Usually Voltage Polarity Magnitude
DIGITAL CODE	Input:	Buffered or Direct Coding Logic Levels Format: Serial Parallel Byte-Serial	Output:	Coding Logic Levels Timing (Clock) Format: Serial Parallel Byte-Serial
CONTROL	Input:	Strobe(s)	Inputs:	Convert Command Enables Clock
			Outputs:	Status Overrange
CONFIGURATION	Serial/Parallel Short Cycle () Bits Address		Byte-Enable Short Cycle () Bits Address	
POWER	Analog:	Usually $\pm 15V$ or same as Digital	Analog:	Usually $\pm 15V$ or same as Digital
	Digital:	+5V (TTL) +5V to +15V (CMOS)	Digital:	+5V (TTL) +5V to +15V (CMOS) -5V to -15V (CMOS V_{SS})
REFERENCE	Internal or External Fixed or Variable Polarity		Internal or External Fixed or Variable Polarity	

Table 12. Converter interfaces.

Figure 10 is a block diagram showing typical connections to a parallel converter. There may be yet other connections, such as a clock synchronization input or output, complementary logic inputs or outputs, and connections that are essentially internal but are brought out for the sake of optional flexibility, such as bipolar offset reference terminals.

Block diagrams used in this book (and much of the literature), for facility of communication, tend to depict only those interfaces that are of specific relevance to the point under discussion. However, the reader should be aware that “out of sight” should not mean “out of mind.”

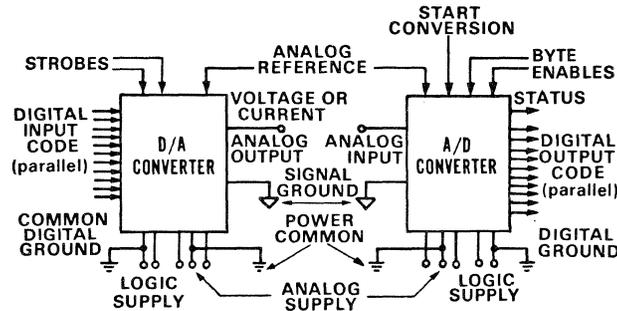


Figure 10. Converter connections.

GROUND RULE

The experienced circuit designer will recognize the feeling of wariness provoked by the presence of two supplies, and several classes of signals, all needing return “to ground.” Grounding is indeed important to system performance; discussions of the essentials of grounding practice will be found (as appropriate) in several places in this book; however, for clarity in the present exposition, we will consider that all grounds are always at true zero potential with respect to all input and output signals. Accordingly, the discussions that follow will everywhere employ the inverted triangle, which represents ideal signal ground.

POWER SUPPLIES

The choice of power supplies for use with converters is governed by their effect on conversion accuracy, system noise, size and weight, reliability, and cost. Supply capacity is determined by the choice of system philosophy: one main supply feeding all elements, vs. a number of satellite supplies or regulators sharing a common primary source (which might itself be a dc voltage derived from the ac mains). For most commercially-available modular converters, supply voltage used for operational amplifiers is usually adequately regulated to provide rated performance. Converter performance specifications as a function of dc variation of power supply voltage are almost always provided by the manufacturer.

DIGITAL LOGIC LEVELS

There are a variety of voltage levels and current-drive capacities corresponding to logic “0” and logic “1.” This variety is a result of historical compromises between the need for speed, reliable differentiation between the logic states, circuit complexity, fanout capability, and the limitations of circuit/processing technology. They are described by such sets of initials as RTL, DTL, HTL, ECL, CMOS, IIL. Most of the modern modular conversion system products are designed to be compatible with TTL, which is the most widely-used logic system at present.

In TTL, as mentioned early in this chapter, a gate must respond to “0” if the input to it is 0.8 volts or less, and it must respond to “1” if the input is 2.0 volts or greater, up to the maximum and minimum voltage ratings. In order to provide a measure of immunity to noise, including dc voltage drops, occurring in transmission, gate outputs (within their current ratings), must furnish a minimum of 2.4 volts to signify “1” and a maximum of 0.4 volts to signify “0.”

Within the TTL system, there are further classifications by fanout (the number of gates that can be driven) and speed. For convenience, input or output currents are normalized in terms of the standard *TTL load*, which is a positive current of $40\mu\text{A}$ for “1” and -1.6mA (sink current) for “0.”

In addition to the *bipolar* transistor logic circuitry, *MOSFET* logic (e.g., CMOS) is often used. Because CMOS logic can operate at higher voltages, with greatly-increased noise immunity, and because of its low power consumption and accordingly higher circuit-packing density, it is especially useful in remote and portable system elements. The Analog Devices ADC1121 and DAC1122 are examples of converters specifically designed for low-power applications, using CMOS, but compatible with TTL. Examples of CMOS IC types include the AD7520 D/A converter and the AD7550 A/D converter.

Products designed for TTL logic can be used with other logic schemes by performing appropriate transformations (level-shifting, gain-or-attenuation, sign-inversion). D/A converters designed for TTL logic will inherently accept DTL inputs.

CONTROL LOGIC: THE *STATUS* OUTPUT

Most types of A/D Converters – except for those that perform continuous conversions – require a time interval, that may be either fixed or variable, to perform the conversion. During this time, the outputs may be changing and may bear no relationship to the final result. If a converter is interrogated during conversion, erroneous information will be transmitted. For this reason, the control output called *Status* (or “busy,” “ready,” etc.) changes state in response to the Convert Command to define the beginning of conversion and does not return to the original state until conversion is completed. It may be used to inhibit readout or to activate a *buffer* output register that holds the previous output word. It may also serve to prevent another conversion from beginning until the previous one is accomplished.

CONTROL LOGIC: THE *STROBE*

Most D/A converters – except for serial types, such as those that depend on charging of capacitors – have basic circuitry that responds immediately and continuously to whatever digital signals are applied. It is often desirable to isolate the basic circuitry from the source of digital information by a register, and update all bits simultaneously, upon command. The command input is called the *strobe* (or “clock” or “enable.”)

For use with microprocessors, the data word is often divided into *bytes*, having a maximum of 8 bits (see Chapter I-4), which are *enabled* in sequence to transmit the information contained in the full word in *byte-serial* format. Input strobes to DAC’s might be called *high-byte strobe* (more-significant bits), *low-byte strobe* (less-significant bits), and – to load the complete information into the DAC – *load-DAC strobe*. Conversely, the parallel outputs of ADC’s are placed on the microprocessor data bus by *high-byte enable* and *low-byte enable* strobes. In order for the *status* output to be treated as information appearing on the data bus, a *status-enable* strobe would be used with microprocessor-compatible ADC’s.

ANALOG SIGNALS

Inputs to A/D converters are usually in the form of voltage. Outputs from D/A converters are often in the form of voltage, at low impedance, from an operational amplifier (an example is AD564). However, many converters provide an output *current* instead of a voltage (for example, AD563). As will become clear in the sections that follow, the basic conversion process may inherently develop a current output that is quite fast, linear, and free from offset. A built-in operational amplifier may be used to convert that current to voltage, but at the present state-of-the-art, on-chip IC op amps having submicrosecond settling time to useful resolution are not available. As a result of the inevitable design tradeoffs, the amplifier will tend to limit converter performance, primarily by increasing settling time. If the current is made available directly, the speed of response is under the control of the user, through the choice of an appropriate external output amplifier. He can also choose the inverting or the noninverting mode. For example, the full-scale settling time of the current output from AD561 to 0.05% ($\frac{1}{2}$ LSB of 10 bits) is 250 nanoseconds. The AD561, followed

by a general-purpose I.C. operational amplifier for voltage output, has settling time of $5\mu\text{s}$ to the same resolution; but with the high-speed AD509, it can be reduced to 600ns.

Converters that have current outputs or “soft” voltage outputs (directly from resistive ladders) may be considered as either voltage generators with series resistance or current generators with parallel resistance (Figure 11). They are used with operational amplifiers in either the inverting or the noninverting connection (Figure 12). Some types, such as the AD561 have one or more internal feedback resistors (for appropriate output voltage scaling) that track the ladder resistors, to minimize temperature variations of gain in inverting configurations. Also present may be a terminating resistor, to develop passively a non-inverted output voltage, which may be amplified with a noninverting amplifier. The gain-determining feedback resistances (R_1 , R_2) do not have to track the converter’s internal resistors, only one another.

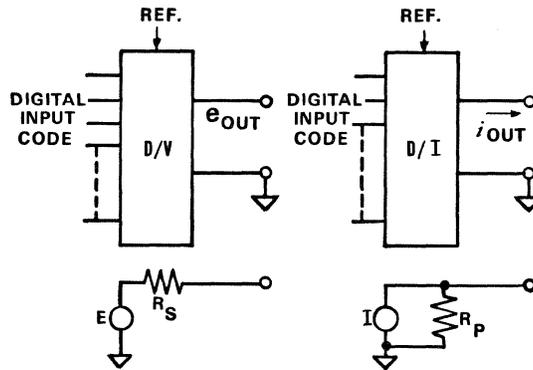


Figure 11. Digital-to-analog converters as voltage or current generators.

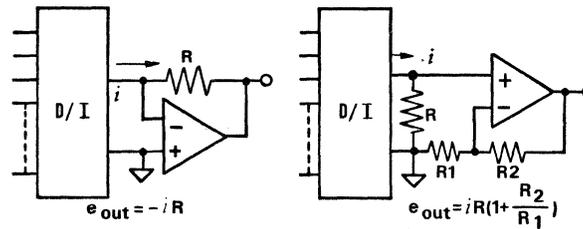


Figure 12. Current-to-voltage conversion using operational amplifier.

Using current-output converters, the inverting connection is the preferred connection, for a number of reasons: With current output, the internal impedance of the D/I converter is usually high. Thus, the loop gain will tend to remain near unity, essentially independently of the value of feedback resistance, minimizing amplifier-contributed errors, such as voltage drift. Furthermore, the output swing of the D/I converter (at the amplifier’s negative input terminal) will be negligible, minimizing loading of the current output – and any associated problems, such as voltage-dependent nonlinearity and variation of internal impedance with temperature. Finally, common-mode rejection is not important, since there is no common-mode swing.

The conversion relationship of D/I converters is “positive reference” (Fig. 6) if the current flowing *out of the converter* increases as the value represented by the digital code increases, irrespective of the actual polarity of the converter’s reference element. If a noninverting amplifier configuration is used, the output voltage will have the same normalized conversion relationship as the output current. If an inverting connection is used, the voltage will have a conversion relationship of opposite output polarity. Figure 13 illustrates this point, for both binary and complementary binary unipolar codes. On the other hand, if current flowing *towards the converter* increases as the value represented by the digital code increases, the relationship is “negative reference” for current, but “positive reference” for voltage in an inverting configuration.

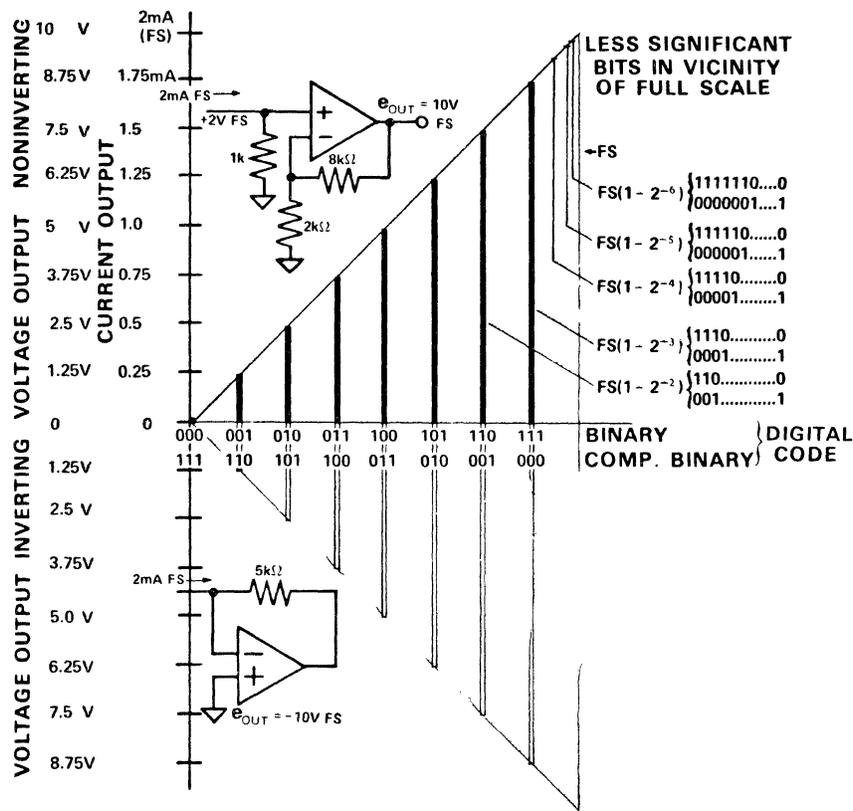


Figure 13. Ideal conversion relationships for 3 most-significant bits in positive reference unipolar D/A converter with noninverting and inverting amplifier connections, and binary vs. complementary binary codes.

D/A CONVERTER CIRCUITS

A basic D/A converter consists of a reference, a set of binary-weighted precision resistors, and a set of switches (Figure 14).

In this example, an operational amplifier holds one end of all the resistors at zero volts. The switches are operated by the digital logic, open for “0,” closed for “1.” Each switch that is closed adds a binary-weighted increment of current E_{REF}/R_j via the summing bus connected to the amplifier’s negative input. The negative output voltage is proportional to the total current, and thus to the value of the binary number.

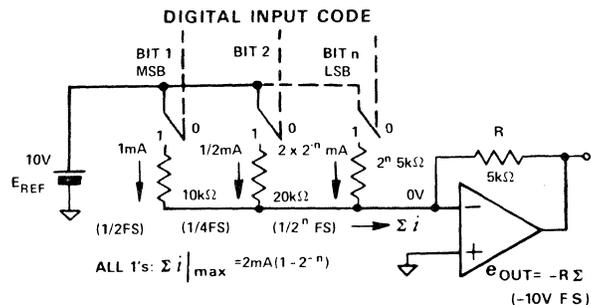


Figure 14. Simple D/A converter.

In practical applications, say for 12-bit D/A conversion, the range of resistance values would be 4,096:1, or 20MΩ for the LSB. If the resistors are to be manufactured in thin- or thick-film, or integrated-circuit form, such a range would be totally impractical. If discrete resistors are used, cost and size are increased, tracking advantages are lost, and inventory becomes a problem

Resistance Ladders

A way to reduce the resistance range is to use a limited number of repeated values, with suitable attenuation. One convenient approach, shown in Figure 15, is to use a binary resistance quad, consisting of the first four values (i.e. 2R, 4R, 8R, 16R) for each group of 4 bits, with attenuation of 16:1 for the second quad, 256:1 for the third quad, etc. As an additional benefit, the proper relative quad weighting for BCD conversion is achieved by changing the attenuation between quads to 10:1.

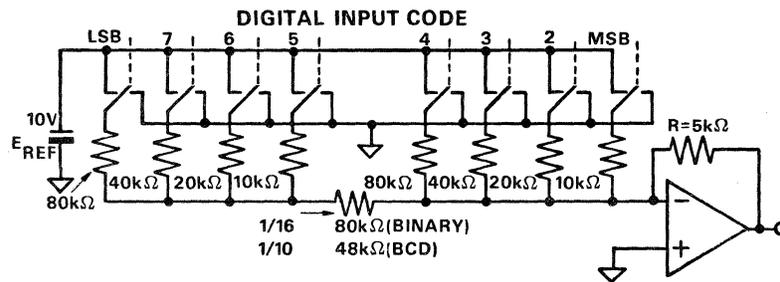
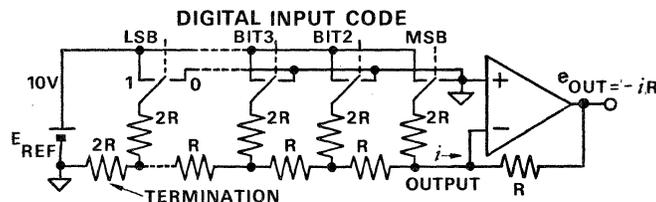
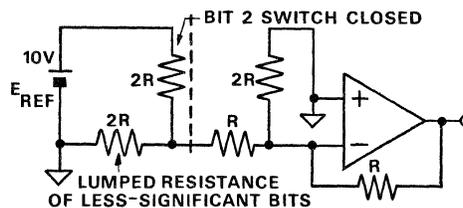


Figure 15. 8-Bit D/A converter using two equal-resistance quads with attenuation for the less-significant quad.

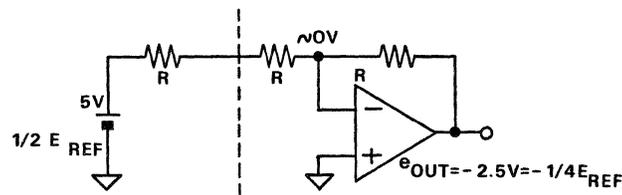
Carrying this reduction of resistance values all the way, one arrives at the R-2R ladder, another convenient – and very popular – form, depicted in Figure 16, which shows its use with an inverting operational amplifier. If all bits but the MSB are “off” (i.e., grounded), the output voltage is $(-R/2R) E_{REF}$. If all bits but bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4} E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is $2R$; the Thévenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance $2R$; since the grounded MSB series resistance, $2R$, has virtually no influence – because the amplifier summing point is at virtual ground – the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the n th bit produces an increment of output equal to $2^{-n}E_{REF}$.



a. Basic circuit.



b. Example: Contribution of bit 2; All other bits “0”.



c. Simplified equivalent of circuit (b).

Figure 16. D/A converter using R-2R ladder network in current mode.

The R-2R network can be employed to give unattenuated noninverting output simply by connecting the output terminal to a high-impedance load, such as the input of a follower-connected operational amplifier (Figure 17). If the line of reasoning described in the preceding paragraph is followed, it can be seen that the MSB output is $\frac{1}{2}E_{REF}$ (2R-2R divider), Bit 2 is $\frac{1}{4}E_{REF}$ ($\frac{1}{2}E_{REF}$ equivalent generator and 2R-2R divider), etc. Since the entire network may be considered to be an equivalent generator having an output voltage NE_{REF} where N is the fractional digital number) and an internal resistance R , the output may be scaled down accurately by connecting precise resistance values to ground. Because of its symmetry and self-duality, the R-2R network may be used in other configurations. Figure 18 shows one example, in which the input and output leads, as depicted in Figure 16, are interchanged, for use in *current-switching conversion*.

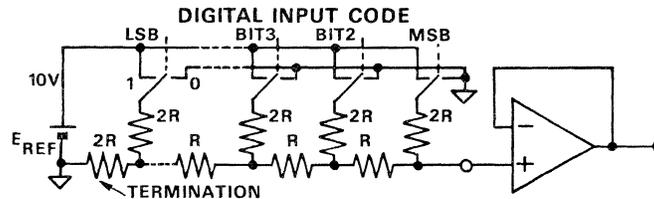


Figure 17. D/A converter using R-2R ladder network in voltage mode.

Switching

A thorough description of the variety of voltage and current switches actually used in converters would be beyond the scope of this chapter. However, the use of monolithic quad switches in converter design is discussed in Chapter II-3. Information on typical CMOS voltage switch quads will be found in the Analog Devices short-form *Product Guide*. Voltage switches are used in converters such as the AD7520 in the manner indicated in Figure 18, switching between the reference and ground, in order to maintain constant impedance. Since they accept reference voltage of either polarity, the AD7520's may be used as 4-quadrant multiplying DAC's.

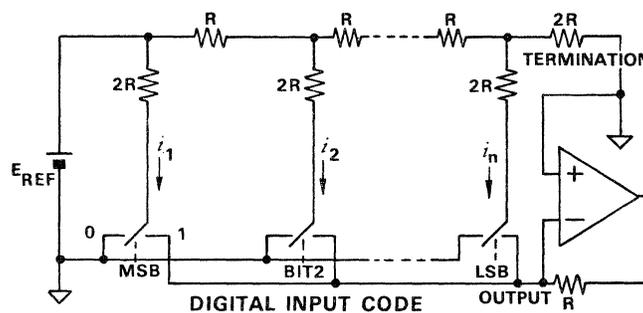


Figure 18. Inverted R-2R ladder in current-switching mode.

Current switches are used to steer current between an amplifier summing point and ground. They are capable of considerably higher speeds than voltage switches, because the reference current is not interrupted, and the only significant voltage changes appear at the output, (in response to code changes) but not across the switches. A simplified form of current switch, first employed in the '60's-vintage MDA-U Minidacs[®], is shown in Figure 19. In this scheme, the switching transistors, in effect, isolate the weighting resistors from the output line (and its attenuators).

To understand the switching scheme of Figure 19, consider the transistor Q1. If its base-emitter voltage is equal to that of Q_R , the voltage across $2R$ will be equal to E_{REF} . The current through the resistor will therefore be $\frac{1}{2}E_{REF}/R$, and (assuming no current through the diode, and very high β) this same current will flow through to the collector circuit (i.e., the output). In order for this to happen, the cathode of the diode must be above the anode potential (i.e., logic "1.")

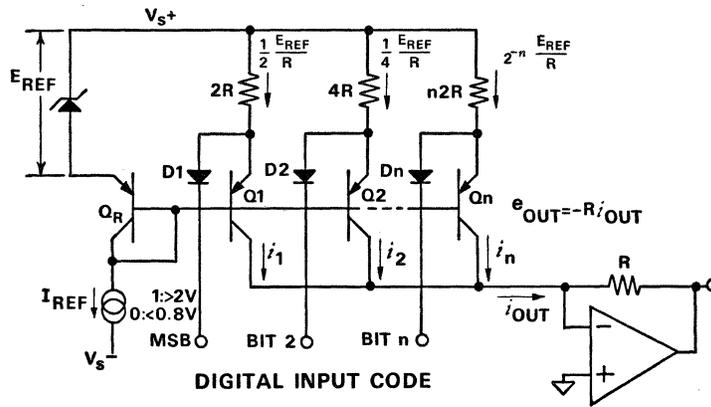


Figure 19. D/A converter using basic current switching technique.

If the base line is at 1.4V, and assuming 0.6V diode conduction voltage, an anode voltage of 2V (minimum for TTL logic "1") would be sufficient for this condition. If the anode of D1 is now switched to "0" (0.8V or less), Q1 will be cut off, because D1 will steal all its current, clamping the emitter of Q1 at or below the base potential, and eliminating Q1's contribution to the output. Since the current is not interrupted, and the voltage change is small, switching time is quite short, with settling to within 1 LSB typically of the order of 200 nano-seconds.

If Q1 and Q_R are matched for V_{BE} and have equal currents flowing through their emitter circuits, the voltage across 2R will track E_{REF} with temperature, making the MSB current essentially independent of temperature, except for β variations. The lesser-order bits operate in similar manner, except that the switching transistors are matched to the reference at the appropriate binary-weighted current levels. Tracking with temperature at these levels is adequate.

The switches and resistors are grouped in quads, with repeated 2R, 4R, 8R, 16R resistance values and 8:1 maximum range of bit currents. The less-significant bit currents are attenuated in the output line (Figure 20). An important benefit of the quad structure is that there are only four different current values, considerably reducing the dimensions of the current-matching problem, and maintaining adequate switching speed for the less-significant bits. Because of the attenuation, the tolerances on the resistor values and transistor tracking in the less-significant quads are greatly relaxed relative to the most significant quad. In monolithic quads, e.g. those in the AD562, the switching transistors have emitter areas bearing power-of-two relationships, so as to inherently maintain constant current density and hence equal (and tracking) V_{BE} and β. The reference transistor, on the same chip, is identical to one of the switching transistors.

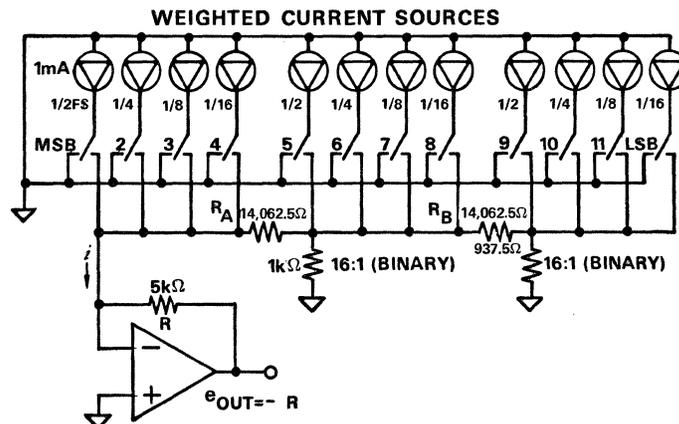


Figure 20. Block diagram of 12-bit current-switching D/A converter, showing weighted attenuation of quad output currents for binary coding. For BCD, R_A and R_B become 8,132.5Ω and 8,437.5Ω, and R becomes 4kΩ, and the interquad attenuations are 10:1.

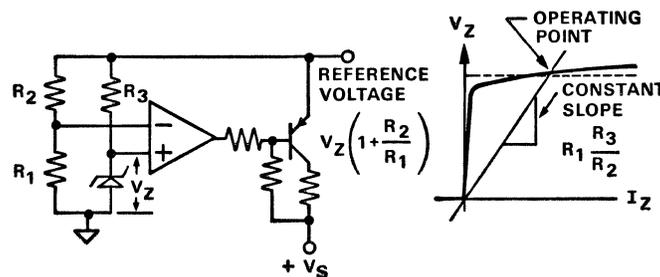
References

The most widely-used reference device is the temperature-compensated zener diode, often used with operational amplifiers for operating-point stabilization, unloading, or transducing to current (Figure 21). Some useful reference-circuit designs are discussed in chapter II-3. Complete references are also available in IC form and are either of the zener type (AD2700, 10V) or band-gap type (AD580, 2.5V).⁶

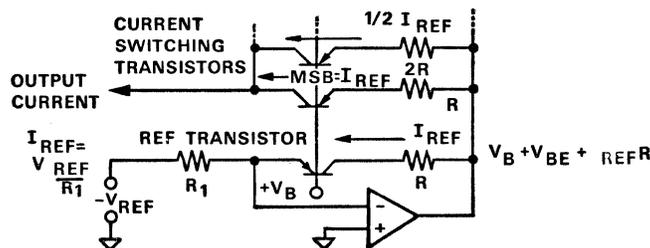
Bipolar Conversion

For bipolar current-switching D/A conversion, using offset binary or two's complement codes, an offset current equal and opposite to the MSB current is added to the converter output. This may be accomplished with a resistor and a separate offset reference, but more usually, it is derived from the converter's basic reference, in order to minimize drift of the output zero with temperature.

The gain of the output inverting amplifier must be doubled, in order to double the output range, e.g., from 0 - 10V to $\pm 10V$. As indicated earlier, (Figure 6) zero output corresponds to offset binary 1 0 0 . . . 0 0, or two's complement 0 0 0 . . . 0 0.



a. Amplifier adjusts feedback current to stabilize zener operating point independently of V_S or load variations.



b. Amplifier converts reference voltage to reference current in current-switching converter.

Figure 21. Examples of use of operational amplifiers in generating reference voltage and current.

Figure 22 shows an example of a current-switching converter connected for bipolar output. Note that because the amplifier is connected for sign inversion, the overall conversion relationship is "negative reference," i.e., +F.S. for all 0's (offset binary), -F.S. (1 - LSB) for all 1's.

⁶Analog Dialogue 9-1 (theory) and 9-2 (applications), 1975.

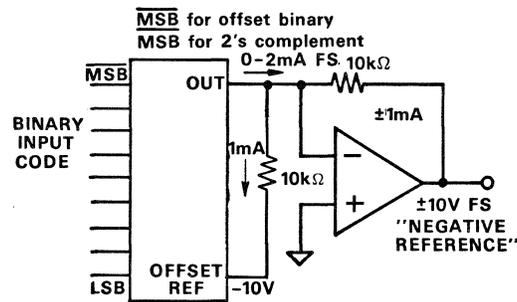


Figure 22. Bipolar connection of current-switching D/A converter for offset binary or 2's complement codes.

For non-inverting applications, the same values of offset voltage and resistance are used, but the proper value of output voltage scale factor depends on the load presented by the parallel combination of the internal resistance, the offset resistance, and the external load. (Figure 23)

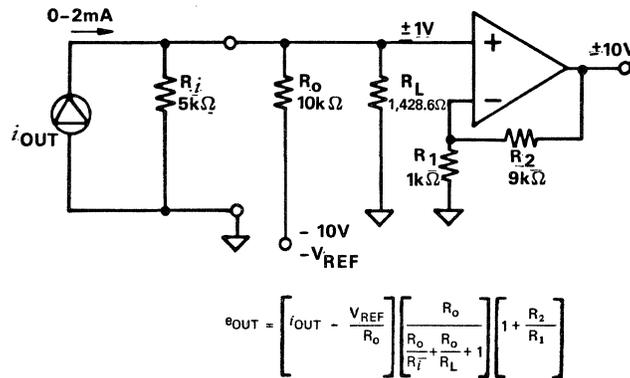


Figure 23. Non-inverting output from current-switching D/A converter.

For bipolar D/A conversion using the voltage switches and R-2R ladder network of Figures 16 and 17, and offset binary or 2's complement coding, one approach is to drive those network terminals that are normally grounded for unipolar operation (one side of the switches and the LSB termination) with the reference signal in the opposite polarity. If the LSB termination is allowed to remain grounded, the output will be symmetrical, resembling the conversion relationship of Figure 8, with no code for analog zero but with normalized gain reduced to $1 - 2^{-(n+1)}$

For sign-magnitude conversion, the converter's current output may be inverted, using a current inverter. Switch circuitry, operated by the MSB, determines whether the output amplifier's input is direct or via the current inverter. One way of accomplishing this is shown in Figure 24.

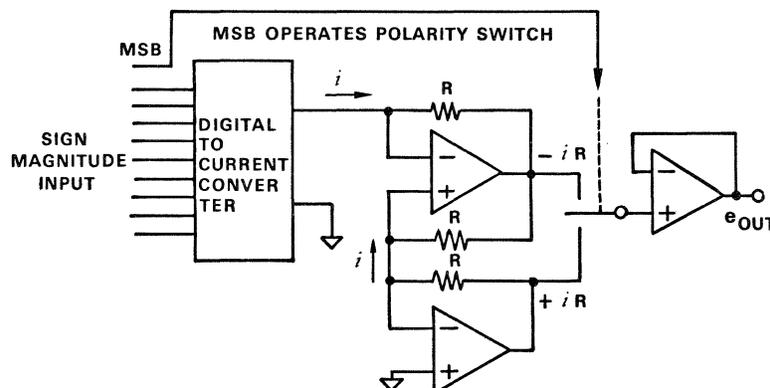


Figure 24. Sign-magnitude bipolar D/A conversion using unipolar DAC and switched outputs of operational amplifiers.

Registers on DAC's (Figure 25)

The basic parallel-input D/A converter circuits considered so far have the common property that the analog output continually reflects the state of the logic inputs. If the basic conversion circuitry is preceded by a register, the device will respond only to the inputs gated into it. This property is especially useful in data distribution systems, in which data is continually appearing, but it is desired that a DAC respond only at certain times, then hold the analog output constant until the next update. In this sense, a DAC with buffer storage may be viewed as a sample-hold with digital input, analog output, and (conceivably) infinite "Hold" time.

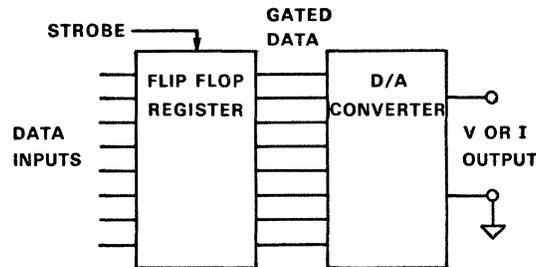


Figure 25. D/A converter with buffer register.

The register is controlled by a *strobe* signal, which causes it to update. The limiting rate at which the strobe may update is determined by two factors: the settling time of the DAC, and the response time of the logic. In general, settling time of the analog portion of the D/A converter is at least an order of magnitude slower than the response time of modern high-speed TTL logic circuits and is thus the limiting factor on update rate.

The only time when the speed of the digital portion of a D/A converter is of importance is when the "glitch" (See II-5) caused by unequal turn-on and turn-off times is an important factor in the application. The digital inputs to a DAC come from digital logic circuits, which exhibit *skew*, or unequal turn-on and turn-off times. The switches used in DAC's also exhibit skew; however, even if the switch circuitry is specifically designed to minimize skew, the additional skew of the digital logic will constitute an irreducible minimum. In such circuit applications, glitch energy can be minimized by using high-speed logic.

A/D CONVERTER CIRCUITS

There are a vast number of conceivable circuit designs for A/D converters.⁷ There are a much more limited number of designs available on the market in small, modular form at low cost, specifically designed for incorporation as components of equipment. The most popular of these are :

- Successive-approximation types
- Integration (single-, dual-, and quad-slope) and V-to-f types
- Counter and "servo" types
- Parallel and modified-parallel types

Each approach has characteristics that make it most useful for a specific class of applications, based on speed, accuracy, cost, size, versatility.

Successive-Approximation

Successive-approximation A/D converters are quite widely used, especially for interfacing with computers, because they are capable of both high resolution (to 16 bits: ADC-16Q), and high speed (to 1 MHz throughput rates: ADC-1103). Conversion time is fixed and independent of the magnitude of the input voltage. Each conversion is unique and independent of the results of previous conversion, because the internal logic is cleared at the start of a conversion.

⁷See *Electronic Analog/Digital Conversions*, by H. Schmid (Van Nostrand Reinhold, 1970) for an encyclopedic panoply of A/D (and D/A) converter circuit designs.

Modern IC converters, such as the monolithic AD7570 10-bit ADC, include 3-state data outputs and byte controls to facilitate interfacing with microprocessors. A “three-state” output has, in addition to the normal “1” and “0” states, when enabled, a not-enabled condition, in which the output is simply disconnected via an open voltage switch. This permits many device outputs to be connected to the same bus – only the device that is enabled (one at a time) can drive the bus. Since typical processor data buses are only 8 bits wide, 10- or 12-bit data must be communicated in two steps, one “byte” at a time.

The conversion technique consists of comparing the unknown input against a precisely-generated internal voltage at the output of a D/A converter. The input of the D/A converter is the digital number at the A/D converter’s output. The conversion process is strikingly similar to a weighing process using a chemist’s balance, with a set of n binary weights (e.g., 1/2lb, 1/4lb, 1/8lb, 1/16lb (= 1oz), 1/2oz, 1/4oz, etc., for unknowns up to 1 lb.)

After the conversion command is applied, and the converter has been cleared, the D/A converter’s MSB output (1/2 full scale) is compared with the input. If the input is greater than the MSB, it remains ON (i.e., “1” in the output register), and the next bit (1/4FS) is tried. If the input is less than the MSB, it is turned OFF (i.e., “0” in the output register), and the next bit is tried. If the second bit doesn’t add enough weight to exceed the input, it is left ON (“1”), and the third bit is tried. If the second bit tips the scales too far, it is turned OFF (“0”), and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. The process completed, the *status* line changes state to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary digital code corresponding to the input signal.

Figure 26 is a block diagram of a successive-approximations A/D converter, accompanied by a time history of a simple 3-bit conversion, in terms of the D/A converter output (the weight added to the balance pan). Note that, to place the D/A converter output in the center of each ideal output quantum, a 1/2-LSB “thumb” is placed on the scale (see Figure 2, this chapter), in order to locate the transitions precisely at the 1/2LSB points.

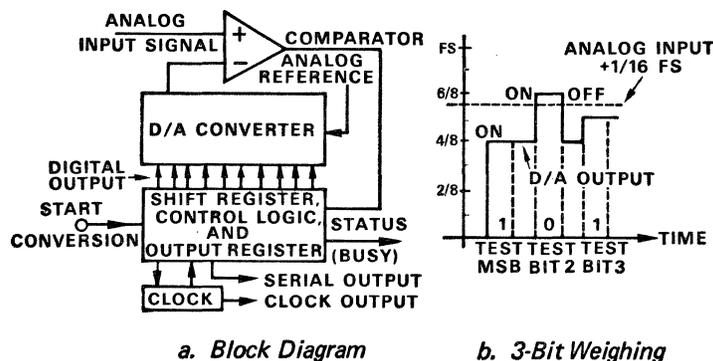


Figure 26. Successive-approximation A/D converter.

Note that the input does not change during conversion in the example of Figure 26b. If the input were to change during conversion, the output number could no longer accurately represent the analog input unless the new value were larger than the sum of the weights already present by an amount less than the sum of the untried weights. Since this is not-often-fulfilled requirement, it is usual to employ a sample-hold device ahead of the converter to retain the input value that was present at a given time before the conversion starts, and maintain it constant throughout the conversion. The *status* output of the converter could be used to release the sample-hold from its *hold* mode at the end of conversion. A sample-hold may not be needed if the signal (by itself, or with filtering) varies slowly enough and is sufficiently noise-free that significant changes will not be expected to occur during the conversion interval.

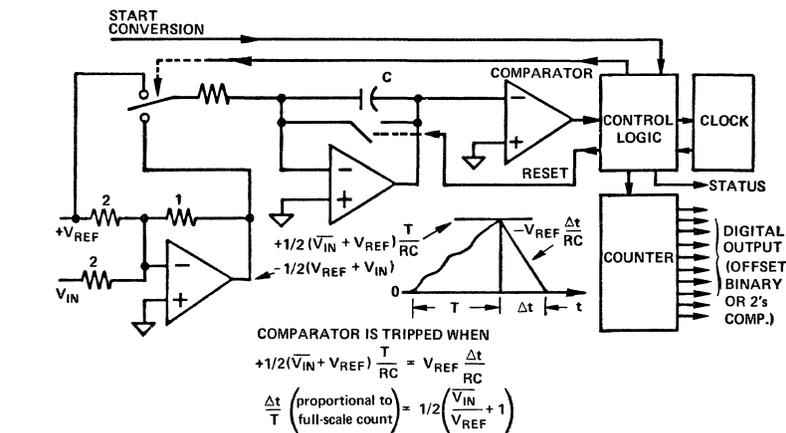
Accuracy, linearity, and speed are primarily affected by the properties of the D/A converter (and its reference), and the comparator. In general, the settling time of the D/A converter and the response time of the comparator are considerably slower than the switching time

of the digital elements. The differential nonlinearity of the D/A converter will be reflected in the differential nonlinearity of the resulting A/D converter. If the D/A converter is non-monotonic, one or more codes may be missing from the A/D converter's output range. Bipolar inputs are dealt with by using a D/A converter with bipolar output and offset binary coding, and appropriate input scaling.

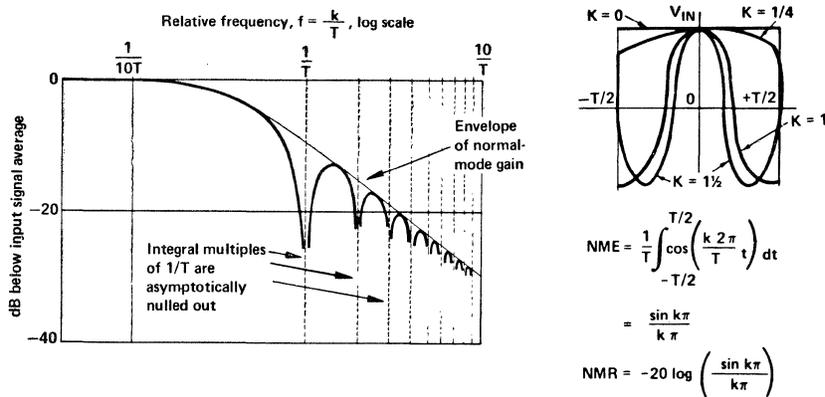
Integration (Ramp and V-to-f Types)

This family of converters is also quite popular. Its members perform an *indirect* conversion, by first converting to a function of time, then converting from the time function to a digital number using a counter. The *dual-ramp type* is especially suitable for use in digital voltmeters and those applications in which a relatively-lengthy time may be taken for conversion to obtain the benefits of noise reduction through signal averaging.

Here's how the dual-ramp type works: The input signal is applied to an integrator; at the same time a counter is started, counting clock pulses. After a predetermined number of counts (a fixed interval of time, T), a reference voltage having opposite polarity is applied to the integrator. At that instant, the accumulated charge on the integrating capacitor is proportional to the average value of the input over the interval T . The integral of the reference is an opposite-going ramp having a slope V_{REF}/RC . At the same time, the counter is again counting from zero. When the integrator output reaches zero, the count is stopped, and the analog circuitry is reset. Since the charge gained is proportional to $\overline{V_{IN}} T$, and the equal amount of charge lost is proportional to $V_{REF} \Delta t$, then the number of counts relative to the full count is proportional to $\Delta t/T$, or $\overline{V_{IN}}/V_{REF}$. If the output of the counter is a binary number, it will therefore be a binary representation of the input voltage. If the input is attenuated and offset by half the reference voltage, the output will be an offset binary representation of a bipolar input, suitable as an input for computer systems. Figure 27a shows a dual-ramp A/D converter for bipolar signals with offset-binary output.



a. Dual-ramp A/D converter for bipolar input.



b. Worst-case normal-mode response of dual-slope A/D converter.

Figure 27. Voltage-to-time-to-digital converters.

Dual-slope integration has many advantages. Conversion accuracy is independent of both the capacitor value and the clock frequency, because they affect both the up-slope and the down-ramp in the same ratio. Differential linearity is excellent, because the analog function is free from discontinuities, the codes are generated by a clock and counter, and all codes can inherently exist. Resolution is limited only by analog resolution, rather than by differential nonlinearity; hence, the excellent fine structure may be represented by more bits than would be needed to maintain a given level of scale-factor accuracy. The integration provides rejection of high-frequency noise and averaging of changes that occur during the sampling period. The fixed averaging period also makes it possible to obtain “infinite” normal-mode rejection⁸ at frequencies that are integral multiples of $1/T$ (see Figure 27b).

Throughput rate of dual-slope converters is limited to somewhat less than $1/2T$ conversions per second. The sample time, T , is determined by the fundamental frequency to be rejected. For example, if one wishes to reject 60Hz and its harmonics, the minimum integrating time is $16\frac{2}{3}$ ms, and the maximum number of conversions is somewhat less than 30/s. Though too slow for fast data acquisition, dual-slope converters are quite adequate for such transducers as thermocouples and gas chromatographs; and they are the predominant circuit used in constructing digital voltmeters. Since DVM's use sign-magnitude BCD coding, bipolar operation requires polarity sensing and reference-polarity switching, rather than simple offsetting.

A shortcoming of conventional dual-slope converters is that errors at the input of the integrating amplifier or the comparator show up as errors in the digital word. Such errors are usually reduced by the introduction of a third portion of the cycle, during which a capacitor is charged with zero-drift errors, which are then introduced in the opposite sense during the integration to (it is hoped) nullify them. An interesting scheme (applied to the 13-bit single-chip AD7550) discussed in Chapter II-2, for nullifying all such input errors, is the patented *quad-slope* principle*; it stores the errors in the form of a digital count during a calibration cycle and subtracts them from the final count during the conversion cycle.

Other conversion approaches in this class include the single-ramp type and V/f converters. In the single-ramp converter, a reference voltage, of opposite polarity to the signal, is integrated (while a counter counts clock pulses) until the output of the integrator is equal to the signal input. At that time (Δt) the output of the integrator is $E_{REF}\Delta t/RC$. Therefore, Δt – hence, the number counts and the corresponding digital number – is proportional to the ratio of the input to the reference. This process has the weakness that its accuracy depends on both the capacitor (extremely-accurate and stable resistors are relatively easy to come by) and the clock frequency. In the V/f converter, a frequency is generated in proportion to the input signal; a counter measures the frequency and provides a digital output code, the value of which is proportional to the input signal. In both of the above schemes, offsetting may be used to obtain offset binary representation of bipolar analog inputs.

Counter and “Servo” Types

Figure 28 is a block diagram of a counter-comparator A/D converter, which is analogous to the single-ramp type, but it is independent of the time scale. The analog input is compared with the output of a D/A converter, the digital input of which is driven by a counter. At the start of the conversion, the counter starts its count, which continues until the D/A output crosses the input value. At that point, conversion ceases, and the converter is ready to perform the next conversion after the counter has been cleared and its output dumped into a storage register. The number of counts appears in the output register. For bipolar inputs, a bipolar D/A converter is used, and the count is an offset binary representation of the input, starting from negative full-scale.

⁸Normal-mode noise consists of unwanted signals that appear on the input line, even if common-mode error is nil. If a low-frequency or dc quantity is to be converted in the presence of a high-frequency ripple, a successive-approximations A/D converter, even if preceded by a sample-hold, will convert the instantaneous values of signal-plus-noise, producing a noisy digital signal. On the other hand, an integrator will inherently attenuate high frequencies, producing smoothing, and, if combined with a fixed averaging period, will null out those frequencies that have whole numbers of cycles during the averaging period.

*U.S. Patent 3,872,466

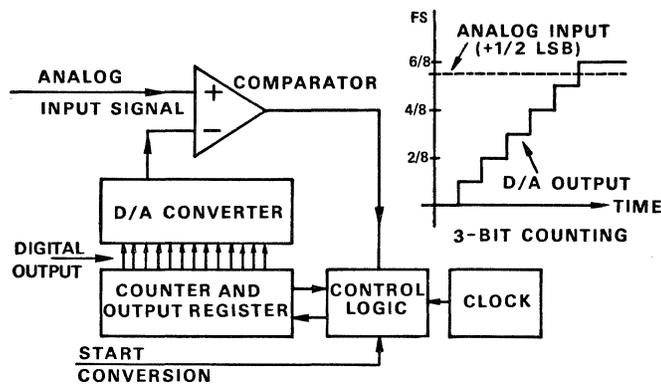


Figure 28. Counter-comparator A/D converter.

Though quite simple in concept, this converter has the disadvantage of limited speed for a given resolution, since the conversion time for a full-scale change is equal to the clock frequency divided into the maximum number of counts. For example, if the clock frequency is 10MHz, the maximum throughput rate for 10-bit resolution (1024 counts) is something less than 10kHz (100 μ s per conversion). A variation of this converter is the “servo” type, in which an “up-down” counter is used.

If the output of the D/A converter is less than the analog input, the counter counts up. If the D/A output is greater than the analog input, the counter counts down. If the analog input is constant, the counter output “hunts” back and forth between the two adjacent bit values. This converter can follow small changes quite rapidly (it will follow 1 LSB changes at the clock rate), but it will require the full count to acquire full-scale step changes. Since it seeks to “home in” on the analog value, the analogy to a servomechanism is quite evident. It seeks to convert continuously, which may be a disadvantage in tying it in with a fast data-

acquisition system, since it can give a valid “conversion complete” report only during the clock period immediately following a change in state of the comparator (which in general occurs at irregular intervals). A buffer storage register may be used to store the previous count, while the counter is seeking the next value. By stopping the count (following a completed conversion) at an externally-determined instant, the servo-type converter may be used as a sample-hold with arbitrarily-long *hold* time (with no droop). If the “up” or the “down” count is disabled, the converter will act as a valley follower or a peak follower, counting in the appropriate direction only when the analog input exceeds the previous extreme value. Both the analog and the digital stored values are available.

Parallel Types

Figure 29 shows a parallel 3-bit converter with Gray code output. It has $2^n - 1$ comparators, biased 1 LSB apart, starting with +1/2 LSB. For 0 input, all comparators are off. As the input increases, it causes an increasing number of comparators to switch state. The outputs of the comparators are applied to the gates, which provide a set of outputs that fulfill the appropriate conditions for Gray-code output. (Natural binary could be implemented in the same way, using an appropriate table).

The evident advantage of this approach is that conversion occurs in parallel, with speed limited only by the switching time of the comparators and gates. As the input changes, the output code changes. Thus, this is the fastest approach to conversion.

Unfortunately, the number of elements increases geometrically with resolution. As linear and digital integrated-circuit elements of increasing complexity become available, increased levels of resolution will tend to approach the threshold of practicality. But high resolution and the fastest speeds at low cost are still some time away.

By combining parallel conversion for small numbers of bits with iteration (to wit, successive approximations taking several bits at a time), it is possible to strike a compromise that gives better resolution than a parallel approach, with less complexity, and improved speed over the successive-approximations approach.

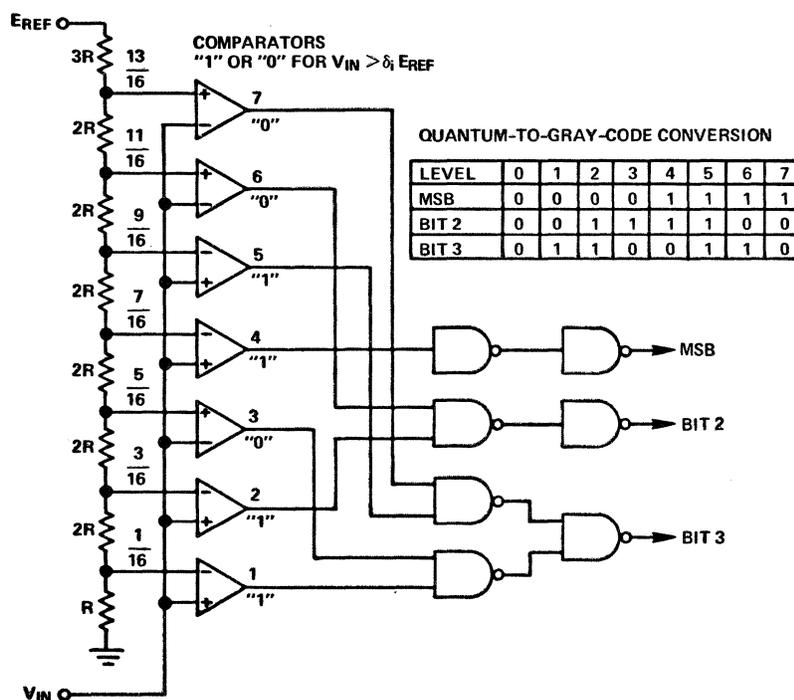


Figure 29. Parallel 3-bit A/D converter with Gray code output.

A NOTE ON SHARED LOGIC

In this book, we are concerned with the embodiment of the conversion function by means of IC's or other modules, in essentially complete form, with *completely defined specifications*. We should acknowledge, however, that in the consideration of the trade-offs between hardware and software, a software-oriented designer will be tempted to consider hardware savings inherent in using the control-logic capability of a microprocessor, along with the precision analog function (the reference and the comparator – and the integrator or the DAC), to perform single or multiplexed conversions, employing the techniques mentioned here, but without using a piece of hardware identifiable as an “a/d converter” *per se*.

A decision to do this is in some respects equivalent to a decision to *design* a converter (analogous to the classical “make-or-buy” decision). While there are applications for which the approach is eminently fruitful (e.g., dedicated instruments, to be manufactured in large quantity), the usual tradeoffs should be considered, lest the fascination of expending design- and manufacturing-effort and software development in areas peripheral to one's primary mission, lead one down the “primrose path” of wasted resources.

CONCLUSION

In this chapter, we have attempted to provide the fundamentals for a basic understanding of converters. In the chapters that follow, we will discuss further some of the considerations faced by the converter designer, provide an understanding of and a guide to specification of converters, and explore the elements of successful system design using converters.

II

Converter Microcircuits

Chapter II-2

As the use of digital techniques in measurement, communication, and control grew by leaps and bounds, the size and price of processors and other LSI (and MSI) logic shrank in similar degree, with the inevitable result that further penetration of digital techniques into those fields became inevitable, in the regenerative fashion that is characteristic of the integrated-circuit era. Along with such other peripherals as keyboards, displays, and memories, converters have followed this spiralling trend – as a matter of necessity.

But it hasn't been easy. Linear IC's have always been more difficult to fabricate for reasonable degrees of resolution and accuracy than digital IC's – in part because the variables that are the input or output involve a continuum of voltage or current, rather than the easier-to-handle two-valued logic. While the problems of implementing digital circuitry have involved questions of functions-per-chip, speed, and dissipation, the analog (precision IC) problems have related more to simple existence and survival. Such matters as offset, bias current, drift, dynamic stability, common-mode errors, and open-loop gain – as well as slewing rate and settling time – have concerned both designers and users of op amps (the “representative” linear-IC product). And op amps entered the “commodity-IC” era a good deal later than (for example) TTL logic.

But converters are more difficult by at least an order of-magnitude. While IC op amps called for precision transistor circuitry and clever design, and IC analog multipliers added a need for precision resistors (and references) – but to-date have attained accuracies to within 0.1% (at best) and are hardly in the commodity class – *converters* call for all of these prodigies of linear design and processing, and *more*: on-chip switches, logic, and everyday resolutions of from 10 to 12 bits (corresponding to accuracies-to-within 0.05% to 0.0125%).

Although the technology still has a considerable distance to go, it is worthwhile to consider the progress made, just within the past five years, as measured by entries within the Analog Devices catalog. In the 1972 *Product Guide*, the IC conversion Product Line consisted of just two families of monolithic quad switches (and compatible resistor networks) for constructing precision 8-10-12 bit A/D and D/A converters, using the design approach described in Chapter II-3. In the just-published 1977 *Short-Form Guide*, there are 12 *families* of IC A/D and D/A converters, spanning resolutions from 8 to 13 bits and technologies from laser-trimmed-on-the-wafer bipolar to thin-films-on-CMOS to hybrids. They include 4-quadrant multiplying DAC's, microprocessor-compatible ADC's and DAC's, and high resolution-and-accuracy devices. And, in addition, there is a large supporting cast of monolithic conversion-related products, including references, sample-holds, multiplexers, CMOS switches, resistance networks, and V/F converters.

The perceptive Reader will observe that such a wealth of products would not be possible if the difficulties due to the diversity of circuitry required on a single chip outweighed the advantages of monolithic IC construction. And indeed, there are significant advantages: components that must be well-matched are inherently well-matched; the small size of the chip makes for excellent thermal tracking; and the low-cost per-die on a reasonably high-yielding wafer results in an attractive price for the end-product, which is welcomed by the user because of both low cost and small size.

As Chapter II-1 points out, the complete D/A converter comprises the basic resistance network and set of switches, plus a reference (if required), registers (if required), current sources (if required), and an output op amp (if voltage output is required). A/D converter circuit requirements depend on the design approach. Integrating types require integrators and counters; successive-approximation types require DAC's and successive-approximation registers; both types need comparators, clocks, and control logic – and they may need references and three-state output registers.

Different technologies are used to optimize devices in production to meet differing classes of user needs (and to accommodate the current state of the Art). It may be useful to discuss these considerations in terms of their application to existing devices now in production and on the market (tabulated in Chapter II-5) and to look briefly into the likely short-term future.

- *CMOS and the AD7520.* CMOS excels at low-power high-density digital logic circuitry and analog voltage switches. It isn't very suitable for high-performance linear circuitry. The AD7520 – and its close relatives, the AD7530 and the 12-bit AD7521 & AD7531 – contain CMOS switches with graduated R_{On} and the logic to drive them (Figure 1), and a thin-film-on-the-chip R-2R ladder network (a significant advance in the technology). The result (to be discussed in detail later) is a digitally controlled attenuator, with 8-10-12-bit conversion-linearity and even better inherent analog-linearity, with very low feedthrough, to frequencies beyond 50kHz. Besides ordinary converter applications, it has many uses as a 2- or 4-quadrant multiplying DAC and as a "digital pot." However, it does require an external op amp, a reference (if used in fixed-reference applications), and registers (if it must interface with processors).

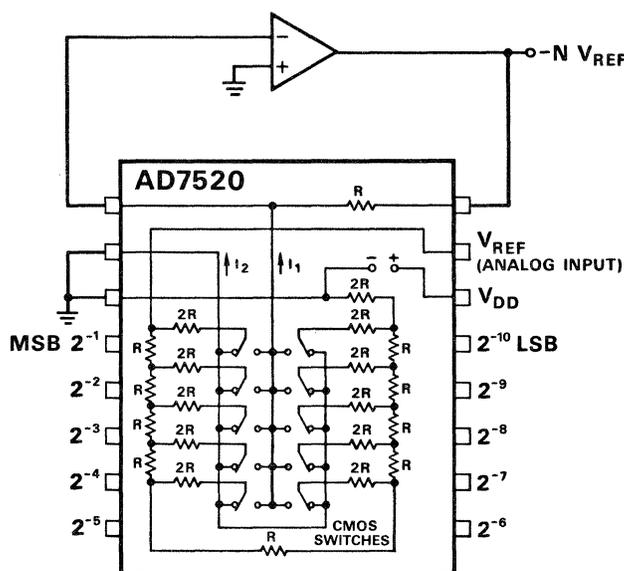


Figure 1. AD7520 10-bit DAC.

- *More CMOS – the AD7522.* The AD7522, using the compact-logic capability of CMOS, provides – not just one, but – two sets of registers, together with the switches and resistors of the AD7520. The result is a double-buffered DAC (Figure 2) that can be directly interfaced to a microprocessor for byte-serial updating. For example, the 8 bits in the low byte can be latched into the buffer register, then the 2 bits in the high byte, and then the whole digital word can be latched into the DAC register to update the analog output at once. The AD7522 also accepts (and shifts along) serial data. And (of course) the input latches can be updated in parallel. An external reference and an output amplifier are still needed for many applications, but the freedom to choose the characteristics of both the reference and the output amplifier is often a great advantage.

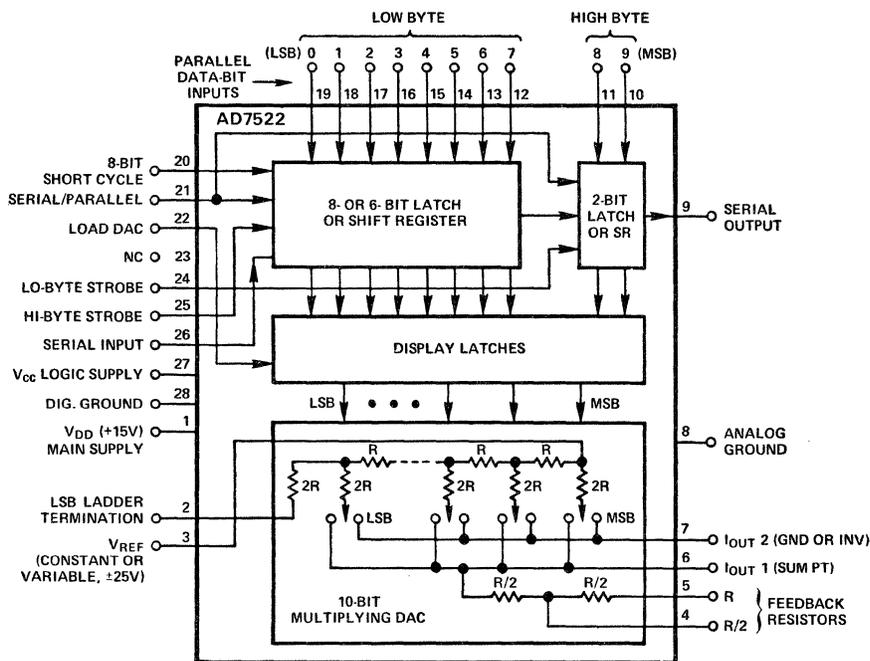


Figure 2. Functional diagram of the AD7522.

• **CMOS A/D Conversion – the AD7570.** The AD7570 is a 10-bit successive-approximation A/D converter that requires only an external reference and a comparator. As Figure 3 shows, it contains a D/A converter (much like the AD7520), control logic, a successive-approximations register, and a three-state output register, that comprises two bytes, for compatibility with micro-processors. The conversion can be self-clocked or driven by an external clock. Since the reference is external, ratiometric conversion is inherent.

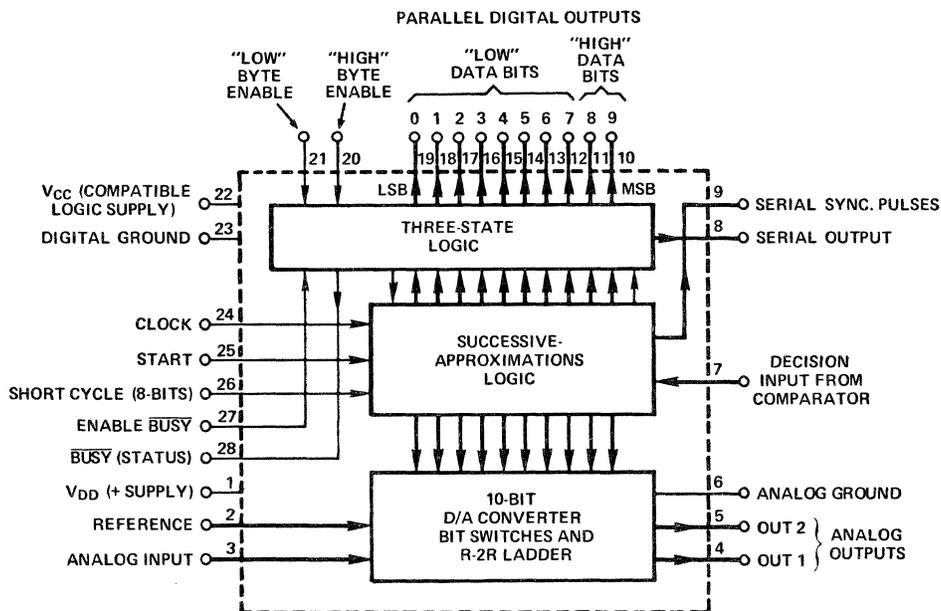


Figure 3. AD7570 10-bit A/D converter.

• **CMOS Quad-Slope Conversion - the AD7550.** The difficulties faced by CMOS in handling analog signals with precision are overcome by integrating-conversion employing “quad slope.” *The AD7550 (Figure 4) contains an integrating amplifier, a comparator, timing and control logic, and counters. Two cycles of dual-slope integration occur – in the first, analog ground is measured against the reference; any errors introduced by the amplifier

*U.S. Patent 3,872,466.

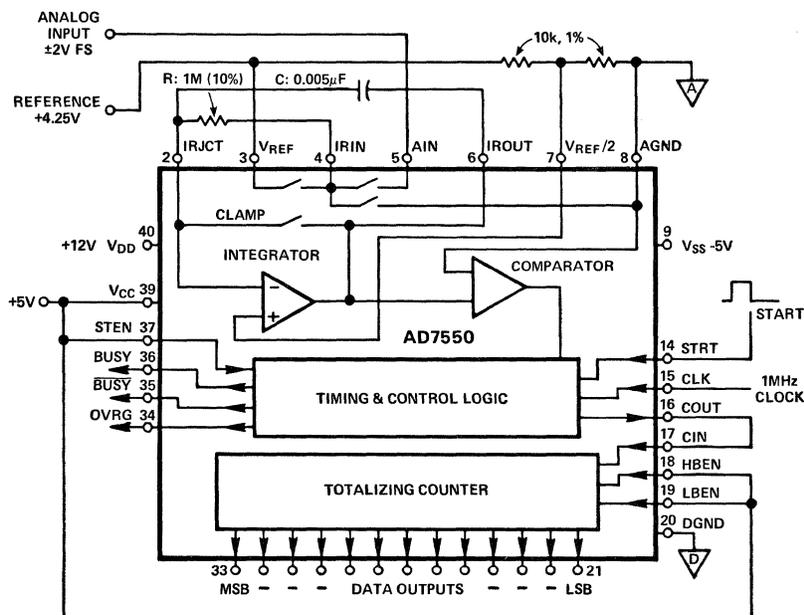


Figure 4. AD7550 connections for basic operation.

and the comparator are stored as a digital count. In the second cycle, the input voltage is measured against the reference, and the error count is subtracted from the output count. (This process will be discussed in greater detail later.)

The technique is very effective: 13-bit conversion occurs, with tempcos in the neighborhood of 1ppm/°C. The only external components needed are the integrating R-C and a (not-very-precise) voltage divider. Data are available in two bytes that can be separately enabled, for interfacing with 8-bit microprocessors. (Since integrating-type conversions require many milliseconds, the status-enable avoids tying-up the processor; end-of-conversion (EOC) can be checked by a polling routine at a time when it is reasonably certain, or on an interrupt basis, for greatest speed.)

- *Bipolar Conversion – the AD562 DAC.* Until the recent developments in Integrated Injection Logic (I²L), reasonably fast IC logic circuitry called for low-voltage processing, and reasonably accurate circuitry (compatible with analog electronics) called for a higher-voltage process, two requirements that were mutually exclusive. The AD562 was an early example of a happy combination of technologies for stable, linear, reasonably fast 12-bit D/A conversion, in which clever circuit-design compensated to some extent for process limitations.

As the functional block diagram in Figure 5 shows, the AD562 consists of a resistance-network chip (laser-trimmed in actual operation) and a complementary amplifier-and-switch chip, embodying (in effect) three sets of quad switches. Unlike the essentially passive AD7520 CMOS species, the AD562 is an *active* device; the reference voltage is transduced to a current, and the output current is a reflected version of it, with the relative magnitude a function of the digital code.

Aspects of the design that contribute to 12-bit (and better) linearity, with microsecond settling, include scaled emitter areas for equal and tracking V_{be} 's, a reference transistor and control amplifier, and current-steering switches that, switching at constant voltage, do not require time-consuming charge transfer. These matters will be discussed later. The external reference can be chosen for desired absolute-accuracy characteristics, and the external op amp can be chosen on the basis of desired output speed.

- *Bipolar Conversion – the AD561 DAC.* This is a monolithic 10-bit converter with an internal reference and high-compliance current output. A number of advanced technologies are combined to provide outstanding performance: the resistance network is a silicon-chromium R-2R ladder deposited directly on the chip and laser-trimmed at the *wafer-probe*

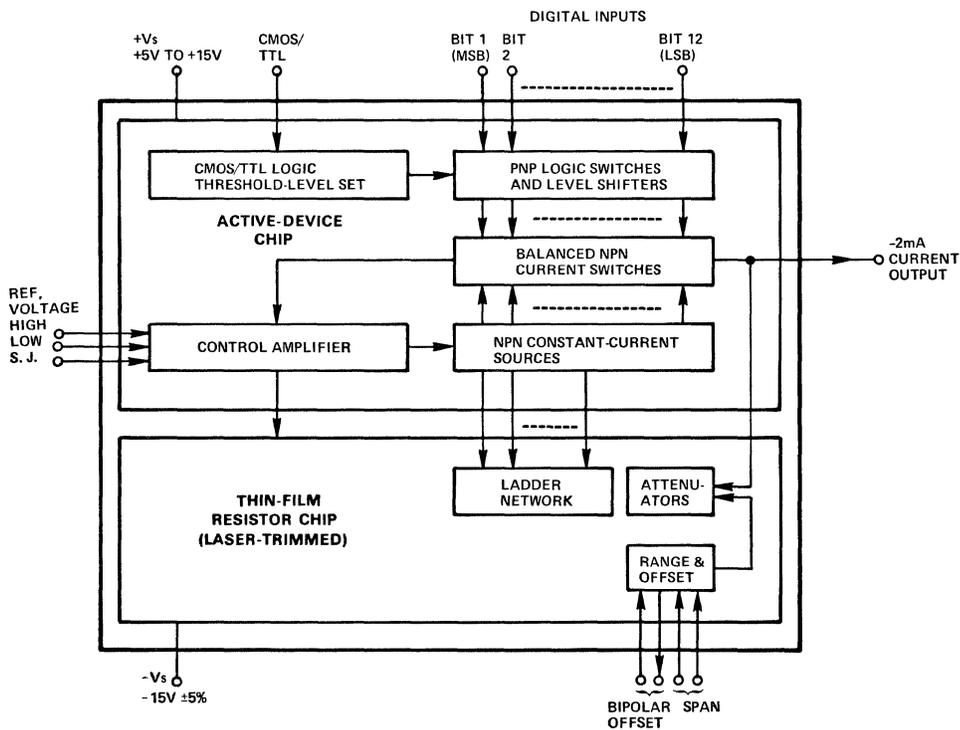


Figure 5. Functional block diagram of the AD562.

stage. The reference is a *buried* Zener diode with high stability – a consequence of its freedom from surface effects.

Because the current-setting network is an R-2R ladder (Figure 6), the output switches do not require attenuation-while-summing of lower-order quad currents, hence the output impedance is of the order of $40M\Omega$, and the usable compliance-voltage range is from $-2V$ to $+10V$ (a simple calculation will show that a swing through the entire compliance range will cause an error of less than 0.2 LSB). This permits a direct voltage output, with an arbitrary load resistance, or direct current-summing at the comparator when the AD561 is used in an ADC circuit. Of course, a conventional output op amp may also be used, chosen for the desired speed of voltage-settling – the converter itself has a 250ns current-settling-time to within $\pm\frac{1}{2}$ LSB, and a 600ns voltage-settling time when the AD509 is used as the output amplifier.

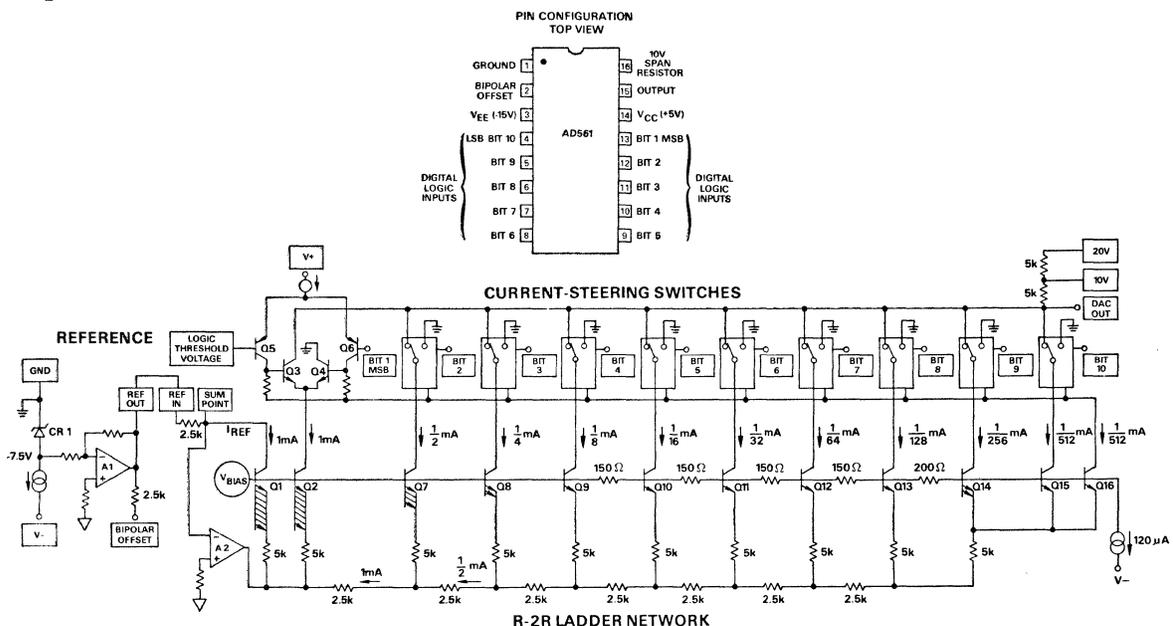


Figure 6. AD561 D/A converter: Schematic and connection diagrams.

• *Integrated Injection Logic conversion – the AD2026 digital panel meter.* I^2L permits analog and high-density logic circuitry to exist as “good neighbors” on a chip manufactured by a bipolar process suitable for high-precision analog circuitry. I^2L eliminates the complexity of conventional bipolar logic by using “inverted” transistors – collectors and emitters are interchanged. When the transistors are inverted, the collectors are isolated without needing the usual wraparound P+ isolation region (which wastes precious “real estate”), and the emitters are grounded.

This leads to very simple logic configurations using interconnection of collectors to provide gating functions.

In the “3.1-digit” AD2026 panel meter (Fig. 7), the I^2L chip contains most of the dual-slope A/D conversion circuitry, including the integrator, comparator, band-gap reference, control logic, clock, counter, display-multiplexer, and display controls. In fact, there are only 13 electrical components in the panel-meter design that are *not* on the chip – 3 light-emitting-diode displays, 3 digit-select transistors, 3 decimal-point current-limiting resistors, 1 LED segment-driver, 2 potentiometers, and the integrating capacitor.

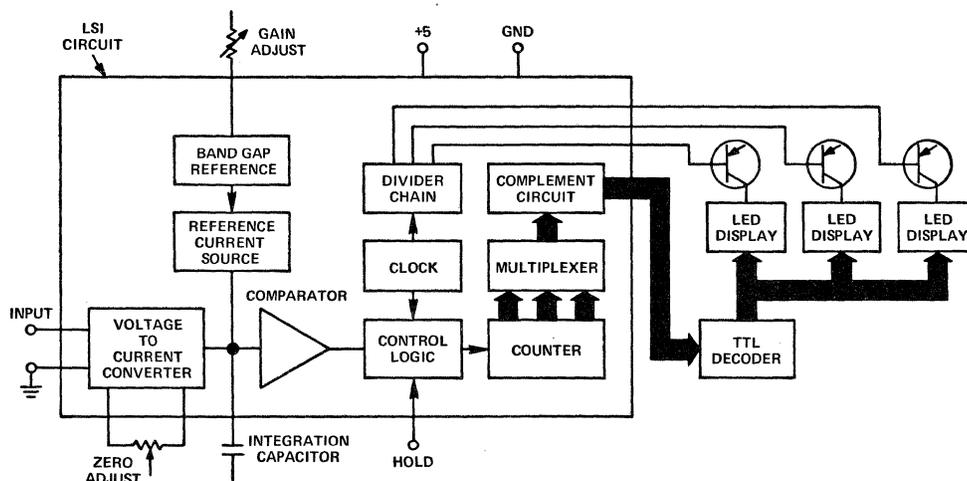


Figure 7. AD2026 block diagram.

I^2L is, in short, a rather promising technique for building monolithic A/D and D/A converters. At this writing, a monolithic 12-bit D/A converter and a monolithic 10-bit A/D converter are close to introduction as new products. They will employ a large part of the arsenal of proven Analog Devices bipolar IC technology, to wit, laser-wafer-trimmed thin-film resistors on an I^2L chip, combining complex logic and high-precision bipolar circuits, and including a buried-Zener reference.

• *Hybrids and Resistance Networks.* As of this writing, completely monolithic 12-bit high-speed (successive-approximations) A/D converters and completely monolithic 12-bit D/A converters with low-impedance voltage (op amp) outputs are not yet manufacturable in quantity with reasonable yields. If we consider the principal advantages of the monolithic technology to be low cost and small size (everything else being more-or-less equal), the next best substitute for monolithic is a dual in-line package (DIP) containing a form of hybrid construction employing a small number of chips on a substrate on which are fabricated both interconnections and resistors. Hybrid technology permits a happy compromise between the functional sophistication of modules and the small size and low cost of IC's.

Until monolithic devices having comparable performance are available, the AD572 A/D converter and the AD564 D/A converter, built with hybrid technology, meet the above requirements for complete 12-bit devices. The AD572 (Figure 8) employs the AD562 basic DAC chips, a reference, buffer-follower (for convenience), comparator, successive-approximations register, and logic circuitry, mounted on a ceramic substrate, which has been fabricated with the resistors and interconnections. The AD564 uses the basic AD562 plus a reference (in the 10V AD2700 class) and an output amplifier.

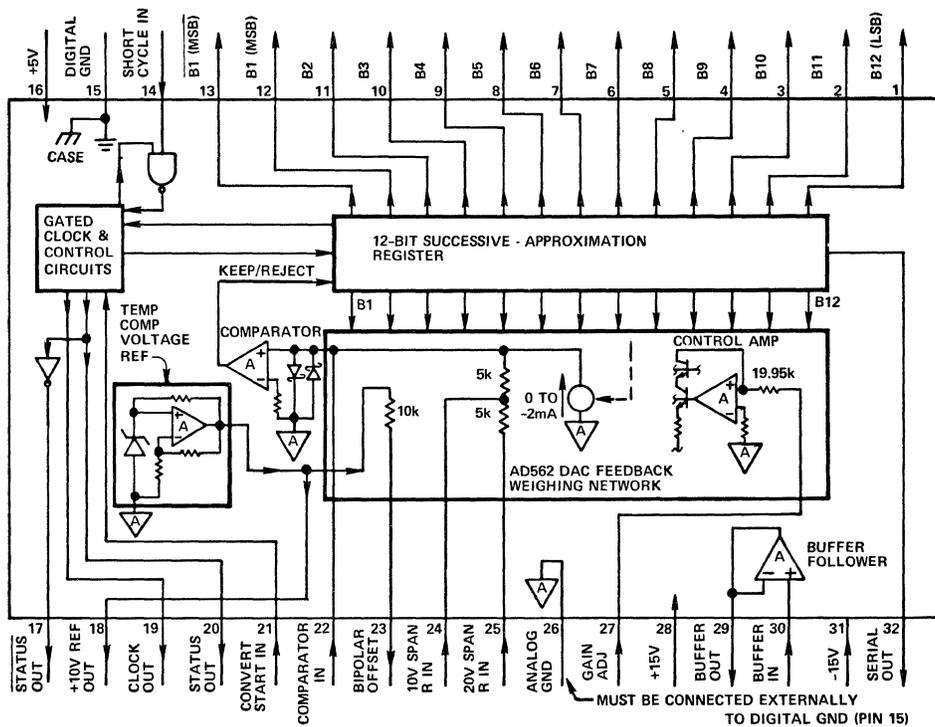


Figure 8. AD572 functional diagram & pinout.

In addition to the buried-Zener technology used in a number of monolithic products that require references, band-gap IC references are also used. The AD580, a 3-terminal reference capable of producing its 2.5V output at currents up to 10mA when operated from 5V logic supplies, is a simple example of the technique (Figure 9). Thin-film-on-silicon resistors help maintain its stability to within 10ppm/°C.

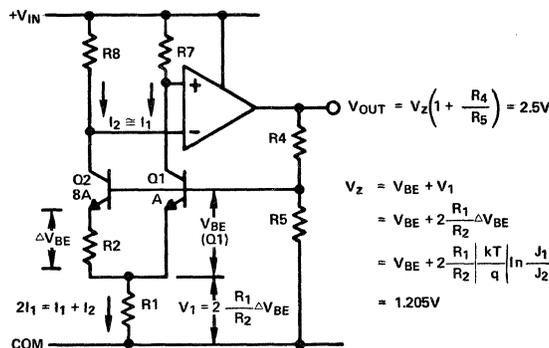


Figure 9. Basic bandgap-reference regulator circuit.

CIRCUIT TECHNIQUES, PERFORMANCE, AND APPLICATIONS

Having discussed the technological variety found in conversion IC's, considered the properties of devices using these technologies, and sated our Readers with generalities, let us now consider some of these devices in greater detail. Our purpose will not be to provide information so complete that the Reader can *design* IC conversion products. Rather, it is to provide: a working knowledge of the relationship between actual circuits and the principles outlined in Chapter II-1, some understanding of the relationship between design and specifications, and a few examples of applications that seem well-suited to each device.

THE AD7520 – A 10-BIT MONOLITHIC CMOS D/A CONVERTER¹

The AD7520 is a 10-bit multiplying digital-to-analog converter constructed on a single silicon chip. It consists of 10 CMOS (complementary metal-oxide semiconductor) switches and

¹Cecil, J. and Whitmore, J. "A 10-Bit Monolithic CMOS D/A Converter that Can Be Used for 4-Quadrant Multiplication," *Analog Dialogue* 8-1, 1974.

a thin-film-on-CMOS R-2R ladder network. The digital input, which responds to the wide voltage swings of CMOS logic, is also compatible with TTL/DTL logic levels. Two complementary current outputs are available for use with inverting operational amplifiers.

Besides the 10-bit resolution, the AD7520 family has maximum nonlinearities as low as $\pm 0.05\%$ of V_{REF} , nonlinearity temperature-coefficient of $2\text{ppm}/^\circ\text{C}$, and maximum feed-through error of $\frac{1}{2}$ least-significant bit ($LSB = 0.1\%$) at 100kHz . Typical settling time following a full-scale digital input change is 500ns .

In addition to a constant or variable reference (current or voltage), of either positive or negative polarity, the AD7520 requires one external operational amplifier for unipolar digitally set gains (2-quadrant multiplication) or two amplifiers for bipolar gains (4-quadrant multiplication).

The 74×96 mil ($1.9 \times 2.4\text{mm}$) chip, normally housed in a 16-pin hermetically-sealed ceramic dual in-line package, can also be made available in a flatpack or plastic DIP. It will operate from a single $+5$ or $+15\text{V}$ power supply, and it dissipates only 20mW , including the ladder network.

It can be used for D/A and A/D conversion, multiplication and division, programmable power supplies, digitally programmed filters, and digital-analog function generation. Besides unipolar conversion (of either polarity), offset-binary, two's-complement, and sign-magnitude bipolar operation can also be implemented.

CMOS D/A CONVERSION

Early commercially-available monolithic D/A converters were principally processed by conventional bipolar linear processing techniques. Before 1974, when the AD7520 was introduced, 10-bit conversion had been difficult to obtain with good yields (and low cost) because of the finite β of switching devices, the V_{BE} -matching requirement, the matching and tracking requirements on the diffused-resistance ladders, and the tracking limitations caused by the thermal gradients produced by high internal power dissipation.

All of these problems were solved or avoided with CMOS devices. They have nearly-infinite current gain, eliminating β problems. There is no equivalent in CMOS circuitry to a bipolar transistor's V_{BE} drop; instead, a CMOS switch in the *on* condition is almost purely resistive, with the resistance value controllable by device geometry. The temperature-tracking problems of diffused resistors were solved easily: they weren't used.

The R-2R ladder is composed of $2\text{k}\Omega/\text{square}$ silicon-chromium resistors (a $10\text{k}\Omega$ resistor has a very manageable length/width of 5:1), deposited on the CMOS die. While the absolute temperature coefficient of these resistors is $150\text{ppm}/^\circ\text{C}$, their tracking with temperature is better than $1\text{ppm}/^\circ\text{C}$. The feedback resistor for the output amplifier is also provided on the chip, to ensure that the DAC's gain-temperature coefficient is better than $10\text{ppm}/^\circ\text{C}$ by sidestepping the absolute temperature coefficient of the network.

Finally, the low on-chip dissipation of only 20mW (including the dissipation of the ladder network), in conjunction with the excellent tracking capabilities of the thin-film resistors, minimizes linearity-drift problems caused by internally-generated thermal gradients. It also helps to minimize the power and cooling requirements for circuitry that the AD7520 is used in.

Figure 10 shows a functional diagram of the D/A converter, which employs an inverted R-2R ladder.² Binary-weighted currents flow continuously in the shunt arms of the network; with 10V applied at the reference input, 0.5mA flows in the first, 0.25mA in the second, 0.125mA in the third, and so on. The I_{OUT_1} and I_{OUT_2} output busses are maintained at ground potential, either by operational-amplifier feedback, or by a direct connection to common.

The switches steer the current to the appropriate output lines in response to the individually-applied logic levels. For example, a "high" digital input to SW1 will cause the 0.5mA of the most-significant bit (MSB) to flow through I_{OUT_1} . When the digital input is "low," the

²The inverted R-2R ladder is one of the structures shown in Chapter II-1 (Figure 18).

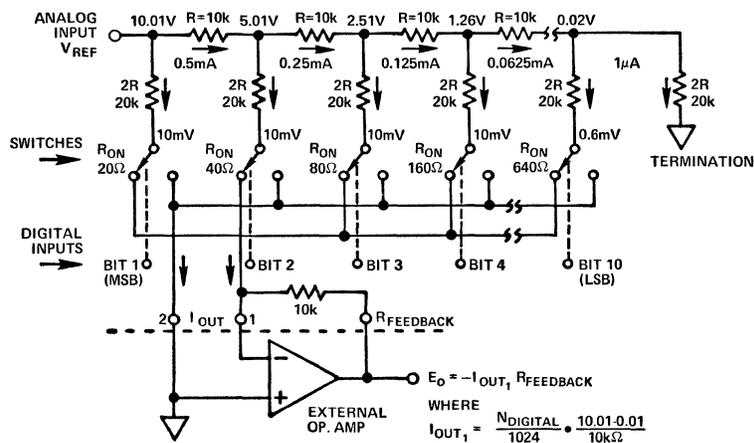


Figure 10. Functional diagram of the AD7520 d/a converter, with $V_{REF} = 10.01V$. Bits 5-9 are omitted for clarity.

current will flow through I_{OUT2} . If I_{OUT1} flows through the summing point of an operational amplifier and I_{OUT2} flows to ground, then “high” logic will cause the nominal output voltage of the op amp to be $-(0.5mA) \times (10k\Omega) = -5V$, for a positive reference voltage of 10V, while “low” logic will make the contribution of Bit 1 zero. With all bits *on* (i.e., “high”), the nominal output will be $-9.99V$. With all bits *off*, the output will be zero.

Linearity errors, and – more important – their variation with temperature, are affected by variations of resistance in both the resistors and the switches. As we have seen, the resistor-network tracking is excellent. However, it is natural to expect that the switches, while tracking one another, will not track the resistance network. With identical switches having realistic resistance values (say 100Ω), one would expect that, as temperature changed, the variation of resistance in the series legs would transform the network into an R - nR network, with n sufficiently different from 2 to destroy the binary character of the network and cause the converter to become non-monotonic.

The key to the linearity of the AD7520 is that the geometries of the switches are tapered so as to obtain *on* resistances that are related in binary fashion, for the first 6 bits. Thus, the nominal values of switch resistance range from 20Ω for the first bit, 40Ω for the second bit, through 640Ω for the last 5 bits. The effect is, as can be seen in Figure 10, to provide equal voltages at the ends of the 6 most-significant arms of the ladder ($0.5mA \times 20\Omega = 0.25mA \times 40\Omega$, etc. = $10mV$). Since this drop is, in effect, in series with the reference, it causes an initial 0.1% scale-factor (“gain”) error, which is well within the specifications but does not affect the linearity. Since the switches tend to track one another with temperature, linearity is essentially unaffected by temperature changes, and the gain error is held to within the $10ppm/^\circ C$ specification.

Ten-bit linearity could, of course, have been obtained by scaling the *on* resistance of all the switches to a negligible value, say 10Ω , but the switches would have required very large geometries, which would result in a 30% to 50% larger chip, at a substantial increase in cost.

Figure 11 illustrates one of the 10 current switches and its associated internal drive circuitry. The geometries of the input devices 1 & 2 are scaled to provide a switching threshold of

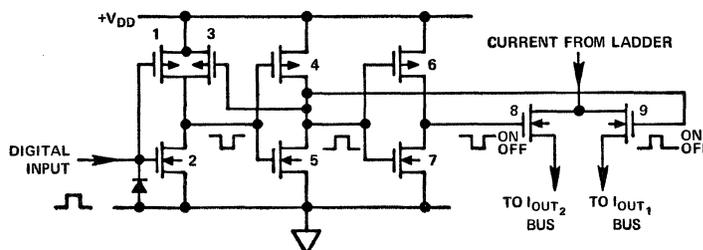


Figure 11. CMOS switch used in the AD7520. Digital input levels may be DTL, TTL, or CMOS.

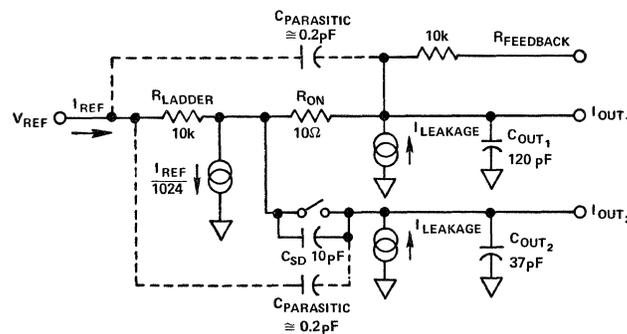
1.4V, which permits the digital inputs to be compatible with TTL, DTL, and CMOS. The input stage drives two inverters (4, 5, 6, & 7), which in turn drive the N-channel output switches.

EQUIVALENT CIRCUIT

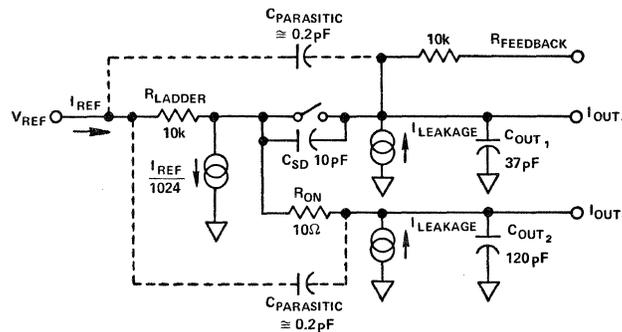
Figure 12 shows the equivalent circuit of the AD7520 at the two extremes of input, all inputs “high” (a) and all inputs “low” (b). V_{REF} (or I_{REF} , if a current reference is used) sees a nominal $10k\Omega$ resistance, regardless of the switch states. The current source $I_{REF}/1024$, represents a 1 LSB current loss through the $20k\Omega$ ladder-termination resistor, shown in Figure 1. R_{ON} , in this case, is the equivalent resistance of all ten switches connected to the I_{OUT_1} bus (a) or the I_{OUT_2} bus (b). Current-source $I_{LEAKAGE}$ represents junction- and surface-leakage to the substrate. Capacitors C_{OUT_1} and C_{OUT_2} are the output capacitances-to-ground for the *on* and *off* switches. C_{SD} is the open-switch capacitance.

The 1000:1 ratio between R_{ladder} and R_{ON} provides a number of benefits, all related to the small voltage drop across R_{ON} :

- V_{REF} can assume values exceeding the absolute-maximum CMOS rating, V_{DD} . For example, V_{REF} could be as large as $\pm 25V$, even if the AD7520's V_{DD} rating were only $+17V$.
- The nonlinearity temperature-coefficient depends primarily on how well the ladder resistances track. Since R_{ON} is only a small fraction of R_{ladder} , any R_{ON} tracking errors will be felt only as 2nd- and 3rd-order effects.
- The same argument holds true for power-supply variations. Any change of switch *on* resistance, as the power supply changes, will be swamped by the 1000:1 attenuation factor. Power-supply rejection is better than $1/3$ LSB per volt.
- If V_{REF} is a fast ac signal, the feedthrough coupling via C_{SD} , the open-switch capacitance, will be negligible, again because of the 1000:1 voltage stepdown. The parasitic capacitances from V_{REF} to I_{OUT_1} and I_{OUT_2} comprise the major source of ac feedthrough. Careful board layout by the user can result in less than $1/2$ LSB of ac feedthrough at 100kHz.



a. All digital inputs high



b. All digital inputs low

Figure 12. Equivalent circuits of the AD7520 D/A converter.

Since the *on* resistance depends only on the value of V_{DD} , not the current through the switch, and the resistance network is unaffected by V_{REF} , the full-scale output current (all bits “high”) is nominally $V_{REF}/10.01k\Omega$, less the “constant” current losses shown in Figure 12. This means that I_{OUT} is almost perfectly proportional to V_{REF} over the whole range from -10V to +10V. Equally important, the conversion linearity error (0.05%) is independent of the sign or magnitude of V_{REF} .

The extremely low analog-linearity error at constant digital input results in excellent fidelity to the input waveform, which suggests some interesting possibilities for the AD7520 in the calibration and control of gain in signal generators, high-fidelity amplifiers, and response-testing systems.

APPLYING THE AD7520

The two most common forms of application are in unipolar D/A conversion (2-quadrant multiplication) and bipolar offset-binary conversion (4-quadrant multiplication), shown in Figures 13 and 14. Where high speed is not desired, the output amplifier may be an AD741. For faster response, the AD518, AD505, or AD509 may be used, with appropriate compensation and a 10-20pF feedback capacitor.

Unipolar conversion. The response equation for Figure 13 is nominally

$$E_o = - \frac{N_{\text{binary}}}{1024} V_{\text{REF}} \quad (1)$$

Responses to typical codes are tabulated. Since V_{REF} may be positive or negative, two-quadrant multiplication is inherent. Circuit gain is easily trimmed by adjusting V_{REF} , inserting adjustable resistance in series with V_{REF} or R_{feedback} , or by tweaking scale factors elsewhere in the system. As noted elsewhere, once set, using low-TC trim resistors, gain stability with temperature is excellent.

Unlike truly passive potentiometers, CMOS devices, like the AD7520 (and the AD7522 and AD7570, to be discussed further on) *must* have their analog outputs at ground level to maintain conversion linearity in the forward direction and to protect the switches in the reverse direction (in other words, their output voltage compliance is negligible). Therefore, their outputs should be connected to op-amp summing points for all applications save for nulling (e.g., with comparators in A/D converters). In any event, it is a sensible practice to *always* use a Schottky diode, connected between the current output and ground, as shown in Figure 13, even if – for the sake of clarity – it is omitted from an application sketch.

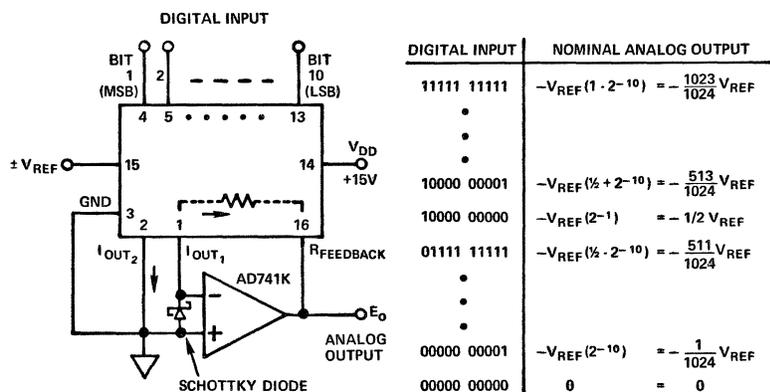


Figure 13. The AD7520 as a unipolar binary digital to voltage converter (2-quadrant multiplier).

Bipolar conversion. The offset binary response equation for Figure 14 is nominally

$$E_o = - \left[\frac{N_{\text{binary}}}{512} - 1 \right] V_{\text{REF}}$$

Responses to typical codes are tabulated. If the MSB is complemented, the conversion relationship will be recognized as appropriate for a 2's-complement input, but with a negative scale factor. The MSB determines the sign, and the last 9 bits determine the magnitude in 2's complement notation. Since V_{REF} may be positive or negative, 4-quadrant multiplication is inherent.

In this configuration, I_{OUT2} , which is the complement of I_{OUT1} , is inverted and added to I_{OUT1} , halving the resolution (of each polarity) and doubling the gain. The $10M\Omega$ resistor corrects for a $1/1024$ difference (inherent in this technique) between I_{OUT1} and I_{OUT2} at zero (10000 00000). A2 is shown as a current inverter, but it might also be a voltage inverter, if the AD505 is used.

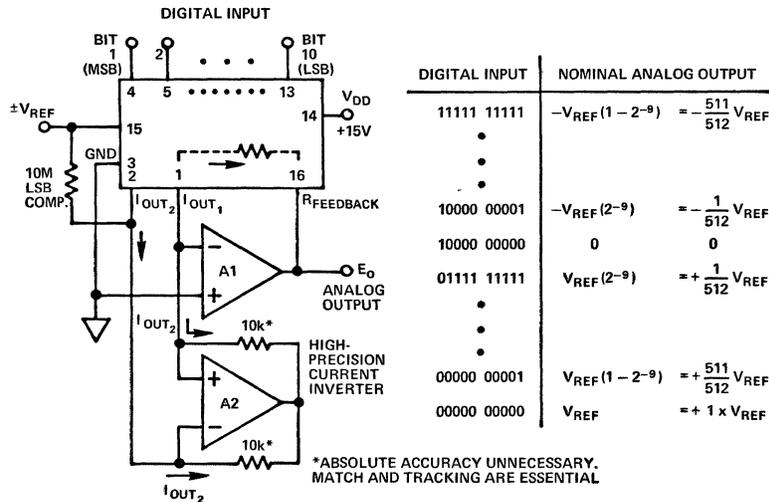


Figure 14. The AD7520 as a bipolar offset-binary digital-to-voltage converter (4-quadrant multiplier).

If sign-magnitude coding is desired, to obtain bipolar conversion with the full 10-bit-plus sign resolution, the output of the unipolar conversion circuit may be fed into a sign-magnitude converter, such as Figure 15. An AD7510 DI quad switch will handle two such circuits.

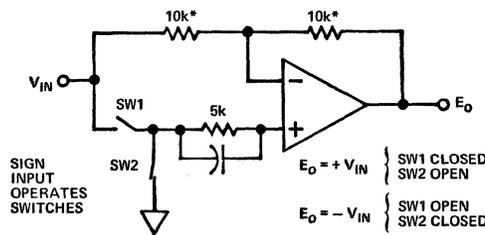


Figure 15. Sign-magnitude to bipolar converter.

ANALOG DIVISION

Since one form of analog division circuit is a multiplier in a feedback loop, one might consider the divider circuit² shown in Figure 16. In this circuit, the feedback current from the converter's "reference" input to the summing point of the op amp is proportional to (i.e., multiplied by) the digital number; but it must also be equal to the current developed through the input resistor. Therefore the op-amp output is constrained to depend on the ratio of the input signal to the gain value of the digital number. Note that the AD7520 in such an application is inherently a 2-quadrant divider, since the input signal (and the inverted output) can be either positive or negative. Connected as shown, the gain magnitude varies from a minimum of $1024/1023$ to (theoretically) $1024/0$, the open-loop gain of the op amp; the largest controlled gain is $1024/1$. At the higher gains, accuracy is lost because the feedback

²Whitmore, J. "Ways of Using the AD7520," *Analog Dialogue* 8-2, 1974.

attenuation for small numbers may only be accurate to within ½LSB; for example, at a gain of 1024, if the LSB has an error of 10%, the gain will be in error by that amount. Naturally, accuracy rapidly improves with increasing denominator magnitude, and the error will typically be less than 0.05% at full-scale denominator, after adjustment.

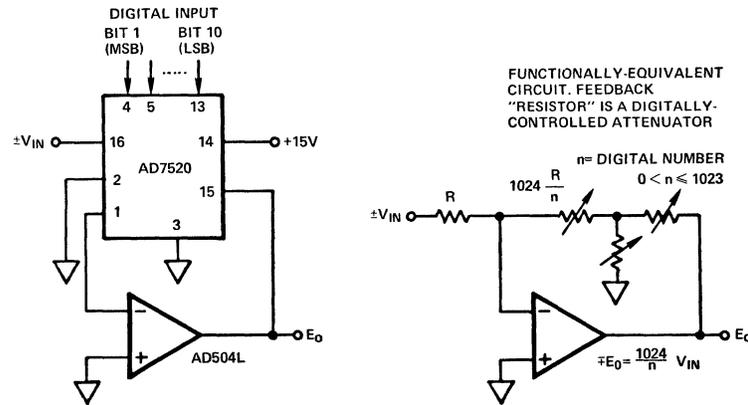


Figure 16. An analog-digital divider.

SINGLE-SUPPLY APPLICATION

In computerized process-control systems,³ digital-to-analog converters are typically used to manipulate set-points and operate valves. General-purpose DAC's, such as the AD7520, usually involve inverting op amps, which call for dual power supplies. However, one-sided supplies are highly desirable because of their lower cost, better reliability, and their compatibility with the 4–20mA range used in transmission of electrical control signals in process-control systems.

The single-supply scheme of Figure 17 employs the AD7520, with an LM324 single-supply quad op amp, and an AD2700 precision 10V reference, to provide a jumper-selected choice of two output voltage ranges, 0–10V and 2–10V. The latter range can be directly transduced into 4–20mA and 10–50mA current ranges appropriate for control systems, by schemes such as that shown.

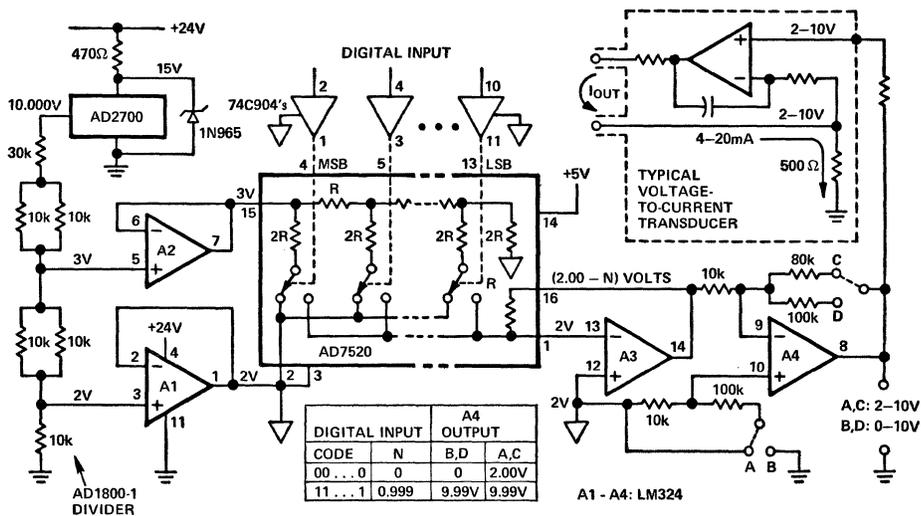


Figure 17. Single-supply 10-bit DAC circuit.

In the circuit of Figure 17, the +24V supply is tapped at +5V for TTL logic levels. The AD2700 reference develops a precise 10 volts without needing adjustment. It is stepped down to +3V and +2V, which appear at the outputs of followers A2 and A1. The 2V output of A1 becomes the reference-ground level for the AD7520 DAC, the inverting op amp, A3, and the two 74C904 Hex Non-Inverting Buffers, which drive the logic inputs of the AD7520 (10 of the 12 buffer channels are used).

³Clark, V.R., "D/A Conversion with a Single-Supply Circuit," *Analog Dialogue* 10-1, 1976.

The net 1V reference voltage applied to the DAC is scaled in proportion to the digital input number (N) and inverted by amplifier A3 at unity gain. The output of A3 swings from 2V to 1.001V as N varies from 0 to $1 - 2^{-10}$. Depending on the jumper connections, the 0-to-full-scale output swing of A4 is either 0–10V or 2–10V. The 2–10V range ($E_4 = 2 + 8N$ volts) can directly scale a current-transducer output, such as the one shown, for 4–20mA or 10–50mA. The actual system uses a proprietary design, capable of generating a grounded or floating source or sink current.

AUDIO-CIRCUIT APPLICATIONS.⁴

High-resolution, high-linearity multiplying DAC's that handle both polarities of analog input become quite attractive to the designer of audio signal-processing equipment when these benefits are combined with wide bandwidth and low cost.

Monolithic IC DAC's available before the advent of the AD7520 generally had less resolution and a limited range of reference variation. The lack of both reference-voltage source and output amplifier is not an important limitation in audio use. In fact, the number-one advantage is that the reference-input voltage swing can exceed $\pm 10V$, with excellent linearity and bandwidth. Although one would expect a "multiplying DAC" to have this capability, not all types possess it fully.

AD7520's can be used with bipolar voltages from volts down to millivolts. Correct and linear ratiometric operation under such conditions makes them ideal scaling elements for audio signals. Since they can be viewed as digitally-programmable attenuators, they can marry high-quality and audio signal-processing circuits to digitally based systems under micro-processor control.

Besides the classical DAC specs of conversion linearity, resolution, etc., the special considerations for audio use include distortion, noise, and crosstalk in the "off" state.

Typical measurements of distortion are of the order of 0.05% or less over the audio band. This is due to the linearity enforced by the thin-film R-2R ladder, which ensures a linear summing-point current in the presence of a varying reference (input) voltage at a given digitally set gain.

Noise is a parameter that can be determined from the data sheet; it is determined by the thin-film network's nominally 10k Ω characteristic resistance. This contrasts favorably with some active types of DAC's, which are noisier.

Reference-input feedthrough is specified on the data sheet as 10mV p-p (max) for 20V p-p input at 100kHz (-66dB). This, being but one point on a curve, doesn't tell the whole story. At lower frequencies, feedthrough is much less, with a floor of $\leq -90dB$ at 1kHz (Figure 18). Feedthrough is essentially capacitively coupled crosstalk. It is layout-sensitive.

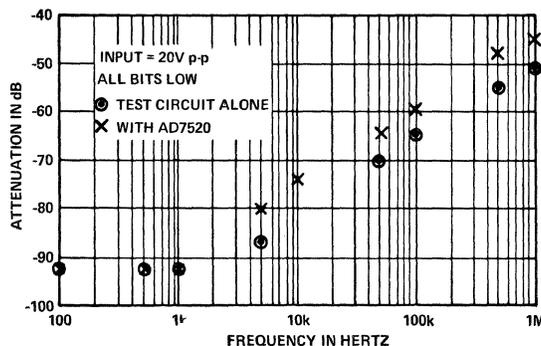


Figure 18. AD7520 feedthrough measurement.

Control-signal feedthrough is undesirable in audio gain control, since it can cause thumps, pops, or clicks. Because there is no bias current in the AD7520/21/22, the output contains the desired signal current only, avoiding dc level shifts. The narrow switching spikes can be filtered without loss of bandwidth.

⁴ Jung, W. "Audio Applications Ideas for CMOS DAC's," *Analog Dialogue* 10-1, 1976

It is interesting to consider the AD7520/21/22 accuracy in relation to the needs of audio level control. Without trim, the full-scale gain error is typically 0.3%, or, in conventional audio parlance, $\pm 0.026\text{dB}$. Even adding the loosest (conversion) nonlinearity† error, the gain error is still only $\pm 0.043\text{dB}$, adequate for a great number of audio applications, without trimming or tweaking. Remember that 1dB is close to the threshold of human perception of gain changes.

For applications where it is desirable to trim the DAC gain exactly to unity, given the possibility that it may be either high or low, resistance may be added in series with either the input (V_{REF}) terminal or the feedback terminal. Figure 19 shows a way of dealing with either contingency with one pot.

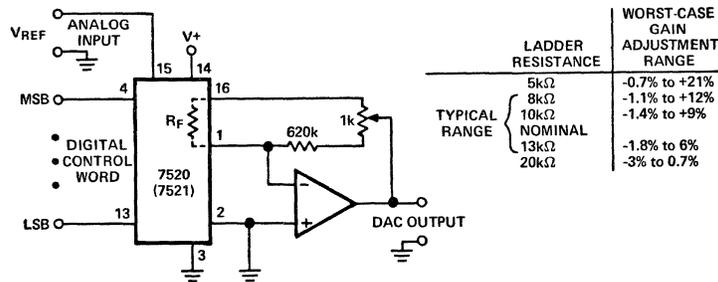


Figure 19. Single-control trim for gain calibration, allowing for a large range of absolute ladder-resistance variation.

Figure 20 shows a basic circuit using the AD7520 as an audio gain control. A low-cost AD301A, used as the output buffer, is operated in the feedforward mode, for a gain-bandwidth of 30MHz and a $10\text{V}/\mu\text{s}$ slewing rate. This combination, using the lowest-cost “J”-suffix DAC, provides perhaps the most cost-effective, high-performance combination for an audio gain-control of this class. It can of course also be used as a general-purpose DAC, with device choice tailored to desired performance. Settling time to $\frac{1}{2}\text{LSB}$ (10 bits) is $6\mu\text{s}$.

In general, the application of high-speed-DAC circuits to audio use can give rise to some serious problems. For instance, if the channel gain is to be manipulated while signals are present, large instantaneous gain changes in the presence of signal peaks will almost guarantee annoying audible switching-transients due to the abrupt change in level.

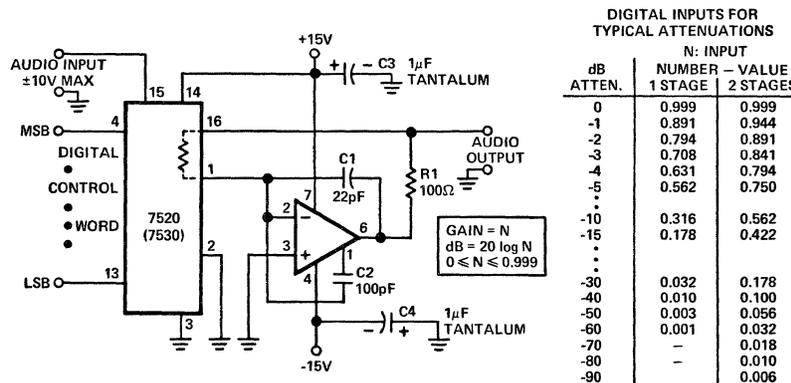


Figure 20. Inexpensive, high-performance gain control.

As a remedy, one might restrict gain-switching to times when the signal is near zero. A more-pleasing and satisfactory approach is to spread the gain change over about 50ms or more by digitally “ramping” it, using a clock and preset counter. If sufficient resolution exists, the staircase effect should be imperceptible. With an 8-bit converter, this permits 48dB of staircasing. Avoid slew-limiting in the DAC output amplifier; it can cause noxious distortion for sufficiently large gain steps, another reason for using controlled-gain steps and fast amplifiers.

†Conversion-linearity errors affect only gain, not analog linearity.

Additional gain range can be obtained by cascading decade blocks of gain, or by cascading DAC's, with common digital input. If you wish to obtain the natural benefits of equal-dB gain steps, the digital number applied to the DAC(s) should vary exponentially. For m cascaded DAC's with $-k$ dB of attenuation, the value, N , of the common digital input should be

$$N = (10)^{k/(20m)} \quad (1)$$

This can be achieved via software instructions in a computer system; it can also be achieved by means of programmable read-only memory (PROM), between the counter output and the DAC(s). Note that only about 2 significant digits are needed for accuracy to within 1dB, from the examples in the table (Figure 20).

Figure 21 illustrates in principle a variation of the basic gain controller which can be used to steer or "pan" an audio signal between two output channels, another common audio processing requirement. The two gains are simply made complementary. Thus, the signal will be fully *left* for all 1's, full-*right* for all 0's, and deployed equally for just the MSB on.

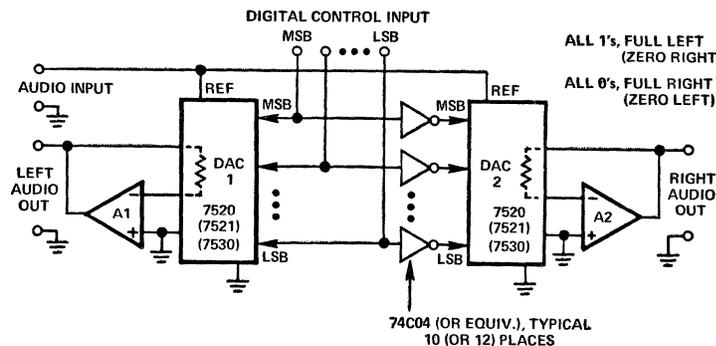


Figure 21. Digitally-programmed audio panner.

In a simpler version (Figure 22) a single DAC is used. Here, the I_{OUT2} line of a 7520, normally grounded, is used to drive a second summing amplifier with an external feedback resistor, R_{f2} . Since the current at I_{OUT2} is inherently the complement of I_{OUT1} , the circuit will work as a complementary panner. The drawback is the necessity to trim R_{f2} for equal channel gains (MSB on); since the external resistor will in general not track the network, the panner may not retain its accuracy for wide temperature variations. However, the method is simple and attractive for non-critical applications.

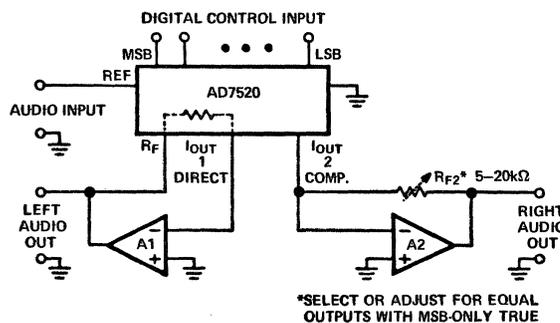


Figure 22. Simplified audio panner.

DAC's are useful for generating, as well as controlling, signals. Figure 23 shows a simple scheme for digitally programming the output frequency of a standard integrator-comparator function generator^{5,6}. The timing resistor (the input resistor to the integrator) is replaced by the DAC's R-2R ladder. Since frequency is proportional to the integrator input current, it will be proportional to the digital input to the DAC.

A calibration control with wide latitude is needed because of the loose tolerance on absolute value of the R-2R ladder resistance; also, as noted above, tracking errors with temperature

⁵ *Nonlinear Circuits Handbook*, Analog Devices, Inc., 502pp., \$5.95 (soft).

⁶ *Audio IC Op-Amp Applications*, W.G. Jung, Howard W. Sams & Co., Inc. Indianapolis, Indiana 46206 (soft).

will limit stability. Fast amplifiers, such as the AD301A (with feedforward in the integrator) are cost-effective.

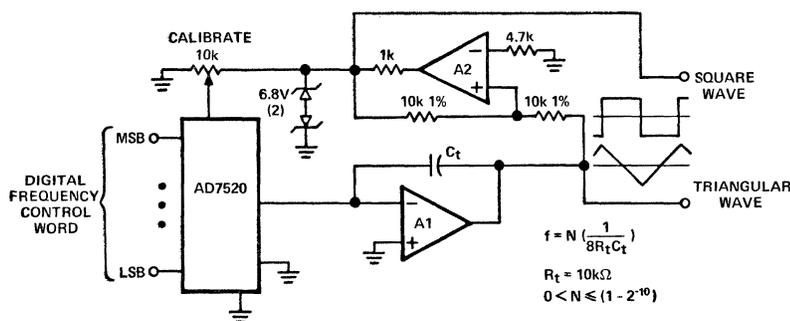


Figure 23. Programmable function generator; p-p amplitude of both waveforms is $\cong 15V$.

There are myriad uses for these versatile DAC's; many have been documented here in the past, and more are sure to come. In audio alone, programmable oscillators, equalizers, filters, etc., may provide the Reader with food for thought.

A final word. Here are some suggestions for getting best results with the AD7520 and similar CMOS DAC's:

1. Tie unused CMOS digital inputs either high or low; don't leave them open.
2. Remember that the current-summing junction is loaded by a capacitance from 40pF to 120pF. If fast amplifiers are used, phase compensation is required for stability (e.g., the usual shunt feedback capacitance across $R_{FEEDBACK}$).
3. The amplifier offset should be minimized to maintain device linearity.
4. The I_{OUT1} and I_{OUT2} terminals should never be allowed to go negative by $1 V_{BE}$ drop – a Schottky diode to ground, as in Figure 13, is recommended.

THE AD7522 – A DOUBLE-BUFFERED 10-BIT CMOS MULTIPLYING DAC⁷

The AD7522 is a systems-compatible 10-bit multiplying D/A converter, fabricated on a single $3 \times 2.2\text{mm}$ (118 x 89 mil) silicon die, and packaged in a 28-pin plastic or ceramic dual in-line package. Like the AD7520, it has 10 SPDT N-channel current-steering switches and a thin-film-on-CMOS R-2R ladder attenuator for current weighting. *In addition*, it has a dual-rank input storage system consisting of 10 "D"-type level-triggered holding latches and a 10-bit edge-triggered serial/parallel input-loading register (which in turn consists of 2 controllable "bytes", of 8- and 2-bit capacity), as was shown in Figure 2 of this chapter.

Basic unipolar operation (either fixed-reference or 2-quadrant multiplication) requires only the addition of an external positive-or-negative, constant-or-variable, "reference" voltage or current and an operational amplifier (Figure 24). For bipolar conversion (4-quadrant multiplication), with offset-binary or 2's complement coding, one additional operational amplifier is needed (see Figure 14).

The main (V_{DD}) supply requires a nominal $+15V @ 2\text{mA max}$; $1\mu\text{A}$ is typical, since most of the current is required only during switching. The choice of the logic (V_{CC}) supply depends on the logic-interface requirements. For example, if $V_{CC} = +5V$, the digital inputs are TTL-compatible. If $V_{CC} = +10V$ to $+15V$, the digital inputs-and-outputs are CMOS compatible.

Three grades of conversion linearity are offered – 8, 9, and 10 bits. Typical current-settling time following a full-scale code change on the digital inputs is 500ns.

The most-interesting aspect of the AD7522 to the system designer is the DAC's double-buffered input structure, offering tremendous versatility, yet still seldom found, even in

⁷Whitmore, J. "Monolithic 10-Bit CMOS Multiplying DAC Provides Direct Interface to Data-Bus Inputs," *Analog Dialogue* 9-3, 1975.

discrete-module D/A converters. Salient features include:

1. Logic-controlled choice of serial or parallel loading.
2. A "load/display" choice, which either allows new data to update the DAC, or locks out unwanted data appearing at the digital inputs. If the AD7522 is used with a CPU data bus, this "lockout" function allows the CPU or other I/O peripheral to place data on the bus without altering data that was previously loaded into the AD7522.
3. Byte-serial (or parallel) loading allows a 10-bit word to be loaded into the DAC from either an 8-bit micro-computer data bus, or from a 10-or-more-bit paralleled line.
4. A serial *output* allows recovery of data from the input register.
5. A short-cycle feature allows 8 bits, to the MSB, to be loaded serially.

A summary of the AD7522 functions, and where to find them in Figure 2, is given in a box on the next page.

The advantages of ADI's thin-film-on-CMOS process, again briefly summarized, are:

- High logic density and low dissipation (hence good yields and low cost).
- No β and V_{BE} problems.
- Since switches are bidirectional, both polarities of analog signals are inherent.
- SiCr resistor networks have better linearity and tracking than diffused resistors.

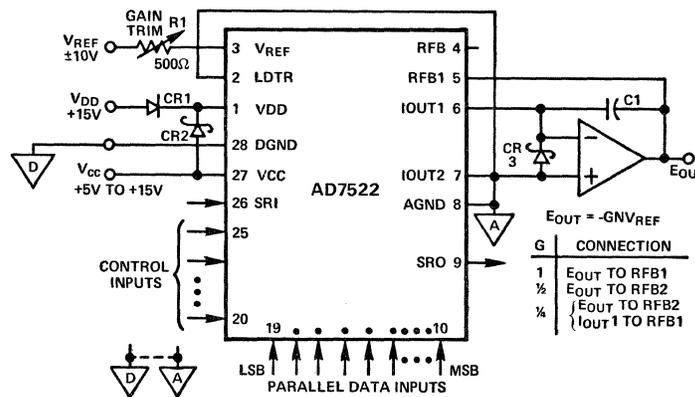


Figure 24. Connecting the AD7522 for unipolar D/A conversion. N is a fractional 10-bit binary number from 0 to $(1 - 2^{-10})$.

APPLICATIONS

The AD7522 can perform all of the conversion functions that are performed by the AD7520, but with the added flexibility of communication with digital systems. However, as a second-generation DAC, it has a few improvements that facilitate analog applications as well. First of all, there are separate analog and digital ground returns. Figure 24 shows how the AD7522 is connected for a unipolar conversion relationship. The feedback resistor is center-tapped, which allows a choice of full-scale gain of 1, $\frac{1}{2}$, or $\frac{1}{4}$. The termination of the ladder, instead of being grounded internally, is brought out to a terminal; this permits bipolar (4-quadrant multiplier) circuits to be instrumented with fewer external resistors than is the case with AD7520.

Two, among many, of the digital-communication possibilities are shown in Figures 25 and 26. Figure 25 illustrates serial operation, and Figure 26 shows how the AD7522 might be connected to a microprocessor bus for byte-serial updating.

It is easy to see that it is a simple matter for a microprocessor to first load the 8 least-significant bits into the 8-bit register, then load the two most-significant bits into the 2-bit register, and finally, to strobe 10-bit data into the output register, for the D/A converter. Note that the DAC register can also accept data in the form of a stream of 10 serial bits — and shift them out as well as in.

(Refer to Figure 2)	FUNCTION	PIN NO.	MNEMONIC NOTATION
DIGITAL – Data (positive-true with respect to I_{OUT1})			
	Parallel Data Input , Data-Bit 9 (MSB) to Data-Bit 0 (LSB) ⁸	10–19	DB9 through DB0 ⁸
	SeRial Input	26	SRI
	SeRial Output (NRZ) – Auxiliary output for recovering data stored in the input register	9	SRO
DIGITAL – Control			
	Serial/Parallel Control – If “0”, parallel data will be loaded into input registers DB0-DB9 when LBS and HBS are exercised; if “1”, serial data will be shifted through input registers when clocked in with LBS and HBS.	21	SPC
	High-Byte Strobe – In the <i>parallel</i> mode, positive edge strobes parallel data appearing on DB8 and DB9 into the input register; in <i>serial</i> , positive edges advance data through the input shift register.	25	HBS
	Low-Byte Strobe – Same functions as HBS, for DB0 through DB7	24	LBS
	Load/Display DAC Strobe – If “0”, AD7522 is in “display” mode, digital activity in input register is locked out; if “1”, data in the input register is strobed into the DAC.	22	LDAC
	Short-Cycle (8 bits) – In <i>serial</i> , if “0”, 2 LSB’s are bypassed for proper loading of 8 bits; if “1”, a full 10-bit serial word is accepted.	20	$\overline{SC8}$
ANALOG			
	Reference Input – Constant or variable ac or dc voltage in the $\pm 25V$ range is proportionally scaled (gain-adjusted) by the input digital word.	3	V_{REF}
	Output Current – Normally connected to summing point of the output op amp; bit-currents flow for “1” DB’s.	6	IOUT1
	Complementary Output – Normally grounded (unipolar) or connected to summing point of inverting op amp (bipolar); bit currents flow for “0” DB’s.	7	IOUT2
	Feedback Resistor (F.S. Gain = 1) One end is connected internally to I_{OUT1} . RFB1 is connected to op-amp output for normal unity-gain operation, or to summing point for gain of $\frac{1}{4}$; no connection for gain of $\frac{1}{2}$.	5	RFB1
	Feedback Resistor Center-Tap (F.S. Gain = $\frac{1}{2}$) —Connected to op-amp output for gain of $\frac{1}{2}$ or $\frac{1}{4}$.	4	RFB2
	Ladder Termination – Grounded for unipolar gain; connected to I_{OUT2} for bipolar gain.	2	LDTR
SERVICE			
	Main Supply – +15V nominal	1	V_{DD}
	Logic Supply – +5V for TTL compatibility; +10V to +15V for CMOS compatibility	27	V_{CC}
	Digital Ground	28	DGND
	Analog Ground – Back gate of the DAC’s N-channel single-pole, double-throw (SPDT) current-steering switches.	8	AGND

⁸ See the discussion, “A Note on Bit-Labeling,” near Figure 12 of Chapter I-4.

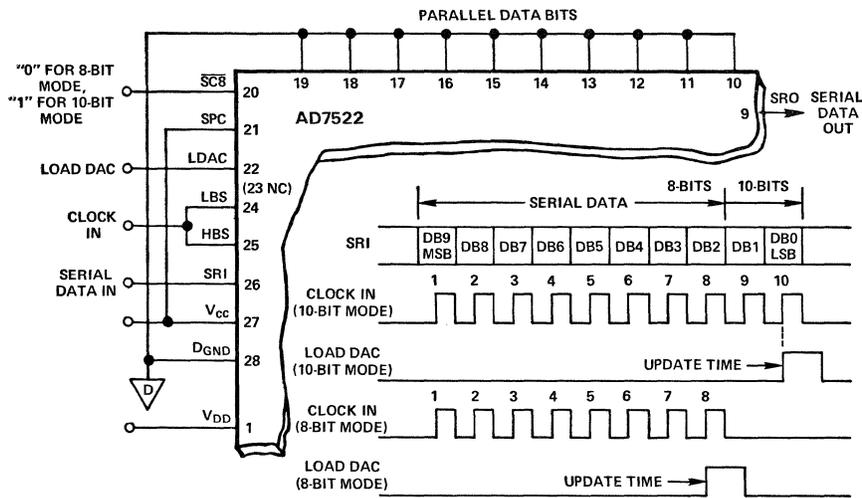


Figure 25. Serial 8- and 10-bit loading. Analog connections omitted for clarity.

Figure 26 shows how the AD7522 is connected into an 8-bit data bus. The bus is wired directly to the 8 least-significant bits; and the two most-significant bits of the converter are wired to the two least-significant bits of the bus.⁸

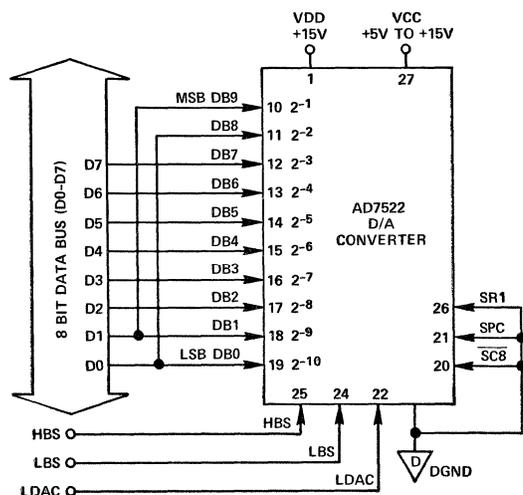


Figure 26. AD7522 - Connection for 2 byte operation.

Figure 27 shows two AD7522's (configured as in Figure 26), interfaced to an "ideal" microprocessor as memory. Since the AD7522 was designed as a compromise for both parallel and byte-serial operation, the external address-decoding logic is necessary as shown. Nevertheless, the interface is extremely simple and can allow either simultaneous or non-simultaneous update of the two D/A converters. The *or* gates allow a single memory address to update the output registers of both D/A converters simultaneously. It is worth noting that many μ P's (the 8080 included) incorporate 16-bit data instructions, which would allow the processor to output the data to both converters with a single *memory-write* instruction.

THE AD7570 - A 10-BIT SUCCESSIVE-APPROXIMATIONS CMOS A/D CONVERTER⁹

The AD7570 is a 10-bit Analog-to-Digital converter on a single 120 x 135 mil (3 x 3.4mm) chip, packaged in a 28-pin dual in-line hermetically-sealed ceramic enclosure. It consists (Figure 3) of a 10-bit D/A converter and the associated logic circuitry required to perform a conversion using the successive-approximations technique. Its analog inputs can be either

⁸ See the discussion, "A Note on Bit-Labeling," near Figure 12 of Chapter I-4.

⁹ Whitmore, J. and Van Aken, R. "10-Bit Monolithic CMOS A/D Converter," *Analog Dialogue* 9-2, 1975.

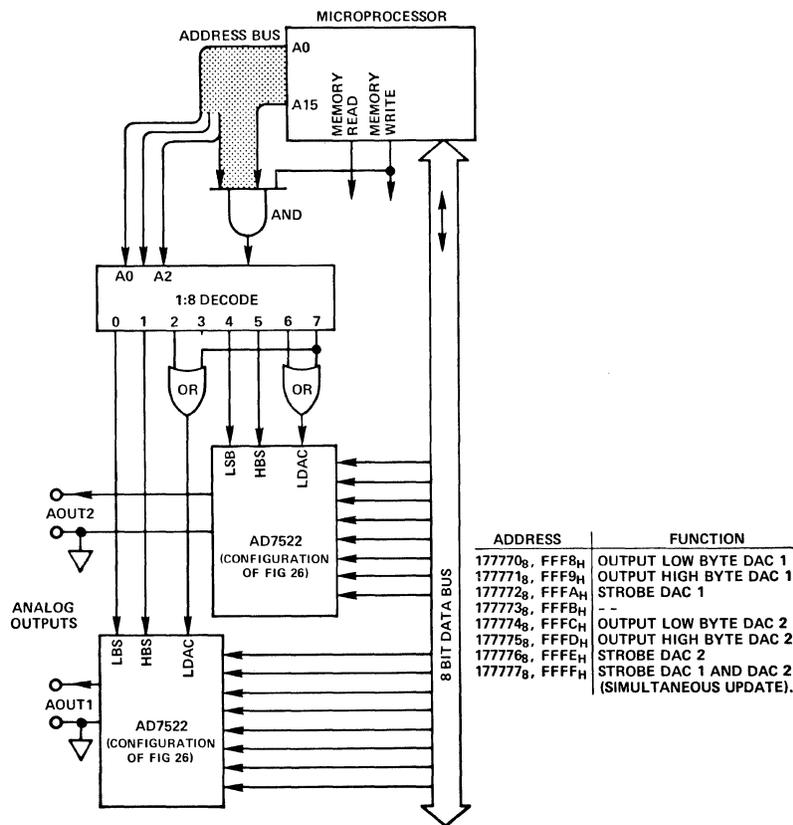
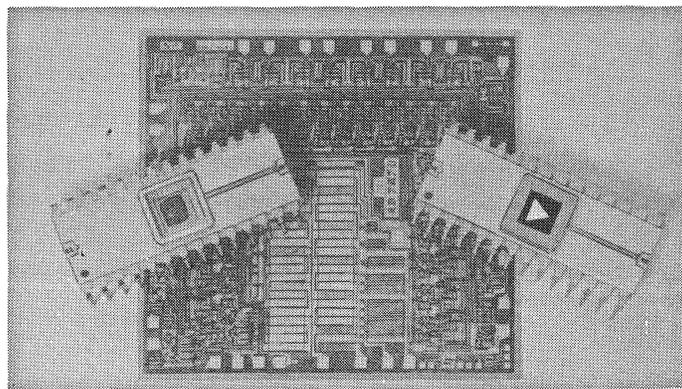


Figure 27. Interfacing multiple AD7522's to a microprocessor.

single-ended (of either polarity) or bipolar using an external inverting op amp. It interfaces with DTL/TTL or CMOS logic and has both serial and parallel outputs, with a number of interesting features designed to make it readily usable in complex data-acquisition systems (for example, with 8-bit microprocessor busses).

Its external operational requirements are 20mW of power (V_{DD} of +15V and V_{CC} of 5 to 15V), an external reference (which allows ratiometric operation and choice of input polarity), an external RC circuit to determine the internal clock frequency, or an external clock (for a wide range of conversion frequencies), and a comparator, such as the AD311 (for best tradeoff between accuracy, conversion-speed, and cost). For bipolar operation, a low-cost external op amp preconditions the analog input.



The AD7570 will accurately digitize signals having full-scale ranges from nearly $\pm 25V$ down to levels limited only by the comparator's ability to detect submillivolt changes. This is a direct consequence of the use of a highly linear on-board multiplying D/A converter (closely related to the AD7520), which can accept a wide range of reference voltage. Normal operation is specified with 10V reference.

Available with 8- or 10-bit linearity (J or L versions, short-cycle-able to 8-bit resolution for increased speed), 40 μ s conversion time (10 bits), and $\pm\frac{1}{2}$ LSB differential nonlinearity (over the temperature range), the AD7570 has a gain-temperature coefficient better than 10ppm/ $^{\circ}$ C.

MICROPROCESSOR CAPABILITY

As noted above, the AD7570 is specifically designed for ease of use in "data-bus" systems, where its three-state outputs are under external control. There are several features of especial interest:

- The parallel data outputs⁸ (bits 0-9) and the conversion status line are "three-state", that is, they are essentially disconnected from the common data bus until appropriate interrogation signals are received. (Data ready? High bits? Low bits?)
- The two most-significant bits and the 8 lower bits can be separately interrogated: this permits all 10 bits to be furnished on an 8-bit common data-bus in two bytes.
- The serial output (non-return-to-zero) and an associated synchronized clock output are also provided with 3-state outputs. The serial output is generated as the conversion proceeds; it and its associated SYNC output float at other times. To interrogate it, in bus applications, a conversion is started.
- The AD7570 can, of course, also be used with fully-committed connections, by connecting the three-state control inputs to the appropriate logic levels for the desired permanent mode of operation.

ADVANTAGES OF CMOS

The most-obvious reason for using CMOS construction is the low power dissipation. For example, an inverter consists of a stack of two complementary devices. When one is *on* (low voltage drop), the other is *off* (low leakage current). Since the output is always very near one or the other power-supply rail (except when switching), little continuous power is dissipated. The total power drain of the AD7570 is 20mW.

The low dissipation allows greater circuit density. Besides this, the CMOS process employed in the AD7570, which involves a two-layer metal-interconnect scheme, allows a 30% further reduction in chip size, to a reasonable, manufacturable 120 x 135 mils (3 x 3.4mm), with good yield.

The most important advantages of CMOS are realized in the D/A converter, which is the critical element in a successive-approximations converter. This topic has been covered in substantial detail in relation to the design of the AD7520, which the AD7570's DAC very

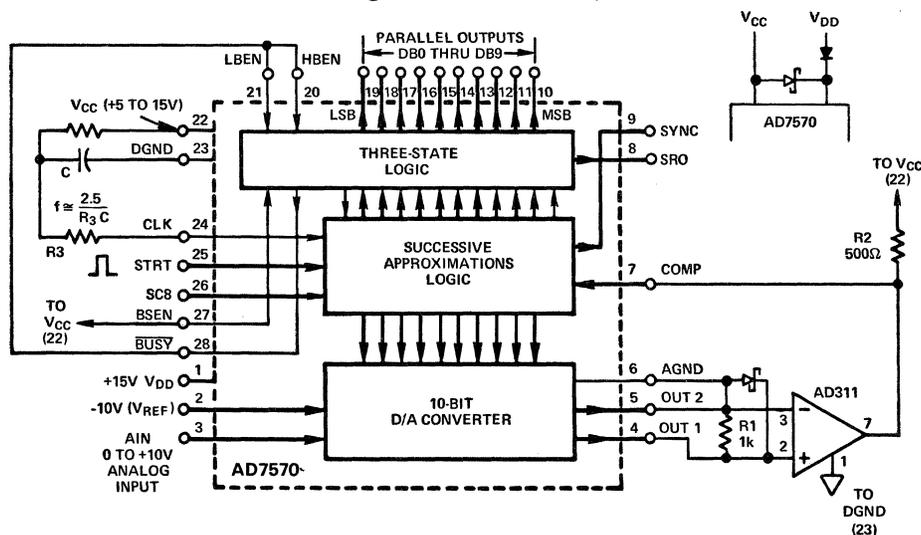


Figure 28. Operational connections for A/D conversion with positive (unipolar) analog input and internal clock. Parallel outputs are enabled when status (BUSY) goes high. The protective diodes indicated should be used in all applications.

⁸See the discussion, "A Note on Bit-Labeling," near Figure 12 of Chapter I-4.

much resembles. Briefly, the deposition of a thin-film high-precision R-2R ladder network on a chip with low-dissipation CMOS switches eliminates problems caused by: finite transistor β and its variations, transistor V_{BE} and its variations, diffused-resistor matching and tracking, and drifts of gain and linearity caused by thermal gradients on the chip (as a result of sizeable dissipations). Though the absolute temperature coefficient of the silicon-chromium resistors used in the AD7570 is about $-150\text{ppm}/^\circ\text{C}$, they track to within $\pm 2\text{ppm}/^\circ\text{C}$; the result is an overall gain tempco better than $10\text{ppm}/^\circ\text{C}$.

HOW THE AD7570 WORKS

Figure 28 is a functional diagram of an AD7570, connected for 10-bit unipolar A/D conversion; Figure 29 is a typical timing diagram showing what happens at the various terminals, and the sequence. (If you are perplexed about the designation or function of any of the terminals, Figure 3 and the table on the next page may be helpful.)

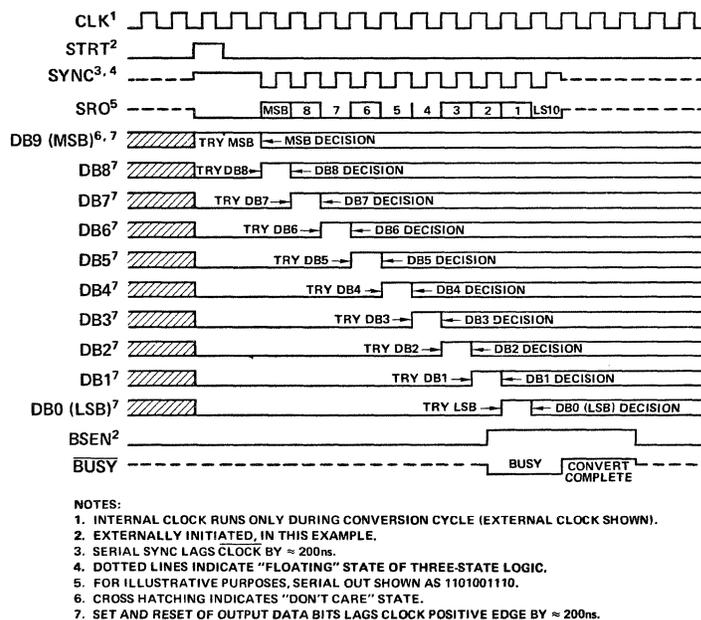


Figure 29. AD7570 timing sequence with externally-initiated start, clock, and BUSY -ENABLE, and parallel outputs continuously enabled.

In the successive-approximations technique (Chapter II-1) the output of a D/A converter is compared against the analog input for a succession of combinations of digits. When the *start* signal is given, the MSB latch output (appearing at DB9, if enabled) goes high and causes the DAC to apply a current equal to one-half of full-scale to the input network, where it is compared with the current developed by the input voltage. If the input is less, the comparator output causes the MSB latch to go low at the 2nd clock pulse plus 200ns; if the input is greater, the MSB stays high, retaining the DAC output at one-half full scale. In either case, the decision initiates the trial of the second bit ($\frac{1}{4}$ full scale); it is compared and accepted (input $> \frac{1}{4}$ or $> \frac{3}{4}$) or rejected (input $< \frac{1}{4}$ or $< \frac{3}{4}$). The comparison proceeds until the LSB has been tried and accepted or rejected. The outputs DB9 through DB0, if all bits are enabled, will indicate a valid binary representation of the magnitude of the analog input, relative to the reference. This result will remain latched until another conversion is initiated.

From the timing diagram, it can be seen that when convert start (STRT) goes high, DB9 is set while DB0 through DB8 are reset. Two-clock-pulses-plus-200ns after the STRT pulse returns to *low* the MSB (DB9) decision is made. Each succeeding trial and decision is made at $T_{\text{clk}} + 200\text{ns}$ (a fixed delay time designed into the AD7570 to ensure that data from the comparator is available at the "data" input of the output latch before clocking the latch). The output data lines (DB0 through DB9) are buffered from the output data latches by three-state drivers (similar to transmission gates in series with the outputs). The transmis-

sion gates are controlled by HBEN (High Byte ENable), which controls DB9 and DB8, the two most-significant bits, and LBEN (Low Byte ENable), which controls DB7 through DB0, the 8 least-significant bits.

The time relationship of the other signals is shown in Figure 29; their meaning and functions are explained in the table.

NOTES ON LOGIC FUNCTIONS

Inputs

- Convert Start (STRT -pin 25): When STRT goes *high*, the MSB data latch goes *high*, all other bits go *low*. Conversion begins when STRT goes *low* (at least 500ns later). If STRT is re-initiated *during* conversion, the conversion sequence starts over.
- High Byte Enable (HBEN-20): When HBEN is *low*, output lines for data bits 9 and 8 (MSB and 2nd bit) float. When HBEN is *high*, digital data from the latches appears on the data lines.
- Low Byte Enable (LBEN-21): Same function as HBEN, bits 0 (LSB) -7.
- Busy Enable (BSEN-27): When *high*, requests status of conversion (see "Busy" under Output functions).
- Short Cycle, 8 Bits ($\overline{SC8}$ -26): When *low*, conversion stops after 8 bits (essential for J); when *high*, conversion runs for 10 bits.
- Clock (CLK-24): External clock (TTL/DTL or CMOS) may be applied here. For internal clock, connect RC as shown in Figure 28 ($f \cong 2.5/RC$); clock begins with STRT, ceases at end of conversion.
- V_{DD} (VDD-1): Principal supply voltage, nominally +15V
- V_{CC} (VCC-22): Compatible logic supply; +15V: CMOS, +5V: DTL/TTL

Outputs

- Busy (\overline{BUSY} -pin 28): Indicates conversion status. Floats when BSEN-27 is *low*. When interrogated (BSEN *high*): goes high when conversion complete, stays low while conversion in process.
- Serial Output (SRO-8): Indicates state of each decision (non-return-to-zero) as conversion proceeds. Must be used with SYNC-9 for correct interpretation of data. Floats when no conversion.
- Serial Synchronization (SYNC-pin 9): Provides 10 positive edges when SRO data valid. Floats when no conversion.

APPLICATIONS

The AD7570 has many uses in standard 10-bit conversion applications. Of especial interest for microprocessor applications are the tri-state output logic and "byte-size" enabling logic. Typical applications with microprocessors are similar to those suggested for the AD7550 in Chapter I-4.

However, the AD7570's analog flexibility, achieved through a design that permits the use of external reference and comparator function, makes possible an interesting variety of applications; as examples, we will consider some resistance-measurement functions.¹⁰

Resistance Deviation

Figure 30 shows a basic configuration in which the AD7570 is used to measure the deviation of an unknown resistance from a standard and convert it to offset binary. The measurement accuracy is independent of the reference-voltage accuracy, since the measurement is performed ratiometrically.

A standard resistance, which is twice the nominal value of the unknown, is the input resistor of an inverter, and the unknown is connected as the feedback resistor. The resistance of the unknown can be expressed as $R_S (1 + \alpha)$, where α is the fractional (\pm) deviation from

¹⁰ Whitmore, J. "Resistance-Ratio-to-Digital Conversion," *Analog Dialogue* 9-3, 1975.

the nominal resistance, R_S . The output of the inverter is

$$E_1 = -\frac{R_X}{2R_S} V_{REF} = -\frac{V_{REF}}{2} (1 + \alpha) \quad (2)$$

The digital output of the A/D converter will be a fractional binary number between 0 and $(1 - 2^{-10})$ of full-scale, representing the ratio,

$$D = \frac{1}{2}(1 + \alpha) = \frac{1}{2} + \frac{1}{2}\alpha \quad (3)$$

If $\alpha = 0$, the digital output number will be 10000 00000 = $\frac{1}{2}$; if $\alpha = +\frac{1}{2}$, the digital output number will be 11000 00000 = $\frac{3}{4}$; and if $\alpha = -\frac{1}{2}$, the digital output number will be 01000 00000. It is readily seen that these values correspond to an offset-binary code that reads α directly as a bipolar number. If the MSB is complemented, the output reading will be in 2's complement coding – for $\alpha = 0, \frac{1}{2}, -\frac{1}{2}$, the codes are 00000 00000, 01000 00000, and 11000 00000, irrespective of the value of V_{REF} .

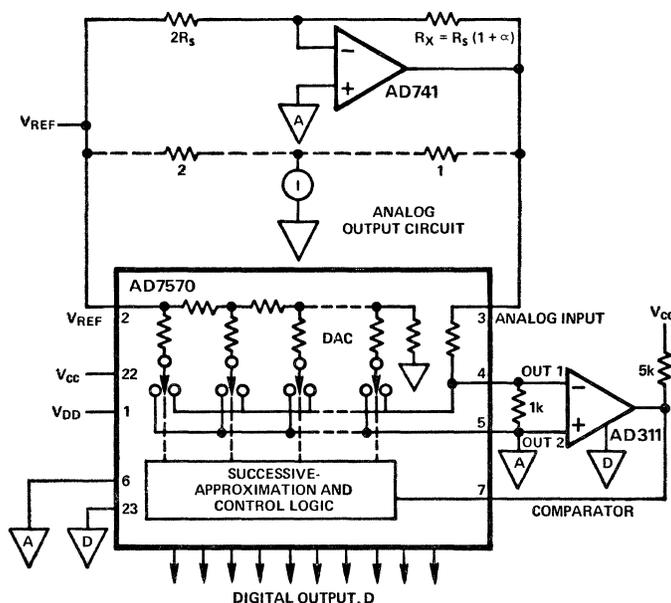


Figure 30. Resistance deviation measurement with binary output, using AD7570 A/D converter. Digital and "housekeeping" circuitry omitted for clarity.

Analog readout may also be provided in the conventional way, by the use of a precision resistance half-bridge, shown in dashed lines. The "null-meter" may be replaced by an op amp for amplification of the null signal. For digital readout with greatly-increased sensitivity, a converter may be connected in the standard bipolar-conversion configuration, to read this amplified error directly with high sensitivity.

Direct Resistance Measurement¹¹

Figure 31 shows a basic configuration in which the analog output of the D/A converter (in the successive-approximations AD7570) is converted to voltage proportional to the digital number, $-DV_{REF}$. This voltage is applied as the A/D converter input. It and the reference voltage are applied to R_X and R_S in series. The comparator acts like an op amp; that is, through the successive-approximation process, it forces the digital number, D , to be whatever value will bring the summing-point voltage, V_S , to within 1 least-significant bit of ground. Thus, at balance, with $V_S \cong 0$,

$$\frac{DV_{REF}}{R_X} = \frac{V_{REF}}{R_S} \quad (4)$$

¹¹See Also, "Simple A/D Converter Circuit Measures Resistance Digitally," by J. Whitmore, *Electronics*, Oct. 2, 1975.

and

$$D = \frac{R_X}{R_S} \quad (5)$$

irrespective of V_{REF} . This scheme can be used to measure any value of R_X less than R_S to within 1LSB of 10 bits, or 1 part in 1024 of R_S , i.e., if $R_S = 10k\Omega$, R_X may be any value from 10Ω to $9,990\Omega$, measured with a resolution of 10Ω . The voltage, $-DV_{REF}$, may be used as an analog output.

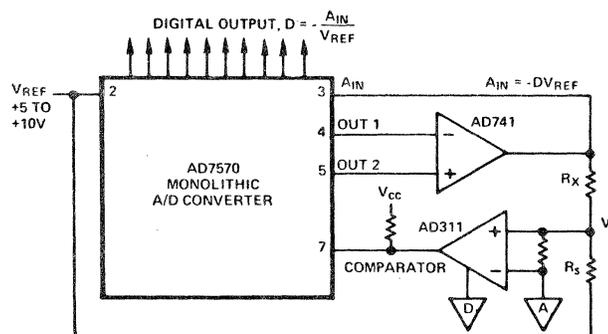


Figure 31. Direct resistance measurement. Digital output is equal to the ratio of R_X to R_S , independently of V_{REF} .

AD7550 – 13-BIT CMOS μ P-COMPATIBLE A/D CONVERTER¹²

The AD7550 is a 13-Bit A/D Converter on a single 3 x 3.2mm (118 x 125 mil) chip, enclosed in a 40-pin dual in-line package (Figure 32). It utilizes a “Quad-Slope” integration technique†, which provides both autozeroing and low sensitivity to component error, supply variations, and temperature changes. It accepts analog inputs of either polarity; the output is available as either a train of pulses for external counting, or as a parallel 2’s-complement word, divided into 5- and 8-bit bytes, and buffered by 3-state logic especially suited for microprocessor-controlled bus-oriented systems. The AD7550 interfaces directly with either TTL or CMOS logic.

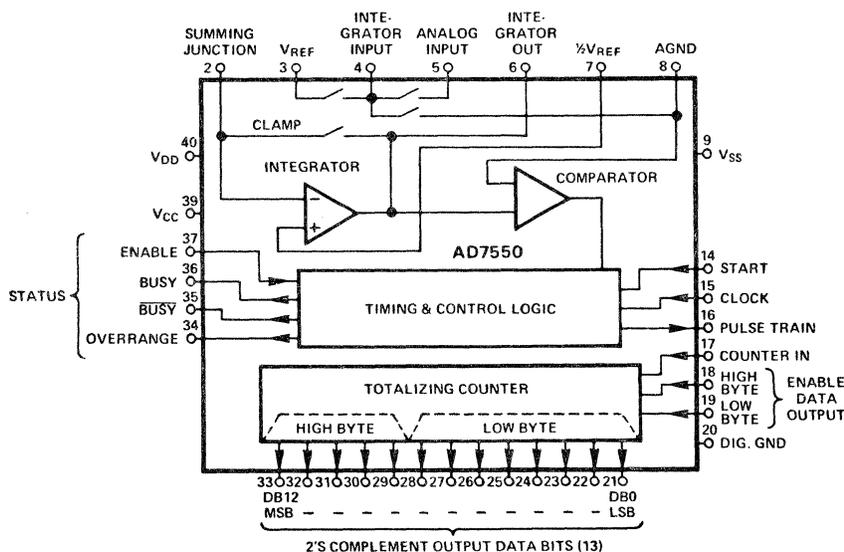


Figure 32. Block diagram of the AD7550 A/D converter.

Requiring typically only 8mW total power ($V_{DD} = 12V$, $V_{SS} = -5V$ to $-12V$, and $V_{CC} = 5V$ up to V_{DD}), and a single external positive reference, the AD7550 contains its own comparator, integrating amplifier, clock, control-, counting-, and buffer logic, and analog switches. Since

¹² Ritmanich, W., Langley, D., and Wold, I., “13-Bit Monolithic CMOS A/D Converter,” *Analog Dialogue* 10-1, 1976.

†U.S. Patent 3,872,466.

the reference is applied externally, the AD7550 may be used for ratiometric conversion. The internal clock may be overridden by an external clock for applications in which an external clock is desirable. The only passive external components normally required are a resistive divider-pair for the reference and a resistor-capacitor pair for the integrator (Figure 4).

Because of the integrating technique used, the digital output is monotonic, with no missing codes. The AD7550 will accurately digitize signals from up to slightly less than one-half the maximum reference down to levels limited only by the internal FET-input amplifier's ability to accurately integrate small microvolt-level signals without errors due to noise. Because the Quad-Slope integration technique accurately adjusts for offsets over the temperature range, the zero-drift and gain-temperature coefficients are less than 1ppm/°C maximum, at typical conversion speeds of 40Hz, with $\pm\frac{1}{2}$ LSB differential nonlinearity.

MICROPROCESSOR COMPATIBILITY

The AD7550 was specifically designed to be easy to use in data-bus systems, where its 3-state outputs are under external control. In this respect, the timing-sequencing and data-bus connections are compatible with those of the AD7570 and the AD7522.

- The positive-true parallel data outputs (bits 0–12), the overrange indication, and the conversion status lines (BUSY, $\overline{\text{BUSY}}$) are 3-state and are isolated from the common data bus until appropriate interrogation signals are received (Data ready? High byte? Low byte?)
- The five most-significant bits (including the sign bit), the 8 least-significant bits, and the three status bits can be interrogated in separate bytes; all 13 bits can be furnished on an 8-bit common data-bus in 2 bytes.
- The serial-output pulse stream is brought out on a separate pin with regular (TTL or CMOS) logic levels; this permits the data to be manipulated before being clocked into the output buffers. The pulse train, C_{OUT} , is activated after the completion of the measurement cycle and has a number of counts:

$$C_{\text{OUT}} = 4096 + 8704 \frac{A_{\text{IN}}}{V_{\text{REF1}}} \quad (6)$$

- If the control inputs are connected to the appropriate logic levels, the AD7550 will work as a conventional 13-bit parallel-binary A/D converter.

APPLICATIONS

The AD7550's *forte* lies in applications for which accuracy and lack of discontinuities (such as missed codes), especially over wide temperature ranges, are vastly more important than speed of conversion. The self-contained nature of the AD7550, its low power consumption, and its insensitivity to temperature and supply voltage make it ideal for use in compact, battery-powered precision instrumentation, for example, in seismic or geological exploration. On the other hand, its special control features allow it to be readily employed in microprocessor-controlled data-acquisition systems where 13-bit accuracy, flexible polarity, and a noise-averaging capability are necessary and high speed isn't.

Panel-meter and digital-voltmeter applications, especially in conjunction with a requirement for binary data for system use, and where high accuracy at elevated temperatures is necessary, are also pregnant possibilities. The count-out/count-in feature permits the pulse count to be manipulated separately (for auxiliary BCD displays), or prior to being counted in the tri-state-buffered counter (for example, by the use of binary rate-multipliers).

Figure 4 shows the basic circuit connection for binary operation. With all the data-output command inputs held high, as shown, parallel data will be present at the outputs. By selectively exercising the various command inputs — as discussed in Chapter I-4, Figs. 12 and 13 — HBEN (High Byte ENable: 5 most-significant bits), LBEN (low Byte ENable: 8 least-significant bits), and STEN (STatus ENable: OVer RanGe, BUSY, $\overline{\text{BUSY}}$), the desired data can be made available on an 8-bit data bus. The internal clock can be employed simply by replacing the 1MHz clock-input lead by a capacitor from the CLoCK terminal to ground.

Similarly, repetitive auto-start can be gained by connecting a capacitor from the STaRT terminal to ground.

3½-DIGIT DPM (0 TO +2V FULL SCALE)

Figure 33 shows a simple circuit to provide 3½-digit readout for positive input voltages. The number of output pulses is divided by 2, and the reference is scaled so that 1999 of the 2047 output pulses clock a National MM74C928 counterlatch-display through a 0 to +1.999V range.

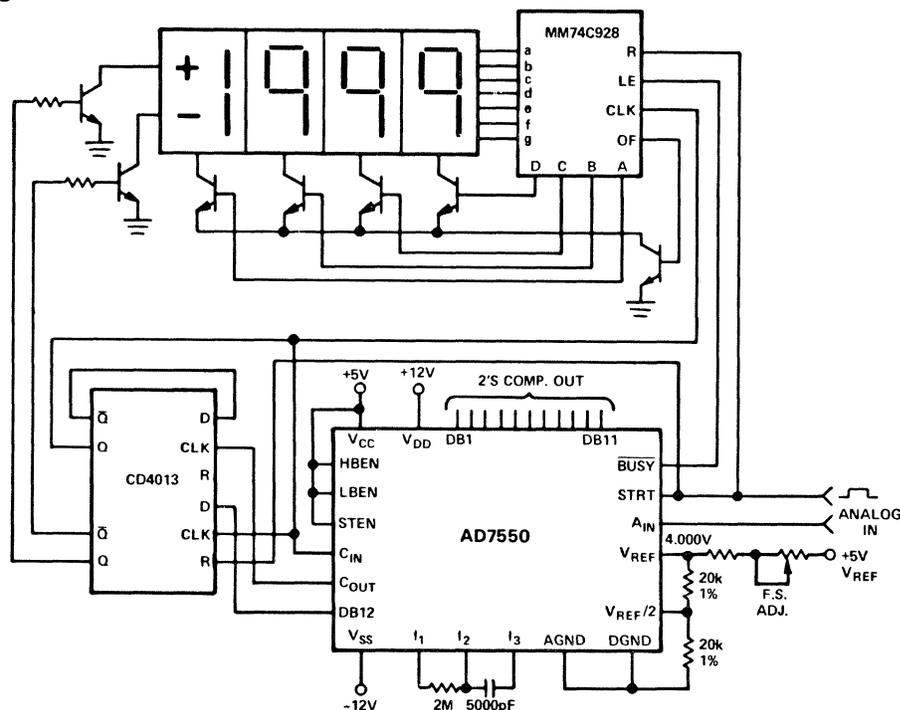


Figure 33. 3½-digit display application.

Conversion begins when the STaRT command is initiated. When DB12 goes low, indicating a positive input, the MM74C928 starts its count, corresponding to the analog input voltage. After the last C_{OUT} pulse, $\overline{\text{BUSY}}$ goes high and latches the display. The Carry output of the MM74C928 indicates overrange by toggling the CD4013 to blank the display for inputs $\geq 2.000\text{V}$.

HOW THE QUAD-SLOPE CONVERTER WORKS

The quad-slope converter is an integrator-counter converter, related to the conventional dual-slope converter. However, it includes two additional integration phases for virtual cancellation of offset- and scale-factor errors by digital subtraction. Its operation can be seen in Figure 34.

The integrator has four modes of connection, determined by internally-controlled CMOS switch settings: Clamped (when no conversion is in process), Grounded input, Reference input, and Analog (signal) input. The positive input of the integrating amplifier is continuously connected to $V_{\text{REF}}/2$. When a conversion is initiated (phase "0"), V_{REF} is applied to the integrator input, providing a net positive voltage, $V_{\text{REF}} - V_{\text{REF}}/2$, across the integrator's input resistor, resulting in a negative-going ramp at the output. When the output is equal to the comparator trip-voltage, Phase 1 is initiated.

Phase 1. The integrator input is connected to Analog Ground. Since the integrating resistor has a net negative voltage across it, equal to $-V_{\text{REF}}/2$, plus any error, the output increases positively at a proportional rate. At the beginning of Phase 1, a counter starts counting clock pulses. When it has counted a number of pulses representing an interval, $T/2$, Phase 2 is initiated; the counter continues to count.

Phase 2. The integrator input is connected to the Reference. Since the voltage across the integrating resistor is $+V_{\text{REF}}/2$, plus any error, the output ramps down at a proportional

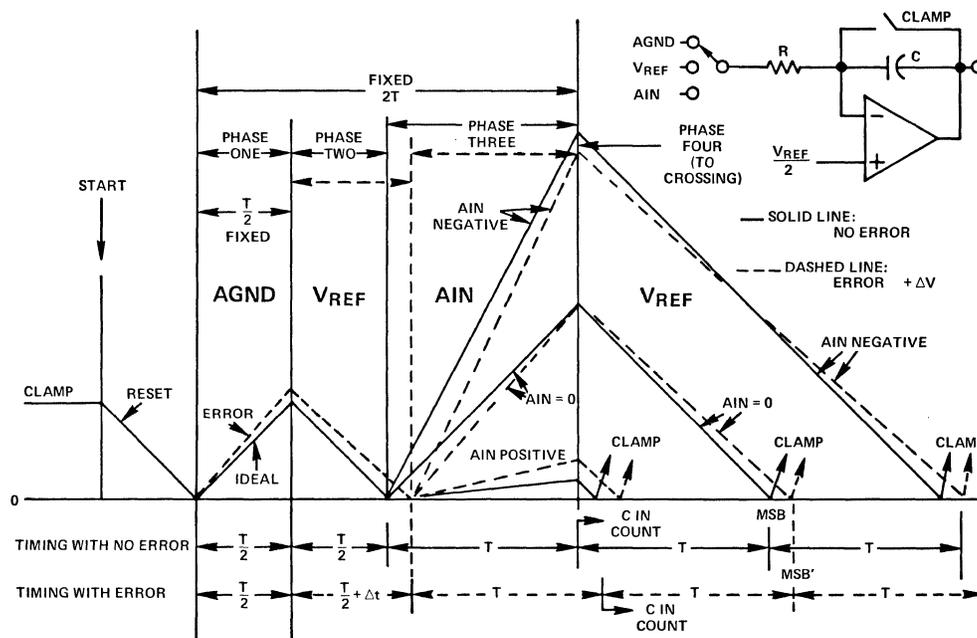


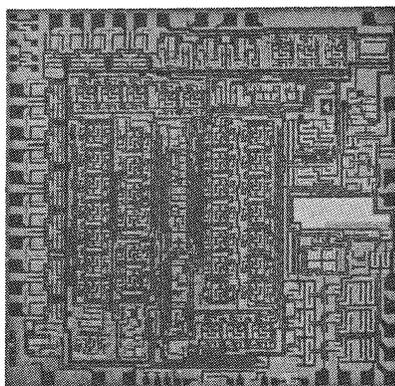
Figure 34. Illustration of quad-slope principle: integrator output waveforms for positive, negative, and zero input – with and without error.

rate. When the output reaches the comparator trip voltage, Phase 3 is initiated. If there were no error, the time for Phase 2 would be equal to $T/2$, the same as for Phase 1. Any error will increase or decrease the time to the trip point by an amount Δt . Note that the trip point is approached with the same slope and from the same direction as at the end of Phase 0 (and also the end of Phase 4), hence any comparator hysteresis errors and differential propagation delays are avoided.

Phase 3. The integrator input is connected to the Analog signal, which is positive or negative, and less than $V_{REF}/2$ in magnitude. The net input to the integrator will always be negative and equal to $A_{IN} - V_{REF}/2$, plus any error. The output of the integrator will ramp upwards with a proportional slope. For large positive inputs, the output slope will be small; for large negative inputs, the output slope will be steep; and for zero input, the slope will be the same as in Phase 1. Phase 3 is terminated when the counter that started at the beginning of Phase 1 reaches a count corresponding to $2T$.

Because Phases 1, 2, and 3 occupy a total period $2T$, Phase 3 is lengthened or shortened by Δt , the same amount by which Phase 2 was shortened or lengthened. At the *beginning* of Phase 3, a second counter is starting, counting *down* from zero*; note that, with zero error, it starts at T exactly; but with an error, it starts at $T \pm \Delta t$.

Phase 4. The integrator input is again connected to the Reference, and it ramps down at the rate $V_{REF}/2$, plus any error. Phase 4 ends when the integrator output reaches the trip point,



*The implementation discussed here is simplified for clarity.

after which the integrator is clamped and the second counter is stopped. Conversion is now complete, and the counter output is a 2's complement representation of the analog input.

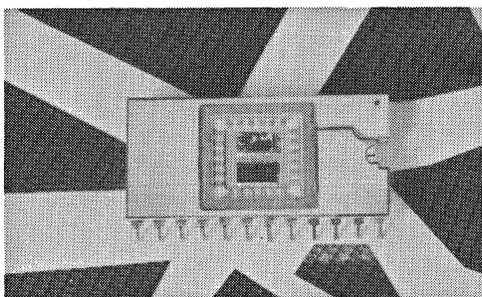
Discussion. The data sheet describes the actual workings of the circuit in some detail and includes a derivation of the error equation, which indicates square-law weighting, making small errors much smaller. Here we will rely somewhat more on graphics and intuition to show that it actually works. In Figure 34, it can be seen that the time from the MSB crossing, corresponding to zero input, to the time of occurrence of the crossing corresponding to a positive or a negative input, is proportional to that input. The effect of an error is simply to shift *all* crossings by an equal amount of time, Δt .

If the counter's capacity is $2T$, and if it counts down from all zero's at the beginning of Phase 3, then at the largest positive number, it will read 0 1111 1111 1111 (and will stop there if a crossing occurs), at zero it will read 0 0000 0000 0000, and at the largest negative number, it will read 1 0000 0000 0000, a range which will be recognized as belonging to a 2's-complement code.

In actual practice, in order to avoid negative integration and allow sufficient time after Phase 4 begins for offset correction and overrange indication, a somewhat different counting scheme is used, in association with an input full-scale range of $V_{REF}/2.125$, instead of $V_{REF}/2$.

THE AD562—12-BIT DIGITAL-TO-ANALOG CONVERTER¹³

The AD562 is a 12-bit integrated-circuit digital-to-analog converter in a hermetically-sealed 24-lead ceramic dual in-line package; it is available in both binary and BCD versions. Monotonic 12-bit resolution is guaranteed over the operating temperature range, with less than $\frac{1}{2}$ LSB ($\frac{1}{4}$ LSB for AD562S) *max* total error at $+25^{\circ}\text{C}$, and $3\text{ppm}/^{\circ}\text{C}$ *max* gain-temperature coefficient. The circuit assembly consists of two interconnected chips: (1) a monolithic bipolar transistor chip, which contains the 12 precision current switches, and (2) a compatible Si-Cr thin-film resistor chip, with the bit-weighting and range-setting resistors. All scale factors are accurately calibrated by computer-controlled automatic laser-trimming of the resistors while the device is operating — the key to its outstanding resolution and calibration accuracy, as well as its low price.



The AD562 (Figure 5) accepts an external analog reference voltage (0 to +10V) and supplies a binary-weighted output current proportional to the product of the 12-bit digital input-code and the value of the reference voltage, which can be either fixed or variable. When the reference is fixed, the AD562 functions as a normal DAC. When V_R is a variable unipolar (0 to +10V) voltage, the device is a 2-quadrant multiplying DAC; the digital input code can be either unipolar (binary or BCD) or bipolar (offset binary). The AD563 D/A converter, which contains an AD562 (scaled for 2.5V reference) and a 2.5V reference, was designed for applications calling for a 12-bit fixed-reference DAC in a single IC Package.

Nominal full-scale output current (unipolar mode) is -2mA. Internally-trimmed gain-, voltage-range-, and bipolar-offset-resistors are incorporated, to provide precise voltage outputs via an external op amp. Since all voltage scale-factors rely on resistance

¹³Craven, R. and Harris, S., "12-Bit Integrated-Circuit D/A Converter," *Analog Dialogue* 8-2, 1974.

ratios, their temperature coefficients are determined by tracking TCR's (about 1ppm/°C) rather than absolute TCR's (about -30ppm/°C). With $V_R = +10V$, the following voltage ranges can be pin-programmed (see Figure 36): 0V to +5V, -2.5V to +2.5V, 0V to +10V, -5V to +5V, -10V to +10V. The AD562's current output, when used with the internal ranging resistors, allows the device to be used as the D/A weighting element in both voltage-output DAC's and voltage-input ADC's, with very low voltage-gain T.C., because these resistors track the other thin-film network resistors to better than $\pm 2\text{ppm}/^\circ\text{C}$.

Logic Inputs. The logic relationship is "positive-true": voltage above threshold ("1") turns a bit *on*; voltage below threshold ("0") turns it *off*. Logic drive currents are only $-100\ \mu\text{A}$ *max* at "0" and $+100\text{nA}$ *max* at "1", values compatible with both CMOS and TTL logic. Pin 2 sets the internal logic threshold for the digital inputs, bits 1–12. When it is open-circuited, with $V_{CC} = +5V$, the threshold is approximately +1.4V, and the device is TTL-compatible. For CMOS, pin 2 is externally connected to pin 1; the internal logic threshold is thereby set at $\sim V_{CC}/2$, and the device is then fully compatible with both low- and high- voltage CMOS, over the range $+4.75V \leq V_{CC} \leq +15.8V$.

Coding. The various voltage ranges that can be pin-programmed are shown in Figure 35. For bipolar ranges, a fixed current is subtracted from the output current to

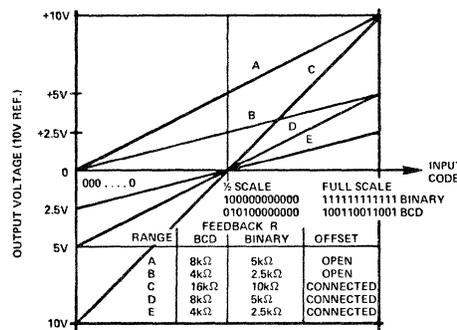


Figure 35. Voltage vs. digital input code for various connections of span and bipolar-offset resistors (10V reference).

offset it by half-scale, by the connection of the other end of the bipolar offset resistor (through an external trim pot) to V_R (Figure 36). Analog voltage zero occurs at digital code 1000 0000 0000 (2048/4096 of F.S. span) for binary models, and at 0101 0000 0000 (500/1000 F.S.) for BCD (binary-coded decimal) models.

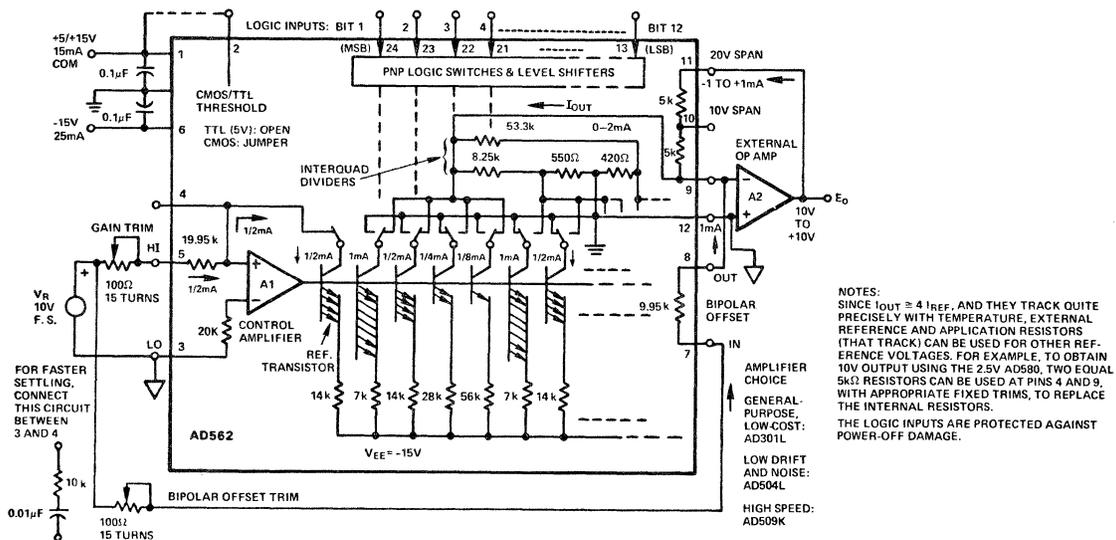


Figure 36. Functional schematic of the AD562.

The AD562 current output is the weighted sum of the outputs of three similar groups of binary-scaled quad current-generators, controlled by V_R . The logic inputs steer these currents through non-saturating bipolar-transistor current switches to either ground or the respective quad output bus. Output currents from the 2nd and 3rd quads are attenuated (in effect) by 16:1 and 256:1 (binary; 10:1 and 100:1 for BCD), and summed with the unattenuated output of the first quad. The output current is thus the sum of 12 individually-switched currents having a binary relationship. Figure 36 shows the overall scheme. Figure 37 shows the simplified details of the control amplifier, constant-current transistors, and switching-cell interconnections.

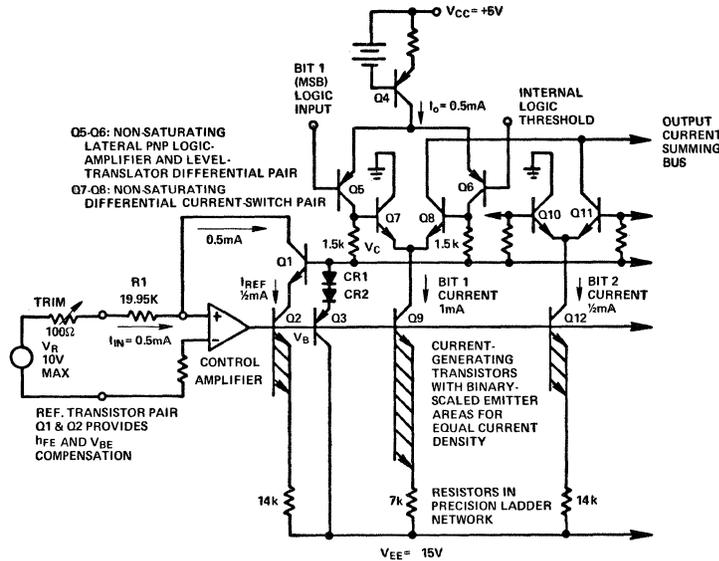


Figure 37. Control amplifier, current generators, and bit-switching cell structure.

The current-generating transistors (Q9, Q12, etc.) of each quad group have emitter areas in the ratio 8:4:2:1. The ladder-network resistances between the emitters of Q9, Q12, etc. and the -15V supply are in the ratio 1:2:4:8 (bits 1, 2, 3, 4 in the first quad). With equal voltages applied to the resistors, the emitter currents of Q9, Q12, etc., are therefore in a binary ratio. Because of their weighted emitter area, these transistors operate at equal emitter-current densities and therefore have nearly-equal V_{BE} 's and h_{FE} 's. The control amplifier (A1) drives the bases of the constant-current transistors and also a reference-transistor pair (Q2–Q1), which has h_{FE} and V_{BE} matched to those of the constant-current (Q9, Q12, etc.) and bit-switching (Q8, Q11, etc.) transistors.

V_R is applied to the externally-trimmed gain resistor R1 to set a reference current, $I_R = 10V/20k\Omega = 0.5mA$ F.S.). Amplifier A1 establishes the appropriate base voltage to force Q1 collector current equal to I_R . Variations in h_{FE} , V_{BE} , or supply voltage with time and/or temperature are sensed in the reference-transistor pair. The control amplifier then adjusts V_{BE} to hold Q1 collector current (and therefore the bit currents) constant in the presence of these variations. The use of Q1, Q2, and A1 reduces the net gain T.C. to a function of the differential h_{FE} and V_{BE} between the monolithically matched reference- and bit-switching-pairs. This close match results in an overall transistor-contribution of $<1ppm/^\circ C$ to the gain T.C.

Output current (for example, Bit 1) is switched by steering Q9's collector current either to ground through Q7, or to the output through Q8. With Bit 1 *high*, Q5 is turned off, and I_O is steered through Q6; Q8 is turned on, Q7 is turned off, and Q9 collector current flows through the output. With Bit 1 *low*, Q6 is turned off, and I_O is steered through Q5; Q7 is on, Q8 is off, and the Q9 collector current flows to ground. This fully-differential switching takes place rapidly, since there is no change in steady-state voltage at the emitters of Q7–Q8, with a speed that is *nearly independent of the current level being switched*. (Switching

speeds for most commercially-available DAC's vary significantly as a function of current level.) This feature is particularly useful in multiplier applications, which require fast switching at reduced (as well as full-scale) current levels, as a function of V_R .

The excellent V_{BE} match (to about 1mV) of Q2, Q9, Q12, etc., permits accurate multiplication (fast or slow) at reduced current levels (V_{BE} mismatch among the output-current switch transistors, Q8, Q11, etc., which are cascode-connected, does not affect bit-weighting accuracy).

Since the collector voltage of Q2, Q9, Q12, etc., does not change during bit switching, there is no differential power change as various bit combinations are switched. Moreover, the four most-significant current-setting transistors (Q9, Q12, Q15, Q18) are located on the axis of symmetry between Q7–Q8, Q10–Q11, etc., virtually freeing the device from nonlinearity and thermal-transient errors attributable to differential heating. Typical AD562 nonlinearity is, in fact, less than 30ppm F.S.

Q3 and diodes CR1 and CR2 form a bootstrapped bias source which causes the voltage V_C (very nearly equal to the collector voltages of Q9, Q12, etc.) to track the base voltage V_B . The collector-base voltage of Q9, Q12, etc., is thus maintained at approximately $3V_{BE}$, irrespective of supply- or reference-voltage variations (which are impressed across the switch transistors instead). Bootstrapping prevents h_{RE} effects from introducing errors into the bit currents and contributes to the AD562's excellent supply-voltage rejection and multiplier performance.

APPLICATIONS

Multiplication. As noted above, the AD562 can be used as a multiplying DAC. The analog input (V_R) must be unipolar (0 to +10V); the digital coding may be either unipolar (single quadrant) or bipolar (2 quadrants). When V_R is +1V (10%F.S.), worst-case error is only about 0.05% of the (reduced) full-scale output. Settling time for a 10V-full-scale V_R step is $5\mu s$ to 0.01%, while the slewing rate is $1mA/\mu s$ (or $5V/\mu s$ with a suitable output amplifier providing a 0–10V range), with all bits *on*. Feedthrough of a full-scale (10Vp-p) sinewave, with all bits *off*, is 0.0125%F.S. at 2kHz, increasing at 20dB/decade at higher frequency.

12-Bit Successive-Approximations A/D Converter (Figure 38). The AD562 is shown here as the D/A weighing element in a 12-bit ADC, for conversion rates up to 40kHz. The digital output-equivalent of the analog input is formed by weighing the programmed DAC-output, one bit at a time (MSB first, LSB last), and accepting or rejecting each bit, depending upon

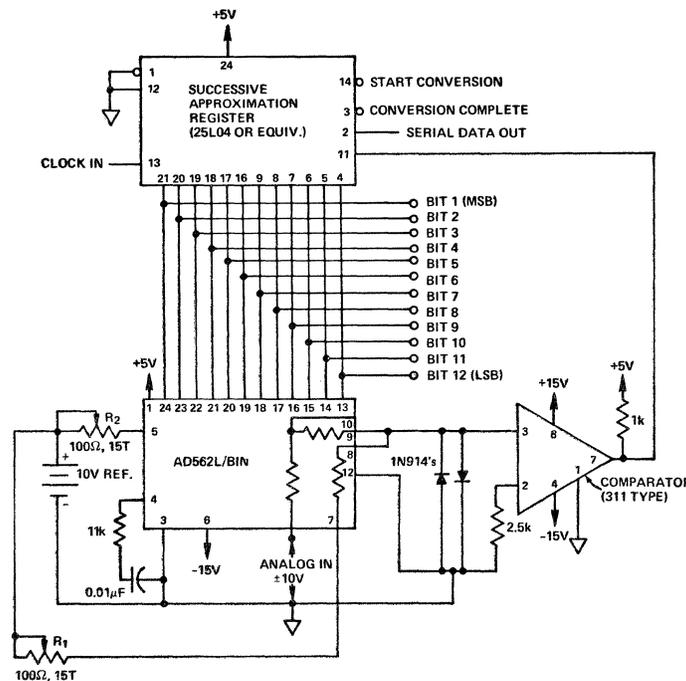


Figure 38. 12-bit successive approximation A/D converter.

the comparator state following each bit-trial. The analog input voltage is applied to the appropriate AD562 span resistor, and the current-output terminal (summing-point) voltage is compared against "ground." The AD562's output voltage is diode-clamped to keep the out-of-balance error voltage within the device's compliance-voltage limits. The AD562's multiplying capability permits the reference voltage to be varied for ratiometric conversion. It should be noted that the AD562 is at the heart of the AD572 A/D converter.

AD561 HIGH-ACCURACY 10-BIT DAC WITH BUILT-IN REFERENCE¹⁴

The AD561 is a 10-bit single-chip digital-to-analog converter in a 16-pin ceramic DIP; it contains its own high-stability voltage reference. In response to a positive-true TTL or CMOS parallel digital input, it produces a high-compliance (-2V to +10V) 0 to 2mA current output. Completely self-contained are the reference, R-2R thin-film-on-silicon ladder network, current-steering switches, and the application resistors needed for generating high-precision $\pm 5V$ and 0 to +10V outputs, when used with an output buffer amplifier. The AD561 has the best guaranteed accuracy at 25°C ($\frac{1}{4}LSB$ max—K,T) and the tightest tempco (30ppm/°C max) among known 10-bit IC D/A converters, and it is the *only* such IC to be guaranteed monotonic over the operating temperature range (0°C to 70°C—J,K; -55°C to +125°C—S,T). As a further bonus, full-scale settling time to within $\frac{1}{2}LSB$ is 250ns.

As of this writing, not only is the AD561 the most-accurate and stable in its class — it is also one of the *least-expensive* 10-bit D/A converters available!

PROCESS LIMITATIONS

Until the AD561 became available, an appropriate IC with the right combination of accuracy and cost had not been available to system designers who needed true 10-bit (0.1%) device accuracy.* The various options theretofore available — none of them attractive — ran the gamut from the compromises inherent in untrimmed, low-priced 10-bit converters to adequate (but expensive) 10-bit hybrids to overdesign by the use of 12-bit converters (to be sure of adequate 10-bit performance at the extremes of temperature). Semiconductor manufacturers had consistently found that it was well-nigh impossible to obtain substantial yields of IC's containing a resistive ladder network, with matching and tracking properties adequate for a 0.1% device, by the use of the photolithographic process alone (and low yield = high cost).

The key to overcoming these linearity limitations, using today's technology, is to laser-trim the resistor networks *and* the reference tempco *at the wafer stage*, a process developed as a cost-effective manufacturing tool at Analog Devices Semiconductor.¹⁵ The thin-film R-2R ladder network is trimmed by a high-resolution laser-trimming system to provide conversion linearity of the order of 0.01%. These devices, which have been trimmed at the wafer stage, are then assembled, sealed, and burned-in, after which they are graded into $\frac{1}{4}LSB$ (K & T) and $\frac{1}{2}LSB$ (J & S) categories. This system adds the benefits of high yield to the already traditionally low IC-manufacturing costs.

BURIED REFERENCE DIODE

The key to the AD561's overall gain accuracy is the stable reference. "Zener" reference diodes are easy to make on an IC chip: just use the reverse-breakdown voltage of a base-emitter junction. This technique is widely used. Unfortunately, such diodes are noisy and unstable, because the breakdown occurs at the surface of the die, where shifts of the breakdown point, caused by variations of stress produced by charged oxide impurities, especially mobile ions, can significantly affect stability. Long-term shifts of up to a few percent are not uncommon, a phenomenon hardly compatible with overall 0.1% device performance.

For the AD561, a deep-diffusion technique is used to "bury" its reference diode; the break-

¹⁴ Kress, D., "Highest-Performance 10-Bit IC DAC," *Analog Dialogue* 11-1, 1977.

*For example, in an industrial measurement and control system where transducer errors may be typically 0.5% to 1%, the AD561's performance combination may be needed to avoid the introduction of significant additional error and further degradation of system accuracy.

¹⁵ Wagner, R., "Laser-Trimming on the Wafer," *Analog Dialogue* 9-3, 1975.

down, occurring well below the surface, is characterized by considerably less noise and by long-term instability of only a few ppm/year. For the complete D/A converter, stability is typically within 50-100ppm/year. Stability of the reference with temperature is optimized by laser-trimming of the reference-compensation circuitry for near-zero overall drift. Combined with the close tracking of the metal-film (Si-Cr) resistors, this results in low initial calibration errors, high linearity, and low drift with temperature.

DESIGN

Figure 6 shows the complete (simplified) circuit of AD561. The buried-reference-diode circuitry develops -7.5V , which is scaled by an inverting amplifier, A1, to $+2.5\text{V}$. This voltage level permits the AD561 to operate well with positive supply voltages as low as 4.5V . The reference voltage produces an input current to inverting amplifier, A2; the 1mA current (I_{REF}) is duplicated by the control transistor, Q1, which enforces the necessary voltage between the base line and one end of the R-2R ladder. Since Q2 is identical to Q1, and its base-emitter circuit operates under exactly the same conditions, its collector current (the MSB) is also equal to I_{REF} . The state of the digital input determines whether the collector current is added to the output current via Q3 or is harmlessly shunted to ground via Q4 by the Craven-cell current-steering switch,¹⁶ described earlier (Figure 37).

A set of binary-weighted currents, produced via an R-2R ladder network, are stabilized and switched by familiar techniques (Chapter II-1) (with a few new wrinkles, explained on the data sheet). $5\text{k}\Omega$ resistors provide the full-range scaling†, and a $2.5\text{k}\Omega$ resistor, connected to the 2.5V reference, provides bipolar offset current.

APPLICATION FEATURES AND CIRCUITS

In Figures 39 and 40, the AD561 is shown connected for operation in the unipolar (0 to $+10\text{V}$) and bipolar ($\pm 5\text{V}$) output modes. The internal $5\text{k}\Omega$ and $2.5\text{k}\Omega$ resistors are pretrimmed and typically provide scale-factor and bipolar-offset accuracy to within 0.1% (0.5% max), with external 25Ω and 10Ω fixed resistors added in series. For higher absolute accuracy, variable resistances of 50Ω and 20Ω full-scale are used instead to calibrate the gain and bipolar offset.

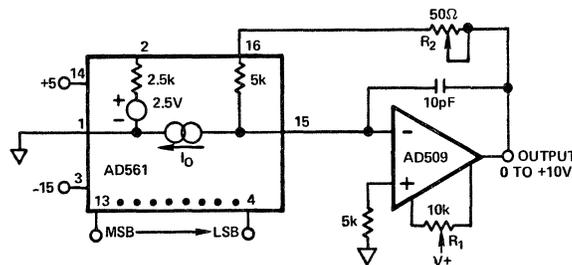


Figure 39. Connecting the AD561 for buffered 0V to $+10\text{V}$ output. The adjustment pot may be replaced by a fixed 25Ω resistor for 10mV typical output error.

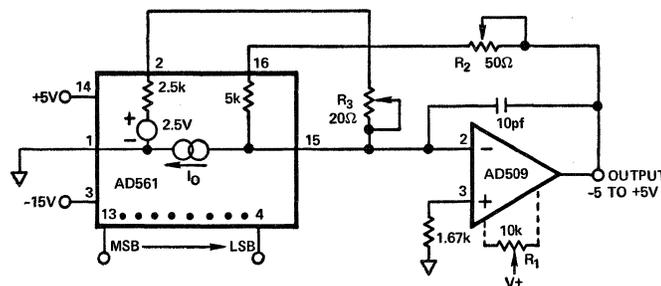


Figure 40. Connections for buffered $\pm 5\text{V}$ output. Adjustment pots may be replaced by mid-range resistances with 10mV typical error.

¹⁶ U.S. Patent 3,961,326.

†Standard output range is $\pm 5\text{V}$ or 0 to $+10\text{V}$. Also available on the chip for optional bonding are: $\pm 10\text{V}$, 0 to $+20\text{V}$; $\pm 2.5\text{V}$, 0 to $+5\text{V}$.

for all-bits-off to all-bits-on is less than 250ns; the lower-order bits settle individually in less the 200ns. When the AD561 is used with the AD509 high-speed op amp, the output can be made to settle in less than 600ns. This kind of high-speed performance is useful for constructing a fast A/D converter, such as the one shown in Figure 42.

THE AD2026 PANEL METER¹⁷

While not an IC converter, in a strict sense, the AD2026 chip design is worth discussing, for several reasons. It is the first-known use of I²L technology for a commercial conversion device (and it is still the only one that can be more-or-less freely discussed at this writing). Second, it permits the reader who is unfamiliar with I²L to gain an insight into its possibilities. Third, the underlying philosophy may be of interest.

The AD2026 is a 3-digit panel meter (DPM), powered by a single +5V supply, with 0.5" (13mm) LED display, and overall dimensions of 87 x 52 x 22mm (3.43" x 2.04" x 0.85"). Intended to supplant measurement-grade analog panel meters in new instrument designs, it provides high reliability at low cost. Achievement of these usually conflicting objectives is the culmination of a project that required innovations* in design, manufacturing, and test. Key elements include a proprietary I²L† chip that reduces total electrical parts count to 14, a single-board design that is batch-assembled and-tested, and a proprietary case that requires no tools or hardware for assembly and mounting.

Besides the design of the I²L chip (and the choice of the technology), the key factors in the cost-effective design of the AD2026 were the fundamental decisions on the features of the device – made after a thorough study of the needs of high-accuracy *analog* panel-meter users (price, display, polarity and zero, accuracy and repeatability, reliability, and size) – and the use of mass-production techniques in the fabrication of the instrument.

DESIGN

The AD2026 uses the classical dual-slope integrating A/D conversion technique. The input signal is integrated for a fixed interval of time, then a reference of opposite polarity is integrated for the time required for the integrator output to “ramp” back to its starting level. That time interval, measured by counting a train of clock pulses, is proportional to the input (and insensitive to such parameters as integrator time constant and accuracy of the clock rate).

In the AD2026, the input is offset, to permit the specified 10% negative capability (Table 1). The offset is interpreted digitally by relatively simple logic circuitry, which complements the BCD data for negative inputs and provides the minus sign in place of the “hundreds” digit. The offset input eliminates the need for two reference polarities, resulting in greatly improved linearity near zero and a saving of chip area.

INPUT	READING
>999mV	E E E
999mV	9 9 9
998mV	9 9 8
●	●
●	●
zero	0 0 0
-1mV	- 0 1
●	●
●	●
-99mV	- 9 9
<-99mV	- - -

Table 1. AD2026 output vs. input (3 decimal points selectable at connector)

¹⁷Boole, R, and Smith, L., “Revolutionary Panel Meter Uses I²L Chip,” *Analog Dialogue* 10-2, 1976.

*Patents applied for

†Integrated Injection Logic.

Conversion is initiated by pulses at 4Hz rate, obtained from a divider chain fed by an on-chip clock. The pulse enables a voltage-to-current converter, which feeds a current proportional to the input into the integrating capacitor. After the preset number of counts, the input stage is turned off, and a reference current (derived from an on-chip band-gap reference) is applied, ramping the capacitor back to the original starting value. The ramp time is measured by a second counter (on-chip), multiplexed onto a 4-bit-wide bus, and fed to the display circuit. The signal integration time is 1ms, and complete conversion requires only 2ms.

There are several advantages to short conversion times: No data latches are required, since the displays are blanked during conversion and unchanged at other times. In addition, LSI area is saved by using an essentially passive integrator. Also, the short conversion time reduces the size of integrating capacitor to manageable proportions. Finally, the display blanking during conversion means that interaction between the display and the converter is eliminated, which makes for outstanding differential linearity.

Figure 43 is a block diagram of the AD2026 circuit. Only 13 electrical components are *not* on the proprietary LSI chip: 3 LED's, 3 digit-select transistors, 3 decimal-point current-limiting resistors, 1 LED segment driver, 2 potentiometers, and the integrating capacitor.

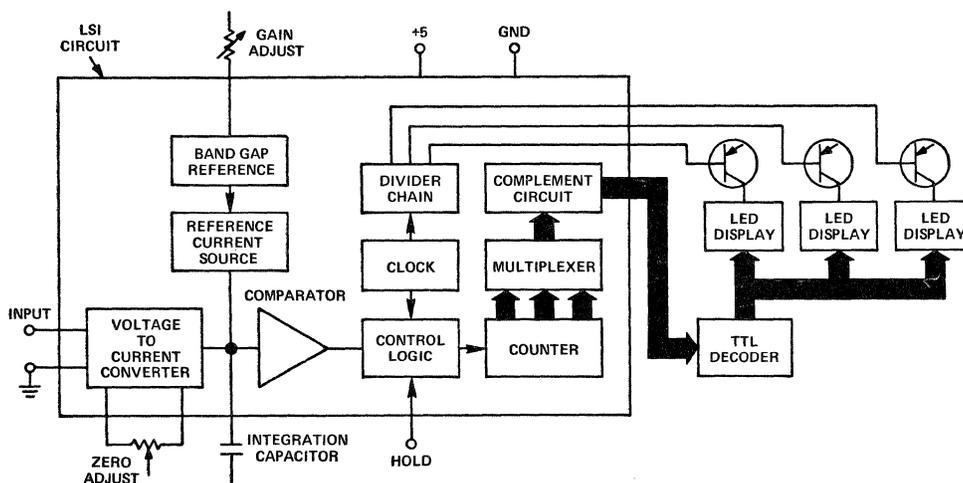


Figure 43. AD2026 block diagram.

THE I²L CHIP

The key to the performance, low cost, and reliability of the AD2026 is the large-scale-integrated (LSI) I²L chip. The current intense developmental activity towards applying I²L to applications which require combining analog and digital circuitry on a single chip testifies to its appropriateness as a technology to apply to DPM's.

Some time ago, ADI recognized I²L's potential for dramatically reducing DPM parts count and cost, while simultaneously further improving reliability. A brief discussion of I²L follows, and an extended discussion can be found in *Electronics*, "The Bipolar LSI Breakthrough", September 4 and October 2, 1975.

The only process that approaches I²L in overall economy is CMOS. Table 2 summarizes some significant differences. I²L has much higher logic density and lacks the noise and drift that CMOS tends to have in active analog circuits (though it makes for excellent switches). Inevitably, there are functions which cannot be integrated into a CMOS chip and must be provided by external components. Because I²L is free from the surface effects found in lightly-doped CMOS, the AD2026 performance is exceptionally stable and reliable. As a manufacturer of both IC's and DPM's, Analog Devices is well-qualified to synthesize DPM performance requirements with the capabilities of the I²L process into a uniquely cost-effective chip design. The AD2026 was, in fact, the first commercial application of I²L to DPM design.

ISSUE	I ² L	CMOS
Yield Factors		
A) Experience	Considerable applicable analog experience.	Considerable digital experience.
B) Major cause of limited yields	Collector to emitter shorts.	Surface contamination.
C) Density	Approximately 10mils ² per gate.	Approximately 30mils ² per gate.
Analog Functions		
A) Versatility	Excellent. Possible circuits include band gap references and power.	Poor. However, good analog switches are inherent.
B) Precision	Good.	Fair.
C) Complexity	Excellent.	Fair. Present state of the art is two or three op amps.
Digital Functions		
A) Power x delay	Less than 1pJ.	Approximately 3pJ.
B) Interface	Good. Will easily sink 10 TTL loads.	Fair. TTL compatibility is possible at the expense of chip area.

Table 2. Comparison of I²L and CMOS.

WHAT IS I²L?

MOS and bipolar are the two basic LSI semiconductor processes. MOS produces very dense – therefore low-cost – logic circuits but is capable only of crude analog devices. Before I²L, *bipolar* could offer stable high-quality devices suitable for precision analog circuits, but logic consumed much expensive chip area.

Integrated Injection Logic (I²L) now allows the design of single-chip devices containing both analog and digital functions, without calling for the compromises required in the past. I²L has a logic density that equals or exceeds that of MOS, while employing a bipolar process suitable for precision analog circuitry.

I²L eliminates the complexity of conventional bipolar logic by using inverted transistors (collectors and emitters are interchanged). Figure 44 shows a conventional transistor, with its wraparound P+ isolation region, which is needed to separate the collectors of adjacent transistors. When the transistors are inverted, the collectors are automatically isolated, and the emitters are fortuitously grounded, at the same time.

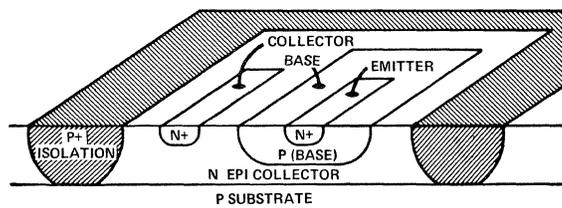


Figure 44. 3-dimensional section of conventional NPN transistor.

Since I²L logic gates can easily have multiple outputs, it is possible to use simple “wired-or logic”, a means of implementing the logical *or* operation using only one conductor (*wire*). Figure 45a shows an example of two I²L gates wire-or’d to implement the *nor* function.

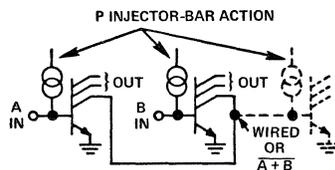


Figure 45a. I²L gates wired to implement NOR function.

A major contributor to I²L’s compactness is replacement of conventional “pullup” resistors or transistors by an injector bar. In Figure 45b, the P injector acts as a combined power-

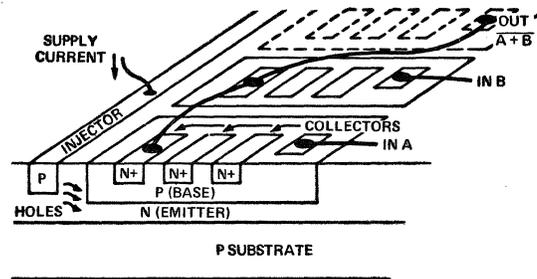


Figure 45b. Sectional view of I^2L circuit.

supply rail and current source for the I^2L gates. Holes are injected into the chip and collected by nearby base regions so as to pull-up each gate.

Analog circuitry may be placed on the same chip by using conventional transistors like that of Figure 44. Thus, I^2L can be seen to combine the possibility of high-density logic functions with precision analog circuitry.

THE AD572 – 12-BIT SUCCESSIVE APPROXIMATION A/D CONVERTER

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of $\pm 0.012\%$, gain T.C. below $15\text{ppm}/^\circ\text{C}$, typical power dissipation of 900mW , and conversion time of less than $25\mu\text{s}$. Of considerable significance in military and aerospace applications is the guaranteed performance from -55 to $+125^\circ\text{C}$ of the AD572S, and the availability of units processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to $+70^\circ\text{C}$, -25 to $+85^\circ\text{C}$, and -55 to $+125^\circ\text{C}$.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ± 2.5 , ± 5.0 , ± 10 , 0 to $+5$, or 0 to $+10$ volts. Adding flexibility and value are the $+10\text{V}$ precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is packaged in a hermetically-sealed, all-metal DIP. Welding-rather than solder sealing-eliminates any possibility of contamination from flux and solder particles. The metal construction provides excellent shielding from random electrostatic and/or electromagnetic radiation which could cause incorrect output codes. To insure a level of reliability consistent with its performance, each AD572 receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, acceleration testing, fine and gross leak testing, and operating burn-in.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25 to $+85^\circ\text{C}$, and the "S" from -55 to $+125^\circ\text{C}$.

DESIGN

The AD572 functional diagram and pin-out are shown in Figure 46. The device consists of the following monolithic bipolar transistor and thin-film-resistor circuit elements:

1. 12-bit successive-approximation register
2. 12-bit feedback DAC weighing network
3. Low-drift comparator
4. Temperature-compensated precision $+10\text{V}$ reference

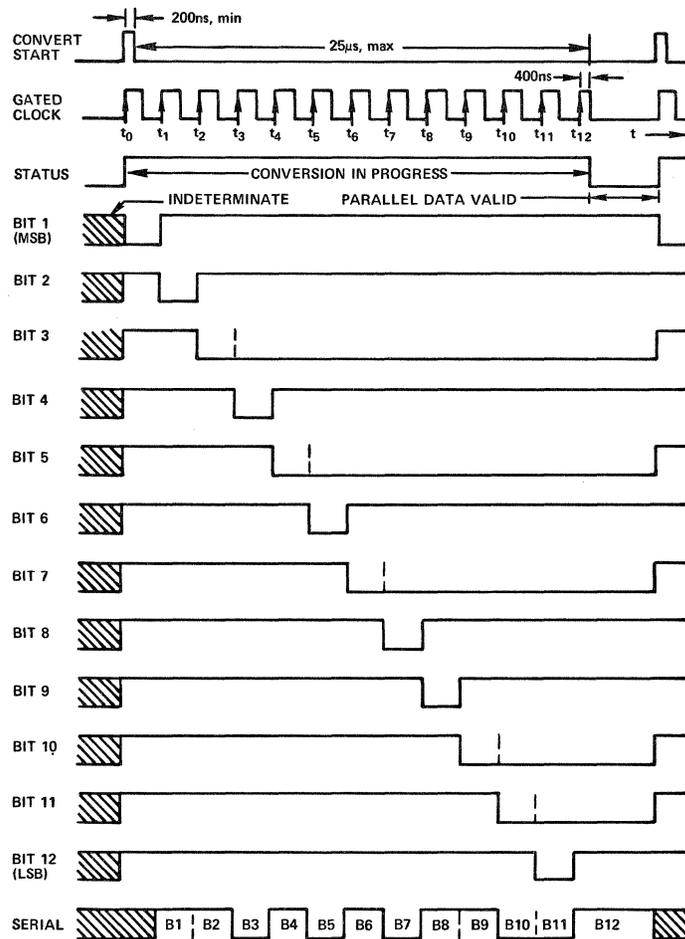


Figure 47. Timing diagram (binary code 110101011001)

to the gated clock, permitting it to run through 13 cycles. All SAR parallel-bit and STATUS flip-flops are initialized on the leading edge, and the gated clock-inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0 , B_1 is reset and B_2 - B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2 , the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12} . After a 400ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 48).

Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the logic "1" to "0" transition of the STATUS flag, permitting parallel data-transfer to be initiated by the trailing edge of the STATUS signal.

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement bipolar, depending on whether Bit 1 (pin 12) or its logical inverse BIT 1 (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 48. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 47. The first edge shifts into the register an invalid bit, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and will be in the receiving shift-register locations shown at the completion of the conversion period.

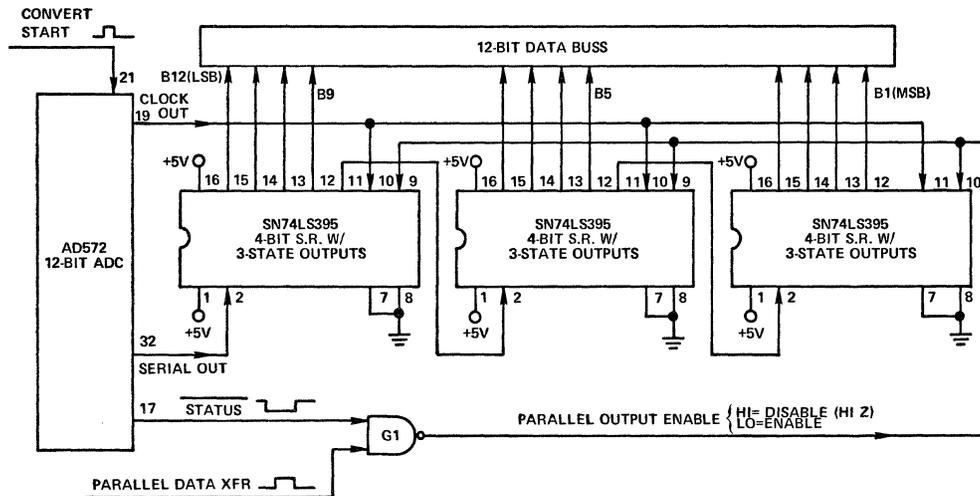


Figure 48. Serial data transfer into shift register with parallel output to data buss.

APPLICATIONS

Sample-Hold Amplifier: A sample-and-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than $\frac{1}{2}$ LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 49. The $\overline{\text{STATUS}}$ output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o \text{ S-H}}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o \text{ S-H}}$ again tracks the analog signal voltage $e_{in \text{ S-H}}$ (after the signal acquisition transient has subsided).

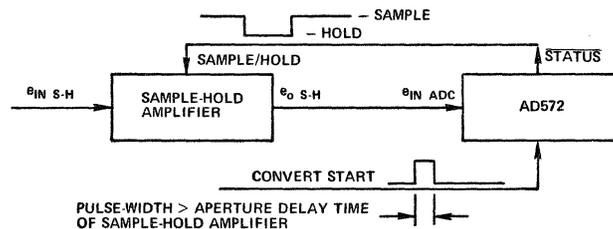
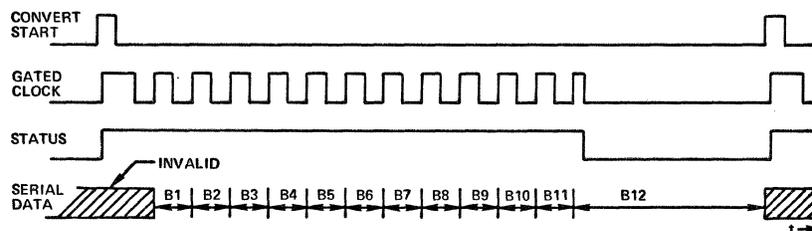
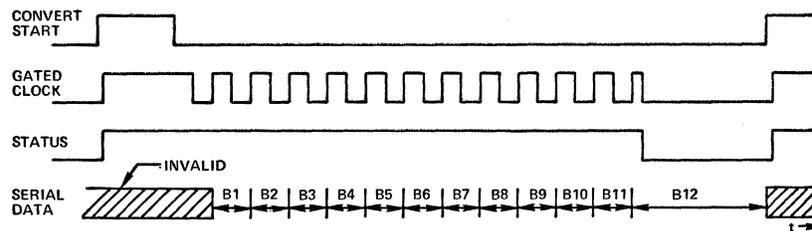


Figure 49. Sample-and-hold amplifier - AD572 interconnections.

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 49, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o \text{ S-H}}$ is in steady-state before conversion is initiated. This insures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 50.



(a) Narrow convert start pulse.



(b) Wide convert start pulse.

Figure 50. Effect of convert-start pulse-width on timing.

Digital Gain Control: Figure 51 shows a method of adjusting the AD572 gain digitally, using an 8-bit DAC. The 100 Ω GAIN ADJ potentiometer is replaced by a 15 Ω fixed resistor. This biases Full-Scale high by approximately $35\Omega/20,000\Omega = +0.18\%$ of FSR. The AD559 has a large positive compliance voltage which permits its Current Output, pin 4, to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage-reference, connected through a 1k Ω resistor to Reference Current input (pin 14). The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current $-2.5\text{mA} \times 15\Omega/20\text{k}\Omega = 1.88\mu\text{A}$, or $-1.88\mu\text{A}/500\mu\text{A} = -0.38\%$ of FSR; this permits a digital gain adjustment range of approximately $\pm 0.2\%$ FSR from nominal.

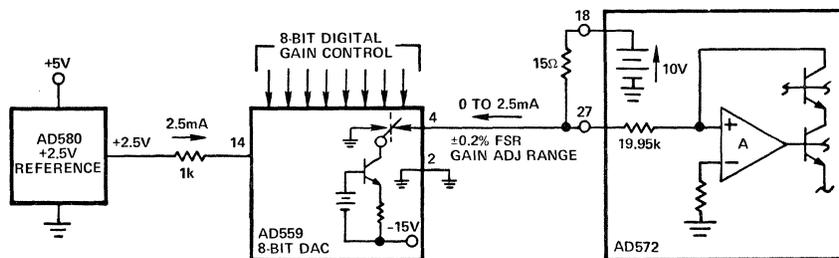
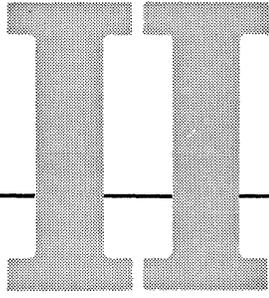


Figure 51. Digital gain control using 8-bit DAC.

CONCLUSION

As we noted at the beginning of this chapter, it would address itself to a discussion of *converter* microcircuits. As we also noted, it should not be forgotten that converter microcircuits from Analog Devices are accompanied by a panoply of supporting linear IC's – references, sample-holds, multiplexers and CMOS switches, resistance networks, V/f converters, op amps, and instrumentation amplifiers – employing similar technologies (as appropriate) to those used for converters.

Also existing are concepts and in-process designs of future generations of conversion products, involving higher levels of speed, accuracy, and integration. However, macro-technologies are not yet abandoned as a means of building converters (e.g., 16-bit) and subsystems, and quite often the earliest generations of a product are in the form of potted modules. In the next chapter, we will consider in more-thorough detail what it takes to design 12-bit discrete converters, using a familiar product line as our example.



Converter Design Insights

Chapter II-3

In Chapter 1, “Understanding Converters,” there is included a hasty survey of the more-popular converter design approaches. The intention of this chapter is to provide more detailed and practical information on the design and construction of D/A and A/D converters.

In this day and age, it is unlikely (from the standpoint of cost) for a user to design his own converters. However, an understanding of the principles and *caveats* may be helpful in gaining an understanding of just what is involved in the detailed design of a 12-bit converter, so that engineering considerations will join economic considerations and a decision to buy rather than make can be made with few regrets. The design approach discussed here is typical of vintage modular designs (using early Analog Devices integrated circuit chips), still available in the popular “12QZ” series.

The design approach chosen for D/A conversion uses quad current switches and a monolithic thin-film resistor network of the AD850 type. The A/D conversion example uses this D/A converter in a successive-approximation device.

This practical example will serve the reader’s purposes well, and for a number of reasons. First, it represents an approach actually used for the construction of converters in production quantities, to be sold at competitive prices, with resolutions ranging from 8 to 16 bits. In addition, it has speed adequate for most purposes; the appropriate components were accessible to the designer at reasonable cost; and having moderate complexity, it is an excellent starting point for understanding other designs of both greater and lesser complexity.

With this view of the inner workings of products engineered for OEM users (probably the first time a module manufacturer has ever “told all”), users of converters may gain better insight into the devices they are using, and design engineers may gain some ideas or principles that will help them in their future designs.

CONVERTER DESIGN

Many writers on this subject claim that a high-precision D/A converter is the most-difficult-to-design section of any device using it, including an A/D converter. This is only partially true; the added design elements, circuiting, and physical layout involved in using a D/A converter in an A/D converter should not be slighted. The increase of difficulty in building A/D converters of high speed and accuracy, even with a well-designed basic D/A-converter building block, can be massive.

The difficulties of designing D/A converters increase rapidly with the useful resolution sought in the design. 8-bit D/A converters are relatively easy to design and manufacture, since the allowable uncertainty is of the order of 0.2%. Ten-bit converters are much more difficult to design, since the resolution sought is 0.05%. By the time one reaches 12 bits of resolution (0.0125%), the design and manufacturing problems become acute. And 16-bit converters should be left entirely alone by the do-it-yourselfer.

In most cases where the make-or-buy decision involves large numbers of units, it may be comforting to follow the example of the mass-transportation officials who suggest:

“... leave the driving to us,” for reliable, economical, and carefree arrival at one’s destination.

REVIEW OF D/A TECHNIQUES

Figure 1 reproduces the current-weighting D/A converter depicted in Figure 14 of “Understanding Converters.” This is perhaps the simplest approach to performing a digital-to-voltage conversion. A set of binary-weighted currents flows through a $5k\Omega$ feedback resistor, producing an analog output voltage proportional to the sum of those currents that are turned on.

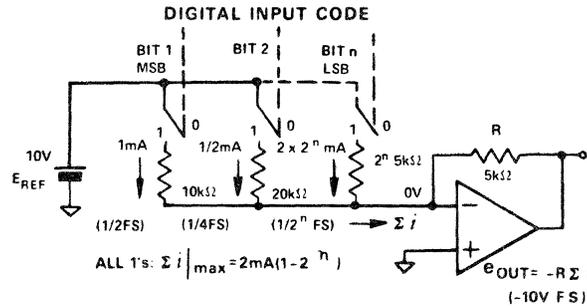


Figure 1. Elementary D/A converter circuit.

While this approach looks simple, the problems of manufacturing a converter of this type are large. The two most difficult problems are the switching speed and resistor T.C. matching. For a 12-bit converter using a $10k\Omega$ resistor for the most significant bit (MSB), the least-significant-bit resistor would be $20.48M\Omega$. This range of resistance cannot be obtained from a consistent film material, so that resistance temperature coefficients cannot even be approximately matched. Furthermore, the switching speed of a current switch depends upon the current available to charge the stray capacitances. Since the LSB is $0.5\mu A$, if the stray capacitance is $10pF$, then the settling time for 1 LSB is $200\mu s$. Obviously, if all currents could be of the order of $1mA$, the conversion time for all bits will be uniformly shortened.

Figure 2 shows a way in which this is commonly accomplished. Basically, the NPN current sources are all made equal to $1mA$.

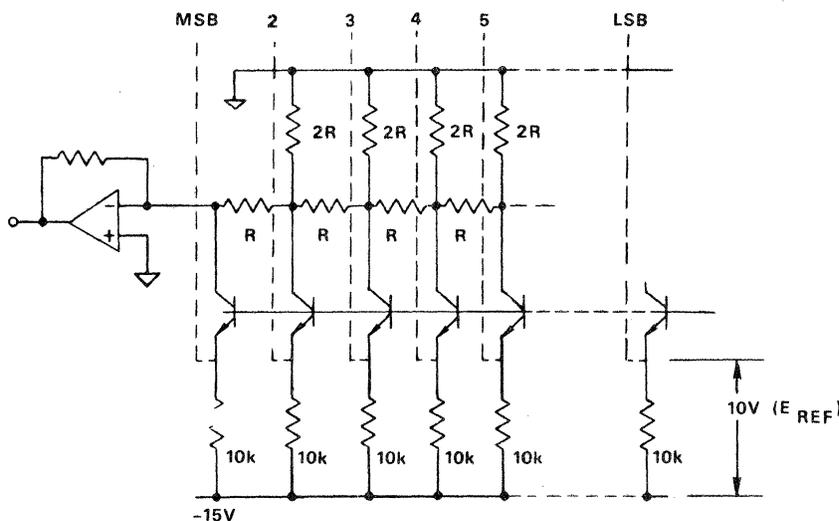


Figure 2. D/A converter using equal current sources and R-2R ladder attenuator.

The individual currents from the collectors of the current source transistors are subjected to binary weighting via the R-2R network. D/A converters of this type yield extremely high speed conversions (e.g., the MDA-10F settles in $40ns$). Other advantages of this circuit are evident: the resistance range is very reasonable and the selection of transistors for matched

V_{BE} is simplified. However, a disadvantage of this circuit is that it requires *two* accurately-trimmed low-T.C. resistance networks.

A third technique (Figure 3) combines good features of both techniques. Commonly known as the quad current-source approach (see Figure 20 in Chapter II-1), the technique relies on binary-weighted current sources, in groups of four, with currents ranging from 1mA (MSB) to 1/8mA. Three such quads provide 12 bits of resolution. The currents from the third quad are resistively attenuated by 16:1 before summing with the currents in the second quad, and this sum is again attenuated by 16:1 before summing with the first quad's currents. Much of the circuitry, being repetitive, is highly amenable to monolithic integration, as exemplified by Analog Devices' monolithic resistors and subsequent converter designs, such as the AD562.¹

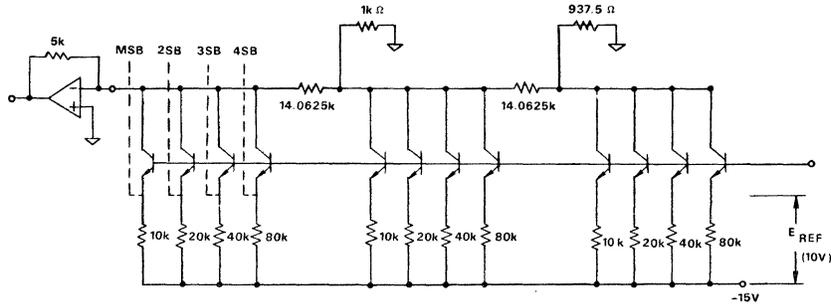


Figure 3. D/A converter using binary-weighted quad current sources.

THE IMPORTANCE OF LOGIC BUFFERING

The manner in which the switching signals from logic circuits are buffered from the analog circuitry of D/A converters, though of great importance, is not commonly well-understood. There are many ways (some good, some not so good), to turn electronic switches on and off. The simplest is the single diode approach shown in Figure 4 (see also Figure 19 in Chapter II-1).

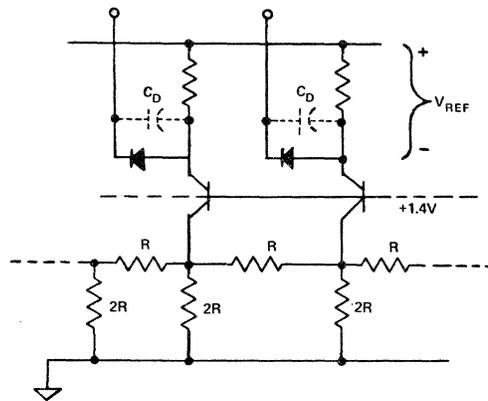


Figure 4. Diode switching in D/A converter.

Here the common base line of the current sources is biased at midrange value of the TTL threshold (1.4V). When the data inputs are low ("0"), the diodes are forward-biased and draw the bit current away from the PNP current source. This, in effect, back-biases the PNP emitter-base junction, turning the transistor off. When the logic input goes high ("1" — greater than 2.0V), the diode is back-biased and the transistor current source is turned on.

Two major error sources are characteristic of this simple approach. The first is leakage current in the diode. 10nA may sound negligible at room temperature, but at 70°C this figure is in the neighborhood of 1μA, an appreciable error. Similarly, when the switch is in the high state, the diode is back-biased; logic transients on the data input side, though not of sufficient magnitude to affect the switch state, are coupled through the diode capacitance,

¹"12-bit Integrated-Circuit D/A Converter," R. Craven and S. Harris, *Analog Dialogue* 8-2, 1974.

to the emitter of the current source, thereby producing transient errors in the weighted current.

Figure 5 shows a much-improved way to electronically switch current sources on and off. This buffered scheme involves essentially two D/A converters. The first, using Q1–Q4, performs the actual high-accuracy conversion. The second D/A, composed of Q5–Q8, accepts the digital inputs and applies back-bias to the emitters of the appropriate switching transistors, Q1–Q4, as required by the input code (which must be complementary to the input code required by the circuit in Figure 4). For example, when the input logic at Q5 is high, the diode is reverse-biased and Q5 conducts. Its positive collector current biases the emitter of Q1 high and effectively diverts the flow of I_1 . When the logic input is low, the diode shuts off Q5's collector current, which allows I_1 to flow normally in the collector circuit of Q1. The buffered scheme solves both problems of the single-diode approach.

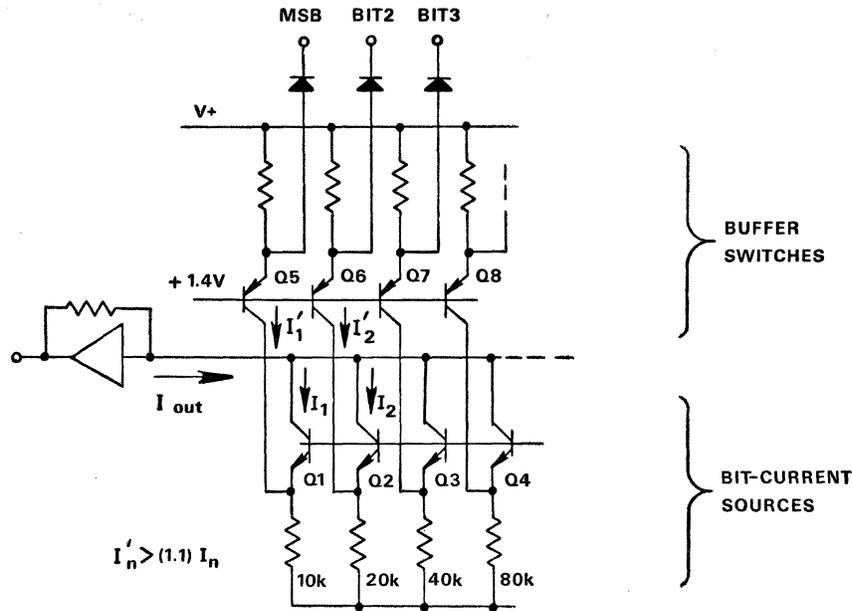


Figure 5. Buffered switches in D/A converter.

Often overlooked in the buffer design is how much swing must be provided at the emitter of Q1 to toggle the switch fully from *on* to *off*. The following exercise may be revealing:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{ON}}{I_{OFF}}$$

For 12-bit resolution, with 1/10LSB uncertainty,

$$\frac{I_{ON}}{I_{OFF}} > 10 \times 2^n \cong 40,000$$

Since $\ln(40,000) \cong 10.5$, at 70°C (343°K)

$$\Delta V_{BE} = 29\text{mV} \times 10.5 = 300\text{mV}$$

and, at 125°C,

$$\Delta V_{BE} = 33\text{mV} \times 10.5 = 350\text{mV}$$

If one considers that the standard TTL input logic thresholds are 0.8V for “0” and 2.0V for “1”, and that diode drops, while conducting I_{ON} , may approach 0.7V, it is evident that the base line must be held within a narrow range of voltage, especially at higher temperatures.

MONOLITHIC COMPONENTS

The basic monolithic conversion components to be discussed in connection with the circuitry encountered in the remainder of this chapter are early monolithic quad switches and the AD850 monolithic thin-film resistor network.

The key factor establishing the accuracy of the quad switches is the binary weighting of the current-source transistors, Q1–Q4 in Figure 6. It is well known that two matched transistors, operating at current densities that cause the V_{BE} drops of the transistors to be equal, will exhibit theoretically perfect tracking with temperature.

If two perfectly-matched paralleled transistors together draw twice the total emitter current of a third matched transistor, their V_{BE} 's will nevertheless be equal.

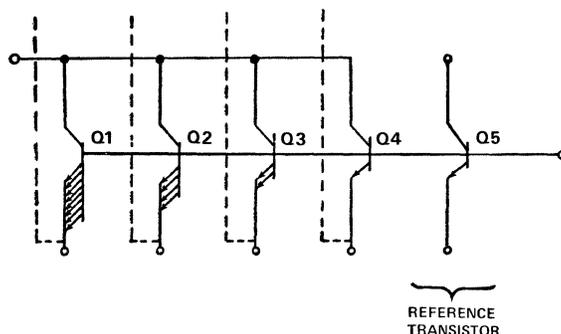
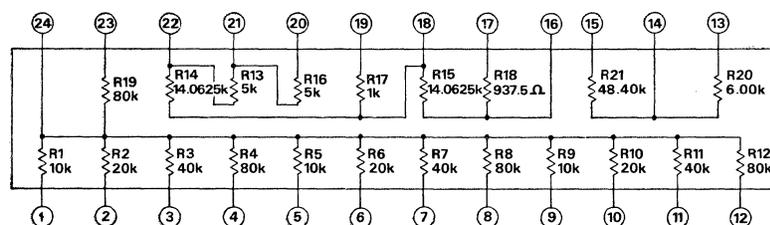


Figure 6. Binary-weighted current source transistors.

The current switches, Q1–Q4, though conducting currents in the ratio 1:2:4:8, have similarly-weighted emitter areas, hence equal current densities, and will therefore exhibit equal V_{BE} 's. If the V_{BE} drops of the current sources are equal, then errors in current due to variations of V_{BE} in series with the measuring resistors track perfectly for all four switches.

The finite β of the current-source transistors represents another source of conversion error, since the base current, $I_E/(1 + \beta)$ subtracts an increment from the emitter current. Monolithic construction leads to initial β -matches within $\pm 5\%$. When used with the reference transistor, Q5, the effects of both V_{BE} and β variation with temperature can be fully compensated, resulting in extremely low temperature coefficients for the conversion.



R 1	10k REF	0.1% ABS	R 8	80k	0.8%	R 15	14.0625k	1.0%*
R 2	20k	0.015%	R 9	10k	1.0%	R 16	5k	0.1%
R 3	40k	0.03%	R 10	20k	1.0%	R 17	1k REF	0.1% ABS
R 4	80k	0.05%	R 11	40k	1.0%	R 18	937.5Ω	1.0%*
R 5	10k	0.1%	R 12	80k	1.0%	R 19	80k	0.1%
R 6	20k	0.2%	R 13	5k	0.1%	R 20	6.00k	0.1%
R 7	40k	0.4%	R 14	14.0625k	0.1%*	R 21	48.40k	0.1%

NOTES:

All resistors ratio to R1 except R14, R15, R18 which ratio to R17. Tolerances shown are for 12-bit accuracy and degrade by factor of four maximum for 10-bit accuracy.

Total positive or negative "contribution to error" is less than 0.012% BCD network, AD851, is: $R_{13} = R_{16} = 4k\Omega$; $R_{14} = 8.1325k\Omega$; $R_{15} = 8.4375k\Omega$.

Figure 7. Typical monolithic thin-film resistor network (AD850).

The companion AD850 thin-film resistor network is shown schematically in Figure 7. Included in this network are:

- Bit-weighting resistors (R1 – R 12)
- Reference compensation resistor (R19)
- Interquad divider resistors (R13, R14, R15, R17, and R18)
- Gain resistors (feedback resistor in D/A's, input resistor in A/D's) (R13 and R16)
- Reference input resistors (R21 and R20)

When used for all its indicated circuit functions, this resistor network has the interesting property that as long as the resistors track one another as temperature changes, the output voltage error due to absolute resistance changes for any given code combination will be nil. The reason is that absolute resistance changes of *all* resistors in the network make little difference – the tracking *between* resistors is the only item of importance. For the AD850, temperature coefficient of tracking error is $\pm 1 \text{ ppm}/^\circ\text{C}$.

COMPONENT TOLERANCE

Save for the reference and the output amplifier, the errors produced by the analog components used to build a D/A converter can be mainly attributed to errors caused by the bit switches and resistance tolerances. The V_{BE} and β mismatch errors in the quad current switches have already been briefly touched upon. Naturally, the tracking of these parameters with temperature influences errors measured when the temperature changes.

Interquad V_{BE} matching is required to minimize errors between bits in the first quad and bits in the second quad. If the V_{BE} difference between Quad 1 and Quad 2 were 100mV, then the apparent error in bit 5 relative to full scale would be 0.03%. When the three quads used in a 12-bit converter are assembled, the V_{BE} groupings of at least the first two quads must match. It can be seen that the availability of quads that can be graded and selected for the required accuracy and matching is crucial to obtaining a successful converter design.

The resistor specifications listed in the table (Figure 7) are often misinterpreted. It is imperative that a D/A-circuit designer understand the meaning of the tolerance specifications, and their effect on a given resistor's contribution to the total error. The most-significant-bit resistor, R1, is used as the reference resistor for ratio-matching purposes; all the other resistors are referred to it. The second-bit resistor, R2, is shown as having a ratio tolerance of 0.015%. Some persons automatically interpret this as meaning that the second-bit resistor could contribute an error of 0.015% *relative to full scale*. This interpretation is wrong. Since the MSB (R1) has a weight of $\frac{1}{2}\text{F.S.}$, the second-bit contribution to error has a weight of $\frac{1}{4}\text{F.S.}$ This means that a ratio tolerance of 0.015% for R_2/R_1 will cause bit 2 to have a contribution to full-scale error of 1/8 LSB of 12 bits (0.00375%).

Applying a tolerance analysis to the specifications, one might be led to expect that a 12-bit set of quads and an AD850, when assembled (with the best of care) will always yield a 12-bit-linear D/A converter, with no bit-trimming necessary. The overall error actually depends upon a statistical distribution of the errors of both sets of components. In the very worst case, it is possible for some code combinations to be outside the 12-bit linearity expected. For this reason, we recommend certain final-trimming procedures, which will be described later. Besides being occasionally necessary, they lead to improved temperature-margins and a sense of confidence that each assembled unit is well within specifications.

THE INTER-QUAD DIVIDER

The inter-quad division network of the AD850 functions quite simply. The basic idea is depicted in Figure 8a, where a current source delivers its current to the node joining a 15k Ω resistor and a 1k Ω resistor. Since the 15k Ω unit is terminated in virtual ground (the amplifier summing junction), the voltage across both resistors will be equal. Hence, 15/16 of the original current (I) goes off to signal ground via the 1k Ω resistor, while the remaining 1/16 I is added at the summing point via the 15k Ω resistor. The problem is just a little more complicated when the multiple-current-source situation depicted in Figure 8b exists.

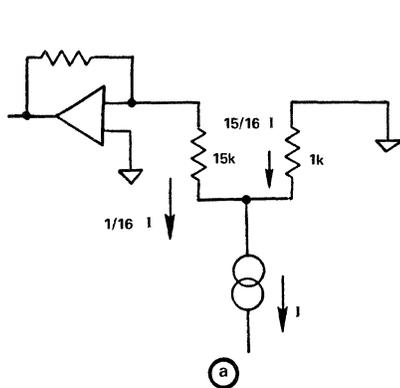


Figure 8a. Current attenuation to 1/16.

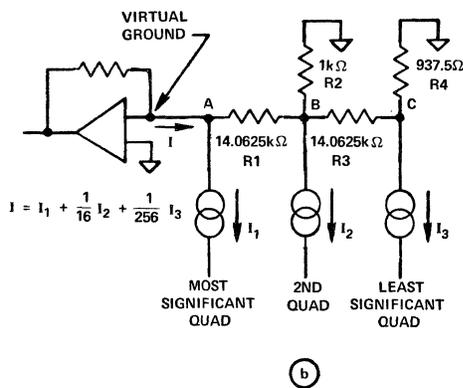


Figure 8b. Current attenuation of three sources to 1, 1/16, 1/256.

Figure 8b is a simplified diagram of the switch outputs and the interquad weighting resistors of the AD850. The 3 current sources I_1 , I_2 , I_3 , represent the common collector lines of the three quads. The current from the most-significant quad (MSQ) flows directly into the summing node of the op amp (virtual ground). The second quad's current is split 16:1 by the following means: As the current enters node "B", 15/16ths of I_2 goes to signal ground through the parallel combination of R_2 with $(R_3 + R_4)$. The remaining 1/16 goes off through R_1 to the summing node "A". Note that the parallel combination of R_2 and $R_3 + R_4$ is 937.5 ohms. Thus, the inter-quad current split effected at node "B" is precisely 16:1.

The inter-quad current division at node "C" is a little more difficult to understand. It is easiest to analyze the two interquad dividers as a single network and solve for a 256:1 attenuation of I_3 as it reaches node "A". By a straightforward analysis, one can learn that the current entering node "B" from node "C" is $(1/17)I_3$. At this point, it is further split, in the ratio 15.0625:1, by R_1 and R_2 . The product of 15.0625 and 17 is, as desired, 256.

One should note that, in the practical situation, the current sources depicted at Figure 8 are the collectors of common-base NPN transistors. The designer must be aware of the fact that when all bits are turned on, a voltage drop appears at nodes "B" and "C" of the order of -1.8V. For this reason, the common base line of the current sources should be operated below -2.0V, in order to keep the transistors well within their linear region. Also, it should be noted that the output resistance of the collectors in the most-significant quad can be as low as $30M\Omega$ without significantly affecting divider accuracy.

REFERENCE LOOP

The overall gain and accuracy of a D/A converter depend on that of a stable current reference. The switch-quad/AD850 system is designed to use the common 6.2V "zero-T.C." zener reference diodes.

Figure 9 shows on such diode, the 1N829A, used in a circuit that provides it with an essen-

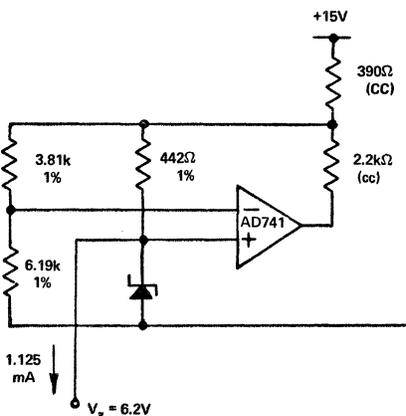


Figure 9. Constant-current excitation of precision reference Zener diode.

that it is difficult to prevent the circuit from bottoming on the -15V rail, since the base of the PNP buffer is within 0.6V of the -15V line.

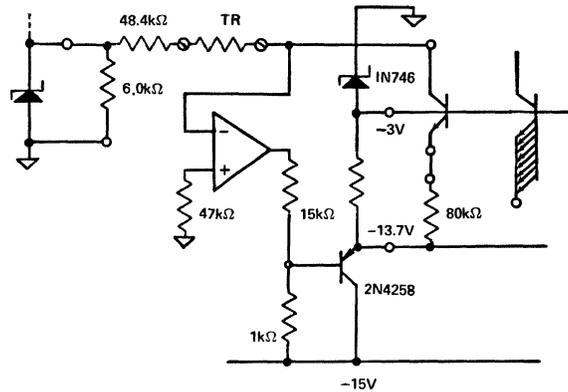


Figure 11. Reference circuit using inverting input.

In Figure 12, the basic non-inverting configuration of Figure 10 is revised to include an anti-latchup circuit – CR2 and the 4.7kΩ resistor. It also includes frequency-response shaping to prevent transient voltages from upsetting the reference loop, as follows: In junction-isolated IC's, such as the quads employed here, capacitive coupling from the collector of one NPN transistor to the collector of another NPN transistor exists via the depletion capacitance of the substrate. When the input bit combination changes, the DAC's output amplifier will usually be driven in a slewing condition, resulting in a fast rising voltage edge on the common collector line. This fast-moving edge is coupled to the collector of the reference transistor on the same chip. Since the collector of the reference transistor looks at a high impedance (48.4kΩ), the coupled transient is applied to the noninverting terminal in the circuit of Figure 10. This, in turn, can upset the reference loop for a period of microseconds.

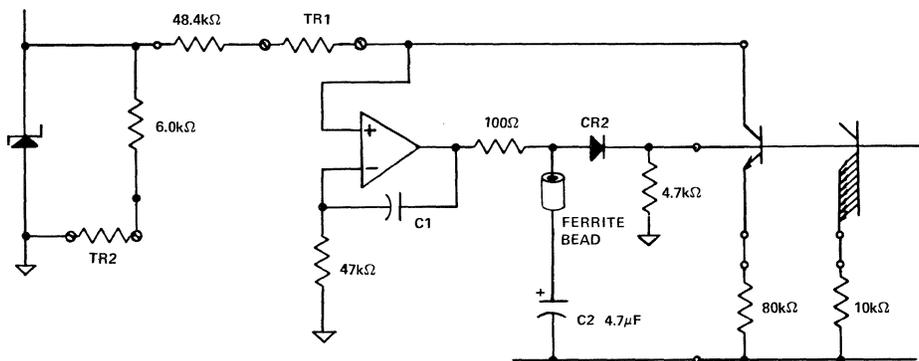


Figure 12. Reference circuit with frequency shaping and anti-latchup circuit.

In the configuration of Figure 12, we can see a means by which this behavior can be controlled. The voltage from the common base rail to -15V is kept from changing instantaneously by a 4.7μF capacitor. However, since a 4.7μF capacitance can by itself cause the reference amplifier to oscillate, a 100Ω isolation resistor provides a predictable time constant. C1, together with the 4.7kΩ common-mode bias-compensation resistor, rolls off the response of the amplifier on a 6dB/octave slope, which intersects unity open-loop gain at the break-point of the 100Ω x 4.7μF combination. CR2 and the 4.7kΩ resistor prevent the latchup mode mentioned earlier. The ferrite bead is added to prevent the common-base bit-switches (with f_t 's of approximately 500MHz) from oscillating in the 100–200MHz region.

The 6.0kΩ resistor on the AD850 (R20) is shown connected to signal ground in Figures 10, 11, and 12. R20 provides 1mA offset current in bipolar offset-binary D/A converters, when it is connected to the output current terminal of the converter. This resistor should be grounded when the unipolar configuration is desired, so that the zener diode (Figure 9) runs

at constant current. Ignoring this consideration – leaving R20 open – can result in a gain error of 0.2%. Of course, with an external reference, or with a circuit in which the reference voltage is applied via a low impedance (e.g., the emitter of an inside-the-loop follower) it would not matter greatly whether or not R20 were terminated.

TRIMMING HIGH-ACCURACY CONVERTERS

One should be always aware that, however easily we may talk of 12-bit accuracy, it still represents *total error* of the order of 0.01%, which may circumspect engineers still consider uncomfortably-close to the limits of the state-of-the-art. Second- and third-order tolerance buildups can become highly significant, as can inadvertent errors in interfacing a converter with its analog output circuit or a measurement circuit.

For 12-bit (and better) linearity, the designer of converters should always seek *the best-possible resolution*, and should make provisions for final trim of the highest-order bits in order to attain it. In addition, he must provide both coarse and fine trims of the overall “gain” (i.e., scale factor) of the converter, offset-bias-current trim for bipolar converters, and overall zero adjustment of the output amplifier.

Let us start with the bit-trimming procedures. The quad switches and the AD850, in combination, are amenable to highly accurate and stable trimming. Figure 13 is a fairly complete schematic of the first 8 bits of a 12-bit D/A; it will illustrate the discussions to follow on trimming and adjustment.

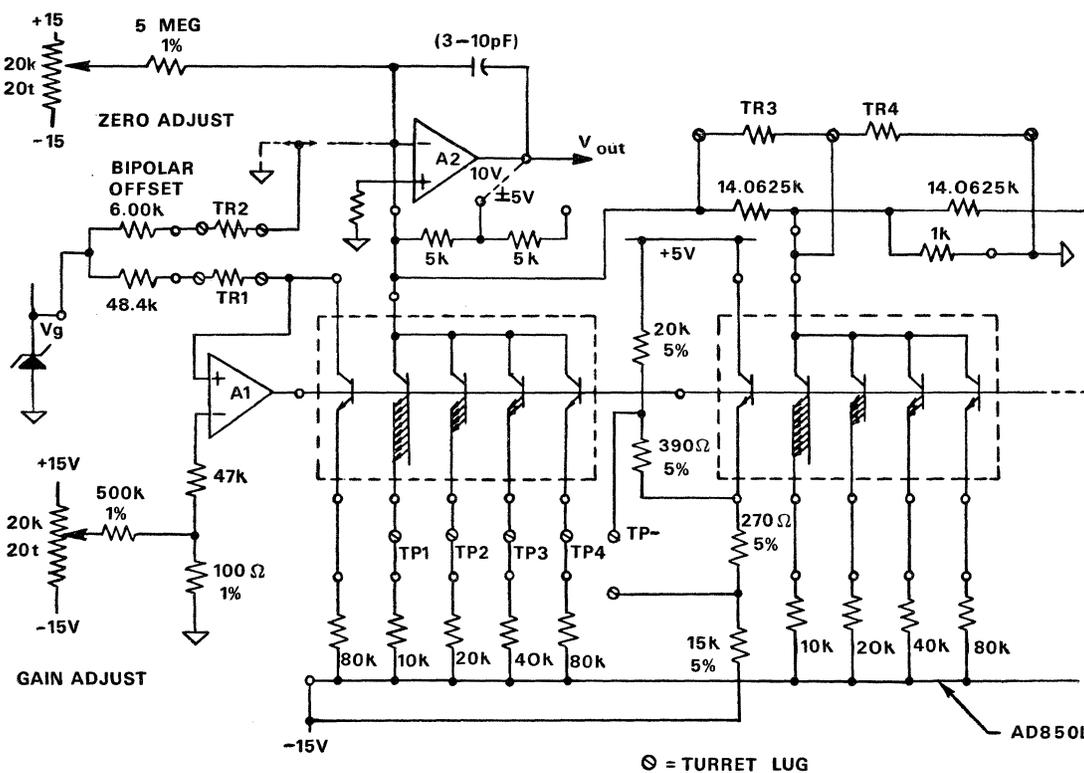


Figure 13. Connections for trimming a D/A converter for 12-bit accuracy.

For final trim of the first 4 bits, a number of nanoamperes of current must be added to or subtracted from the emitter current of each switch to bring it to its calibrated relative value. To do this, we use the conveniently available reference transistor of the second quad to establish two small offset voltages, which will be centred about the emitter voltage of the bit-switches. In Figure 13, the quad’s reference transistor is biased by approximately 1/8mA; ordinary carbon composition resistors may be used. The voltage at TP+ is 200mV below the emitter voltages, while that at TP- is 200mV above the emitters. These arbitrary designations are for convenience in trimming.

If the bit being adjusted does not have sufficient weight (measured at the output, using instrumentation of adequate precision), a current ΔI is added to that bit by connecting a re-

sistor of appropriate value ($R = 200\text{mV}/\Delta I$, or conductance 2.5 micromho/LSB) from the emitter of the bit switch in question to TP+. Similarly, if the bit weight is too high, it can be decreased by connecting an appropriate resistance between the emitter and TP-. It should be noted that, as temperature varies, the V_{BE} of all the transistors will also vary. But the trim voltages will remain fairly constant and centred around the nominal emitter voltage of the quad's reference transistor.

To minimize the effects of slight mismatches between the first two quads, due to either V_{BE} or β differences, one should provide for slight trimming of the first interquad divider (i.e., the relative weight of the second quad). If, after trimming the first four bits, the fifth bit differs from $\frac{1}{2}$ the fourth bit by a significant amount, the following procedure may be followed:

If bit 5 is too *low* in weight, install a trim in the TR3 position (usually of the order of megohms). If bit 5 exhibits *too much* weight, it can be attenuated with a trim in position TR4 (typically of the order of $100\text{k}\Omega$ or more).

Normally, 1/8W carbon-composition resistors can be used in these positions, since only very small quantities of current are drawn through them. The carbon-composition-resistor temperature coefficients are attenuated by both their overall weight relative to the resistors they parallel, and the bit weight, relative to full scale. This effect is negligible.

To trim the overall gain of a converter, trim-position TR1 is utilized. First center the gain-adjust pot (10 turns from one end). Install a decade-resistance box for TR1, and turn on the first four bits (00001 . . . 1 in complementary binary). With the $5\text{k}\Omega$ resistor serving as the feedback resistor for the output amplifier, the proper output voltage should be 0.3750 (unipolar mode) for best adjustment of TR1. Replace the indicated decade resistance by the nearest standard precision-film-resistance value. (R20 of the AD850 should be grounded during this operation). Final gain trim can now be accomplished with the trim resistance installed in TR1. The resistance values shown in Figure 13 provide a mean adjustment of $\pm 0.25\%$.

To adjust zero in unipolar converters, turn off all bits (1 1 1 . . . 1 in complementary binary), and adjust "Zero Adjust" for 0.0000V out. In bipolar converters, to trim the bipolar offset ($\pm 5\text{V}$ full-scale output range), center the 20-turn "zero-adjust" pot and connect the bipolar offset resistor to the output amplifier's summing point, as indicated in Figure 13. Using a decade box in TR2, and leaving all bit switches off, adjust the decade box for -5.0000V out. Install the nearest value of trim resistance to the reading of the decade box in the TR2 position. Final offset trim can now be performed with the MSB only on (0 1 1 1 . . . 1 in complementary offset binary) using the "zero-adjust" pot.

Further details on testing procedures and trimming of D/A and A/D converters can be found in chapter II-4, "Testing Converters." An additional detail of the design of the circuit of ure 13 is worth mentioning:

The feedback capacitance (3 to 10pF) around the output amplifier compensates for the capacitance of the common collector rail, the input capacitance of the output amplifier, and circuit strays. Circuit wiring capacitances should, of course, be minimized to keep the value of feedback capacitance low, since it tends to increase the output settling time. It is adjusted for "optimum" response: minimum transients *and* settling time. Its omission may cause oscillations, or instability.

TEMPERATURE VARIATION EFFECTS

Reiterating an earlier statement, if all resistors in the AD850 network track perfectly, then even if their absolute value changes, say at a rate of $50\text{ppm}/^\circ\text{C}$, the output voltage will remain constant (assuming constant V_Z). This can be shown by the following example: If the reference-current resistor (R21, $48.4\text{k}\Omega$) increases by 2%, the reference current would be decreased by 2%. However, the feedback resistance around the output amplifier is also increased by 2%, increasing the gain by 2% to compensate, with no net error. Since the bipolar offset resistor, R20, also increases in proportion, there is no net error in bipolar applications. Vari-

ation of the current-weighting resistors is compensated by similar variation of the resistance in series with the emitter of the reference transistor. And finally, the interquad attenuation resistors track one another and maintain constant attenuation of the outputs from the less-significant quads.

This example describes the ideal situation. In practice, the resistance values will track ratiometrically to only about 1ppm/°C. Further, the discrete metal-film resistors used for TR1 and TR2 will undoubtedly have temperature coefficients that differ from those of the ladder resistors. Since their effect on total resistance is incremental, the effect of their T.C. on circuit performance is reduced. However, one should always perform a calculation to be sure that they can safely be neglected. Here is an example:

The absolute TCR of the AD850 is within $\pm 25\text{ppm}/^\circ\text{C}$. Assume that TR1 and TR2 have an absolute TCR range of $\pm 50\text{ppm}/^\circ\text{C}$. The effect of these mixed TCR's is dependent upon the absolute value of V_Z . The greater V_Z is, the larger the value of TR1 (and TR2). For $V_Z = 6.5\text{V}$, at the high end of a +5% tolerance range, the worst case of TCR mismatch will be approximately $5\text{ppm}/^\circ\text{C}$ for a $50\text{ppm}/^\circ\text{C}$ TCR of TR1. If the TCR of TR1 is reduced to $\pm 10\text{ppm}/^\circ\text{C}$, this drift mismatch is reduced to $2.5\text{ppm}/^\circ\text{C}$. If the Zener voltage is at its nominal value, 6.2V, and TR1 is $\pm 10\text{ppm}/^\circ\text{C}$, then gain drift is reduced to approximately $1\text{ppm}/^\circ\text{C}$. Suffice it to say that the closer V_Z is to the low end of its allowable tolerance range (6.05V), and the lower the TCR of the trim resistors is kept, the lower the effect of temperature on gain T.C. Then, scale factor (or gain) drift becomes almost entirely dependent on the Zener diode's voltage T.C.

Another contributor to gain drift is the offset drift, with temperature, of the reference amplifier, A1. Both offset voltage and bias current drifts must be considered. As an example, suppose that the total effect amounts to $15\mu\text{V}/^\circ\text{C}$. This will contribute roughly $2.5\text{ppm}/^\circ\text{C}$ to gain drift ($15 \times 10^{-6}/6.2 = 2.5\text{ppm}$). Gain drift error can also result from a reduction in open-loop gain of the output amplifier. For instance, a gain change, in A2, from 20,000 to 10,000, can result in an error contribution of 0.005%. It is therefore very desirable for A2's open-loop gain to be greater than 40,000 at room temperature.

CURRENT vs. VOLTAGE OUTPUT

A converter can be built to produce either an analog current output or an analog voltage output. The AD561 (10 bits) and the AD563 (12 bits) produce a basic current output, which is externally converted to a voltage using an additional output amplifier. However, since the op amp must slow down the response, some users prefer a current output for their application, or a passively-derived (small) voltage output.

Since the drift of the current output is not compensated by a tracking feedback resistor, the drift of current output from the D/A circuit in Figure 13, with the amplifier removed, is subject to the absolute TCR of the resistance ladder network and can be as great as $\pm 25\text{ppm}/^\circ\text{C}$. The current output terminal of the D/A can be terminated in a resistive load to ground. However, one must observe the range over which this kind of loading is applicable. A total load resistance of $1\text{k}\Omega$, with 2mA full-scale output current, will produce an output voltage of -2V full scale. Higher-value resistors will drive the common collector bus into saturation, producing excessive nonlinearity.

Though it might appear at first glance that the interquad division ratios might be disturbed by using a resistive load instead of a virtual ground, vigorous application of Norton's theorem will show that only the overall scale factor is affected. With a resistive load, the overall scale factor is determined by the external load, in parallel with the resistance looking back toward the interquad dividers (and — in the case of bipolar converters — the offset current resistor (R20)).

If the output voltage developed across a passive load is to be amplified, attention must be paid to the common-mode and offset drift requirements of the output configuration and the choice of resistor ratio in the amplifier feedback circuit, especially if large amounts of gain are desired. The problem of gain temperature coefficient due to non-compensation of the absolute TCR by the unused built-in feedback resistor may be solved to a degree by us-

ing a discrete $48k\Omega$ resistor, matching the TCR of the external load resistor, to set the reference current (and another matching resistor to replace R20 for bipolar applications). Though the loading effect of the interquad resistances will tend to worsen it, the gain-temperature coefficient will be greatly improved by good discrete-resistor tracking.

ON ERROR BUDGETS

One can see, from the above discussion, that there are many sources of error. As desired resolution and linearity increase, and as first-order errors are decreased, the many sources that contribute 2nd and 3rd-order errors become more important. One way that some designers keep these sources in mind and try to account for their probable contributions is to use some form of error-budget analysis.

This consists of listing all the anticipated sources of error, with their expected worst-case and probable contributions, and using some form of linear or root-sum-of-the-squares summation to estimate the total error.

Error budget analysis, used as an intelligently-applied checklist, is at its most-useful in pinpointing those sources of error that must be minimized, either by circuit design, by trimming, by component selection, or by performing some cost tradeoff.

As a means of predicting total error, error budgets are no better than the assumptions made, both about the individual error sources and about the way they will occur and combine when the circuits are assembled in production quantities. A too-conservative design for no-rejects, based on straight summation of worst-case errors, may result in greater overall cost of production than a less-conservative but more-clever design (utilizing some insight into how errors might combine), even though the less-costly design may (nay, *should*) produce (an acceptable number of) rejects in testing. (The cost of rejects can be reduced by recycling.) On the other hand, it is possible to defeat the best estimate of overall error by poor layout or component choice, or the best estimate of cost by requiring excessive tweaking or rejects.

LAYOUT CONSIDERATIONS

Up to this point, we have dealt with the strictly electrical circuit design of digital-to-analog converters. We have discussed some of the finer points of error and drift compensation. Now let us turn our attention to those factors that do not show up in the schematic.

Sources of both static and dynamic errors must be considered when designing the layout of the converter. Static errors are most often caused by voltage drops in “ground loops” and result from carelessness in the layout process. To give an appreciation for how easily this problem can arise, consider a hypothetical example. Suppose an analog ground line has 50 milliohms of resistance between two points. Suppose the current variation through that piece of track is 0 to 10mA for various code combinations in the converter. The resulting change in ground potential is 0.5mV. If this ground happens to be in common with the output signal, this type of error can be disastrous in converter designs calling for 12-bit and better resolutions.

Furthermore, the selection of input/output sockets and pins is very important. It is not difficult to pick up $100m\Omega$ of contact resistance in an improperly-chosen connector. Suffice it to say that all lines carrying analog output currents must be carefully located, and calculations should be performed to ensure that lead-resistance and ground-loop errors are minimal. Never try to second-guess. Improper layout can also cause dynamic errors. To avoid them, the current-output bus of current switches (whether discrete or integrated) must be as short as possible and carefully laid out from three standpoints.

First, the longer the run from the current-summing point of the bit switches to the summing point of the output amplifier, the more likely it is to pick up extraneous EMI signals. Second, the longer the track from the output current bus to the summing point, the greater is its distributed capacitance. Third, the longer that track, the higher the inductance. This can lead to high-frequency oscillations, as mentioned previously. (NPN common-base current-sources, with f_t 's of 500 MHz, can easily oscillate in the 200- 300MHz region.)

Because converters interface high-speed, high-energy digital signals with high-resolution analog signals, great care is needed to minimize stray coupling of digital waveforms into the analog circuitry. For example, some D/A converters contain buffer registers to store the digital input words. All digital information is transferred with fast-rising edges of voltage and fast-changing currents. These produce radiation, which must be kept away from critical points in the analog section. A primary design rule is that the digital and analog sections be separated physically with (if at all possible) some sort of ground plate between them.

In addition, the 5V supplies used for TTL logic should be kept apart from the $\pm 15V$ supplies normally used for analog signal processing. In particular, the ground lines from the converter to the supplies should be kept separate and terminated only at the power supplies themselves. This will tend to keep the fast-rising current edges in the logic sections away from the relatively stationary currents encountered in the analog sections. It is generally true that the critical points in the analog sections of the converter are of relatively high impedance. Hence they are very prone to electrostatic pickup. Even though the foregoing discussion would appear to be applicable where speed is important, high-speed transients can sometimes cause dc shifts through rectification and ringing in marginally-stable circuits, and will often require filtering of the analog output.

The faster the desired analog response, the more critical such things as digital feedthrough become, because the analog output is not ready for use until the digital transients have died away. Even though the basic electrical design goal for settling time is several hundred nanoseconds, transients coupled to the output by poor layout may result in $1\mu s$ or greater settling time.

In the design of high-speed D/A converters for CRT display applications, digital transients due to stray coupling must be kept to very low levels. Also, the “glitches” due to intermediate states in code switching must be minimized. In Figure 14 is shown a DAC-10DF, a high-speed D/A converter specifically designed for CRT applications. It includes a sample-hold network to hold the output during switching, while the glitch-causing intermediate codes occur. Of greater relevance to this section, is the attention paid to layout considerations.

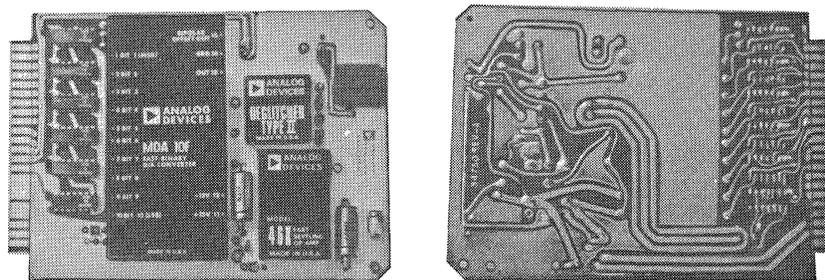


Figure 14. Deglitched high-speed display D/A converter.

The digital section is separated from the analog sections as though a physical barrier existed on the board of the MDA-10F D/I converter module. All the input lines enter through an edge connector on the digital side of the printed-circuit card. All those lines that pass into the analog section are prefiltered by a ferrite-bead, ceramic filter-capacitor combination. For complete isolation, the analog output is not brought back to the edge connector, since it would have to pass through the digital section once again. Instead, a 90-ohm-cable connector is provided at the analog end of the board. The additional module shown in the photograph is the “deglitcher” circuit that minimizes transients resulting from the unavoidable glitches that occur at the switch outputs during code changes.

SUCCESSIVE-APPROXIMATION A/D CONVERTERS

Of all the techniques for analog-to-digital conversion in use today in data-acquisition systems, “successive approximations” is perhaps the most widely used. A simplified block dia-

gram of a converter using this technique is shown in Figure 15. The basic idea of successive approximation is simple, as explained in preceding chapters. In somewhat more detail:

When the appropriate logic signal is applied to the *convert command* input terminal, the D/A switches are set simultaneously to their “off” state, except for the most significant bit (MSB), which is set to logic “1”. This turns on the corresponding D/A switch,* which applies the analog equivalent of the MSB to the comparator. Simultaneously an internal clock is released from the *inhibit* state and allowed to free-run. Until the first clock-pulse edge arrives, the MSB is being compared with the analog voltage. (The scheme shown is only one of several ways). When the first clock pulse arrives, the MSB has shown itself to be either too “heavy” or too “light.”

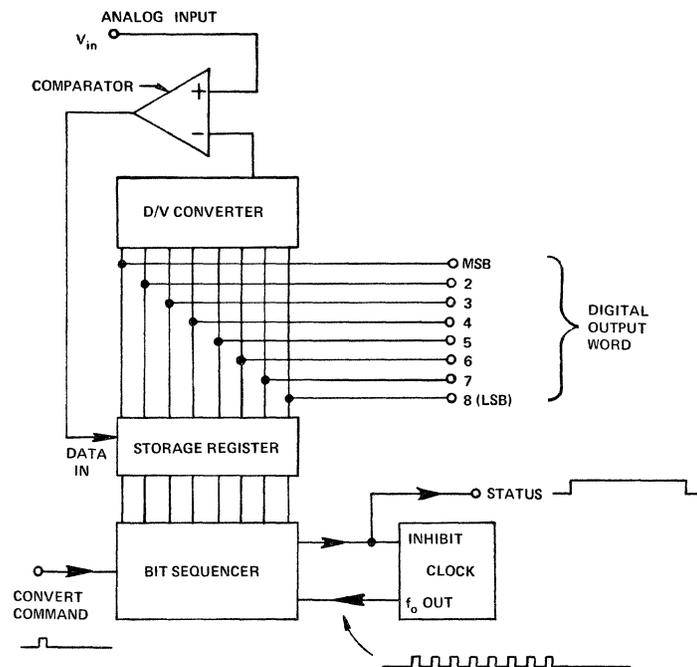


Figure 15. Block diagram of successive-approximations A/D converter.

If the analog input voltage is less than the MSB weight, the MSB will be switched off at the first leading edge of the clock pulse; if the analog input is greater than the MSB, the “1” will remain in the register. Besides enabling the MSB decision, the clock pulse simultaneously turns on the second bit. During the period of the second pulse, the sum of the result of the first choice and the second bit is being compared with the analog input voltage. The comparator’s state, when gated by the next clock pulse, will cause the register to either accept or reject that bit. In a similar manner, succeeding clock pulses cause the bits, in order of decreasing significance, to be tried, and accepted or rejected, until the LSB is finally accepted or rejected.

During this conversion time, the output of a *status* flip-flop is in its “busy/not valid” state, indicating that a conversion is taking place; it signals the end of a conversion by returning to its “ready/conversion valid” state.

Data from the parallel output lines of a successive-approximation converter are not valid until the end of conversion. However, in some applications, it is desirable to read out the data serially. When this is done, as it is in many successive-approximation converters, one must be careful to accept the serial data only as each bit becomes valid (such as on the leading edge of each clock pulse). Hence, after each bit decision is made, the data becomes valid, and the bit can be immediately shipped serially down a data line. Serial data can also be obtained at any later time if the parallel data is “jammed” into a shift register which can then be interrogated at will. Serial data should not be taken from the comparator output, unless it is bist-

*If complementary logic is necessary, as is typical of D/A converters using the quad switches described in this chapter, the “on” state would be “0”, as discussed in “Complementary Codes” in Chapter II-1.

latch-style flip-flops. The individual flip-flops are addressed by a 3-bit input code to the MSI element. This address simply enables the D line to that particular flip-flop. To sequence this arrangement, a 3- or 4-bit counter is used. A note of caution, however: the timing between clock pulses is somewhat more critical, because the addressable latch must be disabled and enabled between address changes to avoid changing the data in intermediate states in the addressable latch.

COMPARATORS: THE MOST CRITICAL ELEMENT

Many IC comparators are available on the market today, and the number continues to increase. Simple in concept, but tricky in practice, these intriguing circuits are a never-ending challenge to IC designers and users alike.

The ideal comparator would have infinite gain and zero comparison time. Practical comparators are limited by parameters similar to those of op amps: open-loop gain, slew rate, bandwidth, and dc and dynamic differential input characteristics. Beyond these, comparators are further distinguished by the availability of such features as *enable* terminals and output drive capability.

There are basically two different ways in which a comparator can be used: To compare voltage, differentially, and to compare current. In the voltage mode, the analog output of the D/A converter is in a voltage form (for instance, from the output of an amplifier) and is presented at the inverting input of the comparator. The analog input voltage is connected to the noninverting terminal. Comparators used in this scheme must have high common-mode input range and excellent common-mode rejection. For instance, a 12-bit converter should have at least 96dB of CMR to keep common-mode error well below 1/10LSB. The voltage mode is generally used in situations where the analog output from the D/A is restricted to the zero-to-1-volt region (e.g., by taking the output from a resistive load on a current-output D/A). The analog input is scaled down by the proper amount and applied to the + input of the comparator, while the 1-volt D/A output is applied at the minus input.

The use of comparators in the *current* mode is perhaps more common these days, because it allows better speed and temperature tracking, and places no severe requirements on the comparator's common-mode rejection. This is particularly well-implemented with the quad-current-switching D/A's discussed earlier in this chapter. Figure 17 shows why. The 5kΩ gain resistors that are normally used as the op amp feedback element to convert current to voltage in a DAC are used as the input scaling resistors. The summing point (pin 22, AD850)

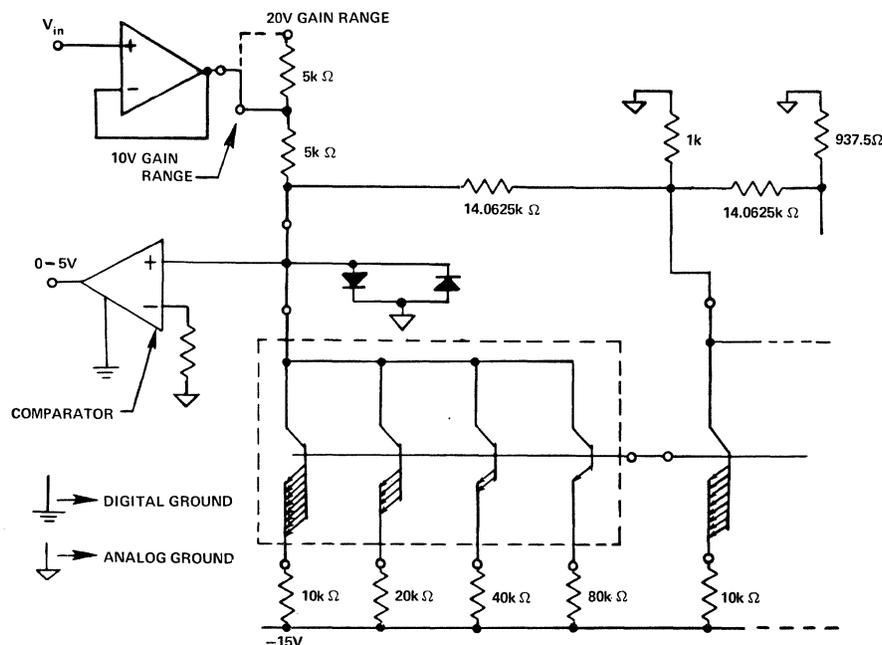


Figure 17. ADC using comparator in the current mode.

is connected to the minus input of the comparator. The plus input is returned to analog signal ground through an appropriate bias-current cancellation resistor (5 or 10kΩ || 15kΩ, for single-ended converters, additional || 6kΩ for bipolar converters). By doing this, we make use of the temperature tracking of the resistors of the AD850L network to retain near-perfect gain tracking.

The “window” determines the conversion accuracy one can obtain with any given comparator. The *window* is that range of input voltage over which the comparator output is traversing the linear region, between logic thresholds, and as such is a measure of the open-loop gain of a comparator circuit. For example, if the analog input is from 0 to +10V, and it is desired to perform a 12-bit conversion, the window must be less than 1mV for the conversion to be within one-half LSB (neglecting quantization uncertainty). Since the output of the comparator must swing between 0.4 and 2.4V to effect logic changes (TTL), the open-loop gain required for 12 bits is at least 2000. However, in practice, this figure should be at least 5000 to minimize the errors due to finite open-loop gain.

Besides gain, dc offset and drift, and impedance level, another spec that must be carefully considered in the selection of a comparator is its *speed*. The typical performance of integrated circuit comparators available today is specified by means of response diagrams on data sheets. A typical plot is shown on Figure 18; it can be seen that the speed is sharply influenced by the amount of overdrive of the comparator. The amount of overdrive applied to a given comparator in an A/D application depends on the input voltage range used and the resolution sought. The designer must be careful to plan for the minimal amount of overdrive appropriate to any given application.

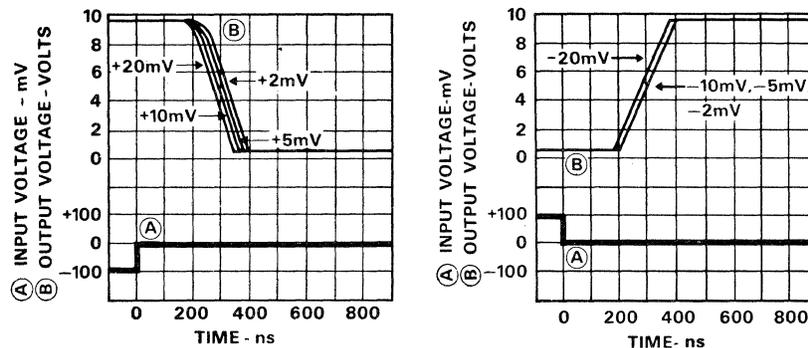


Figure 18. Typical comparator response as a function of input overdrive.

The most troublesome aspect of using any comparator, be it discrete or integrated, is the problem of maintaining frequency stability while within the linear region (i.e., in the “window”). Although the comparator is like an operational amplifier with no overt feedback, it is operating at high gain-bandwidth, with minimal feedback compensation. Even small amounts of parasitic feedback, either directly around the device, or via the power supply leads, can cause oscillation. These oscillations are generally caused by improper layout, for example, in separating the fast-rising output edges from the high-impedance input points. It is intuitively obvious that capacitive coupling of fast edges to the negative input could develop ringing or sustained oscillation when the net input is in the “window” region.

For this reason, it is recommended that adequate shielding, e.g., by ground plane, be used between the input and output. Also, it is wise to keep the digital ground terminal (normally returned to the output transistor of a comparator) away from the analog input grounds and signal lines. Furthermore, for IC comparators (whether the data sheet suggests it or not), it is a wise idea to buffer the load driven by the comparator output with a discrete transistor. This not only leads to a higher gain in the comparator, but will also lighten the changes in power dissipation in the internal output transistor, thereby eliminating thermal feedback effects.

The effect of an oscillating comparator on the A/D conversion is: as the analog input approaches the edge of a quantization level, the codes become indecisive and in fact, exhibit

non-monotonic behavior. For example, one can raise the analog input voltage sufficiently to increase the code by 1 LSB, and then find that, for a slight further increase in analog input, the code goes back to the original digital output. This often-troublesome behavior can be cured in a rather surprising way – elimination by “size.” If the comparator gain is *increased*, such that the window size is reduced to a very small fraction of the total LSB weight, then the region of each code over which the oscillation occurs is reduced to an infinitesimal amount, approaching a magnitude comparable to that of the circuit background noise.

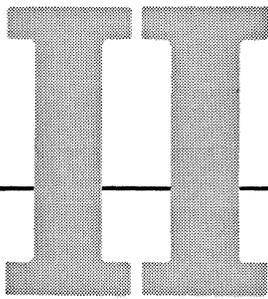
OTHER CONSIDERATIONS IN A/D CONVERTER DESIGN

The additional error sources that occur when a D/A converter is used in A/D conversion are primarily centered around the comparator’s input and gain characteristics. In particular, offset drift and input bias-current drift are important in the selection of a comparator. Further errors are introduced by extraneous noise pickup in the analog sections due to fast-rising and -changing edges of nearby digital logic.

Hence it is most important that much consideration and effort be given to adequate separation between digital and analog components in the circuit layout. Once again, the digital power supply should be kept entirely separate from the analog power supply, the analog input signals, and the D/A output section. This separation should be physical as well as electrical. One should take great care to minimize the *number* of digital signals that must be brought into or near the analog sections.

Another aspect that can spell trouble if not anticipated is the adequacy and use of the conversion time. Two factors place lower limits on this to a significant degree: one is the settling time of the D/A output, the other the switching time of the comparator.

Since the D/A output is driving the comparator towards its new value, the switching times of both elements are accumulated, but not in purely additive fashion. A useful trick is to use the fact that the most-significant bits take much longer to settle to their final values than do the LSB steps of a successive-approximations converter. Hence, to speed the overall conversion time one can use a frequency-modulated clock having decreasing period as the conversion progresses.



Testing Converters

Chapter II-4

INTRODUCTION

The methods and test-fixture configurations used to test DAC's and ADC's are influenced by a number of factors relating to converter applications, nature and speed of tests to be performed, and skill of test personnel involved. The relative importance of various converter performance specifications is dependent on each particular application, and the converter user is naturally interested in testing those parameters which significantly influence his system performance to a greater extent than those which have little effect on this performance. Two typical applications illustrate how usage influences the relative importance of various performance parameters:

Differential linearity, fast settling time, and small switching transient (glitch) amplitude are generally of great concern when DAC's are used as cathode-ray tube vector generators, since display quality is critically dependent on these parameters. Small absolute-calibration errors or zero drift are generally of little consequence, since they cause only small display size and position shifts, which can be corrected easily by operator display adjustments.

By contrast, a DAC used as a programmable stimulus generator in an automatic checkout system might require good absolute calibration and zero-stability, while not requiring fast dynamic response, transient-free switching, or exceptional differential linearity. Converter test-circuit configuration and degree of automation is influenced by: the purpose of the test; e.g., engineering performance evaluation, incoming inspection, functional checks only, etc; its versatility; measurement speed; data-reduction and display capability; and skill level required for its operation. Simple test fixtures designed to test relatively few converter parameters can be implemented easily and inexpensively. These generally must be operated by relatively skilled persons, and test data obtained usually must be reduced to extract meaningful performance information.

Versatile automatic testers are of necessity complex and are generally costly. A general-purpose automatic tester generally performs tests faster, and can be operated by less-skilled personnel, however. High-resolution converters have a potentially large number of data points which must be examined to extract meaningful converter performance information. A 12-bit DAC or ADC, for example, has 2^{12} , or 4096 possible input/output combinations. Fortunately, by knowing the type of converter errors, or deviations from ideal performance, that are commonly encountered, one can devise tests which permit useful performance data to be gained by investigating significantly fewer than the 2^n possible input/output combinations associated with an n-bit converter.

Converter performance parameters that are generally of importance are: calibration accuracy (both absolute and relative to full-scale), linearity (both cumulative and differential), offset, noise, conversion time, and, in the case of DAC's output-switching-transient amplitude-time product. Also of concern are stability of these parameters with variations in time and temperature. The purpose of this chapter is to illustrate common converter errors and deviations from ideal performance, and to outline test schemes, for evaluating converter performance, that can be adapted to both manual and automatic testing.

LINEARITY

D/A CONVERTERS

The analog output of the n-bit DAC shown in Fig. 1a is related to its input binary number in the following manner:

$$E_o = E_{NFS} (B_1 2^{-1} + B_2 2^{-2} + B_3 2^{-3} + \dots + B_n 2^{-n}) \quad (1)$$

where the digits $B_1 \dots B_n$ of the binary N each have the value 0 or 1 and E_{NFS} is the nominal full-scale output. Since

$$\sum_{i=1}^n 2^{-i} = 1 - 2^{-n}, \quad (2)$$

the relation between the output with all bits "1", and nominal full-scale output E_{NFS} is

$$E_o \Big|_{B_1, \dots, B_n = 1} = E_{NFS} (1 - 2^{-n}) \quad (3)$$

and, since $2^{-n} = 1 \text{ LSB}$, E_{FS} , the output with all bits "1" is the nominal full-scale output minus 1 LSB. That is

$$E_{FS} = E_{NFS} [1 - \text{LSB}] \quad (4)$$

The analog values associated with each of the bits acting individually can be found by setting the desired bit B_i to logic "1" and all other bits to "0". Then

$$E_o \Big|_{B_i} = E_{NFS} 2^{-i} \quad (5)$$

Relation (1) indicates a linear relationship between analog output and digital input. It follows that the sum of the analog output values obtained for any combination of bits acting individually should equal the analog output obtained when all bits of this combination are applied simultaneously. This forms the basis for a simple and effective linearity test: Various combinations of bits are turned on and the associated analog output noted. Each bit of this combination is then applied independently and its output recorded. The algebraic sum of these outputs is then compared to that obtained for all bits of the chosen combination turned on together. The difference is the linearity, or summation, error.

With most converters, the maximum linearity error occurs at full-scale. In this case, "all bits on" is the worst-case bit combination.

Converter linearity errors are independent of scale-factor calibration or gain errors. Accurate linearity measurements can be made, even on an uncalibrated DAC. The nonlinearity of the measurement device must be significantly less than that being measured. A 12-bit DAC having a nonlinearity of the order of $\pm 1/2 \text{ LSB}$ (= 1 part in 8192) requires a 5-digit DVM for meaningful linearity measurements in the circuit of Figure 1a. In addition, one should note that a zero error (non-zero output for zero input) must be corrected, so as not to introduce an error in the linearity measurement, since it is added once for each output reading taken. Consider the inequality,

$$E_o (B_1 + B_2 + \dots + B_n) + \epsilon_{LIN} + \epsilon_Z \neq E_o B_1 + E_o B_2 + \dots + E_o B_n + n\epsilon_Z \quad (6)$$

where ϵ_{LIN} is the full-scale linearity error and ϵ_Z is the zero error. The left side of inequality (6) has the zero error added once (all bits on), while the right side has the zero error added n times (n individual readings). Converters using a half-scale offset to accomplish bipolar operation (e.g., offset-binary coding) must be tested for linearity (by this method) in the unipolar operating mode (half-scale offset disconnected) to prevent large errors similar in nature to those indicated by relation (6), but greater in magnitude. When making linearity (or gain) measurements, there is less possibility for computational error if the zero error is recorded and subtracted from each subsequent bit reading before any linearity or gain calculations are made. The simplest way to correct for zero (computationally, at least) is to electrically zero the converter before data are taken.

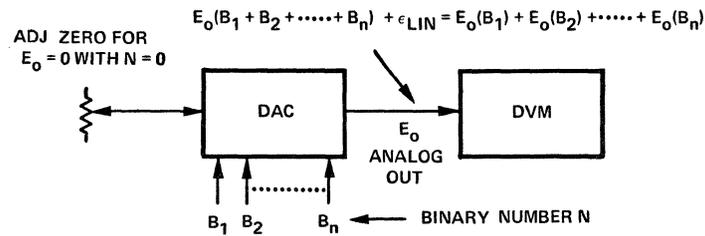
A/D CONVERTERS

The process of ascertaining linearity of an ADC is similar to that described above for a DAC. Consider the ADC of Fig. 1b, having its output binary number N related to its input analog signal E_{IN} in the following manner:

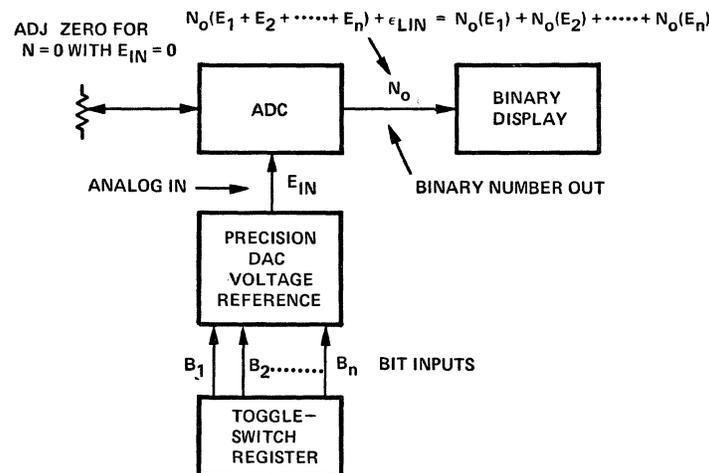
$$E_{NFS} (B_1 2^{-1} + B_2 2^{-2} + B_3 2^{-3} + \dots + B_n 2^{-n}) = E_{IN} \pm \frac{1}{2} \text{ LSB}^* \quad (7)$$

where the definitions associated with relation (1) apply. The analog input E_{IN} required to turn each bit on can be found by setting each bit except the desired one to zero in the relation (7). That is,

$$E_{IN}|_N = B_i 2^{-i} = E_{NFS} 2^{-i} \quad (8)$$



(a) D/A converter test.



(b) A/D converter test.

Figure 1. Linearity (summation) test.

*Quantizing uncertainty

ADC linearity can be evaluated by applying each of the analog input values required to turn on only one bit of a particular bit combination to be examined for linearity. The sum of these analog inputs, when applied to the ADC input, should turn on all bits of the selected combination, and no others.

The most convenient method of generating binary-scaled analog reference values, with which to test ADC's for gain calibration or linearity, is by means of a precision reference DAC and associated toggle-switch register, as shown in Fig. 1b. To simplify linearity measurement, the ADC is first calibrated in the following manner: all bits of the reference DAC are turned off; this applies zero analog input to the ADC. The ADC zero control is adjusted for digital zero on the binary display. (The reference DAC and ADC are assumed to have identical scale factor so that, ideally, the ADC, when properly adjusted, will have a full-scale output for full-scale input to the toggle-switch register.) For convenience, the ADC is calibrated at half-scale. Bit 1 (MSB) of the toggle switch register is turned on, and the ADC gain control is adjusted for bit 1 on only, as viewed on the binary display.

Individual bit gains can then be checked by turning each of the toggle switch bit inputs on and off in succession and looking for correspondence on the binary display. Since linearity error is generally greatest at full-scale, nonlinearity can be checked quite easily, assuming that the individual bit gains are correct, as determined by correspondence between ADC output and reference DAC input for each individual bit. Starting at the most-significant reference-DAC bit-input, each bit, in descending order, is turned on and left on. Any difference between the displayed ADC output and toggle-switch-register input codes, as full-scale is approached, is then caused by an ADC nonlinearity (assuming the nonlinearity of the reference DAC to be negligible).

The methods described above for ADC calibration and linearity testing tacitly assume that the ADC can be calibrated so that each analog calibration value is centered in the respective quantization band corresponding to the desired output code. Methods for accomplishing this are described in the section on ADC testing.

GAIN CALIBRATION

Converter accuracy can be specified in two ways: (a) absolute and (b) relative to full-scale. In testing for (a), one is concerned with ascertaining the calibration of any bit or combination thereof with respect to some absolute external standard. In testing for (b), one is concerned only with ascertaining calibration accuracy relative to the converter's full-scale value. Since, in most instances, the converter's internal calibration reference consists of a temperature-compensated zener reference diode, which might age at the rate of 0.01%/1000h operation, one usually accepts the fact that high-accuracy converters require periodic recalibration to maintain rated absolute calibration accuracy.

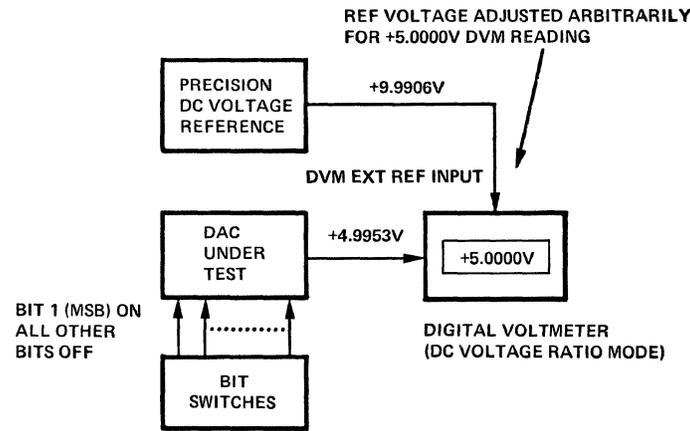
Testing for converter accuracy relative to full-scale is generally of greater interest, since this tests the stability and ratio-accuracy of the converter's precision weighting network and active switching elements; weighting-network ratio adjustments are normally not provided on contemporary modular converters (whereas full-scale adjustment is, because of the realities mentioned above). The evaluation of converter gain accuracy can be expedited by normalizing gain to some convenient reference value. In the case of converters having *zero* and *gain* adjustments, this is simply accomplished by calibrating zero and full-scale before recording the various bit (or combination of bits) readings. The evaluation of gain accuracy relative to full-scale for units having no external calibration adjustments can be expedited by normalizing gain prior to recording the data.

Two methods for accomplishing gain normalization external to the DAC under test are shown in Figs. 2a and 2b. In both figures, it is assumed that the relative accuracy of the individual bit gains and the linearity of the converter are to be tested.

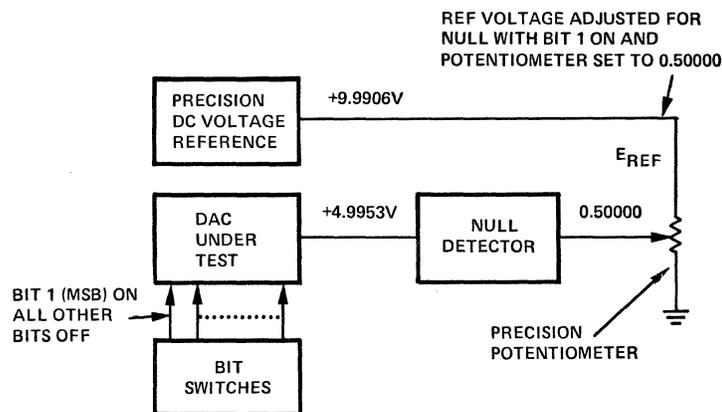
In Figure 2a, a DVM, operated in the ratio mode, is used to read the DAC output. The DAC zero output is first adjusted (all bits off). Bit 1 is then turned on. The value of a stable dc

precision reference standard applied to the DVM ratio reference input is adjusted to make the DVM read +5.0000V (nominal full-scale assumed to be +10V).

In Figure 2b, a precision potentiometer is used to measure the DAC output as a fraction of some reference voltage applied to the high side of the potentiometer. At any bit setting, the position of the potentiometer arm is varied until the pot output voltage equals that of the DAC, as indicated by a zero reading at the null detector. The measurement is first normalized at any desired DAC setting – half-scale in the example of Figure 2b – by adjusting the reference voltage for null at the corresponding potentiometer setting.



(a) DVM in ratio mode.

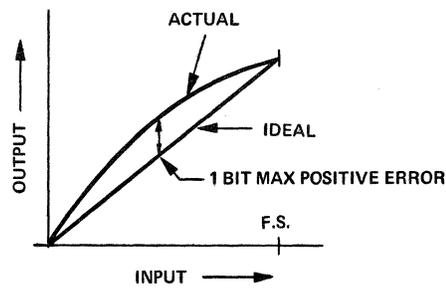


(b) Precision potentiometer & null meter.

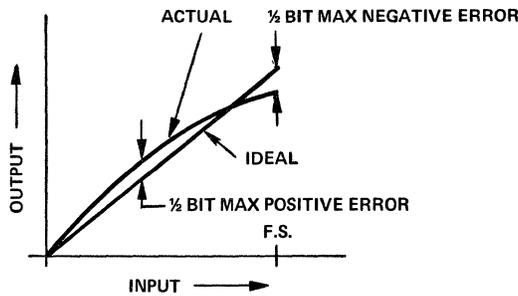
Figure 2. DAC gain normalization methods.

If the converter is nonlinear, the peak linearity error is dependent upon the point chosen for gain calibration or normalization, as illustrated in Figure 3. In Figure 3a, a peak error of 1 bit is assumed to exist at some point on the device transfer function when the unit is calibrated at full-scale. In Figure 3b, the device gain has been adjusted to minimize the peak error – in this case, to $\pm\frac{1}{2}$ bit. In practice, it is generally found that peak linearity error (deviation from a “best straight line”) will be minimized if the converter gain is calibrated at roughly $\frac{3}{4}$ scale. If the device nonlinearity is less than $\frac{1}{4}$ bit, the exact point chosen for gain calibration has little effect on device accuracy.

If this nonlinearity is greater than $\frac{1}{4}$ bit, the output point chosen for gain calibration can determine whether or not the converter meets its accuracy specification (generally $\pm\frac{1}{2}$ bit), since some differential nonlinearity (to be described shortly) must be presumed to exist in any converter. Because calibration at full-scale is straightforward and requires the most conservative linearity and relative-accuracy specification, Analog Devices does this as a standard practice in specifying converters, rather than choosing a “best straight line” approach.



(a) Gain adjusted for zero full-scale error.



(b) Gain adjusted to minimize peak error.

Figure 3. Effect of gain adjustment on linearity error for nonlinear DAC or ADC.

ZERO AND GAIN CALIBRATION

Calibration of the transfer function of a linear device requires determination of two points within the linear operating region of the device. The choice of calibration points and exact procedure depends somewhat on the nature of the particular device under test; generally, device zero is adjusted and then gain is calibrated.

UNIPOLAR DAC

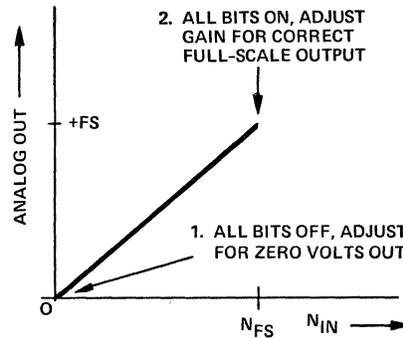
The typical calibration procedure for a unipolar DAC is illustrated in Figure 4a: all bits are turned off (binary zero), and the zero control is adjusted for zero analog output. All bits are then turned on, and the gain control is adjusted for correct full-scale output. (Gain could equally well be calibrated at either 1/2 or 3/4 scale, as discussed above. Device accuracy can then be checked by turning on and off each bit in succession and comparing each bit output with its corresponding theoretical reference value. Worst-case gain error can then be found by turning on all bits having low individual outputs in relation to their respective reference values and noting the DAC output. The process is repeated for all bits having high individual bit outputs with respect to their respective reference values. The DAC output for each of these two bit combinations, which corresponds to worst-case negative and positive gain error, respectively, is then compared to the theoretical value for each of these sums. The worst-case + or - bit-sum error should be less than the device error specification - generally $\pm 1/2$ bit at room temperature.

It should be noted that testing for worst-case calibration error in the manner described above assumes negligible nonlinearity errors. The bit combination corresponding to worst-case positive or negative gain error will not necessarily correspond to that which causes greatest nonlinearity. Nonlinearity can be checked independently of calibration as described earlier.

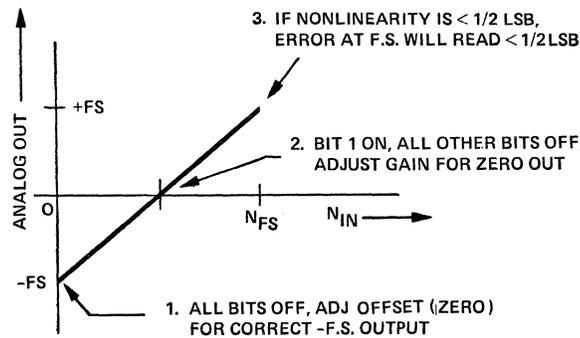
BIPOLAR DAC USING OFFSET BINARY OF 2'S COMPLEMENT (OFFSET-BINARY WITH COMPLEMENTED MSB)

DAC's or ADC's having offset binary coding (as distinguished from sign-magnitude coding) are generally made bipolar by summing with the unipolar output of the DAC weighting net-

work a fixed analog output equal in magnitude, but opposite in polarity, to the first bit (MSB) analog equivalent. This shifts the DAC unipolar transfer characteristic of Fig. 4a down by half-scale, as shown in Figure 4b. With most DAC's (or ADC's), the gain control affects only the unipolar scale factor, and not that of the bipolar offset. DAC's (or ADC's), of this type are generally calibrated in the following manner: All bits are turned off (binary zero) and the bipolar offset is adjusted for correct negative full-scale reading. Bit 1 is then turned on and the gain is adjusted for zero output. All bits can then be turned on, providing a calibration check at + full scale. (Alternatively, the gain can be calibrated at + full scale, with zero analog output providing the calibration check point.) The general calibration procedure, while described for DAC's, is quite similar for ADC's (ADC calibration is discussed under ADC testing).



(a) Binary unipolar.



(b) Offset-binary bipolar.

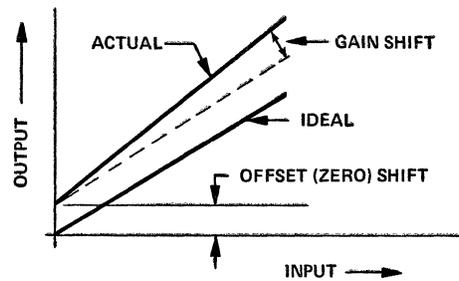
Figure 4. Typical DAC calibration procedure.

TEMPERATURE EFFECTS

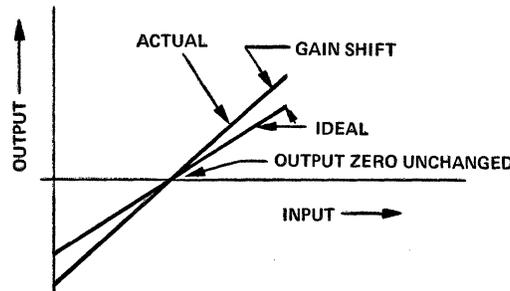
The manner in which the DAC unipolar and offset-binary bipolar DAC output can shift with temperature is illustrated in Figures 5a, 5b, and 5c. In the unipolar DAC transfer curve of Figure 5a, a zero shift moves the transfer curve up or down. Since a zero shift affects all output readings by the same amount, zero temperature coefficient is expressed either directly in $\mu\text{V}/^\circ\text{C}$, or as a fraction (% or ppm) of full-scale per $^\circ\text{C}$. A gain shift, on the other hand, causes the slope of the transfer curve to change. This affects all output readings by the same percentage. Gain temperature coefficient is therefore generally specified as % or ppm of reading/ $^\circ\text{C}$.

In the case of a bipolar DAC, if the temperature coefficient of the half-scale offset were exactly matched to that of the unipolar transfer curve, and there were no zero shift, the bipolar transfer curve would rotate about the zero output point with temperature, as shown in Figure 5b. In actual practice, this does not occur. The difference between the bipolar offset and unipolar gain temperature coefficients, plus the zero temperature-coefficient of the unipolar transfer characteristic will cause the bipolar transfer curve to shift up or down with temperature. The unipolar gain-temperature coefficient causes the bipolar transfer curve to rotate

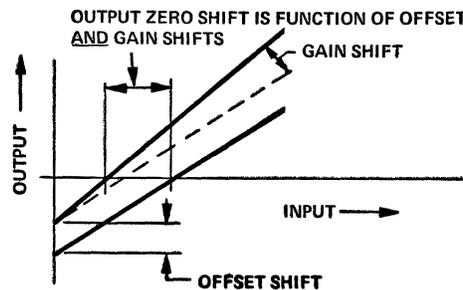
about the intersection of this curve with the output axis as shown in Figure 5c. Figure 5c illustrates that in the case of bipolar converters having offset binary coding, the shift in output zero with temperature is a function of both gain *and* offset shifts.



(a) Unipolar



(b) Bipolar (offset binary) with offset and gain TC matched.



(c) Bipolar (offset binary) with offset and gain TC's not matched

Figure 5. Effects of gain and offset shifts on DAC output.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of the variation in analog value change associated with a one-bit change in the associated digital number, for either a DAC or an ADC. Ideally, a one-bit digital value change should have associated with it a constant (i.e., 1LSB) incremental change in analog signal anywhere on the input/output transfer characteristic. Differential nonlinearity can be quantified in the following manner: Assume an analog signal span E_S , and an n -bit binary converter. A normalized 1-bit increment ΔE_N can be defined, such that

$$\Delta E_N = E_S 2^{-n}$$

Differential linearity error, ϵ_{DL} , can then be defined by the relation:

$$\epsilon_{DL} = (\Delta E - \Delta E_N) / \Delta E_N$$

where ΔE is the actual change in analog value associated with any 1-digit change in the binary number.

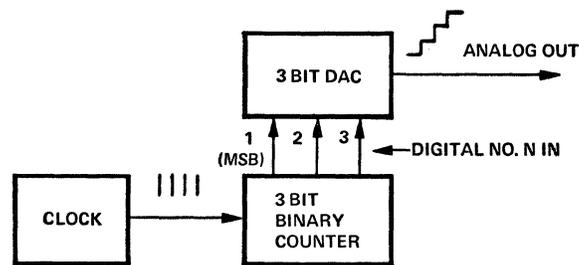
The greatest differential nonlinearity occurs at major carry transitions of the digital number, where significant weighting network gain-factor switching occurs. To illustrate, consider a 3-bit DAC, driven by a 3-bit binary counter to sequentially generate all possible 3-bit codes corresponding to the fractions 0 to 7/8 of full-scale, as shown in Figure 6a. Ideally, this

should produce a staircase output waveform having equal step heights. If the weight of the MSB (Bit 1) is $\frac{1}{2}$ -bit low, the output transition from code 011 ($\frac{3}{8}$) to 100 ($\frac{4}{8}$) will be $\frac{1}{2}$ -bit too small. All succeeding code transitions will have correct amplitude, but the output values associated with each of the codes $\frac{5}{8}$. . . $\frac{7}{8}$ will be $\frac{1}{2}$ -bit low in terms of absolute calibration. In this case, a $\frac{1}{2}$ -bit differential linearity error occurs at the major-carry code transition, shown in Figure 6b.

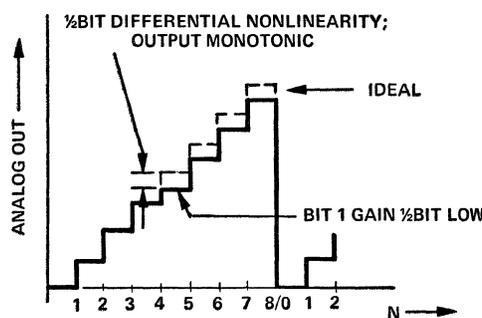
MONOTONICITY

A monotonic output is one that either increases or remains constant, for increasing input, so that the output will always be a single-valued function of input. (Mathematically, this requires that the 1st derivative of a continuous output-input transfer function be ≥ 0 ; for a variable having discrete steps, the first *difference* must be ≥ 0 .) Assume in the example of Figure 6a that the DAC has a bit 1 weight more than one bit low in relation to the weights of bit 2 and bit 3. In this case, the code transition from step 3 to step 4 will actually be *negative*, as shown in Figure 6c, a non-monotonic response. It should be noted that a converter specification of $\pm\frac{1}{2}$ -bit differential nonlinearity is more stringent than one of guaranteed monotonicity, since non-monotonicity implies a differential nonlinearity greater than 1 bit.

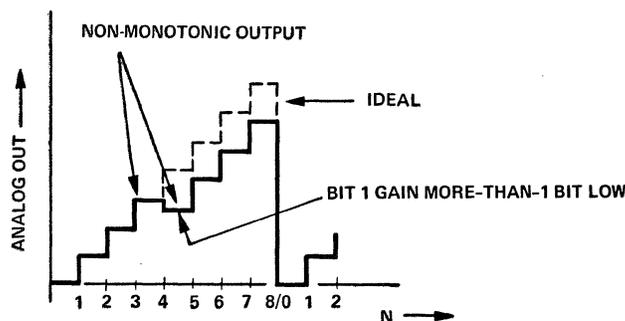
Normal device nonlinearity, as shown in Figure 3, has negligible effect on differential nonlinearity. To illustrate, consider a 10-bit converter having a $\pm\frac{1}{2}$ -bit nonlinearity. If this nonlinearity is assumed uniformly distributed over the full range of $2^{10} = 1024$ bits, the differential nonlinearity contributed at any code transition by this $\pm\frac{1}{2}$ -bit linearity error is no greater than $1/2048$ bit.



(a) DAC driven by counter.



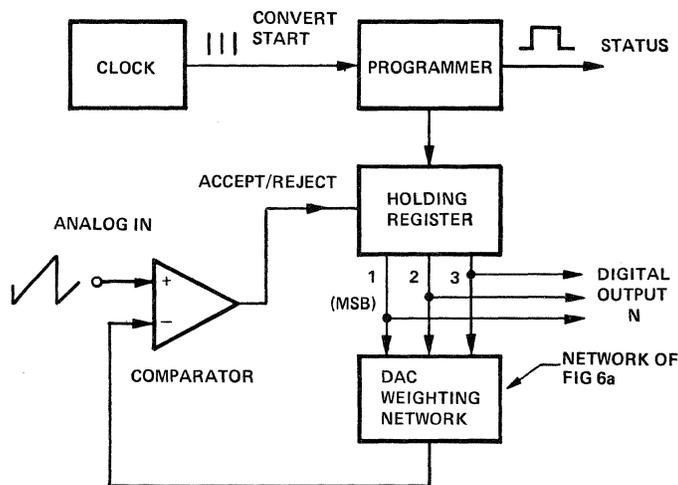
(b) Differential nonlinearity error.



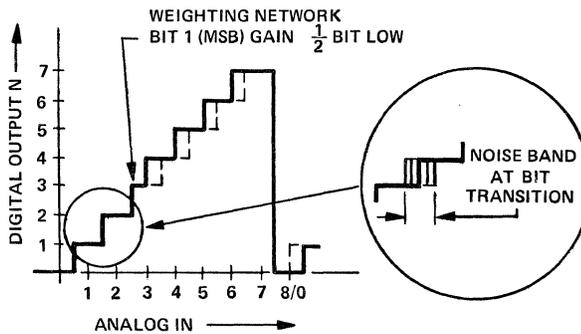
(c) Non-monotonicity.

Figure 6. DAC differential linearity and monotonicity errors.

The effect of switch and weighting-network differential nonlinearity on the digital output of a successive-approximation ADC is illustrated in Figure 7. Figure 7 shows a 3-bit successive-approximation ADC configuration using the DAC of Figure 6a as its weighting network. The analog ramp input to this converter is assumed to be slowly-varying with respect to the conversion rate, so that each point on the analog waveform is successively digitized within the $\pm 1/2$ -bit quantization-error limits inherent in the A/D conversion process. The converter's ideal output is a sequence of codes corresponding to the binary numbers 000 through 111 (0-7), with each code corresponding to the ideal analog value. If bit 1 (MSB) of the weighting network has a weight $1/2$ bit low with respect to those of bits 2 and 3, as in the example of Figure 6, the digital output will jump to the code 100 (4) $1/2$ -bit sooner than it should. The effect on the output is to cause a narrowing of the step width corresponding to the code 011 (3) immediately preceding the code 100 when bit 1 turns on and bits 2&3 turn off, as shown in Figure 7b. Conversely, if the weighting network has its bit-1 gain $1/2$ -bit high with respect to bit-2 and bit-3 gains, the width corresponding to the code 011 (3) will be $1/2$ -bit too large. In both cases, the widths corresponding to output levels 4-7 will have a correct 1-bit amplitude.



(a) Successive-approximation ADC.



(b) Digital output.

Figure 7. Effects of noise and weighting network differential nonlinearity on ADC output.

The waveform inset of Figure 7b illustrates that noise in the analog input to the converter circuit introduces an uncertainty in the analog code transition value. (The noise band associated with each code transition value can be found using an ac dither signal, as will be described in the section on ADC testing.)

If the bit-1 gain of the weighting network is more than 1 bit low, as in the DAC output waveform of Figure 6b, the code 011 will not occur and the digital output will skip from 010 (2) to 100 (4), i.e., a non-monotonic weighting network causes missing ADC output codes. A comparison of the waveforms of Figures 6b and 7b shows that a differential non-

linearity causes a variation in the output step *height* for the case of a DAC transfer function, and causes a variation in output step *width* for the case of an ADC transfer function.

DAC TESTING

A simple and effective DAC test configuration is shown in Figure 8. The digital inputs to both the device under the test (DUT) and a highly accurate reference DAC are driven in parallel from either a toggle-switch register or a dynamic programmer. Both the reference DAC and DUT have the same output range. The output of the reference DAC is compared to that of the DUT. The difference between the two outputs is amplified in an error amplifier, which has its gain calibrated to provide a defined error output with some convenient volts-per-bit scale factor. The toggle-switch register permits selection of logic 0, logic 1, or "dynamic program" for each input bit. This permits entry of any desired code for static-accuracy tests, or dynamic programming for high-speed dynamic testing. Gain and zero adjustment can be provided in the reference DAC to effect gain normalization and zero calibration in the event the DUT has no provision for internal gain or zero calibration.

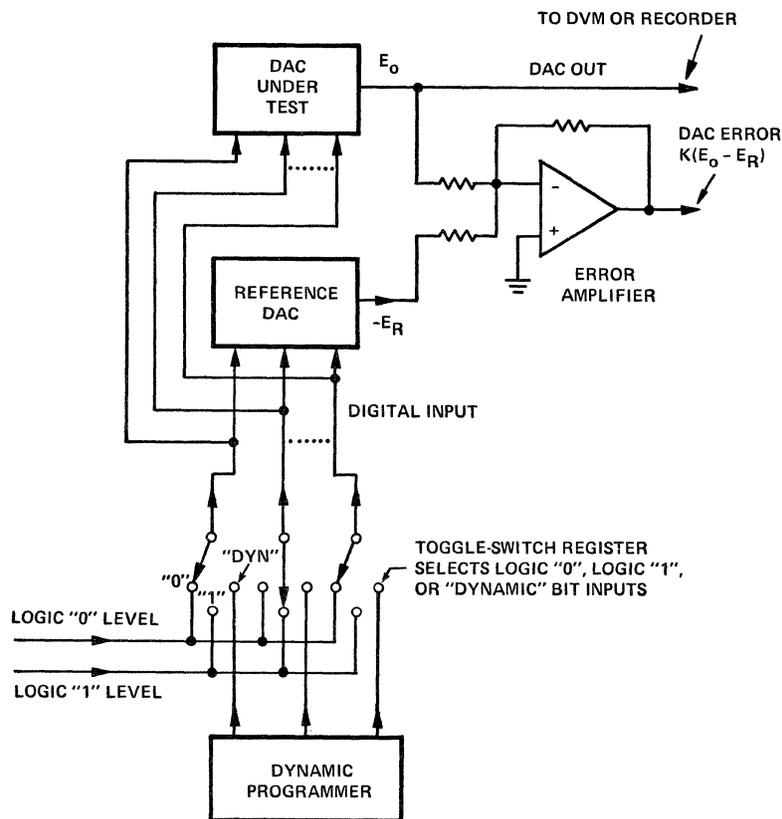


Figure 8. Basic DAC tester.

DYNAMIC PROGRAMMING

There are two dynamic programming modes that are of particular value in permitting the linearity and accuracy characteristics of the DUT to be assessed quickly; they are the *bit-scan* and *count* modes.

Bit-Scan Mode

In the "bit-scan" mode, the individual bit inputs to both the DUT and the reference DAC are time-division multiplexed, so that each bit input is turned on and off in succession. Two additional multiplexed time slots are allocated to full-scale (all bits on) and zero (all bits off) to facilitate device calibration. A bit-scan dynamic programming configuration is illustrated in Figure 9. The resulting bar graph of output error can be displayed on an oscilloscope or a high-speed strip-chart recorder (if a permanent record is desired). Figure 10a shows a typical commutator time-slot allocation for testing a 12-bit DAC in the bit-scan mode.

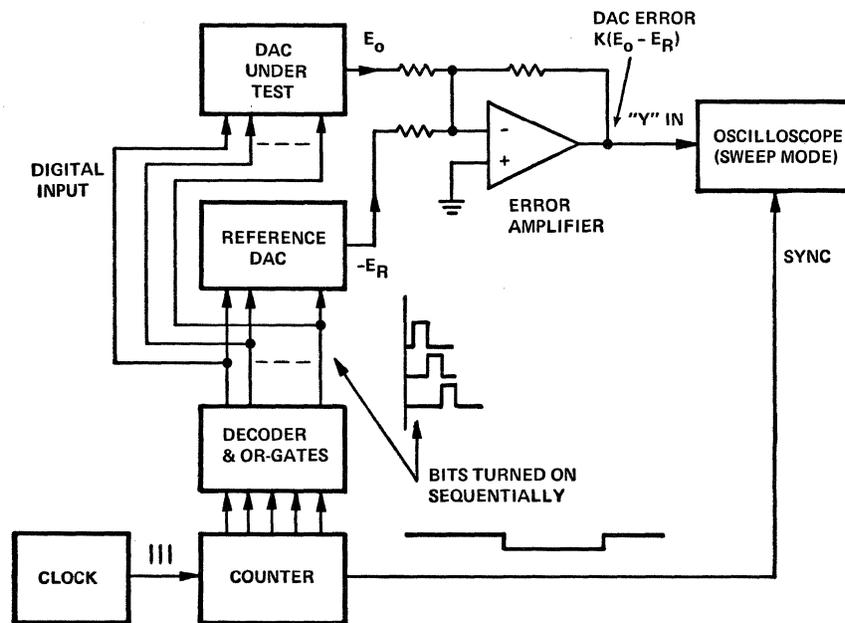
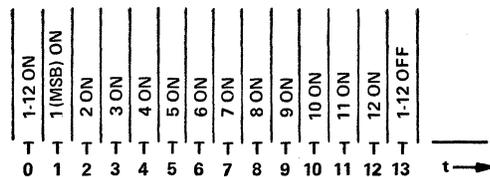


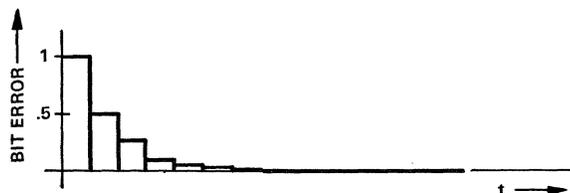
Figure 9. DAC dynamic test – BIT-SCAN mode.

Typical error displays resulting from this test are shown in Figures 10b, c, and d. Figure 10b illustrates an error display for a DAC having the correct binary scaling weights for all bits, but full-scale gain calibration 1-bit high. Since a 1 LSB full-scale gain error (with correct relative scaling) causes the bit 1 error to be 1/2-bit high, bit 2 to be 1/4-bit high, bit 3 1/8-bit high, etc., the error display is exponential in shape, in this case. Figure 10c illustrates the error display for the case of a +1/4-bit offset error, combined with a -1-bit full-scale gain error, assuming perfect relative weighting (i.e., differential linearity). This causes a reversal in full-scale error polarity from that shown in Figure 10b. In addition, the +1/4-bit offset (zero) error shifts the complete display +1/4 bit from the zero baseline. The DUT is calibrated in the following manner, using the bit scan display: Zero is adjusted to bring the bar representing the zero error (time slot T13 in Figure 10a) to the display baseline. The gain is then adjusted to bring the bar corresponding to full-scale (time slot T0) to the baseline. Zero and full-scale of the DUT are now calibrated. (If the DUT does not have zero or full-scale adjustments, zero and full-scale of the reference DAC can be adjusted instead, to normalize the display.)

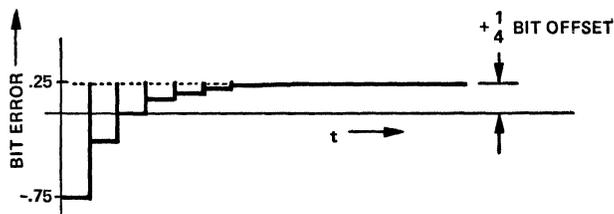
A typical “bit-scan error” display after zero and full-scale of the DUT (or reference DAC) have been calibrated, is shown in Figure 10d. If the DUT is perfectly linear, the sum of all positive bit errors should equal the sum of all negative bit errors after zero and full-scale calibration; any residual error is caused by device nonlinearity.



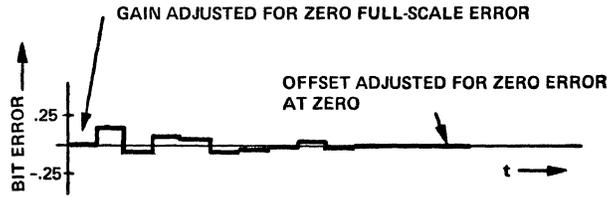
(a) Commutator time-slot allocation.



(b) DAC full-scale gain, 1-Bit high and zero offset.



(c) DAC full-scale gain, 1-Bit low and 1/4-bit offset.



(d) Typical bit error distribution.

Figure 10. 12-bit DAC dynamic test waveforms, bit-scan mode.

COUNT MODE (FIGURE 11)

In the dynamic-programming “count” mode, the digital inputs to both the reference DAC and DUT are driven from a counter so that all possible DAC input code combinations are sequentially generated. This produces a staircase output waveform from the DUT and the reference DAC. Zero and full-scale are most conveniently calibrated in the bit scan mode, as described above. After this calibration has been completed, the error display in the “count” mode is ideally a straight line. Using this testing technique, combined with a high-speed recording oscillograph, and a count rate of 1ms/step, all codes can be generated and a permanent error record obtained in approximately 4 seconds for a 12-bit DAC, and 64 seconds for a 16-bit DAC.

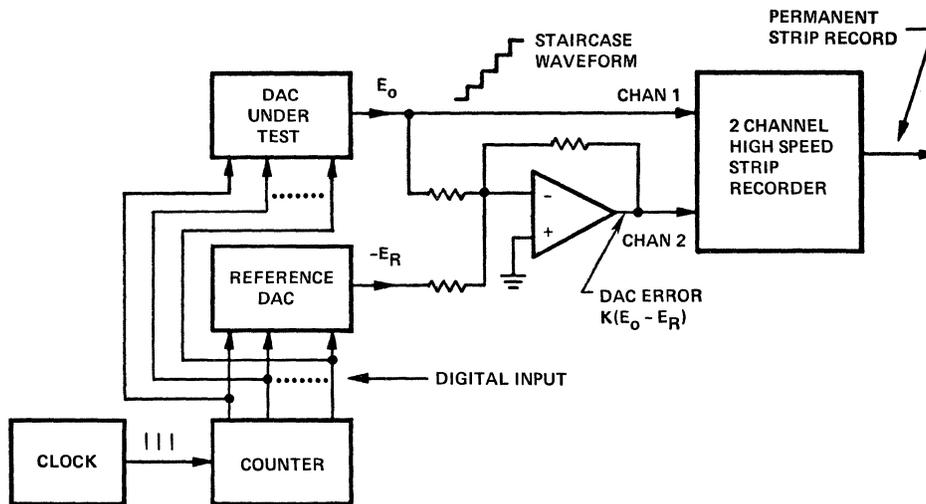
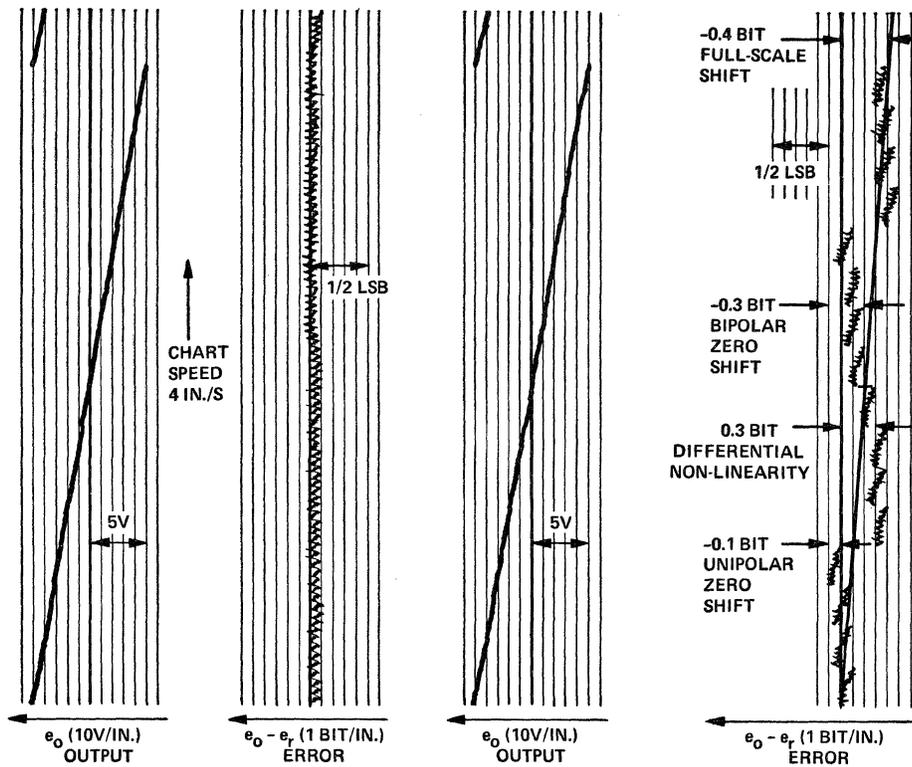


Figure 11. DAC dynamic test – COUNT mode.

COUNT-MODE ERROR RECORD EXAMPLE

The usefulness of the error record obtained in the *count* mode as a means of quickly assessing DAC performance at various temperatures is shown by the error records in Figures 12a and 12b, obtained from an ADI Model DAC-10Z-2 10-bit $\pm 5V$ bipolar D/A converter, tested at 25°C and 70°C, respectively. In these figures, the output e_o of the DUT is recorded directly on another oscillograph channel, to provide a scale reference. A line is drawn through the error-sweep waveform between zero and full-scale.



(a) DAC-10Z-2 @ +25°C.

(b) DAC-10Z-2 @ +70°C.

Figure 12. DAC tester output waveform-COUNT mode typical chart recording.

The slope of this line represents the gain error of the DUT. Deviations from this straight line are caused by linearity and differential-linearity errors. Differential nonlinearity is measured by the peak-to-peak amplitude of the abrupt transition in the error curve occurring at the major-carry transitions of the digital-input code to the DUT. This is a measure of the difference in analog increment corresponding to a change of 1 LSB in the input digital code.

As can be seen from the error record of Figure 12a, the DUT has gain, offset, differential linearity, and linearity errors less than 0.1 bit at +25°C. The error waveform of Figure 12b shows that, at +70°C ambient temperature, full-scale and bipolar zero outputs have shifted -0.4 bit and -0.3 bit from their respective values at 25°C. At 70°C, the differential nonlinearity is 0.3 bits; the nonlinearity (deviation from the straight line joining the digital zero and full-scale analog values) is approximately half the differential nonlinearity, or 0.15 bit. Since 1 LSB, for a 10-bit DAC, is 1/1024 of FS (or 977ppm), the average gain and zero TC's in the range 25°C to 70°C are $0.4 \times 977\text{ppm}/45^\circ\text{C} = 8.7\text{ppm}/^\circ\text{C}$ and $0.3 \times 977\text{ppm}/45^\circ\text{C} = 6.5\text{ppm}/^\circ\text{C}$. The unipolar zero (all bits off) has shifted - 0.1 bit, while the bipolar zero (digital half scale) has shifted - 0.3 bit at 70°C, corresponding to average unipolar and bipolar zero TC's of 2.2 and 6.5ppm/°C, respectively, in the temperature range 25°C to 70°C.

The error records of Figure 12 illustrate the important point that device differential nonlinearity is almost independent of the gain calibration points. That is, choosing a "best straight line" through the DAC output/input transfer curve to minimize gain or linearity error will have negligible effect on the differential linearity of the device, since the differential nonlinearity is the *peak-to-peak* error occurring at the 1-bit code changes associated with major carries in the input digital number.

DIFFERENTIAL LINEARITY TESTER

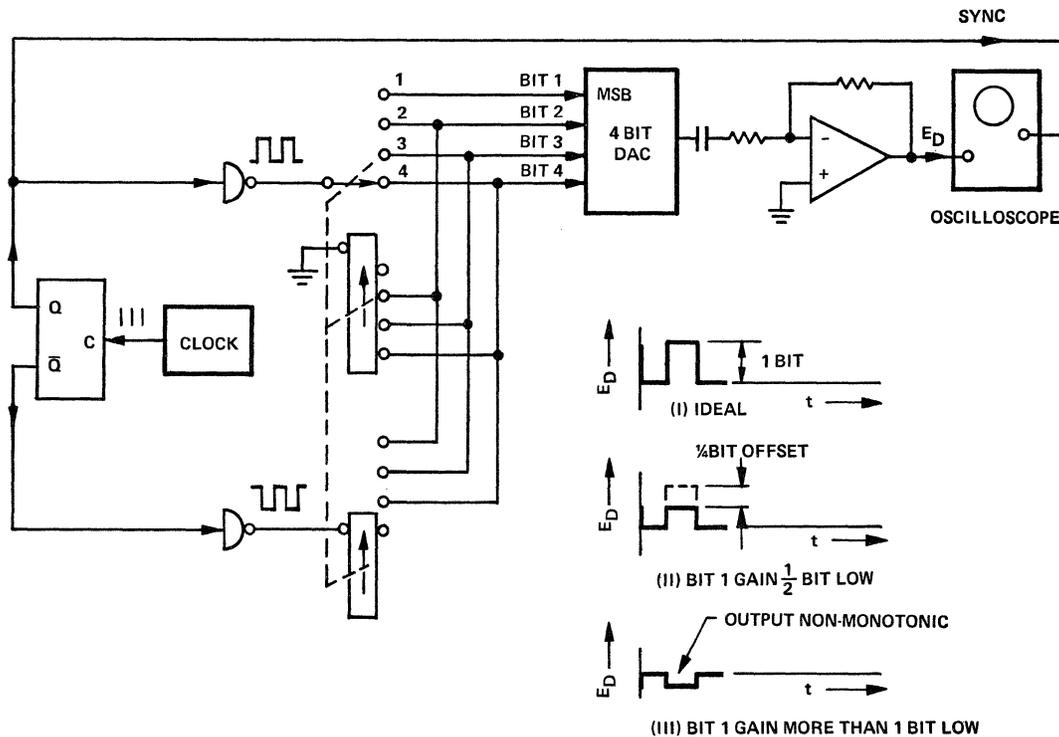
A simple scheme for testing DAC differential linearity is shown in Fig. 13a, for the case of a 4-bit DAC (for simplicity). A three-selection ganged switch is wired to the DAC bit inputs so that the bit codes at either side of each carry-transition are examined by means of two out-

of-phase square-waves applied to the two switch input lines. The carry transitions examined in each switch position are tabulated in Table 1 below.

Switch position	1	2	3	4
Code transition	1000	0100	0010	0001
	0111	0011	0001	0000

Table 1. 4-bit DAC code transitions for differential linearity test

Ideally, the ac component of DAC output for each switch position is a square-wave having 1 LSB amplitude. Waveforms for several differential linearity possibilities are shown in Figure 13b. It should be noted that this test configuration tests differential linearity at major carry transitions only up to half-scale. This is generally sufficient to accurately characterize the differential linearity behavior of the device, since, unless the device is markedly non-linear, the differential nonlinearity pattern associated with bit-2-bit-4 code transitions will repeat itself in the range from half-scale to full-scale output.



(a) Circuit diagram.

(b) Waveforms at half-scale.

Figure 13. Simple DAC differential linearity tester.

Offset Method of Differential Nonlinearity Measurement

An alternate technique to that shown in Figure 13 for measurement of differential nonlinearity is shown in Fig. 14. The reference number, N_R , corresponding to the code of interest is applied to the DUT through the toggle-switch register. A digital subtractor subtracts 1 digit from this reference number so that $N_R - 1$ is applied to the input of a highly-accurate reference DAC. The difference between the output of the DUT and the reference DAC is amplified and displayed on an error indicator. Ideally, this indicator should display a constant 1-bit difference for any number, N_R , applied to the input of the DUT. Differential nonlinearity at each bit code transition is tested merely by turning each individual bit switch in the toggle-switch register on and off in succession. For example, at the major carry, $N_R = 10000.0$, and $N_R - 1 = 01111.1$. Differential nonlinearity is measured as the deviation from the ideal 1-bit step.

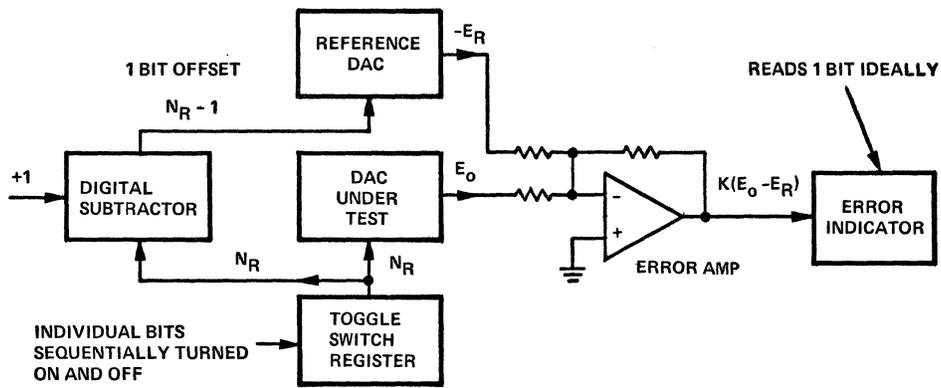


Figure 14. Offsetting digital input to DAC under test to check differential linearity at major carry transitions.

DIGITAL DITHER GENERATOR

Frequently, the evaluation of DAC dynamic response characteristics relating to differential linearity, settling time, and switching transient (glitch) amplitude can be expedited if the DAC output can be periodically cycled through a few counts either side of each specific input code transition of interest so that the DAC output can be observed with an oscilloscope as that particular code transition is repetitively traversed from each direction. Two methods for accomplishing this are now described.

Open-Loop Digital Dither Generation

An open-loop scheme for generating a digital dither signal is shown in Figure 15. An up/down counter is preset to the reference number N_R corresponding to the code of interest. A divide-by-four binary counter and count-direction control flip-flop are driven from the clock so that groups of 4 clock pulses are counted in the up and down directions alternately, so that there is no net change in the counter state at the completion of an 8-count up-down cycle. The up/down counter is preset to N_R in the middle of each burst of up and down pulses. This redundant input forces the up/down counter into the correct reference state twice per cycle, thus preventing this counter from becoming inadvertently offset from the desired reference state N_R by spurious noise pulses.

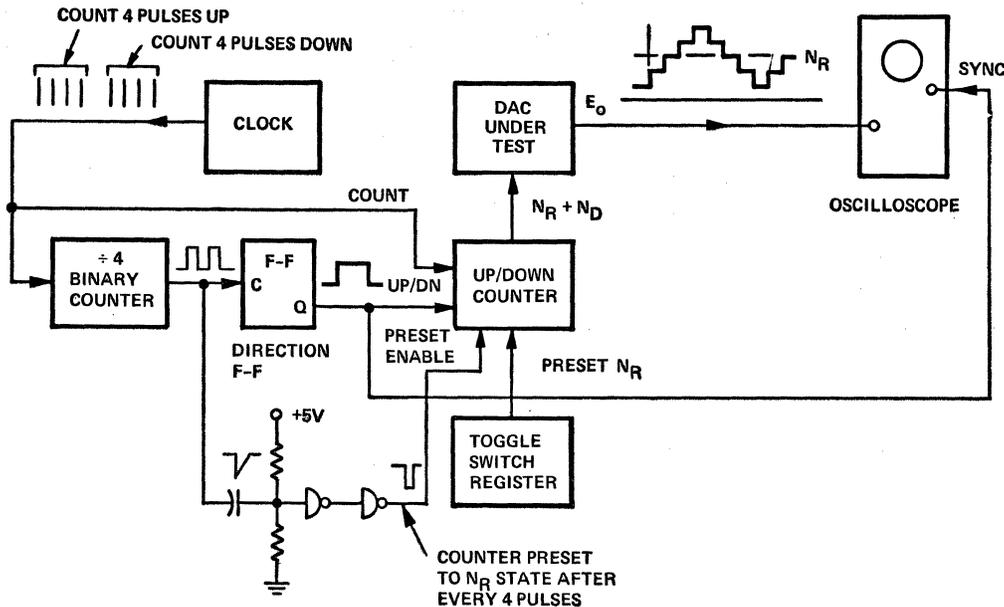


Figure 15. Digital dither generation for DAC differential-linearity dynamic testing.

Alternatively, by incorporating independent digital high and low limit comparators, the count direction of the up/down counter can be reversed each time the high or the low limit is reached, rather than after a defined number of pulses has been counted in each direction,

as in the scheme of Figure 15. This variation of the scheme permits independent control of digital dither amplitude as well as the reference code through the application of programmed high and low limits.

Closed-loop Dither Generation

A closed-loop digital dither generation scheme is shown in Figure 16. In this scheme, the reference number, N_R , corresponding to the code of interest is applied to the digital input of a reference DAC. A digital accumulator configured as a 1-bit adder/subtractor generates the digital dither, causing the code applied to the DUT to oscillate about the reference number N_R . This is accomplished in the following manner: At each "add" time the digital number stored in the accumulator is incremented 1 bit, either up or down, depending on the state of the add/subtract *enable* line. The output of the DUT is compared to that of the reference DAC, which has N_R as its input. The difference in these two outputs is amplified and applied to the input of a Schmitt trigger. The output of this Schmitt trigger drives the add/subtract *enable* line of the digital accumulator. A cycle of operation is as follows: The analog error increases at each "add" time until the output of the error amplifier exceeds the Schmitt trigger hysteresis-threshold reference level. This causes the Schmitt trigger to change state, causing the accumulator to increment in the opposite direction until the analog error exceeds the new threshold level of the Schmitt trigger, at which point the add/subtract *enable* line again changes state, causing the accumulator to increment in the original direction. Dither amplitude can be controlled by varying the gain of the error amplifier to control the number of increments required to overcome the Schmitt trigger hysteresis level. Sufficient filtering must be provided to avoid triggering the Schmitt trigger by transient spikes (glitches).

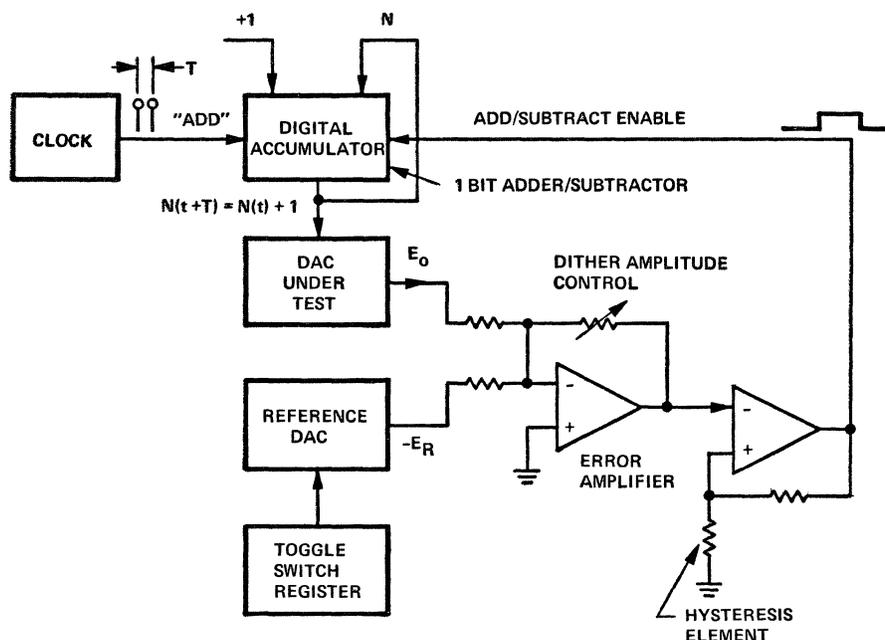


Figure 16. Closed-loop digital dither generation.

DAC SETTling-TIME MEASUREMENT

DAC settling time is a parameter of importance in high-speed applications. Settling time is defined as the time required for the output to approach a final value within the limits of a defined error band, for a step change in input. This fixed error band is generally expressed as a fraction of full scale, typically $\pm\frac{1}{2}$ -bit. If the device step response is oscillatory, so that the output swings through the defined error band before entering it for the final time, the above definition tacitly implies that settling time is measured as the time required for the output to enter the defined error band for the *final* time. The above settling time definition implies that the greater the output step change, the longer the settling time (a 1-bit output step

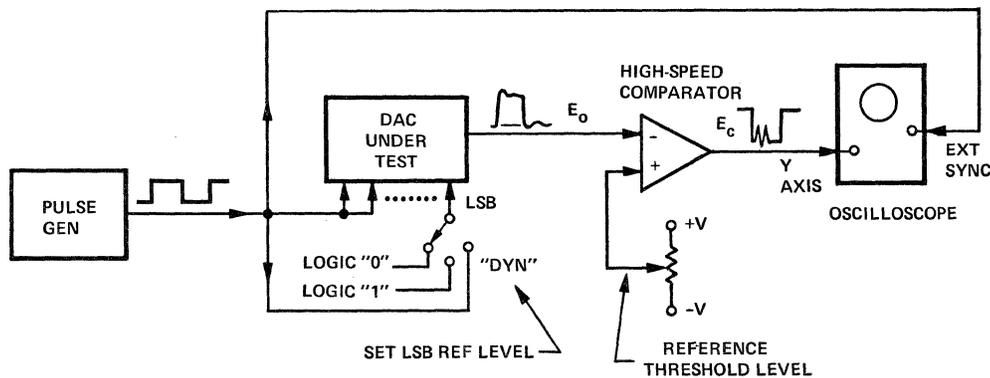
change, for example, will be within $\pm\frac{1}{2}$ bit of final value when this change has reached only 50% of its final value).

In addition to the usual constraints imposed on settling time by normal closed-loop linear bandwidth considerations, large output changes are generally slew-rate limited. There are two settling times of interest, depending on the application. These are *full-scale* and *bit-to-bit tracking*, depending on whether successive digital inputs are sequential or completely random in nature.

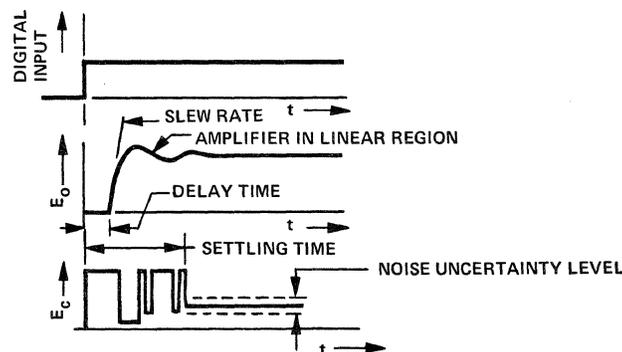
The accurate measurement of settling time for a high-resolution, high-speed DAC is fraught with practical difficulties. Measurement instrument bandwidth and thermal unbalance effects, coupled with the unavoidable presence of noise, can introduce significant measurement uncertainties when high-speed settling times to within error bands of the order of the order of 0.01% of final value are being measured.

Zero and Full-Scale

The general test configuration for measuring full-scale settling time is shown in Figure 17a. All digital input lines except that driving the LSB are connected together and driven with a square-wave having fast rise and fall times with respect to the response times being measured. The LSB DAC input line is connected to a three-position switch so that logic "0", logic "1", or "dynamic" input (consisting of the square-wave drive applied to the other bits) can be selected. When this switch is in the "dynamic" position, the DAC output is driven alternately between zero and full-scale. The DAC output is compared to a threshold reference level at the input to a high-speed comparator so that the comparator output will change state when the DAC output E_o exceeds the threshold reference level E_R . The comparator output is displayed on an oscilloscope having its sweep start synchronized to the square-wave applied to the DAC's digital input. Choice of logic "0", logic "1", or "dynamic" for the LSB DAC digital input facilitates setting the comparator threshold reference level to within $\frac{1}{2}$ -LSB of the DAC full-scale output.



(a. Measuring circuits)



(b. Waveforms)

Figure 17. DAC zero and full-scale settling-time measurement.

Full-scale settling time measurement is made in the following manner: The comparator threshold reference level is adjusted to bias the comparator output corresponding to DAC full-scale digital input into its linear operating region with the LSB set to “dynamic.” This line is then switched to logic “0”, reducing the full-scale DAC output level by 1 bit. This, in turn, causes the comparator output corresponding to full-scale DAC output to shift by the equivalent of 1 LSB. In the case of high-resolution DAC’s having small LSB analog equivalent values, the comparator output will still remain in its linear region. This procedure establishes a calibrated 1-LSB band on the oscilloscope tube face, independent of comparator gain. Settling time is then measured from the time the digital input code changes until the time the comparator output enters a 1-bit band centered about full-scale for the final time. Typical waveforms associated with settling-time measurements made in this manner are shown in Figure 17b.

In the case of current-output DAC’s, settling time can be measured by terminating the output in the inverting node of a high-speed operational amplifier, such as the ADI Model 46, connected in the inverting configuration, and making the measurement in the manner described above. Alternatively, the current output can be terminated in a resistor to convert to voltage directly. Since most current-output DAC’s are output-voltage limited to approximately $\pm 2V$, the 1 LSB analog voltage equivalent is less than 1mV for DAC’s having resolution beyond 11 bits, using this technique. This reduced voltage range heightens the problem of making accurate settling-time measurements, since any noise voltage present becomes a more significant fraction of full-scale.

In general, to make accurate settling-time measurements for a current-out DAC terminated directly in a resistor, it is necessary to keep all lead lengths to an absolute minimum to reduce spurious noise pickup and ringing due to excessive lead inductance. The general tendency of high-gain comparators to oscillate can sometimes be reduced by connecting the output of the DUT to the negative, rather than the positive, comparator input, to reduce inter-wiring capacitive coupling from the comparator output to its positive input, as shown in the configuration of Figure 17.

Comparator Thermal Effects

High-speed comparators of the type used in the test setup of Figure 17a generally have input stages biased at a relatively large current level to maximize comparator gain-bandwidth. As a result, these comparators generally exhibit a thermal time constant of the order of several milliseconds, due to differential self-heating of the input transistor pair as the comparator output changes state. This can add a “tail” of several parts in 10,000 to the final settling time of the comparator output, attributable to the comparator, rather than the DUT. The most effective way of establishing with certainty that observed thermal settling times are due to the measurement system, rather than the DUT, is to make the settling time measurement using the technique described above twice: first with a high-speed comparator, using a square-wave frequency consistent with the anticipated settling time, then with an ultra-low-drift comparator which has been designed to minimize thermal effects (at the expense of gain-bandwidth), and a square-wave frequency below 100Hz.

Alternate Method for Zero and Full-Scale Measurement

A simpler scheme for settling-time measurement than that shown in Fig. 17a which does not require a differential comparator is shown in Figure 18. A square-wave, synchronized to the dynamic digital input square-wave drive, but out of phase with the output of the DUT, is summed with this output. The amplitude of this reference square-wave, E_R , is adjusted to exactly equal that of the DAC output E_O when switching transients have subsided. This produces a zero-volt steady-state error signal or “virtual ground,” by analogy to the error voltage existing at the inverting node of an operational amplifier configured in the inverting mode.

Clamp diodes at the “virtual ground” point limit the voltage excursion during the switching transient period, and the subsequent oscilloscope overdrive; this reduces the oscilloscope

overload recovery time. A calibrated 1-bit threshold level at either zero or full-scale DAC output can be established by switching the LSB digital input from “dynamic” to logic “1”, or logic “0”, respectively, as in the scheme of Figure 17a. A 1-bit band centered about the steady-state display level corresponding to full-scale, or zero, DAC output, can then be readily established on the oscilloscope tube face, and settling time to $\pm\frac{1}{2}$ bit of final value is measured as the time for the error voltage existing at the “virtual” ground point to enter this band for the final time.

If only settling time from full-scale to zero volts is to be measured, the offset square-wave reference, E_R , and its summing resistor R can be eliminated, simplifying the measurement process, using the scheme of Figure 18.

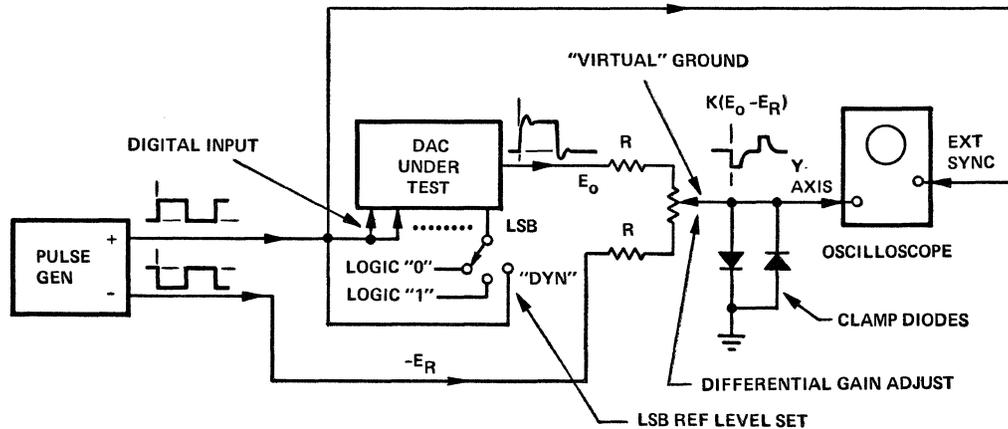


Figure 18. DAC zero and full-scale settling time measurement – virtual-ground method.

Major Carry

When a DAC is operated in a tracking mode, as shown in Figure 6a, for example, the bit-to-bit, rather than full-scale settling time is of importance. The one-bit digital code transition causing the greatest switching transient, and consequently, the longest settling time at the DAC output, generally occurs at the major ($\frac{1}{2}$ -scale) carry transition of the digital code. At this particular code transition, the digital number changes from 0111. . 1 to 1000. . 0 (or vice-versa when counting in the opposite direction), causing all bits to change state, and generally introducing the worst-case 1-LSB switching transient into the DAC output.

Figure 19 illustrates a test configuration for measuring settling time at the major-carry code transition. All bits, except the MSB, are driven in parallel by a square-wave alternating between logic “0” and logic “1” levels. This square-wave is inverted and applied to bit 1, causing this bit to be driven out-of-phase with all the other bits. The steady-state output for this input drive is a square-wave having a 1-LSB peak-to-peak amplitude at half-scale DAC output, corresponding to the major-carry input code transition being traversed from either direction. The DAC output is ac-coupled into an oscilloscope having its sweep *start* synchronized to the input square-wave. Settling time to $\pm\frac{1}{2}$ bit of final value, in this case, is merely the time required for the 1-bit output step-change to reach 50% of its final value. (If the amplitude of the square-wave output is used to establish a 1-bit calibration reference band to expedite the measurement of tracking settling time, the differential nonlinearity occurring at the major carry should first be checked, since this generally represents the code transition causing greatest differential nonlinearity, as well as the greatest switching transient at the DAC output (as discussed under *Differential Linearity*).

Accurate measurement of DAC major carry transient “glitch” duration or amplitude using the scheme of Figure 19 is significantly easier than that of full-scale settling-time measurement, since the DAC analog output steady-state signal excursion in this instance is only 1 bit. As a result, amplifier or comparator overload recovery and thermal response time problems associated with large signal swings at the input to the measurement system are virtually eliminated.

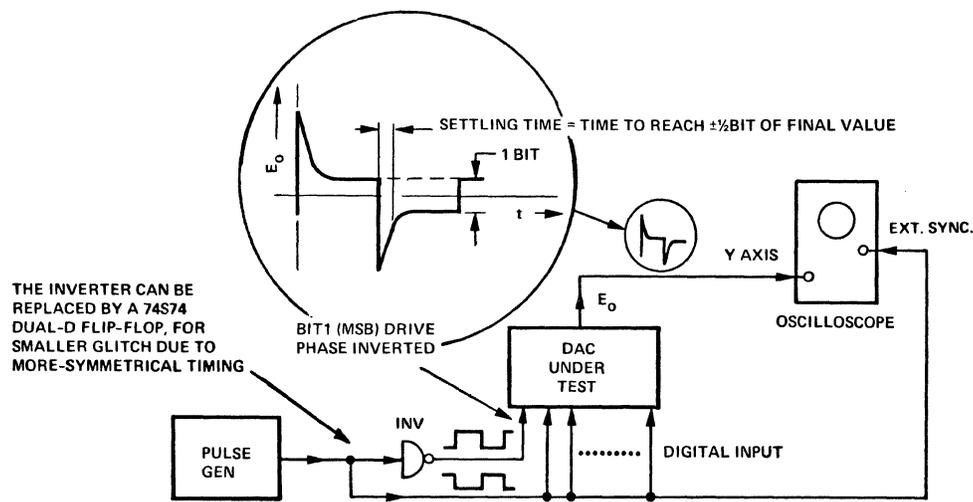


Figure 19. DAC major-carry settling-time measurement.

ADC TESTING

Because of the fundamental $1/2$ -bit quantization uncertainty associated with analog-to-digital conversion, ADC testing is more difficult than DAC testing, owing to the need for determining both the output code and the transition point, referred to the input, rather than simply measuring an output response to a predetermined code. The effects of noise (occurring in either the signal or the converter, or picked up in the wiring) are to introduce an uncertainty in the precise determination of the analog input values at which the output code transitions take place, and to, in effect, increase the quantization band. The nature of these quantization and noise uncertainty errors is shown in Figure 20. (It should be noted, in passing, that the fundamental $\pm 1/2$ -bit worst-case quantization uncertainty sets the requirement that the device accuracy can be no better than its resolution in the case of ADC's. This is in contrast to DAC's, which can have accuracy specifications exceeding their resolution capability. This distinction (or duality) comes about because of the inverse nature of the devices: the DAC output can, with arbitrary precision, locate a level which is a measure of one precise number representing either itself or the quantum determined by the digital number, while the ADC's output level is determined by any input value within the quantized range of input.)

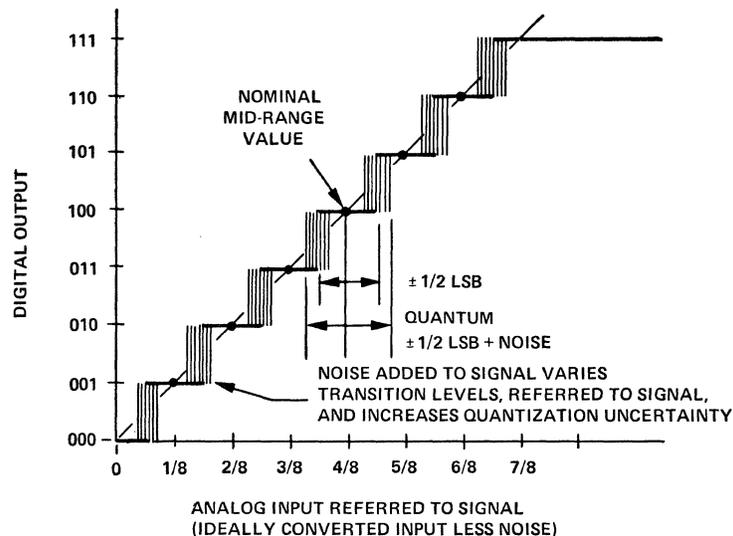


Figure 20. Quantization and noise uncertainty error.

A simplified diagram of an ADC test setup was seen in Figure 1a. The ADC calibration is established by observing correspondence between the state of the input digital toggle-switch register driving the reference DAC and the output digital display representing the state of the ADC. This simplified setup suffers from the disadvantage that the precise location of each analog calibration level within the 1-bit quantization band encompassing each of these respective values cannot be determined. As a result, calibration accuracy, linearity, and differential linearity cannot be determined to a precision greater than 1 LSB using this basic scheme.

One is generally concerned with establishing the calibration of the ADC so that the nominal analog calibration voltage is centered in the quantization band determined by the adjacent transition values. In addition, one normally is interested in checking linearity and differential linearity to a degree better than the $\pm 1/2$ -bit quantization uncertainty imposed on accuracy.

DYNAMIC CROSSPLOT

By summing a small ac signal with the analog reference voltage applied to the input of the ADC under test, the ADC output can be dithered about each of its digital output codes of interest with a large number of analog inputs in a short time. This permits the analog values corresponding to the transitions and the center of each code quantization level to be readily determined, using a dynamic crossplot test. This in turn permits determination of device nonlinearity and differential nonlinearity to a precision greater than $\pm 1/2$ -LSB.

The dynamic crossplot test configuration is shown in Figure 21. The digital code of interest, N_{REF} , is entered into the reference DAC via the toggle-switch register, thereby applying E_{REF} , the analog equivalent of N_{REF} , to the analog input of the DUT. Low-frequency ac dither E_{ac} and adjustable dc offset E_{os} voltages are summed with the reference DAC's output. The dither signal has a frequency that is low with respect to the conversion rate, so that the digitized output of the DUT will exactly track its analog input, within the $\pm 1/2$ -LSB quantization limits. A digital register stores the results of each conversion. A 2-bit DAC is formed using resistors having weights of $2R$ and R to sum the LSB and the adjacent bit, respectively, of the stored ADC output. The decoded 4-step analog output, corresponding to the two stored-ADC least-significant-bit states, is applied to the Y axis of the oscilloscope. The ac

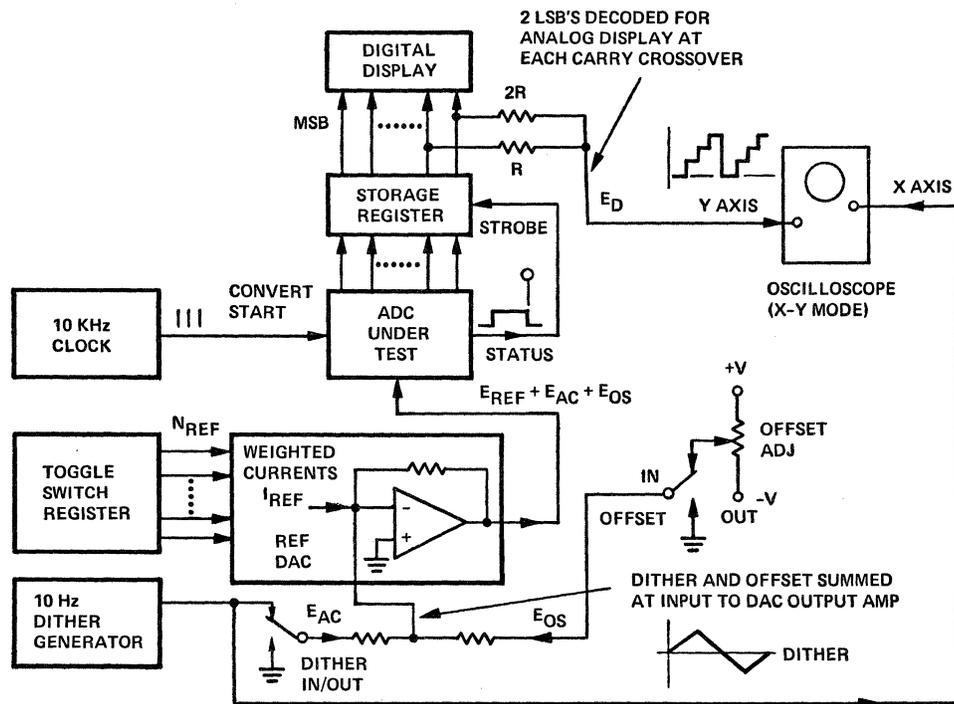


Figure 21. ADC dynamic cross-plot test.

dither signal is applied to the X axis of the oscilloscope, which is operated in the X-Y cross-plot mode. A number of dynamic-crossplot waveforms, obtained using the test configuration of Figure 21, are shown in Figures 22b-22e.

The DUT is calibrated using the dynamic-crossplot display in the following way: The CRT beam is positioned in the center of the tube face, with the X-axis drive signal initially removed, to establish the Y-axis position. All bits, except the LSB of the reference DAC, are turned off; the LSB is turned on. The DUT's zero is adjusted to center the first step of the decoded output staircase waveform, corresponding to the digital code 000 . . . 01 on the Y-axis of the display, as shown in Figure 22b. Next, all bits, except the LSB of the reference DAC, are turned on, corresponding to the digital code 111 . . . 10, and the gain of the ADC is adjusted to center the next-highest step of the decoded staircase waveform on the Y axis, as shown in Figure 22c. These steps calibrate zero and full-scale.

Using the dynamic crossplot display, differential nonlinearity and noise at each bit code transition can be investigated. Figure 22d illustrates the waveform that appears at the major (half-scale)-carry code transition (0 1 1 1 . . . 1 to 1 0 0 0 . . . 0) of the digital output code of the DUT when its bit-1 gain is $\frac{1}{2}$ LSB too large with respect to the gains of the other bits. This causes the staircase step width corresponding to the code 0 1 1 1 . . . 1 to be $\frac{1}{2}$ -LSB too wide.

Figure 22e shows the waveform at the 3/4-scale-carry code transition, 1 0 1 1 . . . 1 to 1 1 0 0 . . . 0, when the bit-2 gain of the DUT is $\frac{1}{2}$ -LSB too small with respect to the other bit gains. This causes the staircase step width corresponding to the code 1 0 1 1 . . . 1 to be $\frac{1}{2}$ -bit too narrow. ADC differential nonlinearity is measured as the deviation in staircase step width from the average step width. The waveforms in both Figures 22d and 22e, show $\frac{1}{2}$ -LSB differential nonlinearity.

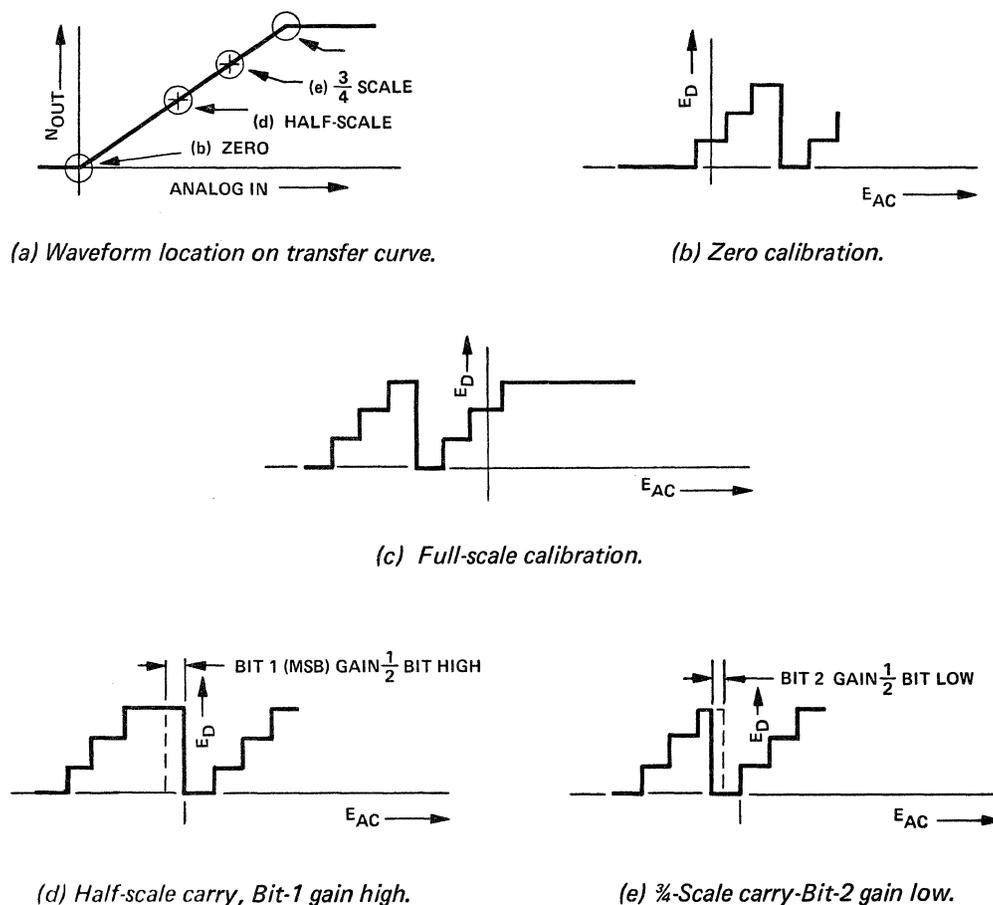


Figure 22. ADC dynamic cross-plot waveforms.

Differential nonlinearity, non-monotonicity (missing codes), and noise can be investigated at each bit code-carry transition by turning on and off each bit of the reference DAC in succession and observing the dynamic crossplot waveform in each case. Summation errors are investigated by turning on all bits, one at a time, in descending order of significance, and leaving them on. The dynamic crossplot waveform is observed as each new bit is turned on. This tests the performance of the DUT in the range from half scale to full scale.

The effects of noise and nonlinearity can also be assessed using the dynamic crossplot test. Noise is seen as a jitter in the location of each staircase-waveform step transition. Device nonlinearity will gradually displace the staircase waveform either to the left or right, as successive bits are turned on and full-scale is approached.

Several points should be noted with respect to the dynamic crossplot test configuration of Figure 21:

- 1) Since, for simplicity, only the two least-significant bits of the DUT's digital output are decoded, the dynamic crossplot waveform repeats every four steps. Initial DUT calibration must therefore be made statically to an error less than 2 bits before the dynamic crossplot is used, so that one can be assured that the desired code transition is being examined, and not one that is 4 LSB's away, which does not have associated with it the desired carry transitions.
- 2) A triangular dither waveform is shown in Figure 21. This waveform could just as well be a sine-wave, since a linear time relationship is not required in the X-Y display mode for a linear X vs Y presentation.
- 3) The external storage register shown in Figure 21 can be eliminated (at the expense of minor crossplot display degradation) if the conversion rate is reduced so that the time between conversions is large, compared to the conversion period, since conversion switching transients will be observed in the crossplot display in this case. Typical dither and conversion clock frequency ranges that have been found useful for dynamic crossplot analysis of high-speed successive-approximation ADC performance using the configuration of Figure 21 are 4-40kHz, and 10kHz to 100kHz, respectively.

ANOMALOUS ERRORS

The dynamic crossplot test just described is very useful in quickly detecting certain ADC performance anomalies, such as might be caused by oscillating comparators and hysteresis, for example. An oscillating comparator causes an excessive randomness in the code transition points on the displayed crossplot – more than could be attributable to random noise.

Some converters exhibit a hysteresis effect, which causes the location of the code transition points to be dependent on the direction from which the point is approached. This causes two horizontally-separated dynamic-crossplot waveforms to appear, much like a series of hysteresis loops. In addition, some converter families have been found to exhibit excessive noise at certain code transitions. The dynamic crossplot test is especially effective in facilitating discovery of such anomalies, because they are displayed quite prominently.

Single-Shot Conversion Errors

Some converters, which appear correctly calibrated when triggered at a high repetition rate, exhibit conversion errors when triggered intermittently at a low rate. Errors of this type can generally be traced to a thermally-induced offset voltage at the comparator input when this device has remained in one state for more than a few hundredths of a second. These effects are more common in older designs, which incorporate discrete-transistor comparators. Use of monolithic comparators in most contemporary converter designs has largely eliminated this problem. One-shot conversion errors are not readily detected using the dynamic-crossplot test configuration of Figure 21, since repeated conversions at a high rate are necessary to obtain a useful display, owing to the restriction on low dither rates imposed by the oscilloscope's short display persistence. Single-shot errors can be detected by removing the

dither and observing the binary display as the conversion rate is reduced, while holding the analog input constant. Errors of this type will generally show up (if present) when the conversion rate is lowered to 1Hz or less.

SEMI-AUTOMATIC TESTING

A more elaborate ADC test configuration than that of Figure 21, which lends itself to semi-automatic ADC testing, is shown in Figure 23. A 3-position toggle switch permits selection of logic "0", logic "1", or "dynamic" for each reference-DAC bit input. The output E_R of the reference DAC is applied to the input of the DUT. The digital output word N_O of the DUT is transferred to a storage register at the completion of each conversion. The digital word N_R at the input of the reference DAC is subtracted from N_O , and the digital error $N_O - N_R$ is applied to a low-resolution DAC, permitting analog presentation of the error. Alternatively, this error, $N_O - N_R$, can be applied to a limit comparator having preset high and low error limits, permitting go-no testing.

Dynamic testing using the configuration of Figure 22 can be done in two principal modes: *bit-scan*, and *count*, by analogy to the DAC test configuration, shown in Figures 9 and 11. The resolution of the reference DAC used in the configuration of Figure 23 should be at least two bits better than that of the ADC being tested, so that quantization of the analog input to the DUT will not limit the error readout resolution to less than that imposed by the $\pm\frac{1}{2}$ -bit quantization band attributable to the DUT.

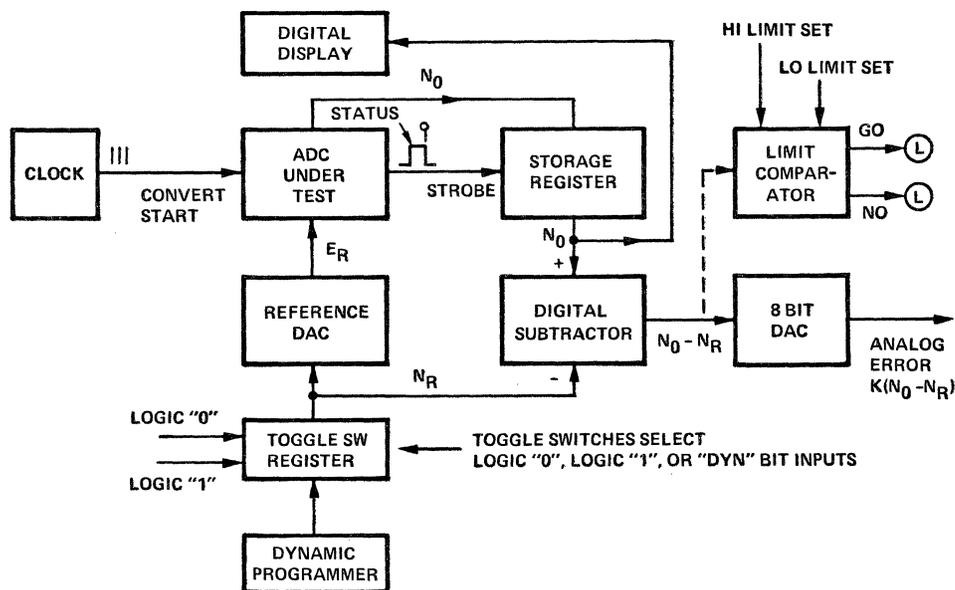


Figure 23. ADC test configuration.

II

Specifying Converters

Chapter II-5

The applications for digital data-handling equipment and the products of the conversion-and-data-acquisition industry have spawned a multiplicity and diversity of companies, product lines, and products. We find it sobering (though not a little gratifying) to discover that, as a major manufacturer, with a reasonably complete line of monolithic, hybrid, and modular products, we can deliver some 125 distinct converter types, of which a large number are in the “recommended-for-new-designs” category, and that the line is growing substantially each year.

Thus the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence, to date, of standardized definitions of specifications among manufacturers.

To remedy this situation, and attempt to make the system designer’s job of finding the “right” converter a little easier,* this chapter lists some of the elements of the decision and steps a user can take to help “home in” on a near-optimum selection. In this chapter are also summarized interpretations of the specifications consistent not only with the previous three chapters and with engineering practice at Analog Devices, but also – it is to be hoped – with interpretations that may become accepted as standard within the industry.

A selection guide is provided for the convenience of the engineer who may seek orientation to the various categories of devices available off-the-shelf from Analog Devices. It is based on the 1977 Analog Devices catalog, which leads to the natural suggestion that the latest catalog available be consulted for specific choices. The reader is invited to request a copy from Analog Devices, either directly or via our nearest sales office.

Finally, a brief example of a data-acquisition design process, based on the suggestions in this chapter, is given.

TWO BASIC FACTORS

The two key factors in choosing the right device are:

Completely define the design objectives. Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interfaces, environmental conditions and space factors, anticipated budgetary limitations that may force performance compromises or a different system approach.

Understand what the specs mean. It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed (in 1977) that any two manufacturers mean the same thing when they publish identical numbers defining a

*It’s possible that some of the points raised here, if previously unanticipated by the reader, may actually make the initial selection more involved, with the benefit that problems will be fewer at a later (and more expensive) stage.

given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. Two examples that give an insight into how differences arise are included and discussed at length in the Specifications section: *linearity* and *temperature coefficient*.

DEFINING THE OBJECTIVES – APPLICATION CHECKLISTS

General Considerations

- A. Accurate description of input and output
 - 1. Analog signal range; source or load impedance
 - 2. Digital code needed: Binary, 2's complement, BCD, etc.
 - 3. Logic-level compatibility: TTL, CMOS, etc., logic polarity
(Unless otherwise noted, logic levels mentioned in Analog Devices publications are standard TTL, positive true)
- B. Data throughput rate
- C. Control and data-interface details or constraints.
- D. What does the system error budget allow for each block?
- E. What are the environmental conditions: temperature range, supply voltage, re-calibration interval, etc., over which the converter should operate to the desired accuracy?
- F. Are there any special environmental conditions that must be coped with?
High-power RF, high humidity, shock and vibration, and cramped space are a few.
- G. What are the bounds of integration for the purchased portion of the system? Turn-key system, real-time interface, data-acquisition subsystem, subassemblies, components? What are the hardware/software, analog/digital tradeoffs?

In addition to the above general considerations, there are specific items to consider when choosing each block in a system.

Considerations for D/A Converters

- A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted? To what degree of accuracy, linearity, etc.?
- B. What logic levels and codes can be provided to the DAC? (The most popular logic system is TTL, and the most-frequently used codes are binary, 2's complement, offset binary (2's complement with a complemented MSB), as outputs of systems, and BCD, usually derived from digital voltmeters or thumbwheel switches.) Is digital input serial or parallel?
- C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier. Voltage-output DAC's are the more convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μs and sub- μs settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., via CRT deflection amplifiers)).
- D. What kind of reference is needed, fixed (internal or external) or variable (multiplying DAC)? How many quadrants are needed, and how arranged, for multiplying DAC's (1-quadrant, 4-quadrant, 2-quadrant digital, 2-quadrant analog)?
- E. What is the nature of the digital interface? What are the speed requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed (i.e., deglitched)

within the DAC? What is the analog signal feedthrough requirement for multiplying DAC's at low frequencies? At high frequency?

F. Over how wide a temperature range (at the device, including its internal temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment? What deterioration of specifications is permitted (gain vs. linearity, etc.)?

G. How stable are the terminal voltages of the power supplies that will power the DAC? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits? Are there constraints on converter dissipation?

Though no list can be complete, the above items will be the minimum consideration in any more-complete tabulation.

Considerations for A/D Converters

The process of selecting an A/D converter is similar to that involved in the selection of D/A converters. Some of the following considerations are analogous to those for D/A's, and others are unique to A/D's.

A. What is the analog input range, and to what resolution must the signal be measured?

B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?

C. To what extent must the various sources of error be minimized as ambient temperature changes? Are missed codes tolerable under any conditions?

D. How much time is allowed for each complete conversion?

E. Is the reference to be fixed, adjustable, or variable (ratiometric measurement)?

F. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system? Are there constraints on converter dissipation?

G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? What conversion circuit philosophies are acceptable for – or indicated by – the application? (e.g., successive-approximation, dual-slope integration, counter-&-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1 MHz. Counter-comparator types provide lowest cost but may be both slow and noise-susceptible; they are useful for peak followers and sample-holds that employ digital storage.)

H. What is the format of the digital interface? Parallel, byte-serial, serial? What kind of logic? Three-state, CMOS, TTL?

Considerations for Analog Multiplexers and Sample-Holds

When a sampled-data system is to be assembled, in which one A/D converter is time-shared among many input channels by the use of a multiplexer and sample-hold, their contribution to system performance errors must be taken into account. These accessory devices are discussed elsewhere, but they are also discussed briefly in this chapter because of their relevance to the converter selection process.

Multiplexers

A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?

B. What kind of hierarchy is used, if a great many channels are involved? What is the addressing scheme?

C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?

- D. How much ac crosstalk error between channels is allowable? At what frequencies?
- E. What error is produced by the leakage current flowing through the source resistance?
- F. What will be the multiplexer “transfer” error, produced by the voltage divider formed by the *on* resistance of the multiplexer and the input resistance of the sample-hold. Is the multiplexer active or passive (i.e., does it have an output amplifier?)
- G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test purposes?
- H. Is there danger of damage to active signal sources when the power is turned off? (MOSFET multiplexers are inherently “safe” (at least in this sense), since the switches open when power is removed. JFET multiplexer switches can conduct when power is removed, making it possible to interconnect, and therefore damage active signal sources.

Sample-Holds

- A. What is the input signal range?
- B. Considering the slewing rate of the signal and the multiplexer’s channel-switching rate, what is the sample-holds’s allowable acquisition time to within the desired error band?
- C. What accuracy is needed (gain, linearity, and offset errors)?
- D. What aperture delay and jitter are allowable, going into *hold*? (The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, $1V/\mu s$ produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance, but jitter modulates the sampling rate.
- E. How much droop is allowable in *hold*?
- F. What are the effects of time, temperature, and power supply variation?
- G. What offset error is caused by the flow of the sample-hold’s input bias current through the series resistance of the multiplex switch and the signal source?

DEFINING THE SPECIFICATIONS

Figures 1 and 2 depict the specifications of typical D/A and A/D converters. Though the specs probably mean “what you think they mean,” it is important that their meaning and implications be spelled out. The following list, in alphabetical order, should prove helpful.

Absolute Accuracy. Absolute accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter.

Absolute accuracy error of an A/D converter is the difference between the analog input theoretically required to produce a given digital output code and the analog input actually required to produce that same code. Since a band of analog values can produce the same code, the “input required to produce a given digital output code” is defined as the midpoint of either the theoretical or the measured band.

Absolute accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Acquisition Time. The acquisition time of a sample-hold circuit is the time it takes to acquire the input signal to within the stated accuracy. When conservatively specified, as in Analog Devices’ specifications, it includes the *settling time* of the output amplifier. Since it is possible, in some cases, for a signal to be fully acquired (and the circuit switched into *hold*) before the output has settled, one should be sure of what a manufacturer means by this term, since the output of the sample-hold is not meaningful until it has settled.

Aperture Time. This is the time it takes in a sample and hold circuit, for the switch to open

SPECIFICATIONS ($T_A = +25^\circ\text{C}$, unless otherwise specified)

MODEL	AD563K			AD563S			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS							
TTL, $V_{CC} = +5\text{V}$, Pin 2							
Open Circuit							
Bit ON Logic "1"	+2.0			+2.0			V
Bit OFF Logic "0"			+0.8			+0.8	V
CMOS, $4.75 \leq V_{CC} \leq 15.8$, Pin 2 tied to Pin 1							
Bit ON Logic "1"	70% V_{CC}			70% V_{CC}			V
Bit OFF Logic "0"			30% V_{CC}			30% V_{CC}	V
Logic Current (each bit)							
Bit ON Logic "1"		+20	+100		+20	+100	nA
Bit OFF Logic "0"		-50	-100		-50	-100	μA
OUTPUT							
Current							
Unipolar	-1.7	-2.0	-2.3	-1.7	-2.0	-2.3	mA
Bipolar	± 0.85	± 1.0	± 1.15	± 0.85	± 1.0	± 1.15	mA
Resistance (exclusive of span resistors)							
Unipolar Zero (all bits OFF)	5.3k	6.6k	7.9k	5.3k	6.6k	7.9k	Ω
Capacitance		33			33		pF
Compliance Voltage		-1.5 to +10			-1.5 to +10		V
RESOLUTION							
		12 Bits			12 Bits		
ACCURACY (Error relative to full scale)							
			$\pm 1/4$ (0.006)			$\pm 1/4$ (0.006)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY							
			$\pm 1/2$			$\pm 1/2$	LSB
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON							
		1.2			1.2		μs
POWER REQUIREMENTS							
V_{CC} , +4.75 to +15.8VDC							
		15	20		15	20	mA
V_{EE} , -15VDC $\pm 5\%$							
		20	25		20	25	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} @ +5VDC							
		3	10		3	10	ppm of F.S./%
V_{CC} @ +15VDC							
		3	10		3	10	ppm of F.S./%
V_{EE} @ -15VDC							
		14	25		14	25	ppm of F.S./%
TEMPERATURE RANGE							
Operating							
		0 to +70			-55 to +125		$^\circ\text{C}$
Storage							
		-65 to +150			-65 to +150		$^\circ\text{C}$
TEMPERATURE COEFFICIENT							
With Internal Reference							
Unipolar Zero							
		1	2		1	2	ppm of F.S./%
Bipolar Zero							
			10			10	ppm of F.S./%
Gain							
			20			30	ppm of F.S./%
Differential Nonlinearity							
		2			2		ppm of F.S./%
MONOTONICITY							
		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
EXTERNAL ADJUSTMENTS*							
Gain error with fixed 10 Ω resistor							
		± 0.1			± 0.1		% of F.S.
Bipolar Zero Error with Fixed 10 Ω resistor							
		± 0.1			± 0.1		% of F.S.
Gain Adjustment Range							
		± 0.25			± 0.25		% of F.S.
Binary Bipolar Zero Adjustments Range							
		± 0.25			± 0.25		% of F.S.
BCD Bipolar Offset Adjustment Range							
		± 0.17			± 0.17		% of F.S.
PROGRAMMABLE OUTPUT RANGES (See Figs. 1a, 1b)							
		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
REFERENCE INPUT							
Input Impedance							
		5k			5k		Ω
REFERENCE OUTPUT							
Voltage							
	2.425	2.500	2.575	2.425	2.500	2.575	V
Current							
			5			5	mA
Impedance							
		1			1		Ω

*Device calibrated with internal reference Specifications subject to change without notice.

Figure 1. Typical microcircuit d/a converter specifications (AD563).

after the control command has been given. In a good SHA, this should not exceed 50ns delay, including 10ns uncertainty.

Common-Mode Range. Common-mode rejection usually varies with the magnitude of the range through which the input signal can swing, determined by the sum of the common-mode and the differential voltage. *Common-mode range* is that range of *total* input voltage

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25 to +85°C	Guaranteed: -55 to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV _S	*	*
±5V	±0.001% FSR/%ΔV _S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C) ±25ppm/°C (-55 to +125°C)
Unipolar Offset	±3ppm FSR/°C	±3ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)			
	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
Status	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE			
	+10.00V, ±5mV	*	*
Max External Current	±4mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	**
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA	*	*
	-15V, ±5% @ -20mA	*	*
	+5V, ±5% @ +50mA	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25 to +85°C	*	-55 to +125°C
Operating	-55 to +125°C	*	*
Storage	-55 to +150°C	*	*
*Same specification as AD572AD			
**Same specification as AD572BD			
Specifications subject to change without notice.			
	Note 1	Positive pulse 200ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.	
	Note 2	With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.	

Figure 2. Typical microcircuit a/d converter specifications (AD572).

over which specified common-mode rejection is maintained. For example, if the common-mode signal is ±5V and the differential signal is ±5V, the common-mode range is ±10V.

Common-Mode Rejection. The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. It is usually expressed either as a ratio (CMRR = 10⁶) or as 20 log₁₀ of the ratio (CMR = 120dB). A CMRR of 10⁶ means that a 10V common-mode voltage is processed by the device as though it were an additive differential input signal of 10μV magnitude.

Common-Mode Voltage. A voltage that appears in common at both input terminals of a device, with respect to its output reference (usually “ground”). For inputs V_1 and V_2 , with respect to ground, $CMV = \frac{1}{2} (V_1 + V_2)$. *Common-mode error* is any error at the output due to the common-mode input voltage.

Compliance-Voltage Range. For a current source (e.g., a current-output DAC), the maximum range of terminal voltage for which the current source will maintain its defined characteristics.

Conversion Time. The time required for a complete measurement by an analog-to-digital converter. In successive-approximation converters, it ranges typically from $1.0\mu s$ (ADC-1103-001) to $400\mu s$ (ADC-16Q). Popular 12-bit general-purpose A/D converters, such as the AD572, have conversion time of about $25\mu s$.

Crosstalk. Leakage of signals between circuits or channels of a multi-channel system or device, such as a multiplexer. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent.

Deglitcher (See Glitch). A device that removes or reduces the effects of time-skew pulses in D/A conversion. A deglitcher normally consists of a sample-hold circuit, which holds the DAC output constant at the previous value until the switches reach equilibrium. Since the phenomena involved can be extremely fast, the *deglitcher* is usually a portion of the circuit, rather than a specific general-purpose modular device.

Differential Nonlinearity. In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 01111111 to 1000000, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic*, or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of $\pm\frac{1}{2}$ LSB at $25^\circ C$ ensures that monotonic behavior will exist over a tangible range of temperature, or each step is $(1 \pm \frac{1}{2})$ LSB.

Differential-Nonlinearity Temperature Coefficient. Since bit weightings vary to some degree with temperature, a converter having acceptable differential nonlinearity at 25° may have > 1 LSB error at some other temperature. The temperature coefficient describes the maximum variation of differential linearity error with temperature over the specified range. Often, instead of a temperature coefficient, this specification may appear as a range of temperature for which behavior is monotonic.

Droop Rate. When a sample-hold circuit using a capacitor for storage is in *hold*, it will not hold the information forever. Droop rate is the rate at which the output voltage changes (by increasing or decreasing), and hence gives up information. As a rule, when using a SHA (sample-hold amplifier) ahead of an ADC, the SHA should not droop more than 0.1 LSB during the conversion time of the ADC.

Dual-Slope Converter. An integrating A/D converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a length of time determined by a counter. Then a reference input is switched to the integrator, which integrates “down” from the level determined by the unknown until a “zero” level is reached. The time for the second integration process is pro-

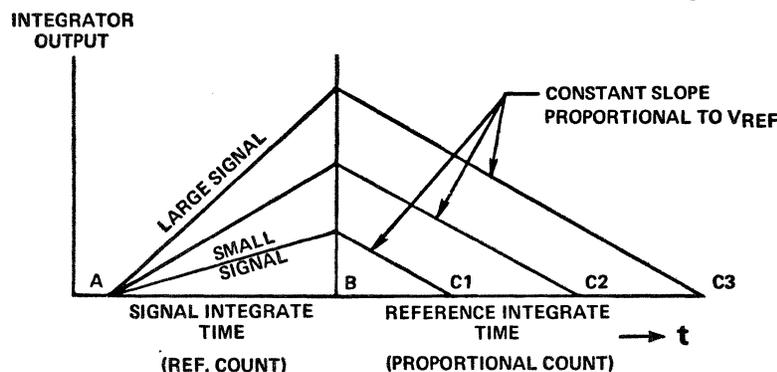


Figure 3. Voltage-time relationships in dual-slope conversion.

portional to the average of the unknown signal level over the predetermined integrating period. The same counter and clock are used for this measurement, and thus the output is immune to long-term variations of the integrator's characteristic time and the clock frequency. The counter provides the digital readout.

Feedthrough. A term referring to that characteristic of a circuit or device manifested by undesirable signal leakage around switches or other devices that are supposed to be turned off or provide isolation. Both digital and analog signals can cause analog feedthrough errors.

Four-Quadrant. In a *four-quadrant* multiplying DAC, if both the reference signal and the number represented by the input may be bipolar, the output can be either positive or negative, obeying the rules of multiplication as to algebraic sign in all four quadrants.

"Gain" Adjustment. The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted, typically, by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

"Glitch". If one applies the output of a counter to the input of a DAC to develop a "staircase" voltage, the number of bits involved in a code change establish "major" and "minor" transitions. The most major transition is at $\frac{1}{2}$ -scale, when the D/A switches all bits, i.e. from 011 . . . 111 to 1000 . . . 00. If, for digital inputs having no skew, the switches are faster to switch *off* than *on*, this means that, for a short time, the DAC will seek zero output, and then return to the required 1LSB above the previous reading. This large transient spike is commonly known as a "glitch." The better-matched the input transitions and the switching times, and the faster the switches, the smaller will be the energy contained in the glitch. Because the size of the glitch is not proportional to the signal amplitude, linear filtering may be unsuccessful and may, in fact, make matters worse. (See also *Deglitcher*)

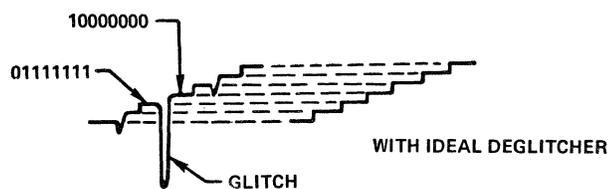


Figure 4. Glitch at a major carry.

Least-Significant Bit (LSB). In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the *least-significant bit* is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + 2^0$), the rightmost "1" is the LSB. The weight of 1LSB, in relation to full scale, is the *resolution* implied by the digital number.

Linearity. Linearity error of a converter is the deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (Figure 5). Sometimes referred to as "end-point" nonlinearity, the latter is the definition used by Analog Devices, both because it is a more conservative measure, and because it is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Relative Accuracy).

For Multiplying D/A converters, the analog linearity error at a given digital code is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Once the converter has been adjusted and calibrated, deviations from linearity become absolute errors. While differential-linearity errors are cyclic, other linearity errors, such as might be caused by amplifier nonlinearity, tend to follow the usual nonlinearity patterns of other analog devices.

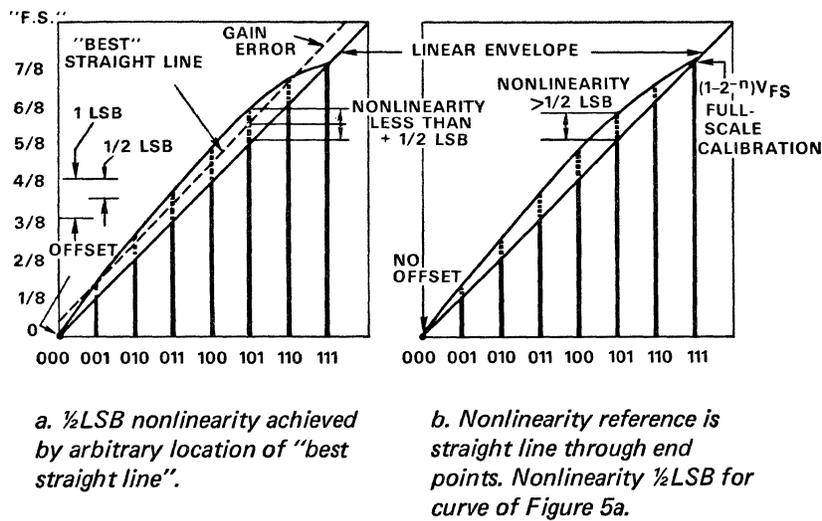


Figure 5. Comparison of linearity criteria for 3-bit D/A converter. Straight line through end points is easier to measure, gives more-conservative specification.

Monotonicity. The output of a monotonic D/A or A/D converter never decreases in response to an increasing input stimulus (or vice versa). In high-speed converters, it is not especially hard to trim a design to be monotonic over limited temperature ranges. In order to be monotonic over very wide temperature ranges, error components of DAC switches and resistor networks must track each other very closely with temperature change. Monotonic behavior requires that the differential nonlinearity be < 1 LSB. In ADC's, the counterpart of non-monotonic behavior is the "missed code," which is produced when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but in one removed by one or more counts. Monotonic behavior in high-resolution conversion over wide temperature ranges is not easy to accomplish at the present state of the art; consequently, converters like the AD572, which have no missed codes over the specified temperature range, at reasonable cost, are not commonly seen in the industry. Integrating converters, such as the AD7550 are inherently monotonic; A/D converters of this class are also inherently slow (usually more than 35ms for a full conversion).

Most Significant Bit (MSB). In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the *most-significant bit* is that digit (or "bit") that carries the greatest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$), the leftmost "1" is the MSB, with a weight of $\frac{1}{2}$ nominal peak-to-peak full scale. In bipolar devices, the sign bit is the MSB. In A/D converters having overrange bits, the MSB is the most-significant "overrange" bit.

Multiplying DAC. A multiplying DAC differs from the conventional fixed-reference DAC in being designed to operate with reference signals that vary, often (ac) at high speeds. The output signal of such a DAC is proportional to the product of the reference voltage and the fractional equivalent of the digital input number. In addition to the usual DAC specifications, the multiplying DAC is specified as to analog signal *feedthrough* at low and high frequencies, and number of quadrants (1, 2-digital, 2-analog, or 4).

Noise. In high-resolution DAC's, such as the DAC1138, noise can be an important consideration, since the resolution is not confidently assignable when the peak noise exceeds the LSB value over a reasonable bandwidth. For an ADC, noise, either in the input signal, the input circuitry, or the conversion device itself, effectively increases the size of the quantization band, and may thus impart statistical properties to the output numbers, which may then require additional processing for successful interpretation.

Noise: RMS vs. Peak-to-Peak. For all but integrating converters, peak noise must be considered carefully, especially where small numbers of readings and limited processing capacity

are available. An rms noise specification over a given bandwidth allows peak-to-peak predictions for gaussian noise (peak-to-peak values greater than 7x rms will probably occur less than 0.1% of the time). However, both peak-to-peak and rms noise specs should be looked at, since large spikes could be present on the output of a chopper-stabilized amplifier, or could be coupled into the analog portion of the system. These spikes, if narrow, will contribute little to driving the rms noise out of spec, but could nevertheless be considerably greater than 7x rms. If a DAC having spike noise on its output were used in a display system, the noise would cause distortion of the pattern, and loss of useful resolution.

Offset. For almost all bipolar converters (e.g., ± 10 volts output) instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the $\frac{1}{2}$ scale offset completely cancels the weight of the MSB at zero, independently of the amplitude of both.

“ON” Resistance. “ON” resistance of a device such as a FET, when used as a switch performing a function (such as multiplexing), refers to the ohmic resistance while turned on. For multiplexer service, a few hundred ohms or less will usually provide adequate accuracy. For other switching service, such as in a DAC, values of 10 ohms or less are desirable.

Power-Supply Sensitivity. The sensitivity of a converter to changes in the power supplies is normally expressed in terms of percent change in analog value (D/A output, A/D input) for a 1% change in power supply, e.g., $0.05\%/\% \Delta V_s$. As a rule, for a good converter, the fractional change in scale factor should be well below the equivalent of $\pm \frac{1}{2}$ LSB for a 3% change in power-supply voltage. When power-supply voltage changes affect conversion accuracy excessively, the key culprit is often a marginal “constant-current-circuit” for the reference diode.

Quad-Slope Converter. This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with tempo (gain and zero temperature coefficients) less than 1ppm/ $^{\circ}$ C.

Quantizing Uncertainty (or “Error”). The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of $\pm \frac{1}{2}$ LSB, associated with the *resolution*, in addition to the actual conversion errors. This uncertainty is a property of the *system* resolution.

Relative Accuracy. Relative accuracy error is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The “discrete points” of a D/A transfer characteristic are measured by the actual analog outputs. The “discrete points” of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Absolute Accuracy).

Resolution. Nominal Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n , as a percentage, in parts-per-million, or simply by “n bits.” *Useful resolution* (not usually specified explicitly) is the smallest uniquely-distinguishable bit for all conditions of required operation (time, temperature, etc.) For example, a “12-bit” converter may have a useful resolution, over its temperature range, of only 10 bits. Useful resolution of DAC’s and devices using them (including ADC’s) is limited by the *relative accuracy*, but resolution need not limit accuracy. For example, a

4-bit D/A converter used in a programmable power supply has 16 levels, but it could have a required accuracy within 0.01% (absolute and/or relative). Note that low-cost completely-monolithic 8-bit DAC's need not necessarily have sufficient accuracy for such an application, although their resolution is more than adequate.

Settling Time. This is the time it takes for a DAC to settle for a full-scale code change, usually to within the analog equivalent of $\pm 1/2$ LSB. For some applications, e.g., in staircase waveform generation, another important specification is the settling time for a single LSB change (at the major carry, and elsewhere).

Slew(ing) Rate. A limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of more than a few volts/ μ s are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a modern D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate magnitude is usually a guide (but by no means infallible) to settling time.

Stability. In a well-designed intelligently-applied converter, *dynamic stability* is never a serious question. The term *stability* usually connotes the insensitivity of a converter's characteristics to time, temperature, etc. All measurements of instability are difficult and time-consuming (especially in high-resolution devices), but instabilities vs. temperature are sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see *temperature coefficient*).

Successive Approximations. A method of comparing an unknown against a group of weighted references (usually binary), capable of high speed. The process of successive approximations in an A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights, such as 1 gram, $1/2$ gram, $1/4$ gram, etc.

Switching Time. In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time.

Temperature Coefficient (See also *Differential-Nonlinearity Temperature Coefficient*). Temperature coefficients of gain and offset are defined in terms of the "average" deviation over a range of temperature variation, i.e. $(\epsilon_{T_1} - \epsilon_{T_2})/(T_1 - T_2)$. For specified temperature ranges that extend from below room temperature to above room temperature, the device is zeroed and calibrated at room temperature, and the temperature coefficient for the "high" range ($T_H - T_A$) and for the "low" range ($T_R - T_A$) are both compared with the specification; both must be better than specified.

a. *Gain TC* This is affected by the reference zener (< 5 ppm/ $^{\circ}$ C for a good diode) and the reference circuitry, including the reference amplifier and switches (3ppm/ $^{\circ}$ C in very good converters). The total gain (or scale factor) change is specified in ppm/ $^{\circ}$ C.

b. *Zero TC (unipolar converters)* The zero stability of a unipolar DAC is almost entirely governed by the output amplifier's zero stability. Since output amplifiers are usually employed essentially as current-to-voltage converters, they operate at low values of closed-loop gain, and the zero TC is not greatly affected by the choice of programmable gain setting (i.e., 0-5V or 0-10V). Zero TC is usually expressed in μ V/ $^{\circ}$ C. Zero TC in ADC's is generally dependent only on the zero stability of the input buffer amplifier (if included) and the comparator and is expressed in μ V/ $^{\circ}$ C, referred to the input.

c. *Zero TC (bipolar converters)* Converters that use offset-binary coding are "zero" set at the all-bits-off point, and their scale factor is set at either all-bits-on, or (for more precise zero) at the MSB transition. However, the zero TC is measured at the MSB transition (analog zero). It is affected by the reference TC, the tracking of the offset reference, and the tracking of the bipolar-offset and gain-setting resistors. For such precision DAC types as AD561, which use the same reference for both the scale factor and the MSB offset, and monolithic resistor networks (with their excellent tracking), the zero-TC specification differs little for both the unipolar and bipolar connections.

Zero Setting. The zero level of a unipolar DAC is set to zero volts at the code corresponding to 0V. The LSB transition of an ADC is offset by $\frac{1}{2}$ LSB, so that all subsequent transitions ideally occur midway between the nominal code values. (See also *offset* and *zero TC*.)

SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of "successive approximations:" Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy.

If its performance seems far in excess of that needed (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember, though, that in a maturing industry, costs can be expected to decline. *It is often less costly, in the long run, to go for better performance (rather than lowest possible cost) in the initial stages of a design.* Also, efforts aimed at reducing the cost of any element of a system should bear in mind the relationship of its cost relative to that of the entire project.

In fact, where new designs are concerned, and early results are essential, unless one is an experienced system designer with plenty of component and manufacturing experience (if quantities are involved), it is usually good judgement to ignore initial cost (within the limits of good sense) and go for performance, convenience, and the highest level of system integration that the budget will allow (see Chapter I-4).

TYPICAL CONVERTER CLASSIFICATIONS

Once the problem is defined and the key specifications have been determined, one is still faced with the question of narrowing the choices to devices (converters) likely to "fill the bill" as rapidly as possible, so as to conserve the time needed for actual evaluation.

The selection guides from the 1977 Analog Devices Short-Form catalog are useful for this purpose and are reproduced on the following 6 pages for the convenience of our readers. They are classified by family (a/d, d/a, v/f, etc.) and by technological groupings (IC's, modules), and within that grouping, by salient specifications (resolution, linearity error, settling time, gain tempco, etc.) They are up-to-date as of Spring, 1977.*

AN EXAMPLE OF THE SELECTION AND VERIFICATION PROCESS†

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers $\pm 10V$ full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is $+25^{\circ}C$ to $+55^{\circ}C$. Sufficient power at both $\pm 15V$ and $+5V$ is available, but the regulation of the $\pm 15V$ supply is 150mV.

The objective: specify a set of conversion components having appropriate accuracy and speed.

FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better

*Readers of this book are invited to communicate with ADI or our representatives for more recent listings, or to receive additional product suggestions for a given application.

†For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the less-salient sources of error have been intentionally omitted. If there are any that you're concerned about for your application but don't see here, we invite you to communicate with our Applications Engineers.

CONVERTER ICs: DIGITAL-TO-ANALOG

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Resolution	Accuracy	Differential Nonlinearity	Gain T.C.	Inputs	Output	Power Dissipation	Temp. Range*	Package
AD559K	8-bit DAC, replaces	8-Bits	±0.19% max	±1/2LSB max	20ppm/°C	TTL	Unipolar	280mW max	C	16 Pin DIP
AD559S	Motorola 1408/1508	8-Bits	±0.19% max	±1/2LSB max	20ppm/°C	TTL		280mW max	M	16 Pin DIP
AD7520JN/JD	10-bit monolithic	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	16 Pin DIP
AD7520SD	CMOS multiplying	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	16 Pin DIP
AD7520KN/KD	DAC	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7520TD		10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	16 Pin DIP
AD7520LN/LD		10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7520UD		10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	16 Pin DIP
AD7521JN/JD	12-bit, monolithic	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	18 Pin DIP
AD7521SD	CMOS multiplying	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	18 Pin DIP
AD7521KN/KD	DAC	12-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD7521TD		12-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	18 Pin DIP
AD7521LN/LD		12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD7521UD		12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	18 Pin DIP
AD7522JN/JD	10-bit, monolithic	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	28 Pin DIP
AD7522SD	CMOS multiplying	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	28 Pin DIP
AD7522KN/KD	DAC with micro-	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	28 Pin DIP
AD7522TD	processor com-	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	28 Pin DIP
AD7522LN/LD	patible input buffer	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	28 Pin DIP
AD7522UD	& holding register	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	28 Pin DIP
AD7530JN/JD	Low cost 10-bit	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	16 Pin DIP
AD7530KN/KD	monolithic CMOS	10-Bits	±0.1% max	±0.2% max	10ppm/°C max	CMOS	Bipolar	20mW	C/I	16 Pin DIP
AD7530LN/LD	multiplying DAC	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7531JN/JD	Low cost 12-bit	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	18 Pin DIP
AD7531KN/KD	monolithic CMOS	12-Bits	±0.1% max	±0.2% max	10ppm/°C max	CMOS	Bipolar	20mW	C/I	18 Pin DIP
AD7531LN/LD	multiplying DAC	12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD561J	10-bit DAC	10-Bits	±0.05% max	±0.05%	80ppm/°C max	TTL/	Unipolar/	290mW max	C	16 Pin DIP
AD561K	with reference,	10-Bits	±0.025% max	±0.05% max	30ppm/°C max	CMOS	Bipolar	290mW max	C	16 Pin DIP
AD561S	monotonic	10-Bits	±0.05% max	±0.05%	60ppm/°C max			290mW max	M	16 Pin DIP
AD561T	performance	10-Bits	±0.025% max	±0.05% max	30ppm/°C max			290mW max	M	16 Pin DIP
AD562K	12-bit DAC, mono-	12-Bits	±0.006% max	±0.012%	5ppm/°C max	TTL/	Unipolar/	475mW max	C	24 Pin DIP
AD562A	tonic performance	12-Bits	±0.006% max	±0.012%	5ppm/°C max	CMOS	Bipolar	475mW max	I	24 Pin DIP
AD562S		12-Bits	±0.006% max	±0.012%	5ppm/°C max			475mW max	M	24 Pin DIP
AD563J	12-bit DAC with	12-Bits	±0.012% max	±0.012% max	30ppm/°C max	TTL/	Unipolar/	475mW max	C	24 Pin DIP
AD563K	reference, monotonic	12-Bits	±0.006% max	±0.012% max	20ppm/°C max	CMOS	Bipolar	475mW max	C	24 Pin DIP
AD563S	performance	12-Bits	±0.006% max	±0.012% max	30ppm/°C max			475mW max	M	24 Pin DIP
AD563T		12-Bits	±0.006% max	±0.012% max	10ppm/°C max			475mW max	M	24 Pin DIP

*Note: C = 0 to +70°C I = -25°C to +85°C M = -55°C to +125°C Suffix N - Plastic Suffix D - Ceramic

CONVERTER ICs: ANALOG-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Resolution	Accuracy	Differential Nonlinearity	Gain T.C.	Conversion Time	Power Dissipation	Temp. Range*	Package
AD7570JD	8 & 10-bit, CMOS,	8-Bits	±0.19% max	No missing	10ppm/°C max	20μs	20mW	C	28 Pin DIP
AD7570LD	successive approxi-	10-Bits	±0.05% max	codes	10ppm/°C max	20μs	20mW	C	28 Pin DIP
	mation A/D								
AD7550BD	13-bit, quad slope	13-Bits	±0.006% max	No missing	1ppm/°C	40ms	9mW	C	40 Pin DIP
	A/D			codes					
AD572A	12-bit bipolar A/D	12-Bits	±0.012% max	±½LSB max	30ppm/°C max	25μs max	900mW	I	32 Pin
AD572B	with reference,	12-Bits	±0.012% max	No missing	15ppm/°C max	25μs max	900mW	I	Metal
AD572S	comparator, buffer	12-Bits	±0.012% max	codes	25ppm/°C max**	25μs max	900mW	M	DIP
	amplifier								

*Note: C = 0 to +70°C I = -25°C to +85°C M = -55°C to +125°C
 **±15ppm/°C max for temperature range -25°C to +85°C

CONVERTER ICs: VOLTAGE-TO-FREQUENCY

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Input	Output	Nonlinearity (10kHz)	Quiescent Current	Temp. Range*	Package
AD537J	Low cost	±10V	0.001 to 100kHz	0.15% max	1.2mA	C	14 Pin DIP
AD537K	monolithic V/F	±10V	0.001 to 100kHz	0.07% max	1.2mA	C	14 Pin DIP
AD537S	converter	±10V	0.001 to 100kHz	0.07% max	1.2mA	M	14 Pin DIP

*Note: C = 0 to +70°C I = -25°C to +85°C M = -55°C to +125°C

CONVERTER MODULES: DIGITAL-TO-ANALOG

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Description ²	Model	Resolution	Linearity Error	Settling Time to % Accuracy for F.S. Step	Gain TC	Size (Inches)	Input Code Options ¹
General Purpose	DAC-10Z	10 bits	±0.05% max	5μs to ±0.05%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
	MDA-10Z	10 bits	±0.05% max	300ns to ±0.05%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC-12QZ	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±30ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC1118	12 bits/3 digits	±0.0125% max	5μs to ±0.01%	±30ppm/°C max	2 x 4 x 0.4	BIN, BCD, OBN, 2SC
	DAC1009	12 bits/3 digits	±0.0125% max	4μs to ±0.01%	±11ppm/°C	2 x 2 x 0.4	BIN, OBN, BCD
High Performance	DAC-8QS	8 bits/2 digits	±0.2%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC-10QS	10 bits	±0.05%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB
	DAC-12QS	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC-8QM	8 bits/2 digits	±0.2%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	DAC-10QM	10 bits	±0.05%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
	DAC-12QM	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	DAC1132	12 bits	±0.0125%	2μs to ±0.01%	±10ppm/°C max	2 x 2 x 0.4	BIN, OBN
High Speed	DAC-10DF	10 bits	±0.05% max	200ns max to ±0.05%	±50ppm/°C max	4.5 x 6	OBN, 2SC
	MDA-8F	8 bits	±0.2%	40ns to ±0.05%	±25ppm/°C	2 x 4 x 0.4	C-B, COB
	MDA-10F	10 bits	±0.05%	40ns to ±0.05%	±25ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1106-001	8 bits	±0.2%	25ns to ±0.2%	±10ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC1106-002	10 bits	±0.05%	50ns to ±0.05%	±10ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC1108	12 bits	±0.0125% max	150ns to ±0.01%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
High Resolution	DAC-14QG ⁴	14 bits	±0.003%	250μs to ±0.0015%	±7ppm/°C	4.5 x 4.75	BIN, OBN, 2SC, SMB
	DAC-16QG ⁴	16 bits/4 digits	±0.0015%	250μs to ±0.0015%	±7ppm/°C	4.5 x 4.75	BIN, OBN, 2SC, SMB, SMD, BCD
	DAC-14QM	14 bits	±0.003%	250μs to ±0.0015%	±15ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC-16QM	16 bits/4 digits	±0.0015%	250μs to ±0.0015%	±15ppm/°C	2 x 4 x 0.4	C-B, COB, CBD
	DAC1136J ⁵	16 bits	±0.0015%	18μs to ±0.0015%	±5ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1136K ⁵	16 bits	±0.00076%	30μs to ±0.00076%	±5ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1138J ⁵	18 bits	±0.00038%	60μs to ±0.00038%	±1ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1138K ⁵	18 bits	±0.00019%	230μs to ±0.00038%	±1ppm/°C	2 x 4 x 0.4	C-B, COB
Low Power	DAC1122J	12 bits	±0.01% max	20μs to ±0.01%	±30ppm/°C	2 x 3 x 0.4	BIN, OBN, C-B, COB
	DAC1122K	12 bits	±0.01% max	10μs to ±0.01%	±15ppm/°C	2 x 3 x 0.4	BIN, OBN, C-B, COB
Multiplying³	DAC-8M	8 bits	±0.2%	10μs to ±0.2%	±25ppm/°C max	2 x 2 x 0.4	BIN, OBN
	DAC-12M	12 bits	±0.02%	15μs to ±0.01%	±5ppm/°C max	2 x 2 x 0.4	BIN, OBN
	MDA-11MF	11 bits	±0.03%	1μs to ±0.01%	±30ppm/°C	2 x 4 x 0.4	BIN, OBN
	DAC1125	12 bits	±0.0125% max	3μs to ±0.01%	±3ppm/°C	2 x 2 x 0.4	C-B, OBN, 2SC
Herm. Sealed	MDA-12QD	12 bits	±0.0125%	3μs to ±0.01%	±15ppm/°C	1 x 1.5 x 0.4	C-B, COB
High Reliability	DAC1112	12 bits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB
	DAC1117	12 bits	±0.0125% max	4μs to ±0.01%	±15ppm/°C max	1 x 1.5 x 0.4	C-B, COB

CONVERTER MODULES: ANALOG-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Description ²	Model	Resolution	Linearity Error	Conversion Time	Gain TC	Size (Inches)	Output Code Options ¹
General Purpose	ADC-8S	8 bits/2 digits	±0.2% max	1ms max	±60ppm/°C	2 x 3 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10Z	10 bits	±0.05% max	20μs max	±40ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC-12QZ	12 bits	±0.0125% max	40μs max	±30ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
High Performance	ADC-8QM	8 bits/2 digits	±0.2%	18μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10QM	10 bits	±0.05%	22μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC-12QM	12 bits/3 digits	±0.0125%	25μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-8QU	8 bits/2 digits	±0.2%	6.4μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10QU	10 bits	±0.05%	8μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC-12QU	12 bits/3 digits	±0.025%	15μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC1133	12 bits	±0.0125% max	25μs max	±7.5ppm/°C	2 x 2 x 0.4	BIN, OBN, 2SC
Dual Slope	ADC1100	11 bits/3½ digits	±0.05% ±1 bit	42ms max	±50ppm/°C max	2 x 4 x 0.4	SMB, SMD
	ADC-14I	14 bits	±0.01% ±1 bit	40ms max	±5ppm/°C	3 x 4 x 0.4	SMB
	ADC-17I	4½ digits	±0.01% ±1 bit	40ms max	±5ppm/°C	3 x 4 x 0.4	SMD
	ADC1105J	up to 1:2,000	±0.1% ±1 bit	(depends on the resolution)	±20ppm/°C max	2 x 4 x 0.6	(any sign-magnitude code)
	ADC1105K	up to 1:20,000	±0.01% ±1 bit	(depends on the resolution)	±5ppm/°C max	2 x 4 x 0.6	(any sign-magnitude code)
High Speed	ADC1102	12 bits	±0.0125% max	8μs max	±10ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC1103-001	8 bits	±0.2% max	1μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
	ADC1103-002	10 bits	±0.05% max	1.5μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
	ADC1103-003	12 bits	±0.025% max	3.5μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
ADC1109	10 bits	±0.05%	4μs max	±30ppm/°C	2 x 3 x 0.4	BIN, OBN, 2SC	
High Resolution	ADC-16Q	16 bits	±0.0015%	400μs	±8ppm/°C max	4.5 x 6	BIN, OBN, 2SC
Low Power,	ADC-12QL/J	12 bits	±0.01%	85-130μs	±50ppm/°C max	3.65 x 4.1	BIN, OBN
	ADC-12QL/K	12 bits	±0.01%	85-130μs	±20ppm/°C max	3.65 x 4.1	BIN, OBN
	ADC1121	12 Bits	±0.0125% max	52μs max	±20ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
ADC1123	10 bits	±0.05% max	65-90μs	±40ppm/°C	3.65 x 4.1	BIN, OBN	
High Reliability	ADC1111	12 bits	±0.0125%	25μs max	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC

NOTES: 1. Logic Codes: BIN, binary; C-B, complementary binary; OBN, offset binary; COB, complementary offset binary; BCD, binary coded decimal; CBD, complementary BCD; 2SC, two's complement; SMB, sign-magnitude binary; SMD, sign-magnitude BCD.

2. Standard temperature range on most converters is 0 to +70°C, with storage temperature from -55°C to +125°C. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally -55°C to +125°C for 8 and 10 bit devices and -25°C to +85°C for 12 bit devices.

3. Analog input range of DAC-8M, DAC-12M, and DAC1125 is ±10V; input range of MDA-11MF is 0 to -10V.

4. Also available as a card mounted assembly with input code option (see DAC16QG) and output amplifiers model 44K or model 234L.

CONVERTER MODULES: DIGITAL-TO-SYNCHRO

SPECIFICATIONS (typical @ +25°C and ±15VDC and +5VDC unless otherwise noted)

	Input Resolution Bits	Accuracy (See Note) Arc-Min	Signal & Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Minimum Output Load Z _{LL} Ohms	Output VA	Size (See Note)	Temp Range (See Note)	Settling Time Micro-Sec
DSC1605511	14	±4	400	11.8	26	107	1.3	A	C	100
DSC1605512	14	±4	400	90	115	6200	1.3	A	C	100
DSC1605507 plus STM1634522	14	±4	60	90	115	6200	1.3	A plus E	C	100
DSC1605711	14	±4	400	11.8	26	107	1.3	A	M	100
DSC1605712	14	±4	400	90	115	6200	1.3	A	M	100
DSC1605707 plus STM1634722	14	±4	60	90	115	6200	1.3	A plus E	M	100
DSC1606511	10	±30	400	11.8	26	107	1.3	A	C	80
DSC1606512	10	±30	400	90	115	6200	1.3	A	C	80
DSC1606507 plus STM1633522	10	±30	60	90	115	6200	1.3	A plus E	C	80
DSC1606711	10	±30	400	11.8	26	107	1.3	A	M	80
DSC1606712	10	±30	400	90	115	6200	1.3	A	M	80
DSC1606707 plus STM1633722	10	±30	60	90	115	6200	1.3	A plus E	M	80
DSC1607517	16	±1	50-1000	7.5	2	2000	N/A	A	C	150
DSC1607717	16	±1	50-1000	7.5	2	2000	N/A	A	I	150

Sizes: A is 3.125" x 2.625" x 0.8"
E is 4.5" x 2.0" x 1.5"

Temp Ranges: C is 0°C to +70°C
I is -55°C to +85°C
M is -55°C to +105°C
full power to +85°C
½ power at +105°C

Accuracy applies: over operating temp range and ±10% reference frequency and amplitude changes and 10% harmonic distortion and ±5% power supply variation and any balanced load from no load to full load.

DSC1605 and DSC1606 models shown are synchro outputs. Consult factory for resolver versions.

DSC1607 is resolver form, without power amplifiers.

CONVERTER MODULES: SYNCHRO-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C and ±15VDC and +5VDC unless otherwise noted)

	Output Resolution Bits	Accuracy (See Note) Arc-Min	Signal Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Tracking Rate Deg/Sec	Acceleration for 1LSB Error Deg/Sec ²	Size (See Note)	Temp Range (See Note)	Frequency Range Hz
SDC160251Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	C	350-1500
SDC160261Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	M	350-1500
SDC1602507 plus STM1631522	14	±4	60	90	115	430	6	A plus D	C	50-450
SDC1602607 plus STM1631622	14	±4	60	90	115	430	6	A plus D	M	50-450
SDC160351Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	C	350-1500
SDC160361Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	M	350-1500
SDC1603507 plus STM1630522	10	±30	60	90	115	2880	48	A plus D	C	50-450
SDC1603607 plus STM1630622	10	±30	60	90	115	2880	48	A plus D	M	50-450
SDC1604507 plus STM163251Z	16	±1.3	400	11.8 or 90	26 or 115	360	60	A plus D	C	350-450
SDC1604707 plus STM163271Z	16	±2	400	11.8 or 90	26 or 115	360	60	A plus D	I	350-450
SDC178651Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	C	350-1500
SDC178661Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	M	350-1500
SDC1786507 plus STM1630522	10	±30	60	90	115	1260	850	A plus D	C	50-450
SDC1786607 plus STM1630622	10	±30	60	90	115	1260	850	A plus D	M	50-450
SDC170051Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	C	350-1600
SDC170052Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	C	50-1200
SDC170054Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	C	2300-2700
SDC170061Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	M	350-1600
SDC170062Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	M	50-1200
SDC170064Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	M	2300-2700
SDC170451Z	14	±5 ±1LSB	400	11.8 or 90	26 or 115	3240	720	B	C	350-1000
SDC170452Z	14	±5 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	C	50-500
SDC170461Z	14	±5 ±1LSB	400	11.8 or 90	26 or 115	3240	720	B	M	350-1000
SDC170462Z	14	±5 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	M	50-500

Sizes: A is 3.125" x 2.625" x 0.8"
B is 3.125" x 2.625" x 0.4"
D is 3.125" x 1.5" x 1.0"

Accuracy: Applies over operating temp range and ±10% frequency variation and ±10% signal and ref amplitude variation and 10% signal and ref harmonic distortion and ±5% power supply variation.

Consult factory for other options.

Temp Ranges: C is commercial 0°C to +70°C
I is industrial -55°C to +85°C
M is military -55°C to +105°C

Z is replaced by a number, when ordering, to specify input type:
Z = 1 signifies synchro, signal 11.8V, reference 26V
Z = 2 signifies synchro, signal 90V, reference 115V
Z = 8 signifies resolver, signal 11.8V, reference 26V

CONVERTER MODULES: FREQUENCY-TO-VOLTAGE

SPECIFICATIONS (Typical @ +25°C and $V_S = \pm 15\text{VDC}$ unless otherwise noted)

Model	10kHz Full Scale 451J (K) (L)	100kHz Full Scale 453J (K) (L)
Frequency Input		
Frequency Range	DC to 10kHz min	DC to 100kHz min
Overrange	10% min	10% min
Waveforms	← Sine, Square, Triangle, Pulse Train →	
Threshold	+1.4V	+1.4V
With External Adjustment	0V to ±12V	0V to ±12V
Hysteresis	±50mV	±100mV
Levels (TTL Compatible)	High Low	High Low
	+1.45V to +12V -12V to +1.35V	+1.5V to +12V -12V to +1.3V
Accuracy		
Nonlinearity		
$F_{IN} = 1\text{Hz to } 11\text{kHz}$	±0.03%(0.015%)(0.008%) max	—
$F_{IN} = 1\text{Hz to } 110\text{kHz}$	—	±0.03%(0.015%)(0.008%) max
Gain vs. Temperature (0 to +70°C)	±100 (50) (50) ppm/°C max	±100 (50) (50) ppm/°C max
Response		
Step Response to ±0.5% of Final Value		
$F_{IN} = \text{DC to Full Scale}$	4ms	0.8ms
$F_{IN} = \text{Full Scale to DC}$	30ms	4ms
Output		
Voltage ($F_{IN} = \text{Full Scale}$)	+9.85V min; +9.95V max	+9.85V min; +9.95V max
Current ($E_O = +10\text{V}, -10\text{V}$)	(+20, -2)mA min	(+20, -2)mA min
Offset Voltage @ +25°C	±7.5mV max	±7.5mV max
vs. Temperature (0 to +70°C)	±30μV/°C max	±30μV/°C max
Power Supply		
Voltage, Rated Performance	±15VDC	±15VDC
Current, Quiescent	(+10, -8)mA	(+10, -8)mA
Temperature Range		
Rated Performance	0 to +70°C	0 to +70°C
Case Size	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"

CONVERTER MODULES: VOLTAGE-TO-FREQUENCY

SPECIFICATIONS (typical @ +25°C and $V_S = \pm 15\text{VDC}$ unless otherwise noted)

Model	Economy 10kHz 456J (K)	High Performance 10kHz 450J (K)	Versatile 20kHz 454J (K)	Economy 100kHz 452J (K) (L)	Low Drift 100kHz 458J (K) (L)	Low Drift 1MHz 460J (K) (L)
Analog Input						
Voltage Signal Range	0 to +10V, min	0 to +10V, min	0 to +20V, min	0 to +10V, min	0 to ±10V, min	0 to ±10V, min
Current Signal Range	—	—	0 to +0.67mA, min	0 to +0.5mA, min	0 to +0.5mA, min	0 to +1.0mA min
Overrange	50%, min	50%, min	10%, min	10%, min	10%, min	10%, min
Accuracy						
Nonlinearity, max						
Voltage Input	±0.03%(±0.2%)	±0.01%(±0.005%)	±0.01%(±0.005%)	±0.015%	±0.01%	±0.015%
Current Input	—	—	±0.01%(±0.005%)	±0.015%	±0.01%	±0.015%
Gain vs. temperature, ppm/°C, max	±120(±80)	±50(±25)	±50(±25)	±150(±100)(±50)	±20(±10)(±5)	±50(±25)(±15)
Input Offset Voltage	±10mV	±5mV, max	±5mV, max	±7.5mV, max	±10mV, max	±10mV, max
vs. Temperature (0 to +70°C)	±100μV/°C	±50(±25)μV/°C, max	±50(±25)μV/°C, max	±30μV/°C, max	±30μV/°C, max	±30μV/°C, max
Response						
Settling Time	120μs	120μs	120μs	22μs	22μs	15μs
Overload Recovery	15ms	15ms	22ms	1.5ms	10ms	1ms
Output						
Waveform	← TRAIN OF TTL/DTL COMPATIBLE PULSES →					
Pulse Width	50μs	50μs	25μs	6μs	5μs	0.5μs
Pulse Polarity	← POSITIVE →					
Logic "1" (HIGH) Level	← +2.4V, min →					
Logic "0" (LOW) Level	← +0.4V, min →					
Power Supply						
Voltage, Rated Performance	← ±15VDC →					
Current, Quiescent	(+15, -9)mA	(+15, -9)mA	(+15, -9)mA	(+25, -10)mA	(+25, -8)mA	(+35, -8)mA
Temperature Range						
Rated Performance	← 0 to +70°C →					
Case Size	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	2" x 2" x 0.4"	2" x 2" x 0.4"

IC SAMPLE-HOLD AMPLIFIERS

SPECIFICATIONS (typical @ +25°C)

	AD582K	AD582S	AD583K
Open Loop Gain $R_L = 2k\Omega$	25k min	25k min	25k min
Output Swing	$\pm 10V$ min	$\pm 10V$ min	$\pm 10V$ min
Gain Bandwidth	1.5MHz	1.5MHz	2MHz
Acquisition Time (0.1%) $A_V = 1, R_L = 2k, C_L = 50pF$	5 μ sec	5 μ sec	4 μ sec
Aperture Time	150nsec	150nsec	50nsec
Drift Current	50pA max	50pA max	50pA max
Charge Transfer	5pC max	5pC max	20pC max
Operating Temp.*	C	M	C

*C = 0 to +70°C; M = 55°C to +125°C

MODULAR SAMPLE-HOLD AMPLIFIERS

SPECIFICATIONS (typical @ +25°C)

Model	Product Classification	Acquisition Time To % Accuracy	Drop Rate	Aperture Delay	Aperture Jitter	Input Resistance	Size (inches)
SHA-1A SHA1134	General Purpose	5 μ s max to $\pm 0.01\%$ 3.4 μ s to $\pm 0.01\%$	$\pm 50\mu V/ms$ max $\pm 50\mu V/ms$	40ns max 50ns max	5ns max 5ns max	$10^{12}\Omega$ $10^7\Omega$ min	2 x 2 x 0.4 1.125 x 2 x 0.4
SHA-2A	High Speed	500ns max to $\pm 0.01\%$	$\pm 10\mu V/\mu s$	10ns	0.25ns	$10^{11}\Omega$	2 x 3 x 0.4
SHA-3 SHA-4	Low Droop	75 μ s to $\pm 0.01\%$ 75 μ s to $\pm 0.01\%$	$\pm 10\mu V/ms$ $\pm 10\mu V/ms$	50ns 50ns	5ns 5ns	$10^8\Omega$ $10^8\Omega$	1.125 x 2 x 0.4 1.125 x 2 x 0.4
SHA-5	Low Cost	15 μ s max to $\pm 0.01\%$	$\pm 20\mu V/ms$	40ns	4ns	$4 \times 10^9\Omega$	1.125 x 2 x 0.4
SHA-6	High Resolution	5ms max to $\pm 0.00075\%$	$\pm 10\mu V/ms$ max	-1.7 μ s	10ns	$10^9\Omega$ min	2 x 4 x 0.4
SHA1114	High Reliability	500ns max to $\pm 0.01\%$	$\pm 100\mu V/\mu s$ max	10ns	0.25ns	$10^{11}\Omega$	2 x 3 x 0.5

NOTES

¹ Gain of all SHA's is +1 except that the SHA-6 and SHA-2A can be connected for gains greater than unity: the SHA-2A can also be operated in the inverting mode.

² SHA-3 and SHA-4 differ only in that the SHA-4 settles much faster when switched from HOLD to SAMPLE. Settling time to $\pm 1mV$ is 100 μ s for SHA-3 and 20 μ s for SHA-4.

CMOS MULTIPLEXERS

SPECIFICATIONS ($T_A = +25^\circ C$, $V_{SUPPLY} = \pm 15V$ unless otherwise noted)

Type ¹	Function	R_{ON}	Out Leakage	Temp ² Range	Package
AD7501JN/JD AD7501KN/KD AD7501SD	8-Channel MUX	300 Ω , max	10nA, max 10nA, max 5nA, max	C/I C/I M	16-pin DIP
AD7502JN/JD AD7502KN/KD AD7502SD	Dual 4-Channel MUX	300 Ω , max	5nA, max 5nA, max 3nA, max	C/I C/I M	16-pin DIP
AD7503JN/JD AD7503KN/KD AD7503SD	8-Channel MUX	300 Ω , max	10nA, max 10nA, max 5nA, max	C/I C/I M	16-pin DIP
AD7506JN/JD AD7506KN/KD AD7506SD/TD	16-Channel MUX	450 Ω , max 450 Ω , max 400 Ω , max	20nA, max 20nA, max 10nA, max	C/I C/I M	28-pin DIP
AD7507JN/JD AD7507KN/KD AD7507SD/TD	Dual 8-Channel MUX	450 Ω , max 450 Ω , max 400 Ω , max	10nA, max 10nA, max 5nA, max	C/I C/I M	28-pin DIP

¹ Suffix "N": plastic; Suffix "D": ceramic

² C: Commercial (0° to +70°C)

I: Industrial (-25°C to +85°C)

M: Military (-55°C to +125°C)

MODULAR MULTIPLEXER

SPECIFICATION SUMMARY (typical @ +25°C)

Model	MPX-8A
Channels	
Single-Ended	8 ¹
Differential	4
Voltage Range	
Rated Operation	±10V
Overload Protection	±15V
Transfer Error	
Settling to 0.01%	0.01%
Cross Channel Coupling	<2μs
Common Mode Rejection	<-80dB
DC	120dB
60Hz	106dB
Package Dimensions	2" x 2" x 0.4"

¹MPX-8A includes logic for expansion to 64 channels.

CMOS SWITCHES

SPECIFICATIONS (T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type ¹	Function	R _{ON}	Off Leakage	Temp ³ Range	Package
AD7510DIJN/JD	Quad SPST Note 2	100Ω, max	5nA, max	C/I	16-pin DIP
AD7510DIKN/KD			5nA, max	C/I	
AD7510DISD			3nA, max	M	
AD7511DIJN/JD	Quad SPST Note 2	100Ω, max	5nA, max	C/I	16-pin DIP
AD7511DIKN/KD			5nA, max	C/I	
AD7511DISD/TD			3nA, max	M	
AD7512DIJN/JD	Dual SPDT Note 2	100Ω, max	15nA, max	C/I	14-pin DIP
AD7512DIKN/KD			15nA, max	C/I	
AD7512DISD/TD			9nA, max	M	
AD7513JN/KN	Dual SPST	80Ω, max	5nA, max	C	14-pin DIP
AD7513JH/KH		80Ω, max	5nA, max	I	TO-100
AD7513SH/TH		70Ω, max	2nA, max	M	TO-100
AD7516JN/KN	Quad SPST Note 4	400/280Ω, max	100pA	C	14-pin DIP
AD7516 SD/TD		400/280Ω, max		M	
AD7519JN	Quad SPST Current Switch Note 5	100Ω, max	50nA	C	14-pin DIP

¹Suffix N: plastic/Suffix D: ceramic/Suffix H: TO-100

²Dielectrically isolated-features latch free, overvoltage proof operation

³C: Commercial (0°C to +70°C)

I: Industrial (-25°C to +85°C)

M: Military (-55°C to +125°C)

⁴VDD - VSS (supply voltages) = +15V

⁵VDD (supply voltage) = 8V

IC REFERENCES

SPECIFICATIONS

Model	Output Voltage	*Error, mV max T _{min} , T _{max}	Temp Range††
AD580J	2.500 ±3%	±90	C
AD580K	2.500 ±2%	±57	C
AD580L	2.500 ±2%	±54.3	C
AD580M	2.500 ±1%	±26.75	C
AD580S	2.500 ±3%	±100	M
AD580T	2.500 ±2%	±61	M
AD580U	2.500 ±1%	±29.5	M
AD2700L/U	10.000 ±0.025%	±5	I/M
AD2701L/U	-10.000 ±0.025%	±5	I/M
AD2702L/U	±10.000 ±0.025%	±5	I/M

*Including initial offset.

††C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with compatible multiplexer and sample-hold

Reviewing the available A/D converters, we find ADC-12QM to be a possible choice. The ADC-12QM completes a conversion in 25 μ s. For sample-hold, the compatible SHA-1A is chosen, adding 5 μ s of settling time. Thus, the combination appears to be amply capable of meeting the 50 μ s/channel scanning requirement. Since the multiplexer will scan sequentially, its settling time is inconsequential. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least 25 μ s to settle before a measurement is called for. For convenience, one may use the MPX-8A; the small 2" x 2" x 0.4" module fits into the packaging concept, and the built-in complete binary-address decoding makes it easy to work with.

ERROR ANALYSIS

It's clear that the MPX-8A, the SHA-1A, and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst-case situation is within the allowable 0.1% system error.

Multiplexer

The switches of the MPX-8A, being MOSFET's, with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.

Leakage current @ 25°C	10nA
Source impedance	10 Ω
Error voltage = $10 \times 10 \times 10^{-9}$	= 10^{-7} V (negligible)

2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the SHA-1A:

ON resistance	1000 Ω maximum
SHA-1A R_{in}	10^{12} Ω
Divider ratio attenuation error:	10^{-9} (negligible)

Sample-Hold

1. Nonlinearity is 2mV over the 20V range, or 0.01%
2. Gain error of 0.05% maximum (and other similarly small initial gain errors in the system) may be compensated for overall when calibrating the system by setting the scale constant of the ADC. It is not considered as part of the error budget.
3. Input bias current of 10nA (max) causes an offset error voltage in the source resistance.

Source resistance = 10 Ω (source) + 1k Ω (MPX switch)
Offset error = $10^3 \times 10^{-8}$ = 10 μ V (negligible)

4. Offset vs. temperature = 25 μ V/°C

Since the temperature inside the housing may change by as much as 30°C, the total change over the range will be

$$25 \times 30 = 750\mu\text{V, or } 75 \text{ ppm of } \pm 10\text{V}$$

An offset adjustment is provided for initial trimming.

5. Offset vs power supply = 100 μ V/% ΔV_s

Since the supply may vary by 150mV or 1% of 15V, the error contribution is 100 μ V, or 0.001% of full scale.

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate-and settling-time allowances. However, the components selected for this example have more than adequate settling time, even for 0.01% operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Converter

1. Specified linearity error (relative accuracy) $\frac{1}{2}$ LSB, or 0.0125%
2. Quantizing uncertainty: $\frac{1}{2}$ LSB, or 0.0125%. This is a resolution limitation, not normally considered in the error budget.
3. Temperature errors
 - a. Gain temperature coefficient: 5ppm/ $^{\circ}$ C for 30 $^{\circ}$ C
 $5 \times 30 = 150$ ppm, or 0.015%
 - b. Zero temperature coefficient: 5ppm/ $^{\circ}$ C for 30 $^{\circ}$ C
 $5 \times 30 = 150$ ppm, or 0.015%
4. Power supply sensitivity error: 0.002%/ $\% \Delta V_s$
For a 1% shift, the error is 20ppm
5. Differential nonlinearity temperature coefficient, 3ppm/ $^{\circ}$ C.
For 30 $^{\circ}$ C temperature change, error is 90ppm, less than $\frac{1}{2}$ LSB. Therefore, 12-bit monotonicity can be maintained, with no missing codes.

In this example, the worst-case arithmetic sum of these errors is 0.07%, and the rms sum is 0.03%. Since these values are reasonably conservative for a system with specified error of 0.1%, the designer may either rest with these choices and go on to the more-difficult hardware, software, interface, and wiring problems, or — if absolute-minimum cost or size of conversion hardware is an important objective — seek to reduce cost by considering a perhaps more marginal design.

Two approaches might be considered. The first would use integrated-circuit components, such as the AD572 12-bit A/D converter, the AD582 or AD583 sample-hold, and the AD7501 or AD7503 multiplexer. The compromises that this approach makes necessary would have to be determined and negotiated in terms of the advantages gained. On the other hand, one might consider a product embodying a higher level of integration, such as the DAS1128 data-acquisition subsystem (Chapter I-4). The advantages gained by this approach would include the consolidation of a number of specifications, the elimination of a number of system-design details, and possible savings in both space and initial cost.

CONCLUSION

In this chapter, we have sought to help the designer in his process of choosing a converter by providing checklists of relevant questions in making a choice, definitions of specifications and related features, a selection guide, and an example of selection and evaluation. We now go on to some considerations for what must be done to make the system work as expected.

II

Applying Converters Successfully

Chapter II-6

In Chapter 5, it was pointed out that, considering the many different types of converters on the market, the complex manner in which converter specifications relate to a specific system application, and the fact that prices of converters range from less than \$10 to several hundreds of dollars, selecting the most economical converter for an application is not a simple task. To make the most appropriate converter choice requires that the user consider a number of questions: What are the real objectives of the conversion process, and how do they relate to the converter's specifications? How may the system be configured to relax the converter's performance (and price) requirements, and at what overall cost? How will the other system components limit and degrade the converter's performance? What tradeoffs are available in the system error budget? Is it more economical to make a long-term choice of one "general-purpose" converter, which will meet the needs of a large number of system designs, or to go through an optimum selection process for each individual application?

In this chapter, we will discuss system aspects of selecting converters, a continuation of the discussion in the last chapter.

After selecting the appropriate converter, the user should be fully aware that the thorough preliminary analysis and economic component choice usually involved is not by itself sufficient to ensure that the system performance needs will be met. The system designer must take into account the physical surroundings, interconnections, grounding and power supplies, protection circuitry, and all the other details that constitute good engineering practice.

While these few pages cannot (and are not intended to) be a primer on engineering practice, it is useful for the converter user to become aware of those elements of practice that are of particular relevance to converter-system design.

MAKING THE PROPER SYSTEM CHOICES

A general rule of thumb used by some designers may be expressed as follows: "As the converter performance requirements approach state-of-the-art converter capabilities in *both speed and accuracy*, the price of the converter will increase exponentially." The user may expect substantial cost savings if he can relax either of these parameters.

Data-Acquisition Systems

An example will serve to illustrate the process of elimination and winnowing that can be profitably employed to determine a converter's minimum performance requirements. Figure 1 shows, in the simplest terms, a block diagram of an analog data-acquisition system, the primary application for which A/D converters are used.

The data-acquisition system, under the direction of the control unit, selects the multiplexer input points, one at a time, and directs the signal appearing on each point to the analog input of the A/D converter via the associated multiplex channel. The signal level is encoded by the converter and outputted to storage. The storage unit retains each piece of data in a pre-determined format, and holds it for further processing.

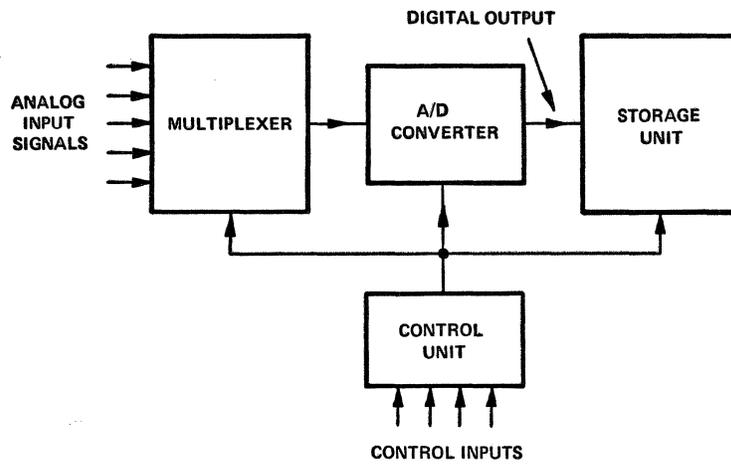


Figure 1. Data-acquisition system.

Three Classes of Converter Specifications

In attacking the problem of determining the converter performance requirements, it is useful to divide the converter specifications into three classes: Those that determine accuracy under optimum conditions, those that are dependent on time (or speed of response), and those that are substantially affected by the environment.

In the first class are included resolution, relative accuracy, differential linearity, noise, quantization uncertainty, monotonicity, and differential-linearity temperature coefficient. The reason this last term is included, though it would appear to be an environmental specification, may be somewhat unexpected: Although the ambient temperature may be in the steady state, it can be elevated (e.g., 25°C above normal room temperature) by virtue of enclosure in a cabinet. Although calibration *in situ* can correct for errors produced by variation of gain and offset with temperature, no correction can normally be effected for errors characterized by the differential-linearity T.C., due to individual bit variations with temperature. For this reason, the differential-linearity error at 25°C is augmented by the product of the steady-state temperature rise and the differential-nonlinearity temperature coefficient.

Speed-dependent specifications in the second category include conversion time, bandwidth, settling time of the input circuitry, etc. Environment-related specifications in the third category include gain (i.e., scale-factor) T.C., offset T.C., limits of the operating temperature range, etc.

Approaches to Relaxing the Specifications

Relaxation of the specifications in the first class may be effected through the use of signal conditioners. Choice of the specific form signal-conditioning may take is based on our knowledge of the input signals to be encoded and the information to be extracted from the encoded data. Known or unwanted signal components may be extracted from the input signals, and the peak-to-peak variation of the remaining signals may be scaled to equal the input voltage range of the A/D converter with an analog subtractor having adjustable gain. For example, if the signal conditioner is a differential instrumentation amplifier, such as the Model AD521 or AD522, it may be used to bias out dc offsets, and to scale the input appropriately (Figure 2).

The level-shifting-and-scaling operation can be used to obtain efficient use of the converter's input range. By scaling, voltage increments in the original signals that were less than 1 LSB of the converter's input voltage range may be measured.

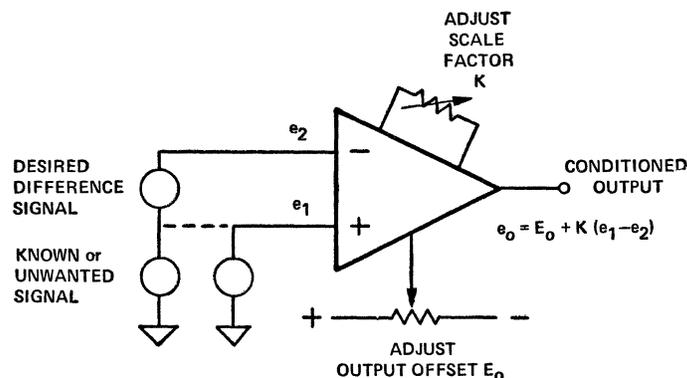


Figure 2. Differential instrumentation amplifier as a signal conditioner for data acquisition.

Logarithmic Compression

In applications calling for wide dynamic signal range but capable of tolerating constant fractional error (e.g., 1% of actual value), rather dramatic efficiency can be realized through the use of logarithmic amplifiers for data compression, as shown in Figure 3. Here, a logarithmic amplifier allows encoding of signals, that would ordinarily require a minimum of 20-bit conversion to handle the dynamic range, with a far-less-costly 12-bit converter. Modest accuracy in a fixed ratio to (e.g., % of) actual value is substituted for extreme accuracy in relation to the entire full-scale range, at considerably less cost. For many applications this is an ideal performance mode, except for those applications in which extremely small errors are required at all points in the range (e.g., measuring long-term stability of voltage sources). The logarithmic data can be dealt with easily if the data is to be processed digitally; or it can be recovered in linear analog form (if it is simply to be stored or transmitted digitally) by the use of another log amplifier, in the antilog connection, with a D/A converter.

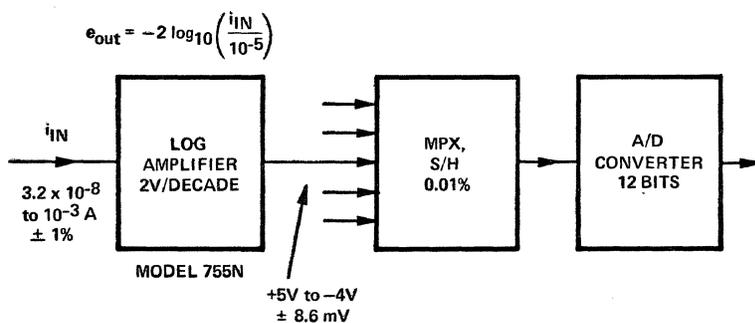


Figure 3. Using a log amplifier for range compression in a data-acquisition system.

Filtering

Another commonly-used signal-conditioning unit is the filter. Low pass filters are used to extract carrier, signal, and noise components, above the frequencies of interest, from the input signals. These components appear as noise if the converter is unable to follow them. A/D converters often incorporate follower circuits for impedance buffering. With a modicum of external wiring, they can be connected as active low-pass filters. (Figure 4)

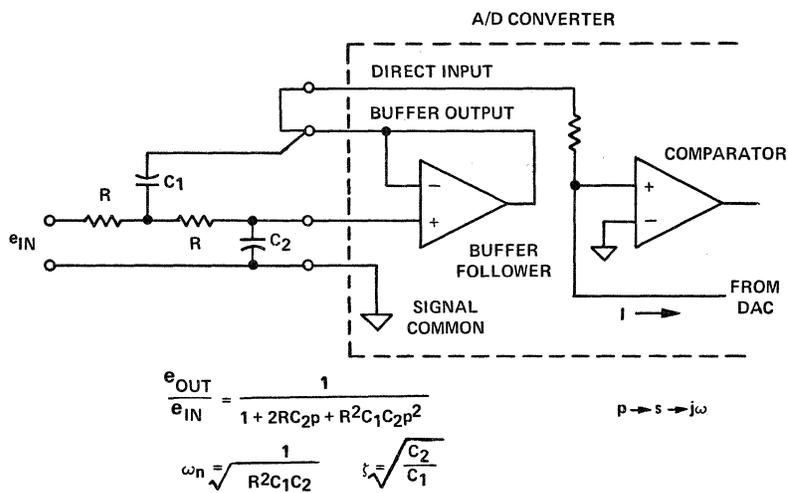


Figure 4. Input buffer of an A/D converter connected as an active low-pass filter.

Sample-Hold

A relaxation of the second class of specifications can also be effected by adding a sample-and-hold amplifier to the system configuration, as depicted in Figure 5.

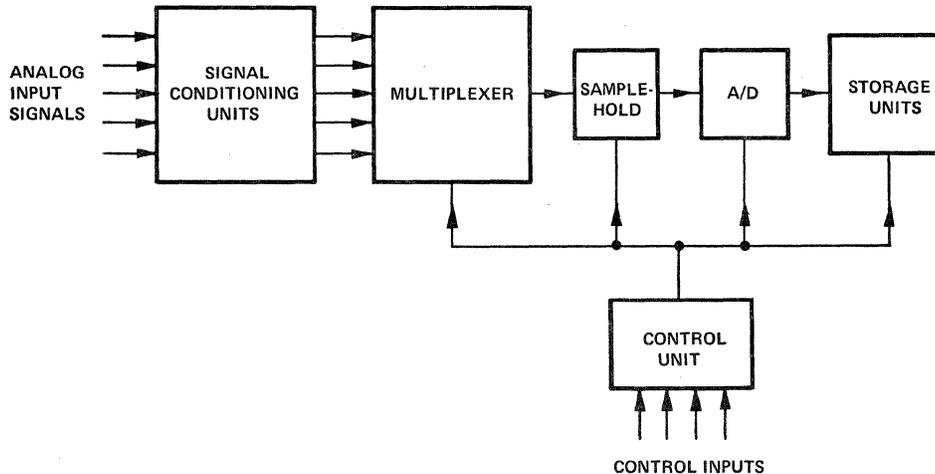


Figure 5. Data-acquisition system with sample-and-hold and input pre-conditioning.

The use of a sample-and-hold amplifier can increase the system throughput rate and increase the highest-frequency signal, of a given amplitude, that may be encoded within the resolution of the converter. The system throughput rate, without the sample-and-hold, is determined primarily by the multiplexer's settling time, plus the A/D converter's conversion time.

The multiplexer settling time is the time required for an analog signal to settle to within its share of the system error budget, as measured at the input to the converter, after selection by the multiplexer. For a 12-bit conversion system, with a $\pm 10V$ range, multiplexers typically settle within $1\mu s$, and typical conversion times are $20\mu s$. The sample-and-hold can be used to hold the last channel's signal level for conversion, while the next channel is selected and settles. Since sample-and-hold amplifiers with acquisition times of less than $5\mu s$ to within 0.01% are readily available, the throughput time can be reduced to approach the conversion time. Pairs of sample-and-holds and A/D converters can be used for alternate conversions to increase throughput rate even further, though at considerable increase in cost.

The following example indicates the improvement possible with a sample-and-hold: If the input is a full-scale sine wave, $E_{FS}\sin(2\pi ft)$, the maximum rate-of-change is at zero, and (as can be

found by differentiating with respect to t) equal to $2\pi f E_{FS}$. If the change is to be less than 1 LSB in the conversion time, the highest frequency that can be applied is

$$f_{\max} = \frac{\Delta E}{E_{FS}} \frac{1}{2\pi \Delta t}$$

For a 12-bit converter with a $20\mu\text{s}$ conversion time, $f_{\max} \approx 2\text{Hz}$! Using a sample-and-hold, one can reduce the uncertainty in the time of measurement from the ADC's conversion time to the aperture time of the sample-and-hold, thus effecting an improvement in f_{\max} by the ratio of the conversion time to the aperture-time uncertainty.

Since 20ns or better is routinely available in sample-and-holds designed for operation with 12-bit converters, an improvement of 1000:1 is quite feasible, assuming that the S/H has adequate bandwidth.

If the speed of A/D conversion is significantly limited by the settling time of the input buffer-follower, the sample-and-hold may be connected to bypass it, providing an even greater increase in throughput rate.

Relaxation of the third class of errors, those due to environment-related specifications, may be abetted by allotting one multiplexer channel to carry a ground-level signal, and another to carry a precision reference-voltage level that is near-full scale. Data obtained from these channels may be used by a processor to correct gain and offset variations common to all channels, generated in the sample-and-hold, the A/D converter, and the associated wiring.

Contributions to Error

The decision to seek means of relaxing the required specifications is based on the availability and cost of devices that meet the original specifications, as compared to the cost of alternatives and any additional problems engendered by departing from a straightforward approach. To evaluate the performance tradeoffs, an error budget is a useful tool.

Three classes of errors should be considered:

- Errors due to the non-ideal nature of each component
- Errors due to the physical interconnections of the system components
- Errors due to the interaction of system components.

The first group of errors can be determined from the spec sheets for the system components. The second group result from parasitic interactions that are a function of the way the interconnections are managed, e.g., grounding, shielding, contact resistance, etc. The third group result from specific interactions between components in the system; though they are not specifically called out in spec sheets, they can be predicted from careful reading of the specifications of the individual devices, or from the user's knowledge of how they are designed. An example of this class of error sources might be the offsets created by series impedances in the signal path (signal-source impedance, multiplexer-switch *on* impedance) and the bias and leakage currents of the stages following these impedances, to which they are connected. A second example might be disturbances caused at the signal source as the multiplexer switches it into the circuit.

By showing where the important contributions to error lie, the error budget is used as a tool for establishing tradeoffs to set the final performance requirements for the system. The error budget can be used as a tool in predicting the overall expected error, whether by worst-case summation, by root-sum-of-the-squares summation, or by combinations of the above using specific knowledge of possible compensations and common sense.

INSTALLATION AND GROUNDING

The current popularity of module and IC converters make it worthwhile to consider some elements of their design.

For one thing, many types are “customer-programmable.” This means that the customer may select one of several possible signal voltage ranges by choosing the appropriate jumper-wiring configuration at the module’s terminals. It goes without saying that all terminals used to determine the signal voltage range involve analog signals; to protect their low resolution levels, they should be kept away from circuit-card etch runs that carry logic signals.

Customer-programmable inputs also permit modification by the connection of external resistors, in addition to the jumpering mentioned above. Care should be exercised in doing this, for the reasons mentioned above. In addition, it should be noted that the excellent gain and offset T.C.’s of these devices are achieved by depending, not on absolute stability with temperature, but rather on the close tracking with temperature of key resistors within the module. Therefore, even if $0\text{ppm}/^\circ\text{C}$ TCR resistors are used externally, the overall gain and offset performance vs. temperature may be appreciably degraded. Since there may be ways of avoiding excessive errors, the manufacturer should be consulted before external resistors are “frozen” into the design. It may also be helpful to read about resistor tracking in actual designs, as covered in Chapters II-2 and II-3.

In the design of the converter module, great care is taken to separate the analog and digital signal lines. This procedure should also be followed with the external layout of the board on which the converter is mounted. Etch runs of digital signal lines should not run parallel in close proximity with etch runs of analog signal lines. If these lines must cross, they should do so at right angles. Particular care should be taken with low-level high-gain points, e.g., the comparator input on A/D converters and the summing junction of the output amplifier on D/A converters. Etch runs to these points should be as short as possible and should not create loops. Analog-ground guard runs may also help reduce interference.

Grounding

Converter modules (actually, most data-acquisition components) have a number of ground terminals, which are not connected together within the module. These “grounds” are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground (or Sense). These grounds must be tied together at one point, the system “mecca,” usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts could be generated between the system mecca point and the ground terminal of the module. Separate ground returns are provided to minimize the current flow in the path from sensitive points to the system mecca point. In this way, supply currents do not flow in the same return path with analog signals, and logic-gate return currents are not summed into the return from a precision reference-zener diode. (Figure 6)

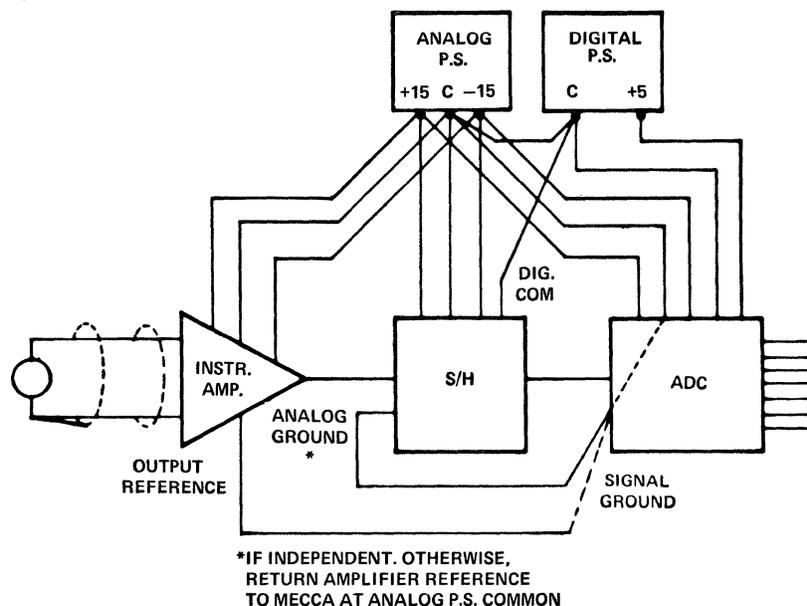


Figure 6. Basic grounding practice.

In any event, the connections between the system mecca point and the ground terminals should be as short as possible and should have the lowest feasible impedance.

Each of the module's supply terminals should be capacitively decoupled as close to the module as possible. A large-value capacitor with a high resonant frequency should be used. A $15\mu\text{F}$ solid-tantalum capacitor is usually sufficient. Analog supplies are bypassed to the module's analog power return terminal, and the logic-supply terminal is bypassed to the logic power return terminal.

When gain and offset adjustments are available and are intended to be used, the potentiometers with which they are performed should be mounted (with short leads) in such a position that they will be accessible when the mounting board is installed in the system.

The same care should be taken to locate a converter properly within a system as is taken to mount a module on its circuit board. A converter should never be located near a transformer or fan blower motor. Using mu-metal shielding to protect against electromagnetic and RFI pickup is an expensive and not-always-successful proposition. D/A converters should be located at their loads. This may require long cable runs for the digital control signals; however, the reduction in noise pickup and ground-potential differences between the D/A's output and the load can easily justify the expense. Similarly, A/D converters should be located near the signal source when possible. Since this is not always possible, one suggestion is to use a differential amplifier to receive the signal at the end of a long cable run before presenting it to the A/D converter. When the system is laid out, unshielded analog signal lines should never run in channels with either digital signal lines or power lines.

Reducing Common-Mode Errors

As we have indicated, a differential amplifier may be used to eliminate ground-potential differences in various parts of the system in which the converter is used. In Figure 7, the signal source is a remotely-located transducer, and the differential amplifier is located near the A/D converter. The common-mode signal is the potential difference between the ground signal at the converter and the ground signal at the transducer, plus any undesirable common-mode signal produced by the transducer, and any voltages developed across the unbalanced impedances of the two lines.

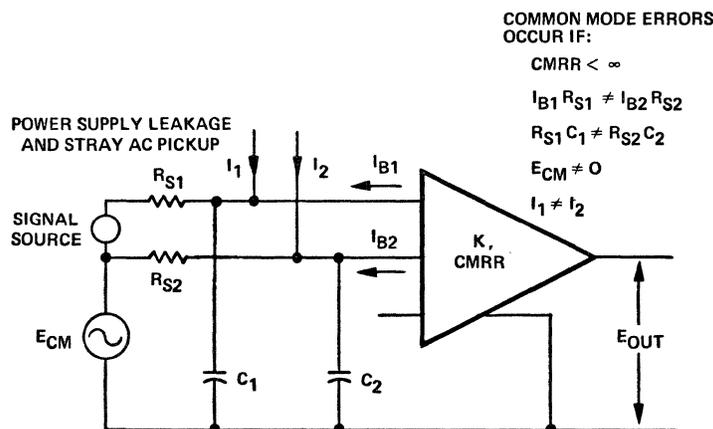


Figure 7. Common-mode and the difference signals due to line unbalance.

If the signal source is the output of the system's D/A converter, the differential amplifier would be located near the remote load. The common-mode signal is developed by the differences in ground potential at the two locations.

The amount of dc common-mode offset that is rejected depends on the CMRR of the amplifier. However, bias currents flowing through the signal source leads can cause offsets if either the bias currents or the source impedances are unbalanced. DC CMRR specifications generally include a specified amount of source unbalance (e.g., $1\text{k}\Omega$). Such specifications also indicate a top frequency for which the dc spec is valid, usually the line frequency (50-

60HZ), but sometimes 100HZ. At higher frequencies, unbalanced RC time constants (balanced or unbalanced series resistance and shunt capacitance to common, plus the amplifier's internal unbalances) reduce the common-mode rejection, by producing a quadrature normal-mode signal. This source of error can be greatly reduced by proper use of a guard shield, as shown in Figure 8.

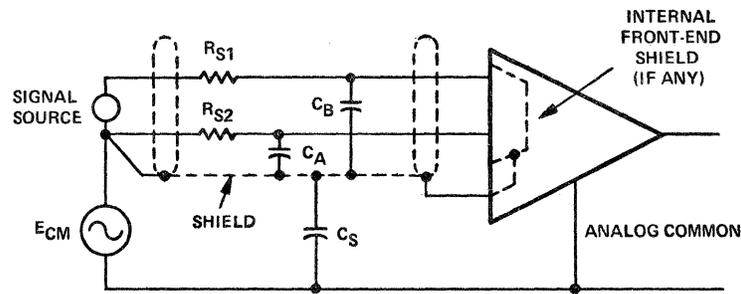


Figure 8. Use of guard shield to improve common-mode rejection at higher frequencies.

Here, no part of the common-mode signal appears across the capacitors C_A and C_B , since the shield is driven by the source of the common-mode signal. The shield also provides electrostatic shielding to minimize coupling to other signal lines in close proximity to the input leads.

When installing a guard shield, it is important that the guard shield connect only at one point to the source of the common-mode signal and that the shield be continuous, i.e., through multiplexers, connectors, patch panels, etc. Since the shield is carrying a common-mode signal, it should be properly insulated to prevent it from shorting to other shields or the earth ground. A final precaution that should be taken is to make sure that a conductive return path exists for the bias and leakage currents of the differential amplifier (unless it has transformer or optically-isolated, floating inputs).

It is helpful, in reducing noise and improving common-mode rejection, to connect the largest tolerable capacitance *between* the input leads. It will provide some filtering, and will reduce the capacitive unbalance by more than its ratio to the stray capacitance. (Figure 9)

In portions of a system where differential amplifiers are not used, sufficient precautions should be taken to insure that voltages are not induced in ground return leads to the single-point ground, and that the system is free from ground loops.

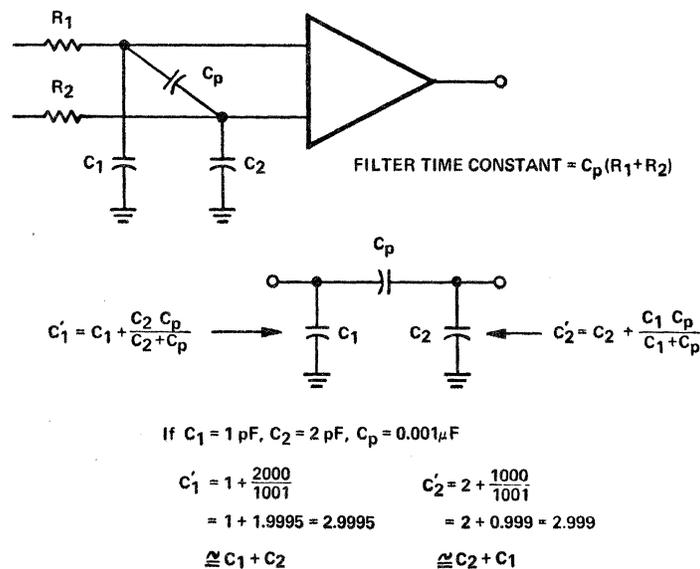


Figure 9. Capacitance between the input leads to reduce unbalance and provide filtering.

HOW TO ADJUST ZERO AND GAIN OF CONVERTERS

Many converter types are pretrimmed and require no adjustments as purchased to meet specified accuracy. For those cases where adjustments are called for, or where cost-savings can be effected by trimming inexpensive pre-trimmed devices, with modest specs, for use over narrow ranges for better-than-specified accuracy, or where long-term corrections are necessary during years of operation, here are some general principles of adjustment for converters. Naturally, the user should follow the specific instructions on product data sheets, especially where they conflict with these general guidelines.

Proper adjustment of zero and gain in DAC's and ADC's is a procedure that requires great care, and the use of extremely sensitive reference instruments. The voltmeter used to read the output of a DAC, or the voltage source used as a driving signal for the ADC, must be capable of stable and clear resolution of $1/10$ LSB at both ends of the range of the converter; e.g., at zero and full scale.

Most DAC's and successive approximation ADC's manufactured by Analog Devices are provided with Zero and Gain adjustments *which are completely independent of each other*, as long as the adjustment of Zero is attempted *only* when the actual conversion circuit is producing Zero, and as long as the Zero (or Offset) adjustment is accurately completed before proceeding to adjustment of Gain (at full scale – 1 LSB). Of course, it is possible to make Zero and Gain adjustments in reverse order and at other points on the transfer function – but it must be expected that the adjustments will no longer be independent, and the procedure will require a series of successive approximations.

Adjustment Process

Particularly for bipolar converters, fast and successful adjustment requires knowledge of the technique used in the circuit to convert the inherently unipolar DAC or ADC for bipolar operation.

1. Sign & Magnitude Codes are generally obtained by use of a unipolar converter with separate means of reversing polarity. The Zero adjustment is always made by calling for a zero from the converter. (Logic zero into a DAC produces zero volts output, or zero volts into an ADC produces data-zero output.)

2. Bipolar binary converters utilizing offset binary or two's complement coding usually employ analog offsetting to convert a unipolar design into bipolar. For instance, a 0 to +10V DAC may have its output amplifier offset by -5V, resulting in an output of -5 volts corresponding to 000000 input and +5 volts (minus 1 LSB) corresponding to a 111111 input. *Such a converter should have its "Zero" adjusted at -5V (100000 in 2's complement)*

An alternate explanation is as follows: converter Zero controls should always be set at the "All Bits Off" condition, and then Gain should be set at the "All Bits On" condition.

Adjustment For DAC's

ZERO: set input code so that all bits are "off", then adjust pot until output signal is within $1/10$ LSB of proper reading, or zero.

GAIN: set input code so that all bits are "on", then adjust pot until output signal reads within $1/10$ LSB of *Full Scale less 1LSB*.

Adjustment For ADC's

ZERO: set input voltage precisely at $1/2$ LSB above the "all bits off" specified input. Zero control should be adjusted so that the converter just switches in its LSB.

GAIN: set input voltage precisely at $1/2$ LSB less than "all bits on" input. Note that this is $1/2$ LSB's less than the nominal full scale value: i.e., all-1's value of a zero to +10V 12-bit

ADC is actually +9.9976. Gain adjustment should be made with an input $\frac{1}{2}$ LSB less, or +9.9963 volts. With input voltage set as described, GAIN control is rotated to the point where the last bit just comes on. For instance, in a 12 bit binary converter, reading of 111111111110 would change to 111111111111.

Converter Resolution	Converter Range		
	20V	10V	5V
8 bits	39.06mV	19.53mV	9.77mV
10 bits	9.77mV	4.88mV	2.44mV
12 bits	2.44mV	1.22mV	610 μ V
14 bits	610 μ V	305 μ V	153 μ V
16 bits	153 μ V	76 μ V	38 μ V

Table 1. Voltage equivalent of $\frac{1}{2}$ LSB for various resolutions and voltage ranges.

It is important to note that this discussion is relevant for *offset-binary positive-true* coding. For 2's complement, the "all-bits-off" positive-true condition is 10000000 and "all bits on" is 01111111. For negative-true devices, the "all-bits-off" condition is 11111111 in offset binary, 01111111 in two's complement. When in doubt (or to avoid doubt), consult the data sheet.

