ASTEC SEMICONDUCTOR DATA BOOK

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ASTEC

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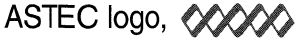
ASTEC reserves the right to make changes without further notice to any products described herein to improve reliability, function, or design. ASTEC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights or the rights of others. ASTEC products are not authorized for use as components in life support devices or systems intended for surgical implant into the body or intended to support or sustain life. Buyer agrees to notify ASTEC of any such intended end use whereupon ASTEC will determine availability and suitability of its products for the intended use. **ASTEC** and the ASTEC logo,  , are trademarks of ASTEC (BSR) PLC.

Table of Contents

Application Notes

Appendix

Astec Semiconductor Division (ASD) was chartered in 1983 to design and manufacture high quality power management integrated circuits for the Astec family of power supplies.

Extending from this charter, ASD has become power management specialist, developing semiconductor products optimized for the specific need of all customers in power supply, lighting ballast, temperature controllers and consumer electronic applications. Our products are built on modern Bipolar, BiMOS and CMOS technologies. ASD provides their customers products and services built to the highest standards of quality and reliability.

Our goal is to provide quality, technology and predictability in our pursuit of customer satisfaction.

Gene R. Miller
President
Astec Semiconductor Division

Order Entry

Products contained within this data book can be ordered from:

Astec Semiconductor
255 Sinclair Frontage Road
Milpitas, California 95035 USA
Phone: 408-263-8300
Facsimile: 408-263-8340

Ordering Information

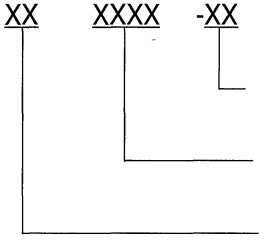
Minimum engineering order: 50 pieces (product samples available upon request)

Minimum production order: 500 pieces

Each item ordered must appear exactly as listed in the data sheet

F.O.B.: Milpitas, California

Part Number Information



Package Style

Generic or Product Part Number

Designator
UC, TL, LM, and LT are industry standard second source devices
AS are proprietary or improved devices

Package Suffix Explanation

Letter Designation	Description
N	8, 14, 16, 18, and 20 Lead Plastic DIP
D	8, 14, and 16 Lead Plastic Narrow Body SOIC
DW	16, 18, and 20 Lead Plastic Wide Body SOIC
LP	TO-92 Plastic (3 Lead)
HP	TO-237 Plastic (3 Lead, TO-92 with Top Heat Spreader)
VS	SOT-23 Plastic (3 Lead)
S	SOT-89 Plastic (3 Lead with Heat Spreader)
G	SOT-223 Plastic (3 Lead with Heat Spreader)

Package Marking Information

Package Marking Explanation

Package marking provides a consistent way of identifying product types and managing lot traceability. All Astec products, with the exception of the SOT-23 and SOT-89 packages, are marked with product type, lot number, date code, and country of origin. Each assembly lot in the SOT-23 and SOT-89 packages, receives a unique alpha-numeric code which is recorded in a data base for cross reference to lot number, date code, and country of origin. A complete marking format table is shown below.

8, 14, 16, 18, and 20 Lead Plastic DIP:

Top- Astec Logo
Product Name
Lot Identificaton Code

Bottom- Lot Identification Code
Country of Origin
Date Code

8, 14, and 16 Lead Plastic Narrow Body SOIC:

Top- Product Name
Lot Identificaton Code

Bottom- Date Code
Country of Origin

16, 18, and 20 Lead Plastic Wide Body SOIC:

Top- Astec Logo
Product Name
Lot Identificaton Code

Bottom- Lot Identification Code
Country of Origin
Date Code

TO-92/237 Plastic (3 Lead):

Face- Astec Logo
Product Name
Lot Identificaton Code
Country of Origin
Date Code

SOT-23 Plastic (3 Lead):

Top- Log Book Code

SOT-89 Plastic (3 Lead with Heat Spreader):

Top- Product Name
Log Book Code

SOT-223 Plastic (3 Lead with Heat Spreader):

Top- Product Name
Lot Identificaton Code

Bottom- Date Code
Country of Origin

Alternate Source and Product Cross-Reference

P/N	ASD Direct Replacement Part
Cherry Semiconductor	
CS384XA	AS384X
CS384X	AS384X
Hitachi	
HA17431	A431
HA17384	AS3842
HA17345	AS3843
Linear Techology	
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
LT1004-1.2	AS1004-1.2
LT1004-2.5	AS1004-2.5
LT1431CZ	AS1431*
LT1242	AS3842*
LT1243	AS3843*
LT1244	AS3844*
LT1245	AS3845*
Motorola Semiconductor	
TL431	A431
TL431A	A431
UC384X	AS384X
UC384XA	AS384X

P/N	ASD Direct Replacement Part
National Semiconductor	
LM431A	A431
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
Samsung Semiconductor	
SKA431	A431
KA384X	AS384X
Texas Instruments	
TL431	A431
TL431A	A431
TL1431	AS1431
LM385-1.2	AS1004-1.2
LM385-2.5	AS1004-2.5
LT1004-1.2	AS1004-1.2
LT1004-2.5	AS1004-2.5
UC384X	AS384X

P/N	ASD Direct Replacement Part
Unitrode	
UC384X	AS384X
UC384XA	AS384X*

* Similar Device: Please consult data sheet to determine the suitability of replacement for specific applications

Definition of Terms

Data Sheet Identification	Product Status	Definition
Proposed	In Design	This data sheet contains the design specifications for product development. These specifications are subject to change. Further information will be published upon product release.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date. Astec Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.
No Identification	Full Production	This data sheet contains final specifications and complete typical curves. Astec Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

Data Sheets

Notes

AS431

Precision Adjustable Shunt Reference

Features

- Temperature-compensated: 30 ppm/°C
- Trimmed 0.5% bandgap reference
- Internal amplifier with 150 mA capability
- Nominal temperature range extended to 105° C
- Low frequency dynamic output impedance: < 150 m
- Low output noise
- Robust ESD protection

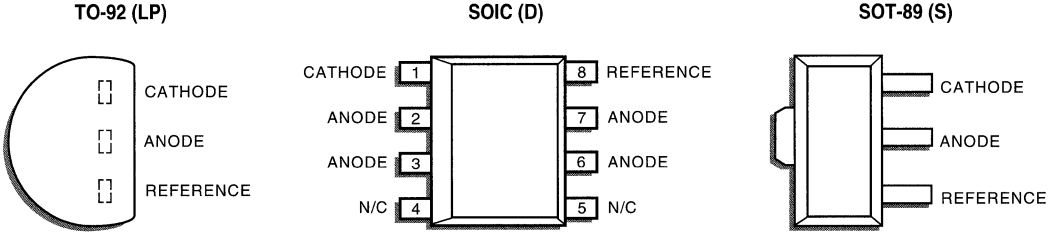
Description

The AS431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.5% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference a perfect zener diode replacement .

The A431 regulator is a low-cost solution where a bandgap reference tolerance is not critical. The A431 has a 1% bandgap reference and can be used as a direct replacement for the standard TL431.

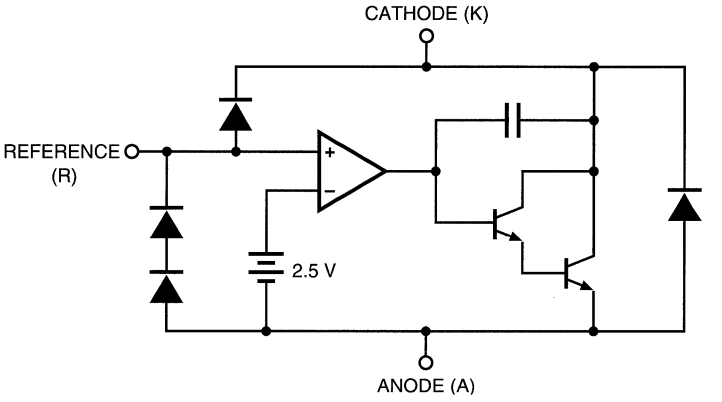
Pin Configuration — Top view



Ordering Information

Description	Temperature Range	Order Codes	
		0.5%	1.0%
TO-92	0 to 105° C	AS431LP	A431LP
8-Pin Plastic SOIC	0 to 105° C	AS431D	A431D
SOT-89	0 to 105° C	AS431S	A431S

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	37	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	250	mA
Reference Input Current	I_{REF}	10	mA
Continuous Power at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

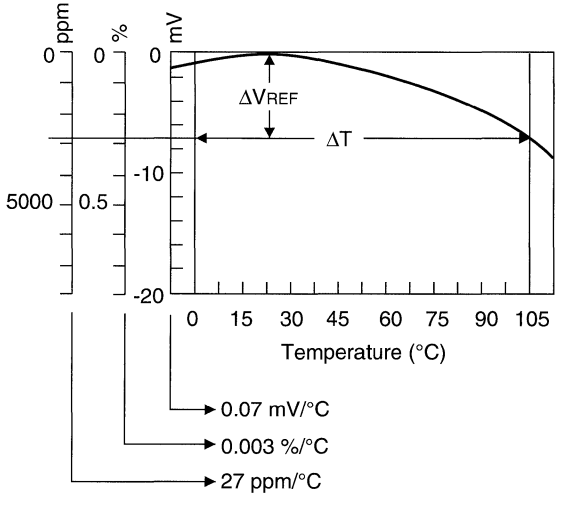
Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and I_K = 10 mA unless otherwise stated.

Parameter	Symbol	Test Condition	AS431 (0.5%) Min	Typ	Max	A431 (1.0%) Min	Typ	Max	Unit	Test Circuit
Reference Voltage	V_{REF}	T_A = 25° C	2.490	2.503	2.515	2.470	2.495	2.520	V	1
		Over temp.	2.469		2.536	2.449		2.541	V	1
V_{REF} with Temp*	TC			0.07	0.20		0.07	0.20	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{V_{REF}}{V_K}$	V_{REF} to 10 V	− 2.7	− 1.0		− 2.7	−1.0		mV/V	2
		10 V to 36 V	− 2	− 0.4	0.3	− 2	− 0.4	0.3		
Reference Input Current	I_{REF}			0.7	4		0.7	4	µA	2
I_{REF} Temp Deviation	I_{REF}	Over temp.		0.4	1.2		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1		0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	V_{REF} = 0 V, V_{KA} = 36 V		0.04	250		0.04	250	nA	3
Dynamic Output Impedance	Z_{KA}	f 1 kHz I_K = 1 to 150 mA		0.15	0.5		0.15	0.5	Ω	1

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\frac{\Delta V_{REF}\ (mV)}{\Delta T_A}$

- TC in %/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 100}{\Delta T_A}$

- TC in ppm/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 10^6}{\Delta T_A}$

Test Circuits

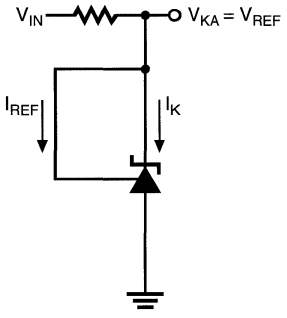


Figure 1a. Test Circuit 1

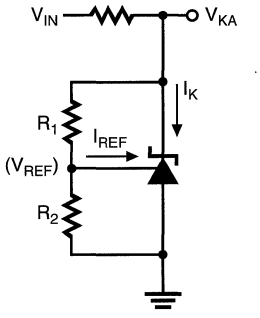


Figure 1b. Test Circuit 2

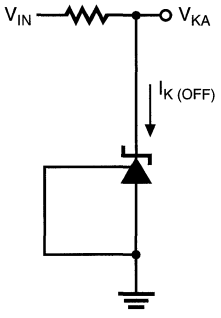


Figure 1c. Test Circuit 3

Typical Performance Curves

Low Current Operating Characteristics

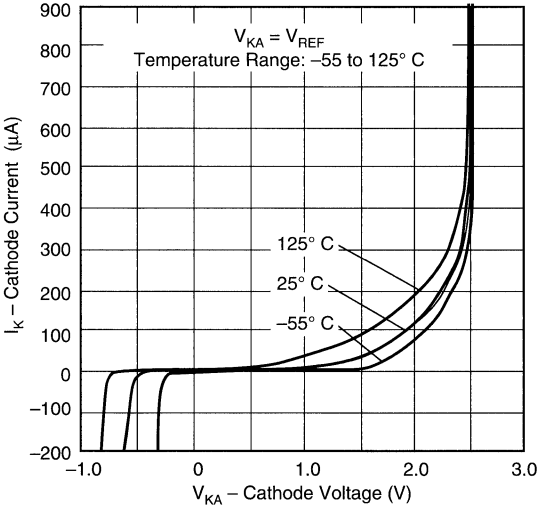


Figure 2

High Current Operating Characteristics

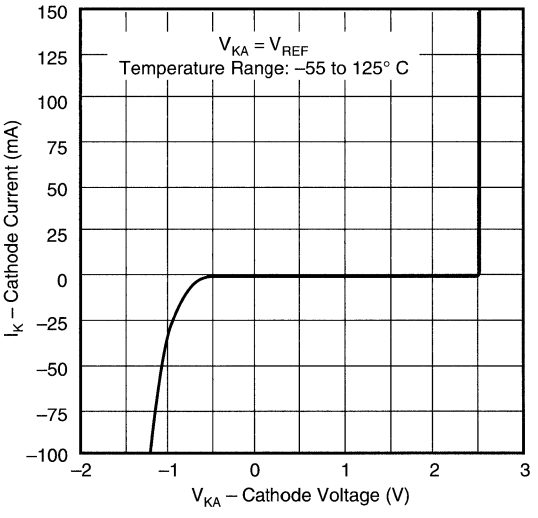


Figure 3

Off State Leakage

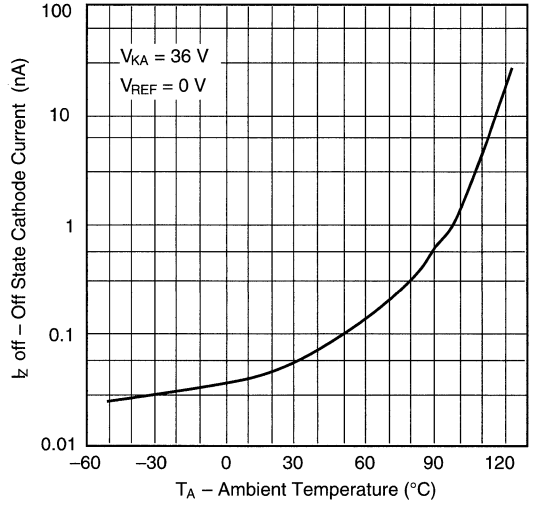


Figure 4

Temperature Coefficient as a Function of Trim Value

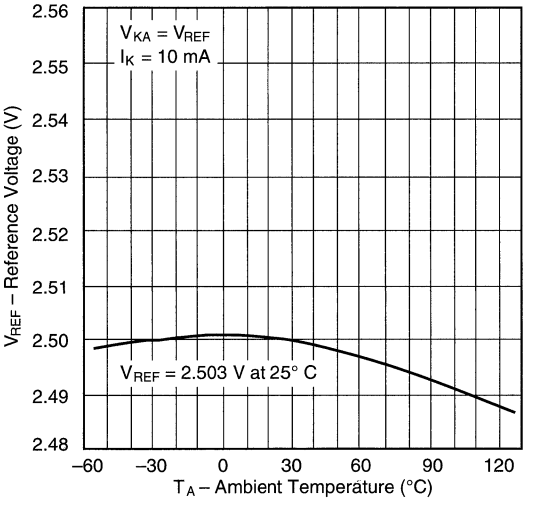


Figure 5

Typical Performance Curves

Reference Input Current

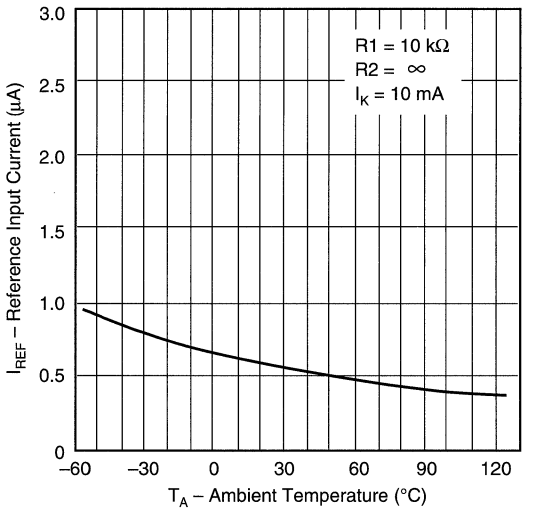


Figure 6

Reference Voltage Line Regulation

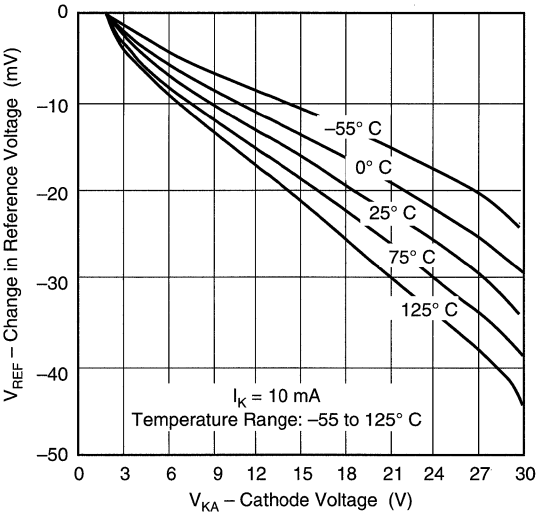


Figure 7

Noise Voltage

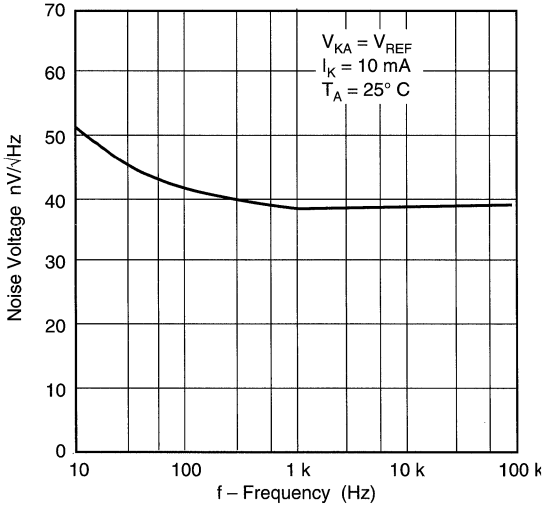


Figure 8

Low Frequency Dynamic Output Impedance

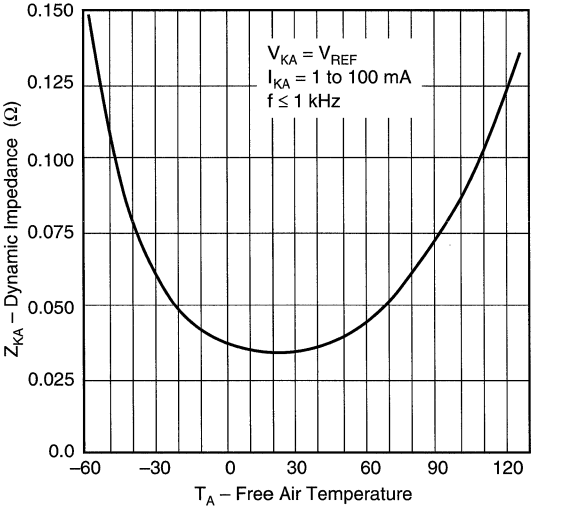


Figure 9

Typical Performance Curves

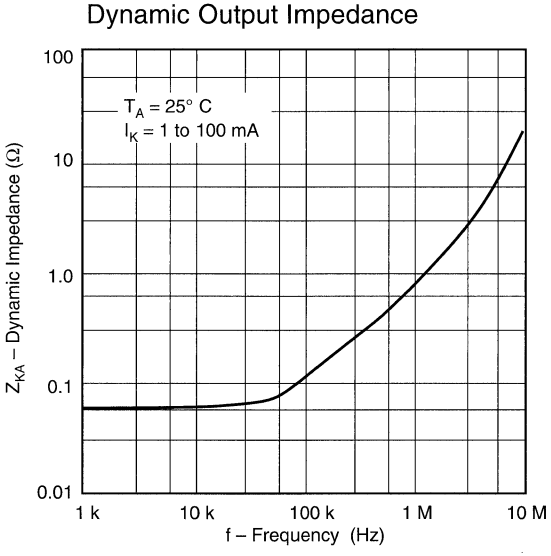


Figure 10

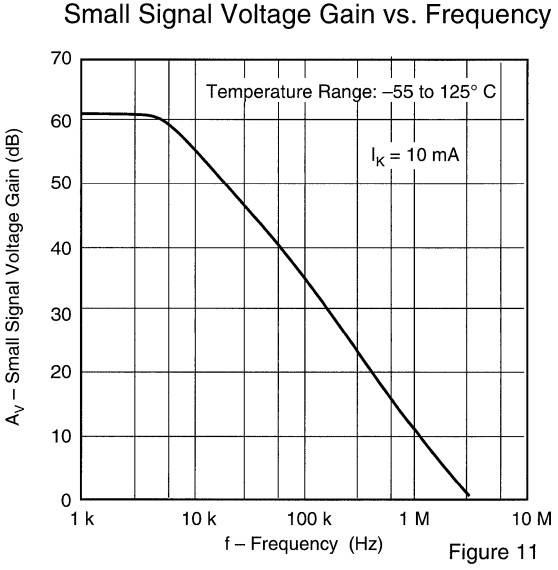
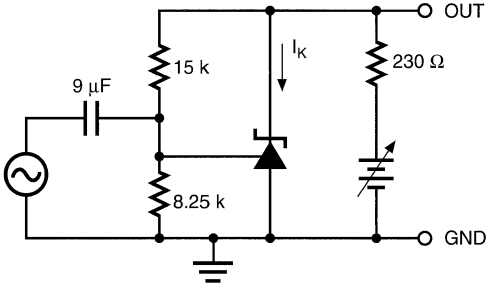


Figure 11



Typical Performance Curves

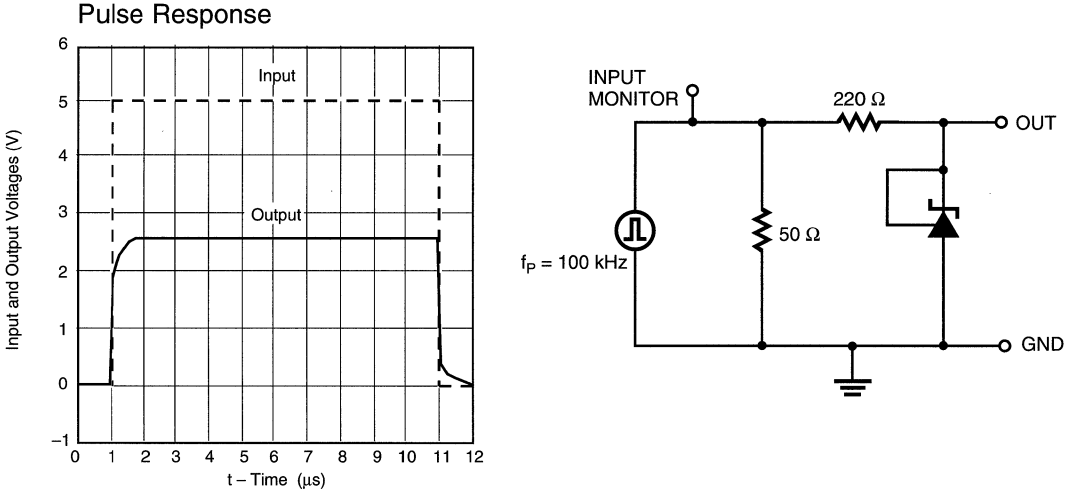


Figure 12

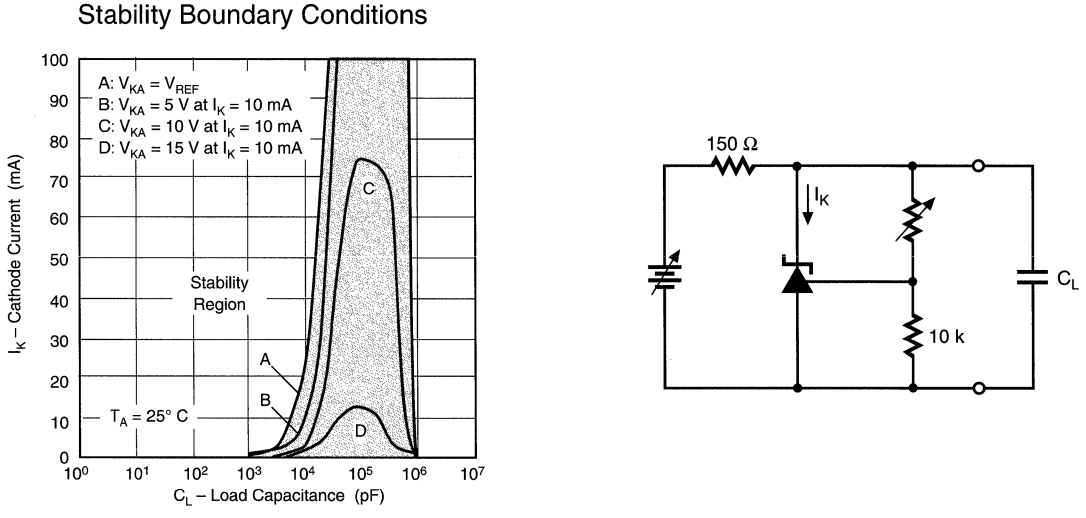


Figure 13

AS1431

Precision Adjustable Shunt Reference

Features

- Temperature-compensated: 30 ppm/°C
- Trimmed 0.4% bandgap reference
- Internal amplifier with 150 mA capability
- Temperature range: Extended to -55 to125° C
- Low frequency dynamic output impedance: < 150 m
- Low output noise
- Robust ESD protection

Description

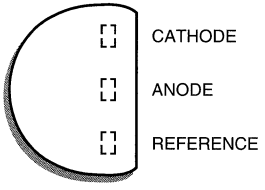
The AS1431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.4% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference a perfect zener diode replacement .

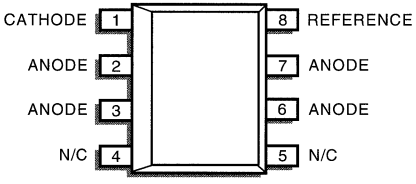
The AS1431 is characterized to operate over the full automotive temperature range of -55 to 125° C and is now available in the SOT-89 package.

Pin Configuration — Top view

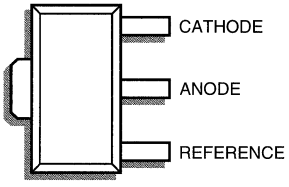
TO-92 (LP)



SOIC (D)



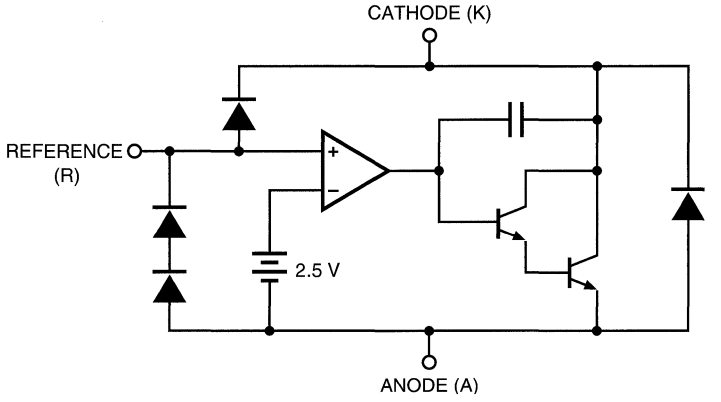
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	-55 to 125° C	AS1431LP
8-Pin Plastic SOIC	-55 to 125° C	AS1431D
SOT-89	-55 to 125° C	AS1431S

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	37	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	250	mA
Reference Input Current	I_{REF}	10	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

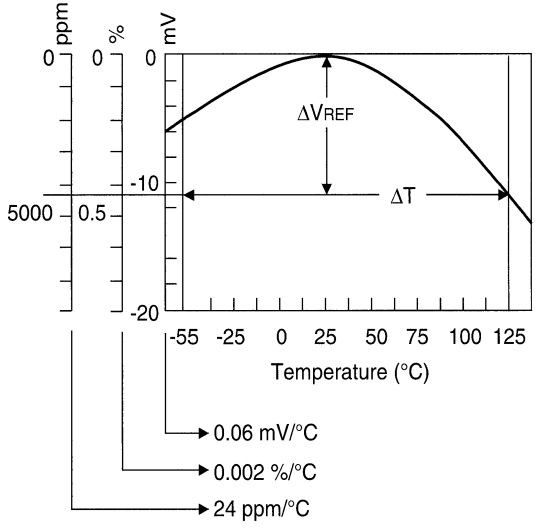
Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (-55 to 125° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Circuit
Reference Voltage	V_{REF}	T_A = 25° C	2.490	2.500	2.510	V	1
		Over temp.	2.470		2.530	V	1
V_{REF} with Temp*	TC			0.06	0.16	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	V_{REF}	V_K = 3 V to 36 V	– 2	– 1.1		mV/V	2
Reference Input Current	I_{REF}	R_1 = 10 k ; R_2 =		0.7	1.9	µA	2
I_{REF} Temp Deviation	I_{REF}	Over temp.		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	V_{REF} = 0 V, V_{KA} = 36 V		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	f 1 kHz I_K = 1 to100 mA		0.15	0.2	Ω	1

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\dfrac{\Delta V_{REF}\ (mV)}{\Delta T_A}$

- TC in %/°C = $\dfrac{\left(\dfrac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 100}{\Delta T_A}$

- TC in ppm/°C = $\dfrac{\left(\dfrac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 10^6}{\Delta T_A}$

Test Circuits

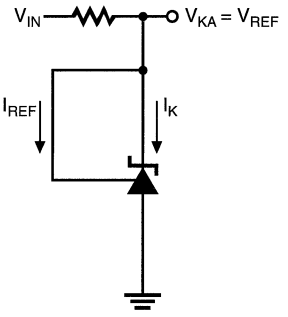


Figure 1a. Test Circuit 1

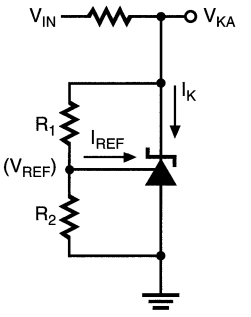


Figure 1b. Test Circuit 2

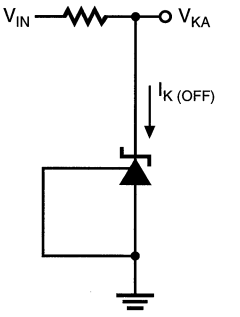


Figure 1c. Test Circuit 3

Typical Performance Curves

Low Current Operating Characteristics

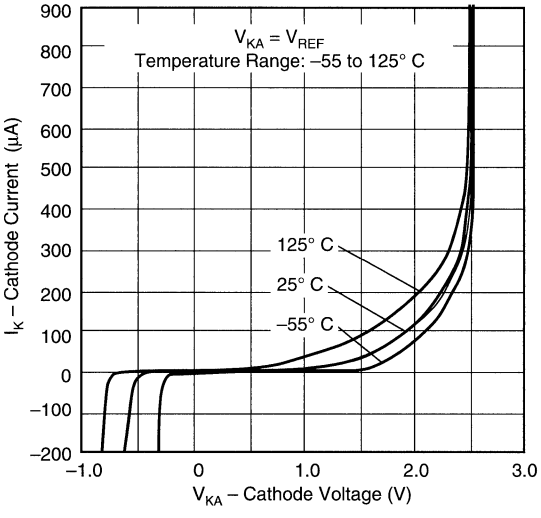


Figure 2

High Current Operating Characteristics

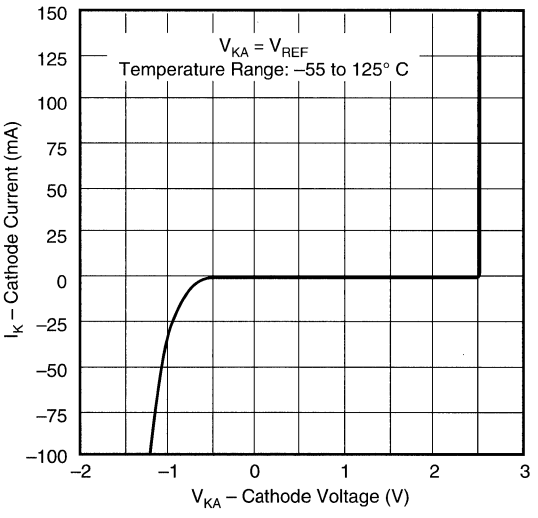


Figure 3

Off State Leakage

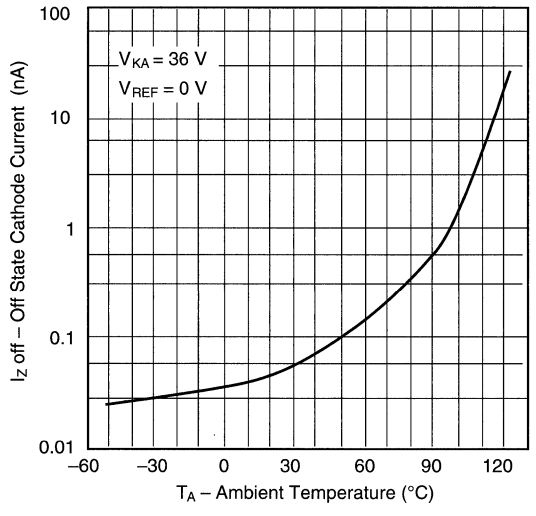


Figure 4

Reference Voltage vs Ambient Temperature

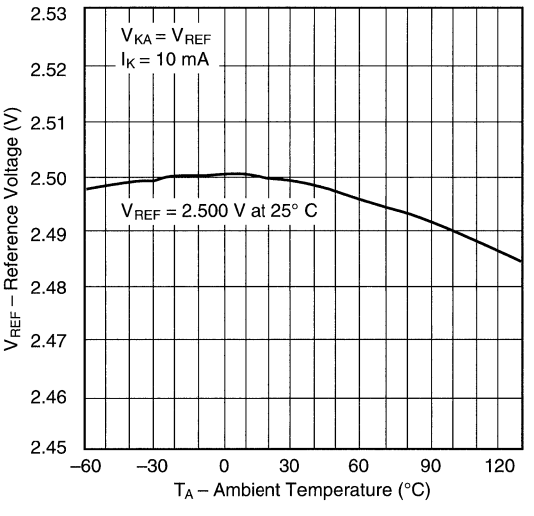


Figure 5

Typical Performance Curves

Reference Input Current

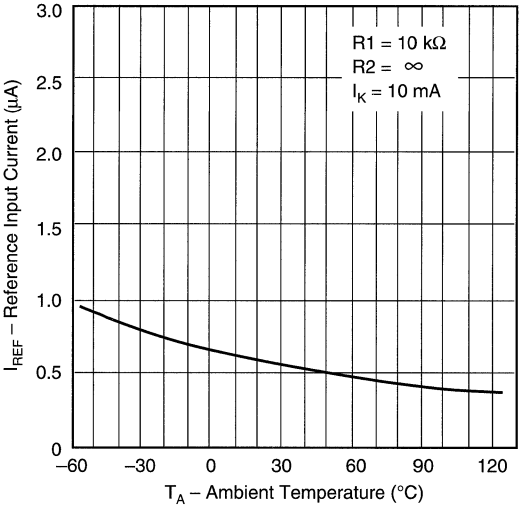


Figure 6

Reference Voltage Line Regulation

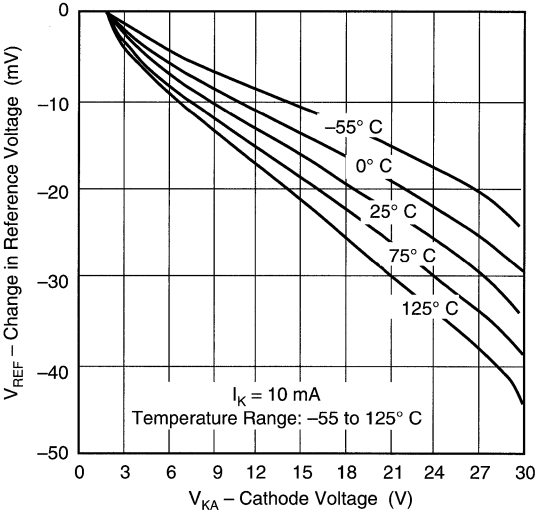


Figure 7

Noise Voltage

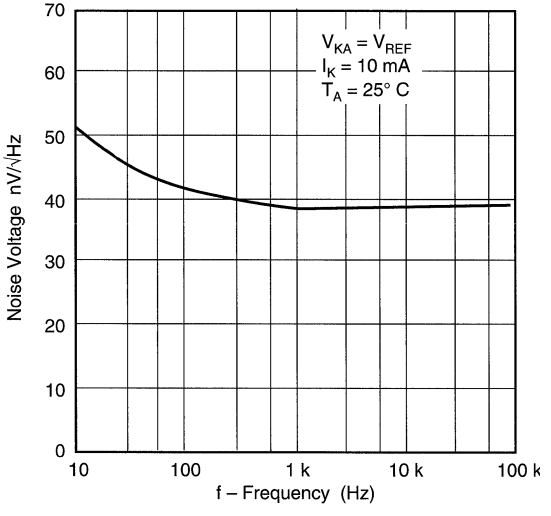


Figure 8

Low Frequency Dynamic Output Impedance

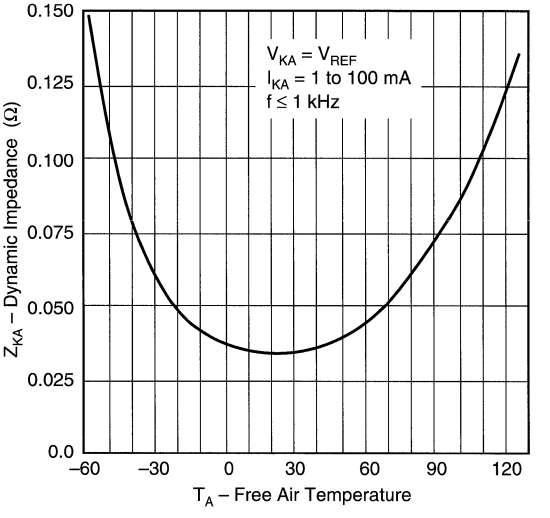


Figure 9

Typical Performance Curves

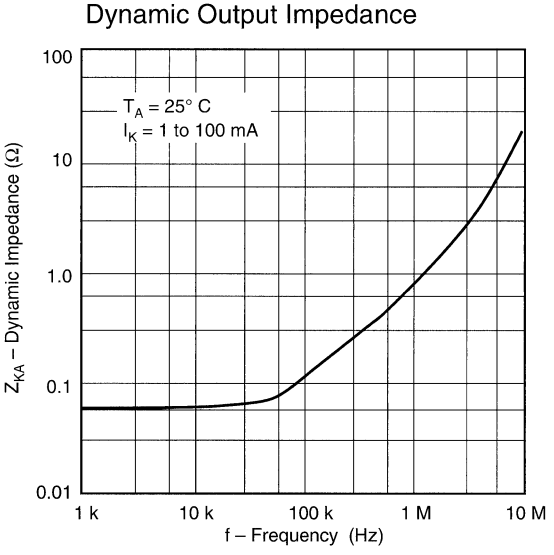


Figure 10

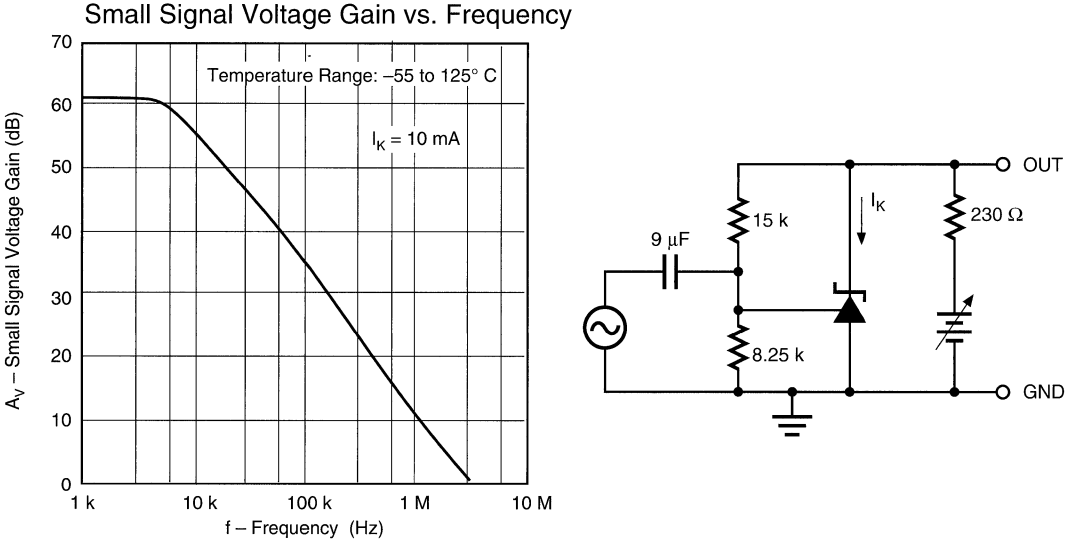


Figure 11

Typical Performance Curves

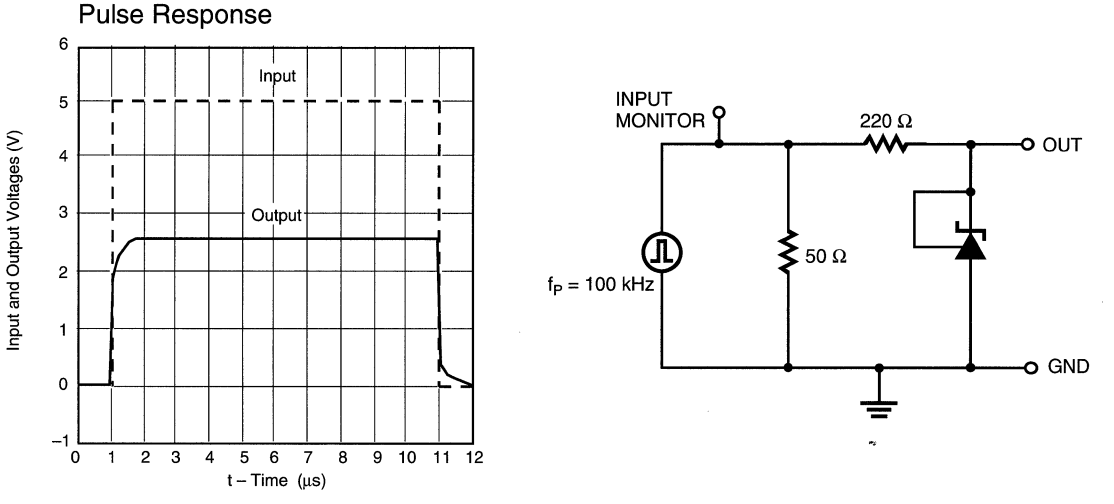


Figure 12

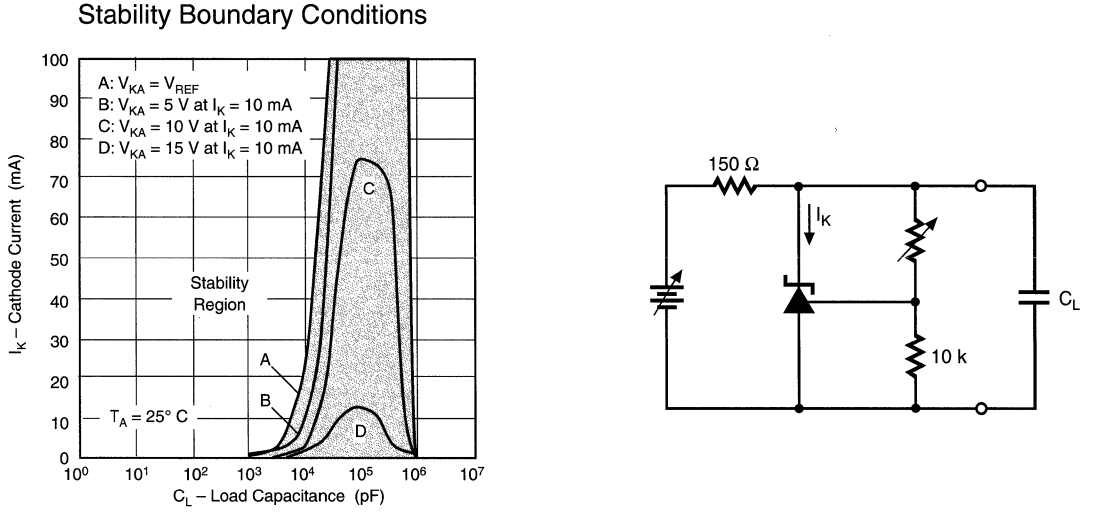


Figure 13

AS2431

Precision Adjustable Shunt Reference

Preliminary Specification

Features

- Temperature-compensated: 15 ppm/°C
- Trimmed 0.5% bandgap reference
- Internal amplifier with 100 mA capability
- Temperature range: Extended to 0 t o 105° C
- Low frequency dynamic output impedance: < 150 m
- Low output noise

Description

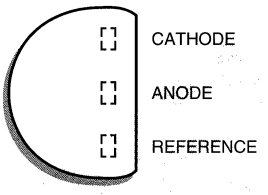
The AS2431 is a three-terminal adjustable shunt regulator providing a highly accurate 0.5% bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.

In the standard shunt configuration, the combination of low temperature coefficient (T.C.), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference an excellent error amplifier.

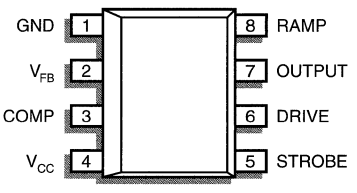
The AS2431 is a direct replacement for the AS431 in low voltage, low current applications. It is also available in the very small footprint SOT-23.

Pin Configuration — Top view

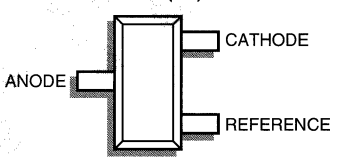
TO-92 (LP)



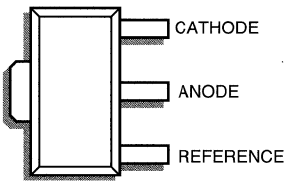
SOIC (D)



SOT-23 (VS)



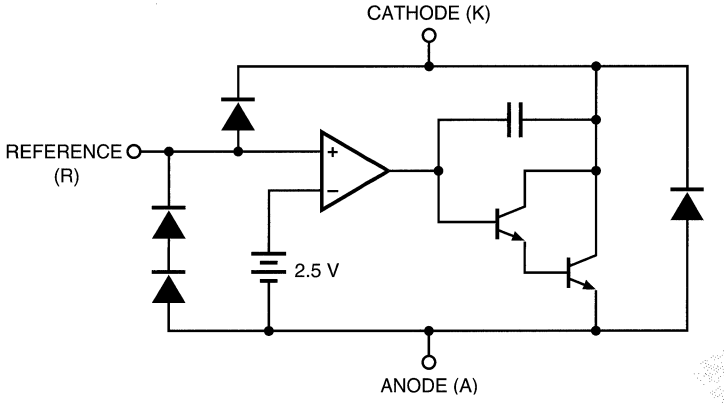
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	0 to 105° C	AS2431LP
8-Pin Plastic SOIC	0 to 105° C	AS2431D
SOT-23	0 to 105° C	AS2431VS
SOT-89 (S)	0 to 105° C	AS2431S

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	18	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	100	mA
Reference Input Current	I_{REF}	1	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-23		200	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	–65 to 150	°C
Lead Temp, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 18	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

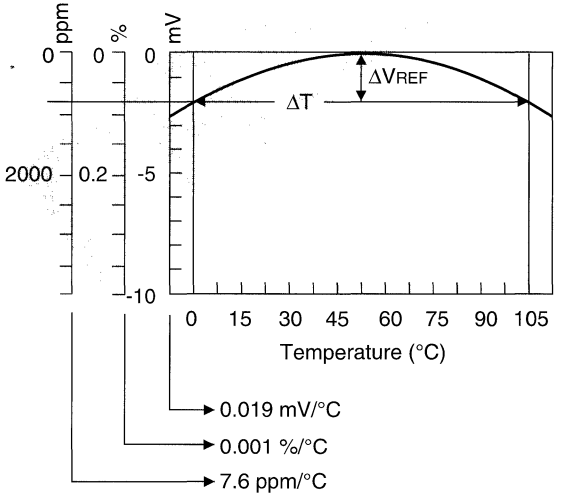
Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-23	575°C/W	150° C/W	1.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10$ mA unless otherwise stated.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	Circuit
Reference Voltage	V_{REF}	T_A = 25° C	2.490	2.500	2.510	V	1
		Over temp.	2.480		2.530	V	1
ΔV_{REF} with Temp*	TC			0.02	0.06	mV/ ° C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	– 2.7	– 1.01		mV/V	2
		10V to 18 V	– 2	– 0.4	0.3		
Reference Input Current	I_{REF}			0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	V_{REF} = 0 V, V_{KA} = 18 V		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	f ≤ 1 kHz I_K = 1 to100 mA		0.15	0.5	Ω	1

*Calculating Average Temperature Coefficient (TC)



- TC in mV/°C = $\frac{\Delta V_{REF}\ (mV)}{\Delta T_A}$

- TC in %/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 100}{\Delta T_A}$

- TC in ppm/°C = $\frac{\left(\frac{\Delta V_{REF}}{V_{REF}\text{ at }25°C}\right) \times 10^6}{\Delta T_A}$

Test Circuits

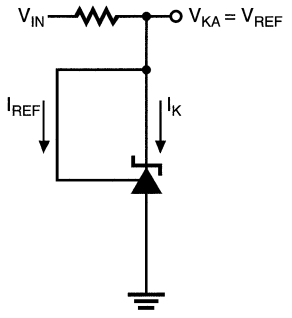


Figure 1a. Test Circuit 1

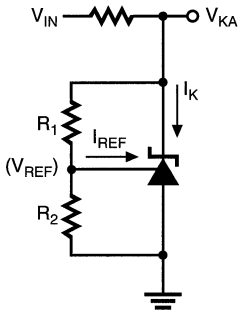


Figure 1b. Test Circuit 2

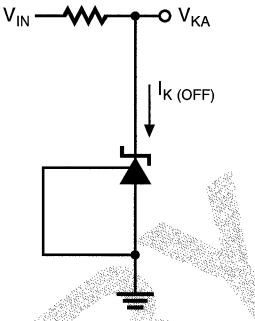


Figure 1c. Test Circuit 3

Typical Performance

Low Current Operating Characteristics

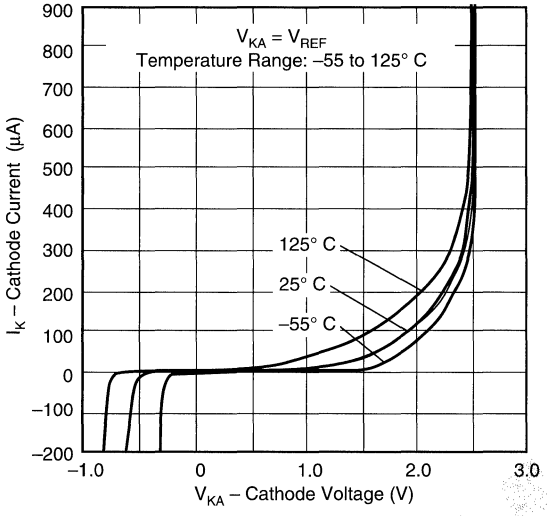


Figure 2

High Current Operating Characteristics

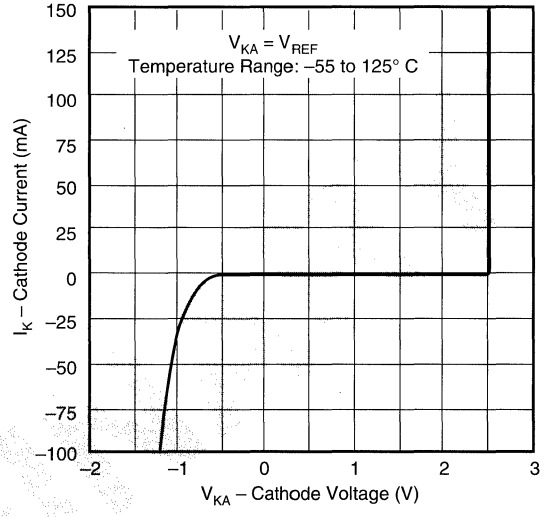


Figure 3

Off State Leakage

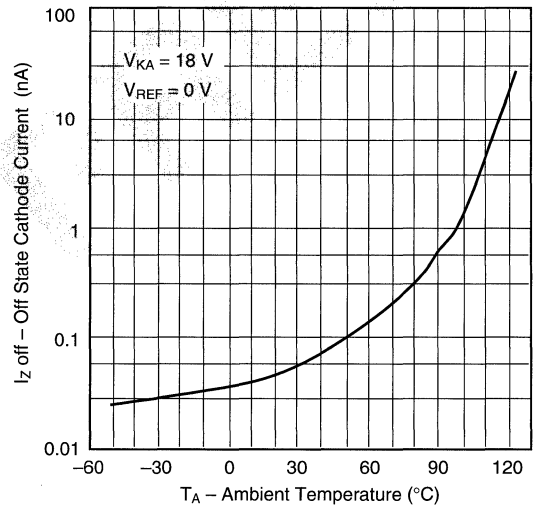


Figure 4

Temperature Coefficient as a Function of Trim Value

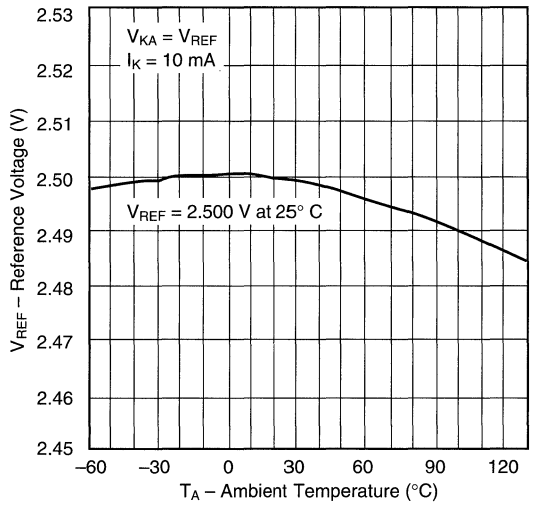


Figure 5

Typical Performance Curves

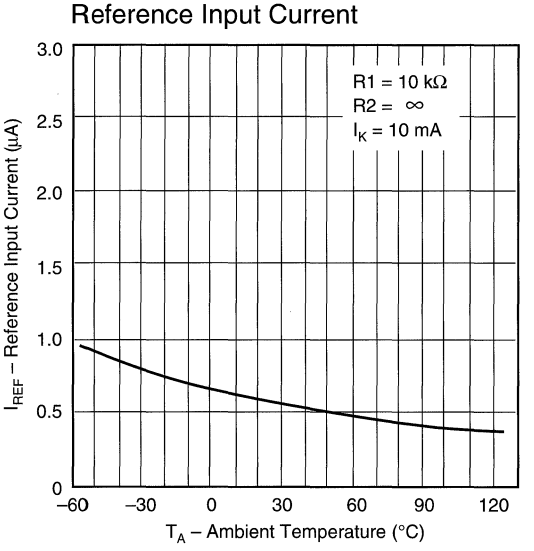


Figure 6

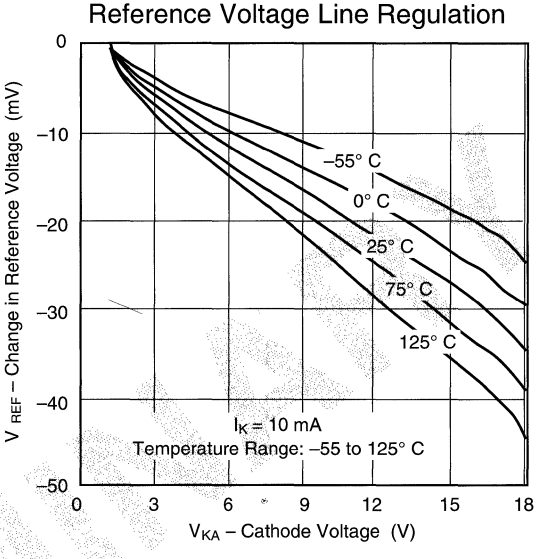


Figure 7

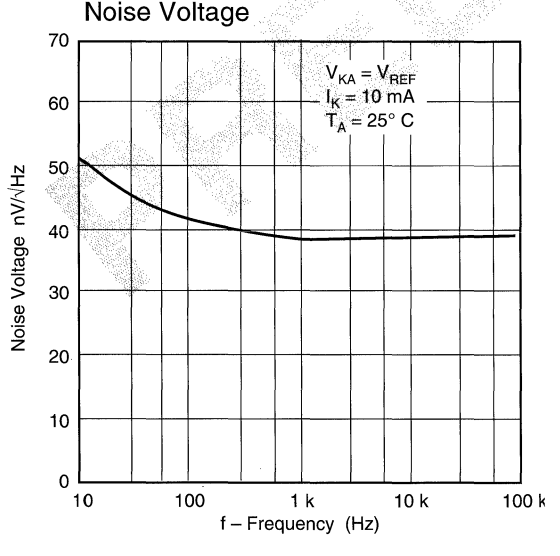


Figure 8

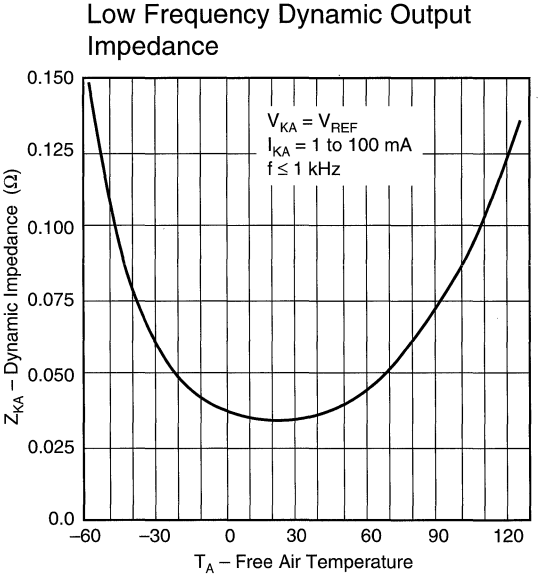


Figure 9

Typical Performance Curves

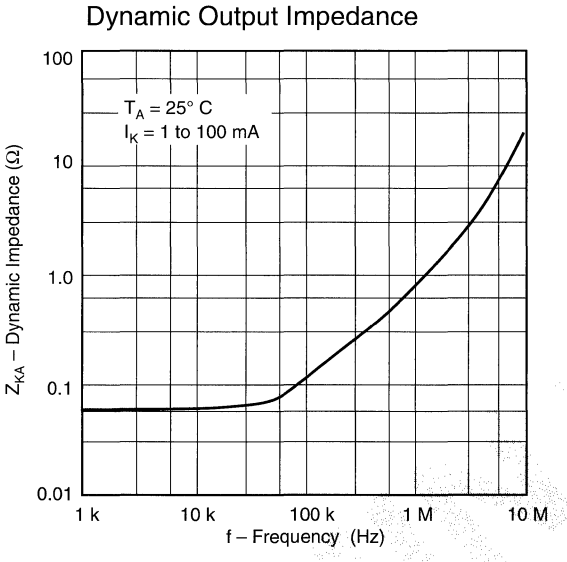
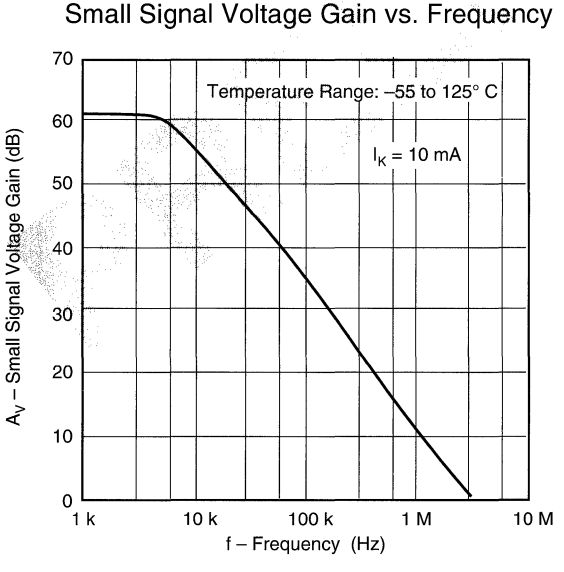


Figure 10



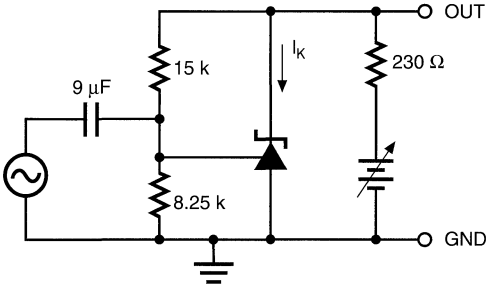
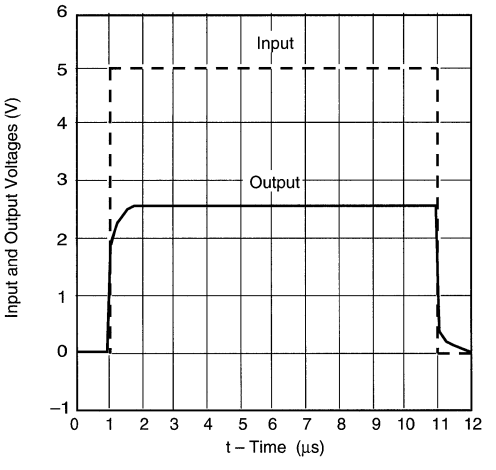


Figure 11

Typical Performance Curves

Pulse Response



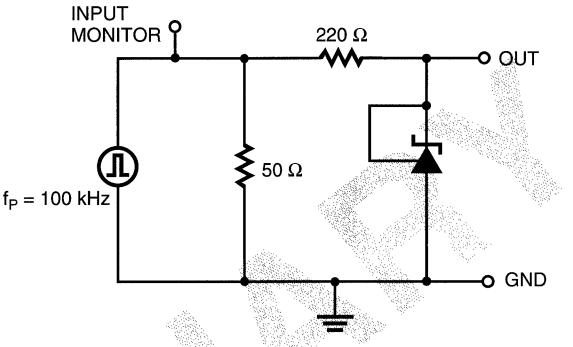
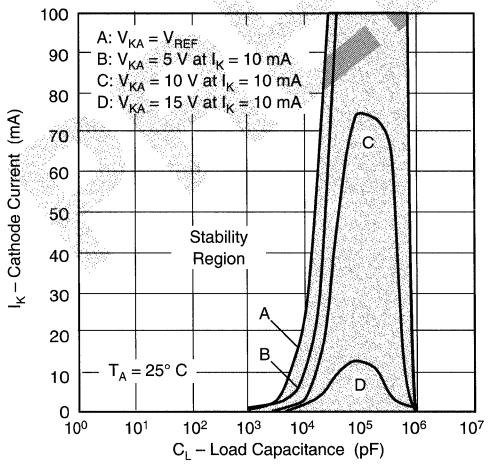


Figure 12

Stability Boundary Conditions



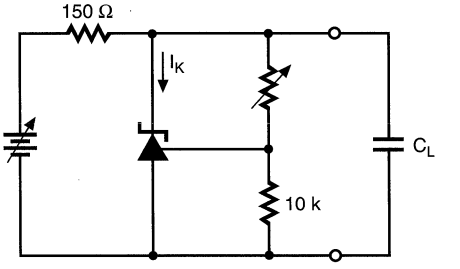


Figure 13

AS432

1.25 V Precision Adjustable Shunt Reference / Amplifier

Proposed Specification

Features

- Temperature-compensated: 50 ppm/°C
- Trimmed 0.5% bandgap reference
- Internal amplifier with 150 mA capability
- Nominal temperature range extended to 105° C
- Low frequency dynamic output impedance: < 150 m
- Low output noise

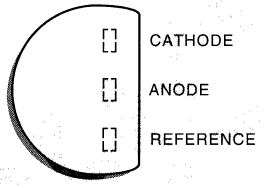
Description

The AS432 is a three terminal adjustable shunt regulator utilizing an accurate 1.25V bandgap reference. The AS432 is functionally similar to an AS431 except for its lower reference voltage, making it usable in a wide variety of low voltage applications.

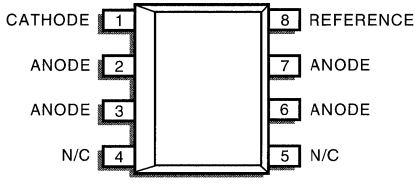
Because of its robust bipolar technology, the AS432 handles a wide range of current, and holds off more than 18V so its use is not limited to low power, low voltage systems. Significant care has been taken to provide adequate AC bandwidth to allow the AS432 as an amplifier in control systems and power electronics.

Pin Configuration — Top view

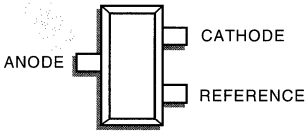
TO-92 (LP)



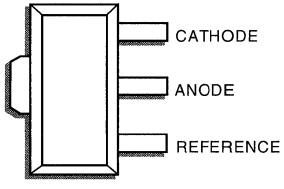
SOIC (D)



SOT-23 (VS)



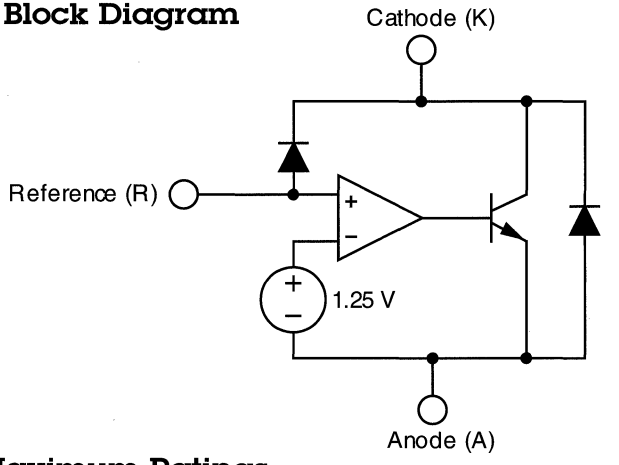
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	0 to 105° C	AS432LP
8-Pin Plastic SOIC	0 to 105° C	AS432D
SOT - 89	0 to 105° C	AS432S
SOT - 23	0 to 105° C	AS432VS

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	18	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	100	mA
Reference Input Current	I_{REF}	1	mA
Continuous Power at 25° C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
SOT-23		200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	– 65 to 150	°C
Lead Temperature (Soldering 10 sec.)	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 18	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C
SOT-23	575° C/W	150° C/W	1.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over the full junction temperature range (0-105 °C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics. Unless otherwise stated, test conditions are: VKA= VREF and IK=10 mA.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	V_{REF}	I_K=1 0 mA, T_J = 25° C, $V_K = V_{REF}$	1.244	1.250	1.256	V
Line Regulation	V_{REF}	V_{KA} = 1.25 to 15 V		10	15	mV
Load Regulation	V_{REF}	I_K = 1 to 100 mA		3	6	mV
Temperature Deviation	V_{REF}	0 < T_J < 105° C		2	6	mV
Reference Input Current	I_{REF}			3	6	µA
Reference Input Current Temperature Coefficient	I_{REF}	0 < T_J < 105 °C		0.3	0.6	µA
Minimum Cathode Current for Regulation	$I_{K(MIN)}$			0.6	1	mA
Off State Leakage	$I_{K(MIN)}$	V_{REF} = 0 V, V_{KA} = 18 V		0.04	500	nA

*Temperature deviation is defined as the maximum deviation of the reference over the given temperature range and does not imply an incremental deviation at any given temperature.

Typical Performance Curves

Not Available at Time of Publishing

ASTEC SEMICONDUCTOR

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Notes

AS1004

Micropower Voltage Reference

Features

- Low voltage reference
- 10 μA turn-on current for AS1004-1.2
- 20 μA turn-on current for AS1004-2.5
- ± 4 mV (0.3 %) initial accuracy for AS1004-1.2
- ± 20 mV (0.8 %) initial accuracy for AS1004-2.5
- Guaranteed operation to 20 mA. Over three orders of magnitude of operating current!
- Temperature performance guaranteed
- Very low dynamic impedance

Description

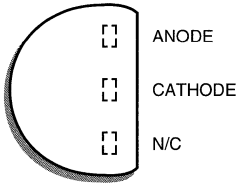
The AS1004 is a two-terminal precision band-gap voltage reference with a low turn-on current of 10 μA.

Emulating a 1.235 V zener diode, the AS1004 operates more than three orders of magnitude of output current with minute output impedance and guaranteed stability. With an initial tolerance of ± 4 mV and guaranteed temperature performance, it is ideal for precision instrumentation, especially in low power applications. Being a low-voltage reference, the AS1004 is also well-suited as a reference for low-voltage power supply applications, especially in power supplies intended for low-voltage logic systems, laptop computers and other portable or battery operated equipment.

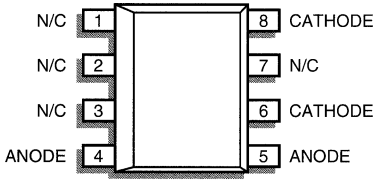
The AS1004 is pin-for-pin compatible with the LT1004 and the LM385 and offers improved specifications over both the LM385 and the MP5010. It is also available as a 2.5 V reference with a guaranteed start-up current of 20 μA.

Pin Configuration — Top view

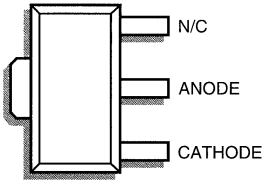
TO-92 (LP)



SOIC (D)



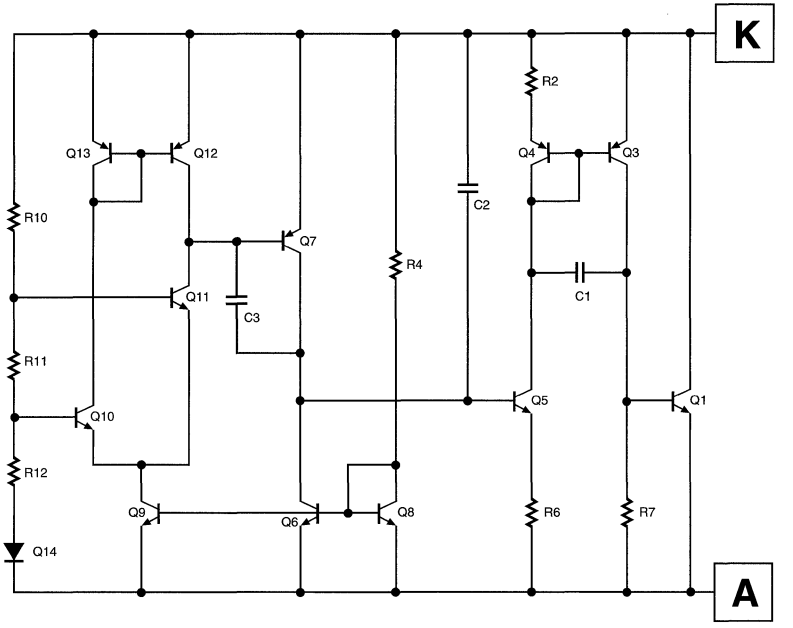
SOT-89 (S)



Ordering Information

Description	Temperature Range	Order Codes	
TO-92	0 to 70° C	AS1004-1.2LP	AS1004-2.5LP
8-Pin Plastic SOIC	0 to 70° C	AS1004-1.2D	AS1004-2.5D
SOT-89	0 to 70° C	AS1004-1.2S	AS1004-2.5S

Simplified Schematic



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Reverse Breakdown Current	I_Z	30	mA
Forward Current	I_F	30	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
8LSOIC		750	mW
SOT-89		1000	mW
Maximum Junction Temp	T_J	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Current	I_Z	100	µA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 70° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics.

Parameter	Symbol	Test Condition	AS1004-1.2 Min	AS1004-1.2 Typ	AS1004-1.2 Max	AS1004-2.5 Min	AS1004-2.5 Typ	AS1004-2.5 Max	Unit
Reverse Breakdown Voltage	V_Z	I_Z = 100 µA, T_J = 25° C	1.231	1.235	1.239	2.480	2.500	2.520	V
		0° C ≤ T_A ≤ 70° C	1.225	1.235	1.245	2.470	2.500	2.530	V
Average Temperature Coefficient	$\Delta V_Z/\Delta T$	$I_{min} \le I_Z \le$ 20 mA		20			60		ppm/°C
Minimum Operating Current	$I_{Z(min)}$			4	10		12	20	µA
Reverse Breakdown Voltage Change With Current	$\Delta V_Z/\Delta I_Z$	$I_{min} \le I_Z \le$ 1 mA		0.5	1		0.5	1	mV
		Over Temperature		0.5	1.5		0.5	1.5	mV
		1 mA ≤ I_Z ≤ 20 mA		6.5	10		6.5	10	mV
		Over Temperature		6.5	20		6.5	20	mV
Reverse Dynamic Impedance	Z_Z	I_Z = 100 mA, f = 25 Hz		0.2	0.6		0.8	0.9	Ω
		Over Temperature		1	1.5			1.5	Ω
Wide Band Noise	e_n	I_Z = 100 µA 10 Hz ≤ f ≤ 10 KHz		60			60		µV
Long Term Stability	$\Delta V_Z/\Delta T$	I_Z = 100 µA T_A = 25° C ± 0.1° C		20			60		ppm/kH

Typical Performance Curves

Calculating Average Temperature Coefficient for the AS1004-1.2 Reference

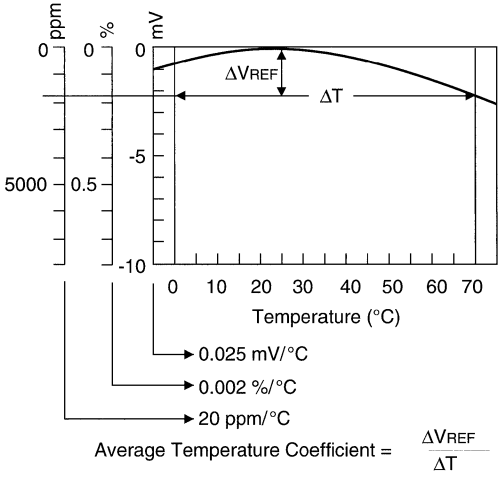


Figure 1

AS1004-1.2 Reference Voltage vs. Ambient Temperature

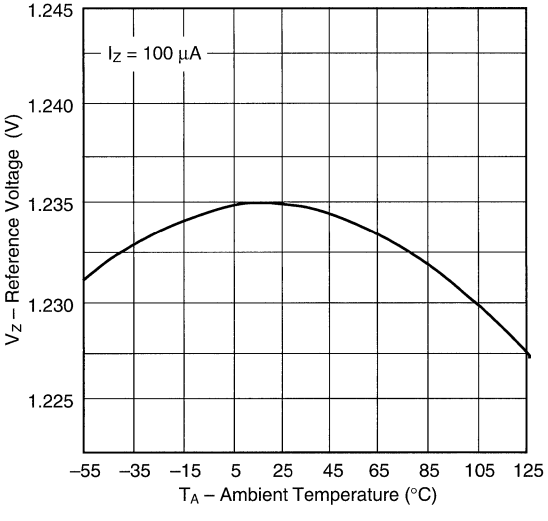


Figure 2

Typical Performance Curves

Calculating Average Temperature Coefficient for the AS1004-2.5 Reference

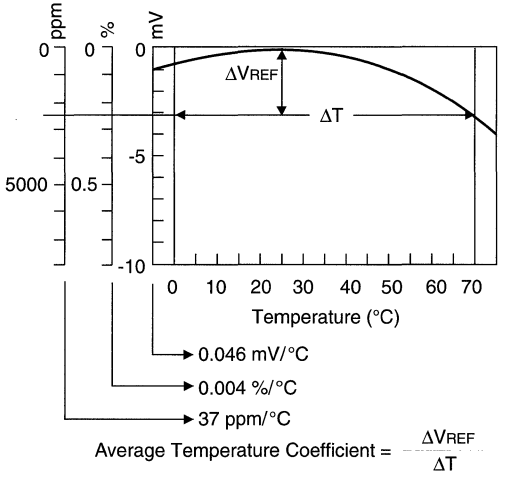


Figure 3

AS1004-2.5 Reference Voltage versus Ambient Temperature

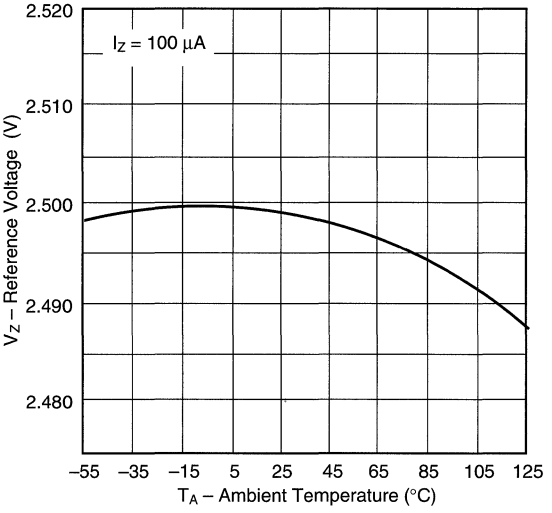


Figure 4

AS1004-1.2 Reverse Operating Characteristics

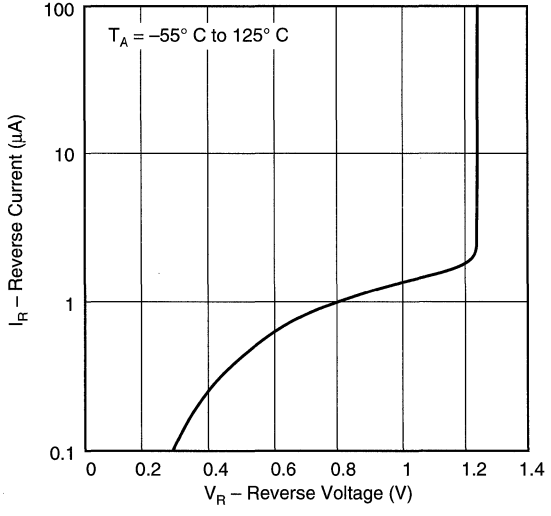


Figure 5

AS1004-2.5 Reverse Operating Characteristics

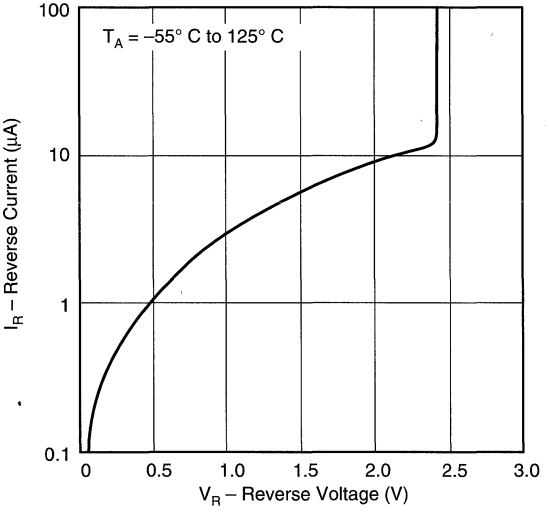


Figure 6

Typical Performance Curves

AS1004-1.2 Change in Reference Voltage versus Reverse Current

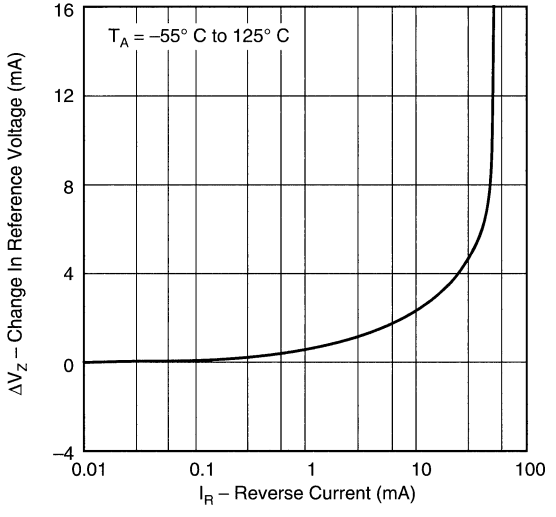


Figure 7

AS1004-2.5 Change in Reference Voltage versus Reverse Current

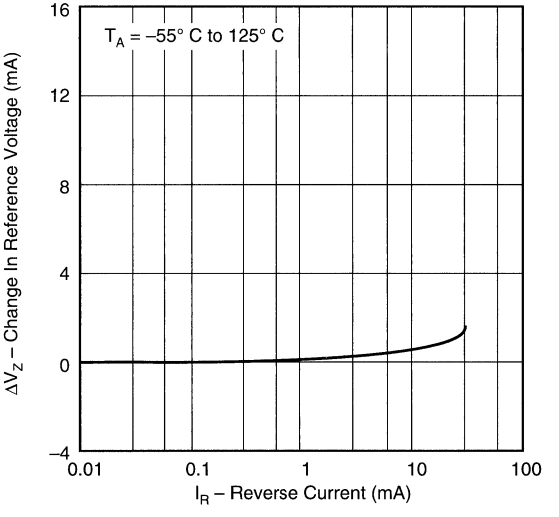


Figure 8

AS1004-1.2 Transient Response

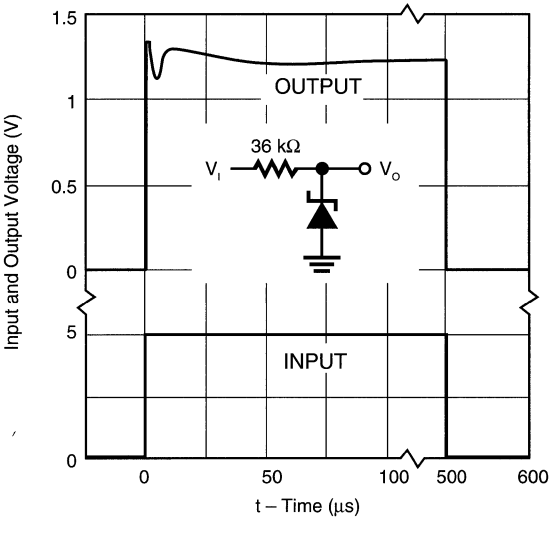


Figure 9

AS1004-2.5 Transient Response

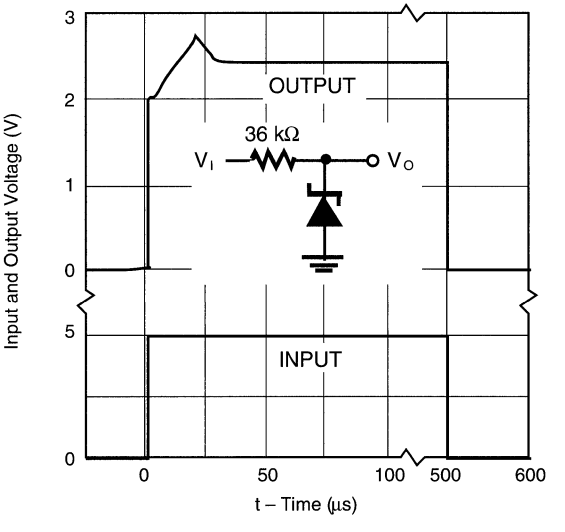


Figure 10

Typical Performance Curves

AS1004-1.2 Reverse Dynamic Impedance

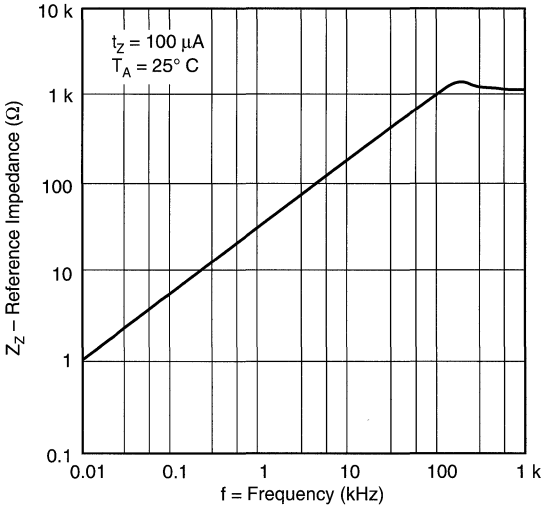


Figure 11

AS1004-2.5 Reverse Dynamic Impedance

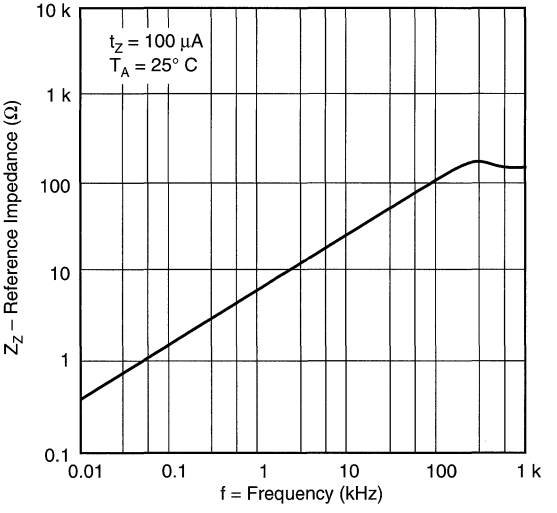


Figure 12

Forward Characteristics

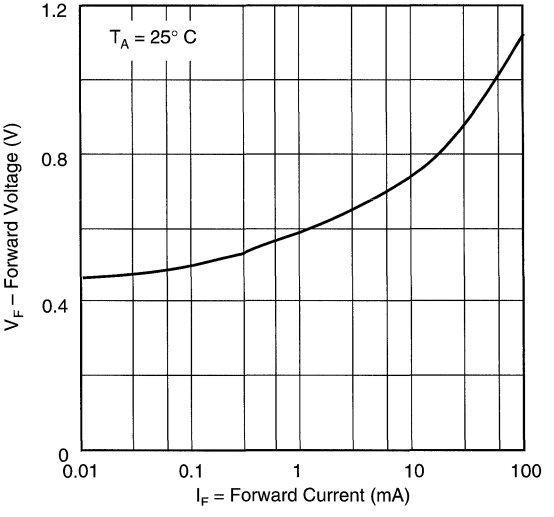


Figure 13

Low Frequency Reverse Dynamic Impedance

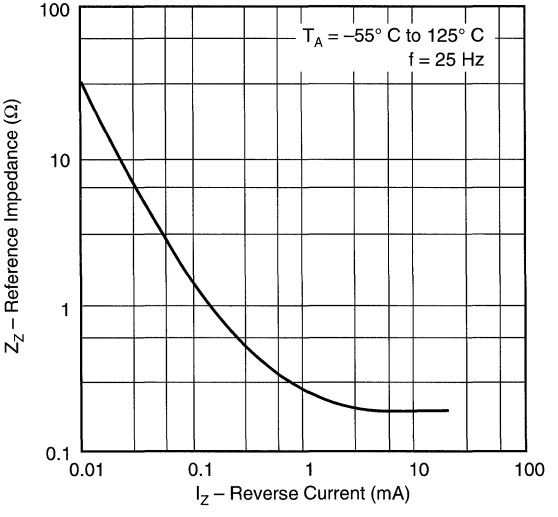


Figure 14

Typical Applications

1.235V Reference

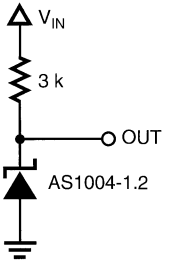


Figure 15

2.5V Reference

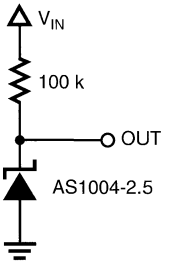


Figure 16

Low Noise Reference

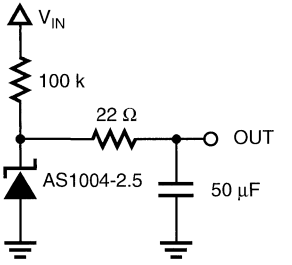


Figure 17

Variable Output Regulator

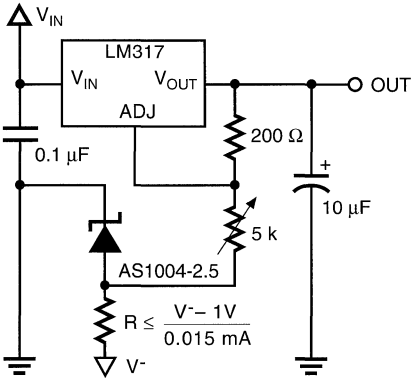


Figure 18

High Stability 5V Regulator

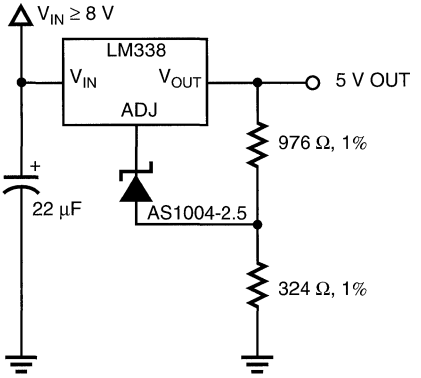


Figure 19

Lead Acid Low Battery Detector

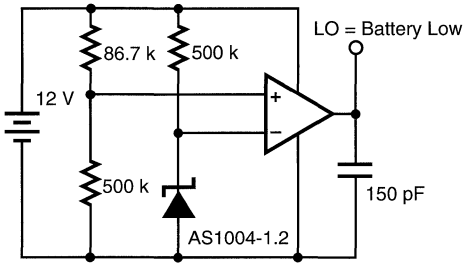


Figure 20

Micropower 10V Reference

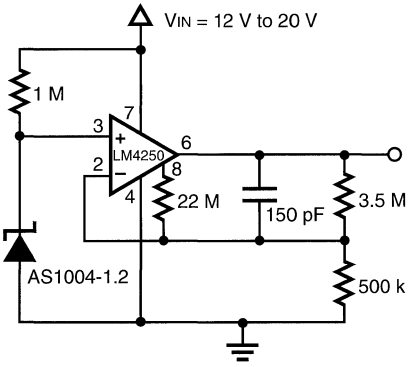


Figure 21

Notes

AS2842/3/4/5

Current Mode Controller

Features

- 2.5 V bandgap reference trimmed to 1.0% and temperature-compensated
- Extended temperature range from - 40 to 105° C
- AS2842/3 oscillations trimmed for precision duty cycle clamp
- AS2844/5 have exact 50% max duty cycle clamp
- Advanced oscillator design simplifies synchronization
- Improved specs on UVLO and hysteresis provide more predictable start-up and shutdown
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with current sense pulled below ground
- Over-temperature shutdown

Description

The AS2842 family of control ICs provide pin-for-pin replacement of the industry standard UC3842 series of devices. The devices are redesigned to provide significantly improved tolerances in power supply manufacturing. The 2.5 V reference has been trimmed to 1.0% tolerance. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping rather than specified discharge current. The circuit is more completely specified to guarantee all parameters impacting power supply manufacturing tolerances.

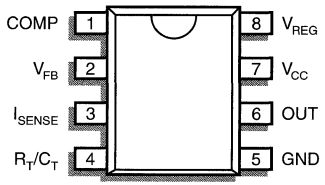
In addition, the oscillator and flip-flop sections have been enhanced to provide additional performance. The R_T/C_T pin now doubles as a synchronization input that can be easily driven from open collector/open drain logic outputs. This sync input is a high impedance input and can easily be used for externally clocked systems. The new flip-flop topology allows the duty cycle on the AS2844/5 to be guaranteed between 49 and 50%. The AS2843/5 requires less than 0.5 mA of start-up current over the full temperature range.

Ordering Information

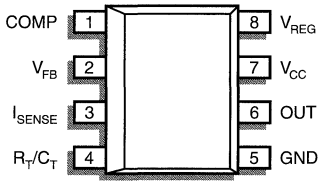
Description	Temperature Range	Order Codes
8-Pin Plastic DIP	-40 to 105° C	AS2842/3/4/5N
8-Pin Plastic SOIC	-40 to 105° C	AS2842/3/4/5D-8

Pin Configuration — Top view

PDIP (N)



8L SOIC (D)



Functional Block Diagram

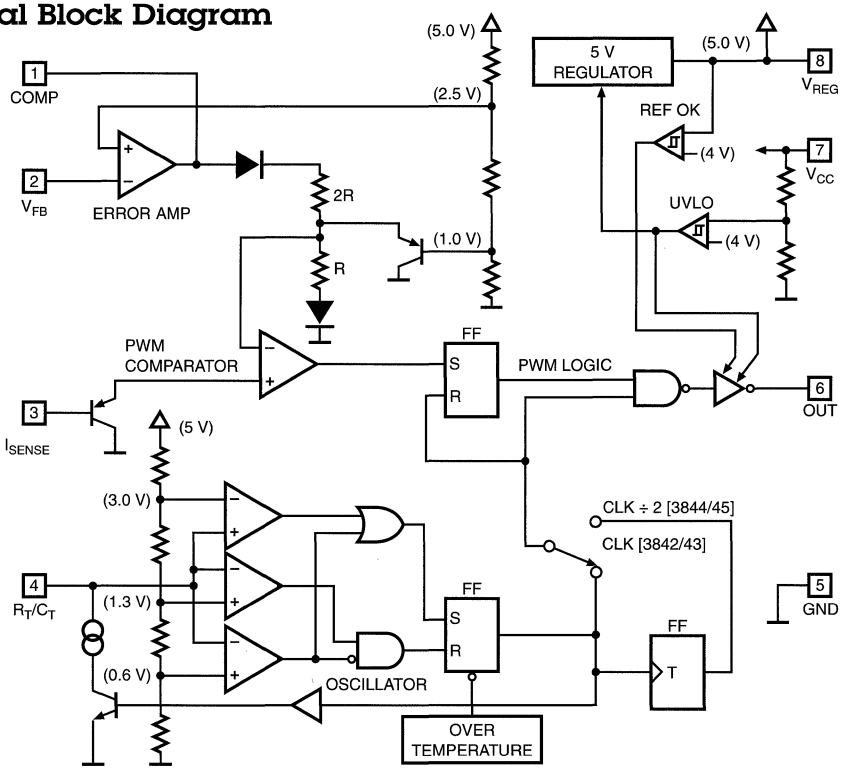


Figure 1. Block Diagram of the AS2842/3/4/5

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	I_{SENSE}	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	OUT	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the AS2844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (I_{CC} < 30 mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	µJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
AS2842,4		15	V
AS2843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
Line Regulation	PSRR	12 V_{CC} 25 V		2	10	mV
Load Regulation		1 I_{REG} 20 mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 Hz f 100 kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
Nominal Voltage	V_{FB}	T = 25° C; I_{REG} = 1 mA	2.475	2.500	2.525	V
Line Regulation	PSRR	12 V V_{CC} 25 V		2	5	mV
Load Regulation		1 I_{REG} 20 mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	T_J = 25° C	47	52	57	kHz
Voltage Stability		12 V V_{CC} 25 V		0.2	1	%
Temperature Stability[1]	TC_f	T_{MIN} T_J T_{MAX}		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Sync Threshold	V_{SYNC}		400	600	800	mV
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		R_T = 680 Ω, C_T = 5.3 nF, T_J = 25° C	46	50	52	%

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	T_J = 25° C	2.475	2.50	2.525	V
Input Bias Current	I_{BIAS}			–0.1	–1	µA
Voltage Gain	A_{VOL}	2 V_{COMP} 4 V	65	90		dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	12 V_{CC} 25 V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V, V_{COMP} = 1.1V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	0.8		mA
Output Swing High	V_{COMPH}	V_{FB} = 2.3 V, R_L = 15 kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	–0.2 V_{SENSE} 0.8 V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	V_{SENSE} = 0 V		1.5		V
Maximum Input Signal[2]		V_{COMP} = 5 V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	12 V_{CC} 25 V		70		dB
Input Bias Current	I_{BIAS}			–1	–10	µA
Propagation Delay to Output[1]	t_{PD}			85	150	ns
Output						
Output Low Level	V_{OL}	I_{SINK} = 20 mA		0.1	0.4	V
	V_{OL}	I_{SINK} = 200 mA		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5		V
	V_{OH}	I_{SOURCE} = 200mA	12	13.5		V
Rise Time[1]	t_R	C_L = 1 nF		50	150	ns
Fall Time[1]	t_F	C_L = 1 nF		50	150	ns
Housekeeping						
Start-up Threshold	V_{CC}(on)	2842/4	15	16	17	V
		2843/5	7.8	8.4	9.0	V
Minimum Operating Voltage	V_{CC}(min)	2842/4	9	10	11	V
After Turn On		2843/5	7.0	7.6	8.2	V
Output Low Level in UV State	V_{OUV}	I_{SINK} = 20 mA, V_{CC} = 6 V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (-40 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM						
Maximum Duty Cycle	D_{max}	2842/3	94	97	100	%
Minimum Duty Cycle	D_{min}	2842/3			0	%
Maximum Duty Cycle	D_{max}	2844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	2844/5			0	%
Supply Current						
Start-up Current	I_{CC}	2842/4, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 14 V 2843/5, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 7 V		0.5 0.3	1.0 0.5	mA mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25 mA		30		V

Notes:

1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \leq V_{SENSE} \leq 0.8\ V$$

4. At the over-temperature threshold, T_{OT}, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM latch, remain powered.

Typical Performance Curves

Supply Current vs Supply Voltage

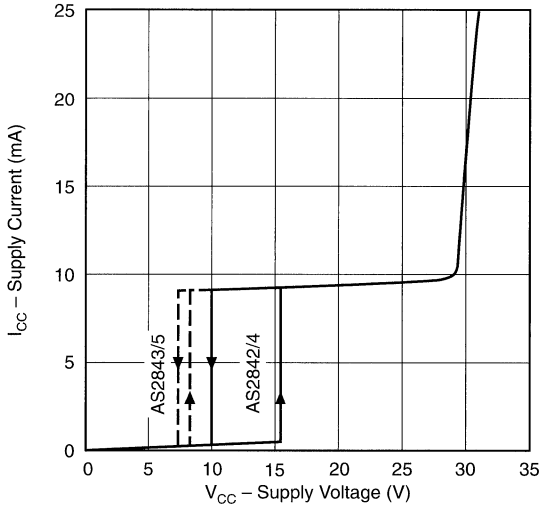


Figure 2

Output Voltage vs Supply Voltage

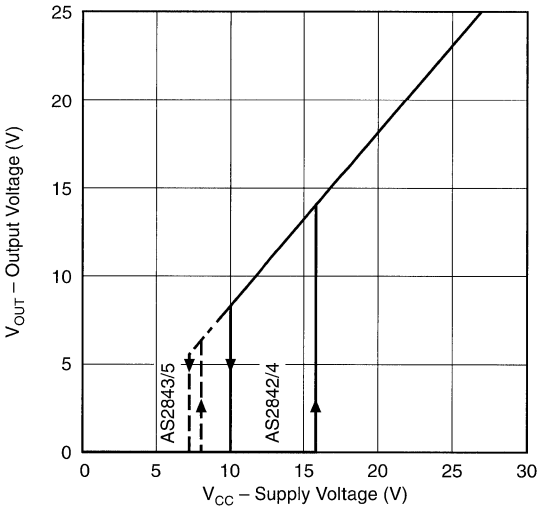


Figure 3

Regulator Output Voltage vs Ambient Temperature

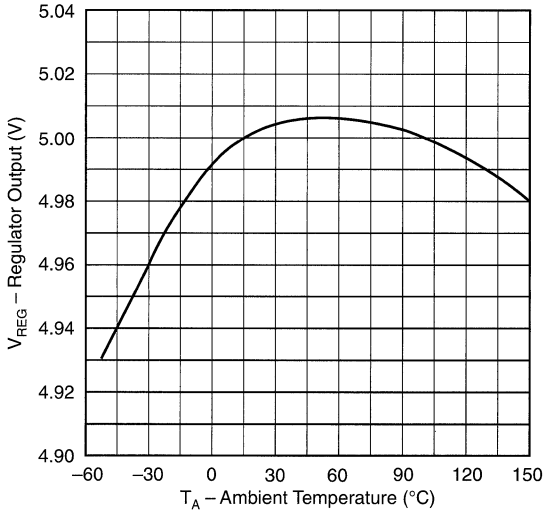


Figure 4

Regulator Short Circuit Current vs Ambient Temperature

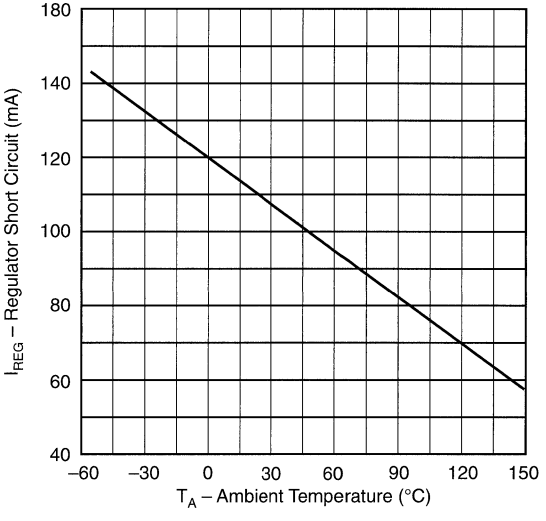


Figure 5

Typical Performance Curves

Regulator Load Regulation

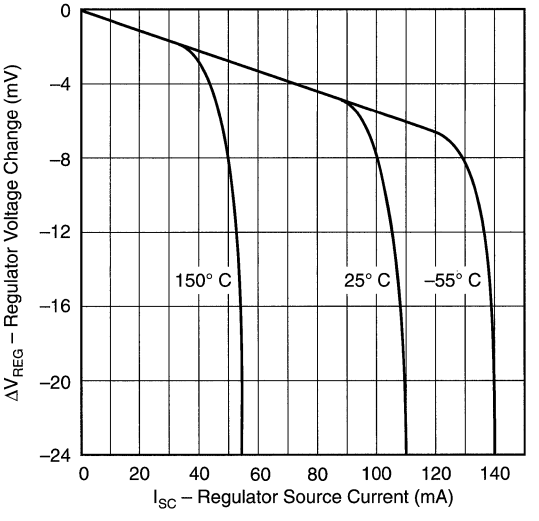


Figure 6

Maximum Duty Cycle vs Timing Resistor

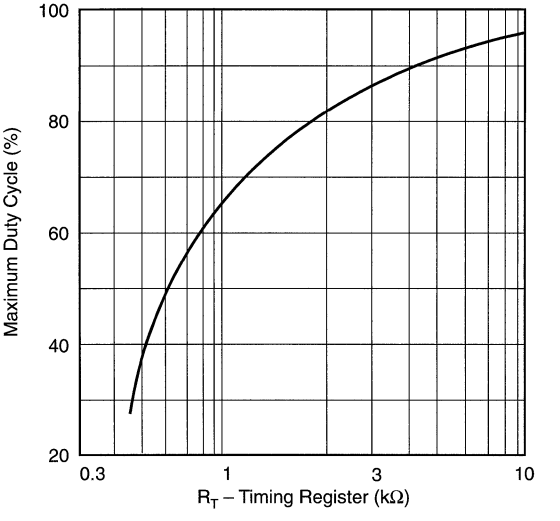


Figure 7

Timing Capacitor vs Oscillator Frequency

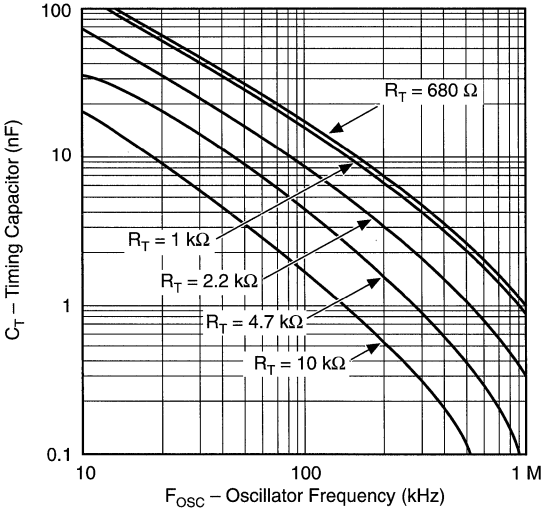


Figure 8

Maximum Duty Cycle Temperature Stability

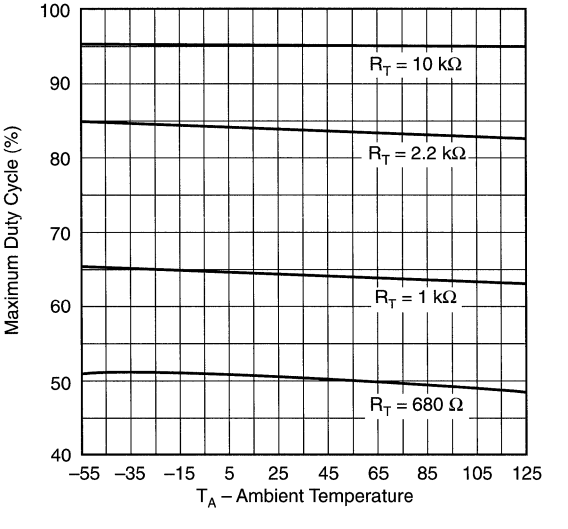


Figure 9

Typical Performance Curves

Current Sense Input Threshold vs Error Amp Output Voltage

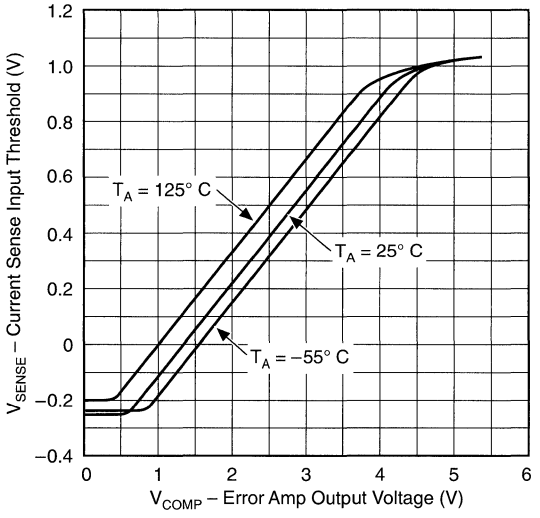


Figure 10

Error Amp Input Voltage vs Ambient Temperature

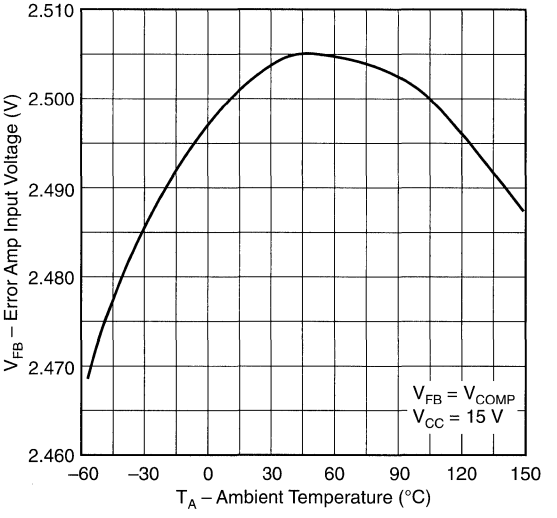


Figure 11

Output Sink Capability In Under-Voltage Mode

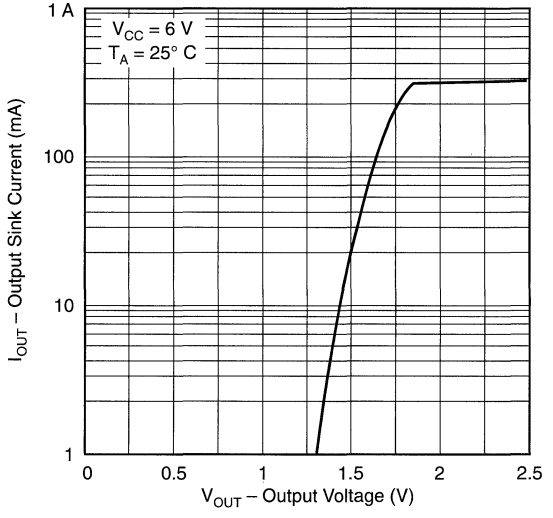


Figure 12

Output Saturation Voltage

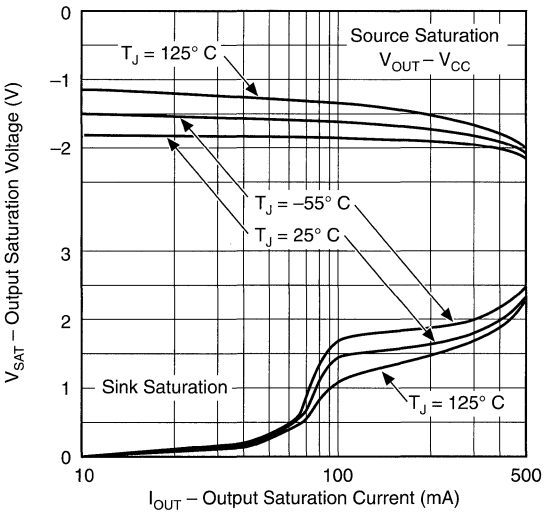


Figure 13

Application Information

The AS2842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC2842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line and DC-DC converters. The AS2842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105 °C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (±0.5% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 2844/45 types, and an improved 5 V regulator for better AC noise immunity. Furthermore, the AS2842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

Section 1— Theory of Operation

The functional block diagram of the AS2842 is shown in Figure 1. The IC is comprised of the six basic functions necessary to implement current mode control; the under voltage lockout; the reference; the oscillator; the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Undervoltage lockout (UVLO)

The undervoltage lockout function of the AS2842 holds the IC in a low quiescent current (1 mA) "standby" mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the IC's internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS2842 allows "bootstrapping"—a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply's main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is

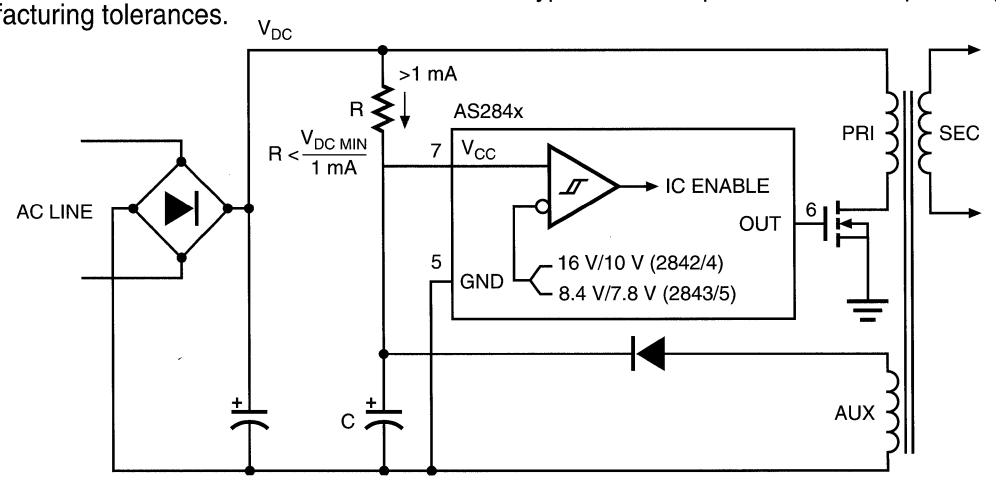


Figure 14. Bootstrap Circuit

charged via resistor (R) from the rectified AC line. When the voltage on the capacitor (V_{CC}) reaches the upper UVLO threshold, the IC (and hence, the power supply) turns on and the voltage on C begins to quickly discharge due to the increased operating current. During this time, the auxiliary winding begins to supply the current necessary to run the IC. The capacitor must be sufficiently large to maintain a voltage greater than the lower UVLO threshold during start up. The value of R must be selected to provide greater than 1 mA of current at the minimum DC bus voltage (R < VDCmin/1 mA).

The UVLO feature of the AS2842 has significant advantages over standard 2842 devices. First, the UVLO thresholds are based on a temperature compensated band gap reference rather than conventional zeners. Second, the UVLO disables the output at power down, offering additional protection in cases where V_{REG} is heavily decoupled. The UVLO on some 2842 devices shuts down the 5 volt regulator only, which results in eventual power down of the output only after the 5 volt rail collapses. This can lead to unwanted stresses on the switching devices during power down. The AS2842 has two separate comparators which monitor both V_{CC} and V_{REF} and hold the output low if either are not within specification.

The AS2842 family offers two different UVLO options. The AS2842/4 has UVLO thresholds of 16 volts (on) and 10 volts (off). The AS2843/5 has UVLO levels of 8.4 volts (on) and 7.6 volts (off).

1.2 Reference (V_{REG} and V_{FB})

The AS2842 effectively has two precise band gap based temperature compensated voltage references. Most obvious is the V_{REG} pin (pin 8) which is the output of a series pass regulator. This 5.0 V output is normally used to provide charging current to the oscillator's timing capacitor (Section 1.3). In addition, there is a trimmed internal 2.5 V reference which is connected to the non-inverting (+) input of the error amplifier. The tolerance of the internal reference is ±0.5% over the full specified temperature range, and ±1% for V_{REG}.

The reference section of the AS2842 is greatly improved over the standard 2842 in a number of ways. For example, in a closed loop system, the voltage at the error amplifier's inverting input (V_{FB}, pin 1) is forced by the loop to match the voltage at the non-inverting input. Thus, V_{FB} is the voltage which sets the accuracy of the entire system. The 2.5 V reference of the AS2842 is tightly trimmed for precision at V_{FB}, including errors caused by the op amp, and is specified over temperature. This method of trim provides a precise reference voltage for the error amplifier while maintaining the original 5 V regulator specifications. In addition, force/sense (Kelvin) bonding to the package pin is utilized to further improve the 5 V load regulation. Standard 2842's, on the other hand, specify tight regulation for the 5 V output only and rate it over line, load and temperature. The voltage at V_{FB}, which is of critical importance, is loosely specified and only at 25° C.

The reference section, in addition to providing a precise DC reference voltage, also powers most of the IC's internal circuitry. Switching noise, therefore, can be internally coupled onto the reference. With this in mind, all of the logic within the AS2842 was designed with ECL type circuitry which generates less switching noise because it runs at essentially constant current regardless of logic state. This, together with improved AC noise rejection, results in substantially less switching noise on the 5 V output.

The reference output is short circuit protected and can safely deliver more than 20 mA to power external circuitry.

1.3 Oscillator

The newly designed oscillator of the AS2842 is enhanced to give significantly improved performance. These enhancements are discussed in the following paragraphs. The basic operation of the oscillator is as follows:

A simple RC network is used to program the frequency and the maximum duty ratio of the AS2842 output. See Figure 15. Timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PWM latch, when the voltage across C_T reaches the upper oscillator trip point (3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS2842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS2844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing an absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T

The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T f_{OSC}} \quad (1)$$

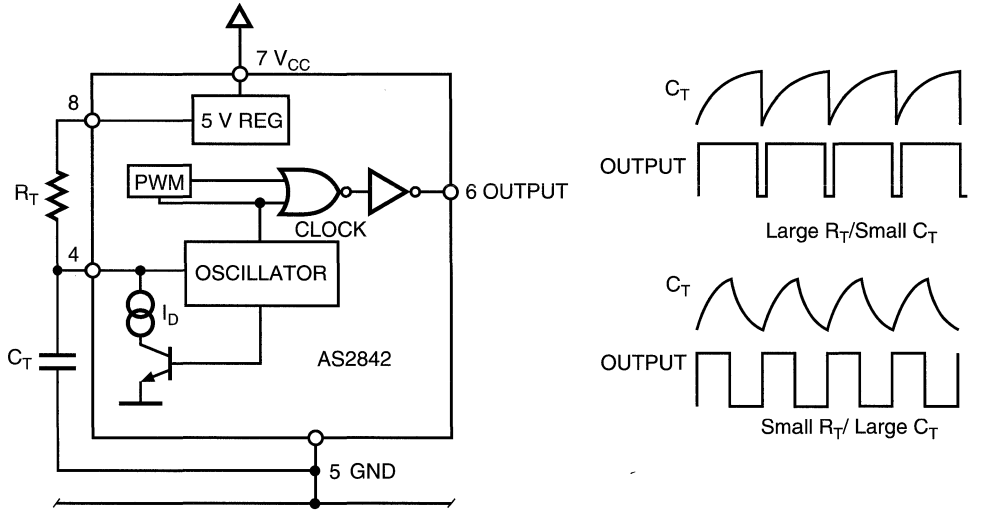


Figure 15. Oscillator Set-up and Waveforms

$$R_T = \frac{V_{REG}}{I_D} \cdot \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \quad (2)$$

$$= 582 \cdot \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$K_L = \frac{V_{REG} - V_L}{V_{REG}} \approx 0.736 \quad (3)$$

$$K_H = \frac{V_{REG} - V_H}{V_H} \approx 0.432 \quad (4)$$

where f_{osc} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the Reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683 . Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS2842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

1.3.2 Oscillator enhancements

The AS2842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, then I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufactur-

Table 1. R_T vs Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

ing. Standard 2842 devices specify or trim only for a specific value of discharge current. This makes precise and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS2844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard AS2844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

1.3.3 Synchronization

The advanced design of the AS2842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error amplifier (COMP)

The AS2842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5 V reference, and the inverting (–) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down and a 0.8 mA current source pull-up as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire "OR-ing" of the error amplifier outputs of several 2842s, or complete bypass of the error amplifier when its output is forced to remain in its "pull-up" condition.

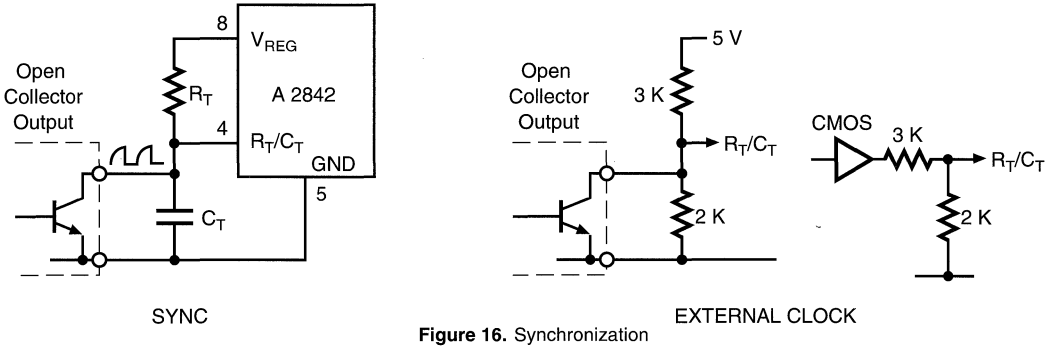


Figure 16. Synchronization

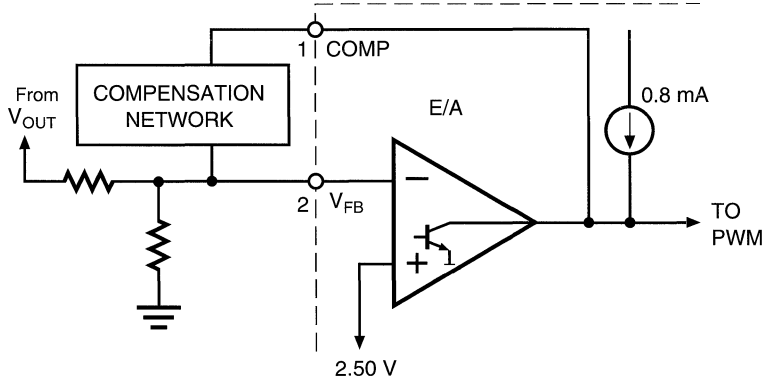


Figure 17. Error Amplifier Compensation

In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output from going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply - i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converters overall gain/phase response approaches that of a single pole with a –20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (> 45°) to ensure stability.

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57° C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula;

$$f_P = \frac{1}{2\pi\, R_f\, C_f} \qquad (5)$$

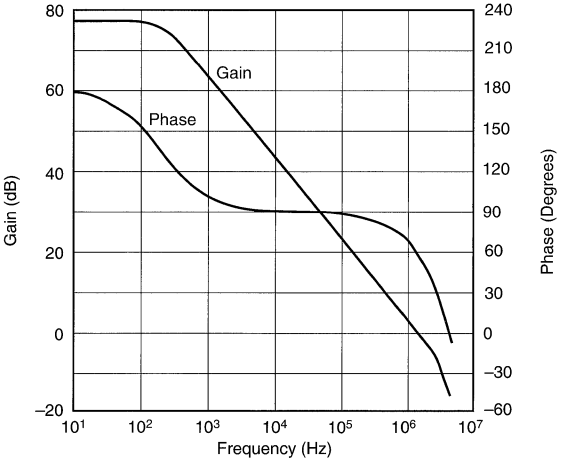


Figure 18. Gain/Phase Response of the AS2842

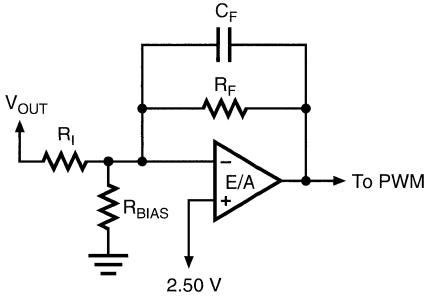


Figure 19. A Typical Compensation Network

Resistors R_1 and R_F set the low frequency gain and should be chosen to provide the highest possible gain, without exceeding the unity gain crossing frequency limit of f_{SW} /4. R_{BIAS}, in conjunction with R_1, sets the converter's output voltage; but has no effect on the loop gain/phase response.

There are a few converter design considerations associated with the error amplifier. First, the values of the divider network (R_1 and R_{BIAS}) should be kept low in order to minimize errors caused by the error amplifier's input bias current (–1.0 µA). An output voltage error equal to the product of the input bias current and the equivalent divider resistance, can be quite significant with divider values greater than 5 k . Low divider resistor values also help to improve the noise immunity of the sensitive V_{FB} input.

The second consideration is that the error amplifier will typically source only 0.8 mA; thus, the value of feedback resistance (R_F) should be no lower than 5 kΩ in order to maintain the error amplifier's full output range. In practice, however, the feedback resistance required is usually much greater than 5 kΩ, hence this limitation is normally not a problem.

Some power supply topologies may require a more elaborate compensation network. For example, flyback and boost converters operating with continuous current have transfer functions that include a right half plane (RHP) zero. These types of systems require an additional pole element within the compensation network. A detailed discussion of loop compensation, however, is beyond the scope of this application note.

1.5 I_{SENSE} current comparator/PWM latch

The current sense comparator (sometimes called the PWM comparator) and accompanying latch circuitry make up the pulse width modulator (PWM). It provides pulse-by-pulse current sensing/limiting and generates a variable duty ratio pulse train which controls the output voltage of the power supply. Included is a high speed comparator followed by ECL type logic circuitry which has very low propagation delays and switching noise. This is essential for high frequency power supply designs. The comparator has been designed to provide guaranteed performance with the current sense input below ground. The PWM latch ensures that only one pulse is allowed at the output for each oscillator period.

The inverting input to the current sense comparator is internally connected to the level shifted output of the error amplifier (V_E) as discussed in the previous section. The non-inverting input is the I_{SENSE} input (pin 3). It monitors the switched inductor current of the converter.

Figure 20 shows the current sense/PWM circuitry of the AS2842, and associated waveforms. The output is set high by an internal clock pulse and remains high until one of two conditions occur; 1) the oscillator times out (Section 1.3)or 2) the PWM latch is set by the current sense comparator. During the time when the output is high, the converter's switching device is turned on and current flows through resistor R_S. This produces a stepped ramp waveform at pin 3 as shown in Figure 20. The current will continue to ramp up until it reaches the level of V_E at the inverting input. At that point, the comparator's output goes high, setting the PWM latch and the output pulse is then terminated. Thus, V_E is a variable reference for the current sense comparator, and it controls the peak current sensed by R_S on a cycle-by-cycle basis. V_S varies in proportion to changes in the input voltage/current (inner control loop) while V_E varies in proportion to changes in the converters output voltage/current (outer control loop). The two control loops merge at the current sense comparator, producing a variable duty ratio pulse train that controls the output of the converter.

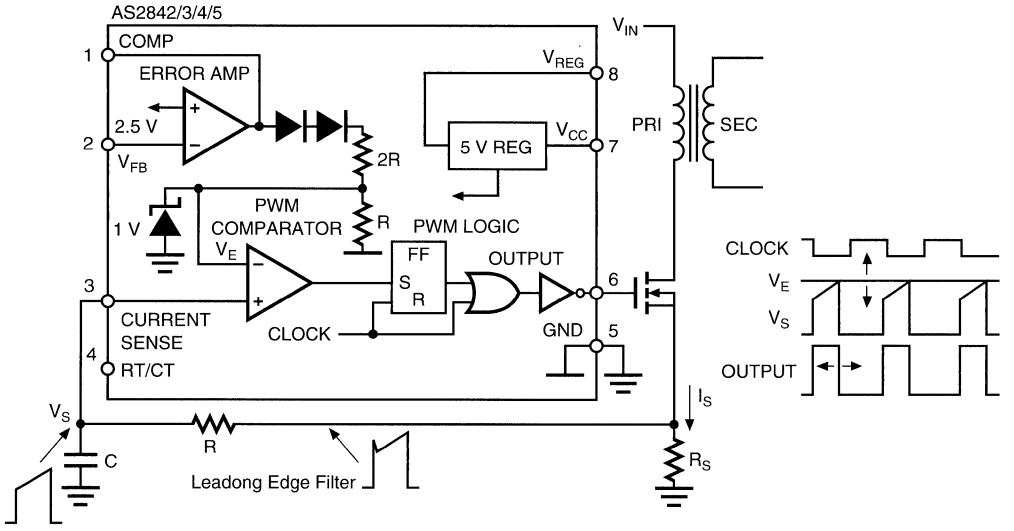


Figure 20. Current Sense/PWN Latch Circuit and Waveforms

The current sense comparator's inverting input is internally clamped to a level of 1.0 V to provide a current limit (or power limit for multiple output supplies) function. The value of R_S is selected to produce 1.0 V at the maximum allowed current. For example, if 1.5 A is the maximum allowed peak inductor current, then R_S is selected to equal 1 V/1.5 A = 0.66 Ω. In high power applications, power dissipation in the current sense resistor may become intolerable. In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

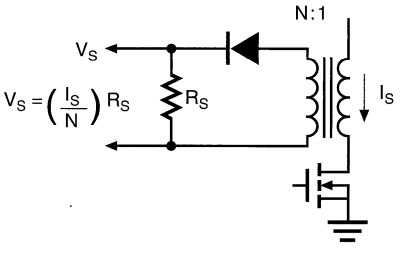


Figure 21. Optional Current Transformer

1.6 Output (OUT)

The output stage of the AS2842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourcing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During undervoltage shutdown conditions, the output is active low. This eliminates the need for an external pulldown resistor.

1.7 Over-temperature shutdown

The AS2842 has a built-in over-temperature shutdown which will limit the die temperature to 130° C typically. When the over-temperature condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM

latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 – Design Considerations

2.1 Leading edge filter

The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode(s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$C = \frac{\text{Time Constant}}{1\ \text{k}\Omega} \qquad (6)$$

$$= \frac{100\ \text{ns}}{1\ \text{k}\Omega}$$

$$= 100\ \text{pF}$$

2.2 Slope compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations when operated at duty ratios greater than 50%. Two different phenomena can occur as shown

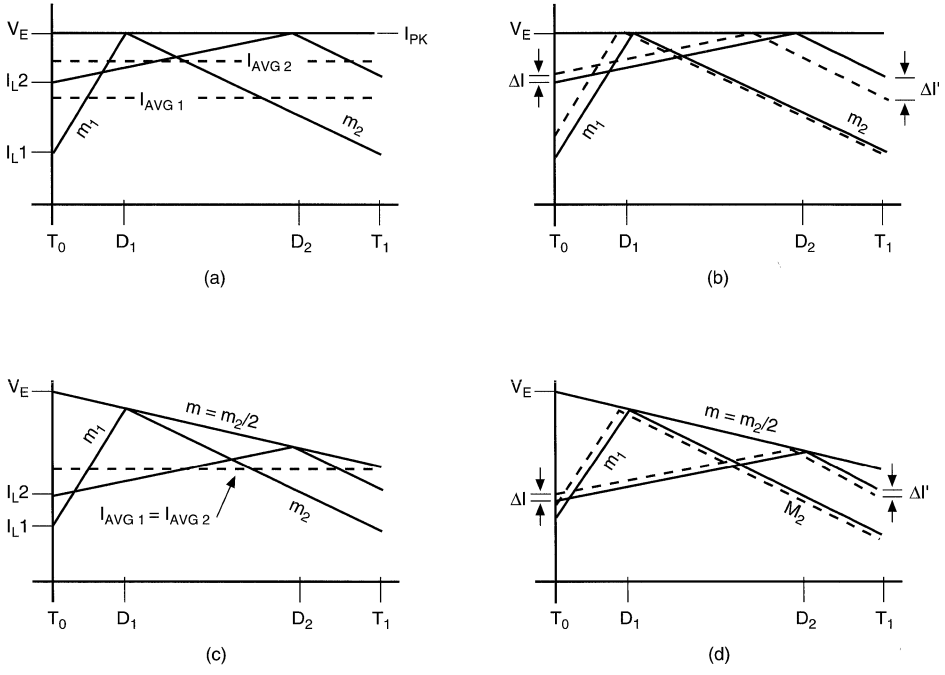


Figure 22. Slope Compensation

graphically in Figure 22.

First, current-mode controllers detect and control the peak inductor current, where as the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (I) can result in an unstable condition. For duty ratios less than 50 %, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50 %, I progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in Figure 22(c) & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a positive ramp waveform is readily available from the oscillator at pin 4, it is more practical to add the slope compensation to the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23(a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than 1/2 the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \qquad (7)$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies

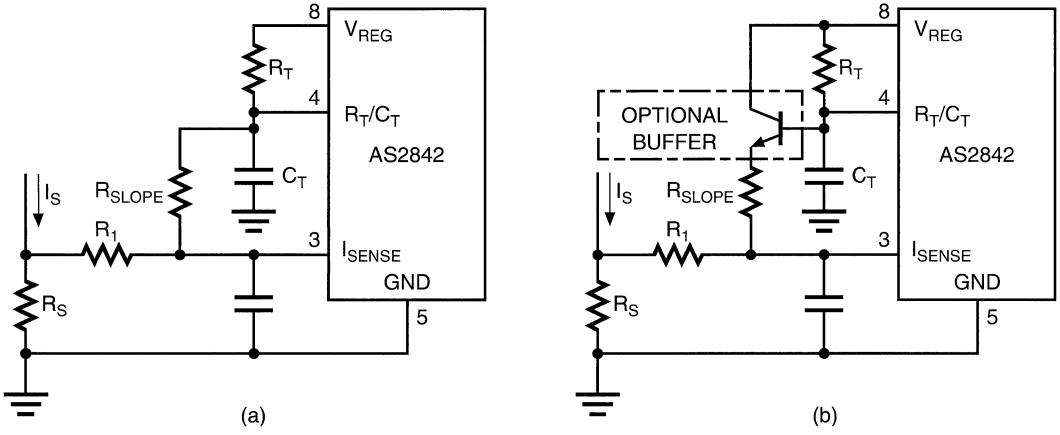


Figure 23. Slope Compensation

operating under very light load can experience instabilities caused by the low amplitude of the current sense ramp waveform. In such a case, any noise on the waveform can be sufficient to trip the comparator resulting in random and premature pulse termination. The addition of a small amount of artificial ramp (slope compensation) can eliminate such problems without drastically affecting the overall performance of the system.

2.3 Circuit layout and other considerations

The electronic noise generated by any switch-mode power supply can cause severe stability problems if the circuit is not layed-out (wired) properly. A few simple layout practices will help to minimize noise problems.

When building prototype breadboards, never use plug-in protoboards or wire wrap construction. For best results, do all breadboarding on double sided PCB using ground plane techniques. Keep all traces and lead lengths to a minimum. Avoid large loops and keep the area enclosed within any loops to a minimum. Use common point grounding techniques and separate the power ground traces from the signal ground traces. Locate the control IC and circuitry away from switching devices and magnetics. Also, the timing capacitor's ground connection must be right at pin 5 as shown in Figure 15. These grounding and wiring techniques are very important because the resistance and inductance of the traces are significant enough to generate noise glitches which can disrupt the normal operation of the IC.

Also, to provide a low impedance path for high frequency noise, V_{CC} and V_{REF} should be decoupled to IC ground with 0.1 µF capacitors. Additional decoupling in other sensitive areas may also be necessary. It is very important to locate the decoupling capacitors as close as possible to the circuit being decoupled.

AS3842/3/4/5

Current Mode Controller

Features

- 2.5 V bandgap reference trimmed to 1.0% and temperature-compensated
- Standard temperature range extended to 105° C
- AS3842/3 oscillations trimmed for precision duty cycle clamp
- AS3844/5 have exact 50% max duty cycle clamp
- Advanced oscillator design simplifies synchronization
- Improved specs on UVLO and hysteresis provide more predictable start-up and shutdown
- Improved 5 V regulator provides better AC noise immunity
- Guaranteed performance with current sense pulled below ground

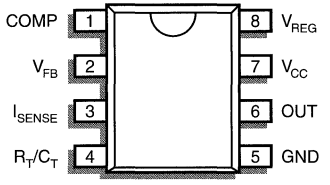
Description

The AS3842 family of control ICs provide pin-for-pin replacement of the industry standard UC3842 series of devices. The devices are redesigned to provide significantly improved tolerances in power supply manufacturing. The 2.5 V reference has been trimmed to 1.0% tolerance. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping rather than specified discharge current. The circuit is more completely specified to guarantee all parameters impacting power supply manufacturing tolerances.

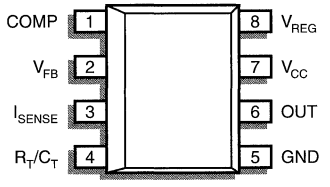
In addition, the oscillator and flip-flop sections have been enhanced to provide additional performance. The R_T/C_T pin now doubles as a synchronization input that can be easily driven from open collector/open drain logic outputs. This sync input is a high impedance input and can easily be used for externally clocked systems. The new flip-flop topology allows the duty cycle on the AS3844/5 to be guaranteed between 49 and 50%. The AS3843/5 requires less than 0.5 mA of start-up current over the full temperature range.

Pin Configuration — Top view

PDIP (N)



8L SOIC (D)



Ordering Information

Description	Temperature Range	Order Codes
8-Pin Plastic DIP	0 to 105° C	AS3842/3/4/5N
8-Pin Plastic SOIC	0 to 105° C	AS3842/3/4/5D-8

Functional Block Diagram

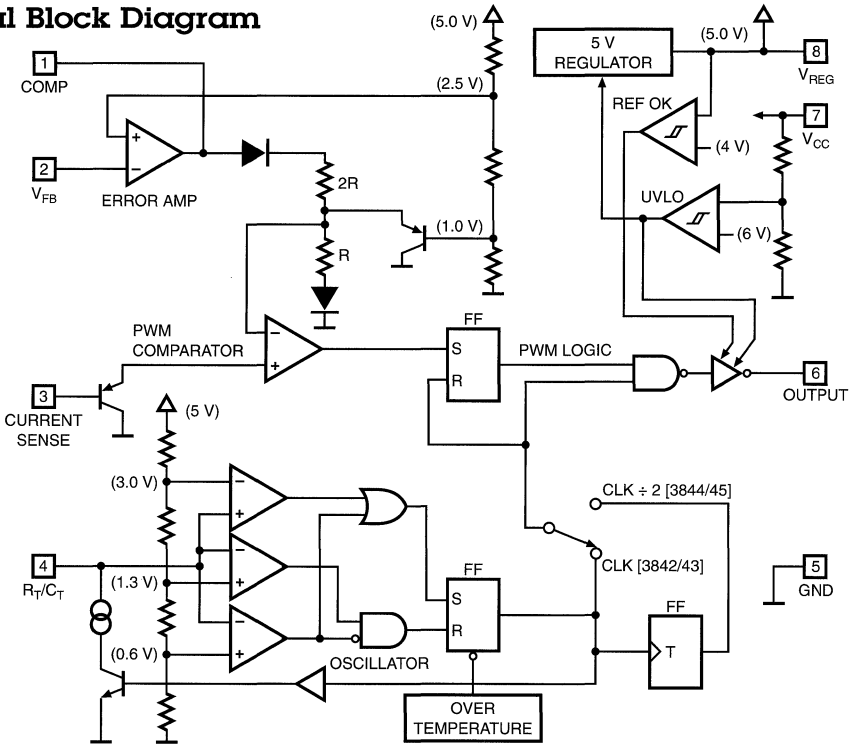


Figure 1. Block Diagram of the AS3842/3/4/5

Pin Function Description

Pin Number	Function	Description
1	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
2	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
3	Current Sense	A voltage proportional to inductor current is connected to the input. The PWM uses this information to terminate the gate drive of the output.
4	R_T/C_T	Oscillator frequency and maximum output duty cycle are set by connecting a resistor (R_T) to V_{REG} and a capacitor (C_T) to ground. Pulling this pin to ground or to V_{REG} will accomplish a synchronization function.
5	GND	Circuit common ground, power ground, and IC substrate.
6	Output	This output is designed to directly drive a power MOSFET switch. This output can sink or source peak currents up to 1A. The output for the AS3844/5 switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply voltage for the IC.
8	V_{REG}	This 5 V regulated output provides charging current for the capacitor C_T through the resistor R_T.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (I_{CC} < 30 mA)	V_{CC}	Self-Limiting	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Output Current	I_{OUT}	±1	A
Output Energy (Capacitive Load)		5	µJ
Analog Inputs (Pin 2, Pin 3)		−0.3 to 30	V
Error Amp Sink Current		10	mA
Maximum Power Dissipation	P_D		
8L SOIC		750	mW
8L PDIP		1000	mW
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}		
AS3842,4		15	V
AS3843,5		10	V
Oscillator	f_{OSC}	50 to 500	kHz

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
8L PDIP	95° C/W	50° C/W	10.5 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	T_J = 25° C, I_{REG} = 1 mA	4.95	5.00	5.05	V
Line Regulation	PSRR	12 V_{CC} 25 V		2	10	mV
Load Regulation		1 I_{REG} 20 mA		2	10	mV
Temperature Stability[1]	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation[1]		Line, load, temperature	4.85		5.15	V
Long-term Stability[1]		Over 1,000 hrs at 25° C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 Hz f 100 kHz, T_J = 25° C		50		µV
Short Circuit Current	I_{SC}		30	100	180	mA
2.5 V Internal Reference						
Nominal Voltage	V_{FB}	T = 25° C; I_{REG} = 1 mA	2.475	2.500	2.525	V
Line Regulation	PSRR	12 V V_{CC} 25 V		2	5	mV
Load Regulation		1 I_{REG} 20 mA		2	5	mV
Temperature Stability[1]	TC_{VFB}			0.1	0.2	mV/°C
Total Output Variation[1]		Line, load, temperature	2.450	2.500	2.550	V
Long-term Stability[1]		Over 1,000 hrs at 125° C		2	12	mV
Oscillator						
Initial Accuracy	f_{OSC}	T_J = 25° C	47	52	57	kHz
Voltage Stability		12 V V_{CC} 25 V		0.2	1	%
Temperature Stability[1]	TC_f	T_{MIN} T_J T_{MAX}		5		%
Amplitude	f_{OSC}	$V_{RT/CT}$ peak-to-peak		1.6		V
Upper Trip Point	V_H			2.9		V
Lower Trip Point	V_L			1.3		V
Sync Threshold	V_{SYNC}		400	600	800	mV
Discharge Current	I_D		7.5	8.7	9.5	mA
Duty Cycle Limit		R_T = 680 Ω, C_T = 5.3 nF, T_J = 25° C	46	50	52	%

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	T_J = 25° C	2.475	2.500	2.525	V
Input Bias Current	I_{BIAS}			–0.1	–1	µA
Voltage Gain	A_{VOL}	2 V_{COMP} 4 V	65	90	1	dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth[1]	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	12 V_{CC} 25 V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V, V_{COMP} = 1.1V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	0.8		mA
Output Swing High	V_{COMPH}	V_{FB} = 2.3 V, R_L = 15 kΩ to Ground	5	5.5		V
Output Swing Low	V_{COMPL}	V_{FB} = 2.7 V, R_L = 15 kΩ to Pin 8		0.7	1.1	V
Current Sense Comparator						
Transfer Gain[2,3]	AV_{CS}	–0.2 V_{SENSE} 0.8 V	2.85	3.0	3.15	V/V
I_{SENSE} Level Shift[2]	V_{LS}	V_{SENSE} = 0 V		1.5		V
Maximum Input Signal[2]		V_{COMP} = 5 V	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	12 V_{CC} 25 V		70		dB
Input Bias Current	I_{BIAS}			–1	–10	µA
Propagation Delay to Output[1]	t_{PD}			85	150	ns
Output						
Output Low Level	V_{OL}	I_{SINK} = 20 mA		0.1	0.4	V
	V_{OL}	I_{SINK} = 200 mA		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20mA	13	13.5		V
	V_{OH}	I_{SOURCE} = 200mA	12	13.5		V
Rise Time[1]	t_R	C_L = 1 nF		50	150	ns
Fall Time[1]	t_F	C_L = 1 nF		50	150	ns
Housekeeping						
Start-up Threshold	V_{CC}(on)	3842/4	15	16	17	V
		3843/5	7.8	8.4	9.0	V
Minimum Operating Voltage	V_{CC}(min)	3842/4	9	10	11	V
After Turn On		3843/5	7.0	7.6	8.2	V
Output Low Level in UV State	V_{OUV}	I_{SINK} = 20 mA, V_{CC} = 6 V		1.5	2.0	V
Over-Temperature Shutdown[4]	T_{OT}			125		°C

Electrical Characteristics (cont'd)

Electrical characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: V_{CC} = 15 V, R_T = 10 kΩ, and C_T = 3.3 nF, unless otherwise stated. To override UVLO, V_{CC} should be raised above 17 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PWM						
Maximum Duty Cycle	D_{max}	3842/3	94	97	100	%
Minimum Duty Cycle	D_{min}	3842/3			0	%
Maximum Duty Cycle	D_{max}	3844/5	49	49.5	50	%
Minimum Duty Cycle	D_{min}	3844/5			0	%
Supply Current						
Start-up Current	I_{CC}	3842/4, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 14 V		0.5	1.0	mA
		3843/5, V_{FB} = V_{SENSE} = 0 V, V_{CC} = 7 V		0.3	0.5	mA
Operating Supply Current	I_{CC}			9	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} = 25 mA		30		V

Notes:
1. This parameter is not 100% tested in production.
2. Parameter measured at trip point of PWM latch.
3. Transfer gain is the relationship between current sense input and corresponding error amplifier output at the PWM latch trip point and is mathematically expressed as follows:

$$A = \frac{\Delta I_{COMP}}{\Delta V_{SENSE}}; -0.2 \leq V_{SENSE} \leq 0.8\ V$$

4. At the over-temperature threshold, T_{OT}, the oscillator is disabled. The 5 V reference and the PWM stages, including the PWM latch, remain powered.

Typical Performance Curves

Supply Current vs Supply Voltage

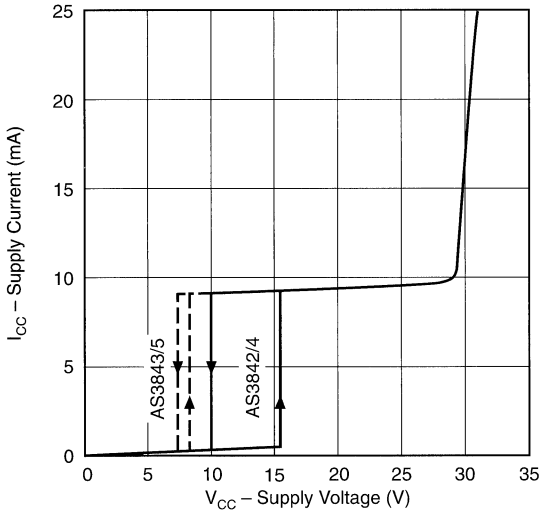


Figure 2

Output Voltage vs Supply Voltage

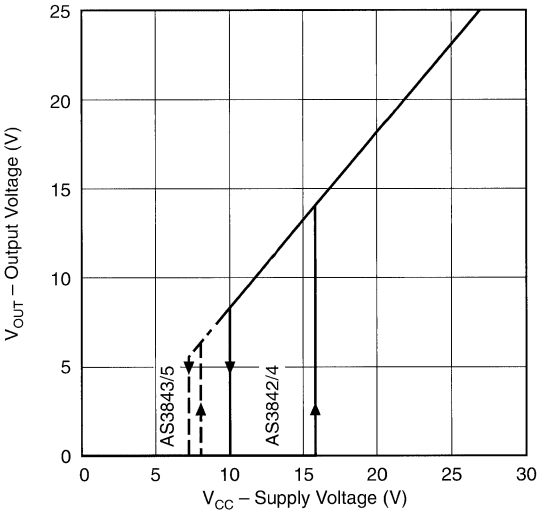


Figure 3

Regulator Output Voltage vs Ambient Temperature

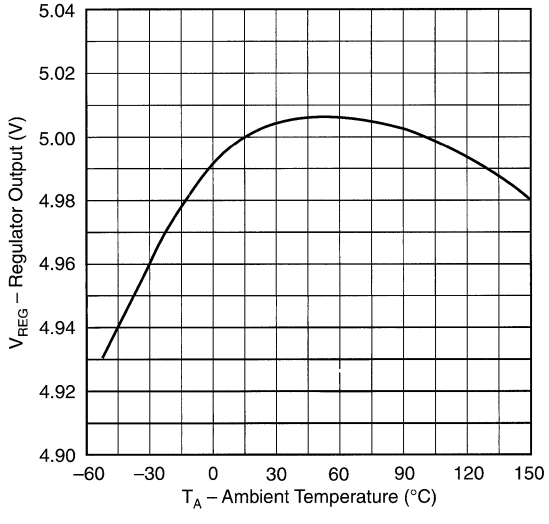


Figure 4

Regulator Short Circuit Current vs Ambient Temperature

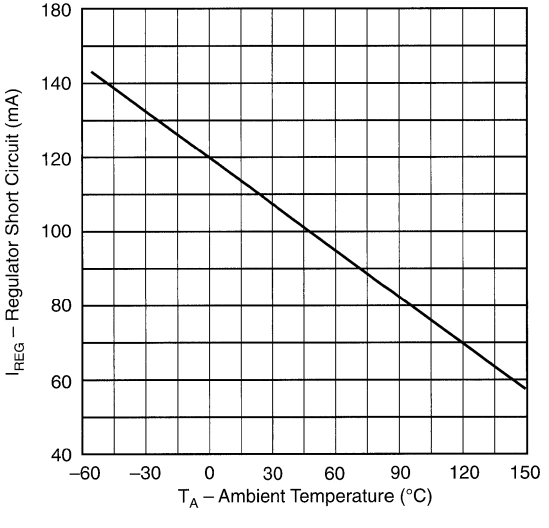


Figure 5

Typical Performance Curves

Regulator Load Regulation

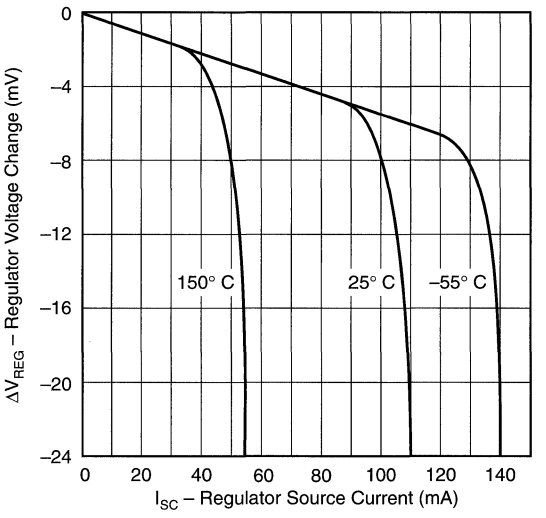


Figure 6

Maximum Duty Cycle vs Timing Resistor

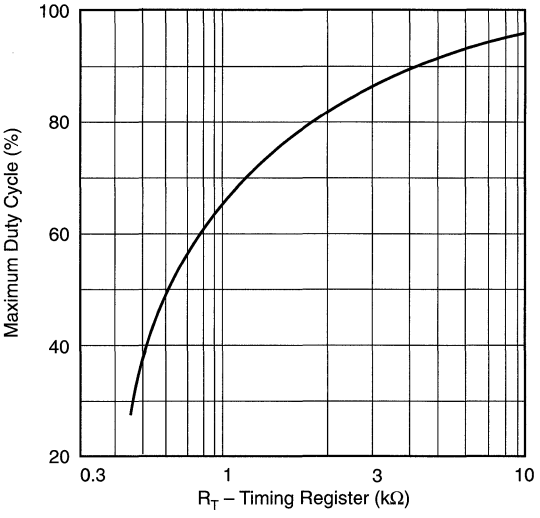


Figure 7

Timing Capacitor vs Oscillator Frequency

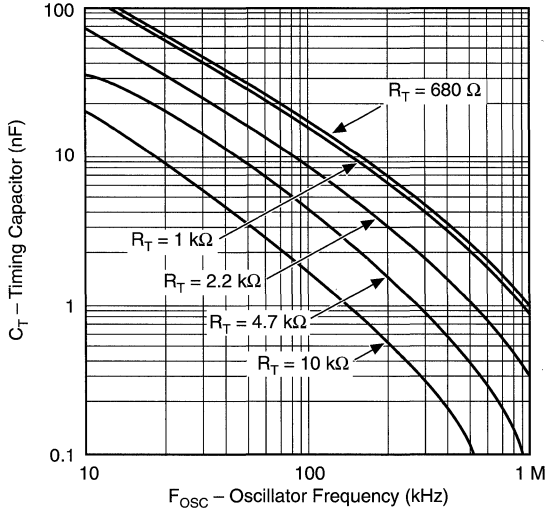


Figure 8

Maximum Duty Cycle Temperature Stability

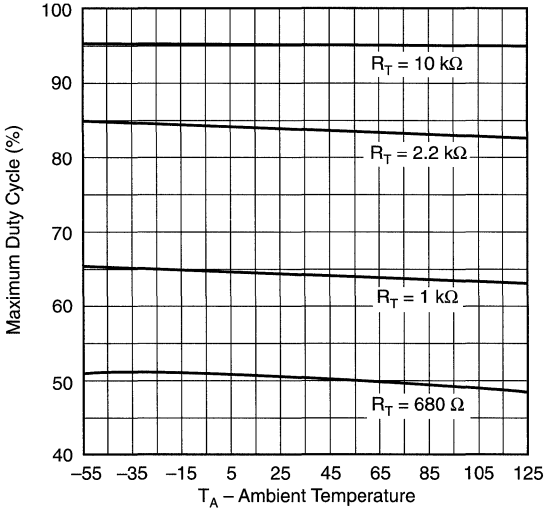


Figure 9

Typical Performance Curves

Current Sense Input Threshold vs Error Amp Output Voltage

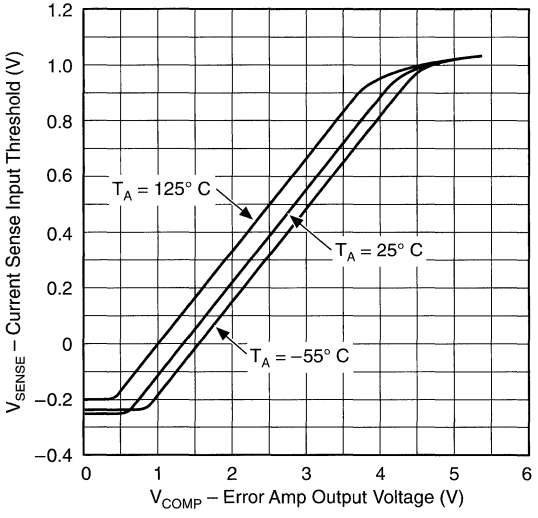


Figure 10

Error Amp Input Voltage vs Ambient Temperature

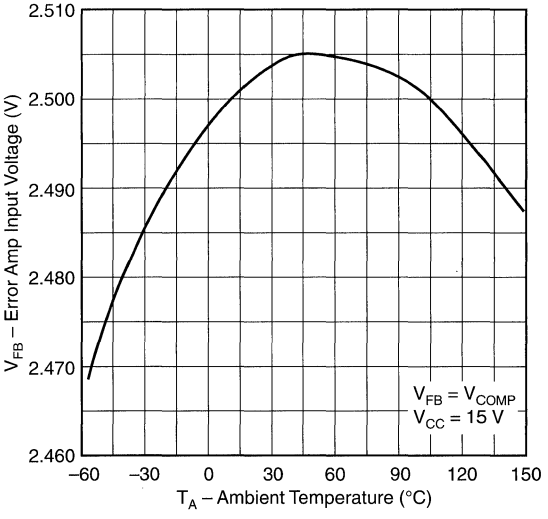


Figure 11

Output Sink Capability In Under-Voltage Mode

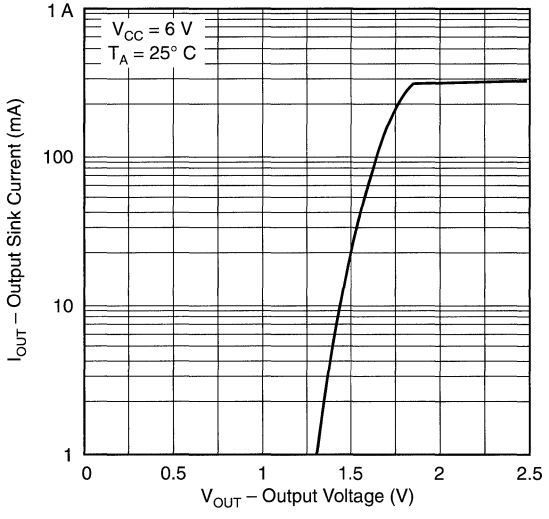


Figure 12

Output Saturation Voltage

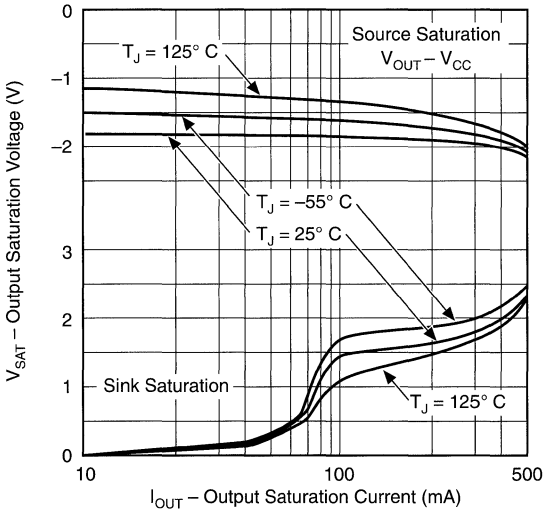


Figure 13

Application Information

The AS3842/3/4/5 family of current-mode control ICs are low cost, high performance controllers which are pin compatible with the industry standard UC3842 series of devices. Suitable for many switch mode power supply applications, these ICs have been optimized for use in high frequency off-line and DC-DC converters. The AS3842 has been enhanced to provide significantly improved performance, resulting in exceptionally better tolerances in power supply manufacturing. In addition, all electrical characteristics are guaranteed over the full 0 to 105 °C temperature range. Among the many enhancements are: a precision trimmed 2.5 volt reference (+/- 1% of nominal at the error amplifier input), a significantly reduced propagation delay from current sense input to the IC output, a trimmed oscillator for precise duty-cycle clamping, a modified flip-flop scheme that gives a true 50% duty ratio clamp on 3844/45 types, and an improved 5 V regulator for better AC noise immunity. Furthermore, the AS3842 provides guaranteed performance with current sense input below ground. The advanced oscillator design greatly simplifies synchronization. The device is more completely specified to guarantee all parameters that impact power supply manufacturing tolerances.

Section 1— Theory of Operation

The functional block diagram of the AS3842 is shown in Figure 01. The IC is comprised of the six basic functions necessary to implement current mode control; the under-voltage lockout; the reference; the oscillator; the error amplifier; the current sense comparator/PWM latch; and the output. The following paragraphs will describe the theory of operation of each of the functional blocks.

1.1 Under-voltage lockout (UVLO)

The under-voltage lockout function of the AS3842 holds the IC in a low quiescent current (1 mA) "standby" mode until the supply voltage (V_{CC}) exceeds the upper UVLO threshold voltage. This guarantees that all of the IC's internal circuitry are properly biased and fully functional before the output stage is enabled. Once the IC turns on, the UVLO threshold shifts to a lower level (hysteresis) to prevent V_{CC} oscillations.

The low quiescent current standby mode of the AS3842 allows "bootstrapping"—a technique used in off-line converters to start the IC from the rectified AC line voltage initially, after which power to the IC is provided by an auxiliary winding off the power supply's main transformer. Figure 14 shows a typical bootstrap circuit where capacitor (C) is

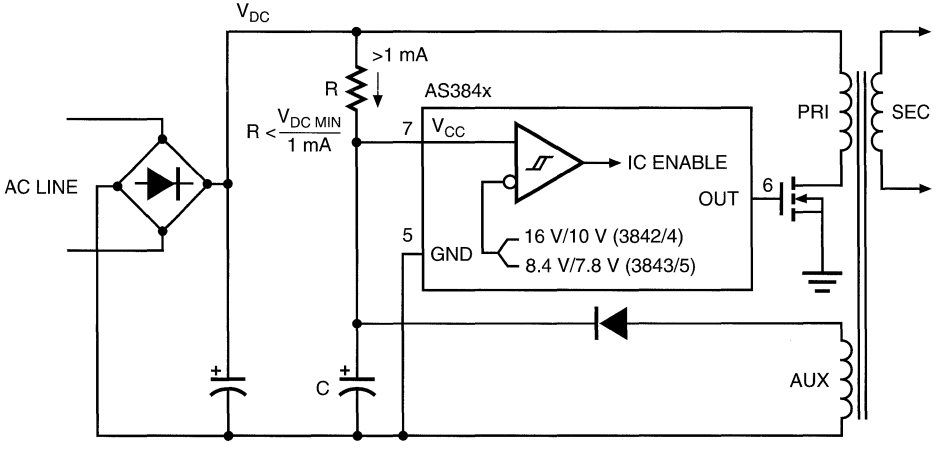


Figure 14. Bootstrap Circuit

charged via resistor (R) from the rectified AC line. When the voltage on the capacitor (V_{CC}) reaches the upper UVLO threshold, the IC (and hence, the power supply) turns on and the voltage on C begins to quickly discharge due to the increased operating current. During this time, the auxiliary winding begins to supply the current necessary to run the IC. The capacitor must be sufficiently large to maintain a voltage greater than the lower UVLO threshold during start up. The value of R must be selected to provide greater than 1 mA of current at the minimum DC bus voltage (R < VDCmin/1 mA).

The UVLO feature of the AS3842 has significant advantages over standard 3842 devices. First, the UVLO thresholds are based on a temperature compensated band gap reference rather than conventional zeners. Second, the UVLO disables the output at power down, offering additional protection in cases where V_{REG} is heavily decoupled. The UVLO on some 3842 devices shuts down the 5 volt regulator only, which results in eventual power down of the output only after the 5 volt rail collapses. This can lead to unwanted stresses on the switching devices during power down. The AS3842 has two separate comparators which monitor both V_{CC} and V_{REF} and hold the output low if either are not within specification.

The AS3842 family offers two different UVLO options. The AS3842/4 has UVLO thresholds of 16 volts (on) and 10 volts (off). The AS3843/5 has UVLO levels of 8.4 volts (on) and 7.6 volts (off).

1.2 Reference (V_{REG} and V_{FB})

The AS3842 effectively has two precise band gap based temperature compensated voltage references. Most obvious is the V_{REG} pin (pin 8) which is the output of a series pass regulator. This 5.0 V output is normally used to provide charging current to the oscillator's timing capacitor (Section 1.3). In addition, there is a trimmed internal 2.5 V reference which is connected to the non-inverting (+) input of the error amplifier. The tolerance of the internal reference is ± 1% over the full specified temperature range, and ± 1% for V_{REG}.

The reference section of the AS3842 is greatly improved over the standard 3842 in a number of ways. For example, in a closed loop system, the voltage at the error amplifier's inverting input (V_{FB}, pin 1) is forced by the loop to match the voltage at the non-inverting input. Thus, V_{FB} is the voltage which sets the accuracy of the entire system. The 2.5 V reference of the AS3842 is tightly trimmed for precision at V_{FB}, including errors caused by the op amp, and is specified over temperature. This method of trim provides a precise reference voltage for the error amplifier while maintaining the original 5 V regulator specifications. In addition, force/sense (Kelvin) bonding to the package pin is utilized to further improve the 5 V load regulation. Standard 3842's, on the other hand, specify tight regulation for the 5 V output only and rate it over line, load and temperature. The voltage at V_{FB}, which is of critical importance, is loosely specified and only at 25° C.

The reference section, in addition to providing a precise DC reference voltage, also powers most of the IC's internal circuitry. Switching noise, therefore, can be internally coupled onto the reference. With this in mind, all of the logic within the AS3842 was designed with ECL type circuitry which generates less switching noise because it runs at essentially constant current regardless of logic state. This, together with improved AC noise rejection, results in substantially less switching noise on the 5 V output.

The reference output is short circuit protected and can safely deliver more than 20 mA to power external circuitry.

1.3 Oscillator

The newly designed oscillator of the AS3842 is enhanced to give significantly improved performance. These enhancements are discussed in the following paragraphs. The basic operation of the oscillator is as follows:

A simple RC network is used to program the frequency and the maximum duty ratio of the AS3842 output. See Figure 15. Timing capacitor (C_T) is charged through timing resistor (R_T) from the fixed 5.0 V at V_{REG}. During the charging time, the OUT (pin 6) is high. Assuming that the output is not terminated by the PWM latch, when the voltage across C_T reaches the upper oscillator trip point (3.0 V), an internal current sink from pin 4 to ground is turned on and discharges C_T towards the lower trip point. During this discharge time, an internal clock pulse blanks the output to its low state. When the voltage across C_T reaches the lower trip point (1.3 V), the current sink is turned off, the output goes high, and the cycle repeats. Since the output is blanked during the discharge of C_T, it is the discharge time which controls the output deadtime and hence, the maximum duty ratio.

The nature of the AS3842 oscillator circuit is such that, for a given frequency, many combinations of R_T and C_T are possible. However, only one value of R_T will yield the desired maximum duty ratio at a given frequency. Since a precise maximum duty ratio clamp is critical for many power supply designs, the oscillator discharge current is trimmed in a unique manner which provides significantly improved tolerances as explained later in this section. In addition, the AS3844/5 options have an internal flip-flop which effectively blanks every other output pulse (the oscillator runs at twice the output frequency), providing an absolute maximum 50% duty ratio regardless of discharge time.

1.3.1 Selecting timing components R_T and C_T

The values of R_T and C_T can be determined mathematically by the following expressions:

$$C_T = \frac{D}{R_T f_{OSC} \ln\left(\frac{K_L}{K_H}\right)} = \frac{1.63D}{R_T f_{OSC}} \quad (1)$$

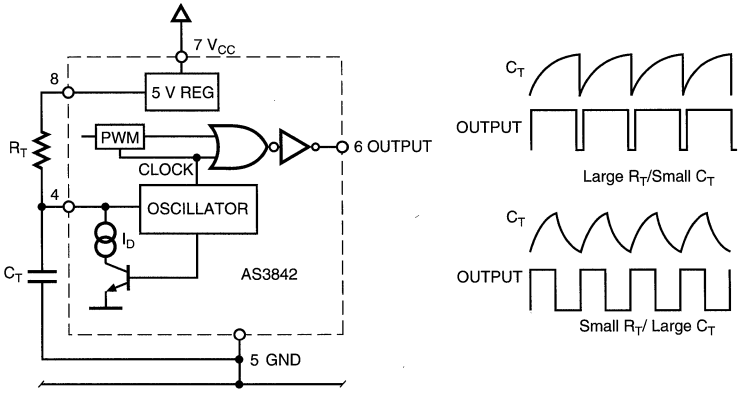


Figure 15. Oscillator Set-up and Waveforms

$$R_T = \frac{V_{REG}}{I_D} \cdot \frac{(K_L)^{\frac{1}{D}} - (K_H)^{\frac{1}{D}}}{(K_L)^{\frac{1-D}{D}} - (K_H)^{\frac{1-D}{D}}} \quad (2)$$

$$= 582 \cdot \frac{(0.736)^{\frac{1}{D}} - (0.432)^{\frac{1}{D}}}{(0.736)^{\frac{1-D}{D}} - (0.432)^{\frac{1-D}{D}}}$$

$$K_L = \frac{V_{REG} - V_L}{V_{REG}} \approx 0.736 \quad (3)$$

$$K_H = \frac{V_{REG} - V_H}{V_H} \approx 0.432 \quad (4)$$

where f_{osc} is the oscillator frequency, D is the maximum duty ratio, V_H is the oscillator's upper trip point, V_L is the lower trip point, V_R is the Reference voltage, I_D is the discharge current.

Table 1 lists some common values of R_T and the corresponding maximum duty ratio. To select the timing components; first, use Table 1 or equation (2) to determine the value of R_T that will yield the desired maximum duty ratio. Then, use equation (1) to calculate the value of C_T. For example, for a switching frequency of 250 kHz and a maximum duty ratio of 50%, the value of R_T, from Table 1, is 683 . Applying this value to equation (1) and solving for C_T gives a value of 4700 pF. In practice, some fine tuning of the initial values may be necessary during design. However, due to the advanced design of the AS3842 oscillator, once the final values are determined, they will yield repeatable results, thus eliminating the need for additional trimming of the timing components during manufacturing.

1.3.2 Oscillator enhancements

The AS3842 oscillator is trimmed to provide guaranteed duty ratio clamping. This means that the discharge current (I_D) is trimmed to a value that compensates for all of the tolerances within the device (such as the tolerances of V_{REG}, propagation delays, the oscillator trip points, etc.) which have an effect on the frequency and maximum duty ratio. For example, if the combined tolerances of a particular device are 0.5% above nominal, then I_D is trimmed to 0.5% above nominal. This method of trimming virtually eliminates the need to trim external oscillator components during power supply manufactur-

Table 1. R_T vs Maximum Duty Ratio

R_T (Ω)	Dmax
470	22%
560	37%
683	50%
750	54%
820	58%
910	63%
1,000	66%
1,200	72%
1,500	77%
1,800	81%
2,200	85%
2,700	88%
3,300	90%
3,900	91%
4,700	93%
5,600	94%
6,800	95%
8,200	96%
10,000	97%
18,000	98%

ing. Standard 3842 devices specify or trim only for a specific value of discharge current. This makes precise and repeatable duty ratio clamping virtually impossible due to other IC tolerances. The AS3844/5 provides true 50% duty ratio clamping by virtue of excluding from its flip-flop scheme, the normal output blanking associated with the discharge of C_T. Standard 3844/5 devices include the output blanking associated with the discharge of C_T, resulting in somewhat less than a 50% duty ratio.

1.3.3 Synchronization

The advanced design of the AS3842 oscillator simplifies synchronizing the frequency of two or more devices to each other or to an external clock. The R_T/C_T doubles as a synchronization input which can easily be driven from any open collector logic output. Figure 16 shows some simple circuits for implementing synchronization.

1.4 Error amplifier (COMP)

The AS3842 error amplifier is a wide bandwidth, internally compensated operational amplifier which provides a high DC open loop gain (90 dB). The input to the amplifier is a PNP differential pair. The non-inverting (+) input is internally connected to the 2.5 V reference, and the inverting (–) input is available at pin 2 (V_{FB}). The output of the error amplifier consists of an active pull-down and a 0.8 mA current source pull-up as shown in Figure 17. This type of output stage allows easy implementation of soft start, latched shutdown and reduced current sense clamp functions. It also permits wire "OR-ing" of the error amplifier outputs of several 3842s, or complete bypass of the error amplifier when its output is forced to remain in its "pull-up" condition.

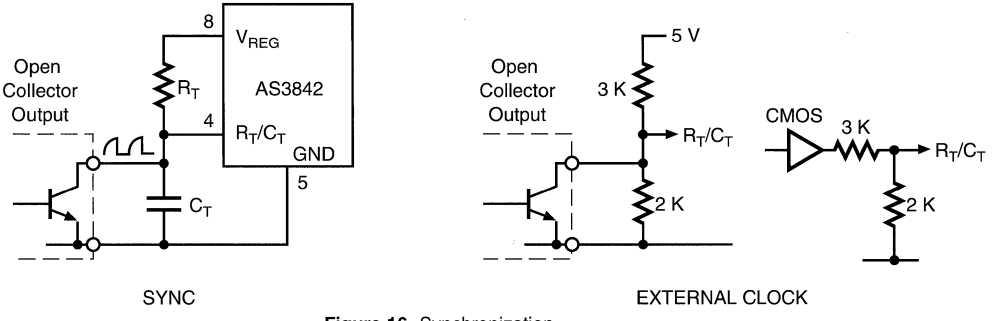


Figure 16. Synchronization

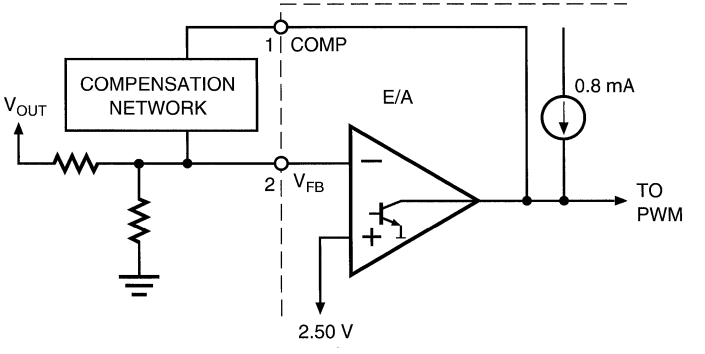


Figure 17. Error Amplifier Compensation

In most typical power supply designs, the converter's output voltage is divided down and monitored at the error amplifier's inverting input, V_{FB}. A simple resistor divider network is used and is scaled such that the voltage at V_{FB} is 2.5 V when the converter's output is at the desired voltage. The voltage at V_{FB} is then compared to the internal 2.5 V reference and any slight difference is amplified by the high gain of the error amplifier. The resulting error amplifier output is level shifted by two diode drops and is then divided by three to provide a 0 to 1 V reference (V_E) to one input of the current sense comparator. The level shifting reduces the input voltage range of the current sense input and prevents the output from going high when the error amplifier output is forced to its low state. An internal clamp limits V_E to 1.0 V. The purpose of the clamp is discussed in Section 1.5.

1.4.1 Loop compensation

Loop compensation of a power supply is necessary to ensure stability and provide good line/load regulation and dynamic response. It is normally provided by a compensation network connected between the error amplifier's output (COMP) and inverting input as shown in Figure 17. The type of network used depends on the converter topology and in particular, the characteristics of the major functional blocks within the supply - i.e. the error amplifier, the modulator/switching circuit, and the output filter. In general, the network is designed such that the converter's overall gain/phase response approaches that of a single pole with a –20 dB/decade rolloff, crossing unity gain at the highest possible frequency (up to $f_{SW}/4$) for good dynamic response, with adequate phase margin (> 45°) to ensure stability.

Figure 18 shows the Gain/Phase response of the error amplifier. The unity gain crossing is at 1.2 MHz with approximately 57° C of phase margin. This information is useful in determining the configuration and characteristics required for the compensation network.

One of the simplest types of compensation networks is shown in Figure 19. An RC network provides a single pole which is normally set to compensate for the zero introduced by the the output capacitor's ESR. The frequency of the pole (f_P) is determined by the formula;

$$f_P = \frac{1}{2\pi R_f C_f} \qquad (5)$$

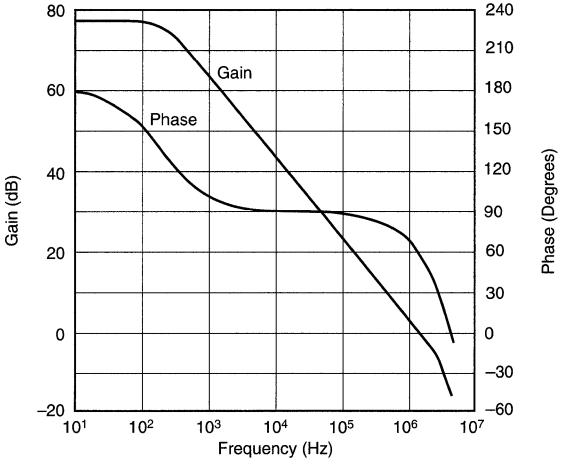


Figure 18. Gain/Phase Response of the AS3842

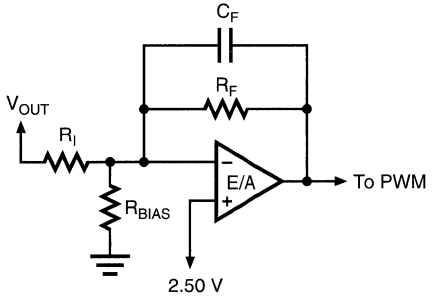


Figure 19. A Typical Compensation Network

Resistors R_1 and R_F set the low frequency gain and should be chosen to provide the highest possible gain, without exceeding the unity gain crossing frequency limit of f_{SW} /4. R_{BIAS}, in conjunction with R_1, sets the converter's output voltage; but has no effect on the loop gain/phase response.

There are a few converter design considerations associated with the error amplifier. First, the values of the divider network (R_1 and R_{BIAS}) should be kept low in order to minimize errors caused by the error amplifier's input bias current. An output voltage error equal to the product of the input bias current and the equivalent divider resistance, can be quite significant with divider values greater than 5 k . Low divider resistor values also help to improve the noise immunity of the sensitive V_{FB} input.

The second consideration is that the error amplifier will typically source only 0.8 mA; thus, the value of feedback resistance (R_F) should be no lower than 5 kΩ in order to maintain the error amplifier's full output range. In practice, however, the feedback resistance required is usually much greater than 5 kΩ, hence this limitation is normally not a problem.

Some power supply topologies may require a more elaborate compensation network. For example, flyback and boost converters operating with continuous current have transfer functions that include a right half plane (RHP) zero. These types of systems require an additional pole element within the compensation network. A detailed discussion of loop compensation, however, is beyond the scope of this application note.

1.5 I_{SENSE} current comparator/PWM latch

The current sense comparator (sometimes called the PWM comparator) and accompanying latch circuitry make up the pulse width modulator (PWM). It provides pulse-by-pulse current sensing/limiting and generates a variable duty ratio pulse train which controls the output voltage of the power supply. Included is a high speed comparator followed by ECL type logic circuitry which has very low propagation delays and switching noise. This is essential for high frequency power supply designs. The comparator has been designed to provide guaranteed performance with the current sense input below ground. The PWM latch ensures that only one pulse is allowed at the output for each oscillator period.

The inverting input to the current sense comparator is internally connected to the level shifted output of the error amplifier (V_E) as discused in the previous section. The non-inverting input is the I_{SENSE} input (pin 3). It monitors the switched inductor current of the converter.

Figure 20 shows the current sense/PWM circuitry of the AS3842, and associated waveforms. The output is set high by an internal clock pulse and remains high until one of two conditions occur; 1) the oscillator times out (Section 1.3)or 2) the PWM latch is set by the current sense comparator. During the time when the output is high, the converter's switching device is turned on and current flows through resistor R_S. This produces a stepped ramp waveform at pin 3 as shown in Figure 20. The current will continue to ramp up until it reaches the level of V_E at the inverting input. At that point, the comparator's output goes high, setting the PWM latch and the output pulse is then terminated. Thus, V_E is a variable reference for the current sense comparator, and it controls the peak current sensed by R_S on a cycle-by-cycle basis. V_S varies in proportion to changes in the input voltage/current (inner control loop) while V_E varies in proportion to changes in the converters output voltage/current (outer control loop). The two control loops merge at the current sense comparator, producing a variable duty ratio pulse train that controls the output of the converter.

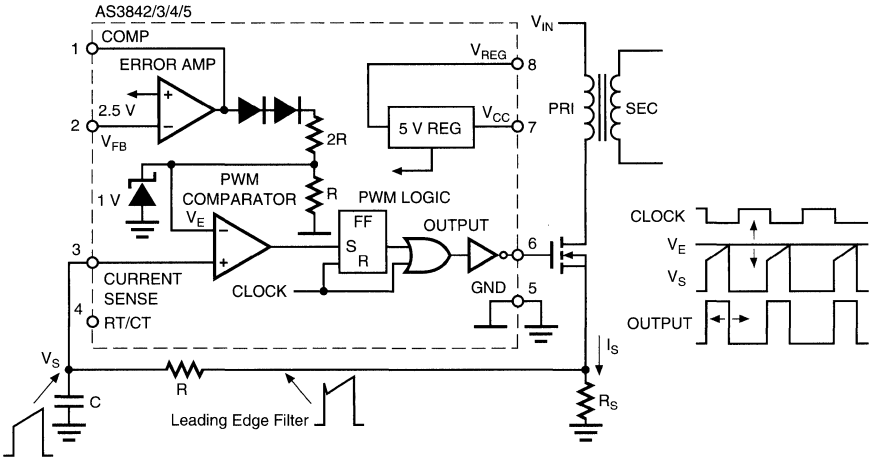


Figure 20. Current Sense/PWN Latch Circuit and Waveforms

The current sense comparator's inverting input is internally clamped to a level of 1.0 V to provide a current limit (or power limit for multiple output supplies) function. The value of R_S is selected to produce 1.0 V at the maximum allowed current. For example, if 1.5 A is the maximum allowed peak inductor current, then R_S is selected to equal 1 V/1.5 A = 0.66 Ω. In high power applications, power dissipation in the current sense resistor may become intolerable. In such a case, a current transformer can be used to step down the current seen by the sense resistor. See Figure 21.

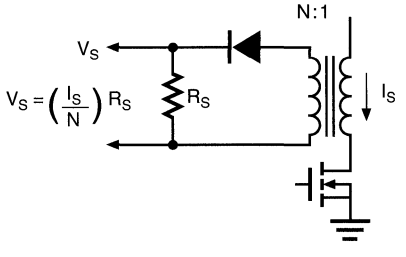


Figure 21. Optional Current Transformer

1.6 Output (OUT)

The output stage of the AS3842 is a high current totem-pole configuration that is well suited for directly driving power MOSFETs. It is capable of sourcing and sinking up to 1 A of peak current. Cross conduction losses in the output stage have been minimized resulting in lower power dissipation in the device. This is particularly important for high frequency operation. During under-voltage shutdown conditions, the output is active low. This eliminates the need for an external pulldown resistor.

1.7 Over-temperature shutdown

The AS3842 has a built-in over-temperature shutdown which will limit the die temperature to 130° C typically. When the over-temperature condition is reached, the oscillator is disabled. All other circuit blocks remain operational. Therefore, when the oscillator stops running, output pulses terminate without losing control of the supply or losing any peripheral functions that may be running off the 5 V regulator. The output may go high during the final cycle, but the PWM

latch is still fully operative, and the normal termination of this cycle by the current sense comparator will latch the output low until the over-temperature condition is rectified. Cycling the power will reset the over-temperature disable mechanism, or the chip will re-start after cooling through a nominal hysteresis band.

Section 2 – Design Considerations

2.1 Leading edge filter

The current sensed by R_S contains a leading edge spike as shown in Figure 20. This spike is caused by parasitic elements within the circuit including the interwinding capacitance of the power transformer and the recovery characteristics of the rectifier diode(s). The spike, if not properly filtered, can cause stability problems by prematurely terminating the output pulse.

A simple RC filter is used to suppress the spike. The time constant should be chosen such that it approximately equals the duration of the spike. A good choice for R_1 is 1 kΩ, as this value is optimum for the filter and at the same time, it simplifies the determination of R_{SLOPE} (Section 2.2). If the duration of the spike is, for example, 100 ns, then C is determined by:

$$C = \frac{\text{Time Constant}}{1\ \text{k}\Omega} \qquad (6)$$

$$= \frac{100\ \text{ns}}{1\ \text{k}\Omega}$$

$$= 100\ \text{pF}$$

2.2 Slope compensation

Current-mode controlled converters can experience instabilities or subharmonic oscillations when operated at duty ratios greater than 50%. Two different phenomena can occur as shown

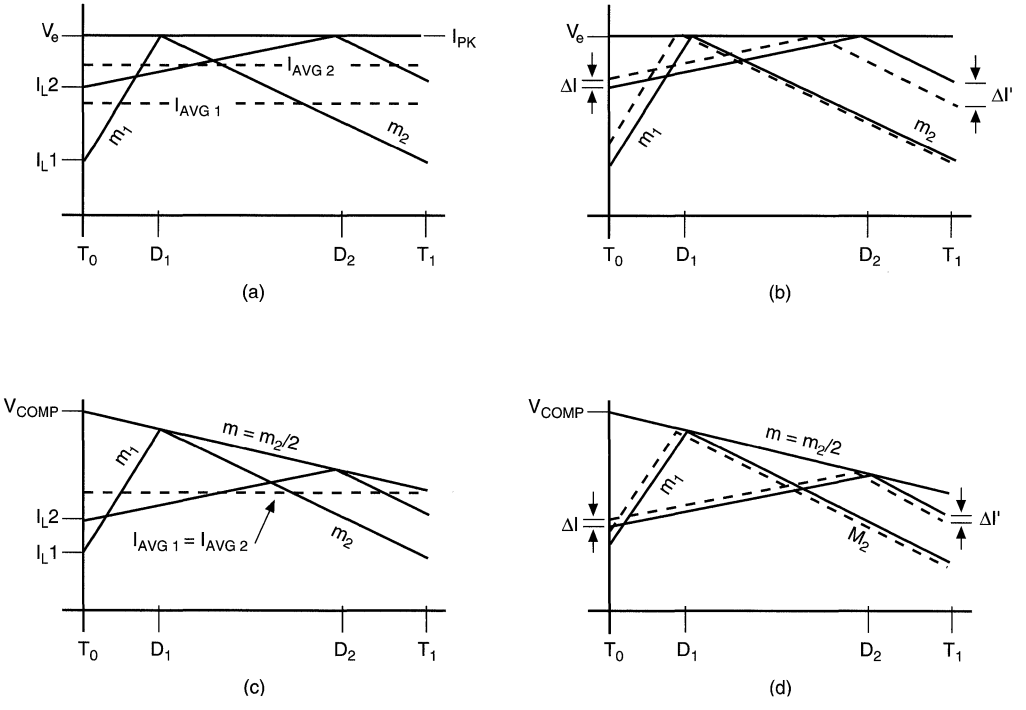


Figure 22. Slope Compensation

graphically in Figure 22.

First, current-mode controllers detect and control the peak inductor current, where as the converter's output corresponds to the average inductor current. Figure 22(a) clearly shows that the average inductor current (I_1 & I_2) changes as the duty ratio (D_1 & D_2) changes. Note that for a fixed control voltage, the peak current is the same for any duty ratio. The difference between the peak and average currents represents an error which causes the converter to deviate from true current-mode control.

Second, Figure 22(b) depicts how a small perturbation of the inductor current (I) can result in an unstable condition. For duty ratios less than 50 %, the disturbance will quickly converge to a steady state condition. For duty ratios greater than 50 %, I progressively increases on each cycle, causing an unstable condition.

Both of these problems are corrected simultaneously by injecting a compensating ramp into either the control voltage (V_E) as shown in Figure 22(c) & (d), or to the current sense waveform at pin 3. Since V_E is not directly accessible, and, a positive ramp waveform is readily available from the oscillator at pin 4, it is more practical to add the slope compensation to the current waveform. This can be implemented quite simply with the addition of a single resistor, R_{SLOPE}, between pin 4 and pin 3 as shown in Figure 23(a). R_{SLOPE}, in conjunction with the leading edge filter resistor, R_1 (Section 2.1), forms a divider network which determines the amount of slope added to the waveform. The amount of slope added to the current waveform is inversely proportional to the value of R_{SLOPE}. It has been determined that the amount of slope (m) required is equal to or greater than 1/2 the downslope (m_2) of the inductor current. Mathematically stated:

$$m \geq \frac{m_2}{2} \qquad (7)$$

In some cases the required value of R_{SLOPE} may be low enough to affect the oscillator circuit and thus cause the frequency to shift. An emitter follower circuit can be used as a buffer for R_{SLOPE} as depicted in Figure 23(b).

Slope compensation can also be used to improve noise immunity in current mode converters operating at less than 50% duty ratio. Power supplies

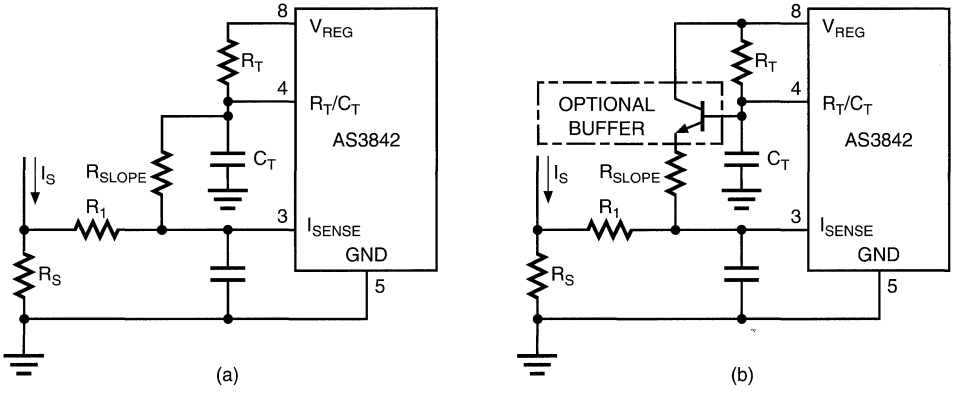


Figure 23. Slope Compensation

operating under very light load can experience instabilities caused by the low amplitude of the current sense ramp waveform. In such a case, any noise on the waveform can be sufficient to trip the comparator resulting in random and premature pulse termination. The addition of a small amount of artificial ramp (slope compensation) can eliminate such problems without drastically affecting the overall performance of the system.

2.3 Circuit layout and other considerations

The eletronic noise generated by any switch-mode power supply can cause severe stability problems if the circuit is not layed-out (wired) properly. A few simple layout practices will help to minimize noise problems.

When building prototype breadboards, never use plug-in protoboards or wire wrap construction. For best results, do all breadboarding on double sided PCB using ground plane techniques. Keep all traces and lead lengths to a minimum. Avoid large loops and keep the area enclosed within any loops to a minimum. Use common point grounding techniques and separate the power ground traces from the signal ground traces. Locate the control IC and circuitry away from switching devices and magnetics. Also, the timing capacitor's ground connection must be right at pin 5 as shown in Figure 15. These grounding and wiring techniques are very important because the resistance and inductance of the traces are significant enough to generate noise glitches which can disrupt the normal operation of the IC.

Also, to provide a low impedance path for high frequency noise, V_{CC} and V_{REF} should be decoupled to IC ground with 0.1 µF capacitors. Additional decoupling in other sensitive areas may also be necessary. It is very important to locate the decoupling capacitors as close as possible to the circuit being decoupled.

AS2214

Primary Side PWM Controller

Proposed Specification

Features

- Low Startup Current
- Bulk and AC sensing
- Soft Start
- Single-start or auto-restart modes
- Oscillator trimmed for precision duty cycle clamp
- Standard temperature range extended to 105°C
- Remote on / off control
- Buffered Ramp for slope compensation
- Standard current mode control

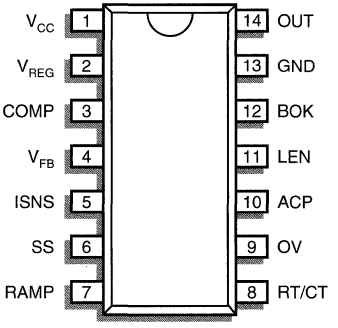
Description

The AS2214 is a full featured, pulse width modulation controller. Based on an improved AS3842, the AS2214 provides additional features that reduce component count and improve specifications in a wide range of power supply designs. The added functionality includes AC power and bulk voltage sensing, over-voltage input, as well as the ability to latch off or bounce through different fault conditions.

The PWM function is controlled by the current sense comparator for normal current mode control and a second comparator for voltage mode soft start. A buffered RAMP signal is available for slope compensation without loading the oscillator. The output stage is a high current totem pole output that sees only 140ns delay from the PWM comparator.

The AS2214 requires less than 10µA of startup current. The undervoltage lockout (UVLO) thresholds are nominally 15V for turn on and 8 V for turn off. A precision 2.5 V bandgap reference serves as an input for the error amplifier. The oscillator discharge current is trimmed to provide guaranteed duty cycle clamping.

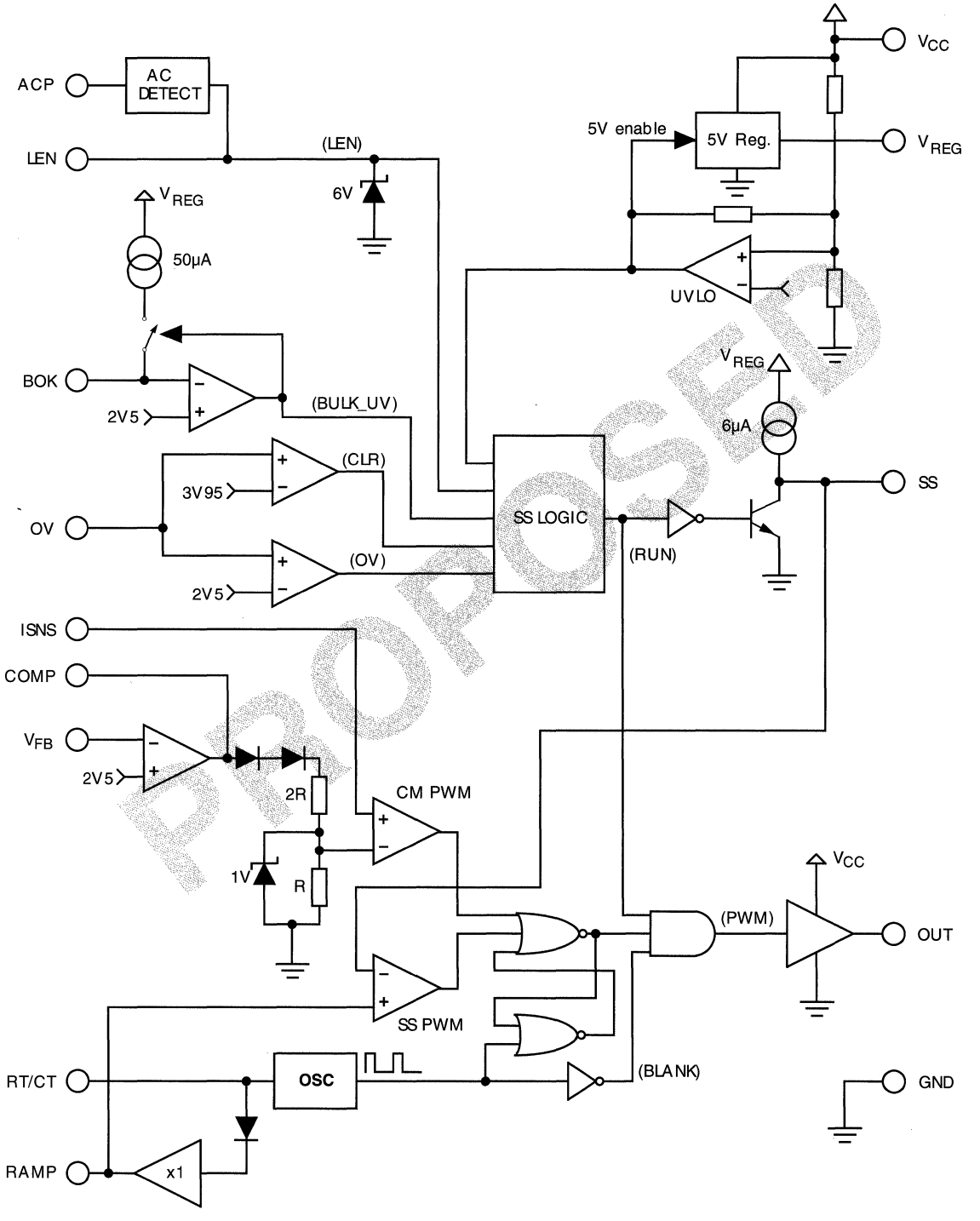
Pin Configuration — Top view



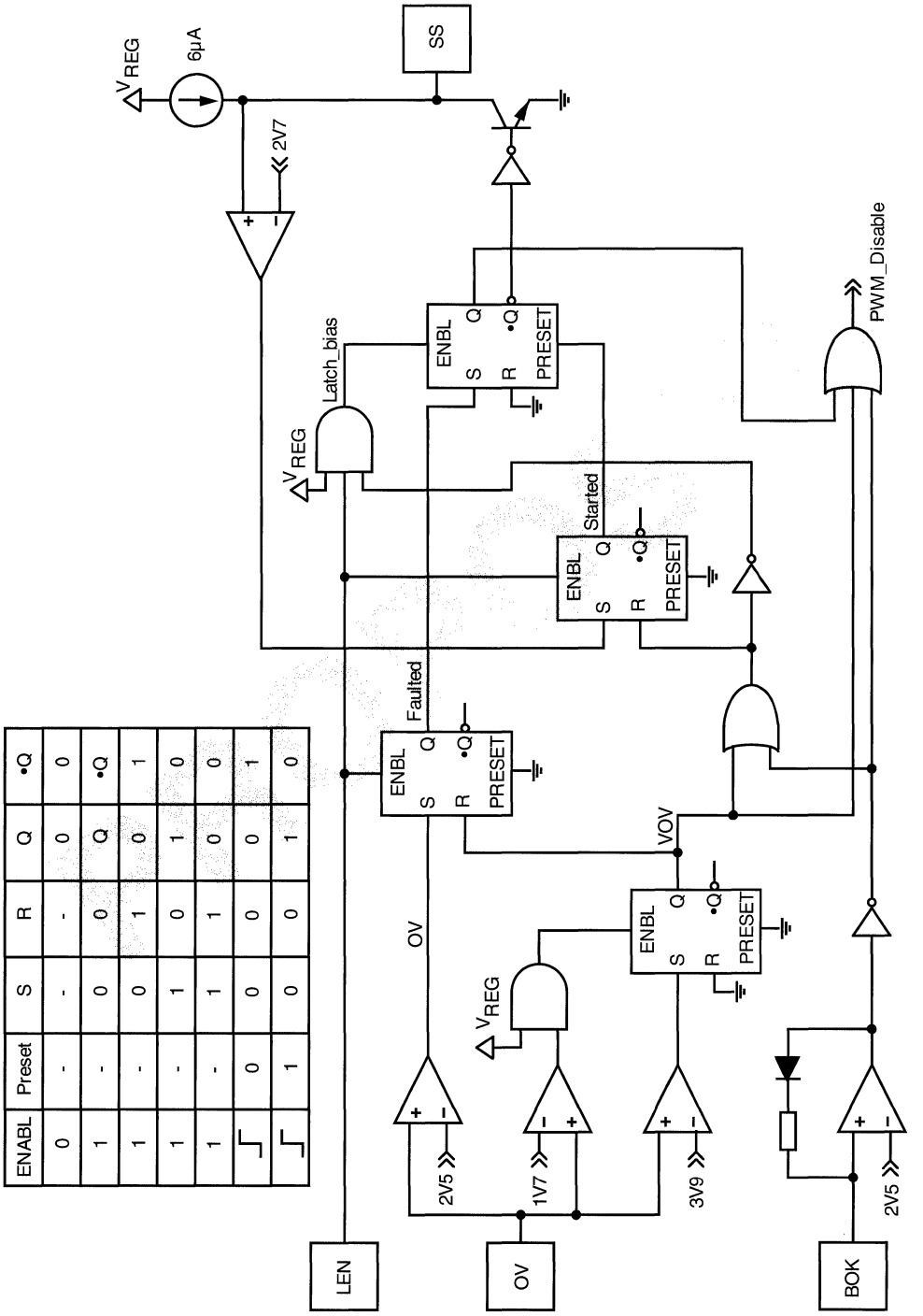
Ordering Information

Product	Package	Temperature Range	Order Code
AS2214	14-Pin Plastic DIP	0 to 105° C	2214-14*N-F-000

Functional Block Diagram



AS2214 Soft Start Logic



ENABL	Preset	S	R	Q	•Q
0	-	-	-	0	0
1	-	0	0	Q	•Q
1	-	0	1	0	1
1	-	1	0	1	0
1	-	1	1	0	0
⌐	0	0	0	0	1
⌐	1	0	0	1	0

Pin Function Description

Pin Number	Function	Description
1	V_{CC}	Positive supply voltage for the IC.
2	V_{REG}	Output of 5V series regulator.
3	COMP	This pin is the error amplifier output. Typically used to provide loop compensation to maintain V_{FB} at 2.5 V.
4	V_{FB}	Inverting input of the error amplifier. The non-inverting input is a trimmed 2.5 V bandgap reference.
5	ISNS	A voltage proportional to inductor current is connected to this pin. The PWM uses this information to terminate the gate drive of the output.
6	SS	This pin provides a 6µA current source to linearly charge an external capacitor. This pin is compared to the RAMP pin in the soft start comparator, terminating output pulses when RAMP goes above the SS voltage.
7	RAMP	This pin is a level-shifted and buffered oscillator signal used to provide slope compensation to the current sense signal. The pin also serves as the non-inverting input of the soft-start comparator.
8	RT/CT	Oscillator frequency and maximum duty cycle are set by connecting a resistor (R_T) to VREG and a capacitor (C_T) to ground.
9	OV	This pin latches SS low when pulled above 2.5 V. The latch can be reset by pulling OV above 4 V then back to ground.
10	ACP	This pin detects the presence of AC signal and drives LEN high.
11	LEN	This pin must be high to enable starting. The pin can also clear all latches by going low then high.
12	BOK	This pin monitors the bulk voltage through a resistor divider and, when BOK exceeds 2.5 V, provides a 50µA current source for hysteresis. When BOK drops below 2.5V, SS is pulled low and the hysteresis current is turned off. Auto-restart after a brown-out is possible.
13	GND	Circuit common ground.
14	OUT	This totem pole output is designed to directly drive a power MOSFET switch capable of sourcing and sinking peak currents up to 1 A.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Regulator Current	I_{REG}	200	mA
Output Current	I_{OUT}	1	A
Supply Voltage	V_{CC}	30	V
Output Voltage	V_{OUT}	30	V
Continuous Power Dissipation at 25° C	P_D	500	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	10 - 15	V
Oscillator	F_{OSC}	50 - 250	kHz

Typical Thermal Resistance

Package	θ_{JA}	θ_{JC}	Typical Derating
14L PDIP	85° C/W	40° C/W	11.7 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 15 V; BOK = 3 V; OV = 0V; R_T = 680 ; C $_T$ = 10 nF. To override UVLO, V_{CC} should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error Amplifier						
Input Voltage	V_{FB}	T_J = 25°C	2.465	2.500	2.535	V
Input Bias Current	I_{BIAS}			-0.1	-1	µA
Voltage Gain	A_{VOL}	2 V_{COMP} 4 V	65	90		dB
Transconductance	G_m			1		mA/mV
Unity Gain Bandwidth	GBW		0.8	1.2		MHz
Power Supply Rejection Ratio	PSRR	12 V_{CC} 25 V	60	70		dB
Output Sink Current	I_{COMPL}	V_{FB} = 2.7 V; V_{COMP} = 1.1 V	2	6		mA
Output Source Current	I_{COMPH}	V_{FB} = 2.3 V; V_{COMP} = 5 V	0.5	1.0		mA
Output Swing High	I_{COMPH}	V_{FB} = 2.3 V; R_L = 15 Ω to GND	5	5.5		V
Output Swing Low	I_{COMPL}	V_{FB} = 2.7 V; R_L = 15 Ω to V_{REG}		0.7	1.1	V

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 15 V; BOK = 3 V; OV = 0V; R_T = 680 ; C $_T$ = 10 nF. To override UVLO, V_{CC} should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5 V Regulator						
Output Voltage	V_{REG}	I_{REG} = 1 mA, T_J= 25° C	4.90	5.00	5.10	V
Line Regulation	PSRR	12 V_{CC} 25 V		5	15	mV
Load Regulation		1 I_{REG} 20mA		5	15	mV
Temperature Stability	TC_{REG}			0.2	0.4	mV/°C
Total Output Variation		Line, Load,Temperature	4.85		5.15	V
Long-Term Stability		Over 1,000 hrs at 25°C		5	25	mV
Output Noise Voltage	V_{NOISE}	10 f 100kHz, T $_J$ = 25°C		50		µV
Maximum Source Current	I_{MAX}	V_{REG} = 4.8 V	30	120	180	mA
Oscillator						
Initial Accuracy	F_{OSC}	T_J =25°C	108	120	132	kHz
Voltage Stability		12 V_{CC} 25 V		0.2	1	%
Temperature Stability	TC_F	T_{MIN} T_J T_{MAX}		5		%
Amplitude	V_{OSC}	VRT/CT peak-to-peak		1.55		V
Upper Trip Point	V_H			2.80		V
Lower Trip Point	V_L			1.25		V
Discharge Current	I_{DSC}		7.50	8.70	9.50	mA
Duty cycle Limit		R_T =680 Ω, C_T =10nF, T_J =25°C	46	50	55	%
Over-Temperature Shutdown	T_{OT}			140		°C
Soft Start Comparator						
SS Charge Current	I_{SS}	V_{SS} V_{RAMP}	-4	-6	-10	µA
SS Discharge Current	I_{Dsc} SS	V_{SS} = 1 V, V_{OV} > 2.5V	2	8		mA
SS Lower Clamp	$V_{SS\ Low}$			0.6		V
RAMP High Level	V_{RAMPH}	T_J =25°C		2.15		V
RAMP Low Level	V_{RAMPL}	T_J =25°C		0.6		V
RAMP Levels TC		Note: RAMP wavefrom is the same as the RT/CT wavefrom, but level shifted down one diode drop		-2		mV/°C
RAMP Sink Current	I_{RAMPL}	T_J =25°C	−0.1	−0.2		mA
RAMP Source Current	I_{RAMPH}	T_J =25°C	1			mA
Propagation Delay to Output	t_{PB}			140	300	ns

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 15 V; BOK = 3 V; OV = 0V; R_T = 680 ; C $_T$ = 10 nF. To override UVLO, V_{CC} should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Housekeeping						
BOK UV Threshold	V_{BOK} UV	V_{REG} = 5 V	2.500	2.537	2.575	V
BOK UV Hysteresis Current	$I_{HYST\ BOK}$	V_{BOK} = 2.6 V	42	50	58	µA
BOK Input Bias Current	$I_{OFF\ BOK}$	V_{BOK} = 2.4 V		0.1	1.0	µA
OV Threshold	V_{OV}		2.20	2.50	2.80	V
OV Clear Threshold	V_{OVH}		3.60	3.95	4.50	V
OV Reset Threshold	V_{OVL}		1.10	1.75	2.20	V
OV Bias Current	$I_{BIAS\ OV}$	V_{REG} = 5 V, V_{OV} OV Threshold	-1	-0.2	1	µA
ACP Voltage	V_{ACP}	I_{ACP} = 10 µA		1.3		V
ACP Voltage	V_{ACP}	I_{ACP} = -10 µA		-1.2		V
LEN Charge Current	I_{LEN}	I_{ACP} = 10 µA; V_{LEN} = 0 V	-30	-45	-65	µA
LEN Charge Current	I_{LEN}	I_{ACP} = -10 µA; V_{LEN} = 0 V	-30	-50	-65	µA
Minimum Voltage for LEN Functionality	$V_{LEN\ MIN}$		4.5			V
LEN Logic Reset Voltage	V_{LEN}		1.7	2.5	3.0	V
LEN Clamp	V_{LEN}	I_{ACP} = 5 µA	5.2	5.9	6.6	V
LEN Bias Current	$I_{BIAS\ LEN}$	V_{LEN} = 5 V, I_{ACP} = 0 µA		5		µA
Current Sense Comparator						
Transfer Gain	AV_{ISNS}	-0.2 V $_{ISNS}$ 0.8 V	2.85	3.00	3.15	V/V
I_{SNS} Level Shift	V_{LS}	V_{ISNS} = 0 V		1.50		V
Maximum Input Signal		V_{COMP} =+5 V	1.00	1.08	1.20	V
Power Supply Rejection Ratio	PSRR			70		dB
Input Bias Current	I_{BIAS}			-1	-10	µA
Propagation Delay to Output	t_{PB}			140	300	ns
Under Voltage Lockout						
Startup Threshold	V_{CC} (ON)		13.8	15.0	16.8	V
Minimum Operating Voltage after Trun-on	V_{CC} (OFF)		7.3	8.0	8.5	AV
Startup Current	I_{CC}	V_{CC} = 13 V; V_{ACP} = V_{LEN} = 0 V		2	10	µA
Startup Current	I_{CC}	V_{CC} = 13 V; I_{ACP} = 5 µA		105	150	µA
Operating Supply Current	I_{CC}			12	20	mA
Output Impedance to GND in UVLO State	Z_{OUT}	V_{CC} = 6 V		22.0		kΩ

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 15 V; BOK = 3 V; OV = 0V; R_T = 680 ; C $_T$ = 10 nF. To override UVLO, V_{CC} should be raised above 18 V prior to test.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output						
Output Low Level	V_{OL}	I_{SINK} = 20 mA		0.1	0.4	V
Output Low Level	V_{OL}	I_{SINK} = 150 mA		1.5	2.2	V
Output High Level	V_{OH}	I_{SOURCE} = 20 mA	13	–13.5		V
Output High Level	V_{OH}	I_{SOURCE} = 150 mA	12	13		V
Rise Time	t_R	C_L = 1 nF		50	150	ns
Fall Time	t_F	C_L = 1 nF		50	150	ns
Maximum Duty Cycle	D_{MAX}		94	97	100	%
Minimum Duty Cycle	D_{MIN}		0			%

ASTEC SEMICONDUCTOR

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AS23xx

Secondary Side Housekeeping Circuit

Proposed Specification

Features

- Standard PC Power Good:
  - UV Detection on 4 rails
  - UV Detection of AC/Bulk supply
  - OV Detection on 4 rails
  - Open collector PG out
- Pogrammable Fault output:
  - OV
  - OV plus UV
  - OV plus UV after startup delay
- OV Crow Bar Driver
- Digital ON/OFF input
- 2.5V Voltage Reference
- Operates from 5V or 12V rail
- Choice of:
  - ± 12V, ± 5V detection (AS2350)
  - ± 12V, + 5V, +3.3V detection (AS2333)

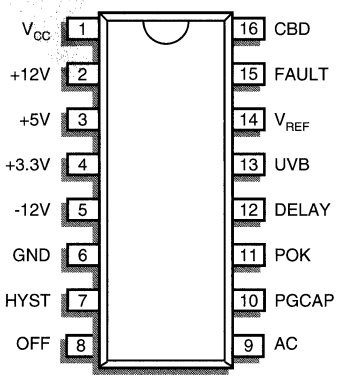
Description

The AS23xx is a housekeeping circuit for monitoring the outputs of power supplies. It directly senses all the output rails without the need for external dividers and detects undervoltage and overvoltage. It also provides an additional undervoltage comparator which may be configured with any arbitrary hysteresis to sense a divided down representation of the AC bulk voltage. The housekeeping section provides all the features necessary to allow external caps to set the common timing features of PC type power supplies. In addition, negative rails may be sensed without the necessity of a V_{EE} connection, and negative sensing may be disabled without affecting operation of the positive sense section. The 2.5 V series reference is available and can source up to 5 mA. This IC is available in 16 lead packages.

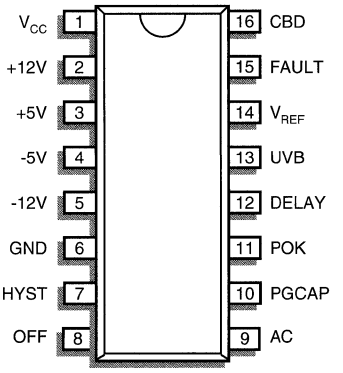
Ordering Information

Product	Package	Temperature Range	Order Code
AS2333	16-Pin Plastic DIP	0 to 105° C	2333-16*N-C-000
AS2350	16-Pin Plastic DIP	0 to 105° C	2350-16*N-C-000

Pin Configuration — Top view

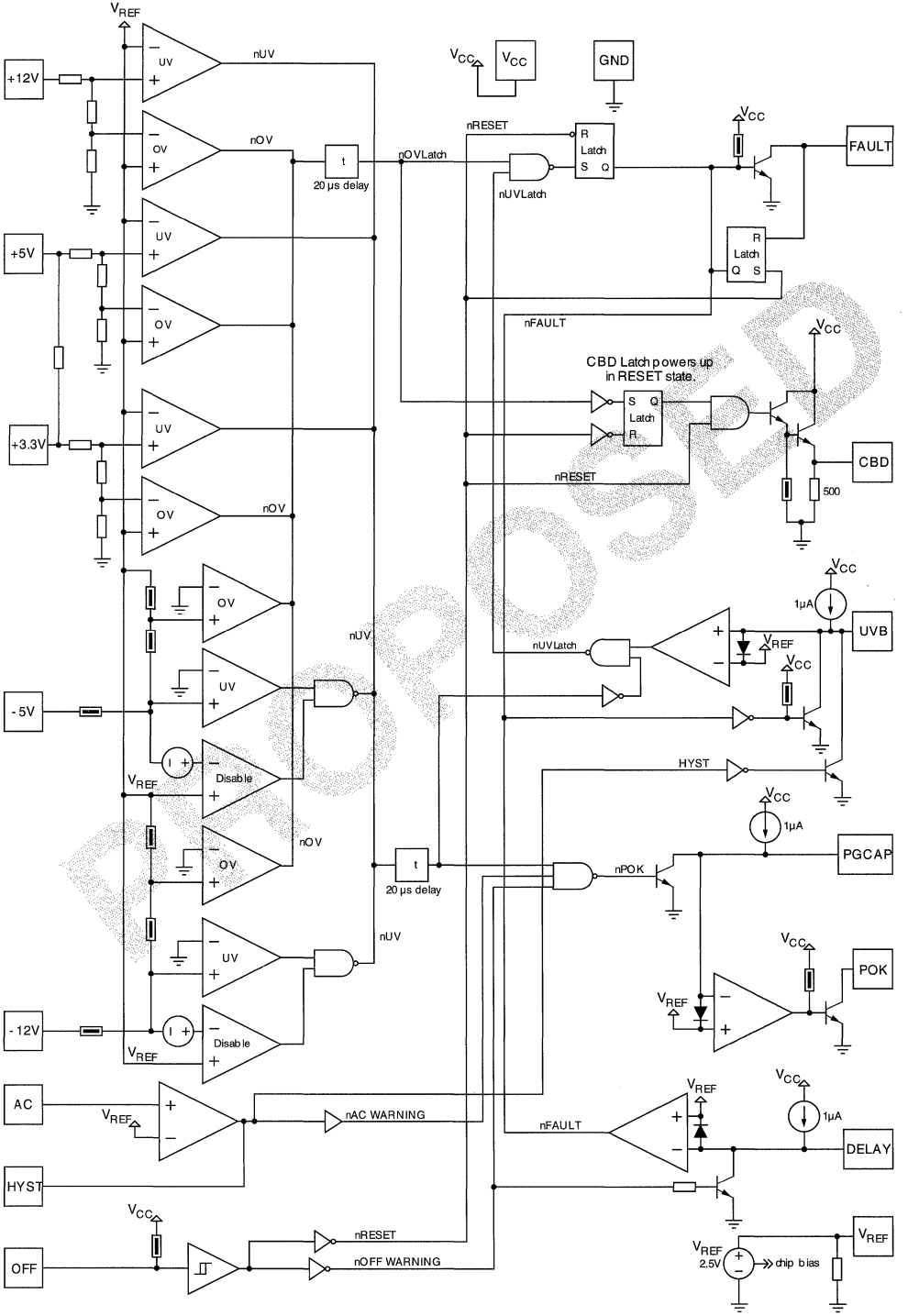


AS2333



AS2350

Functional Block Diagram



Pin Function Description

Pin Number	Function	Description
1	V_{CC}	Power input to the chip.
2	+12 V	Input for overvoltage and undervoltage for the +12 V rail.
3	+5 V	Input for overvoltage and undervoltage for the +5 V rail.
4	+3.3/–5 V	Input for overvoltage and undervoltage for the +3.3V rail or –5 V rail, depending on product option.
5	–12 V	Input for overvoltage and undervoltage for the –12 V rail. This function may disabled by tying this pin to a positive voltage above 2.4 V.
6	GND	Signal ground and silicon substrate.
7	HYST	Open collector output of the AC undervoltage comparator. A resistor between this pin and AC will provide hysteresis to the AC undervoltage sensing.
8	OFF	Pulling this pin low will reset the FAULT latch and discharge the start-up timing capacitors, UVB and PG CAP, allowing normal start-up for the system. Pulling this pin high will send the FAULT signal high, prompting a system shutdown.
9	AC	Non-inverting input to the AC undervoltage sensing comparator. If the AC pin is less than 2.5 V, POK goes low and UVB cap discharges.
10	PG CAP	A cap to ground provides a delay between undervoltage sensing becoming good and the POK output going high. Cap discharges whenever an output or AC undervoltage is detected.
11	POK	Open collector output of the undervoltage sensing comparators. This pin goes low upon an undervoltage condition. Except for the delay set by the PG CAP, this pin always reflects the actual state of the undervoltage sensing.
12	DELAY	A cap to ground will delay the FAULT signal when the OFF pin is used to shut down the system. The POK will signal a power fail warning immediately, but the FAULT shutdown of the power supply will be delayed.
13	UVB	A cap to ground provides start-up blanking of the undervoltage sensing portion of the FAULT signal. This pin may also be grounded to prevent undervoltage conditions from triggering the FAULT signal. This pin discharges the cap whenever AC goes low or FAULT pin goes high.
14	V_{REF}	2.5 V Voltage reference. This is a series regulator type reference.
15	FAULT	Open collector output of the overvoltage and undervoltage comparators.
16	CBD	Optional crow bar drive output of the overvoltage faults only.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	20	V
Continuous Power Dissipation at 25° C	P_D	1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	5 - 12	V

Typical Thermal Resistance

Package	θ_{JA}	θ_{JC}	Typical Derating
16L PDIP	80° C/W	35° C/W	12.5 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; −12 V = −12 V; −5 V = −5 V; OFF = low.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bias						
Supply Current	I_{CC}	no faults		8	12	mA
Min. V_{CC} for operation	V_{CC} Min.	V_{REF} = 2.5 V, no faults			4.2	V
Undervoltage, Overvoltage +3.3 V						
+3.3 V Undervoltage	UV		2.87	2.95	3.03	V
+3.3 V Overvoltage	OV		3.76	3.86	3.96	V
+3.3 V Input Current	I_B	$V_{+3.3}$ =+3.3V, V_{+5} =+5.0V	-0.1	0	0.1	mA
+5 V						
+5 V Undervoltage	UV		4.40	4.50	4.60	V
+5 V Overvoltage	OV		5.74	5.89	6.04	V
+5 V Input Current	I_B	V_{+5} =+5.0V, $V_{+3.3}$ =+3.3V		1	2	mA
+12 V						
+12 V Undervoltage	UV		10.25	10.50	10.60	V
+12 V Overvoltage	OV		14.53	14.90	15.27	V
+12 V Input Current	I_B	V_{+12} =+12.0V		0.5	1	mA

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; –12 V = –12 V; –5 V = –5 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
–5 V						
–5 V Undervoltage	UV		–3.80	–4.00	–4.20	V
–5 V Overvoltage	OV		–6.00	–6.25	–6.55	V
–5 V Input Current	I_B	V_{-5} =-5.0V		–65	–110	µA
–5 V Disable Voltage	V_D	Minimum voltage to disable		2.3	2.4	V
–12 V						
–12 V Undervoltage	UV		–9.20	–9.55	–9.80	V
–12 V Overvoltage	OV		–14.55	–15.04	–15.60	V
–12 V Input Current	I_B	V_{-12} =-12.0V		–125	–220	µA
–12 V Disable Voltage	V_D	Minimum voltage to disable		2.0	2.2	V
AC/HYST						
AC Undervoltage	UV	T_J = 25° C	2.425	2.465	2.505	V
AC Undervoltage	UV	T_J = 0 - 105° C	2.375		2.505	V
AC Input Current	I_B			–0.5	–1	µA
HYST High State Leakage	I_L	V_{HYST} = 5 V; AC > 2.5 V		0.01	1	µA
HYST Output Current	I_{OL}	V_{HYST} = 0.3 V; AC < 2.5 V	1	3		mA
HYST Low Voltage	V_{OL}	I_{HYST} = 1 mA; AC < 2.5 V			0.3	V
Outputs						
POK High State Leakage	I_L	V_{POK} = 12 V; no faults		0.01	1	µA
POK Output Current	I_{OL}	V_{POK} = 0.4 V; V_{CC} = 7 V undervoltage condition	5	10		mA
FAULT High State Leakage	I_L	V_{FAULT} = 12 V; OFF = High		0.01	1	µA
FAULT Output Current	V_{OL}	V_{FAULT} = 0.4 V; no faults V_{CC} = 12 V V_{CC} = 5 V	 3 1.3	 10 4		 mA mA
CBD (Crow Bar Drive) Minimum Output Current	I_{OH}	overvoltage condition	–25	–35		mA
CBD Output High Voltage	V_{OH}	I_{CBD} = 0 mA; T = 25 ° C I_{CBD} = 0 mA; T = 105 ° C; overvoltage condition	2.1 1.4	2.4	2.7 3	V V
CBD Pulldown Resistance	R_{OUT}	I_{CBD} = 1 mA; no faults	300	500	1000	Ω

Electrical Characteristics (cont'd)

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105° C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. Unless otherwise specified, the conditions of test are V_{CC} = 12 V; +3.3 V = 3.3 V; +5 V = 5V; +12 V = 12 V; –12 V = –12 V; –5 V = –5 V.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage Reference						
Output Voltage	V_{REF}	I_{REF} = 0 mA, T_J = 25° C	2.488	2.500	2.525	V
Line Regulation	ΔV_{REF}	V_{CC} = 5 V to 15 V		10	15	mV
Load Regulation	ΔV_{REF}	I_{REF} = 0 V to –5 mA		10	15	mV
Temperature Deviation*	ΔV_{REF}	0 < T_J < 105° C		10	15	mV
Start-Up Functions						
UVB Pull-up Current Source	I_{OH}	V_{UVB} = 2.0 V; no faults	–0.4	–1	–1.9	µA
UVB Clamp	$V_{OH\ MAX}$	I_{UVB} = 10 µA; no faults	2.9	3.1	3.3	V
UVB Discharge Current (AC shutdown)	I_{UVB}	V_{UVB} = 2.0 V; FAULT = low; AC < 2.5 V	3	8		mA
UVB Discharge Current (FAULT shutdown)	I_{OL}	V_{UVB} = 2.0 V; FAULT = high; AC > 2.5 V	2.5	10		mA
UVB Low Output Voltage	V_{OL}	I_{UVB} = 100 µA; FAULT = low; AC < 2.5 V			0.2	V
PG CAP Pull-up Current Source	I_{OH}	V_{PGCAP} = 2.0 V; no faults	–0.5	–1	–1.4	µA
PG CAP Clamp	$V_{OH\ MAX}$	I_{PGCAP} = 10 µA; no faults; AC > 2.5 V	2.9	3.1	3.3	V
PG CAP Discharge Current	I_{OL}	V_{PGCAP} = 2.0 V; undervoltage condition	2	6		mA
PG CAP Low Output Voltage	V_{OL}	I_{PGCAP} = 100µA; undervoltage condition			0.2	V
OFF Input High Voltage	V_{IH}		2.0			V
OFF Input Low Voltage	V_{IL}				0.8	V
OFF Input High Clamp		I_{OFF} = 100µA		0.7		V
OFF Pull-up to V_{CC}	R	V_{OFF} = 0 V	25	50	100	kΩ
DELAY Pull-up Current Source	I_{OH}	V_{DELAY} = 0 V; OFF = high	–0.5	–1	–2.0	µA
DELAY Clamp	$V_{OH\ MAX}$	I_{DELAY} = 10 µA; OFF = high	2.9	3.1	3.3	V
DELAY Discharge Current	I_{OL}	V_{DELAY} = 2.0 V; OFF = low	2.5	10		mA
DELAY Low Output Voltage	V_{OL}	I_{DELAY} = 100µA; OFF = low			0.2	V

*Temperature deviation is defined as the maximum deviation of the reference over the given temperature range and does not imply an incremental deviation at any given temperature.

Typical Performance Curves

Not Available at Time of Publishing

Theory of Operation

The AS23xx performs housekeeping functions for power supplies, especially switching power supplies for personal computers. The chip resides on the secondary side of the power supply (PSU), and it performs three primary functions:

1) monitors the output voltages and reports faults
2) sequences the start-up of the PSU
3) sequences the shutdown of the PSU

Section 1 - Output Voltages and Faults

1.0 Output Voltage Monitoring

The AS23xx monitors the standard voltage outputs for PC type power supplies. It has inputs for +12 V, +5 V, +3.3 V, -5 V and -12 V. These inputs are tied directly to the outputs of the PSU, and therefore do not require external dividers to set the error thresholds. These pins are monitored for both overvoltage (OV) and undervoltage (UV) conditions. The spec's for these thresholds are listed in the data sheet.

1.1 Overvoltage Faults: FAULT and CBD

An overvoltage condition in a power supply is considered to be a catastrophic and dangerous condition which must result in a safe, complete and near-instantaneous shutdown of the system. Overvoltages most often result from a break in the system feedback and control circuitry or from a short between outputs. When the AS23xx detects an overvoltage, the fault is latched internally, and the FAULT and CBD pins go high. The FAULT pin is an open collector NPN output which is intended to drive an optocoupler LED for feedback to the primary side controller of the PSU. The CBD pin is an NPN Darlington output which is intended to drive an SCR crowbar circuit which will short circuit the outputs of the PSU. Usually, just one or the other output is used depending on the PSU's cost and system definition. Both methods are intended to protect the customer's system, and the customer, as the first priority.

1.2 Undervoltage Faults: POK and FAULT

An undervoltage condition is sometimes not considered a catastrophic or dangerous condition, but always one which the customer should be warned about. The POK signal is a logic line to the customer's system that is specified in most PC type power supply systems. The AS23xx will pull the POK signal low when a UV fault is detected. A UV fault may or may not require the system to shut down, so an undervoltage blanking pin is provided (UVB). Grounding this pin will prevent UV faults from propogating to the FAULT pin. CBD does not react to UV faults.

1.3 Input Undervoltage: AC and HYST

In addition, there is a special undervoltage detection input for sensing the input voltage to the power supply, designated as the AC pin. This pin will cause the POK pin to go low if there is insufficient voltage to run the PSU outputs. Since power supplies must maintain high voltage isolation between the primary and secondary sides of the system, the AC pin is usually tied to a divided down and filtered representation of the secondary side switching waveform. Hysteresis for this function, to provide immunity from line ripple, is configured by the PSU designer and is implemented with the HYST pin, which is an open collector output of the AC comparator.

Section 2 - PSU Start-up Sequences

2.0 System Start-up Sequence

When the power supply starts up, the AS23xx must not erroneously report a FAULT. In addition, most PC type power supply specifications

require a specific timing sequence for the POK signal. Some PSU systems also require an isolated, low voltage, low power remote turn-on switch, rather than a large line cord switch.

2.1 VREF Enable of Chip Bias

Since the VCC of the AS23xx comes up in a finite amount of time, and since the VREF of the chip and the bias for the comparators are not within specification until approximately 4.2 V of VCC is available, the comparators for OV and UV and most other functions are disabled until VREF is within spec. This prevents the false detection of a FAULT due to an erroneous VREF. Similarly, if VREF is too heavily loaded and gets pulled low out of spec, these functions will also shut off.

2.2 Blanking UV's During Start-up: UVB

As the power supply outputs come up, the undervoltage FAULTs must be blanked to allow the supply to complete its start-up. Putting a capacitor to ground on the UVB pin will allow the PSU designer to set a specific period of time during which undervoltages will not propogate to the FAULT pin. The UVB pin provides a 1 µA current source to charge the cap, and once the UVB pin charges above 2.5 V, the undervoltage sensing is enabled. UVB does not blank undervoltages to the POK pin. The UVB pin is clamped one diode above VREF, or about 3.1 V, allowing fast discharge of the capacitor when the system resets.

2.3 POK Bias

The POK pin has some specific requirements based on industry standard PC power supply specifications. At start-up, the POK pin must not rise above 0.4 V. The POK pin is an NPN open collector whose base is tied to VCC via a simple resistor. Therefore, once VCC pulls above one diode or about 0.6 V, the POK pin will go low and saturate. If the POK pin external pull-up is to the 5 V output, the POK signal will not go above 0.4 V if the VCC of the AS23xx is tied to the 12 V output or an auxilliary rail.

2.4 POK Start-up Timing: PGCAP

In addition to 2.3 above, most PC power supplies require the POK pin to remain low until all outputs have been good for at least 100 ms but not more than 500 ms. A cap to ground on the PGCAP pin allows to the PSU designer to set the timing delay between the PSU outputs becoming good and the POK pin going high. The PGCAP pin provides a 1 µA current source to charge the cap, and when the cap charges above 2.5 V, the POK pin goes high. When an undervoltage occurs, the PGCAP pin discharges rapidly and the POK pin goes low. The POK pin does not respond to overvoltages.

2.5 Isolated Remote On/Off Switching: OFF and FAULT

A low voltage, isolated remote on/off switch may be implemented with the AS23xx OFF pin. If the chip VCC is run off an auxilliary rail, the FAULT signal may be used to start and stop the PSU. When the OFF pin is pulled from high to low or grounded, the FAULT pin resets to a low state, which may be used to drive an optocoupler to enable the primary side PWM controller. Allowing the OFF pin to go open circuit or high causes the POK pin to go low immediately, and the FAULT pin will go high after a time delay set by a cap to ground on the DELAY pin. This allows the customer's system to receive a POK warning before the PSU actually shuts down.

Section 3 - PSU Shutdown Sequences

3.0 Shutdown Sequence

For normal shutdowns, the primary requirement is that the POK signal should go low some minimum time before the PSU outputs fall out of spec.

3.1 Delaying Remote OFF: DELAY

In systems which use the OFF and FAULT pins to provide remote on/off switching, the delay between the OFF pin going high and the FAULT signal going high is programmable with a capacitor to ground on the DELAY pin as described in 2.5 above. The POK pin, on the other hand will go high immediately after the OFF pin is open circuited or pulled high, giving the system warning of the impending shutdown. The DELAY pin provides a 1 µA current source to charge the cap, and when the cap charges above 2.5 V, the FAULT pin will go high.

3.2 AC Warning Prior to Primary Drop-out

In systems where the input line voltage is switched, the AC pin threshold should be set so that it causes POK to go low before the primary bulk voltage reaches drop-out and the primary PWM shuts off. The output of the AC comparator also causes the UVB pin to pull low, so that the undervoltage sensing does not trip the FAULT latch as the outputs fall below spec. Recall that the AC pin senses a divided down and filtered representation of the secondary side switching waveform, which will provide a proportional representation of the primary voltage via the turns ratio of the transformer.

Notes

AS300

Shunt Temperature Sensor

Features

- Calibrated directly in Kelvin
- Linear 10 mV/°C scale factor
- 1° C typical accuracy at 27° C (300 K)
- Fully rated for - 40 to 125° C (233 to 398 K)
- Suitable for remote applications
- Low-impedance output, 0.3 for a 1mA load
- Now available in the SOT-223 for improved substrate temperature sensing

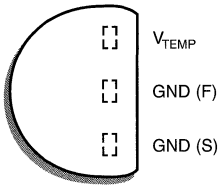
Description

The AS300 is a two-terminal integrated circuit temperature sensor. It is a precision-trimmed shunt type regulator that emulates a zener diode in function. Its output voltage is linearly proportional to temperature in Kelvin. The output voltage is calibrated for 3.000 V at 27° C (300 K) and increases by 10 mV/°C.

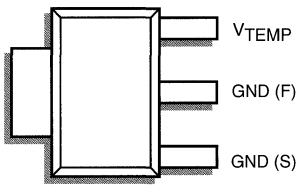
The AS300 is available in four packages. Both the TO-237 and SOT-223 offer large heat-sinks for transferring heat to the die for fast and accurate thermal sensing. The TO-237 makes an ideal free air sensor. This package has the same package dimensions as the familiar TO-92, but integrates a 10 square millimeter heat-sink extending from the top of the package. The SOT-223 is especially effective at sensing the temperature of hybrid and MCM substrates. The 8L SOIC is best-suited for applications requiring a small footprint or precision force/sense metering.

Pin Configuration — Top view

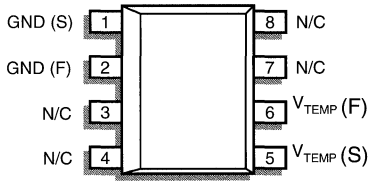
TO-92 (LP)
TO-237 (HP)



SOT-223 (G)



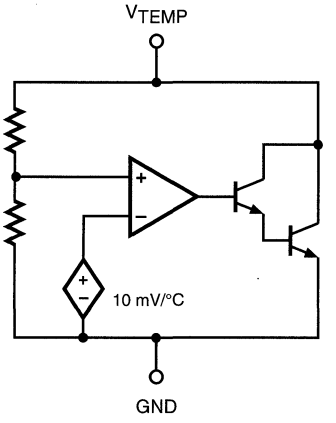
SOIC (D)



Ordering Information

Description	Temperature Range	Order Codes
TO-92	-40 to 125° C	AS300LP
TO-237	-40 to 125° C	AS300HP
SOT-223	-40 to 125° C	AS300G
8-Pin Plastic SOIC	-40 to 125° C	AS300D

Functional Block Diagram



Pin Function Description

Pin Number		Function	Description
TO, SOT	SOIC		
1	1	GND (S)	Optional sense pin ground, otherwise tie to substrate pin GND (F).
2	2	GND (F)	Signal ground and circuit substrate.
3	6	V_{TEMP} (F)	Output voltage proportional to temperature. V_{TEMP} is nominally 3.00V at 27° C (300 K) and increases at 10 mV/°C.
–	5	V_{TEMP} (S)	Optional sense pin for V_{TEMP}. Available on the 8L SOIC package only. Tie pin to V_{TEMP} (F) if not using force/sense metering.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Current	I_{REF}	20	mA
Continuous Power Dissipation at 25° C	P_D		
TO-92		775	mW
TO-237		1000	mW
SOT-223		1250	mW
8L SOIC		750	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Lead Temp, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160° C/W	80° C/W	6.3 mW/°C
TO-237	125° C/W	8° C/W	8.0 mW/°C
SOT-223	115° C/W	8° C/W	8.7 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over the full junction temperature range (-40 to 125° C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	V_{TEMP}	I_K = 2 mA, T_J = 27° C (300 K)	2.970	3.000	3.030	V
	V_{TEMP}	I_K = 2 mA, T_J = 100° C (373 K)	3.690	3.730	3.770	V
Temperature Coefficient Error		I_K = 2 mA, deviation from 10 mV/°C		40		µV/°C
Minimum Operating Current	$I_{K\,(min)}$				0.6	mA
Output Impedance	Z_{KA}	I_K = 0.6 to 5.5 mA		0.3	2	Ω

Test Circuit

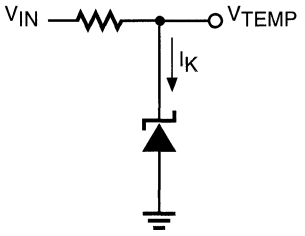


Figure 1

Typical Performance Curves

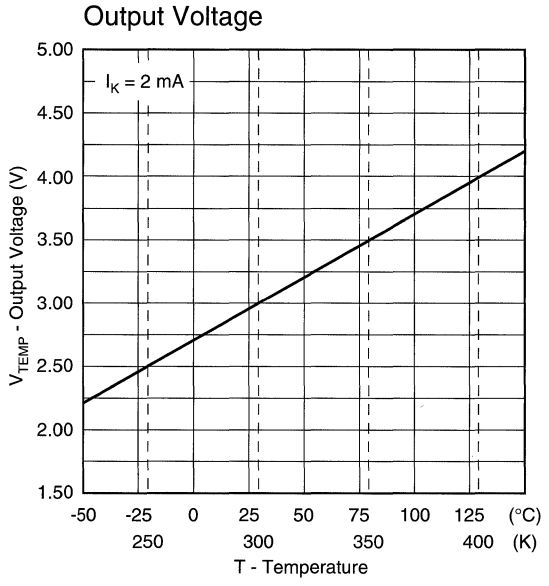


Figure 2

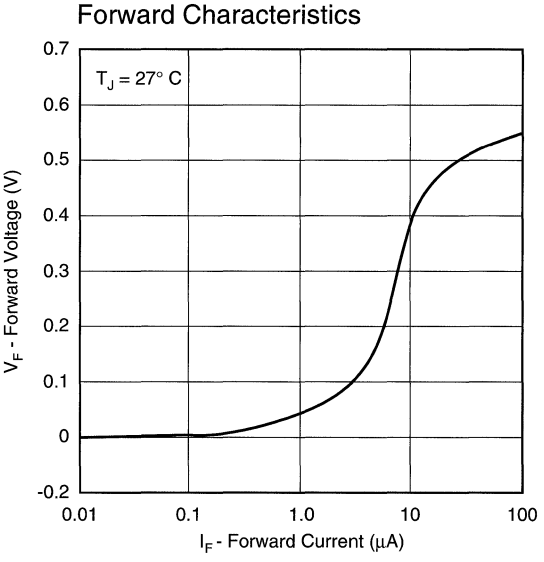


Figure 3

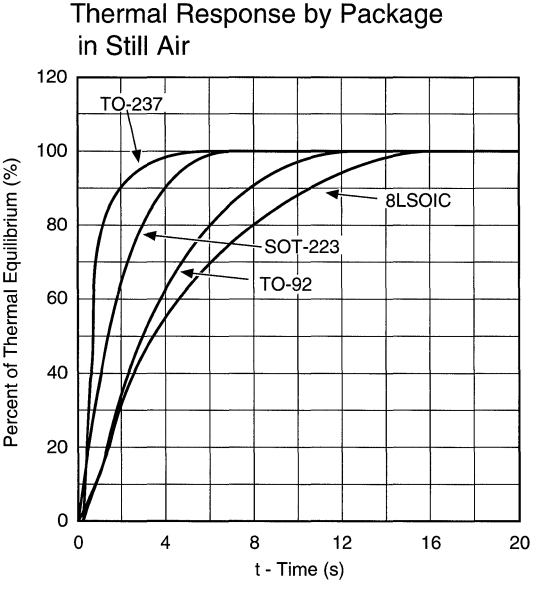


Figure 4

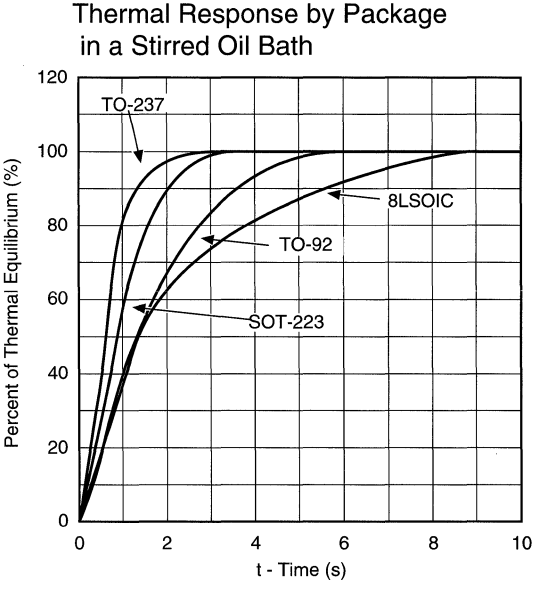


Figure 5

Typical Performance Curves

Operating Characterisitics

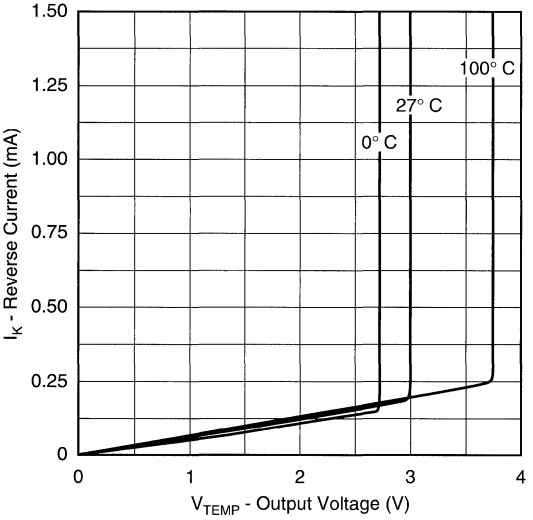


Figure 6

Operating Characterisitics

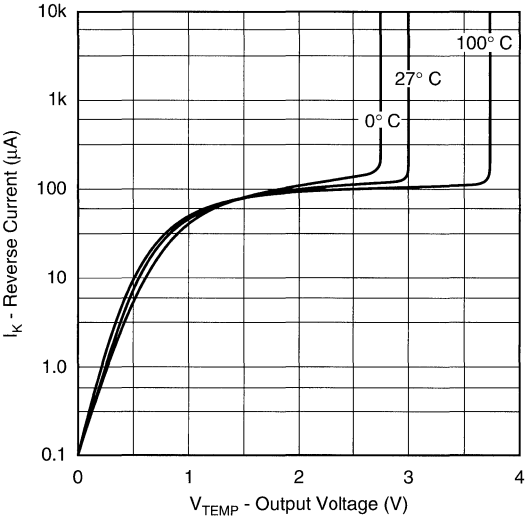


Figure 7

Dynamic Impedance

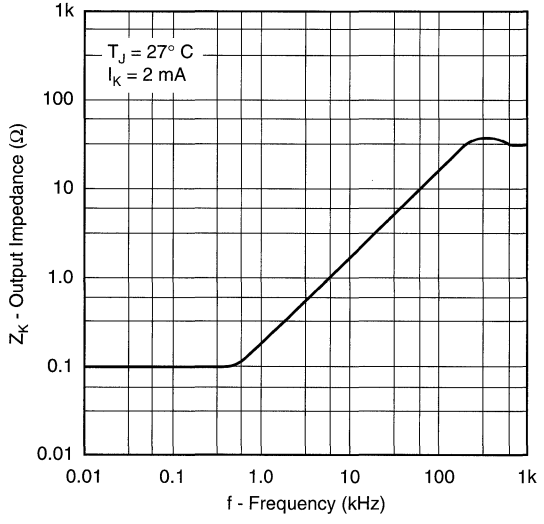


Figure 8

Transient Response

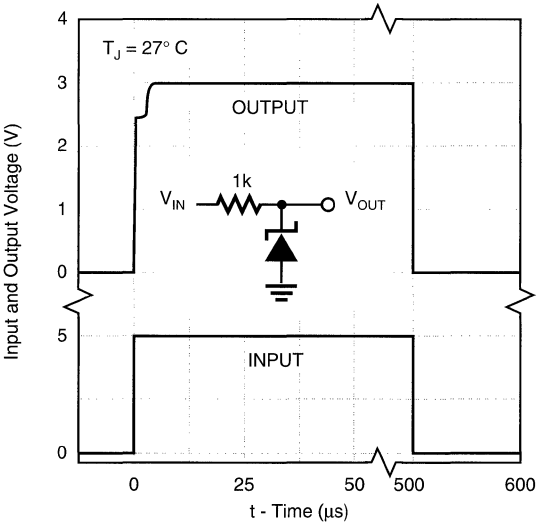


Figure 9

Typical Applications

Linear Fan Controller

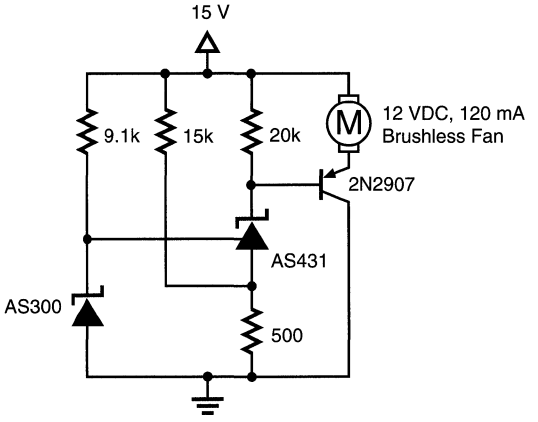
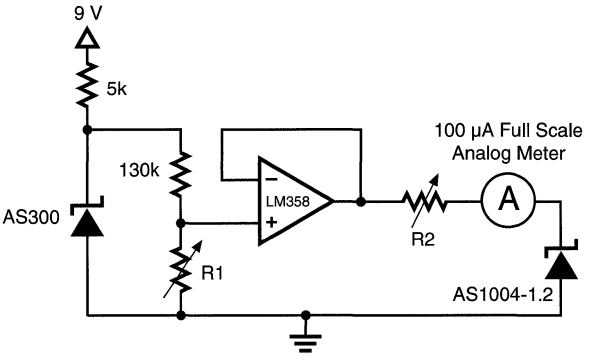


Figure 10

Fahrenheit Thermometer



Adjust R1 to set 0° F reading (120k)
Adjust R2 to set 100° F reading (2.7k)

Figure 11

Linear Fan Controller

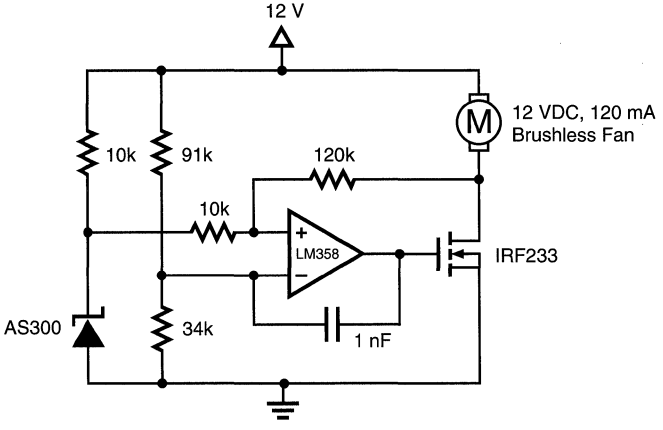


Figure 12

Thermostat

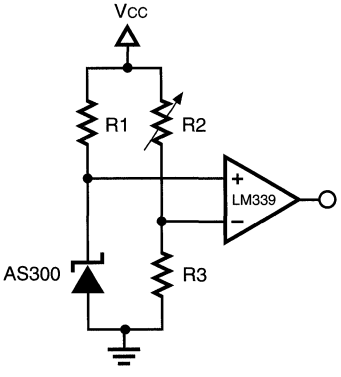


Figure 13

AS273

Over-Temperature Detector

Features

- Programmable to three different Over-temperature thresholds
- 2.5 V temperature compensated bandgap reference trimmed to 1%
- Open collector output goes low on over-temp condition
- ±3° C temperature accuracy
- Reference shunt current serves to program over-temp threshold
- Available with 5° C or 10° C of temperature hysteresis
- Available in a wide range of over-temp thresholds to fit most temperature monitoring applications
- Now available in the SOT-223 for improved substrate temperature sensing

Description

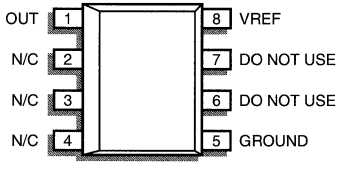
The AS273 is a series of programmable over-temperature detectors. Each is internally composed of a precision 2.5 V shunt reference, a proportional-to-absolute temperature thermal sensor, a comparator with controlled hysteresis, and an open collector output that indicates an over-temp condition. The threshold for the over-temp signal can be set to any of three values on a given part by controlling the magnitude of the reference shunt current.

The AS273 has an excellent absolute temperature accuracy of ±3° C for each of the three over-temp thresholds. The low power dissipation minimizes any temperature sensing errors due to self-heating. There is either 5° C or 10° C of temperature hysteresis to prevent bouncing when an over-temp condition is removed.

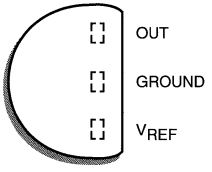
The packaging options available with the AS273 make it appealing to a wide variety of temperature-sensing applications. The TO-237 package with a built-in heat sink allows for highly accurate ambient temperature sensing. The TO-92 package can be mechanically clamped to a heat sink to monitor the temperature of power devices. The 8L-SOIC and SOT-223 surface mount packages allow for temperature sensing in high component density applications.

Pin Configuration — Top view

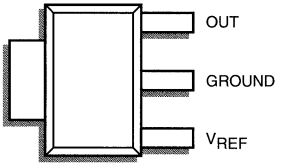
SOIC (D)



TO-92 (LP), TO-237 (HP)



SOT-223 (G)



Ordering Information

AS273 - T H - P

- T: Temperature Option see A
- H: Hysteresis Option see C
- P: Package Type see B

A. Temperature Options

Code	T_{OT1}	T_{OT2}	T_{OT3}
D	40	45	50
F	75	80	85
G	90	95	100
H	105	110	115

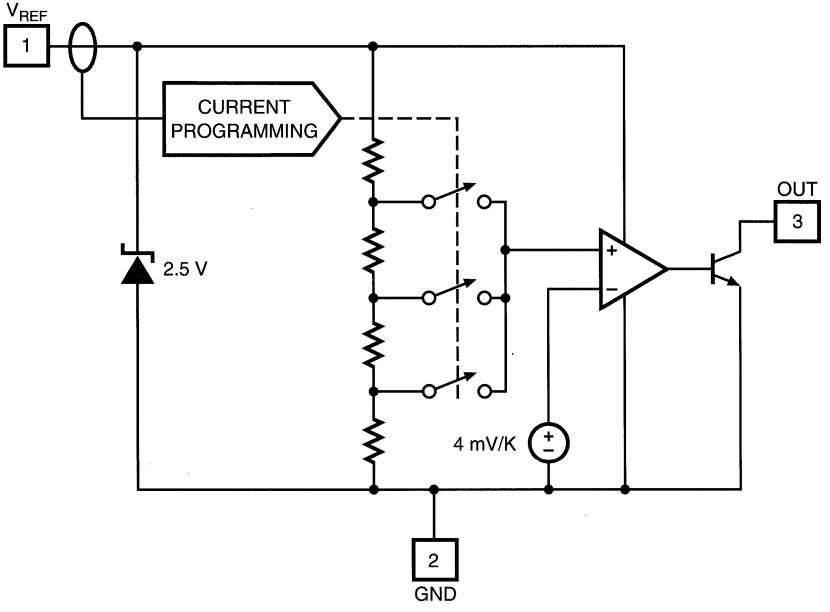
B. Package Types

Code	Package
HP	TO-237
LP	TO-92
D	SO-8
G	SOT-223

C. Hysteresis Options

Code	Temp. Hysteresis
1	10° C
5	5° C

Functional Block Diagram



Pin Function Description

Pin Number	Function	Description
1	V_{REF}	2.5 V shunt reference; current into V_{REF} pin also programs over-temperature trip point to one of three T_{OT} values
2	GND	Circuit ground and silicon substrate
3	OUT	Open collector output. Output low when die temperature exceeds programmed trip point

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Reference Current	V_{REF}	±10	mA
Output Current	I_{OUT}	±10	mA
Output Voltage	V_{OUT}	18	V
Continuous Power Dissipation at 25° C			
TO-92	P_D	775	mW
TO-237	P_D	1000	mW
8-SOIC	P_D	750	mW
SOT-223	P_D	1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Lead Temp, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
SOT-223	115° C/W	8° C/W	8.7 mW/°C
TO-92	160° C/W	80° C/W	6.3 mW/°C
TO-237	125° C/W	8° C/W	8.0 mW/°C
8L SOIC	175° C/W	45° C/W	5.7 mW/°C

Electrical Characteristics

Electrical Characteristics are guaranteed over the full junction temperature range (0 to 125° C). Ambient temperature must be derated based upon power dissipation and package thermal characteristics.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference						
Reference Voltage	V_{REF}	I_{REF} = 2 mA, T_J = 25° C	2.500	2.525	2.550	V
Load Regulation	V_{Id}	0.65 mA ≤ I_{REF} ≤ 5.5 mA		5	10	mV
Average Temperature Coefficient	$\Delta V_{REG}/\Delta T$	0.65 mA ≤ I_{REF} ≤ 5.5 mA		75		ppm/°C
Output						
Saturation Voltage	V_{OL}	I_{OUT} = 4 mA; $T_J > T_{OT}$		200	400	mV
Breakdown Voltage	BV	I_{OUT} =100 µA; $T_J < T_{OT}$	18	30		V
Leakage Current	I_{OH}	V_{OUT} = 18 V; $T_J < T_{OT}$		1	1000	nA
Over-Temp Sensing						
Temperature Accuracy	$T_{OT(1)}$	0.7 mA ≤ I_{REF} ≤ 1.3 mA	–3		+3	°C
	$T_{OT(2)}$	1.55 mA ≤ I_{REF} ≤ 2.6 mA	–3		+3	°C
	$T_{OT(3)}$	3.0 mA ≤ I_{REF} ≤ 5.0 mA	–3		+3	°C
Hysteresis	H_{OT}	Percentage Error in Nominal Hysteresis	–30		+30	%

Test Circuit

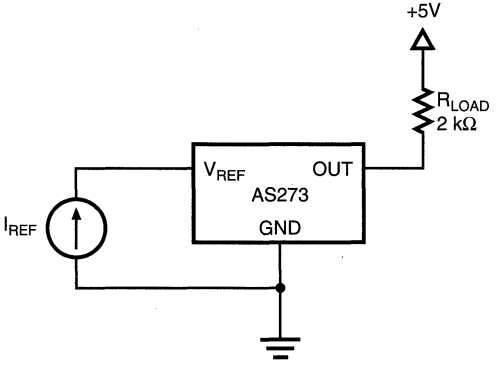


Figure 1. Test Circuit for Output Hysteresis Curve

Typical Performance Curves

Minimum Reference Current for Regulation

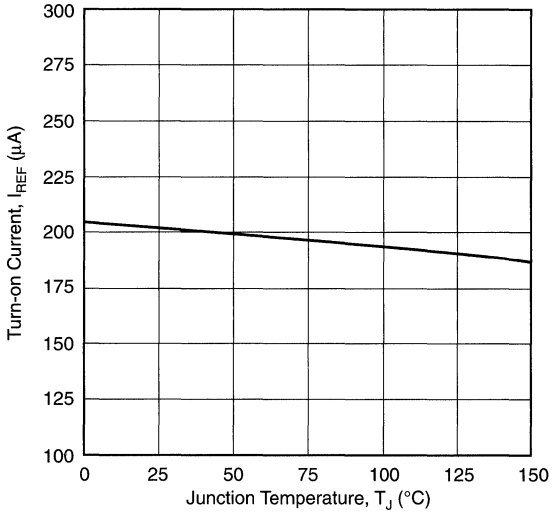


Figure 2

Turn-on Characteristic of Reference

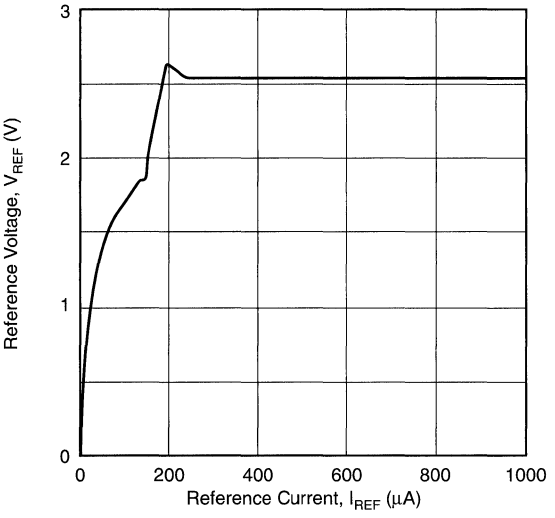


Figure 3

Temperature Regulation of Reference

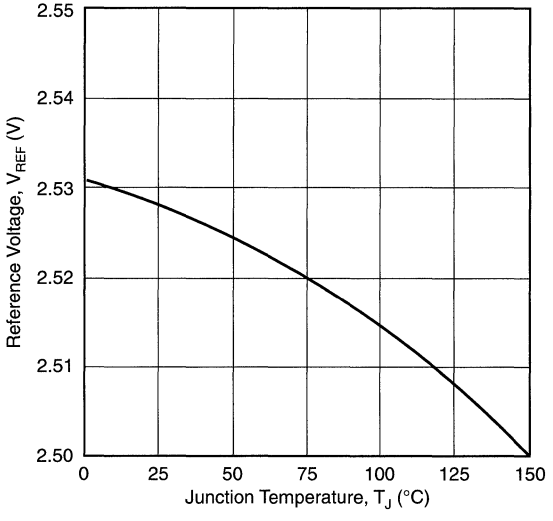


Figure 4

Load Regulation of Reference Over-temperature

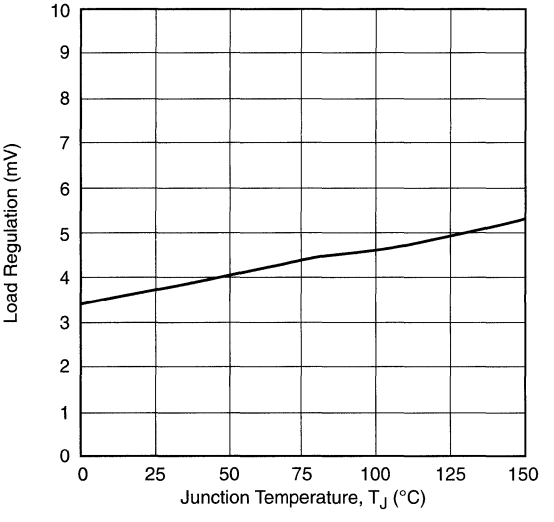


Figure 5

Typical Performance Curves

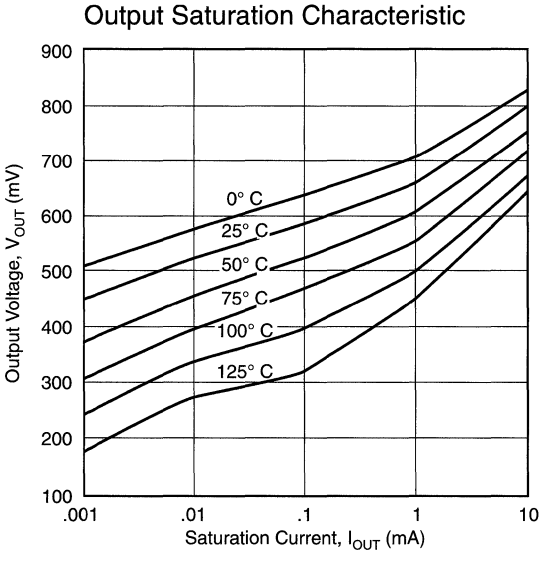


Figure 6

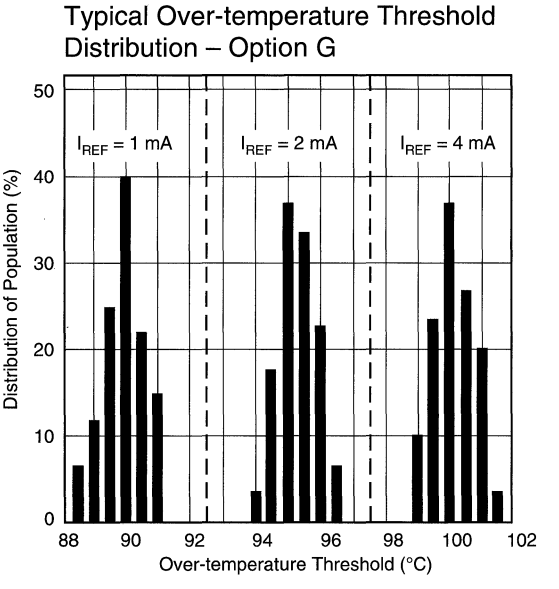


Figure 7

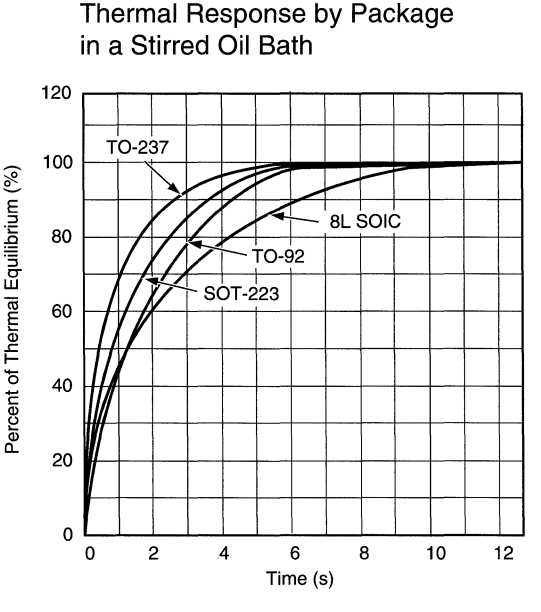


Figure 8

Theory of Operation

The AS273 is an over-temperature detector that gives an over-temp signal when the device junction temperature exceeds a programmed over-temp threshold. Over-temp threshold programming is accomplished by controlling the magnitude of the reference shunt current.

Over-temperature Condition

Internal to the AS273 is a temperature sensor which creates a voltage proportional to the absolute temperature(PTAT) of the die. This PTAT voltage is compared with a fraction of the reference voltage corresponding to the over-temperature threshold. When the PTAT voltage exceeds the reference voltage, the comparator is tripped and an over-temp signal is given to the output. The output consists of an open collector transistor that pulls low on an over-temp condition. Built into the comparator is temperature hysteresis, which keeps the over-temp signal until the junction temperature has fallen 5° C (or 10° C) below the over-temp threshold. Figure 9 shows the output of the AS273 (with 10° C of hysteresis) over a range of junction temperature.

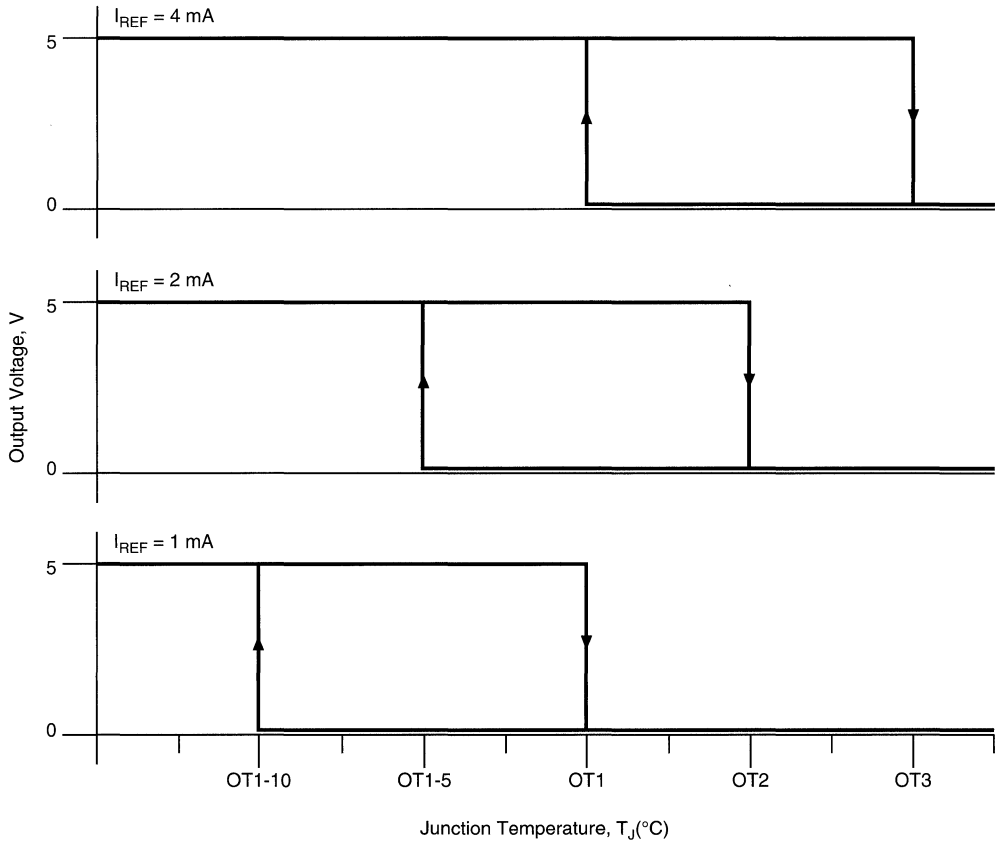


Figure 9. Temperature Characteristic of Output with 10° C of Hysteresis

Current Programming

There are three different over-temp thresholds for each AS273. The detector senses the amount of current being shunted through the 2.5 V reference of pin 1 and programs an over-temp threshold based on the magnitude of that current. Figure 10 illustrates the ranges of reference shunt current, I_{REF}, associated with each of the three over-temp thresholds, OT1, OT2 and OT3.

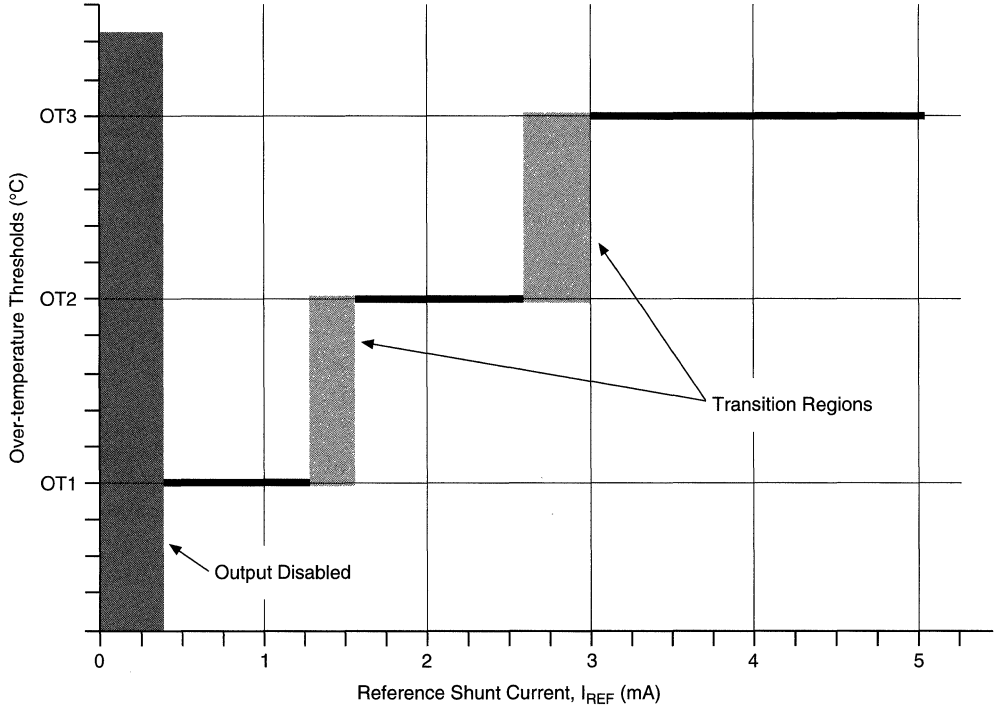


Figure 10. Reference Shunt Current Programming Ranges of Over-temperature Thresholds

Typical Over-Temperature Detector Applications

Over-Temperature Detector

The AS273 senses the ambient temperature and turns on its open collector output to indicate an over-temp condition. Each AS273 can be programmed to any one of its three over-temp thresholds by forcing a different range of current into the reference pin.

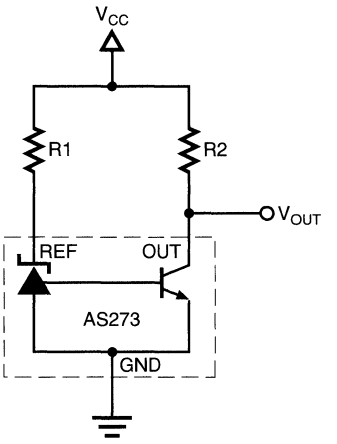


Figure 11.

Dual Speed Fan Control

The diagram of Figure 12 shows an easy way to implement smart fan control. When the temperature is below the over-temp trip point set by R1, the detector's open collector output is off. Therefore, the fan speed is controlled by the ratio between R2 and R3. When the temperature exceeds the over temp set point, the open collector is turned on, and fan motor runs at its full speed.

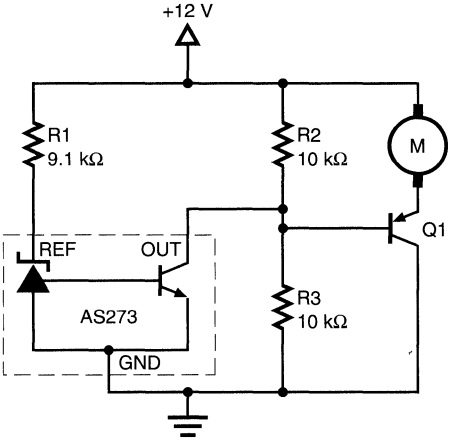


Figure 12.

Over-Temperature Protection with Latch (Low Current)

The diagram of Figure 13 illustrates how a power supply can be shut down with a simple two-transistor latch. When the programmed over-temp is reached, the open collector output of the AS273 enables the latch and pulls V_{CC} below the under-voltage threshold of the AS3842 ,shutting off the AS3842. The latch can be disabled only with a power reset.

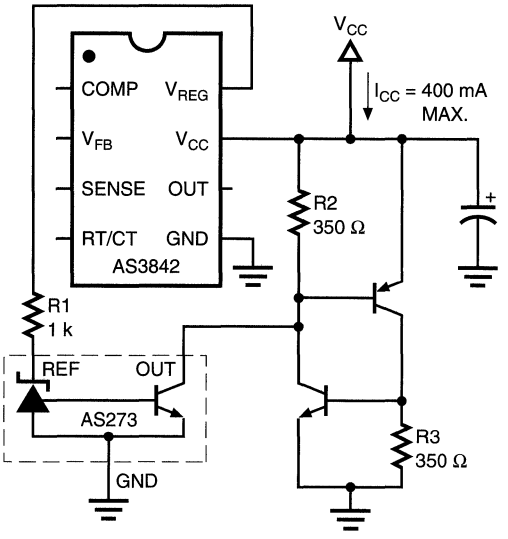


Figure 13.

Over-Temperature Protection with Hysteresis

In this over-temperature circuit, the hysteresis of the AS273 is used to automatically restart the power supply after the temperature drops below the hysteresis temperature window. R1 supplies the current to power the AS273 after the AS3842 and the power supply are shut down. R2 and the external zener set the over temperature trip point.

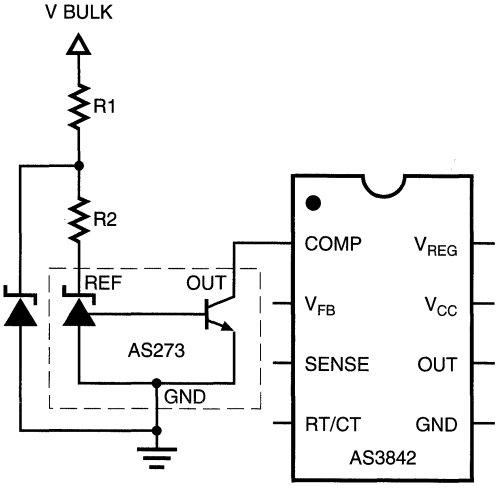


Figure 14.

Adjustable Hysteresis Temperature Detector

The hysteresis of the AS273 can be increased by reprogramming the device to a lower temperature set point upon over-temp. A higher temperature is set by R1. When the temperature exceeds the high-temp set point, the open collector output is turned on and allows R2 to rob current from the reference pin and resets the AS273 to the low-temp set point. As a result, the hysteresis escalates by the difference between the high-temp and the low-temp set points.

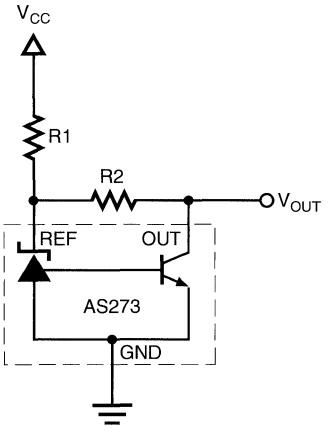
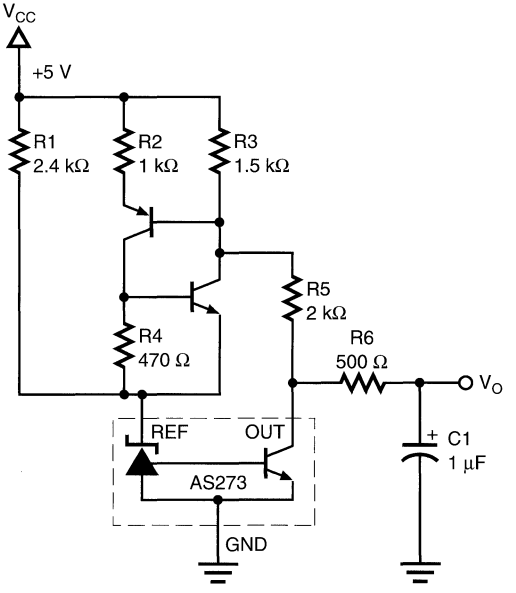


Figure 15.

Three-State Temperature Sensor

In the Three-State Temperature Sensor shown in Figure 16, a low-temp trip point is selected by R1 and a high-temp trip point is selected by the two-transistor latch. When the temperature is below the low-temp set point, V_{OUT} is in the high state (V_{OUT} = 5.0 V). When the temperature exceeds the low-temp set point, the two-transistor latch is set and V_{OUT} is pulled low (V_{OUT} = 2.5 V). The latch also supplies extra current to the reference pin to reset the IC to sense a higher temperature. Once the high-temp is reached, the output will turn "on" (V_{OUT} = 0.2 V). This circuit is highly useful in applications where a stand-by, a warning and a shut-down state are required.



Stand-by State:	T < T1, T2	V_O = 5.0 V
Warning State:	T1 < T < T2	V_O = 2.5 V
Shut-down State:	T1, T2 < T	V_O = 0.2 V

Figure 16.

Notes

AS17xx

Semicustom Bipolar Array

Features

Size (single tile)

- 87 x 75 mils
  Expandability of array
  (to 2 or 4 tiles)

Component Availability (single tile)

• Small NPN	48
• Dual collector PNP	21
• Vertical PNP	4
• Power NPN	3
• Diffused Resistors (total)	300 k
• Pinch Resistors (3-terminal, 30k)	8
• Cross-unders	13
• Buses	6

Basic Electrical Specs

• Transistor Matching (NPN & PNP)	<2%
• Primary voltage limitations:	
LV_{CEO}	18 V
BV_{CBO}	30 V
• Diffusion to substrate (Ground)	30 V
• NPN Parameters	
Beta	80–500
f_T (1mA)	300 MHz
BV_{EBO}	7 V
• PNP Parameters:	
Beta	20–300
f_T (1mA)	300 MHz
BV_{EBO}	30 V

Description

The AS17xx is Astec's proprietary semicustom bipolar array. This semicustom IC is a collection of individual transistors and resistors in a fixed configuration. The custom circuit is manufactured by creating a single metal mask to connect the components. This allows the designer to deal with only one mask for the IC layout instead of the actual 10 mask process. The semicustom array is useful for a wide range of functions, both analog and digital. In its simplest configuration, the AS17xx has 76 active devices available, but can be expanded to give up to four times this number in its largest configuration. This expandability of the array is a unique feature, allowing a whole range of semicustom circuits to be manufactured.

Because Astec has ongoing manufacturing of high volume circuits on this array, incremental wafer costs for engineering purposes are low. Therefore quality and reliability can be maintained even with small volume or engineering lots. Since the silicon can be completely processed and held awaiting only the metal etch and passivation steps, extremely fast turn-around times can be achieved.

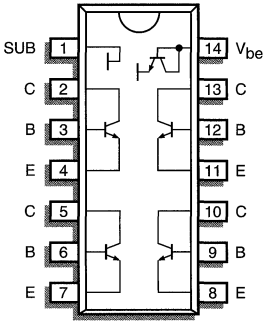
The AS17xx bipolar array uses a standard "20 Volt" bipolar technology. Although quite similar to industry standard arrays, it has a number of important improvements. First, the ratio of PNPs to NPNs has been increased to allow for more modern design practice. Second, the process has been modified to allow for a deep collector diffusion (sinker) which not only improves the $V_{CE(SAT)}$ of the transistors, but also allows for the elimination of regions with thin oxide which historically plague semicustom die with electrostatic discharge reliability concerns. Third, a set of low resistance sinker resistors allows for bussing supply or signal lines without using active components for cross-unders. In addition, the specific component geometries have been further optimized to facilitate the layout compared to the industry standard arrays. Resistors are now in a binary weighted 500 / 1k / 2k / 4k sequence for more simple value calculations. The power devices use multiple standard size emitters

so that they may also be used to create a device with an integral emitter area ratio with respect to a standard small NPN.

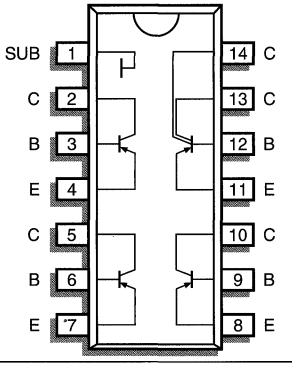
The AS17xx bipolar array can be packaged in industry standard DIP or surface mount packages with 8 to 40 leads. The number of pads available on the AS17xx varies with the number of tiles used as follows: single tile per die = 18 pads, two tiles per die = 30 pads, and four tiles per die = 40 pads. The extra pads not used for bonding to leads can be used for wafer level testing, trimming, and debugging.

Pin Configuration — Top view

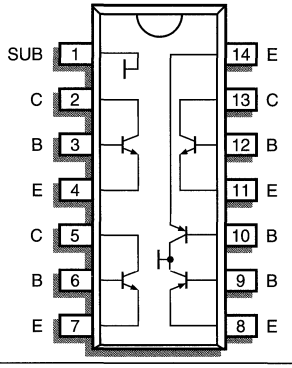
PDIP (N)
AS1700-NPN Kit Part



PDIP (N)
AS1700-PNP Kit Part



PDIP (N)
AS1700-PWR Kit Part



Die Configuration — Top view

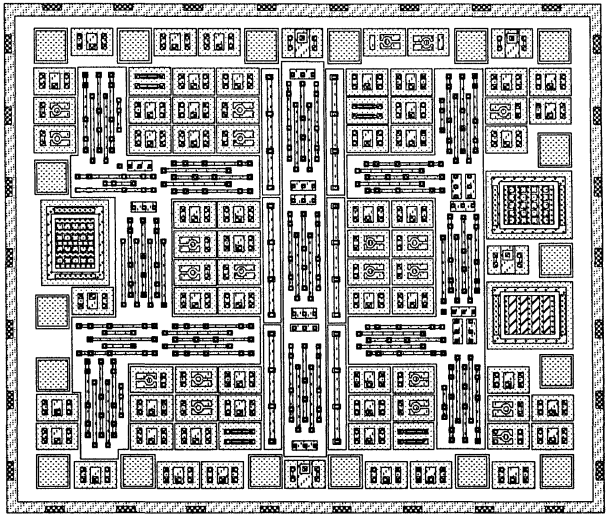


Figure 1. Single Tile Bipolar Array

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Continuous Power Dissipated at 25° C	P_D		
Single Transistor		300	mW
Total Package		1400	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Lead Temperature, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-NPN: Minimum NPN						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	60		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	8		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_C = 100 µA	0	95	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 100 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 100 µA	80	125	500	
Early Voltage	V_A			−150		V
Transistor Matching (measuring Δ I_C)		I_C = 200 µA	−10	<1	10	%
AS1700-PWR: Large NPN (20-emitter)						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_C = 1 mA	20	35		V
Collector-to-Base Breakdown Voltage	BV_{CBO}	I_C = 100 µA	50	58		V
Emitter-to-Base Breakdown Voltage	BV_{EBO}	I_E = 10 µA	5	7.6		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 200 µA, I_C = 2 mA	0	20	200	mV
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 200 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{CE} = 3 V, I_C = 2 mA	80	125	500	
Early Voltage	V_A			−150		V

Electrical Characteristics (cont'd)

All parameters measured at 25° C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AS1700-PNP: Lateral PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_E = 100 µA	30	50		V
Field-Effect Threshold Voltage	VTF	I_E = 10 µA		36		V
P + to Substrate Leakage	I_{SUB}	I_E = 100 µA, V_B = 1 V	0	150	500	nA
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_E = 100 µA	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	V_{EC} = 3 V, I_E = 100 µA	630	690	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{EC} = 3 V, I_E = 100 µA	20	60	300	
Early Voltage	V_A			–105		V
Transistor Matching (measuring Δ I_E)		I_E = 200 µA	–10	<1	10	%
Double Collector Matching (meas. Δ I_E)		I_E = 200 µA	–10	<1	10	%
AS1700-PWR: Vertical PNP						
Collector-to-Emitter Breakdown Voltage	LV_{CEO}	I_E = 100 µA	30	50		V
Collector Cutoff Current	I_{CEO}	V_{CE} = 18 V	0	2	100	nA
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	I_B = 10 µA, I_E = 100 µA	0	150	200	mV
Base-to-Emitter Voltage	V_{EB}	V_{EC} = 3 V, I_E = 100 µA	650	680	700	mV
Static Forward Current-Transfer Ratio	β (h_{FE})	V_{EC} = 3 V, I_E = 100 µA	20	125	500	

Typical Performance Curves

Minimum NPN

BETA vs I_C Over Temperature (−55° C to 125° C)

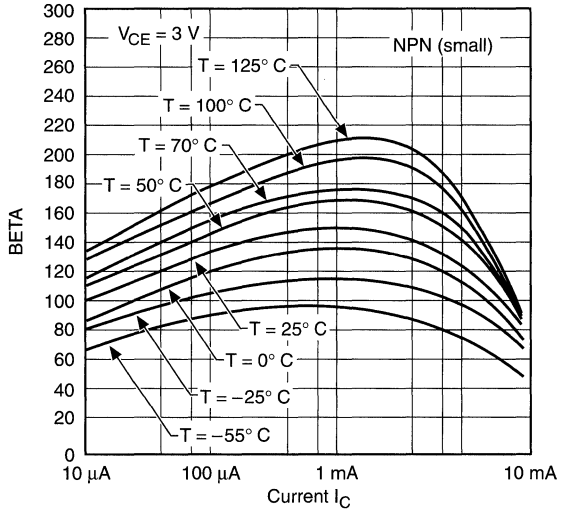


Figure 19

V_{EBO} Breakdown Voltage vs Temperature

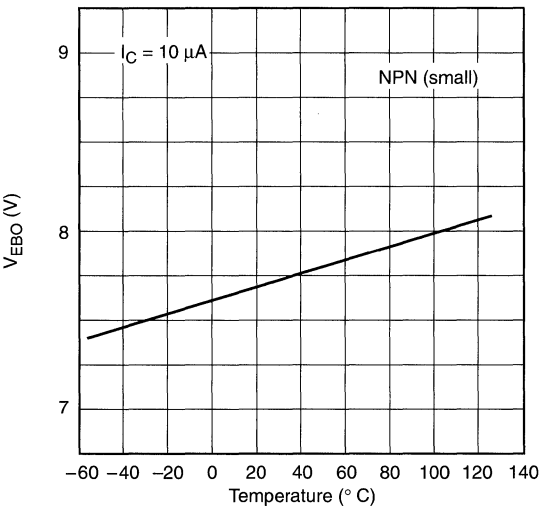


Figure 20

$V_{CE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

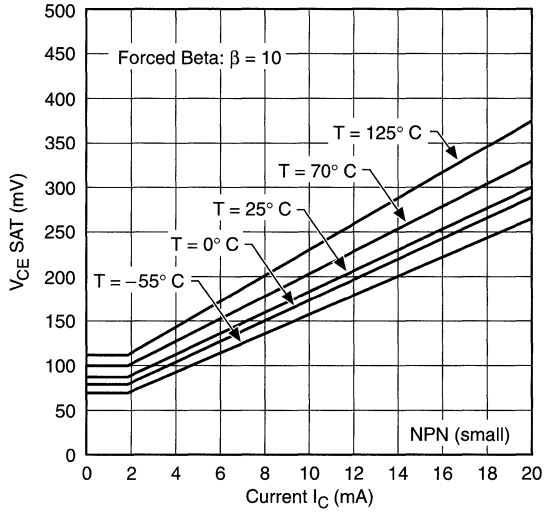


Figure 21

$V_{BE\ SAT}$ vs I_C Over Temperature (−55° C to 125° C)

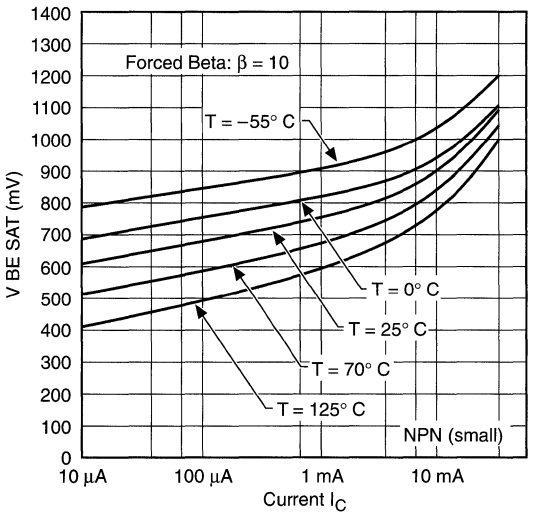


Figure 22

Typical Performance Curves

V_{BE} vs I_C Over Temperature
(−55° C to 125° C)

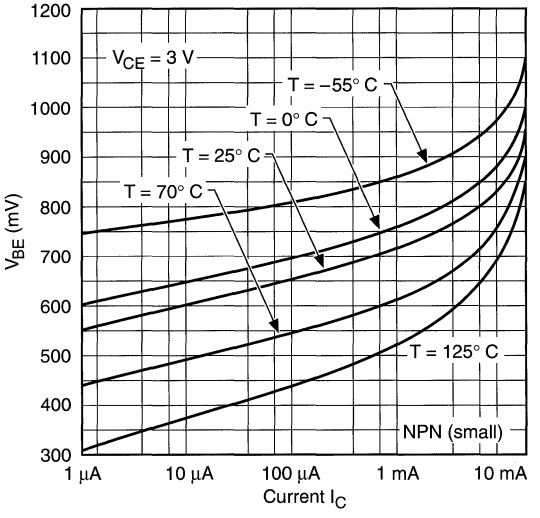


Figure 23

V_{BE} vs Temperature with Different I_C

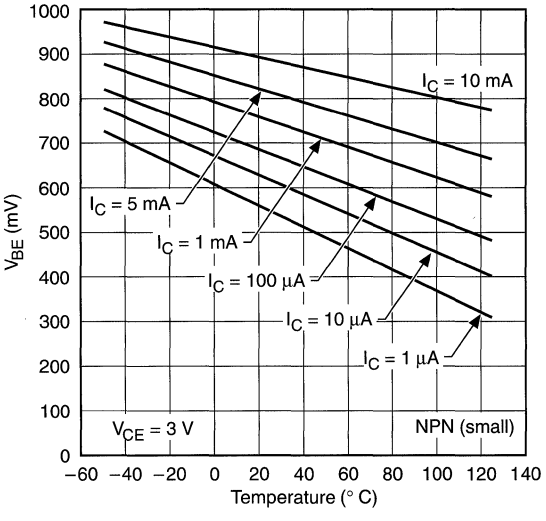


Figure 24

BETA vs I_C Over Temperature
(−55° C to 125° C)

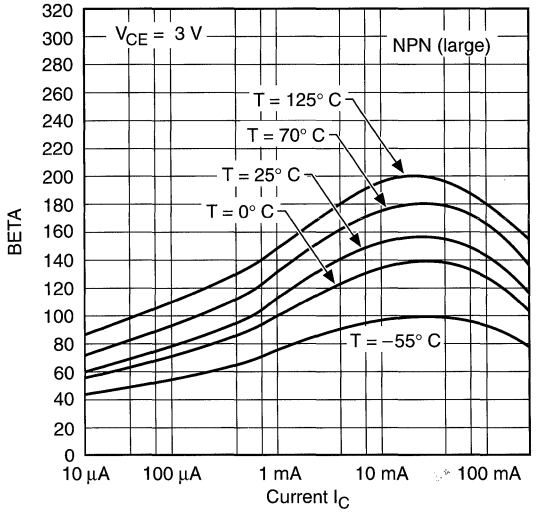


Figure 25

V_{EBO} Breakdown Voltage vs Temperature

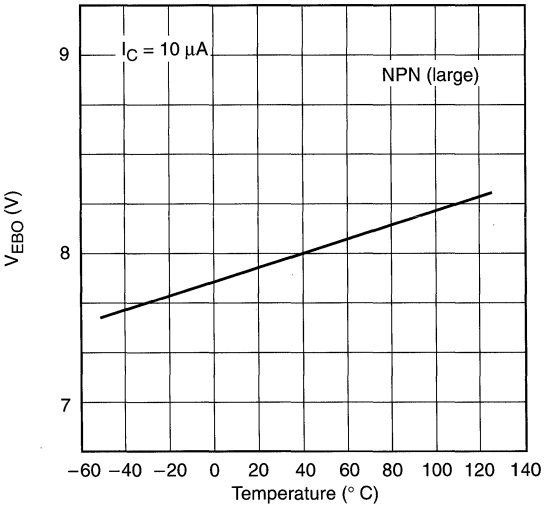


Figure 26

Typical Performance Curves

$V_{CE\ SAT}$ vs I_C Over Temperature
(−55° C to 125° C)

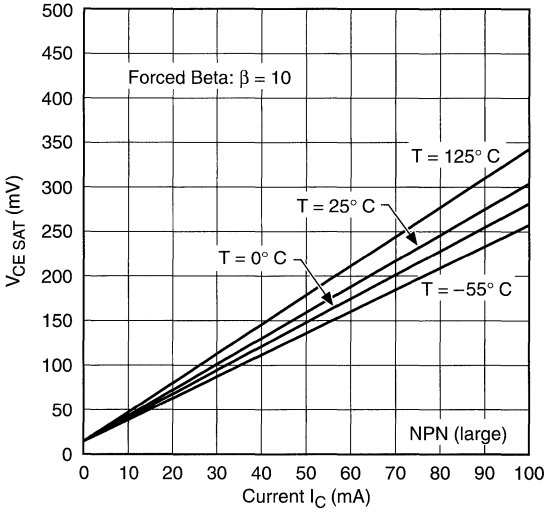


Figure 27

$V_{BE\ SAT}$ vs I_C Over Temperature
(−55° C to 125° C)

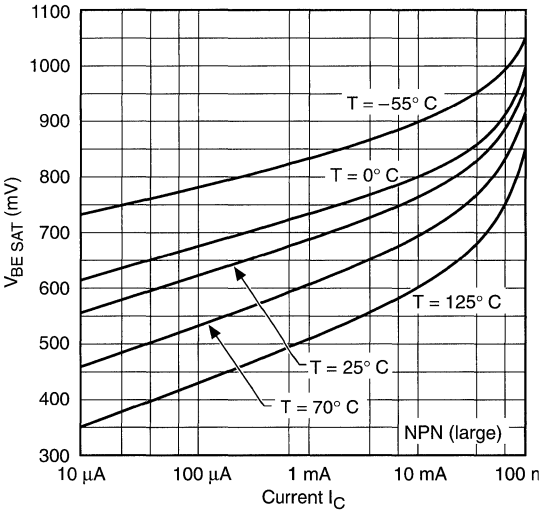


Figure 28

V_{BE} vs I_C Over Temperature
(−55° C to 125° C)

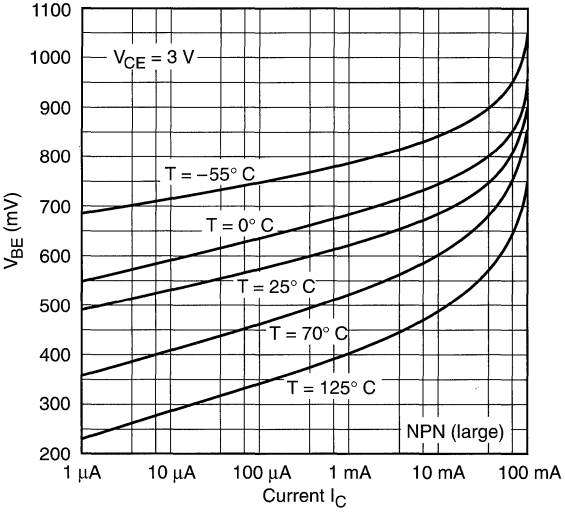


Figure 29

V_{BE} vs Temperature with Different I_C

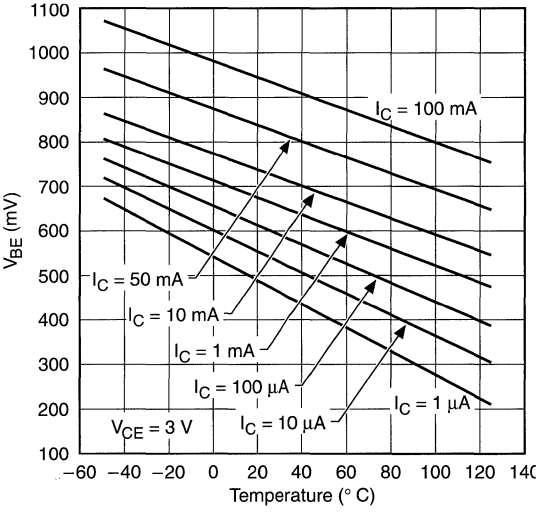


Figure 30

Typical Performance Curves

BETA vs I_E Over Temperature
(−55° C to 125° C)

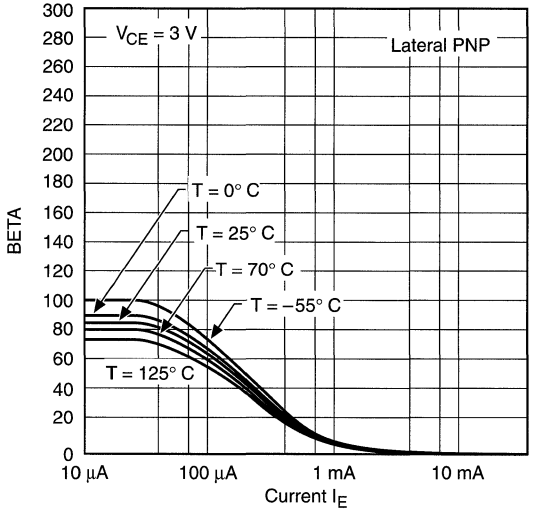


Figure 31

BETA vs I_E Over Temperature
(−55° C to 125° C)

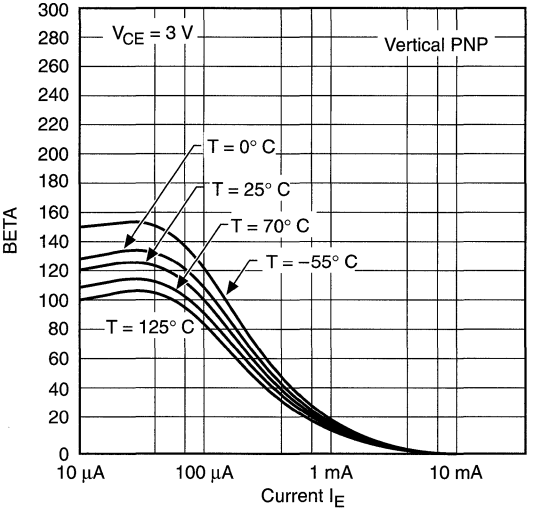


Figure 32

$V_{CE\ SAT}$ vs I_C

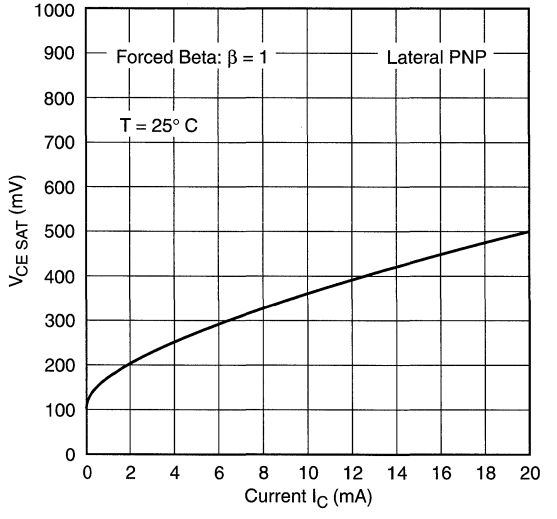


Figure 33

$V_{BE\ SAT}$ vs Temperature
(With different I_C)

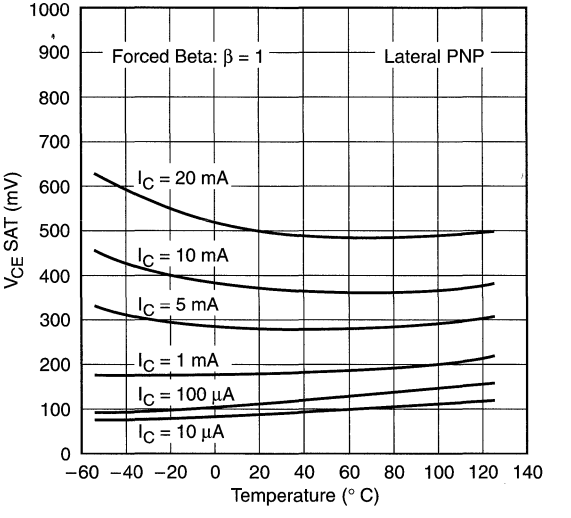


Figure 34

Typical Performance Curves

V_{BE} vs I_C Over Temperature
(−55° C to 125° C)

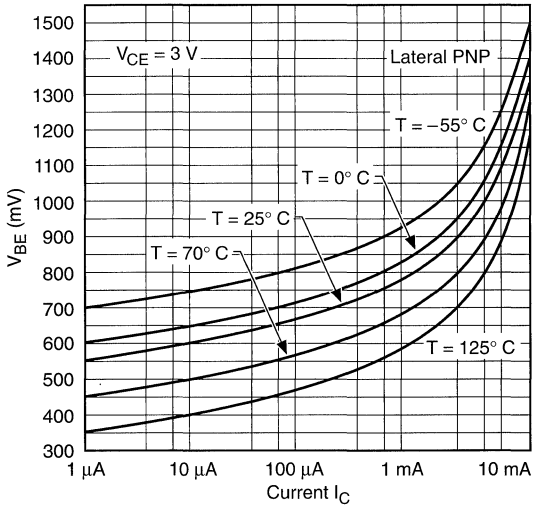


Figure 35

V_{BE} vs I_C Over Temperature
(−55° C to 125° C)

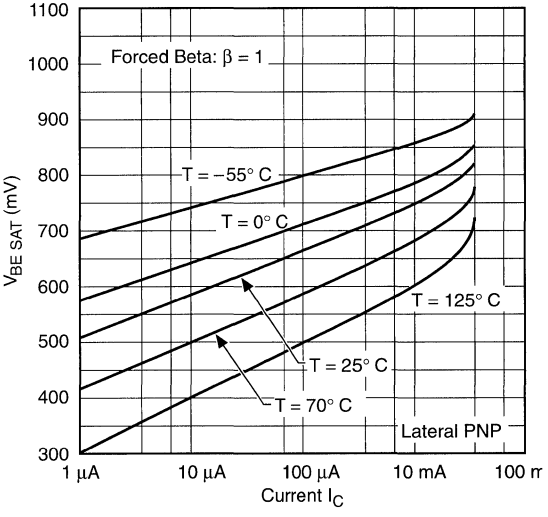


Figure 36

The Semicustom Application

The Design Considerations

The designer should take advantage of the resistor and transistor matching available with ICs and not rely on the absolute values of parameters. If a certain emitter area is desired for current ratioing, several transistors can be connected in parallel to simulate this condition, or by using the desired emitter area of an NPN power device (when breadboarding use the previous method). When using the double-collector PNP transistors, do not float one of the collectors; either tie them together or tie one to the substrate. Floating one of the collectors will severely reduce the beta. There are several values and types of resistors available on the AS17xx semicustom array as outlined in the resistor summary.

Resistor Summary

8 - Pinch Resistors
(30 k ± 50%, use at 5 V)
80 - Base String Resistors
Using full string lengths gives:
73 – 4 k
7 – 1.5 k
Using separate pieces of the strings gives:
67 – 500
63 – 1 k
43 – 2 k
30 – 4 k

Note: Do not try to use one resistor string for more than one resistor unless they are connected together in the circuit.

Additional components and their resistances are as follows:
13 - Cross-unders (370 for full length, and 190 for half length)
6 - Buses (at 10 between connection points)

Non-Integratable Components

Identify all non-integratable components such as inductors and capacitors. These will have to be supplied with external components. Note that junction capacitors can be formed using transistors with collector and emitter tied together for limited capacitance values.

Minimizing Stray Effects (Parasitics, Currents, and Capacitance)

The following steps are recommended:

1) Try to keep substrate currents as low as possible (under a few mA) to prevent isolation loss and cross-talk between adjacent components. If a component has a high substrate current, try to isolate it from the other components and keep it as close to the substrate bonding pad as possible. The substrate current should be measured for either each kit part or the whole breadboard (with all the substrates tied together) using a 10 resistor connected to the most negative potential in the circuit.
2) Do not saturate any PNP. If this is unavoidable, limit the base current so that the substrate current in the kit part lead is kept low. This is because of the parasitic vertical PNP formed between the emitter, base and substrate in a lateral PNP will become active when the lateral PNP is saturated.
3) Do not use any diode-connected PNP over about 500 µA to avoid the above mentioned parasitic PNP.
4) Contact the N-layer (collector-plug) in the resistor-tubs to the most positive potential (this is for resistor-tub biasing and isolation, and is a concern only for the semicustom implementation of the circuit), and the substrate to the most negative potential in the circuit.
5) High-frequency oscillations can, on rare occasions, occur in the integrated circuit when the breadboard did not show any tendency toward oscillation. This can be caused by the stray capacitances in the breadboard, which are larger than those associated with the IC and tend to stabilize potentially unstable circuits. Therefore, every effort should be made to minimize stray capacitances in the breadboard. This can be done by using DIP sockets and soldered wire or printed circuit interconnects rather than the popular solderless plug-in breadboards which have up to 10 pF of pin-to-pin capacitance.

Breadboarding with Kit Parts

All circuits should be breadboarded before being implemented on the semicustom array using AS1700 Kit Parts, (which are transistor arrays made using the AS17xx semicustom array). This breadboard will simulate as accurately as possible all stray effects and how the circuit will perform when implemented with the semicustom array. We recommend that standard carbon resistors be used to simulate the integrated resistors, or precision thin film resistors if accurate ratios are required.

Evaluating your breadboard

After obtaining satisfactory performance from the breadboard, evaluate the effects of resistor, transistor and temperature variations.

We recommend simulating the worst-case resistance variations (which is 30% globally and 1% for matching and ratioing) on the breadboard by substituting the appropriate values for all resistors. Sensitivity to transistor parameter variations can be seen by interchanging kit parts. We also recommend that the breadboard be tested over the full operating temperature range of the circuit.

After testing is complete, make sure that the breadboard circuit is accurately reflected in the schematic by doing a thorough check to see if all modifications to the breadboard are included.

Layout options

After thoroughly testing the breadboard, begin the layout process. There are three options for doing the layout:

- **Customer layout** - You do the layout and provide Astec with a completed layout sheet (at 500x - which Astec will provide) ready for entry into our CAD system. Astec will review the layout for design rule violations and advise you so that you can correct them yourself or elect to have Astec fix them.
- **Vendor layout** - You may assign Astec the responsibility of the IC layout.
- **Customer supervised layout** - You assign the layout implementation to Astec but retain the responsibility for the final form and content. Basically you are subcontracting Astec to do the IC layout under your direction. This option requires a great deal of communication between the customer and Astec, but can yield the greatest control for the customer while reducing the layout time.

Layout guidelines

We recommend that several copies of the layout on the data sheet be made to facilitate the layout process before working with the 500x layout sheet. The layout copies can be used to sketch various interconnect options, and work out any design problems that may be encountered because of the layout process.

Functional blocks: We recommend that the circuit be broken down into functional blocks. The blocks are selected in such a way as to minimize the the number of interconnections with the other blocks. If the blocks are in sequence, the circuit can usually be divided so that only one or two connections are made between the blocks (other than power supply connections).

Block location: Next, add up the number of devices and pads required by each block. Then select an area of the chip for each block. There are a few considerations which must be kept in mind for the block placement. First, the selected area must contain the required number of components and pads. Second, the various areas should be located so that interconnections between them are as easy as possible. Finally, the locations of the various pads to be bonded to pins and their relationships to each other and the blocks should be considered. Bond wires should not cross each other.

Cross-unders & buses: Cross-unders can be useful for small resistance values, but be careful of connections that can not tolerate cross-under resistance (see resistor summary), such as the base connections for a diode-biased current source, etc. To make sure that a connection can tolerate the cross-under resistance, insert the appropriate valued resistor in the breadboard and evaluate its effect on circuit performance. Buses have low resistance and are valuable for connecting functional blocks together, and busing power supply voltages.

Thermal considerations: If one or more components dissipate heat, they should be located away from other components that require close matching. The matched components should be placed together an equal distance from the thermal source. This way both of the matched components will be heated equally. Total power dissipation in the circuit is a function of the package type and size. On average at least 500 mW can be dissipated without trouble. Larger packages can dissipate more heat.

Signal & common coupling: If high frequency signals are present which have large amplitude swings, these lines should be separated as much as possible with respect to their pin locations because of inductive or capacitive coupling between their pins and bonding wires.

Another coupling problem arises when there are long metal lines. For example, if there is a common ground line for both the input and output of an amplifier, the fluctuating current from the output could cause a voltage drop along the line that could effect the input. This coupling could cause distortion or oscillations. The solution to this problem is to run two separate ground lines to the ground pad.

Resistor ratioing: Where matched resistor values or precise ratios are required, identical resistor constructs and orientations should be used. Identical resistors orientated 90° to each other may have different values due to directionally dependent fabrication and packaging tolerances.

Component interconnection: We recommend numbering the components on the circuit schematic and using these numbers on the layout. Work on only one circuit block at a time and leave the block interconnections until all the blocks are finished. Start the layout by selecting several components of a block and placing them on the layout; sketch their interconnections and work outward marking the schematic as you go.

Metal routing: The metal routing can be sketched on the layout sheet taking into account the design rule considerations as follows:

Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance 0.02 per square)

The area around the outside of the chip has a metalized ring with numerous contacts to the substrate. The substrate must be connected to the most negative potential in the circuit. When laying out the circuit, the ground conductors should lead inward from the outer ring. There are several N-layer contacts for the different resistor tub areas that must be connected to the most positive potential in the circuit to maintain isolation.

Bonding pads: The rules for bonding pad layouts are very simple. You must be able to draw a straight line from a bonding pad to its pin without crossing any other wires, and the pads should be evenly spaced around the chip. The pin assignments are arbitrary, but they should be organized such that the pin numbers correspond to the pads in a counter-clockwise rotation around the chip, and not some random pattern that would cause bonding wires to cross each other.

Layout sheets (500x) are available upon request for final layout, and are used to make the metal interconnect mask and check spacing rules. We recommend that the metal interconnect be done on a clear film over the layout sheet with erasable markers before making the final layout. This will allow for modifications to be made with a minimum amount of effort.

Functional Circuit Blocks

The following circuits are presented as a guide to assist in circuit design using the AS17xx Semicustom Array.Complex circuit functions can be created from these elementry building blocks.These circuit blocks can be modified and improved to suit the designer's needs in creating a complete system.

Current Sources

Here are a few examples of PNP current sources; NPN current sinks can easly be derived from the analog of these PNP examples.

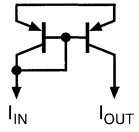


Figure 2. Simple PNP Current Source. Has Slower Frequency Response, and up to ±15% Tolerance Error.
$I_{OUT} = I_{IN} * (1 + 2/\beta)$

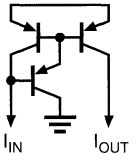


Figure 3. Widlar Current Source, Moderate Frequency Response.
$I_{OUT} = I_{IN} * (1 + 2/\beta^2)$

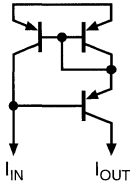


Figure 4. Wilson Current Source, Fast Frequency Response.
$I_{OUT} = I_{IN} * (1 + 1/2\beta^2)$

Comparator Input Stages

Several comparator input stages are illustrated below.

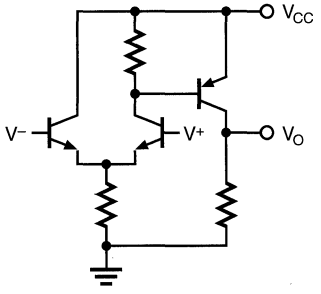


Figure 5. Simple NPN Type Comparator.

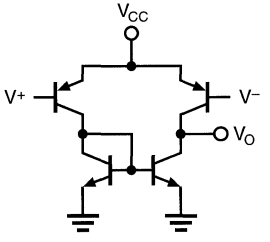


Figure 6. Simple NPN Type Comparator Input Stage.

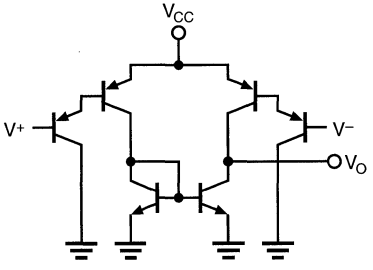


Figure 7. Improved PNP Type (Good GND Sensing) Comparator Input Stage.

Functional Circuit Blocks

Voltage Regulators/References

Figure 8. Zener Diode V_Z = 7 V

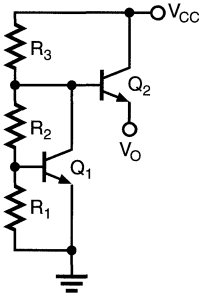


Figure 9. V_{BE} Multipled Regulator.
$V_{OUT} = V_{BE} * R2 / R1$

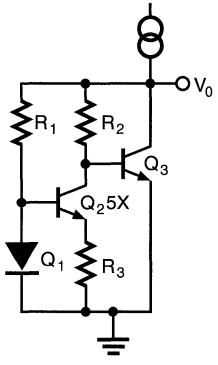


Figure 10. Widlar Band Gap Reference.
$\Delta V_{BE} = V(R3) = V_T * \ln (A2/A1)$
$V_{OUT} = V_{BE}(Q3) + (R2/R3) * \Delta V_{BE}$

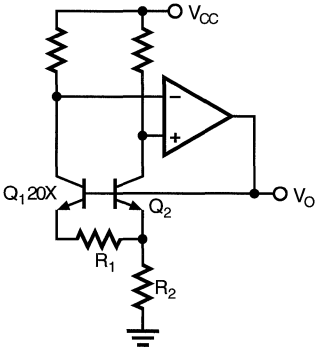


Figure 11. Brokaw Band Gap Reference.
$\Delta V_{BE} = V(R1) = V_T * \ln (A1/A2)$
$V_{OUT} = V_{BE}(Q2) + V(R1) * 2 * R2/R1$

Functional Circuit Blocks

Flip-Flop

Here are two examples of flip-flop circuits.

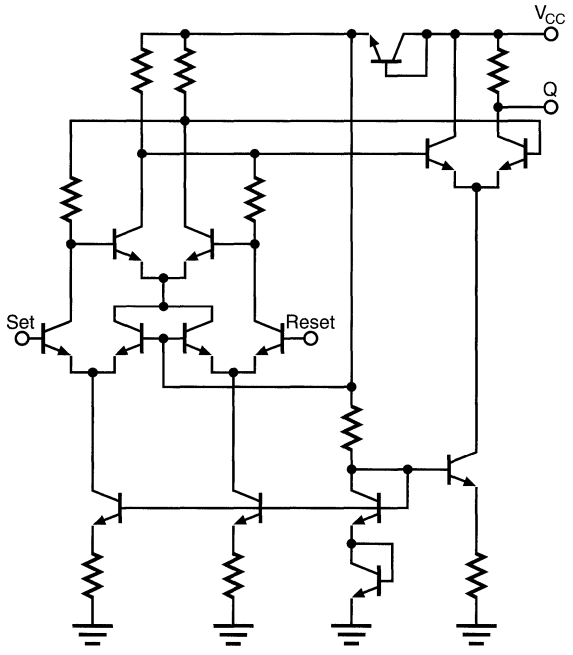


Figure 17. Fast, ECL Flip-Flop

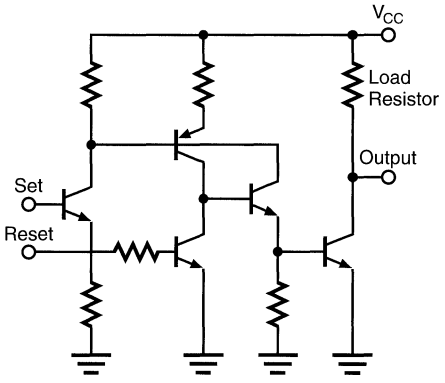


Figure 18. Four Layer Latch Flip-Flop

Functional Circuit Blocks

Trimming Schemes

There often arises the need to trim a parameter (i.e. voltage, current, oscillator frequency, offset null, etc.) to some particular value because of processing variations involved with wafer fabrication. We have developed two methods to accomplish this goal: 1) fuse link, where a fuse is blown to cause an open; and 2) zener zap, where a zener is taken well into breakdown until a short occurs.

Fuse Link

Fuse links can be used similar to zeners for trimming, but the fuses must be located on a bonding pad inside the pad cut because a fuse won't blow if there is passivation over it. One possible trim scheme using fuse links is shown below.

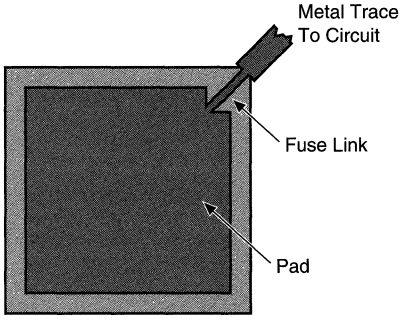


Figure 12.

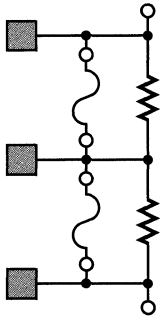


Figure 13.

Zener Zap

When using zener zap trim methods there are several points to keep in mind: the zener should be located near a pad, no cross-unders should be used to connect the zener with the pad, and the metal lines connecting the pad to the zener should be as thick as possible to allow the high current necessary to blow the zener. A few examples of the many possible trim schemes are shown in Figure 14, Figure 15 and Figure 16.

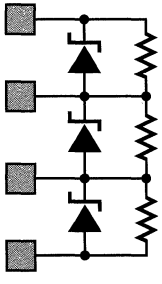


Figure 14. Simple Trim Setup with 8 Trim Steps.

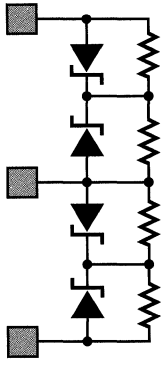


Figure 15. Trim Scheme Using Only 3 Pads to Get 16 Trim Steps.

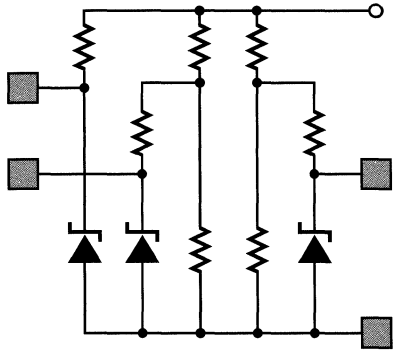


Figure 16. Parallel Trim Scheme with 8 Trim Steps.

Spice Models:

.MODEL Nmin NPN; Minimum NPN

+ (IS = 0.5FA BF = 200 NF = .995 VAF = 100 IKF = 20M NE = 1.45
+ EG = 1.185 BR = 5 NR = 0.98 VAR = 30 IKR = 2M XTB = 0.3
+ RB = 270 RC = 60 RE = 7 TRB1 = 1.5M XTI = 2.5
+ CJE = 450FF VJE = 0.85 MJE = 0.36 TF = 300PS
+ CJC = 200FF VJC = 0.57 MJC = 0.47
+ CJS = 1.4PF VJS = 0.31 MJS = 0.35)

.MODEL Plat LPNP; Lateral PNP

+ (IS = 0.9FA BF = 80 NF = 1 IKF = 60U NE = 1.5
+ EG = 1.2 BR = 30 NR = 0.98 IKR = 2M
+ RB = 30 RC = 200 RE = 15 TRC1 = 1.5M TRE1 = 1.5M
+ VAF = 45 VAR = 30
+ CJE = 150FF VJE = 0.57 MJE = 0.47 TF = 30NS
+ CJC = 950FF VJC = 0.57 MJC = 0.47 XTB = 0.5
+ CJS = 1.4PF VJS = 0.31 MJS = 0.35)

.MODEL Pvert LPNP; Vertical PNP

+ (IS = 0.9FA BF = 100 NF = .995 VAF = 45 IKF = 1.5M
+ EG = 1.22 BR = 30 NR = 0.98 VAR = 30 IKR = 2M NE = 1.25
+ RB = 350 RC = 200 RE = 300 TRC1 = 1.5M TRE1 = 1.5M
+ CJE = 150FF VJE = 0.57 MJE = 0.47 TF = 30NS
+ CJC = 1.6PF VJC = 0.57 MJC = 0.47 XTB = 0.5)

.MODEL RBase RES; Base Resistor

+ (R = 1 TC1 = 2.1m TC2 = 7u)

.MODEL RImp RES; Implant Resistor

+ (R = 1.0 TC1 = 4m TC2 = 6u)

.MODEL RPinch RES; Pinch Resistor

+ (R = 1.0 TC1 = 7m)

.MODEL Dzener D;

+ (BV = 7.2V IBV = 1uA RS = 270 IS = .1fA)

Component Summary

Components Available (single tile):

Small NPN:	48
Dual collector PNP:	21
Vertical PNP	4
Power NPN	3
Diffused Resistors (total)	300 k
Pinch Resistors (3-terminal, 30k)	8
Cross-unders	13
Buses	6

Resistor Summary

Resistor Summary:

8 - Pinch Resistors
(30 k ± 50%, use at 5 V)
80 - Base String Resistors
Using full string lengths gives:
73 - 4 k
7 - 1.5 k
Using separate pieces of the strings gives:
67 - 500
63 - 1 k
43 - 2 k
30 - 4 k

Additional components and their resistances are as follows:

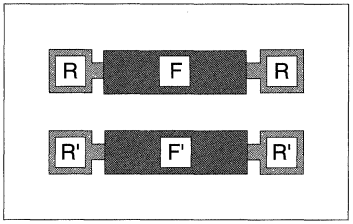
13 - Cross-unders (370 for full length, and 190 for half length)
6 - Buses (at 10 between connection points)

Design Rules

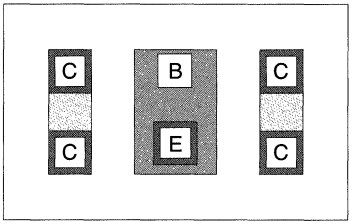
Design Rules:

- Minimum metal width = 8 microns
- Minimum spacing between metal traces = 8 microns
- Current capacity of metal trace = 4 mA per micron of width
- Metal line to pad (active) = 24 microns (note: metal resistance 0.02 per square)

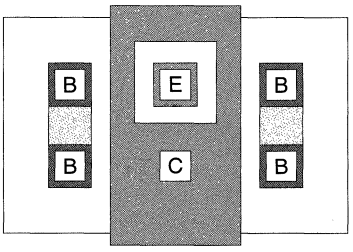
Device Layout



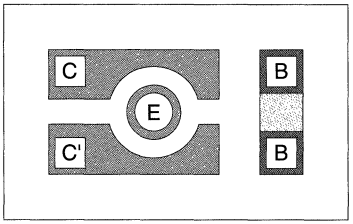
Pinch Resistor with Field Contact



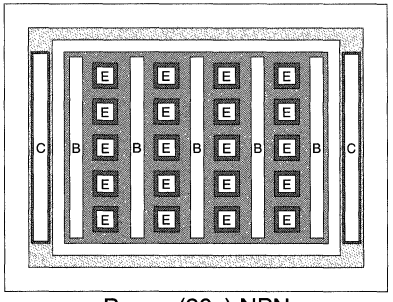
Minimum NPN



Vertical PNP

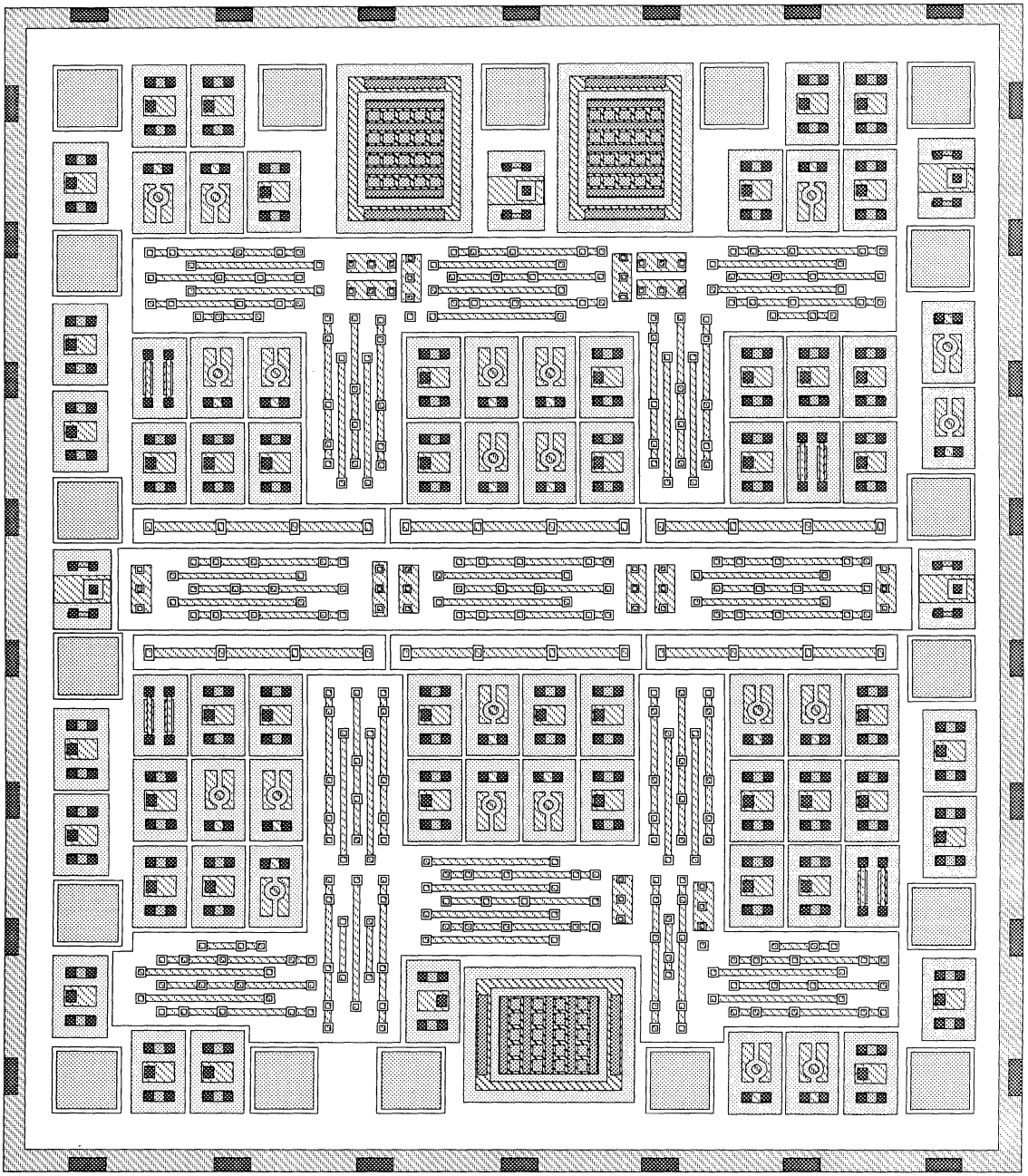


Lateral PNP with Split Collector



Power (20x) NPN

Device Layout



Notes

Application Notes

Product	Application Note
AS431	AN-1, AN-2
AS384X	AN-3, AN-4, AN-5

General Application Information

Steve Contreras

The ASTEC AS431 is a low-cost Precision Temperature Compensated Reference IC that is well-suited for many applications in linear and power electronics. A direct replacement for the industry standard TL431, this IC offers improved AC performance, near zero Temperature Coeficient (TC), trimmed 0.5% tolerance and is available in standard grades from 0 to 105° C and an extended temperature version, the AS1431, from –55 to 125° C.

When used with a minimum of external components, this device is ideal for a wide variety of applications including precision programmable voltage references, high speed amplifiers, comparators, linear series or shunt regulators, current sources or limiters, delay timers, voltage monitors, alarm circuits, and oscillators.

This application note demonstrates the versatility of the AS431 in typical applications and presents data useful for gaining a complete understanding of its application.

Figure 1 shows the schematic symbol and functional block diagram for the AS431. As indicated by the schematic symbol, the device can be thought of as a programmable zener diode. The functional block diagram, however, reveals a versatile IC consisting of a trimmed 2.5 V precision band gap reference, a high speed amplifier (Gain BW Product 3 MHz), ESD protection and a low impedance output stage. It is capable of shunting from 1 to 150 milliamps and has an output voltage range of 2.5 to 30 volts.

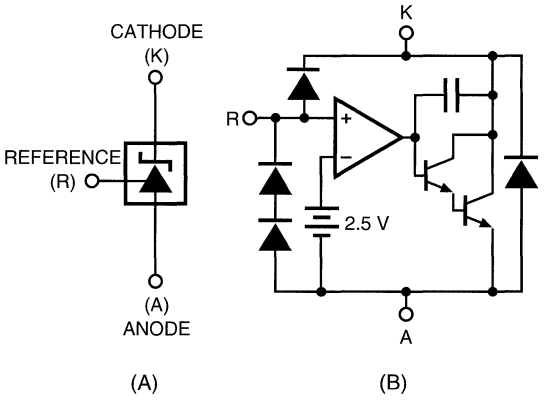


Figure 1. AS431 A) Schematic Symbol
B) Functional Block Diagram

Typical Applications

Precision Voltage Reference

The most common application of the AS431 is a precision temperature compensated voltage reference as shown in Figure 2. Note that only one external resistor is required for an output voltage equal to V_{REF}. For output voltages other than V_{REF}, a simple resistor divider network is used.

Fixed 2.5 Volt Reference

For an output voltage equal to V_{REF}, the reference input pin is connected directly to the cathode. A single resistor R is used to set the cathode current (I_K). The value of R will depend primarily on Vin and the characteristics of the load impedance that the circuit output will see (similar to selecting the series resistor for an ordinary zener

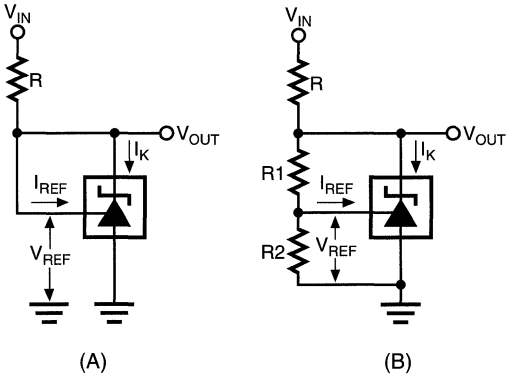


Figure 2. AS431 Precision Voltage Reference
A) Fixed B) Programmable

diode). Generally, R should be chosen to give about 10 mA of cathode current. This will keep the power dissipation low.

Example: Determine the value of R for V_{IN} = 20 volts.

The voltage across R is 20 – 2.5 = 17.5 V. For a desired I_K of 10 mA, R = 17.5/0.01 = 1.75 kΩ. Thus, an R of 1.8 kΩ will give an I_K of about 10 mA.

Programmable Output

To program the output to any desired value between V_{REF} and 30 volts, a simple resistor voltage divider is used as shown in Figure 2B.

V_{OUT} is determined by the formula:

$$V_{OUT} = V_{REF}\,(1 + R1/R2) + I_{REF} \bullet R1.$$

To ensure precise regulation, low TC precision 1% resistors should be used for R1 & R2. Its values should not be so low as to cause excessive power dissipation, nor too high that an error is introduced due to changes in I_{REF} over temperature (I_{REF} is typically 0.7 µA and deviates 0.4 µA over the full temperature range). A good compromise is to always keep R2 at around 2 to 5 kΩ and then select R1 to obtain the desired output voltage. The circuit can be made variable by using a potentiometer for R1.

The AS431 As An Error Amplifier

The AS431 can be used in both linear and switch mode power supplies as high gain error amplifier with a built-in temperature compensated voltage reference.

Linear Voltage Regulator

Figure 3 shows a simple linear voltage regulator. This circuit converts an unregulated DC source (rectified AC or battery) to a low-noise, low-ripple precision-regulated DC output. The output voltage can be set to any desired value between 2.5 to 28 volts, and the output current is limited only by the series pass element.

The high gain of the AS431 allows this circuit to achieve a line/load regulation of typically 0.03% or better, depending on the application.

Switch Mode Power Supply

The AS431 can be similarly used in switch mode power supplies as shown in Figure 4. The only difference is the AS431 does not control the

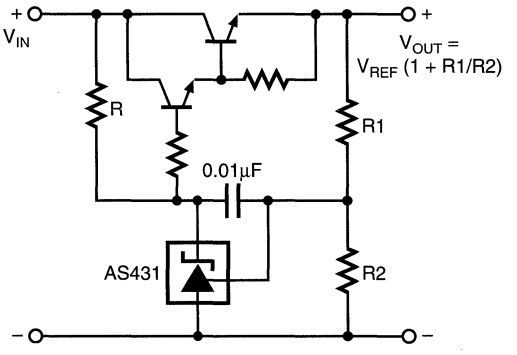


Figure 3. Linear Regulator Using the AS431 as a Reference/Error Amplifier

output voltage directly as in the linear regulator. Instead, it provides an amplified error signal to the PWM circuitry that in turn controls the on/off ratio of the switching device(s), thereby regulating the output voltage. Also, because of the phase shifts and delays associated with the modulator and filter components in switching power supplies, a more elaborate compensation network is required in the control loop to optimize the gain/phase characteristics of system. The network type and values are chosen so as to ensure stability and proper transient response.

Note that there are many different types of switching power supply topologies having different compensation, isolation and PWM configurations. The AS431 and associated circuitry, however, are essentially the same in all cases except for component values, the type of compensation network used and location (it may be located on the primary side in some applications).

The AS431 may also be used for other functions in a switch mode power supply. For example, it can be used as a reference or a comparator in the housekeeping, input/output monitoring, temperature control, or alarm circuitry. Or, as the reference/error amplifier in a MagAmp or linear auxiliary output regulator. Figure 6 illustrates several of these applications.

Frequency Compensation

Frequency compensation of a power supply control loop is achieved with an external compensation network, typically connected between the reference and cathode pins of the AS431. The type of network used can be as simple as a single capacitor, or as elaborate as a dual zero-pole pair network, depending on the power supply's topology. A typical single zero-pole pair compensation network is shown in Figures 4 and 5.

The AS431 typically has 55 dB of gain from DC to 6 kHz, where it rolls off at a 6 dB per octave rate, reaching 0 dB at 3 MHz. Further information characterizing the performance of the AS431 over frequency can be found in the AS431 Data Sheet. Due to the complexity of frequency compensation network design and the vast number of power supply topologies possible, a detailed discussion is beyond the scope of this application note. However, the information provided is useful in determining the compensation needed for a particular application.

The AS431 as a MagAmp Controller

Post regulation is required in many cases for one or more outputs of a switch-mode power supply. Linear regulators incorporating the AS431 are adequate for most low current outputs. When

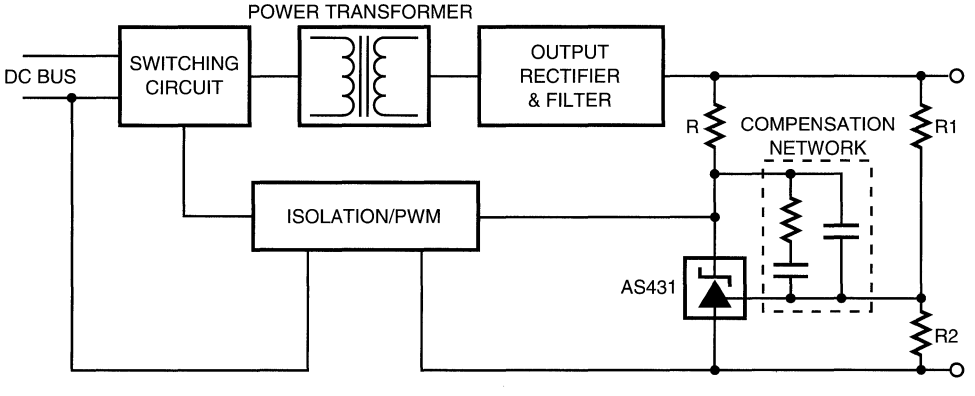


Figure 4. A Switch-Mode Power Supply Using the AS431 as a Reference/Error Amplifier

high current outputs are required, a MagAmp (saturable-core) regulator is usually used because of its high efficiency.

Generally speaking, a MagAmp is a pulse-width modulated buck regulator circuit that uses a saturable core inductor as the switching element. The inductor initially has a high inductance that blocks a pre-determined number of volt-seconds. Upon saturation, the inductor reverts to a very low impedance, which allows current to flow to the output with little loss. The number of volt-seconds blocked in each cycle is defined by the control circuitry and varies in accordance with changes in line and load, providing tight regulation at the output.

The AS431 is an ideal low-cost MagAmp controller, for it contains all the necessary control functions needed (precision reference, high gain error amplifier and an output stage) in a small package. A schematic diagram of a typical MagAmp post regulator using the AS431 is shown in Figure 5. Since this circuit constitutes a closed loop system, frequency compensation of the error amplifier is necessary.

Other Applications

The AS431 also can replace an ordinary zener diode in any circuit where a higher accuracy and temperature stability is required. Viewing the AS431 as a high gain transistor with a V_{BE} of 2.5 V increases usage possibilities. Applications for this device are limited only by the imagination.

Several practical applications are illustrated in Figure 6.

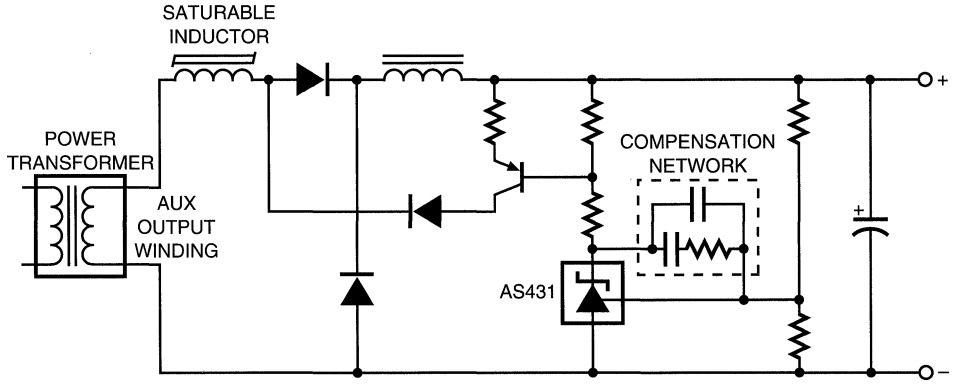


Figure 5. An AS431 Controlled MagAmp Post Regulator

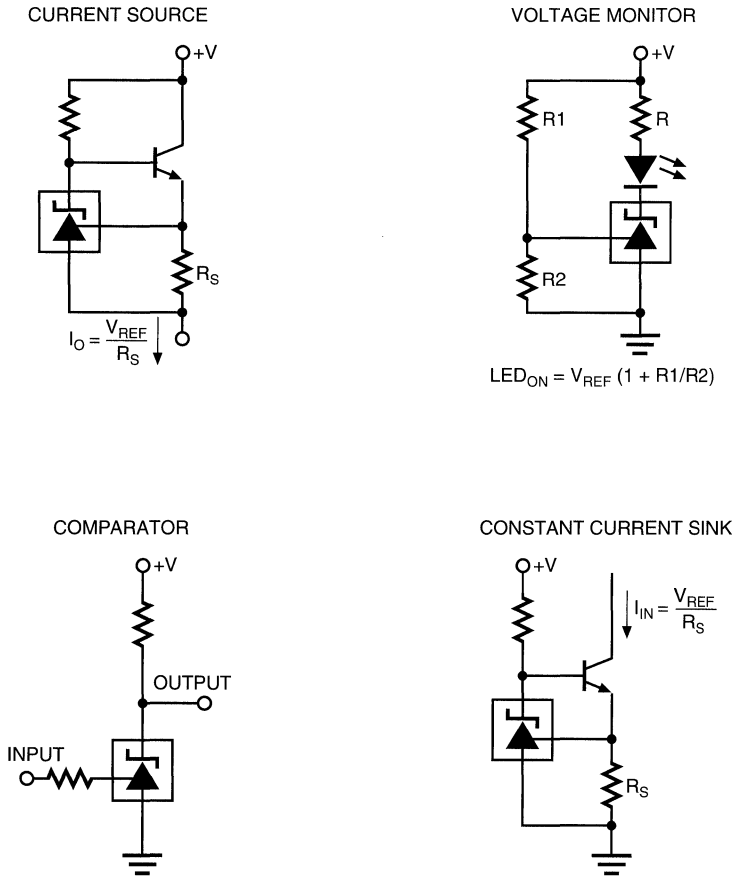


Figure 6. Typical AS431 Applications

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Notes

Secondary Side Error Amplifier Using the AS431

Mike Wong

I. Introduction

One of the most important safety regulations to which an off-line power supply must conform is input to output electrical isolation. This isolation requirement prevents the power supply control IC from directly sensing both the input line and output voltages. In the case of primary side control the output regulation information, an error voltage, must be transferred from the secondary side. This application note discusses a simple way of transmitting regulation information across the electrical isolation using an AS431 and a conventional 4N27 opto-coupler.

II. Power Supply Circuit

Figure 1 illustrates a simple flyback regulator. The AS3842, a low-cost current mode control IC, is configured to regulate the power supply from the primary side. The AS431 acts as a reference and a feedback error amplifier to sense the output voltage and generate a corresponding error voltage. This error voltage is then converted to an error current and coupled to the primary side through a 4N27 opto-coupler.

III. Opto-Coupler

Recently, opto-coupler manufacturers have made major improvements in opto-coupler processing and packaging technologies, resulting in tighter current transfer ratio (CTR) tolerances and better long-term reliability.

When designing the opto-coupler feedback circuitry, the designer should note the opto-coupler forward diode current. The forward diode current sets the device's CTR and effects the long-term reliability of the device. Similar to a lamp filament,

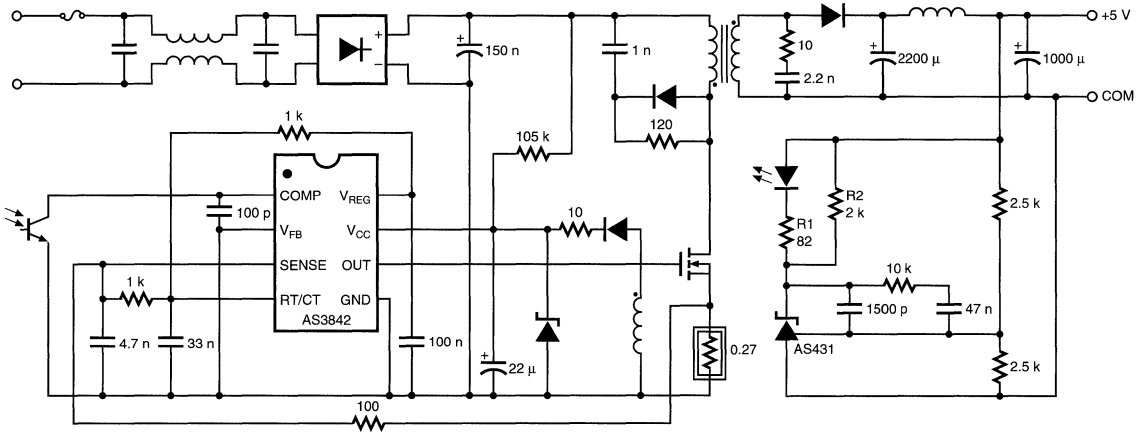


Figure 1. A 40W Flyback Power Regulator

the opto-coupler diode can be worn out or degraded more quickly if it is subjected to higher current. Also, the opto-coupler's unity gain bandwidth increases with forward diode current. The modulation of the gain bandwidth is caused by variations in the transconductance of the output transistor. In addition, the Miller capacitor from the base to collector of the output transistor damps out the effects of the opto-coupler's gain variance. A properly designed opto-coupler circuit not only increases long-term reliability of the regulator but also ensures a superior loop response.

IV. Design Example

Figure 2 shows the amplifier feedback section of the flyback power supply. To keep the 5 V output regulated, the V_{COMP} voltage must track the output voltage. The output voltage is first divided down by two 2.5 kΩ resistors, and its result is fed into an AS431 error amplifier network. The error amplifier output, $V_{CATHODE}$, is then converted to a proportional opto-coupler diode current. The opto-coupler bridges the isolation barrier and generates an output collector current proportional to the input diode current. Since the opto-coupler output is connected to the V_{COMP} pin, the opto-coupler output current is the I_{COMP} source current. In a normal operating condition, a higher output voltage causes $V_{CATHODE}$ to drop and results in a high diode current and I_{COMP} source current and consequently a lower V_{COMP}. A lower V_{COMP} decreases the PWM duty cycle and therefore decreases the regulator output voltage. The result is a regulated output. A determination of the opto-coupler diode operating current and small signal loop gain follows.

IVa. Opto-Coupler Operating Current

This design example shows the diode operating current as determined by the maximum I_{COMP} source current. In order for V_{COMP} to decrease linearly with increasing I_{COMP} source current, I_{COMP} has to operate in a linear region slightly above the maximum I_{COMP} source current. The linear region is depicted in Figure 3.

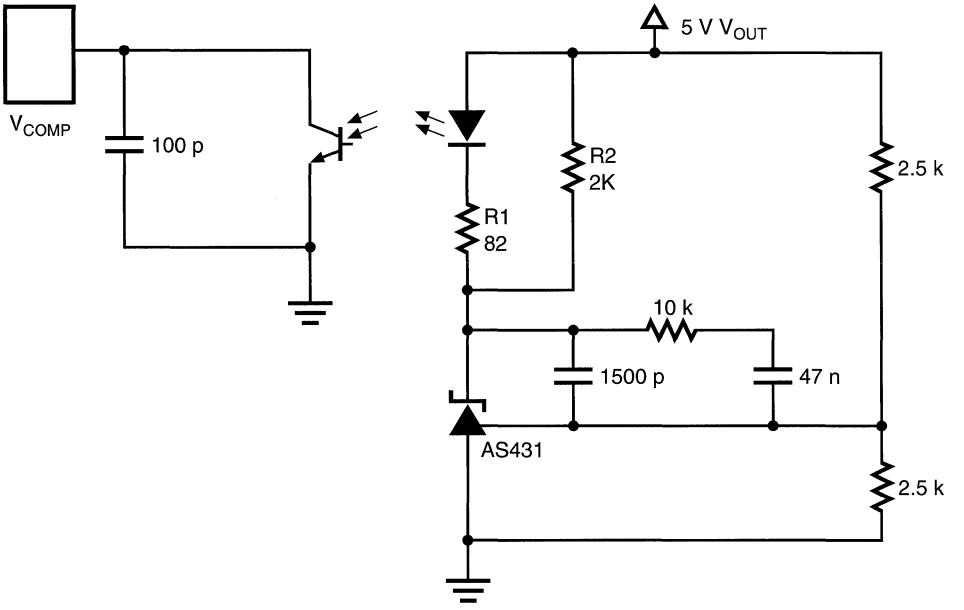


Figure 2.

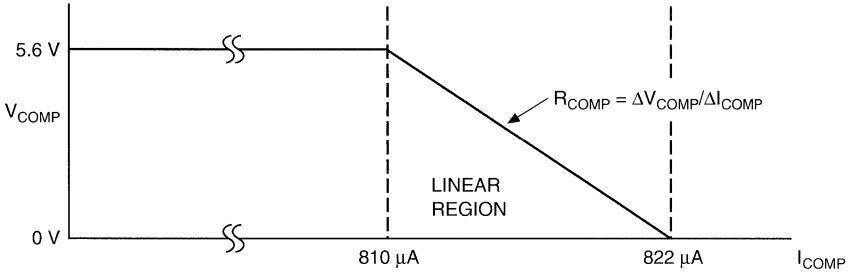
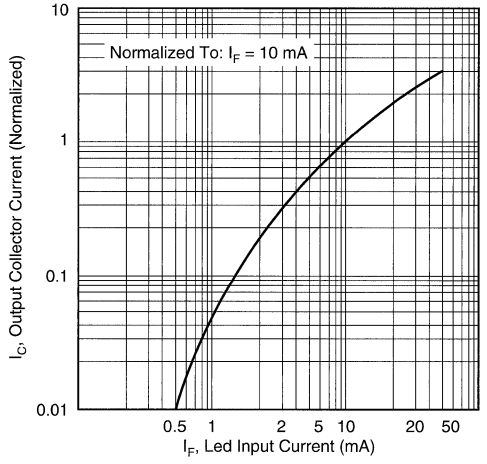


Figure 3. V_{COMP} vs I_{COMP}

Since the I_{COMP} source current is equal to the opto-coupler output current, the opto-coupler output current also modulates in the same I_{COMP} linear region. With a known opto-coupler output current, the input diode current, I_{DIODE}, can then be obtained from the output current versus diode current curve on the opto-coupler data sheet. Figure 4 illustrates the output current versus diode current curve of the 4N27 opto-coupler. The 4N27 data sheet guarantees a minimum of 0.1 CTR at 10 mA diode current.



The typical AS3842 maximum I_{COMP} source current is 800 µA. Using Figure 4, and assuming 0.1 CTR at 10 mA diode current, the forward diode current required to generate 800 µA of opto-coupler current is 8 mA.

IVb. AC Gain Analysis

Once the opto-coupler diode current is determined, the current limiting resistor R1 of Figure 2 can then be chosen to guarantee good output regulations and proper dynamic loop response. The AS431 cathode voltage, $V_{CATHODE}$, is a function of the diode operating current, I_{DIODE}, and the value of R1. Also, $V_{CATHODE}$ must be greater than 2.5 V for proper operation.

$$V_K = V_O - V_D - (I_D \cdot R1) > 2.5\ V \qquad (1)$$
$$= 5.0\ V - 1.2\ V - (8\ mA \cdot R1) > 2.5\ V$$
$$= 3.8 - (8\ mA \cdot R1) > 2.5\ V$$
$$R1 < 162\ \Omega$$
$$= 82\ \Omega\ (chosen)$$
$$V_K = 3.14\ V$$

R1 also plays a significant role in controlling the open loop gain of the power supply. The following equations derive the small signal AC gain from $V_{CATHODE}$ to V_{COMP}.

$$I_{COMP} = I_D \cdot CTR \qquad (2)$$
$$= \frac{(V_O - V_K)}{R1} \cdot CTR$$
$$\frac{\Delta I_{COMP}}{\Delta V_K} = -\frac{CTR}{R1} \qquad (3)$$

At the steady state condition, V_{COMP} is in the linear region,

$$\frac{\Delta V_{COMP}}{\Delta V_K} = \frac{\Delta I_{COMP}}{\Delta V_K} \cdot \frac{\Delta V_{COMP}}{\Delta I_{COMP}} = \frac{CTR}{R1} \cdot R_{COMP} \quad (4)$$

From figure 3:

$$R_{COMP} = \frac{\Delta V_{COMP}}{\Delta I_{COMP}} = \frac{5.6\ V}{(822 - 810)\ \mu A} = 509\ k\Omega$$

Applying equation (4):

$$\frac{\Delta V_{COMP}}{\Delta V_K} = \frac{0.1}{82\ \Omega} \cdot (509\ k\Omega) = 620 = 55.9\ dB$$

IVc. Other Considerations

R2, a 2 k resistor in parallel with the opto-coupler diode and R1, provides the minimum cathode current required to keep the AS431 operating when a minimum opto-coupler diode current is required. In addition, a small filter capacitor is placed close to the V_{COMP} pin of the control IC to attenuate high frequency switching noise being picked up by the metal trace from the opto-coupler to the control IC. Since the location of the pole in the opto-coupler small signal response varies significantly with the dc operating point of the opto-coupler, a resistor can be added from the V_{REG} to V_{COMP} pin to supply additional bias current to stabilize the loop.

Noise and Stability Considerations Using the AS384x

Mike Wong

I. Introduction

The AS384x product series is a state-of-the-art power supply controller designed with high-performance circuit techniques to improve speed and accuracy. Care is required to make effective use of this product's high speed and accuracy, because noise sensitivity is an inherent consequence of peak current mode control. This can lead to jitter at the output of the IC and periodic oscillations on the output of the power supply.

II. Peak Current Mode Control

Current mode control offers several significant advantages over voltage mode control. These include automatic input voltage feed-forward, pulse-by-pulse current limiting, and lower circuit complexity.

Current mode control uses two control loops, a current loop and a voltage loop. Figure 1 shows a simplified current mode controlled buck converter.

When the FET is turned on, current through the transformer, which is proportional to the output inductor current, is sensed with the current sense resistor (R_{SENSE} in Figure 1). When the voltage level across R_{SENSE} reaches V_{ERROR} (a function of the output voltage) the FET is switched off. Figure 2 illustrates the waveforms of the current mode converter shown below.

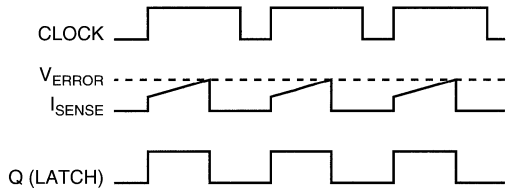


Figure 2.

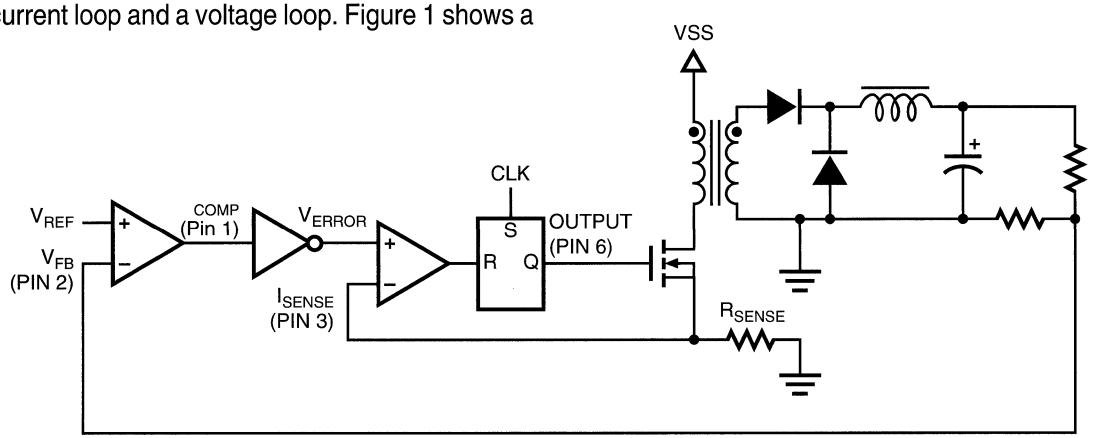


Figure 1.

III. Noise and Stability Considerations

The clock, error amplifier, current sense comparator, and RS latch are incorporated into the 384x family of IC's. Comp is the error amplifier output (pin 1). Comp is level shifted and attenuated to create the internal signal, V_{ERROR}. V_{FB} is the error amplifier feedback input that senses the converter's output voltage (pin 2). I_{SENSE} is the current sense comparator input (pin 3). Below is a pin-by-pin description of how noise can be injected into the control loops and the 384x.

A. Pin 1: Comp [error amplifier output]

The Comp pin in the 384x, is typically used to provide feedback loop compensation for the error amplifier. If no external signal is applied to this pin and the loop compensation network is laid out close to the control IC, this pin will not experience noise problems. However, if the power supply is controlled on the primary side and the V_{ERROR} signal is created by an AS431-2.5V Reference IC coupled across the isolation through an optical coupler, and fed directly into the 384x's Comp pin, a decoupling capacitor is recommended between the Comp pin and ground. The purpose of this capacitor is to filter any noise picked-up from the output of the AS431. Extreme care must be taken in selecting this decoupling capacitor because an excessively large capacitor creates an extra pole into the voltage control loop, which can lead to instability problems. In a power supply with proper lay-out and compensation, this decoupling capacitor may be avoided.

B. Pin 2: V_{FB} [inverting input of the error amplifier]

The signal to this pin comes from a divided voltage in the power supply output. Noise seldom enters into the control loop through this pin, since the error amplifier's compensation network is a low pass filter with a very low corner frequency (1/3 of the switching frequency). This network filters out any noise on the V_{FB} pin.

C. Pin 3: I_{SENSE} [current sense input for the PWM comparator]

The signal to this pin is usually a voltage level proportional to the output inductor current. The 384x output gate drive pulse is terminated when the voltage at I_{SENSE} reaches V_{ERROR}. Most noise-related problems can be traced directly to this pin. One can generally categorize these problems into four groups: leading edge current spike on the current sense waveform, periodic oscillation or noise on the current sense waveform, peak to average current error, and instability caused by greater than 50% duty cycle.

IV. Noise Characteristics Related to Current Sense

A. Leading Edge Current Sense Spike

During the transient when the MOSFET is being switched on, an instantaneous voltage is induced across the power transformer to generate a high surge current through the power MOSFET to ground. This surge current creates a leading edge voltage spike as shown in Figure 3.

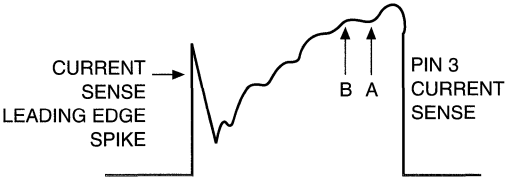


Figure 3.

A low pass RC filter is usually placed in-between the R_{SENSE} resistor and the I_{SENSE} pin to damp out the leading edge voltage spike. Reducing the leakage inductance of the transformer or placing a small series damping resistor from the output of the IC to the gate of the MOSFET are other ways of decreasing the magnitude of the current sense spike.

B. Periodic Oscillation on the Current Sense Waveform

By examining the current sense signal carefully (Figure 3), a high frequency ringing can be seen superimposed on the current sense ramp. This ringing is caused from parasitic elements in the current sense loop and also from noise being coupled across the leading edge low pass filter capacitor. Because manufacturers of the 384x have different current sense comparator circuitry and wafer processes, their comparator bandwidths can be quite different. As a result, one manufacturer's 384x may be more "noise sensitive" than another. For example, in Figure 3, the 384x's output is set to turn off at point A but because of its wide bandwidth, the 384x can be false-triggered at point B. As a result, the duty cycle is reduced prematurely and results in jitter and instability problems. However, if the IC's comparator bandwidth is smaller than the frequency of the ringing oscillation, the ringing is ignored or filtered out by the IC.

If a 384x's current sense comparator bandwidth is larger than the ringing frequency, the effects of the ring can be minimized by increasing the voltage ramp of the slope compensation. (Slope compensation is discussed extensively in section V.) The purpose of increasing slope compensation is to improve the current sense signal to noise ratio, or the ratio of the magnitude of the current ramp to the magnitude of the ringing.

C. Peak vs. Average Current Error

Current mode control regulates the peak inductor current, but the converter's output current corresponds to the average inductor current. Figure 4a shows the output current (average inductor current) increases as the duty cycle increases. Consequently, the line regulation is degraded because the converter delivers different amounts of current at different line conditions (Duty Cycle = V_{OUT}/V_{IN}). Figure 4b and 4c illustrate how this problem can be corrected with slope compensation.

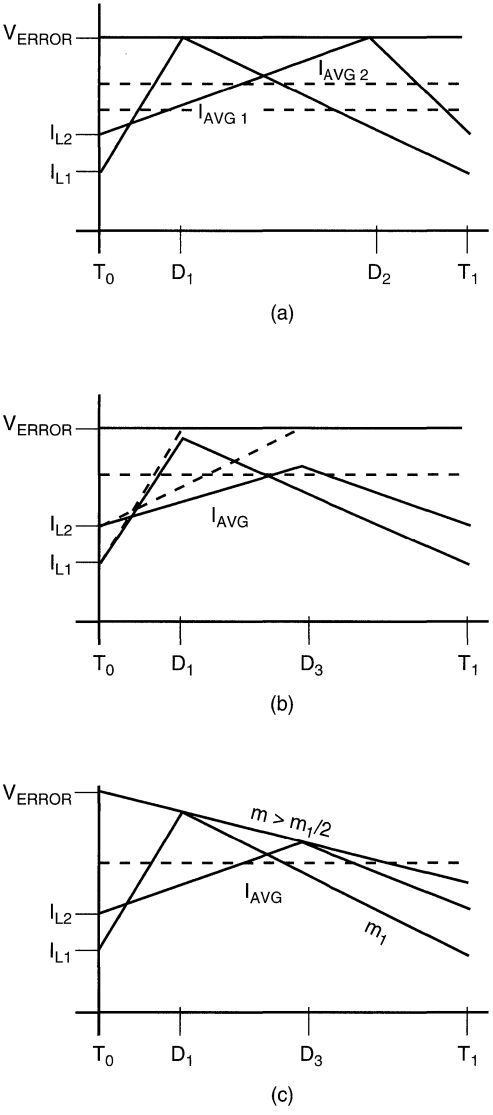


Figure 4.

Figure 4a shows the average inductor current ($I_{AVG\,1}$ and $I_{AVG\,2}$) in dashed lines changes as the duty ratio (D1 and D2) changes. The triangles formed by solid lines represent the actual inductor currents ($I_{L\,1}$ and $I_{L\,2}$) at different duty ratios (D1 and D2), and the areas under the triangles are their average currents.

Figure 4b shows that if an additional voltage ramp is introduced onto the current sense ramp to elevate the current sense ramp and allows it to reach V_{ERROR} early, a controlled premature gate drive turn off can be created (D3<D2). The dashed line is a combination of the inductor current ramp and a constant voltage ramp. (Section V describes how the oscillator ramp can be used as the voltage ramp by placing a resistor from the oscillator pin to the current sense pin.) The dashed lines are the actual current sense waveforms seen by pin 3 of the IC. The same area is obtained under the triangles, which indicates the same average output current is generated.

Figure 4c shows the peaks of the inductor currents can be connected by a straight line. The slope of this line becomes the slope of our slope compensation that normally should be set at greater than half of the down slope of the inductor current (m m1/2).

D. Instability caused by greater than 50% duty cycle

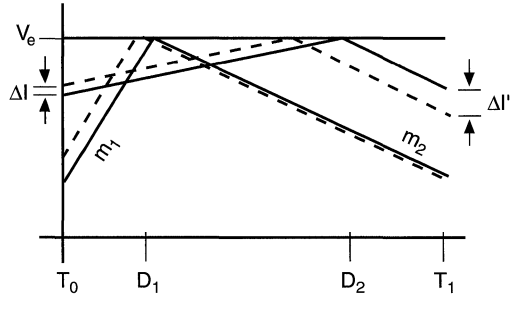
Figure 5a depicts how a small perturbation in the inductor current is amplified when the duty cycle is greater than 50%. The perturbation in the operating point is greater at the end of a given cycle than at the beginning and is opposite in sense. Rather than converging to find value after a number of cycles, the operating point oscillates between two diverging values, giving a half switching frequency oscillation. As shown in Figure 5b, slope compensation again can be used to attenuate the error caused by the perturbation.

V. Implementation of Slope Compensation

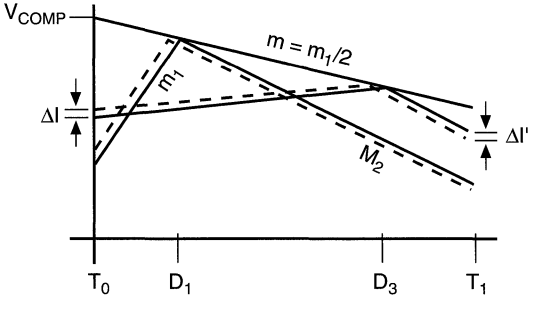
Slope compensation is usually implemented with an additional resistor, R_{SLOPE}, placed between pin 3 and pin 4 of the IC, as shown in Figure 6a. The magnitude of the slope is determined by R_{SLOPE} and R1, the resistor for the low pass filter. Generally, the slope is set at greater than half of the down slope of the inductor current (Slope m1 / 2). A small parallel capacitor, C_{SLOPE} in Figure 6a, is suggested to enhance operation at minimum duty cycle and light loads. In some cases, the addition of R_{SLOPE} may affect the oscillator frequency and duty cycle. Another slope compensation circuit (Figure 6b) is suggested to avoid the frequency shift problem. In Figure 6b, a voltage ramp with positive slope is generated by R_{SLOPE} charging C_{SLOPE} when the output is turned on. This voltage ramp is added onto the current sense waveform through Rb, a buffer resistor. Another advantage of this slope compensation circuit is that the slope can be easily adjusted by changing R_{SLOPE} or C_{SLOPE}.

VI. AS384x

The Astec 384x is designed to provide a number of improvements over the competitor's standard UC384x. Some of the improvements are guaranteed oscillator discharge current, reduced current



(a)



(b)

Figure 5.

sense to output delay (for high frequency operations), and an exact 50% duty cycle clamp for the AS3844/5. However, a couple of simple design considerations allows the improved AS384x to be used identically to the designs of other manufacturers.

A. Slope Compensation With the AS3844/5

In order to guarantee a true 50% duty cycle output clamp, the AS3844/5 is implemented with an alternate "on" cycle scheme. The output of the IC is latched "on" at the peak of the oscillator and turned "off" when the oscillator reaches its next peak. This is illustrated in Figure 7. If the slope compensation is implemented with the scheme shown in Figure 6a (with a resistor going from the oscillator pin to the current sense input), the down slope of the oscillator can be superimposed onto the current sense waveform. This creates a false high signal that can prematurely turn off the gate drive output. Figure 7 illustrates all the associated waveforms.

One of the simplest ways to implement slope compensation and avoid the current sense false trigger problems is illustrated in Figure 6b and described in Section V.

B. Bandwidth of the AS384x

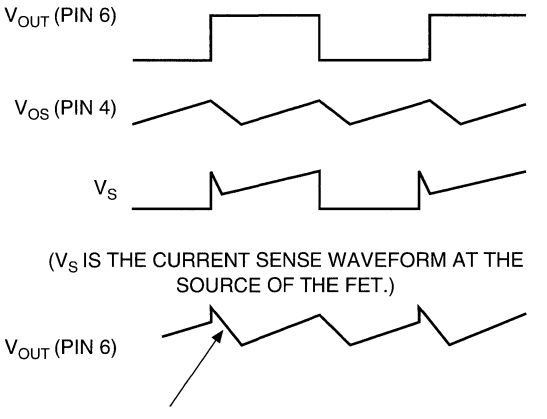


Figure 7.

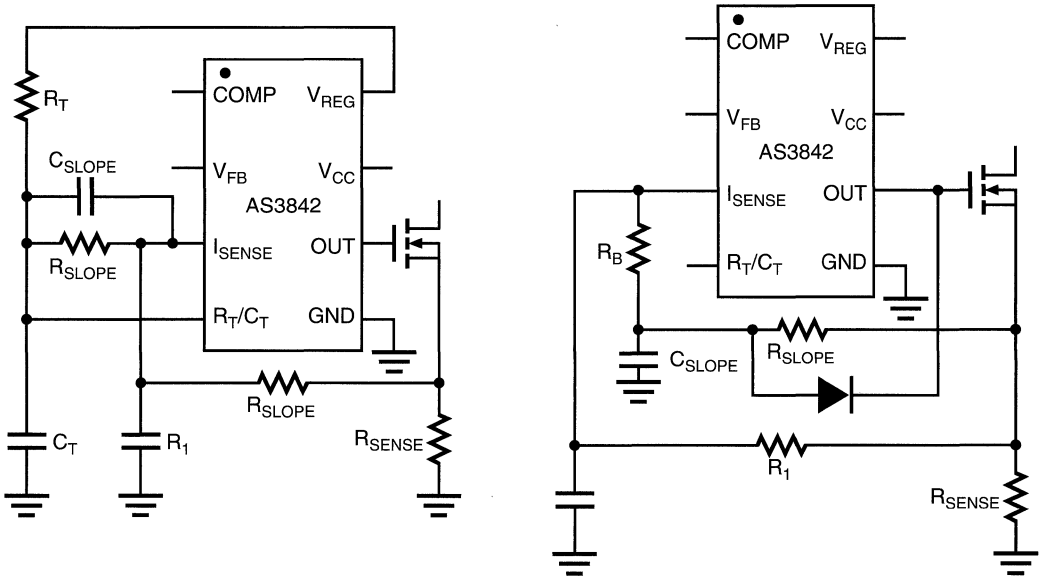


Figure 6.

Since the AS384x is designed for high switching frequency operations, the current sense to output delay time is reduced and the bandwidth of the current sense comparator increased to ensure the converter senses and responds to signals at switching frequencies above 500KHz. As explained previously in Section IV B, an IC with a wide current sense comparator bandwidth is more susceptible to noise. If a fast current loop is not required in the application, the frequency response (or the cross over frequency) of the current loop can be reduced. With increased slope compensation and a slower current loop, the AS384x functions the same as other 384x's.

VII. Circuit Layout

Incorrect layout can cause severe noise problems that cannot be corrected by slope compensation or decoupling. The following is a list of some common layout rules that will help to ensure a noise-free environment for proper operation of the control circuit.

1) Keep all trace and lead lengths to a minimum.
2) Separate the power ground and signal ground.
3) Use ground planes.
4) Keep decoupling capacitors close to the IC.
5) Locate IC and control circuits away from the power devices.
6) Avoid large loops.

This bulletin is intended not to explain the specification differences such as tighter parameter distributions or wider temperature range. At issue, however, are the differences that might be seen in a given power supply when a UC384x is replaced by an AS384x, or vice versa.

Whether or not one part performs "better" is not always at question. What is at issue are differences that may make a power supply optimized with one family of parts and non-optimal with the other. Although many of the minor differences appear only in unusual circumstances, designers must be able to predict when their "unconventional" design techniques may inadvertently expose a significant difference in the behavior of the control chip.

I. Reference

A difference exists between the start-up characteristic of the Astec parts compared with many competitors' parts. On many merchant market 384x chips, a turn-on overshoot is visible, which may reach 6V at its peak. This overshoot is usually very fast, typically less than half a volt, and is a function of load capacitance. The Astec part is much improved in this respect.

II. Oscillator

A. Frequency/ Duty Cycle Drift

There is a small oscillator drift over temperature that is common to all Astec parts but different than most competitive parts. The Astec part is optimized to provide a much improved duty cycle programming stability over temperature. This is at the expense of slightly higher frequency drift over temperature, though this drift is significantly smaller than allowed by specification. In typical applications, a drift in frequency is of much less concern than a varying maximum duty cycle.

B. Synchronization

Synchronization is generally not used in the power supplies typical of 384x designs, but the Astec AS384x parts are designed to transcend this low-cost/low performance distinction. An additional block of circuitry has been added to allow for external clocking and direct duty cycle control. This feature allows the use of an external digital clock that is in phase with the desired output. Our built-in clocking function makes driving the oscillator from an external logic source easier, but the addition of the low voltage sync threshold could cause incompatibility with some design techniques occasionally used with the UC384x.

Any circuit forcing the R_T/C_T pin to ground may behave differently when the AS384x is substituted for a UC series part. In particular, there are some methods of forcing a UC384x series part to synchronize to an external clock that may be problematic with an AS384x. When it is desired to synchronize using the lowest cost part, there are several schemes for synchronizing that perform equally well for both UC384x parts and for the AS384x. These schemes share a general requirement that the sync/oscillator waveform never drops below 1 V. These schemes are recommended as they allow the circuit design to migrate to an AS284x with a minimum of compatibility problems.

C. Very Low C_T Values

On our test jigs, we see occasional problems when trying to achieve high frequencies (>200 kHz) with very small capacitor values. Essentially, a small cap with a high value resistor can excite a poorly damped resonance using the inductance of the interconnect (or of the cap).

This is more a problem on the AS384x than the UC384x. If the resonant network rings below about 0.6V, it can trigger our sync circuit, causing some unusual behavior in the oscillator. As with most high frequency problems, careful layout and appropriate component selection are the solution to the problem. Several 500 kHz schemes, both with and without external clocks, have been successfully implemented. As a general rule, avoid R_T values in excess of 10k when using the AS384x unless the layout is well controlled.

III. Error Amplifier

A. Speed

The gain bandwidth of the op amp of the Astec parts is slightly higher than most competitor's parts (1.2 versus 1.0 MHz). Because of the use of junction capacitors as the compensation cap in the industry standard design, most competitive vendors' parts are far less controlled than Astec's (we use a cap with a glass dielectric and a metal top plate). In essence, we control our gain-bandwidth to be consistently where competitors occassionally find themselves with best-case parameter distributions.

B. Noise

Coming from a divider off of the 5V regulator, the internal 2.5V reference in the 3842 reflects the noise on that supply. Because of our improved regulator design and the use of ECL- type logic with low noise injection, there is far less noise on this reference point. Noise at this point effectively gets amplified to the COMP pin as a function of the external compensation network. Since any synchronous noise there effectively adds to or cancels some of the systems "slope" information, the rate of change of the noise at the time of the current sense amplifier switching event is a contributor to overall system gain.

Although it is arguable that no noise should be injected, the fact we have less noise is equivalent to having different noise, and may either improve or degrade a supply's loop stability (Certainly having less noise makes the system more predictable and less dependent on empirical tweaking).

C. Reference Accuracy

Although it may appear to be primarily a specification issue, the AS384x has a significant improvement in the accuracy of the specification of the 2.5V reference at the V_{FB} input. Whereas the original designers of the UC3842 designed a 5V reference trimmed to 1% and then used a well matched divider to divide it down to 2.5V, ASD has found the original scheme to have unacceptable tolerances. Instead, all ASD parts are trimmed for1% precision at the 2.5 V reference input, and all additional tolerances are controlled to allow the 5V reference to remain within its usual specification for precision.

IV. Housekeeping

A. Turn-Off Behavior

Because of our multiple-redundant shut-off feature, ASD is currently seeing a benign but unexpected phenomenon at the turn-off threshold. If a noise-free DC supply is used to put the V_{CC} within about 10-30 mV of the threshold, as the part is about to shut off, there is an observed increase in the turn-on delay of the output stage. This is a result of the output blanking circuitry being prematurely turned on into a linear range as the UVLO comparator hits its threshold. The turn-off delay is not degraded, and therefore full

control is maintained, but at a slightly reduced maximum duty cycle. This doesn't affect supply hold-up time, as this phenomenon happens only when in the region where supply shutdown is guaranteed.

C. Overtemp Shutdown

Unlike parts from other vendors, ASD limits the absolute maximum die temperature to about 135° C. This is done by disabling the oscillator. The 5V regulator, op amp, etc. remain biased on, as is the logic and output stage. Note: Since all circuits remain active after shutdown, but with a zero frequency oscillator, there can be an unusual waveform in DC testing. The output can go high during the final cycle, and awaits a termination signal from either the oscillator or the current sense amp. This may give the erroneous indication that the output "goes high" at shutdown. In fact, the PWM latch is still operative, and the normal termination of this cycle by the current sense comparator latches the output low until the overtemp condition is rectified. (Normally by the power being cycled, although if kept biased, the chip restarts after cooling down through a nominal temperature hysteresis band.)

V. Logic

A. Propagation Delay

From the current sense input to the output, the propagation delay in the AS384x is actually half the value of the UC384x (75–85 ns compared to 150–180 ns). This is arguably a great advantage, giving better control and significantly better protection from fault conditions, including core saturation. On the other hand, the AS384x comparator and logic sees a 50 ns noise spike as a significant event, whereas the UC384x may ignore it altogether.

Both the AS284x and AS384x series parts use common mode logic (ECL) for high speed, low noise injection, and process insensitivity. This reduces noise sensitivity at the expense of some added propagation delay. The industry standard designs for the UC3842 family have similar propagation delays, but with those designs the delays are due to slow saturating RTL type logic and no effort is made to optimize the bandwidth of the current sense comparator.

B. AS3844/45 Flip-Flop Timing

The timing on the AS3844/5 is designed to guarantee a true 50% duty cycle, unlike the industry standard, which alternates simply both cycles and the oscillator discharge period.

We need to clarify, however, that the scheme actually guarantees less than 50% duty cycle. (50 kHz spec is 49% min, 50% max, actual is about 49.6%) There are asymmetrical logic delays in the system. In practice this causes the output pulse on the 3844 to be about 150 ns less than the expected 50%. This is a trivial error at 50 kHz, but at high frequencies it can become more of an issue.

VI. I/O Clamping

A. Input Clamping Removed

The inputs of the error amplifier and current sense comparator (pins 2 and 3) are rugged epi-base diodes. These provide very high voltage breakdown (typically 60-80 V) and non-degrading performance under stress. The circuit design is such that no odd behavior occurs, even under extreme overvoltage conditions, and the absolute Maximum Ratings on these pins are Rated at 30 V. Several vendors have "protected" these inputs with low voltage (5.8 V) zeners to ground. With proper device design, these structures are not necessary and instead add a new source for leakage and parametric drift.

B. Comp Clamp

The error amp output on the UC3842 is nominally specified to have an output clamping action at 5 V minimum, 6 V typical. This clamping is typically accomplished with a 5.8 V zener. Instead, the Astec part clamps the error amp to one diode drop above VREG, or about 5.6V. This eliminates concern about zener leakage or drift and improves the ESD ruggedness of the circuitry.

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SWITCHING POWER SUPPLY CONTROL LOOP DESIGN

Mike Wong

1. Introduction

In a switched mode power converter, the conduction time of the power switch is regulated according to the input and output voltages. Thus, a power converter is a self-contained control system in which the conduction time is modulated in reaction to changes in the input and output voltages. From a theoretical approach, control loop design often involves complicated equations, making control a challenging but often misunderstood area in switched mode power supply design. A simplified approach to feedback control loop analysis is presented in the following pages, beginning with a general overview of various parameters affecting performance in a switching power system. A demonstration of an actual power supply is given to show the components involved in designing the characteristics of the control loop. Test results and measurement techniques are also included.

2. Basic Control Loop Concepts

2.1 Transfer Functions and the Bode Plots

The transfer function of a system is defined as the output divided by the input. It consists of a gain and a phase element that can be plotted separately in a Bode plot. The gain around a closed loop system is the product of the gains of all the elements around the loop. In a Bode plot, the gain is plotted logarithmically. Since the product of two numbers is their logarithmic sum, their gains can be summed graphically. The phase of the system is the sum of all phase shifts around the loop.

2.2 Poles

Mathematically, in a transfer equation, a pole occurs when its denominator becomes zero. Graphically, a pole in the bode plot occurs when the slope of the gain decreases by 20 dB per decade. Figure 1 illustrates a low pass filter commonly used for creating a pole in the system. Its transfer function and Bode plots are also shown.

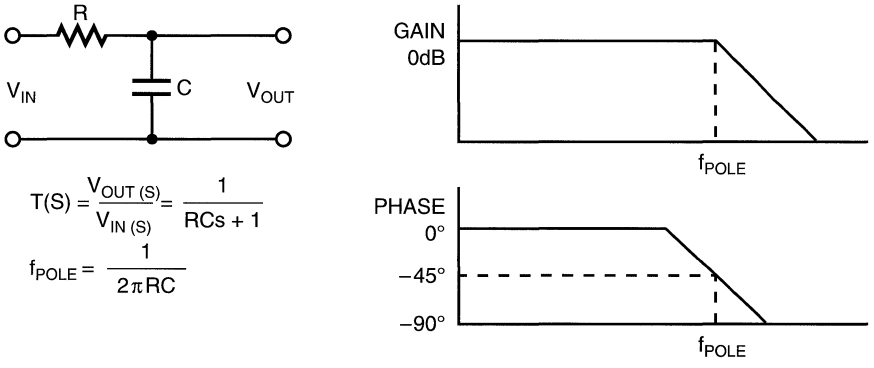
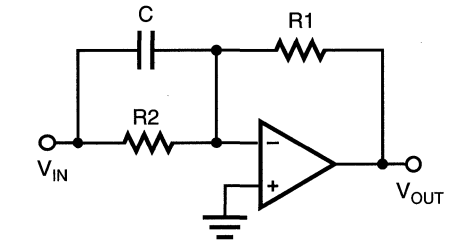


Figure 1.



$$T(S) = \frac{V_{OUT}(S)}{V_{IN}(S)} = \frac{-1}{\frac{1}{R1Cs} + \frac{R2}{R1}}$$

$$f_{ZERO} = \frac{1}{2\pi R2C}$$

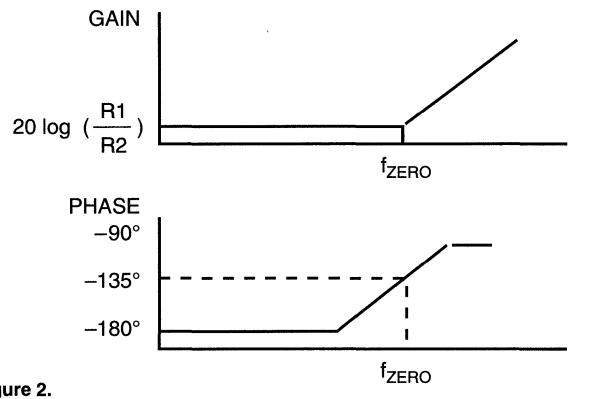


Figure 2.

2.3 Zeros

A zero in a frequency domain transfer function occurs when the numerator of the equation goes to zero. In a Bode plot, a zero occurs at a point where the slope of the gain increases by 20 dB per decade accompanied by 90° phase lead. A high pass filter circuit causing a zero is depicted in Figure 2.

There is a second type of zero, known as a right half plane zero, that causes phase lag instead of phase lead. A right half plane zero causes a 90° phase lag, accompanied by an increase in gain. Right half plane zeros are usually found in boost and buck-boost converters and so extra precaution should be taken during feedback compensation design so the crossover frequency of the system is well below the frequency of the right half plane zero. The Bode plot of a right half plane zero is shown below in Figure 3.

3.0 Ideal Gain-phase Plots for a Switching Mode Power Supply

A goal must be clearly defined prior to designing any control system. Generally, the goal is simply a Bode plot constructed to achieve the best system dynamic response, tightest line and load regulation, and greatest stability. An ideal closed loop Bode plot should possess three characteristics: sufficient phase margin, wide bandwidth, and high gain. A high phase margin damps oscillations and shortens the transient settling time. Wide bandwidth allows the power system to quickly respond to sudden line and load changes. A high gain ensures good line and load regulation.

3.1 Phase Margin

Referring to Figure 4, the phase margin is the amount of phase above 0° at the crossover frequency (f_{cs}). This is different from most control system textbooks that present a measuring phase margin from -180°. They include the negative feedback at DC that gives them 180° phase shift

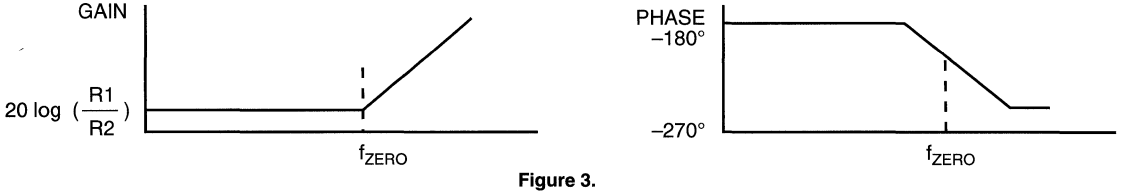


Figure 3.

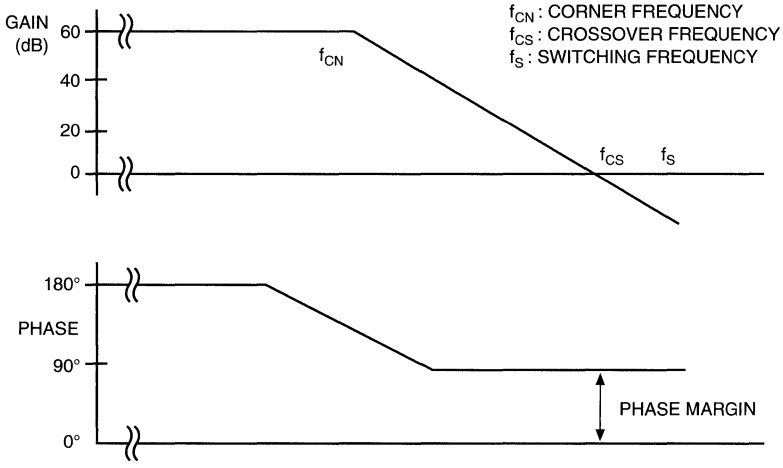


Figure 4.

at the beginning. In the actual measurement, the 180° phase shift is compensated at DC and enables the phase margin to be measured from 0°.

According to Nyquist's stability criterion, a system is stable when its phase margin exceeds 0°. However, a region of marginal stability exists where the system transient response oscillates and eventually damps out after a long settling time. A system is marginally stable if its phase margin is less than 45°. A phase margin above 45° provides the best dynamic response, short settling time and minimal amount of overshoot.

3.2 Gain-Bandwidth

The gain-bandwidth is the frequency at which the gain is unity. In Figure 4, the gain-bandwidth is the crossover frequency, f_{CS}. A major limiting factor of the maximum crossover frequency is the power supply switching frequency. According to sampling theory, if the sampling frequency is less than 2 times the frequency of the information, the information will not be properly read.

In a switched mode power supply, the switching frequency is seen in the output ripple, which is false information and must not be transmitted by the control loop. Therefore, the crossover frequency of the system must not exceed half the switching frequency. Otherwise, the switching noise, the ripple, distorts the desired information, the output voltage, causing the system to be unstable.

3.3 Gain

High system gain contributes significantly to ensuring good line and load regulation. It enables the PWM comparator to accurately change the power switch duty cycle in response to variants in the input and output voltage. Often, a tradeoff needs to be determined between higher gain and lower phase margin.

4. A Practical Design Analysis Example

Applying classical control loop analysis techniques, the control loop of a switching regulator is divided into four main stages, output filter, PWM circuit, error amplifier compensation, and feedback. Figure 5 illustrates a block diagram of the four stages and Figure 6 illustrates a power supply circuit diagram.

The output voltage is first divided down by the feedback network. The feedback voltage is then

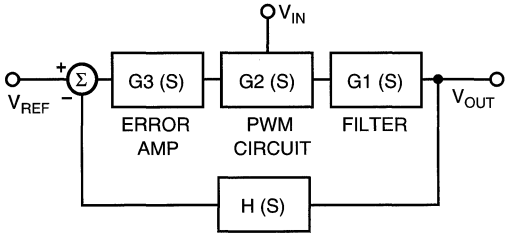


Figure 5.

fed into an error amplifier, which compares it with a reference level and generates an error voltage. The pulse width modulation stage takes the error voltage and compares with the power transformer current and converts it to the proper duty cycle to control the amount of power pulsing to the output stage. The output filter stage smoothes out the chopped voltage or current from the power transformer, completing the feedback control loop. The following determines gain and phase of each stage and combines them to form the system transfer function and the system gain and phase plots.

4.1 Feedback Network, H(s):

The feedback network divides the output voltage down to the reference level of the error amplifier. Its transfer equation is simply a resistor divider equation:

$$H(S) = \frac{R2}{R1 + R2} \quad (1)$$

4.2 Output Filter Stage, G1(s)

In a current mode control system, the output current is regulated to achieve the desired output voltage. The output filter stage converts the pulsating output current into the desired output voltage. Small signal analysis reveals that the ESR of the output capacitor and the feedback network resistors ($R_1 + R_2 = R_{FB}$) dictate the

$$R_{FB} = R1 + R2 \quad (2)$$

$$V_{OUT(S)} = I_{OUT(S)} \left[R_{FB} \parallel \left(\frac{1}{CS} + ESR \right) \right] \quad (3)$$

$$G1(S) = \frac{V_{OUT(S)}}{I_{OUT(S)}} = \frac{R_{FB}\,(1 + ESRCS)}{(R_{FB} + ESR)\,CS + 1} \quad (4)$$

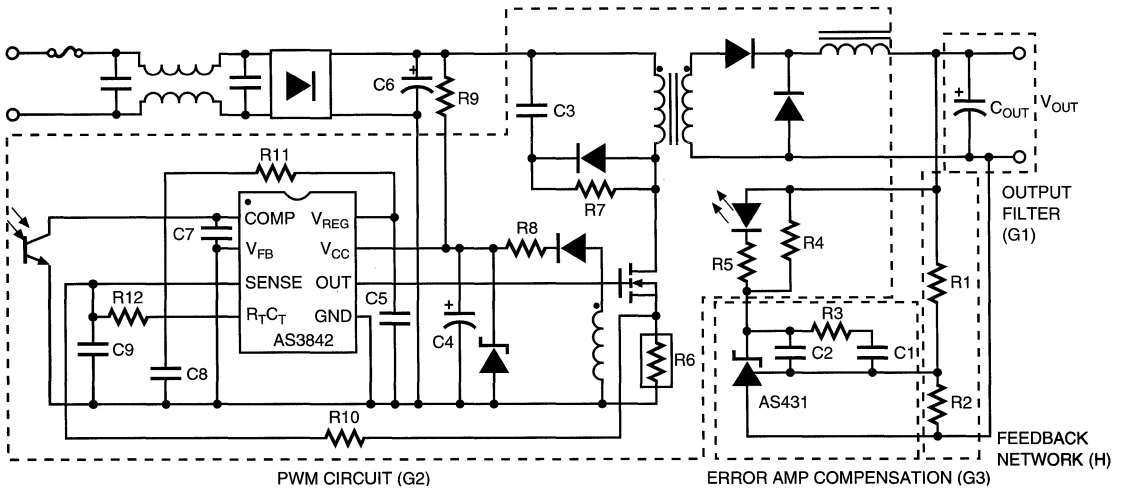


Figure 6.

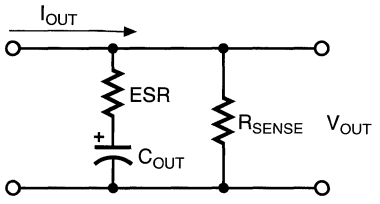


Figure 7.

characteristics of the output filter transfer function. The circuit analysis of Figure 7 demonstrates the effects of ESR and R_{SENSE}.

Transfer equation G1(s) shows an initial low frequency gain of R_{FB}. The gain starts to roll off at fpole = 1/2 (R_{FB}+ESR)C and levels off at f_{ZERO} = 1/2 ESRC. The Bode plots of G1(s) are shown in Figure 8.

4.3 PWM Circuit Stage, G2(s)

The optocoupler circuit transfers the error signal created by the error amplifier network to the primary side. The AS3842 PWM circuit compares the error voltage with current through primary side of the power transformer. The duty cycle of the power FET is then modulated to supply sufficient current to the secondary to maintain a desired output level.

The small signal transfer function of the optocoupler has a constant gain proportional to the current transfer ratio of the optocoupler, R6,a current limit resistor in series with the optocoupler diode, and the output impedance of the AS3842 error amplifier. This is discussed extensively in the application note "Secondary Error Amplifier with the AS431." The transfer function from the output of the error amplifier to the comp pin of the AS3842 is:

$$\frac{\Delta V_{COMP}}{\Delta V_{CATHODE}} = \frac{CTR}{R6} R_{COMP} \qquad (5)$$

$V_{CATHODE}$ is the cathode voltage of the AS431 and the output of the compensation error amplifier. CTR is the current transfer ratio of the optocoupler. R6 is the current limit resistor in series with the optocoupler diode. R_{COMP} is the output impedance of the AS3842 Comp pin when it tries to source above its maximum output current.

After the error signal is transferred to the compensation pin, it is compared with a current sense signal. Figure 9 shows a simplified block diagram of the current sense comparator and switching stages.

In a closed loop system V_{COMP} is maintained in the same level as I_{SENSE}; therefore, $I_{PRIMARY}$ is effectively regulated by V_{COMP}.

$$I_{PRIMARY} = \frac{V_{COMP}}{R_{SENSE}} \qquad (6)$$

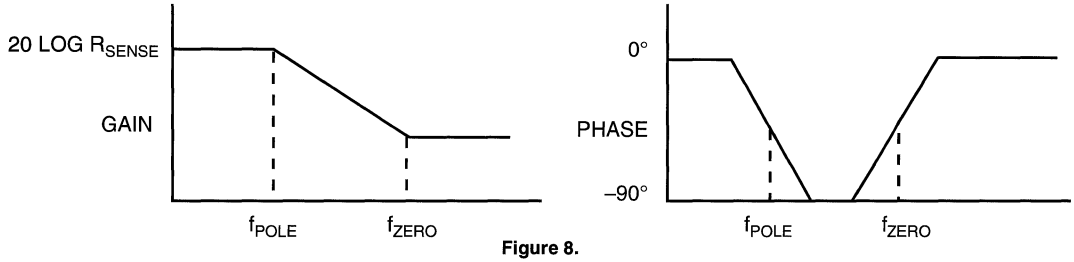


Figure 8.

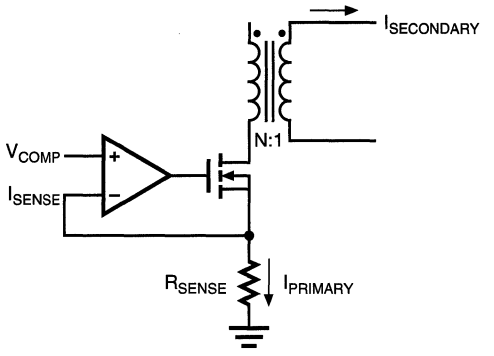


Figure 9.

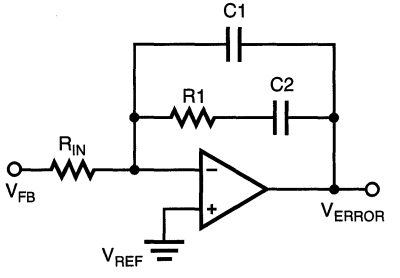
Since $I_{SECONDARY}$, the secondary current or output current, is proportional to the primary current, equation (4) can be rearranged to show a relationship between secondary current and V_{COMP}.

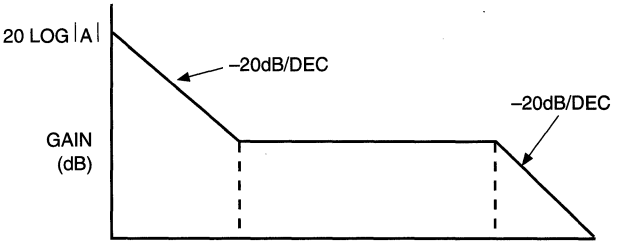
$$I_{PRIMARY} = \frac{I_{SECONDARY}}{N} = \frac{V_{COMP}}{R_{SENSE}} = \frac{I_{OUT}}{N}$$

$$\frac{\Delta V_{COMP}}{\Delta I_{OUT}} = \frac{R_{SENSE}}{N} \quad (8)$$

The transfer function of PWM stage can be created by combining equation (3) and (6):

$$G2(S) = \frac{\Delta I_{OUT}}{\Delta V_{CATHODE}} = \frac{N}{R_{SENSE}} \frac{CTR}{R6} R_{COMP} \quad (9)$$





$$G3(s) = \frac{V_{ERROR}}{V_{FB}} = \frac{1 + R1C2}{R_{IN}(C2 + C1) + SR1(C2 \bullet C1)}$$

$f_{p1} = 0$

$$f_Z = \frac{1}{2\pi R1C2}$$

$$f_{p}2 = \frac{1}{2\pi R1C2\left(\frac{C1}{C1 + C2}\right)}$$

A = OPEN LOOP GAIN OF THE AMPLIFIER

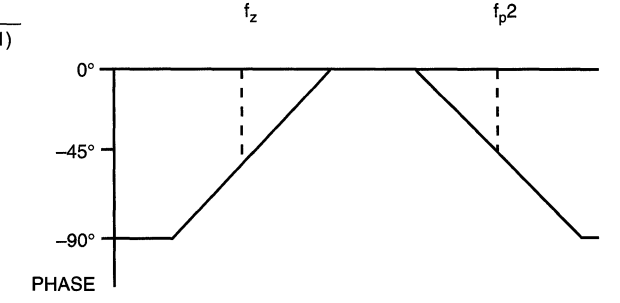


Figure 10.

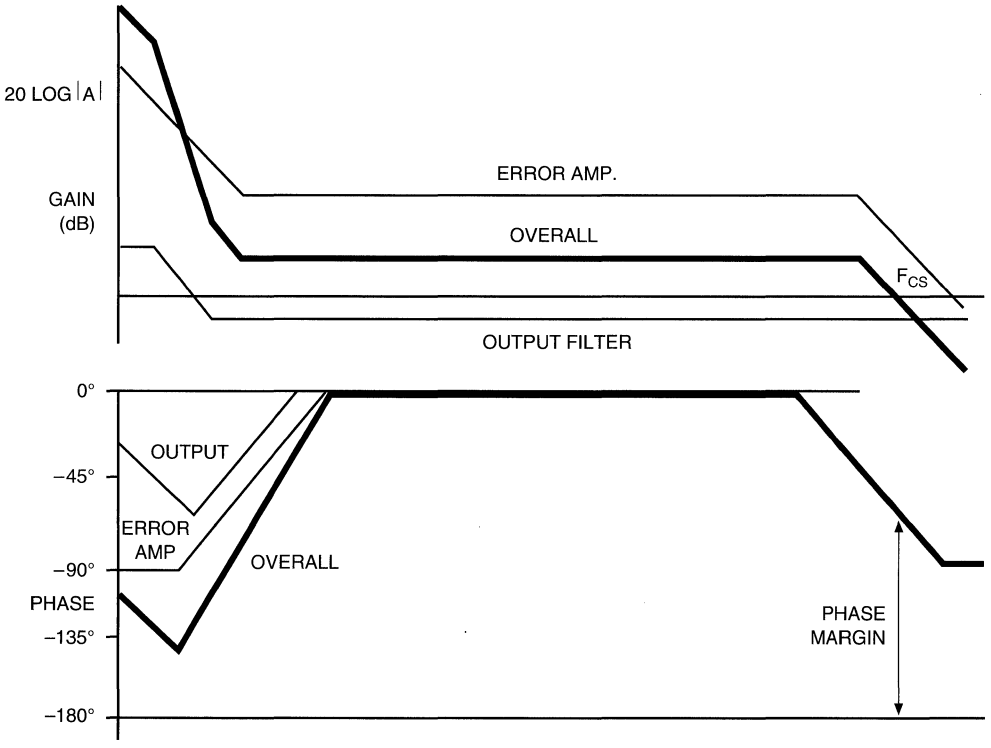


Figure 11.

Transfer function G2 consists of only gain and no phase shift.

4.4 Error Amplifier Compensation Network,G3(s)

Once the transfer functions of the output filter and PWM circuit stage are determined, the error amplifier compensation network can then be configured to achieve the optimum system performance. Figure 10 illustrates a compensation scheme that gives high frequency roll-off and high gain at low frequency.

This compensation scheme has some favorable characteristics for error amplifier compensation. It has very high DC gain and well-controlled roll off.

4.5 Overall System

Since this is a linear system, superposition technique can be applied to derive the overall system transfer function. By superimposing the gains and phases of the stages around the loop, a Bode plot of the overall system is generated. The poles and zeros of the compensation network can then be placed to optimize the system performance. Figure 11 combines the Bode plots of the stages and 180° phase shift is also added to account for the negative feedback of the system.

5. Measurement Results

A 150-watt current mode forward converter was constructed and its small signal loop characteristics modified to demonstrate its effects on system transient response. Figure 12 shows its gain-phase plot. As predicted by Figure 11, the same Bode plot curvature was acquired. The gain-phase shows the system has a phase margin of 86.7°, implying a stable system with a fast transient re-

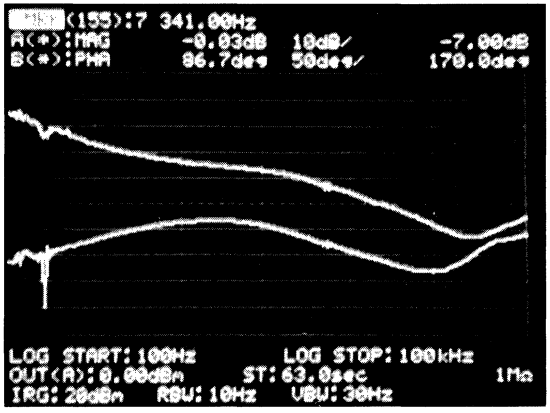


Figure 12.

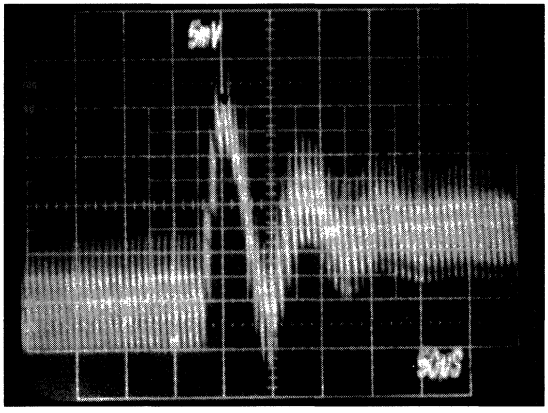


Figure 13.

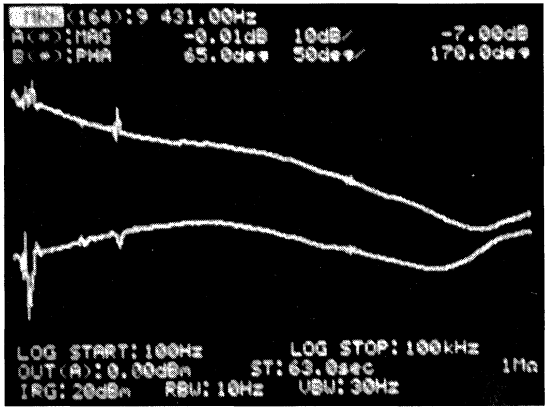


Figure 14.

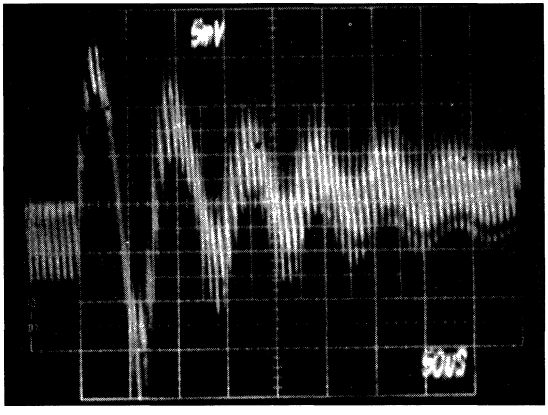


Figure 15.

sponse. Figure 13 shows the transient response of the system. To demonstrate the effects of phase margin, the phase margin of the system was decreased by increasing the overall gain of the system, increasing the crossover frequency. The phase margin decreases with increasing crossover frequency. Figure 14 shows a Bode plot of the system with higher cross over frequency and smaller phase margin of 65°. Its transient response is shown on figure 15. Note that smaller phase margin results in greater oscillation and longer settling time. Table 1 compares the changes in line and load regulations between two systems with different gain magnitudes. As discussed previously, high loop gain results in tighter line and load regulation. It should also be noted that a tradeoff has been made between the high phase margin and lower loop gain.

Load Regulation	High Loop Gain	Low Loop Gain
V_{IN} = 85 V_{AC}	127 mV	132 mV
$_{IN}$ = 135 V_{AC}	101 mV	116 mV
Line Regulation		
Low Load	21 mV	25 mV
High Load	5 mV	9 mV

(Table 1.)

6.0 Measurement Techniques

To guarantee accurate results, the input impedance of the test signal injection node must be larger than its output impedance. In the test circuit (Figure 6) where the error amplifier is on the secondary side and the PWM circuit is on the primary side, the test signal is injected at the output of the optocoupler and before the V_{COMP} input of the AS3842. The input impedance is the impedance looking into the V_{COMP} pin and the output impedance is the output impedance of the optocoupler. In other applications where the error amplifier can not be separated from the PWM circuitry, the test signal can be injected following the output filter capacitor, in series with the input to the error amplifier.

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Jamerson, C., and Hosseini, "A Simplified Procedure for Compensation Current-Mode Control Loops," HFPC Proceedings, June 1991, page 299–318.

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Notes

Appendix

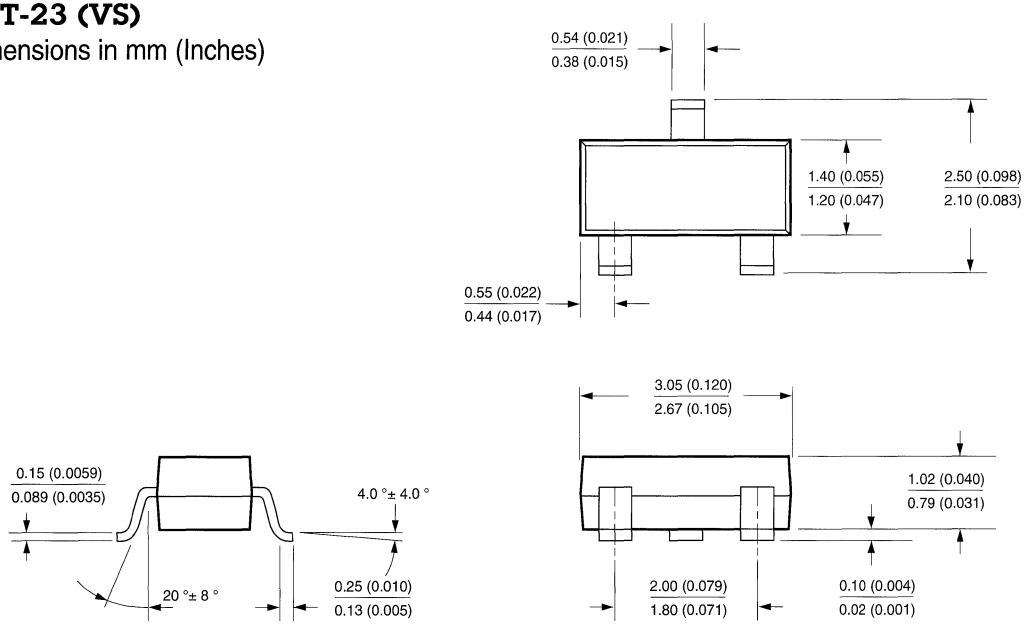
Notes

The following information applies to all packages:

1. Dimensions are in SI units (millimeters), except for those in parentheses which are English units (inches).
2. Shoulder and lead tip dimensions are measured to the centerline of the leads.
3. Tolerances are non-cumulative.
4. Lead material is copper alloy for all packages.
5. Lead finish is solder dip or solder plate.
6. Body material is plastic (epoxy).
7. Pin 1 is denoted by a • (dot) or (triangle per MIL-STD-38510H, ESDE Class 1) and will be silver or white ink, except for those packages which have a molded pin 1 depression.
8. Body dimensions do not include molding flash.

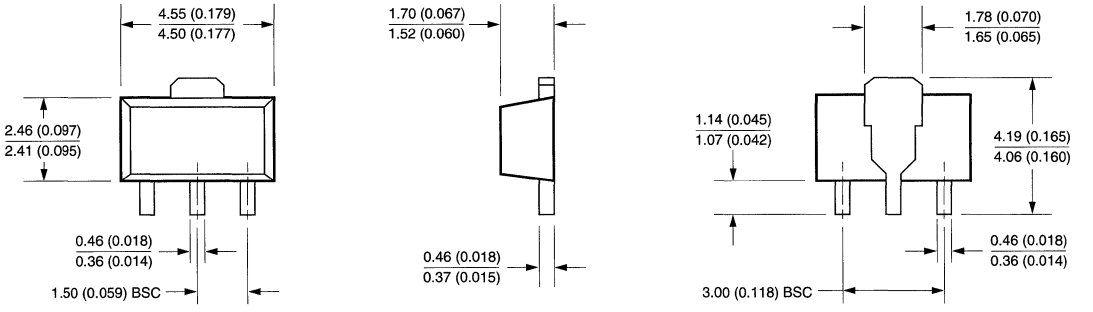
SOT-23 (VS)

Dimensions in mm (Inches)



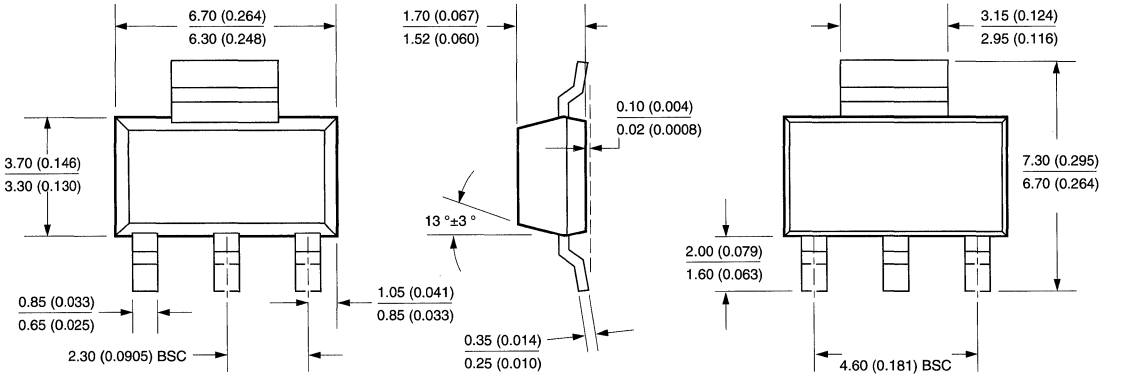
SOT-89 (S)

Dimensions in mm (Inches)



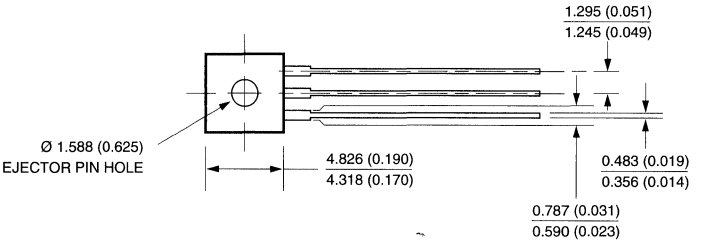
SOT-223 (G)

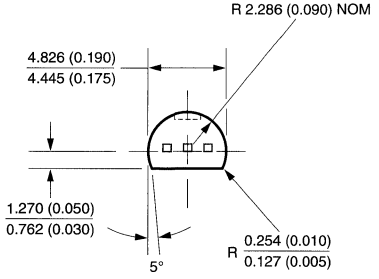
Dimensions in mm (Inches)

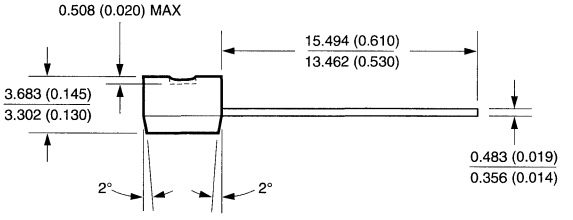


TO-92 PLASTIC (LP)

Dimensions in mm (Inches)

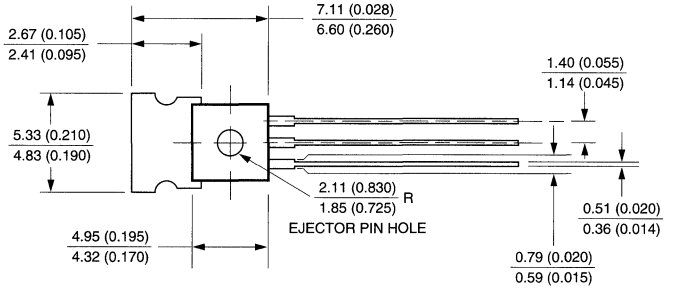


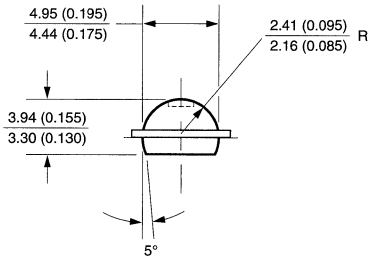


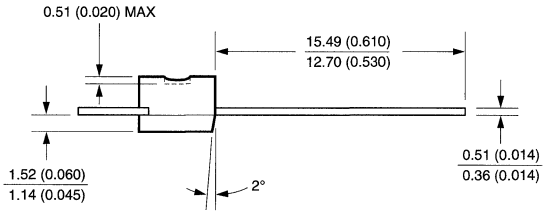


TO-237 PLASTIC (HP)

Dimensions in mm (Inches)

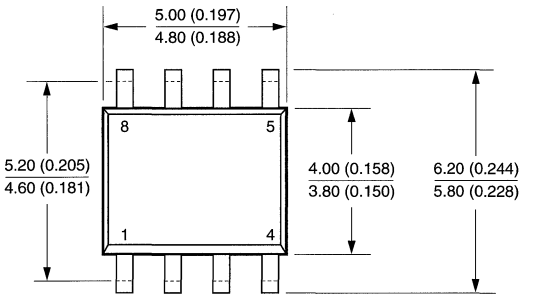


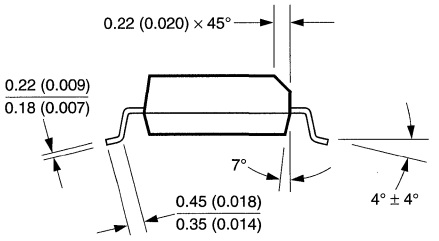


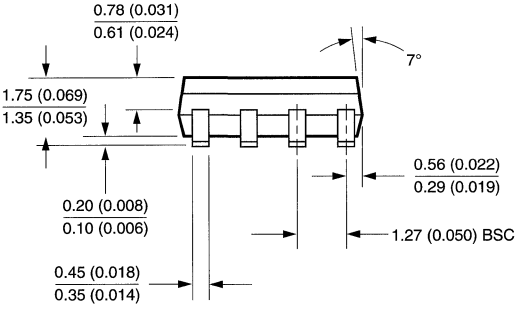


8-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)

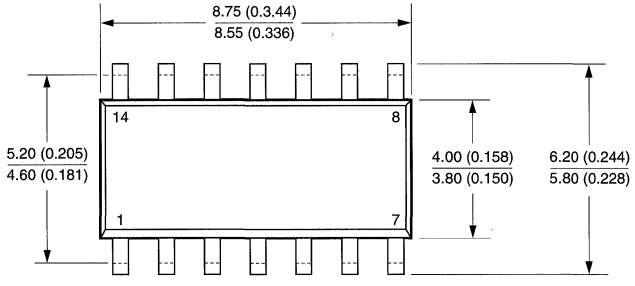


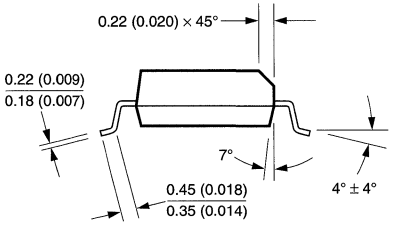


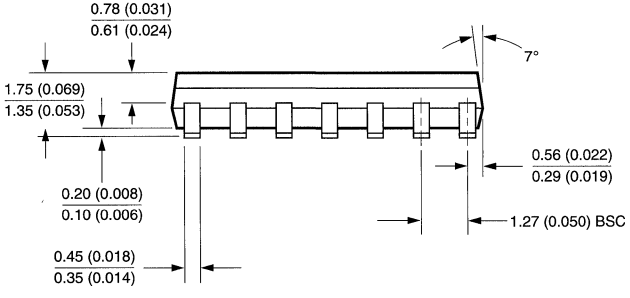


14-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)

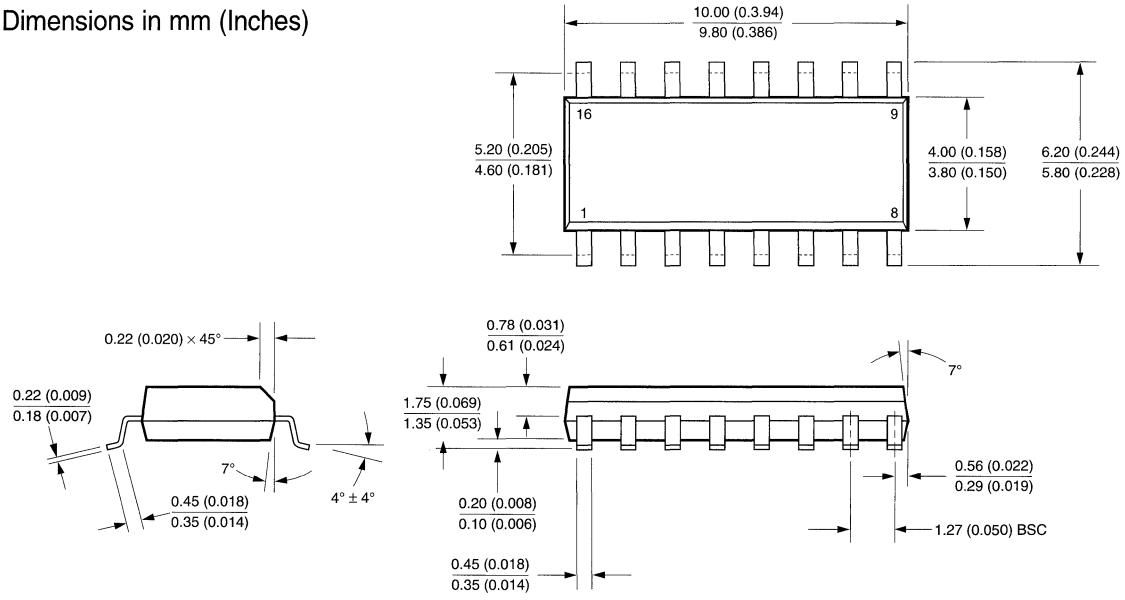






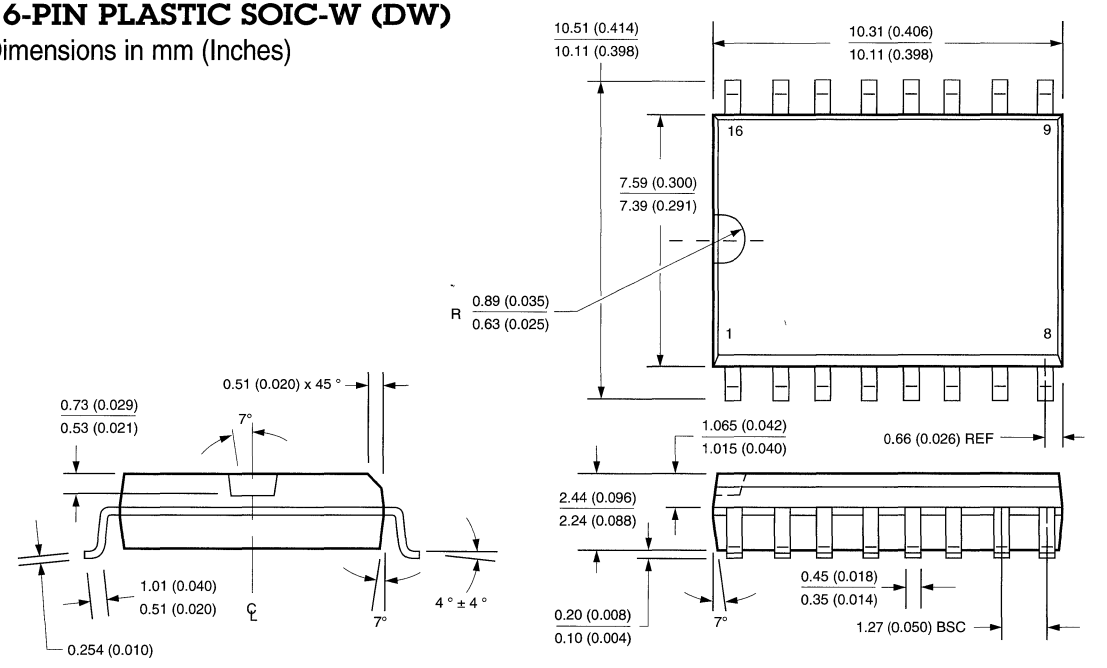
16-PIN PLASTIC SOIC (D)

Dimensions in mm (Inches)



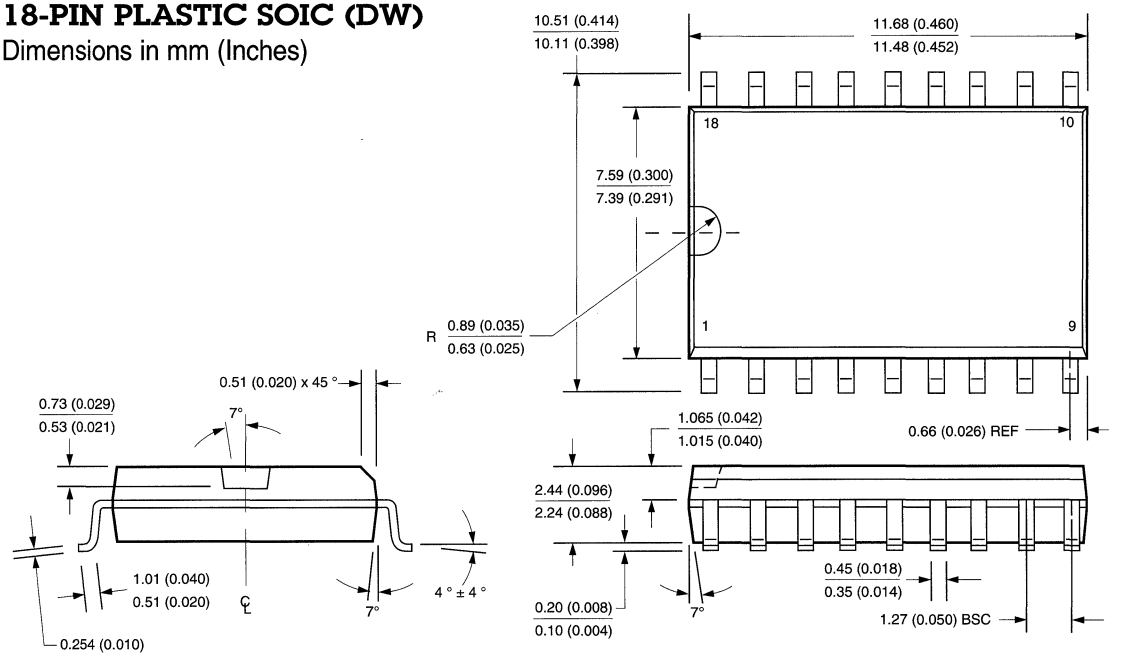
16-PIN PLASTIC SOIC-W (DW)

Dimensions in mm (Inches)



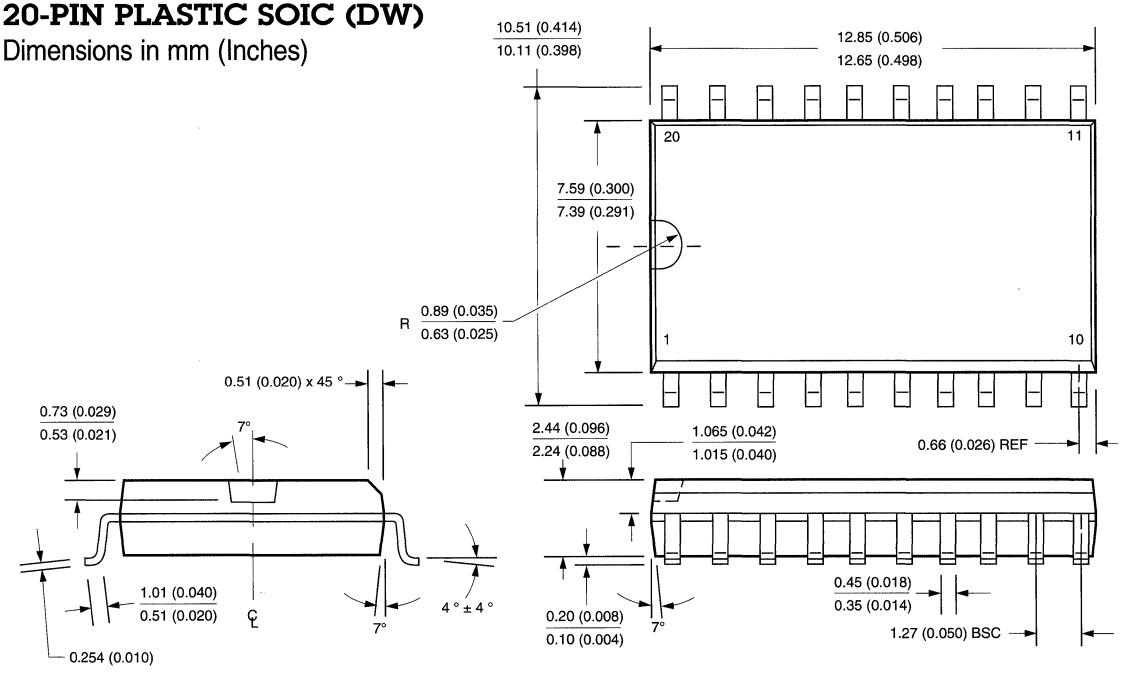
18-PIN PLASTIC SOIC (DW)

Dimensions in mm (Inches)



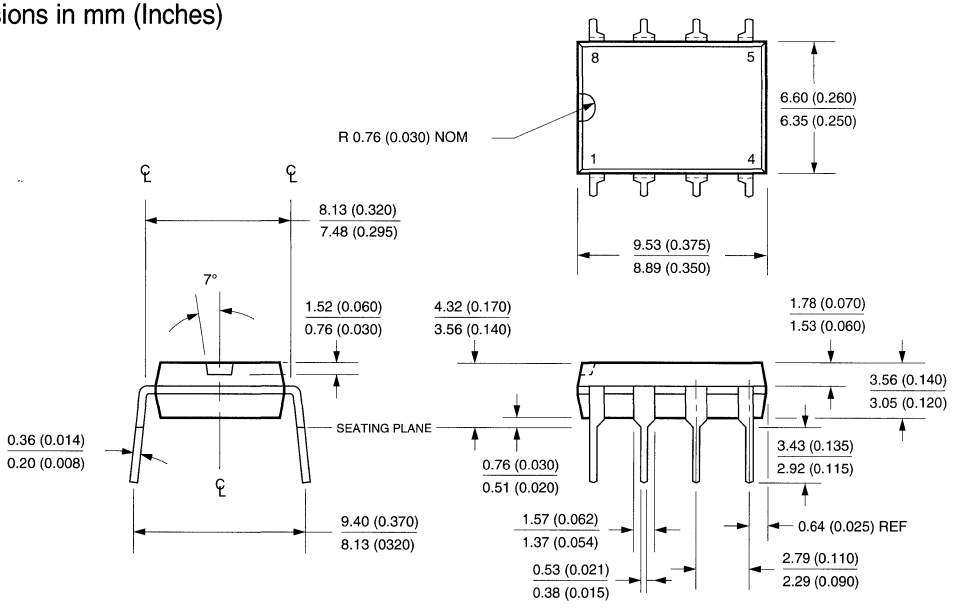
20-PIN PLASTIC SOIC (DW)

Dimensions in mm (Inches)



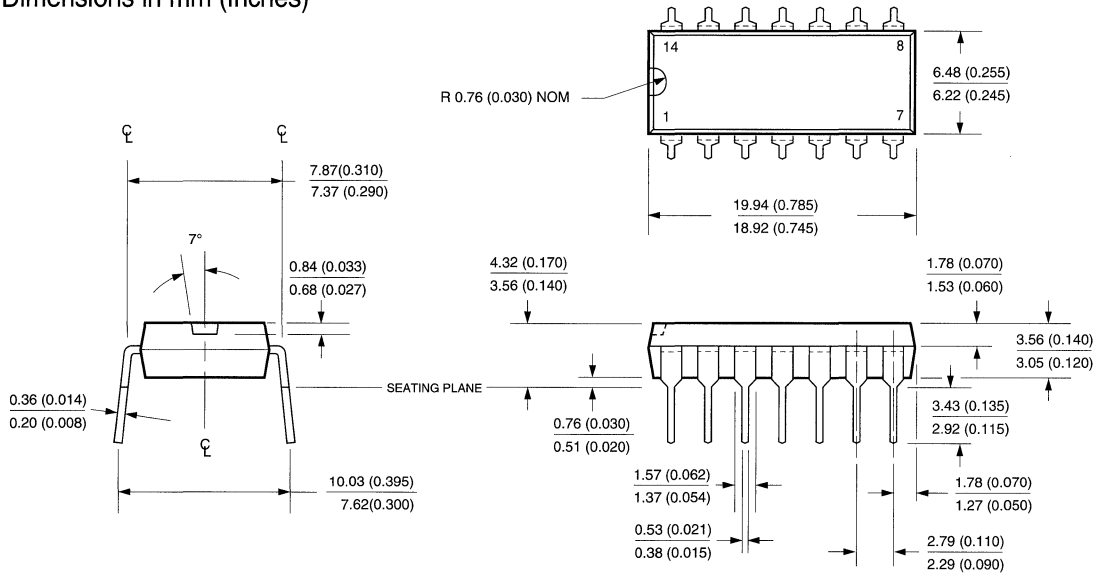
8-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



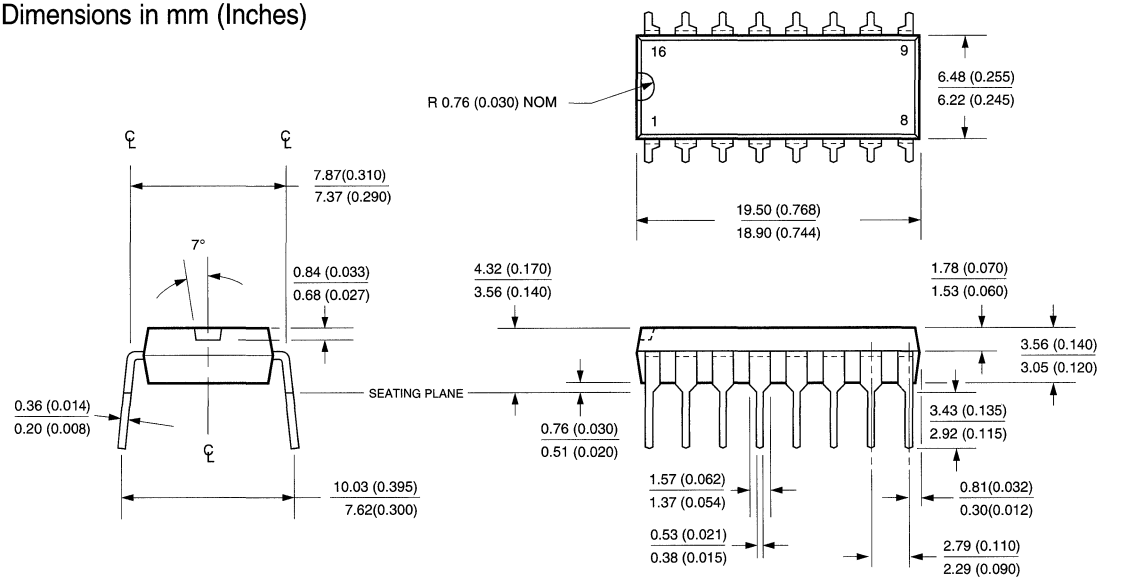
14-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



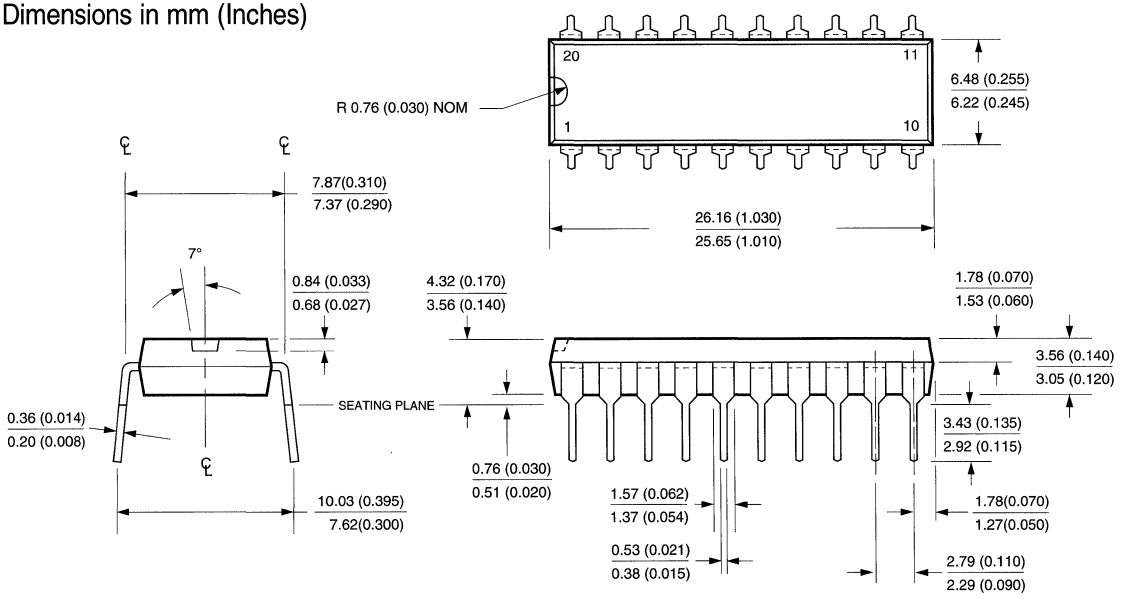
16-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



20-PIN PLASTIC DIP (N)

Dimensions in mm (Inches)



Quality Assurance and Reliability Program

Astec Semiconductor's Quality Assurance and Reliability Program utilizes various accelerated life tests as tools for establishing reliability status and progress. These tests are performed to identify infant mortality and wearout failure mechanisms for specific or generically similar device families. Quality is assured from tight control of layout design rules to final electrical testing of assembled parts. Astec Semiconductor strives towards continuous improvement of product reliability.

I. Lot Integrity

Wafer lot integrity maintained throughout test and assembly.

II. 100% Lot Traceability

Astec Semiconductor maintains 100% lot traceability. Each part is marked with the ASTEC logo, part number, wafer lot code, assembly date code, assembly vendor, and country of origin (package size permitting). Production wafer travelers will contain test site wafer parametric data, wafer sort and yields data, build sheets (mini process, bond pattern, and marking specifications), final test yields through assembly, final test data, and Q A test results.

III. ESD prevention

ESD prevention is emphasized at all levels of manufacturing and test. An adaptive facility, fixturing, clothing and handling techniques are employed consistent with ESD Association ADV-2.0 recommendations.

IV. Wafer Lot Acceptance

Astec Semiconductor contracts wafer foundry. Wafers are required to pass 5 of 9 test sites with 27 electrical specifications of our standard test pattern with incoming inspection comprised of over 100 electrical tests.

Included are:

- NPN, PNP, Vbe, beta, LVceo, Iceo, BVcbo, BVebo, breakdowns to substrate
- Sheet resistivities for base, emitter, resistor
- MOS Capacitor integrity

Wafer sort yields standardized by product and die size. Low yield wafers require engineering evaluation and disposition.

V. Device Reliability

Each lot subjected to:

HTRB- High Temperature Reverse Bias to MIL-STD-883C Method 1015.7

- No/low current, operational or max voltage
- $T_a = T_j = 125°$ C
- Sample size: Est. by MIL-STD 105E (lot), 48 hour minimum testing pass/fail based on sample criteria.

Selected lots subjected to long term reliability per the following:

HTRB- High Temperature Reverse Bias to MIL-STD-883C, Method 1015.7

- No/low current, operational or max voltage
- $T_a = T_j = 125°$ C
- Sample size: Est by MIL-STD 105E (lot) with 1000 hours minimum testing, pass/fail based on sample criteria.

OP Life-Operational Life testing:

- Operational voltage and current
- $T_j = 150°$ C, T_a adjusted based on power dissipation of the device where low power implies 150° C ambient. 150° C temperatures not applicable to circuits with built-in over temperature shut down.
- Sample based on 0.1% of lot size for 1000 hours, all failures require engineering evaluation and material disposition.

VI. Packaging Reliability

Assembly lots receive the following:

Autoclave (Pressure Cooker) accelerated storage test:

- Unbiased
- 121° C, 14.7 psig (2 atm)
- Sample size: Est. by MIL-STD 105E (lot) for 48 hours minimum. Pass/fail based on sample citeria.

Long Term Reliability:

Autoclave (Pressure Cooker) accelerated storage test:

- Unbiased
- 121° C, 14.7 psig (2 atm)
- Sample selection based on package type and supplier.
- Sample size: Est. by MIL-STD 105E (lot) for 1000 hours minimum, process monitor of vendor performance.

Notes

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