RAGE™ 128 VR and 128 GL Graphics Controller Specifications

Technical Reference Manual

P/N: GCS-C04100 Rev 0.05

The information contained in this manual has been carefully checked and is believed to be entirely reliable. No responsibility is assumed for inaccuracies. ATI reserves the right to make changes at any time to improve design and supply the best product possible.

Record of Revisions

Release	Date	Description of Changes
0.01	Apr 1998	Preliminary.
0.02	Jul 1998	General updates. Preliminary .
0.03	Aug 1998	General updates, added I^2C, MPP and VIP timing diagrams. Preliminary.
0.04	Oct 1998	General updates, added descriptions for APGCLAMP and GIOCLAMP. Preliminary.
0.05	Nov 1998	General edits. Book title change. New: 329 BGA package; 2D mode tables. See Revision History.

Related Manuals

RAGE 128 VR and GL Series

- RAGE™ 128 VR and 128 GL Graphics Controller Specifications (GCS-C04100)
- RAGE™ 128 Design Guide (DRS-D04100)

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Chapter 1
Introduction

1.1 About this Manual

This manual is part of a set of reference documents which provide information necessary to design the RAGE 128 VR and RAGE 128 GL graphics controller into a graphics subsystem. These documents are listed under Related Manuals at the beginning of this manual.

The electrical and thermal characteristics described in this document are specific to the RAGE 128 manufactured using TSMC's 0.25µm process, which has voltages of 2.5V core, 3.3V PCI I/O (with 5.0V tolerance), 3.3V AGP, and 3.3V or 2.5V (LVTTL, SSTL_2, and SSTL_3) memory interface. To obtain information about how to support ATI graphics controllers, steppings, and foundries in one PCB design, contact ATI.

The remaining chapters are as follows:

Chapter 2 - Main features of RAGE 128.

Chapter 3 - Pinout details.

Chapter 4 - Controller building-blocks, interface, and strap details.

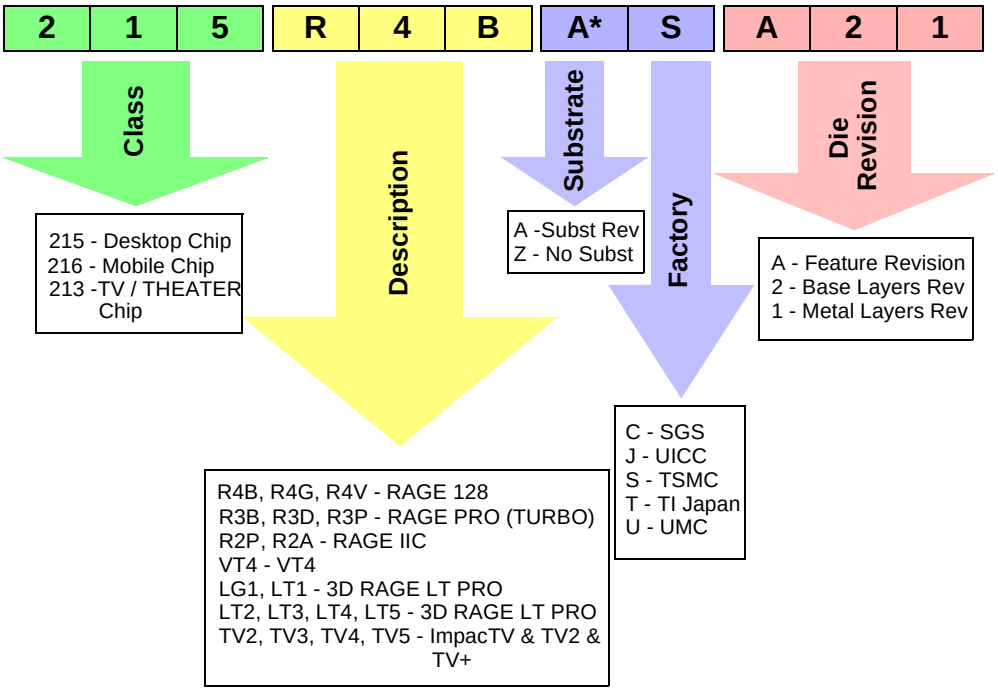
Chapter 5 - Timing diagrams.

Chapter 6 - Electrical and physical characteristics.

1.2 Part Number Code of ATI Components

The present manual is intended to cover components with revisions up to (see code below to identify substrate and die revisions) 215R4BASA21 (RAGE 128 VR), 215R4GASA22 (RAGE 128 GL), and 215R4VASA21 (RAGE 128 VR-O). The manual will be updated periodically to include latest component revisions and respective additional/changed specifications.

The figure below shows how to read the coded information contained in the branded ATI component part number.



* This character features only in the part numbers of post 1998/Q2 products

Figure 1-1. ATI Component Part Number Code

1.3 Conventions and Notations

The following conventions are used throughout this manual:

1.3.1 Pin/Signal Names

Mnemonics are used to represent pin and external strap resistors. For example the Device Select pin and the Interrupt Enable external strap are represented by DEVSEL# and ENINT# respectively.

Note: All active-low signal names are identified by the suffix #, e.g. BLANK#.

Pins may be identified by their *signal names* or ball references. The terms *pin name* and *signal name* are used interchangeably in the industry; in this document pin name is used to allow for situations in which pins have different functions and hence signal names (for example pins in the multimedia group). For such multiplexed pins, the alternate name(s) will be adequately noted.

1.3.2 Pin Types

The assigned codes for the various pin types based on operational characteristics are listed in the table below. For details about the electrical characteristics, refer to *Chapter 6 "Electrical and Physical Data"*.

Table 1-1 Pin Type Code

Code	Pin Type / Operational Characteristics
I	Digital Input
O	Digital Output
I/O	Bi-Directional Digital Input or Output
M	Multifunctional
Pwr	Power
Gnd	Ground
A-O	Analog Output
A-I	Analog Input

1.3.3 Numeric Representation

Hexadecimal numbers are appended with “h” (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

When the same pin name (except the following running integer) is used for pins that have identical functions (e.g. AD0, AD1, etc.), a short-hand notation is used to refer to all of them, i.e., AD[31:0] refers to AD0, AD1,..., and AD31.

The same short-hand notation is used to indicate bit occupation in a register. For example, SUBSYS_VEN_ID[15:0] refers to the Product Type Code field that occupies bit positions 0 through 15 within the 16-bit vendor ID register in PCI configuration space. No confusion is expected as the difference should be obvious by context.

1.3.4 Acronyms

Standard acronyms used in the literature are presumed known and will not be explained. When in doubt, the reader can refer to the following table for a quick check. Less frequently used or ATI-specific acronyms will have the full definition alongside in parenthesis when they appear for the first time in the document.

Table 1-2 Acronyms

Acronym	Full Expression
AGP	Accelerated Graphics Port
AMC	ATI Multimedia Channel
ATSC	Advanced Television Systems Committee
BGA	Ball Grid Array
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DTV	Digital TV
DVS	Digital Video Stream
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
I^2C	Bus Protocol (Philips Specification)
IDCT	Inverse Discrete Cosine Transform
LOD	Level of Detail
MPP	Multimedia Peripheral Port
PEROM	Flash Programmable and Erasable Read Only Memory

Table 1-2 Acronyms (Continued)

Acronym	Full Expression
PLL	Phase Locked Loop
POST	Power On Self Test
PQFP	Plastic Quad Flat Pack
ROP	Raster Operation
SDR	Single Data Rate
UV	Chrominance (also CrCb). Corresponds to the color of a pixel.
VBI	Vertical Blank Interval
VFC	VESA Feature Connector
VIP	Video Interface Port
YUV	The method of video signal color encoding. Includes luma (Y, black and white component) and chroma (UV, color component)

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Chapter 2
Overview

The RAGE 128 VR and 128 GL graphics controllers are ATI's latest offering in 3D technology. They incorporate the following outstanding key features:

- Stunningly fast 2D and 3D performance, achieved through a 128-bit engine, advanced 3D architecture, and support for leading edge memory technologies that includes DDR (double data rate) SGRAM and SDRAM.
- An enhanced 3D feature set with the addition of a 32-bit Z-buffer and an OpenGL stencil buffer, together with improvements in edge anti-aliasing, texture composition, subpixel/subtexel accuracy, and Z-based fog.
- An improved platform for DVD and video playback through the addition of 4-tap x and y filtering to the video overlay, IDCT support for accelerated software MPEG-2 playback, an integrated DVD subpicture decoder, and overlay support for ATSC resolutions.
- Enhanced multimedia functionality through a video port that supports both AMC and VIP 1.1 (VIP 2.0 ready) with extensions for ATSC resolutions, and glueless connections to the RAGE THEATER and ImpacTV companion chips, for TV out and analog video capture, or hardware MPEG-2 decoder chips, for high bit rate MPEG-2 decode.

2.1 Features Overview

2.1.1 General Features

- High integration results in a low cost, small footprint graphics subsystem (128 VR), ideal for motherboard designs.
- PCI version 2.1 with full bus mastering and scatter/gather support.
- Bi-endian support for compliance on a variety of processor platforms.
- Fast response to host commands:
  - 128-entry command FIFO.
  - 32-bit wide memory-mapped registers.
- Triple 8-bit palette DAC with gamma correction for true WYSIWYG color. Pixel rates up to 250 MHz.

- Supports SDRAM and SGRAM at up to 125 MHz memory clock providing bandwidths up to 2 GB/s across a 128-bit interface.
- Supports Double Data Rate SGRAM at up to 125 MHz memory clock providing bandwidths up to 2 GB/s across a 64-bit interface.
- Memory upgrade via industry standard SGRAM SO-DIMM, for reduced board area and higher memory speeds.
- Supports DDC1 and DDC2B+ for Plug-and-Play monitors.
- Power management with full VESA DPMS, EPA Energy Star, PCI and ACPI compliance.
- High quality components through built-in SCAN, Iddq, CRC and chip diagnostics.
- Single chip solution in 0.25 µm, 2.5 V CMOS technology, with multiple package options.
- Comprehensive HDKs, SDKs and utilities augmented by full engineering support.
- Complete local language supports (contact ATI for current list).
- Fully compliant with relevant sections of PC 98.

2.1.2 2D Acceleration

- Highly optimized 128-bit engine, capable of processing multiple pixels/clock.
- Hardware acceleration of Bitblt, Line Draw, Polygon / Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scrolling, Scissoring, and full ROP support (including ROP3).
- Optimized handling of fonts and text using ATI proprietary techniques.
- Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit.
- Acceleration in 8/16/24/32 bpp modes.
- Setup of 2D polygons and lines.

2.1.3 3D Acceleration

- Setup engine is capable of processing 3 million unculled triangles/s and 1.5 million culled triangles/s. The setup engine performs setup of both triangles and lines. This engine accepts all relevant parameters in IEEE floating point format and does not require any additional parameters (such as 1/area) to perform setup.

- 8KB on-chip texture cache with two-way associativity.
- Superscalar rendering engine providing top 3D performance (i.e. 2 pixel/clock pipeline).
- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare.
- Comprehensive enhanced 3D feature set:
    - Improved texture compositing, with no limitations on texture formats or location (i.e. one texture may reside in AGP memory and the other in frame buffer memory). Two textures in one pass.
    - Full screen or window double buffering for smooth animation.
    - Support of special effects such as simultaneous alpha blending and fog (vertex and z-based), video textures, texture lighting, reflections, shadows, spotlights, LOD biasing and texture morphing. Filtered texture alpha channel, and hardware support for D3D 'MODULATEALPHA' texture blending mode.
    - Hidden surface removal using 16, 24, or 32-bit Z-buffering (maximum Z-buffer depth is 24 bits when stencil buffer enabled).
    - 8-bit stencil buffer.
    - Line and Edge anti-aliasing.
    - 4 bits of subpixel and subtexel accuracy.
    - Gouraud and specular shaded polygons.
    - Perspectively correct per pixel mip-mapped texturing with chroma-key support.
    - Bilinear and trilinear texture filtering.
    - Full support of Direct3D texture lighting.
    - Dithering support in 16 bpp for near 24 bpp quality in less memory.
- Extensive 3D mode support:
    - Draw in RGBA32, RGBA16, & RGB16.
    - Texture map modes: RGBA32, RGBA16, RGB16, RGB8, ARGB4444, YC_rC_b444.
    - Compressed texture modes: YC_rC_b422, CLUT4 (CI4), CLUT8 (CI8), VQ
- Full scene sort independent anti-aliasing.

2.1.4 Motion Video Acceleration

- Video scaling and enhanced YC_rC_b to RGB color space conversion for full-screen / full-speed video playback.
- Front and back end scalers plus capture port scaler to support multi-stream video for video conferencing and other applications.
- Front end scaler support for 8, 16, 24, and 32 bpp color depths.
- 4-tap horizontal and 2-tap vertical filtered up and downscaling of RGB content (RGB 15/16/32) to give top quality playback of RGB-based AVI files. 4-tap horizontal and vertical filtering for RGB 32 content at upscaling ratios greater than or equal to 1.5.
- 4-tap filtered upscaling in both horizontal and vertical directions and filtered downscaling (2 and 4-tap) of YC_rC_b content to give top quality playback.
- Enhanced line buffer allowing vertical filtering of native standard definition and high definition images. The overlay and capture system includes support for all proposed ATSC resolutions.
- Enhanced MPEG-2 hardware decode acceleration, including support for both motion compensation and IDCT, to provide dramatically reduced CPU utilization without incurring the cost of a full MPEG-2 decoder. This is superior to competing motion compensation solutions, including those marketed as ‘9-bit’ motion compensation.
- Hardware DVD subpicture decoder with interpolating scaler and alpha compositor to provide optimal DVD subpicture quality in all display bit depths.
- Special filter circuitry eliminating video artifacts caused by displaying interlaced video on non-interlaced displays (i.e., bob and weave).
- Bi-directional bus mastering engine with full YC_rC_b planar mode support for superior MPEG-2 decode and video conferencing.
- Support for graphics and video keying for effective overlay of video and graphics.
- Ability to genlock to any broadcast video signal, eliminating synchronization problems.
- YC_rC_b to RGB color space converter with support for both packed and planar YC_rC_b.
- YC_rC_b422, YC_rC_b410, YC_rC_b420, RGB32, RGB16/15 in back end scaler/overlay.
- Ability to reconstruct frames of field-based content when software indicates that content was originally progressive and has been converted via 3:2 pull down, provided that the decoder gives appropriate cues.

2.1.5 Video Port

- Enhanced 16-bit video port allowing support for all proposed DTV formats.
- High quality horizontal multi-tap downscaler with sharpness control.
- Hardware mirroring for flipping video images in video conferencing systems.
- Simultaneous capture of two video streams. This allows simultaneous use of both video ports, as well as the capture of a single stream at two distinct resolutions (to allow, for example, a stream to be displayed at full resolution and simultaneously captured to disk at a lower resolution).
- Support for both VIP 1.1 (VIP 2.0 ready) and AMC (ATI Multimedia Channel) allowing glueless interface to the RAGE THEATER and/or direct connection to video upgrades such as:
  - Hardware MPEG-2 decoder.
  - Video capture / video conferencing.
  - Digital Broadcast Satellite receiver.
  - TV Tuner with Intercast support.

2.1.6 Display

- Triple 8-bit palette DAC with gamma correction for true WYSIWYG color. Pixel rates up to 250 MHz standard, optional 230 MHz.
- Support for 4/8/15/16/24/32 bpp display modes, with gamma correction for all modes (no acceleration is provided in 4 bpp modes).
- Support for DDC1 and DDC2B+ for plug and play monitors, and AppleSense monitor detection support.
- Hardware cursor (up to 64x64x2).
- Improved VGA read/write throughput.
- Support for Big-Endian and Little-Endian display buffers.

2.1.7 Bus Support

- Comprehensive AGP support, including 2X mode operation, Sideband Addressing, and AGP Texturing (Execute mode).
- PCI version 2.1 with full bus mastering and scatter / gather support.

- Support for both 3.3V and 5V PCI interfaces.
- Reserved pins in anticipation to future pin compatible variants that provide AGP 4X support.

2.1.8 Memory Support

- Supports a variety of memory configurations for bandwidths of up to 2 GB/s:
  - Single Data Rate (SDR) SGRAM/SDRAM at up to 125 MHz across a 128-bit interface (2 GB/s).
  - Double Data Rate (DDR) SGRAM at up to 125 MHz across a 64-bit interface (2.0 GB/s).
  - SDR SGRAM at up to 143 MHz across a 64-bit interface (1.1 GB/s).
- Flexible graphics memory configurations: 2MB up to 32MB SDR/DDR SGRAM or SDR SDRAM.
- Memory upgrade via industry standard SGRAM SO-DIMM, for reduced board area and higher memory speeds.
- Support for LVTTL and SSTL memory interfaces.

2.1.9 Power Management

- Support for version 1.0 of the ACPI Specification and version 1.0 of the PCI Power Management Specification.

2.1.10 Test Capability

The RAGE 128 VR/GL have a variety of test modes and capabilities that provide a very high fault coverage and low DPM (Defect Per Million) ratio:

- Full scan implementation on the digital core logic which provides over 95% fault coverage through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- A HIGH_Z (high impedance) test mode in order to allow board level testing of neighboring devices and I/O current leakage measurements on the RAGE 128 itself.

- A NANDTREE test mode on all the digital I/O's to allow for proper soldering verification at the board level.
- Improved access to the analog modules and PLLs in the chip in order to allow full evaluation and characterization of these modules.
- Improved IDDQ mode support to allow chip evaluation through current leakage measurements.

These test modes can be accessed through the settings on the TESTEN pin and two dedicated straps.

2.2 Chip Packaging Options

RAGE 128 VR/GL are available in three packaging options to give manufacturers maximum flexibility to differentiate products.

RAGE 128 GL (328-Pin BGA)

This higher performance RAGE 128 implementation incorporates a 128-bit memory interface with support for SGRAM at speeds of up to 125 MHz. It is intended for high-end systems.

RAGE 128 VR (272-Pin BGA)

This part is ideal for motherboard implementations. It incorporates a 64-bit memory interface with support for SDR SGRAM and DDR SGRAM at up to 125MHz, giving a memory bandwidth of 2.0 GB/s. This variant is intended for mainstream applications, although it will give an equivalent performance to that of the RAGE 128 GL when coupled with DDR SGRAM.

RAGE 128 VR-0 (329-Pin BGA)

This variant has the same functionality and performance as the 272-pin RAGE 128 VR. It is intended for designs that provide an upgrade path to future MDB (Multiple Die BGA) packages.

Table 2-1 RAGE 128 Packaging and Identification Codes

Chip ID	Description
RE (5245h)	328 BGA PCI, 128-bit memory interface (RAGE 128 GL)
RF (5246h)	328 BGA AGP, 128-bit memory interface (RAGE 128 GL)
RK (524Bh)	272 BGA PCI, 64-bit memory interface (RAGE 128 VR)
RL (524Ch)	272 BGA AGP, 64-bit memory interface (RAGE 128 VR)
	329 BGA AGP, 64-bit memory interface (RAGE 128 VR-O)

2.3 Display Modes

Note: The modes below are based on the 250 MHz DAC.

2.3.1 2D Modes for 128-bit SDR or 64-bit DDR SD/SGRAM (100MHz)

Table 2-2 2D Modes for 128-bit SDR/64-bit DDR SD/SGRAM (100MHz)

Display Mode	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Buffer Memory (MB)															
				4				8				16				32			
				Colour Depth (bpp)															
				8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
640x480	60	31.5	25.2																
	72	37.9	31.5																
	75	37.5	31.5																
	85	43.3	36.0																
	90	45.4	37.8																
	100	50.9	43.1																
	120	61.8	52.4																
	160	84.3	72.8																
	200	108.0	95.0																

Table 2-2 2D Modes for 128-bit SDR/64-bit DDR SD/SGRAM (100MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Buffer Memory (MB)															
				4				8				16				32			
				Colour Depth (bpp)															
				8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
800x600	48	26.4	29.3																
	56	35.1	36.0																
	60	37.9	39.9																
	70	43.7	45.5																
	72	48.1	50.0																
	75	46.9	49.5																
	85	53.7	56.3																
	90	56.8	60.0																
	100	63.6	68.1																
	120	77.1	83.9																
	160	105.4	116.4																
	180	120.0	132.5																
	200	135.0	149.0																
1024x768	43	35.5	44.9																
	60	48.4	65.0																
	70	56.5	75.0																
	72	57.6	78.4																
	75	60.0	78.8																
	85	68.7	94.5																
	90	72.8	100.1																
	100	81.4	113.3																
	120	98.7	139.0																
	140	116.6	164.2																
	150	125.7	176.9																
	160	134.8	192.0																
	180	153.5	218.6																

Table 2-2 2D Modes for 128-bit SDR/64-bit DDR SD/SGRAM (100MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Buffer Memory (MB)															
				4				8				16				32			
				Colour Depth (bpp)															
				8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
1152x864	43	38.0	56.0	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	47	41.7	62.1	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	60	53.7	81.6	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	70	63.0	96.7	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	75	67.5	108.0	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	80	72.4	112.3	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	85	77.0	119.6	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	100	91.5	143.4	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	120	111.1	176.0	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	150	141.4	226.3	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
	160	151.6	242.6	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■
1280x1024	43	45.1	75.1	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	47	49.4	83.0	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	60	64.0	108.0	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	70	74.6	128.9	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	74	79.0	138.5	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	75	80.0	135.0	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	85	91.1	157.5	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	90	97.0	169.2	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	100	108.5	190.9	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	120	131.6	233.7	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	125	137.6	244.4	■	■			■	■	■	■	■	■	■	■	■	■	■	■
1600x1200	52	64.2	137.7	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	58	71.9	155.4	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	60	75.0	162.0	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	66	82.2	178.9	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	72	90.0	195.9	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	75	93.8	202.5	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	76	95.2	208.7	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	85	106.3	229.5	■	■			■	■	■	■	■	■	■	■	■	■	■	■
1800x1440	60	89.4	219.5	■				■	■	■	■	■	■	■	■	■	■	■	■
	65	97.1	238.5	■				■	■	■	■	■	■	■	■	■	■	■	■
	70	104.9	249.9	■				■	■	■	■	■	■	■	■	■	■	■	■

Table 2-2 2D Modes for 128-bit SDR/64-bit DDR SD/SGRAM (100MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Hor. Scan (KHz)	Pixel Clock (MHz)	Buffer Memory (MB)															
				4				8				16				32			
				Colour Depth (bpp)															
				8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
1920x1080	60	67.0	172.7																
	70	78.6	205.1																
	75	84.6	220.6																
	80	90.4	237.4																
1920x1200	60	74.5	193.1																
	72	90.0	236.3																
	75	93.9	246.5																
	76	95.2	249.8																
1920x1440	60	89.4	234.5																

Note: Shaded areas are supported. Areas not shaded are not supported.

2.3.2 2D Modes for 64-bit SDR SD/SGRAM (100MHz)

Table 2-3 2D Modes for 64-bit SDR SD/SGRAM (100MHz)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
640x480	60																
	72																
	75																
	85																
	90																
	100																
	120																
	160																
	200																

Table 2-3 2D Modes for 64-bit SDR SD/SGRAM (100MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
800x600	48																
	56																
	60																
	70																
	72																
	75																
	85																
	90																
	100																
	120																
	160																
	180																
1024x768	43																
	60																
	70																
	72																
	75																
	85																
	90																
	100																
	120																
	140																
1152x864	43																
	47																
	60																
	70																
	75																
	80																
	85																
	100																
	120																

Table 2-3 2D Modes for 64-bit SDR SD/SGRAM (100MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
1280x1024	43	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	47	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	60	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	70	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	74	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	75	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	85	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	90	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■
	100	■	■	■		■	■	■		■	■	■		■	■	■	
1600x1200	52	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	58	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	60	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	66	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	72	■	■			■	■	■		■	■	■		■	■	■	
	75	■	■			■	■	■		■	■	■		■	■	■	
	76	■	■			■	■	■		■	■	■		■	■	■	
	85	■	■			■	■	■		■	■	■		■	■	■	
1800x1440	60	■				■	■	■		■	■	■	■	■	■	■	■
	65	■				■	■	■		■	■	■		■	■	■	
	70	■				■	■			■	■			■	■		
1920x1080	60	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	70	■	■			■	■	■		■	■	■		■	■	■	
	75	■	■			■	■	■		■	■	■		■	■	■	
	80	■	■			■	■	■		■	■	■		■	■	■	
1920x1200	60	■				■	■	■		■	■	■	■	■	■	■	■
	72	■				■	■	■		■	■	■		■	■	■	
	75	■				■	■	■		■	■	■		■	■	■	
	76	■				■	■	■		■	■	■		■	■	■	
1920x1440	60	■				■	■	■		■	■	■	■	■	■	■	■

Note: Shaded areas are supported. Areas not shaded are not supported.

2.3.3 2D Display Modes for 64-bit SDR SD/SGRAM 2:1 (143 MHz)

Note: “2:1” in the heading above refers to the memory clock ratio, i.e., 143 MHz external memory clock over 71.5 MHz internal memory clock.

Table 2-4 2D Display Modes for 64-bit SDR SD/SGRAM (2:1, 143 MHz)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
640x480	60																
	72																
	75																
	85																
	90																
	100																
	120																
	160																
	200																
800x600	48																
	56																
	60																
	70																
	72																
	75																
	85																
	90																
	100																
	120																
	160																
	180																
	200																

Table 2-4 2D Display Modes for 64-bit SDR SD/SGRAM (2:1, 143 MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
1024x768	43																
	60																
	70																
	72																
	75																
	85																
	90																
	100																
	120																
	140																
	150																
	160																
1152x864	43																
	47																
	60																
	70																
	75																
	80																
	85																
	100																
	120																
	140																
	150																
1280x1024	43																
	47																
	60																
	70																
	74																
	75																
	85																
	90																
	100																
	120																

Table 2-4 2D Display Modes for 64-bit SDR SD/SGRAM (2:1, 143 MHz) (Continued)

Display Mode	Refresh Rate (Hz)	Buffer Memory (MB)															
		4				8				16				32			
		Color Depth (bpp)															
		8	16	24	32	8	16	24	32	8	16	24	32	8	16	24	32
1600x1200	52	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	58	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	60	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	66	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	72	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	75	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	76	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	85	■	■			■	■	■		■	■	■		■	■	■	
1800x1440	60	■				■	■	■		■	■	■	■	■	■	■	■
	65	■				■	■	■		■	■	■		■	■	■	
	70	■				■	■	■		■	■	■		■	■	■	
1920x1080	60	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	70	■	■			■	■	■	■	■	■	■	■	■	■	■	■
	75	■	■			■	■	■		■	■	■		■	■	■	
	80	■	■			■	■	■		■	■	■		■	■	■	
1920x1200	60	■				■	■	■		■	■	■	■	■	■	■	■
	72	■				■	■	■		■	■	■	■	■	■	■	■
	75	■				■	■	■		■	■	■		■	■	■	
	76	■				■	■	■		■	■	■		■	■	■	
1920x1440	60	■				■	■	■		■	■	■	■	■	■	■	■

Note: Shaded areas are supported. Areas not shaded are not supported.

2.3.4 ATSC Modes

The table below lists all 18 North American ATSC modes (the term *ATSC* used in this document encompasses all of these modes unless otherwise indicated). Support for ATSC implies support for these modes in the video port and back-end scaler, as well as display support. For the 1920x1080 and 1280x720 modes, it may be necessary to convert the source content to a lower horizontal resolution via the multi-tap horizontal downscaler, with a minor reduction in image quality.

Table 2-5 ATSC Modes

Vertical Lines	Pixels	Aspect Ratio	Picture Rate
1080	1920	16:9	60I, 30P, 24P

Table 2-5 ATSC Modes

Vertical Lines	Pixels	Aspect Ratio	Picture Rate
720	1280	16:9	60P, 30P, 24P
480	704	16:9 and 4:3	60P, 60I, 30P, 24P
480	640	4:3	60P, 60I, 30P, 24P

For more information about ATSC modes, refer to the *ATSC Digital Television Standard* (ATSC Document A/53) and the *Use of the ATSC Digital Television Standard* (ATSC Document A/54). These documents are available at *http://www.atsc.org*.

2.3.5 3D Modes

Table 2-6 3D Modes

Frame Buffer (MB)	Screen Resolution	Color Depth (bpp)	Front Buffer (MB)	Back Buffer (MB)	Z Buffer Depth[1] (bpp)	Z buffer (MB)	Local Texture Memory[2] WZ (MB)	Local Texture Memory[2] W/O Z (MB)	Primary Use of Configuration
2	640x480	16	0.59	0.59	16	0.59	0.24	0.83	Value systems
4	640x480	32	1.17	1.17	16	0.59	1.07	1.66	Mainstream systems
	800x600	16	0.92	0.92	16	0.92	1.25	2.17	
8	800x600	32	1.83	1.83	32	1.83	2.51	4.34	PowerUsers
	1024x768	16	1.50	1.50	32	3.00	2.00	5.00	
	1024x768	32	3.00	3.00	16	1.50	0.50	2.00	
	1280x1024	16	2.50	2.50	16	2.50	0.50	3.00	
16	1280x1024	32	5.00	5.00	32	5.00	1.00	6.00	Volume CAD
	1600x1200	16	3.66	3.66	32	7.32	1.35	8.68	
32	1600x1200	32	7.32	7.32	32	7.32	10.0	17.35	PC Workstations
	1920x1200	32	8.79	8.79	32	8.79	5.63	14.42	

[1] 32 bit Z-buffer can optionally be configured as 24 bit Z-Buffer plus 8 bit Stencil Buffer.
[2] AGP configurations can use system memory for additional textures.

2.4 Software Support

Table 2-7 OS and API Support

Software Support	DOS	Win 3.x[6]	Win 95	Win 98	NT 3.51	NT 4.0	NT 5.0	Mac OS	OS/2[6]
2D Software Support [1]									
Accelerated Driver	VESA[2]	3	3	3	3	3	3	3	3
Video Software Support									
MS DirectDraw			3	3		3	3		
MS ActiveMovie/ Direct Show			3	3			3		
MPEG-1 software playback			3	3		3	3	3	
MPEG-2 software playback			3	3			3		
QuickTime acceleration									
3D Software Support									
MS Direct3D			3	3			3		
QuickDraw 3D RAVE								3	
OpenGL			3	3		3	3		
ATI 3D CIF[5]			3	3					
AGP			3	3		4	3		

1 - Additional third parties (including SCO Unix and UNIXWARE)
2 - Direct BIOS support
3 - Available 2H98
4 - NT 4.0 Service pack 3 supports AGP devices, but does not provide support for AGP texturing
5 - ATI's 3D API for the RAGE family
6 - Basic acceleration only

Chapter 3
Pinout Descriptions

3.1 Pin Grouping

This chapter provides brief descriptions of the pins. For more details about interfacing and electrical characteristics, refer to *Chapter 4*, *Chapter 6* and *Appendix C*.

For description purposes, pins are grouped according to their interface functionality. The table below lists the 12 pin groups and the pin counts for the four RAGE 128 packages.

Table 3-1 Pin Grouping

Pin Group	272 BGA (RAGE 128VR)	328 BGA (RAGE 128GL)	329 BGA (RAGE 128VR-O)
AGP / PCI	66	66	66
Memory (64 bits)	99	-	99
Memory (128 bits)	-	171	-
Monitor	11	11	11
PLL and Crystal	4	4	4
Multimedia:			
AMC	23	23	23
Enhanced Video Port	10	0 (Muxed on upper 64 bits of memory)	10
MPP2	10	0 (Muxed on upper 64 bits of memory)	0
Test	1	1	1
DAC	4	4	4
ROM / EPROM	2	2	2
Clamps	2	2	2
Power and Ground	40	44	77
No Connects			40
Total Pin Count	**272**	**328**	**329**

3.2 Pinout Top Views

The following three figures show the top view of the three RAGE 128 variants. For a full listing of the pinouts for all variants, refer to the tables in Appendix A.

3.2.1 Top View of the 272 BGA Package (RAGE 128VR)

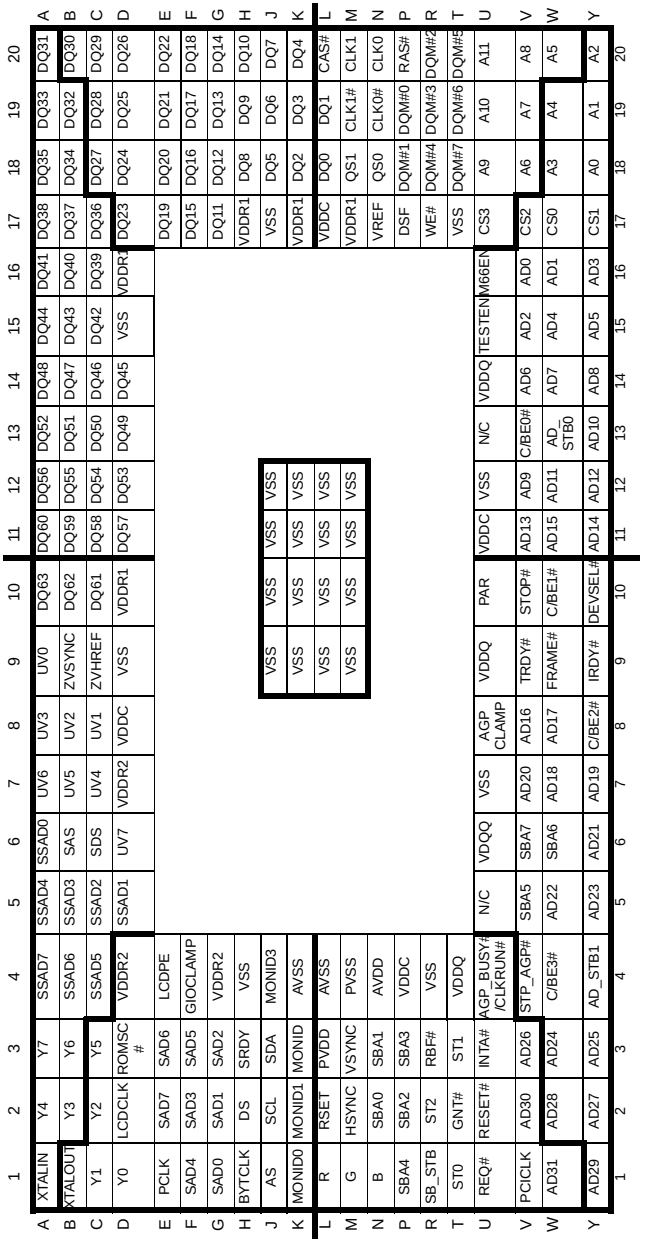


Figure 3-1 Top View of the 272 BGA Package (RAGE 128VR)

3.2.2 Top View of the 328 BGA Package (RAGE 128GL)

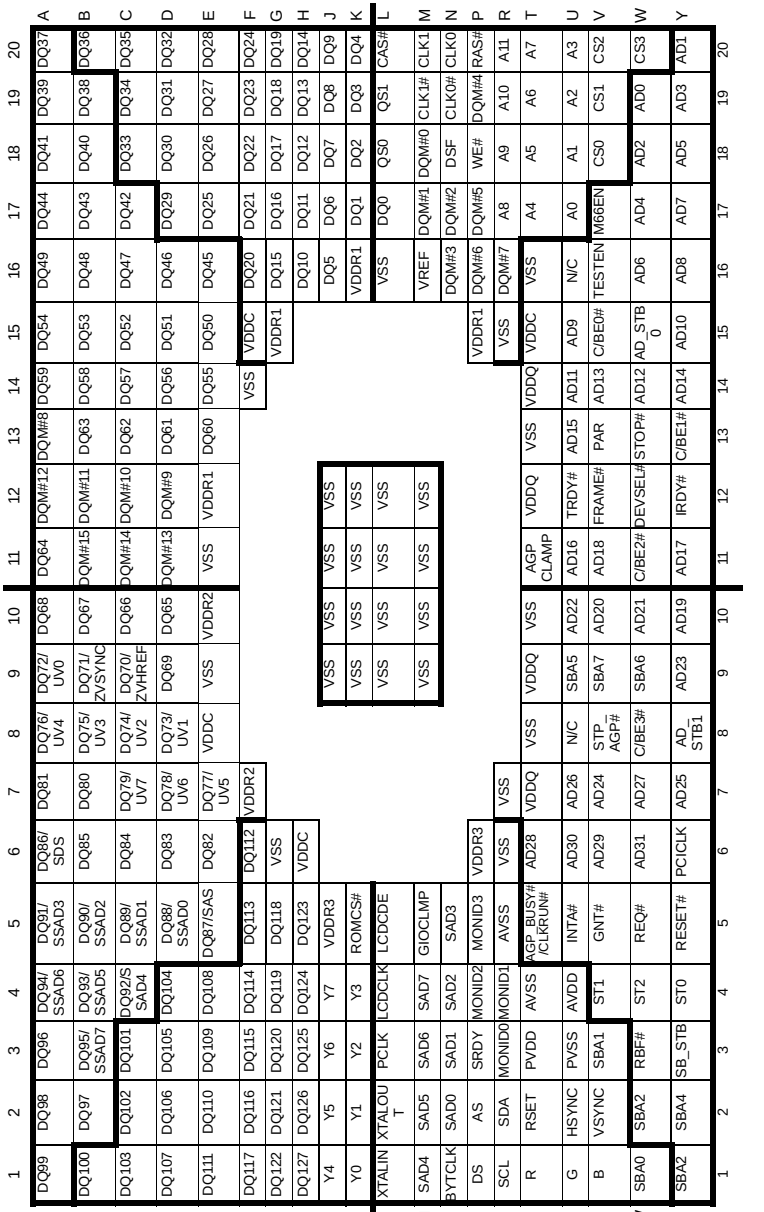


Figure 3-2 Top View of the 328 BGA Package (RAGE 128GL)

3.2.3 Top View of the 329 BGA Package

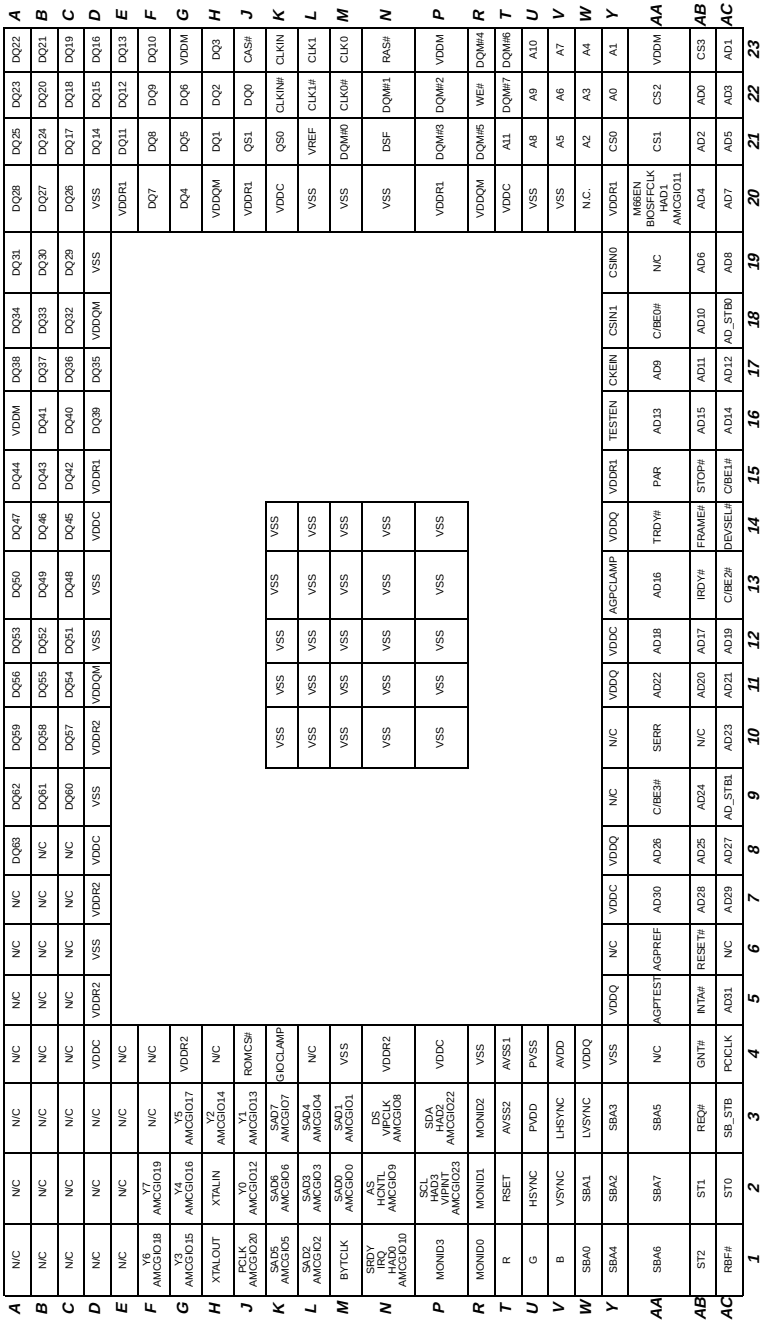


Figure 3-3 Top View of the 329 BGA Package

3.3 AGP/PCI Bus Interface

Table 3-2 AGP/PCI Bus Interface

Pin Name	Type	Description
AD[31:0]	I/O	Multiplexed — System address or data bits [31:0]
PCICLK	I	Bus Clock
RESET#	I	Bus Reset
IRDY#	I/O	Initiator Ready — Indicates the bus master is able to complete the current data phase of the transaction
FRAME#	I/O	Frame is driven by the current bus master to indicate the beginning and duration of an access
TRDY#	I/O	Target Ready — Indicates the target agent is able to complete the current data phase of the transaction
DEVSEL#	I/O	Device Select — When driven active “Low”, it is indication that the controller has decoded its address. Not used by AGP
STOP#	I/O	Stop — Indicates the current target is requesting the master to stop the current transaction. Not used by AGP
PAR	I/O	Parity — Even parity used (expand on parity detection)
C/BE#[3:0]	I/O	Multiplexed — Bus Command or Byte Enable bits 3:0. (BE# is active low)
INTA#	O	Interrupt Request — Level triggered. Active “Low” by default
REQ#	I/O	Request — Indicates to the chip set that there is request for bus master cycle
GNT#	I	Grant — Indicates to the agent that a bus access has been granted
*SB_STB	I/O	Sideband Strobe for AGP 1X/2X support
*ST[2:0]	I	Status bus — Provides information from the arbiter to the master on what it may do
SBA[7] **or** IDSEL	I/O	AGP Sideband Address Port bit 7 **or** PCI initialization device select (in PCI mode)
*SBA[6:0]	O	Sideband Address Port for AGP 1X/2X support
*RBF#	O	Read Buffer Full — Indicates when the master is ready to accept previously requested low priority read data
*AD_STB[1:0]	I/O	AGP-133 Address Strobe —- provides tuning for 2x data transfer
AGP_BUSY# **or** CLKRUN[a]	I/O	Power management input signal for AGP **or** PCI bus

Table 3-2 AGP/PCI Bus Interface (Continued)

Pin Name	Type	Description
*STP_AGP#[b]	I/O	Power management input signal for AGP bus
AGPIO[3:2][c]	I/O	Not used (reserved for future AGP4x support)

Footnotes:

a. For AGP or PCI bus respectively. Named SB_STB# when used for future AGP4x support.
b. Named WBF# when used for future AGP4x support.
c. Named AD_STB1# and AD_STB2# when used for future AGP4x support.
* Pins preceded with * are AGP-only. For PCI implementations, all such pins should be no connects (i.e., open).

3.4 Memory Interface

Table 3-3 Memory Interface

Pin Name	Type	Description
DQ[63:0]	I/O	Memory Data Bus
DQ[127:64]	I/O	Memory Data Bus
DQM#[7:0]	O	Byte enables
DQM#[15:8]	O	Byte enables
A[11:0]	O	Memory Address Bus
CS[3:0]	O	Chip selects
QS[1:0]	I	Read Strobes
RAS#	O	Row Address Select
CAS#	O	Column Address Select
WE#	O	Write enable
DSF	O	DRAM special function
CLK0*	I/O	Memory clock 0
CLK0#*	I/O	Memory clock 0 bar
CLK1*	I/O	Memory clock 1
CLK1#*	I/O	Memory clock 1 bar
VREF**	I	Reference voltage for DDR

* Refer to Layout Considerations in Design Guide for handling of these bi-directional traces.
** For more details on the electrical requirements for this pin, refer to *Section 6.1.6 on page 6-3*

3.5 Monitor Interface

Table 3-4 Monitor Interface

Pin Name	Type	Description
R	A-O	Red analog current output. Can drive a doubly terminated 75Ω line
G	A-O	Green analog current output. Can drive a doubly terminated 75Ω line
B	A-O	Blue analog current output. Can drive a doubly terminated 75Ω line
HSYNC	O	Horizontal Sync for monitor
VSYNC	O	Vertical Sync for monitor
MONID[3:0]	I/O	DDC pins / AppleSense

3.6 PLL and Crystal Interface

Table 3-5 PLL and Crystal Interface

Pin Name	Type	Description
XTALIN	I	PLL reference clock or MXCLK source (3.3 V or 2.5 V input level)
XTALOUT	O	PLL reference clock
PVDD	Pwr	Phase Lock Loop power (2.5 V)
PVSS	Gnd	Phase Lock Loop (PLL) ground

3.7 Multimedia Port Interfaces

Pins in this group are multiplexed which means they have different names depending on the selected interfacing mode (see *Table 3-7* Multimedia Configuration Options on page 3-10). The second name in brackets applies to the cases in which the pins are used as General Purpose I/O pins.

Table 3-6 Multimedia Port Interface

Pin Name	Type	Description
SAD[3:0] (AMCGIO[3:0])	I/O	Address / data for MPP bits [3:0]
SAD[7:4] / HAD[7:4] (AMCGIO[7:4])	I/O	Address / data for MPP **or** VIP host data bits [7:4]
DS / VIPCLK (AMCGIO[8])	I/O	MPP data strobe **or** VIP host clock
AS / HCNTL (AMCGIO[9])	I/O	MPP address strobe **or** VIP host control
SRDY/ IRQ / HAD[0] (AMCGIO[10])	I/O	MPP ready / interrupt **or** VIP host data bit [0]
M66EN / Biosffclk / HAD[1] (AMCGIO[49])	I/O	Bus_clk_sel strap / Clock for eprom flops / VIP host data bit 1
PDATA[7:0] (AMCGIO[38:31])	I	DVS / ITU656 / ZV data in
PCLK (AMCGIO[39])	I/O	DVS / ITU656 / ZV clock in
UV[7:0] / (AMCGIO[18:11])	I	Extended VIP / DVS port / ZV data in
ZVHREF / PCLK_1 (AMCGIO[19])	I	ZV control port **or** PCLK_1 for second DVS port
ZVVSYNC (AMCGIO[20])	I	ZV control port
BYTCLK (AMCGIO[40])	I/O	Bytclk for ImpacTV or RAGE THEATER used on MPP1 or MPP2
SDA / HAD[2] (AMCGIO[41])	I/O	I^2C data in/out / VIP host data bit 2
SCL / HAD[3] / VIPINT (AMCGIO[42])	O	I^2C clock out / VIP host data bit 3 / VIP Interrupt

The next two tables show the different possibilities for multimedia interface.

Table 3-7 Multimedia Configuration Options

Pin Name	MPP1 Port	DVS Port	I²C	Extended Functionality	
				Multimedia	Second Order[a]
PDATA[7:0] (AMCGIO[19:12])		YUV[7:0]	*	*	*
PCLK (AMCGIO[20])		CLK	*	*	*
SAD[3:0] (AMCGIO[3:0])	SAD[3:0]	*	*	*	*
SAD[7:4] (AMCGIO[7:4])	SAD[7:4]	*	*	HAD[7:4] VIP Host Data (8 bit VIP)	*
SIOW (AMCGIO[8])	SIOW (DS)	*	*	VIPCLK VIP Host Clk	*
SIOR (AMCGIO[9])	SIOR (AS)	*	*	HCNTL VIP Host Cntl	*
SRDY (AMCGIO[10])	SRDY / IRQ	*	*	HAD[0][b] VIP Host Data (2, 4, or 8 bit VIP)	*
BYTCLK (AMCGIO[21])	BYTCLK (TVout) for MPP1or MPP2	*	*	Bytclk for MPP2	*
SDA (AMCGIO[22])	*	*	I²CDATA	HAD[2] VIP Host Data (4, or 8 bit VIP)	*
SCL (AMCGIO[23])	*	*	I²CCLK	HAD[3] VIP Host Data (4, or 8 bit VIP)	VIPINT (optional VIP interrupt)
UV[7:0] (AMCGIO[15:8])	*	*	*	Extended VIP (or ZV, or second DVS) Muxed on upper memory data bits	*
ZVHREF (AMCGIO[6])	*	*	*		*
ZVVSYNC (AMCGIO[7])	*	*	*		*

Table 3-7 Multimedia Configuration Options (Continued)

Pin Name	MPP1 Port	DVS Port	I²C	Extended Functionality	
				Multimedia	Second Order[a]
SSAD[7:0] (AMCGIO[31:24])	*	*	*	Second MPP for TVout. Muxed on upper memory data bits	*
SDS (AMCGIO[22])	*	*	*		I²CDATA
SAS (AMCGIO[23])	*	*	*		I²CCLK
M66EN (AMCGIO[11])	*	*	*	HAD[1] VIP Host Data (2, 4, or 8 bit VIP)	*

General Notes:

- Any extra pins not used (indicated by *) in a particular mode can be used as a general purpose I/O pins GPIO.
- The Multimedia peripheral port MPP1 can be used in conjuction with the DVS (Bt, Philips,...) and I²C port.
- There is only one Bytclk pin for both MPP1and MPP2. Bytclk is only used for ImpacTV / RAGE THEATER and it will be used in conjunction with MPP1or MPP2 depending on which MP port the ImpacTV / RAGE THEATER chip is connected to.

Footnotes:

a. If the use of a VIP Interrupt pin is necessary, then the I2CCLK (AMCGIO(23)) pin will be used as the VIP interrupt pin, and the I2CCLK functionality can be supported through the SAS (AMCGIO(23)) pin, or the whole I²C functionality will be supported through the RAGE THEATER chip. An alternative pin is provided for the I2CDATA through the SDS (AMCGIO(22)) pin in case the default I2CDATA pin needs to be used for another functionality (VIP 4 bits).

An automatic VIP interrupt polling scheme is also being implemented in the RAGE 128. Once proven functional, this scheme should eliminate the need for a VIP Interrupt pin. Note that currently, the VIP interrupt pin would not be available in a VIP 4 Bit implementation.

b. The detection of the presence of a VIP device on the board is done by the RAGE 128 detecting whether bit HAD(0) is pulled low (by the VIP device) during reset (refer to the VIP protocol for further details).

Table 3-8 Capture Port Pin Multiplexing

Pin Name	ZV, Philips Port		ITU-656 Double Input Port		Extended VIP (16 bits) Video in	
	Signal Name	Direction	Signal Name	Direction	Signal Name	Direction
PDATA[0]	Y0	In	YUV0_0	In	YUV0_0	In
PDATA[1]	Y1	In	YUV0_1	In	YUV0_1	In
PDATA[2]	Y2	In	YUV0_2	In	YUV0_2	In
PDATA[3]	Y3	In	YUV0_3	In	YUV0_3	In
PDATA[4]	Y4	In	YUV0_4	In	YUV0_4	In
PDATA[5]	Y5	In	YUV0_5	In	YUV0_5	In
PDATA[6]	Y6	In	YUV0_6	In	YUV0_6	In
PDATA[7]	Y7	In	YUV0_7	In	YUV0_7	In
PCLK	PCLK	In	PCLK_0	In	PCLK	In
UV[0]	UV0	In	YUV1_0	In	YUV0_8	In
UV[1]	UV1	In	YUV1_1	In	YUV0_9	In
UV[2]	UV2	In	YUV1_2	In	YUV0_10	In
UV[3]	UV3	In	YUV1_3	In	YUV0_11	In
UV[4]	UV4	In	YUV1_4	In	YUV0_12	In
UV[5]	UV5	In	YUV1_5	In	YUV0_13	In
UV[6]	UV6	In	YUV1_6	In	YUV0_14	In
UV[7]	UV7	In	YUV1_7	In	YUV0_15	In
ZVHREF	ZVHREF	In	PCLK_1	In		
ZVVSYNC	ZVVSYNC	In				

The diagram below shows the recommended interconnection between the RAGE 128 and various peripheral devices.

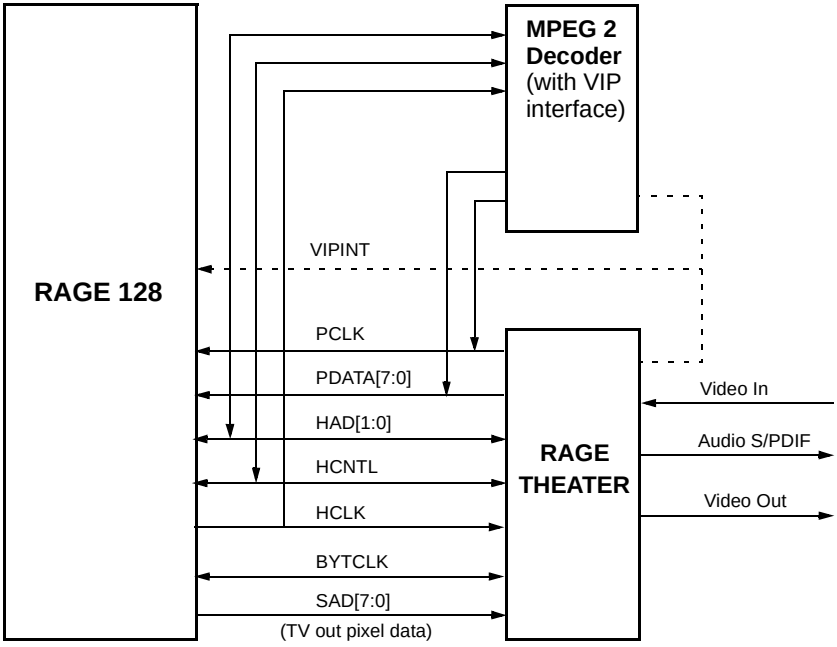


Figure 3-4 RAGE 128 Interconnection Example

3.8 MPP2 (for ImpacTV) Interface

Table 3-9 MPP2 Interface

Pin Name	Type	Description
SSAD[7:0] [a]	I/O	Address/data for MPP2
SDS / SDA[b]	I/O	MPP2 data strobe **or** I^2C data in/out
SAS / SCL[c]	I/O	MPP2 read/address strobe **or** I^2C clock out

a. Also named AMCGIO[28:21]
b. Also named AMCGIO[29]
c. Also named AMCGIO[30]

3.9 Testing Pin

Table 3-10 Testing Pin

Pin Name	Type	Description
TESTEN	I	Test enable

3.10 DAC Interface

Table 3-11 DAC Interface

Pin Name	Type	Description
AVDD	Pwr	DAC VDD (2.5 V)
AVSS	Pwr	DAC VSS
AVSS	Pwr	Band Gap Ref. VSS
RSET	A-O	Internal DAC reference

3.11 BIOS ROM Interface

Table 3-12 BIOS ROM Interface

Pin Name	Type	Description
ROMCS#	O	BIOS ROM Chip Select

3.12 Clamp Pins

Table 3-13 Clamp Pins

Pin Name	Type	Description*
AGPCLAMP	I	Clamp for 5 V tolerance and signal integrity on PCI For more details, refer to Appendix C.
GIOCLAMP	I	Clamp for 5 V tolerance and signal integrity on GIOs For more details, refer to Appendix C.

* For more details on these pins, please refer to *Section 6.1.7 on page 6-4* and *Appendix C.*

3.13 Power and Ground Pins

Table 3-14 Power and Ground Pins

Pin Name	Quantity 272 / 328	Type	Description
VDDQ	4 / 4	Pwr	PCI/AGP I/O power: 3.3 V
VDDR1	5 / 4	Pwr	Memory: 2.5 V or 3.3 V
VDDR2	3 / 2	Pwr	Memory / Multimedia GIO: 2.5 V or 3.3 V
VDDR3	0 / 2	Pwr	Multimedia GIO: 3.3 V
VDDC	4 / 4	Pwr	Core power: 2.5 V
VSS	24 / 28	Gnd	Common core, I/O ground

Table 3-15 Power Pin Voltage Levels

Pin	64-Bit Memory and Multimedia Interface	128-Bit Memory Interface
VDDC	2.5 V	2.5 V
VDDQ	3.3 V	3.3 V
VDDR1	2.5 (3.3) V	2.5 (3.3) V
VDDR2	3.3 V	2.5 (3.3) V
VDDR3	N/A	3.3 V

Chapter 4
Functional Blocks, Interfaces and Straps

This chapter describes the major subsystems and interfaces of the RAGE 128 VR/GL. The diagram below shows the major functional blocks of the chip.

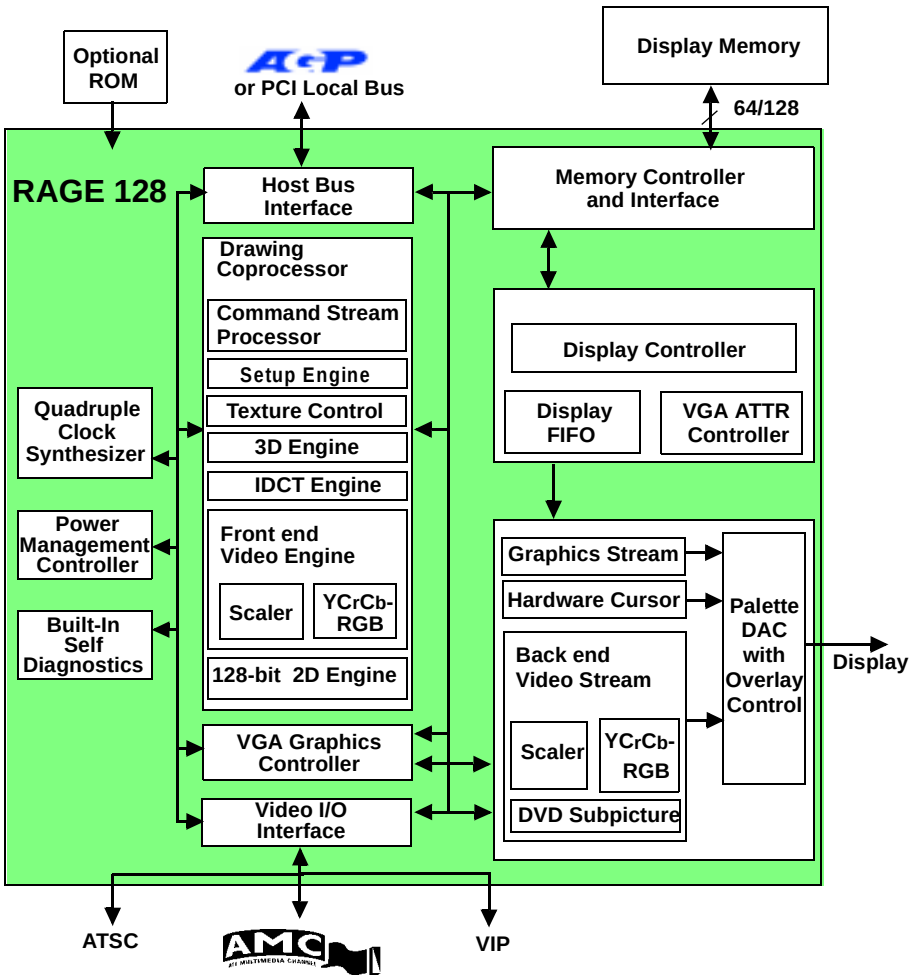


Figure 4-1. RAGE 128VR/GL Functional Block Diagram

4.1 3D Graphics Coprocessor

The 3D graphics coprocessor offers a number of orthogonal pixel processing features associated with the rendering of 3D images. These coprocessor functions were chosen to accelerate features of all of Microsoft's Direct 3D, OpenGL ICD, and Apple's QuickDraw 3D RAVE interfaces. Drivers including OpenGL ICD will be available for all major operating systems and APIs (see *"Software Support" on page 2-18*).

RAGE 128 VR/GL include a triangle setup engine, which needs only color, alpha, Z, U and V information at vertices of triangles to successfully draw Gouraud shaded, or perspectively correct texture mapped triangles. The setup engine significantly reduces the CPU load in 3D graphics applications, giving applications more CPU time to perform non-setup related tasks.

Pixels to be displayed can be further modified by alpha blending with pixels in the destination, by fogging pixels with a fog color, and in the case of texture mapping, by lighting them and by LOD biasing. Depth buffering is achieved by associating a 16, 24, or 32-bit Z value with each pixel. The Z, alpha, and fog color for each new pixel is supplied from interpolators within the 3D coprocessor. In case of texture mapping, the alpha factor may even be stored in the texture map on a pixel-by-pixel basis.

Pixels in the 3D coprocessor are always operated on as 24-bit entities (8 bits each of Red, Green, and Blue). Other pixel sizes, i.e., 8-bit and 16-bit, are dithered by the 3D graphics subsystem to output at the desired pixel size.

The 3D coprocessor contains a powerful texture mapping engine. This engine takes a series of precomputed maps (mip maps) and selects texels from these maps in a way that allows them to look perspectively correct. Texels can be filtered in a number of ways, and then lit (lightened or darkened). Once the texel is formed by filtering and lighting, any of the pixel processing modes mentioned previously can be applied to the texel.

An 8K texture cache greatly reduces the memory bandwidth needed to support texture mapping.

With AGP support, texture maps can be stored in system memory and pulled into the local texture cache as needed. This rids the system of the need to add significant amount of local frame buffer memory in order to support multiple detailed texture maps, and allows applications to support a richer and more realistic environment.

4.2 2D Engine

The RAGE 128 VR/GL 2D engine is a fixed-function subunit that runs concurrently with the host processor. It incorporates full ROP3 (Pattern/Src/Dst) support and is capable of drawing both rectangle and line draw primitives. A sophisticated pixel datapath (128-bits wide drawing multiple pixels per clock) allows monochrome to two-color expansion, fast solid color fills (via block writes), patterned fills, and host-to-screen transfers.

2D Engine features summary:

- Support of up to 64MB virtual address (lower 32 is frame buffer, upper AGP).
- Full ROP3 support (Pattern/Src/Dst).
- Patterns (8x8 color/mono brushes, 32x1 mono pens for lines).
- Rectangle and line trajectories.
- 128-bit datapath (multiple pixels generated per clock), 8/15/16/24/32 bpp support.
- Colorcmp on both src/dst channels.
- Colorcmp flip.
- Blockwrite support for solid fills in tiled/non-tiled memory.
- Interrupt support.
- Multimedia event triggers.
- Quick engine setup.
- A four-function simultaneous source/destination color compare for transparent blits, bit masking, and scissoring.

4.3 DVD Subpicture Decoder and Scaler

The RAGE 128 VR/GL includes a DVD subpicture decoder and scaler with the following features:

- Subpicture Decoder:
  - Operates on 2 bpp and produces YUV444 and K.
  - Compliant to DVD specifications.
  - Button support.
  - Maximum source width: 720 pixel.s
- Subpicture Scaler:
  - Operates on YUV444 and K from the subpicture decoder.
  - 2-tap vertical up/down scaling.
  - 2-tap horizontal up/down scaling.
  - Subpicture can be shifted anywhere within the overlay window.
  - Allows pixel replication or blending.
  - Supports “bob and weave”.

4.4 IDCT Engine

RAGE 128 VR/GL incorporate an integrated IDCT (Inverse Discrete Cosine Transform) engine as well as motion compensation (MC) support for the acceleration of MPEG decoding. The acceleration hardware is fed directly from an advanced packet parsing engine, enabling high processing rates with minimal software overhead.

Using the advanced packet parsing engine also increases the parallelism between the hardware and software which ensures that the most is made of the host processor’s power. This combination of hardware acceleration decreases the loading on the host processor to significantly below that of past MC-only engines, and enables quality software DVD playback on processors which, until now, had relied on dedicated hardware decoders. It can also provide acceleration for decode of HD0 level bitstreams.

The IDCT engine implements an IEEE 1180 compliant IDCT algorithm which, when combined with a run/level and dezig-zag formatter, off-loads a significant portion of the MPEG decoding process from the host processor. Run/level codes are combined with

control words by the host processor in a packetized format, which the advanced packet parsing engine bus masters down from system memory over the AGP bus. The run/level codes are expanded and then dezig-zagged before being fed into the IDCT engine. Dezig-zagging is selectable through the register interface. There is also selection for intra/non-intra block support. The IDCT engine takes the dezig-zagged coefficients and performs a 2-D IDCT before buffering the result and sending it to the MC hardware.

The MC hardware allows for implementation of all motion compensation modes required for MPEG-2 support. It fetches data from the frame buffer based on control information supplied by the advanced packet parsing engine on a macroblock basis, combines the data from the frame buffer with the output of the IDCT engine through a full 9-bit signed adder, and then writes the result back to the frame buffer.

4.5 Display System

The RAGE 128 VR/GL display system supports VGA, VESA super VGA, and accelerator mode graphics display. The full features are outlined below:

4.5.1 Extended VGA Graphics Controller

- Fully register compatible with VGA standard.
- BIOS compatible with VESA super VGA.
- Includes support for text modes up to 132 columns.
- Enhanced VGA refresh rates up to 85 Hz.

4.5.2 CRT Controller (CRTC)

- The CRTC subsystem supports standard display resolutions up to 1920x1440. For higher resolutions, or non-standard modes, contact ATI.
- Produces synchronization signals to allow the drawing engines to synchronize with the display raster or frame.
- Display buffer flips (front and back buffer) are synchronized with the drawing engines, and can occur on either vertical (normal) or horizontal retraces.
- Frame rate monitoring and adjustment logic to allow frame rate locking to video broadcasts (GEN-locking).
- Support for both interlaced and non-interlaced display.

- Up to 200 Hz vertical refresh rate.
- Support for overscan and double scan.
- Separate or composite horizontal and vertical sync generation.
- Optional hardware interrupt generation on CRTC events.

4.5.3 Accelerated Graphics Display

- Supports 4 bpp and 8 bpp indexed color modes, and 15, 16, 24 and 32 bpp true color modes.
- Gamma correction in all modes (triple 256x8 palette).
- Per-pixel keying for video overlay, and multiple key mix functions.
- Hardware cursor up to 64x64x2 bpp. XGA compatible, with two solid colors, transparent, and inverse transparent.
- Support for 32MB frame buffer, in either linear or tiled modes.
- Large FIFO for improved memory efficiency.

4.5.4 Video Scaler/Overlay

- Surface formats supported: RGB1555, RGB565, RGB8888, Planar YUV9, YUV12, Packed YUYV, UYVY.
- Four-tap horizontal filtering on all color components.
- Four-tap vertical filtering on all color components.
- Four-tap filters adaptively programmed to the optimal filter for the scaling ratio.
- When downscaling, the scaler can read in up to four lines and blend them together to produce a single output line. This means that up to 25% vertical reduction without line dropping is possible (50% only in RGB565 and RGB1555).
- The scaler can add black borders for DVD letterboxing and then composite the subpicture on top of the black.
- The scaler can zoom in with subpixel windowing accuracy.
- The scaler can pan-and-scan for DVD.
- When the video window is cropped by the desktop, it can be updated (a register locking mechanism allows autonomous updates of the overlay characteristics) without any artifacts thanks to sufficient double buffering of scaler control register fields. Double buffering can be disabled.
- Supports either capture port or an application as a video provider.

- Can either bob fields (with vertical shift on either field) or weave two fields together in a variety of styles designed to eliminate motion artifacts, including styles optimal for films provided via NTSC and PAL video standards, and viewing freeze frame on a VCR.
- Quad 768-pixel line buffer for up to 4 tap vertical scaling.
- Double wide source mode to allow ATSC standards widths.
- Enhanced YUV to RGB conversion.
- Enhanced de-interlacing.
- Optional per-pixel video keying for mixing with graphics.
- Ability to overlay 24 bpp video in any graphics bit depth (4/8/15/16/24/32).
- Window controller for per-pixel alignment and scaling of video window.

4.5.5 Display Output

- Standard analog VGA CRT output using integrated triple 8-bit DACs with built-in reference circuit.
- Up to 250 MHz pixel clock.
- Analog monitor detection with integrated DAC comparators.
- Support for DDC1 and DDC2B+. Also AppleSense compatible.
- Digital interface to external video encoder for NTSC or PAL signal generation. Can use ATI ImpactTV1/2, or RAGE THEATER parts.
- Digital frame based CRC generator for testing of display system output.

4.6 Analog Output Section

Load each of the R, G, B lines on the board (see *Figure 4-2.*) with a 75 Ω resistor. To protect the controller from any large transient voltages that may enter from the connector when a monitor is connected, install protection diodes.

To filter the output, install bypass capacitors on all lines. In order to comply with FCC Class B requirements for radio frequency emissions, you may need to install inductors (ferrites) in series on the RGB line. The proper value is determined as a trade-off between filtering the signals for FCC requirements and video signal clarity. For more details, see the Reference Schematics.

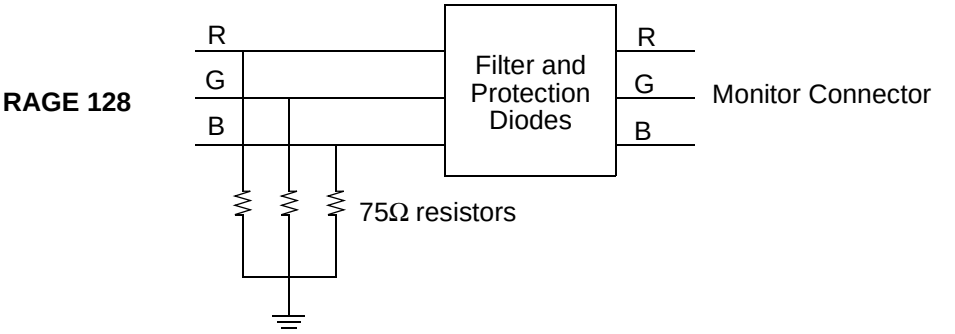


Figure 4-2. Analog Output

4.7 Quadruple Clock Synthesizer

The internal clock synthesizer consists of four independent phase locked loops (PLLs) capable of synthesizing any frequency up to 250 MHz. All PLLs have been optimized for low jitter graphics applications.

- The first PLL generates clocks for the display system. This PLL is reprogrammed by the BIOS or driver for each display mode.
- The second PLL generates the clock for the 2D, 3D and IDCT engines.
- The third PLL generates the clock for the memory (independent from the drawing engines).
- The fourth PLL is used to generate the internal 2x clock for AGP 2x operation and the internal 1x clock for PCI-66 and AGP 1x operations.

4.8 ATI Multimedia Channel (AMC) Interface

4.8.1 DVS Mode

Digital Video Stream Mode supports a direct connection to MPEG decoders such as the IBM-CD11, and video decoders such as Brooktree Bt829, Bt827, Bt819, Bt817, or Bt815, and Philips SAA7111/2.

The DVS video capture port has the following features:

- Support of simultaneous capture of two video streams.
- Support of video stream format of BT Byte Stream, CCIR656, VIP1.1, VIP2.0, and Zoom Video.
- Capable of video data capture rate up to 75 MHz with resolution 1920x1152.
- Hardware support for “bob and weave” and single field video capture.
- Hardware support for 3:2 pull down.
- Hardware support for VBI data capture.
- Hardware support for ANC data block capture.
- Hardware support of video mirroring during capture.
- Horizontal and vertical scaling on incoming video at arbitrary ratios up to 16.
- Hardware support for single, double, triple, and quadruple buffering for video capture.
- Hardware support of Signed UV format.
- Hardware interrupt support for video capture.

Support for VFC has been removed due to the sharp decline in VFC peripherals.

4.8.2 MPP Mode

Multimedia Peripheral Port Mode can stream data either from the host memory out of this port, or from this port to the system memory. Both data streams can be handled through bus mastering, thus minimizing software overhead. Timing and protocol can be programmed to support different peripheral chips. By connecting this port to an external NTSC/PAL encoder, the display screen can be modulated to an NTSC/PAL signal.

4.8.3 I^2C Bus

The I^2C is an industry standard 2-bit serial bus. Implemented through the AMC, the I^2C interface allows programming of peripherals such as video decoders, TV tuners, teletext decoders, and volume control.

Two dedicated signals, I2CCLK and I2CDATA, are used to drive the AMC I^2C pins. The I^2C data transfer can be done in two modes, the software mode or the hardware-assisted mode. In general, software controlled I^2C has higher flexibility, but yields a lower throughput because of the time involved in programming the GPIOs.

Since the I^2C clock and data are open-collector signals and rely on external pull-up resistors, noise can be a factor during transition from low to high. The I^2C in RAGE 128 VR/GL can be programmed such that I^2C signals can either be driven high directly, or be pulled up by the external pullup resistor as before. Note that the driving of I2CCLK and I2CDATA signals is controlled separately, as this eliminates any potential problem when only one of the signals is desired to be driven high.

4.9 Video Interface Port (VIP)

VESA Video Interface Port (VIP) is a new multimedia bus capable of supporting a maximum of four slave devices with the graphics chip being the sole master. The bus can be configured to use 2-bit or 4-bit data width and run up to a maximum of 33 MHz clock speed.

In RAGE 128 VR/GL, up to four busmaster channels can be supported and each channel is set to run in either direction, i.e, system to VIP devices or VIP devices to system memory. During FIFO burst mode, it is possible for the VIP driver to do a VIP register access without having to change the operating mode. Arbitration between register and FIFO transfer is hidden in the hardware. In addition, the VIP controller is capable of doing byte-aligned and dword aligned transfers, automatic interrupt polling, automatic FIFO port polling, and detect VIP slave timeout.

4.10 Host Bus Interface

The Host Bus interface supports both AGP 2.0 and PCI 2.1 standards. Support for AGP is by sideband addressing mode. Texture map data for 3D objects can be obtained directly from system memory. Similarly the AGP can be used to accumulate MPEG-2 playback. In these applications, AGP fetches are execute-mode fetches.

The AGP function supports pipelined reads, long reads, and writes of varying lengths. All throttling is done in a way to prevent the bus from being waitstated. The AGP function supports 1x and 2x data transfers.

With PCI 2.1, functions such as bus control, data flow control, address/data signal generation, signal timings, and address decoding are supported. Data flow control is enhanced by a 6x64-bit write-through FIFO available in both VGA and direct memory modes.

The controller achieves zero wait-state memory read/write burst cycles with burst access. It also supports Block I/O decoding and DAC palette snooping, and a separate aperture for accessing registers.

Bus mastering functions between (1) system memory and frame buffer, (2) system memory and MPP and VIP, and (3) system memory and GUI engine, allow all data transfer operations to be off-loaded from the host processor onto the motherboard chip set. The bus master function concurrently performs transfers on nine buffered channels, moving a “programmable amount” at a time from each of them, to prevent the other channels from starving. It also selects the highest available transfer protocol (PCI or AGP) to use for each of the channels, and arbitrates between them.

4.10.1 AGP Bus Interface

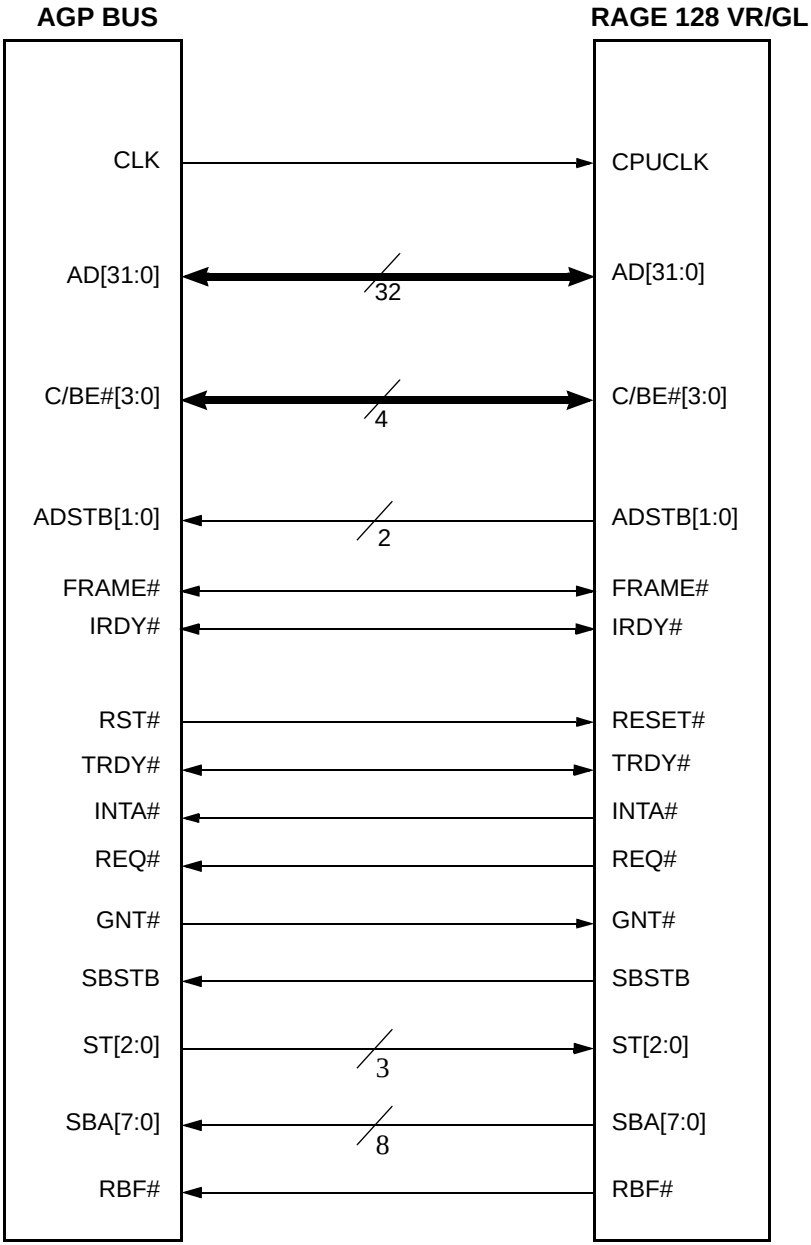


Figure 4-3. AGP Bus Configuration

4.10.2 PCI Bus Interface

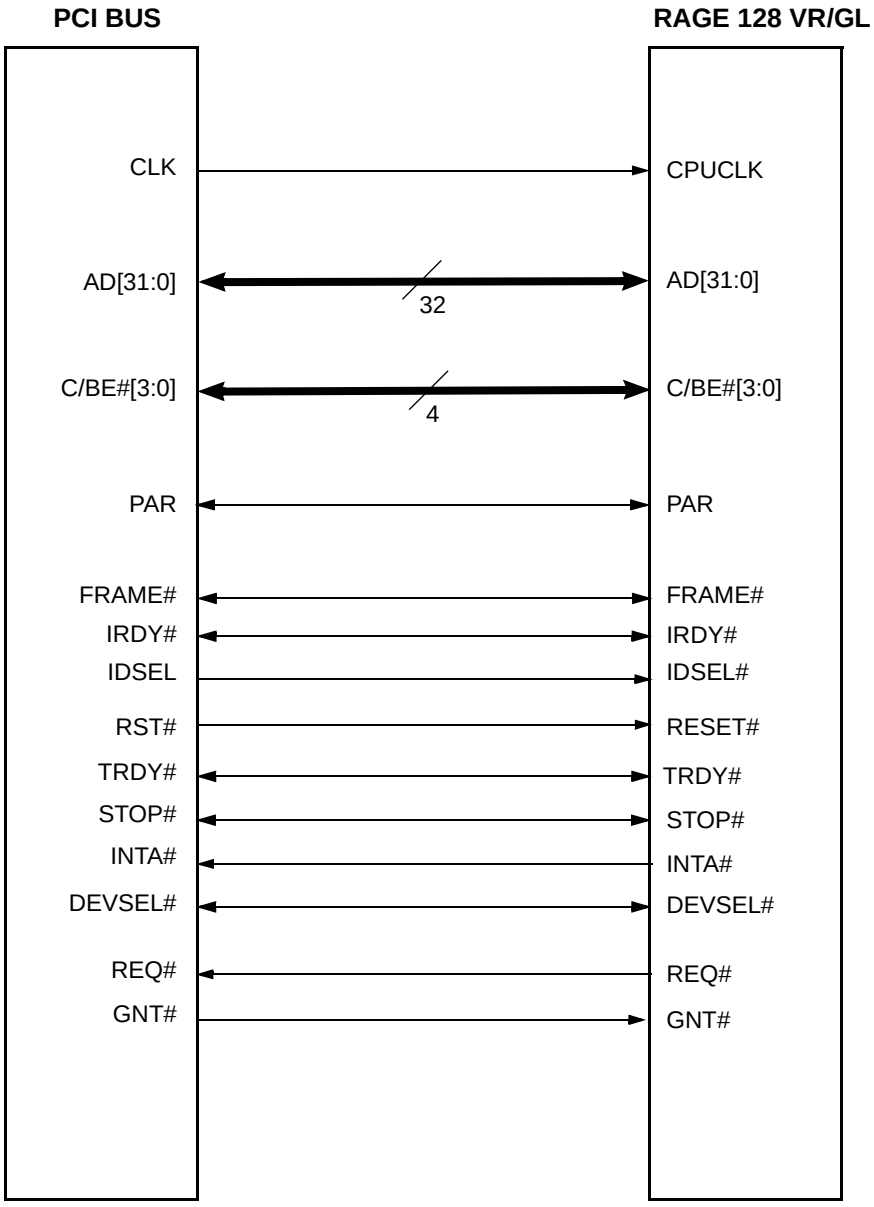


Figure 4-4. PCI Bus Configuration

4.11 Memory Interface

The memory controller subsystem arbitrates requests from the VGA graphics controller, the drawing coprocessor, the display controller, the video scaler, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

4.11.1 Memory Configurations

The memory interface supports both full 128-bit and 64-bit path. Memory configurations range from 2MB to 32MB (see tables below).

The following memory types are supported: SGRAM SDR (block-write support), SGRAM DDR and SDRAM SDR.

SGRAM SDR

The targeted timing for SGRAM SDR is:

- 64 bits SDR at 143 MHz (max) and SSTL-3 (3.3 V) levels, or 125 MHz (max) in LVTTL.
- 128 bits SDR at 125 MHz (max) and LVTTL (3.3 V) levels.

The tables below list the supported SGRAM SDR configurations, and the number of memory parts required:

Table 4-1 SGRAM SDR Support

Memory Size Mbit	Configuration	Row x Column bits	64-bit Granularity	128-bit Granularity
8	128K x 32 x 2	10 x 8	2MB	4MB
16	256K x 32 x 2	11 x 8	4MB	8MB

SGRAM DDR

Targeted timing: 64 bits DDR at 125 MHz (max) and SSTL-2 (2.5 V) levels.

The table below lists the supported SDRAM DDR configurations, and the number of memory parts required:

Table 4-2 SGRAM DDR Support

Memory Size Mbit	Configuration	Row x Column bits	64-bit Granularity	128-bit Granularity
16	128K x 32 x 4	11 x 8	4MB	n/a
16	128K x 32 x 4	12 x 7	4MB	n/a
32	256K x 32 x 4	12 x 8	8MB	n/a
32	256K x 32 x 4	13 x 7	8MB	n/a

SDRAM SDR (Main Memory)

The targeted timing for SDRAM SDR is:

- 64 bits SDR at 143 MHz (max) and SSTL-3 (3.3 V) levels
- 128 bits SDR at 125 MHz (max) and LVTTL (3.3 V) levels

The tables below list the supported SDRAM SDR configurations, and the number of memory parts required:

Table 4-3 SDRAM SDR (Main Memory) Support

Memory Size Mbit	Configuration	Row x Column bits	64-bit Granularity	128-bit Granularity
16	512K x 16 x 2	12 x 8	8MB	16MB
64	1M x 32 x 2	13 x 8	16MB	32MB
64	512K x 32 x 4	13 x 8	16MB	32MB
64	2M x 16 x 2	14 x 8	32MB	n/a
64	1M x 16 x 4	14 x 8	32MB	n/a

4.11.2 8Mbit (10x8) Single Data Rate (SDR) SGRAM Interface

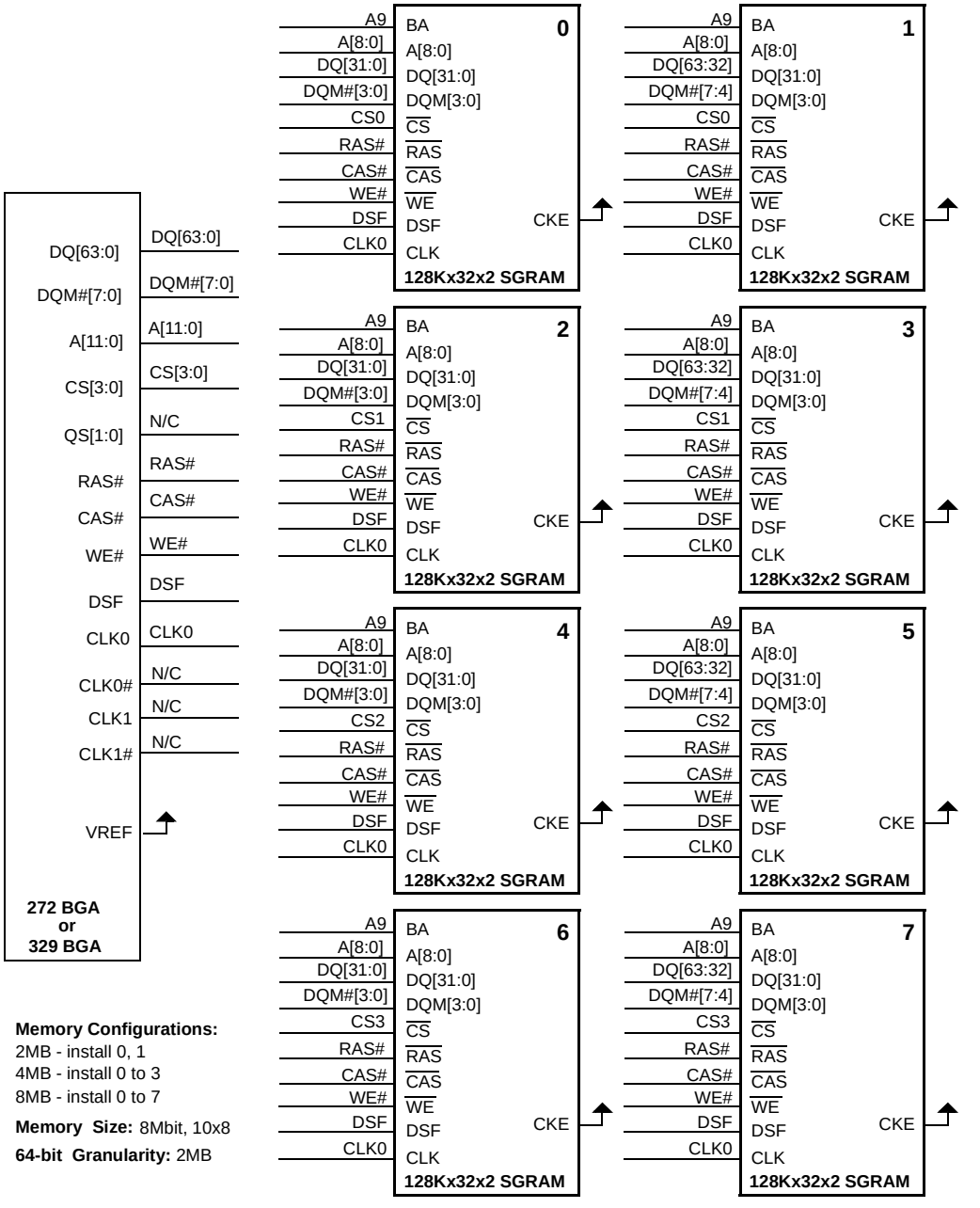


Figure 4-5. 8Mbit (10x8) SDR SGRAM Implementation for 272/329 BGA Packages

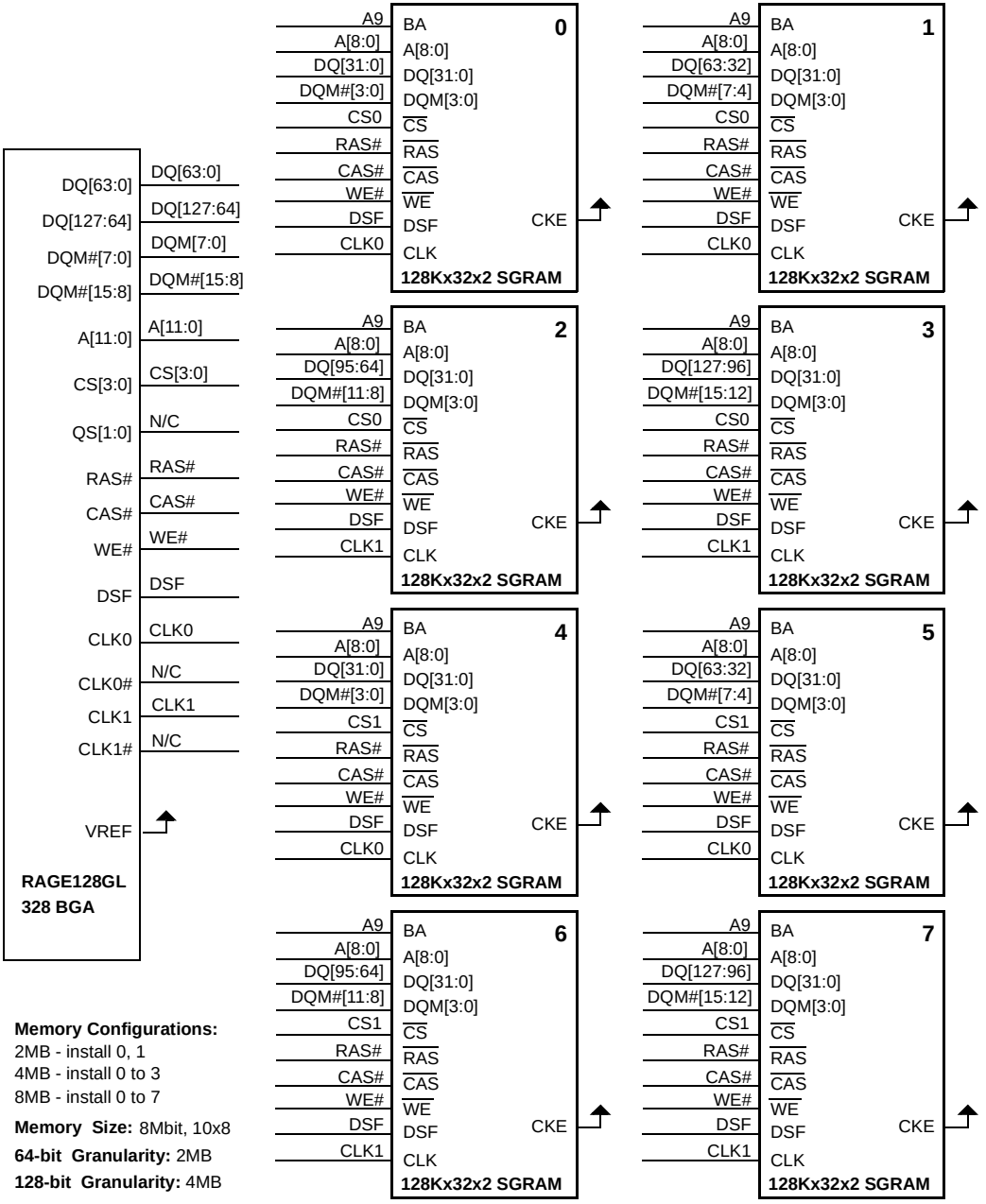


Figure 4-6. 8Mbit (10x8) SDR SGRAM Implementation for 328 BGA Package

4.11.3 16Mbit (11x8) Single Data Rate (SDR) SGRAM Interface

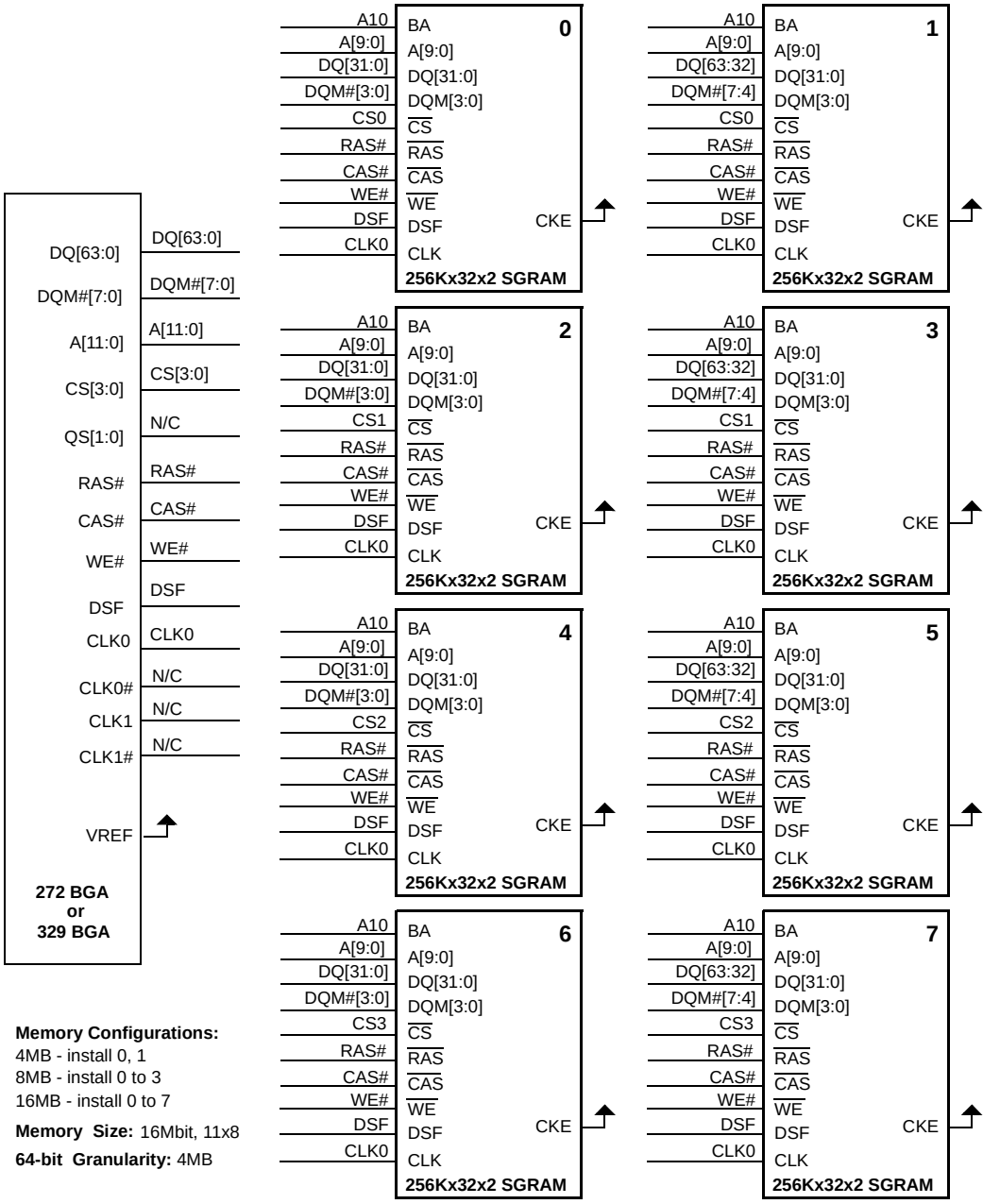


Figure 4-7. 16Mbit (11x8) SDR SGRAM Implementation for 272/329 BGA Packages

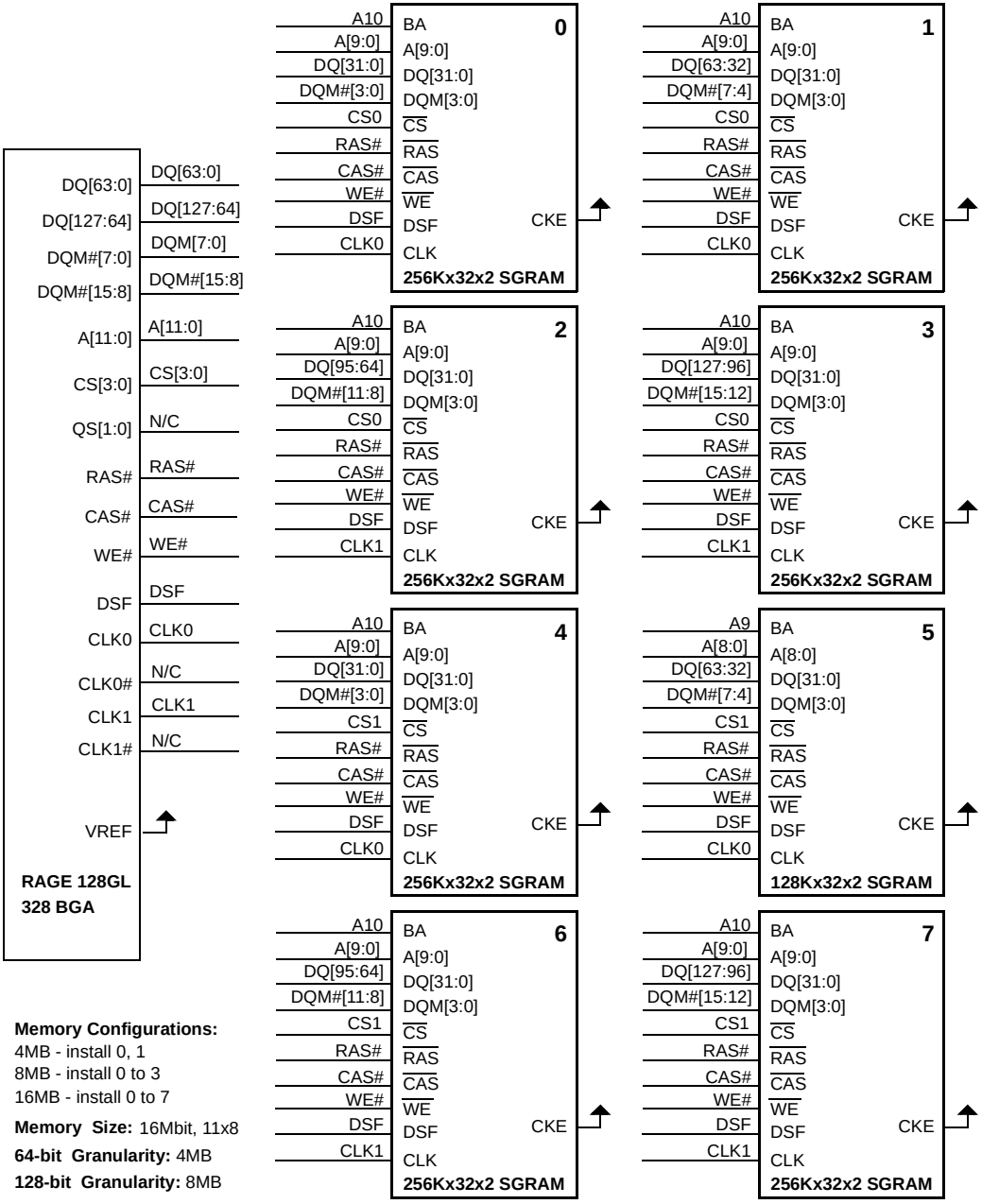


Figure 4-8. 16Mbit (11X8) SDR SGRAM Implementation for 328 BGA Package

4.11.4 16Mbit (11x8) Double Data Rate (DDR) SGRAM Interface

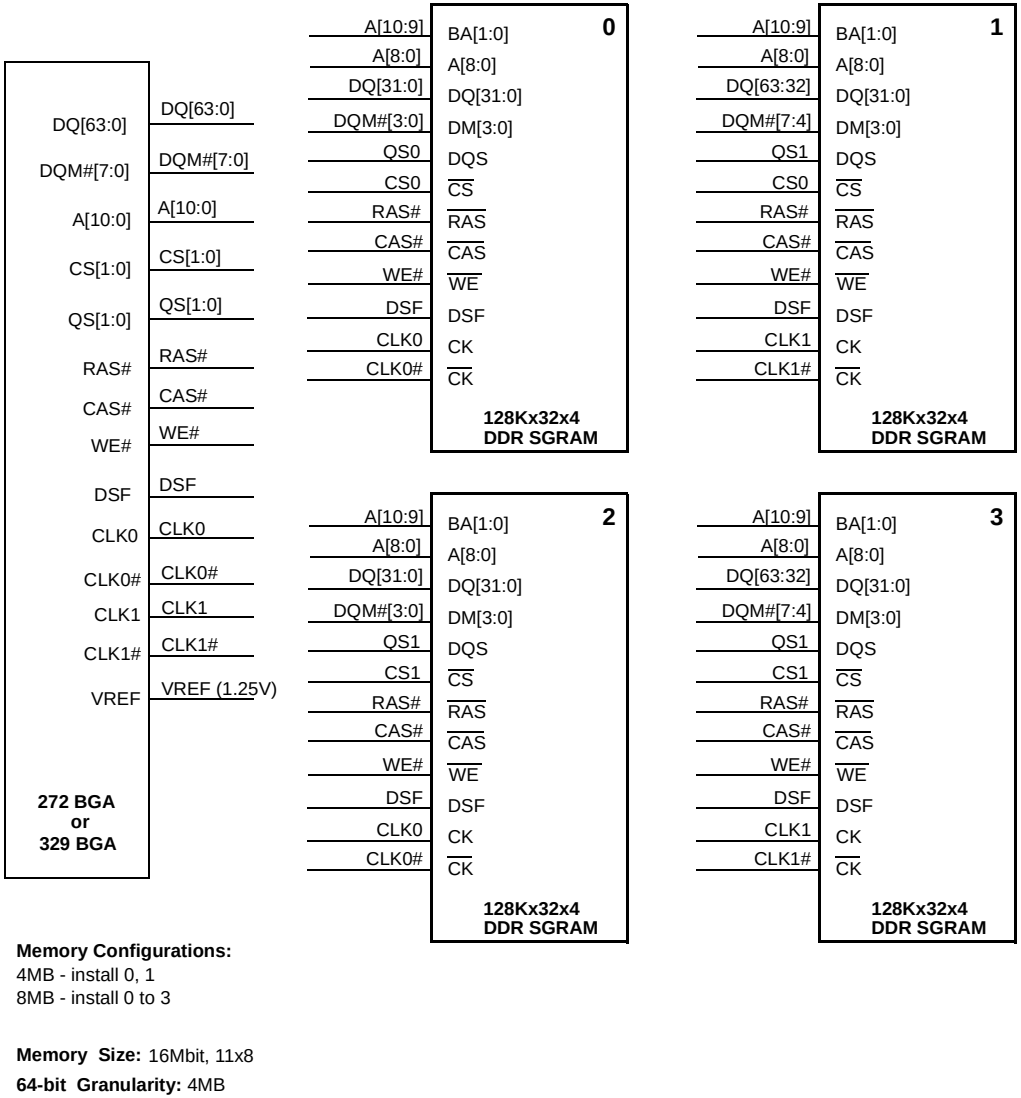


Figure 4-9. 16Mbit (11X8) DDR SGRAM Implementation for 272/329 BGA Packages

4.11.5 32Mbit (Double Data Rate (DDR) SGRAM Interface

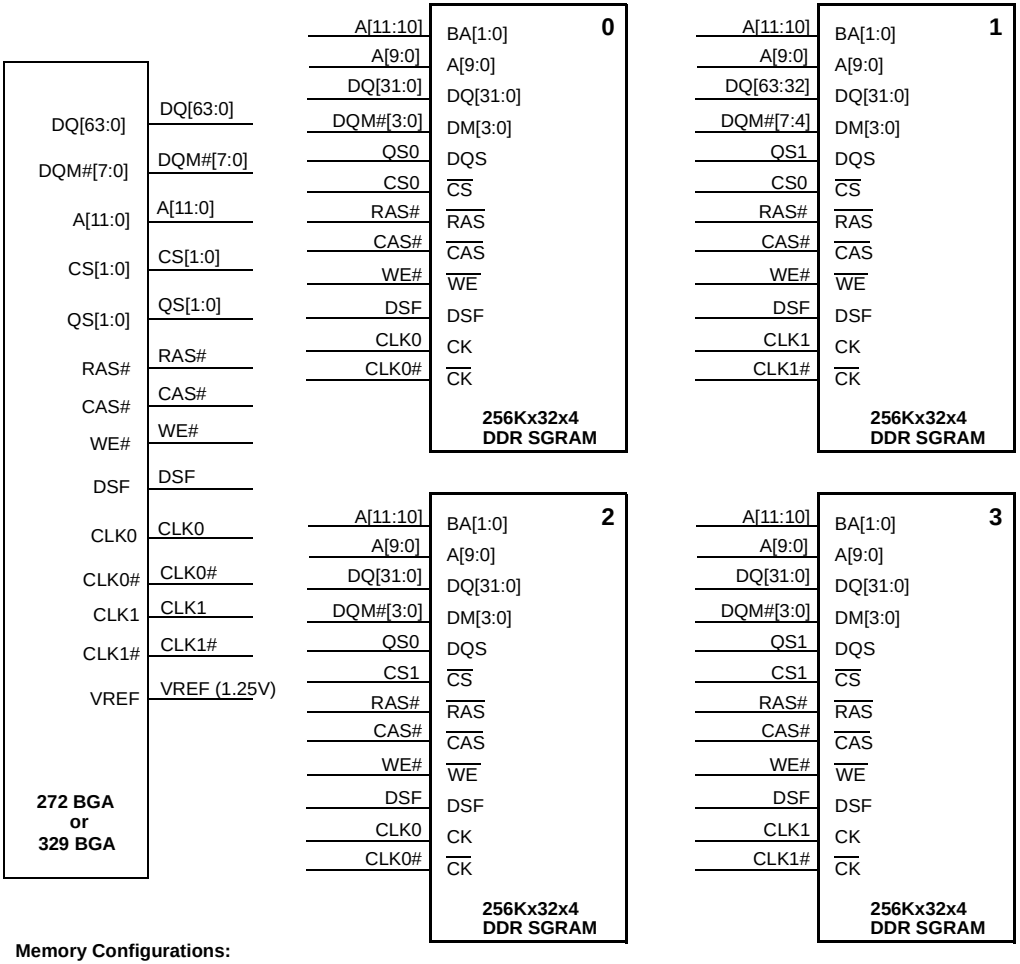


Figure 4-10. 32Mbit (12X8) DDR SGRAM Implementation for 272/329 BGA Packages

4.11.6 16Mbit (12x8) Single Data Rate (SDR) SDRAM Interface

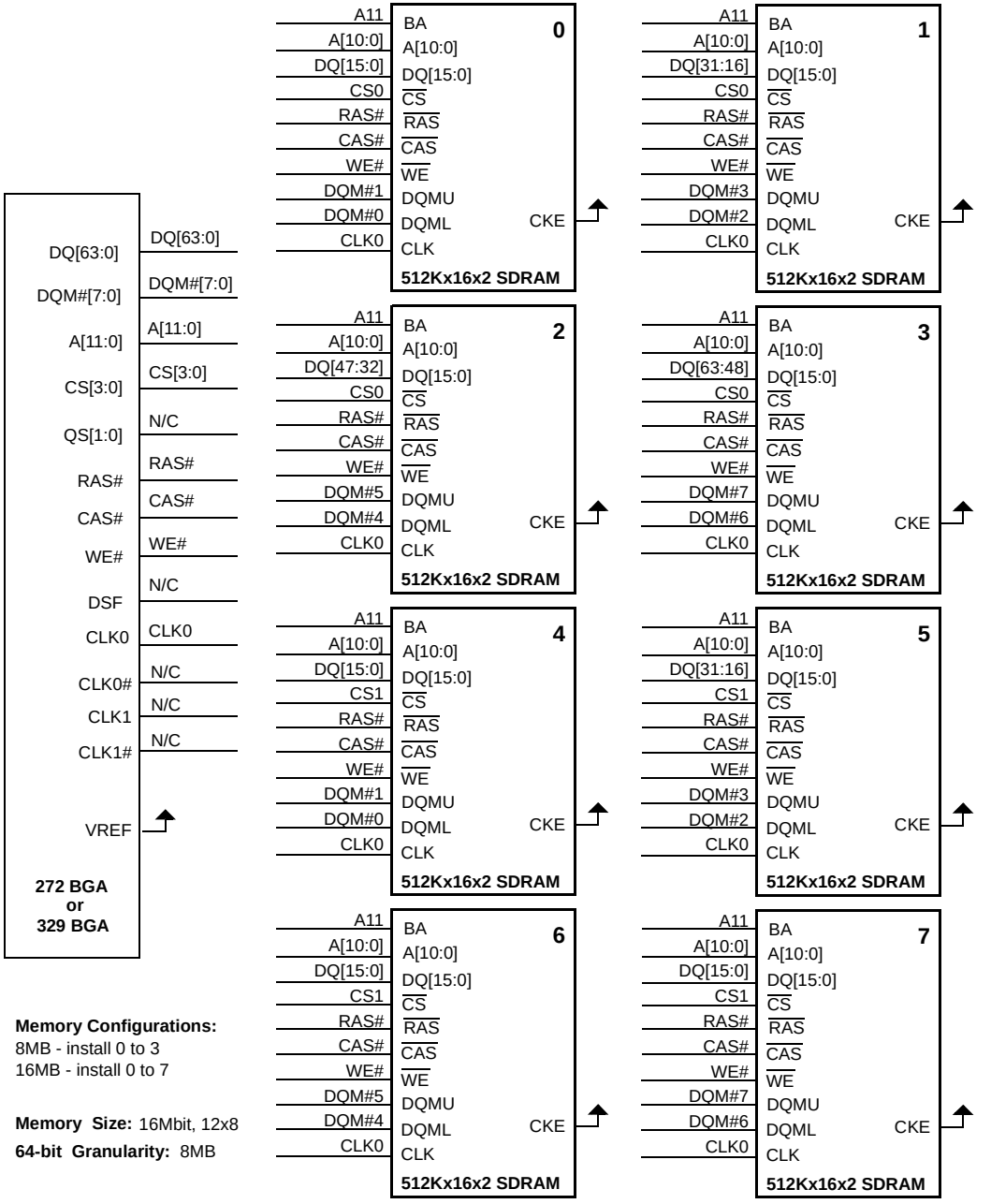


Figure 4-11. 16Mbit (12X8) SDR SDRAM Implementation for 272/329 BGA Packages

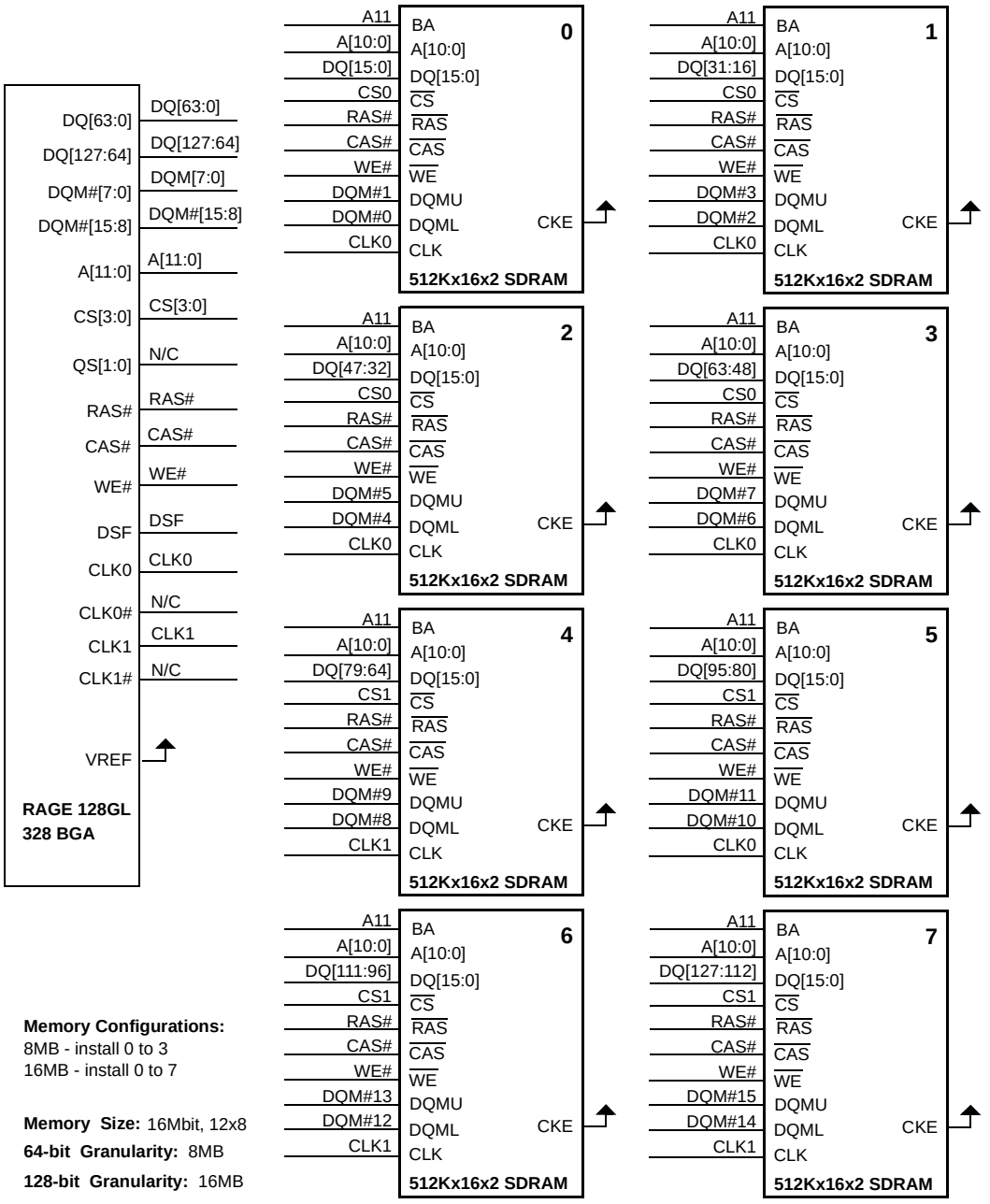
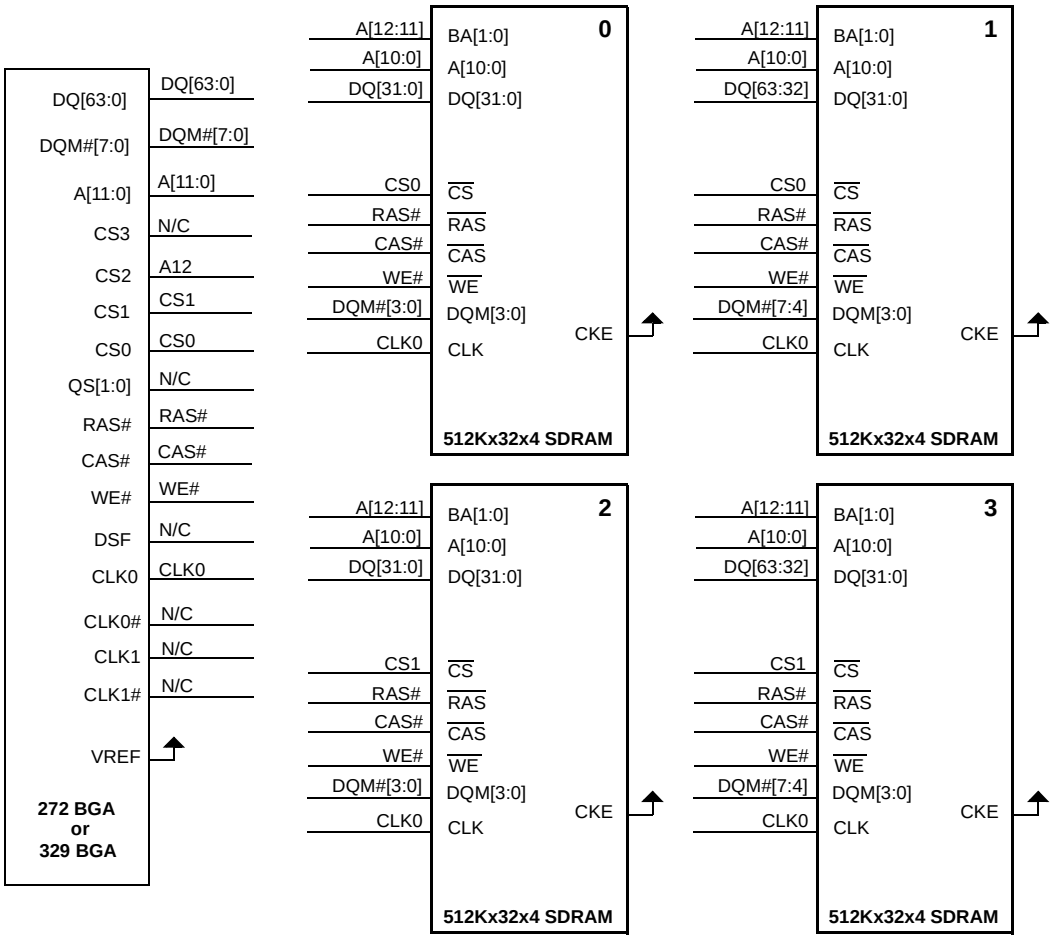


Figure 4-12. 16Mbit (12X8) SDR SDRAM Implementation for 328 BGA Package

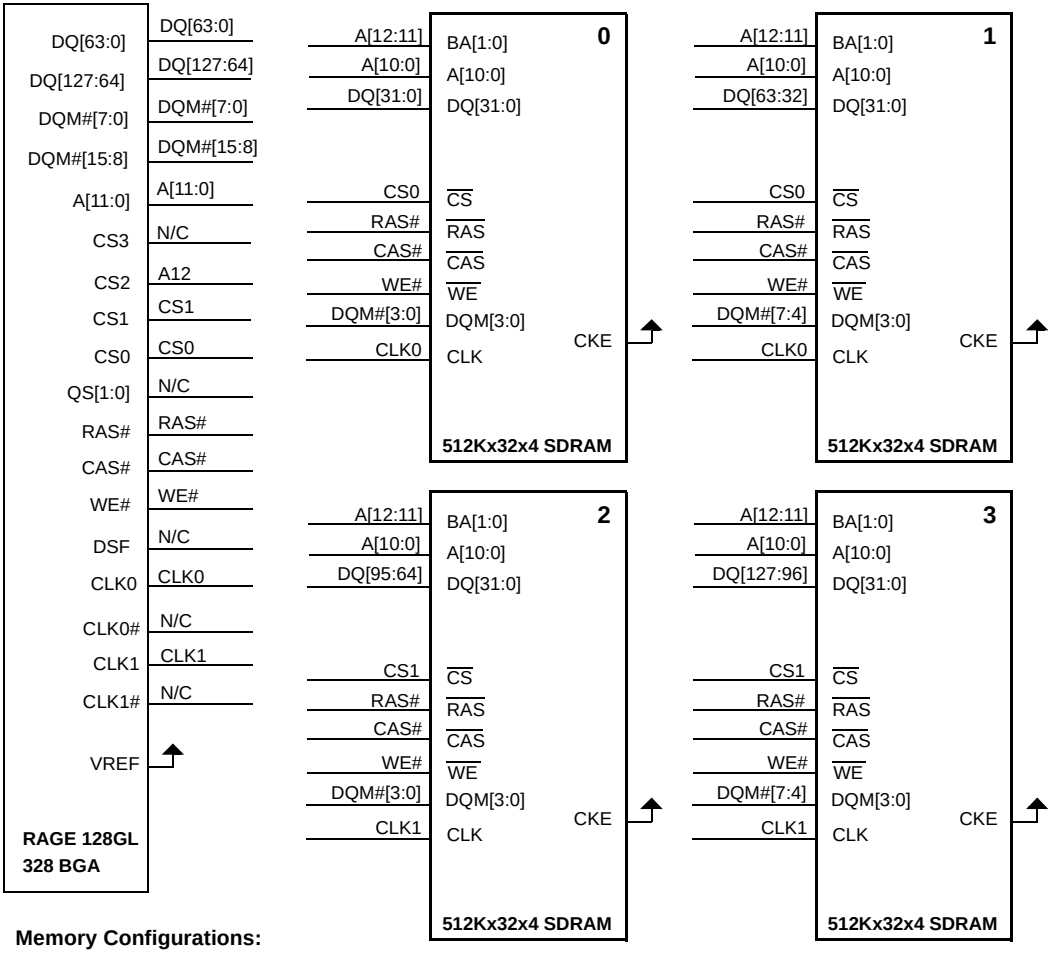
4.11.7 64Mbit (13x8) Single Data Rate (SDR) SDRAM Interface



Memory Configurations:
16MB - install 0, 1
32MB - install 0 to 3

Memory Size: 64Mbit, 13x8
64-bit Granularity: 16MB

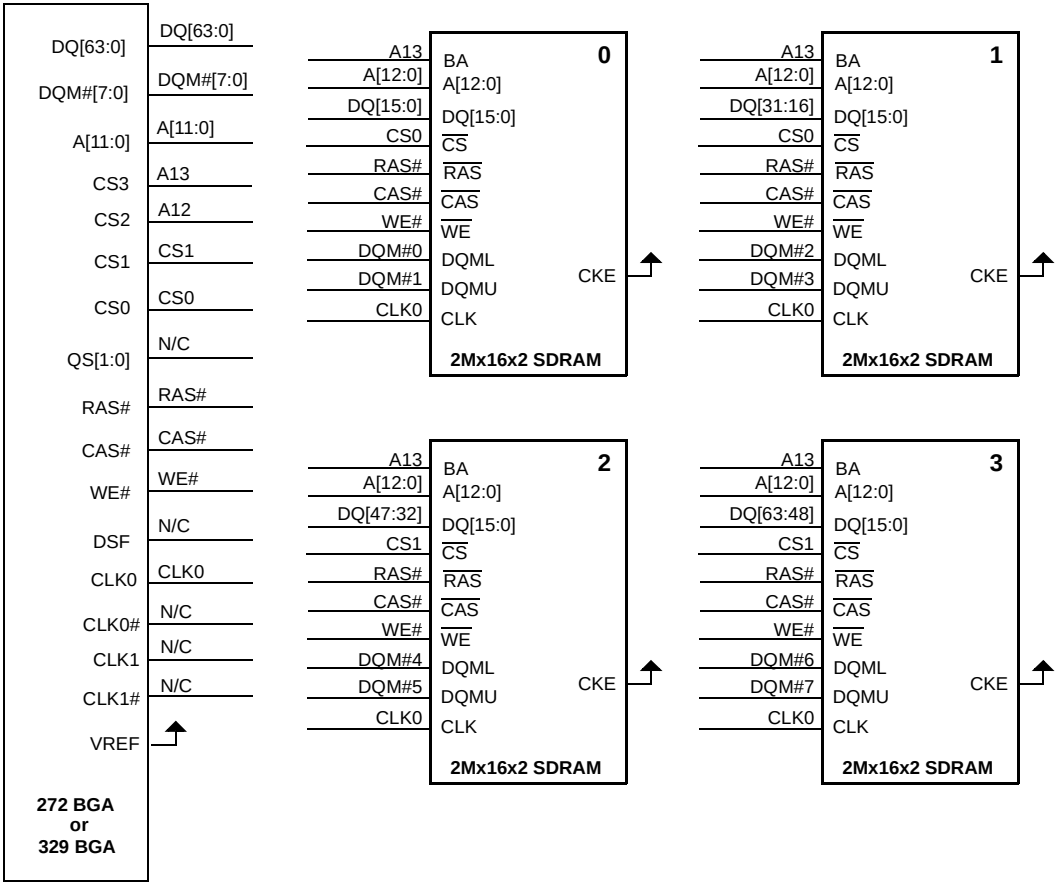
Figure 4-13. 64Mbit (13X8) SDR SDRAM Implementation for 272/329 BGA Packages



Memory Configurations:
16MB - install 0, 1
32MB - install 0 to 3

Memory Size: 64Mbit, 13x8
64-bit Granularity: 16MB
128-bit Granularity: 32MB

Figure 4-14. 64Mbit (13X8) SDR SDRAM Implementation for 328 BGA Package



Memory Configurations:
32MB - install 0 to 3

Memory Size: 64Mbit, 14x8
64-bit Granularity: 32MB

Figure 4-15. 64Mbit (14X8) SDR SDRAM Implementation for 272/329 BGA Packages

4.11.8 Memory Address Mapping:

A[24:0] = input byte address

Table 4-4 Memory Address Mapping

ADDR_MAPPING (Row bits x Col bits x Banks)	BUSWIDTH	GROUP / CS [1:0]	ROW / PAGE [11:0]	BANK[1:0]	COLUMN[7:0]
0) 9 x 8 x 2	64	A[22:21]	“000” & A[20:12]	‘0’ & A[11]	A[10:3]
	128	A[23:22]	“000” & A[21:13]	‘0’ & A[12]	A[11:4]
1) 10 x 8 x 2	64	A[23:22]	“00” & A[21:12]	‘0’ & A[11]	A[10:3]
	128	A[24:23]	“00” & A[22:13]	‘0’ & A[12]	A[11:4]
2) 11 x 8 x 2	64	A[24:23]	‘0’ & A[22:12]	‘0’ & A[11]	A[10:3]
	128	‘0’ & A[24]	‘0’ & A[23:13]	‘0’ & A[12]	A[11:4]
3) 12 x 8 x 2	64	‘0’ & A[24]	A[23:12]	‘0’ & A[11]	A[10:3]
	128	“00”	A[24:13]	‘0’ & A[12]	A[11:4]
4) 13 x 8 x 2	64	“00”	A[24:12]	‘0’ & A[11]	A[10:3]
	128	n/a	n/a	n/a	n/a
8) 9 x 8 x 4	64	A[23:22]	“000” & A[21:13]	A[12:11]	A[10:3]
	128	A[24:23]	“000” & A[22:14]	A[13:12]	A[11:4]
9) 10 x 7 x 4	64	A[23:22]	“00” & A[21:12]	A[11:10]	‘0’ & A[9:3]
	128	A[24:23]	“00” & A[22:13]	A[12:11]	‘0’ & A[10:4]
10) 10 x 8 x 4	64	A[24:23]	“00” & A[22:13]	A[12:11]	A[10:3]
	128	‘0’ & A[24]	“00” & A[23:14]	A[13:12]	A[11:4]
11) 11 x 7 x 4	64	A[24:23]	‘0’ & A[22:12]	A[11:10]	‘0’ & A[9:3]
	128	‘0’ & A[24]	‘0’ & A[23:13]	A[12:11]	‘0’ & A[10:4]
12) 11 x 8 x 4	64	‘0’ & A[24]	‘0’ & A[23:13]	A[12:11]	A[10:3]
	128	“00”	‘0’ & A[24:14]	A[13:12]	A[11:4]
13) 12 x 8 x 4	64	“00”	‘0’ & A[24:13]	A[12:11]	A[10:3]
	128	n/a	n/a	n/a	n/a

4.11.9 Clock Speeds

Table 4-5 Clock Speeds (MHz)

Configuration	Bus Width Bits	HCLK Freq Bounds		XCLK Freq Bounds	
		Lower	Upper	Lower	Upper
SDR: LVTTL	64	83	125	83	125
SDR: LVTTL	128	83	125	83	125
SDR: SSTL_3	64	125	143	62.5	71.5
DDR: SSTL_2	64	100	125	100	125

4.12 BIOS ROM (Flash ROM) Interface

Due to timing and electrical restrictions on the memory pads and the restrictions on the VIP and Zoom Video ports, a very limited number of pins is available for the implementation of straps. In order to provide the initialization information to the chip, the majority of the straps are implemented as pull-ups and pull-downs on the MPP data pins. The remaining straps are stored inside the BIOS ROM and read during reset.

4.12.1 Standard Boot-up Sequence

- PCI reset is asserted.
- External straps are fed into the chip.
- PCI reset is deasserted.
- External straps are flopped in.
- ROM state machine begins to read “ROM based straps”. Note that this operation occurs only in the add-in card implementation.
- PCI may begin its first transfer, taken but not serviced yet.
- Finished reading the straps and begin processing PCI request.
- Setup of PCI configuration space during system BIOS bus emulation.
- Copy ROM into system memory.

There are three configurations for strap/BIOS implementation:

Configuration 1. The controller is located on an add-in card, and there is access to a local video BIOS EPROM / Flash RAM.

The suggested sequence of events at power up is as follows:

- System reset goes active and the strap latches are opened to read pin level straps.
- Reset is removed and shortly after the strap latches are closed.
- A local routine between the controller and the eprom is initiated to read the additional straps stored in the eprom.
- The first PCI configuration cycle is initiated and the eprom is read and stored in the system memory.
- Standard operations can begin.

The ROM state machine of the 128 VR/GL will read in all the “ROM based straps” right after PCI reset is deasserted. There are a total of 5 bytes worth of “ROM based straps” which are stored at byte location 0x70 through 0x74 in the eprom/flashrom. The first four bytes contain **subsys_venid[15:0] and subsys_id[15:0]**, and the fifth byte is reserved.

Configuration 2. The controller is located on the system motherboard and the video BIOS is stored in the system BIOS EPROM/Flash RAM.

The suggested sequence of events at power up is as follows:

- System reset goes active and the strap latches are opened to read pin level straps.
- Reset is removed and shortly after the strap latches are closed
- The first PCI config cycle is initiated and the additional straps stored in the system BIOS are written into the controller. This occurs before POST begins in system BIOS, as per PC98.
- Standard operations can begin.

The System BIOS will be responsible for loading the subsystem-id and subsystem-vendor-id through an aliased address in the reserved configuration space. The reason for writing through an aliased address (16#4c) is that config location 16#2c is read-only. Any writes to this location (16#4c) will also change the content of the subsystem vendor ID at 16#2c.

Configuration 3. Combination of configurations **1** and **2** (add-in card and device on motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the “ROM based straps” independently from the video BIOS.

Note: If neither the system BIOS nor the add-in card video BIOS supply the subsystem-id and subsystem-vendor-id, their values are defaulted to chip-id and vendor-id (0x1002 h) respectively inside the chip.

4.12.2 Add-in Card Implementation

Due to pin constraints, for a 128KB EPROM / Flash ROM, two “octo-flops” and two “flops” are required as shown below.

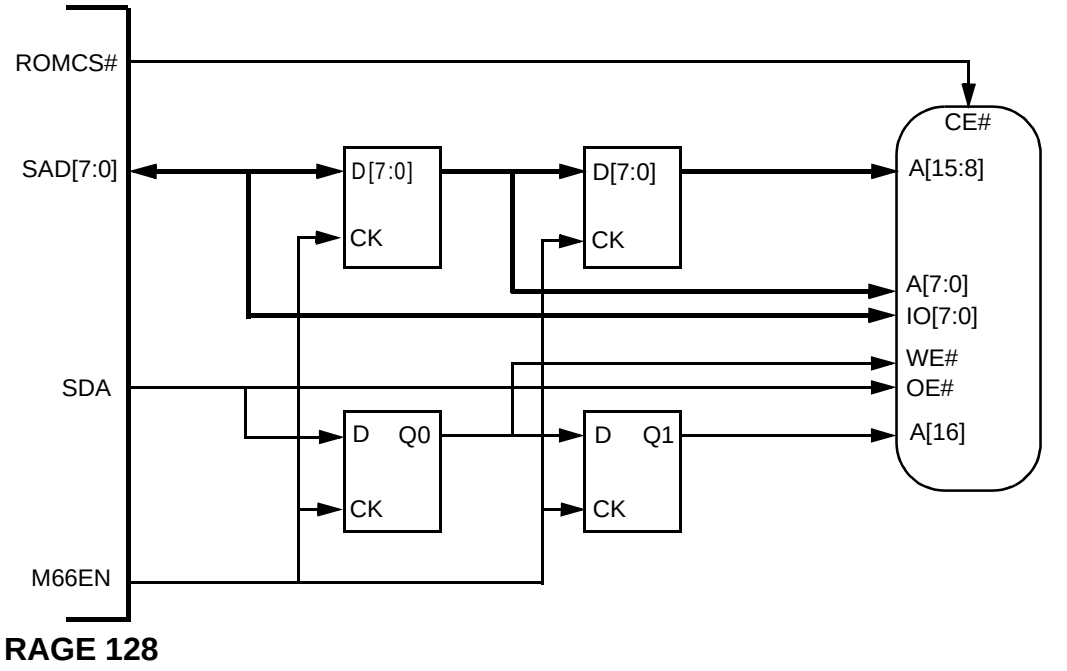


Figure 4-16. 128K Configuration

However, for a 32K/64K EPROM / Flash ROM, only two “octo-flops” and an inverter can be used as shown below.

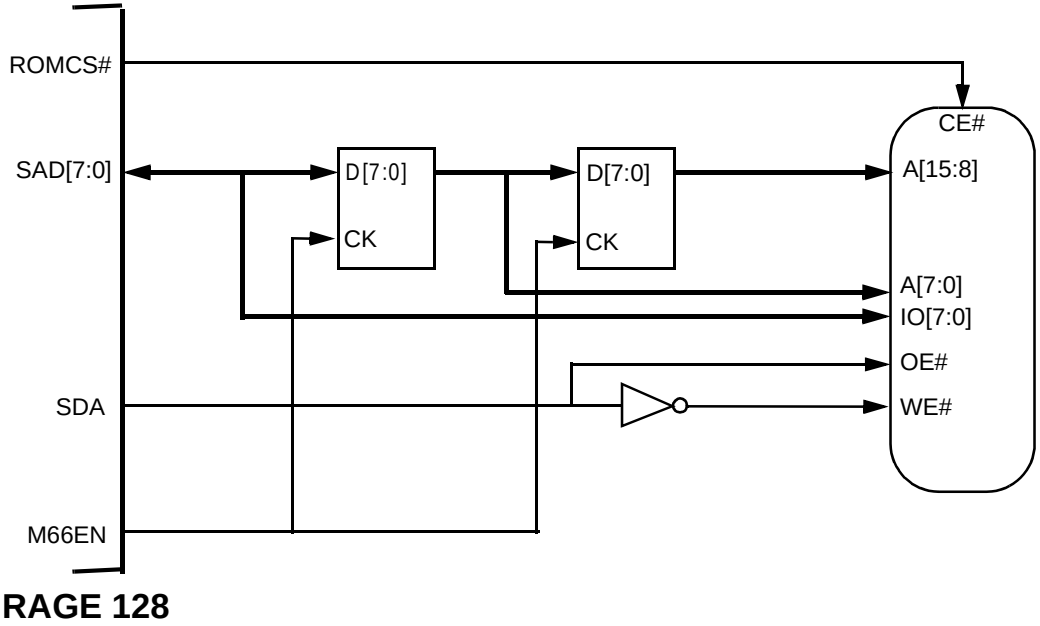


Figure 4-17. 32K/64K Configuration

A minimum of 11 pins is required.

Table 4-6 Pin Connections for the above configurations

Pin Name	PROM / EPROM		Flash ROM	
	64KB	128KB	64KB	128KB
Muxed on SAD[7:0]	A[7:0]	A[7:0]	A[7:0]	A[7:0]
	A[15:8]	A[15:8]	A[15:8]	A[15:8]
SDA	N/A	A[16]	N/A	A[16]
Muxed on SAD[7:0]	D[7:0]	D[7:0]	D[7:0]	D[7:0]
SDA	OE#	OE#	OE#	OE#
ROMCS#	CE#	CE#	CE#	CE#
SDA	N/A	N/A	WE#	WE#
M66EN	CLK	CLK	CLK	CLK

4.13 Straps

4.13.1 External Straps

The table below lists the minimum external straps that must be installed on the (system or add-in) board to enable the PCI clock and start the first PCI frame.

Table 4-7 External Straps

Strap	Pin	Description	Default
vga_disable	SAD7	0 - VGA controller capability enabled 1 - The device will not be recognized as the system's VGA controller, but only as an extended mode controller	0 (enable) (internal pull-down)
idsel#	SAD6	In AGP mode, determines whether pin AD16 or AD17 is used as IDSEL 0 - AD16 1 - AD17	0 (AD16) (internal pull-down)
lcd	LCDCDE	Future LCD interface 0 - Panel interface disabled 1 - Panel interface enabled	0 (disable) (internal pull-down)
id_disable	LCDCLK	0 - Normal operation 1 - Shuts the chip down by not responding to any config cycles. In a system with two graphics chips, one on motherboard, the other on add-in card, this strap can be used to disable one of the two through a jumper.	0 (the chip will respond) (internal pull-down)
enint#	VSYNC	0 - Enables interrupt 1 - Disables interrupt	0 (enable) (internal pull-down)
bus_clk_sel*	HSYNC	Chooses between refclk or pllclk	0 (see table) (internal pull-down)
bustype[1:0]*	SAD[5:4]	Together with Bus_clk_sel they define the bus type (PCI or AGP)	(0,0) see table (internal pull-down)
agpskew[1:0]	SAD[1:0]	AGP 1x clock feedback phase adjustment wrt refclk (cpuclk) 00 - refclk slightly earlier than feedback 01 - refclk 1 tap earlier than feedback 10 - refclk 1 tap later than feedback 11 - refclk 2 taps earlier than feedback clock	00 (aligned) (internal pull-down)
x1clk_skew[1:0]	SAD[3:2]	Clock phase adjustment between x1clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (no skew) (internal pull-down)

Table 4-7 External Straps (Continued)

Strap	Pin	Description	Default
add_in_card	ROMCS#	1 - add-in card implementation, bios cycles will occur. 0 - motherboard implementation, bios cycles will not occur.	1 (add-in card) (internal pullup)

* See table below for bus type combination modes.

Table 4-8 Bus Type Combinations

Mode	Bus_clk_sel	Bus Type(1)	Bus Type(0)	Description
1	1	0	0	Ref. clk, PCI 5v signaling environment.
2	1	0	1	Ref. clk, PCI 3.3v signaling environment
3	0	1	0	PLL clk, PCI 66 Mhz
4	0	0	0	PLL clk, AGP 1x, 2x (Default Mode)
5	0	0	1	PLL clk, AGP 4x (future implementation, will default to mode 4 for now)
6	1	1	1	Ref. clk, AGP test mode

Note: Combinations ‘1,1,0’ and ‘0,1,1’ (and ‘0,0,1’) which are not currently used will default to mode 4 (PLL clk, AGP 1x, 2x).

4.13.2 Board Level Buffer Implementation

In order to better guarantee the proper latching of the straps on the SAD lines even if there is an AMC/MPP device connected which does not properly tristate its SAD data lines during system reset, the use of on board tristate-able buffers (LS244) is recommended (see figure below).

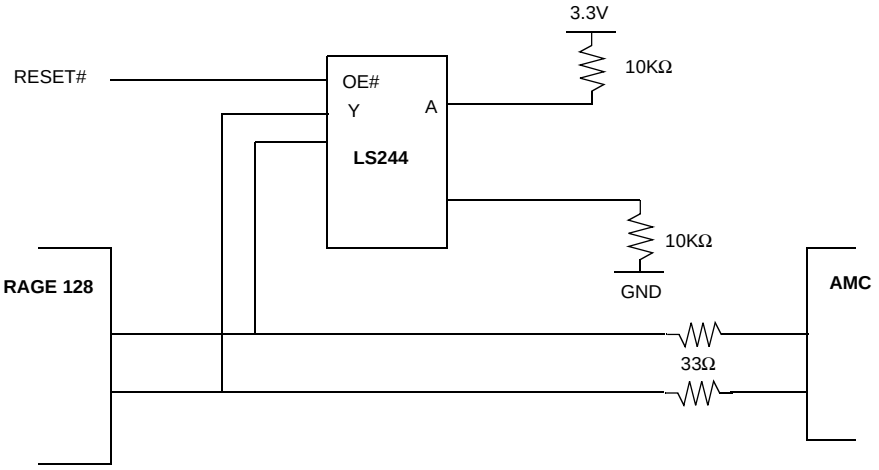


Figure 4-18 Implementation of Board Level Buffers

Notes:

This scheme can also be implemented for the straps that are on the HSYNC and VSYNC lines in case there is concern about the leakage current on the LS125 input pins which are connected to HSYNC and VSYNC.

For straps that must be set on the board, the use of 4.7 kΩ (min) to 10 kΩ (max) resistors is recommended for pull-ups to power (3.3 V) or pull downs to ground. 4.7 kΩ provides more noise immunity, whereas 10 kΩ will result in lower static power dissipation.

4.13.3 ROM Based Straps

The table below describes the straps that must be stored in the system (or video) BIOS.

Table 4-9 ROM Based Straps

Strap	ROM Location	Description	Default
subsys_ven_ id[15:0]	0x71- 0x70	Special class of config id required for WIN9x. On add-in card, video ROM writes in the id after pcireset On motherboard, system ROM writes in the id **before** the enumeration cycle is initiated	1002h
subsys_id[15:0]	0x73- 0x72	Same as subsys_ven_id	chip_id

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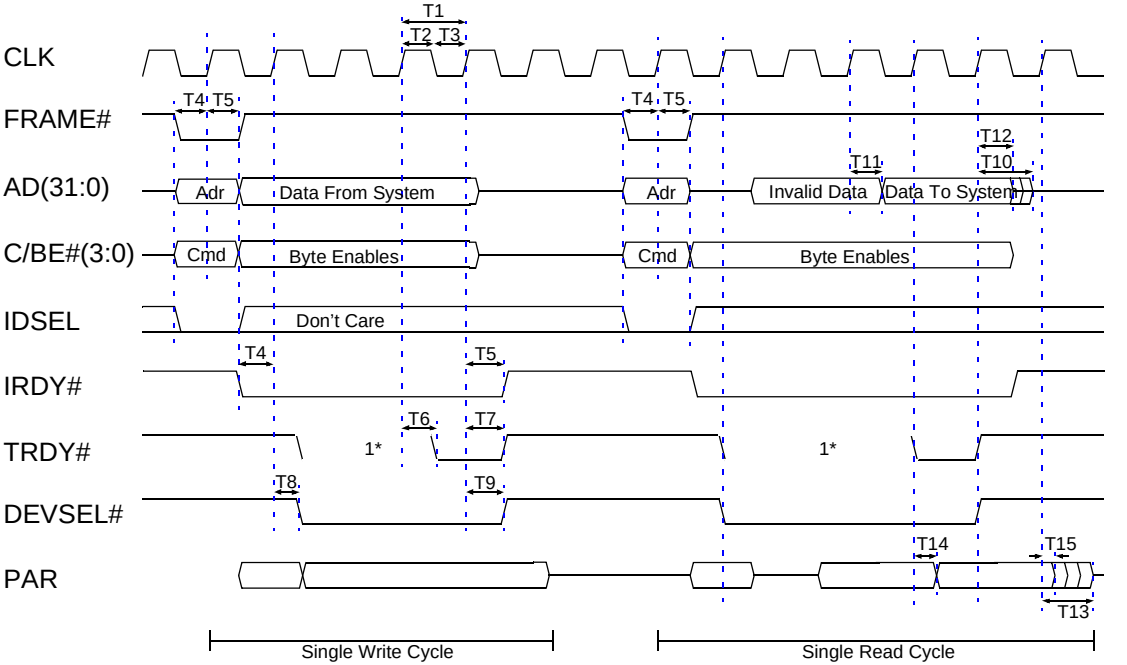
Chapter 5
Bus Timing Specifications

5.1 Bus Timing

Timing specifications for PCI and AGP bus operations are given by:

- Single Read/Write Cycle Timing, see *Figure 5-1*.
- Disconnect On Burst Cycle, see *Figure 5-2*.
- Burst Access Timing, see *Figure 5-3*.
- PCI Bus Master Operation, see *Figure 5-4*.
- AGP AC Timing, see *Figure 5-5*. and *Figure 5-6*.

5.1.1 Single Read/Write Cycle Timing - PCI Bus



1* The minimum number of clocks from FRAME# active to TRDY# active is programmable.

Figure 5-1. Single Read/Write Cycle Timing - PCI Bus

5.1.2 Disconnect On Burst Cycle - PCI Bus

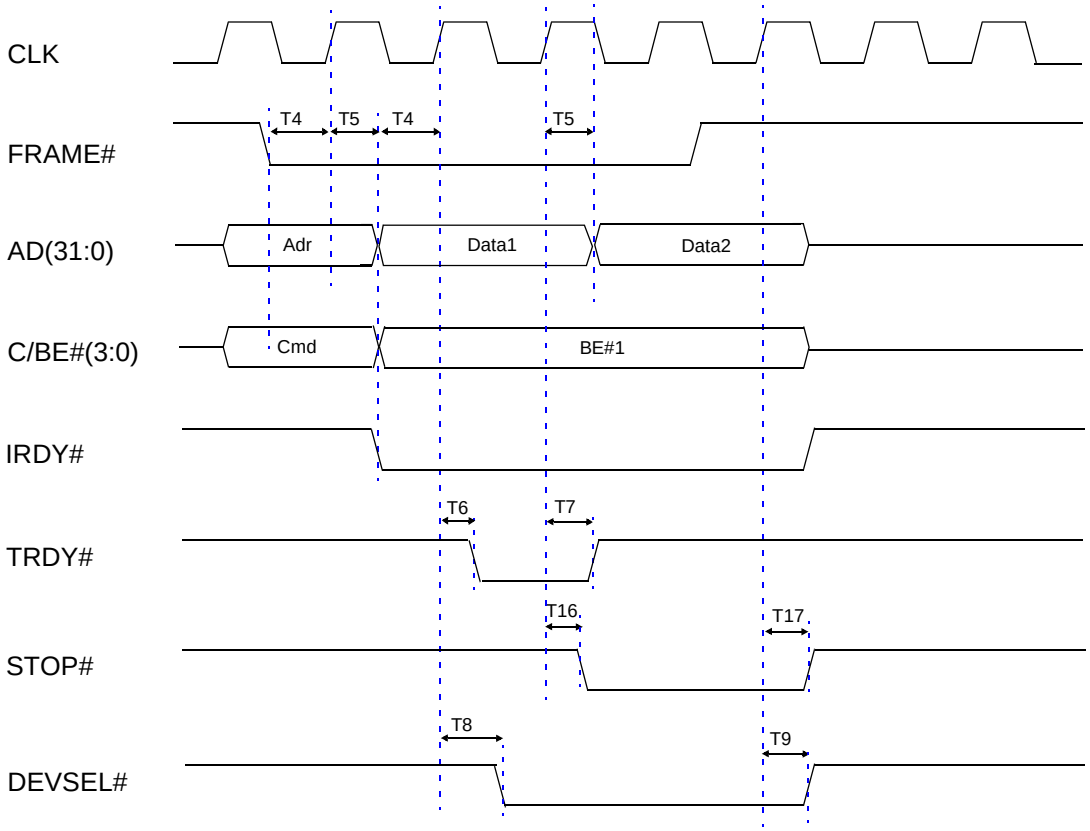


Figure 5-2. Disconnect On Burst Cycle - PCI Bus

5.1.3 Burst Access Timing - PCI Bus

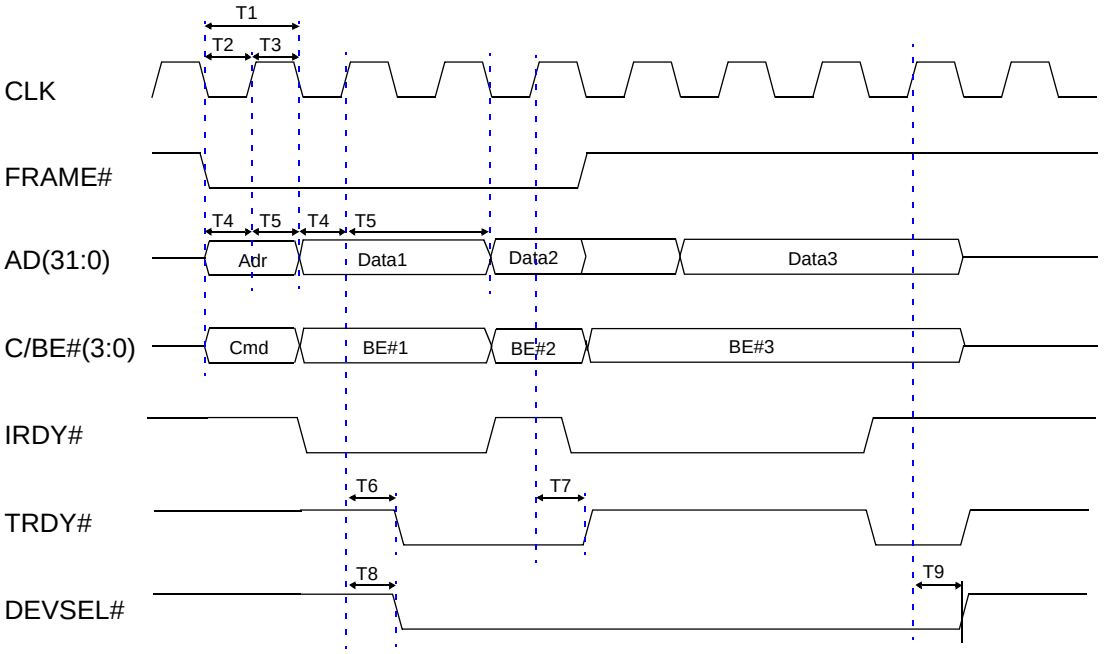


Figure 5-3. Burst Access Timing - PCI Bus

5.1.4 PCI Bus Master Operation

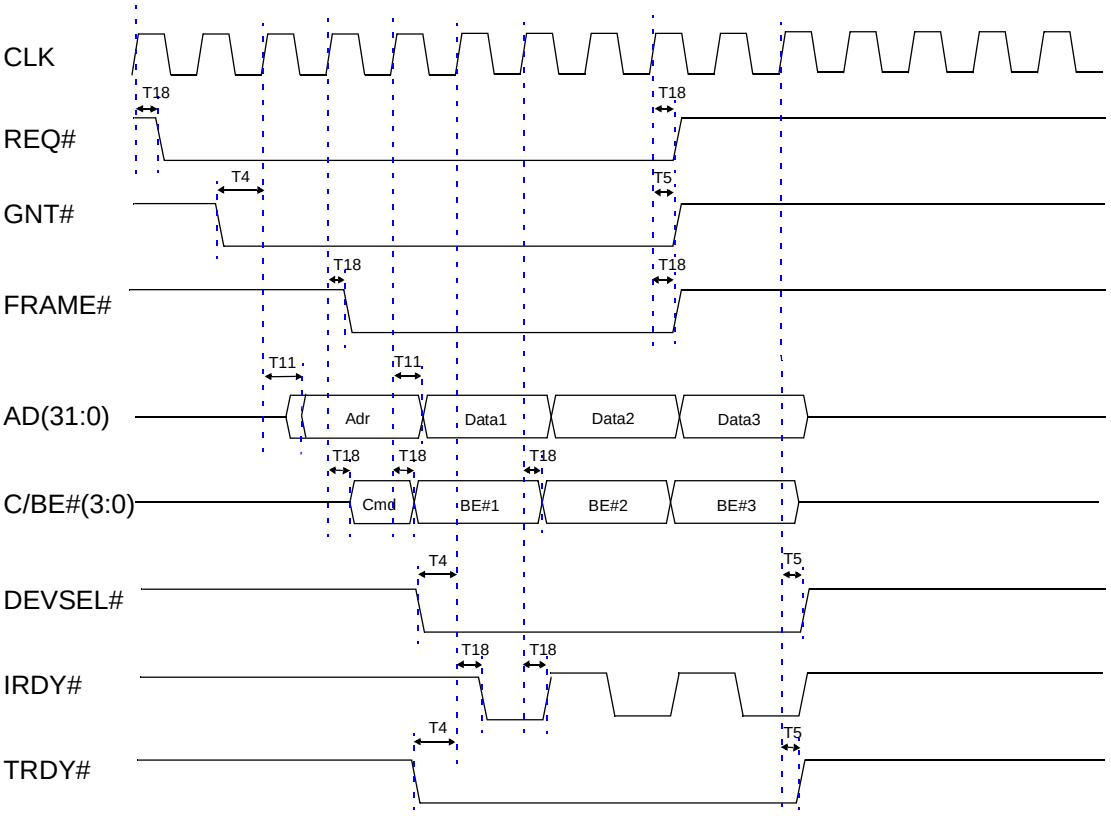


Figure 5-4. PCI Bus Master Operation

Table 5-1 PCI Bus Interface Timing Values

Symbol	Description	Min.(ns)	Max.(ns)
T1	Bus Clock Period	30	-
T2	Bus Clock High Time	12	-
T3	Bus Clock Low Time	12	-
T4	Bus Input Signal Setup to CLK[a]	7	-
T5	Bus Input Signal Hold from CLK[a]	0	-
T6	CLK to TRDY# active	2	11
T7	CLK to TRDY# inactive	2	11
T8	CLK to DEVSEL# active	2	11
T9	CLK to DEVSEL# inactive	2	11
T10	CLK to data output tri-state	2	20
T11	CLK to data output valid delay (data stepping buffer)	2	20
T12	CLK to data output invalid delay	2	-
T13	CLK to PAR tri-state	2	20
T14	CLK to PAR valid delay (data stepping buffer)	2	20
T15	CLK to PAR invalid delay	2	-
T16	CLK to STOP# active delay	2	11
T17	CLK to STOP# inactive delay	2	11
T18	CLK to signal valid delay	2	11

a. Bus input signals include FRAME#, AD(31-0), IDSEL, IRDY#, TRDY#, GNT#, DEVSEL#.

5.1.5 AGP Timing

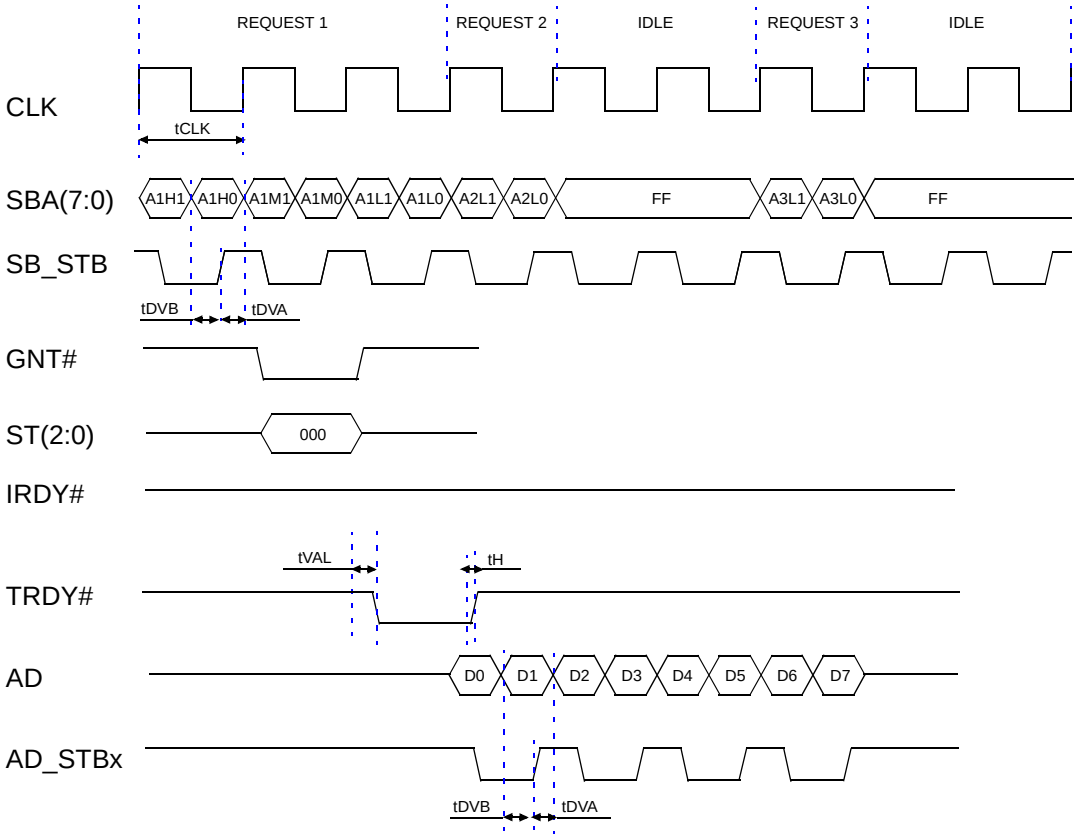


Figure 5-5. AGP 2X Read Request with Return Data (4Qw)

Table 5-2 AGP 2X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tCLK	Clock	-	15
tDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	-
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

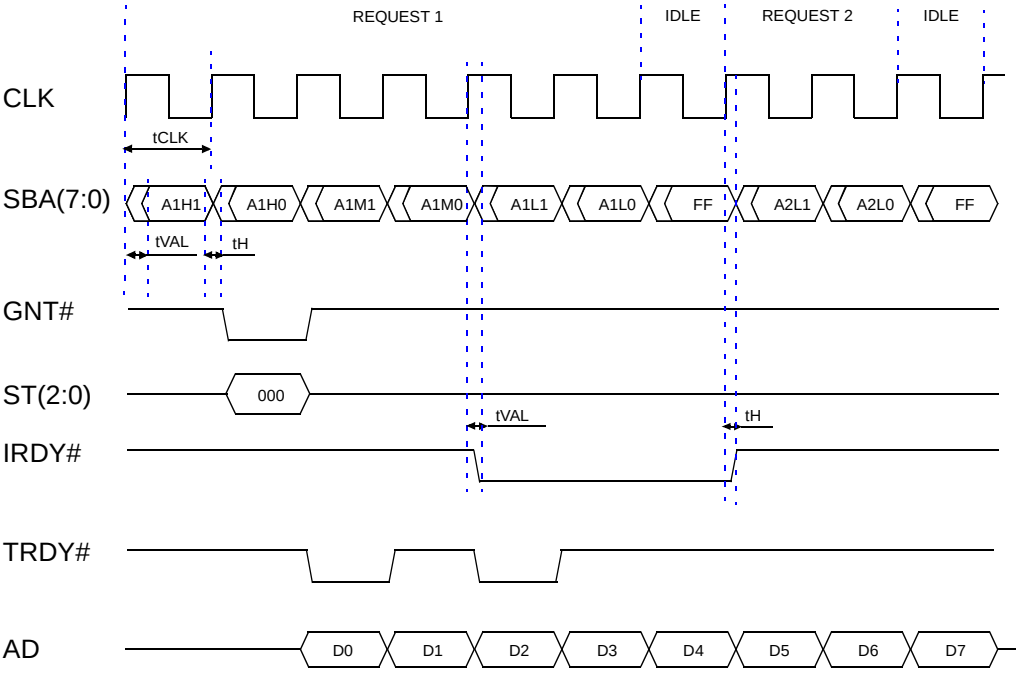


Figure 5-6. AGP 1X Read Request with Return Data (4Qw)

Table 5-3 AGP 1X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

5.2 Memory Timing

5.2.1 Timing Values

Single Data Rate SDRAM/SGRAM

Table 5-4 AC Single Data Rate SDRAM/SGRAM Cycle Timing Values

Parameter	Symbol	Min. (ns)	Max. (ns)
Clock period	tC	8	-
Clock high time	tCH	3.75	4.25
Clock low time	tCL	3.75	4.25
Command setup time provided (RAS, CAS, WE, CS, DSF)	tCMS	2.82	-
Command hold time provided (RAS, CAS, WE,CS, DSF)	tCMH	1.88	-
Address setup time provided	tAS	2.82	-
Address hold time provided	tAH	1.88	-
DQM setup time provided	tDQMS	2.93	-
DQM hole time provided	tDQMH	1.67	-
Write data setup time provided	tWDS	2.93	-
Write data hold time provided	tWDH	1.67	-
Read data setup time required	tRDS	0.16	-
Read data hole time required	tRDH	1.69	-

Double Data Rate SGRAM

Table 5-5 AC Double Data Rate SGRAM Cycle Timing Values

Parameter	Symbol	Min. (ns)	Max. (ns)
Clock period	tC	8	-
Clock high time	tCH	3.75	4.25
Clock low time	tCL	3.75	4.25
Command setup time provided (RAS, CAS, WE, CS, DSF)	tCMS	2.82	-
Command hold time provided (RAS, CAS, WE,CS, DSF)	tCMH	1.88	-
Address setup time provided	tAS	2.82	-
Address hold time provided	tAH	1.88	-

Table 5-5 AC Double Data Rate SGRAM Cycle Timing Values (Continued)

Parameter	Symbol	Min. (ns)	Max. (ns)
Clock to valid write strobe provided	tWQS	4.35	6.64
Write strobe preable provided	tWPRE	3.75	-
Write strobe postamble provided	tWPST	8	-
DM setup time provided w.r.t. QS	tDQMS	1.33	-
DM hole time provided w.r.t. QS	tDQMH	0.93	-
Write data setup time provided w.r.t. QS	tWDS	1.33	-
Write data hold time provided w.r.t. QS	tWDH	0.93	-
Clock to read data strobe required	tRQS	2.5	5.5
Read strobe preamble required	tRPRE	5	11
Read strobe postamble required	tRPST	4	10
Read data to DQS variance required	tRDQS	-	0.50

5.2.2 Programming Timing Values

The table below shows the memory timing parameters that may be programmed through the register EXT_MEM_CNTL(=0x0000D55A). They apply to both Single Data Rate SDRAM/SGRAM and Double Data Rate SDRAM/SGRAM.

Table 5-6 Programming of Timing Values

Parameter	Symbol	Min (clocks)	Max (clocks)	Register field in EXT_MEM_CNTL
Row cycle time	tRC	2	12	MEM_TRP[1:0] + MEM_TRAS[6:4]
PRE to ACTV minimum delay	tRP	1	4	MEM_TRP[1:0]
ACTV to CMD minimum delay	tRCD	1	4	MEM_TRCD[3:2]
ACTV to PRE minimum delay	tRAS	1	8	MEM_TRAS[6:4]
ACTV to ACTV minimum delay	tRRD	1	4	MEM_TRRD[9:8]
Read to write data minimum turnaround cycles	tR2W	0	3	MEM_TR2W[11:10]
Write recovery time	tWR	1	4	MEM_TWR[13:12]
Block write cycle time	tBWC	1	2	MEM_TBWC[14]
Special mode register latency	tSML	1	2	MEM_TSML[15]

Table 5-6 Programming of Timing Values (Continued)

Parameter	Symbol	Min (clocks)	Max (clocks)	Register field in EXT_MEM_CNTL
Different group read to read data minimum turnaround cycles	tR2R	0	3	MEM_TR2R[17:16]
Write to read command delay	tW2R	1	4	MEM_TW2R_MODES [28]

The table below shows the recommended values for the above parameters for DDR SGRAM.

Table 5-7 Recommended Timing Values

Parameter	Symbol	Register field in EXT_MEM_CNTL
Row cycle time	tRC	9 clocks
PRE to ACTV minimum delay	tRP	MEM_TRP[1:0] = 2 (3 clocks)
ACTV to CMD minimum delay	tRCD	MEM_TRCD[3:2] = 2 (3 clocks)
ACTV to PRE minimum delay	tRAS	MEM_TRAS[6:4] = 5 (6 clocks)
ACTV to ACTV minimum delay	tRRD	MEM_TRRD[9:8] = 1 (2 clocks)
Read to write data minimum turnaround cycles	tR2W	MEM_TR2W[11:10] = 1 (1 clock)
Write recovery time	tWR	MEM_TWR[13:12] = 2 (3 clocks)
Block write cycle time	tBWC	MEM_TBWC[14] = 1 (2 clocks)
Special mode register latency	tSML	MEM_TSML[15] = 0 (1 clocks)
Different group read to read data minimum turnaround cycles	tR2R	MEM_TR2R[17:16] = 2 (2 clocks)
Write to read command delay	tW2R	MEM_TW2R_MODE = 1 (tWR clocks)

5.2.3 Single Data Rate (SDR) SDRAM/SGRAM Timing Diagrams

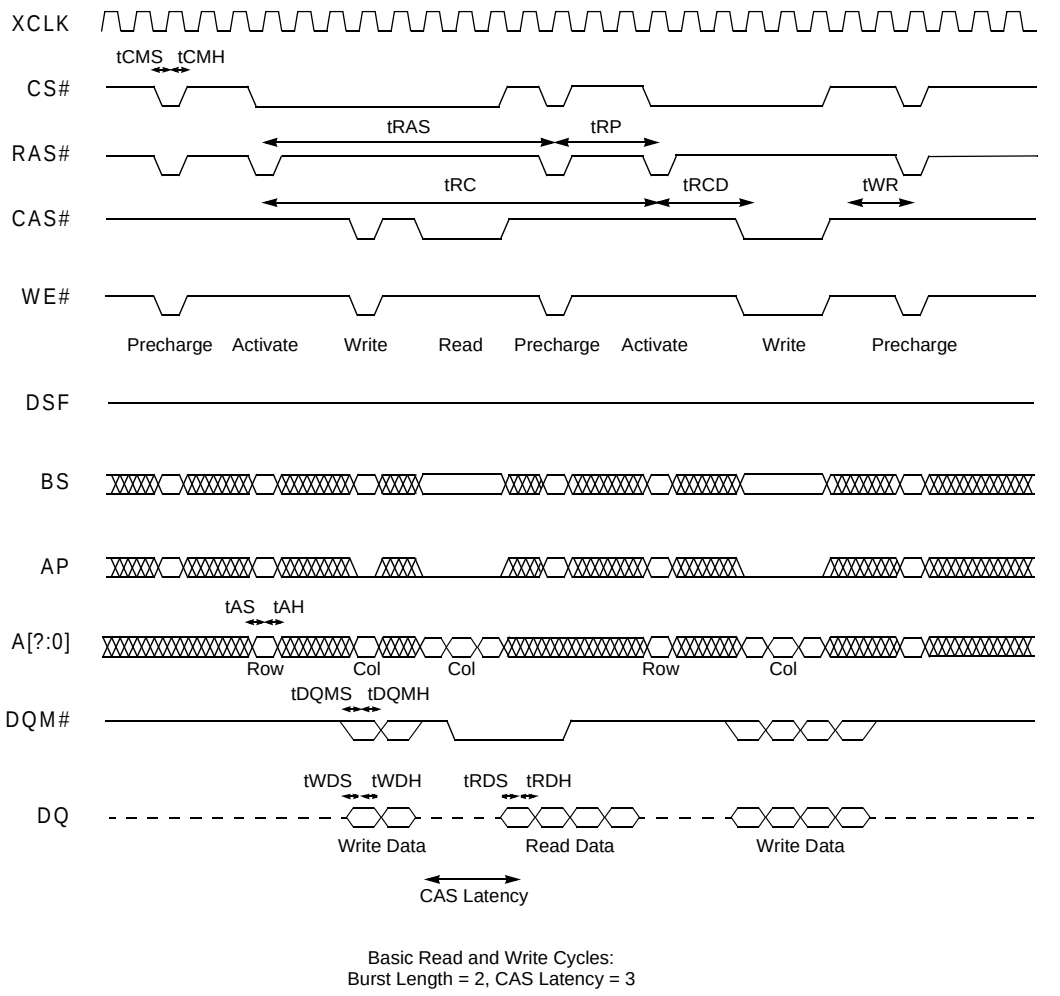


Figure 5-7. SDRAM/SGRAM Basic Read/Write Cycle Timing

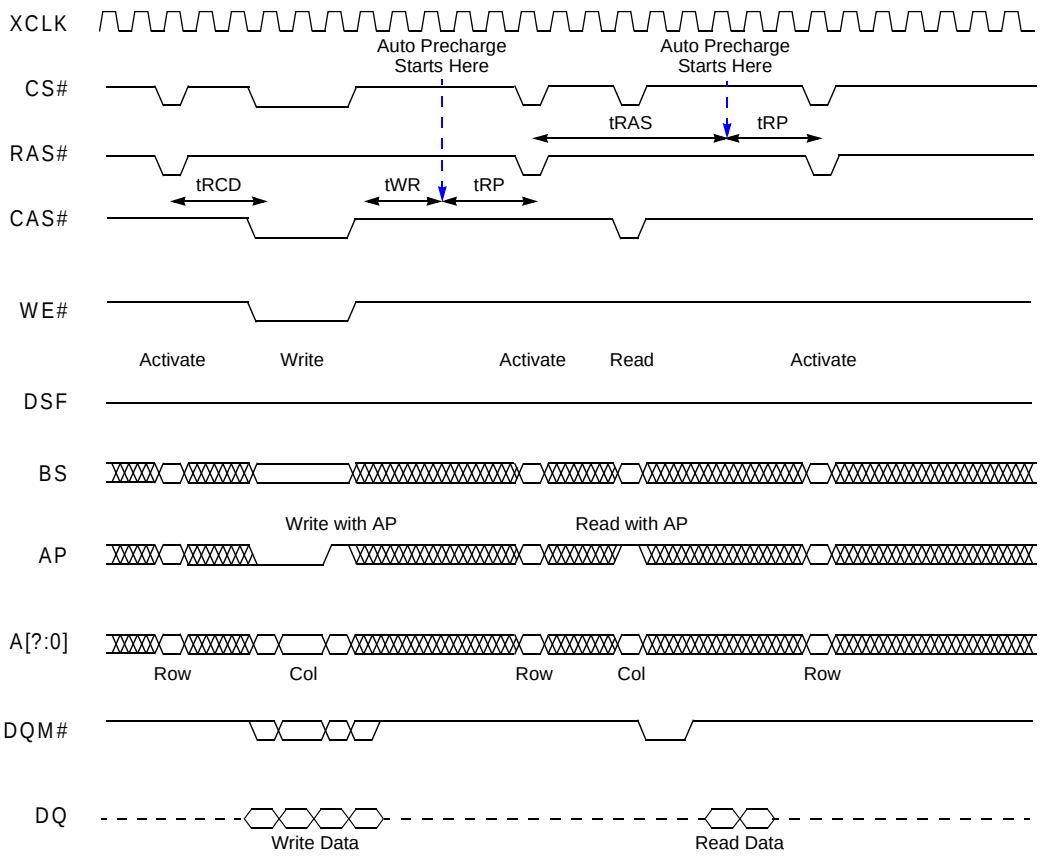


Figure 5-8. Read/Write Cycles with Auto Precharge

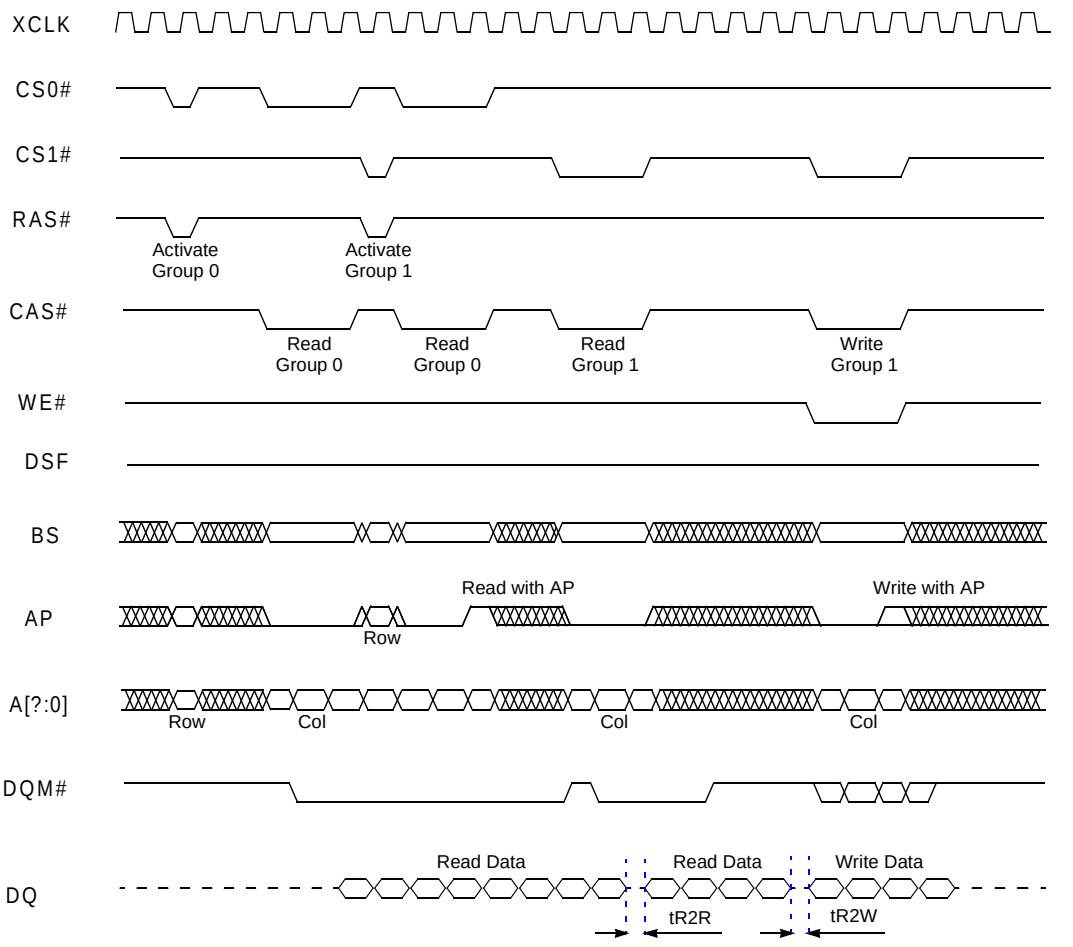


Figure 5-9. Read/Write Data Turnaround Cycles

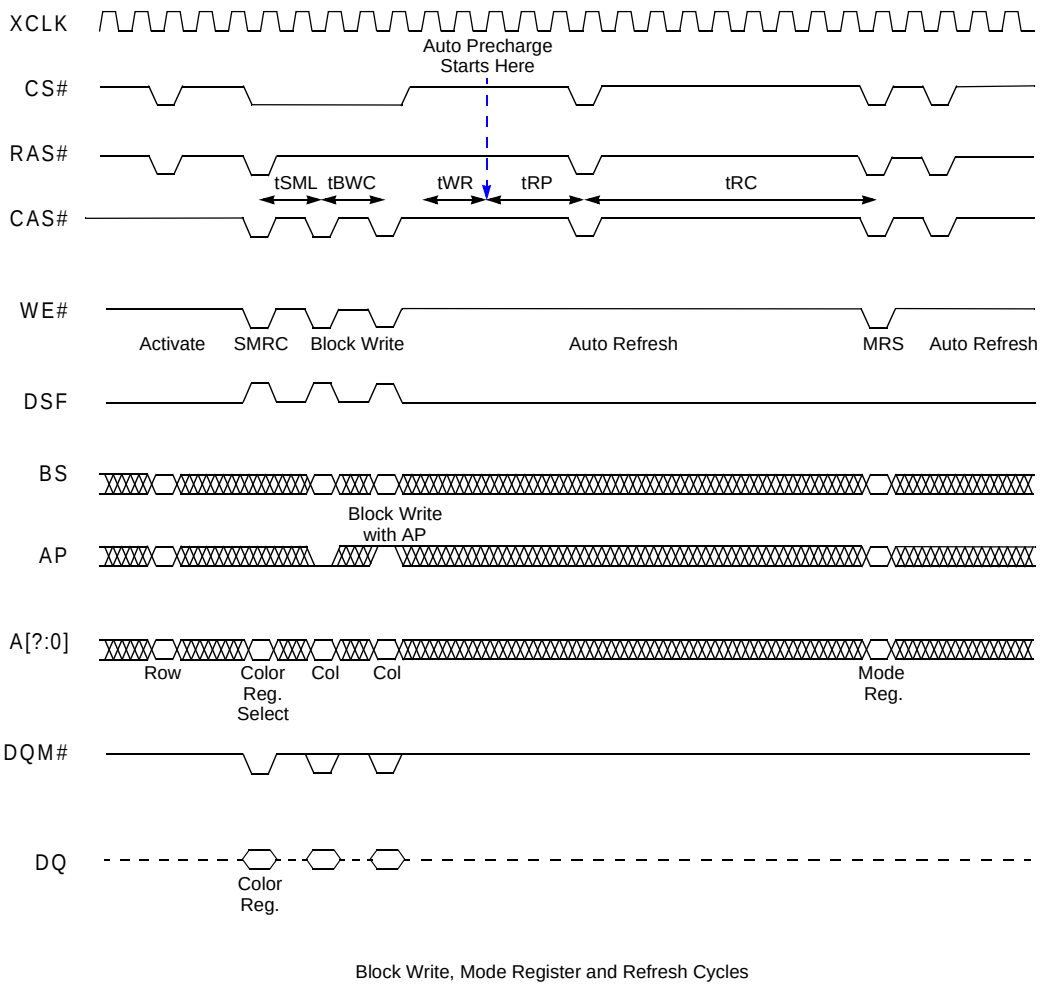


Figure 5-10. Block Write, Mode Register, and Refresh Cycles

5.2.4 Double Data Rate (DDR) SGRAM Timing Diagrams

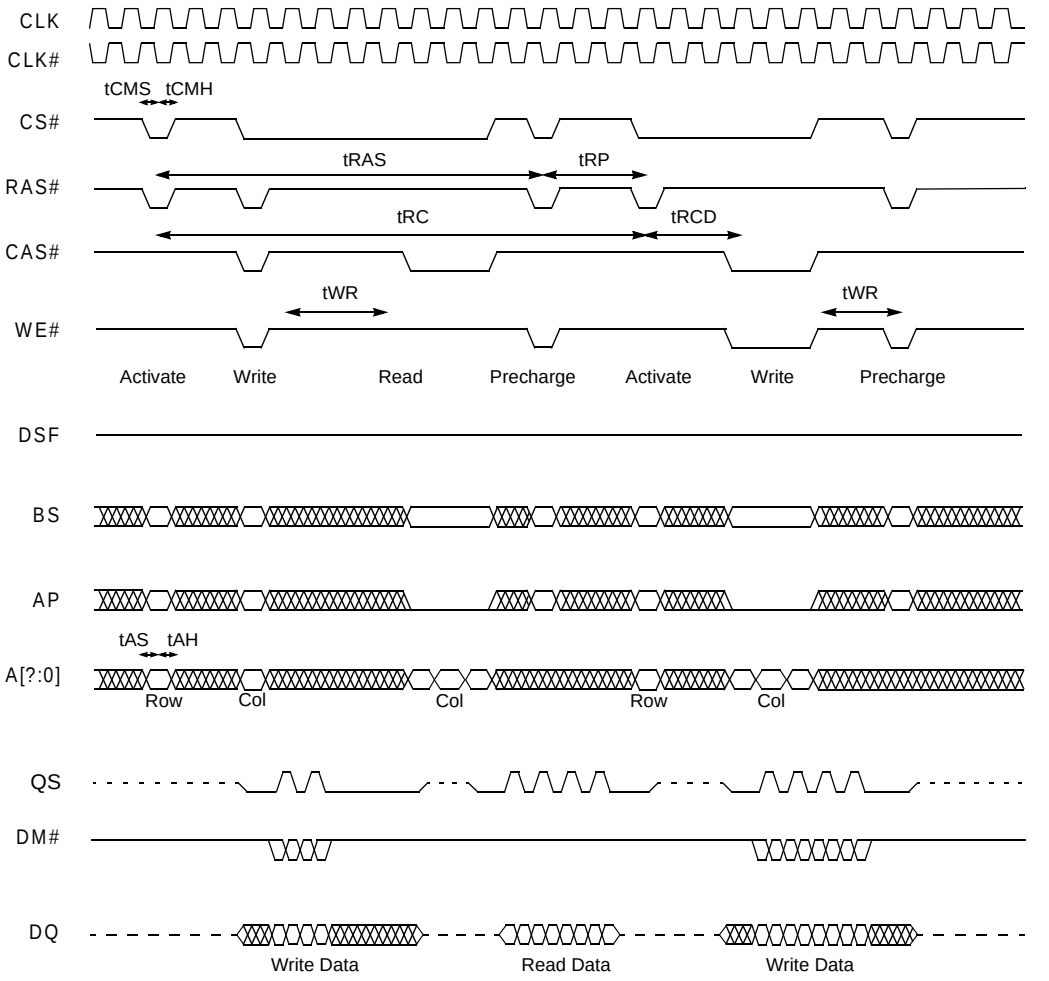
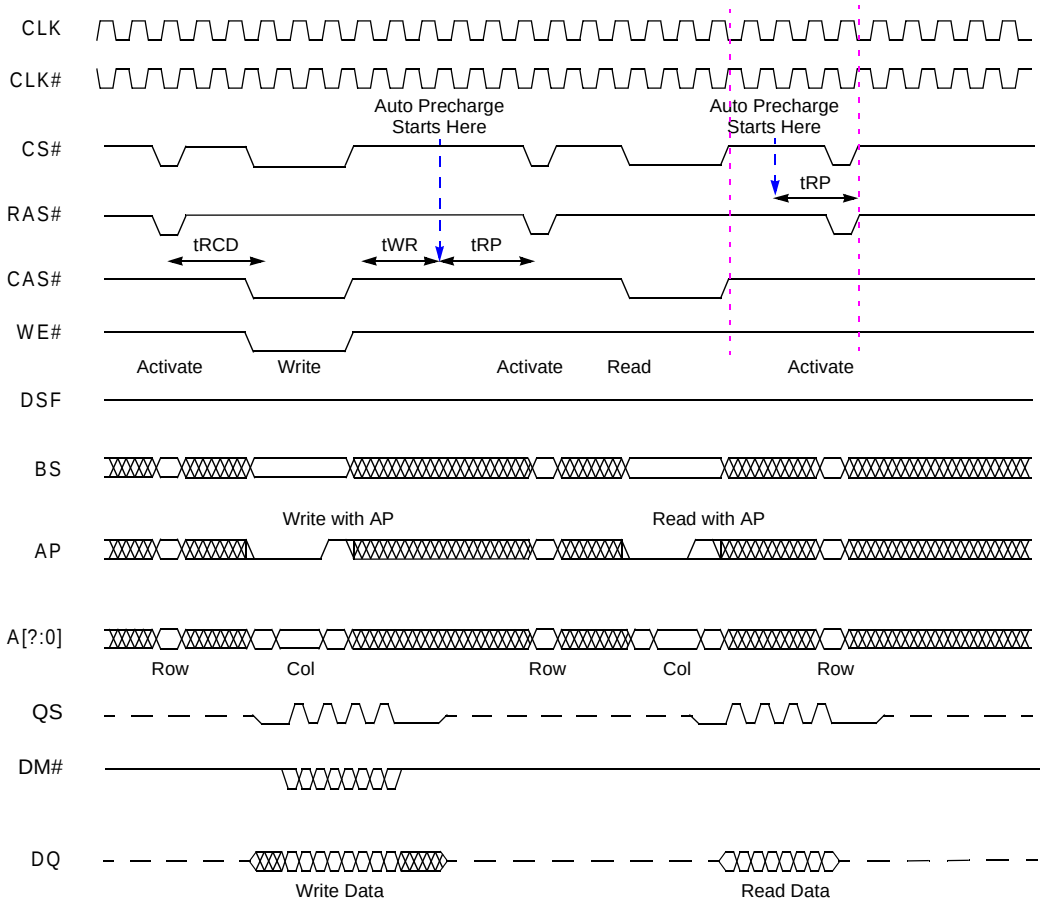


Figure 5-11. SDRAM/SGRAM Basic Read/Write Cycle Timing



Read and Write Cycles with Auto Precharge
Burst Length = 4, CAS Latency = 3

Figure 5-12. Read/Write Cycles with Auto Precharge

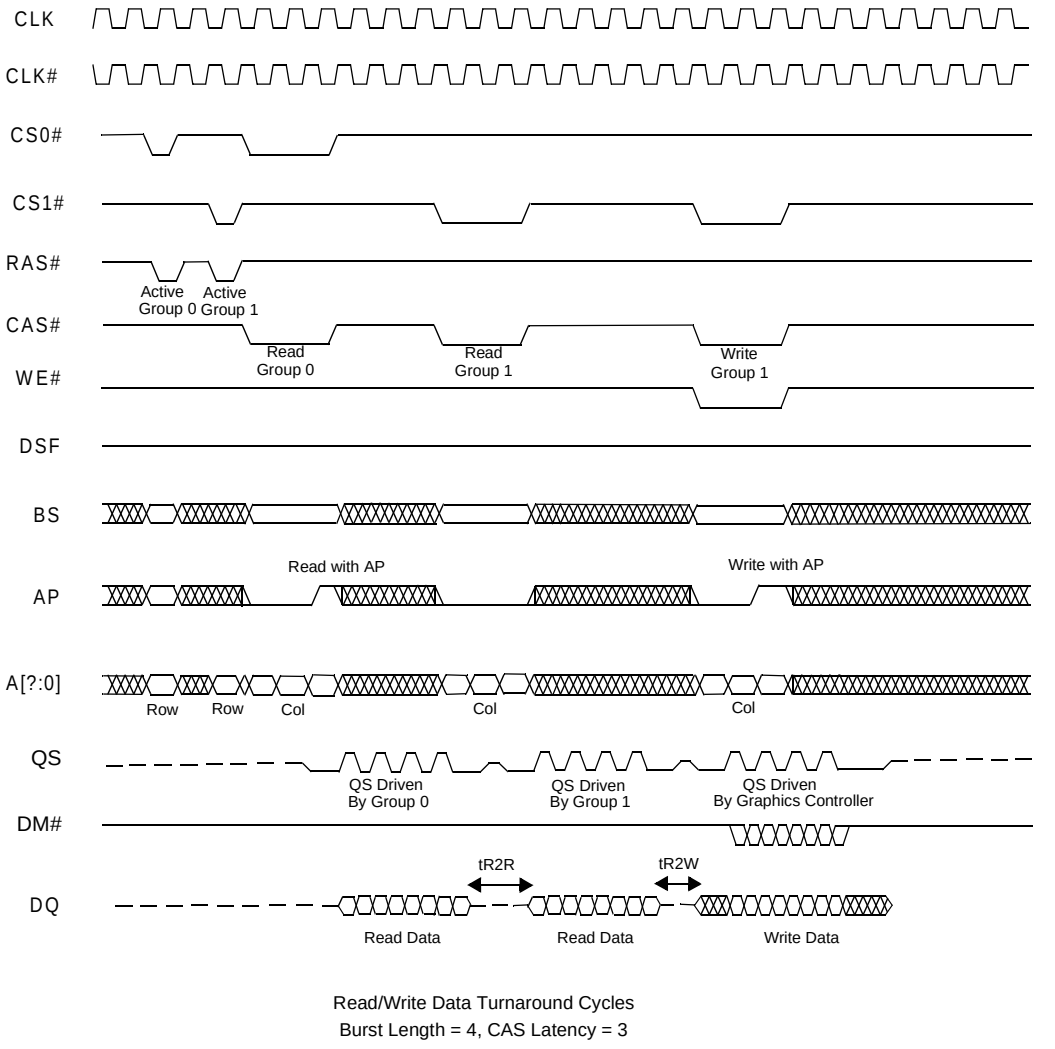
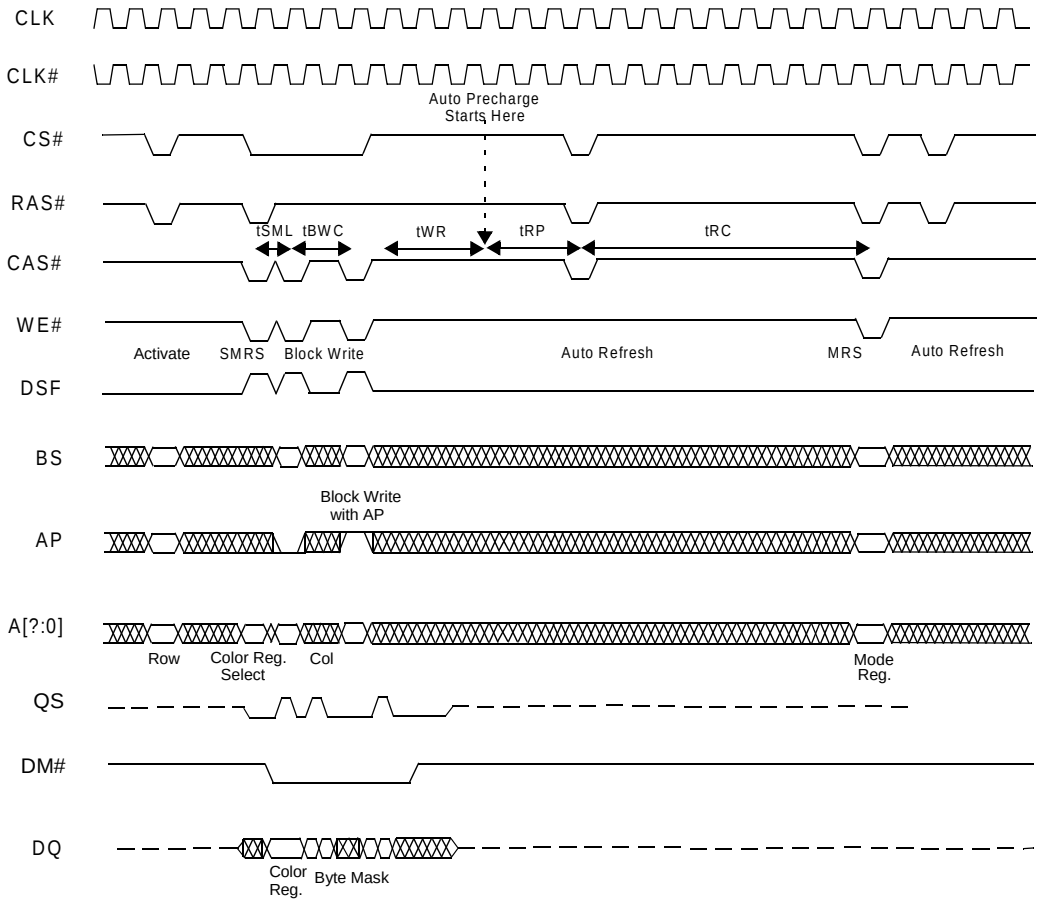


Figure 5-13. Read/Write Data Turnaround Cycles



Block Write, Mode Register, and Refresh Cycles

Figure 5-14. Block Write, Mode Register, and Refresh Cycles

5.2.5 I²C Timing

Write Cycle

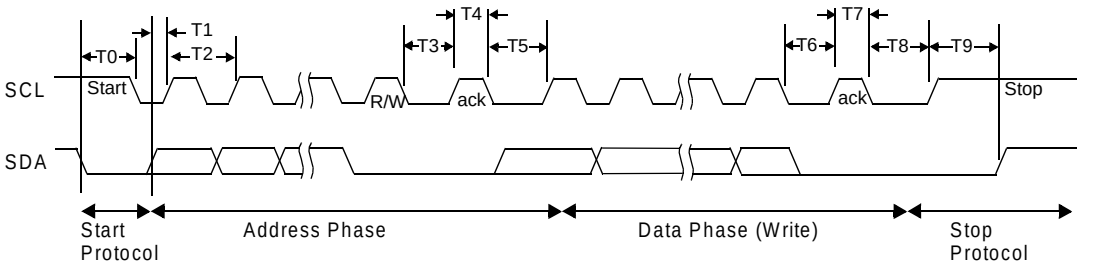


Figure 5-15. I²C Write Cycle

Table 5-8 I²C Write Cycle Timing Parameters

Parameter	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of writing data to the ACK from slave	$7T_{period}/4$	$7T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	$3T_{period}/4$	$3T_{period}/4$
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

Read Cycle

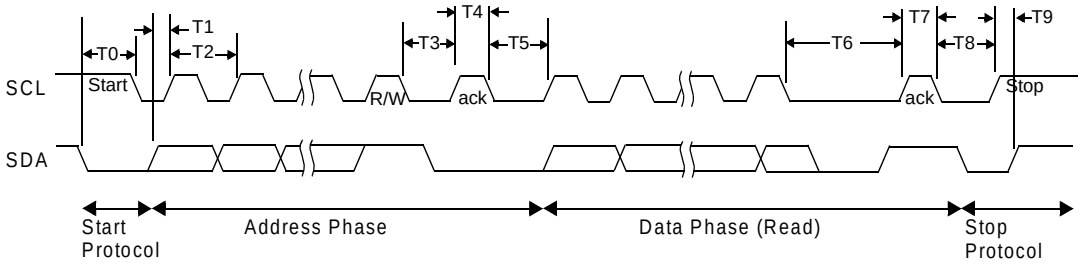


Figure 5-16. I²C Read Cycle

Table 5-9 I²C Read Cycle Timing Parameters

Parameter	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of reading data to ACK from master	$3T_{period}/4$	$3T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	T_{period}	T_{period}
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

5.2.6 MPP Timing

Basic Read/Write Cycle (No Wait State)

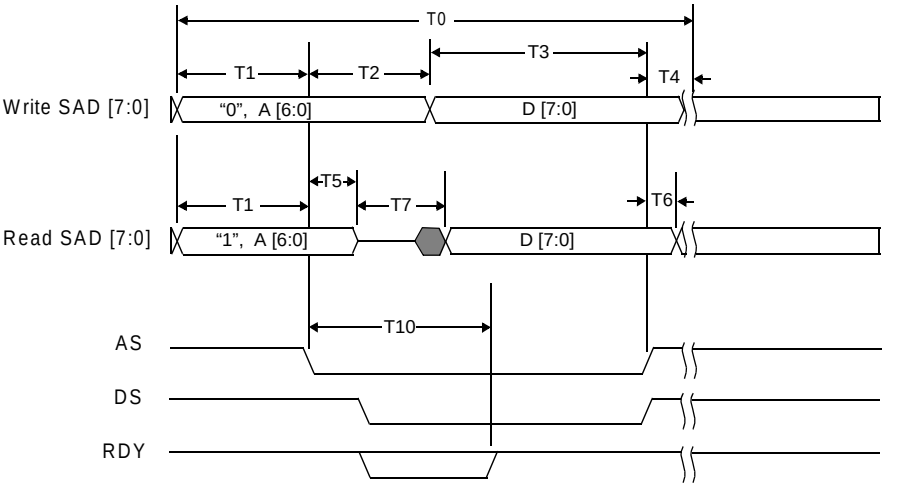


Figure 5-17. MPP Read/Write Cycle (No Wait State)

Table 5-10 MPP Read/Write Cycle Timing Parameters (No Wait State)

Parameter	Description	Min (ns)	Max (ns)
T0	Read/Write cycle time	90	180
T1	Address setup to AS	20	40
T2	Address hold (write cycle)	20	40
T3	Write data setup to DS rising (write cycle)	40	80
T4	Write data hold	10	20
T5	Address to Hi-Z from falling AS (read cycle)	10	20
T6	Read data hold	0	14
T7	Falling DS to valid read data	0	45
T8	Falling AS to falling DS	10	20
T10	Rising AS to RDY high	30	70

Basic Read/Write Cycle (Wait State)

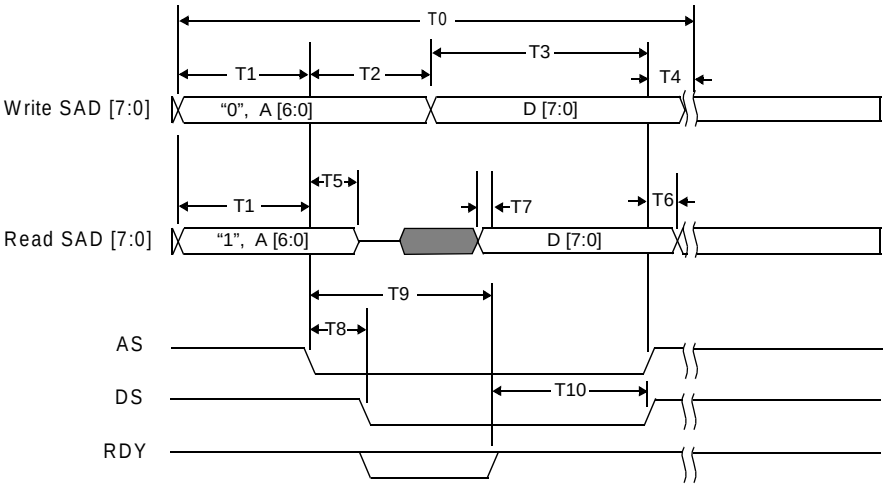


Figure 5-18. MPP Read/Write Cycle (Wait State)

Table 5-11 MPP Read/Write Cycle Timing Parameters (Wait State)

Parameter	Description	Min (ns)	Max (ns)
T0	Read/Write cycle time	90	180
T1	Address setup to AS	20	40
T2	Address hold (write cycle)	20	40
T4	Write data hold	10	20
T5	Address to Hi-Z from falling AS (read cycle)	10	20
T6	Read data hold	0	14
T7	Read data valid to RDY high	5	-
T8	Falling AS to falling DS	10	20
T10	Rising AS to RDY low	30	70

Burst Read/Write Cycle

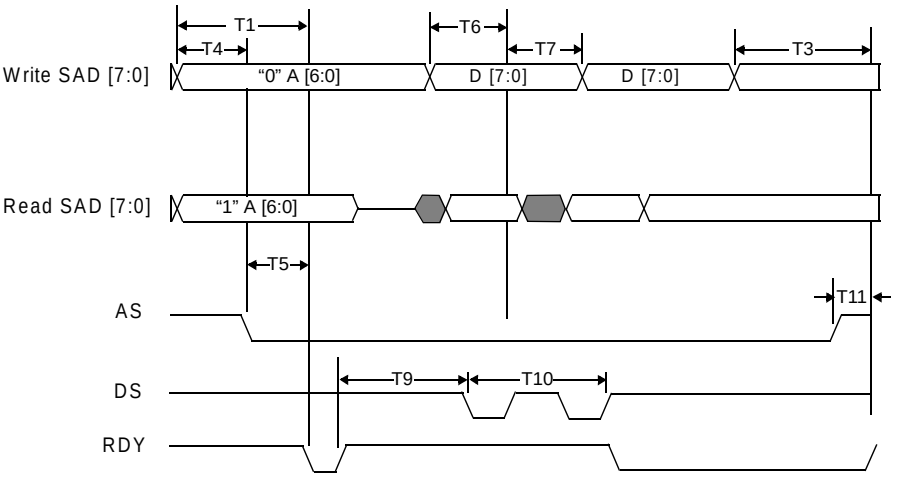


Figure 5-19. MPP Burst Read/Write Cycle

Table 5-12 MPP Burst Read/Write Cycle Timing Parameters

Parameter	Description	Min (ns)	Max (ns)
T1	Header Cycle time	40	-
T3	Footer Cycle time	40	-
T4	Address setup to AS	20	-
T5	Address hold	20	-
T6	Data setup to DS	20	-
T7	Data hold	20	-
T8	Falling AS to SRDY being driven	0	20
T9	Request to start of Burst Write	20	-
T10	Request hold after falling DS	0	10
T11	Rising AS to SRDY Hi-Z	0	20

5.2.7 VIP Host Basic Timings and Protocol

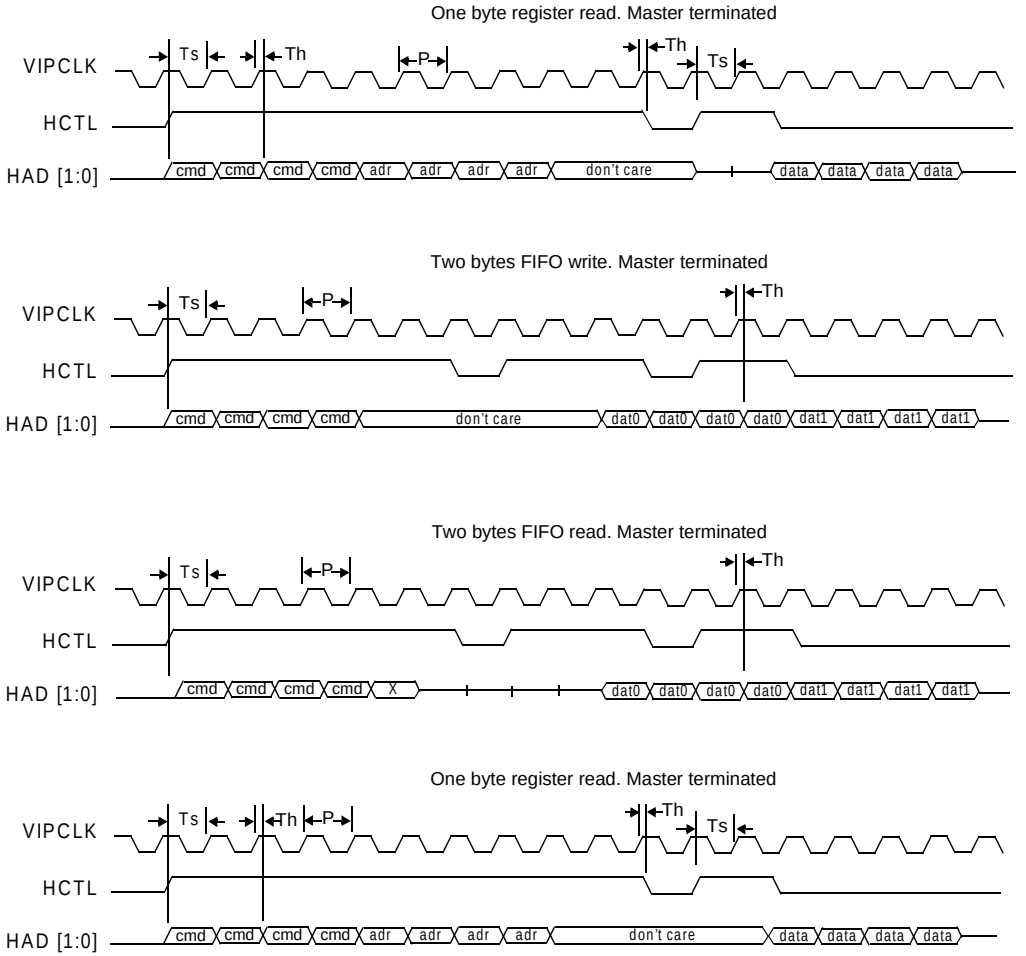


Figure 5-20. VIP Timings and Protocol

Table 5-13 VIP Timing Parameters

Symbol	Description	Min (ns)	Max (ns)
P	Clock period	-	33
Th	Hold time for hctl and had	0	-
Ts	Setup time for hctl and had	5	-

5.3 ROM Read/Write Timing (for 128K EPROMs, Add-in Board Implementation)

The ROM cycle (read/write) is split into two phases:

1- Addresses and ROM control signals are shift-loaded into the external flops in the first phase.

2- The actual ROM cycle (where CE# is asserted).

Note: The timing diagrams for 32K/64K EPROMs are similar except that SDA drives OE# directly and the inverted version of SDA drives WE#.

5.3.1 ROM Write Timing Diagram

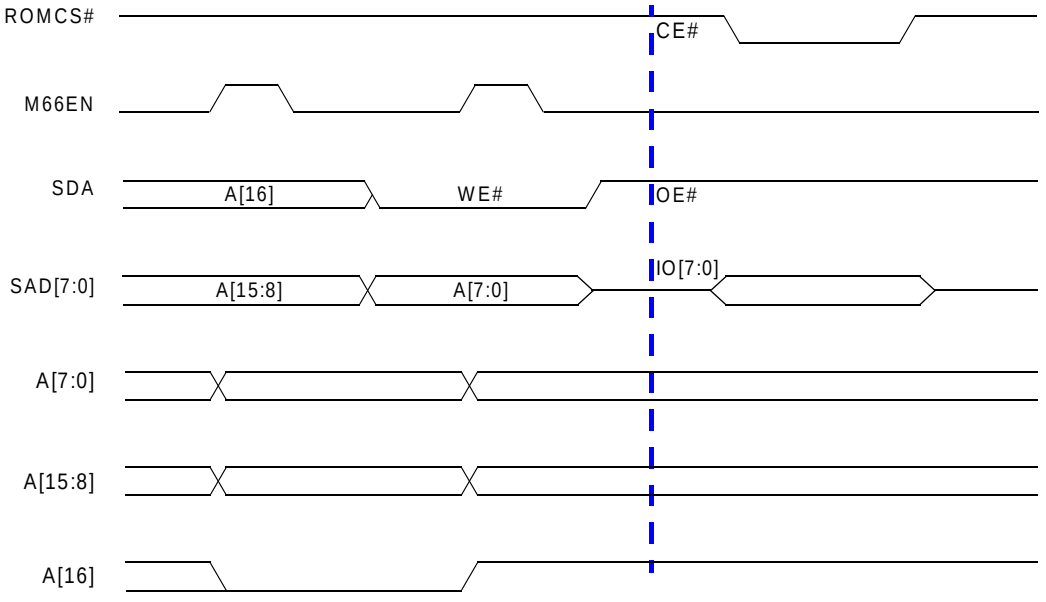


Figure 5-21. ROM Write

5.3.2 ROM Read Timing Diagram

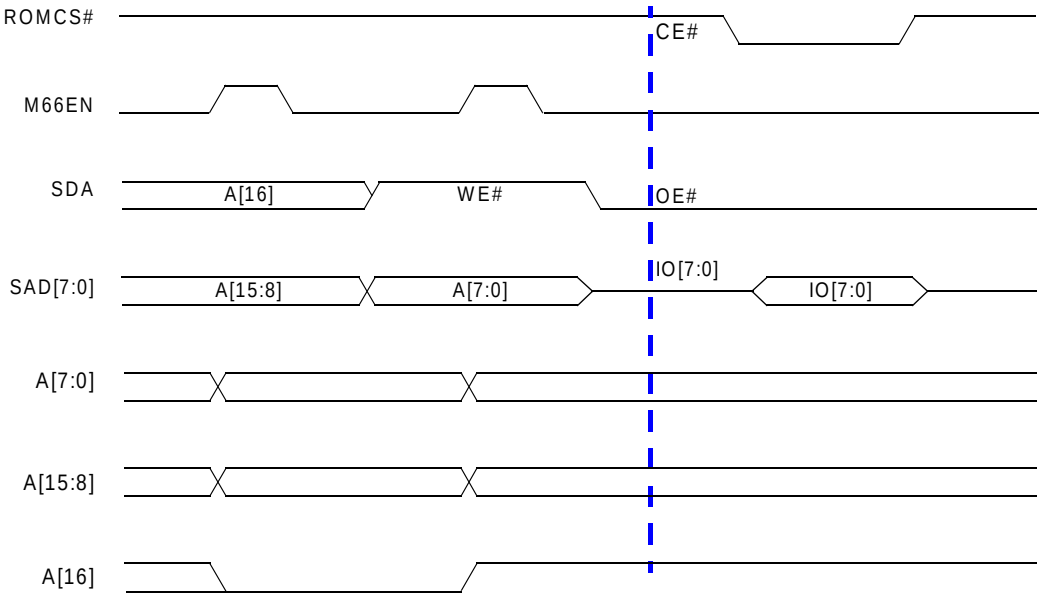


Figure 5-22. ROM Read

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Chapter 6
Electrical and Physical Data

6.1 Electrical Characteristics

All voltages are with respect to VSS unless specified otherwise.

6.1.1 Maximum Rating Conditions

Note: These are stress ratings only, i.e., operation of the device at these conditions is not implied. Ratings are referenced to VDD. Any stress greater than the *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 6-1 Maximum Rating Conditions

Item	Value
Supply Voltage (VDD)	-0.50 V to +6.00 V
Input or Output Voltage	-0.50 V to (VDD + 0.50 V)
DC Forward Bias Current	-12 mA (source), +24 mA (sink)
Storage Temperature (Plastic)	-40 ^{o}C to +125 ^{o}C

6.1.2 Recommended DC Operating Conditions

Table 6-2 Recommended DC Operating Conditions

Item	Value
I/O Supply (VDDR1)	(3.3 / 2.5 V) ± 5%
I/O Supply (VDDR2)	(3.3 / 2.5 V) ± 5%
I/O Supply (VDDR3)	3.3 V ± 5%
PCI/AGP I/O Supply (VDDQ)	3.3 V ± 5%
Digital Core Supply (VDDC)	2.5 V ± 5%
Analog (DAC) Supply (AVDD)	2.5 V ± 5%
PLL Supply (PVDD)	2.5 V ± 5%
Operating Case Temperature (Tc)	0 ^{o}C to +95 ^{o}C

6.1.3 TTL Interface

Table 6-3 TTL Interface (GPIOs)

Parameter	Condition	Min.	Typical	Max.
VIL - Low Level Input Voltage	-	-	-	0.8 V
VIH - High Level Input Voltage	-	2.0 V	-	-
VOL - Low Level Output Voltage	IOL = Rated buffer current	-	0.2 V	0.4 V
VOH - High Level Output Voltage	IOH = Half-rated buffer current	2.4 V	3.4 V	-

6.1.4 DAC Characteristics

Table 6-4 DAC Characteristics

Parameter	Min	Typ	Max	Notes
Resolution	8 bits	-	-	a
Vo (max) - Maximum Output Voltage	1.4 V	-	-	a
Io (max) - Maximum Output Current	-	40 mA	-	a
Full Scale Error	-10%	-	+10%	b,c
DAC to DAC Correlation	-2%	-	+2%	a,d
Integral Linearity	-0.5 lsb	-	+0.5 lsb	a,e
Rise Time (10% to 90%)	-	-	3 ns	a,f
Full Scale Settling Time	-	<8 ns	-	a,g,h
Glitch Energy	-	60 pV-s	-	a,h
Monotonicity	-	-	-	i

Notes:
a - Tested over the operating temperature range, at nominal supply voltage, with an Iref of -3.04 mA. Iref is the level of the current flowing in the Rset resistor.
b - Tested over the operating temperature range, at reduced supply voltage, with an Iref of -3.04 mA. Iref is the level of the current flowing in the Rset resistor.
c - Full scale error from the value predicted by the design equations.
d - About the mid point of the distribution of the three DACs measured at full scale deflection.
e - Linearity measured from the best fit line through the DAC characteristics. Monotonicity guaranteed.
f - Load = 37.5 Ω + 20 pF with Iref = -3.04 mA (Iref is the current flowing in the Rset resistor).
g - From a 2% change in the output voltage until settling to within 2% of the final value.
h - This parameter is sampled, not 100% tested.
i - Monotonicity is guaranteed.

6.1.5 General

Table 6-5 General Interface

Parameter	Condition	Min.	Typical	Max.
IIL - Low Level Input Current	VI = VSS	-	-	+1 µA
IIH - High Level Input Current	VI = VCC	-	-	-1 µA
IOZ - Tristate Output Leakage	VO = 0 V or VCC	-	-	± 10µA
CIN - Input Capacitance	Freq = 1 MHz @ 0 V	-	4 pF	8 pF
CO - Output Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	-
CIO - Bidirectional I/O Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	10 pF
IKLU - I/O Latch-up Current	V<VSS, V>VCC	500 mA	-	-
VEPO - Electrostatic Protection	C=100 pF R=1.5 kΩ	2 kV	-	-

6.1.6 Memory Interface Electrical Characteristics

Table 6-6 Memory Interface Electrical Characteristics

	SSTL-2			SSTL-3		
Parameters	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
VDD (Core) - Device voltage supply	VDDR	-	-	2.3 V	-	-
VDDR (Ring) - Output voltage supply	2.3 V	2.5 V	2.7 V	3.0 V	3.3 V	3.6 V
VREF* - Input reference voltage = 0.5 x VDD for SSTL2, = 0.45 x VDD for SSTL3)	1.15 V	1.25 V	1.35 V	1.3 V	1.5 V	1.7 V
VTT - Termination voltage	Vref -40 mV	Vref	Vref +40 mV	Vref -50 mV	Vref	Vref +50 mV
VIH(dc) - DC input logic HIGH	Vref +180 mV	-	VDDR +300 mV	Vref +200 mV	-	VDDR +300 mV
VIL(dc) - DC input logic LOW	-300 mV	-	Vref -180 mV	-300 mV	-	Vref -200 mV
VIH(ac) - AC input logic HIGH	Vref +350 mV	-	-	Vref +400 mV	-	-
VIL(ac) - AC input logic LOW	-	-	Vref -350 mV	-	-	Vref -400 mV

Table 6-6 Memory Interface Electrical Characteristics (Continued)

	SSTL-2			SSTL-3		
Parameters	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
Delta Vout1 (7.6 mA x 50 Ω)	380 mV	380 mV	380 mV			
Delta Vout2 (0.38V + (0.38 V / 2))	570 mV	570 mV	570 mV			
Output High Driver (worst case):						
Vmin at VIN (1.11 V + 350 mV)	1.47 V	1.47 V	1.47 V			
Vmin at VOUT (1.11 V + 0.57 V)	1.69 V	1.69 V	1.69 V			
Imin output (0.57 V + 0.38 V) / 25 Ω	-7.6 mA	-7.6 mA	-7.6 mA			
Max.ON resistor (2.5 V - 1.25 V - 0.57 V) / 7.6 mA	80.26 Ω	89.47 Ω	98.68 Ω			
Output Low Driver (worst case):						
Vmax at VIN (1.11 V - 0.35 V)	0.77 V	0.90 V	1.03 V			
Vmax at VOUT(1.11 V - 0.57 V)	0.55 V	0.68 V	0.81 V			
Imin output	7.6 mA	7.6 mA	7.6 mA			
Max.ON resistor	72.37 Ω	89.47 Ω	106.58 Ω			

Notes:
- Peak to peak AC noise on VREF may not exceed ± 25 mV (± 0.2% VREF).
- VTT of transmitting device must track VREF of receiving device.
- The 1 V/ns input signal minimum slew rate is to be maintained.

* In cases where the differential signaling interface on the memory is not used, e.g., in Single Data Rate mode, Vref should be connected to the memory I/O's VDDR (3.3 V or 2.5 V).

6.1.7 Clamp Pins Connections and Voltages

Two clamp pins (AGPCLAMP and GIOCLAMP) are used to provide the following:

- Signal integrity and overshoot protection of input signals to the chip
- 5 V tolerance capability with respect to input signals to the chip.

The board level connection guidelines of these pins are as follows:

- For the AGPCLAMP pin:
  - For AGP systems with 3.3 V signaling, use 3.3 V.
  - For PCI systems with 3.3 V signaling, use 3.3 V.
  - For PCI systems with 5 V signaling, use 5.5 V.

- For the GIOCLAMP pin:
  - For 5 V GIO signals sent to the chip, use 5 V.
  - For 3.3 V GIO signals sent to the chip, use 3.3 V.

6.1.8 Calculating RSET Resistance (DAC Interface)

A precision resistor (with 1% of nominal) is placed between RSET (pin 123) and analog ground (AVSS) to set the full-scale DAC current. This resistance is typically 422 Ω for PS/2 applications where the effective impedance is 37.5 Ω (doubly terminated 75 Ω loads, shown in Figure 8-1). The 422 Ω is an acceptable value for RSET with a slightly reduced white level.

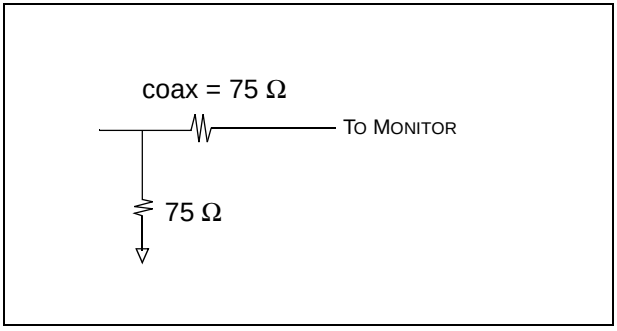

Figure 6-1. PS/2 Example

The required resistor value can be calculated using the formula:

$$\mathbf{RSET\ (\Omega) = (6.22 \times V_{REF} \times \alpha) / I_{OUT}}$$

where: 6.22 is the idealized 8-bit gain constant

V_{REF} is the idealized reference voltage (1.2 V)

α is the systematic **composite** skew on idealized V_{REF} and gain constant. It has been empirically determined to be 1.051 from data logging. This amounts to a 5.1% overall correction. (2.9% attributed to V_{REF} and 2.2% to the gain constant)

I_{OUT} is the required DAC full-scale current given by:

$$\mathbf{I_{OUT} = (V_{WHITE} - V_{BLACK}) / Z_{EFF}}$$

For: V_{WHITE} = 0.7 V
V_{BLACK} = 0 V
Z_{EFF} = 37.5 Ω

I_{OUT}= (0.7 V - 0 V) / 37.5 Ω = 0.0186 A

Defining RSET in this fashion allows for a one-time compensation for the systematic skew due to shifts on both V_{REF} and the gain constant on the output white level by adjustment of α.

The variation in α has been set to be 10%, of which 6% has been attributed to the bandgap (V_{REFM} = 1.2 x 1.029 ± 6% = 1.235 ± 6%), and the rest (4%) to the variation of the gain constant. Hence,

I_{OUT} max = 18.6 mA x 1.1
I_{OUT} min = 18.6 mA x 0.9

PS/2 Example:

RSET (Ω) = (6.22 x V_{REF} x α) / I_{OUT}
= (6.22 x 1.2 x 1.051) / 0.0186
= 422 Ω

Table 6-7 PS/2 DAC Characteristics*

Parameter	Min.	Typ.	Max.	Unit
V_{WHITE}	630	700	770	mV
I_{OUT}	-10%	18.6	+10%	mA

* Values obtained using 37.5 Ω load, 422 Ω (± 1%) RSET with 8-bit white level.

6.1.9 Analog Output Specification

Conceptually, each 8-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

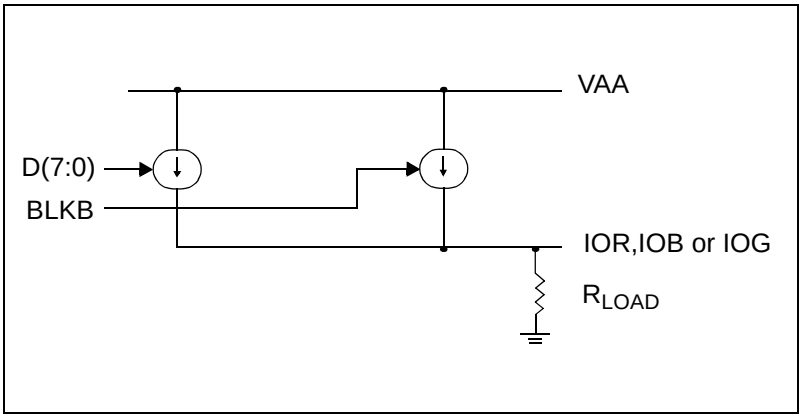

Figure 6-2. Analog Output (DAC)

With a 75 Ω doubly-terminated load, V_{REFM} = 1.235 V, and RSET = 422 Ω, PS/2 levels are shown below, with pedestal current set to 7.5 IRE.

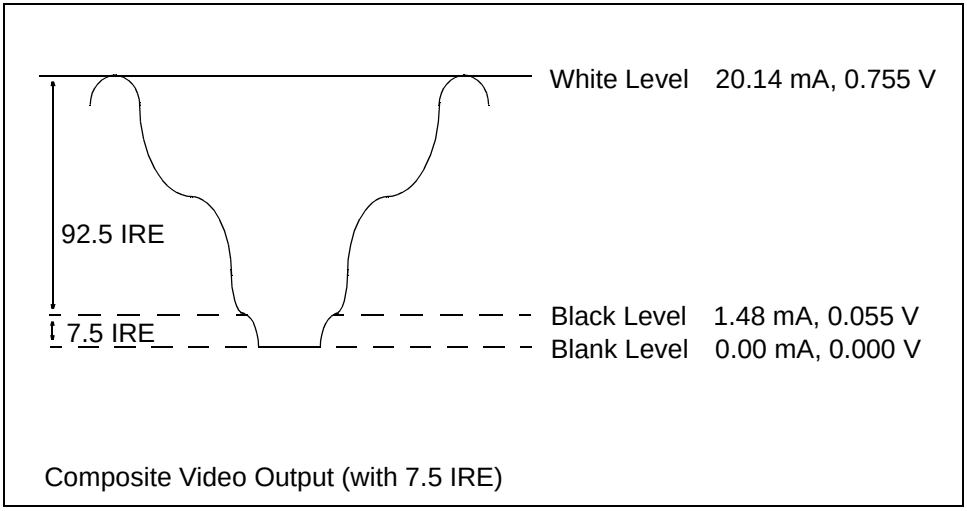

Figure 6-3. Analog Output (Composite)

6.2 Thermal Characteristics

The thermal operation characteristics of the chip depend on the board it is mounted on. The tables below present the values of θCA (case-to-ambient thermal resistance) and TA*max* (maximum ambient temperature) for different airflows over the chip.

Table 6-8 Single-layer Board

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	21.0	15.8	14.5	11.9	11.3
TA*max*(°C)	28	44	49	57	59

Table 6-9 Multi-layer Board with Ground Plane

Airflow (m/s)	0	0.5	1.0	2.0	3.0
θCA(°C/W)	17.6	14	12.5	10.4	10.0
TA*max*(°C)	39	50	55	62	63

6.2.1 Maximum Ambient Temperature

Typical maximum ambient temperatures (TA*max*) can be derived from the maximum case temperature (TC*max*), power dissipation, and case-to-ambient thermal resistance (θCA) as follows:

$$\mathbf{TA}max = \mathbf{TC}max - \mathbf{P} * \theta\mathbf{CA}$$

Power dissipation (**P**) range varies with different display frequencies but is typically between 1.0 W to 2.0 W when chip is operating at nominal VDD. Case temperature (**TC**) may be measured in any environment, and should be taken at the center of the top surface of the device.

6.2.2 Junction Temperature

The junction-to-case thermal resistance (θJC) of this device is approximately 6.7°C/W. Junction temperature (TJ) may be calculated as follows:

$$\mathbf{T_J} = (\theta\mathbf{JC} + \theta\mathbf{CA}) * \mathbf{P} + \mathbf{T_A}$$

The maximum allowed junction temperature is 100 °C.

6.3 Power and Case Temperature Measurements

TBD

Table 6-10 Power Consumption and Case Temperature

Operation Conditions	ASIC		SGRAM (4M)
	Power	Case Temp.	

Note: Room temperature was 23.9 ^{o}C.

6.4 Physical Dimensions

6.4.1 272 BGA Package (RAGE 128VR)

Package Outline: PBGA 27x27mm - 256 +16

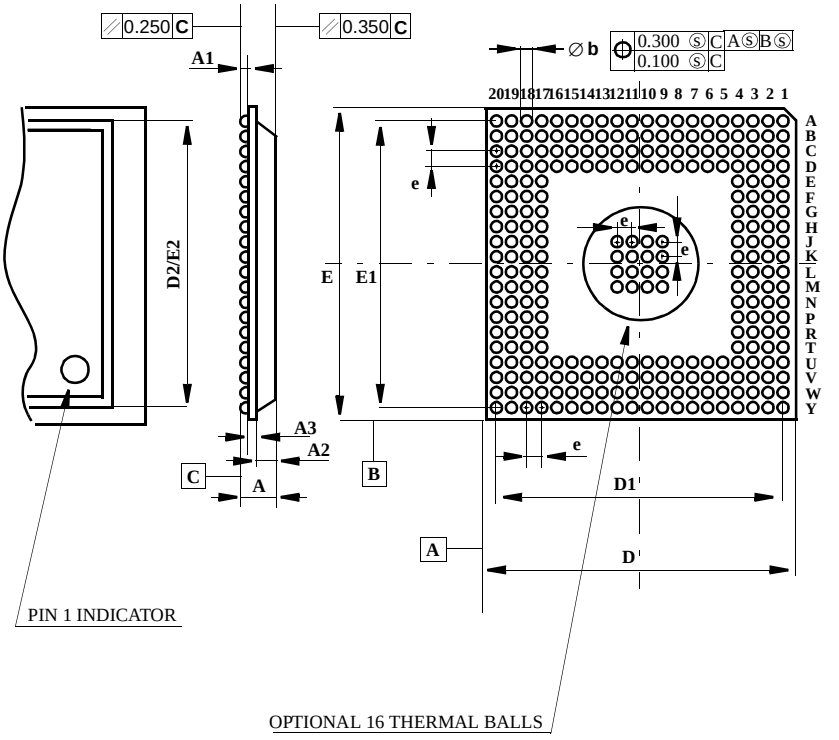

Figure 6-4. Physical Dimensions for 272-Pin BGA Package (RAGE 128VR)

Table 6-11 272 BGA Physical Dimensions

Ref.	Typical (mm)	Min. (mm)	Max. (mm)
A	2.13	1.93	2.33
A1	0.6	0.50	0.70
A2	1.17	1.12	1.22
A3	0.36	0.31	0.41
b	0.75	0.60	0.90
D	27.00	26.82	27.18
D1	24.13 BASIC		
D2	24.00	23.90	24.10
e	1.27 BASIC		
E	27.00	26.82	27.18
E1	24.13 BASIC		
E2	24.00	23.90	24.10

6.4.2 328 BGA Package (RAGE 128GL)

Package Outline: PBGA 27x27mm - 312 +16

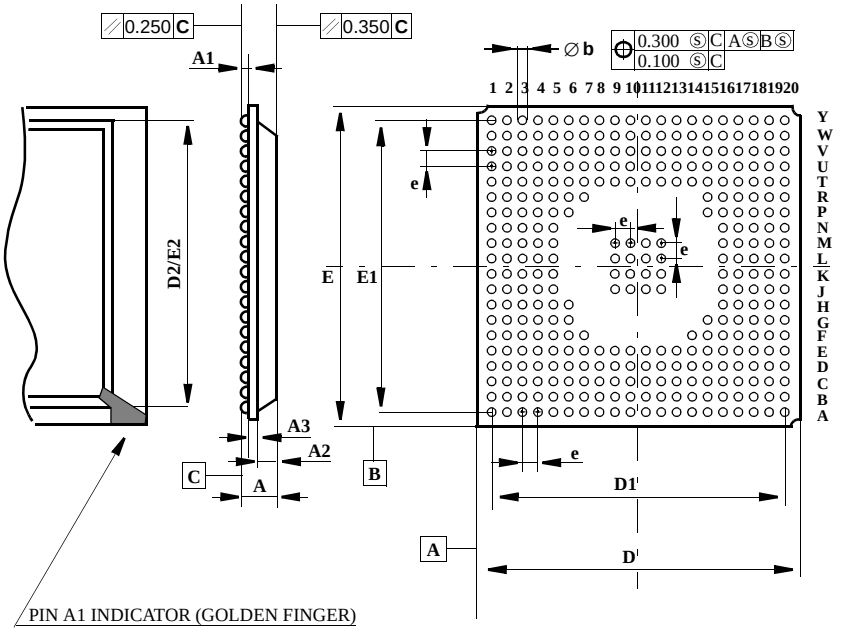

Figure 6-5. Physical Dimensions for 328-Pin BGA Package

Table 6-12 328-Pin PBGA Package Physical Dimensions

Ref.	Typical (mm)	Min. (mm)	Max. (mm)
A	2.13	1.93	2.33
A1	0.6	0.50	0.70
A2	1.17	1.12	1.22
A3	0.36	0.31	0.41
b	0.75	0.60	0.90
D	27.00	26.82	27.18
D1	24.13 BASIC		
D2	24.00	23.90	24.10
e	1.27 BASIC		
E	27.00	26.82	27.18
E1	24.13 BASIC		
E2	24.00	23.90	24.10

6.4.3 329 BGA Packages

Package Outline: BGA 31x31mm - 304 +25

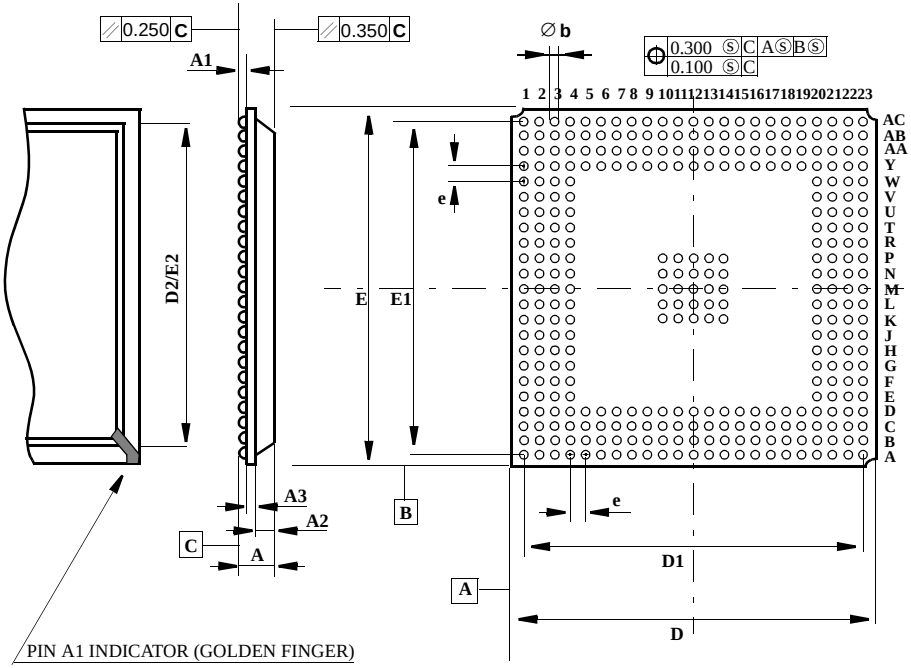

Figure 6-6. 329-pin BGA Physical Dimensions

Table 6-13 329 BGA Packages Physical Dimensions (in mm)

Ref	Min	Normal	Max
A	1.93	2.13	2.33
A1	0.50	0.60	0.70
A2	1.12	1.17	1.22
A3	0.31	0.36	0.41
b		0.75	
D	30.80	31.50	31.20
D1		27.94	
D2	28.90	29.00	29.10
e		1.27	
E	30.80	31.50	31.20
E1		27.94	
E2	28.90	29.00	29.10

6.5 Environmental Requirements

6.5.1 Ambient Temperature

Operation: 50 °F to 122 °F (10 °C to 50 °C)

Storage: 32 °F to 162 °F (0 °C to 70 °C)

6.5.2 Relative Humidity

Operation: 5% to 90% non-condensing

Storage: 0% to 95%

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Appendix A
Pin Listings

A.1 272, 328, and 329 BGA Pins Sorted by Signal Name

Note: Power and Ground Pins are listed separately in *Table A-2 on page A-11*

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
A0	Y18	U17	Y22	Memory Address line	Tristate
A1	Y19	U8	Y23	Memory Address line	Tristate
A2	Y20	U19	W21	Memory Address line	Tristate
A3	W18	U20	W22	Memory Address line	Tristate
A4	W19	T17	W23	Memory Address line	Tristate
A5	W20	T18	V21	Memory Address line	Tristate
A6	V18	T19	V22	Memory Address line	Tristate
A7	V19	T20	V23	Memory Address line	Tristate
A8	V20	R17	U21	Memory Address line	Tristate
A9	U18	R18	U22	Memory Address line	Tristate
A10	U19	R19	U23	Memory Address line	Tristate
A11	U20	R20	T21	Select Bank	Tristate
AD0	V16	W19	AB22	Address/data	Bi
AD1	W16	Y20	AC23	Address/data	Bi
AD2	V15	W18	AB21	Address/data	Bi
AD3	Y16	Y19	AC22	Address/data	Bi
AD4	W15	W17	AB20	Address/data	Bi
AD5	Y15	Y18	AC21	Address/data	Bi
AD6	V14	W16	AB19	Address/data	Bi
AD7	W14	Y17	AC20	Address/data	Bi
AD8	Y14	Y16	AC19	Address/data	Bi
AD9	V12	U15	AA17	Address/data	Bi
AD10	Y13	Y15	AB18	Address/data	Bi
AD11	W12	U14	AB17	Address/data	Bi
AD12	Y12	W14	AC17	Address/data	Bi
AD13	V11	V14	AA16	Address/data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
AD14	Y11	Y14	AC16	Address/data	Bi
AD15	W11	U13	AB16	Address/data	Bi
AD16	V8	U11	AA13	Address/data	Bi
AD17	W8	Y11	AB12	Address/data	Bi
AD18	W7	V11	AA12	Address/data	Bi
AD19	Y7	Y10	AC12	Address/data	Bi
AD20	V7	V10	AB11	Address/data	Bi
AD21	Y6	W10	AC11	Address/data	Bi
AD22	W5	U10	AA11	Address/data	Bi
AD23	Y5	Y9	AC10	Address/data	Bi
AD24	W3	V7	AB9	Address/data	Bi
AD25	Y3	Y7	AB8	Address/data	Bi
AD26	V3	U7	AA8	Address/data	Bi
AD27	Y2	W7	AC8	Address/data	Bi
AD28	W2	T6	AB7	Address/data	Bi
AD29	Y1	V6	AC7	Address/data	Bi
AD30	V2	U6	AA7	Address/data	Bi
AD31	W1	W6	AC5	Address/data	Bi
AD_STB0	W13	W15	AC18	AGP-133 Address strobe	Bi
AD_STB1	Y4	Y8	AC9	AGP-133 Address strobe	
AGPCLAMP	U8	T11		5V tolerance clamp	
AGPGPIO0/AGP_BUSY#/CLKRUN#	U4	T5		Future AGP4x support / AGP / PCI power management output signal	
AGPGPIO1/STP_AGP#	V4	V8		Future AGP4x support / Power management input from AGP bus	
AGPGPIO2	U5	U8		Future AGP4x support	
AGPGPIO3	U13	U16		Future AGP4x support	
AS/HCNTL	J1	P2		MPP address strobe / VIP host control	Bi
B	N1	V1	V1	Blue	Out
BYTCLK	H1	N1	M1	MPP (Tvout) byte clock	Bi
C/BE#0	V13	V15	AA18	Bus Command / Byte Enable	Bi
C/BE#1	W10	Y13	AC15	Bus Command / Byte Enable	Bi
C/BE#2	Y8	W11	AC13	Bus Command / Byte Enable	Bi
C/BE#3	W4	W8	AA9	Bus Command / Byte Enable	

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
CAS#	L20	L20	J23	Column Address Strobe	
CLK0	N20	N20	M23	Memory Clock	
CLK0#	N19	N19	M22	Memory Clock bar	
CLK1	M20	M20	L23	Memory Clock (upper 32 bits DDR)	
CLK1#	M19	M19	L22	Memory Clock bar (upper 32 bits DDR)	
CS0	W17	V18	Y21	Chip select	Tristate
CS1	Y17	V19	AA21	Chip select	Tristate
CS2	V17	V20	AA22	Chip select	Tristate
CS3	U17	W20	AB23	Chip select	Tristate
DEVSEL#	Y10	W12	AC14	Device select	Bi
DQ0	L18	L17	J22	Memory Data	Bi
DQ1	L19	K17	H21	Memory Data	Bi
DQ2	K18	K18	H22	Memory Data	Bi
DQ3	K19	K19	H23	Memory Data	Bi
DQ4	K20	K20	G20	Memory Data	Bi
DQ5	J18	J16	G21	Memory Data	Bi
DQ6	J19	J17	G22	Memory Data	Bi
DQ7	J20	J18	F20	Memory Data	Bi
DQ8	H18	J19	F21	Memory Data	Bi
DQ9	H19	J20	F22	Memory Data	Bi
DQ10	H20	H16	F23	Memory Data	Bi
DQ11	G17	H17	E21	Memory Data	Bi
DQ12	G18	H18	E22	Memory Data	Bi
DQ13	G19	H19	E23	Memory Data	Bi
DQ14	G20	H20	D21	Memory Data	Bi
DQ15	F17	G16	D22	Memory Data	Bi
DQ16	F18	G17	D23	Memory Data	Bi
DQ17	F19	G18	C21	Memory Data	Bi
DQ18	F20	G19	C22	Memory Data	Bi
DQ19	E17	G20	C23	Memory Data	Bi
DQ20	E18	F16	B22	Memory Data	Bi
DQ21	E19	F17	B23	Memory Data	Bi
DQ22	E20	F18	A23	Memory Data	Bi
DQ23	D17	F19	A22	Memory Data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
DQ24	D18	F20	B21	Memory Data	Bi
DQ25	D19	E17	A21	Memory Data	Bi
DQ26	D20	E18	C20	Memory Data	Bi
DQ27	C18	E19	B20	Memory Data	Bi
DQ28	C19	E20	A20	Memory Data	Bi
DQ29	C20	D17	C19	Memory Data	Bi
DQ30	B20	D18	B19	Memory Data	Bi
DQ31	A20	D19	A19	Memory Data	Bi
DQ32	B19	D20	C18	Memory Data	Bi
DQ33	A19	C18	B18	Memory Data	Bi
DQ34	B18	C19	A18	Memory Data	Bi
DQ35	A18	C20	D17	Memory Data	Bi
DQ36	C17	B20	C17	Memory Data	Bi
DQ37	B17	A20	B17	Memory Data	Bi
DQ38	A17	B19	A17	Memory Data	Bi
DQ39	C16	A19	D16	Memory Data	Bi
DQ40	B16	B18	C16	Memory Data	Bi
DQ41	A16	A18	B16	Memory Data	Bi
DQ42	C15	C17	C15	Memory Data	Bi
DQ43	B15	B17	B15	Memory Data	Bi
DQ44	A15	A17	A15	Memory Data	Bi
DQ45	D14	E16	C14	Memory Data	Bi
DQ46	C14	D16	B14	Memory Data	Bi
DQ47	B14	C16	A14	Memory Data	Bi
DQ48	A14	B16	C13	Memory Data	Bi
DQ49	D13	A16	B13	Memory Data	Bi
DQ50	C13	E15	A13	Memory Data	Bi
DQ51	B13	D15	C12	Memory Data	Bi
DQ52	A13	C15	B12	Memory Data	Bi
DQ53	D12	B15	A12	Memory Data	Bi
DQ54	C12	A15	C11	Memory Data	Bi
DQ55	B12	E14	B11	Memory Data	Bi
DQ56	A12	D14	A11	Memory Data	Bi
DQ57	D11	C14	C10	Memory Data	Bi
DQ58	C11	B14	B10	Memory Data	Bi
DQ59	B11	A14	A10	Memory Data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
DQ60	A11	E13	C9	Memory Data	Bi
DQ61	C10	D13	B9	Memory Data	Bi
DQ62	B10	C13	A9	Memory Data	Bi
DQ63	A10	B13	A8	Memory Data	Bi
DQ64	N/A	A11	N/A	Memory Data	Bi
DQ65	N/A	D10	N/A	Memory Data	Bi
DQ66	N/A	C10	N/A	Memory Data	Bi
DQ67	N/A	B10	N/A	Memory Data	Bi
DQ68	N/A	A10	N/A	Memory Data	Bi
DQ69	N/A	D9	N/A	Memory Data	Bi
DQ70 / ZVHREF/ LCD0	C9	C9		Memory Data / Zoom video ctlr / LCD interface data	Bi
DQ71/ ZVVSYNC / LCD1	B9	B9		Memory Data / Zoom video ctrl / LCD interface data	Bi
DQ72 / UV0 / LCD2	A9	A9		Memory Data / DVS2 data / LCD interface data	Bi
DQ73 / UV1 / LCD3	C8	D8		Memory Data / DVS2 data / LCD interface data	Bi
DQ74 / UV2 / LCD4	B8	C8		Memory Data / DVS2 data / LCD interface data	Bi
DQ75 / UV3 / LCD5	A8	B8		Memory Data / DVS2 data / LCD interface data	Bi
DQ76 / UV4/ LCD6	C7	A8		Memory Data / DVS2 data / LCD interface data	Bi
DQ77 / UV5 / LCD7	B7	E7		Memory Data / DVS2 data / LCD interface data	Bi
DQ78 / UV6 / LCD8	A7	D7		Memory Data / DVS2 data / LCD interface data	Bi
DQ79 / UV7 / LCD9	D6	C7		Memory Data / DVS2 data / LCD interface data	Bi
DQ80	N/A	B7	N/A	Memory Data	Bi
DQ81	N/A	A7	N/A	Memory Data	Bi
DQ82	N/A	E6	N/A	Memory Data	Bi
DQ83	N/A	D6	N/A	Memory Data	Bi
DQ84	N/A	C6	N/A	Memory Data	Bi
DQ85	N/A	B6	N/A	Memory Data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
DQ86 / SDS / LCD10 / SDA	C6	A6		Memory Data / MPP2 data strobe / LCD interface data / I2CDATA	Bi
DQ87 / SAS/ LCD11 / SCL	B6	E5		Memory Data / MPP2 adr. strobe / LCD interface data / I2CCLK	Bi
DQ88/ SSAD0/ LCD12	A6	D5		Memory Data / MPP2 data / LCD interface data	Bi
DQ89/ SSAD1/ LCD13	D5	C5		Memory Data / MPP2 data / LCD interface data	Bi
DQ90/ SSAD2/ LCD14	C5	B5		Memory Data / MPP2 data / LCD interface data	Bi
DQ91/ SSAD3/ LCD15	B5	A5		Memory Data / MPP2 data / LCD interface data	Bi
DQ92/ SSAD4/ LCD16	A5	C4		Memory Data / MPP2 data / LCD interface data	Bi
DQ93/ SSAD5/ LCD17	C4	B4		Memory Data / MPP2 data / LCD interface data	Bi
DQ94/ SSAD6/ LCD18	B4	A4		Memory Data / MPP2 data / LCD interface data	Bi
DQ95/ SSAD7/ LCD19	A4	B3		Memory Data / MPP2 data / LCD interface data	Bi
DQ96	N/A	A3	N/A	Memory Data	Bi
DQ97	N/A	B2	N/A	Memory Data	Bi
DQ98	N/A	A2	N/A	Memory Data	Bi
DQ99	N/A	A1	N/A	Memory Data	Bi
DQ100	N/A	B1	N/A	Memory Data	Bi
DQ101	N/A	C3	N/A	Memory Data	Bi
DQ102	N/A	C2	N/A	Memory Data	Bi
DQ103	N/A	C1	N/A	Memory Data	Bi
DQ104	N/A	D4	N/A	Memory Data	Bi
DQ105	N/A	D3	N/A	Memory Data	Bi
DQ106	N/A	D2	N/A	Memory Data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
DQ107	N/A	D1	N/A	Memory Data	Bi
DQ108	N/A	E4	N/A	Memory Data	Bi
DQ109	N/A	E3	N/A	Memory Data	Bi
DQ110	N/A	E2	N/A	Memory Data	Bi
DQ111	N/A	E1	N/A	Memory Data	Bi
DQ112	N/A	F6	N/A	Memory Data	Bi
DQ113	N/A	F5	N/A	Memory Data	Bi
DQ114	N/A	F4	N/A	Memory Data	Bi
DQ115	N/A	F3	N/A	Memory Data	Bi
DQ116	N/A	F2	N/A	Memory Data	Bi
DQ117	N/A	F1	N/A	Memory Data	Bi
DQ118	N/A	G5	N/A	Memory Data	Bi
DQ119	N/A	G4	N/A	Memory Data	Bi
DQ120	N/A	G3	N/A	Memory Data	Bi
DQ121	N/A	G2	N/A	Memory Data	Bi
DQ122	N/A	G1	N/A	Memory Data	Bi
DQ123	N/A	H5	N/A	Memory Data	Bi
DQ124	N/A	H4	N/A	Memory Data	Bi
DQ125	N/A	H3	N/A	Memory Data	Bi
DQ126	N/A	H2	N/A	Memory Data	Bi
DQ127	N/A	H1	N/A	Memory Data	Bi
DQM#0	P19	M18	M21	Memory data Byte write enable	Tristate
DQM#1	P18	M17	N22	Memory data Byte write enable	Tristate
DQM#2	R20	N17	P22	Memory data Byte write enable	Tristate
DQM#3	R19	N16	P21	Memory data Byte write enable	Tristate
DQM#4	R18	P19	R23	Memory data Byte write enable	Tristate
DQM#5	T20	P17	R21	Memory data Byte write enable	Tristate
DQM#6	T19	P16	T23	Memory data Byte write enable	Tristate
DQM#7	T18	R16	T22	Memory data Byte write enable	Tristate

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
DQM#8	N/A	A13	N/A	Memory data Byte write enable	Tristate
DQM#9	N/A	D12	N/A	Memory data Byte write enable	Tristate
DQM#10	N/A	C12	N/A	Memory data Byte write enable	Tristate
DQM#11	N/A	B12	N/A	Memory data Byte write enable	Tristate
DQM#12	N/A	A12	N/A	Memory data Byte write enable	Tristate
DQM#13	N/A	D11	N/A	Memory data Byte write enable	Tristate
DQM#14	N/A	C11	N/A	Memory data Byte write enable	Tristate
DQM#15	N/A	B11	N/A	Memory data Byte write enable	Tristate
DS/VIPCLK	H2	P1	N3	MPP data strobe/ VIP host clock	Bi
DSF	P17	N18	N21		Tristate
FRAME#	W9	V12	AB14	Cycle Frame	Bi
G	M1	U1	U1	Green	Out
GIOCLAMP	F4	M5	K4	5V tolerance clamp	
GNT#	T2	V5	AB4	PCI BM grant signal from arbiter	
HSYNC	M2	U2	U2	Horizontal Sync	Bi
INTA#	U3	U5		Interrupt request line	Tristate
IRDY#	Y9	Y12		Initiator (BM) ready	Bi
LCDCDE	E4	L5		LCD interface Display enable	Bi
LCDCLK	D2	L4		LCD interface clock	Bi
M66EN/ Biosffclk/ HAD1	U16	V17		clock for add-in card flops on Bios/VIP host data bit 1	
MONID0 / LCD20	K1	R3		Monitor DDC / LCD interface data	Bi
MONID1 / LCD21	K2	R4		Monitor DDC / LCD interface data	Bi
MONID2 / LCD22	K3	P4		Monitor DDC / LCD interface data	Bi
MONID3 / LCD23	J4	P5		Monitor DDC / LCD interface data	Bi

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
PAR	U10	V13	AA15	Parity for AD[31:0] and C/BE#[3:0]	Out
PCICLK	V1	Y6	AC4	BUS clock	
PCLK	E1	L3	J1	DVS clock	Bi
QS0	N18	L18	K21	Data Strobe (lower 32 bits DDR)	
QS1	M18	L19	J21	Data Strobe (upper 32 bits DDR)	
R	L1	T1	T1	Red	Out
RAS#	P20	P20	N23	Row Address Strobe	Tristate
RBF#	R3	W3	AC1	AGP read buffer full	
REQ#	U1	W5	AB3	PCI BM request signal to arbiter	
RESET#	U2	Y5	AB6	Active low PCI reset	
ROMCS#	D3	K5	J4	Bios Eprom Chip Select	
RSET	L2	T2	T2	DAC current set resistor	In
SAD4/HAD4	F1	M1	L3	MPP/VIP host data	Bi
SAD5/HAD5	F3	M2	K1	MPP/VIP host data	Bi
SAD6/HAD6	E3	M3	K2	MPP/VIP host data	Bi
SAD7/HAD7	E2	M4	K3	MPP/VIP host data	Bi
SAD0	G1	N2	M2	MPP data	Bi
SAD1	G2	N3	M3	MPP data	Bi
SAD2	G3	N4	L1	MPP data	Bi
SAD3	F2	N5	L2	MPP data	Bi
SB_STB	R1	Y3	AC3	Side band strobe for AGP1X/2X	
SBA0	N2	W1	W1	Sideband address port for AGP1X/2X	Bi
SBA1	N3	V3	W2	Sideband address port for AGP1X/2X	Bi
SBA2	P2	Y1	Y2	Sideband address port for AGP1X/2X	Bi
SBA3	P3	W2	Y3	Sideband address port for AGP1X/2X	Bi
SBA4	P1	Y2	Y1	Sideband address port for AGP1X/2X	Bi
SBA5	V5	U9	AA3	Sideband address port for AGP1X/2X	

Table A-1 272 BGA, 328 BGA and 329 BGA Pins Sorted by Signal Name (Continued)

Signal Name	272 BGA (128 VR)	328 BGA (128 GL)	329 BGA (128 VR-O)	Function	Type
SBA6	W6	W9	AA1	Sideband address port for AGP1X/2X	
SBA7/ IDSEL	V6	V9	AA2	Sideband address port for AGP1X/2X / PCI initialization device select	
SCL/HAD3/ VIPINT	J2	R1	P2	I^2C clock/VIP host data / VIP Interrupt	Bi
SDA2/HAD2	J3	R2	P3	I^2C data/VIP host data	Bi
SERR	N/A	N/A	AA10		
SRDY/INT/ HAD0	H3	P3	N1	MPP ready / VIP host data bit 0	Bi
ST0	T1	Y4	AC2	AGP status Bus	
ST1	T3	V4	AB2	AGP status Bus	
ST2	R2	W4	AB1	AGP status Bus	
STOP#	V10	W13	AB15	Target transaction termination required.	Bi
TESTEN	U15	V16	Y16	Test mode	
TRDY#	V9	U12	AA14	Target device ready	Bi
VREF	N17	M16	L21	DDR Reference Power supply	Analog
VSYNC	M3	V2	V2	Vertical Sync	Bi
WE#	R17	P18	R22	Memory write enable	Tristate
XTALIN	A1	L1	H2	Crystal in	In
XTALOUT	B1	L2	H1	Crystal out	Out
Y0	D1	K1	J2	DVS data	Bi
Y1	C1	K2	J3	DVS data	Bi
Y2	C2	K3	H3	DVS data	Bi
Y3	B2	K4	G1	DVS data	Bi
Y4	A2	J1	G2	DVS data	Bi
Y5	C3	J2	G3	DVS data	Bi
Y6	B3	J3	F1	DVS data	Bi
Y7	A3	J4	F2	DVS data	Bi

A.1.1 Power and Ground Pins

Table A-2 Power and Ground Pins

Signal Name	272 BGA	328 BGA	329 BGA	Description
VSS	J9	J9	D5	Ground (common core and I/O)
	J10	J10	D6	
	J11	J11	D9	
	J12	J12	D10	
	K9	K9	D12	
	K10	K10	D13	
	K11	K11	D14	
	K12	K12	D19	
	L9	L9	D20	
	L10	L10	E20	
	L11	L11	G4	
	L12	L12	K10	
	M9	M9	K11	
	M10	M10	K12	
	M11	M11	K13	
	M12	M12	K14	
	T17	R15	K20	
	J17	L16	L10	
	D15	F14	L11	
	D9	E11	L12	
	H4	E9	L13	
	R4	G6	L14	
	U7	R6	L20	
	U12	R7	M4	
		T8	M10	
		T10	M11	
		T13	M12	
		T16	M13	
			M14	
			M20	
			N10	
			N11	
			N12	
			N13	

Table A-2 Power and Ground Pins (Continued)

Signal Name	272 BGA	328 BGA	329 BGA	Description
VSS			N14	Ground (common core and I/O)
			P10	
			P11	
			P12	
			P13	
			P14	
			U20	
			V20	
			Y4	
			Y7	
			Y12	
			Y20	
AVSS	K4	R5	T3	BGR Analog Ground
	L4	T4	T4	Analog DAC Ground
PVSS	M4	U3	U4	PLL Ground
VDDC	L17	F15	T20	Core Power 2.5 V
	D8	E8	N20	
	P4	H6	D8	
	U11	T15	R4	
VDDQ	T4	T7	W4	AGP/PCI I/O power 3.3 V
	U6	T9	Y5	
	U9	T12	Y8	
	U14	T14	Y11	
VDDR1	M17	P15	Y15	I/O Power1 (memory) 2.5 V / 3.3 V
	K17	K16	P20	
	H17	G15	J20	
	D16	E12	D15	
	D10			
VDDR2	D7	E10	D4	I/O Power2 (memory/ multimedia GIO) 2.5 V / 3.3 V
	D4	F7	D7	
	G4			
VDDR3	-	J5	N4	I/O Power3 (multimedia GIO) 3.3 V
	-	P6	P4	
AVDD	N4	U4	V4	Analog DAC Power 2.5 V
PVDD	L3	T3	U3	PLL Power 2.5 V

A.2 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number

Pin No	Signal Name	Function	Type
A1	XTALIN	Crystal in	In
A2	Y4	DVS data	Bi
A3	Y7	DVS data	Bi
A4	SSAD7/ LCD19	MPP2 data / LCD interface data	Bi
A5	SSAD4/ LCD16	MPP2 data / LCD interface data	Bi
A6	SSAD0/ LCD12	MPP2 data / LCD interface data	Bi
A7	UV6 / LCD8	MPP2 data / LCD interface data	Bi
A8	UV3 / LCD5	MPP2 data / LCD interface data	Bi
A9	UV0 / LCD2	MPP2 data / LCD interface data	Bi
A10	DQ63	Memory Data	Bi
A11	DQ60	Memory Data	Bi
A12	DQ56	Memory Data	Bi
A13	DQ52	Memory Data	Bi
A14	DQ48	Memory Data	Bi
A15	DQ44	Memory Data	Bi
A16	DQ41	Memory Data	Bi
A17	DQ38	Memory Data	Bi
A18	DQ35	Memory Data	Bi
A19	DQ33	Memory Data	Bi
A20	DQ31	Memory Data	Bi
B1	XTALOUT	Crystal out	Out
B2	Y3	DVS data	Bi
B3	Y6	DVS data	Bi
B4	SSAD6/ LCD18	MPP2 data / LCD interface data	Bi
B5	SSAD3/ LCD15	MPP2 data / LCD interface data	Bi
B6	SAS/ LCD11 / SCL	MPP2 adr. strobe / LCD interface data / I2CCLK	Bi
B7	UV5 / LCD7	DVS2 data / LCD interface data	Bi
B8	UV2 / LCD4	DVS2 data / LCD interface data	Bi
B9	ZVVSYNC / LCD1	Zoom video ctrl / LCD interface data	Bi
B10	DQ62	Memory Data	Bi
B11	DQ59	Memory Data	Bi
B12	DQ55	Memory Data	Bi
B13	DQ51	Memory Data	Bi
B14	DQ47	Memory Data	Bi

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
B15	DQ43	Memory Data	Bi
B16	DQ40	Memory Data	Bi
B17	DQ37	Memory Data	Bi
B18	DQ34	Memory Data	Bi
B19	DQ32	Memory Data	Bi
B20	DQ30	Memory Data	Bi
C1	Y1	DVS data	Bi
C2	Y2	DVS data	Bi
C3	Y5	DVS data	Bi
C4	SSAD5/ LCD17	MPP2 data / LCD interface data	Bi
C5	SSAD2/ LCD14	MPP2 data / LCD interface data	Bi
C6	SDS / LCD10 / SDA	MPP2 data strobe / LCD interface data / I2CDATA	Bi
C7	V4/ LCD6	DVS2 data / LCD interface data	Bi
C8	UV1 / LCD3	DVS2 data / LCD interface data	Bi
C9	ZVHREF/ LCD0	Zoom video ctlr / LCD interface data	Bi
C10	DQ61	Memory Data	Bi
C11	DQ58	Memory Data	Bi
C12	DQ54	Memory Data	Bi
C13	DQ50	Memory Data	Bi
C14	DQ46	Memory Data	Bi
C15	DQ42	Memory Data	Bi
C16	DQ39	Memory Data	Bi
C17	DQ36	Memory Data	Bi
C18	DQ27	Memory Data	Bi
C19	DQ28	Memory Data	Bi
C20	DQ29	Memory Data	Bi
D1	Y0	DVS data	Bi
D2	LCDCLK	LCD interface clock	Bi
D3	ROMCS#	Bios Eprom Chip Select	
D5	SSAD1/ LCD13	MPP2 data / LCD interface data	Bi
D6	UV7 / LCD9	DVS2 data / LCD interface data	Bi
D11	DQ57	Memory Data	Bi
D12	DQ53	Memory Data	Bi
D13	DQ49	Memory Data	Bi
D14	DQ45	Memory Data	Bi
D17	DQ23	Memory Data	Bi

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
D18	DQ24	Memory Data	Bi
D19	DQ25	Memory Data	Bi
D20	DQ26	Memory Data	Bi
E1	PCLK	DVS clock	Bi
E2	SAD/HAD7	MPP/VIP host data	Bi
E3	SAD/HAD6	MPP/VIP host data	Bi
E4	LCDCDE	LCD interface display enable	Bi
E17	DQ19	Memory Data	Bi
E18	DQ20	Memory Data	Bi
E19	DQ21	Memory Data	Bi
E20	DQ22	Memory Data	Bi
F1	SAD/HAD4	MPP/VIP host data	Bi
F2	SAD3	MPP data	Bi
F3	SAD/HAD5	MPP/VIP host data	Bi
F4	GIOCLAMP	5V tolerance clamp	
F17	DQ15	Memory Data	Bi
F18	DQ16	Memory Data	Bi
F19	DQ17	Memory Data	Bi
F20	DQ18	Memory Data	Bi
G1	SAD0	MPP data	Bi
G2	SAD1	MPP data	Bi
G3	SAD2	MPP data	Bi
G17	DQ11	Memory Data	Bi
G18	DQ12	Memory Data	Bi
G19	DQ13	Memory Data	Bi
G20	DQ14	Memory Data	Bi
H1	BYTCLK	MPP (Tvout) byte clock	Bi
H2	DS/VIPCLK	MPP data strobe/ VIP host clock	Bi
H3	SRDY/INT/HAD0	MPP ready / VIP host data bit 0	Bi
H18	DQ8	Memory Data	Bi
H19	DQ9	Memory Data	Bi
H20	DQ10	Memory Data	Bi
J1	AS/HCNTL	MPP address strobe / VIP host control	Bi
J2	SCL/HAD3/ VIPINT	I^2C clock/VIP host data / VIP Interrupt	Bi
J3	SDA/HAD2	I^2C data/VIP host data	Bi
J4	MONID3 / LCD23	Monitor DDC / LCD interface data	Bi

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
J18	DQ5	Memory Data	Bi
J19	DQ6	Memory Data	Bi
J20	DQ7	Memory Data	Bi
K1	MONID0 / LCD20	Monitor DDC / LCD interface data	Bi
K2	MONID1 / LCD21	Monitor DDC / LCD interface data	Bi
K3	MONID2 / LCD22	Monitor DDC / LCD interface data	Bi
K18	DQ2	Memory Data	Bi
K19	DQ3	Memory Data	Bi
K20	DQ4	Memory Data	Bi
L1	R	Red	Out
L2	RSET	DAC current set resistor	In
L18	DQ0	Memory Data	Bi
L19	DQ1	Memory Data	Bi
L20	CAS#	Column Address Strobe	
M1	G	Green	Out
M2	HSYNC	Horizontal Sync	Bi
M3	VSYNC	Vertical Sync	Bi
M18	QS1	Data Strobe (upper 32 bits DDR)	
M19	CLK1#	Memory Clock bar (upper 32 bits DDR)	
M20	CLK1	Memory Clock (upper 32 bits DDR)	
N1	B	Blue	Out
N2	SBA0	Sideband address port for AGP1X/2X	Bi
N3	SBA1	Sideband address port for AGP1X/2X	Bi
N17	VREF	DDR Reference Power supply	Analog
N18	QS0	Data Strobe (lower 32 bits DDR)	
N19	CLK0#	Memory Clock bar	
N20	CLK0	Memory Clock	
P1	SBA4	Sideband address port for AGP1X/2X	Bi
P2	SBA2	Sideband address port for AGP1X/2X	Bi
P3	SBA3	Sideband address port for AGP1X/2X	Bi
P17	DSF		Tristate
P18	DQM#1	Memory data Byte write enable	Tristate
P19	DQM#0	Memory data Byte write enable	Tristate
P20	RAS#	Row Address Strobe	Tristate
R1	SB_STB	Side band strobe for AGP1X/2X	
R2	ST2	AGP status Bus	

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
R3	RBF#	AGP read buffer full	
R17	WE#	Memory write enable	Tristate
R18	DQM#4	Memory data Byte write enable	Tristate
R19	DQM#3	Memory data Byte write enable	Tristate
R20	DQM#2	Memory data Byte write enable	Tristate
T1	ST0	AGP status Bus	
T2	GNT#	PCI BM grant signal from arbiter	
T3	ST1	AGP status Bus	
T18	DQM#7	Memory data Byte write enable	Tristate
T19	DQM#6	Memory data Byte write enable	Tristate
T20	DQM#5	Memory data Byte write enable	Tristate
U1	REQ#	PCI BM request signal to arbiter	
U2	RESET#	Active low PCI reset	
U3	INTA#	Interrupt request line	Tristate
U4	AGPGPIO0/AGP_BUSY#/CLKRUN#	Future AGP4x support / AGP / PCI power management output signal	
U5	AGPGPIO2	Future AGP4x support	
U8	AGPCLAMP	5 V tolerance clamp	
U10	PAR	Parity for AD[31:0] and C/BE#[3:0]	Out
U13	AGPGPIO3	Future AGP4x support	
U15	TESTEN	Test mode	
U16	M66EN/ Biosffclk/ HAD1	clock for add-in card flops on Bios/VIP host data bit 1	
U17	CS3	Chip select	Tristate
U18	A9	Memory Address line	Tristate
U19	A10	Memory Address line	Tristate
U20	A11	Select Bank	Tristate
V1	PCICLK	BUS clock	
V2	AD30	Address/data	Bi
V3	AD26	Address/data	Bi
V4	AGPGPIO1/ STP_AGP#	Future AGP4x support / Power management input from AGP bus	
V5	SBA5	Sideband address port for AGP1X/2X	
V6	SBA7/ IDSEL	Sideband address port for AGP1X/2X / PCI initialization device select	
V7	AD20	Address/data	Bi
V8	AD16	Address/data	Bi
V9	TRDY#	Target device ready	Bi

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
V10	STOP#	Target transaction termination required.	Bi
V11	AD13	Address/data	Bi
V12	AD9	Address/data	Bi
V13	C/BE#0	Bus Command / Byte Enable	Bi
V14	AD6	Address/data	Bi
V15	AD2	Address/data	Bi
V16	AD0	Address/data	Bi
V17	CS2	Chip select	Tristate
V18	A6	Memory Address line	Tristate
V19	A7	Memory Address line	Tristate
V20	A8	Memory Address line	Tristate
W1	AD31	Address/data	Bi
W2	AD28	Address/data	Bi
W3	AD24	Address/data	Bi
W4	C/BE#3	Bus Command / Byte Enable	
W5	AD22	Address/data	Bi
W6	SBA6	Sideband address port for AGP1X/2X	
W7	AD18	Address/data	Bi
W8	AD17	Address/data	Bi
W9	FRAME#	Cycle Frame	Bi
W10	C/BE#1	Bus Command / Byte Enable	Bi
W11	AD15	Address/data	Bi
W12	AD11	Address/data	Bi
W13	AD_STB0	AGP-133 Address strobe	Bi
W14	AD7	Address/data	Bi
W15	AD4	Address/data	Bi
W16	AD1	Address/data	Bi
W17	CS0	Chip select	Tristate
W18	A3	Memory Address line	Tristate
W19	A4	Memory Address line	Tristate
W20	A5	Memory Address line	Tristate
Y1	AD29	Address/data	Bi
Y2	AD27	Address/data	Bi
Y3	AD25	Address/data	Bi
Y4	AD_STB1	AGP-133 Address strobe	
Y5	AD23	Address/data	Bi

Table A-3 272 BGA (RAGE 128 VR) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
Y6	AD21	Address/data	Bi
Y7	AD19	Address/data	Bi
Y8	C/BE#2	Bus Command / Byte Enable	Bi
Y9	IRDY#	Initiator (BM) ready	Bi
Y10	DEVSEL#	Device select	Bi
Y11	AD14	Address/data	Bi
Y12	AD12	Address/data	Bi
Y13	AD10	Address/data	Bi
Y14	AD8	Address/data	Bi
Y15	AD5	Address/data	Bi
Y16	AD3	Address/data	Bi
Y17	CS1	Chip select	Tristate
Y18	A0	Memory Address line	Tristate
Y19	A1	Memory Address line	Tristate
Y20	A2	Memory Address line	Tristate

A.3 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number

Pin No	Signal Name	Function	Type
A1	DQ99	Memory Data	Bi
A2	DQ98	Memory Data	Bi
A3	DQ96	Memory Data	Bi
A4	DQ94/ SSAD6/ LCD18	Memory Data / MPP2 data / LCD interface data	Bi
A5	DQ91/ SSAD3/ LCD15	Memory Data / MPP2 data / LCD interface data	Bi
A6	DQ86 / SDS / LCD10 / SDA	Memory Data / MPP2 data strobe / LCD interface data / I2CDATA	Bi
A7	DQ81	Memory Data	Bi
A8	DQ76 / UV4/ LCD6	Memory Data / DVS2 data / LCD interface data	Bi
A9	DQ72 / UV0 / LCD2	Memory Data / DVS2 data / LCD interface data	Bi
A10	DQ68	Memory Data	Bi
A11	DQ64	Memory Data	Bi
A12	DQM#12	Memory data Byte write enable	Tristate
A13	DQM#8	Memory data Byte write enable	Tristate
A14	DQ59	Memory Data	Bi
A15	DQ54	Memory Data	Bi
A16	DQ49	Memory Data	Bi
A17	DQ44	Memory Data	Bi
A18	DQ41	Memory Data	Bi
A19	DQ39	Memory Data	Bi
A20	DQ37	Memory Data	Bi
B1	DQ100	Memory Data	Bi
B2	DQ97	Memory Data	Bi
B3	DQ95/ SSAD7/ LCD19	Memory Data / MPP2 data / LCD interface data	Bi
B4	DQ93/ SSAD5/ LCD17	Memory Data / MPP2 data / LCD interface data	Bi
B5	DQ90/ SSAD2/ LCD14	Memory Data / MPP2 data / LCD interface data	Bi
B6	DQ85	Memory Data	Bi
B7	DQ80	Memory Data	Bi
B8	DQ75 / UV3 / LCD5	Memory Data / DVS2 data / LCD interface data	Bi
B9	DQ71/ ZVVSYNC / LCD1	Memory Data / Zoom video ctrl / LCD interface data	Bi
B10	DQ67	Memory Data	Bi
B11	DQM#15	Memory data Byte write enable	Tristate
B12	DQM#11	Memory data Byte write enable	Tristate
B13	DQ63	Memory Data	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
B14	DQ58	Memory Data	Bi
B15	DQ53	Memory Data	Bi
B16	DQ48	Memory Data	Bi
B17	DQ43	Memory Data	Bi
B18	DQ40	Memory Data	Bi
B19	DQ38	Memory Data	Bi
B20	DQ36	Memory Data	Bi
C1	DQ103	Memory Data	Bi
C2	DQ102	Memory Data	Bi
C3	DQ101	Memory Data	Bi
C4	DQ92/ SSAD4/ LCD16	Memory Data / MPP2 data / LCD interface data	Bi
C5	DQ89/ SSAD1/ LCD13	Memory Data / MPP2 data / LCD interface data	Bi
C6	DQ84	Memory Data	Bi
C7	DQ79 / UV7 / LCD9	Memory Data / DVS2 data / LCD interface data	Bi
C8	DQ74 / UV2 / LCD4	Memory Data / DVS2 data / LCD interface data	Bi
C9	DQ70 / ZVHREF/ LCD0	Memory Data / Zoom video ctlr / LCD interface data	Bi
C10	DQ66	Memory Data	Bi
C11	DQM#14	Memory data Byte write enable	Tristate
C12	DQM#10	Memory data Byte write enable	Tristate
C13	DQ62	Memory Data	Bi
C14	DQ57	Memory Data	Bi
C15	DQ52	Memory Data	Bi
C16	DQ47	Memory Data	Bi
C17	DQ42	Memory Data	Bi
C18	DQ33	Memory Data	Bi
C19	DQ34	Memory Data	Bi
C20	DQ35	Memory Data	Bi
D1	DQ107	Memory Data	Bi
D2	DQ106	Memory Data	Bi
D3	DQ105	Memory Data	Bi
D4	DQ104	Memory Data	Bi
D5	DQ88/ SSAD0/ LCD12	Memory Data / MPP2 data / LCD interface data	Bi
D6	DQ83	Memory Data	Bi
D7	DQ78 / UV6 / LCD8	Memory Data / DVS2 data / LCD interface data	Bi
D8	DQ73 / UV1 / LCD3	Memory Data / DVS2 data / LCD interface data	Bi
D9	DQ69	Memory Data	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
D10	DQ65	Memory Data	Bi
D11	DQM#13	Memory data Byte write enable	Tristate
D12	DQM#9	Memory data Byte write enable	Tristate
D13	DQ61	Memory Data	Bi
D14	DQ56	Memory Data	Bi
D15	DQ51	Memory Data	Bi
D16	DQ46	Memory Data	Bi
D17	DQ29	Memory Data	Bi
D18	DQ30	Memory Data	Bi
D19	DQ31	Memory Data	Bi
D20	DQ32	Memory Data	Bi
E1	DQ111	Memory Data	Bi
E2	DQ110	Memory Data	Bi
E3	DQ109	Memory Data	Bi
E4	DQ108	Memory Data	Bi
E5	DQ87 / SAS/ LCD11 / SCL	Memory Data / MPP2 adr. strobe / LCD interface data / I2CCLK	Bi
E6	DQ82	Memory Data	Bi
E7	DQ77 / UV5 / LCD7	Memory Data / DVS2 data / LCD interface data	Bi
E13	DQ60	Memory Data	Bi
E14	DQ55	Memory Data	Bi
E15	DQ50	Memory Data	Bi
E16	DQ45	Memory Data	Bi
E17	DQ25	Memory Data	Bi
E18	DQ26	Memory Data	Bi
E19	DQ27	Memory Data	Bi
E20	DQ28	Memory Data	Bi
F1	DQ117	Memory Data	Bi
F2	DQ116	Memory Data	Bi
F3	DQ115	Memory Data	Bi
F4	DQ114	Memory Data	Bi
F5	DQ113	Memory Data	Bi
F6	DQ112	Memory Data	Bi
F16	DQ20	Memory Data	Bi
F17	DQ21	Memory Data	Bi
F18	DQ22	Memory Data	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
F19	DQ23	Memory Data	Bi
F20	DQ24	Memory Data	Bi
G1	DQ122	Memory Data	Bi
G2	DQ121	Memory Data	Bi
G3	DQ120	Memory Data	Bi
G4	DQ119	Memory Data	Bi
G5	DQ118	Memory Data	Bi
G16	DQ15	Memory Data	Bi
G17	DQ16	Memory Data	Bi
G18	DQ17	Memory Data	Bi
G19	DQ18	Memory Data	Bi
G20	DQ19	Memory Data	Bi
H1	DQ127	Memory Data	Bi
H2	DQ126	Memory Data	Bi
H3	DQ125	Memory Data	Bi
H4	DQ124	Memory Data	Bi
H5	DQ123	Memory Data	Bi
H16	DQ10	Memory Data	Bi
H17	DQ11	Memory Data	Bi
H18	DQ12	Memory Data	Bi
H19	DQ13	Memory Data	Bi
H20	DQ14	Memory Data	Bi
J1	Y4	DVS data	Bi
J2	Y5	DVS data	Bi
J3	Y6	DVS data	Bi
J4	Y7	DVS data	Bi
J16	DQ5	Memory Data	Bi
J17	DQ6	Memory Data	Bi
J18	DQ7	Memory Data	Bi
J19	DQ8	Memory Data	Bi
J20	DQ9	Memory Data	Bi
K1	Y0	DVS data	Bi
K2	Y1	DVS data	Bi
K3	Y2	DVS data	Bi
K4	Y3	DVS data	Bi
K5	ROMCS#	Bios Eprom Chip Select	

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
K17	DQ1	Memory Data	Bi
K18	DQ2	Memory Data	Bi
K19	DQ3	Memory Data	Bi
K20	DQ4	Memory Data	Bi
L1	XTALIN	Crystal in	In
L2	XTALOUT	Crystal out	Out
L3	PCLK	DVS clock	Bi
L4	LCDCLK	LCD interface clock	Bi
L5	LCDCDE	LCD interface Display enable	Bi
L17	DQ0	Memory Data	Bi
L18	QS0	Data Strobe (lower 32 bits DDR)	
L19	QS1	Data Strobe (upper 32 bits DDR)	
L20	CAS#	Column Address Strobe	
M1	SAD/HAD4	MPP/VIP host data	Bi
M2	SAD/HAD5	MPP/VIP host data	Bi
M3	SAD/HAD6	MPP/VIP host data	Bi
M4	SAD/HAD7	MPP/VIP host data	Bi
M5	GIOCLAMP	5V tolerance clamp	
M16	VREF	DDR Reference Power supply	Analog
M17	DQM#1	Memory data Byte write enable	Tristate
M18	DQM#0	Memory data Byte write enable	Tristate
M19	CLK1#	Memory Clock bar (upper 32 bits DDR)	
M20	CLK1	Memory Clock (upper 32 bits DDR)	
N1	BYTCLK	MPP (Tvout) byte clock	Bi
N2	SAD0	MPP data	Bi
N3	SAD1	MPP data	Bi
N4	SAD2	MPP data	Bi
N5	SAD3	MPP data	Bi
N16	DQM#3	Memory data Byte write enable	Tristate
N17	DQM#2	Memory data Byte write enable	Tristate
N18	DSF		Tristate
N19	CLK0#	Memory Clock bar	
N20	CLK0	Memory Clock	
P1	DS/VIPCLK	MPP data strobe/ VIP host clock	Bi
P2	AS/HCNTL	MPP address strobe / VIP host control	Bi
P3	SRDY/INT/HAD0	MPP ready / VIP host data bit 0	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
P4	MONID2	Monitor DDC	Bi
P5	MONID3	Monitor DDC	Bi
P16	DQM#6	Memory data Byte write enable	Tristate
P17	DQM#5	Memory data Byte write enable	Tristate
P18	WE#	Memory write enable	Tristate
P19	DQM#4	Memory data Byte write enable	Tristate
P20	RAS#	Row Address Strobe	Tristate
R1	SCL/HAD3/ VIPINT	I^2C clock/VIP host data / VIP Interrupt	Bi
R2	SDA/HAD2	I^2C data/VIP host data	Bi
R3	MONID0	Monitor DDC	Bi
R4	MONID1	Monitor DDC	Bi
R16	DQM#7	Memory data Byte write enable	Tristate
R17	A8	Memory Address line	Tristate
R18	A9	Memory Address line	Tristate
R19	A10	Memory Address line	Tristate
R20	A11	Select Bank	Tristate
T1	R	Red	Out
T2	RSET	DAC current set resistor	In
T5	AGPGPIO0/AGP_BUSY# / CLKRUN#	Future AGP4x support / AGP / PCI power management output signal	
T6	AD28	Address/data	Bi
T11	AGPCLAMP	5 V tolerance clamp	
T17	A4	Memory Address line	Tristate
T18	A5	Memory Address line	Tristate
T19	A6	Memory Address line	Tristate
T20	A7	Memory Address line	Tristate
U1	G	Green	Out
U2	HSYNC	Horizontal Sync	Bi
U5	INTA#	Interrupt request line	Tristate
U6	AD30	Address/data	Bi
U7	AD26	Address/data	Bi
U8	A1	Memory Address line	Tristate
U8	AGPGPIO2	Future AGP4x support	
U9	SBA5	Sideband address port for AGP1X/2X	
U10	AD22	Address/data	Bi
U11	AD16	Address/data	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
U12	TRDY#	Target device ready	Bi
U13	AD15	Address/data	Bi
U14	AD11	Address/data	Bi
U15	AD9	Address/data	Bi
U16	AGPGPIO3	Future AGP4x support	
U17	A0	Memory Address line	Tristate
U19	A2	Memory Address line	Tristate
U20	A3	Memory Address line	Tristate
V1	B	Blue	Out
V2	VSYNC	Vertical Sync	Bi
V3	SBA1	Sideband address port for AGP1X/2X	Bi
V4	ST1	AGP status Bus	
V5	GNT#	PCI BM grant signal from arbiter	
V6	AD29	Address/data	Bi
V7	AD24	Address/data	Bi
V8	AGPGPIO1/ STP_AGP#	Future AGP4x support / Power management input from AGP bus	
V9	SBA7/ IDSEL	Sideband address port for AGP1X/2X / PCI initialization device select	
V10	AD20	Address/data	Bi
V11	AD18	Address/data	Bi
V12	FRAME#	Cycle Frame	Bi
V13	PAR	Parity for AD[31:0] and C/BE#[3:0]	Out
V14	AD13	Address/data	Bi
V15	C/BE#0	Bus Command / Byte Enable	Bi
V16	TESTEN	Test mode	
V17	M66EN/ Biosffclk/ HAD1	Clock for add-in card flops on Bios/VIP host data bit 1	
V18	CS0	Chip select	Tristate
V19	CS1	Chip select	Tristate
V20	CS2	Chip select	Tristate
W1	SBA0	Sideband address port for AGP1X/2X	Bi
W2	SBA3	Sideband address port for AGP1X/2X	Bi
W3	RBF#	AGP read buffer full	
W4	ST2	AGP status Bus	
W5	REQ#	PCI BM request signal to arbiter	
W6	AD31	Address/data	Bi
W7	AD27	Address/data	Bi

Table A-4 328 BGA (RAGE 128 GL) Pins Sorted by Pin Number (Continued)

Pin No	Signal Name	Function	Type
W8	C/BE#3	Bus Command / Byte Enable	
W9	SBA6	Sideband address port for AGP1X/2X	
W10	AD21	Address/data	Bi
W11	C/BE#2	Bus Command / Byte Enable	Bi
W12	DEVSEL#	Device select	Bi
W13	STOP#	Target transaction termination required.	Bi
W14	AD12	Address/data	Bi
W15	AD_STB0	AGP-133 Address strobe	Bi
W16	AD6	Address/data	Bi
W17	AD4	Address/data	Bi
W18	AD2	Address/data	Bi
W19	AD0	Address/data	Bi
W20	CS3	Chip select	Tristate
Y1	SBA2	Sideband address port for AGP1X/2X	Bi
Y2	SBA4	Sideband address port for AGP1X/2X	Bi
Y3	SB_STB	Side band strobe for AGP1X/2X	
Y4	ST0	AGP status Bus	
Y5	RESET#	Active low PCI reset	
Y6	PCICLK	BUS clock	
Y7	AD25	Address/data	Bi
Y8	AD_STB1	AGP-133 Address strobe	
Y9	AD23	Address/data	Bi
Y10	AD19	Address/data	Bi
Y11	AD17	Address/data	Bi
Y12	IRDY#	Initiator (BM) ready	Bi
Y13	C/BE#1	Bus Command / Byte Enable	Bi
Y14	AD14	Address/data	Bi
Y15	AD10	Address/data	Bi
Y16	AD8	Address/data	Bi
Y17	AD7	Address/data	Bi
Y18	AD5	Address/data	Bi
Y19	AD3	Address/data	Bi
Y20	AD1	Address/data	Bi

A.4 329 BGA Pins Sorted by Pin Number

This list does not show the power pins.

Table A-5 329 BGA Pins Sorted by Pin Number

Pin Number	Signal Name	Description	Type
A1	N/C		
A2	N/C		
A3	N/C		
A4	N/C		
A5	N/C		
A6	N/C		
A7	N/C		
A8	DQ63	Memory Data	Bi-directional
A9	DQ62	Memory Data	Bi-directional
A10	DQ59	Memory Data	Bi-directional
A11	DQ56	Memory Data	Bi-directional
A12	DQ53	Memory Data	Bi-directional
A13	DQ50	Memory Data	Bi-directional
A14	DQ47	Memory Data	Bi-directional
A15	DQ44	Memory Data	Bi-directional
A17	DQ38	Memory Data	Bi-directional
A18	DQ34	Memory Data	Bi-directional
A19	DQ31	Memory Data	Bi-directional
A20	DQ28	Memory Data	Bi-directional
A21	DQ25	Memory Data	Bi-directional
A22	DQ23	Memory Data	Bi-directional
A23	DQ22	Memory Data	Bi-directional
AA1	SBA6	Sideband Address Port for AGP1X/2X	
AA2	SBA7 IDSEL	Sideband Address Port for AGP1X/2X Pci initialization device select	
AA3	SBA5	Sideband Address Port for AGP1X/2X	
AA4	N/C		
AA5	AGPTEST		
AA6	AGPREF		
AA7	AD30	Address/Data	Bi-directional
AA8	AD26	Address/Data	Bi-directional
AA9	C/BE#3	Bus command / byte enable	

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
AA10	SERR		
AA11	AD22	Address/Data	Bi-directional
AA12	AD18	Address/Data	Bi-directional
AA13	AD16	Address/Data	Bi-directional
AA14	TRDY#	Target device ready	Bi-directional
AA15	PAR	Parity for ad[31:0] and c/beb[3:0]	Out
AA16	AD13	Address/Data	Bi-directional
AA17	AD9	Address/Data	Bi-directional
AA18	C/BE#0	Bus command / byte enable	Bi-directional
AA19	N/C		
AA20	M66EN BIOSFFCLK HAD1 AMCGIO11	Clock for add-in card flops on bios VIP host Data bit 1	
AA21	CS1	Chip select	Tristate
AA22	CS2	Chip select	Tristate
AB1	ST2	Agp status bus	
AB2	ST1	Agp status bus	
AB3	REQ#	Pci bm request signal to arbiter	
AB4	GNT#	Pci bm grant signal from arbiter	
AB5	INTA#	Interrupt request line	
AB6	RESET#	Active low pci reset	
AB7	AD28	Address/Data	Bi-directional
AB8	AD25	Address/Data	Bi-directional
AB9	AD24	Address/Data	Bi-directional
AB10	N/C		
AB11	AD20	Address/Data	Bi-directional
AB12	AD17	Address/Data	Bi-directional
AB13	IRDY#	Initiator (bm) ready	Bi-directional
AB14	FRAME#	Cycle frame	Bi-directional
AB15	STOP#	Target transaction termination request	Bi-directional
AB16	AD15	Address/Data	Bi-directional
AB17	AD11	Address/Data	Bi-directional
AB18	AD10	Address/Data	Bi-directional
AB19	AD6	Address/Data	Bi-directional
AB20	AD4	Address/Data	Bi-directional
AB21	AD2	Address/Data	Bi-directional

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
AB22	AD0	Address/Data	Bi-directional
AB23	CS3	Chip select	Tristate
AC1	RBF#	Agp read buffer full	
AC2	ST0	Agp status bus	
AC3	SB_STB	Sideband strobe for AGP1X/2X	
AC4	PCICLK	Bus clock	
AC5	AD31	Address/Data	Bi-directional
AC6	N/C		
AC7	AD29	Address/Data	Bi-directional
AC8	AD27	Address/Data	Bi-directional
AC9	AD_STB1	AGP-133 Address strobe	
AC10	AD23	Address/Data	Bi-directional
AC11	AD21	Address/Data	Bi-directional
AC12	AD19	Address/Data	Bi-directional
AC13	C/BE#2	Bus command / byte enable	Bi-directional
AC14	DEVSEL#	Device select	Bi-directional
AC15	C/BE#1	Bus command / byte enable	Bi-directional
AC16	AD14	Address/Data	Bi-directional
AC17	AD12	Address/Data	Bi-directional
AC18	AD_STB0	AGP-133 Address strobe	Bi-directional
AC19	AD8	Address/Data	Bi-directional
AC20	AD7	Address/Data	Bi-directional
AC21	AD5	Address/Data	Bi-directional
AC22	AD3	Address/Data	Bi-directional
AC23	AD1	Address/Data	Bi-directional
B1	N/C		
B2	N/C		
B3	N/C		
B4	N/C		
B5	N/C		
B6	N/C		
B7	N/C		
B8	N/C		
B9	DQ61	Memory Data	Bi-directional
B10	DQ58	Memory Data	Bi-directional
B11	DQ55	Memory Data	Bi-directional

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
B12	DQ52	Memory Data	Bi-directional
B13	DQ49	Memory Data	Bi-directional
B14	DQ46	Memory Data	Bi-directional
B15	DQ43	Memory Data	Bi-directional
B16	DQ41	Memory Data	Bi-directional
B17	DQ37	Memory Data	Bi-directional
B18	DQ33	Memory Data	Bi-directional
B19	DQ30	Memory Data	Bi-directional
B20	DQ27	Memory Data	Bi-directional
B21	DQ24	Memory Data	Bi-directional
B22	DQ20	Memory Data	Bi-directional
B23	DQ21	Memory Data	Bi-directional
C1	N/C		
C2	N/C		
C3	N/C		
C4	N/C		
C5	N/C		
C6	N/C		
C7	N/C		
C8	N/C		
C9	DQ60	Memory Data	Bi-directional
C10	DQ57	Memory Data	Bi-directional
C11	DQ54	Memory Data	Bi-directional
C12	DQ51	Memory Data	Bi-directional
C13	DQ48	Memory Data	Bi-directional
C14	DQ45	Memory Data	Bi-directional
C15	DQ42	Memory Data	Bi-directional
C16	DQ40	Memory Data	Bi-directional
C17	DQ36	Memory Data	Bi-directional
C18	DQ32	Memory Data	Bi-directional
C19	DQ29	Memory Data	Bi-directional
C20	DQ26	Memory Data	Bi-directional
C21	DQ17	Memory Data	Bi-directional
C22	DQ18	Memory Data	Bi-directional
C23	DQ19	Memory Data	Bi-directional
D1	N/C		

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
D2	N/C		
D3	N/C		
D16	DQ39	Memory Data	Bi-directional
D17	DQ35	Memory Data	Bi-directional
D21	DQ14	Memory Data	Bi-directional
D22	DQ15	Memory Data	Bi-directional
D23	DQ16	Memory Data	Bi-directional
E1	N/C		
E2	N/C		
E3	N/C		
E4	N/C		
E21	DQ11	Memory Data	Bi-directional
E22	DQ12	Memory Data	Bi-directional
E23	DQ13	Memory Data	Bi-directional
F1	Y6	DVS Data	Bi-directional
F2	Y7	DVS Data	Bi-directional
F3	N/C		
F4	N/C		
F20	DQ7	Memory Data	Bi-directional
F21	DQ8	Memory Data	Bi-directional
F21	DQ8	Memory Data	Bi-directional
F22	DQ9	Memory Data	Bi-directional
F23	DQ10	Memory Data	Bi-directional
G1	Y3	DVS Data	Bi-directional
G2	Y4	DVS Data	Bi-directional
G3	Y5	DVS Data	Bi-directional
G20	DQ4	Memory Data	Bi-directional
G21	DQ5	Memory Data	Bi-directional
G22	DQ6	Memory Data	Bi-directional
H1	XTALOUT	Crystal out	Out
H2	XTALIN	Crystal in	In
H3	Y2	DVS Data	Bi-directional
H4	N/C		
H21	DQ1	Memory Data	Bi-directional
H22	DQ2	Memory Data	Bi-directional
H23	DQ3	Memory Data	Bi-directional

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
J1	PCLK	DVS clock	Bi-directional
J2	Y0	DVS Data	Bi-directional
J3	Y1	DVS Data	Bi-directional
J4	ROMCS#	Bios eprom chip select	
J21	QS1	Data strobe (upper 32 bits ddr)	
J22	DQ0	Memory Data	Bi-directional
J23	CAS#	Column Address strobe	
K1	HAD5 SAD5	VIP host Data MPP host Data	Bi-directional
K2	SAD6 HAD6	MPP host Data VIP host Data	Bi-directional
K3	SAD7 HAD7	MPP host Data VIP host Data	Bi-directional
K4	GIOCLAMP	5v tolerance clamp	
K21	QS0	Data strobe (lower 32 bits ddr)	
L1	SAD2	MPP Data	Bi-directional
L2	SAD3	MPP Data	Bi-directional
L3	SAD4 HAD4	MPP host Data VIP host Data	Bi-directional
L4	N/C		
L21	VREF	DDR reference Power supply	Analog
L22	CLK1#	Memory clock bar (upper 32 bits ddr)	
L23	CLK1	Memory clock (upper 32 bits ddr)	
M1	BYTCLK	MPP (tvout) byte clock	Bi-directional
M2	SAD0	MPP Data	Bi-directional
M3	SAD1	MPP Data	Bi-directional
M21	DQM#0	Memory Data byte write enable	Tristate
M22	CLK0#	Memory clock bar	
M23	CLK0	Memory clock	
N1	HAD0 SRDY INT	MPP ready VIP host Data bit 0	Bi-directional
N2	HCNTL AS	VIP host control MPP Address strobe	Bi-directional
N3	DS VIPCLK	MPP Data strobe VIP host clock	Bi-directional
N21	DSF		TRISTATE
N22	DQM#1	Memory Data byte write enable	Tristate

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
N23	RAS#	Row Address strobe	Tritate
P1	MONID3	Monitor ddc	Bi-directional
P2	VIPINT SCL HAD3	VIP interrupt I2c clock VIP host Data	Bi-directional
P3	SDA2 HAD2	I2c Data VIP host Data	Bi-directional
P21	DQM#3	Memory Data byte write enable	Tristate
P22	DQM#2	Memory Data byte write enable	Tristate
R1	MONID0	Monitor ddc	Bi-directional
R2	MONID1	Monitor ddc	Bi-directional
R3	MONID2	Monitor ddc	Bi-directional
R21	DQM#5	Memory Data byte write enable	Tristate
R22	WE#	Memory write enable	Tristate
R23	DQM#4	Memory Data byte write enable	Tristate
T1	R	Red	Out
T2	RSET	Dac current set resistor	In
T21	A11	Select bank	Tristate
T22	DQM#7	Memory Data byte write enable	Tristate
T23	DQM#6	Memory Data byte write enable	Tristate
U1	G	Green	Out
U2	HSYNC	Horizontal sync	Bi-directional
U21	A8	Memory Address line	Tristate
U22	A9	Memory Address line	Tristate
U23	A10	Memory Address line	Tristate
V1	B	Blue	Out
V2	VSYNC	Vertical sync	Bi-directional
V3	LHSYNC	LCD panel horizontal sync	Bi-directional
V21	A5	Memory Address line	Tristate
V22	A6	Memory Address line	Tristate
V23	A7	Memory Address line	Tristate
W1	SBA0	Sideband Address Port for AGP1X/2X	Bi-directional
W2	SBA1	Sideband Address Port for AGP1X/2X	Bi-directional
W3	LVSYNC	LCD panel vertical sync	Bi-directional
W21	A2	Memory Address line	Tristate
W22	A3	Memory Address line	Tristate
W23	A4	Memory Address line	Tristate

Table A-5 329 BGA Pins Sorted by Pin Number (Continued)

Pin Number	Signal Name	Description	Type
Y1	SBA4	Sideband Address Port for AGP1X/2X	Bi-directional
Y2	SBA2	Sideband Address Port for AGP1X/2X	Bi-directional
Y3	SBA3	Sideband Address Port for AGP1X/2X	Bi-directional
Y16	TESTEN	Test mode	
Y21	CS0	Chip select	Tristate
Y22	A0	Memory Address line	Tristate
Y23	A1	Memory Address line	Tristate

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Appendix B
Chip ID Registers

B.1 Legacy ASIC and Chip Identification

Two read-only register fields, ASIC_ID and CHIP_ID, are used to uniquely identify each ASIC type/variant in the VT/GT/RAGE families.

B.1.1 ASIC ID

The ASIC_ID (also known as the REV_ID) is an 8-bit register consisting of three fields — Major Revision ID, Foundry ID, and Minor Revision ID.

B.1.2 Chip ID

The **CHIP_ID** (also known as the **DEVICE_ID**) is represented by a double ASCII character that uniquely identifies the ASIC. For example, the CHIP_ID of the GT-B is “GT”, or 0x4754.

Table B-1 CHIP ASCII Character ID

Chip Name	CHIP_ID (device-id)	Description
VT-A	VT	
VT-B	VT	
GT-B	GT	
RAGE II+	GU /GT	
	VU /VT	
RAGE IIC	GV	PQFP package, PCI 33 MHz
	GZ	PQFP package, PCI 66 MHz
	GW	BGA package, PCI 66 MHz
	GY	BGA package, PCI-33 MHz
	VV	PQFP package, PCI 33 MHz, driver disables 3D functionality

Table B-1 CHIP ASCII Character ID (Continued)

Chip Name	CHIP_ID (device-id)	Description
RAGE PRO	GB	BGA package, AGP: both 1X and 2X
	GD	BGA package, AGP: 1X support only
	GI	BGA package, PCI 33 MHz only
	GP	PQFP, PCI 33 MHz, driver utilizes full 3D functionality
	GQ	PQFP, PCI 33 MHz, driver disables some 3D functionality

B.2 RAGE 128 Chip and Revision Identification

B.2.1 Chip ID

The RAGE 128 ASCII chip ids are as follows:

Table B-2 RAGE 128 CHIP ID's

CHIP_ID	Description
RE (5245h)	RAGE 128 GL, 328 BGA, PCI
RF (5246h)	RAGE 128 GL, 328 BGA, AGP
RK (524Bh)	RAGE 128 VR, 272 BGA, PCI
RL (524Ch)	RAGE 128 VR, 272 BGA, AGP

B.2.2 New Revision ID Register

Prior to RAGE 128 VR/GL, the CHIP_ID and ASIC_ID (REV ID) of a chip was obtained through the PCI_POS registers in PCI configuration space, or through the CONFIG_CHIP_ID register. Starting with RAGE 128, however, a new register, REVISION_ID, will be used to provide the chip/revision information (see *RAGE 128 Register Reference Guide* for full description):

Table B-3 REVISION ID Register

REVISION_ID [R] (CFG:0 0_08, MM:0 0xF08)			
Field Name	**Bits**	**Default**	**Description**
MINOR_REV_ID	3:0	0x0	Minor ASIC revision number
MAJOR_REV_ID	7:4	0x0	Major ASIC revision number

Appendix C
Detailed Pinout Descriptions

C.1 Detailed Pinout Descriptions

Table C-1

Interface	Signal Name	I/O	Function
Host PCI/AGP 66 pins	RESET#	I	Active Low PCI Reset, used to initialize the chip to a known state. All PCI signals on the RAGE 128 will be tristated during its assertion. This signal may be asserted or deasserted asynchronously to the PCICLK, but it must be guaranteed to be clean and have bounce-free edges.
	PCICLK	I	Bus Clock, this signal is used as a reference for all transactions on the PCI bus. Except for RESET# and INTA#, all PCI signals are sampled on the rising edge of this clock signal and all timing parameters are defined with respect to this rising edge. Its frequency can be 33 - 66 - 133 MHz depending on the system bus type (PCI 33 - PCI 66 / AGP1x - AGP2x)
	AD(31:0)	I/O	Multiplexed Address/Data (31:0) A bus cycle consists of an address phase followed by one or more data phases. **PCI:** When the RAGE 128 is a target on the PCI bus, these signals are inputs for address read/writes and write data, and outputs for read data. This bus contains the address during the clock cycle in which FRAME# is asserted (address phase), and it contains the data in the subsequent clock cycles. **AGP:** The RAGE 128 acts as an AGP master. Data is driven or received through the AD lines by the RAGE 128 after appropriate commands are sent to the host-to-PCI bridge via the side band address bus (SBA(7:0)). Note: In AGP mode, AD16 or AD17 (depending on the IDSEL# strap setting) are also used for the IDSEL function.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Host PCI/AGP 66 pins	C/BE#(3:0)	I/O	Multiplexed Bus Command/ Byte Enable(3:0) **PCI:** During the address phase of a transaction, these signals define the bus command (Int ack., spec. cycle, IO R/W, Mem R/W, Config R/W, etc.). During the data phase, they are used as Byte Enables (determine which byte on the AD line carries meaningful data). **AGP:** Provide valid byte information during AGP write transactions and are driven by the master. They are driven to '0000' by the target and ignored by the master (RAGE 128) during the return of AGP read data.
	FRAME#	I/O	Cycle Frame **PCI:** This signal is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate the beginning of a bus transaction. Data transfer will continue while this signal is asserted. When FRAME# is deasserted, the transaction is in its final data phase. **AGP:** Not used in AGP and kept in its deasserted state
	IRDY#	I/O	Initiator (bus master) ready **PCI:** It indicates the ability of the current initiator (current bus master) to complete the current data phase of the transaction. During a write cycle, IRDY# indicates that valid data is present on the AD line. During a read cycle, it indicates that the master is ready to accept data. IRDY# is used in conjunction with the TRDY# signal. Wait cycles are inserted until both IRDY# and TRDY# are asserted. A data phase is completed on any clock where both IRDY# and TRDY# are sampled as asserted. **AGP:** For AGP writes, it indicates that the master is ready to provide all write data for the current write transaction. Once this signal is asserted for a write operation, the master is not allowed to insert wait states. For AGP reads, the assertion of this signal indicates that the master is ready to accept a subsequent block (32 bytes) of read data. The master is never allowed to insert a wait state during the initial block of a read transaction, but it may do so after subsequent block transfers (there is no FRAME# -- IRDY# relationship for AGP transactions). The target is allowed to insert wait states on block boundaries but not on individual data phases (for both Read and Write operations).

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Host PCI/AGP 66 pins	TRDY#	I/O	Target device (slave) ready **PCI:** It indicates the ability of the target to complete the current data phase of the transaction. During a read cycle, TRDY# indicates that valid data is present on the AD line. During a write cycle, it indicates that the target is ready to accept data. TRDY# is used in conjunction with IRDY#. Wait cycles are inserted until both IRDY# and TRDY# are asserted. A data phase is completed on any clock where both IRDY# and TRDY# are sampled as asserted. **AGP:** For AGP reads, it indicates that the target is ready to provide read data for the entire transaction (when transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions.
	DEVSEL#	I/O	Device select **PCI:** When actively driven, it indicates that the driving device (target) has decoded its address as the target of the current access. As an input to other devices and the current master, it indicates whether any device on the bus has been selected. **AGP:** Not used in AGP and kept in its deasserted state.
	STOPb	I/O	Target transaction termination request **PCI:** It indicates that the current target is requesting the master to stop the current transaction. **AGP:** Not used in AGP and kept in its deasserted state.
	PAR	O	Parity bit for AD(31:0) and C/BE#(3:0) **PCI:** Parity is even across the AD and C/BEb lines. It means that PAR = 1 when the count of the number of ‘1s’ on the AD, C/BE# and PAR line is even. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. PAR has the same timing as the AD line but delayed by one clock. The master drives PAR for address and write data phases and the target drives PAR for read data phases. **AGP:** Not used in AGP but must be actively driven by the current owner of the AD bus.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Host PCI/AGP 66 pins	INTA#	O	Interrupt request line **PCI and AGP:** Used to request an interrupt. It's a shareable, level sensitive, active low signal. INTA# is for a single function device.
	REQ#	O	PCI/AGP Bus Master Request signal to arbiter **PCI and AGP:** This signal indicates to the arbiter that this agent desires the use of the bus. This is a point to point signal (i.e., each master has its own REQ# line).
	GNT#	I	PCI/AGP Bus Master Grant signal from arbiter **PCI:** This signal indicates to the agent that access to the bus has been granted by the arbiter. This is a point to point signal (i.e. each master has its own REQ# line). **AGP:** Same as PCI but used in combination with the ST signals. The additional information provided by the ST lines indicates whether the master is the recipient of previously requested read data (high or low priority), or whether it is to provide write data (high or low priority) for a previously enqueued write command, or whether it has been given permission to start a bus transaction (AGP or PCI).
	ST(2:0)	I	AGP Status bus **AGP:** These signals provide information from the arbiter to the master on what it may do. The ST lines have meaning to the master only when that master's GNT# is asserted. When GNT# is not asserted, these signals have no meaning and must be ignored.
	SBA7/IDSEL	I/O	AGP Sideband Address port bit 7 **or** PCI Initialization device select (in PCI mode) **PCI:** It is used as a chip select during configuration read and write cycles. **AGP:** AGP sideband address port bit 7.
	SBA(6:0)	O	Sideband Address port for AGP1X/2X support **AGP:** It is an additional bus used to pass requests (address and command) to the target from the master. Note: the RAGE 128 does not use the PIPE# mechanism to enqueue requests, it uses the SBA lines to enqueue requests to the arbiter.
	RBF#	O	AGP Read buffer full **AGP:** This signal indicates whether the master is ready to accept previously requested low priority read data or not. When asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Host PCI/AGP 66 pins	AD_STB(1:0)	I/O	AGP-133 Address strobe **AGP:** AD_STB0 and AD_STB1 provide timing for AGP2x data transfer mode on respectively AD(15:0) and AD(31:16). The agent that is providing data drives this signal.
	SB_STB	O	Sideband Strobe for AGP1X/2X support **AGP:** This signal provides timing for the SBA lines (when supported) and is always driven by the master.When the side band strobe has been idle, a sync cycle needs to be performed before a request can be enqueued.
	AGP_BUSY#/ CLKRUN# AGPIO(0)	I/O	Power management output signal for AGP/PCI bus Future AGP4x support.
	STP_AGP# AGPIO(1)	I/O	Power management input signal for AGP bus Future AGP4x support.
	AGPIO(3:2)	I/O	Future AGP4x support.
Memory SGRAM/ SGRAM DDR/ SDRAM 99 pins(64 bits) or 171 pins(128 bits)	DQ(63:0)	I/O	Memory data bus Supports SSTL2 and SSTL3 (DDR), and LVTTL (SDR) memory interface (internally pulled low in LVTTL mode when tristated).
	DQ(127:64)	I/O	Memory data bus (internally pulled low in LVTTL mode when tristated). Supports LVTTL (SDR) memory interface. Has multiplexed multimedia functionality (on DQ(79:70) and DQ(95:86)).
	DQM#(7:0)	O	Memory data byte enables for write cycles (lower 64 bits)
	DQM#(15:8)	O	Memory data byte enables for write cycles (upper 64 bits)
	A(11:0)	O	Memory address bus Provide multiplexed row and column addresses to the DRAMs.
	CS(3:0)	O	Chip selects
	QS(1:0)	I	Read strobes
	RAS#	O	Row address select
	CAS#	O	Column address select
	WE#	O	Write enable
	DSF	O	DSF Special function control bit for SGRAM. If high, it enables the SGRAM's "block-write" capability. If low, it disables "block-write" (functionality equivalent to SDRAM's).
	CLK0	I/O	Memory clock 0
	CLK0#	I/O	Memory clock 0 bar Differential clock used in DDR mode.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Memory (continued)	CLK1	I/O	Memory clock 1
	CLK1#	I/O	Memory clock 1 bar Differential clock used in DDR mode.
	VREF	I	Reference voltage for DDR (0.55xVDD for SSTL2, or 0.45xVDD for SSTL3) Note: if the differential signaling interface is not used, this pin must be connected to the memory I/Os VDDR (3.3 V or 2.5 V)
ROM 1 pin	ROMCS#	O	BIOS ROM Chip Select, used to enable the ROM for ROM Read and Write (if Flash ROM) operations.
AMC (MPP1, DVS,VIP, I^2C) 20+10 pins (muxed)	SAD(3:0) [AMCGIO(3:0)]	I/O	Address/data for MPP bits (3:0) **MPP:** MPP data bit (3:0) Pixel Data transfer and register reads and writes may occur using the MPP data lines. Reads and writes may be to any of the MPP peripheral device (ImpacTV, MPEG decoder, Rage Theater, etc.) registers.
	SAD(7:4) / HAD(7:4) [AMCGIO(7:4)]	I/O	Address/data for MPP **or** VIP host data bit (7:4) **MPP:** MPP data bit (7:4). **VIP:** Host VIP data bit (7:4), for future expansion from the initial 2 bit host VIP port to an 8 bit port.
	DS / VIPCLK [AMCGIO(8)]	I/O	MPP data strobe **or** VIP host clock **MPP:** This strobe is driven by RAGE 128 and indicates to the targeted MPP device that data is on the MPPData lines. On the rising edge of this signal, the data will be latched. This signal requires and on-board pull-up resistor. **VIP:** VIP host clock (25 - 33 MHz), driven by the RAGE 128 (VIP master) and used to synchronize operations on the VIP host bus.
	AS / HCNTL [AMCGIO(9)]	I/O	MPP address strobe **or** VIP host control **MPP:** This strobe is driven by RAGE 128 and indicates to the targeted MPP device that an address is on the MPP Data lines. On the falling edge of this signal, the address will be latched. This signal requires and on board pull-up resistor. **VIP:** Shared control pin. It is driven by the master to initiate and terminate data transfers; and it is driven by the slave to terminate and add wait states to data transfers.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
AMC (MPP1, DVS,VIP, I^2C) 20+10 pins (muxed)	SRDY/ IRQ / HAD(0) [AMCGIO(10)]	I/O	MPP ready/interrupt **or** VIP host data bit 0 **MPP:** During MPP cycles, this signal is driven by the MPP target and used for handshaking (Wait/Request) with the MPP master (RAGE 128). When there is no MPP cycle occurring, this signal can be used as an interrupt (active low) by the MPP targets. (Note: ImpacTV does not use this signal.) This signal requires and on-board pull-up resistor (even if not used). **VIP:** Host address data bus (bit 0), part of the basic two bit host VIP data bus, used to transfer commands, addresses and data between master (RAGE 128) and slave devices (RAGE THEATER, MPEG decoder, etc.).
	M66EN / Biosffclk / HAD(1) [AMCGIO(11)]	I/O	Clock for eprom flops / VIP host data bit 1 **BIOS:** On an add-in card implementation, during the initial BIOS read cycles which occur just after reset, this signal is used as the clock signal for the on board quadflops between the RAGE 128 and the on board BIOS. After the BIOS read cycles are completed, this pin will resume its operation as a VIP data bit if necessary. **VIP:** Host address data bus (bit 1).
	PDATA(7:0) [AMCGIO(19:12)]	I	DVS/ITU656/ZV data in Video Capture data input port, supports BT byte stream, CCIR/ITU656, VIP1.1, VIP2.0 (16 bits), and Zoom Video formats. These signals are internally pulled down by default in order to stop them from floating in cases where they are not driven by external signals.
	PCLK [AMCGIO(20)]	I	DVS/ITU656/ZV clock in Video Capture pixel clock input port. This signal is internally pulled down by default in order to stop it from floating in cases where it is not driven by an external signal
	UV(7:0)/LCD(9:2) [MDGIO(15:8)]	I	Extended VIP/DVS port/ZV data in **or** future LCD interface Second Video Capture port, multiplexed on the upper bits of the memory data line DQ(79:72). It can be used as a second 8 bit DVS video in port or combined with the main DVS port to provide support for 16 bit DVS and Zoom Video.
	ZVHREF/LCD(0)/ PCLK_1 [MDGIO(6)]	I	ZV control port **or** future LCD interface
	ZVVSYNC/LCD(1) [MDGIO(7)]	I	ZV control port **or** future LCD interface

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
AMC (MPP1, DVS,VIP, I^2C) 20+10 pins (muxed)	BYTCLK [AMCGIO(21)]	I/O	Bytclk “to” or “from” (“to” if in Genlock mode) ImpacTV/RAGE THEATER, used on MPP1 or MPP2 **MPP:** The PLL in the ImpacTV/RAGE THEATER chip derives a very accurate 3 or 2 times pixel clock for the RAGE 128. By using this clock, the RAGE 128 display frame rate can stay in sync with the TV display, and simultaneous CRT and TV display is possible. In Genlock mode, the clock will be provided by the RAGE 128 to the ImpacTV/RAGE THEATER chips in order to provide full synchronization and prevent any potential frame loss in video playback
	SDA / HAD(2) [AMCGIO(22)]	I/O	I^2C data in/out / VIP host data bit 2 **I2C:** Serial I^2C data line. This signal requires an on-board pull-up resistor. **VIP:** Host VIP data bit 2, for future expansion from the initial 2 bit host VIP port to an 4 or 8 bit port.
	SCL / HAD(3) / VIPINT [AMCGIO(23)]	O	I^2C clock out / VIP host data bit 3 or VIP Interrupt **I2C:** Serial I^2C Clock line This signal requires an on-board pull-up resistor **VIP:** Host VIP data bit 3, for future expansion from the initial 2 bit host VIP port to an 4 or 8 bit port. In a 2 bit host VIP mode, this pin could also be used as a VIP interrupt (open collector, level sensitive) driven by the VIP slaves to initiate a request.
MPP2 for ImpacTV 10 pins (muxed)	SSAD(7:0)/LCD(19:12) [MDGIO(31:24)]	I/O	Address/data for MPP2 **or** future LCD interface **MPP2:** Secondary TVout only MPP line which could be optionally used to connect a TVout chip (ImpacTV, RAGE THEATER).
	SDS / SDA / LCD10 [MDGIO(22)]	I/O	MPP2 data strobe **or** I^2C data in/out **or** future LCD interface **MPP2:** Data Strobe for the secondary MPP line. **I2C:** Alternate I^2C serial data line which can be used if the default SDA line is being used for other functionality (VIP 4-8 bits). Would require an on-board pull-up if used for I^2C.
	SAS / SCL / LCD11 [MDGIO(23)]	I/O	MPP2 address strobe **or** I^2C clock out **or** future LCD interface **MPP2:** Address strobe for the secondary MPP line. **I2C:** Alternate I^2C serial clock line which can be used if the default SCL line is being used for other functionality (VIP 4-8 bits, VIP interrupt). Would require an on-board pull-up if used for I^2C
LCD Intf. 2 + 24 pins (muxed)	LCDCLK [AMCGIO(24)]	O	Future LCD interface Currently not used.
	LCDCDE [AMCGIO(25)]	O	Future LCD interface Currently not used.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Monitor 9 pins	R	O	Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Red pin of the monitor. 37.5 Ω = 75 Ω pull-down resistor on-board in parallel with the 75 Ω CRT load/Impedance.
	G	O	Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Green pin of the monitor. 37.5 Ohm = 75 Ohm pull-down resistor on-board in parallel with the 75 Ohm CRT load/Impedance.
	B	O	Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Blue pin of the monitor. 37.5 Ω = 75 Ω pull-down resistor on-board in parallel with the 75 Ω CRT load/Impedance).
	HSYNC	O	Horizontal sync with programmable polarity for the display monitor. This signal requires an on-board TTL buffer (e.g. LS125).
	VSYNC	O	Vertical sync with programmable polarity for the display monitor. This signal requires an on-board TTL buffer (e.g. LS125).
	MONID(3:0) / LCD(20:23)	I/O	Display Data Channel (DDC) / Monitor plug-n-play interface / AppleSense **or** future LCD interface.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
DAC 4 pins	AVDD	I	DAC VDD (2.5 V) Dedicated power for the RAGE 128 DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the DAC which in turn can affect the display quality. Adequate decoupling should be provided between this pin and AVSS.
	AVSS	O	DAC VSS Dedicated ground for the RAGE 128 DAC. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in turn can affect the display quality. Adequate decoupling should be provided between this pin and AVDD.
	AVSS	O	BGR VSS Dedicated ground for the RAGE 128 Band Gap Reference (DAC). Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in turn can affect the display quality. Adequate decoupling should be provided between this pin and AVDD.
	RSET	O	Internal DAC reference Used to set the full scale DAC current through a high-precision resistor (1%) of 422 Ω (preliminary value) placed between this pin and AVSS

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
PLLs & XTAL 4 pins	XTALIN	I	PLL Reference Clock or MXCLK source (14.318 - 29.4989 MHz)
	XTALOUT	O	(3.3 V or 2.5 V Input level) A series resonant crystal can be connected between these two pins to provide the reference clock for the internal PLLs of RAGE 128. An external LVTTL (3.3 / 2.5 V) oscillator can also be connected to XTALIN to provide the reference clock. In order to provide reliable functionality, proper video synchronization and high quality display, it is recommended that the crystal/oscillator have as small an error and jitter as possible, with a balanced duty cycle. Xtal characteristics (also valid for oscillators): -Frequency: 14.31818 / 29.498928 MHz (if with TVout) -Accuracy: 50 ppm -Duty Cycle (worst case): 45-55 (max) -Jitter: 500 ps (max) cycle to cycle -Voltage Supply: 2.5 V / 3.3 V
	PVDD	I	Phase Lock Loop Power (2.5 V) Dedicated power pin for the RAGE 128 PLLs. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the PLLs which in turn can affect the display quality and functional reliability of the RAGE 128. Adequate decoupling should be provided between this pin and PVSS.
	PVSS	O	Phase Lock Loop Ground Dedicated ground for the RAGE 128 PLLs. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the PLLs which in turn can affect the display quality and functional reliability of the RAGE 128. Adequate decoupling should be provided between this pin and PVDD.
Test 1 pin	TESTEN	I	Test enable This signal is dedicated to the assertion of the various test modes (nandtree, Hi Z, Chipid, tester) supported in the RAGE 128. The state of two test mode strap signals (PCICLK, GNT#) on the rising edge of TESTEN will define the test mode selected. This signal is internally pulled down by default. If on-board testing is not required, this signal should be tied to ground on the board through a 10 kΩ resistor.

Table C-1 (Continued)

Interface	Signal Name	I/O	Function
Clamps 2 pins	AGPCLAMP	I	AGPCLAMP - clamp for 5 V tolerance and signal integrity of PCI systems - For AGP systems with 3.3 V signaling, use 3.3 V. - For PCI systems with 3.3 V signaling, use 3.3 V. - For PCI systems with 5 V signaling, use 5.5 V.
	GIOCLAMP	I	GIOCLAMP - for 5 V tolerance and signal integrity on memory and multimedia GIOs - For 5 V GIO signals sent to the chip, use 5 V. - For 3.3 V GIO signals sent to the chip, use 3.3 V.
PCI Power 4 pins / 272 4pins / 328	VDDQ (PCI/AGP)	I	3.3 V I/O power for the AGP / PCI pins
I/O1 Power 5 pins / 272 4 pins / 328	VDDR1 (memory)	I	2.5 V or 3.3 V I/O power for the lower memory bus
I/O2 Power 3 pins / 272 2 pins / 328	VDDR2 (memory/ multimedia GIO)	I	2.5 V or 3.3 V I/O power for the upper memory bus and the multimedia pins
I/O3 Power 0 pins / 272 2 pins / 328	VDDR3 (multimedia GIO)	I	3.3 V I/O power for the multimedia pins
Core Power 4 pins / 272 4 pins / 328	VDDC	I	2.5 V dedicated core power, provides power to the RAGE 128 internal logic
I/O Ground 24 pins / 272 28 pins / 328	VSS	O	Common ground

Appendix D
Revision History

D.1 Rev 0.01 (Apr 1998), GC41001.pdf

- Initial draft.

D.2 Rev 0.02 (Jul 1998), GC41002.pdf

- Added 16 and 32MB to 2D Mode table.
- Changed heading 5.3 from *ROM Read/Write Timing (for 128K and Add-in Boards)* to *ROM Read/Write Timing (for 128K EPROM and Add-in Board Implementation)*
- Updated section *6.4 "Physical Dimensions" on page 6-10*: two dimension drawings and tables.

D.3 Rev 0.03 (Aug 1998), GC41003.pdf

- Added Appendix D - Revision History.
- General updates, added timing diagrams for I^2C, MPP and VIP.

D.4 Rev 0.04 (Oct 1998), GC41004.pdf

- Modified descriptions for pins AGPCLAMP and GIOCLAMP in *Appendix C* and *Chapter 6*.
- Updated *Figure 4-4. "PCI Bus Configuration" on page 4-13*. Changed IDSEL/PIPE# to IDSEL#.
- General editing.

D.5 Rev 0.50 (Nov 1998), GC41005.pdf

- Changed title of the book from RAGE 128 Graphics Controller Specifications to RAGE 128 VR and 128 GL Graphics Controller Specifications.
- Removed LCD functions in 272 BGA Top View (section 3.2). (LCD functions are kept in the listing in Appendix A, but repositioned regarding their pairing with MONIDs, i.e., it is now MONID1/LCD21 instead of previous MONID1/LCD22, etc.)

- Added new 2D mode tables in Chapter 2.
- Added 329 BGA package, and modified text throughout the document to reflect the new addition.
- General edits

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