



BURR-BROWN IC DATA BOOK

1995

QUEST-REP INC.
MANUFACTURERS' REPRESENTATIVE

6494 Weathers Place, Suite 200
San Diego, CA 92121
(619) 622-5040 • Fax: (619) 622-5047
email: questrep@questrep.com



LINEAR PRODUCTS

BURR-BROWN IC DATA BOOK
LINEAR PRODUCTS



1995

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NOTE: (*) This product can be found in the 1995
Burr-Brown IC Data Book—Linear Products.

For information on any of these products or to receive the *Burr-Brown Data Conversion Products IC Data Book*, call our automated literature request line at 1-602-741-3884, or contact your local sales representative.

How to Use This Book

If you know the
MODEL NUMBER,

Use the Model Index on the
INSIDE FRONT COVER.

If you know the
PRODUCT TYPE,

Use the **TABBED TABLE OF CONTENTS,**
or use the **SELECTION GUIDE TABLES** at
the front of each tabbed section.

If you want
NEW MODELS,

Use the Model Index on the **INSIDE FRONT
COVER** or the **SELECTION GUIDE
TABLES** at the front of each tabbed section. All
new models contained in this edition are shown
in **boldface**. Also, contact your local Burr-
Brown representative for information on new
models released since publication of this data
book.

If you want a **PRICE,**

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tive. See **INSIDE BACK COVER.**

If you want **TAPE
& REEL SPECS,**

See **TAPE & REEL SPECIFICATIONS,**
Appendix C, or contact your local Burr-Brown
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Burr-Brown Integrated Circuits Data Book

**Linear Products
1995**



For Immediate Assistance, Contact Your Local Salesperson

LI-464

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Printed in USA

Burr-Brown Corporation
International Airport Industrial Park

Mailing Address:
PO Box 11400
Tucson, AZ 85734

Street Address:
6730 S. Tucson Blvd.
Tucson, AZ 85706

Tel: (602) 746-1111⁽¹⁾ • FAX: (602) 889-1510⁽¹⁾ • Cable: BBRCORP

For immediate Product Information or Technical Assistance, call
1-800-548-6132
in the USA.

Worldwide FAX Number
1-602-889-1510⁽¹⁾

Burr-Brown FAXLine (USA Only)
1-800-548-6133

NOTE: (1) As of March 19, 1995, the area code for Arizona (except for the metropolitan Phoenix area) will be changed from 602 to 520, please dial your operator for further assistance.

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1 Burr-Brown Corporation

About Burr-Brown

Burr-Brown Corporation is an international leader in the design and manufacturer of precision microcircuits and microelectronic-based systems for use in data acquisition, signal conditioning, and control applications throughout the world.

The Company's products range from precision linear integrated circuits to data collection systems and personal computer instrumentation. The Company's integrated circuit components are used in analog and digital signal processing applications found in medical and scientific instrumentation, factory automation, automatic test equipment, process control, and consumer products such as electronic musical instruments and professional audio equipment.

Company Facts

- Founded in 1956.
- Corporate headquarters: Tucson, Arizona.
- 1470 employees.
- 1000+ products.
- Manufacturing and technical facilities in: Tucson, Arizona; Atsugi, Japan; Livingston, Scotland.
- 7 North American direct sales offices, 130 sales representatives and distributors in 180+ locations.
- International sales and distribution subsidiaries in Austria, France, Germany, Italy, Japan, the Netherlands, Switzerland, and the United Kingdom; 26 sales representatives throughout the rest of the world.
- Over 200 sales and service staff worldwide.

Burr-Brown Receives ISO9001 Certification in U.S. and Europe

In September 1993, Burr-Brown Corporation received ISO9001 certification in the United States and Europe, simultaneously. In the United States, registration is recognized through the AT&T Quality Registrar by the Registration Accreditation Board (RAB). Certification is accepted through the Electronics Industries Quality Registrar by the Dutch Registration Board (RCV) in Europe.

ISO9001 is the international standard for assessing the quality systems of companies that design, manufacture, and test products. Adopted by 91 member countries, it's the international quality standard for manufacturing, trade, and communications industries. Certification indicates that a formal quality system exists for all processes and that these processes are audited on a timely basis.



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Applications Library

Applications Bulletins and Design Software

APPLICATIONS LIBRARY

The following applications information is available from Burr-Brown at no charge.

Call 1-800-548-6132 to order.

APPLICATIONS BULLETINS

Increasing INA117 Differential Input Range	AB-001	Thermal and Electrical Properties of Selected Packaging Materials	AB-030
Make a Precision Current Source or Current Sink	AB-002	IC Building Blocks Form Complete Isolated 4-20mA Current-Loop Systems	AB-032
Voltage-Reference Filters	AB-003	Single-Supply, Low-Power Measurements of Bridge Networks	AB-033
Make a Precision -10V Reference	AB-004	MFB Low-Pass Filter Design Program	AB-034
Make a Precision ±10V Reference	AB-005	Filter Design Program for the UAF42 Universal Active Filter	AB-035
Make a -10V to +10V Adjustable Precision Voltage Source	AB-006	Diode-Based Temperature Measurement	AB-036
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BURR-BROWN CORPORATION

Sales and Service

ABOUT THIS BOOK

To keep with the easy-to-use format we established last year, the *Burr-Brown Integrated Circuits Data Books* for 1995 will be similar to the 1994 books. Both the Linear Products and Data Conversion Products books are available free from your local salesperson or representative—see **Sales Office Listings** at back of book—or by calling our literature request line at **1-800-548-6132**. Order both, or just the one that fits your needs.

How to Use This Book

Burr-Brown model numbers are listed in the Selection Guides at the beginning of each tabbed section. With these tables you can quickly compare specs among different models and choose the best part for your design. Products appearing in **boldface** type are new products introduced by Burr-Brown since publication of the 1994 data books.

Data sheets are arranged alphanumerically by product type, so if you know the name of the part you can find it quickly. Or, use the Model Index on the **inside front cover**, or page numbers as listed in the Selection Guide tables.

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In addition to individual data sheets, Burr-Brown also provides its customers with applications bulletins, a comprehensive product selection guide on either a PC or Macintosh diskette, promotional samples, comprehensive brochures featuring many product types, and applications assistance by calling **1-800-548-6132**.

Literature requests may also be posted 24 hours/day by calling our automated literature request line at **(602) 741-3884**. When using this service, please be prepared to give your name, company, full address and phone number, as well as the product name or type of literature you are requesting.

FAXLine

The Burr-Brown **FAXLine** is now available for customer requests for product literature. Call **1-800-548-6133** (USA Only) to receive a Component Literature Fax Form, complete with **FAXLine** literature order numbers. Up to three pieces of literature may be requested per call.

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Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. Please call your local sales representative or distributor (see list at the back of this book).

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Or, Call Customer Service at 1-800-548-6132 (USA Only)

Sales and Service

Returns and Warranty Service

When returning products for any reason, contact Burr-Brown prior to shipping for authorization and shipping instructions. For complete instructions, contact your local salesperson or representative. Customers outside the USA should call the nearest sales office for details and information—see **International Sales Office Listing** at back of book.

To return product, please call for your RMA number. Ship units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned devices, Burr-Brown will verify the mal-

function and inform you of the warranty status, cost to repair or replace, credits, and status of replacements where applicable.

Area Code Alert!

Beginning March 19, 1995, the area code for Arizona will be changed from a single area code state to a dual area code state (The area code for the entire state, with the exception of the Phoenix Metropolitan area, will change from **602** to **520**.) The phone company will provide a new number change message until June, 1995.

BURR-BROWN CORPORATION



2 Operational Amplifiers

The following selection guides include new products which combine exceptional performance with monolithic IC reliability and economy. Many of these products implement low noise bipolar, **Difet**[®], and wideband complementary bipolar processes.

The following highlights some of our newest developments:

OPA124—Low Cost, Low Noise Op Amp. Proven **Difet**[®] technology in low cost 8-pin plastic DIP and surface mount packages. High performance grade offers 1pA bias current and 2μV/°C drift.

OPA129—Ultra-Low Bias Current **Difet**[®] Op Amp. This amplifier has bias current under 100fA in a low cost, 8-pin plastic DIP and SOIC package.

OPA64x—Wideband Op Amps. This series offers unity-gain bandwidths up to 1.3GHz while providing other unique features such as:

- 95dBc Spurious Free Dynamic Range
- 1.8nV/√Hz Voltage Noise
- 55mW Power Dissipation
- 2500V/μs Slew Rate
- 0.007%/0.008° Differential Gain/Phase Errors

OPA628—Low Distortion Voltage Feedback Op Amp. This product features 0.1dB gain flatness to 30MHz together with differential gain error 0.015% max and differential phase error of 0.015° max.

OPA65x—Low Cost, Wideband Op Amps. This high speed family of eight features both current

and voltage feedback models with unity gain stable bandwidths up to 900MHz and input bias currents as low as 100pA. Two models are also available in dual and quad configurations.

OPA2604—Dual FET-Input, Low Distortion Op Amp. This low cost, dual op amp features 0.0003% distortion and wide supply range (to ±24V).

OPA678—Wideband Switched-Input Op Amp. This amplifier has two input stages which can be switched to the output stages in 4ns.

VCA610—Wideband Voltage Controlled Amplifier. This product has a gain control range from -40dB to +40dB and is available in an 8-pin plastic DIP or SOIC package.

OPA2662—Dual, Wide-Bandwidth Transconductance Amplifier. This product is ideal for applications requiring a tightly controlled current to drive laser diodes, tuning coils, and driver transformers.

Spice macromodels are available for many of our products. By using a simulation program with integrated circuit emphasis (SPICE), designers can model amplifier behavior to investigate circuit performance over a variety of conditions and signals.

Power operational amplifiers and buffers are described in Section 3, instrumentation amplifiers in Section 4, and isolation amplifiers in Section 5.

SPECIAL PURPOSE OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Offset Voltage, max		Bias Current (25°C) max (μA)	Open Loop Gain min (dB)	Frequency Response		Rated Output, min (±V) (±mA)	Temp Range ⁽¹⁾	Pkg	Page No.
		At 25°C, (±mV)	Temp Drift, (±μV/°C)			Unity Gain (MHz)	Slew Rate (V/μs)				
Two-Channel	OPA675	1	5	35	65	185 ⁽²⁾	350	2.1 30	Com, Mil	DIP	2.353
	OPA676	1	5	35	65	185 ⁽²⁾	350	2.1 30	Com, Mil	DIP	2.353
	OPA678	1.5	20	50	50	200	350	2.5 30	Com, Mil	DIP, SOIC	2.366
Voltage Controlled Gain	VCA610	—	—	6 ⁽³⁾	⁽⁴⁾	30 ⁽⁵⁾	60	3.0 ⁽⁶⁾ 80 ⁽⁷⁾	Ind	DIP, SOIC	2.449

NOTES: (1) Com = 0°C to +70°C, Mil = -55°C to +125°C. (2) -3dB BW at Gain of +10V/V. (3) Typical. (4) C/L Gain range: -40 to +40dB. (5) Gain = 40dB. (6) Vp-p typ. (7) Short circuit current.

Difet[®], Burr-Brown Corporation



For Immediate Assistance, Contact Your Local Salesperson

LOW DRIFT OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Offset Voltage max		Bias Current (25°C) max (nA)	Open Loop Gain min (dB)	Frequency Response		Rated Output, min		Temp Range ⁽¹⁾	Pkg	Page No.
		At 25°C (±mV)	Temp Drift (±μV/°C)			Unity Gain ⁽²⁾ (MHz)	Slew Rate ⁽³⁾ (V/μs)	(±V)	(±mA)			
FET	OPA627	0.1	0.8	.005	112	16	55	11.5	45 ⁽³⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA637	0.1	0.8	.005	112	80	135	11.5	45 ⁽³⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA111	0.25	1	±0.001	120	2	2	11	5.5	Ind	TO-99	2.27
	OPA124	0.25	2	±0.001	120	1.5	1	11	5.5	Ind	DIP, SOIC	2.45
	OPA671	5.0	10 ⁽³⁾	.05	74	35	107	10.5	50	Ind	DIP	2.346
Wideband	OPA602	0.25	2	±0.01	92	6.5	35	11.5	15	Ind	TO-99, DIP, SOIC	2.85
	OPA606	0.5	5	±0.01	100	13	35	12	5	Com	TO-99, DIP	2.118
	OPA671	5.0	10 ⁽³⁾	.05	74	35	107	10.5	50	Ind	DIP	2.346
Dual FET	OPA2111	0.5	2.8	±0.004	114	2	2	10	5	Ind, Mil	TO-99, DIP	2.397
	OPA2107	0.5	5	.005	84	4.5 ⁽⁵⁾	18	11	5.5	Ind	TO-99, DIP, SOIC	2.390
Low Power (Dual) Single Supply Operation	OPA1013	0.3	2.5	30	120	0.6	.35	12	6.5	Com	DIP	2.381
Bipolar	OPA177	0.01	0.1	1.5	134	0.6	0.3	12	12	Ind	DIP, SOIC	2.19
	OPA77	0.025	0.3	2.0	134	0.6	0.3	12	12	Ind	DIP	2.19
	OPA27	0.025	0.6	±40	120	8	1.9	12	16.7	Mil, Com	TO-99, DIP, SOIC	2.6
	OPA37	0.025	0.6	±40	120	63	11.9	12	16.7	Mil, Com	TO-99, DIP, SOIC	2.6

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, Mil = -55°C to +125°C. (2) Gain BW Product at G = 5. (3) Typical. (4) Gain BW Product at G = 10. (5) Gain BW Product at G = 100.

LOW BIAS CURRENT OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Offset Voltage max		Bias Current (25°C) max (pA)	Open Loop Gain min (dB)	Frequency Response		Rated Output, min		Temp Range ⁽¹⁾	Pkg	Page No.
		At 25°C (±mV)	Temp Drift (±μV/°C)			Unity Gain ⁽²⁾ (MHz)	Slew Rate ⁽²⁾ (V/μs)	(±V)	(±mA)			
FET	OPA111	0.25	1	±1	120	2	2	11	5.5	Ind	TO-99	2.27
	OPA124	0.25	2	±1	120	1.5	2	11	5.5	Ind	DIP, SOIC	2.45
	OPA627	0.1	0.8	5	112	16	55	11.5	45 ⁽²⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA637	0.1	0.8	5	112	80 ⁽⁴⁾	135	11.5	45 ⁽²⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA671	5.0	10 ⁽³⁾	50	74	35	107	10.5	50	Ind	DIP	2.346
Ultra-Low Bias Current	OPA128	0.5	5	±0.075	110	1	3	10	5	Com	TO-99	2.53
	OPA129	1.5	15	±0.100	94	1	3	10	5	Com	DIP, SOIC	2.62

LOW BIAS CURRENT OPERATIONAL AMPLIFIERS (Continued)												Page No.
Description	Model	Offset Voltage, max		Bias Current (25°C) max (pA)	Open Loop Gain min (dB)	Frequency Response		Rated Output, min		Temp Range ⁽¹⁾	Pkg	
		At 25°C (±mV)	Temp Drift (±µV/°C)			Unity Gain (MHz)	Slew Rate (V/µs)	(±V)	(±mA)			
Dual FET	OPA2111	0.5	2.8	±4	114	2	2	10	5	Ind	TO-99, DIP	2.397
	OPA2107	0.5	5	5	84	4.5	18	11	5.5	Ind	TO-99, DIP, SOIC	2.390
Quad FET	OPA404	0.75	3 ⁽²⁾	±4	92	6.4	35	11.5	5	Ind	DIP, SOIC	2.71
Low Cost	OPA121	2	10	±5	110	2	2	11	5.5	Com	TO-99, DIP, SOIC	2.39
	OPA602	0.25	2	1	92	6.5	35	11.5	15	Ind	TO-99, DIP, SOIC	2.85
Wideband	OPA606	0.5	5	±10	100	13	35	12	5	Com DIP	TO-99, DIP	2.118
	OPA654	3	40 ⁽²⁾	50	94 ⁽²⁾	32	750	11	200 ⁽²⁾	Ind	TO-3	2.316
	OPA671	5.0	10 ⁽³⁾	50	74	35	107	10.5	50	Ind	DIP	2.346

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, Mil = -55°C to +125°C. (2) Typical. (3) Gain = 3V/V. (4) Gain BW Product at G = 10.

LOW NOISE OPERATIONAL AMPLIFIERS												Page No.	
Description	Model	Noise Voltage at 10kHz, max (nV/√Hz)	Offset Voltage, max		Bias Current (25°C) max (pA)	Open Loop Gain min (dB)	Frequency Response		Rated Output, min		Temp Range ⁽¹⁾	Pkg	
			at 25°C (±mV)	Temp Drift (±µV/°C)			Gain BW (MHz)	Slew Rate min (V/µs)	(±V)	(±mA)			
Bipolar	OPA27	3.8	0.025	0.6	±40nA	120	8	1.9	12	16.7	Mil	TO-99, DIP, SOIC	2.6
	OPA37	3.8	0.025	0.6	±40nA	120	63	11	12	16.7	Mil	TO-99, DIP, SOIC	2.6
	OPA177	10 ⁽²⁾	0.01	0.1	1.5nA	134	0.6	0.1	12	12	Ind	DIP, SOIC	2.19
	OPA77	11	0.025	0.3	2.0nA	134	0.6	0.1	12	12	Ind	DIP	2.19
FET	OPA111	8	0.25	1	±1	120	2	1	11	5.5	Ind	TO-99	2.27
	OPA124	6 ⁽²⁾	.25	2	±1	120	1.5	1	11	5.5	Ind	DIP SOIC	2.45
	OPA602	12 ⁽²⁾	0.25	2	1	92	6.5	28	11.5	15	Ind	TO-99, DIP, SOIC	2.85
	OPA627	6	0.1	0.8	5	112	16	40	11.5	45 ⁽²⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA637	6	1	0.8	5	112	80	100	11.5	45 ⁽²⁾	Ind	TO-99, DIP, SOIC	2.193
	OPA604 ⁽³⁾	10 ⁽²⁾	3	8 ⁽²⁾	50 ⁽²⁾	80	20	15	11	35 ⁽²⁾	Ind	DIP, SOIC	2.106
OPA2604 ⁽³⁾	10 ⁽²⁾	3	8 ⁽²⁾	100 ⁽²⁾	80	20	15	11	35 ⁽²⁾	Ind	DIP, SOIC	2.410	
Low Cost	OPA27	4.5	0.100	1.8	±80nA	117	8	1.7	12	16.7	Com	DIP, SOIC	2.6
	OPA37	4.5	0.100	1.8	±80nA	117	63	11	12	16.7	Com	DIP, SOIC	2.6
Dual FET	OPA2111	8	0.5	2.8	±4	114	2	2	10	5	Ind	TO-99, DIP	2.397

NOTES: (1) Ind = -25°C to +85°C, Mil = -55°C to +125°C, Com = 0°C to +70°C. (2) Typical. (3) Low distortion, 0.0003%.

2 OPERATIONAL AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

UNITY-GAIN BUFFER OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Rated Output, min		Frequency Response			Gain (V/V)	Input Impedance (Ω)	Temp Range ⁽¹⁾	Pkg	Page No.
		(\pm V)	(\pm mA)	-3dB (MHz)	Full Power (MHz)	SR (V/ μ s)					
High Performance	3553	10	200	300	32	2000	\approx 1	10 ¹¹	Ind	TO-3	A
Low Cost	BUF634	10	250	180		2000	\approx 1	50M	Ind	DIP, SO-8, TO-220	3.18
	OPA633	11	80	275	65	2500	\approx 1	1.5M	Ind	DIP	3.70
Transconductance Amp and Buffer	OPA660	3.7	10	850	570	3000	\approx 1	1M	XInd	DIP, SOIC	2.328
High Slew Rate	BUF600	3.3	20	650	320	3400	\approx 1	4.8M	XInd	DIP, SOIC	3.1.3
	BUF601	3.3	20	900	320	3600	\approx 1	2.5M	XInd	DIP, SOIC	3.1.3

NOTE: (1) Ind = -25°C to +85°C. (2) XInd = -40°C to +85°C.

"A" indicates a product that is still available but not included in the 1995 Data Books—contact factory for data sheet.

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Frequency Response				Comp	Rated Output, min		Offset Voltage, max		Open Loop Gain, min (dB)	Temp Range ⁽¹⁾	Pkg	Page No.
		Gain BW (MHz)	Slew Rate min (V/ μ s)	t_s \pm 0.1% (ns)			(\pm V)	(\pm mA)	At 25°C (\pm mV)	Temp Drift (\pm μ V/°C)				
FET	OPA602	6.5 ⁽⁹⁾	28	600	int	11.5	15	0.25	2	92	Ind	TO-99, DIP, SOIC	2.85	
	OPA604	20	15	1 μ s	int	11	35 ⁽²⁾	3	8 ⁽²⁾	80	Ind	DIP, SOIC	2.106	
	OPA654	32	750 ⁽²⁾	150	ext	11	200 ⁽²⁾	3	40 ⁽²⁾	94 ⁽²⁾	Ind	TO-3	2.316	
	OPA655	400	300	12	int	2.5	35⁽²⁾	1	20	55	XInd, Mil	DIP, SOIC	2.324	
	OPA671	35	107	150	int	10.5	50 ⁽²⁾	5	10 ⁽²⁾	74 ⁽²⁾	Ind	DIP	2.346	
Dual	OPA2107	4.5 ⁽⁹⁾	13	1.5 μ s	int	11	5.5	0.5	5	84	Ind, Mil	TO-99, DIP, SOIC	2.390	
Dual	OPA2604	20	15	1 μ s	int	11	35 ⁽²⁾	3	8 ⁽²⁾	80	Ind	DIP, SOIC	2.410	
Op Amp	OPA606	13	25	1 μ s	int	12	5	0.5	5	100	Com	TO-99, DIP	2.118	
	OPA627	16	40	450	int	11.5	45 ⁽²⁾	0.1	0.8	112	Ind	TO-99, DIP, SOIC	2.193	
	OPA637	80	100	300	G>5	11.5	45 ⁽²⁾	0.1	0.8	112	Ind	TO-99, DIP, SOIC	2.193	
	3554	1700, A=1000	1000	120	ext	10	100	1	15	100	Ind	TO-3	2.461	
Current-Feedback	OPA603	160	1000 ⁽²⁾	50	int	10	150 ⁽²⁾	5	8 ⁽²⁾	440k Ω ⁽⁸⁾	Ind	DIP	2.94	
	OPA644 OPA648	500 1GHz	2500 1200	16.5 9	int int	2.75 2.2	40 25	3.0 6.0	35 10⁽²⁾	2MΩ⁽⁸⁾ 165kΩ⁽⁹⁾	Ind, Mil XInd, Mil	DIP, SOIC DIP, SOIC	2.275 2.301	
Low Power Current-Feedback	OPA623	350	2100 ⁽²⁾	9	NA	3.0	70	-8 ⁽²⁾	125 ⁽²⁾	53	XInd	DIP, SOIC	2.177	
	OPA658 OPA2658 OPA4658	900 750 750	1700⁽²⁾ 1700 1700	11.5 11.5 11.5	int int int	2.5 2.5 2.5	30 30 30	5.5 5 5	20⁽²⁾ 25 25	100kΩ⁽⁸⁾ TBD TBD	XInd XInd XInd	DIP, SOIC DIP, SOIC DIP, SOIC	2.326 2.424 2.447	
Transconductance Amp and Buffer	OPA660	850	3000 ⁽²⁾	25	NA	4.0	10	+7 ⁽²⁾	50 ⁽²⁾	125 ⁽⁷⁾	Ind	DIP, SOIC	2.328	
Dual Transconductance Amp	OPA2662	370	58⁽⁹⁾	2.6⁽⁹⁾	NA	3.4	75	12⁽²⁾	35	580⁽⁷⁾	XInd	DIP, SOIC	2.426	
Quad FET	OPA404	6.4	28	600	int	11.5	5	0.75 ⁽²⁾	3 ⁽²⁾	92	Ind	DIP, SOIC	2.71	
Low Noise Bipolar	OPA27	8, A=1	1.7	—	int	12	16.7	0.025	0.6	120	Mil	TO-99, DIP	2.6	
	OPA37	63, A=5	11	—	int ⁽⁹⁾	12	16.7	0.025	0.6	120	Mil	TO-99, DIP	2.6	

WIDE BANDWIDTH OPERATIONAL AMPLIFIERS (Continued)

Boldface = NEW

Description	Model	Frequency Response			Comp	Rated Output		Offset Voltage max		Open Loop Gain, min (dB)	Temp Range ⁽¹⁾	Pkg	Page No.
		Gain BW (MHz)	Slew Rate min (V/ μ s)	t_s $\pm 0.1\%$ (ns)		($\pm V$)	($\pm mA$)	At 25°C ($\pm mV$)	Temp Drift ($\pm \mu V/^\circ C$)				
Low Distortion	OPA628	160	310 ⁽²⁾	20	int	3	30	1	6 ⁽²⁾	90	XInd	DIP, SOIC	2.206
	OPA642	450	380 ⁽²⁾	11.5	int	2.5	35	1.0	2.0 ⁽²⁾	95 ⁽²⁾	XInd, Mil	DIP, SOIC	2.247
	OPA643	1.5GHz A=5	1000	16.5	int	2.5	40	1.5	3 ⁽²⁾	95 ⁽²⁾	XInd, Mil	DIP, SOIC	2.262
Very Wideband Low Noise Low Power	OPA640	1.3GHz	350	18	int	2.25	25	2.0	6 ⁽²⁾	57 ⁽²⁾	XInd, Mil	DIP, SOIC	2.221
	OPA641	1.6GHz A=2	640	6	int	2.2	25	2.0	6⁽²⁾	57⁽²⁾	XInd, Mil	DIP, SOIC	2.254
Low Noise Wideband	OPA646	650	180	11.5	int	2.0	25	2.5	12	51 ⁽²⁾	XInd, Mil	DIP, SOIC	2.288
	OPA651	575 A=2	350	11.5	int	2.5	30	1.0	3⁽²⁾	47	XInd	DIP, SOIC	
Low Noise Wideband	OPA620	300	175	13	int	3	50	0.5	8 ⁽²⁾	55	Ind, Mil	DIP, SOIC	2.127
	OPA621	500, A=2	350	15	int	3	50	0.5	12 ⁽²⁾	55	Ind, Mil	DIP,	2.143
High Slew Rate	OPA622	250	1600 ⁽²⁾	17	NA	3	70	0.1 ⁽²⁾	210 ⁽²⁾	50	XInd	DIP, SOIC	2.159
Fast Settling	OPA600	5000, A=1000	400	80	ext	9	180	4	20	86	Ind	DIP	2.82
Very Fast Settling Switched Input	OPA675	3000, A=16	240	15	ext	2.1	30 ⁽²⁾	1	5	65	Com, Mil	DIP	2.353
	OPA676	3000, A=16	240	15	ext	2.1	30 ⁽²⁾	1	5	65	Com, Mil	DIP	2.353
	OPA678	200 A=1	350 ⁽²⁾	22	ext	2.5	44	1	10	50	Ind, Mil	DIP, SOIC	2.366
Low Cost	OPA27	8, A=1	1.7	—	int	12	16.7	0.100	1.8	117	Com	DIP, SOIC	2.6
	OPA37	63, A=5	11	—	int ⁽³⁾	12	16.7	0.100	1.8	117	Com	DIP, SOIC	2.6
	OPA650	560	180	11.5	int	2.0	30	1	3⁽²⁾	45	XInd	DIP, SOIC	2.312
Dual Quad	OPA2650	560	180	11.5	int	2.5	25	3	5	43	XInd	DIP, SOIC	2.422
	OPA4650	900	1500	11.5	int	2.5	25	3	5	43	XInd	DIP, SOIC	2.422
Voltage Controlled Gain	VCA610	30	60	—	int	2	80 Short Circuit	—	—	C/L	Ind	DIP, SOIC	2.449

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, XInd = -40°C to +85°C, Mil = -55°C to +125°C. (2) Typical. (3) G = 5 min. (4) Typical G \geq 50. (5) Rise time, 10% to 90%. (6) Current output, mA/ns. (7) Transconductance, mA/V. (8) Open-loop transimpedance. (9) Gain Bandwidth G=100.

HIGH VOLTAGE, HIGH CURRENT OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Rated Supply ($\pm V$)	Output Current ($\pm mA$)	Offset Voltage		Bias Current (25°C), max (pA)	Frequency Response		Open Loop Gain (dB)	Temp Range ⁽¹⁾	Pkg	Page No.
				At 25°C ($\pm mV$)	Temp Drift ($\pm \mu V/^\circ C$)		Unity Gain (MHz)	Slew Rate (V/ μ s)				
High Power	OPA501	± 34	10A	5	40	20nA	1	1.35	98	Ind	TO-3	3.2.33
	OPA502	± 45	10A	5	5 ⁽⁶⁾	200	1.4	10	103	XInd/Mil	TO-3	3.2.39
	OPA511	22	5A	10	65	40nA	1	1	91	Ind	TO-3	A
	OPA512	± 45	10A	6	65	30nA	4	2.5	110	Ind	TO-3	3.2.49
		± 45	15A	3	40	20nA	4	2.5	110	Mil	TO-3	
	OPA541	± 40	5A	1	30	50	1.6	6	90	Ind/Mil	TO-3	3.2.55
± 35		5A	10	40	50	1.6	6	90	Ind	Power Plastic		
(Dual)	OPA2541	± 40	5A	1	30	50	1.6	6	90	Ind/Mil	TO-3	3.2.78
	OPA544	± 35	2A	5	10	100	1.4	8	90	XInd	5-Pin TO-220	3.2.63
(Dual)	OPA2544	± 35	2A	5	10	50	1.4	8	90	XInd/Mil	TO-3	3.2.63
	3573	20	2A ⁽⁴⁾	10	65	40nA	1	2.6	94	Ind	TO-3	A

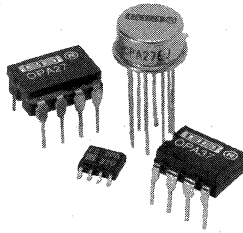
NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, XInd = -40°C to +85°C, Mil = -55°C to +125°C. (2) Typical. (3) G = 5 min. (4) Typical G \geq 50. (5) Rise time, 10% to 90%. (6) Current output, mA/ns. (7) Transconductance, mA/V. (8) Open-loop transimpedance. (9) Gain Bandwidth G=100.

"A" indicates a product that is still available but not included in the 1995 Data Books—contact factory for data sheet.

OPERATIONAL AMPLIFIERS

2

For Immediate Assistance, Contact Your Local Salesperson



OPA27
OPA37

Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- LOW NOISE: $3.8\text{nV}/\sqrt{\text{Hz}}$ max at 1kHz
- LOW OFFSET: $25\mu\text{V}$ max
- LOW DRIFT: $0.6\mu\text{V}/^\circ\text{C}$
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 114dB min
- HIGH POWER SUPPLY REJECTION: 100dB min
- FITS OP-07, OP-05, AD510, AD517 SOCKETS

APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIER
- RADIATION HARD EQUIPMENT

DESCRIPTION

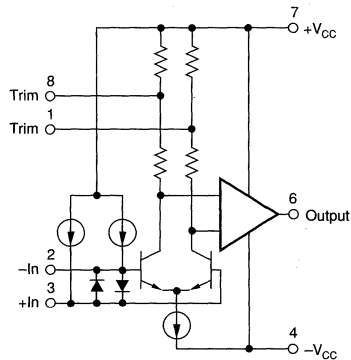
The OPA27/37 is an ultra-low noise, high precision monolithic operational amplifier.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full -55°C to $+125^\circ\text{C}$ temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain ≥ 5 .

The Burr-Brown OPA27/37 is an improved replacement for the industry-standard OP-27/OP-37.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT												
NOISE⁽⁶⁾ Voltage, $f_o = 10\text{Hz}$ $f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$ $f_b = 0.1\text{Hz}$ to 10Hz Current, ⁽¹⁾ $f_o = 10\text{Hz}$ $f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$			3.1	5.5		3.5	5.5		3.8	8.0	nV/√Hz	
			2.9	4.5		3.1	4.5		3.3	5.6	nV/√Hz	
			2.7	3.8		3.0	3.8		3.2	4.5	nV/√Hz	
			0.07	0.18		0.08	0.18		0.09	0.25	μVp-p	
			1.7	4.0		1.7	4.0		1.7	4.0	pA/√Hz	
			1.0	2.3		1.0	2.3		1.0	2.3	pA/√Hz	
		0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz		
OFFSET VOLTAGE⁽²⁾ Input Offset Voltage Average Drift ⁽³⁾ Long Term Stability ⁽⁴⁾ Supply Rejection	T_{AMIN} to T_{AMAX}		±6	±25		±12	±60		±25	±100	μV	
			±0.2	±0.6		±0.3	±1.3		±0.4	±1.8 ⁽⁶⁾	μV/°C	
			0.2	1		0.3	1.5		0.4	2.0	μV/mo	
		$\pm V_{CC} = 4$ to 18V	100	134		100	125		94	120	dB	
		$\pm V_{CC} = 4$ to 18V		±0.2	±10		±0.6	±10		±1	±20	μV/V
BIAS CURRENT Input Bias Current			±11	±40		±13	±55		±15	±80	nA	
OFFSET CURRENT Input Offset Current			6	35		8	50		10	75	nA	
IMPEDANCE Common-Mode			3 2.5			2.5 2.5			2 2.5		GΩ pF	
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 11\text{VDC}$		±11	±12.3		±11	±12.3		±11	±12.3	V	
			114	128		106	125		100	122	dB	
OPEN-LOOP GAIN, DC												
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$ $R_L \geq 1\text{k}\Omega$		120	126		120	125		117	124	dB	
			118	125		118	125		124	124	dB	
FREQUENCY RESPONSE												
Gain-Bandwidth Product ⁽⁵⁾	OPA27 OPA37		5	8		5	8		5 ⁽⁶⁾	8	MHz	
Slew Rate ⁽⁵⁾	$V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$		45	63		45	63		45 ⁽⁶⁾	63	MHz	
			1.7	1.9		1.7	1.9		1.7 ⁽⁶⁾	1.9	V/μs	
Settling Time, 0.01%	OPA27, G = +1		11	11.9		11	11.9		11 ⁽⁶⁾	11.9	V/μs	
	OPA27, G = +1		25	25		25	25		25	25	μs	
	OPA37, G = +5		25	25		25	25		25	25	μs	
RATED OUTPUT												
Voltage Output	$R_L \geq 2\text{k}\Omega$ $R_L \geq 600\Omega$		±12	±13.8		±12	±13.8		±12	±13.8	V	
			±10	±12.8		±10	±12.8		±10	±12.8	V	
Output Resistance	DC, Open Loop		70	70		70	70		70	70	Ω	
Short Circuit Current	$R_L = 0\Omega$		25	60		25	60		25	60 ⁽⁶⁾	mA	
POWER SUPPLY												
Rated Voltage			±15	±15		±15	±15		±15	±15	VDC	
Voltage Range, Derated Performance			±4	±22		±4	±22		±4	±22	VDC	
			3	4.7		3	4.7		3.3	5.7	mA	
Current, Quiescent	$I_o = 0\text{mADC}$		3	4.7		3	4.7		3.3	5.7	mA	
TEMPERATURE RANGE												
Specification A, B, C (J, Z) E, F (J, Z) G (P, U, J, Z) Operating J, Z P, U			-55	+125		-55	+125		-55	+125	°C	
			-25	+85		-25	+85		-40	+85	°C	
											°C	
				-55	+125		-55	+125		-55	+125	°C
										-40	+85	°C

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specifications on grades A and E are also guaranteed with units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter guaranteed by design.

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ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range											
A, B, C (J, Z)		-55		+125	-55		+125	-55		+125	°C
E, F (J, Z)		-25		+85	-25		+85				°C
G (P, U, J, Z)								-40		+85	°C
INPUT											
OFFSET VOLTAGE ⁽¹⁾											
Input Offset Voltage											
A, B, C			±24	±60		±45	±200		±60	±300	μV
E, F, G			±17	±50		±33	±140		±48	±220 ⁽³⁾	μV
Average Drift ⁽²⁾	$T_{A MIN}$ to $T_{A MAX}$		±0.2	±0.6		±0.3	±1.3		±0.4	±1.8 ⁽³⁾	μV/°C
Supply Rejection											
A, B, C	$\pm V_{CC} = 4.5$ to 18V	96	130		94	127		86	122		dB
E, F, G	$\pm V_{CC} = 4.5$ to 18V	97	130		96	127		90 ⁽³⁾	122		dB
BIAS CURRENT											
Input Bias Current											
A, B, C			±16	±60		±22	±95		±29	±150	nA
E, F, G			±13	±60		±16	±95		±21	±150 ⁽³⁾	nA
OFFSET CURRENT											
Input Offset Current											
A, B, C			23	50		25	85		35	135	nA
E, F, G			12	50		14	85		20	135 ⁽³⁾	nA
VOLTAGE RANGE											
Common-Mode Input Range											
A, B, C		±10.3	±11.5		±10.3	±11.5		±10.3	±11.5		V
E, F, G		±10.5	±11.8		±10.5	±11.8		±10.5 ⁽³⁾	±11.8		V
Common-Mode Rejection	$V_{IN} = \pm 11\text{VDC}$										
A, B, C		108	124		100	122		94	120		dB
E, F, G		110	126		102	124		96 ⁽³⁾	122		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$										
A, B, C		116	121		114	120		110	118		dB
E, F, G		118	123		117	122		113 ⁽³⁾	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$										
A, B, C		±11.5	±13.7		±11.0	±13.5		±10.5	±13.3		V
E, F, G		±11.7	±13.8		±11.4	±13.6		±11.0 ⁽³⁾	±13.4		V
Short Circuit Current	$V_O = 0\text{VDC}$		25			25			25		mA

NOTES: (1) Offset voltage specifications on grades A and E are also guaranteed with the units fully warmed up. Grades B, C, F, and G are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8kΩ to 20kΩ potentiometer. (3) This parameter guaranteed by design in P-DIP, "P" package and SOIC "U" package.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation ⁽¹⁾	500mW
Input Voltage	± V_{CC}
Output Short-Circuit Duration ⁽²⁾	Indefinite
Differential Input Voltage ⁽³⁾	±0.7V
Differential Input Current ⁽³⁾	±25mA
Storage Temperature Range:	
J, Z	-65°C to +150°C
P, U	-55°C to +125°C
Operating Temperature Range:	
A, B, C, E, F, G (J, Z)	-55°C to +125°C
G (P, U)	-40°C to +85°C
Lead Temperature:	
J, Z, P (soldering, 10s)	+300°C
U (soldering, 3s)	+260°C

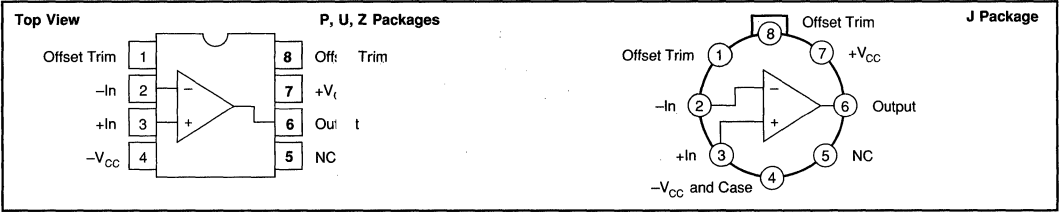
PACKAGE TYPE	θ_{JA}	UNITS
TO-99 (J)	150	°C/W
8-Pin Hermetic DIP (Z)	150	°C/W
8-Pin Plastic DIP (P)	100	°C/W
8-Pin SOIC (U)	160	°C/W

NOTES: (1) Maximum package power dissipation vs ambient temperature; (2) To common with $\pm V_{CC} = 15\text{V}$. (3) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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CONNECTION DIAGRAMS



ORDERING INFORMATION

MODEL ⁽¹⁾	PACKAGE	TEMPERATURE RANGE (°C)	OFFSET VOLTAGE MAX (μV), 25°C
OPA27AJ	TO-99	-55 to +125	±25
OPA27BJ	TO-99	-55 to +125	±60
OPA27CJ	TO-99	-55 to +125	±100
OPA27EJ	TO-99	-25 to +85	±25
OPA27FJ	TO-99	-25 to +85	±60
OPA27GJ	TO-99	-40 to +85	±100
OPA27AZ	Ceramic	-55 to +125	±25
OPA27BZ	Ceramic	-55 to +125	±60
OPA27CZ	Ceramic	-55 to +125	±100
OPA27EZ	Ceramic	-25 to +85	±25
OPA27FZ	Ceramic	-25 to +85	±60
OPA27GZ	Ceramic	-40 to +85	±100
OPA27GP	Plastic	-40 to +85	±100
OPA27GU ⁽²⁾	SOIC	-40 to +85	±100

NOTE: (1) Packages and prices for OPA37 are same as for OPA27. (2) OPA27GU may be marked OPA27U. Likewise, OPA37GU may be marked OPA37U.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA27AJ	TO-99	001
OPA27BJ	TO-99	001
OPA27CJ	TO-99	001
OPA27EJ	TO-99	001
OPA27FJ	TO-99	001
OPA27GJ	TO-99	001
OPA27AZ	Ceramic	001
OPA27BZ	Ceramic	161
OPA27CZ	Ceramic	161
OPA27DZ	Ceramic	161
OPA27EZ	Ceramic	161
OPA27FZ	Ceramic	161
OPA27GZ	Ceramic	161
OPA27GP	Plastic	006
OPA27GU ⁽²⁾	SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

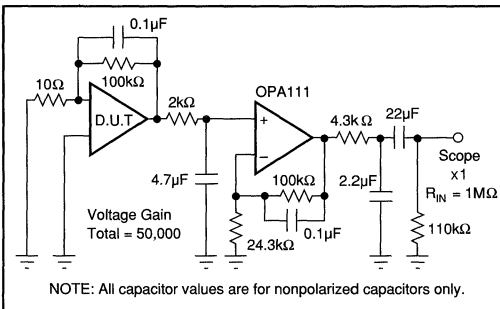


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

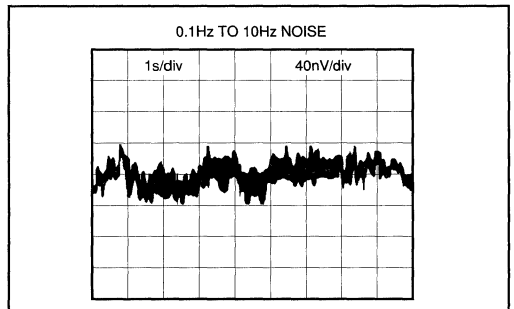
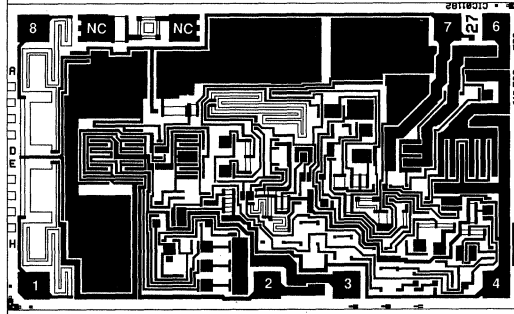


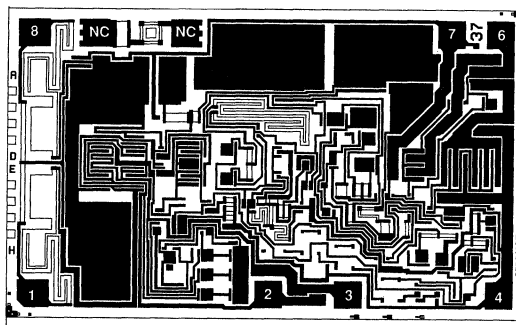
FIGURE 2. Low Frequency Noise.

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DICE INFORMATION



OPA27 DIE TOPOGRAPHY



OPA37 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	No Pad
2	-In	6	Output
3	+In	7	+V _{CC}
4	-V _{CC}	8	Offset Trim
		NC	No Connection

Substrate Bias: -V_{CC}

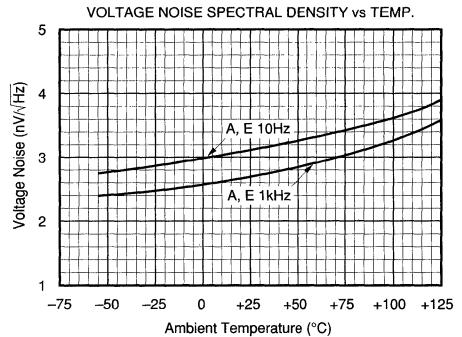
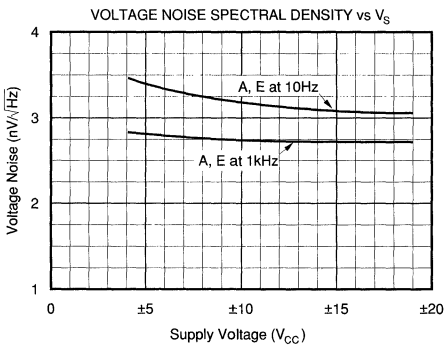
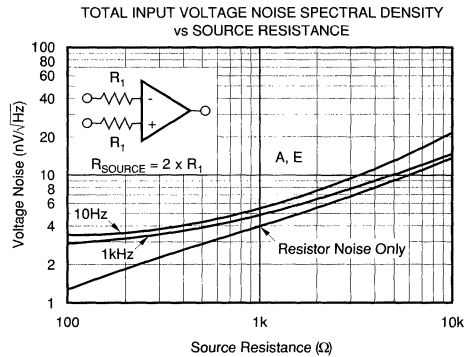
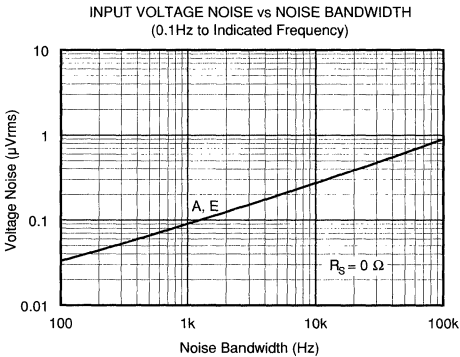
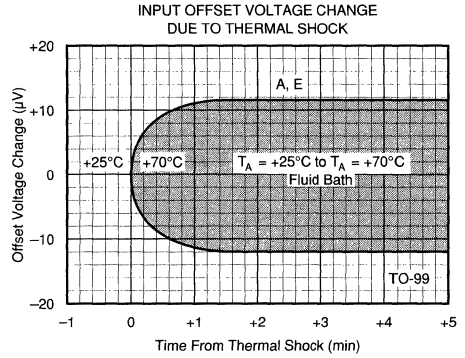
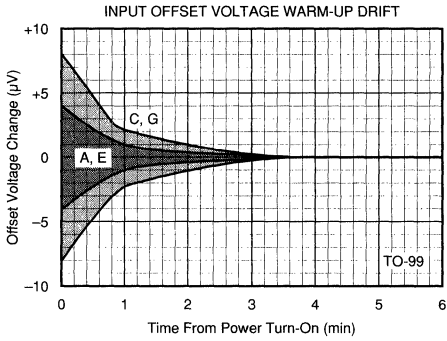
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	99 x 61 ±5	2.51 x 1.55 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
OPA27 Transistor Count		47
OPA37 Transistor Count		42
Backing		Gold

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TYPICAL PERFORMANCE CURVES

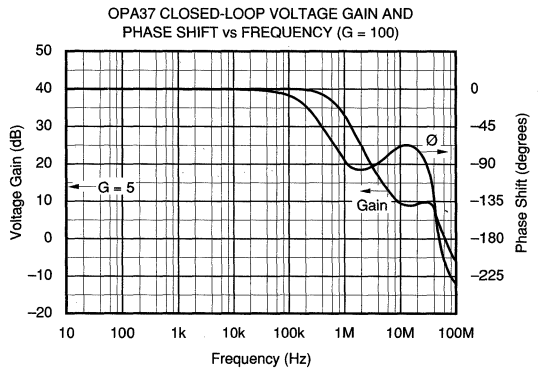
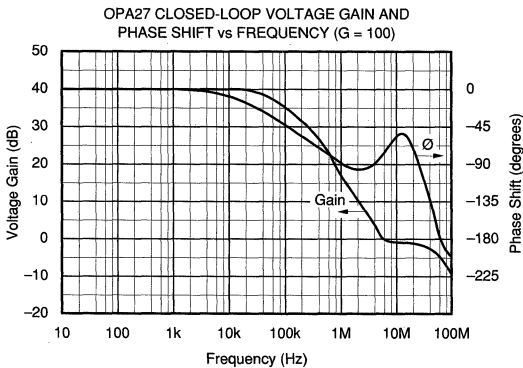
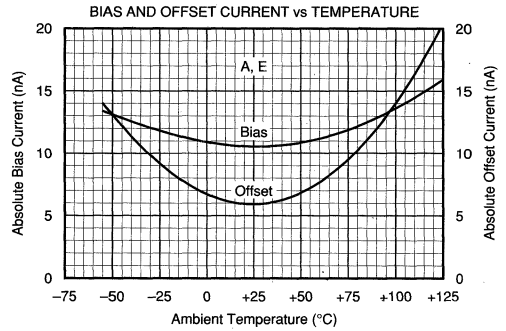
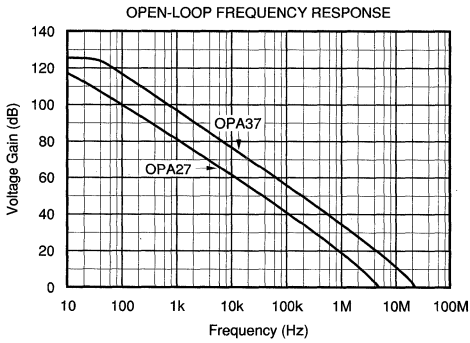
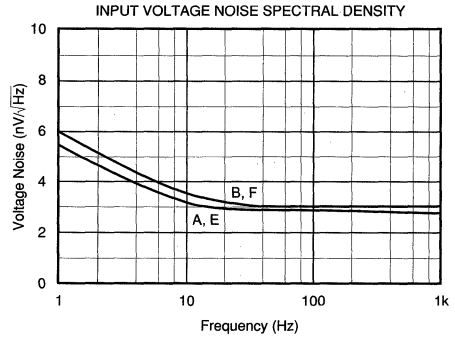
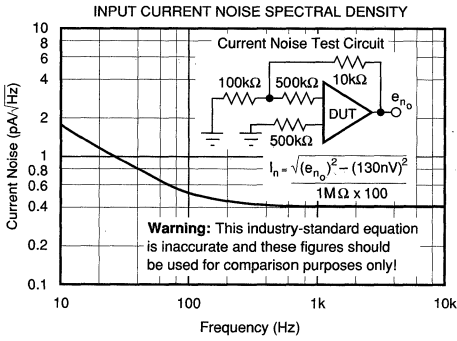
$T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

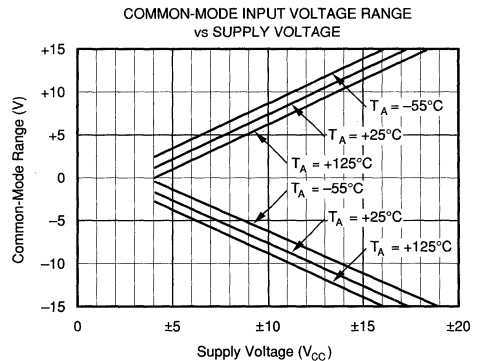
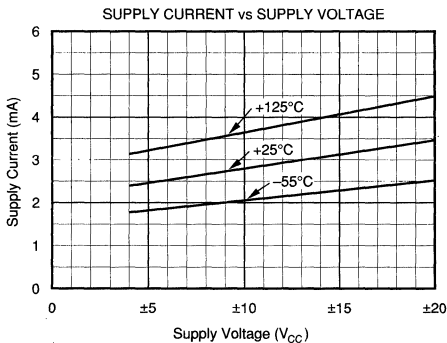
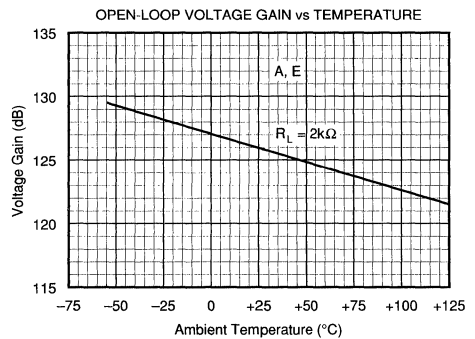
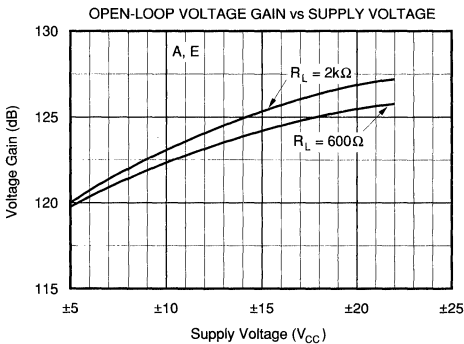
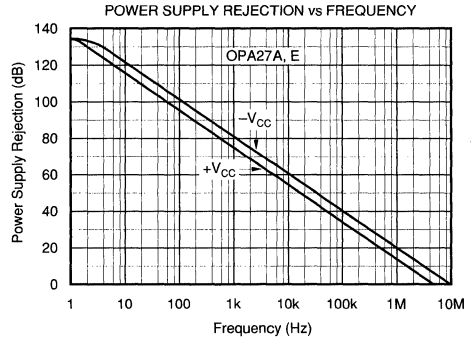
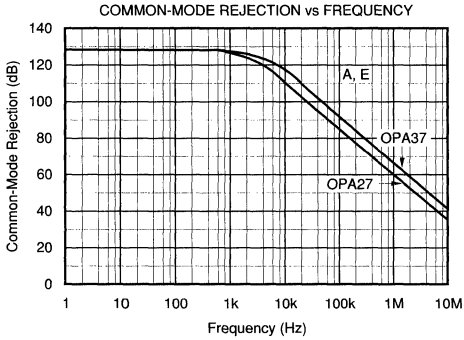
$T_A = +25^\circ\text{C}$, $\pm V_{OC} = \pm 15\text{VDC}$ unless otherwise noted.



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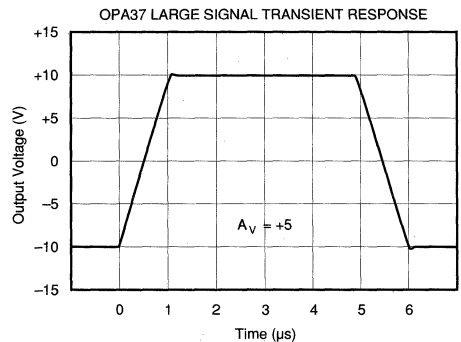
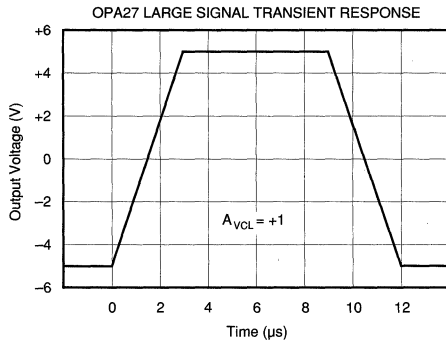
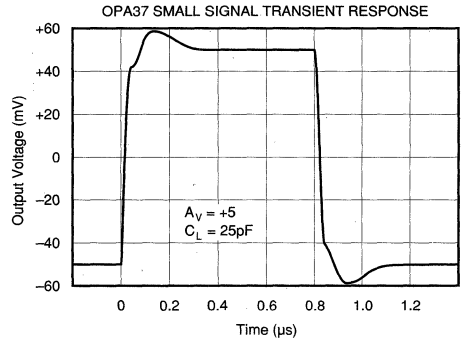
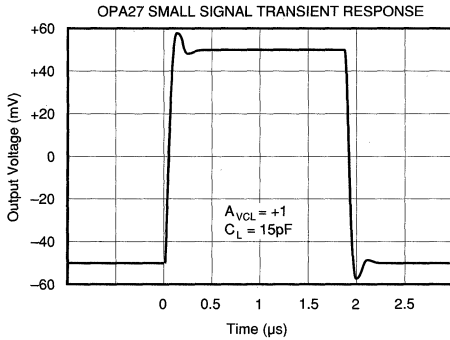
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA27/37 offset voltage is laser-trimmed and will require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a $10\text{k}\Omega$ trim potentiometer. Other potentiometer values from $1\text{k}\Omega$ to $1\text{M}\Omega$ can be used but V_{OS} drift will be degraded by an additional 0.1 to $0.2\mu\text{V}/^\circ\text{C}$. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately $3.3\mu\text{V}/^\circ\text{C}$ per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27/37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

THERMOELECTRIC POTENTIALS

The OPA27/37 is laser-trimmed to microvolt-level input offset voltage and for very low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference. See Figure 11.

Short, direct mounting of the OPA27/37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the Burr-Brown OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27 (see Figure 5).

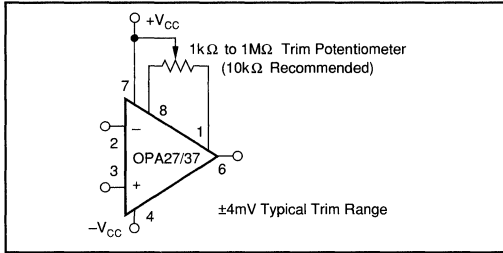


FIGURE 3. Offset Voltage Trim.

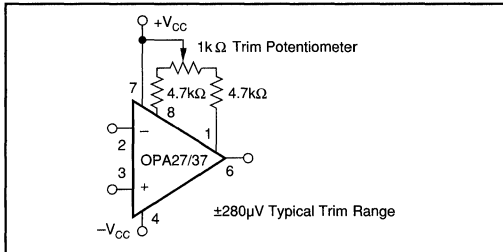


FIGURE 4. High Resolution Offset Voltage Trim.

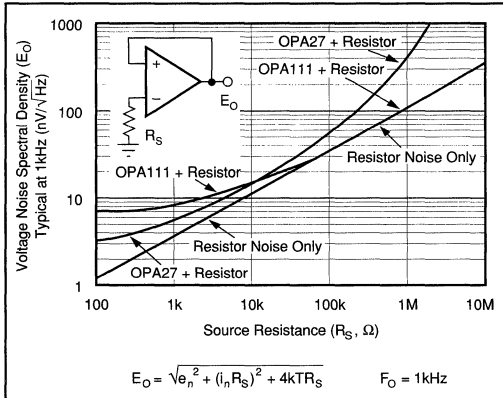


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor (R_f) which is greater than 2kΩ. This capacitor will compensate the pole generated by R_f and C_{in} and eliminate peaking or oscillation.

INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27/37. Exceeding a few hundred millivolts differential input signal will cause current to flow and without external current limiting resistors the input will be destroyed.

Accidental static discharge as well as high current can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OP-27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended (see Figure 6).

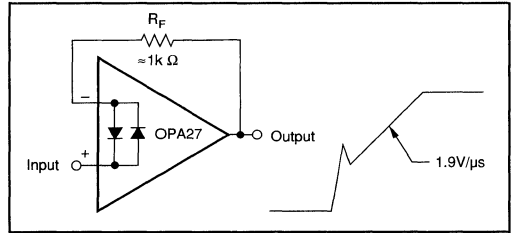


FIGURE 6. Pulsed Operation.

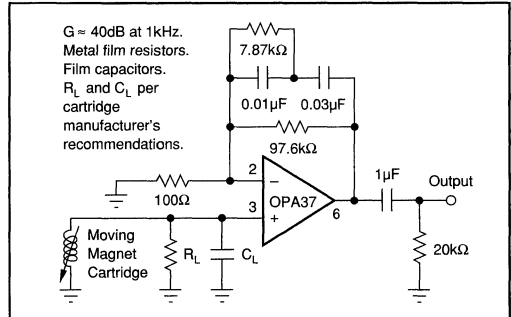


FIGURE 7. Low-Noise RIAA Preamplifier.

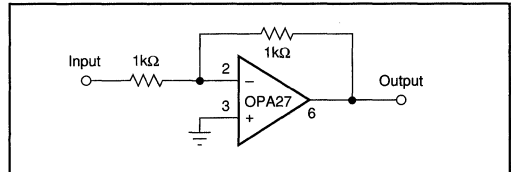


FIGURE 8. Unity-Gain Inverting Amplifier.

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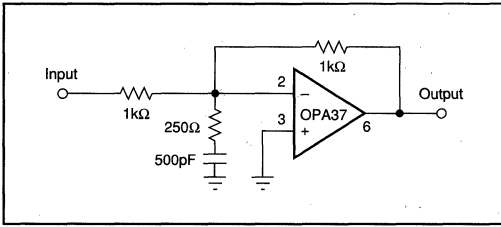


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

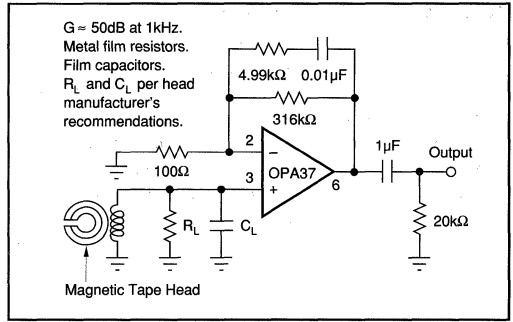


FIGURE 10. NAB Tape Head Preamplifier.

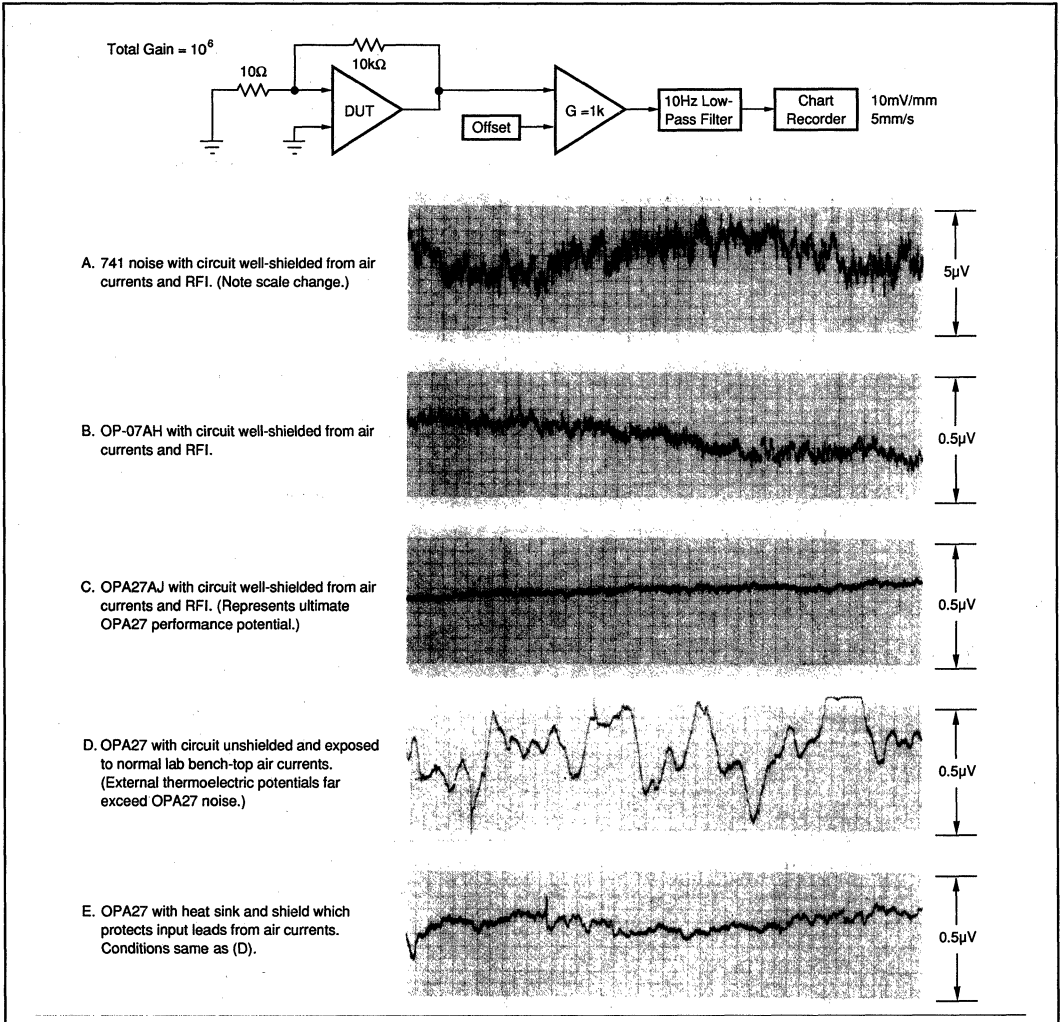


FIGURE 11. Low Frequency Noise Comparison.

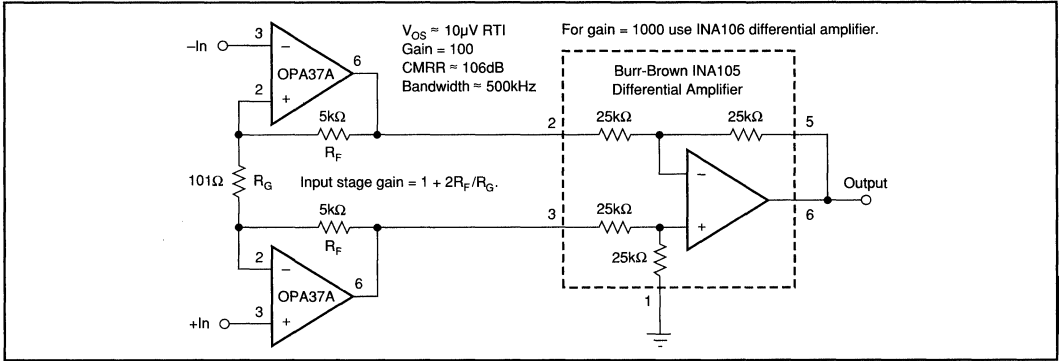


FIGURE 12. Low Noise Instrumentation Amplifier.

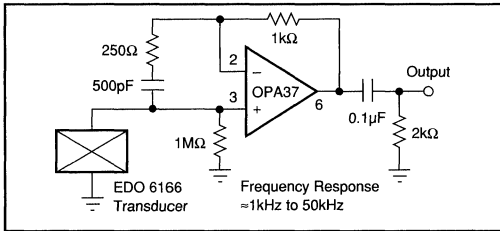


FIGURE 13. Hydrophone Preamplifier.

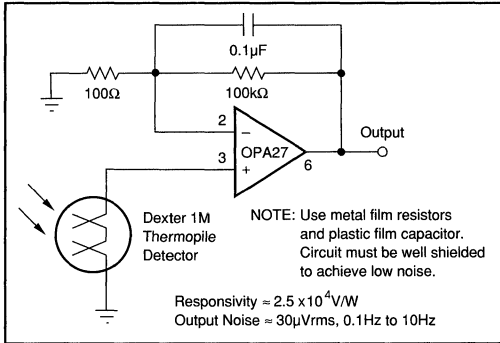


FIGURE 14. Long-Wavelength Infrared Detector Amplifier.

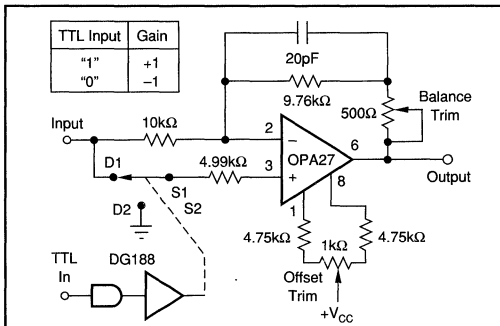


FIGURE 15. High Performance Synchronous Demodulator.

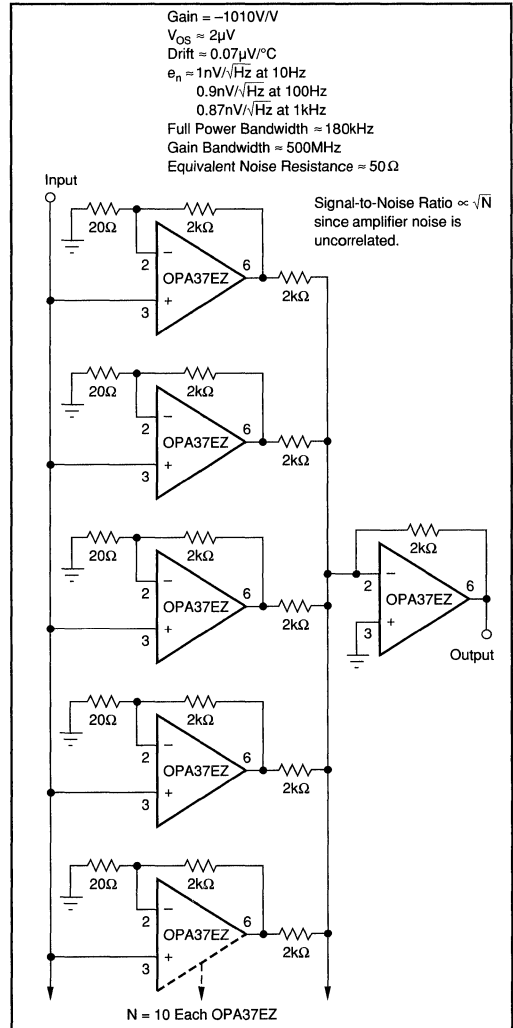


FIGURE 16. Ultra-Low Noise "N" Stage Parallel Amplifier.

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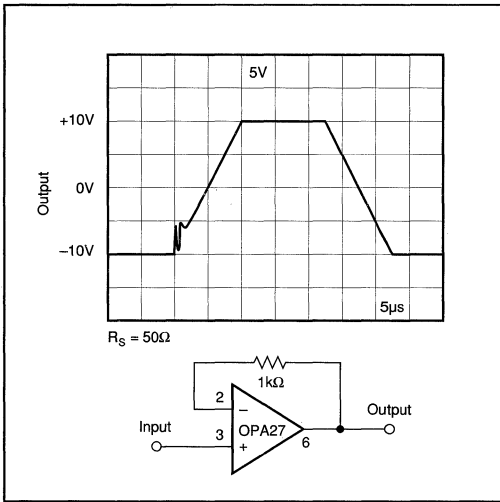


FIGURE 17. Unity-Gain Buffer.

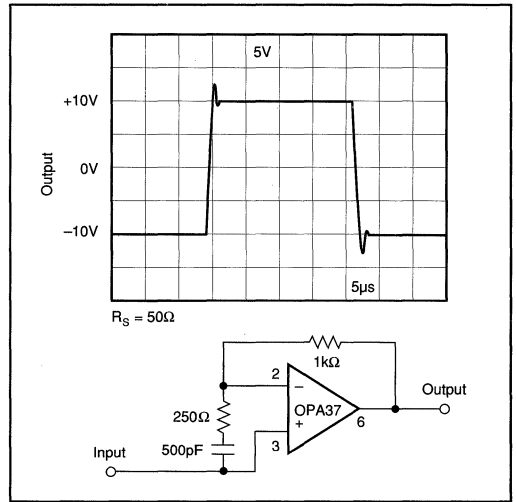


FIGURE 18. High Slew Rate Unity-Gain Buffer.

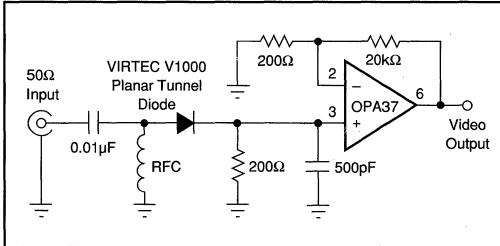


FIGURE 19. RF Detector and Video Amplifier.

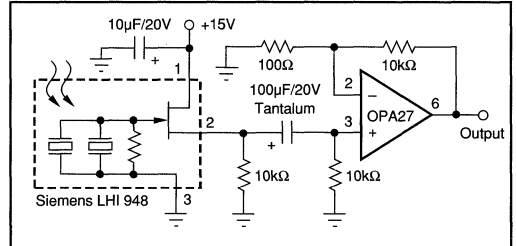


FIGURE 20. Balanced Pyroelectric Infrared Detector.

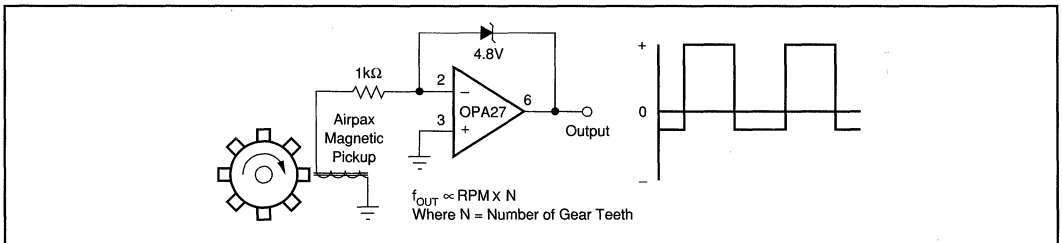
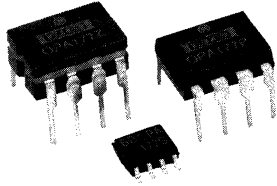


FIGURE 21. Magnetic Tachometer.

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OPA177
OPA77

OPA177/77

2

OPERATIONAL AMPLIFIERS

Precision OPERATIONAL AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 10 μ V max
- **LOW DRIFT:** 0.1 μ V/ $^{\circ}$ C
- **HIGH OPEN-LOOP GAIN:** 130dB min
- **LOW QUIESCENT CURRENT:** 1.5mA typ
- **REPLACES INDUSTRY-STANDARD OP AMPS:** OP-07, OP-77, OP-177, AD707, ETC.

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **BRIDGE AMPLIFIER**
- **THERMOCOUPLE AMPLIFIER**

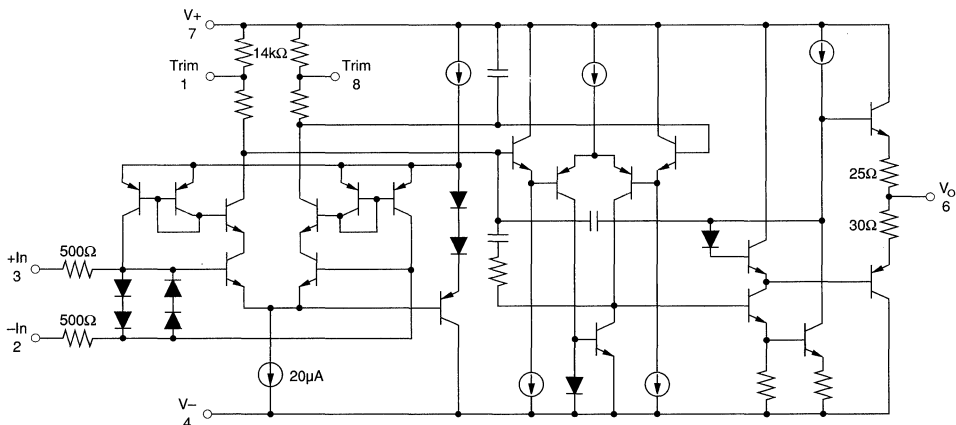
DESCRIPTION

The OPA177 and OPA77 precision bipolar op amps feature very low offset voltage and drift. Laser-trimmed offset, drift and input bias current virtually eliminate the need for costly external trimming. Their high performance and low cost make them ideally suited to a wide range of precision instrumentation.

The low quiescent current of the OPA177 and OPA77 dramatically reduce warm-up drift and errors due to

thermoelectric effects in input interconnections. They provide an effective alternative to chopper-stabilized amplifiers. The low noise of the OPA177 and OPA77 maintains accuracy.

OPA177 and OPA77 performance gradeouts are available. Packaging options include 8-pin plastic DIP, 8-pin ceramic DIP, and SO-8 surface-mount packages.



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OPA177 SPECIFICATIONS

ELECTRICAL

At $V_s = \pm 15V$, $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITION	OPA177E			OPA177F			OPA177G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Long-Term Input Offset ⁽¹⁾ Voltage Stability Offset Adjustment Range Power Supply Rejection Ratio			4	10		10	25		20	60	μV
			0.2			0.3		0.4			$\mu V/Mo$
		$R_p = 20k\Omega$		± 3		*	*	*	*	*	mV
		$V_s = \pm 3V$ to $\pm 18V$	120	125		115	*		110	120	dB
INPUT BIAS CURRENT Input Offset Current Input Bias Current			0.3	1		*	1.5		*	2.8	nA
			0.5	± 1.5		*	± 2		*	± 2.8	nA
NOISE Input Noise Voltage Input Noise Current	1Hz to 100Hz ⁽²⁾		85	150		*	*		*	*	nVrms
	1Hz to 100Hz		4.5			*	*		*	*	pArms
INPUT IMPEDANCE Input Resistance	Differential Mode ⁽³⁾	26	45		*	*		18.5	*		M Ω
	Common Mode		200		*	*			*		G Ω
INPUT VOLTAGE RANGE Common-Mode Input Range ⁽⁴⁾ Common-Mode Rejection		± 13	± 14		*	*		*	*		V
	$V_{CM} = \pm 13V$	130	140		*	*		115	*		dB
OPEN-LOOP GAIN Large-Signal Voltage Gain	$R_L \geq 2k\Omega$				*	*					V/mV
	$V_o = \pm 10V$ ⁽⁵⁾	5000	12000		*	*		2000	6000		V/mV
OUTPUT Output Voltage Swing Open-Loop Output Resistance	$R_L \geq 10k\Omega$	± 13.5	± 14		*	*		*	*		V
	$R_L \geq 2k\Omega$	± 12.5	± 13		*	*		*	*		V
	$R_L \geq 1k\Omega$	± 12	± 12.5		*	*		*	*		V
			60		*	*		*	*		Ω
FREQUENCY RESPONSE Slew Rate Closed-Loop Bandwidth	$R_L \geq 2k\Omega$	0.1	0.3		*	*		*	*		V/ μs
	$G = +1$	0.4	0.6		*	*		*	*		MHz
POWER SUPPLY Power Consumption Supply Current	$V_s = \pm 15V$, No Load		40	60		*	*		*	*	mW
	$V_s = \pm 3V$, No Load		3.5	4.5		*	*		*	*	mW
	$V_s = \pm 15V$, No Load		1.3	2		*	*		*	*	mA

ELECTRICAL

At $V_s = \pm 15V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

OFFSET VOLTAGE Input Offset Voltage Average Input Offset Voltage Drift ⁽⁶⁾ Power Supply Rejection Ratio			10	20		15	40		20	100	μV
			0.03	0.1		0.1	0.3		0.7	1.2	$\mu V/^\circ C$
		$V_s = \pm 3V$ to $\pm 18V$	120	125		110	120		106	115	dB
INPUT BIAS CURRENT Input Offset Current Average Input Offset Current Drift ⁽⁷⁾ Input Bias Current Average Input Bias Current Drift ⁽⁷⁾			0.5	1.5		*	2.2		*	4.5	nA
			1.5	25		*	40		*	85	pA/ $^\circ C$
			0.5	± 4		*	*		*	± 6	nA
			8	25		*	40		15	60	pA/ $^\circ C$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection		± 13	± 13.5		*	*		*	*		V
	$V_{CM} = \pm 13V$	120	140		*	*		110	*		dB
OPEN-LOOP GAIN Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	2000	6000		*	*		1000	4000		V/mV
OUTPUT Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		*	*		*	*		V
POWER SUPPLY Power Consumption Supply Current	$V_s = \pm 15V$, No Load		60	75		*	*		*	*	mW
	$V_s = \pm 15V$, No Load		2	2.5		*	*		*	*	mA

* Same as specification for product to left.

NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{os} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically less than $2\mu V$. (2) Sample tested. (3) Guaranteed by design. (4) Guaranteed by CMRR test condition. (5) To insure high open-loop gain throughout the $\pm 10V$ output range, A_{OL} is tested at $-10V \leq V_o \leq 0V$, $0V \leq V_o \leq +10V$, and $-10V \leq V_o \leq +10V$. (6) OP177EZ and OP177FZ: TCV_{os} is 100% tested. (7) Guaranteed by end-point limits.

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OPA77 SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 15V$, $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITION	OPA77E			OPA77F			OPA77G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE											
Input Offset Voltage			10	25		20	60		50	100	μV
Long-Term Input Offset Voltage Stability ⁽¹⁾			0.3			0.4			*		$\mu V/Mo$
Offset Adjustment Range	$R_{TRM} = 20k\Omega$		± 3			*			*		mV
Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		0.7	3		*	*		*	*	$\mu V/V$
INPUT BIAS CURRENT											
Input Offset Current			0.3	1.5		*	2.8		*	*	nA
Input Bias Current			1.2	± 2		*	± 2.8		*	*	nA
NOISE											
Input Noise Voltage	0.1Hz to 10Hz ⁽²⁾		0.35	0.6		0.38	0.65		*	*	$\mu V\sqrt{p}$
Input Noise Voltage Density	$f = 10Hz^{(2)}$		8.5	18		*	20		*	*	nV/ \sqrt{Hz}
	$f = 100Hz^{(2)}$		7.5	13		*	13.5		*	*	nV/ \sqrt{Hz}
	$f = 1000Hz^{(2)}$		7.5	11		*	11.5		*	*	nV/ \sqrt{Hz}
Input Noise Current	0.1Hz to 10Hz		35			*			*	*	pA \sqrt{p}
Input Noise Current Density	$f = 10Hz$		0.73			*			*	*	pA/ \sqrt{Hz}
	$f = 100Hz$		0.26			*			*	*	pA/ \sqrt{Hz}
	$f = 1000Hz$		0.22			*			*	*	pA/ \sqrt{Hz}
INPUT RESISTANCE											
Differential Input Resistance ⁽³⁾		26	45		18.5	*		*	*	*	M Ω
Common-mode Input Resistance			200			*		*	*	*	G Ω
INPUT VOLTAGE RANGE											
Common Mode Input Range		± 13	± 14		*	*		*	*	*	V
Common-Mode Rejection	$V_{CM} = \pm 13V$		0.1	1		*	1.6		*	*	$\mu V/V$
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000		2000	6000		*	*	*	V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 10k\Omega$	± 13.5	± 14		*	*		*	*	*	V
	$R_L \geq 2k\Omega$	± 12.5	± 13		*	*		*	*	*	V
	$R_L \geq 1k\Omega$	± 12	± 12.5		*	*		*	*	*	V
Open-Loop Output Resistance			60			*			*	*	Ω
FREQUENCY RESPONSE											
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		*	*		*	*	*	V/ μs
Closed-Loop Bandwidth	AVCL = +1	0.4	0.6		*	*		*	*	*	MHz
POWER SUPPLY											
Power Consumption	$V_S = \pm 15V$, No Load		50	60		*	*		*	*	mW
	$V_S = \pm 3V$, No Load		3.5	4.5		*	*		*	*	mW

ELECTRICAL

At $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OPA77EZ and OPA77FZ, $0^\circ C \leq T_A \leq +70^\circ C$ for OPA77FP and OPA77GP, unless otherwise noted.

OFFSET VOLTAGE											
Input Offset Voltage	Z Package		10	45		20	100		*	*	μV
	P Package		10	55		20	100		80	150	μV
Average Input Offset ⁽⁴⁾	Z Package		0.1	0.3		0.2	0.6		*	*	$\mu V/^\circ C$
Voltage Drift	P Package		0.3	0.6		0.4	1		0.7	1.2	$\mu V/^\circ C$
Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		1	3		*	5		*	*	$\mu V/V$
INPUT BIAS CURRENT											
Input Offset Current			0.5	2.2		*	4.5		*	*	nA
Avg Input Offset Current Drift ⁽⁵⁾			1.5	40		*	85		*	*	pA/ $^\circ C$
Input Bias Current			2.4	± 4		*	± 6		*	*	nA
Avg Input Bias Current Drift ⁽⁵⁾			8	40		15	60		*	*	pA/ $^\circ C$
INPUT VOLTAGE RANGE											
Common Mode Input Range		± 13	± 13.5		*	*		*	*	*	V
Common-Mode Rejection	$V_{CM} = \pm 13V$		0.1	1		*	3		*	*	$\mu V/V$
OPEN-LOOP GAIN											
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000		1000	4000		*	*	*	V/mV
OUTPUT											
Output Voltage Swing	$R_L \geq 2k\Omega$	± 12	± 13		*	*		*	*	*	V
POWER SUPPLY											
Power Consumption	$V_S = \pm 15V$, No Load		60	75		*	*		*	*	mW

* Same as specification for product to left. NOTES: (1) Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended period after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. (2) Sample tested. (3) Guaranteed by design. (4) OPA77E: TCV_{OS} is 100% tested on Z package. (5) Guaranteed by end-point limits.

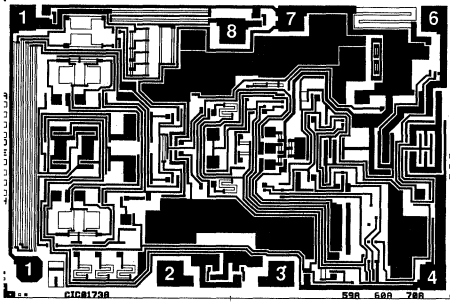
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DICE INFORMATION



OPA177/77 DIE TOPOGRAPHY

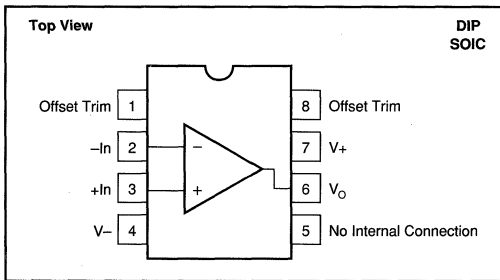
PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	V-
5	NC
6	V _O
7	V+
8	Offset Trim

Substrate Bias: $-V_S$
 NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 92 ± 5	1.60 x 2.34 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	46	
Backing	Gold	

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	±V _S
Output Short Circuit	Continuous
Operating Temperature:	
Ceramic DIP (Z)	-55°C to +125°C
Plastic DIP (P), SO-8 (S)	-40°C to +85°C
θ _{JA} (PDIP)	100°C/W
θ _{JA} (SOIC)	160°C/W
θ _{JA} (Ceramic)	148°C/W
Storage Temperature:	
Ceramic DIP (Z)	-65°C to +150°C
Plastic DIP (P), SO-8 (S)	-65°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) P, Z packages	+300°C
(soldering, 3s) S package	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA177FP	8-Pin Plastic DIP	-40°C to +85°C
OPA177GP	8-Pin Plastic DIP	-40°C to +85°C
OPA177GS	SO-8 Surface-Mount	-40°C to +85°C
OPA177EZ	8-Pin Ceramic DIP	-40°C to +85°C
OPA177FZ	8-Pin Ceramic DIP	-40°C to +85°C
OPA177GZ	8-Pin Ceramic DIP	-40°C to +85°C
OPA77FP	8-Pin Plastic DIP	0°C to +70°C
OPA77GP	8-Pin Plastic DIP	0°C to +70°C
OPA77EZ	8-Pin Ceramic DIP	-25°C to +85°C
OPA77FZ	8-Pin Ceramic DIP	-25°C to +85°C

PACKAGE INFORMATION⁽¹⁾

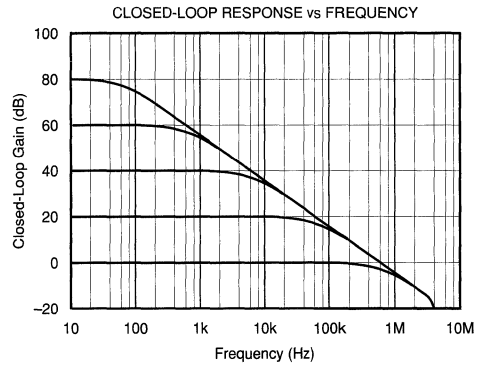
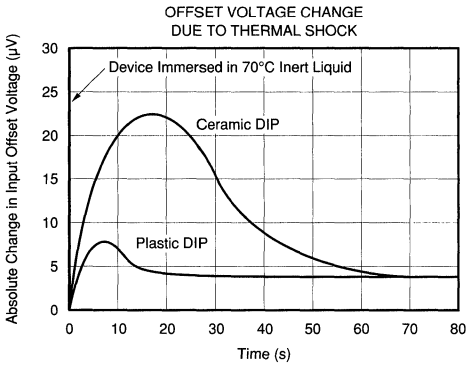
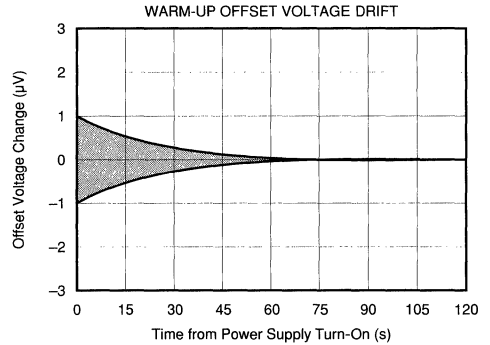
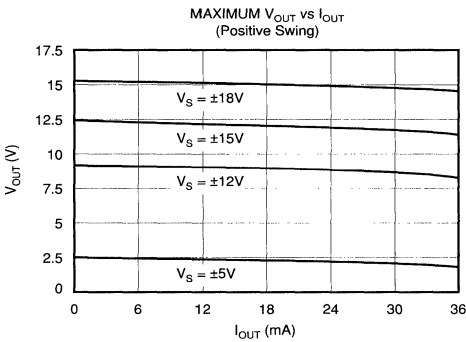
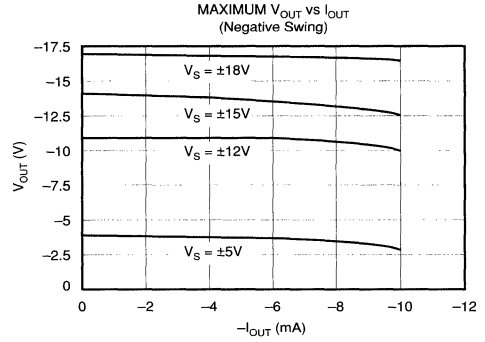
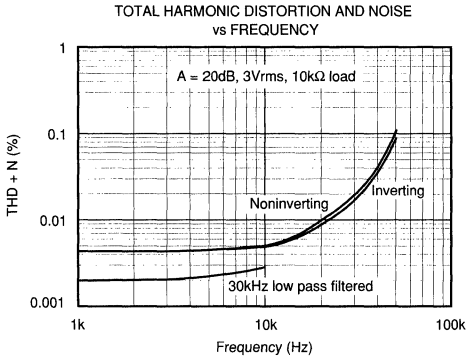
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA177FP	8-Pin Plastic DIP	006
OPA177GP	8-Pin Plastic DIP	006
OPA177GS	SO-8 Surface-Mount	182
OPA177EZ	8-Pin Ceramic DIP	254
OPA177FZ	8-Pin Ceramic DIP	254
OPA177GZ	8-Pin Ceramic DIP	254
OPA77FP	8-Pin Plastic DIP	006
OPA77GP	8-Pin Plastic DIP	006
OPA77EZ	8-Pin Ceramic DIP	254
OPA77FZ	8-Pin Ceramic DIP	254

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



OPA177/77

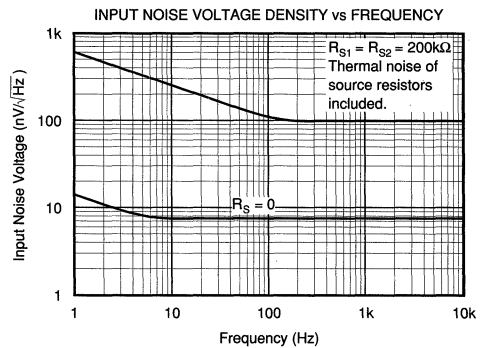
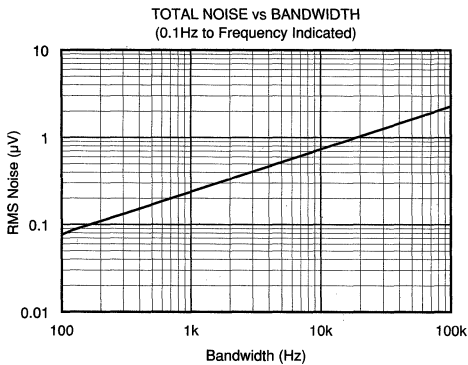
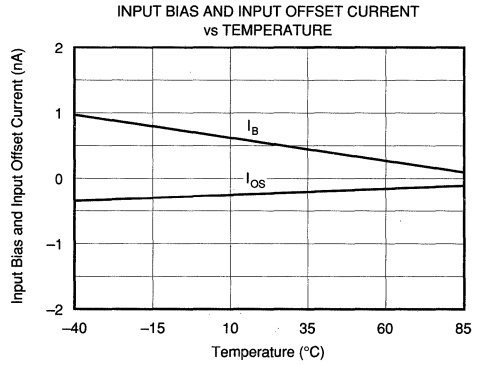
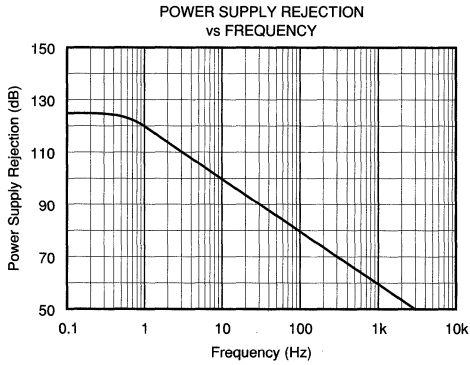
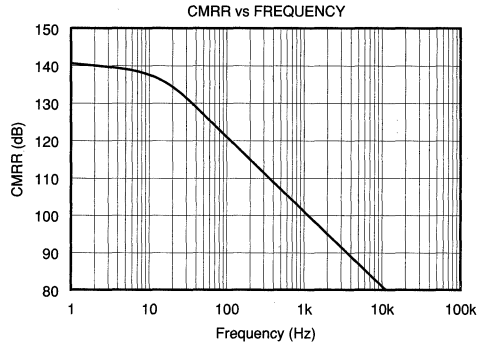
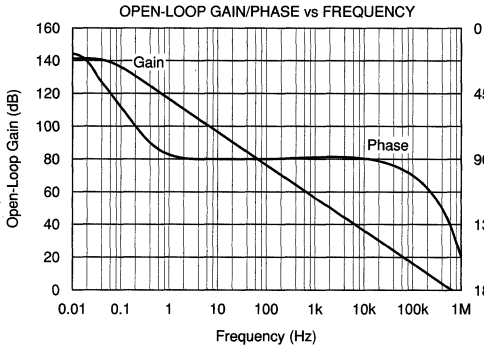
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OPERATIONAL AMPLIFIERS

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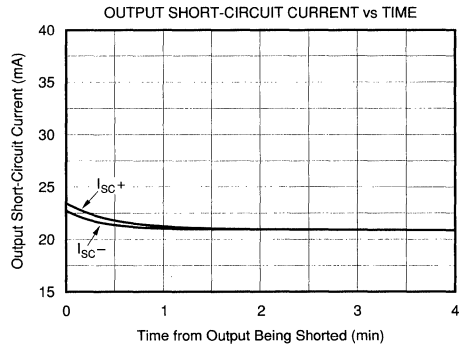
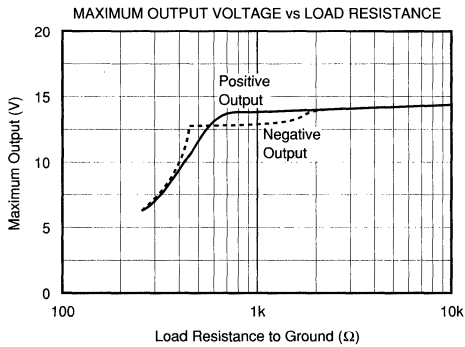
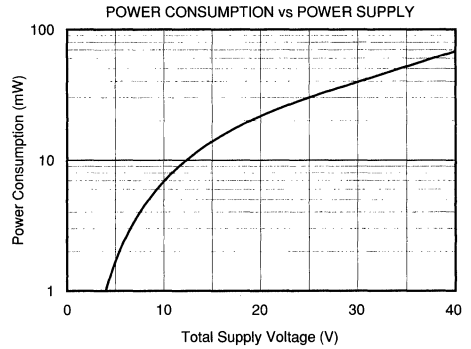
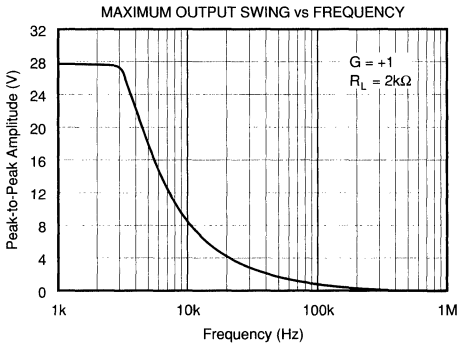
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5k Ω) applied to each pin.

Failure to observe proper handling procedures could result in small changes to the OPA177's input bias current.

APPLICATIONS INFORMATION

The OPA177 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 0.1 μ F ceramic capacitors are adequate.

The OPA177 has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions must be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can mask the ultimate performance of the OPA177. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

1. Keep connections made to the two input terminals close together.
2. Locate heat sources as far as possible from the critical input circuitry.
3. Shield the op amp and input circuitry from air currents such as cooling fans.

OFFSET VOLTAGE ADJUSTMENT

The OPA177 and OPA77 have been laser-trimmed for low offset voltage and drift so most circuits will not require external adjustment. Figure 1 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce excessive temperature drift.

INPUT PROTECTION

The inputs of the OPA177 and OPA77 are protected with 500 Ω series input resistors and diode clamps as shown in the simplified circuit diagram. The inputs can withstand \pm 30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

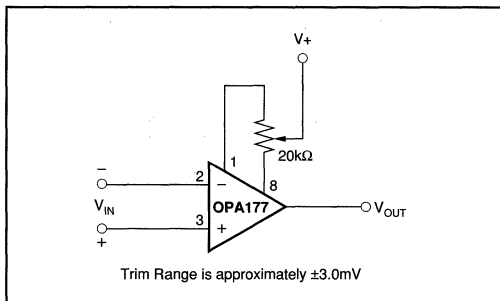


FIGURE 1. Optional Offset Nulling Circuit.

NOISE PERFORMANCE

The noise performance of the OPA177 and OPA77 is optimized for circuit impedances in the range of 2k Ω to 50k Ω . Total noise in an application is a combination of the op amp's input voltage noise and input bias current noise reacting with circuit impedances. For applications with higher source impedance, the OPA627 FET-input op amp will generally provide lower noise. For very low impedance applications, the OPA27 will provide lower noise.

INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA177 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to balance the DC resistance seen at the two input terminals (Figure 2). A resistor added to balance the input resistances may actually increase offset and noise.

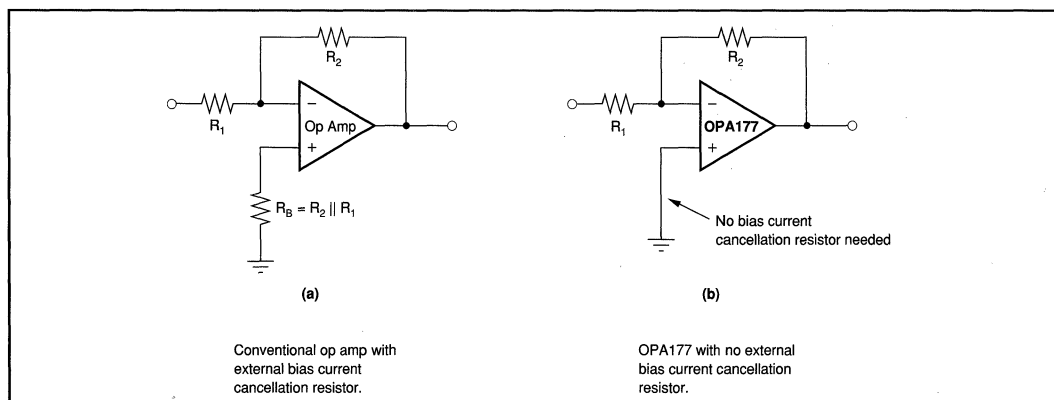
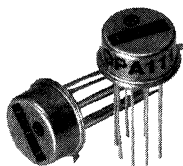


FIGURE 2. Input Bias Current Cancellation.

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OPA111

OPA111

2

OPERATIONAL AMPLIFIERS

Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** 100% Tested, $8nV\sqrt{Hz}$ max (10kHz)
- **LOW BIAS CURRENT:** 1pA max
- **LOW OFFSET:** 250 μ V max
- **LOW DRIFT:** 1 μ V/ $^{\circ}$ C max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH COMMON-MODE REJECTION:** 100dB min

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **OPTOELECTRONICS**
- **MEDICAL EQUIPMENT—CAT SCANNER**
- **RADIATION HARD EQUIPMENT**

DESCRIPTION

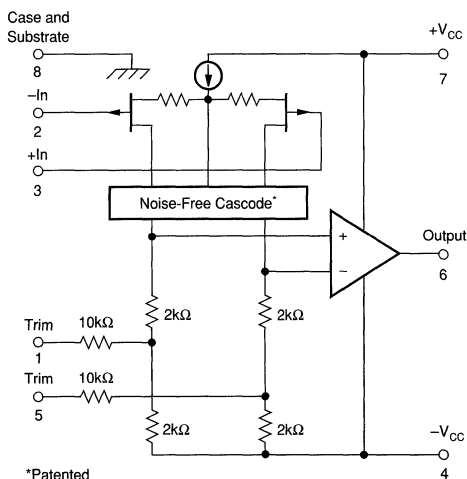
The OPA111 is a precision monolithic dielectrically isolated FET (*Difet*[®]) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



BIFET[®] National Semiconductor Corp., *Difet*[®] Burr-Brown Corp.

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PDS-526K

2.27

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
NOISE											
Voltage, $f_o = 10\text{Hz}$	100% Tested		40	80		30	60		40	80	$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 100\text{Hz}$	100% Tested		15	40		11	30		15	40	$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 1\text{kHz}$	100% Tested		8	15		7	12		8	15	$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 10\text{kHz}$	100% Tested		6	8		6	8		6	8	$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 10\text{Hz to } 10\text{kHz}$	100% Tested		0.7	1.2		0.6	1		0.7	1.2	μVrms
Current, $f_o = 0.1\text{Hz to } 10\text{Hz}$	(1)		1.6	3.3		1.2	2.5		1.6	3.3	$\mu\text{Vp-p}$
$f_o = 0.1\text{Hz to } 10\text{Hz}$	(1)		9.5	15		7.5	12		9.5	15	fA p-p
$f_o = 0.1\text{Hz thru } 20\text{kHz}$	(1)		0.5	0.8		0.4	0.6		0.5	0.8	$\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE(2)											
Input Offset Voltage	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}		± 100	± 500		± 50	± 250		± 100	± 500	μV
Average Drift			± 2	± 5		± 0.5	± 1		± 2	± 5	$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_{CC} = \pm 10\text{V to } \pm 18\text{V}$	90	110	± 31	100	110	± 10	90	110	± 31	dB $\mu\text{V/V}$
BIAS CURRENT(2)											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 0.8	± 2		± 0.5	± 1		± 0.8	± 2	pA
OFFSET CURRENT(2)											
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 0.5	± 1.5		± 0.25	± 0.75		± 0.5	± 1.5	pA
IMPEDANCE											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE											
Common-Mode Input Range		± 10	± 11		± 10	± 11		± 10	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	90	110		100	110		90	110		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	114	125		120	125		114	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			2			2					MHz
Full Power Response	20Vp-p , $R_L = 2\text{k}\Omega$	16	32		16	32		16	32		kHz
Slew Rate	$V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	1	2		1	2		1	2		$\text{V}/\mu\text{s}$
Settling Time, 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		6			6			6		μs
0.01%	10V Step		10			10			10		μs
Overload Recovery, 50% Overdrive(3)	Gain = -1		5			5			5		μs
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$	± 11	± 12		± 11	± 12		± 11	± 12		V
Current Output	$V_o = \pm 10\text{VDC}$	± 5.5	± 10		± 5.5	± 10		± 5.5	± 10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			± 15			± 15			± 15		VDC
Voltage Range, Derated Performance		± 5		± 18	± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_o = 0\text{mADC}$		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	Ambient Temp.	-25		+85	-25		+85	-55		+125	$^\circ\text{C}$
Operating	Ambient Temp.	-55		+125	-55		+125	-55		+125	$^\circ\text{C}$
Storage	Ambient Temp.	-65		+150	-65		+150	-65		+150	$^\circ\text{C}$
$\theta_{\text{Junction-Ambient}}$			200			200			200		$^\circ\text{C}/\text{W}$

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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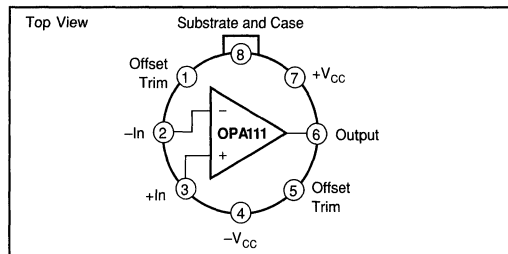
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA111AM			OPA111BM			OPA111SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range	Ambient Temp.	-25		+85	-25		+85	-55		+125	°C
INPUT											
OFFSET VOLTAGE⁽¹⁾											
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		± 220	± 1000		± 110	± 500		± 300	± 1500	μV
Average Drift			± 2	± 5		± 0.5	± 1		± 2	± 5	$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$	86	100	± 10	90	100	± 10	± 32	86	100	$\mu\text{V}/\text{V}$
BIAS CURRENT⁽¹⁾											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 50	± 250		± 30	± 130		± 820	± 4100	pA
OFFSET CURRENT⁽¹⁾											
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 30	± 200		± 15	± 100		± 510	± 3100	pA
VOLTAGE RANGE											
Common-Mode Input Range		± 10	± 11		± 10	± 11		± 10	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	86	100		90	100		86	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	110	120		114	120		110	120		dB
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$	± 10.5	± 11		± 11	± 11.5		± 11	± 11.5		V
Current Output	$V_O = \pm 10\text{VDC}$	± 5.25	± 10		± 5.25	± 10		± 5.25	± 10		mA
Short Circuit Current	$V_O = 0\text{VDC}$	10	40		10	40		10	40		mA
POWER SUPPLY											
Current, Quiescent	$I_O = 0\text{mADC}$		2.5	3.5		2.5	3.5		2.5	3.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ⁽¹⁾	750mW
Differential Input Voltage ⁽²⁾	$\pm 36\text{VDC}$
Input Voltage Range ⁽²⁾	$\pm 18\text{VDC}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short Circuit Duration ⁽³⁾	Continuous
Junction Temperature	$+175^\circ\text{C}$

NOTES: (1) Packages must be derated based on $\theta_{JC} = 150^\circ\text{C}/\text{W}$ or $\theta_{JA} = 300^\circ\text{C}/\text{W}$. (2) For supply voltages less than $\pm 18\text{VDC}$, the absolute maximum input voltage is equal to $+18\text{V} > V_{IN} > -V_{CC} - 6\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to $+25^\circ\text{C}$ ambient. Observe dissipation limit and T_J .

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA111AM	TO-99	001
OPA111BM	TO-99	001
OPA111SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

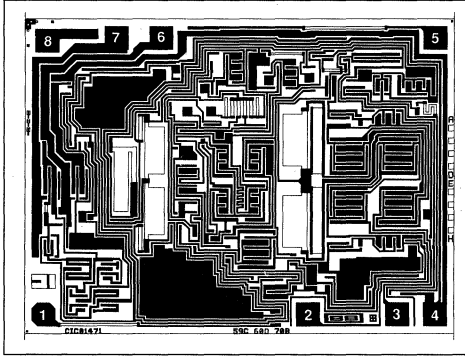
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, MAX (μV)
OPA111AM	TO-99	-25°C to $+85^\circ\text{C}$	± 500
OPA111BM	TO-99	-25°C to $+85^\circ\text{C}$	± 250
OPA111SM	TO-99	-55°C to $+125^\circ\text{C}$	± 500



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DICE INFORMATION



OPA111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _s
5	Offset Trim
6	Output
7	+V _s
8	Substrate

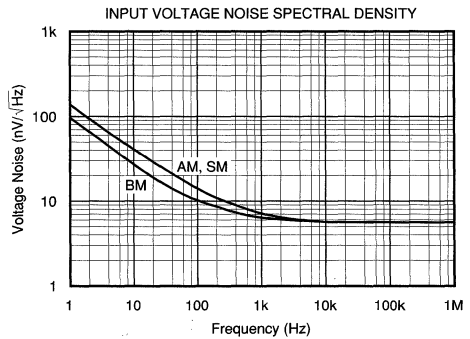
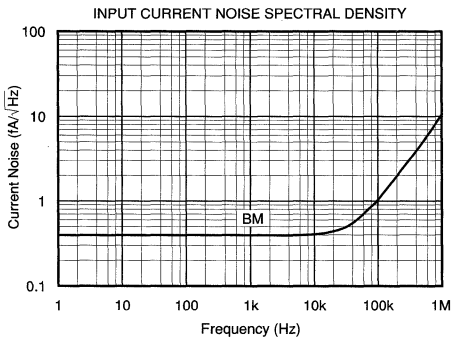
Substrate Bias: This Dielectrically-Isolated Substrate is normally connected to common.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	95 x 71 ±5	2.41 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:		None
Transistor Count:		44

TYPICAL PERFORMANCE CURVES

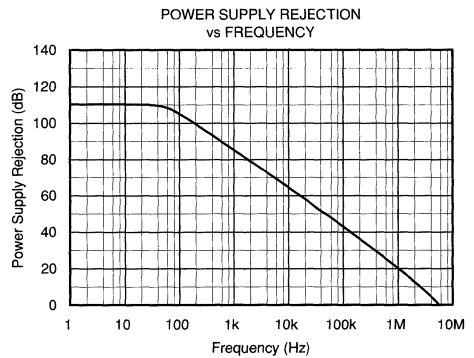
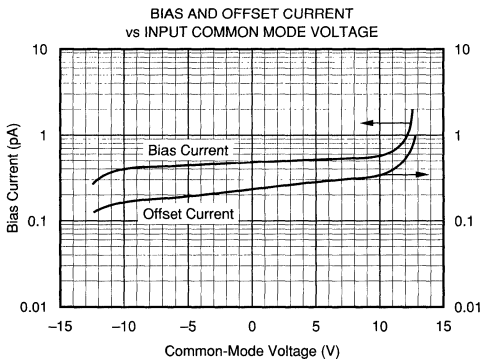
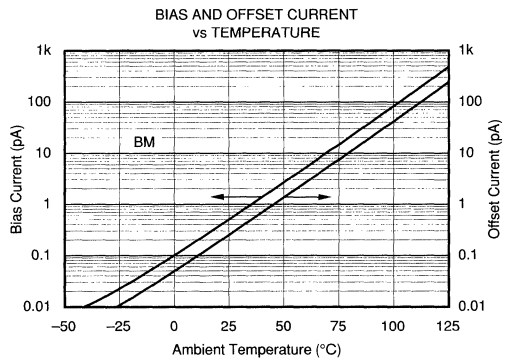
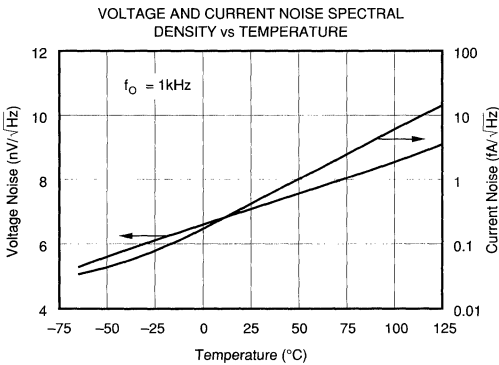
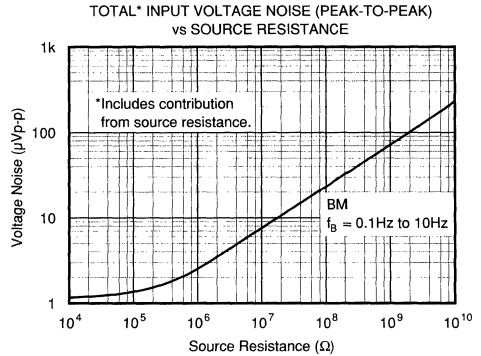
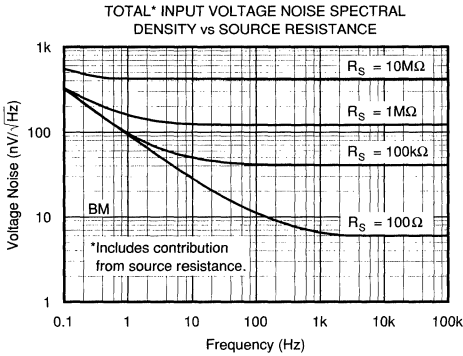
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

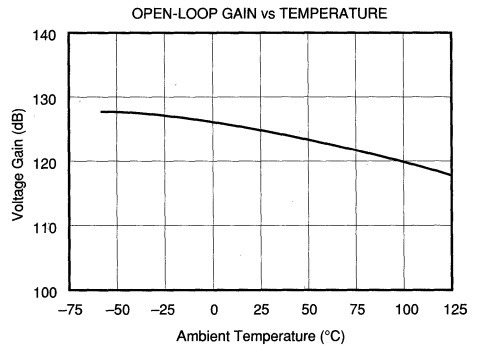
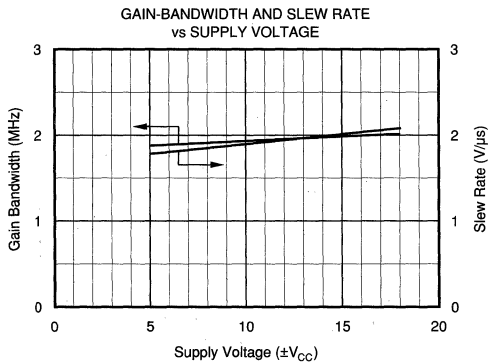
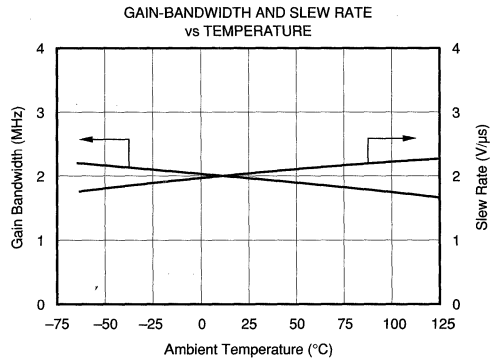
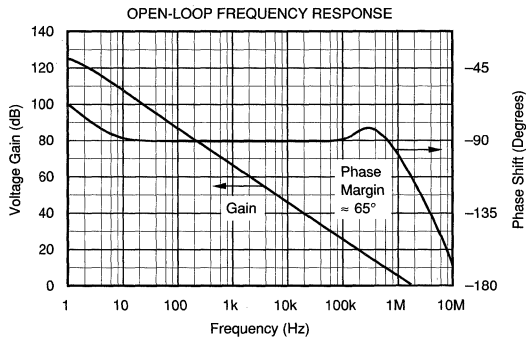
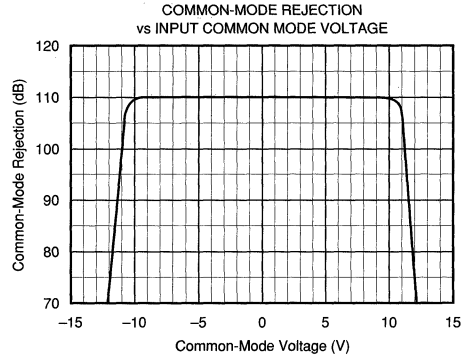
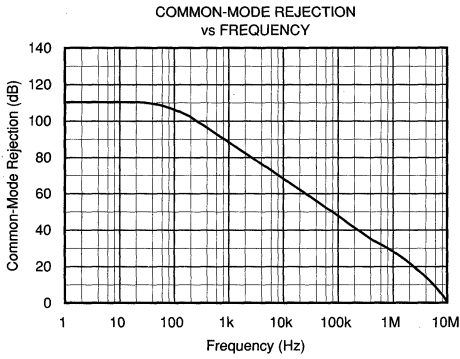
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

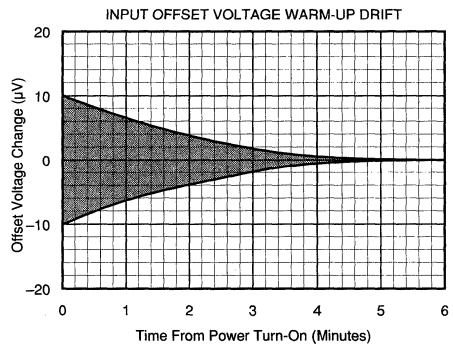
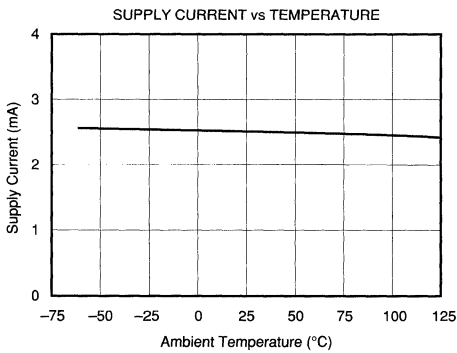
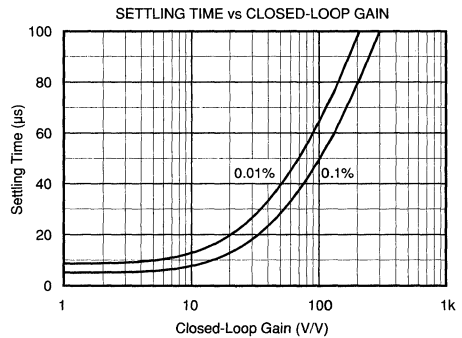
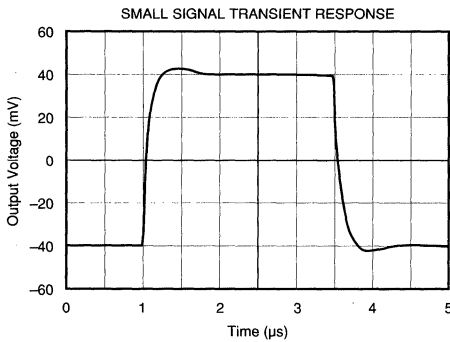
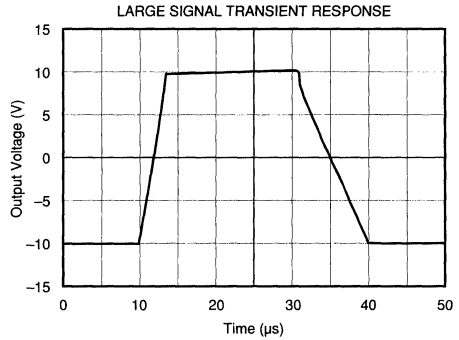
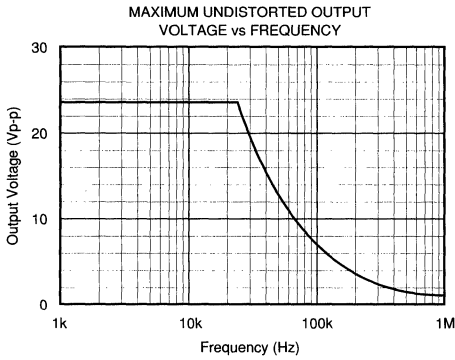
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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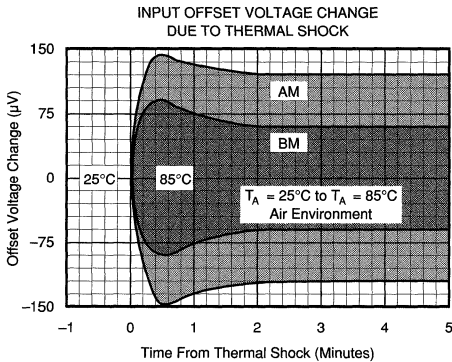
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA111 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA111 can replace most other amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

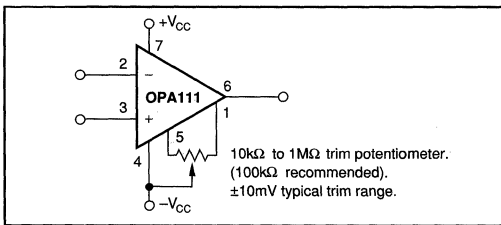


FIGURE 1. Offset Voltage Trim.

Unlike BIFET amplifiers, The *Difet* OPA111 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A 10k Ω series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels, even if both supply voltages are lost.

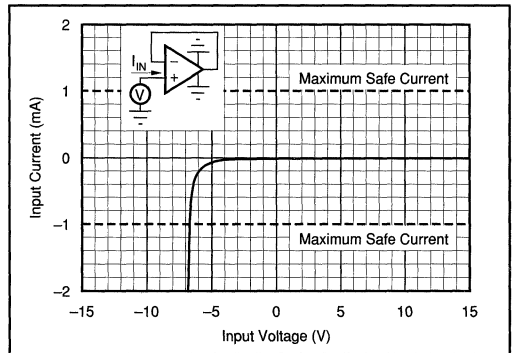


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA111. To avoid leakage problems, it is recommended that the signal input lead of the OPA111 be wired to a Teflon standoff. If the OPA111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern

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should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 (case) should be connected to ground.

NOISE: FET VERSUS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall

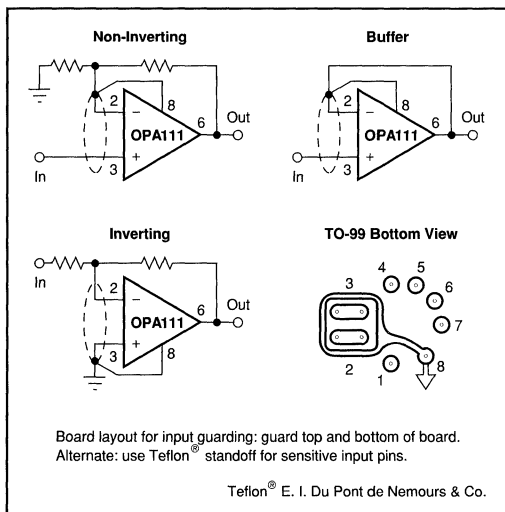


FIGURE 3. Connection of Input Guard.

operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15k Ω , the OPA111 will have a lower total noise than an OP-27 (see Figure 4).

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias current of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 5). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA111 is not compromised by common-mode voltage.

APPLICATIONS CIRCUITS

Figures 6 through 18 are circuit diagrams of various applications for the OPA111.

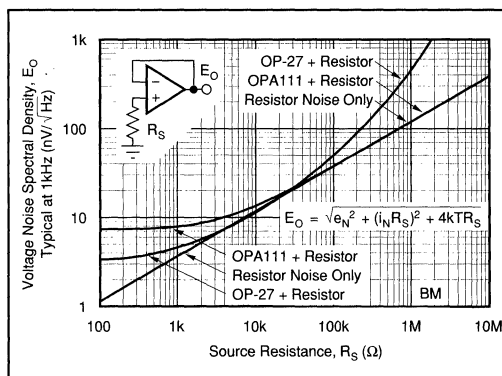


FIGURE 4. Voltage Noise Spectral Density vs Source Resistance.

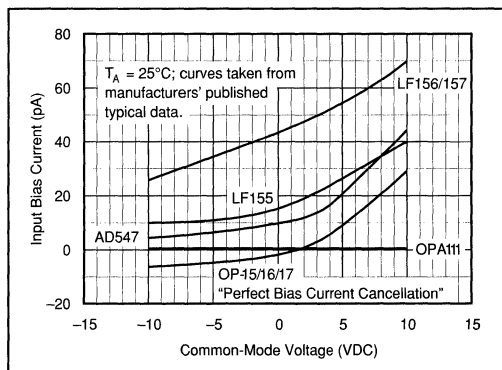


FIGURE 5. Input Bias Current vs Common-Mode Voltage.

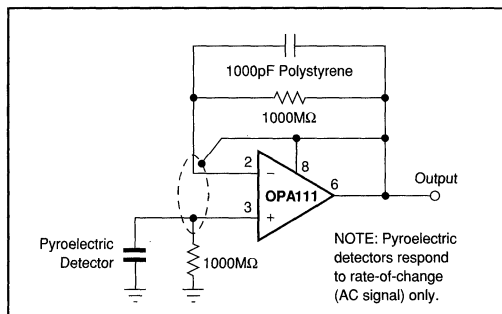


FIGURE 6. Pyroelectric Infrared Detector.

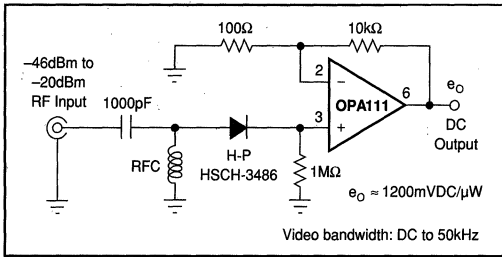


FIGURE 7. Zero-Bias Schottky Diode Square-Law RF Detector.

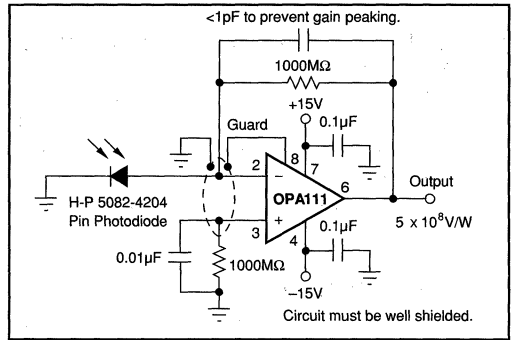


FIGURE 10. Sensitive Photodiode Amplifier.

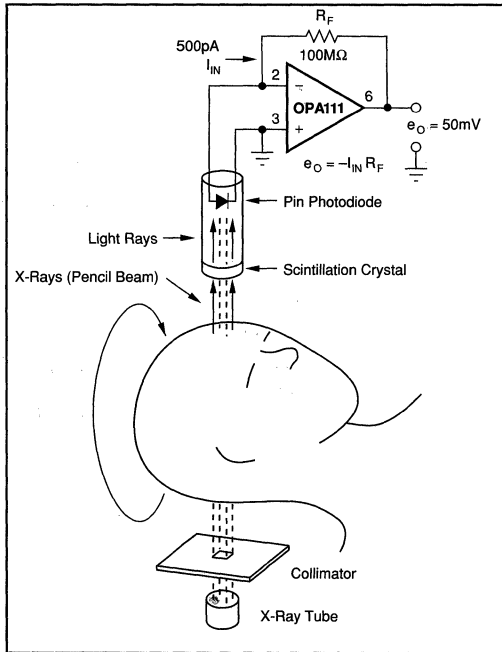


FIGURE 8. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

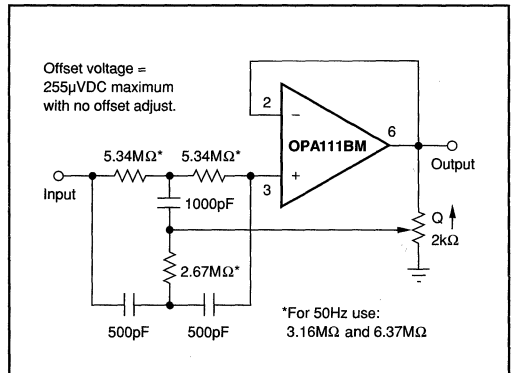


FIGURE 11. 60Hz Reject Filter.

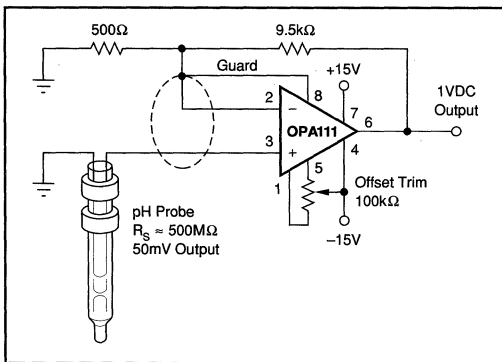


FIGURE 9. High Impedance ($10^{14}\Omega$) Amplifier.

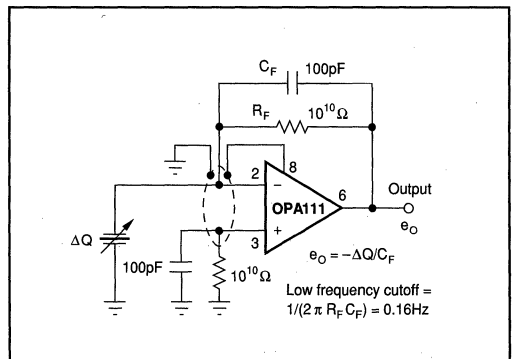


FIGURE 12. Piezoelectric Transducer Charge Amplifier.

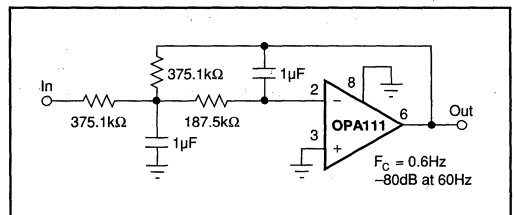


FIGURE 13. 0.6Hz Second Order Low-Pass Filter.

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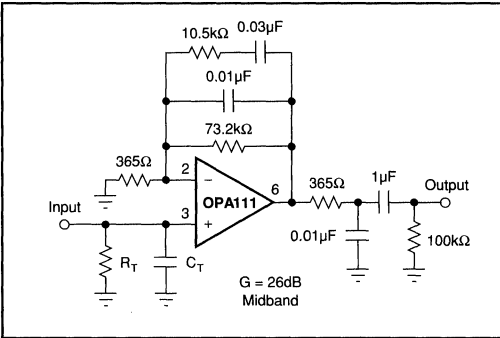


FIGURE 14. RIAA Equalized Phono Preamp.

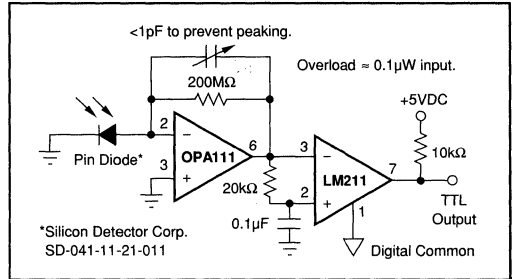


FIGURE 15. High Sensitivity (under 1nW) Fiber Optic Receiver for 9600 Baud Manchester Data.

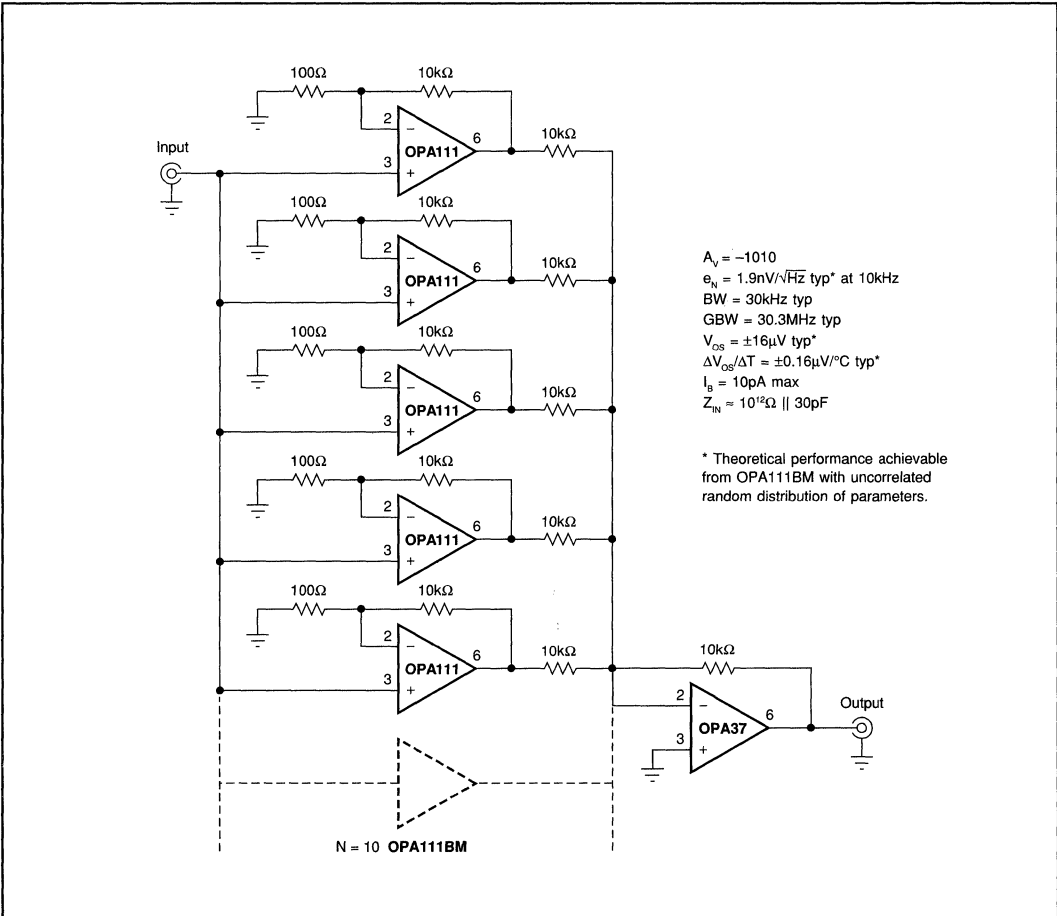


FIGURE 16. 'N' Stage Parallel-Input Amplifier for Reduced Relative Amplifier Noise at the Output.

OPA111

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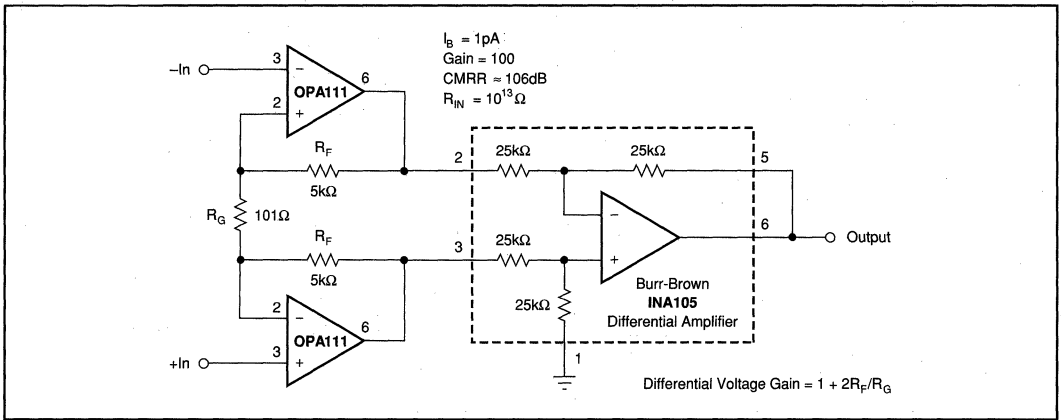


FIGURE 17. FET Input Instrumentation Amplifier.

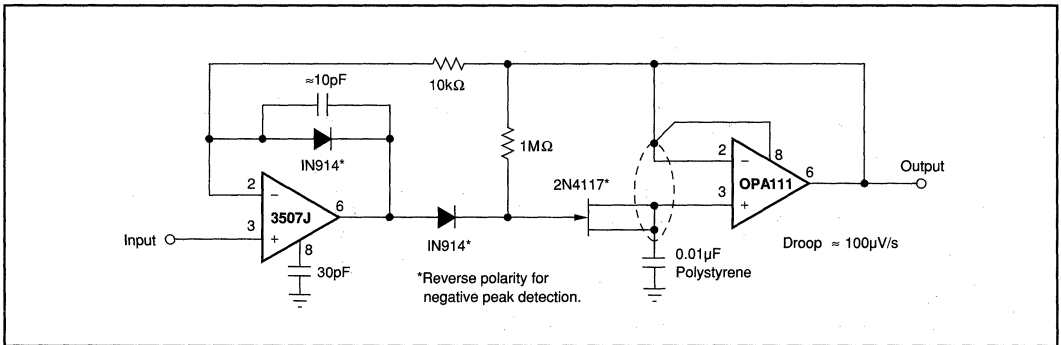
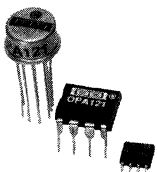


FIGURE 18. Low-Droop Positive Peak Detector.



OPA121

OPA121

2

OPERATIONAL AMPLIFIERS

Low Cost Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: $6\text{nV}/\sqrt{\text{Hz}}$ typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: $3\mu\text{V}/^\circ\text{C}$ typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*[®]) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

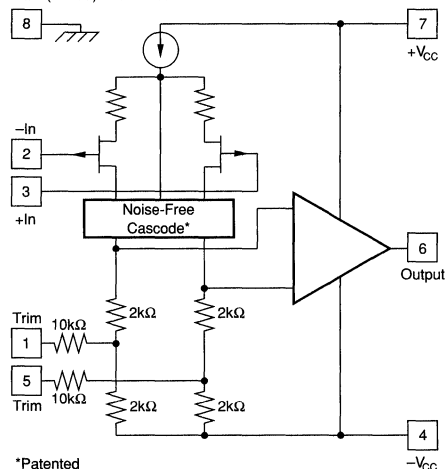
Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.

Case (TO-99) and Substrate



*Patented

OPA121 Simplified Circuit

Difet[®], Burr-Brown Corp.
BIFET[®], National Semiconductor Corp.



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE								
Voltage, $f_o = 10\text{Hz}$	(1)		40			50		nV/ $\sqrt{\text{Hz}}$
$f_o = 100\text{Hz}$	(1)		15			18		nV/ $\sqrt{\text{Hz}}$
$f_o = 1\text{kHz}$	(1)		8			10		nV/ $\sqrt{\text{Hz}}$
$f_o = 10\text{kHz}$	(1)		6			7		nV/ $\sqrt{\text{Hz}}$
$f_o = 10\text{Hz to } 10\text{kHz}$	(1)		0.7			0.8		μVrms
Current, $f_o = 0.1\text{Hz to } 10\text{Hz}$	(1)		1.6			2		$\mu\text{Vp-p}$
$f_o = 0.1\text{Hz to } 10\text{Hz}$	(1)		15			21		fA, p-p
$f_o = 0.1\text{Hz thru } 20\text{kHz}$	(1)		0.8			1.1		fA/ $\sqrt{\text{Hz}}$
OFFSET VOLTAGE (2)								
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		± 0.5	± 2		± 0.5	± 3	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 3	± 10		± 3	± 10	$\mu\text{V}/^\circ\text{C}$
Supply Rejection		86	104	± 50	86	104	± 50	dB
BIAS CURRENT (2)								
Input Bias Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 1	± 5		± 1	± 10	pA
OFFSET CURRENT (2)								
Input Offset Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 0.7	± 4		± 0.7	± 8	pA
IMPEDANCE								
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE								
Common-Mode Input Range		± 10	± 11		± 10	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	86	104		82	100		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	110	120		106	114		dB
FREQUENCY RESPONSE								
Unity Gain, Small Signal			2			2		MHz
Full Power Response	20Vp-p, $R_L = 2\text{k}\Omega$		32			32		kHz
Slew Rate	$V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$		2			2		V/ μs
Settling Time, 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		6			6		μs
0.01%	10V Step		10			10		μs
Overload Recovery, 50% Overdrive(3)	Gain = -1		5			5		μs
RATED OUTPUT								
Voltage Output	$R_L = 2\text{k}\Omega$	± 11	± 12		± 11	± 12		V
Current Output	$V_o = \pm 10\text{VDC}$	± 5.5	± 10		± 5.5	± 10		mA
Output Resistance	DC, Open Loop		100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000		pF
Short Circuit Current		10	40		10	40		mA
POWER SUPPLY								
Rated Voltage			± 15			± 15		VDC
Voltage Range, Derated Performance		± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_o = 0\text{mADC}$		2.5	4		2.5	4.5	mA
TEMPERATURE RANGE								
Specification	Ambient Temperature	0		+70	0		+70	$^\circ\text{C}$
Operating	Ambient Temperature	-40		+85	-25		+85	$^\circ\text{C}$
Storage	Ambient Temperature	-65		+150	-55		+125	$^\circ\text{C}$
θ Junction-Ambient			200			150(4)		$^\circ\text{C}/\text{W}$

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) 100 $^\circ\text{C}/\text{W}$ for KU grade.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15VDC$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temperature	0		+70	0		+70	°C
INPUT OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0VDC$		± 1 ± 3 82	± 3 ± 10 94 ± 20		± 1 ± 3 82 ± 20	± 5 ± 10 94 ± 80	mV $\mu V/^\circ C$ dB $\mu V/V$
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0VDC$ Device Operating		± 23	± 115		± 23	± 250	pA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0VDC$ Device Operating		± 16	± 100		± 16	± 200	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10VDC$	± 10 82	± 11 98		± 10 80	± 11 96		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	106	116		100	110		dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2k\Omega$ $V_O = \pm 10VDC$ $V_O = 0VDC$	± 10.5 ± 5.25 10	± 11 ± 10 40		± 10.5 ± 5.25 10	± 11 ± 10 40		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0mADC$		2.5	4.5		2.5	5	mA

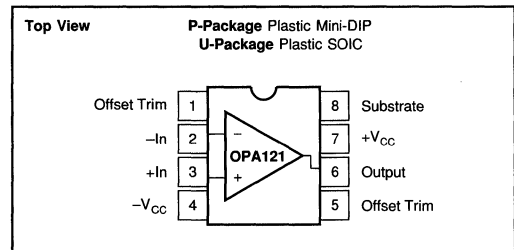
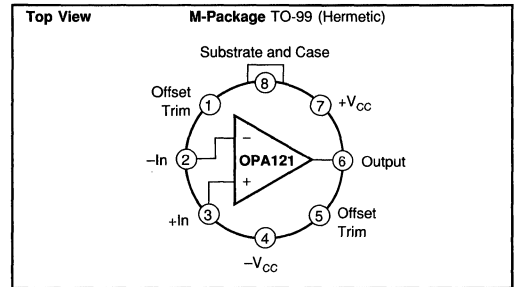
NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18VDC$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage	$\pm 36VDC$
Input Voltage Range	$\pm 18VDC$
Storage Temperature Range	
M package	$-65^\circ C$ to $+150^\circ C$
P, U packages	$-55^\circ C$ to $+125^\circ C$
Operating Temperature Range	
M package	$-40^\circ C$ to $+85^\circ C$
P, U packages	$-25^\circ C$ to $+85^\circ C$
Lead Temperature	
M, P packages (soldering, 10s)	$+300^\circ C$
U package (soldering, 3s)	$+260^\circ C$
Output Short-Circuit Duration ⁽²⁾	Continuous
Junction Temperature	$+175^\circ C$

NOTES: (1) Packages must be derated based on $\theta_{JA} = 150^\circ C/W$ (P package); $\theta_{JA} = 200^\circ C/W$ (M package); $\theta_{JA} = 100^\circ C/W$ (U package).
(2) Short circuit may be to power supply common only. Rating applies to $+25^\circ C$ ambient. Observe dissipation limit and T_{Jr} .

CONNECTION DIAGRAMS



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA121KM	TO-99	001
OPA121KP	8-Pin Plastic DIP	006
OPA121KU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

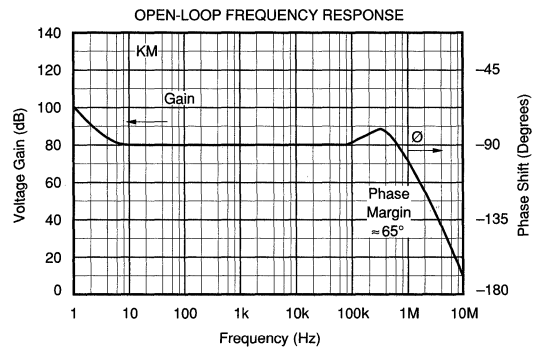
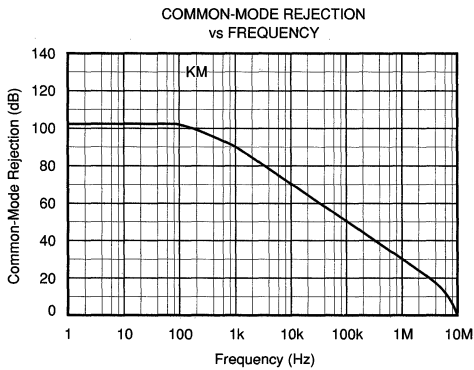
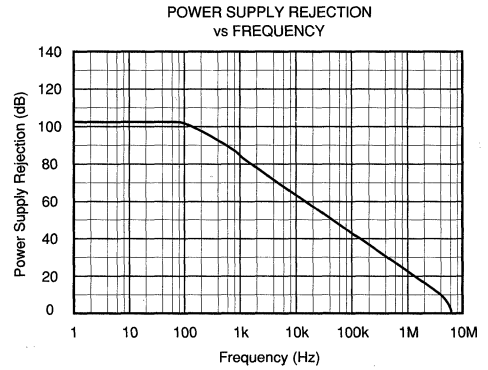
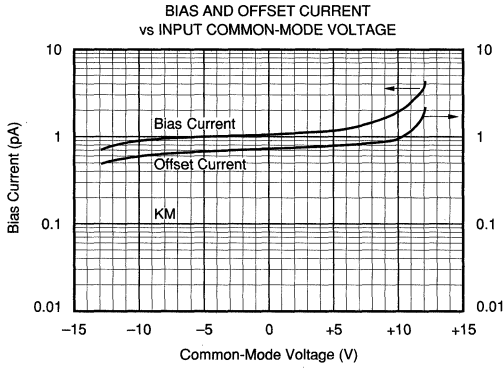
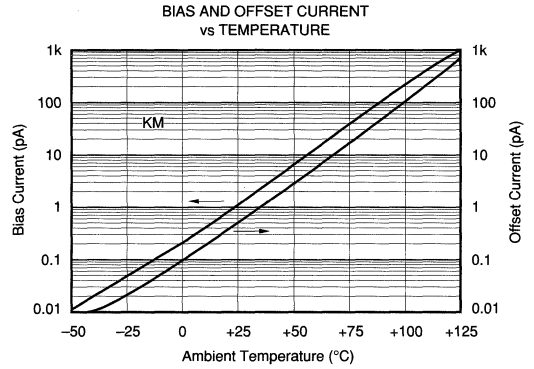
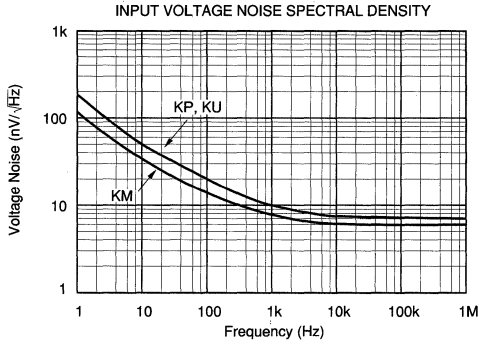
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA121KM	TO-99	$0^\circ C$ to $+70^\circ C$
OPA121KP	8-Pin Plastic DIP	$0^\circ C$ to $+70^\circ C$
OPA121KU	8-Pin SOIC	$0^\circ C$ to $+70^\circ C$

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TYPICAL PERFORMANCE CURVES

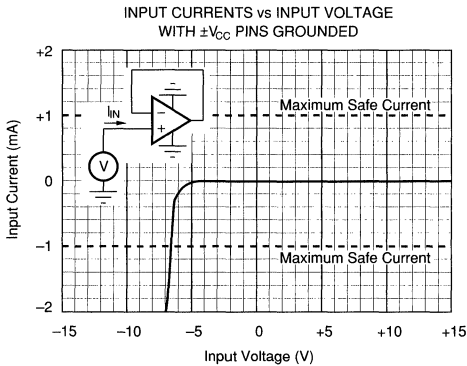
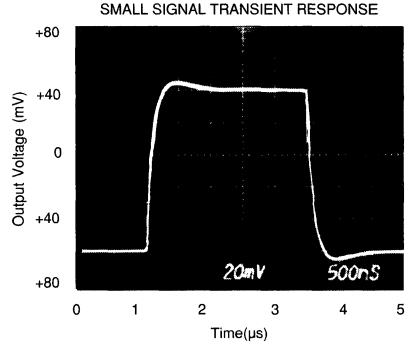
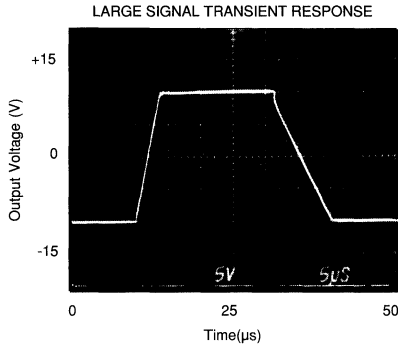
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA121 requires input current limiting resistors only if its input voltage is greater

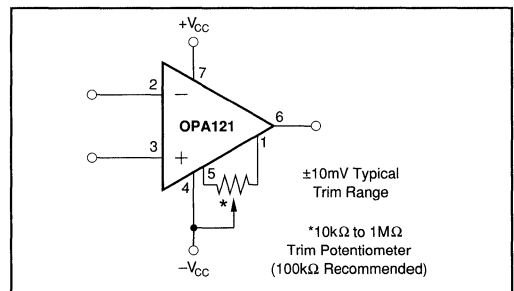


FIGURE 1. Offset Voltage Trim.

than 6V more negative than $-V_{CC}$. A $10\text{k}\Omega$ series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types),

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this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon™ standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high-impedance input leads and should be connected to a low-impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure #2).

If guarding is not required, pin 8 (case) should be connected to ground.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

Teflon™ E.I. du Pont de Nemours & Co.

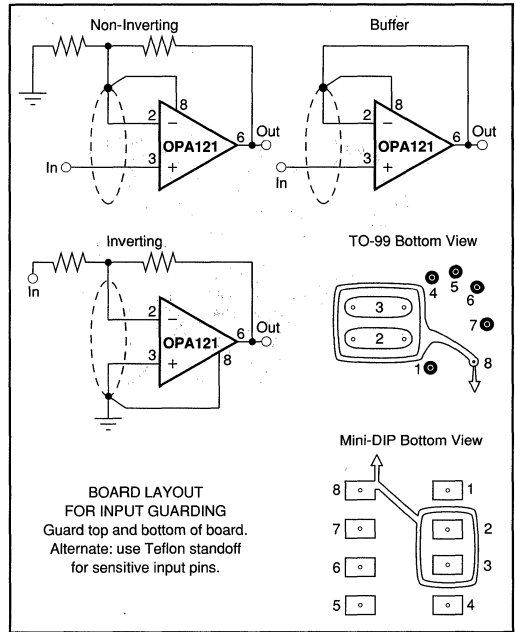


FIGURE 2. Connection of Input Guard.

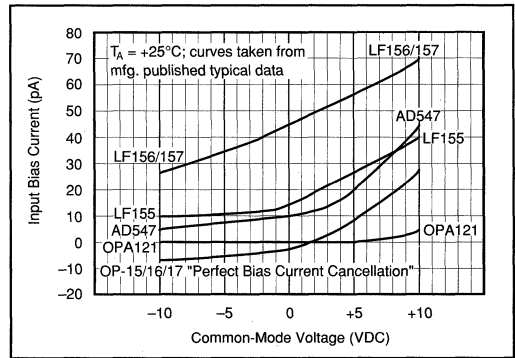


FIGURE 3. Input Bias Current vs Common-Mode Voltage.



OPA124

OPA124

2

OPERATIONAL AMPLIFIERS

Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: $6\text{nV}/\sqrt{\text{Hz}}$ (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250 μV max
- LOW DRIFT: 2 $\mu\text{V}/^\circ\text{C}$ max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES

APPLICATIONS

- PRECISION PHOTODIODE PREAMP
- MEDICAL EQUIPMENT
- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT

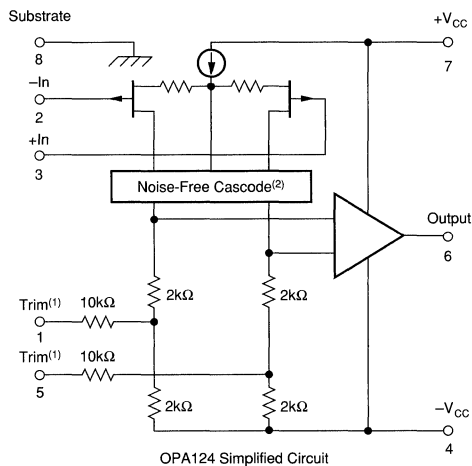
DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a *Difet* (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. *Difet* fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.

BIFET[®] National Semiconductor Corp.,
Difet[®] Burr-Brown Corp.



NOTES: (1) Omitted on SOIC. (2) Patented.

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SPECIFICATIONS

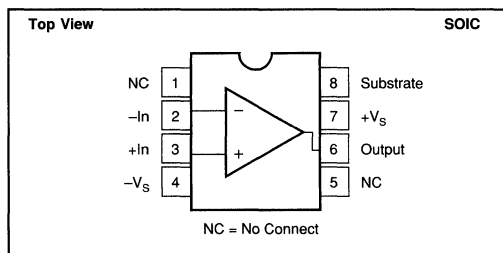
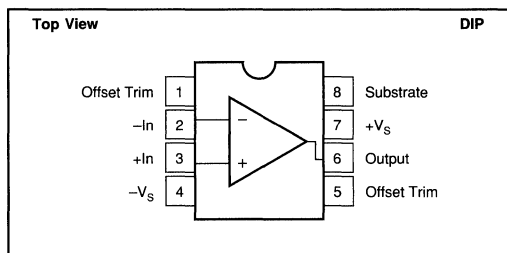
ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITION	OPA124U/P			OPA124UA/PA			OPA124UB/PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage, $f_o = 10\text{Hz}^{(4)}$			40	80		40	80		40	80	nV/ $\sqrt{\text{Hz}}$
$f_o = 100\text{Hz}^{(4)}$			15	40		15	40		15	40	nV/ $\sqrt{\text{Hz}}$
$f_o = 1\text{kHz}^{(4)}$			8	15		8	15		8	15	nV/ $\sqrt{\text{Hz}}$
$f_o = 10\text{kHz}^{(5)}$			6	8		6	8		6	8	nV/ $\sqrt{\text{Hz}}$
$f_b = 10\text{Hz to } 10\text{kHz}^{(5)}$			0.7	1.2		0.7	1.2		0.7	1.2	μVrms
$f_b = 0.1\text{Hz to } 10\text{Hz}$			1.6	3.3		1.6	3.3		1.6	3.3	$\mu\text{Vp-p}$
Current, $f_b = 0.1\text{Hz to } 10\text{Hz}$			9.5	15		9.5	15		9.5	15	fA/p-p
$f_o = 0.1\text{Hz thru } 20\text{kHz}$			0.5	0.8		0.5	0.8		0.5	0.8	fA/ $\sqrt{\text{Hz}}$
OFFSET VOLTAGE⁽¹⁾											
Input Offset Voltage vs Temperature	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}		± 200	± 800		± 150	± 500		± 100	± 250	μV
Supply Rejection vs Temperature	$V_{CC} = \pm 10\text{V to } \pm 18\text{V}$ $T_A = T_{MIN}$ to T_{MAX}	88	± 4	± 7.5	90	± 2	± 4	100	± 1	± 2	$\mu\text{V}/^\circ\text{C}$
		84	100		86	100		90	100		dB
BIAS CURRENT⁽¹⁾											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 1	± 5		± 0.5	± 2		± 0.35	± 1	pA
OFFSET CURRENT⁽¹⁾											
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 1	± 5		± 0.5	± 1		± 0.25	± 0.5	pA
IMPEDANCE											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE											
Common-Mode Input Range		± 10	± 11		± 10	± 11		± 10	± 11		V
Common-Mode Rejection vs Temperature	$V_{IN} = \pm 10\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}	92	110		94	110		100	110		dB
		86	100		86	100		90	100		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	106	125		106	125		120	125		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1.5			1.5			1.5		MHz
Full Power Response	20Vp-p, $R_L = 2\text{k}\Omega$	16	32		16	32		16	32		kHz
Slew Rate	$V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	1	1.6		1	1.6		1	1.6		V/ μs
THD			0.0003			0.0003			0.0003		%
Settling Time, 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		6			6			6		μs
0.01%	10V Step		10			10			10		μs
Overload Recovery, 50% Overdrive ⁽²⁾	Gain = -1		5			5			5		μs
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$	± 11	± 12		± 11	± 12		± 11	± 12		V
Current Output	$V_o = \pm 10\text{VDC}$	± 5.5	± 10		± 5.5	± 10		± 5.5	± 10		mA
Output Resistance	DC, Open Loop		100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		mA
POWER SUPPLY											
Rated Voltage			± 15			± 15			± 15		VDC
Voltage Range, Derated		± 5		± 18	± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_o = 0\text{mADC}$		2.5	3.5		2.5	3.5		2.5	3.5	mA
TEMPERATURE RANGE											
Specification	T_{MIN} and T_{MAX}	-25		+85	-25		+85	-25		+85	$^\circ\text{C}$
Storage		-65		+125	-65		+125	-65		+125	$^\circ\text{C}$
θ Junction-Ambient: PDIP			90			90			90		$^\circ\text{C}/\text{W}$
SOIC			100			100			100		$^\circ\text{C}/\text{W}$

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ⁽¹⁾	750mW
Differential Input Voltage ⁽²⁾	±36VDC
Input Voltage Range ⁽²⁾	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration ⁽³⁾	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JA} = 90^\circ\text{C/W}$ for PDIP and 100°C/W for SOIC. (2) For supply voltages less than $\pm 18\text{VDC}$, the absolute maximum input voltage is equal to $+18\text{V} > V_{IN} > -V_{DC} - 6\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA124U	8-Pin SOIC	182
OPA124P	8-Pin Plastic DIP	006
OPA124UA	8-Pin SOIC	182
OPA124PA	8-Pin Plastic DIP	006
OPA124UB	8-Pin SOIC	182
OPA124PB	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

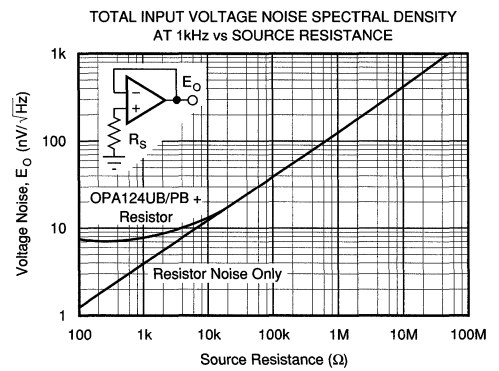
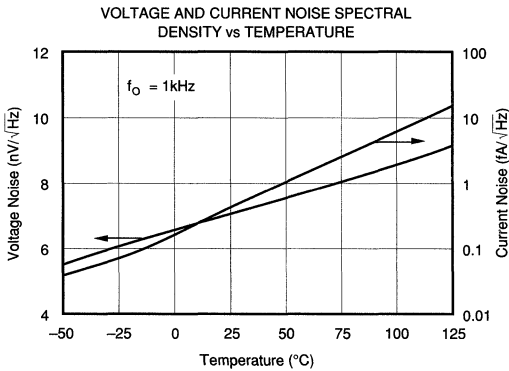
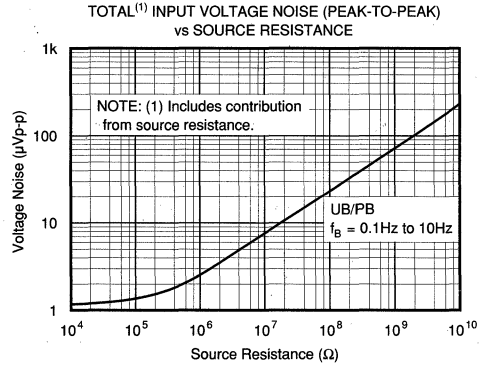
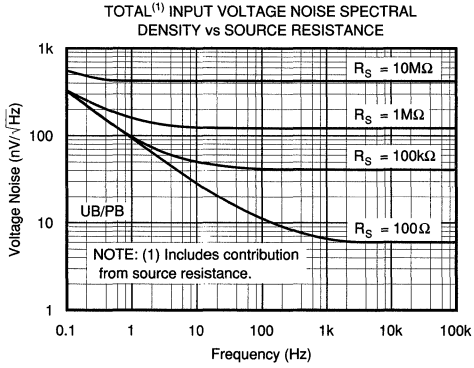
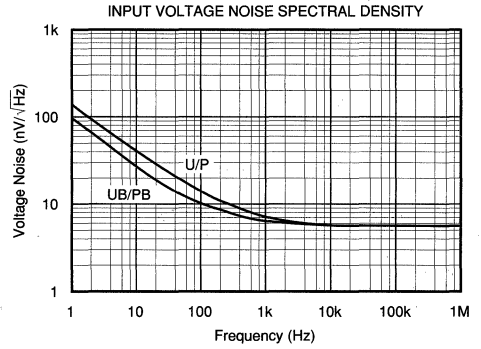
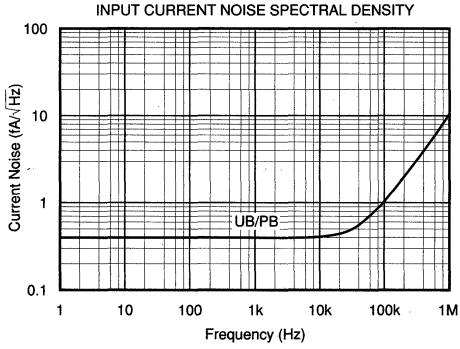
MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT pA, max	OFFSET DRIFT $\mu\text{V}/^\circ\text{C}$, max
OPA124U	8-PIN SOIC	-25°C TO +85°C	5	7.5
OPA124P	8-Pin Plastic DIP	-25°C to +85°C	5	7.5
OPA124UA	8-Pin SOIC	-25°C to +85°C	2	4
OPA124PA	8-Pin Plastic DIP	-25°C to +85°C	2	4
OPA124UB	8-Pin SOIC	-25°C to +85°C	1	2
OPA124PB	8-Pin Plastic DIP	-25°C to +85°C	1	2

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TYPICAL PERFORMANCE CURVES

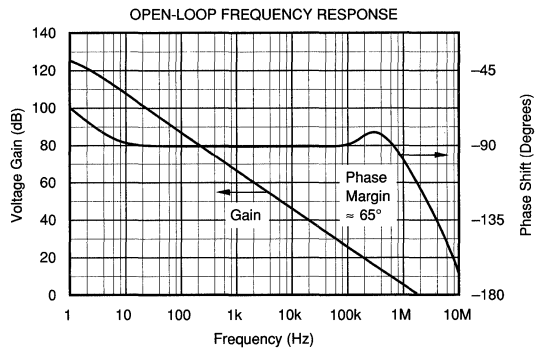
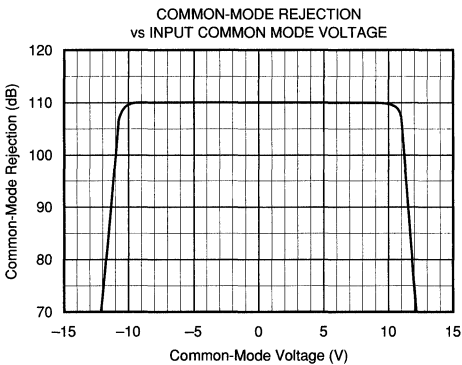
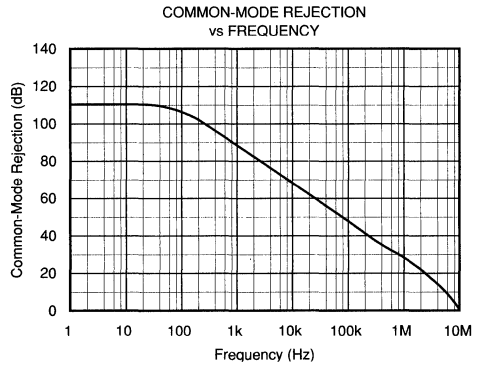
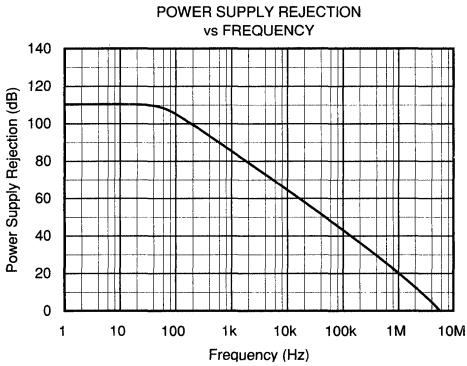
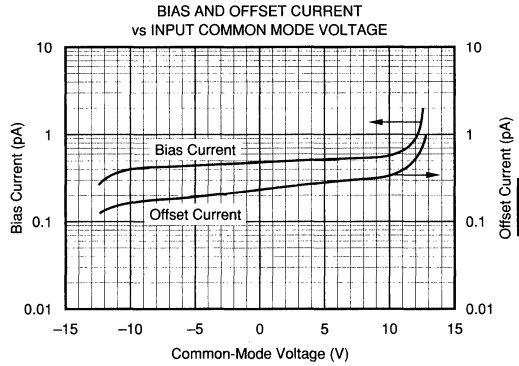
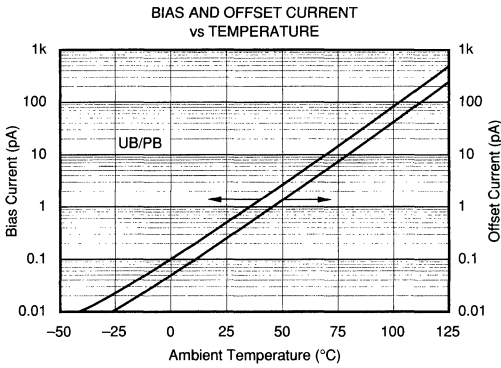
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

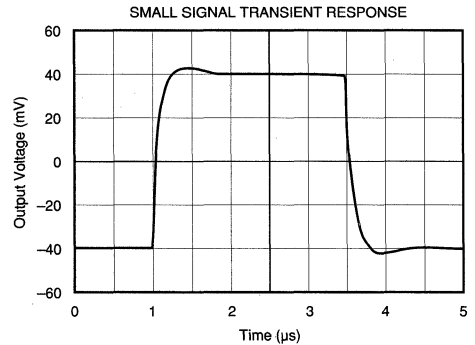
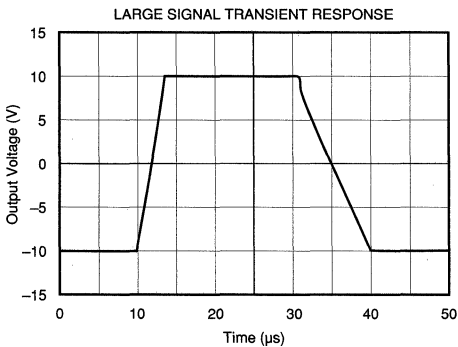
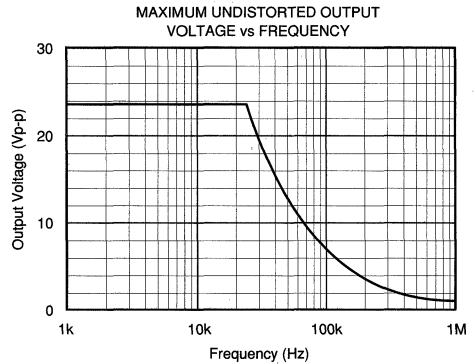
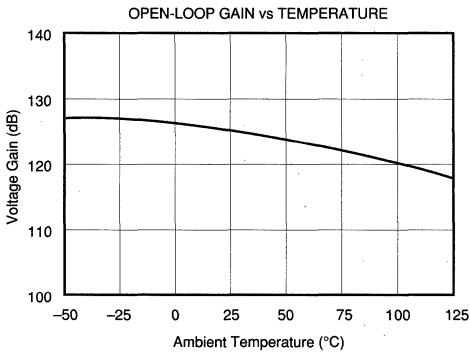
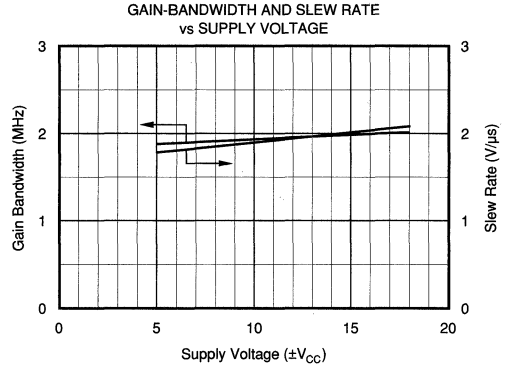
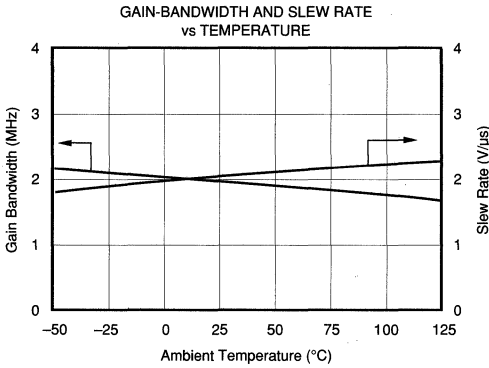
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

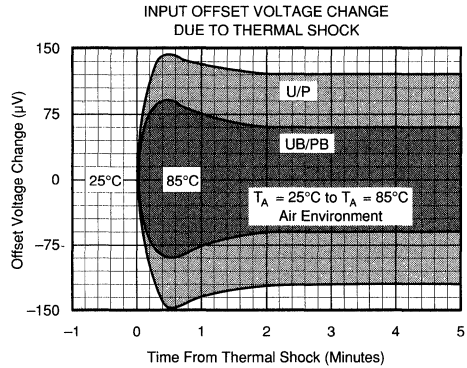
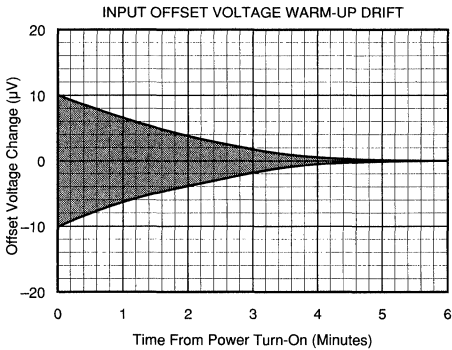
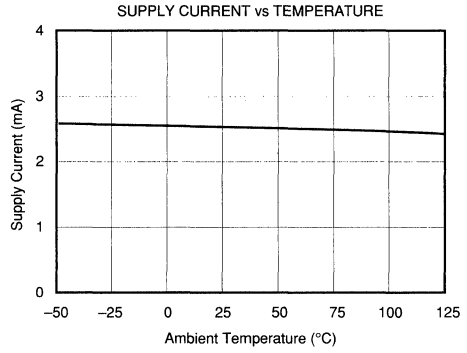
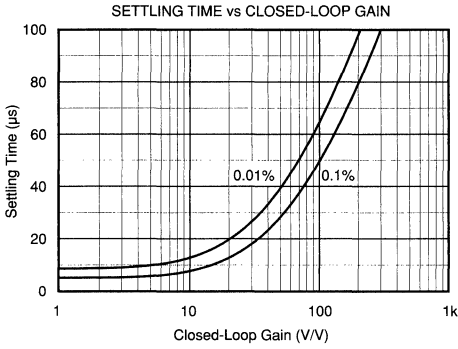
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA124 offset voltage is laser-trimmed and will require no further trim for most applications. In order to reduce layout leakage errors, the offset adjust capability has been removed from the SOIC versions (OPA124UB, OPA124UA, and OPA124U). The PDIP versions (OPA124PB, OPA124PA, and OPA124P) do have pins available for offset adjustment. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. The correct circuit configuration for offset adjust for the PDIP packages is shown in Figure 1.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA124 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A $10\text{k}\Omega$ series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels, even if both supply voltages are lost (Figure 2).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA124. To avoid leakage problems, the OPA124 should be soldered directly into a printed circuit board. Utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier substrate should be connected to any input shield or guard via pin 8 minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 should be connected to ground.

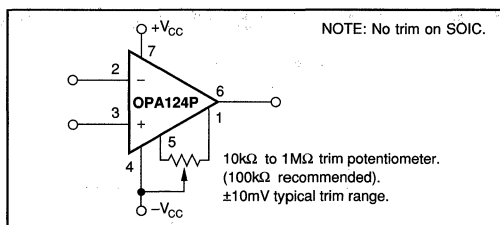


FIGURE 1. Offset Voltage Trim for PDIP packages.

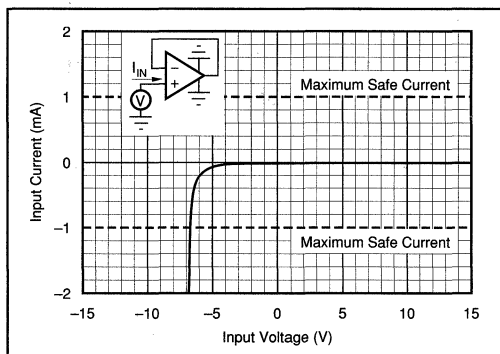
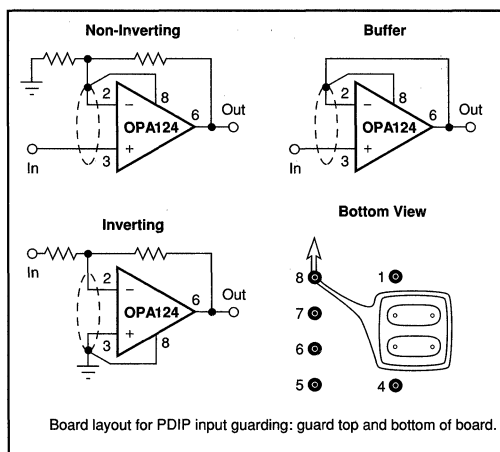


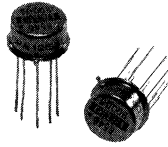
FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.



Board layout for PDIP input guarding: guard top and bottom of board.

FIGURE 3. Connection of Input Guard.

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OPA128

Difet[®] Electrometer-Grade OPERATIONAL AMPLIFIER

OPA128
2
OPERATIONAL AMPLIFIERS

FEATURES

- ULTRA-LOW BIAS CURRENT: 75fA max
- LOW OFFSET: 500 μ V max
- LOW DRIFT: 5 μ V/ $^{\circ}$ C max
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 90dB min
- IMPROVED REPLACEMENT FOR AD515 AND AD549

APPLICATIONS

- ELECTROMETER
- MASS SPECTROMETER
- CHROMATOGRAPH
- ION GAUGE
- PHOTODETECTOR
- RADIATION-HARD EQUIPMENT

DESCRIPTION

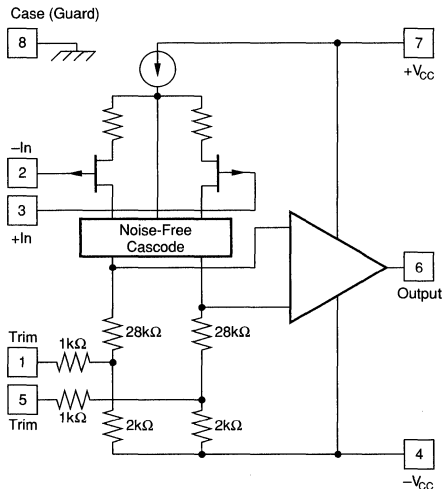
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (*Difet*[®]) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

Difet[®] Burr-Brown Corp.



OPA128 Simplified Circuit

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT														
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$, $R_L \geq 10\text{k}\Omega$		± 150	± 300		± 75	± 150		± 40	± 75		± 75	± 150	fA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$, $R_L \geq 10\text{k}\Omega$		65			30			30			30		fA
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}		± 260	± 1000 ± 20		± 140	± 500 ± 10		± 140	± 500 ± 5		± 140	± 500 ± 10	μV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V/V}$
NOISE Voltage: $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_b = 10\text{Hz}$ to 10kHz $f_b = 0.1\text{Hz}$ to 10Hz Current: $f_b = 0.1\text{Hz}$ to 10Hz $f_b = 0.1\text{Hz}$ to 20kHz			92 78 27 15 2.4 4 4.2 0.22			92 78 27 15 2.4 4 3 0.16			92 78 27 15 2.4 4 2.3 0.12			92 78 27 15 2.4 4 3 0.16	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\mu\text{Vp-p}$ fA, p-p fA/ $\sqrt{\text{Hz}}$	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{15} \parallel 2$			$10^{13} \parallel 1$ $10^{15} \parallel 2$			$10^{13} \parallel 1$ $10^{15} \parallel 2$			$10^{13} \parallel 1$ $10^{15} \parallel 2$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
VOLTAGE RANGE⁽⁴⁾ Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10	± 12		± 10	± 12		± 10	± 12		± 10	± 12		V dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	94	128		110	128		110	128		110	128		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal Full Power Response Slew Rate Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽³⁾	⁽²⁾ 20Vp-p , $R_L = 2\text{k}\Omega$ $V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Gain = -1 , $R_L = 2\text{k}\Omega$ 10V Step Gain = -1	0.5	1		0.5	1		0.5	1		0.5	1		MHz kHz V/ μs μs μs
RATED OUTPUT														
Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_o = \pm 10\text{VDC}$ DC, Open Loop Gain = $+1$	± 10 ± 5	± 13 ± 10		± 10 ± 5	± 13 ± 10		± 10 ± 5	± 13 ± 10		± 10 ± 5	± 13 ± 10		V mA Ω pF mA
POWER SUPPLY														
Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_o = 0\text{mADC}$		± 15			± 15			± 15			± 15		VDC VDC mA
TEMPERATURE RANGE														
Specification Operating Storage θ Junction-Ambient	Ambient Temp. Ambient Temp. Ambient Temp.	0 -55 -65		+70 -55 +150	0 -55 -65		+70 -55 +150	0 -55 -65	+70 -55 +150		+70 -55 -65		+125 -55 +150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. Bias current doubles approximately every 11°C . (2) Sample tested. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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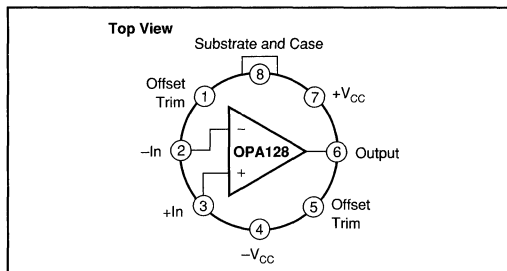
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MN}$ and T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
TEMPERATURE RANGE															
Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	-55		+125	°C	
INPUT															
BIAS CURRENT⁽¹⁾															
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 2.5	± 8		± 1.3	± 4		± 0.7	± 2		± 43	± 170	pA	
OFFSET CURRENT⁽¹⁾															
Input Offset Current	$V_{CM} = 0\text{VDC}$		1.1			0.6			0.6			18		pA	
OFFSET VOLTAGE⁽¹⁾															
Input Offset Voltage	$V_{CM} = 0\text{VDC}$			$\pm 2.2\text{mV}$			$\pm 1\text{mV}$			± 750			$\pm 1.5\text{mV}$	μV	
Average Drift				± 20			± 10			± 5			± 10	$\mu\text{V}/^\circ\text{C}$	
Supply Rejection		74	114	± 2	± 200	80	114	± 2	± 100	80	114	± 2	± 100	$\mu\text{V}/\text{V}$	
VOLTAGE RANGE⁽²⁾															
Common-Mode Input Range		± 10	± 11			± 10	± 11			± 10	± 11			V	
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	74	112			80	112			80	112			dB	
OPEN-LOOP GAIN, DC															
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	90	125			104	125			104	125			dB	
RATED OUTPUT															
Voltage Output	$R_L = 2\text{k}\Omega$	± 10				± 10				± 10				V	
Current Output	$V_O = \pm 10\text{VDC}$	± 5				± 5				± 5				mA	
Short Circuit Current	$V_O = 0\text{VDC}$	10	22			10	22			10	22			mA	
POWER SUPPLY															
Current, Quiescent	$I = 0\text{mADC}$		0.9	1.8		0.9	1.8			0.9	1.8		0.9	2	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (2) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage	$\pm 36\text{VDC}$
Input Voltage Range	$\pm 18\text{VDC}$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration ⁽²⁾	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JA} = 150^\circ\text{C}/\text{W}$ or $\theta_{JK} = 200^\circ\text{C}/\text{W}$. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT, max (fA)
OPA128JM	TO-99	0°C to +70°C	± 300
OPA128KM	TO-99	0°C to +70°C	± 150
OPA128LM	TO-99	0°C to +70°C	± 75
OPA128SM	TO-99	-55°C to +125°C	± 150

PACKAGE INFORMATION⁽¹⁾

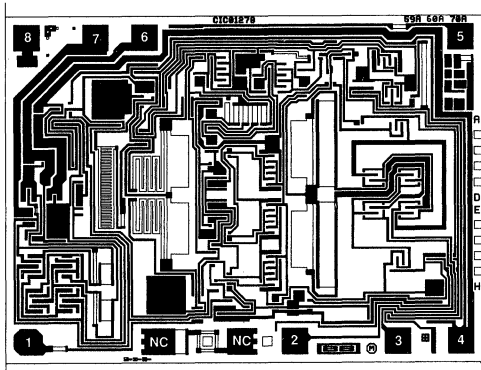
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA128JM	TO-99	001
OPA128KM	TO-99	001
OPA128LM	TO-99	001
OPA128SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

OPERATIONAL AMPLIFIERS 2 OPA128

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DICE INFORMATION



OPA128 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _{cc}
5	Offset Trim
6	Output
7	+V _{cc}
8	Substrate
NC	No Connection

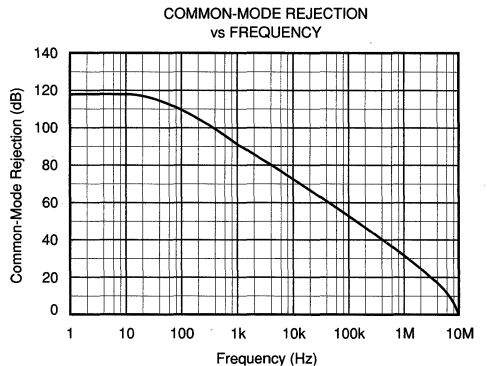
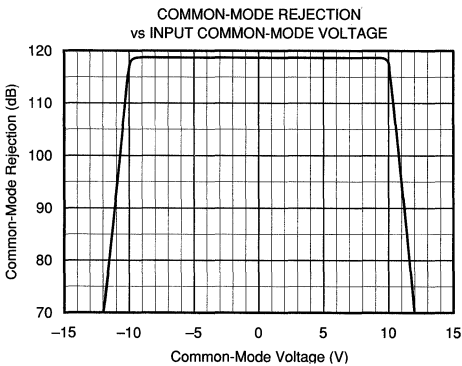
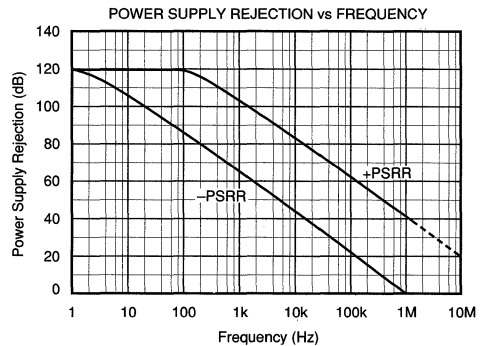
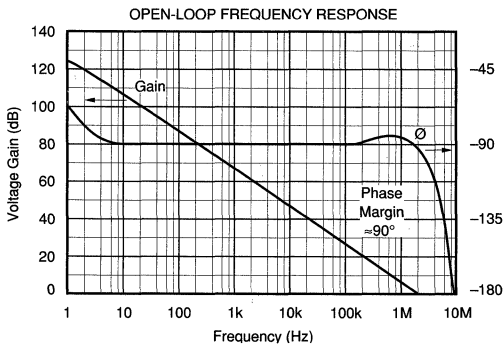
Substrate Bias: Isolated, normally connected to common.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	96 x 71 ±5	2.44 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

TYPICAL PERFORMANCE CURVES

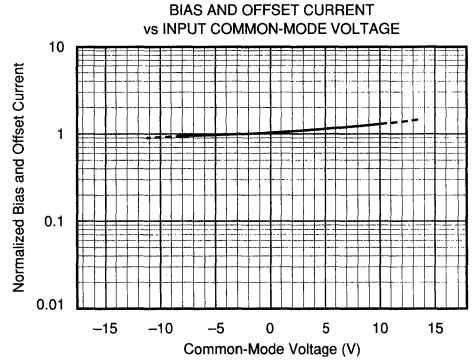
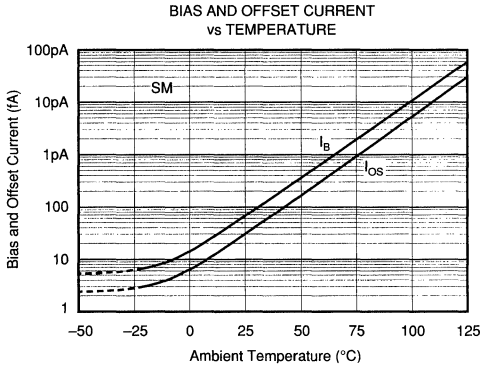
T_A = +25°C, ±15VDC, unless otherwise noted.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

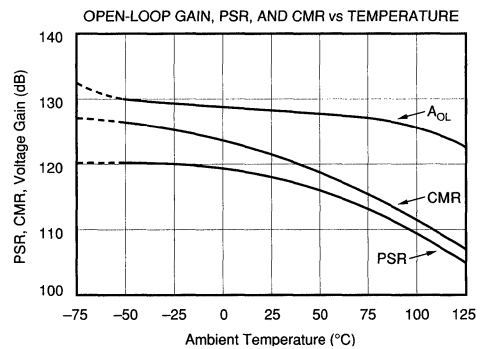
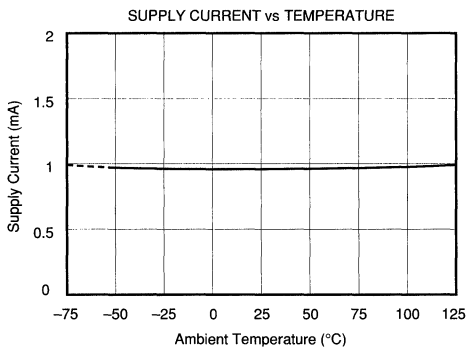
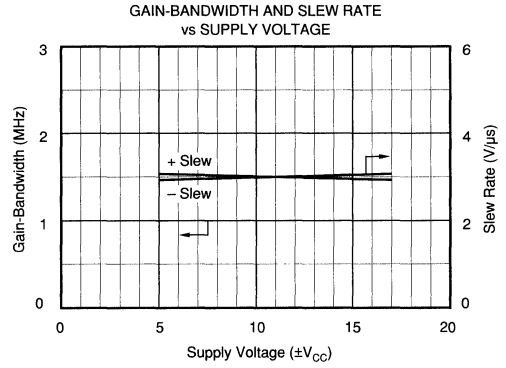
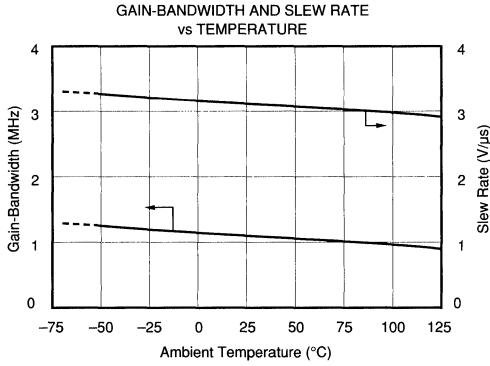
At $T_A = +25^\circ\text{C}$, +15VDC unless otherwise noted.



OPA128

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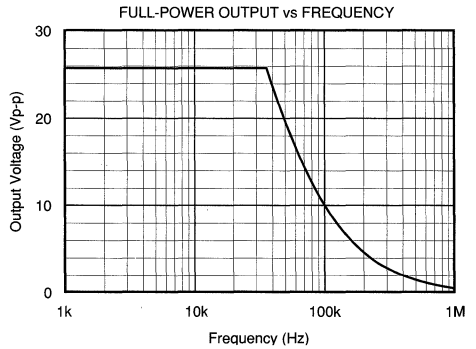
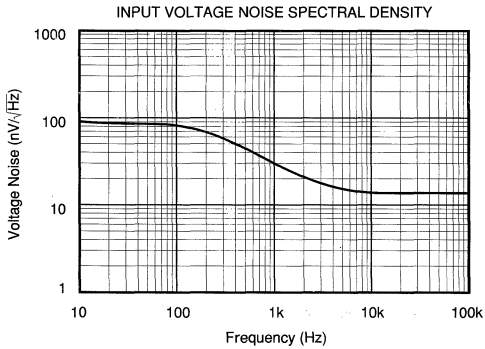
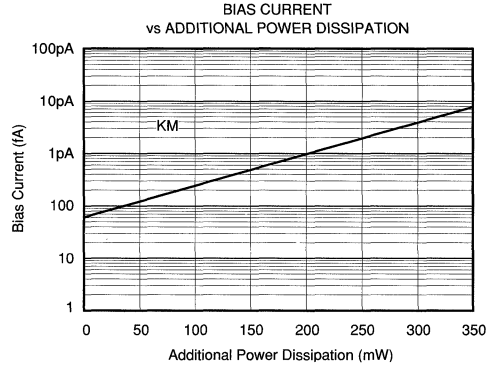
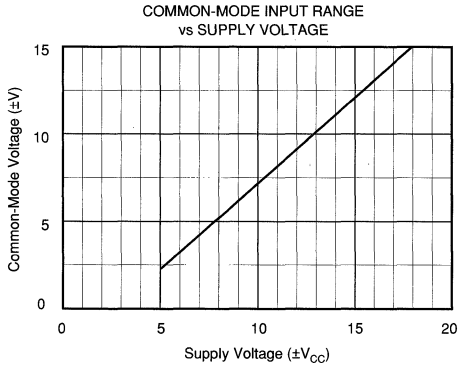
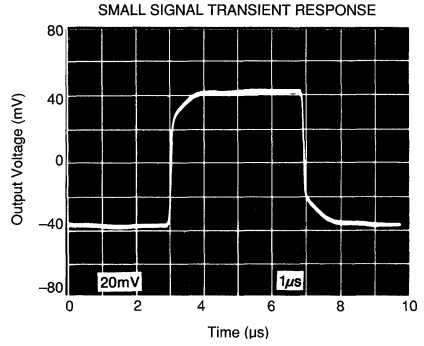
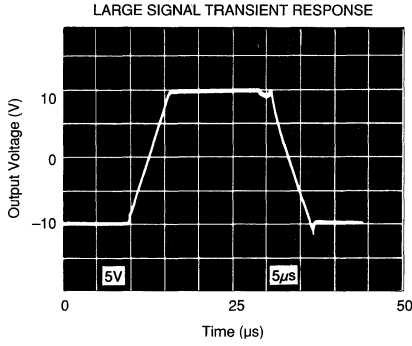
OPERATIONAL AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, +15VDC unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA128 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted effort. Note that the trim (Figure 1) is similar to operational amplifiers such as HA-5180 and AD515. The OPA128 can replace many other amplifiers by leaving the external null circuit unconnected.

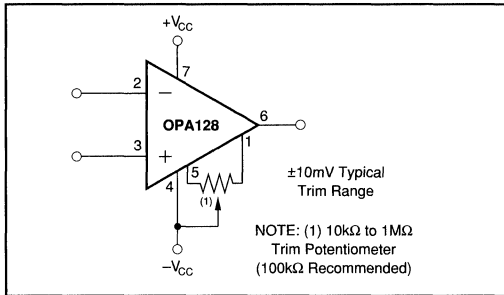


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers' inputs must be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA128. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA128. To avoid leakage problems, it is recommended that the signal input lead of the OPA128 be wired to a Teflon standoff. If the input is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

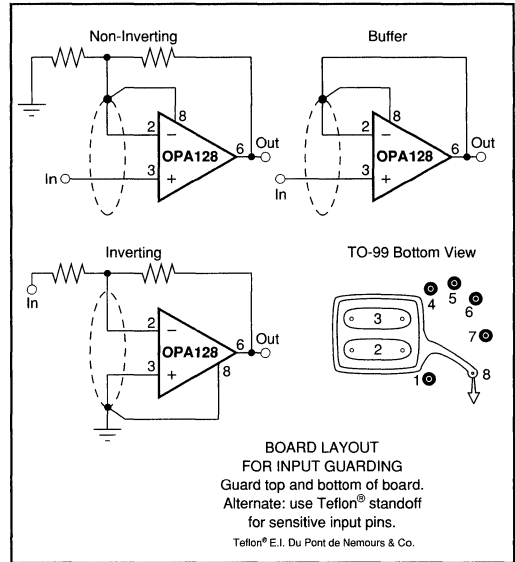


FIGURE 2. Connection of Input Guard.

Triboelectric charge (static electricity generated by friction) can be a troublesome noise source from cables connected to the input of an electrometer amplifier. Special low-noise cable will minimize this effect but the optimum solution is to mount the signal source directly at the electrometer input with short, rigid, wiring to preclude microphonic noise generation.

TESTING

Accurately testing the OPA128 is extremely difficult due to its high level of performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage
2. Unclean package
3. Humidity or dew point condensation
4. Circuit contamination from fingerprints or anti-static treatment chemicals
5. Test ambient temperature
6. Load power dissipation

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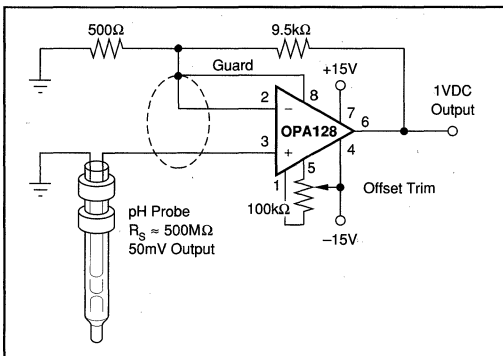


FIGURE 3. High Impedance ($10^{15}\Omega$) Amplifier.

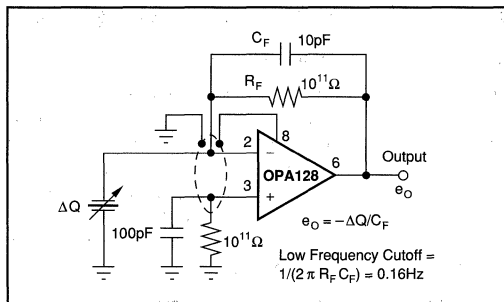


FIGURE 4. Piezoelectric Transducer Charge Amplifier.

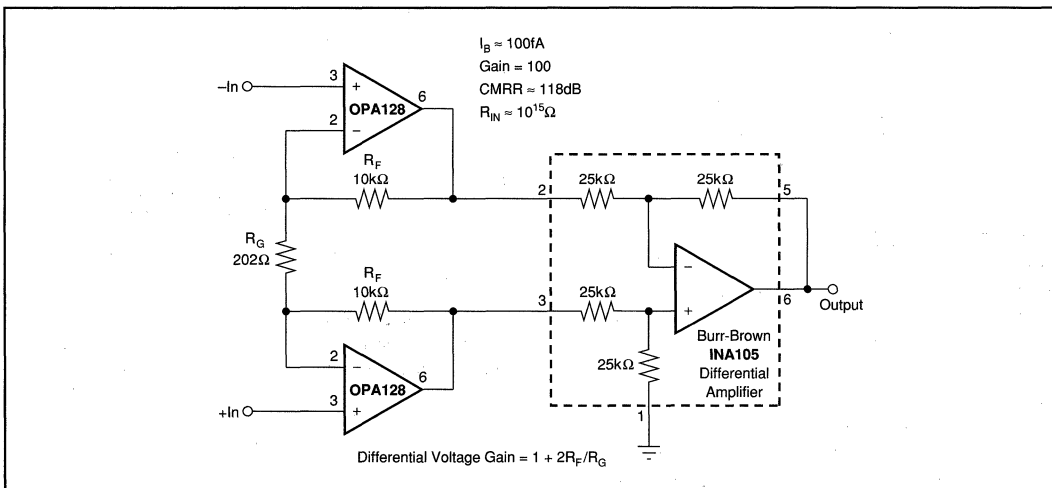
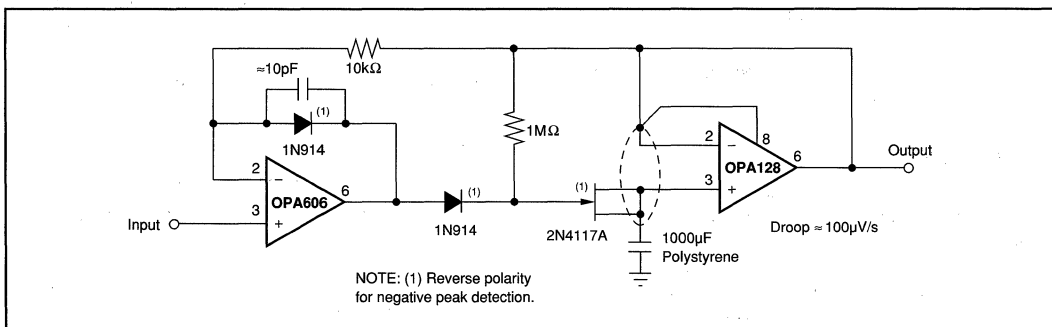


FIGURE 5. FET Input Instrumentation Amplifier for Biomedical Applications.



NOTE: (1) Reverse polarity for negative peak detection.

FIGURE 6. Low-Droop Positive Peak Detector.

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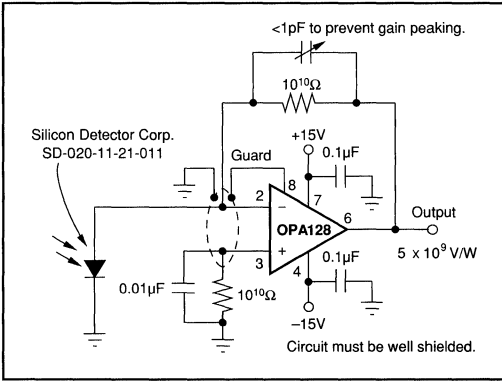


FIGURE 7. Sensitive Photodiode Amplifier.

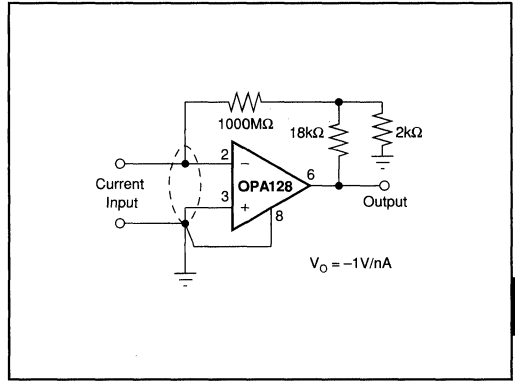


FIGURE 8. Current-to-Voltage Converter.

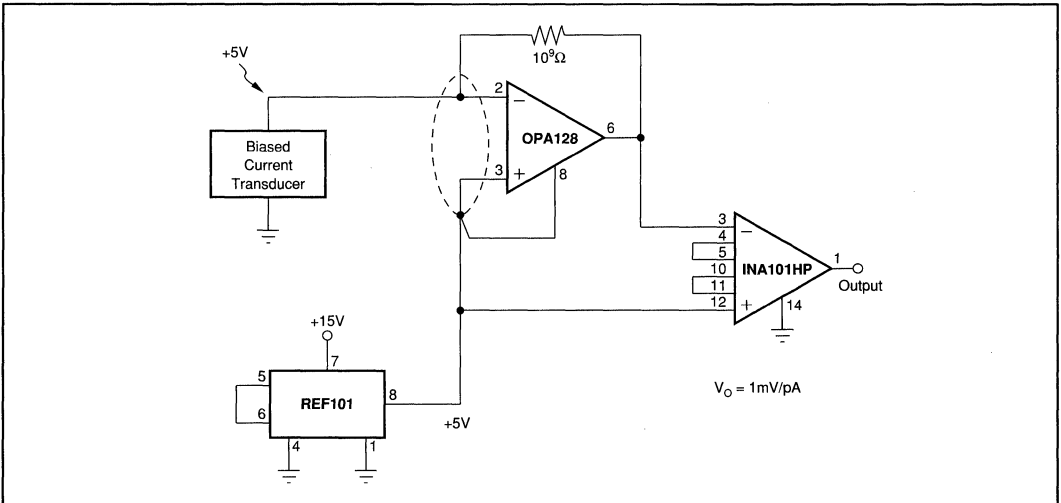
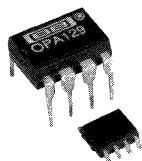


FIGURE 9. Biased Current-to-Voltage Converter.

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OPA129

Ultra-Low Bias Current *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- ULTRA-LOW BIAS CURRENT: 100fA max
- LOW OFFSET: 2mV max
- LOW DRIFT: 10 μ V/ $^{\circ}$ C max
- HIGH OPEN-LOOP GAIN: 94dB min
- LOW NOISE: 15nV/ $\sqrt{\text{Hz}}$ at 10kHz
- PLASTIC DIP and SOIC PACKAGE

APPLICATIONS

- PHOTODETECTOR PREAMP
- CHROMATOGRAPHY
- ELECTROMETER AMPLIFIERS
- MASS SPECTROMETER
- pH PROBE AMPLIFIER
- ION GAGE MEASUREMENT

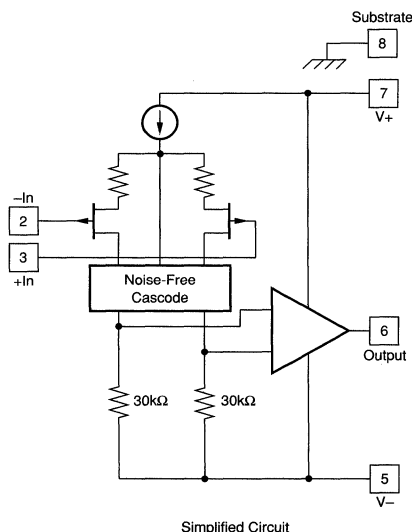
DESCRIPTION

The OPA129 is an ultra-low bias current monolithic operational amplifier offered in an 8-pin PDIP and SO-8 package. Using advanced geometry dielectrically-isolated FET (*Difet*[®]) inputs, this monolithic amplifier achieves a high performance level.

Difet fabrication eliminates isolation-junction leakage current—the main contributor to input bias current with conventional monolithic FETs. This reduces input bias current by a factor of 10 to 100. Very low input bias current can be achieved without resorting to small-geometry FETs or CMOS designs which can suffer from much larger offset voltage, voltage noise, drift, and poor power supply rejection.

The OPA129's special pinout eliminates leakage current that occurs with other op amps. Pins 1 and 4 have no internal connection, allowing circuit board guard traces—even with the surface-mount package version.

OPA129 is available in 8-pin DIP and SO-8 packages, specified for operation from -40°C to $+85^{\circ}\text{C}$.



Difet[®] Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 899-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 15V$ and $T_A = +25^\circ C$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITION	OPA129PB, UB			OPA129P, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT BIAS CURRENT⁽¹⁾ vs Temperature	$V_{CM} = 0V$		± 30	± 100		*	± 250	fA
			Doubles every 10°C					
INPUT OFFSET CURRENT	$V_{CM} = 0V$		± 30			*		fA
OFFSET VOLTAGE Input Offset Voltage vs Temperature Supply Rejection	$V_{CM} = 0V$ $V_S = \pm 5V$ to $\pm 18V$		± 0.5 ± 3 ± 3	± 2 ± 10 ± 100		± 1 ± 5 *	± 5 *	mV $\mu V/^\circ C$ $\mu V/V$
NOISE Voltage	$f = 10Hz$ $f = 100Hz$ $f = 1kHz$ $f = 10kHz$ $f_b = 0.1Hz$ to $10Hz$ $f = 10kHz$		85 28 17 15 4 0.1			*		nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} $\mu Vp-p$ fA/\sqrt{Hz}
Current						*		
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{15} \parallel 2$			*	*	$\Omega \parallel pF$ $\Omega \parallel pF$
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10V$	± 10 80	± 12 118		*	*		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	94	120		*	*		dB
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate Settling Time: 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽²⁾	$20Vp-p, R_L = 2k\Omega$ $V_O = \pm 10V, R_L = 2k\Omega$ $G = -1, R_L = 2k\Omega, 10V$ Step $G = -1$	1	1 47 2.5 5 10 5		*	*		MHz kHz V/ μs μs μs μs
RATED OUTPUT Voltage Output Current Output Load Capacitance Stability Short-Circuit Current	$R_L = 2k\Omega$ $V_O = \pm 12V$ Gain = +1	± 12 ± 6	± 13 ± 10 1000 ± 35		*	*	*	V mA pF mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0mA$	± 5	± 15 1.2 1.8	± 18	*	*	*	V V mA
TEMPERATURE Specification Operating Storage Thermal Resistance PDIP—"P" SOIC—"U"	Ambient Temperature Ambient Temperature θ_{JA} , Junction-to-Ambient	-40 -40 -40		+85 +125 +125	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$

NOTES: (1) High-speed automated test. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.

OPA129

OPERATIONAL AMPLIFIERS

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Differential Input Voltage	V- to V+
Input Voltage Range	V- to V+
Storage Temperature Range	-40°C to +125°C
Operating Temperature Range	-40°C to +125°C
Lead Temperature (soldering, 10s; SOIC 3s)	+300°C
Output Short Circuit Duration ⁽¹⁾	Continuous
Junction Temperature (T _J)	+150°C

NOTE: (1) Short circuit may be to power supply common at +25°C ambient.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA129P	8-pin Plastic DIP	006
OPA129PB	8-pin Plastic DIP	006
OPA129U	8-pin SOIC	182
OPA129UB	8-pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

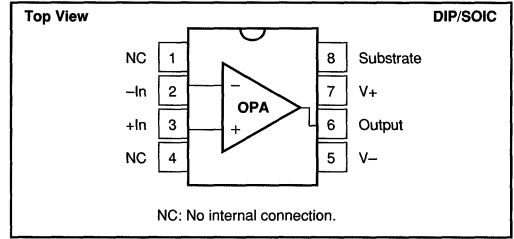


ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

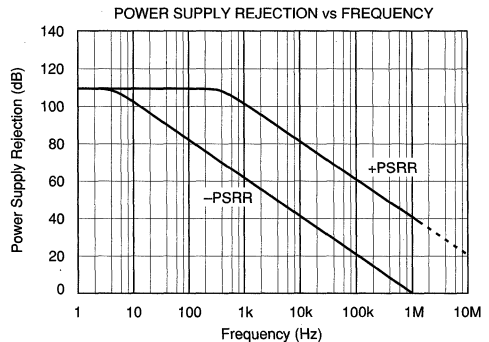
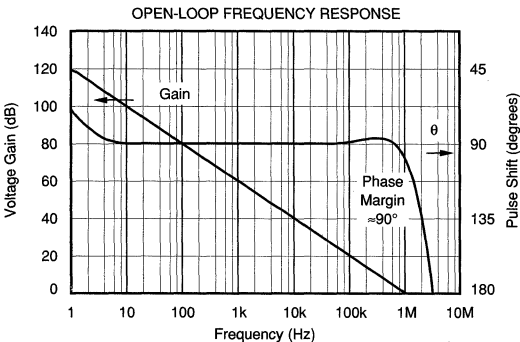
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES

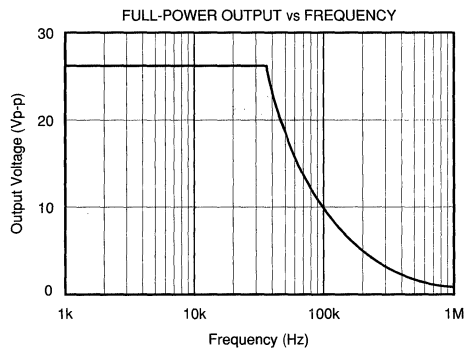
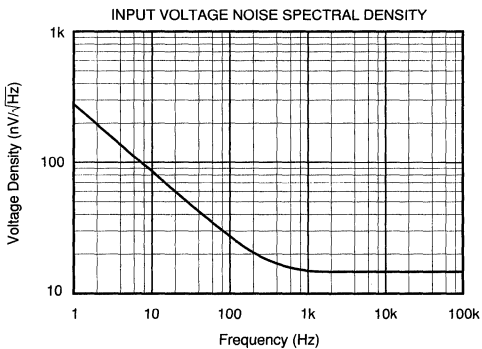
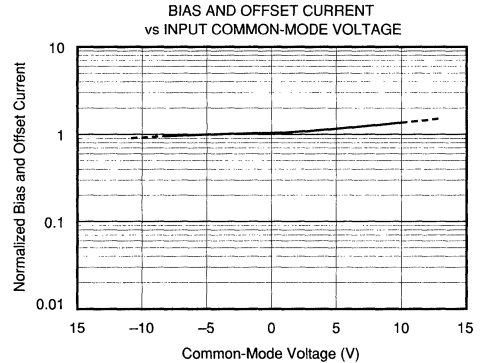
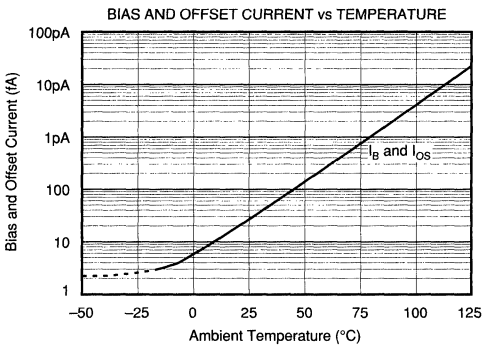
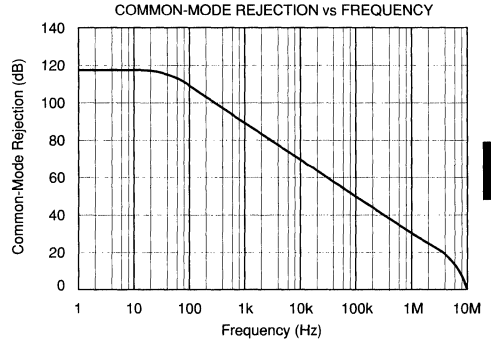
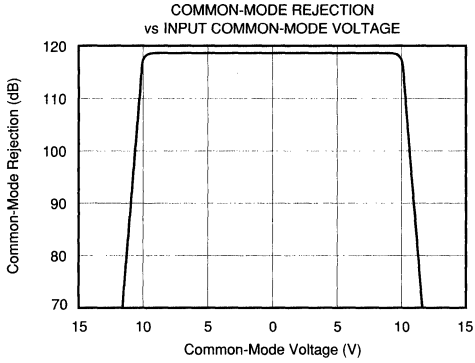
T_A = +25°C, +15VDC, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

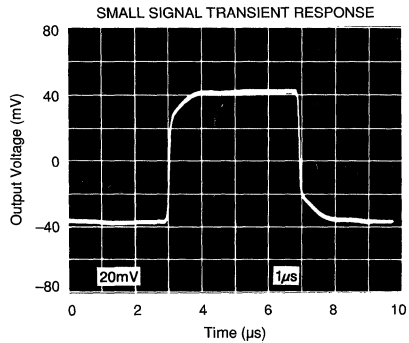
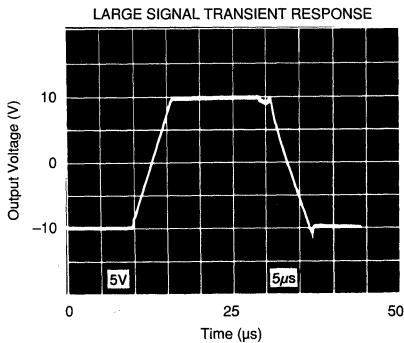
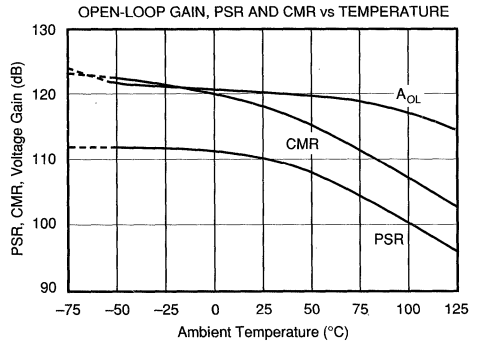
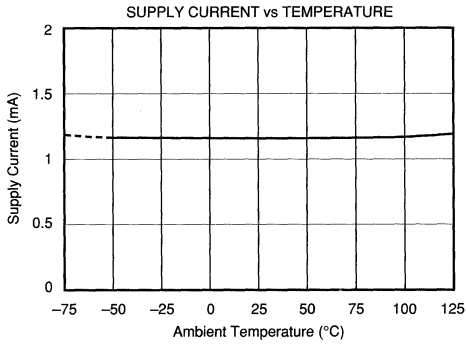
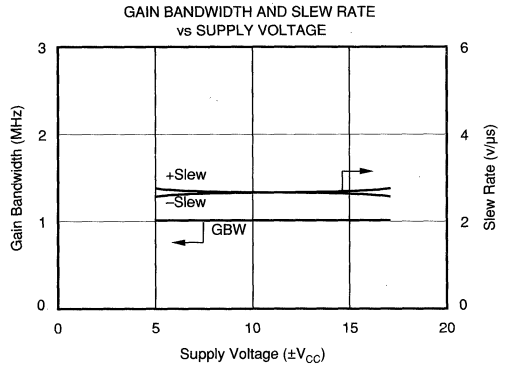
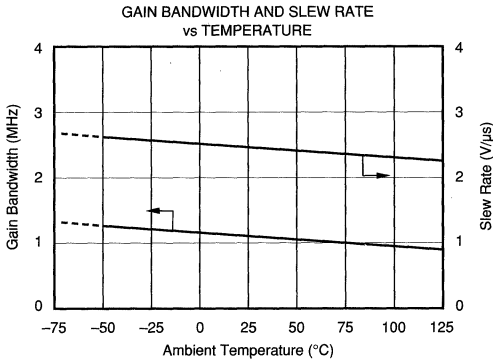
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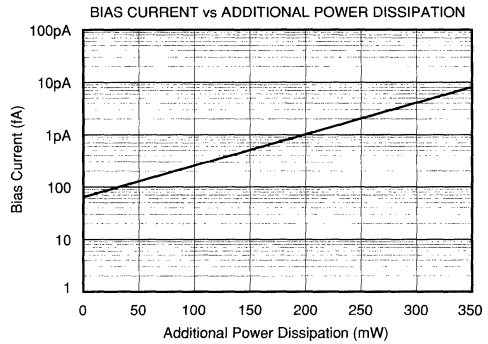
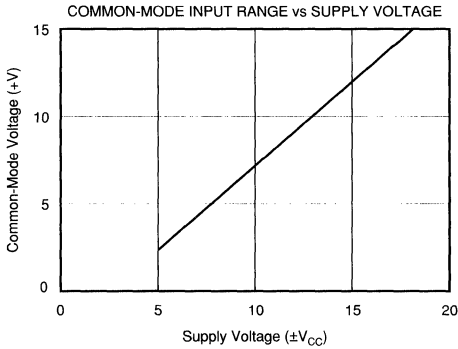
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, +15VDC, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, +15VDC, unless otherwise noted.



APPLICATIONS INFORMATION

NON-STANDARD PINOUT

The OPA129 uses a non-standard pinout to achieve lowest possible input bias current. The negative power supply is connected to pin 5—see Figure 1. This is done to reduce the leakage current from the V⁻ supply (pin 4 on conventional op amps) to the op amp input terminals. With this new pinout, sensitive inputs are separated from both power supply pins.

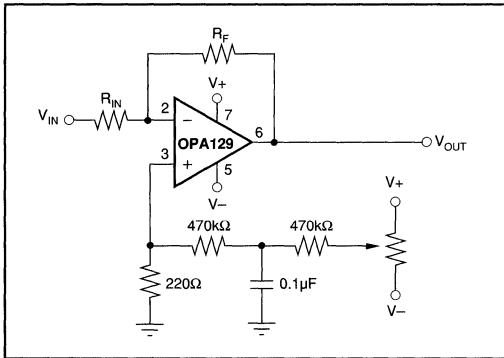


FIGURE 1. Offset Adjust Circuit.

OFFSET VOLTAGE TRIM

The OPA129 has no conventional offset trim connections. Pin 1, next to the critical inverting input, has no internal connection. This eliminates a source of leakage current and allows guarding of the input terminals. Pin 1 and pin 4, next to the two input pins, have no internal connection. This allows an optimized circuit board layout with guarding—see “circuit board layout.”

Due to its laser-trimmed input stage, most applications do not require external offset voltage trimming. If trimming is required, the circuit shown in Figure 1 can be used. Power supply voltages are divided down, filtered and applied to the non-inverting input. The circuit shown is sensitive to variation in the supply voltages. Regulation can be added, if needed.

GUARDING AND SHIELDING

Ultra-low input bias current op amps require precautions to achieve best performance. Leakage current on the surface of circuit board can exceed the input bias current of the amplifier. For example, a circuit board resistance of $10^{12}\Omega$ from a power supply pin to an input pin produces a current of 15pA—more than one-hundred times the input bias current of the op amp.

To minimize surface leakage, a guard trace should completely surround the input terminals and other circuitry connecting to the inputs of the op amp. The DIP package should have a guard trace on both sides of the circuit board. The guard ring should be driven by a circuit node equal in potential to the op amp inputs—see Figure 2. The substrate, pin 8, should also be connected to the circuit board guard to assure that the amplifier is fully surrounded by the guard potential. This minimizes leakage current and noise pick-up.

Careful shielding is required to reduce noise pickup. Shielding near feedback components may also help reduce noise pick-up.

Triboelectric effects (friction-generated charge) can be a troublesome source of errors. Vibration of the circuit board, input connectors and input cables can cause noise and drift. Make the assembly as rigid as possible. Attach cables to avoid motion and vibration. Special low noise or low leakage cables may help reduce noise and leakage current. Keep all input connections as short as possible. Surface-mount components may reduce circuit board size and allow a more rigid assembly.

For Immediate Assistance, Contact Your Local Salesperson

CIRCUIT BOARD LAYOUT

The OPA129 uses a new pinout for ultra low input bias current. Pin 1 and pin 4 have no internal connection. This allows ample circuit board space for a guard ring surrounding the op amp input pins—even with the tiny SO-8 surface-mount package. Figure 3 shows suggested circuit board layouts. The guard ring should be connected to pin 8 (substrate) as shown. It should be driven by a circuit node equal in potential to the input terminals of the op amp—see Figure 2 for common circuit configurations.

TESTING

Accurately testing the OPA129 is extremely difficult due to its high performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current. Inaccurate bias current measurements can be due to:

1. Test socket leakage,
2. Unclean package,
3. Humidity or dew point condensations,
4. Circuit contamination from fingerprints or anti-static treatment chemicals,
5. Test ambient temperature,
6. Load power dissipation,
7. Mechanical stress,
8. Electrostatic and electromagnetic interference.

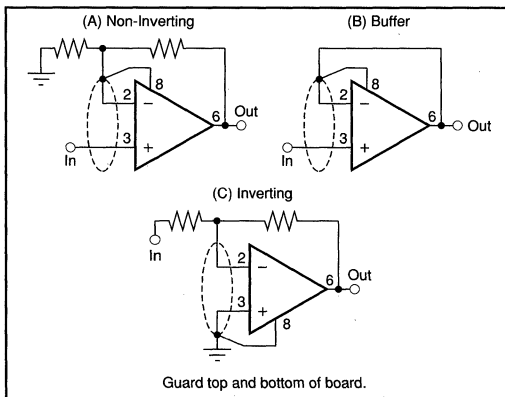


FIGURE 2. Connection of Input Guard.

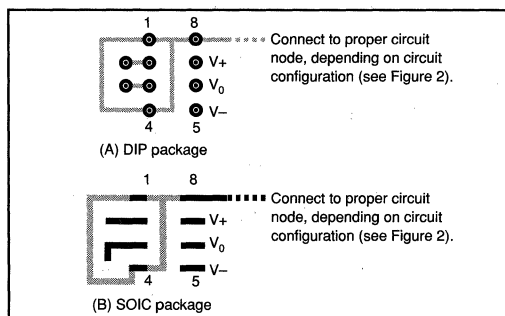


FIGURE 3. Suggested Board Layout for Input Guard.

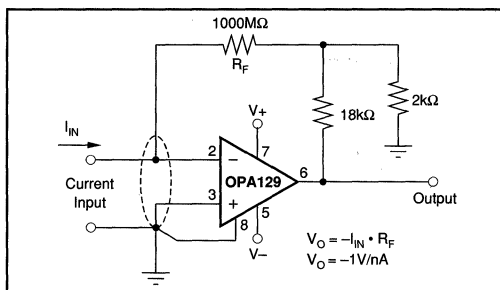


FIGURE 4. Current-to-Voltage Converter.

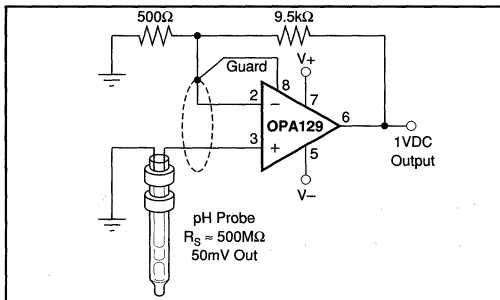


FIGURE 5. High Impedance ($10^{15}\Omega$) Amplifier.

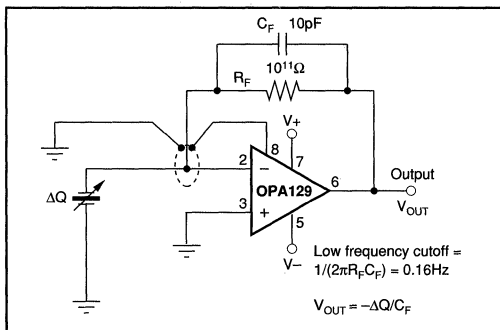


FIGURE 6. Piezoelectric Transducer Charge Amplifier.

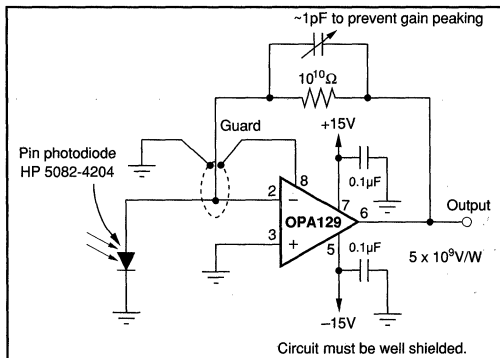
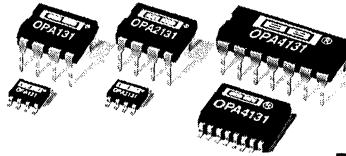


FIGURE 7. Sensitive Photodiode Amplifier.

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**OPA131
OPA2131
OPA4131**

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

OPA131/2131/4131

2

General Purpose FET-INPUT OPERATIONAL AMPLIFIERS

FEATURES

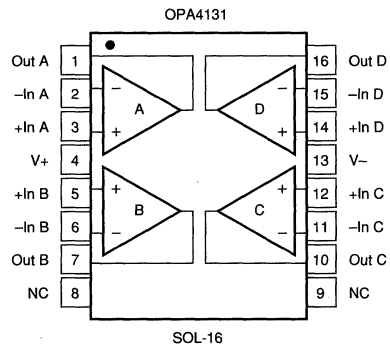
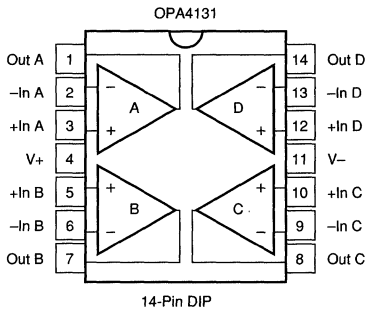
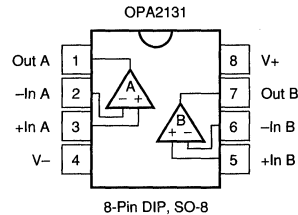
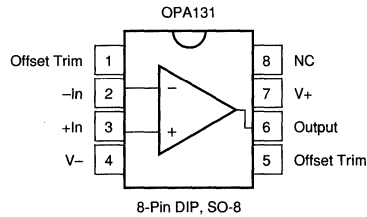
- FET INPUT: $I_b = 50\text{pA}$
- LOW OFFSET VOLTAGE: 2mV max
- WIDE SUPPLY RANGE: ± 4.5 to $\pm 18\text{V}$
- SLEW RATE: 10V/ μs
- WIDE BANDWIDTH: 4MHz
- SINGLE, DUAL, QUAD VERSIONS

DESCRIPTION

The OPA131 series of FET-input op amps provides high performance at low cost. Single, dual and quad versions in industry-standard pinouts allow cost-effective design options.

The OPA131 series offers excellent general purpose performance, including low offset voltage, drift, and good dynamic characteristics.

All are available in DIP and SOIC packages, specified for operation from -40°C to $+85^\circ\text{C}$.



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OPERATIONAL AMPLIFIERS

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PRELIMINARY SPECIFICATIONS

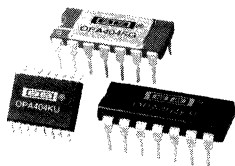
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITION	OPA131P, U OPA2131P, U OPA4131P, U			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage OPA131 single OPA2131 dual OPA4131 quad vs Temperature vs Power Supply	Operating Temperature Range $V_S = \pm 4.5\text{V to } \pm 18\text{V}$		± 0.5 ± 0.5 ± 0.5 ± 2 50	± 2 ± 3 ± 5	mV mV mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V/V}$
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		± 5 Doubles every 10°C ± 3	± 50 ± 50	pA pA
NOISE Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			25 15 12 12 0.6		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-mode Rejection	$V_{CM} = (V_+) - 1 \text{ to } (V_-) + 3\text{V}$	70	80		dB
INPUT IMPEDANCE Differential Common-Mode	$V_{CM} = -12 \text{ to } +12\text{V}$		$10^{13} \parallel 2$ $10^{13} \parallel 6$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-loop Voltage Gain	$V_O = -12 \text{ to } +12\text{V}$	90	112		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.1% 0.01% Total Harmonic Distortion	$G = -1, 10\text{V Step}$ $G = -1, 10\text{V Step}$ 1kHz		4 10 1.5 2.2 0.004		MHz $\text{V}/\mu\text{s}$ μs μs %
OUTPUT Voltage Output, Positive Negative Short-Circuit Current		(V_+) -3 (V_-) +3	(V_+) -2.5 (V_-) +2.5 ± 25		V V mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	± 4.5	± 15 ± 1.5	± 18 ± 1.75	V V mA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ_{JA}		-40 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$

NOTES: (1) High-speed test at $T_J = 25^\circ\text{C}$.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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OPA404

OPA404

2

OPERATIONAL AMPLIFIERS

Quad High-Speed Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/μs
- LOW OFFSET: ±750μV max
- LOW BIAS CURRENT: ±4pA max
- LOW SETTLING: 1.5μs to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

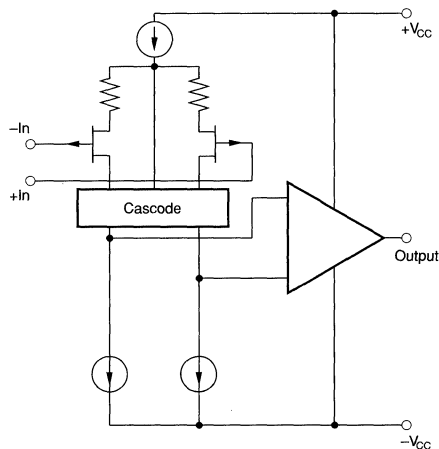
The OPA404 is a high performance monolithic *Difet*[®] (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET[®] amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet[®], Burr-Brown Corp.
BIFET[®], National Semiconductor Corp.

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU ⁽¹⁾			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_b = 10\text{Hz to } 10\text{kHz}$ $f_b = 0.1\text{Hz to } 10\text{Hz}$ Current: $f_b = 0.1\text{Hz to } 10\text{Hz}$ $f_o = 0.1\text{Hz thru } 20\text{kHz}$			32			*			*		$\text{nV}/\sqrt{\text{Hz}}$
				19			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				15			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				12			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				1.4			*		*		μVrms
				0.95			*		*		$\mu\text{Vp-p}$
				12			*		*		fA, p-p
			0.6			*		*		fA/ $\sqrt{\text{Hz}}$	
OFFSET VOLTAGE Input Offset Voltage KP, KU Average Drift KP, KU Supply Rejection KP, KU Channel Separation	$V_{CM} = 0\text{VDC}$		± 260	$\pm 1\text{mV}$		*	± 750		*	*	μV μV
	$T_A = T_{MIN}$ to T_{MAX}		± 3	$\pm 2.5\text{mV}$		*			*	*	$\mu\text{V}/^\circ\text{C}$
	$\pm V_{CC} = 12\text{V to } 18\text{V}$	80	100		86	*		*	*	*	dB
	100Hz, $R_L = 2\text{k}\Omega$	76	100			*		*	*	*	dB
				125			*		*	*	dB
BIAS CURRENT Input Bias Current KP, KU	$V_{CM} = 0\text{VDC}$		± 1	± 8		*	± 4		*	*	pA pA
			± 1	± 12		*			*	*	
OFFSET CURRENT Input Offset Current KP, KU	$V_{CM} = 0\text{VDC}$		0.5	8		*	4		*	*	pA pA
			0.5	12		*			*	*	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$			*			*	*	$\Omega \parallel \text{pF}$
			$10^{14} \parallel 3$			*			*	*	$\Omega \parallel \text{pF}$
VOTAGE RANGE Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10.5	$+13, -11$		*	*		*	*		V dB dB
		88	100		92	*		*	*		
		84	100			*		*	*		
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	88	100		92	*		*	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100	4	6.4		5	*		*	*		MHz
	20Vp-p, $R_L = 2\text{k}\Omega$		570			*		*	*		kHz
	$V_o = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	24	35		28	*		*	*		V/ μs
	Gain = -1, $R_L = 2\text{k}\Omega$		0.6			*		*	*		μs
	$C_L = 100\text{ pF}$, 10V Step		1.5				*		*		μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$	± 11.5	$+13.2, -13.8$		*	*		*	*		V
	$V_o = \pm 10\text{VDC}$	± 5	± 10		*	*		*	*		mA
	1MHz, Open Loop		80			*		*	*		Ω
	Gain = +1		1000			*		*	*		pF
		± 10	± 27	± 40	*	*	*	*	*	*	mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent			± 15			*			*		VDC
		± 5		± 18	*	*	*	*	*	*	VDC
	$I_o = 0\text{mADC}$		9	10		*	*	*	*	*	mA
TEMPERATURE RANGE Specification KP, KU Operating KP, KU Storage KP, KU θ Junction-Ambient KP, KU	Ambient Temperature	-25		+85	*	*		-55		+125	$^\circ\text{C}$
		0		+70		*					$^\circ\text{C}$
	Ambient Temperature	-55		+125	*	*		*	*	*	$^\circ\text{C}$
		-25		+85		*					$^\circ\text{C}$
	Ambient Temperature	-65		+150	*	*		*	*	*	$^\circ\text{C}$
		-40		+125		*					$^\circ\text{C}$
			100			*			*		$^\circ\text{C}/\text{W}$
		120/100								$^\circ\text{C}/\text{W}$	

*Specifications same as OPA404AG.

NOTE: (1) OPA404KU may be marked OPA404U.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE											
Specification Range KP, KU	Ambient Temperature	-25 0		+85 +70	*		*	-55		+125	°C °C
INPUT OFFSET VOLTAGE											
Input Offset Voltage KP, KU	$V_{CM} = 0\text{VDC}$		± 450 ± 1	2mV ± 3.5		*	$\pm 1.5\text{mV}$		± 550	$\pm 2.5\text{mV}$	μV mV
Average Drift KP, KU			± 3 ± 5			*			*		$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
Supply Rejection		75	96		80	*		70	93		dB
BIAS CURRENT											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 32	± 200		*	± 100		± 500	$\pm 5\text{nA}$	pA
OFFSET CURRENT											
Input Offset Current	$V_{CM} = 0\text{VDC}$		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE											
Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10 82 80	$\pm 12.7, -10.6$ 99 99		*	*		± 10 80	$+12.6, -10.5$ 88		V dB dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT											
Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 11.5 ± 5 ± 8	$\pm 12.9, -13.8$ ± 9 ± 20	± 50	*	*	*	± 11 *	$+12.7, -13.8$ ± 8 *		V mA mA
POWER SUPPLY											
Current, Quiescent	$I_O = 0\text{mADC}$		9.3	10.5		*	*		9.4	11	mA

* Specification same as OPA404AG.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA404KP	14-Pin Plastic DIP	0°C to +70°C
OPA404KU ⁽¹⁾	16-Pin Plastic SOIC	0°C to +70°C
OPA404AG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404BG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404SG	14-Pin Ceramic DIP	-55°C to +125°C

NOTE: (1) OPA404KU may be marked OPA404U.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA404KP	14-Pin Plastic DIP	010
OPA404KU ⁽²⁾	16-Pin Plastic SOIC	211
OPA404AG	14-Pin Ceramic DIP	169
OPA404BG	14-Pin Ceramic DIP	169
OPA404SG	14-Pin Ceramic DIP	169

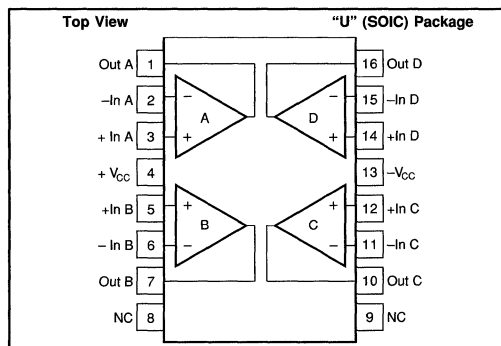
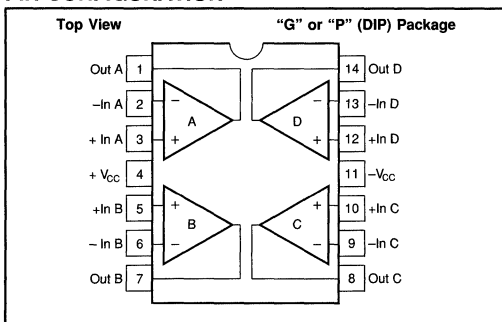
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

ABSOLUTE MAXIMUM RATINGS

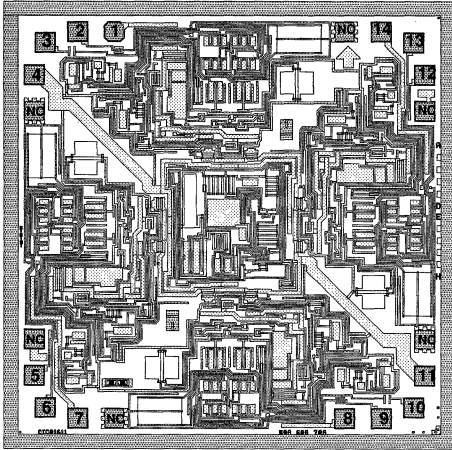
Supply	$\pm 18\text{VDC}$	Operating Temperature Range	P, U = -25°C/+85°C, G = -55°C/+125°C
Internal Power Dissipation ⁽¹⁾	1000mW	Lead Temperature (soldering, 10s)	300°C
Differential Input Voltage ⁽²⁾	$\pm 36\text{VDC}$	SOIC (soldering, 3s)	+260°C
Input Voltage Range ⁽²⁾	$\pm 18\text{VDC}$	Output Short-Circuit Duration ⁽³⁾	Continuous
Storage Temperature Range	P, U = -40°C/+125°C, G = -65°C/+150°C	Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JC} = 30^\circ\text{C}/\text{W}$ or $\theta_{JA} = 120^\circ\text{C}/\text{W}$. (2) For supply voltages less than $\pm 18\text{VDC}$ the absolute maximum input voltage is equal to: $18\text{V} > V_{IN} > -V_{CC} - 8\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

PIN CONFIGURATION



DICE INFORMATION



OPA404 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Output A	8	Output C
2	-Input A	9	-Input C
3	+Input A	10	+Input C
4	+V _{CC}	11	-V _{CC}
5	+Input B	12	+Input D
6	-Input B	13	-Input D
7	Output B	14	Output D

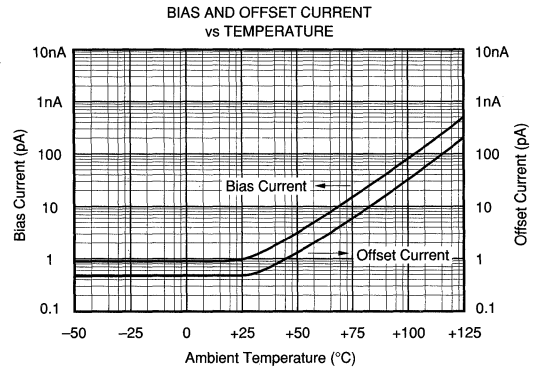
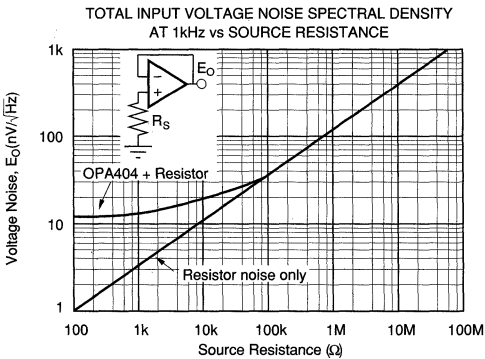
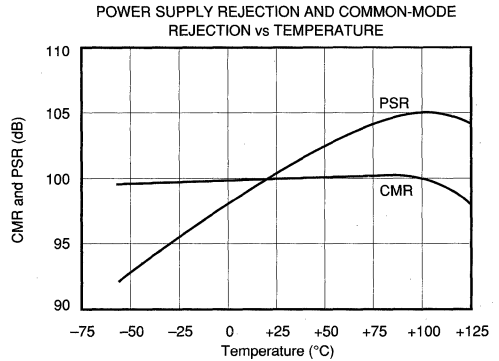
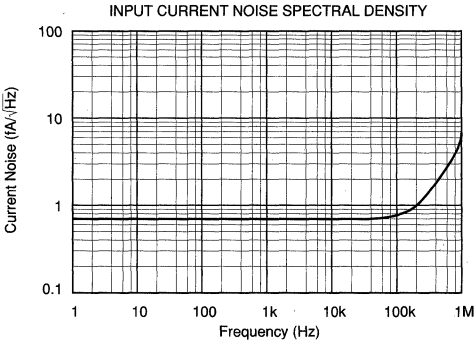
Substrate Bias: -V_{CC}
 NC: No connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	108 x 108 ±5	2.74 x 2.74 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

TYPICAL PERFORMANCE CURVES

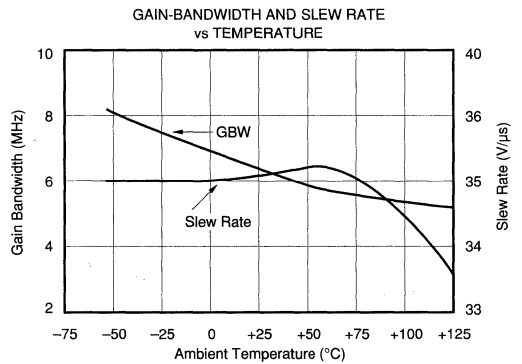
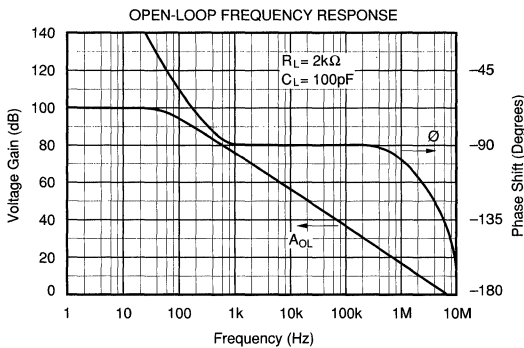
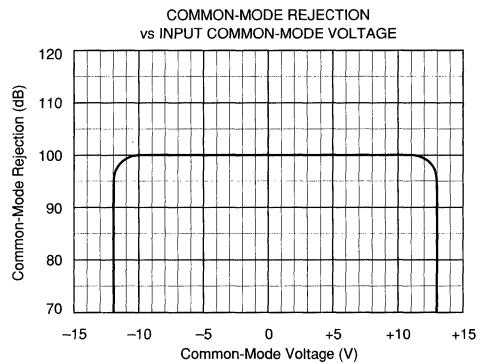
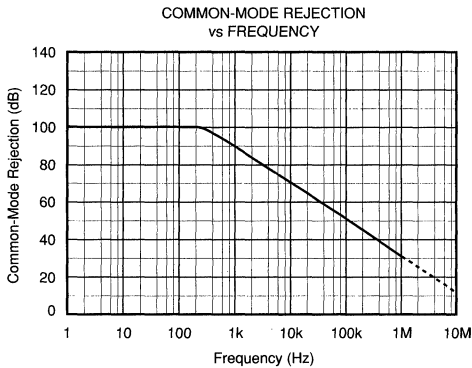
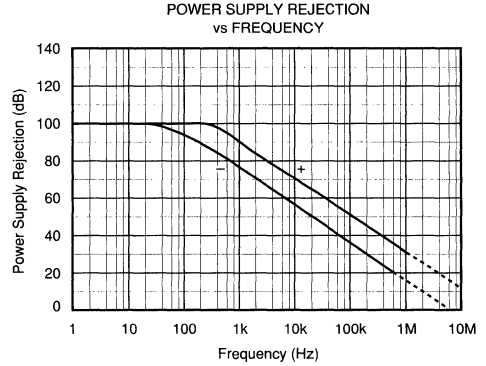
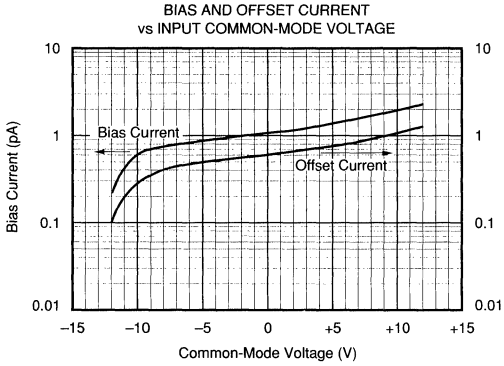
T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

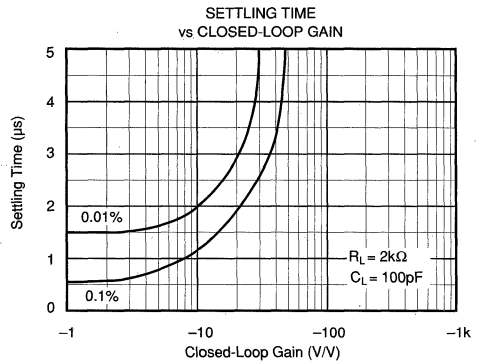
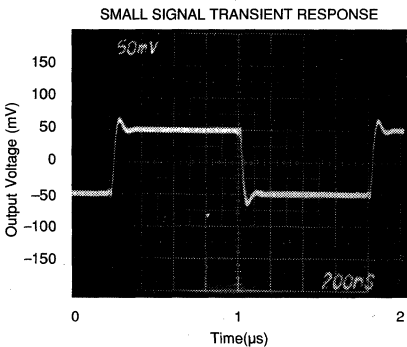
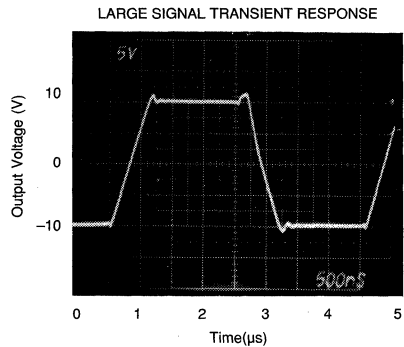
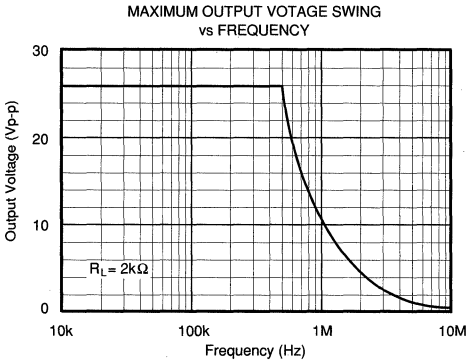
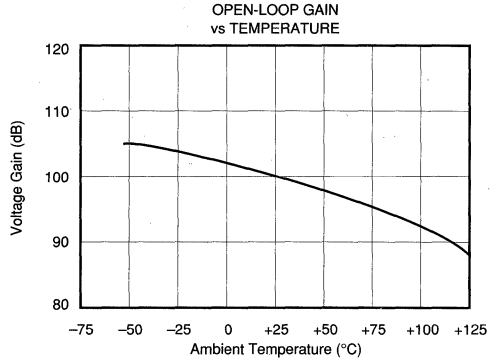
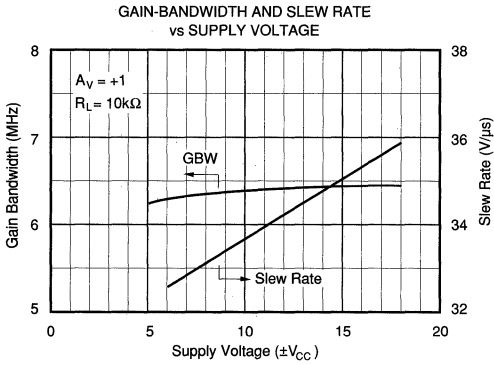
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

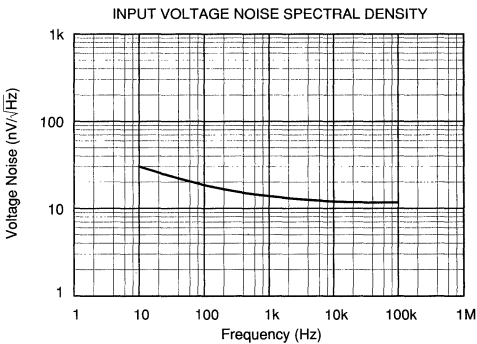
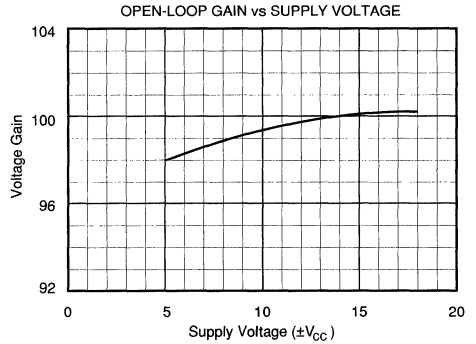
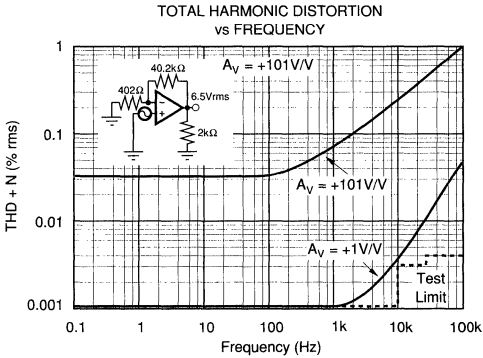
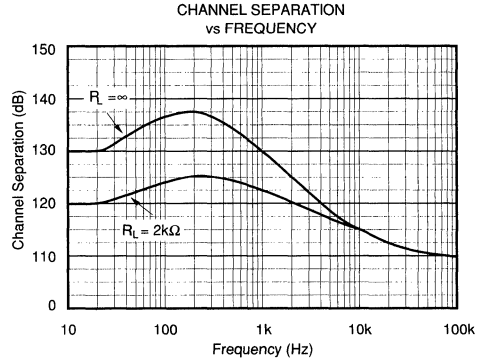
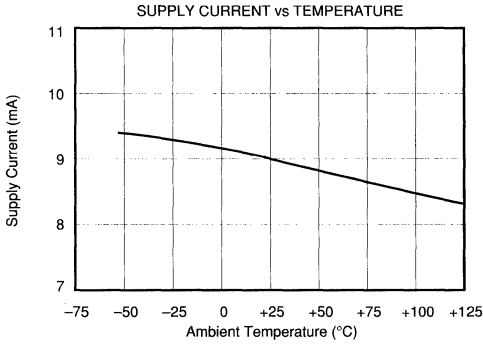
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

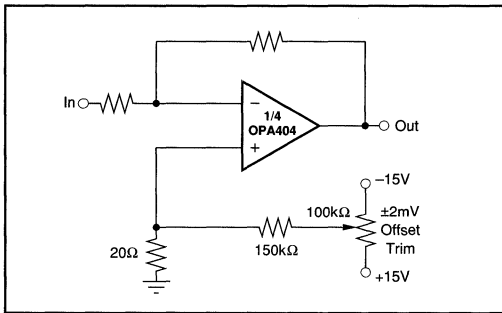


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA404 requires input current limiting resistors only if its input voltage is greater than 8 volts more negative than $-V_{CC}$. A 10kΩ series resistor will limit the input current to a safe value with up to $\pm 15V$ input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

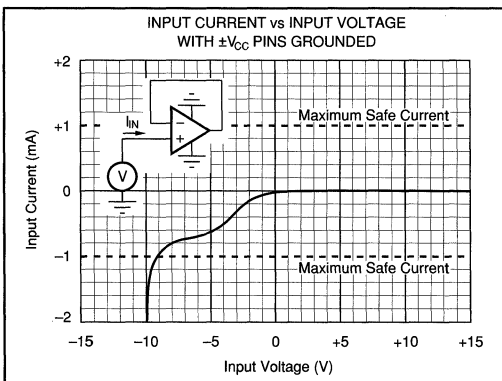


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low-impedance point which is at the signal input potential. (See Figure 3).

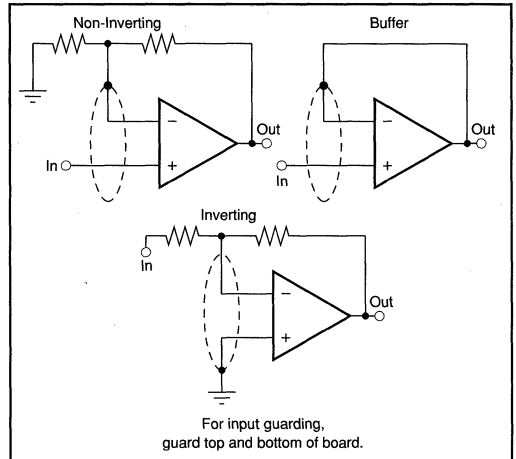


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

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If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF[®], baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA404 is not compromised by common-mode voltage.

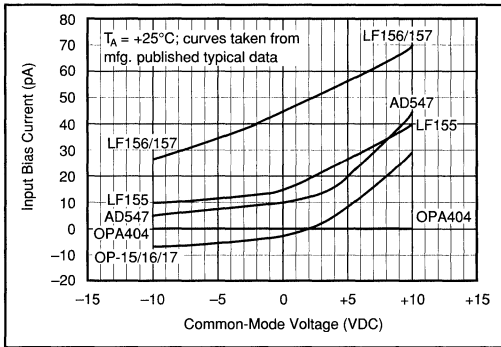


FIGURE 4. Input Bias Current vs Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

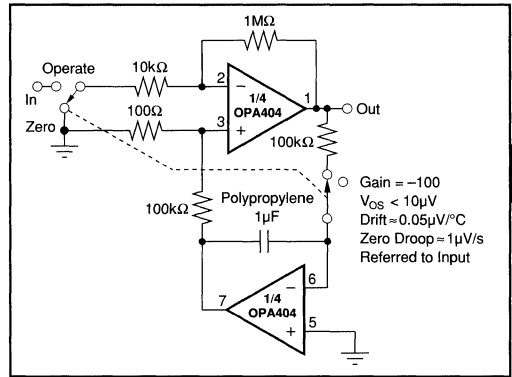


FIGURE 5. Auto-Zero Amplifier.

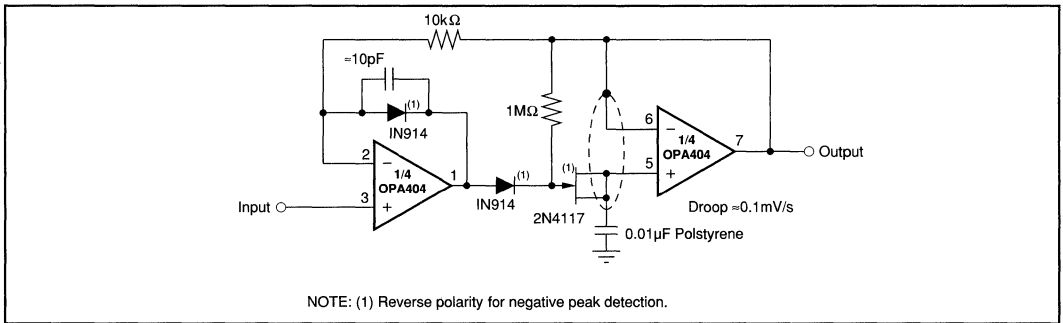


FIGURE 6. Low-Droop Positive Peak Detector.

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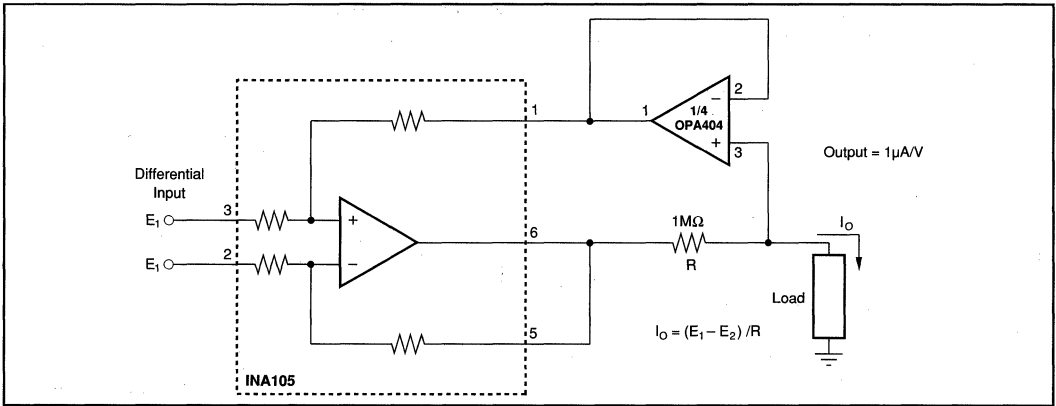


FIGURE 7. Voltage-Controlled Microamp Current Source.

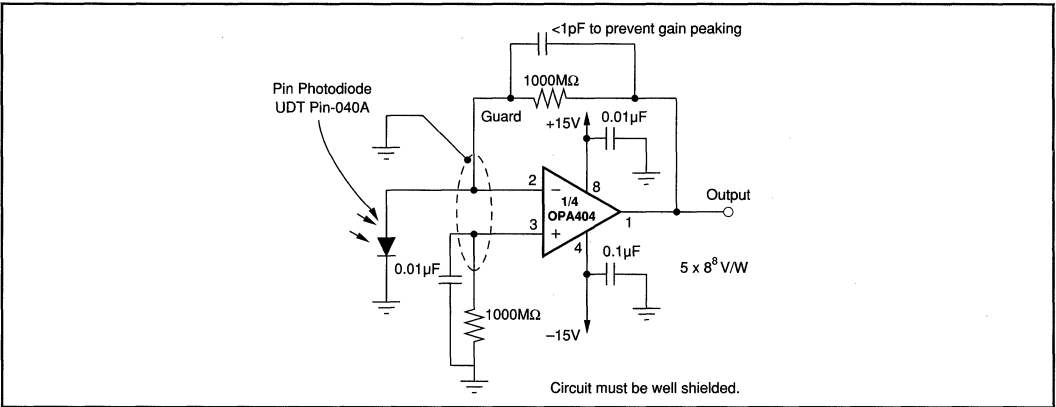


FIGURE 8. Sensitive Photodiode Amplifier.

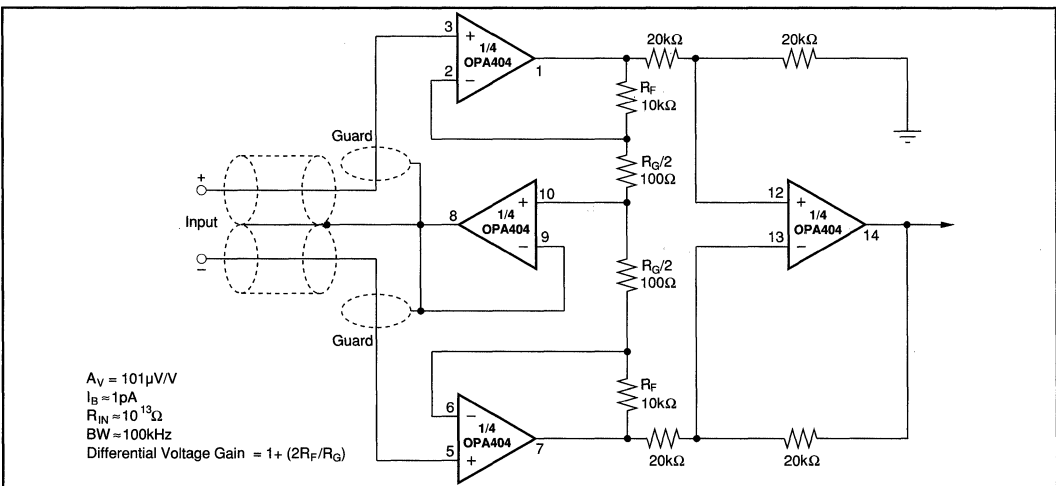


FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

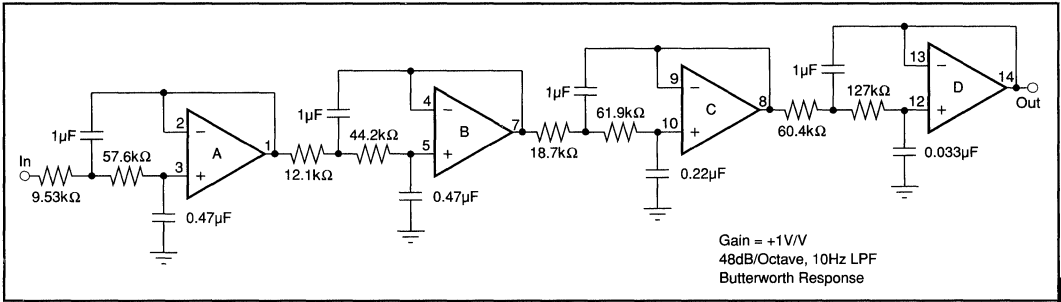


FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

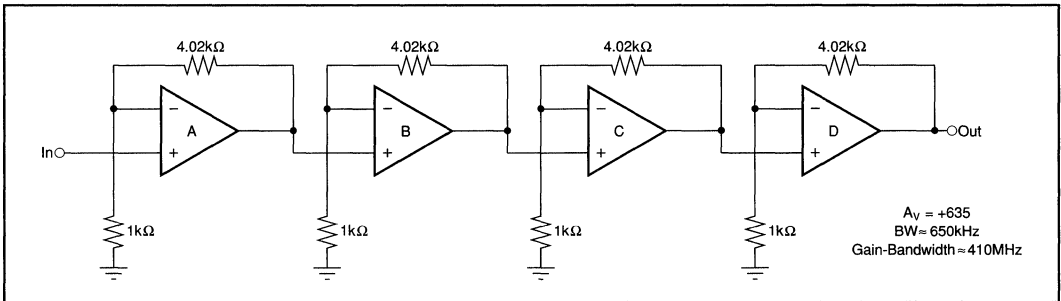
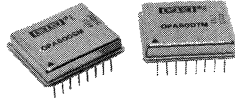


FIGURE 11. Wide-Band Amplifier.

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OPA600
ABRIDGED DATA SHEET
For Additional Technical
Information, Request
PDS-672.

Fast-Settling Wideband OPERATIONAL AMPLIFIER

FEATURES

- **FAST SETTLING:** 80ns to $\pm 0.1\%$
100ns to $\pm 0.01\%$
- **FULL DIFFERENTIAL FET INPUT**
- **-25°C to +85°C AND**
-55°C to +125°C TEMPERATURE
RANGES
- **$\pm 10V$ OUTPUT: 200mA**
- **GAIN BANDWIDTH PRODUCT: 5GHz**

DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to $\pm 0.01\%$ accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes an FET input stage to give low input bias current. Its DC stability over temperature is outstanding. The slew rate exceeds $400V/\mu s$. All of this combines to form an outstanding amplifier for large and small signals.

High accuracy with fast settling time is achieved by using a high open-loop gain which provides the accuracy at high frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External frequency compensation allows the user to optimize

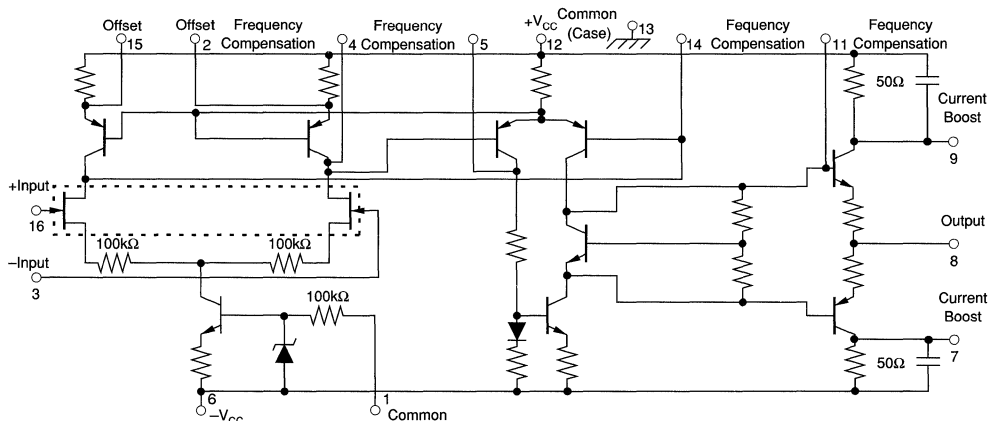
APPLICATIONS

- **VOLTAGE CONTROLLED OSCILLATOR DRIVER**
- **LARGE SIGNAL, WIDEBAND DRIVERS**
- **HIGH SPEED D/A CONVERTER OUTPUT AMPLIFIER**
- **VIDEO PULSE AMPLIFIER**

the settling time for various gains and load conditions.

The OPA600 is useful in a broad range of video, high speed test circuits and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

The OPA600 is specified over the industrial temperature range (OPA600BM, CM) and military temperature range (OPA600SM, TM). The OPA600 is housed in a welded, hermetic metal package.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15VDC$ and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA600CM, TM ⁽¹⁾			OPA600BM, SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT								
Voltage	$R_L = 2k\Omega$	± 10			*			V
	$R_L = 50\Omega^{(2)}$	± 9			*			V
Current	$R_L = 50\Omega^{(2)}$	± 180	± 200		*	*		mA
Current Pulse	$R_L = 50\Omega^{(3)}$	± 180	± 200		*	*		mA
Resistance	Open Loop DC		75			*		Ω
Short-Circuit Current	To COMMON Only, $t_{MAX} = 1s^{(4)}$		250	300		*	*	mA
DYNAMIC RESPONSE								
Settling Time ⁽⁵⁾ : to $\pm 0.01\%$ ($\pm 1mV$) to $\pm 0.1\%$ ($\pm 10mV$) to $\pm 1\%$ ($\pm 100mV$)	$\Delta V_{OUT} = 10V$		100	125		*	*	ns
	$\Delta V_{OUT} = 10V$		80	105		*	*	ns
	$\Delta V_{OUT} = 10V$		70	95		*	*	ns
Gain-Bandwidth Product (open-loop)	$C_C = 0pF, G = 1V/V$		150			*	*	MHz
	$C_C = 0pF, G = 10V/V$		500			*	*	MHz
	$C_C = 0pF, G = 100V/V$		1.5			*	*	GHz
	$C_C = 0pF, G = 1000V/V$		5			*	*	GHz
	$C_C = 0pF, G = 10,000V/V$		10			*	*	GHz
Bandwidth ($-3dB$ small signal) ⁽⁶⁾	$G = +1V/V$		125			*	*	MHz
	$G = -1V/V$		90			*	*	MHz
	$G = -10V/V$		95			*	*	MHz
	$G = -100V/V$		20			*	*	MHz
	$G = -1000V/V$		6			*	*	MHz
Full Power Bandwidth	$V_{OUT} = \pm 5V, G = -1V/V, C_C = 3.3pF, R_L = 100\Omega$		16			*	*	MHz
Slew Rate	$V_{OUT} = \pm 5V, G = -1000V/V, C_C = 0pF, R_L = 100\Omega$		400	500		*	*	V/ μs
	$V_{OUT} = \pm 5V, G = -1V/V^{(4)}$			440		*	*	V/ μs
Phase Margin	$G = -1V/V, C_C = 3.3pF$		40			*	*	Degrees
GAIN								
Open-Loop Voltage Gain	$f = DC, R_L = 2k\Omega, T_A = +25^\circ C$	86	94		*	*		dB
INPUT								
Offset Voltage ⁽⁷⁾	$T_A = +25^\circ C$		± 1	± 4		± 2	± 5	mV
	$T_A = -25^\circ C$ to $+85^\circ C$			± 5			± 10	mV
	$T_A = -55^\circ C$ to $+125^\circ C$			± 6			± 15	mV
Offset Voltage Drift	$T_A = -25^\circ C$ to $+85^\circ C$			± 20			± 80	$\mu V/^\circ C$
	$T_A = -55^\circ C$ to $+125^\circ C$			± 20			± 100	$\mu V/^\circ C$
Bias Current	$T_A = +25^\circ C$		-20	-100		*	*	pA
	$T_A = -25^\circ C$ to $+125^\circ C$		-20	-100		*	*	nA
Offset Current	$T_A = +25^\circ C$		20			*	*	pA
	$T_A = -55^\circ C$ to $+125^\circ C$		20			*	*	nA
Power Supply Rejection Ratio	$V_{CC} = \pm 15V, \pm 1V$		200	500		*	*	$\mu V/V$
Common-Mode Voltage Range		-10		+7	*	*	*	V
Common-Mode Rejection Ratio	$V_{CM} = -5V$ to $+5V$	60	80		*	*	*	dB
Impedance	Differential and Common-Mode		$10^{11} \parallel 2$			*	*	$\Omega \parallel pF$
Voltage Noise	10kHz Bandwidth		20			*	*	nV/\sqrt{Hz}
POWER SUPPLY								
Rated (V_{CC})			± 15			*	*	VDC
Operating Range		± 9		± 16		*	*	VDC
Quiescent Current			± 30	± 38		*	*	mA
TEMPERATURE RANGE (Ambient)								
Operating: BM, CM		-25		+85	*	*	*	$^\circ C$
SM, TM		-55		+125	*	*	*	$^\circ C$
Storage		-65		+150	*	*	*	$^\circ C$
θ_{JC} , (junction-to-case)			30			*	*	$^\circ C/W$
θ_{CA} , (case-to-ambient)			35			*	*	$^\circ C/W$

*Specification same as OPA600CM, TM.

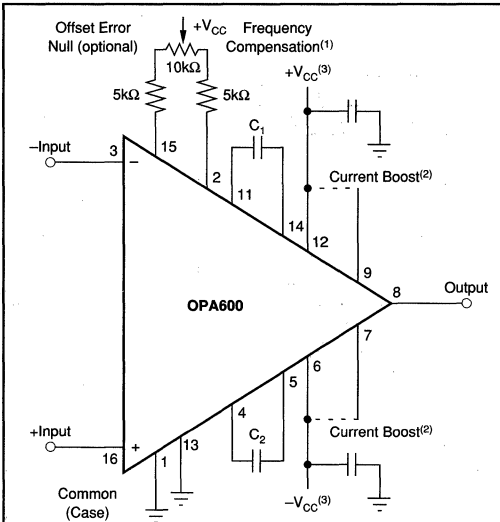
NOTES: (1) BM, CM grades: $-25^\circ C$ to $+85^\circ C$. SM, TM grades: $-55^\circ C$ to $+125^\circ C$. (2) Pin 9 connected to $+V_{CC}$, pin 7 connected to $-V_{CC}$. Observe power dissipation ratings. (3) Pin 9 and 7 open. Single pulse $t = 100ns$. Observe power dissipation ratings. (4) Pin 9 and 7 open. See section on Current Boost. (5) $G = -1V/V$. Optimum setting time and slew rate achieved by individually compensating each device. Refer to section on Compensation. (6) Frequency compensation as discussed in section on Compensation. (7) Adjustable to zero.

OPA600

OPERATIONAL AMPLIFIERS

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CONNECTION DIAGRAM



NOTES: (1) Refer to Figure 4 for recommended frequency compensation. (2) connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information. (3) Bypass each power supply lead as close as possible to the amplifier pins. A 1 μ F CS13 tantalum capacitor is recommended. (4) There is no internal connection. An external connection may be made. (5) It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, +V _{CC} to -V _{CC}	±17V
Power Dissipation, At T _{case} +125°C ⁽²⁾	1.6W
Input Voltage: Differential	±V _{CC}
Common-Mode	±V _{CC}
Output Short Circuit Duration to Common	<5s
Temperature: pin (soldering, 20s)	+300°C
Junction ⁽¹⁾ , T _J	+175°C
Temperature Range: Storage	-65°C to +150°C
Operating (case)	-55°C to +125°C

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE (°C)	VOLTAGE OFFSET DRIFT (μV/°C)
OPA600BM	-25 to +85	±80
OPA600CM	-25 to +85	±20
OPA600SM	-55 to +125	±100
OPA600TM	-25 to +125	±20

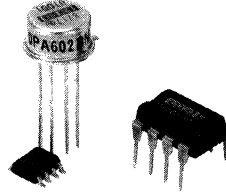
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA600CM	16-Pin	142
OPA600BM	16-Pin	142
OPA600SM	16-Pin	142
OPA600TM	16-Pin	142

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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OPA602

High-Speed Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/ μ s
- LOW OFFSET: $\pm 250\mu$ V max
- LOW BIAS CURRENT: ± 1 pA max
- FAST SETTLING TIME: 1 μ s to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

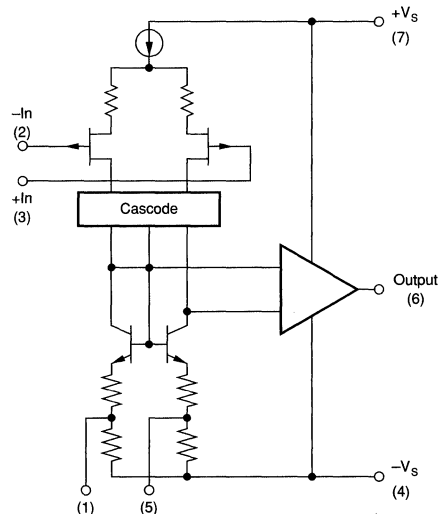
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic *Difet* (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1k Ω resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. *Difet* construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet[®] Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_S = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/AP/AU			OPA602BM/SM/BP			OPA602CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_b = 10\text{Hz}$ to 10kHz $f_b = 0.1\text{Hz}$ to 10Hz Current: $f_b = 0.1\text{Hz}$ to 10Hz $f_b = 0.1\text{Hz}$ to 20kHz			*			23		*		$\text{nV}/\sqrt{\text{Hz}}$	
			*			19		*		$\text{nV}/\sqrt{\text{Hz}}$	
			*			13		*		$\text{nV}/\sqrt{\text{Hz}}$	
			*			12		*		$\text{nV}/\sqrt{\text{Hz}}$	
			*			1.4		*		μVrms	
			*			0.95		*		$\mu\text{Vp-p}$	
			*			12		*		$\text{fA}/\sqrt{\text{p}}$	
		*			0.6		*		$\text{fA}/\sqrt{\text{Hz}}$		
OFFSET VOLTAGE Input Offset Voltage: M Package P Package U Package Over Specified Temperature M Package P, U Packages Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$		± 300	± 1000		± 150	± 500		± 100	± 250	μV mV mV
			1	2		0.5	1				
			± 550			± 250	± 1000		± 200	± 500	μV mV
		$T_A = T_{MIN}$ to T_{MAX} $\pm V_S = 12\text{V}$ to 18V	70	± 1.5	± 15	80	± 0.75	± 1.5	86	*	± 2
BIAS CURRENT Input Bias Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{VDC}$		± 2	± 10		± 1	± 2		± 0.5	± 1	pA pA pA
				± 20	± 500		± 20	± 200		± 10	± 100
OFFSET CURRENT Input Offset Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{VDC}$		1	10		0.5	2		0.5	1	pA pA pA
			20	500		20	200		10	100	
						200	1000				
INPUT IMPEDANCE Differential Common-Mode			*			$10^{13} \parallel 1$			*		$\Omega \parallel \text{pF}$
			*			$10^{14} \parallel 3$			*		$\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection		*	*		± 10.2	+13, -11		*	*		V dB
	$V_{IN} = \pm 10\text{VDC}$	75	*		88	100		92	*		
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 1\text{k}\Omega$	75	*		88	100		92	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100 20Vp-p, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ Gain = -1, $R_L = 1\text{k}\Omega$ $C_L = 500\text{pF}$, 10V Step	3.5	*		4	6.5		5	*		MHz kHz V/ μs μs μs
		20	*		24	35		28	*		
			*			0.6			*		
			*			1.0			*		
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 1\text{k}\Omega$	± 11	*		± 11.5	+12.9, -13.8		*	*		V mA Ω pF mA
	$V_O = \pm 10\text{VDC}$ 1MHz, Open Loop Gain = +1	*	*		± 15	± 20		*	*		
			*			80		*	*		
		± 25	*		± 30	1500		*	*		
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent Over Specified Temperature			*			± 15			*		VDC VDC mA mA
		*	*		± 5	3	± 18	*	*		
	$I_O = 0\text{mA}$		*			4	4		*	*	
			*			3.5	4.5		*	*	
TEMPERATURE RANGE Specification SM Grade Operating: M Package P, U Packages Storage: M Package P, U Packages θ_{JA}	Ambient Temperature	*	*		-25 -55		+85 +125	*	*		$^\circ\text{C}$ $^\circ\text{C}$
	Ambient Temperature	*	*		-55		+125	*	*		$^\circ\text{C}$
	Ambient Temperature	-25	*	+85	-25		+85				$^\circ\text{C}$
	Ambient Temperature	*	*		-65		+150	*	*		$^\circ\text{C}$
	Ambient Temperature	-40	*	+125	-40		+125				$^\circ\text{C}$ $^\circ\text{C}/\text{W}$
			*			200			*		

* Same specifications as OPA602BM.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation ($T_j \leq +175^\circ\text{C}$)	1000mW
Differential Input Voltage	Total V_s
Input Voltage Range	$\pm V_s$
Storage Temperature Range	
M Package	-65°C to +150°C
P and U Packages	-40°C to +125°C
Operating Temperature Range	
M Package	-55°C to +125°C
P and U Packages	-25°C to +85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION⁽¹⁾

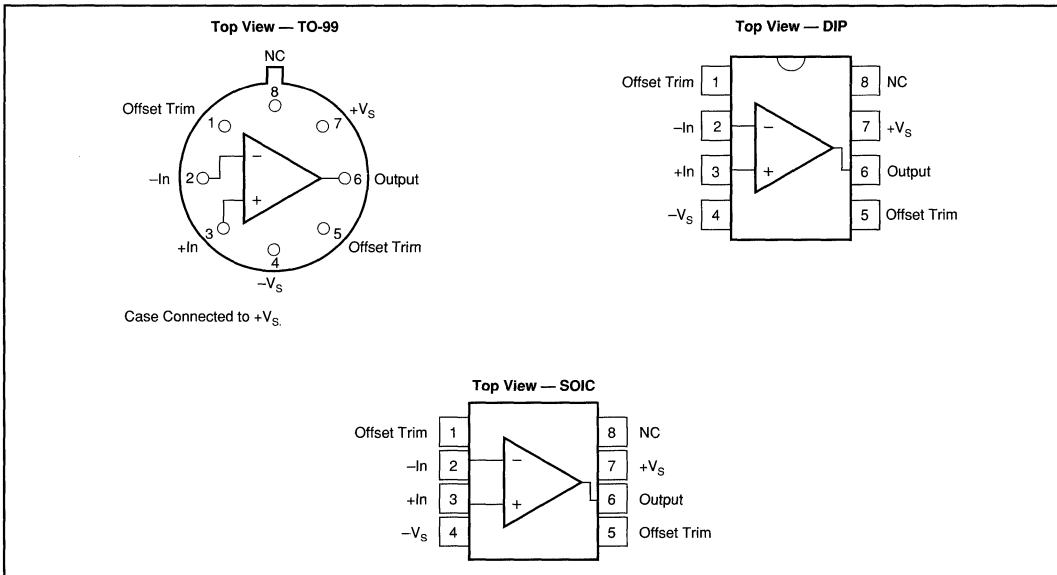
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA602AM	TO-99	001
OPA602BM	TO-99	001
OPA602CM	TO-99	001
OPA602SM	TO-99	001
OPA602AP	Plastic DIP	006
OPA602BP	Plastic DIP	006
OPA602AU	Plastic SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (μV) AT 25°C
OPA602AM	TO-99	-25 to +85°C	±1000
OPA602BM	TO-99	-25 to +85°C	±500
OPA602CM	TO-99	-25 to +85°C	±250
OPA602SM	TO-99	-55 to +125°C	±500
OPA602AP	Plastic DIP	-25 to +85°C	±2000
OPA602BP	Plastic DIP	-25 to +85°C	±1000
OPA602AU	Plastic SOIC	-25 to +85°C	±3000

PIN CONFIGURATIONS



OPA602

2

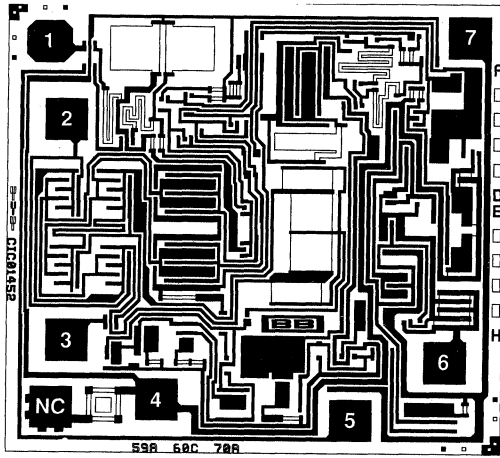
OPERATIONAL AMPLIFIERS

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DICE INFORMATION



OPA602 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _s
5	Offset Trim
6	Output
7	+V _s

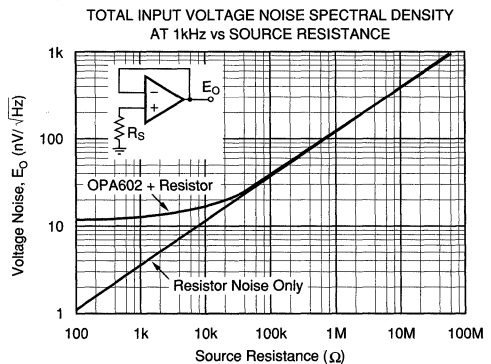
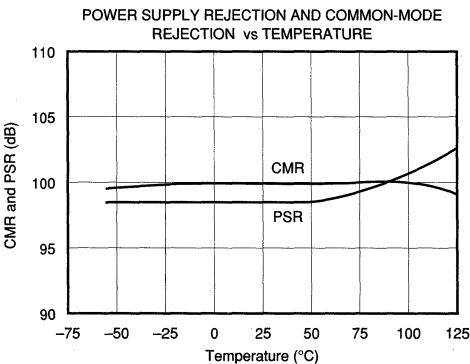
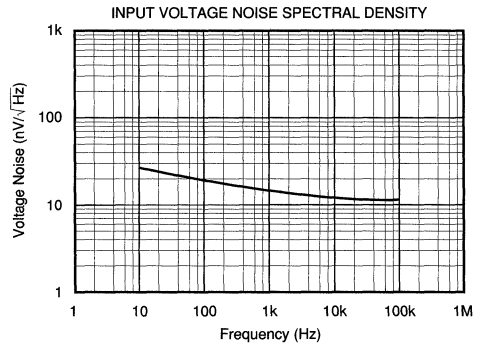
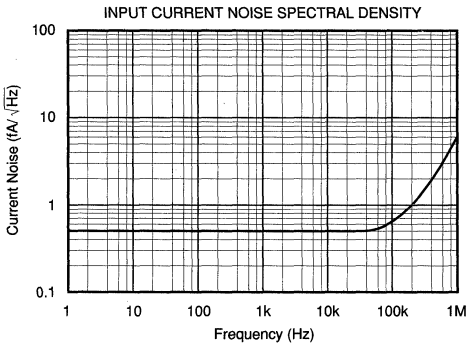
Substrate Bias: -V_s
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 58 ±5	1.60 x 1.47 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		36

TYPICAL PERFORMANCE CURVES

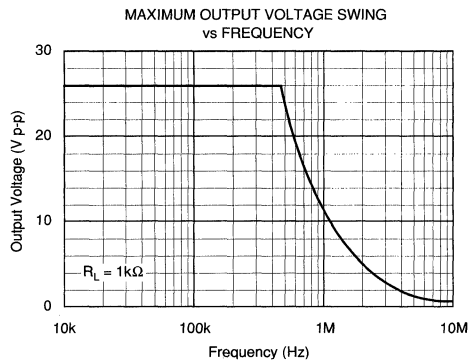
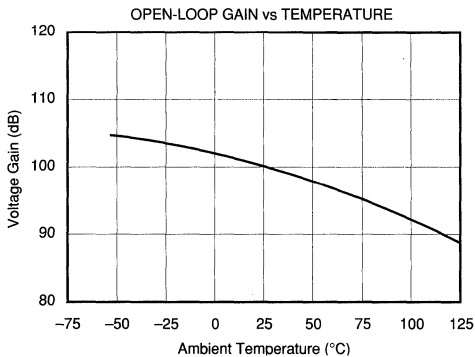
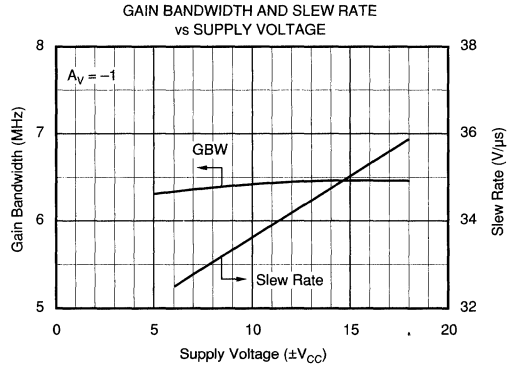
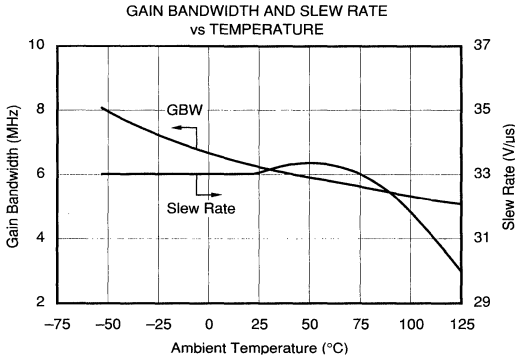
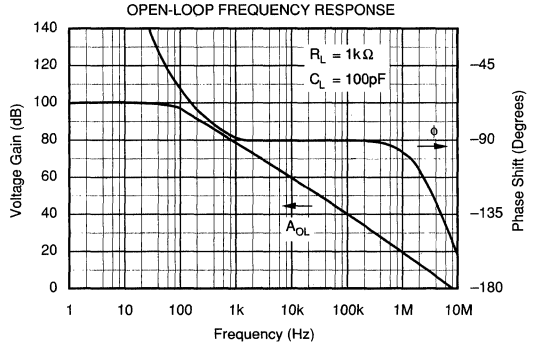
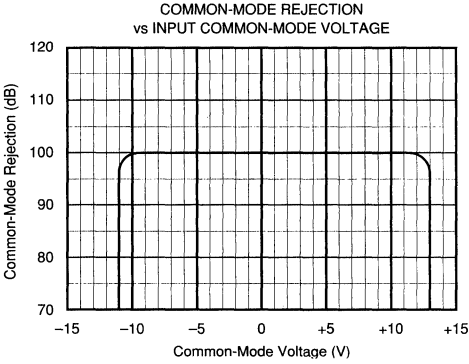
T_A = +25°C, V_s = ±15VDC unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

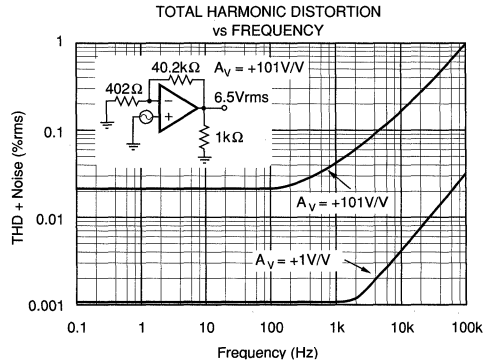
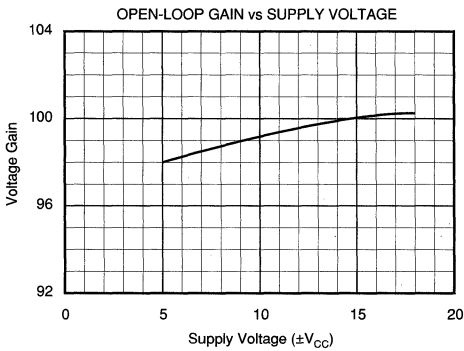
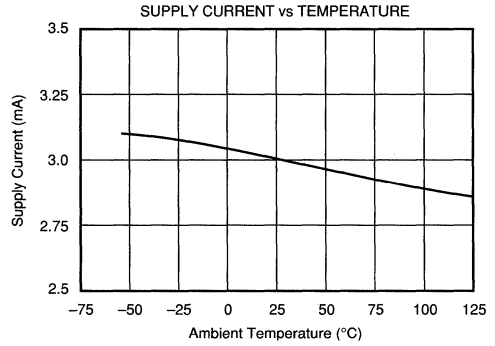
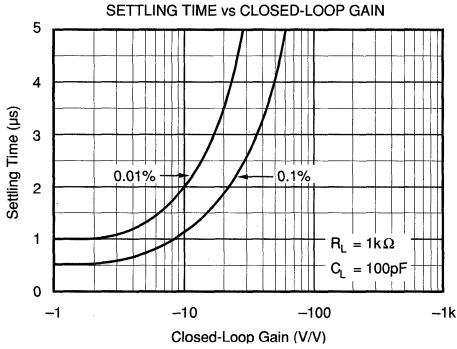
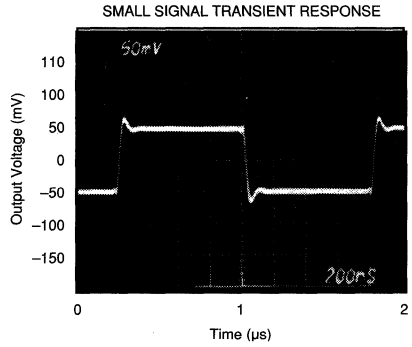
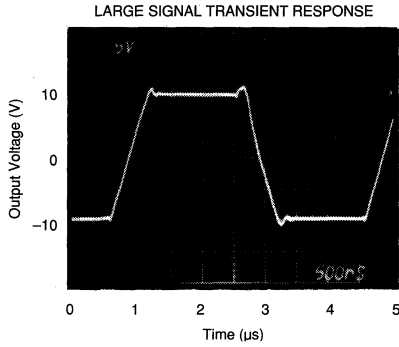
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

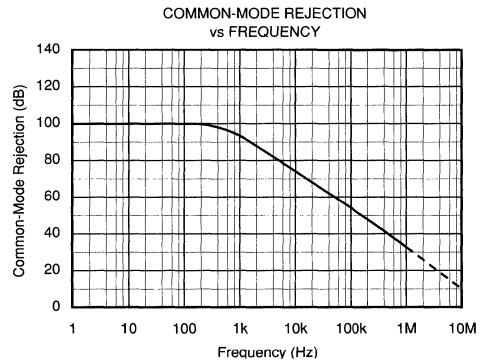
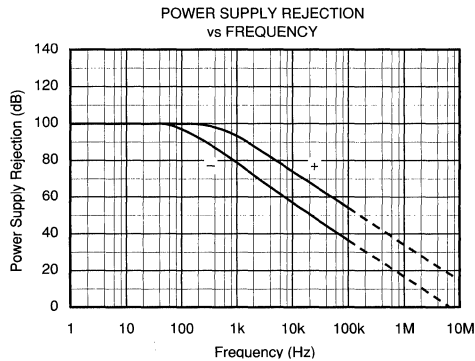
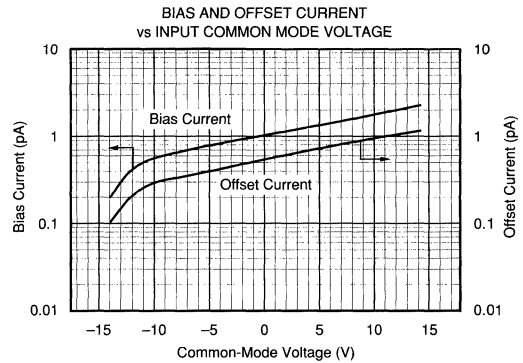
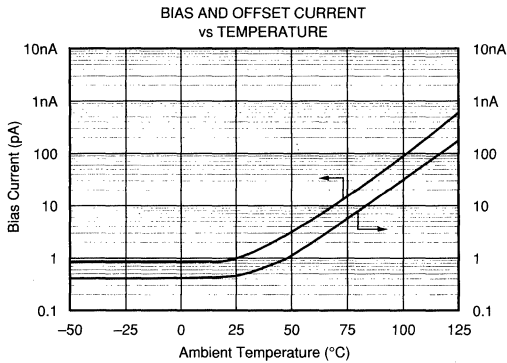
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high speed amplifiers. But with any high speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1 μF ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional 1.0 μF tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board “guard” pattern (Figure 1) is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and de-ionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

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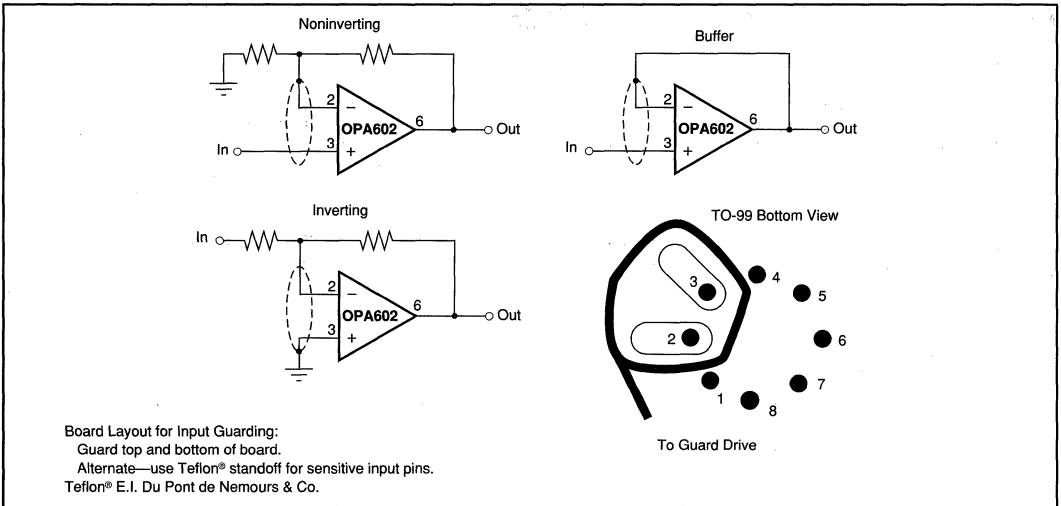


FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS

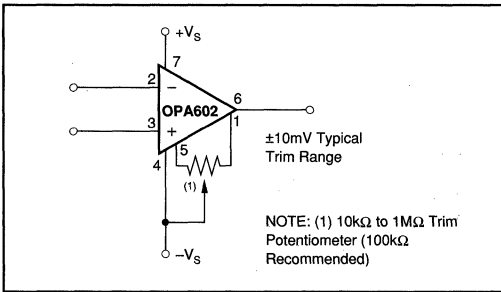


FIGURE 2. Offset Voltage Trim.

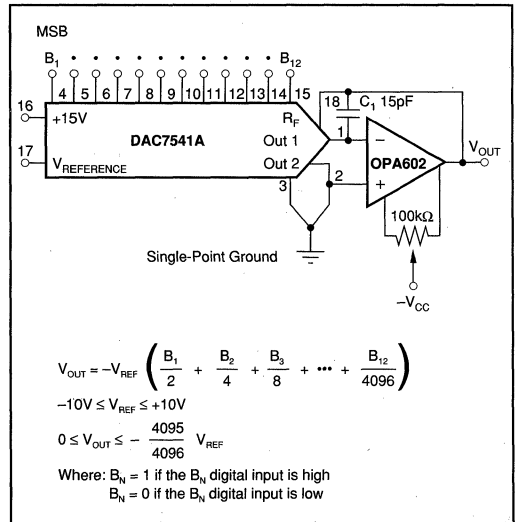


FIGURE 3. Voltage Output D/A Converter.

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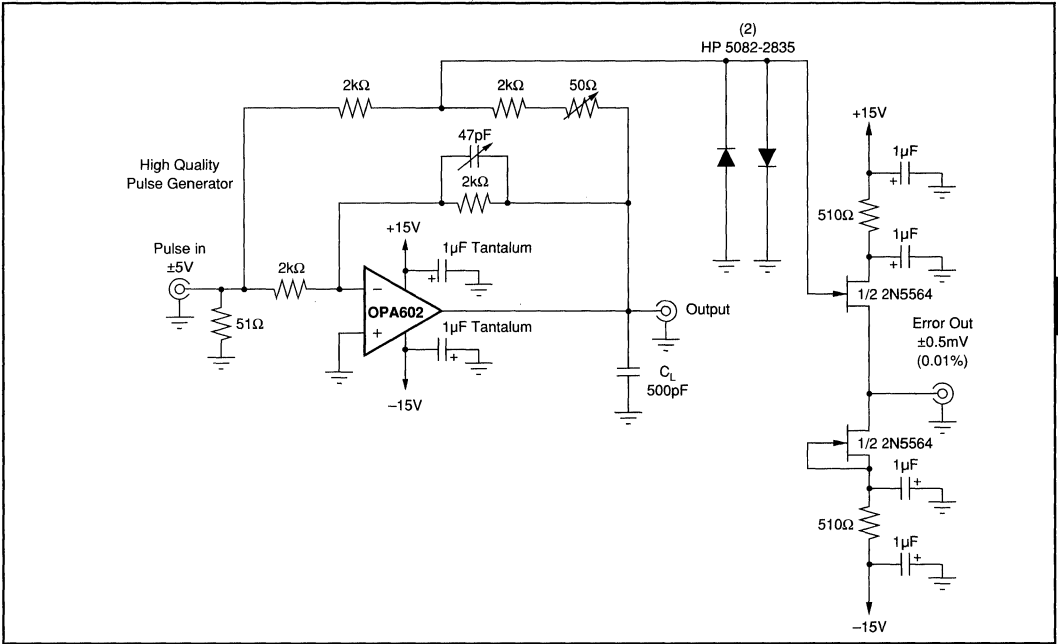
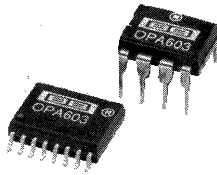


FIGURE 4. Settling Time and Slew Rate Test Circuit.

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OPA603

High Speed, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- BANDWIDTH: 100MHz, $G = 1$ to 10
- SLEW RATE: 1000V/ μ s
- FAST SETTLING TIME: 50ns to 0.1%
- WIDE SUPPLY RANGE: ± 4.5 to ± 18 V
- HIGH OUTPUT CURRENT: ± 150 mA peak
- 8-PIN PLASTIC MINI-DIP PACKAGE
- SOL-16 SURFACE-MOUNT PACKAGE

APPLICATIONS

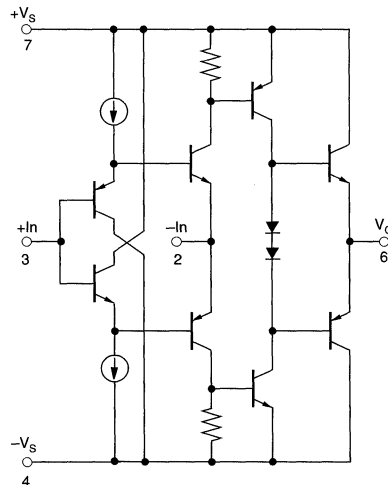
- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- SONAR, ULTRASOUND CIRCUITRY
- ATE PIN DRIVERS
- LINE DRIVERS
- FAST DATA ACQUISITION
- WAVEFORM GENERATORS

DESCRIPTION

The OPA603 is a high-speed current-feedback op amp with guaranteed specifications at both ± 5 V and ± 15 V power supplies. It can deliver full ± 10 V signals into 150 Ω loads with up to 1000V/ μ s slew rate. This allows it to drive terminated 75 Ω cables. With 150mA peak output current capability it is suitable for driving load capacitance or long lines at high speed.

In contrast with conventional op amps, the current-feedback approach provides nearly constant bandwidth and settling time over a wide range of closed-loop voltage gains.

The OPA603 is available in a plastic 8-pin dual-in-line and SOL-16 surface-mount packages, specified for the industrial temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS, $V_S = \pm 15V$

ELECTRICAL

$T_A = +25^\circ C$, $R_L = 150\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP/AU			UNITS
		MIN	TYP	MAX	
INPUT OFFSET VOLTAGE Initial vs Temperature vs Common-Mode Voltage vs Supply (tracking) Voltage vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 10V$ $V_S = \pm 12V$ to $\pm 18V$ $ V_{SI} = 12V$ to $18V$	50 80 55	8 60 85 60	5	mV $\mu V/^\circ C$ dB dB
+INPUT BIAS CURRENT Initial vs Temperature vs Common-Mode vs Supply (tracking) vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 10V$ $V_S = \pm 12V$ to $\pm 18V$ $ V_{SI} = 12V$ to $18V$		30 200 50 150	5 500 100 300	μA $nA/^\circ C$ nA/V nA/V nA/V
-INPUT BIAS CURRENT Initial vs Temperature vs Common-Mode vs Supply (tracking) vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 10V$ $V_S = \pm 12V$ to $\pm 18V$ $ V_{SI} = 12V$ to $18V$		300 200 300 1500	25 600 500 2000	μA $nA/^\circ C$ nA/V nA/V nA/V
INPUT IMPEDANCE +Input -Input			5 2 30 2		$M\Omega$ pF Ω pF
OPEN LOOP CHARACTERISTICS Transresistance Transcapacitance	$V_O = \pm 10V$	300	440 1.8		k Ω pF
OUTPUT CHARACTERISTICS Voltage Peak Current Short-Circuit Current ⁽²⁾ Output Resistance, Open-Loop	$R_L = 150\Omega$ $V_O = 0V$	± 10	± 12 150 250 70		V mA mA Ω
FREQUENCY RESPONSE Small-Signal Bandwidth ⁽³⁾ Gain Flatness, $\pm 0.5dB$ Full-Power Bandwidth Differential Gain Differential Phase	$G = +2$ $V_O = 20Vp-p$ $f = 4.43MHz$, $V_O = 1V$ $f = 4.43MHz$, $V_O = 1V$	70 35	160 75 10 0.03 0.025		MHz MHz MHz % Degrees
TIME DOMAIN RESPONSE Propagation Delay Rise and Fall Time Settling Time to 0.10% Slew Rate	$G = +2$ 10V Step		10 10 50 1000		ns ns ns V/ μs
DISTORTION 2nd Harmonic Distortion 3rd Harmonic Distortion	$G = +2$, $R_L = 100\Omega$, $f = 10MHz$ $V_O = 0.2Vp-p$ $V_O = 0.2Vp-p$	-60 -70	-65 -90		dBc dBc
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 21	± 18 ± 25	V V mA
TEMPERATURE RANGE Specification Storage		-25 -40		+85 +150	$^\circ C$ $^\circ C$
THERMAL RESISTANCE, $\theta_{JUNCTION-AMBIENT}$	Soldered to Printed Circuit		90		$^\circ C/W$

NOTES: (1) One power supply fixed at 15V; the other supply varied from 12V to 18V. (2) Observe power derating curve. (3) See bandwidth versus gain curve, Figure 5.

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SPECIFICATIONS, $V_S = \pm 5V$

ELECTRICAL

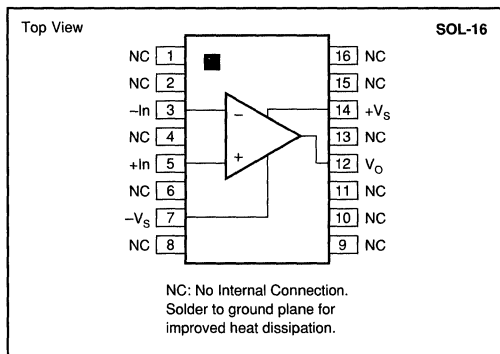
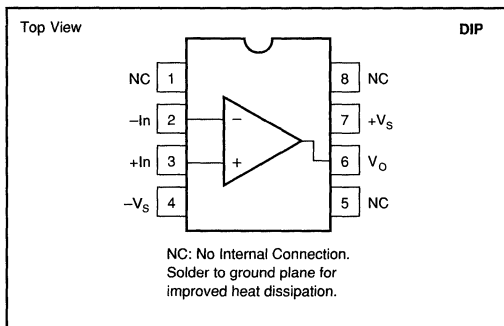
$T_A = +25^\circ C$, $R_L = 75\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA603AP/AU			UNITS
		MIN	TYP	MAX	
INPUT OFFSET VOLTAGE Initial vs Temperature vs Common-Mode vs Supply (tracking) vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 3V$ $V_S = \pm 4V$ to $\pm 6V$ $ V_S = 4V$ to $6V$		8	6	mV
		50	55		$\mu V/^\circ C$
		75	80		dB
		55	60		dB
+INPUT BIAS CURRENT Initial vs Temperature vs Common-Mode vs Supply (tracking) vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 3V$ $V_S = \pm 4V$ to $\pm 6V$ $ V_S = 4V$ to $6V$		30	5	μA
			350	600	nA/°C
			100	200	nA/V
			200	300	nA/V
-INPUT BIAS CURRENT Initial vs Temperature vs Common-Mode vs Supply (tracking) vs Supply (non-tracking) ⁽¹⁾	$V_{CM} = \pm 3V$ $V_S = \pm 4V$ to $\pm 6V$ $ V_S = 4V$ to $6V$		300	25	μA
			300	600	nA/°C
			500	700	nA/V
			2500	3000	nA/V
INPUT IMPEDANCE +Input -Input			3.3 2		M Ω pF
			30 2		Ω pF
OPEN LOOP CHARACTERISTICS Transresistance Transcapacitance	$V_O = \pm 2V$	225	330		k Ω
			2.4		pF
OUTPUT CHARACTERISTICS Voltage Peak Current Short-Circuit Current ⁽²⁾ Output Resistance, Open-Loop	$R_L = 75\Omega$ $V_O = 0V$	± 2	± 2.75		V
			150		mA
			250		mA
			80		Ω
FREQUENCY RESPONSE Small-Signal Bandwidth ⁽³⁾ Gain Flatness, $\pm 0.5dB$ Full-Power Bandwidth Differential Gain Differential Phase	G = +2 f = 4.43MHz, $V_O = 1V$, $R_L = 150\Omega$ f = 4.43MHz, $V_O = 1V$, $R_L = 150\Omega$		140		MHz
			65		MHz
			20		MHz
			0.03		%
			0.025		Degrees
TIME DOMAIN RESPONSE Propagation Delay Rise and Fall Time Settling Time to 0.10% Slew Rate	G = +2, $R_L = 100\Omega$		15		ns
			20		ns
			60		ns
			750		V/ μs
DISTORTION 2nd Harmonic Distortion 3rd Harmonic Distortion	G = +2, $R_L = 100\Omega$, f = 10MHz $V_O = 0.2Vp-p$ $V_O = 0.2Vp-p$		-67		dBc
			-78		dBc
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 5	± 18	V
				± 25	V
			± 21		mA
TEMPERATURE RANGE Specification Storage		-25		+85	°C
		-40		+150	°C
THERMAL RESISTANCE, $\theta_{JUNCTION-AMBIENT}$	Soldered to Printed Circuit		90		°C/W

NOTES: (1) One power supply fixed at 5V; the other supply varied from 4V to 6V. (2) Observe power derating curve. (3) See bandwidth versus gain curves, Figure 5.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Input Voltage Range	$\pm V_s$
Differential Input Voltage	$\pm 6V$
Power Dissipation	See derating curve
Operating Temperature	+100°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
(soldering SOL-16 package, 3s)	+260°C

ORDERING INFORMATION

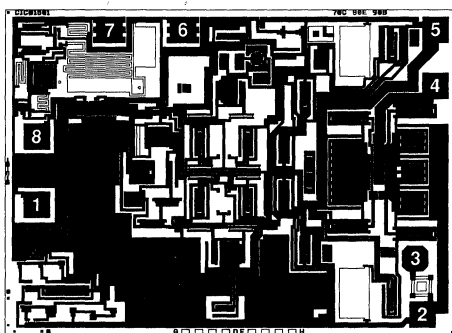
MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
OPA603AP	Plastic DIP	-25°C to +85°C
OPA603AU	SOL-16	-25°C to +85°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA603AP	Plastic DIP	006
OPA603AU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



OPA603 DIE TOPOGRAPHY

PAD	FUNCTION
1	Noninverting Input
2	$-V_s$
3	Laser Alignment
4	V_o (Output)
5	$+V_s$
6	RT (Trim Sense Point)
7	CE
8	(Compensation Capacitor) Inverting Input

Substrate Bias: Dielectrically Isolated.
Recommend tying to $+V_s$.

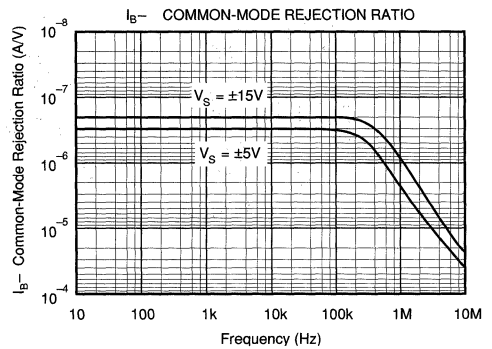
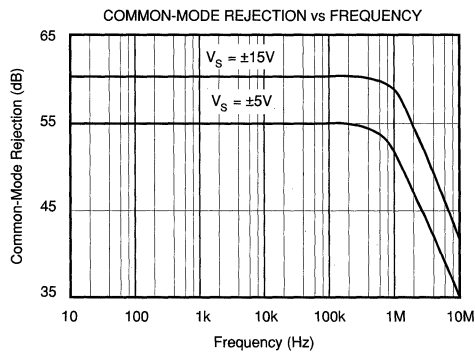
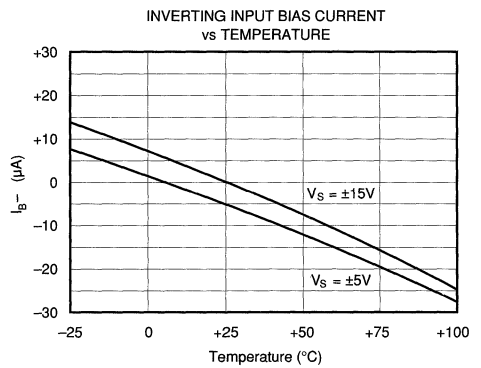
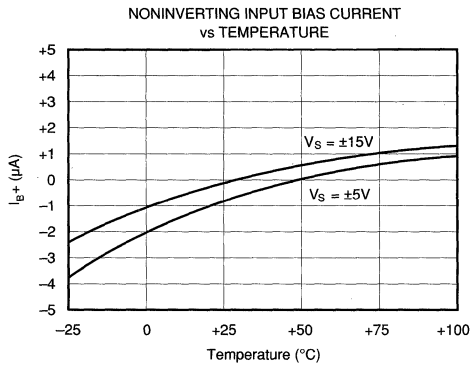
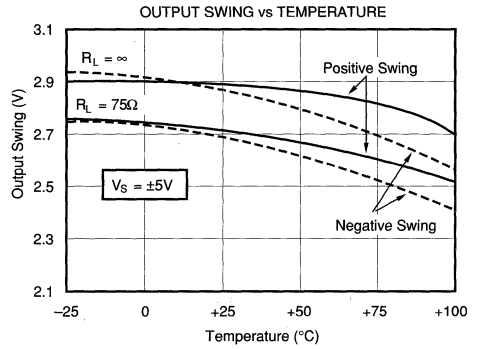
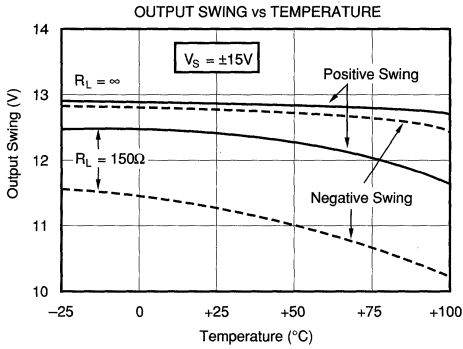
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	94 x 69 ± 5	2.39 x 1.75 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

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TYPICAL PERFORMANCE CURVES

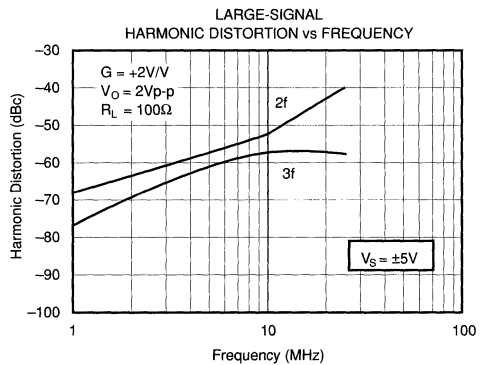
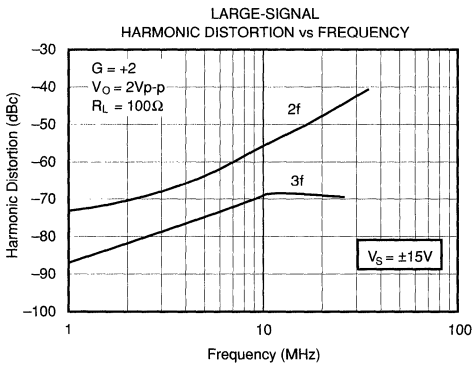
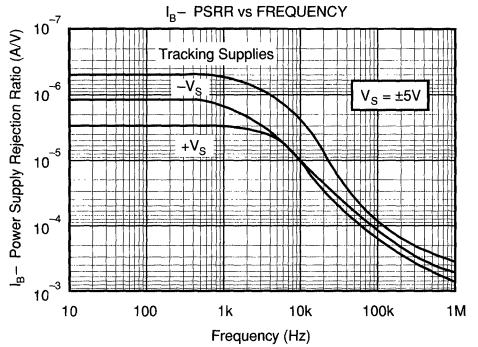
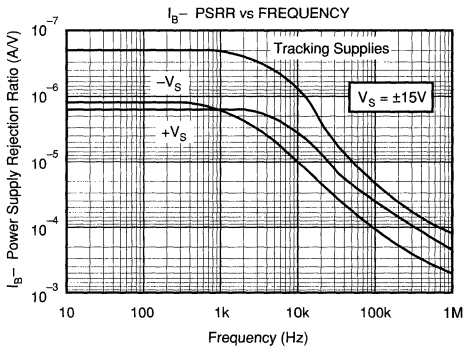
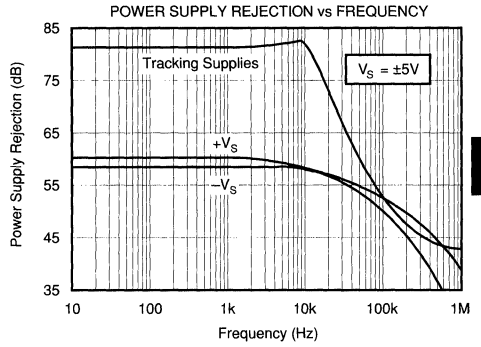
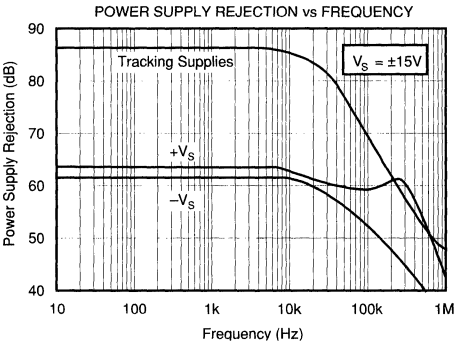
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

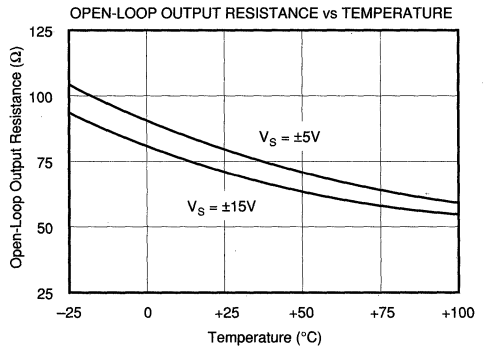
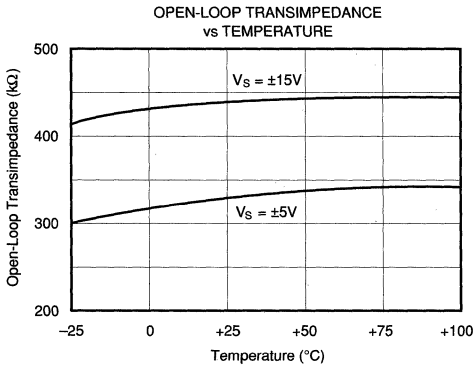
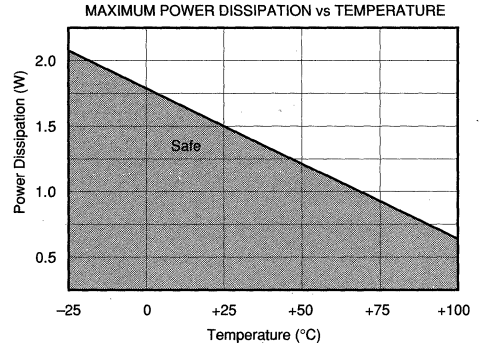
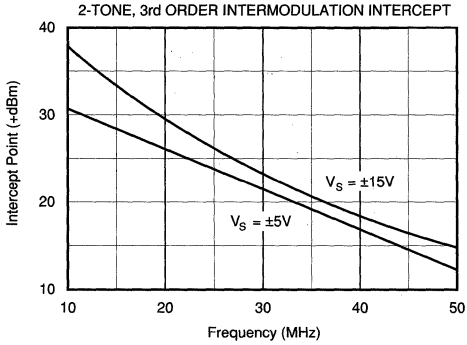
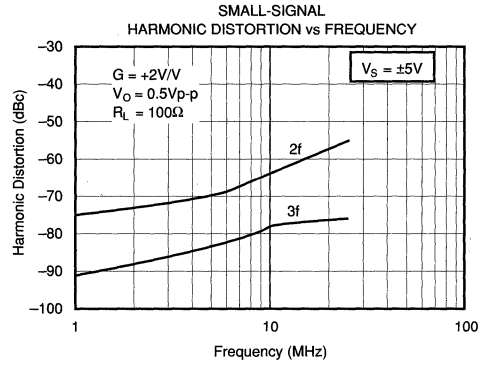
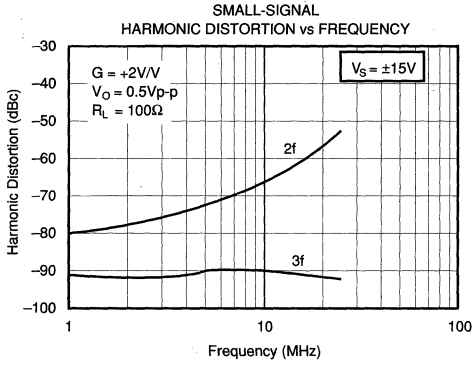
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

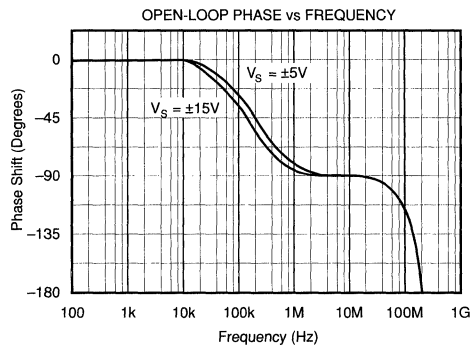
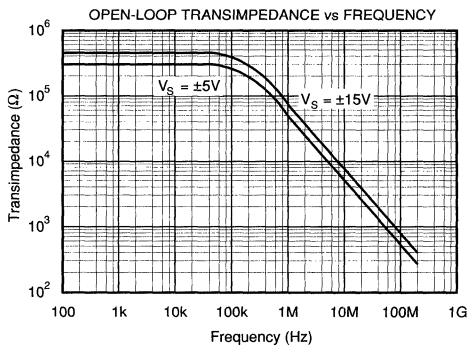
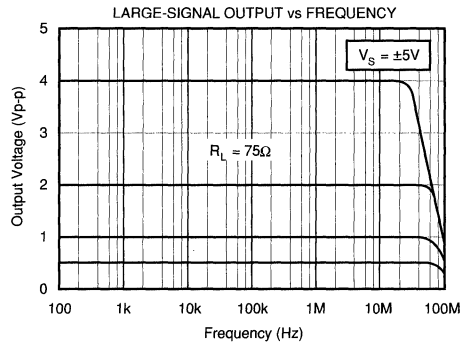
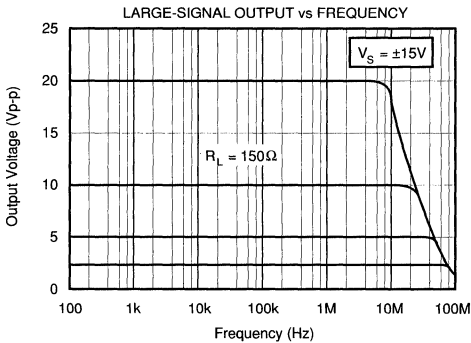
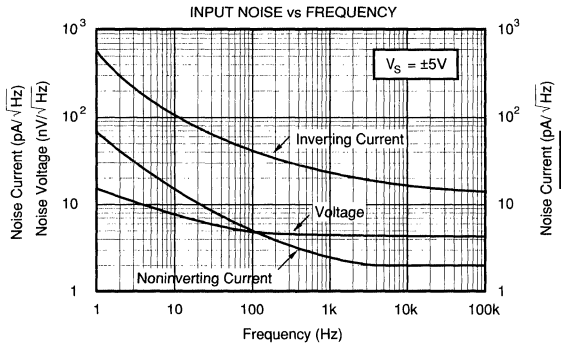
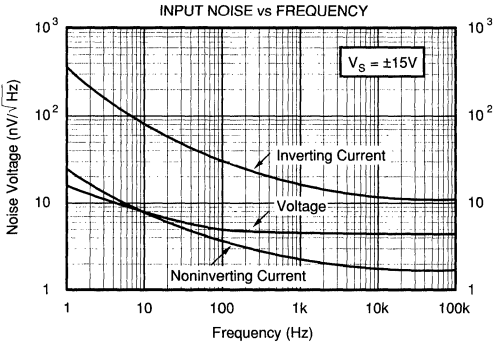
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ unless otherwise noted.

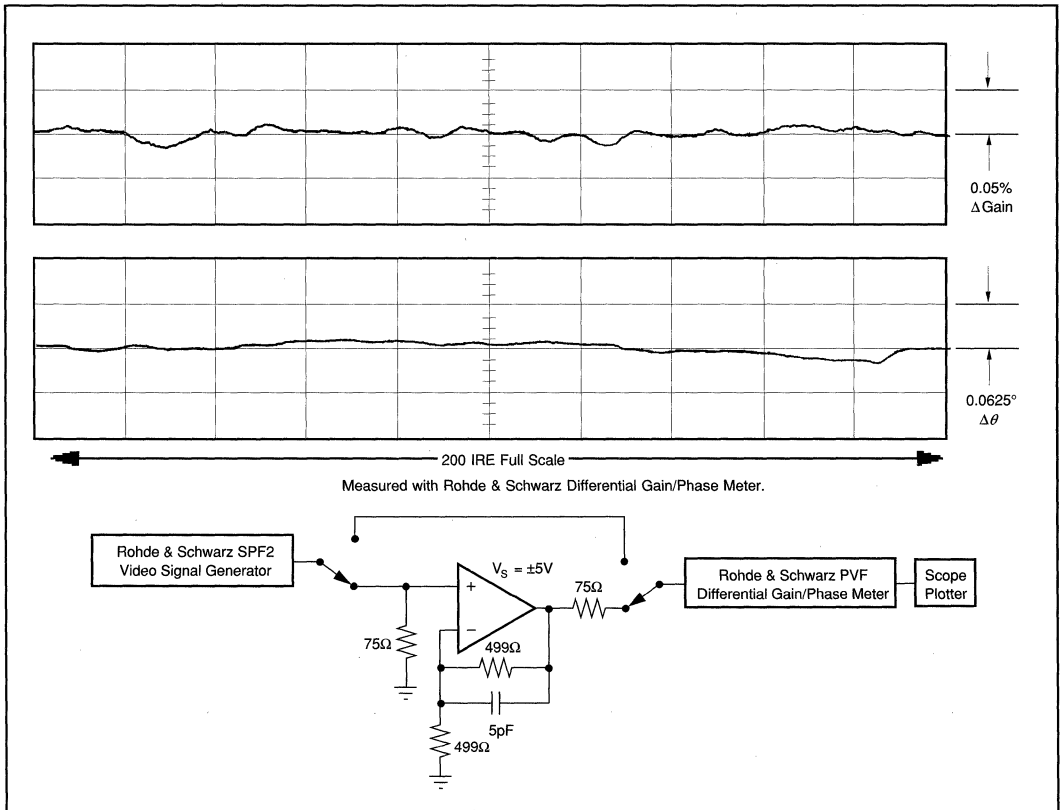
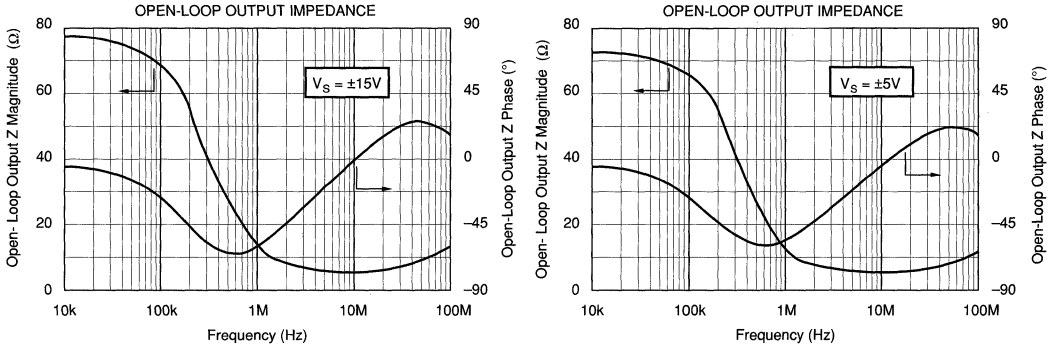


FIGURE 1. Video Differential Gain/Phase Performance.

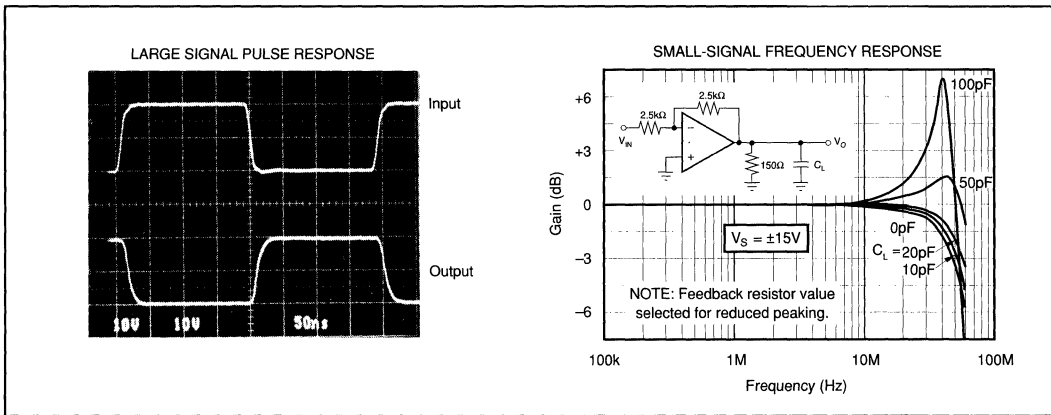


FIGURE 2. Dynamic Response, Inverting Unity-Gain.

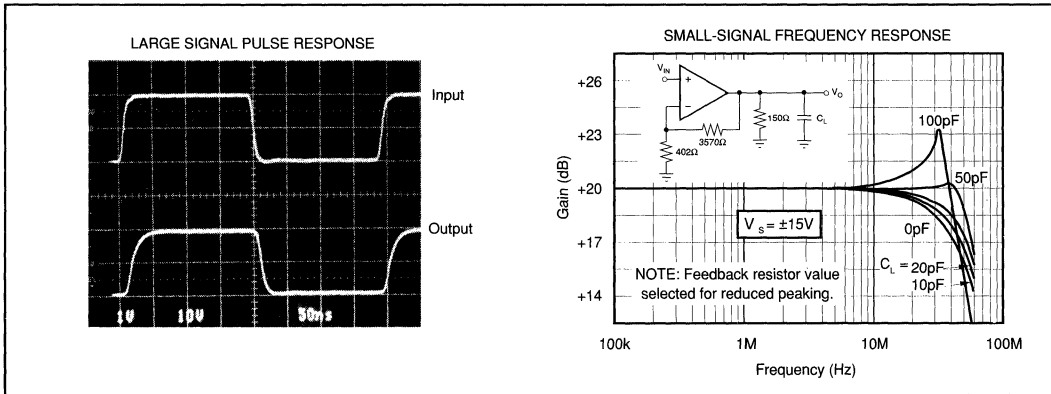


FIGURE 3. Dynamic Response, Gain = +10.

APPLICATIONS INFORMATION

For most circuit configurations, the OPA603 current-feedback op amp can be treated like a conventional op amp. As with a conventional op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response.

Feedback resistor values can be selected to provide a nearly constant closed-loop bandwidth over a very wide range of gain. This is in contrast to a conventional op amp where circuit bandwidth is inversely proportional to the closed-loop gain, sharply limiting bandwidth at high gain.

Figures 4a and 4b show appropriate feedback resistor values versus closed-loop gain for maximum bandwidth with minimal peaking. The dual vertical axes of these curves also show the resulting bandwidth. Note that the bandwidth remains nearly constant as gain is increased.

With control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to an application's requirements. Lower feedback resistance gives wider bandwidth, more frequency-response peaking and more pulse response overshoot. The higher open-loop gain resulting from lower feedback network resistors also yields lower distortion. Higher feedback network resistance gives an over-damped response with little or no peaking and overshoot. This may be beneficial when driving capacitive loads. Feedback network impedance can also be varied to optimize dynamic performance. To achieve wider bandwidth, use a feedback resistor value somewhat lower than indicated in Figure 4.

EXTENDING BANDWIDTH

For gains less than approximately 20, bandwidth can be extended by adding a capacitor, C_p , in parallel with a lower value for R_f . The optimum gain-setting resistor value in this case is far lower than those shown in Figure 1. For $\pm 15V$ operation, select R_f with the following equation:

$$R_F (\Omega) = 30 \cdot (30 - G) \text{ for } V_s = \pm 15V$$

For example, for a gain of 10, use $R_F = 600\Omega$. Optimum values differ slightly for $\pm 5V$ operation:

$$R_F (\Omega) = 30 \cdot (23 - G) \text{ for } V_s = \pm 5V$$

C_F will range from 1pF to 10pF depending on the selected gain, load, and circuit layout. Adjust C_F to optimize bandwidth and minimize peaking. Figure 5 shows bandwidth which can be achieved using this technique.

Typical values for this capacitor range from 1pF to 10pF depending on closed-loop gain and load characteristics. Too large a value of C_F can cause instability.

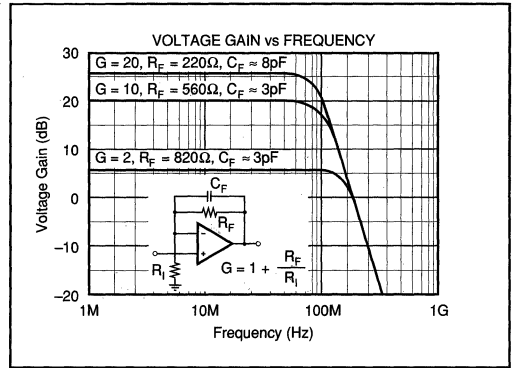


FIGURE 5. Bandwidth Results with Added Capacitor C_F .

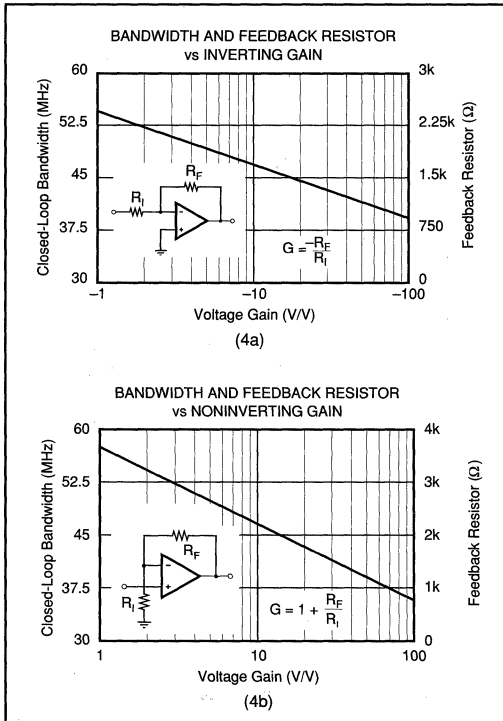


FIGURE 4. Feedback Resistor Selection Curves.

UNITY-GAIN OPERATION

As Figure 4b indicates, the OPA603 can be operated in unity gain. A feedback resistor (approximately $2.8k\Omega$) sets the appropriate open-loop characteristics and resistor R_I is omitted. Just as with gains greater than one, the value of the feedback resistor (and capacitor if used) can be optimized for the desired dynamic response and load characteristics.

Care should be exercised not to exceed the maximum differential input voltage rating of $\pm 6V$. Large input voltage steps which exceed the device's slew rate of $1000V/\mu s$ can apply excessive differential input voltage.

CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a $0.01\mu F$ ceramic capacitor in parallel with a $2.2\mu F$ solid tantalum capacitor at each power supply pin is adequate. The OPA603 can deliver high load current—up to 150mA peak. Applications with low impedance or capacitive loads demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as $10\mu F$ solid tantalum capacitors may improve performance in these applications.

POWER DISSIPATION

High output current causes increased internal power dissipation in the OPA603. Copper leadframe construction maximizes heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces. Solder the unused pins, (1, 5 and 8) to a top-side ground plane for improved power dissipation. Limit the load and signal conditions depending on maximum ambient temperature to assure operation within the power derating curve.

The OPA603 may be operated at reduced power supply voltage to minimize power dissipation. Detailed specifications are provided for both $\pm 15V$ and $\pm 5V$ operation.

APPLICATIONS CIRCUITS

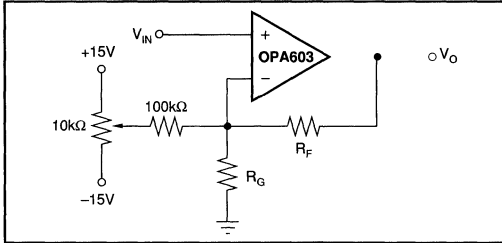


FIGURE 6. Offset Voltage Adjustment.

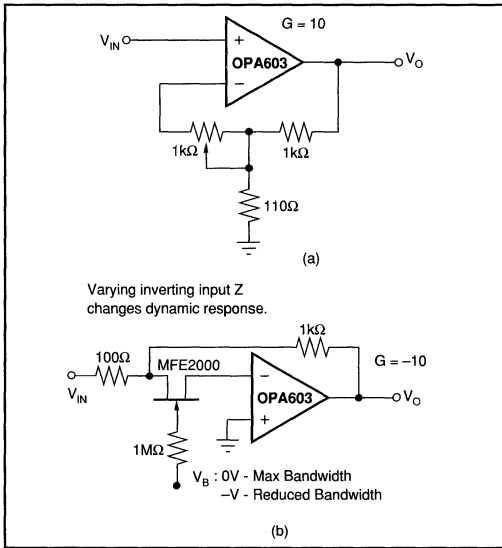


FIGURE 7. Controlling Dynamic Performance.

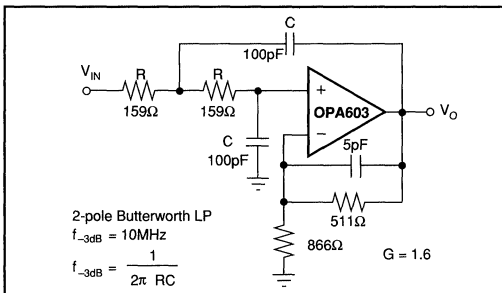


FIGURE 8. Low-Pass Filter — 10MHz.

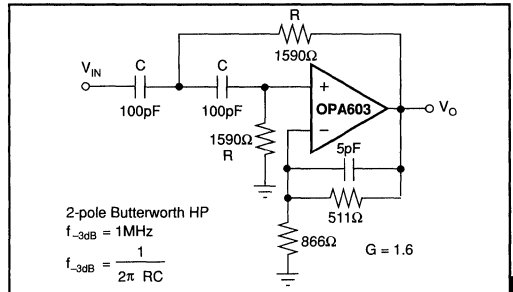


FIGURE 9. High-Pass Filter — 1MHz.

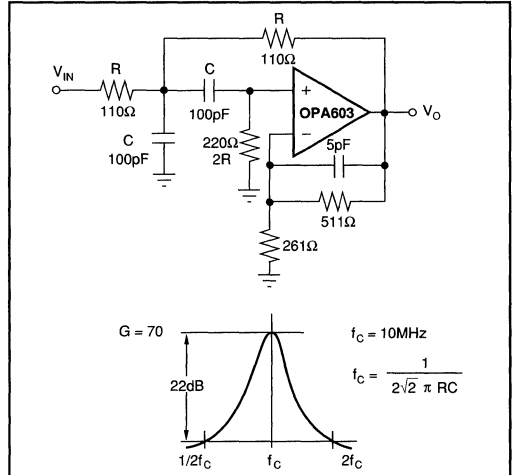
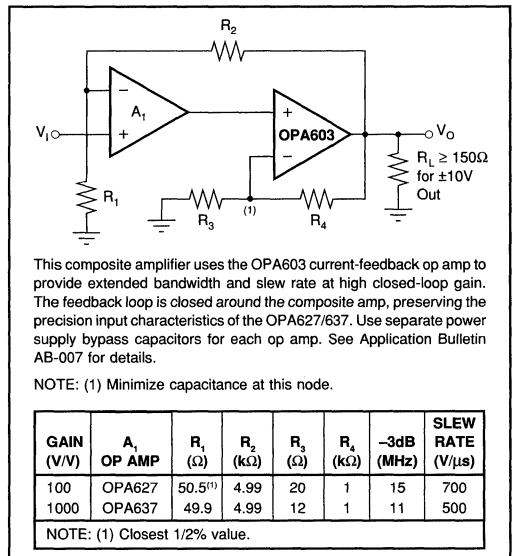


FIGURE 10. Bandpass Filter — 10MHz.



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp. See Application Bulletin AB-007 for details.

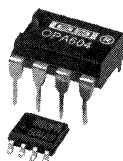
NOTE: (1) Minimize capacitance at this node.

GAIN (V/V)	A ₁ OP AMP	R ₁ (Ω)	R ₂ (kΩ)	R ₃ (Ω)	R ₄ (kΩ)	-3dB (MHz)	SLEW RATE (V/μs)
100	OPA627	50.5 ⁽¹⁾	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

FIGURE 11. Precision-Input Composite Amplifier.

For Immediate Assistance, Contact Your Local Salesperson



OPA604

FET-Input, Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: $10\text{nV}/\sqrt{\text{Hz}}$
- HIGH SLEW RATE: $25\text{V}/\mu\text{s}$
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_s = \pm 4.5$ to $\pm 24\text{V}$
- DRIVES 600Ω LOAD
- DUAL VERSION AVAILABLE (OPA2604)

APPLICATIONS

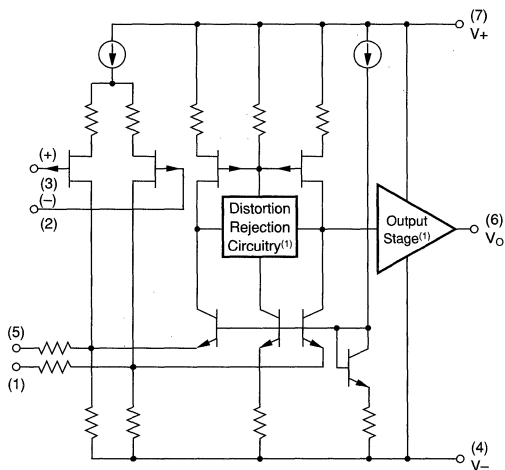
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA604 is a FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the -25°C to $+85^\circ\text{C}$ temperature range.



NOTE: (1) Patents Granted: #5053718, 5019789

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITION	OPA604AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection	$V_S = \pm 5$ to $\pm 24\text{V}$		± 1 ± 8 100	± 3	mV $\mu\text{V}/^\circ\text{C}$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		50 ± 3		pA pA
NOISE Input Voltage Noise Noise Density: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Voltage Noise, BW = 20Hz to 20kHz Input Bias Current Noise Current Noise Density, $f = 0.1\text{Hz}$ to 20kHz			25 15 11 10 1.5 4		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{CM} = \pm 12\text{V}$	± 12 80	± 13 100		V dB
INPUT IMPEDANCE Differential Common-Mode			$10^{12} \parallel 8$ $10^{12} \parallel 10$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-loop Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$	80	100		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.01% 0.1% Total Harmonic Distortion + Noise (THD + N)	$G = 100$ 20Vp-p , $R_L = 1\text{k}\Omega$ $G = -1$, 10V Step $G = 1$, $f = 1\text{kHz}$ $V_O = 3.5\text{Vrms}$, $R_L = 1\text{k}\Omega$	15	20 25 1.5 1 0.0003		MHz $\text{V}/\mu\text{s}$ μs μs %
OUTPUT Voltage Output Current Output Short Circuit Current Output Resistance, Open-Loop	$R_L = 600\Omega$ $V_O = \pm 12\text{V}$	± 11	± 12 ± 35 ± 40 25		V mA mA Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 5.3	± 24 ± 6	V V mA
TEMPERATURE RANGE Specification Storage Thermal Resistance ⁽²⁾ , θ_{JA}		-25 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

OPA604

2

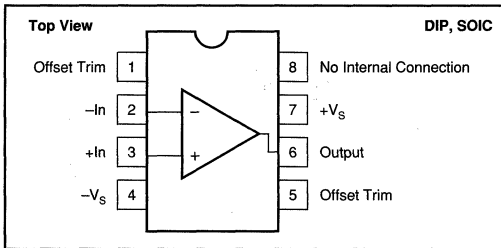
OPERATIONAL AMPLIFIERS

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±25V
Input Voltage	(V ₋)-1V to (V ₊)+1V
Output Short Circuit to Ground	Continuous
Operating Temperature	-40°C to +100°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA604AP	8-Pin Plastic DIP	-25°C to +85°C
OPA604AU	SO-8 Surface-Mount	-25°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA604AP	8-Pin Plastic DIP	006
OPA604AU	SO-8 Surface-Mount	182

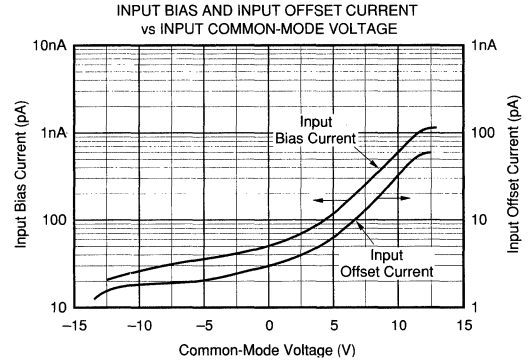
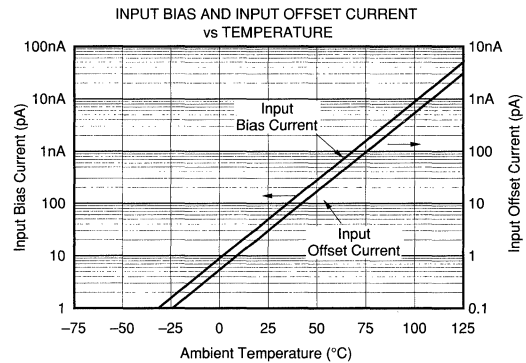
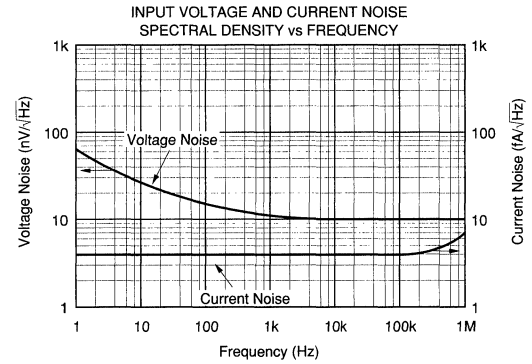
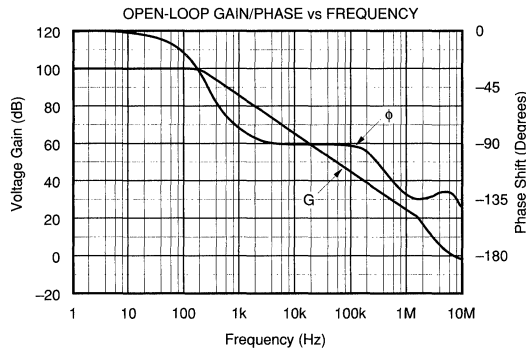
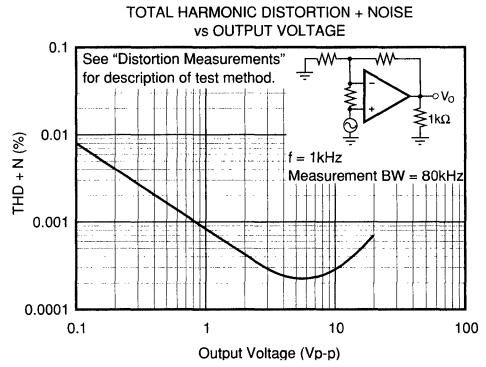
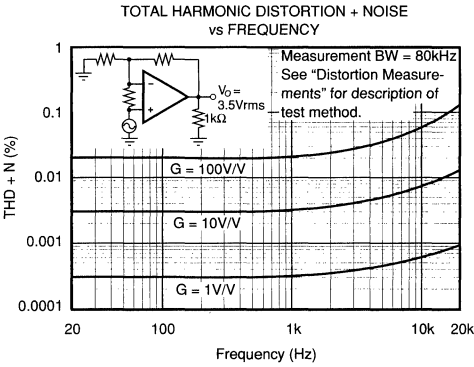
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

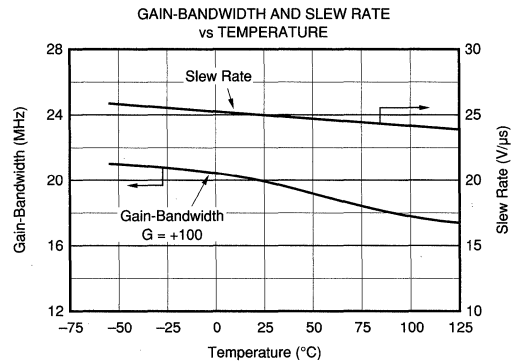
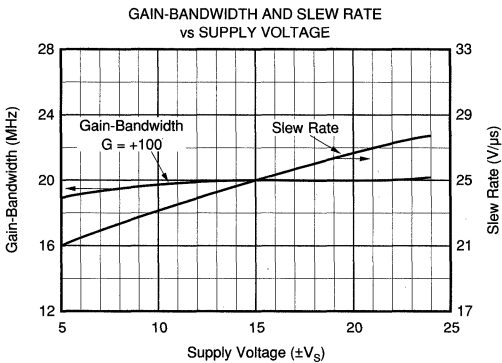
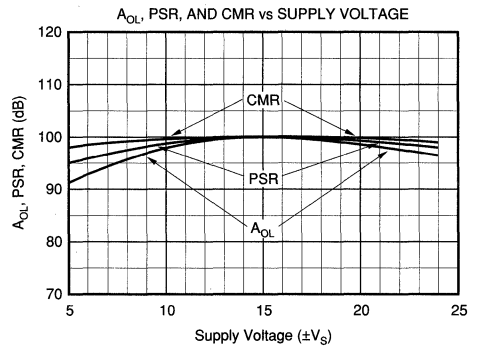
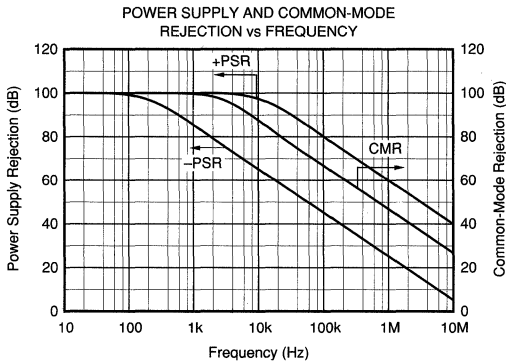
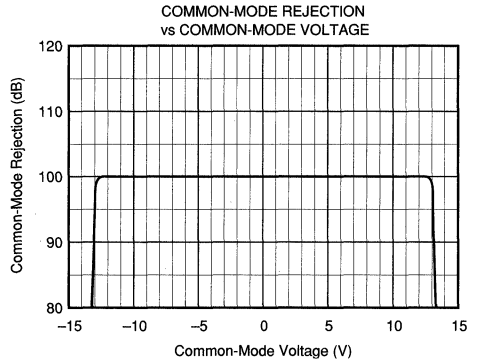
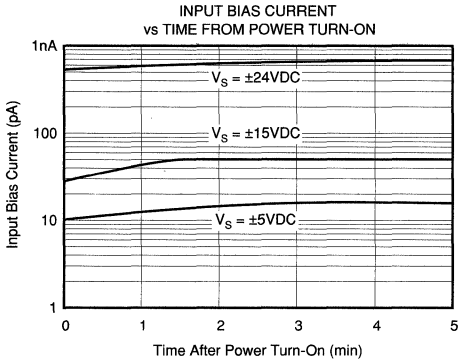


OPA604
2
OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

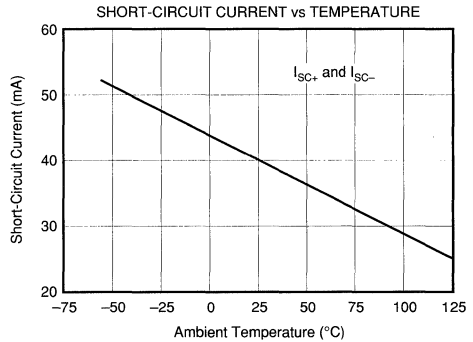
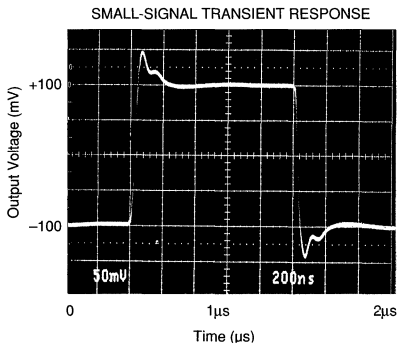
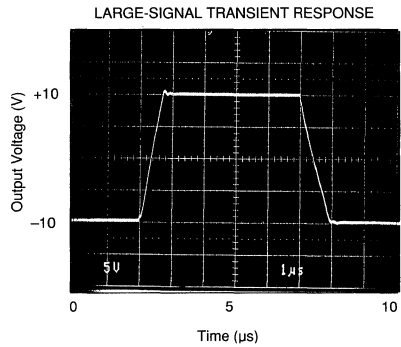
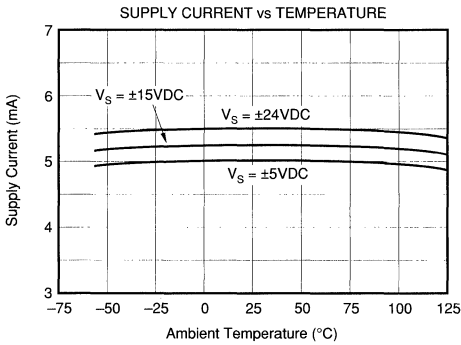
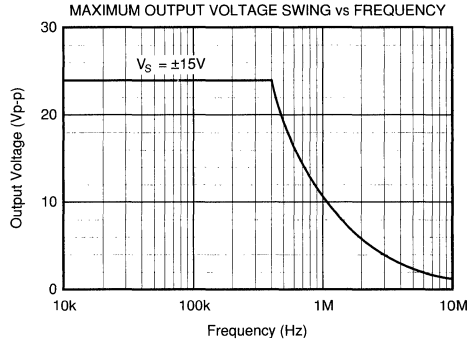
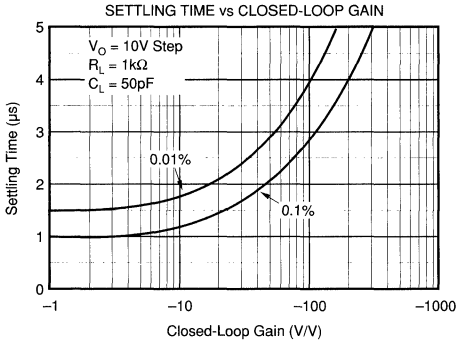
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



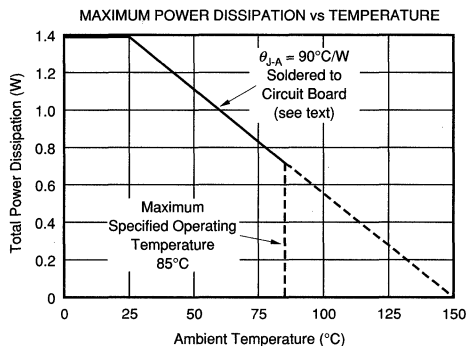
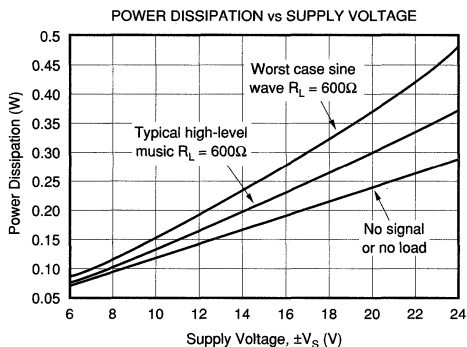
OPA604

2

OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA604 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. The OPA604 can replace many other amplifiers by leaving the external null circuit unconnected.

The OPA604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases, a $1\mu\text{F}$ tantalum capacitor at each power supply pin is adequate.

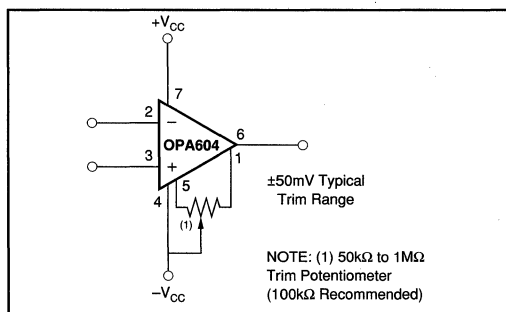


FIGURE 1. Offset Voltage Trim.

DISTORTION MEASUREMENTS

The distortion produced by the OPA604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 2 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3 .

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision, System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 3 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

For the unity-gain buffer, Figure 3a, stability is preserved by adding a phase-lead network, R_C and C_C . Voltage drop

across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 3b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 3c and 3d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 3d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 3e and 3f show input lead compensation networks for inverting and difference amplifier configurations.

NOISE PERFORMANCE

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and

will dominate. At a few thousand ohms source impedance and above, the OPA604 will generally provide lower noise.

POWER DISSIPATION

The OPA604 is capable of driving a 600 Ω load with power supply voltages up to $\pm 24V$. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately $\pm 40mA$ at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.

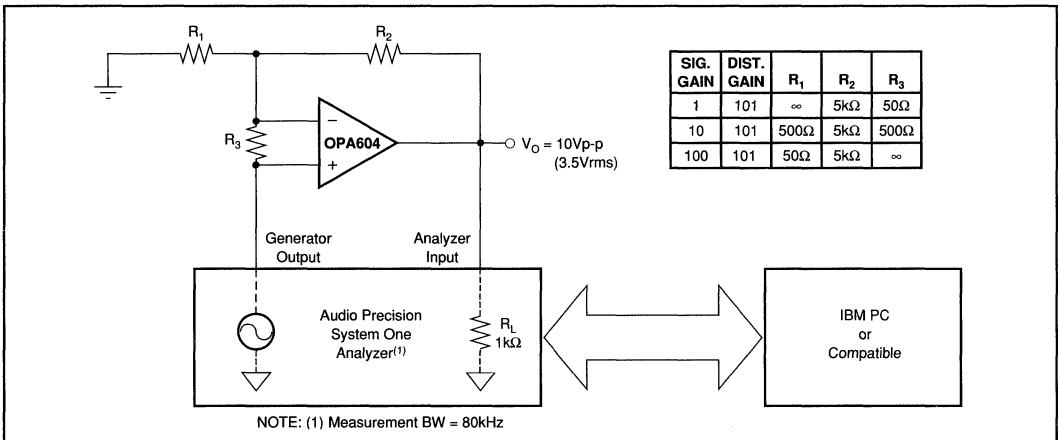
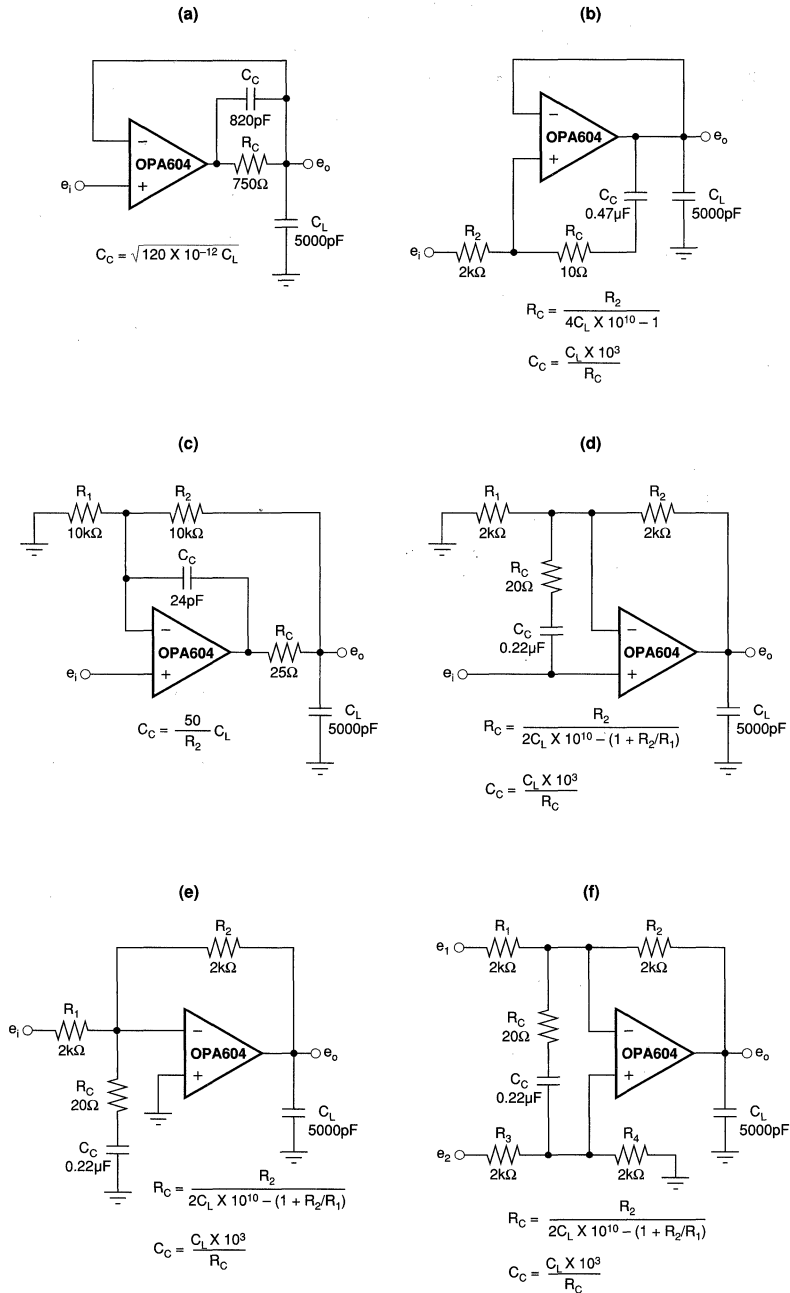


FIGURE 2. Distortion Test Circuit.

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NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 3. Driving Large Capacitive Loads.

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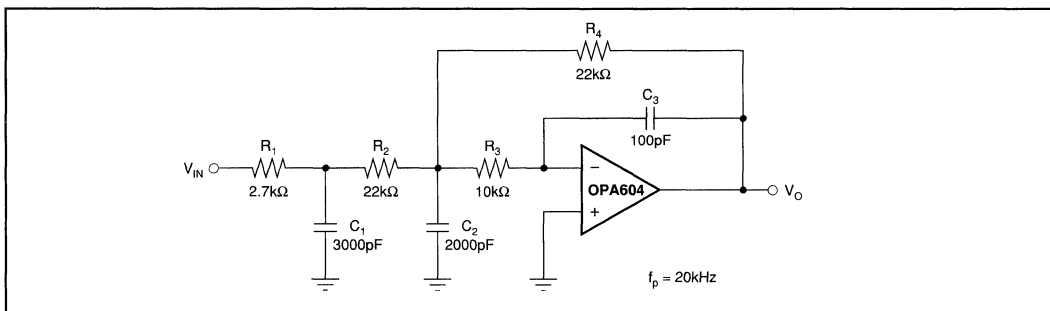


FIGURE 4. Three-Pole Low-Pass Filter.

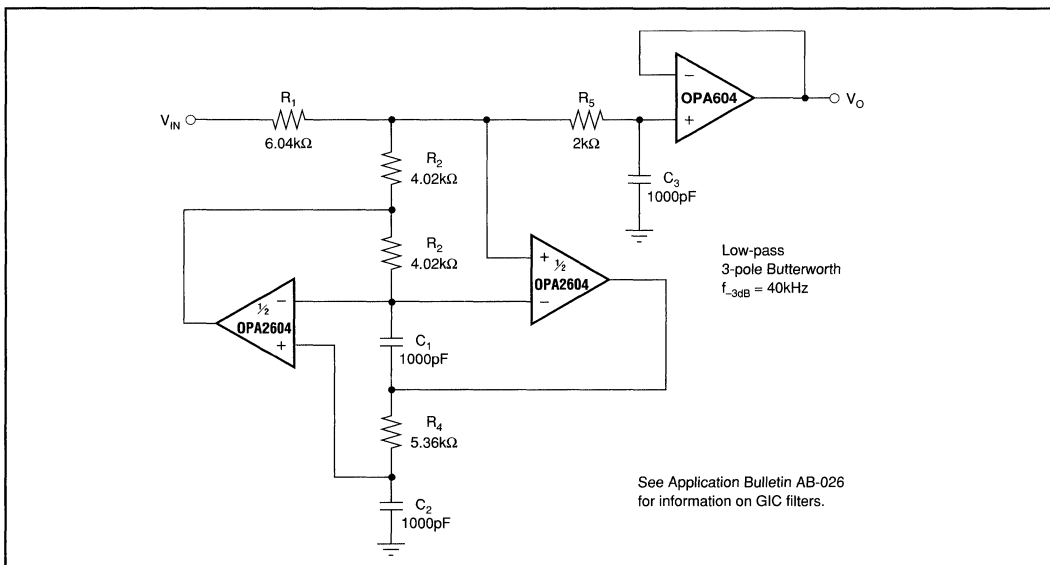


FIGURE 5. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

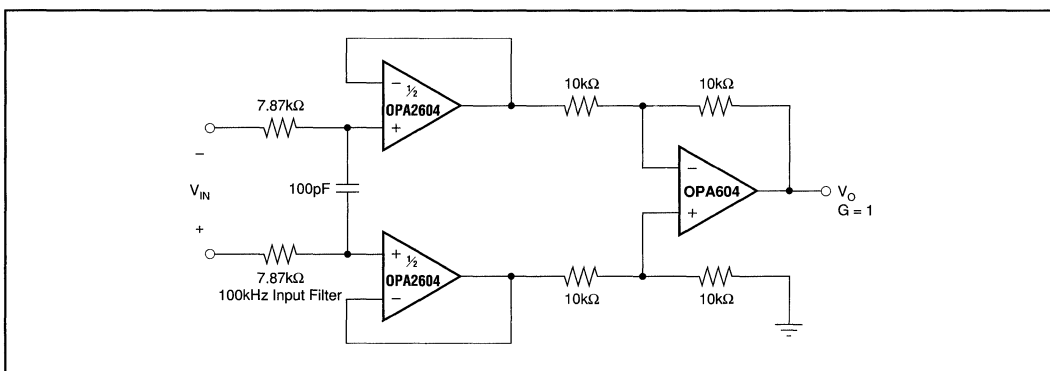


FIGURE 6. Differential Amplifier with Low-Pass Filter.

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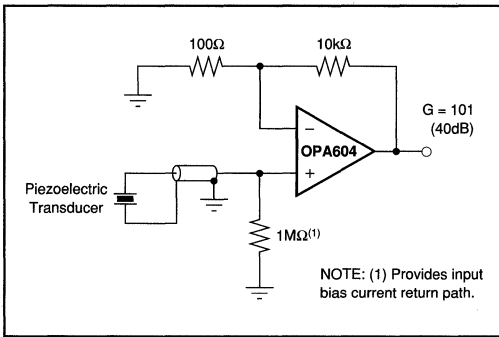


FIGURE 7. High Impedance Amplifier.

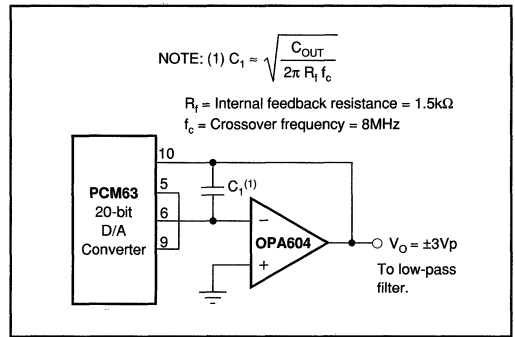


FIGURE 8. Digital Audio DAC I-V Amplifier.

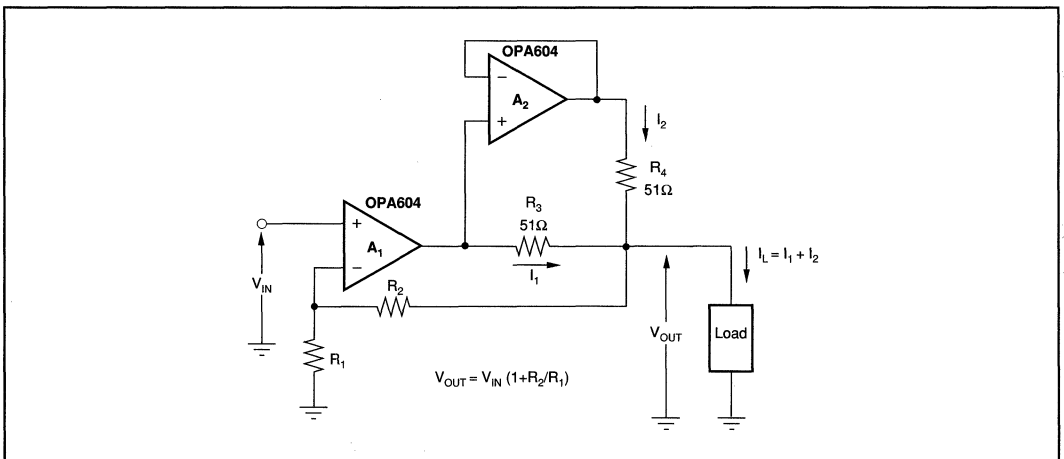


FIGURE 9. Using Two OPA604 Op Amps to Double the Output Current to a Load.

SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

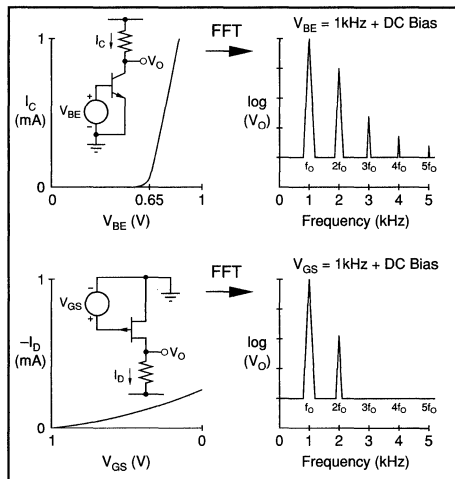
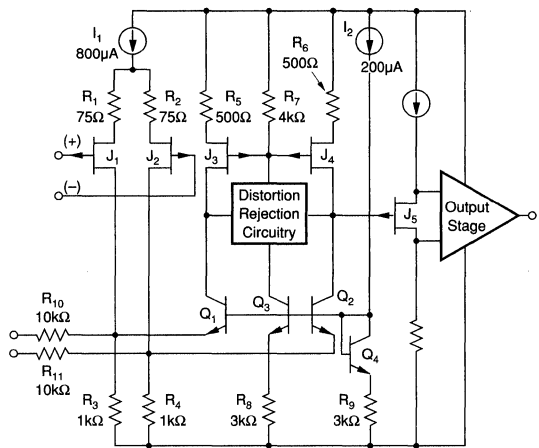


FIGURE 10. I-V and Spectral Response of NPN and JFET.



THE OPA604 DESIGN

The OPA604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important and where their transfer characteristics have minimal impact.

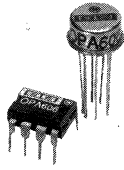
The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J_1 and J_2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high $800\mu\text{A}$, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of $\pm 25\text{V}/\mu\text{s}$.

The JFET input stage holds input bias current to approximately 50pA or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

The drains of J_1 and J_2 are cascoded by Q_1 and Q_2 , driving the input stage loads, FETs J_3 and J_4 . Distortion reduction circuitry (patented) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

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OPA606

Wide-Bandwidth *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 13MHz typ
- HIGH SLEW RATE: 35V/μs typ
- LOW BIAS CURRENT: 10pA max at
 $T_A = +25^\circ\text{C}$
- LOW OFFSET VOLTAGE: 500μV max
- LOW DISTORTION: 0.0035% typ at 10kHz

APPLICATIONS

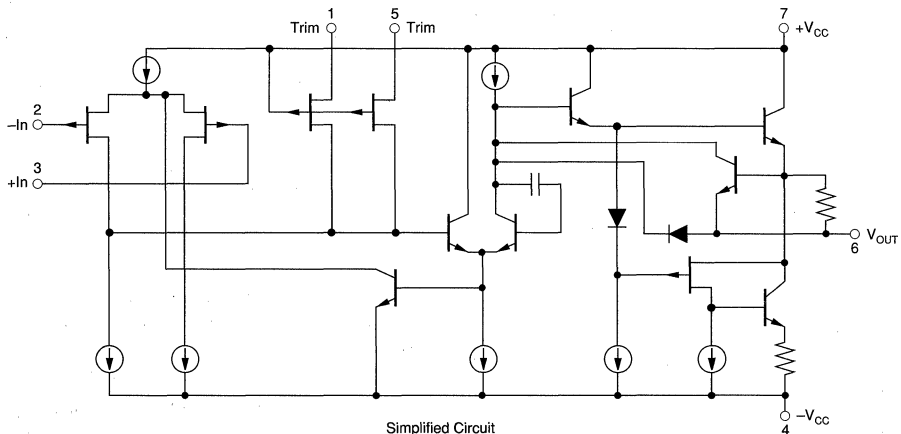
- OPTOELECTONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*[®]) operational amplifier featuring a wider bandwidth and lower bias current than BIFET[®] LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, as opposed to a junction temperature of +25°C.

Laser-trimmed thin-film resistors offer improved offset voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.



Difet[®]; Burr-Brown Corp.

BIFET[®]; National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE											
Gain Bandwidth	Small Signal	10	12.5		11	13		9	12		MHz
Full Power Response	20Vp-p, $R_L = 2\text{k}\Omega$		515			550			470		kHz
Slew Rate	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	22	33		25	35		20	30		V/ μs
Settling Time ⁽¹⁾ : 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		1.0			1.0			1.0		μs
0.01%	10V Step		2.1			2.1			2.1		μs
Total Harmonic Distortion	G = +1, 20Vp-p $R_L = 2\text{k}\Omega$ f = 10kHz		0.0035			0.0035			0.0035		%
INPUT OFFSET VOLTAGE⁽²⁾											
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		± 180	$\pm 1.5\text{mV}$		± 100	± 500		± 300	$\pm 3\text{mV}$	μV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 5			± 3	± 5		± 10		$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$	82	100		90	104		80	90		dB
			± 10	± 79		± 6	± 32		± 32	± 100	$\mu\text{V}/\text{V}$
BIAS CURRENT⁽²⁾											
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 7	± 15		± 5	± 10		± 8	± 25	pA
OFFSET CURRENT⁽²⁾											
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 0.6	± 10		± 0.4	± 5		± 1	± 15	pA
NOISE											
Voltage, $f_O = 10\text{Hz}$	100% tested (L)		37			30	40		37		nV/ $\sqrt{\text{Hz}}$
100Hz	100% tested (L)		21			20	28		21		nV/ $\sqrt{\text{Hz}}$
1kHz	100% tested (L)		14			13	16		14		nV/ $\sqrt{\text{Hz}}$
10kHz	⁽³⁾		12			11	13		12		nV/ $\sqrt{\text{Hz}}$
20kHz	⁽³⁾		11			10.5	13		11		nV/ $\sqrt{\text{Hz}}$
$f_B = 10\text{Hz}$ to 10kHz	⁽³⁾		1.3			1.2	1.5		1.3		μVrms
Current, $f_O = 0.1\text{Hz}$ thru 20kHz	⁽³⁾		1.5			1.3	2		1.7		fA/ $\sqrt{\text{Hz}}$
IMPEDANCE											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE											
Common-Mode Input Range		± 10.5	± 11.5		± 11	± 11.6		± 10.2	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	80	95		85	96		78	90		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	95	115		100	118		90	110		dB
RATED OUTPUT											
Voltage Output	$R_L = 2\text{k}\Omega$	± 11	± 12.2		± 12	± 12.6		± 11	± 12		V
Current Output	$V_O = \pm 10\text{VDC}$	± 5	± 10		± 5	± 10		± 5	± 10		mA
Output Resistance	DC, Open Loop		40			40			40		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
POWER SUPPLY											
Rated Voltage			± 15			± 15			± 15		VDC
Voltage Range, Derated Performance		± 5		± 18	± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_O = 0\text{mADC}$		6.5	9.5		6.2	9		6.5	10	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	0		+70	0		+70	0		+70	$^\circ\text{C}$
Operating	KM, KP, LM	-55		+125	-55		+125	-40		+85	$^\circ\text{C}$
θ_{JA}	Ambient Temperature		200			200			155		$^\circ\text{C}/\text{W}$

NOTES: (1) See settling time test circuit in Figure 2. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Sample tested—this parameter is guaranteed on L grade only.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	°C
INPUT OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $V_{CC} = \pm 10\text{V to } \pm 18\text{V}$		± 400 ± 5 98 ± 13	$\pm 2\text{mV}$ ± 100		± 335 ± 3 100 ± 10	± 750 ± 5 ± 56		± 750 ± 10 95 ± 18	$\pm 3.5\text{mV}$ ± 126	μV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V}/\text{V}$
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$		± 158	± 339		± 113	± 226		± 181	± 566	pA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		± 14	± 226		± 9	± 113		± 23	± 339	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10.4 78	± 11.4 92		± 10.9 82	± 11.5 95		± 10 75	± 10.9 88		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	90	106		95	112		88	104		dB
RATED OUTPUT Voltage Output Current Output	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$	± 10.5 ± 5	± 12 ± 10		± 11.5 ± 5	± 12.4 ± 10		± 10.4 ± 5	± 11.8 ± 10		V mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		6.6	10		6.4	9.5		6.6	10.5	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 180\text{VDC}$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage	$\pm 36\text{VDC}$
Input Voltage Range	$\pm 18\text{VDC}$
Storage Temperature Range	M = $-65^\circ\text{C to } +150^\circ\text{C}$ P = $-40^\circ\text{C to } +85^\circ\text{C}$
Operating Temperature Range	M = $-55^\circ\text{C to } +125^\circ\text{C}$ P = $-40^\circ\text{C to } +85^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short-Circuit Duration ⁽³⁾	Continuous
Junction Temperature	$+175^\circ\text{C}$

NOTES: (1) Packages must be derated based on $\theta_{JC} = 15^\circ\text{C}/\text{W}$ or θ_{JA} . (2) For supply voltages less than $\pm 18\text{VDC}$, the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to $+25^\circ\text{C}$ ambient. Observe dissipation limit and T_J .

PACKAGE INFORMATION⁽¹⁾

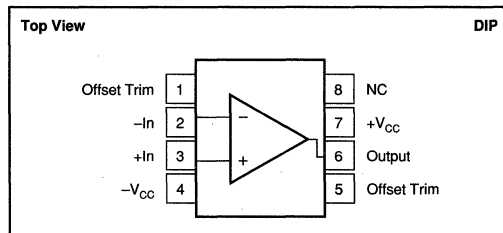
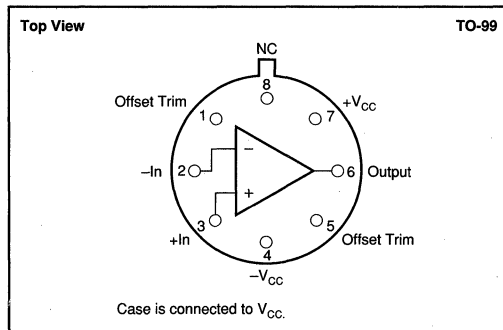
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA606KM	TO-99	001
OPA606LM	TO-99	001
OPA606KP	Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

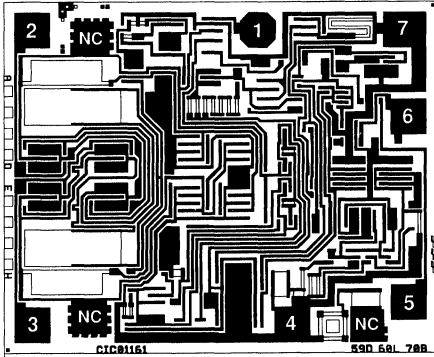
MODEL	PACKAGE	TEMPERATURE RANGE
OPA606KM	TO-99	$0^\circ\text{C to } 70^\circ\text{C}$
OPA606LM	TO-99	$0^\circ\text{C to } 70^\circ\text{C}$
OPA606KP	Plastic DIP	$0^\circ\text{C to } 70^\circ\text{C}$

CONNECTION DIAGRAMS



Or, Call Customer Service at 1-800-548-6132 (USA Only)

DICE INFORMATION



OPA606 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _S
5	Offset Trim
6	Output
7	+V _S
8	NC
NC	No Connection

Substrate Bias: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	65 x 54 ±5	1.65 x 1.37 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		43

OPA606

2

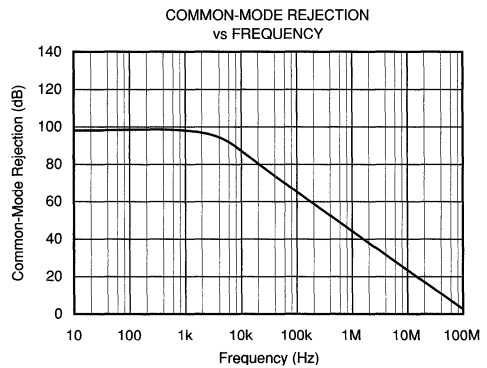
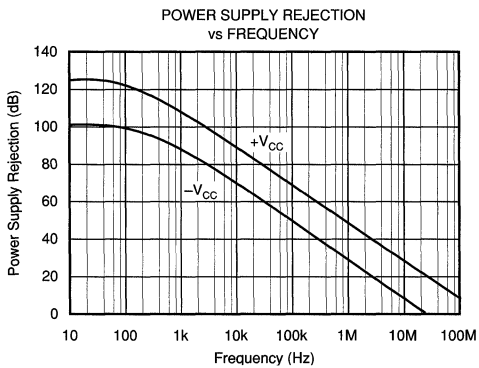
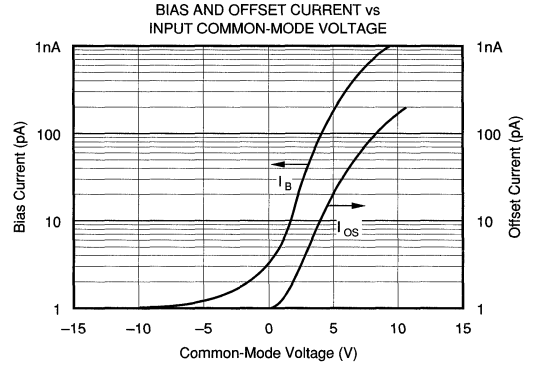
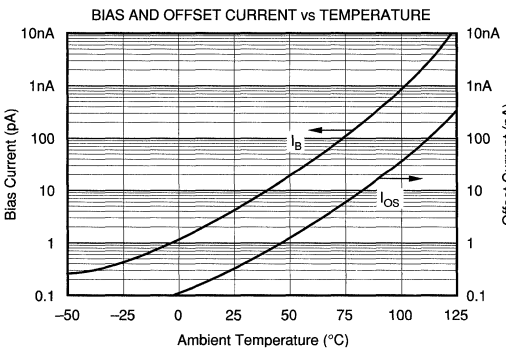
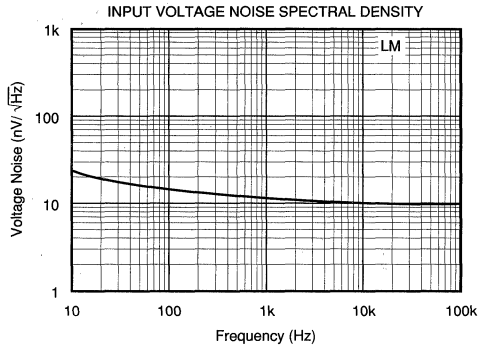
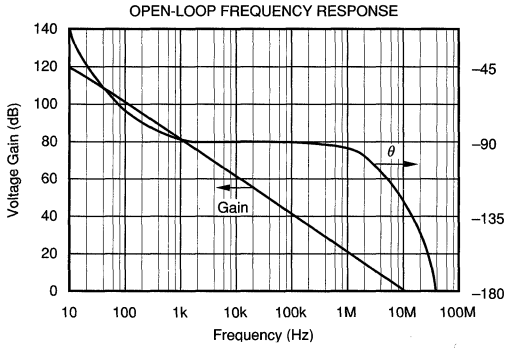
OPERATIONAL AMPLIFIERS

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.

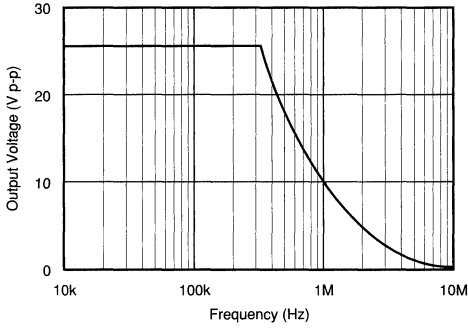


Or, Call Customer Service at 1-800-548-6132 (USA Only)

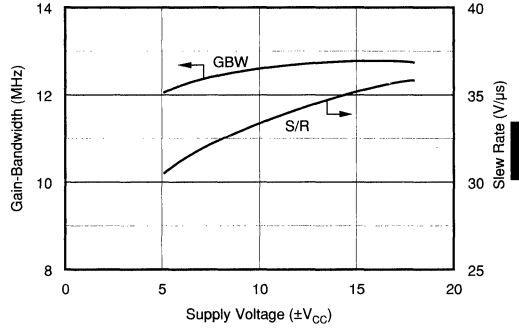
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise noted.

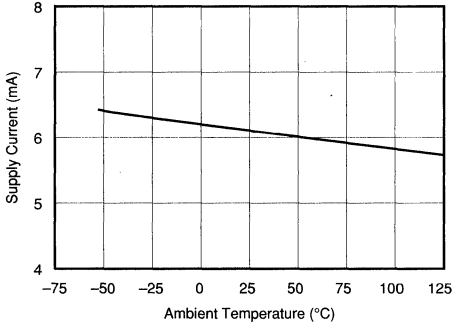
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



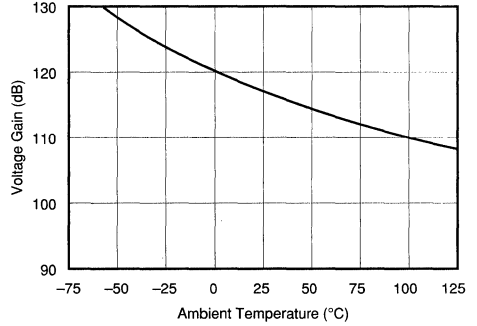
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



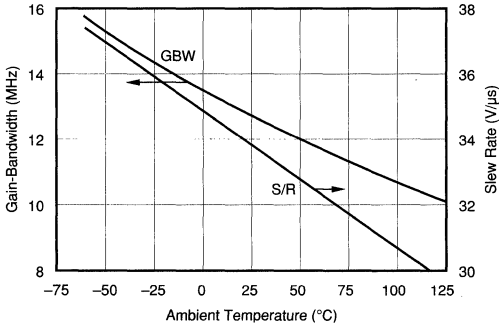
SUPPLY CURRENT vs TEMPERATURE



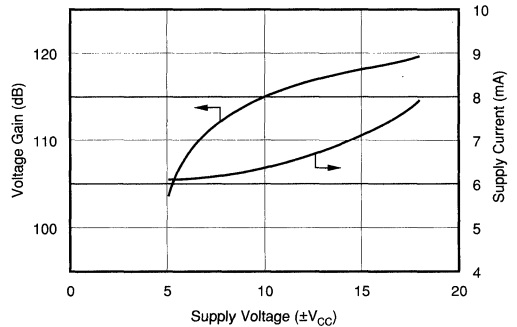
OPEN-LOOP GAIN vs TEMPERATURE



GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



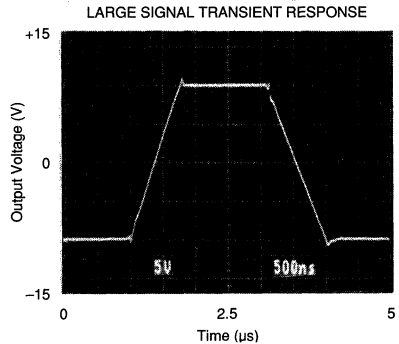
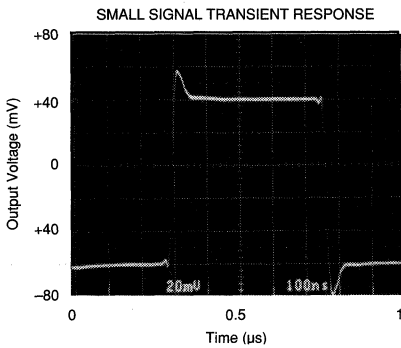
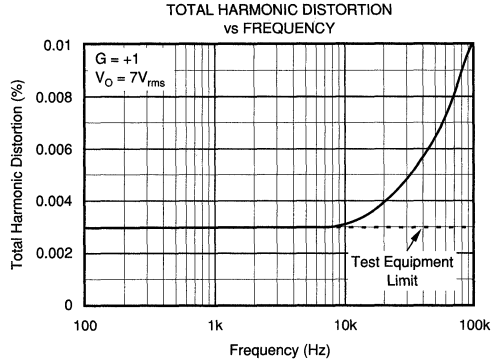
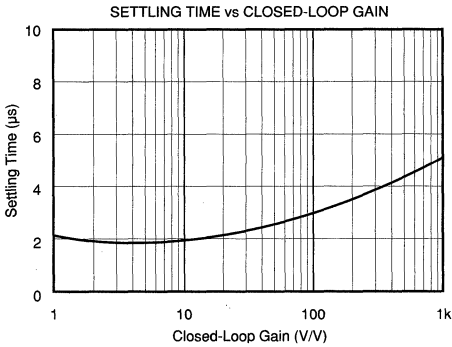
OPEN-LOOP GAIN AND SUPPLY CURRENT vs SUPPLY VOLTAGE



For Immediate Assistance, Contact Your Local Salesperson

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA606 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.5\mu\text{V}/^\circ\text{C}$ for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA606 can replace most other amplifiers by leaving the external null circuit unconnected.

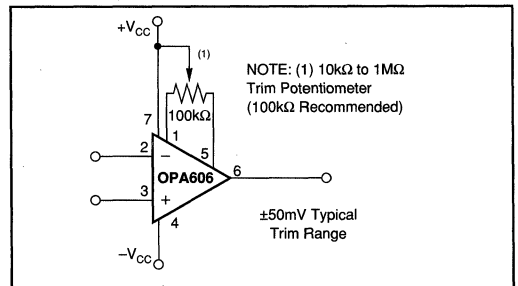


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA606. To avoid leakage problems, it is recommended that the signal input lead of the OPA606 be wired to a Teflon® standoff. If the OPA606 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 3).

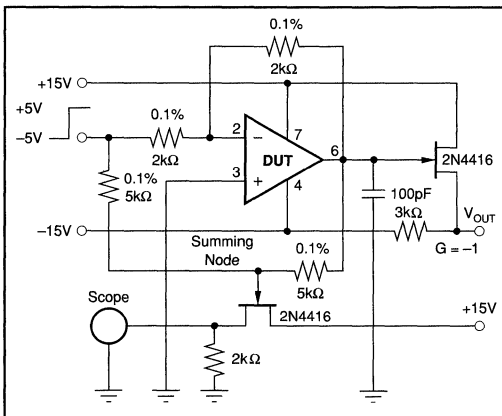


FIGURE 2. Settling Time Test Circuit.

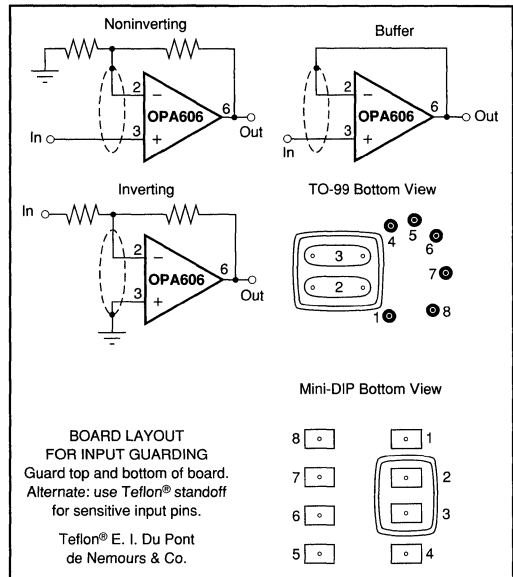


FIGURE 3. Connection of Input Guard.

APPLICATIONS CIRCUITS

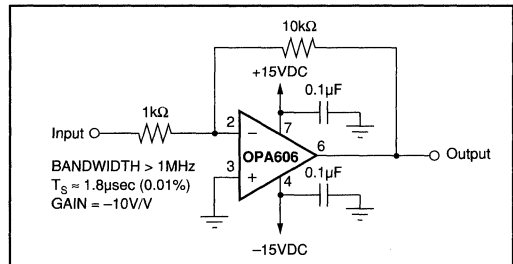


FIGURE 4. Inverting Amplifier.

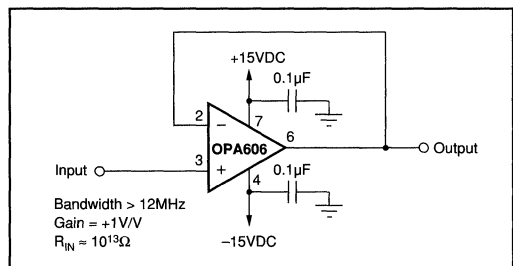


FIGURE 5. Noninverting Buffer.

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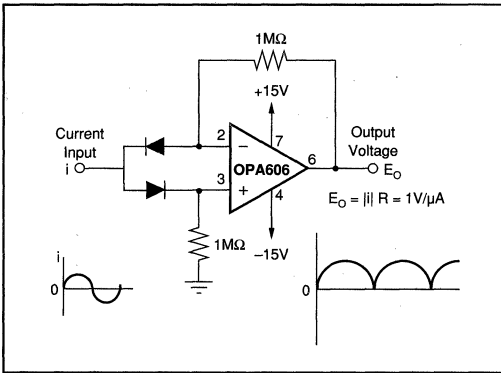


FIGURE 6. Absolute Value Current-to-Voltage Circuit.

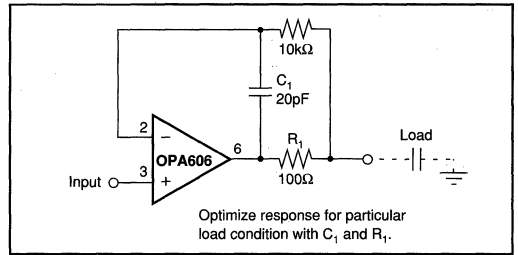


FIGURE 8. Isolating Load Capacitance from Buffer.

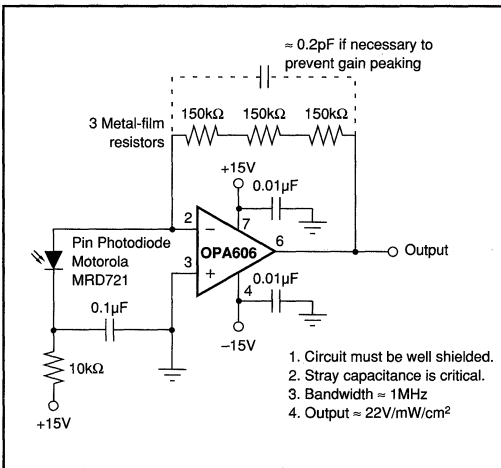


FIGURE 7. High-Speed Photodetector.

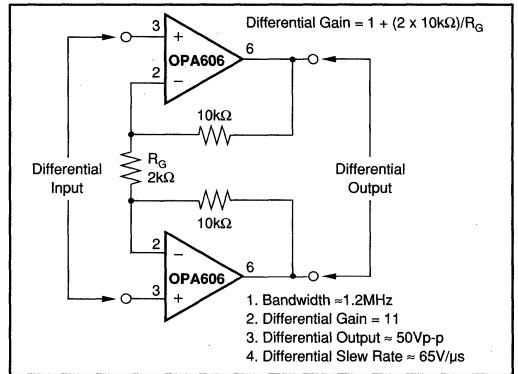


FIGURE 9. Differential Input/Differential Output Amplifier.

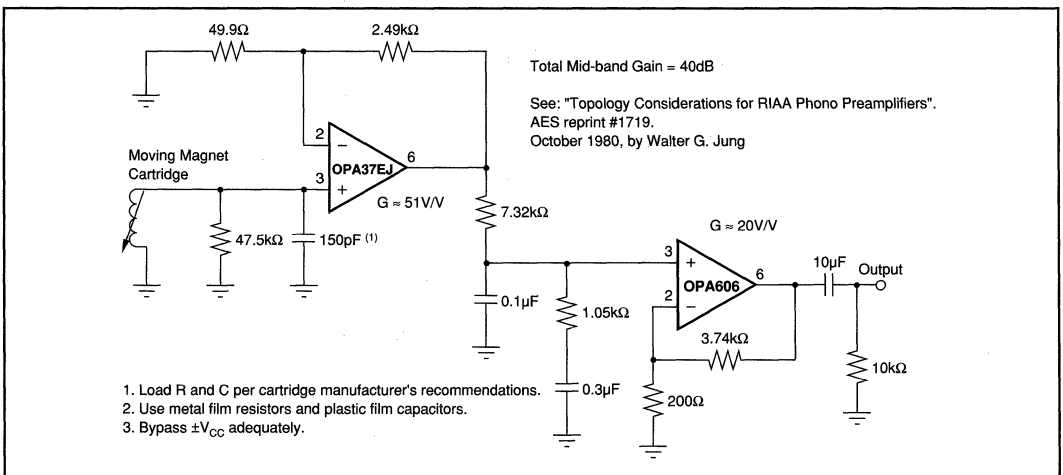
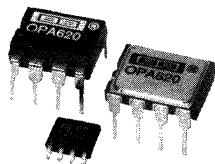


FIGURE 10. Low Noise/Low Distortion RIAA Preampfier.

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OPA620

OPA620

2

OPERATIONAL AMPLIFIERS

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: $2.3\text{nV}/\sqrt{\text{Hz}}$
- HIGH OUTPUT CURRENT: 100mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: $\pm 100\mu\text{V}$
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP, SOIC PACKAGES

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- LINE DRIVER
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

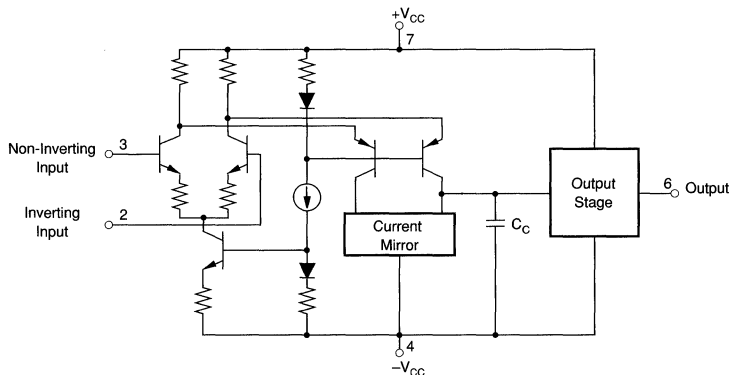
The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be

used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: -40°C to $+85^{\circ}\text{C}$ and -55°C to $+125^{\circ}\text{C}$.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP, KU, KG			OPA620, SG			OPA620LG			UNITS		
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
INPUT NOISE Voltage: $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$ $f_o = 100kHz$ $f_o = 1MHz$ to 100MHz $f_b = 100Hz$ to 10MHz Current: $f_o = 10kHz$ to 100MHz	$R_s = 0\Omega$		10			*			*		nV/\sqrt{Hz}		
			5.5			*			*		nV/\sqrt{Hz}		
			3.3			*			*		nV/\sqrt{Hz}		
			2.5			*			*		nV/\sqrt{Hz}		
			2.3			*			*		nV/\sqrt{Hz}		
			8.0			*			*		$\mu V, rms$		
			2.3			*			*		pA/\sqrt{Hz}		
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to T_{MAX} $\pm V_{CC} = 4.5V$ to $5.5V$		± 200	$\pm 1mV$		*	*		± 100	± 500	μV $\mu V/^\circ C$ dB		
			50	60	*	*		55	*				
BIAS CURRENT Input Bias Current	$V_{CM} = 0VDC$		15	30		*	*		*	25	μA		
OFFSET CURRENT Input Offset Current	$V_{CM} = 0VDC$		0.2	2		*	*		*	*	μA		
INPUT IMPEDANCE Differential Common-Mode	Open-Loop		15 1			*			*		k Ω pF M Ω pF		
			1 1			*			*				
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$, $V_O = 0VDC$		± 3.0	± 3.5		*	*		*	*	V dB		
			65	75		*	*		70	*			
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$		50	60		*	*		55	*	dB		
			48	58		*	*		53	*	dB		
FREQUENCY RESPONSE Closed-Loop Bandwidth (-3dB) Gain-Bandwidth Differential Gain Differential Phase Harmonic Distortion ⁽²⁾ Full Power Response ⁽²⁾ Slew Rate ⁽²⁾ Overshoot Settling Time: 0.1% 0.01% Phase Margin Rise Time	Gain = +1V/V Gain = +2V/V Gain = +5V/V Gain = +10V/V Gain = +10V/V 3.58MHz, G = +1V/V 3.58MHz, G = +1V/V G = +2V/V, f = 10MHz, $V_O = 2Vp-p$ Second Harmonic Third Harmonic $V_O = 5Vp-p$, Gain = +1V/V $V_O = 2Vp-p$, Gain = +1V/V 2V Step, Gain = -1V/V 2V Step, Gain = -1V/V 2V Step, Gain = -1V/V Gain = +1V/V Gain = +1V/V, 10% to 90% $V_O = 100mVp-p$; Small Signal $V_O = 6Vp-p$; Large Signal		300			*	*		*	*	MHz		
			100			*	*		*	*		MHz	
			40			*	*		*	*		MHz	
			20			*	*		*	*		MHz	
			200			*	*		*	*		MHz	
			0.05			*	*		*	*		%	
			0.05			*	*		*	*		Degrees	
				-61	-50		*	*		*	*		dBc ⁽³⁾
				-65	-55		*	*		*	*		dBc
			11	16		*	*		*	*		MHz	
			27	40		*	*		*	*		MHz	
			175	250		*	*		*	*		V/ μs	
				10		*	*		*	*		%	
				13		*	*		*	*		ns	
				25		*	*		*	*		ns	
		60		*	*		*	*		Degrees			
		2		*	*		*	*		ns			
		22		*	*		*	*		ns			
RATED OUTPUT Voltage Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 100\Omega$ $R_L = 50\Omega$ 1MHz, Gain = +1V/V Gain = +1V/V Continuous		± 3.0	± 3.5		*	*		*	*	V V Ω pF mA		
			± 2.5	± 3.0		*	*		*	*			
				0.015		*	*		*	*			
				20		*	*		*	*			
			± 150		*	*		*	*				
POWER SUPPLY Rated Voltage Derated Performance Current, Quiescent	$\pm V_{CC}$ $\pm V_{CC}$ $I_o = 0mADC$		4.0	5	6.0	*	*		*	*	VDC VDC mA		
				21	23		*	*		*	*		
TEMPERATURE RANGE Specification: KP, KU, KG, LG SG Operating: KG, LG, SG KP, KU θ_{JA} KG, LG, SG KP KU	Ambient Temperature	-40		+85	*		*	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C$		
						-55	-55	+125	+125	-55	+125		
	Ambient Temperature	-40		+85								$^\circ C/W$ $^\circ C/W$ $^\circ C/W$	
							125			125			
				90	100								

* Same specifications as for KP/KU.

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SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA620KP, KU, KG			OPA620SG			OPA620LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification: KP, KU, KG, LG SG	Ambient Temperature	-40		+85	*		*	*		*	°C °C
OFFSET VOLTAGE⁽¹⁾ Average Drift Supply Rejection	Full Temp. 0°C to +70°C, $\pm V_{CC} = 4.5V$ to $5.5V$ Full Temp., $\pm V_{CC} = 4.5$ to $5.5V$	45 40	± 8 60 55		*	*	*	50 45	*	*	$\mu V/^\circ C$ dB dB
BIAS CURRENT Input Bias Current	Full Temp., $V_{CM} = 0VDC$		15 40		*	*	*	*	35		μA
OFFSET CURRENT Input Offset Current	Full Temp., $V_{CM} = 0VDC$		0.2 5		*	*	*	*	*		μA
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$, $V_O = 0VDC$	± 2.5 60	± 3.0 75		*	*	*	65	*		V dB
OPEN LOOP GAIN, DC Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$	46 44	60 58		*	*	*	52 50	*		dB dB
RATED OUTPUT Voltage Output	0°C to +70°C, $R_L = 100\Omega$ -40°C to +85°C, $R_L = 100\Omega$ 0°C to +70°C, $R_L = 50\Omega$ -40°C to +85°C, $R_L = 50\Omega$	± 3.0 ± 2.75 ± 2.5 ± 2.25	± 3.5 ± 3.25 ± 3.0 ± 2.7		*	*	*	*	*		V V V V
POWER SUPPLY Current, Quiescent	$I_O = 0mADC$		21 25		*	*	*	*	*		mA

* Same specifications as for KP/KU.

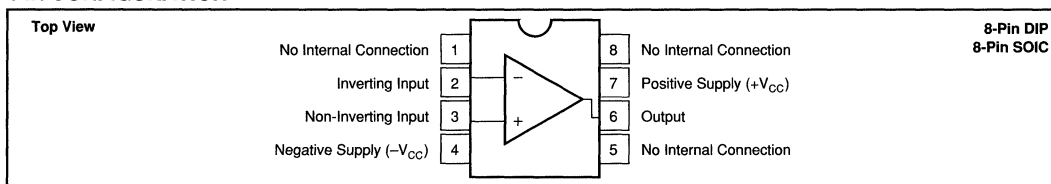
NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

OPA620

2

OPERATIONAL AMPLIFIERS

PIN CONFIGURATION



ORDERING INFORMATION

Basic Model Number	OPA620	()	()	(Q)
Performance Grade Code				
K, L = -40°C to +85°C				
S = -55°C to +125°C				
Package Code				
G = 8-pin Ceramic DIP				
P = 8-pin Plastic DIP				
U = 8-pin Plastic SOIC				
Reliability Screening				
Q = Q-Screened				

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 7VDC$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: KG, LG, SG	-65°C to +150°C
KP, KU	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground Junction Temperature (T_J)
	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA620KP	8-Pin Plastic DIP	006
OPA620KU	8-pin Plastic SOIC	182
OPA620KG	8-pin Ceramic DIP	157
OPA620LG	8-Pin Ceramic DIP	157
OPA620SG	8-Pin Ceramic DIP	157

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



DICE INFORMATION

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	-V _{CC}
2	-Input	8	NC
3	+Input	9	V _{OUT}
4	NC	10	+V _{CC}
5	NC	11	NC
6	NC	12	NC
		13	NC

Substrate Bias: Negative Supply -V_{CC}.

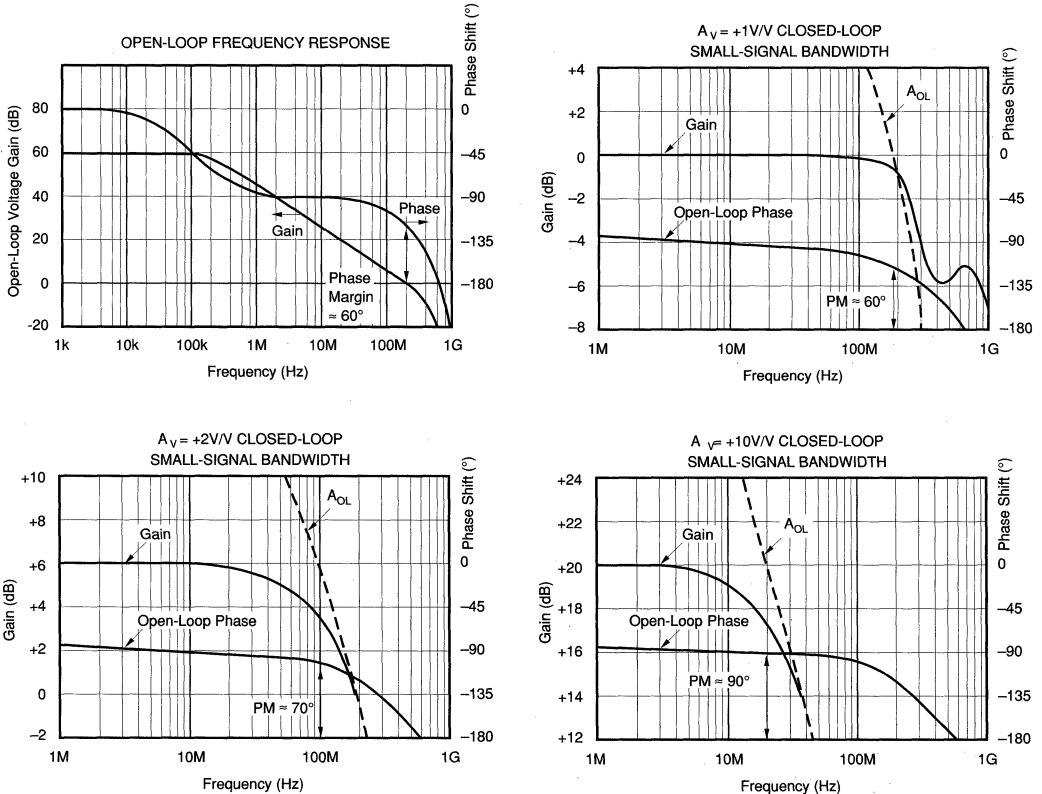
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.22 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold
Metalization		Gold

OPA620 DIE TOPOGRAPHY

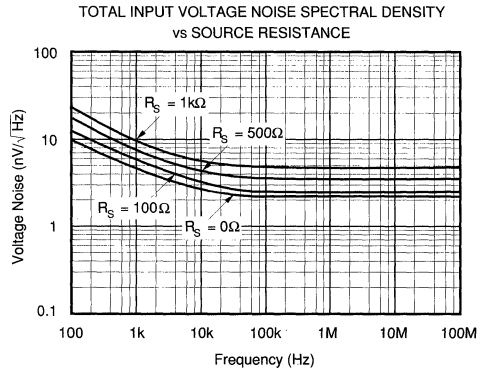
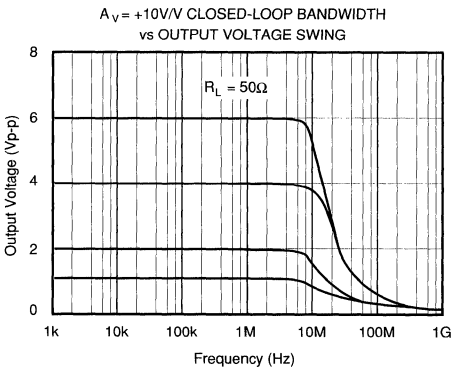
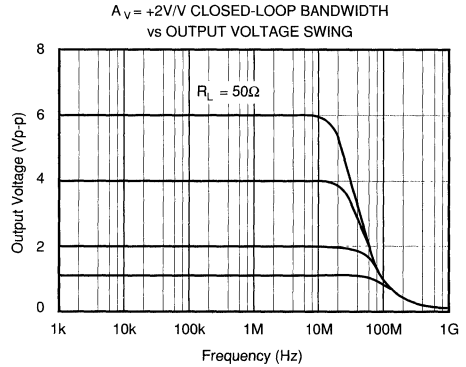
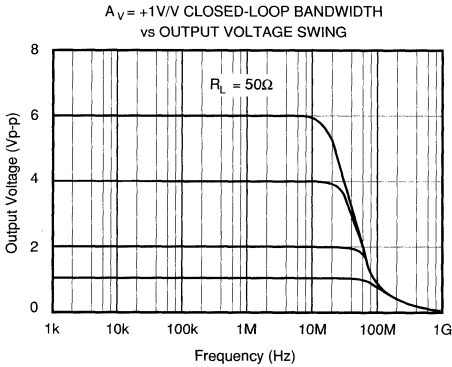
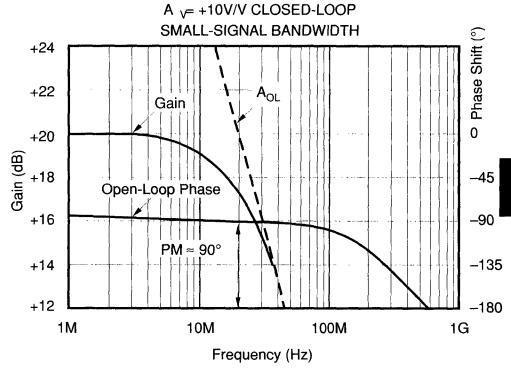
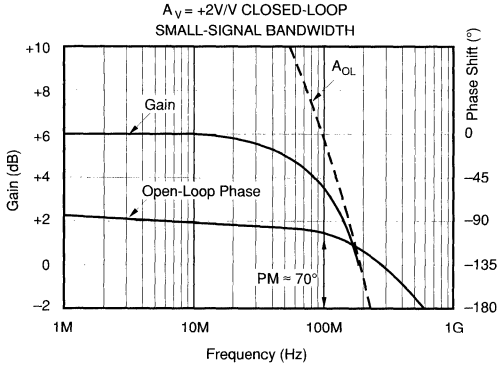
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω, and T_A = +25°C unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

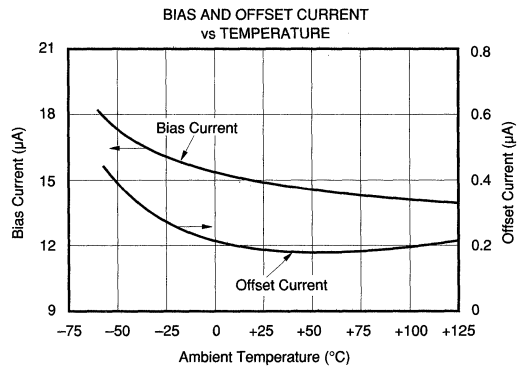
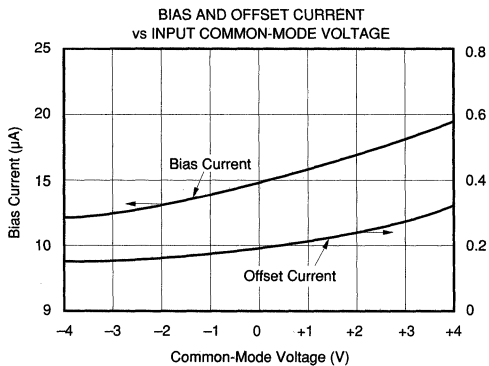
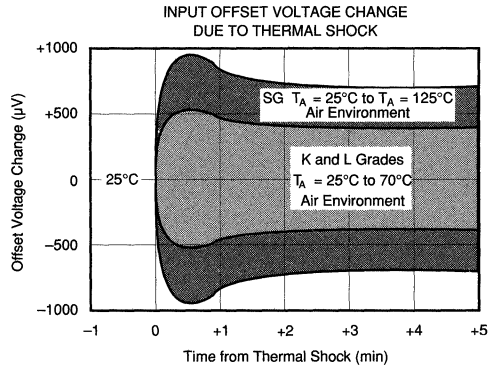
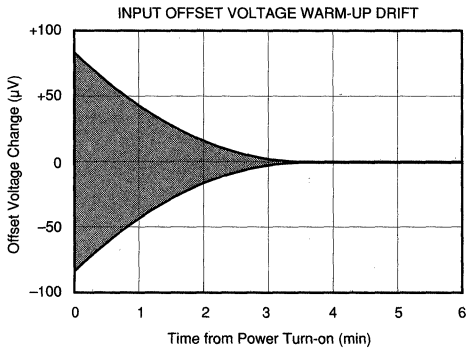
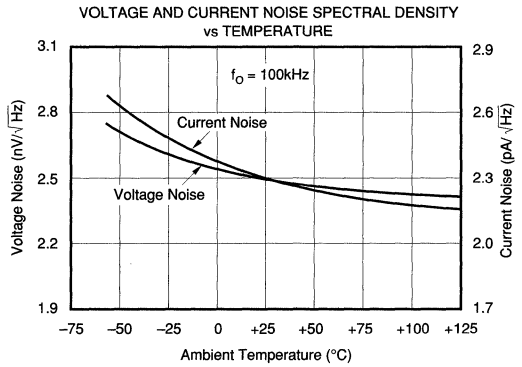
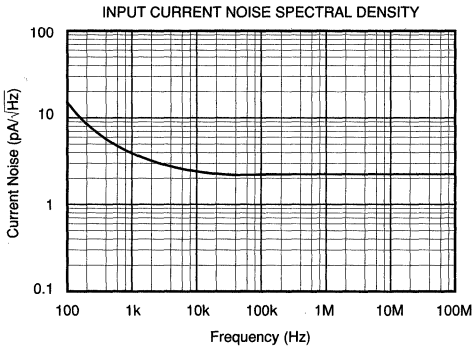
At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

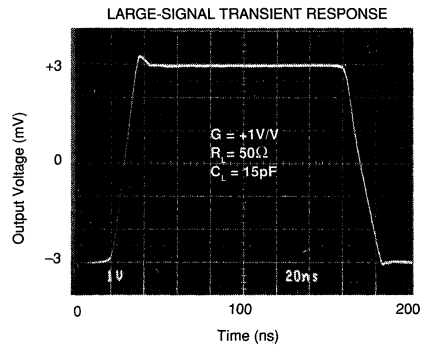
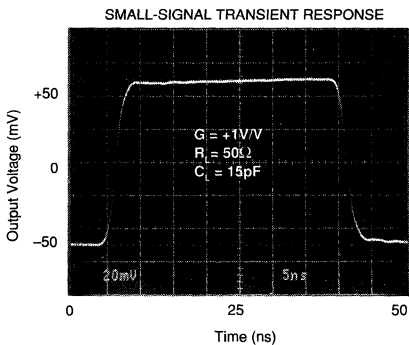
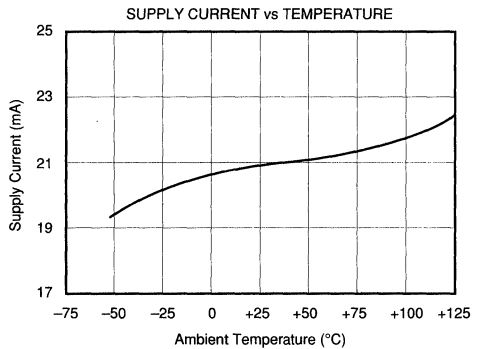
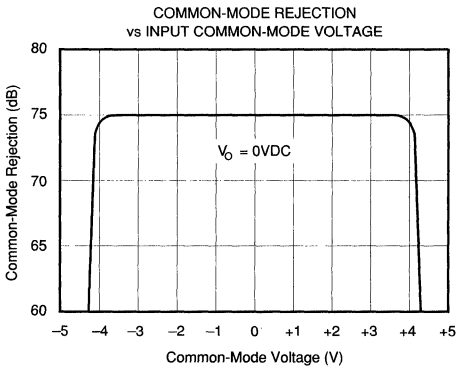
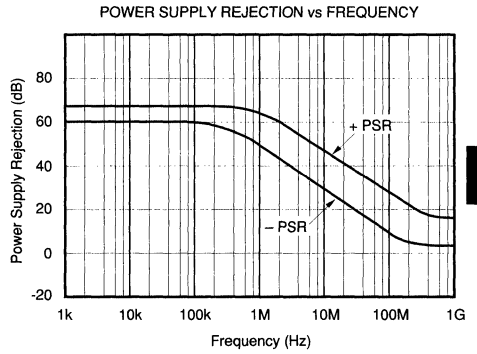
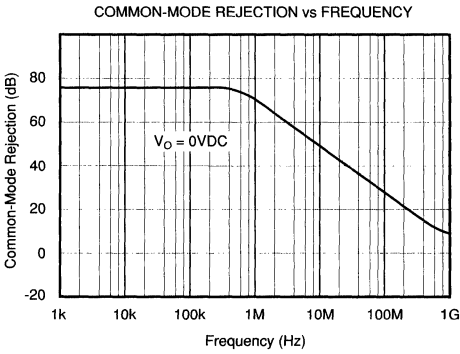
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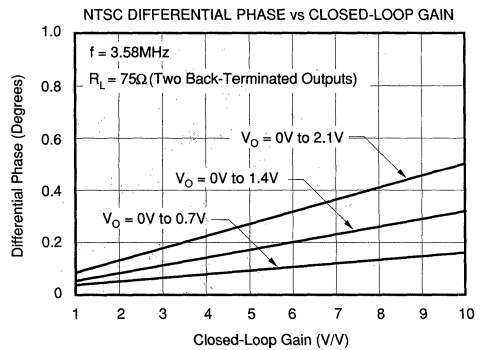
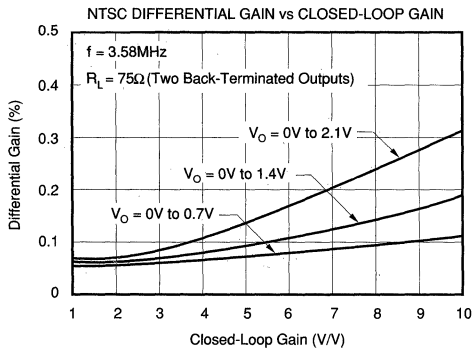
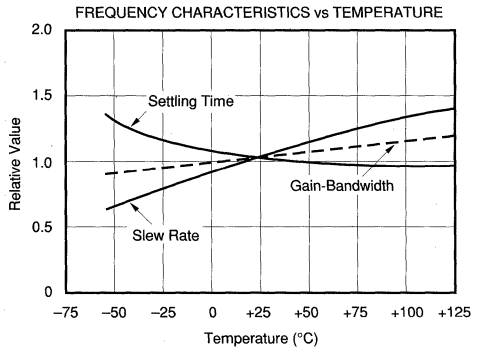
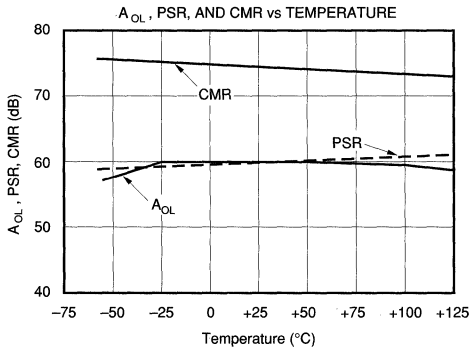
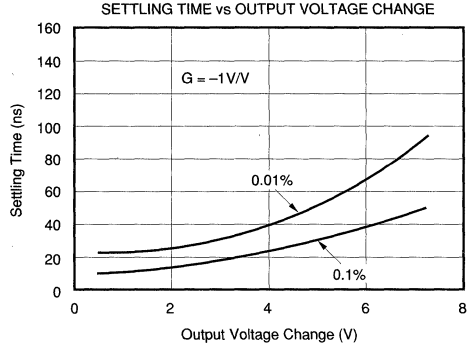
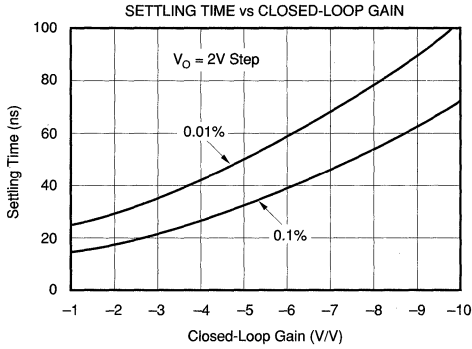
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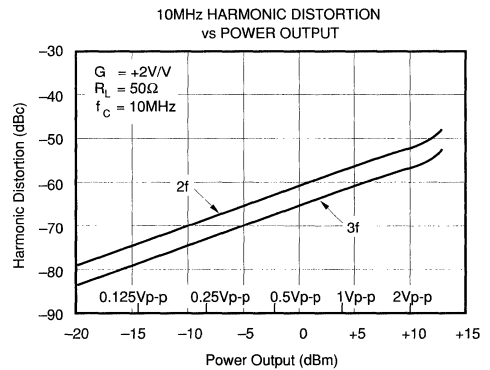
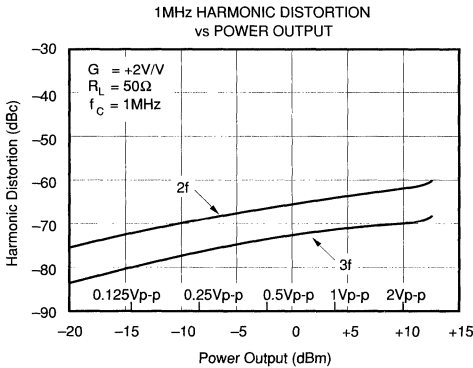
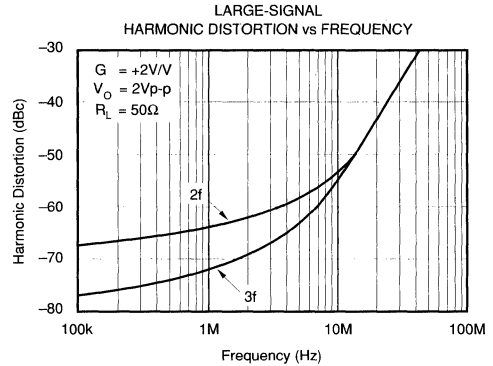
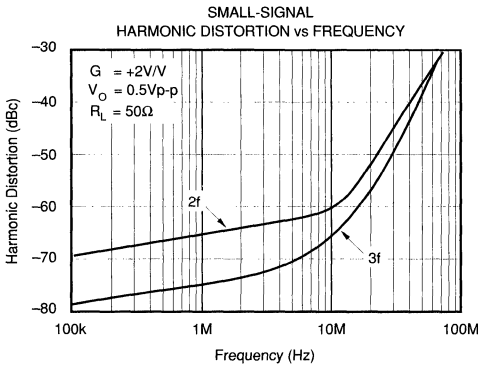
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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA620 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA620's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit

settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA620's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA620. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 200MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100 μV .

WIRING PRECAUTIONS

Maximizing the OPA620's capability requires some wiring precautions and high-frequency layout techniques. Oscilla-

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tion, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA620, as it is with all high-frequency circuits. Oscillations at frequencies of 200MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1 μ F to 10 μ F) with very short leads are recommended. Although not required, a parallel 0.01 μ F ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 3) Whenever possible, solder the OPA620 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® stand-

Teflon® E. I. Du Pont de Nemours & Co.

offs located close to the amplifier's pins can be used to mount feedback components.

- 4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits.
- 5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA620KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.
- 6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.
- 7) Don't forget that these amplifiers use ± 5 V supplies. Although they will operate perfectly well with +5V and -5.2V, use of ± 15 V supplies will destroy the part.
- 8) Standard commercial test equipment has not been designed to test devices in the OPA620's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
- 9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- 10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA620's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2 μ A.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA620 incorporates on-chip ESD protection diodes as shown in Figure 2.

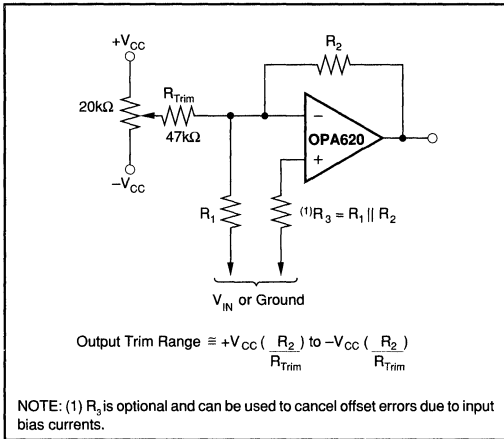


FIGURE 1. Offset Voltage Trim.

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA620 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

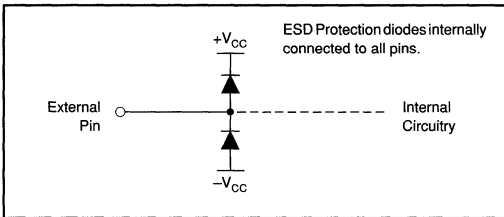


FIGURE 2. Internal ESD Protection.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA620.

OUTPUT DRIVE CAPABILITY

The OPA620's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The

device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA620 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA620 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

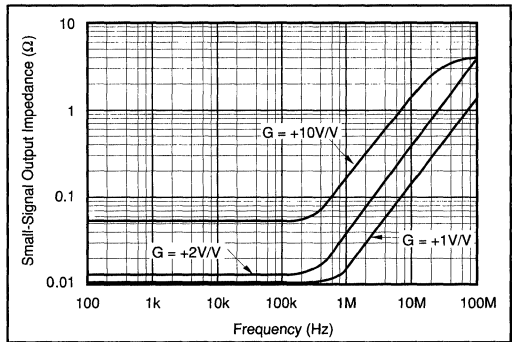


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA620 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

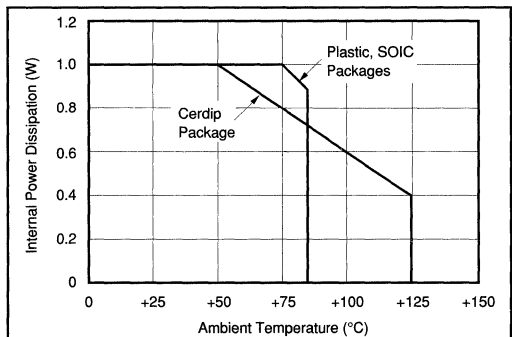


FIGURE 4. Maximum Power Dissipation.

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The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 230mW + 750mW \approx 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA} , of each package. The variation of short-circuit current with temperature is shown in Figure 5.

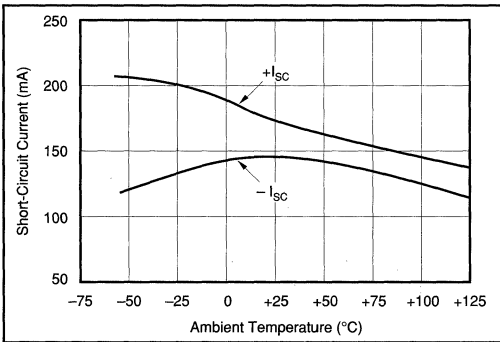


FIGURE 5. Short-Circuit Current vs Temperature.

CAPACITIVE LOADS

The OPA620's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

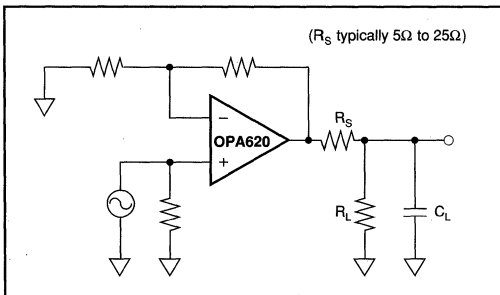


FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA620 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of -1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA620 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu V$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 25ns to 0.01% for a 2V step, making the OPA620 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

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In practice, settling time measurements on the OPA620 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA620. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA620's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA620's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA620 to operate in a gain of +2V/V and drive 2V_{p-p} into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +40dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_o)$$

where OPI³P = third-order output intercept, dBm

P_o = output level/tone, dBm/tone

Third IMD = third-order intermodulation ratio below each output tone, dB

For this case OPI³P = 40dBm, P_o = 10dBm, and the third-order IMD = 2(40 - 10) = 60dB below either 10dBm tone. The OPA620's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

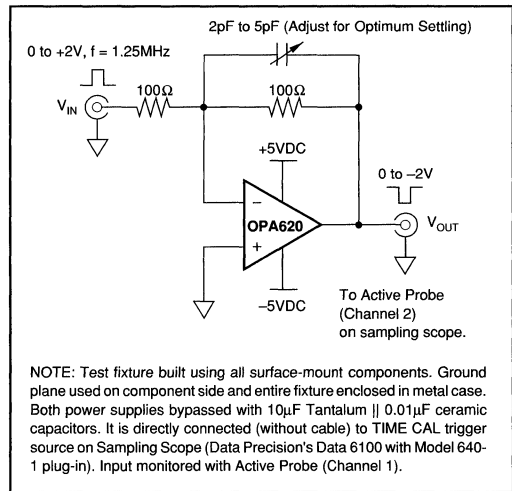


FIGURE 7. Settling Time Test Circuit.

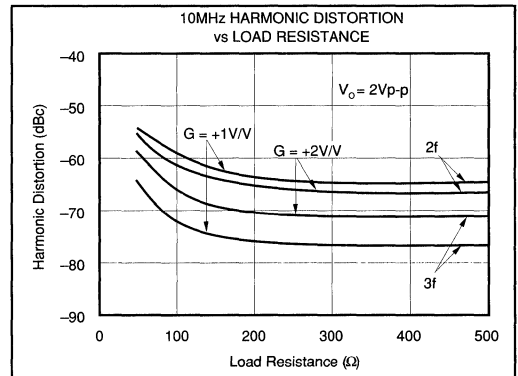


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

NOISE FIGURE

The OPA620's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA620's Noise Figure vs Source Resistance is shown in Figure 10.

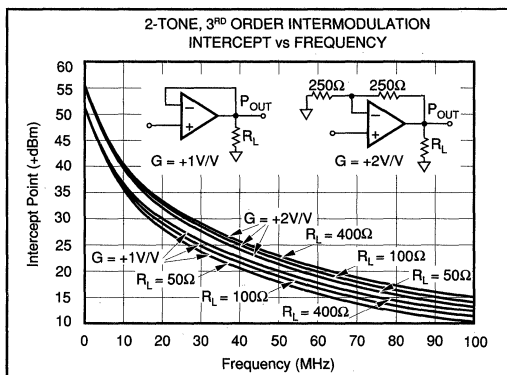


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA620. Request Burr-Brown Application Note AN-167.

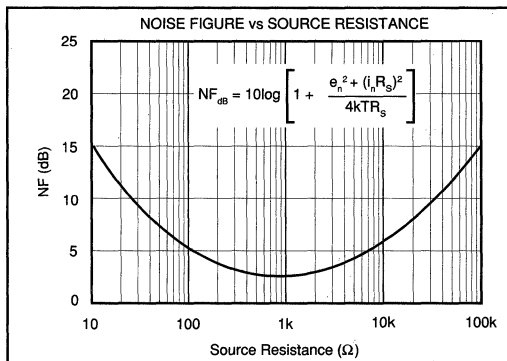


FIGURE 10. Noise Figure vs Source Resistance.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA620. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = -55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 atm cc/s Gross: Perfluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on SG package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

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APPLICATIONS

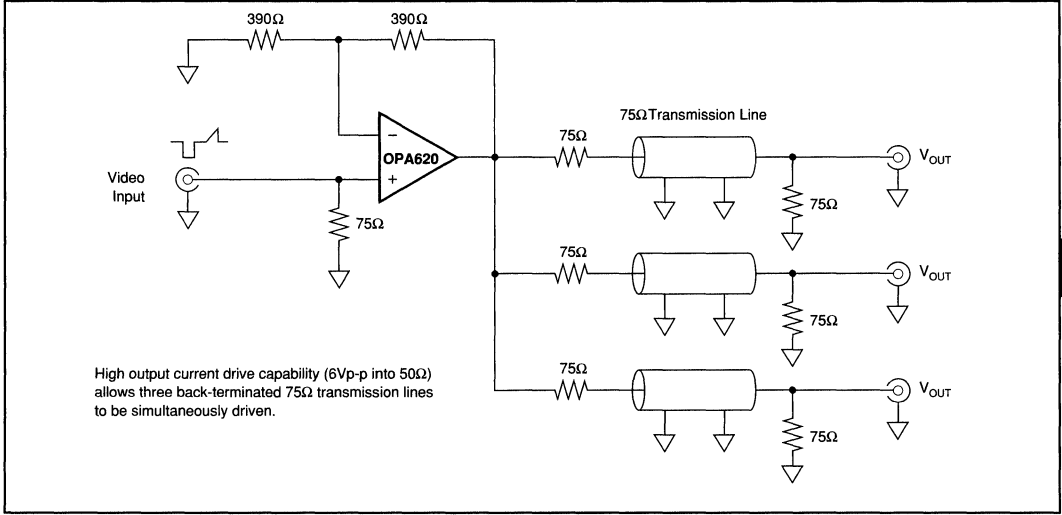


FIGURE 11. Video Distribution Amplifier.

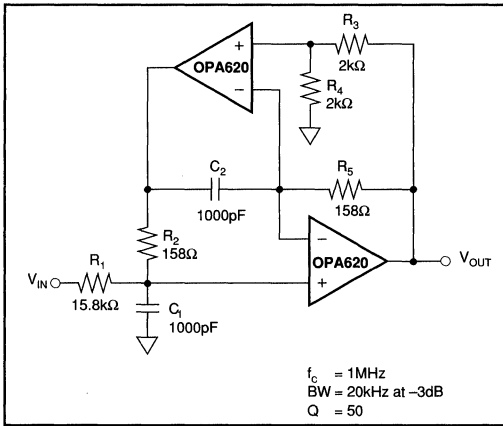


FIGURE 12. High-Q 1MHz Bandpass Filter.

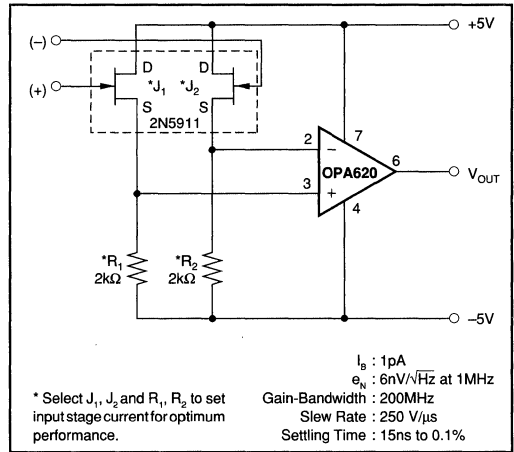


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

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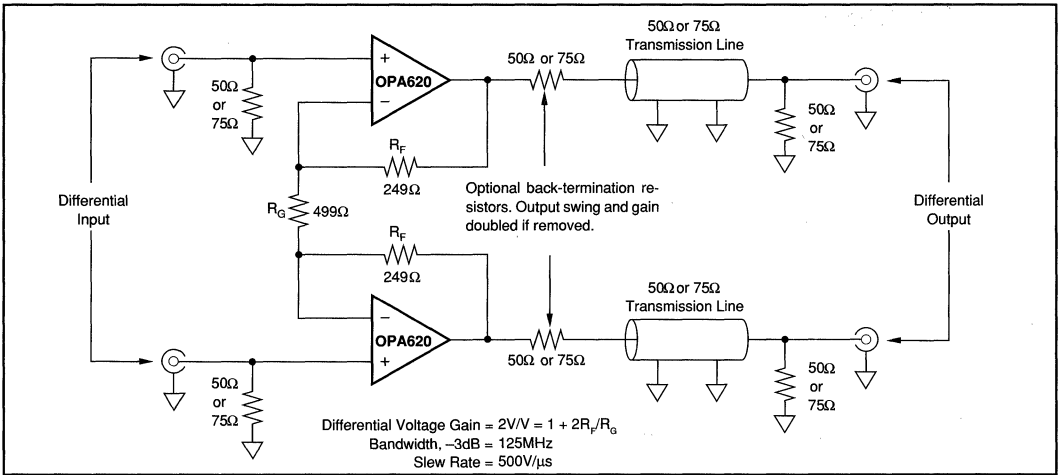


FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

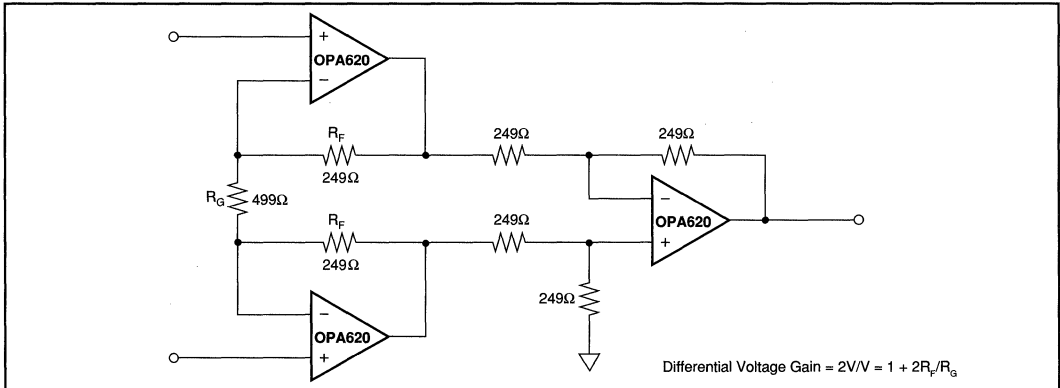


FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

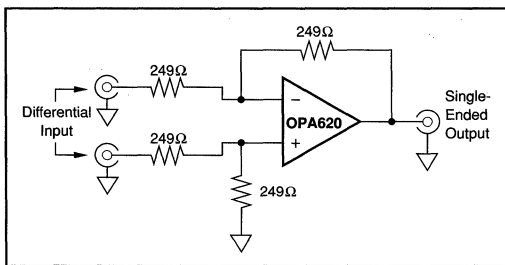


FIGURE 16. Unity Gain Difference Amplifier.

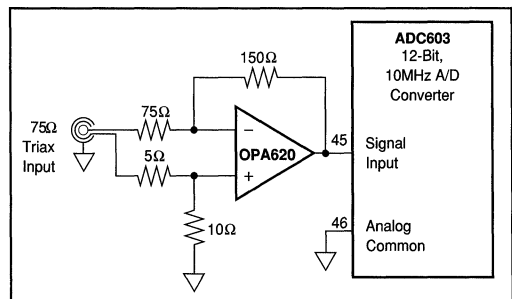
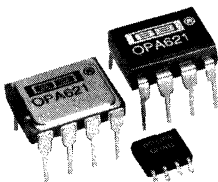


FIGURE 17. Differential Input Buffer Amplifier ($G = -2V/V$).

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA621

OPA621

2

OPERATIONAL AMPLIFIERS

Wideband Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: $2.3\text{nV}/\sqrt{\text{Hz}}$
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- HIGH OUTPUT CURRENT: 150mA
- FAST SETTling: 25ns (0.01%)
- GAIN-BANDWIDTH: 500MHz
- STABLE IN GAINS: $\geq 2\text{V}/\text{V}$
- LOW OFFSET VOLTAGE: $\pm 100\mu\text{V}$
- SLEW RATE: $500\text{V}/\mu\text{s}$
- 8-PIN DIP, SOIC PACKAGES

APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LINE DRIVER
- HIGH-SPEED SIGNAL PROCESSING
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

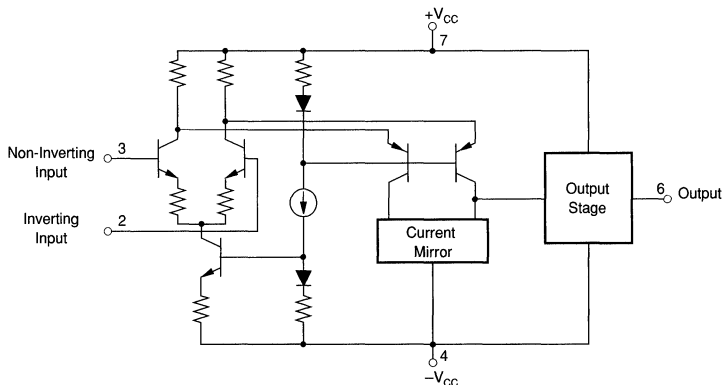
The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of $\pm 2\text{V}/\text{V}$ or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" am-

plifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: -40°C to $+85^{\circ}\text{C}$ and -55°C to $+125^{\circ}\text{C}$.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-939E

2.143

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU			OPA621KG, SG			OPA621LG			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT NOISE Voltage: $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$ $f_o = 100kHz$ $f_o = 1MHz$ to 100MHz $f_b = 100Hz$ to 10MHz Current: $f_o = 10kHz$ to 100MHz	$R_s = 0\Omega$		10			*			*		nV/\sqrt{Hz}	
			5.5			*			*		nV/\sqrt{Hz}	
			3.3			*			*		nV/\sqrt{Hz}	
			2.5			*			*		nV/\sqrt{Hz}	
			2.3			*			*		nV/\sqrt{Hz}	
			8.0			*			*		$\mu V, rms$	
			2.3			*			*		pA/\sqrt{Hz}	
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to T_{MAX} $\pm V_{CC} = 4.5V$ to 5.5V		± 200	$\pm 1mV$		*	*		± 100	± 500	μV $\mu V/^\circ C$ dB	
		50	± 12	60	*	*		55	*	*		
BIAS CURRENT Input Bias Current	$V_{CM} = 0VDC$		18	30		*	*		*	25	μA	
OFFSET CURRENT Input Offset Current	$V_{CM} = 0VDC$		0.2	2		*	*		*	*	μA	
INPUT IMPEDANCE Differential Common-Mode	Open-Loop		$15 \parallel 1$			*	*		*	*	$k\Omega \parallel pF$ $M\Omega \parallel pF$	
			$1 \parallel 1$			*	*		*	*		
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$, $V_O = 0VDC$	± 3.0	± 3.5		*	*		*	*		V dB	
		65	75		*	*		70	*			
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$	50	60		*	*		55	*		dB dB	
		48	58		*	*		53	*			
FREQUENCY RESPONSE Closed-Loop Bandwidth (-3dB) Gain-Bandwidth Differential Gain Differential Phase Harmonic Distortion ⁽²⁾ Full Power Response ⁽²⁾ Slew Rate ⁽²⁾ Overshoot Settling Time: 0.1% 0.01% Phase Margin Rise Time	Gain = +2V/V Gain = +5V/V Gain = +10V/V Gain = +10V/V 3.58MHz, G = +2V/V 3.58MHz, G = +2V/V G = +2V/V, f = 10MHz, $V_O = 2Vp-p$ f = 10MHz, Second Harmonic Third Harmonic $V_O = 5Vp-p$, Gain = +2V/V $V_O = 2Vp-p$, Gain = +2V/V 2V Step, Gain = -2V/V 2V Step, Gain = -2V/V 2V Step, Gain = -2V/V Gain = +2V/V Gain = +2V/V, 10% to 90% $V_O = 100mVp-p$; Small Signal $V_O = 6Vp-p$; Large Signal		500			*	*		*	*	MHz MHz MHz MHz %	
			100			*	*		*	*		MHz
			50			*	*		*	*		MHz
			500			*	*		*	*		MHz
			0.05			*	*		*	*		°
			0.05			*	*		*	*		Degrees
			-62	-50		*	*	*	*	*	*	dBc ⁽³⁾
			-80	-70		*	*	*	*	*	*	dBc
			22	32		*	*	*	*	*	*	MHz
			55	80		*	*	*	*	*	*	MHz
			350	500		*	*	*	*	*	*	V/ μs
				15		*	*	*	*	*	*	%
				15		*	*	*	*	*	*	ns
				25		*	*	*	*	*	*	ns
				50		*	*	*	*	*	*	Degrees
RATED OUTPUT Voltage Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 100\Omega$ $R_L = 50\Omega$ 1MHz, Gain = +2V/V Gain = +2V/V Continuous	± 3.0	± 3.5		*	*		*	*		V V Ω pF mA	
		± 2.5	± 3.0		*	*		*	*			
			0.015		*	*		*	*			
			15		*	*		*	*			
		± 150		*	*		*	*				
POWER SUPPLY Rated Voltage Derated Performance Current, Quiescent	$\pm V_{CC}$ $\pm V_{CC}$ $I_o = 0mAADC$	4.0	5	6.0	*	*	*	*	*	*	VDC VDC mA	
			26	28	*	*	*	*	*	*		
TEMPERATURE RANGE Specification: KP, KU, KG, LG, SG SG Operating: KG, LG, SG KP, KU θ_{JA} KG, LG, SG KP KU	Ambient Temperature Ambient Temperature	-40		+85	*		*	*	*	*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$	
					-55			+125				$^\circ C$
					-55			+125	-55		+125	$^\circ C$
					+85							$^\circ C$
							125				125	$^\circ C/W$
				90		100						$^\circ C/W$

* Same Specifications as for KP, KU.

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SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP/KU			OPA621KG/SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification: KP, KU, KG, LG SG	Ambient Temperature	-40		+85	*		*	*		*	°C °C
OFFSET VOLTAGE⁽¹⁾ Average Drift Supply Rejection	Full Temperature Range $\pm V_{CC} = 4.5V$ to $5.5V$	45	± 12 60		*	*	*	50	*	*	$\mu V/^\circ C$ dB
BIAS CURRENT Input Bias Current	Full Temperature, $V_{CM} = 0VDC$		18	40		*	*		*	35	μA
OFFSET CURRENT Input Offset Current	Full Temperature, $V_{CM} = 0VDC$		0.2	5		*	*		*	*	μA
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$, $V_O = 0VDC$	± 2.5 60	± 3.0 75		*	*	*	*	*	*	V dB
OPEN LOOP GAIN, DC Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$	46 44	60 58		*	*	*	52 50	*	*	dB dB
RATED OUTPUT Voltage Output	$R_L = 100\Omega$ $R_L = 50\Omega$	± 3.0 ± 2.5	± 3.5 ± 3.0		*	*	*	*	*	*	V V
POWER SUPPLY Current, Quiescent	$I_O = 0mADC$		26	30		*	*		*	*	mA

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

OPA621

2

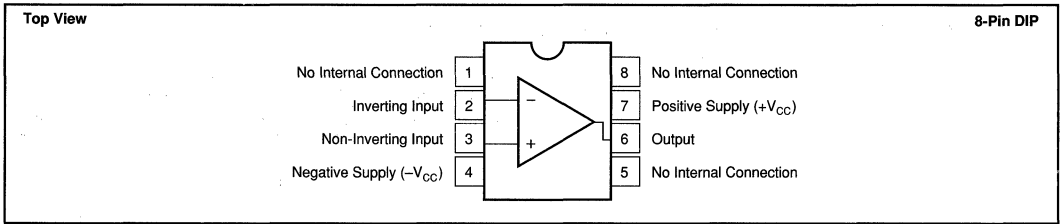
OPERATIONAL AMPLIFIERS

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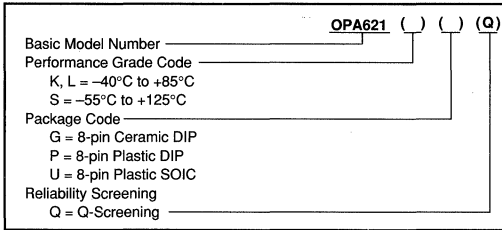


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PIN CONFIGURATION



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V _{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range KG, LG, SG:	-65°C to +150°C
KP, KU:	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T _J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PACKAGE INFORMATION ⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA621KP	8-Pin Plastic DIP	006
OPA621KU	8-Pin Surface Mount	182
OPA621KG	8-Pin Ceramic DIP	157
OPA621SG	8-Pin Ceramic DIP	157
OPA621LG	8-Pin Ceramic DIP	157

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION

OPA621 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	7	-V _{CC}
2	-Input	8	NC
3	+Input	9	V _{OUT}
4	NC	10	+V _{CC}
5	NC	11	NC
6	NC	12	NC
		13	NC

Substrate Bias: Negative Supply -V_{CC}.

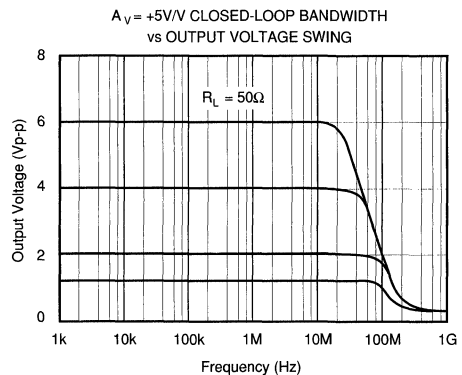
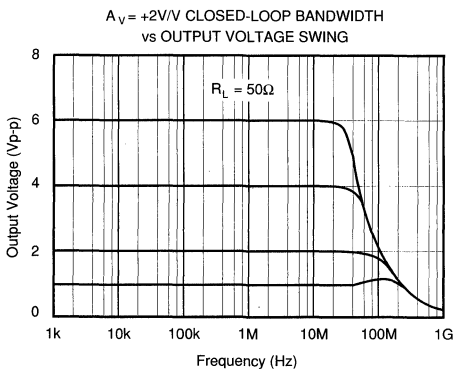
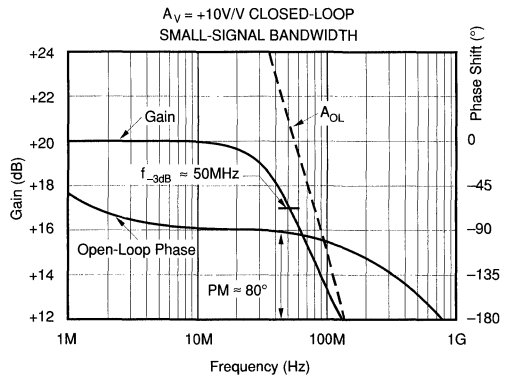
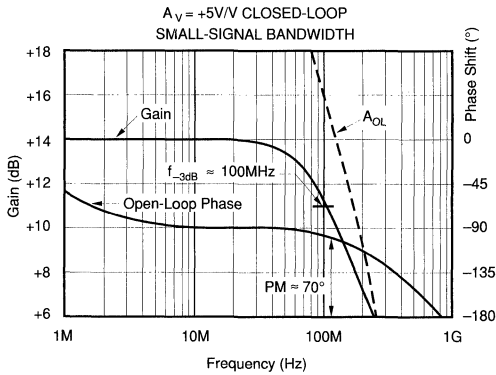
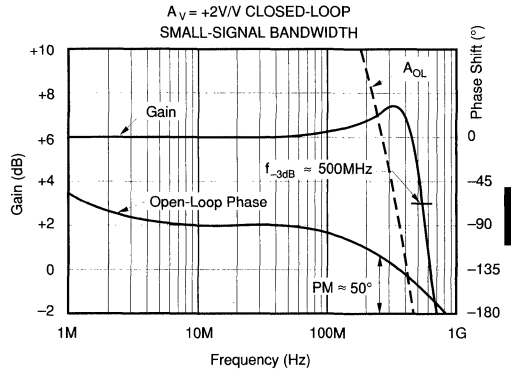
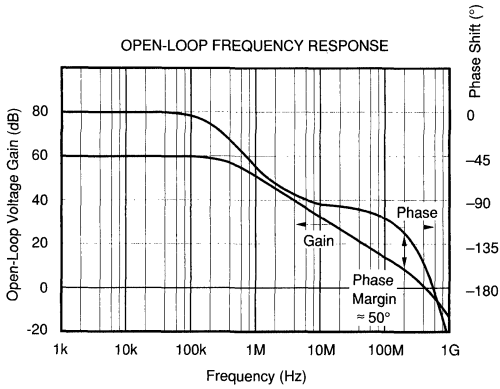
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 47 ±5	1.60 x 1.20 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold
Top Metalization		Gold

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TYPICAL PERFORMANCE CURVES

At $V_{oc} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

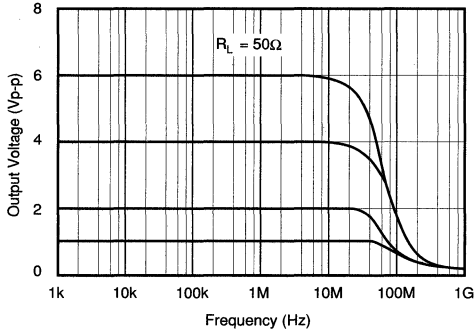


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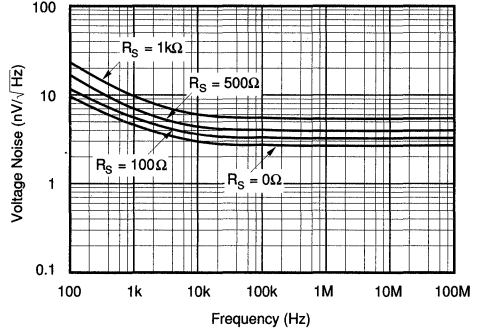
TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

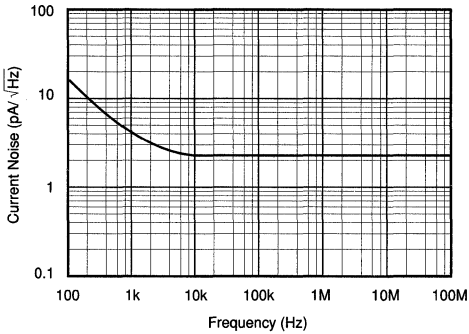
$A_V = +10V/V$ CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



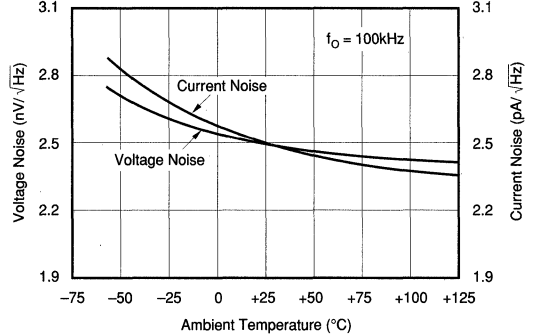
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



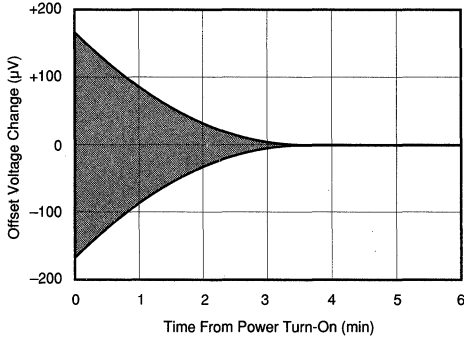
INPUT CURRENT NOISE SPECTRAL DENSITY



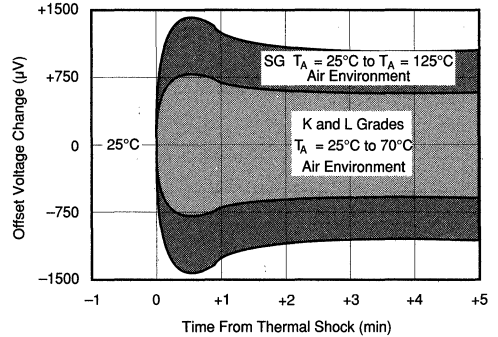
VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY
vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



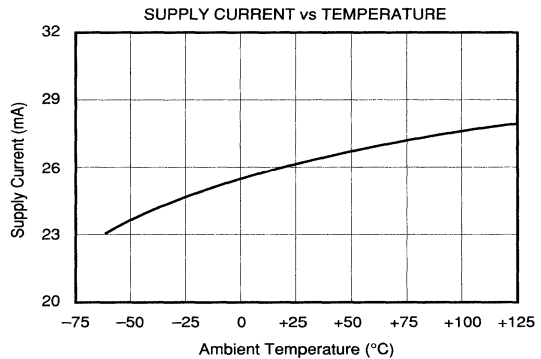
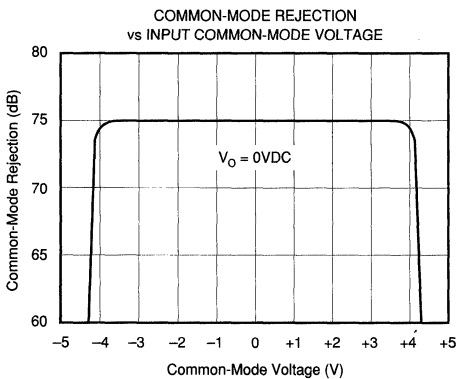
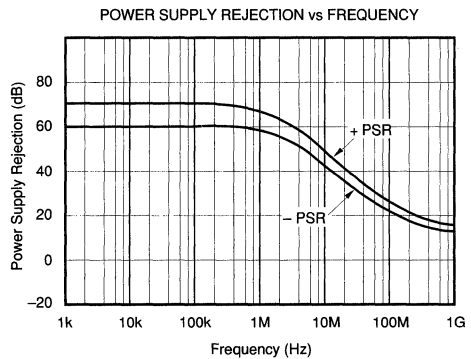
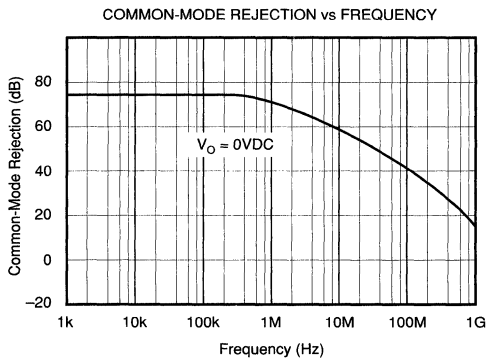
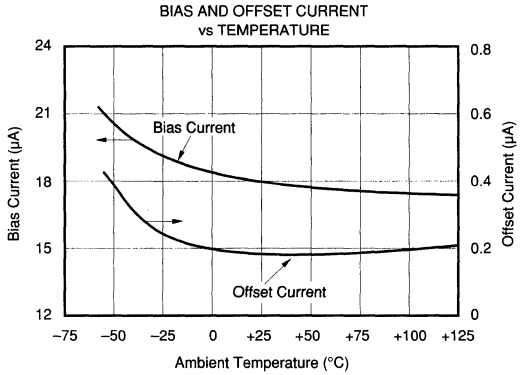
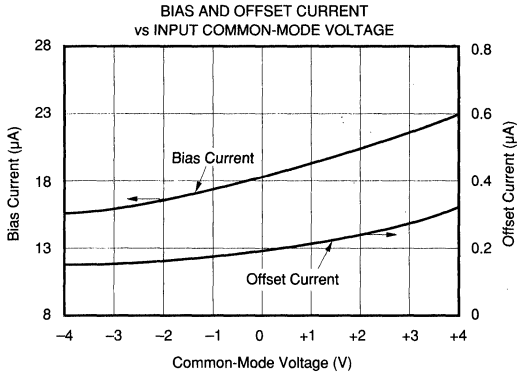
INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



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TYPICAL PERFORMANCE CURVES (CONT)

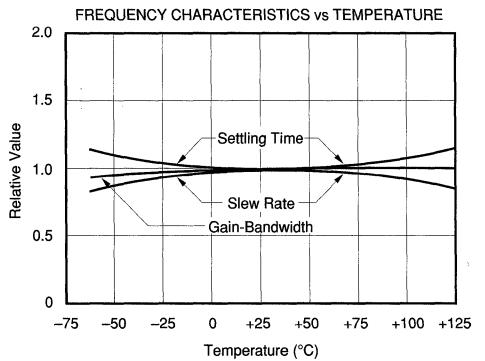
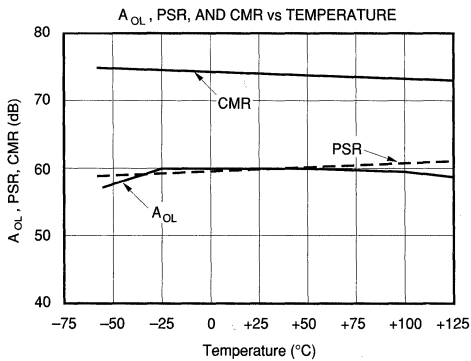
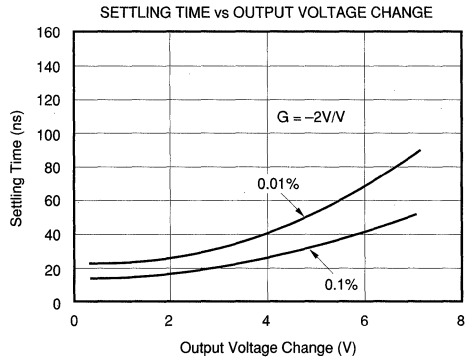
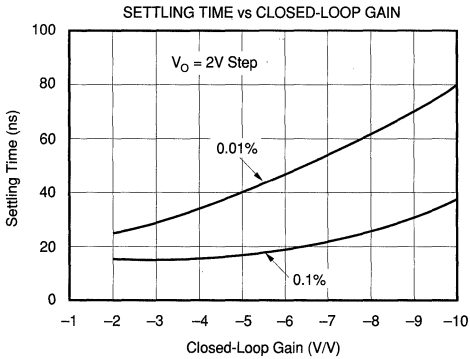
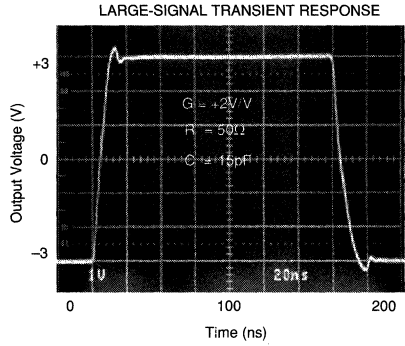
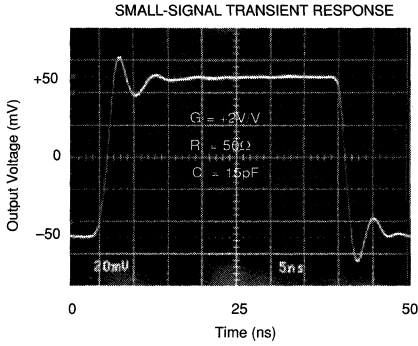
At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

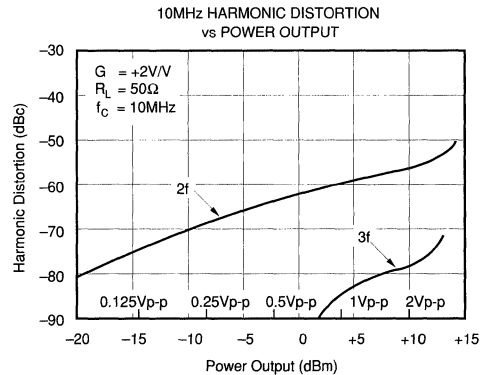
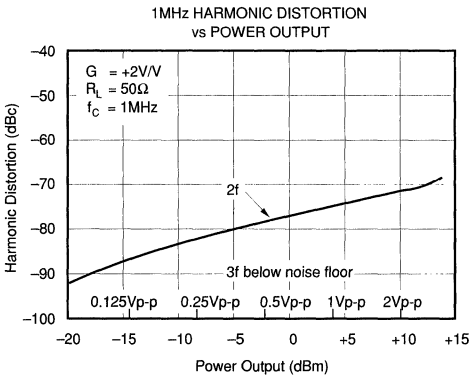
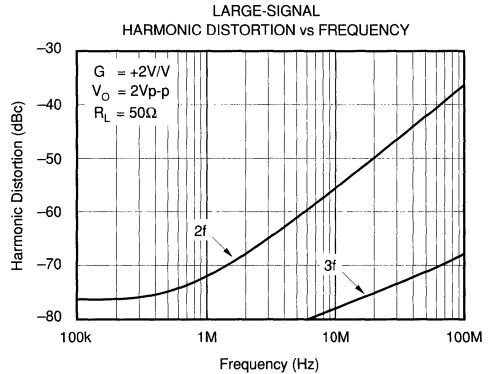
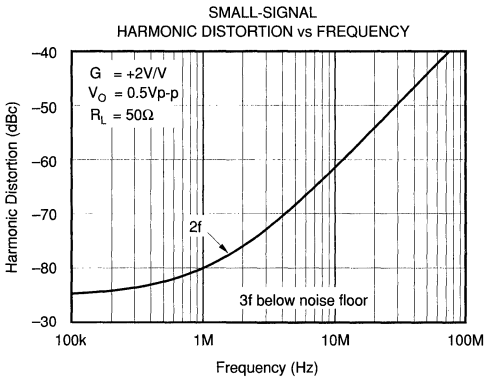
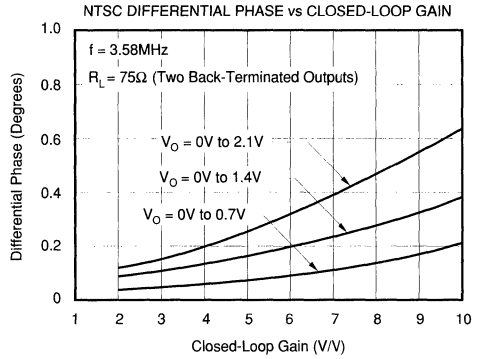
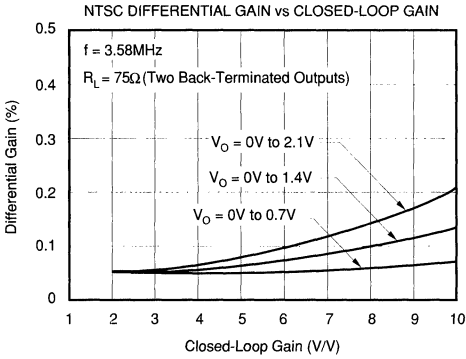
At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100 μ V.

WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration

for the OPA621, as it is with all high-frequency circuits. Oscillations at frequencies of 500MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1 μ F to 10 μ F) with very short leads are recommended. Although not required, a parallel 0.01 μ F ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® stand-offs located close to the amplifier's pins can be used to mount feedback components.
- 4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.
- 5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA621AU (SOIC package) will offer the best AC

performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with $+5V$ and $-5.2V$, use of $\pm 15V$ supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R3. This will reduce input bias current errors to the amplifier's offset current, which is typically only $0.2\mu A$.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about $0.7V$. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of $30mA$ without destruction. To insure long term reliability, however, diode current should be externally limited to $10mA$ or so whenever possible.

Teflon® E. I. Du Pont de Nemours & Co.



The internal protection diodes are designed to withstand $2.5kV$ (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.

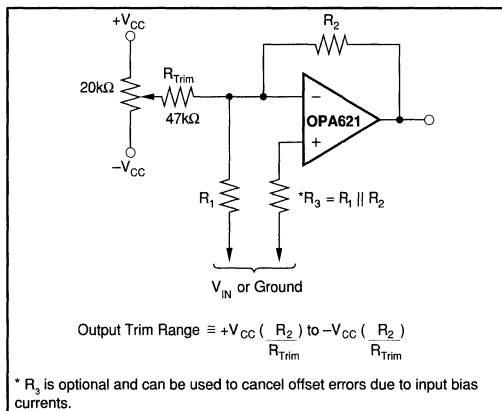


FIGURE 1. Offset Voltage Trim.

OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive $6V_{p-p}$ into a 50Ω load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about $150mA$ at $25^\circ C$. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

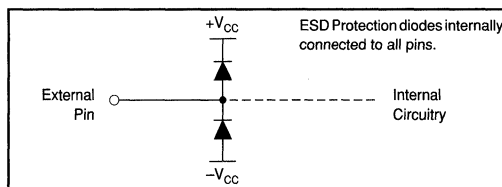


FIGURE 2. Internal ESD Protection.

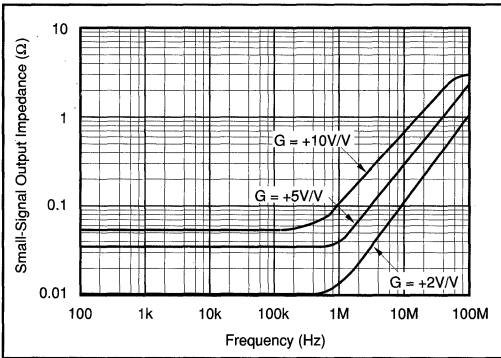


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See “Maximum Power Dissipation” curve, Figure 4.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 28mA = 280mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 280mW + 750mW = 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the “Maximum Power Dissipation” curve starts at 1W and is derated based on a 175°C maximum junction temperature

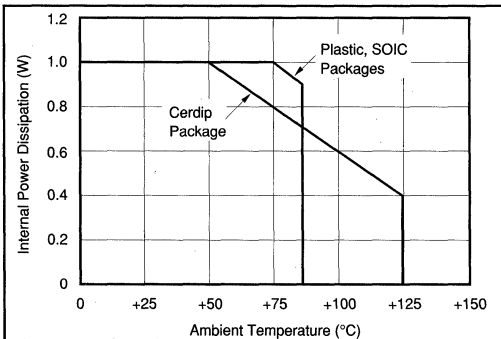


FIGURE 4. Maximum Power Dissipation.

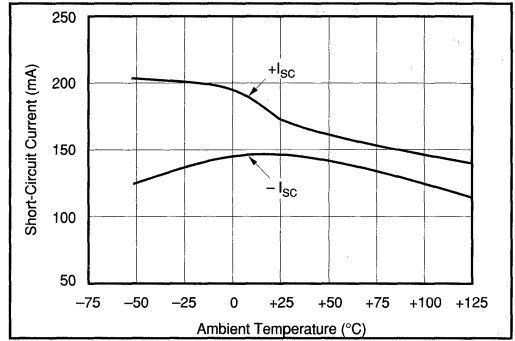


FIGURE 5. Short-Circuit Current vs Temperature.

and the junction-to-ambient thermal resistance, θ_{JA} , of each package. The variation of short-circuit current with temperature is shown in Figure 5.

CAPACITIVE LOADS

The OPA621’s output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier’s phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

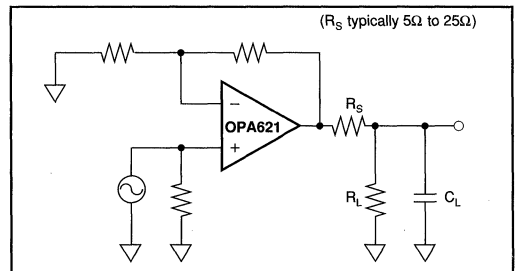


FIGURE 6. Driving Capacitive Loads.

COMPENSATION

The OPA621 is stable in inverting gains of $\geq -2V/V$ and in non-inverting gains $\geq +2V/V$. Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and -2V/V are the most demanding circuit configurations for loop stability and oscillations are most

likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of $-2V/V$ is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu V$ centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical atten-

tion to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

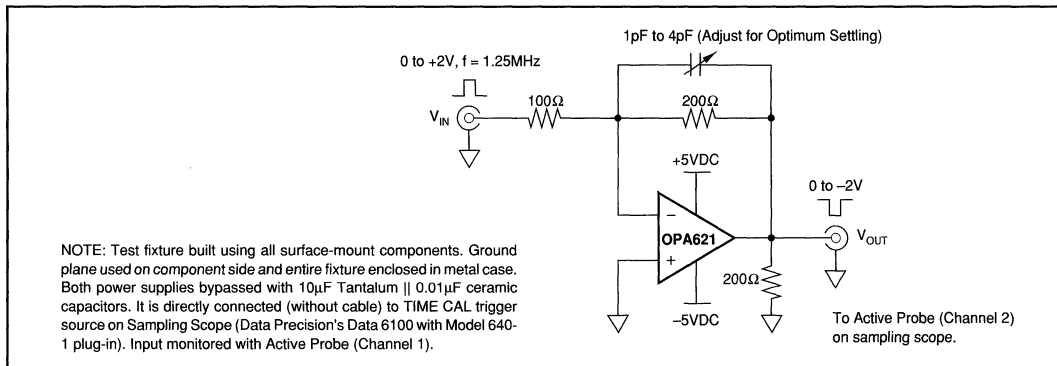


FIGURE 7. Settling Time Test Circuit.

DISTORTION

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - \text{P}_o)$$

where OPI^3P = third-order output intercept, dBm

P_o = output level/tone, dBm/tone

Third IMD = third-order intermodulation ratio below each output tone, dB

For this case $\text{OPI}^3\text{P} = 47\text{dBm}$, $\text{P}_o = 10\text{dBm}$, and the third-order $\text{IMD} = 2(47 - 10) = 74\text{dB}$ below either 10dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

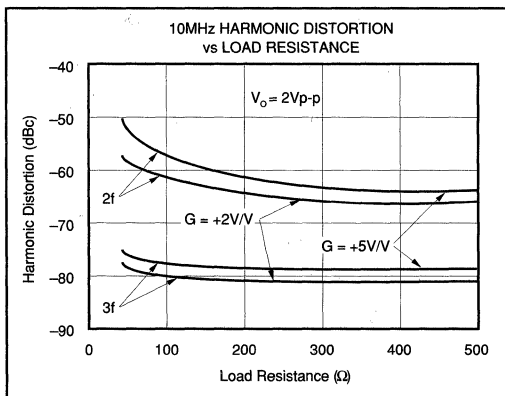


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

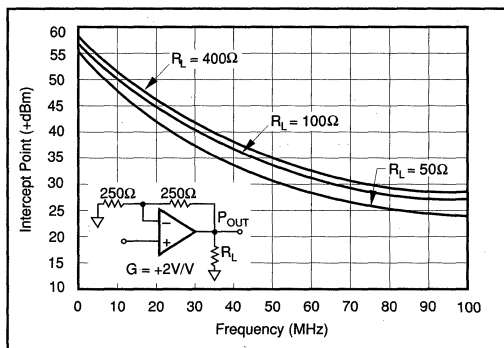


FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA621. Request Burr-Brown Application Note AN-167.

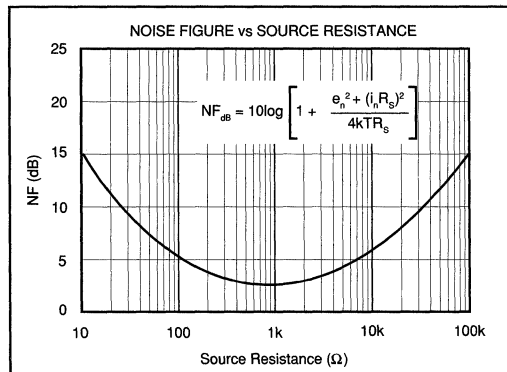


FIGURE 10. Noise Figure vs Source Resistance.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown “Q-Screening” provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = -55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 ⁻¹⁰ atm cc/s Gross: Perfluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on SG package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

APPLICATIONS

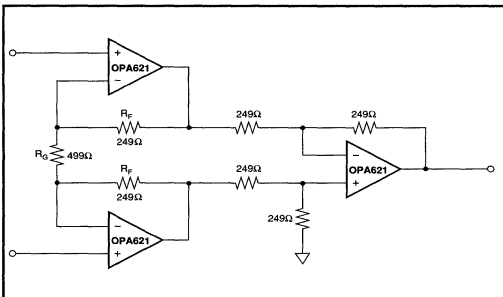


FIGURE 11. Unity Gain Difference Amplifier.

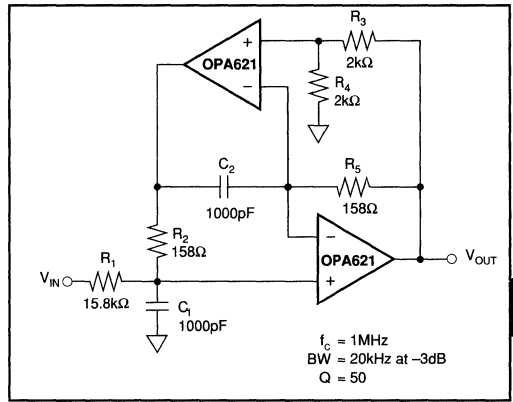


FIGURE 12. High-Q 1MHz Bandpass Filter

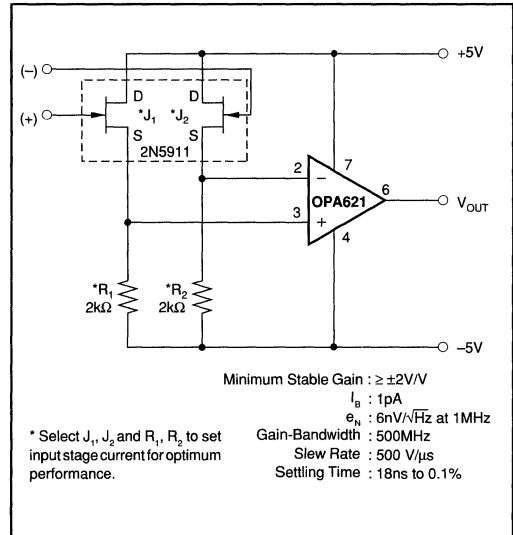


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

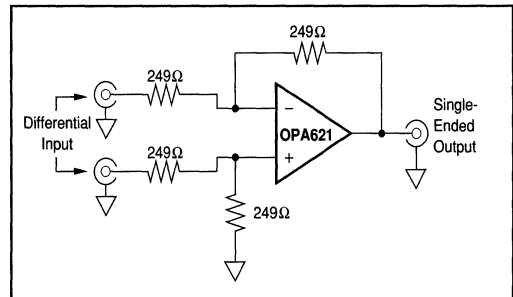


FIGURE 14. Differential Input Buffer Amplifier (G = -2V/V).

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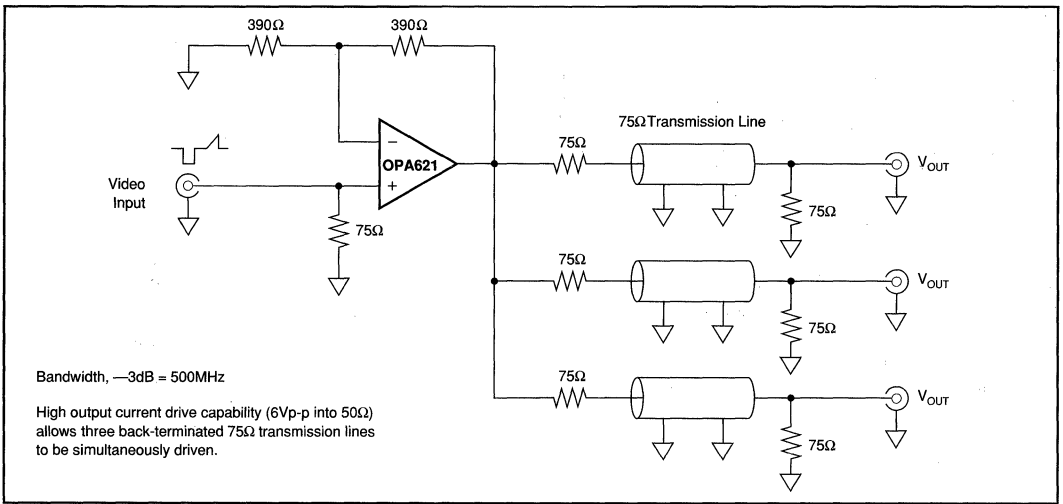


FIGURE 15. Video Distribution Amplifier.

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OPA622

Wide-Bandwidth OPERATIONAL AMPLIFIER

OPA622

2

OPERATIONAL AMPLIFIERS

FEATURES

- **LARGE SIGNAL BANDWIDTH:**
150MHz (AP), 200MHz (AU)
(Voltage-Feedback)
- **HIGH OUTPUT CURRENT:** $\pm 70\text{mA}$
- **SLEW RATE:** 1500V/ μs (AP), 1700V/ μs (AU)
- **DIFFERENTIAL GAIN:** 0.15%
- **DIFFERENTIAL PHASE:** 0.08°
- **EXCELLENT BANDWIDTH/SUPPLY CURRENT RATIO:** 200MHz/5mA
- **LOW INPUT BIAS CURRENT:** $-1.2\mu\text{A}$

APPLICATIONS

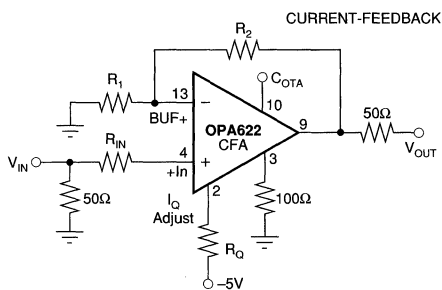
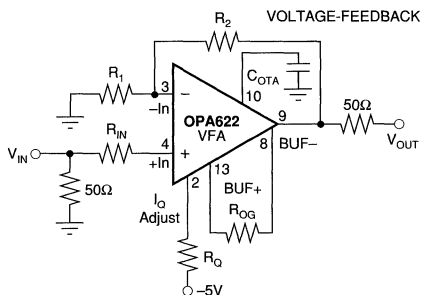
- **BROADCAST/HDTV EQUIPMENT**
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- **PULSE/RF AMPLIFIERS**
- **ACTIVE FILTER**
- **HIGH SPEED ANALOG SIGNAL PROCESSING**
- **MULTIPLIER OUTPUT AMP**
- **DIFFERENTIATOR FOR DIGITIZED VIDEO SIGNALS**

DESCRIPTION

The OPA622 is a monolithic amplifier component designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment. It includes a monolithic integrated current-feedback operational amplifier block and a voltage buffer block, which, when combined, form a voltage-feedback operational amplifier.

When combined as a current-feedback amplifier, it provides a 280MHz large-signal bandwidth at $\pm 2.5\text{V}$ output level and a 1700V/ μs slew rate. The output buffer stage can deliver $\pm 70\text{mA}$ output current. The high output current capability allows the OPA622 to drive two 50 Ω or 75 Ω lines with $\pm 3\text{V}$ output swing, making it ideal along with the low differential gain/phase errors for RF, IF, and video applications.

The feedback buffer stage provides 700MHz bandwidth, a very high slew rate, and a very short signal delay time. It is designed primarily for interstage buffering and not for driving long cables. When combined with the current-feedback amplifier section, the OPA622 can be interconnected as a voltage-feedback amplifier with two identical high-impedance inputs. In this configuration, it features a low common-mode gain, low input offset, and, due to the delay time of the additional feedback buffer, a decrease in frequency bandwidth compared with the current-feedback configuration. Unlike "classical" operational amplifiers, the OPA622 achieves a nearly constant bandwidth over a wide gain and output voltage range. The external setting of the open loop gain with R_{OG} avoids a large compensation capacitor, improves the slew rate, and allows a frequency response adaption to various gains and load conditions.



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SPECIFICATIONS

ELECTRICAL

DC-SPECIFICATION

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_o = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_o = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA622AP, AU			UNITS
		MIN	TYP	MAX	
CLOSED LOOP OFFSET VOLTAGE					
Initial			0.1	± 7	mV
vs Temperature			210		$\mu V/^\circ C$
vs Supply (tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$	-46	-54		dB
vs Supply (non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		-43		dB
vs Supply (non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		-51		dB
\pmINPUT BIAS CURRENT					
Initial			-1.2	± 4	μA
vs Temperature			7		$nA/^\circ C$
vs Supply (tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$		29		nA/V
vs Supply (non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		170		nA/V
vs Supply (non-tracking)	$V_{CC} = -4.5V$ to $5.5V$		58		nA/V
OFFSET CURRENT					
Input Offset Current	$V_{CM} = 0VDC$		0.1		nA
INPUT IMPEDANCE					
Differential Mode			$2.4 \parallel 1$		$M\Omega \parallel pF$
INPUT NOISE					
Voltage Noise Density	$f = 100kHz$ to $100MHz$		11		nV/\sqrt{Hz}
Signal-to-Noise Ratio	$S/N = 20 \log 0.7/(V_n \cdot \sqrt{5MHz})$		89		dB
INPUT VOLTAGE RANGE					
Common Mode Input Range		± 3	± 3.2		V
Common Mode Rejection	$V_i = +2.5VDC$, $V_o = 0VDC$		78		dB
RATED OUTPUT					
Voltage Output		± 3	± 3.2		V
Closed Loop Output Impedance			$0.2 \parallel 1.5$		$\Omega \parallel pF$
Current Output			70		mA
POWER SUPPLY					
Rated Voltage			± 5		VDC
Derated Performance		± 4		± 6	VDC
Quiescent Current	$R_o = 430\Omega$, $I_o = 0mADC$	± 4.4	± 5	± 5.6	mA
Quiescent Current (programmable)	Useful Range, $I_o = 0mADC$	3		8	mA
Rejection Ratio		-46	-54		dB
TEMPERATURE					
Specification	Ambient Temperature	-40		85	$^\circ C$
Storage	Ambient Temperature	-40		125	$^\circ C$

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	$\pm 6V$
Input Voltage ⁽¹⁾	$\pm V_{CC}$ to $\pm 0.7V$
Operating Temperature	$-40^\circ C$ to $+85^\circ C$
Storage Temperature	$-40^\circ C$ to $+125^\circ C$
Junction Temperature	$+150^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PACKAGE INFORMATION⁽¹⁾

MODEL	DESCRIPTION	PACKAGE DRAWING NUMBER
OPA622AP	Plastic 14-Pin DIP	010
OPA622AU	SO-14 Surface-Mount	235

NOTE:(1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
OPA622AP	Plastic 14-Pin DIP	$-40^\circ C$ to $+85^\circ C$
OPA622AU	SO-14 Surface-Mount	$-40^\circ C$ to $+85^\circ C$

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ELECTRICAL

AC-SPECIFICATION

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_O = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_O = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA622AP	OPA622AU	UNITS
		TYP	TYP	
FREQUENCY DOMAIN				
LARGE SIGNAL Closed Loop Bandwidth (–3dB)	$V_O = 2.8Vp-p$, Gain = +1V/V	220	250	MHz
	$V_O = 2.8Vp-p$, Gain = +2V/V	200	250	MHz
	$V_O = 2.8Vp-p$, Gain = +5V/V	170	230	MHz
	$V_O = 2.8Vp-p$, Gain = +10V/V	110	110	MHz
	$V_O = 2.8Vp-p$, Gain = –1V/V	150	250	MHz
	$V_O = 2.8Vp-p$, Gain = –2V/V	160	250	MHz
	$V_O = 5.0Vp-p$, Gain = +2V/V	150	200	MHz
SMALL SIGNAL BANDWIDTH	$V_O = 0.2Vp-p$, Gain = +2V/V	150	170	MHz
GROUP DELAY TIME		1.4	1.4	ns
DIFFERENTIAL GAIN	$f = 4.43MHz$, $R_{LOAD} = 150\Omega$ $V_O = 0.7V$, Gain = +1V/V	0.12	0.12	%
	$V_O = +1.4V$, Gain = +2V/V	0.15	0.15	%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $R_{LOAD} = 150\Omega$ $V_O = 0.7V$, Gain = +1V/V	0.06	0.06	Degrees
	$V_O = +1.4V$, Gain = +2V/V	0.08	0.08	Degrees
HARMONIC DISTORTION Second Harmonic 2f Third Harmonic 3f Second Harmonic 2f Third Harmonic 3f Second Harmonic 2f Third Harmonic 3f	Gain = +2V/V $f = 10MHz$, $V_O = 2.8Vp-p$	–57	–57	dBc
		–55	–55	dBc
	$f = 30MHz$, $V_O = 2.8Vp-p$	–38	–38	dBc
		–43	–43	dBc
	$f = 50MHz$, $V_O = 2.8Vp-p$	–33	–33	dBc
	–30	–30	dBc	
GAIN FLATNESS PEAKING	Gain = +2V/V $V_O = 2.8Vp-p$, DC to 30MHz	0.12	0.12	dB
	$V_O = 2.8Vp-p$, DC to 100MHz	0.3	0.3	dB
TIME DOMAIN				
RISE TIME	Gain = +2V/V, 10% to 90% $V_O = 5Vp-p$, $C_L = 2pF$	2.4	2.7	ns
FALL TIME	Gain = +2V/V, 10% to 90% $V_O = 5Vp-p$, $C_L = 2pF$	3.5	3.2	ns
SLEW RATE	Gain = +2V/V, Rise Time = 2ns $V_O = 6.2Vp-p$			
	Positive	1500	1700	V/ μs
Negative	1300	1600	V/ μs	
SETTLING TIME	Gain = +2V/V, Rise Time = 2ns $V_O = 2Vp-p$, 0.1%	17	17	ns

OPA622

2

OPERATIONAL AMPLIFIERS

ELECTRICAL (FULL TEMPERATURE RANGE, –40°C to +85°C)

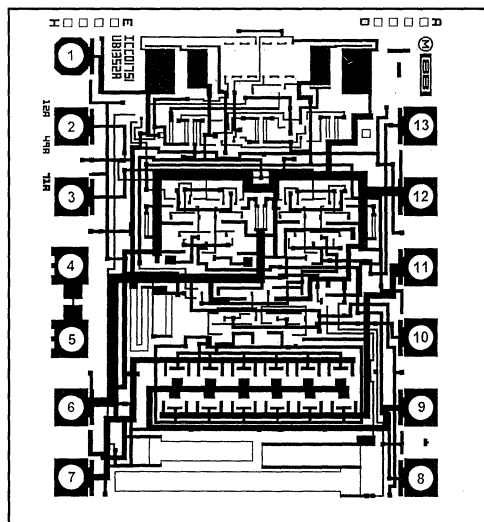
VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_O = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_O = 430\Omega$, and $R_{OG} = 150\Omega$.

PARAMETER	CONDITIONS	OPA622AP, AU			UNITS
		MIN	TYP	MAX	
CLOSED LOOP OFFSET VOLTAGE Initial			0.1	+30/–25	mV
BIAS CURRENT \pm Input Bias Current	$V_{cm} = 0VDC$		–1.5	± 5	μA
OFFSET CURRENT Input Offset Current	$V_{cm} = 0VDC$		0.1	+0.2/–0.3	μA
INPUT VOLTAGE RANGE Common Mode Input Range		± 3	± 3.2	± 3.4	V
RATED OUTPUT		± 3	± 3.2		V
POWER SUPPLY Quiescent Current	$I_O = 0mADC$	± 4.4	± 5	± 5.7	mA



DICE INFORMATION



OPA622AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Quiescent Current Adjustment
2	Inverting Analog Input
3	Non-Inverting Analog Input
4	NC
5	NC
6	-5V Supply
7	-5V Supply, Output
8	Inverting Buffer Output
9	Analog Output
10	Analog OTA Output
11	+5V Supply, Output
12	+5V Supply
13	Non-Inverting Buffer Output

Substrate Bias: Negative Supply

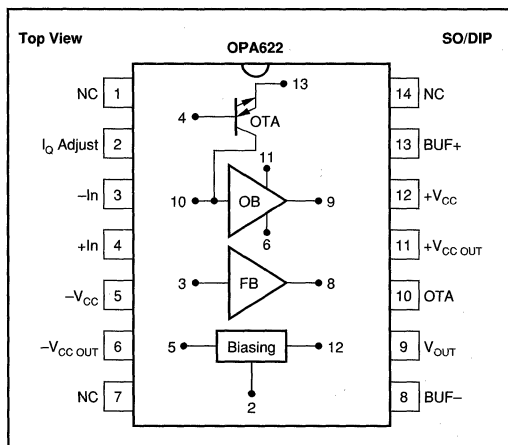
NC: No Connection

Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	57 x 69 ±5	1.44 x 1.76 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02+0.05,-0.0	0.0005+0.0013, -0.0
Gold	0.30±0.05	0.0076 ±0.0013

PIN CONFIGURATION



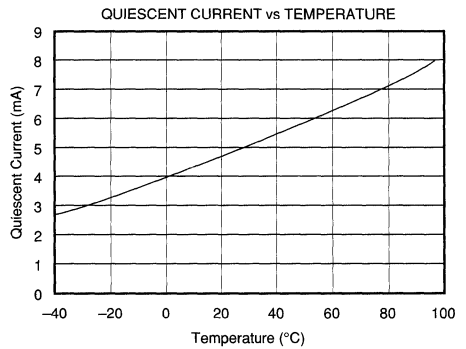
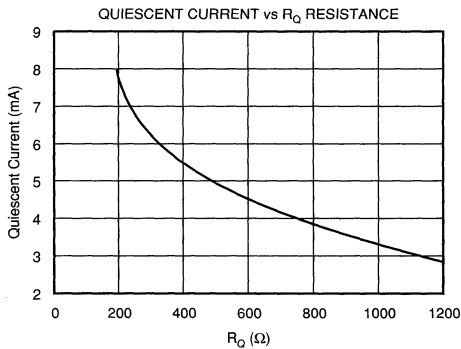
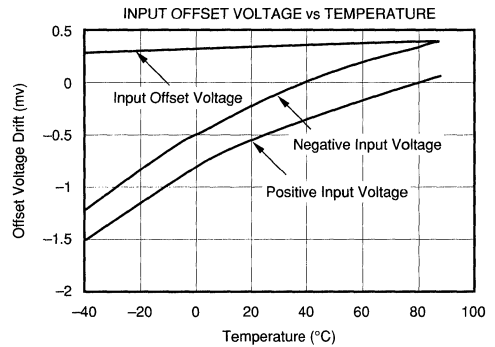
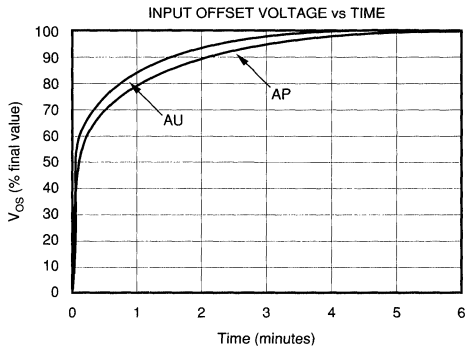
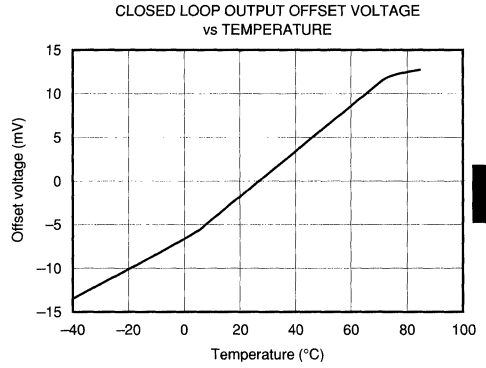
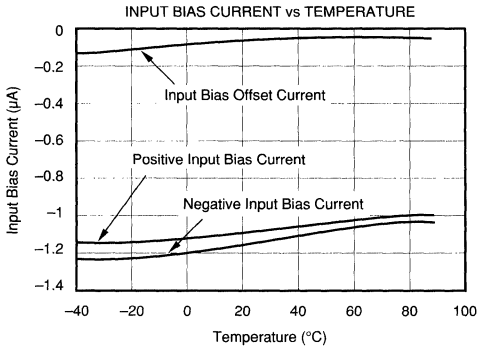
FUNCTIONAL DESCRIPTION

PIN NO.	DESCRIPTION	FUNCTION
1	NC	No Connection
2	I_o Adjust	Quiescent Current Adjustment; typical 3-8mA
3	-In	Inverting Analog Input
4	+In	Noninverting Analog Input
5	- V_{cc}	Negative Supply Voltage; typical -5VDC
6	- $V_{cc OUT}$	Negative Supply Voltage Output Buffer; typical -5VDC
8	BUF-	Analog Output Feedback Buffer
9	V_{OUT}	Analog Output
10	OTA	Analog Output OTA
11	+ $V_{cc OUT}$	Positive Supply Voltage Output Buffer; typical +5VDC
12	+ V_{cc}	Positive Supply Voltage; typical +5VDC
13	BUF+	Analog Output/Input
14	NC	No Connection

TYPICAL PERFORMANCE CURVES

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_Q = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_O = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.



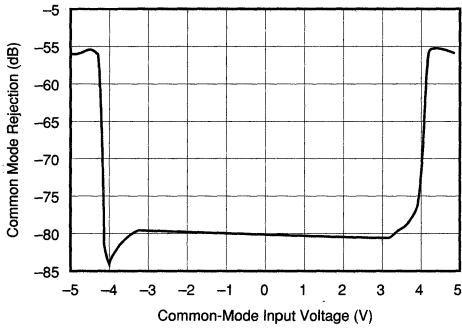
For Immediate Assistance, Contact Your Local Salesperson

TYPICAL PERFORMANCE CURVES (CONT)

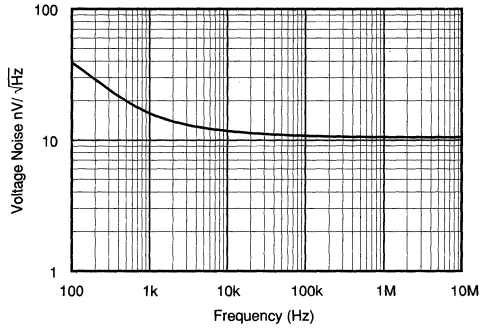
VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_o = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_o = 430\Omega$, $R_{CO} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.

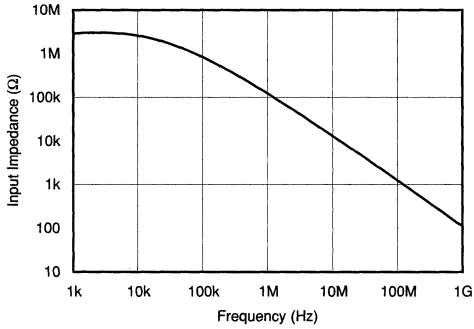
COMMON-MODE REJECTION
vs COMMON-MODE INPUT VOLTAGE



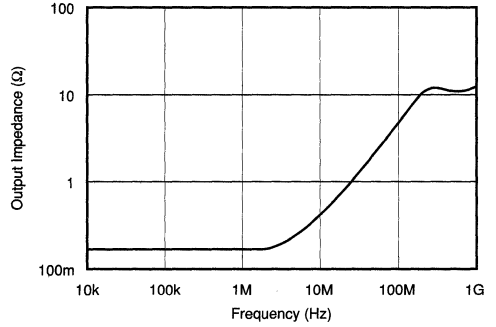
SPECTRAL NOISE VOLTAGE DENSITY



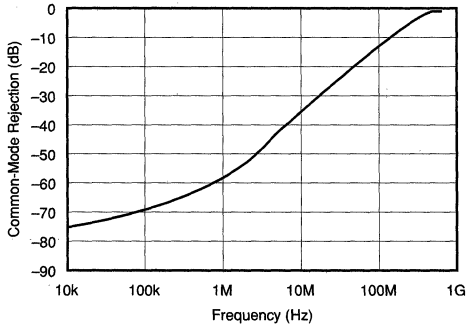
INPUT IMPEDANCE vs FREQUENCY



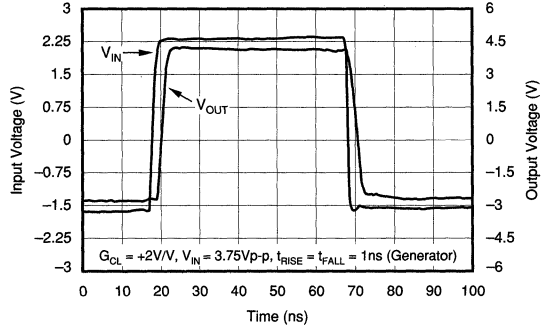
OUTPUT IMPEDANCE vs FREQUENCY



COMMON MODE REJECTION vs FREQUENCY



OVERLOAD RECOVERY CHARACTERISTICS

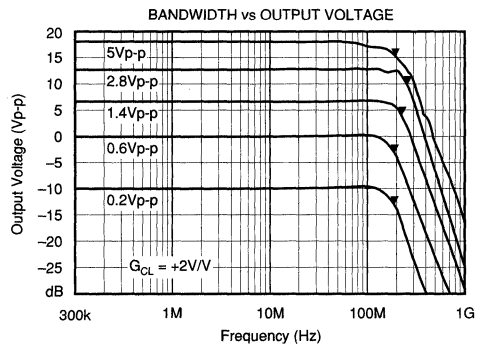
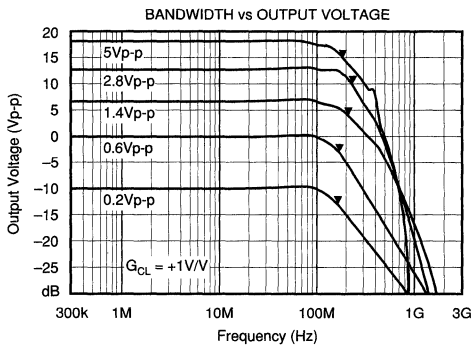
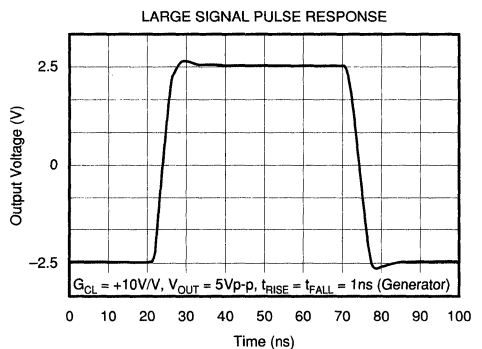
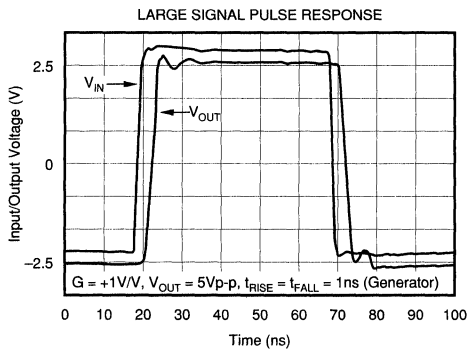
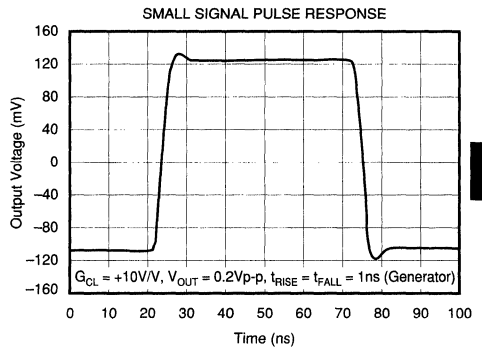
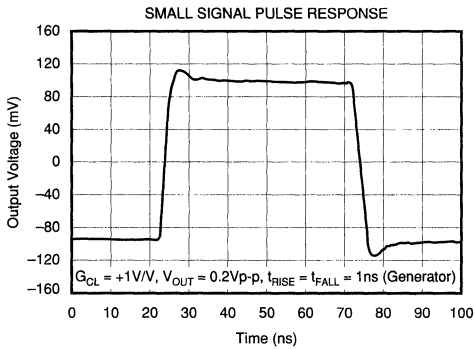


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TYPICAL PERFORMANCE CURVES (CONT)

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_Q = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_Q = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.

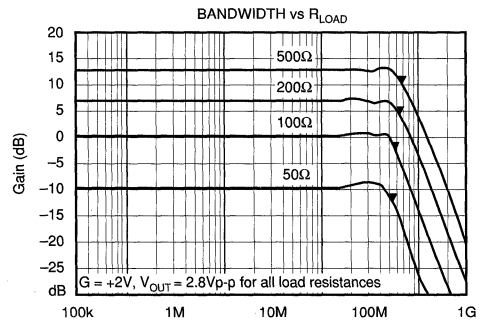
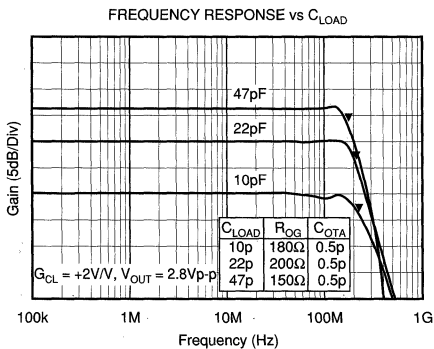
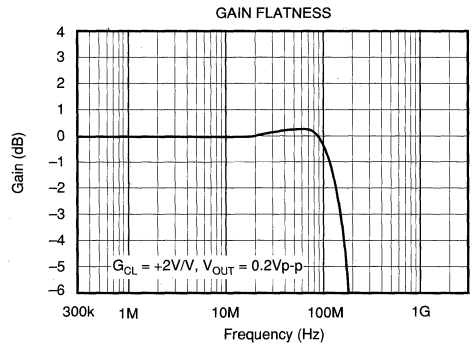
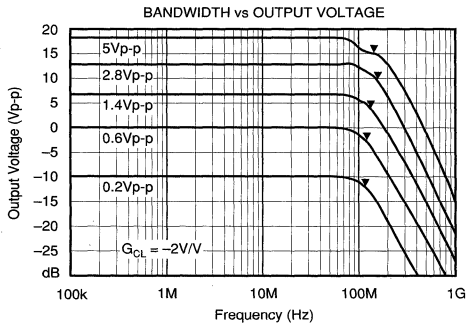
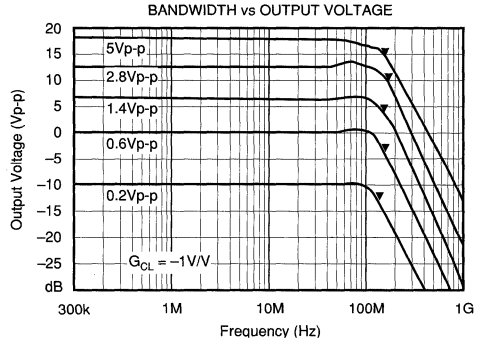
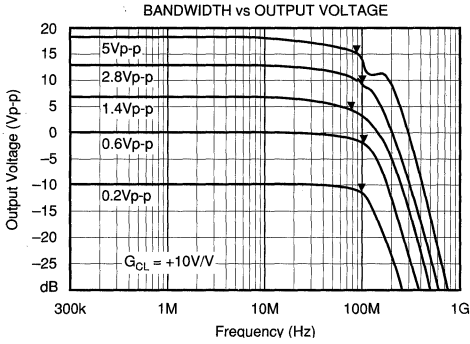


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TYPICAL PERFORMANCE CURVES (CONT)

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_Q = \pm 5mA$, $G_{CL} = +2V/V$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_O = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.

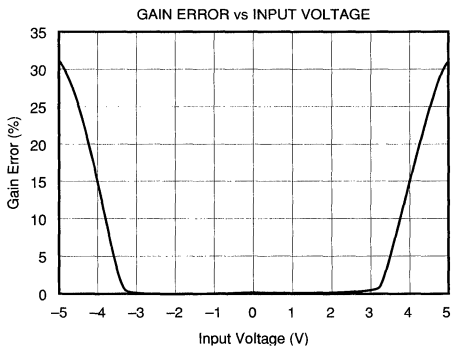
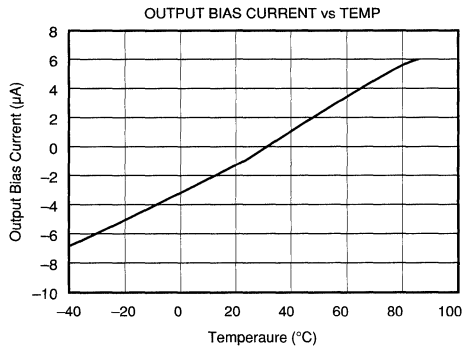
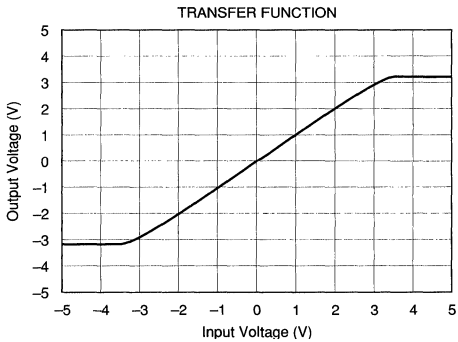
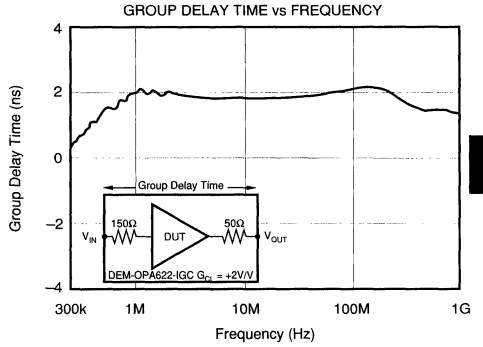
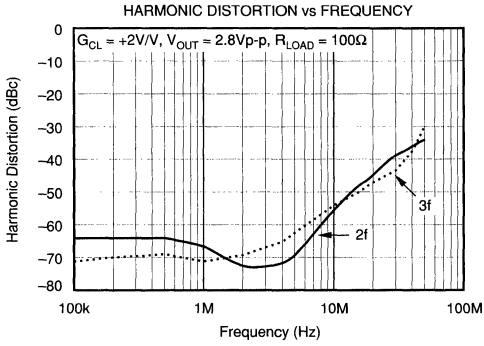


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TYPICAL PERFORMANCE CURVES (CONT)

VOLTAGE-FEEDBACK AMPLIFIER (Figure 5)

At $V_{CC} = \pm 5VDC$, $I_Q = \pm 5mA$, $G_{CL} = +2V/V$, $V_{OUT} = 2.8Vp-p$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_O = 430\Omega$, $R_{OG} = 150\Omega$ and $T_A = +25^\circ C$ unless otherwise specified.



OPA622

OPERATIONAL AMPLIFIERS

INPUT PROTECTION

The need for protection from static damage has long been recognized for MOSFET devices, but all semiconductor devices deserve protection from this potentially damaging source. The OPA622 incorporates on-chip ESD protection diodes as shown in Figure 1. These diodes eliminate the need for external protection diodes, which can add capacitance and degrade AC performance.

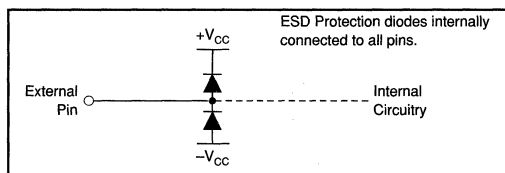


FIGURE 1. Internal ESD Protection.

As shown, all input pins of the OPA622 are protected from ESD internally by a pair of back-to-back reverse-biased diodes to either power supply. These diodes begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur when the amplifier loses its power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, the diode current should be limited externally to approximately 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the amplifier input characteristics without necessarily destroying the device. In precision amplifiers, such changes

may degrade offset and drift noticeably. For this reason, static protection is strongly recommended when handling the OPA622.

DISCUSSION OF PERFORMANCE

The OPA622 provides a level of full-power bandwidth previously unattainable in monolithic devices. In addition, the amplifier operates with reduced quiescent current and lower input bias current, which are very important factors in an increasingly complex electronic environment. The flexibility of the OPA622 design enables engineers to choose the speed advantages of a current-feedback amplifier or the precision advantages of a voltage-feedback amplifier such as two symmetrical inputs, low offset voltage, high impedance inputs, and a better CMRR. The programmable quiescent current feature also helps to adapt the amplifier to the particular design requirements.

The OPA622 is specified for the extended industrial temperature range (-40°C to $+85^{\circ}\text{C}$) and is available in 14-pin plastic surface assembly or 14-pin plastic DIP.

Figure 2 shows the simplified circuit diagram of the OPA622. It contains four major sections: the bias circuitry, the OTA and output buffer sections, and the feedback buffer section.

BIAS CIRCUITRY

The bias circuitry controls the quiescent current of the signal processing stages, allows external quiescent current setting using the resistor R_Q connected from Pin 2 to $-V_{CC}$, sets the amplifier's transconductance, and, with its temperature characteristics, maintains a constant transconductance over temperature. The quiescent current controls the small-signal bandwidth and AC behavior. The OPA622 is specified with

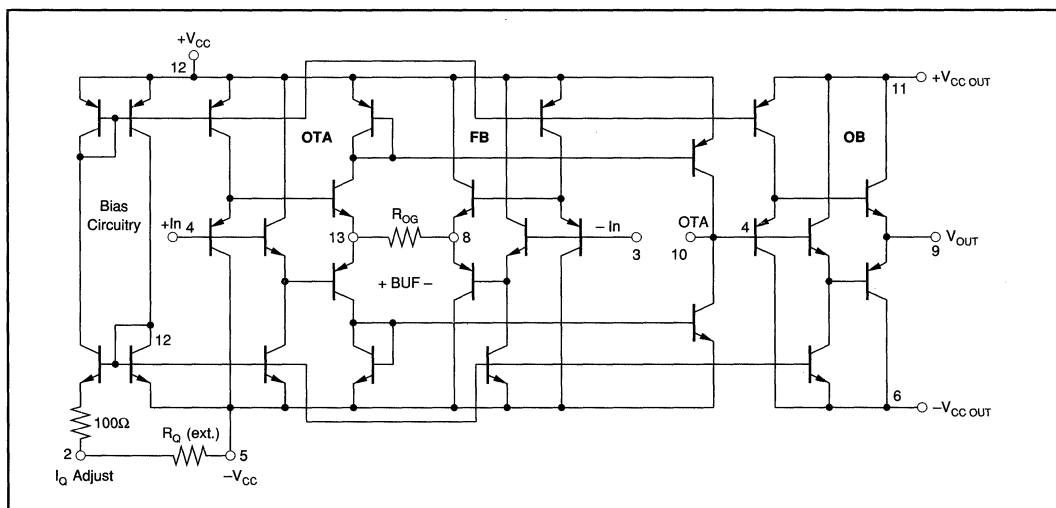


FIGURE 2. Simplified Circuit Diagram.

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a quiescent current of $\pm 5\text{mA}$. The recommended range is $\pm 3\text{mA}$ to $\pm 8\text{mA}$. An R_O of 430Ω sets approximately $\pm 5\text{mA}$ total quiescent current at $+25^\circ\text{C}$.

Application circuits generally do not show the resistor R_O , but it is required for proper operation.

With a fixed R_O , the quiescent current increases with temperature (see Typical Performance Curves.) This variation of the quiescent current with temperature keeps the bandwidth and AC behavior constant with temperature as well. It is also possible to vary the quiescent current by an external control signal or circuitry. Figure 3 shows a logic-controlled disable circuit to disable the OPA622 with TTL-compatible logic levels. $0\text{V}/5\text{V}$ logic levels are converted into a $1\text{mA}/0\text{mA}$ current connected to Pin 2. The current flowing in R_O increases the voltage at Pin 2 to approximately 1V above the $-V_{CC}$ rail, thus reducing I_Q to near zero and disabling the OPA622.

OTA AND OUTPUT BUFFER SECTIONS

An Operational Transconductance Amplifier (OTA) and an output buffer are the basic building blocks of a current-feedback amplifier. The current-feedback configuration of the OPA622 is illustrated in Figure 4. The OTA consists of a complementary emitter follower and a subsequent complementary current mirror. The voltage at the high-impedance $+In$ terminal is transferred to the $BUF+$ input/output terminal at a low impedance. If a current flows into or out of the $BUF+$ terminal, the complementary mirror reflects the current to the OTA terminal. The current flow at the high-impedance OTA terminal is determined by the product of the voltage between the $+In$ and $BUF+$ terminals and the transconductance. The output buffer section is an open-loop buffer consisting of complementary emitter followers. It is designed to drive cables or low-impedance loads. The buffer output is not current limited or protected. As can be seen in

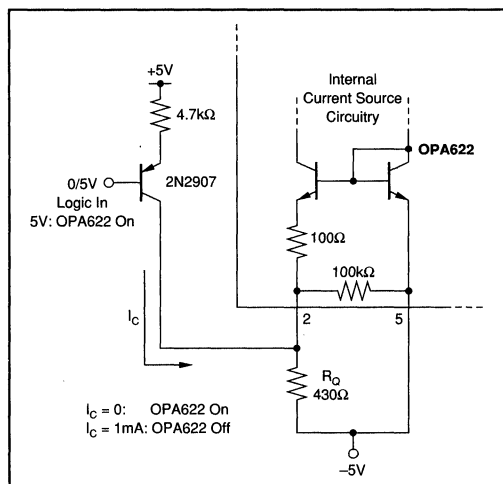


FIGURE 3. Logic-Controlled Disable Circuit.

Figure 4, the feedback network for a current-feedback amplifier is applied between the V_{OUT} and $BUF+$ terminals. Figure 8 illustrates the bandwidth for various output voltages of the current feedback configuration.

FEEDBACK BUFFER SECTION

This section of the OPA622 is a complementary emitter follower identical to the input buffer of the OTA section. It is designed primarily for interstage buffering, not for driving long cables or low-impedance loads. A minimum load resistance of 500Ω is recommended when using the feedback buffer as a stand-alone device. The buffer output is not current-limited or -protected. The bandwidth of the feedback buffer is shown in Figure 7.

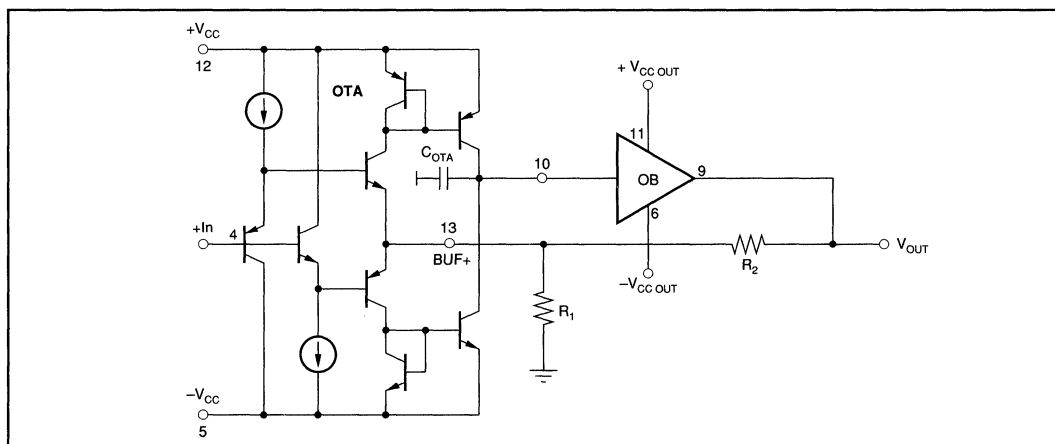


FIGURE 4. Current-Feedback Amplifier.

CONFIGURATIONS

VOLTAGE-FEEDBACK AMPLIFIER

The OPA622's internal design differs from a "classical" operational amplifier structure, but it can nevertheless be used in all traditional operational amplifier applications. As with conventional op amps, the feedback network connected to the inverting input controls closed-loop gain (G_{CL}). But with the OPA622, the resistor R_{OG} is simultaneously adapted to the closed-loop gain, optimizing the frequency response and stability.

The "classical" differential input stage consists of two identical transistors with an emitter degeneration resistor, two current sources, and an active load diode. However, the classical configuration limits the current through the gain transistor to that supplied by the current sources.

In the new design, a complementary push-pull buffer (emitter follower) replaces one side of the differential stage without the 0.7V offset. The feedback buffer as a second complementary emitter follower and the open-loop gain resistor R_{OG} connected between the outputs recreate the differential stage without the disadvantages of the classical design. The current charging the parasitic capacitance at the base of the gain transistor is no longer limited to the fixed current of the current sources and is proportional to the input signal. This improvement results in an approximately 10 times better slew rate.

The amplified current through the gain transistor of one of the buffers is mirrored and becomes the output current. The high-impedance output of the OTA is now buffered by the high current output stage, which is designed to drive long cables or low-impedance loads at full power.

The identical input buffers reduce the input offset to typically less than $\pm 7\mu\text{V}$. Closed-loop output offset is typically

due to mismatch of the NPN and PNP transistors in the OTA mirror $\pm 100\mu\text{V}$ after the output bias current is trimmed.

Figure 5 illustrates the circuit configuration of the voltage-feedback op amp in a complementary circuit design. The feedback buffer and the OTA input buffer form the differential input. Inserting the feedback buffer section transforms the current feedback shown in Figure 4 into the voltage feedback shown in Figure 5.

The resistor R_{OG} sets the open-loop gain and corresponds to the emitter degeneration resistor in the already mentioned classical differential stage. Because the R_{OG} resistor can be varied externally, a flat frequency response can be achieved over a wide range of applications without the need to compensate the amplifier with a capacitor. In contrast to a current-feedback amplifier, it is possible to adjust the closed-loop gain using the feedback resistors and to adjust the open-loop gain separately using R_{OG} to optimize the frequency response.

Unlike "classical" operational amplifier structures, the OPA622 configuration makes it possible to attain a nearly constant bandwidth for varying closed-loop gains, as well as improved frequency response and large-signal behavior. In addition—and also unlike current-feedback op amps—it provides two identical high-impedance inputs, lower input offset values, and improved CMRR.

CURRENT-FEEDBACK AMPLIFIER

Figure 4 shows the current-feedback configuration. The feedback loop is closed from the output to the BUF+ terminal of the OTA section. The shorter feedback loop without the feedback buffer produces the wider bandwidth of the current-feedback concept. The additional signal delay time through the feedback buffer determines the difference in AC performance between voltage and current feedback.

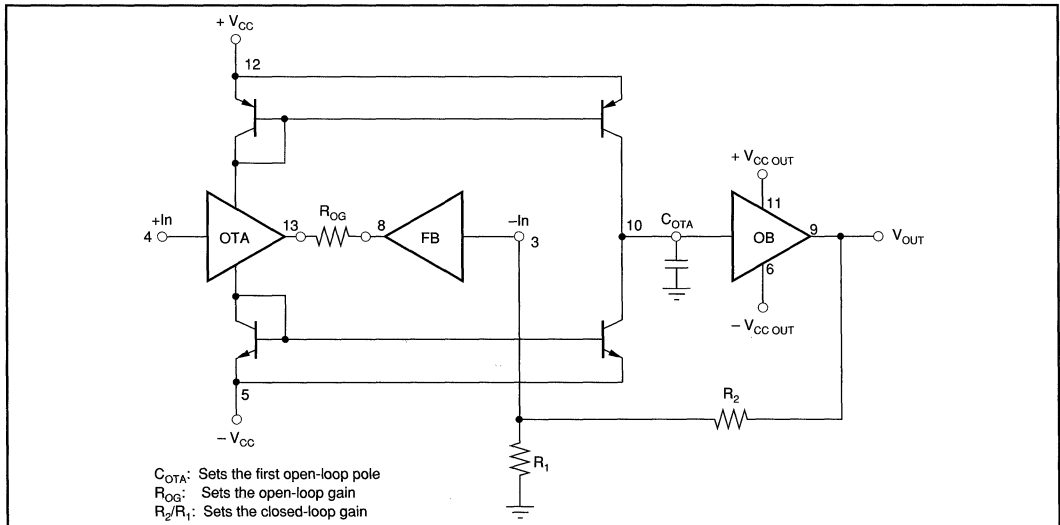


FIGURE 5. Voltage-Feedback Amplifier.

The specifications for offset voltage, CMMR, and settling times are the compromise for higher speed.

The open-loop gain for the current-feedback amplifier varies directly with the closed-loop gain and can be adjusted by changing the size of R2/R1. For gains of less than 10V/V, the open-loop gain can be adjusted to achieve bandwidth independent of gain, but the effects of this adjustment become limited when second-order effects start to dominate.

Figure 6 gives an overview of the OPA622 inverting and noninverting amplifier configurations and shows the equations for the closed-loop gains.

OPTIMAL FREQUENCY RESPONSE ADJUSTMENT

Conventional voltage-feedback op amps use a compensation capacitor for stable unity-gain operation. During transitions, the quiescent current charges and discharges this capacitor, and both parameters determine the slow rate according to:

$$SR = \frac{\Delta V_{OUT}}{\Delta t} = \frac{I}{C}$$

This method is not appropriate for wide-band op amps. The slow rate and thus the large-signal behavior are significantly reduced, and the bandwidth decreases with increasing closed-loop gains according to the gain-bandwidth product.

Amplifiers with an external compensation capacitor allow optimal frequency adjustment versus closed-loop gain, but nevertheless do not significantly improve large-signal behavior. The most effective solution is to make the open-loop gain (G_{OL}) externally adjustable.

The widely-used current-feedback op amp type designed with real complementary circuit techniques overcomes the internal compensation capacitor and allows the feedback

network to set the open-loop gain. The ratio of the feedback resistors determines the low-frequency closed-loop gain, and the parallel impedance defines the amplifier's open-loop gain for stable operation and flat frequency response. A nearly constant bandwidth can be achieved over a wide range of closed-loop gains. However, current-feedback op amps suffer from nonidentical inputs and poor input offset and CMRR. The voltage-feedback op amp OPA622 with its complementary topology features two identical high-impedance inputs, lower input offset values, and improved CMRR. The ratio of the feedback resistors determines the low-frequency closed-loop gain, and the external resistor R_{OG} sets the open-loop gain to achieve a flat frequency response over a wide range of closed-loop gains. Since R_{OG} can be selected, optimized pulse responses are possible even with larger load capacitances. The OPA622 combines the slow rate enhancements of a complementary amplifier design with the precision of a voltage-feedback system.

The hybrid model shown in Figure 9 describes the AC behavior of a noncompensated wide-band differential op amp. The open-loop frequency response, which is illustrated in Figure 10 for various R_{OG} values, is determined by two time constants. The elements R and C_{OTA} between the current source output and the output buffer form the first open-loop pole T_C . The signal delay time, T_D , modelled in the output buffer, combines several small phase-shifting time constants and delay times. They are distributed throughout the amplifier and are also present in the feedback loop. As shown in Figure 10, an increasing R_{OG} leads to a decreasing open-loop gain. The ratio of the two time constants, T_C and T_D , of the open-loop frequency response also determines the product $G_{OL} \cdot G_{CL}$ for optimal closed-loop frequency response.

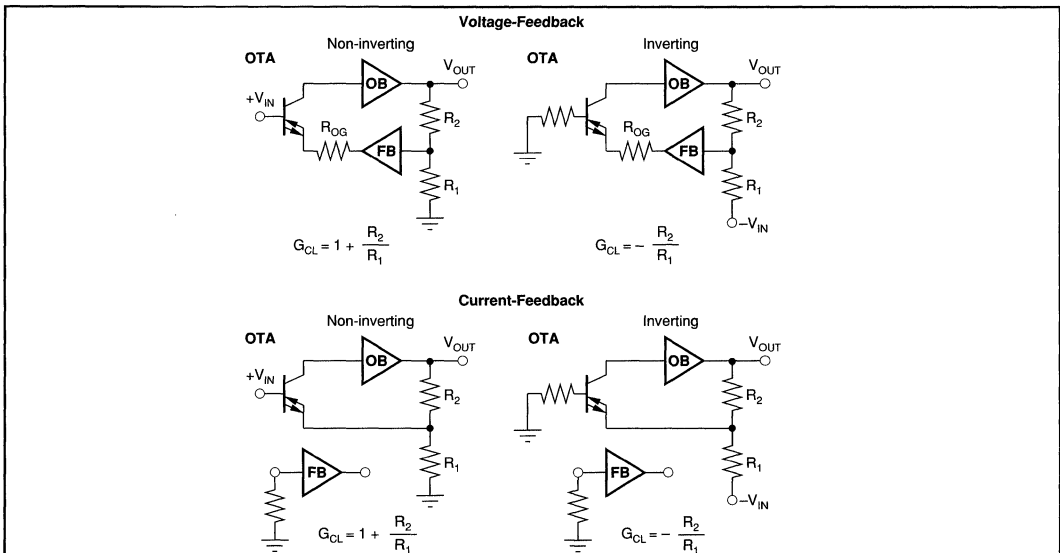


FIGURE 6. Op Amp Configurations OPA622.

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$$G_{OL} = G_{CL} \cdot \frac{T_C}{2T_D}$$

T_C and T_D are fixed by the op amp design. The purpose of R_{OG} now is to vary G_{OL} versus G_{CL} to keep the product $G_{OL} \cdot G_{CL}$ constant, which is the theoretical condition for optimal and gain-independent frequency response. Figure 11 summarizes some optimal flat closed-loop responses and indicates the R_{OG} values. It should be noted that the bandwidth remains relatively constant and R_{OG} has its highest value (low open-loop gain) at low closed-loop gains (low open-loop gain) at low closed-loop gains. Harmonic distortion is also improved with increased open-loop gain. Figure 12 shows the OPA622 frequency response at $G_{CL} = +2V/V$ and variable R_{OG} to demonstrate its influence on a flat frequency response. Versus various load capacitors, a slight variation of R_{OG} might be necessary. However, the external adjustment of the open-loop gain using R_{OG} allows adaption to different load capacitances. It is possible to achieve optimal pulse response over a wide range of load capacitances without overshooting and ringing. As an example, Figure 13 shows a selection curve for the optimal R_{OG} value versus the load capacitance at a gain (G_{CL0}) of $+2V/V$.

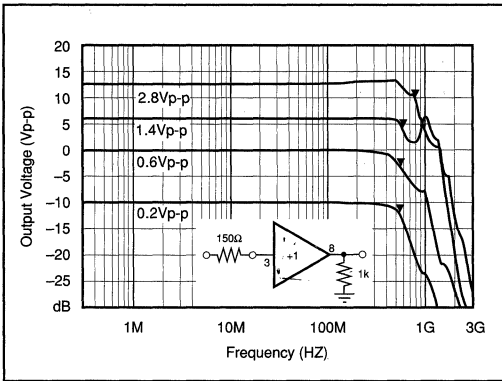


FIGURE 7. Bandwidth vs Output Voltage (Buffer Amplifier).

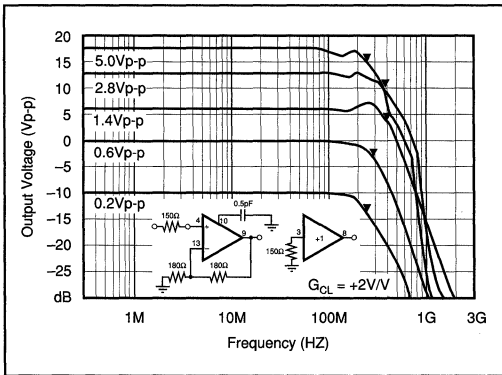


FIGURE 8. Bandwidth vs Output Voltage (Current-Feedback Amplifier).

Thermal Considerations

The OPA622 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise, resulting in cooler, more reliable operation. At extreme temperatures and under full load conditions, a heat sink is necessary. The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$ (P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load). Although the P_{DQ} is very low (50mW at $V_{CC} = \pm 5V$), care should be taken when a signal is applied. For high-speed op amps, a more precise approach to determine power consumption is to measure the average total quiescent current for several typical load conditions. The power consumption of the OPA622 is influenced by the kind of signal and frequency, the output voltage and load resistor, and the repetition rate of the signal transitions. Figure 14 shows the total average supply current versus the frequency of an applied sine wave for various output voltages. Figure 15 illustrates the total quiescent current versus the repetition frequency of an applied square wave signal.

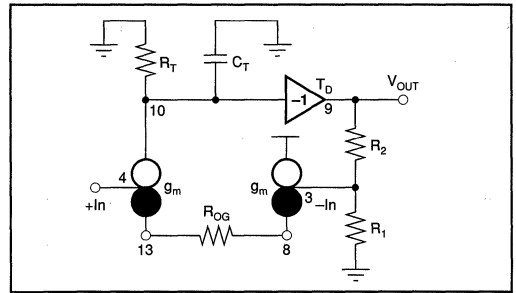


FIGURE 9. Hybrid Model of a Wideband Op Amp.

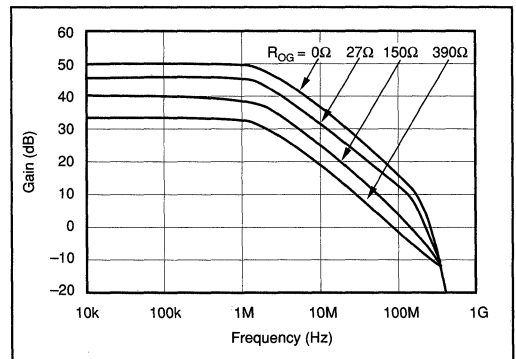


FIGURE 10. Open-Loop Gain vs R_{OG} .

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the OPA622 to speed prototyping. This board allows fast and easy performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The complete AC characterization was performed with the same type. Figure 16 shows the schematic and Figure 17 the silk screen and double-sided layout. Request DEM-OPA622-1GC to test the operational amplifier in the 14-pin DIP.

CIRCUIT LAYOUT

The high-frequency performance of the operational amplifier OPA622 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute musts. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

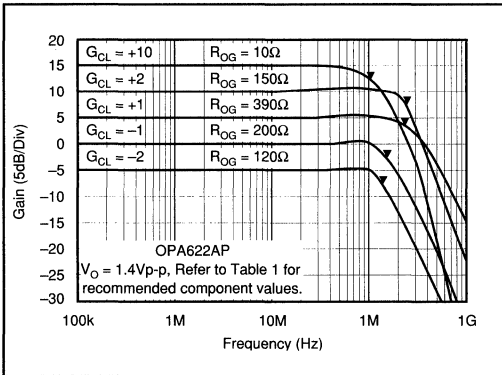


FIGURE 11. Optimum Response vs Closed-Loop Gains.

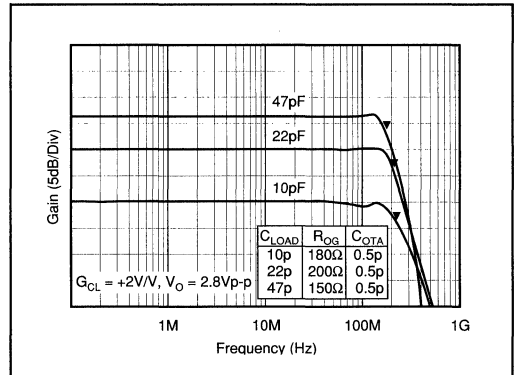


FIGURE 13. Bandwidth vs C_{LOAD} .

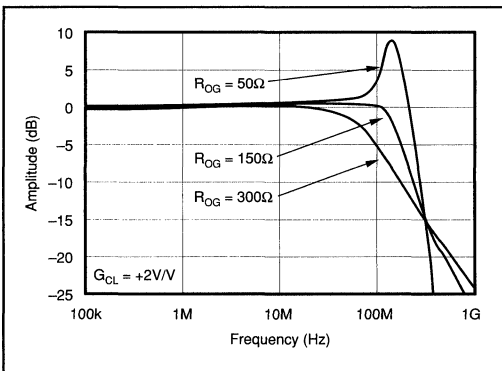


FIGURE 12. Closed-Loop Gain vs R_{OG} .

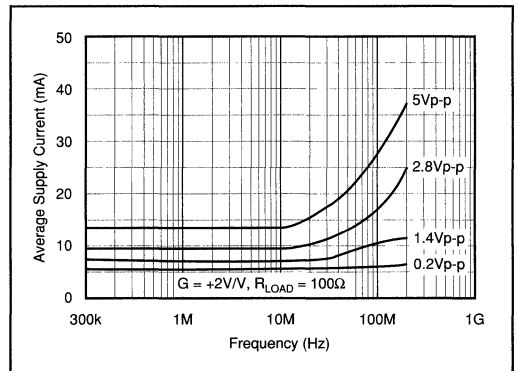


FIGURE 14. Average Supply Current vs Frequency (Sine Wave).

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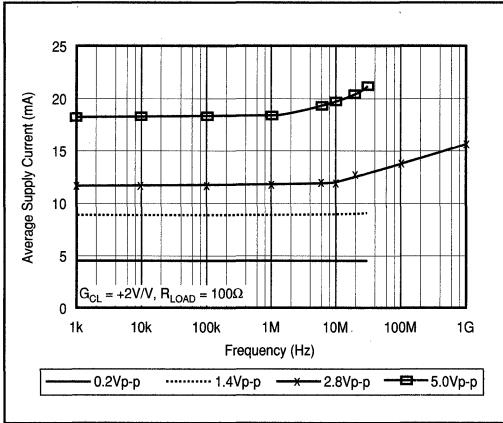


FIGURE 15. Average Supply Current vs Frequency (Square Wave).

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2 μ F) and a parallel 470pF ceramic chip capacitor. Surface-mount types are recommended because of their low lead inductance.
- PC board traces for power lines should be wide to reduce impedance or inductance.
- Make short, low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout.
- Place the R_{OG} resistor as close as possible to the package and use the shortest possible trace length.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input and R_{OG} terminals.

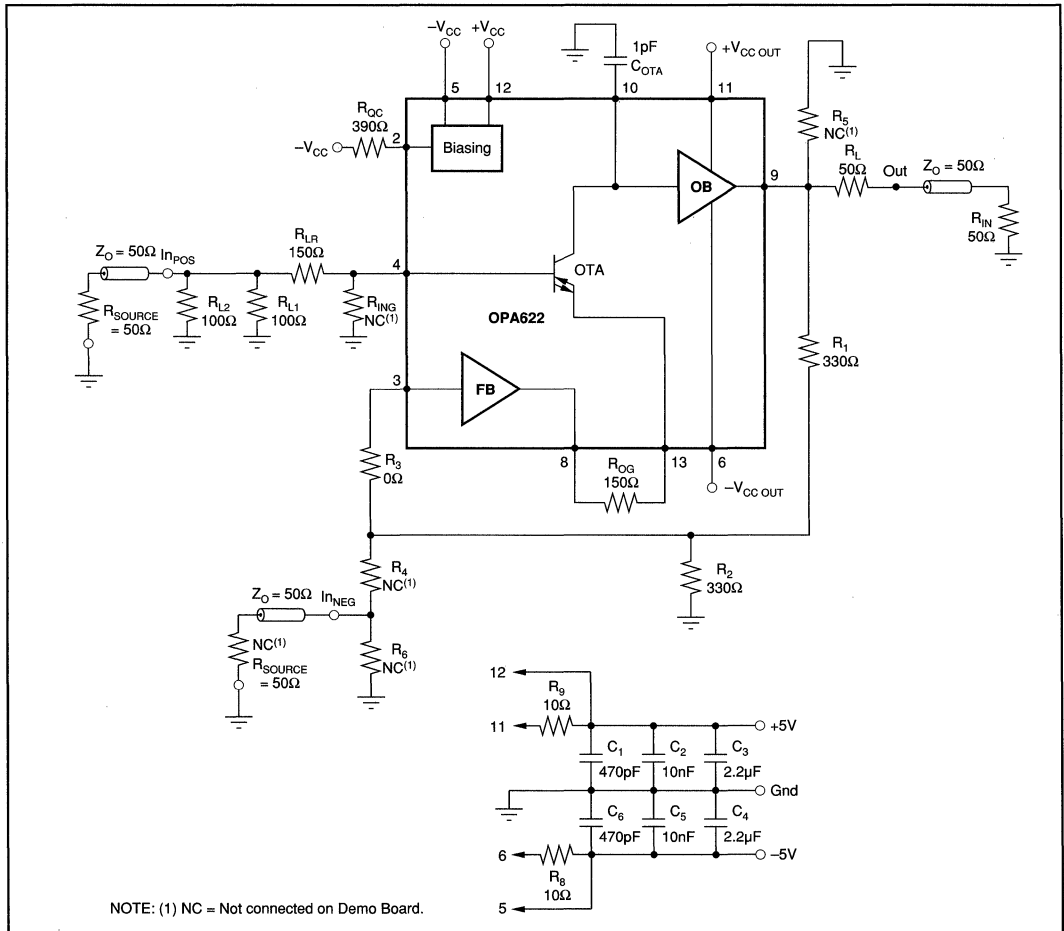


FIGURE 16. Circuit Schematic DEM-OPA622-1GC.

- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance, surface-mounted components. Circuits using all surface-mount components with the OPA622AU will offer the best AC performance.
- A resistor (50Ω to 330Ω) in series with the high-impedance inputs is strictly recommended for stable operation.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential here—there are not shortcuts.

RECOMMENDED COMPONENTS VALUES

For the most common gains Table I summarizes recommended component values for optimum flat frequency re-

sponses. The recommended values were taken applying a 100Ω load resistance and a 2pF load capacitance to the output. They may change when applying different load conditions especially with high load capacitances. According to the behavior shown in Figure 12 the frequency response will show a peaking when the R_{OG} is decreased and will slope down when R_{OG} is increased. The C_{OTA} capacitor is responsible for the first open-loop pole and a small external capacitor for the gains +1V/V and +2V/V is required for stable operation. The package pins, the internal lead frame, and band wires form a resonant circuit. The use of a resistor in the range of 150Ω to 390Ω is strictly recommended in series to all high impedance inputs to damp the package related resonant circuit. Also the feedback resistor R1 is in series to the inverting high impedance inputs and therefore a component value equal or higher than 330Ω for the DIL

OPA622AP								OPA622AU							
$I_o = 5mA$								$R_{OC} = 430\Omega$							
G_{CL}	+1	+2	+5	+10	-1	-2	UNITS	G_{CL}	+1	+2	+5	+10	-1	-2	UNITS
R_1	0	330	620	1600	390	470	Ω	R_1	150	240	470	820	240	300	Ω
R_2	—	330	160	180	—	—	Ω	R_2	—	240	120	91	—	—	Ω
R_3	220	0	0	0	0	0	Ω	R_3	0	0	0	0	0	0	Ω
R_{OG}	330	150	56	10	200	150	Ω	R_{OG}	270	150	47	10	160	100	Ω
C_{OTA}	2.2	1	—	—	1	1	pF	C_{OTA}	2.2	1	—	—	1	1	pF
R_{ILR}	150	150	150	150	150	150	Ω	R_{ILR}	200	150	200	200	150	150	Ω
R_4	—	—	—	—	390	240	Ω	R_4	—	—	—	—	240	150	Ω
R_5	—	—	—	—	62	62	Ω	R_5	—	—	—	—	68	68	Ω
Ring	—	—	—	—	150	150	Ω	Ring	—	—	—	—	150	150	Ω
Bandwidth								Bandwidth							
$V_{OUT} = 0.2Vp-p$	170	160	140	110	135	125	MHz	$V_{OUT} = 0.2Vp-p$	200	170	160	100	180	175	MHz
$V_{OUT} = 2.8Vp-p$	220	200	170	110	150	150	MHz	$V_{OUT} = 2.3Vp-p$	250	240	230	100	250	240	MHz

TABLE I. Recommended Components Values for Optimum Frequency Performance.

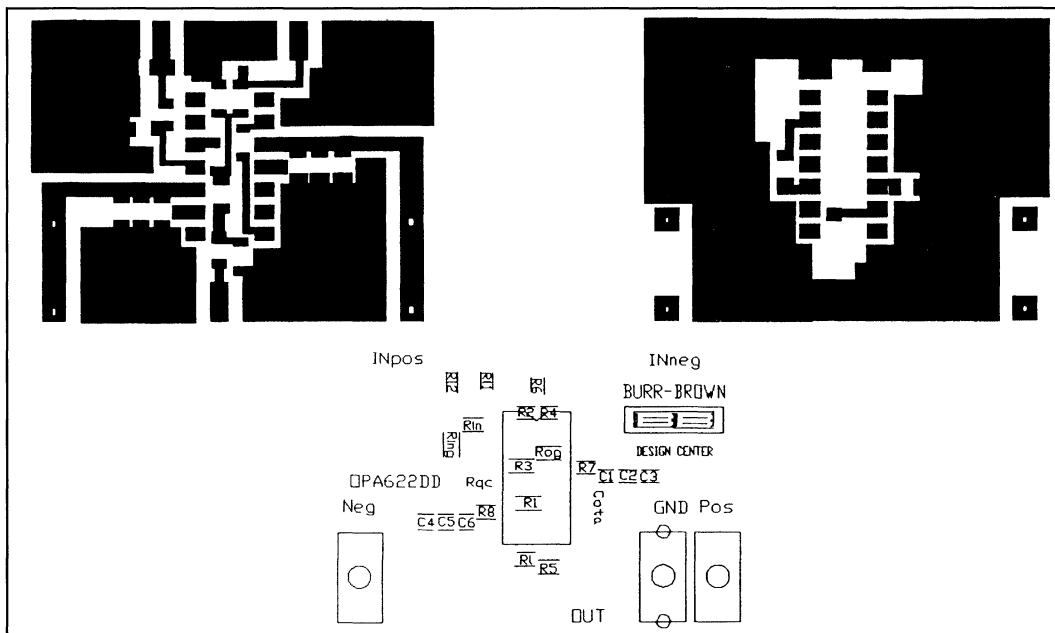


FIGURE 17. Silkscreen and Board Layouts for DEM-OPA622-1GC.

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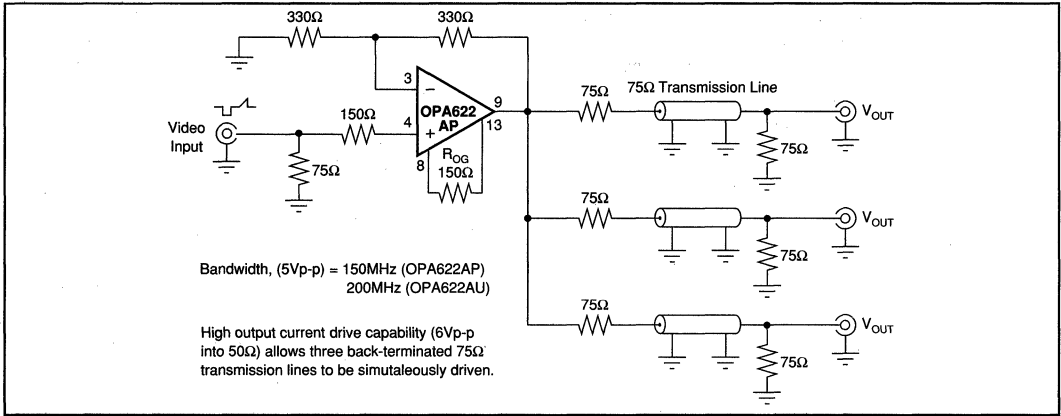


FIGURE 18. Video Distribution Amplifier.

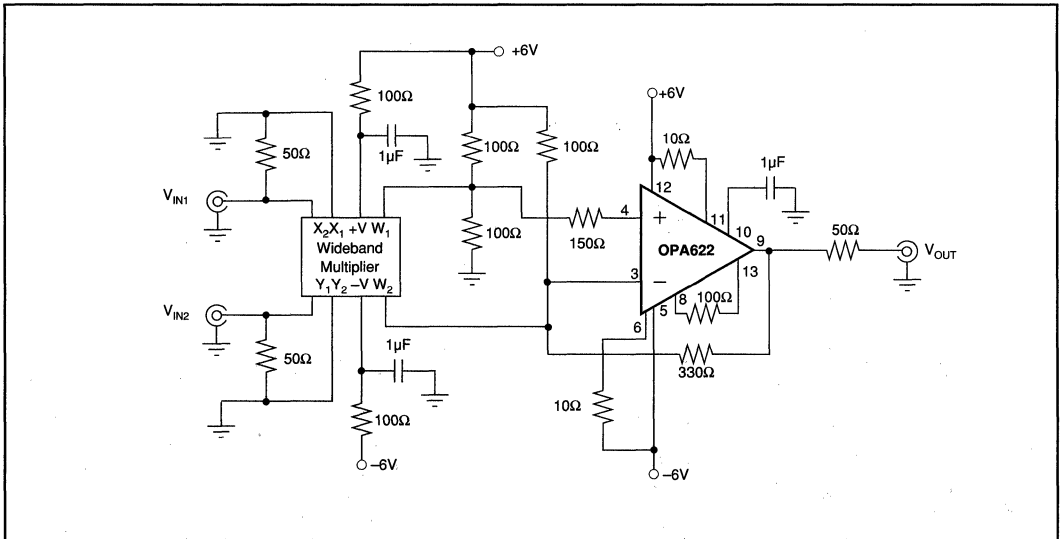


FIGURE 19. Wideband Multiplier Output Amplifier

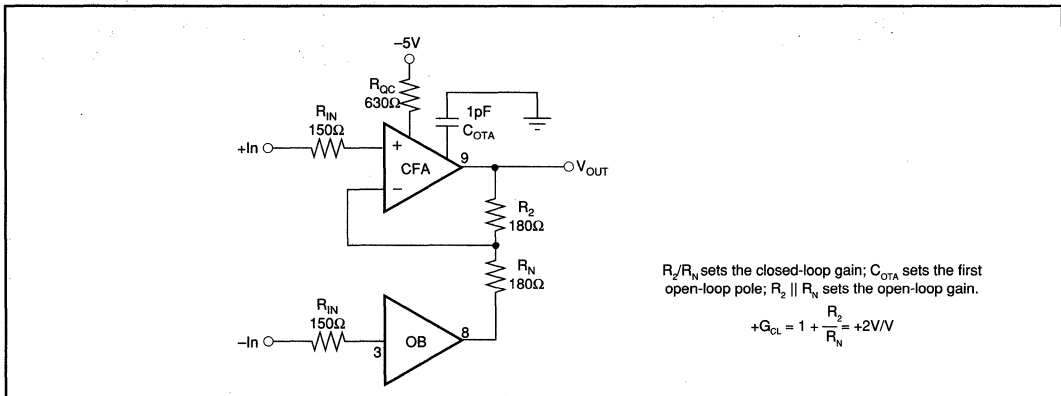
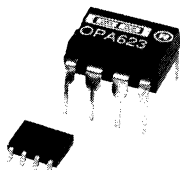


FIGURE 20. Current-Feedback Amplifier with Two Equal and High Impedance Inputs.



OPA623

OPA623

2

OPERATIONAL AMPLIFIERS

Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

FEATURES

- **BANDWIDTH:** 350MHz, 2.8Vp-p
- **HIGH OUTPUT CURRENT:** $\pm 70\text{mA}$
- **SLEW RATE:** 2100V/ μs , 5Vp-p
- **DIFFERENTIAL GAIN/PHASE:** 0.12%/0.05°
- **LOW QUIESCENT CURRENT:** $\pm 4\text{mA}$
- **LOW INPUT BIAS CURRENT:** 1.2 μA
- **RISE TIME:** 1.9ns, 5Vp-p
- **SETTLING TIME:** 9ns, 0.1%

APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- HIGH-SPEED DIGITAL COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- LINE DRIVING (50 Ω , 75 Ω)
- DISTRIBUTION AMP
- CRT OUTPUT STAGE DRIVER
- ACTIVE FILTER

DESCRIPTION

The OPA623 is a current-feedback operational amplifier designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment.

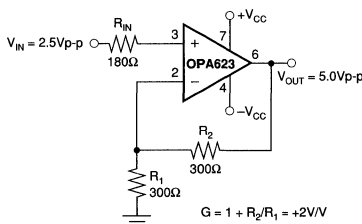
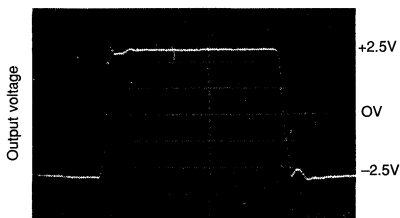
The new circuit design, together with the complementary bipolar process, achieves performance previously unattainable in monolithic integrated circuit technology.

The current-feedback op amp is optimized for wide bandwidth, excellent pulse response, gain flatness, low distortion, and operation at a low quiescent current of $\pm 4\text{mA}$.

It provides a 350MHz large-signal bandwidth at 2.8Vp-p output voltage, as well as a 2100V/ μs slew rate. The gain flatness of 0.05dB over a 30MHz bandwidth makes it suitable for HDTV designs. Another feature of the op amp is its high output current of $\pm 70\text{mA}$, enabling it to drive two back-terminated 75 Ω cables when using the amplifier as a line driver in video routers, distribution amplifiers, and analog and digital communications equipment.

The OPA623 operates from a $\pm 5\text{V}$ supply, is specified for the extended industrial temperature range (-40°C to $+85^\circ\text{C}$), and is available in 8-pin plastic SOIC and 8-pin plastic DIP.

LARGE SIGNAL PULSE RESPONSE



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SPECIFICATIONS

DC-SPECIFICATION

At $V_{CC} = \pm 5\text{VDC}$, $I_O = \pm 4\text{mA}$, $R_L = 100\Omega$, $R_{IN} = 210\Omega$, and $T_{AMB} = +25^\circ\text{C}$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP/AU			UNITS
		MIN	TYP	MAX	
INPUT OFFSET VOLTAGE Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking)	$V_{CC} = \pm 4.5\text{V to } \pm 5.5\text{V}$ $V_{CC} = +4.5\text{V to } +5.5\text{V}$ $V_{CC} = -4.5\text{V to } -5.5\text{V}$	45	-8	± 25	mV
			125		$\mu\text{V}/^\circ\text{C}$
			50		dB
			47		dB
			39		dB
+INPUT BIAS CURRENT Initial vs Temperature			-1.2	± 4	μA
			7		$\text{nA}/^\circ\text{C}$
-INPUT BIAS CURRENT Initial vs Temperature			+4.5	± 20	μA
			340		$\text{nA}/^\circ\text{C}$
INPUT IMPEDANCE +Input			2.74 1		M Ω pF
INPUT NOISE Voltage Noise Density Signal-to-Noise Ratio	$f = 100\text{kHz to } 100\text{MHz}$ $S/N = 0.7/(V_n \cdot \sqrt{5\text{MHz}})$		10		$\text{nV}/\sqrt{\text{Hz}}$
			89		dB
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection			± 3	± 3.2	V
			43	50	dB
RATED OUTPUT Voltage Output Output Current Closed-Loop Output Impedance	$R_L = 100\Omega$ Gain = +2		± 3	± 3.1	V
				± 70	mA
				0.12 1.5	Ω pF
POWER SUPPLY Rated Voltage Derated Performance Quiescent Current Rejection Ratio	$I_O = 0\text{mA}$		± 4.5	± 5.5	VDC
			± 4	± 6	VDC
			± 3.5	± 4.5	mA
			45	50	dB

ELECTRICAL (FULL TEMPERATURE RANGE, -40°C to $+85^\circ\text{C}$)

At $V_{CC} = \pm 5\text{VDC}$, $I_O = \pm 4\text{mA}$, $R_L = 100\Omega$, and $R_{IN} = 210\Omega$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU			UNITS
		MIN	TYP	MAX	
INPUT OFFSET VOLTAGE				± 30	mV
BIAS CURRENT +Input			-1.5	± 5	μA
BIAS CURRENT -Input			27	± 50	μA
RATED OUTPUT Voltage Output	$R_L = 100\Omega$		± 3	± 3.1	V
POWER SUPPLY Quiescent Current	$I_O = 0\text{mA}$		± 2	± 4	mA

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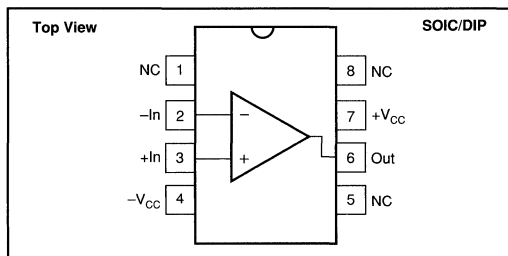
SPECIFICATIONS

AC-SPECIFICATION

At $V_{CC} = \pm 5VDC$, $I_O = \pm 4mA$, $R_L = 100\Omega$, $R_N = 210\Omega$, and $T_{AMB} = +25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP/AU			UNITS
		MIN	TYP	MAX	
FREQUENCY DOMAIN					
Large Signal Closed-Loop Bandwidth (-3dB)	$V_O = 2.8Vp-p$, Gain = +1V/V		340		MHz
	$V_O = 2.8Vp-p$, Gain = +2V/V		350		MHz
	$V_O = 2.8Vp-p$, Gain = +5V/V		260		MHz
	$V_O = 2.8Vp-p$, Gain = +10V/V		210		MHz
	$V_O = 2.8Vp-p$, Gain = -1V/V		360		MHz
	$V_O = 2.8Vp-p$, Gain = -2V/V		330		MHz
	$V_O = 5.0Vp-p$, Gain = +2V/V		240		MHz
SMALL SIGNAL BANDWIDTH	$V_O = 0.2Vp-p$, Gain = +2V/V		290		MHz
GROUP DELAY TIME	Pin 3 to Pin 6, Gain = +2V/V		1.2		ns
DIFFERENTIAL GAIN	$G = +2V/V$, $f = 4.43MHz$, $R_L = 150\Omega$ $V_O = +1.4V$		0.12		%
DIFFERENTIAL PHASE	$G = +2V/V$, $f = 4.43MHz$, $R_L = 150\Omega$ $V_O = +1.4V$		0.05		Degrees
HARMONIC DISTORTION	Gain = +2V/V				
	Second Harmonic $f = 10MHz$, $V_O = 2.0Vp-p$		-56		dBc
	Third Harmonic		-59		dBc
	Second Harmonic $f = 30MHz$, $V_O = 2.0Vp-p$		-30		dBc
	Third Harmonic		-37		dBc
	Second Harmonic $f = 50MHz$, $V_O = 2.0Vp-p$		-30		dBc
Third Harmonic		-33		dBc	
GAIN FLATNESS PEAKING	Gain = +2V/V				
	$V_O = 2.0Vp-p$, DC to 30MHz $V_O = 2.0Vp-p$, DC to 100MHz		0.05 0.20		dB dB
TIME DOMAIN					
Rise Time	Gain = +2V/V, 10% to 90% $V_O = 2.0Vp-p$ $V_O = 5.0Vp-p$		1.4 1.9		ns ns
Fall Time	Gain = +2V/V, 10% to 90% $V_O = 2.0Vp-p$ $V_O = 5.0Vp-p$		1.4 2.6		ns ns
SLEW RATE	Gain = +2V/V, Rise Time = 1ns $V_O = 0.2Vp-p$ $V_O = 5.0Vp-p$		140 2100		V/ μs V/ μs
SETTLING TIME	Gain = +2V/V, Rise Time = 2ns $V_O = 2V_{pp}$, 0.1%		9		ns

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA623AP	Plastic DIP	006
OPA623AU	Plastic SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA623AP	8-Pin Plastic DIP	-40°C to +85°C
OPA623AU	8-Pin SOIC	-40°C to +85°C

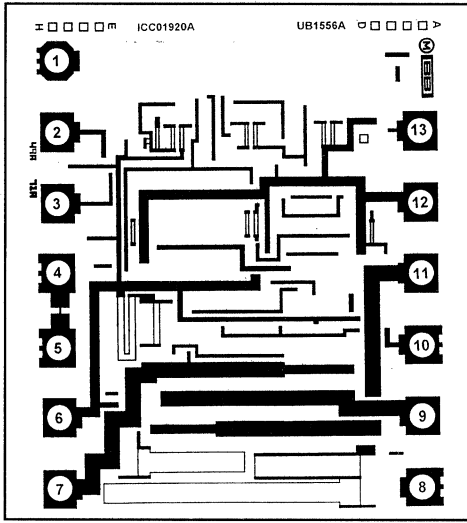
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage ⁽¹⁾	± $V_{CC} \pm 0.7V$
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to ± V_{CC} .



DICE INFORMATION



OPA623 DIE TOPOGRAPHY

PAD	FUNCTION
1	NC
2	Inverting Input
3	Non-Inverting Input
4	NC
5	NC
6	-5V Supply
7	-5V Supply, Output
8	NC
9	Output
10	OTA Output
11	+5V Supply, Output
12	+5V Supply
13	NC

Substrate Bias: Negative Supply

NC: No Connection

Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	57 x 69 ±5	1.44 x 1.76 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02 +0.05, -0.0	0.0005 +0.0013, -0.0
Gold	0.30 ±0.05	0.0076 ±0.0013

INPUT PROTECTION

The need for protection from static damage has long been recognized for MOSFET devices, but all semiconductor devices deserve protection from this potentially damaging source. The OPA623 incorporates on-chip ESD protection diodes as shown in Figure 1. These diodes eliminate the need for external protection diodes, which can add capacitance and degrade AC performance.

As shown, all input pins of the OPA623 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur when the amplifier loses its power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, the diode current should be limited externally to approximately 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the amplifier input characteristics without necessarily destroying the device. In precision amplifiers, such changes may degrade offset and drift noticeably. For this reason, static protection is strongly recommended when handling the OPA623.

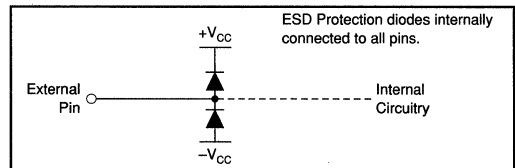
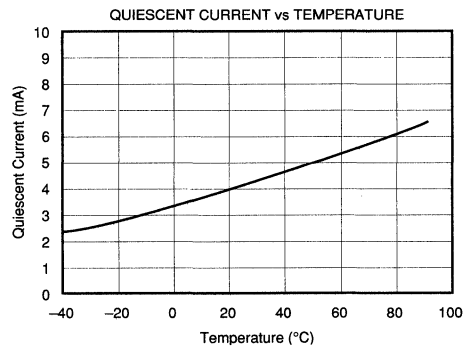
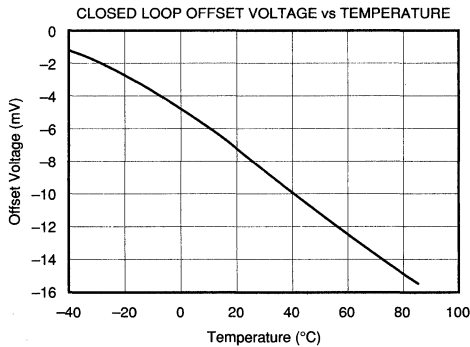
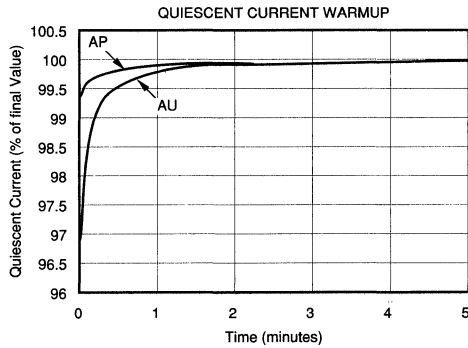
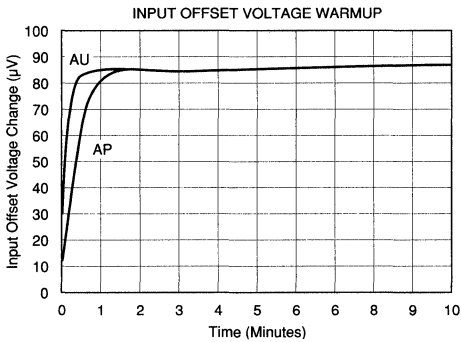
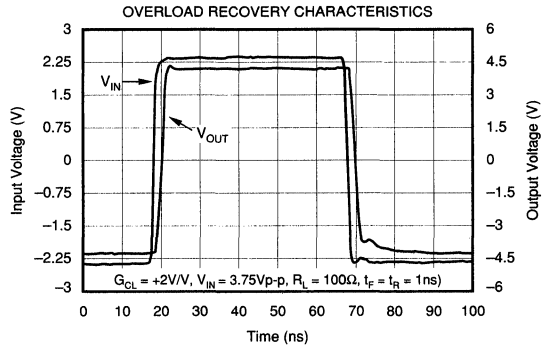
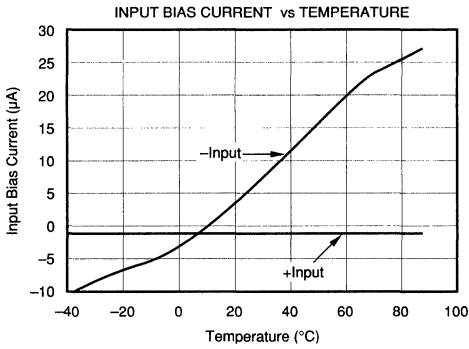


FIGURE 1. Internal ESD Protection.

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TYPICAL PERFORMANCE CURVES

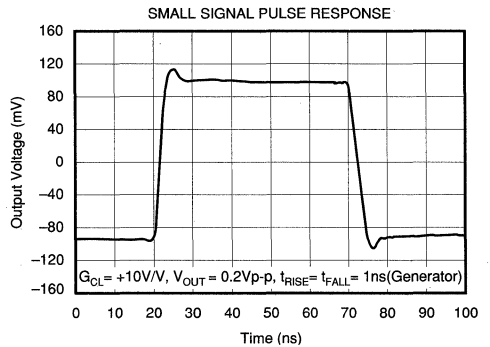
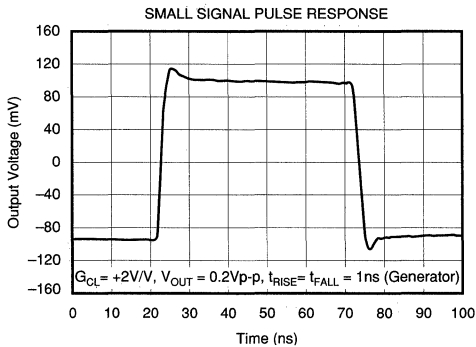
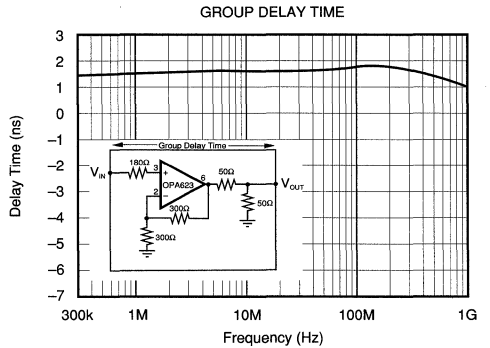
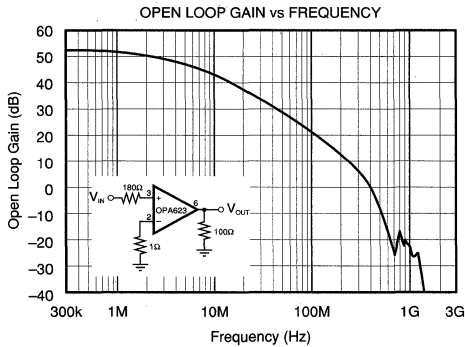
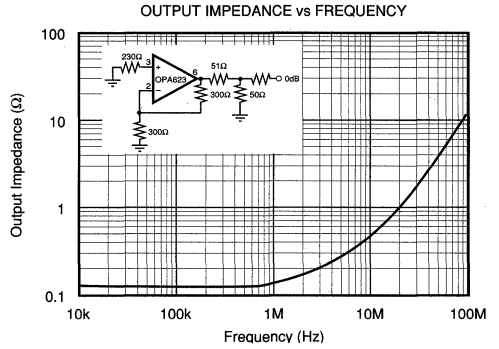
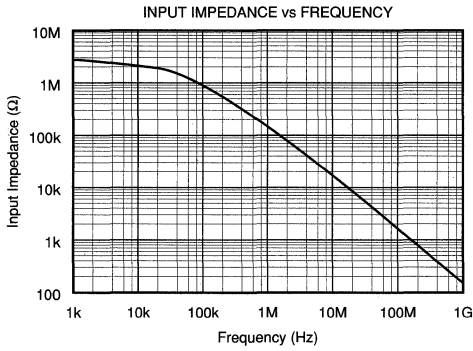
At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, $I_Q = \pm 4mA$, $R_{IN} = 150\Omega$, $T_{AMB} = +25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, $I_Q = \pm 4mA$, $R_{IN} = 150\Omega$, $T_{AMB} = +25^\circ C$ unless otherwise noted.

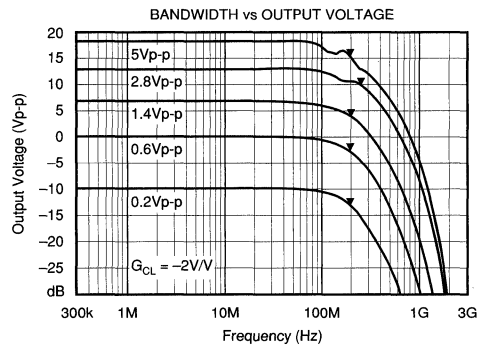
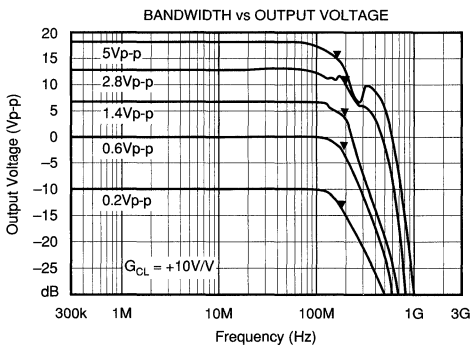
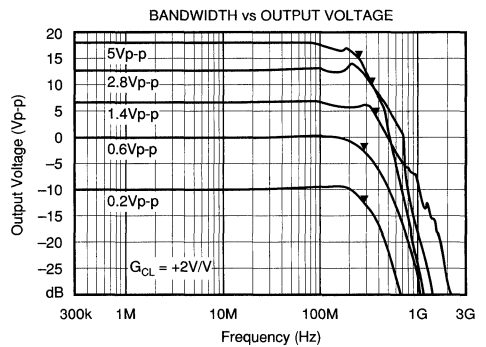
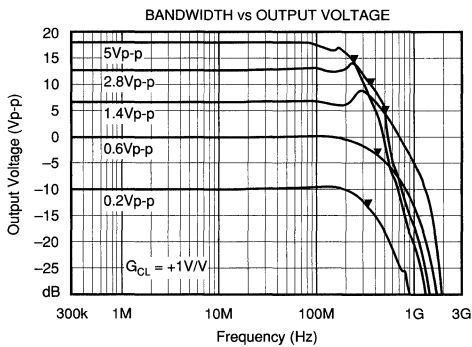
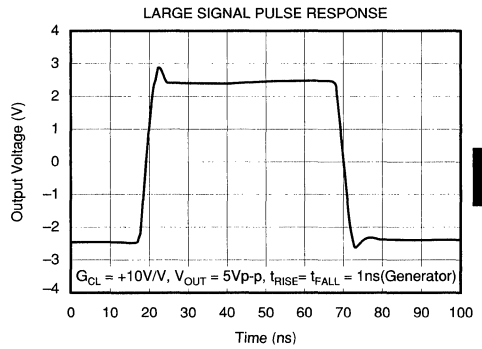
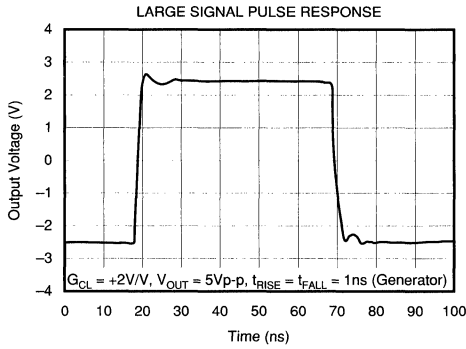


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TYPICAL PERFORMANCE CURVES (CONT)

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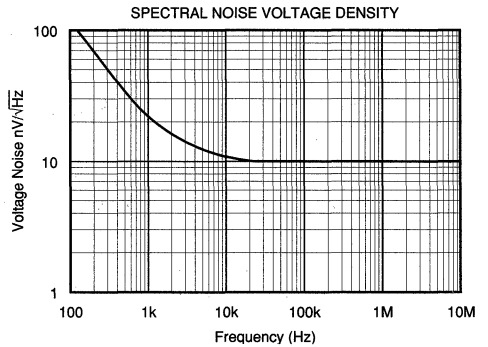
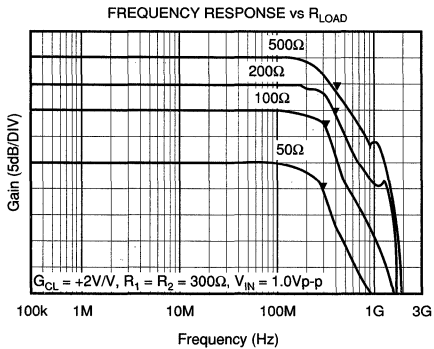
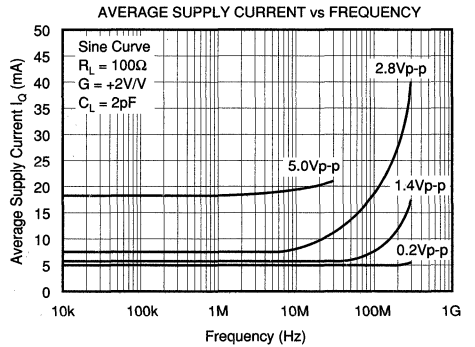
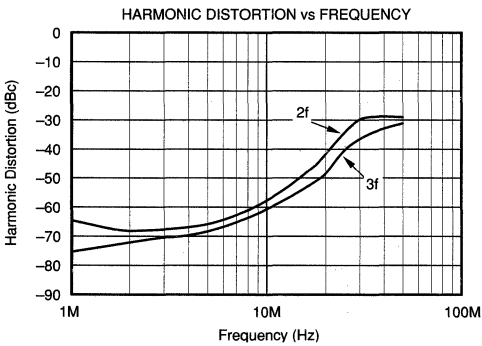
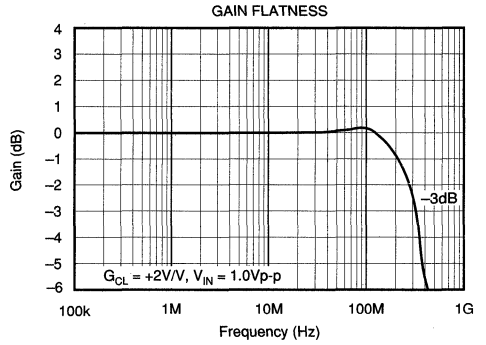
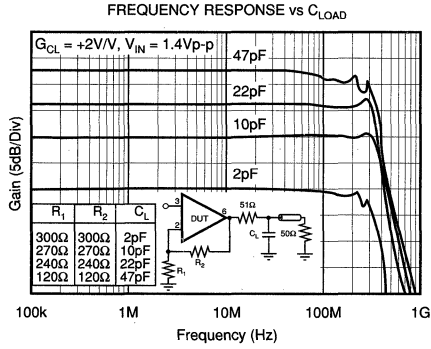
OPA623
2
OPERATIONAL AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$, $I_O = \pm 4mA$, $R_{IN} = 150\Omega$, $T_{AMB} = +25^\circ C$ unless otherwise noted.



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DISCUSSION OF PERFORMANCE

Requiring very low quiescent power, the OPA623 achieves its exceptional AC performance by using the current-feedback topology. This wide-band monolithic operational amplifier is designed for gain applications of up to 20V/V, where power and cost are of primary concern.

Operating from a $\pm 5V$ supply, the OPA623 consumes only 40mW, yet maintains a 350MHz large-signal bandwidth at $V_{OUT} = 2.8V_{p-p}$ and a 2100V/ μs slew rate. Benefiting from the current-feedback architecture, the OPA623 offers stable operation with no compensation capacitor, even at unity gain.

With its low differential gain and phase errors of typically 0.12% and 0.05° at 4.43MHz, the OPA623 meets the performance and cost requirements of high-volume broadcast and HDTV applications.

The OPA623's large-signal bandwidth, high slew rate, excellent pulse response, and high drive capabilities are features well-suited to wide-band RGB video applications, RF instruments, and even high-speed digital communication systems.

For most circuit configurations, the OPA623 current-feedback op amp can be treated like a conventional op amp. As with a voltage-feedback op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response. Feedback resistor values can be selected to provide nearly constant closed-loop bandwidth over a wide range of gains and flat gain adjustment vs frequency.

DESCRIPTION

A wide-band operational transconductance amplifier (OTA) and an output buffer are the main blocks of a current-feedback op amp. The simplified circuit diagram is illustrated in Figure 2. The OTA consists of a complementary unity-gain amplifier and a subsequent current mirror. The input buffer is connected across the inputs of the op amp. The voltage at the high-impedance +In terminal is transferred to the -In terminal at a low impedance. The current mirrors reflect any current flowing into or out of the +In terminal by a fixed ratio to the high-impedance OTA output, which is directly connected to the complementary output buffer. It is designed to drive low-impedance transmission

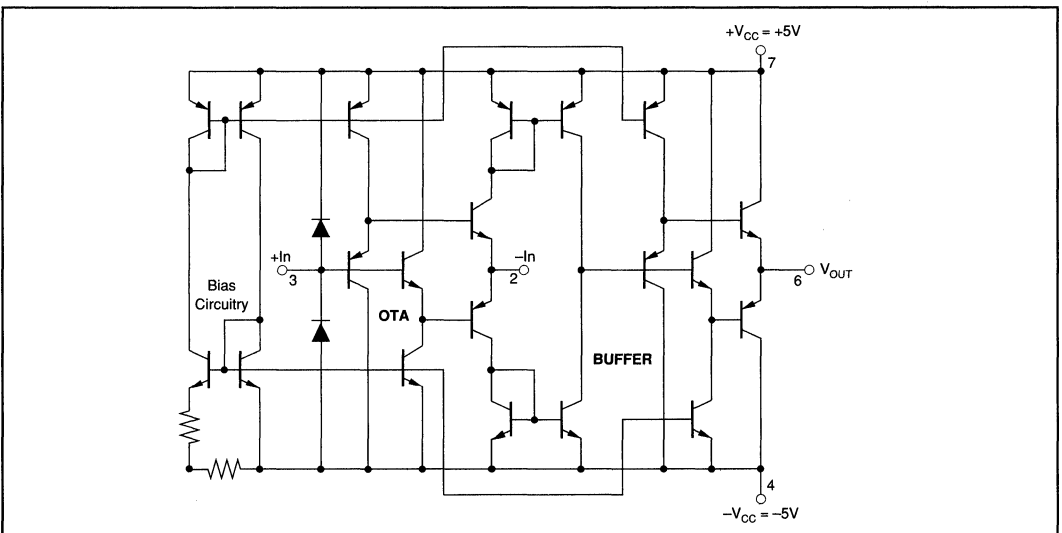


FIGURE 2. Simplified Circuit Diagram.

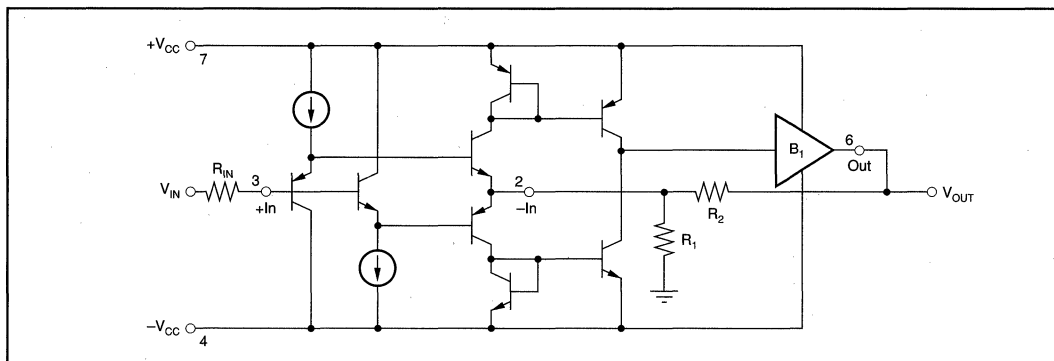


FIGURE 3. Non-Inverting Current-Feedback Op Amp Configuration.

lines or loads. The buffer output is not current-limited or protected.

As can be seen in Figure 3, the feedback in the form of a current is applied through R_2 to the low-impedance inverting input, and the size of $R_2 \parallel R_1$ determines the open-loop gain of the op amp.

The hybrid model shown in Figure 4 describes the AC behavior of a wide-band current-feedback op amp that is not internally compensated. The open-loop frequency response, which is illustrated in Figure 5 for various R_2 values, is determined by two time constants. The elements R and C between the current source output and the output buffer form the dominant open-loop pole T_C . The signal delay time T_D modelled in the output buffer combines several small phase-shifting time constants and delay times. They are distributed throughout the amplifiers and are also present in the feedback loop. As shown in Figure 5, increasing $R_2 \parallel R_1$ leads to a decreasing open-loop gain. The ratio of the two time

$$G_{OL} = G_{CL} \cdot \frac{T_C}{2T_D}$$

constants T_C and T_D also determines the product $G_{OL} \cdot G_{CL}$ for optimal closed-loop frequency response:

The two time constants T_C and T_D , however, are fixed by the op amp design. But varying $R_2 \parallel R_1$ externally in the feedback loop allows for variation of the open-loop gain G_{OL} versus the closed-loop gain G_{CL} . This keeps the product $G_{OL} \cdot G_{CL}$ constant, which is the theoretical condition for optimally flat frequency response.

This variation may be beneficial when driving high capacitive loads. Setting the open-loop gain externally also allows the circuit to be optimized to a wide range of capacitive loads, as shown in Figure 7 for a closed-loop gain of $+2V/V$ and a capacitive load of up to 47pF.

It should be noted here that higher open-loop gain (resulting from lower feedback resistors) also yields lower distortion.

With external control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to individual application requirements, and the open-loop gain selection

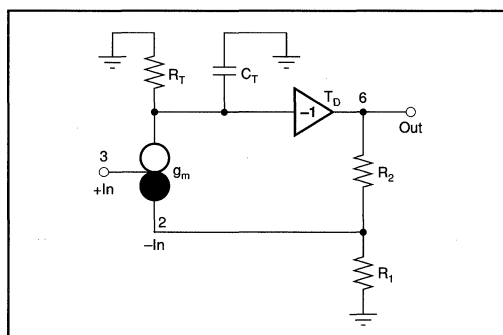


FIGURE 4. Hybrid Model OPA623.

provides a nearly constant closed-loop bandwidth, as shown in Figure 6 for various gains with an optimal flat frequency response. This behavior stands in contrast to op amps that are internally compensated for stable unity-gain operation, where the bandwidth is inversely proportional to the closed-loop gain, sharply limiting the bandwidth and slew rate at high output levels and gains.

In general, lower feedback resistors produce wider bandwidth, more frequency response peaking, and more pulse response overshooting. Higher feedback resistors results in an overdamped response with little or no peaking and overshooting.

Component pin and layout capacitances together with trace and wire board inductances from a resonant IC circuit can lead to oscillations of several hundreds of MHz. This very high frequency oscillation leads to an excessive increase in supply current which can destroy the device.

A resistor (100Ω to 250Ω) in series and close to the high-impedance, non-inverting input damps the LC circuit and generates a safe operation.

THERMAL CONSIDERATIONS

The OPA623 does not require a heat sink for operation in most environments. The use of a heat sink, however, will

reduce the internal thermal rise, resulting in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, (P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load). Although the P_{DQ} is very low (40mW at $V_{CC} = \pm 5V$), care should be taken when a signal is applied. For high-speed op amps, a more precise approach to determine power consumption is to measure the average total quiescent current for several typical load conditions. The power consumption of the OPA623 is influenced by the kind of signal, the applied signal frequency, the output voltage, load resistor, and the repetition rate of the signal transitions. Figure 8 shows the average supply current versus the frequency of an applied sine wave for various output voltages. Figure 9 illustrates the average supply current versus the repetition frequency of an applied square wave signal.

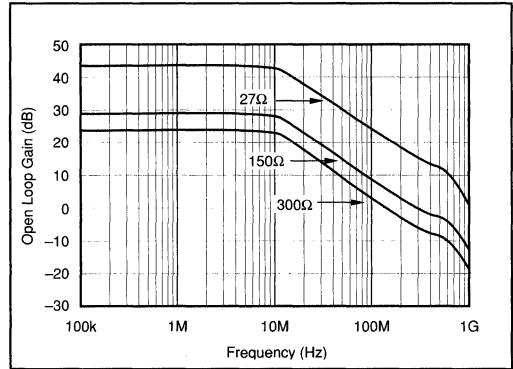


FIGURE 5. Open Loop Gain vs $R_2 \parallel R_1$.

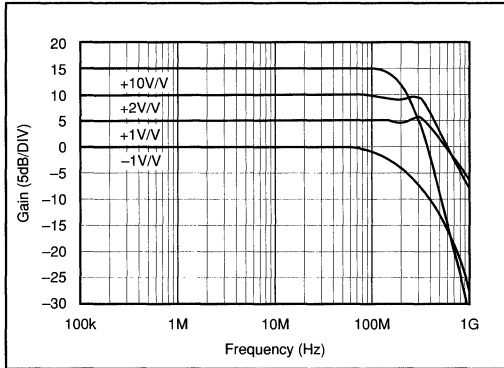


FIGURE 6. Optimum Frequency Response vs Closed-Loop Gain.

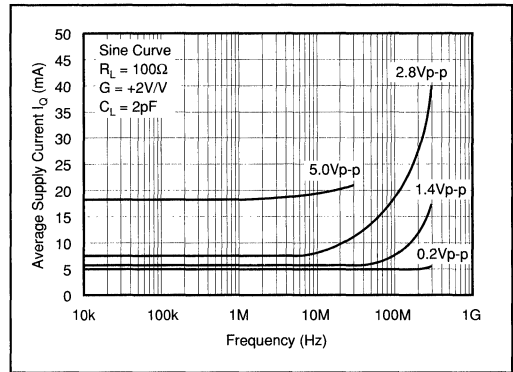


FIGURE 8. Average Supply Current vs Frequency (sine wave).

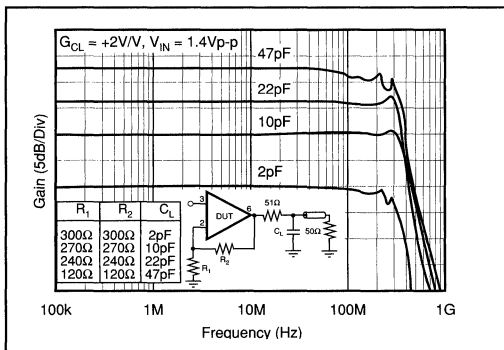


FIGURE 7. Frequency Response vs C_{LOAD} .

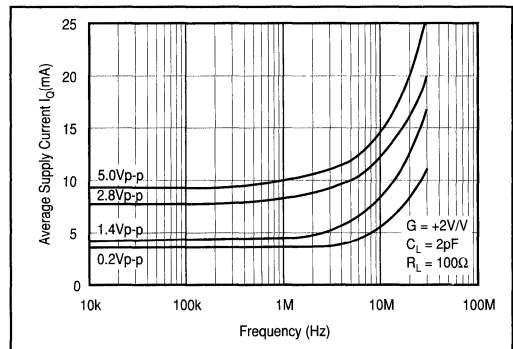


FIGURE 9. Average Supply Current vs Frequency (square wave).

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CIRCUIT LAYOUT

The high-frequency performance of the operational amplifier OPA623 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- A resistor (100Ω to 250Ω) in series and close to the high-impedance, noninverting input is necessary to reduce peaking; this resistor prevents any very high-frequency oscillations at the op amp input, which can lead to an excessive increase in quiescent current.
- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2μF) with a parallel 470pF ceramic chip capacitor. Surface-mount types are recommended because of their low lead inductance. Although the OPA623 operates at a low quiescent current, high charging and discharging currents flow during steep transitions.
- PC board traces for power lines should be wide to reduce impedance and inductance.
- Make short low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout, however, do not extend the ground plane under high-impedance nodes such as the amplifier's input terminals, which are sensitive to stray capacitances.

- Sockets are not recommended because they add significant inductance and parasitic capacitance.
- Use low-inductance, surface-mounted components. Circuits using all surface-mount components with the OPA623AU will offer the best AC performance.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Make the feedback trace as short as possible. The inverting input is sensitive to stray capacitances that lead to peaking in the frequency response. A stray capacitance at the inverting input increases the gain at high frequencies.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the OPA623 DIP package in a +2V/V configuration to speed prototyping. This board allows fast and easy performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. For the most common gains Table 1 summarizes recommended component values for optimum flat frequency response. The complete AC characterization was performed with this board. Figure 10 shows the schematic and Figure 11 the silk screen and double-sided layout. Request DEM-OPA623-1GC to test the operational amplifier in the 8-pin DIP package.

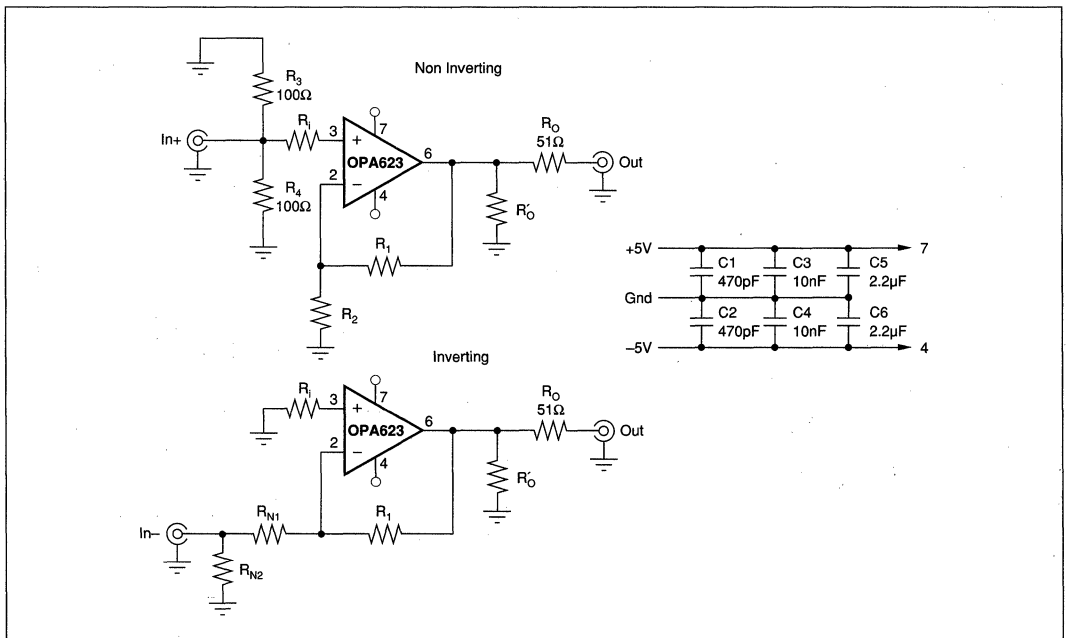


FIGURE 10. Circuit Schematic DEM-OPA623-1GC.

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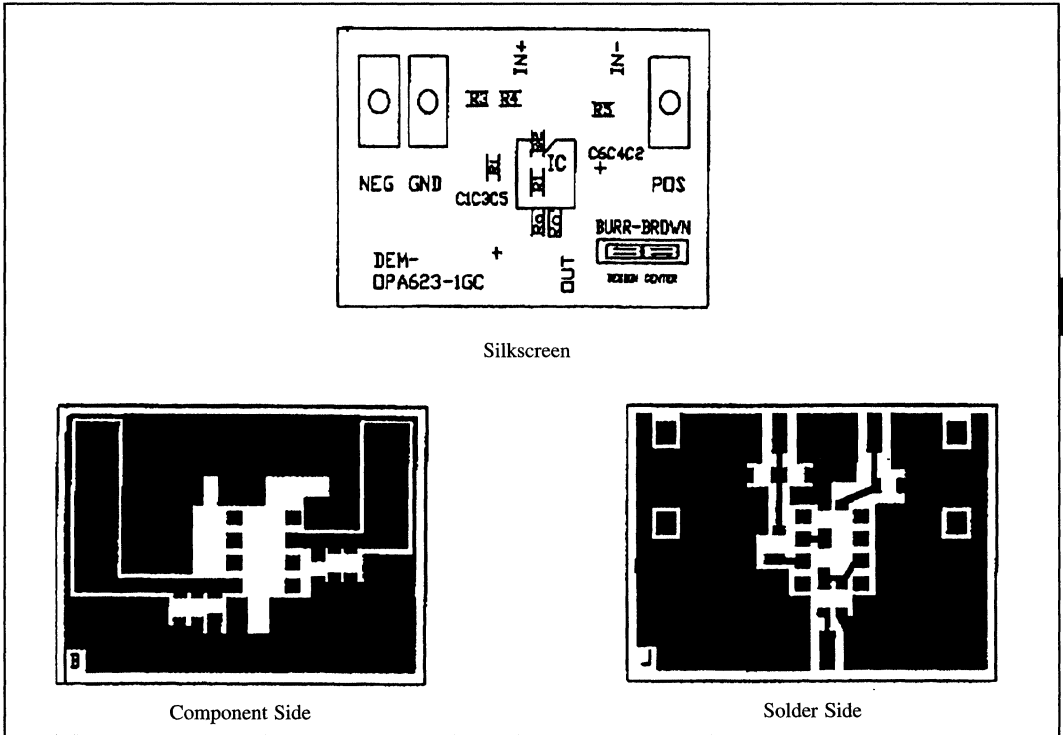


FIGURE 11. Silkscreen and Board Layouts DEM-OPA623-1GC.

COMPONENT	OPA623AP						OPA623AU					
	GAIN						GAIN					
	-2	-1	+1	+2	+5	+10	-2	-1	+1	+2	+5	+10
R ₁	150Ω	150Ω	200Ω	180Ω	100Ω	100Ω	150Ω	150Ω	270Ω	180Ω	100Ω	100Ω
R ₁	390Ω	390Ω	360Ω	300Ω	300Ω	130Ω	390Ω	390Ω	470Ω	300Ω	300Ω	160Ω
R ₂	—	—	—	300Ω	75Ω	15Ω	—	—	—	300Ω	76Ω	18Ω
R _{n1}	200Ω	390Ω	—	—	—	—	200Ω	390Ω	—	—	—	—
R _{n2}	68Ω	56Ω	—	—	—	—	68Ω	56Ω	—	—	—	—
Typical Bandwidth (MHz)												
V _{OUT} = 0.2Vp-p	200	—	320	290	—	170	200	—	320	290	—	170
V _{OUT} = 2.8Vp-p	330	360	340	350	260	210	330	360	340	350	260	210

TABLE I. Recommended Component Values.

APPLICATIONS INFORMATION

The precise pulse response and high slew rate enables the OPA623 to be used in digital communication systems. Figure 12 shows the circuit schematic of an output amplifier with a gain of $+2V/V$, which can drive a 75Ω coaxial cable with a high-speed data stream of 140Mbit/s. Figure 13, for a binary 0, and Figure 14, for a binary 1, shows the pulse masks of the CCITT recommendation G.703 and the corresponding pulse responses of the OPA623. The signal code at the file rate of 139.264Mbit/s is CMI, the signal amplitude is 1Vp-p with ± 11 dB amplitude limits. Naturally, the OPA623 can also be used for HDB3 encoded 34Mbit/s, 155Mbit/s, STM-1, and 155Mbit/s B-ISDN transmission systems.

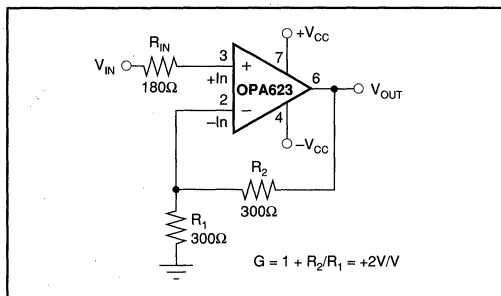


FIGURE 12. Driver Amplifier for a Digital 140Mbit/s Transmission system.

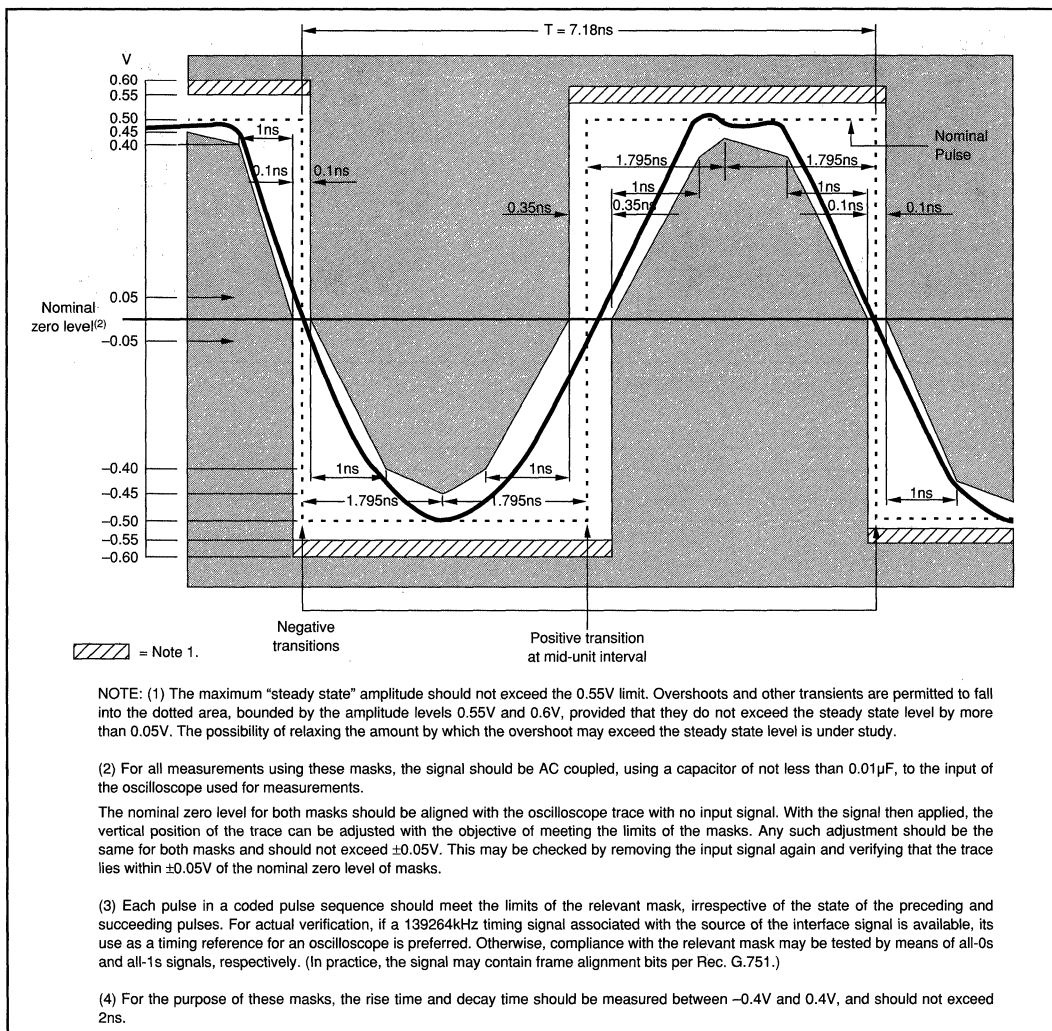


FIGURE 13. Mask of a Pulse Corresponding to a Binary 0 per CCITT Recommendation G.703.

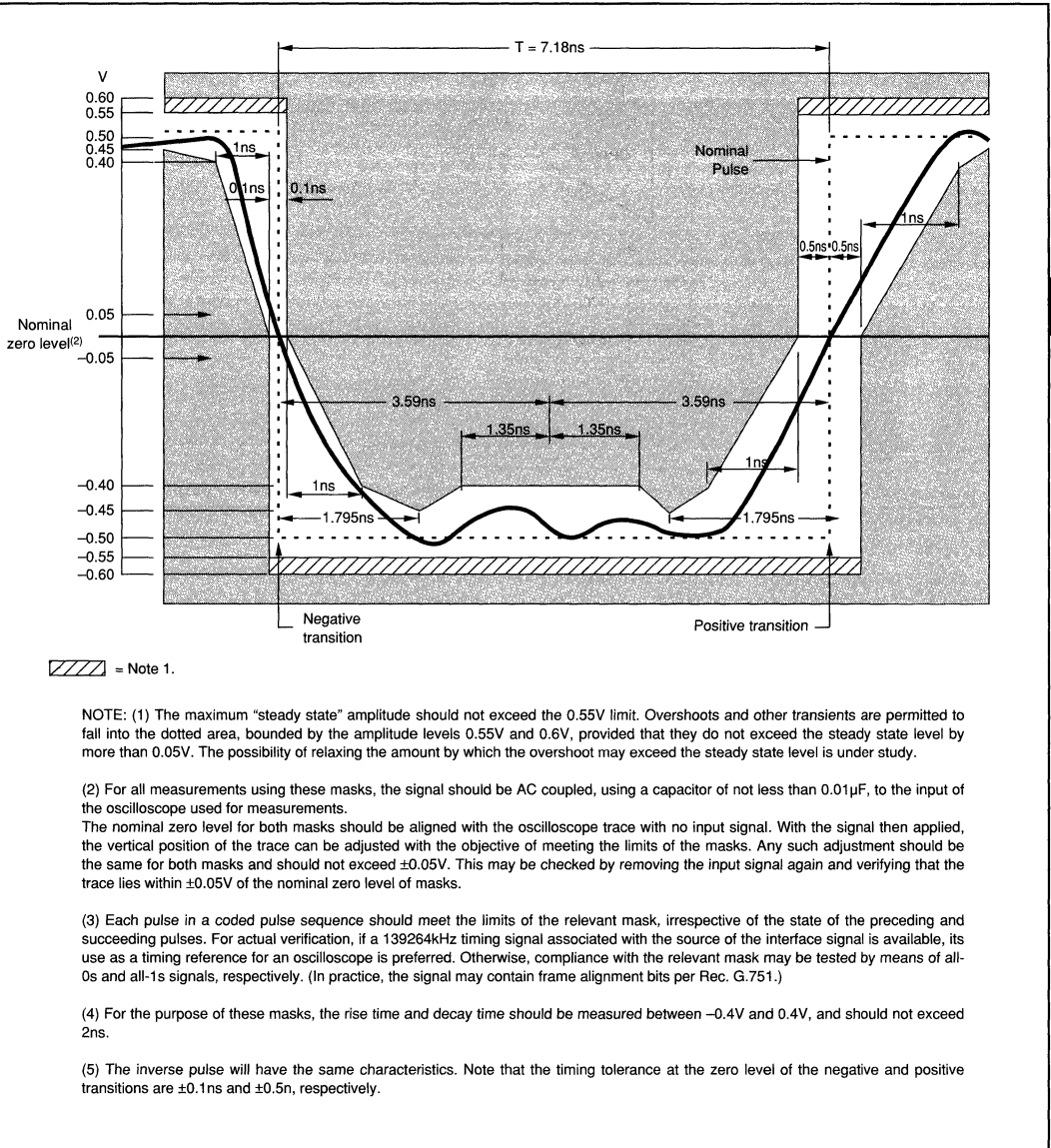


FIGURE 14. Mask of a Pulse Corresponding to a Binary 1 per CCITT Recommendation G.703.

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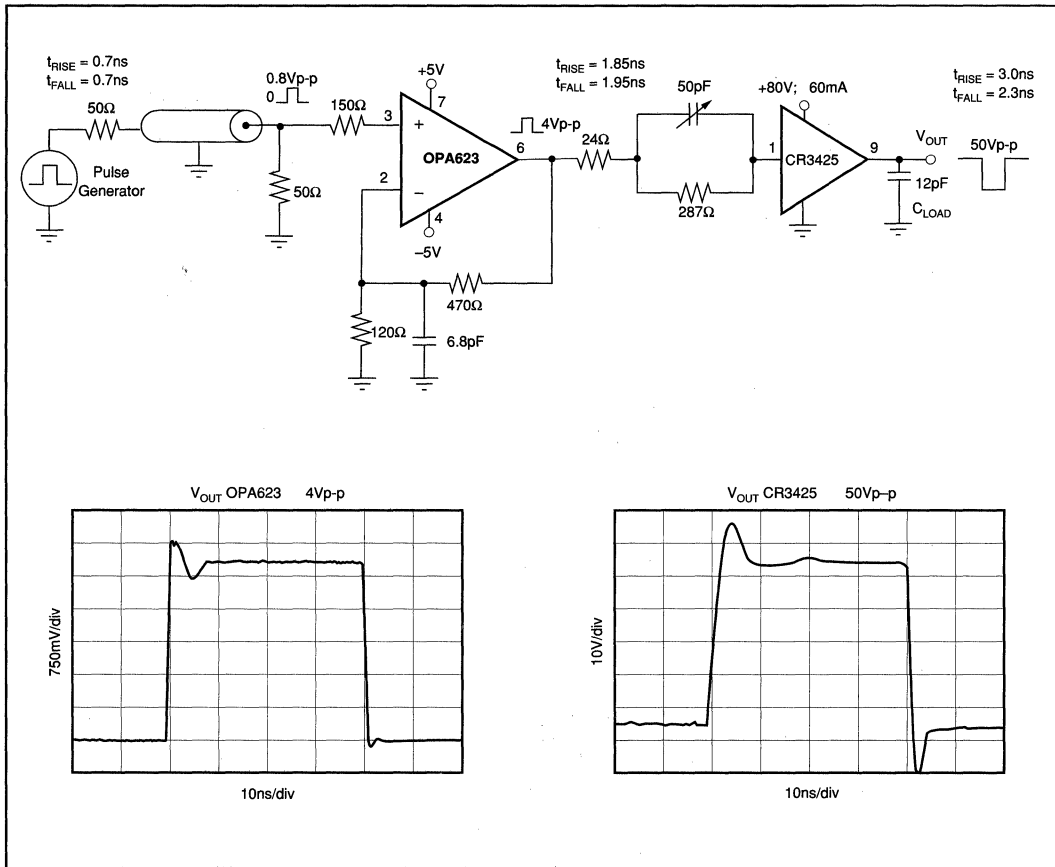


FIGURE 15. Video Amplifier for High Resolution Monitor (1600 x 1200 pixel).

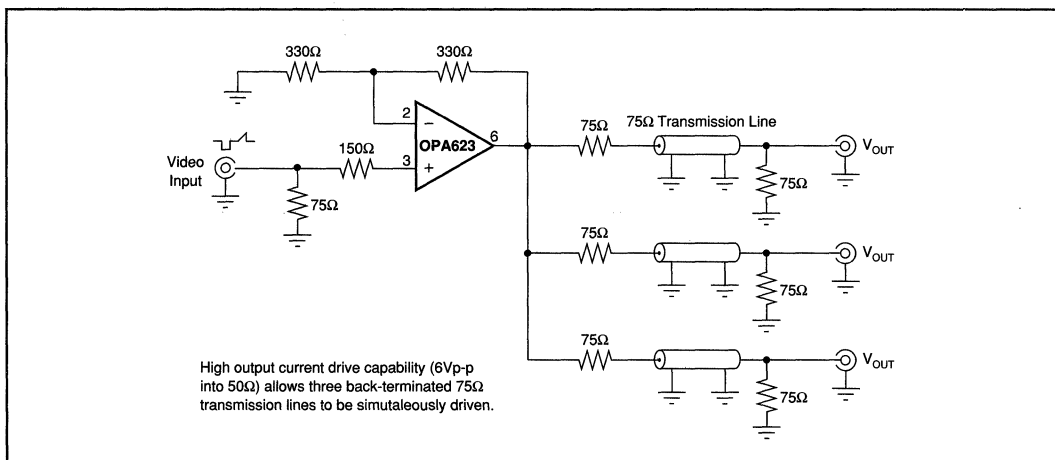
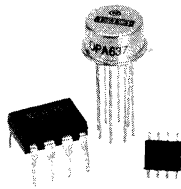


FIGURE 16. Video Distribution Amplifier.

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OPA627
OPA637

OPA627/637

2

OPERATIONAL AMPLIFIERS

Precision High-Speed *Difet*® OPERATIONAL AMPLIFIERS

FEATURES

- VERY LOW NOISE: $4.5\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- FAST SETTLING TIME:
OPA627—550ns to 0.01%
OPA637—450ns to 0.01%
- LOW V_{os} : 100 μV max
- LOW DRIFT: 0.8 $\mu\text{V}/^\circ\text{C}$ max
- LOW I_b : 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain ≥ 5

DESCRIPTION

The OPA627 and OPA637 *Difet* operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage— $\pm 4.5\text{V}$ to $\pm 18\text{V}$. Laser-trimmed *Difet* input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

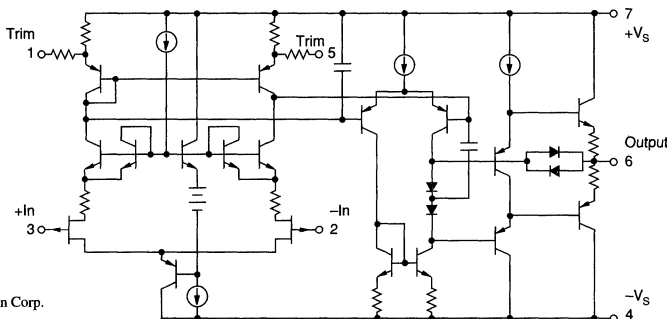
APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

Difet fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



Difet®, Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-998F

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

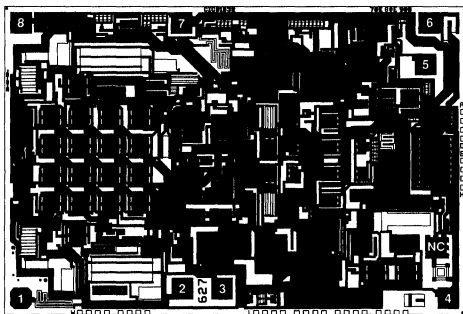
PARAMETER	CONDITIONS	OPA627BM/BP/SM OPA637BM/BP/SM			OPA627AM/AP/AU OPA637AM/AP/AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage AP, BP, AU Grades Average Drift AP, BP, AU Grades Power Supply Rejection	V _S = ±4.5 to ±18V		40 100 0.4 0.8	100 250 0.8 2		130 280 1.2 2.5	250 500 2	μV μV μV/°C μV/°C dB
INPUT BIAS CURRENT ⁽²⁾ Input Bias Current Over Specified Temperature SM Grade Over Common-Mode Voltage Input Offset Current Over Specified Temperature SM Grade	V _{CM} = 0V V _{CM} = 0V V _{CM} = 0V V _{CM} = ±10V V _{CM} = 0V V _{CM} = 0V		1 1 0.5	5 1 5 1 50		2 2 1	10 2 10 2	pA nA nA pA pA nA nA
NOISE Input Voltage Noise Noise Density: f = 10Hz f = 100Hz f = 1kHz f = 10kHz Voltage Noise, BW = 0.1 to 10Hz Input Bias Current Noise Noise Density, f = 100Hz Current Noise, BW = 0.1 to 10Hz			15 8 5.2 4.5 0.6	40 20 8 6 1.6		20 10 5.6 4.8 0.8		nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVp-p fA/√Hz fAp-p
INPUT IMPEDANCE Differential Common-Mode			10 ¹³ 8 10 ¹³ 7			*	*	Ω pF Ω pF
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	V _{CM} = ±10.5V	±11 ±10.5 106	±11.5 ±11 116		*	*	100 110	V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature SM Grade	V _O = ±10V, R _L = 1kΩ V _O = ±10V, R _L = 1kΩ V _O = ±10V, R _L = 1kΩ	112 106 100	120 117 114		106 100	116 110		dB dB dB
FREQUENCY RESPONSE Slew Rate: OPA627 OPA637 Settling Time: OPA627 0.01% 0.1% OPA637 0.01% 0.1% Gain-Bandwidth Product: OPA627 OPA637 Total Harmonic Distortion + Noise	G = -1, 10V Step G = -4, 10V Step G = -1, 10V Step G = -1, 10V Step G = -4, 10V Step G = -4, 10V Step G = 1 G = 10 G = +1, f = 1kHz	40 100	55 135 550 450 450 300 16 80 0.00003		*	*	*	V/μs V/μs ns ns ns ns MHz MHz %
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		±4.5	±15 ±7	±18 ±7.5	*	*	*	V V mA
OUTPUT Voltage Output Over Specified Temperature Current Output Short Circuit Current Output Impedance, Open-Loop	R _L = 1kΩ V _O = ±10V 1MHz	±11.5 ±11 ±35	±12.3 ±11.5 ±45 +70-55 55	±100	*	*	*	V mA mA Ω
TEMPERATURE RANGE Specification: AP, BP, AM, BM, AU SM Storage: AM, BM, SM AP, BP, AU θ _{J-A} : AM, BM, SM AP, BP AU		-25 -55 -60 -40		+85 +125 +150 +125	*	*	*	°C °C °C °C °C/W °C/W °C/W

* Specifications same as "B" grade.

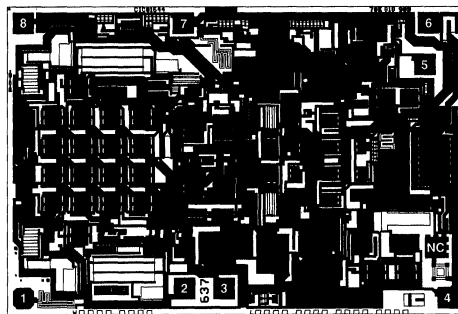
NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at T_J = 25°C. See Typical Performance Curves for warmed-up performance.

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DICE INFORMATION



OPA627 DIE TOPOGRAPHY



OPA637 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	Offset Trim
2	-In	6	Output
3	+In	7	+V _S
4	-V _S	8	Substrate
		NC	No Connection

Substrate Bias: Dielectrically isolated. See data sheet for connection options.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	117 x 80 ±5	2.97 x 2.03 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	46	
Backing:	None	

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	-25°C to +85°C
OPA627BP	Plastic DIP	-25°C to +85°C
OPA627AU	SOIC	-25°C to +85°C
OPA627AM	TO-99 Metal	-25°C to +85°C
OPA627BM	TO-99 Metal	-25°C to +85°C
OPA627SM	TO-99 Metal	-55°C to +125°C
OPA637AP	Plastic DIP	-25°C to +85°C
OPA637BP	Plastic DIP	-25°C to +85°C
OPA637AU	SOIC	-25°C to +85°C
OPA637AM	TO-99 Metal	-25°C to +85°C
OPA637BM	TO-99 Metal	-25°C to +85°C
OPA637SM	TO-99 Metal	-55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	+V _S + 2V to -V _S - 2V
Differential Input Range	Total V _S + 4V
Power Dissipation	1000mW
Operating Temperature	
M Package	-55°C to +125°C
P, U Package	-40°C to +125°C
Storage Temperature	
M Package	-65°C to +150°C
P, U Package	-40°C to +125°C
Junction Temperature	
M Package	+175°C
P, U Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
SOIC (soldering, 3s)	+260°C

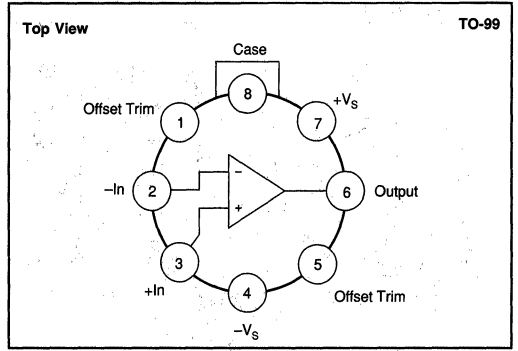
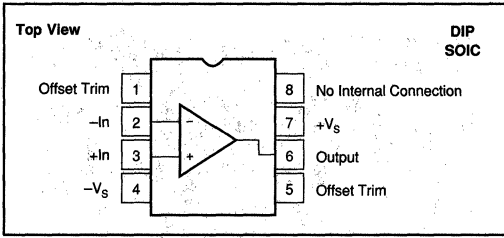
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA627AP	Plastic DIP	006
OPA627BP	Plastic DIP	006
OPA627AU	SOIC	182
OPA627AM	TO-99 Metal	001
OPA627BM	TO-99 Metal	001
OPA627SM	TO-99 Metal	001
OPA637AP	Plastic DIP	006
OPA637BP	Plastic DIP	006
OPA637AU	SOIC	182
OPA637AM	TO-99 Metal	001
OPA637BM	TO-99 Metal	001
OPA637SM	TO-99 Metal	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

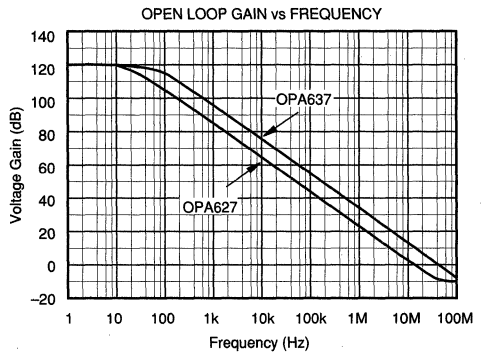
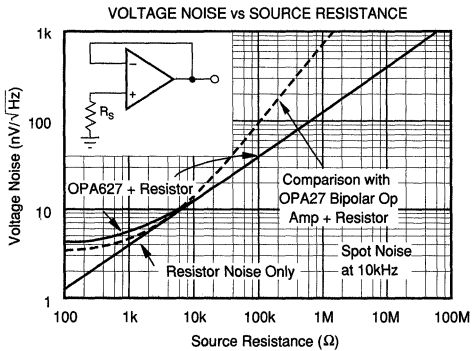
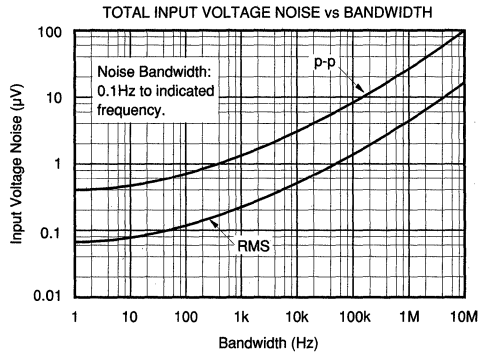
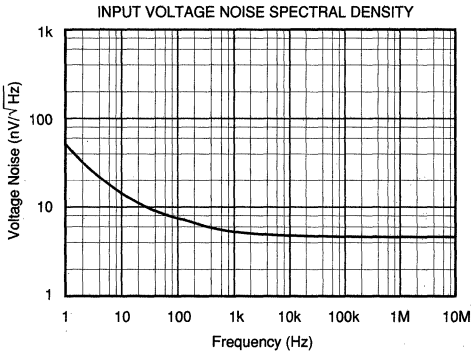
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PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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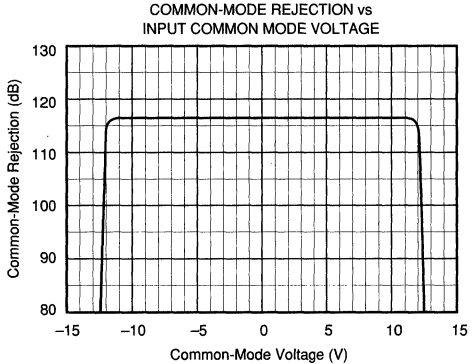
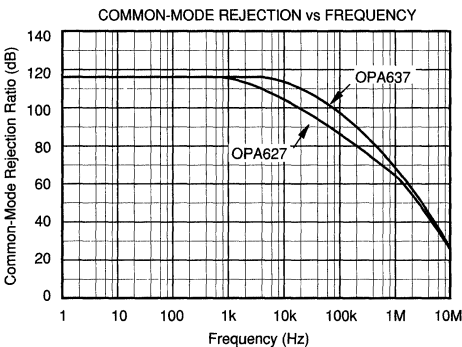
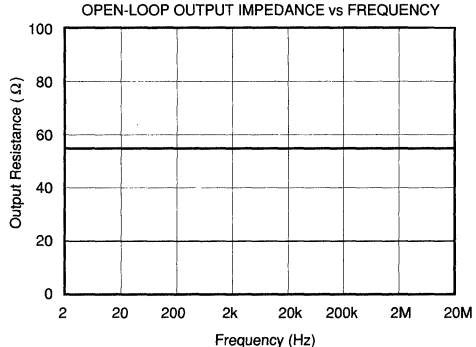
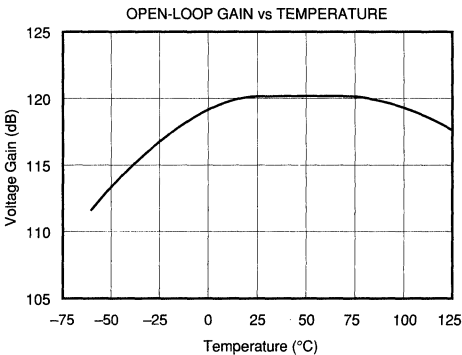
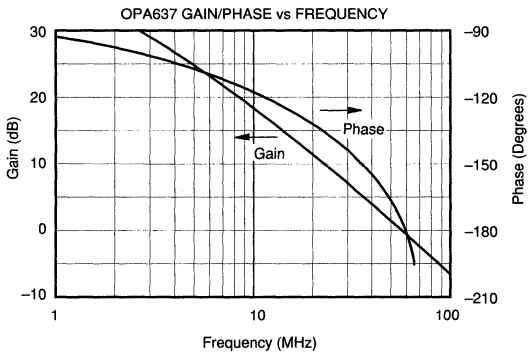
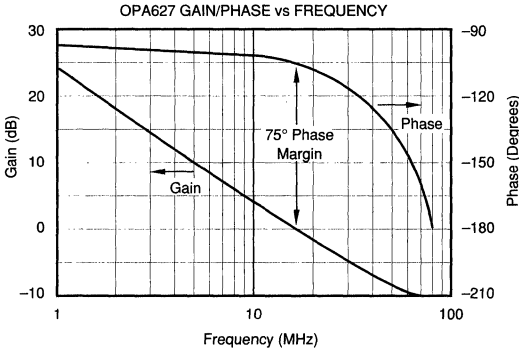
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

OPA627/637

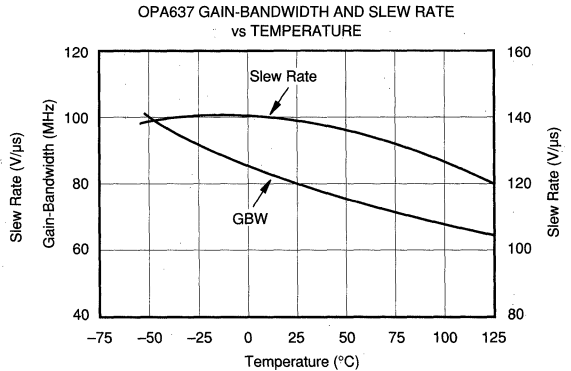
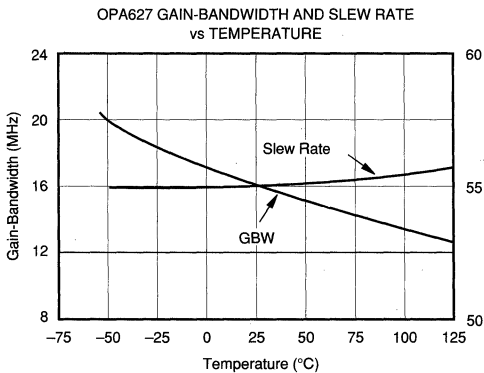
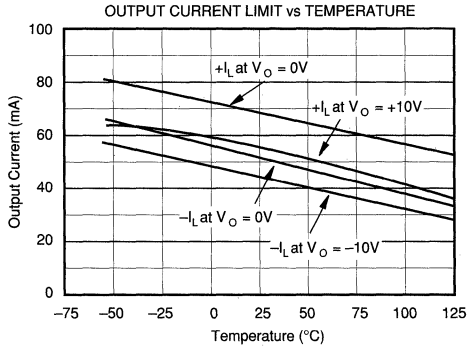
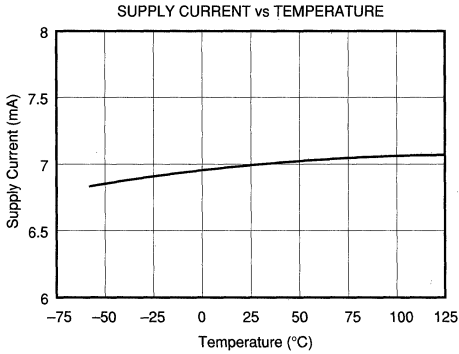
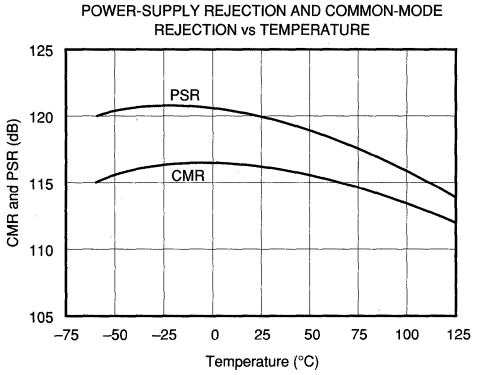
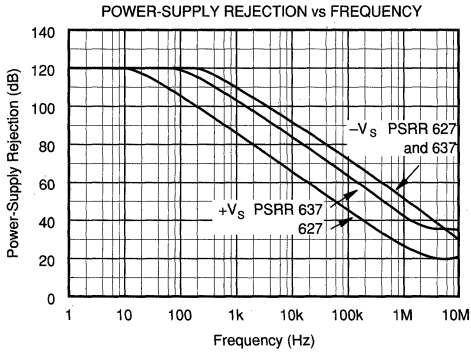
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OPERATIONAL AMPLIFIERS



TYPICAL PERFORMANCE CURVES (CONT)

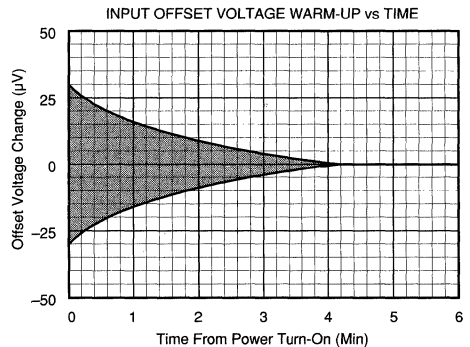
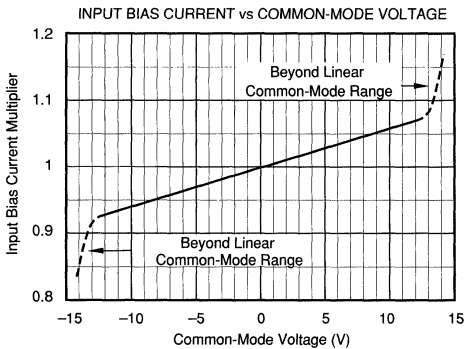
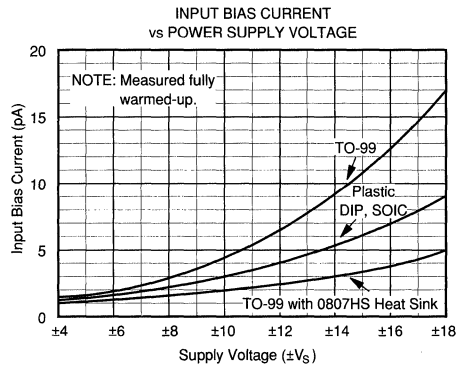
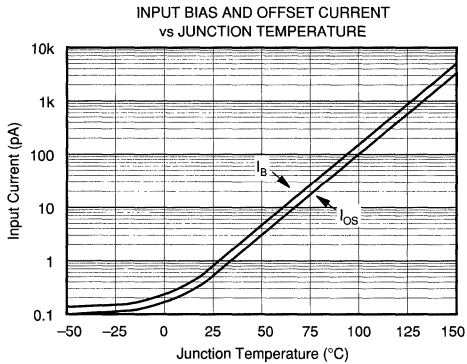
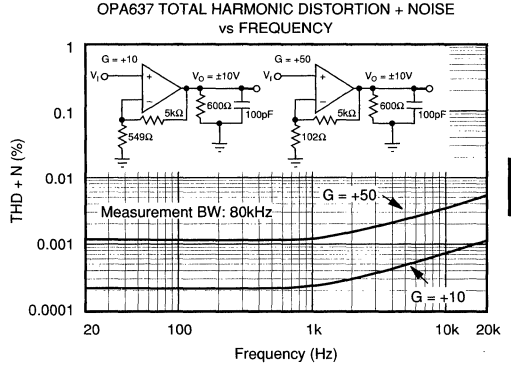
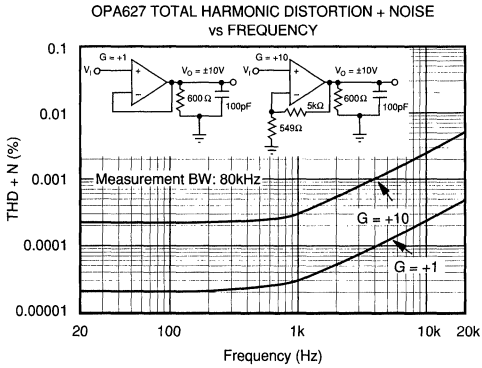
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

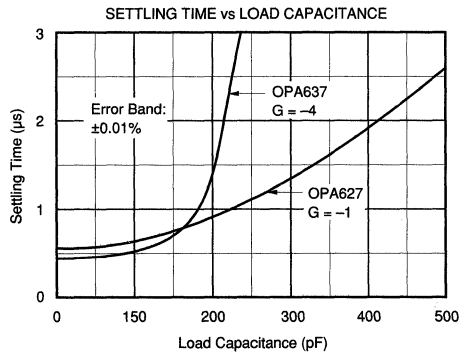
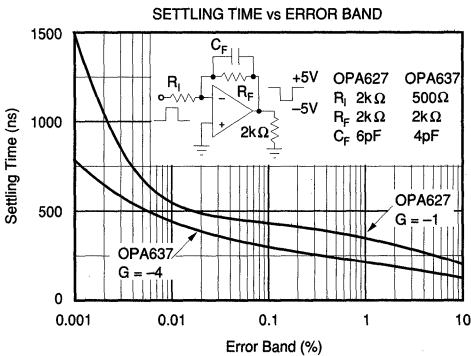
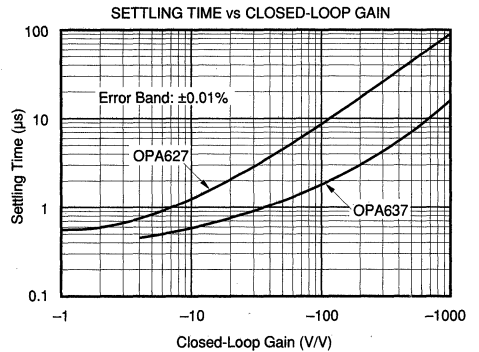
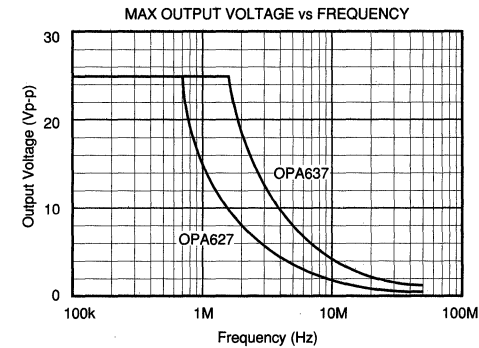
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

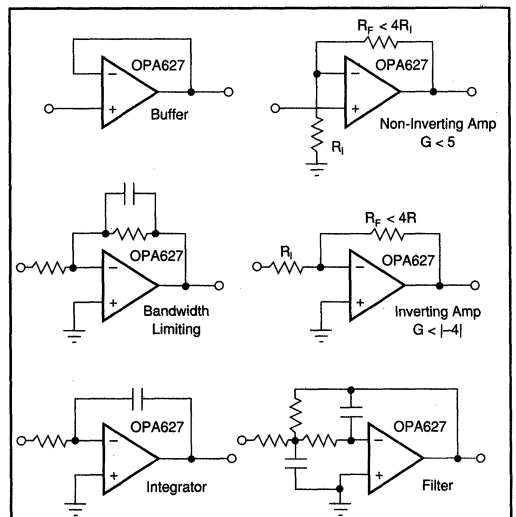


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.

OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately $4\mu\text{V}/^\circ\text{C}$ for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

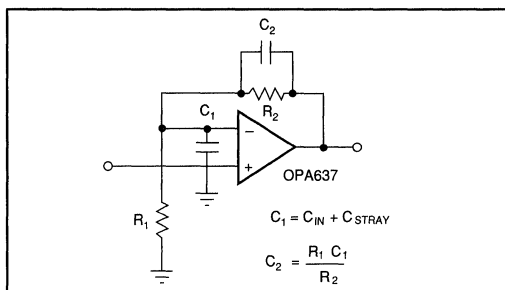


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the

noise of an OPA627. Above a $2\text{k}\Omega$ source resistance, the op amp contributes little additional noise. Below $1\text{k}\Omega$, op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp

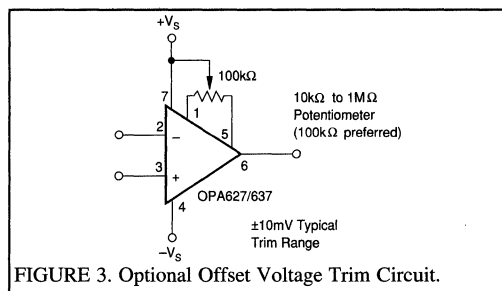


FIGURE 3. Optional Offset Voltage Trim Circuit.

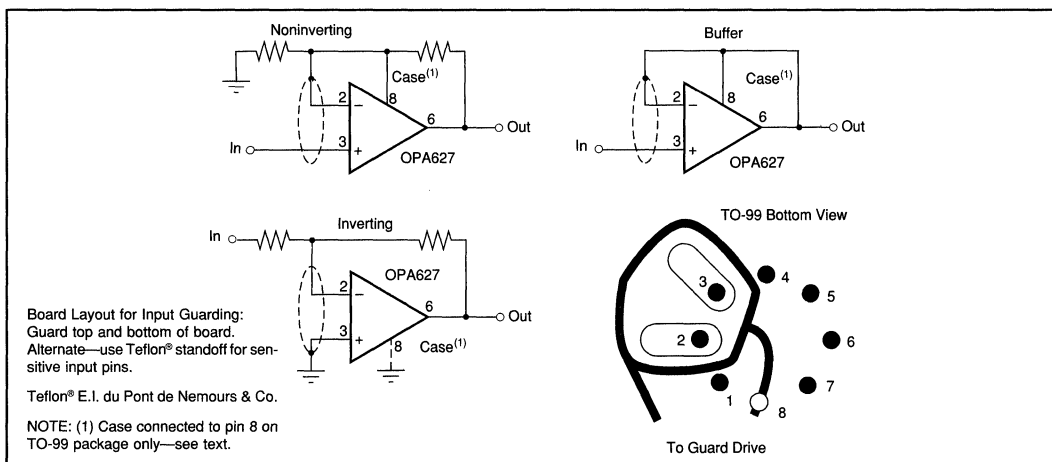


FIGURE 4. Connection of Input Guard for Lowest I_B .

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pins. In most cases 0.1 μ F ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1 μ F solid tantalum capacitors may improve dynamic performance in these applications.

INPUT BIAS CURRENT

Difet fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ± 5 V power supplies reduces power dissipation to one-third of that at ± 15 V. This reduces the I_B of TO-99 metal package devices to approximately one-fourth the value at ± 15 V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board "guard" pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal pack-

age only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to $-V_S$.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

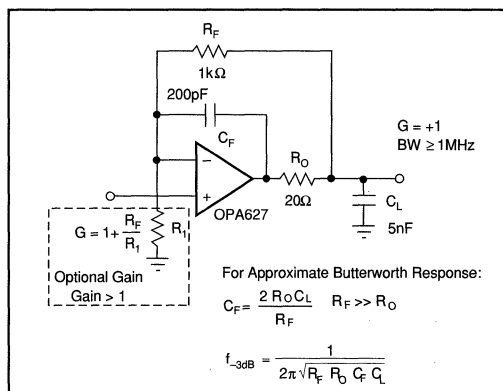


FIGURE 6. Driving Large Capacitive Loads.

PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below -12 V, causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6 μ s. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

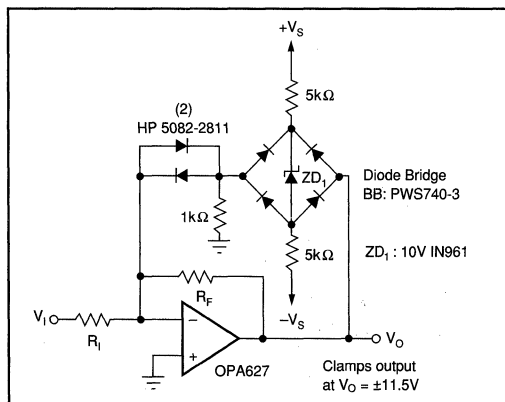


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between $+V_s + 2V$ and $-V_s - 2V$. If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_s , to limit the current. Be aware that adding resistance to the input will increase noise. The $4nV/\sqrt{Hz}$ theoretical thermal noise of a $1k\Omega$ resistor will add to the $4.5nV/\sqrt{Hz}$ noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of $6nV/\sqrt{Hz}$. Resistors below 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately $25nA$ —more than a thousand

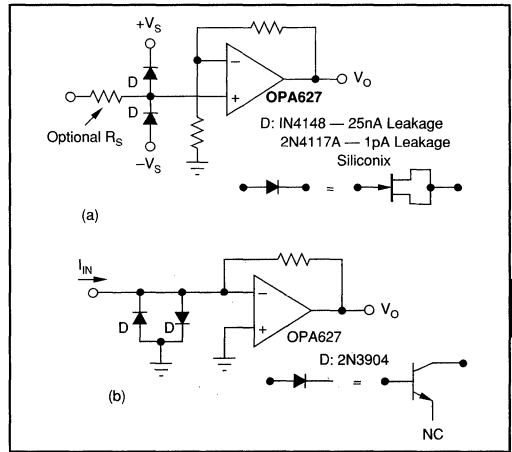


FIGURE 7. Input Protection Circuits.

times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at $1pA$ and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed $2V$ beyond the

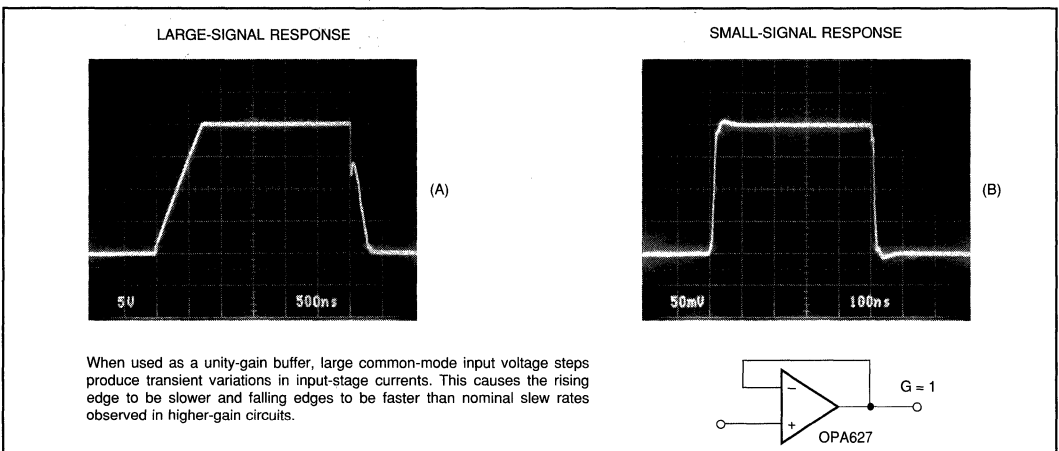


FIGURE 8. OPA627 Dynamic Performance, $G = +1$.

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power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the the low voltage present at the summing junction, common signal diodes may have excessive leakage current.

Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

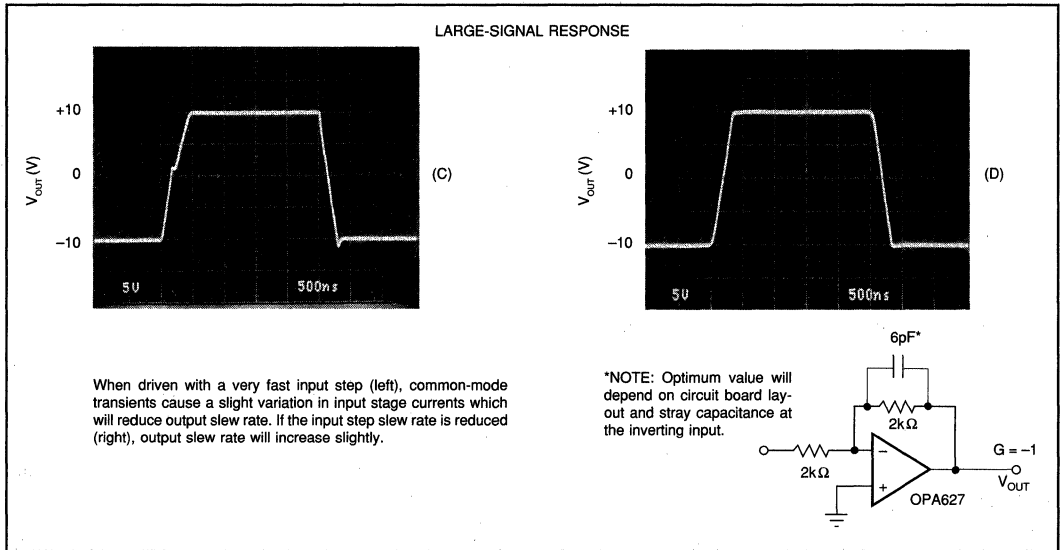


FIGURE 9. OPA627 Dynamic Performance, $G = -1$.

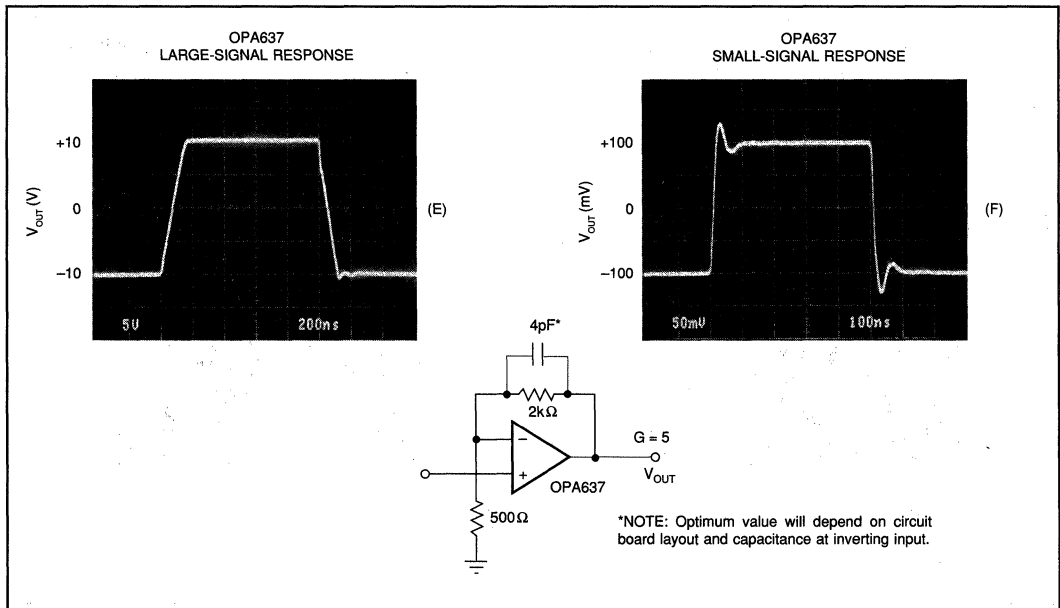


FIGURE 10. OPA637 Dynamic Response, $G = 5$.

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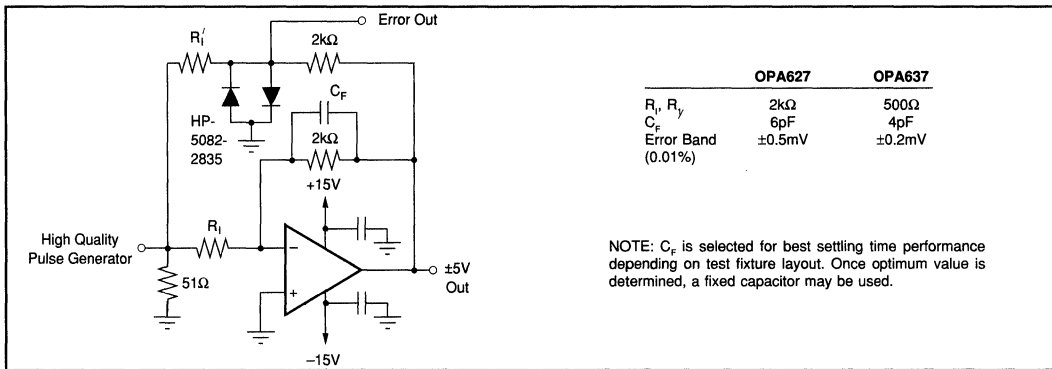


FIGURE 11. Settling Time and Slew Rate Test Circuit.

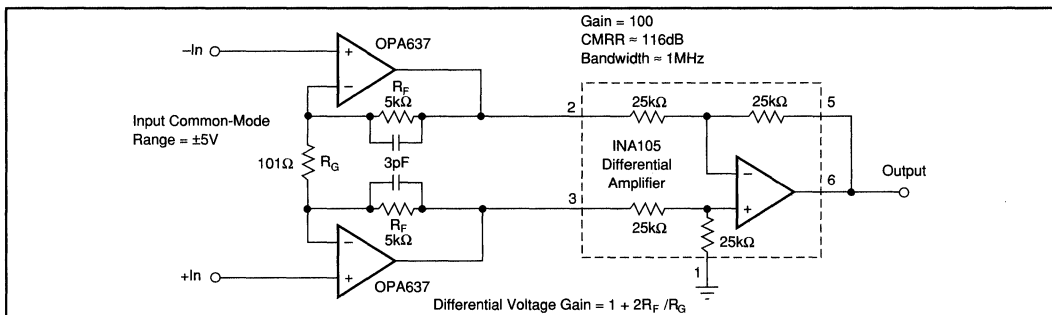


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

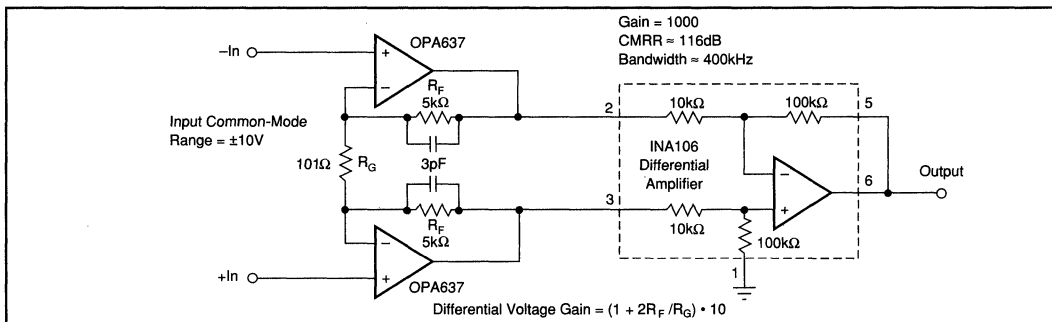


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.

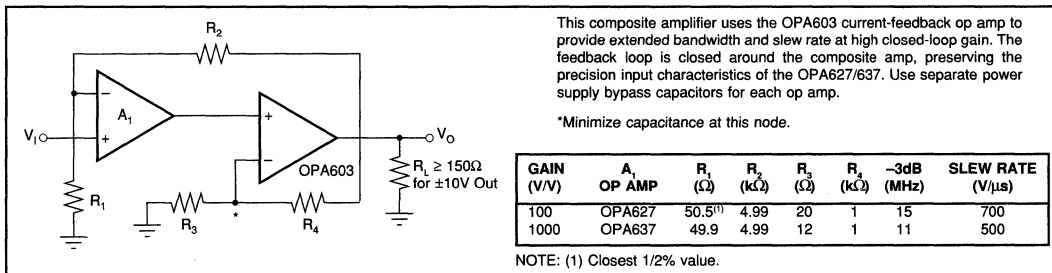


FIGURE 14. Composite Amplifier for Wide Bandwidth.



OPA628

Low Distortion Wideband OPERATIONAL AMPLIFIER

FEATURES

- EXCELLENT DIFFERENTIAL GAIN: 0.015%
- EXCELLENT DIFFERENTIAL PHASE: 0.015°
- LOW DISTORTION: 90dB SFDR
- TWO TONE THIRD ORDER INTERCEPT: 60dBm
- LOW NOISE: $2.5nV/\sqrt{Hz}$
- LOW NOISE FIGURE: 9dB
- BANDWIDTH (Gain = +1): 160MHz
- 0.1dB GAIN FLATNESS: 30MHz
- LOW OFFSET VOLTAGE: 500 μ V

APPLICATIONS

- BROADCAST QUALITY VIDEO
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- PRECISION ADC/DAC BUFFER
- TELECOMMUNICATIONS
- ANALYTICAL INSTRUMENTS
- ACTIVE FILTERS
- DC RESTORATION CIRCUITS

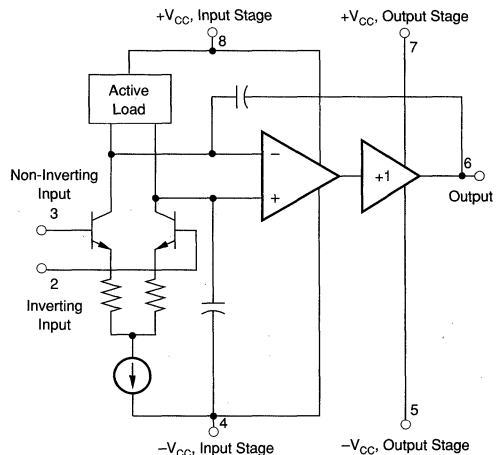
DESCRIPTION

The OPA628 is a low distortion, wideband operational amplifier. It features low differential gain error of 0.015% and low differential phase error of 0.015° at NTSC and PAL frequencies with a 150 Ω load (a back-terminated 75 Ω cable). The 0.1dB gain flatness to 30MHz, and the excellent differential gain and phase, make the OPA628 ideal for broadcast quality video applications. In addition, the spurious free dynamic range of 90dB makes the OPA628 an excellent choice to buffer the input of precision A/D converters. It can also be used to provide a buffer for the output of precision high speed D/A converters. The two tone third order intercept of the OPA628 is 60dBm.

The OPA628 is a unity gain stable, voltage feedback operational amplifier. It has all of the benefits associated with voltage feedback amplifiers including high input impedance, high common mode rejection, and symmetrical differential input flexibility. The unity gain bandwidth of the OPA628 is 160MHz. The low noise of $2.5nV/\sqrt{Hz}$ and low noise figure of 9dB ($R_s = 50\Omega$) make the OPA628 very useful in precision applications requiring wide dynamic range.

The superior distortion performance of the OPA628 is achieved by its multistage architecture which provides high open loop gain. The distortion performance is additionally enhanced by separating the power supplies

to the input and output stages requiring four power supply connections as shown in the block diagram below. This separation of supplies eliminates the effects of package and wire bond parasitic capacitance and inductance. The OPA628 is powered with $\pm 5VDC$ supplies for low power dissipation. The OPA628 is available in 8-pin plastic DIP and SOIC packages. The temperature range is -40°C to +85°C.



SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$ (including feedback impedance), and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA628AP, AU			UNITS	
		MIN	TYP	MAX		
INPUT NOISE Voltage: $R_S = 0\Omega$	$f_O = 100Hz$		8.3		nV/ \sqrt{Hz}	
	$f_O = 1kHz$		3.5		nV/ \sqrt{Hz}	
Current Noise Figure	$f_O = 10kHz$		2.6		nV/ \sqrt{Hz}	
	$f_O = 100kHz$		2.5		nV/ \sqrt{Hz}	
	$f_O = 1MHz$ to 100MHz		2.5		nV/ \sqrt{Hz}	
	$f_B = 100Hz$ to 10MHz		8.1		μV_{rms}	
	$f_O = 100kHz$ to 100MHz		2.2		$\mu A/\sqrt{Hz}$	
	$R_S = 50\Omega$, $f_O = 1MHz$ to 100MHz		9.3		dB	
OFFSET VOLTAGE Input Offset Voltage	$V_{CM} = 0VDC$		± 0.5	± 1	mV	
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 6		$\mu V/^\circ C$	
Supply Rejection (PSRR)	$\pm V_{CC} = \pm 4.5V$ to $\pm 5.5V$	90	105		dB	
Over Specification Temperature	$\pm V_{CC} = \pm 4.5V$ to $\pm 5.5V$, $T_A = T_{MIN}$ to T_{MAX}		100		dB	
INPUT BIAS CURRENT Input Bias Current	$V_{CM} = 0VDC$		15	30	μA	
Over specification Temperature	$V_{CM} = 0VDC$, $T_A = T_{MIN}$ to T_{MAX}		22		μA	
Input Offset Current	$V_{CM} = 0VDC$		± 0.3	± 2	μA	
Over Specification Temperature	$T_A = T_{MIN}$ to T_{MAX}		± 0.8		μA	
INPUT IMPEDANCE Differential	Open-Loop		30 2		k Ω pF	
Common-Mode			10 6		M Ω pF	
INPUT VOLTAGE RANGE Common-Mode Input Range		90	± 2.5		V	
Common-Mode Rejection (CMRR)	$V_{CM} = \pm 2.5V$		110		dB	
Over Specification Temperature	$V_{CM} = \pm 2.5V$, $T_A = T_{MIN}$ to T_{MAX}		105		dB	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain		90	100		dB	
Over Specification Temperature	$T_A = T_{MIN}$ to T_{MAX}		96		dB	
FREQUENCY RESPONSE Closed-Loop Bandwidth (-3dB)	Gain = +1V/V		160		MHz	
Bandwidth 0.1dB Flat	Gain = +2V/V		77		MHz	
	Gain = +5V/V		24		MHz	
Differential Gain	Gain = +2V/V		30		MHz	
Differential Phase	3.58MHz, Gain = +2, $V_O = 1.4V$ Ramp		0.015		%	
Harmonic Distortion	3.58MHz, Gain = +2, $V_O = 1.4V$ Ramp		0.015		degrees	
3rd-Order Intercept	$R_L = 100\Omega$, $G = +1V/V$, $f = 5MHz$, $V_O = 2Vp-p$					
	Second Harmonic		-91		dBc	
	Third Harmonic		-98		dBc	
	$R_L = 500\Omega$, $G = +2V/V$, $f = 5MHz$, $V_O = 2Vp-p$					
	Second Harmonic		-90		dBc	
	Third Harmonic		-97		dBc	
	$R_L = 500\Omega$, $G = +2V/V$, $f = 10MHz$, $V_O = 2Vp-p$					
	Second Harmonic		-83		dBc	
	Third Harmonic		-87		dBc	
	3rd-Order Intercept	$f_C = 5MHz$, $G = +2$		70		dBm
	3rd-Order Intercept	$f_C = 10MHz$, $G = +2$		60		dBm
	Two-tone 3rd-Order Intercept	$f_C = 5MHz$, $G = +2$		60		dBm
Full Power Response ⁽¹⁾	$V_O = 5Vp-p$, Gain = +1V/V		20		MHz	
	$V_O = 2Vp-p$, Gain = +1V/V		49		MHz	
Slew Rate	2V Step, Gain = -1V/V		310		V/ μs	
Overshoot	2V Step, Gain = -1V/V		2		%	
Settling Time: 0.10%	2V Step, Gain = -1V/V		20		ns	
0.01%			64		ns	
Overload Recovery Time ⁽²⁾			60		ns	
Phase Margin	Gain = +1V/V		60		degrees	
Rise Time	Gain = +1V/V, 10% to 90%		60		degrees	
Small Signal	$V_O = 100mVp-p$		3		ns	
Large Signal	$V_O = 6Vp-p$		15		ns	
RATED OUTPUT Voltage Output	$f_O = 1MHz$, $R_L = 100\Omega$	± 3			V	
Over Specification Temperature	$f_O = 1MHz$, $R_L = 100\Omega$, $T_A = T_{MIN}$ to T_{MAX}		± 3		V	
Output Resistance	$f_O = 1MHz$, $R_L = 50\Omega$		± 3		V	
Load Capacitance Stability	1MHz, Gain = +1V/V		0.0005		Ω	
Short Circuit Current	Gain = +1V/V, $V_O = 2Vp-p$		20		pF	
Short Circuit Current	Continuous, Source		+180		mA	
Short Circuit Current	Continuous, Sink		-130		mA	

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SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$ (including feedback impedance), and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA628AP, AU			UNITS
		MIN	TYP	MAX	
POWER SUPPLY					
Rated Voltage	$\pm V_{CC}$		± 5		VDC
Derated Performance	$\pm V_{CC}$	± 4.5		± 6	VDC
Current, Quiescent	$I_O = 0mADC$		29	32	mA
Current, Quiescent	$I_O = 0mADC, T_A = T_{MIN}$ to T_{MAX}		31	35	mA
TEMPERATURE RANGE					
Specification: AP, AU	T_{MIN} and T_{MAX}	-40		+85	$^\circ C$
Storage: AP, AU	Ambient Temperature	-55		+125	$^\circ C$
θ_{JA} AP			90		$^\circ C/W$
AU			100		$^\circ C/W$

NOTES: (1) Full power response = slow rate/($2\pi V_{peak}$). (2) Time for output to resume linear operation after saturation.

ORDERING INFORMATION

MODEL	PACKAGE
OPA628AP	8-Pin Plastic DIP
OPA628AU	8-Pin SOIC

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA628AP	8-Pin Plastic DIP	006
OPA628AU	8-Pin SOIC	182

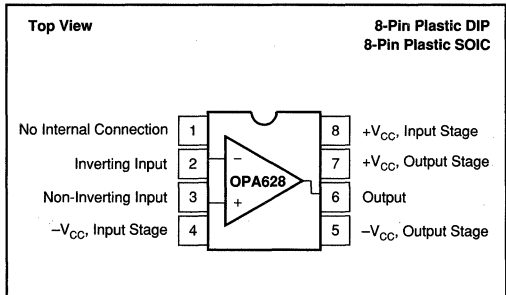
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 7VDC$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	5V
Input Voltage Range	See Applications Information
Storage Temperature Range: AP, AU	$-55^\circ C$ to $+125^\circ C$
Lead Temperature (soldering, DIP 10s)	$+300^\circ C$
(soldering, SOIC 3s)	$+260^\circ C$
Output Short Circuit to Ground ($+25^\circ C$)	Continuous to Ground
Junction Temperature (T_J)	$+175^\circ C$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may cause damage.

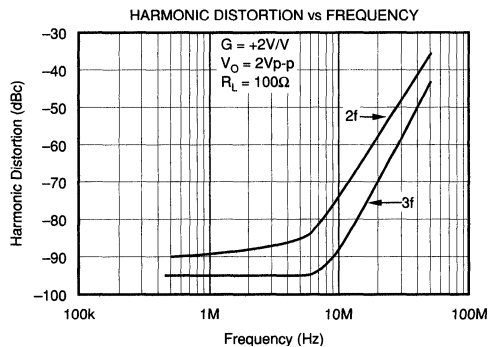
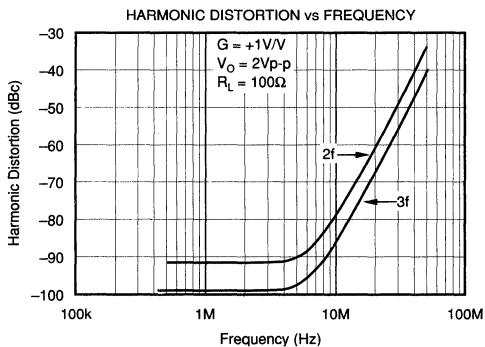
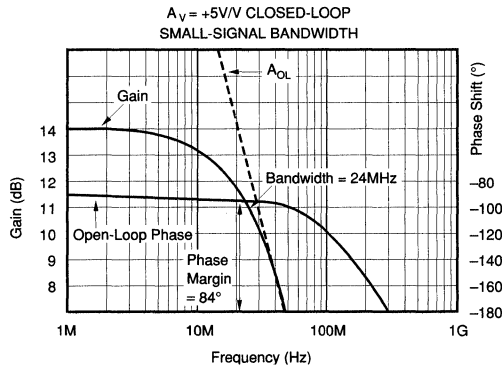
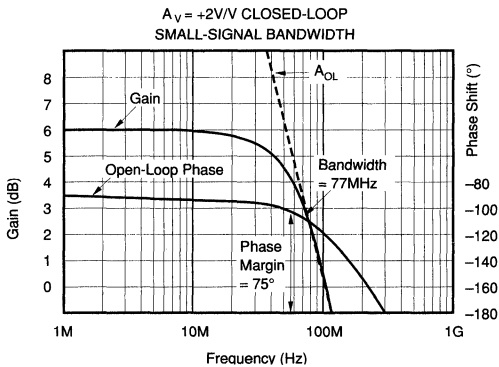
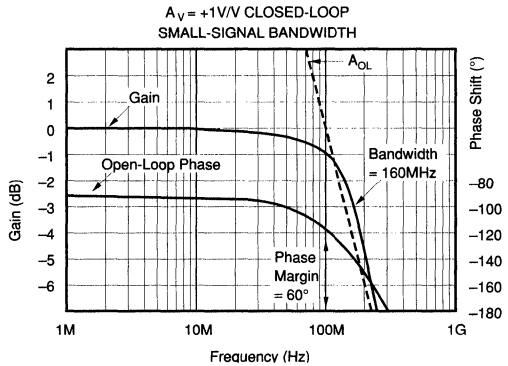
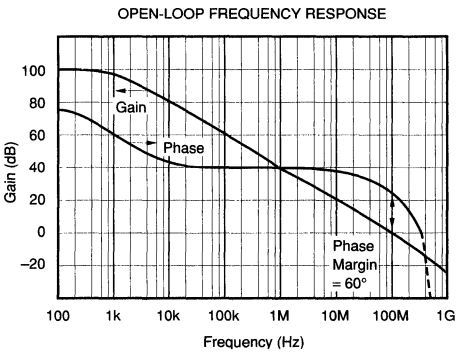
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

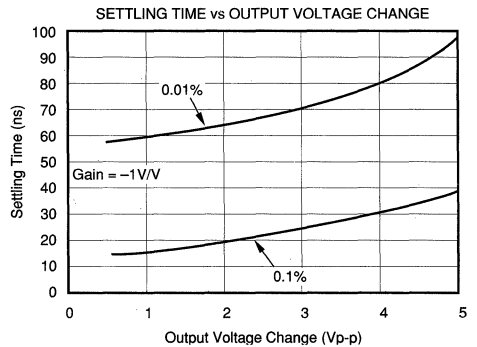
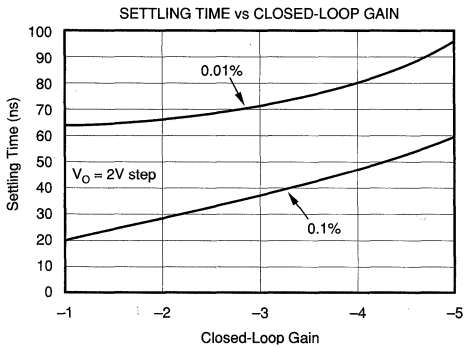
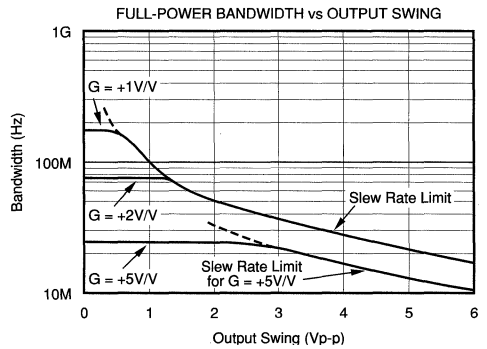
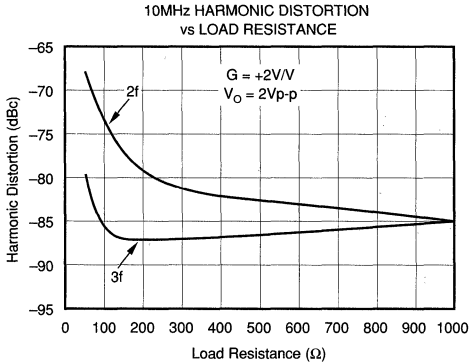
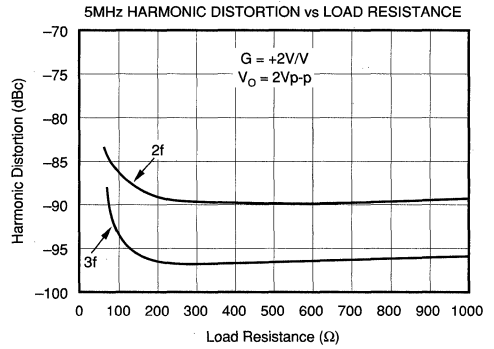
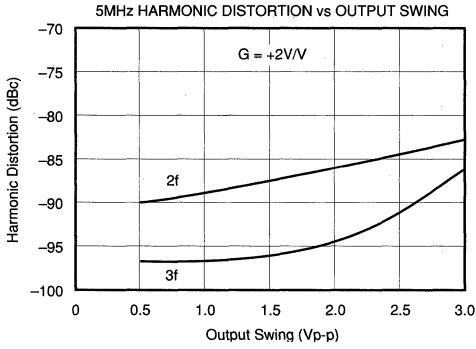
At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$ (including feedback impedance), and $T_A = +25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

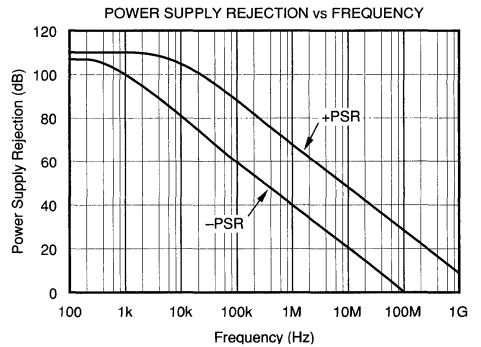
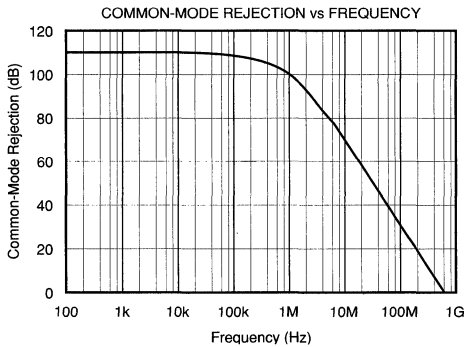
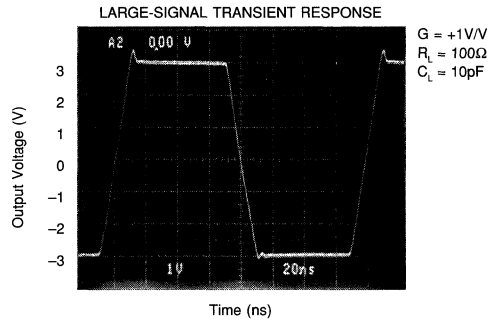
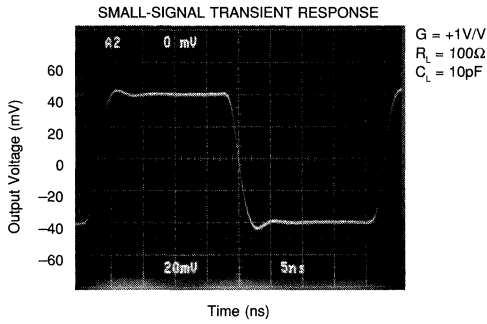
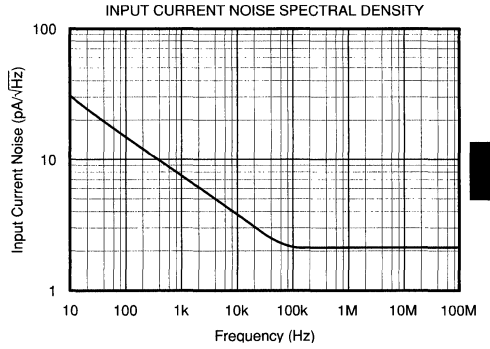
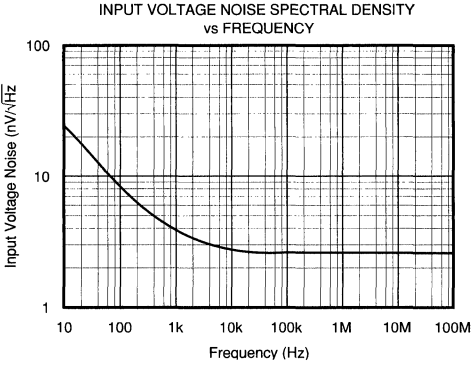
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TYPICAL PERFORMANCE CURVES (CONT)

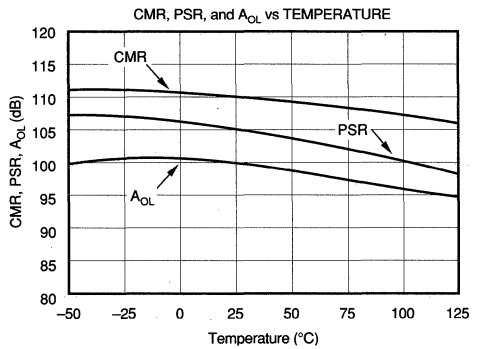
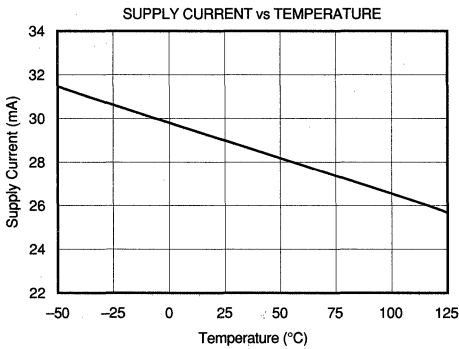
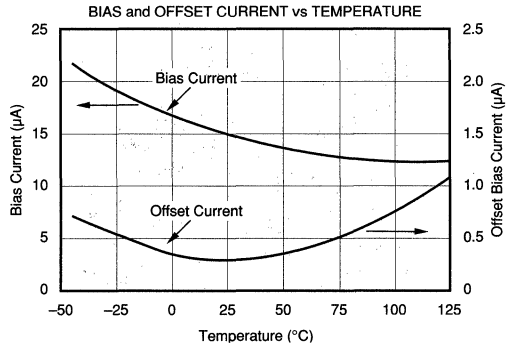
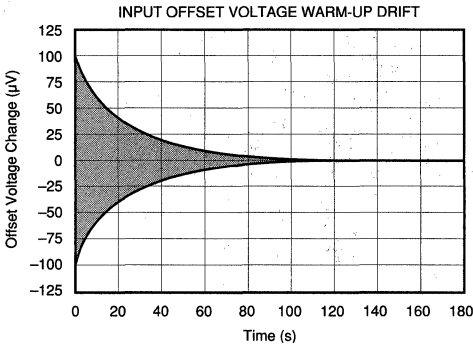
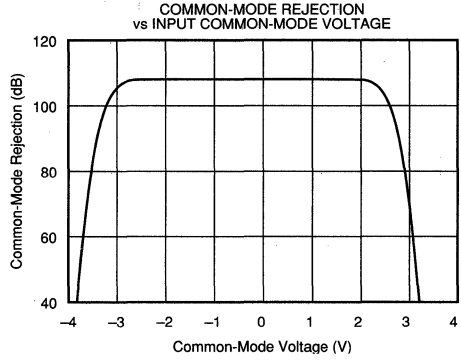
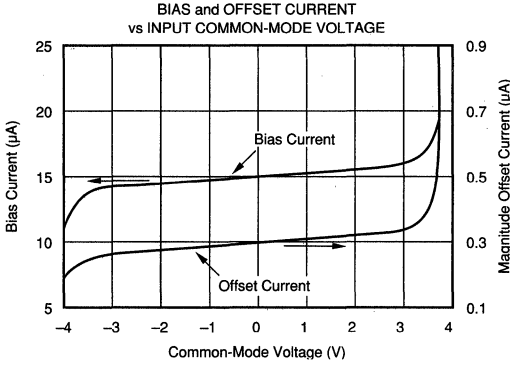
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TYPICAL PERFORMANCE CURVES (CONT)

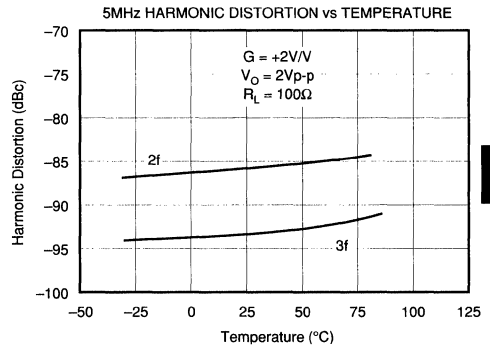
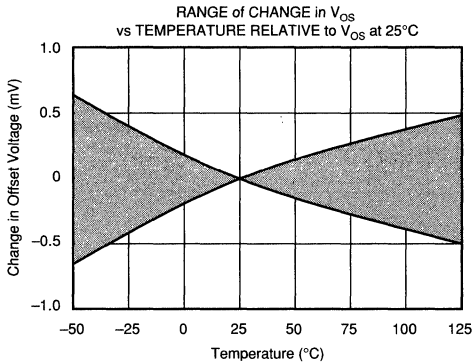
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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_L = 100\Omega$ (including feedback impedance), and $T_A = +25^\circ C$ unless otherwise noted.



DISCUSSION OF PERFORMANCE

The OPA628's classical operational amplifier architecture employs true differential and fully symmetrical inputs allowing optimal performance in either inverting or non-inverting circuit applications. All traditional circuit configurations and op amp theory apply to the OPA628. The use of low drift thin film resistors allows internal operating currents to be laser trimmed at wafer level to optimize AC performance such as distortion, bandwidth and settling time, as well as DC parameters such as input offset voltage. The result is a wideband, high frequency monolithic operational amplifier with a gain-bandwidth product of 150MHz, a spurious free dynamic range (SFDR) of 90dB, and input offset voltage of 500 μV .

The layout considerations described in the "Printed Circuit Board Guidelines" section must be followed to achieve the best possible performance of the OPA628.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set. All PAL measurements were performed using a Rohde & Schwarz Video Analyzer UAF.

DG and DP of the OPA628 were measured with the amplifier in a gain of +2V/V with 75 Ω input impedance and the output back-terminated in 75 Ω . The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse.

With these conditions the test circuit shown in Figure 1 delivered a 100IRE modulated ramp to the 75 Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA628 is 0.015% differential gain and 0.015 $^\circ$ differential phase to both NTSC and PAL standards. Increasing the closed loop gain degrades the DP and DG.

GAIN FLATNESS

Small signal ± 0.1 dB gain flatness can be achieved up to 30MHz in a non-inverting gain of +2V/V through careful layout of the printed circuit board and frequency shaping of the feedback network. Frequency shaping is achieved empirically by placing a small capacitor in parallel with either the feedback resistor or the input resistor of the OPA628 to compensate for printed circuit parasitic capacitance. A capacitor in the range of approximately 1pF to 20pF is suggested. Printed circuit board layout design will determine if the capacitor should be placed across the feedback resistor or the input resistor.

Small signal ± 0.1 dB gain flatness of greater than 30MHz can be achieved at a gain of +1V/V. To eliminate the effects of package lead inductance, a small value resistor should be included in the feedback path. Maximizing gain flatness for a particular layout requires optimization of the feedback resistor; an approximate value is 50 Ω to 75 Ω .

DISTORTION

The OPA628's Harmonic Distortion characteristics when driving a 100 Ω load are shown vs frequency and vs voltage output in the Typical Performance Curves. Distortion can be further optimized by decreasing output loading as also shown in Typical Performance Curves. Include the contribution of

OPA628

2

OPERATIONAL AMPLIFIERS

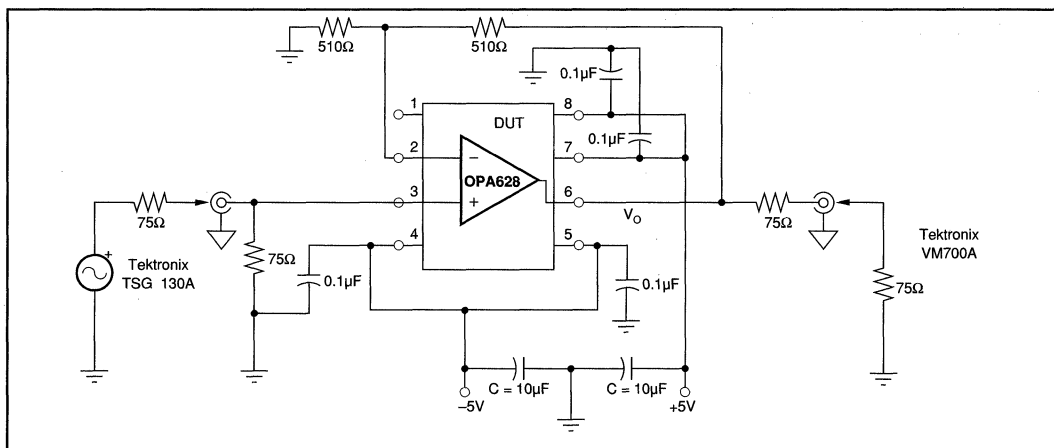


FIGURE 1. Configuration For Testing Differential Gain/Phase.

the feedback resistance when calculating the effective load resistance at the amplifier output. A high performance spectrum analyzer such as the HP3585B should be used to measure distortion.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. The specification table shows the OPA628's two-tone, third order IM intercept at 5MHz and 10MHz. For these measurements, tones were spaced 200kHz apart. This data is particularly useful for determining the magnitude of the third-order IM products. The magnitude of the third-order IM products can be easily calculated from the expression:

$$\text{Third IM} = 2(\text{OIP3} - P_o)$$

where OIP3 = third-order output intercept, dBm
 P_o = output level/tone, dBm/tone
 Third IM = third-order intermodulation ratio below each output tone, dB

As an example, with OIP3 = 60dBm, for $P_o = 10$ dBm, the third order IM = $2(60 - 10) = 100$ dB below either 10dBm tone. The OPA628's low IM makes the device an excellent choice for a variety of RF signal processing applications. In order to obtain the full low distortion performance of the OPA628, it is imperative to follow the recommendations described in the "Printed Circuit Board Guidelines" section.

OUTPUT DRIVE CAPABILITY

The OPA628 has been optimized for low distortion performance with back terminated 50Ω and 75Ω loads ($R_{LOAD} = 100\Omega$ and 150Ω , respectively). However, it is capable of driving 6Vpp into a 50Ω load with a sacrifice in distortion. This high-output drive capability makes the OPA628 an ideal choice for a wide range of RF, IF, and video applications. All transmission lines should be terminated with the characteristic impedance of the transmission line.

Internal current-limiting circuitry limits output current to about 130mA at 25°C. This prevents damage from accidental shorts to common and eliminates the need for external

current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 2, the OPA628 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

NOISE FIGURE

The OPA628's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA628's Noise Figure vs Source Resistance is shown in Figure 3 for frequencies above 1MHz.

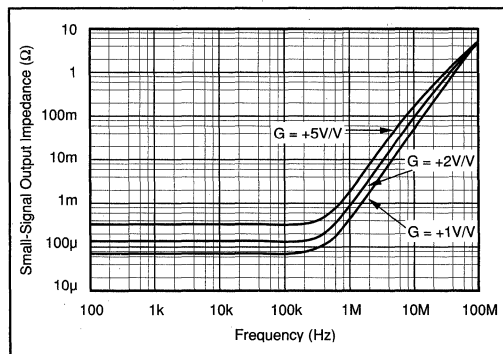


FIGURE 2. Small-Signal Output Impedance vs Frequency.

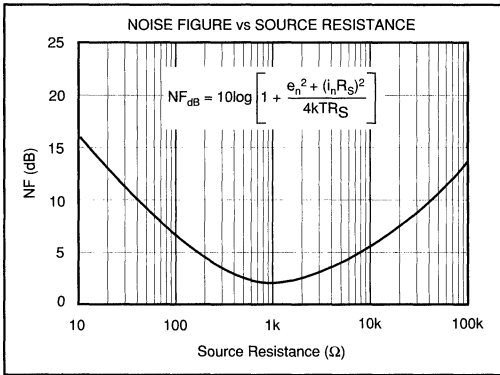


FIGURE 3. Noise Figure vs Source Resistance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu\text{V}$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, is only 64ns to 0.01% for a 2V step. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Printed Circuit Board Guidelines." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 60ns. Settling time measurements for the OPA628 were performed in the circuit configuration of Figure 5. A sampling oscilloscope was used with signal averaging.

CAPACITIVE LOADS

Capacitive loads will decrease the OPA628's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω , in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

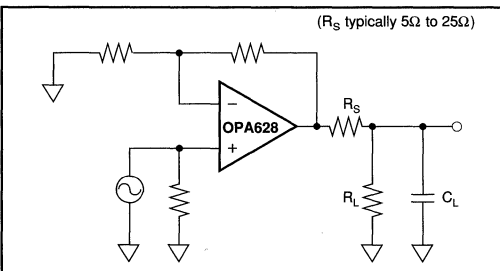


FIGURE 4. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA628 is internally compensated and is stable in unity gain with a phase margin of approximately 60° . However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of $-1/V$ is equivalent to a noise gain of $2V/V$.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA628 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

THERMAL CONSIDERATIONS

The OPA628 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 6.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 32mA = 320mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage (V_{OUT}) the maximum value of P_{DL} occurs at $V_{OUT} = V_{CC}/2$, and is equal to $P_{DL, max} = (V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 180mA = 900mW$. Thus, $P_D, max = 320mW + 900mW \approx 1.2W$. Note that the short-circuit condition represents the maximum

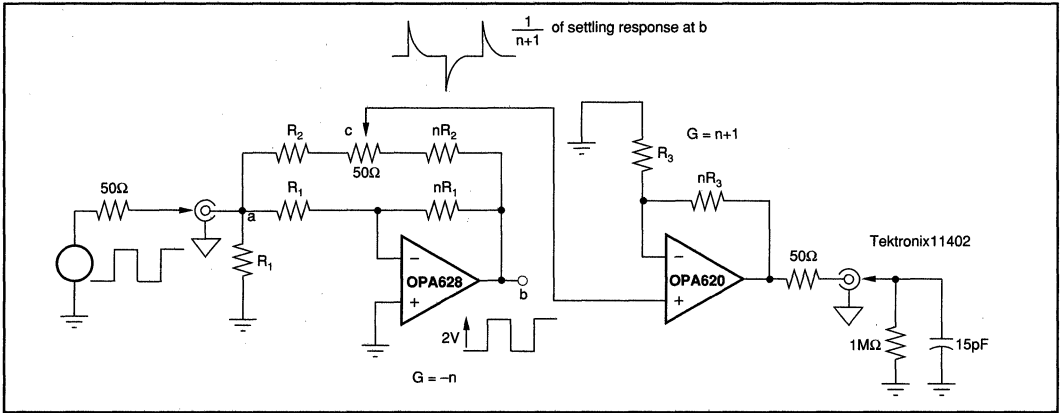


FIGURE 5. Settling Time Test Circuit.

amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1.2W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA} , of each package. The variation of short-circuit current with temperature is shown in Figure 7.

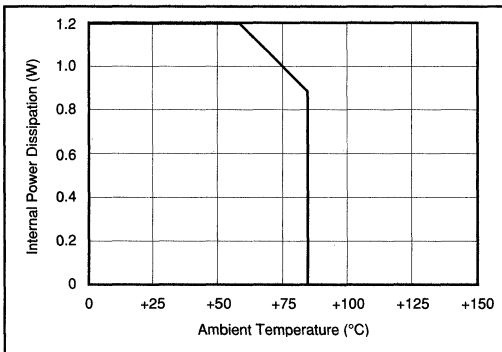


FIGURE 6. Maximum Power Dissipation.

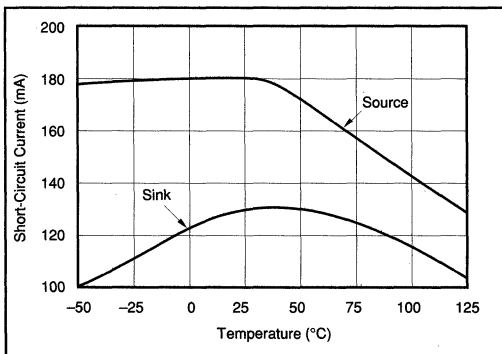


FIGURE 7. Short-Circuit Current vs Temperature.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA628 incorporates on-chip ESD protection diodes as shown in Figure 8. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

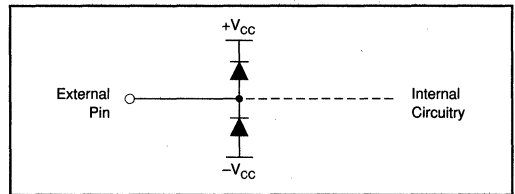


FIGURE 8. Internal ESD Protection.

All pins on the OPA628 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

OFFSET VOLTAGE ADJUSTMENT

The OPA628's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 9 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match

the impedance seen by both inputs as is shown with R_3 . This will reduce error due to the amplifier's input bias current.

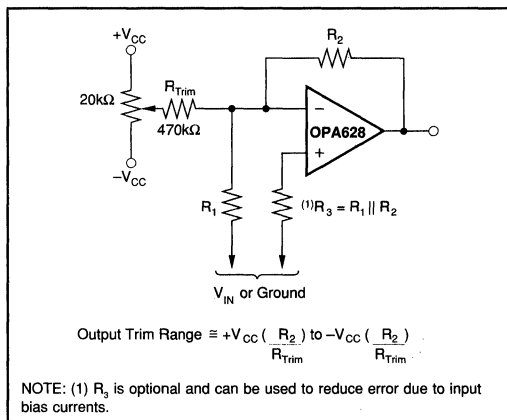


FIGURE 9. Offset Voltage Trim.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA628. Contact Burr-Brown Applications Department to receive a SPICE diskette.

RELIABILITY DATA

Reliability reports are available upon request for each of the package options offered.

DEMONSTRATION BOARDS

Contact Burr-Brown Applications Department for availability of demonstration boards for the OPA628. There are separate demonstration boards for the DIP and SOIC packages. These demonstration boards use the PC board layouts shown in Figures 10a and 10b. They are carefully designed for optimum low distortion performance as described in the wiring precaution section.

PRINTED CIRCUIT BOARD GUIDELINES

The printed circuit board layout is critical to obtaining the full performance of the OPA628, particularly optimum distortion and gain flatness. The guidelines below should be employed to design the OPA628 printed circuit board. Conceptual layouts illustrating these guidelines for the DIP and SOIC packages are shown in Figures 10a and 10b.

1. Establish the primary ground plane on the IC side of the pc board. The primary ground plane is the lowest impedance ground plane, it should be as wide as possible with minimal interruptions. Connect all unused space on both sides of the board to the ground plane. The ground plane should extend beneath the body of the IC on **both** sides of the board. A 2-ounce copper ground plane is recommended. The input signal ground return, the load return, and the power supply common should all be connected to the same physical point to avoid ground loops which can cause unwanted feedback.

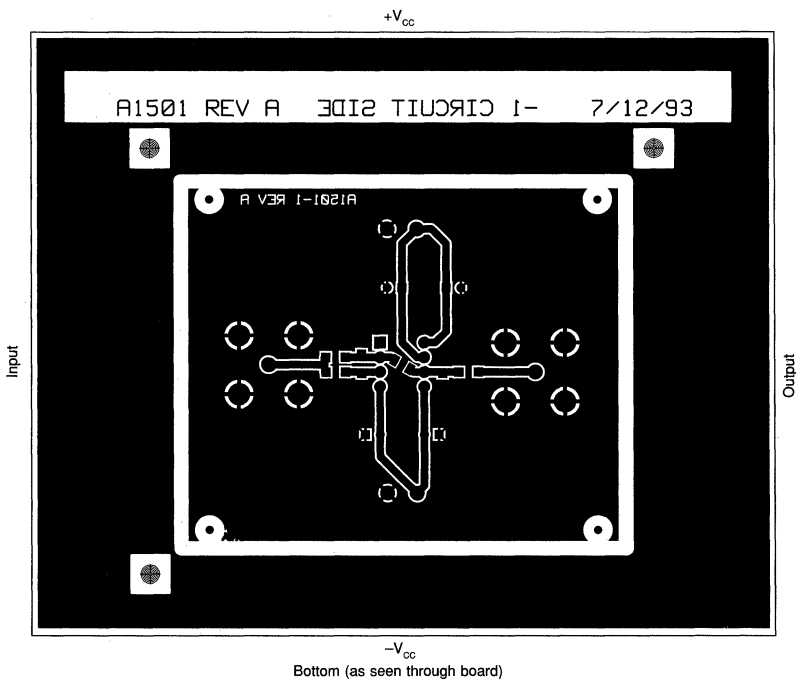
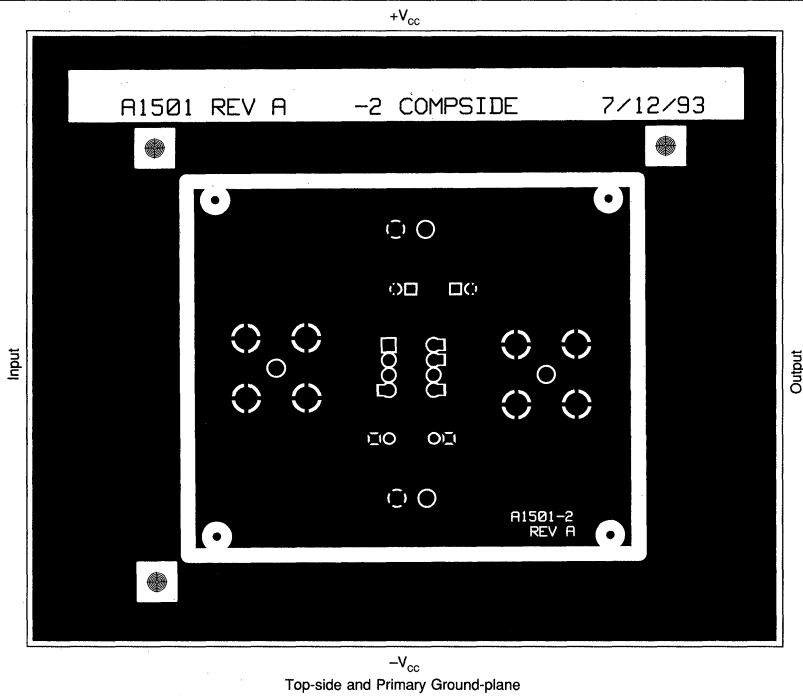
2. The entire physical circuit should be as small as practical. All signal and power supply paths should be as short and direct as possible to minimize stray capacitance and inductance which are detrimental to high frequency performance. Minimize signal trace impedance by keeping traces as wide and short as possible. Stray capacitance should be minimized, especially at high impedance nodes such as the amplifier's input terminals. In addition, stray signal coupling from the output of the amplifier back to the input should be minimized.

3. In general, the use of surface mount components improves performance over through-hole components by minimizing parasitics. (However, it should be noted that use of the DIP version of the OPA628 will not compromise amplifier performance.) If circuit elements with leads are used, the leads should be kept as short as possible (6mm) to minimize lead inductance. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1,000Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load.

4. As with any low distortion, wide bandwidth amplifier, power supply bypassing is extremely critical and must always be used. The system power supplies should be well bypassed at the board level with a minimum of 2.2μF tantalum capacitors. In addition, all four power supply leads should be locally bypassed to ground as close as possible to the amplifier pins. Surface mount 0.1μF capacitors will provide the best performance for local bypassing. Johanson 0.1μF capacitors (part number 250R18B104ZP4W) are used on the OPA628 demonstration board. All power supply bypass capacitors should be low impedance designs and should be located on the primary ground plane side of the pc board for the lowest impedance connection to ground. Properly bypassed and modulation free power supply lines allow optimum amplifier performance.

5. The OPA628 should be soldered directly into the pc board for best performance.

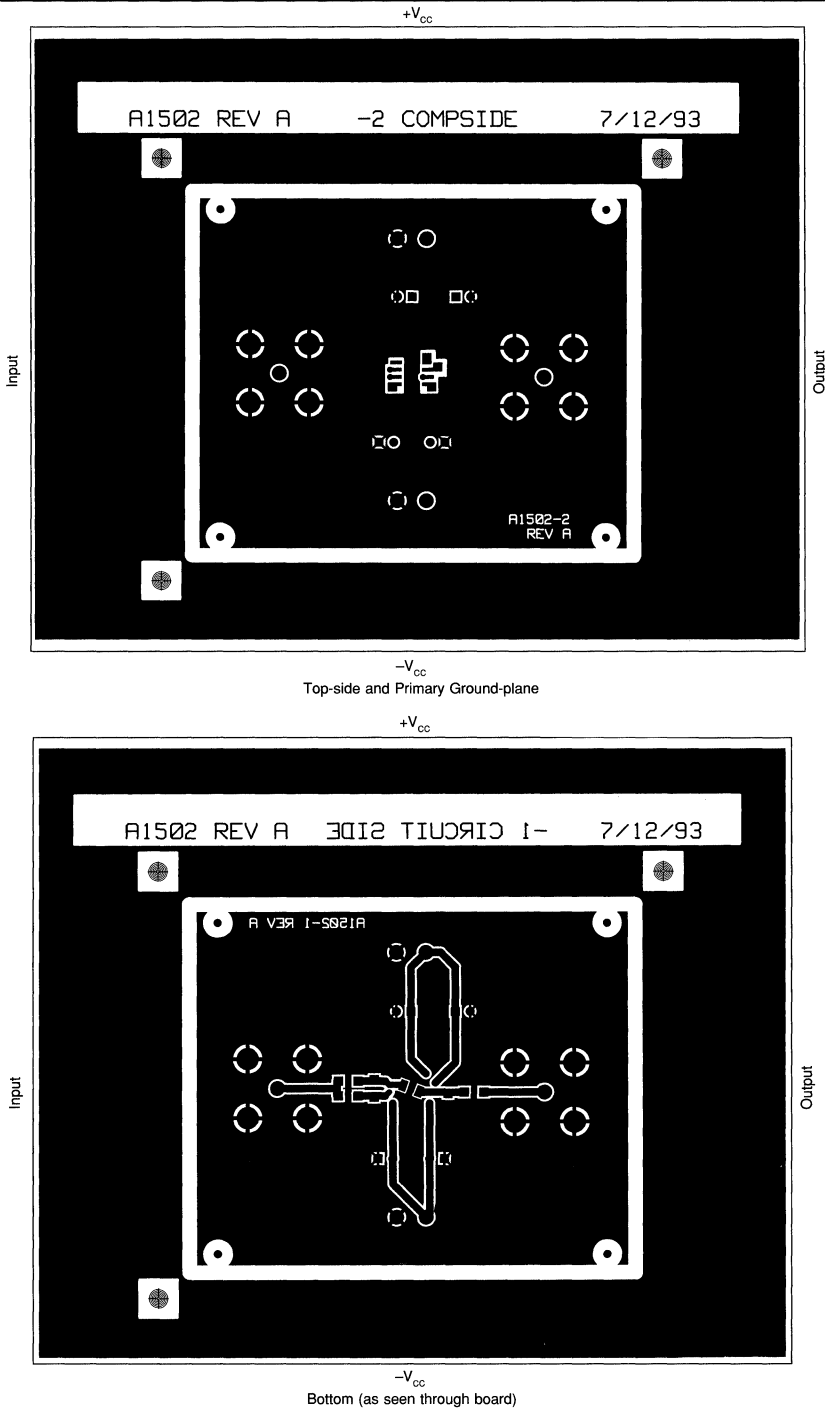
For Immediate Assistance, Contact Your Local Salesperson



NOTES: (1) Pin 1 designated by rectangular pad. (2) DUT inserted Top-side. (3) Power supply by-pass caps installed at pin locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both-sides.

FIGURE 10a. Conceptual PCB Layout (8-pin DIP).

Or, Call Customer Service at 1-800-548-6132 (USA Only)



NOTES: (1) Pad 1 designated by smallest rectangle. (2) DUT installed Top-side. (3) Power supply by-pass caps installed at pad locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both sides.

FIGURE 10b. Conceptual PCB Layout (8-pin SOIC).

APPLICATIONS

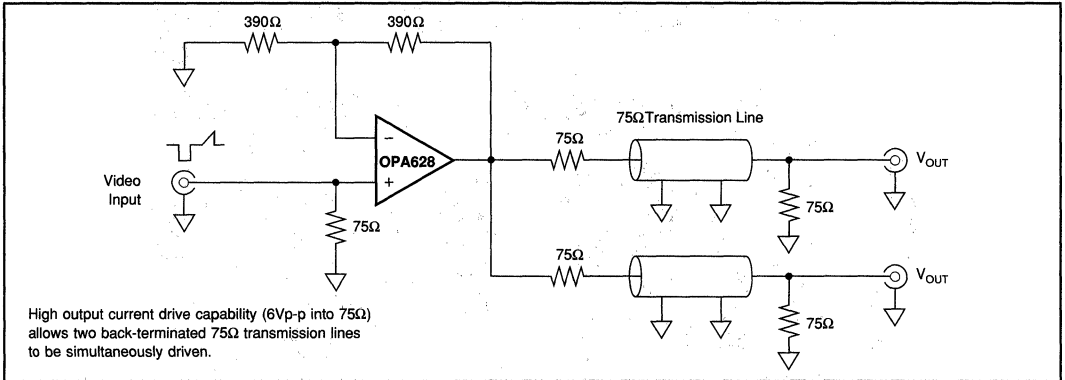


FIGURE 11. Video Distribution Amplifier.

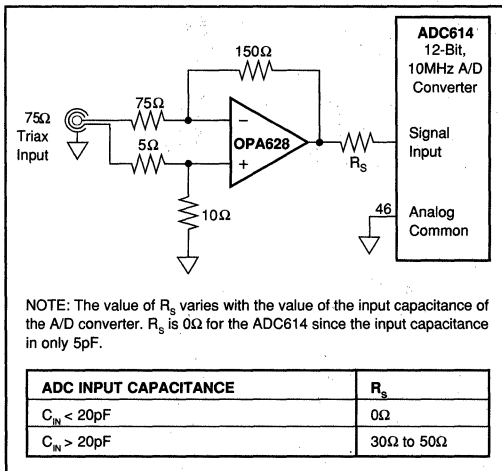


FIGURE 12. Differential Input Buffer Amplifier ($G = 2V/V$).

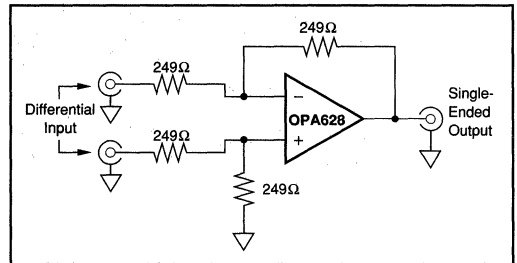
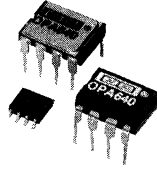


FIGURE 13. Low Distortion Unity Gain Difference Amplifier.

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OPA640

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY-GAIN BANDWIDTH: 1.3GHz
- UNITY-GAIN STABLE
- LOW NOISE: $2.9\text{nV}/\sqrt{\text{Hz}}$
- LOW HARMONICS: -75dBc at 10MHz
- HIGH COMMON MODE REJECTION: 85dB
- HIGH SLEW RATE: $350\text{V}/\mu\text{s}$

APPLICATIONS

- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- DIFFERENTIAL AMPLIFIER
- ACTIVE FILTERS

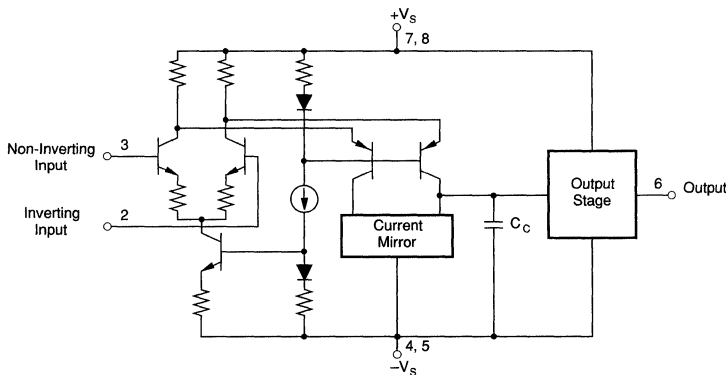
DESCRIPTION

The OPA640 is an extremely wideband operational amplifier featuring low noise, high common mode rejection and high spurious free dynamic range.

The OPA640 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier

circuit architecture. This allows the OPA640 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF and video applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1179B

2.221

OPA640

2

OPERATIONAL AMPLIFIERS

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA640H, P, U			OPA640HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Average Drift, HSQ Grade Over Temperature Power Supply Rejection (+V _S) (-V _S)	V _S = ±4.5 to ±5.5V		±2.0	±5		1.0	±2.0	mV
			±10			±6		μV/°C
			60	75	*	±3.0	±5	mV
			53	60	*	*		dB
INPUT BIAS CURRENT ⁽¹⁾ Input Bias Current Over Specified Temperature HSQ Grade Over Temperature Input Offset Current Over Specified Temperature HSQ Grade Over Temperature	V _{CM} = 0V		15	25		*	*	μA
			30	75		18	55	μA
	V _{CM} = 0V		0.3	2.0		20	75	μA
			0.5	2.5		*	1.0	μA
NOISE Input Voltage Noise Density f = 100Hz f = 10kHz f = 1MHz f = 1MHz to 500MHz Voltage Noise, BW = 100Hz to 500MHz Input Bias Current Noise Density f = 0.1Hz to 20kHz Noise Figure (NF) R _S = 1kΩ R _S = 50Ω			7.0		*		nV/√Hz	
			2.8		*		nV/√Hz	
			2.8		*		nV/√Hz	
			2.9		*		nV/√Hz	
			65		*		μVrms	
			2.0		*		ρA/√Hz	
			2.6		*		dB	
			10.9		*		dB	
	INPUT VOLTAGE RANGE Common-Mode Input Range Over Temperature Common-Mode Rejection	V _{CM} = ±0.5V		±2.5	±2.85	*	*	V
				±2.5	±2.75	*	*	V
			70	85	80	88	dB	
INPUT IMPEDANCE Differential Common-Mode			15 1		*		kΩ pF	
			2 1		*		MΩ pF	
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Over Specified Temperature	V _O = ±2V, R _L = 100Ω V _O = ±2V, R _L = 100Ω		50	57	53	*	dB	
			45	55	*	*	dB	
FREQUENCY RESPONSE, R_{FB} = 402Ω Closed-Loop Bandwidth Slew Rate ⁽²⁾ At Minimum Specified Temperature Settling Time 0.01% 0.1% 1% Spurious Free Dynamic Range Gain Flatness to 0.1dB Differential Gain at 3.58MHz, G = +2V/V Differential Phase at 3.58MHz, G = +2V/V	All Four Power Pins Used		1.3		*	*	GHz	
		Gain = +1V/V	280		*	*	MHz	
		Gain = +2V/V	65		*	*	MHz	
		Gain = +5V/V	31		*	*	MHz	
		Gain = +10V/V	350		*	*	V/μs	
		G = +1, 2V Step	285		*	*	V/μs	
		G = +1, 2V Step	22		*	*	ns	
		G = +1, 2V Step	18		*	*	ns	
		G = +1, 2V Step	4.5		*	*	ns	
		G = +1, f = 5MHz, V _O = 2Vp-p	85		*	*	dBc	
		G = +1, f = 10MHz, V _O = 2Vp-p	75		*	*	dBc	
		G = +1, f = 20MHz, V _O = 2Vp-p	65		*	*	dBc	
		G = +1 or +2	120		*	*	MHz	
		V _O = 0V to 1.4V, R _L = 150Ω	0.07		*	*	%	
V _O = 0V to 1.4V, R _L = 150Ω	0.008		*	*	Degrees			
OUTPUT Voltage Output Over Specified Temperature HSQ Grade Over Temperature Voltage Output Over Specified Temperature HSQ Grade Over Temperature Current Output, +25°C Over Specified Temperature HSQ Grade Over Temperature Short Circuit Current Output Resistance	No Load		±2.6	±3.0	*	*	V	
						±2.5	±2.8	V
	R _L = 100Ω		±2.25	±2.5	*	*	V	
			±40	±52	±2.0	±2.25	V	
		±25	±45	*	*	mA		
				±25	±35	*	mA	
				75	*	*	mA	
		1MHz, G = +1V/V		0.2		*	Ω	

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA640H, P, U			OPA640HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}	± 4.5	± 5	± 5.5	*	*	*	V
Operating Voltage Range	T_{MIN} to T_{MAX}		± 18	± 22		*	*	V
Quiescent Current			± 19	± 24		*	*	mA
Over Specified Temperature						*	*	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	-40		+85	*		*	$^\circ\text{C}$
HSQ	Ambient				-55		+125	$^\circ\text{C}$
Thermal Resistance	θ_{JA} , Junction to Ambient							$^\circ\text{C}/\text{W}$
P			120			*		$^\circ\text{C}/\text{W}$
U			170			*		$^\circ\text{C}/\text{W}$
H			120			*		$^\circ\text{C}/\text{W}$

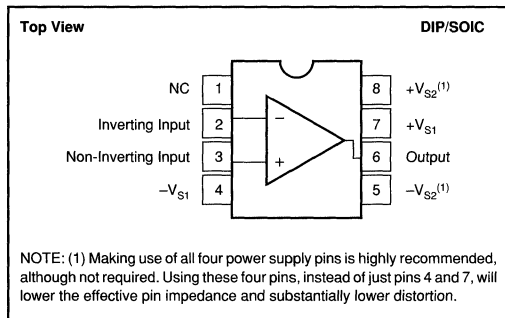
NOTE: (1) Slow rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

Basic Model Number	OPA640	()	()	(Q)
Package Code				
H = 8-pin Sidebraze DIP				
P = 8-pin Plastic DIP				
U = 8-pin Plastic SOIC				
Performance Grade Code				
S = -55°C to $+125^\circ\text{C}$				
B ⁽¹⁾ or No Letter = -40°C to $+85^\circ\text{C}$				
Reliability Screening				
Q = Q-Screened (HSQ Model Only)				

NOTE: (1) The "B" grade of the SOIC package will be designated with a dot. Refer to the mechanical section for the location.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 5.5\text{VDC}$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65°C to $+150^\circ\text{C}$
P, PB, U, UB	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
(soldering, SOIC 3s)	$+260^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA640H, HSQ	8-Pin Sidebraze DIP	157
OPA640P, PB	8-Pin DIP	006
OPA640U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

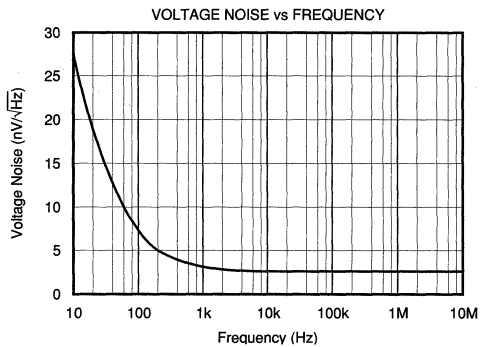
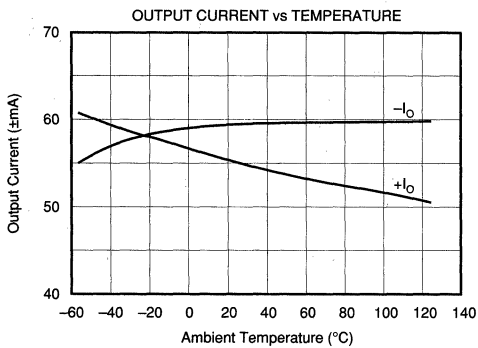
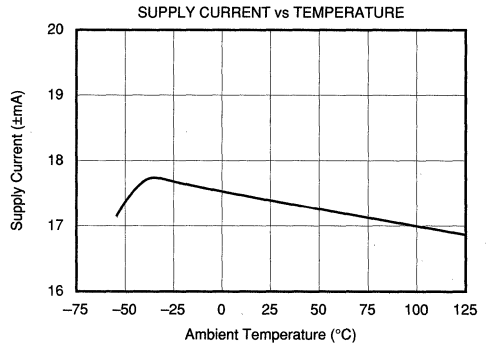
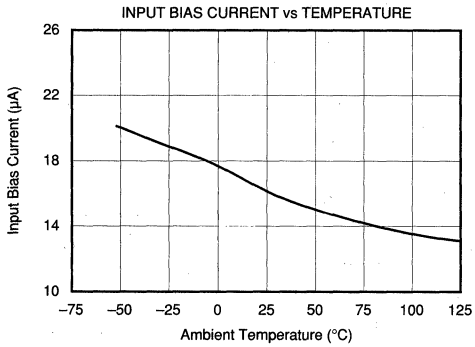
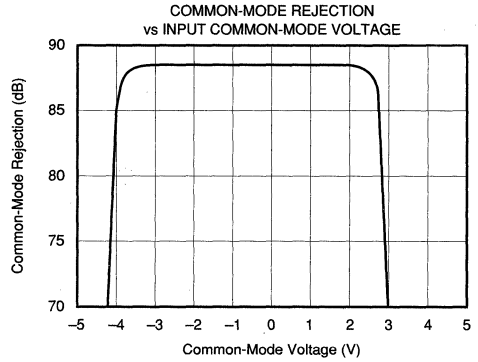
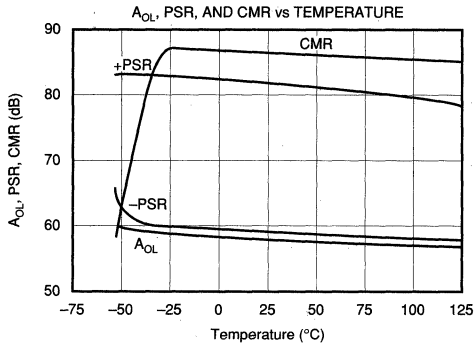
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

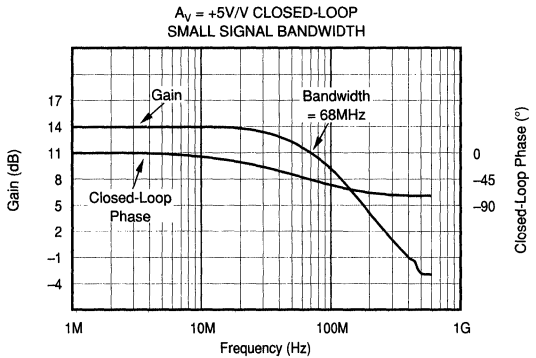
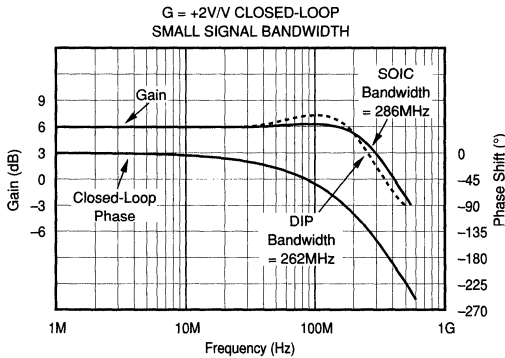
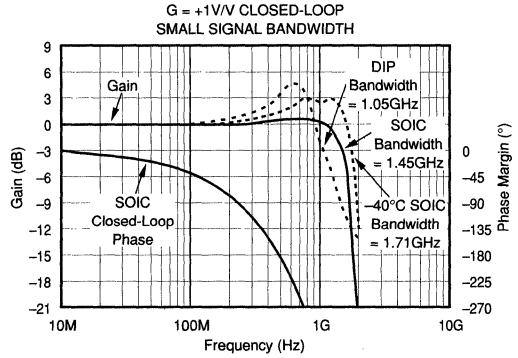
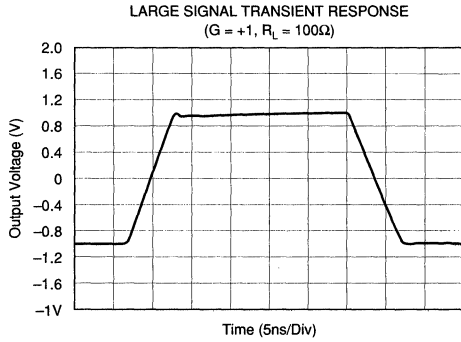
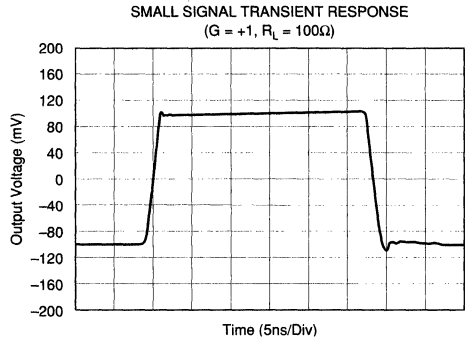
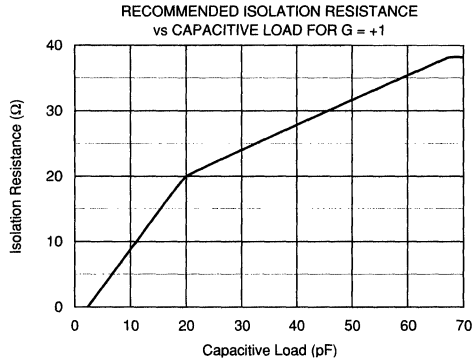
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Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

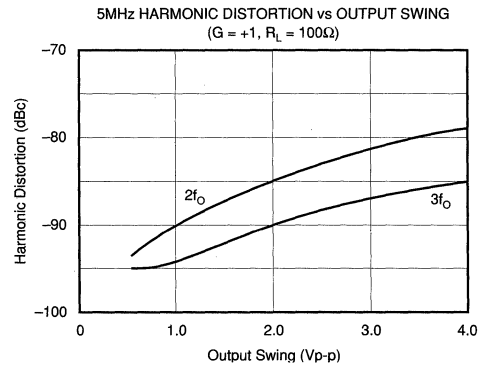
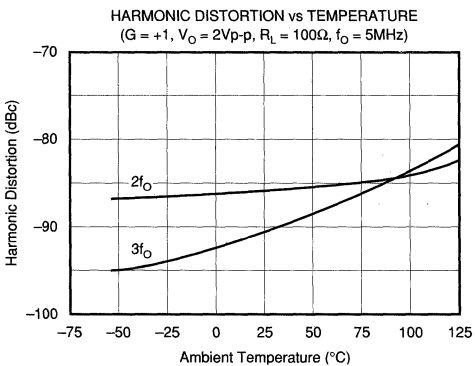
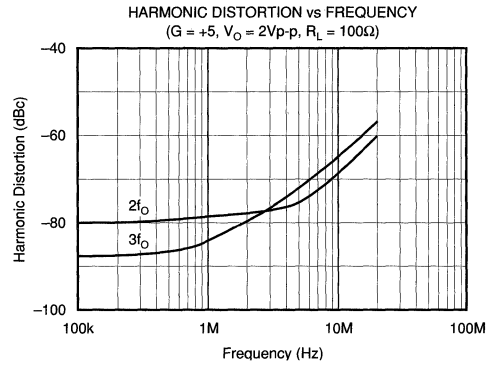
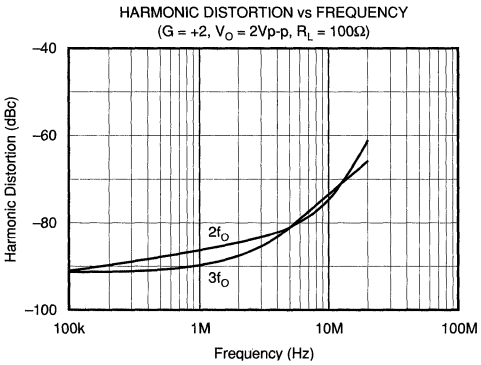
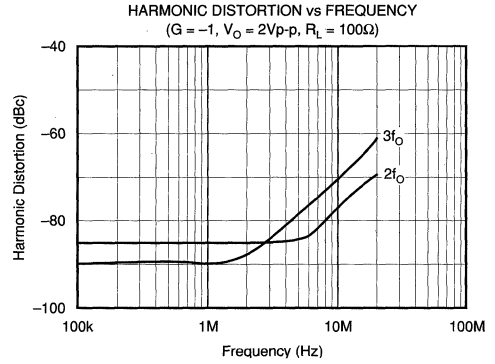
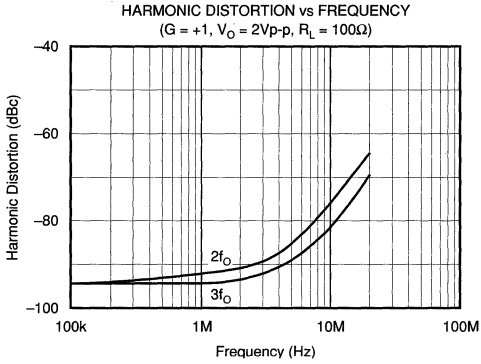
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For Immediate Assistance, Contact Your Local Salesperson

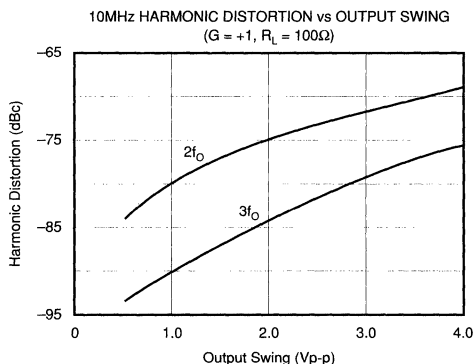
TYPICAL PERFORMANCE CURVES (CONT)

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA640 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA640's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA640's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA640.

WIRING PRECAUTIONS

Maximizing the OPA640's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and

instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA640, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μF) with very short leads are recommended. A parallel 0.01 μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separate traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors on the top side of the PC board is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the DEM-OPA64X data sheet for the recommended layout and component placements.
- 2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 4) Whenever possible, solder the OPA640 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.
- 5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**
- 6) Due to the extremely high bandwidth of the OPA640, the SOIC package is strongly recommended due its low parasitic impedance. The parasitic impedance in the PDIP and CERDIP packages causes the OPA640 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SOIC package in unity-gain. The gain peaking in the PDIP and CERDIP packages is minimized in gains of 2 or greater, however. Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are also strongly recommended.

- 7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.
- 8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and -5.2V, use of $\pm 15V$ supplies will destroy the part.
- 9) Standard commercial test equipment has not been designed to test devices in the OPA640's speed range. Bench-top amp testers and ATE systems will require a special test head to successfully test these amplifiers.
- 10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- 11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

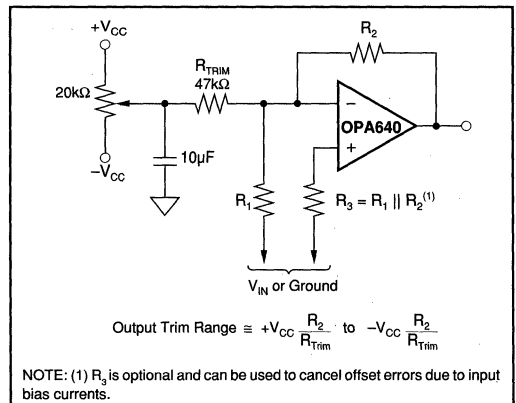


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA640 incor-

porates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

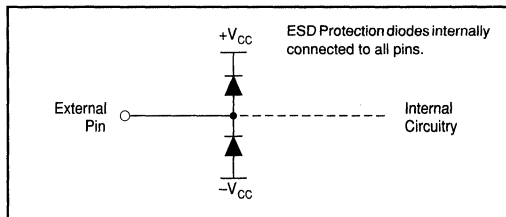


FIGURE 2. Internal ESD Protection.

All pins on the OPA640 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA640 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA640.

OUTPUT DRIVE CAPABILITY

The OPA640 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA640 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA640 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

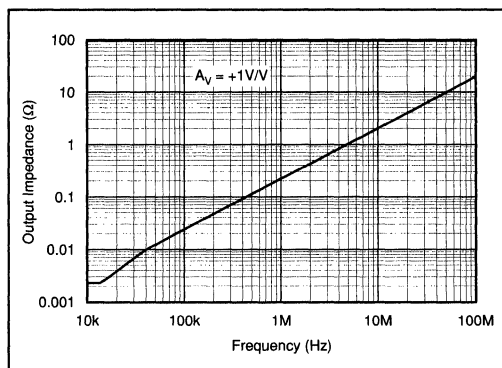


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA640 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 22mA = 220mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

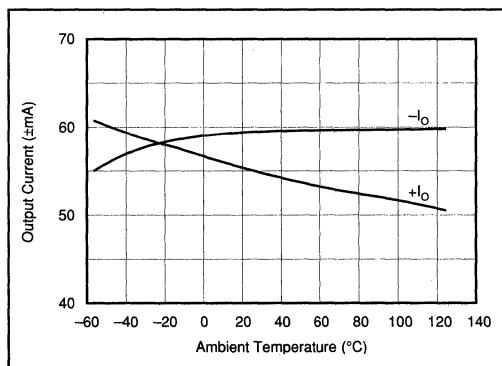


FIGURE 4. Output Current vs. Temperature.

CAPACITIVE LOADS

The OPA640's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 2pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

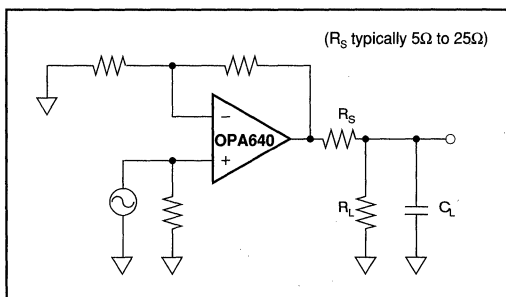


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA640 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of $-1V/V$ is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA640 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and

closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu V$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA640 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 35ns.

In practice, settling time measurements on the OPA640 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA640's Harmonic Distortion characteristics vs frequency and power output are shown in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance. Refer to Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

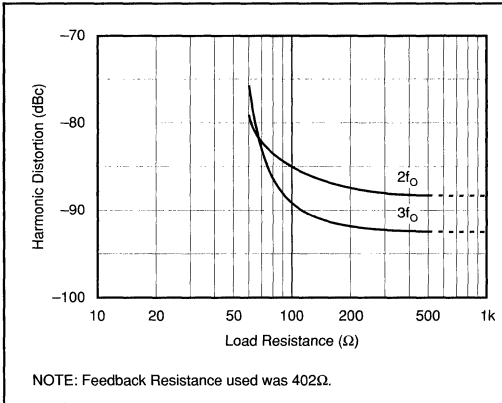


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 7 shows the OPA640's single tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA640 to operate in a gain of +1V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 11 we find that the intercept point is +47dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_o)$$

where OPI³P = third-order intercept, dBm
 P_o = output level, dBm

For this case OPI³P = 47dBm, P_o = 47dBm, and the third Harmonic = 2(47 - 10) = 74dB below the fundamental tone. The OPA640's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

The value for the two-tone, third-order intercept is typically 8dB lower than the single tone value.

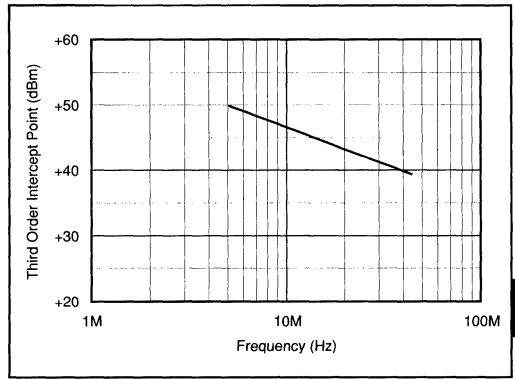


FIGURE 7. Single-Tone, 3rd Order Intercept Point vs Frequency.

NOISE FIGURE

The OPA640 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA640's Noise Figure vs Source Resistance is shown in Figure 8.

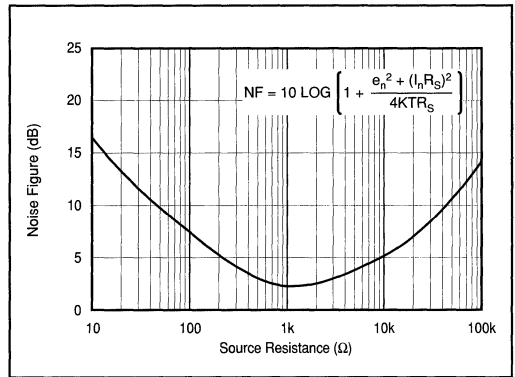


FIGURE 8. Noise Figure vs Source Resistance.

For Immediate Assistance, Contact Your Local Salesperson

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown “Q-Screening” provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate <math> < 5 \times 10^{-8}</math> atm cc/s, 30PSiG Gross: Perfluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on the HS package only.

APPLICATIONS

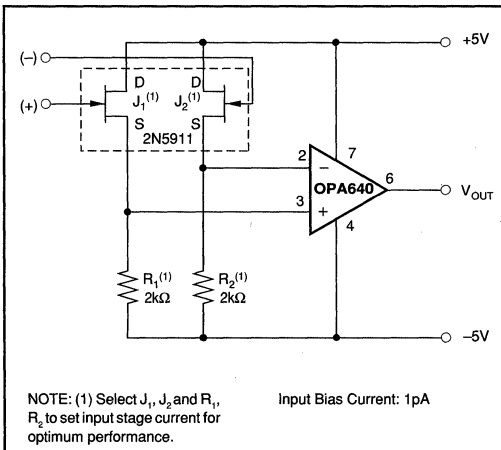


FIGURE 9. Low Noise, Wideband FET Input Op Amp.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA640. Contact Burr-Brown Applications Department to receive a spice diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x data sheet for details.

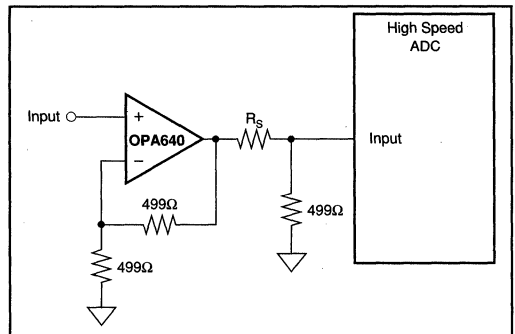


FIGURE 10. Differential Input Buffer Amplifier ($G = +2V/V$).

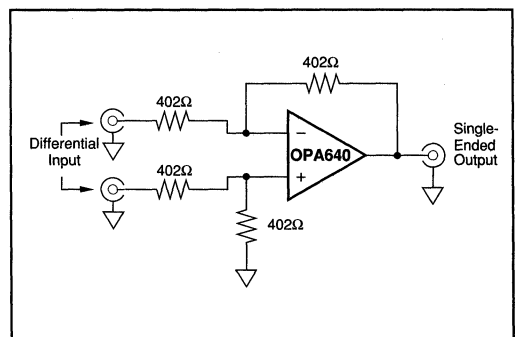


FIGURE 11. Unity Gain Difference Amplifier.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

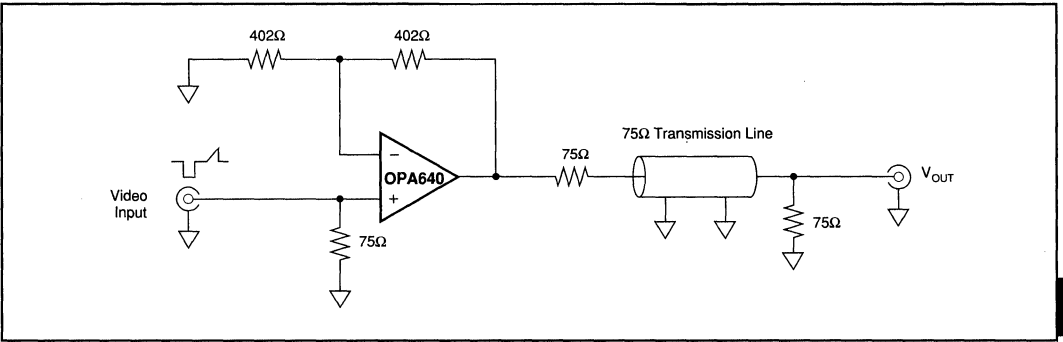


FIGURE 12. Video Gain Amplifier.

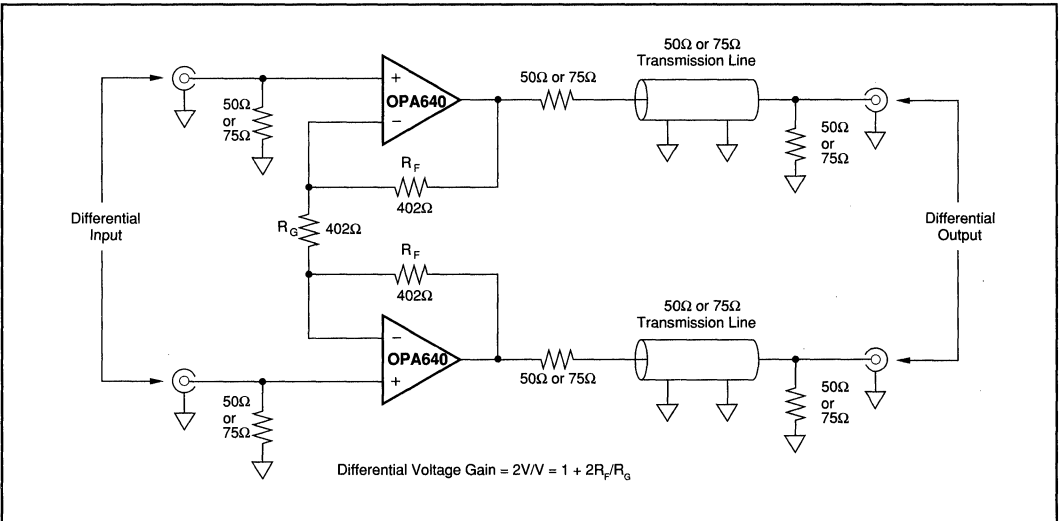


FIGURE 13. Differential Line Driver for 50Ω or 75Ω Systems.

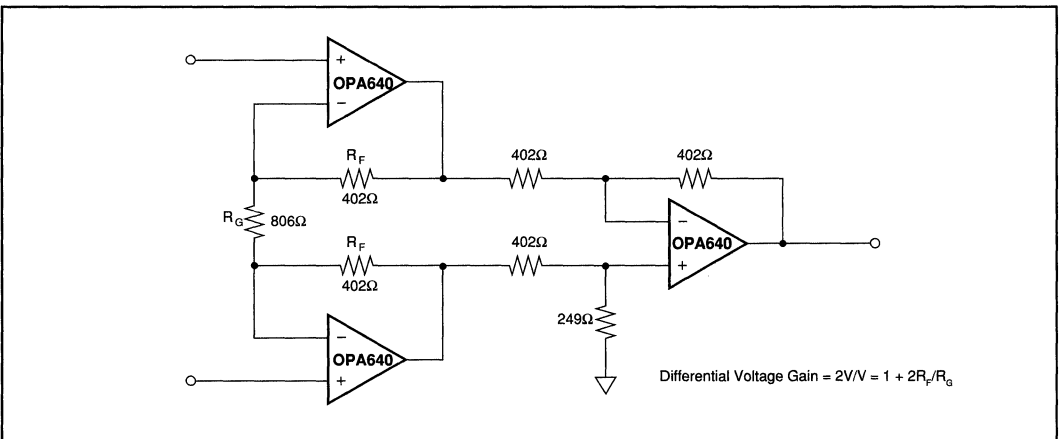
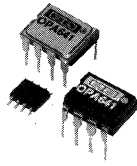


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier.



OPA641

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- GAIN-BANDWIDTH: 1.6GHz
- STABLE IN GAINS ≥ 2
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.015%/0.006°
- HIGH SLEW RATE: 650V/ μ s
- FAST 12-BIT SETTLING: 18ns (0.01%)
- HIGH COMMON MODE REJECTION: 80dB
- LOW HARMONICS: -72 dBc at 10MHz

APPLICATIONS

- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- ACTIVE FILTERS

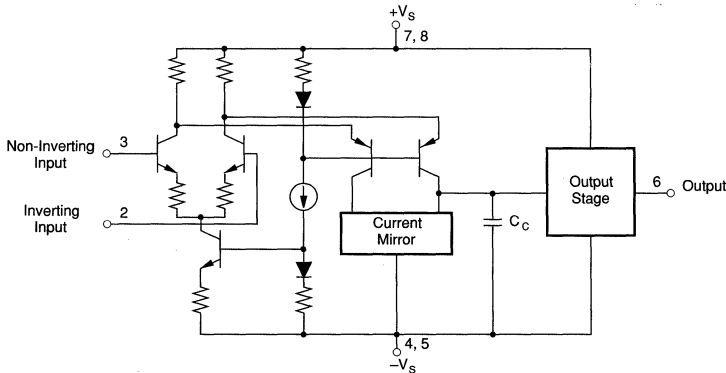
DESCRIPTION

The OPA641 is an extremely wideband operational amplifier featuring low noise, high slew rate and high spurious free dynamic range.

The OPA641 is conservatively compensated for stability in gains of 2 or greater. This amplifier has a fully symmetrical differential input due to its "classical"

operational amplifier circuit architecture. This allows the OPA641 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF, video, and imaging applications.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			± 2	± 6		± 1	± 2	mV
Average Drift			± 10			± 6		$\mu\text{V}/^\circ\text{C}$
HSQ Grade Over Temperature						± 3	± 6	mV
Power Supply Rejection ($+V_S$)	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$	56	79		61	82		dB
Power Supply Rejection ($-V_S$)		51	58		54	60		dB
INPUT BIAS CURRENT								
Input Bias Current	$V_{CM} = 0\text{V}$		13	30		*	*	μA
Over Specified Temperature			20	90		*	*	μA
HSQ Grade Over Temperature						30	75	μA
Input Offset Current	$V_{CM} = 0\text{V}$		0.2	2		*	1.0	μA
Over Specified Temperature			0.5	2.5		*	2.0	μA
HSQ Grade Over Temperature						1.2	4.0	μA
NOISE								
Input Voltage Noise								
Noise Density, $f = 100\text{Hz}$			8.0			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			2.9			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$			2.8			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$ to 500MHz			2.8			*		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise, $\text{BW} = 100\text{Hz}$ to 500MHz			63			*		μVrms
Input Bias Current Noise Density								
$f = 0.1\text{Hz}$ to 20kHz			2.0			*		$\text{pA}/\sqrt{\text{Hz}}$
Noise Figure (NF)								
$R_S = 1\text{k}\Omega$			4			*		dB
$R_S = 50\Omega$			13			*		dB
INPUT VOLTAGE RANGE								
Common-mode Input Range		± 2.5	± 2.85		*	*		V
Over Specified Temperature		± 2.5	± 2.75		*	*		V
Common-mode Rejection	$V_{CM} = \pm 0.5\text{V}$	56	78		65	80		dB
INPUT IMPEDANCE								
Differential			15 1			*		$\text{k}\Omega$ pF
Common-Mode			2 1			*		$\text{M}\Omega$ pF
OPEN-LOOP GAIN, DC								
Open-loop Voltage Gain	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	50	58		53	61		dB
Over Specified Temperature	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	45	56		48	*		dB
FREQUENCY RESPONSE, $R_{FB} = 402\Omega$								
Closed Loop Bandwidth	All Four Power Pins Used							
	Gain = $+2\text{V}/\text{V}$		800			*		MHz
	Gain = $+5\text{V}/\text{V}$		78			*		MHz
	Gain = $+10\text{V}/\text{V}$		39			*		MHz
Slew Rate ⁽¹⁾	$G = +2$, 2V Step		650			*		$\text{V}/\mu\text{s}$
At Minimum Specified Temperature	$G = +2$, 2V Step		550			*		$\text{V}/\mu\text{s}$
Settling Time: 0.01%	$G = +2$, 2V Step		18			*		ns
0.1%	$G = +2$, 2V Step		13			*		ns
1%	$G = +2$, 2V Step		5			*		ns
Differential Gain at 3.58MHz, $G = +2\text{V}/\text{V}$	$V_O = 0\text{V}$ to 1.4V , $R_L = 150\Omega$		0.015			*		%
Differential Phase at 3.58MHz, $G = +2\text{V}/\text{V}$	$V_O = 0\text{V}$ to 1.4V , $R_L = 150\Omega$		0.006			*		degrees
Gain Flatness	$G = +2$		0.1			*		MHz
Spurious Free Dynamic Range	$G = +2$, $f = 5\text{MHz}$, $V_O = 2\text{Vp-p}$		78			*		dBc
	$G = +2$, $f = 10\text{MHz}$, $V_O = 2\text{Vp-p}$		72			*		dBc
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		± 2.6	± 3.0		*	*		V
HSQ Grade Over Temperature					± 2.5	± 2.8		V
Voltage Output	$R_L = 100\Omega$							
Over Specified Temperature		± 2.25	± 2.5		*	*		V
HSQ Grade Over Temperature		± 2.0	± 2.3					
Current Output		± 40	± 55		*	*		mA
Over Specified Temperature		± 25	± 50		*	*		mA
HSQ Grade Over Temperature					± 25	± 50		mA
Short Circuit Current			75					mA
Output Resistance	1MHz, $G = +2\text{V}/\text{V}$		0.04			*		Ω

OPA641

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OPERATIONAL AMPLIFIERS

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SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}	± 4.5	± 5	± 5.5	*	*	*	V
Operating Voltage Range	T_{MIN} to T_{MAX}							V
Quiescent Current			± 15	± 22		*	*	mA
Over Specified Temperature			± 19	± 24		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	-40		+85	*		*	$^\circ\text{C}$
HSQ	Ambient				-55		+125	$^\circ\text{C}$
Thermal Resistance	θ_{JA} , Junction to Ambient							$^\circ\text{C/W}$
P			120			*		$^\circ\text{C/W}$
U			170			*		$^\circ\text{C/W}$
H			120			*		$^\circ\text{C/W}$

NOTE: (1) Slow rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

Basic Model Number	OPA641	()	()	(Q)
Package Code				
H = 8-pin Sidebraze DIP				
P = 8-pin Plastic DIP				
U = 8-pin Plastic SOIC				
Performance Grade Code				
S = -55°C to $+125^\circ\text{C}$				
B ⁽¹⁾ or No Letter = -40°C to $+85^\circ\text{C}$				
Reliability Screening				
Q = Q-Screened (HSQ Model Only)				

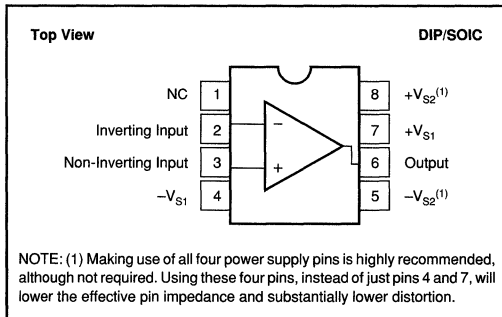
NOTE: (1) The "B" grade of the SOIC package will be designated with a "B". Refer to the mechanical section for the location.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 5.5\text{VDC}$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{DC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65°C to $+150^\circ\text{C}$
P, PB, U, UB	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
(soldering, SOIC 3s)	$+260^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA641H, HSQ	8-Pin Cerdip	157
OPA641P, PB	8-Pin DIP	006
OPA641U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

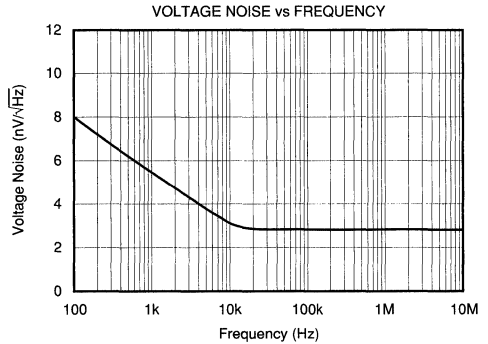
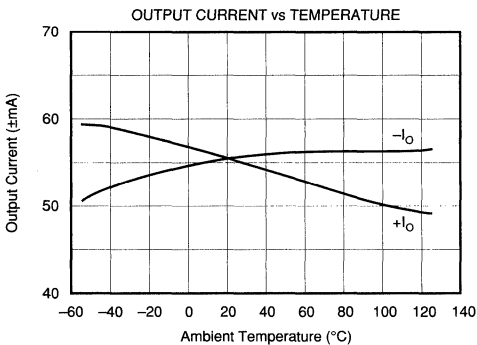
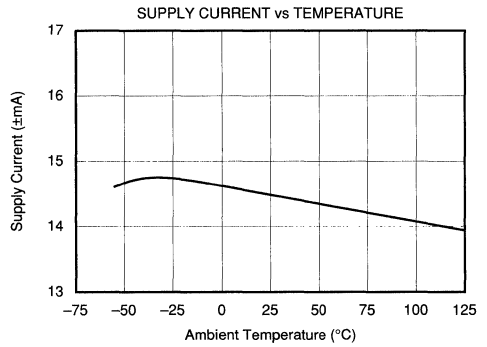
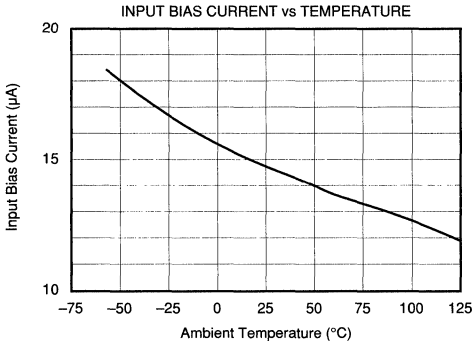
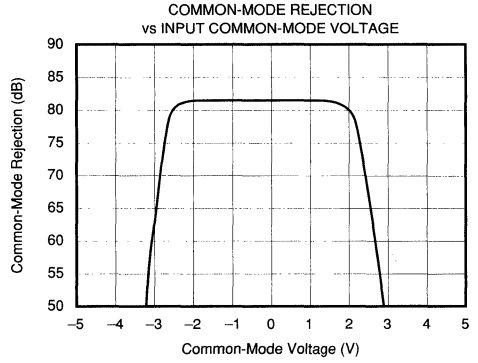
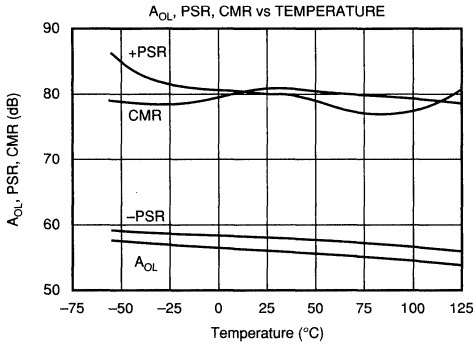
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.



OPA641

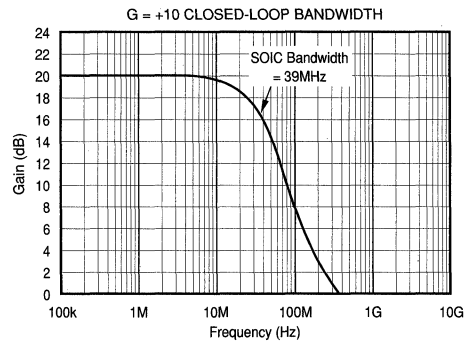
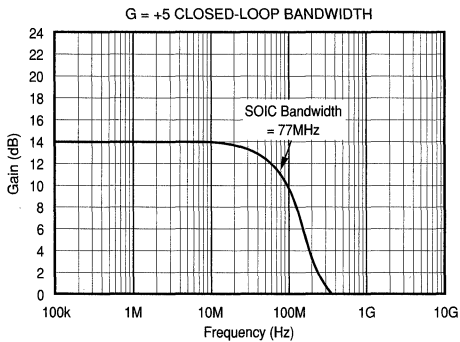
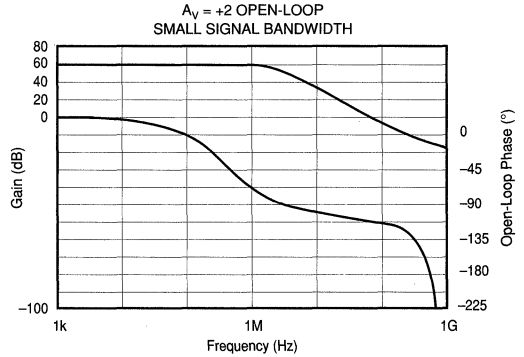
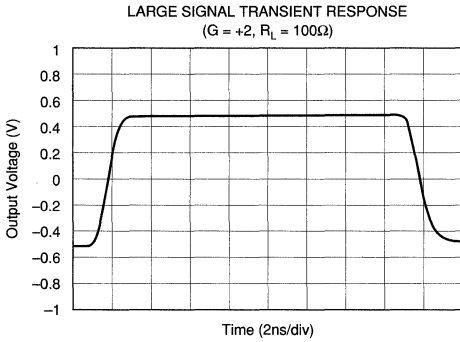
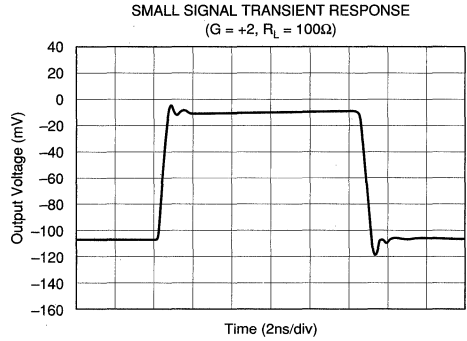
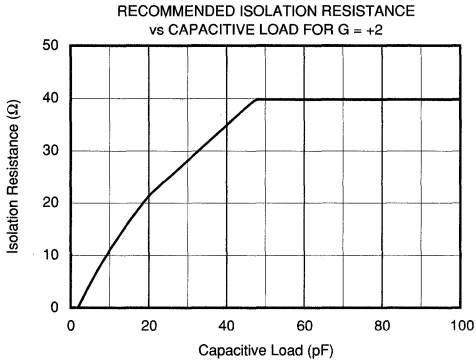
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OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

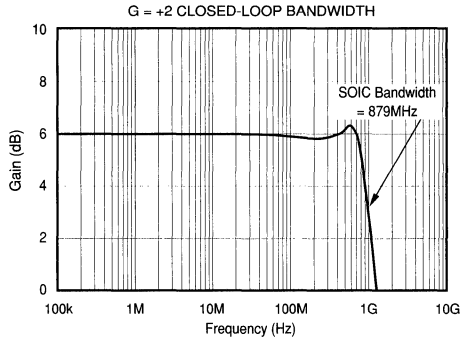
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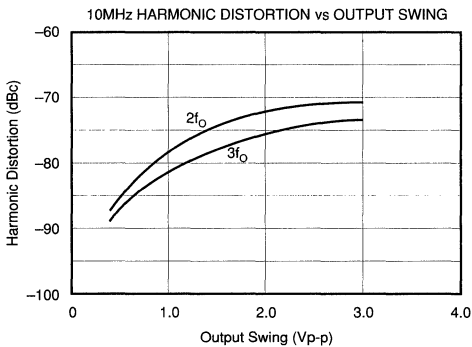
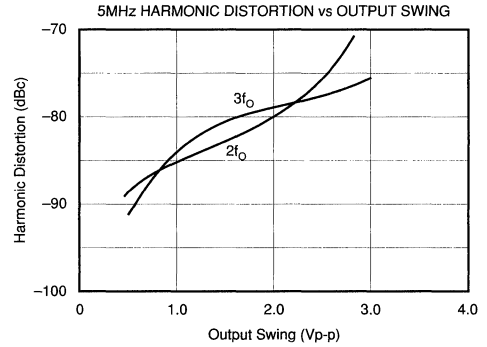
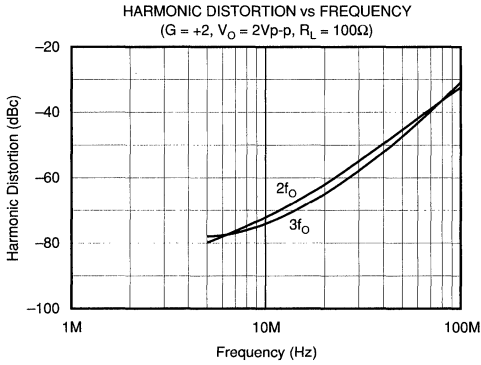
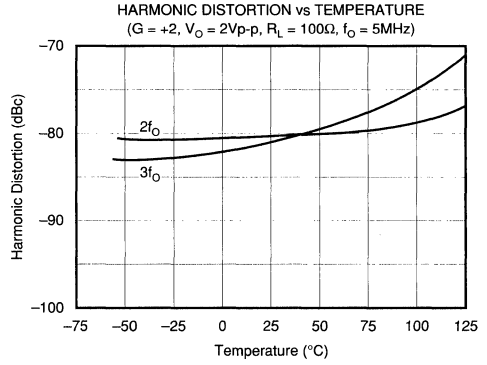
Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.



NOTE: Dip Bandwidth = 785MHz



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA641 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA641's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA641's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA641.

WIRING PRECAUTIONS

Maximizing the OPA641's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA641, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct

heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μ F) with very short leads are recommended. A parallel 0.01 μ F ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors on the top side of the PC board is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the DEM-OPA64x Datasheet for the recommended layout and component placement.
- 2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 3) Surface mount on the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 4) Whenever possible, solder the OPA641 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.
- 5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the

highest bandwidth. See the demonstration board layout at the end of the datasheet. A **longer feedback path than this will decrease the realized bandwidth substantially.**

6) Due to the extremely high bandwidth of the OPA641, the SOIC package is strongly recommended due its low parasitic impedance. The parasitic impedance in the PDIP and CERDIP packages causes the OPA641 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SOIC package in unity-gain. The gain peaking in the PDIP and CERDIP packages is minimized in gains of 4 or greater, however. Surface mount components (chip resistors, capacitors, etc.) also have low lead inductance and are therefore strongly recommended.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with $+5V$ and $-5.2V$, use of $\pm 15V$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA641's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with

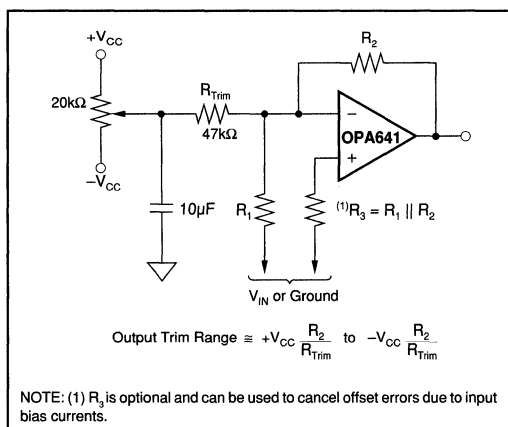


FIGURE 1. Offset Voltage Trim.

temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA641 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

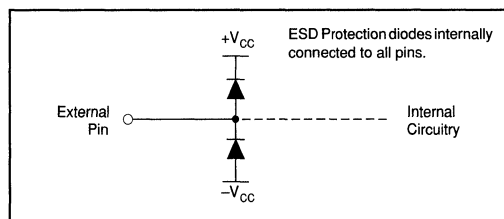


FIGURE 2. Internal ESD Protection.

All pins on the OPA641 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA641 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA641.

OUTPUT DRIVE CAPABILITY

The OPA641 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA641 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are needed.

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Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA641 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

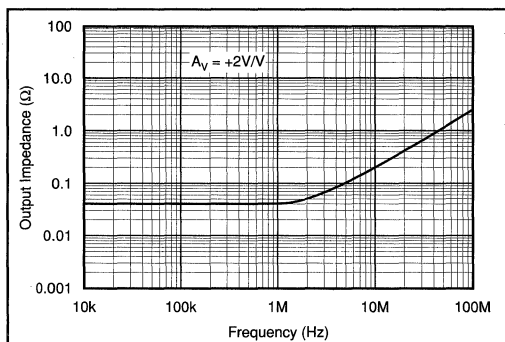


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA641 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 24mA = 240mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$), the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA641's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax

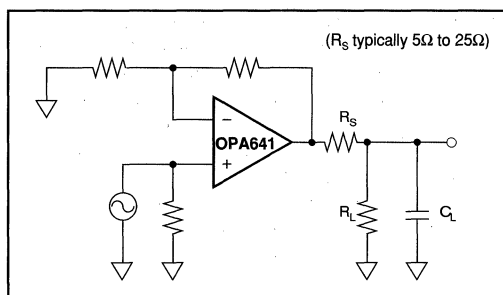


FIGURE 4. Driving Capacitive Loads.

cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA641 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of $-1V/V$ is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA641 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu V$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 18ns to 0.01% for a 2V step, making the OPA641 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA641 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 6 shows the test circuit used to measure settling time for the OPA641. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION AND NOISE

The OPA641's Harmonic Distortion characteristics vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance (refer to Figure 5). Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Although harmonic distortion may decrease with higher load resistances (i.e. higher feedback resistors), the effective output noise will increase due to the higher resistance. Therefore, noise or harmonic distortion may be optimized by picking the appropriate feedback resistor.

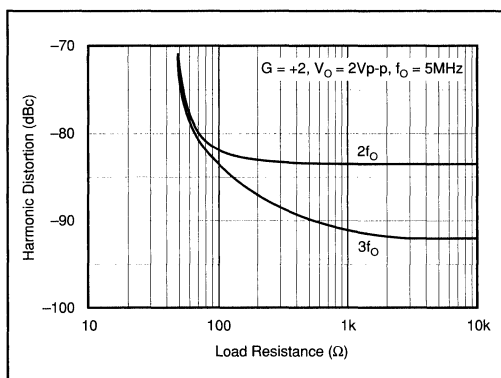


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 6 shows the OPA641's single-tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA641 to operate in a gain of +2V/V and drive 2Vp-p into 100Ω at a frequency of 5MHz. Referring to Figure 6 we find that the intercept point is +38dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OIP3P} - P_o)$$

where OIP3P = third-order output intercept, dBm
 P_o = output level/tone, dBm/tone

For this case OIP3P = 38dBm, P_o = 7dBm, and the third-Harmonic = $2(38 - 7) = 62$ dB below the fundamental tone. The OPA641's low IMD makes the device an excellent choice for a variety of RF signal processing applications. The value for the two-tone, third-order intercept is typically 6dB lower than the single-tone value.

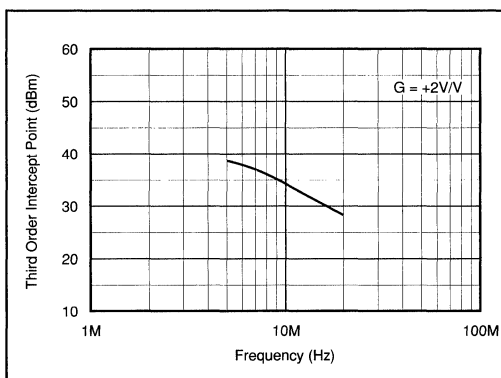


FIGURE 6. Single-Tone, Third Order Intercept Point vs Frequency.

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NOISE FIGURE

The OPA641 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA641's Noise Figure vs Source Resistance is shown in Figure 7.

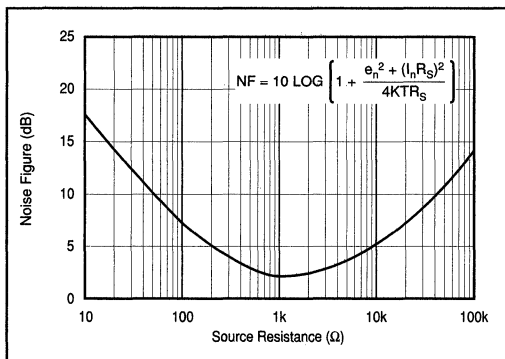


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA641. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 10 ⁻⁸ atm cc/s, 30PSiG Gross: Perfluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on the H5Q package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x Datasheet for details.

APPLICATIONS

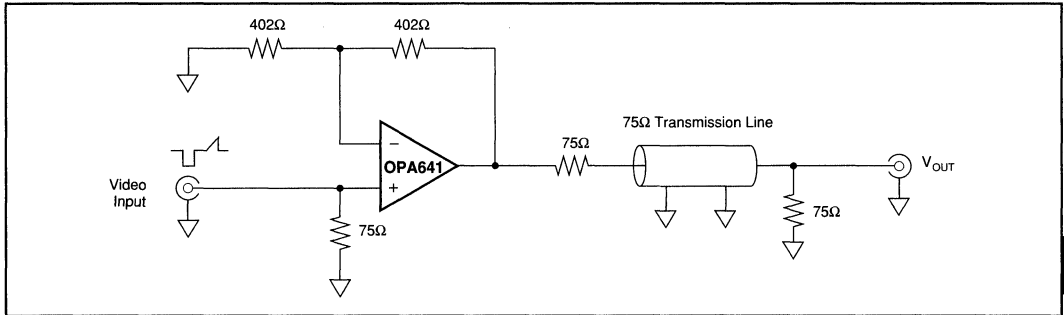


FIGURE 8. Video Gain Amplifier.

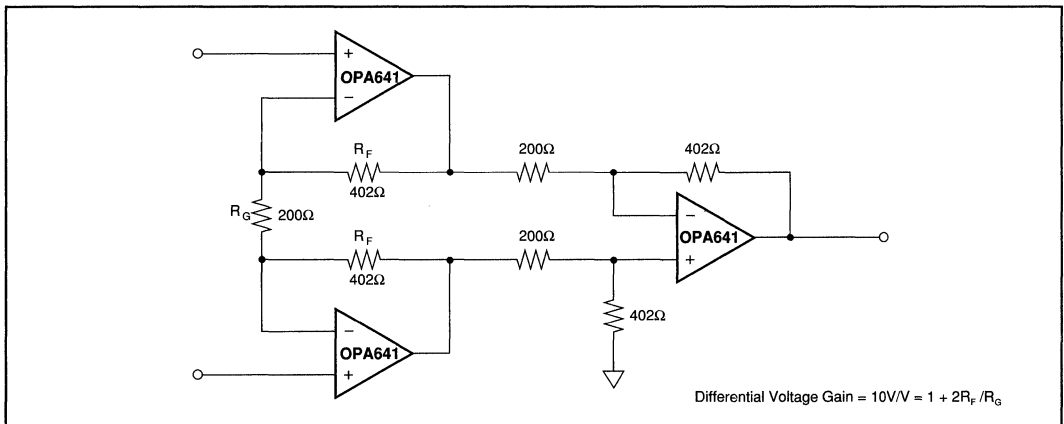


FIGURE 9. Wideband, Fast-Settling Instrumentation Amplifier.

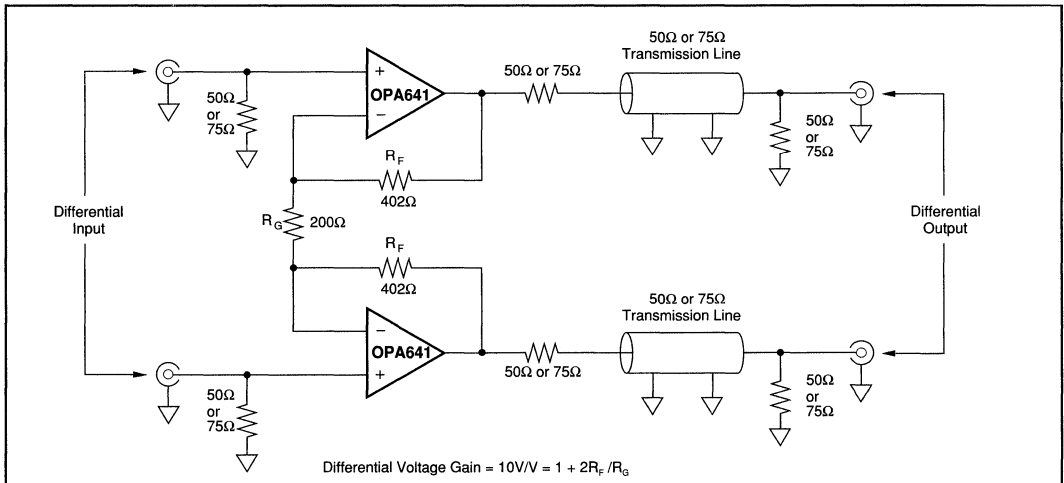


FIGURE 10. Differential Gain Amplifier and Driver for 50Ω or 75Ω Systems.

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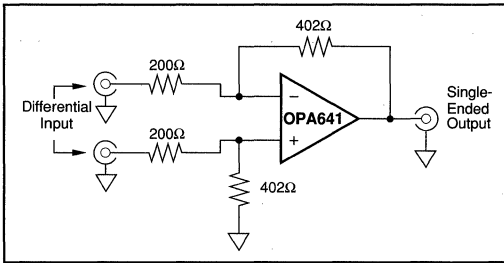


FIGURE 11. Difference Amplifier with Gain.

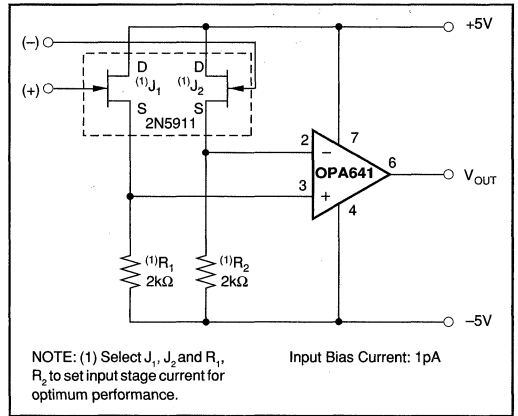


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

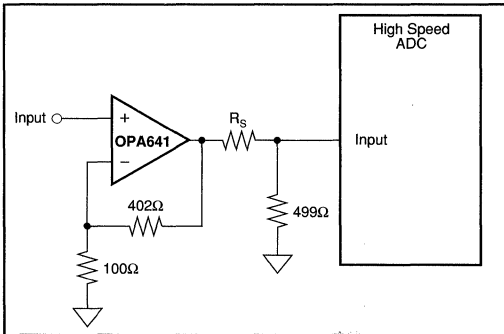
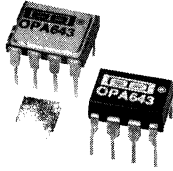


FIGURE 12. Gain Amplifier for ADCs ($G = +5V/V$).

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA642

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

OPA642

2

OPERATIONAL AMPLIFIERS

Wideband Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: -95dBc at 5MHz
- UNITY-GAIN BANDWIDTH: 450MHz
- UNITY-GAIN STABLE
- HIGH OPEN LOOP GAIN: 95dB
- HIGH COMMON MODE REJECTION: 90dB
- FAST 12-BIT SETTLING: 13ns (0.01%)
- LOW NOISE: $2.3\text{nV}/\sqrt{\text{Hz}}$
- HIGH OUTPUT CURRENT: $\pm 60\text{mA}$
- VERY LOW DIFF GAIN/PHASE ERROR:
 $0.007\%/0.008^\circ$

APPLICATIONS

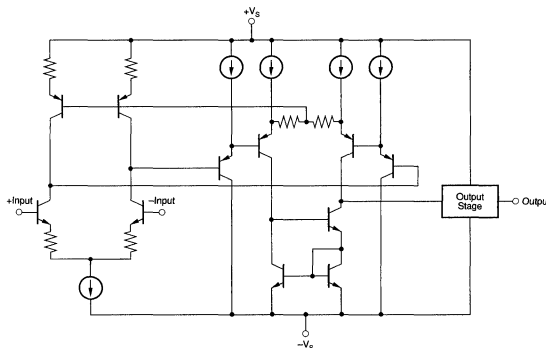
- ADC/DAC GAIN AMPLIFIER
- LOW DISTORTION COMMUNICATIONS
- HIGH RESOLUTION IMAGING
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- HIGH CMR DIFFERENCE AMPLIFIER
- VIDEO AMPLIFICATION
- TEST INSTRUMENTATION
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA642 is a voltage feedback operational amplifier featuring an unusual combination of high open loop gain and high bandwidth. The high open loop gain allows for minimal DC errors. The extra open loop gain at high bandwidths gives exceptionally low harmonic distortion. This makes the OPA642 compatible with high resolution and high dynamic range systems. It also offers fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA642 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA642 to be used in all op amp applications requiring high speed and precision.

Low distortion, low noise and high bandwidth make this amplifier suitable for a variety of RF, video, imaging and audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1190B

2.247

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA642H, P, U			OPA642HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			± 1.5	± 4		± 0.5	± 1.0	mV
Average Drift			4			2		$\mu\text{V}/^\circ\text{C}$
HSQ Grade Over Temperature						± 2.0	± 4.0	mV
Power Supply Rejection	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$	65	85		73	95		dB
INPUT BIAS CURRENT⁽¹⁾								
Input Bias Current	$V_{CM} = 0\text{V}$		18	30		*	*	μA
Over Specified Temperature			24	40		*	*	μA
HSQ Grade Over Temperature						25	40	μA
Input Offset Current	$V_{CM} = 0\text{V}$		0.1	2.0		*	*	μA
Over Specified Temperature			0.5	3.0		*	*	μA
HSQ Grade Over Temperature						1.0	5.0	μA
NOISE								
Input Voltage Noise								
Noise Density: $f = 100\text{Hz}$			8.6			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			2.5			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$			2.3			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 1\text{MHz}$ to 100MHz			2.3			*		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise, $\text{BW} = 100\text{Hz}$ to 100MHz			40			*		μVrms
Input Bias Current Noise Density								
$f = 0.1\text{Hz}$ to 20kHz			2.4			*		$\text{pA}/\sqrt{\text{Hz}}$
Noise Figure								
$R_S = 1\text{k}\Omega$			2.2			*		dB
$R_S = 50\Omega$			9.5			*		dB
INPUT VOLTAGE RANGE								
Common-mode Input Range			± 2.75	± 3.0		*	*	V
Over Temperature			± 2.5	± 2.75		*	*	V
Common-mode Rejection	$V_{CM} = \pm 0.5\text{V}$	65	85		80	92		dB
INPUT IMPEDANCE								
Differential			15 1			*		$\text{k}\Omega$ pF
Common-Mode			1.3 1			*		$\text{M}\Omega$ pF
OPEN-LOOP GAIN								
Open-loop Voltage Gain	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	80	95		85	98		dB
Over Specified Temperature		80	90		*	*		dB
FREQUENCY RESPONSE								
Closed Loop Response	All Four Pins Used					*		
Gain = +1V/V			450			*		MHz
Gain = +2V/V			150			*		MHz
Gain = +5V/V			45			*		MHz
Gain = +10V/V			21			*		MHz
Slew Rate ⁽¹⁾						*		
At Minimum Specified Temperature						*		
G = +1, 2V Step			380			*		V/ μs
G = +1, 2V Step			340			*		V/ μs
Settling Time: 0.003%						*		
G = +1, 1V Step			20			*		ns
0.01%			13			*		ns
0.1%			11.5			*		ns
1%			3.5			*		ns
Spurious Free Dynamic Range			92		80	95		dBc
Differ. Gain Error at 3.58MHz, G = +2V/V	$V_O = 2\text{Vp-p}$, $R_L = 100\Omega$		0.007			*		%
Differ. Phase Error at 3.58MHz, G = +2V/V	$V_O = 0\text{V}$ to 1.4V , $R_L = 150\Omega$		0.008			*		degrees
OUTPUT								
Current Output, +25°C			± 40	± 60		± 50	± 65	mA
Over Specified Temperature			± 35	± 55		± 40	± 60	mA
Voltage Output	No Load							
Over Specified Temperature			± 3.0	± 3.5		*	*	V
Voltage Output	$R_L = 100\Omega$							
Over Specified Temperature			± 2.5	± 2.75		*	*	V
Short Circuit Current						*	*	mA
Output Resistance	1MHz, G = +1V/V			0.04		*	*	Ω

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA642H, P, U			OPA642HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		± 5		*	*	*	V
Operating Voltage Range	T_{MIN} to T_{MAX}	± 4.5		± 5.5				V
Quiescent Current	T_{MIN} to T_{MAX}		± 22	± 29		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, U HSQ	Ambient	-40		+85	*	*	*	$^\circ\text{C}$
Storage	Ambient			+150	-55		+125	$^\circ\text{C}$
Thermal Resistance	Ambient	-55			-55		+150	$^\circ\text{C}$
	θ_{JA} , Junction-to-Ambient							$^\circ\text{C}/\text{W}$
P			120			*		$^\circ\text{C}/\text{W}$
U			170			*		$^\circ\text{C}/\text{W}$
H			120			*		$^\circ\text{C}/\text{W}$

NOTES: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

Basic Model Number	OPA642	()	()	(Q)
Package Code				
H = 8-pin Sidebraze DIP				
P = 8-pin Plastic DIP				
U = 8-pin Plastic SOIC				
Performance Grade Code				
S = -55°C to $+125^\circ\text{C}$				
B ⁽¹⁾ or No Letter = -40°C to $+85^\circ\text{C}$				
Reliability Screening				
Q = Q-Screened (HSQ Model Only)				

NOTE: (1) The "B" Grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 5\text{VDC}$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65°C to $+150^\circ\text{C}$
P, PB, U, UB	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
(soldering, SOIC 3s)	$+260^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$

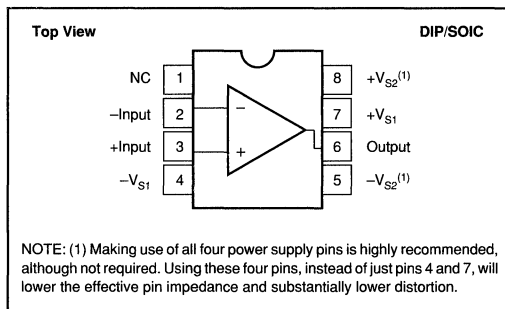
NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA642H, HSQ	8-Pin Sidebraze DIP	157
OPA642P, PB	8-Pin DIP	006
OPA642U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

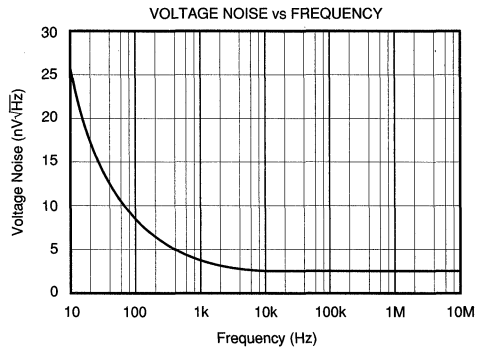
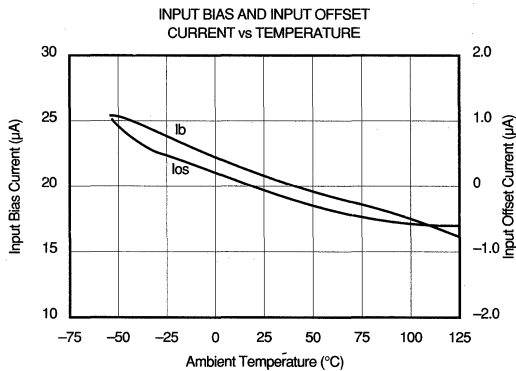
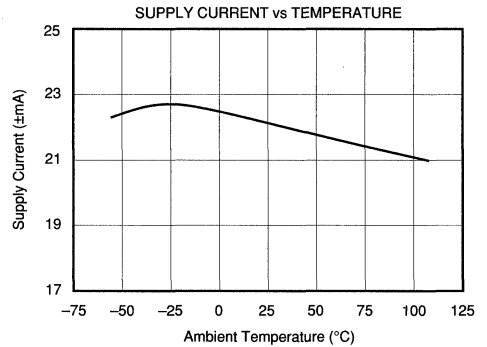
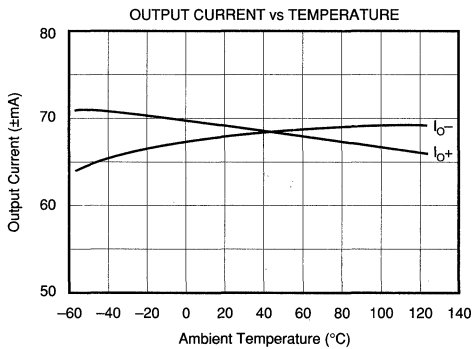
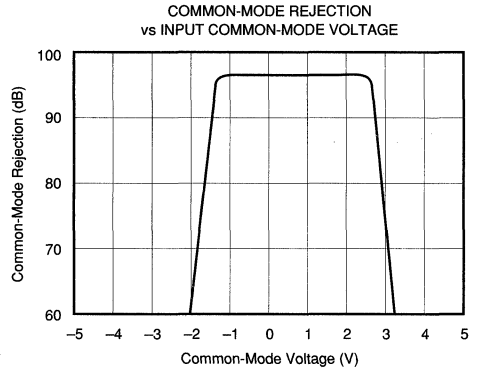
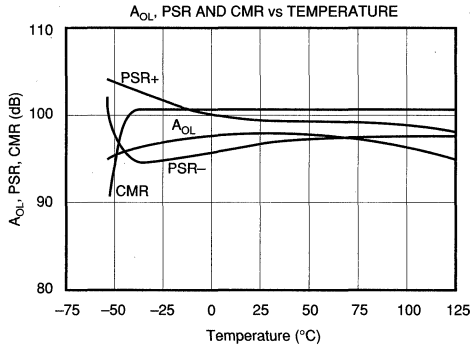
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

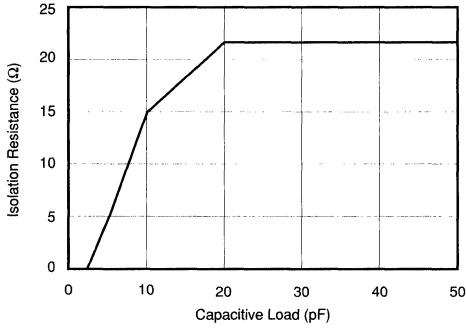


Or, Call Customer Service at 1-800-548-6132 (USA Only)

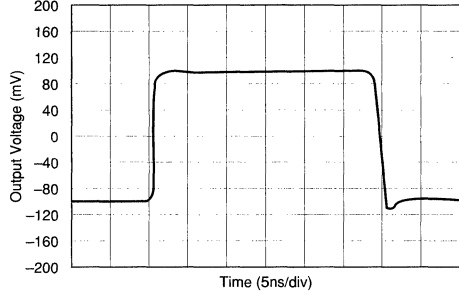
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_G = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

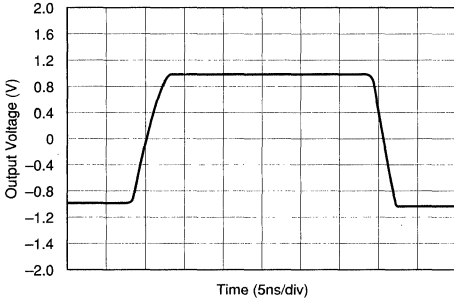
RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD FOR $G = +1$



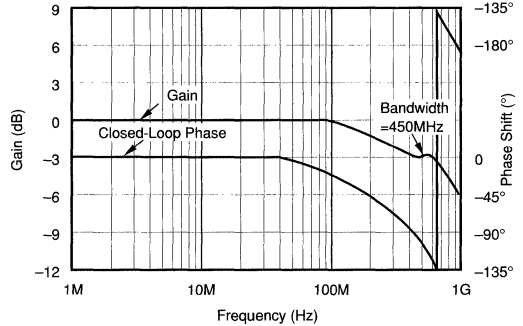
SMALL SIGNAL TRANSIENT RESPONSE
($G = +1$, $R_L = 100\Omega$)



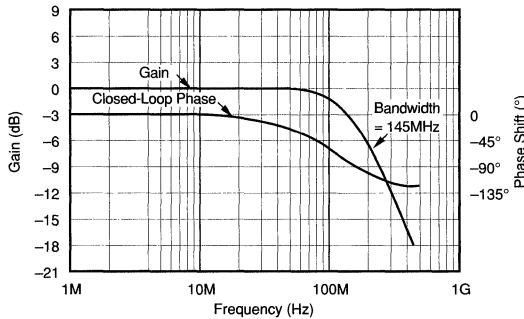
LARGE SIGNAL TRANSIENT RESPONSE
($G = +1$, $R_L = 100\Omega$)



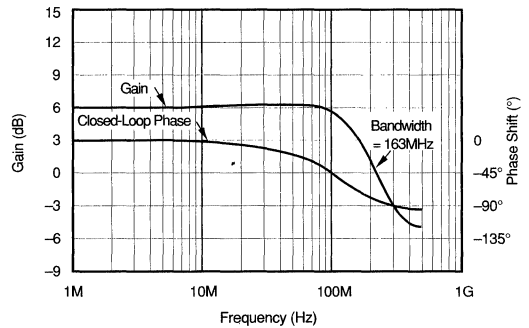
$G = +1\text{V/V}$ CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



$G = -1\text{V/V}$ CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



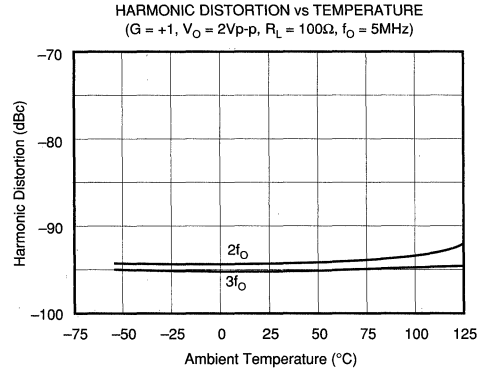
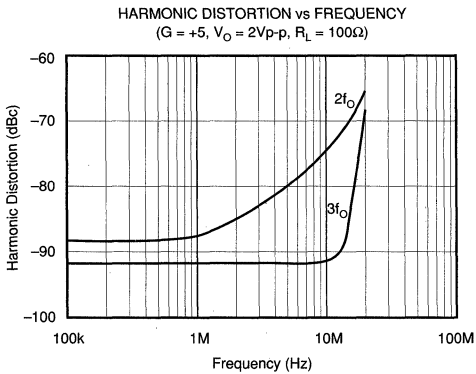
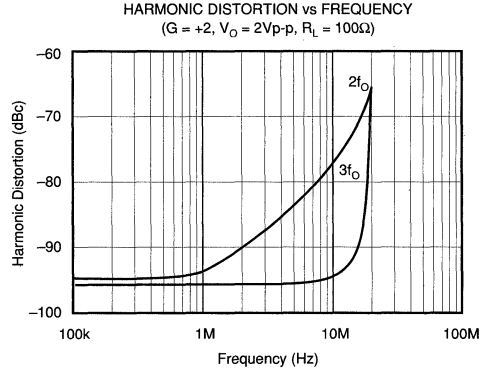
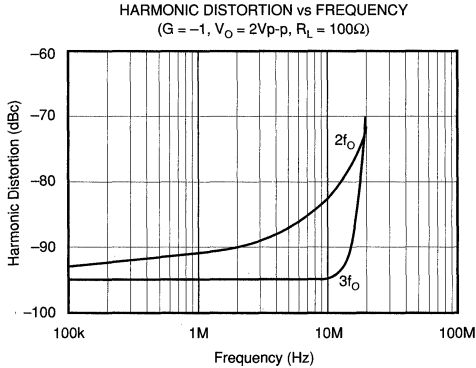
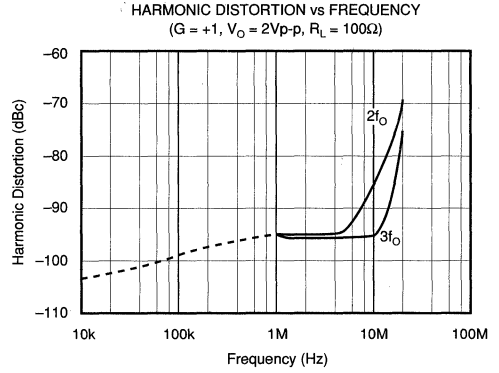
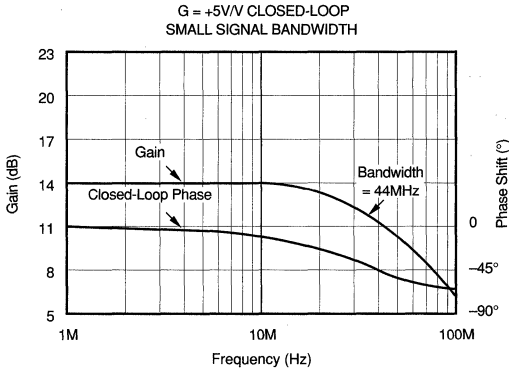
$G = +2\text{V/V}$ CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

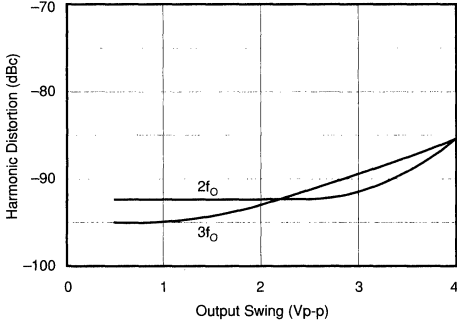


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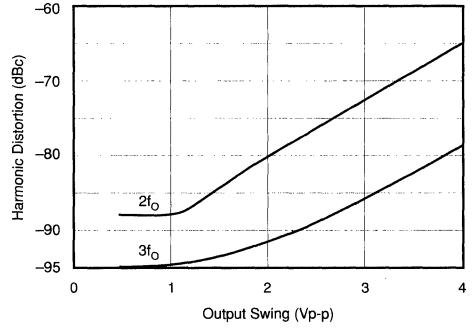
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

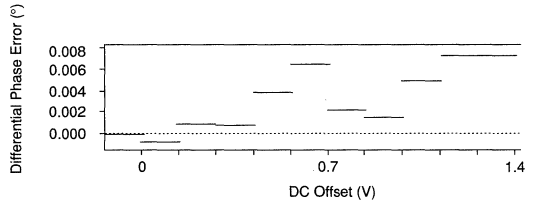
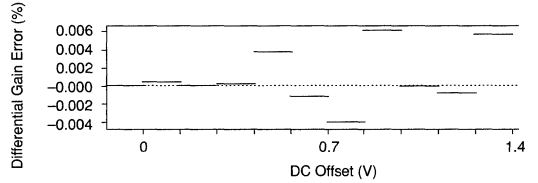
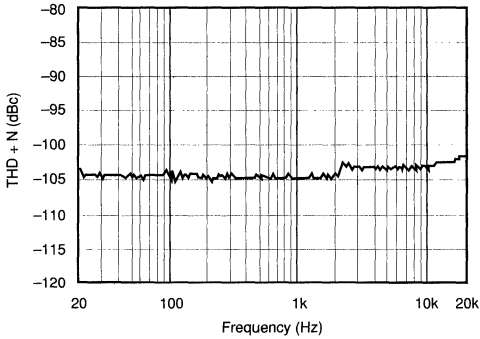
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +1$, $R_L = 100\Omega$)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +1$, $R_L = 100\Omega$)



THD + N vs FREQUENCY
($V_A = 2\text{Vp-p}$, $R_L = 100\Omega$)



OPA642

2 OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA642 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA642's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors due to input bias currents through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA642's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA642.

WIRING PRECAUTIONS

Maximizing the OPA642's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA642, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μ F) with very short leads are recommended. A parallel 0.01 μ F ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages and improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the DEM-OPA64X Data Sheet for the recommended layout and component placements.
- 2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 4) Whenever possible, solder the OPA642 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.
- 5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA642U (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and -5.2V, use of $\pm 15V$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA642's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

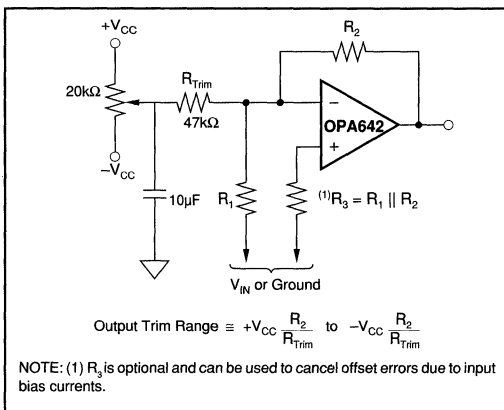


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA642 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

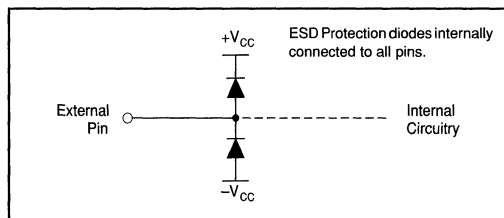


FIGURE 2. Internal ESD Protection.

All pins on the OPA642 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA642 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA642.

OUTPUT DRIVE CAPABILITY

The OPA642 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA642 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA642 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

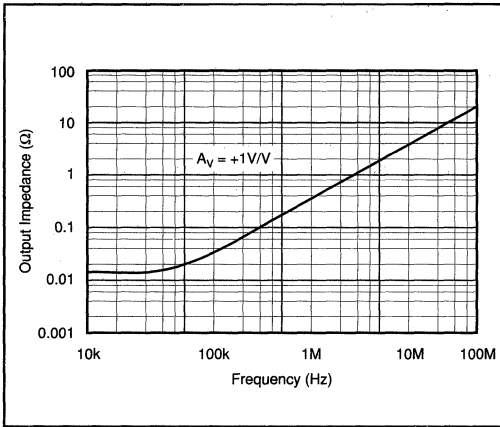


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA642 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 27mA = 270mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

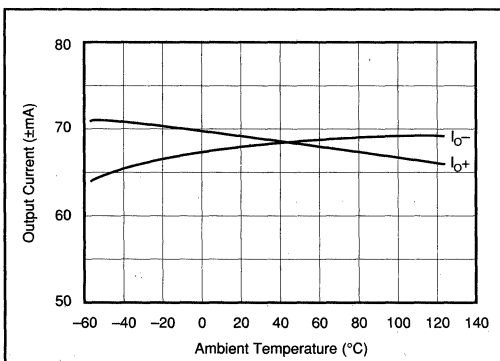


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA642's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the

amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 2pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the Gain from +1 will improve the capacitive load drive due to increased phase margin.

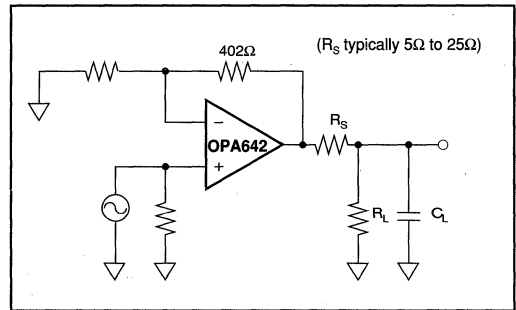


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA642 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of -1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA642 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break

frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu\text{V}$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA642 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 90ns.

In practice, settling time measurements on the OPA642 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA642 were measured with the amplifier in a gain of +2V/V with 75 Ω input impedance and the output back-terminated in 75 Ω . The input signal selected from the generator was a 0V to 1.4V modulated ramp with a sync pulse.

With these conditions the test circuit shown in Figure 6 delivered a 100IRE modulated ramp to the 75 Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the perfor-

mance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA642 is 0.007% differential gain and 0.008° differential phase to both NTSC and PAL standards. Increasing the closed loop gain degrades the DP and DG.

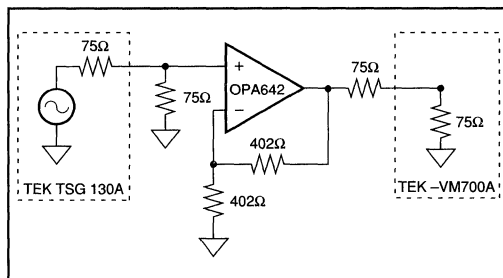


FIGURE 6. Differential Gain and Differential Phase Test Circuit.

DISTORTION

The OPA642's Harmonic Distortion characteristics into a 100 Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 7. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

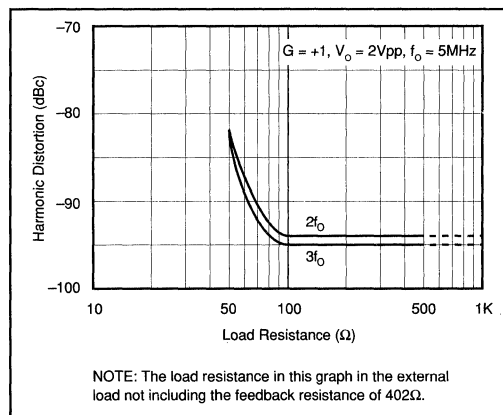


FIGURE 7. Harmonic Distortion vs Load Resistance.

For Immediate Assistance, Contact Your Local Salesperson

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 8 shows the OPA642's single tone, third-order IM intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency and load resistance. For example, assume that the application requires the OPA642 to operate in a gain of +1V/V and drive 2V_{p-p} into 50Ω at a frequency of 5MHz. Referring to Figure 8, we find that the intercept point is +58dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OIP3P} - P_o)$$

where OIP3P = third-order output intercept, dBm
 P_o = output level, dBm

For this case OIP3P = 58dBm, P_o = 10dBm, and the third harmonic = 2(58 - 10) = 96dB below the fundamental. The OPA642's low distortion makes the device an excellent choice for a variety of RF signal processing applications. The two-tone third-order intercept point is approximately 8dB lower than the single tone intercept.

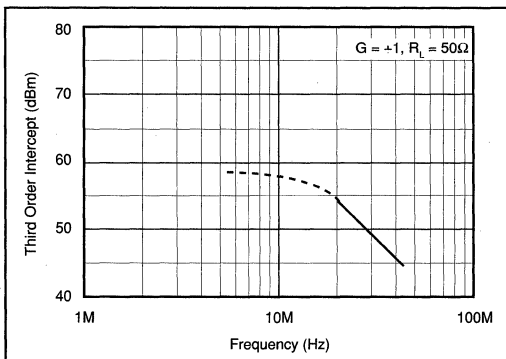


FIGURE 8. Single Tone, 3rd Order Intercept vs Frequency.

NOISE FIGURE

The OPA642 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA642's Noise Figure vs Source Resistance is shown in Figure 9.

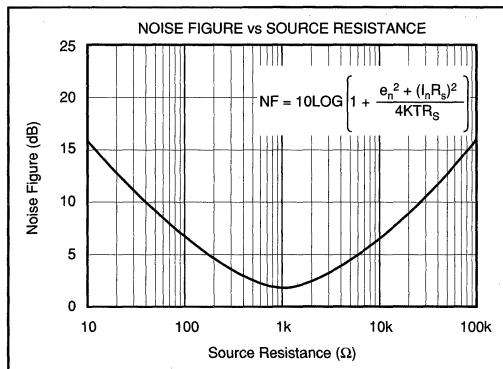


FIGURE 9. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA642. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x 10 ⁻⁸ atm cc/s, 30PSiG Gross: Perfluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on the HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x Datasheet for details.

APPLICATIONS

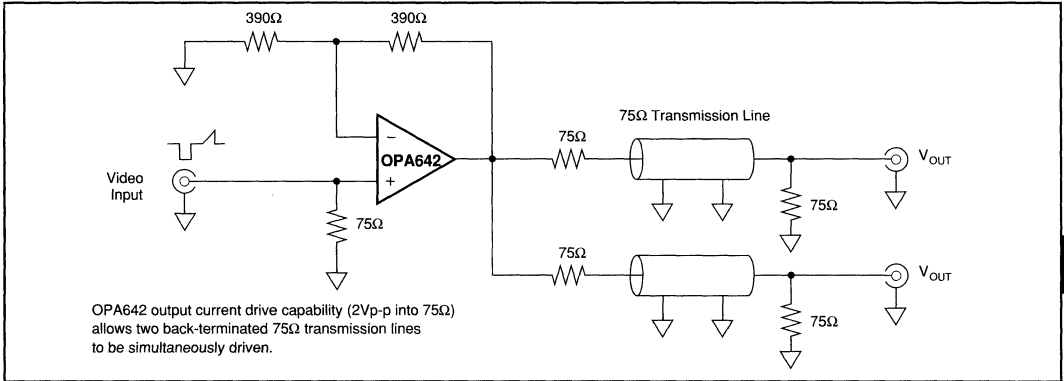


FIGURE 10. Video Distribution Amplifier.

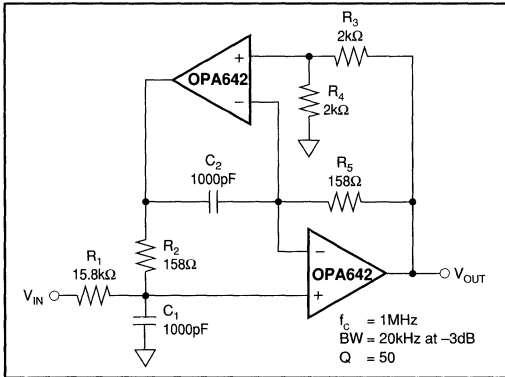


FIGURE 11. High-Q 1MHz Bandpass Filter.

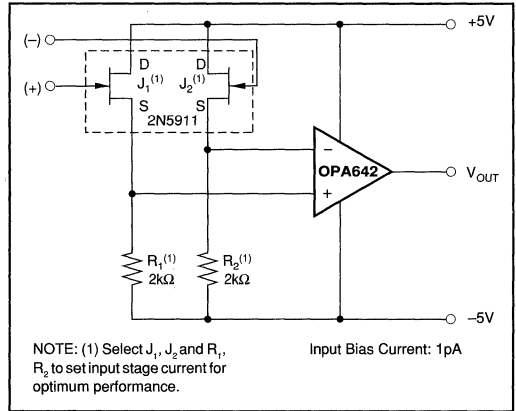


FIGURE 12. Low Noise, Wideband FET Input Op Amp.

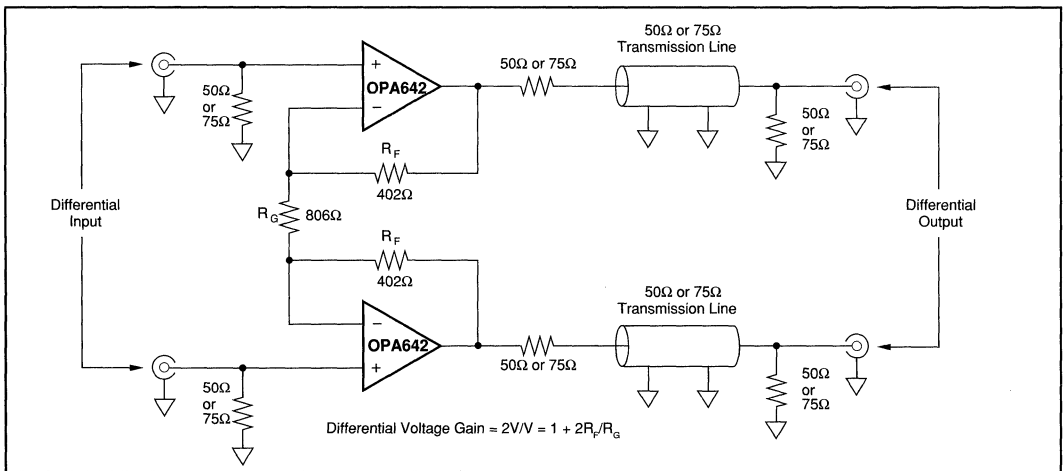


FIGURE 13. Differential Line Driver for 50Ω or 75Ω Systems.

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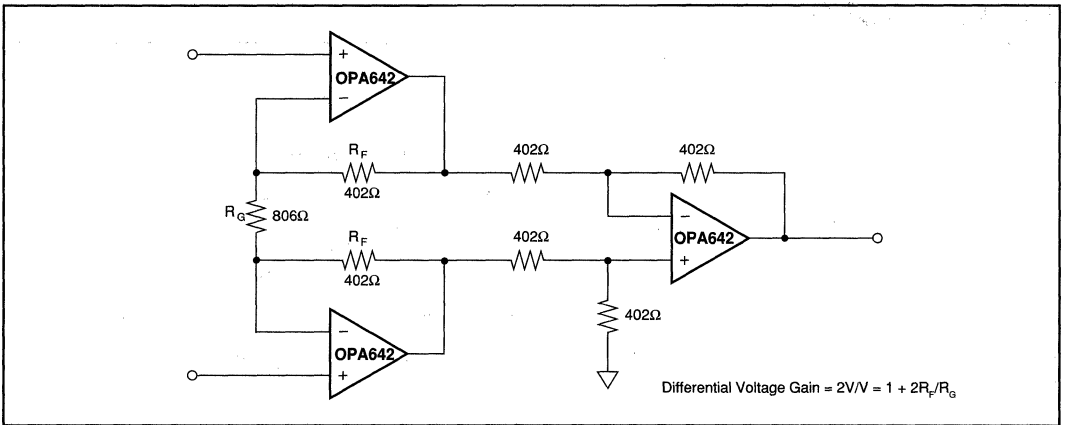


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier.

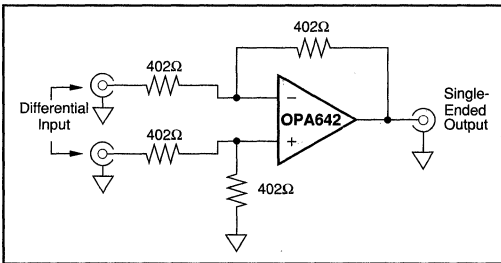


FIGURE 15. Unity Gain Difference Amplifier.

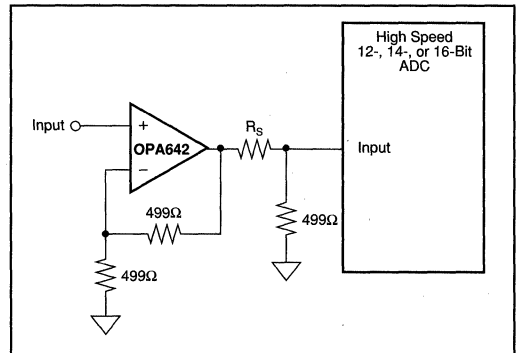


FIGURE 16. Low Distortion Gain Amplifier for ADCs ($G = -2V/V$).

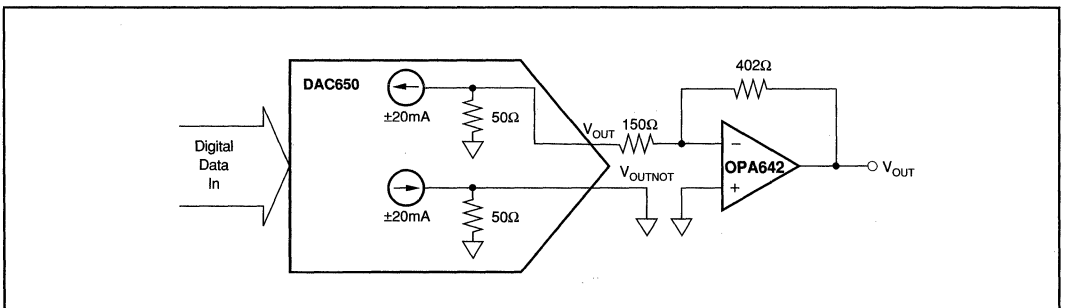


FIGURE 17. Gain Amplifier for High Speed Digital-to-Analog Converters Like the DAC650.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

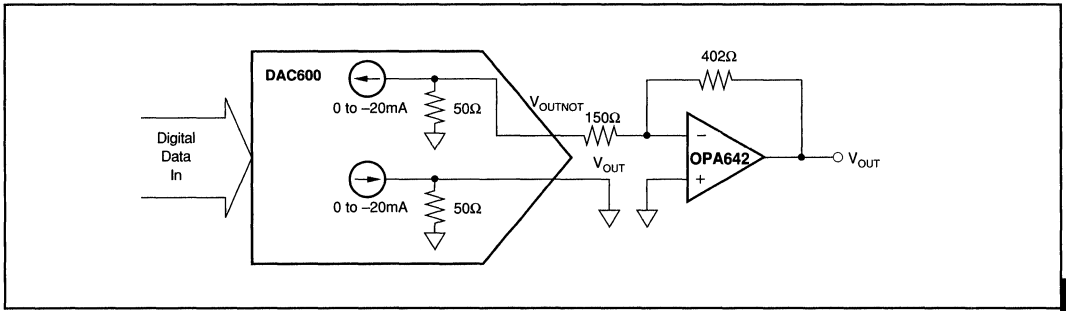
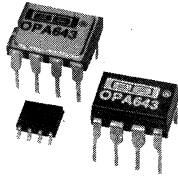


FIGURE 18. Gain Amplifier for High Speed Digital-to-Analog Converters Like the DAC600.

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OPA643

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

Wideband Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- **LOW DISTORTION:** -90dBc at 5MHz
- **LOW NOISE:** $1.8\text{nV}/\sqrt{\text{Hz}}$
- **GAIN-BANDWIDTH:** 1.5GHz
- **STABLE IN GAINS** ≥ 5
- **HIGH SLEW RATE:** $1000\text{V}/\mu\text{s}$
- **HIGH OPEN LOOP GAIN:** 95dB
- **HIGH COMMON MODE REJECTION:** 90dB
- **FAST 12-BIT SETTLING:** 21ns (0.01%)
- **LOW DIFFERENTIAL GAIN/PHASE ERROR:** 0.005%/0.015°

APPLICATIONS

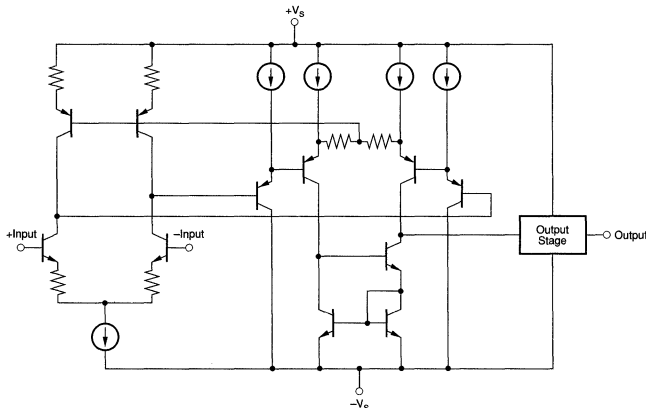
- **ADC/DAC GAIN AMPLIFIER**
- **LOW DISTORTION COMMUNICATIONS**
- **HIGH RESOLUTION IMAGING**
- **MEDICAL IMAGING**
- **LOW NOISE PREAMPLIFIER**
- **VIDEO AMPLIFICATION**
- **TEST INSTRUMENTATION**
- **AUDIO AMPLIFICATION**

DESCRIPTION

The OPA643 is a voltage feedback operational amplifier featuring an unusual combination of high open loop gain and high bandwidth. The high open loop gain allows for minimal DC errors. The extra open loop gain at high bandwidths gives exceptionally low harmonic distortion. This makes the OPA643 compatible with high resolution and high dynamic range systems. It also offers fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA643 is internally compensated for stability in gains of 5 or greater. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA643 to be used in all op amp applications requiring high speed and precision.

Low distortion, low noise and high linearity make this amplifier suitable for RF, video, imaging and audio applications.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRBCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA643H, P, U			OPA643HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±2.5	±4		±0.5	±1.5	mV
Average Drift			5			3		μV/°C
HSQ Grade Over Temperature						±2.5	±5	mV
Power Supply Rejection (+V _S)	V _S = ±4.5 to ±5.5V	65	85		70	*		dB
INPUT BIAS CURRENT⁽¹⁾								
Input Bias Current	V _{CM} = 0V		19	30		*	*	μA
Over Specified Temperature			24	40		*	*	μA
HSQ Grade Over Temperature						2.5	40	μA
Input Offset Current	V _{CM} = 0V		0.1	2.0		*	*	μA
Over Specified Temperature			0.5	3.0		*	*	μA
HSQ Grade Over Temperature						1.0	5.0	μA
NOISE								
Input Voltage Noise								
Noise Density: f = 100Hz			10.3			*		nV/√Hz
f = 10kHz			1.9			*		nV/√Hz
f = 1MHz			1.8			*		nV/√Hz
f _B = 1MHz to 100MHz			1.8			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			18			*		μVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			2.4			*		pA/√Hz
Noise Figure								
R _S = 1kΩ			1.6			*		dB
R _S = 50Ω			7.0			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.75	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-Mode Rejection	V _{CM} = ±0.5V	65	85		80	92		dB
INPUT IMPEDANCE								
Differential			15 1			*		kΩ pF
Common-Mode			8 1			*		MΩ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V _O = ±2V, R _L = 100Ω	82	95		87	*		dB
Over Specified Temperature	V _O = ±2V, R _L = 100Ω	80	90		82	*		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	Gain = +5V/V		300			*		MHz
	Gain = +10V/V		112			*		MHz
	Gain = +20V/V		47			*		MHz
Slew Rate ⁽¹⁾	G = +5, 2V Step		1000			*		V/μs
At Minimum Specified Temperature	G = +5, 2V Step		920			*		V/μs
Settling Time: 0.003%	G = +5, 2V Step		60			*		ns
0.01%	G = +5, 2V Step		21			*		ns
0.1%	G = +5, 2V Step		16.5			*		ns
1%	G = +5, 2V Step		7.5			*		ns
Spurious Free Dynamic Range	G = +5, f = 5MHz		90		80	90		dBc
	V _O = ±2Vp-p, R _L = 100Ω							
Differential Gain Error at 3.58MHz	G = +5V/V, V _O = 0V to 1.4V, R _L = 150Ω		0.005			*		%
Differential Phase Error at 3.58MHz	G = +5V/V, V _O = 0V to 1.4V, R _L = 150Ω		0.015			*		degrees
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±3.0	±3.25		*	*		V
Voltage Output, +25°C	R _L = 100Ω							
Over Specified Temperature		±2.5	±2.75		*	*		V
Current Output, +25°C		±40	±60		±50	±65		mA
Over Specified Temperature		±35	±50		±40	*		mA
Output Resistance	1MHz, G = +5V/V		0.035			*		Ω
POWER SUPPLY								
Specified Operating Voltage		±4.5	±5	±5.5	*	*	*	V
Operating Voltage Range				±27		*	*	V
Quiescent Current			±22	±27		*	*	mA
Over Specified Temperature			±23	±29		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, U	Ambient	-40		+85	*		*	°C
HSQ	Ambient				-55		+125	°C
Thermal Resistance	θ _{JA} , Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

OPA643

2

OPERATIONAL AMPLIFIERS

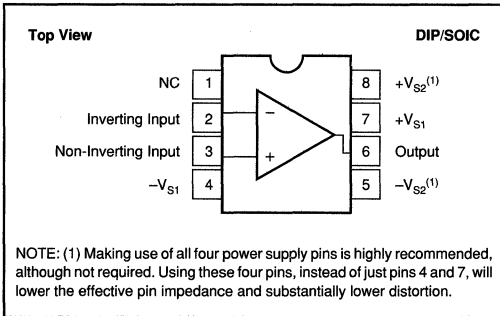
For Immediate Assistance, Contact Your Local Salesperson

ORDERING INFORMATION

Basic Model Number	OPA643	()	()	(Q)
Package Code				
H = 8-pin Sidebraze DIP				
P = 8-pin Plastic DIP				
U = 8-pin Plastic SOIC				
Performance Grade Code				
S = -55°C to +125°C				
B ⁽¹⁾ or No Letter = -40°C to +85°C				
Reliability Screening				
Q = Q-Screened (HSQ Model Only)				

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65°C to +150°C
P, PB, U, UB	-40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA643H, HSQ	8-Pin Cerdip	157
OPA643P, PB	8-Pin DIP	006
OPA643U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

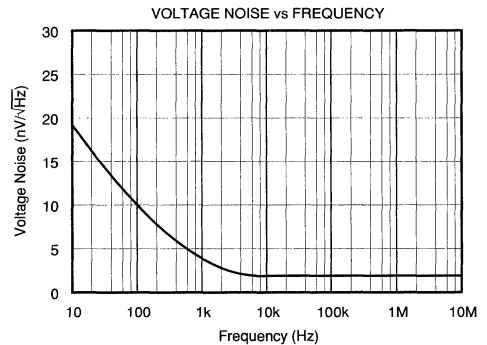
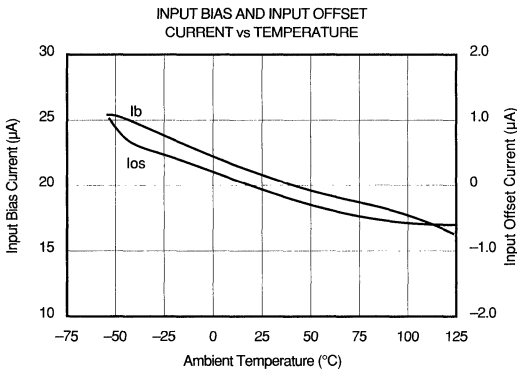
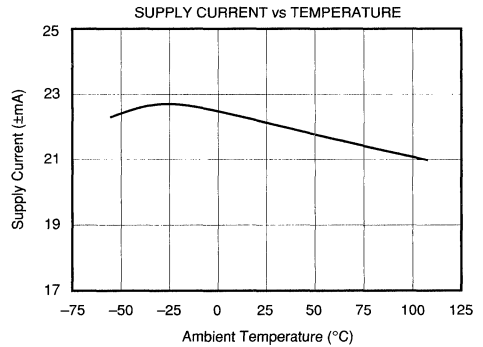
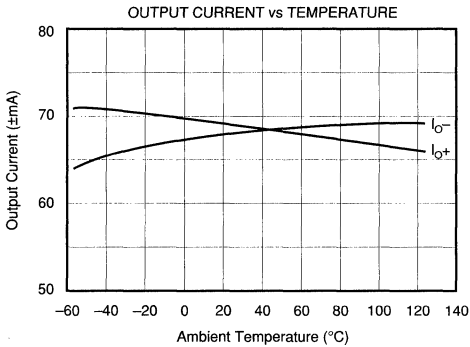
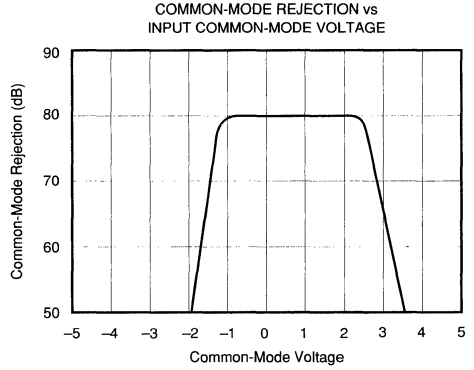
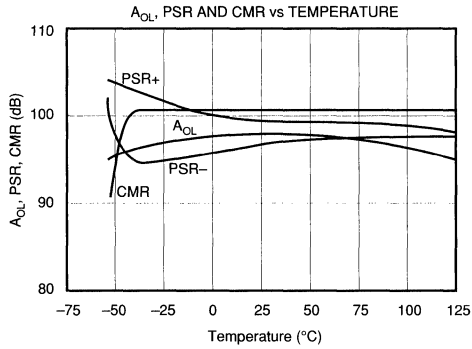
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted

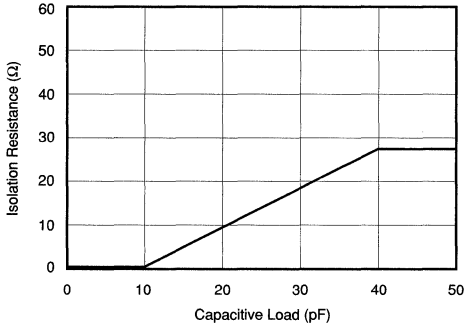


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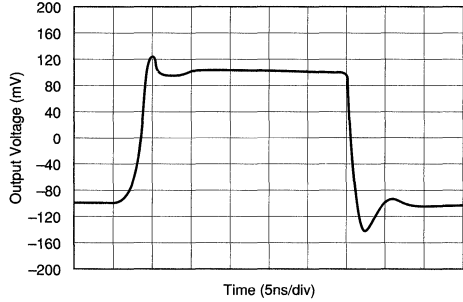
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

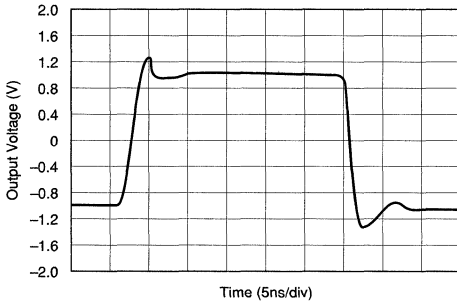
RECOMMENDED ISOLATION RESISTANCE vs
CAPACITIVE LOAD FOR $G = +5$



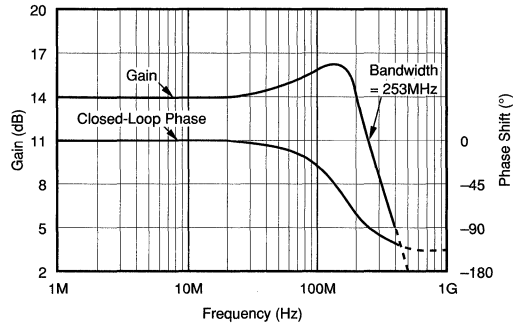
SMALL SIGNAL TRANSIENT RESPONSE
($G = +5$, $R_L = 100\Omega$)



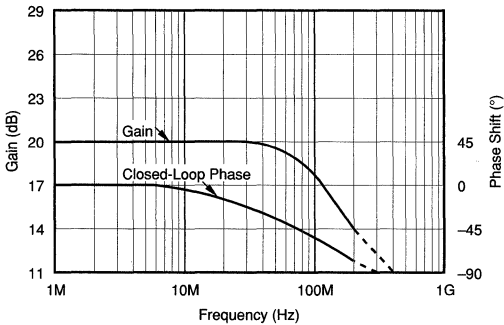
LARGE SIGNAL TRANSIENT RESPONSE
($G = +5$, $R_L = 100\Omega$)



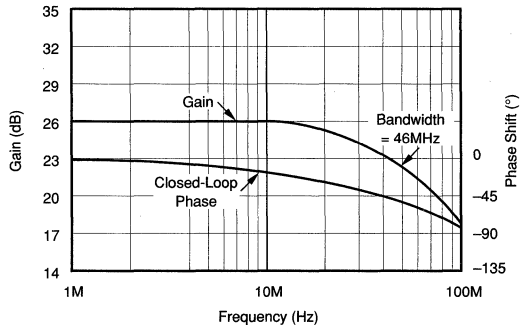
$G = \text{CLOSED-LOOP}$
SMALL SIGNAL BANDWIDTH



$G = +10$ CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



$G = +20$ CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

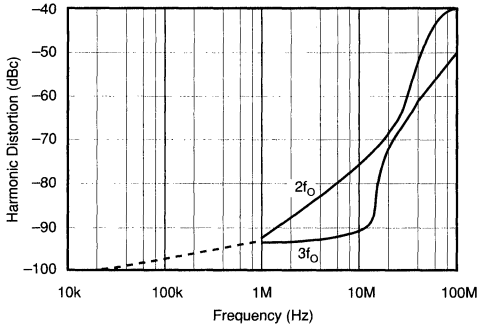


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TYPICAL PERFORMANCE CURVES (CONT)

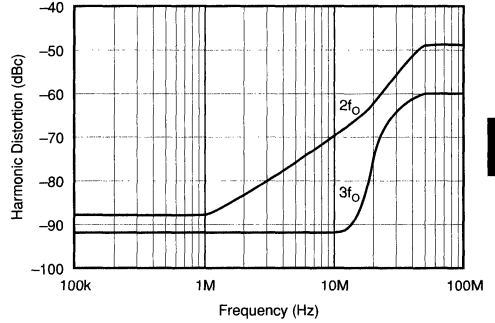
$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY
($G = +5$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$)

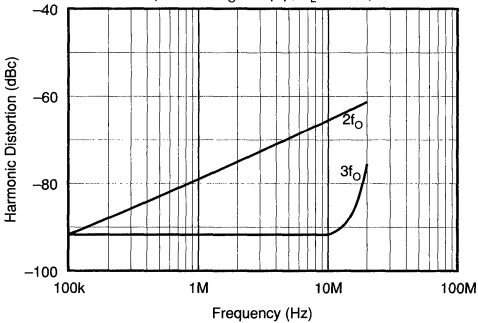


NOTE: The Dashed Line Represents THD + N.
The Actual Harmonics will be lower.

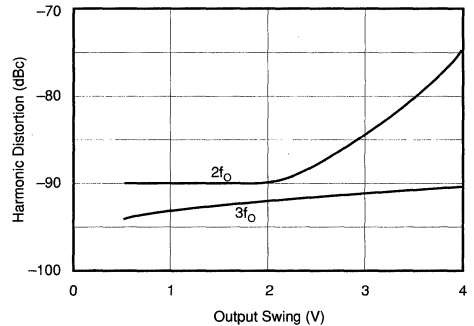
HARMONIC DISTORTION vs FREQUENCY
($G = +10$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$)



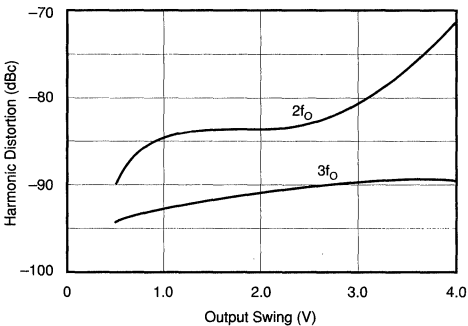
HARMONIC DISTORTION vs FREQUENCY
($G = +20$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$)



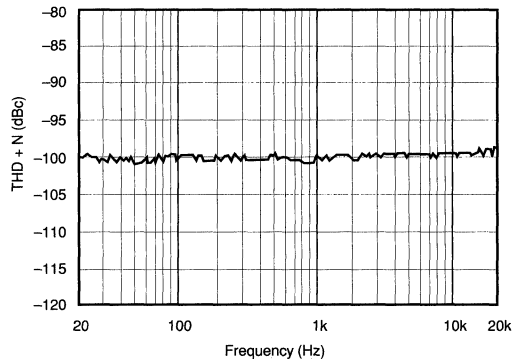
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +5$, $R_L = 100\Omega$)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = +5$, $R_L = 100\Omega$)



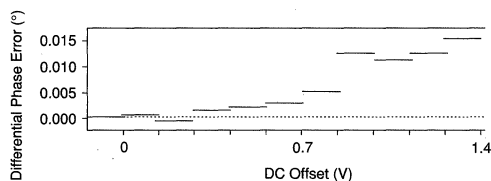
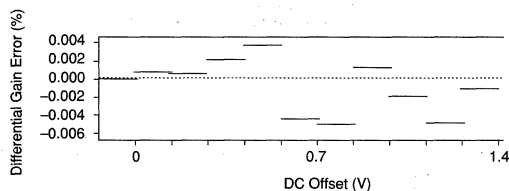
AUDIO PRECISION THD + N vs FREQUENCY



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA643 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA643's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA643's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA643.

WIRING PRECAUTIONS

Maximizing the OPA643's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed

amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA643, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μF) with very short leads are recommended. A parallel 0.01 μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective pin impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with $0.01\mu\text{F}$ and $2.2\mu\text{F}$ surface mount capacitors is recommended. It is essential to keep the $0.01\mu\text{F}$ capacitor very close to the power supply pins. Refer to the demonstration board figure at the end of the data sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA643 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about $1\text{k}\Omega$ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. **A longer feedback path than this will decrease the realized bandwidth substantially.** Refer to the demonstration board layout at the end of the data sheet.

6) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA643U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5\text{V}$ supplies. Although they will operate perfectly well with $+5\text{V}$ and -5.2V , use of $\pm 15\text{V}$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA643's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current, which is typically only $0.2\mu\text{A}$.

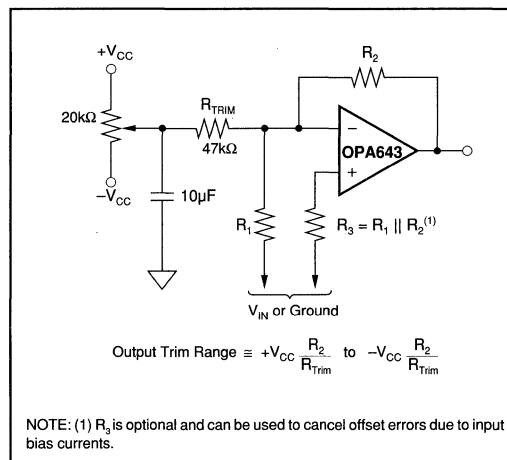


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA643 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

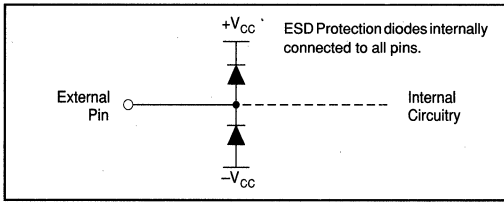


FIGURE 2. Internal ESD Protection.

All pins on the OPA643 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA643 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA643.

OUTPUT DRIVE CAPABILITY

The OPA643 has been optimized to drive 30Ω, 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA643 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA643 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

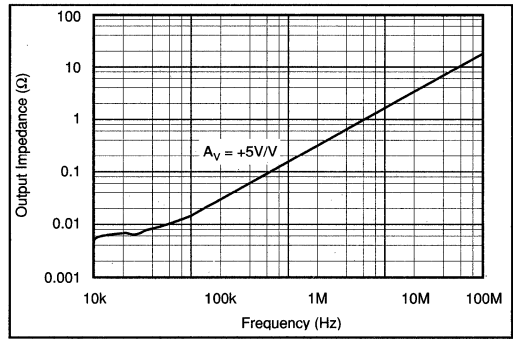


FIGURE 3. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA643 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 29mA = 290mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Figure 4.

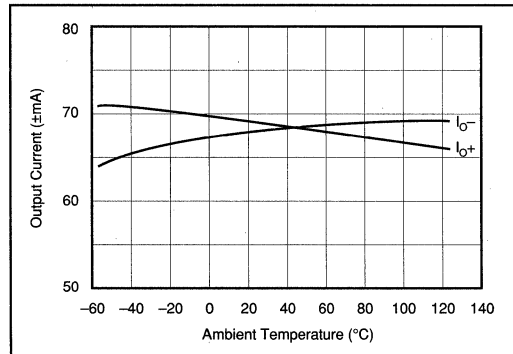


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA643's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +5 will improve the capacitive load drive due to increased phase margin.

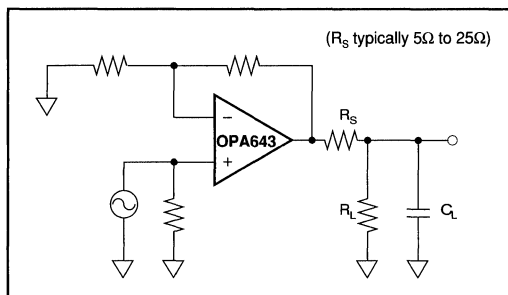


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA643 is internally compensated and is stable in a noise gain of 5 or greater with a phase margin of approximately 60°. Higher gains will improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of -5V/V is equivalent to a noise gain of 6.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA643 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-

loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

Settling time, specified in a non-inverting gain of 5, occurs in only 15ns to 0.01% for a 2V output step, making the OPA643 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 90ns.

In practice, settling time measurements on the OPA643 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set. All PAL measurements were performed using a Rohde & Schwarz Video Analyzer UAF.

DG and DP of the OPA643 were measured with the amplifier in a gain of +5V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse.

With these conditions the test circuit shown in Figure 1 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer

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was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA643 is 0.005% differential gain and 0.015° differential phase to both NTSC and PAL standards. Increasing the closed loop gain degrades the DP and DG.

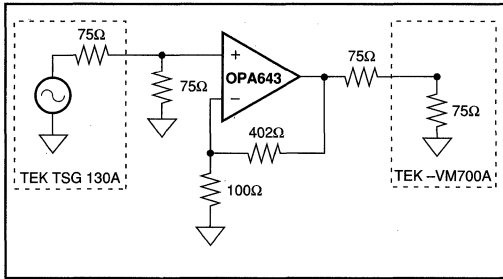


FIGURE 6. Configuration for Testing Differential Gain/Phase.

DISTORTION

The OPA643's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 7. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

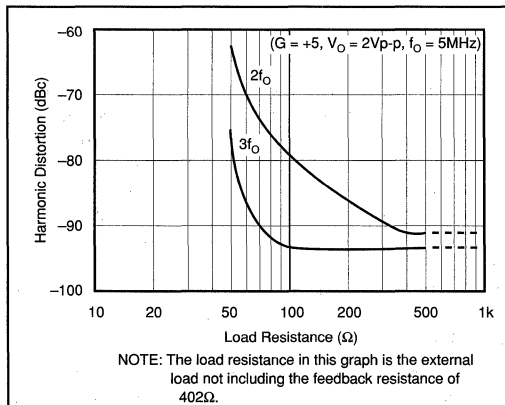


FIGURE 7. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 8 shows the OPA643's single-tone, third-order intercept vs frequency. This curve is particularly useful for determining the magni-

tude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA643 to operate in a gain of +5V/V and drive 2Vp-p into 50Ω at a frequency of 5MHz. Referring to Figure 8 we find that the intercept point is +47dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OIP3} - P_o)$$

where OIP3 = third-order output intercept, dBm
 P_o = output level, dBm

For this case $\text{OIP3} = 47\text{dBm}$, $P_o = 10\text{dBm}$, and the third-order $\text{IMD} = 2(47 - 10) = 74\text{dB}$ below the fundamental. The OPA643's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

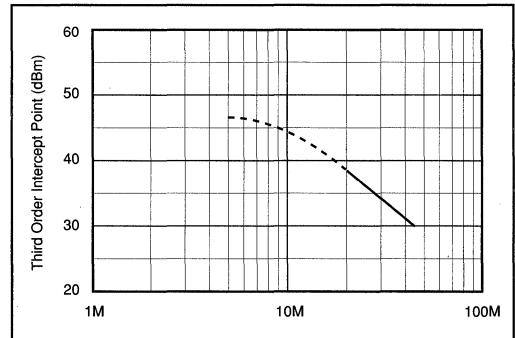


FIGURE 8. Single-Tone, 3rd Order Intermodulation Intercept vs Frequency.

NOISE FIGURE

The OPA643 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA643's Noise Figure vs Source Resistance is shown in Figure 9.

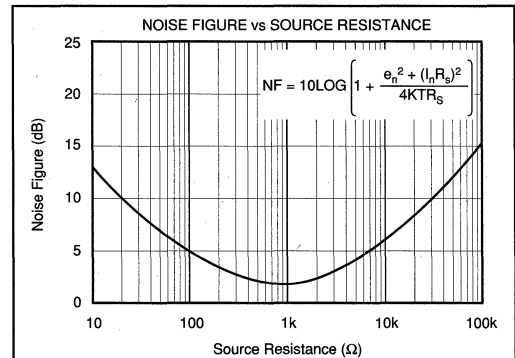


FIGURE 9. Noise Figure vs Source Resistance.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown “Q-Screening” provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5×10^{-8} atm cc/s, 30PSIG Gross: Perfluorocarbon bubble test, 60PSIG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on the HS package only.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA643. Contact Burr-Brown Applications Department to receive a spice diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x Datasheet for details.

APPLICATIONS

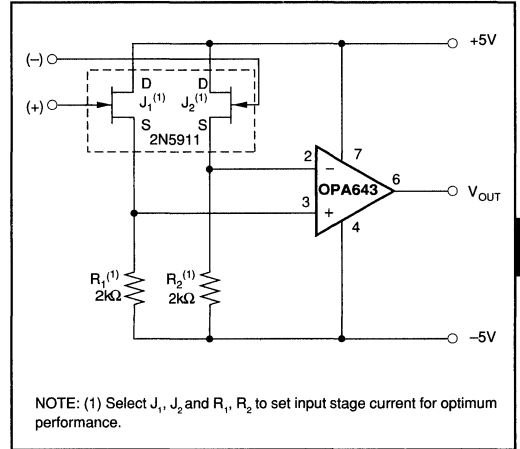


FIGURE 10. Low Noise, Wideband FET Input Op Amp.

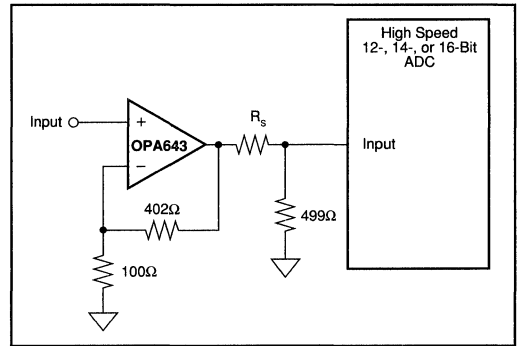


FIGURE 11. Differential Input Buffer Amplifier ($G = +5V/V$).

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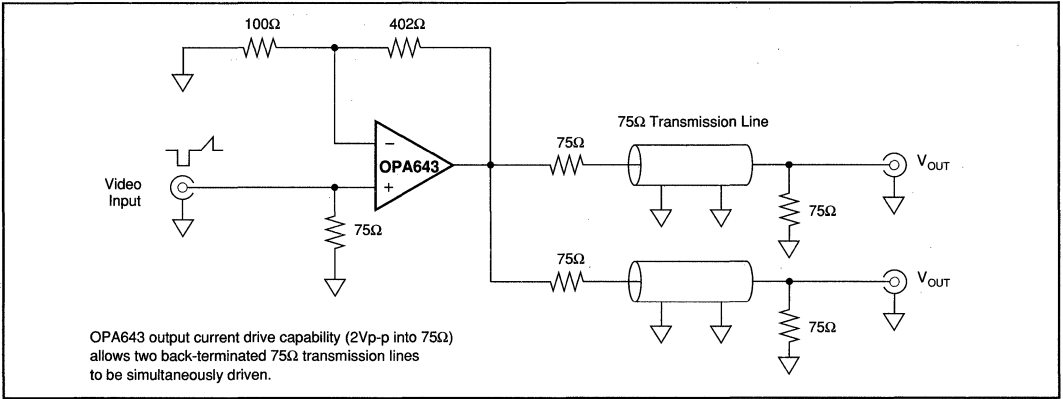


FIGURE 12. Video Distribution Amplifier.

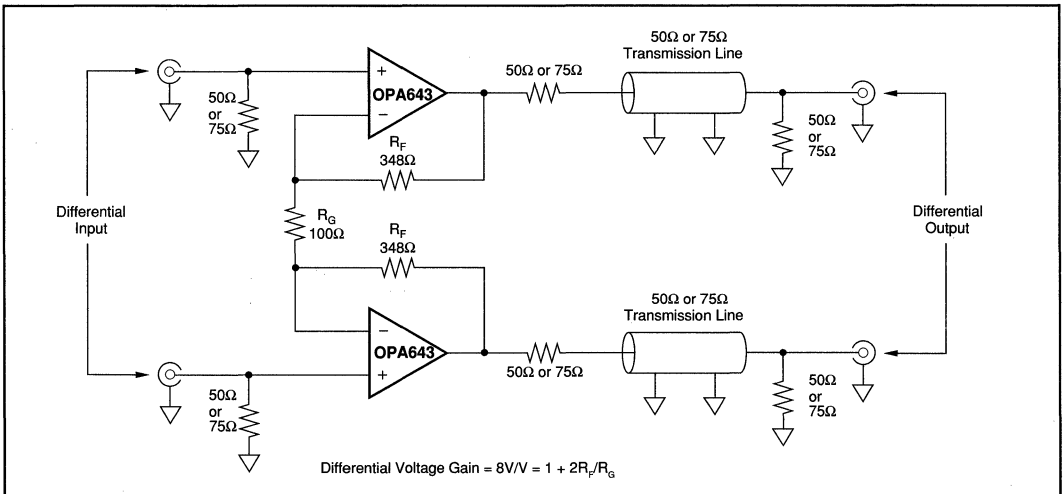


FIGURE 13. Differential Gain Amplifier and Driver for 50Ω and 75Ω Systems.

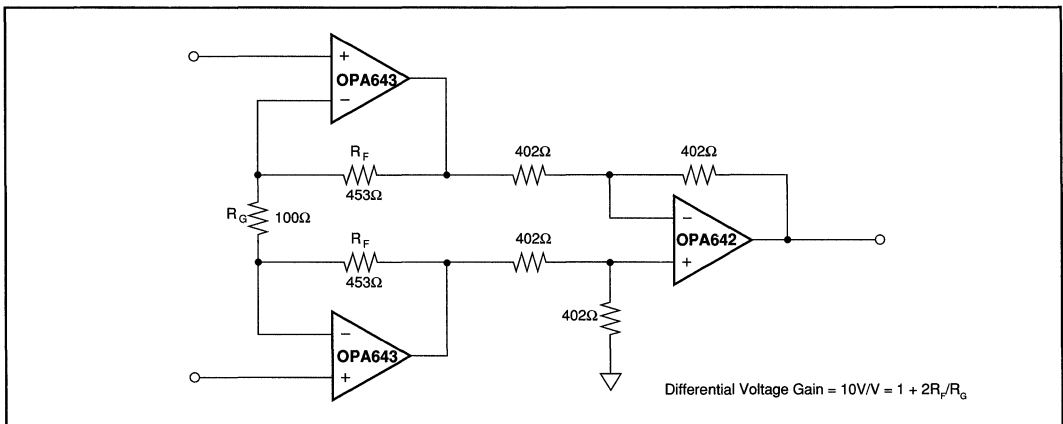
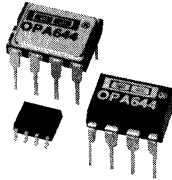


FIGURE 14. Wideband, Fast-Settling Instrumentation Amplifier with Two High Impedance Inputs.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA644

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

Low Distortion Current Feedback OPERATIONAL AMPLIFIER

FEATURES

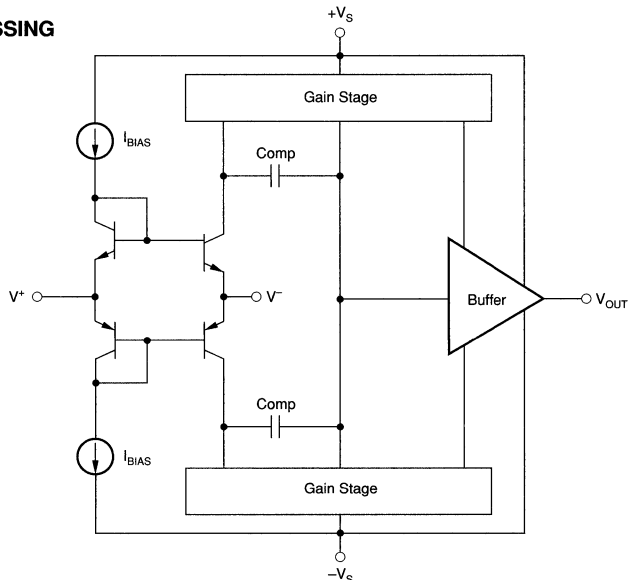
- SLEW RATE: 2500V/ μ s
- VERY LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.008%/0.009°
- LOW DISTORTION AT 5MHz: -85dBc
- HIGH BANDWIDTH: 500MHz
- CLEAN PULSE RESPONSE
- HIGH OPEN LOOP TRANSMIMPEDANCE: 2.0M Ω
- HIGH LINEARITY
- FAST 12-BIT SETTLING: 21ns to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- COMMUNICATIONS
- ADC/DAC GAIN AMPLIFIER
- RF AMPLIFICATION
- MEDICAL IMAGING
- AUDIO AMPLIFICATION

DESCRIPTION

The OPA644 is a wideband precision current feedback operational amplifier featuring exceptionally high open loop transimpedance and high slew rate. The current feedback architecture allows for excellent large signal bandwidth, even at high gains. The high transimpedance allows this op amp to be used in applications requiring 16-bits or more of accuracy. This extra transimpedance at high bandwidths gives very low distortion and low differential gain and phase errors. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA644 offers exceptional performance in monolithic form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 899-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA644H, P, U			OPA644HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage	$G = +10$		± 2.5	± 6		± 2	± 3	mV
Average Drift			20			10		$\mu\text{V}/^\circ\text{C}$
HSQ Grade Average Drift						20	35	$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$	40	65		60	75		dB
INPUT BIAS CURRENT⁽¹⁾								
Non-Inverting			± 20	± 40		± 15	± 20	μA
Over Specified Temperature			± 24	± 90		± 20	± 50	μA
HSQ Grade Over Temperature						35	60	μA
Inverting			± 2	± 25		*	± 10	μA
Over Specified Temperature			± 4	± 35		± 3	± 25	μA
HSQ Grade Over Temperature						± 5	± 25	μA
NOISE								
Input Voltage Noise Density	$G = +10$							
$f = 100\text{Hz}$			10.3			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			2.9			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			1.9			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$			1.9			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 100\text{Hz}$ to 200MHz			33.6			*		μVrms
Inverting Input Bias Current								
Noise Density: $f = 10\text{MHz}$			15			*		$\text{pA}/\sqrt{\text{Hz}}$
Non-Inverting Input Current								
Noise Density: $f = 10\text{MHz}$			15			*		$\text{pA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE								
Common-Mode Input Range		± 2.0	± 2.25		*	*		V
Over Specified Temperature		± 1.8	± 2.1		*	*		V
Common-Mode Rejection	$V_{CM} = \pm 2\text{V}$	35	55		45	65		dB
INPUT IMPEDANCE								
Non-Inverting			500 1.0			*		$\text{k}\Omega$ pF
Inverting			20			46		Ω
Open-Loop Transimpedance	$V_O = \pm 2\text{V}$, $R_L = 1\text{k}\Omega$	1.4	2.0		*	*		$\text{M}\Omega$
FREQUENCY RESPONSE, $R_{FB} = 402\Omega$	All Four Power Pins Used							
Closed Loop Bandwidth	$G = +1\text{V/V}$		500			*		MHz
	$G = +2\text{V/V}$		300			*		MHz
	$G = +5\text{V/V}$		180			*		MHz
	$G = +10\text{V/V}$		125			*		MHz
	$G = +20\text{V/V}$		80			*		MHz
Slew Rate ⁽¹⁾	$G = +2$, 2V Step		2500			*		$\text{V}/\mu\text{s}$
Settling Time: 0.01%	$G = +2$, 2V Step		21			*		ns
0.1%	$G = +2$, 2V Step		16.5			*		ns
1%	$G = +2$, 2V Step		5.5			*		ns
Overload Recovery Time ⁽²⁾			60			*		ns
Spurious Free Dynamic Range	$G = -1$, $f = 5.0\text{MHz}$ $V_O = 2\text{Vp-p}$ $G = -1$, $f = 20\text{MHz}$		84			86		dBc
Differential Gain Error at 3.58MHz	$G = +2\text{V/V}$, $V_O = 0\text{V}$ to 1.4V $R_L = 150\Omega$		0.008			*		dBc
Differential Phase Error at 3.58MHz	$G = +2\text{V/V}$, $V_O = 0\text{V}$ to 1.4V $R_L = 150\Omega$		0.009			*		Degrees
Gain Flatness to 1dB	$G = +1$		250			*		MHz
OUTPUT								
Current Output		± 40	± 60		± 50	± 66		mA
Over Specified Temperature		± 30	± 45		± 40	± 50		mA
Voltage Output	No Load							
Over Specified Temperature		± 3.0	± 3.5		*	*		V
Voltage Output	$R_L = 100\Omega$							
Over Specified Temperature		± 2.75	± 3.25		*	*		V
Short Circuit Current			75				*	mA
Output Resistance	1MHz, $G = +2\text{V/V}$		0.2				*	Ω
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		± 5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	± 4.5		± 5.5	*	*		V
Quiescent Current	T_{MIN} to T_{MAX}		± 18	± 26	*	*		mA

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA644H, P, U			OPA644HSQ, PB UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification: H, P, U HSQ Thermal Resistance, θ_{JA} P U H		-40		+85	*		*	$^\circ\text{C}$ $^\circ\text{C}$
			120		*		*	$^\circ\text{C}/\text{W}$
			170		*		*	$^\circ\text{C}/\text{W}$
			120		*		*	$^\circ\text{C}/\text{W}$

NOTE: (1) Slew rate is rate of change from 10% to 90% of the output voltage step. (2) Time for the output to resume linear operation after saturation.

ORDERING INFORMATION

Basic Model Number	OPA644	()	()
Package Code			
H = 8-pin Sidebraze DIP			
P = 8-pin Plastic DIP			
U = 8-pin Plastic SOIC			
Performance Grade Code			
SQ = -55°C to $+125^\circ\text{C}$, Reliability Screened			
B ⁽¹⁾ or No Letter = -40°C to $+85^\circ\text{C}$			

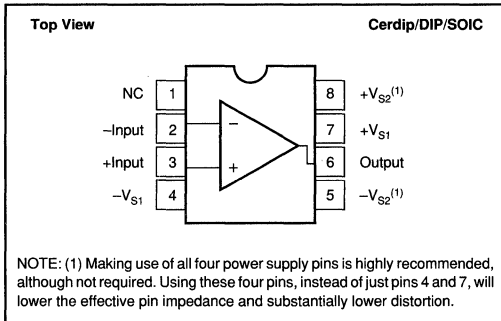
NOTE: (1) The "B" Grade of the SOIC package will be marked with a "B" by pin 8. Refer to the mechanical section for the location.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 5.5\text{VDC}$
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65°C to $+150^\circ\text{C}$
P, PB, U, UB	-40°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
(soldering, SOIC 3s)	$+260^\circ\text{C}$
Junction Temperature (T_J)	$+175^\circ\text{C}$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PIN CONFIGURATION (All Packages)



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA644H, HSQ	8-Pin Cerdip	157
OPA644P, PB	8-Pin DIP	006
OPA644U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

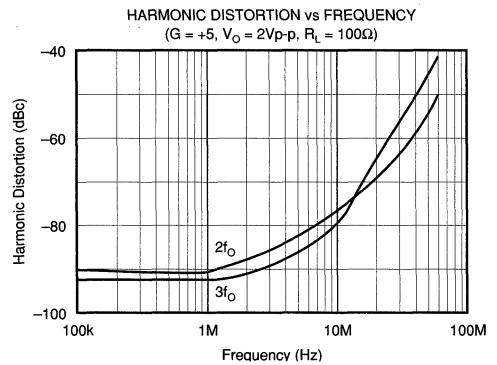
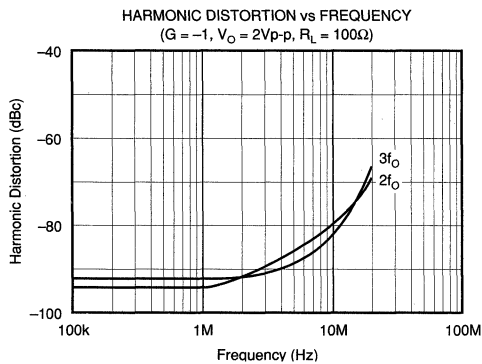
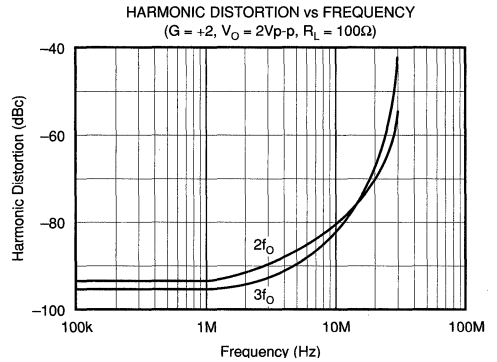
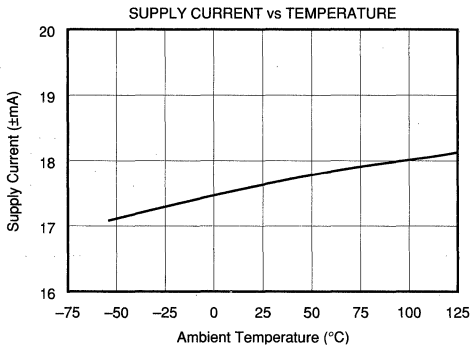
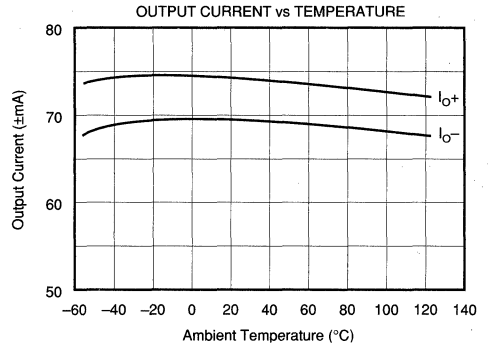
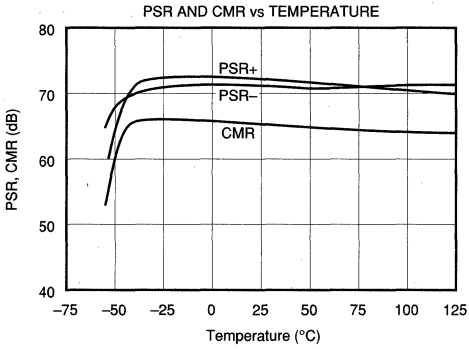
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\mu\text{F}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

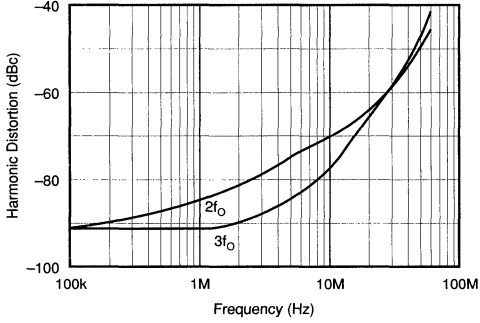


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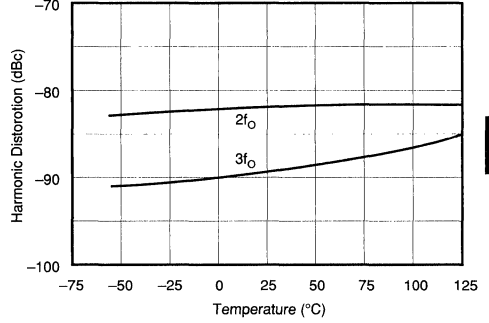
TYPICAL PERFORMANCE CURVES (CONT.)

$T_A = +25^\circ\text{C}$, $V_O = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

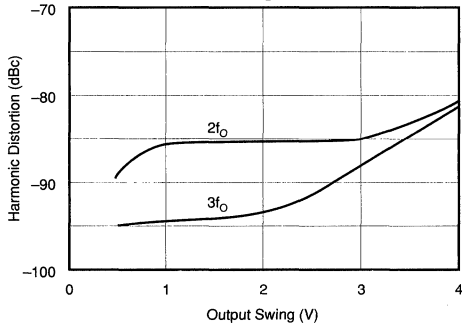
HARMONIC DISTORTION vs FREQUENCY
($G = +10$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$)



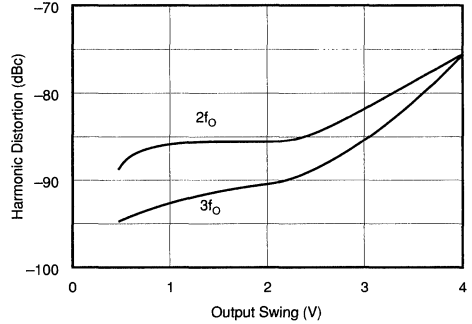
HARMONIC DISTORTION vs TEMPERATURE
($G = -1$, $V_O = 2\text{Vp-p}$, $R_L = 100\Omega$, $f_O = 5\text{MHz}$)



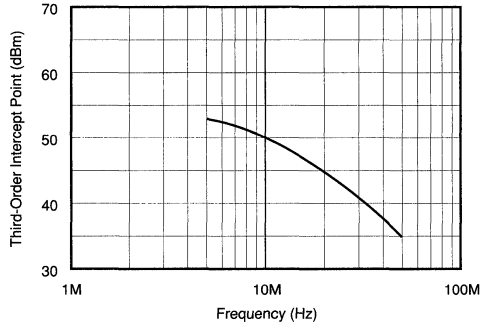
5MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = -1$, $R_L = 100\Omega$)



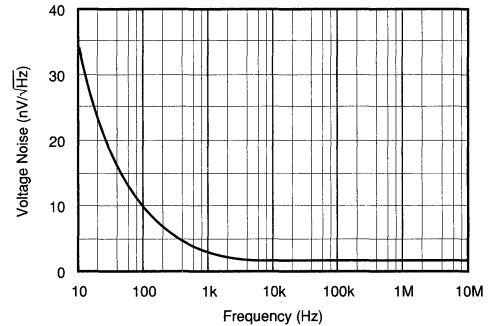
10MHz HARMONIC DISTORTION vs OUTPUT SWING
($G = -1$, $R_L = 100\Omega$)



THIRD-ORDER INTERCEPT POINT vs FREQUENCY
($G = -1$, $R_L = 50\Omega$, $R_{FB} = 402\Omega$)



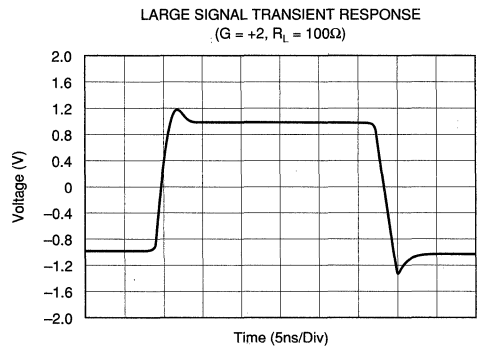
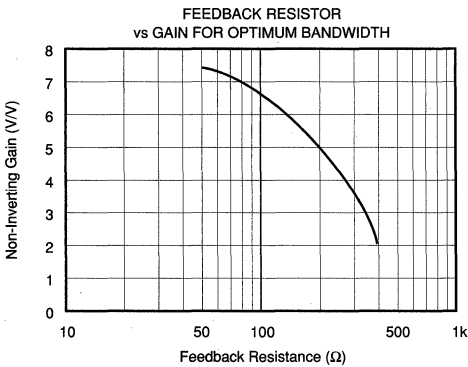
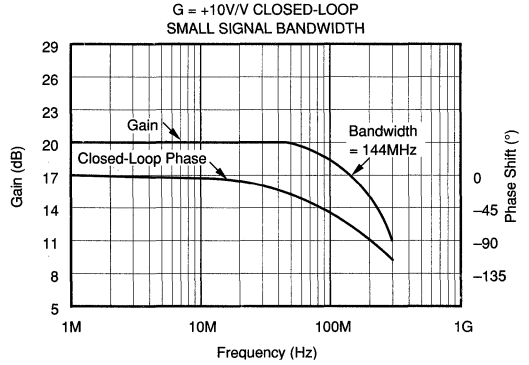
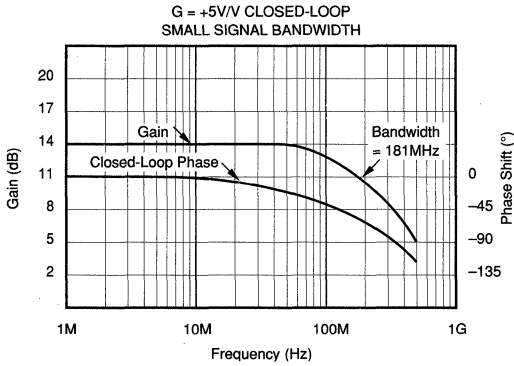
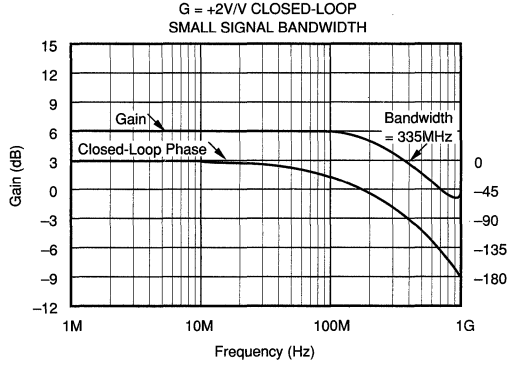
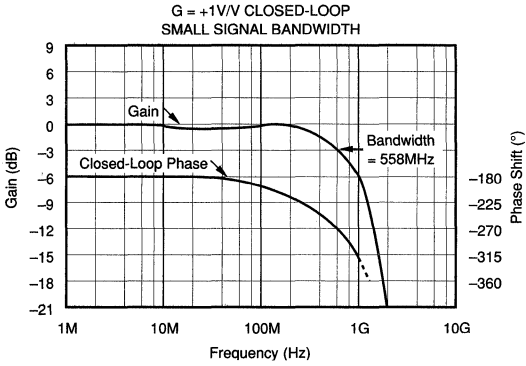
NON-INVERTING INPUT
VOLTAGE NOISE vs FREQUENCY
($G = +10$)



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TYPICAL PERFORMANCE CURVES (CONT.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

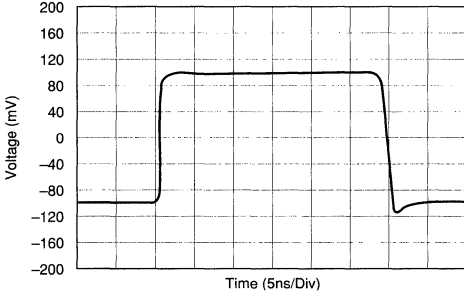


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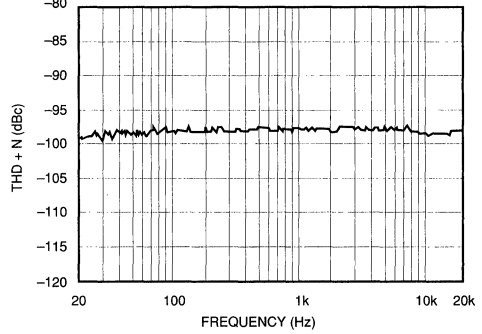
TYPICAL PERFORMANCE CURVES (CONT.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

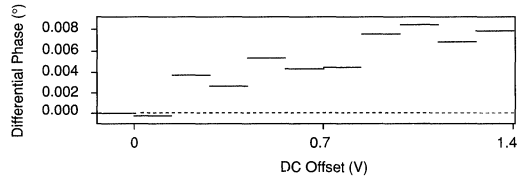
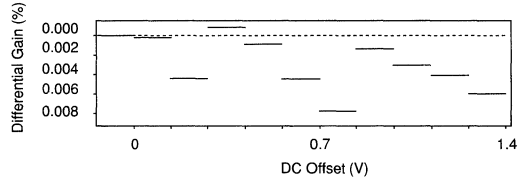
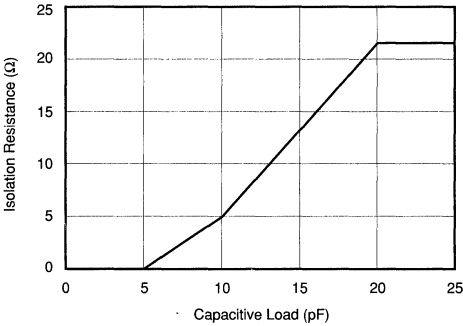
SMALL SIGNAL TRANSIENT RESPONSE
($G = +2$, $R_L = 100\Omega$)



AUDIO PRECISION THD + N vs FREQUENCY



RECOMMENDED ISOLATION RESISTANCE
vs. CAPACITIVE LOAD



APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is very little bandwidth degradation at higher gain settings.

The current feedback architecture of the OPA644 provides the traditional strength of excellent large signal response with the unusual addition of very high open-loop transimpedance. This high open-loop transimpedance allows the OPA644 to be used in applications requiring 16-bits or more of accuracy and dynamic linearity.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_e) is amplified by the open loop transimpedance gain (T_o). The output signal generated is equal to $T_o \times I_e$. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

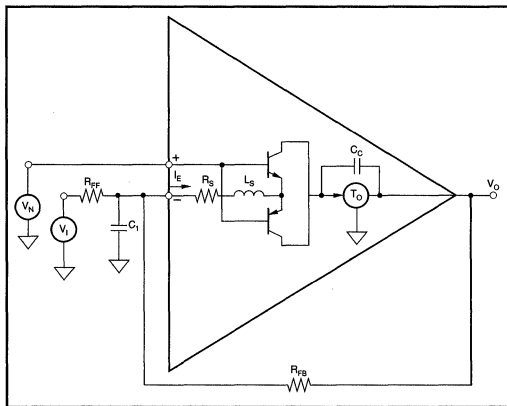


FIGURE 1. Equivalent Circuit

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_e) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FF}/R_I)$.

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA644 can be calculated using the following equations:

$$\text{Inverting Gain} = (-R_{FB}/R_{FF})/(1+1/\text{Loop Gain}) \quad (1)$$

$$\text{Non-inverting Gain} = (1 + R_{FB}/R_{FF})/(1 + 1/\text{Loop Gain}) \quad (2)$$

$$\text{where: Loop Gain} = T(o)/(R_{FB}) \times (1/(1+T(o)/(R_{FB}/R_{FF})))$$

At higher gains the small value inverting input impedance (R_{INV}) causes an apparent loss in bandwidth. This can be seen from the equation:

$$\text{Factual} = F_{IDEAL}/(1 + (R_{INV}/R_{FB}) (1 + R_{FB}/R_{FF})) \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm I_{bN} \times R_N (1 + R_{FB}/R_G) \pm V_{IO} (1 + R_{FB}/R_G) \pm I_{bI} \times R_{FB} \quad (4)$$

If all terms are divided by the gain $(1 + R_{FB}/R_G)$ it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

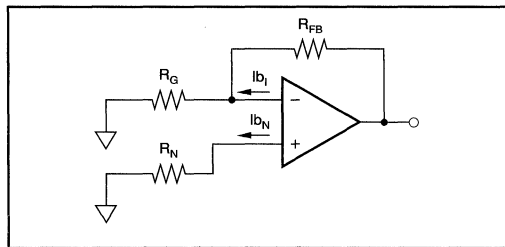


FIGURE 2. Output Offset Voltage Equivalent Circuit.

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB} (refer to Figure 1). This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} . As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF} , which reduces closed loop bandwidth. To maintain specified bandwidth, the following equations can be used to approximate R_F and R_I for any gain from ± 1 to ± 15 .

$R_{FB} = 424 \pm 8G$ (+ for inverting and – for non-inverting)

$R_{FF} = (424 - 8G)/(G - 1)$ (non-inverting)

$R_I = (424 + 8G)/G$ (inverting)

G = Closed loop gain

WIRING PRECAUTIONS

Maximizing the OPA644's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low inductance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA644, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μ F) with very short leads are recommended. A parallel 0.01 μ F ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X datasheet for the recommended layout and component placements.

(2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA644 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the datasheet.

6) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA644U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and –5.2V, use of $\pm 15V$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA644's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

For Immediate Assistance, Contact Your Local Salesperson

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA644 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

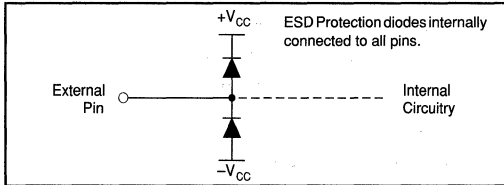


FIGURE 3. Internal ESD Protection.

All pins on the OPA644 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA644 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA644.

OUTPUT DRIVE CAPABILITY

The OPA644 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA644 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA644 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

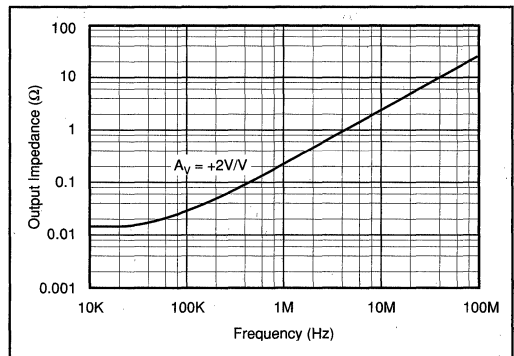


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA644 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 26mA = 260mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA644's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

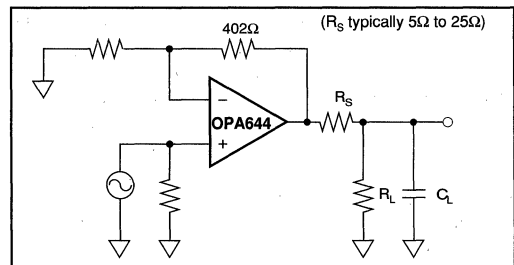


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA644 is internally compensated and is stable in unity gain with a phase margin of approximately 70°. (Note that, from a stability standpoint, an inverting gain of $-1V/V$ is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves. The high-frequency response of the OPA644 in a good layout is very flat with frequency.

DISTORTION

The OPA644's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

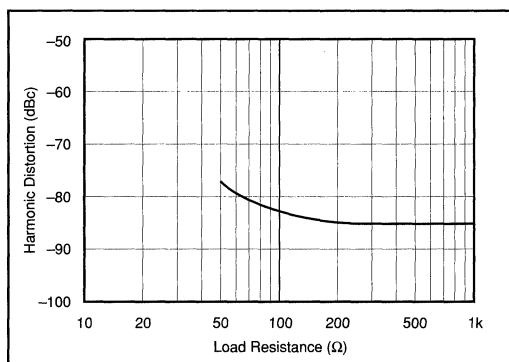


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept is an important parameter for many RF amplifier applications. Figure 6 shows the OPA644's single tone, third-order intercept vs frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA644 to operate in a gain of $+2V/V$ and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 6 we find that the intercept point is +50dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(\text{OPI}^3\text{P} - P_o)$$

where OPI^3P = third-order output intercept, dBm

P_o = output level, dBm

For this case $\text{OPI}^3\text{P} = 60\text{dBm}$, $P_o = 10\text{dBm}$, and the third Harmonic $= 2(50 - 10) = 80\text{dB}$ below the fundamental. The OPA644's low distortion makes the device an excellent choice for a variety of RF signal processing applications.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA644 were measured with the amplifier in a gain of $+2V/V$ with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA644 is 0.008% differential gain and 0.009° differential phase to both NTSC and PAL standards.

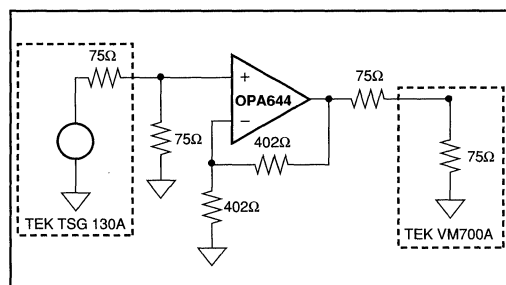


FIGURE 7. Configuration for Testing Differential Gain/Phase.

NOISE FIGURE

The OPA644's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA644's Noise Figure vs Source Resistance is shown in Figure 8.

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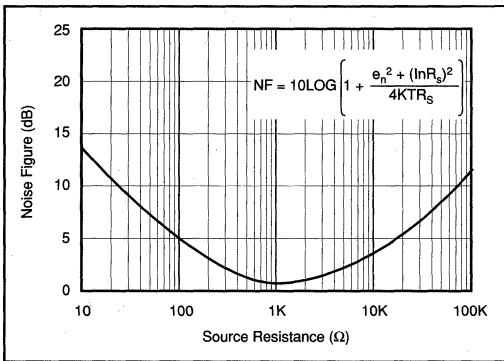


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA644. Contract Burr-Brown applications departments to receive a SPICE Diskette.

APPLICATIONS

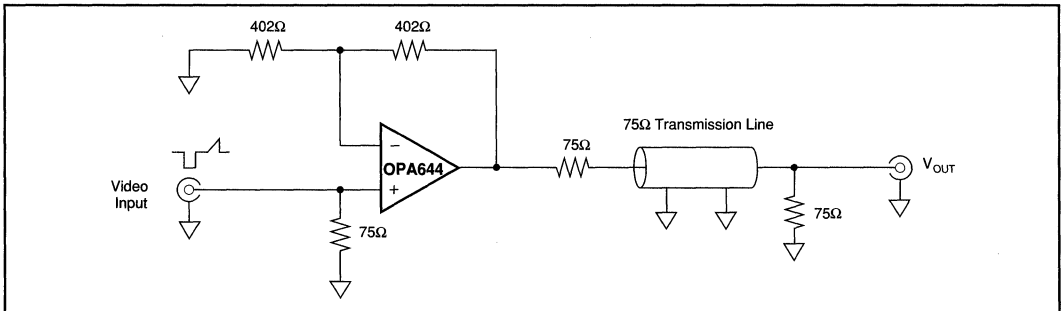


FIGURE 9. Low Distortion Video Amplifier.

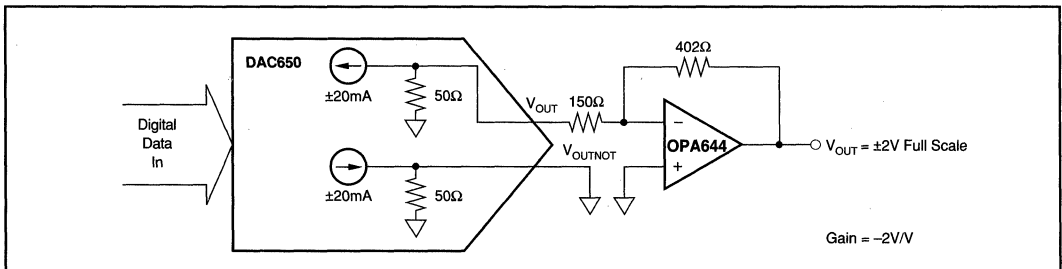


FIGURE 10. Output Amplification for the DAC650.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5×10^{-8} atm cc/s, 30pPSiG Gross: Perfluorocarbon bubble test, 30pPSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x datasheet for details.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

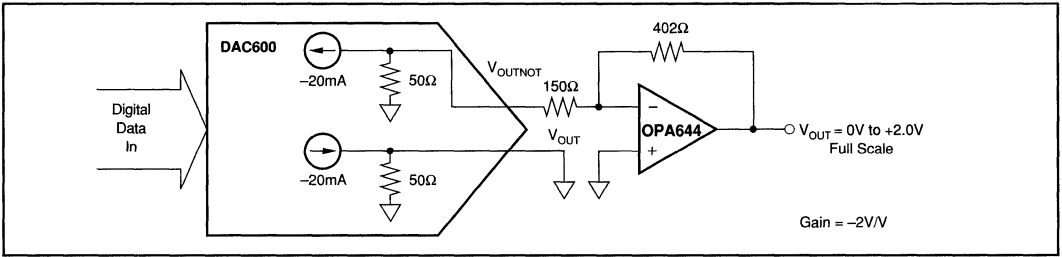


FIGURE 11. Output Amplification for the DAC600.

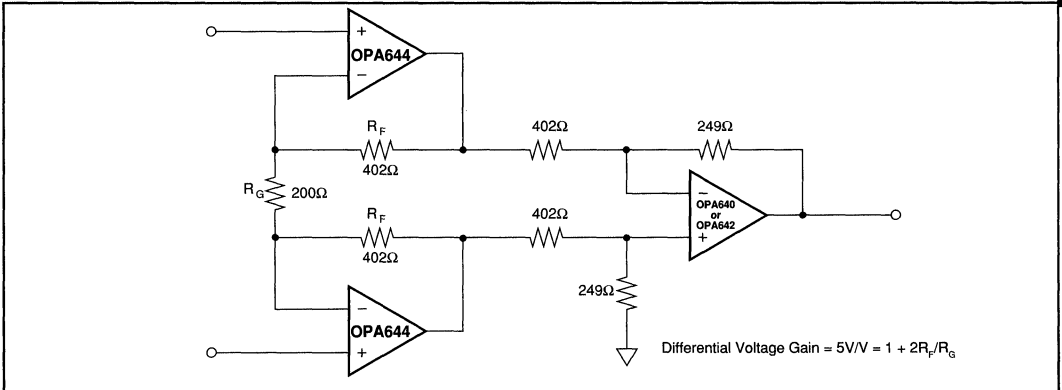


FIGURE 12. Wideband, Fast-Settling Instrumentation Amplifier.

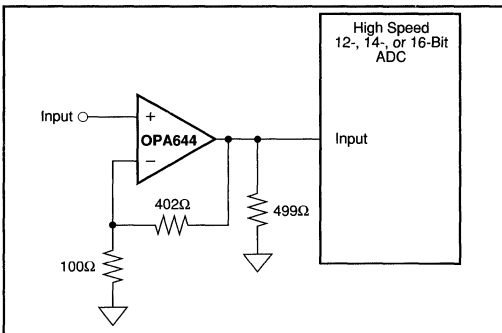
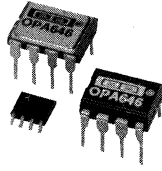


FIGURE 13. Low Distortion Gain Amplifier ($G = +5V/V$).

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OPA646

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

Low Power, Wide Bandwidth OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER:** 55mW
- **UNITY-GAIN BANDWIDTH:** 650MHz
- **UNITY-GAIN STABLE**
- **FAST 12-BIT SETTling:** 15ns (0.01%)
- **LOW INPUT BIAS CURRENT:** 2 μ A
- **LOW HARMONICS:** -82dBc at 5MHz
- **LOW DIFF GAIN/PHASE ERRORS:** 0.025%/0.08°

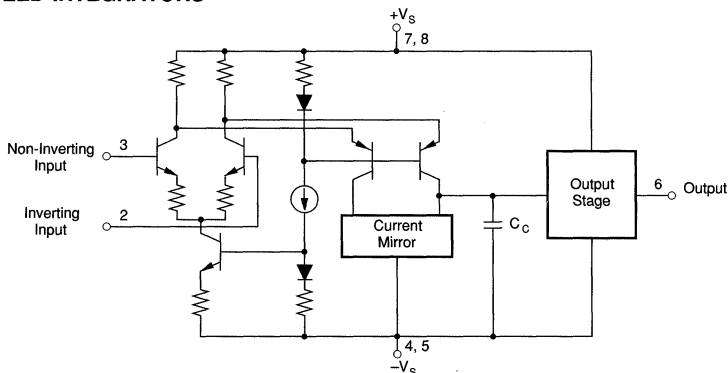
APPLICATIONS

- TELECOMMUNICATIONS
- MEDICAL IMAGING
- CCD IMAGING
- PORTABLE EQUIPMENT
- ACTIVE FILTERS
- VIDEO AMPLIFICATION
- ADC/DAC GAIN AMPLIFIER
- HIGH SPEED INTEGRATORS

DESCRIPTION

The OPA646 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 650MHz as well as a 12-bit settling time of only 15ns. Its low input bias current and wide bandwidth allows it to be used for high speed integrator and active filter designs. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA646 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an ideal choice for many portable, multichannel and other high speed applications where power is at a premium.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			± 3	± 8		± 1	± 2.5	mV
Average Drift			± 20			± 12		$\mu\text{V}/^\circ\text{C}$
HSQ Grade Over Temperature						± 5	± 8	mV
Power Supply Rejection (+ V_S)	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$	50	70		60	*		dB
Power Supply Rejection (- V_S)		45	55		48	*		dB
INPUT BIAS CURRENT								
Input Bias Current	$V_{CM} = 0\text{V}$		2	5		*	3.5	μA
Over Specified Temperature			3	7		*	*	μA
HSQ Grade Over Temperature						4	10	μA
Input Offset Current	$V_{CM} = 0\text{V}$		0.4	1.5		*	*	μA
Over Specified Temperature			0.9	3.0		*	*	μA
HSQ Grade Over Temperature						1.5	5.0	μA
NOISE								
Input Voltage Noise								
Noise Density: $f = 100\text{Hz}$			23.2			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			7.5			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz}$			7.1			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{MHz to } 100\text{MHz}$			7.2			*		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise, BW = 100Hz to 100MHz			141			*		μVrms
Input Bias Current Noise						*		
Current Noise Density, $f = 0.1\text{Hz to } 20\text{kHz}$			1.1			*		$\text{pA}/\sqrt{\text{Hz}}$
Noise Figure (NF)						*		dB
$R_S = 10\text{k}\Omega$			3.0			*		dB
$R_S = 50\Omega$			19.1			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			± 2.5	± 3.0		*	*	V
Over Specified Temperature			± 2.5	± 3.0		*	*	V
Common-Mode Rejection	$V_{CM} = \pm 0.5\text{V}$	60	80		75	90		dB
INPUT IMPEDANCE								
Differential			15 1			*		k Ω pF
Common-Mode			1.6 1			*		M Ω pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	$V_O = \pm 2\text{V}$, $R_L = 100\Omega$	45	51		47	55		dB
Over Specified Temperature		43	49		45	53		dB
FREQUENCY RESPONSE, $R_{FB} = 402\Omega$	All Four Power Pins Used							
Closed-Loop Bandwidth	$G = +1\text{V}/\text{V}$		650			*		MHz
	$G = +2\text{V}/\text{V}$		160			*		MHz
	$G = +5\text{V}/\text{V}$		45			*		MHz
	$G = +10\text{V}/\text{V}$		22			*		MHz
Slew Rate ⁽¹⁾	$G = +1$, 2V Step		180			*		V/ μs
At Minimum Specified Temperature			155			*		V/ μs
Rise Time	1V Step		5.3			*		ns
Fall Time	1V Step		5.9			*		ns
Settling Time: 0.01%	$G = +1$, 2V Step		15			*		ns
0.1%	$G = +1$, 2V Step		11.5			*		ns
1%	$G = +1$, 2V Step		6			*		ns
Over-Voltage Recovery (2)			65			*		ns
Spurious Free Dynamic Range	$G = +1$, $f = 5.0\text{MHz}$		82			*		dBc
Differential Gain Error at 3.58MHz	$V_O = 2\text{Vp-p}$, $R_L = 402\Omega$					*		%
Differential Phase Error at 3.58MHz	$G = +2\text{V}/\text{V}$, $V_O = 0$ to 1.4V, $R_L = 150\Omega$		0.025			*		degrees
Gain Flatness to 0.1dB	$G = +2\text{V}/\text{V}$, $V_O = 0$ to 1.4V, $R_L = 150\Omega$		0.08			*		degrees
			100			*		MHz
OUTPUT								
Voltage Output	No Load					*	*	V
Over Specified Temperature		± 2.5	± 2.75		± 2.3	± 2.5		V
HSQ Grade Over Temperature								V
Voltage Output	$R_L = 250\Omega$					*	*	V
Over Specified Temperature		± 2.5	± 2.7		± 2.0	± 2.5		V
HSQ Grade Over Temperature								V
Voltage Output	$R_L = 100\Omega$					*	*	V
Over Specified Temperature		± 2.0	± 2.5		± 2.0	± 2.3		V
HSQ Grade Over Temperature								V
Current Output, +25°C to max Temp		± 40	± 52		*	*		mA
Over Specified Temperature		± 30	± 48		*	*		mA
HSQ Grade Over Temperature					± 25	± 35		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, $G = +1\text{V}/\text{V}$		0.2			*		Ω

OPA646

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OPERATIONAL AMPLIFIERS

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SPECIFICATIONS (CONT.)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current Over Specified Temperature HSQ Grade Over Temperature	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}	±4.5	±5	±5.5	*	*	*	V	
			±5.25	±6.5		*	*	mA	
			±6.5	±7.5		*	*	mA	
						±7.5		±8.5	mA
									mA
TEMPERATURE RANGE Specification: H, P, PB, U, UB HSQ Thermal Resistance P U H	Ambient Ambient θ_{JA} , Junction to Ambient	-40		+85	*		*	$^\circ\text{C}$	
					-55		+125	$^\circ\text{C}$	
			120			*			$^\circ\text{C}/\text{W}$
			170			*			$^\circ\text{C}/\text{W}$
			120			*			$^\circ\text{C}/\text{W}$

NOTE: (1) Slow rate is rate of change from 10% to 90% of output voltage step. (2) Recovery time to linear operation after a 50% overload recovery.

ORDERING INFORMATION

Basic Model Number	OPA646	()	()
Package Code			
H = 8-pin Sidebraze DIP			
P = 8-pin Plastic DIP			
U = 8-pin Plastic SOIC			
Performance Grade Code			
SQ = -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$, Reliability Screened			
B ⁽¹⁾ or No Letter = -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$			

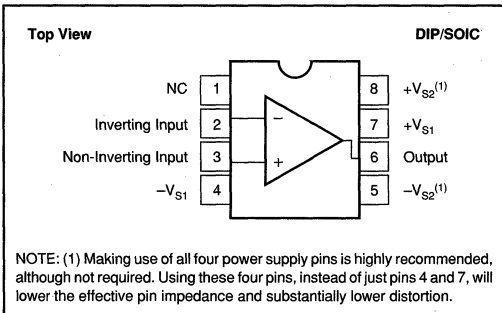
NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
P, PB, U, UB	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$
(soldering, SOIC 3s)	+260 $^\circ\text{C}$
Junction Temperature (T_J)	+175 $^\circ\text{C}$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_J must be observed.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA646H, HSQ	8-Pin Cerdip	157
OPA646P, PB	8-Pin DIP	006
OPA646U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

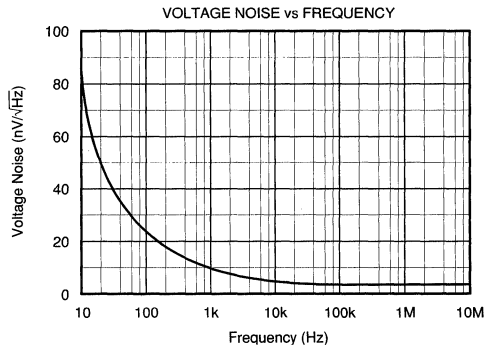
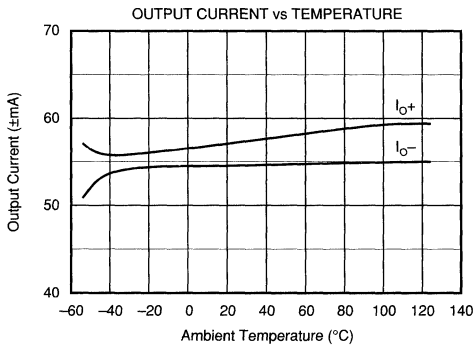
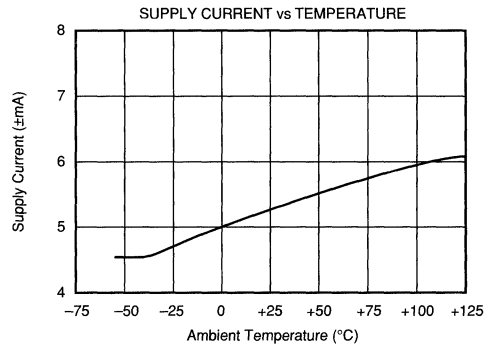
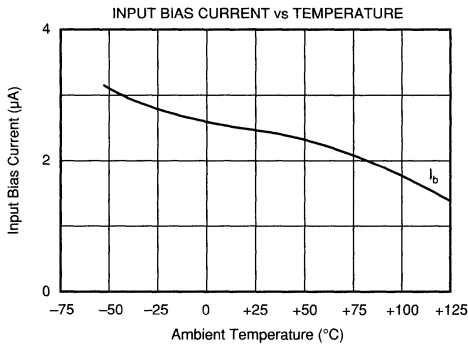
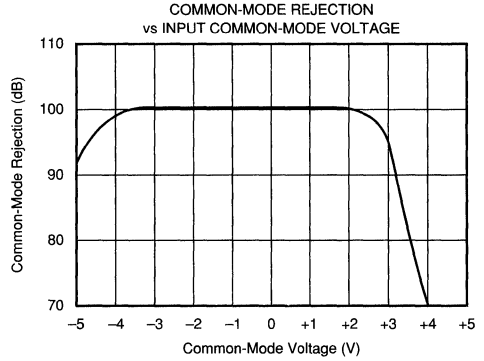
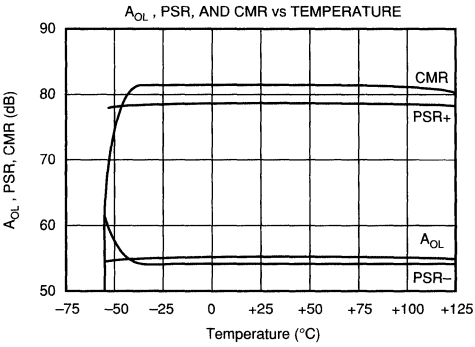
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

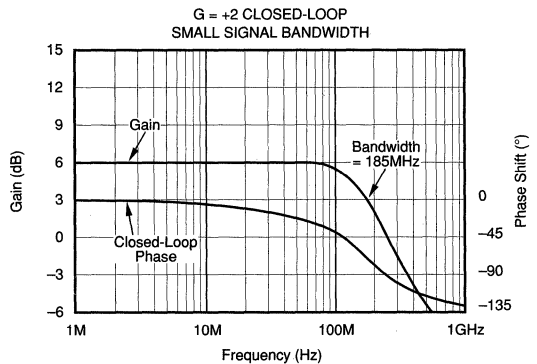
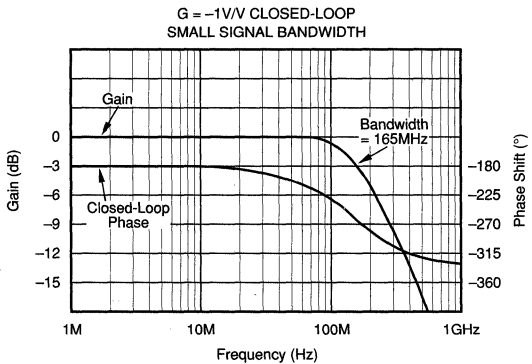
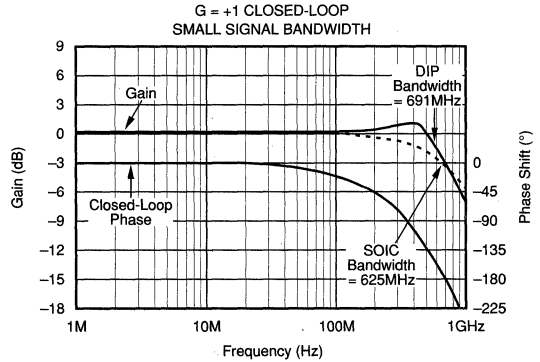
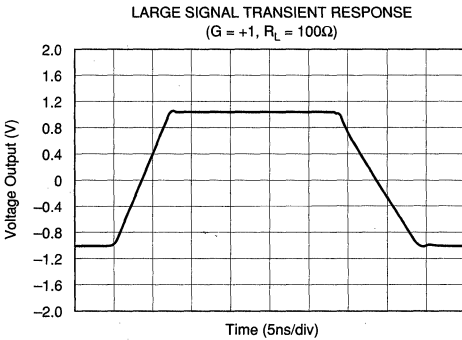
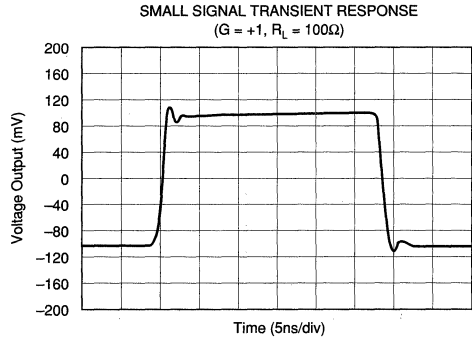
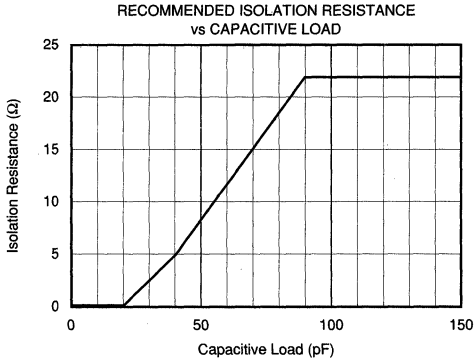
$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



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TYPICAL PERFORMANCE CURVES (CONT.)

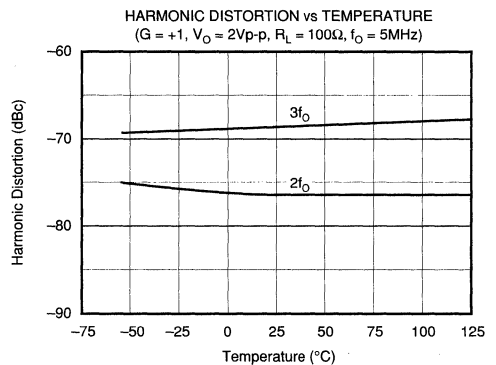
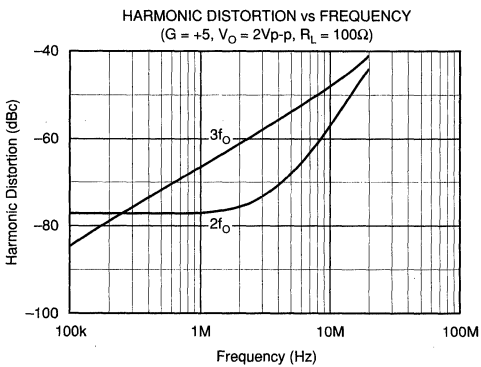
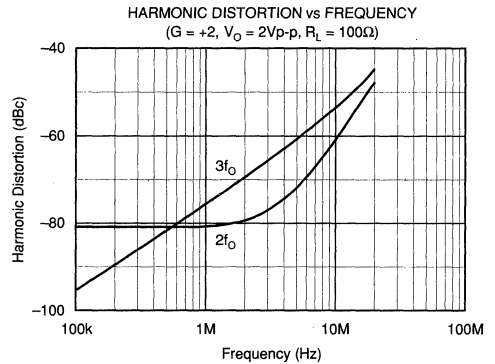
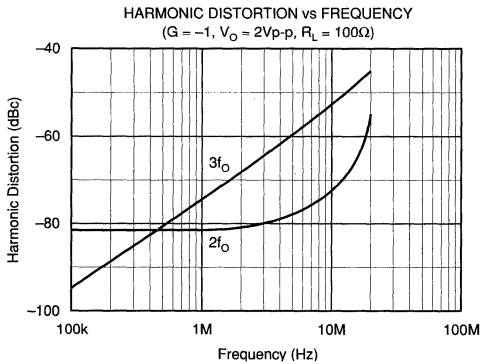
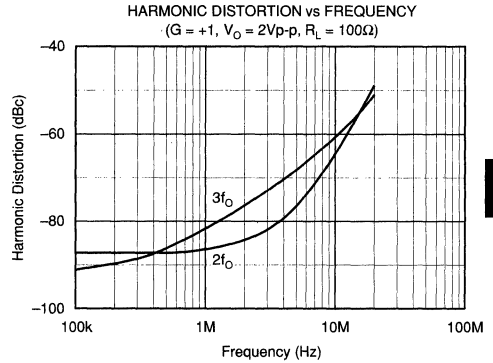
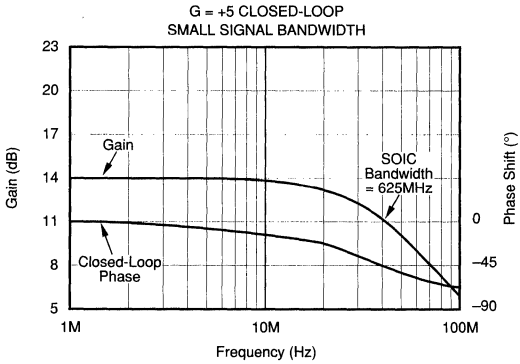
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TYPICAL PERFORMANCE CURVES (CONT.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



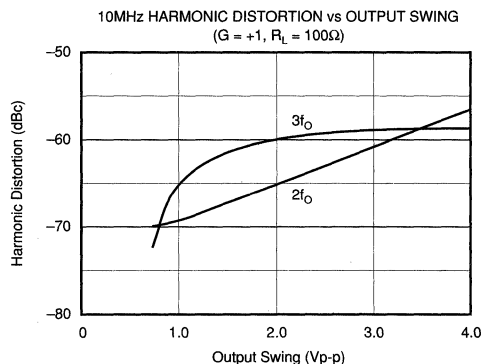
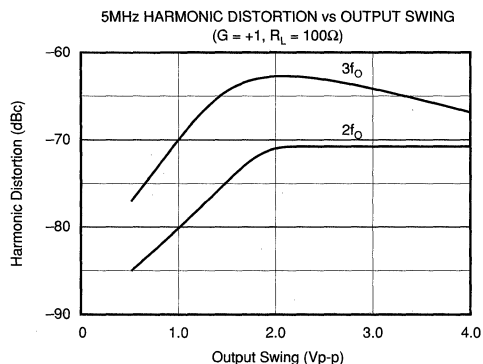
OPA646

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OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT.)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 402\Omega$ and all four power supply pins are used unless otherwise noted. $R_{FB} = 25\Omega$ for a gain of +1.



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA646 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA646's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA646's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA646.

WIRING PRECAUTIONS

Maximizing the OPA646's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and

instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA646, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μF) with very short leads are recommended. A parallel 0.01 μF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to

isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors on the topside of the PC Board is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the DEM-OPA64X Data Sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA646 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the datasheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA646U (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and -5.2V, use of $\pm 15V$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA646's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3 . This will reduce input bias current errors to the amplifier's offset current.

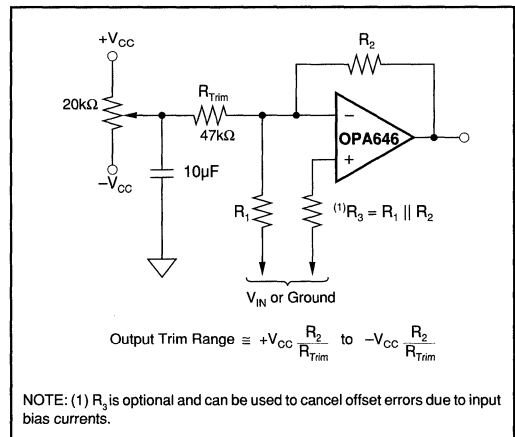


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection

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from this potentially damaging source. The OPA646 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA646 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

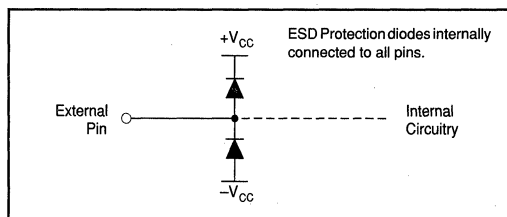


FIGURE 2. Internal ESD Protection.

The OPA646 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA646.

OUTPUT DRIVE CAPABILITY

The OPA646 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA646 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are not needed.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA646 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

THERMAL CONSIDERATIONS

The OPA646 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 7.5mA = 75mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

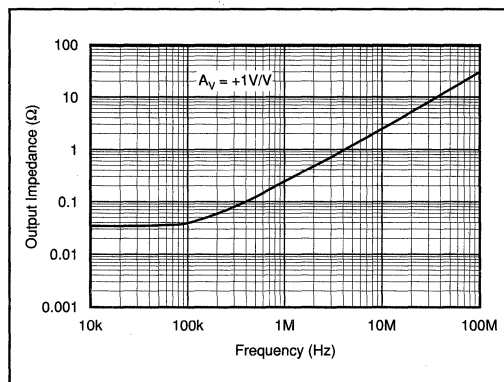


FIGURE 3. Small-Signal Output Impedance vs Frequency.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

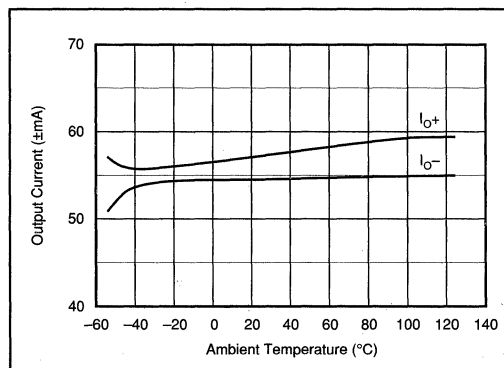


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA646's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

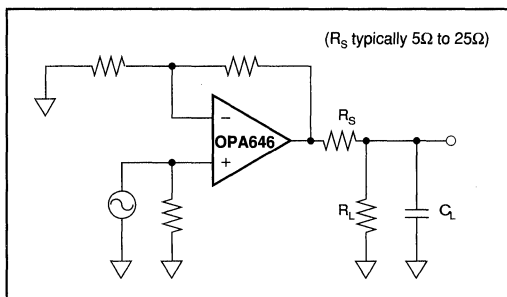


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA646 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of -1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA646 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve

the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of $\pm 200\mu\text{V}$ centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA646 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 65ns.

In practice, settling time measurements on the OPA646 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA646's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

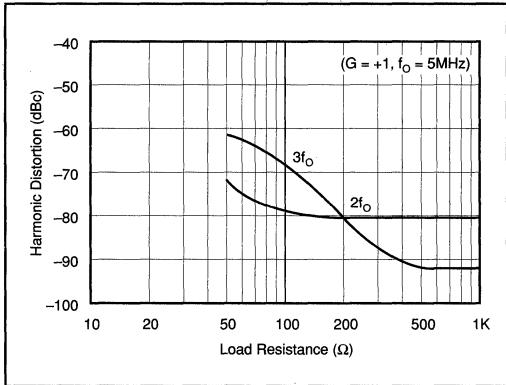


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance with $R_p = 402\Omega$.

NOISE FIGURE

The OPA646 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA646's Noise Figure vs Source Resistance is shown in Figure 7.

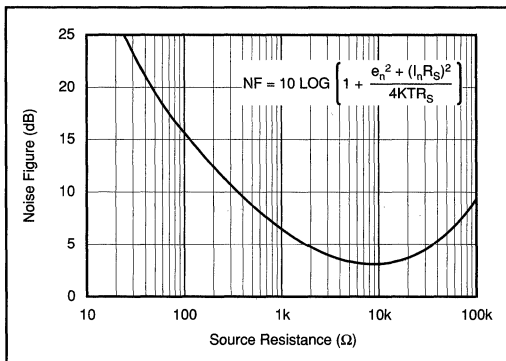


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA646. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" on the HSQ grade provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = -65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20000G
Hermetic Seal	Fine: He leak rate < 5×10^{-9} atm cc/s, 30PSIG Gross: Perfluorocarbon bubble test, 60PSIG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q Screening is available on the HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Data Sheet for details.

APPLICATIONS

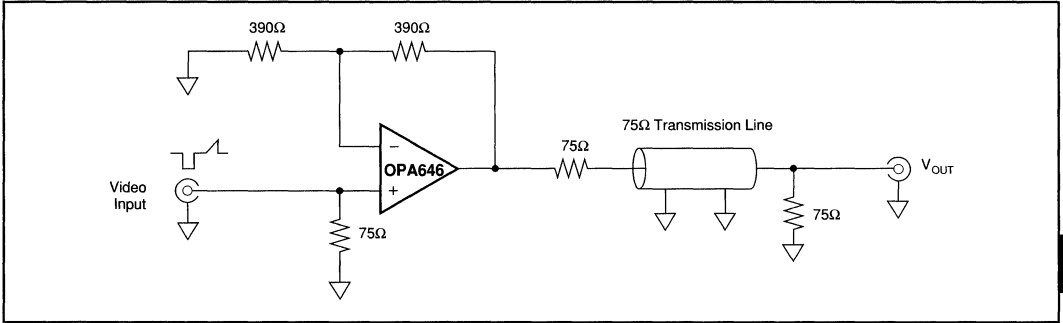


FIGURE 8. Low Power Video Amplifier.

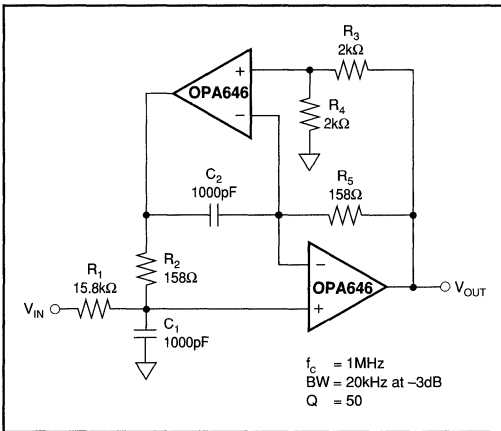


FIGURE 9. High-Q 1MHz Bandpass Filter.

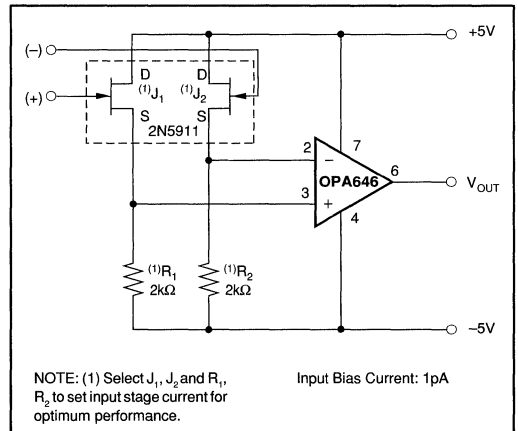


FIGURE 10. Low Power, Wideband FET Input Op Amp.

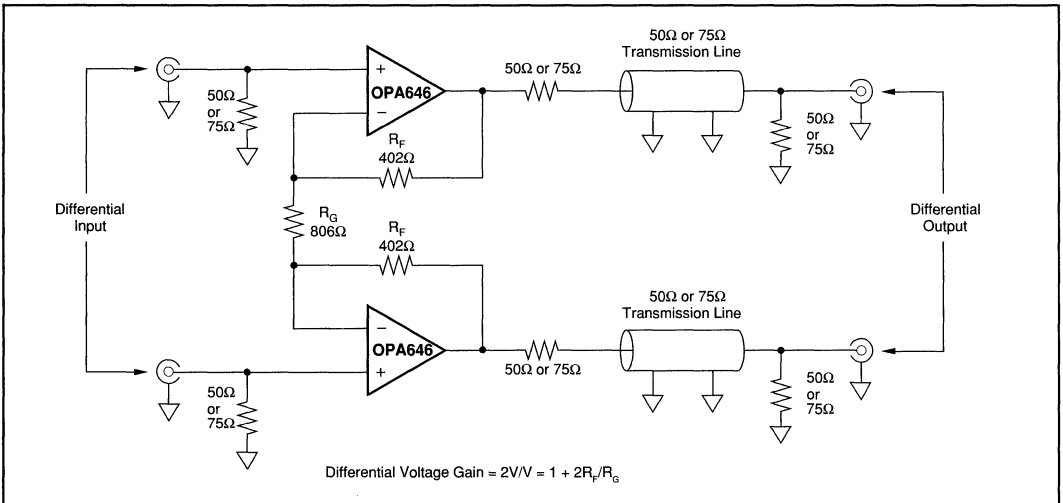


FIGURE 11. Differential Line Driver for 50Ω or 75Ω Systems.

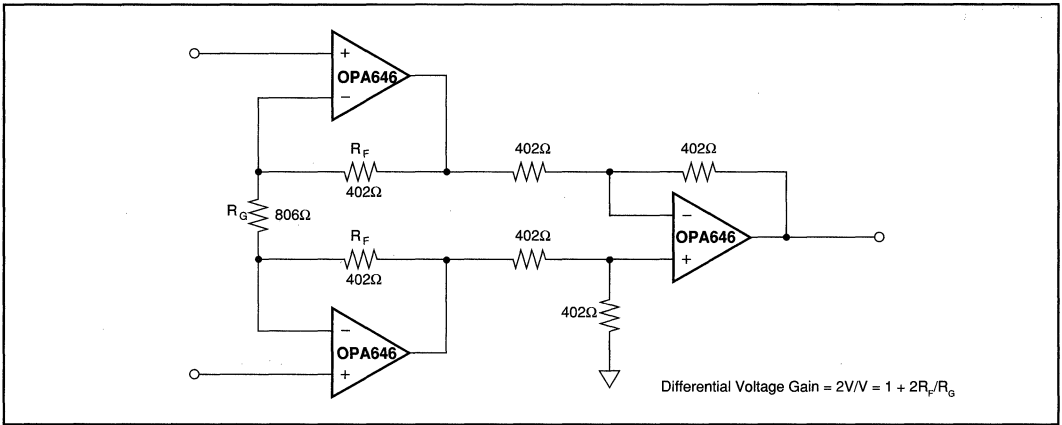


FIGURE 12. Wideband, Fast-Settling Instrumentation Amplifier.

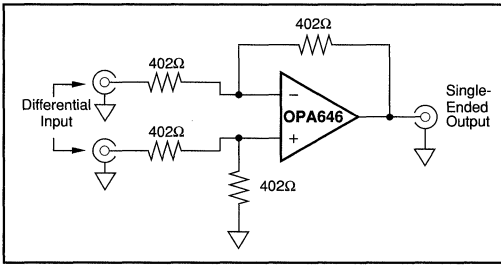


FIGURE 13. Unity Gain Difference Amplifier.

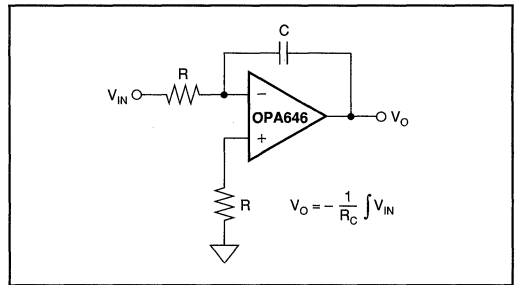


FIGURE 15. A High Speed Integrator.

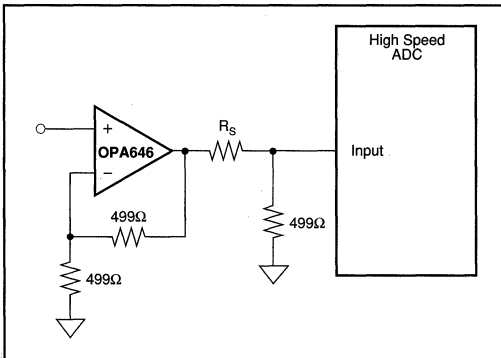


FIGURE 14. Differential Input Buffer Amplifier ($G = +2V/V$).

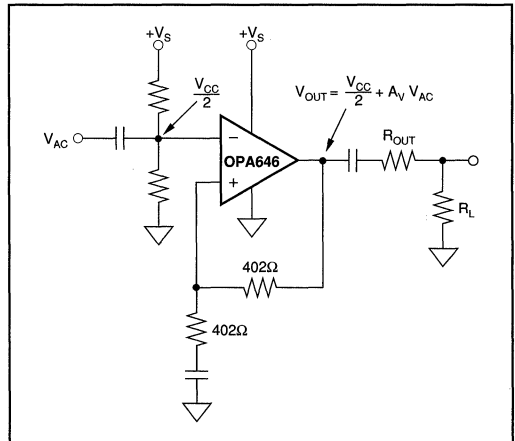
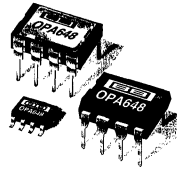


FIGURE 16. Single Supply Operation.

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OPA648

DEMO BOARD AVAILABLE
See Appendix A,
Burr-Brown IC Data Book—
Data Conversion Products

ULTRA-WIDEBAND CURRENT FEEDBACK OPERATIONAL AMPLIFIER

FEATURES

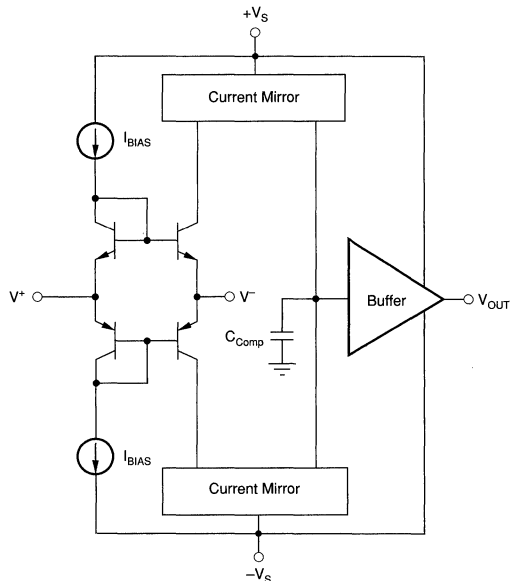
- WIDE BANDWIDTH: 1GHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%/0.02°
- GAIN FLATNESS: 0.1dB to 100MHz
- FAST SLEW RATE: 1200V/ μ s
- CLEAN PULSE RESPONSE
- UNITY GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION CRT PREAMP
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- IF SIGNAL PROCESSING
- DAC I/V CONVERSION
- ADC BUFFER

DESCRIPTION

The OPA648 is an ultra high bandwidth current feedback operational amplifier. The current feedback architecture also allows for a very high slew rate, which gives excellent large signal bandwidth, even at high gains. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA648 offers exceptional performance in monolithic form.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (602) 548-6132



PDS-1253

2.301

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 243\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA648H, P, U			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
Small Signal Bandwidth ⁽¹⁾	G = +1		1.0		GHz
	G = +2		600		MHz
Slew Rate ⁽²⁾	G = +2, 1V Step		1200		V/ μs
Settling Time					
0.01%	G = +2, 1V Step		20		ns
0.1%	G = +2, 1V Step		9		ns
1%	G = +2, 1V Step		3		ns
Spurious Free Dynamic Range	G = +2, f = 5.0MHz, $V_O = 2\text{Vp-p}$		60		dBc
	G = +2, f = 20.0MHz, $V_O = 2\text{Vp-p}$		51		dBc
Differential Gain, G = +2	3.58MHz, $V_O = 1.4\text{Vp-p}$, $R_L = 150\Omega$		0.02		%
Differential Phase, G = +2	3.58MHz, $V_O = 1.4\text{Vp-p}$, $R_L = 150\Omega$		0.02		degrees
Gain Flatness	DC to 100MHz		0.1		dB
OFFSET VOLTAGE					
Input Offset Voltage			± 2	± 6	mV
Average Drift			± 10		$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection Ratio	$V_S = \pm 4.5$ to $\pm 5.5\text{V}$	45	58		dB
INPUT BIAS CURRENT					
Non-Inverting			± 12	± 65	μA
Over Specified Temperature			± 30	± 95	μA
Inverting			± 20	± 65	μA
Over Specified Temperature			± 50	± 95	μA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			10.4		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			2.3		$\text{nV}/\sqrt{\text{Hz}}$
f = 10kHz			2.3		$\text{nV}/\sqrt{\text{Hz}}$
f = 1MHz			2.3		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise, BW = 10Hz to 200MHz			32.5		μVrms
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			15		$\text{pA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-mode Input Range		± 2	± 2.25		V
Common-mode Rejection	$V_{CM} = 0.5$	35	55		dB
INPUT IMPEDANCE					
Non-inverting			$22 \parallel 0.75$		$\text{k}\Omega \parallel \text{pF}$
Inverting			20		Ω
OPEN-LOOP TRANSIMPEDANCE					
Open-Loop Transimpedance	$V_O = \pm 2\text{V}$, $R_L = 1\text{k}\Omega$	100	165		$\text{k}\Omega$
OUTPUT					
Current Output		33	42		mA
Over Specified Temperature		25	40		mA
Voltage Output	No Load				
Over Specified Temperature		± 2.75	± 3.0		V
Voltage Output	$R_L = 150\Omega$	± 2.2	± 2.5		V
Over Specified Temperature		± 2.0	± 2.3		V
Short Circuit Current			75		mA
Output Resistance	1MHz, G = +2V/V		0.08		Ω
POWER SUPPLY					
Specified Operating Voltage	T_{MIN} to T_{MAX}		± 5		V
Operating Voltage Range	T_{MIN} to T_{MAX}	± 4.5		± 5.5	V
Quiescent Current			± 13	± 20	mA
Over Specified Temperature			± 15	± 23	mA
TEMPERATURE RANGE					
Specification	Ambient	-40		+85	$^\circ\text{C}$
Storage	Ambient	-55		+150	$^\circ\text{C}$
Thermal Resistance, θ_{JA}					
P			120		$^\circ\text{C}/\text{W}$
U			170		$^\circ\text{C}/\text{W}$
H			120		$^\circ\text{C}/\text{W}$

NOTES: (1) Bandwidth can be degraded by a non-optimal PC board layout. Refer to the DEM-OPA64x datasheet for layout recommendations. (2) Slew rate is the rate of change from 10% to 90% of the output voltage step.

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ABSOLUTE MAXIMUM RATINGS

Supply	± 5.5 VDC
Internal Power Dissipation ⁽¹⁾	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H	-65°C to $+150^{\circ}\text{C}$
P	-40°C to $+125^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
(soldering, SOIC 3s)	$+260^{\circ}\text{C}$
Junction Temperature (T_j)	$+175^{\circ}\text{C}$

NOTE: (1) Packages must be derated based on specified θ_{JA} . Maximum T_j must be observed.

ORDERING INFORMATION

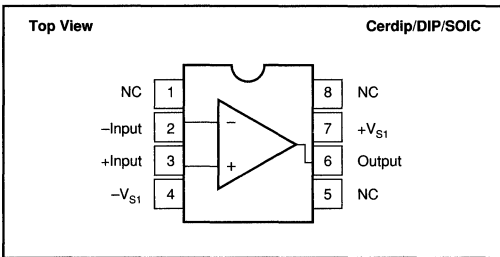
Basic Model Number	OPA648	()
Package Code	_____	
H = 8-pin Sidebraze DIP		
P = 8-pin Plastic DIP		
U = 8-pin Plastic SOIC		

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA648H	8-Pin Cerdip	157
OPA648P	8-Pin DIP	006
OPA648U	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION (All Packages)



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

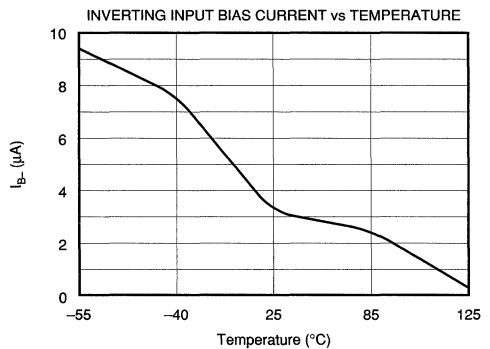
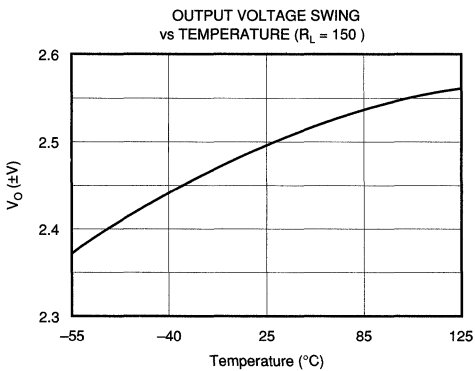
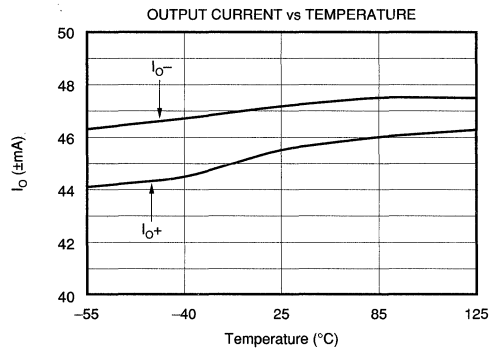
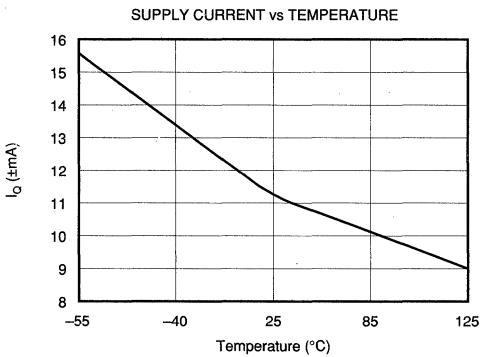
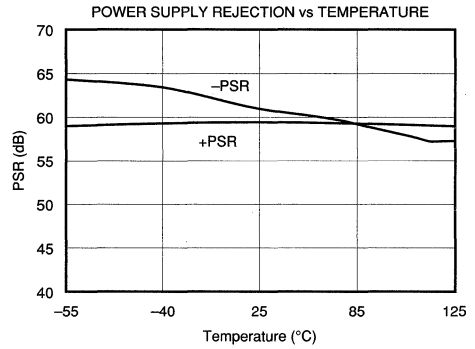
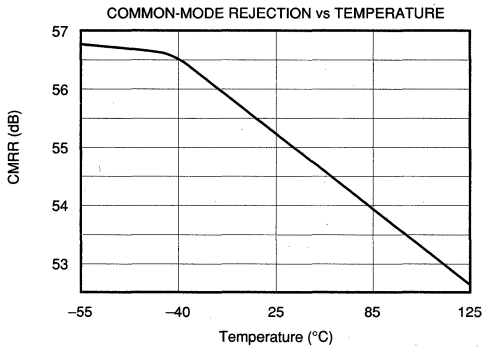
OPA648
2
OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES

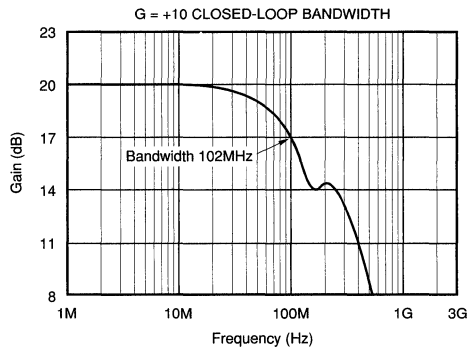
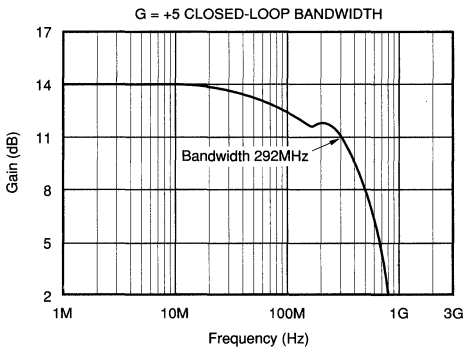
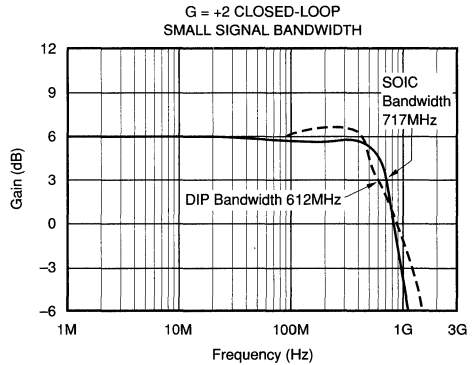
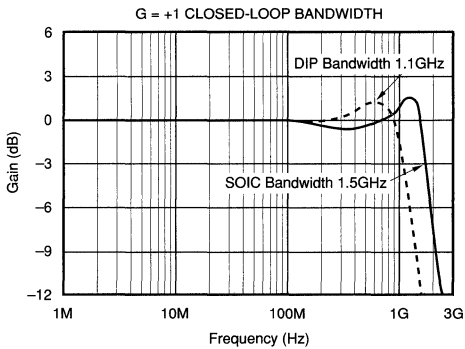
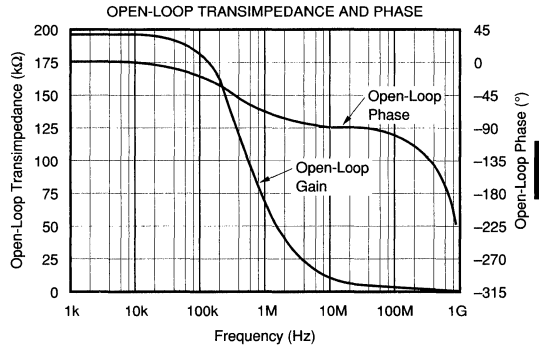
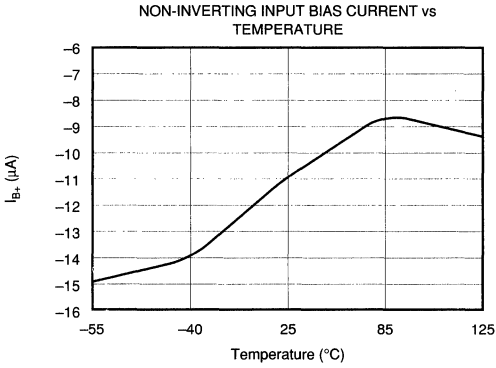
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TYPICAL PERFORMANCE CURVES (CONT)

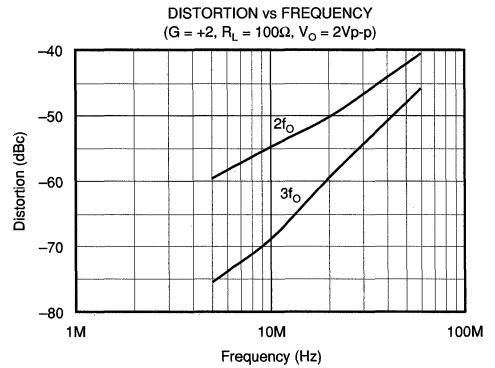
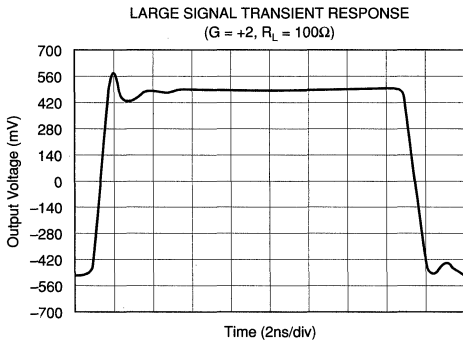
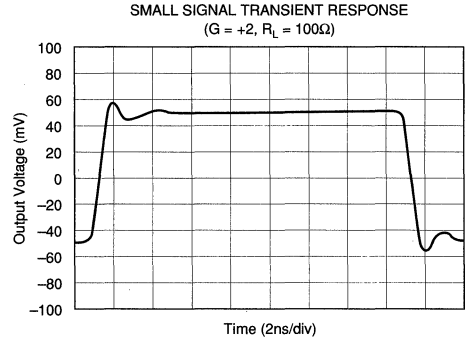
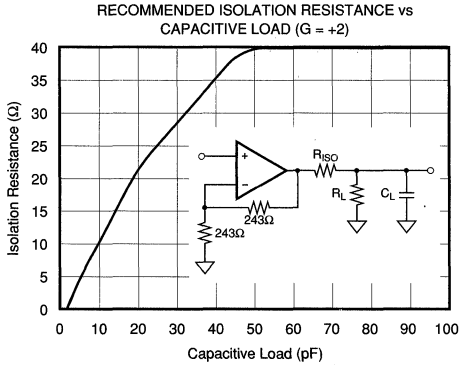
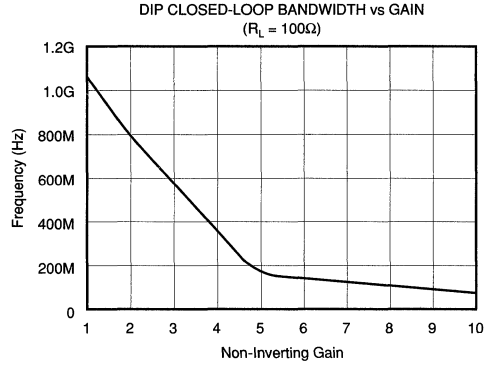
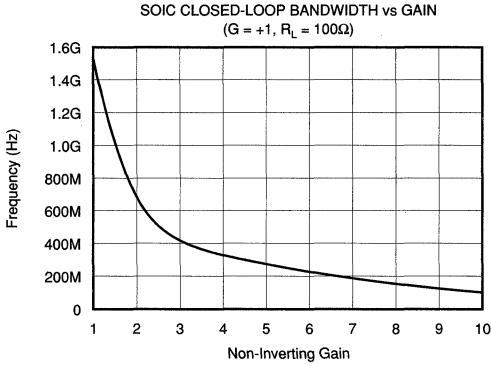
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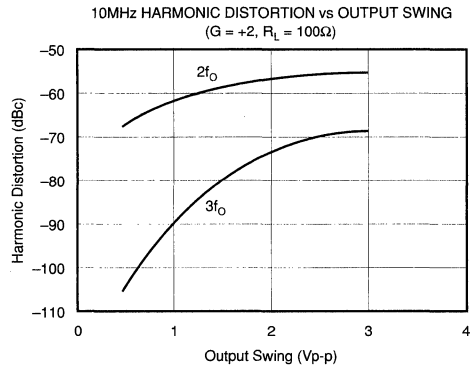
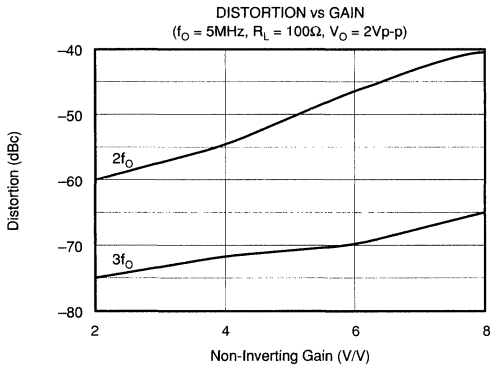
TYPICAL PERFORMANCE CURVES (CONT)

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 100\Omega$, $C_L = 2\text{pF}$, $R_{FB} = 243\Omega$ unless otherwise noted.



APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is less bandwidth degradation at higher gain settings.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

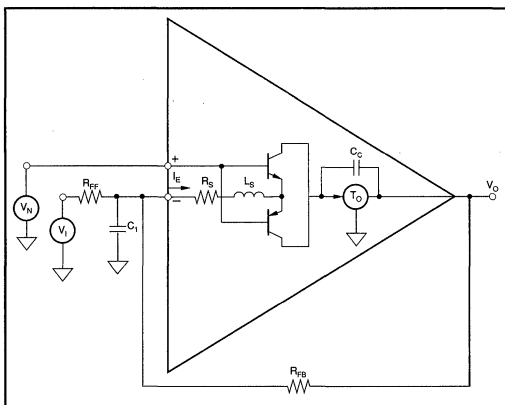


FIGURE 1. Equivalent Circuit

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_L)$.

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA648 can be calculated using the following equations:

$$\text{Inverting Gain} = (-R_{FB}/R_{FF})/(1+1/\text{Loop Gain}) \quad (1)$$

$$\text{Non-inverting Gain} = (1 + R_{FB}/R_{FF})/(1 + 1/\text{Loop Gain}) \quad (2)$$

$$\text{where: Loop Gain} = T(o)/(R_{FB}) \times (1/(1+T(o)/(R_{FB}/R_{FF})))$$

At higher gains the small value inverting input impedance (R_{INV}) causes an apparent loss in bandwidth. This can be seen from the equation:

$$\text{Factual} = F_{\text{IDEAL}}/(1 + (R_{INV}/R_{FB}) (1 + R_{FB}/R_{FF})) \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 243Ω .

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

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$$\text{Output Offset Voltage} = \pm I_{bN} \times R_N (1 + R_{FB}/R_G) \pm V_{IO} (4) \\ (1 + R_{FB}/R_G) \pm I_{bI} \times R_{FB}$$

If all terms are divided by the gain $(1 + R_F/R_G)$ it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

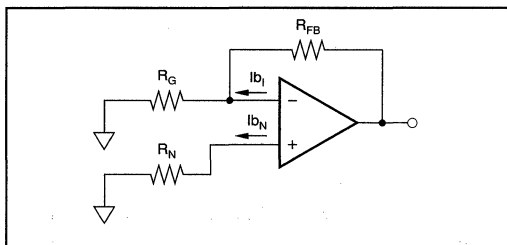


FIGURE 2. Output Offset Voltage Equivalent Circuit.

WIRING PRECAUTIONS

Maximizing the OPA648's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA648, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be

used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2 μ F) with very short leads are recommended. A parallel 0.01 μ F ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

- 1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2} . Power supply bypassing with 0.01 μ F and 2.2 μ F surface mount capacitors is recommended. It is essential to keep the 0.01 μ F capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X datasheet for the recommended layout and component placements.
- 2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 4) Whenever possible, solder the OPA648 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.
- 5) Use a small feedback resistor (usually 25 Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the datasheet.

6) Surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA648U (SOIC package) will offer the best AC performance. The parasitic package impedance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and -5.2V, use of $\pm 15V$ supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA648's speed range. Bench-top op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA648 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

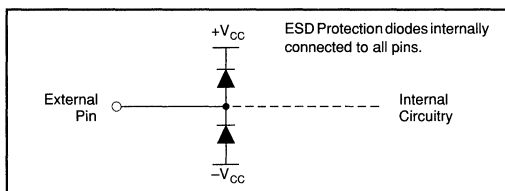


FIGURE 3. Internal ESD Protection.

All pins on the OPA648 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA648 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA648.

OUTPUT DRIVE CAPABILITY

The OPA648 has been optimized to drive 75Ω and 100Ω resistive loads. This high-output drive capability makes the OPA648 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA648 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

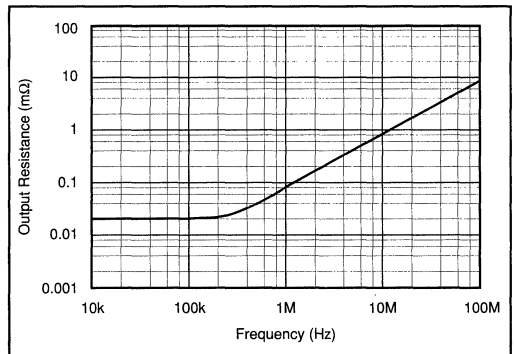


FIGURE 4. Output Resistance vs Frequency (G=+2).

THERMAL CONSIDERATIONS

The OPA648 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC} / 2$, and is equal to $P_{DL, max} = (\pm V_{CC})^2 / 4R_L$. Note that it is the voltage across the

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output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA648's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

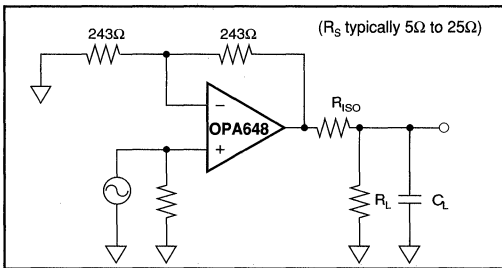


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA648 is internally compensated and is stable in unity gain with a phase margin of approximately 68°. (Note that, from a stability standpoint, an inverting gain of -1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA648 in a good layout is very flat with frequency.

DISTORTION

The OPA648's Harmonic Distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

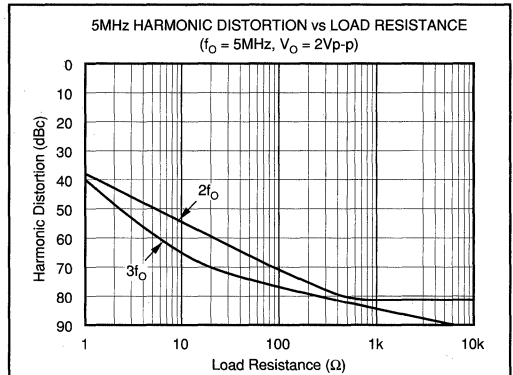


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA648 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA648 is 0.02% differential gain and 0.02° differential phase to both NTSC and PAL standards.

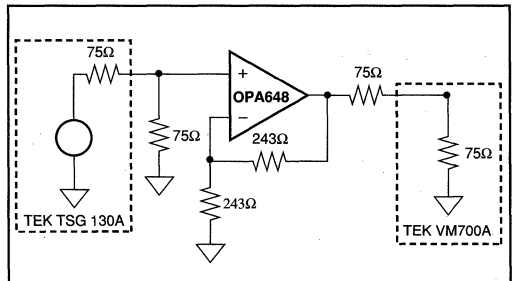


FIGURE 7. Configuration for Testing Differential Gain/Phase.

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NOISE FIGURE

The OPA648's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA648's Noise Figure vs Source Resistance is shown in Figure 8.

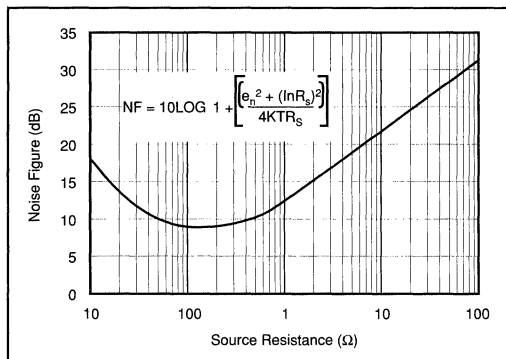


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA648. Contact Burr-Brown applications departments to receive a SPICE Diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64x datasheet for details.

APPLICATIONS

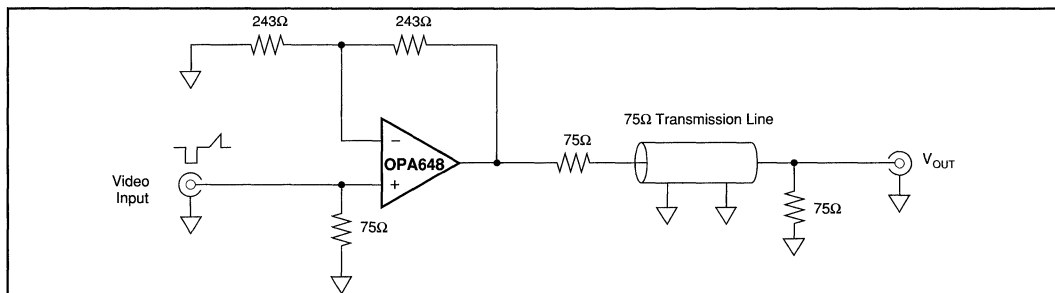


FIGURE 9. Low Distortion Video Amplifier.

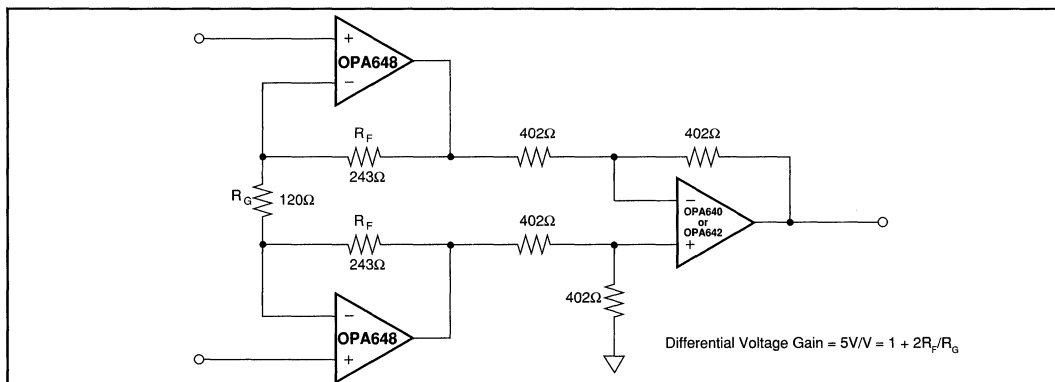
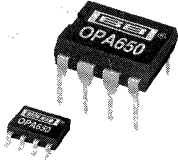


FIGURE 10. Wideband, Fast-Settling Instrumentation Amplifier.

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OPA650

PRELIMINARY INFORMATION
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Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER:** 50mW
- **UNITY GAIN STABLE BANDWIDTH:** 560MHz
- **FAST SETTLE TIME:** 15ns to 0.01%
- **LOW INPUT BIAS CURRENT:** 2.7 μ A
- **DIFFERENTIAL GAIN/PHASE ERROR:** 0.01%/0.01°
- **PACKAGE:** 8-Pin DIP and 8-Pin SOIC

APPLICATIONS

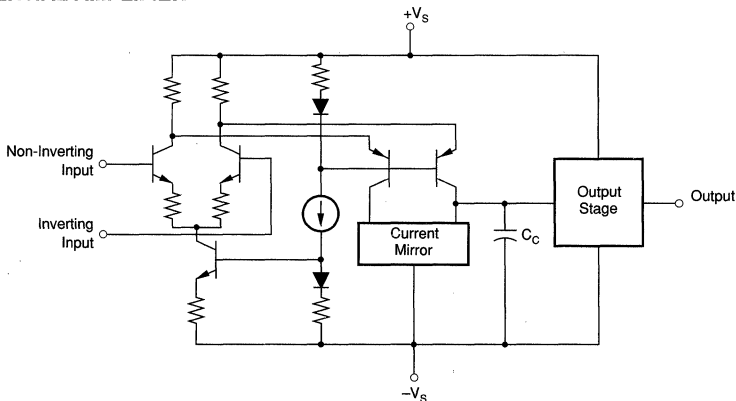
- **HIGH RESOLUTION VIDEO**
- **MONITOR PREAMPLIFIER**
- **CCD IMAGING AMPLIFIER**
- **ULTRASOUND SIGNAL PROCESSING**
- **ADC/DAC GAIN AMPLIFIER**
- **ACTIVE FILTERS**
- **HIGH SPEED INTEGRATORS**
- **DIFFERENTIAL AMPLIFIER**

DESCRIPTION

The OPA650 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 15ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA650 is also available in dual OPA2650 and quad OPA4650 configurations.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

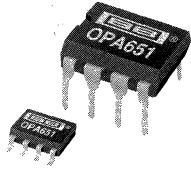
PARAMETER	CONDITIONS	OPA650P, U			OPA650PB, UB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
FREQUENCY RESPONSE Closed-Loop Bandwidth ⁽²⁾ Slew Rate ⁽³⁾ At Minimum Specified Temperature Rise Time Fall Time Settling Time 0.01% 0.1% 1% Spurious Free Dynamic Range Differential Gain Differential Phase Gain Flatness	G = +1 G = +2 G = +5 G = +10 G = +1, 2V Step		560 160 40 18 180			* ⁽¹⁾ * * * *	MHz MHz MHz MHz V/μs		
	G = +1, 2V Step		155 5.3 5.9 15 11.5 6 82			* * * * * * *	V/μs ns ns ns ns ns dBc		
	G = +1, 2V Step G = +1, 2V Step G = +1, 2V Step G = +1, f = 5.0 MHz V _O = 2Vp-p, R _L = 402Ω			0.01 0.01 0.01 0.01 0.1			* * * * *	% % ° ° dB	
	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω DC to 100MHz						* * * * *		
	INPUT OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection (+V _S) (-V _S)	V _S = ±4.5V to ±5.5V		±1 ±5 70 55	±3		±0.35 3 * *	±1 mV μV/°C dB	
	INPUT BIAS CURRENT Input Bias Current Over Temperature Input Offset Current Over Temperature	V _{CM} = 0V V _{CM} = 0V		2 3 0.4 0.9	5 7 1.5 3.0		* * * *	4 5.5 * *	μA μA μA μA
	NOISE Input Voltage Noise Noise Density, f = 100Hz f = 10kHz f = 1MHz f = 10Hz to 100MHz Voltage Noise, BW = 10Hz to 100MHz Input Bias Current Noise Current Noise Density, f = 0.1Hz to 20kHz Noise Figure (NF)	R _{FB} = 10kΩ R _S = 50Ω		23.2 7.5 7.1 72 141 1.1 3.0 19.0			* * * * * * * *	nV √Hz nV √Hz nV √Hz nVrms μVp-p pA √Hz dB dB	
	INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	V _{CM} = +2V		±2.2 60	±2.8 80		* *	85 V dB	
	INPUT IMPEDANCE Differential Common-Mode			15 1 16 1			* *	kΩ pF MΩ pF	
	OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature	V _O = ±2V, R _L = 100Ω V _O = ±2V, R _L = 100Ω		45 43	51 49		47 45	55 53	dB dB
	OUTPUT Voltage Output Over Specified Temperature Current Output Over Specified Temperature Short Circuit Current	No Load R _L = 250Ω R _L = 100Ω +25°C to Max Temperature		±2.5 ±2.5 ±2.0 ±40 ±30	±2.75 ±2.7 ±2.5 ±50 ±48 60		* * * ±43 ±52 *	±55 V V V mA mA mA	
	POWER SUPPLY Output Resistance Specified Operating Voltage Derated Voltage Range Quiescent Current Over Specified Temperature	1MHz, G = +1		0.2 ±5 ±4.5 ±5.1 ±5.4	±5.5 ±7.75 ±8.75		* * * ±4.9 ±5.2	* * * ±6.5 ±7.5m	Ω V V mA mA
TEMPERATURE RANGE Specification: P, U, PB, UB Thermal Resistance, θ _{JA} P U			-40 120 170	+85		* * *	* * *	°C °C/W °C/W	

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

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OPA651

PRELIMINARY INFORMATION
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Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER:** 50mW
- **GAIN BANDWIDTH:** 1GHz
- **STABLE IN GAINS:** $\geq 2V/V$
- **FAST SETTLING TIME:** 15ns to 0.01%
- **LOW INPUT BIAS CURRENT:** 2.7 μ A
- **DIFFERENTIAL GAIN/PHASE ERROR:** 0.01%/0.01°
- **PACKAGE:** 8-pin DIP and 8-pin SOIC

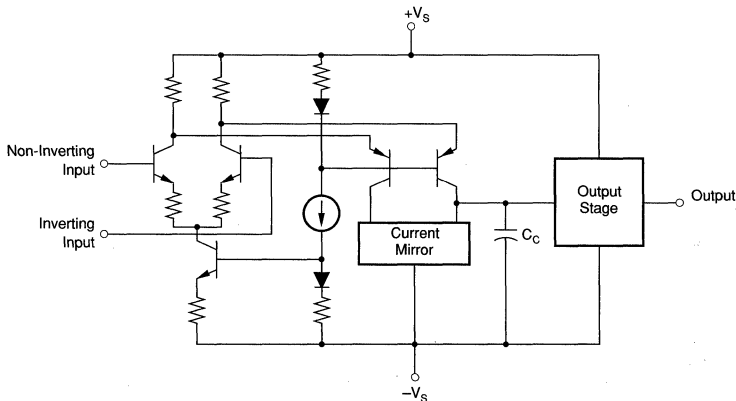
APPLICATIONS

- **HIGH RESOLUTION VIDEO**
- **MONITOR PREAMPLIFIER**
- **DIFFERENTIAL AMPLIFIER**
- **CCD IMAGING AMPLIFIER**
- **ULTRASOUND SIGNAL PROCESSING**
- **ADC/DAC GAIN AMPLIFIER**
- **ACTIVE FILTERS**
- **HIGH SPEED INTEGRATORS**

DESCRIPTION

The OPA651 is a low power, wideband voltage feedback operational amplifier. It features a wide bandwidth of 500MHz as well as a 12-bit settling time of only 15ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA651 is decompensated for stability in gains of two or more. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.



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SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

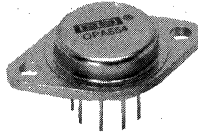
PARAMETER	CONDITIONS	OPA651P, U			OPA651PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE Closed-Loop Bandwidth ⁽²⁾ Slew Rate ⁽³⁾ At Minimum Specified Temperature Rise Time Fall Time Settling Time 0.01% 0.1% 1% Spurious Free Dynamic Range Differential Gain Differential Phase Gain Flatness	G = +2		500			* ⁽¹⁾		MHz
	G = +5		80			*		MHz
	G = +10		40			*		MHz
	G = +2, 2V Step		350			*		V/μs
			325			*		V/μs
			5.3			*		ns
			5.9			*		ns
		G = +2, 2V Step		15		*		ns
		G = +2, 2V Step		11.5		*		ns
		G = +2, 2V Step		6		*		ns
	G = +2, f = 5.0 MHz V _O = 2Vp-p, R _L = 402Ω		82		*		dBc	
	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω		0.01		*		%	
	G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01		*		%	
	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω		0.01		*		Degrees	
	G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01		*		Degrees	
	DC to 100MHz		0.1		*		dB	
INPUT OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection (+V _S) (-V _S)	V _S = ±4.5V to ±5.5V		±1 ±5	±3		±0.35 ±3	±1	mV μV/°C dB dB
			50 45	70 55		60 48		
INPUT BIAS CURRENT Input Bias Current Over Temperature Input Offset Current Over Temperature	V _{CM} = 0V		2 3	5 7		*	4 5.5	μA μA
	V _{CM} = 0V		0.4 0.9	1.5 3.0		*	*	μA μA
INPUT NOISE Input Voltage Noise Noise Density, f = 100Hz f = 10kHz f = 1MHz f = 10Hz to 100MHz Voltage Noise, BW = 10Hz to 100MHz Input Bias Current Noise Current Noise Density, f = 0.1Hz to 20kHz Noise Figure (NF)	R _S = 10kΩ R _S = 50Ω		23.2 7.5 7.1 7.2 72			*		nV/√Hz nV/√Hz nV/√Hz nVrms μVp-p
			1.1			*		pA/√Hz
			3.0			*		dBm
			19.0			*		dBm
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	V _{CM} = +2V		±2.2 52	±2.8 57		* 65	* 85	V dB
INPUT IMPEDANCE Differential Common-Mode			15 1 16 1			*		kΩ pF MΩ pF
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature	V _O = ±2V, R _L = 100Ω V _O = ±2V, R _L = 100Ω		55 53	61 59		47 45	55 53	dB dB
OUTPUT Voltage Output Over Specified Temperature Current Output Over Specified Temperature Short Circuit Current Output Resistance	No Load R _L = 250Ω R _L = 100Ω +25°C to Max Temperature		±2.5 ±2.5 ±2.0	±2.75 ±2.7 ±2.5		* * *	* * *	V V V
			±40 ±30	±50 ±48		±43 ±32	±55 ±52	mA mA
				60			*	mA
		1MHz, G = +2		0.2			*	Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current Over Specified Temperature			±4.5	±5		*	*	V V
			±5.1 ±5.4	±7.75 ±8.75		±4.9 ±5.2	±6.5 ±7.5	mA mA
TEMPERATURE RANGE Specification: P, U, PB, UB Thermal Resistance, θ _{JA} P U			-40	+85		*	*	°C
				120		*	*	°C/W
				170		*	*	°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

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OPA654

Wide Bandwidth, High Output Current *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- HIGH SLEW RATE: 750V/ μ s
- HIGH OUTPUT CURRENT: 200mA
- WIDE GAIN-BANDWIDTH: 700MHz
- FAST SETTLING: 150ns to 0.1%
- FET INPUT: $I_b = 50$ pA max

APPLICATIONS

- LINE DRIVERS
- PIN DRIVERS
- HIGH-SPEED DATA ACQUISITION
- WAVEFORM GENERATORS

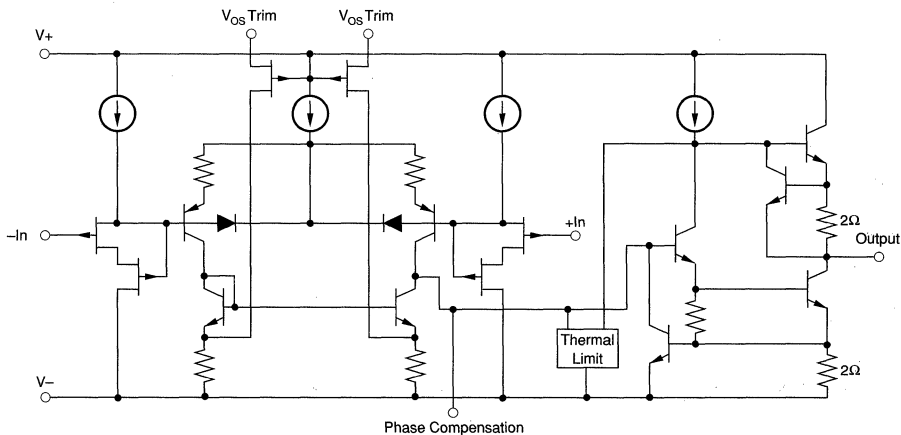
DESCRIPTION

The OPA654 is a high-speed monolithic operational amplifier featuring 200mA output current. Fabricated using Burr-Brown's Complementary-Bipolar, *Difet* process, it provides an excellent combination of high speed and high output current.

The OPA654 is versatile, operating from power supplies ranging from ± 5 V to ± 18 V. It can deliver up to ± 10 V signals into a 50 Ω load at slew rates of 750V/ μ s. Its speed and output current make it useful for line driver and automatic test applications.

The OPA654 is externally compensated, allowing open-loop gain and phase characteristics to be optimized for the desired closed-loop gain, load and dynamic characteristics.

The OPA654 is available in an 8-pin metal TO-3 package that provides excellent thermal characteristics and is specified for the industrial temperature range.



Difet® Burr-Brown Corp.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITION	OPA654AM			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE			See Typical Curve		
Gain-Bandwidth Product ⁽²⁾					V/ μs
Slew Rate ^(2,3)			750		V/ μs
Settling Time ⁽²⁾ 0.01%	G = -1, 20V Step		240		ns
0.1%	G = -1, 10V Step		150		ns
1%	G = -1, 10V Step		85		ns
OFFSET VOLTAGE					
Input Offset Voltage			± 0.1	± 3	mV
Average Drift			± 40		$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection	$V_S = \pm 5$ to $\pm 15\text{V}$	72	82		dB
INPUT BIAS CURRENT⁽¹⁾					
Input Bias Current	$V_{CM} = 0\text{V}$		3	50	μA
Input Offset Current	$V_{CM} = 0\text{V}$		2	25	μA
NOISE					
Input Voltage Noise					$\text{nV}/\sqrt{\text{Hz}}$
Noise Density,	f = 10Hz		115		$\text{nV}/\sqrt{\text{Hz}}$
	f = 100Hz		37		$\text{nV}/\sqrt{\text{Hz}}$
	f = 1kHz		19		$\text{nV}/\sqrt{\text{Hz}}$
	f = 10kHz		14		$\text{nV}/\sqrt{\text{Hz}}$
Voltage Noise,	$f_B = 10\text{Hz}$ to 1MHz		85		$\mu\text{Vp-p}$
Input Bias Current Noise					$\text{fA}/\sqrt{\text{Hz}}$
Current Noise Density, f = 0.1Hz to 20kHz			1		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE					
Common-Mode Input Range		± 12	± 13		V
Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	70	76		dB
INPUT IMPEDANCE					
Differential			$10^{12} \parallel 2.5$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{12} \parallel 3.2$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 50\Omega$		94 82		dB dB
OUTPUT					
Voltage Output	$R_L = 50\Omega$	± 11	± 12.3		V
Current Output	$V_O = \pm 10\text{V}$		200		mA
Short Circuit Current			325		mA
Output Resistance, Open-Loop	DC		800		Ω
POWER SUPPLY					
Specified Operating Voltage			± 15		V
Operating Voltage Range		± 5		± 18	V
Quiescent Current			± 38	± 43	mA
TEMPERATURE RANGE					
Specification		-25		+85	$^\circ\text{C}$
Operating		-55		+125	$^\circ\text{C}$
Storage		-55		+150	$^\circ\text{C}$
Thermal Resistance, θ_{JC}			15		$^\circ\text{C}/\text{W}$
θ_{JA}			45		$^\circ\text{C}/\text{W}$

NOTES: (1) High-speed test at $T_A = 25^\circ\text{C}$. (2) Varies with external phase compensation, C_1 . See typical curves for performance with other gains and C_1 . (3) Slew rate is rate of change from 10% to 90% of output voltage step.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

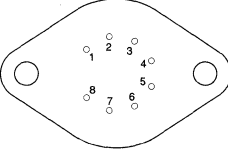
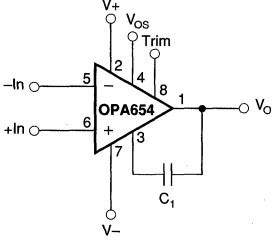
PIN CONFIGURATION

"M" TO-3 Metal Package

PIN LIST

1. V_o
2. V_+
3. Compensation
4. V_{os} Trim
5. $-In$
6. $+In$
7. V_-
8. V_{os} Trim

BOTTOM VIEW

Case is connected to IC substrate. Connect case to ground—see text.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	$\pm 18V$
Input Voltage	$\pm V_S \pm 1V$
Output Short Circuit (to ground)	10s
Operating Temperature	$-55^\circ C$ to $+125^\circ C$
Storage Temperature	$-55^\circ C$ to $+150^\circ C$
Junction Temperature	$+165^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA654AM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

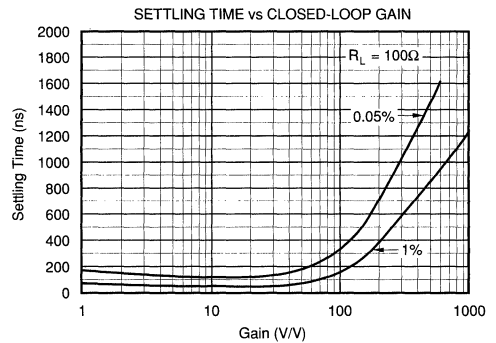
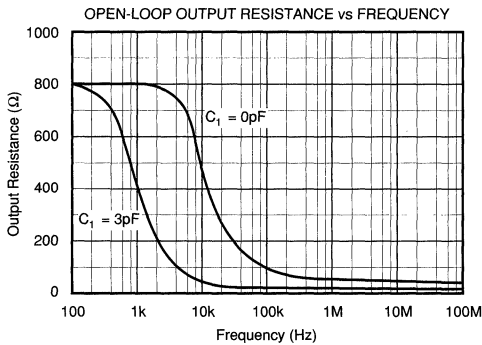
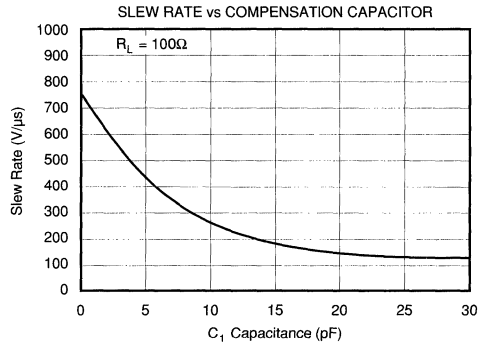
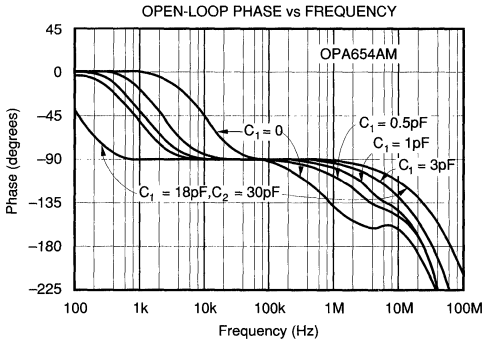
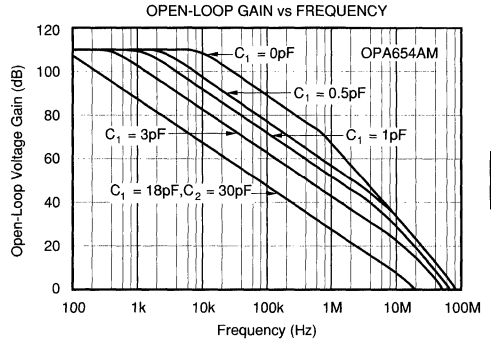
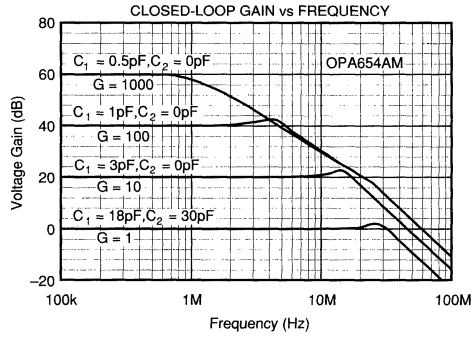
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA654AM	8-Pin Metal TO-3	$-25^\circ C$ to $+85^\circ C$

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



OPA654

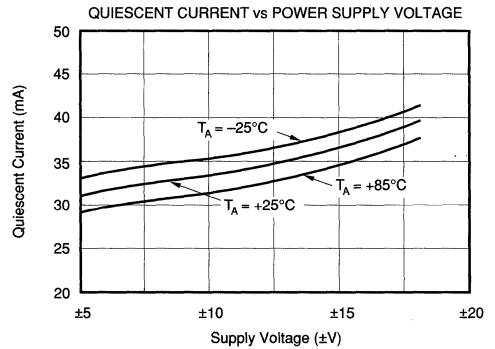
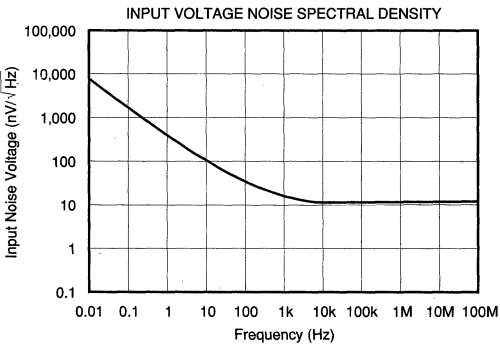
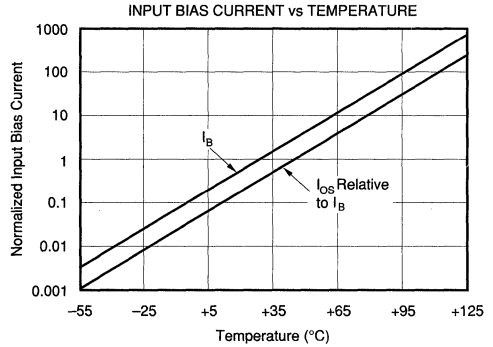
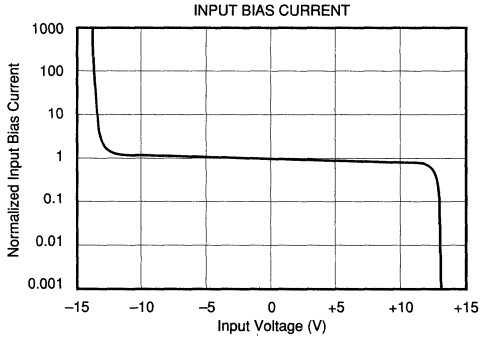
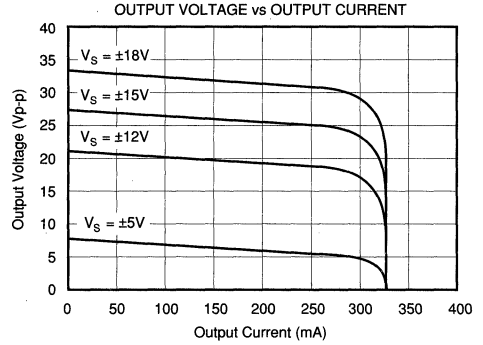
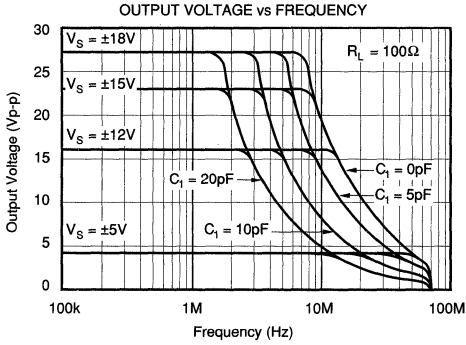
2

OPERATIONAL AMPLIFIERS

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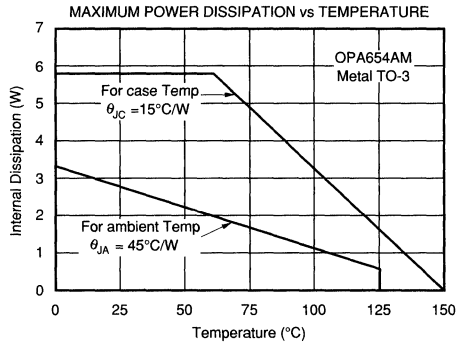
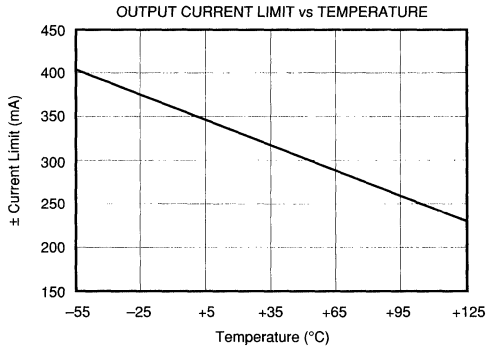
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



CIRCUIT LAYOUT

With any wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

Power supplies should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 2.2μF solid tantalum capacitor for each power supply is adequate. The OPA654 can deliver load currents up to 200mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 10μF solid tantalum capacitors may improve dynamic performance in these applications.

CASE CONNECTION

The case of the TO-3 metal package should be connected to ground. Failure to connect the case to ground will not damage the device but will degrade its AC performance. The case is internally connected to the substrate of the dielectrically isolated IC. This substrate is DC-neutral—it is not connected to the V₋ power supply as it would be with most analog ICs. In principle, it could be connected to any AC ground potential such as one of the power supplies, but DC ground is usually most convenient. Do not connect the case to DC potentials which exceed the power supply voltages, ±V_S.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1a shows connection of an optional offset voltage trimming potentiometer. Use a small, non-inductive potentiometer with short connections to the trim pins. Avoid stray capacitance from the input or output nodes. The added resistors in Figure 1b help decouple the potentiometer from

these sensitive nodes, making the type and location of the potentiometer less critical. This also reduces the trim range, providing more adjustment resolution. Do not use an offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage drift.

COMPENSATION

The OPA654 uses external compensation capacitors. This tailors the open-loop response characteristics to the application. Its effect can be seen in the open-loop gain and phase curves.

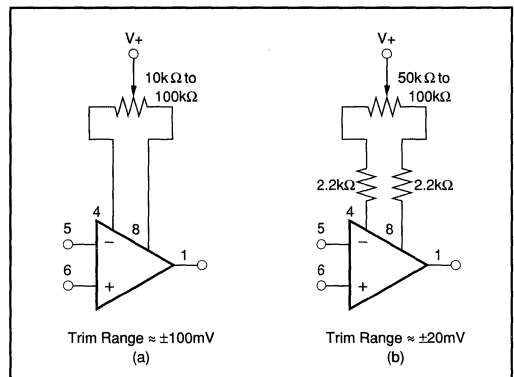
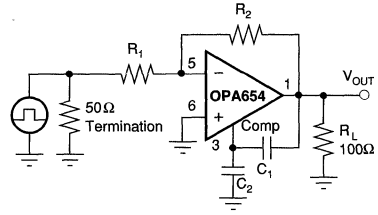
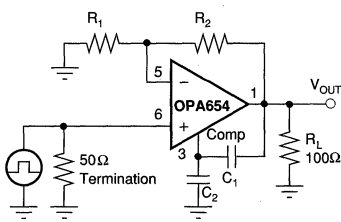


FIGURE 1. Optional Offset Voltage Trim Circuits.

Figures 2 shows typical capacitor values for various closed-loop gains. This chart should be considered a starting point for optimizing an application. Many variables including circuit layout, source and load characteristics, and desired dynamic behavior will affect the optimum capacitor values. Capacitive loads change op amp behavior and higher compensation capacitor values are generally required. Resistor R_s, shown in Figure 3, can improve the ability to drive a capacitive load. Typical values for R_s range from 5Ω to 50Ω, depending on the load and how much voltage drop can be tolerated.

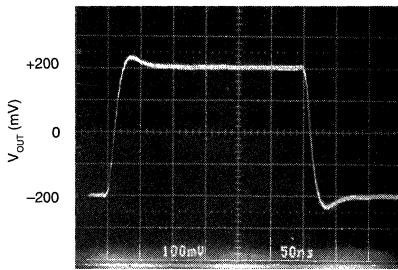
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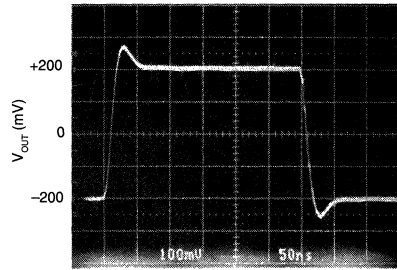
CLOSED-LOOP GAIN	C ₁	C ₂	R ₁	R ₂
+1000	0.5pF	0	10Ω	10kΩ
+100	1pF	0	100Ω	10kΩ
+10	3pF	0	100Ω	900Ω
+1	18pF	30pF	—	0

CLOSED-LOOP GAIN	C ₁	C ₂	R ₁	R ₂
-1000	0.5pF	0	10Ω	10kΩ
-100	1pF	0	100Ω	10kΩ
-10	3pF	0	100Ω	1kΩ
-1	18pF	20pF	1kΩ	1kΩ

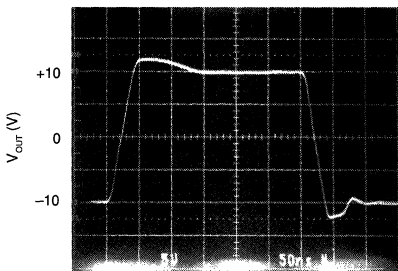
G = +10 SMALL-SIGNAL RESPONSE, R_L = 100Ω



G = -10 SMALL-SIGNAL RESPONSE, R_L = 100Ω



G = +10 LARGE-SIGNAL RESPONSE, R_L = 100Ω



G = -10 LARGE-SIGNAL RESPONSE, R_L = 100Ω

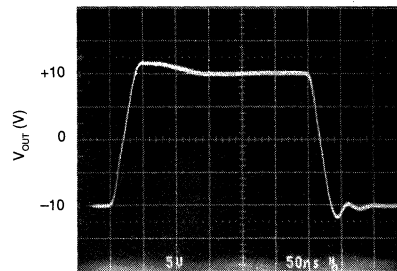


FIGURE 2. Basic Amplifier Circuits.

Figure 3 also demonstrates a compensation technique using an additional network, R_3 - C_3 . This allows use of a smaller value for C_1 , producing a corresponding increase in slew rate. It reduces the high frequency loop gain by placing the op amp in a higher noise gain at high frequency. This technique improves large-signal response at the sacrifice of small-signal behavior. Settling time is increased and high frequency noise performance will be somewhat degraded.

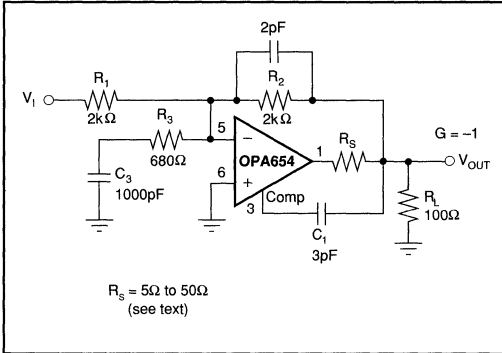


FIGURE 3. High Slew Rate Compensation Circuit.

Figure 4 shows an alternative compensation network for unity gain. This technique provides a small amount of positive feedback, reducing the net negative feedback factor. Large signal response and load driving capability is improved with this approach.

The compensation for a given application can be evaluated by observing amplifier pulse response. Both small-signal and large-signal response should be checked to assure that both are acceptable. Large overshoot or many cycles of ringing in the small-signal response is a sign of instability and the circuit may require further optimization. Good practice dictates a somewhat conservative approach to allow for device-to-device variation.

POWER DISSIPATION

Many applications do not require an external heat sink. However, with high ambient temperature or heavy load conditions, a heat sink may be required. The heat sink should be electrically connected to ground—see “Connections to Case”. Operate within the power derating curve (Maximum Power Dissipation vs Temperature) shown in the typical performance curve section.

Exceeding the maximum die temperature of 165°C may activate the internal thermal limit circuitry, disabling the output stage. This thermal limit is set for a junction temperature of approximately 185°C.

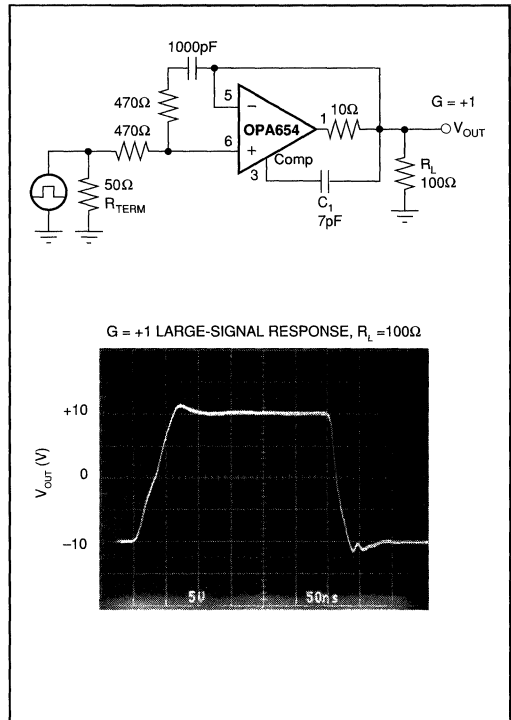


FIGURE 4. $G = +1$ Amplifier with Alternative Compensation.

The OPA654 may be operated at reduced power supply voltage, thus reducing internal power dissipation. This can eliminate the need for heat sinking in some applications.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 325mA at 25°C. The limit current decreases with increasing junction temperature as shown in the typical curves. The combination of current limit and thermal limit protects the device from short circuits to ground.

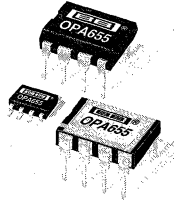
INPUT BIAS CURRENT

The OPA654 is fabricated with Burr-Brown’s dielectrically isolated *Difet* process, giving it very low input bias current. Like other FET amplifiers, input bias current doubles for every 10°C increase in junction temperature. This increase can be minimized by providing a heat sink and, if possible, operating with reduced power supply voltage to minimize power dissipation.

For Immediate Assistance, Contact Your Local Salesperson



OPA655



PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

\$9.75 ea / 1000

Wideband FET-Input OPERATIONAL AMPLIFIER

FEATURES

- **UNITY GAIN STABLE BANDWIDTH:**
400MHz
- **LOW INPUT BIAS CURRENT:**
100pA
- **SUPPLY VOLTAGE:** $\pm 5V$
- **FAST SETTLING:** 17ns (0.01%)
- **LOW DISTORTION:** 85dB SFDR at 5MHz
- **HIGH INPUT IMPEDANCE:** $10^{12}\Omega \parallel 1pF$

APPLICATIONS

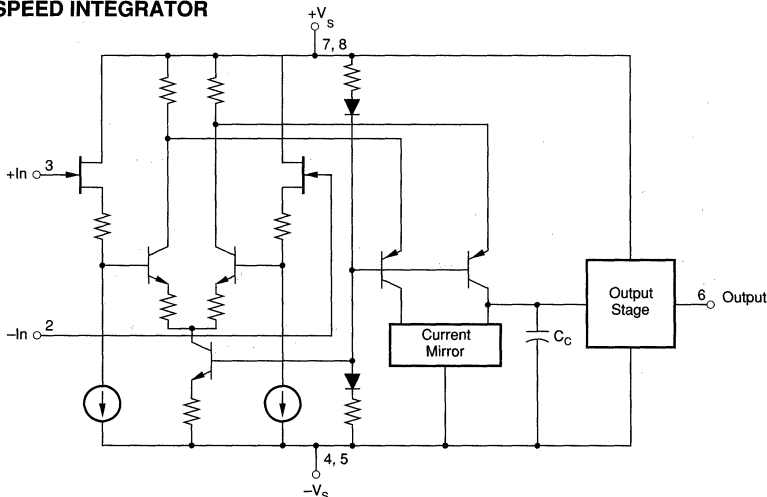
- **INSTRUMENT INPUT AMPLIFIER**
- **PHOTODIODE AMPLIFIER**
- **CURRENT-TO-VOLTAGE AMPLIFIER**
- **CCD OUTPUT BUFFER**
- **ACTIVE FILTERS**
- **HIGH SPEED INTEGRATOR**

DESCRIPTION

The OPA655 is a high-speed monolithic, fast settling operational amplifier with a unique architecture incorporating a FET input and folded cascode configuration. The FET input stage ensures a low input bias current resulting in a low DC errors and very low noise, while the folded cascode arrangement helps achieve the 400MHz bandwidth.

The low current noise of $9.8fA/\sqrt{Hz}$ provides wide dynamic range, even with high source impedance. The low input bias current and wide bandwidth make it a good choice for high speed integrators and active filter designs. Its notably low distortion combined with high bandwidth and low noise make it a superior choice for applications requiring excellent dynamic performance.

The OPA655 is available in two grades and three packages; SOIC, DIP and SIDEBRAZE.



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Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 5pF unless otherwise noted.

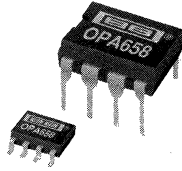
PARAMETER	CONDITIONS	OPA655P, U, HSQ			OPA655PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Response	Gain = +1V/V		400			*		MHz
	Gain = +2V/V		150			*		MHz
	Gain = +5V/V		75			*		MHz
	Gain = +10V/V		37			*		MHz
Gain-Bandwidth Product			400			*		MHz
Slew Rate ⁽²⁾	G = +1, 1V Step	250	300			*		V/μs
Settling Time: 0.003%	G = +1, 1V Step		20			*		ns
0.01%	G = +1, 1V Step		16			*		ns
0.1%	G = +1, 1V Step		12			*		ns
1%	G = +1, 1V Step		6			*		ns
Spurious-Free Dynamic Range	G = +1, f = 5MHz V _O = ±1V, R _L = 100Ω	70	80			*		dBc
Differential Gain	3.58MHz, 0 to 1.4V, R _L = 150Ω		0.02			*		%
Differential Phase	3.58MHz, 0 to 1.4V, R _L = 150Ω		0.03			*		degrees
OFFSET VOLTAGE								
Input Offset Voltage			±1	±2				mV
Average Drift			10	20			±0.5	μV/°C
Power Supply Rejection	V _S = ±4.5 to ±5.5V	65	75		(1)	*	±1	dB
INPUT BIAS CURRENT								
Input Bias Current	V _{CM} = 0V		90	300		*	200	pA
Drift	V _{CM} = 0V		9			*		pA/°C
Input Offset Current	V _{CM} = 0V		30	75		*	*	pA
Drift	V _{CM} = 0V		3			*		pA/°C
NOISE								
Input Voltage Noise								
Noise Density: f = 10Hz			30			*		nV/√Hz
f = 100Hz			13			*		nV/√Hz
f = 1kHz			5.0			*		nV/√Hz
f = 10kHz			5.0			*		nV/√Hz
f = 100kHz			5.0			*		nV/√Hz
f = 1MHz to 100MHz			5.0			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			62.6			*		μVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			9.8			*		fA/√Hz
INPUT VOLTAGE RANGE								
Common-mode Input Range			±2.5	±3.0		*	*	V
Over Temperature						*	*	
Common-mode Rejection	V _{CM} = ±1V	60	70			*	*	dB
INPUT IMPEDANCE								
Differential			10 ¹² 1			*		Ω pF
Common-Mode			10 ¹² 1			*		Ω pF
OPEN-LOOP GAIN								
Open-loop Voltage Gain	V _O = ±2V, R _L = 100Ω	55	60			*	*	dB
Over Temperature	V _O = ±2V, R _L = 100Ω	50	53			*	*	dB
OUTPUT								
Voltage Output	R _L = 100Ω	±2.5	±3.0			*	*	V
Over Specified Temperature	R _L = 100Ω	±2.5	±3.0			*	*	V
Current Output		25	50			*	*	mA
Over Specified Temperature			35			*	*	mA
Short Circuit Current			75			*	*	mA
Output Resistance, Open-Loop	DC		15			*	*	Ω
POWER SUPPLY								
Specified Operating Voltage	T _{MIN} to T _{MAX}		±5			*	*	V
Operating Voltage Range	T _{MIN} to T _{MAX}	±4.5		±5.5		*	*	V
Quiescent Current	T _{MIN} to T _{MAX}		±25	±30		*	*	mA
TEMPERATURE RANGE								
Specification: P, PB, U, UB			-40	+85		*	*	°C
HSQ			-55	+150		*	*	°C
Thermal Resistance, θ _{JA}								°C/W
P								°C/W
U								°C/W
H								°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left.

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OPA658

PRELIMINARY INFORMATION
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Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY GAIN STABLE BANDWIDTH:
900MHz
- LOW POWER: 47mW
- LOW DIFF GAIN/PHASE ERRORS:
0.01%/0.01°
- HIGH SLEW RATE: 2000V/ μ s
- GAIN FLATNESS: 0.1dB to 200MHz
- PACKAGE: 8-Pin DIP and 8-Pin SOIC

APPLICATIONS

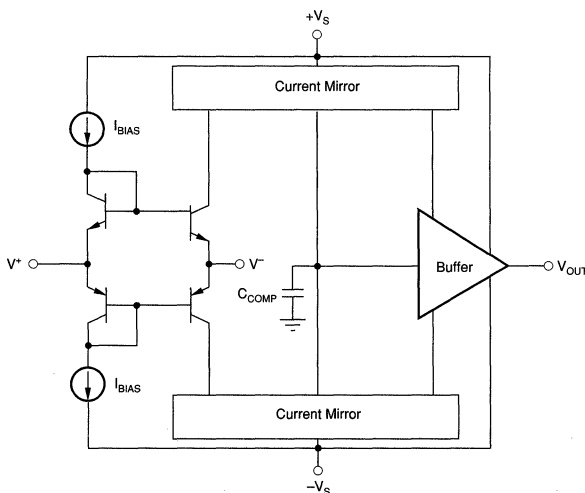
- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA658 is an ultra-wideband, low power current feedback video operational amplifier featuring a high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent

current make the OPA658 a perfect choice for numerous video, imaging and communications applications.

The OPA658 is internally compensated for unity-gain stability. The OPA658 is also available in dual, OPA2658 and quad, OPA4658 configurations.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{fb} = 402Ω unless otherwise noted.

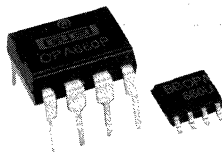
PARAMETER	CONDITION	OPA658P, U			OPA658PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE Closed-Loop Bandwidth ⁽²⁾ Slew Rate ⁽³⁾ At Minimum Specified Temperature Settling Time: 0.01% 0.1% 1% Spurious Free Dynamic Range Third Order Intercept Point Differential Gain Differential Phase Gain Flatness Bandwidth for 0.1dB of Flatness	G = +1		900					MHz
	G = +2	400	700		*	*(1)		MHz
	G = +5		320			*		MHz
	G = +10	195	2000			*		V/μs
	G = +1, 2V Step	900	1500		*	*		V/μs
	G = +1, 2V Step		15		*	*		ns
	G = +1, 2V Step		11.5		*	*		ns
	G = -1, 2V Step		6		*	*		ns
	f = 5MHz, G = +1, V _O = 2Vp-p		63		*	*		dBc
	f = 20MHz, G = +1, V _O = 2Vp-p		52		*	*		dBc
	f = 10MHz	TBD			TBD		dBm	
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 150Ω	0.01	0.025		*	*	%	
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 400Ω	0.01	0.025		*	*	%	
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 150Ω	0.015	0.03		*	*	degrees	
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 400Ω	0.01	0.03		*	*	degrees	
	G = +2, DC to 200 MHz	0.1			*	*	dB	
	G = +2	TBD			TBD		MHz	
OFFSET VOLTAGE Input Offset Voltage Over Specified Temperature Power Supply Rejection (+V _S) (-V _S)	V _{CM} = 0V V _S = ±4.7 to ±5.5V		±3 ±20	±5.5		*	*	mV μV/°C dB dB
		55	58		*	*		
		45	52		*	*		
INPUT BIAS CURRENT Non-Inverting Over Temperature Inverting Over Temperature	V _{CM} = 0V V _{CM} = 0V		5 40 2 30	12 80 20 90		*	*	μA μA μA μA
NOISE Input Voltage Noise Density f = 100Hz f = 1kHz f = 10kHz f = 1MHzQ f _B = 100Hz to 200MHz Inverting Input Bias Current Noise Density: f = 10MHz Non-Inverting Input Current Noise Density: f = 10MHz Noise Figure (NF)	G = TBD R _S = 10kΩ R _S = 50Ω		10.3 2.9 1.9 1.9 33.6			*	*	nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVrms pA/√Hz pA/√Hz dBm dBm
			15			*	*	
			15			*	*	
			3.0			*	*	
			19.0			*	*	
INPUT VOLTAGE RANGE Common-mode Input Range Over Specified Temperature Common-mode Rejection	V _{CM} = ±1V	±2.7 45	±3.0 50		*	*	*	V dB
INPUT IMPEDANCE Non-Inverting Inverting			500 1 20			*	*	kΩ pF Ω
OPEN-LOOP TRANSRESISTANCE Open-loop Transresistance Over Specified Temperature	V _O = ±2V, R _L = 100Ω V _O = ±2V, R _L = 100Ω	150 100	190		200 175	250		kΩ kΩ
OUTPUT Voltage Output Over Specified Temperature Voltage Output Over Specified Temperature Voltage Output Over Specified Temperature Current Output Over Specified Temperature Short Circuit Current Output Resistance	No Load R _L = 250Ω R _L = 100Ω +25°C to max Temperature 1MHz, G = +1	±2.7 ±2.5 ±2.7 ±2.5 ±2.2 ±2.0 ±5.0 ±30	±2.9 ±2.75 ±2.9 ±2.7 ±2.8 ±2.5 ±60 ±48 60 0.025		*	*	*	V V V V V V mA mA mA Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current Over Specified Temperature	V _S = ±5V	±4.5	±5	±5.5 ±7.75 ±8.5	*	*	*	V V mA mA
TEMPERATURE RANGE Specification: P, U, PB, UB Thermal Resistance, θ _{JA} P U		-40		+85	*	*	*	°C °C/W °C/W
			120 170			*	*	

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Closed-loop bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for detailing. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

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For Immediate Assistance, Contact Your Local Salesperson



OPA660

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

FEATURES

- WIDE BANDWIDTH: 700MHz
- HIGH SLEW RATE: 3000V/μs
- LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.06%/0.02°
- VERSATILE CIRCUIT FUNCTION
- EXTERNAL I_Q-CONTROL
- HIGH IMPEDANCE CURRENT SOURCE

DESCRIPTION

The OPA660 is a versatile monolithic component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes a wideband, bipolar integrated voltage-controlled current source and voltage buffer amplifier in an 8-pin package.

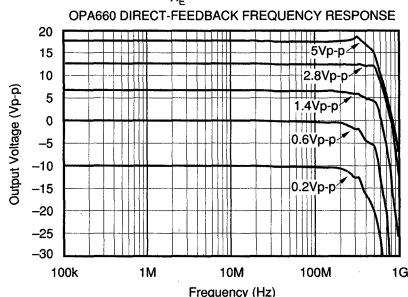
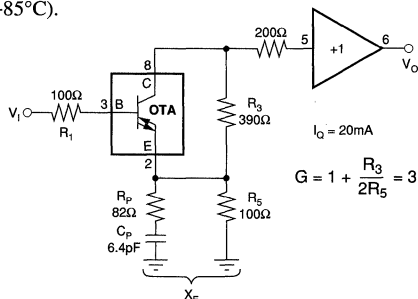
The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero for zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain trade-offs to be optimized.

The open loop buffer amplifier provides 700MHz bandwidth and 3000V/μs slew rate. Used as a basic building block, the OPA660 simplifies the design of AGC amplifiers, LED driver circuits for Fiber Optic Transmission, integrators for short ns pulses, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters.

APPLICATIONS

- VIDEO/BROADCAST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- WIDEBAND LED DRIVER
- DIRECT-FEEDBACK AMPLIFIER
- AGC-MULTIPLIER
- NS-PULSE INTEGRATOR
- CONTROL LOOP AMPLIFIER
- 400MHz DIFFERENTIAL INPUT AMPLIFIER

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP packages and is specified for the extended industrial temperature range (-40°C to +85°C).



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SPECIFICATIONS

ELECTRICAL

Typical at $I_o = 20\text{mA}$, $V_s = \pm 5\text{VDC}$, $T_A = +25^\circ\text{C}$, $R_L = 500\Omega$ unless otherwise specified.

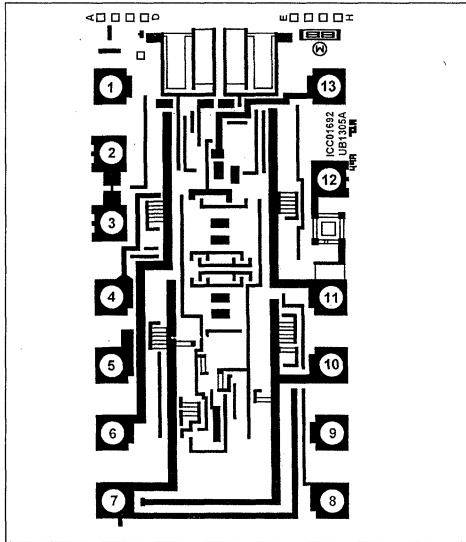
PARAMETER	CONDITIONS	OPA660AP, AU			UNITS
		MIN	TYP	MAX	
OTA TRANSCONDUCTANCE Transconductance	$V_o = 0\text{V}$	75	125	200	mA/V
OTA INPUT OFFSET VOLTAGE Initial			+7	±30	mV
vs Temperature			50		$\mu\text{V}/^\circ\text{C}$
vs Supply (tracking)	$V_s = \pm 4.5\text{V to } \pm 5.5\text{V}$	55	60		dB
vs Supply (non-tracking)	$V_+ = 4.5\text{V to } 5.5\text{V}$	40	45		dB
vs Supply (non-tracking)	$V_- = -4.5\text{V to } -5.5\text{V}$	40	48		dB
OTA B-INPUT BIAS CURRENT Initial			-2.1	±5	μA
vs Temperature			5		$\text{nA}/^\circ\text{C}$
vs Supply (tracking)	$V_s = \pm 4.5\text{V to } \pm 5.5\text{V}$			±750	nA/V
vs Supply (non-tracking)	$V_+ = 4.5\text{V to } 5.5\text{V}$			±1500	nA/V
vs Supply (non-tracking)	$V_- = -4.5\text{V to } -5.5\text{V}$			±500	nA/V
OTA OUTPUT BIAS CURRENT Output Bias Current	$V_o = 0\text{V}$		±10	±20	μA
vs Temperature			500		$\text{nA}/^\circ\text{C}$
vs Supply (tracking)	$V_s = \pm 4.5\text{V to } \pm 5.5\text{V}$		±10	±25	$\mu\text{A}/\text{V}$
vs Supply (non-tracking)	$V_+ = 4.5\text{V to } 5.5\text{V}$		±10	±25	$\mu\text{A}/\text{V}$
vs Supply (non-tracking)	$V_- = -4.5\text{V to } -5.5\text{V}$		±10	±25	$\mu\text{A}/\text{V}$
OTA OUTPUT Output Current		±10	±15		mA
Output Voltage Compliance	$I_o = \pm 1\text{mA}$	±4.0	±4.7		V
Output Impedance			25k 4.2		Ω pF
Open Loop Gain	$f = 1\text{kHz}$		70		dB
BUFFER OFFSET VOLTAGE Initial			+7	±30	mV
vs Temperature			50		$\mu\text{V}/^\circ\text{C}$
vs Supply (tracking)	$V_s = \pm 4.5\text{V to } \pm 5.5\text{V}$	55	60		dB
vs Supply (non-tracking)	$V_+ = 4.5\text{V to } 5.5\text{V}$	40	45		dB
vs Supply (non-tracking)	$V_- = -4.5\text{V to } -5.5\text{V}$	40	48		dB
BUFFER INPUT BIAS CURRENT Initial			-2.1	±5	μA
vs Temperature			5		$\text{nA}/^\circ\text{C}$
vs Supply (tracking)	$V_s = \pm 4.5\text{V to } \pm 5.5\text{V}$			±750	nA/V
vs Supply (non-tracking)	$V_+ = 4.5\text{V to } 5.5\text{V}$			±1500	nA/V
vs Supply (non-tracking)	$V_- = -4.5\text{V to } -5.5\text{V}$			±500	nA/V
BUFFER and OTA INPUT IMPEDANCE Input Impedance			1.0 2.1		M Ω pF
BUFFER INPUT NOISE Voltage Noise Density, $f = 100\text{kHz}$			4		$\text{nV}/\sqrt{\text{Hz}}$
BUFFER DYNAMIC RESPONSE Small Signal Bandwidth	$V_o = \pm 100\text{mV}$	700	850		MHz
Full Power Bandwidth	$V_o = \pm 1.4\text{V}$		800		MHz
	$V_o = \pm 2.5\text{V}$		570		MHz
Differential Gain Error	3.58MHz, at 0.7V		0.06		%
Differential Phase Error	3.58MHz, at 0.7V		0.02		Degrees
Harmonic Distortion, 2nd Harmonic	$f = 10\text{MHz}$, $V_o = 0.5\text{Vp-p}$		-68		dBc
Slew Rate	5V Step		3000		V/ μs
Settling Time 0.1%	2V Step		25		ns
Rise Time (10% to 90%)	$V_o = 100\text{mVp-p}$		1		ns
	5V Step		1.5		ns
Group Delay Time			250		ps
BUFFER RATED OUTPUT Voltage Output	$I_o = \pm 1\text{mA}$	±3.7	±4.2		V
Current Output		±10	±15		mA
Gain		0.96	0.975		V/V
	$R_L = 5k\Omega$		0.99		V/V
Output Impedance			7 2		Ω pF
POWER SUPPLY Voltage, Rated			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current (Programmable, Useful Range)		±3	±20	±26	mA

OPA660

2

OPERATIONAL AMPLIFIERS

DICE INFORMATION



OPA660 DIE TOPOGRAPHY

PAD	FUNCTION
1	Enable
2	NC
3	NC
4	OTA Input, Low Impedance
5	OTA Input, High Impedance
6	-5V Supply, Output
7	-5V Supply
8	Buffer Input
9	Buffer Output
10	+5V Supply
11	+5V Supply, Output
12	NC
13	OTA Output
14	NC

Substrate Bias: Negative Supply

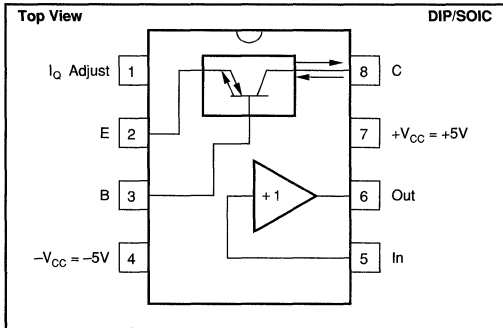
NC: No Connection

Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	41 x 77, ±5	1.05 x 1.95, ±0.13
Die Thickness	14 ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, ±0.05, -0.0	0.0005, ±0.0013, -0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage (1)	±V _S ±0.7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to ±V_S.

PACKAGING INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA660AP	8-Pin Plastic DIP	006
OPA660AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

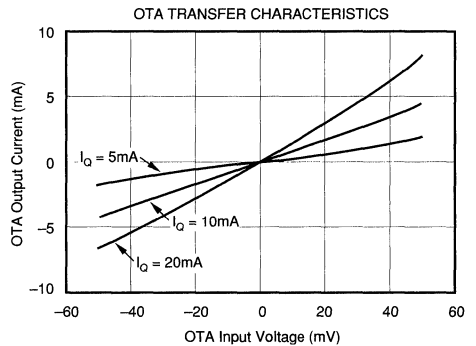
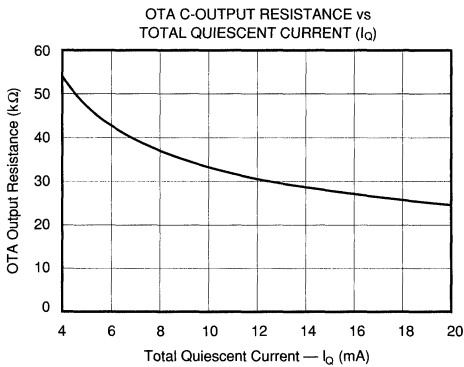
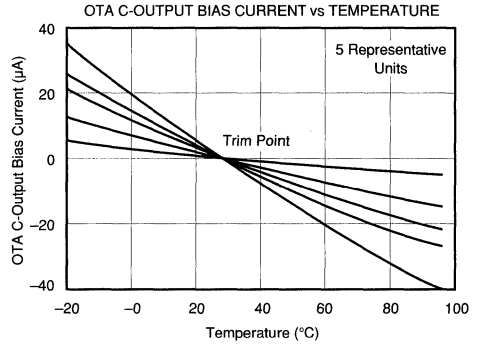
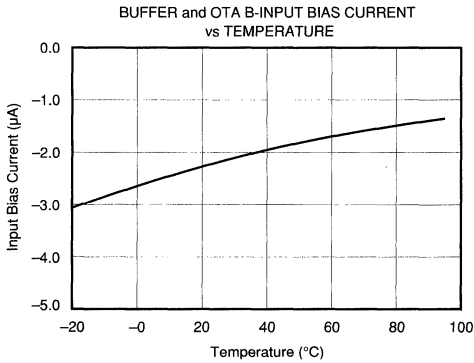
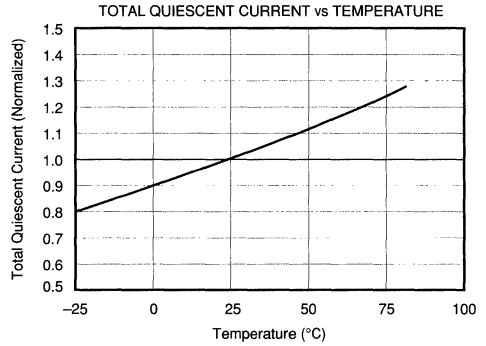
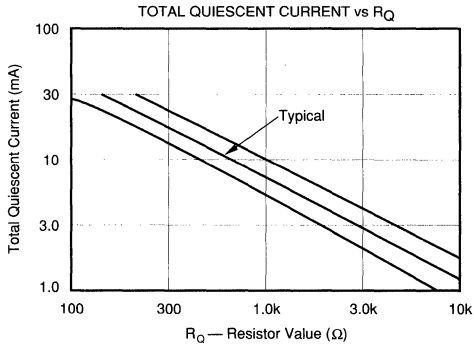
MODEL	PACKAGE	TEMPERATURE RANGE
OPA660AP	Plastic 8-Pin DIP	-25°C to +85°C
OPA660AU	SO-8 Surface-Mount	-25°C to +85°C

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TYPICAL PERFORMANCE CURVES

$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



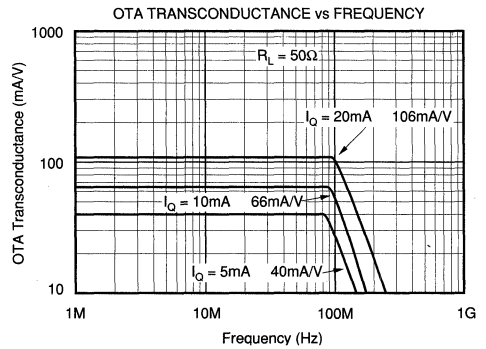
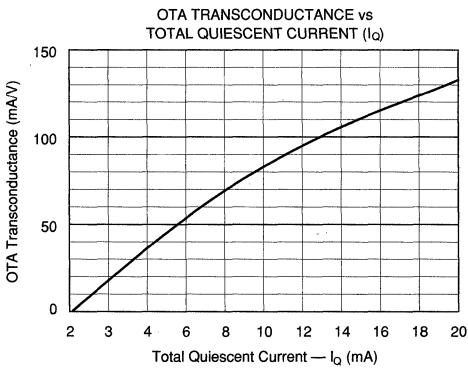
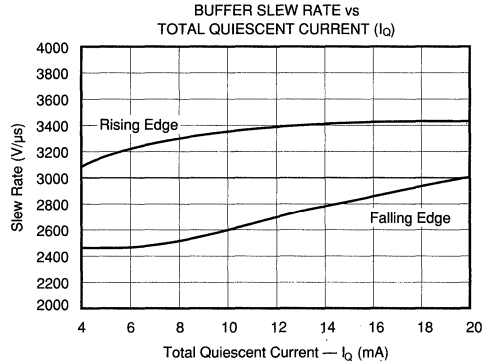
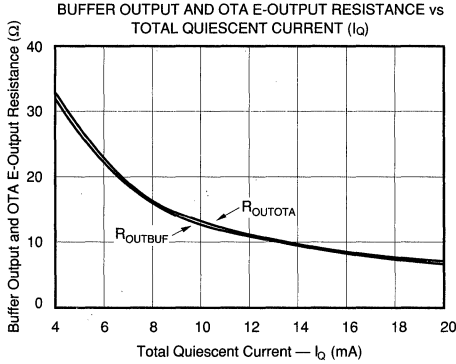
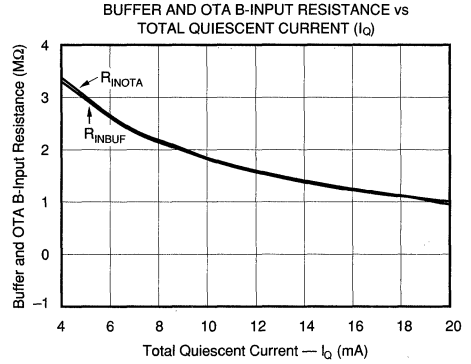
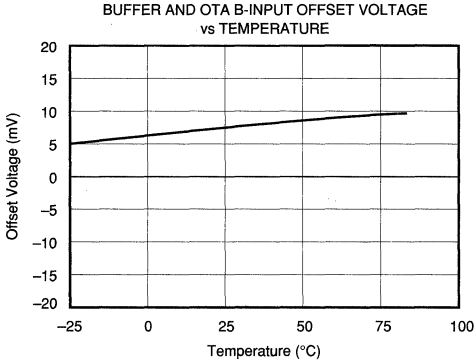
OPA660

OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

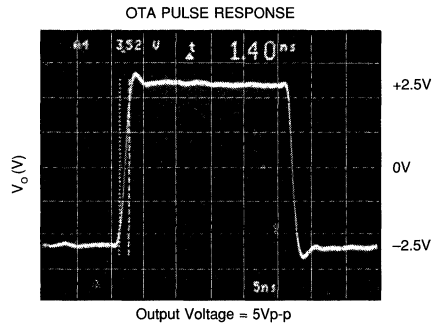
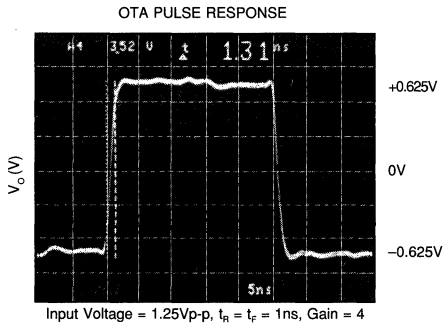
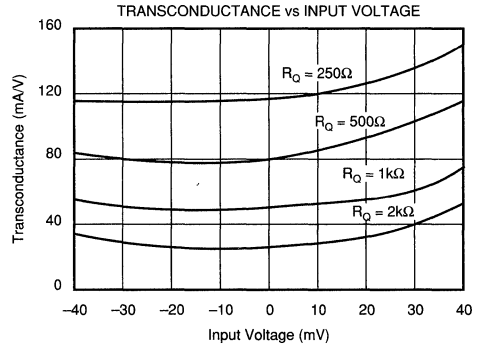
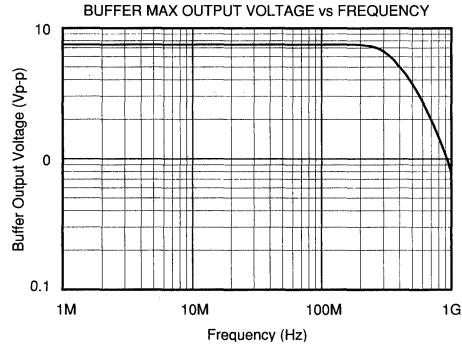
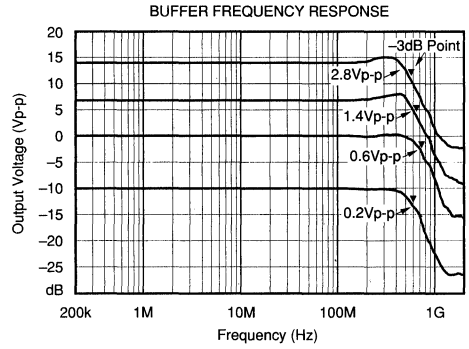
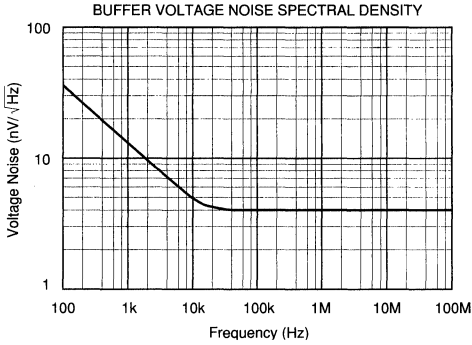
$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



OPA660

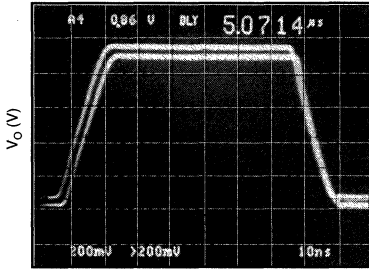
OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

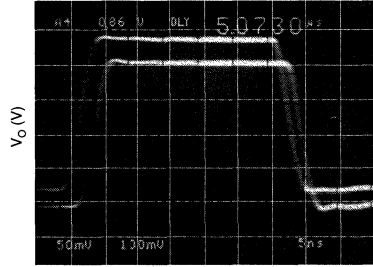
$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.

BUFFER LARGE SIGNAL PULSE RESPONSE

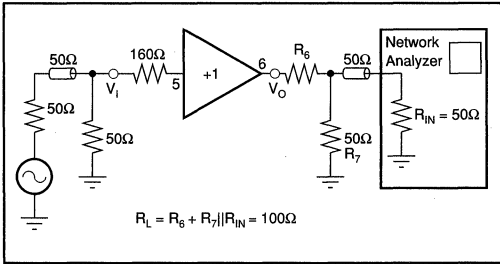


(HDTV Signal Pulse) $t_r = t_f = 10\text{ns}$, $V_O = 5\text{Vp-p}$

BUFFER LARGE SIGNAL PULSE RESPONSE

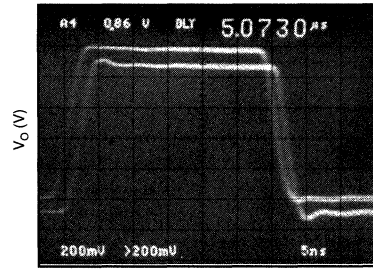


$t_r = t_f = 3\text{ns}$, $V_O = 5\text{Vp-p}$



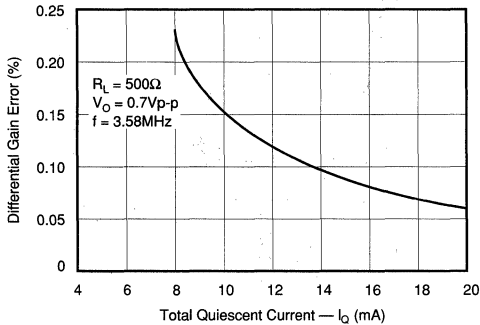
Test Circuit Buffer Pulse and Frequency Response

BUFFER SMALL SIGNAL PULSE RESPONSE

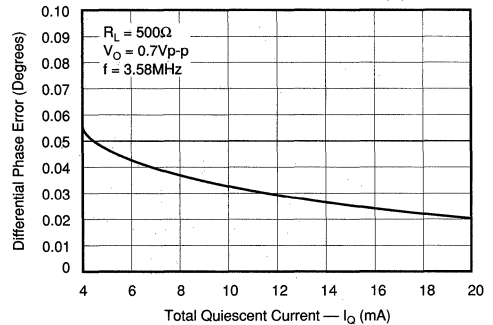


$t_r = t_f = 3\text{ns}$, $V_O = 0.2\text{Vp-p}$

BUFFER DIFFERENTIAL GAIN ERROR
vs TOTAL QUIESCENT CURRENT (I_Q)



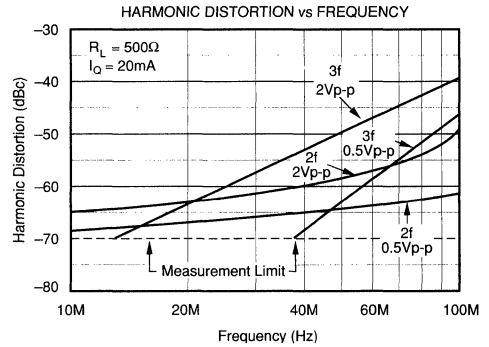
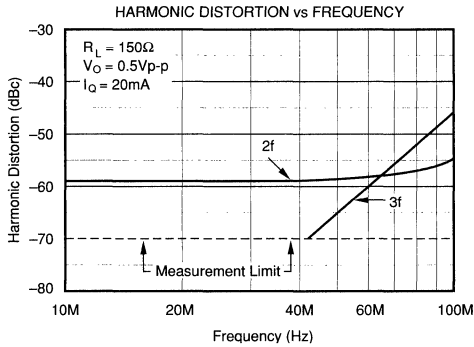
BUFFER DIFFERENTIAL PHASE ERROR
vs TOTAL QUIESCENT CURRENT (I_Q)



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TYPICAL PERFORMANCE CURVES (CONT)

$I_O = 20\text{mA}$, $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

The OPA660 operates from $\pm 5\text{V}$ power supplies ($\pm 6\text{V}$ maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the OPA660 are protected with internal diode clamps as shown in the simplified schematic, Figure 1. These protection diodes can safely conduct 10mA , continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V , the input signal current must be limited.

The buffer output is not current-limited or protected. If the output is shorted to ground, currents up to 60mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage. The same cautions apply to the OTA section when connected as a buffer (see Basic Applications Circuits, Figure 6b).

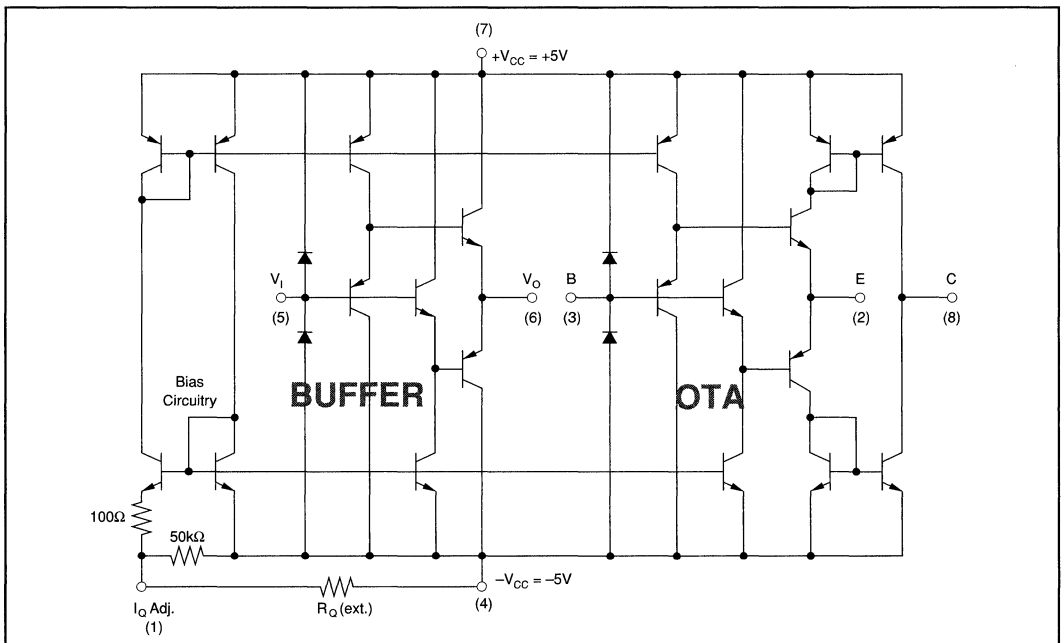


FIGURE 1. Simplified Circuit Diagram.

BUFFER SECTION—AN OVERVIEW

The buffer section of the OPA660 is an open-loop buffer consisting of complementary emitter-followers. It uses no feedback, so its low frequency gain is slightly less than unity and somewhat dependent on loading. It is designed primarily for interstage buffering. It is not designed for driving long cables or low impedance loads (although with small signals, it may be satisfactory for these applications).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor. Applications circuits for the OTA look and operate much like transistor circuits—the transistor, too, is a voltage-controlled current source. Not only does this simplify the understanding of applications circuits, but it aids the circuit optimization process. Many of the same intuitive techniques used with transistor designs apply to OTA circuits as well. The three terminals of the OTA are labeled B, E, and C. This calls attention to its similarity to a transistor, yet draws distinction for clarity.

While it is similar to a transistor, one essential difference is the sense of the C output current. It flows out the C terminal for positive B-to-E input voltage and in the C terminal for negative B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. The OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents—this implies a fundamental improvement of linearity.

BASIC CONNECTIONS

Figure 2 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See "Circuit Layout" at the end of the applications discussion and Figure 26 for further suggestions on layout.

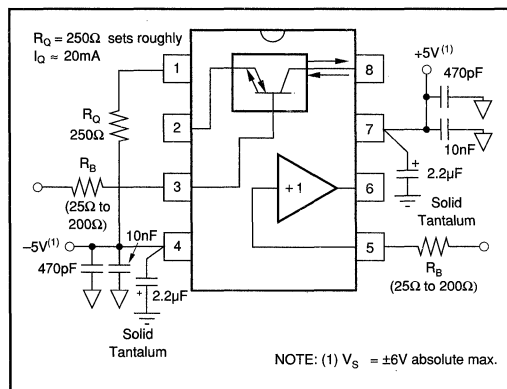


FIGURE 2. Basic Connections.

QUIESCENT CURRENT CONTROL PIN

The quiescent current of the OPA660 is set with a resistor, R_Q , connected from pin 1 to V_- . It affects the operating currents of both the buffer and OTA sections. This controls the bandwidth and AC behavior as well as the transconductance of the OTA section.

$R_Q = 250\Omega$ sets approximately 20mA total quiescent current at 25°C. With a fixed 250Ω resistor, process variations could cause this current to vary from approximately 16mA to 26mA. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show resistor, R_Q , but it is required for proper operation.

With a fixed R_Q resistor, quiescent current increases with temperature (see typical performance curve, Quiescent Current vs Temperature). This variation of current with temperature holds the transconductance, g_m , of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 3 shows a 1/2 of a REF200 current source used to develop 100mV on R_1 . The loop forces 100mV to appear on R_2 . Total quiescent current of the OPA660 is approximately $85 \cdot I_1$, where I_1 is the current made to flow out of pin 1.

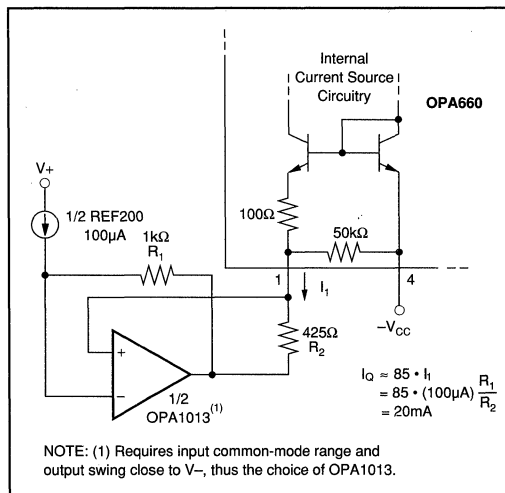


FIGURE 3. Optional Control Loop for Setting Quiescent Current.

With this control loop, quiescent current will be nearly constant with temperature. Since this differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in typical performance curves.

The circuit of Figure 3 will control the I_Q of the OPA660 somewhat more accurately than with a fixed external resis-

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tor, R_Q . Otherwise, there is no fundamental advantage to using this more complex biasing circuitry. It does, however, demonstrate the possibility of signal-controlled quiescent current. This may suggest other possibilities such as AGC, dynamic control of AC behavior, or VCO.

Figure 4 shows logic control of pin 1 used to disable the OPA660. Zero/5V logic levels are converted to a 1mA/0mA current connected to pin 1. The 1mA current flowing in R_Q increases the voltage at pin 1 to approximately 1V above the -5V rail. This will reduce I_Q to near zero, disabling the OPA660.

BASIC APPLICATIONS CIRCUITS

Most applications circuits for the OTA section consist of a few basic types which are best understood by analogy to a transistor. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C. See Figures 5, 6 and 7.

A positive voltage at the B, pin 3, causes a positive current

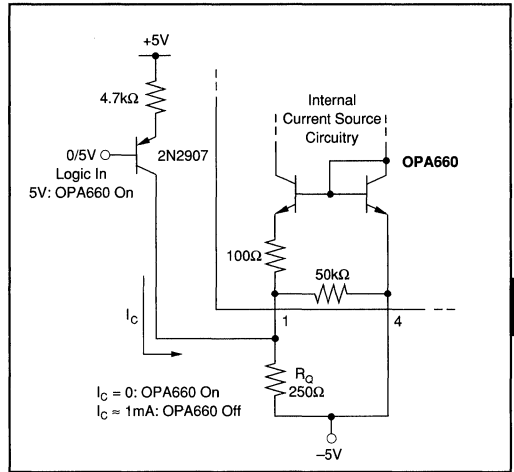


FIGURE 4. Logic-Controlled Disable Circuit.

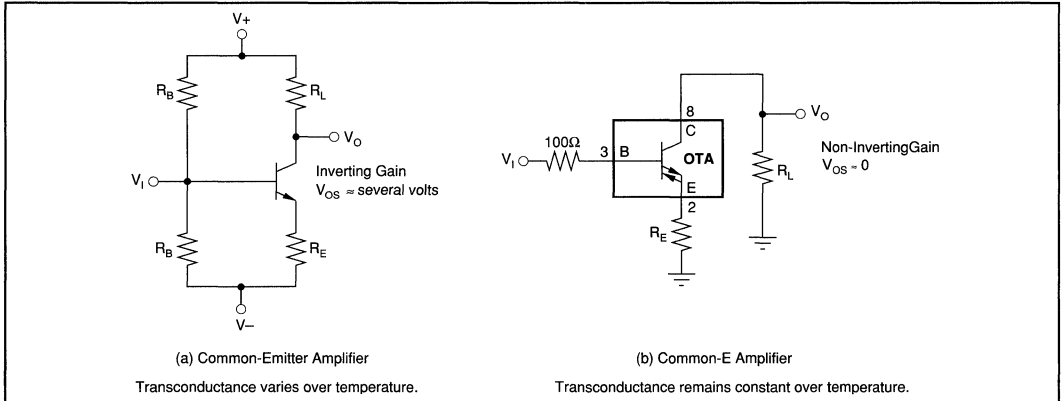


FIGURE 5. Common-Emitter vs Common-E Amplifier.

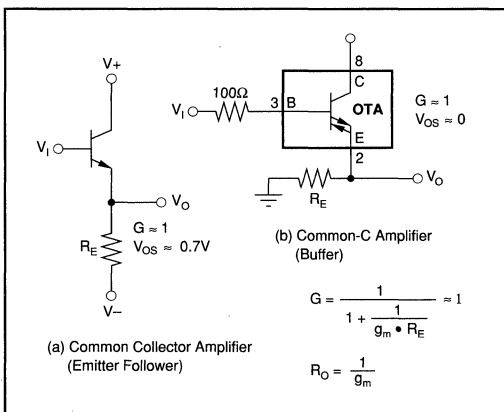


FIGURE 6. Common Collector vs Common-C Amplifier.

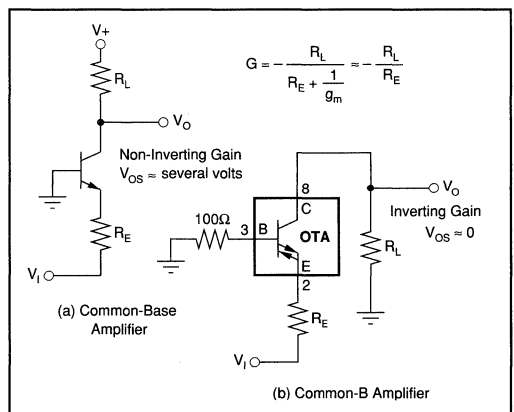


FIGURE 7. Common-Base vs Common-B Amplifier.

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to flow out of the C, pin 8. Figure 5b shows an amplifier connection of the OTA, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting. Figure 8 shows the amplifier with various gains and output voltages using this configuration.

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This can be used to reduce the effect that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high-frequency performance.

The transconductance of the OTA with degeneration can be calculated by—

$$g_m' = \frac{1}{\frac{1}{g_m} + R_E}$$

Figure 6b shows the OTA connected as an E-follower—a voltage buffer. The buffer formed by this connection performs virtually the same as the buffer section of the OPA660 (the actual signal path is identical).

It is recommended to use a low value resistor in series with the B OTA and buffer inputs. This reduces any tendency to oscillate and controls frequency response peaking. Values from 25Ω to 200Ω are typical.

Figure 7 shows the Common-B amplifier. This configuration produces an inverting gain, and a low impedance input. This low impedance can be converted to a high impedance by inserting the buffer amplifier in series.

CIRCUIT LAYOUT

The high frequency performance of the OPA660 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not dogma.

- Bypass power supplies very close to the device pins. Use a combination between tantalum capacitors (approximately 2.2μF) and polyester capacitors. Surface-mount types are best because they provide lowest inductance.
- Make short, wide interconnection traces to minimize series inductance.
- Use a large ground plane to assure that a low impedance ground is available throughout the layout.
- Do not extend the ground plane under high impedance nodes sensitive to stray capacitance.
- Sockets are not recommended because they add significant inductance.

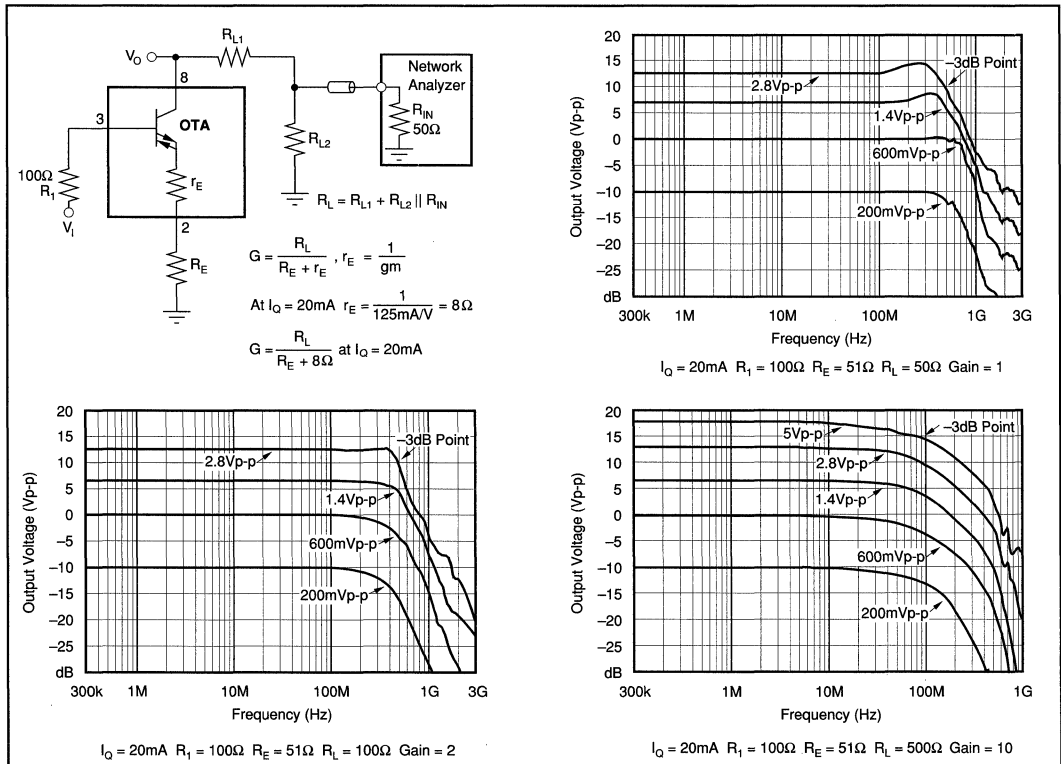


FIGURE 8. Common-E Amplifier Performance.

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- Use low-inductance components. Some film resistors are trimmed with spiral cuts which increase inductance.
- Use surface-mount components—they generally provide the lowest inductance.

- A resistor (25Ω to 200Ω) in series with the buffer and/or B input may help reduce oscillations and peaking.
- Use series resistors in the supply lines to decouple multiple devices.

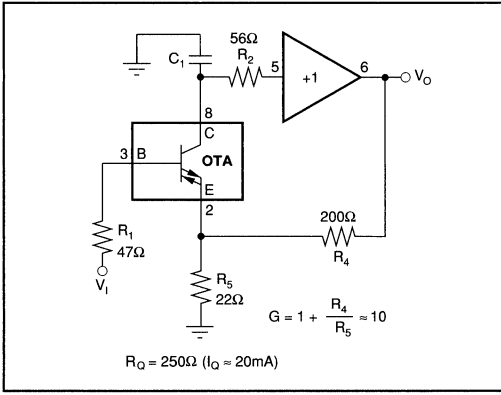


FIGURE 9. Current-Feedback Amplifier.

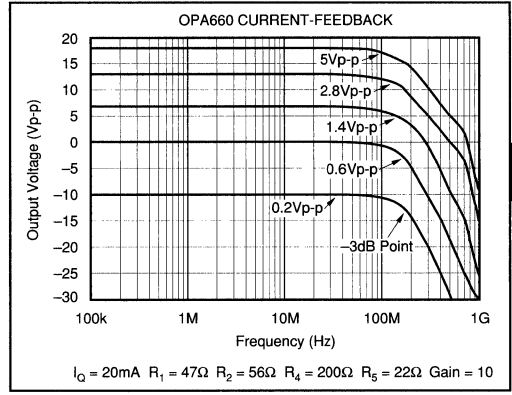


FIGURE 10. Current-Feedback Amplifier Frequency Response, G = 10.

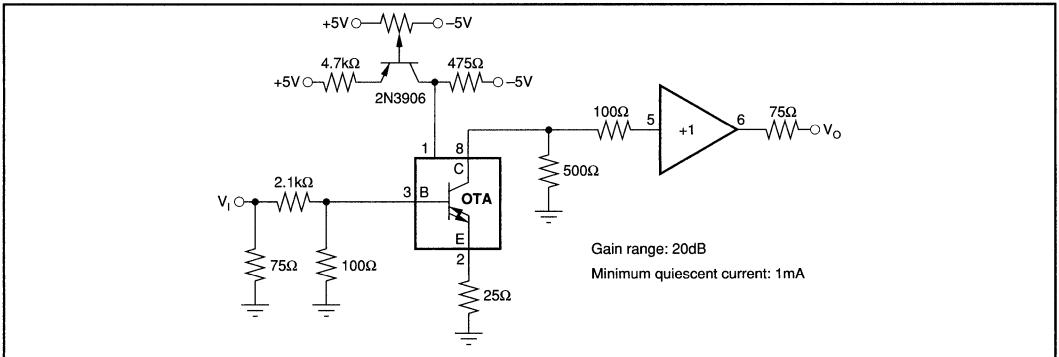


FIGURE 11. Variable Gain Amplifier (Luminance).

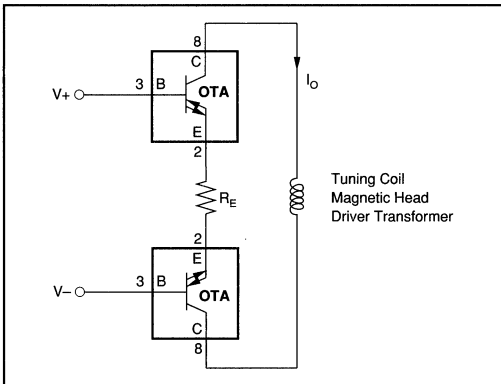


FIGURE 12. High-Speed Current Driver (bridge combination for increased output voltage capability).

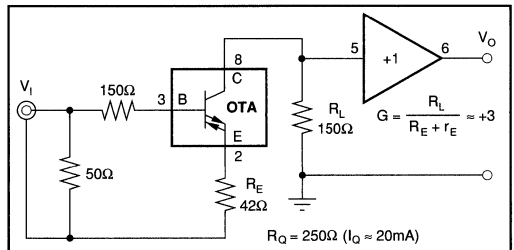


FIGURE 13. Cable Amplifier.

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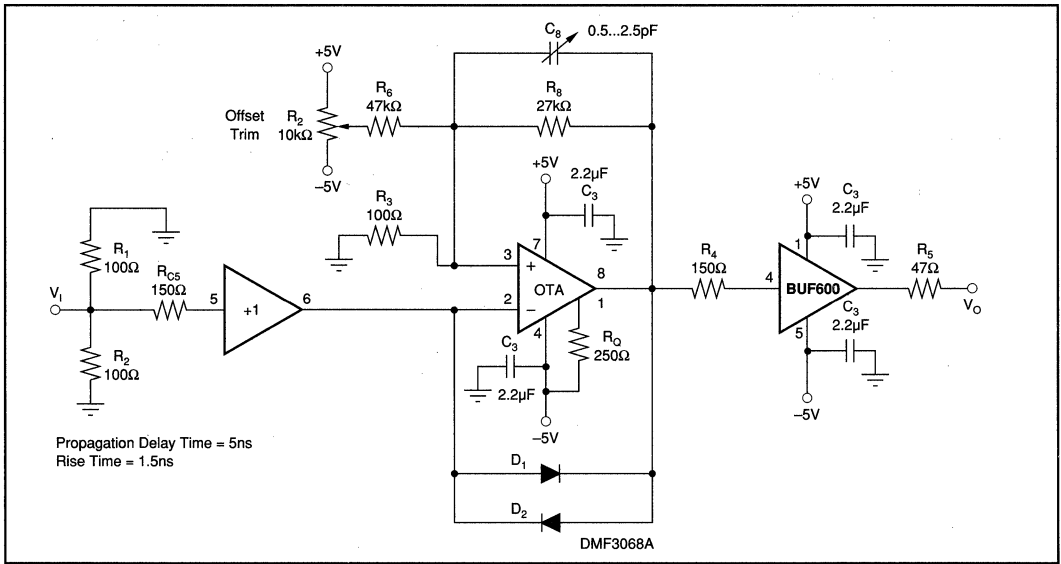


FIGURE 14. Comparator (Low Jitter).

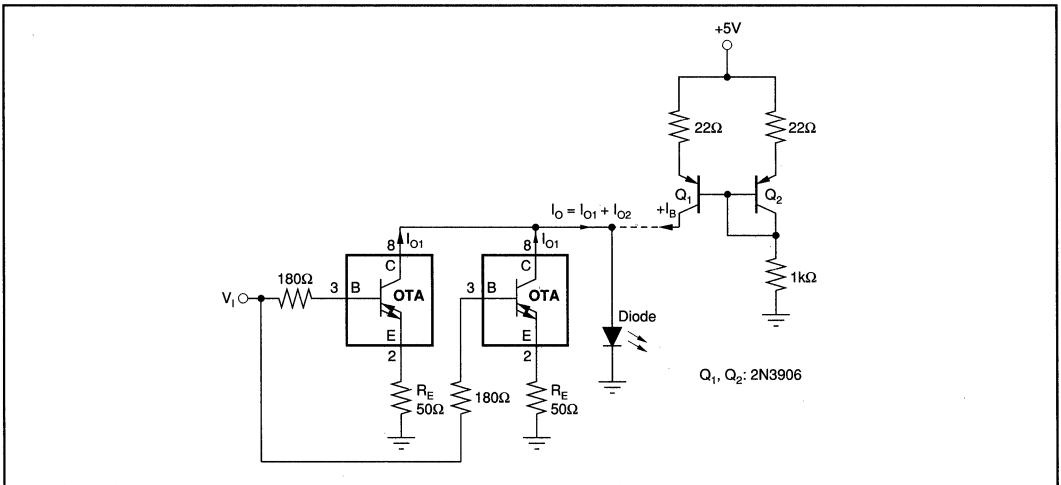


FIGURE 15. High Speed Current Driver.

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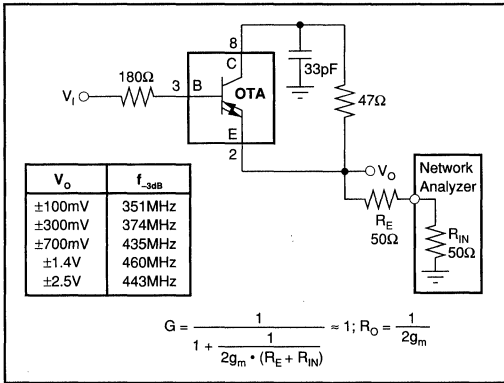


FIGURE 16. Voltage Buffer with Doubled Output Current.

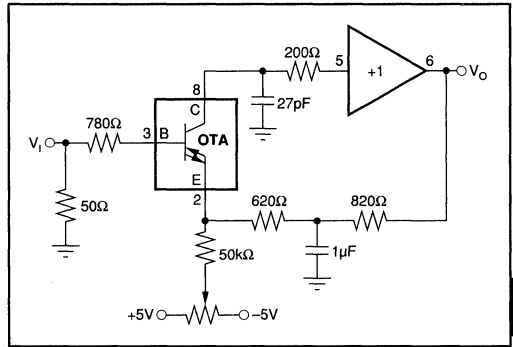


FIGURE 17. Integrator for ns-pulses.

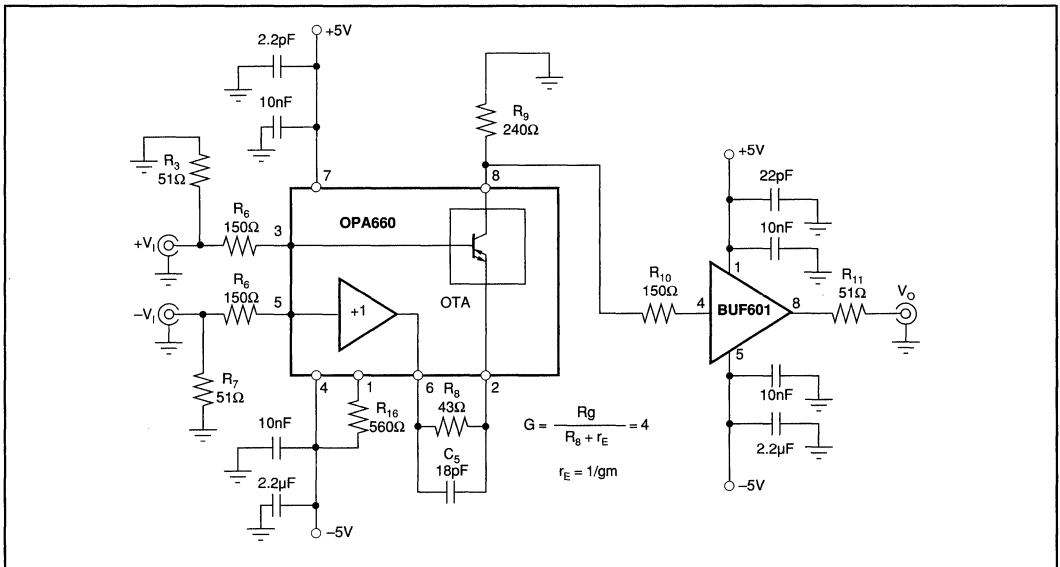


FIGURE 18. 400MHz Differential Amplifier

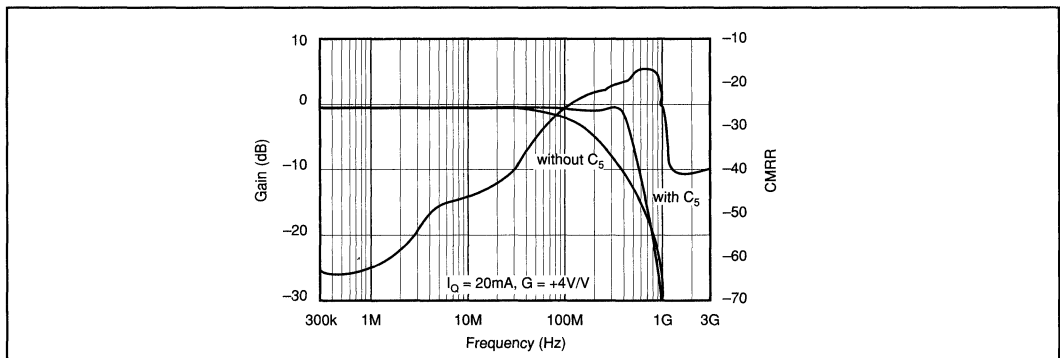


FIGURE 19. CMRR and Bandwidth of the Differential Amplifier

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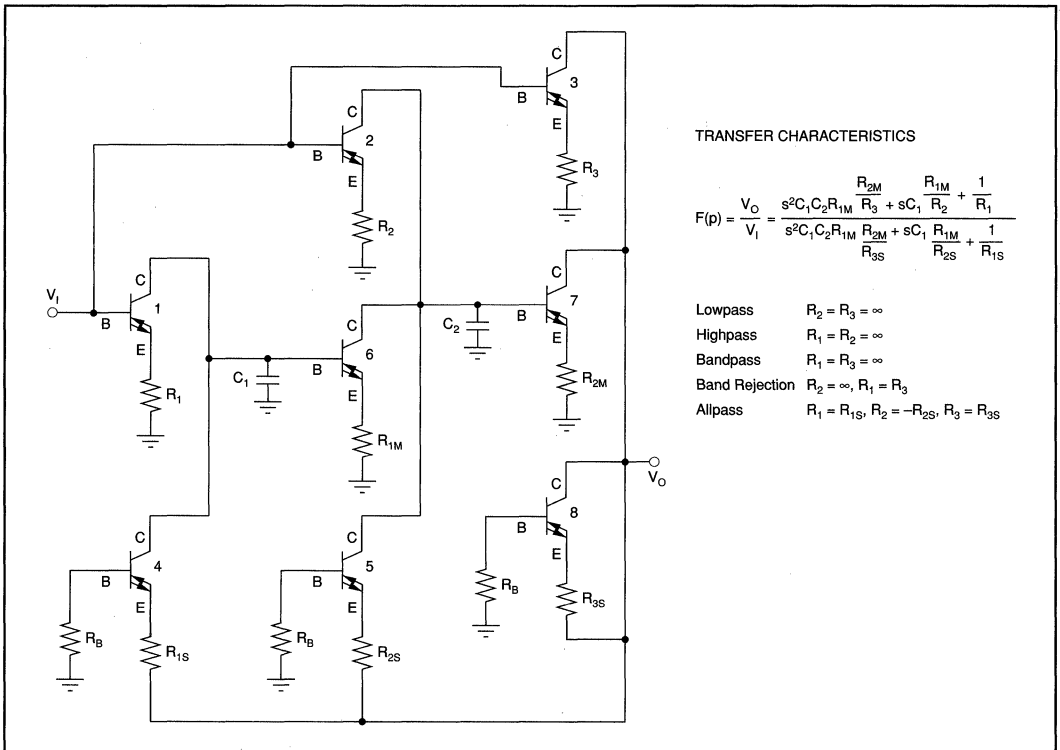


FIGURE 20. Universal Active Filter for the MHz Frequency Range.

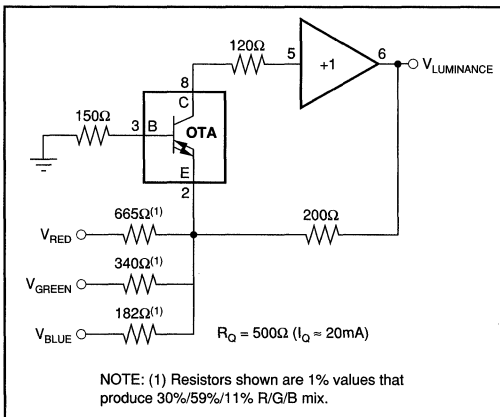


FIGURE 21. Video Luminance Matrix.

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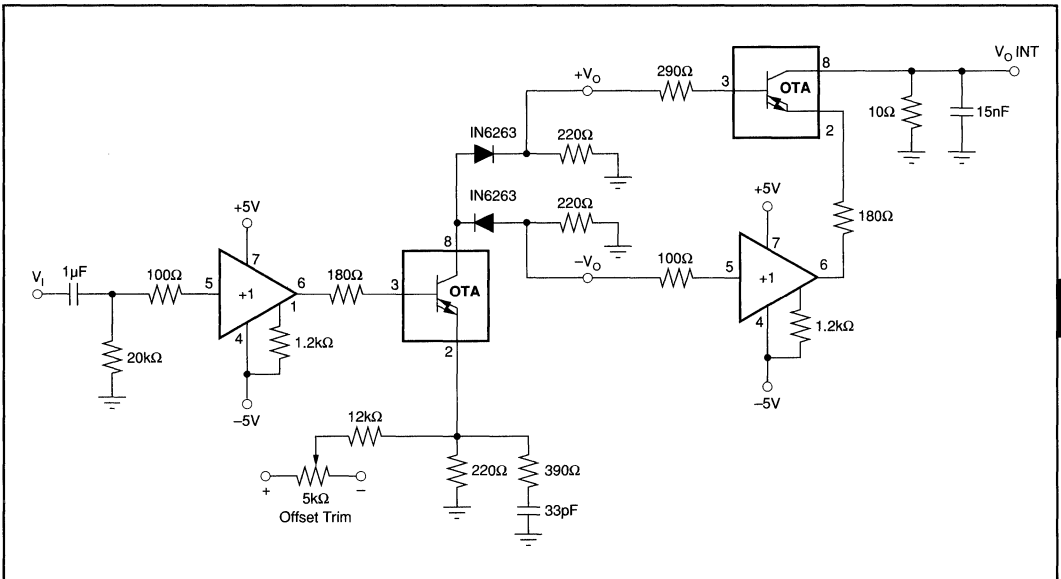


FIGURE 22. Signal Envelope Detector (Full Wave Rectifier).

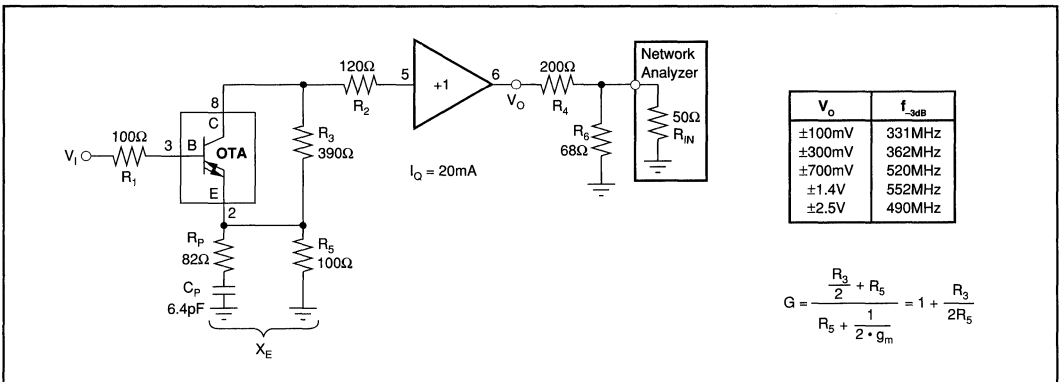


FIGURE 23. Direct-Feedback Amplifier.

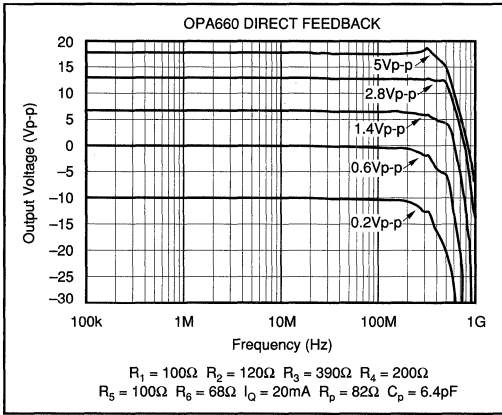


FIGURE 24. Frequency Response Direct-Feedback Amplifier.

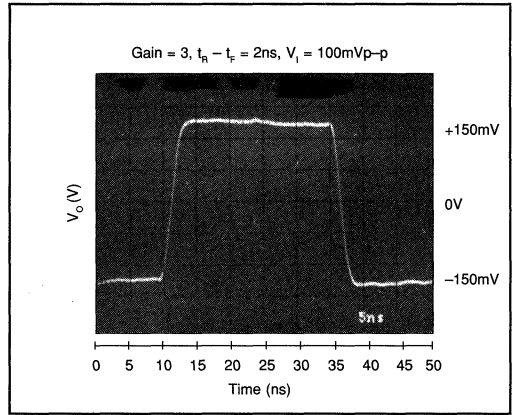


FIGURE 25. Direct-Feedback Amplifier Small-Signal Pulse Response.

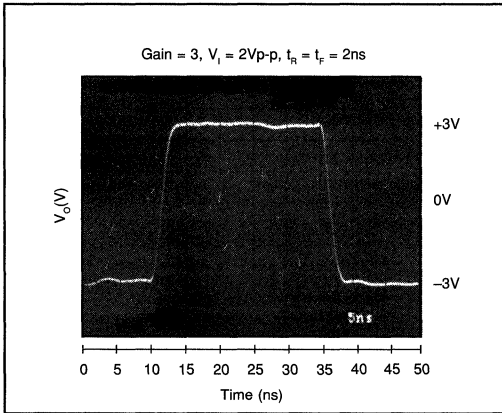


FIGURE 26. Direct-Feedback Amplifier Large-Signal Pulse Response.

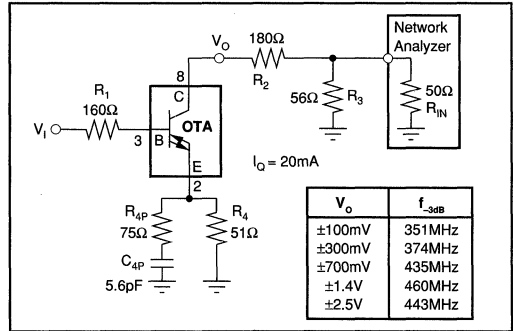


FIGURE 27. Forward Amplifier.

SPICE MODELS

Computer simulation using SPICE models is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using PSPICE from the Micro Sim Corporation are available for the OPA660.

RELIABILITY DATA

Extensive reliability testing has been performed on the OPA660. Accelerated life testing (1000 hours) at $+125^\circ\text{C}$ was used to calculate MTTF at an ambient temperature of $+25^\circ\text{C}$. These test results yield a MTTF of: SO-package = $1.59\text{E} + 07$, and plastic DIP = $1.59\text{E} + 07$ hours. Additional tests such as PTH and ESD have been performed. Reliability reports are available upon request for each of the package options offered.

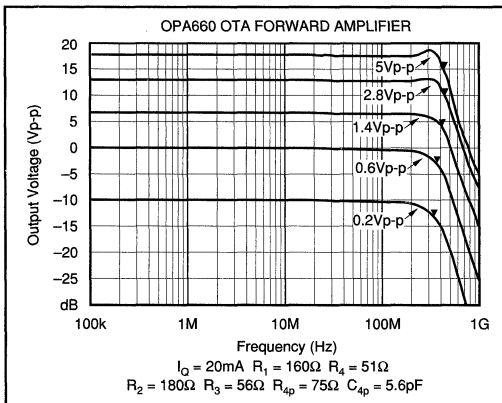


FIGURE 28. Frequency Response Forward Amplifier.

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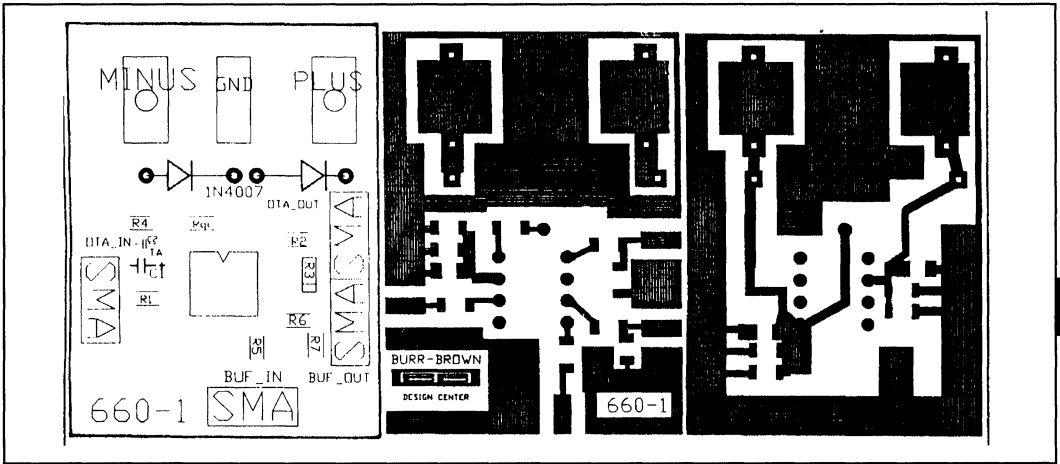


FIGURE 29. Silk Screen and Board Layouts of DEM-OPA660-1GC.

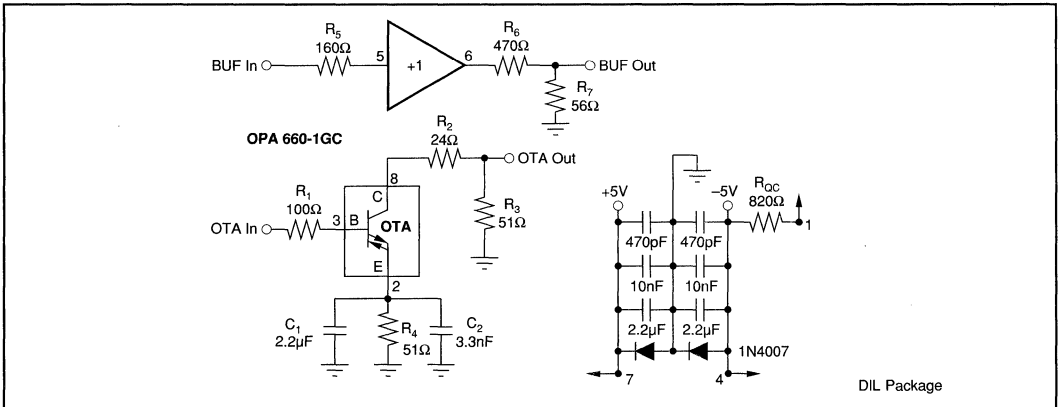


FIGURE 30. Circuit Diagram DEM OPA660-1GC.

DEMONSTRATION BOARDS

Five different demonstration boards are available to speed prototyping. Each of the five demonstration boards has a companion piece of literature which includes information about the component values, basic connection, etc. -1GC to -3GC are completely assembled with the OPA660 in the DIL Package.

DEM-OPA660-1GC	Diamond Transistor and Buffer (LI-407)
DEM-OPA660-2GC	Current-Feedback Operational Amplifier (LI-406)
DEM-OPA660-3GC	Direct-Feedback Amplifier (LI-405)
DEM-OPA660-4G	Layouts for all applications using SOIC packages, unassembled (LI-418)
DEM-OPA660-5G	Layouts for all applications using DIP packages, unassembled (LI-417)

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OPA671

Wide Bandwidth, Fast Settling *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE GAIN-BANDWIDTH: 35MHz
- HIGH SLEW RATE: 100V/μs
- FAST SETTLING: 240ns to 0.01%
- FET INPUT: $I_b = 50\text{pA max}$
- HIGH OUTPUT CURRENT: 50mA
- WIDE SUPPLY RANGE: $V_s = \pm 4.5 // \pm 18\text{V}$

APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTOELECTRONICS
- TRANSIMPEDANCE AMPLIFIER
- LINE DRIVER

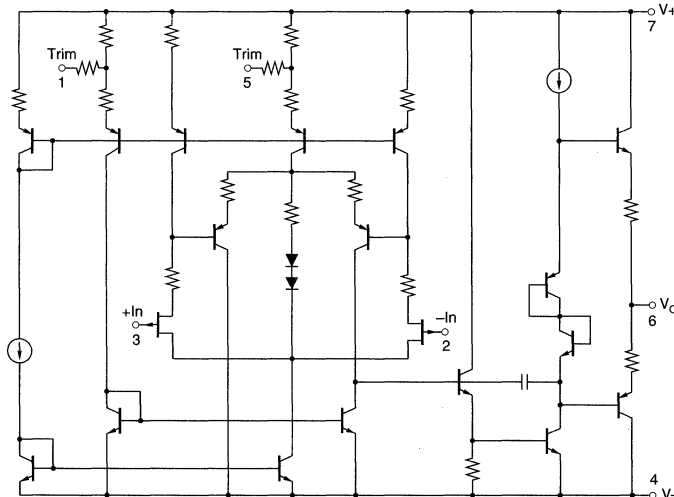
DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's *Difet*, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from $\pm 4.5\text{V}$ to $\pm 18\text{V}$ power supplies. It can deliver $\pm 10\text{V}$ signals into a 200Ω load at slew rates of $100\text{V}/\mu\text{s}$. OPA671's *Difet* input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated and is unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.



Difet[®] Burr-Brown Corporation

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SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITION	OPA671AP			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection	$V_S = \pm 4.5$ to $\pm 16.5\text{V}$	72	± 0.5 ± 10 94	± 5	mV $\mu\text{V}/^\circ\text{C}$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		5 2	50	μA μA
NOISE Input Voltage Noise Noise Density, $f = 100\text{Hz}$ Noise Density, $f = 1\text{kHz}$ Noise Density, $f = 10\text{kHz}$ Noise Density, $f = 100\text{kHz}$ Voltage Noise, BW = 10Hz to 1MHz Input Bias Current Noise Current Noise Density, $f = 10\text{Hz}$ to 1MHz			24 15 12 10 60 2		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	± 12 74	± 13 92		V dB
INPUT IMPEDANCE Differential Common-Mode			$10^{12} \parallel 4.5$ $10^{12} \parallel 6$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 200\Omega$	74	80 78		dB dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.01% Settling Time 0.1% Settling Time 1% Total Harmonic Distortion	$G = -1$, 10V Step $G = -1$, 10V Step $G = -1$, 10V Step $G = -1$, 10V Step $G = 1$, $f = 100\text{kHz}$ $V_O = 3\text{V}$, $R_L = 200\Omega$		35 107 240 150 85 0.0006		MHz V/ μs ns ns ns %
OUTPUT Voltage Output Current Output Short Circuit Current Output Resistance, Open-Loop	$R_L = 200\Omega$ $V_O = \pm 10\text{V}$ DC	± 10.5	± 11.5 50 $-90/+105$ 20		V mA mA Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current		± 4.5	± 15 ± 14.8	± 18 ± 17	V V mA
TEMPERATURE RANGE Specification Operating Storage Thermal Resistance, θ_{JA}		-25 -40 -40	100	+85 +85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTE: (1) Tested without warmup at $T_J = 25^\circ\text{C}$.

OPA671

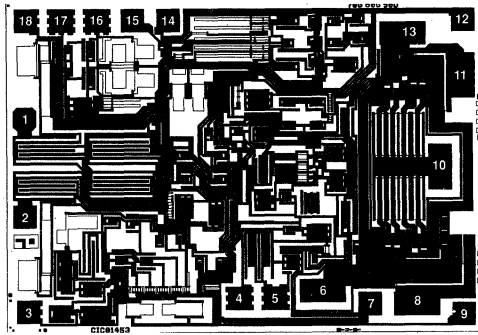
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OPERATIONAL AMPLIFIERS

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.



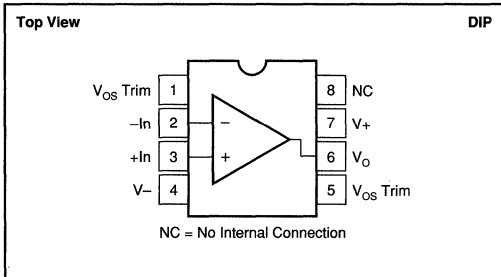
DIE INFORMATION



OPA671 DIE TOPOGRAPHY

PAD	FUNCTION
1	-In
2	+In
3	IQ
4	Comp In
5	Comp Out
6	-Short Circuit Bypass
7	-V
8	-V for O/P Stage
9	Balance 2A
10	Output
11	+V for O/P Stage
12	+V
13	+Short Circuit Bypass
14	Balance 2B
15	Balance 1
16	Slope
17	R_{CM}
18	R_9

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	(V+) +1V to (V-) -1V
Operating Temperature	-40°C to +100°C
Storage Temperature	-40°C to +125°C
Output Short-Circuit to Ground	15s
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA671AP	8-Pin Plastic DIP	-25°C to +85°C

PACKAGE INFORMATION⁽¹⁾

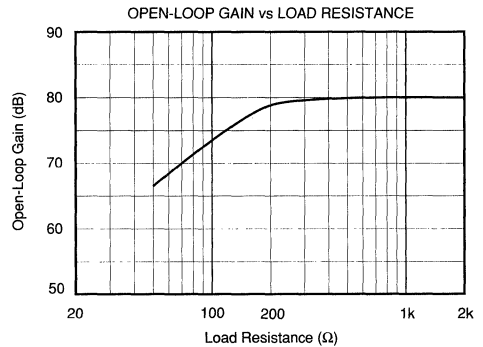
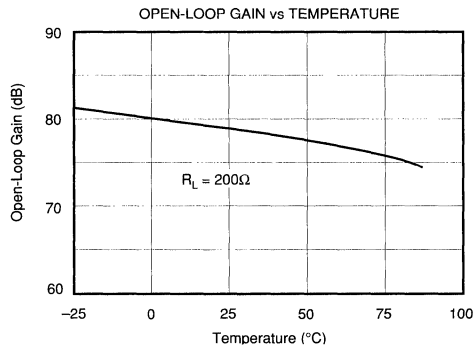
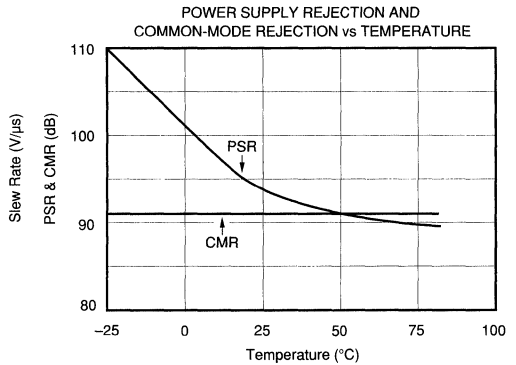
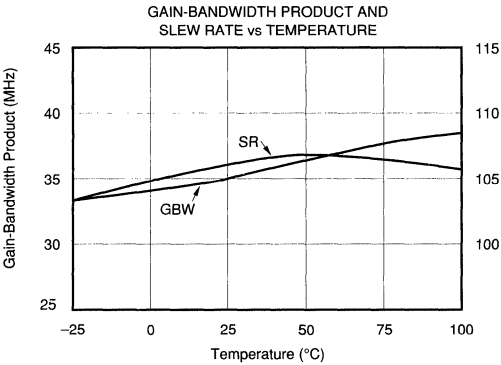
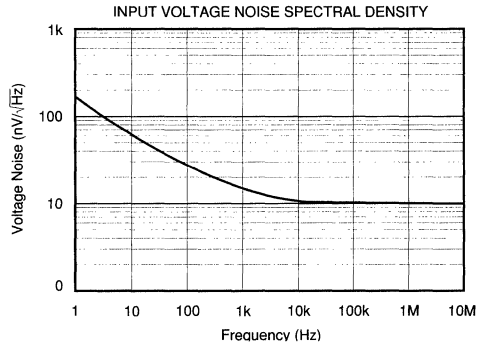
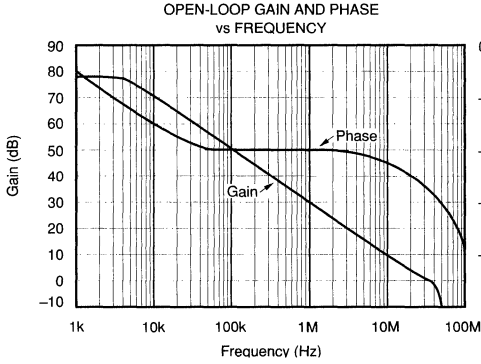
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA671AP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



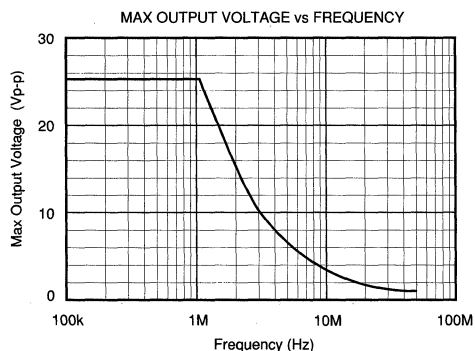
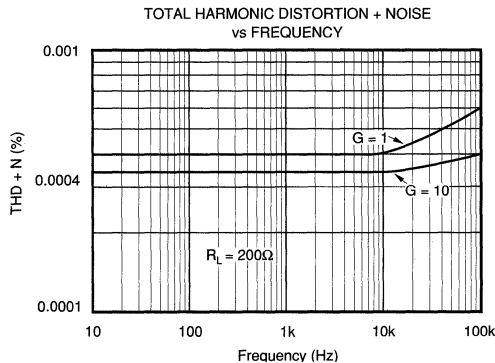
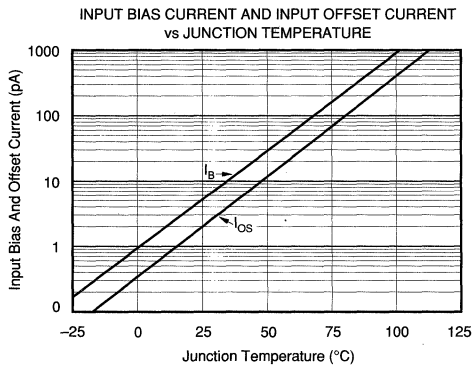
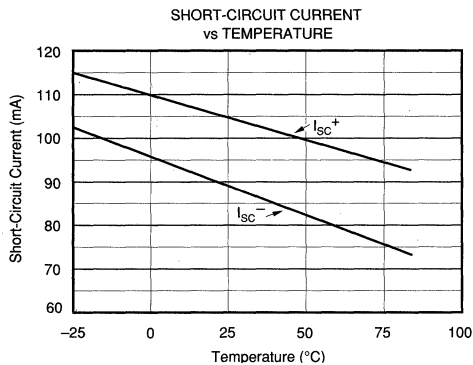
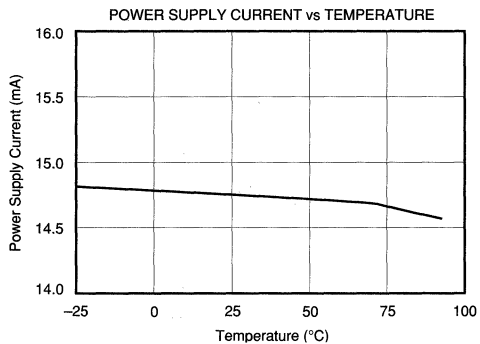
OPA671

OPERATIONAL AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_O = \pm 15\text{V}$ unless otherwise noted.

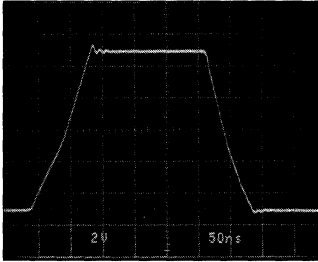


Or, Call Customer Service at 1-800-548-6132 (USA Only)

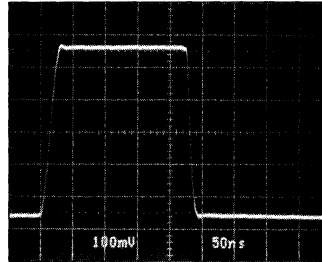
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

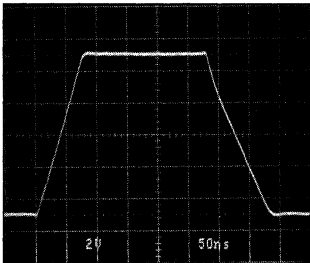
G = +1 LARGE SIGNAL RESPONSE



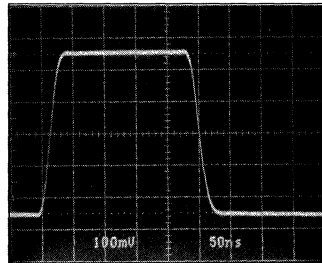
G = +1 SMALL SIGNAL RESPONSE



G = -1 LARGE SIGNAL RESPONSE



G = -1 SMALL SIGNAL RESPONSE



CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

The power supply connections should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a $1\mu\text{F}$ solid tantalum capacitor for each power supply is adequate. The OPA671 can deliver peak load currents up to 100mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as $4.7\mu\text{F}$ solid tantalum capacitors may improve dynamic performance in some applications.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1 shows an optional circuit for trimming the offset voltage. Do not use this offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage temperature drift.

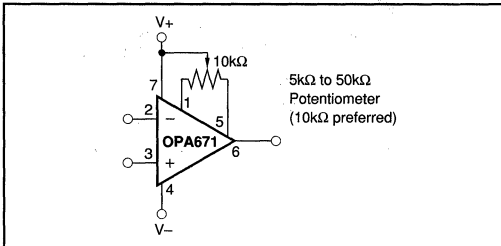


FIGURE 1. Optional Offset Voltage Trim Circuit.

CAPACITIVE LOADS

The OPA671 is internally compensated to be unity-gain stable with minimal capacitive load. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. With wideband op amps, load capacitance as low as 50pF can introduce enough phase shift to degrade dynamic performance. Figure 2 shows circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details on various compensation circuits and analysis techniques.

POWER DISSIPATION

High output current can cause large internal power dissipa-

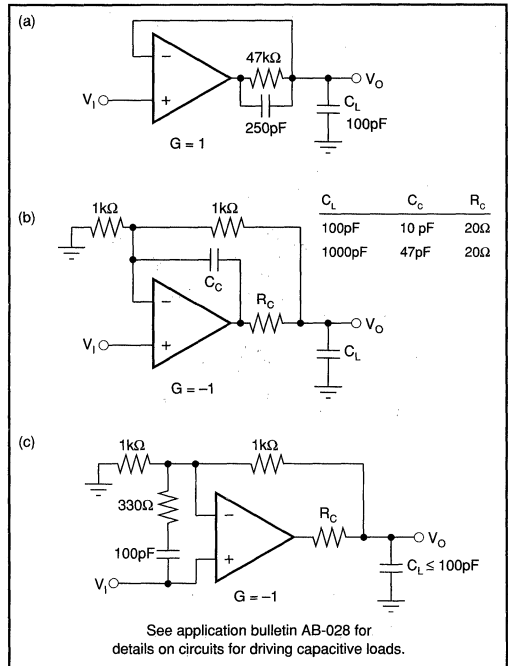


FIGURE 2. Compensation Circuits for Capacitive Loads.

tion in the OPA671. Copper leadframe construction improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces close to the device pins. Limit the ambient temperature, load and signal to assure that the maximum junction temperature is not exceeded. The OPA671 may be operated at reduced power supply voltage to minimize power dissipation.

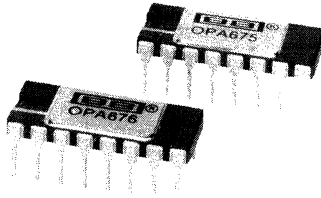
OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately 90mA at 25°C. The short-circuit limit current decreases with increasing junction temperature as shown in the typical curves. The current limit will protect the device from inadvertent short-circuits to ground. The power dissipation under this condition, however, is quite high so short-circuits should be avoided.

INPUT BIAS CURRENT

The OPA671 is fabricated with Burr-Brown's dielectrically isolated *Difet* process, giving it extremely low input bias current. As with other FET-input amplifiers, input bias current approximately doubles with every 10°C increase in junction temperature. Input bias current can be minimized by soldering the device to the circuit board to provided best heat dissipation. Reduced power supply voltage will also minimize input bias current by reducing internal power dissipation.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA675
OPA676

OPA675/676

2

OPERATIONAL AMPLIFIERS

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTling: 9ns (1%)
- WIDE BANDWIDTH: 185MHz ($A_v = 10$)
- LOW OFFSET VOLTAGE: $\pm 250\mu\text{V}$
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 8ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

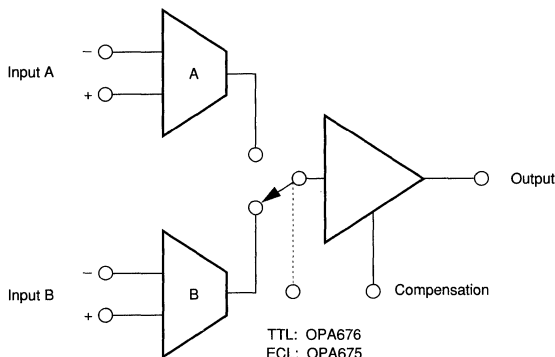
DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its

"classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (-55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 150\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE⁽¹⁾ Voltage: $f_o = 10Hz$ $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$ $f_o = 100kHz$ $f_b = 10Hz$ to 10MHz Current: $f_o = 10Hz$ to 1MHz	$R_S = 0\Omega$		27 10 3.8 2.6 2.4 7.9 2.7			*	*	nV/ \sqrt{Hz} nV/ \sqrt{Hz} nV/ \sqrt{Hz} nV/ \sqrt{Hz} nV/ \sqrt{Hz} μV_{rms} pA/ \sqrt{Hz}
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to T_{MAX} $\pm V_{CC} = 4.5V$ to 5.5V		± 500 ± 3 65	$\pm 2mV$ ± 10 86		± 250 ± 1 70	$\pm 1mV$ ± 5	μV $\mu V/^\circ C$ dB
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0VDC$		23	35		*	30	μA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0VDC$		0.8	5		*	*	μA
INPUT IMPEDANCE⁽¹⁾ Differential Common-Mode			4k 2 10 ⁵ 5			*	*	Ω pF Ω pF
INPUT VOLTAGE RANGE⁽¹⁾ Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 0.5VDC$, $V_O = \pm 1.25V$	± 1.25 75	± 2.5 100		*	*	*	V dB
OPEN LOOP GAIN, DC⁽¹⁾ Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE Closed-Loop Bandwidth Crosstalk Harmonic Distortion: 10MHz Full Power Response Slew Rate Settling Time: 1% 0.1% 0.01%	Gain = +2V/V Gain = +5V/V Gain = +10V/V Gain = +50V/V Gain = +10V/V, $f = 100kHz$ $f = 1MHz$ $f = 10MHz$ $f = 100MHz$ G = +10V/V, $R_L = 50\Omega$, $V_O = 0.5Vp-p$ Second Harmonic Third Harmonic $V_O = 2.5Vp-p$, Gain = +10V/V Gain = +10V/V 0.625V Output Step		100 145 185 60 -100 -80 -68 -35 -61 -73 25 200			*	*	MHz MHz MHz MHz dBC ⁽²⁾ dBC dBC dBC dBC dBC MHz V/ μs ns ns ns
INPUT SELECTION⁽³⁾ Transition Time 50% In to 50% Out	ECL: OPA675 TTL: OPA676		5 7.5			*	*	ns ns
DIGITAL INPUT TTL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH} ECL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH}	Logic "LO" Logic "HI" Logic "LO", $V_{IL} = 0V$ Logic "HI", $V_{IH} = +2.7V$ Logic "LO" Logic "HI" Logic "LO", $V_{IL} = -1.6V$ Logic "HI", $V_{IH} = -1.0V$	0 +2.0 -1.81 -1.15		+0.8 +5 -0.05 1 -1.475 -0.88 -50 -50		*	*	V V mA μA V V μA μA
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 150\Omega$ $R_L = 50\Omega$ 1MHz, Open Loop, $C_C = 5pF$ Gain = +2V/V Continuous to Gnd	± 2.1 +1.25 -0.95	± 2.6 +1.8 -1.1 ± 30 5 50 +45 -25		*	*	*	V V V mA Ω pF mA mA

* Same specifications as for JG.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 150\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5		*	*	*	VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*	*	*	VDC
Current, Quiescent	$I_0 = 0mADC$		22	30	*	*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG SG	0		+70	*	*	*	$^\circ C$
Operating:	Ambient Temp JG, KG, SG	-55		+125	*	*	*	$^\circ C$
θ_{JA}		-55	125	+125	*	*	*	$^\circ C/W$

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 5VDC$, $R_L = 150\Omega$, and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG SG	0		+70	*	*	*	$^\circ C$
		-55		+125	*	*	*	$^\circ C$
OFFSET VOLTAGE								
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 3	± 10		± 1	± 5	$\mu V/^\circ C$
Supply Rejection	$\pm V_{CC} = 4.5V$ to $5.5V$	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	$V_{CM} = 0VDC$		29	50		*	*	μA
OFFSET CURRENT								
Input Offset Current	$V_{CM} = 0VDC$		0.8	10		*	*	μA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		± 2.0	± 2.3		*	*		V
Common-Mode Rejection	$V_{IN} = \pm 0.5VDC$, $V_O = \pm 1.25V$	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic "LO"	0		+0.8	*	*	*	V
V_{IH}	Logic "HI"	+2.0		+5	*	*	*	V
I_{IL}	Logic "LO", $V_{IL} = 0V$		-0.08	-0.4		*	*	mA
I_{IH}	Logic "HI", $V_{IH} = +2.7V$		5	50		*	*	μA
ECL Logic Levels: V_{IL}	Logic "LO"	-1.81		-1.475	*	*	*	V
V_{IH}	Logic "HI"	-1.15		-0.88	*	*	*	V
I_{IL}	Logic "LO", $V_{IL} = -1.6V$		-50			*	*	μA
I_{IH}	Logic "HI", $V_{IH} = -1.0V$		-50			*	*	μA
RATED OUTPUT								
Voltage Output	$R_L = 150\Omega$	± 2.0	± 2.5		*	*	*	V
	$R_L = 50\Omega$	+1.25	+1.6		*	*	*	V
		-0.8	-1.0		-0.9	*	*	V
POWER SUPPLY								
Current, Quiescent	$I_0 = 0mADC$		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dB = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

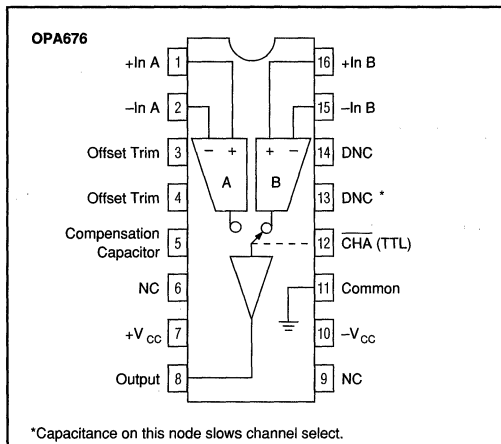
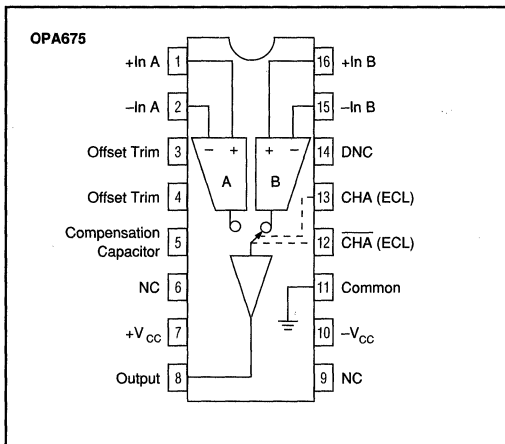
OPA675/676

2

OPERATIONAL AMPLIFIERS

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATIONS



*Capacitance on this node slows channel select.

PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	-In A	15	-In B
3	Offset Trim	14	DNC
4	Offset Trim	13	CHA (ECL)
5	Compensation Capacitor	12	CHA (ECL)
6	NC	11	Common
7	+V _{cc}	10	-V _{cc}
8	Output	9	NC

DNC = Do Not Connect

NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	-In A	15	-In B
3	Offset Trim	14	DNC
4	Offset Trim	13	DNC
5	Compensation Capacitor	12	CHA (TTL)
6	NC	11	Common
7	+V _{cc}	10	-V _{cc}
8	Output	9	NC

DNC = Do Not Connect

NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V _{cc}
Input Voltage Range (Analog and Digital)	±V _{cc}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

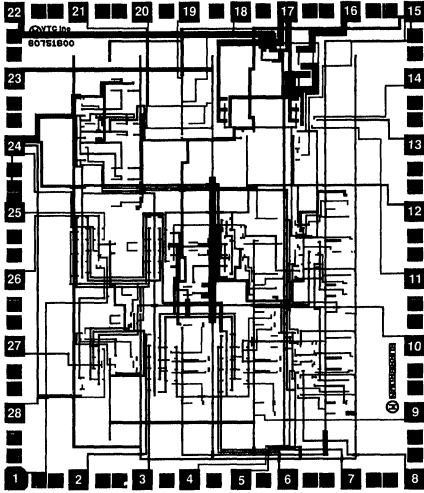
	OPA675	() ()
	OPA676	() ()
Basic Model Number		
Performance Grade Code		
J, K: 0°C to +70°C		
S: -55°C to +125°C		
Package Code		
G: 16-pin Ceramic DIP		

PACKAGE INFORMATION (1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA675/76JG	16-Pin Hermetic DIP	109
OPA675/76SG	16-Pin Hermetic DIP	109
OPA675/76KG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



OPA675/676 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	TTL Set	15	+V _{CC}
2	-I _{nA}	16	+V _{CC}
3	+I _{nA}	17	V _{OUT}
4	NC	18	NC
5	NC	19	NC
6	+I _{nA}	20	NC
7	-I _{nA}	21	NC
8	NC	22	-V _{CC}
9	V _{OS} Adjust	23	-V _{CC}
10	V _{OS} Adjust	24	Ground
11	NC	25	CHA (TTL)
12	Comp Cap	26	ECL _{OUT}
13	NC	27	CHA (ECL)
14	NC	28	CHA (ECL)

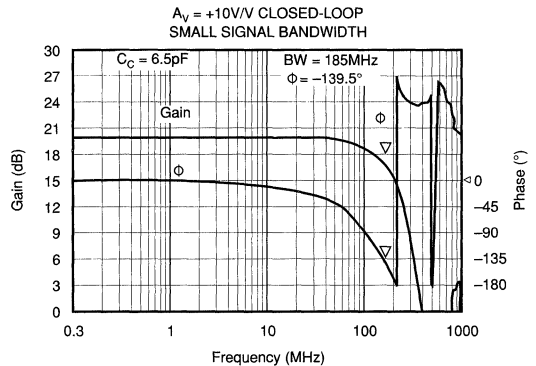
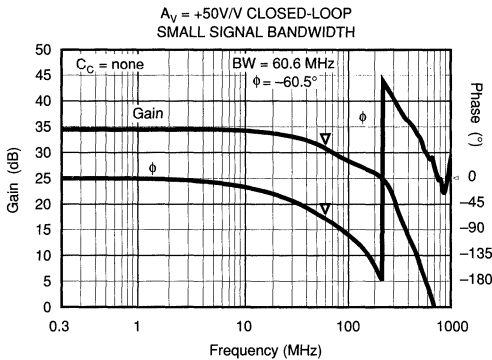
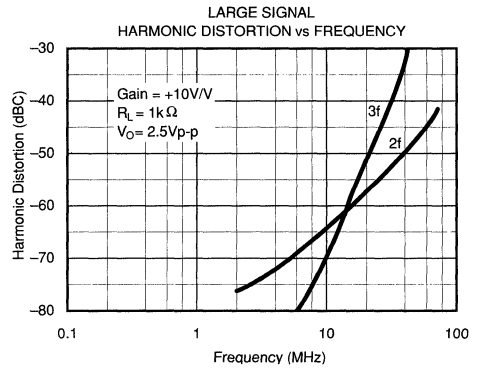
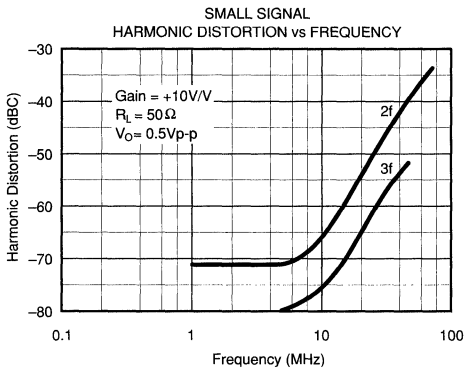
NC: No Connection (Do Not Connect). OPA675-Do not use pads 1, 25, 26. OPA676-Connect pad 26 to pad 27. Connect pad 1 to pad 28.

Substrate Bias: -V_{CC}

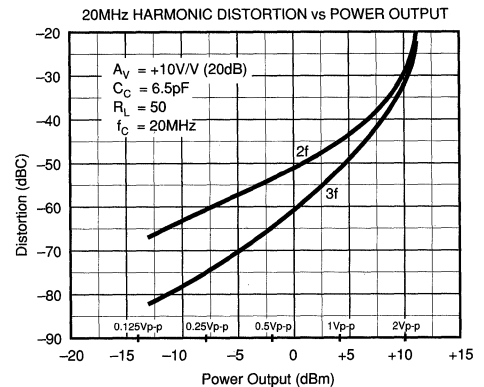
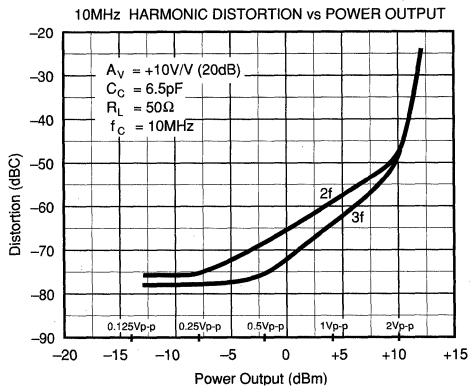
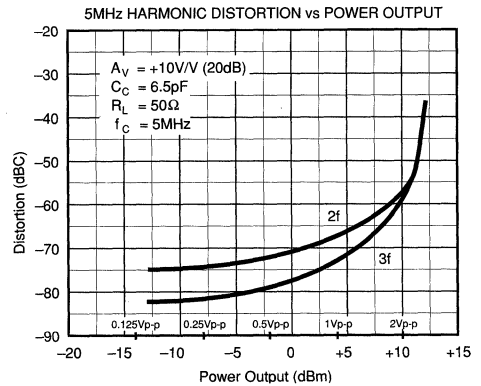
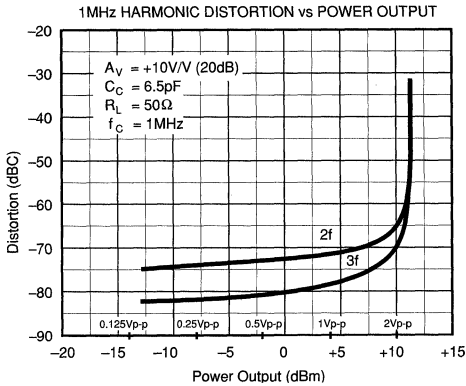
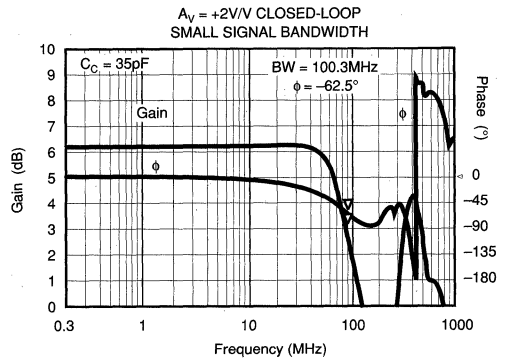
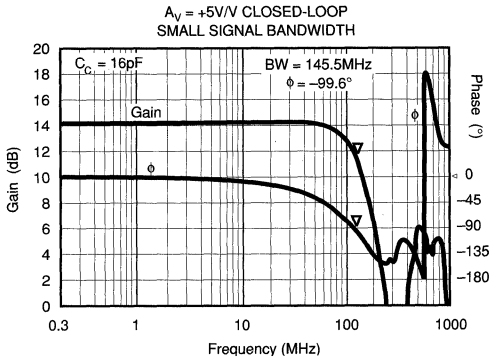
MECHANICAL INFORMATION

	MILS (0.001")
Die Size	103 x 90 ±5
Die Thickness	20 ±3

TYPICAL PERFORMANCE CURVES

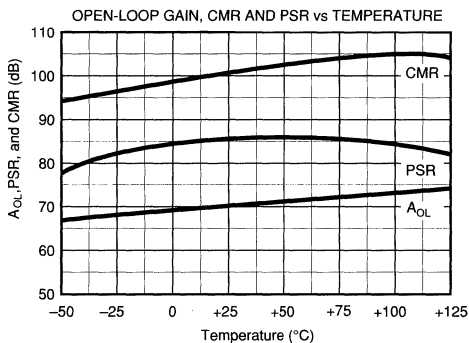
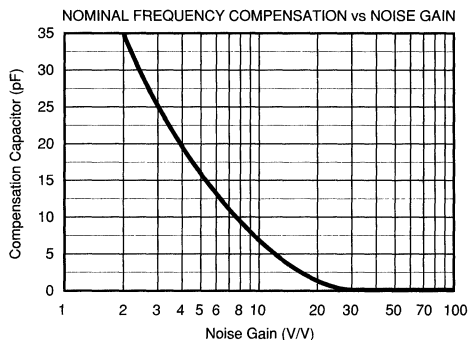
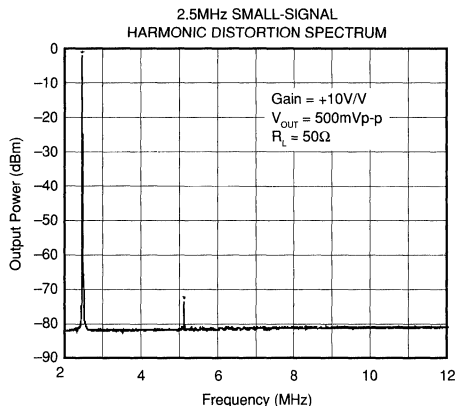
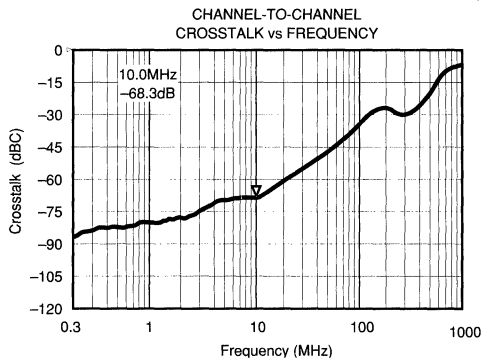


TYPICAL PERFORMANCE CURVES (CONT)



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)



OPA675/676

2 OPERATIONAL AMPLIFIERS

THEORY OF OPERATION

An OPA675 simplified circuit is shown in Figure 1. It is a “classical” high-speed op-amp architecture with one important exception — the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and \bar{A} (labeled B Select) will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to

each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier’s output stage.

The switched-input op amp (SWOP AMP) circuit of the OPA676 is basically the same as the OPA675 but a TTL compatible level shifter (Figure 2) has been added to its input selection logic circuit.

Standard TTL (OPA676) and ECL (OPA675) logic levels may be applied to each input selection circuit but only

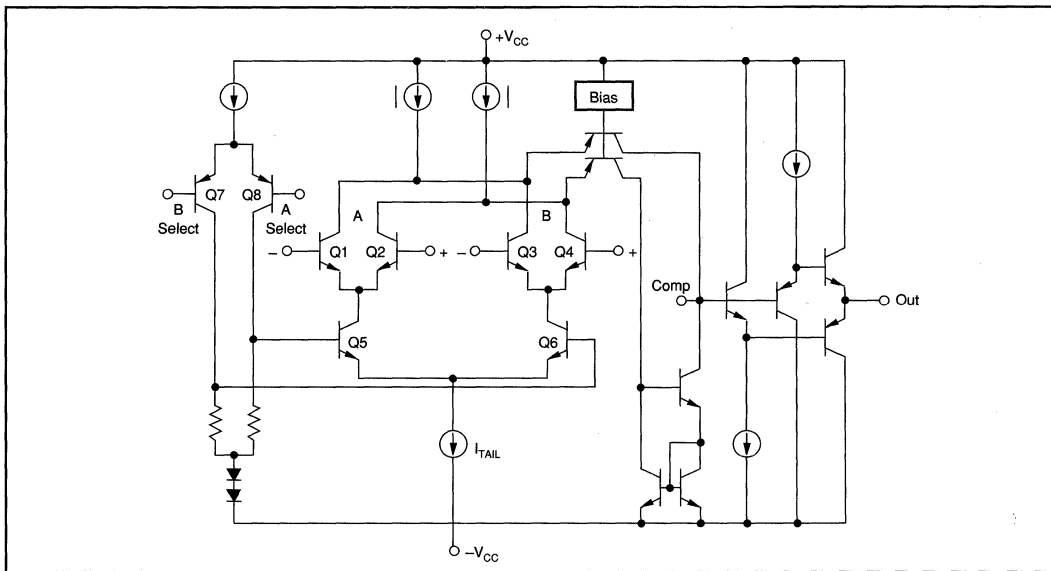


FIGURE 1. OPA675 Simplified Circuit Diagram.

350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

The OPA675 and OPA676 are designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in Typical Performance Curves. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. This amplifier is designed for optimum performance in gains of 5V/V to 20V/V, but it can also be used over a far wider

range of gains with excellent results. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

Input offset voltage is low enough for many video applications. If desired, offset voltage can be trimmed with a 1k Ω potentiometer connected to $+V_{CC}$. Trimming offset voltage in this manner will effect both input A and input B; independent control of input offset will require that trim adjust current be summed into one or both inputs. This technique is shown in a few applications circuits on the pages to follow.

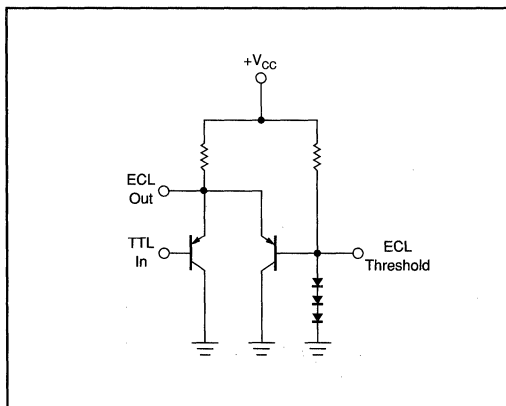


FIGURE 2. Internal OPA676 TTL Logic Level Shifter.

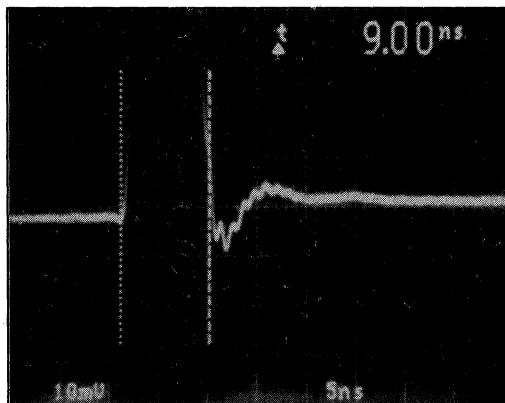


FIGURE 3. 1% Settling Time.

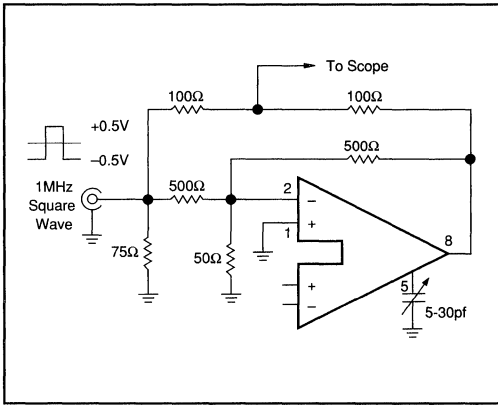


FIGURE 4. OPA675/676 Settling Time Test Circuit.

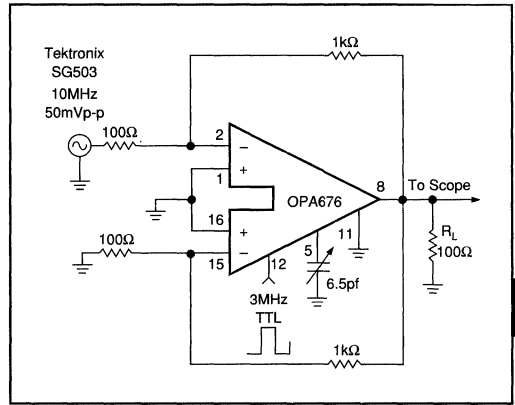


FIGURE 5. OPA676 Input Selection Transition Time Test Circuit.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2oz copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA675/676. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA675 and OPA676 are no different in this respect — any amplifier with a gain bandwidth product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of tantalum capacitors (1 to 10 μ F/10V) with very short leads is highly recommended. Supply pins should not be left unbypassed.
3. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc. should have lead lengths no longer than 1/4 inch (6cm).
4. Surface mount components (chip resistors, capacitors, etc.) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
5. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1k Ω or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
6. Wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high frequency circuits.
7. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
8. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
9. Don't forget that these amplifiers use ± 5 V supplies. Although they will operate perfectly well with +5V and -5.2V, the use of ± 15 V supplies will result in destruction.
10. Standard commercial test equipment has not been designed to test devices in the OPA675/676 speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
11. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
12. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
13. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
14. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.

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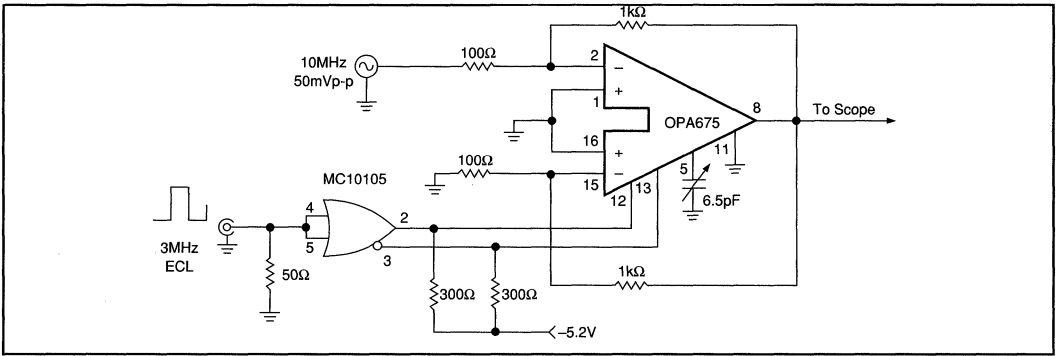


FIGURE 6. OPA675 Input Selection Transition Time Test Circuit.

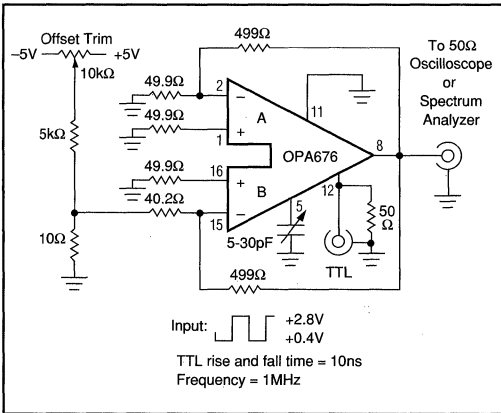


FIGURE 7. OPA676 Carrier Feedthrough and Switching Transient Test Circuit.

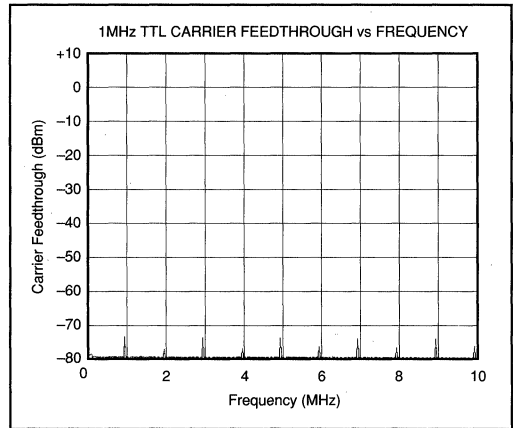


FIGURE 9. Carrier Feedthrough from 1MHz TTL Logic. Offset Trimmed for Maximum Carrier Rejection.

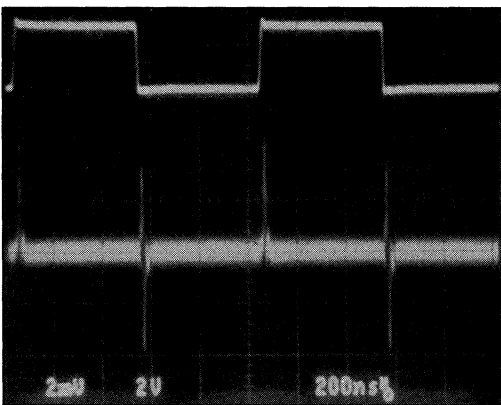


FIGURE 8. OPA676 Switching Transient. Top Trace: TTL Input (2V/cm). Bottom Trace: Amplifier Output (2mV/cm). Input B Offset Voltage has been Trimmed to Match Input A Offset Voltage.

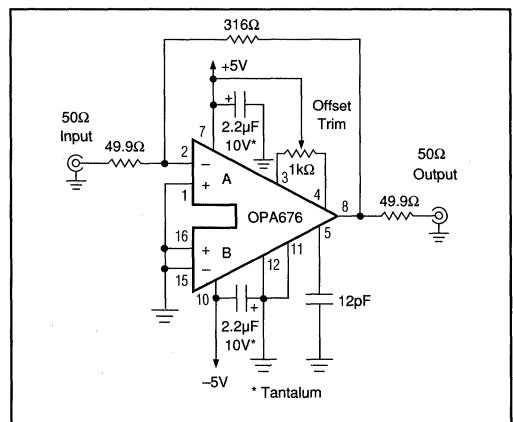


FIGURE 10. OPA676 Used as a Conventional Op Amp: A 10dB Gain Wideband Video Amplifier with 50Ω Input/Output Impedance.

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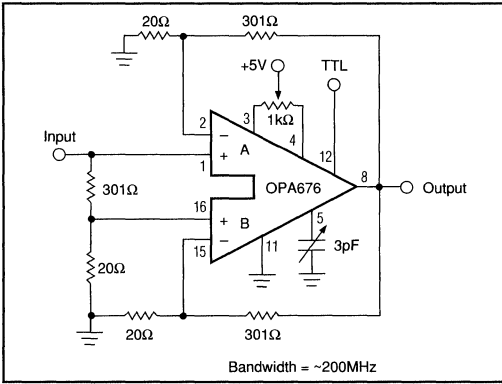


FIGURE 11. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +16V/V (0dB and 24dB).

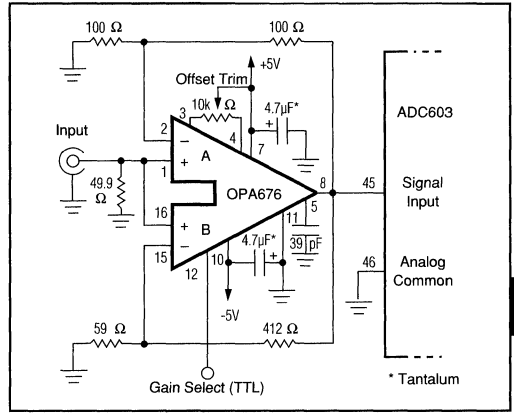


FIGURE 12. Programmable-Gain +2V/V (6dB) or +8V/V (18dB) Buffer Amplifier for Floating-Point Conversion.

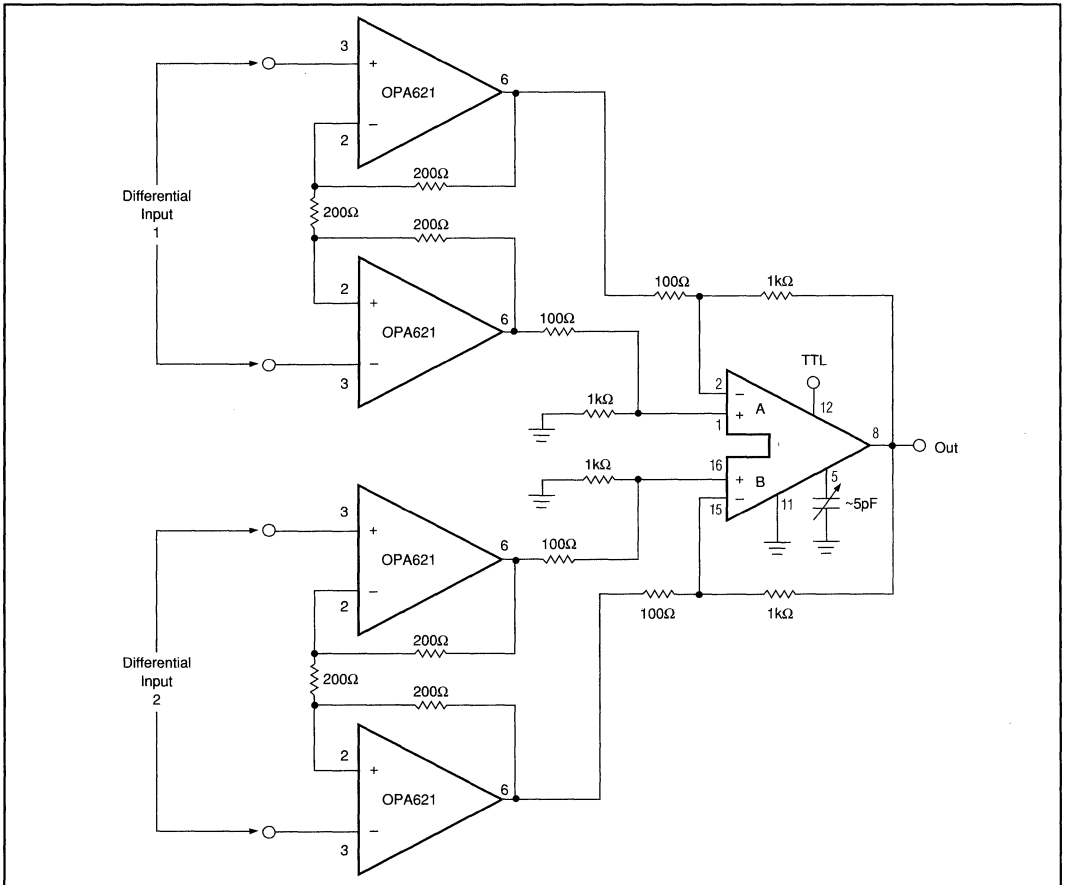


FIGURE 13. High Input Impedance Differential Input Multiplexer with Gain of 30V/V (30dB).

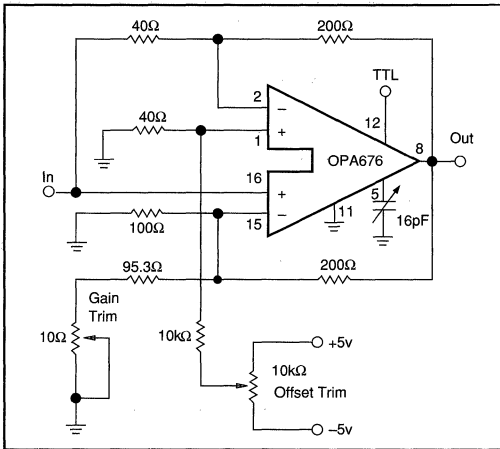


FIGURE 14. Synchronous Modulator/Demodulator with Carrier Balance Trim (Gain = $\pm 5V/V$).

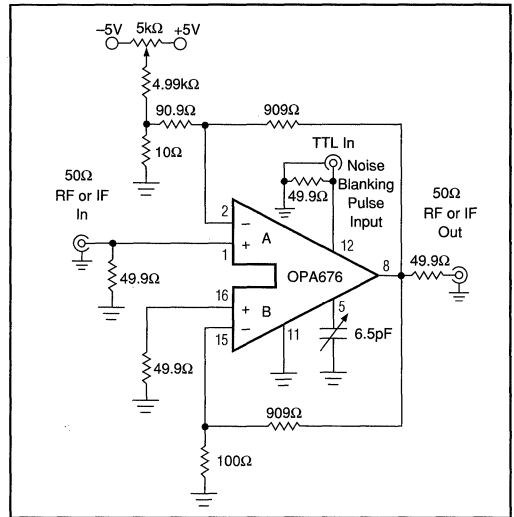


FIGURE 16. Receiver Noise Blanker: A Wideband Gated Video Amplifier.

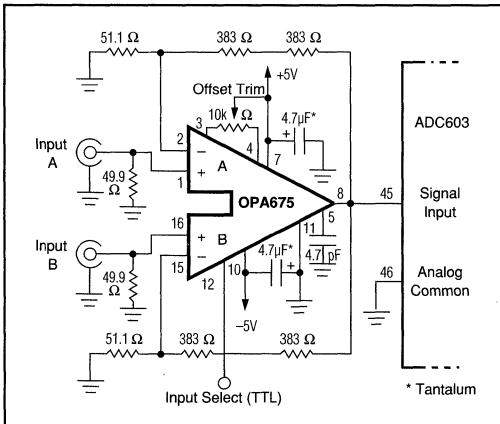


FIGURE 15. Multiplexed Input +16V/V Gain (24dB) Buffer Amplifier.

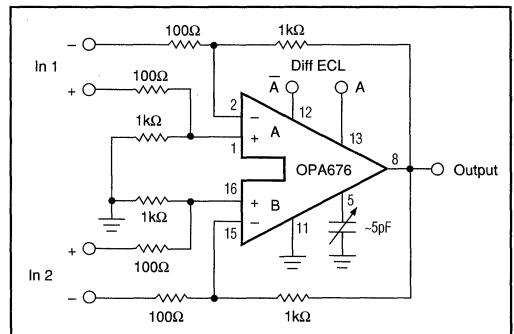


FIGURE 17. Differential Input Multiplexer with Gain of 10V/V (20dB).

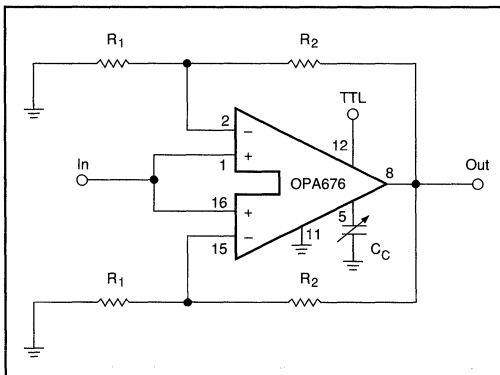


FIGURE 18. Programmable-Gain Amplifier.

VOLTAGE GAIN (V/V)	R ₁ (Ω)	R ₂ (Ω)	C _c (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5

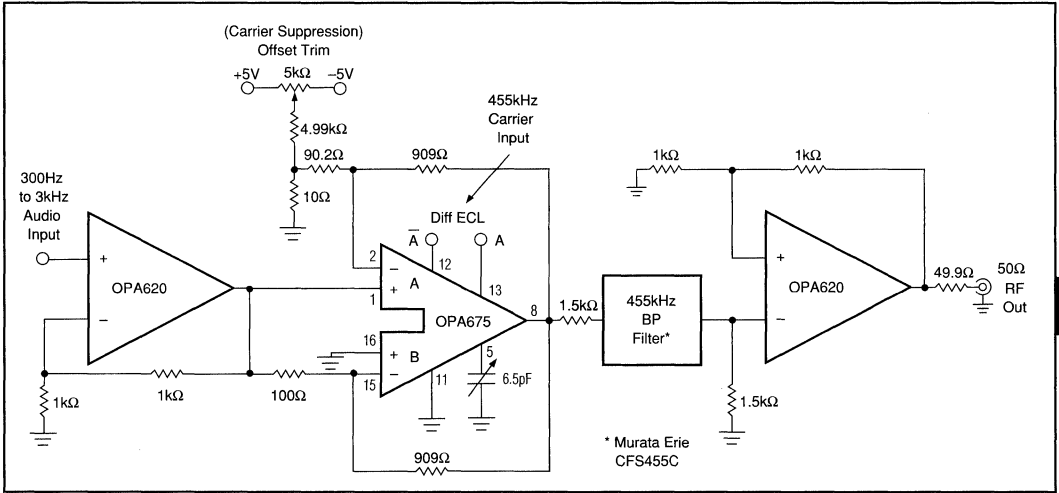


FIGURE 19. Single Sideband Suppressed Carrier Generator.

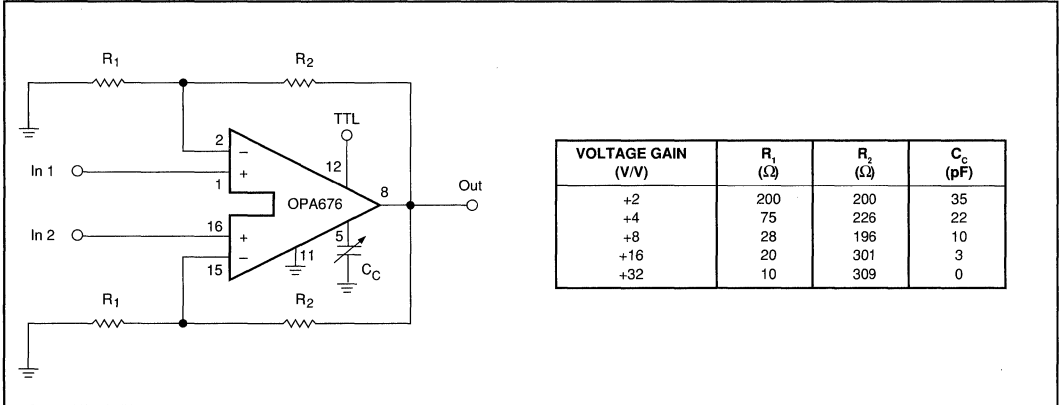


FIGURE 20. Two-Input Multiplexer (with gain).

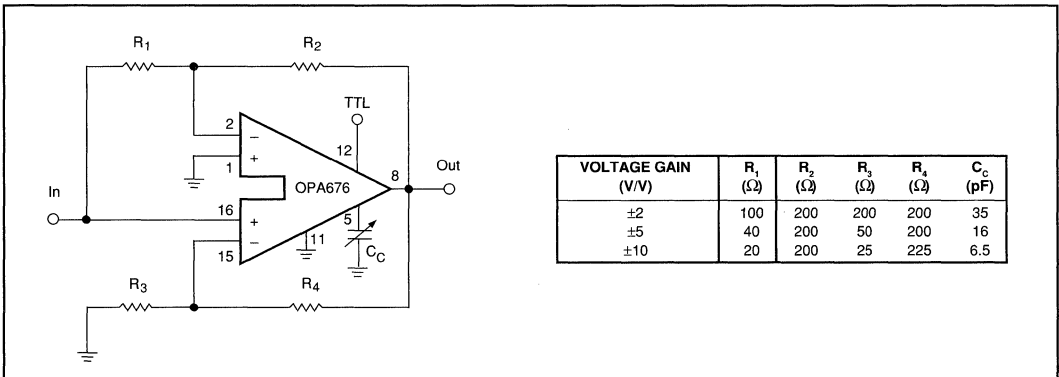
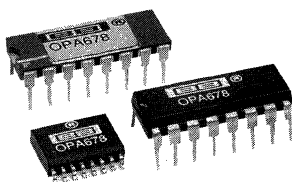


FIGURE 21. Synchronous Modulator/Demodulator (with gain).



OPA678

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 11ns (1%)
- WIDE BANDWIDTH: 200MHz
- TWO LOGIC SELECTABLE INPUTS
- LOW OFFSET VOLTAGE: $\pm 380\mu\text{V}$
- FAST INPUT SWITCHING: 4ns
- ACCEPTS TTL/ECL SWITCHING SIGNALS
- UNITY GAIN STABLE
- 16-PIN DIP AND SOIC PACKAGES

APPLICATIONS

- VIDEO AMPLIFICATION AND SWITCHING
- FAST 2-INPUT MULTIPLEXER
- PULSE/RF AMPLIFIERS
- PROGRAMMABLE-GAIN AMPLIFIER
- ACTIVE FILTERS
- SYNCHRONOUS DEMODULATOR

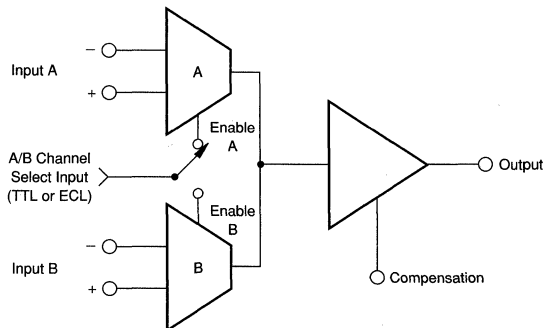
DESCRIPTION

The OPA678 is a wideband monolithic operational amplifier with two independent differential inputs. Either input can be selected by an external TTL or ECL logic signal. The amplifier is externally compensated and features a very fast input selection speed, 4ns for either ECL or TTL. This amplifier features fully symmetrical differential inputs due to its "classical" operational am-

plifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA678 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make this amplifier suitable for RF and video applications.

The OPA678 is available in DIP, SOIC, and sidebraze packages. A military temperature range part is available in the sidebraze package.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_L = 150\Omega$, $C_{COMP} = 5pF$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE⁽¹⁾ Voltage: $f_o = 100Hz$ $f_o = 1kHz$ $f_o = 10kHz$ $f_o = 100kHz$ $f_b = 10Hz$ to $10MHz$ Current: $f_o = 10Hz$ to $1MHz$	$R_s = 0\Omega$		55 21 7.8 4.9 18 2.1			*	*	nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} nV/\sqrt{Hz} μV_{rms} pA/\sqrt{Hz}
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Offset Voltage Drift Supply Rejection	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to T_{MAX} $\pm V_{CC} = 4.5V$ to $5.5V$		± 380 ± 3 71	$\pm 1.5mV$ ± 15		± 380 ± 3 *	$\pm 1mV$ ± 10	μV $\mu V/^\circ C$ dB
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0VDC$		14	50		*	*	μA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0VDC$		0.2	2		*	1.5	μA
INPUT IMPEDANCE⁽¹⁾ Differential Common-Mode			25k 2 10 ⁹ 5			*	*	Ω pF Ω pF
INPUT VOLTAGE RANGE⁽¹⁾ Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 0.5VDC$, $V_O = \pm 1.25V$	2.0 75	± 2.5 85		*	*		V dB
OPEN LOOP GAIN, DC⁽¹⁾ Open-Loop Voltage Gain		50	60		*	*		dB
FREQUENCY RESPONSE Closed-Loop Bandwidth Crosstalk Harmonic Distortion: 5MHz Large Signal Response ⁽⁴⁾ Slew Rate Settling Time: 1% 0.1% 0.01% Differential Gain (0V to 0.7V) Differential Phase (0V to 0.7V)	Gain = +1V/V, $C_C = 9pF$ Gain = +2V/V, $C_C = 7pF$ Gain = +5V/V, $C_C = 1pF$ Gain = +1V/V, $f = 100kHz$ $f = 1MHz$ $f = 10MHz$ $f = 100MHz$ G = +1V/V, $R_L = 150\Omega$, $V_O = 0.25V_{p-p}$ Second Harmonic Third Harmonic $V_O = 2.5V_{p-p}$, Gain = +1V/V Gain = +1V/V Gain = -1V/V, $1V_{OUT}$ Step 4.5MHz, Gain = +2V/V, $C_C = 2.2pF$ 4.5MHz, Gain = +2V/V, $C_C = 2.2pF$	140	200 100 70 -102 -83 -64 -44		*	*		MHz MHz MHz dB ⁽²⁾ dB ⁽²⁾ dB ⁽²⁾ dB ⁽²⁾ dB ⁽³⁾ dB ⁽³⁾ MHz V/ μs ns ns ns % Degrees
INPUT SELECTION⁽⁵⁾ Transition Time 50% In to 50% Out	ECL: Operation TTL: Operation		4 4	8 8		*	9 9	ns ns
DIGITAL INPUT TTL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH} ECL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH}	Logic "LO" Logic "HI" Logic "LO", $V_{IL} = 0V$ Logic "HI", $V_{IH} = +2.7V$ Logic "LO" Logic "HI" Logic "LO", $V_{IL} = -1.6V$ Logic "HI", $V_{IH} = -1.0V$	0 +2.0 -1.81 -1.15	-0.05 1	+0.8 +5 -0.2 20 -1.475 -0.88 -50 -100 -50 -100	*	*	*	V V mA μA V V μA μA
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 150\Omega$ $R_L = 50\Omega$ 1MHz, Open Loop, $C_C = 5pF$ $R_L = 100\Omega$, Gain = +1V/V, $C_C = 10pF$ Continuous to Gnd	± 2.5 ± 1.7 ± 30	± 3.75 ± 2.2 ± 44 5 17 +45		*	*		V V mA Ω pF mA

OPA678

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OPERATIONAL AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm 5\text{VDC}$, $R_L = 150\Omega$, $C_{COMP} = 5\text{pF}$, and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY Rated Voltage Derated Performance Current, Quiescent	$\pm V_{CC}$ $\pm V_{CC}$ $I_O = 0\text{mADC}$	4.5	5 26	5.5 30	*	*	*	VDC VDC mA
TEMPERATURE RANGE Specification θ_{JA}	Ambient Temp AG, AP, AU SG AG, SG AP AU	-40 -55		+85 +125	*		*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$

* Same specifications as for OPA678AG/AP/AU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 5\text{VDC}$, $R_L = 150\Omega$, $C_{COMP} = 5\text{pF}$, and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

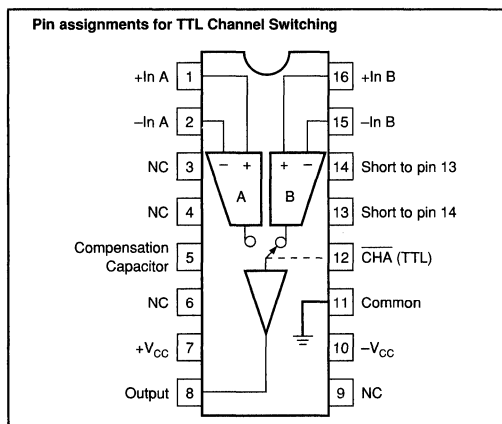
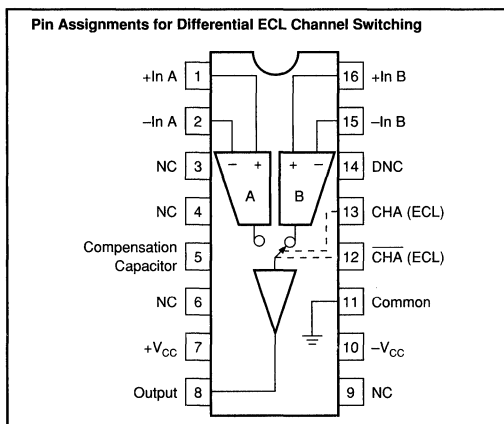
PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification	Ambient Temp AG/AP/AU SG	-40		+85	*		*	$^\circ\text{C}$ $^\circ\text{C}$
OFFSET VOLTAGE Input Offset Voltage Offset Voltage Drift Supply Rejection	$T_A = T_{MIN}$ to T_{MAX} SG $T_A = T_{MIN}$ to T_{MAX} $\pm V_{CC} = 4.5\text{V}$ to 5.5V		600 ± 3 70	$\pm 2.4\text{mV}$ ± 15		*	$\pm 2\text{mV}$ ± 10	μV $\mu\text{V}/^\circ\text{C}$ dB
BIAS CURRENT Input Bias Current	$V_{CM} = 0\text{VDC}$		15	85		*	*	μA
OFFSET CURRENT Input Offset Current	$V_{CM} = 0\text{VDC}$		0.5	5		*	7	μA
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 0.5\text{VDC}$, $V_O = \pm 1.25\text{V}$	± 2.0 60	± 2.5 80		*	*		V dB
OPEN LOOP GAIN, DC Open-Loop Voltage Gain		50	60		*	*		dB
DIGITAL INPUT TTL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH} ECL Logic Levels: V_{IL} V_{IH} I_{IL} I_{IH}	Logic "LO" Logic "HI" Logic "LO", $V_{IH} = 0\text{V}$ Logic "HI", $V_{IL} = +2.7\text{V}$ Logic "LO" Logic "HI" Logic "LO", $V_{IL} = -1.6\text{V}$ Logic "HI", $V_{IH} = -1.0\text{V}$	0 +2.0	-0.08 5	+0.8 +5 -0.4 50 -1.475 -0.88	*	*	*	V V mA μA V V μA μA
RATED OUTPUT Voltage Output Output Current	$R_L = 150\Omega$ $R_L = 50\Omega$	± 2.5 ± 1.5	± 3.75 ± 2.0 44		*	*		V V mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		25	35		*	*	mA

* Same specifications as for AG/AP/AU.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBc = Level referred to carrier-input signal. (3) Harmonic distortion will typically be improved significantly in the inverting mode. (4) Large Signal Response is calculated from the formula $\text{LSBW} = \frac{\text{SR}}{2\pi V_{PEAK}}$. (5) Switching time from application of digital logic signal to input signal selection.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 7\text{VDC}$
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	$\pm V_{CC}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (soldering, 10s)	$+300^{\circ}\text{C}$
Output Short Circuit to Ground ($+25^{\circ}\text{C}$)	Continuous to ground
Junction Temperature	$+175^{\circ}\text{C}$

ORDERING INFORMATION

Basic Model Number	OPA678	() ()
Performance Grade Code		
A:	-40°C to $+85^{\circ}\text{C}$	
S:	-55°C to $+125^{\circ}\text{C}$	
Package Code		
G:	16-pin Ceramic DIP	
P:	16-pin Plastic DIP	
U:	16-pin SOIC	

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA678AG	16-Pin Hermetic DIP	109
OPA678AP	16-Pin Plastic DIP	180
OPA678AU	16-Pin SOIC	211
OPA678SG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

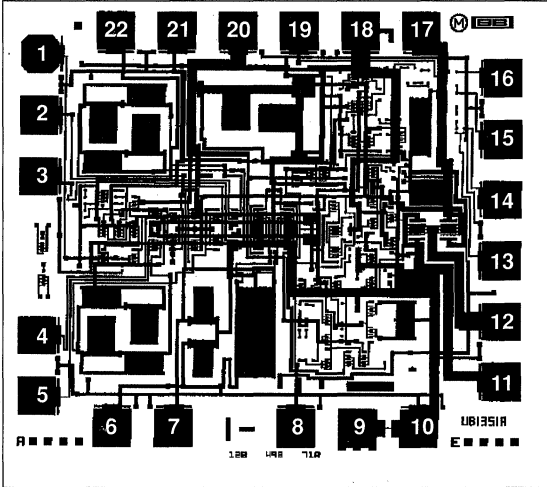
OPA678

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OPERATIONAL AMPLIFIERS

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DICE INFORMATION



OPA678B DIE TOPOGRAPHY

PAD	FUNCTION
1	TTL set
2	-In ₂
3	+In ₂
4	+In ₁
5	-In ₁
6	V _{OS1}
7	V _{OS2}
8	Comp
9 ⁽¹⁾	Fuse
10	V _{CC}
11	V _{CC} O/P
12	Output
13 ⁽¹⁾	FDBK ₃
14 ⁽¹⁾	FDBK ₄
15 ⁽¹⁾	FDBK ₅
16 ⁽¹⁾	FDBK ₁
17	V _{EE} O/P
18	V _{EE}
19 ⁽¹⁾	SRC ₁
20	GND
21	CH, LO
22	CH, HI

NOTE: (1) No connection required.

MECHANICAL INFORMATION

	MILS (0.001")
Die Size	103 x 90±5
Die Thickness	20 ± 3
Min. Pad Size	4 x 4
Backing	Gold
Top Metallization	Gold

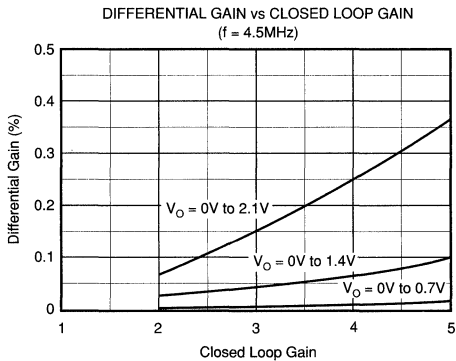
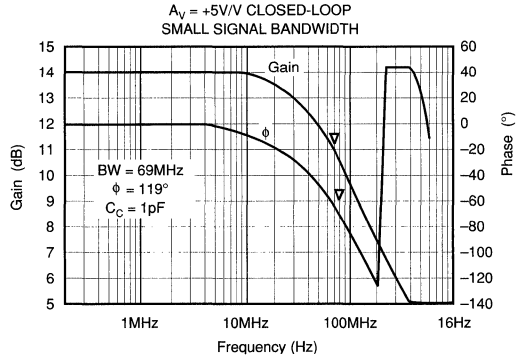
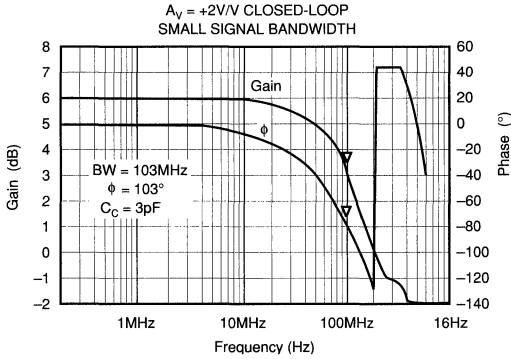
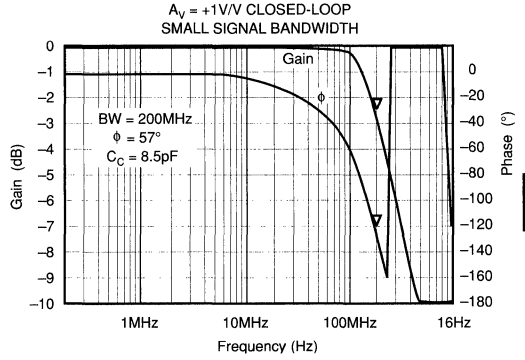
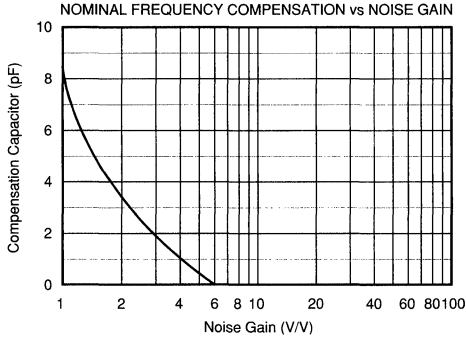
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TYPICAL PERFORMANCE CURVES

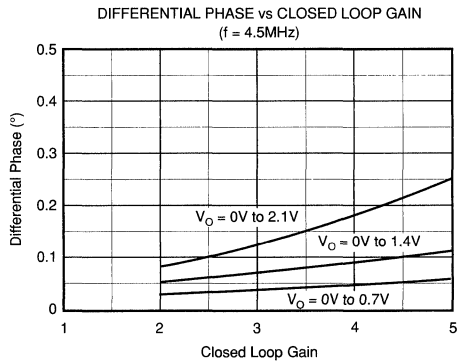
OPA678

OPERATIONAL AMPLIFIERS

2



NOTE: For the gain of $+2V/V$, $C_C = 2.2\text{pF}$; for the gain of $+5V/V$, $C_C = 0$.

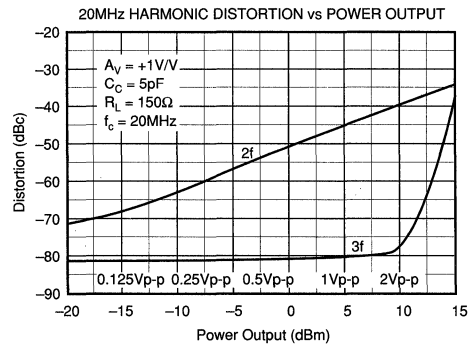
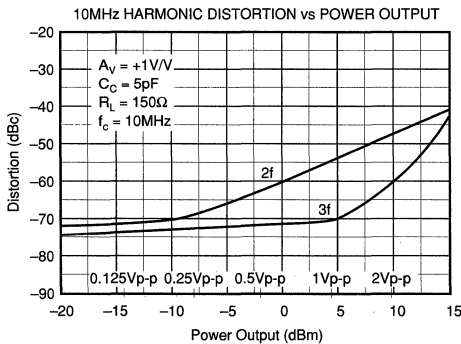
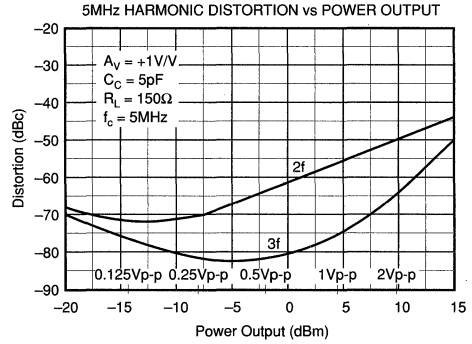
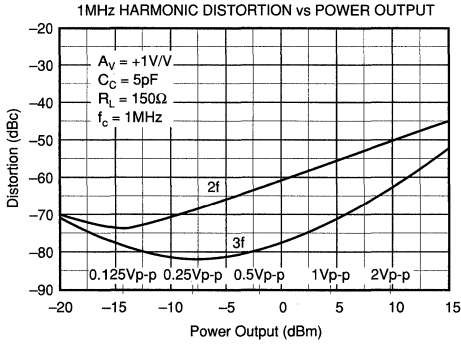
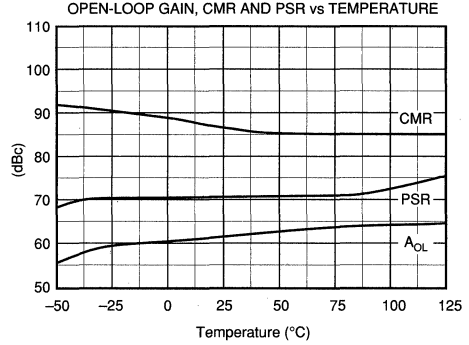
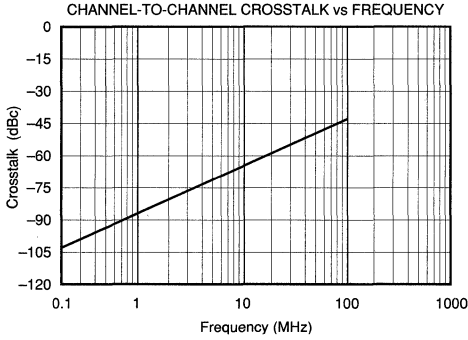


NOTE: For the gain of $+2V/V$, $C_C = 2.2\text{pF}$; for the gain of $+5V/V$, $C_C = 0$.



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TYPICAL PERFORMANCE CURVES (CONT)



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THEORY OF OPERATION

The simplified circuit of the ECL compatible OPA678 is shown in Figure 1. It is a "classical" high-speed op-amp architecture with one important exception—the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and \bar{A} will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier's output stage.

For TTL operation, "A select" is held to an internal reference level by tying pins 13 and 14 together. This allows "A" to become the single-ended TTL input.

Standard TTL and ECL logic levels may be applied to each input selection circuit but only 350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

The OPA678 is designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in the Typical Performance Curve section. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

The laser trimmed input offset voltage is low enough for many video and RF applications. Independent control of input offset will require that trim adjust current be summed into one or both inputs.

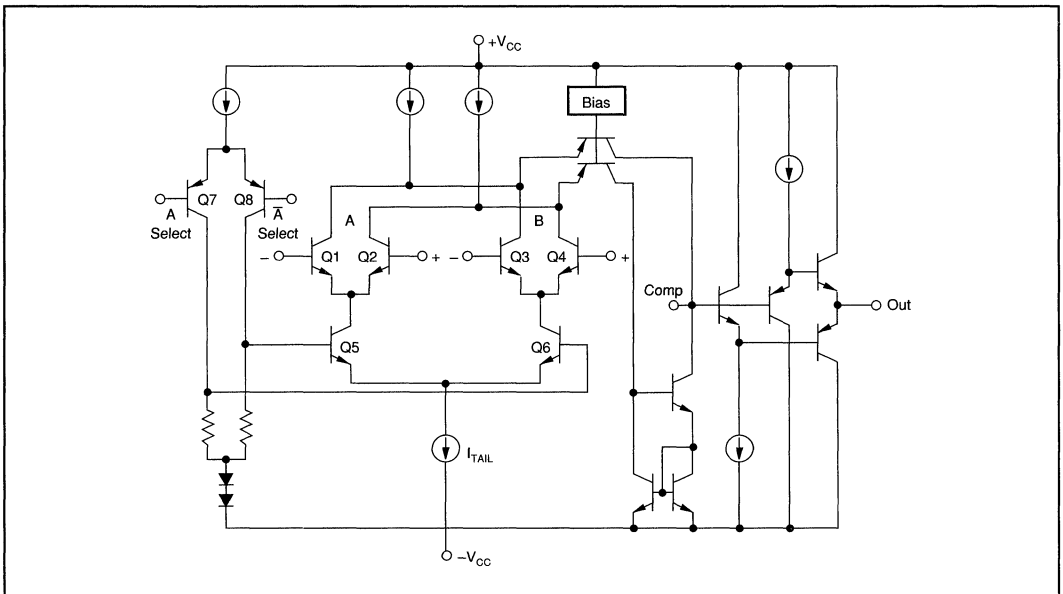


FIGURE 1. OPA678 Simplified Circuit Diagram.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2oz copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA678. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA678 is no different in this respect—any amplifier with a gain bandwidth product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of monoblock or tantalum capacitors with very short leads is highly recommended. A 0.1 μ F in parallel with a 1.0 μ F will be optimum in most applications. The 0.1 μ F should be placed directly at the device's power supply leads.
3. When using the OPA678 in the unity gain voltage follower configuration it is recommended that a 100 Ω resistor be connected from the output to the inverting input for optimum performance.
4. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc. should have lead lengths no longer than 1/4 inch (6cm).
5. Surface mount components (chip resistors, capacitors, etc.) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
6. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1k Ω or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
7. Wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high frequency circuits.
8. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
9. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
10. Don't forget that these amplifiers use $\pm 5V$ supplies. Although they will operate perfectly well with +5V and -5.2V, the use of $\pm 15V$ supplies will result in destruction.
11. Standard commercial test equipment has not been designed to test devices in the OPA678 speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
12. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
13. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
14. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
15. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.

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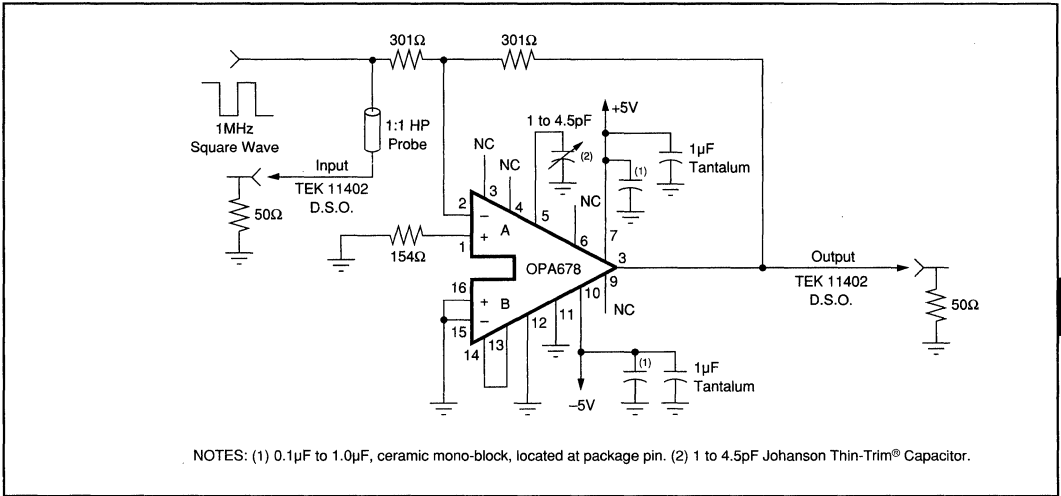


FIGURE 2. OPA678 Settling Time Test Circuit.

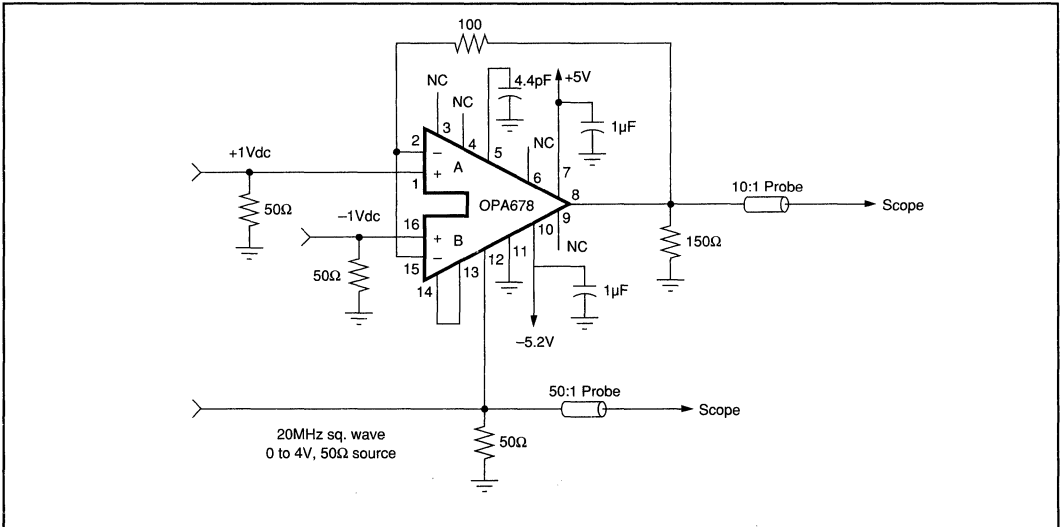


FIGURE 3. OPA678 (TTL) Input Selection Transition Time Test Circuit.

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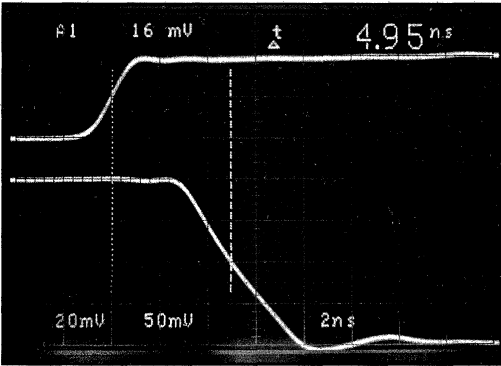


FIGURE 4. OPA678 (TTL) Input Selection Time. Input A to B. Larger output voltages will have slightly slower switching times due to more slewing of the op amp.

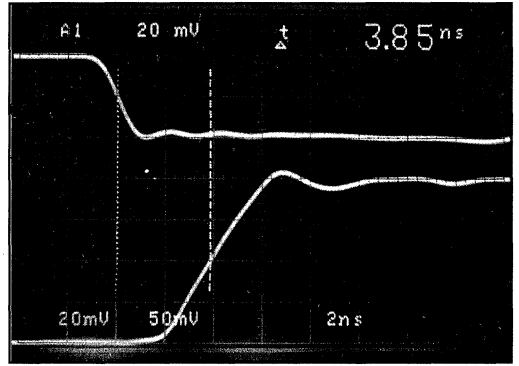


FIGURE 5. OPA678 (ECL) Input Selection Time. Input A to B. Larger output voltages will have slightly slower switching times due to more slewing of the op amp.

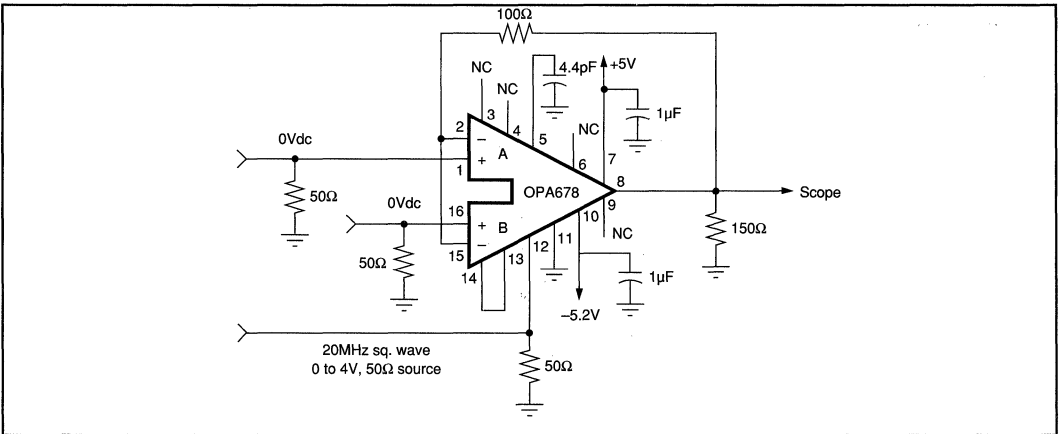


FIGURE 6. Channel Select Switching Transient Test Schematic.

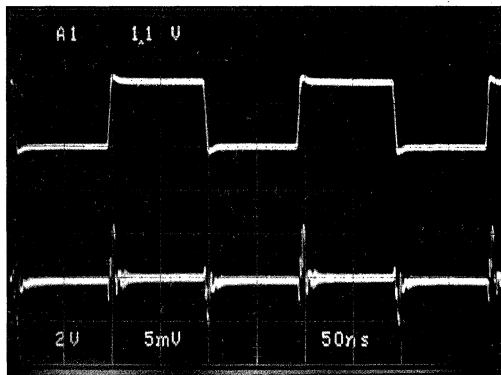


FIGURE 7. OPA678 Switching Transient. The switching transient levels will be lower for switching signals with slower rising edges.

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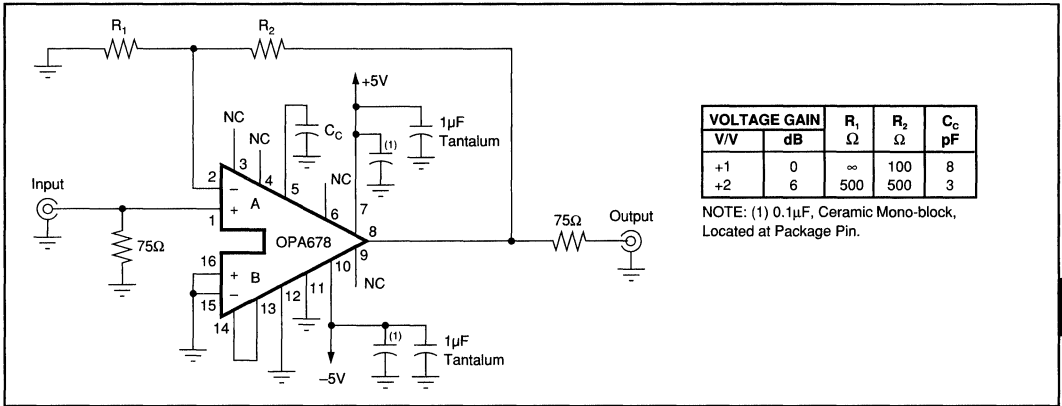


FIGURE 8. OPA678 used as Conventional Op Amp. A wideband video amplifier with 75 Ω input and output impedance.

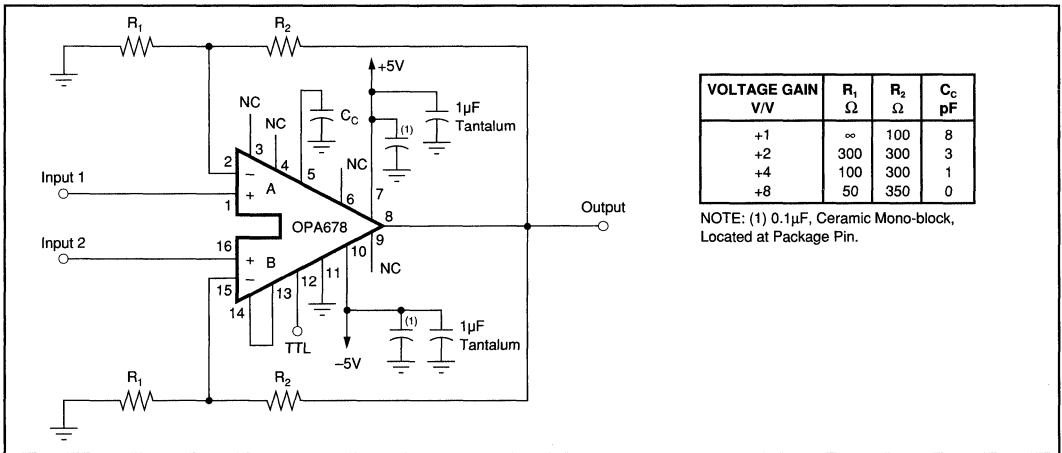


FIGURE 9. Two Input Multiplexer with Gain. This circuit can be used to multiplex I & Q signals into one sampling ADC.

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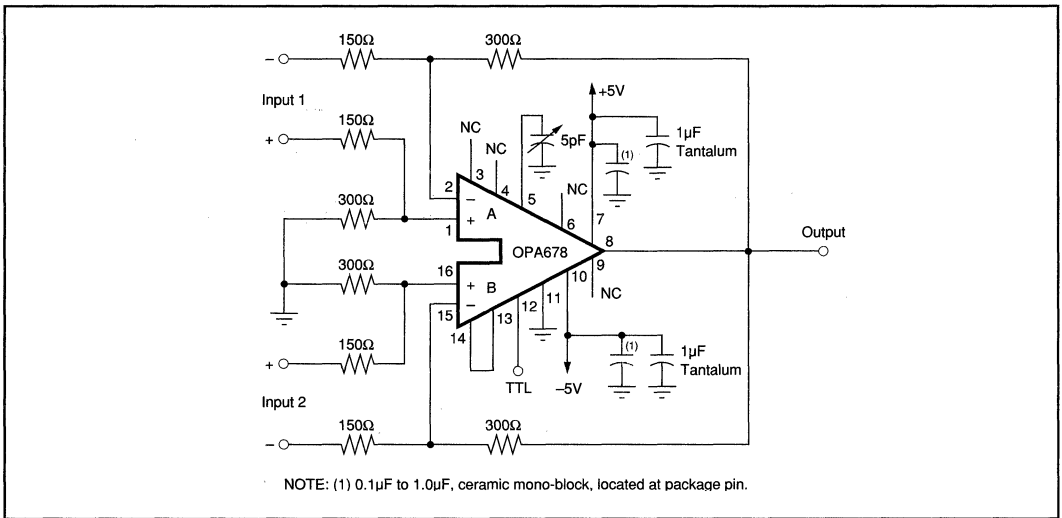


FIGURE 10. Differential Input Multiplexer with Gain of +2V/V.

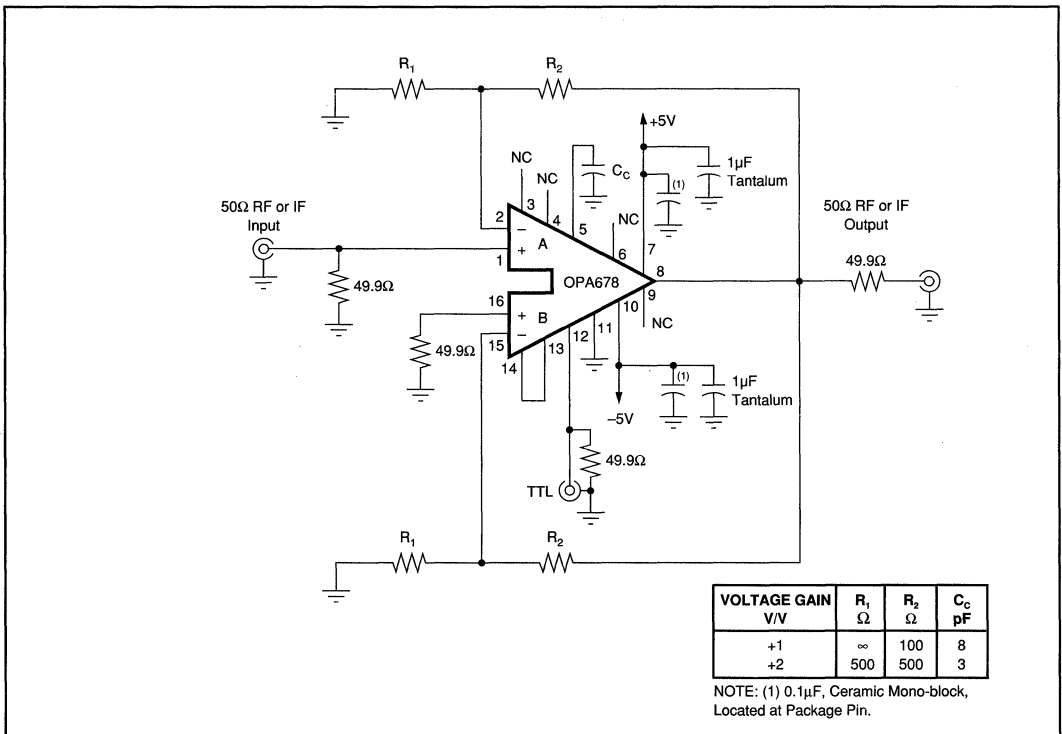


FIGURE 11. Receiver Noise Blanker: A Wideband Gated Video Amplifier.

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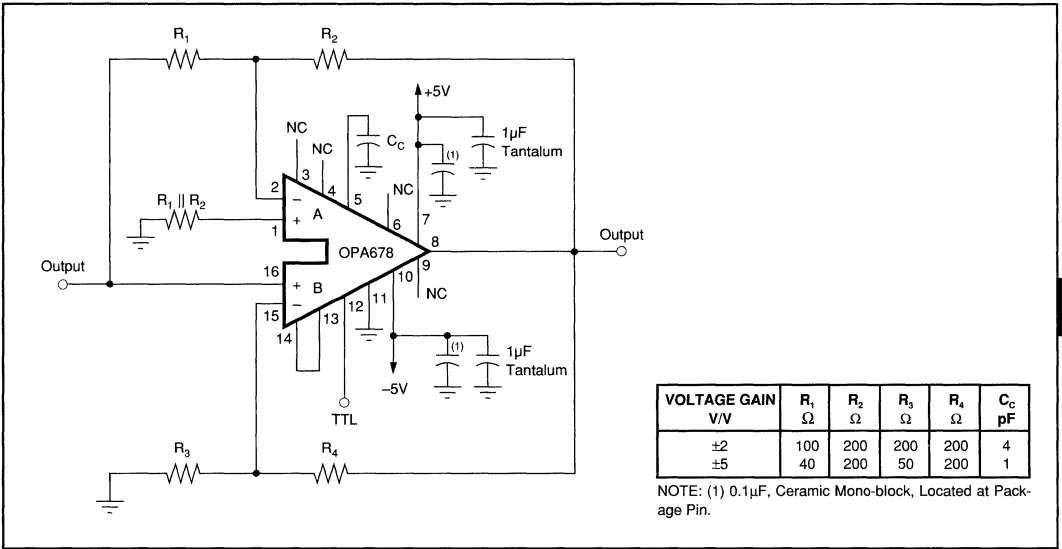


FIGURE 12. Synchronous Modulator/Demodulator (with Gain).

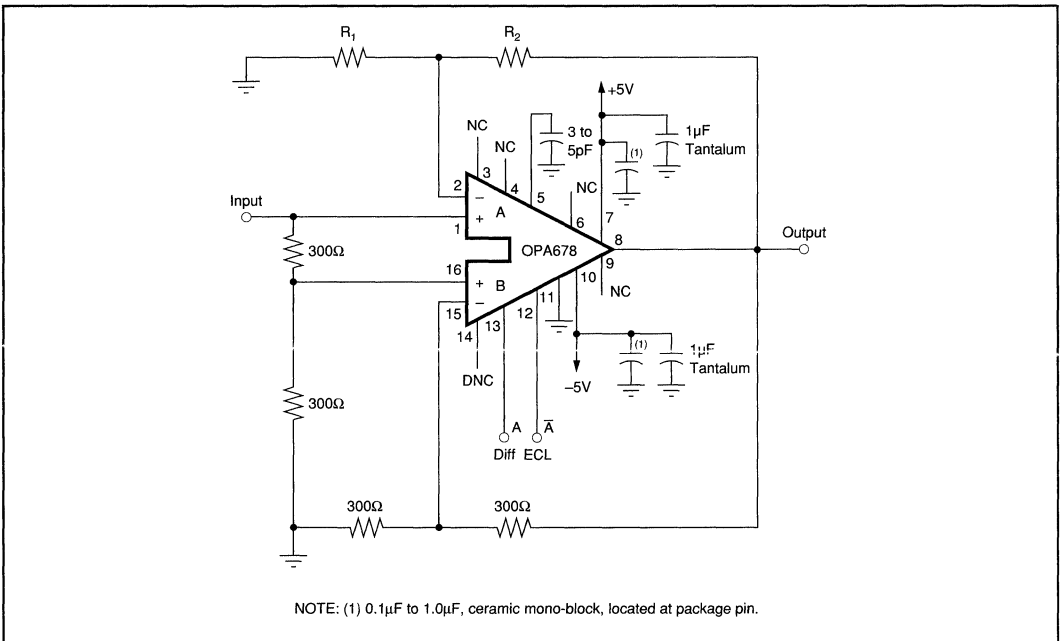


FIGURE 13. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +2V/V (0dB and 6dB).

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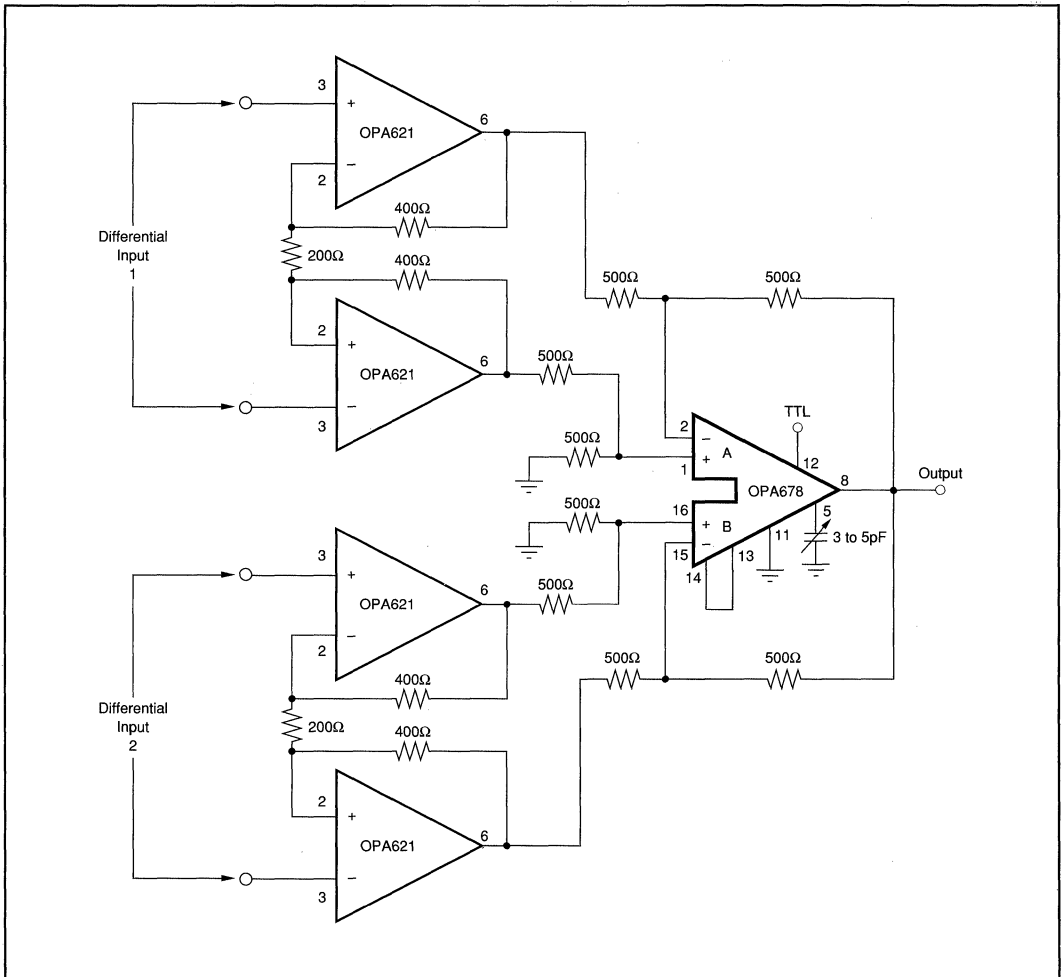
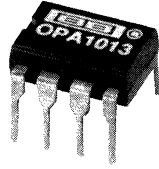


FIGURE 14. High Input Impedance Differential Input Multiplexer with Gain of 5V/V (14dB).

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OPA1013

OPA1013

2

OPERATIONAL AMPLIFIERS

Precision, Single-Supply DUAL OPERATIONAL AMPLIFIER

FEATURES

- SINGLE POWER SUPPLY OPERATION
- INPUT VOLTAGE RANGE TO GROUND
- OUTPUT SWINGS NEAR GROUND
- LOW QUIESCENT CURRENT: 550 μ A max
- LOW V_{OS} : 300 μ V max
- LOW DRIFT: 2.5 μ V/ $^{\circ}$ C max
- LOW I_{OS} : 1.5nA max
- LOW NOISE: 0.55 μ Vp-p, 0.1Hz to 10Hz

APPLICATIONS

- PRECISION INSTRUMENTATION
- BATTERY-POWERED EQUIPMENT
- BRIDGE AMPLIFIERS
- 4-20mA CURRENT TRANSMITTERS
- VOLTAGE COMPARATOR

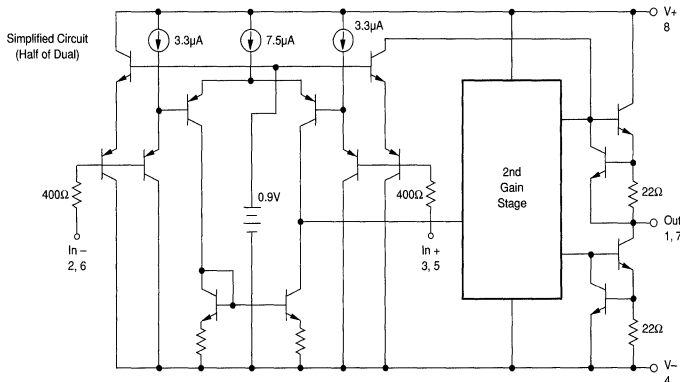
DESCRIPTION

The OPA1013 dual operational amplifier provides precision performance in single power supply and low power applications. It is laser trimmed for low offset voltage and drift, greatly reducing the large errors common with LM324-type op amps. Input offset current is also trimmed to reduce errors in high impedance applications.

The OPA1013 is characterized for operation at both +5V (single supply) and \pm 15V power supplies. When

operated from a single supply, the input common-mode range includes ground and the output can swing to within 15mV of ground. Completely independent biasing networks eliminate interaction between the two amplifiers—even when one is used as a comparator.

The OPA1013 is available in an 8-pin plastic DIP specified for the 0 $^{\circ}$ C to +70 $^{\circ}$ C temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITION	OPA1013CN8			OPA1013DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±50	±300		±200	±800	μV
Time Stability			0.5			*	*	μV/Mo
Input Offset Current			±0.08	±1.5		*	*	nA
Input Bias Current			7	30		*	*	nA
Voltage Noise, BW = 0.1 to 10Hz			0.55			*	*	μVp-p
Noise Density, f = 10Hz			28			*	*	nV/√Hz
f = 1kHz			25			*	*	nV/√Hz
Current Noise Density, f = 10Hz			0.12			*	*	pA/√Hz
Input Resistance: Differential		70	300		*	*		MΩ
Input Resistance: Common-Mode			4		*	*		GΩ
Open-Loop Voltage Gain	$V_O = \pm 10V$, $R_L = 2k\Omega$	1.2	2.9		*	*		V/μV
	$V_O = \pm 10V$, $R_L = 600\Omega$	0.5	1.9		*	*		V/μV
Common-Mode Input Range		+13.5	+13.8		*	*		V
			-15		*	*		V
Common-Mode Rejection	$V_{CM} = +13.5$ to $-15V$	97	114		*	*		dB
Power Supply Rejection	$V_S = \pm 2$ to $\pm 18V$	100	117		*	*		dB
Channel Separation	$V_O = \pm 10V$, $R_L = 2k\Omega$	120	137		*	*		dB
Voltage Output	$R_L = 2k\Omega$	±12.5	±14		*	*		V
Slew Rate		0.2	0.35		*	*		V/μs
Quiescent Current (per amplifier)			±0.35	±0.55		*	*	mA

*Specification same as OPA1013CN8.

$V_S = +5V/0V$, $V_{CM} = 0V$, $V_O = +1.4V$, $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITION	OPA1013CN8			OPA1013DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			±90	±450		±250	±950	μV
Input Offset Current			±3.0	±2.0		*	*	nA
Input Bias Current			10	50		*	*	nA
Open-Loop Voltage Gain	$V_O = 5mV$ to $4V$ $R_L = 500\Omega$		0.1			*	*	V/μV
Common-Mode Input Range		+3.5	+3.8		*	*		V
		0	-0.3		*	*		V
Voltage Output Low	No Load		15	25		*	*	mV
Low	$R_L = 600\Omega$ to Ground		5	10		*	*	mV
Low	$I_{SINK} = 1mA$		200	350		*	*	mV
High	No Load		4.4		*	*		V
High	$R_L = 600\Omega$ to Ground	3.4	4		*	*		V
Quiescent Current (per amplifier)			0.33	0.5		*	*	mA

*Specification same as OPA1013CN8.

$T_A = 0^\circ C$ to $+70^\circ C$, $V_S = \pm 15V$, $V_{CM} = 0V$ unless otherwise noted.

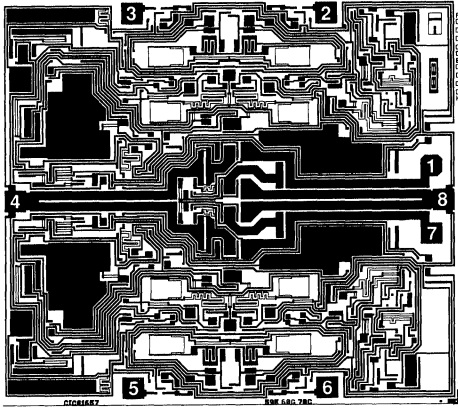
PARAMETER	CONDITION	OPA1013CN8			OPA1013DN8			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_S = +5/0V$, $V_O = +1.4V$		±80	±400		±230	±1000	μV
			±110	±570		±280	±1200	μV
Input Offset Voltage Drift ⁽¹⁾			0.4	2.5		0.7	5	μV/°C
Input Offset Current			±0.3	±2.8		*	*	nA
	$V_S = +5/0V$, $V_O = +1.4V$		±0.5	±6		*	*	nA
Input Bias Current			9	38		*	*	nA
	$V_S = +5/0V$, $V_O = +1.4V$		13	90		*	*	nA
Open-Loop Voltage Gain	$V_O = \pm 10V$, $R_L = 2k\Omega$	0.7	2.2		*	*		V/μV
Common-Mode Rejection	$V_{CM} = +13$ to $-15V$	94	113		*	*		dB
Power Supply Rejection	$V_S = \pm 2$ to $\pm 18V$	97	116		*	*		dB
Voltage Output	$R_L = 2k\Omega$	±12.0	±13.9		*	*		V
V_O Low	$V_S = +5/0V$, $R_L = 600\Omega$		6	13		*	*	mV
V_O High	$V_S = +5/0V$, $R_L = 600\Omega$	3.2	3.9		*	*		V
Quiescent Current (per amplifier)			±0.37	±0.6		*	*	mA
	$V_S = +5/0V$, $V_O = +1.4V$		0.34	0.55		*	*	mA

*Specification same as OPA1013CN8.

NOTE: (1) Guaranteed by design. This specification is established to a 98% confidence level.

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DICE INFORMATION



OPA1013 DIE TOPOGRAPHY

PAD	FUNCTION
1	Output A
2	-In A
3	+In A
4	V-
5	+In B
6	-In B
7	Output B
8	V+

Substrate Bias: $-V_s$

MECHANICAL INFORMATION

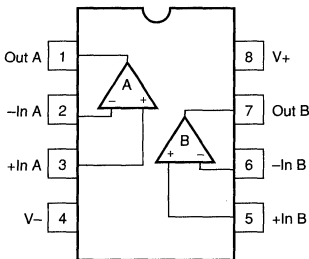
	MILS (0.001")	MILLIMETERS
Die Size	112 x 100 ±5	2.84 x 2.54 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	92	
Backing	Gold	

OPA1013

OPERATIONAL AMPLIFIERS

CONNECTION DIAGRAM

N8 — Plastic Package — Top View



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	V+ to (V-) -5V
Output Short Circuit (T _a = 25°C)	Continuous
Operating Temperature	0°C to +70°C
Storage Temperature	-65 to +150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA1013CN8	Plastic DIP	0°C to +70°C
OPA1013DN8	Plastic DIP	0°C to +70°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA1013CN8	Plastic DIP	006
OPA1013DN8	Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

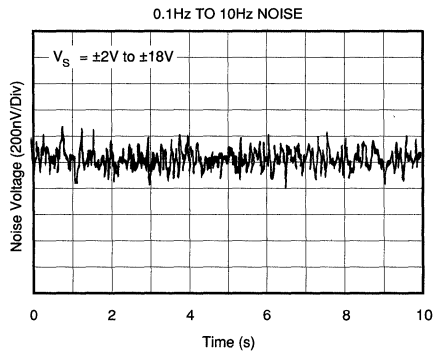
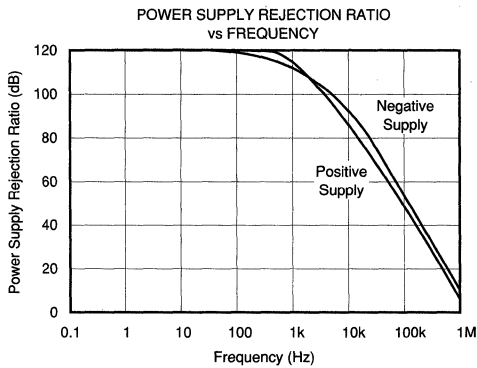
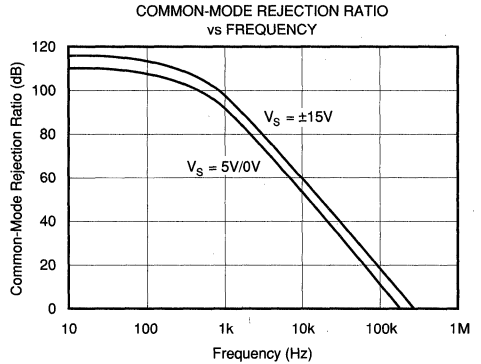
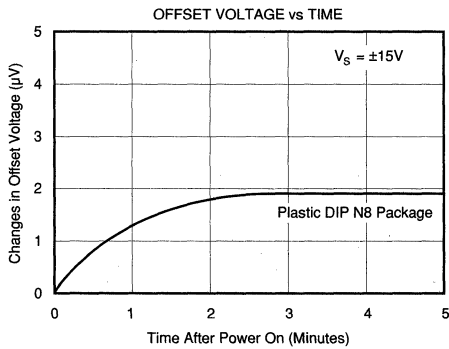
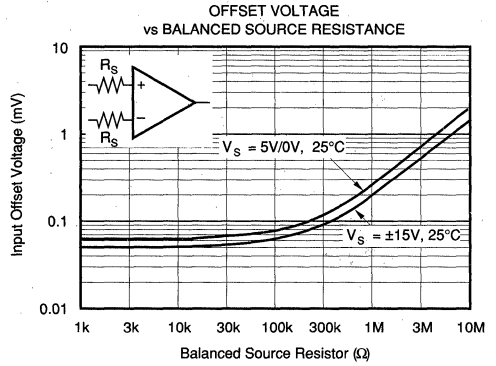
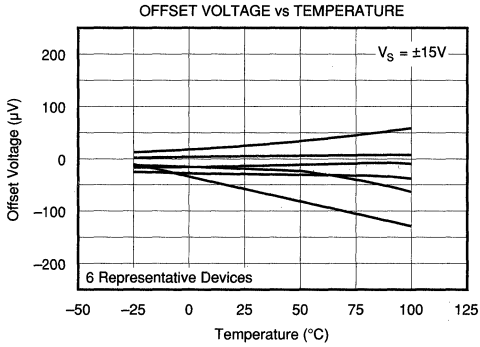
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TYPICAL PERFORMANCE CURVES

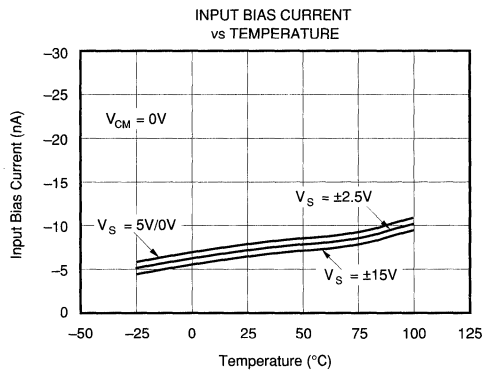
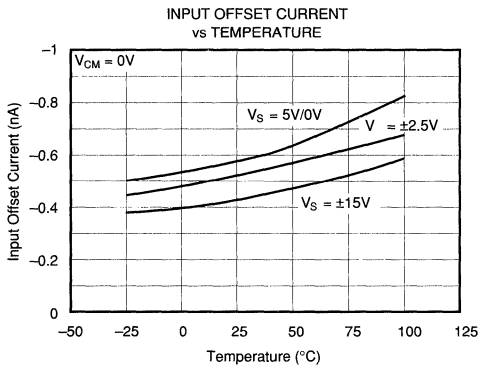
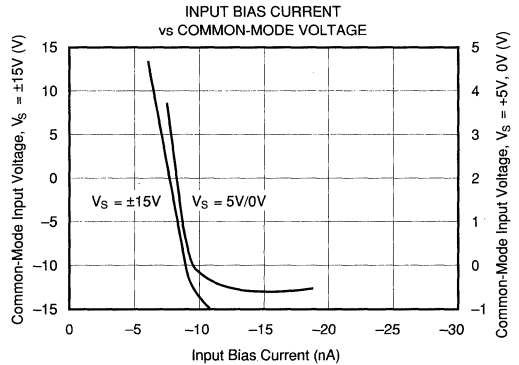
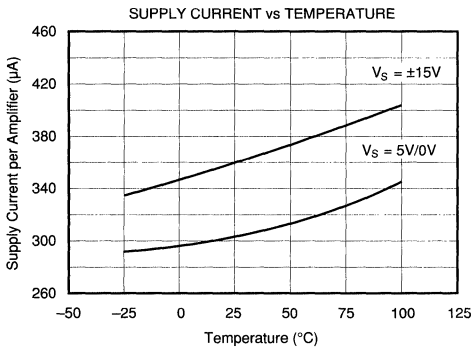
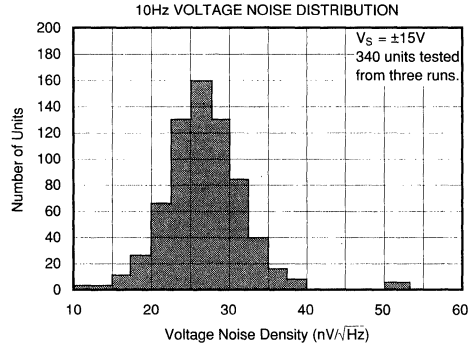
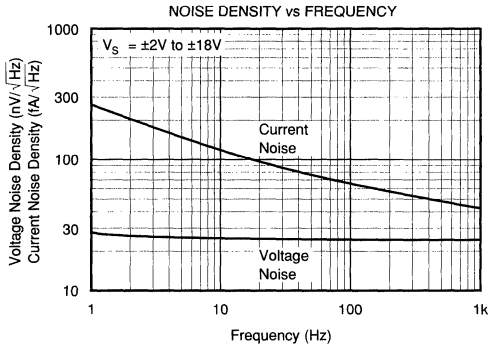
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

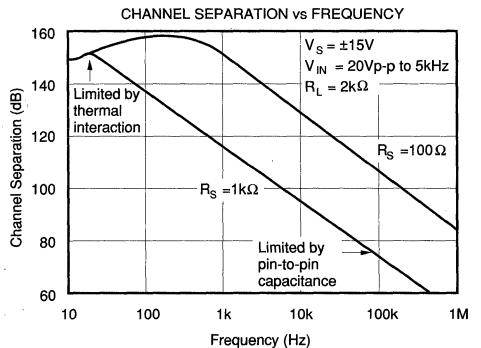
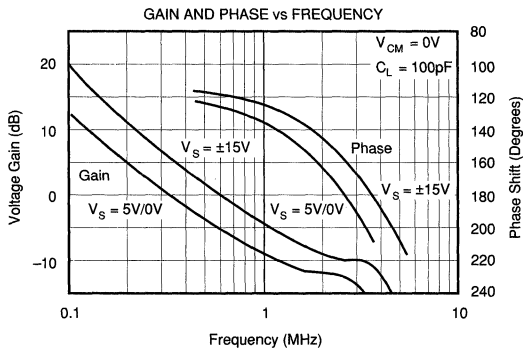
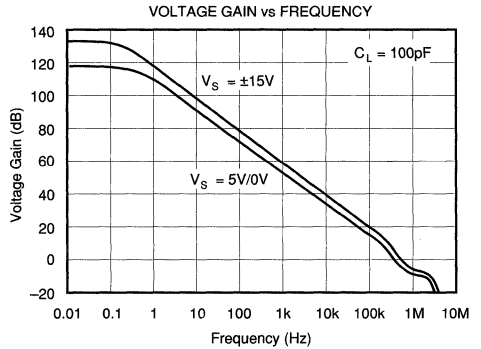
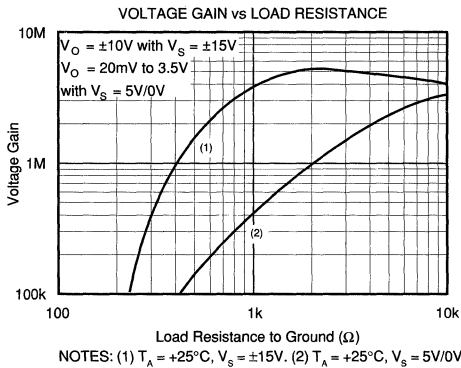
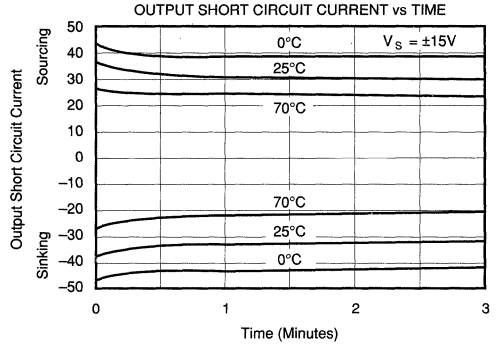
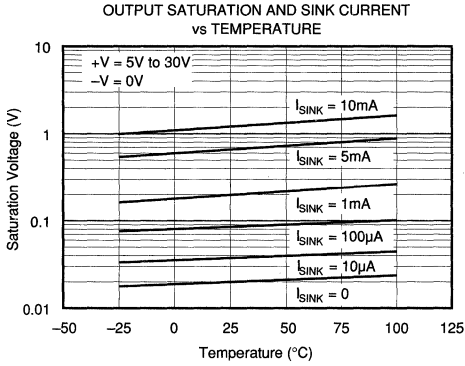
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TYPICAL PERFORMANCE CURVES (CONT)

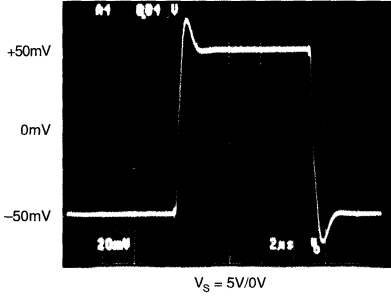
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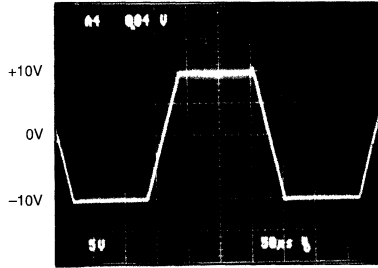
Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

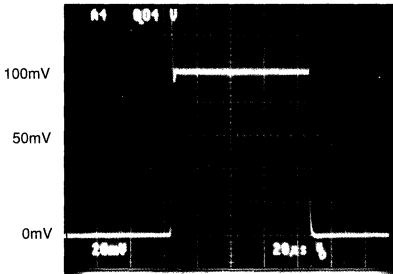
SMALL SIGNAL TRANSIENT RESPONSE
 $V_S = \pm 15V, G = +1$



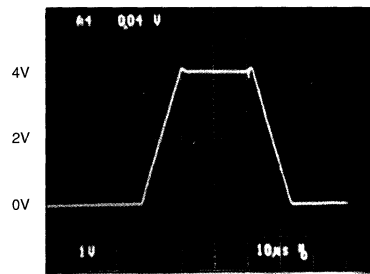
LARGE SIGNAL TRANSIENT RESPONSE
 $V_S = \pm 15V, G = +1$



SMALL SIGNAL TRANSIENT RESPONSE
 $V_S = 5V/0V, G = +1, R_L = 600\Omega$ to Ground

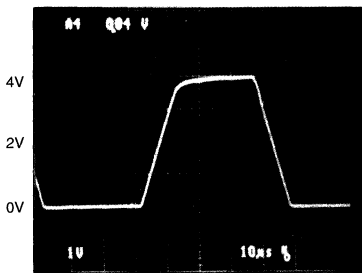


LARGE SIGNAL TRANSIENT RESPONSE
 $V_S = 5V/0V, G = +1, R_L = 4.7k\Omega$ to 5V



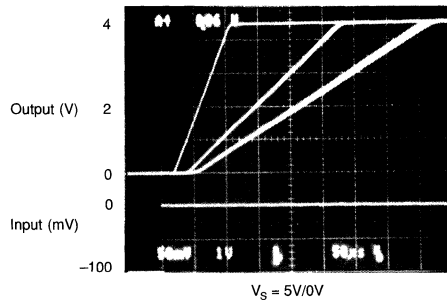
Input = 0V to 4V Pulse

LARGE SIGNAL TRANSIENT RESPONSE
 $V_S = 5V/0V, G = +1, \text{No Load}$

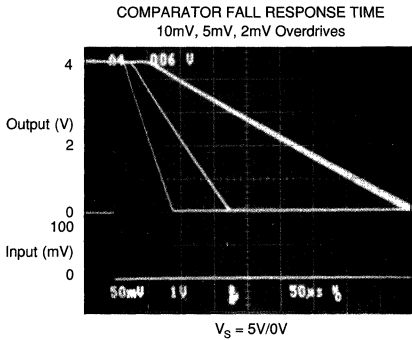


Input = 0V to 4V Pulse

COMPARATOR RISE RESPONSE TIME
 10mV, 5mV, 2mV Overdrives



TYPICAL PERFORMANCE CURVES (CONT)



APPLICATIONS INFORMATION

The OPA1013 is unity-gain stable, making it easy to use and free from oscillations in the widest range of circuitry. Follow good design practice by bypassing the power supplies close to the op amp pins. In most cases 0.1 μ F ceramic capacitors are adequate.

SINGLE POWER SUPPLY OPERATION

The OPA1013 is specified for operation from a single power supply. This means that linear operation continues with the input terminals at (or even somewhat below) ground potential. When used in a non-inverting amplifier, 0V input must produce 0V output. In practice, the output swing is limited to approximately 15mV above ground with no load. Output swing near ground can be optimized when the output load is connected to ground. If the output must sink current, the ability to swing near ground will be diminished. The output swings to within approximately 200mV of ground when sinking 1mA.

INPUT PROTECTION

The circuitry of the OPA1013 is protected against overload for input voltages ranging from the positive supply voltage to 5V below the negative supply voltage (below ground in single supply operation). No external protection circuitry is required, as it is with other common single-supply op amps.

Furthermore, the OPA1013 is free from phase-reversal problems common with other single-supply op amps. When the inputs are driven below ground (or below the negative power supply), the output polarity remains correct.

COMPARATOR OPERATION

The OPA1013 functions well as a comparator, where high speed is not required. Sometimes, in fact, the low offset and docile characteristics of the OPA1013 may simplify the design of comparator circuitry. The two op amps in the OPA1013 use completely independent bias circuitry to avoid interaction when the inputs are over-driven. Driving one op amp into saturation will not affect the characteristics of the other amplifier. The outputs of the OPA1013 can drive one TTL load. Quiescent current remains stable when the inputs are overdriven.

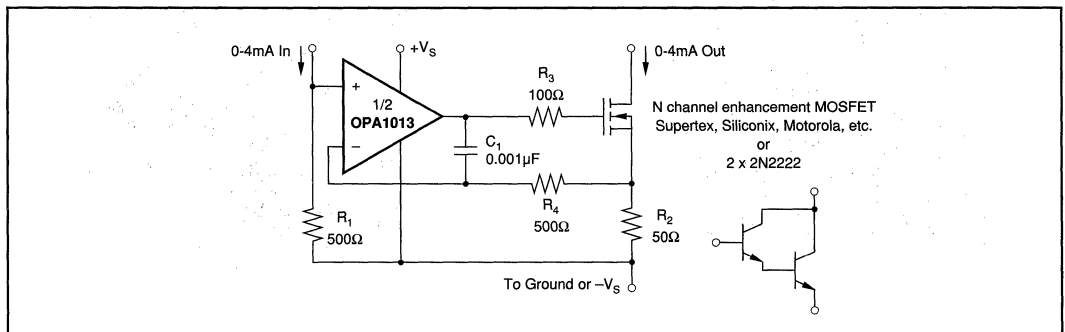


FIGURE 1. Precision Current Mirror.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

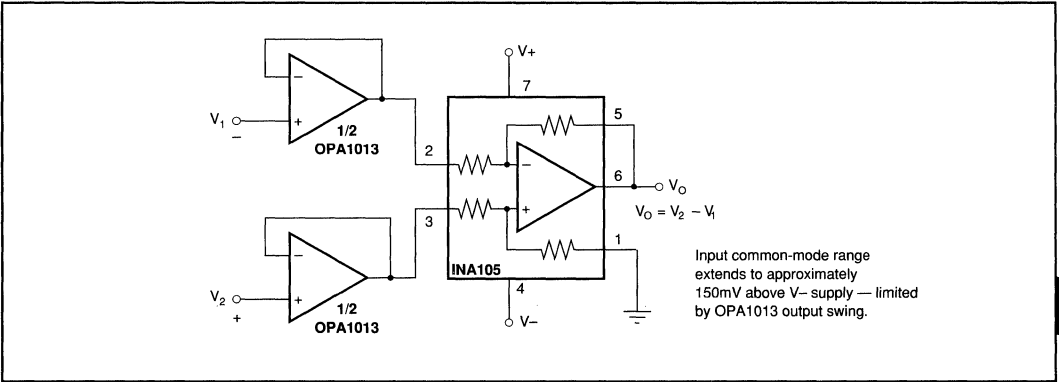


FIGURE 2. Instrumentation Amplifier.

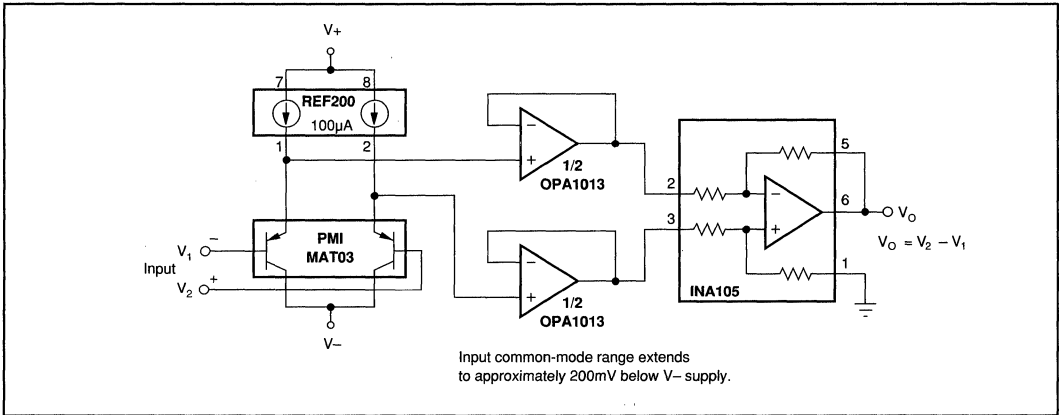


FIGURE 3. Instrumentation Amplifier.

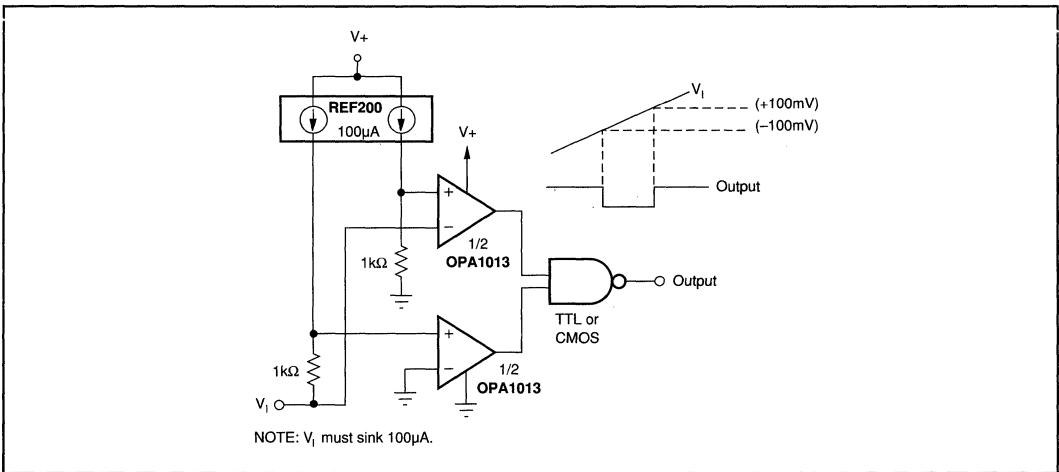
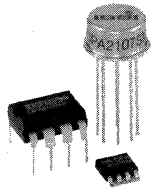


FIGURE 4. Window Comparator.

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OPA2107

Precision Dual *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: $8\text{nV}/\sqrt{\text{Hz}}$ at 10kHz
- LOW V_{os} : 500 μV max
- LOW DRIFT: 5 $\mu\text{V}/^\circ\text{C}$ max
- LOW I_{b} : 5pA max
- FAST SETTLING TIME: 2 μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

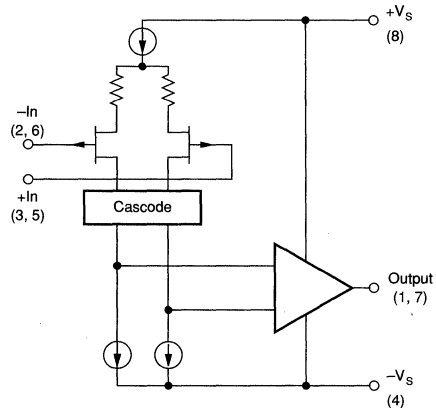
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision *Difet* performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET[®] type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (*Difet*) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



Difet[®] Burr-Brown Corp.
BIFET[®] National Semiconductor

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 899-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITION	OPA2107AM, SM, AP, AU			OPA2107BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Over Specified Temperature SM Grade Average Drift Over Specified Temperature Power Supply Rejection	$V_{CM} = 0\text{V}$ $V_S = \pm 10 \text{ to } \pm 18\text{V}$		100 0.5 0.8 3	1mV 2 2.5 10		50 0.2 2 100	500 1 5	μV mV mV $\mu\text{V}/^\circ\text{C}$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Over Specified Temperature SM Grade Input Offset Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		4 0.25 4 1 1	10 1.5 35 8 1 28		2 0.15 0.5	5 1 3 0.5	pA nA nA pA nA nA
INPUT NOISE Voltage: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ BW = 0.1 to 10Hz BW = 10 to 10kHz Current: $f = 0.1\text{Hz}$ thru 20kHz BW = 0.1Hz to 10Hz	$R_S = 0$		30 12 9 8 1.2 0.85 1.2 23			* * * * * * 0.9 17		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ μVrms $\text{fA}/\sqrt{\text{Hz}}$ fAp-p
INPUT IMPEDANCE Differential Common-Mode			$10^{13} \parallel 2$ $10^{14} \parallel 4$			* *		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE Common-Mode Input Range Over Specified Temperature SM Grade Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	± 10.5 ± 10.2 ± 10 80	± 11 ± 10.5 ± 10.3 94		* * *	* * *		V V V dB
OPEN-LOOP GAIN Open-Loop Voltage Gain Over Specified Temperature SM Grade	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	82 80 80	96 94 92		84 82	100 96		dB dB dB
DYNAMIC RESPONSE Slew Rate Settling Time: 0.1% 0.01% Gain-Bandwidth Product THD + Noise Channel Separation	$G = +1$ $G = -1$, 10V Step $G = 100$ $G = +1$, $f = 1\text{kHz}$ $f = 100\text{Hz}$, $R_L = 2\text{k}\Omega$	13	18 1.5 2 4.5 0.001 120		* * * * * *	* * * * * *		V/ μs μs μs MHz % dB
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current		± 4.5	± 15 ± 4.5	± 18 ± 5	* *	* *	* *	V V mA
OUTPUT Voltage Output Over Specified Temperature SM Grade Short Circuit Current Output Resistance, Open-Loop Capacitive Load Stability	$R_L = 2\text{k}\Omega$ 1MHz $G = +1$	± 11 ± 10.5 ± 10.2 ± 10	± 12 ± 11.5 ± 11.3 ± 40 70 1000		* * * * * *	* * * * * *		V V V mA Ω pF
TEMPERATURE RANGE Specification AP, AU, AM, BM SM Operating AP, AU AM, BM, SM Storage AP, AU AM, BM, SM Thermal Resistance (θ_{JA}) AP AU AM, BM, SM		-25 -55 -25 -55 -40 -65		+85 +125 +85 +125 +125 +150	* * * * * *	* * * * * *		$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±V _S ±2V
Differential Input Voltage	Total V _S ±4V
Operating Temperature	
M Package	-55°C to +125°C
P and U Packages	-25°C to + 85°C
Storage Temperature	
M Package	-65°C to +150°C
P and U Packages	-40°C to +125°C
Output Short Circuit to Ground (T _A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

PACKAGE INFORMATION⁽¹⁾

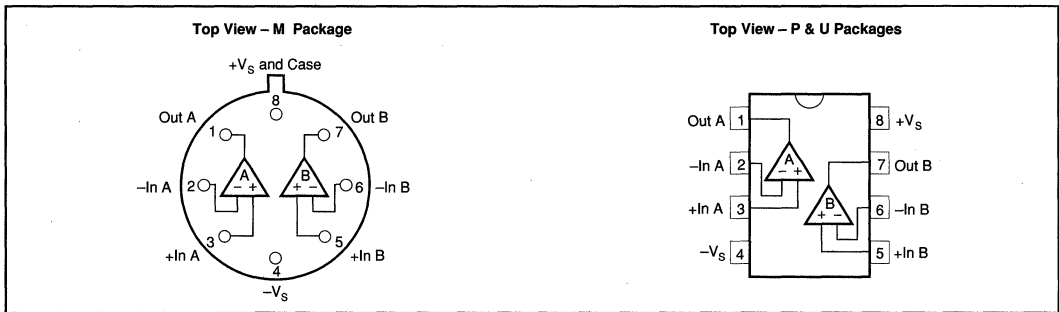
MODELS	PACKAGE	PACKAGE DRAWING NUMBER
OPA2107AP	Plastic DIP	006
OPA2107AM	Metal TO-99	001
OPA2107BM	Metal TO-99	001
OPA2107SM	Metal TO-99	001
OPA2107AU	SO-8 SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	-25 to +85°C
OPA2107AM	Metal TO-99	-25 to +85°C
OPA2107BM	Metal TO-99	-25 to +85°C
OPA2107SM	Metal TO-99	-55 to +125°C
OPA2107AU	SO-8 SOIC	-25 to +85°C

PIN CONFIGURATIONS



DICE INFORMATION

OPA2107 DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	-In A
3	+In A
4	-V _S
5	+In B
6	-In B
7	Out B
8	+V _S

Substrate Bias: -V_S

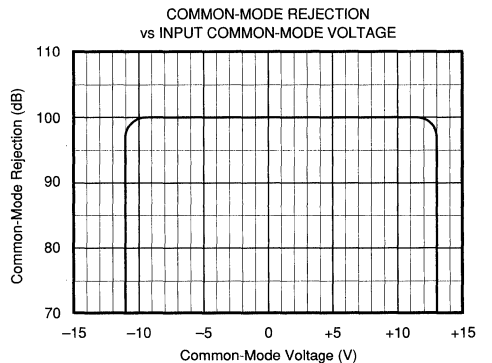
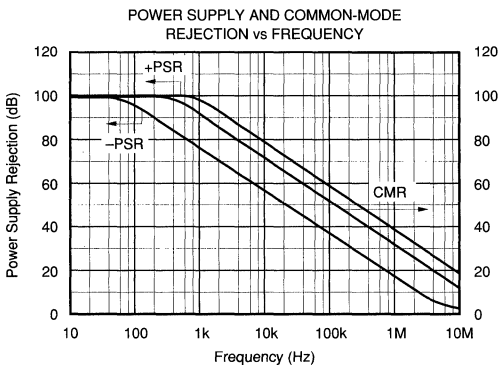
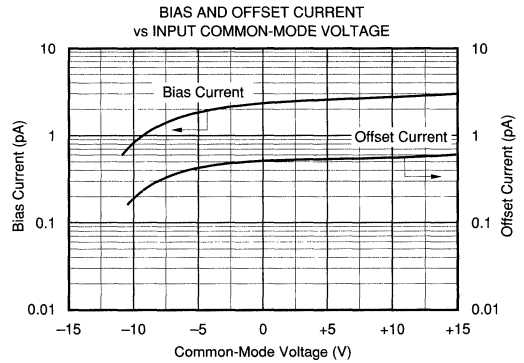
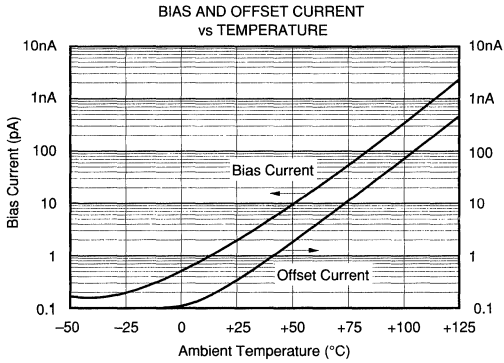
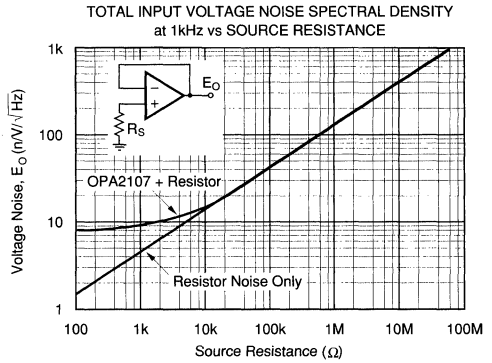
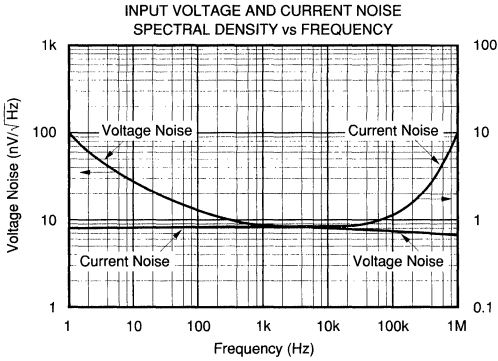
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	97 x 77 ±3	2.46 x 1.96 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	53	
Backing	None	

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



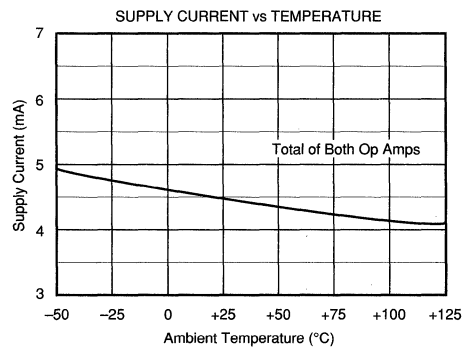
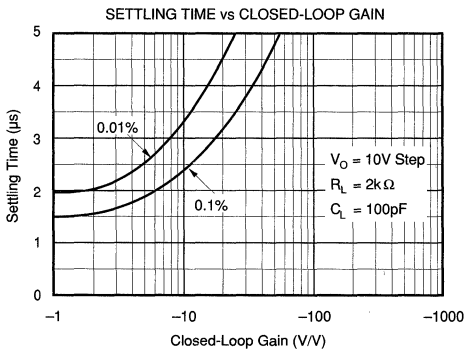
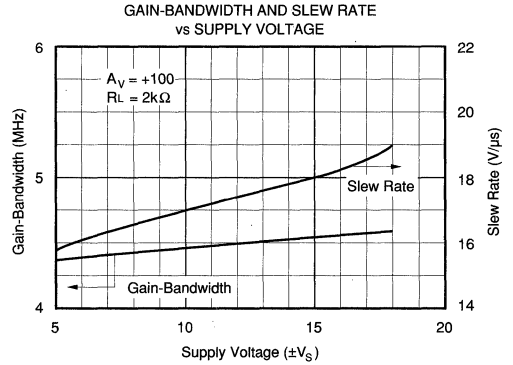
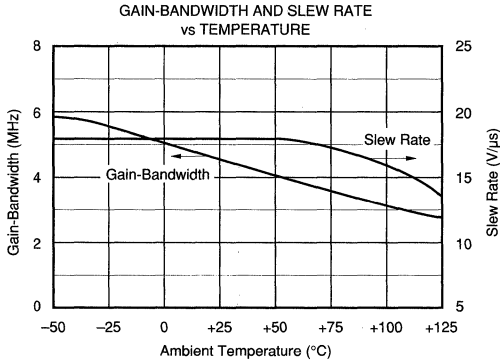
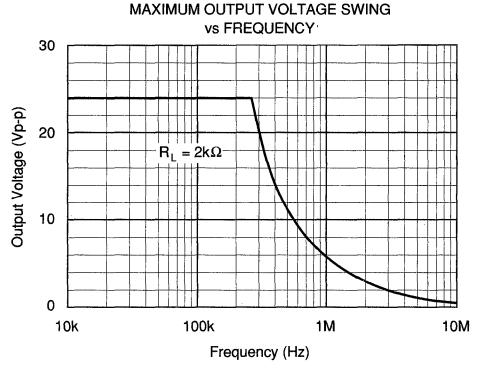
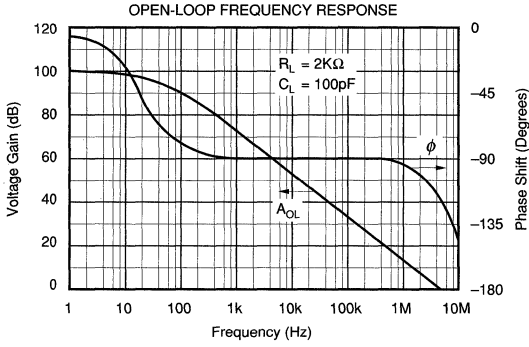
OPA2107

2 OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

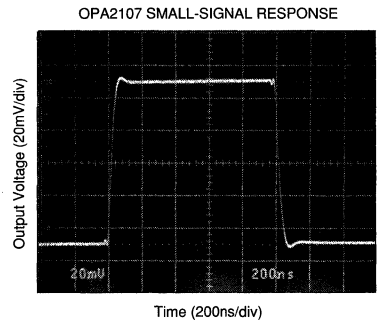
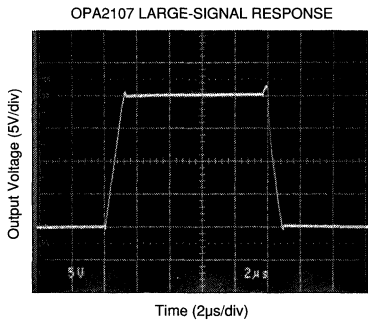
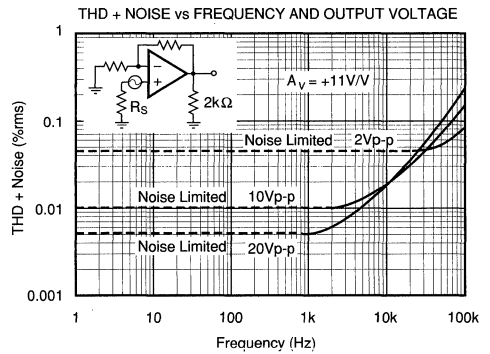
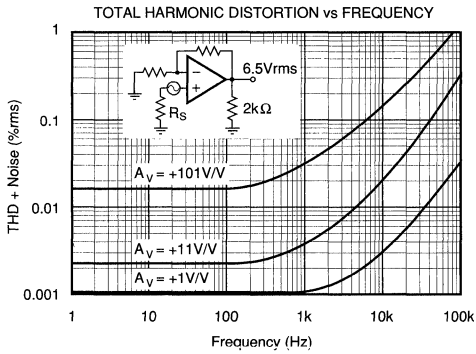
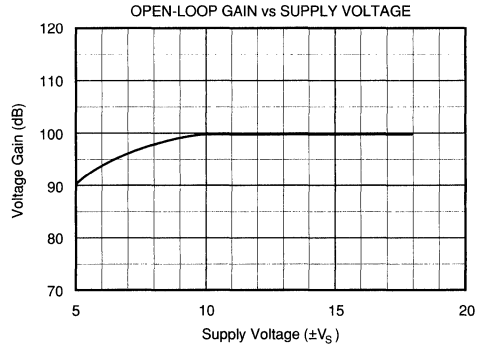
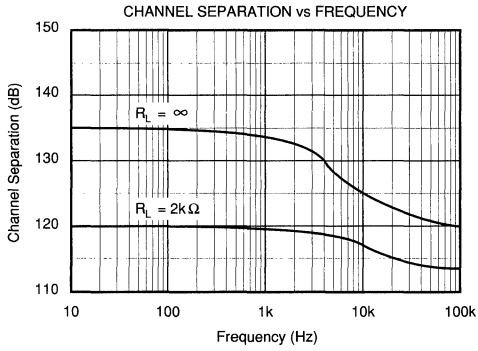
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_a = +25^\circ\text{C}$, $V_s = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1 μ F ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1 μ F tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's *Difet* input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

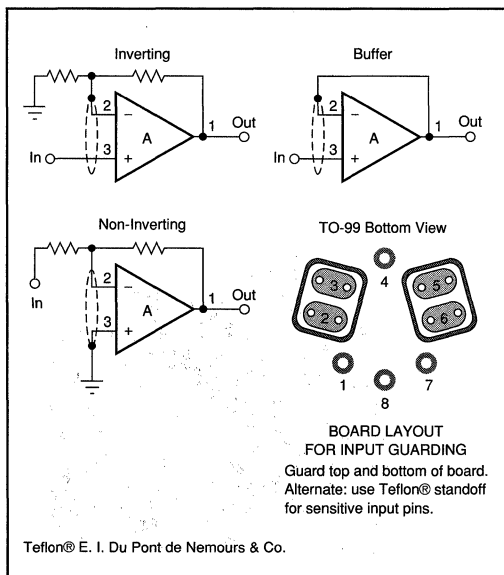


FIGURE 1. Connection of Input Guard.

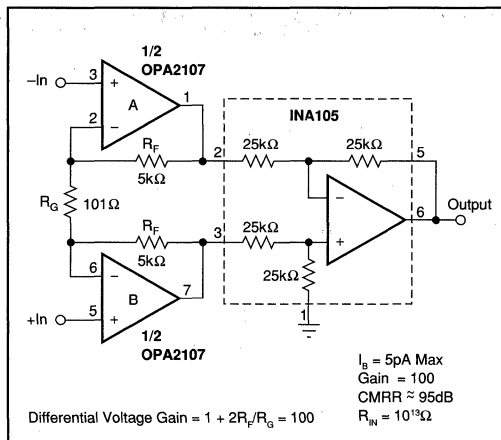


FIGURE 2. FET Input Instrumentation Amplifier.

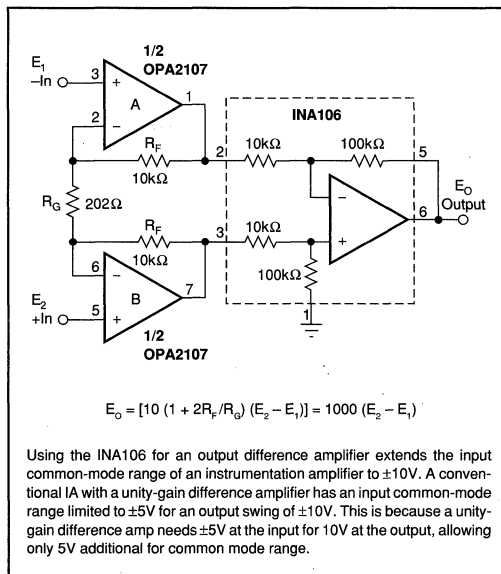
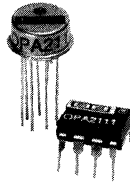


FIGURE 3. Precision Instrumentation Amplifier.

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OPA2111

OPA2111

2

OPERATIONAL AMPLIFIERS

Dual Low Noise Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- **LOW NOISE:** 100% Tested, $8\text{nV}/\sqrt{\text{Hz}}$ max at 10kHz
- **LOW BIAS CURRENT:** 4pA max
- **LOW OFFSET:** 500 μV max
- **LOW DRIFT:** 2.8 $\mu\text{V}/^\circ\text{C}$
- **HIGH OPEN-LOOP GAIN:** 114dB min
- **HIGH COMMON-MODE REJECTION:** 96dB min

APPLICATIONS

- **PRECISION INSTRUMENTATION**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **PROFESSIONAL AUDIO EQUIPMENT**
- **MEDICAL EQUIPMENT**
- **DETECTOR ARRAYS**

DESCRIPTION

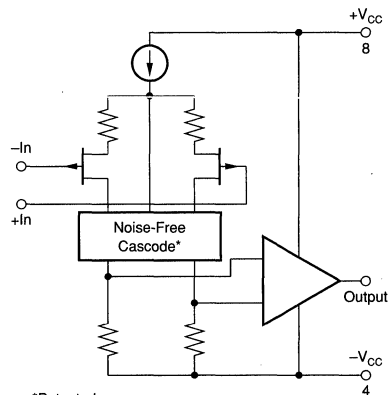
The OPA2111 is a high precision monolithic dielectrically isolated FET (*Difet*) operational amplifier. Outstanding performance characteristics allow its use in the most critical instrumentation applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with patented circuit design techniques. A cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard dual op amp pin configuration allows upgrading of existing designs to higher performance levels.



OPA2111 Simplified Circuit
(Each Amplifier)

BIFET[®] National Semiconductor Corp., *Difet*[®] Burr-Brown Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE														
Voltage, $f_o = 10\text{Hz}$	100% Tested		40	80		30	60		40	80		40		$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 100\text{Hz}$	100% Tested		15	40		11	30		15	40		15		$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 1\text{kHz}$	100% Tested		8	15		7	12		8	15		8		$\text{nV}/\sqrt{\text{Hz}}$
$f_o = 10\text{kHz}$	(1)		6	8		6	8		6	8		6		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 10\text{Hz to } 10\text{kHz}$	(1)		0.7	1.2		0.6	1		0.7	1.2		0.7		μVrms
$f_B = 0.1\text{Hz to } 10\text{Hz}$	(1)		1.6	3.3		1.2	2.5		1.6	3.3		1.6		$\mu\text{Vp-p}$
Current, $f_B = 0.1\text{Hz to } 10\text{Hz}$	(1)		15	24		12	19		15	24		15		fA-p-p
$f_o = 0.1\text{Hz to } 20\text{kHz}$	(1)		0.8	1.3		0.6	1		0.8	1		0.8		$\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE(2)														
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		± 0.1	± 0.75		± 0.05	± 0.5		± 0.1	± 0.75		± 0.3	± 2	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		± 2	± 6		± 0.5	± 2.8		± 2	± 6		± 8	± 15	$\mu\text{V}/^\circ\text{C}$
Match			± 1			± 0.5			2			2		$\mu\text{V}/^\circ\text{C}$
Supply Rejection		90	110		96	110		90	110		86	110		dB
Channel Separation	100Hz, $R_L = 2\text{k}\Omega$		± 3	± 31		± 3	± 16		± 3	± 31		± 3	± 50	$\mu\text{V/V}$
			136			136			136			136		dB
BIAS CURRENT(2)														
Input Bias Current	$V_{CM} = 0\text{VDC}$		± 2	± 8		± 1.2	± 4		± 2	± 8		± 3	± 15	pA
Match			± 1			± 0.5			± 1			2		pA
OFFSET CURRENT(2)														
Input Offset Current	$V_{CM} = 0\text{VDC}$		± 1.2	± 6		± 0.6	± 3		± 1.2	± 6		± 3	± 12	pA
IMPEDANCE														
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
VOLTAGE RANGE														
Common-Mode Input Range		± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	90	110		96	110		90	110		82	110		dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	110	125		114	125		110	125		106	125		dB
Match			3			2			3			3		dB
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	20Vp-p, $R_L = 2\text{k}\Omega$	16	32		16	32		16	32			32		kHz
Slew Rate	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	1	2		1	2		1	2			2		V/ μs
Settling Time, 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		6			6			6			6		μs
0.01%	10V Step		10			10			10			10		μs
Overload Recovery, 50% Overdrive(3)	Gain = -1		5			5			5			5		μs
RATED OUTPUT														
Voltage Output	$R_L = 2\text{k}\Omega$	± 10	± 11		± 10	± 11		± 10	± 11		± 10	± 11		V
Current Output	$V_O = \pm 10\text{VDC}$	± 5	± 10		± 5	± 10		± 5	± 10		± 5	± 10		mA
Output Resistance	DC, Open Loop		100			100			100			100		Ω
Load Capacitance Stability	Gain = +1		1000			1000			1000			1000		pF
Short Circuit Current		10	40		10	40		10	40		10	40		mA
POWER SUPPLY														
Rated Voltage			± 15			± 15			± 15			± 15		VDC
Voltage Range, Derated Performance		± 5		± 18	± 5		± 18	± 5		± 18	± 5		± 18	VDC
Current, Quiescent	$I_O = 0\text{mADC}$		5			5			5			5		mA
			7			7			7			7		mA
TEMPERATURE RANGE														
Specification	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	$^\circ\text{C}$
Operating "M" Package	Ambient Temp.	-55		+125	-55		+125	-55		+125	-55		+125	$^\circ\text{C}$
"P" Package											-40		+85	$^\circ\text{C}$
Storage "M" Package	Ambient Temp.	-65		+150	-65		+150	-65		+150	-65		+150	$^\circ\text{C}$
"P" Package											-40		+85	$^\circ\text{C}$
θ_{JA} Junction-Ambient			200			200			200			200(4)		$^\circ\text{C}/\text{W}$

NOTES: (1) Sample tested—this parameter is guaranteed. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) Typical $\theta_{JA} = 150^\circ\text{C}/\text{W}$ for plastic DIP.

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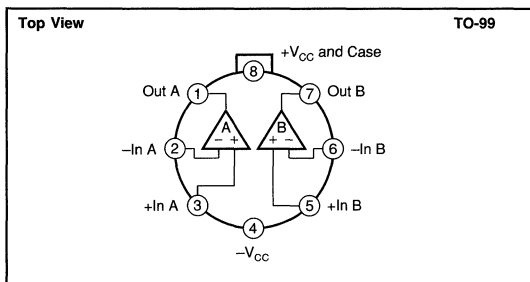
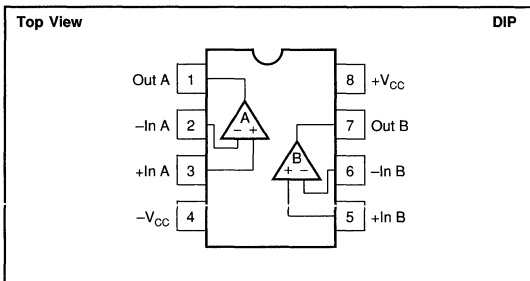
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITION	OPA2111AM			OPA2111BM			OPA2111SM			OPA2111KM, KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temp.	-25		+85	-25		+85	-55		+125	0		+70	°C
INPUT OFFSET VOLTAGE ⁽¹⁾ Input Offset Voltage Average Drift Match Supply Rejection	$V_{CM} = 0\text{VDC}$		± 0.22 ± 2 1 ± 10	± 1.2 ± 6 ± 50		± 0.08 ± 0.5 0.5 ± 10	± 0.75 ± 2.8 ± 32		± 0.3 ± 2 2 ± 10	± 1.5 ± 6 ± 50		± 0.9 ± 8 2 ± 10	± 5 ± 15 ± 80	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$
BIAS CURRENT ⁽¹⁾ Input Bias Current Match	$V_{CM} = 0\text{VDC}$		± 125 60	$\pm 1\text{nA}$ ± 50		± 75 30	± 500		$\pm 2\text{nA}$ 1nA	$\pm 16.3\text{nA}$		± 125 ± 500	pA pA	
OFFSET CURRENT ⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		± 75	± 750		± 38	± 375		$\pm 1.3\text{nA}$	$\pm 12\text{nA}$		± 75	± 375	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10 86	± 11 100		± 10 90	± 11 100		± 10 86	± 11 100		± 10 80	± 11 100		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain Match	$R_L \geq 2\text{k}\Omega$	106 86	120 100	5	110 90	120 100	3	106 86	120 100	5	100 80	120 100	5	dB dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40		± 10.5 ± 5 10	± 11 ± 10 40		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		5	8		5	8		5	8		5	10	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ($T_J \leq +175^\circ\text{C}$)	500mW
Differential Input Voltage	Total V_{CC}
Input Voltage Range	$\pm V_{CC}$
Storage Temperature Range: "M" Package	-65°C to $+150^\circ\text{C}$
"P" Package	-40°C to $+85^\circ\text{C}$
Operating Temperature Range: "M" Package	-55°C to $+125^\circ\text{C}$
"P" Package	-40°C to $+85^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short Circuit to Ground ($+25^\circ\text{C}$)	Continuous
Junction Temperature	$+175^\circ\text{C}$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA2111AM	TO-99	001
OPA2111BM	TO-99	001
OPA2111KM	TO-99	001
OPA2111SM	TO-99	001
OPA2111KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

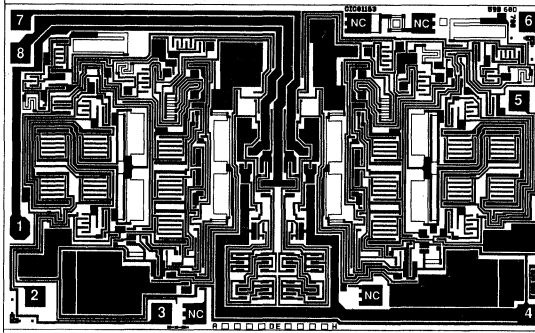
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE, max (mV)
OPA2111AM	TO-99	-25°C to $+85^\circ\text{C}$	± 0.75
OPA2111BM	TO-99	-25°C to $+85^\circ\text{C}$	± 0.5
OPA2111KM	TO-99	0°C to $+70^\circ\text{C}$	± 2
OPA2111SM	TO-99	-55°C to $+125^\circ\text{C}$	± 0.75
OPA2111KP	8-Pin Plastic DIP	0°C to $+70^\circ\text{C}$	± 2



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DICE INFORMATION



OPA2111AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	-In A
3	+In A
4	-V _s
5	+In B
6	-In B
7	Out B
8	+V _s
NC	No Connection

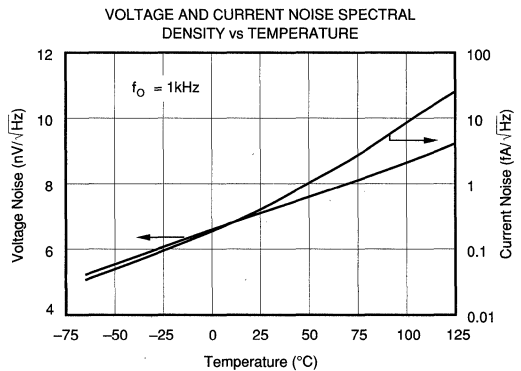
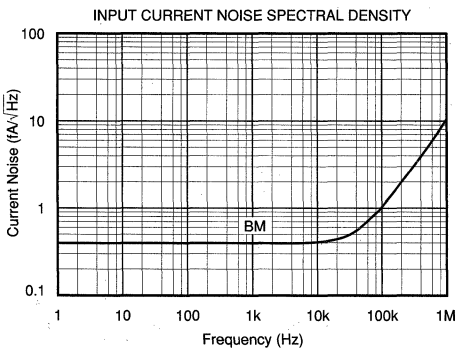
Substrate Bias: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	138 x 84 ±5	3.51 x 2.13 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		102

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{cc} = ±15VDC unless otherwise noted.

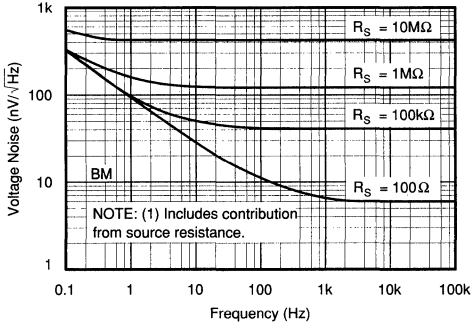


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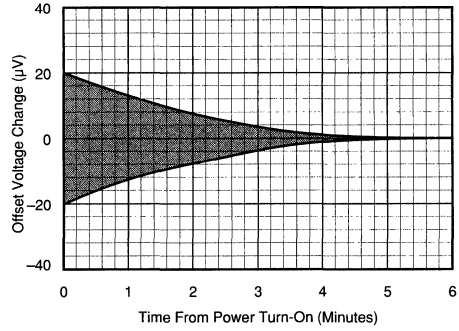
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.

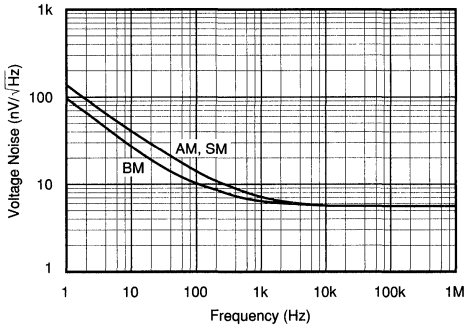
TOTAL⁽¹⁾ INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



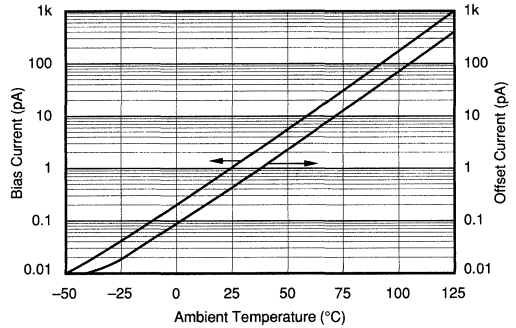
INPUT OFFSET VOLTAGE WARM-UP DRIFT



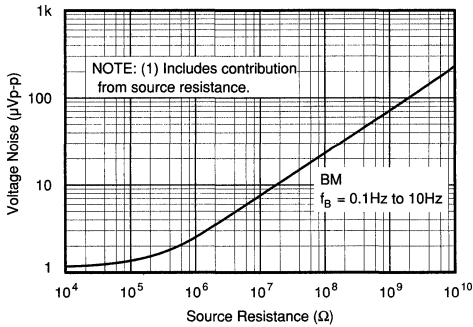
INPUT VOLTAGE NOISE SPECTRAL DENSITY



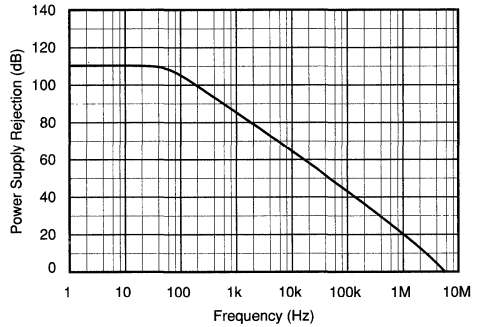
BIAS AND OFFSET CURRENT vs TEMPERATURE



TOTAL⁽¹⁾ INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



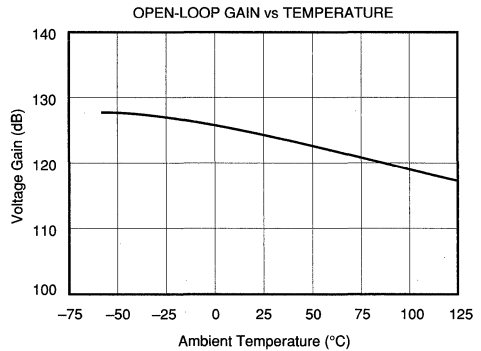
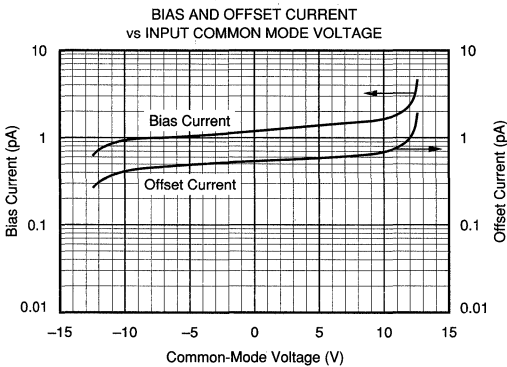
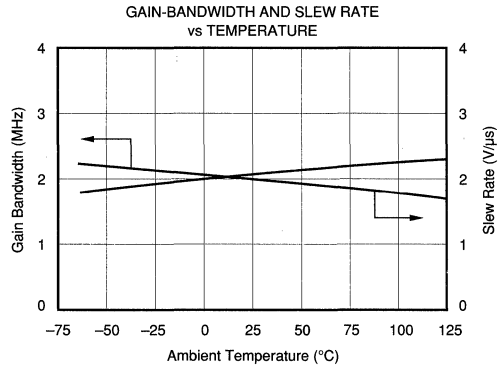
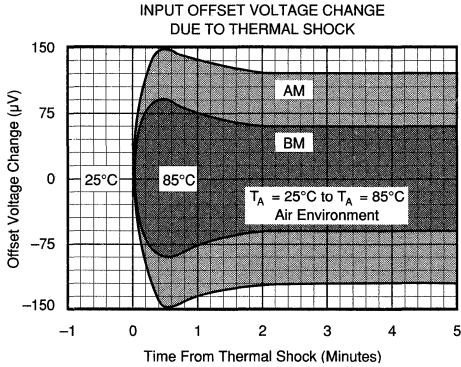
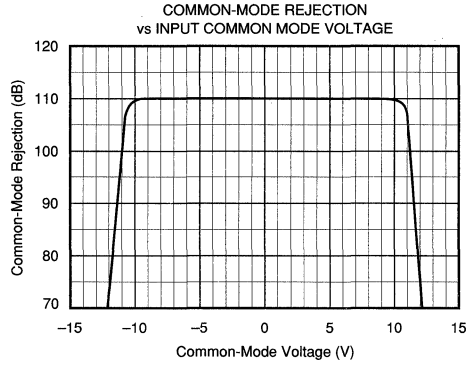
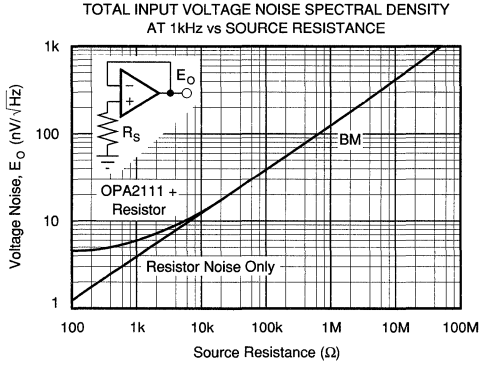
POWER SUPPLY REJECTION vs FREQUENCY



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TYPICAL PERFORMANCE CURVES (CONT)

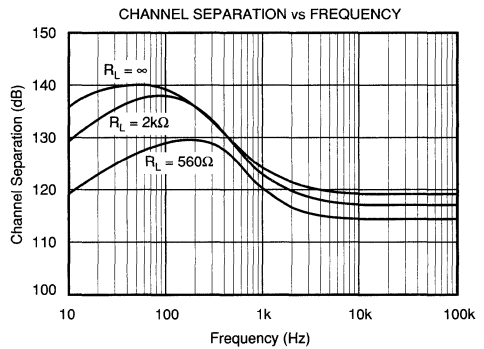
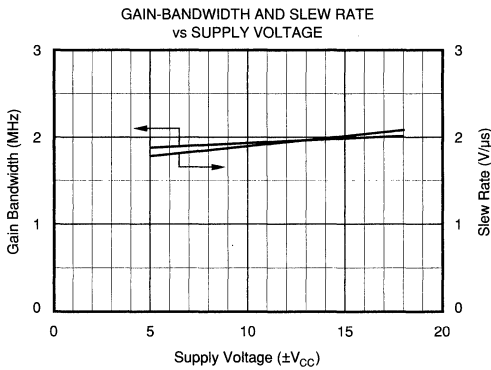
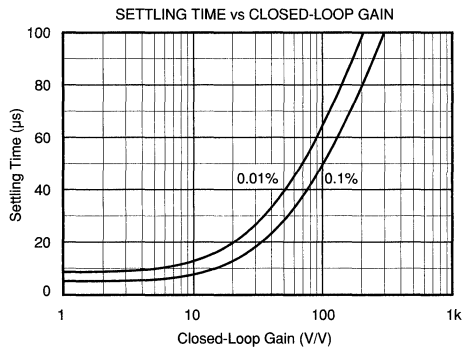
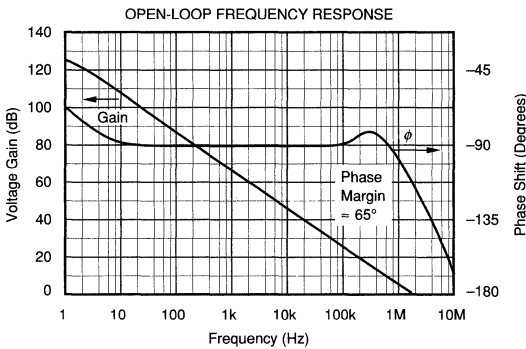
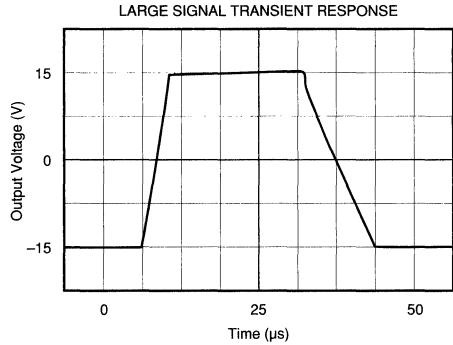
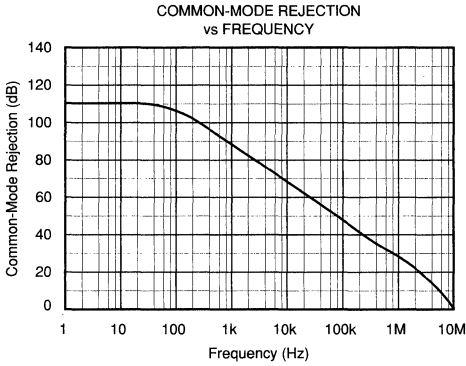
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

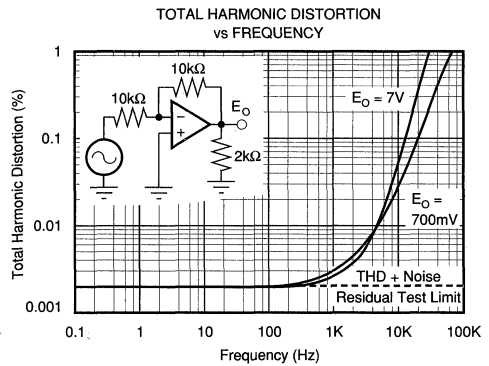
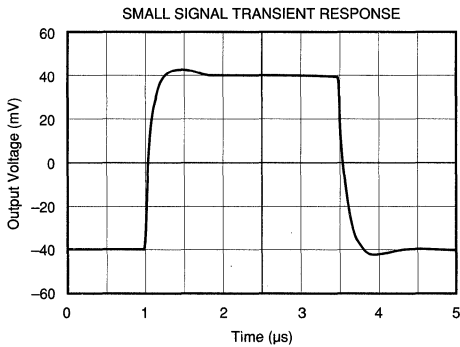
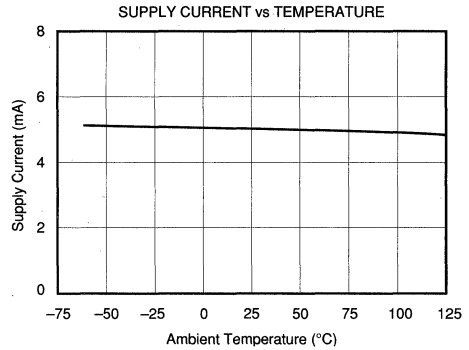
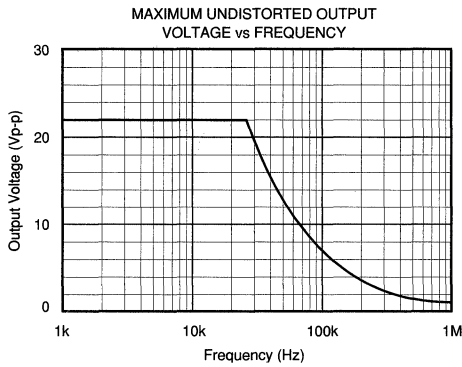
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA2111 offset voltage is laser-trimmed and will require no further trim for most applications.

Offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

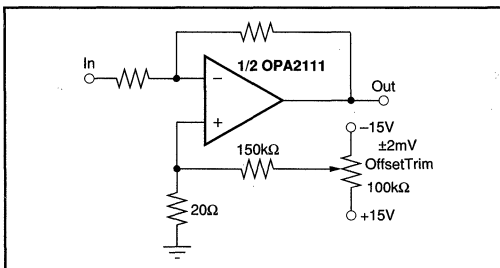


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA2111. Of course, the differential and common-mode voltage limits should be observed. Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA2111. To avoid leakage problems, it is recommended that the signal input lead of the OPA2111 be wired to a Teflon standoff. If the OPA2111 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 2).

NOISE: FET VS BIPOLAR

Low noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the low voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ the OPA2111 will have lower total noise than an OP-27 (see Figure 3).

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET® operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA2111 is not compromised by common-mode voltage.

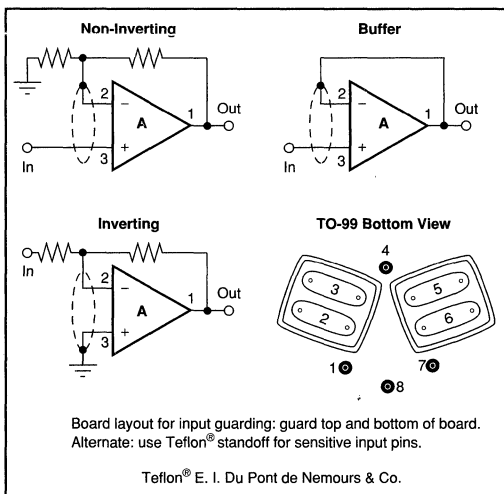


FIGURE 2. Connection of Input Guard.

APPLICATIONS CIRCUITS

Figures 5 through 13 are circuit diagrams of various applications for the OPA2111.

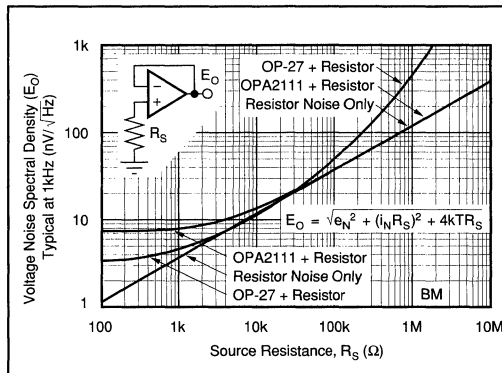


FIGURE 3. Voltage Noise Spectral Density vs Source Resistance.

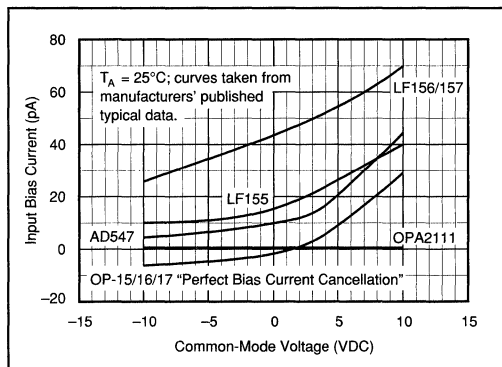


FIGURE 4. Input Bias Current vs Common Mode Voltage.

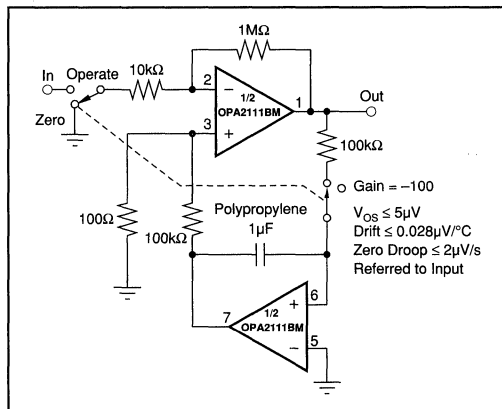


FIGURE 5. Auto-Zero Amplifier.

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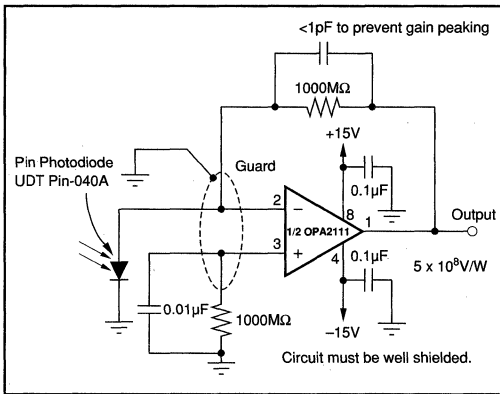


FIGURE 6. Sensitive Photodiode Amplifier.

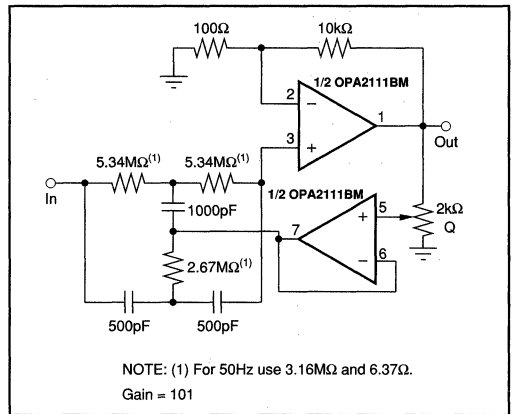


FIGURE 7. High Impedance 60Hz Reject Filter with Gain.

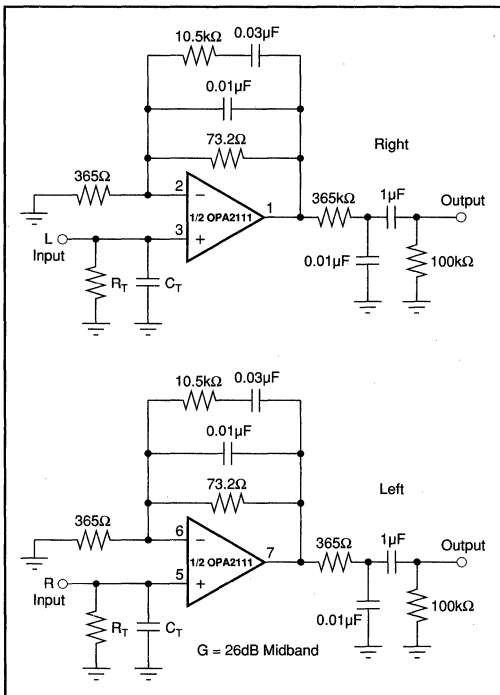


FIGURE 8. RIAA Equalized Stereo Preamp.

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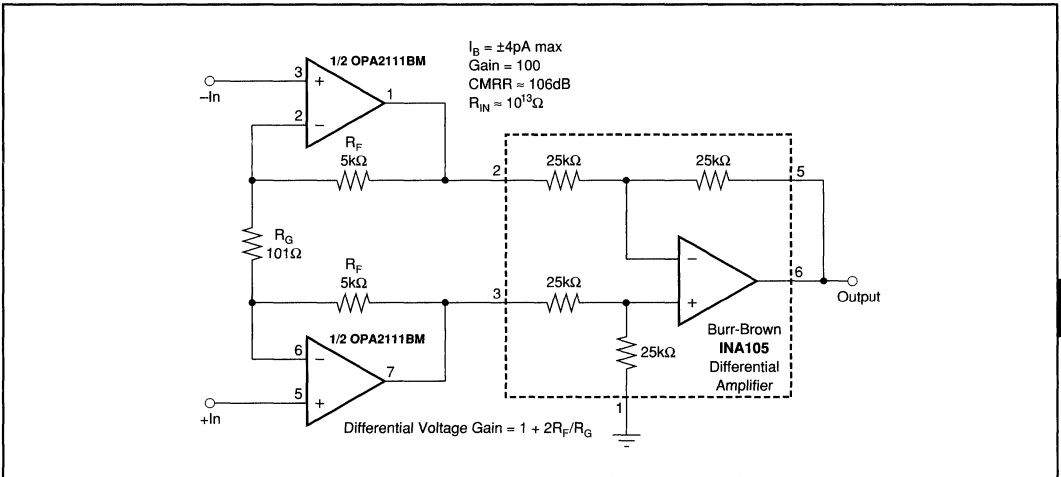


FIGURE 9. FET Input Instrumentation Amplifier.

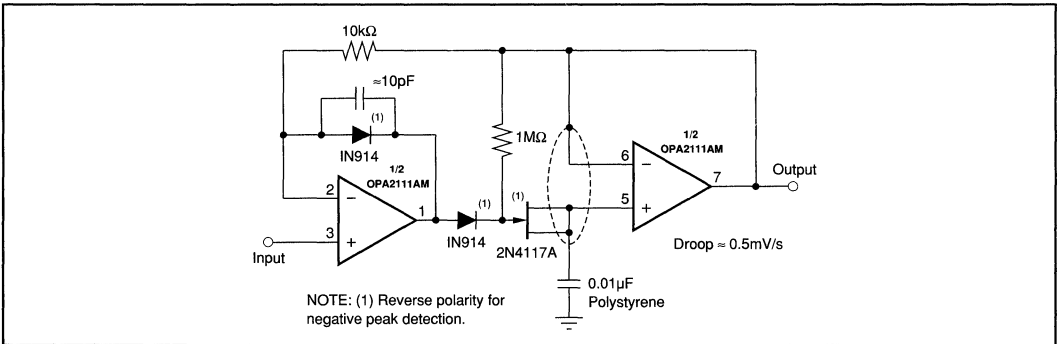


FIGURE 10. Low-Droop Positive Peak Detector.

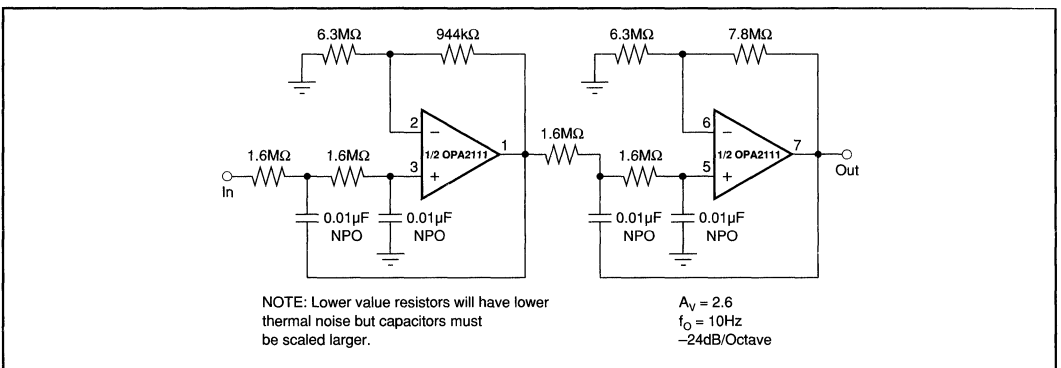


FIGURE 11. 10Hz Fourth-Order Butterworth Low-Pass Filter.

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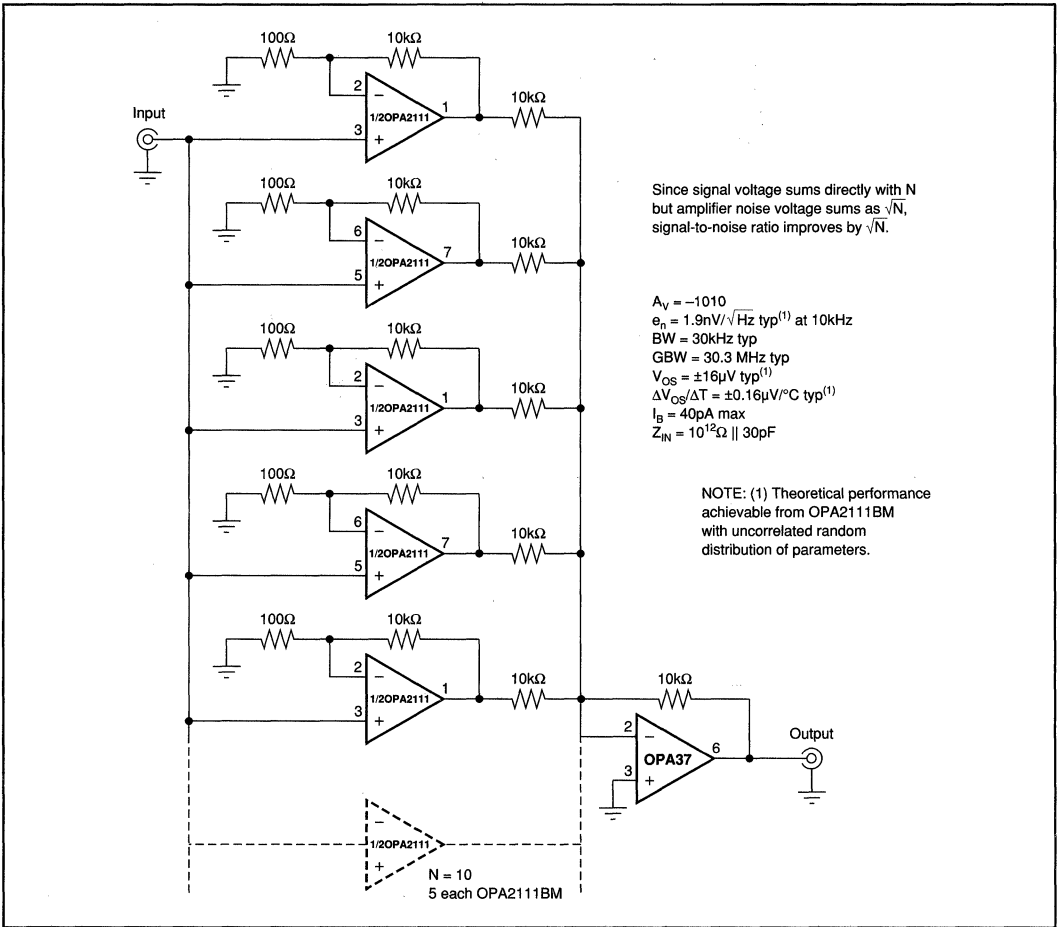


FIGURE 12. 'N' Stage Parallel-Input Amplifier.

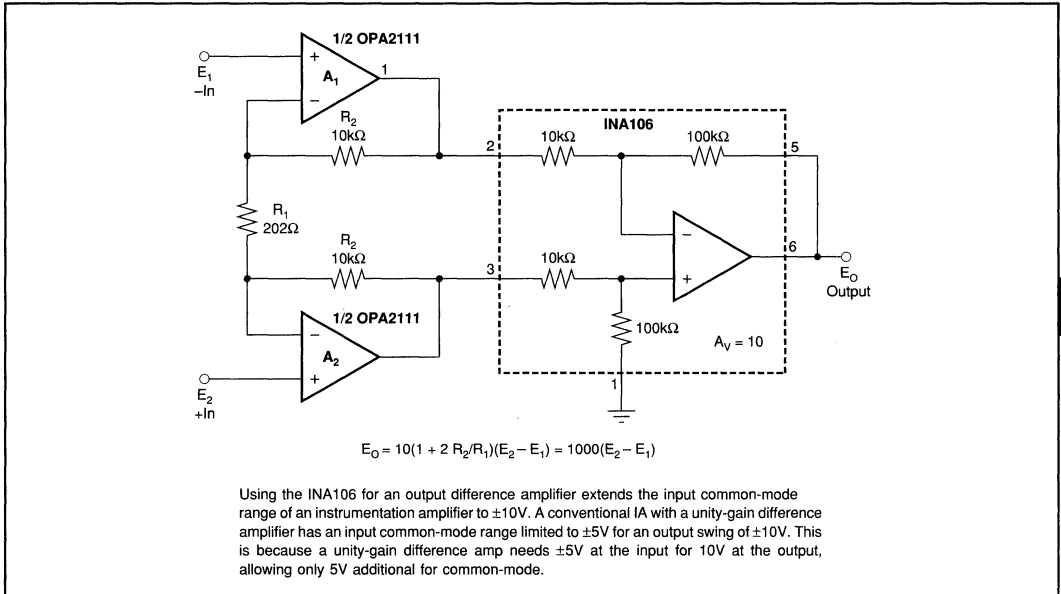
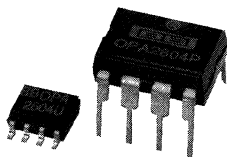


FIGURE 13. Precision Instrumentation Amplifier.

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OPA2604

Dual FET-Input, Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- **LOW DISTORTION:** 0.0003% at 1kHz
- **LOW NOISE:** $10\text{nV}/\sqrt{\text{Hz}}$
- **HIGH SLEW RATE:** $25\text{V}/\mu\text{s}$
- **WIDE GAIN-BANDWIDTH:** 20MHz
- **UNITY-GAIN STABLE**
- **WIDE SUPPLY RANGE:** $V_s = \pm 4.5$ to $\pm 24\text{V}$
- **DRIVES 600Ω LOADS**

APPLICATIONS

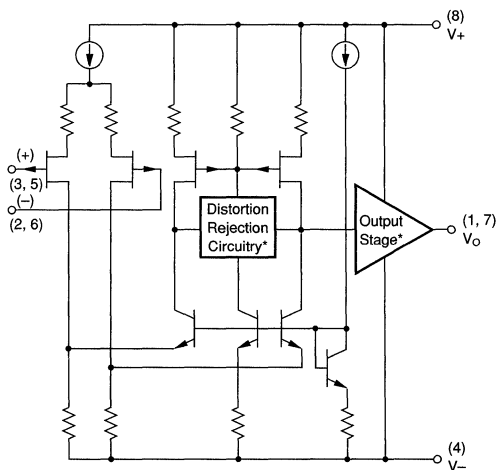
- **PROFESSIONAL AUDIO EQUIPMENT**
- **PCM DAC I/V CONVERTER**
- **SPECTRAL ANALYSIS EQUIPMENT**
- **ACTIVE FILTERS**
- **TRANSDUCER AMPLIFIER**
- **DATA ACQUISITION**

DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the -25°C to $+85^\circ\text{C}$ temperature range.



* Patents Granted:
#5053718, 5019789

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2604AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage Average Drift Power Supply Rejection	V _S = ±5 to ±24V	80	±1 ±8 100	±3	mV μV/°C dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	V _{CM} = 0V V _{CM} = 0V		100 ±4		pA pA
NOISE Input Voltage Noise Noise Density: f = 10Hz f = 100Hz f = 1kHz f = 10kHz Voltage Noise, BW = 20Hz to 20kHz Input Bias Current Noise Current Noise Density, f = 0.1Hz to 20kHz			25 15 11 10 1.5 6		nV/√Hz nV/√Hz nV/√Hz nV/√Hz μVp-p fA/√Hz
INPUT VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	V _{CM} = ±12V	±12 80	±13 100		V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹² 8 10 ¹² 10		Ω pF Ω pF
OPEN-LOOP GAIN Open-loop Voltage Gain	V _O = ±10V, R _L = 1kΩ	80	100		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time: 0.01% 0.1% Total Harmonic Distortion + Noise (THD + N) Channel Separation	G = 100 20Vp-p, R _L = 1kΩ G = -1, 10V Step G = 1, f = 1kHz V _O = 3.5Vrms, R _L = 1kΩ f = 1kHz, R _L = 1kΩ	15	20 25 1.5 1 0.0003 142		MHz V/μs μs μs % dB
OUTPUT Voltage Output Current Output Short Circuit Current Output Resistance, Open-Loop	R _L = 600Ω V _O = ±12V	±11	±12 ±35 ±40 25		V mA mA Ω
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Current, Total Both Amplifiers		±4.5	±15 ±10.5	±24 ±12	V V mA
TEMPERATURE RANGE Specification Storage Thermal Resistance ⁽²⁾ , θ _{JA}		-25 -40		+85 +125	°C °C °C/W

NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±25V
Input Voltage	(V ₋) - 1V to (V ₊) + 1V
Output Short Circuit to Ground	Continuous
Operating Temperature	-40°C to +100°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA2604AP	8-Pin Plastic DIP	-25°C to +85°C
OPA2604AU	SO-8 Surface-Mount	-25°C to +85°C

PACKAGING INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA2604AP	8-Pin Plastic DIP	006
OPA2604AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

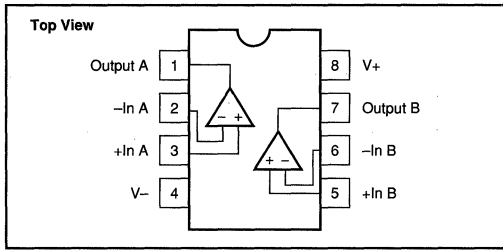
OPA2604

2

OPERATIONAL AMPLIFIERS

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PIN CONFIGURATION



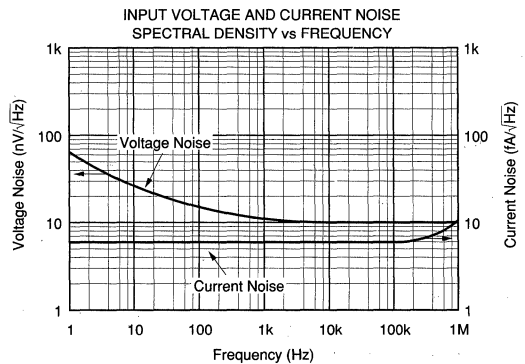
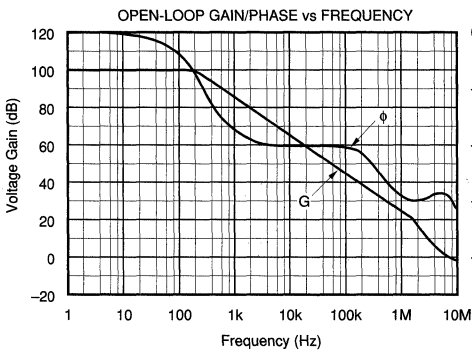
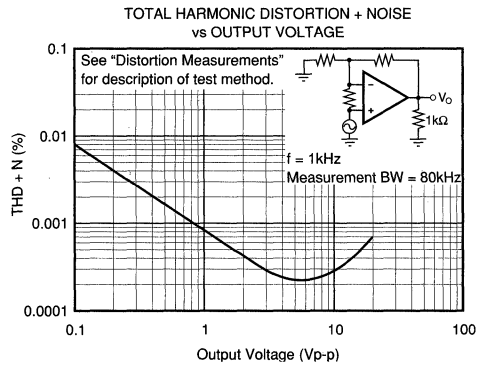
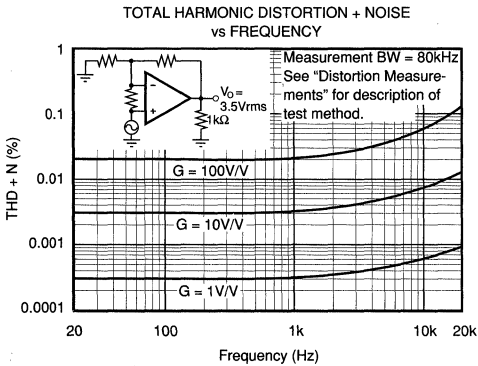
ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

TYPICAL PERFORMANCE CURVES

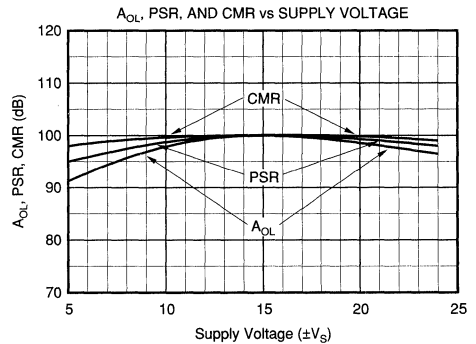
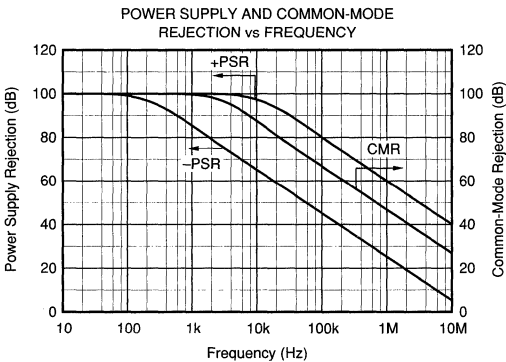
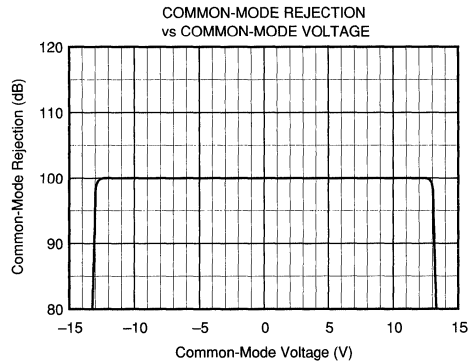
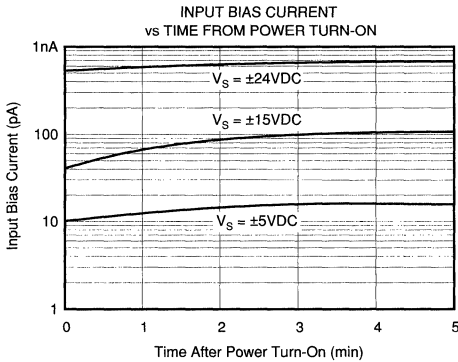
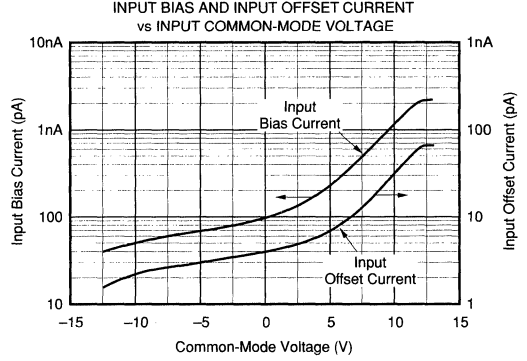
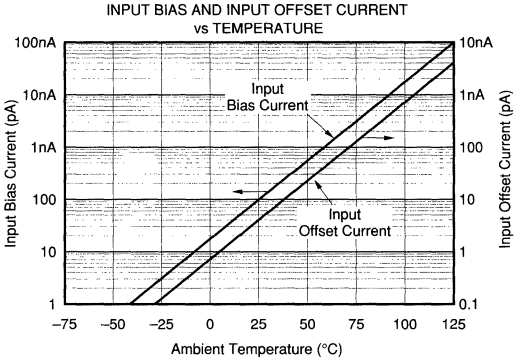
$T_A = +25^\circ\text{C}$, $V_s = \pm 15\text{V}$ unless otherwise noted.



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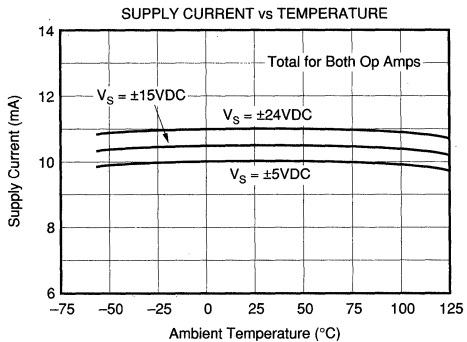
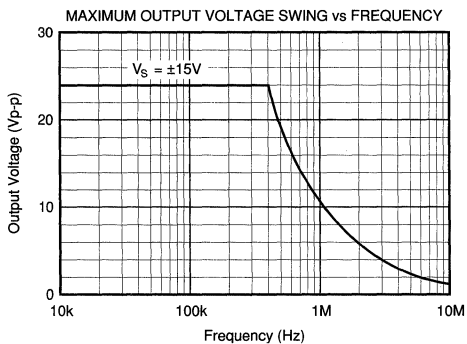
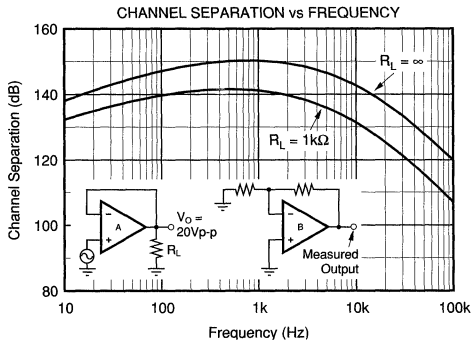
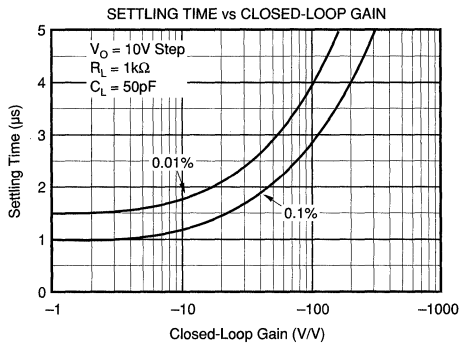
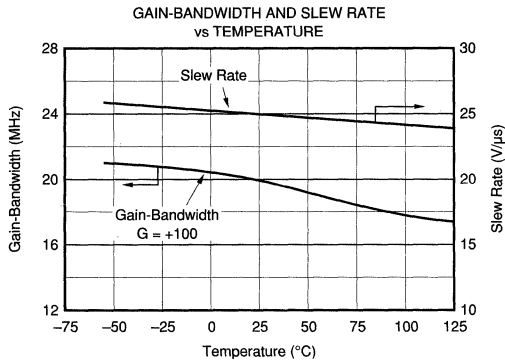
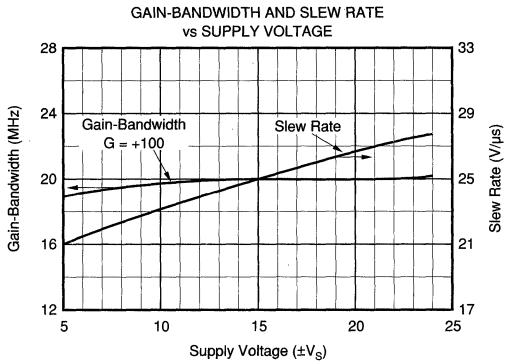
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

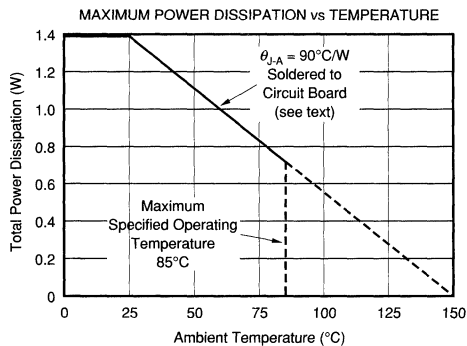
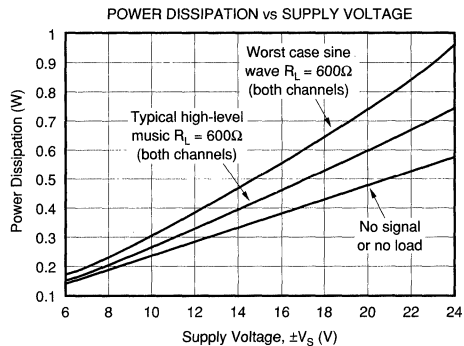
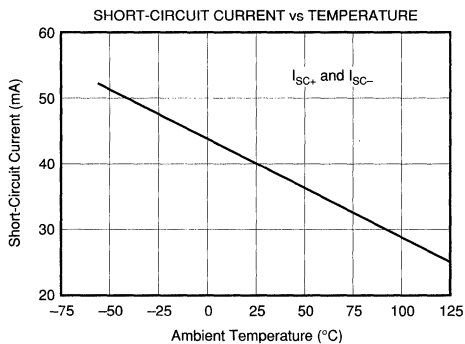
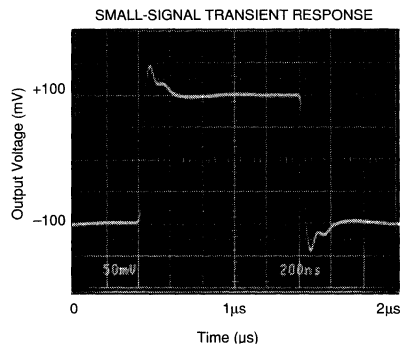
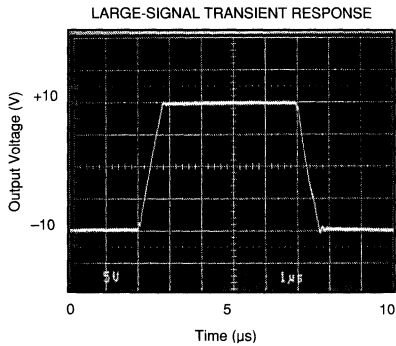
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

The OPA2604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 1 μ F tantalum capacitors are adequate.

DISTORTION MEASUREMENTS

The distortion produced by the OPA2604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 1 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3 .

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision, System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA2604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain

and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 2 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

For the unity-gain buffer, Figure 2a, stability is preserved by adding a phase-lead network, R_C and C_C . Voltage drop across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 2b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 2c and 2d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 2d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 2e and 2f show input lead compensation networks for inverting and difference amplifier configurations.

NOISE PERFORMANCE

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA2604 will generally provide lower noise.

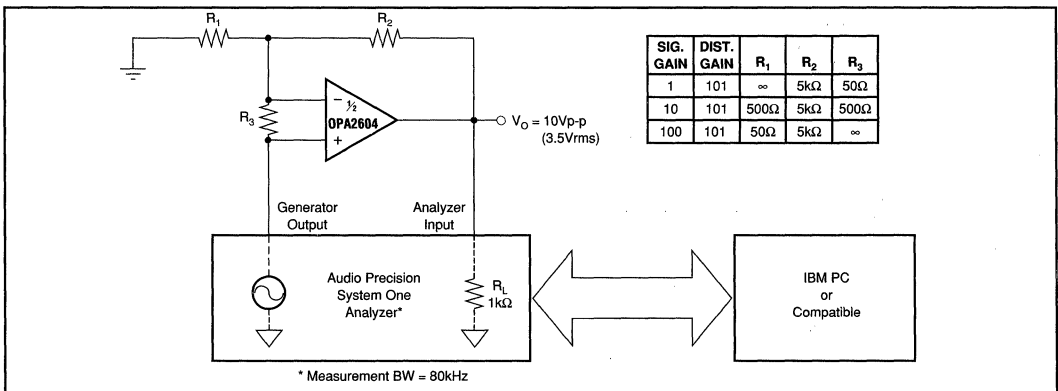
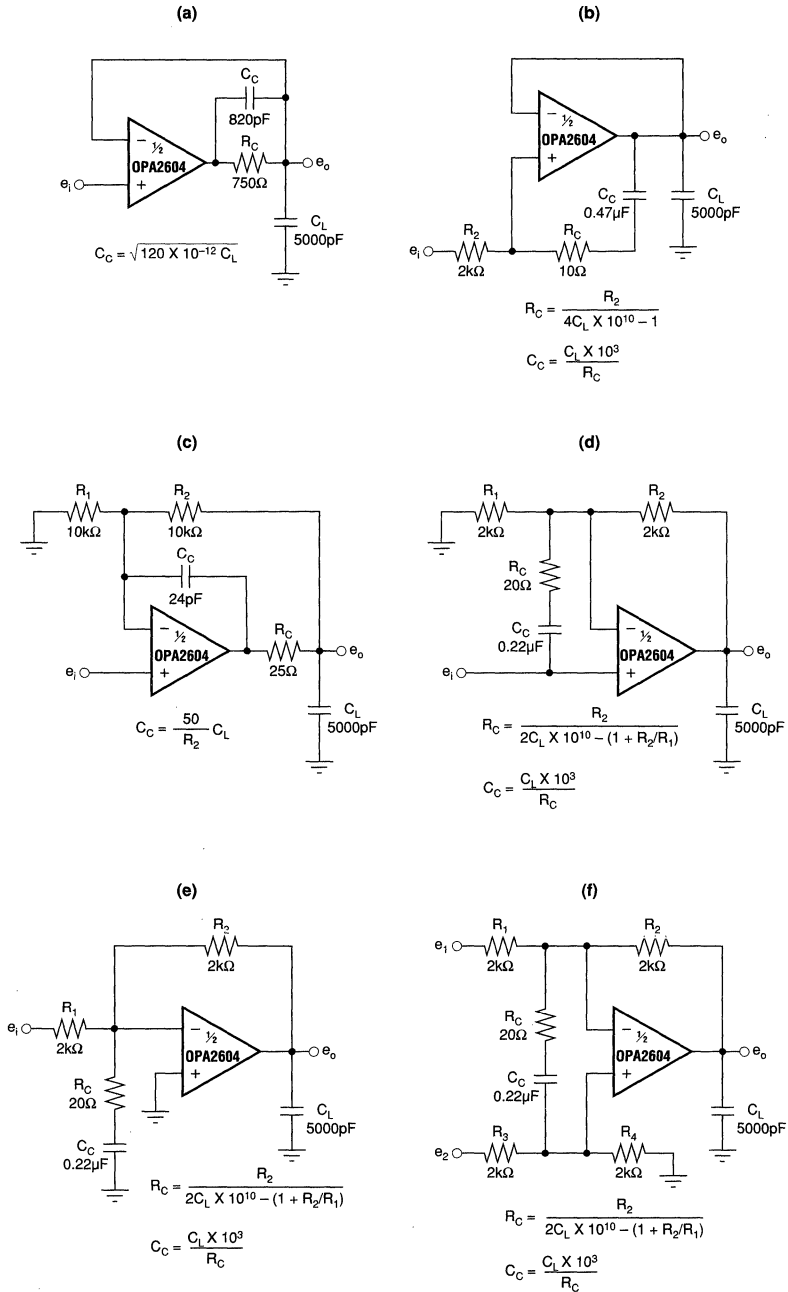


FIGURE 1. Distortion Test Circuit.

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NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 2. Driving Large Capacitive Loads.

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POWER DISSIPATION

The OPA2604 is capable of driving 600Ω loads with power supply voltages up to $\pm 24\text{V}$. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA2604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately $\pm 40\text{mA}$ at 25°C . The limit current decreases with increasing temperature as shown in the typical curves.

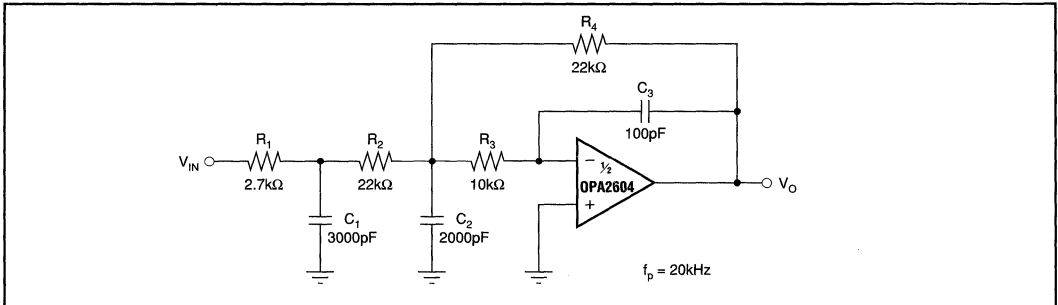


FIGURE 3. Three-Pole Low-Pass Filter.

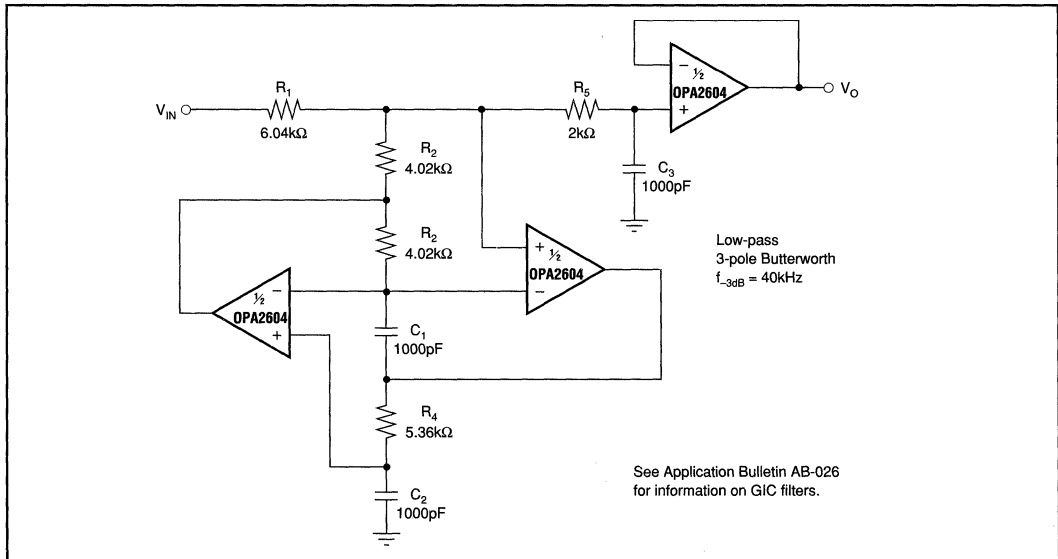


FIGURE 4. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

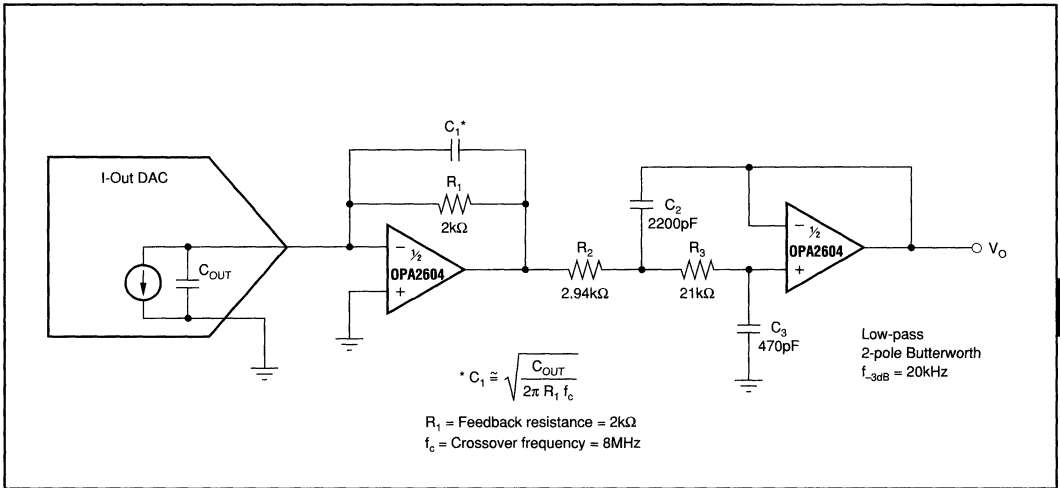


FIGURE 5. DAC I/V Amplifier and Low-Pass Filter.

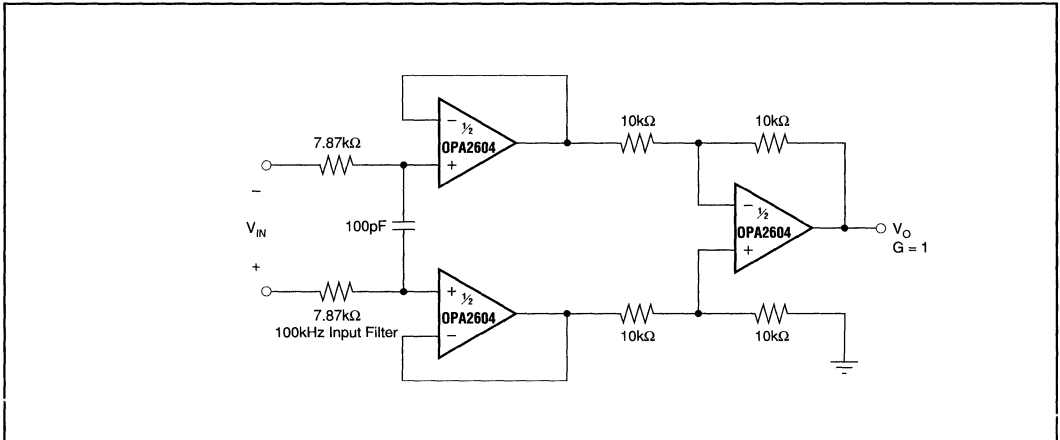


FIGURE 6. Differential Amplifier with Low-Pass Filter.

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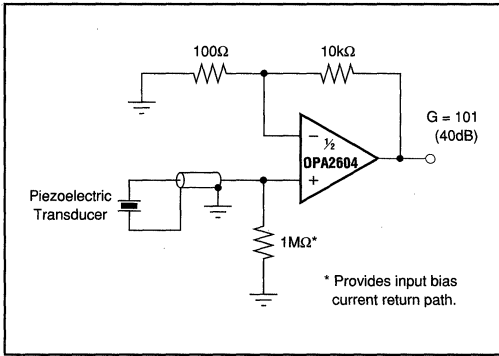


FIGURE 7. High Impedance Amplifier.

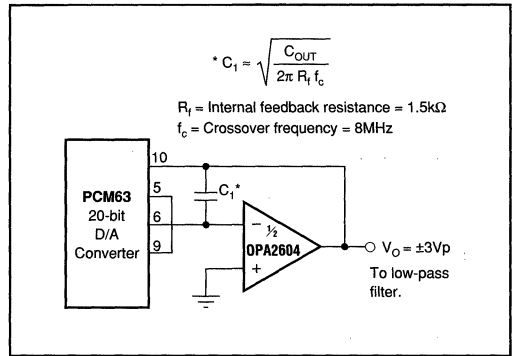


FIGURE 8. Digital Audio DAC I-V Amplifier.

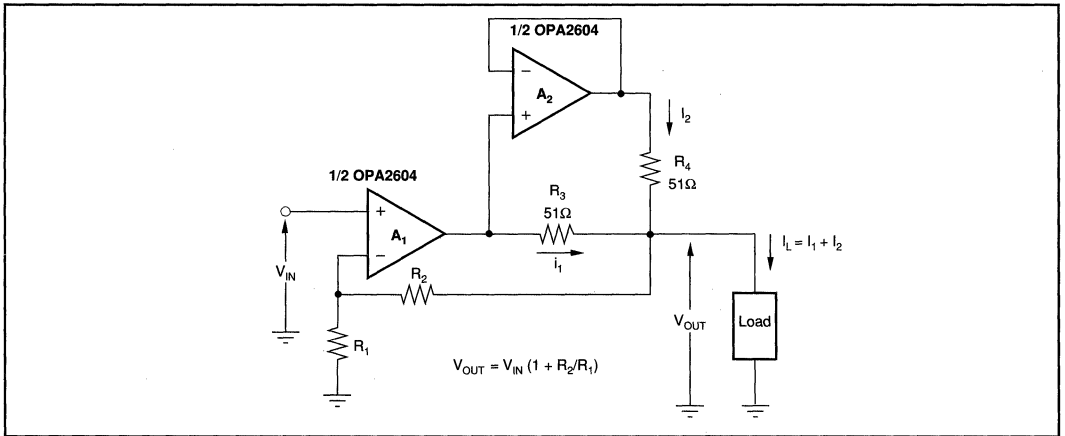


FIGURE 9. Using the Dual OPA2604 Op Amp to Double the Output Current to a Load.

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SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA2604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

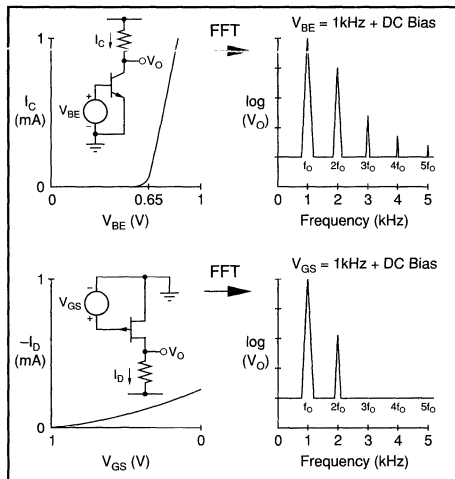
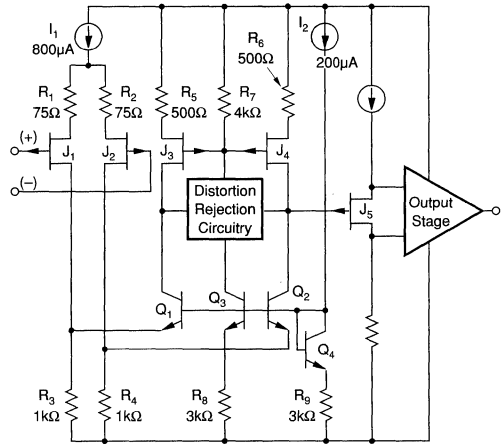


FIGURE 10. I-V and Spectral Response of NPN and JFET.



THE OPA2604 DESIGN

The OPA2604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important and where their transfer characteristics have minimal impact.

The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J_1 and J_2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high $800\mu\text{A}$, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of $\pm 25\text{V}/\mu\text{s}$.

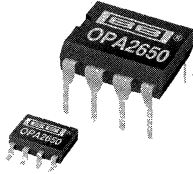
The JFET input stage holds input bias current to approximately 100pA , or roughly 3000 times lower than common bipolar-input audio op amps. This dramatically reduces noise with high-impedance circuitry.

The drains of J_1 and J_2 are cascoded by Q_1 and Q_2 , driving the input stage loads, FETs J_3 and J_4 . Distortion reduction circuitry (patent pending) linearizes the open-loop response and increases voltage gain. The 20MHz bandwidth of the OPA2604 further reduces distortion through the user-connected feedback loop.

The output stage consists of a JFET phase-splitter loaded into high speed all-NPN output drivers. Output transistors are biased by a special circuit to prevent cutoff, even with full output swing into 600Ω loads.

The two channels of the OPA2604 are completely independent, including all bias circuitry. This eliminates any possibility of crosstalk through shared circuits—even when one channel is overdriven.

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OPA2650

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER:** 50mW
- **UNITY GAIN STABLE BANDWIDTH:** 560MHz
- **FAST SETTLING TIME:** 15ns to 0.01%
- **LOW INPUT BIAS CURRENT:** 2.7 μ A
- **DIFFERENTIAL GAIN/PHASE ERROR:** 0.01%/0.01 $^\circ$
- **PACKAGE:** 8-Pin DIP and 8-Pin SOIC

APPLICATIONS

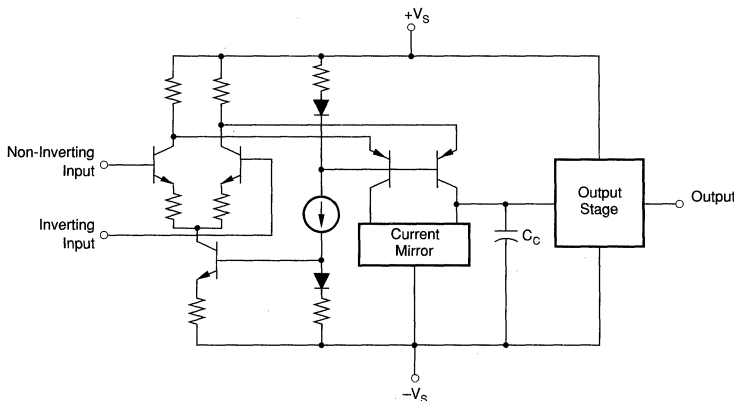
- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA2650 is a dual, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 15ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA2650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA2650 is also available in single OPA650 and quad OPA4650 configurations.



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SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA2650P, U			OPA2650PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth ⁽²⁾	G = +1		560			*(1)		MHz
	G = +2		160			*		MHz
	G = +5		40			*		MHz
	G = +10		18			*		MHz
Slew Rate ⁽³⁾	G = +1, 2V Step		180			*		V/μs
At Minimum Specified Temperature			155			*		V/μs
Rise Time			5.3			*		ns
Fall Time			5.9			*		ns
Settling Time 0.01%	G = +1, 2V Step		15			*		ns
0.1%	G = +1, 2V Step		11.5			*		ns
1%	G = +1, 2V Step		6			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz		82			*		dBc
	V _O = 2Vp-p							
Differential Gain	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω		0.01			*		%
	G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01			*		%
Differential Phase	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω		0.01			*		Degrees
	G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01			*		Degrees
Gain Flatness	DC to 100MHz		0.1			*		dB
Crosstalk	Input Referred, 5MHz, Channel-to-Channel					*		
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±3		±0.35	±1	mV
Average Drift			±5			3		μV/°C
Power Supply Rejection (+V _S)	V _S = ±4.5V to ±5.5V	50	70		60	*		dB
		45	55		48	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V _{CM} = 0V		2	5		*	4	μA
Over Temperature			3	8		*	5.5	μA
Input Offset Current	V _{CM} = 0V		0.4	1.5		*	*	μA
Over Temperature			0.9	3.0		*	*	μA
INPUT NOISE								
Input Voltage Noise						*		nV √Hz
Noise Density, f = 100Hz			23.2			*		nV √Hz
f = 10kHz			7.5			*		nV √Hz
f = 1MHz			7.1			*		nV √Hz
f = 10Hz to 100MHz			7.2			*		nVrms
Voltage Noise, BW = 10Hz to 100MHz			72			*		μVp-p
Input Bias Current Noise						*		pA √Hz
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA √Hz
Noise Figure (NF)	R _S = 10kΩ		3.0					dBm
	R _S = 50Ω		19.0					dBm
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.2	±2.8		*	*	V
Over Specified Temperature			52	57		65	85	dB
Common-Mode Rejection	V _{CM} = +2V							
INPUT IMPEDANCE								
Differential			15 1			*		kΩ pF
Common-Mode			16 1			*		MΩ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V _O = ±2V, R _L = 100Ω	45	51		47	55		dB
Over Specified Temperature	V _O = ±2V, R _L = 100Ω	43	49		45	53		dB
OUTPUT								
Voltage Output	No Load	±2.5	±2.75		*	*		V
Over Specified Temperature	R _L = 250Ω	±2.5	±2.7		*	*		V
	R _L = 100Ω	±2.0	±2.5		*	*		V
Current Output	+25°C to Max Temperature	±35	±50		±40	±55		mA
Over Specified Temperature		±25	±48		±30	±52		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +1		0.2			*		Ω
POWER SUPPLY								
Specified Operating Voltage		±4.5	±5	±5.5	*	*	*	V
Operating Voltage Range				±15.5				V
Quiescent Current			±10.5	±17.5		±10	±14	mA
Over Specified Temperature			±11	±17.5		±10.5	±16	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		-40		+85	*	*	*	°C
Thermal Resistance, θ _{JA}						*	*	°C/W
P			120			*	*	°C/W
U			170			*	*	°C/W

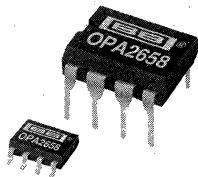
NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

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OPA2658

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

FEATURES

- UNITY GAIN STABLE BANDWIDTH: 900MHz
- LOW POWER: 47mW PER AMP
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.01%/0.01°
- HIGH SLEW RATE: 2000V/ μ s
- GAIN FLATNESS: 0.1dB TO 200MHz
- PACKAGE: 8-Pin DIP and 8-Pin SOIC

APPLICATIONS

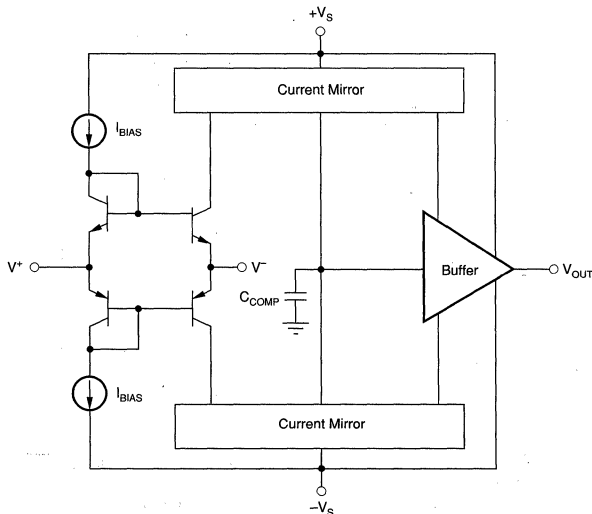
- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA2658 is a dual, ultra-wideband, low power current feedback video operational amplifier featuring a high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low

quiescent current make the OPA2658 a perfect choice for numerous video, imaging and communications applications.

The OPA2658 is internally compensated for unity-gain stability. The OPA2658 is also available in single, OPA658 and quad, OPA4658 configurations.



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SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{fb} = 402Ω, R_{fb} = 25 for a gain of +1, unless otherwise noted.

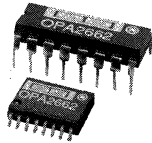
PARAMETER	CONDITION	OPA2658P, U			OPA2658PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth ⁽²⁾	G = +1		750			*(1)		MHz
	G = +2		700			*		MHz
	G = +5		320			*		MHz
	G = +10		195			*		MHz
Slew Rate ⁽³⁾	G = +1, 2V Step		1700			*		V/μs
At Minimum Specified Temperature			1500			*		V/μs
Settling Time: 0.01%	G = +1, 2V Step		15			*		ns
0.05%	G = +1, 2V Step		11.5			*		ns
0.2%	G = +1, 2V Step		6			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +1, V _O = 2Vp-p		75			*		dBc
	f = 20MHz, G = +1, V _O = 2Vp-p		TBD			*		dBc
Third-Order Intercept Point	f = 10MHz		TBD			*		dBm
Differential Gain	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 150Ω		0.025			*		%
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 400Ω		0.015			*		%
Differential Phase	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 150Ω		0.03			*		degrees
	G = +2, NTSC, V _O = 1.4Vp-p, R _L = 400Ω		0.015			*		degrees
Gain Flatness	G = +2, DC to 100 MHz		0.1			*		dB
Bandwidth for 0.1dB of Flatness	G = +2		TBD			TBD		MHz
Crosstalk	Input Referred, 5MHz, channel-to-channel		TBD			*		dB
OFFSET VOLTAGE								
Input Offset Voltage			±5	±8		±13	±5	mV
Over Specified Temperature			±25			15		μV/°C
Power Supply Rejection (+VS)	V _S = ±4.5 to ±5.5V	50	70		60	*		dB
(-VS)		45	55		48	*		dB
INPUT BIAS CURRENT								
Non-Inverting	V _{CM} = 0V		TBD	TBD		*	*	μA
Over Temperature			TBD	TBD		*	*	μA
Inverting	V _{CM} = 0V		TBD	TBD		*	*	μA
Over Temperature			TBD	TBD		*	*	μA
NOISE								
Input Voltage Noise Density	G = TBD							
f = 100Hz			TBD			*		nV/√Hz
f = 1kHz			TBD			*		nV/√Hz
f = 10kHz			TBD			*		nV/√Hz
f = 1MHz			TBD			*		nV/√Hz
f _B = 100Hz to 200MHz			TBD			*		μVrms
Inverting Input Bias Current						*		pA/√Hz
Noise Density: f = 10MHz			TBD			*		pA/√Hz
Non-Inverting Input Current						*		pA/√Hz
Noise Density: f = 10MHz			TBD			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-mode Input Range		±2.5	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-mode Rejection	V _{CM} = ±1V	57	62		75	85		dB
INPUT IMPEDANCE								
Differential			15 1		*	*		kΩ pF
Common-Mode			1.8 1		*	*		MΩ pF
OPEN-LOOP TRANSMIMPEDANCE								
Open-loop Transimpedance	V _O = ±2V, R _L = 100Ω	TBD	TBD		TBD	TBD		kΩ
Over Specified Temperature	V _O = ±2V, R _L = 100Ω	TBD	TBD		TBD	TBD		kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±2.9		*	*		V
Over Specified Temperature		±2.5	±2.75		*	*		V
Voltage Output	R _L = 250Ω	±2.7	±2.9		*	*		V
Over Specified Temperature		±2.5	±2.7		*	*		V
Voltage Output	R _L = 100Ω	±2.2	±2.8		*	*		V
Over Specified Temperature		±2.0	±2.5		*	*		V
Current Output	+25°C to max Temperature	±40	±52		*	*		mA
Over Specified Temperature		±30	±48		*	*		mA
Short Circuit Current			60		*	*		mA
Output Resistance, Open-Loop	1MHz, G = +1		0.2		*	*		Ω
POWER SUPPLY								
Specified Operating Voltage		±4.5	±5	±5.5	*	*	*	V
Operating Voltage Range	All Channels			±15.5	±6.5	*	*	V
Quiescent Current			±9.5	±15.5	*	*	*	mA
Over Specified Temperature			±9.8	±17	*	*	*	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		-40		+85	*	*	*	°C
Thermal Resistance, θ _{JA}								°C/W
P			120			*		°C/W
U			170			*		°C/W

NOTES: (1) An asterisk (*) specifies the same. (2) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

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OPA2662

Wide-Bandwidth, Dual, Power OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

FEATURES

- 370MHz BANDWIDTH
- 58mA/ns SLEW RATE
- HIGH OUTPUT CURRENT $\pm 75\text{mA}$
- 400Mbit/s DATA RATE
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ENABLE/DISABLE FUNCTION

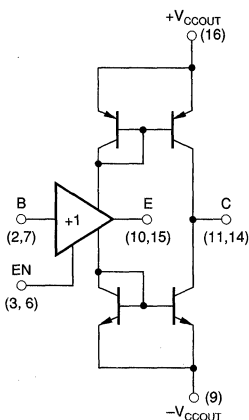
APPLICATIONS

- HEAD DRIVE AMPLIFIER FOR ANALOG/ DIGITAL VIDEO TAPES AND DATA RECORDERS
- LED AND LASER DIODE DRIVER
- HIGH CURRENT VIDEO BUFFER OR LINE DRIVER
- RF OUTPUT STAGE DRIVER
- HIGH DENSITY DISK DRIVES

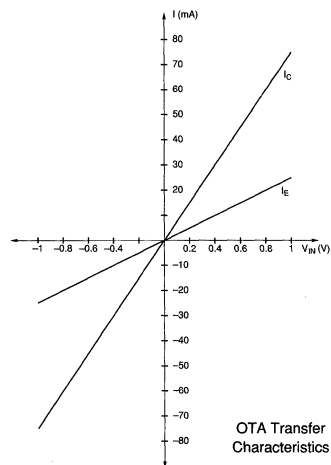
DESCRIPTION

The OPA2662 is a versatile driver device for ultra wide-bandwidth systems, including high-resolution video, RF and IF circuitry, communications and test equipment. The OPA2662 includes two power voltage-controlled current sources, or operational transconductance amplifiers (OTAs), in a 16-pin DIL or SOL package and is specified for the extended industrial temperature range (-40°C to $+85^{\circ}\text{C}$). The output current is zero for zero differential input voltage. The OTAs provide a 250MHz large-signal bandwidth, a 58mA/ns slew rate, and each current source delivers up to $\pm 75\text{mA}$ output current.

The transconductance of both OTAs can be adjusted between Pin 5 and $-V_{\text{CC}}$ by an external resistor, allowing bandwidth, quiescent current, harmonic distortion and gain trade-offs to be optimized. The output current can be set with a degeneration resistor between the emitter and GND. The current mirror ratio between the collector and emitter currents is fixed to three. Switching stages compatible to logic TTL levels make it possible to turn each OTA separately on within 30ns, and off within 200ns at full power.



1/2 OPA2662



OTA Transfer Characteristics

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SPECIFICATIONS

ELECTRICAL

DC-SPECIFICATIONS

At $V_{CC} = \pm 5V$, $R_O = 750\Omega$, $T_A = 25^\circ C$, and configured as noted under "CONDITIONS".

PARAMETER	CONDITIONS	OPA2662AP, AU			UNITS
		MIN	TYP	MAX	
OTA INPUT OFFSET VOLTAGE Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking) Matching	$R_E = 50k\Omega$, $R_C = 40\Omega$		12	± 30	mV
	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		35		$\mu V/^\circ C$
	$V_{CC} = +4.5V$ to $+5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		27		dB
	$V_{CC} = -4.5V$ to $-5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		15		dB
			40		dB
			2		mV
OTA B-INPUT BIAS CURRENT Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking) Matching	$R_E = 100\Omega$, $R_C = 40\Omega$		1	$-1/+5$	μA
	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		-5		$nA/^\circ C$
	$V_{CC} = +4.5V$ to $+5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		60		nA/V
	$V_{CC} = -4.5V$ to $5.5V$, $R_E = 50k\Omega$, $R_C = 1k\Omega$		160		nA/V
			40		nA/V
			0.2		μA
OTA C-OUTPUT BIAS CURRENT Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking) Matching	$R_E = 100\Omega$, $R_C = 1k\Omega$		0.5	$-0.5/+1.5$	μA
	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$		1.5		$\mu A/^\circ C$
	$V_{CC} = +4.5V$ to $+5.5V$		72		$\mu A/V$
	$V_{CC} = -4.5V$ to $-5.5V$		236		$\mu A/V$
			92		$\mu A/V$
			0.06		mA
B-INPUT IMPEDANCE Impedance	$I_O = \pm 17mA$		$4.5 \parallel 1.5$		$M\Omega \parallel pF$
OTA INPUT NOISE Input Noise Voltage Density Output Noise Current Density Signal-to-Noise Ratio	$f = 20kHz$ to $100MHz$		4.4		nV/\sqrt{Hz}
			0.09		nA/\sqrt{Hz}
	$S/N = 20 \log \cdot (0.7/V_N \cdot \sqrt{5MHz})$		97		dB
OTA C-RATED OUTPUT Output Voltage Compliance Output Current Output Impedance, r_C	$I_C = \pm 5mA$, $R_E = 100\Omega$, $R_C = 1k\Omega$		± 3.4		V
	$R_C = 40\Omega$, $R_E = 100\Omega$		± 75		mA
	$V_{IN} = \pm 3V$				
	$I_O = \pm 17mA$		$4.5 \parallel 6.5$		$k\Omega \parallel pF$
OTA E-RATED OUTPUT Voltage Output DC Current Output Voltage Gain Output Impedance, r_E	$R_E = 100\Omega$, $R_C = 40\Omega$		± 3.0		V
	$R_E = 100\Omega$, $R_C = 40\Omega$				
	$V_{IN} = \pm 4V$		± 25		mA
	$V_{IN} = \pm 2.5V$				
	$R_E = 100\Omega$		0.86		V/V
	$R_F = 50k\Omega$		0.98		V/V
	$I_O = \pm 17mA$		$16 \parallel 2.2$		$\Omega \parallel pF$
POWER SUPPLY Rated Voltage Derated Performance Positive Quiescent Current for both OTAs ⁽⁴⁾ Positive Quiescent Current for both OTAs ⁽⁴⁾ Quiescent Current Range	$R_E = 50k\Omega$, $R_C = 1k\Omega$	± 4.5		± 5.5	VDC
	$R_E = 50k\Omega$, $R_C = 40\Omega$	± 3		± 6	VDC
	$R_O = 750\Omega$, $R_E = 50k\Omega$, $R_C = 1k\Omega$, Both Channels Enabled	$+15$	$+17$	$+18$	mA
	$R_O = 750\Omega$, $R_E = 50k\Omega$, $R_C = 1k\Omega$, Both Channels Disabled		$+4$		mA
	Programmable $R_O = 3k\Omega$ to 30Ω	± 3		± 65	mA
TEMPERATURE RANGE Specification Thermal Resistance, θ_{JA} AP AU	Ambient Temperature	-40		$+85$	$^\circ C$
			90		$^\circ C/W$
			100		$^\circ C/W$

NOTES: (1) Characterization sample; (2) "Typical Values" are Mean values. The average of the two amplifiers is used for amplifier specific parameters. (3) "Min" and "Max" Values are mean ± 3 Standard Deviations. Worst case of the two amplifiers (Mean ± 3 Standard Deviations) is used for amplifier specific parameters. (4) I_{CO} typically 2mA less than I_{CO} due to OTA C-Output Bias Current and TTL Select Circuit Current.

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SPECIFICATIONS (CONT)

ELECTRICAL

AC-SPECIFICATION

Typical at $V_{CC} = \pm 5VDC$, $R_O = 750\Omega$, $I_C = \pm 37.5mA$ ($V_{IN} = 2.5Vpp$, $R_E = 100\Omega$), $I_C = \pm 75mA$ ($V_{IN} = 2.5Vpp$, $R_E = 50\Omega$), $R_{SOURCE} = 50\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA2662AP, AU			UNITS
		MIN	TYP	MAX	
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH $I_C = \pm 37.5mA$ $I_C = \pm 75mA$ $I_C = \pm 37.5mA$ (Optimized) $I_C = \pm 75mA$ (Optimized)	$R_E = 100\Omega$, $R_C = 50\Omega$		150		MHz
	$R_E = 100\Omega$, $R_C = 25\Omega$		200		MHz
	$R_E = 100\Omega$, $R_C = 50\Omega$, $C_C = 5.6pF$		370		MHz
	$R_E = 100\Omega$, $R_C = 25\Omega$, $C_C = 5.6pF$		250		MHz
GROUP DELAY TIME Measured Input to Output (Demo Board Used)	$R_E = 100\Omega$, $R_C = 50\Omega$ B to E		1.2		ns
	B to C		2.5		ns
HARMONIC DISTORTION Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic	$f = 10MHz$, $I_C = \pm 37.5mA$		-31		dBc
			-37		dBc
	$f = 10MHz$, $I_C = \pm 75mA$		-33		dBc
			-32		dBc
	$f = 30MHz$, $I_C = \pm 37.5mA$		-29		dBc
			-32		dBc
	$f = 30MHz$, $I_C = \pm 75mA$		-30		dBc
			-25		dBc
	$f = 50MHz$, $I_C = \pm 37.5mA$		-31		dBc
			-30		dBc
	$f = 50MHz$, $I_C = \pm 75mA$		-28		dBc
			-23		dBc
CROSSTALK Typical Curve Number 3 $I_C = \pm 37.5mA$, $f = 30MHz$ $I_C = \pm 75mA$, $f = 30MHz$			-51		dB
			-56		dB
FEEDTHROUGH Off Isolation	$R_E = 100\Omega$, $f = 30MHz$		-90		dB
	$R_E = 50\Omega$, $f = 30MHz$		-90		dB
TIME DOMAIN					
RISE TIME	10% to 90%				ns
	75mA Step I_C 150mA Step I_C		2 2.6		ns
SLEW RATE	$I_C = 75mA$		37.5		mA/ns
	$I_C = 150mA$		58		mA/ns

CHANNEL SELECTION

PARAMETER	CONDITIONS	OPA2662AP, AU			UNITS
		MIN	TYP	MAX	
ENABLE INPUTS Logic 1 Voltage Logic 0 Voltage Logic 1 Current Logic 0 Current		2		$V_{CC} + 0.6$	V
		0		0.8	V
	$V_{SEL} = 2.0V$ to $5V$	0.8	1.1	10	μA
	$V_{SEL} = 0V$ to $0.8V$	-1	0.05		μA
SWITCHING CHARACTERISTICS EN to Channel ON Time EN to Channel OFF Time Switching Transient, Positive Switching Transient, Negative	$I_C = 150mA$ p-p, $f = 5MHz$		30		ns
	90% Point of $V_O = 1V$ p-p		200		ns
	10% Point of $V_O = 1V$ p-p (Measured While Switching Between the Grounded Channels)		30		mV
			-80		mV

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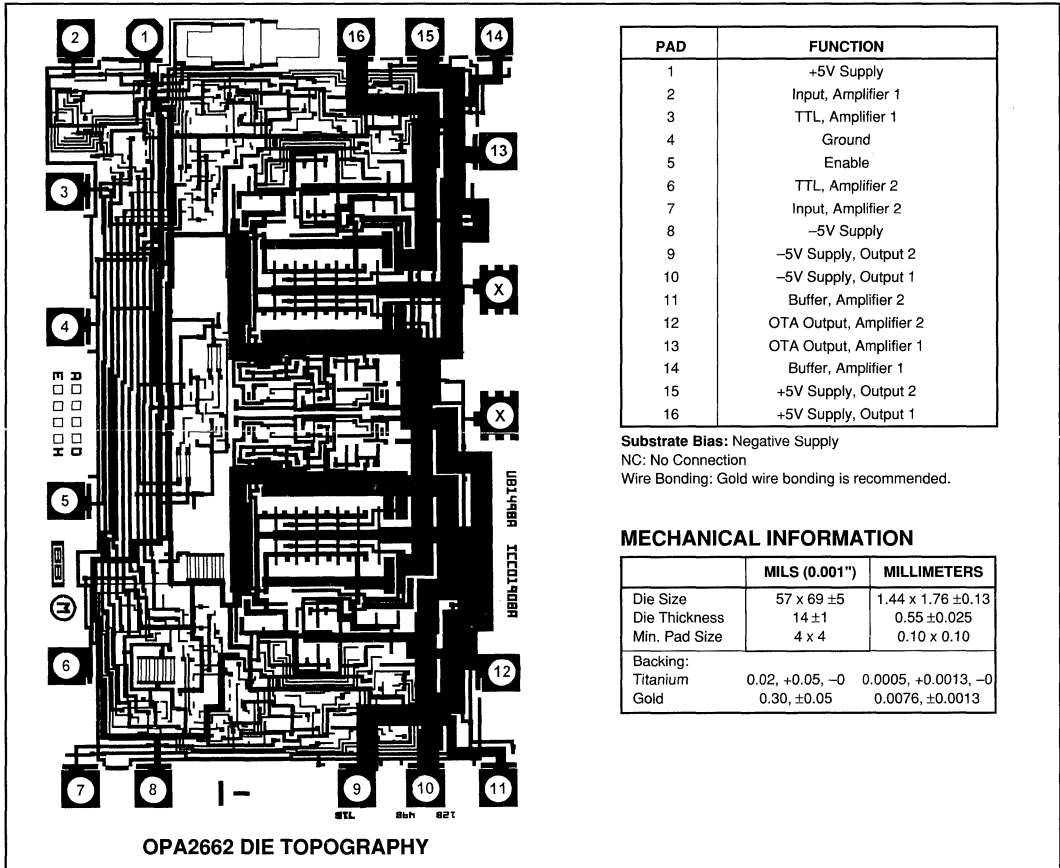
SPECIFICATIONS (CONT)

ELECTRICAL (Full Temperature Range -40°C to $+85^{\circ}\text{C}$)

At $V_{\text{CC}} = \pm 5\text{VDC}$, $R_{\text{O}} = 750\Omega$, $T_{\text{A}} = T_{\text{MIN}}$ to T_{MAX} , unless otherwise noted, and configured as noted under "CONDITIONS".

PARAMETER	CONDITIONS	OPA2662AP, AU			UNITS
		MIN	TYP	MAX	
OTA INPUT OFFSET VOLTAGE	$R_{\text{E}} = 50\text{k}\Omega$, $R_{\text{O}} = 40\Omega$				
			12	± 36	mV
OTA INPUT BIAS CURRENT	$R_{\text{E}} = 100\Omega$, $R_{\text{O}} = 40\Omega$				
			2	± 7.2	mV
OTA INPUT BIAS CURRENT	$R_{\text{E}} = 100\Omega$, $R_{\text{O}} = 40\Omega$				
			-1.9	1	μA
OTA TRANSCONDUCTANCE	$I_{\text{C}} = 75\text{mA}$, $R_{\text{E}} = 0$				
			-1.2	0.2	μA
OTA TRANSCONDUCTANCE	$I_{\text{C}} = 75\text{mA}$, $R_{\text{E}} = 0$				
			580	610	mA/V
OTA C-RATED OUTPUT	$I_{\text{C}} = \pm 5\text{mA}$, $R_{\text{E}} = 100\Omega$, $R_{\text{O}} = 16\Omega$				
			± 3.2		V
POWER SUPPLY	$R_{\text{O}} = 750\Omega$, $R_{\text{E}} = 50\text{k}\Omega$, $R_{\text{O}} = 1\text{k}\Omega$, Both Channels Selected				
			+8	+17	+25

DICE INFORMATION



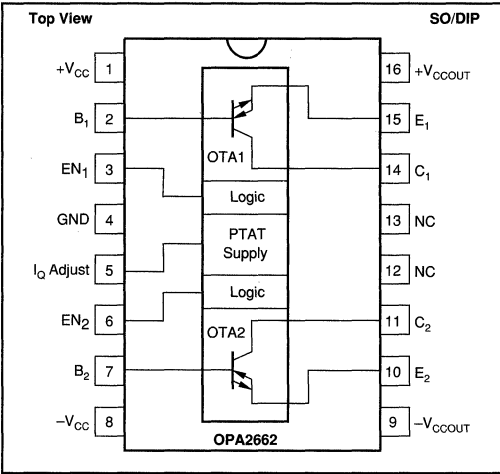
OPA2662

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OPERATIONAL AMPLIFIERS

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage ⁽¹⁾	±V _{CC} to ±0.7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (EN ₁ , EN ₂)	-0.5 to +V _{CC} +0.7V

NOTE: (1) Inputs are internally diode-clamped to ±V_{CC}.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
OPA2662AP	16-Pin Plastic DIP	-40°C to +85°C
OPA2662AU	16-Pin SOIC	-40°C to +85°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA2662AP	16-Pin Plastic DIP	180
OPA2662AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. ESD can cause damage ranging from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

Burr-Brown's standard ESD test method consists of five 1000V positive and negative discharges (100pF in series with 1.5kΩ) applied to each pin.



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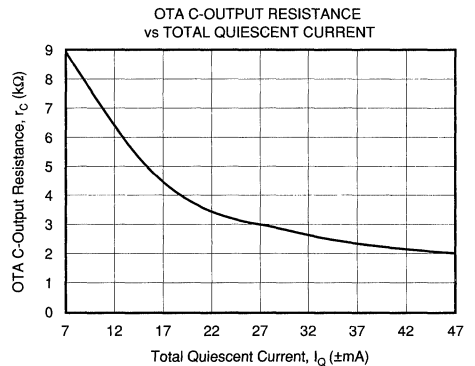
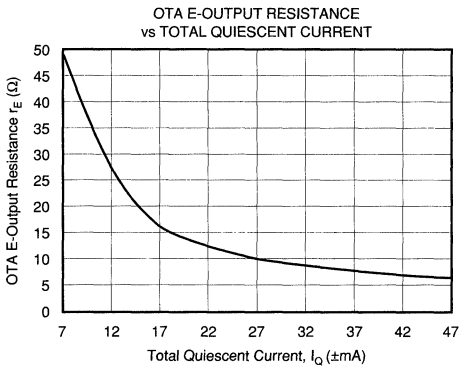
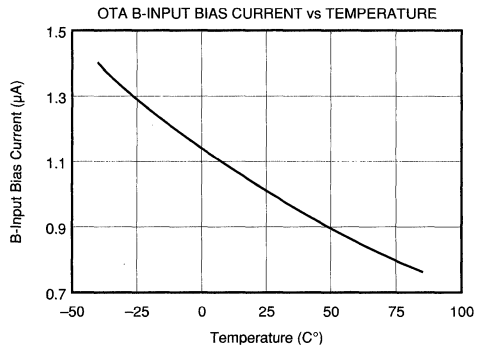
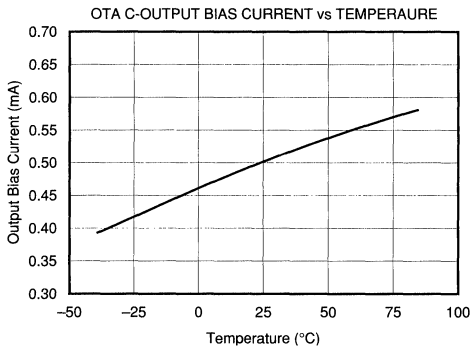
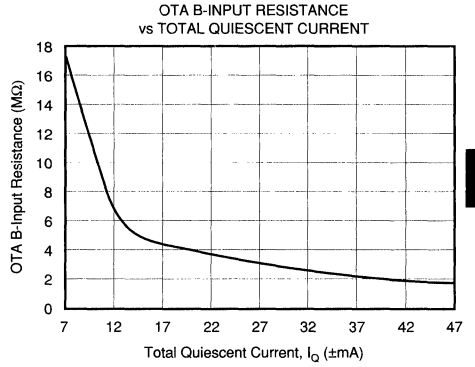
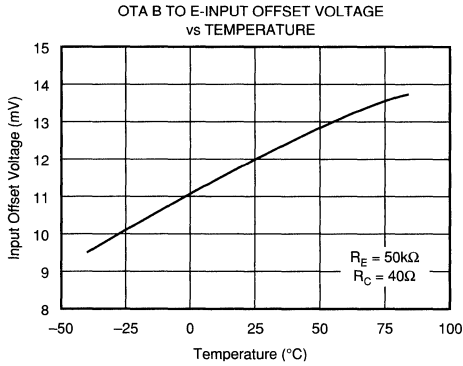
TYPICAL PERFORMANCE CURVES

At $V_{cc} = \pm 5V$, $R_O = 750\Omega$, and $T_A = +25^\circ C$ unless otherwise specified.

OPA2662

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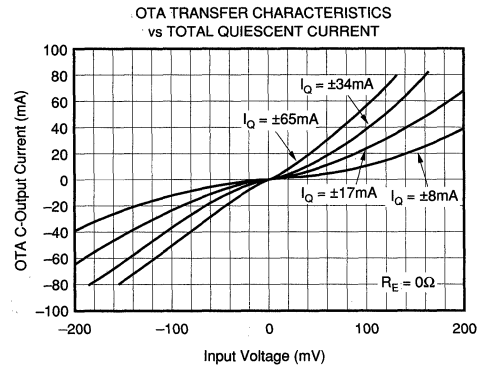
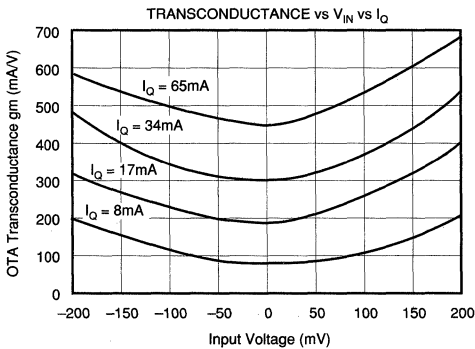
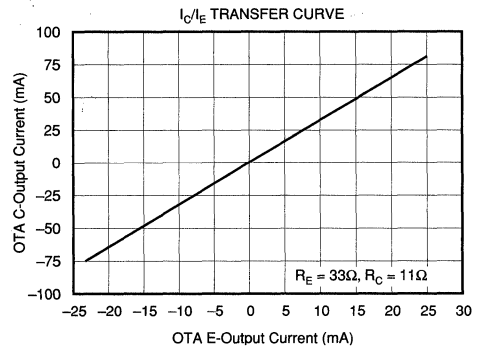
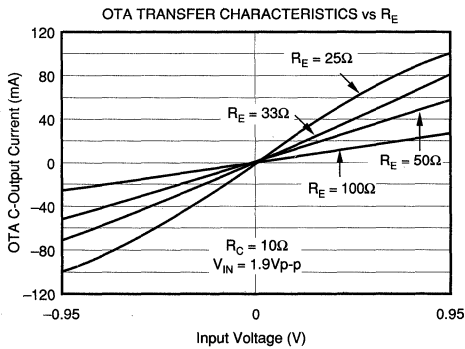
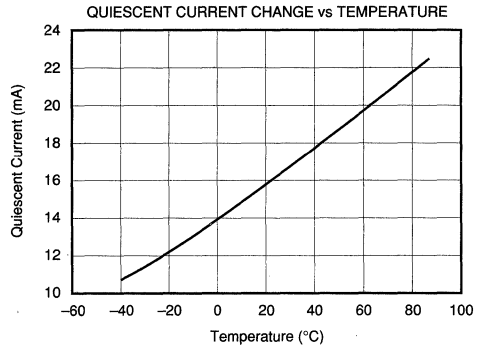
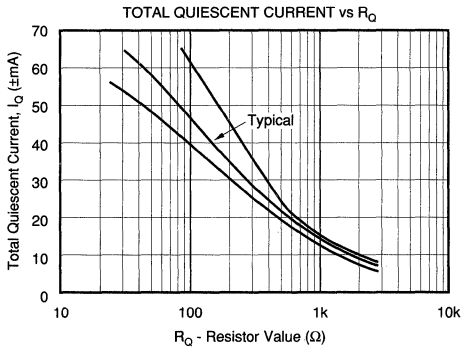
OPERATIONAL AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5V$, $R_O = 750\Omega$, and $T_A = +25^\circ C$ unless otherwise specified.



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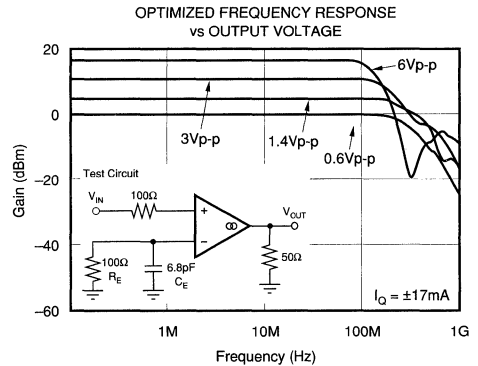
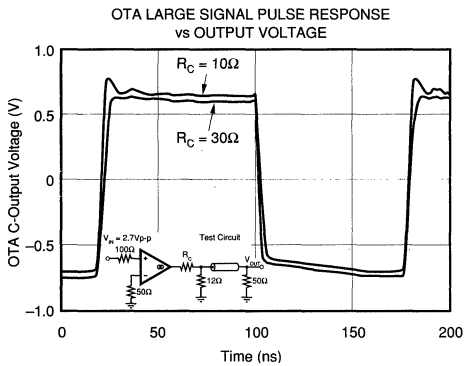
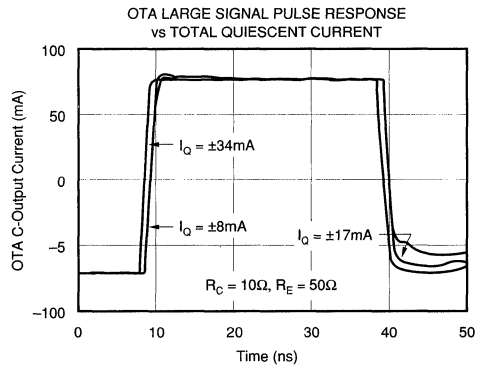
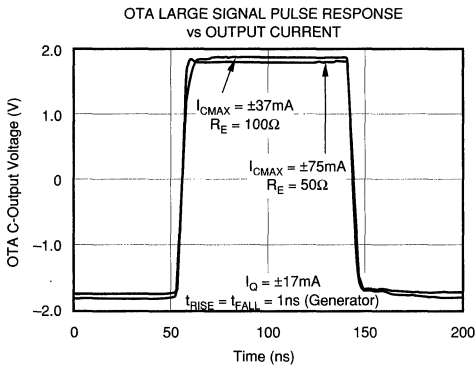
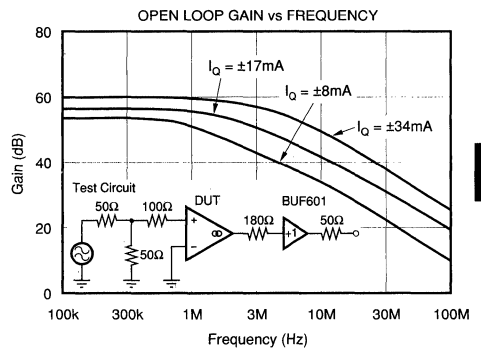
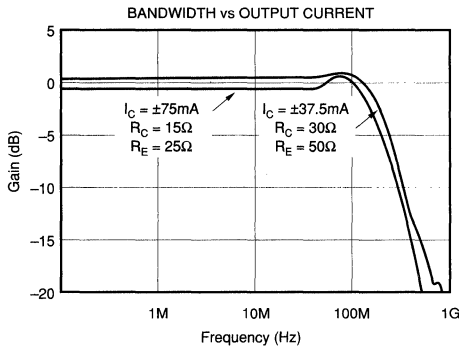
TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5V$, $R_O = 750\Omega$, $I_C = \pm 37.5mA$ ($R_E = 100\Omega$, $V_{IN} = 2.5Vp-p$), $I_C = \pm 75mA$ ($R_E = 50\Omega$, $V_{IN} = 2.5Vp-p$), and $T_{AMB} = +25^\circ C$ unless otherwise noted.

OPA2662

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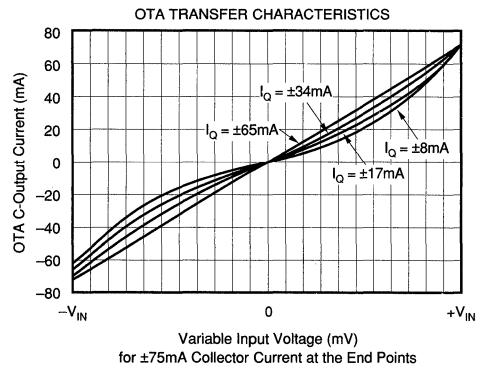
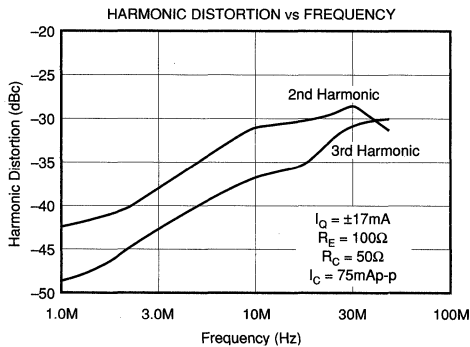
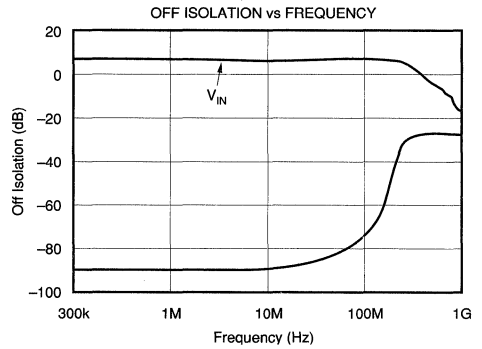
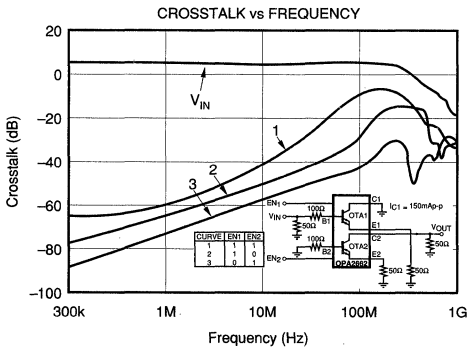
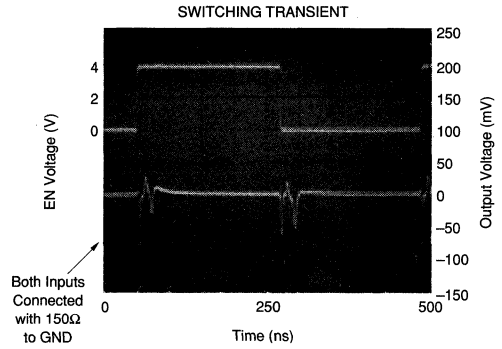
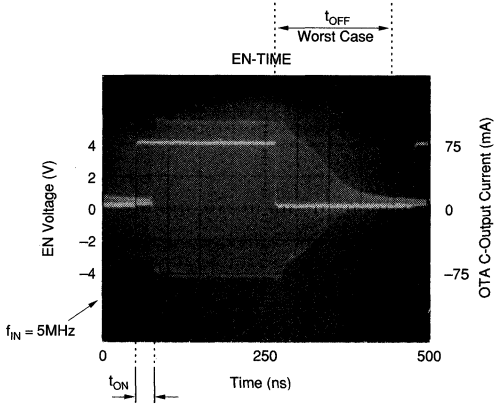
OPERATIONAL AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

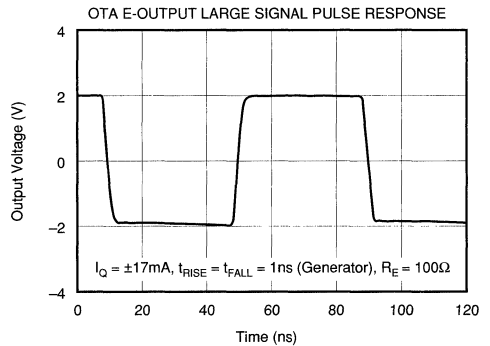
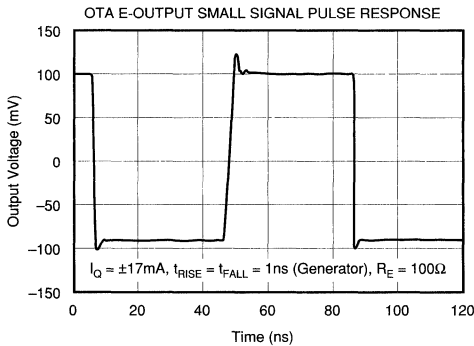
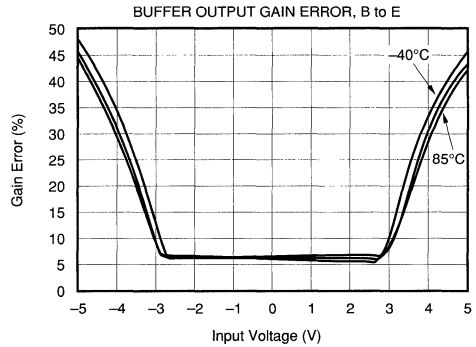
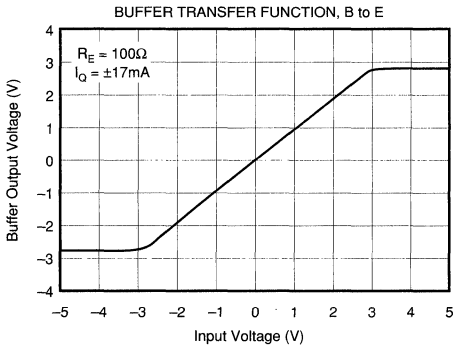
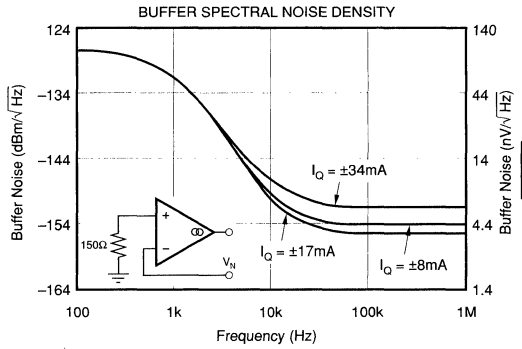
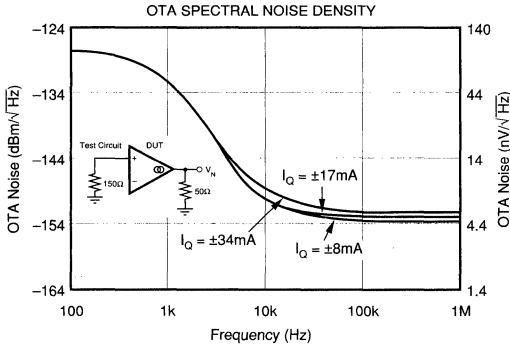
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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5V$, $R_O = 750\Omega$, ($R_E = 100\Omega$, $V_{IN} = 2.5V_{p-p}$), $I_C = \pm 75mA$ ($R_E = 50\Omega$, $V_{IN} = 2.5V_{p-p}$), and $T_A = +25^\circ C$ unless otherwise specified.



APPLICATION INFORMATION

The OPA2662 typically operates from $\pm 5V$ power supplies ($\pm 6V$ maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. All inputs of the OPA2662 are protected by internal diode clamps, as shown in the simplified schematic in Figure 1. These protection diodes can safely, continuously conduct 10mA (30mA peak). The input signal current must be limited if input voltages can exceed the power supply voltages by 0.7V, as can occur when power supplies are switched off and a signal source is still present. The buffer outputs E_1 and E_2 are not current-limited or protected. If these outputs are shorted to ground, high currents could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

DISCUSSION OF PERFORMANCE

OTA

The two OTA sections of the OPA2662 are versatile driver devices for wide-bandwidth systems. Applications best suited to this new circuit technology are those where the output signal is current rather than voltage. Such applications include driving LEDs, laser diodes, tuning coils, and driver transformers. The OPA2662 is also an excellent choice to drive the video heads of analog or digital video tape recorders in broadcast and HDTV-quality or video heads of high-density data recorders.

The symbol for the OTA sections is similar to that of a bipolar transistor. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor,

too, is a voltage-controlled current source. The three OTA terminals are labelled base (B), emitter (E) and collector (C), calling attention to its similarity to a transistor. The OTA sections can be viewed as wide-band, voltage-controlled, bipolar current sources. The collector current of each OTA is controlled by the differential voltage between the high-impedance base and low-impedance emitter. If a current flows at the emitter, then the current mirror reflects this current to the high-impedance collector by a fixed ratio of three. Thus, the collector is determined by the product of the base-emitter voltage times the transconductance times the current mirror factor. The typical performance curves illustrate the OTA open-loop transfer characteristic. Due to the PTAT (Proportional to Absolute Temperature) biasing, the transconductance is constant vs temperature and can be adjusted by an external resistor. The typical performance curves show the transfer characteristic for various quiescent currents. While similar to that of a transistor, this characteristic has one essential difference, as can be seen in the performance curve: the (sense) of the C output current. This current flows out of the C terminal for positive B-to-E input voltage and into for negative.

The OTAs offer many advantages over discrete transistors. First of all, they are self-biased and bipolar. The output current is zero for zero differential input voltage. AC inputs centered at zero produce an output current that is bipolar and centered at zero. The self-biased OTAs simplify the design process and reduce the number of components. It is far more linear than a transistor. The transconductance of a transistor is proportional to its collector current. But since the collector current is dependent upon the signal, it and the transconductance are fundamentally nonlinear. Like transistor circuits, OTA circuits may also use emitter degeneration

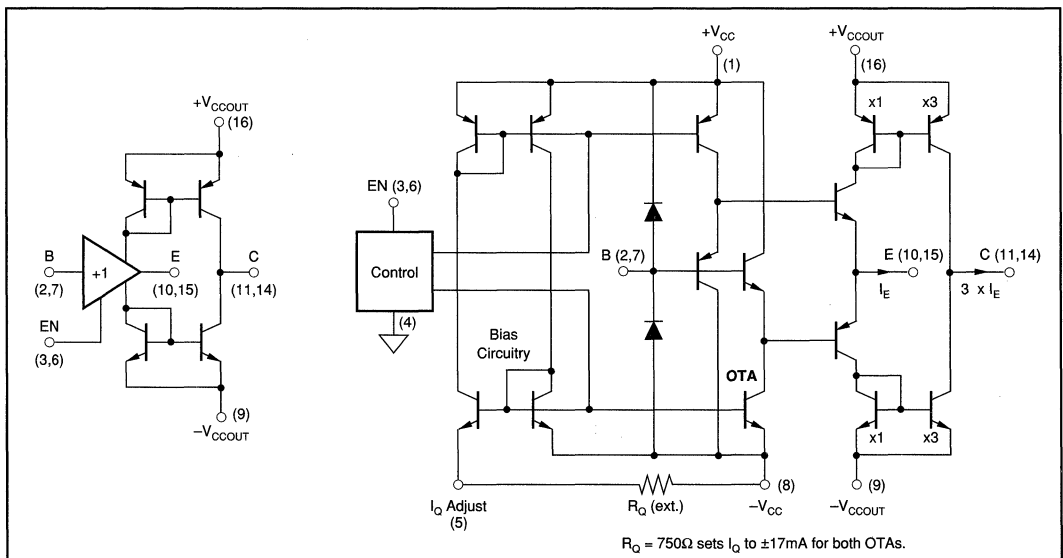


FIGURE 1. Simplified Block and Circuit Diagram.

to reduce the effect that offset voltages and currents might otherwise have on the DC operating point of the OTA. The E degeneration resistor may be bypassed by a capacitor to maintain high AC gain. Other cases may require a capacitor with less value to optimize high-frequency performance. The transconductance of the OTA with degeneration can be calculated by:

$$gm' = \frac{1}{\frac{1}{gm} + R_E}; gm = \frac{1}{r_E}$$

In application circuits, the resistor R_E between the E-output and ground is used to set the OTA transfer characteristic. The input voltage is transferred with a voltage gain of 1V/V to the E-output. According to the E-output impedance and the R_E resistor size a certain current flows to ground. As mentioned before this current is reflected by the current mirror to the high impedance collector output by a fixed ratio of three. Figure 2 and Figure 3 show the OTA transfer characteristic for a $R_E = 33\Omega$ and $R_E = 84\Omega$, which equal to voltage-to-current conversion factors (transconductance) of $\pm 75\text{mA/V}$ and $\pm 25\text{mA/V}$. The limitation for this transconductance adjustment is the maximum E-output current of $\pm 25\text{mA}$. The achievable transconductance and the corresponding minimum R_E versus the input voltage shows Figure 4. The area left to the $R_E + r_E$ curve can be used and results in a transconductance below the gm' curve. The variation of r_E vs total quiescent current is shown in the typical performance curve section.

$$I_C \approx 3 \cdot \frac{V_{IN}}{R_E + r_E}; R_E \approx \frac{3 \cdot V_{IN}}{I_C} - r_E$$

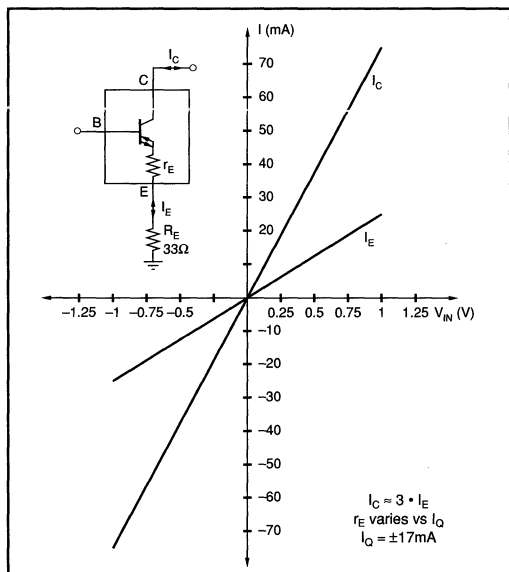


FIGURE 2. OTA Transfer Characteristic, $R_E = 33\Omega$.

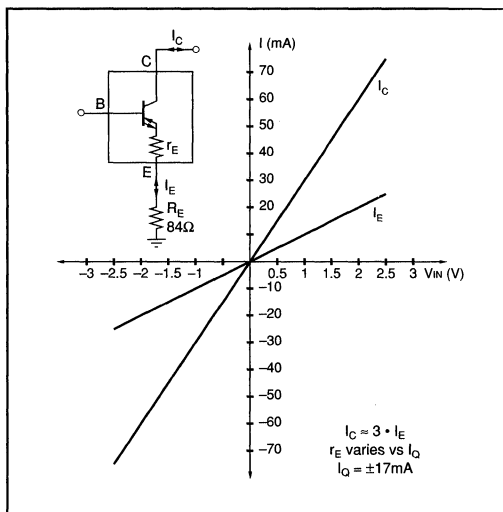


FIGURE 3. OTA Transfer Characteristic, $R_E = 84\Omega$.

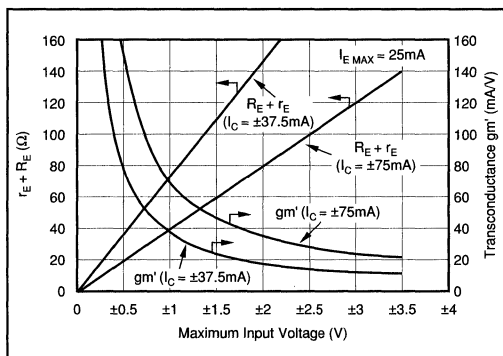


FIGURE 4. $R_E + r_E$ Selection Curve.

DISTORTION

The OPA2662's harmonic distortion characteristics into a 50Ω load are shown vs frequency in the typical performance curves for a total quiescent current of $\pm 17\text{mA}$ for both OTAs, which equals to $\pm 8.5\text{mA}$ for each of them.

The harmonic distortion performance is greatly affected by the applied quiescent current. In order to demonstrate this behavior Figure 5 illustrates the harmonic distortion performance vs frequency for a low quiescent current of $\pm 8\text{mA}$, for a medium of $\pm 17\text{mA}$ and for a high of $\pm 34\text{mA}$. It can be seen that the harmonic distortion decreases with all increasing quiescent current.

The same effect is expressed in other ways by the OTA transfer characteristics for different IQs in the typical performance curves.

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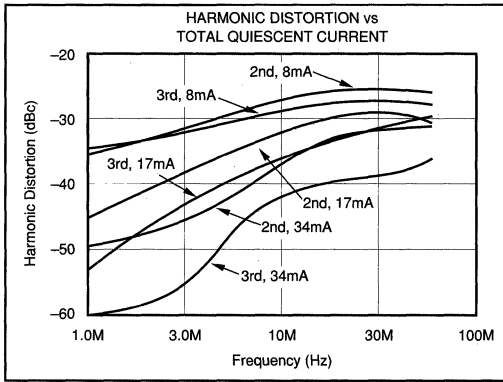


FIGURE 5. Harmonic Distortion.

BASIC CONNECTIONS

Shown in Figure 6 are the basic connections for the OPA2662's standard operation. Most of these connections are not shown in subsequent circuit diagrams for better clarification. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally the better choice. For further details see the "Circuit Layout" section.

ENABLE INPUTS

Switching stages compatible to TTL logic levels are provided for each OTA to switch the corresponding voltage-controlled current source on within 30ns, and off within

200ns at full output power ($I_{OUT} = \pm 75\text{mA}$). This enable feature allows multiplexing and demultiplexing, or a shut-down mode, when the device is not in use. If the EN-input is connected to ground or a digital "Low" is applied to it, the collector (C) and emitter (E) pins are switched in the high-impedance mode. When the EN-input is connected to +5V (+V_{CC}) or a digital "High" is applied to it, the corresponding OTA operates at the adjusted quiescent current. The initial setting for the enable pins is that they are connected to the positive supply as shown in Figure 6.

THERMAL CONSIDERATIONS

The performance of the OPA2662 is dependent on the total quiescent current which can be externally adjusted over a wide range. As shown later, the distortion will reduce when setting the OTAs for higher quiescent current. For a reliable operation, some thermal considerations should be made. The total power dissipation consists of two separate terms:

a) the quiescent power dissipation, P_{DQ}

$$P_{DQ} = |V_{CC}| \cdot I_Q^+ + |V_{CC}| \cdot I_Q^- \quad (1)$$

b) the power dissipation in the output transistors, P_{DO}

$$P_{DO} = (V_{OUT} - V_{CC}) \cdot I_{OUT} \quad (2)$$

Equations 1 and 2 can be used in conjunction with the OPA2662's absolute maximum rating of the junction temperature for a safe operation.

$$T_J = T_A + (P_{DQ} + P_{DO}) \cdot \theta_{JA} \quad (3)$$

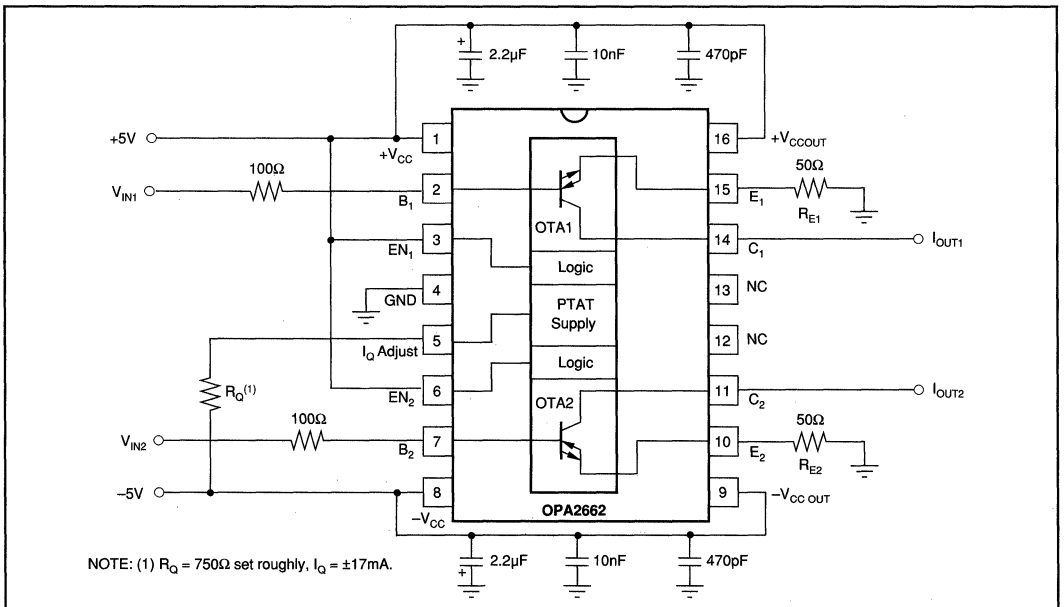


FIGURE 6. Basic Connections.

QUIESCENT CURRENT CONTROL

The quiescent current of the OPA2662 can be varied by connecting a user selectable external resistor, R_Q , between pin 5 and $-V_{CC}$. The quiescent current affects the operating currents of both OTA sections simultaneously, controlling the bandwidth and the AC-behavior as well as the transconductance. The typical performance curves illustrate the relationship of the quiescent current versus the R_Q and the transconductance, g_M . The OPA2662 is specified at a typical quiescent current of $\pm 17\text{mA}$. This is set by a resistor R_Q of 750Ω at 25°C ambient temperature. The useful range for the I_Q is from $\pm 3\text{mA}$ to $\pm 65\text{mA}$ (see Figure 7). The application circuits do not always show the resistor R_Q , but it is required for proper operation. With a fixed resistor, the quiescent current increases with increasing temperature, keeping the transconductance and AC-behavior constant. Figure 7 shows the internal current source circuitry. A resistor with a value of 150Ω is used to limit the current if pin 5 is shorted to $-V_{CC}$. This resistor has a relative accuracy of $\pm 25\%$ which causes an increasing deviation from the typical R_Q vs I_Q curve at decreasing R_Q values.

CIRCUIT LAYOUT

The high-frequency performance of the power operational transconductance amplifier OPA2662 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute musts. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately $2.2\mu\text{F}$); a parallel 470pF ceramic and a $10\mu\text{F}$ chip capacitor may be added if desired. Surface-mount types are recommended because of their low lead inductance.
- PC board traces for power lines should be wide to reduce impedance or inductance.
- Make short, low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.
- Sockets are not recommended because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance, surface-mounted components. Circuits using all surface-mount components with the OPA2662 will offer the best AC performance.
- A resistor (100Ω to 250Ω) in series with the high-impedance inputs is recommended to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Some applications may require a limitation for the maximum output current to flow. This can be achieved by adding a resistor (about 10Ω) between supply lines 1 and 16, and, 8 and 9 (see also Figure 8). The tradeoff of this technique is a reduced output voltage swing. This is due to the voltage drop across the resistors caused by both the collector and the emitter currents.

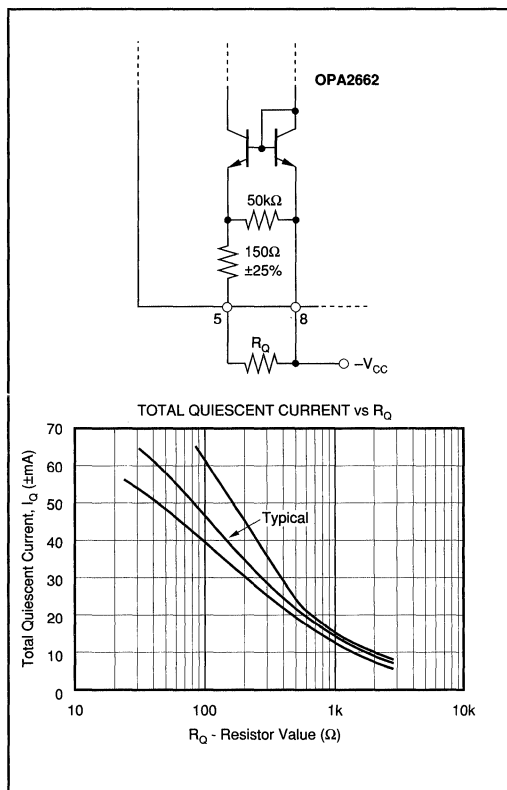


FIGURE 7. Quiescent Current Setting.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the OPA2662 to speed prototyping. This board allows fast and easy performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The complete AC characterization was performed with the same type. Figure 7 shows the schematic and Figure 8 the silkscreen and double-sided layout. Request DEM-OPA2662-1GC to test the operational amplifier in the 16-pin DIP package.

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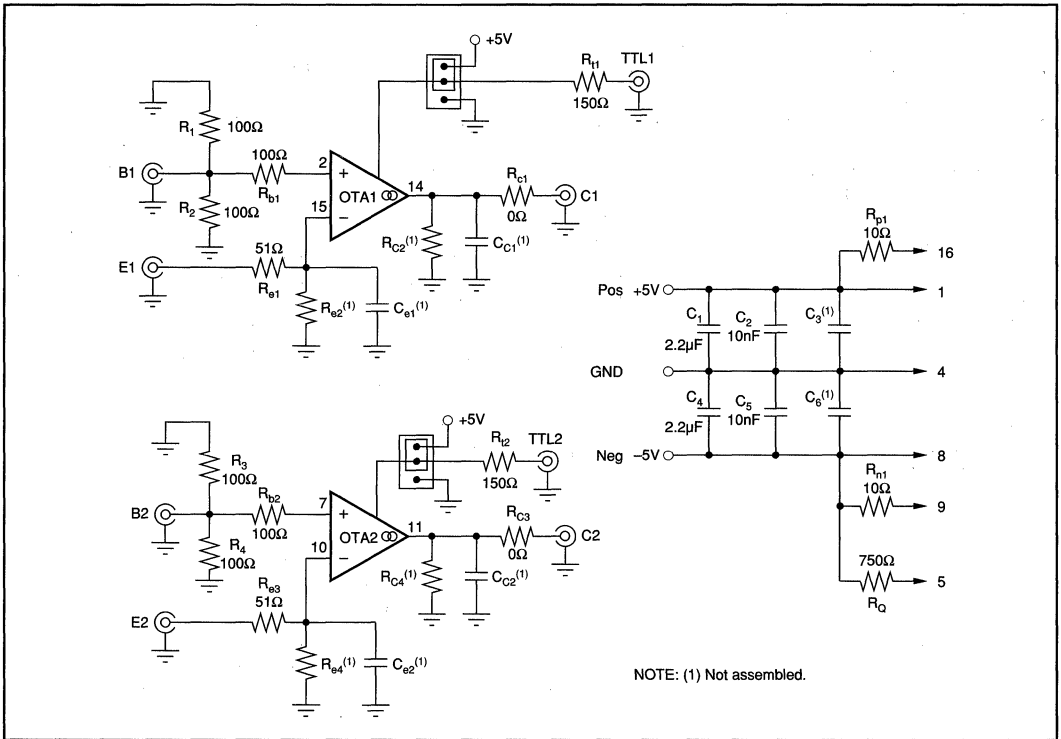


FIGURE 8. Circuit Schematic of the DEM-OPA2662-1GC.

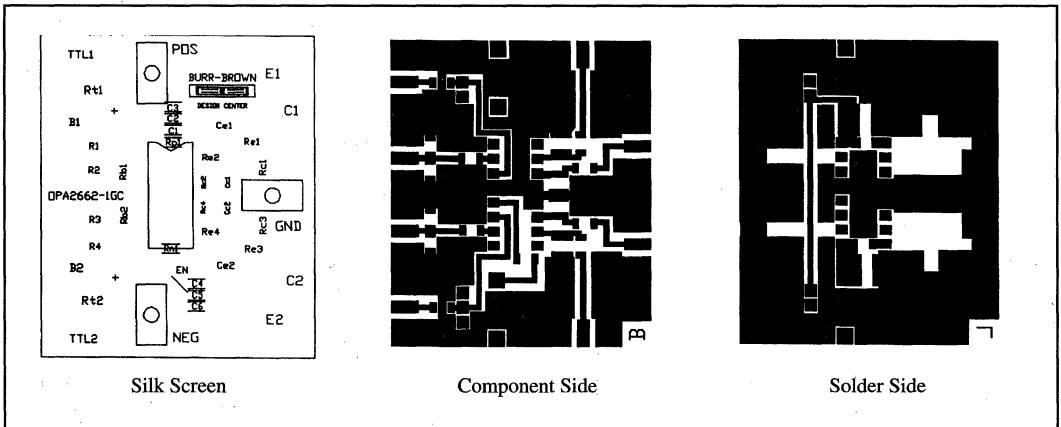


FIGURE 9. Silkscreen and Board Layouts of the DEM-OPA2662-1GC.

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TYPICAL APPLICATIONS

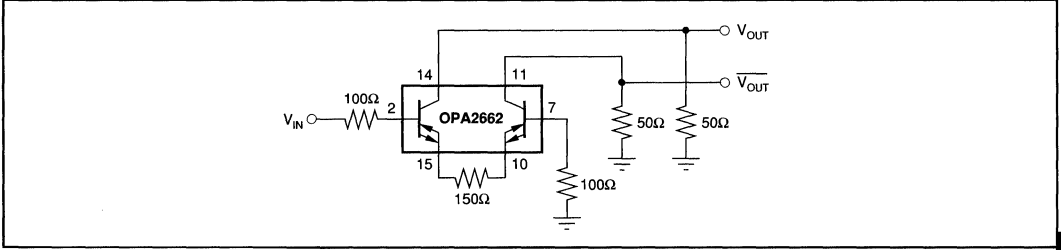


FIGURE 10. Single Ended to Differential Line Driver

OPA2662

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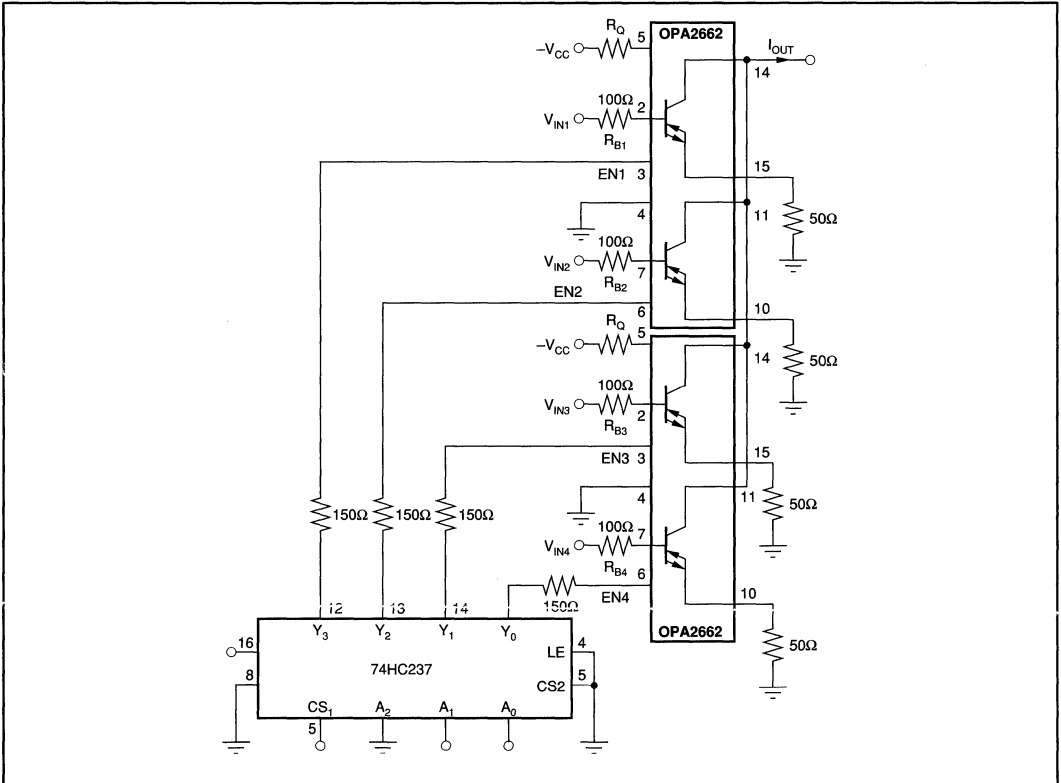


FIGURE 11. Current Distribution Multiplexer

OPERATIONAL AMPLIFIERS

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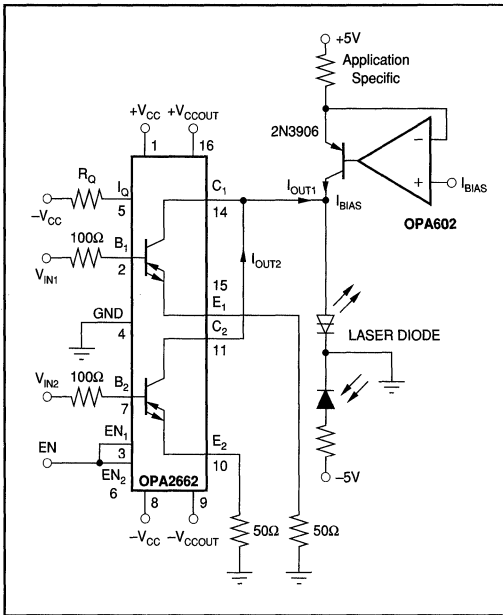


FIGURE 12. Laser Diode Driver.

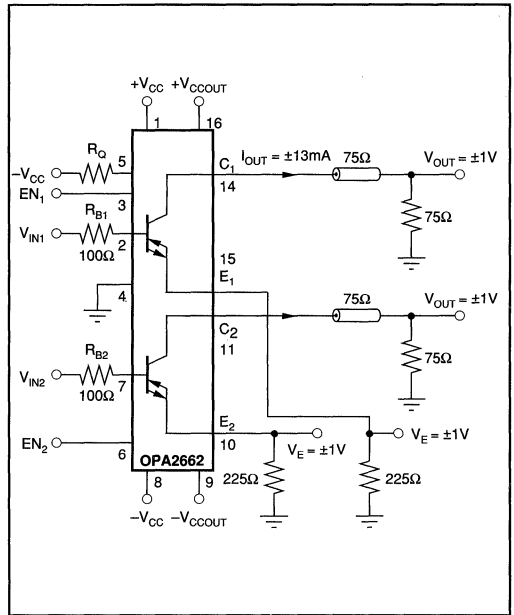


FIGURE 13. Two Channel Current Output Driver.

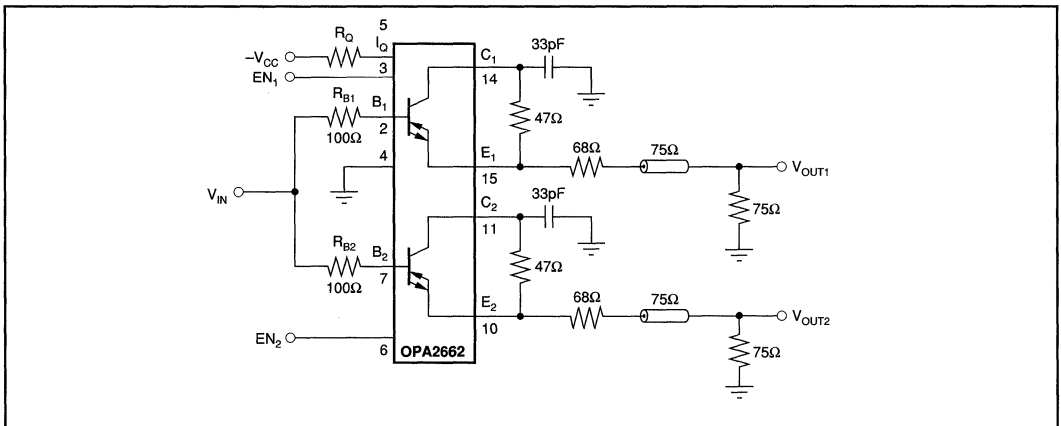


FIGURE 14. Direct Feedback Buffer and 1 to 2 Demultiplexer.

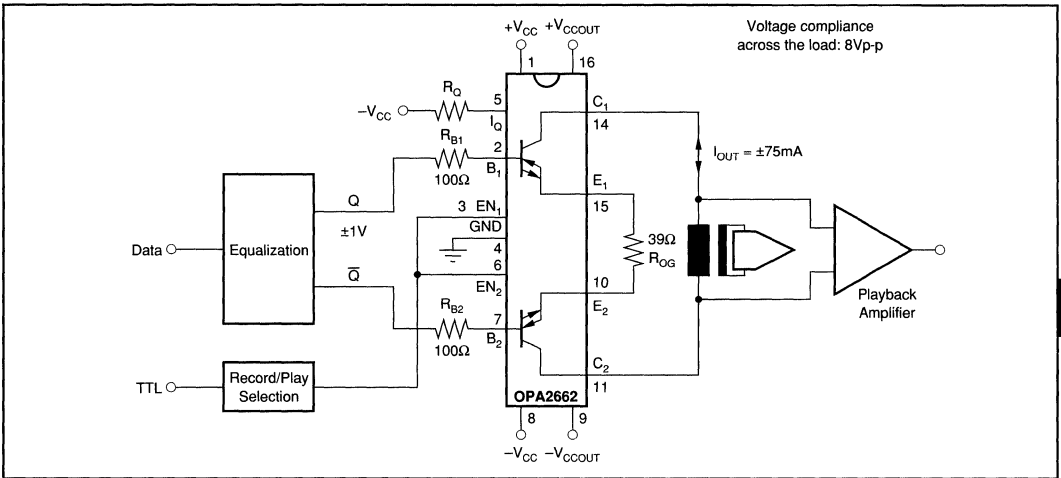


FIGURE 15. Analog/Digital Video Tape Record Amplifier.

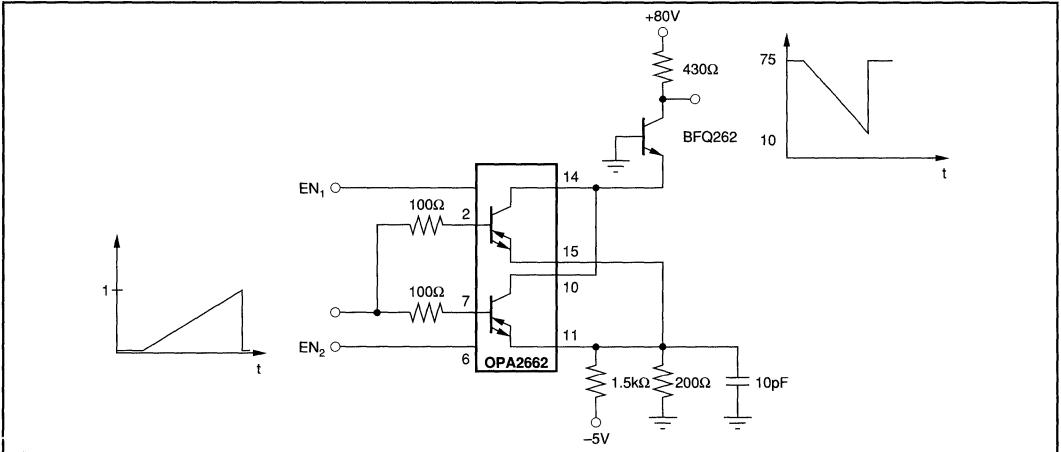


FIGURE 16. Cascode Stage Driver.

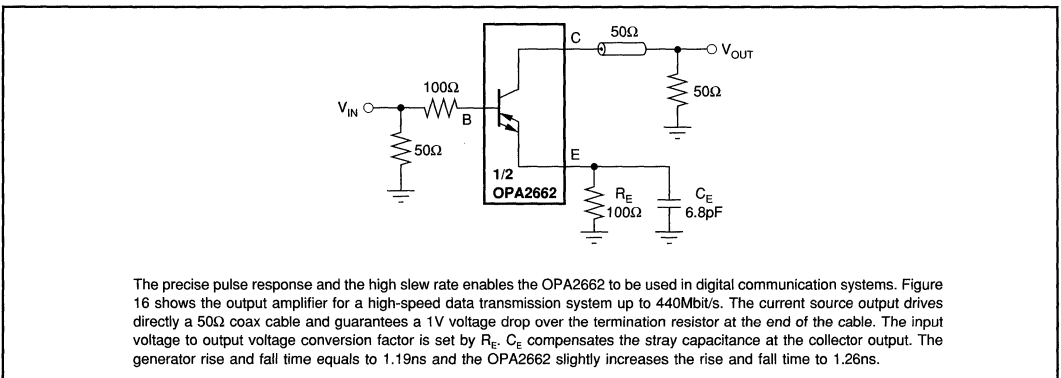


FIGURE 17. Driver Amplifier for a Digital 440Mbit/s Transmission System.

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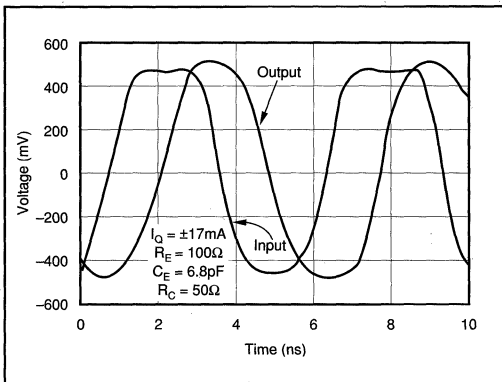


FIGURE 18. Pulse Response of the 400Mbit/s Line Driver.

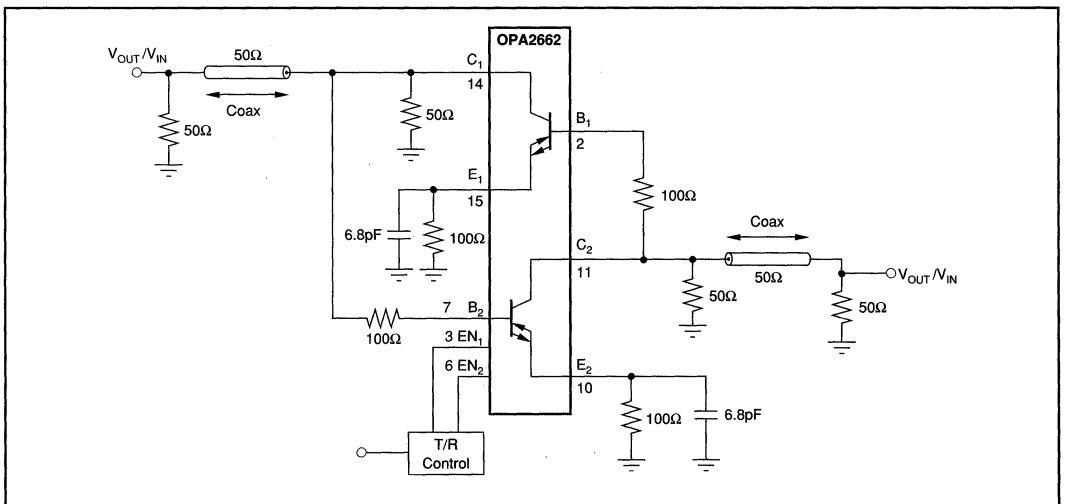


FIGURE 19. Bidirectional Line Driver.

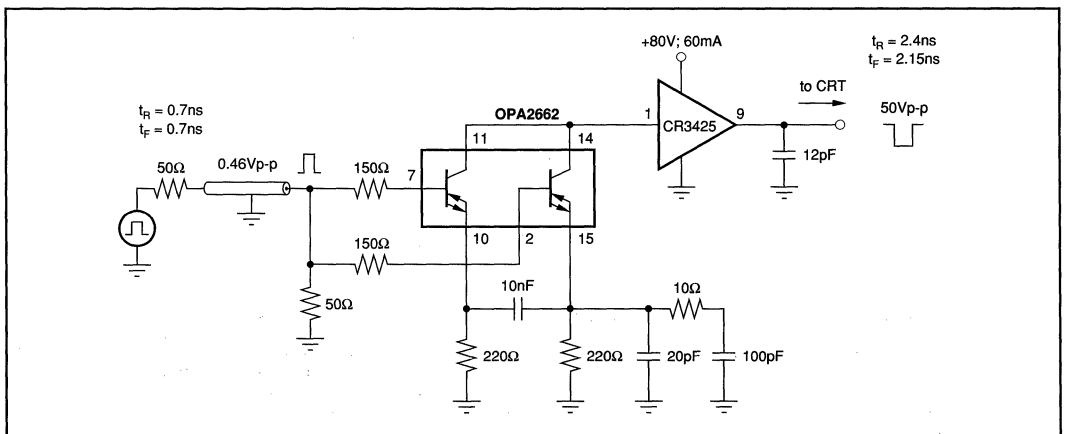
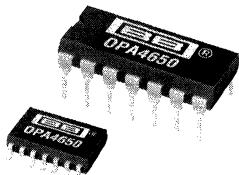


FIGURE 20. CRT Output Stage Driver for a 1600 X 1200 High-Resolution Graphic Monitor.

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OPA4650

PRELIMINARY INFORMATION
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Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- **LOW POWER:** 50mW PER AMP
- **UNITY GAIN STABLE BANDWIDTH:** 560MHz
- **FAST SETTling TIME:** 15ns to 0.01%
- **LOW INPUT BIAS CURRENT:** 2.7 μ A
- **DIFFERENTIAL GAIN/PHASE ERROR:** 0.01%/0.01°
- **PACKAGE:** 14-pin DIP and 14-pin SOIC

APPLICATIONS

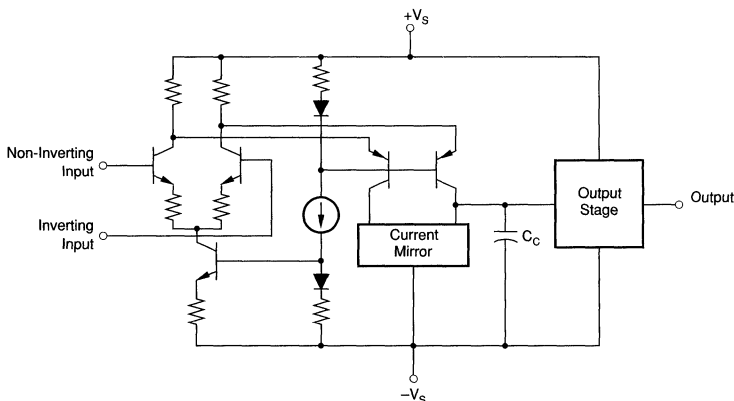
- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- ACTIVE FILTERS
- HIGH SPEED INTEGRATORS
- DIFFERENTIAL AMPLIFIER

DESCRIPTION

The OPA4650 is a quad, low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 560MHz as well as a 12-bit settling time of only 15ns. The low input bias current allows its use in high speed integrator applications, while the wide bandwidth and true differential input stage make it suitable for use in a variety of active filter applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA4650 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.

The OPA4650 is also available in single OPA650 and dual OPA2650 configurations.



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PDS-1267

2.445

OPA4650

OPERATIONAL AMPLIFIERS

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SPECIFICATIONS

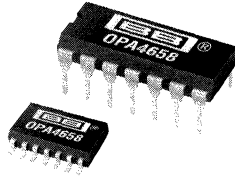
T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA4650P, U			OPA4650PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth ⁽²⁾	G = +1 G = +2 G = +5 G = +10 G = +1, 2V Step		900 700 40 80			* ⁽¹⁾ * * * *		MHz MHz MHz MHz
Slew Rate ⁽³⁾			1700			*		V/μs
At Minimum Specified Temperature			1500			*		V/μs
Rise Time	1 V Step		5.3			*		ns
Fall Time	1 V Step		5.9			*		ns
Settling Time 0.01%	G = +1, 2V Step		15			*		ns
0.1%	G = +1, 2V Step		11.5			*		ns
1%	G = +1, 2V Step		6			*		ns
Spurious Free Dynamic Range	G = +1, f = 5.0 MHz V _O = 2Vp-p, R _L = 402Ω		82			*		dBc
Differential Gain	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01 0.01	0.025 0.015		* *		% %
Differential Phase	G = +2, NTSC, V _O = 1.4Vp, R _L = 150Ω G = +2, NTSC, V _O = 1.4Vp, R _L = 400Ω		0.01 0.01	0.03 0.015		* *		Degrees Degrees
Gain Flatness	DC to 100MHz		0.1			*		dB
Bandwidth for 0.1dB of Flatness	G = +2		TBD			TBD		dB
Crosstalk	Input Referred, 5MHz, all hostile Input Referred, 5MHz, Channel-to-Channel		TBD TBD			* *		dB dB
OFFSET VOLTAGE								
Input Offset Voltage			±1	±3		±0.35	±1	mV
Average Drift			±5			3		μV/°C
Power Supply Rejection (+V _S) (-V _S)	V _S = ±4.5V to ±5.5V	50 45	70 55		60 48	* *		dB dB
INPUT BIAS CURRENT								
Input Bias Current	V _{CM} = 0V		2	6		*	4	μA
Over Temperature				8		*	6	μA
Input Offset Current	V _{CM} = 0V		0.4	1.5		*	*	μA
Over Temperature			0.9	3.0		*	*	μA
INPUT NOISE								
Input Voltage Noise						*		nV √Hz
Noise Density, f = 100Hz			23.2			*		nV √Hz
f = 10kHz			7.5			*		nV √Hz
f = 1MHz			7.1			*		nV √Hz
f = 10Hz to 100MHz			7.2			*		nV,rms
Voltage Noise, BW = 10Hz to 100MHz			72			*		μVp-p
Input Bias Current Noise						*		pA √Hz
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA √Hz
Noise Figure (NF)	R _S = 10kΩ R _S = 50Ω		3.0 19.0					dBm dBm
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±2.2	±2.8		*	*	V
Over-Specified Temperature			40	52		TBD	TBD	V
Common-Mode Rejection	V _{CM} = +2V							dB
INPUT IMPEDANCE								
Differential			15 1			*		kΩ pF
Common-Mode			16 1			*		MΩ pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V _O = ±2V, R _L = 100Ω	45	51		47	55		dB
Over Specified Temperature	V _O = ±2V, R _L = 100Ω	43	49		45	53		dB
OUTPUT								
Voltage Output						*	*	V
Over Specified Temperature	No Load R _L = 250Ω R _L = 100Ω	±2.5 ±2.2 ±2.0	±2.75 ±2.5 ±2.5		* * *	* * *		V V V
Current Output	+25°C to Max Temperature	±35	±50		±40	±55		mA
Over Specified Temperature		±25	±48		±30	±52		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +1		0.2			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*	*	V
Operating Voltage Range		±4.5		±5.5	*	*	*	V
Quiescent Current	All Channels		±21	±27		*	*	mA
Over Specified Temperature			±26	±31		*	*	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		-40		+85	*	*		°C
Thermal Resistance, θ _{JA}			120			*		°C/W
P			170			*		°C/W
U						*		°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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OPA4658

PRELIMINARY INFORMATION
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OPA4658

Wideband, Low Power Current Feedback OPERATIONAL AMPLIFIER

2

OPERATIONAL AMPLIFIERS

FEATURES

- UNITY GAIN BANDWIDTH: 900MHz
- LOW POWER: 47mW PER AMP
- LOW DIFF GAIN/PHASE ERRORS:
0.01%/0.01°
- HIGH SLEW RATE: 2000V/ μ s
- GAIN FLATNESS: 0.1dB TO 200MHz
- PACKAGE: 14-Pin DIP and 14-Pin SOIC

APPLICATIONS

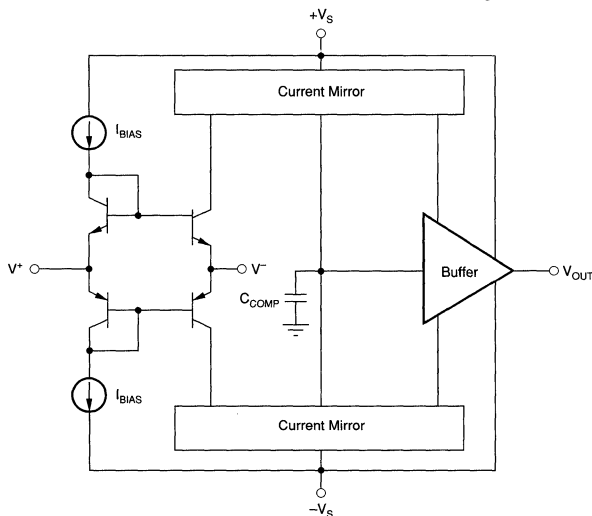
- MEDICAL IMAGING
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- COMMUNICATIONS
- PULSE AMPLIFIERS
- ADC/DAC GAIN AMPLIFIER
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER

DESCRIPTION

The OPA4658 is an ultra-wideband, low power current feedback video operational amplifier featuring a high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low

quiescent current make the OPA4658 a perfect choice for numerous video, imaging and communications applications.

The OPA4658 is internally compensated for unity-gain stability. The OPA4658 is also available in dual, OPA2658 and single, OPA658 configurations.



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PDS-1270

2.447

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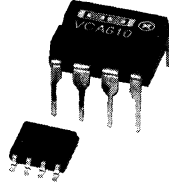
SPECIFICATIONS

TA = +25°C, VS = ±5V, RL = 100Ω, CL = 2pF unless otherwise noted.

PARAMETER	CONDITION	OPA4658P, U			OPA4658PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	G = +1		750			*(1)		MHz
	G = +2		700			*		MHz
	G = +5		320			*		MHz
	G = +10		195			*		MHz
Slew Rate ⁽²⁾	G = +1, 2 V Step		1700			*		V/μs
At Minimum Specified Temperature			1500			*		V/μs
Settling Time: 0.01%	G = +1, 2V Step		15			*		ns
0.1%	G = +1, 2V Step		11.5			*		ns
1%	G = +1, 2V Step		6			*		ns
Spurious Free Dynamic Range	f = 5MHz, G = +1, VO = 2Vp-p		75			*		dBc
	f = 20MHz, G = +1, VO = 2Vp-p		TBD			*		dBc
	f = 10MHz		TBD			*		dBm
Third-Order Intercept Point	G = +2, NTSC, VO = 1.4Vp-p, RL = 150Ω		0.025			*		%
Differential Gain	G = +2, NTSC, VO = 1.4Vp-p, RL = 400Ω		0.015			*		%
Differential Phase	G = +2, NTSC, VO = 1.4Vp-p, RL = 150Ω		0.03			*		degrees
	G = +2, NTSC, VO = 1.4Vp-p, RL = 400Ω		0.015			*		degrees
Gain Flatness	DC to 100 MHz		0.1			*		dB
Bandwidth for 0.1dB of Flatness	G = +2		TBD			TBD		MHz
Crosstalk	Input Referred, 5MHz, all hostile		TBD			*		dB
	Input Referred, 5MHz, Channel-to-Channel		TBD			*		dB
OFFSET VOLTAGE								
Input Offset Voltage			±5	±8		±3	±5	mV
Over Specified Temperature			±25			15		μV/°C
Power Supply Rejection (+Vs)	VS = ±4.5 to ±5.5V	50	70		60	*		dB
		45	55		48	*		dB
INPUT BIAS CURRENT								
Non-Inverting	VCM = 0V		TBD	TBD		*	*	μA
Over Temperature			TBD	TBD		*	*	μA
Inverting	VCM = 0V		TBD	TBD		*	*	μA
Over Temperature			TBD	TBD		*	*	μA
NOISE								
Input Voltage Noise Density	G = TBD					*	*	nV/√Hz
f = 100Hz			TBD			*	*	nV/√Hz
f = 1kHz			TBD			*	*	nV/√Hz
f = 10kHz			TBD			*	*	nV/√Hz
f = 1MHz			TBD			*	*	nV/√Hz
fB = 100Hz to 200MHz			TBD			*	*	μVrms
Inverting Input Bias Current						*	*	pA/√Hz
Noise Density: f = 10MHz			TBD			*	*	pA/√Hz
Non-Inverting Input Current						*	*	pA/√Hz
Noise Density: f = 10MHz			TBD			*	*	pA/√Hz
Noise Figure (NF)	RS = 1kΩ		TBD			*	*	dBm
	RS = 50Ω		TBD			*	*	dBm
INPUT VOLTAGE RANGE								
Common-mode Input Range		±2.5	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-mode Rejection	VCM = ±1V	57	62		75	85		dB
INPUT IMPEDANCE								
Differential			15 1			*		kΩ pF
Common-Mode			1.6 1			*		MΩ pF
OPEN-LOOP TRANSIMPEDANCE								
Open-loop Transimpedance	VO = ±2V, RL = 100Ω		TBD	TBD		TBD	TBD	kΩ
Over Specified Temperature	VO = ±2V, RL = 100Ω		TBD	TBD		TBD	TBD	kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±2.9		*	*		V
Over Specified Temperature		±2.5	±2.75		*	*		V
Voltage Output	RL = 250Ω	±2.7	±2.9		*	*		V
Over Specified Temperature		±2.5	±2.7		*	*		V
Voltage Output	RL = 100Ω	±2.2	±2.8		*	*		V
Over Specified Temperature		±2.0	±2.5		*	*		V
Current Output	+25°C to max Temperature	±40	±52		*	*		V
Over Specified Temperature		±30	±48		*	*		mA
Short Circuit Current			60		*	*		mA
Output Resistance	1MHz, G = +1		0.2		*	*		Ω
POWER SUPPLY								
Specified Operating Voltage		±4.5	±5	±5.5	*	*	*	V
Operating Voltage Range					*	*	*	V
Quiescent Current	All Channels		±19	±31		*	*	mA
Over Specified Temperature			±20	±34		*	*	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		-40		+85	*	*	*	°C
Thermal Resistance, θJA			120			*	*	°C/W
P			170			*	*	°C/W
U						*	*	°C/W

NOTES: (1) An asterisk (*) specifies the same value as the grade to the left. (2) Slew rate is rate of change from 10% to 90% of output voltage step.

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VCA610

VCA610

2

OPERATIONAL AMPLIFIERS

WIDEBAND VOLTAGE CONTROLLED AMPLIFIER

FEATURES

- WIDE GAIN CONTROL RANGE: 80dB
- SMALL PACKAGE: 8-pin SOIC or DIP
- WIDE BANDWIDTH: 30MHz
- LOW VOLTAGE NOISE: $2.2\text{nV}/\sqrt{\text{Hz}}$
- FAST GAIN SLEW RATE: $300\text{dB}/\mu\text{s}$
- EASY TO USE

DESCRIPTION

The VCA610 is a wideband, continuously variable, voltage controlled gain amplifier. It provides linear-dB gain control with op amp style, high impedance inputs. It is designed to be used as a flexible gain control element in a variety of electronic systems.

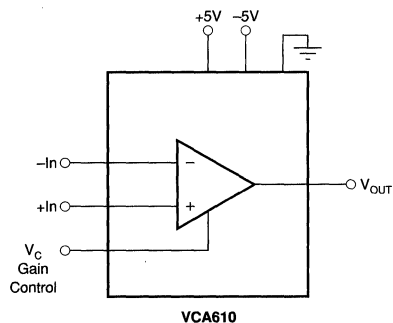
The VCA610 has a gain control range of 80dB (-40dB to +40dB) providing both gain and attenuation for maximum flexibility in a small 8-pin SOIC or plastic dual-in-line package. The broad attenuation range can be used for gradual or controlled channel turn-on and turn-off for applications in which abrupt gain changes can create artifacts or other errors. In addition, the output can be disabled to provide -80dB of attenuation. Group delay variation with gain is typically less than $\pm 2\text{ns}$ across a bandwidth of 1 to 15MHz.

The VCA610 has a noise figure of 3.5dB (with an R_s of 200Ω) including the effects of both current and voltage noise, $1.4\text{pA}/\sqrt{\text{Hz}}$ and $2.2\text{nV}/\sqrt{\text{Hz}}$ respectively. Instantaneous output dynamic range is 70dB for gains of 0dB to +40dB with 1MHz noise bandwidth. The output is capable of driving 100Ω . The high speed, $300\text{dB}/\mu\text{s}$, gain control signal is an easy to generate unipolar voltage that varies the gain linearly in dB/V.

APPLICATIONS

- ULTRASOUND
- AGC AMPLIFIER
- ANALYTICAL INSTRUMENTATION
- SONAR
- ACTIVE FILTERS
- LOG AMPLIFIER
- IF CIRCUITS
- CCD CAMERAS

The VCA610 is designed with a very fast overload recovery time of only 200ns. This allows a large signal transient to overload the output at high gain, without obscuring low-level signals following closely behind. The excellent overload recovery time and distortion specifications optimize this device for low-level doppler measurements.



SPECIFICATIONS

ELECTRICAL

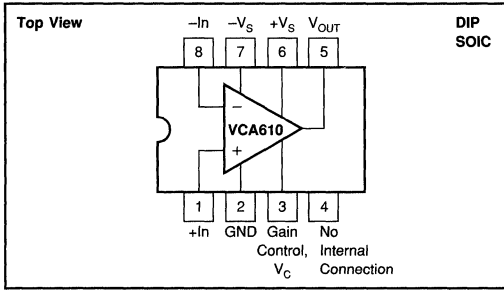
All specifications at $V_S = \pm 5\text{VDC}$, $R_L = 500\Omega$, $R_S = 0\Omega$, and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	VCA610AP, AU			UNITS
		MIN	TYP	MAX	
INPUT NOISE Input Voltage Noise Input Current Noise Noise Figure	$G = +40\text{dB}$, $R_S = 0\Omega$ $G = -40\text{dB}$ to $+40\text{dB}$ $G = +40\text{dB}$, $R_S = 200\Omega$		2.2 1.4 3.5		$\text{nV}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ dB
INPUT Input Impedance Bias Current Offset Current Differential Voltage Range Common-Mode Voltage Range Common-Mode Rejection	Common-Mode All Gains All Gains		1 1 6 2 (1)		$\text{M}\Omega$ pF μA μA
GAIN Specified Gain Range Gain Accuracy, (2) Gain Accuracy Temperature Drift Gain with Output Disabled	$-40\text{dB} \leq G \leq +40\text{dB}$ $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ $+0.1\text{V} \leq V_O \leq +2.0\text{V}$, $f = 1\text{MHz}$	-40	± 0.5 ± 0.01 -80	+40 ± 2	dB dB $\text{dB}/^\circ\text{C}$ dB
GAIN CONTROL Gain Scaling Factor Control Voltage (V_C) Bandwidth Slew Rate Settling Time: 1% Input Impedance Input Bias Current Output Offset Change(3)	$-40\text{dB} \leq G \leq +40\text{dB}$ $G = -40\text{dB}$ ($V_C = 0\text{V}$) to $+40\text{dB}$ ($V_C = -2\text{V}$) -3dB 80dB Gain Step $V_{IN} = 10\text{mVDC}$, $\Delta G = 80\text{dB}$	0	40 1 300 800 1 1 2	-2	dB/V V MHz $\text{dB}/\mu\text{s}$ ns $\text{M}\Omega$ pF μA mV
FREQUENCY RESPONSE Bandwidth, Small-Signal Bandwidth, Large-Signal Group Delay Variation 0dB $\leq G \leq +40\text{dB}$ -40dB $\leq G < 0\text{dB}$ Output Slew Rate Overload Recovery(4) Two-tone Intermodulation Distortion(5) Two-tone, 3rd Order IMD Intercept(6)	-3dB, All Gains $V_O = 1\text{Vp-p}$, $G \geq 0\text{dB}$ $f = 1$ to 15MHz $f = 1$ to 15MHz $V_O = 1\text{Vp-p}$ Small-Signal Small-Signal		30 25 ± 1 ± 2 60 200 -50 15	± 2 ± 3	MHz MHz ns ns V/ μs ns dBc dBm
OUTPUT Voltage Swing(1) $G = +40\text{dB}$ $G = 0\text{dB}$ Output Voltage Limit Short-Circuit Current Instantaneous Dynamic Range (IDR)(6) $G = 0\text{dB}$ to $+40\text{dB}$ Offset Output Resistance	Continuous to Common $V_O = 1.5\text{Vp-p}$ $G = -40\text{dB}$ $f = 1\text{MHz}$, All Gains	2 1	3 1.5 Symmetrical to Ground ($\pm 10\%$) ± 80 70 ± 10 10	± 30	Vp-p Vp-p mA dB mV Ω
POWER SUPPLY Specification Operation PSR Quiescent Current	$\pm 5\text{VDC}$ Recommended Output Referred, $f = 100\text{kHz}$	± 4.5 ± 4 40	50 26	± 5.5 ± 6 32	VDC VDC dB mA
TEMPERATURE Specification Operation θ_{JA} AP AU	Applies to Temperature Drift Specs	-25 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

NOTES: (1) See Input/Output Range discussion in Applications Information Section (Figure 2). (2) Gain is laser trimmed and tested over the -40dB to $+40\text{dB}$ gain range; $V_{IN} = 1\text{Vp-p}$ for gains less than 0dB ; $V_{OUT} = 1\text{Vp-p}$ for gains of 0dB to $+40\text{dB}$. (3) Output offset change from offset at $G = -40\text{dB}$. (4) Gain = $+40\text{dB}$; input step of 2V to 2mV ; time required for output to return from saturation to linear operation. (5) $V_{IN} = 7\text{mVp-p}$, $V_{OUT} = 700\text{mVp-p}$ (250mVrms); Output Power = $-10\text{dBm}/\text{tone}$, equal amplitude tones of $5\text{MHz} \pm 50\text{Hz}$, $G = +40\text{dB}$. See typical performance curves. (6) With $R_S = 0\Omega$, and noise bandwidth of 1MHz . $\text{IDR} = 20 \log (V_{\text{ORMS}}/(\theta_{\text{ORMS}} \times \sqrt{\text{BW}}))$; where V_{ORMS} is rms output voltage, θ_{ORMS} is output noise spectral density, and BW is noise bandwidth.

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PIN CONFIGURATION



ORDERING INFORMATION

MODEL	PACKAGE
VCA610AP	8-pin Plastic DIP
VCA610AU	8-pin Plastic SOIC

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VCA610AP	8-pin Plastic DIP	006
VCA610AU	8-pin Plastic SOIC	182

NOTE:(1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply	±7V
Differential Input Voltage	Total V _s
Input Voltage Range	See Input Protection Section
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, DIP, 10s)	+300°C
Lead Temperature (soldering, SOIC, 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature (T _j)	+175°C

VCA610

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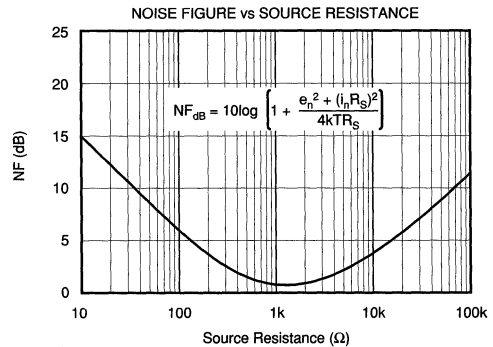
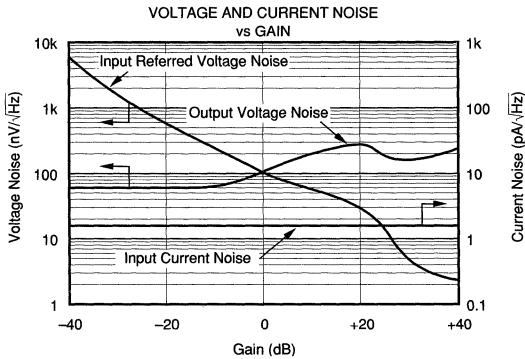
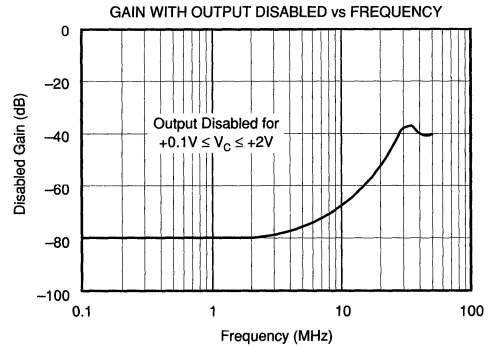
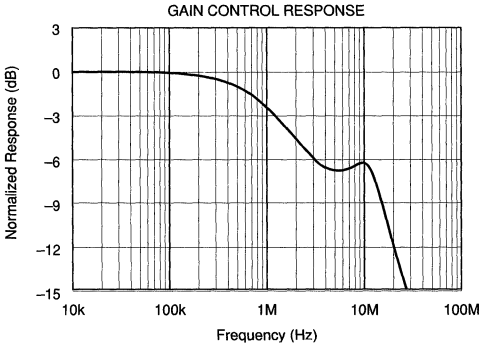
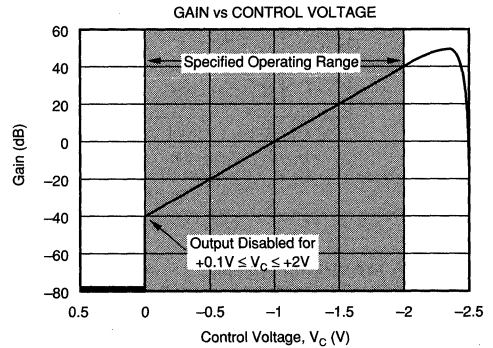
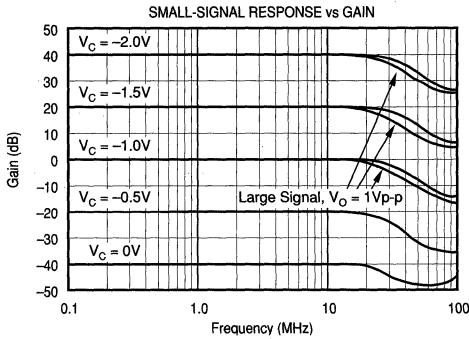
OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES

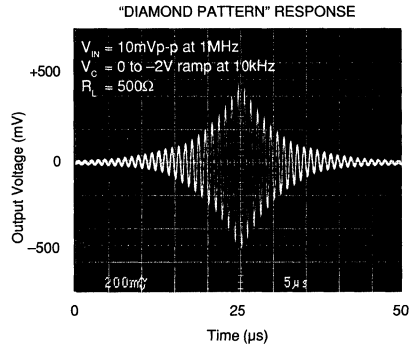
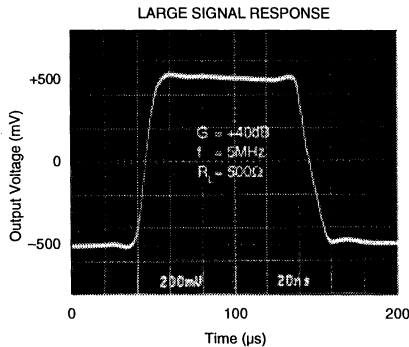
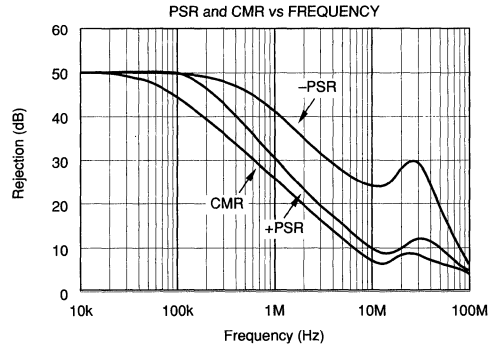
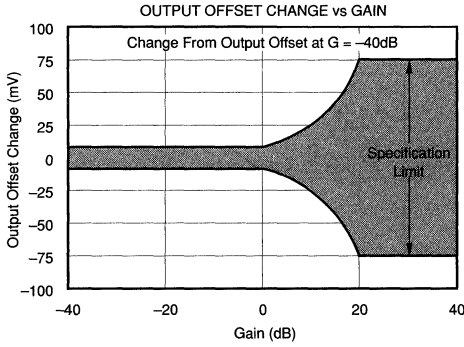
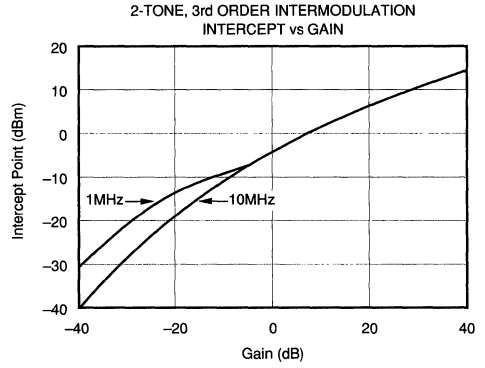
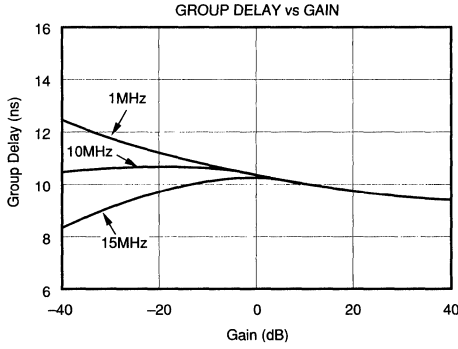
At $V_S = \pm 5\text{VDC}$, $R_L = 500\Omega$, $R_S = 0\Omega$, and $T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_S = \pm 5VDC$, $R_L = 500\Omega$, $R_S = 0\Omega$, and $T_A = +25^\circ C$ unless otherwise noted.



VCA610
2
OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

CIRCUIT DESCRIPTION

The VCA610 is a wideband voltage amplifier having a voltage-controlled gain, as modeled in Figure 1. The circuit's basic voltage amplifier responds to the control of an internal gain control amplifier. At its input, the voltage amplifier presents the high impedance of a differential stage, permitting termination freedom in impedance matching. To preserve termination options, no internal circuitry connects to the input bases of this differential stage. For this reason, the user should provide DC return paths to ground for the input base currents either through a grounded termination resistor or a direct connection to ground. The differential input stage also permits rejection of common-mode signals to remove ground bounce effects. At its output, the voltage amplifier presents the low impedance of class A-B emitter-follower stage, again simplifying impedance matching. An open-loop design produces wide bandwidth at all gain levels and avoids the added overload-recovery and propagation delays of feedback designs. Repeated use of differential stages minimizes offset effects for reduced feedthrough of the gain control signal. A ground-sensing, differential to single-ended converter retains the low offset in the amplifier output stage.

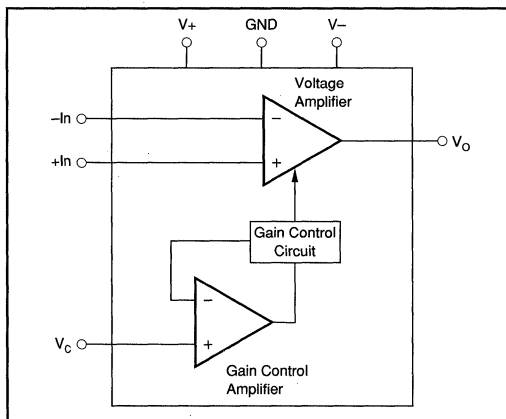


FIGURE 1. Block Diagram of the VCA610.

A user-applied voltage, V_c , controls the amplifier's gain magnitude through a high-speed control circuit. Gain polarity can be either inverting or noninverting depending upon the amplifier input driven by the input signal. Use of the inverting input is recommended since this connection tends to minimize positive feedback from the output to the non-inverting input. The gain control circuit presents the high input impedance of a noninverting op amp connection.

Control voltage V_c varies the amplifier gain according to the exponential relationship $G(V/V) = 10^{-2(V_c+1)}$. This translates to the linear, logarithmic relationship $G(\text{dB}) = -40 - 40V_c$. Thus, $G(\text{dB})$ varies linearly over the specified -40dB to

+40dB range as V_c varies from 0 to -2V. Optionally, making V_c slightly positive, $\geq 0.1V$, effectively disables the amplifier, producing 80dB of attenuation.

Internally, the gain control circuit varies the amplifier gain through a time-proven method which exploits the linear relationship between the transconductance, g_m , of a bipolar transistor and the transistor's bias current. Varying the bias currents of differential stages varies g_m to control the voltage gain of the VCA610. Relying on transistor g_m to set gain also avoids the need for a noise-producing gain-set resistor in the amplifier input circuit. This reliance normally introduces a high thermal sensitivity to the gain. However, the VCA610 employs specialized analog signal processing that removes this thermal effect.

INPUT/OUTPUT RANGE

The VCA610's 80dB gain range allows the user to handle an exceptionally wide range of input signal levels. If the unit's input and output voltage range specifications are exceeded, however, signal distortion and amplifier overloading will occur. The VCA610's maximum input and output voltage range is best illustrated in Figure 2.

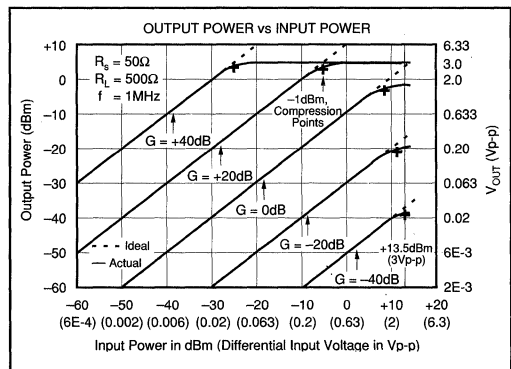


FIGURE 2. Input and Output Range.

Figure 2 plots output power vs input power for five voltage gains spaced at 20dB intervals. The 1dBm compression points occur where the actual output power (solid lines) deviates by -1dBm from the ideal output power (dashed lines). Compression is produced by different mechanisms depending on the selected gain. For example, at $G = -40\text{dB}$, 1dBm compression occurs when the input signal approaches approximately 3Vp-p (13.5dBm for $R_s = 50\Omega$). Input overloading is the compression mechanism for all gains from -40dB to about -5dB. For gains between -5dB and +5dB, the compression is due to internal gain stage overloading. Compression over this gain range occurs when the output signal becomes distorted as internal gain stages become overdriven. At $G = 0\text{dB}$, 1dBm compression occurs when the input exceeds approximately 1.5Vp-p (7.5dBm). At gains greater than about 5dB, the compression mechanism is due to output stage overloading. Output overloading occurs

when either the maximum output voltage swing or output current is exceeded. The VCA610's high output current of $\pm 80\text{mA}$ insures that virtually all output overloads will be limited by voltage swing rather than by current limiting. At $G = +40\text{dB}$, 1dBm compression occurs when the output voltage approaches 3Vp-p (3.5dBm for $R_L = 500\Omega$). Table I below summarizes these results.

GAIN RANGE	OUTPUT COMPRESSION MECHANISM	TO PREVENT OPERATE WITHIN
$-40\text{dB} < G < -5\text{dB}$	Input Stage Overload	Input Voltage Range
$-5\text{dB} < G < +5\text{dB}$	Internal Stages Overloading	Output Voltage Range
$+5\text{dB} < G < +40\text{dB}$	Output Stage Overload	Output Voltage Range

TABLE I. Output Signal Compression.

WIRING PRECAUTIONS

Maximizing the VCA610's capability requires some wiring precautions and high-frequency layout techniques. In general, printed circuit board conductors should be as short and as wide as possible to provide low resistance, low impedance signal paths. Stray signal coupling from the output or power supplies to the inputs should be minimized. Unused inputs should be grounded as close to the package as possible.

Low impedance ground returns for signal and power are essential. Proper supply bypassing is also extremely critical and must *always* be used. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors ($1\mu\text{F}$ to $10\mu\text{F}$) with very short leads are recommended. Surface mount bypass capacitors will provide excellent results due to their low lead inductance.

OVERLOAD RECOVERY

As shown in Figure 2, the onset of overload occurs whenever the actual output begins to deviate from the ideal expected output. If possible, the user should operate the VCA610 within the linear regions shown in order to minimize signal distortion and overload delay time. However, instances of amplifier overload are actually quite common in Automatic Gain Control (AGC) circuits which involve the application of variable gain to signals of varying levels. The VCA610's design incorporates circuitry which allows it to recover from most overload conditions in 200ns or less. Overload recovery time is defined as the time required for the output to return from overload to linear operation following the removal of either an input or gain control overdrive signal.

OFFSET ADJUSTMENT

Where desired, the offset of the VCA610 can be removed as shown in Figure 3. This circuit simply presents a DC voltage to one of the amplifier's inputs to counteract the offset error voltage. For best offset performance, the trim adjustment should be made with the amplifier set at the maximum gain of the intended application. The offset voltage of the VCA610 varies with gain, limiting the complete offset cancellation to

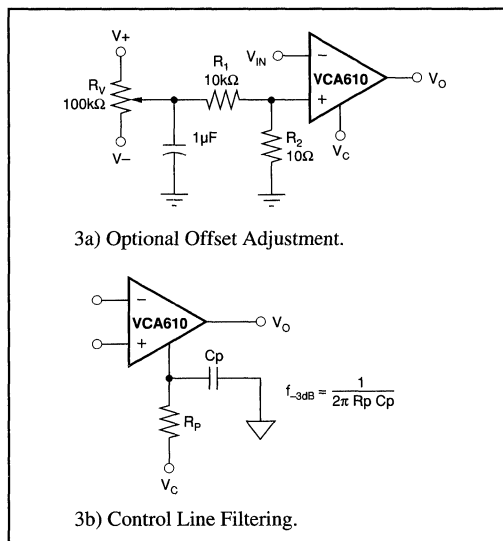


FIGURE 3. Optional Offset Adjustment and Control Line Filtering.

one selected gain. Selecting the maximum gain optimizes offset performance for higher gains where high amplification of the offset effects produces the greatest output offset. Two features minimize the offset control circuit's noise contribution to the amplifier input circuit. First, making the resistance of R_2 a low value minimizes the noise directly introduced by the control circuit. This reduces both the thermal noise of the resistor and the noise produced by the resistor with the amplifier's input noise current. A second noise reduction results from capacitive bypass of the potentiometer output. This filters out power supply noise that would otherwise couple to the amplifier input.

This filtering action would diminish as the wiper position approaches either end of the potentiometer but practical conditions prevent such settings. Over its full adjustment range, the offset control circuit produces a $\pm 5\text{mV}$ offset correction for the values shown. However, the VCA610 only requires one tenth of this range for offset correction, assuring that the potentiometer wiper will always be near the potentiometer center. With this setting, the resistance seen at the wiper remains high and this stabilizes the filtering function.

GAIN CONTROL

The VCA610's gain is controlled by means of a unipolar negative voltage applied between ground and the gain control input, pin 3. If use of the output disable feature is required, a ground-referenced bipolar voltage is needed. Output disable occurs for $+0.1\text{V} \leq V_c \leq +2\text{V}$, and produces 80dB of attenuation. The control voltage should be limited to $+2\text{V}$ in disable mode, and -2V in the gain mode in order to prevent saturation of internal circuitry.

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The VCA610's gain control input has a -3dB bandwidth of 1MHz and varies with frequency as shown in the Typical Performance Curves. This wide bandwidth, although useful for many applications, can allow high frequency noise to modulate the gain control input. In practice, this can be easily avoided by filtering the control input as shown in Figure 3b. R_p should be no greater than 100Ω so as not to introduce gain errors by interacting with the gain control's input bias current of $2\mu\text{A}$.

INPUT PROTECTION

Electrostatic damage (ESD) has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The VCA610 incorporates on-chip ESD protection diodes as shown in Figure 4. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

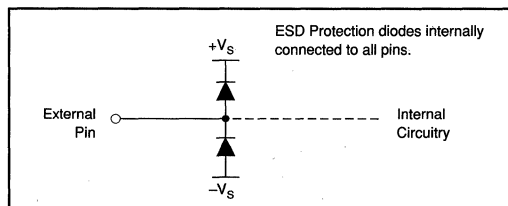


FIGURE 4. Internal ESD Protection.

All pins on the VCA610 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the pin voltage exceeds either power supply by about 0.7V . This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and provides adequate ESD protection for most normal handling procedures. However, static protection is strongly recommended since static damage can cause subtle changes in amplifier operational characteristics without necessarily destroying the device.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM-VCA610AP-C for 8-pin DIP.

APPLICATIONS

The electronically variable gain of the VCA610 suits pulse-echo imaging systems well. Such applications include medical imaging, non-destructive structural inspection and sonar.

The amplifier's variable gain also serves AGC amplifiers, amplitude-stabilized oscillators, log amplifiers and exponential amplifiers. The discussions below present examples of these applications.

ULTRASOUND TGC AMPLIFIER

The Figure 5 block diagram illustrates the fundamental configuration common to pulse-echo imaging systems. A piezoelectric crystal serves as both the ultrasonic pulse generator and the echo monitor transducer. A transmit/receive (T/R) switch isolates the monitor amplifier from the crystal during the pulse generation cycle and, then, connects the amplifier to the crystal during the echo monitor cycle.

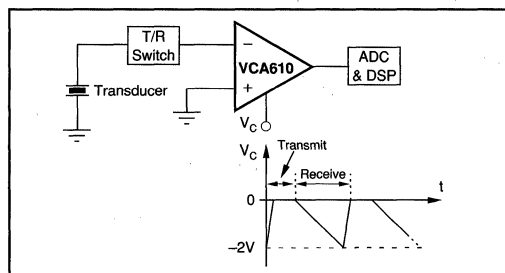


FIGURE 5. Typical Ultrasound Application.

During the monitor (receive) cycle, the control voltage V_c varies the amplifier gain. The gain is varied for three basic signal processing requirements of a transducer array based beamformer: compensation for depth attenuation effects, sometimes called Time Gain Compensation (TGC); receive apodization or windowing for reducing side lobe energy; and dynamic aperture sizing for better near field resolution.

Time gain compensation increases the amplifier's gain as the ultrasound signal moves through the material to compensate for signal attenuation versus material depth. For this purpose, a ramp signal applied to the VCA610 gain control input linearly increases the dB gain of the VCA610 with time. The gain control provides signal apodization or windowing with transducer arrays connected to amplifier arrays. Selective weighting of amplifier gains across the transducer aperture suppresses side lobe effects in the beamformer output to reduce image artifacts. Gain controlled attenuation or disabling the amplifier can be used to dynamically size the array aperture for better near field resolution. The controlled attenuation of the VCA610 minimizes switching artifacts and eliminates the bright radial rings that can result. The VCA610's 80dB gain range accommodates these functions.

WIDE-RANGE LOW-NOISE VCA

Figure 6 combines two VCA610s in series, extending the overall gain range and improving noise performance. This combination produces a gain equal to the sum of the two amplifier's logarithmic gains for a composite range of

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-80dB to +80dB. Simply connecting V_{C1} and V_{C2} to the same 0 to -2V gain control voltage can produce this range, however, separate control voltages for the two amplifiers offer a noise performance improvement. In that configuration, each amplifier separately controls one half the gain range in a manner that always holds G_1 at the maximum level possible.

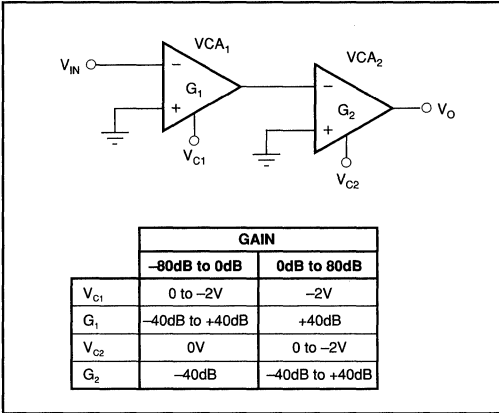


FIGURE 6. Two Series Connected VCA610s Expand the Gain Range and Improve Noise Performance.

At higher gains, variation of V_{C2} alone makes VCA₂ provide all of the gain control, leaving the gain of VCA₁ fixed at its maximum of 40dB. This gain maximum corresponds to the maximum bias currents in VCA₁, minimizing this amplifier's noise. Thus, for composite circuit gains of 0dB to +80dB, V_{CA1} serves as a low-noise, fixed-gain preamp.

For lower composite gains, VCA₁ provides the gain control and VCA₂ acts as a fixed attenuator. There, variation of V_{C1} varies G_1 from -40dB to +40dB while V_{C2} remains fixed at 0V for $G_2 = -40$ dB. This mode produces the -80dB to 0dB segment of the compositic gain range.

WIDE-RANGE AGC AMPLIFIER

The voltage-controlled gain feature of the VCA610 makes this amplifier ideal for precision AGC applications with control ranges as large as 60dB. The AGC circuit of Figure 7 adds an op amp and diode for amplitude detection, a holding capacitor to store the control voltage and resistors R_1 through R_3 that determine attack and release times. Resistor R_3 and capacitor C_C phase compensate the AGC feedback loop. The op amp compares the positive peaks of output V_O with a DC reference voltage V_R . Whenever a V_O peak exceeds V_R , the OPA620 output swings positive, forward biasing the diode and charging the holding capacitor. This drives the capacitor voltage in a positive direction, reducing the amplifier gain. R_3 and the C_H largely determine the attack time of this AGC correction.

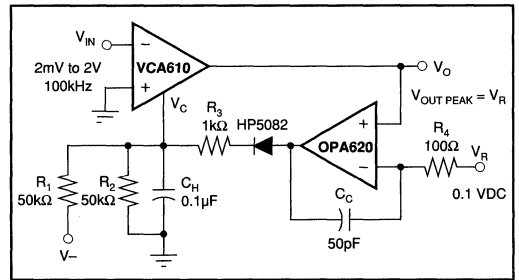


FIGURE 7. This AGC Circuit Maintains a Constant Output Amplitude for a 1000:1 Input Range.

Between gain corrections, resistor R_1 charges the capacitor in a negative direction, increasing the amplifier gain. R_1 , R_2 and C_H determine the release time of this action. Resistor R_2 forms a voltage divider with R_1 , limiting the maximum negative voltage developed on C_H . This limit prevents input overload of the VCA610's gain control circuit.

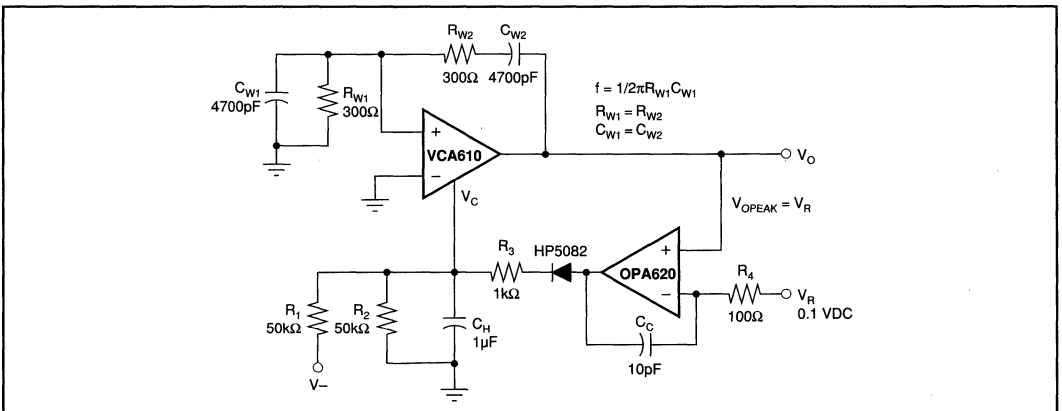


FIGURE 8. Adding Wein-bridge Feedback to the AGC Circuit of Figure 7 Produces an Amplitude Stabilized Oscillator.

STABILIZED WEIN-BRIDGE OSCILLATOR

Adding Wein-bridge feedback to the above AGC amplifier produces an amplitude-stabilized oscillator. Shown in Figure 8, this alternative requires the addition of just two resistors (R_{W1} , R_{W2}) and two capacitors (C_{W1} , C_{W2}).

Connecting the feedback network to the amplifier's noninverting input introduces positive feedback to induce oscillation. The feedback factor displays a frequency dependence due to the changing impedances of the C_w capacitors. As frequency increases, the decreasing impedance of the C_{w2} increases the feedback factor. Simultaneously, the decreasing impedance of the C_{w1} decreases this factor.

Analysis shows that the maximum factor occurs at $f = 1/2\pi R_w C_w$, making this the frequency most conducive to oscillation. At this frequency the impedance magnitude of C_w equals R_w and inspection of the circuit shows that this condition produces a feedback factor of 1/3. Thus, self-sustaining oscillation requires a gain of three through the amplifier. The AGC circuitry establishes this gain level. Following initial circuit turn on, R_1 begins charging C_H negative, increasing the amplifier gain from its minimum. When this gain reaches three, oscillation begins at $f = 1/2\pi R_w C_w$ and R_1 's continued charging effect makes the oscillation amplitude grow. This growth continues until that amplitude reaches a peak value equal to V_R . Then, the AGC circuit counteracts the R_1 effect, controlling the peak amplitude at V_R by holding the amplifier gain at a level of three. Making V_R an AC signal, rather than a DC reference, produces amplitude modulation of the oscillator output.

LOW-DRIFT WIDEBAND LOG AMP

The VCA610 can be used to provide a 250kHz (-3dB) log amp with low offset voltage and low gain drift.

The exponential gain control characteristic of the VCA610 permits simple generation of a temperature-compensated logarithmic response. Enclosing the exponential function in an op amp feedback path inverts this function, producing the log response. Figure 9 shows the practical implementation of this technique. A DC reference voltage, V_R , sets the VCA610 inverting input voltage. This makes the amplifier's output voltage $V_{OA} = -GV_R$ where $G = 10^{-2(V_C + 1)}$.

A second input voltage also influences V_{OA} through control of gain G . The feedback op amp forces V_{OA} to equal the input voltage V_{IN} connected at the op amp inverting input. Any difference between these two signals drops across R_3 , producing a feedback current that charges C_C . The resulting change in V_{OL} adjusts the gain of the VCA610 to change V_{OA} . At equilibrium, $V_{OA} = V_{IN} = -V_R 10^{-2(V_C + 1)}$. The op amp forces this equality by supplying the gain control voltage $V_C = R_1 V_{OL} / (R_1 + R_2)$. Combining the last two expressions and solving for V_{OL} yields the circuit's logarithmic response.

$$V_{OL} = - (1 + R_2/R_1) [1 + 0.5 \text{LOG} (-V_{IN}/V_R)]$$

Examination of this result illustrates several circuit characteristics. First, the argument of the Log term, $-V_{IN}/V_R$, reveals an option and a constraint. In Figure 9, V_R represents

a DC reference voltage. Optionally, making this voltage a second signal produces log-ratio operation. Either way, the Log term's argument constrains the polarities of V_R and V_{IN} . These two voltages must be of opposite polarities to ensure a positive argument. This polarity combination results when V_R connects to the inverting input of the VCA610. Alternately, switching V_R to this amplifier's noninverting input removes the minus sign of the log term's argument. Then, both voltages must be of the same polarity to produce a positive argument. In either case, the positive polarity requirement of the argument restricts V_{IN} to a unipolar range.

The above V_{OL} expression reflects a circuit gain introduced by the presence of R_1 and R_2 . This feature adds a convenient scaling control to the circuit. However, a practical matter sets a minimum level for this gain. The voltage divider formed by R_1 and R_2 attenuates the voltage supplied to the V_C terminal by the op amp. This attenuation must be great enough to prevent any possibility of an overload voltage at the V_C terminal. Such an overload saturates the VCA610's gain control circuitry, reducing the amplifier's gain. For the feedback connection of Figure 9, this overload condition permits a circuit latch. To prevent this, choose R_1 and R_2 to ensure that the op amp can not possibly deliver more than 2.5V to the V_C terminal.

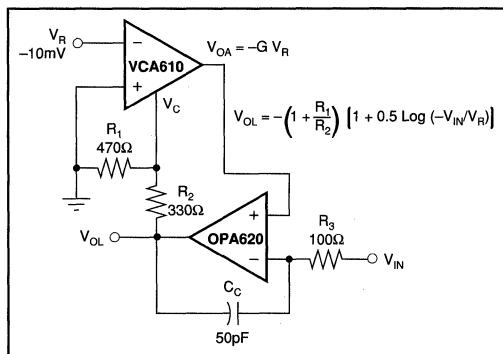


FIGURE 9. Driving the Gain Control Pin of the VCA610 with a Feedback Amplifier Produces a Temperature-Compensated Log Response.

LOW-DRIFT WIDEBAND EXPONENTIAL AMP

A common use of the Log amp above involves signal companding. The inverse function, signal expanding, requires an exponential transfer function. The VCA610 produces this latter response directly as shown in Figure 10. DC reference V_R again sets the amplifier's input voltage and the input signal V_{IN} now drives the gain control point. Resistors R_1 and R_2 attenuate this drive to prevent overloading the gain control input. Setting these resistors at the same values as in the preceding Log amp produces an exponential amplifier with the inverse function of the Log amp.

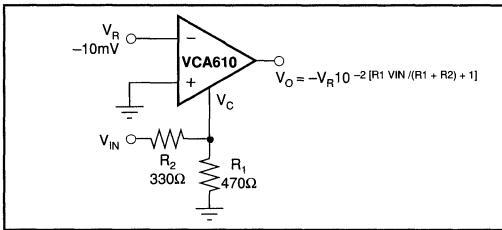


FIGURE 10. Signal Drive of the VCA610 Gain Control Pin Produces and Exponential Response, Re-expanding Signal Comped by Figure 9.

VOLTAGE-CONTROLLED LOW-PASS FILTER

In the circuit of Figure 11, the VCA610 serves as the variable gain element of a voltage-controlled low-pass filter. As will be described, this implementation expands the circuit's voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit's response pole responds to control voltage V_C according to the relationship $f_p = G/2\pi R_2 C$ where $G = 10^{-2(V_C + 1)}$. With the components shown, the circuit provides a linear variation of the low-pass cutoff from 300Hz to 1MHz.

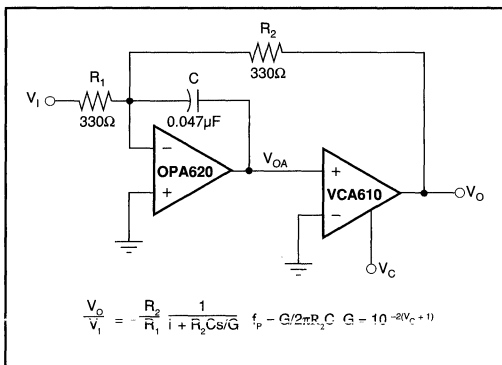


FIGURE 11. This Voltage-Tuneable Low-Pass Filter Produces a Variable Cutoff Frequency with a 3,000:1 Range.

The response control results from amplification of the feedback voltage applied to R_2 . Consider first the case where the VCA610 produces $G = 1$. Then, the circuit performs as if this amplifier were replaced by a short circuit. Visually doing so leaves a simple voltage amplifier with a feedback resistor bypassed by a capacitor. This basic circuit produces a response pole at $f_p = 1/2\pi R_2 C$.

For $G > 1$, the circuit applies a greater voltage to R_2 , increasing the feedback current this resistor supplies to the summing junction of the OPA620. The increased feedback current produces the same result as if R_2 had been decreased in value in the basic circuit described above. Decreasing the effective R_2 resistance moves the circuit's pole to a higher frequency, producing the $f_p = G/2\pi R_2 C$ response control.

Finite loop gain and a signal swing limitation set performance boundaries for the circuit. Both limitations occur when the VCA610 attenuates rather than amplifies the feedback signal. These two limitations reduce the circuit's utility at the lower extreme of the VCA610's gain range. For $-1 \leq V_C \leq 0$, this amplifier produces attenuating gains in the range from 0dB to -40dB. This directly reduces the net gain in the circuit's feedback loop, increasing gain error effects. Also, this attenuation transfers an output swing limitation from the OPA620 output to the overall circuit's output. Note that OPA620 output voltage, V_{OA} , relates to V_O through the expression $V_O = G V_{OA}$. Thus, a $G < 1$ limits the maximum V_O swing to a value less than the maximum V_{OA} swing.

However, the circuit shown provides greater output swing than the more common multiplier implementation. The latter replaces the VCA610 of the figure with an analog multiplier having a response of $V_O = XY/10$. Then, $X = V_{OA}$ and $Y = V_C$, making the circuit output voltage $V_O = V_{OA} V_C/10$. Thus, the multiplier implementation amplifies V_{OA} by a gain of $V_C/10$. Circuit constraints require that $V_C \leq 10$, making this gain ≤ 1 . Thus, the multiplier performs only as a variable attenuator and never provides amplification. As a result, the voltage swing limitation of V_{OA} restricts the V_O swing throughout most of the circuit's control range. Replacing the multiplier with the VCA610 shown permits equivalent gains greater > 1 . Then, operating the VCA610 with gains in the range of one to 100 avoids the reduction in output swing capability.

VOLTAGE-CONTROLLED HIGH-PASS FILTER

A circuit analogous to the above low-pass filter produces a voltage-controlled high-pass response. The gain control provided by the VCA610 of Figure 12 varies this circuit's response zero from 1Hz to 10kHz according to the relationship $f_z \approx 1/2\pi G R_1 C$ where $G = 10^{-2(V_C + 1)}$.

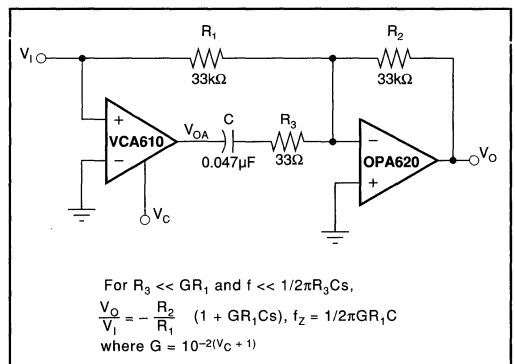


FIGURE 12. A Voltage-Tuneable High-Pass Filter Produces a Response Zero Variable from 1Hz to 10kHz.

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To visualize the circuit's operation, consider a circuit condition and an approximation that permit replacing the VCA610 and R_3 with short circuits. First consider the case where the VCA610 produces $G = 1$. Then, replacing this amplifier with short circuit leaves the operation unchanged. In this shorted state, the circuit is simply a voltage amplifier with an R-C bypass around R_1 . The resistance of this bypass, R_3 , serves only to phase compensate the circuit and practical factors make $R_3 \ll R_1$. Neglecting R_3 for the moment, the circuit becomes just a voltage amplifier with capacitive bypass of R_1 . This circuit produces a response zero at $f_z = 1/2\pi R_1 C$.

Adding the VCA610 as shown permits amplification of the signal applied to capacitor C and produces voltage control of the frequency f_z . Amplified signal voltage on C increases the signal current conducted by the capacitor to the op amp feedback network. The result is the same as if C had been increased in value to GC. Replacing C with this effective capacitance value produces the circuit's control expression $f_z = 1/2\pi R_1 GC$.

Two factors limit the high-frequency performance of the resulting high-pass filter. The finite bandwidth of the op amp and the circuit's phase compensation produce response poles. These limit the frequency duration of the high-pass response. Selecting the R_3 phase compensation with the equation $R_3 = \sqrt{(R_1/2\pi f_c C)}$ assures stability for all values of G and sets the circuit's bandwidth at $BW = \sqrt{(f_c/2\pi R_1 C)}$. Here, f_c is the unity-gain crossover frequency of the op amp used. With the components shown, $BW = 100\text{kHz}$. This bandwidth provides a high-pass response duration of five decades of frequency for $f_z = 1\text{Hz}$, dropping to one decade for $f_z = 10\text{kHz}$.

The output voltage limit of the VCA610 imposes an input voltage limit for the filter. The expression $V_{OA} = GV_I$ relates these two voltages. Thus, an output voltage limit V_{OAL} constrains the input voltage to $V_I \leq V_{OAL}/G$.

VOLTAGE-CONTROLLED BAND-PASS FILTER

The VCA610's variable gain also provides voltage control over the center frequency of a band-pass filter. Shown in Figure 13, this filter follows from the state-variable configuration with the VCA610 replacing the inverter common to that configuration. Variation of the VCA610 gain moves the filter's center frequency through a 100:1 range following the relationship $f_o = [10^{-V_C + 1}] / 2\pi RC$.

As before, variable gain controls a circuit time constant to vary the filter response. The gain of the VCA610 amplifies or attenuates the signal driving the lower integrator of the circuit. This alters the effective resistance of the integrator time constant producing the response

$$\frac{V_o}{V_i} = \frac{-s/nRC}{s^2 + s/nRC + G/R^2C^2}$$

Evaluation of this response equation reveals a passband gain of $A_o = -1$, a bandwidth of $BW = 1/2\pi nRC$ and a selectivity of $Q = n10^{-V_C + 1}$. Note that variation of control voltage V_C alters Q but not bandwidth.

The gain provided by the VCA610 restricts the output swing of the filter. Output signal V_o must be constrained to a level that does not drive the VCA610 output, V_{OA} , into its saturation limit. Note that these two outputs have voltage swings related by $V_{OA} = GV_o$. Thus, a swing limit V_{OAL} imposes a circuit output limit of $V_{OL} \leq V_{OAL}/G$.

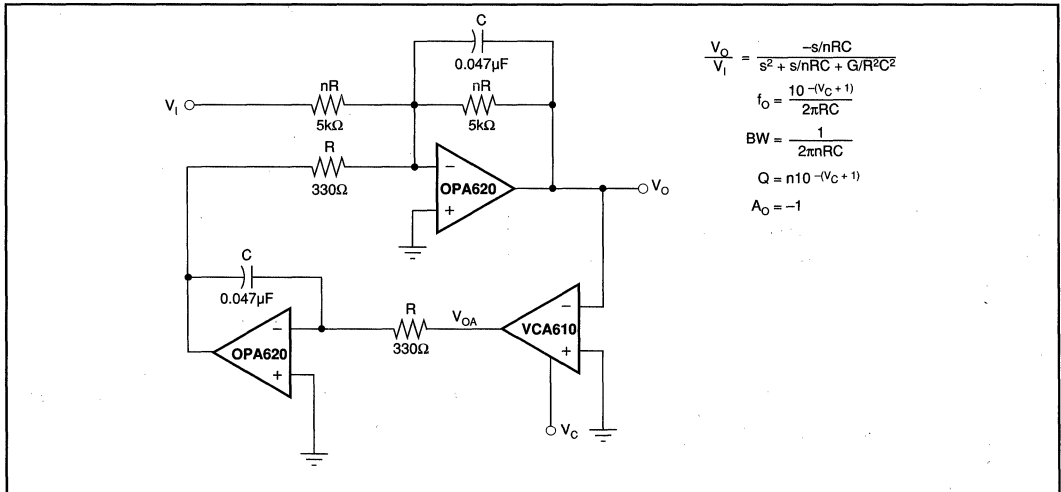
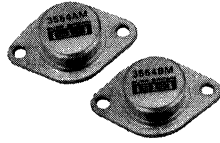


FIGURE 13. Adding the VCA610 to a State-Variable Filter Produces a Voltage-Controlled BandPass Filter With a Center Frequency Variable Over a 100:1 Range.

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Wideband, Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE: 1000V/μs
- FAST SETTLING: 150ns, max (to ±0.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

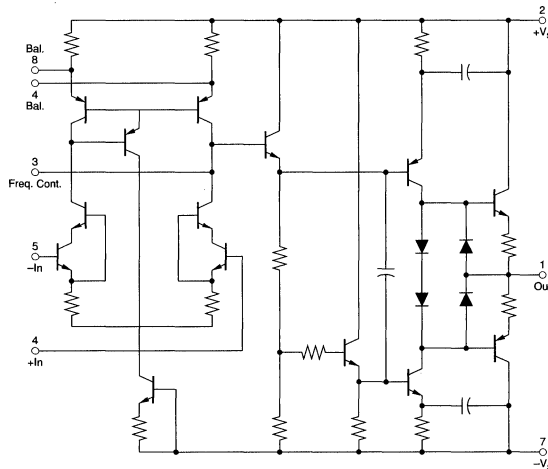
DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

The 3554 has a slew rate of 1000V/μs and will output ±10V and ±100mA. When used as a fast settling

amplifier, the 3554 will settle to ±0.05% of the final value within 150ns. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged, and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-331C

2.461

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OPERATIONAL AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

At $T_{CASE} = +25^{\circ}C$ and $\pm 15VDC$, unless otherwise noted.

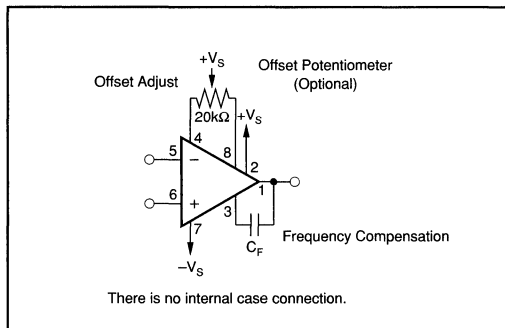
PARAMETER	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC											
No Load		100	106		*	*		*	*		dB
Rated Load	$R_L = 100\Omega$	90	96		*	*		*	*		dB
RATED OUTPUT											
Voltage	$I_O = \pm 100mA$	± 10	± 11		*	*		*	*		V
Current	$V_O = \pm 10V$	± 100	± 125		*	*		*	*		mA
Output Resistance, Open-Loop	$f = 10MHz$		20		*	*		*	*		Ω
DYNAMIC RESPONSE											
Bandwidth (0dB, small signal)	$C_f = 0$	70	90		*	*		*	*		MHz
Gain-bandwidth Product	$C_f = 0, G = 10V/V$	150	225		*	*		*	*		MHz
	$C_f = 0, G = 100V/V$	425	725		*	*		*	*		MHz
	$C_f = 0, G = 1000V/V$	1000	1700		*	*		*	*		MHz
Full Power Bandwidth	$C_f = 0, V_O = 20Vp-p, R_L = 100\Omega$	16	19		*	*		*	*		MHz
Slew Rate	$C_f = 0, V_O = 20Vp-p, R_L = 100\Omega$	1000	1200		*	*		*	*		V/ μs
Settling Time: to $\pm 1\%$	$A = 1$		60		*	*		*	*		ns
	$A = 1$		120		*	*		*	*		ns
	$A = 1$		140	150	*	*	*	*	*		ns
	$A = 1$		200	250	*	*	*	*	*		ns
INPUT OFFSET VOLTAGE											
Input Offset, $T_A = 25^{\circ}C$		± 0.5	± 2		± 0.2	± 1		± 0.2	± 1		mV
vs Temp ($T_A = -25^{\circ}C$ to $+85^{\circ}C$)		± 20	± 50		± 8	± 15		± 12	± 25		$\mu V/^{\circ}C$
vs Temp ($T_A = -55^{\circ}C$ to $+125^{\circ}C$)					*	*		*	*		$\mu V/^{\circ}C$
vs Supply Voltage		± 80	± 300		*	*		*	*		$\mu V/V$
INPUT BIAS CURRENT											
Input Bias, $25^{\circ}C$		0	-10	-50	*	*	*	*	*	*	pA
vs Temp			⁽¹⁾		*	*	*	*	*	*	pA
vs Supply Voltage			± 1		*	*	*	*	*	*	pA/V
INPUT DIFFERENCE CURRENT											
Initial Difference, $25^{\circ}C$			± 2	± 10	*	*		*	*		pA
INPUT IMPEDANCE											
Differential			$10^{11} \parallel 2$		*	*		*	*		$\Omega \parallel pF$
Common-Mode			$10^{11} \parallel 2$		*	*		*	*		$\Omega \parallel pF$
INPUT NOISE											
Voltage, $f_o = 1Hz$	$R_s = 100\Omega$		125		*	*		*	*		nV/\sqrt{Hz}
$f_o = 10Hz$	$R_s = 100\Omega$		50		*	*		*	*		nV/\sqrt{Hz}
$f_o = 100kHz$	$R_s = 100\Omega$		25		*	*		*	*		nV/\sqrt{Hz}
$f_o = 1kHz$	$R_s = 100\Omega$		15		*	*		*	*		nV/\sqrt{Hz}
$f_o = 10kHz$	$R_s = 100\Omega$		10		*	*		*	*		nV/\sqrt{Hz}
$f_o = 100kHz$	$R_s = 100\Omega$		8		*	*		*	*		nV/\sqrt{Hz}
$f_o = 1MHz$	$R_s = 100\Omega$		7		*	*		*	*		nV/\sqrt{Hz}
$f_o = 0.3Hz$ to $10Hz$	$R_s = 100\Omega$		2		*	*		*	*		$\mu Vp-p$
$f_o = 10Hz$ to $1MHz$	$R_s = 100\Omega$		8		*	*		*	*		μV_{rms}
Current, $f_o = 0.3Hz$ to $10Hz$	$R_s = 100\Omega$		45		*	*		*	*		fA p-p
$f_o = 10Hz$ to $1MHz$	$R_s = 100\Omega$		2		*	*		*	*		pArms
INPUT VOLTAGE RANGE											
Common-Mode Voltage Range	Linear Operation	44	$\pm(V_{CC}-4)$	78	*	*		*	*		V
Common-Mode Rejection	$f = DC, V_{CM} = +7V, -10V$		± 78		*	*		*	*		dB
Maximum Safe Input Voltage			$\pm Supply$		*	*		*	*		V
POWER SUPPLY											
Rated Voltage			± 15		*	*		*	*		VDC
Voltage Range, Derated Performance		± 5		± 18	*	*	*	*	*	*	VDC
Current, Quiescent		± 17	± 35	± 45	*	*	*	*	*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	-25		+85	-25		+85	-55		+125	$^{\circ}C$
Operating, Derated Performance	Ambient Temperature	-55		+125	-55		+125	-55		+125	$^{\circ}C$
Storage	Ambient Temperature	-65		+150	-65		+150	-65		+150	$^{\circ}C$
θ Junction-Case	Ambient Temperature		15			15			15		$^{\circ}C/W$
θ Junction-Ambient	Ambient Temperature		45			45			45		$^{\circ}C/W$

* Specifications same as for 3554AM.

NOTE: (1) Doubles every $+10^{\circ}C$.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

AMPLIFIER CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	$\pm 18V$
Input Voltage	$\pm V_S$
Output Short Circuit (to ground)	10s
Operating Temperature	$-55^{\circ}C$ to $+125^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature	$+165^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
3554AM	8-Pin Metal TO-3	$-25^{\circ}C$ to $+85^{\circ}C$
3554BM	8-Pin Metal TO-3	$-25^{\circ}C$ to $+85^{\circ}C$
3554SM	8-Pin Metal TO-3	$-55^{\circ}C$ to $+125^{\circ}C$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING
		NUMBER
3554AM	8-Pin Metal TO-3	030
3554BM	8-Pin Metal TO-3	030
3554SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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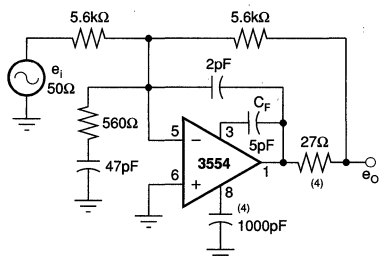
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OPERATIONAL AMPLIFIERS

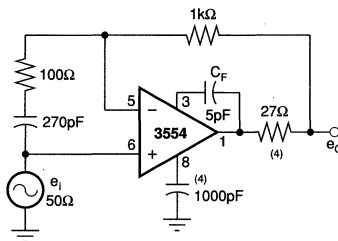
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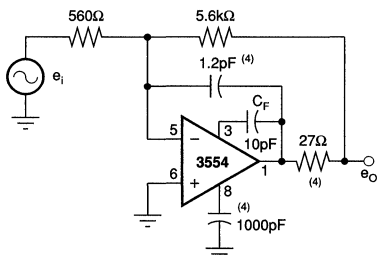
TYPICAL CIRCUITS



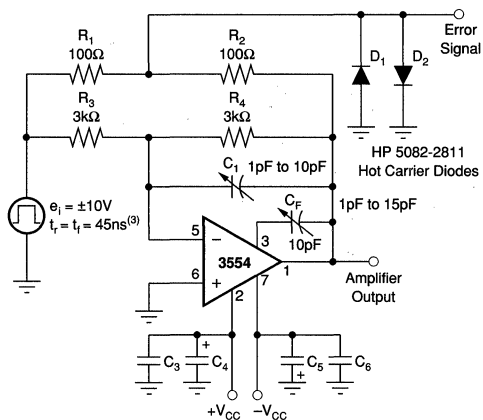
Gain = $-1V/V$ (1)



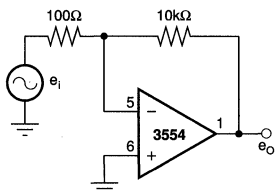
Gain = $+1V/V$ (1)



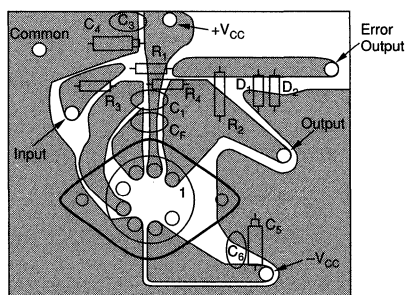
Gain = $-10V/V$ (1)



Settling Time Test Circuit Schematic



Gain = $+100V/V$ (2)



Settling Time Test Circuit Layout

View from component side.

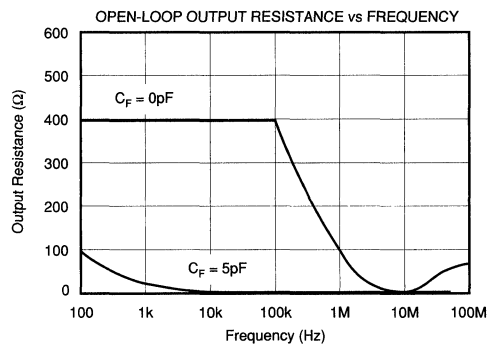
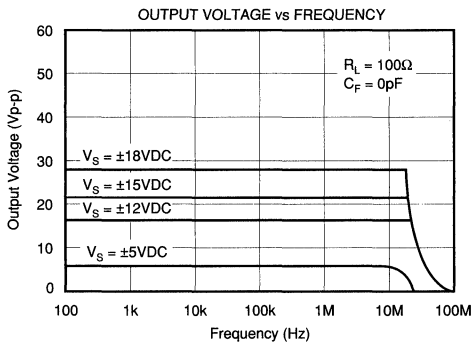
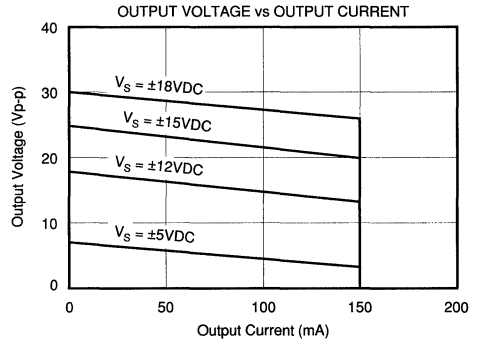
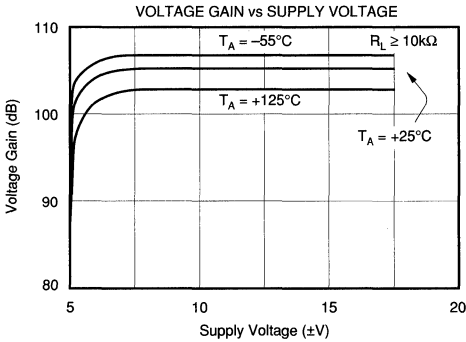
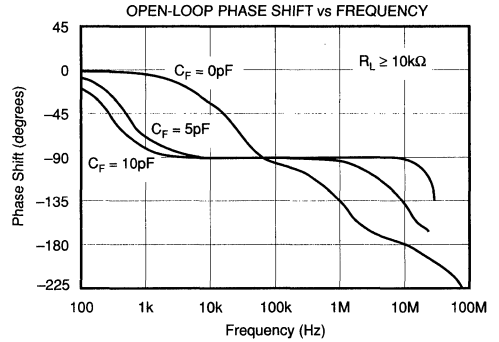
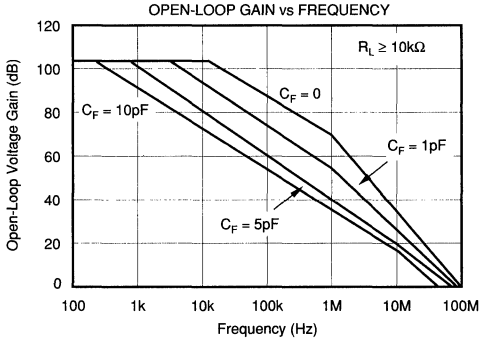
Shaded area is the pattern side conductor.

NOTES: (1) These circuits are optimized for driving large capacitive loads (to 470pF). (2) The 3554 is stable at gains of greater than 55 ($C_L \leq 100pF$) without any frequency compensation. (3) 45ns is optimum. Very fast rise times (10-20ns) may saturate the input stage causing less than optimum settling time performance. (4) Component may be eliminated when large capacitive loads are not being driven by the device.

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TYPICAL PERFORMANCE CURVES

At $T_C = +25^\circ\text{C}$ and $\pm 15\text{VDC}$, unless otherwise noted.

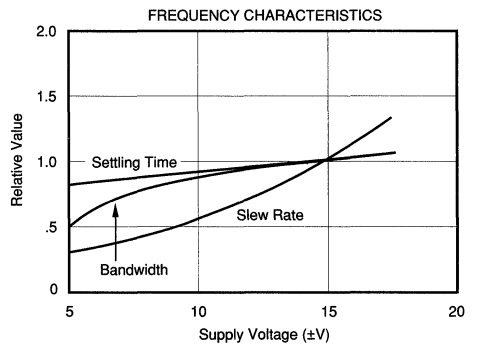
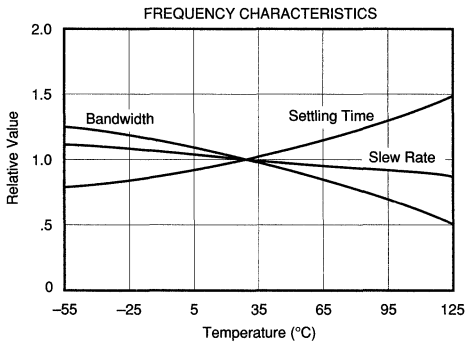
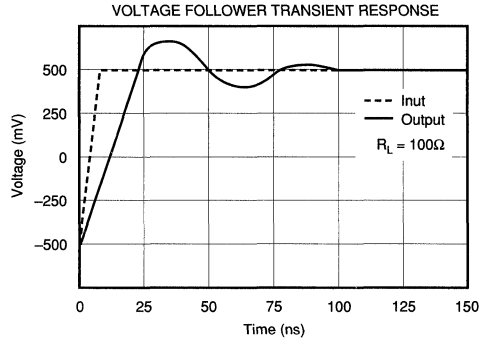
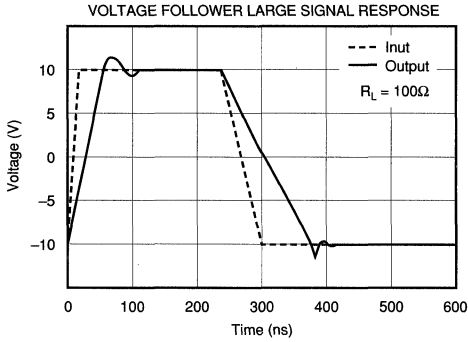
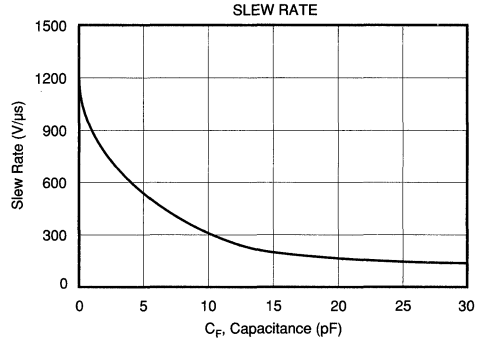
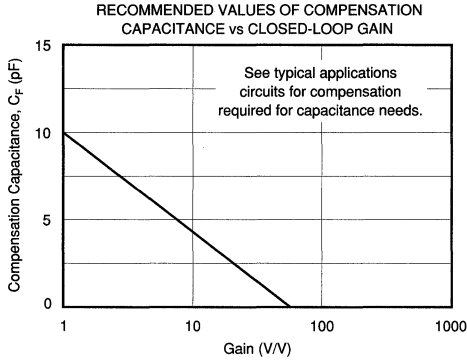


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OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

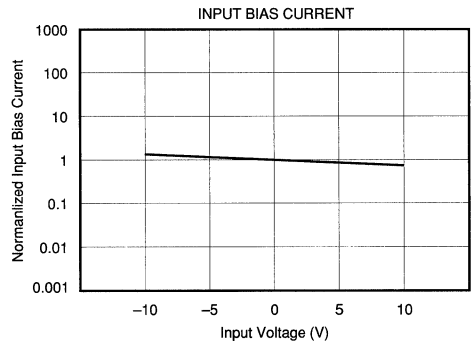
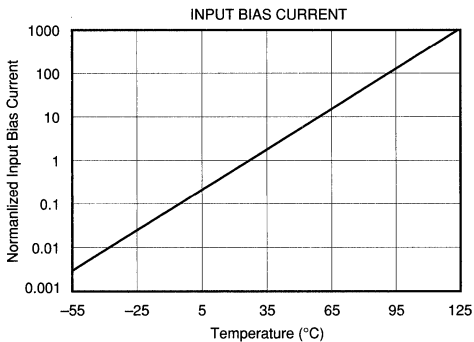
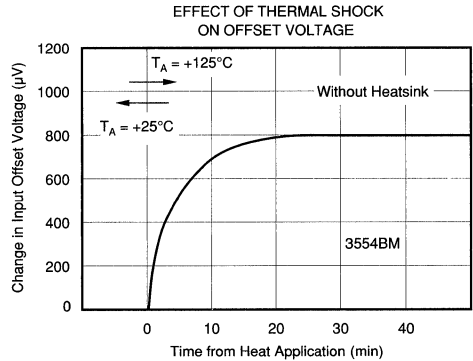
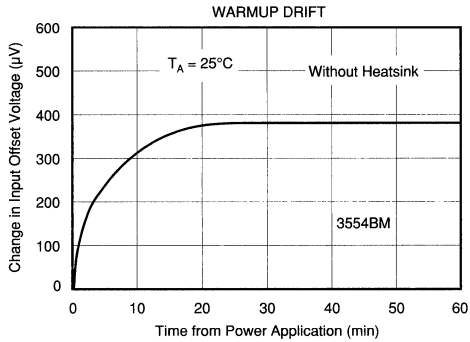
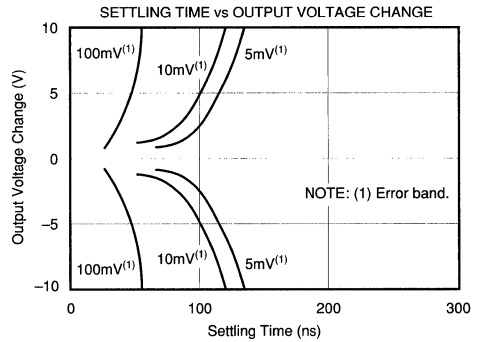
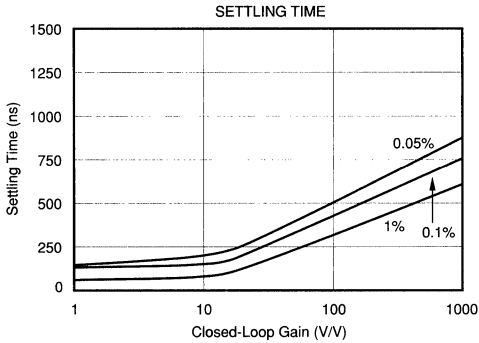
At $T_c = +25^\circ\text{C}$ and $\pm 15\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

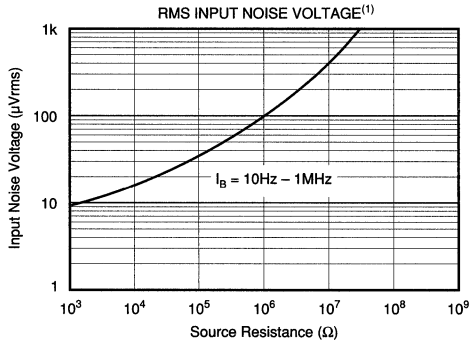
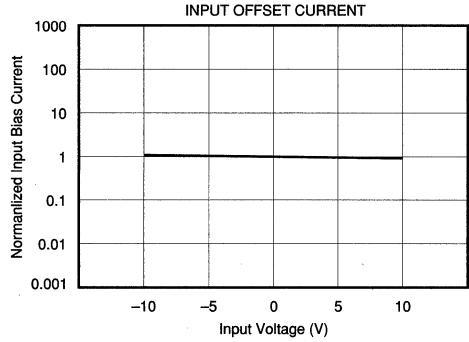
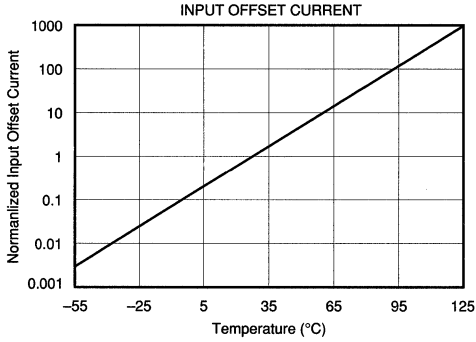
At $T_c = +25^\circ\text{C}$ and $\pm 15\text{VDC}$, unless otherwise noted.



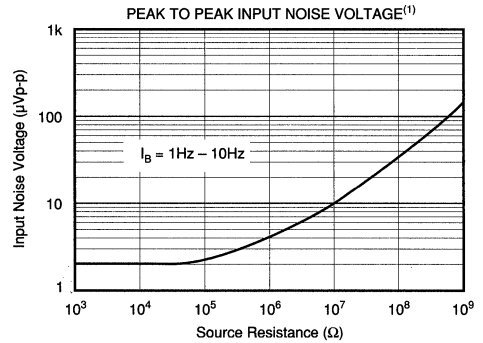
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TYPICAL PERFORMANCE CURVES (CONT)

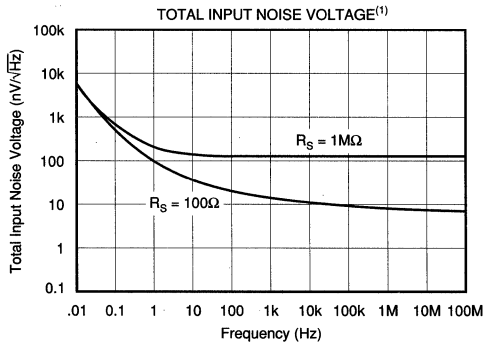
At $T_c = +25^\circ\text{C}$ and $\pm 15\text{VDC}$, unless otherwise noted.



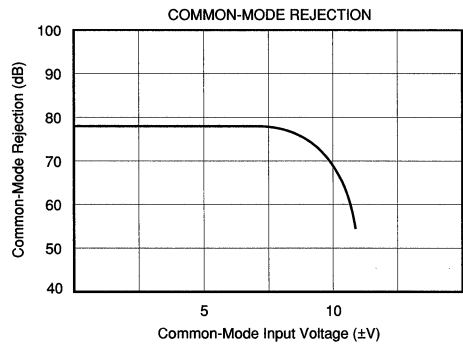
NOTE: (1) Includes contribution from source resistance.



NOTE: (1) Includes contribution from source resistance.



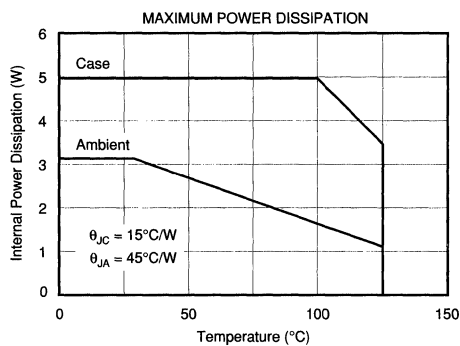
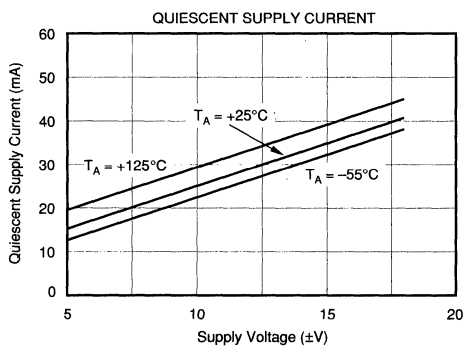
NOTE: (1) Includes contribution from source resistance.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_c = +25^\circ\text{C}$ and $\pm 15\text{VDC}$, unless otherwise noted.



APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1GHz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the "Typical Circuits." It may also be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than $5.6\text{k}\Omega$ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits, a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed

circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the "Typical Circuits."

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a $1\mu\text{F}$ tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the noninverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the noninverting input. A slight offset error will result, however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point-to-point wiring is used or a ground plane is not, single point grounding should be used. The input signal return, the load signal return, and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit, grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

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2

OPERATIONAL AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard will also reduce stray signal coupling to the input.

In high frequency applications, guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the following section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition, several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F , is connected between pins 1 and 3. As the performance curves show, larger closed-loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed-loop gains above 55V/V and when the load capacitance is less than 100pF.

When driving large capacitive loads, 470pF and greater, an additional capacitor, C_S , is connected between pin 8 and ground. This capacitor is typically 1000pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the "Typical Circuits" for the XGain = -10V/V circuit.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6k Ω are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit

layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1k Ω) and up to 10pF for circuits using larger resistances.

SETTLING TIME

Settling time is a complete dynamic measure of the 3554's total performance. It includes the slew rate time (a large signal dynamic parameter) and the time to accurately reach the final value (a small signal parameter that is a function of bandwidth and open loop-gain). The settling time may be optimized for the particular application by selection of the closed-loop gain and the compensation capacitance. The best settling time is observed in low closed-loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required from the signal input step for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the bandwidth. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000pF) when properly compensated. See the section on "Compensation." The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50 Ω loads connected via coaxial cables due to its ± 100 mA output drive capability. The capacitance of the coaxial cable, 29pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20k Ω linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, noninductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be extremely short to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided or oscillation may occur.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by $\pm 0.004\mu\text{V}/^\circ\text{C}$.

HEAT SINKING

The 3554 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heat sink will be necessary as indicated in the "Maximum Power Dissipation" curve. A heat sink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heat sinks available in three sizes $-3^\circ\text{C}/\text{W}$, $4.2^\circ\text{C}/\text{W}$ and $12^\circ\text{C}/\text{W}$. A separate product data sheet is available upon request.

When heat sinking the 3554, it is recommended that the heat sink be connected to the amplifier case and the combination not connected to the ground plane. For a single-sided printed circuit board, the heat sink may be mounted between the 3554 and the nonconductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heat sink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heat sink to each pin will depend on the thickness and type of heat sink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

3554

2

OPERATIONAL AMPLIFIERS



3 Power Operational Amplifiers

Burr-Brown power amplifiers are designed for high output voltage and/or high output current. Versatile power operational amplifiers can be used in virtually any op amp circuit configuration, yet can supply up to $\pm 15A$ load current or $\pm 140V$ output voltage.

Buffer amplifiers can be used with common op amps to drive long lines or heavy loads such as valves, voice-coils and actuators.

Choose from a wide variety of power amp types, including:

BUF634—250mA, 2000V/ μs buffer amp. Used with a common op amp, this buffer amp boosts output current to 250mA and increases capacitive load drive capability. Versatile and rugged, it's available in SO-8, 8-pin DIP and 5-pin TO-220 packages.

OPA541—This monolithic power op amp delivers output current up to $\pm 5A$ and operates from power supplies up to $\pm 40V$. Available in low cost plastic power SIP and hermetic 8-pin TO-3 packages.

OPA502— $\pm 10A$ output from $\pm 40V$ supplies highlight this rugged performer. Ideal for programmable power sources, motor drivers, or even high performance audio amplifiers.

3583—Power supply voltages up to $\pm 150V$ and output current to 75mA suit many programmable V/I source or high voltage transducer applications.

3584—Power supplies to $\pm 150V$ and slew rates to 150V/ μs are ideal for piezoelectric transducers and electrostatic deflection circuitry.

Other models provide special features and performance. Use our detailed selection guide to locate the power amp for your application.

3

POWER OPERATIONAL AMPLIFIERS

HIGH VOLTAGE, HIGH CURRENT OPERATIONAL AMPLIFIERS

Boldface = NEW

Description	Model	Rated Supply Voltage ($\pm V$)	Output Current ($\pm mA$)	Offset Voltage		Bias Current (25°C), max (μA)	Frequency Response		Open Loop Gain (dB)	Temp Range ⁽¹⁾	Pkg	Page No.
				At 25°C ($\pm mV$)	Temp Drift ($\pm \mu V/^\circ C$)		Unity Gain (MHz)	Slew Rate (V/ μs)				
High Power	OPA501	± 34	10A	5	40	20nA	1	1.35	98	Ind	TO-3	3.2.33
	OPA502	± 45	10A	5	5 ⁽⁹⁾	200	1.4	10	103	XInd/Mil	TO-3	3.2.39
	OPA511	22	5A	10	65	40nA	1	1	91	Ind	TO-3	A
	OPA512	± 45	10A	6	65	30nA	4	2.5	110	Ind	TO-3	3.2.49
		± 45	15A	3	40	20nA	4	2.5	110	Mil	TO-3	
		± 40	5A	1	30	50	1.6	6	90	Ind/Mil	TO-3	3.2.55
		± 35	5A	10	40	50	1.6	6	90	Ind	Power Plastic	
(Dual)	OPA2541	± 40	5A	1	30	50	1.6	6	90	Ind/Mil	TO-3	3.2.71
	OPA544	± 35	2A	5	10	100	1.4	8	90	XInd	5-Pin TO-220	3.2.63
(Dual)	OPA2544	± 35	2A	5	10	50	1.4	8	90	XInd/Mil	TO-3	3.2.86
	3573	20	2A ⁽⁴⁾	10	65	40nA	1	2.6	94	Ind	TO-3	A

^(A) indicates a product that is still available but not included in the 1995 Data Books—contact factory for data sheet.

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HIGH VOLTAGE, HIGH CURRENT OPERATIONAL AMPLIFIERS (Continued) Boldface = NEW

Description	Model	Rated Output min		Offset Voltage max		Bias Current (25°C) max (pA)	Frequency Response		Loop Gain (dB)	Open Temp Range ⁽¹⁾	Pkg	Page No.
		(±V)	(±mA)	At 25°C (±mV)	Temp Drift (±µV/°C)		Unity Gain (MHz)	Slew Rate (V/µs)				
Wideband	3554	10	100	1	15	-50	1700 ⁽²⁾	1200	100	Ind	TO-3	2.426
	OPA654	11	200 ⁽⁵⁾	3	40 ⁽⁵⁾	50	32	750	94	Ind	TO-3	2.316
High Voltage	3584	145	15	3	25	20	20 ⁽²⁾	150	120	Com	TO-3	3.2.100
	3583	140	75	3	23	20	5	30	118	Com/Ind	TO-3	3.2.95
	3582	145	15	3	25	20	5	20	118	Com	TO-3	A
	3581	70	30	3	25	20	5	20	112	Com	TO-3	A
	3580	30	60	10	30	50	5	15	106	Com	TO-3	A
	OPA445	35	15	3	10	50	2	10	100	Ind/Mil	TO-99, DIP	3.2.27

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, XInd = -40°C to +85°C, Mil = -55°C to +125°C. (2) Gain-bandwidth product. (3) 2A peak. (4) 5A peak. (5) Typical.

"A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

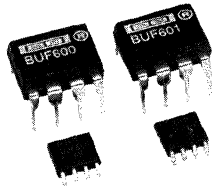
UNITY-GAIN BUFFER OPERATIONAL AMPLIFIERS Boldface = NEW

Description	Model	Rated Output, min		Frequency Response			Gain (V/V)	Input Impedance (Ω)	Temp Range ⁽¹⁾	Pkg	Page No.
		(±V)	(±mA)	-3dB (MHz)	Full Power (MHz)	SR (V/µs)					
High Performance	3553	10	200	300	32	2000	≈1	10 ¹¹	Ind	TO-3	A
Low Cost	BUF634	10	250	180		2000	≈1	50M	Ind	DIP, SO-8, TO-220	3.1.18
	OPA633	11	80	275	65	2500	≈1	1.5M	Ind	DIP	3.2.70
Transconductance Amp and Buffer	OPA660	3.7	10	850	570	3000	≈1	1M	XInd	DIP, SOIC	2.328
High Slew Rate	BUF600	3.3	20	650	320	3400	≈1	4.8M	XInd	DIP, SOIC	3.1.3
	BUF601	3.3	20	900	320	3600	≈1	2.5M	XInd	DIP, SOIC	3.1.3

NOTE: (1) Ind = -25°C to +85°C. (2) XInd = -40°C to +85°C.

"A" indicates a product that is still available but not included in the 1995 Data Books—contact factory for data sheet.

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BUF600/601

HIGH-SPEED BUFFER AMPLIFIER

BUF600/601

3.1

BUFFER AMPLIFIERS

FEATURES

- OPEN-LOOP BUFFER
- HIGH-SLEW RATE: 3600V/ μ s, 5.0Vp-p
- BANDWIDTH: 320MHz, 5.0Vp-p
900MHz, 0.2Vp-p
- LOW INPUT BIAS CURRENT: 0.7 μ A/1.5 μ A
- LOW QUIESCENT CURRENT: 3mA/6mA
- GAIN FLATNESS: 0.1dB, 0 to 300MHz

DESCRIPTION

The BUF600/601 are monolithic open-loop unity-gain buffer amplifiers with a high symmetrical slew rate of up to 3600V/ μ s and a very wide bandwidth of 320MHz at 5Vp-p output swing. They use a complementary bipolar IC process, which incorporates pn-junction isolated high-frequency NPN and PNP transistors to achieve high-frequency performance previously unattainable with conventional integrated circuit technology.

Their unique design offers a high-performance alternative to expensive discrete or hybrid solutions.

The buffer amplifiers BUF600/601 feature low quiescent current, low input bias current, small signal delay time and phase shift, and low differential gain and phase errors.

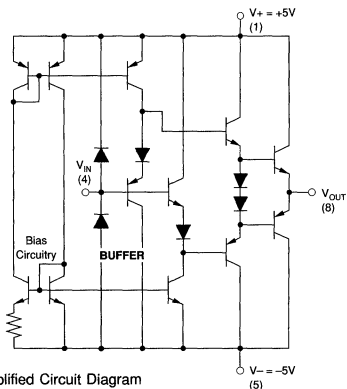
The BUF600 with 3mA quiescent current is well-suited for operation between high-frequency processing stages. It demonstrates outstanding performance even in feedback loops of wide-band amplifiers or phase-locked loop systems.

APPLICATIONS

- VIDEO BUFFER/LINE DRIVER
- INPUT/OUTPUT AMPLIFIER FOR MEASUREMENT EQUIPMENT
- PORTABLE SYSTEMS
- TRANSMISSION SYSTEMS
- TELECOMMUNICATIONS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- ULTRASOUND

The BUF601 with 6mA quiescent current and therefore lower output impedance can easily drive 50 Ω inputs or 75 Ω systems and cables.

The broad range of analog and digital applications extends from decoupling of signal processing stages, impedance transformation, and input amplifiers for KF equipment and ATE systems to video systems, distribution fields, IF/communications systems, and output drivers for graphic cards.



Simplified Circuit Diagram

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL—DC SPECIFICATION

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 10k\Omega$, $R_{SOURCE} = 50\Omega$, and $T_{AMB} = +25^{\circ}C$, unless otherwise noted.

PARAMETER	CONDITIONS	BUF600AP/AU			BUF601AP/AU			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT OFFSET VOLTAGE Initial vs Temperature vs Supply (tracking) vs supply (non-tracking) vs Supply (non-tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +4.5V$ to $+5.5V$ $V_{CC} = -4.5V$ to $-5.5V$		-4 9	± 30		-1.5 25	± 30	mV $\mu V/^{\circ}C$	
			-54	-72	-54	-77		dB	
				-55		-55		dB	
				-54		-54		dB	
									dB
INPUT BIAS CURRENT Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +4.5V$ to $+5.5V$ $V_{CC} = -4.5V$ to $5.5V$		0.7 0.4	-2.5/+5		1.5 0.7	-5/+10	μA nA/ $^{\circ}C$	
				0.15		0.3		$\mu A/V$	
				0.5		0.5		$\mu A/V$	
				20		20		nA/V	
									nA/V
INPUT IMPEDANCE			4.8 1			2.5 1	$M\Omega$ pF		
INPUT NOISE Voltage Noise Density Signal-to-Noise Ratio	f = 100kHz to 100MHz S/N = 20 Log (0.7/(Vn · $\sqrt{5MHz}$))		5.2			4.8		nV/ \sqrt{Hz}	
			95			96		dB	
TRANSFER CHARACTERISTICS Voltage Gain; $V_{IN} = \pm 2.5V$ $R_{LOAD} = R_i = 100\Omega$ $R_{LOAD} = R_i = 200\Omega$ $R_{LOAD} = R_i = 10k\Omega$						0.95		V/V	
			0.96			0.99		V/V	
			0.99					V/V	
									V/V
RATED OUTPUT Voltage Output DC Current Output Output Impedance	Gain > 0.94 $R_{LOAD} = 100\Omega$ $R_{LOAD} = 200\Omega$ DC, $R_{LOAD} = 100\Omega$		± 2.5	± 3.3	± 2.5	± 3.0		V V mA	
			± 20		± 20			Ω pF	
			6.2 2			3.6 2			
POWER SUPPLY Rated Voltage Derated Performance Quiescent Current Rejection Ratio			± 4.5	± 5	± 5.5	± 5	± 5.5	VDC VDC	
			± 2.6	± 3	± 3.4	± 5.4	± 6	± 6.6	mA
			-54	-72		-54	-77		dB
									dB
TEMPERATURE RANGE Specification Storage			-40	85	-40		85	$^{\circ}C$	
			-40	125	-40		125	$^{\circ}C$	

AC-SPECIFICATION

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 200\Omega$ (BUF600) and 100Ω (BUF601), $R_{SOURCE} = 50\Omega$, and $T_{AMB} = +25^{\circ}C$, unless otherwise noted.

PARAMETER	CONDITIONS	BUF600AP/AU			BUF601AP/AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY DOMAIN								
LARGE SIGNAL BANDWIDTH (-3dB)	$V_O = 5Vp-p$, $C_{OUT} = 1pF$ $V_O = 2.8Vp-p$, $C_{OUT} = 1pF$ $V_O = 1.4Vp-p$, $C_{OUT} = 1pF$		320			320		MHz
			400			400		MHz
			700			700		MHz
SMALL SIGNAL BANDWIDTH	$V_O = 0.2Vp-p$, $C_{OUT} = 1pF$		650			900		MHz
GROUP DELAY TIME			250			200		ps
DIFFERENTIAL GAIN	$V_{IN} = 0.3Vp-p$, f = 4.43MHz VDC = 0 to 0.7V BUF600 $R_{LOAD} = 200\Omega$ $R_{LOAD} = 1k\Omega$ BUF601 $R_{LOAD} = 100\Omega$ $R_{LOAD} = 500\Omega$		0.5					%
			0.075					%
						0.4		%
						0.05		%
DIFFERENTIAL PHASE	$V_{IN} = 0.3Vp-p$, f = 4.43MHz VDC = 0 to 0.7V BUF600 $R_{LOAD} = 200\Omega$ $R_{LOAD} = 1k\Omega$ BUF601 $R_{LOAD} = 100\Omega$ $R_{LOAD} = 500\Omega$		0.02					Degrees
			0.04					Degrees
						0.025		Degrees
						0.03		Degrees

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AC-SPECIFICATIONS (CONT)

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 200\Omega$ (BUF600) and 100Ω (BUF601), $R_{SOURCE} = 50\Omega$, and $T_{AMB} = +25^{\circ}C$, unless otherwise noted.

PARAMETER	CONDITIONS	BUF600AP/AU			BUF601AP/AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
HARMONIC DISTORTION Second Harmonic Third Harmonic Second Harmonic Third Harmonic Second Harmonic Third Harmonic	$f = 10MHz$, $V_o = 1.4Vp-p$		-65			-65		dBc
			-64			-67		dBc
	$f = 30MHz$, $V_o = 1.4Vp-p$		-51			-59		dBc
			-56			-62		dBc
	$f = 50MHz$, $V_o = 1.4Vp-p$		-43			-53		dBc
			-48			-54		dBc
GAIN FLATNESS PEAKING	$V_o = 0.4Vp-p$, DC to 30MHz		0.01			0.005		dB
	$V_o = 0.4Vp-p$, 30MHz to 300MHz		0.3			0.1		dB
LINEAR PHASE DEVIATION	$V_o = 0.4Vp-p$, DC to 30MHz		5.5			3.8		Degrees
	$V_o = 0.4Vp-p$, 30 to 300MHz		55			45		Degrees
TIME DOMAIN								
RISE TIME	10% to 90%, 700ps							
	1.4Vp-p Step		0.82			0.87		ns
	2.8Vp-p Step		0.97			0.95		ns
	5.0Vp-p Step		1.18			1.13		ns
SLEW RATE	$V_o = 1.4Vp-p$		1500			1500		V/ μ s
	$V_o = 2.8Vp-p$		2400			2400		V/ μ s
	$V_o = 5.0Vp-p$		3400			3600		V/ μ s

BUF600/601

3.1

BUFFER AMPLIFIERS

ELECTRICAL (FULL TEMPERATURE RANGE $-40^{\circ}C$ to $+85^{\circ}C$)

PARAMETER	CONDITIONS	BUF600AP/AU			BUF601AP/AU			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OFFSET VOLTAGE			-4	± 30		-1.5	± 30	mV	
TRANSFER CHARACTERISTIC	Voltage Gain; $V_{in} = \pm 2.5V$ $R_{LOAD} = 100\Omega$ $R_{LOAD} = 200\Omega$ $R_{LOAD} = 10k\Omega$					0.95		V/V	
			0.99	0.99		0.98	0.99	V/V	
									V/V
									V/V
BIAS CURRENT Input Bias Current			0.7	-2.5/5		1.5	-5/+10	μ A	
RATED OUTPUT Voltage Output	Gain > 0.9 $R_{LOAD} = 100\Omega$ $R_{LOAD} = 200\Omega$ $R_{LOAD} = 10k\Omega$				± 2.8	± 3.2		V	
			± 2.8	± 3.4		± 3.2	± 3.6	V	
			± 3.2	± 3.6		± 3.2	± 3.6	V	
									V
POWER SUPPLY Quiescent Current	$I_o = 0mADC$	± 1.3	± 3	± 6.0	± 2.7	± 6	± 12.0	mA	

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	$\pm 6V$
Input Voltage ⁽¹⁾	$\pm V_{CC} \pm 0.7V$
Operating Temperature	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature	$-40^{\circ}C$ to $+125^{\circ}C$
Junction Temperature	$+150^{\circ}C$
Lead Temperature (soldering, 10s)	$+300^{\circ}C$

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
BUF600AP	Plastic 8-Pin DIP	006
BUF600AU	SO-8 Surface-Mount	182
BUF601AP	Plastic 8-Pin DIP	006
BUF601AU	SO-8 Surface-Mount	182

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
BUF600AP	Plastic 8-Pin DIP	$-40^{\circ}C$ to $+85^{\circ}C$
BUF600AU	SO-8 Surface-Mount	$-40^{\circ}C$ to $+85^{\circ}C$
BUF601AP	Plastic 8-Pin DIP	$-40^{\circ}C$ to $+85^{\circ}C$
BUF601AU	SO-8 Surface-Mount	$-40^{\circ}C$ to $+85^{\circ}C$

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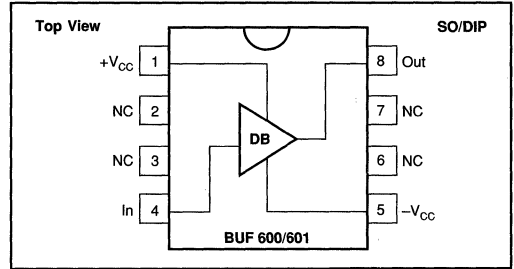


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FUNCTIONAL DESCRIPTION

FUNCTION	DESCRIPTION
In	Analog Input
Out	Analog Output
+V _{cc}	Positive Supply Voltage; typical +5VDC
-V _{cc}	Negative Supply Voltage; typical -5VDC

PIN CONFIGURATION



DICE INFORMATION

BUF600/601 DIE TOPOGRAPHY

PAD	FUNCTION
1	Analog Input
2	-5V Supply
3	-5V, Output
4	Analog Output
5	+5V Supply, Output
6	+5V Supply

Substrate Bias: Negative Supply
 NC: No Connection
 Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	39 x 42 ±5	0.99 x 1.07 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Minimum Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02 +0.05-0.0	0.0005 +0.0013-0.0
Gold	0.30 ±0.05	0.0076 ±0.0013

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The BUF600/601 incorporate on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

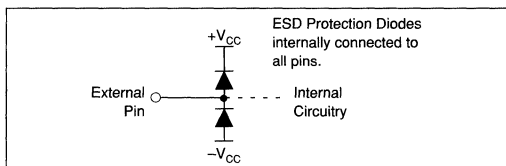


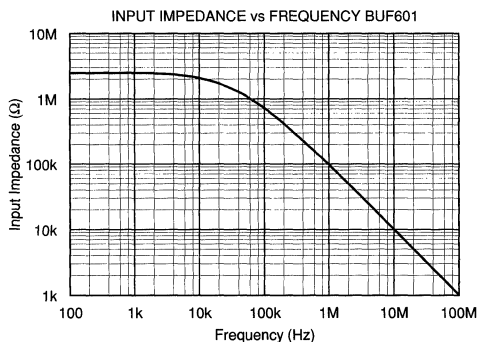
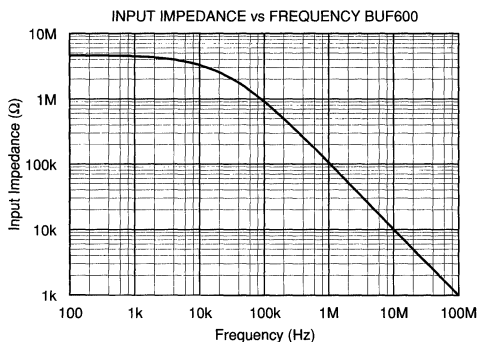
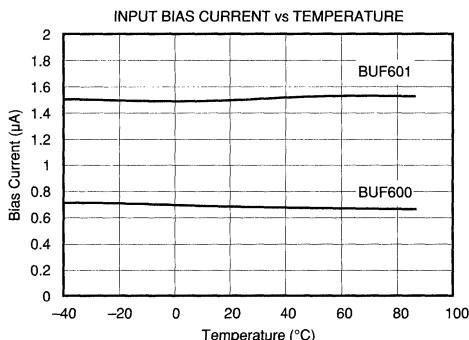
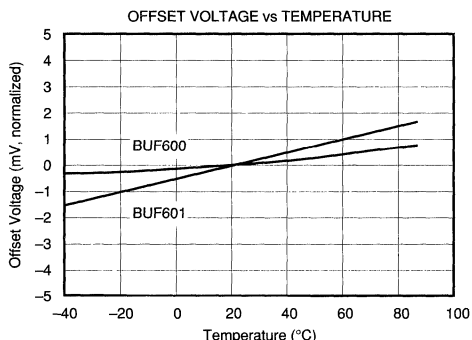
FIGURE 1. Internal ESD Protection.

All input pins on the BUF600/601 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, the diode current should be externally limited to 10mA or so whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision amplifiers, this may cause a noticeable degradation of offset and drift. Therefore, static protection is strongly recommended when handling the BUF600/601.

TYPICAL PERFORMANCE CURVES

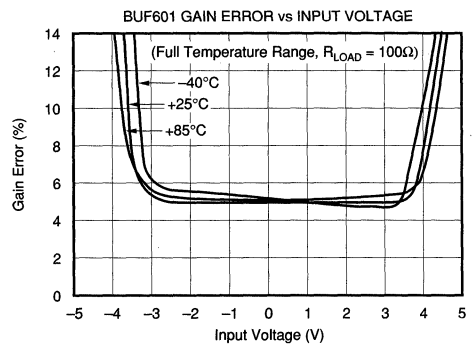
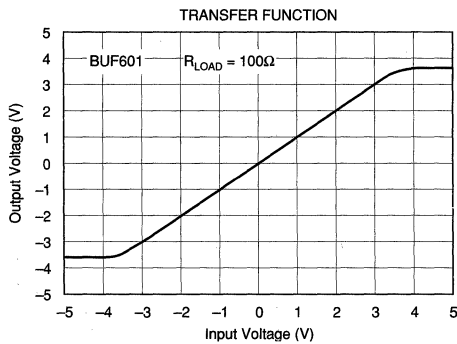
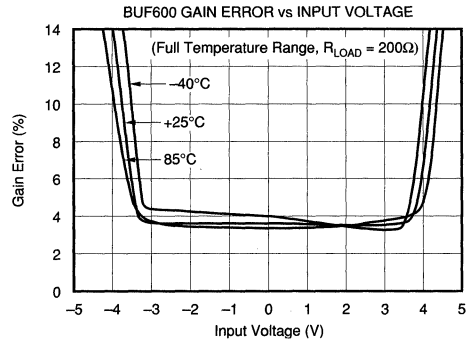
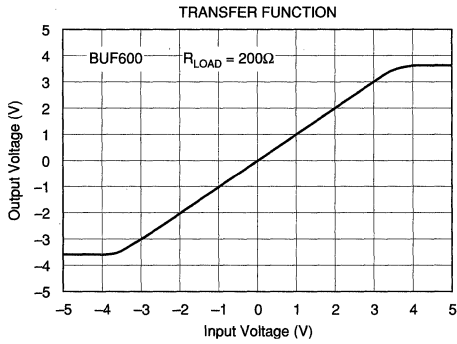
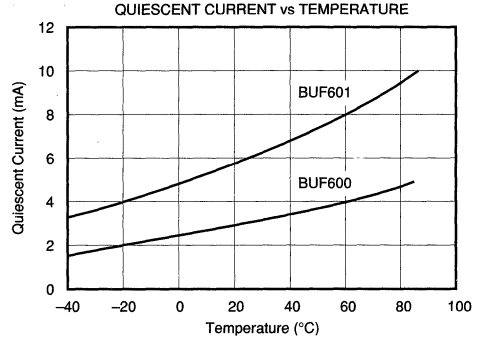
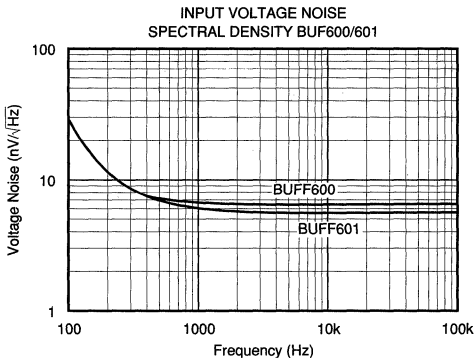
At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 10k\Omega$, and $T_A = 25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

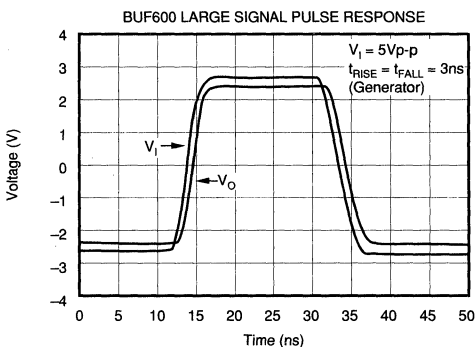
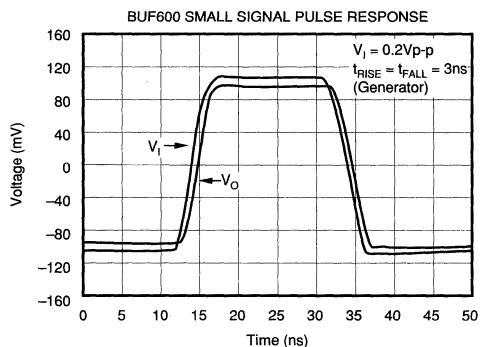
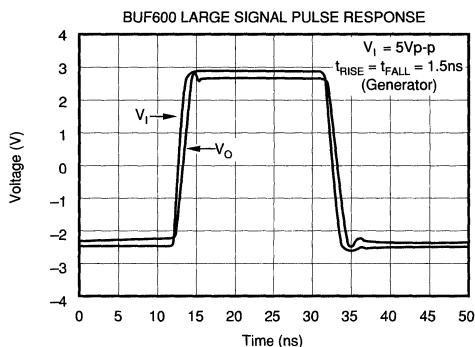
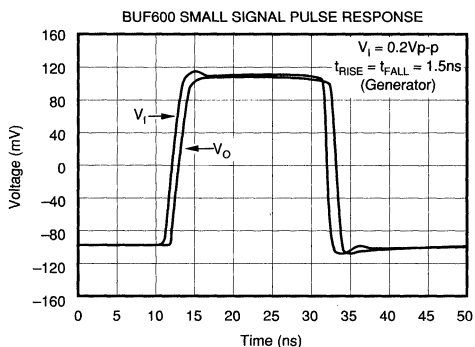
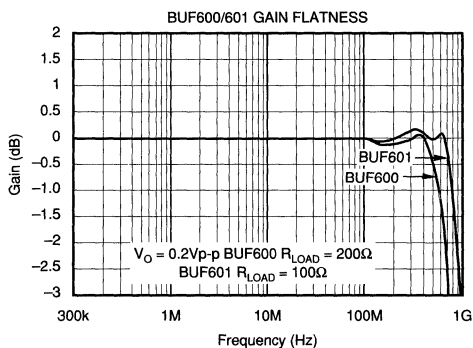
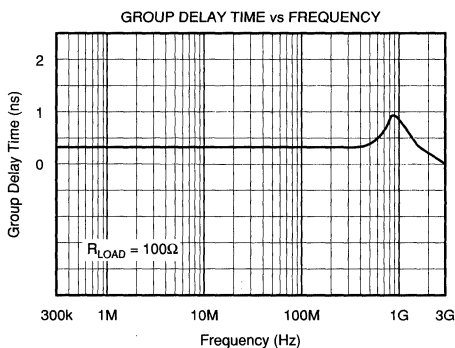
At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 10k\Omega$, and $T_A = 25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25^\circ C$ unless otherwise noted.



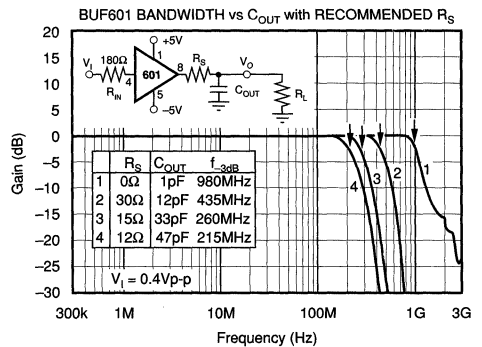
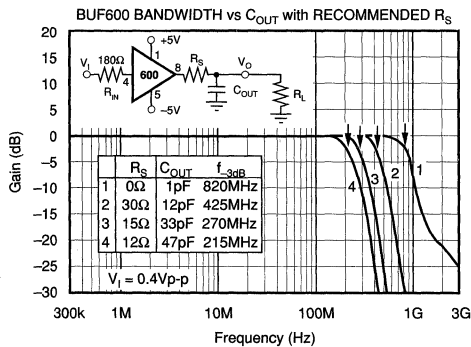
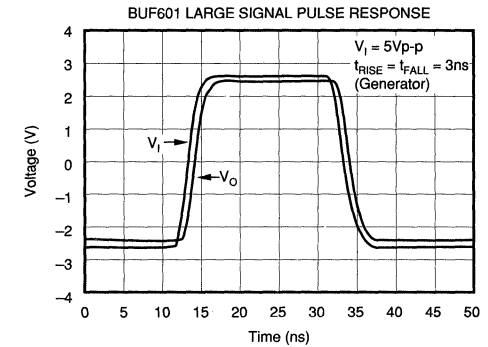
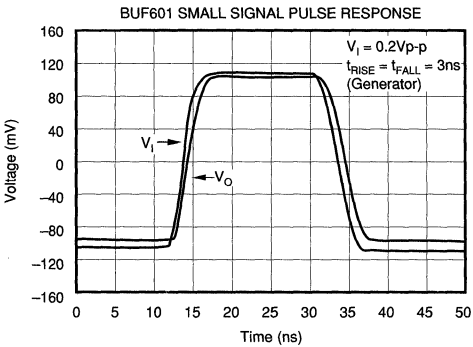
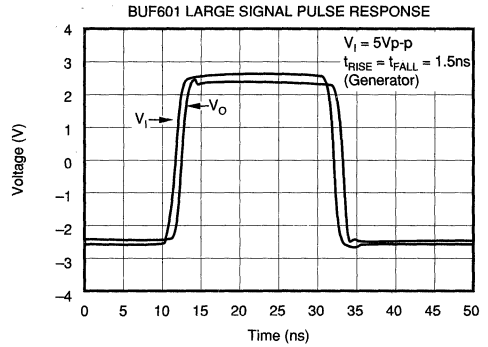
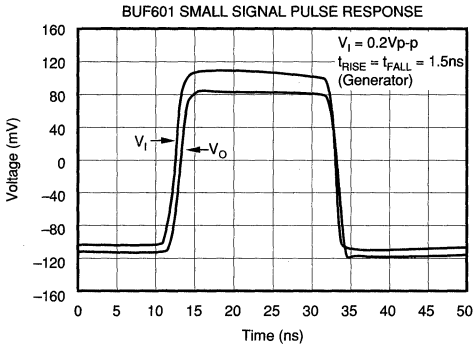
BUF600/601

3.1

BUFFER AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

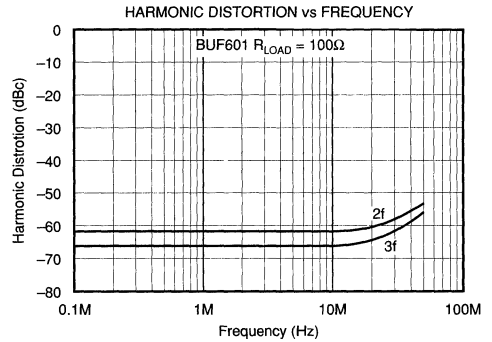
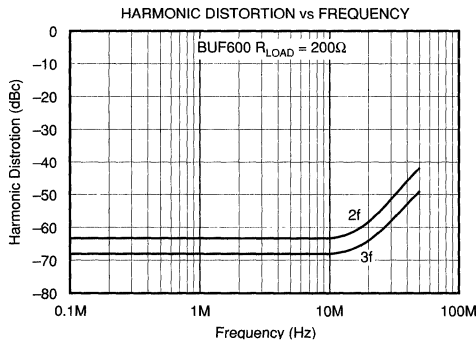
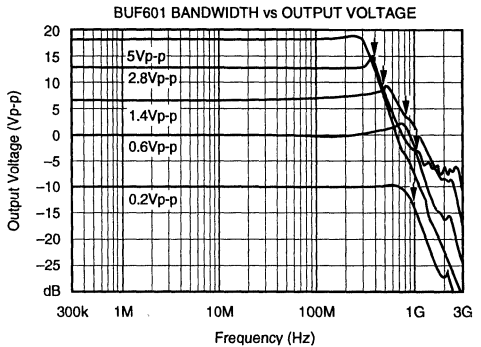
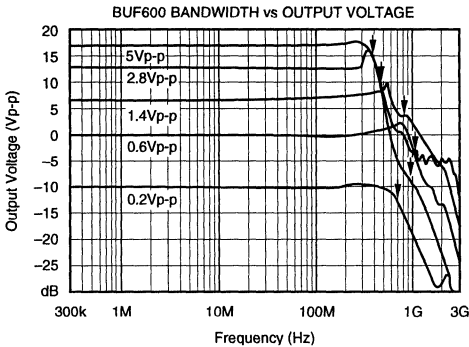
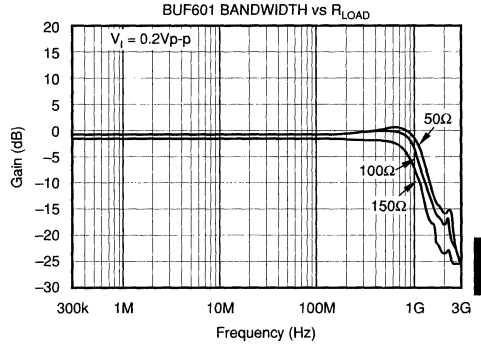
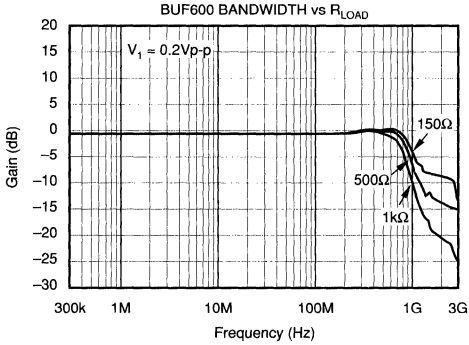
At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25^\circ C$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25^\circ C$ unless otherwise noted.



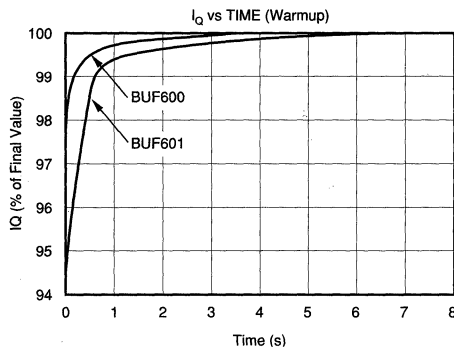
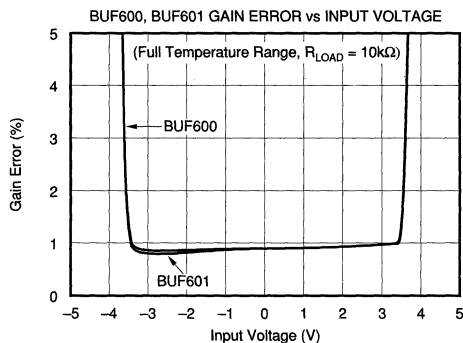
BUF600/601

3.1

BUFFER AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$ (BUF601), $R_{LOAD} = 200\Omega$ (BUF600), and $T_A = 25^\circ C$ unless otherwise noted.



DISCUSSION OF PERFORMANCE

The BUF600/601 are fabricated using a high-performance complementary bipolar process, which provides high-frequency NPN and PNP transistors with gigahertz transition frequencies (f_T). Power supplies are rated at $\pm 6V$ maximum, with the data sheet parameters specified at $\pm 5V$ supplies. The BUF600/601 are 3-stage open-loop buffer amplifiers consisting of complementary emitter followers with a symmetrical class AB Darlington output stage. The complementary structure provides both sink and source current capability independent of the output voltage, while maintaining constant output and input impedances. The amplifiers use no feedback, so their low-frequency gain is slightly less than unity and somewhat dependent on loading. The optimized input stage is responsible for the high slew rate of up to $3600V/\mu s$, wide large signal bandwidth of $320MHz$, and quiescent current reduction to $\pm 3mA$ (BUF600) and $\pm 6mA$ (BUF601). These features yield an excellent large signal bandwidth/quiescent current ratio of $320MHz$, $5Vp-p$ at $3mA/6mA$ quiescent current. The complementary emitter followers of the input stage work with current sources as loads. The internal PTAT power supply controls their quiescent current and with its temperature characteristics keeps the transconductance of the buffer amplifiers constant. The Typical Performance Curves show the quiescent current variation versus temperature.

The cross current in the input stage is kept very low, resulting in a low input bias current of $0.7\mu A/1.5\mu A$ and high input impedance of $4.8M\Omega \parallel 1pF/2.5M\Omega \parallel 1pF$. The second stage drives the output transistors and reduces the output impedance and the feedthrough from output to input when driving RLC loads.

The input of the BUF600/601 looks like a high resistance parallel to a picofarad capacitance. The input characteristics change very little with output loading and input voltage swing. The BUF600/601 have excellent input-to-output isolation and feature high tolerance to variations in source impedances. A resistor between 100Ω and 250Ω in series with the buffer

input lead will usually eliminate oscillation problems from inductive sources such as unterminated cables without sacrificing speed.

Another excellent feature is the output-to-input isolation over a wide frequency range. This characteristic is very important when the buffer drives different equipment over cables. Often the cable is not perfect or the termination is incorrect and reflections arise that act like a signal source at the output of the buffer.

Open-loop devices often sacrifice linearity and introduce frequency distortion when driving low load impedance. The BUF600/601, however, do not. Their design yields low distortion products. The harmonic distortion characteristics into loads greater than 100Ω (BUF601) and greater than 200Ω (BUF600) are shown in the Typical Performance Curves. The distortion can be improved even more by increasing the load resistance.

Differential gain (DG) and differential phase (DP) are among the important specifications for video applications. DG is defined as the percent change in gain over a specified change in output voltage level ($0V$ to $0.7V$.) DP is defined as the phase change in degrees over the same output voltage change. Both DG and DP are specified at the PAL subcarrier frequency of $4.43MHz$. The errors for differential gain are lower than 0.5% , while those for differential phase are lower than 0.04° .

With its minimum $20mA$ long-term DC output current capability, $50mA$ pulse current, low output impedance over frequency, and stability to drive capacitive loads, the BUF601 can drive 50Ω and 75Ω systems or lines. The BUF600 with lower quiescent current and therefore higher output impedance is well-suited primarily to interstage buffering. This type of open-loop amplifier is a new and easy-to-use step to prevent an interaction between two points in complex high-speed analog circuitry.

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The buffer outputs are not current-limited or protected. If the output is shorted to ground, high currents could arise when the input voltage is $\pm 3.6\text{V}$. Momentary shorts to ground (a few seconds) should be avoided but are unlikely to cause permanent damage.

- A resistor (100 Ω to 250 Ω) in series with the input of the buffers may help to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.

CIRCUIT LAYOUT

The high-frequency performance of the buffer amplifiers BUF600/601 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute musts. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2 μF); a parallel 470nF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile solderless sockets.
- Use low-inductance and surface-mounted components. Circuits using all surface-mount components with the BUF600/601AU will offer the best AC performance.

SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the BUF600/601 to speed prototyping. This board allows easy and fast performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. The complete AC characterization was performed with the same type. Figure 2 shows the schematic and Figure 3 the silk screen and double-sided layout. Request DEM-BUF600-1GC or DEM-BUF601-1GC to test the buffer amplifiers in the 8-pin DIP package.

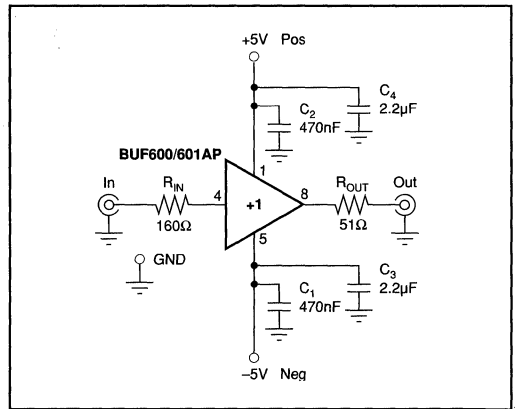


FIGURE 2. Circuit Schematic DEM-BUF600-1GC/DEM-BUF601-1GC.

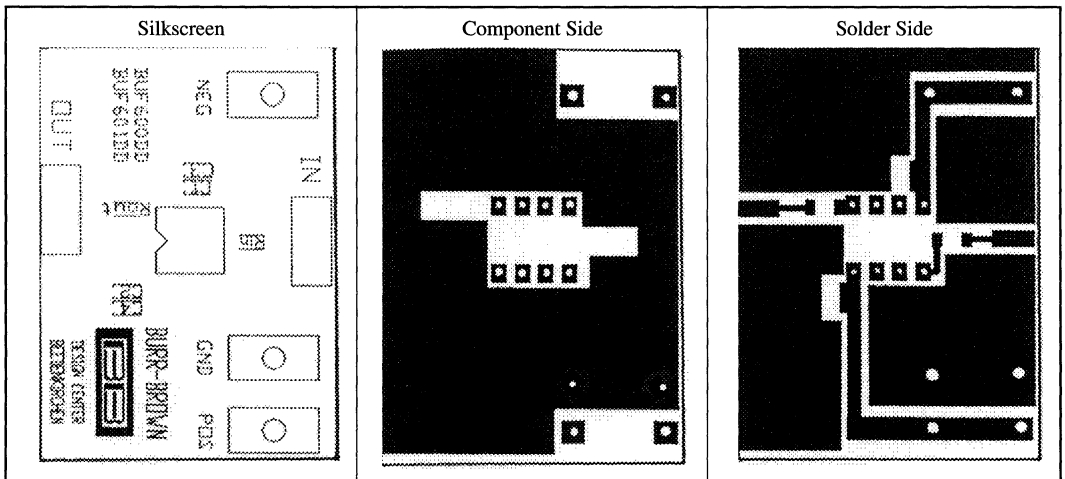


FIGURE 3. Silkscreen and Board Layouts DEM-BUF600-1GC/DEM-BUF601-1GC (DIP package.)



IMPEDANCE MATCHING

The BUF600/601 provides power gain and isolation between source and load when used as an active tap or impedance matching device as illustrated in Figure 4. In this example, there is no output matching path between the BUF600/601 and the 75Ω line. Such matching is not needed when the distant end of the cable is properly terminated, as there is no reflected signal to worry about because the BUF600/601 isolates the source. This technique allows the full output voltage of the BUF600/601 to be applied to the load.

DRIVING CABLES

The most obvious way is to connect the cable directly to the output of the buffer. This results in a gain determined by the buffer output resistance and the characteristic impedance of the cable, assuming it is properly terminated.

Double termination of a cable is the cleanest way to drive it, since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance less the output resistance of the buffer amplifiers. The gain is -6dB excluding of the cable attenuation.

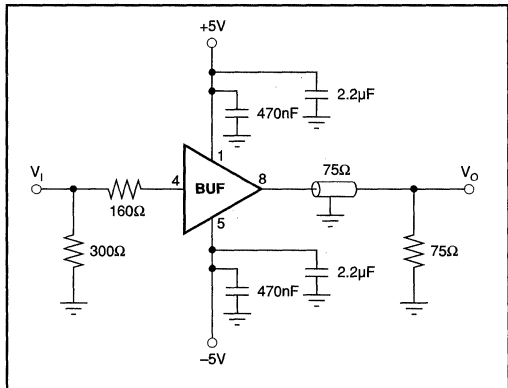


FIGURE 4. Impedance Converter.

VIDEO DISTRIBUTION AMPLIFIER

In this broadcast quality circuit, the OPA623 provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The OPA623 provides a voltage gain of 2.5V/V, while the potentiometer of 200Ω allows the overall gain to be adjusted to drive the standard signal levels into the back-terminated 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated.

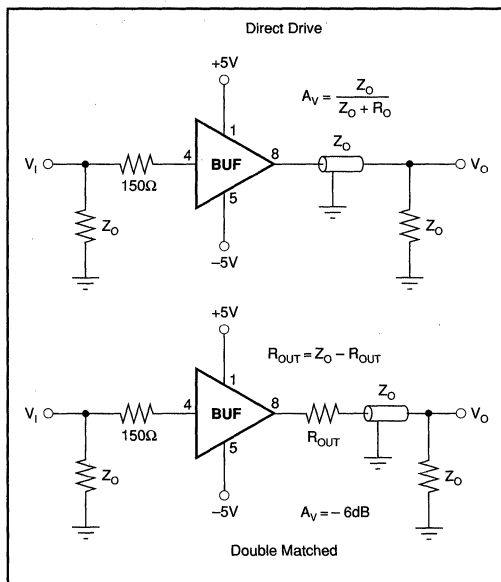
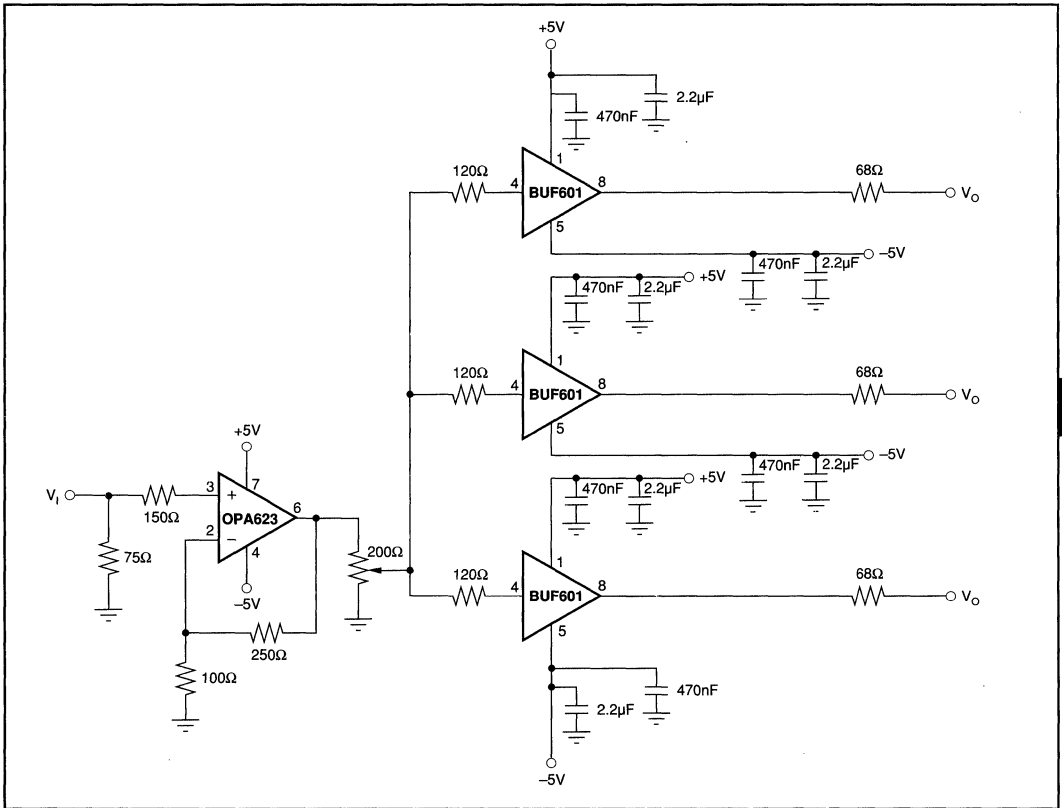


FIGURE 5. Driving Cables.

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BUF600/601

3.1

BUFFER AMPLIFIERS

FIGURE 6. Video Distribution Amplifier.

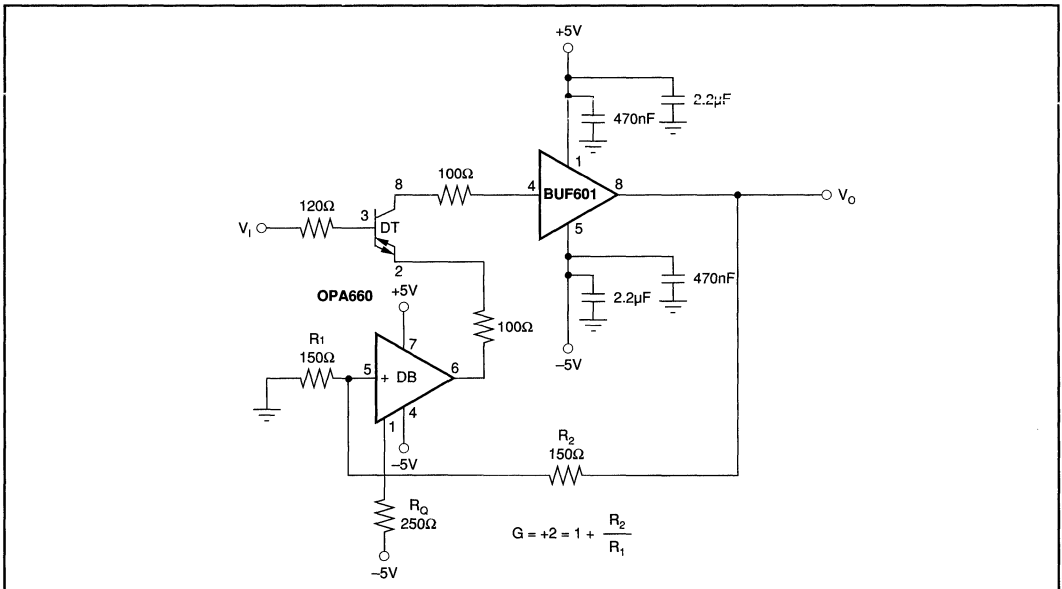


FIGURE 7. Inside a Feedback Loop of a Voltage Feedback Amplifier (BUF601 and OPA660).

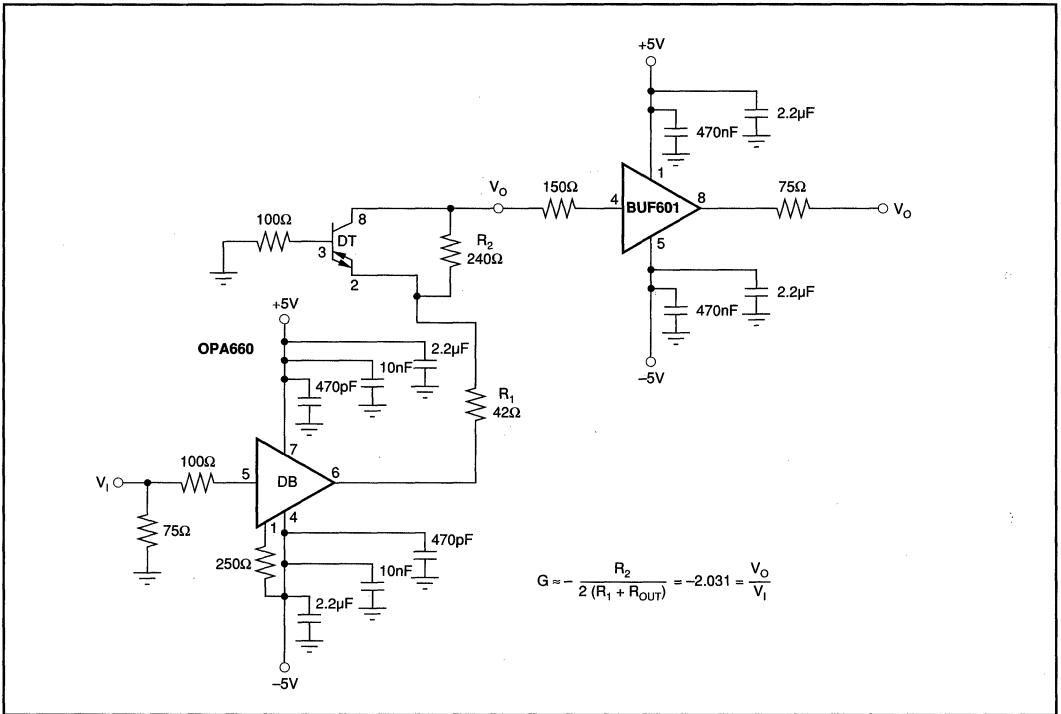


FIGURE 8. Output Buffer for an Inverting RF-Amplifier (Direct Feedback).

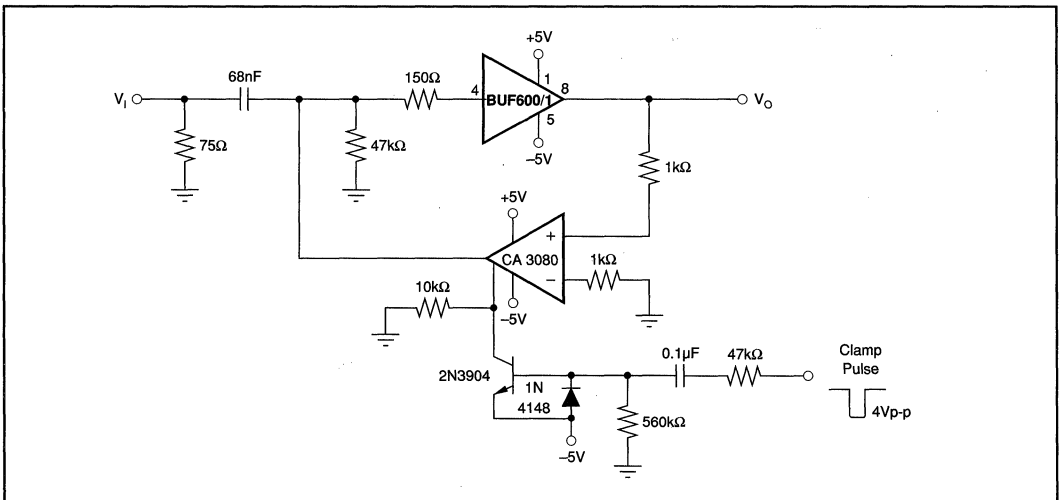


FIGURE 9. Input Amplifier with Baseband Video DC Restoration.

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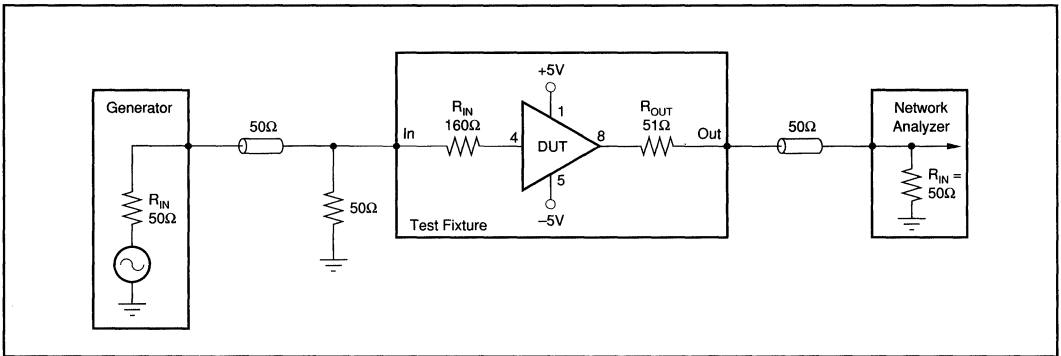


FIGURE 10. Test Circuit Frequency Response.

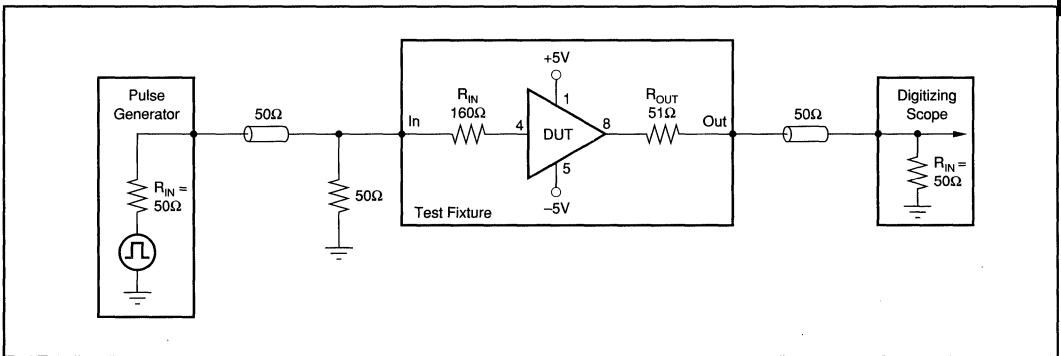


FIGURE 11. Test Circuit Pulse Response.

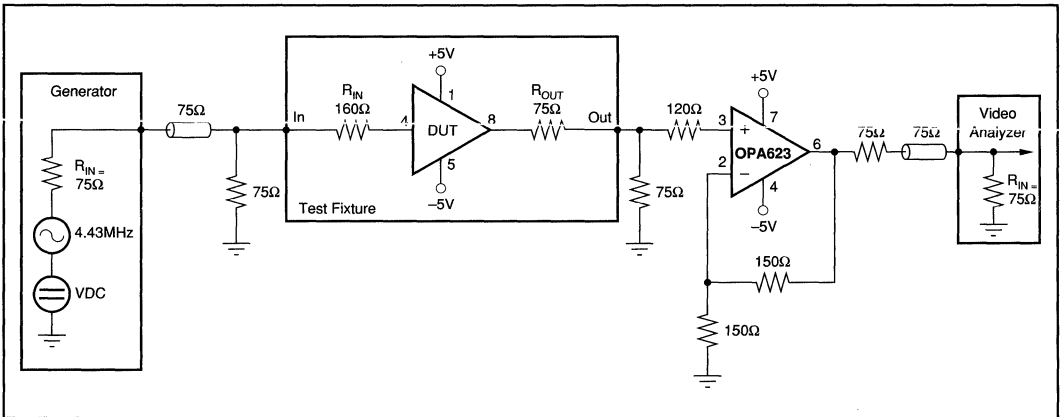


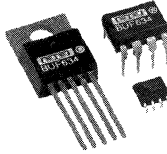
FIGURE 12. Test Circuit Differential Gain and Phase.

BUF600/601

3.1

BUFFER AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson



BUF634

250mA HIGH-SPEED BUFFER

FEATURES

- HIGH OUTPUT CURRENT: 250mA
- SLEW RATE: 2000V/ μ s
- PIN-SELECTED BANDWIDTH: 30MHz/180MHz
- LOW QUIESCENT CURRENT: 1.5mA (30MHz BW)
- WIDE SUPPLY RANGE: ± 2.25 to ± 18 V
- INTERNAL CURRENT LIMIT
- THERMAL SHUT-DOWN
- 8-PIN DIP, SO-8, 5-PIN TO-220 PACKAGES

APPLICATIONS

- VALVE DRIVER
- SOLENOID DRIVER
- OP AMP CURRENT BOOSTER
- LINE DRIVER
- HEADPHONE DRIVER
- VIDEO DRIVER
- MOTOR DRIVER
- TEST EQUIPMENT
- ATE PIN DRIVER

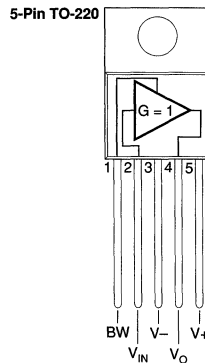
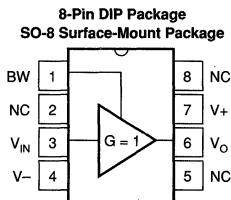
DESCRIPTION

The BUF634 is a high speed unity-gain open-loop buffer recommended for a wide range of applications. It can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback and improve capacitive load drive.

For low power applications, the BUF634 operates on 1.5mA quiescent current with 250mA output and 2000V/ μ s slew rate. Bandwidth is increased from 30MHz to 180MHz by connecting pin 1 to V₋.

Output circuitry is fully protected by internal current limit and thermal shut-down making it rugged and easy to use.

The BUF634 is available in a variety of packages to suit mechanical and power dissipation requirements. Types include 8-pin DIP, SO-8 surface-mount and 5-pin TO-220.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRBCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}^{(1)}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

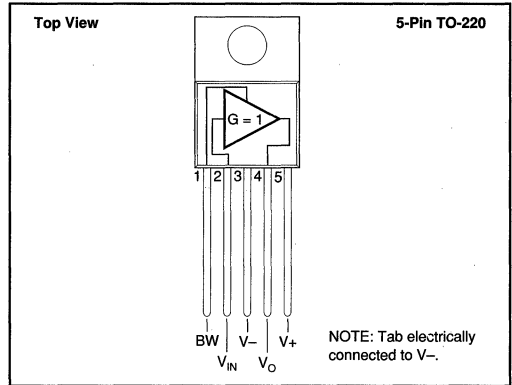
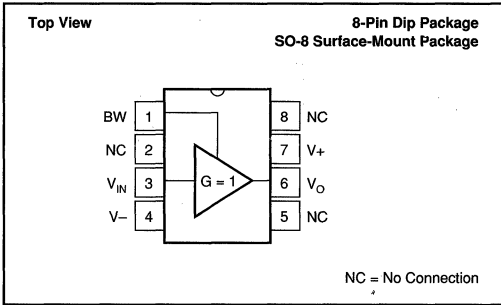
PARAMETER	CONDITION	BUF634P, U, T						UNITS
		LOW QUIESCENT CURRENT MODE			WIDE BANDWIDTH MODE			
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage vs Temperature vs Power Supply	Specified Temperature Range $V_S = \pm 2.25\text{V}^{(2)}$ to $\pm 18\text{V}$		± 30 ± 100	± 100		*	*	mV $\mu\text{V}/^\circ\text{C}$
Input Bias Current	$V_{IN} = 0\text{V}$		0.1	1		*	*	mV/V
Input Impedance	$R_L = 100\Omega$		± 0.5	± 2		± 5	± 20	μA
Noise Voltage	$f = 10\text{kHz}$		$80 \parallel 8$ 4			$8 \parallel 8$		$\text{M}\Omega \parallel \text{pF}$ $\text{nV}/\sqrt{\text{Hz}}$
GAIN	$R_L = 1\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 100\Omega$, $V_O = \pm 10\text{V}$ $R_L = 67\Omega$, $V_O = \pm 10\text{V}$	0.95 0.85 0.8	0.99 0.93 0.9		*	*	*	V/V V/V V/V
OUTPUT								
Current Output, Continuous			± 250		*	*		mA
Voltage Output, Positive	$I_O = 10\text{mA}$	(V+) -2.1	(V+) -1.7		*	*		V
Negative	$I_O = -10\text{mA}$	(V-) +2.1	(V-) +1.8		*	*		V
Positive	$I_O = 100\text{mA}$	(V+) -3	(V+) -2.4		*	*		V
Negative	$I_O = -100\text{mA}$	(V-) +4	(V-) +3.5		*	*		V
Positive	$I_O = 150\text{mA}$	(V+) -4	(V+) -2.8		*	*		V
Negative	$I_O = -150\text{mA}$	(V-) +5	(V-) +4		*	*		V
Short-Circuit Current			± 350	± 550		± 400	*	mA
DYNAMIC RESPONSE								
Bandwidth, -3dB	$R_L = 1\text{k}\Omega$ $R_L = 100\Omega$		30 20			180 160		MHz MHz
Slew Rate	20V-p-p, $R_L = 100\Omega$		2000			*		V/ μs
Settling Time, 0.1%	20V Step, $R_L = 100\Omega$		200			*		ns
1%	20V Step, $R_L = 100\Omega$		50			*		ns
Differential Gain	3.58MHz, $V_O = 0.7\text{V}$, $R_L = 150\Omega$		4			0.4		%
Differential Phase	3.58MHz, $V_O = 0.7\text{V}$, $R_L = 150\Omega$		2.5			0.1		°
POWER SUPPLY								
Specified Operating Voltage			± 15		*	*		V
Operating Voltage Range		$\pm 2.25^{(2)}$		± 18			*	V
Quiescent Current, I_Q	$I_O = 0$		± 1.5	± 2		± 15	± 20	mA
TEMPERATURE RANGE								
Specification		-40		+85	*	*	*	$^\circ\text{C}$
Operating		-40		+125	*	*	*	$^\circ\text{C}$
Storage		-40		+125	*	*	*	$^\circ\text{C}$
Thermal Shutdown								
Temperature, T_J			175			*	*	$^\circ\text{C}$
Thermal Resistance, θ_{JA}	"P" Package ⁽³⁾		100			*	*	$^\circ\text{C}/\text{W}$
θ_{JA}	"U" Package ⁽³⁾		150			*	*	$^\circ\text{C}/\text{W}$
θ_{JA}	"T" Package ⁽³⁾		65			*	*	$^\circ\text{C}/\text{W}$
θ_{JC}	"T" Package		6			*	*	$^\circ\text{C}/\text{W}$

NOTES: (1) Tests are performed on high speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product will cause some parameters to shift when warmed up. See typical performance curves for over-temperature performance. (2) Limited output swing available at low supply voltage. See Output voltage specifications. (3) Typical when all leads are soldered to a circuit board. See text for recommendations.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±V _s
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION⁽¹⁾

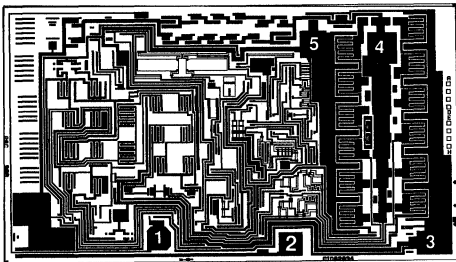
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
BUF634P	8-Pin PDIP	006
BUF634U	SO-8 Surface Mount	182
BUF634T	5-Pin TO-220	315

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
BUF634P	8-Pin Plastic DIP	-40 to +85°C
BUF634U	SO-8 Surface-Mount	-40 to +85°C
BUF634T	5-Pin TO-220	-40 to +85°C

DICE INFORMATION



BUF634 DIE TOPOGRAPHY

PAD	FUNCTION
1	BW
2	V _{IN}
3	V-
4	V _O
5	V+

Substrate Bias: Internally connected to V- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	120 x 70 ±5	3.05 x 1.78 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Chromium-Silver

⚡ ELECTROSTATIC DISCHARGE SENSITIVITY

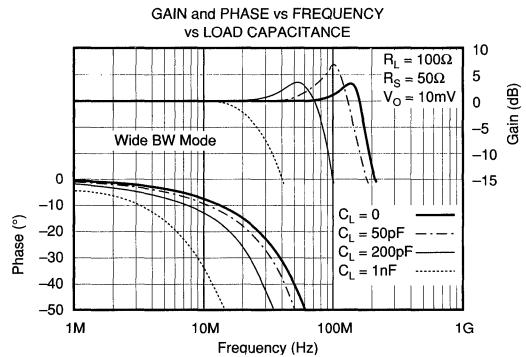
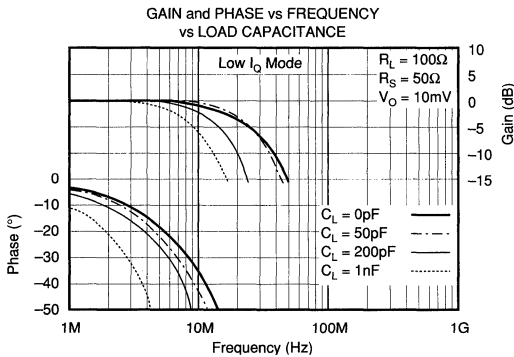
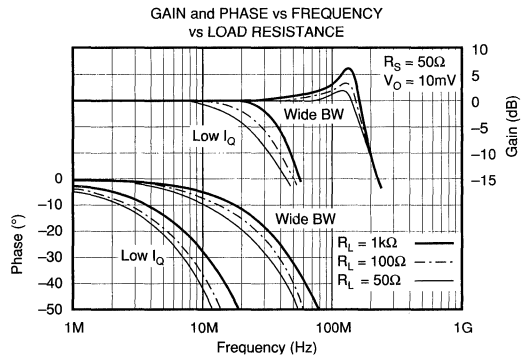
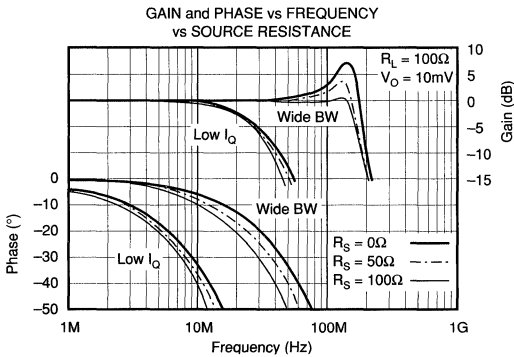
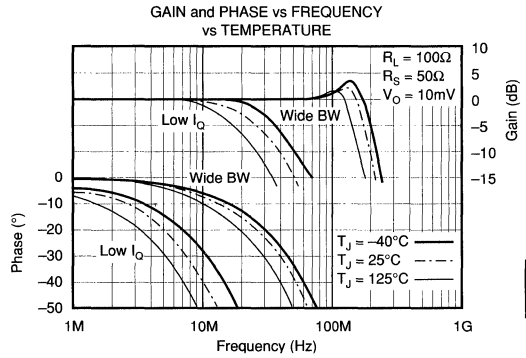
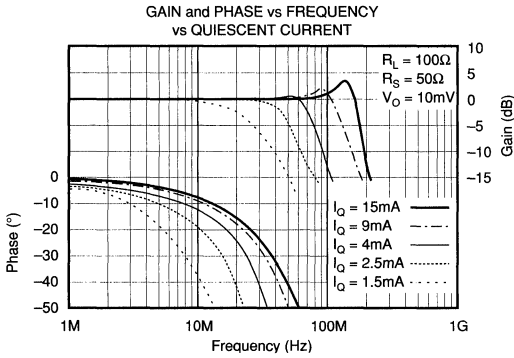
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



BUF634

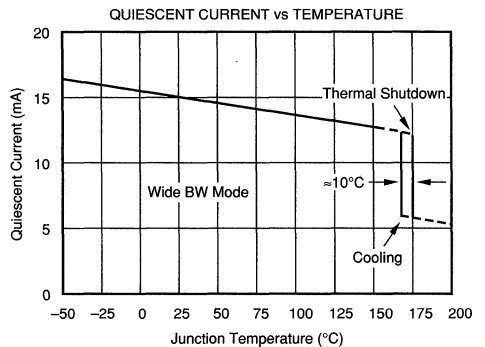
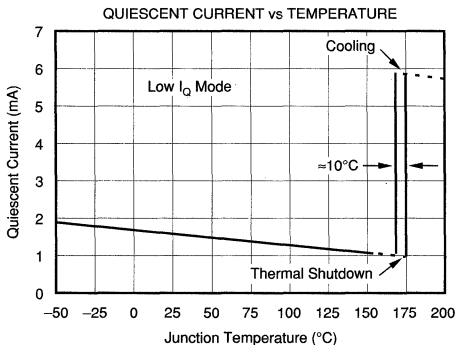
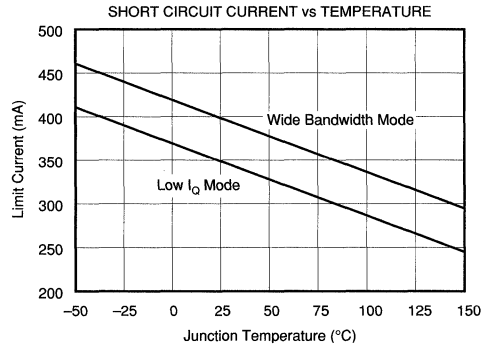
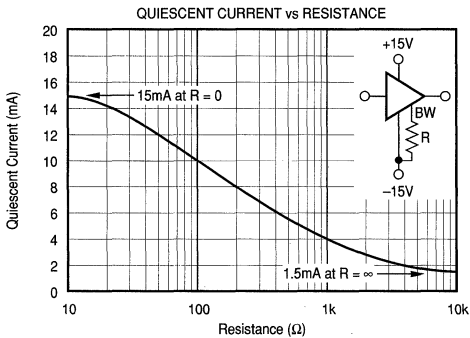
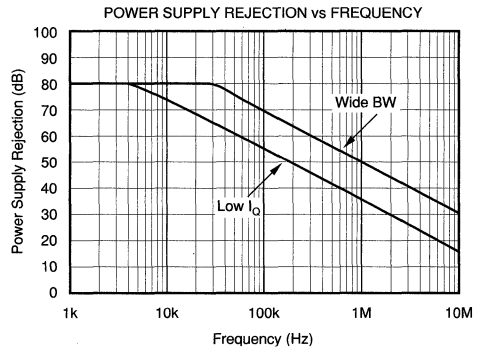
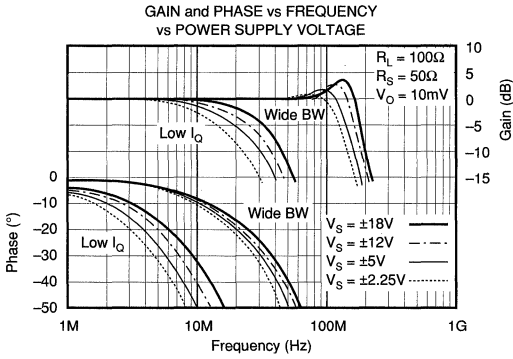
3.1

BUFFER AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

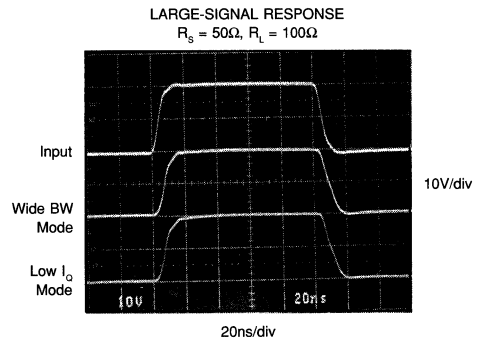
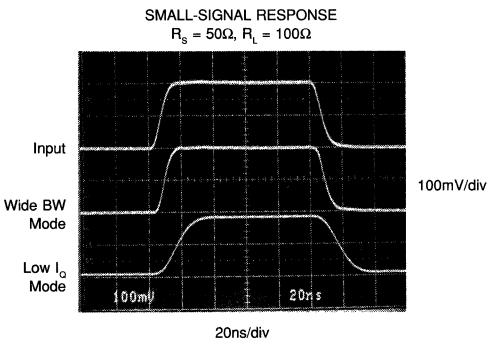
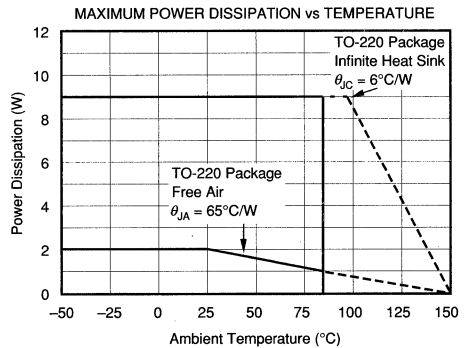
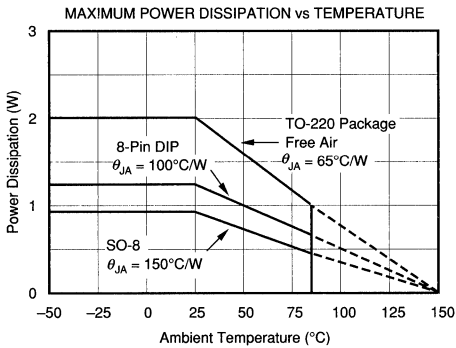
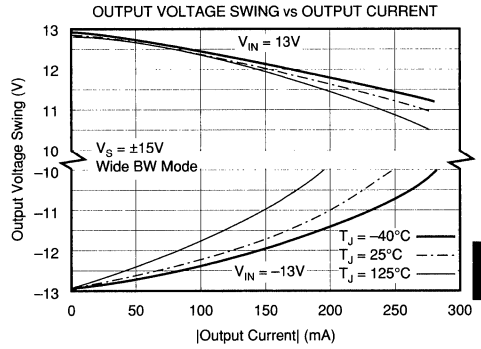
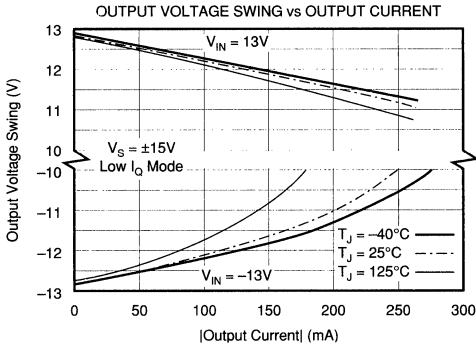
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



BUF634

3.1

BUFFER AMPLIFIERS

APPLICATION INFORMATION

Figure 1 is a simplified circuit diagram of the BUF634 showing its open-loop complementary follower design.

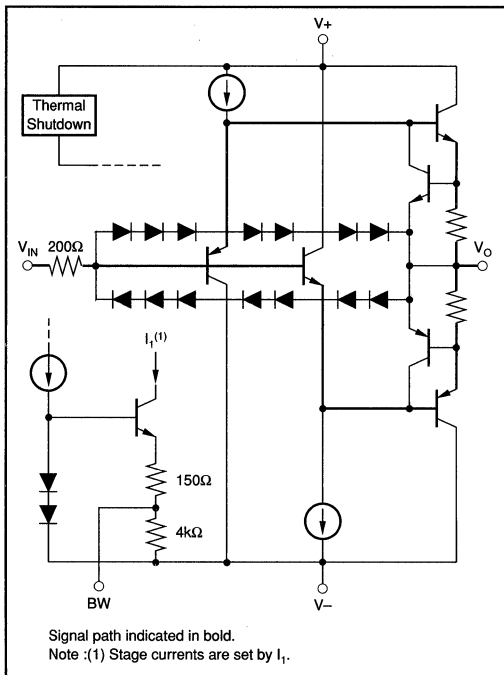


FIGURE 1. Simplified Circuit Diagram.

Figure 2 shows the BUF634 connected as an open-loop buffer. The source impedance and optional input resistor, R_S , influence frequency response—see typical curves. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as $0.1\mu\text{F}$ will assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum $10\mu\text{F}$ capacitors are recommended.

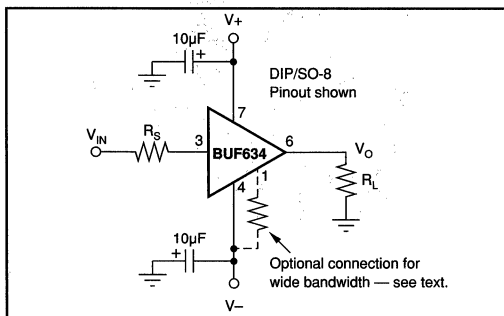


FIGURE 2. Buffer Connections.

High frequency open-loop applications may benefit from special bypassing and layout considerations—see “High Frequency Applications” at end of applications discussion.

OUTPUT CURRENT

The BUF634 can deliver up to $\pm 250\text{mA}$ continuous output current. Internal circuitry limits output current to approximately $\pm 350\text{mA}$ —see typical performance curve “Short Circuit Current vs Temperature”. For many applications, however, the continuous output current will be limited by thermal effects.

The output voltage swing capability varies with junction temperature and output current—see typical curves “Output Voltage Swing vs Output Current.” Although all three package types are tested for the same output performance using a high speed test, the higher junction temperatures with the DIP and SO-8 package types will often provide less output voltage swing. The TO-220 package can be used with a heat sink to reduce junction temperature, allowing maximum possible output swing.

THERMAL PROTECTION

Power dissipated in the BUF634 will cause the junction temperature to rise. A thermal protection circuit in the BUF634 will disable the output when the junction temperature reaches approximately 175°C . When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 6mA during thermal shutdown. When the junction temperature cools to approximately 165°C the output circuitry is again enabled. This can cause the protection circuit to cycle on and off with a period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load and thermal environment.

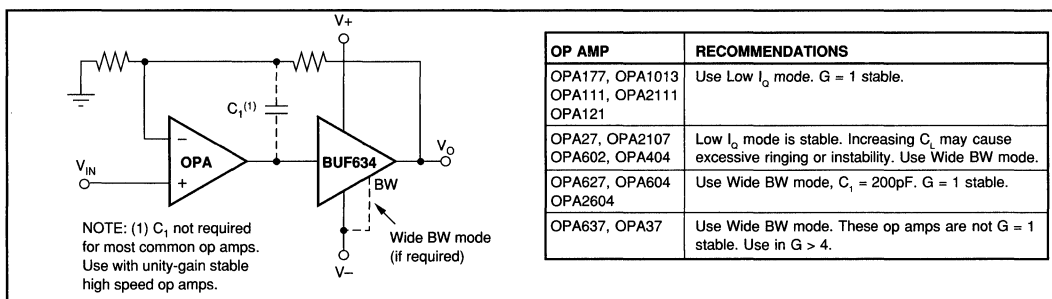
The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

The 5-pin TO-220 package provides best thermal performance. When used with a properly sized heat sink, output of the TO-220 version is not limited by thermal performance. See Application Bulletin AB-037 for details on heat sink calculations. The mounting tab of the TO-220 package is electrically connected to the V^- power supply.

The DIP and SO-8 surface-mount packages are excellent for applications requiring high output current with low average power dissipation.

To achieve the best possible thermal performance with the DIP or SO-8 packages, solder the device directly to a circuit board. Since much of the heat is dissipated by conduction through the package pins, sockets will degrade thermal performance. Use wide circuit board traces on all the device pins, including pins that are not connected. With the DIP package, use traces on both sides of the printed circuit board if possible.

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OP AMP	RECOMMENDATIONS
OPA177, OPA1013 OPA111, OPA2111 OPA121	Use Low I_o mode. $G = 1$ stable.
OPA27, OPA2107 OPA602, OPA404	Low I_o mode is stable. Increasing C_1 may cause excessive ringing or instability. Use Wide BW mode.
OPA627, OPA604 OPA2604	Use Wide BW mode, $C_1 = 200\text{pF}$. $G = 1$ stable.
OPA637, OPA37	Use Wide BW mode. These op amps are not $G = 1$ stable. Use in $G > 4$.

FIGURE 3. Boosting Op Amp Output Current.

POWER DISSIPATION

Power dissipation depends on power supply voltage, signal and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection should trigger more than 45°C above the maximum expected ambient condition of your application.

INPUT CHARACTERISTICS

Internal circuitry is protected with a diode clamp connected from the input to output of the BUF634—see Figure 1. If the output is unable to follow the input within approximately 3V (such as with an output short-circuit), the input will conduct increased current from the input source. This is limited by the internal 200Ω resistor. If the input source can be damaged by this increase in load current, an additional resistor can be connected in series with the input.

BANDWIDTH CONTROL PIN

The -3dB bandwidth of the BUF634 is approximately 30MHz in the low quiescent current mode (1.5mA typical). To select this mode, leave the bandwidth control pin open (no connection).

Bandwidth can be extended to approximately 180MHz by connecting the bandwidth control pin to V-. This increases the quiescent current to approximately 15mA. Intermediate bandwidths can be set by connecting a resistor in series with the bandwidth control pin—see typical curve "Quiescent

Current vs Resistance" for resistor selection. Characteristics of the bandwidth control pin can be seen in the simplified circuit diagram, Figure 1.

The rated output current and slew rate are not affected by the bandwidth control, but the current limit value changes slightly. Output voltage swing is somewhat improved in the wide bandwidth mode. The increased quiescent current when in wide bandwidth mode produces greater power dissipation during low output current conditions. This quiescent power is equal to the total supply voltage, (V+)+|V-|, times the quiescent current.

BOOSTING OP AMP OUTPUT CURRENT

The BUF634 can be connected inside the feedback loop of most op amps to increase output current—see Figure 3. When connected inside the feedback loop, the BUF634's offset voltage and other errors are corrected by the feedback of the op amp.

To assure that the op amp remains stable, the BUF634's phase shift must remain small throughout the loop gain of the circuit. For a $G=+1$ op amp circuit, the BUF634 must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that may affect stability of the op amp—see typical Gain and Phase curves.

Most general-purpose or precision op amps remain unity-gain stable with the BUF634 connected inside the feedback loop as shown. Large capacitive loads may require the BUF634 to be connected for wide bandwidth for stable operation. High speed or fast-settling op amps generally require the wide bandwidth mode to remain stable and to assure good dynamic performance. To check for stability with an op amp, look for oscillations or excessive ringing on signal pulses with the intended load and worst case conditions that affect phase response of the buffer.

HIGH FREQUENCY APPLICATIONS

The BUF634's excellent bandwidth and fast slew rate make it useful in a variety of high frequency open-loop applications. When operated open-loop, circuit board layout and bypassing technique can affect dynamic performance.

For best results, use a ground plane type circuit board layout and bypass the power supplies with 0.1μF ceramic chip

BUF634

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BUFFER AMPLIFIERS

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capacitors at the device pins. Source resistance will affect high-frequency peaking and step response overshoot and ringing. Best response is usually achieved with a series input resistor of 25Ω to 200Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10Ω to 150Ω in series with the output.

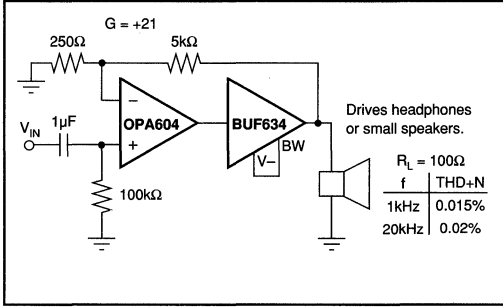


FIGURE 4. High Performance Headphone Driver.

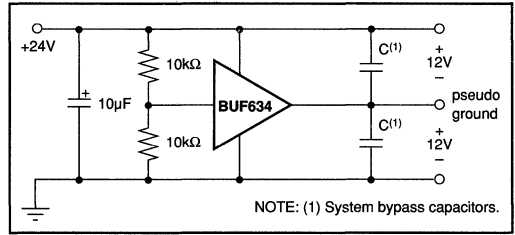


FIGURE 5. Pseudo-Ground Driver.

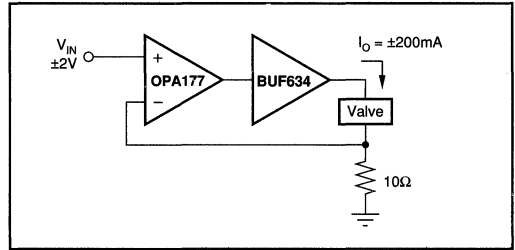


FIGURE 6. Current-Output Valve Driver.

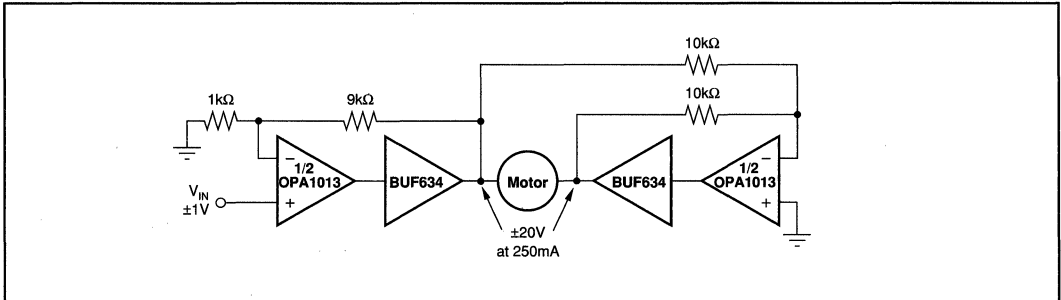


FIGURE 7. Bridge-Connected Motor Driver.

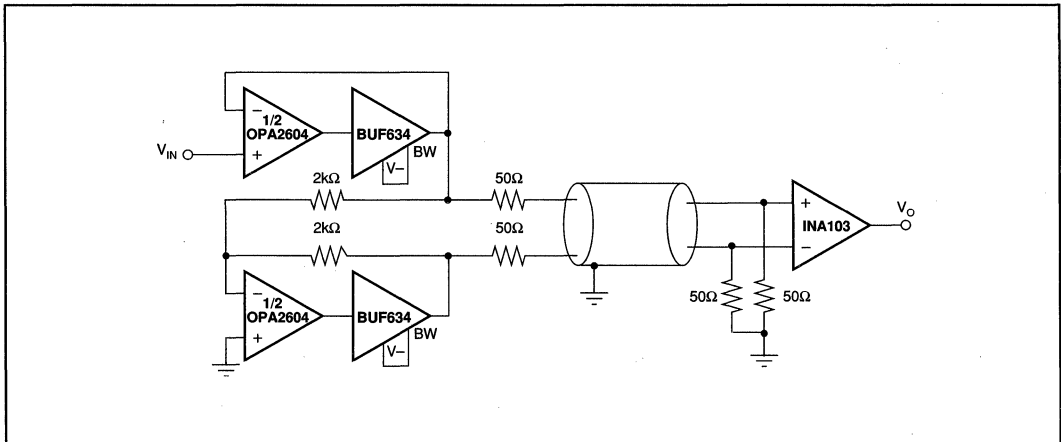
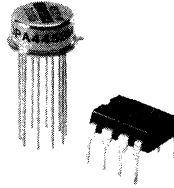


FIGURE 8. Differential Line Driver.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA445

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY RANGE: $\pm 10V$ to $\pm 45V$
- HIGH SLEW RATE: $10V/\mu s$
- LOW INPUT BIAS CURRENT: $50pA$ max
- STANDARD-PINOUT TO-99 AND DIP PACKAGES

APPLICATIONS

- TEST EQUIPMENT
- HIGH VOLTAGE REGULATORS
- POWER AMPLIFIERS
- DATA ACQUISITION
- SIGNAL CONDITIONING

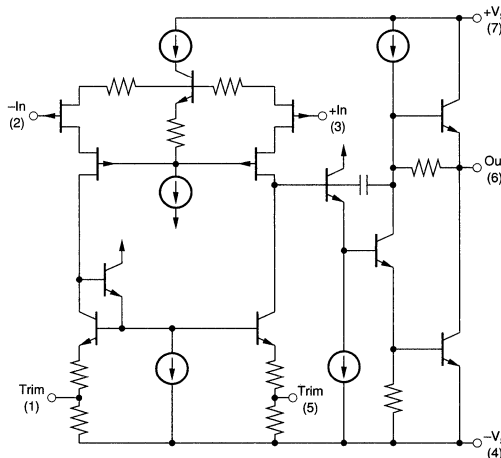
DESCRIPTION

The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to $\pm 45V$ and output currents of $15mA$. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high voltage applications. FET input circuitry allows the

use of high impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is unity-gain stable and requires no external compensation components. It is available in both industrial ($-25^{\circ}C$ to $+85^{\circ}C$) and military ($-55^{\circ}C$ to $+125^{\circ}C$) temperature ranges.



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PDS-754C

3.2.27

OPA445

3.2

POWER OPERATIONAL AMPLIFIERS

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SPECIFICATIONS

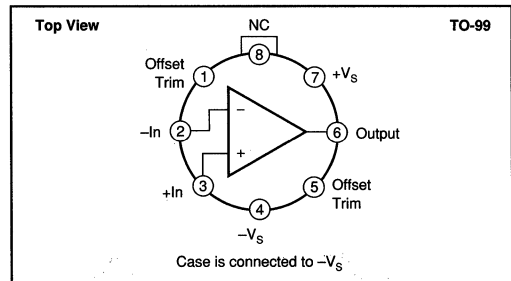
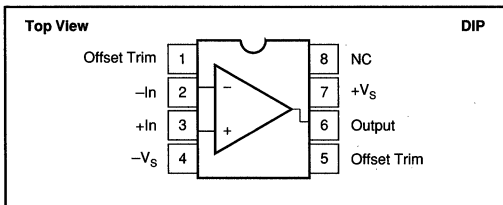
ELECTRICAL

At $V_s = \pm 40^\circ\text{C}$ and $T_A = +25^\circ\text{C}$, unless otherwise specified.

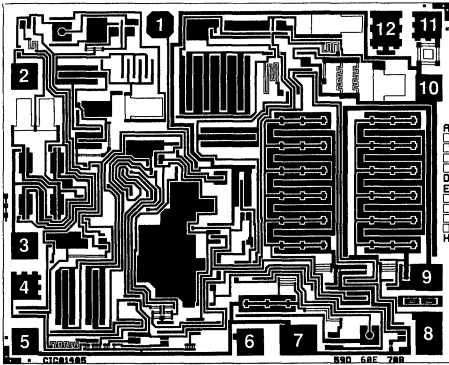
PARAMETER	CONDITIONS	OPA445SM			OPA445BM			OPA445AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
OFFSET VOLTAGE											
Input Offset Voltage	$V_{CM} = 0\text{V}$		0.5	1.0		1.0	3.0		2.0	5.0	mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}	*	*			10		*	15		$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_s = \pm 10\text{V}$ to $\pm 50\text{V}$	*	*		80	110		*	*		dB
BIAS CURRENT											
Input Bias Current	$V_{CM} = 0\text{V}$		*	*		20	50		50	100	pA
Over Temperature				100			10			20	nA
OFFSET CURRENT											
Input Offset Current	$V_{CM} = 0\text{V}$		*	*		4	10		20	40	pA
Over Temperature				50			5			10	nA
IMPEDANCE											
Differential			*	*		$10^{13} \parallel 1$			*		$\Omega \parallel \text{pF}$
Common-Mode			*	*		$10^{14} \parallel 3$			*		$\Omega \parallel \text{pF}$
VOLTAGE RANGE											
Common-Mode Input Range		*			± 35			*			V
Common-Mode Rejection	$V_{IN} = \pm 30\text{V}$, Over Temp.	*	*		80	95		*	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L = 5\text{k}\Omega$	*	*		100	105		*	*		dB
Over Temperature		*	*		97			*	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Small Signal	*	*			2		*	*		MHz
Full Power Response	35Vp-p, $R_L = 5\text{k}\Omega$	*	*		45	55		*	*		kHz
DYNAMIC RESPONSE											
Slew Rate	$V_o = \pm 35\text{V}$, $R_L = 5\text{k}\Omega$	*	*		5	10		*	*		V/ μs
Rise Time	$V_o = \pm 200\text{mV}$	*	*			100		*	*		ns
Overshoot	$A_v = +1$ $Z_L = 5\text{k}\Omega \parallel 50\text{pF}$	*	*			30		*	*		%
OUTPUT											
Voltage Output, Over Temp.	$R_L = 5\text{k}\Omega$	*			± 35			*			V
Current Output	$V_o = \pm 28\text{V}$	*			± 15			*			mA
Output Resistance	DC, Open Loop		*			220			*		Ω
Short Circuit Current			*			± 26			*		mA
POWER SUPPLY											
Rated Voltage, $\pm V_s$			*			± 40			*		V
Voltage Range, $\pm V_s$			*						*		V
Derated Performance	Over Temperature	*	*		± 10			*	*		V
Current, Quiescent	$I_o = 0\text{mA}$		*			3.8	± 45		*	*	mA
			*				4.5		*	*	mA
TEMPERATURE RANGE											
Specification		-55		+125	-25		+85	*		*	$^\circ\text{C}$
Operating	Ambient Temperature	*		*	-55		+125	-25		+85	$^\circ\text{C}$
θ Junction-Ambient			*			200			100		$^\circ\text{C}/\text{W}$

*Specifications same as OPA445BM.

CONNECTION DIAGRAMS



DICE INFORMATION



OPA445 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	7	-V _S
2	-In	8	(Compensation)
3	+In	9	Output
4	NC	10	+V _S
5	-V _S	11	NC
6	Offset Trim	12	NC

Substrate Bias: Electrically connected to -V_S supply.
NC: No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	88 x 72 ±5	2.24 x 1.83 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Chromium-Silver	

ABSOLUTE MAXIMUM RATINGS

Power Supply	±50V
Internal Power Dissipation	680mW
Differential Input Voltage	±80V
Input Voltage Range	±V _{in} -3V
Storage Temperature Range: M	-65°C to +150°C
P	-40°C to +85°C
Operating Temperature Range: M	-55°C to +125°C
P	-40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit to Ground (T _A = +25°C)	Continuous
Junction Temperature	+175°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA445AP	8-pin plastic DIP	-25°C to +85°C
OPA445BM	8-pin TO-99	-25°C to +85°C
OPA445SM	8-pin TO-99	-55°C to +125°C

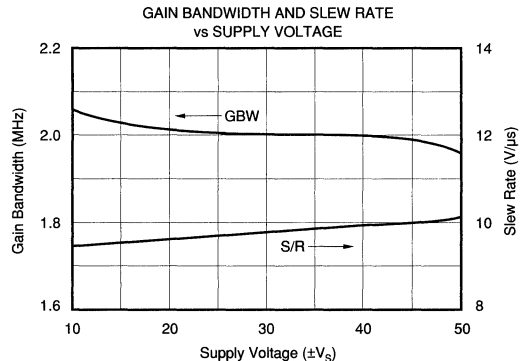
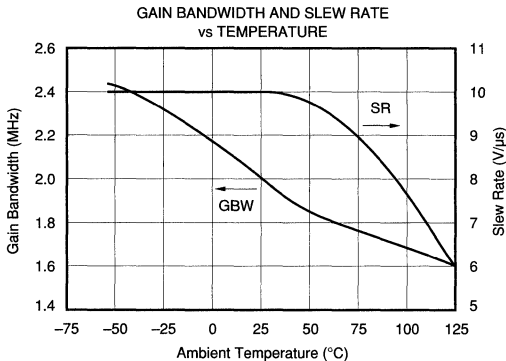
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA445AP	8-pin plastic DIP	006
OPA445BM	8-pin TO-99	001
OPA445SM	8-pin TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

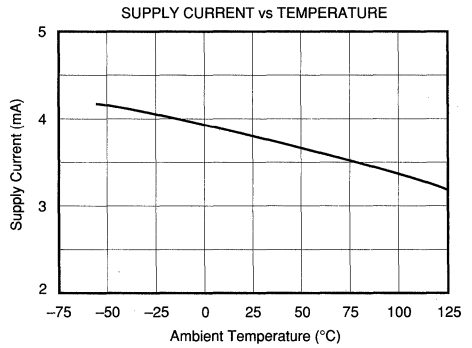
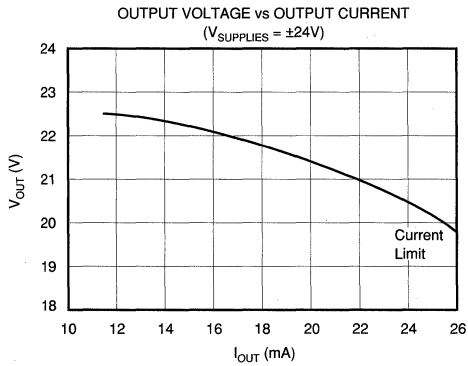
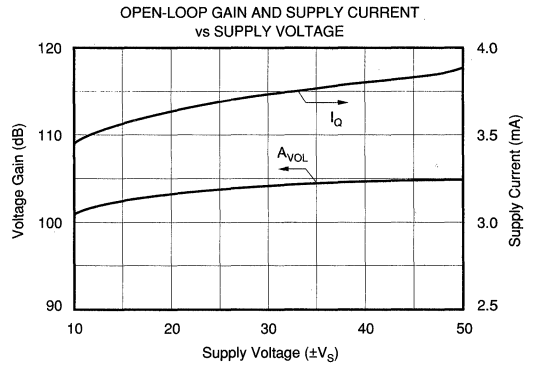
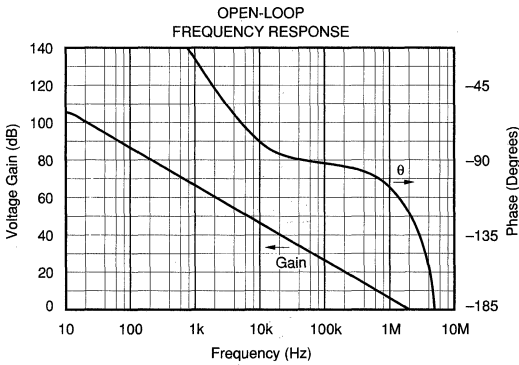
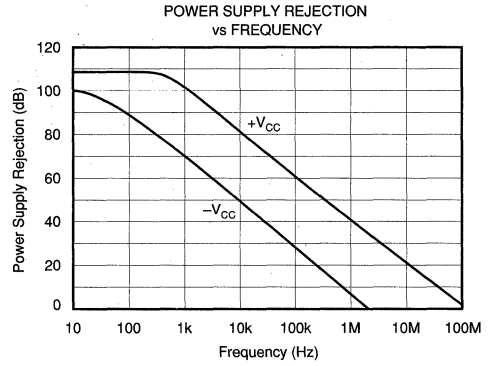
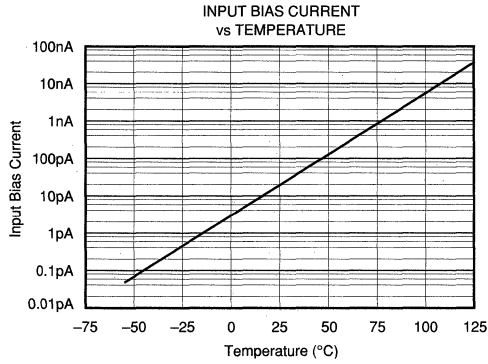
T_A = +25°C, V_S = ±40VDC, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

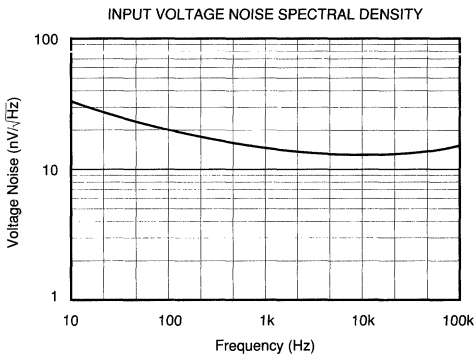
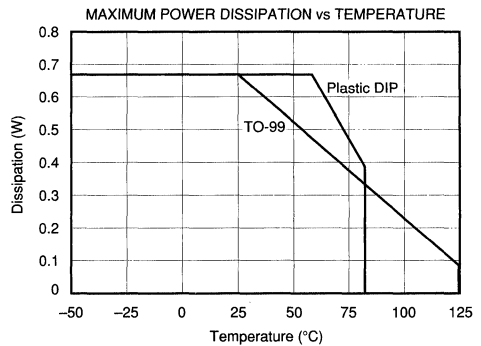
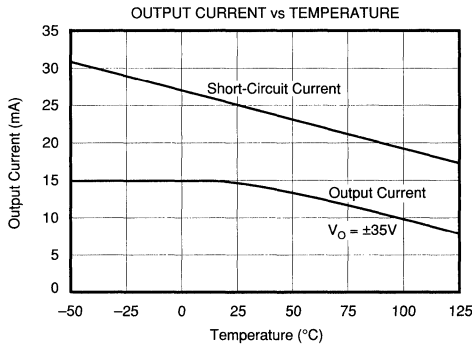
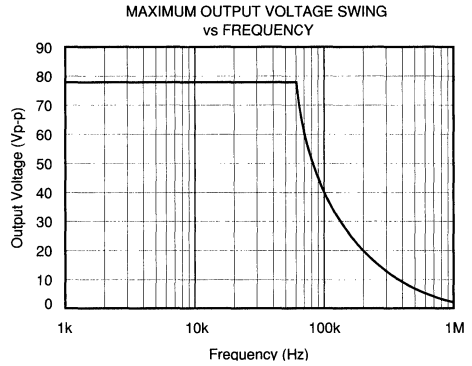
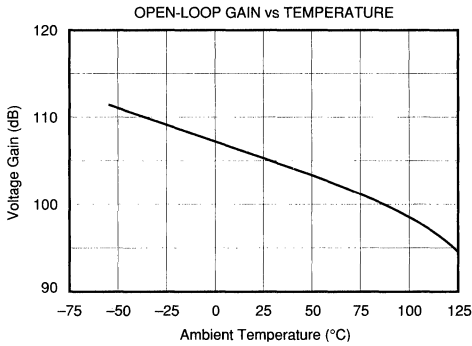
$T_A = +25^\circ\text{C}$, $V_S = \pm 40\text{VDC}$, unless otherwise noted.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$ unless otherwise noted.



OPA445

3.2

POWER OPERATIONAL AMPLIFIERS

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INSTALLATION AND OPERATING INSTRUCTIONS

The OPA445 may be operated from power supplies up to $\pm 45\text{V}$ or a total of 90V . Power supplies should be bypassed with $0.022\mu\text{F}$ capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the supply voltage used.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from $\pm 15\text{V}$ supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a larger voltage is impressed across the conducting output transistor.

Dissipation should be limited to 680mW at 25°C . At temperatures above 25°C , the maximum dissipation should be derated according to the thermal resistance of the package type used.

Package thermal resistance, θ_{IC} , is affected by mounting techniques and environments. The figures provided are typical for common mounting configurations with convection air flow. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks can reduce the thermal resistance of the TO-99 metal package by as much as $50^\circ\text{C}/\text{W}$.

A short-circuit to ground will produce a typical output current of 25mA . With $\pm 40\text{V}$ power supplies, this creates an internal power dissipation of 1.0W . This exceeds the maximum rating for the device, and is not recommended. Permanent damage is unlikely, however, since the short-circuit output current will diminish as the junction temperature rises.

TYPICAL APPLICATIONS

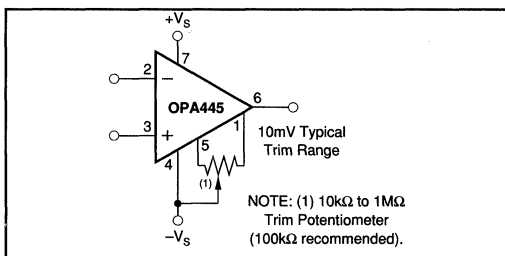


FIGURE 1. Offset Voltage Trim.

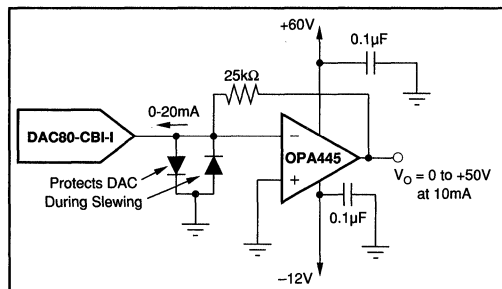


FIGURE 3. Programmable Voltage Source.

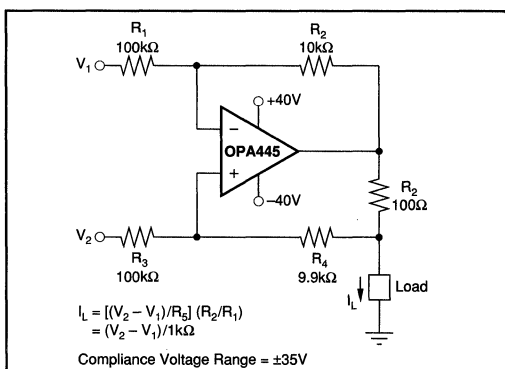
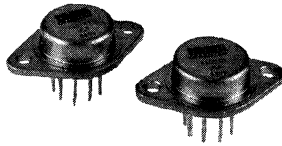


FIGURE 2. Voltage-to-Current Converter.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



OPA501

High Current, High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: $\pm 10A$ Peak
- WIDE POWER SUPPLY RANGE:
 ± 10 to $\pm 40V$
- LOW QUIESCENT CURRENT: 2.6mA
- ISOLATED CASE TO-3 PACKAGE

APPLICATIONS

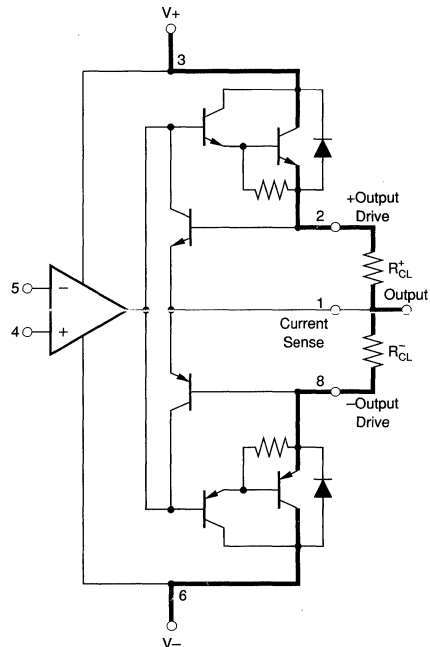
- MOTOR DRIVER
- SERVO AMPLIFIER
- VALVE ACTUATOR
- SYNCRO DRIVER
- PROGRAMMABLE POWER SUPPLY

DESCRIPTION

The OPA501 is a high output current operational amplifier. It can be used in virtually all common op amp circuits, yet is capable of output currents up to $\pm 10A$. Power supply voltages up to $\pm 40V$ allow very high output power for driving motors or other electro-mechanical loads.

Safe operating area is fully specified, and user-set current limits provide protection for both the amplifier and load. The class-B (zero output stage bias) provides low quiescent current during small-signal conditions.

This rugged hybrid integrated circuit is packaged in a metal 8-pin TO-3 package. Both industrial and military temperature range models are available.



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SPECIFICATIONS

ELECTRICAL

At $T_C = +25^\circ\text{C}$, $V_S = \pm 28\text{V}$, (OPA501RM, AM); $V_S = \pm 34\text{V}$ (OPA501SM, BM) unless otherwise noted.

PARAMETER	CONDITIONS	OPA501RM, AM			OPA501SM, BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RATED OUTPUT ^(1, 2)								
Output Current	$R_L = 2\Omega$ (RM, AM)	± 10			*			A
Continuous ⁽³⁾	$R_L = 2.6\Omega$ (SM, BM)	± 10			*			A
Output Voltage ⁽³⁾	$I_O = 10\text{A peak}$	± 20	± 23		± 26	± 29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	$V_O = 40\text{Vp-p}$, $R_L = 8\Omega$	10	16		*	*		kHz
Slew Rate	$R_L = 5\Omega$ (RM, AM)	1.35			*			V/ μs
	$R_L = 6.5\Omega$ (SM, BM)	1.35			*			V/ μs
INPUT OFFSET VOLTAGE								
Initial Offset			± 5	± 10		± 2	± 5	mV
vs Temperature	$-25^\circ\text{C} < T < +85^\circ\text{C}$ (AM, BM)		± 10	± 65				$\mu\text{V}/^\circ\text{C}$
vs Supply Voltage	$-55^\circ\text{C} < T < +125^\circ\text{C}$ (RM, SM)		± 35			± 10	± 40	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT								
Initial	$T_{\text{CASE}} = +25^\circ\text{C}$		15	40		*	20	nA
vs Temperature			± 0.05			*		$\text{nA}/^\circ\text{C}$
vs Supply Voltage			± 0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	$T_{\text{CASE}} = +25^\circ\text{C}$		± 5	± 10		± 2	± 3	nA
vs Temperature	$-25^\circ\text{C} < T < +85^\circ\text{C}$ (AM, BM)		± 0.01					$\text{nA}/^\circ\text{C}$
	$-55^\circ\text{C} < T < +125^\circ\text{C}$ (RM, SM)					± 0.01		$\text{nA}/^\circ\text{C}$
OPEN-LOOP GAIN, DC								
$R_L = 6.5\Omega$ (SM, BM)	$R_L = 5\Omega$ (RM, AM)	94	115		98	115		dB
								dB
INPUT IMPEDANCE								
Differential			10			*		M Ω
Common-mode			250			*		M Ω
INPUT NOISE								
Voltage Noise	$f_n = 0.3\text{Hz to } 10\text{Hz}$		3		*	*		$\mu\text{Vp-p}$
	$f_n = 10\text{Hz to } 10\text{kHz}$	5			*	*	μVrms	
Current Noise	$f_n = 0.3\text{Hz to } 10\text{Hz}$		20		*	*		pA p-p
	$f_n = 10\text{Hz to } 10\text{kHz}$	4.5			*	*	pArms	
INPUT VOLTAGE RANGE								
Common-mode Voltage ⁽⁴⁾	Linear Operation	$\pm(V_S -6)$	$\pm(V_S -3)$		*	*		V
Common-mode Rejection	$f = \text{DC}$, $V_{\text{CM}} = \pm(V_S -6)$	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			± 28	± 36	*	± 34		V
Operating Voltage Range		± 10		± 10			± 40	V
Current, quiescent			± 2.6			*	*	mA
TEMPERATURE RANGE								
Specification, RM, SM	case	-55		+125	*		*	$^\circ\text{C}$
AM, BM		-25		+85	*		*	$^\circ\text{C}$
Operating, derated					*		*	$^\circ\text{C}$
performance, AM, BM		-55		+125	*		*	$^\circ\text{C}$
Storage		-65		+150	*		*	$^\circ\text{C}$
THERMAL RESISTANCE								
	Steady State θ_{JC}		2.0	2.2		*	*	$^\circ\text{C}/\text{W}$

*Specification same as for OPA501RM, AM.

NOTES: (1) Package must be derated based on a junction-to-case thermal resistance of $2.2^\circ\text{C}/\text{W}$ or a junction-to-ambient thermal resistance of $30^\circ\text{C}/\text{W}$. (2) Safe Operating Area and Power Derating Curves must be observed. (3) With $\pm R_{\text{SC}} = 0$. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed. (4) The absolute maximum voltage is 3V less than supply voltage.

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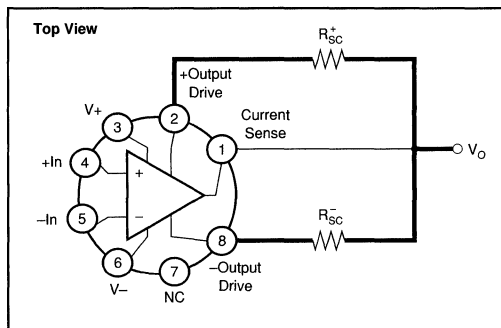
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ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (V_S)	$\pm 40V$
Power Dissipation at +25°C ^(1,2)	79W
Differential Input Voltage	$\pm V_S - 3V$
Common-Mode Input Voltage	$\pm V_S$
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+200°C
Output Short-Circuit Duration ⁽³⁾	Continuous

NOTES: (1) At case temperature of +25°C. Derate at 2.2°C/W above case temperature of +25°C. (2) Average dissipation. (3) Within safe operating area and with appropriate derating.

CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA501AM	8-Pin Metal TO-3	-25°C to +85°C
OPA501BM	8-Pin Metal TO-3	-25°C to +85°C
OPA501RM	8-Pin Metal TO-3	-55°C to +125°C
OPA501SM	8-Pin Metal TO-3	-55°C to +125°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA501AM	8-Pin Metal TO-3	030
OPA501BM	8-Pin Metal TO-3	030
OPA501RM	8-Pin Metal TO-3	030
OPA501SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

OPA501

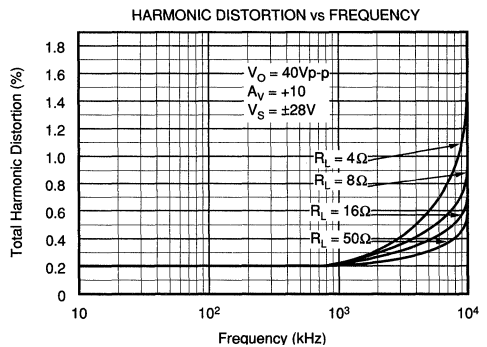
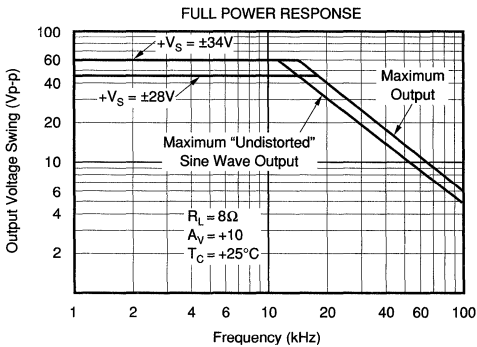
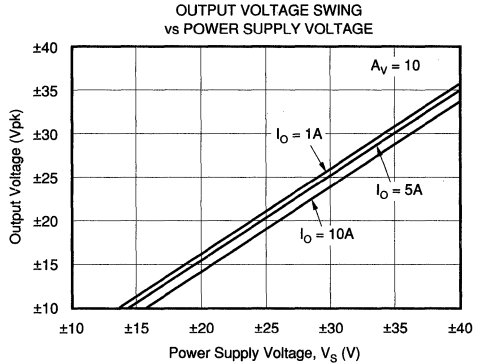
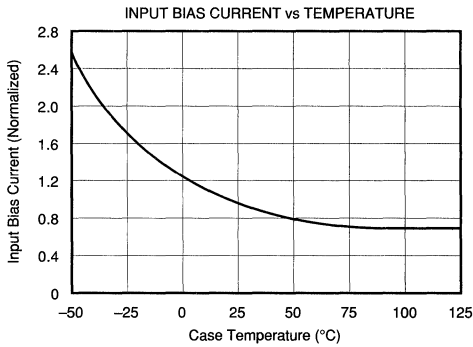
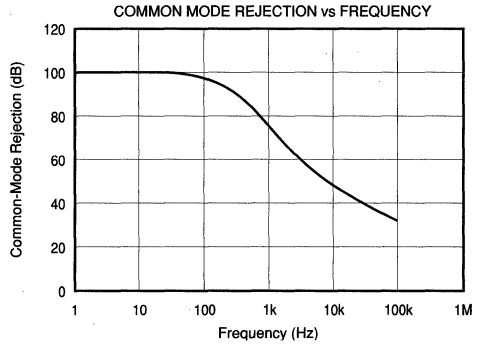
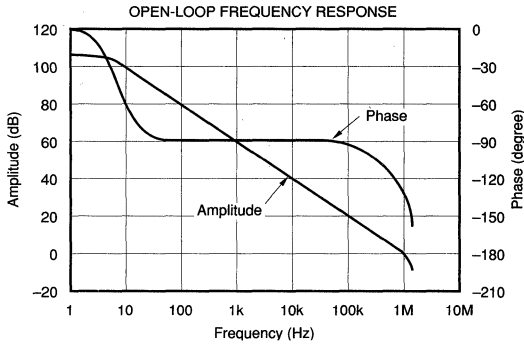
3.2

POWER OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES

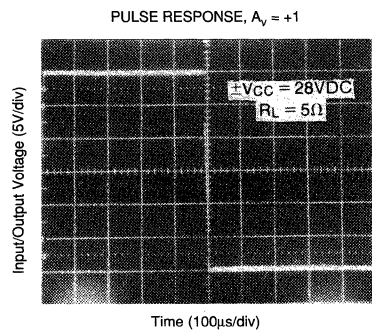
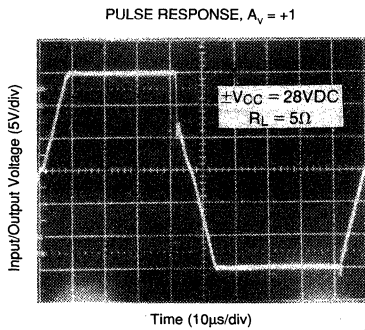
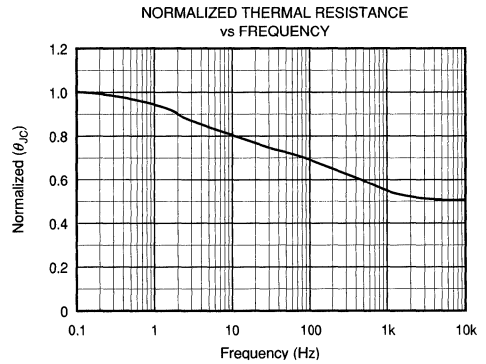
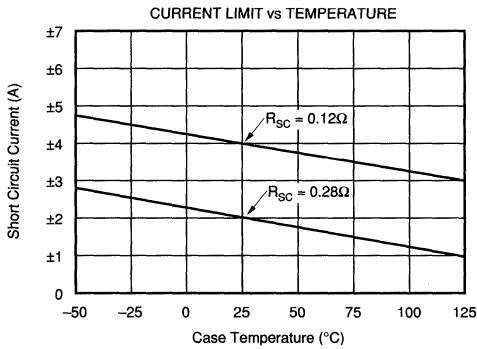
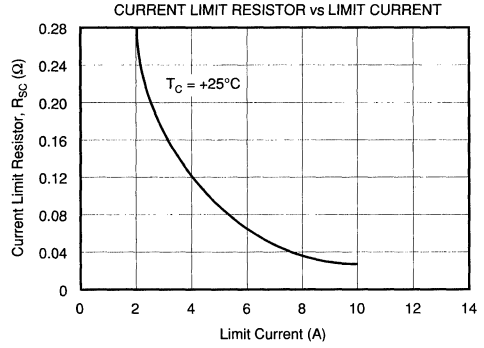
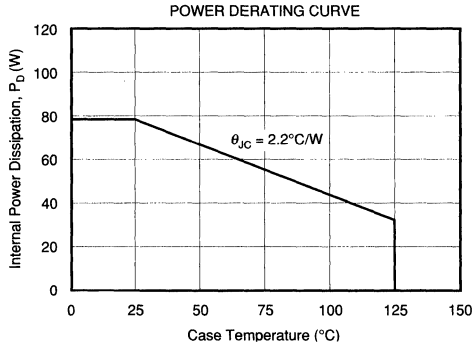
Typical at +25°C case and $\pm V_S = 28\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

Typical at +25°C case and $\pm V_o = 28\text{VDC}$, unless otherwise noted.



OPA501

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POWER OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

Grounding techniques can greatly affect the performance of a power op amp. Figure 1 shows grounds connected so that load current does not flow through signal ground connections. Power supply and load connections should be physically separated from the amplifier input and signal connections.

Power supply connections to the amplifier should be bypassed with 10μF tantalum capacitors connected close to the device pins. The capacitors should be connected to load ground as shown.

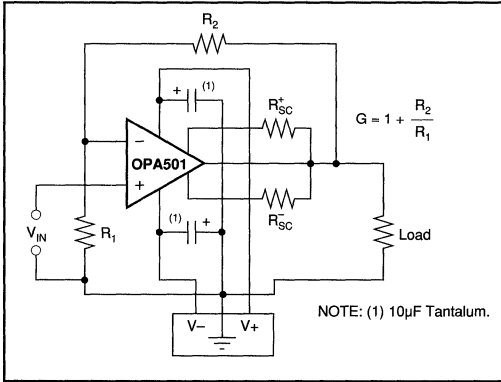


FIGURE 1. Basic Circuit Connections.

CURRENT LIMITS

The OPA501 has independent positive and negative current limit circuits. Current limits are set by the value of R_{SC}^+ and R_{SC}^- . The approximate value of these resistors is:

$$R_{SC} = \frac{0.65}{I_{LIMIT}} - 0.0437\Omega$$

I_{LIMIT} is the desired maximum current at room temperature in Amperes and R_{SC} is in ohms. The current limit value decreases with increasing temperature—see typical performance curves. The current limit resistors conduct the full amplifier output current. Power dissipation of the current limit resistors at maximum current is:

$$P_{MAX} = (I_{LIMIT})^2 R_{SC}$$

The current limit resistors can be chosen from a variety of types. Most wire-wound types are satisfactory, although some physically large resistors may have excessive inductance which can cause instability.

SAFE OPERATING AREA

Stress on the output transistor is determined by the output current and the voltage across the conducting output transistor. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE} . The Safe Operating Area (SOA),

Figure 2, shows the permissible range of voltage and current. SOA is reduced at high operating temperature—see Figure 3.

The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding. A short-circuit to ground forces the full power supply voltage (positive or negative side) across the conducting transistor. With $V_S = \pm 30V$, the current limit must be set for 2A to be safe for short-circuit to ground. For further information on SOA and evaluating signal and load conditions, consult Applications Bulletin AB-039.

HEAT SINKING

Most applications require a heat sink to assure that the maximum junction temperature of 200°C is not exceeded. The size of the heat sink required depends on the power dissipated by the amplifier and ambient temperature conditions. Application Bulletin AB-039 explains how to find maximum power dissipation for dc, ac, reactive loads, and other conditions. Applications Bulletin AB-038 shows how to determine heat sink requirements.

The case of the OPA501 is isolated from all circuitry and can be fastened directly to a heat sink. This eliminates cumbersome insulating hardware that degrades thermal performance. See Applications Bulletin AB-037 for information on mounting techniques and procedures.

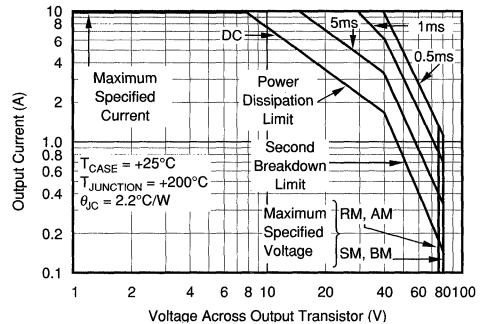


FIGURE 2. Transistor Safe Operating Area at +25°C Case Temperature.

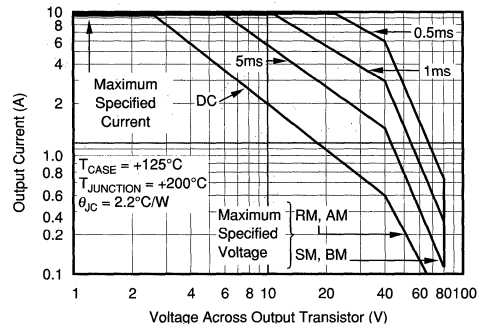
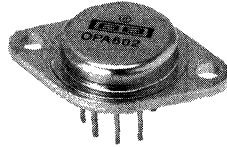


FIGURE 3. Transistor Safe Operating Area at +125°C Case Temperature.



OPA502

High Current, High Power OPERATIONAL AMPLIFIER

OPA502

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FEATURES

- HIGH OUTPUT CURRENT: 10A
- WIDE POWER SUPPLY VOLTAGE: $\pm 10V$ to $\pm 45V$
- USER-SET CURRENT LIMIT
- SLEW RATE: $10V/\mu s$
- FET INPUT: $I_B = 200pA$ max
- CLASS A/B OUTPUT STAGE
- QUIESCENT CURRENT: 25mA max
- HERMETIC TO-3 PACKAGE — ISOLATED CASE

APPLICATIONS

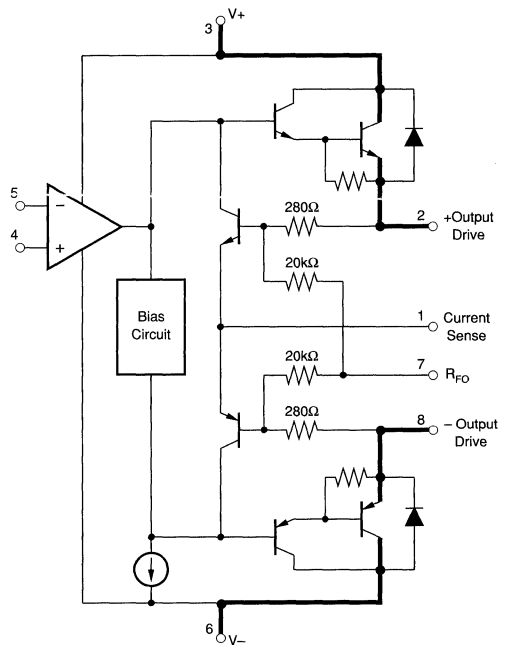
- MOTOR DRIVER
- SERVO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- ACTUATOR DRIVER
- AUDIO AMPLIFIER
- TEST EQUIPMENT

DESCRIPTION

The OPA502 is a high output current operational amplifier designed to drive a wide range of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from crossover distortion. Resistor-programmable current limits provide protection for both the amplifier and the load during abnormal operating conditions. An adjustable foldover current limit can also be used to protect against potentially damaging conditions.

The OPA502 employs a custom monolithic op amp/driver circuit and rugged complementary output transistors, providing excellent DC and dynamic performance.

The industry-standard 8-pin TO-3 package is electrically isolated from all circuitry. This allows the OPA502 to be mounted directly to a heat sink without cumbersome insulating hardware which degrade thermal performance. The OPA502 is available in $-40^\circ C$ to $+85^\circ C$ and $-55^\circ C$ to $+125^\circ C$ temperature ranges.



POWER OPERATIONAL AMPLIFIERS



For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 40V$ unless otherwise noted.

PARAMETER	CONDITION	OPA502BM			OPA502SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply	Specified Temp. Range $V_S = \pm 10V$ to $\pm 45V$		± 0.5 ± 5 74	± 5 92		*	*	mV $\mu V/^{\circ}C$ dB
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current Input Offset Current	$V_{CM} = 0V$ $V_{CM} = 0V$		12 ± 3	200		*	*	pA pA
NOISE Input Voltage Noise Noise Density, Current Noise Density,	$f = 1kHz$ $f = 1kHz$		25 3			*		nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-Mode Input Range, Positive Negative Common-Mode Rejection	Linear Operation Linear Operation $V_{CM} = \pm 35V$	(V+) -5 (V-) +5 74	(V+) -4 (V-) +4 106		*	*	*	V V dB
INPUT IMPEDANCE Differential Common-Mode			$10^{12} \parallel 5$ $10^{12} \parallel 4$			*	*	$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-Loop Voltage Gain	$V_O = \pm 34V$, $R_L = 6\Omega$	92	103		*	*		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Full-Power Bandwidth Total Harmonic Distortion Capacitive Load	$G = +10$, $R_L = 50\Omega$ $68Vp-p$, $R_L = 6\Omega$ $G = +3$, $f = 20kHz$ $V_O = 20V$, $R_L = 8\Omega$	5	2.0 10 See Typical Curves 0.06 See Figure 6		*	*	*	MHz V/ μs %
OUTPUT Voltage Output, Positive Negative Positive Negative Current Output Short Circuit Current	$I_O = 10A$ $I_O = 10A$ $I_O = 1A$ $I_O = 1A$	(V+) -6 (V-) +6	(V+) -3.5 (V-) +3.6 (V+) -2.5 (V-) +3.1 See SOA Curves Resistor Programmed		*	*	*	V V V V
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	$I_O = 0$	± 10	± 40 ± 20	± 45 ± 25	*	*	*	V V mA
TEMPERATURE RANGE Specification Storage Thermal Resistance, θ_{JC} θ_{JA}	DC AC $f \geq 50Hz$ No Heat Sink	-40 -55	1.25 0.8 30	+85 +125 1.4 0.9	-55 *	*	+125 *	$^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$

NOTE: (1) High-speed test at $T_J = 25^{\circ}C$.

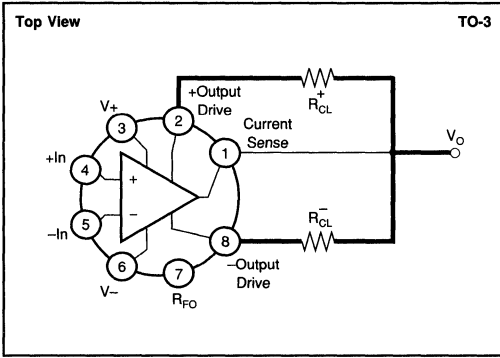
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA502BM	8-Pin TO-3	-40°C to +85°C
OPA502SM	8-Pin TO-3	-55°C to +125°C

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_+ to V_-	90V
Output Current	See SOA Curve
Input Voltage	$(V_-) -1V$ to $(V_+) +1V$
Case Temperature, Operating	150°C
Junction Temperature	200°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA502BM	8-Pin TO-3	030
OPA502SM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

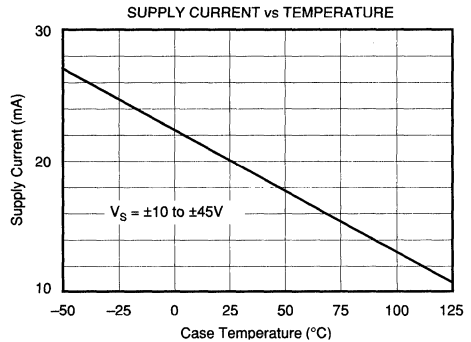
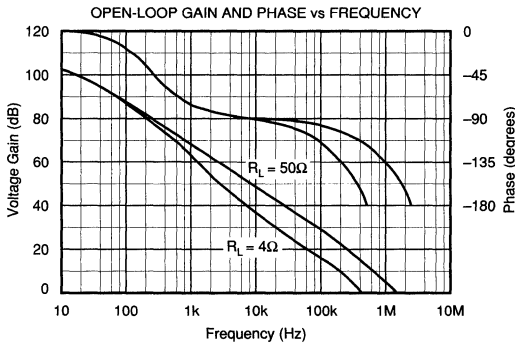
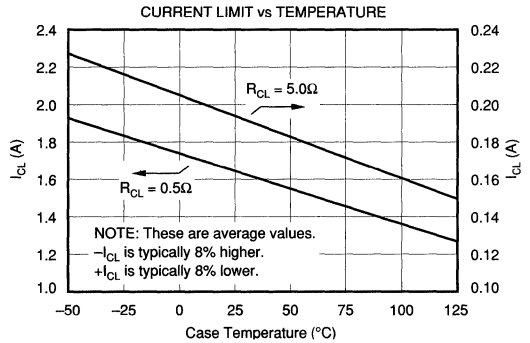
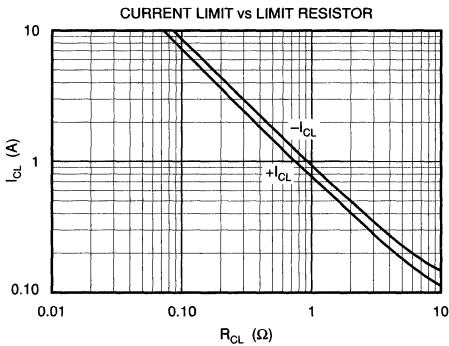
OPA502

3.2

TYPICAL PERFORMANCE CURVES

$T_{CASE} = +25^\circ C$, $V_S = \pm 40V$ unless otherwise noted.

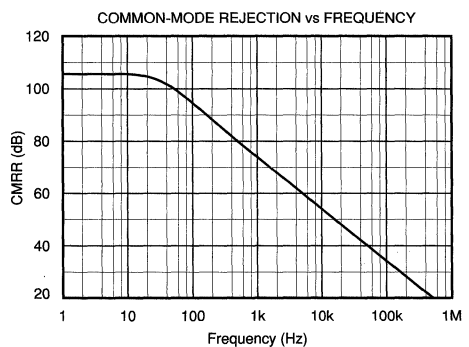
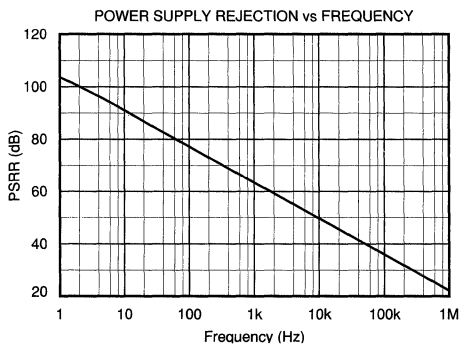
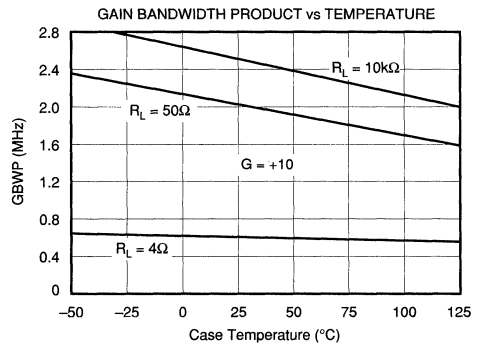
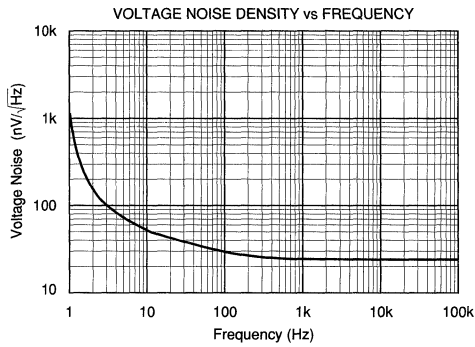
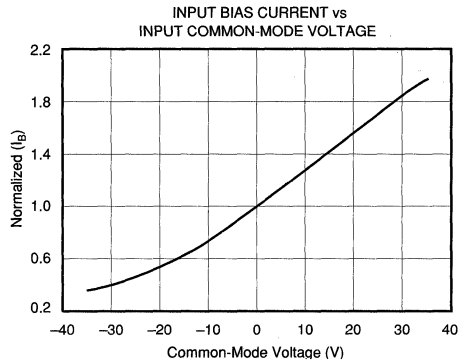
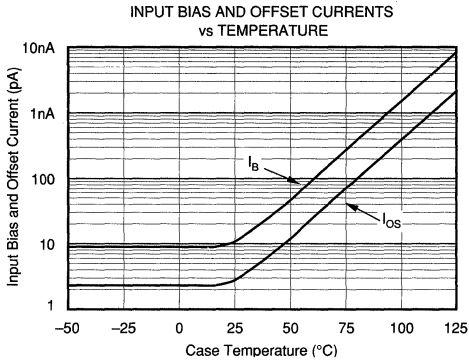
POWER OPERATIONAL AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

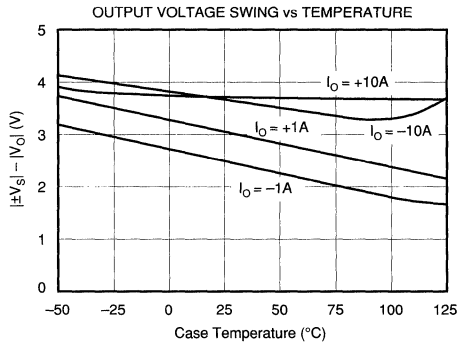
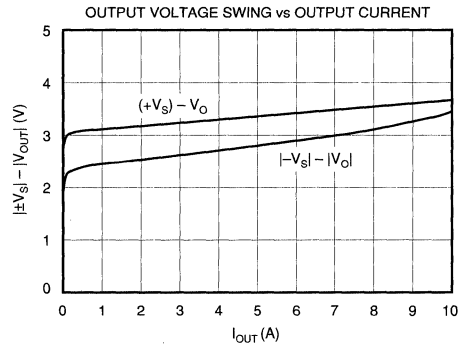
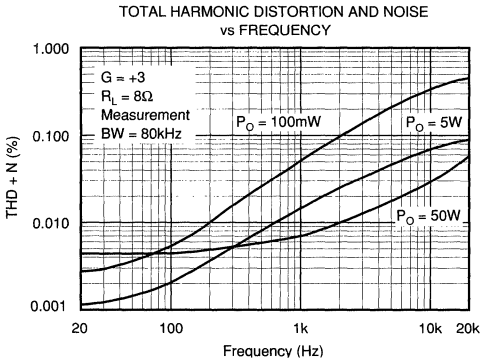
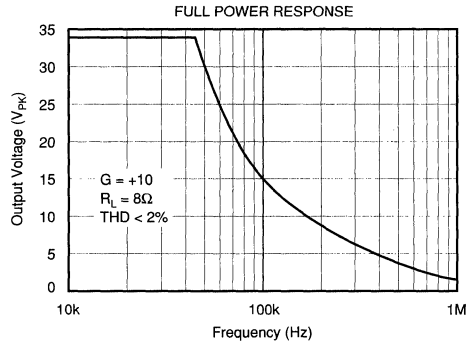
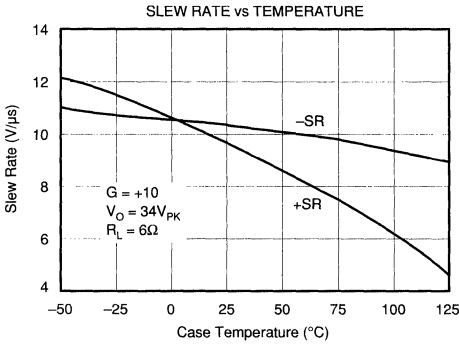
$T_{CASE} = +25^{\circ}C$, $V_S = \pm 40V$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 40V$ unless otherwise noted.



OPA502

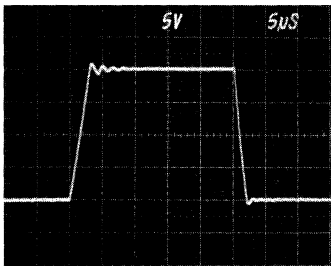
3.2

POWER OPERATIONAL AMPLIFIERS

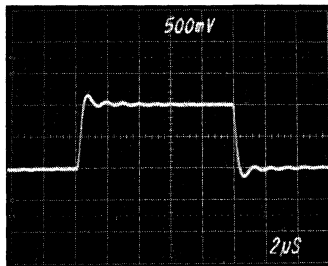
TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 40V$ unless otherwise noted.

LARGE SIGNAL RESPONSE
 $G = +3$, $R_L = 4\Omega$



SMALL SIGNAL RESPONSE
 $G = +3$, $C_L = 1000pF$



APPLICATIONS INFORMATION

Power supply terminals should be bypassed with low series impedance capacitors such as ceramic or tantalum close to the device pins. Power supply wiring should have low series impedance and inductance. Figure 1 indicates the high current connections in bold lines.

Current limit is set with two external resistors—one for positive output current and one for negative output current (see Figure 1). For conventional current limit, independent of output voltage, pin 7 should be left open (see “Foldback Current Limit”). Limiting occurs when the output current causes sufficient voltage drop across R_{CL} to turn on the respective current limit transistor. The limit current decreases at high temperature (see typical performance curve “Current Limit vs Temperature”).

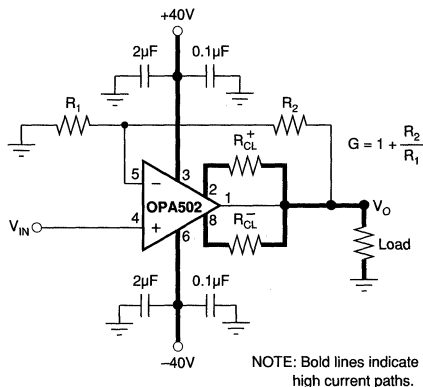
Figure 1 also shows nominal current limit produced by standard resistor values. See also the typical performance curve “Current Limit vs Limit Resistance”. The output current must flow through this resistor, so its power rating must be chosen accordingly. The table in Figure 1 shows the power dissipation of the current limit resistor during continuous current limit (room temperature). Connections from the current limit resistors to the device pins can typically add 0.02Ω to 0.05Ω to the effective value of R_{CL} . This significantly affects the current limit value for high output currents.

The current limit resistors can be chosen from a variety of types. Most common wire-wound types are satisfactory, although some physically large types may have excessive inductance which can cause problems. You should test your circuits with the exact resistor type planned for production use.

You can set different current limits for positive and negative current. Resistors are chosen with the same table of values in Figure 1.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transi-



NOTE: Bold lines indicate high current paths.

R_{CL} (Ω)	I_{CL} at $25^{\circ}C$ (A)	Power Dissipation ¹ of R_{CL} (W)
10	0.11	0.12
5	0.19	0.18
2	0.44	0.39
1	0.78	0.61
0.68	1.22	1.0
0.5	1.65	1.4
0.3	2.73	2.2
0.2	4.0	3.2
0.15	5.4	4.4
0.1	8.1	6.6

NOTE 1: Power dissipation during continuous current limit at $T_{CASE} = +25^{\circ}C$.

FIGURE 1. Basic Circuit Connections.

tor. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE} . The Safe Operating Area (SOA) curve, Figure 2) shows the permissible range of voltage and current.

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The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ($V+$ or $V-$) across the conducting transistor. With $V_s = \pm 40V$ the current limit must be set for 3A (25°C) to be safe for continuous short-circuit to ground. For further insight on SOA, consult AB-039.

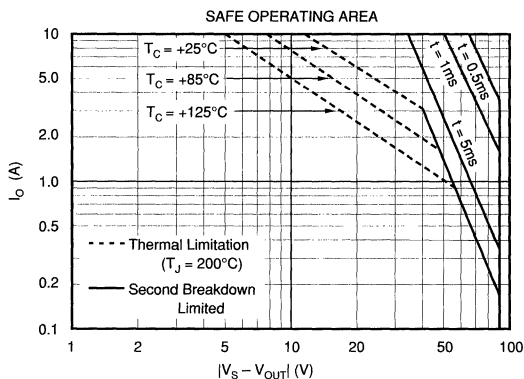


FIGURE 2. Safe Operating Area (SOA).

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA502 do not need to be equal. Figure 3 shows a circuit designed for a positive output voltage and current. The $-5V$ power supply voltage assures that the inputs of the OPA502 are operated within their linear common-mode range. The $V+$ power supply could range from 15V to 85V. The total voltage ($V-$ to $V+$) can range from 20V to 90V.

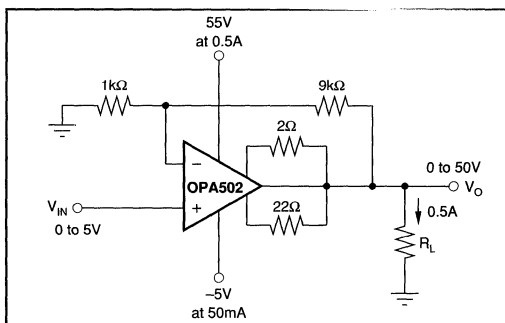


FIGURE 3. Unbalanced Power Supplies.

FOLDOVER CURRENT LIMIT

By connecting a resistor from pin 7 to ground, you can make the limit current vary with output voltage. The foldover limit

circuit can be set to allow high output current when V_{CE} is low (high output voltage). Output current limits at a lower value under the more stressful condition when V_{CE} is high, (output voltage is low).

The behavior of this voltage-dependant current limit is described by the following equation.

$$I_{LIMIT} = \frac{0.81 + \left(\frac{0.28 V_O}{R_{FO} + 20} \right)}{R_{CL}} + 0.03$$

where: V_O is the output voltage measured with respect to ground.

R_{FO} is the resistor connected from pin 7 to ground (in k ohms).

R_{CL} is the current limit resistor (in ohms).

The foldover limit circuitry can be set to allow large voltage and current to resistive loads, yet limit output current to a safe value with an output short circuit.

Reactive or EMF-generating loads can produce unexpected behavior with the foldover circuit driven into limiting. With a reactive load, peak output current occurs at low or zero output voltage. Compared to a resistive load, a reactive load with the same total impedance will be more likely to activate the foldover limit circuitry.

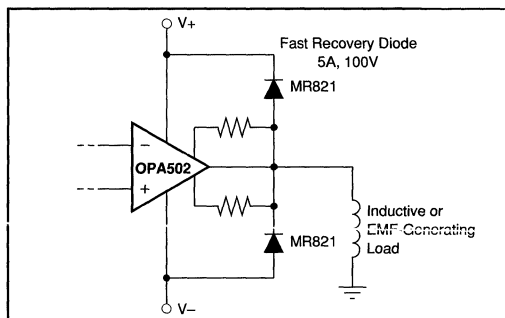


FIGURE 4. Diode Protection of Output.

OUTPUT PROTECTION

The output stage of the OPA502 is protected by internal diode clamps to the power supply terminals. These internal diodes are similar to common silicon rectifier types and may not be fast enough for adequate protection. For loads that can deliver large reverse kickback current (greater than 5A) to the output, external fast-recovery clamp diodes are recommended (Figure 4). For these diodes (internal or external) to provide the intended protection, the power supplies must provide a low impedance to a reverse current.

OPA502

3.2

POWER OPERATIONAL AMPLIFIERS

COMPENSATION AND STABILITY

Capacitance at the inverting input causes a high frequency pole in the feedback path. This reduces phase margin, causing pulse response ringing, and in severe cases, oscillations. A low value feedback capacitor can reduce or eliminate this effect by maintaining a constant feedback factor at high frequency (see Figure 5).

Depending on the load conditions, precautions may be required when using the OPA502 in low gains. Gains less than $+3V/V$ or $-2V/V$ may cause oscillations, particularly with capacitive loads. Figure 6 shows several circuits for low gain and capacitive loads.

Large value feedback capacitors used to limit the closed-loop bandwidth or form an integrator may also produce instability because the closed-loop gain approaches unity at high frequency.

MOUNTING AND HEAT SINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The case of the OPA502 is isolated from all circuitry and can be fastened directly to a heat sink. This eliminates cumbersome insulating hardware that degrades thermal performance. Consult Application Bulletin AB-037 for proper mounting techniques and procedures for TO-3 power products.

SOCKET

A mating socket, 0804MC is available for the OPA502 and can be purchased from Burr-Brown. Although not required, this socket makes interchanging parts easy, especially during design and testing.

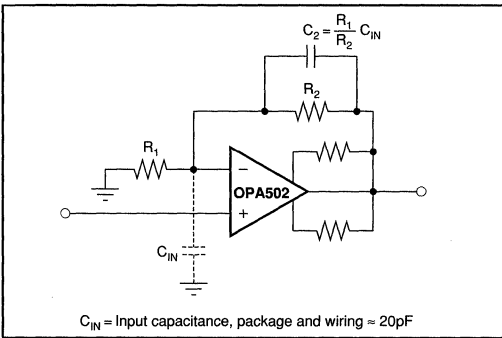


FIGURE 5. Compensating Input Capacitance.

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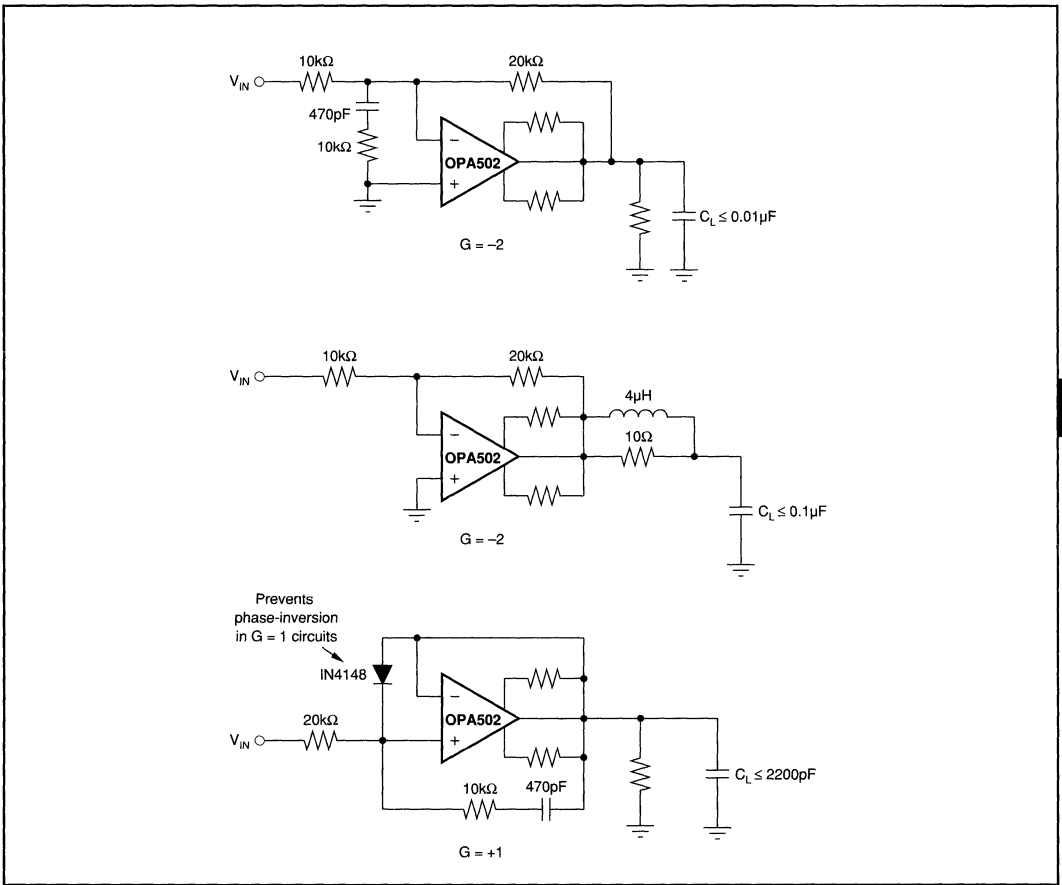


FIGURE 6. Compensation Circuits.

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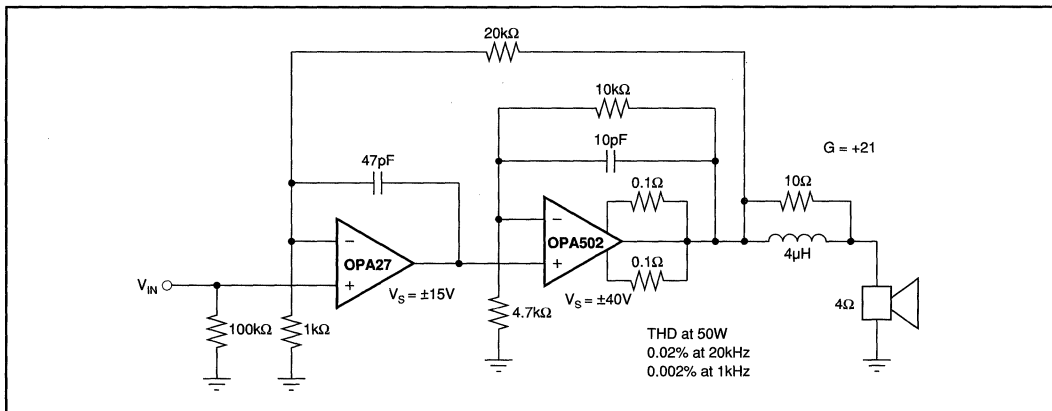


FIGURE 7. Low Distortion Composite Amplifier.

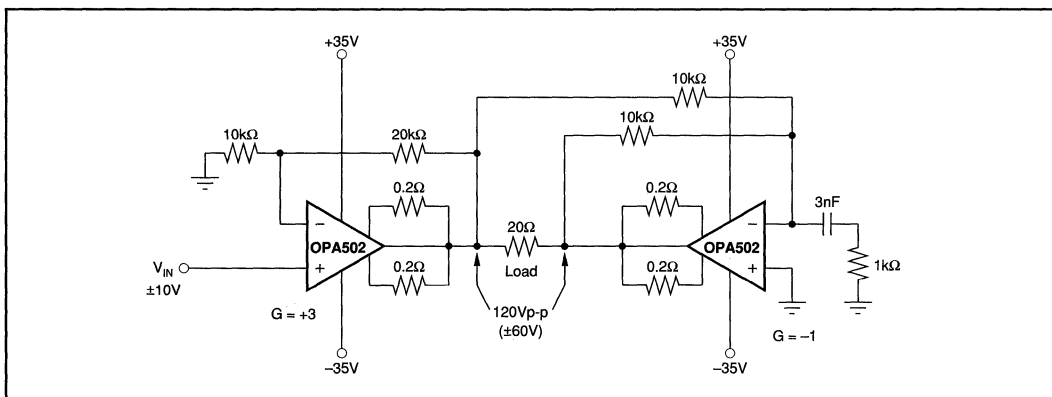


FIGURE 8. Bridge Drive Circuit.

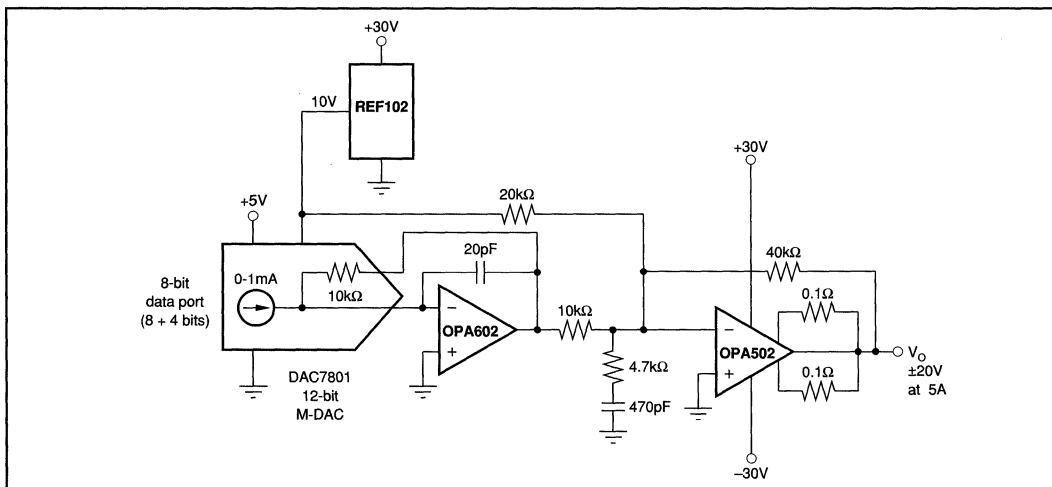


FIGURE 9. Digitally Programmable Power Supply.

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OPA512

Very-High Current—High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE: $\pm 10V$ to $\pm 50V$
- HIGH OUTPUT CURRENT: 15A Peak
- CLASS A/B OUTPUT STAGE:
Low Distortion
- VOLTAGE-CURRENT LIMIT PROTECTION
CIRCUIT
- SMALL TO-3 PACKAGE

APPLICATIONS

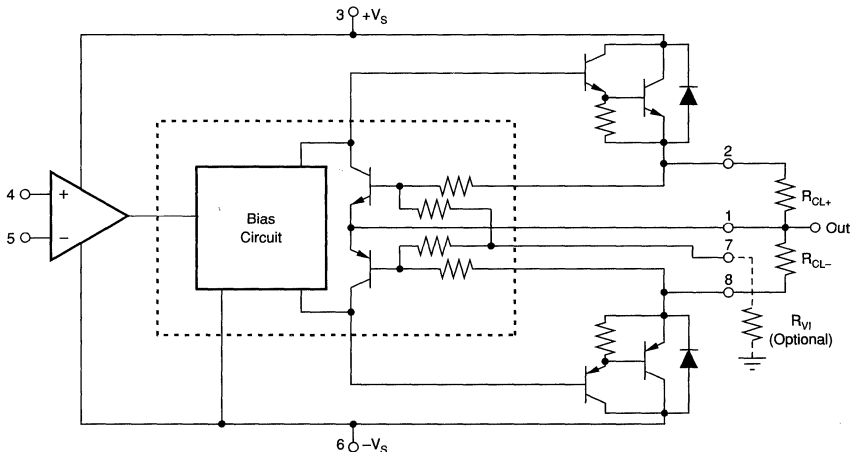
- SERVO AMPLIFIER
- MOTOR DRIVER
- SYNCRO EXCITATION
- AUDIO AMPLIFIER
- TEST PIN DRIVER

DESCRIPTION

The OPA512 is a high voltage, very-high current operational amplifier designed to drive a wide variety of resistive and reactive loads. Its complementary class A/B output stage provides superior performance in applications requiring freedom from cross-over distortion. User-set current limit circuitry provides protection to the amplifier and load in fault conditions. A resistor-programmable voltage-current limiter circuit may be used to further protect the amplifier from damaging conditions.

The OPA512 employs a laser-trimmed monolithic integrated circuit to bias the output transistors, providing excellent low-level signal fidelity and high output voltage swing. The reduced internal parts count made possible with this monolithic IC improves performance and reliability.

This hybrid integrated circuit is housed in a hermetic TO-3 package and all circuitry is electrically-isolated from the case. This allows direct mounting to a chassis or heat sink without cumbersome insulating hardware and provides optimum heat transfer.



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PDS-600B

3.2.49

OPA512

3.2

POWER OPERATIONAL AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

At $T_c = +25^\circ\text{C}$, and $V_s = \pm 40\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA512BM			OPA512SM			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT OFFSET VOLTAGE Initial Offset vs Temperature vs Supply Voltage vs Power	Specified Temp. Range		± 2	± 6		± 1	± 3	mV	
			± 10	± 65		*	± 40	$\mu\text{V}/^\circ\text{C}$	
			± 30	± 200		*	*	$\mu\text{V}/\text{V}$	
			± 20			*	*	$\mu\text{V}/\text{V}$	
INPUT BIAS CURRENT Initial vs Temperature vs Supply Voltage	Specified Temp. Range		12	30		10	20	nA	
			± 50	400		*	*	$\text{pA}/^\circ\text{C}$	
			± 10			*		pA/V	
INPUT OFFSET CURRENT Initial vs Temperature	Specified Temp. Range		± 12	± 30		± 5	± 10	nA	
			± 50			*		$\text{pA}/^\circ\text{C}$	
INPUT IMPEDANCE, DC			200			*		M Ω	
INPUT CAPACITANCE			3			*		pF	
VOLTAGE RANGE Common-Mode Voltage Common-Mode Rejection	Specified Temp. Range	$\pm(V_s - 5)$		$\pm(V_s - 3)$	*	*		V	
	Specified Temp. Range	74		100	*	*		dB	
GAIN Open-Loop Gain at 10Hz Gain-Bandwidth Product, 1MHz Power Bandwidth Phase Margin	1k Ω Load Specified Temp. Range		110			*		dB	
	8 Ω Load	96	108		*	*		dB	
	8 Ω Load		4		*	*		MHz	
	8 Ω Load	13	20		*	*		kHz	
	8 Ω Load		20			*		Degrees	
OUTPUT Voltage Swing ⁽¹⁾ Current, Peak Settling Time to 0.1% Slew Rate Capacitive Load	BM at 10A, SM at 15A Specified Temp. Range	$\pm(V_s - 6)$				$\pm(V_s - 7)$		V	
	$I_o = 80\text{mA}$	$\pm(V_s - 5)$				*		V	
	$I_o = 5\text{A}$	$\pm(V_s - 5)$				*		V	
	2V Step	10				15		A	
	2.5	2				*		μs	
	4	4				*		$\text{V}/\mu\text{s}$	
	Specified Temp. Range G = 1				1.5		*	nF	
Specified Temp. Range G > 10				SOA ⁽²⁾		*			
POWER SUPPLY Voltage Current, Quiescent	Specified Temp. Range	± 10	± 40	± 45	*	*	± 50	V	
			25	50		*	35	mA	
THERMAL RESISTANCE AC Junction-to-Case ⁽³⁾ DC Junction-to-Case Junction to Air	$T_c = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $f > 60\text{Hz}$ $T_c = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $T_c = -55^\circ\text{C}$ to $+125^\circ\text{C}$		0.8	0.9		*	*	$^\circ\text{C}/\text{W}$	
				1.25	1.4		*	*	$^\circ\text{C}/\text{W}$
				30			*	*	$^\circ\text{C}/\text{W}$
TEMPERATURE RANGE Specified	T_c	-25		+85	-55		+125	$^\circ\text{C}$	

⁽¹⁾Specification same as OPA512BM.

NOTES: (1) $+V_s$ and $-V_s$ denote the positive and negative supply voltage, respectively. Total V_s is measured from $+V_s$ to $-V_s$. (2) SOA = Safe Operating Area. (3) Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

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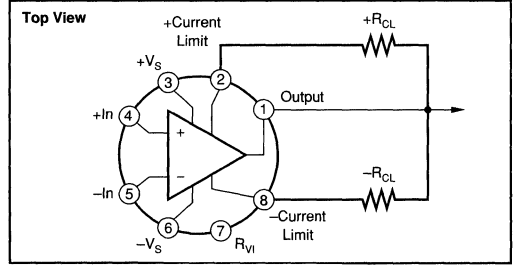
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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	100V
Output Current: Source	15A
Sink	see SOA
Power Dissipation, Internal ⁽¹⁾	125W
Input Voltage: Differential	$\pm(V_S - 3V)$
Common-mode	$\pm V_S$
Temperature: Pins (soldering, 10s)	+300°C
Junction ⁽¹⁾	+200°C
Temperature Range: Storage ⁽²⁾	-65°C to +150°C
Operating (Case)	-55°C to +125°C

NOTES: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. (2) OPA512BM, -55°C to +100°C.

CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA512BM	8-pin TO-3	-25°C to +85°C
OPA512SM	8-pin TO-3	-55°C to +125°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA512BM	8-Pin TO-3	030
OPA512SM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

OPA512

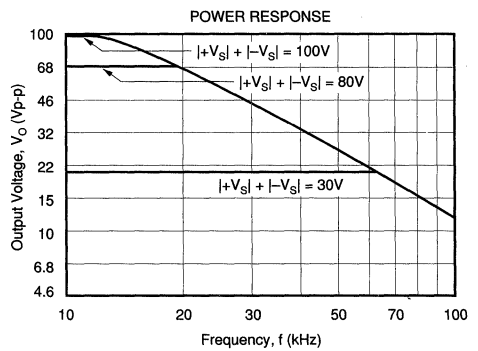
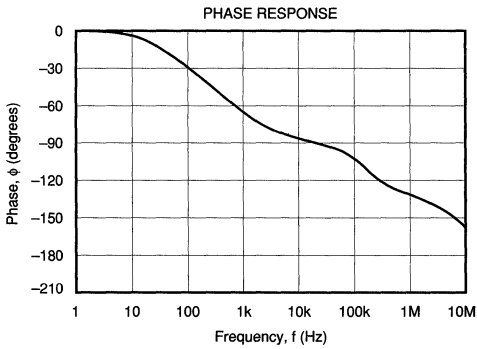
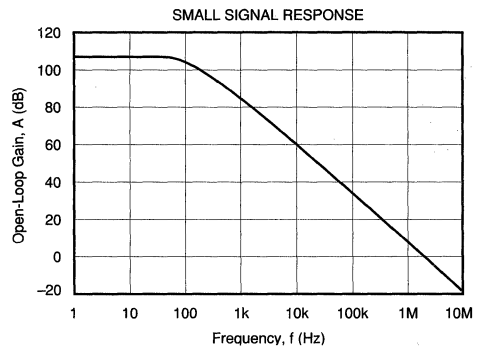
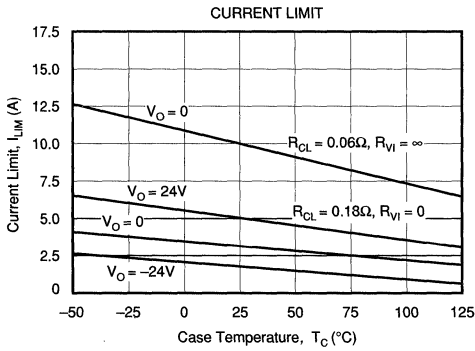
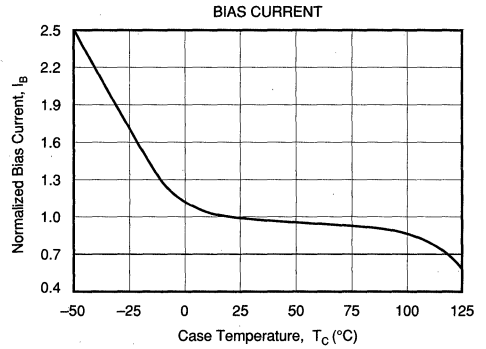
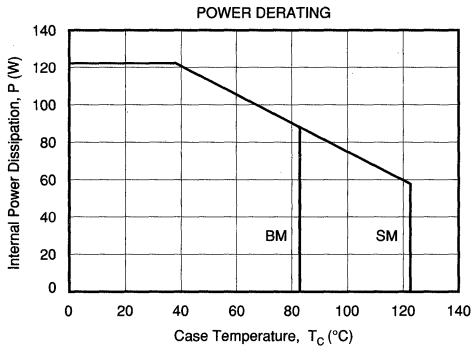
3.2

POWER OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES

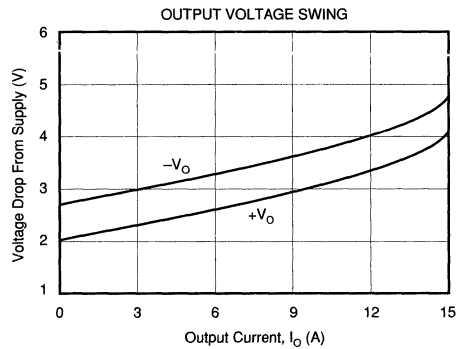
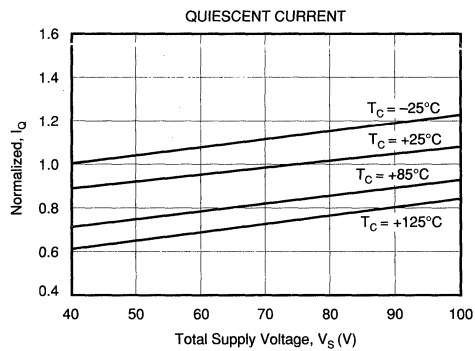
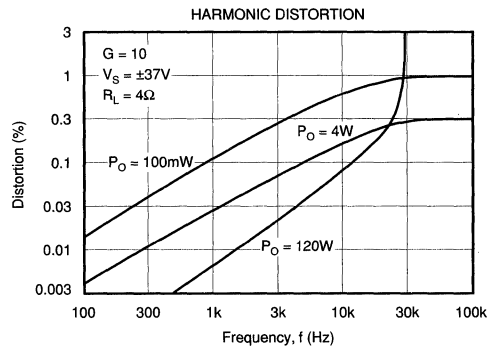
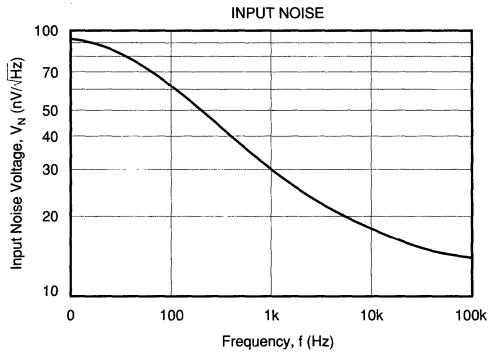
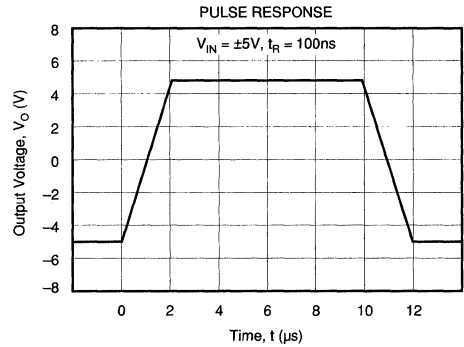
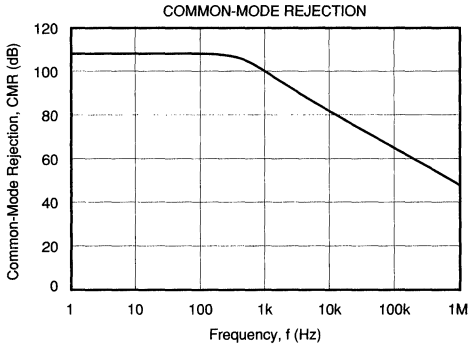
$T_A = 25^\circ\text{C}$, $V_S = \pm 40\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25^\circ\text{C}$, $V_S = \pm 40\text{VDC}$, unless otherwise noted.



OPA512

3.2

POWER OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

POWER SUPPLIES

Specifications for the OPA512 are based on a nominal operating voltage of $\pm 40V$. A single power supply or unbalanced supplies may be used as long as the maximum total operating voltage (total of $+V_S$ and $-V_S$) is not greater than 90V (100V for OPA512SM model).

CURRENT LIMITS

Current limit resistors must be provided for proper operation. Independent positive and negative current limit values may be selected by choice of R_{CL+} and R_{CL-} , respectively. Resistor values are calculated by:

$$R_{CL} = 0.65/I_{LIM} \text{ (amps)} - 0.007$$

This is the nominal current limit value at room temperature. The maximum output current decreases at high temperature as shown in the typical performance curve. Most wire-wound resistors are satisfactory, but some highly inductive types may cause loop stability problems. Be sure to evaluate performance with the actual resistors to be used in production.

HEAT SINKING

Power amplifiers are rated by case temperature (not ambient temperature.) The maximum allowable power dissipation is a function of the case temperature as shown in the power derating curve. Load characteristics, signal conditions, and power supply voltage determine the power dissipated by the amplifier. The case temperature will be determined by the heat sinking conditions. Sufficient heat sinking must be provided to keep the case temperature within safe bounds given the power dissipated and ambient temperature. See Application Bulletin AB-038 for further details.

SAFE OPERATING AREA (SOA)

The safe area plot provides a comprehensive summary of the power handling limitations of a power amplifier, including maximum current, voltage and power as well as the secondary breakdown region (see Figure.) It shows the allowable output current as a function of the power supply to output voltage differential (voltage across the conducting power device.) See Application Bulletin AB-039 for details on SOA.

VOLTAGE-CURRENT LIMITER CIRCUITRY

The voltage-current (V-I) limiter circuit provides a means to protect the amplifier from SOA damage such as a short circuit to ground, yet allows high output currents to flow

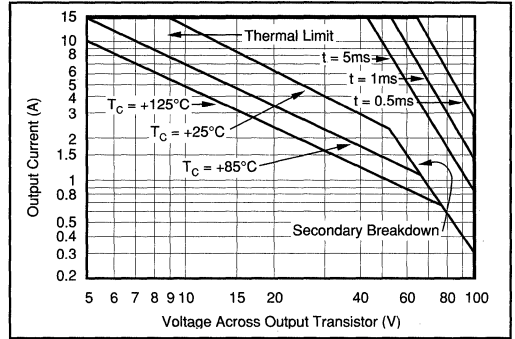


FIGURE 1. Safe Operating Area.

under normal load conditions. Sensing both the output current and the output voltage, this limiter circuit increases the current limit value as the output voltage approaches the power supply voltage (where power dissipation is low.) This type of limiting is achieved by connecting pin 7 through a programming resistor to ground. The V-I limiter circuit is governed by the equation:

$$I_{LIMIT} = \frac{0.65 + \frac{0.28 V_o}{20 + R_{VI}}}{R_{CL} + 0.007}$$

where:

I_{LIMIT} is the maximum current available at a given output voltage.

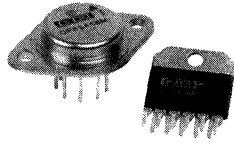
R_{VI} is the value (k Ω) of the resistor from pin 7 to ground.

R_{CL} is the current limit resistor in ohms.

V_o is the instantaneous output voltage in volts.

Reactive or EMF-generating loads may produce unusual (perhaps undesirable) waveforms with the V-I limit circuit driven into limit. Since current peaks in a reactive load do not align with the output voltage peaks, the output waveform will not appear as a simple voltage-limited waveform. Response of the load to the limiter, in fact, may produce a "backfire" reaction producing unusual output waveforms.

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OPA541

High Power Monolithic OPERATIONAL AMPLIFIER

OPA541

FEATURES

- POWER SUPPLIES TO $\pm 40V$
- OUTPUT CURRENT TO 10A PEAK
- PROGRAMMABLE CURRENT LIMIT
- INDUSTRY-STANDARD PIN OUT
- FET INPUT
- TO-3 AND LOW-COST POWER PLASTIC PACKAGES

APPLICATIONS

- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCHRO EXCITATION
- AUDIO AMPLIFIER
- PROGRAMMABLE POWER SUPPLY

3.2

POWER OPERATIONAL AMPLIFIERS

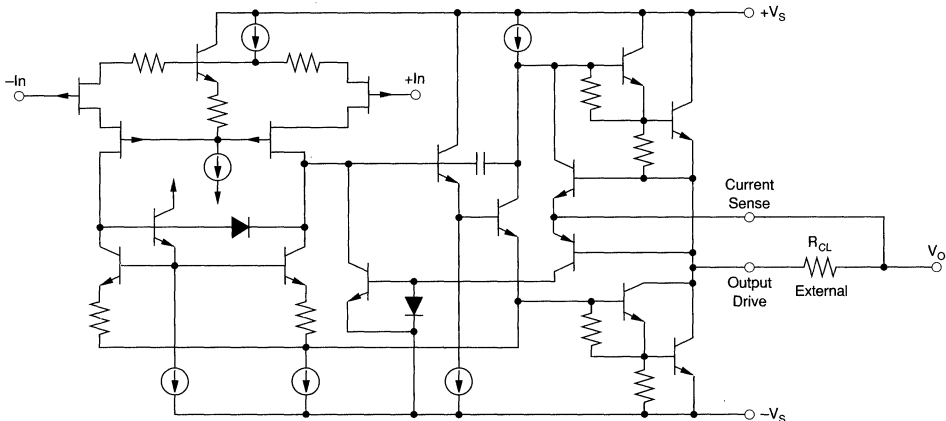
DESCRIPTION

The OPA541 is a power operational amplifier capable of operation from power supplies up to $\pm 40V$ and delivering continuous output currents up to 5A. Internal current limit circuitry can be user-programmed with a single external resistor, protecting the amplifier and load from fault conditions. The OPA541 is fabricated using a proprietary bipolar/FET process.

Pinout is compatible with popular hybrid power amplifiers such as the OPA511, OPA512 and the 3573.

The OPA541 uses a single current-limit resistor to set both the positive and negative current limits. Applications currently using hybrid power amplifiers requiring two current-limit resistors need not be modified.

The OPA541 is available in an 11-pin power plastic package and an industry-standard 8-pin TO-3 hermetic package. The power plastic package has a copper-lead frame to maximize heat transfer. The TO-3 package is isolated from all circuitry, allowing it to be mounted directly to a heat sink without special insulators.



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PDS-737G

3.2.55

SPECIFICATIONS

ELECTRICAL

At $T_c = +25^\circ\text{C}$ and $V_s = \pm 35\text{VDC}$ unless otherwise noted.

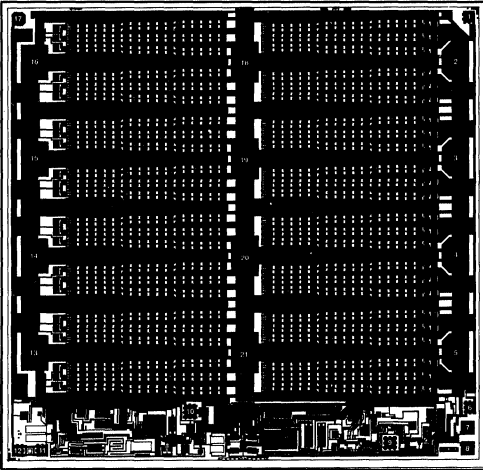
PARAMETER	CONDITIONS	OPA541AM/AP			OPA541BM/SM			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT OFFSET VOLTAGE V_{OS} vs Temperature vs Supply Voltage vs Power	Specified Temperature Range $V_s = \pm 10\text{V to } \pm V_{MAX}$		± 2	± 10		± 0.1	± 1	mV	
			± 20	± 40		± 15	± 30	$\mu\text{V}/^\circ\text{C}$	
			± 2.5	± 10		*	*	$\mu\text{V}/\text{V}$	
			± 20	± 60		*	*	$\mu\text{V}/\text{W}$	
INPUT BIAS CURRENT I_b			4	50		*	*	pA	
INPUT OFFSET CURRENT I_{OS}	Specified Temperature Range		± 1	± 30 5		*	*	pA nA	
INPUT CHARACTERISTICS Common-Mode Voltage Range Common-Mode Rejection Input Capacitance Input Impedance, DC	Specified Temperature Range $V_{CM} = (\pm V_s - 6\text{V})$		$\pm(V_s - 6)$	$\pm(V_s - 3)$	*	*		V	
			95	113	*	*		dB	
				5		*	*		pF
				1		*	*		T Ω
GAIN CHARACTERISTICS Open Loop Gain at 10Hz Gain-Bandwidth Product	$R_L = 6\Omega$		90	97 1.6		*	*	dB MHz	
						*	*		
OUTPUT Voltage Swing Current, Peak	$I_o = 5\text{A, Continuous}$ $I_o = 2\text{A}$ $I_o = 0.5\text{A}$		$\pm(V_s - 5.5)$ $\pm(V_s - 4.5)$	$\pm(V_s - 4.5)$ $\pm(V_s - 3.6)$	*	*		V V V	
			$\pm(V_s - 4)$ 9	$\pm(V_s - 3.2)$ 10	*	*		A	
AC PERFORMANCE Slew Rate Power Bandwidth Settling Time to 0.1% Capacitive Load Phase Margin	$R_L = 8\Omega, V_o = 20\text{Vrms}$ 2V Step Specified Temperature Range, $G = 1$ Specified Temperature Range, $G > 1$ Specified Temperature Range, $R_L = 8\Omega$		6	10		*	*	V/ μs	
			45	55		*	*	kHz	
			3.3	2		*	*		μs nF
					SOA ⁽¹⁾		*	*	Degrees
POWER SUPPLY Power Supply Voltage, $\pm V_s$ Current, Quiescent	Specified Temperature Range	± 10	± 30 20	± 35 25	*	± 35 *	± 40 *	V mA	
THERMAL RESISTANCE θ_{JC} (Junction-to-Case) ⁽²⁾ $\theta_{JC}^{(2)}$ θ_{JA} (Junction-to-Ambient) OPA541AP (Plastic)	AC Output $f > 60\text{Hz}$ DC Output No Heat Sink			2.5				$^\circ\text{C}/\text{W}$	
				3				$^\circ\text{C}/\text{W}$	
				40					$^\circ\text{C}/\text{W}$
				40					$^\circ\text{C}/\text{W}$
TEMPERATURE RANGE T_{CASE}	AM, BM, AP SM	-25		+85	*		*	$^\circ\text{C}$ $^\circ\text{C}$	

* Specification same as OPA541AM/AP.

NOTE: (1) SOA is the Safe Operating Area shown in Figure 1. (2) Plastic package may require insulator which typically adds $1^\circ\text{C}/\text{W}$.

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DICE INFORMATION



OPA541 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	NC	11	NC
2	-V _s	12	Current Sense
3	-V _s	13	+V _s
4	-V _s	14	+V _s
5	-V _s	15	+V _s
6	NC	16	+V _s
7	-In	17	Current Sense
8	+In	18	Output Drive
9	NC	19	Output Drive
10	NC	20	Output Drive
		21	Output Drive

NOTE: For full output current capability, wire-bond all like connections of +V_s, -V_s and Output Drive.

Substrate Bias: Electrically connected to -V_s supply.

MECHANICAL INFORMATION

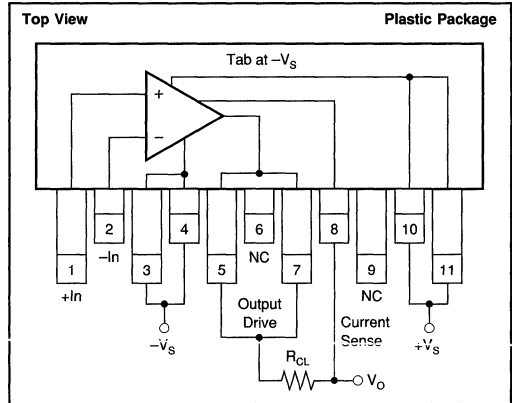
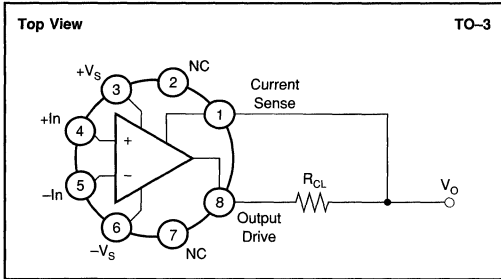
	MILS (0.001")	MILLIMETERS
Die Size	213 x 205 ±5	5.41 x 5.21 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Chromium-Silver	

OPA541

3.2

POWER OPERATIONAL AMPLIFIERS

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V _s to -V _s	80V
Output Current	see SOA
Power Dissipation, Internal ⁽¹⁾	125W
Input Voltage: Differential	±V _s
Common-mode	±V _s
Temperature: Pin solder, 10s	+300°C
Junction ⁽¹⁾	+150°C

Temperature Range:	
AM, BM SM	
Storage	-65°C to +150°C
Operating (case)	-55°C to +125°C
AP	
Storage	-40°C to +85°C
Operating (case)	-25°C to +85°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	CONTINUOUS CURRENT
OPA541AP	Power Plastic	-25°C to +85°C	5A at 25°C
OPA541AM	TO-3	-25°C to +85°C	5A at 25°C
OPA541BM	TO-3	-25°C to +85°C	5A at 25°C
OPA541SM	TO-3	-55°C to +125°C	5A at 25°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA541AP	Power Plastic	242
OPA541AM	TO-3	030
OPA541BM	TO-3	030
OPA541SM	TO-3	030

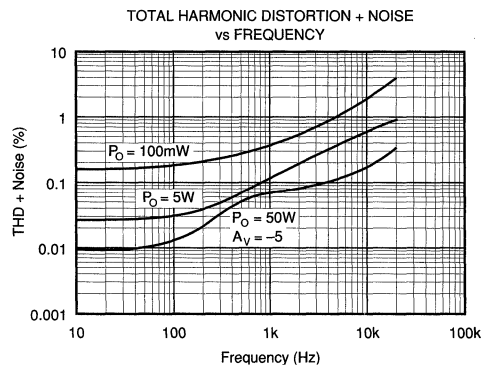
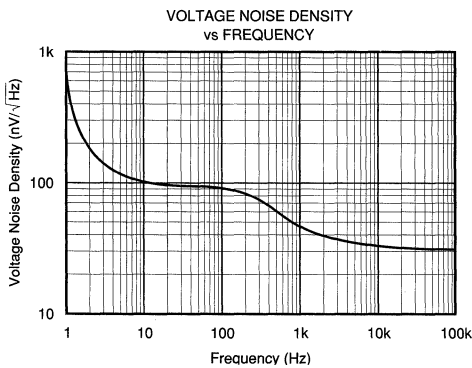
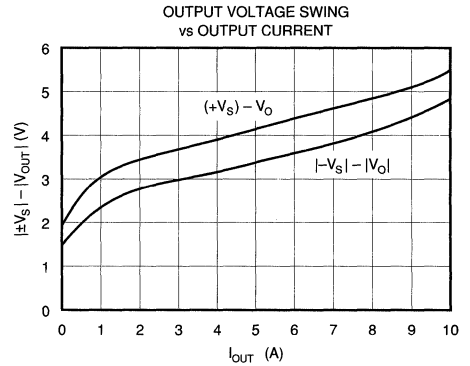
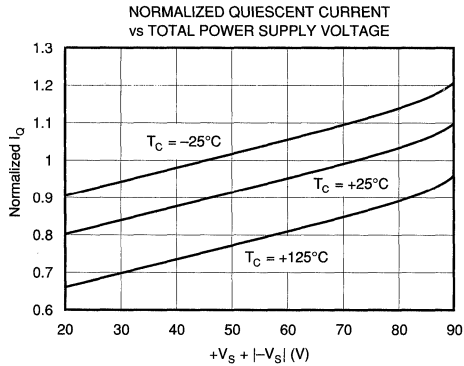
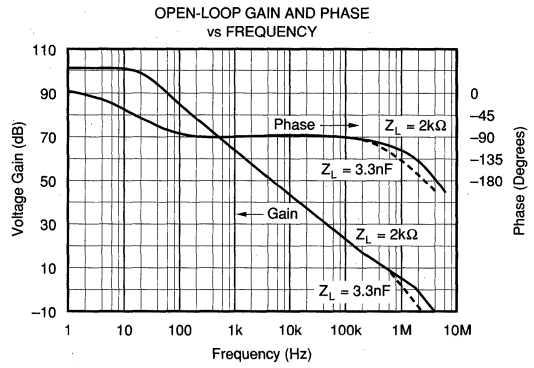
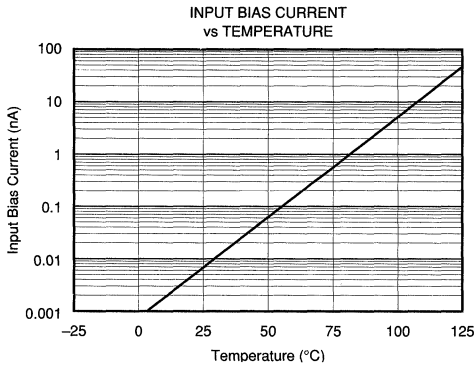
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



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TYPICAL PERFORMANCE CURVES

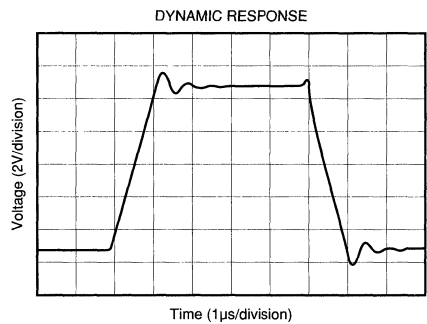
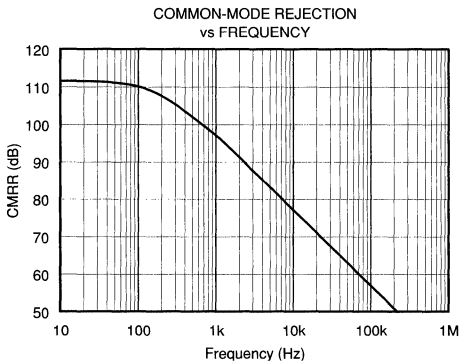
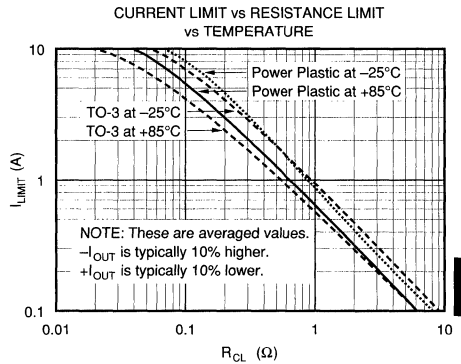
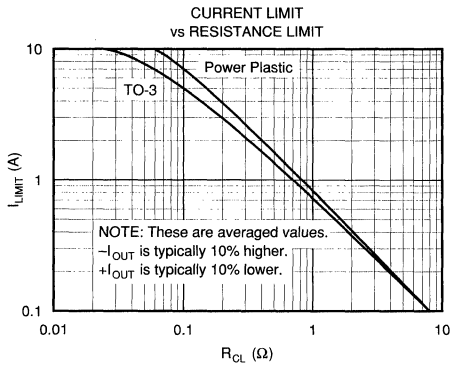
$T_A = +25^\circ\text{C}$, $V_S = \pm 35\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 35\text{VDC}$ unless otherwise noted.



OPA541

3.2

POWER OPERATIONAL AMPLIFIERS

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA541 is specified for operation from power supplies up to $\pm 40V$. It can also be operated from unbalanced power supplies or a single power supply, as long as the total power supply voltage does not exceed 80V. The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and oscillations.

CURRENT LIMIT

Internal current limit circuitry is controlled by a single external resistor, R_{CL} . Output load current flows through this external resistor. The current limit is activated when the voltage across this resistor is approximately a base-emitter turn-on voltage. The value of the current limit resistor is approximately:

$$(AM, BM, SM) \quad R_{CL} = \frac{0.809}{|I_{LIM}|} - 0.057$$

$$(AP) \quad R_{CL} = \frac{0.813}{|I_{LIM}|} - 0.02$$

Because of the internal structure of the OPA541, the actual current limit depends on whether current is positive or negative. The above R_{CL} gives an average value. For a given R_{CL} , $+I_{OUT}$ will actually be limited at about 10% below the expected level, while $-I_{OUT}$ will be limited about 10% above the expected level.

The current limit value decreases with increasing temperature due to the temperature coefficient of a base-emitter junction voltage. Similarly, the current limit value increases at low temperatures. Current limit versus resistor value and temperature effects are shown in the Typical Performance Curves. Approximate values for R_{CL} at other temperatures may be calculated by adjusting R_{CL} as follows:

$$\Delta R_{CL} = \frac{-2mV}{|I_{LIM}|} \times (T - 25)$$

The adjustable current limit can be set to provide protection from short circuits. The safe short-circuit current depends on power supply voltage. See the discussion on Safe Operating Area to determine the proper current limit value.

Since the full load current flows through R_{CL} , it must be selected for sufficient power dissipation. For a 5A current limit on the TO-3 package, the formula yields an R_{CL} of 0.105 Ω (0.143 Ω on the power plastic package due to different internal resistances). A continuous 5A through 0.105 Ω would require an R_{CL} that can dissipate 2.625W.

Sinusoidal outputs create dissipation according to rms load current. For the same R_{CL} , AC peaks would still be limited to 5A, but rms current would be 3.5A, and a current limiting resistor with a lower power rating could be used. Some applications (such as voice amplification) are assured of signals with much lower duty cycles, allowing a current resistor with a low power rating. Wire-wound resistors may be used for R_{CL} . Some wire-wound resistors, however, have excessive inductance and may cause loop-stability problems. Be sure to evaluate circuit performance with resistor type planned for production to assure proper circuit operation.

HEAT SINKING

Power amplifiers are rated by case temperature, not ambient temperature as with signal op amps. Sufficient heat sinking must be provided to keep the case temperature within rated limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{HS} = \frac{T_{CASE} - T_{AMBIENT}}{P_D (\max)}$$

Commercially available heat sinks often specify their thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the TO-3 package. Since mica and other similar insulators typically add approximately 0.7°C/W thermal resistance, their elimination significantly improves thermal performance. See Burr-Brown Application Note AN-83 for further details on heat sinking. On the power plastic package, the metal tab is connected to $-V_S$, and appropriate actions should be taken when mounting on a heat sink or chassis.

SAFE OPERATING AREA

The safe operating area (SOA) plot provides comprehensive information on the power handling abilities of the OPA541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

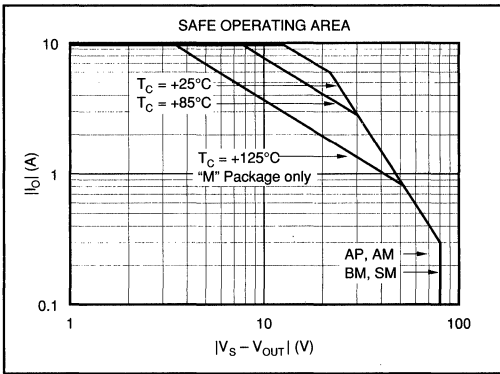


FIGURE 1. Safe Operating Area.

Short circuit protection requires evaluation of SOA. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. The current limit must be set to a value which is safe for the power supply voltage used. For instance, with $V_S \pm 35V$, a short to ground would force 35V across the conducting power transistor. A current limit of 1.8A would be safe.

Reactive, or EMF-generating, loads such as DC motors can present difficult SOA requirements. With a purely reactive load, output voltage and load current are 90° out of phase. Thus, peak output current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

REPLACING HYBRID POWER AMPLIFIERS

The OPA541 can be used in applications currently using various hybrid power amplifiers, including the OPA501, OPA511, OPA512, and 3573. Of course, the application must be evaluated to assure that the output capability and other performance attributes of the OPA541 meet the necessary requirement. These hybrid power amplifiers use two current limit resistors to independently set the positive and negative current limit value. Since the OPA541 uses only one current limit resistor to set both the positive and negative current limit, only one resistor (see Figure 4) need be installed. If installed, the resistor connected to pin 2 (TO-3 package) is superfluous, but it does no harm.

Because one resistor carries the current previously carried by two, the resistor may require a higher power rating. Minor adjustments may be required in the resistor value to achieve the same current limit value. Often, however, the change in current limit value when changing models is small compared to its variation over temperature. Many applications can use the same current limit resistor.

APPLICATIONS CIRCUITS

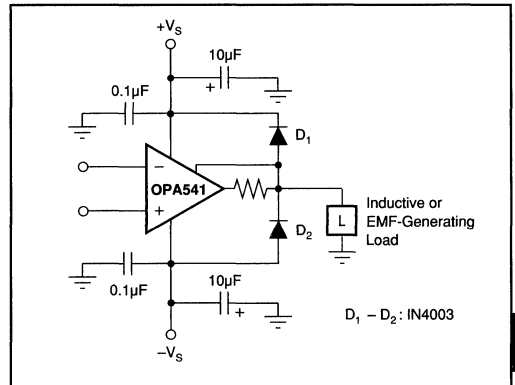


FIGURE 2. Clamping Output for EMF-Generating Loads.

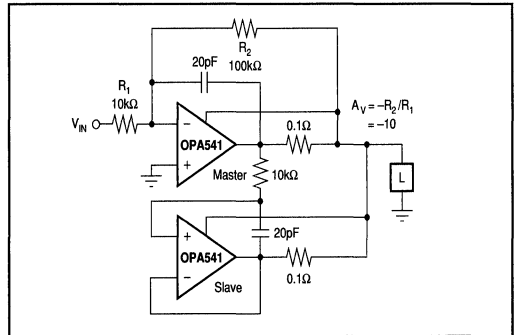


FIGURE 3. Isolating Capacitive Loads.

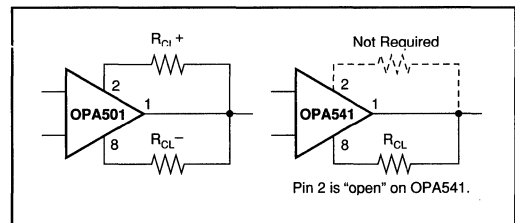


FIGURE 4. Replacing OPA501 with OPA541.

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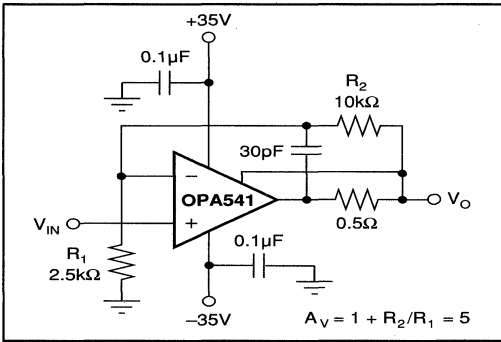


FIGURE 5. Paralleled Operation, Extended SOA.

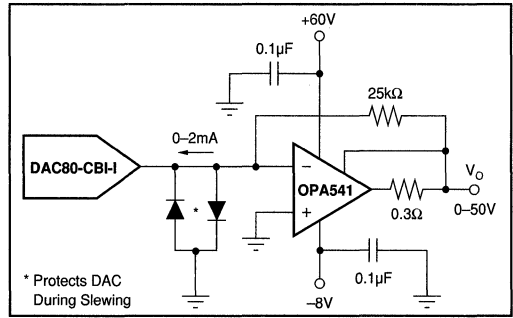


FIGURE 6. Programmable Voltage Source.

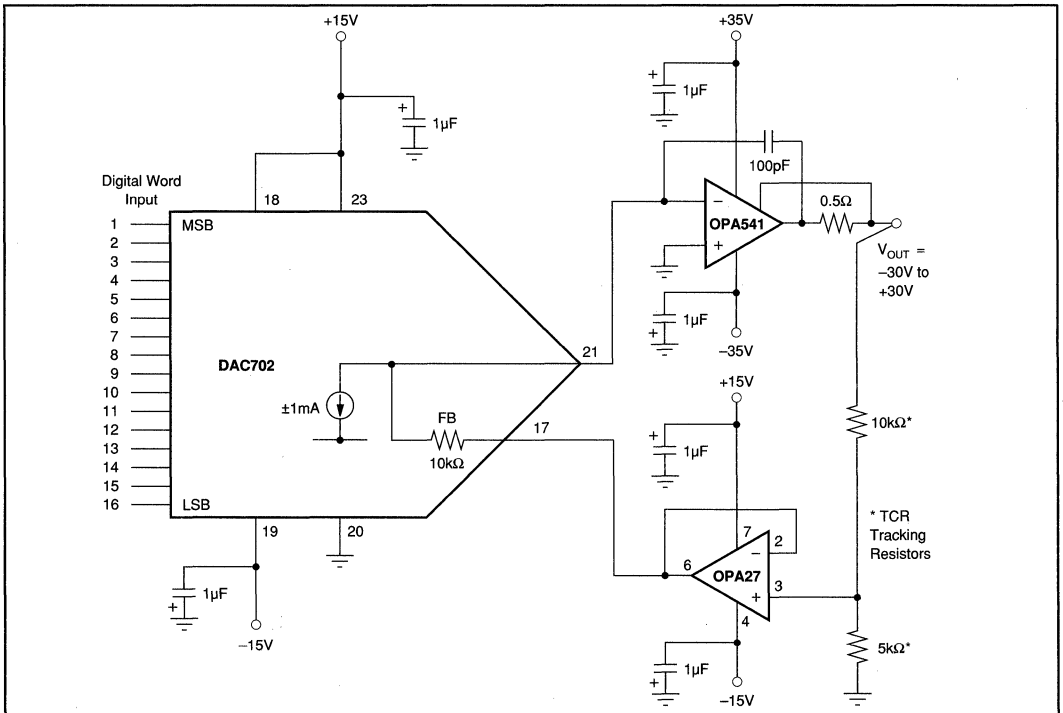


FIGURE 7. 16-Bit Programmable Voltage Source.

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OPA544

OPA544

High-Voltage, High-Current OPERATIONAL AMPLIFIER

3.2

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE: ± 10 to ± 35 V
- SLEW RATE: $8\text{V}/\mu\text{s}$
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: $I_b = 100\text{pA}$ max
- 5-PIN TO-220 PLASTIC PACKAGE

APPLICATIONS

- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER

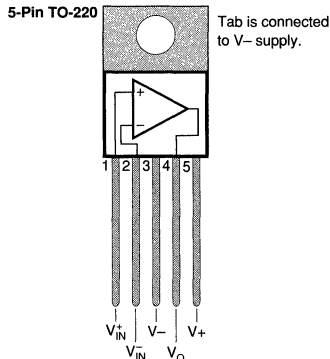
DESCRIPTION

The OPA544 is a high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. High performance FET op amp circuitry and high power output stage are combined on a single monolithic chip.

The OPA544 is protected by internal current limit and thermal shutdown circuits.

The OPA544 comes in an industry-standard 5-pin TO-220 package. Its copper tab allows easy mounting to a heat sink for excellent thermal performance. It is specified for operation over the extended industrial temperature range, -40°C to $+85^\circ\text{C}$.

POWER OPERATIONAL AMPLIFIERS



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PDS-1250

3.2.63

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SPECIFICATIONS

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$ unless otherwise noted.

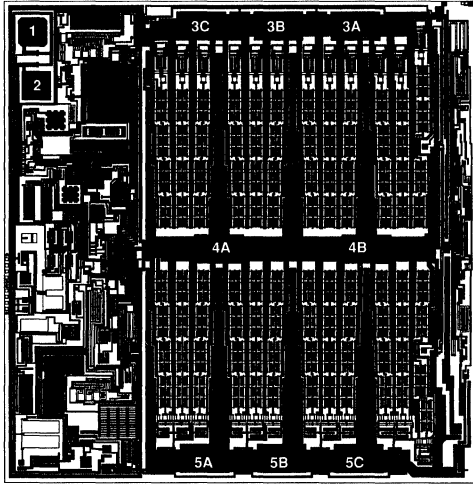
PARAMETER	CONDITION	OPA544T			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply	Specified Temperature Range $V_S = \pm 10V$ to $\pm 35V$		± 1 ± 10 ± 10	± 5 ± 100	mV $\mu V/^{\circ}C$ $\mu V/V$
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0V$ $V_{CM} = 0V$		± 15 See Typical Curve ± 10	± 100 ± 100	pA pA
NOISE Input Voltage Noise Noise Density, $f = 1kHz$ Current Noise Density, $f = 1kHz$			36 3		nV/\sqrt{Hz} fA/\sqrt{Hz}
INPUT VOLTAGE RANGE Common-mode Input Range, Positive Negative Common-mode Rejection	Linear Operation Linear Operation $V_{CM} = \pm V_S - 6V$	(V+) -6 (V-) +6 90	(V+) -4 (V-) +4 106		V V dB
INPUT IMPEDANCE Differential Common-Mode			$10^{12} \parallel 8$ $10^{12} \parallel 10$		$\Omega \parallel pF$ $\Omega \parallel pF$
OPEN-LOOP GAIN Open-loop Voltage Gain	$V_O = \pm 30V$, $R_L = 1k\Omega$	90	103		dB
FREQUENCY RESPONSE Gain Bandwidth Product Slew Rate Full-Power Bandwidth Settling Time 0.1% Total Harmonic Distortion	$R_L = 15\Omega$ $60Vp-p$, $R_L = 15\Omega$ $G = -10$, 60V Step	5	1.4 8 See Typical Curve 25 See Typical Curve		MHz V/ μs μs
OUTPUT Voltage Output, Positive Negative Positive Negative Current Output Short-Circuit Current	$I_O = 2A$ $I_O = 2A$ $I_O = 0.5A$ $I_O = 0.5A$	(V+) -5 (V-) +5 (V+) -4.2 (V-) +4	(V+) -4.4 (V-) +3.8 (V+) -3.8 (V-) +3.1 See SOA Curves 4		V V V V A
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	 $I_O = 0$	± 10	± 35 ± 12	± 35 ± 15	V V mA
TEMPERATURE RANGE Operating Storage Thermal Resistance, θ_{JC} Thermal Resistance, θ_{JC} Thermal Resistance, θ_{JA}	 $f > 50Hz$ DC No Heat Sink	-40 -40	2.7 3 65	+85 +125	$^{\circ}C$ $^{\circ}C$ $^{\circ}C/W$ $^{\circ}C/W$ $^{\circ}C/W$

NOTES: (1) High-speed test at $T_J = 25^{\circ}C$.

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DICE INFORMATION



OPA544 DIE TOPOGRAPHY

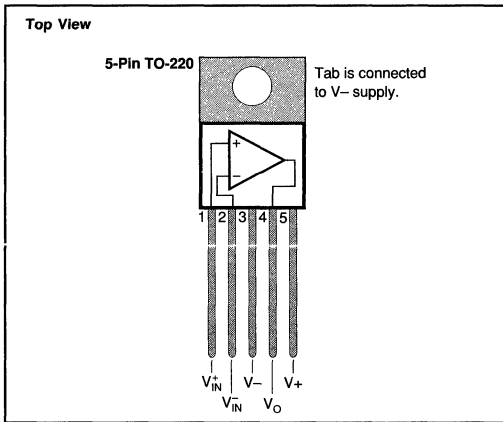
PAD	FUNCTION
1	+In
2	-In
3A, 3B, 3C	V-
4A, 4B	V _O
5A, 5B, 5C	V+

Substrate Bias: Internally connected to V- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	159 x 162 ±5	4.04 x 4.11 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Chromium-Silver	

CONNECTION DIAGRAMS



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA544T	5-Lead TO-220	-40°C to +85°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA544T	5-Lead TO-220	315

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-	70V
Output Current	See SOA Curve
Input Voltage	(V-) -0.7V to (V+) +0.7V
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering -10s)	300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

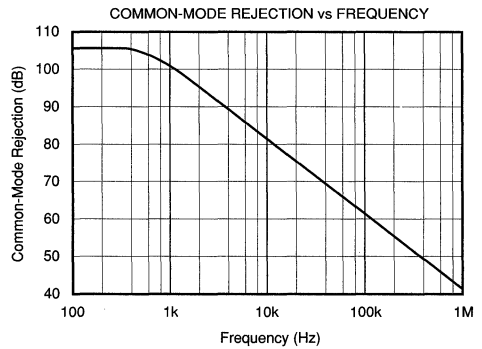
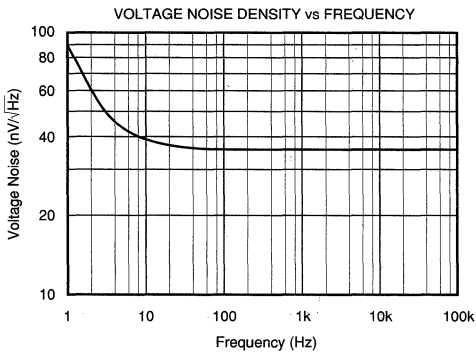
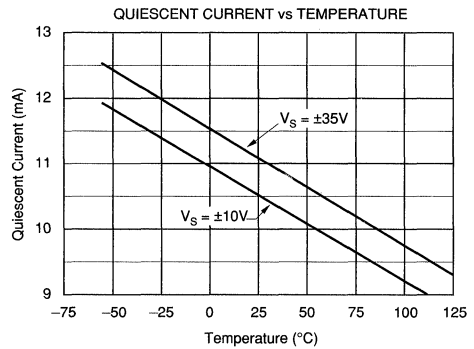
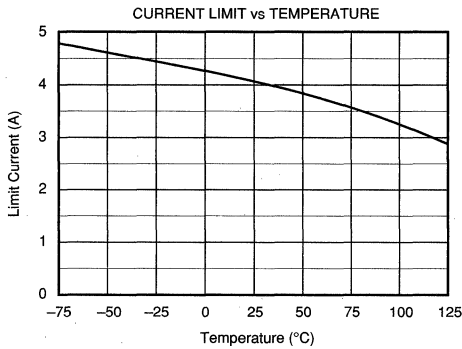
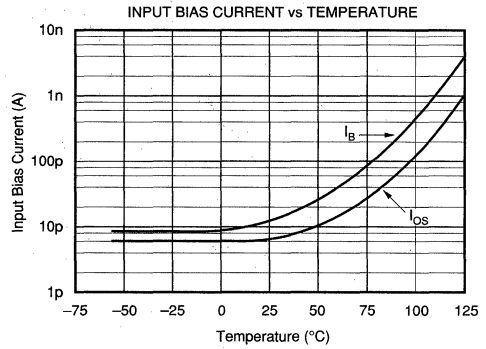
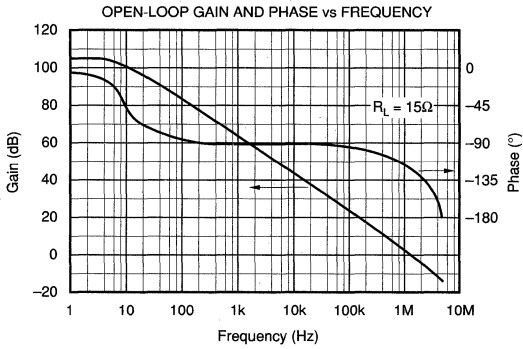
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



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TYPICAL PERFORMANCE CURVES

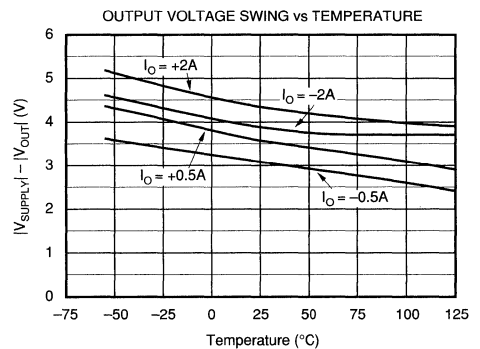
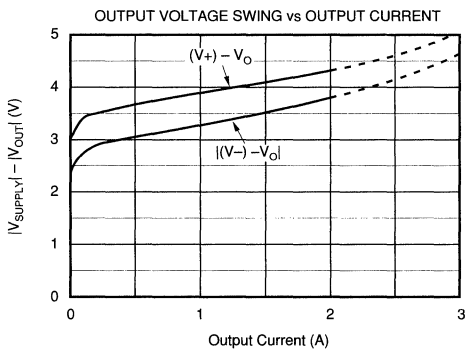
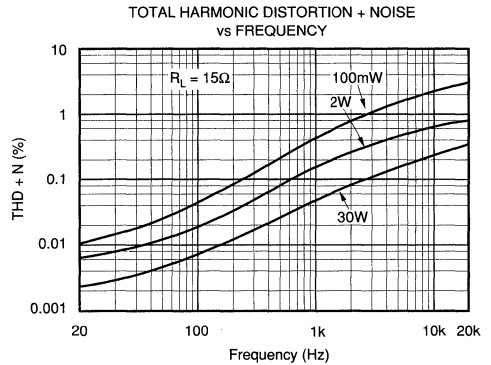
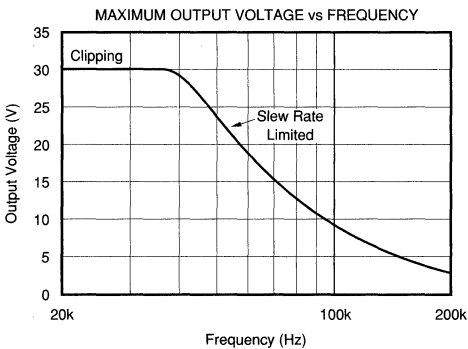
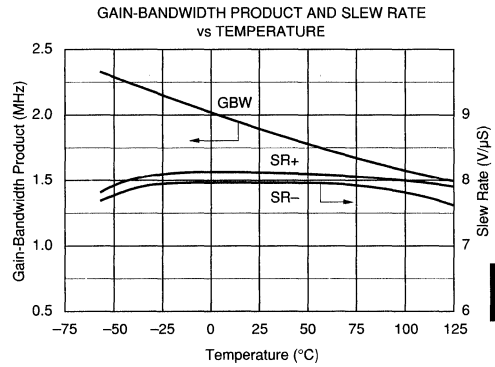
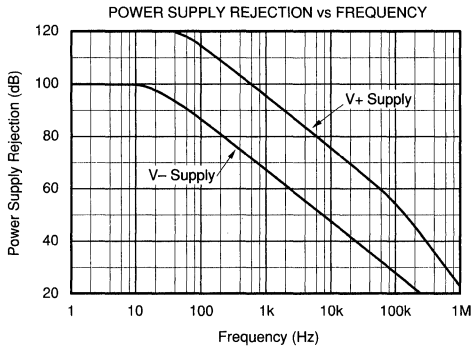
$T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$ unless otherwise noted.



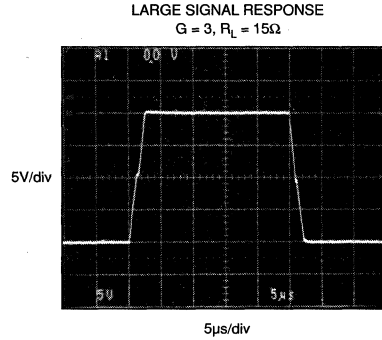
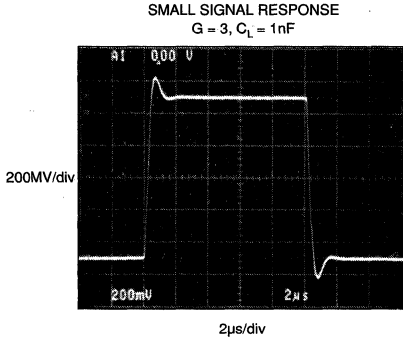
OPA544

3.2

POWER OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$ unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the OPA544 connected as a basic non-inverting amplifier. The OPA544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. Power supply wiring should have low series impedance and inductance.

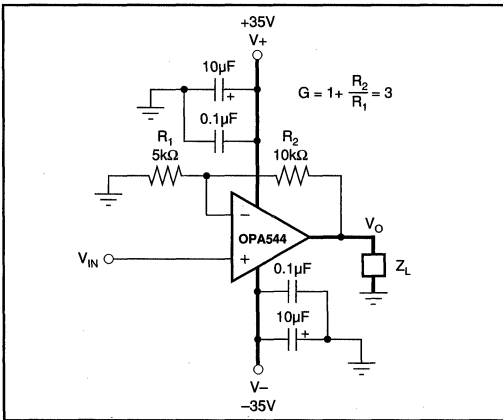


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, V_{CE} . The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE} . The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage ($V+$ or $V-$) across

the conducting transistor. With $V_S = \pm 35V$ the safe output current is 1.5 (at $25^{\circ}C$). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA544. For further insight on SOA, consult Application Bulletin AB-039.

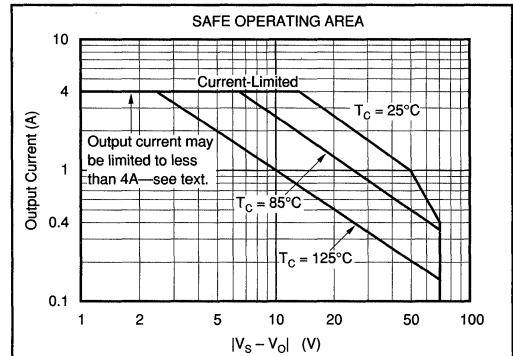


FIGURE 2. Safe Operating Area.

CURRENT LIMIT

The OPA544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit vs Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

THERMAL PROTECTION

The OPA544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately 155°C. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

OUTPUT STAGE COMPENSATION

The complex load impedances common in power op amp applications can cause output stage instability. Figure 3

shows an output series R/C compensation network (1Ω in series with 0.01μF) which generally provides excellent stability. Some variation in circuit values may be required with certain loads.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA544 do not need to be equal. For example, a -6V negative power supply voltage assures that the inputs of the OPA544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power supply could range from 15V to 65V. The total voltage (V- to V+) can range from 20V to 70V. With a 65V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 2. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

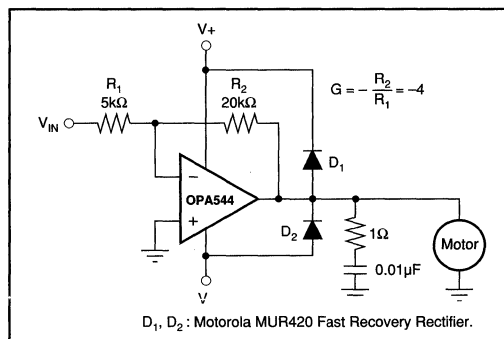


FIGURE 3. Motor Drive Circuit.

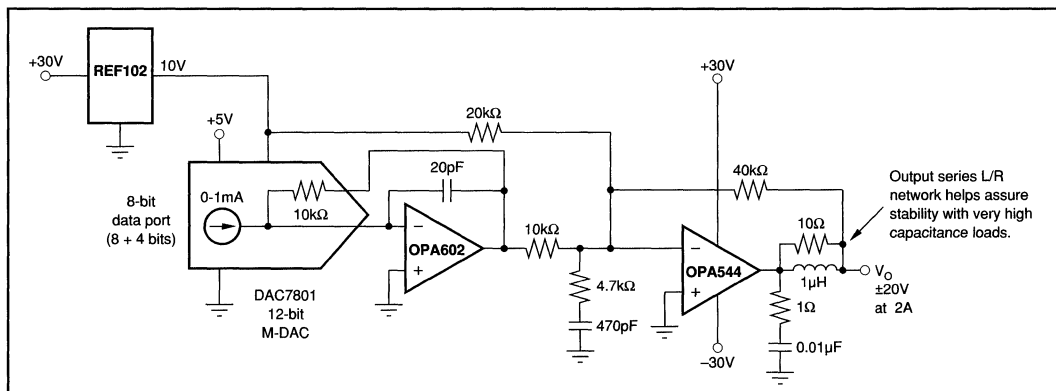
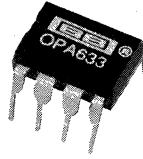


FIGURE 4. Digitally Programmable Power Supply.

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OPA633

High Speed BUFFER AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 260MHz
- HIGH SLEW RATE: 2500V/ μ s
- HIGH OUTPUT CURRENT: 100mA
- LOW OFFSET VOLTAGE: 1.5mV
- REPLACES HA-5033
- IMPROVED PERFORMANCE/PRICE:
LH0033, LTC1010, H0S200

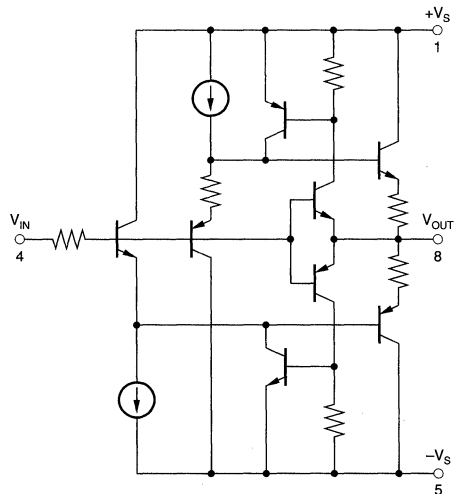
APPLICATIONS

- OP AMP CURRENT BOOSTER
- VIDEO BUFFER
- LINE DRIVER
- A/D CONVERTER INPUT BUFFER

DESCRIPTION

The OPA633 is a monolithic unity-gain buffer amplifier featuring very wide bandwidth and high slew rate. A dielectric isolation process incorporating both NPN and PNP high frequency transistors achieves performance unattainable with conventional integrated circuit technology. Laser trimming provides low input offset voltage.

High output current capability allows the OPA633 to drive 50 Ω and 75 Ω lines, making it ideal for RF, IF and video applications. Low phase shift allows the OPA633 to be used inside amplifier feedback loops. OPA633 is available in a low cost plastic DIP package specified for 0°C to +75°C operation.



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SPECIFICATIONS

ELECTRICAL

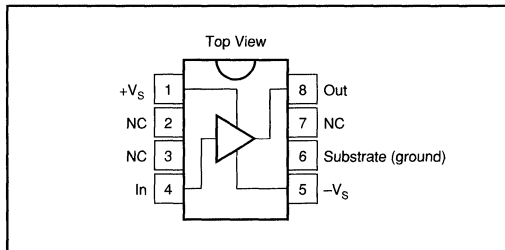
At +25°C, $V_S = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, and $C_L = 10pF$, unless otherwise specified.

PARAMETER	CONDITIONS	OPA633KP			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
Small Signal Bandwidth	$V_O = 1V_{rms}$, $R_L = 1k\Omega$ $V_O = 10V$, $V_S = \pm 15V$, $R_L = 1k\Omega$ $V_O = 500mV$		260		MHz
Full Power Bandwidth			40		MHz
Slew Rate		1000	2500		V/ μs
Rise Time, 10% to 90%			2.5		ns
Propagation Delay			1		ns
Overshoot			10		%
Settling Time, 0.1%			50		ns
Differential Phase Error ⁽¹⁾			0.1		Degrees
Differential Gain Error ⁽¹⁾			0.1		%
Total Harmonic Distortion	$V_O = 1V_{rms}$, $R_L = 1k\Omega$, $f = 100kHz$ $V_O = 1V_{rms}$, $R_L = 100\Omega$, $f = 100kHz$		0.005		%
			0.02		%
OUTPUT CHARACTERISTICS					
Voltage	$T_A = T_{MIN}$ to T_{MAX} $R_L = 1k\Omega$, $V_S = \pm 15V$	± 8	± 10		V
Current		± 11	± 13		V
Resistance		± 80	± 100		mA
			5		Ω
TRANSFER CHARACTERISTICS					
Gain	$R_L = 1k\Omega$ $T_A = T_{MIN}$ to T_{MAX}	0.93	0.95		V/V
			0.99		V/V
			0.92	0.95	
INPUT					
Offset Voltage	$T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX}		± 5	± 15	mV
vs Temperature			± 6	± 25	mV
vs Supply	$T_A = T_{MIN}$ to T_{MAX} $T_A = +25^\circ C$ $T_A = T_{MIN}$ to T_{MAX}	54	± 33		$\mu V/^\circ C$
Bias Current			72		dB
			± 15	± 35	μA
Noise Voltage	$T_A = T_{MIN}$ to T_{MAX} 10Hz to 1MHz		± 20	± 50	μA
Resistance			20		$\mu Vp-p$
Capacitance			1.5		M Ω
			1.6		pF
POWER SUPPLY					
Rated Supply Voltage	Specified Performance		± 12		V
Operating Supply Voltage	Derated Performance	± 5		± 16	V
Current, Quiescent	$I_O = 0$ $I_O = 0$, $T_A = T_{MIN}$ to T_{MAX}		21	25	mA
			21	30	mA
TEMPERATURE RANGE					
Specification, Ambient		0		+75	$^\circ C$
Operating, Ambient		-25		+85	$^\circ C$
$\theta_{Junction}$, Ambient			90		$^\circ C/W$

3.2 POWER OPERATIONAL AMPLIFIERS OPA633

NOTE: (1) Differential phase error in video transmission systems is the change in phase of a color subcarrier resulting from a change in picture signal from blanked to white. Differential gain error is the change in amplitude at the color subcarrier frequency resulting from a change in picture signal from blanked to white.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply, $\pm V_S$	$\pm 20V$
Input Voltage V_{IN}	$+V_S + 2V$ to $-V_S - 2V$
Output Current (peak)	$\pm 20mA$
Internal Power Dissipation (25°C)	1.95W
Junction Temperature	200°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering, 10s)	300°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA633KP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

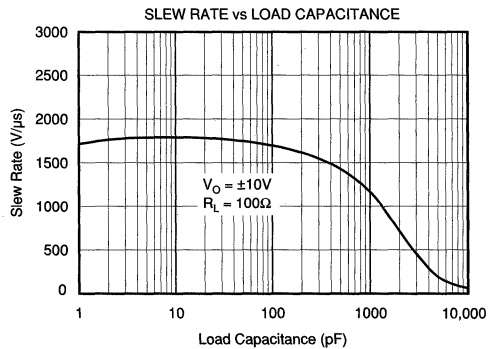
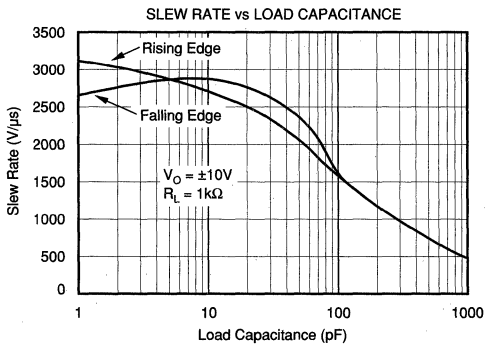
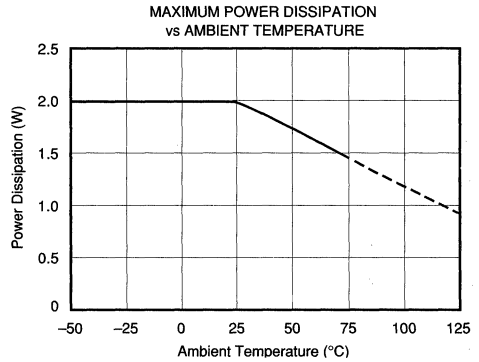
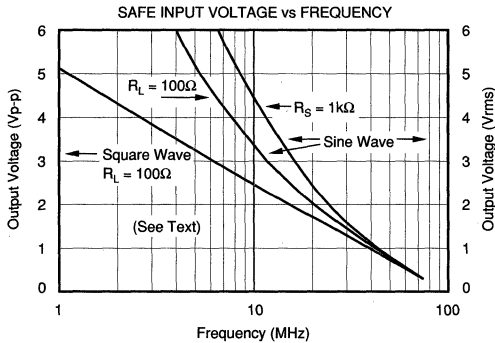
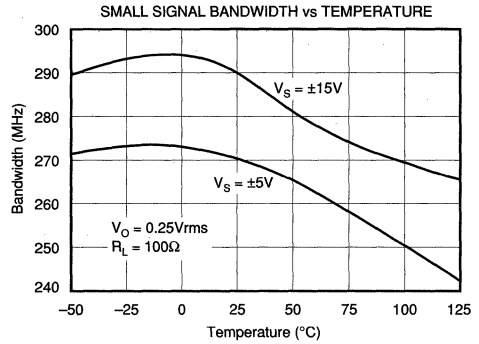
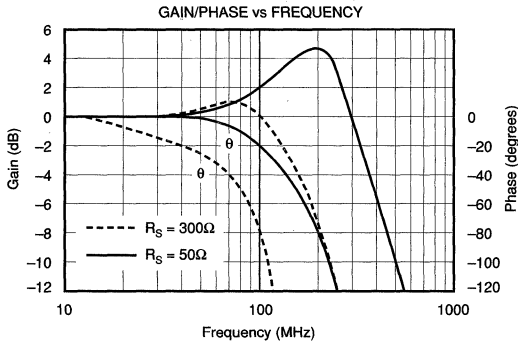
MODEL	PACKAGE	TEMPERATURE RANGE
OPA633KP	8-Pin Plastic DIP	0°C to +75°C



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TYPICAL PERFORMANCE CURVES

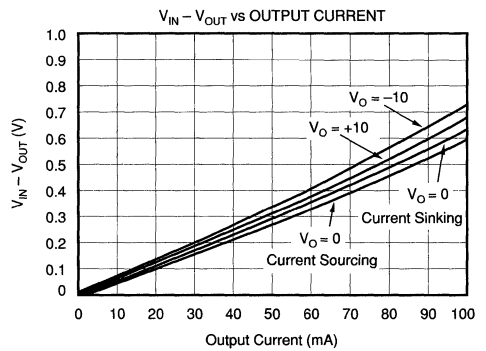
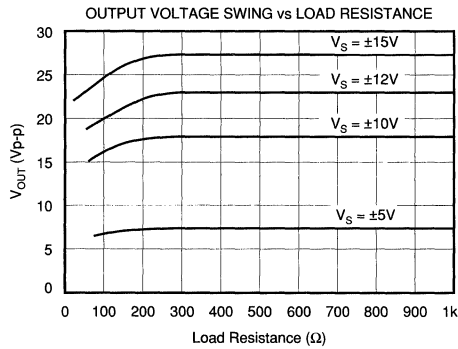
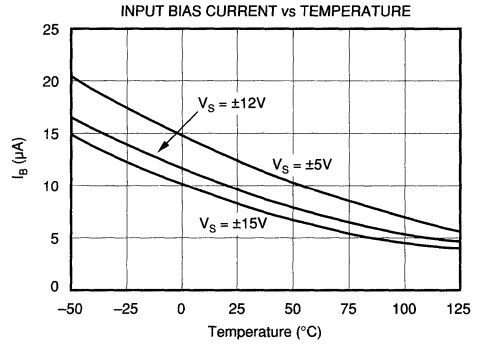
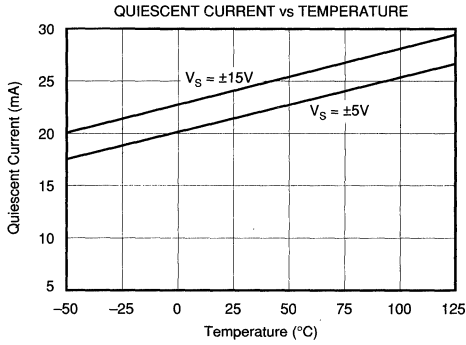
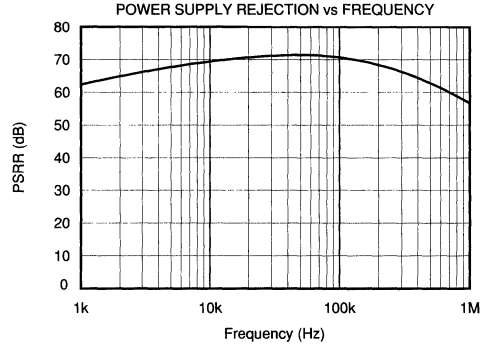
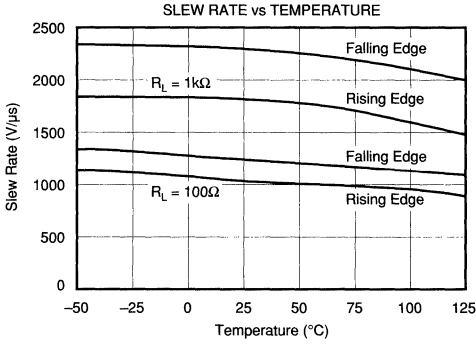
At +25°C, $V_S = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, and $C_L = 10pF$, unless otherwise specified.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, $V_S = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, and $C_L = 10pF$, unless otherwise specified.



OPA633

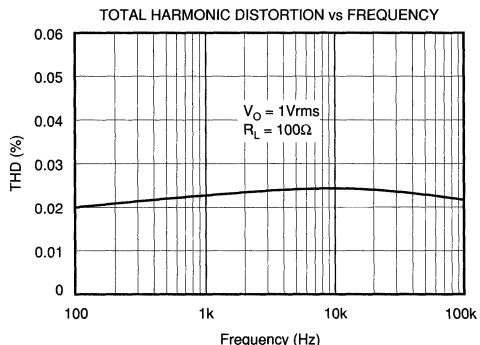
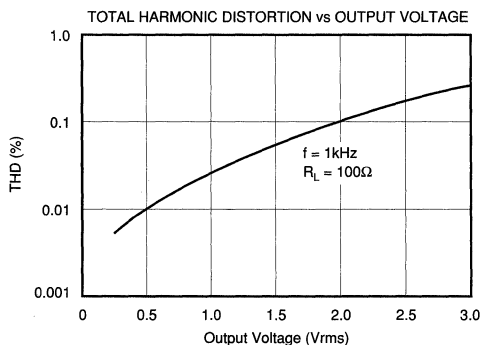
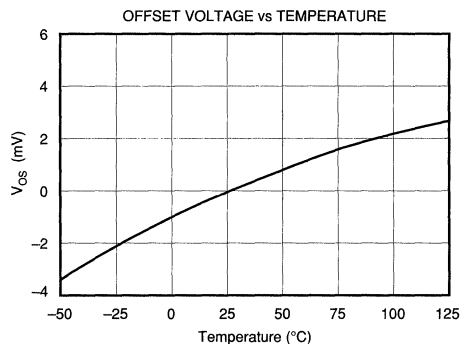
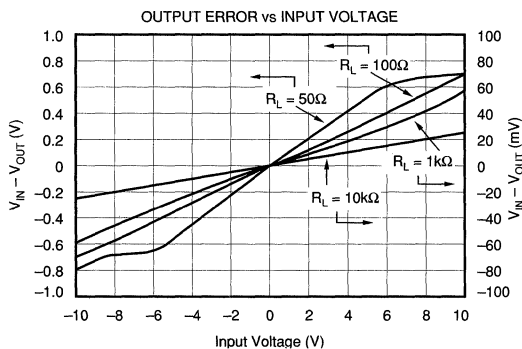
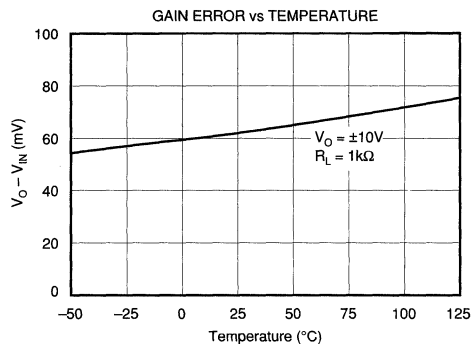
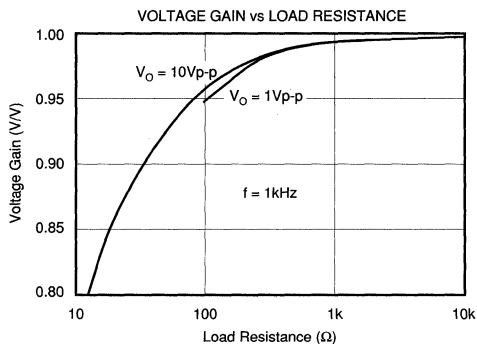
3.2

POWER OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, $V_s = \pm 12V$, $R_s = 50\Omega$, $R_L = 100\Omega$, and $C_L = 10pF$, unless otherwise specified.



APPLICATIONS INFORMATION

As with any high frequency circuitry, good circuit layout technique must be used to achieve optimum performance. Power supply connections must be bypassed with high frequency capacitors. Many applications benefit from the use of two capacitors on each power supply—a ceramic capacitor for good high frequency decoupling and a tantalum type for lower frequencies. They should be located as close as possible to the buffer's power supply pins. A large ground plane is used to minimize high frequency ground drops and stray coupling.

Pin 6 connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to $+V_s$ or $-V_s$, but ground is preferable. The additional lead length and capacitance associated with sockets may cause problems in applications requiring the highest fidelity of high speed pulses.

Depending on the nature of the input source impedance, a series input resistor may be required for best stability. This behavior is influenced somewhat by the load impedance (including any reactive effects). A value of 50Ω to 200Ω is typical. This resistor should be located close to the OPA633's input pin to avoid stray capacitance at the input which could reduce bandwidth (see Gain and Phase versus Frequency curve).

OVERLOAD CONDITIONS

The input and output circuitry of the OPA633 are not protected from overload. When the input signal and load characteristics are within the devices' capabilities, no protection circuitry is required. Exceeding device limits can result in permanent damage.

The OPA633's small package and high output current capability can lead to overheating. The internal junction temperature should not be allowed to exceed 150°C . Although failure is unlikely to occur until junction temperature exceeds 200°C , reliability of the part will be degraded significantly at such high temperatures. Since significant heat transfer takes place through the package leads, wide printed circuit traces to all leads will improve heat sinking. Sockets reduce heat transfer significantly and are not recommended.

Junction temperature rise is proportional to internal power dissipation. This can be reduced by using the minimum supply voltage necessary to produce the required output voltage swing. For instance, 1V video signals can be easily handled with $\pm 5\text{V}$ power supplies thus minimizing the internal power dissipation.

Output overloads or short circuits can result in permanent damage by causing excessive output current. The 50Ω or 75Ω series output resistor used to match line impedance will, in most cases, provide adequate protection. When this resistor is not used, the device can be protected by limiting the power supply current. See "Protection Circuits."

Excessive input levels at high frequency can cause increased internal dissipation and permanent damage. See the safe

input voltage versus frequency curves. When used to buffer an op amp's output, the input to the OPA633 is limited, in most cases, by the op amp. When high frequency inputs can exceed safe levels, the device must be protected by limiting the power supply current.

PROTECTION CIRCUITS

The OPA633 can be protected from damage due to excessive currents by the simple addition of resistors in series with the power supply pins (Figure 5a). While this limits output current, it also limits voltage swing with low impedance loads. This reduction in voltage swing is minimal for AC or high crest factor signals since only the average current from the power supply causes a voltage drop across the series resistor. Short duration load-current peaks are supplied by the bypass capacitors.

The circuit of Figure 5b overcomes the limitations of the previous circuit with DC loads. It allows nearly full output voltage swing up to its current limit of approximately 140mA. Both circuits require good high frequency capacitors (e.g., tantalum) to bypass the buffer's power supply connections.

CAPACITIVE LOADS

The OPA633 is designed to safely drive capacitive loads up to $0.01\mu\text{F}$. It must be understood, however, that rapidly changing voltages demand large output load currents:

$$I_{\text{LOAD}} = C_{\text{LOAD}} \frac{dV}{dt}$$

Thus, a signal slew rate of $1000\text{V}/\mu\text{s}$ and load capacitance of $0.01\mu\text{F}$ demands a load current of 10A. Clearly maximum slew rates cannot be combined with large capacitive loads. Load current should be kept less than 100mA continuous (200mA peak) by limiting the rate of change of the input signal or reducing the load capacitance.

USE INSIDE A FEEDBACK LOOP

The OPA633 may be used inside the feedback path of an op amp such as the OPA602. Higher output current is achieved without degradation in accuracy. This approach may actually improve performance in precision applications by removing load-dependent dissipation from a precision op amp. All vestiges of load-dependent offset voltage and temperature drift can be eliminated with this technique. Since the buffer is placed within the feedback loop of the op amp, its DC errors will have a negligible effect on overall accuracy. Any DC errors contributed by the buffer are divided by the loop gain of the op amp.

The low phase shift of the OPA633 allows its use inside the feedback loop of a wide variety of op amps. To assure stability, the buffer must not add significant phase shift to the loop at the gain crossing frequency of the circuit—the frequency at which the open loop gain of the op amp is equal to the closed loop gain of the application. The OPA633 has a typical phase shift of less than 10° up to 70MHz, thus making it useful even with wideband op amps.

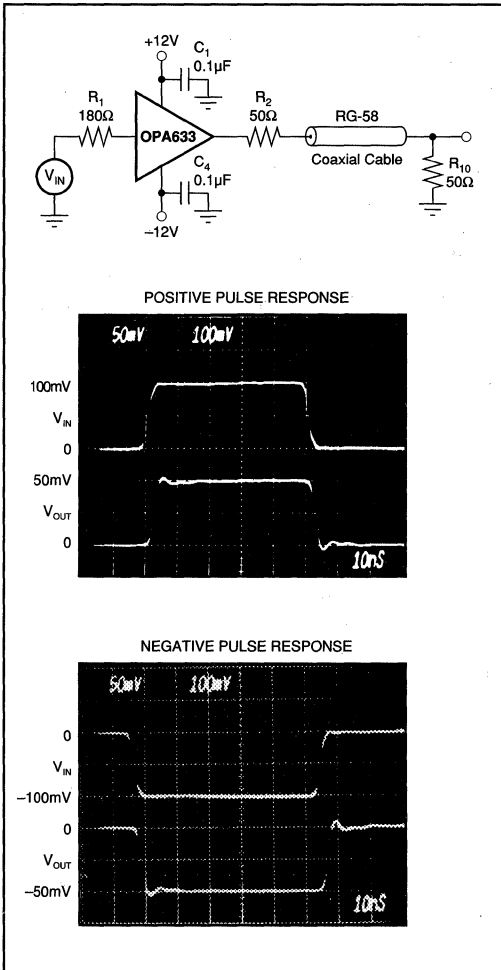


FIGURE 1. Coaxial Cable Driver Circuit.

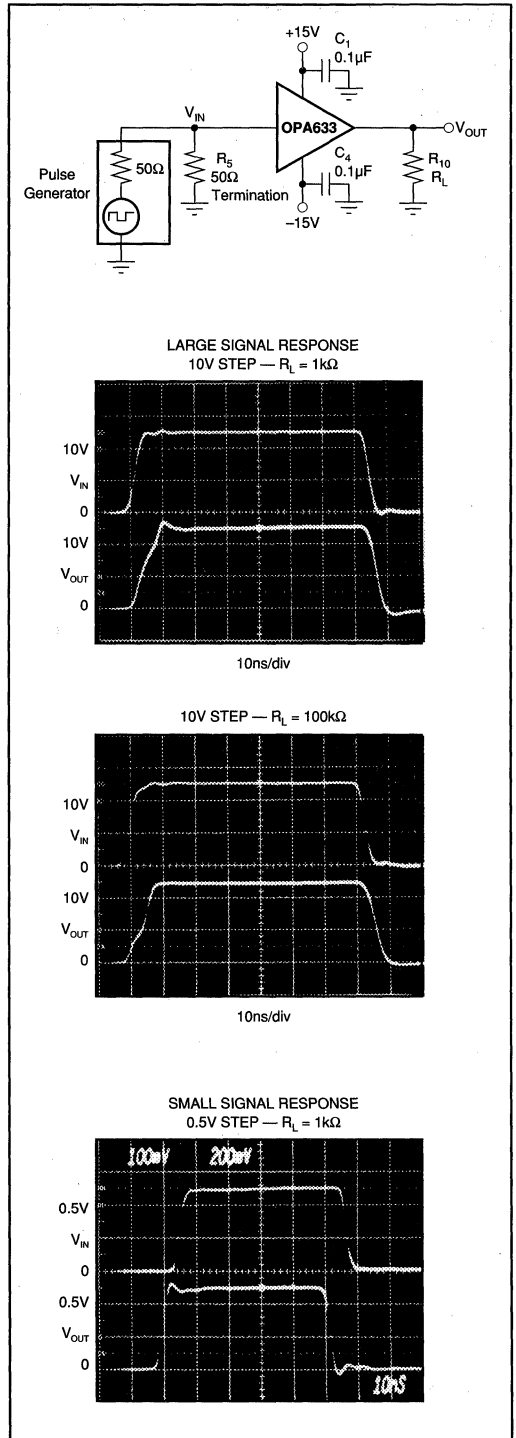


FIGURE 2. Dynamic Response Test Circuit.

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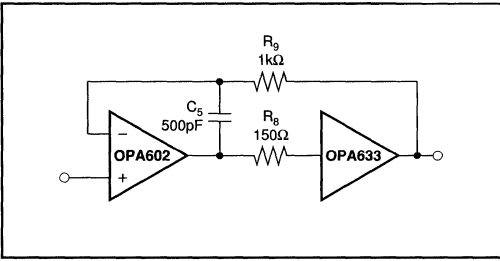


FIGURE 3. Precision High Current Buffer.

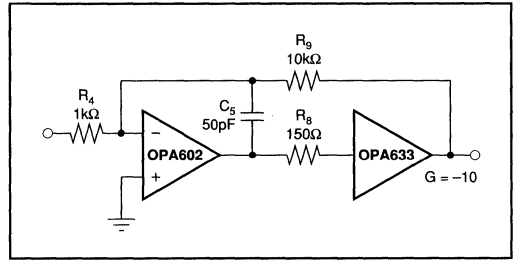


FIGURE 4. Buffered Inverting Amplifier.

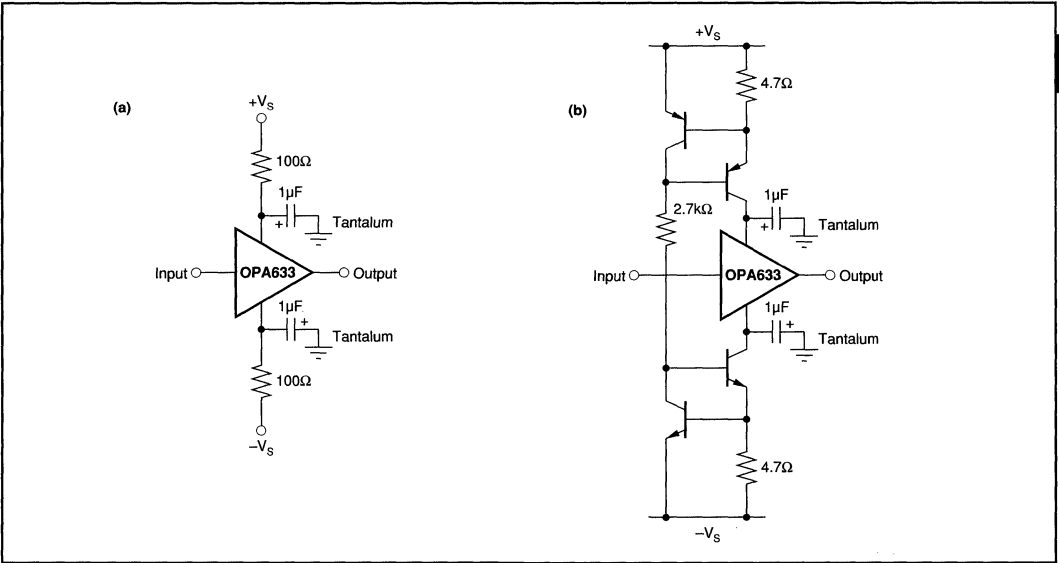
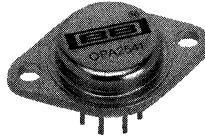


FIGURE 5. Output Protection Circuits.

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OPA2541

Dual High Power OPERATIONAL AMPLIFIER

FEATURES

- OUTPUT CURRENTS TO 5A
- POWER SUPPLIES TO $\pm 40V$
- FET INPUT
- ELECTRICALLY ISOLATED CASE

APPLICATIONS

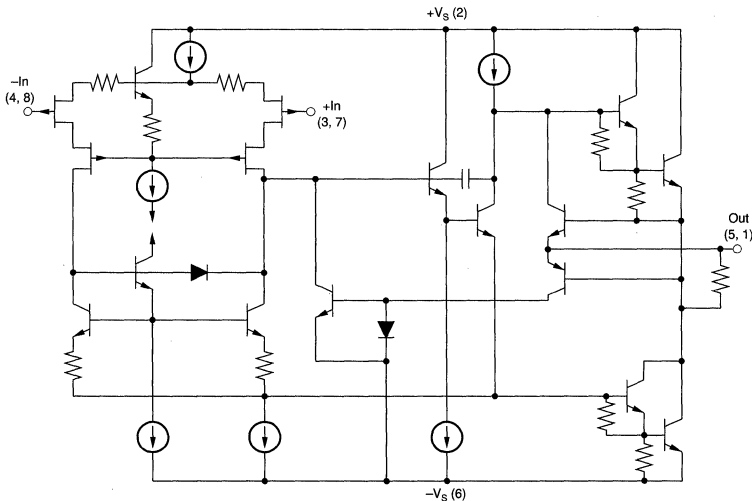
- MOTOR DRIVER
- SERVO AMPLIFIER
- SYNCRO/RESOLVER EXCITATION
- VOICE COIL DRIVER
- BRIDGE AMPLIFIER
- PROGRAMMABLE POWER SUPPLY
- AUDIO AMPLIFIER

DESCRIPTION

The OPA2541 is a dual power operational amplifier capable of operation from power supplies up to $\pm 40V$ and output currents of 5A continuous. With two monolithic power amplifiers in a single package it provides unequaled functional density.

The industry-standard 8-pin TO-3 package is isolated from all internal circuitry allowing it to be mounted directly to a heat sink without insulators which degrade thermal performance. Internal circuitry limits output current to approximately 6A.

The OPA2541 is available in both industrial and military temperature range versions.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

At $T_c = +25^\circ\text{C}$ and $V_s = \pm 35\text{VDC}$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA2541AM			OPA2541BM, SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT OFFSET VOLTAGE								
V_{os} vs Temperature vs Supply Voltage vs Power	Specified Temperature Range $V_s = \pm 10\text{V to } \pm V_{MAX}$		± 2 ± 20 ± 2.5 ± 20	± 10 ± 40 ± 10 ± 60		± 0.25 ± 15 *	± 1 ± 30 *	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{W}$
INPUT BIAS CURRENT								
I_b	Specified Temperature Range		15 Note 1	50		*	*	pA
INPUT OFFSET CURRENT								
I_{os}	Specified Temperature Range		± 5 Note 1	± 30		*	*	pA
INPUT CHARACTERISTICS								
Common-Mode Voltage Range Common-Mode Rejection Input Capacitance Input Impedance, DC	Specified Temperature Range $V_{CM} = (\pm V_s - 6\text{V})$	$\pm (V_s - 6)$ 95	$\pm (V_s - 3)$ 106 5 1		*	*	*	V dB pF $10^{12}\Omega$
GAIN CHARACTERISTICS								
Open Loop Gain at 10Hz Gain-Bandwidth Product	$R_L = 6\Omega$	90	96 1.6		*	*		dB MHz
OUTPUT								
Voltage Swing Current, Continuous	$I_o = 5\text{A}$ $I_o = 2\text{A}$ $I_o = 0.5\text{A}$ +25°C +85°C +125°C (SM grade only)	$\pm (V_s - 5.5)$ $\pm (V_s - 4.5)$ $\pm (V_s - 4)$ 5 4	$\pm (V_s - 4.5)$ $\pm (V_s - 3.6)$ $\pm (V_s - 3.2)$ 7.0 5.0		*	*	*	V V V A A A
AC PERFORMANCE								
Slew Rate Power Bandwidth Settling Time to 0.1% Capacitive Load Phase Margin Channel Separation	$R_L = 8\Omega$, $V_o = 20\text{Vrms}$ 2V Step Specified Temperature Range, $G = 1$ Specified Temperature Range, $G > 10$ Specified Temperature Range, $R_L = 8\Omega$ 1kHz, $R_L = 6\Omega$	6 45	8 55 2 40 80		*	*	*	V/ μs kHz μs nF Degrees dB
POWER SUPPLY								
Power Supply Voltage, $\pm V_s$ Current, Quiescent	Specified Temperature Range Total—Both Amplifiers	± 10	± 30 40	± 35 50	*	± 35 *	± 40 *	V mA
THERMAL RESISTANCE								
θ_{JC} (Junction-to-Case) θ_{JC} θ_{JC} θ_{JC} θ_{JA} (Junction-to-Ambient)	Both Amplifiers ⁽²⁾ , AC Output $f > 60\text{Hz}$ Both Amplifiers ⁽²⁾ , DC Output One Amplifier, AC Output $f > 60\text{Hz}$ One Amplifier, DC Output No Heat Sink		0.8 0.9 1.25 1.4 30	1.0 1.2 1.5 1.9		*	*	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
TEMPERATURE RANGE								
Case	AM, BM SM	-25		+85	*	-55	*	$^\circ\text{C}$ $^\circ\text{C}$

*Specification same as OPA2541AM.

NOTES: (1) Input bias and offset current approximately doubles for every 10°C increase in temperature. (2) Assumes equal dissipation in both amplifiers.

OPA2541

3.2

POWER OPERATIONAL AMPLIFIERS

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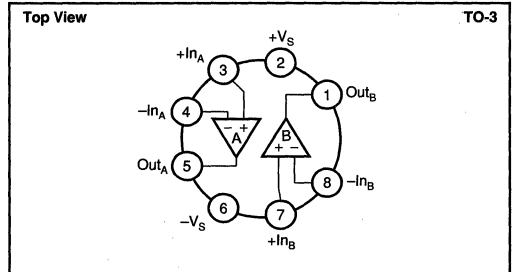
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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$	80V
Output Current	see SOA
Power Dissipation, Internal ⁽¹⁾	125W
Input Voltage: Differential	$\pm V_S$
Common-mode	$\pm V_S$
Temperature: Pin Solder, 10s	+300°C
Junction ⁽¹⁾	+150°C
Temperature Range:	
Storage	-65°C to +150°C
Operating (Case)	-55°C to +125°C

NOTE: (1) Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CONNECTION DIAGRAM



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA2541AM	TO-3	030
OPA2541BM	TO-3	030
OPA2541SM	TO-3	030

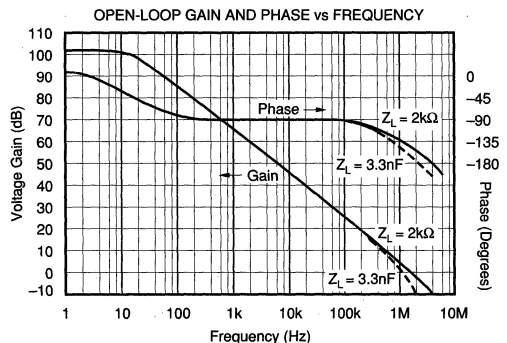
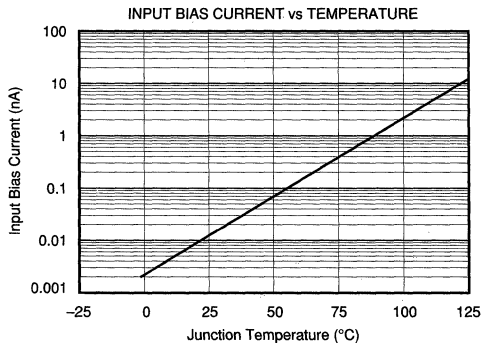
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2541AM	TO-3	-25°C to +85°C
OPA2541BM	TO-3	-25°C to +85°C
OPA2541SM	TO-3	-55°C to +125°C

TYPICAL PERFORMANCE CURVES

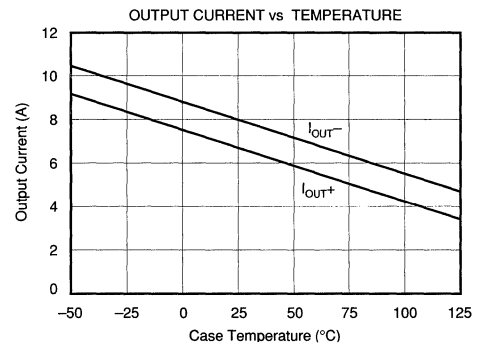
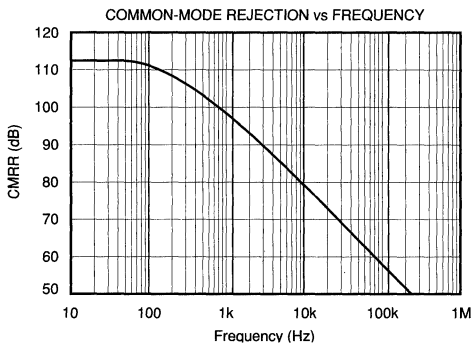
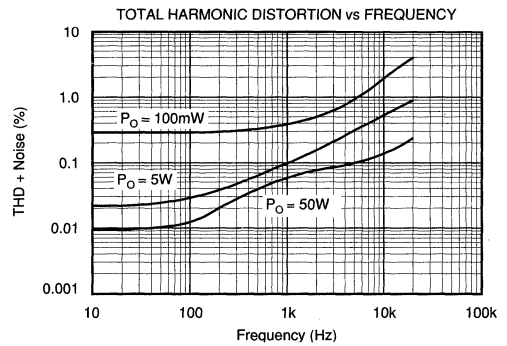
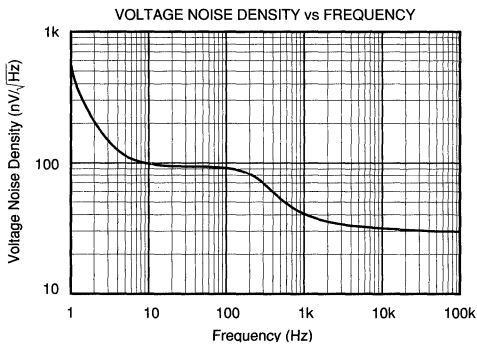
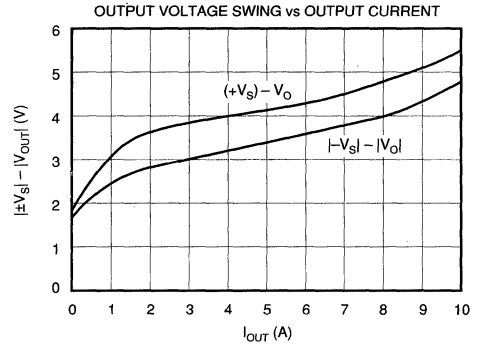
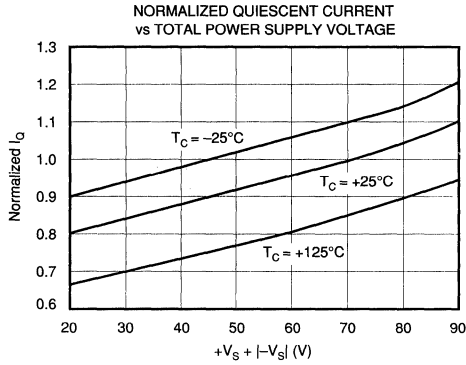
$T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ and $V_S = \pm 35\text{VDC}$, unless otherwise noted.



OPA2541

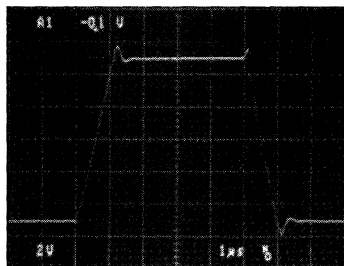
3.2

POWER OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

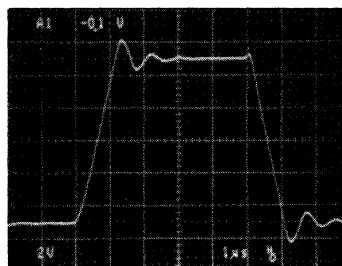
$T_A = +25^\circ\text{C}$ and $V_S = \pm 35\text{VDC}$, unless otherwise noted.

DYNAMIC RESPONSE



$Z_{\text{LOAD}} = \infty$, $V_S = \pm 35\text{V}$, $A_V = +1$

DYNAMIC RESPONSE



$Z_{\text{LOAD}} = 4700\text{pF}$, $V_S = \pm 35\text{V}$, $A_V = +1$

INSTALLATION INSTRUCTIONS

POWER SUPPLIES

The OPA2541 is specified for operation from power supplies up to $\pm 40\text{V}$. It can also be operated from an unbalanced or a single power supply so long as the total power supply voltage does not exceed 80V (70V for "AM" grade). The power supplies should be bypassed with low series impedance capacitors such as ceramic or tantalum. These should be located as near as practical to the amplifier's power supply pins. Good power amplifier circuit layout is, in general, like good high-frequency layout. Consider the path of large power supply and output currents. Avoid routing these connections near low-level input circuitry to avoid waveform distortion and instability.

Signal dependent load current can modulate the power supply voltage with inadequate power supply bypassing. This can affect both amplifiers' outputs. Since the second amplifier's signal may not be related to the first, this will degrade the inherent channel separation of the OPA2541.

HEAT SINKING

Most applications will require a heat sink to prevent junction temperatures from exceeding the 150°C maximum rating. The type of heat sink required will depend on the output signals, power dissipation of each amplifier, and ambient temperature. The thermal resistance from junction-to-case, θ_{JC} , depends on how the power dissipation is distributed on the amplifier die.

DC output concentrates the power dissipation in one output transistor. AC output distributes the power dissipation equally between the two output transistors and therefore has lower thermal resistance. Similarly, the power dissipation may be all in one amplifier (worst case) or equally distributed between the two amplifiers (best case). Thermal resistances are provided for each of these possibilities. The case-to-junction temperature rise is the product of the power dissi-

pation (total of both amplifiers) times the appropriate thermal resistance—

$$\Delta T_{\text{JC}} = (P_{\text{D total}}) (\theta_{\text{JC}}).$$

Sufficient heat sinking must be provided to keep the case temperature within safe limits for the maximum ambient temperature and power dissipation. The thermal resistance of the heat sink required may be calculated by:

$$\theta_{\text{HS}} = (150^\circ\text{C} - \Delta T_{\text{JC}} - T_A) / P_{\text{D}}.$$

Commercially available heat sinks usually specify thermal resistance. These ratings are often suspect, however, since they depend greatly on the mounting environment and air flow conditions. Actual thermal performance should be verified by measurement of case temperature under the required load and environmental conditions.

No insulating hardware is required when using the OPA2541. Since mica and other similar insulators typically add $0.7^\circ\text{C}/\text{W}$ thermal resistance, this is a significant advantage. See Burr-Brown Application Note AN-83 for further details on heat sinking.

SAFE OPERATING AREA

The Safe Operating Area (SOA) curve provides comprehensive information on the power handling abilities of the OPA2541. It shows the allowable output current as a function of the voltage across the conducting output transistor (see Figure 1). This voltage is equal to the power supply voltage minus the output voltage. For example, as the amplifier output swings near the positive power supply voltage, the voltage across the output transistor decreases and the device can safely provide large output currents demanded by the load.

The internal current limit will not provide short-circuit protection in most applications. When the amplifier output is shorted to ground, the full power supply voltage is impressed across the conducting output transistor. For instance, with $V_s = \pm 35V$, a short circuit to ground would impress 35V across the conducting power transistor. The maximum safe output current at this voltage is 1.8A, so the internal current limit would not protect the amplifier. The unit-to-unit variation and temperature dependence of the internal current limit suggest that it be used to handle abnormal conditions and not activated in commonly encountered circuit operation.

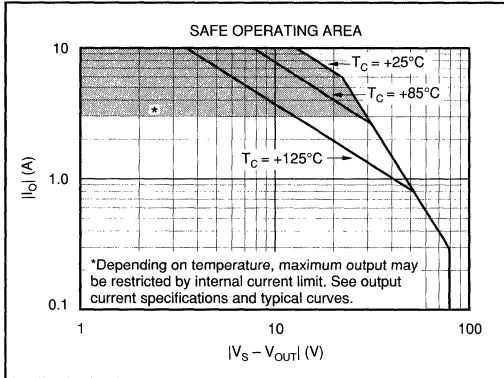


FIGURE 1. Safe Operating Area.

Reactive, or EMF generating loads such as DC motors can present demanding SOA requirements. With a purely reactive load, output voltage current occurs when the output voltage is zero and the voltage across the conducting transistor is equal to the full power supply voltage. See Burr-Brown Application Note AN-123 for further information on evaluating SOA.

Applications with inductive or EMF-generating loads which can produce "kick back" voltage surges to the amplifiers should include clamp diodes from the output terminals to the power supplies. These diodes should be chosen to limit the peak amplifier output voltage surges to less than 2V beyond the power supply rail voltage. Common 1A rated rectifier diodes will suffice in most applications.

APPLICATIONS CIRCUITS

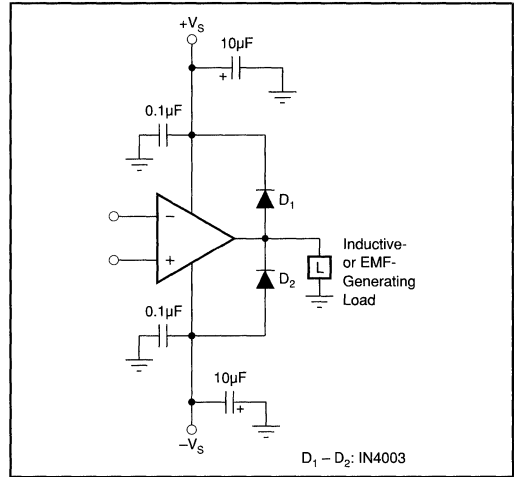


FIGURE 2. Clamping Output for EMF-Generating Loads.

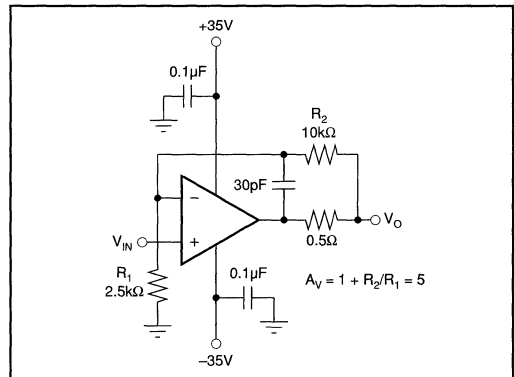


FIGURE 3. Isolating Capacitive Loads.

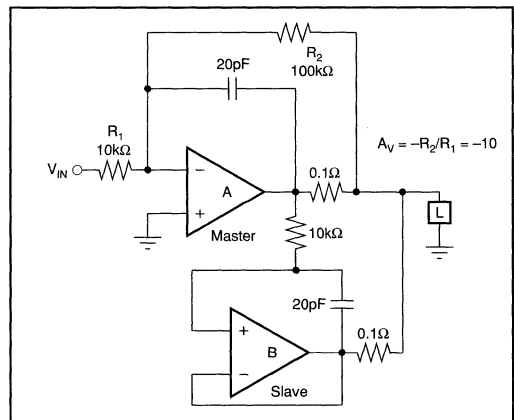


FIGURE 4. Paralleled Operation, Extended SOA.

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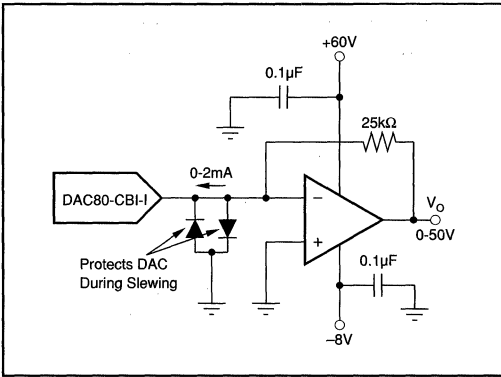


FIGURE 5. Programmable Voltage Source.

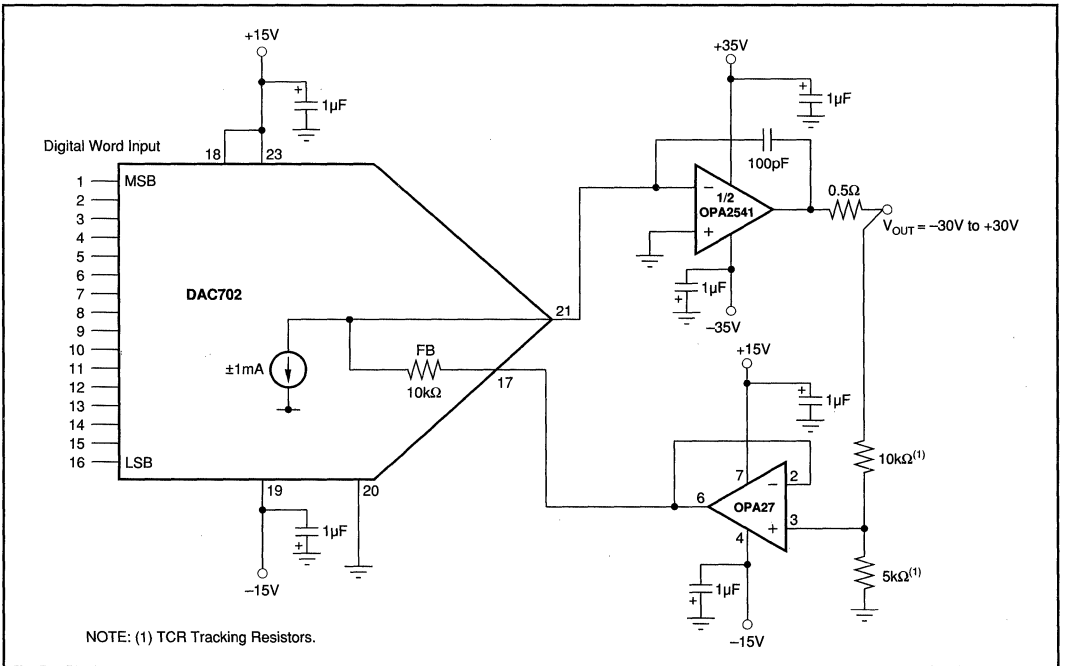


FIGURE 6. 16-Bit Programmable Voltage Source.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

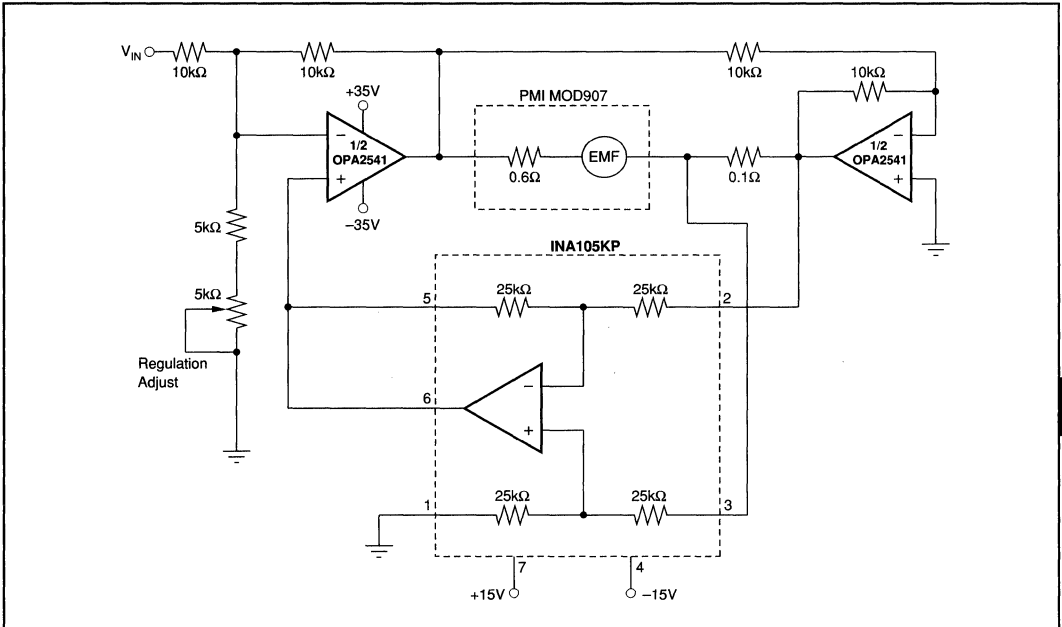


FIGURE 7. Bridge Amplifier Motor-Speed Controller.

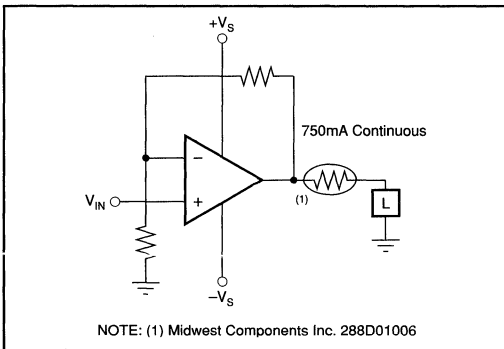
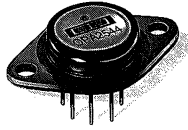


FIGURE 8. Limiting Output Current.

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OPA2544

High-Voltage, High-Current DUAL OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT CURRENT: 2A min
- WIDE POWER SUPPLY RANGE:
 ± 10 to $\pm 35V$
- SLEW RATE: $8V/\mu s$
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- FET INPUT: $I_B = 50pA$ max
- 8-PIN TO-3 METAL PACKAGE
- ELECTRICALLY ISOLATED CASE

DESCRIPTION

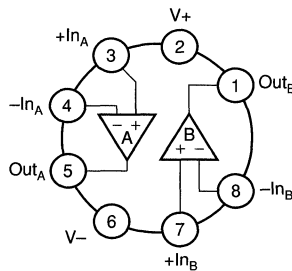
The OPA2544 is a dual high-voltage/high-current operational amplifier suitable for driving a wide variety of high power loads. It provides 2A output current and power supply voltage range extends to $\pm 35V$.

The OPA2544 integrates two high performance FET op amps with high power output stages on a single monolithic chip. Internal current limit and thermal shutdown protect the amplifier and load from damage.

The OPA2544 is available in a hermetic 8-pin metal TO-3 package, specified for operation over the $-40^\circ C$ to $+85^\circ C$ and $-55^\circ C$ to $+125^\circ C$ temperature ranges.

APPLICATIONS

- MOTOR DRIVER
- PROGRAMMABLE POWER SUPPLY
- SERVO AMPLIFIER
- VALVES, ACTUATOR DRIVER
- MAGNETIC DEFLECTION COIL DRIVER
- AUDIO AMPLIFIER



Top View

Case Electrically
Isolated

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PRELIMINARY SPECIFICATIONS

T_{CASE} = +25°C, V_S = ±35V unless otherwise noted.

PARAMETER	CONDITIONS	OPA2544BM			OPA2544SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply	Specified Temp. Range V _S = ±10V to ±35V		±1 ±10 ±1Q	±5 ±100		*	*	mV μV/°C μV/V
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature Input Offset Current	V _{CM} = 0V V _{CM} = 0V		±15 Doubles every 10°C ±10	±50 ±50		*	*	pA pA
NOISE Input Voltage Noise Noise Density, f = 1kHz Current Noise Density, f = 1kHz			36 3			*		nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-mode Input Range Positive Negative Common-mode Rejection	Linear Operation Linear Operation V _{CM} = ±V _S -6V	(V ₊) -6 (V ₋) +6 90	(V ₊) -4 (V ₋) +4 106		*	*	*	V V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹² 8 10 ¹² 10			*	*	Ω pF Ω pF
OPEN-LOOP GAIN Open-loop Voltage Gain	V _O = ±30V, R _L = 15Ω	90	103		*	*		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Full-Power Bandwidth Settling Time 0.1% Total Harmonic Distortion	R _L = 15Ω 60Vp-p, R _L = 15Ω G = -10, 60V Step	5	1.4 8 See Typical Curve 25 See Typical Curve		*	*	*	MHz V/μs μs
OUTPUT Voltage Output: Positive Negative Positive Negative Current Output Short-Circuit Current	I _O = 2A I _O = 2A I _O = 0.5A I _O = 0.5A	(V ₊) -5 (V ₋) +5 (V ₊) -4.2 (V ₋) +4	(V ₊) -4.4 (V ₋) +3.8 (V ₊) -3.8 (V ₋) +3.1 See SOA Curves 4		*	*	*	V V V V A
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (total)	 I _O = 0	±10	±35 ±22	±35 ±30	*	*	*	V V mA
TEMPERATURE RANGE Operating Range Storage Thermal Resistance, θ _{JC} ² Thermal Resistance, θ _{JC} ² Thermal Resistance, θ _{JC} ² Thermal Resistance, θ _{JC} ² Thermal Resistance, θ _{JK} ²	Both Amplifiers, f > 50Hz Both Amplifiers, DC One Amplifier, f > 50Hz One Amplifier, DC No Heat Sink	-40 -65	2 2.5 2.7 3 30	+85 +125	-55 *		+125 *	°C °C °C/W °C/W °C/W °C/W

NOTES: (1) High-speed test at T_J = 25°C. (2) Calculated from total power dissipation of both amplifiers.

OPA2544

3.2

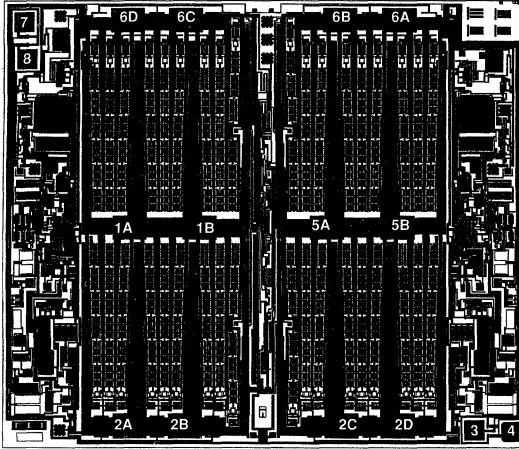
POWER OPERATIONAL AMPLIFIERS

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DICE INFORMATION



OPA2544 DIE TOPOGRAPHY

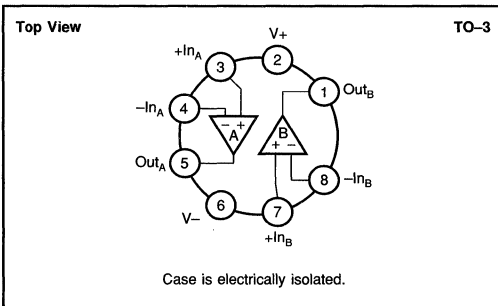
PAD	FUNCTION
1A, 1B	Out _B
2A, 2B, 2C, 2D	V ₊
3	+In _A
4	-In _A
5A, 5B	Out _A
6A, 6B, 6C, 6D	V ₋
7	+In _B
8	-In _B

Substrate Bias: Internally connected to V₋ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	218 x 252 ±5	8.58 x 9.92 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Chromium-Silver	

CONNECTION DIAGRAMS



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA2544BM	8-Pin Metal TO-3	-40°C to +85°C
OPA2544SM	8-Pin Metal TO-3	-55°C to +125°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA2544BM	8-Pin Metal TO-3	030
OPA2544SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V ₊ to V ₋	70V
Output Current	See SOA Curve
Input Voltage	(V ₋) -0.7V to (V ₊) +0.7V
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering -10s)	300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

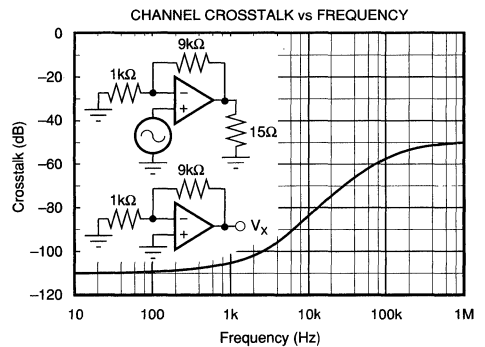
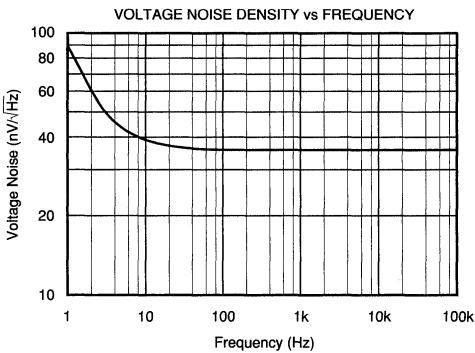
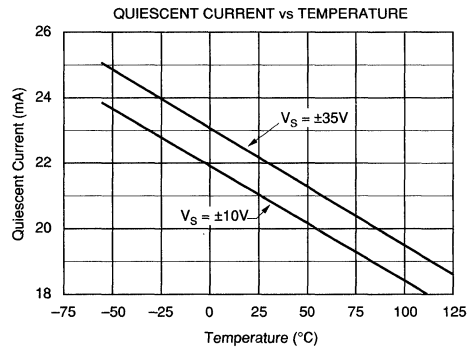
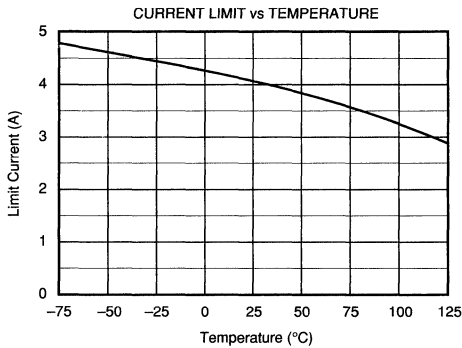
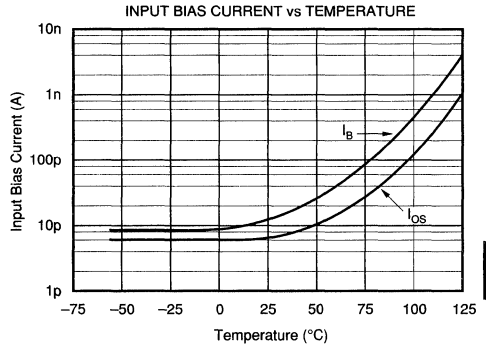
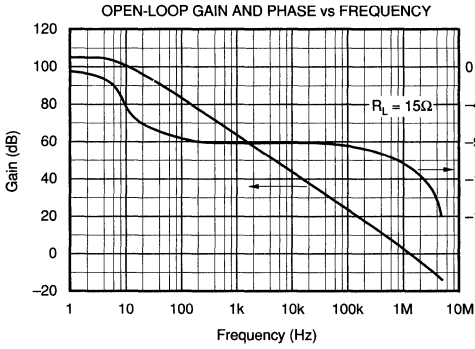
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 35V$ unless otherwise noted.



OPA2544

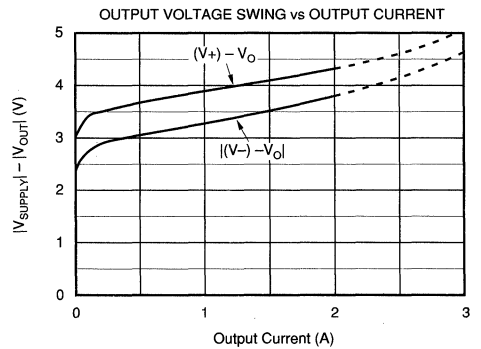
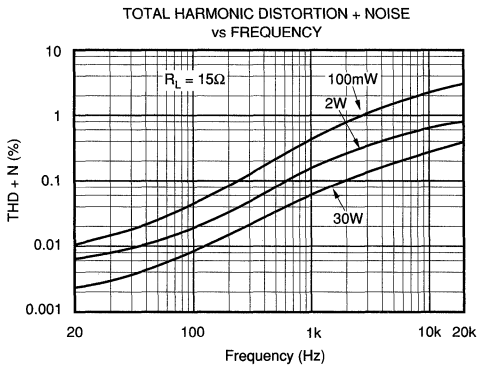
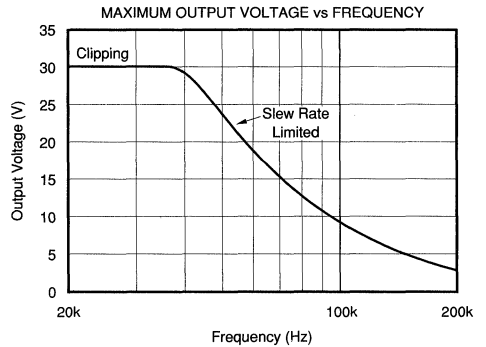
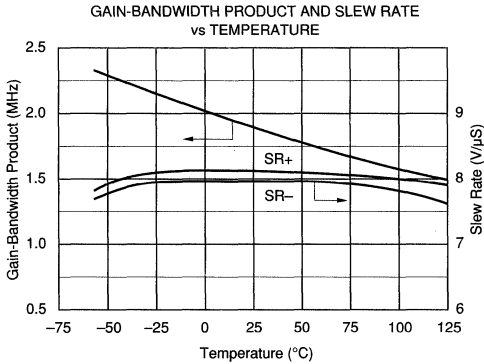
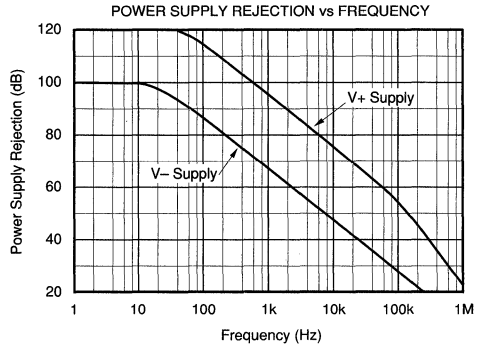
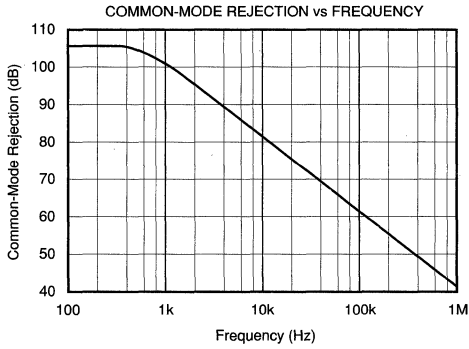
3.2

POWER OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

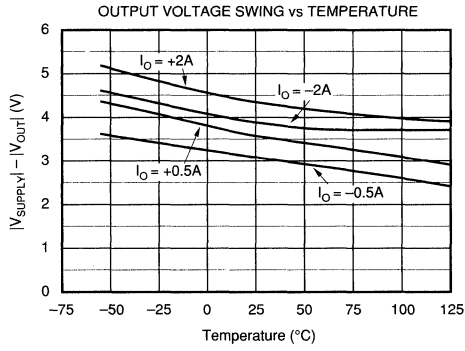
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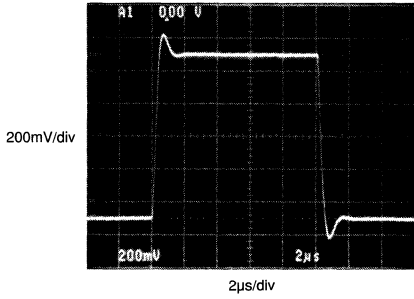
Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

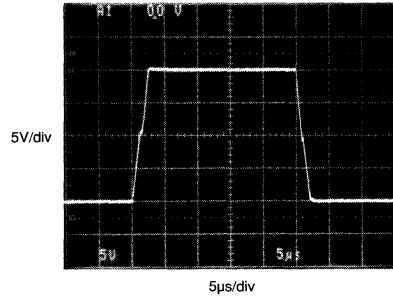
$T_A = +25^\circ\text{C}$, $V_S = \pm 35\text{V}$ unless otherwise noted.



SMALL SIGNAL RESPONSE
 $G = 3$, $C_L = 1\text{nF}$



LARGE SIGNAL RESPONSE
 $G = 3$, $R_L = 15\Omega$



OPA2544

3.2

POWER OPERATIONAL AMPLIFIERS

APPLICATIONS INFORMATION

Figure 1 shows the OPA2544 connected as a basic non-inverting amplifier. The OPA2544 can be used in virtually any op amp configuration. Power supply terminals should be bypassed with low series impedance capacitors. The technique shown, using a ceramic and tantalum type in parallel is recommended. Power supply wiring should have low series impedance and inductance.

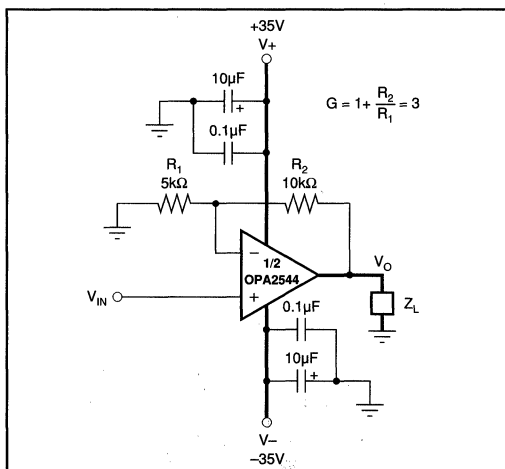


FIGURE 1. Basic Circuit Connections.

SAFE OPERATING AREA

Stress on the output transistors is determined by the output current and the voltage across the conducting output transistor, V_{CE} . The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, V_{CE} . The Safe Operating Area (SOA curve, Figure 2) shows the permissible range of voltage and current.

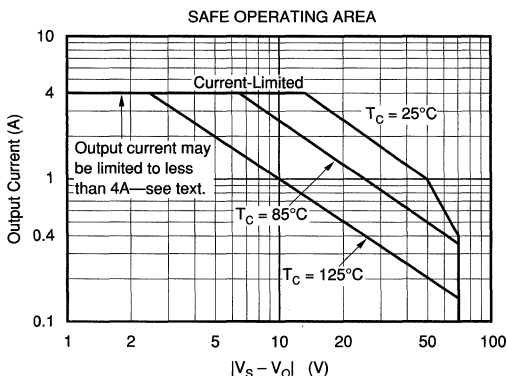


FIGURE 2. Safe Operating Area.

The safe output current decreases as V_{CE} increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V_+ or V_-) across the conducting transistor. With $V_S = \pm 35V$ the safe output current is 1.5 (at $25^\circ C$). The short-circuit current is approximately 4A which exceeds the SOA. This situation will activate the thermal shutdown circuit in the OPA2544. For further insight on SOA, consult AB-039.

CURRENT LIMIT

The OPA2544 has an internal current limit set for approximately 4A. This current limit decreases with increasing junction temperature as shown in the typical curve, Current Limit vs Temperature. This, in combination with the thermal shutdown circuit, provides protection from many types of overload. It may not, however, protect for short-circuit to ground, depending on the power supply voltage, ambient temperature, heat sink and signal conditions.

POWER DISSIPATION

Power dissipation depends on power supply, signal and load conditions. For dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

HEATSINKING

Most applications require a heat sink to assure that the maximum junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions. Consult Application Bulletin AB-038 for information on determining heat sink requirements.

The case of the OPA2544 is electrically isolated from all circuitry and can be connected directly to a heat sink. This eliminates cumbersome insulating hardware that increases thermal resistance. Consult Application Bulletin AB-037 for proper mounting techniques and procedures for TO-3 power products.

THERMAL PROTECTION

The OPA2544 has thermal shutdown that protects the amplifier from damage. Any tendency to activate the thermal shutdown circuit during normal operation is indication of excessive power dissipation or an inadequate heat sink.

The thermal protection activates at a junction temperature of approximately $155^\circ C$. For reliable operation, junction temperature should be limited to $150^\circ C$, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal

protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than 25°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Depending on load and signal conditions, the thermal protection circuit may produce a duty-cycle modulated output signal. This limits the dissipation in the amplifier, but the rapidly varying output waveform may be damaging to some loads. The thermal protection may behave differently depending on whether internal dissipation is produced by sourcing or sinking output current.

UNBALANCED POWER SUPPLIES

Some applications do not require equal positive and negative output voltage swing. The power supply voltages of the OPA2544 do not need to be equal. For example, a -5V negative power supply voltage assures that the inputs of the OPA2544 are operated within their linear common-mode range, and that the output can swing to 0V. The V+ power

supply could range from 15V to 65V. The total voltage (V- to V+) can range from 20V to 70V. With a 65V positive supply voltage, the device may not be protected from damage during short-circuits because of the larger V_{CE} during this condition.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies as shown in Figure 2. Fast-recovery rectifier diodes with a 4A or greater continuous rating are recommended.

SOCKET

A socket, Burr-Brown model 0804MC is available for the OPA2544. Although not required, this socket makes mounting and interchanging parts easy, especially during design and testing.

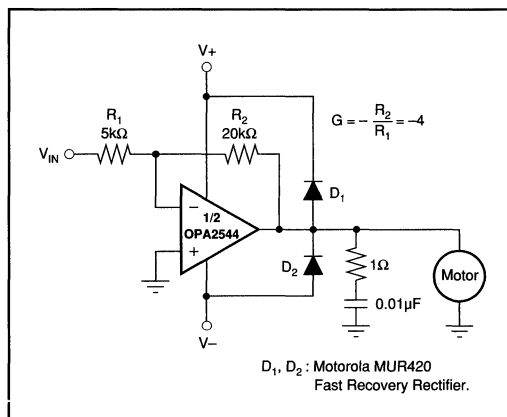


FIGURE 3. Motor Drive Circuit.

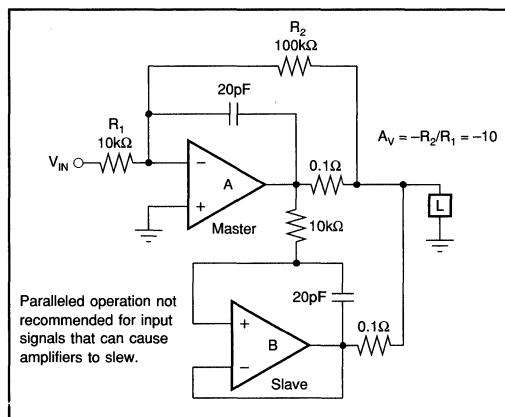


FIGURE 5. Paralleled Operation, Extended SOA.

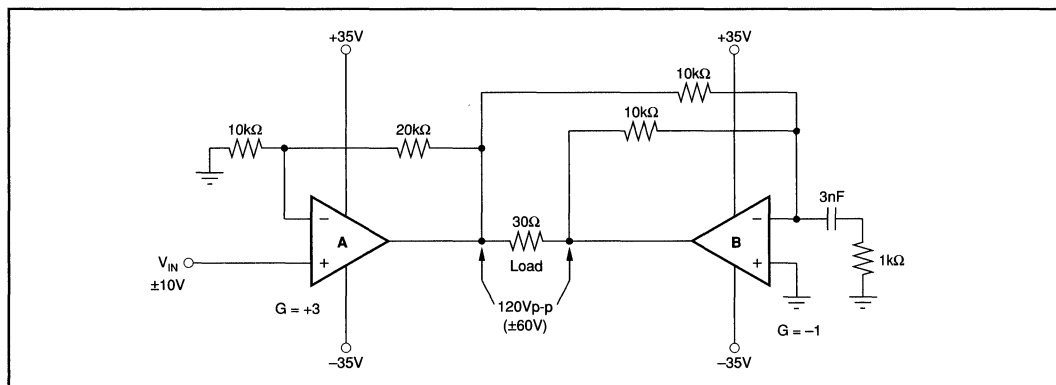
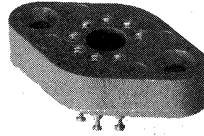


FIGURE 4. Bridge Drive Circuit.

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0804MC

8-Pin TO-3 Socket

FEATURES

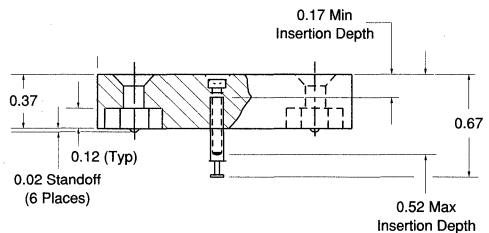
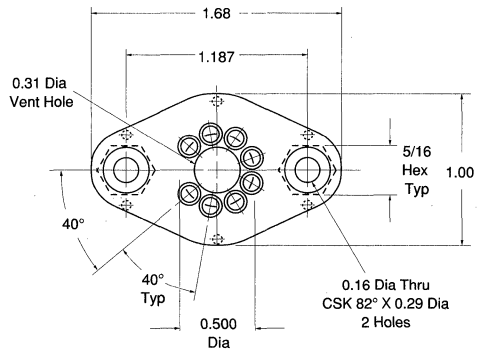
- LOW CONTACT RESISTANCE
- CLOSED CONTACT ENDS
- GOLD-PLATED INNER CONTACTS
- -55°C TO +150°C TEMPERATURE RANGE

DESCRIPTION

The 0804MC is a high quality socket designed for use with Burr-Brown's 8-pin TO-3 type products such as the OPA541 and OPA512.

Although not required for use with these products, the 0804MC socket makes interchanging parts easy, especially during design and testing. Its rugged inner contacts provide positive insertion and low contact resistance. Closed contact ends prevent solder and flux contamination of the internal contacts.

The socket body is molded of glass-filled polyester and incorporates counter-sunk mounting holes and hex-nut retaining feature. It accommodates a variety of mounting hardware and mechanical designs.



Contact Resistance: 0.02Ω Typ

Outer Contact: Brass

200μ inch Tin over 100μ inch Nickel Plate

Inner Contact: BeCu

30μ inch Gold over 50μ inch Nickel Plate

Socket Body: Glass-Filled Polyester, 94 V-0 rating

Operating Temperature Range: -55°C to +150°C

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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3583

High Voltage, High Current OPERATIONAL AMPLIFIER

3583

3.2

FEATURES

- WIDE POWER SUPPLY VOLTAGE:
 $\pm 70V$ to $\pm 150V$
- OUTPUT CURRENT TO 75mA
- SLEW RATE: $30V/\mu s$
- FET INPUT: $I_b = 20pA$ max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

APPLICATIONS

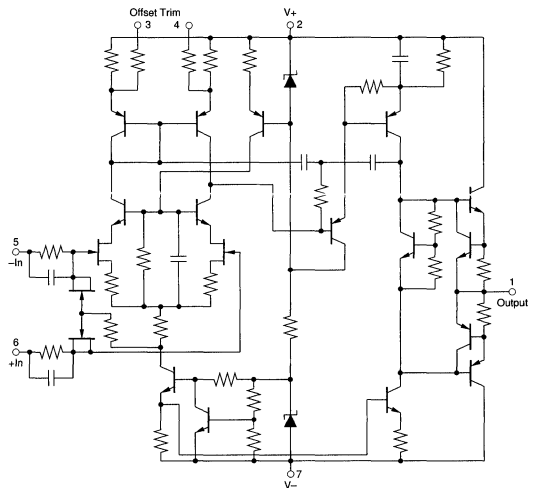
- PROGRAMMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- HIGH VOLTAGE CURRENT SOURCE

DESCRIPTION

The 3583 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3583 operates over a wide power supply range ($\pm 50V$ to $\pm 150V$) and provides outputs up to 75mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

Commercial and industrial temperature range models are available. The 3583's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.



POWER OPERATIONAL AMPLIFIERS

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PDS-343D

3.2.95

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SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

PARAMETER	CONDITIONS	3583AM			3583JM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply vs Time	Specified Temp. Range		20 50	±3 ±23		*	*	mV μV/°C μV/V μV/month
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature vs Power Supply Input Offset Current vs Temperature vs Power Supply	V _{CM} = 0V V _{CM} = 0V		Doubles Every 10°C 0.2 Doubles Every 10°C 0.2	-20 ±20		*	*	pA pA/V pA pA/V
NOISE Voltage, 0.01Hz to 10Hz 10Hz to 1kHz Current, 0.01Hz to 10Hz			5 1.7 0.3			*	*	μVp-p μVrms pAp-p
INPUT VOLTAGE RANGE Max Safe Differential Input Max Safe Common-Mode Input Common-mode Input Range Common-mode Rejection	Linear Operation		(V+) + V- V- to V+ V _S -10 110			*	*	V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹¹ 10 10 ¹¹			*	*	Ω pF Ω pF
OPEN-LOOP GAIN Open-loop Voltage Gain Open-loop Voltage Gain	No Load, DC Rated Load, DC	94	118 105		*	*	*	dB dB
FREQUENCY RESPONSE Unity-Gain Bandwidth Full-Power Bandwidth Slew Rate Settling Time: 0.1%	Small-Signal R _L = 10kΩ		5 60 30 12			*	*	MHz kHz V/μs μs
OUTPUT Voltage Output Current Output Short Circuit Current Load Capacitance		V _S -10 ±75	±100	10	*	*	*	V mA mA nF
POWER SUPPLY Operating Voltage Range Quiescent Current	I _O = 0	±50		±150 ±8.5	*	*	*	V mA
TEMPERATURE RANGE (CASE) Specification Operating Storage θ _{JC} = 4°C/W		-25 -55 -55		+85 +125 +125	0 * *		+70 * *	°C °C °C

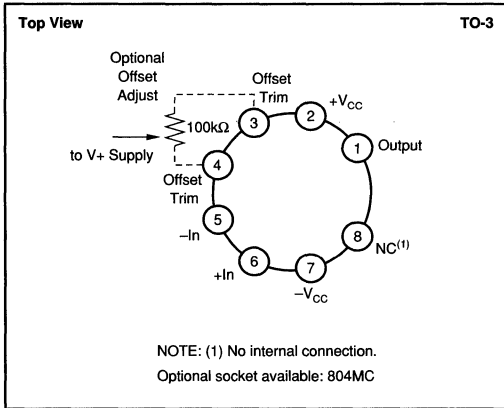
* Specification same as 3583AM.

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/μs. Inputs can be protected from signals exceeding 1000V/μs by limiting input current to 150mA with external series resistors (pins 5 and 6).

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CONNECTION DIAGRAM



PACKAGING INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
3583AM	8-Pin TO-3	030
3583JM	8-Pin TO-3	030

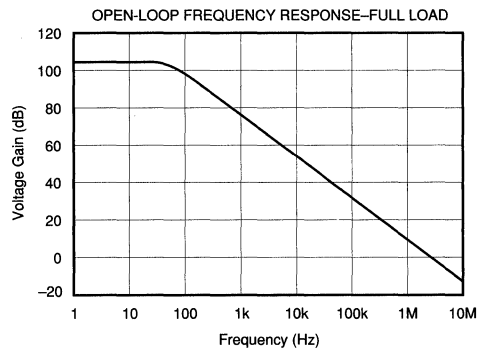
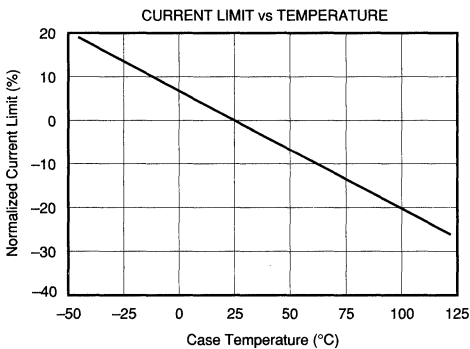
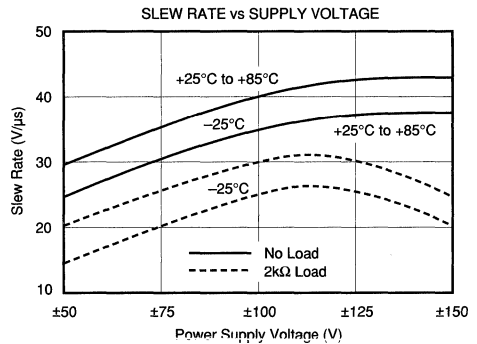
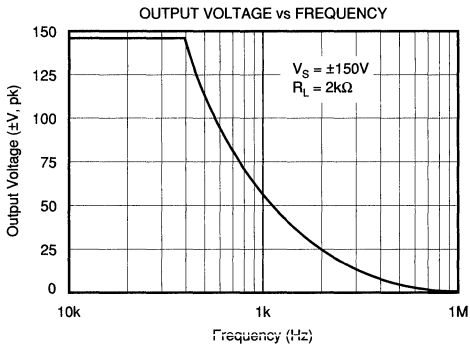
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
3583AM	8-Pin TO-3	-25°C to +85°C
3583JM	8-Pin TO-3	0°C to +70°C

TYPICAL PERFORMANCE CURVES

T_{CASE} = +25°C, ±V_{CC} = 150VDC, unless otherwise noted.



3583

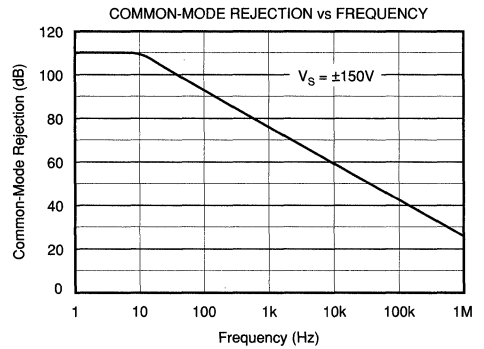
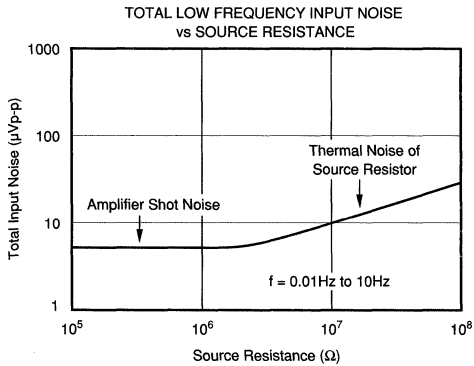
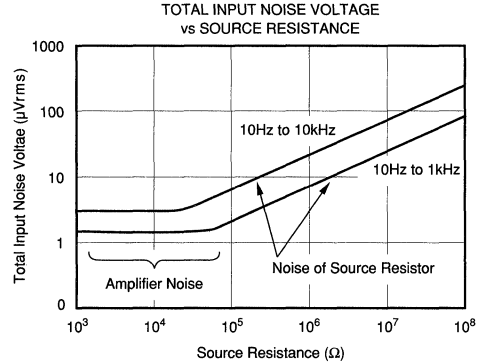
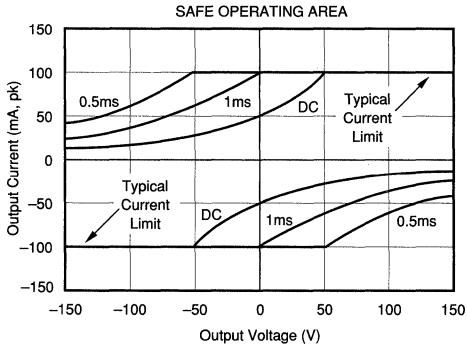
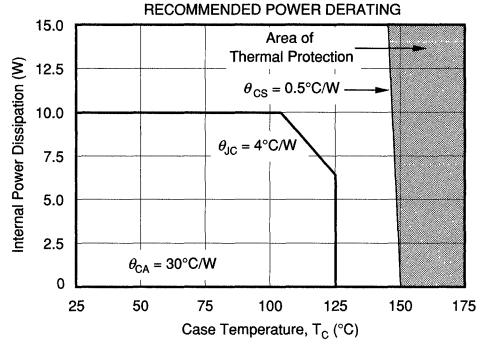
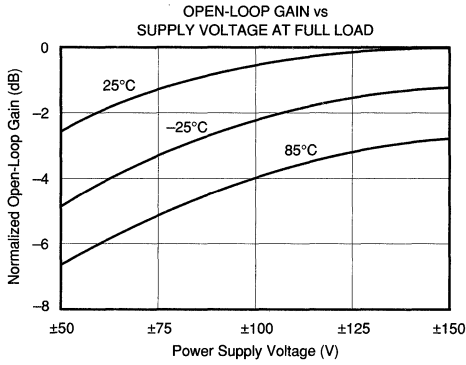
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POWER OPERATIONAL AMPLIFIERS

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TYPICAL PERFORMANCE CURVES (CONT)

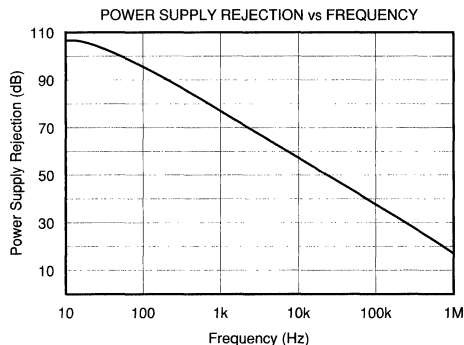
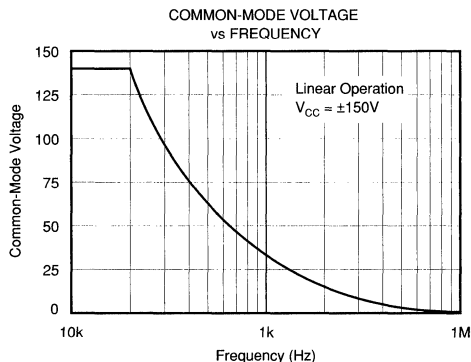
$T_{CASE} = +25^{\circ}C$, $\pm V_{CC} = 150VDC$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $\pm V_{CC} = 150VDC$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required to operate the 3583. Power supply bypass capacitors should be connected close to the device pins. Be sure that these capacitors have an adequate voltage rating.

Input offset voltage and drift of the 3583 are laser-trimmed. Many applications require no external offset trimming. Figure 1 also shows connection of an optional offset trim potentiometer connected to pins 3 and 4.

FET input circuitry reduces the input bias current of the 3583 to less than 20pA at room temperature. Input bias current remains nearly constant throughout the full common-mode range. Input bias current approximately doubles for each 10°C increase in case temperature above 25°C. Heat sinking can help minimize this effect by reducing the case temperature.

Input circuitry of the 3583 is protected with series limiting resistors and input clamp diodes. The inputs can withstand the full rated supply voltage of $\pm 150V$ (common-mode or differential).

THEMAL PROTECTION

The 3583 has internal thermal shut-down circuitry that activates at a case temperature of approximately 150°C or higher. As this circuitry is activated, the output current drive is reduced. As the case temperature returns to less than the activation temperature, operation will return to normal. A heat sink may be required depending on load and signal conditions.

Note that a 75mA output may not be safe for all output voltages—see typical performance curve “Safe Operating Area”. Applications such as current sources where output voltage may be low (or the opposite polarity of the output current) can overstress the output stage.

The thermal shut-down circuit will normally protect the amplifier during a short-circuit to ground. It will not protect against short-circuit to one of the power supplies. The typical performance curve “Safe Operating Area” shows that the large stress occurring during this high voltage condition may cause damage if it exceeds 5ms duration. The thermal protection circuitry will not activate fast enough to protect the device from short-circuits to one of the power supplies.

The package case of the 3583 is electrically isolated from all circuitry. No special insulating hardware is required. Although not absolutely required, it is recommended that the case be connected to ground.

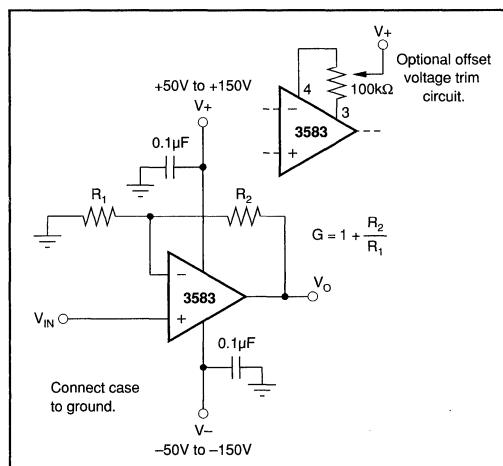


FIGURE 1. Basic Circuit Connections.

3583

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POWER OPERATIONAL AMPLIFIERS

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3584

High Voltage, High Speed OPERATIONAL AMPLIFIER

FEATURES

- WIDE POWER SUPPLY VOLTAGE:
 $\pm 70V$ to $\pm 150V$
- GAIN-BANDWIDTH PRODUCT: 50MHz
- SLEW RATE: $150V/\mu s$
- FET INPUT: $I_b = 20pA$ max
- THERMAL SHUT-DOWN PROTECTION
- HERMETIC TO-3 PACKAGE, ISOLATED CASE

APPLICATIONS

- PROGRAMABLE POWER SUPPLY
- PIEZO-ELECTRIC TRANSDUCER DRIVER
- ELECTROSTATIC TRANSDUCER DRIVER
- CRT DEFLECTION

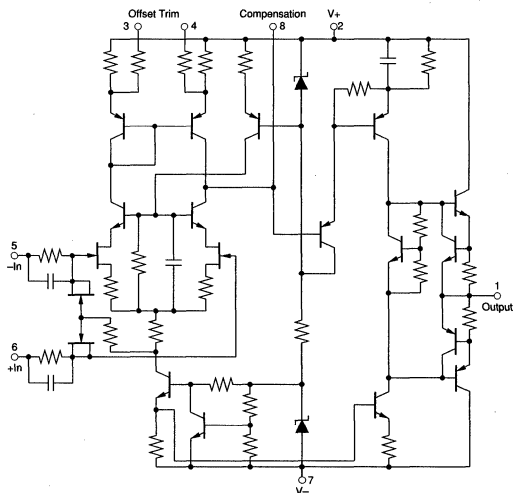
DESCRIPTION

The 3584 is a high voltage, high speed hybrid operational amplifier designed for a wide variety of programmable power supply and transducer driver applications.

The 3584 operates over a wide power supply range ($\pm 70V$ to $\pm 150V$) and provides outputs up to 15mA. Laser-trimmed FET input circuitry provides low offset voltage (3mV max) and low input bias current (20pA max). Thermal shut-down circuitry protects internal circuitry from excessive power dissipation.

The 3584 provides a gain-bandwidth product of 20MHz min (50MHz typical). External frequency compensation (series R/C) allows the user to optimize the bandwidth and slew rate for a particular application.

Specified temperature range is $0^\circ C$ to $+70^\circ C$. The 3584's hermetic 8-pin TO-3 package is electrically isolated from all internal circuitry.



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SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.

PARAMETER	CONDITIONS	3584JM			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply vs Time	Specified Temperature Range		20 50	±3 ±25	mV μV/°C μV/V μV/month
INPUT BIAS CURRENT⁽¹⁾ Input Bias Current vs Temperature vs Power Supply Input Offset Current vs Temperature vs Power Supply	V _{CM} = 0V V _{CM} = 0V		Doubles Every 10°C 0.2 Doubles Every 10°C 0.2	-20 ±20	pA pA/V pA pA/V
NOISE Voltage, 0.01Hz to 10Hz 10Hz to 1kHz Current, 0.01Hz to 10Hz			5 1.7 0.3		μVp-p μVrms pAp-p
INPUT VOLTAGE RANGE Maximum Safe Differential Input Maximum Safe Common-Mode Input Common-Mode Input Range Common-Mode Rejection	Linear Operation		(V+) + V- V- to V+ V _S - 10 110		V dB
INPUT IMPEDANCE Differential Common-Mode			10 ¹¹ 10 10 ¹¹		Ω pF Ω pF
OPEN-LOOP GAIN Open-Loop Voltage Gain Open-Loop Voltage Gain	No Load, DC Rated Load, DC	100	120		dB dB
FREQUENCY RESPONSE Unity-Gain Bandwidth Gain-Bandwidth Product Full-Power Bandwidth Slew Rate Settling Time: 0.1%	Small-Signal f = 1kHz, G = 100 G = 100 G = 100 G = 100	20	7 135 150 12		MHz MHz kHz V/μs μs
OUTPUT Voltage Output Current Output Short Circuit Current Load Capacitance (Maximum)		V _S - 5 ±15	±25 10		V mA mA nF
POWER SUPPLY Operating Voltage Range Quiescent Current	I _O = 0	+70		±150 ±6.5	V mA
TEMPERATURE RANGE Specification Operating Storage		0 -55 -55		+70 +125 +150	°C °C °C

NOTE: (1) Inputs may be damaged by input slew rates exceeding 1000V/μs. Inputs can be protected from signals exceeding 1000V/μs by limiting input current to 150mA with external series resistors (pins 5 and 6).

3584

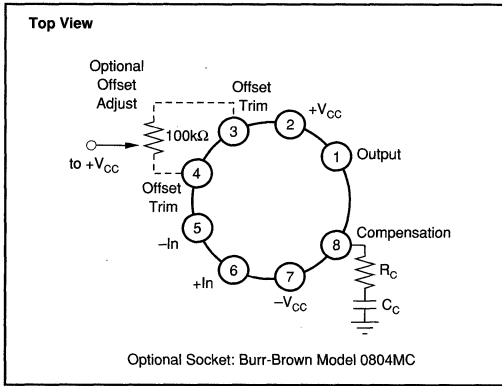
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POWER OPERATIONAL AMPLIFIERS

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CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
3584JM	8-Pin TO-3	0°C to +70°C

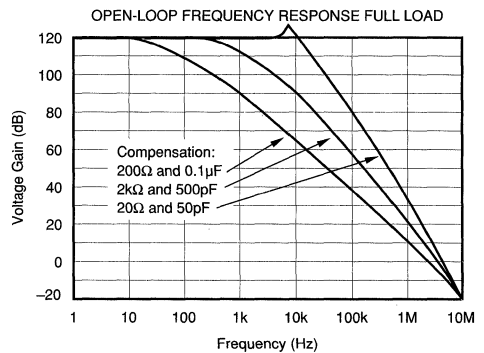
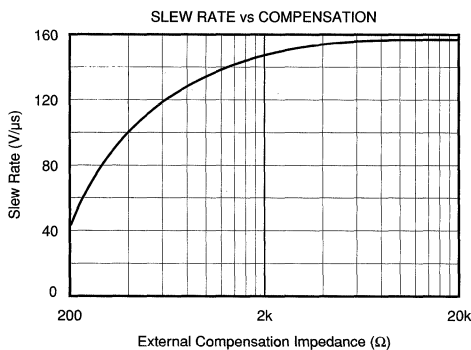
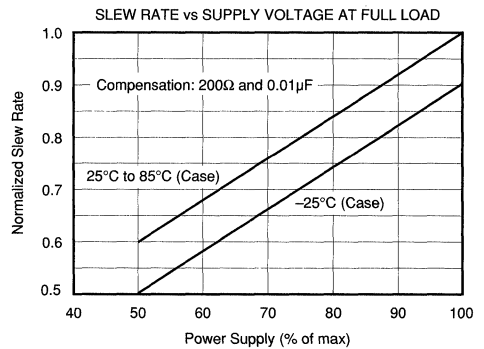
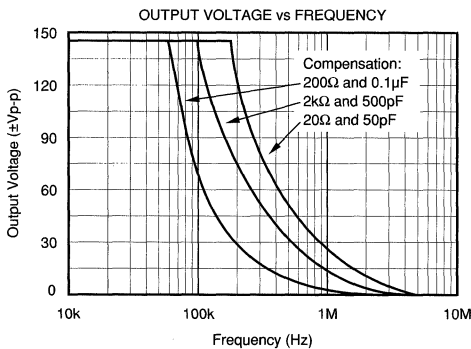
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
3584JM	8-Pin TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

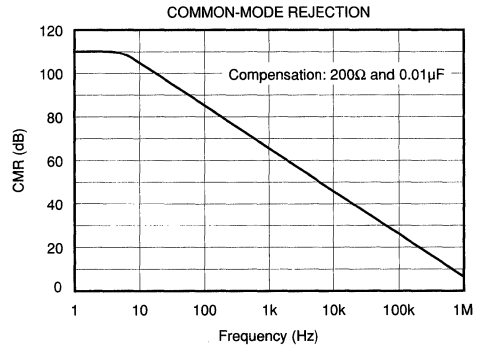
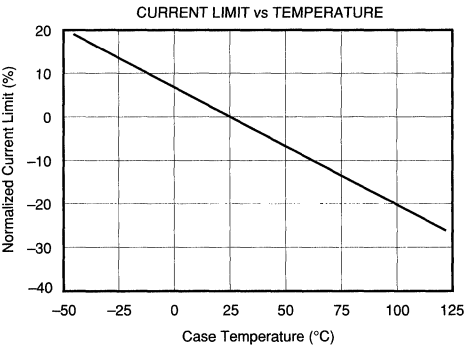
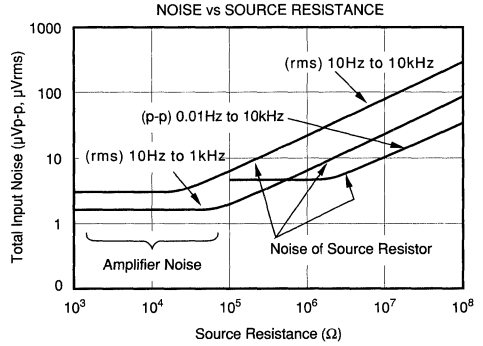
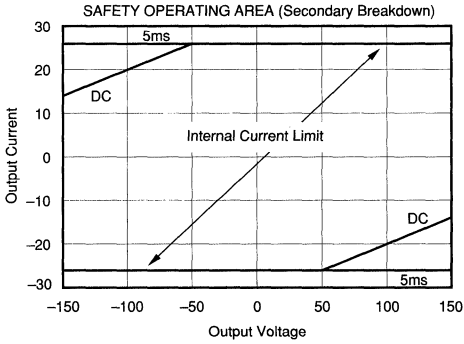
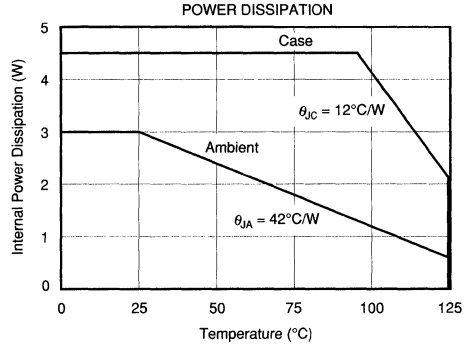
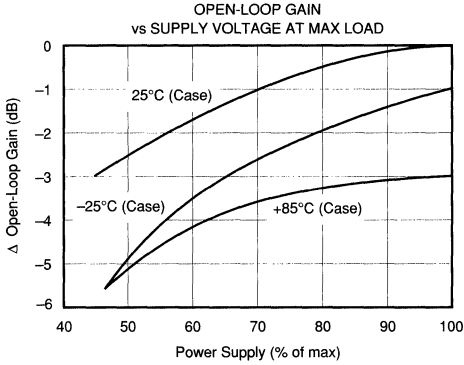
T_{CASE} = +25°C, V_S = ±150V, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}\text{C}$, $V_S = \pm 150\text{V}$, unless otherwise noted.



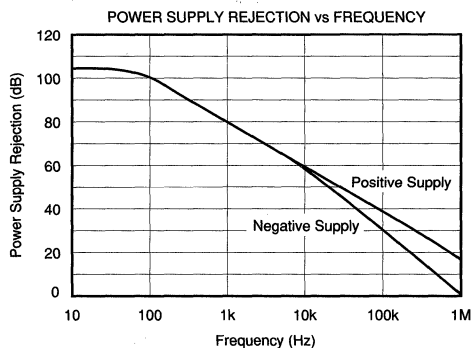
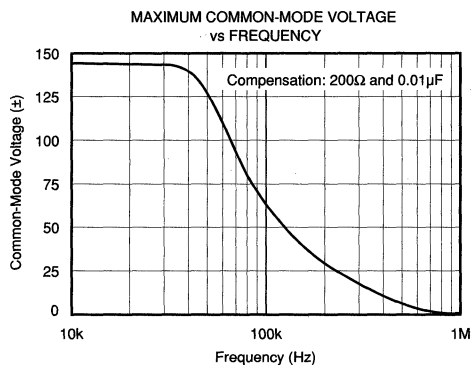
3584

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POWER OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CURVES (CONT)

$T_{CASE} = +25^{\circ}C$, $V_S = \pm 150V$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required to operate the 3584. Bypass capacitors should be connected close to the device pins. Be sure that these capacitors have an adequate voltage rating.

Frequency compensation components must be connected to pin 8 for closed-loop gains of 100 or less. Recommended values are shown in Figure 1. Some adjustment in these values may be required depending on exact circuit configuration and load conditions. Be sure the compensation capacitor has a voltage rating equal to or greater than the positive power supply voltage, V_+ . Standard 0.25W resistors can be used for R_C .

Input offset voltage and drift of the 3584 are laser-trimmed. Many applications require no external offset trimming. Figure 1 shows connection of an optional offset trim potentiometer which connects to pins 3 and 4.

FET input circuitry reduces the input bias current of the 3584 to less than 20pA at room temperature. Input bias current remains nearly constant throughout the full common-mode range. Input bias current approximately doubles for each $10^{\circ}C$ increase in case temperature above $25^{\circ}C$. Heat sinking can help minimize this effect by reducing the case temperature.

Input circuitry of the 3584 is protected with series limiting resistors and input clamp diodes. The inputs can withstand the full rated supply voltage of $\pm 150V$ (common-mode or differential).

THERMAL PROTECTION

The 3584 has internal thermal shut-down circuitry that activates at a case temperature of approximately $150^{\circ}C$ or higher. As this circuitry is activated, the output current drive is reduced. As the case temperature returns to less than the

activation temperature, operation will return to normal.

The thermal shut-down circuit will normally protect the amplifier during a short-circuit to ground. It will not protect against short-circuit to one of the power supplies. The typical performance curve "Safe Operating Area" shows that the large stress occurring during this high voltage condition may cause damage if it exceeds 5ms duration. The thermal protection circuitry will not activate fast enough to protect the device from short-circuits to one of the power supplies.

The package case of the 3584 is electrically isolated from all circuitry. No special insulating hardware is required. Although not absolutely required, it is recommended that the case be connected to ground.

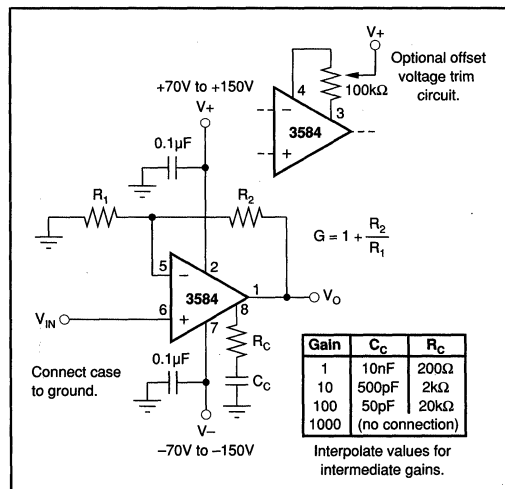


FIGURE 1. Basic Circuit Connections.

4 Instrumentation Amplifiers

Instrumentation amplifiers (IAs) are much more than just precise op amps. They are closed loop amplifiers with built-in precision feedback components. Knowledgeable designers use IAs to extract low-level signals from system errors and noise.

Instrumentation amplifiers can amplify signals in the presence of large common-mode signals. They are ideal for use with all sensor types such as strain gages, load cells, thermocouples, RTDs, current shunts, chemical sensors, and physiological probes. They also make excellent universal input amplifiers for data acquisition systems.

Programmable gain amplifiers are ideal for systems that must connect to a variety of sources with varying signal levels. Models include programmable-gain IAs and op amps.

Choose from the industry's widest selection, including:

INA105, INA106—Simple $G=1$ and $G=10$ difference amplifiers... incredibly versatile circuit elements.

INA114, INA118—The industry's most versatile and accurate 8-pin IAs. INA118 features low-power operation.

INA2128, INA2141—Industry's first dual instrumentation amplifiers.

INA111—High-speed, FET-input IAs using a current-feedback architecture.

INA116—Electrometer IA with ultra-low input bias current.

INA103—Ultra-low $1\text{nV}/\sqrt{\text{Hz}}$ noise makes this IA ideal for microphones, bridges or other low impedance sources.

INA117—A difference amplifier with $\pm 200\text{V}$ common-mode voltage range.

PGA204, PGA206—Programmable gain IAs great for data acquisition systems that connect to a variety of sources or needing exceptional dynamic range.

XTR101, XTR103, XTR104—4 to 20mA current loop transmitters with built-in IAs for RTDs or bridges.

Other popular models provide special features and performance. Use our detailed selection guide to locate the IA for your application.

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INSTRUMENTATION AMPLIFIERS

Boldface = NEW

Description	Model	Gain Range	Gain Error G=100 25°C, max(%)	Gain Drift G=100 (ppm/°C)	Non- Linearity G=100 max(%)	Input Parameters		Dynamic Response G=100 -3dB BW (kHz)	Temp Range ⁽¹⁾	Pkg	Page No.
						CMR ⁽⁵⁾ min(dB)	Offset Voltage vs Temp max(μV/°C)				
Very High Accuracy	INA114	1-10,000 ⁽²⁾	0.5	25	±0.002	96	±0.25+5/G	10	Ind	DIP, SOIC	4.74
	INA115	1-10,000 ⁽²⁾	0.5	25	±0.002	96	±0.25+5/G	10	Ind	SOIC	4.87
	INA131	100	0.024	10	±0.002	110	±0.25	70	Ind	DIP, SOIC	4.135
	INA120	1, 10, 100, 1000	0.5	30	±0.01	96	±0.25±10/G	20	Ind	DIP	4.125
	INA104	1-1000 ⁽²⁾	0.15	22 ⁽³⁾	±0.003	96	±0.25±10/G	25	Ind	DIP	A
	INA101	1-1000 ⁽²⁾	0.1	22 ⁽³⁾	±0.003	96	±0.25±10/G	25	Ind, Mil	DIP TO-100, DIP	4.4
Electrometer Input <i>I_b</i> = 10fA typ	INA116	1-10,000⁽²⁾	0.5	25	±0.005	90	±5±20/G	70	Ind	DIP/SOIC	4.98
Dual	INA2128	1-10,000⁽²⁾	0.5	10	±0.002	97	±0.75±20G	200	XInd	DIP/SOIC	4.145
	INA2141	10,100	0.15	10	±0.002	97	1⁽⁷⁾	200	XInd	DIP/SOIC	4.147
Low Quiescent Power	INA118	1-10,000	0.5	25	±0.002	97	±0.5 + 20/G	100	Ind	DIP, SOIC	4.114
	INA102	1,10,100, 1000	0.15	15	±0.02	90	±2±5/G	3	Com, Ind	DIP, SOIC	4.10
Low Noise, Low Distortion	INA103	1-1000 ⁽²⁾	0.1	25	±0.004	100	±0.5+10/G typ	800	Ind	DIP	4.22
		1-1000 ⁽²⁾	0.25	25	±0.010	90	±0.5+20/G typ	800	Com	DIP, SOIC	
Fast Settling FET Input	INA110	1,10,100, 200,500	0.1	20	±0.01	96	±2±50/G	470	Ind	DIP, SOIC	4.52
	INA111	1-10,000 ⁽²⁾	0.5	25	±0.01	96	±5+100/G	450	Ind	DIP, SOIC	4.63
Unity-Gain Difference Amp	INA105	1V/V, fixed	0.01 ⁽³⁾	5	±0.001 ⁽³⁾	86 ⁽⁴⁾	10	1000 ⁽³⁾	Ind	TO-99, DIP SOIC	4.34
	3627	1V/V, fixed	0.01 ⁽³⁾	5	±0.001 ⁽³⁾	100	20	800 ⁽³⁾	Ind	TO-99	A
Gain of 10 Diff. Amp	INA106	10V/V, fixed	0.025	10	±0.001	100 ⁽⁴⁾	0.20	500	Ind	DIP, SOIC	4.46
High Com. Mode Volt. Diff. Amp (200VDC CMV)	INA117	1V/V, fixed	0.02	10	±0.001	86 ⁽⁴⁾	20	200 ⁽³⁾	Ind	TO-99, DIP SOIC	4.100
4-20mA Loop Receiver	RCV420	4-20mA in 0 - 5V Out	0.05	25	±0.002	86	25 ⁽⁶⁾	150	Com, Ind	DIP	4.190

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, Mil = -55°C to +125°C. (2) Set with external resistor. (3) Unity-gain. (4) No source imbalance. (5) DC to 60Hz, Gain = 10, (or specified gain of device). (6) RTO. (7) G = 100.

"A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

DIGITALLY PROGRAMMABLE GAIN AMPLIFIERS

Boldface = NEW

Description	Model	Digitally Selected Gains	Gain Error G=100 25°C, max(%)	Gain Drift, G=100 (ppm/°C)	Non-Linearity G=100 max(%)	Input Parameters		Dynamic Response G=100 ±3dB BW (kHz)	Temp Range ⁽¹⁾	Pkg	Page No.
						CMR min (dB)	Offset Voltage vs Temp max (µV/°C)				
Noninverting Amplifier	PGA100	1, 2, 4... to 128	0.02	10	±0.005	NA	6 typ	5MHz	Ind	DIP	A
	PGA102	1, 10, 100	0.015	20	±0.01	NA	3,G=100	250	Com, Ind	DIP	4.149
	PGA103	1, 10, 100	0.2	30	±0.01	NA	2 typ	250	XInd	DIP, SOIC	4.157
Instrumentation Amplifier Input	PGA200	1, 10, 100, 1000	0.02	10	±0.003	96	0.4,G=100	30	Ind	DIP	A
Fast Settling 2µs to 0.01%	PGA202	1, 10, 100, 1000	0.15	40	±0.012	86	±3+50/G	1000	Ind, Com	DIP	4.164
	PGA203	1, 2, 4, 8	0.15	40	±0.012	86	±3+50/G	1000	Ind, Com	DIP	4.164
Low Cost	PGA204	1, 10, 100, 1000	0.024	10	±0.002	96	±0.25 + 5/G	10	Ind	DIP, SOL-16	4.174
	PGA205	1, 2, 4, 8	0.024	10	±0.002	96	±0.25 + 5/G	100 ⁽⁴⁾	Ind	DIP, SOL-16	4.174
	PGA206	1, 2, 4, 8	0.024	10	±0.0025	90	±1 ± 10/G⁽²⁾	1.5⁽³⁾	XInd	DIP, SOIC	4.188
	PGA207	1, 2, 5, 10	0.024	10	±0.0025	90	±1 ± 10/G⁽²⁾	1.5⁽³⁾	XInd	DIP, SOIC	4.188
Binary Gain	3606	1, 2, 4, 8 to 1024	0.02	10	±0.004	90,G=1	±1+20/G	40	Ind	DIP	A

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C. XInd = -40°C to +85°C. (2) Typical. (3) G = 10. (4) G = 8. "A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

4

4-20mA CURRENT TRANSMITTERS

Boldface = NEW

Description	Model	Span		Temp Drift (ppm/°C)	Input Parameters			Output Parameters			Temp Range ⁽¹⁾	Pkg	Page No.
		Untrimmed Error, max (%)	Non-linearity, max (%)		Offset Voltage max (µV/°C)	Offset vs Temp max (µV/°C)	DC min (dB)	CMR min (dB)	Current Range (mA)	Offset Current Error max (µA)			
Two-Wire	XTR101	5	0.01	±100	±30µV	±0.75	90	4-20	±6	±30	XInd	DIP, SOIC	4.200
Two-Wire RTD Linearity Compensation	XTR103	1	0.01	±50	±2500µV	±2.5	80	4-20	±25	±50	XInd ⁽²⁾	DIP, SOIC	4.215
Two-Wire Bridge Linearity Compensation	XTR104	1	0.01	±50	±2500µV	±2.5	80	4-20	±25	±50	XInd ⁽²⁾	DIP, SOIC	4.225
Three-Wire and Current	XTR110	0.2	0.005	30	—	—	—	4-20, 0-20, 5-25	±16	±32	XInd	DIP, SOIC	4.236
High-Current Bridge Driver	XTR501	5	0.1	—	2500µV	50	100	4-20	250	—	Ind	MOD	4.245

NOTES: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C. (2) -40°C to +85°C.

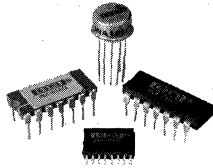
PRECISION CURRENT TRANSMITTERS

Boldface = NEW

Two-Wire	IXR100	See Isolation Products
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INSTRUMENTATION AMPLIFIERS

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INA101

High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW DRIFT: $0.25\mu\text{V}/^\circ\text{C}$ max
- LOW OFFSET VOLTAGE: $25\mu\text{V}$ max
- LOW NONLINEARITY: 0.002%
- LOW NOISE: $13\text{nV}/\sqrt{\text{Hz}}$
- HIGH CMR: 106dB AT 60Hz
- HIGH INPUT IMPEDANCE: $10^{10}\Omega$
- 14-PIN PLASTIC AND CERAMIC DIP
SOL-16, TO-100 PACKAGES

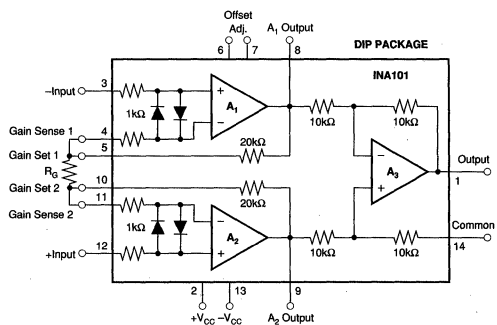
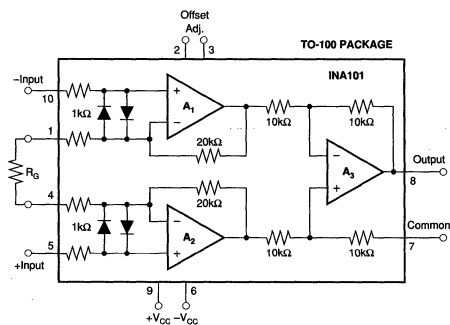
APPLICATIONS

- STRAIN GAGES
- THERMOCOUPLES
- RTDs
- REMOTE TRANSDUCERS
- LOW-LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The INA101 is a high accuracy instrumentation amplifier designed for low-level signal amplification and general purpose data acquisition. Three precision op amps and laser-trimmed metal film resistors are integrated on a single monolithic integrated circuit.

The INA101 is packaged in TO-100 metal, 14-pin plastic and ceramic DIP, and SOL-16 surface-mount packages. Commercial, industrial and military temperature range models are available.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted.

PARAMETER	INA101AM, AG			INA101SM, SG			INA101CM, CG			INA101HP, KU			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN	1		1000	*	*	*	*	*	*	*	*	*	V/V
Range of Gain													V/V
Gain Equation		$G = 1 + (40k/R_G)$		*	*	*	*	*	*	*	*	*	%
Error from Equation, DC ⁽¹⁾		$\pm(0.04 + 0.00016G - 0.02/G)$	$\pm(0.1 + 0.0003G - 0.05/G)$	*	*	*	*	*	*	$\pm(0.1 + 0.00015G - 0.05/G)$	$\pm(0.3 + 0.0002G - 0.10/G)$	*	
Gain Temp. Coefficient⁽²⁾													ppm/°C
G = 1		2	5	*	*	*	*	*	*	*	*	*	ppm/°C
G = 10		20	100	*	*	*	10	*	*	*	*	*	ppm/°C
G = 100		22	110	*	*	*	11	*	*	*	*	*	ppm/°C
G = 1000		22	110	*	*	*	11	*	*	*	*	*	ppm/°C
Nonlinearity, DC ⁽³⁾		$\pm(0.002 + 10^{-6}G)$	$\pm(0.005 + 2 \times 10^{-6}G)$	$\pm(0.001 + 10^{-6}G)$	$\pm(0.002 + 10^{-6}G)$	$\pm(0.001 + 10^{-6}G)$	$\pm(0.001 + 10^{-6}G)$	$\pm(0.002 + 10^{-6}G)$	$\pm(0.002 + 10^{-6}G)$				% of p-p FS
RATED OUTPUT													
Voltage	±10	±12.5		*	*	*	*	*	*	*	*	*	V
Current	±5	±10		*	*	*	*	*	*	*	*	*	mA
Output Impedance		0.2		*	*	*	*	*	*	*	*	*	Ω
Capacitive Load		1000		*	*	*	*	*	*	*	*	*	pF
INPUT OFFSET VOLTAGE													
Initial Offset at +25°C		$\pm(25 + 200/G)$	$\pm(50 + 400/G)$	$\pm 10 + 100/G$	$\pm(25 + 200/G) \pm(0.75 + 10/G)$		$\pm(10 + 100/G)$	$\pm(25 + 200/G) \pm(0.25 + 10/G)$		$\pm(125 + 450/G) \pm(2 + 20/G)$	$\pm(250 + 900/G)$		μV
vs Temperature			$\pm(2 + 20/G)$										μV/°C
vs Supply		$\pm(1 + 20/G)$		*	*	*	*	*	*	*	*	*	μV/V
vs Time		$\pm(1 + 20/G)$		*	*	*	*	*	*	*	*	*	μV/mo
INPUT BIAS CURRENT													
Initial Bias Current (each input)		±15	±30	±10	*	*	±5	±20	*	*	*	*	nA
vs Temperature		±0.2		*	*	*	*	*	*	*	*	*	nA/°C
vs Supply		±0.1		*	*	*	*	*	*	*	*	*	nA/V
Initial Offset Current		±15	±30	±10	*	*	±5	±20	*	*	*	*	nA
vs Temperature		±0.5		*	*	*	*	*	*	*	*	*	nA/°C
INPUT IMPEDANCE													
Differential		$10^9 \parallel 3$		*	*	*	*	*	*	*	*	*	Ω pF
Common-mode		$10^9 \parallel 3$		*	*	*	*	*	*	*	*	*	Ω pF
INPUT VOLTAGE RANGE													
Range, Linear Response	±10	±12		*	*	*	*	*	*	*	*	*	V
CMR with 1kΩ Source Imbalance				*	*	*	*	*	*	*	*	*	
DC to 60Hz, G = 1	80	90		*	*	*	*	*	65	85			dB
DC to 60Hz, G = 10	96	106		*	*	*	*	*	90	95			dB
DC to 60Hz, G = 100 to 1000	106	110		*	*	*	*	*	100	105			dB
INPUT NOISE													
Input Voltage Noise				*	*	*	*	*	*	*	*	*	μV, p-p
$f_b = 0.01\text{Hz to } 10\text{Hz}$		0.8		*	*	*	*	*	*	*	*	*	
Density, G = 1000				*	*	*	*	*	*	*	*	*	nV/√Hz
$f_b = 10\text{Hz}$		18		*	*	*	*	*	*	*	*	*	nV/√Hz
$f_b = 100\text{Hz}$		15		*	*	*	*	*	*	*	*	*	nV/√Hz
$f_b = 1\text{kHz}$		13		*	*	*	*	*	*	*	*	*	nV/√Hz
Input Current Noise				*	*	*	*	*	*	*	*	*	pA, p-p
$f_b = 0.01\text{Hz to } 10\text{Hz}$		50		*	*	*	*	*	*	*	*	*	
Density				*	*	*	*	*	*	*	*	*	pA/√Hz
$f_b = 10\text{Hz}$		0.8		*	*	*	*	*	*	*	*	*	pA/√Hz
$f_b = 100\text{Hz}$		0.46		*	*	*	*	*	*	*	*	*	pA/√Hz
$f_b = 1\text{kHz}$		0.35		*	*	*	*	*	*	*	*	*	pA/√Hz
DYNAMIC RESPONSE													
Small Signal, ±3dB Flatness				*	*	*	*	*	*	*	*	*	kHz
G = 1		300		*	*	*	*	*	*	*	*	*	kHz
G = 10		140		*	*	*	*	*	*	*	*	*	kHz
G = 100		25		*	*	*	*	*	*	*	*	*	kHz
G = 1000		2.5		*	*	*	*	*	*	*	*	*	kHz
Small Signal, ±1% Flatness				*	*	*	*	*	*	*	*	*	kHz
G = 1		20		*	*	*	*	*	*	*	*	*	kHz
G = 10		10		*	*	*	*	*	*	*	*	*	kHz
G = 100		1		*	*	*	*	*	*	*	*	*	Hz
G = 1000		200		*	*	*	*	*	*	*	*	*	Hz
Full Power, G = 1 to 100		6.4		*	*	*	*	*	*	*	*	*	Hz
Slew Rate, G = 1 to 100	0.2	0.4		*	*	*	*	*	*	*	*	*	V/μs
Settling Time (0.1%)				*	*	*	*	*	*	*	*	*	μs
G = 1		30	40	*	*	*	*	*	*	*	*	*	μs
G = 100		40	55	*	*	*	*	*	*	*	*	*	μs
G = 1000		350	470	*	*	*	*	*	*	*	*	*	μs
Settling Time (0.01%)				*	*	*	*	*	*	*	*	*	μs
G = 1		30	45	*	*	*	*	*	*	*	*	*	μs
G = 100		50	70	*	*	*	*	*	*	*	*	*	μs
G = 1000		500	650	*	*	*	*	*	*	*	*	*	μs
POWER SUPPLY													
Rated Voltage		±15		*	*	*	*	*	*	*	*	*	V
Voltage Range	±5		±20	*	*	*	*	*	*	*	*	*	V
Current, Quiescent ⁽⁴⁾		±6.7	±8.5	*	*	*	*	*	*	*	*	*	mA
TEMPERATURE RANGE⁽⁵⁾													
Specification	-25		+85	-55		+125	*	*	0		+70		°C
Operation	-55			*	*	*	*	*	-25		+85		°C
Storage	-65		+150	*	*	*	*	*	-40		+85		°C

* Specifications same as for INA101AM, AG.

NOTES: (1) Typically the tolerance of R_G will be the major source of gain error. (2) Nonlinearity is the maximum peak deviation from the best straight-line as a percentage of peak-to-peak full scale output. (3) Not including the TCR of R_G . (4) Adjustable to zero at any one gain. (5) q_{ic} output stage = 113°C/W, q_{ic} quiescent circuitry = 19°C/W, q_{ic} = 83°C/W.

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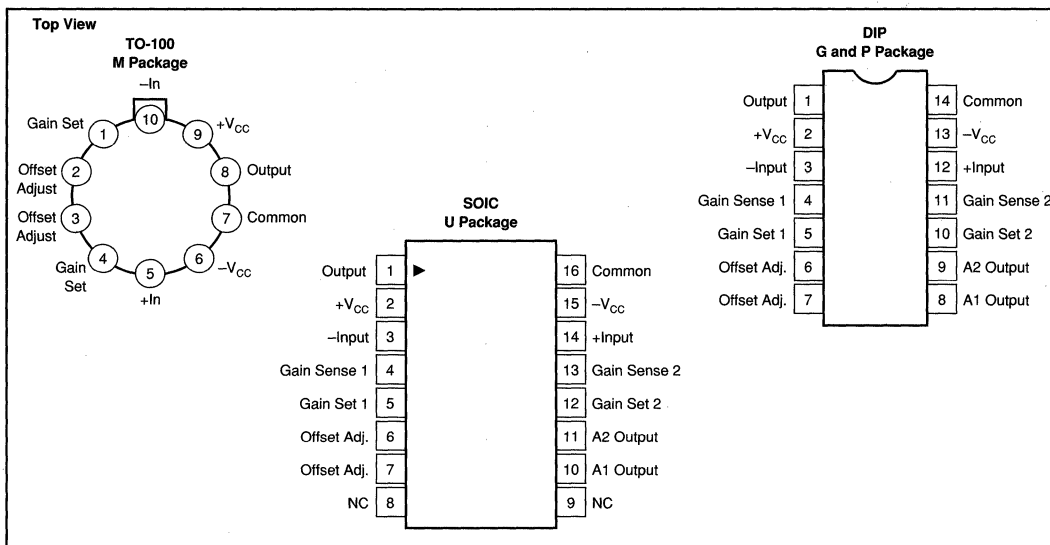
Burr-Brown IC Data Book—Linear Products

INA101

4

INSTRUMENTATION AMPLIFIERS

PIN CONFIGURATIONS



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA101AM	10-Pin Metal TO-100	-25°C to +85°C
INA101CM	10-Pin Metal TO-100	-25°C to +85°C
INA101AG	14-Pin Ceramic DIP	-25°C to +85°C
INA101CG	14-Pin Ceramic DIP	-25°C to +85°C
INA101HP	14-Pin Plastic DIP	0°C to +70°C
INA101KU	SOL-16 Surface-Mount	0°C to +70°C
INA101SG	14-Pin Ceramic DIP	-55°C to +125°C
INA101SM	10-Pin Metal TO-100	-55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Power Dissipation	600mW
Input Voltage Range	±V _{CC}
Output Short-Circuit (to ground)	Continuous
Operating Temperature M, G Package	-55°C to +125°C
P, U Package	-25°C to +85°C
Storage Temperature M, G Package	-65°C to +150°C
P, U Package	-40°C to +85°C
Lead Temperature (soldering, 10s) M, G, P Package	+300°C
Lead Temperature (wave soldering, 3s) U Package	+260°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA101AM	10-Pin Metal TO-100	007
INA101CM	10-Pin Metal TO-100	007
INA101AG	14-Pin Ceramic DIP	169
INA101CG	14-Pin Ceramic DIP	169
INA101HP	14-Pin Plastic DIP	010
INA101KU	SOL-16 Surface-Mount	211
INA101SG	14-Pin Ceramic DIP	169
INA101SM	10-Pin Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

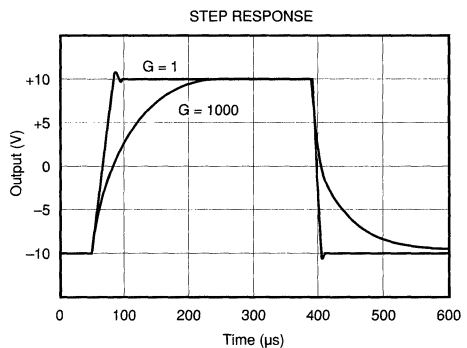
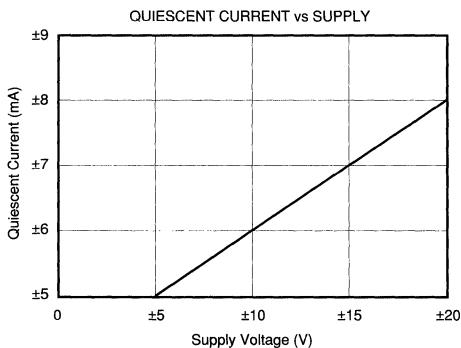
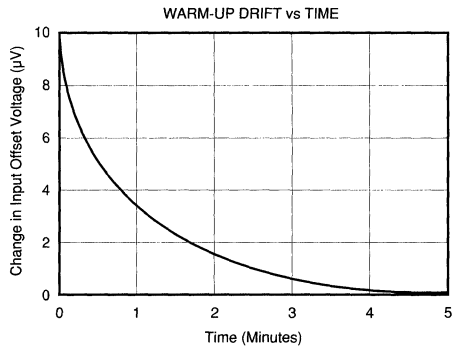
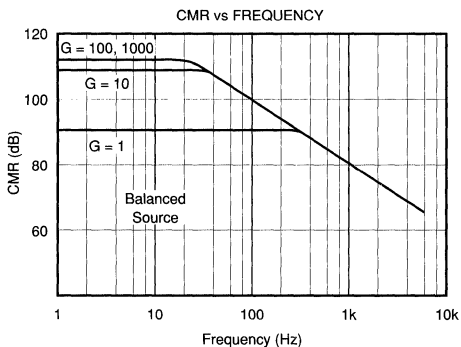
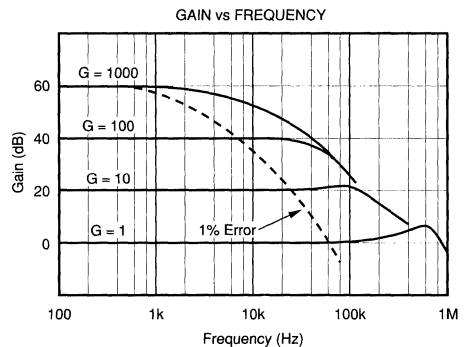
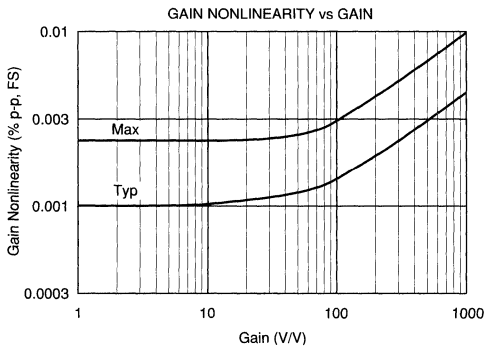
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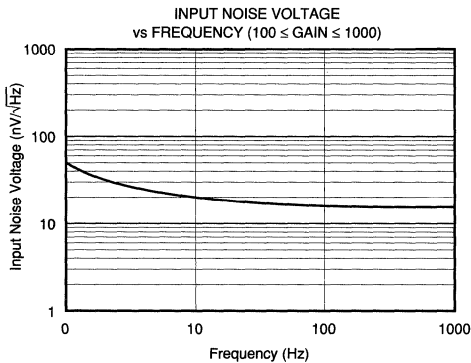
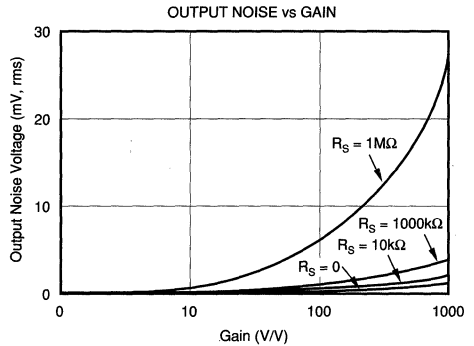
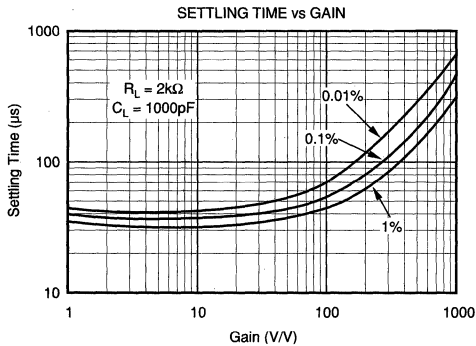
TYPICAL PERFORMANCE CURVES

At +25°C, $V_{CC} = \pm 15V$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At +25°C, $V_{CC} = \pm 15V$ unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA101. (Pin numbers shown are for the TO-100 metal package.) Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output Common terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance greater than 0.1Ω in series with the Common pin will cause common-mode rejection to fall below 106dB.

SETTING THE GAIN

Gain of the INA101 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{40k\Omega}{R_G} \quad (1)$$

The $40k\Omega$ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA101.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. The gain sense connections on the DIP and SOL-16 packages (see Figure 2) reduce the gain error produced by wiring or socket resistance.

OFFSET TRIMMING

The INA101 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows connection of an optional potentiometer connected to the Offset Adjust pins for trimming the input offset voltage. (Pin numbers shown are for the DIP package.) Use this adjustment to null the offset voltage in high gain ($G \geq 100$) with both inputs connected to ground. Do not use this adjustment to null offset produced by the source or other system offset since this will increase the offset voltage drift by $0.3\mu\text{V}/^\circ\text{C}$ per $100\mu\text{V}$ of adjusted offset.

Offset of the output amplifier usually dominates when the INA101 is used in unity gain ($G = 1$). The output offset

voltage can be adjusted with the optional trim circuit connected to the Common pin as shown in Figure 2. The voltage applied to Common terminal is summed with the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp connected as a buffer provides low impedance.

THERMAL EFFECTS ON OFFSET VOLTAGE

To achieve lowest offset voltage and drift, prevent air currents from circulating near the INA101. Rapid changes in temperature will produce a thermocouple effect on the package leads that will degrade offset voltage and drift. A shield or cover that prevents air currents from flowing near the INA101 will assure best performance.

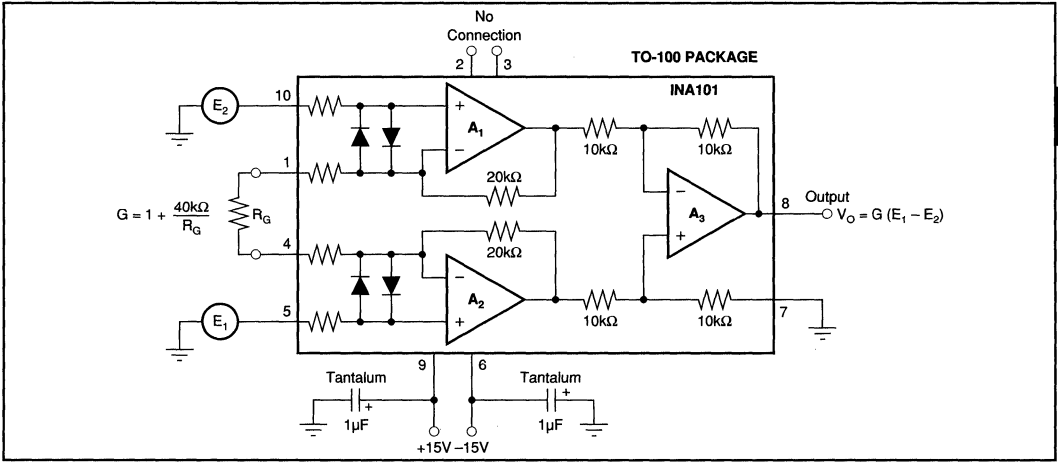


FIGURE 1. Basic Connections.

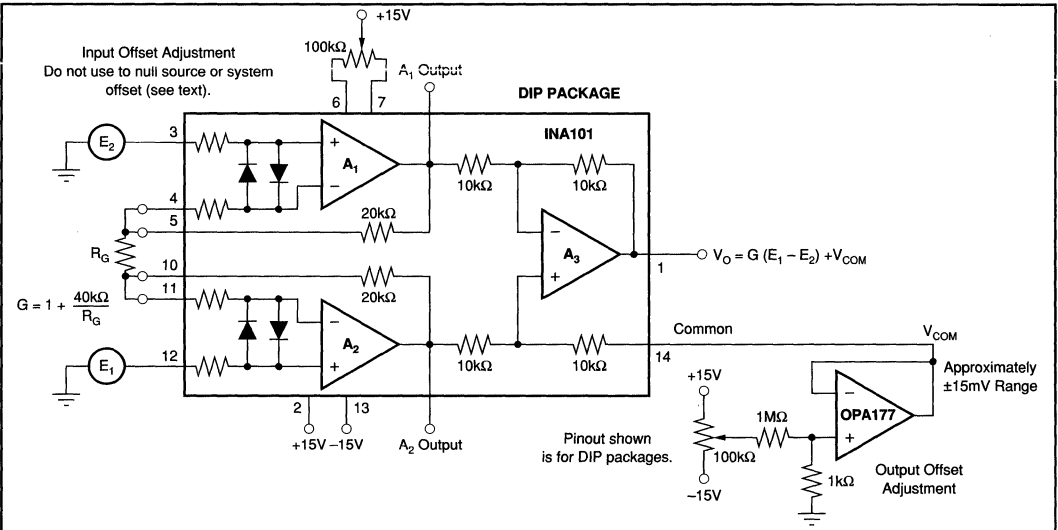
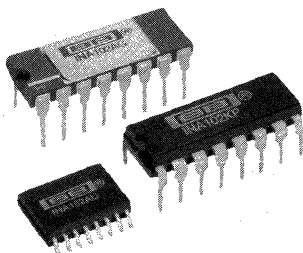


FIGURE 2. Optional Trimming of Input and Output Offset Voltage.

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INA102

Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 750 μ A max
- INTERNAL GAINS: 1, 10, 100, 1000
- LOW GAIN DRIFT: 5ppm/ $^{\circ}$ C max
- HIGH CMR: 90dB min
- LOW OFFSET VOLTAGE DRIFT: 2 μ V/ $^{\circ}$ C max
- LOW OFFSET VOLTAGE: 100 μ V max
- LOW NONLINEARITY: 0.01% max
- HIGH INPUT IMPEDANCE: 10¹⁰ Ω

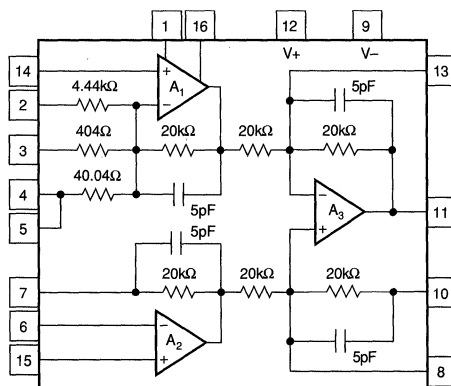
APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
Strain Gages (Weigh Scale Applications)
Thermocouples
Bridge Transducers
- REMOTE TRANSDUCER AMPLIFIER
- LOW-LEVEL SIGNAL AMPLIFIER
- MEDICAL INSTRUMENTATION
- MULTICHANNEL SYSTEMS
- BATTERY POWERED EQUIPMENT

DESCRIPTION

The INA102 is a high-accuracy monolithic instrumentation amplifier designed for signal conditioning applications where low quiescent power is desired. On-chip thin-film resistors provide excellent temperature and stability performance. State-of-the-art laser-trimming technology insures high gain accuracy and common-mode rejection while avoiding expensive external components. These features make the INA102 ideally suited for battery-powered and high-volume applications.

The INA102 is also convenient to use. A gain of 1, 10, 100, or 1000 may be selected by simply strapping the appropriate pins together. A gain drift of 5ppm/ $^{\circ}$ C in low gains can then be achieved without external adjustment. When higher-than-specified CMR is required, CMR can be trimmed using the pins provided. In addition, balanced filtering can be accomplished in the output stage.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ with $\pm 15\text{VDC}$ power supply and in circuit of Figure 2 unless otherwise noted.

PARAMETER	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
GAIN												
Range of Gain		1		1000	*		*	*		*	V/V	
Gain Equation, External, $\pm 20\%$		$G = 1 + (40k/R_G)^{(1)}$				*			*		V/V	
Error, DC: $G = 1$	$T_A = +25^\circ\text{C}$			0.1			0.05			0.15	%	
$G = 10$	$T_A = +25^\circ\text{C}$			0.1			0.05			0.35	%	
$G = 100$	$T_A = +25^\circ\text{C}$			0.25			0.15			0.4	%	
$G = 1000$	$T_A = +25^\circ\text{C}$			0.75			0.5			0.9	%	
$G = 1$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.16			0.08			0.21	%	
$G = 10$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.19			0.11			0.44	%	
$G = 100$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.37			0.21			0.52	%	
$G = 1000$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.93			0.62			1.08	%	
Gain Temp. Coefficient												
$G = 1$				10			5			*	ppm/ $^\circ\text{C}$	
$G = 10$				15			10			*	ppm/ $^\circ\text{C}$	
$G = 100$				20			15			*	ppm/ $^\circ\text{C}$	
$G = 1000$				30			20			*	ppm/ $^\circ\text{C}$	
Nonlinearity, DC												
$G = 1$	$T_A = +25^\circ\text{C}$			0.03			0.01			*	% of FS	
$G = 10$	$T_A = +25^\circ\text{C}$			0.03			0.01			*	% of FS	
$G = 100$	$T_A = +25^\circ\text{C}$			0.05			0.02			*	% of FS	
$G = 1000$	$T_A = +25^\circ\text{C}$			0.1			0.05			*	% of FS	
$G = 1$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.045			0.015			*	% of FS	
$G = 10$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.045			0.015			*	% of FS	
$G = 100$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.075			0.03			*	% of FS	
$G = 1000$	$T_A = T_{\text{MIN}}$ to T_{MAX}			0.15			0.1			*	% of FS	
RATED OUTPUT												
Voltage	$R_L = 10\text{k}\Omega$	$\pm(V_{\text{CC}} - 2.5)$			*		*	*		*	V	
Current				± 1						*	mA	
Short-Circuit Current ⁽²⁾				2			*			*	mA	
Output Impedance, $G = 1000$				0.1			*			*	Ω	
INPUT												
OFFSET VOLTAGE												
Initial Offset ⁽³⁾	$T_A = +25^\circ\text{C}$			$\pm 300 \pm 300/G$			$\pm 100 \pm 200/G$			$\pm 500 \pm 300/G$		μV
vs Temperature				$\pm 5 \pm 10/G$			$\pm 2 \pm 5/G$			$\pm 10 \pm 20/G$		$\mu\text{V}/^\circ\text{C}$
vs Supply				$\pm 40 \pm 50/G$			$\pm 10 \pm 20/G$					$\mu\text{V}/\text{V}$
vs Time				$\pm(20 + 30/G)$			*		*			$\mu\text{V}/\text{mo}$
BIAS CURRENT												
Initial Bias Current (Each Input)	$T_A = T_{\text{MIN}}$ to T_{MAX}			25	50		5	30		*	nA	
vs Temperature				± 0.1			*			*	nA/ $^\circ\text{C}$	
vs Supply				± 0.1			*			*	nA/V	
Initial Offset Current	$T_A = T_{\text{MIN}}$ to T_{MAX}			± 2.5	± 15		± 2.5	± 10		*	nA	
vs Temperature				± 0.1			*			*	nA/ $^\circ\text{C}$	
IMPEDANCE												
Differential				$10^{10} \parallel 2$			*			*	$\Omega \parallel \text{pF}$	
Common-Mode				$10^{10} \parallel 2$			*			*	$\Omega \parallel \text{pF}$	
VOLTAGE RANGE												
Range, Linear Response	$T_A = T_{\text{MIN}}$ to T_{MAX}	$\pm(V_{\text{CC}} - 4.5)$			*		*	*		*	V	
CMR With 1k Ω Source Imbalance												
$G = 1$	DC to 60Hz	80	94			90	*	75	*	*	dB	
$G = 10$	DC to 60Hz	80	100			90	*	*	*	*	dB	
$G = 10$ to 1000	DC to 60Hz	80	100			90	*	*	*	*	dB	
NOISE												
Input Voltage Noise												
$f_b = 0.01\text{Hz}$ to 10Hz				1			*		*	*	$\mu\text{Vp-p}$	
Density, $G = 1000$: $f_o = 10\text{Hz}$				30			*		*	*	nV/ $\sqrt{\text{Hz}}$	
$f_o = 100\text{Hz}$				25			*		*	*	nV/ $\sqrt{\text{Hz}}$	
$f_o = 1\text{kHz}$				25			*		*	*	nV/ $\sqrt{\text{Hz}}$	
Input Current Noise												
$f_b = 0.01\text{Hz}$ to 10Hz				25			*		*	*	pAp-p	
Density: $f_o = 10\text{Hz}$				0.3			*		*	*	pA/ $\sqrt{\text{Hz}}$	
$f_o = 100\text{Hz}$				0.2			*		*	*	pA/ $\sqrt{\text{Hz}}$	
$f_o = 1\text{kHz}$				0.15			*		*	*	pA/ $\sqrt{\text{Hz}}$	

INA102

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INSTRUMENTATION AMPLIFIERS

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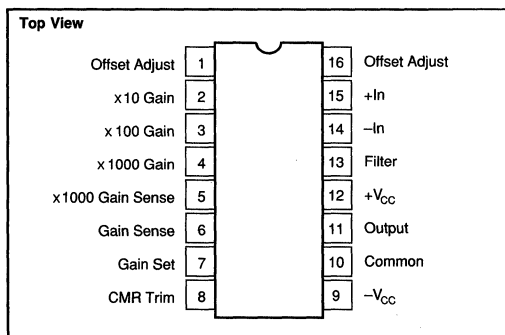
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA102AG			INA102CG			INA102KP/INA102AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE											
Small Signal ±3dB Flatness G = 1 G = 10 G = 100 G = 1000	$V_{OUT} = 0.1V_{rms}$										
			300			*			*		kHz
			30				*			*	kHz
			3				*			*	kHz
Small Signal, ±1% Flatness G = 1 G = 10 G = 100 G = 1000	$V_{OUT} = 0.1V_{rms}$		30			*			*		kHz
			3				*			*	kHz
			0.3				*			*	kHz
			0.03				*			*	kHz
Full Power, G = 1 to 100 Slew Rate, G = 1 to 100	$V_{OUT} = 10V, R_L = 10k\Omega$ $V_{OUT} = 10V, R_L = 10k\Omega$	1.7	2.5		*	*		*	*	kHz	
		0.1	0.15		*	*		*	*	V/ μ s	
Settling Time 0.1%: G = 1 G = 100 G = 1000	$R_L = 10k\Omega, C_L = 100pF$ 10V Step		50			*			*	μ s	
			360			*			*	μ s	
0.01%: G = 1 G = 100 G = 1000	10V Step		3300			*			*	μ s	
			60			*			*	μ s	
			500			*			*	μ s	
			4500			*			*	μ s	
POWER SUPPLY											
Rated Voltage Voltage Range Quiescent Current	$V_O = 0V$ $T_A = T_{MIN} \text{ to } T_{MAX}$	±3.5	±15	±18	*	*	*	*	*	*	V V μ A
			±500	±750							
TEMPERATURE RANGE											
Specification INA102AU Operation Storage	$R_L > 50k\Omega^{(2)}$	-25		+85	*		*	0		+70	°C
								-25		+85	°C
									-25		+85
		-65		+150	*		*	-55		+125	°C

*Specification same as for INA102AG.

NOTES: (1) The internal gain set resistors have an absolute tolerance of ±20%; however, their tracking is 50ppm/°C. R_o will add to the gain error if gains other than 1, 10, 100 or 1000 are set externally. (2) At high temperature, output drive current is limited. An external buffer can be used if required. (3) Adjustable to zero.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Voltage Range	± V_{CC}
Operating Temperature Range	-25°C to +85°C
Storage Temperature Range: Ceramic	-65°C to +150°C
Plastic, SOIC	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration	Continuous to Ground

PACKAGE INFORMATION⁽¹⁾

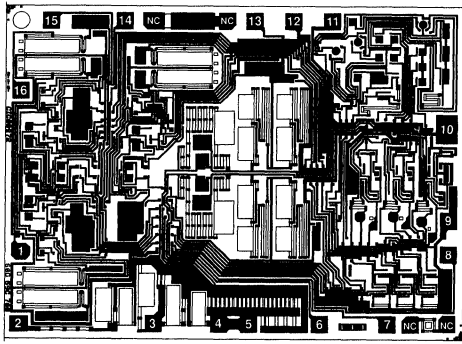
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA102AG	16-Pin Ceramic DIP	109
INA102CG	16-Pin Ceramic DIP	109
INA102KP	16-Pin Plastic DIP	180.
INA102AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA102AG	16-Pin Ceramic DIP	-25°C to +85°C
INA102CG	16-Pin Ceramic DIP	-25°C to +85°C
INA102KP	16-Pin Plastic DIP	0°C to +70°C
INA102AU	16-Pin Plastic SOIC	-25°C to +85°C

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INA102 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Adjust	10*	Common
2	X10 Gain	11	Output
3	X100 Gain	12	+V _{CC}
4	X1000 Gain	13	Filter
5	X1000 Gain Sense	14	-In
6	Gain Sense	15	+In
7	Gain Set	16	Offset Adjust
8	CMR Trim	17	(A ₁ Output)
9	-V _{CC}	18	(A ₂ Output)

* Glass covers upper one-third of this pad.

Substrate Bias: Electrically connected to -V supply.

NC: No Connection.

MECHANICAL INFORMATION

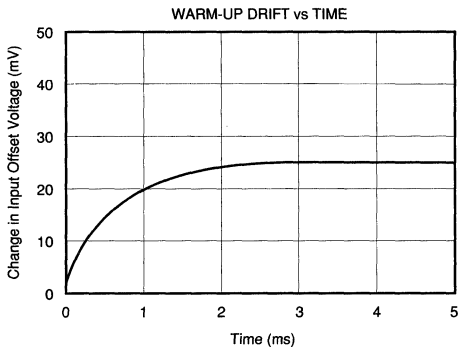
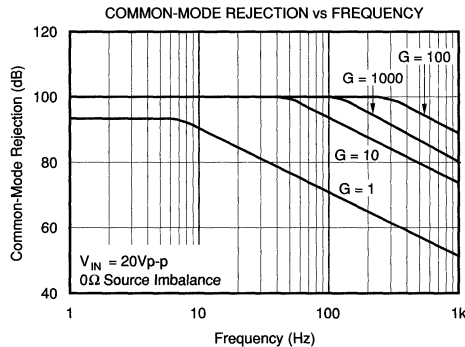
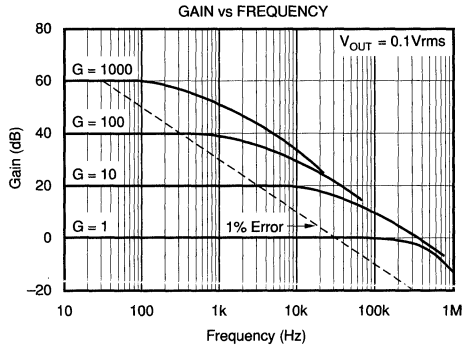
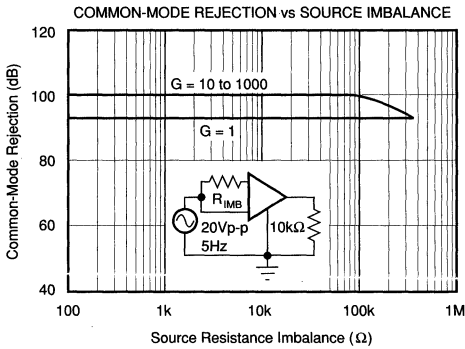
	MILS (0.001")	MILLIMETERS
Die Size	142 x 104 ±5	3.61 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

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TYPICAL PERFORMANCE CURVES

At +25°C and in circuit of Figure 2 unless otherwise noted.



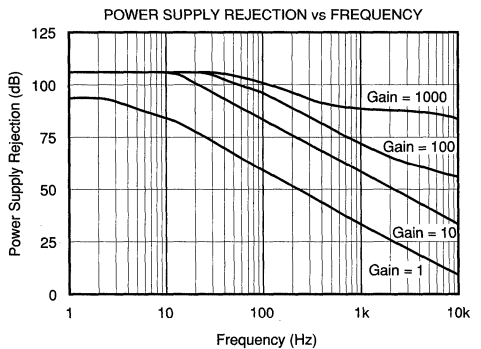
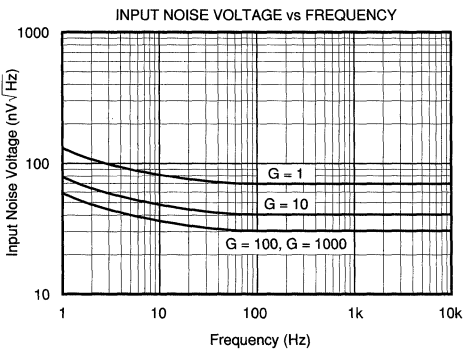
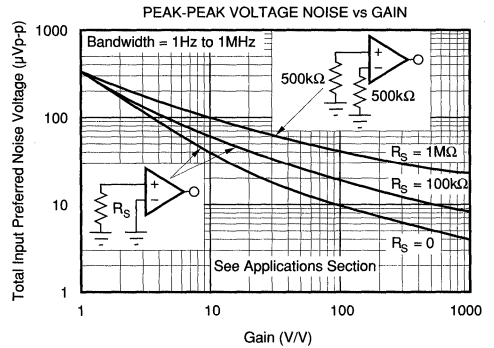
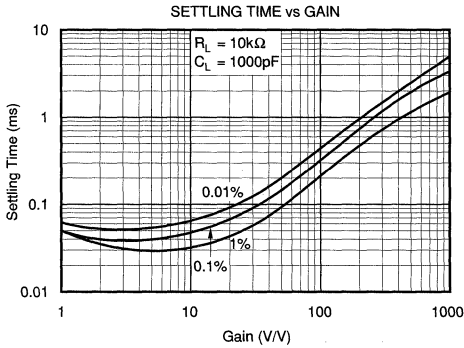
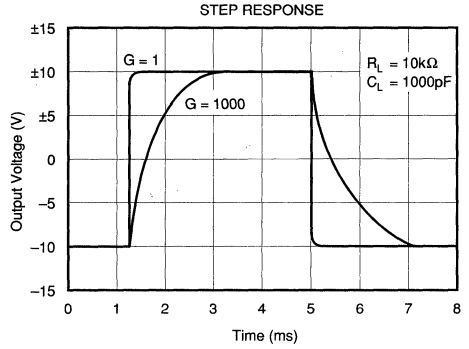
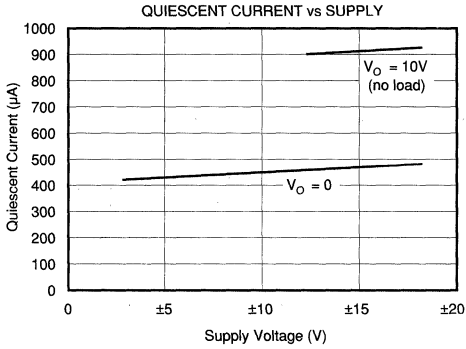
INSTRUMENTATION AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

At +25°C and in circuit of Figure 2 unless otherwise noted.



DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential-input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond mainly to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. The feedback networks of this instrumentation amplifier are included on the monolithic chip. No external resistors are required for gains of 1, 10, 100, and 1000 in the INA102.

An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design tradeoffs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high-input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems associated with op amps.

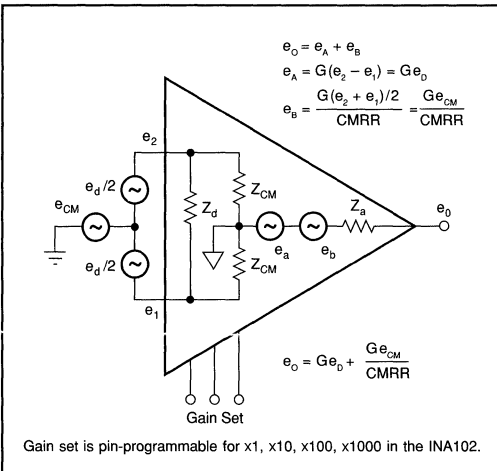


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA102

A simplified schematic of the INA102 is shown on the first page. A three-amplifier configuration is used to provide the desirable characteristics of a premium performance instrumentation amplifier. In addition, INA102 has features not normally found in integrated circuit instrumentation amplifiers.

The input buffers (A_1 and A_2) incorporate high performance, low-drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input

impedance ($10^{10}\Omega$) desirable in instrumentation amplifier applications. The offset voltage, and offset voltage versus temperature, are low due to the monolithic design, and improved even further by state-of-the-art laser-trimming techniques.

The output stage (A_3) is connected in a unity-gain differential amplifier configuration. A critical part of this stage is the matching of the four 20k Ω resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain good common-mode rejection.

All of the internal resistors are made of thin-film nichrome on the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability and provides excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA102 is operated over wide temperature ranges.

USING THE INA102

Figure 2 shows the simplest configuration of the INA102. The output voltage is a function of the differential input voltage times the gain.

A gain of 1, 10, 100, or 1000 is selected by programming pins 2 through 7 (see Table I). Notice that for the gain of 1000, a special gain sense is provided to preserve accuracy. Although this is not always required, gain errors caused by external resistance in series with the low value 40.04 Ω internal gain set resistor are thus eliminated.

GAIN	CONNECT PINS
1	6 to 7
10	2 to 6 and 7
100	3 to 6 and 7
1000	4 to 7 and separately 5 to 6

TABLE I. Pin-Programmable Gain Connections.

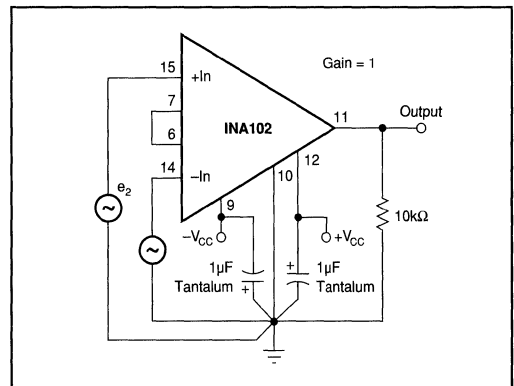


FIGURE 2. Basic Circuit Connection for the INA102.

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Other gains between 1 and 10, 10 and 100, and 100 and 1000 can also be obtained by connecting an external resistor between pin 6 and either pin 2, 3, or 4, respectively (see Figure 6 for application).

$G = 1 + (40/R_G)$ where R_G is the total resistance between the two inverting inputs of the input op amps. At high gains, where the value of R_G becomes small, additional resistance (i.e., relays or sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is sometimes desirable to null the input and/or output offset to achieve higher accuracy. The quality of the potentiometer will affect the results; therefore, choose one with good temperature and mechanical-resistance stability.

The optional offset null capabilities are shown in Figure 3. R_4 adjustment affects only the input stage component of the offset voltage. Note that the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu\text{V}/^\circ\text{C}$ per $100\mu\text{V}$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offset correction can be accomplished with A_1 , R_1 , R_2 , and R_3 , by applying a voltage to Common (pin 10) through a buffer amplifier. This buffer limits the resistance in series with pin 10 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 100dB. Be certain to keep this resistance low.

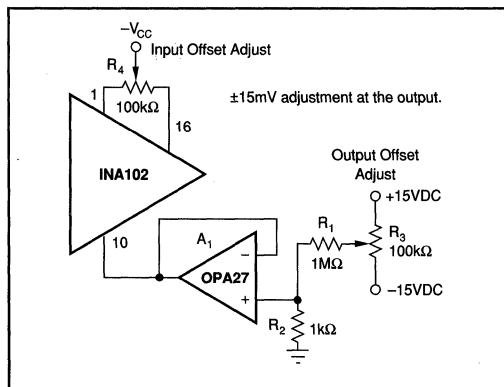


FIGURE 3. Optional Offset Nulling.

It is important to not exceed the input amplifiers' dynamic range. The amplified differential input signal and its associated common-mode voltage should not cause the output of A_1 or A_2 to exceed approximately $\pm 12\text{V}$ with $\pm 15\text{V}$ supplies, or nonlinear operation will result. To protect against moisture, especially in high gain, sealing compound may be used. Current injected into the offset pins should be minimized.

OPTIONAL FILTERING

The INA102 has provisions for accomplishing filtering with one external capacitor between pins 11 and 13. This single-pole filter can be used to reduce noise outside the signal bandwidth, but with some degradation to AC CMR.

When it is important to preserve CMR versus frequency (especially at 60Hz), two capacitors should be used. The additional capacitor is connected between pins 8 and 10. This will maintain a balance of impedances in the output stage. Either of these capacitors could also be trimmed slightly, to maximize CMR, if desired. Note that their ratio tracking will affect CMR over temperature.

OPTIONAL COMMON-MODE REJECTION TRIM

The INA102 is laser-adjusted during manufacturing to assure high CMR. However, if desired, a small resistance can be added in series with pin 10 to trim the CMR to an improved level. Depending upon the nature of the internal imbalances, either positive or negative resistance value could be required. The circuit shown in Figure 4 acts as a bipolar potentiometer and allows easy adjustment of CMR.

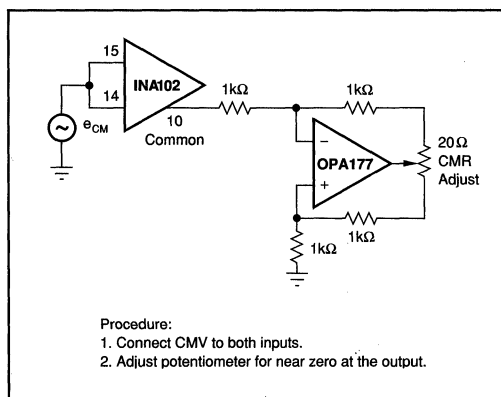


FIGURE 4. Optional Circuit for Externally Trimming CMR.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTDs. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA102 accomplishes all of these with high precision at surprisingly low quiescent current. However, in higher gains (>100), the bias current can cause a large offset error at the output. This can saturate the output unless the source impedance is separated, e.g., two $500\text{k}\Omega$ paths instead of one $1\text{M}\Omega$ unbalanced input. Figures 5 through 16 show some typical applications circuits.

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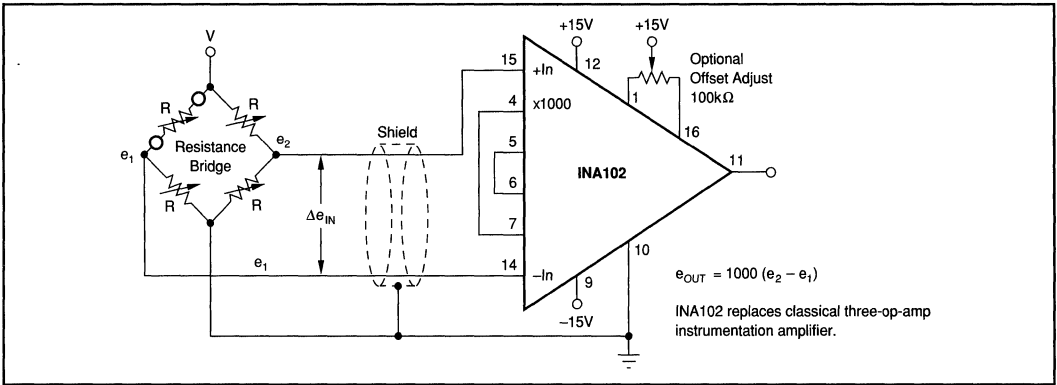


FIGURE 5. Amplification of a Differential Voltage from a Resistance Bridge.

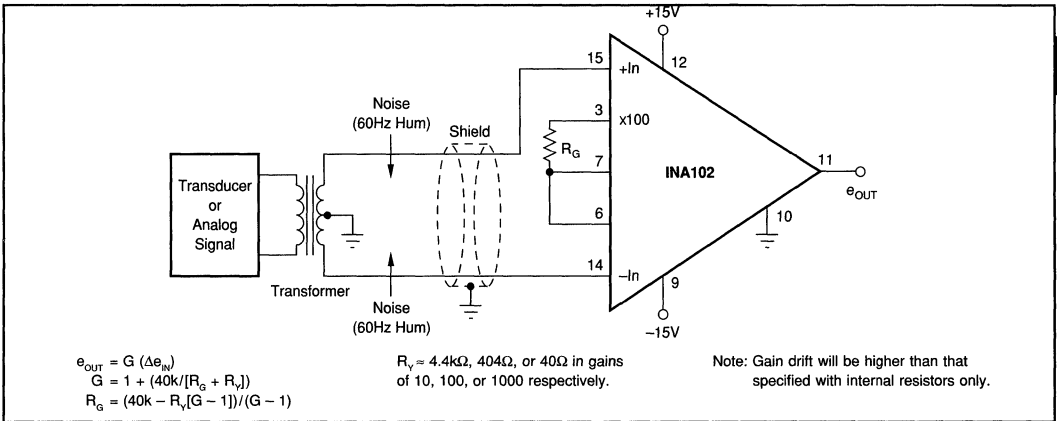


FIGURE 6. Amplification of a Transformer-Coupled Analog Signal Using External Gain Set.

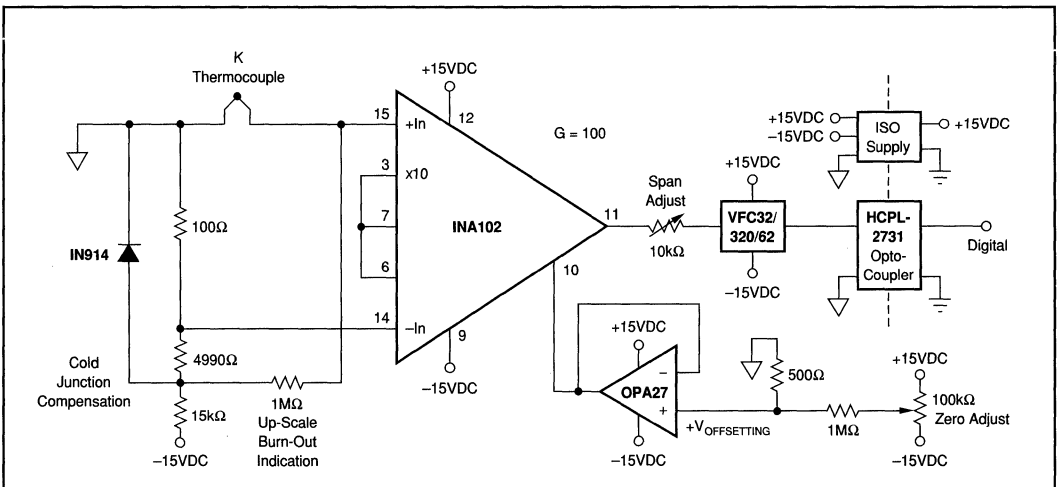


FIGURE 7. Isolated Thermocouple Amplifier with Cold Junction Compensation.

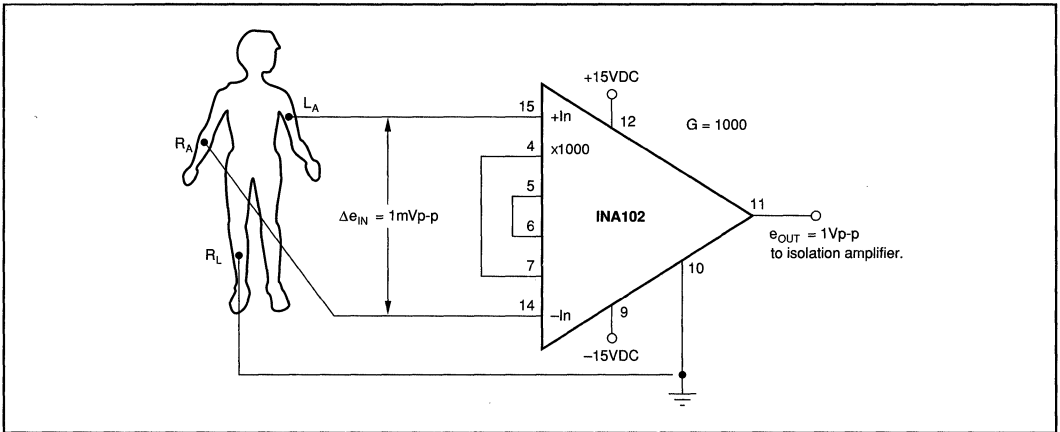


FIGURE 8. ECG Amplifier or Recorder Preamp for Biological Signals.

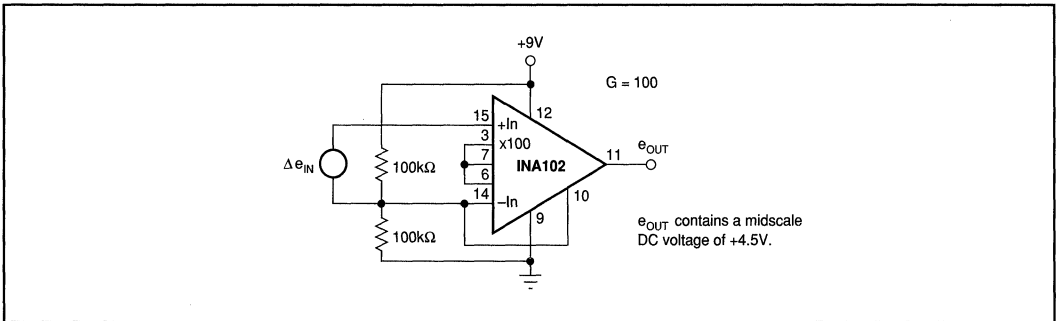


FIGURE 9. Single Supply Low Power Instrumentation Amplifier.

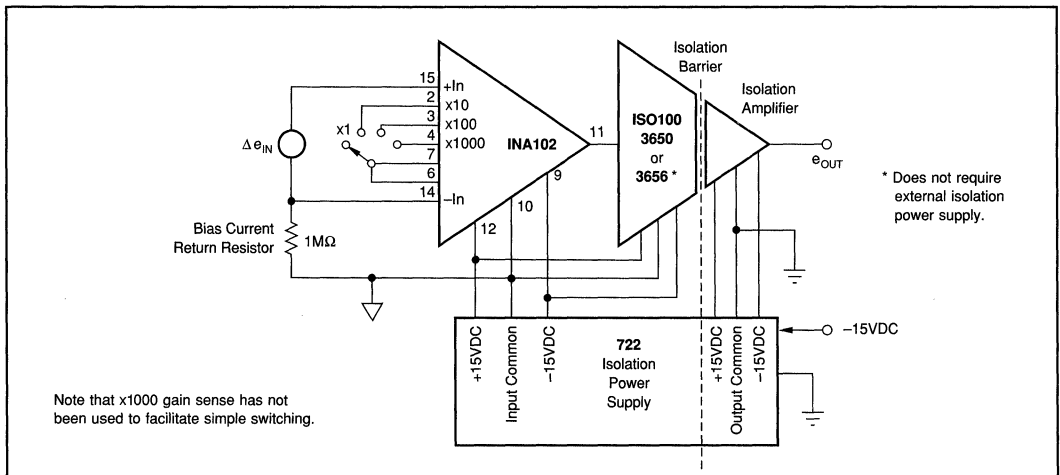


FIGURE 10. Precision Isolated Instrumentation Amplifier.

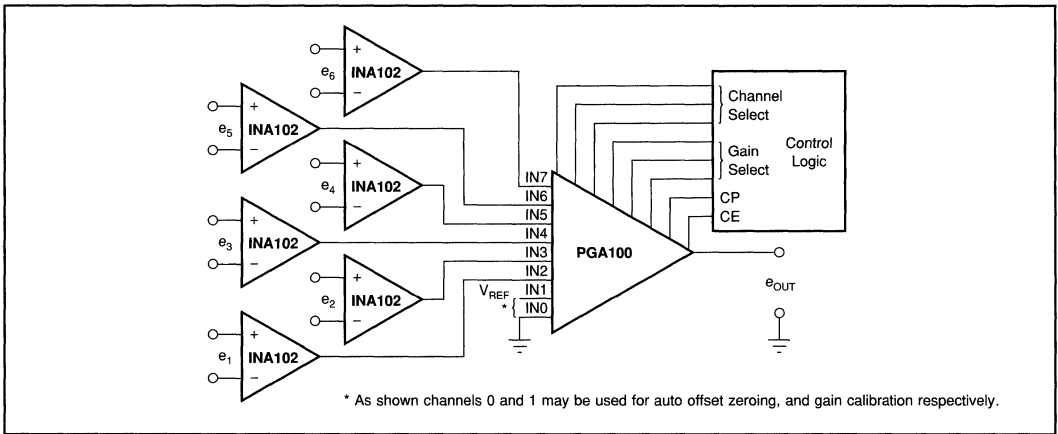


FIGURE 11. Multiple Channel Precision Instrumentation Amplifier with Programmable Gain.

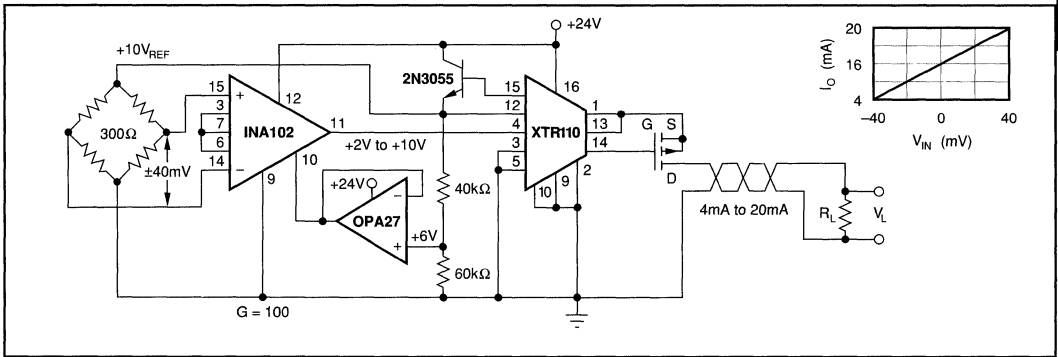


FIGURE 12. 4mA to 20mA Bridge Transmitter Using Single Supply Instrumentation Amplifier.

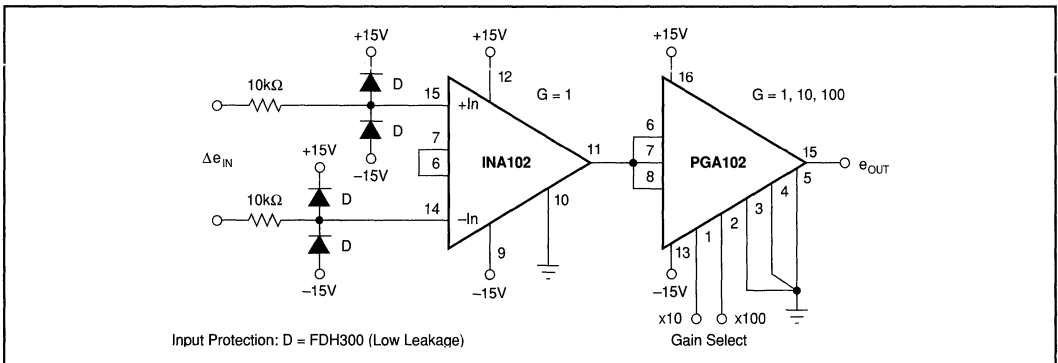


FIGURE 13. Programmable-Gain Instrumentation Amplifier Using the INA102 and PGA102.

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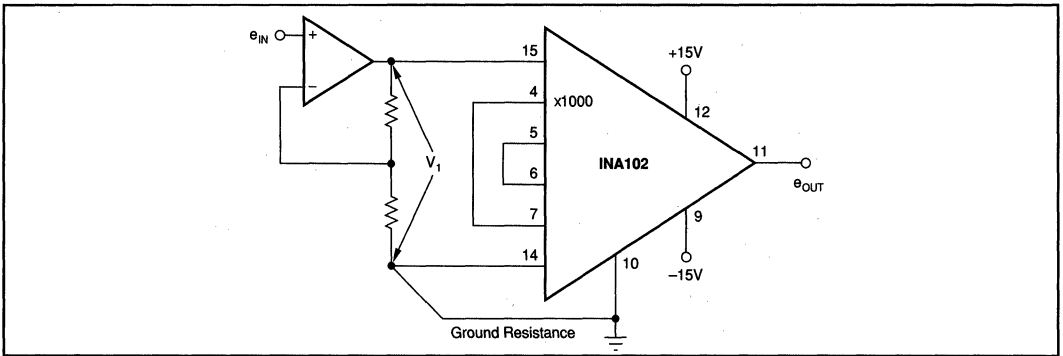


FIGURE 14. Ground Resistance Loop Eliminator (INA102 senses and amplifies V_1 accurately).

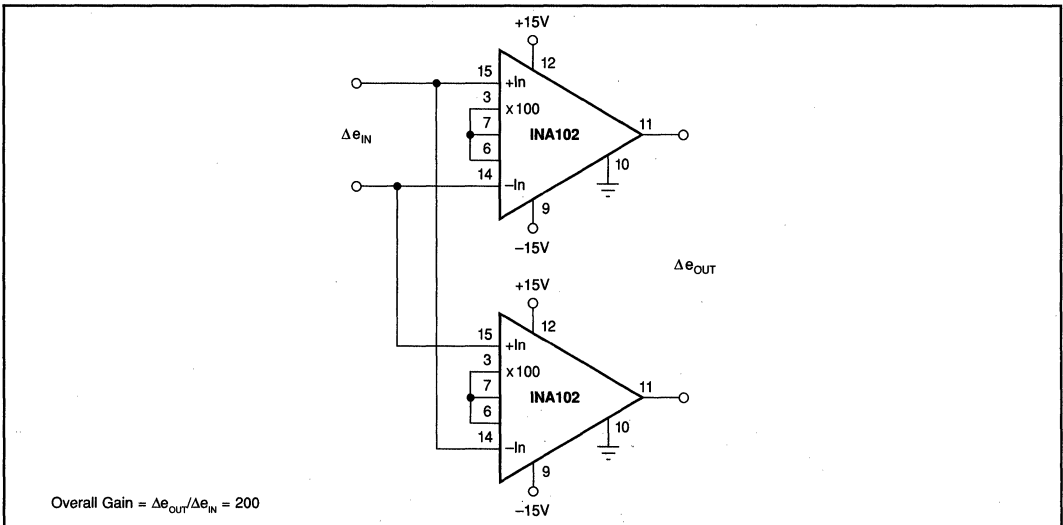


FIGURE 15. Differential Input/Differential Output Amplifier (twice the gain of one INA).

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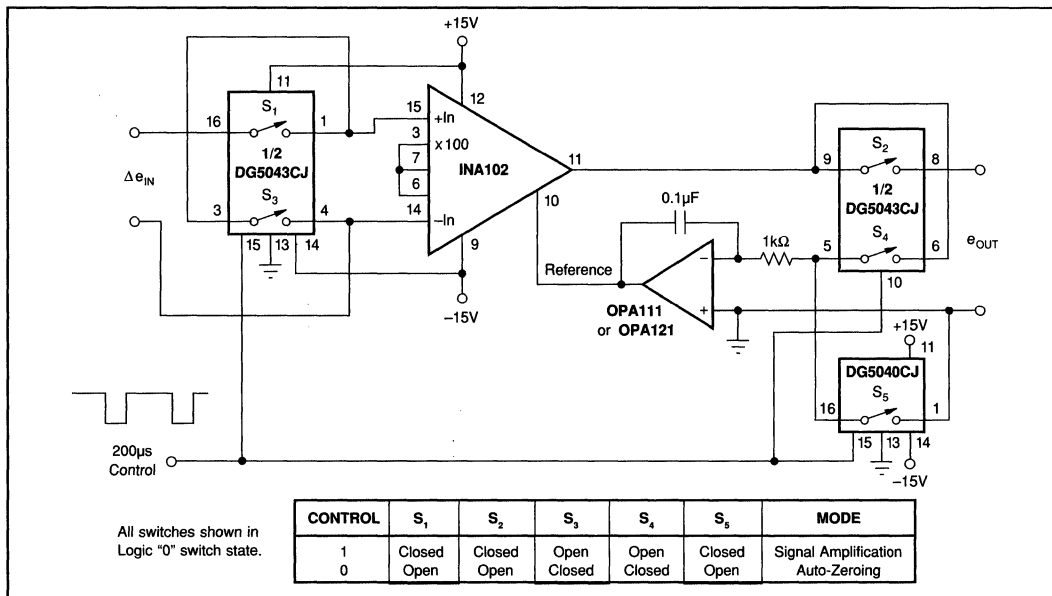
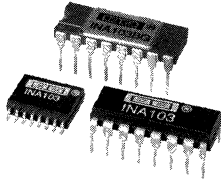


FIGURE 16. Auto-Zeroing Instrumentation Amplifier Circuit.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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INA103

Low Noise, Low Distortion INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW NOISE:** $1\text{nV}/\sqrt{\text{Hz}}$
- **LOW THD+N:** 0.0009% at 1kHz, $G = 100$
- **HIGH GBW:** 100MHz at $G = 1000$
- **WIDE SUPPLY RANGE:** $\pm 9\text{V}$ to $\pm 25\text{V}$
- **HIGH CMRR:** $>110\text{dB}$
- **BUILT-IN GAIN SETTING RESISTORS:**
 $G = 1, 100$
- **UPGRADES AD625**

APPLICATIONS

- **HIGH QUALITY MICROPHONE PREAMPS**
(REPLACES TRANSFORMERS)
- **MOVING-COIL PREAMPLIFIERS**
- **DIFFERENTIAL RECEIVERS**
- **AMPLIFICATION OF SIGNALS FROM:**
Strain Gages (Weigh Scale Applications)
Thermocouples
Bridge Transducers

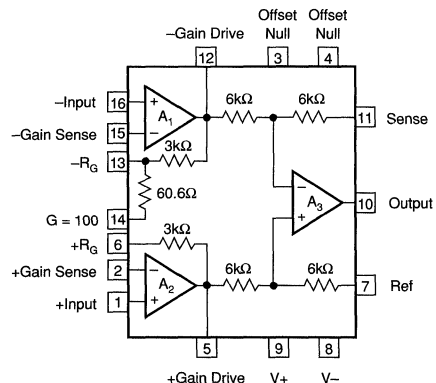
DESCRIPTION

The INA103 is a very low noise, low distortion monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response. It is ideal for low-level audio signals such as balanced low-impedance microphones. The INA103 provides near-theoretical limit noise performance for 200Ω source impedances. Many industrial applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. Its balanced input, low noise and low distortion provide superior performance compared to transformer-coupled microphone amplifiers used in professional audio equipment.

The INA103's wide supply voltage (± 9 to $\pm 25\text{V}$) and high output current drive allow its use in high-level audio stages as well. A copper lead frame in the plastic DIP assures excellent thermal performance.

The INA103 is available in 16-pin plastic DIP, 16-pin ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

All specifications at $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ and $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG			INA103BG			INA103KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1		1000	*	*	*	*	*	*	V/V
Gain Equation ⁽¹⁾		$G = 1 + 6\text{k}\Omega/R_G$				*			*	*	V/V
Gain Error, DC $G = 1$	$\pm 10\text{V}$ Output		0.005	0.05		0.003	0.01		*	*	%
$G = 100$			0.05	0.25		0.04	0.1		0.07	*	%
Equation			0.5			0.1			*	*	%
Gain Temp. Co. $G = 1$	$\pm 10\text{V}$ Output		10			*			*	*	ppm/ $^\circ\text{C}$
$G = 100$			25			*			*	*	ppm/ $^\circ\text{C}$
Equation			25			*			*	*	ppm/ $^\circ\text{C}$
Nonlinearity, DC $G = 1$	$\pm 10\text{V}$ Output		0.0003	0.01		0.0002	0.002		*	*	% of FS ⁽²⁾
$G = 100$			0.0006	0.01		0.0006	0.004		*	*	% of FS
OUTPUT											
Voltage, $R_L = 600\Omega$	$T_A = T_{\text{MIN}}$ to T_{MAX}	± 11.5	± 12		*	*		*	*	*	V
$R_L = 600\Omega$	$V_S = \pm 25$, $T_A = 25^\circ\text{C}$	± 20	± 21		*	*		*	*	*	V
Current	$T_A = T_{\text{MIN}}$ to T_{MAX}	± 40			*	*		*	*	*	mA
Short Circuit Current			± 70			*			*	*	mA
Capacitive Load Stability			10			*			*	*	nF
INPUT OFFSET VOLTAGE											
Initial Offset RTI ⁽³⁾			(20 + 700/G)	(100 + 5000/G)		(20 + 320/G)	(50 + 2000/G)		(30 + 1200/G)		μV
(KU Grade)										(250 + 5000/G)	μV
vs Temp $G = 1$ to 1000	$T_A = T_{\text{MIN}}$ to T_{MAX}		1 + 20/G			0.75 + 10/G			1 + 20/G		$\mu\text{V}/^\circ\text{C}$
$G = 1000$	$T_A = T_{\text{MIN}}$ to T_{MAX}		1	2		*	*		*	*	$\mu\text{V}/^\circ\text{C}$
vs Supply	$\pm 9\text{V}$ to $\pm 25\text{V}$		0.2 + 8/G	4 + 60/G		*	2 + 30/G		*	*	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT											
Initial Bias Current	$T_A = T_{\text{MIN}}$ to T_{MAX}		2.5	12		*	8		*	*	μA
vs Temp			15			*	40 ⁽⁴⁾		*	*	nA/ $^\circ\text{C}$
Initial Offset Current	$T_A = T_{\text{MIN}}$ to T_{MAX}		0.04	1		0.03	0.5		*	*	μA
vs Temp			0.5			*	2.5 ⁽⁴⁾		*	*	nA/ $^\circ\text{C}$
INPUT IMPEDANCE											
Differential Mode			60 2			*			*	*	M Ω pF
Common-Mode			60 5			*			*	*	M Ω pF
INPUT VOLTAGE RANGE											
Common-Mode Range ⁽⁵⁾		± 11	± 12		*	*		*	*	*	V
CMR											
$G = 1$	DC to 60Hz	72	86		80	91		*	*	*	dB
$G = 100$	DC to 60Hz	100	125		110	129		*	*	*	dB
INPUT NOISE											
Voltage ⁽⁶⁾	$R_G = 0\Omega$										
10Hz			2			*			*	*	nV/ $\sqrt{\text{Hz}}$
100Hz			1.2			*			*	*	nV/ $\sqrt{\text{Hz}}$
1kHz			1			*	1.4 ⁽⁴⁾		*	*	nV/ $\sqrt{\text{Hz}}$
Current, 1kHz			2			*			*	*	pA/ $\sqrt{\text{Hz}}$
OUTPUT NOISE											
Voltage	1kHz		65			*			*	*	nV/ $\sqrt{\text{Hz}}$
A Weighted, 20Hz-20kHz	20Hz-20kHz		-100			*			*	*	dBu
DYNAMIC RESPONSE											
-3dB Bandwidth: $G = 1$	Small Signal		6			*			*	*	MHz
$G = 100$	Small Signal		800			*			*	*	kHz
Full Power Bandwidth	$G = 1$					*			*	*	kHz
	$V_{\text{OUT}} = \pm 10\text{V}$, $R_L = 600\Omega$		240			*			*	*	kHz
Slew Rate	$G = 1$ to 500		15			*			*	*	V/ μs
THD + Noise	$G = 100$, $f = 1\text{kHz}$		0.0009			*			*	*	%
Settling Time 0.1%											
$G = 1$	$V_O = 20\text{V}$ Step		1.7			*			*	*	μs
$G = 100$			1.5			*			*	*	μs
Settling Time 0.01%											
$G = 1$	$V_O = 20\text{V}$ Step		2			*			*	*	μs
$G = 100$			3.5			*			*	*	μs
Overload Recovery ⁽⁷⁾	50% Overdrive		1			*			*	*	μs

*Same specification as INA103AG.

NOTES: (1) Gains other than 1 and 100 can be set by adding an external resistor, R_G between pins 2 and 15. Gain accuracy is a function of R_G . (2) FS = Full Scale. (3) Adjustable to zero. (4) Guaranteed by design. (5) $V_O = 0\text{V}$, see Typical Curves for V_{CM} vs V_O . (6) $V_{\text{NOISE RTI}} = \sqrt{V_{\text{N INPUT}}^2 + (V_{\text{N OUTPUT}}/\text{Gain})^2 + 4\text{KTR}_G}$. See Typical Curves. (7) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.



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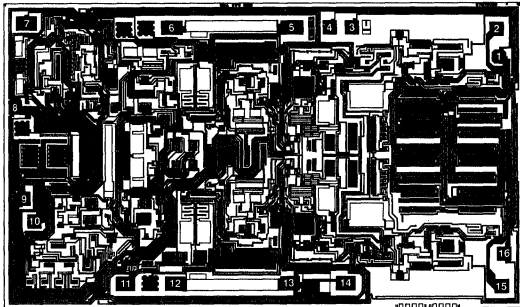
SPECIFICATIONS (CONT)

ELECTRICAL

All specifications at $T_A = +25^\circ\text{C}$, $V_G = \pm 15\text{V}$ and $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA103AG			INA103BG			INA103KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			± 15		*	*	*	*	*	*	V
Voltage Range		± 9		± 25							V
Quiescent Current			9	12.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		-25		+85	*		*	0		+70	$^\circ\text{C}$
Operation		-55		+125	*		*	-40		+85	$^\circ\text{C}$
Storage		-65		+150	*		*	-40		+100	$^\circ\text{C}$
Thermal Resistance, θ_{JA}			100			*			*		$^\circ\text{C}/\text{W}$

DICE INFORMATION



INA103 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+Input	9	V+
2	+Gain Sense	10	Output
3	+Offset Null	11	Sense
4	-Offset Null	12	-Gain Drive
5	+Gain Drive	13	- R_G
6	+ R_G	14	G = 100
7	Ref	15	-Gain Sense
8	V-	16	-Input

Substrate Bias: Electrically connected to V- supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	194 x 115 ± 5	4.93 x 2.92 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Chromium-Silver	

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA103AG	Ceramic DIP	109
INA103BG	Ceramic DIP	109
INA103KP	Plastic DIP	180
INA103KU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMP RANGE
INA103AG	Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
INA103BG	Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
INA103KP	Plastic DIP	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$
INA103KU	SOL-16	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$

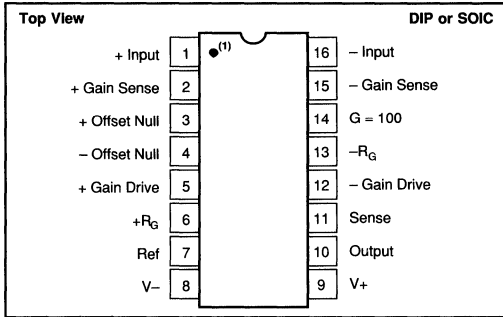
ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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PIN CONFIGURATION



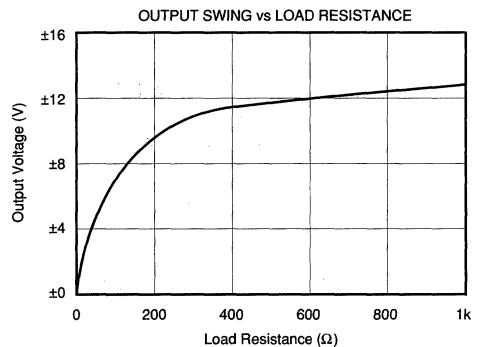
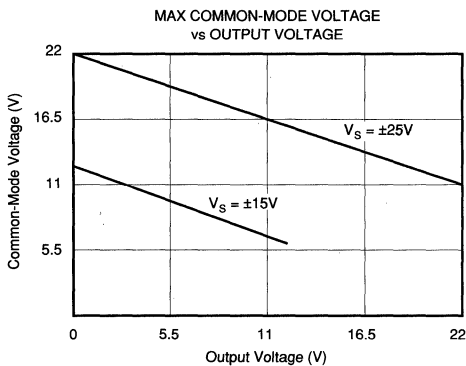
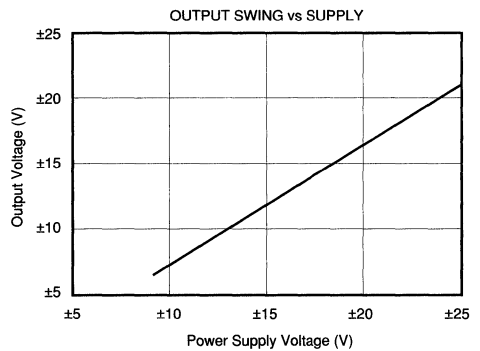
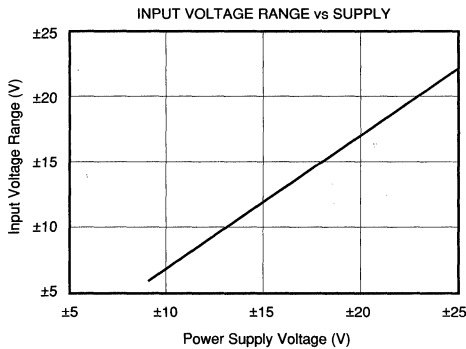
NOTE: (1) Pin 1 Marking—SOL-16 Package

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±25V
Input Voltage Range, Continuous	±V _S
Operating Temperature Range:	
P, U Package	-40°C to +85°C
G Package	-55°C to +125°C
Storage Temperature Range:	
P, U Package	-40°C to +100°C
G Package	-65°C to +150°C
Junction Temperature:	
P, U Package	+125°C
G Package	+150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V unless otherwise noted.

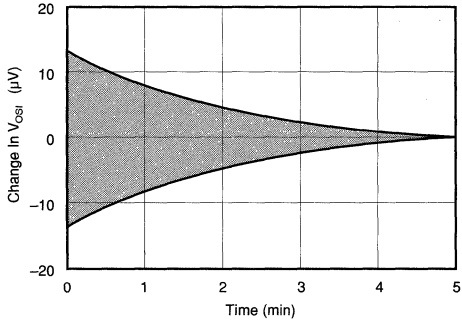


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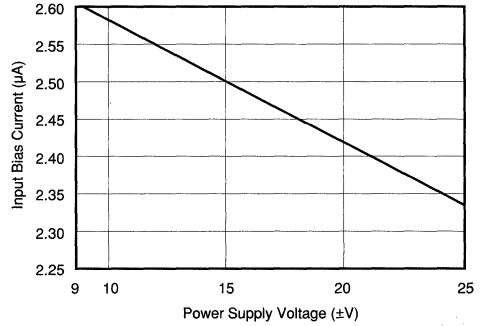
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

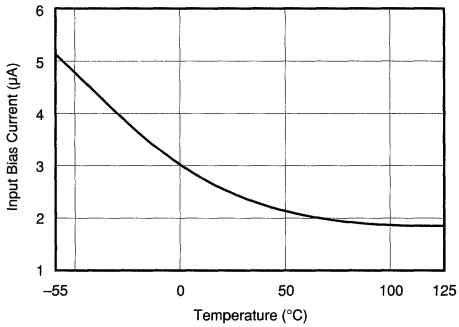
OFFSET VOLTAGE vs TIME FROM POWER UP
($G = 100$)



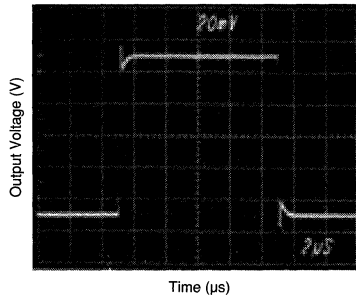
INPUT BIAS CURRENT vs SUPPLY



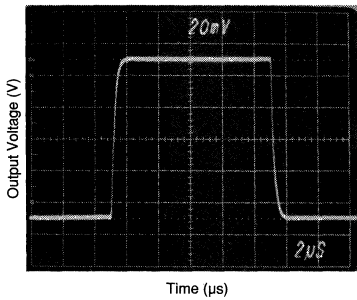
INPUT BIAS CURRENT vs TEMPERATURE



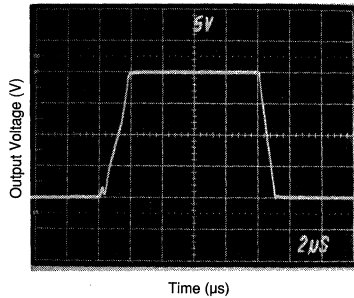
SMALL SIGNAL TRANSIENT RESPONSE
($G = 1$)



SMALL SIGNAL TRANSIENT RESPONSE
($G = 100$)



LARGE SIGNAL TRANSIENT RESPONSE
($G = 1$)

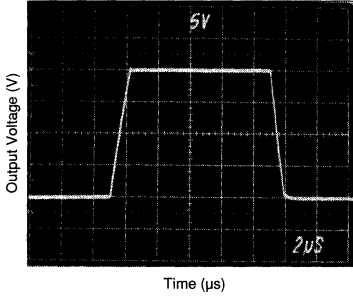


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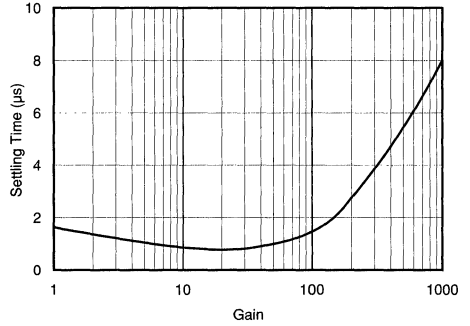
TYPICAL PERFORMANCE CURVES (CONT)

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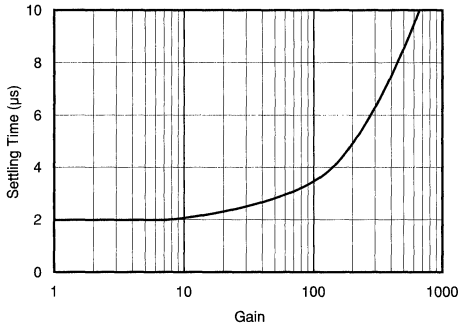
LARGE SIGNAL TRANSIENT RESPONSE
($G = 100$)



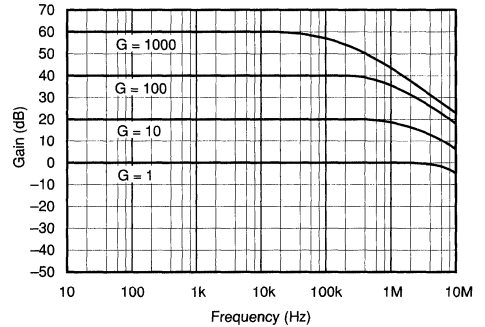
SETTLING TIME vs GAIN
(0.1%, 20V STEP)



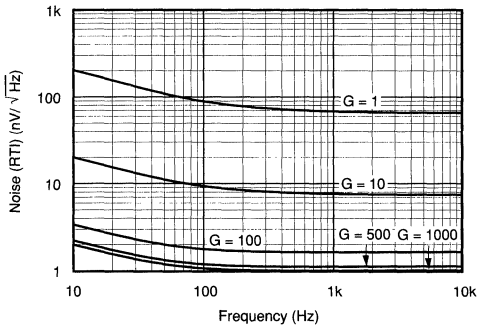
SETTLING TIME vs GAIN
(0.01%, 20V STEP)



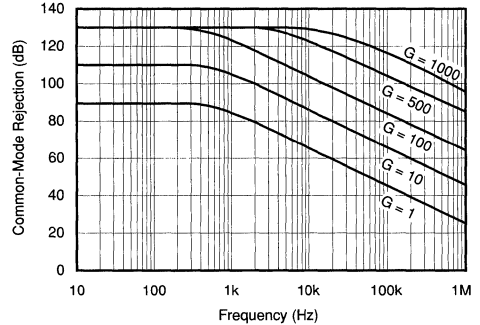
SMALL-SIGNAL FREQUENCY RESPONSE



NOISE VOLTAGE (RTI) vs FREQUENCY



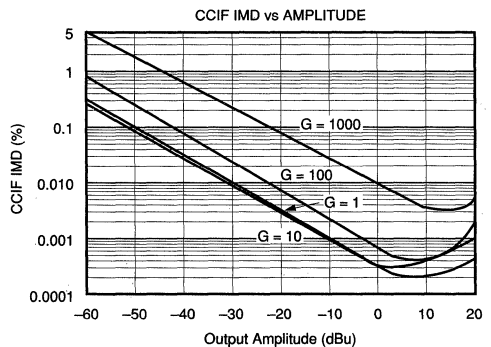
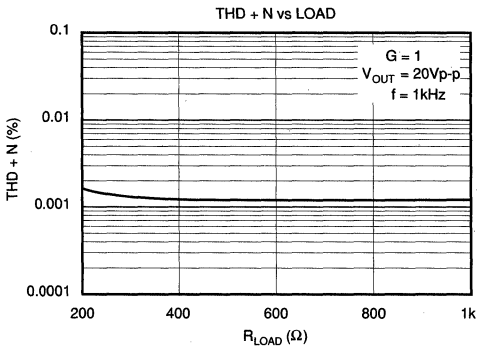
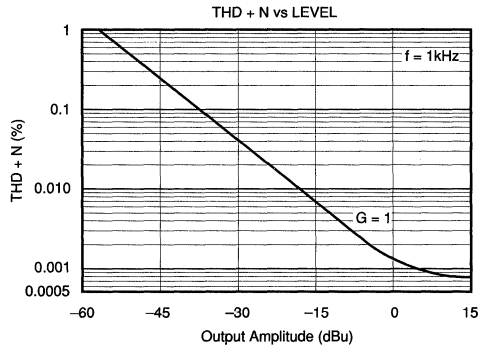
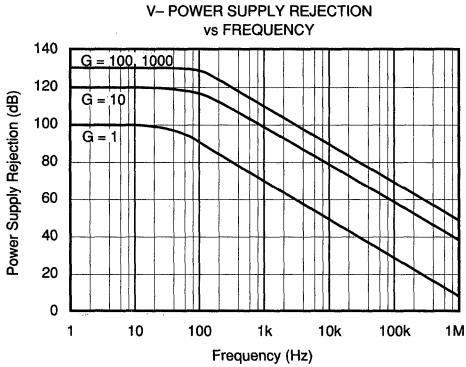
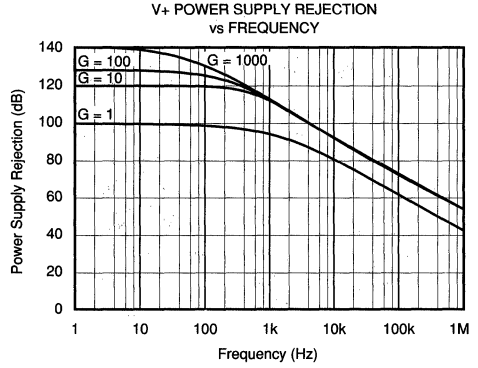
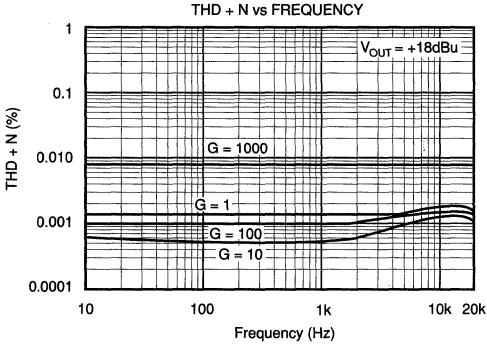
CMR vs FREQUENCY



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TYPICAL PERFORMANCE CURVES (CONT)

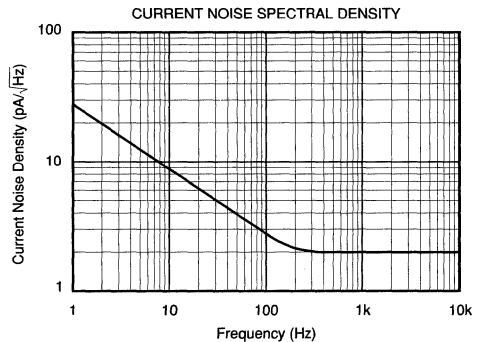
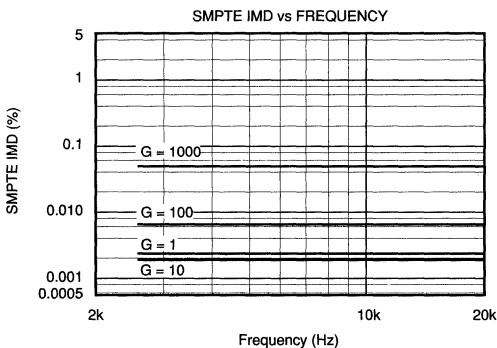
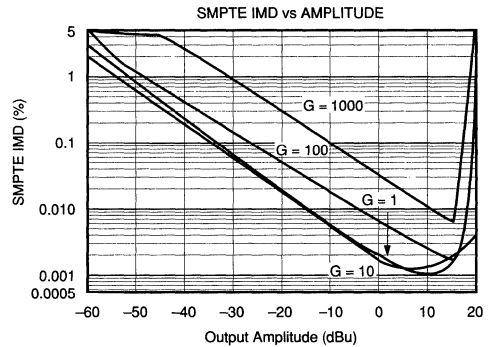
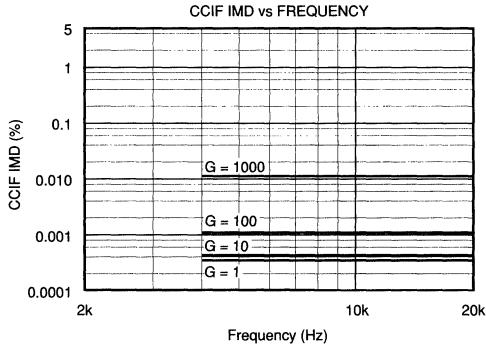
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with $1\mu\text{F}$ tantalum capacitors near the device pins. The output Sense (pin 11) and output Reference (pin 7) should be low impedance connections. Resistance of a few ohms in series with these connections will degrade the common-mode rejection of the amplifier.

To avoid oscillations, make short, direct connection to the gain set resistor and gain sense connections. Avoid running output signals near these sensitive input nodes.

INPUT CONSIDERATIONS

Certain source impedances can cause the INA103 to oscillate. This depends on circuit layout and source or cable characteristics connected to the input. An input network consisting of a small inductor and resistor (Figure 2) can greatly reduce the tendency to oscillate. This is especially

useful if various input sources are connected to the INA103. Although not shown in other figures, this network can be used, if needed, with all applications shown.

GAIN SELECTION

Gains of 1 or 100V/V can be set without external resistors. For $G = 1\text{V/V}$ (unity gain) leave pin 14 open (no connection)—see Figure 4. For $G = 100\text{V/V}$, connect pin 14 to pin 6—see Figure 5.

Gain can also be accurately set with a single external resistor as shown in Figure 1. The two internal feedback resistors are laser-trimmed to $3\text{k}\Omega$ within approximately $\pm 0.1\%$. The temperature coefficient of these resistors is approximately $50\text{ppm}/^\circ\text{C}$. Gain using an external R_G resistor is—

$$G = 1 + \frac{6\text{k}\Omega}{R_G}$$

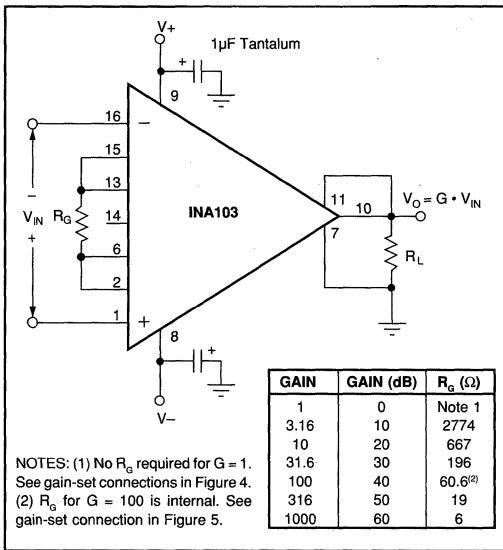


FIGURE 1. Basic Circuit Configuration.

Accuracy and TCR of the external R_G will also contribute to gain error and temperature drift. These effects can be directly inferred from the gain equation.

Connections available on A₁ and A₂ allow external resistors to be substituted for the internal 3kΩ feedback resistors. A precision resistor network can be used for very accurate and stable gains. To preserve the low noise of the INA103, the value of external feedback resistors should be kept low. Increasing the feedback resistors to 20kΩ would increase noise of the INA103 to approximately 1.5nV/√Hz. Due to the current-feedback input circuitry, bandwidth would also be reduced.

NOISE PERFORMANCE

The INA103 provides very low noise with low source impedance. Its 1nV/√Hz voltage noise delivers near theoretical noise performance with a source impedance of 200Ω.

Relatively high input stage current is used to achieve this low noise. This results in relatively high input bias current and input current noise. As a result, the INA103 may not provide best noise performance with source impedances greater than 10kΩ. For source impedance greater than 10kΩ, consider the INA114 (excellent for precise DC applications), or the INA111 FET-input IA for high speed applications.

OFFSET ADJUSTMENT

Offset voltage of the INA103 has two components: input stage offset voltage is produced by A₁ and A₂; and, output stage offset is produced by A₃. Both input and output stage offset are laser trimmed and may not need adjustment in many applications.

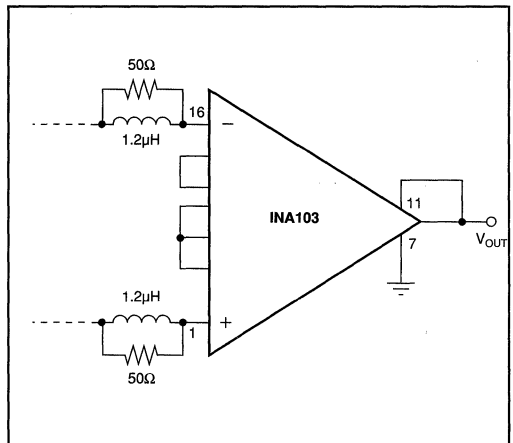


FIGURE 2. Input Stabilization Network.

Offset voltage can be trimmed with the optional circuit shown in Figure 3. This offset trim circuit primarily adjusts the output stage offset, but also has a small effect on input stage offset. For a 1mV adjustment of the output voltage, the input stage offset is adjusted approximately 1µV. Use this adjustment to null the INA103's offset voltage with zero differential input voltage. Do not use this adjustment to null offset produced by a sensor, or offset produced by subsequent stages, since this will increase temperature drift.

To offset the output voltage without affecting drift, use the circuit shown in Figure 4. The voltage applied to pin 7 is summed at the output. The op amp connected as a buffer provides a low impedance at pin 7 to assure good common-mode rejection.

Figure 5 shows a method to trim offset voltage in ac-coupled applications. A nearly constant and equal input bias current of approximately 2.5µA flows into both input terminals. A variable input trim voltage is created by adjusting the balance of the two input bias return resistances through which the input bias currents must flow.

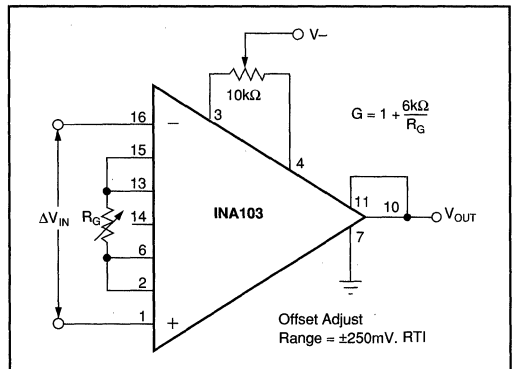


FIGURE 3. Offset Adjustment Circuit.

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Figure 6 shows an active control loop that adjusts the output offset voltage to zero. A₂, R, and C form an integrator that produces an offsetting voltage applied to one input of the INA103. This produces a -6dB/octave low frequency roll-off like the capacitor input coupling in Figure 5.

COMMON-MODE INPUT RANGE

For proper operation, the combined differential input signal and common-mode input voltage must not cause the input amplifiers to exceed their output swing limits. The linear input range is shown in the typical performance curve "Maximum Common-Mode Voltage vs Output Voltage." For a given total gain, the input common-mode range can be increased by reducing the input stage gain and increasing the output stage gain with the circuit shown in Figure 7.

OUTPUT SENSE

An output sense terminal allows greater gain accuracy in driving the load. By connecting the sense connection at the load, I•R voltage loss to the load is included inside the feedback loop. Current drive can be increased by connecting a current booster inside the feedback loop as shown in Figure 11.

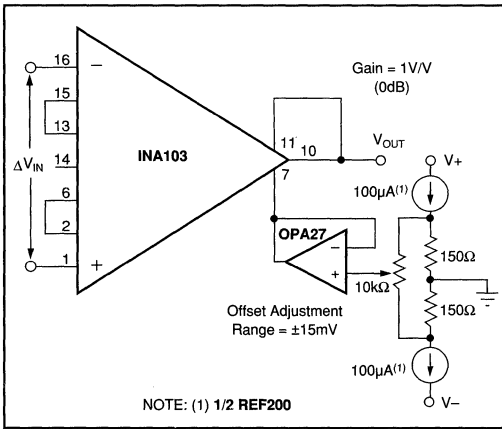


FIGURE 4. Output Offsetting.

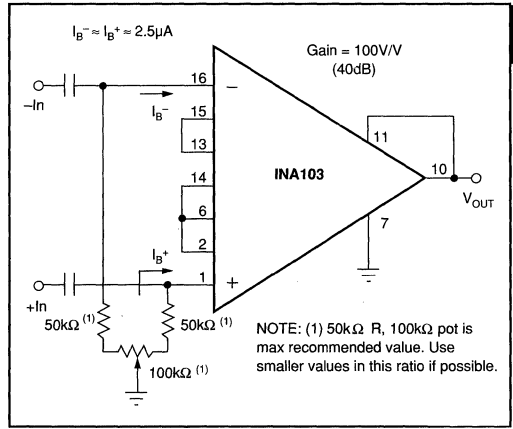


FIGURE 5. Input Offset Adjustment for AC-Coupled Inputs.

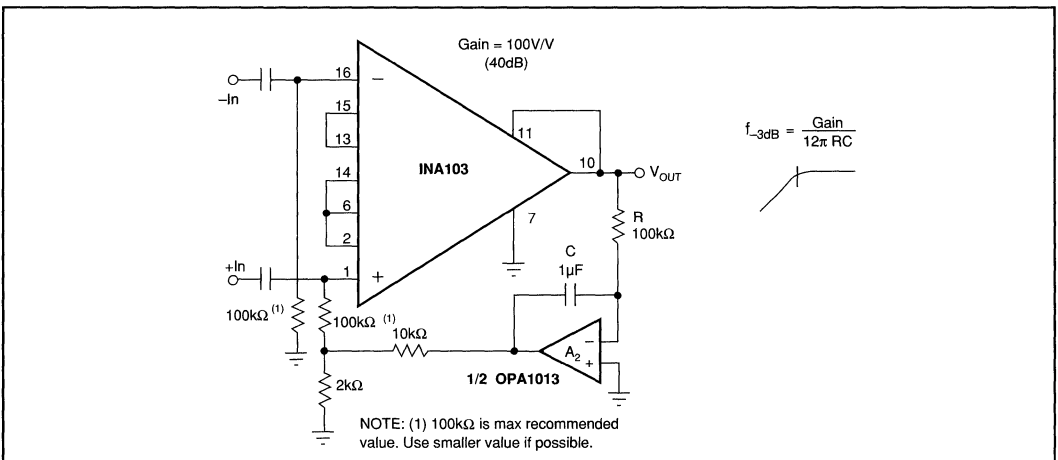


FIGURE 6. Automatic DC Restoration.

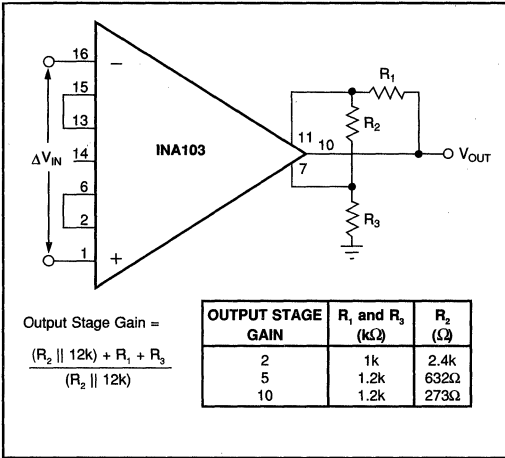


FIGURE 7. Gain Adjustment of Output Stage.

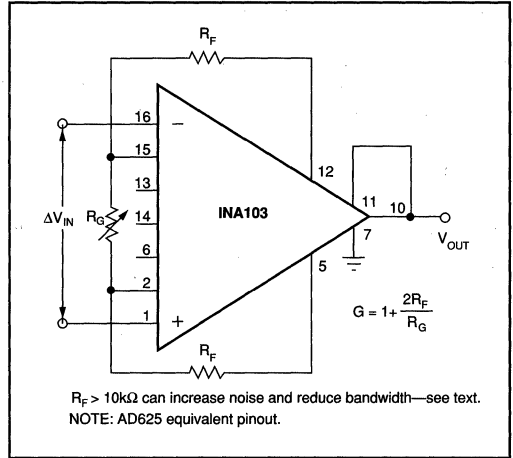


FIGURE 8. Use of External Resistors for Gain Set.

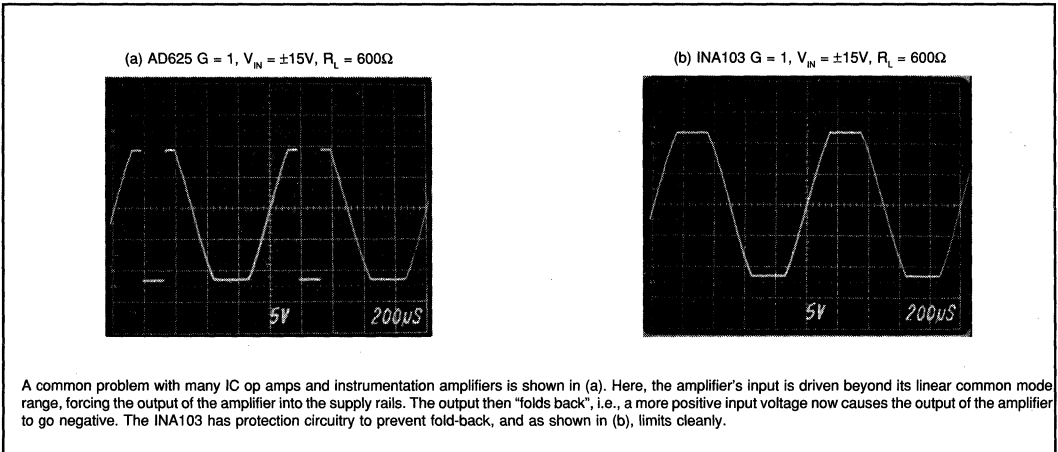


FIGURE 9. INA103 Overload Condition Performance.

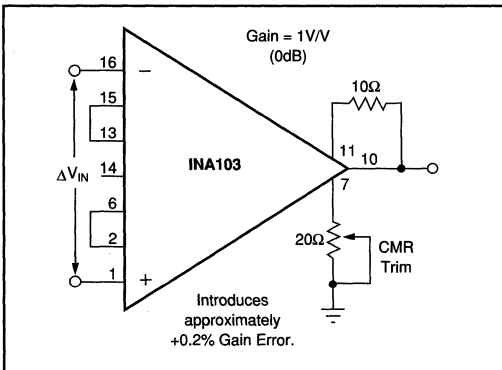


FIGURE 10. Optional Circuit for Externally Trimming CMR.

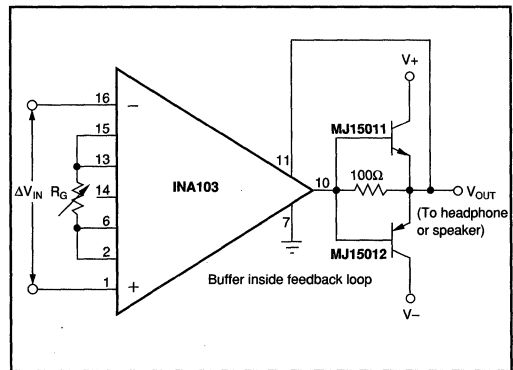


FIGURE 11. Increasing Output Circuit Drive.

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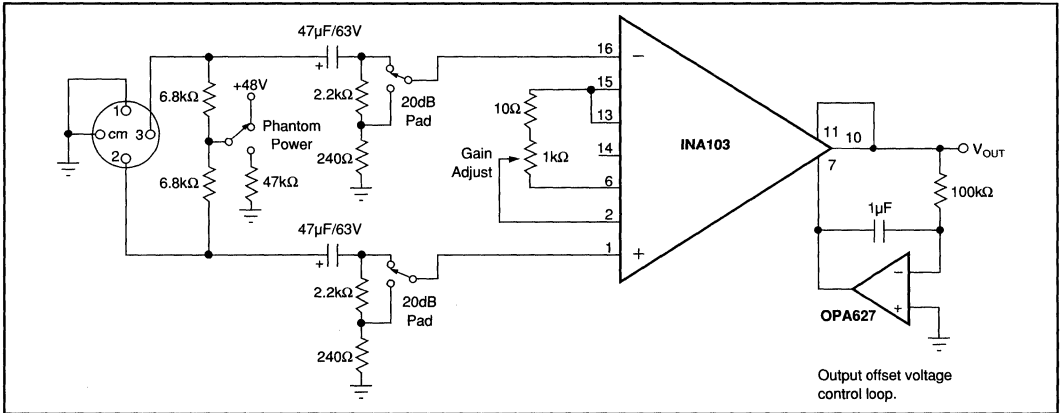


FIGURE 12. Microphone Preamplifier with Provision for Phantom Power Microphones.

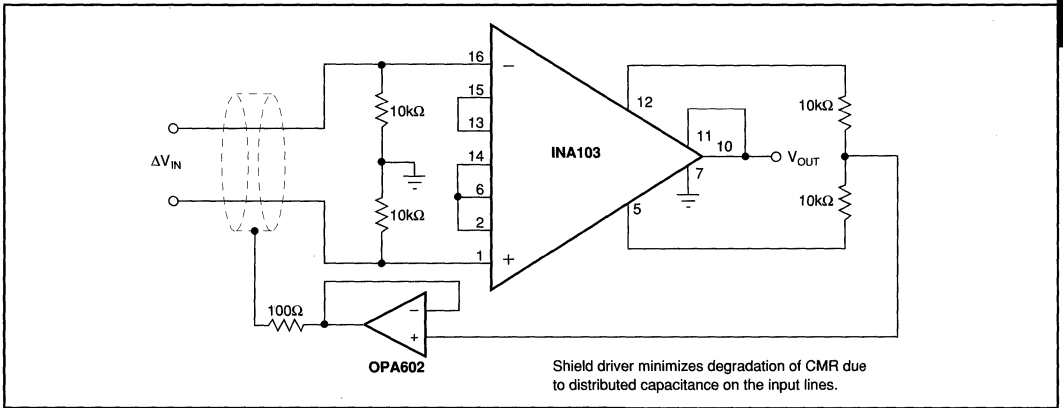


FIGURE 13. Instrumentation Amplifier with Shield Driver.

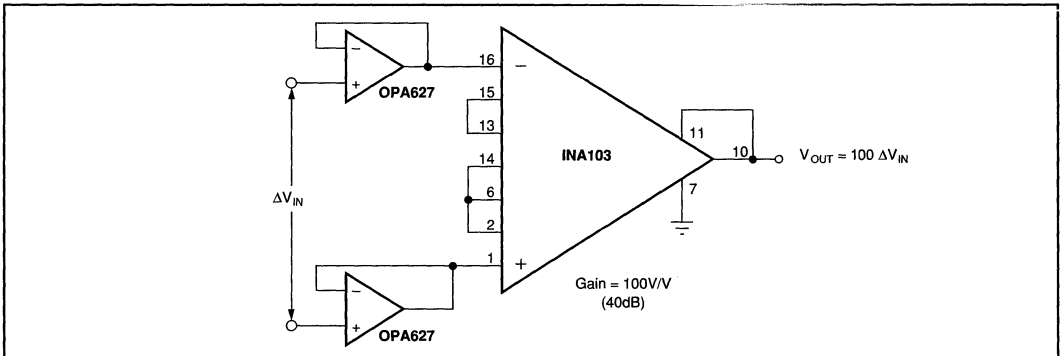
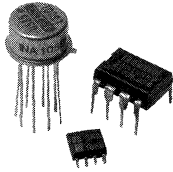


FIGURE 14. Gain-of-100 INA103 with FET Buffers.

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INA105

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR 0.01% max
- NONLINEARITY 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- PLASTIC DIP, TO-99 HERMETIC METAL, AND SO-8 SOIC PACKAGES

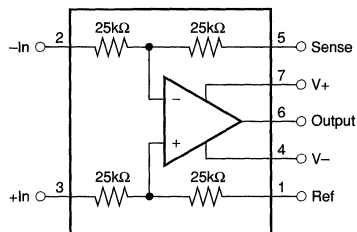
APPLICATIONS

- DIFFERENTIAL AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a monolithic Gain=1 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides this precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SO-8 surface-mount and TO-99 metal packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At +25°C, $V_{CC} = \pm 15V$ unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM			INA105BM			INA105KP/KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial ⁽¹⁾			1		*	*		*	*		V/V
Error vs Temperature			0.005	0.01	*	*		0.01	0.025		%
Nonlinearity ⁽²⁾			1	5	*	*		*	*		ppm/°C
			0.0002	0.001	*	*		*	*		%
OUTPUT											
Rated Voltage	$I_O = +20mA, -5mA$	10	12		*	*		*	*		V
Rated Current	$V_O = 10V$	+20, -5			*	*		*	*		mA
Impedance			0.01		*	*		*	*		Ω
Current Limit	To Common		+40/-10		*	*		*	*		mA
Capacitive Load	Stable Operation		1000		*	*		*	*		pF
INPUT											
Impedance ⁽³⁾	Differential		50		*	*		*	*		k Ω
	Common-mode		50		*	*		*	*		k Ω
Voltage Range ⁽⁴⁾	Differential	± 10			*	*		*	*		V
	Common-mode	± 20			*	*		*	*		V
Common-mode Rejection ⁽⁵⁾	$T_A = T_{MIN}$ to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE											
Initial	RTO ⁽⁶⁾⁽⁷⁾		50	250	*	*		*	*	500	μV
vs Temperature			5	20	*	5	10	*	*	*	$\mu V/°C$
vs Supply	$\pm V_S = 6V$ to $18V$		1	25	*	*	15	*	*	*	$\mu V/V$
vs Time			20		*	*		*	*	*	$\mu V/mo$
OUTPUT NOISE VOLTAGE											
$f_b = 0.01Hz$ to $10Hz$	RTO ⁽⁶⁾⁽⁸⁾		2.4		*	*		*	*		$\mu Vp-p$
$f_o = 10kHz$			60		*	*		*	*		nV/\sqrt{Hz}
DYNAMIC RESPONSE											
Small Signal Bandwidth	-3dB		1		*	*		*	*		MHz
Full Power Bandwidth	$V_O = 20Vp-p$	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/ μs
Settling Time: 0.1%	$V_O = 10V$ Step		4		*	*		*	*		μs
0.01%	$V_O = 10V$ Step		5		*	*		*	*		μs
0.01%	$V_{CM} = 10V$ Step, $V_{DIFF} = 0V$		1.5		*	*		*	*		μs
POWER SUPPLY											
Rated			± 15		*	*		*	*		V
Voltage Range	Derated Performance	± 5		± 18	*	*		*	*		V
Quiescent Current	$V_O = 0V$		± 1.5	± 2	*	*		*	*		mA
TEMPERATURE RANGE											
Specification		-40		+85	*	*		*	*		°C
Operation		-55		+125	*	*		-40	+85		°C
Storage		-65		+150	*	*		-40	+125		°C

* Specification same as for INA105AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25k Ω resistors are ratio matched but have $\pm 20\%$ absolute value. (4) Maximum input voltage without protection is 10V more than either $\pm 15V$ supply ($\pm 25V$). Limit I_{IN} to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18V$
Input Voltage Range	$\pm V_S$
Operating Temperature Range: M	-55°C to +125°C
P, U	-40°C to +85°C
Storage Temperature Range: M	-65°C to +150°C
P, U	-40°C to +125°C
Lead Temperature (soldering, 10s) M, P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

PACKAGE INFORMATION⁽¹⁾

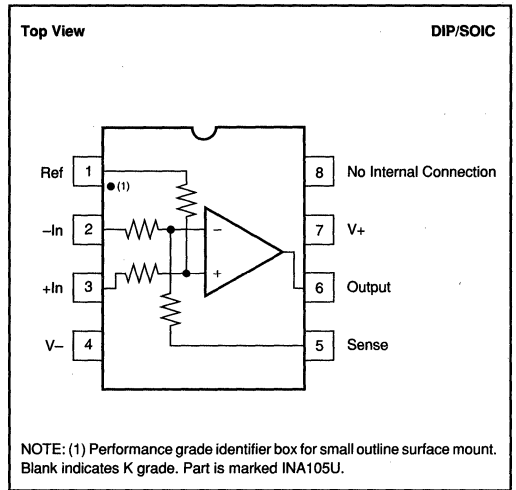
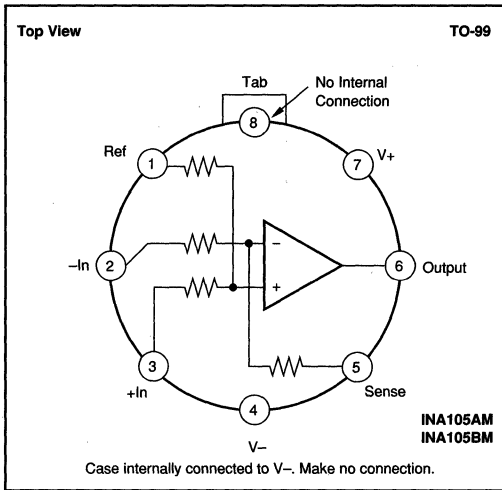
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA105AM	TO-99 Metal	001
INA105BM	TO-99 Metal	001
INA105KP	8-Pin Plastic DIP	006
INA105KU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

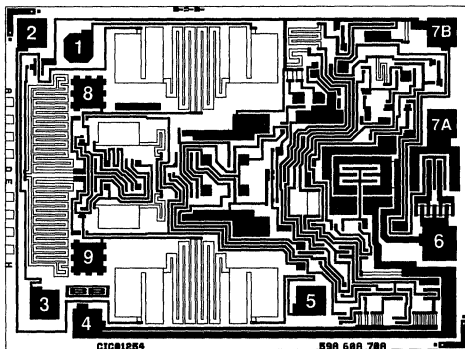
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PIN DESIGNATIONS



DICE INFORMATION



PAD	FUNCTION
1	Reference
2	-In
3	+In
4	V-
5	Sense
6	Output
7A	V+ (Connect Both)
7B	V+ (Connect Both)
8	(Op Amp +In)
9	(Op Amp -In)

Substrate Bias: Electrically connected to V- supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	83 x 63 ±5	2.11 x 1.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

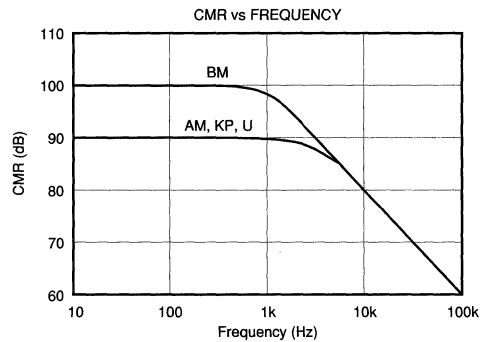
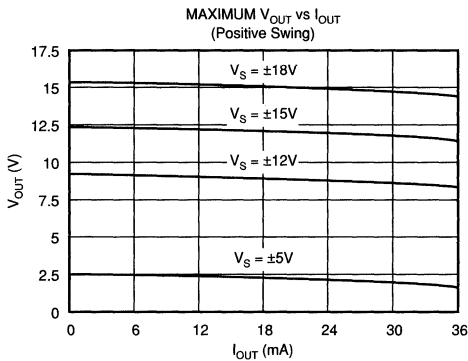
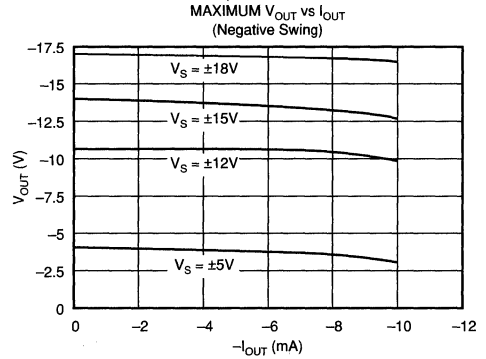
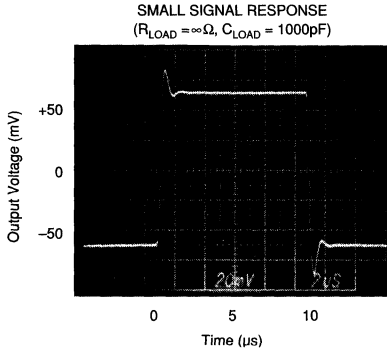
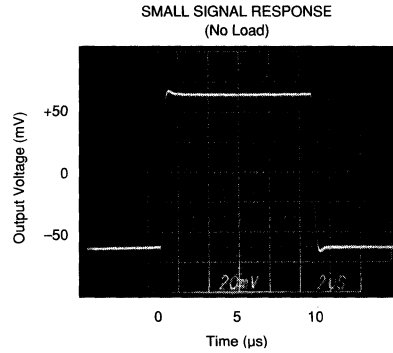
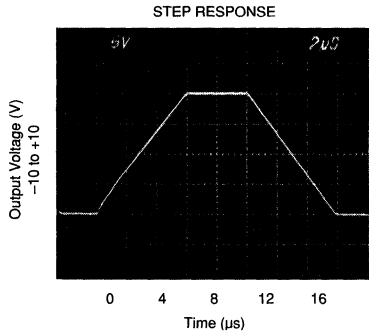
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
INA105AM	TO-99 Metal	-40°C to +85°C
INA105BM	TO-99 Metal	-40°C to +85°C
INA105KP	8-Pin Plastic DIP	-40°C to +85°C
INA105KU	8-Pin SOIC	-40°C to +85°C

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

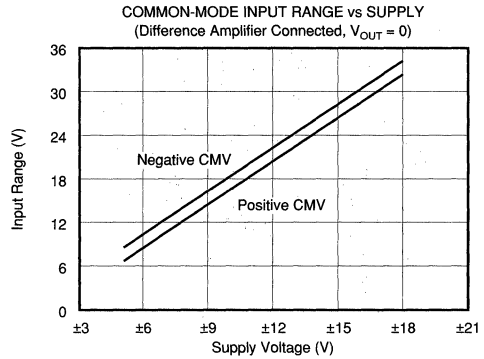
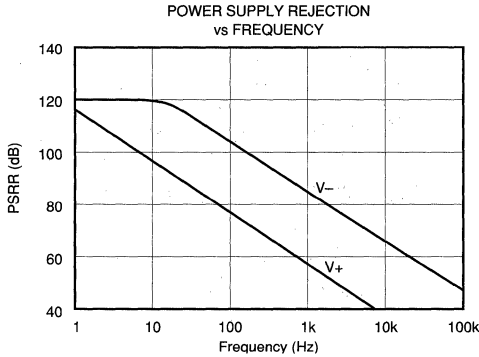
$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA105. Power supply bypass capacitors should be connected close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. The source impedances connected to the inputs must be nearly equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 80dB. If the source has a known mismatch in source impedance, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. This can be used to null offset voltage as shown in Figure 2. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins would not provide specified performance.

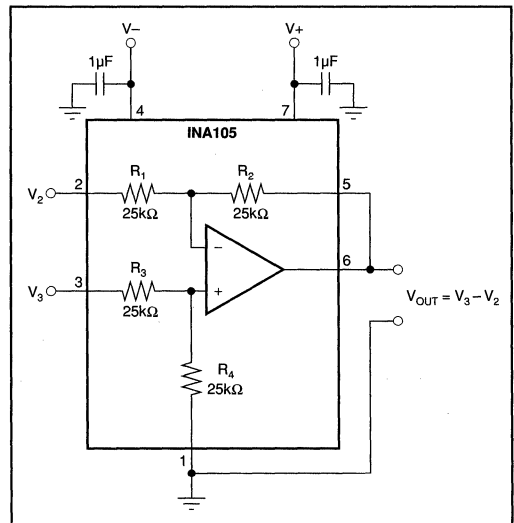


FIGURE 1. Basic Power Supply and Signal Connections.

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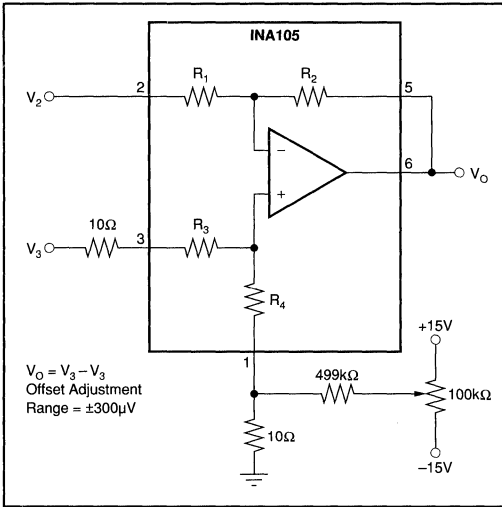


FIGURE 2. Offset Adjustment.

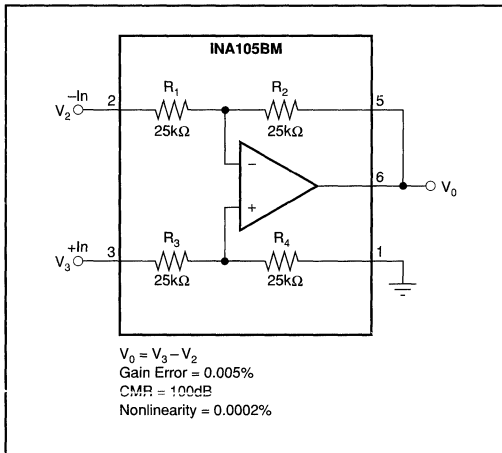


FIGURE 3. Precision Difference Amplifier.

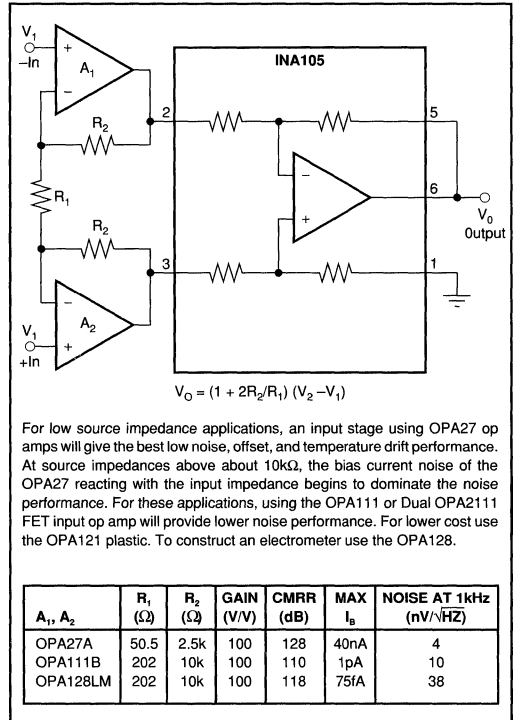


FIGURE 4. Precision Instrumentation Amplifier.

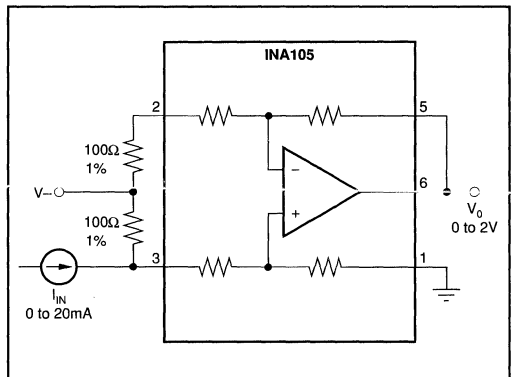


FIGURE 5. Current Receiver with Compliance to Rails.

INA105

4

INSTRUMENTATION AMPLIFIERS

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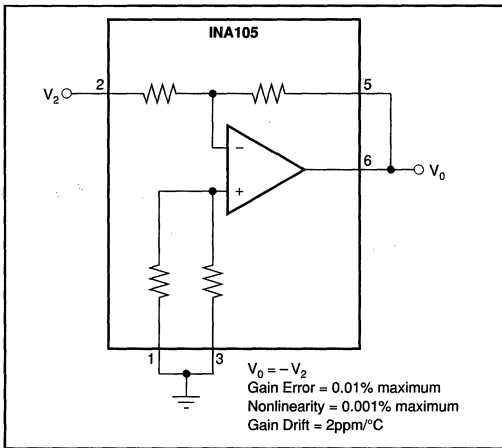


FIGURE 6. Precision Unity-Gain Inverting Amplifier.

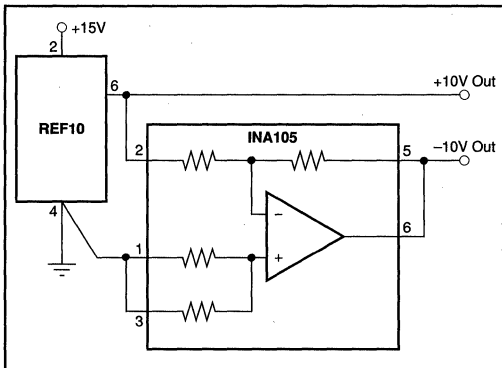


FIGURE 7. ±10V Precision Voltage Reference.

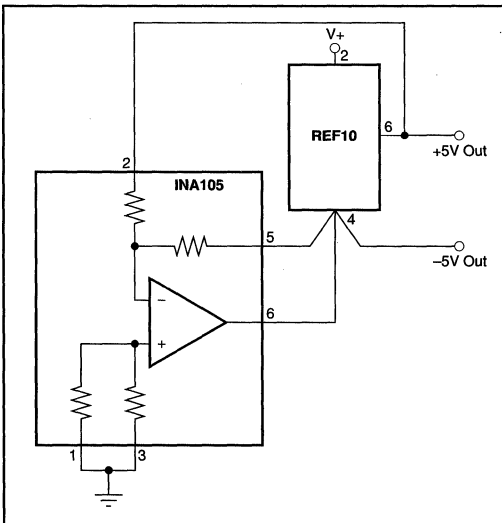


FIGURE 8. ±5V Precision Voltage Reference.

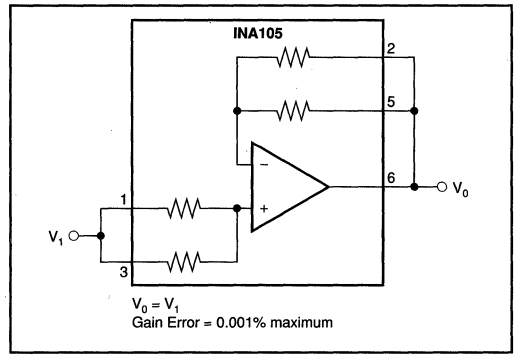


FIGURE 9. Precision Unity-Gain Buffer.

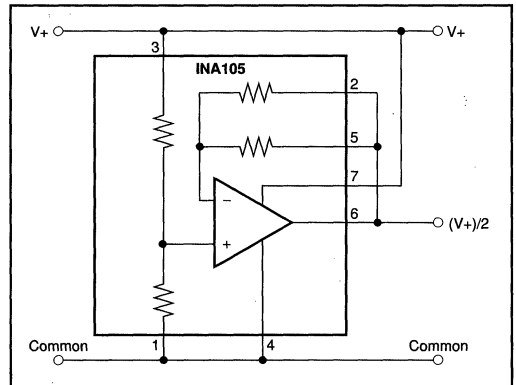


FIGURE 10. Pseudoground Generator.

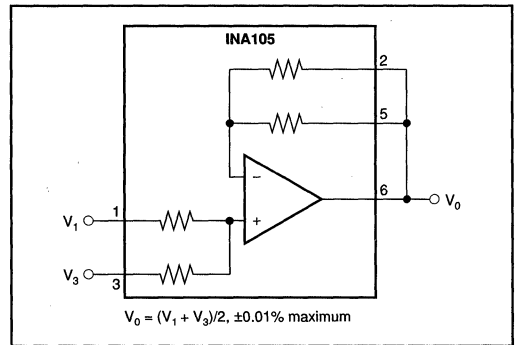


FIGURE 11. Precision Average Value Amplifier.

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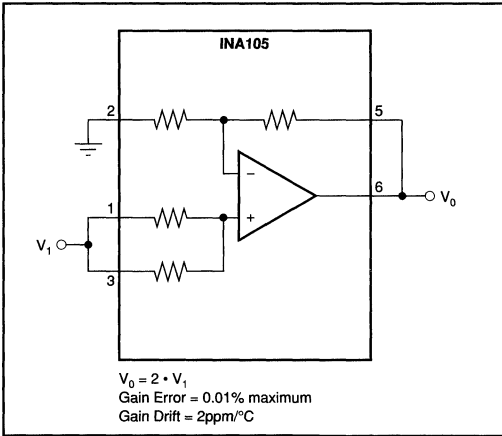


FIGURE 12. Precision (G = 2) Amplifier.

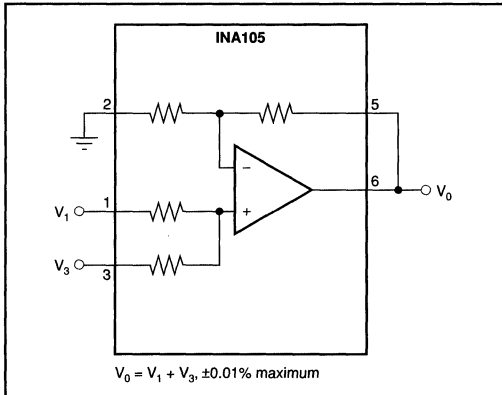


FIGURE 13. Precision Summing Amplifier.

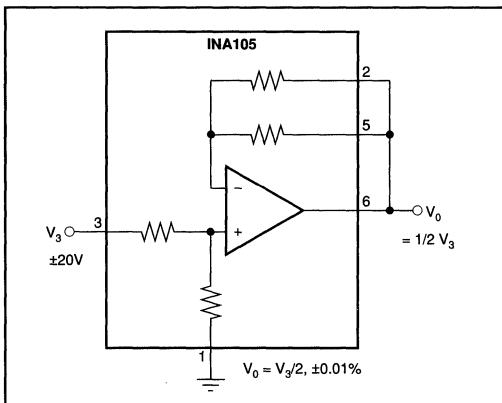


FIGURE 14. Precision Gain = 1/2 Amplifier.

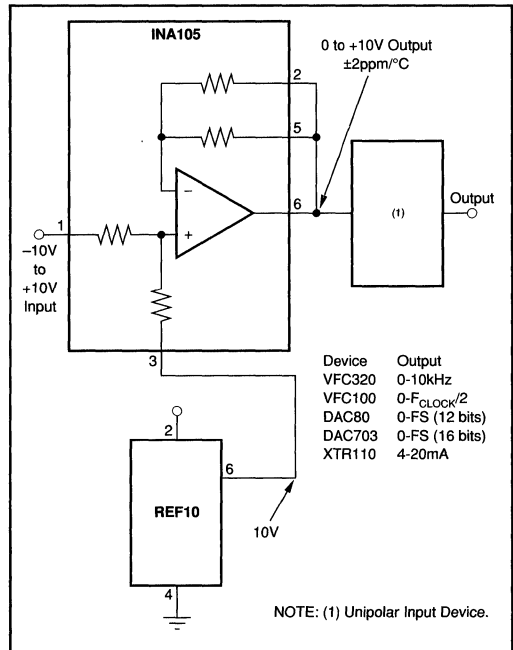


FIGURE 15. Precision Bipolar Offsetting.

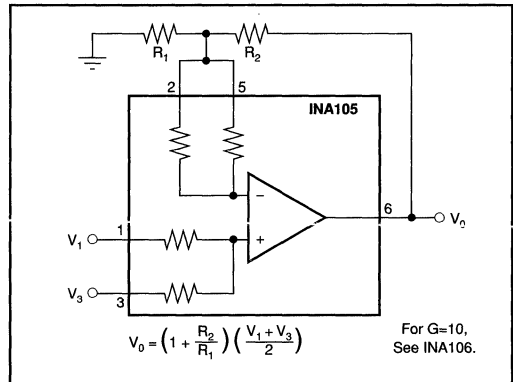


FIGURE 16. Precision Summing Amplifier with Gain.

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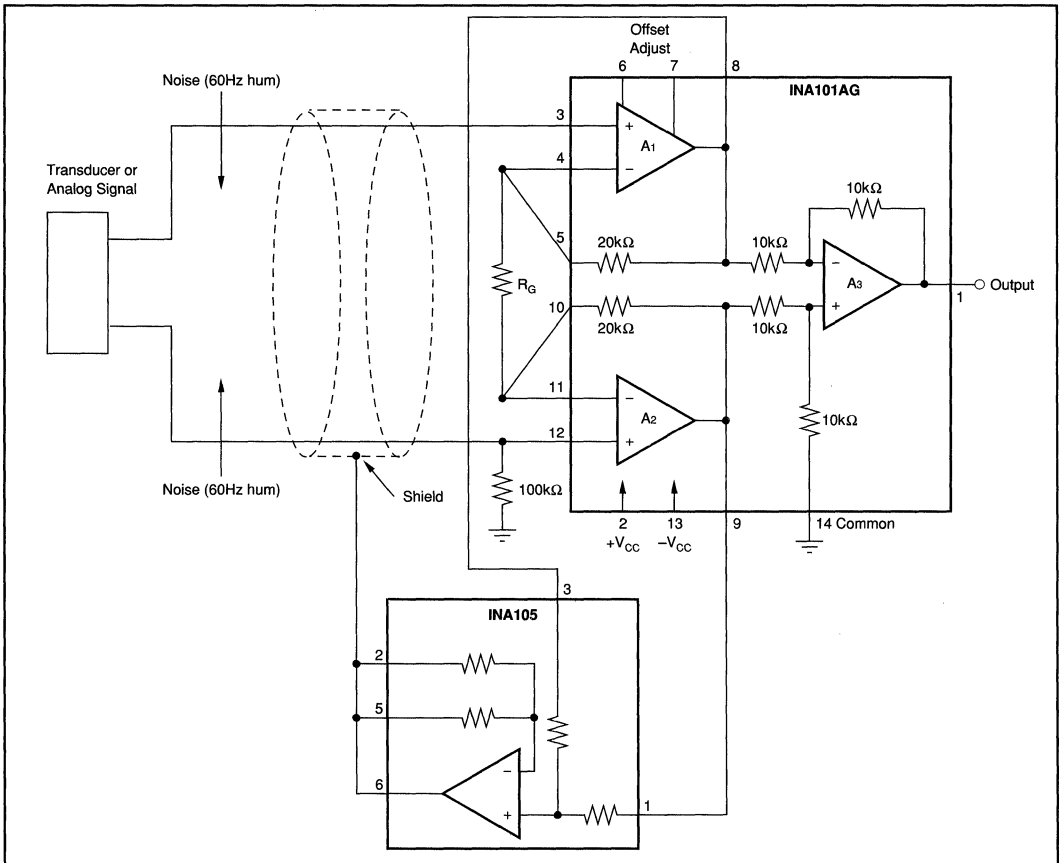


FIGURE 17. Instrumentation Amplifier Guard Drive Generator.

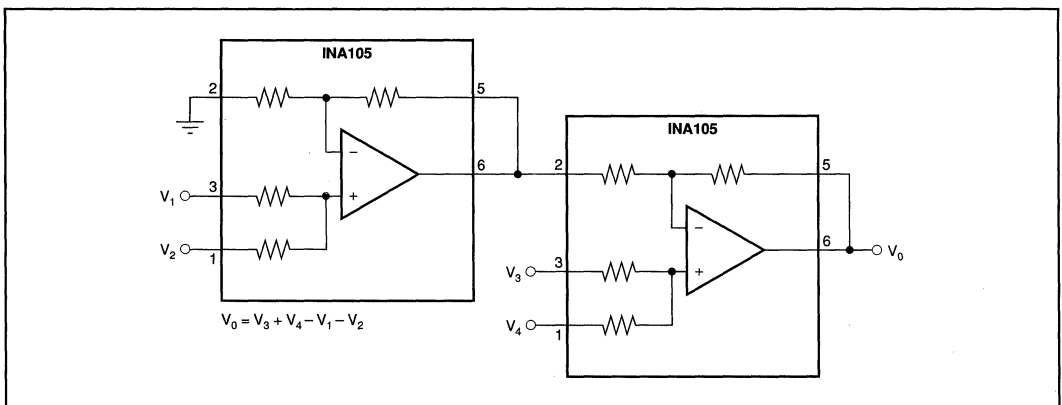


FIGURE 18. Precision Summing Instrumentation Amplifier.

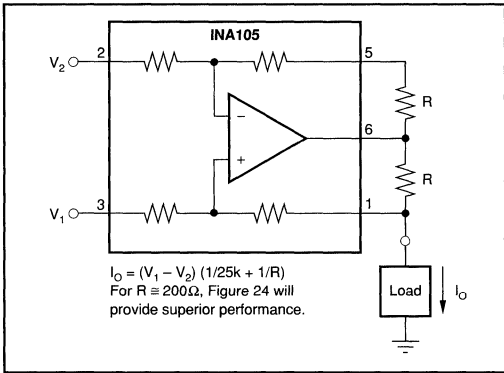


FIGURE 19. Precision Voltage-to-Current Converter with Differential Inputs.

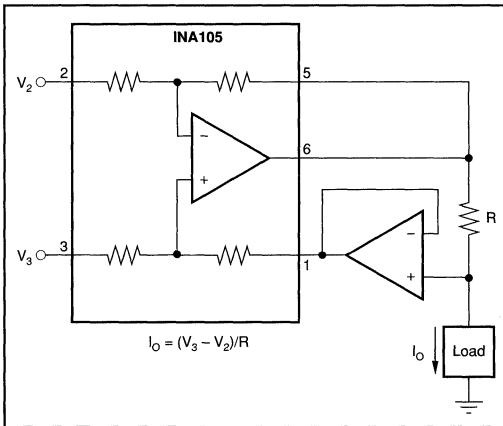


FIGURE 20. Differential Input Voltage-to-Current Converter for Low I_{OUT} .

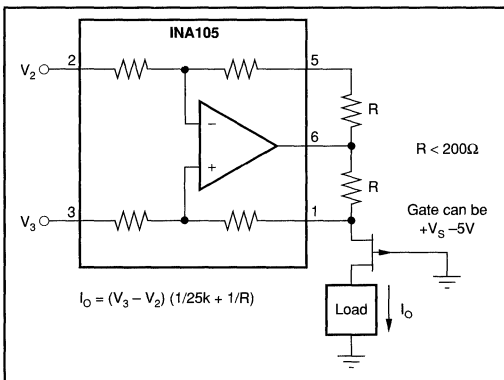


FIGURE 21. Isolating Current Source.

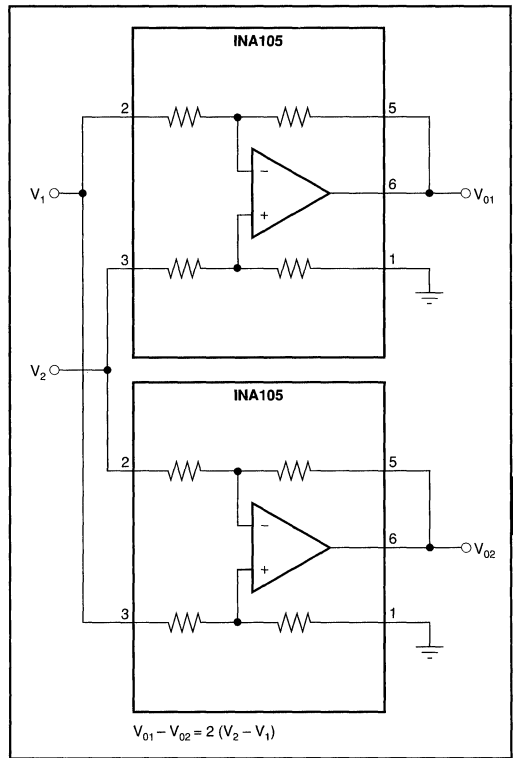


FIGURE 22. Differential Output Difference Amplifier.

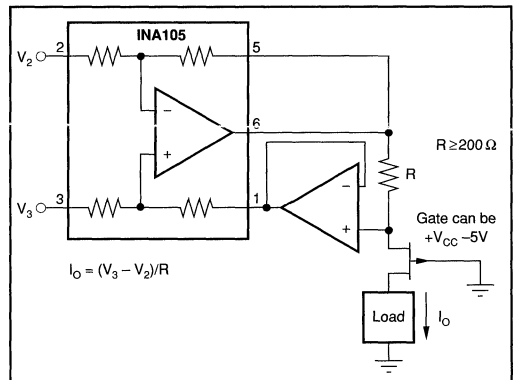


FIGURE 23. Isolating Current Source with Buffering Amplifier for Greater Accuracy.

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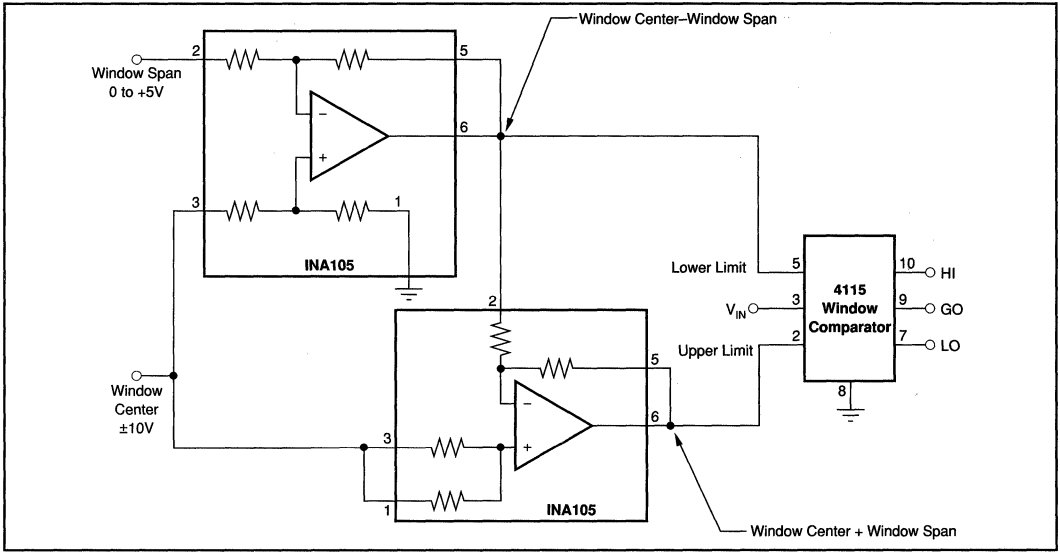


FIGURE 24. Window Comparator with Window Span and Window Center Inputs.

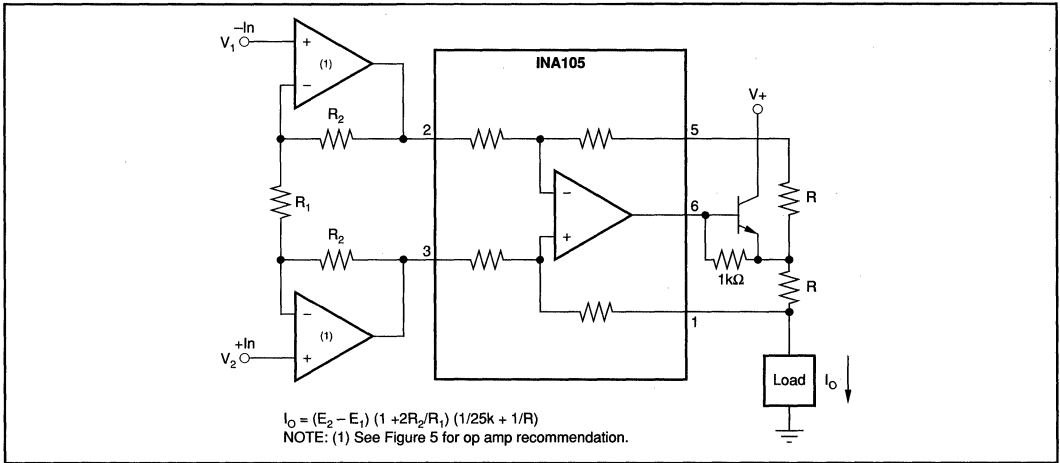


FIGURE 25. Precision Voltage-Controlled Current Source with Buffered Differential Inputs and Gain.

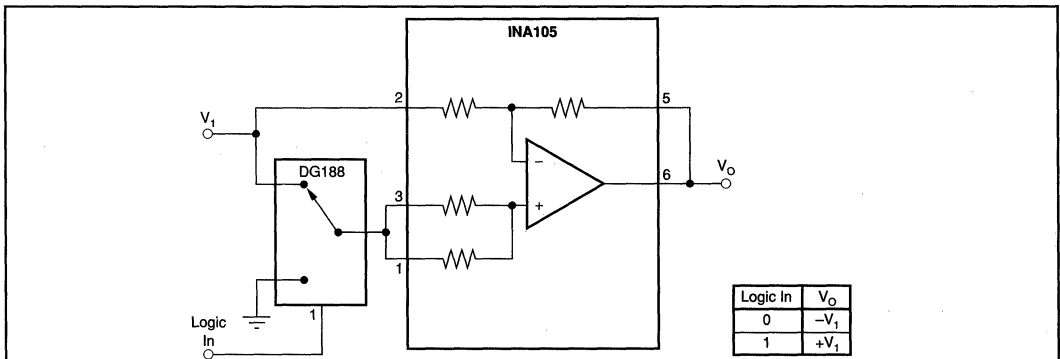


FIGURE 26. Digitally Controlled Gain of ±1 Amplifier.

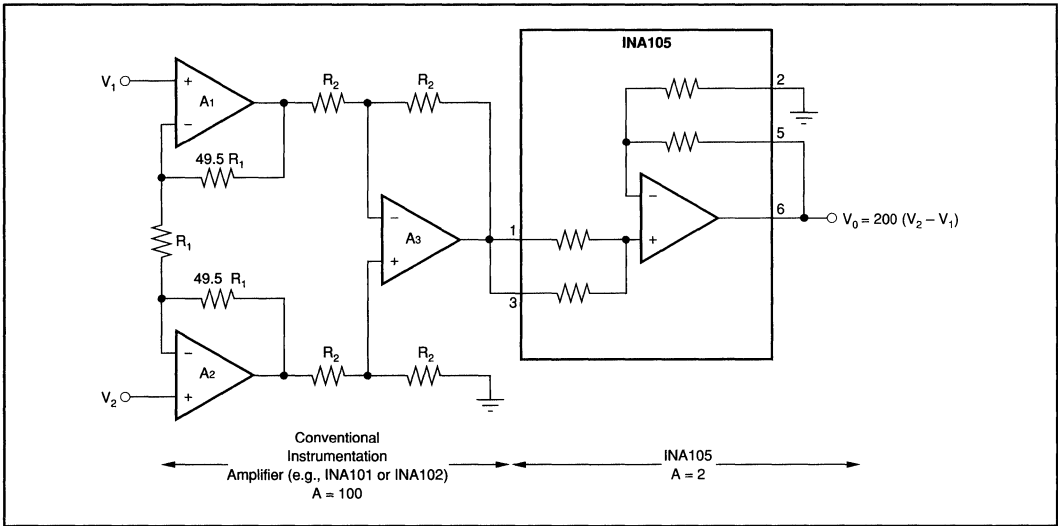


FIGURE 27. Boosting Instrumentation Amplifier Common-Mode Range From ± 5 to ± 7.5 V with 10V Full-Scale Output.

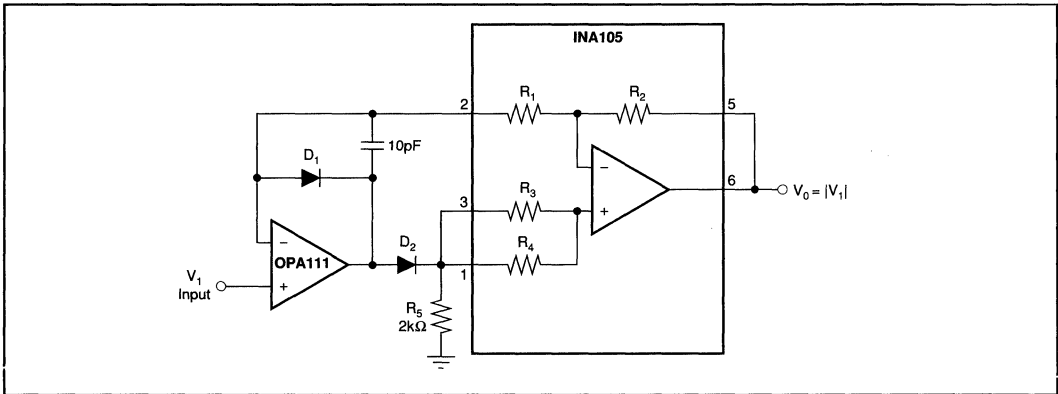


FIGURE 28. Precision Absolute Value Buffer.

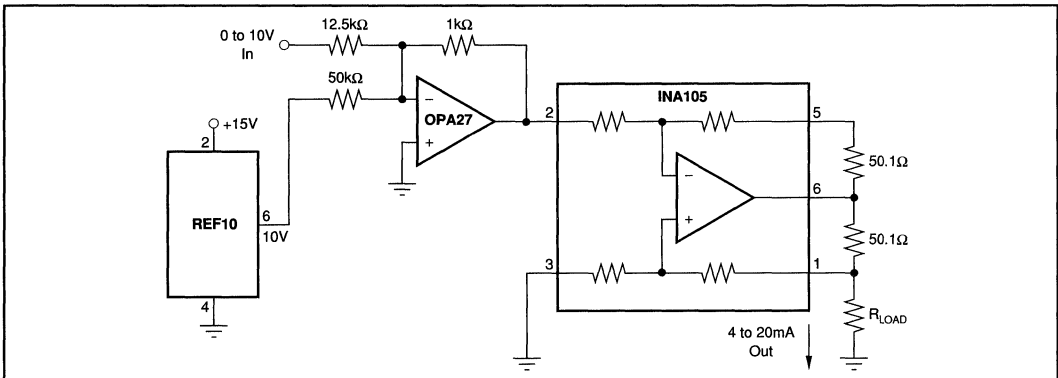
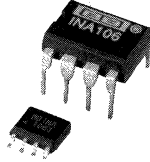


FIGURE 29. Precision 4-20mA Current Transmitter.

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INA106

Precision Gain=10 DIFFERENTIAL AMPLIFIER

FEATURES

- ACCURATE GAIN: $\pm 0.025\%$ max
- HIGH COMMON-MODE REJECTION: 86dB min
- NONLINEARITY: 0.001% max
- EASY TO USE
- PLASTIC 8-PIN DIP, SO-8 SOIC PACKAGES

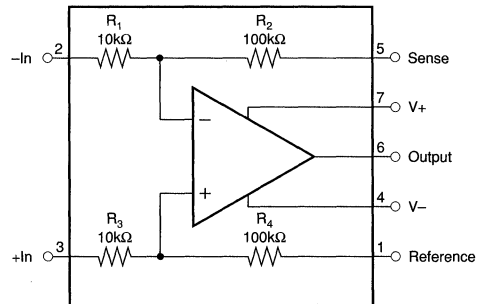
APPLICATIONS

- G=10 DIFFERENTIAL AMPLIFIER
- G=+10 AMPLIFIER
- G=-10 AMPLIFIER
- G=+11 AMPLIFIER
- INSTRUMENTATION AMPLIFIER

DESCRIPTION

The INA106 is a monolithic Gain=10 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA106 provides this precision circuit function without using an expensive resistor network. The INA106 is available in 8-pin plastic DIP and SO-8 surface-mount packages.



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SPECIFICATIONS

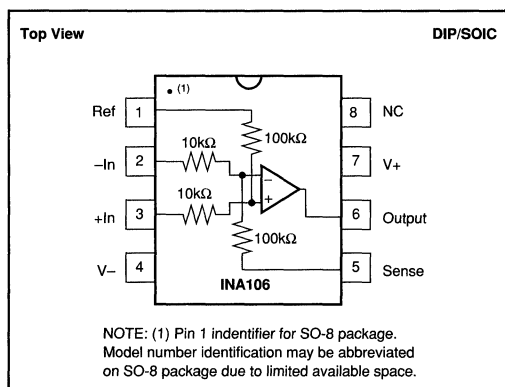
ELECTRICAL

At +25°C, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER	CONDITIONS	INA106KP, U			UNITS
		MIN	TYP	MAX	
GAIN Initial ⁽¹⁾ Error vs Temperature Nonlinearity ⁽²⁾			10 0.01 -4 0.0002		V/V % ppm/°C %
OUTPUT Related Voltage Rated Current Impedance Current Limit Capacitive Load	$I_O = +20mA, -5mA$ $V_O = 10V$ To Common Stable Operation	10 +20, -5	12 0.01 +40/-10 1000		V mA Ω mA pF
INPUT Impedance Voltage Range Common-Mode Rejection ⁽³⁾	Differential Common-mode Differential Common-mode $T_A = T_{MIN}$ to T_{MAX}		10 110 ± 1 ± 11 100		k Ω k Ω V V dB
OFFSET VOLTAGE Initial vs Temperature vs Supply vs Time	RTI ⁽⁴⁾ $\pm V_S = 6V$ to $18V$		50 0.2 1 10	200	μV $\mu V/^\circ C$ $\mu V/V$ $\mu V/mo$
NOISE VOLTAGE $f_b = 0.01Hz$ to $10Hz$ $f_o = 10kHz$	RTI ⁽⁵⁾		1 30		$\mu Vp-p$ nV/ \sqrt{Hz}
DYNAMIC RESPONSE Small Signal Full Power BW Slew Rate Settling Time: 0.1% 0.01% 0.01%	-3dB $V_O = 20Vp-p$ $V_O = 10V$ Step $V_O = 10V$ Step $V_{CM} = 10V$ Step, $V_{DIFF} = 0V$	30 2	5 50 3 5 10 5		MHz kHz V/ μs μs μs μs
POWER SUPPLY Rated Voltage Range Quiescent Current	Derated Performance $V_O = 0V$	± 5	5 ± 1.5	± 18 ± 2	V V mA
TEMPERATURE RANGE Specification Operation Storage		0 -40 -65		+70 +85 +150	°C °C °C

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see "Maintaining CMR" section). (4) Includes effects of amplifiers's input bias and offset currents. (5) Includes effect of amplifier's input current noise and thermal noise contribution of resistor network.

PIN CONFIGURATION



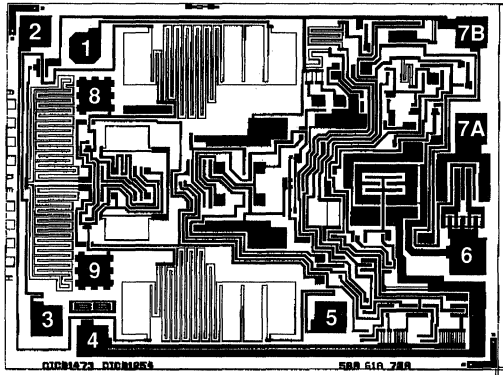
ELECTROSTATIC DISCHARGE SENSITIVITY

This integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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DICE INFORMATION



INA106 DIE TOPOGRAPHY

PAD	FUNCTION
1	Reference
2	-In
3	+In
4	V-
5	Sense
6	Output
7A, 7B	V+ (Connect Both)
8	(Op Amp +In)
9	(Op Amp -In)

Substrate Bias: Electrically connected to V- supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	83 x 63 ±5	2.11 x 1.60 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing:	Gold	

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage Range	±V _S
Operating Temperature Range: P, U	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering, 10s): P	+300°C
Wave Soldering (3s, max) U	+260°C
Output Short Circuit to Common	Continuous

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA106KP	8-Pin Plastic DIP	0°C to +70°C
INA106U	SO-8 Surface Mount	0°C to +70°C

PACKAGING INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA106KP	8-Pin Plastic DIP	006
INA106U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

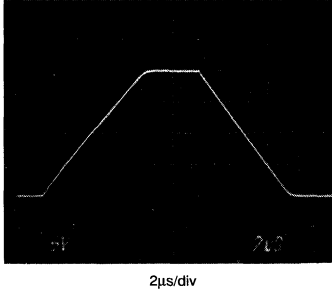
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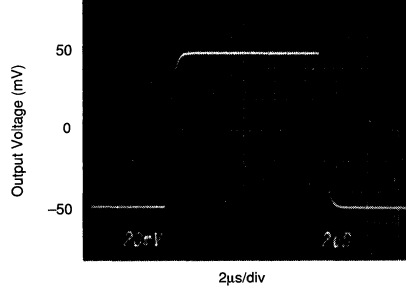
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

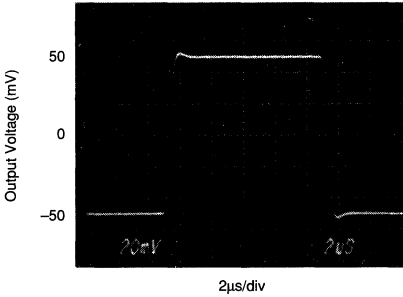
STEP RESPONSE



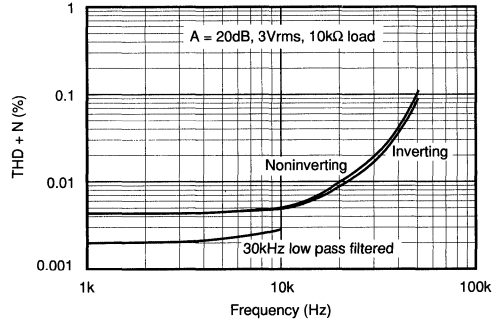
SMALL SIGNAL RESPONSE
(No Load)



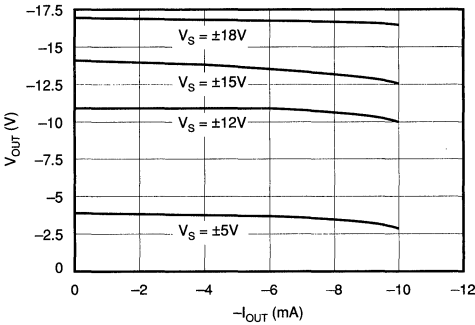
SMALL SIGNAL RESPONSE
($R_{LOAD} = \infty$, $C_{LOAD} = 100\text{pF}$)



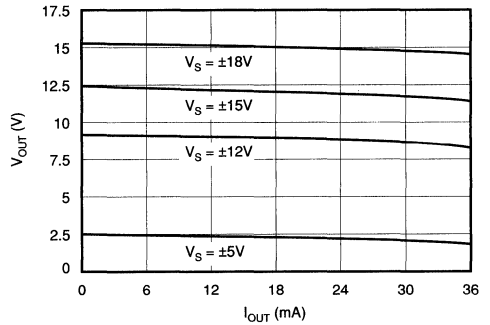
TOTAL HARMONIC DISTORTION AND NOISE
vs FREQUENCY



MAXIMUM V_{OUT} vs I_{OUT}
(Negative Swing)



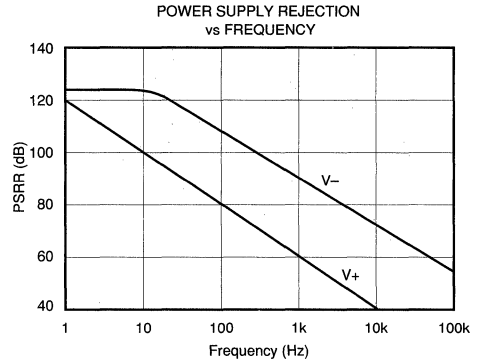
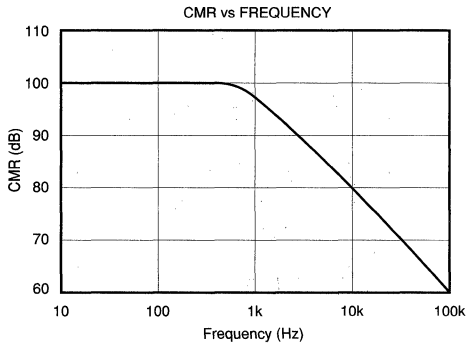
MAXIMUM V_{OUT} vs I_{OUT}
(Positive Swing)



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA106. Power supply bypass capacitors should be connected close to the device pins as shown.

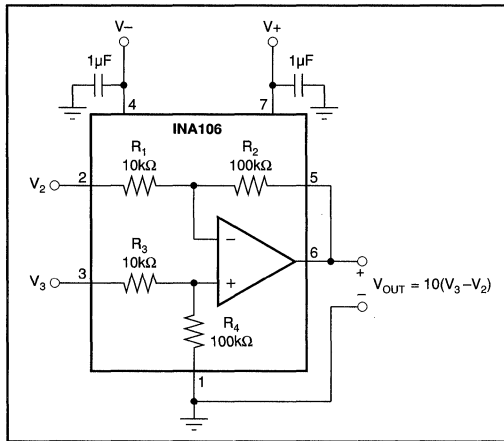


FIGURE 1. Basic Power Supply and Signal Connections.

The differential input signal is connected to pins 2 and 3 as shown. The source impedance connected to the inputs must be equal to assure good common-mode rejection. A 5Ω mismatch in source impedance will degrade the common-mode rejection of a typical device to approximately 86dB. If the source has a known source impedance mismatch, an additional resistor in series with one input can be used to preserve good common-mode rejection.

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal will be summed with the output signal. The source impedance of a signal applied to the Ref terminal should be less than 10Ω to maintain good common-mode rejection.

Figure 2 shows a voltage applied to pin 1 to trim the offset voltage of the INA106. The known 100Ω source impedance of the trim circuit is compensated by the 10Ω resistor in series with pin 3 to maintain good CMR.

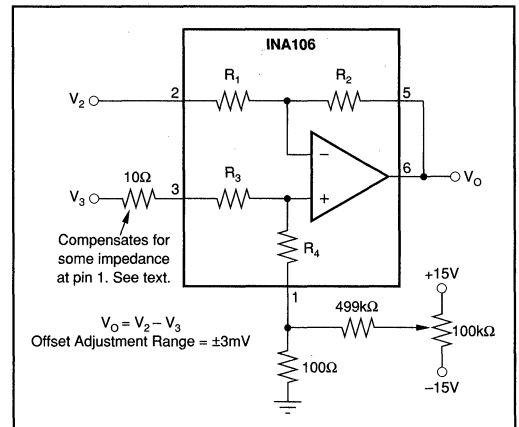


FIGURE 2. Offset Adjustment.

Referring to Figure 1, the CMR depends upon the match of the internal R_4/R_3 ratio to the R_1/R_2 ratio. A CMR of 106dB requires resistor matching of 0.005%. To maintain high CMR over temperature, the resistor TCR tracking must be better than 2ppm/°C. These accuracies are difficult and expensive to reliably achieve with discrete components.

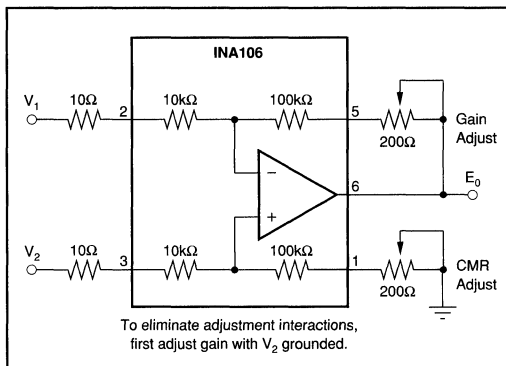


FIGURE 3. Difference Amplifier with Gain and CMR Adjust.

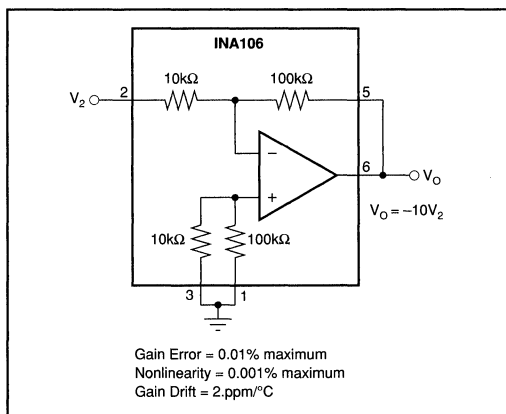


FIGURE 4. Precision $G = -10$ Inverting Amplifier.

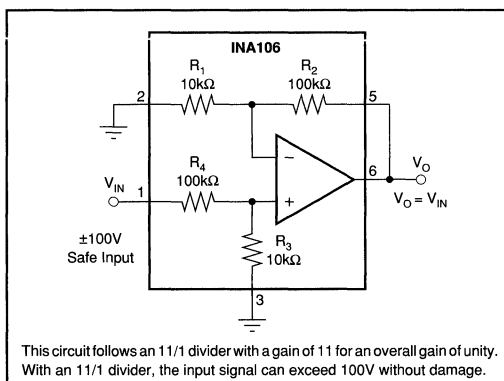
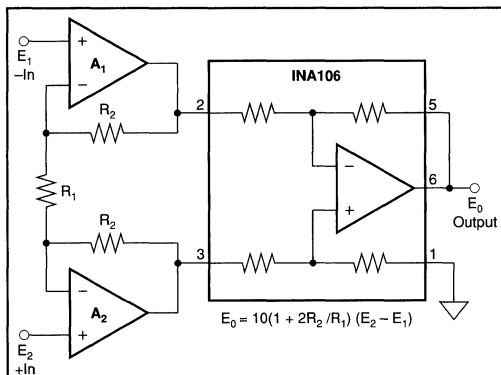


FIGURE 5. Voltage Follower with Input Protection.



To make a high performance high gain instrumentation amplifier, the INA106 can be combined with state-of-the-art op amps. For low source impedance applications, OPA37s will give the best noise, offset, and temperature drift. At source impedances above about 10kΩ, the bias current noise of the OPA37 reacting with input impedance degrades noise. For these applications, use an OPA111 or a dual OPA2111 FET input op amp for lower noise. For an electrometer grade IA, use the OPA128—see table below.

Using the INA106 for the difference amplifier also extends the input common-mode range of the instrumentation amplifier to $\pm 10V$. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to $\pm 5V$ for an output swing of $\pm 10V$. This is because a unity-gain difference amp needs $\pm 5V$ at the input for 10V at the output, allowing only 5V additional for common-mode.

A_1, A_2	R_1 (Ω)	R_2 (k Ω)	GAIN (V/V)	CMRR (dB)	I_b (pA)	NOISE AT 1kHz (nV/ \sqrt{Hz})
OPA37A	50.5	2.5	1000	128	40000	4
OPA111B	202	10	1000	110	1	10
OPA128LM	202	10	1000	118	0.075	38

FIGURE 6. Precision Instrumentation Amplifier.

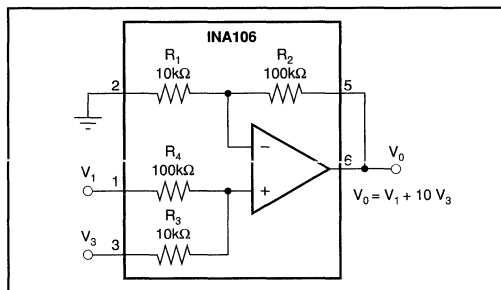


FIGURE 7. Precision Summing Amplifier.

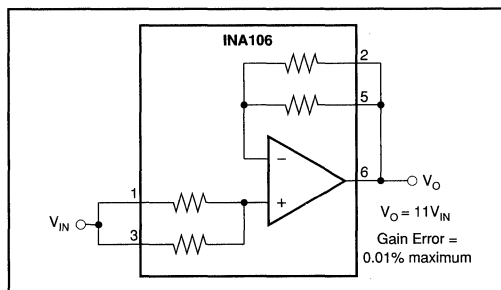
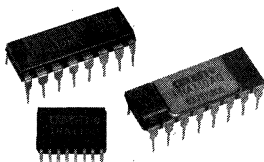


FIGURE 8. Precision $G = 11$ Buffer.

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INA110

Fast-Settling FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4 μ s to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY-LOW GAIN DRIFT: 10 to 50ppm/ $^{\circ}$ C
- LOW OFFSET DRIFT: 2 μ V/ $^{\circ}$ C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

APPLICATIONS

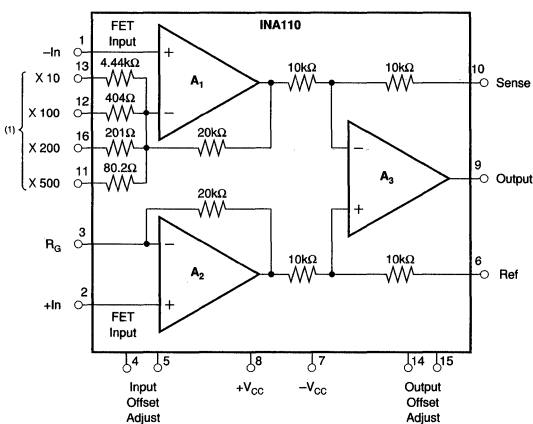
- MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
- FAST DIFFERENTIAL PULSE AMPLIFIER
- HIGH SPEED GAIN BLOCK
- AMPLIFICATION OF HIGH IMPEDANCE SOURCES

DESCRIPTION

The INA110 is a versatile monolithic FET-input instrumentation amplifier. Its current-feedback circuit topology and laser trimmed input stage provide excellent dynamic performance and accuracy. The INA110 settles in 4 μ s to 0.01%, making it ideal for high speed or multiplexed-input data acquisition systems.

Internal gain-set resistors are provided for gains of 1, 10, 100, 200 and 500V/V. Inputs are protected for differential and common-mode voltages up to $\pm V_{CC}$. Its very high input impedance and low input bias current make the INA110 ideal for applications requiring input filters or input protection circuitry.

The INA110 is available in 16-pin plastic and ceramic DIPs, and in the SOL-16 surface-mount package. Military, industrial and commercial temperature range grades are available.



NOTE: (1) Connect to R_G for desired gain.

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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC} = 15VDC$, $R_L = 2k\Omega$, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Range of Gain		1	*	800	*	*	*	*	*	*	V/V
Gain Equation ⁽¹⁾					$G = 1 + [40k/(R_G + 50\Omega)]$						V/V
Gain Error, DC: G = 1			0.002	0.04			0.02	*	*	*	%
G = 10			0.01	0.1		0.005	0.05	*	*	*	%
G = 100			0.02	0.2		0.01	0.1	*	*	*	%
G = 200			0.04	0.4		0.02	0.2	*	*	*	%
G = 500			0.1	1		0.05	0.5	*	*	*	%
Gain Temp. Coefficient: G = 1			± 3	± 20		*	± 10	*	*	*	ppm/°C
G = 10			± 4	± 20		± 2	± 10	*	*	*	ppm/°C
G = 100			± 6	± 40		± 3	± 20	*	*	*	ppm/°C
G = 200			± 10	± 60		± 5	± 30	*	*	*	ppm/°C
G = 500			± 25	± 100		± 10	± 50	*	*	*	ppm/°C
Nonlinearity, DC: G = 1			± 0.001	± 0.01		± 0.0005	± 0.005	*	*	*	% of FS
G = 10			± 0.002	± 0.01		± 0.001	± 0.005	*	*	*	% of FS
G = 100			± 0.004	± 0.02		± 0.002	± 0.01	*	*	*	% of FS
G = 200			± 0.006	± 0.02		± 0.003	± 0.01	*	*	*	% of FS
G = 500			± 0.01	± 0.04		± 0.005	± 0.02	*	*	*	% of FS
OUTPUT											
Voltage, $R_L = 2k\Omega$	Over Temperature	± 10	± 12.7		*	*		*	*	*	V
Current	Over Temperature	± 5	± 25		*	*		*	*	*	mA
Short-Circuit Current			± 25			*		*	*	*	mA
Capacitive Load	Stability		5000			*		*	*	*	pF
INPUT OFFSET VOLTAGE⁽²⁾											
Initial Offset: G, P			$\pm(100 + 1000/G)$	$\pm(500 + 5000/G)$		$\pm(50 + 600/G)$	$\pm(250 + 3000/G)$	*	*	*	μV
U								$\pm(200 + 2000/G)$	$\pm(1000 + 5000/G)$	*	μV
vs Temperature			$\pm(2 + 20/G)$	$\pm(5 + 100/G)$		$\pm(1 + 10/G)$	$\pm(2 + 50/G)$	*	*	*	$\mu V/°C$
vs Supply	$V_{CC} = \pm 6V$ to $\pm 18V$		$\pm(4 + 60/G)$	$\pm(30 + 300/G)$		$\pm(2 + 30/G)$	$\pm(10 + 180/G)$	*	*	*	$\mu V/V$
BIAS CURRENT											
Initial Bias Current	Each Input		20	100		10	50	*	*	*	pA
Initial Offset Current			2	50		1	25	*	*	*	pA
Impedance: Differential			$5 \times 10^{12} 6$			*		*	*	*	ΩpF
Common-Mode			$2 \times 10^{12} 1$			*		*	*	*	ΩpF
VOLTAGE RANGE											
Range, Linear Response	V_{in} Diff. = $0V^{(3)}$	± 10	± 12					*	*	*	V
CMR with $1k\Omega$ Source Imbalance:								*	*	*	dB
G = 1	DC	70	90		80	100		*	*	*	dB
G = 10	DC	67	104		90	112		*	*	*	dB
G = 100	DC	100	110		106	116		*	*	*	dB
G = 200	DC	100	110		106	116		*	*	*	dB
G = 500	DC	100	110		106	116		*	*	*	dB
INPUT NOISE⁽⁴⁾											
Voltage, $f_c = 10kHz$			10			*		*	*	*	nV/\sqrt{Hz}
$f_b = 0.1Hz$ to $10Hz$			1			*		*	*	*	$\mu Vp-p$
Current, $f_c = 10kHz$			1.8			*		*	*	*	fA/\sqrt{Hz}
OUTPUT NOISE⁽⁴⁾											
Voltage, $f_c = 10kHz$			65			*		*	*	*	nV/\sqrt{Hz}
$f_b = 0.1Hz$ to $10Hz$			8			*		*	*	*	$\mu Vp-p$
DYNAMIC RESPONSE											
Small Signal: G = 1	-3dB		2.5			*		*	*	*	MHz
G = 10			2.5			*		*	*	*	MHz
G = 100			470			*		*	*	*	kHz
G = 200			240			*		*	*	*	kHz
G = 500			100			*		*	*	*	kHz
Full Power	$V_{OUT} = \pm 10V$, G = 2 to 100				*	*		*	*	*	kHz
Slew Rate	G = 2 to 100	190	270		*	*		*	*	*	kHz
Settling Time:		12	17		*	*		*	*	*	$V/\mu s$
0.1%, G = 1	$V_O = 20V$ Step		4			*		*	*	*	μs
G = 10			2			*		*	*	*	μs
G = 100			3			*		*	*	*	μs
G = 200			5			*		*	*	*	μs
G = 500			11			*		*	*	*	μs

INSTRUMENTATION AMPLIFIERS 4 INA110

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SPECIFICATIONS (CONT)

ELECTRICAL

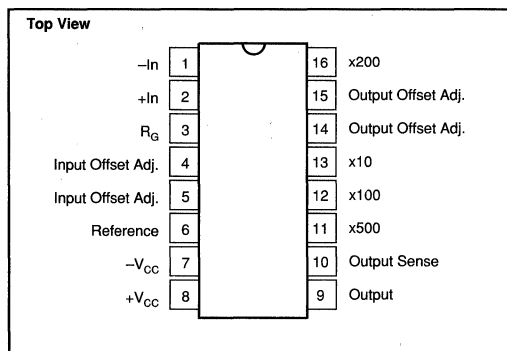
At +25°C, $\pm V_{CC}$ 15VDC, $R_L = 2K\Omega$, unless otherwise specified.

PARAMETER	CONDITIONS	INA110AG			INA110BG, SG			INA110KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time: 0.01%, G = 1	$V_O = 20V$ Step		5	12.5		*	*		*		μs
G = 10			3	7.5		*	*		*		μs
G = 100			4	7.5		*	*		*		μs
G = 200			7	12.5		*	*		*		μs
G = 500			16	25		*	*		*		μs
Recovery ⁽⁵⁾	50% Overdrive		1			*			*		μs
POWER SUPPLY											
Rated Voltage	$V_O = 0V$		± 15		*	*		*	*		V
Voltage Range		± 6		± 18							V
Quiescent Current			± 3		± 4.5		*		*		mA
TEMPERATURE RANGE											
Specification: A, B, K S		-25		+85	*		*	0		+70	°C
Operation					-55		+125				°C
Storage		-55		+125	*		*	-25		+85	°C
θ_{JA}		-65		+150	*		*	-40		+85	°C
			100			*			*		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G , between pin 3 and pins 11, 12 and 16. Gain accuracy is a function of R_O and the internal resistors which have a $\pm 20\%$ tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE RTI} = \sqrt{V_{N, INPUT}^2 + (V_{N, OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Input Voltage Range	$\pm V_{CC}$
Operating Temperature Range: G	-55°C to +125°C
P, U	-25°C to +85°C
Storage Temperature Range: G	-65°C to +150°C
P, U	-40°C to +85°C
Lead Temperature (soldering, 10s): G, P	+300°C
(soldering, 3s): U	+260°C
Output Short Circuit Duration	Continuous to Common

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA110AG	16-Pin Ceramic DIP	109
INA110BG	16-Pin Ceramic DIP	109
INA110SG	16-Pin Ceramic DIP	109
INA110KP	16-Pin Plastic DIP	180
INA110KU	SOL-16 SOIC	211

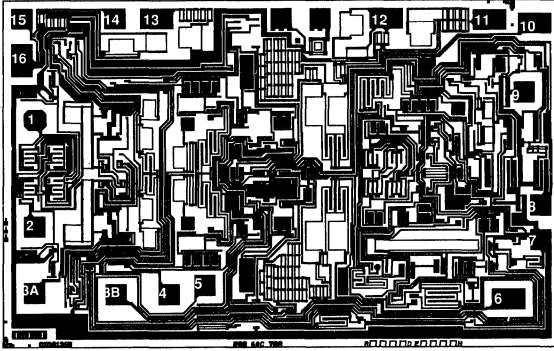
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA110AG	16-Pin Ceramic DIP	-25°C to +85°C
INA110BG	16-Pin Ceramic DIP	-25°C to +85°C
INA110SG	16-Pin Ceramic DIP	-55°C to +125°C
INA110KP	16-Pin Plastic DIP	0°C to +70°C
INA110KU	SOL-16 SOIC	0°C to +70°C

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DICE INFORMATION



INA110 DIE TOPOGRAPHY

PAD	FUNCTION
1	-In
2	+In
3A,3B	R_G (connect both)
4	Input Offset Adjust
5	Input Offset Adjust
6	Reference
7	$-V_{CC}$
8	$+V_{CC}$
9	Output
10	Output Sense
11	x500
12	x100
13	x10
14	Output Offset Adjust
15	Output Offset Adjust
16	x200

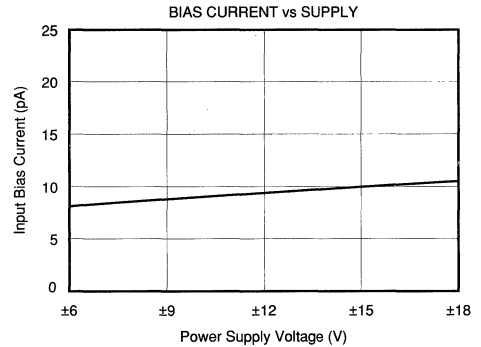
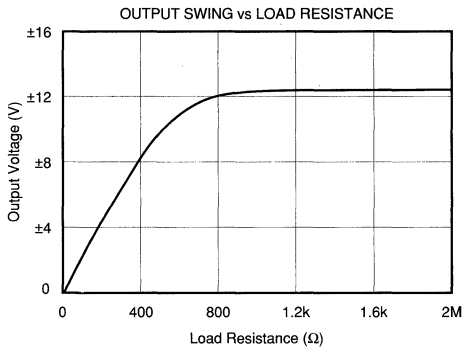
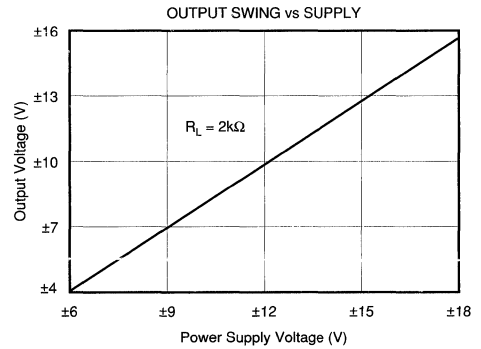
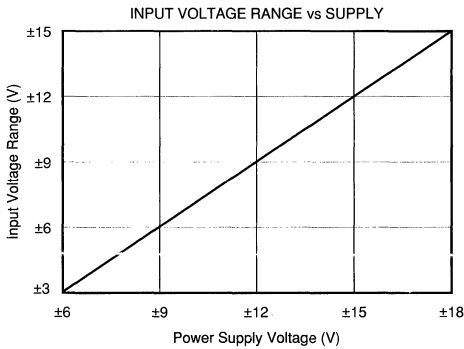
Pads 3A and 3B must be connected.
Substrate Bias: Internally connected to $-V_{CC}$ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	139 x 89 ±5	3.53 x 2.26 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

TYPICAL PERFORMANCE CURVES

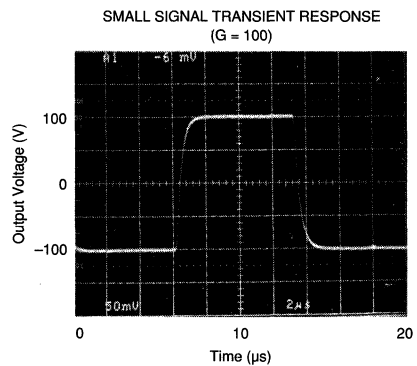
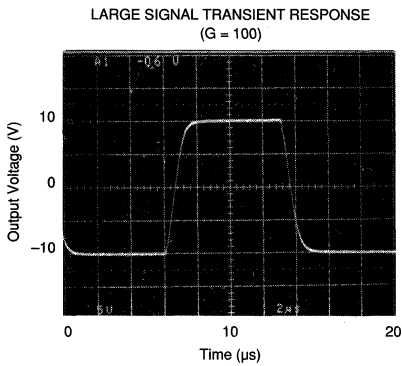
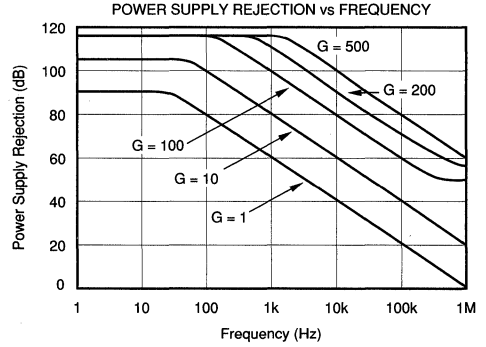
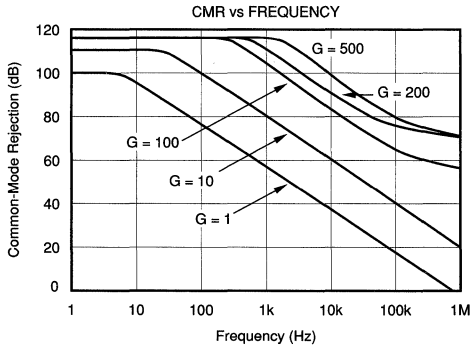
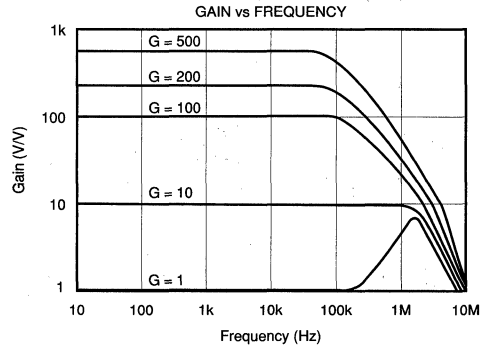
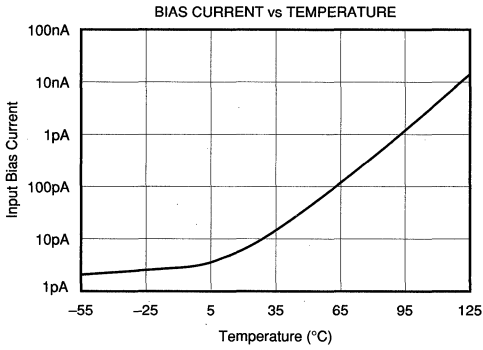
$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise noted.

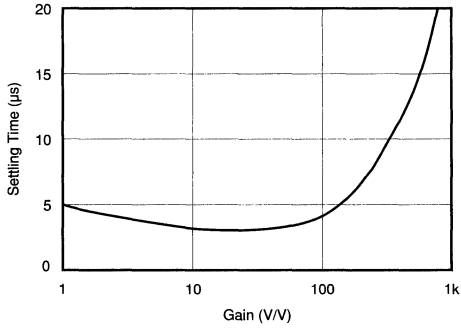


Or, Call Customer Service at 1-800-548-6132 (USA Only)

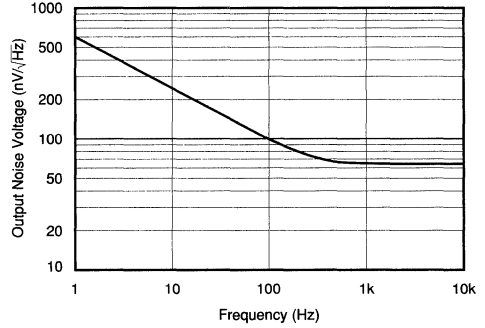
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise noted.

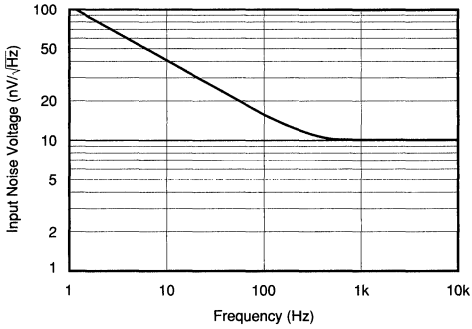
SETTLING TIME vs GAIN
(0.01%, 20V Step)



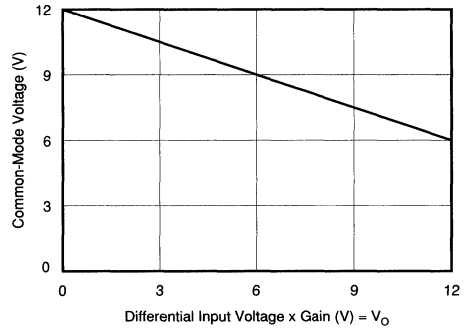
OUTPUT NOISE VOLTAGE vs FREQUENCY



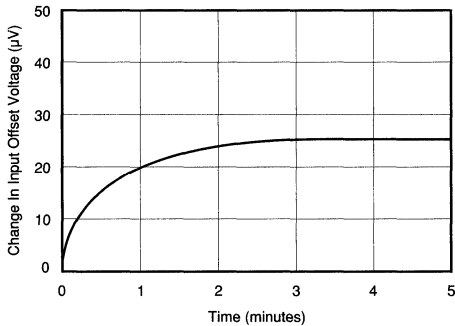
INPUT NOISE VOLTAGE vs FREQUENCY



COMMON-MODE VOLTAGE vs
DIFFERENTIAL INPUT VOLTAGE



WARM-UP DRIFT vs TIME



INA110

4

INSTRUMENTATION AMPLIFIERS

DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration using current-feedback type op amps with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10k Ω resistors, especially over temperature and time, assures high common-mode rejection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1 μ F tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. To maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

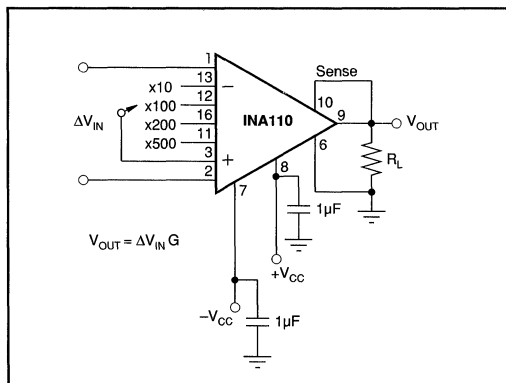


FIGURE 1. Basic Circuit Connection.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by the gain of the input stage. This allows specification of offset independent of gain.

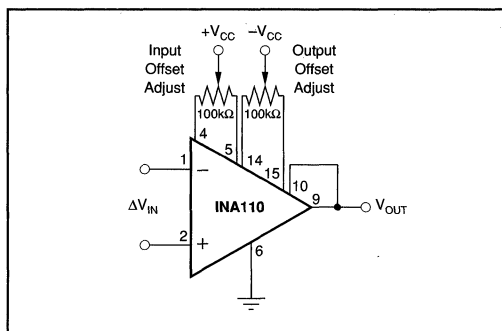


FIGURE 2. Offset Adjustment Circuit.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications, the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33 μ V/ $^{\circ}$ C per 100 μ V of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 3 by applying a voltage to the reference (pin 6) through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

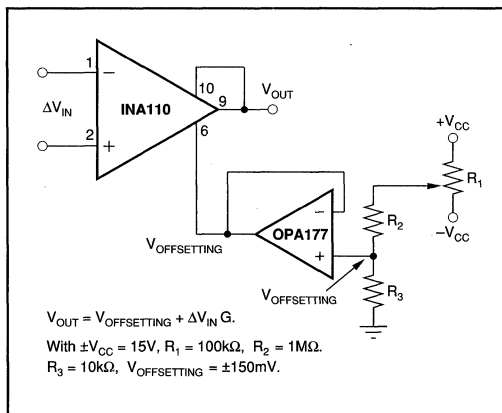


FIGURE 3. Output Offsetting.

GAIN SELECTION

Gain selection is accomplished by connecting the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

GAIN	CONNECT PIN 3 TO PIN	GAIN ACCURACY (%)	GAIN DRIFT (ppm/°C)
The following gains have guaranteed accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12, 16	0.25	10
600	11, 12	0.25	40
700	11, 16	2	40
800	11, 12, 16	2	80

TABLE I. Internal Gain Connections.

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G , between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a $\pm 20\%$ tolerance with $20\text{ppm}/^\circ\text{C}$ drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G-1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 4. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

OUTPUT STAGE GAIN	R_1 AND R_3	R_2
2	1.2k Ω	2.74k Ω
5	1k Ω	511 Ω
10	1.5k Ω	340 Ω

TABLE II. Output Stage Gain Control.

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately $\pm 10\text{V}$ with $\pm 15\text{V}$ supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 4).

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents that

are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 5. Buffer errors are minimized by the loop gain of the output amplifier.

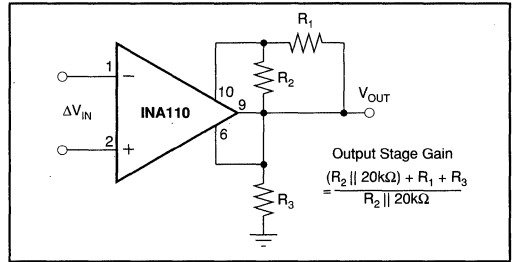


FIGURE 4. Gain Adjustment of Output Stage Using H Pad Attenuator.

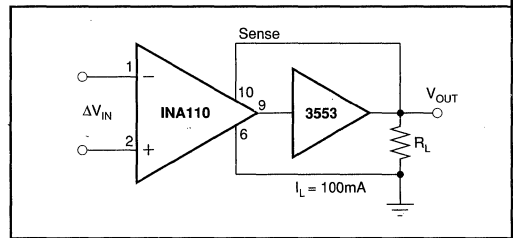


FIGURE 5. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise, the output can wander and saturate. A $1\text{M}\Omega$ to $10\text{M}\Omega$ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins.

Applications with balanced-source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the

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negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the circuit stability. If the impedance in the positive input is greater, the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback depends upon source impedance imbalance, operating gain, and board layout. The addition of a small bypass capacitor of 5pF to 50pF directly between the inputs of the IA will generally eliminate any positive feedback. CMR errors due to the input impedance mismatch will also be reduced by the capacitor.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit significant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response. CMR is not affected by the addition of the 400kHz RC in a gain of 1.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 6 through 19 show application circuits.

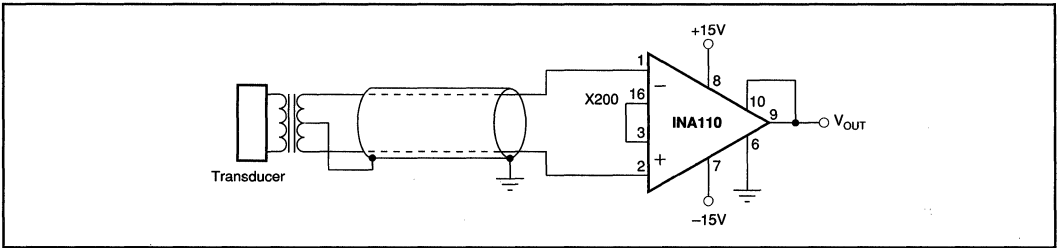


FIGURE 6. Transformer-Coupled Amplifier.

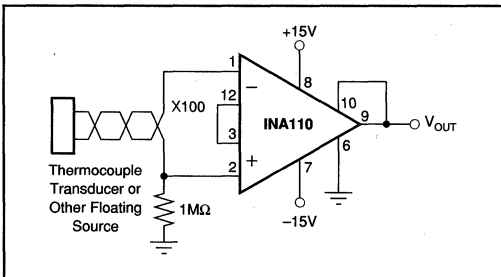


FIGURE 7. Floating Source Instrumentation Amplifier.

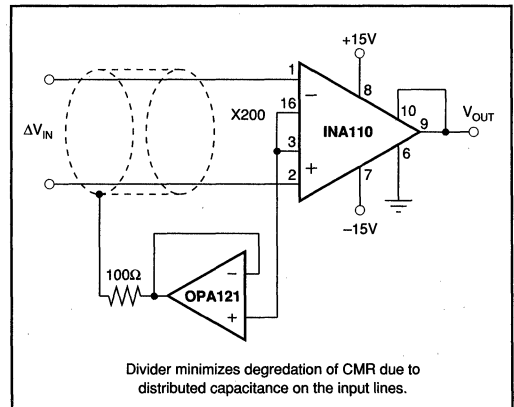


FIGURE 8. Instrumentation Amplifier with Shield Driver.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

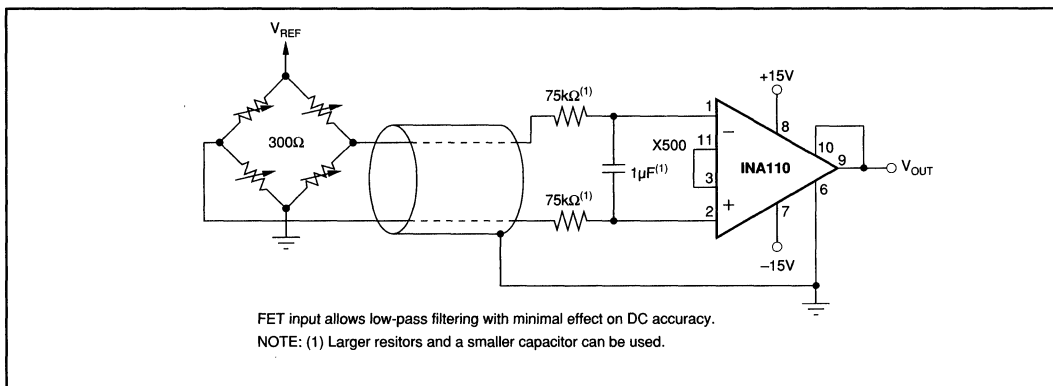


FIGURE 9. Bridge Amplifier with 1Hz Low-Pass Input Filter.

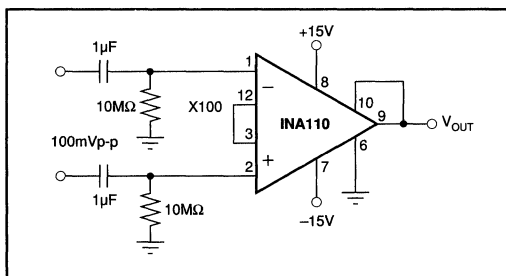


FIGURE 10. AC-Coupled Differential Amplifier for Frequencies Greater Than 0.016Hz.

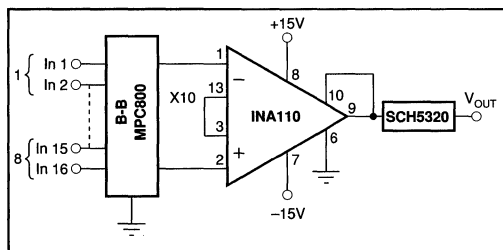


FIGURE 12. Rapid-Scanning-Rate Data Acquisition Channel with 5μs Settling to 0.01%.

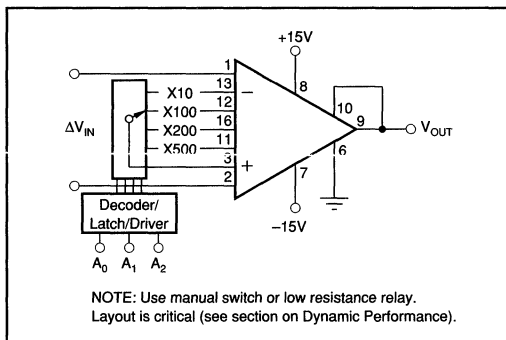


FIGURE 11. Programmable-Gain Instrumentation Amplifier (Precision Noninverting or Inverting Buffer with Gain).

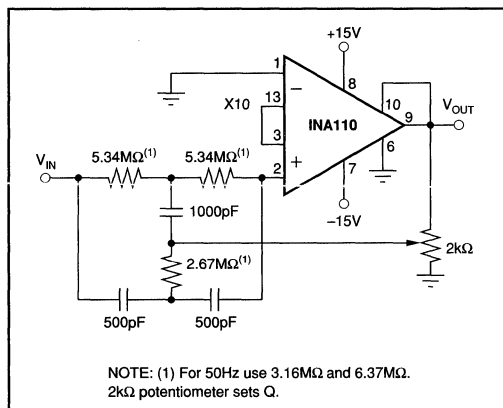


FIGURE 13. 60Hz Input Notch Filter.

INA110

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INSTRUMENTATION AMPLIFIERS

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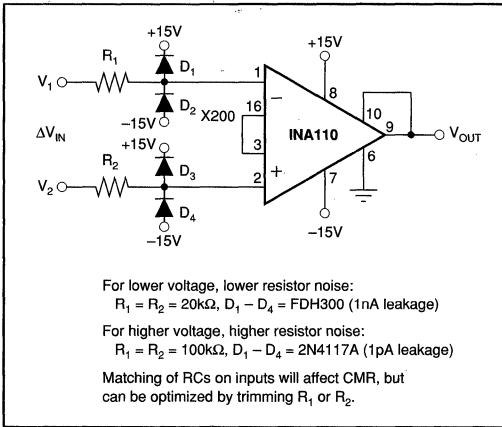


FIGURE 14. Input-Protected Instrumentation Amplifier.

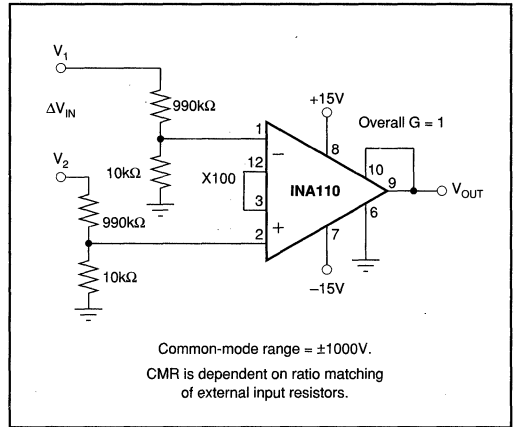


FIGURE 15. High Common-Mode Voltage Differential Amplifier.

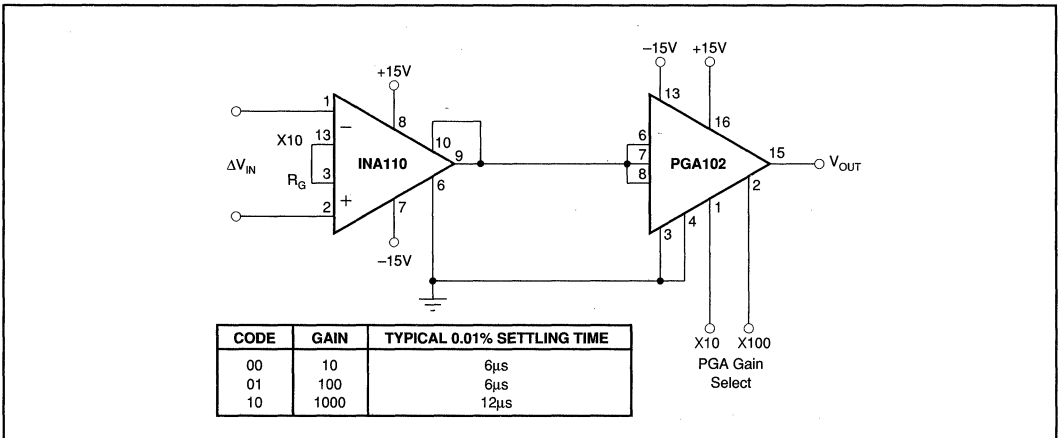


FIGURE 16. Digitally-Controlled Fast-Settling Programmable-Gain Instrumentation Amplifier.

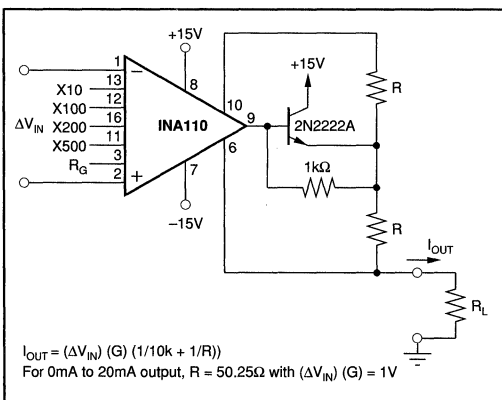


FIGURE 17. Differential Input FET Buffered Current Source.

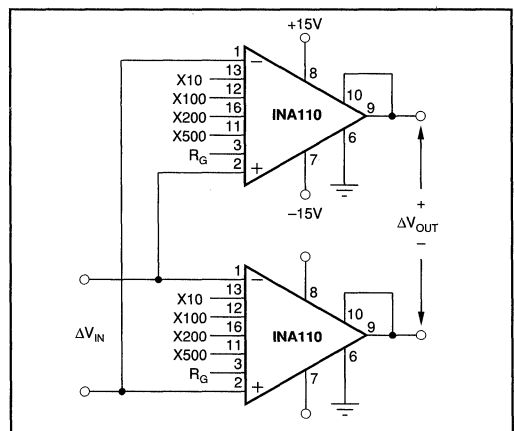


FIGURE 18. Differential Input/Differential Output Amplifier.



INA111

High Speed FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- FET INPUT: $I_B = 20\text{pA max}$
- HIGH SPEED: $T_s = 4\mu\text{s}$ ($G = 100, 0.01\%$)
- LOW OFFSET VOLTAGE: $500\mu\text{V max}$
- LOW OFFSET VOLTAGE DRIFT: $5\mu\text{V}/^\circ\text{C max}$
- HIGH COMMON-MODE REJECTION: 106dB min
- 8-PIN PLASTIC DIP, SOL-16 SOIC

APPLICATIONS

- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

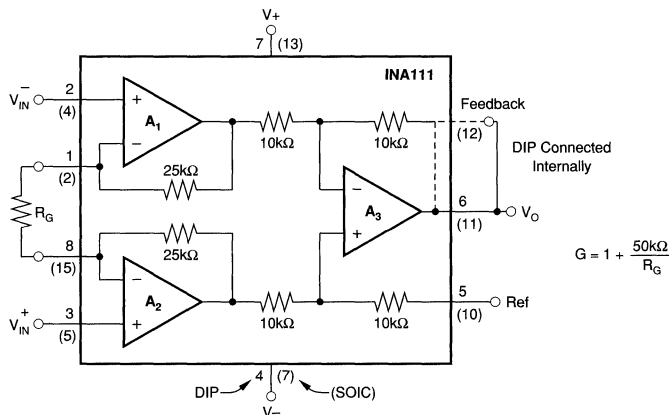
DESCRIPTION

The INA111 is a high speed, FET-input instrumentation amplifier offering excellent performance.

The INA111 uses a current-feedback topology providing extended bandwidth (2MHz at $G = 10$) and fast settling time ($4\mu\text{s}$ to 0.01% at $G = 100$). A single external resistor sets any gain from 1 to over 1000.

Offset voltage and drift are laser trimmed for excellent DC accuracy. The INA111's FET inputs reduce input bias current to under 20pA , simplifying input filtering and limiting circuitry.

The INA111 is available in 8-pin plastic DIP, and SOL-16 surface-mount packages, specified for the -40°C to $+85^\circ\text{C}$ temperature range.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA111BP, BU			INA111AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25^\circ\text{C}$		$\pm 100 \pm 500/\text{G}$	$\pm 500 \pm 2000/\text{G}$		$\pm 200 \pm 500/\text{G}$	$\pm 1000 \pm 5000/\text{G}$	μV
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}		$\pm 2 \pm 10/\text{G}$	$\pm 5 \pm 100/\text{G}$		$\pm 2 \pm 20/\text{G}$	$\pm 10 \pm 100/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 6\text{V}$ to $\pm 18\text{V}$		$2 + 10/\text{G}$	$30 + 100/\text{G}$		*	*	$\mu\text{V}/\text{V}$
Impedance, Differential			$10^{12} 6$			*		ΩpF
Common-Mode			$10^{12} 3$			*		ΩpF
Input Common-Mode Range	$V_{\text{DIFF}} = 0\text{V}$	± 10	± 12		*	*		V
Common-Mode Rejection	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$							
	$G = 1$	80	90		75	*		dB
	$G = 10$	96	110		90	*		dB
	$G = 100$	106	115		100	*		dB
	$G = 1000$	106	115		100	*		dB
BIAS CURRENT			± 2	± 20		*	*	pA
OFFSET CURRENT			± 0.1	± 10		*	*	pA
NOISE VOLTAGE, RTI	$G = 1000$, $R_S = 0\Omega$							
$f = 100\text{Hz}$			13			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			10			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			10			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			1			*		$\mu\text{Vp-p}$
Noise Current						*		$\text{fA}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			0.8			*		
GAIN								
Gain Equation			$1 + (50\text{k}\Omega/R_G)$			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	$G = 1$, $R_L = 10\text{k}\Omega$		± 0.01	± 0.02			0.05	%
	$G = 10$, $R_L = 10\text{k}\Omega$		± 0.1	± 0.5			*	%
	$G = 100$, $R_L = 10\text{k}\Omega$		± 0.15	± 0.5			± 0.7	%
	$G = 1000$, $R_L = 10\text{k}\Omega$		± 0.25	± 1			± 2	%
Gain vs Temperature	$G = 1$		± 1	± 10			*	$\text{ppm}/^\circ\text{C}$
50k Ω Resistance ⁽¹⁾			± 25	± 100			*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	$G = 1$		± 0.0005	± 0.005			*	% of FSR
	$G = 10$		± 0.001	± 0.005			± 0.01	% of FSR
	$G = 100$		± 0.001	± 0.005			± 0.01	% of FSR
	$G = 1000$		± 0.005	± 0.02			± 0.04	% of FSR
OUTPUT								
Voltage	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX}	± 11	± 12.7		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+30/-25			*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	$G = 1$		2			*		MHz
	$G = 10$		2			*		MHz
	$G = 100$		450			*		kHz
	$G = 1000$		50			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$, $G = 2$ to 100		17			*		V/ μs
Settling Time, 0.01%	$G = 1$		2			*		μs
	$G = 10$		2			*		μs
	$G = 100$		4			*		μs
	$G = 1000$		30			*		μs
Overload Recovery	50% Overdrive		1			*		μs
POWER SUPPLY								
Voltage Range		± 6	± 15	± 18	*	*	*	V
Current	$V_{\text{IN}} = 0\text{V}$		± 3.3	± 4.5			*	mA
TEMPERATURE RANGE								
Specification		-40		85	*		*	$^\circ\text{C}$
Operating	Plastic P, U	-40		125	*		*	$^\circ\text{C}$
θ_{JA}	Plastic P, U		100			*		$^\circ\text{C}/\text{W}$

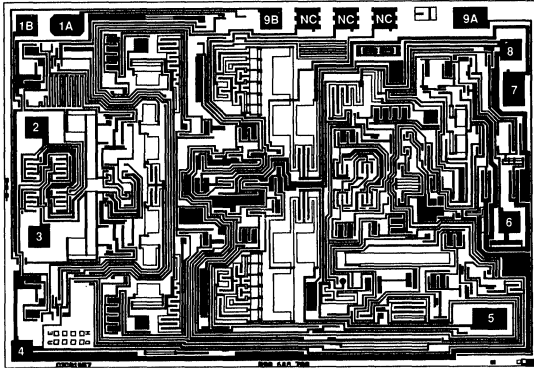
* Specification same as INA111BP.

NOTE: (1) Temperature coefficient of the "50k Ω " term in the gain equation.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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DICE INFORMATION



INA111 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	6	V_O
2	V_{IN}^-	7	Feedback
3	V_{IN}^+	8	V^+
4	V^-	9A, 9B	R_G
5	Ref		

Pads 1A and 1B must be connected. Pads 9A and 9B must be connected.

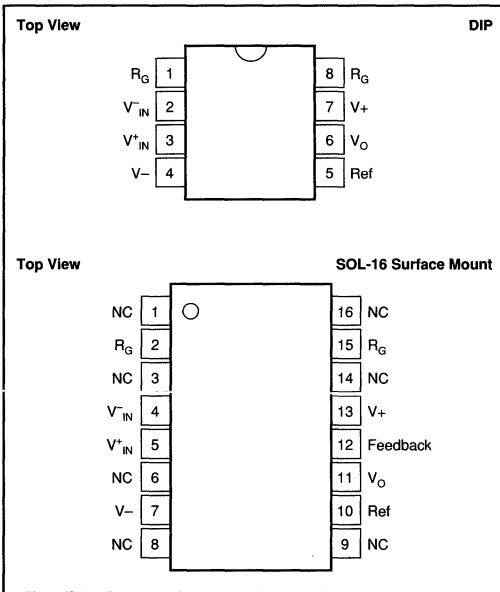
NC = No Connection.

Substrate Bias: Internally connected to V^- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	129 x 90 ±5	3.28 x 2.29 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ±18V
Input Voltage Range (V^-) -0.7V to (V^+) +15V
Output Short-Circuit (to ground) Continuous
Operating Temperature -40°C to +125°C
Storage Temperature -40°C to +125°C
Junction Temperature +150°C
Lead Temperature (soldering, 10s) +300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA111AP	8-Pin Plastic DIP	-40°C to +85°C
INA111BP	8-Pin Plastic DIP	-40°C to +85°C
INA111AU	SOL-16 Surface-Mount	-40°C to +85°C
INA111BU	SOL-16 Surface-Mount	-40°C to +85°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA111AP	8-Pin Plastic DIP	006
INA111BP	8-Pin Plastic DIP	006
INA111AU	16-Pin Surface Mount	211
INA111BU	16-Pin Surface Mount	211

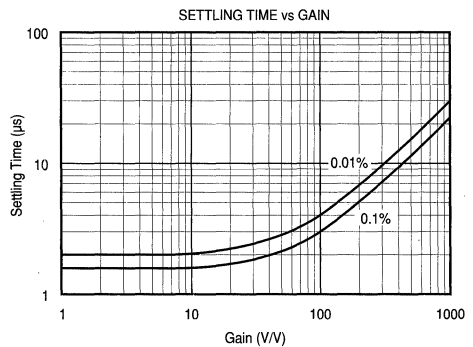
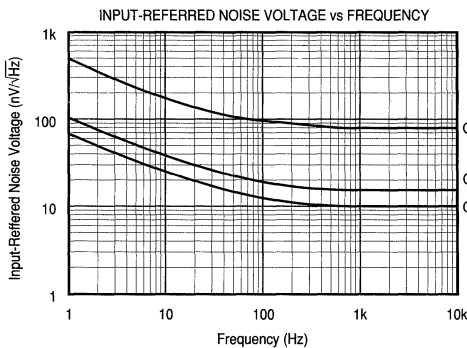
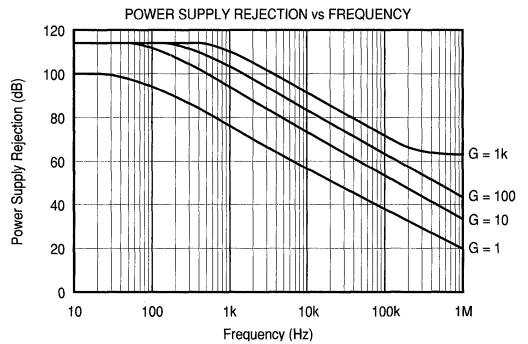
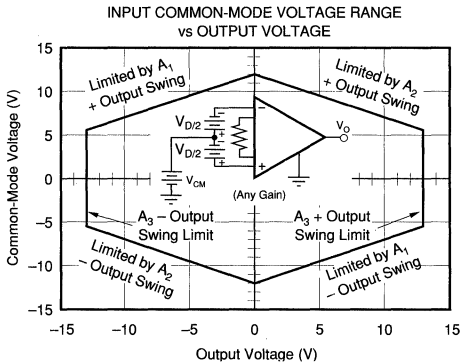
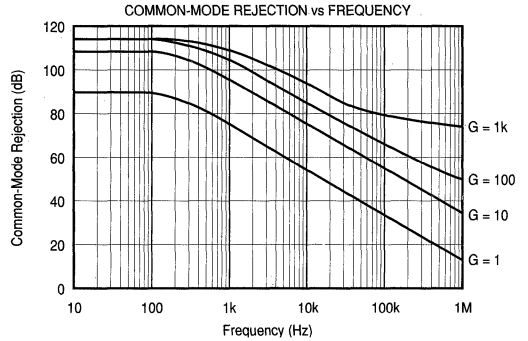
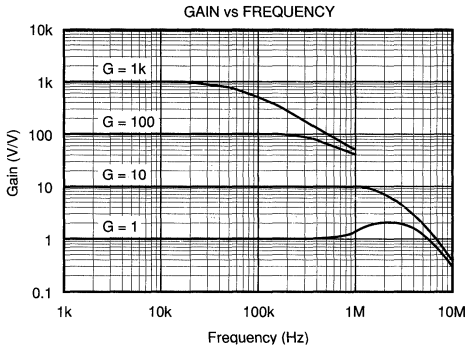
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



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TYPICAL PERFORMANCE CURVES

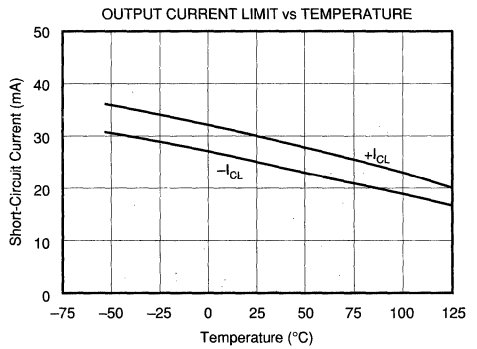
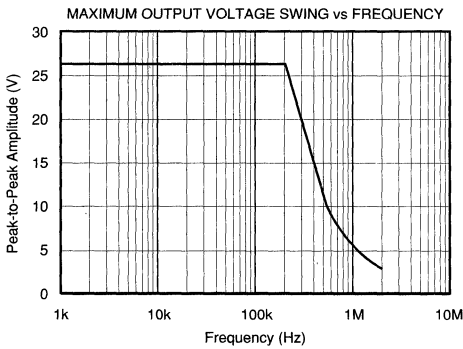
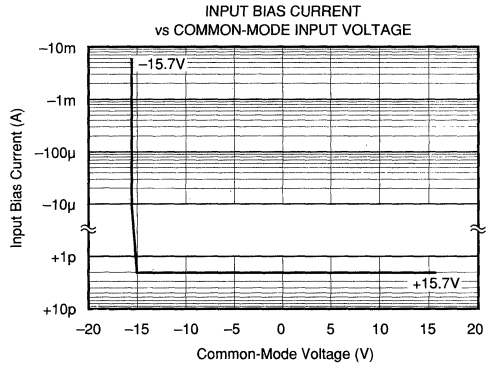
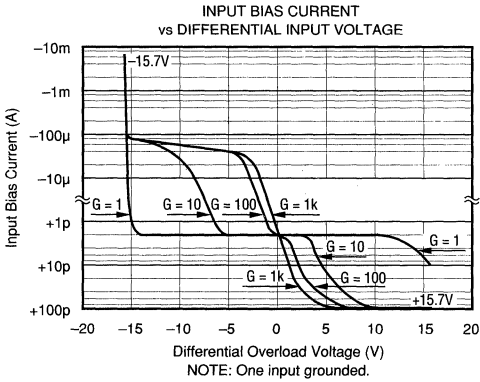
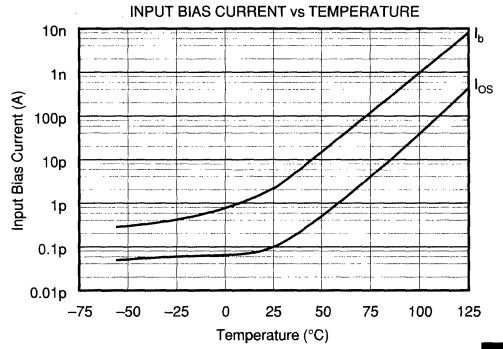
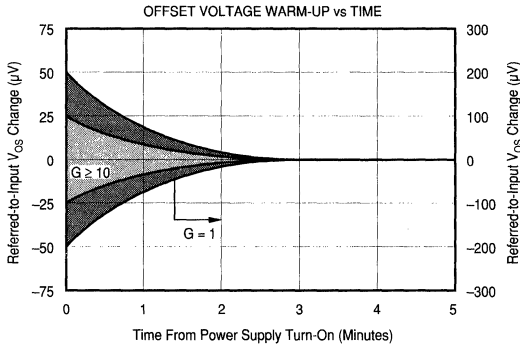
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



INA111

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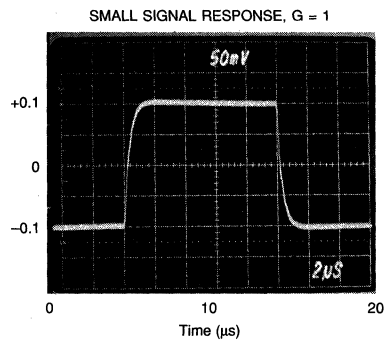
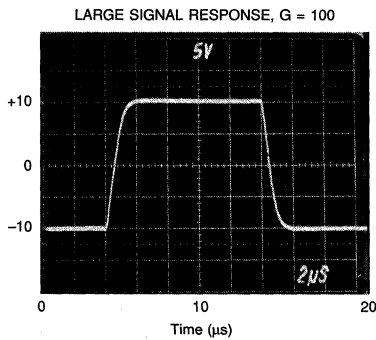
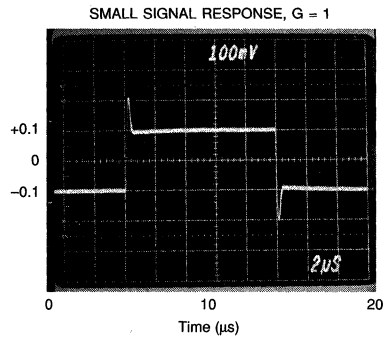
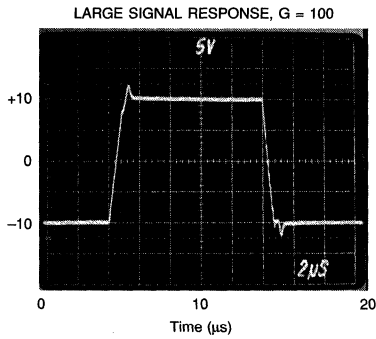
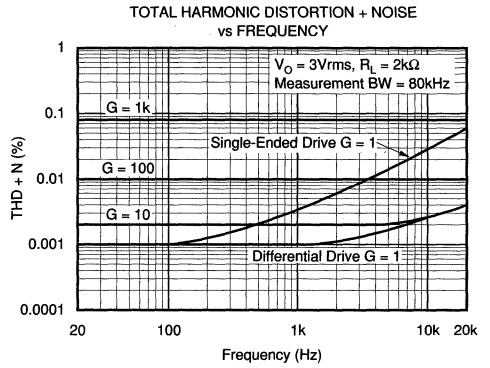
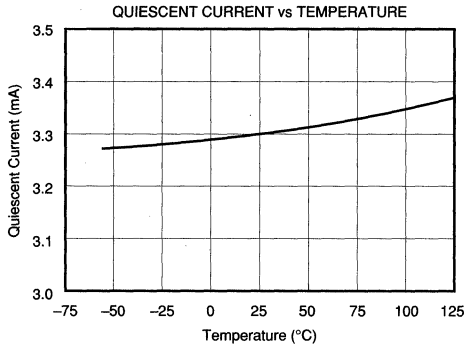
INSTRUMENTATION AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



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APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA111. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device with 90dB CMR to degrade to approximately 80dB CMR ($G=1$).

SETTING THE GAIN

Gain of the INA111 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The $50k\Omega$ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA111.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that the INA111 achieves wide bandwidth over a wide range of gain. This is due to the current-feedback topology of the INA111. Settling time also remains excellent over wide gains.

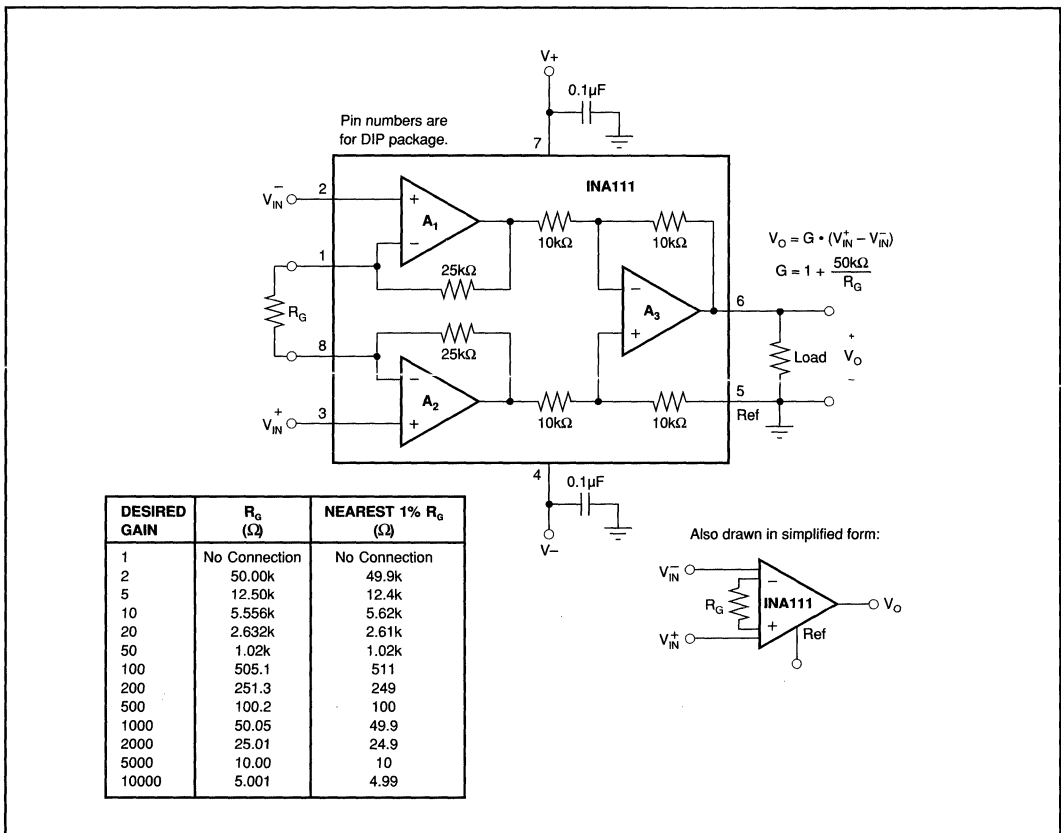


FIGURE 1. Basic Connections

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The INA111 exhibits approximately 6dB rise in gain at 2MHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 700kHz or lower will produce a flat passband response (see Input Filtering).

The INA111 provides excellent rejection of high frequency common-mode signals. The typical performance curve, "Common-Mode Rejection vs Frequency" shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^+ and V_{IN}^- connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA111's FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2k Ω to 50k Ω the INA114 may provide lower offset voltage and drift. For very low source impedance ($\leq 1k\Omega$), the INA103 may provide improved accuracy and lower noise.

OFFSET TRIMMING

The INA111 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp shown maintains low output impedance at high frequency. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

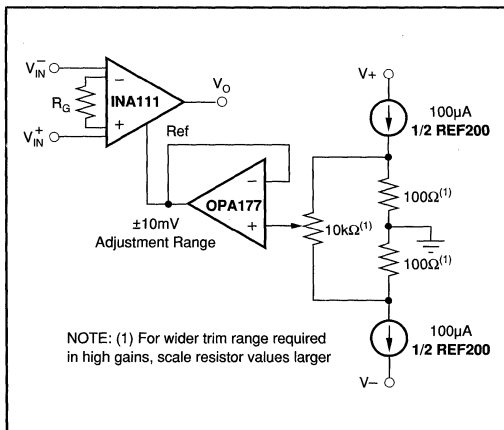


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA111 is extremely high—approximately $10^{12}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than 10pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA111 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA111 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

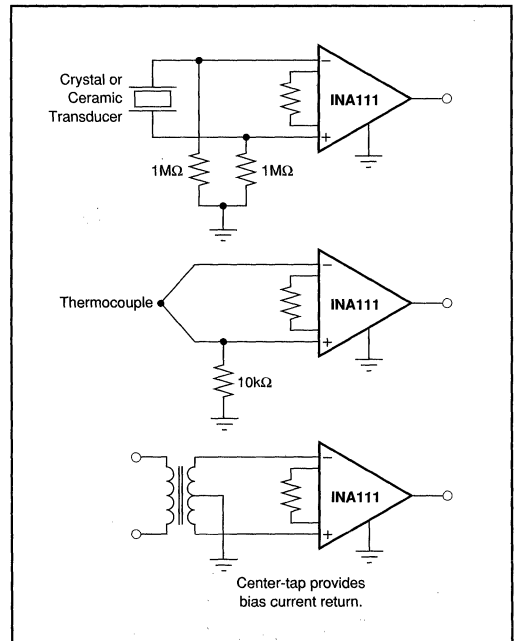


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA111 is approximately $\pm 12V$ (or 3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage".

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A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA111 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA111 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +14V on one input and +15V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA111 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

Inputs of the INA111 are protected for input voltages from 0.7V below the negative supply to 15V above the positive supply voltages. If the input current is limited to less than 1mA, clamp diodes are not required; internal junctions will clamp the input voltage to safe levels. If the input source can supply more than 1mA, use external clamp diodes as shown in Figure 5. The source current can be limited with series resistors R_1 and R_2 as shown. Resistor values greater than 10k Ω will contribute noise to the circuit.

A diode formed with a 2N4117A transistor as shown in Figure 5 assures low leakage. Common signal diodes such as

the 1N4148 may have leakage currents far greater than the input bias current of the INA111 and are usually sensitive to light.

INPUT FILTERING

The INA111's FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 6 shows proper implementation of this input filter to preserve the INA111's excellent high frequency common-mode rejection. Mismatch of the common-mode input capacitance (C_1 and C_2), either from stray capacitance or

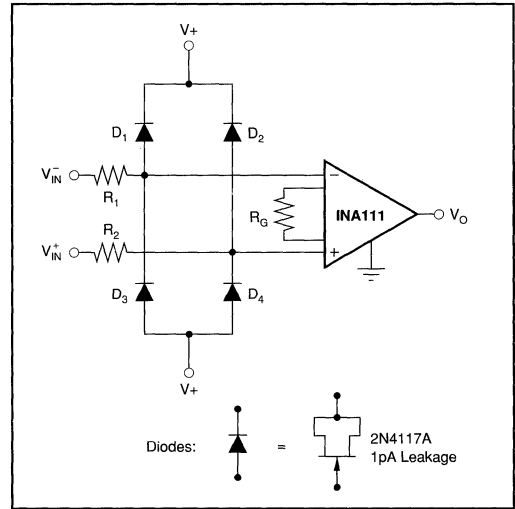


FIGURE 5. Input Protection Voltage Clamp.

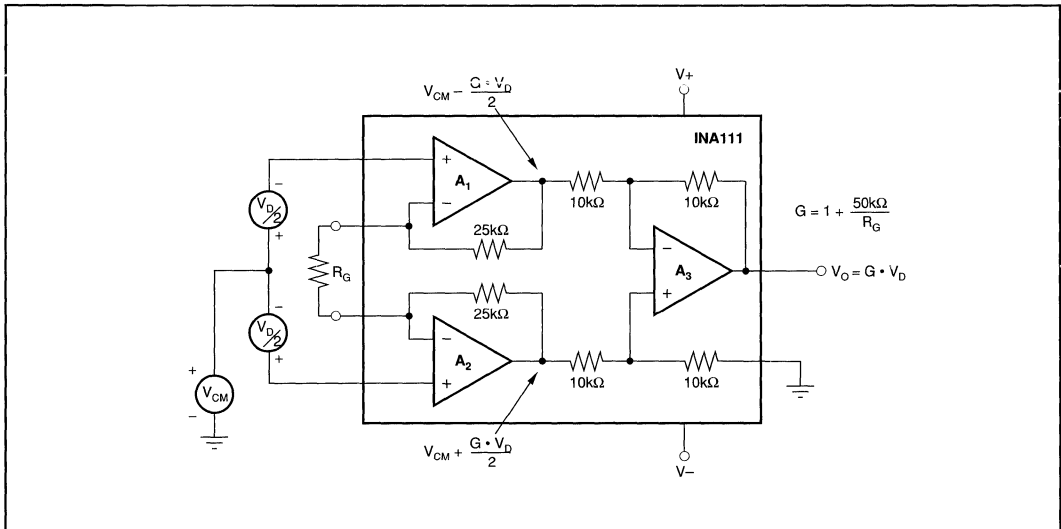


FIGURE 4. Voltage Swing of A_1 and A_2 .

mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor, C_3 , reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2 . Make C_3 much larger than C_1 and C_2 . If properly matched, C_1 and C_2 also improve CMR.

OUTPUT VOLTAGE SENSE (SOL-16 Package Only)

The surface-mount version of the INA111 has a separate output sense feedback connection (pin 12). Pin 12 must be connected, usually to the output terminal, pin 11, for proper operation. (This connection is made internally on the DIP version of the INA111.)

The output feedback connection can be used to sense the output voltage directly at the load for best accuracy. Figure 8 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1 .

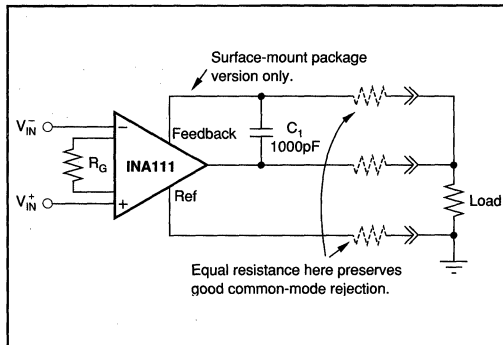


FIGURE 8. Remote Load and Ground Sensing.

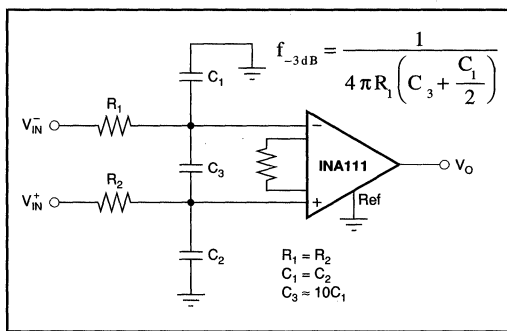


FIGURE 6. Input Low-Pass Filter.

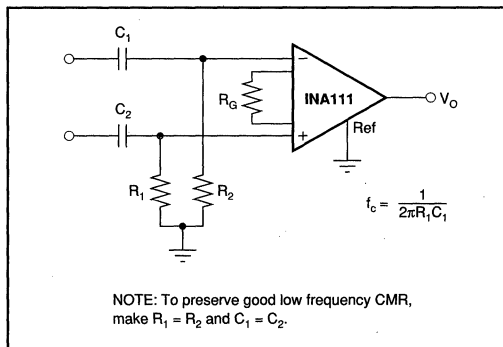


FIGURE 9. High-Pass Input Filter.

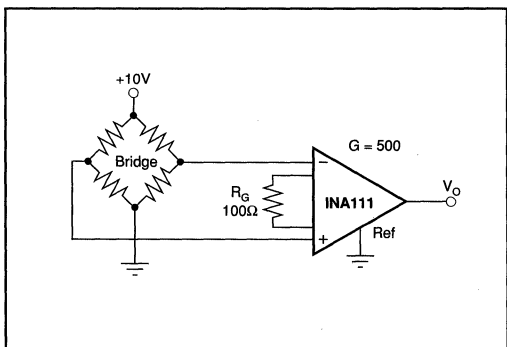


FIGURE 7. Bridge Transducer Amplifier.

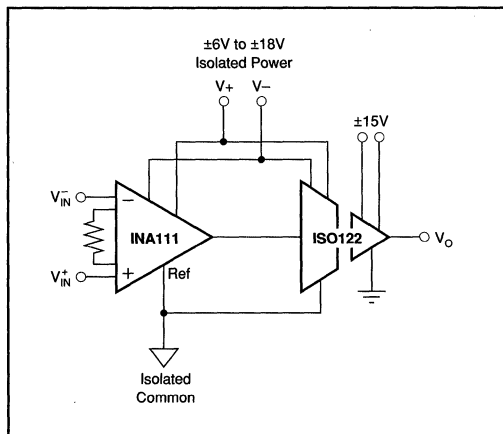


FIGURE 10. Galvanically Isolated Instrumentation Amplifier.

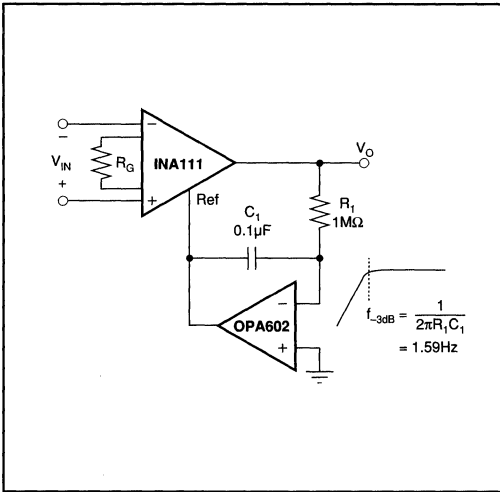


FIGURE 11. AC-Coupled Instrumentation Amplifier.

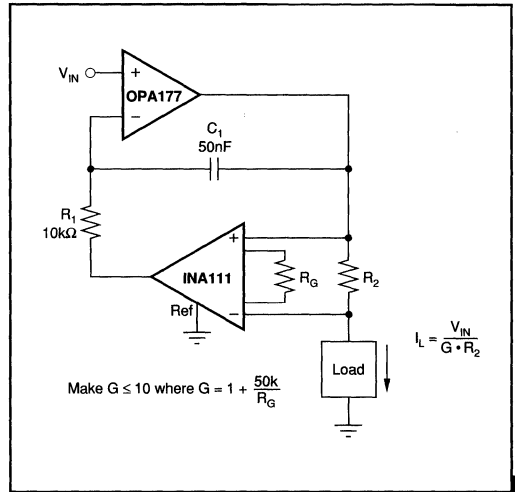


FIGURE 12. Voltage Controlled Current Source.

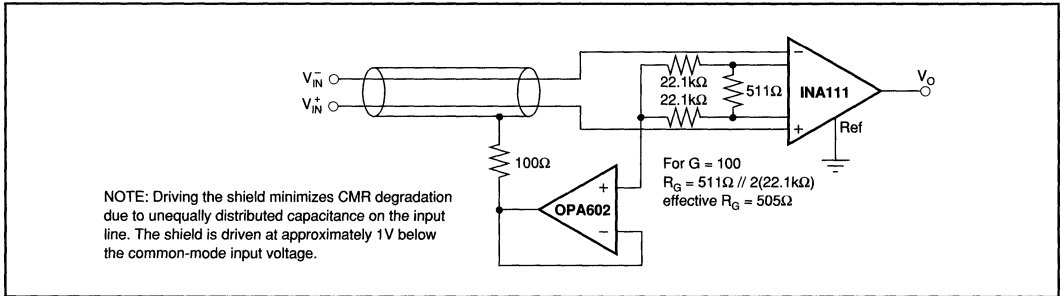


FIGURE 13. Shield Driver Circuit.

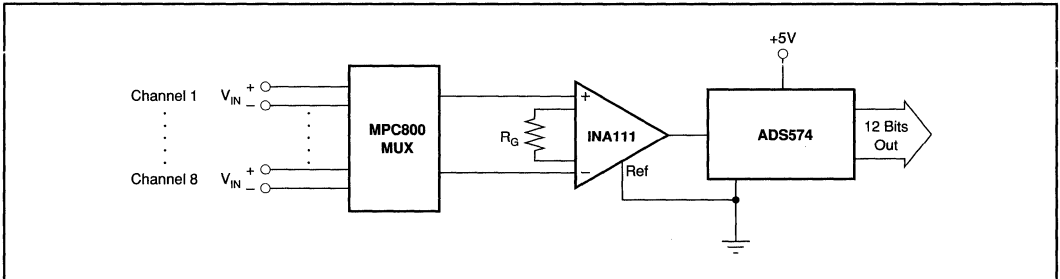
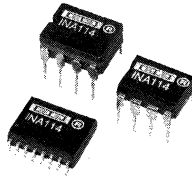


FIGURE 14. Multiplexed-Input Data Acquisition System.

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INA114

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 50 μ V max
- **LOW DRIFT:** 0.25 μ V/ $^{\circ}$ C max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 115dB min
- **INPUT OVER-VOLTAGE PROTECTION:** \pm 40V
- **WIDE SUPPLY RANGE:** \pm 2.25 to \pm 18V
- **LOW QUIESCENT CURRENT:** 3mA max
- **8-PIN PLASTIC AND CERAMIC DIP, SOL-16**

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

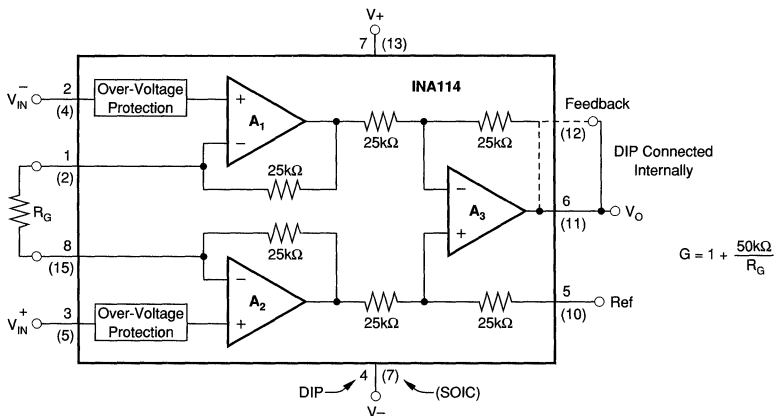
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to \pm 40V without damage.

The INA114 is laser trimmed for very low offset voltage (50 μ V), drift (0.25 μ V/ $^{\circ}$ C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as \pm 2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and ceramic DIPs, and SOL-16 surface-mount packages, specified for the -40° C to $+85^{\circ}$ C temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	INA114BP, BG, BU			INA114AP, AG, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25^\circ\text{C}$		$\pm 10 + 20/\text{G}$	$\pm 50 + 100/\text{G}$		$\pm 25 + 30/\text{G}$	$\pm 125 + 500/\text{G}$	μV
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}		$\pm 0.1 + 0.5/\text{G}$	$\pm 0.25 + 5/\text{G}$		$\pm 0.25 + 5/\text{G}$	$\pm 1 + 10/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		$0.5 + 2/\text{G}$	$3 + 10/\text{G}$		*	*	$\mu\text{V}/\text{V}$
Long-Term Stability			$\pm 0.2 + 0.5/\text{G}$			*	*	$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Common-Mode			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Input Common-Mode Range		± 11	± 13.5		*	*	*	V
Safe Input Voltage				± 40				V
Common-Mode Rejection	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$							
G = 1		80	96		75	90		dB
G = 10		96	115		90	106		dB
G = 100		110	120		106	110		dB
G = 1000		115	120		106	110		dB
BIAS CURRENT								
vs Temperature			± 0.5	± 2		*	± 5	nA
			± 8			*		$\text{pA}/^\circ\text{C}$
OFFSET CURRENT								
vs Temperature			± 0.5	± 2		*	± 5	nA
			± 8			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	$G = 1000$, $R_S = 0\Omega$							
f = 10Hz			15			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			11			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			11			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.4			*		$\mu\text{Vp-p}$
Noise Current						*		
f = 10Hz			0.4			*		$\text{pA}/\sqrt{\text{Hz}}$
f = 1kHz			0.2			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			18			*		pAp-p
GAIN								
Gain Equation			$1 + (50\text{k}\Omega/R_G)$		*	*	*	V/V
Range of Gain		1		10000				V/V
Gain Error	G = 1		± 0.01	± 0.05		*	*	%
	G = 10		± 0.02	± 0.4		*	± 0.5	%
	G = 100		± 0.05	± 0.5		*	± 0.7	%
	G = 1000		± 0.5	± 1		*	± 2	%
	G = 1		± 2	± 10		*	± 10	ppm/ $^\circ\text{C}$
Gain vs Temperature			± 25	± 100		*	*	ppm/ $^\circ\text{C}$
50k Ω Resistance ⁽¹⁾			± 0.0001	± 0.001		*	± 0.002	% of FSR
Nonlinearity	G = 1		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 10		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 100		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 1000		± 0.002	± 0.01		*	± 0.02	% of FSR
OUTPUT								
Voltage	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX}	± 13.5	± 13.7		*	*	*	V
	$V_S = \pm 11.4\text{V}$, $R_L = 2\text{k}\Omega$	± 10	± 10.5		*	*	*	V
	$V_S = \pm 2.25\text{V}$, $R_L = 2\text{k}\Omega$	± 1	± 1.5		*	*	*	V
Load Capacitance Stability			1000			*	*	pF
Short Circuit Current			$+20/-15$			*	*	mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	G = 1		1			*	*	MHz
	G = 10		100			*	*	kHz
	G = 100		10			*	*	kHz
	G = 1000		1			*	*	kHz
Slew Rate	$V_O = \pm 10\text{V}$, G = 10	0.3	0.6		*	*	*	V/ μs
Settling Time, 0.01%	G = 1		18			*	*	μs
	G = 10		20			*	*	μs
	G = 100		120			*	*	μs
	G = 1000		1100			*	*	μs
Overload Recovery	50% Overdrive		20			*	*	μs
POWER SUPPLY								
Voltage Range		± 2.25	± 15	± 18	*	*	*	V
Current	$V_{\text{IN}} = 0\text{V}$		± 2.2	± 3		*	*	mA
TEMPERATURE RANGE								
Specification		-40		85	*	*	*	$^\circ\text{C}$
Operating		-40		125	*	*	*	$^\circ\text{C}$
θ_{JA}			80			*	*	$^\circ\text{C}/\text{W}$

* Specification same as INA114BP/BU.

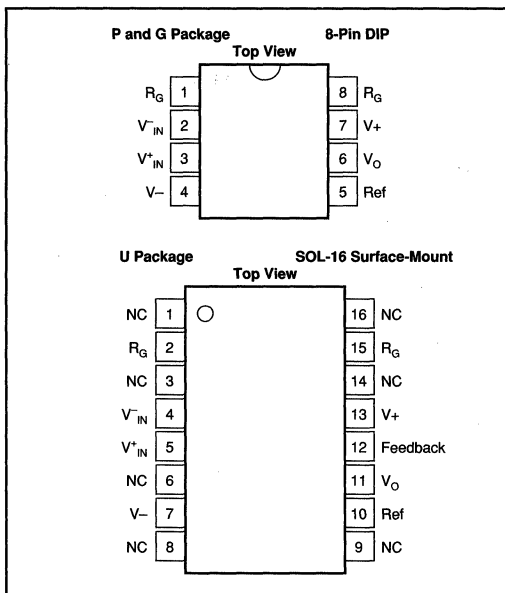
NOTE: (1) Temperature coefficient of the "50k Ω " term in the gain equation.

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PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA114AP	Plastic DIP	-40°C to +85°C
INA114BP	Plastic DIP	-40°C to +85°C
INA114AG	Ceramic DIP	-40°C to +85°C
INA114BG	Ceramic DIP	-40°C to +85°C
INA114AU	Surface-Mount	-40°C to +85°C
INA114BU	Surface-Mount	-40°C to +85°C

PACKAGE INFORMATION⁽¹⁾

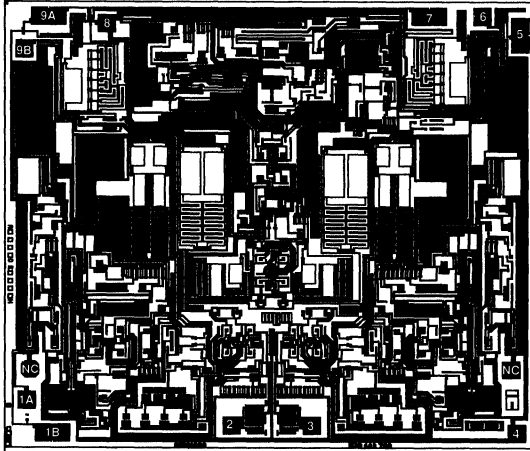
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA114AP	8-Pin Plastic DIP	006
INA114BP	8-Pin Plastic DIP	006
INA114AG	8-Pin Ceramic DIP	254
INA114BG	8-Pin Ceramic DIP	254
INA114AU	SOL-16 Surface-Mount	211
INA114BU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



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DICE INFORMATION



INA114 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	6	V_O
2	V_{IN}	7	Feedback
3	V_{IN}^+	8	V_+
4	V_{IN}^-	9A, 9B	R_G
5	Ref		

Pads 1A and 1B must be connected. Pads 9A and 9B must be connected.

NC = No Connection.

Substrate Bias: Internally connected to V_- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

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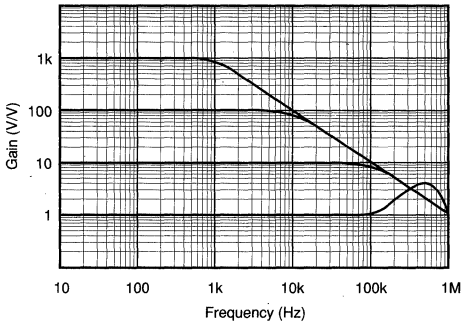
INSTRUMENTATION AMPLIFIERS

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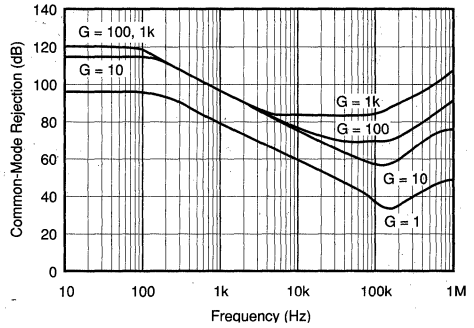
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

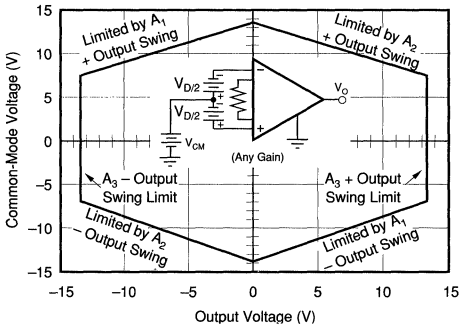
GAIN vs FREQUENCY



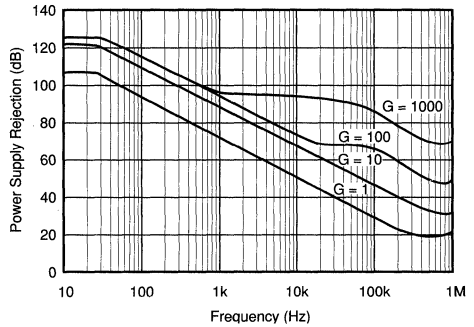
COMMON-MODE REJECTION vs FREQUENCY



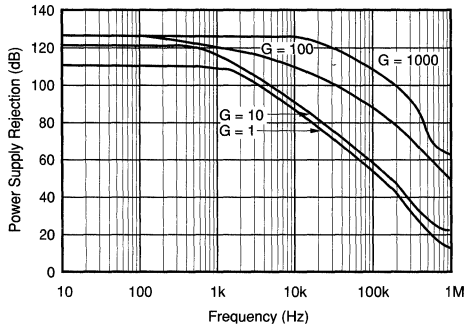
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



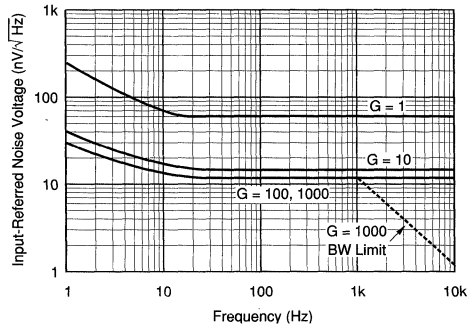
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



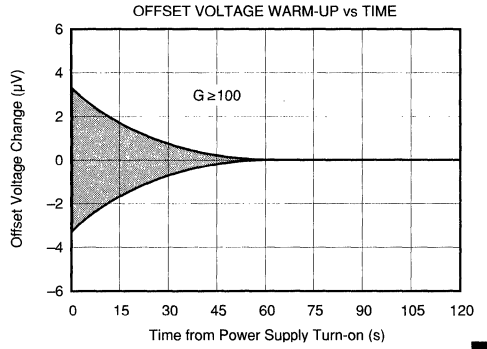
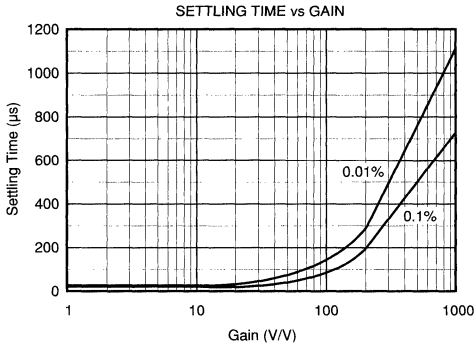
INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY



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TYPICAL PERFORMANCE CURVES (CONT)

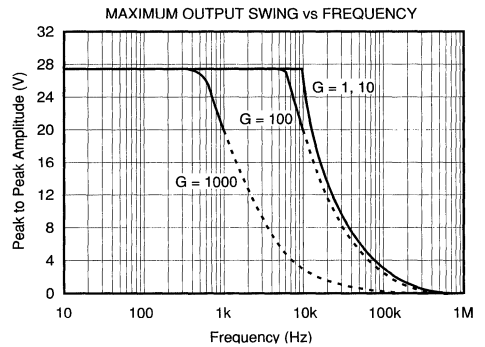
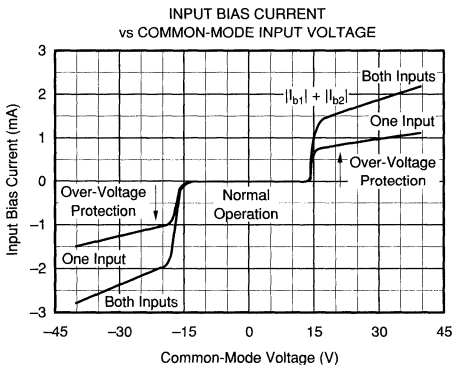
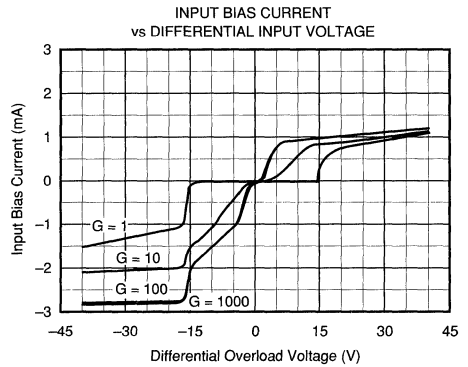
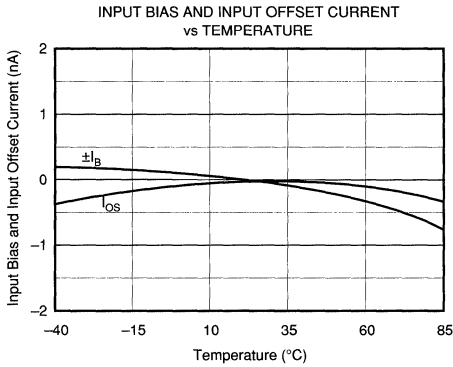
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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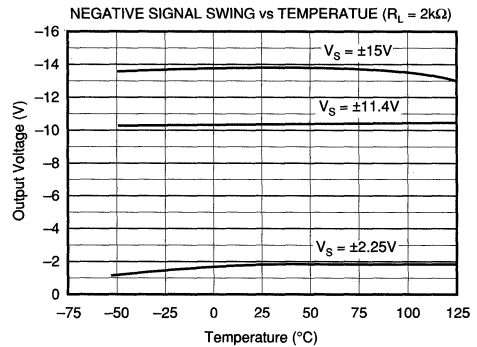
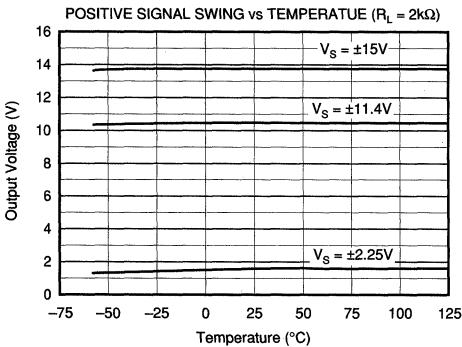
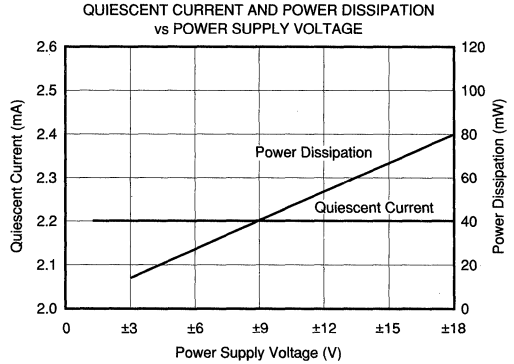
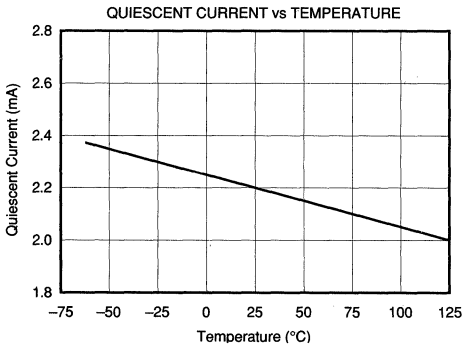
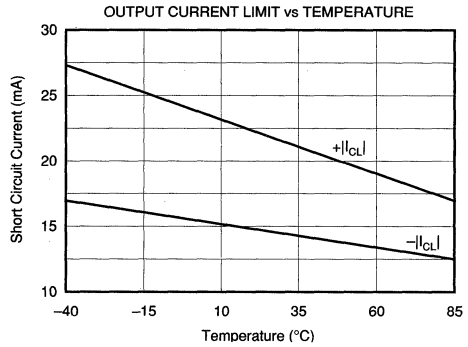
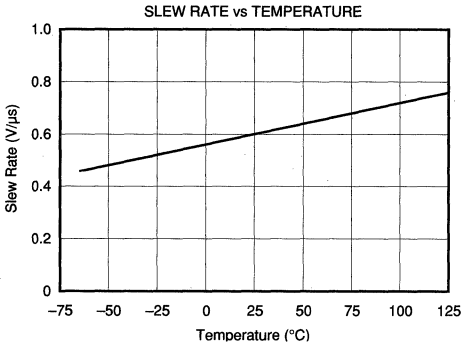
INSTRUMENTATION AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

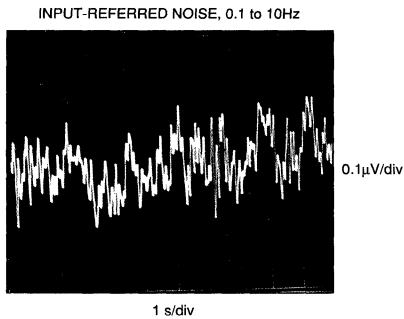
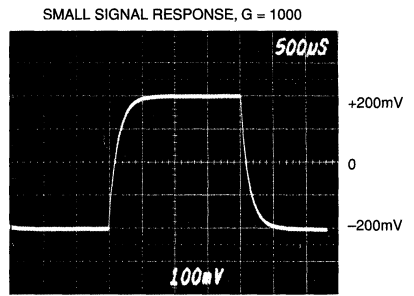
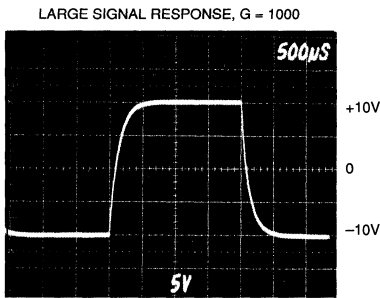
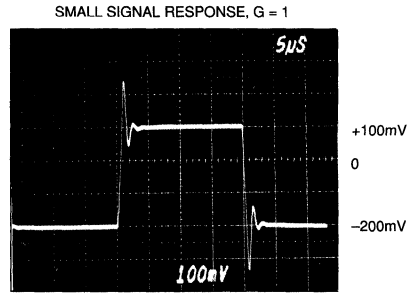
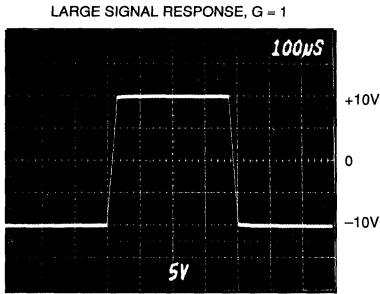
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



INA114

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INSTRUMENTATION AMPLIFIERS

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ($G = 1$).

SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute val-

ues. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.

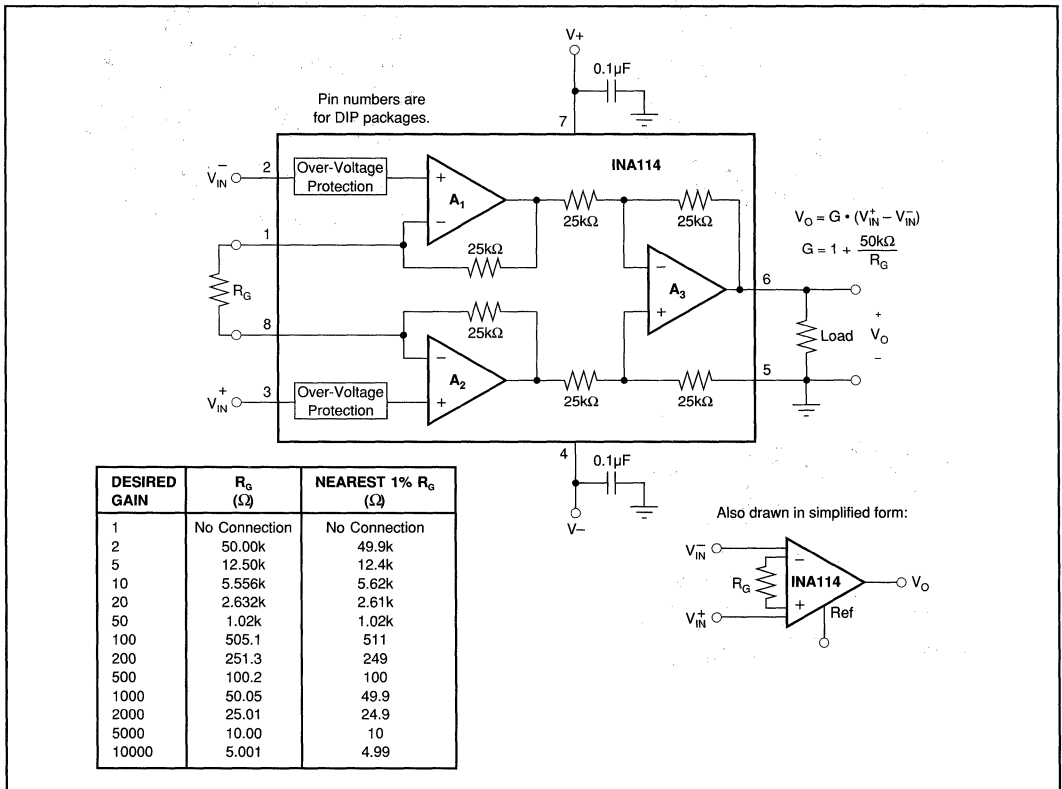


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

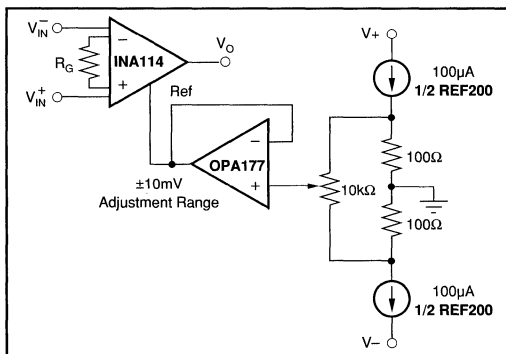


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage”.

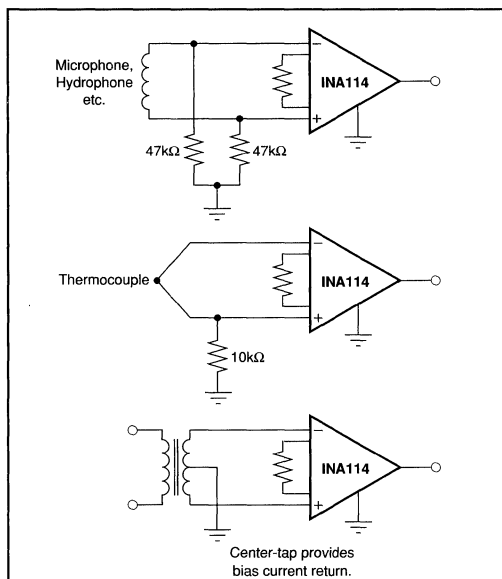


FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of $+20\text{V}$ on one input and $+40\text{V}$ on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input

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current limit behavior. The inputs are protected even if no power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1 . Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).

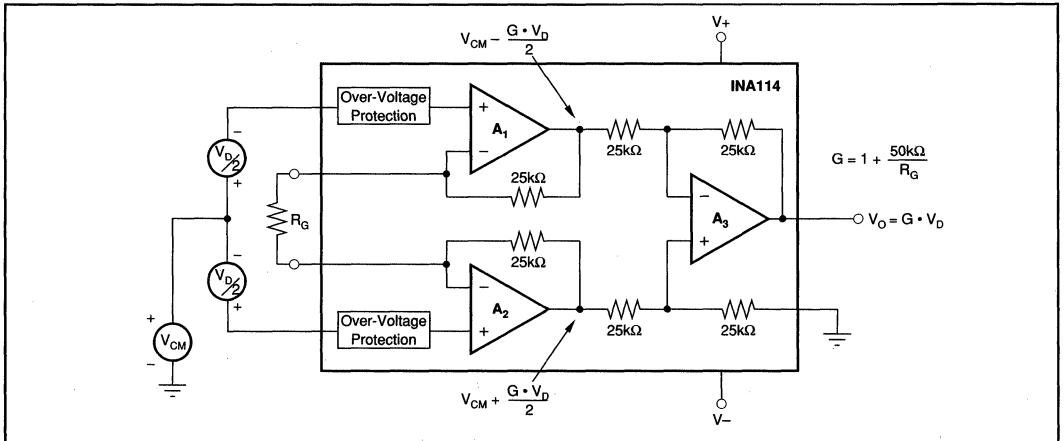


FIGURE 4. Voltage Swing of A_1 and A_2 .

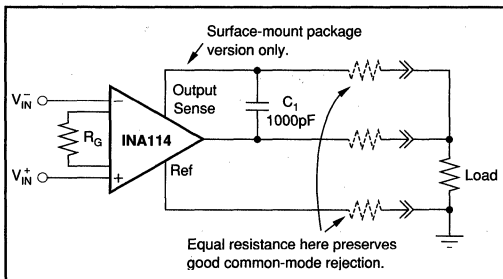


FIGURE 5. Remote Load and Ground Sensing.

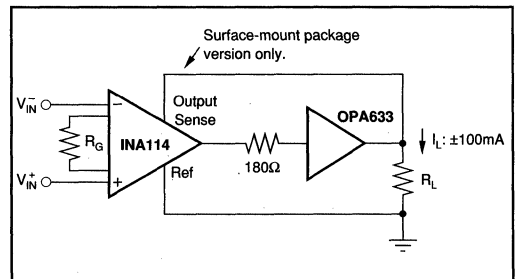


FIGURE 6. Buffered Output for Heavy Loads.

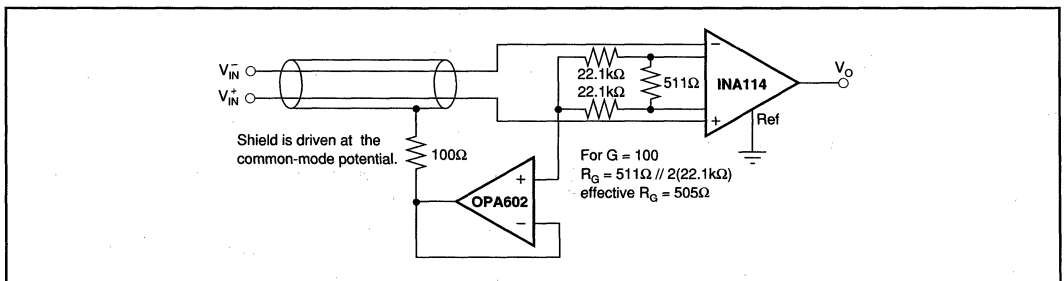


FIGURE 7. Shield Driver Circuit.

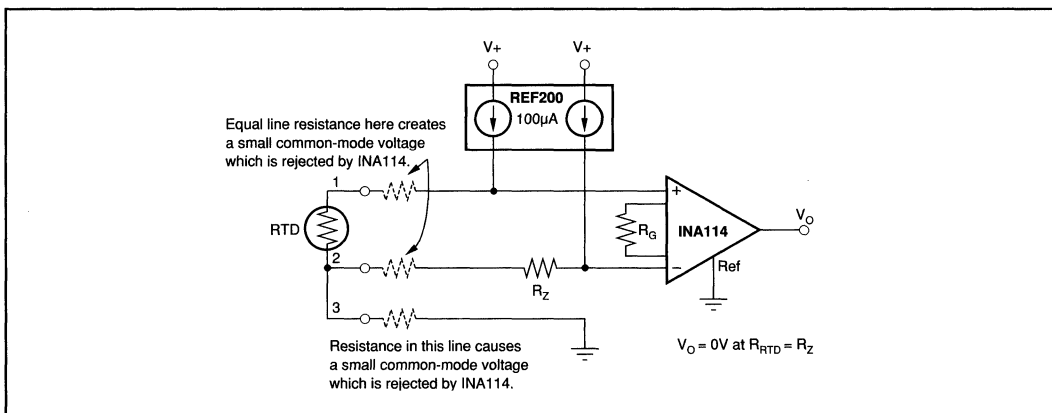


FIGURE 8. RTD Temperature Measurement Circuit.

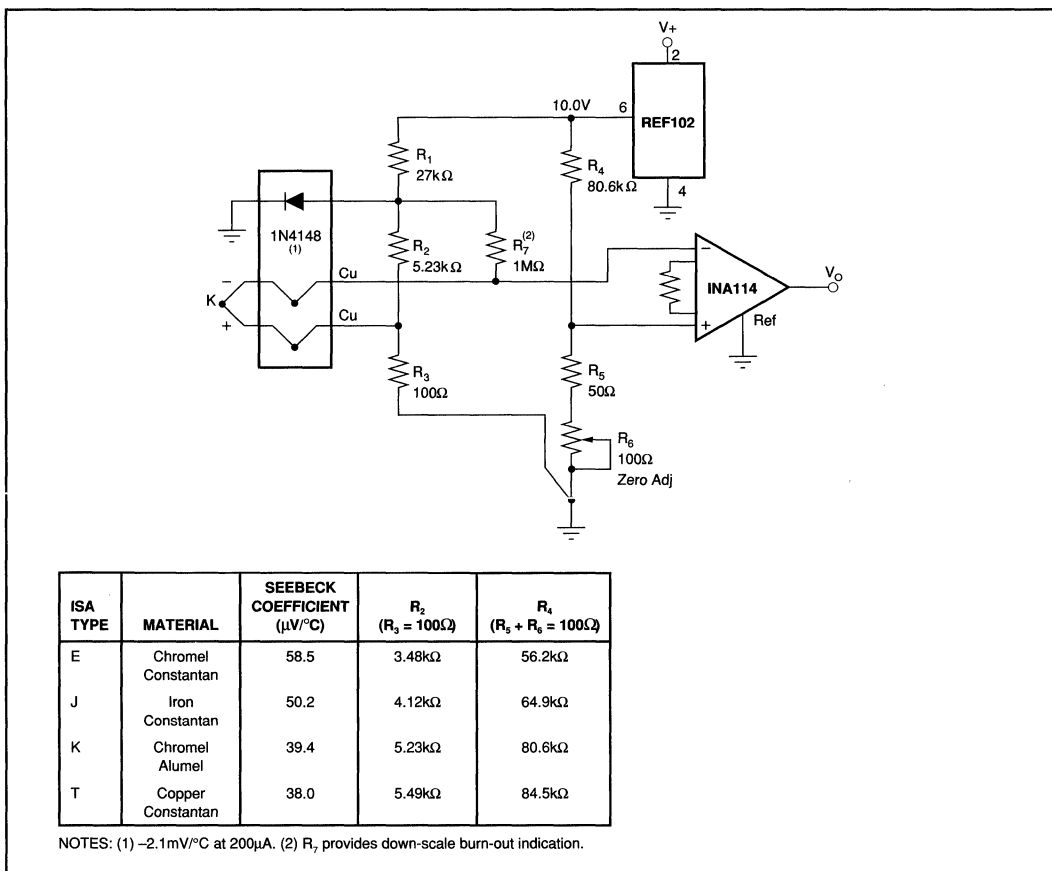


FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

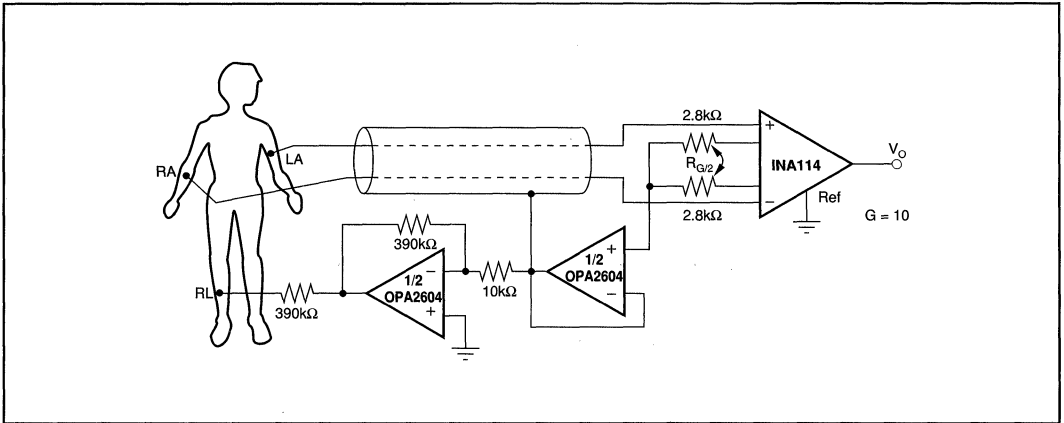


FIGURE 10. ECG Amplifier With Right-Leg Drive.

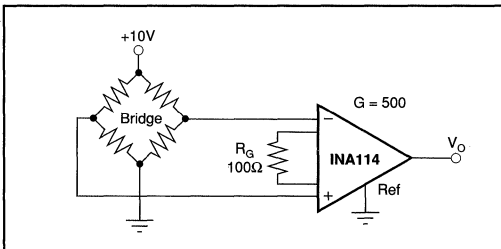


FIGURE 11. Bridge Transducer Amplifier.

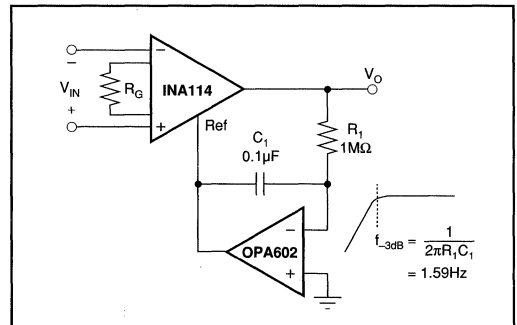


FIGURE 12. AC-Coupled Instrumentation Amplifier.

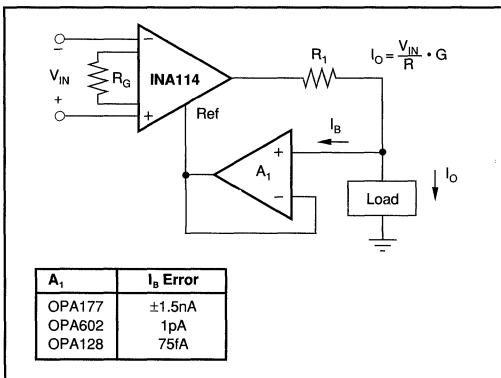


FIGURE 13. Differential Voltage to Current Converter.

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INA115

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 50 μ V max
- **LOW DRIFT:** 0.25 μ V/ $^{\circ}$ C max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 115dB min
- **INPUT OVER-VOLTAGE PROTECTION:** \pm 40V
- **WIDE SUPPLY RANGE:** \pm 2.25 TO \pm 18V
- **LOW QUIESCENT CURRENT:** 3mA max
- **SOL-16 SURFACE-MOUNT PACKAGE**

APPLICATIONS

- **SWITCHED-GAIN AMPLIFIER**
- **BRIDGE AMPLIFIER**
- **THERMOCOUPLE AMPLIFIER**
- **RTD SENSOR AMPLIFIER**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION**

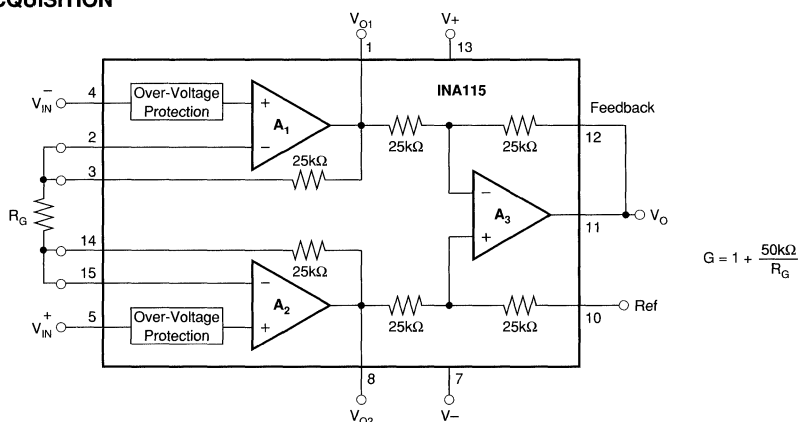
DESCRIPTION

The INA115 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and small size make it ideal for a wide range of applications. Similar to the model INA114, the INA115 provides additional connections to the input op amps, A_1 and A_2 , which improve gain accuracy in high gains and are useful in forming switched-gain amplifiers.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to \pm 40V without damage.

The INA115 is laser trimmed for very low offset voltage (50 μ V), drift (0.25 μ V/ $^{\circ}$ C) and high common-mode rejection (115dB at $G=1000$). It operates with power supplies as low as \pm 2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA115 is available in the SOL-16 surface-mount package, specified for the -40° C to $+85^{\circ}$ C temperature range.



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PDS-1169A

4.87

INA115

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	INA115BU			INA115AU			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT Offset Voltage, RTI Initial vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$ $V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$		$\pm 10 + 20/G$ $\pm 0.1 + 0.5/G$ $0.5 + 2/G$ $\pm 0.2 + 0.5/G$ $10^{10} \parallel 6$ $10^{10} \parallel 6$ ± 13.5	$\pm 50 + 100/G$ $\pm 0.25 + 5/G$ $3 + 10/G$		$\pm 25 + 30/G$ $\pm 0.25 + 5/G$ * * * * *	$\pm 125 + 500/G$ $\pm 1 + 10/G$ * * * * *	μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{m}\Omega$ $\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$ V V	
		80	96		75	90		dB	
		96	115		90	106		dB	
		110	120		106	110		dB	
		115	120		106	110		dB	
									nA
									pA/°C
									nA
									pA/°C
									nV/√Hz
							nV/√Hz		
							nV/√Hz		
							μVp-p		
							pA/√Hz		
							pA/√Hz		
							pAp-p		
GAIN Gain Equation Range of Gain Gain Error Gain vs Temperature 50kΩ Resistance ⁽¹⁾ Nonlinearity	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$	1	$1 + (50\text{k}\Omega/R_D)$	10000	*	*	*	V/V	
			± 0.01	± 0.05	*	*	*	V/V	
			± 0.02	± 0.4	*	*	*	%	
			± 0.05	± 0.5	*	*	*	%	
			± 0.5	± 1	*	*	*	%	
			± 2	± 10	*	*	*	ppm/°C	
			± 25	± 100	*	*	*	ppm/°C	
			± 0.0001	± 0.001	*	*	*	% of FSR	
			± 0.0005	± 0.002	*	*	*	% of FSR	
			± 0.0005	± 0.002	*	*	*	% of FSR	
OUTPUT⁽²⁾ Voltage Load Capacitance Stability Short Circuit Current	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX} $V_S = \pm 11.4\text{V}$, $R_L = 2\text{k}\Omega$ $V_S = \pm 2.25\text{V}$, $R_L = 2\text{k}\Omega$	± 13.5	± 13.7	*	*	*	V		
		± 10	± 10.5	*	*	*	V		
		± 1	± 1.5	*	*	*	V		
			1000	*	*	*	pF		
			$+20/-15$	*	*	*	mA		
FREQUENCY RESPONSE Bandwidth, -3dB Slew Rate Settling Time, 0.01% Overload Recovery	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $V_O = \pm 10\text{V}$, $G = 10$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$ 50% Overdrive		1		*	*	*	MHz	
			100		*	*	*	kHz	
			10		*	*	*	kHz	
			1		*	*	*	kHz	
		0.3	0.6		*	*	*	V/μs	
			18		*	*	*	μs	
			20		*	*	*	μs	
			120		*	*	*	μs	
			1100		*	*	*	μs	
			20		*	*	*	μs	
POWER SUPPLY Voltage Range Current	$V_{\text{IN}} = 0\text{V}$	± 2.25	± 15	± 18	*	*	*	V	
			± 2.2	± 3	*	*	*	mA	
					*	*	*	°C	
TEMPERATURE RANGE Specification Operating θ_{JA}		-40		+85	*	*	*	°C	
		-40		+125	*	*	*	°C	
			80		*	*	*	°C/W	

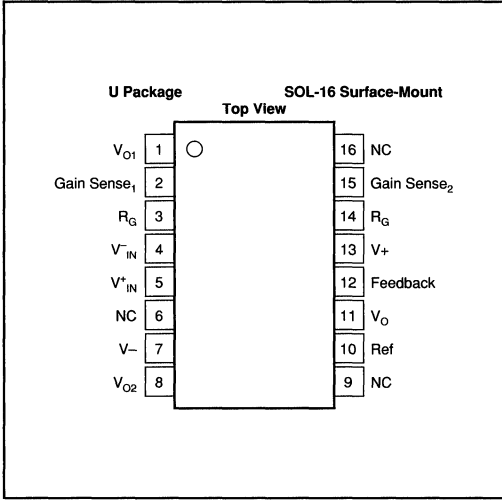
* Specification same as INA115BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) Output specifications are for output amplifier, A_3 . A_1 and A_2 provide the same output voltage swing but have less output current drive. A_1 and A_2 can drive external loads of $25\text{k}\Omega \parallel 200\text{pF}$.

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PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION⁽¹⁾

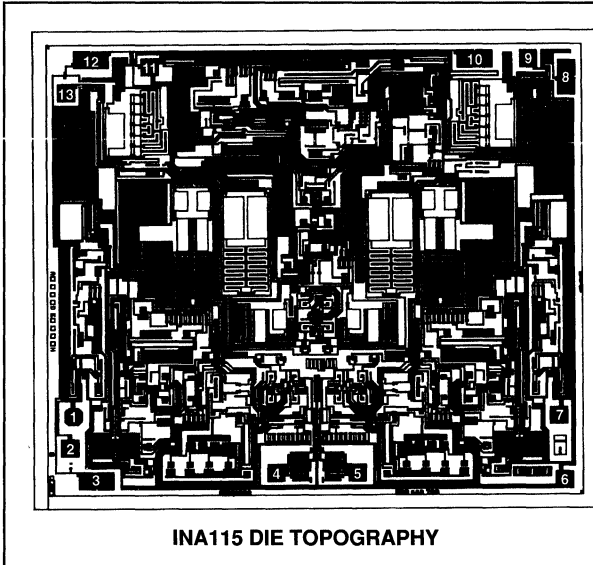
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA115AU	SOL-16 Surface-Mount	211
INA115BU	SOL-16 Surface-Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA115AU	SOL-16 Surface-Mount	-40°C to +85°C
INA115BU	SOL-16 Surface-Mount	-40°C to +85°C

DICE INFORMATION



INA115 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V _{O1}	8	Ref
2	Gain Sense ₁	9	V _O
3	R _G	10	Feedback
4	V _{IN}	11	V ₊
5	V _{IN} ⁺	12	R _G
6	V ₋	13	Gain Sense ₂
7	V _{O2}		

Substrate Bias: Internally connected to V₋ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

INA115

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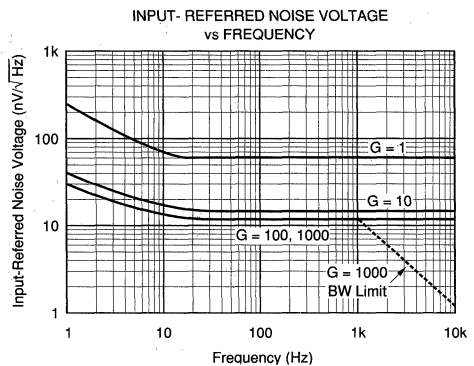
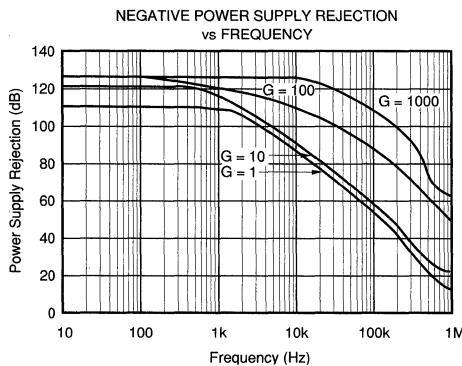
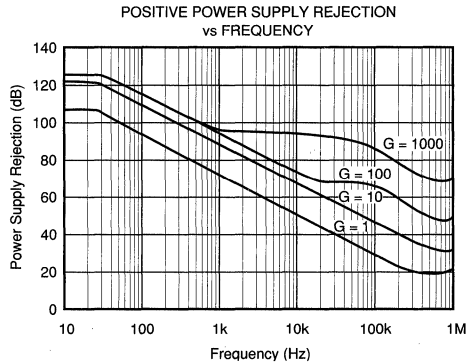
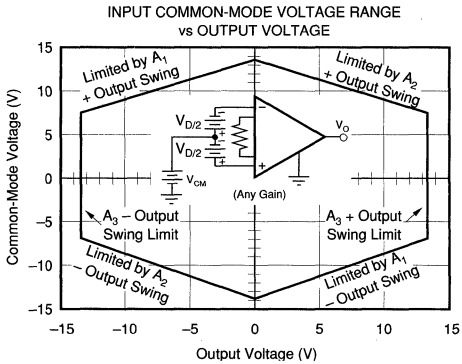
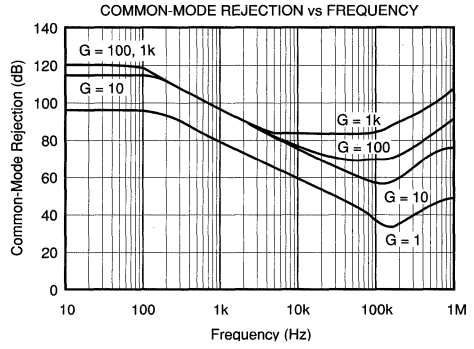
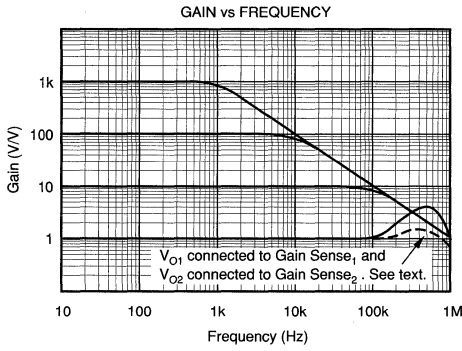
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TYPICAL PERFORMANCE CURVES

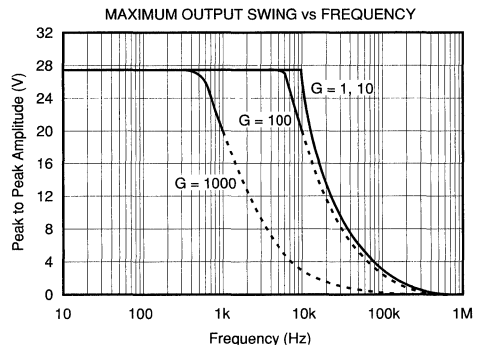
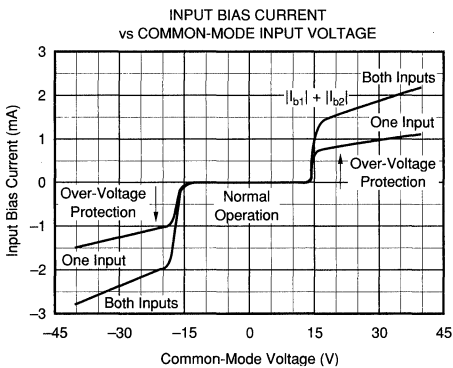
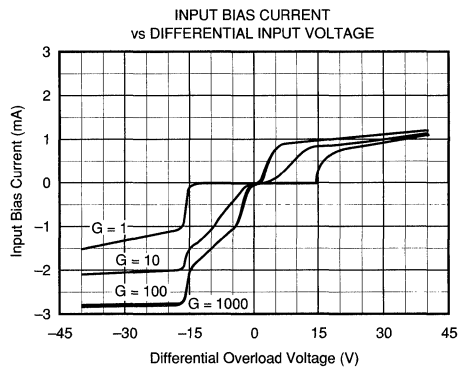
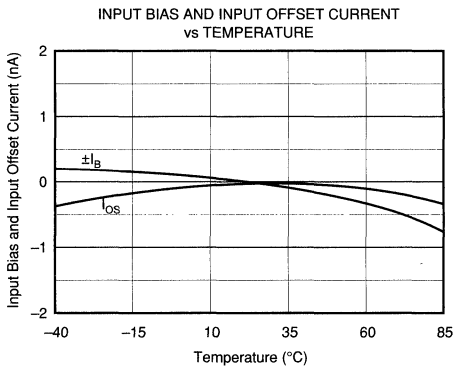
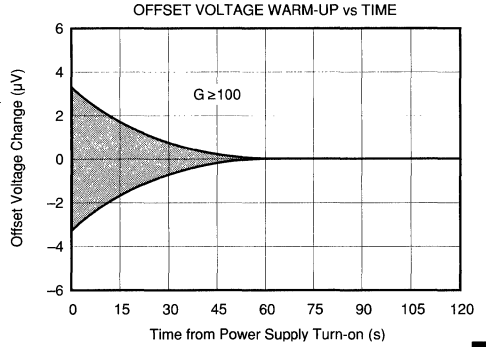
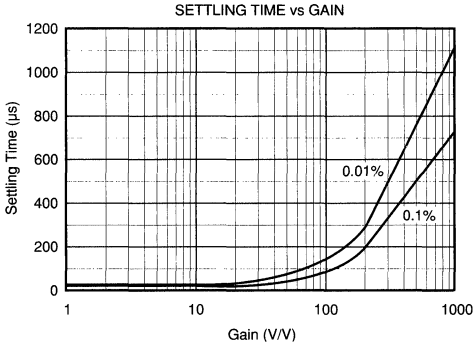
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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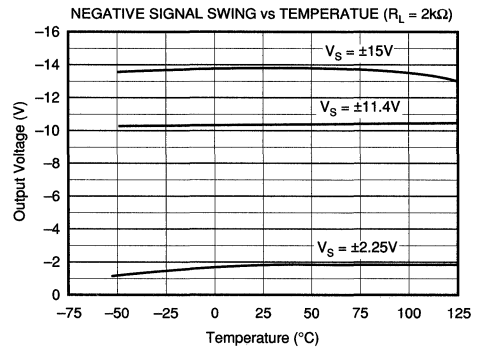
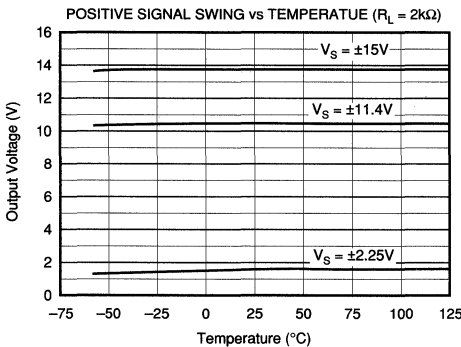
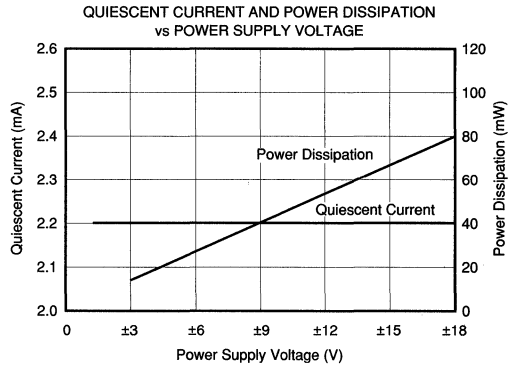
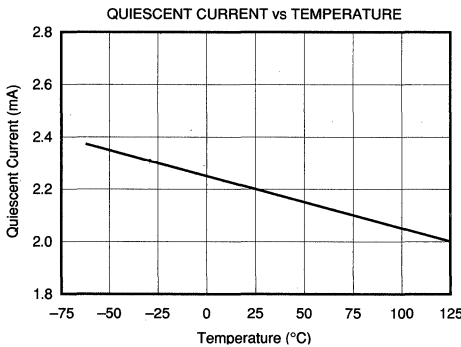
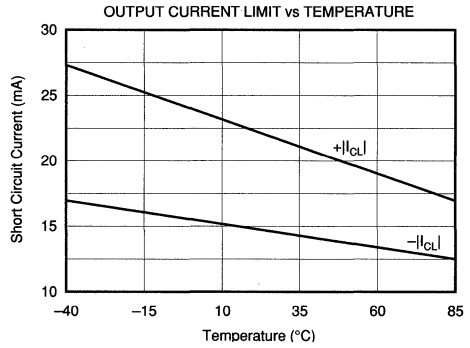
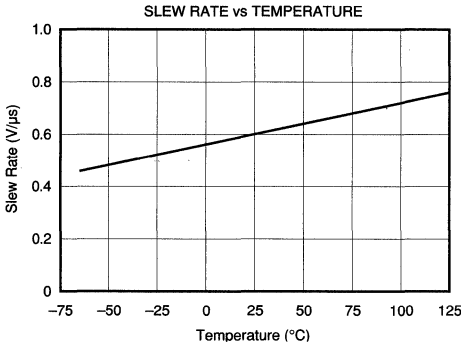
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TYPICAL PERFORMANCE CURVES (CONT)

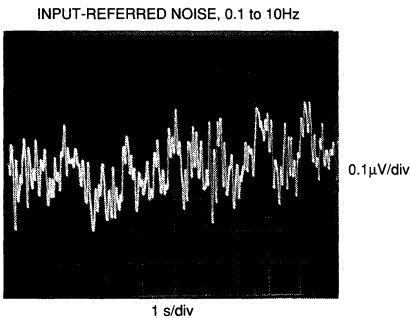
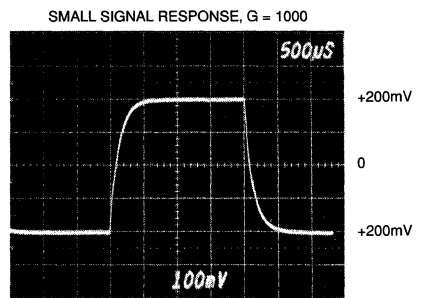
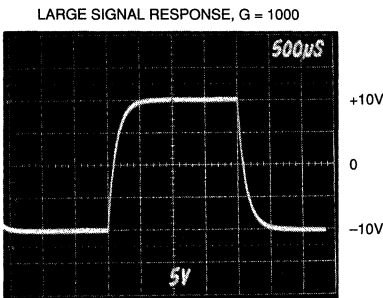
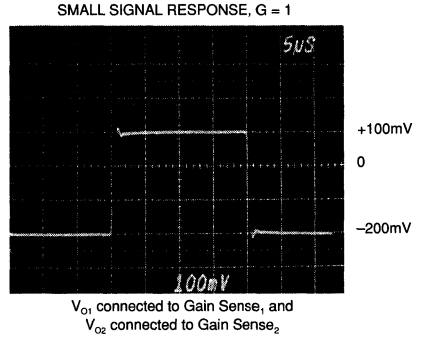
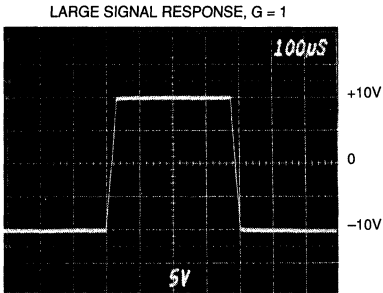
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA115. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

The INA115 has a separate output sense feedback connection (pin 12). Pin 12 must be connected (normally to the output terminal, pin 11) for proper operation. The output sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain of the INA115 is set by connecting a single external resistor, R_G :

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

For $G=1$, no resistor is required, but connect pins 2-3 and connect pins 14-15. Gain peaking in $G=1$ can be reduced by shorting the internal 25kΩ feedback resistors (see typical performance curve Gain vs Frequency). To do this, connect pins 1-2-3 and connect pins 8-14-15.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA115.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain error and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. The "force and sense" type connections illustrated in Figure 1 help reduce the effect of interconnection resistance.

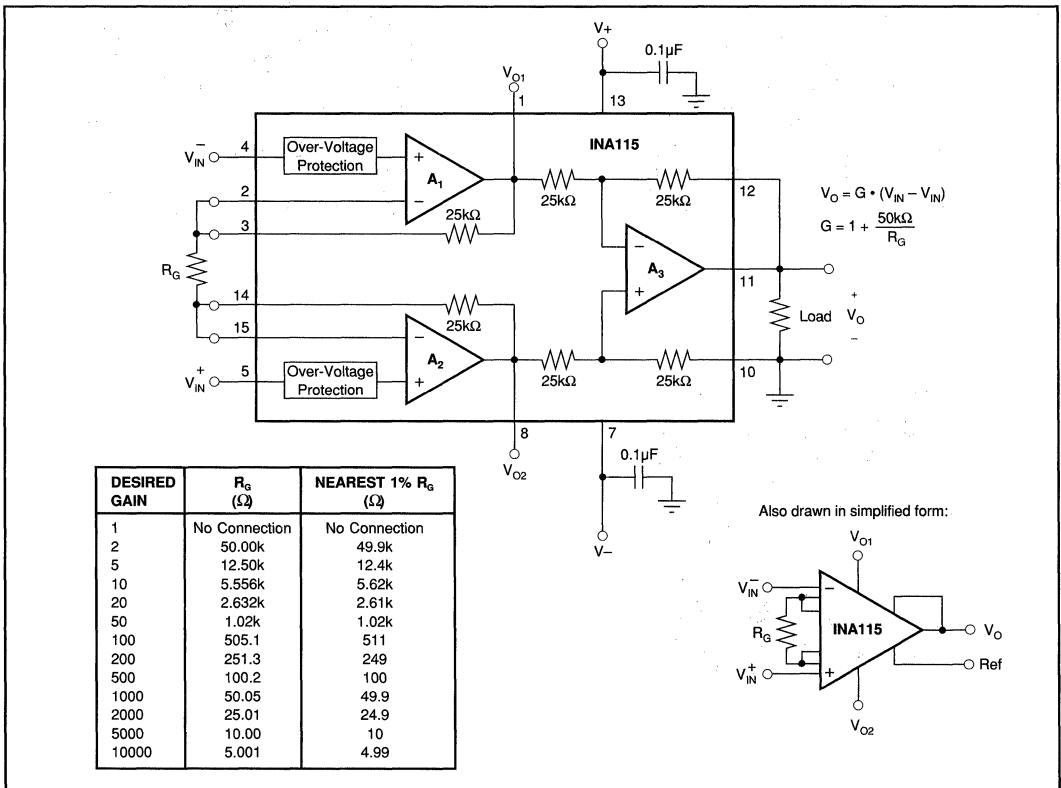


FIGURE 1. Basic Connections.

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SWITCHED GAIN

Figure 2 shows a circuit for digital selection of four gains. Multiplexer “on” resistance does not significantly affect gain. The resistor values required for some commonly used gain steps are shown. This circuit uses the internal $25\text{k}\Omega$ feedback resistors, so the resistor values shown cannot be scaled to a different impedance level.

Figure 3 shows an alternative switchable gain configuration. This circuit does not use the internal $25\text{k}\Omega$ feedback resistors, so the nominal values shown can be scaled to other impedance levels. This circuit is ideal for use with a precision resistor network to achieve excellent gain accuracy and lowest gain drift.

NOISE PERFORMANCE

The INA115 provides very low noise in most applications. For differential source impedances less than $1\text{k}\Omega$, the INA103 may provide lower noise. For source impedances greater than $50\text{k}\Omega$, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA115 is approximately $0.4\mu\text{Vp-p}$ measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

OFFSET TRIMMING

The INA115 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA115 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA115 is to operate properly. Figure 5 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA115 and the input amplifiers will saturate. If the differential source resistance is low, a bias current return path can be connected to one input (see thermocouple example in Figure 5). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

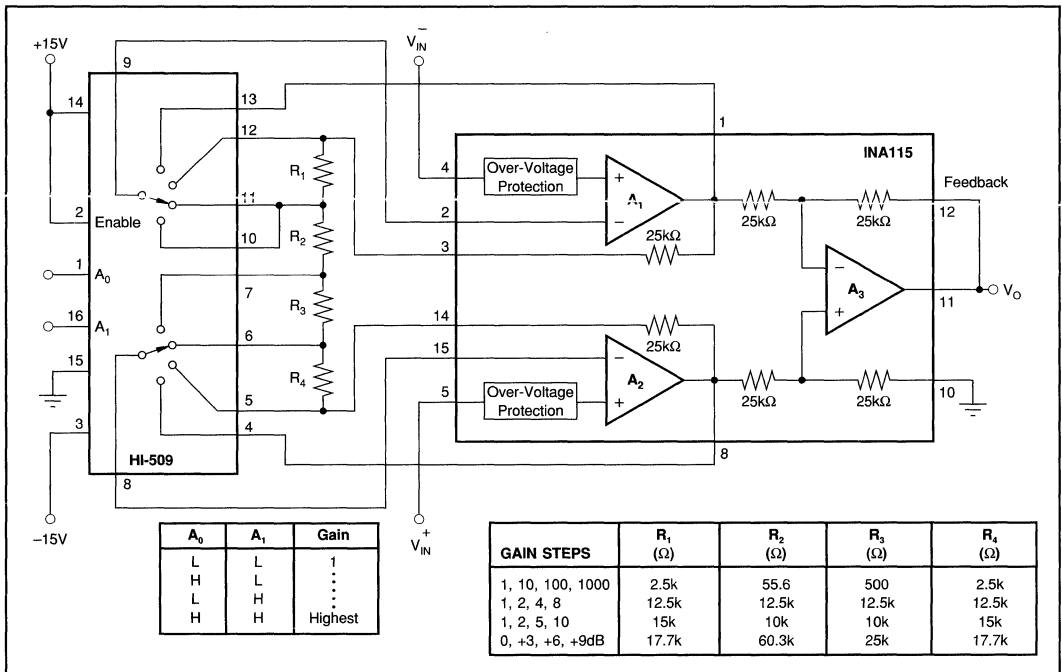


FIGURE 2. Switched-Gain Instrumentation Amplifier (minimum components).

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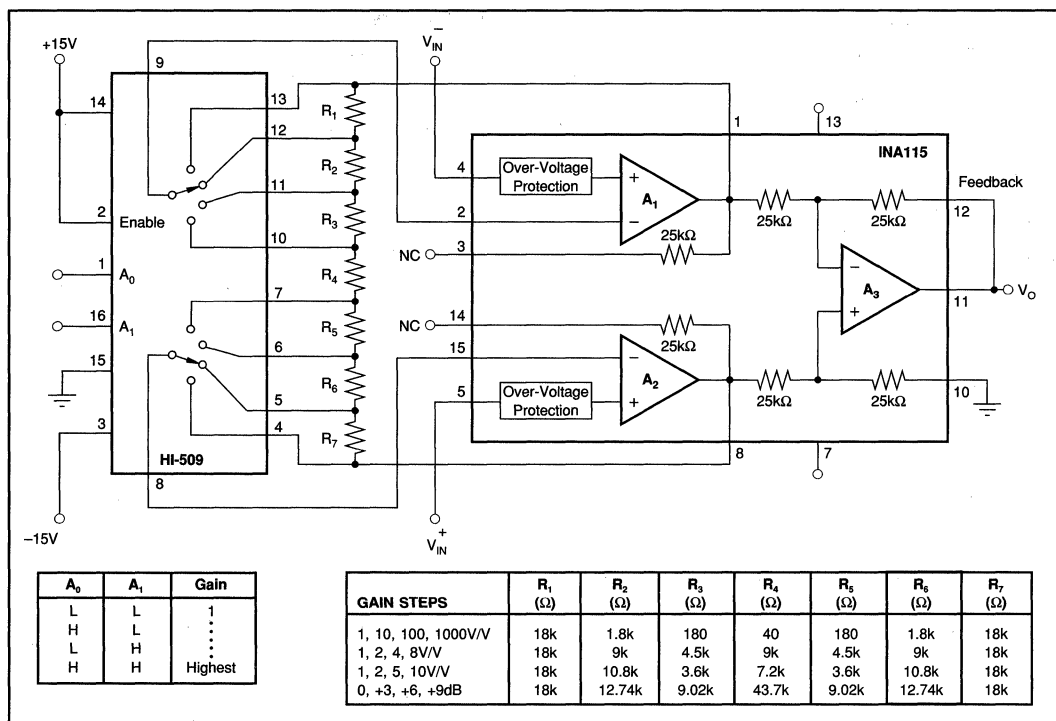


FIGURE 3. Switched-Gain Instrumentation Amplifier (improved gain drift).

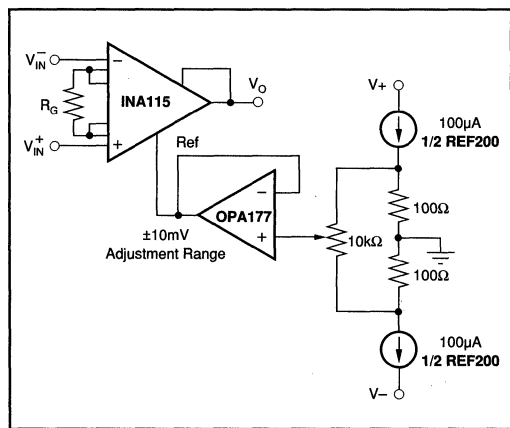


FIGURE 4. Optional Trimming of Output Offset Voltage.

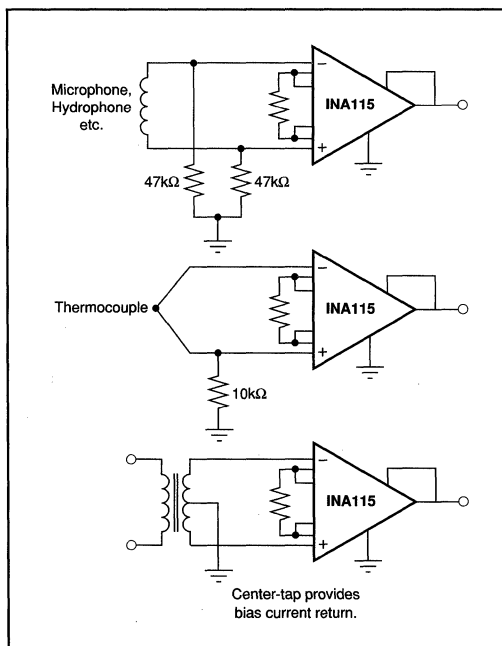


FIGURE 5. Providing an Input Common-Mode Current Path.

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INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA115 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage.”

A combination of common-mode and differential input signals can cause the output of A_1 or A_2 to saturate. Figure 6 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of the input amplifiers, A_1 and A_2 , is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA115 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA115 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of $+20\text{V}$ on one input and $+40\text{V}$ on the other input will obviously exceed the linear

common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA115 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA115 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Common-Mode Input Voltage” shows this input current limit behavior. The inputs are protected even if the power supply voltage is zero.

OTHER APPLICATIONS

See the INA114 data sheet for other applications circuits of general interest.

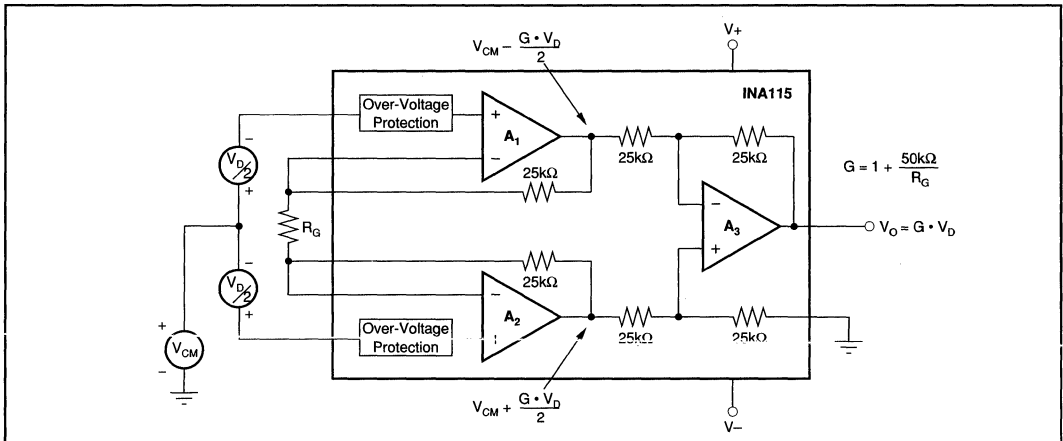


FIGURE 6. Voltage Swing of A_1 and A_2 .

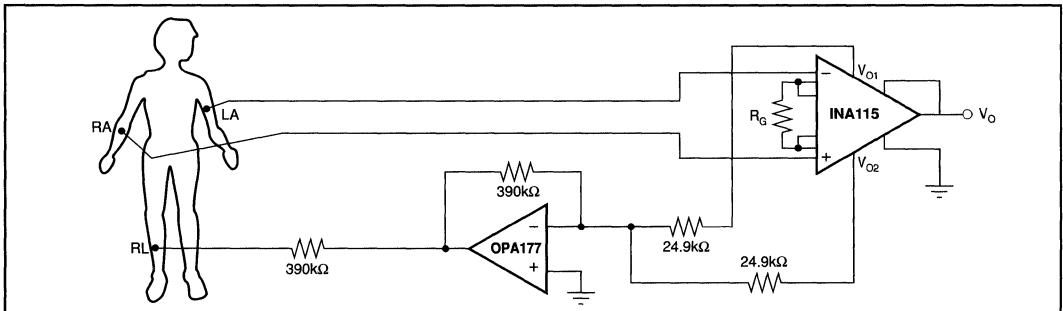
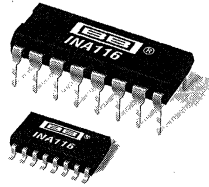


FIGURE 7. ECG Amplifier with Right Leg Drive.

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INA116

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

Electrometer Input INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW INPUT BIAS CURRENT:** 10fA
- **BUFFERED GUARD DRIVE PINS**
- **LOW OFFSET VOLTAGE:** 1mV
- **HIGH COMMON-MODE REJECTION:** 115dB (G=1000)
- **LOW QUIESCENT CURRENT:** 1mA
- **INPUT OVER-VOLTAGE PROTECTION:** $\pm 40V$

APPLICATIONS

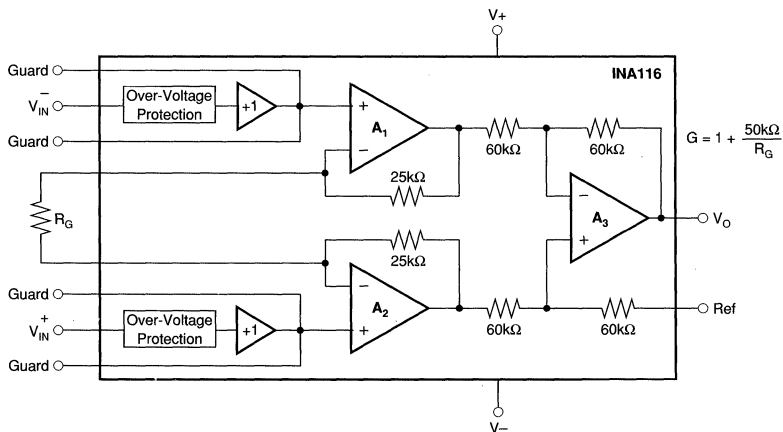
- **LABORATORY INSTRUMENTATION**
- **pH MEASUREMENT**
- **ION DETECTOR**
- **LEAKAGE CURRENT MEASUREMENT**

DESCRIPTION

The INA116 is a complete monolithic FET-input instrumentation amplifier with extremely low input bias current. *Difet*[®] inputs and special guarding techniques yield input bias currents of 10fA. Its 3-op amp topology allows gains to be set from 1 to 1000 by connecting a single external resistor.

Guard pins adjacent to both input connections can be used to drive circuit board and input cable guards to maintain extremely low input bias current.

The INA116 is available in 16-pin plastic DIP and SOL-16 surface-mount packages, specified for the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.



Difet[®]; Burr-Brown Corporation

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15V, R_L = 10kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA116P, U			INA116PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	T _A = +25°C		±0.2 ±0.5/G	±1 ±5/G		±0.2 ±0.5/G	±5 ±10/G	mV
vs Temperature	T _A = T _{MIN} to T _{MAX}		±0.5 ±2/G	±5 ±30/G		±1 ±5/G	±10 ±30/G	μV/°C
vs Power Supply	V _S = ±4.5V to ±18V		±1 ±10/G	±10 ±100/G		*	±20 ±100/G	μV/V
Long-Term Stability			±1 ±20/G			*		μV/mo
Bias Current			±10	±75		*	±150	fA
vs Temperature			Doubles Every 10°C			*		
Offset Current			±10	±75		*	±150	fA
vs Temperature			Doubles Every 10°C			*		
Impedance, Differential			>10 ¹²			*		Ω
Common-Mode			>10 ¹²			*		Ω
Linear Input Voltage Range		(V+) -4.5 (V-) +3.0	(V+) -3.5 (V-) +2.0		*	*		V
Safe Input Voltage		±40			*	*		V
Common-Mode Rejection	V _{CM} = ±10.5V, ΔR _S = 1kΩ							
	G = 1	80	90		73	*		dB
	G = 10	96	110		90	*		dB
	G = 100	106	115		100	*		dB
	G = 1000	106	115		100	*		dB
NOISE								
Voltage Noise, RTI	G = 1000, R _S = 0Ω					*		nV/√Hz
f = 1kHz			24			*		μVp-p
f _s = 0.1Hz to 10Hz			2			*		fA/√Hz
Current Noise						*		
f = 1kHz			0.2			*		
GAIN								
Gain Equation			1+(50kΩ/R _G)		*	*		V/V
Range of Gain		1		1000	*	*		V/V
Gain Error	G = 1		±0.01	±0.05	*	*		%
	G = 10		±0.25	±0.4	*	±0.5		%
	G = 100		±0.35	±0.5	*	±0.7		%
	G = 1000		±1.25	±1.75	*	±2		%
Gain vs Temperature	G = 1		±5	±10	*	±20		ppm/°C
50kΩ Resistance ⁽¹⁾			±25	±100	*	±100		ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005	*	±0.005		% of FSR
	G = 10		±0.001	±0.005	*	±0.01		% of FSR
	G = 100		±0.001	±0.005	*	±0.01		% of FSR
	G = 1000		±0.005	±0.02	*	±0.04		% of FSR
GUARD OUTPUTS								
Offset Voltage			±1	±10		*	*	mV
Output Impedance			1			*		kΩ
Current Drive			+2/-0.05			*		mA
OUTPUT								
Voltage Positive	R _L = 10kΩ	(V+) -1	(V+) -0.7		*	*		V
Negative	R _L = 10kΩ	(V-) +0.35	(V-) +0.2		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+5/-12			*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	V _O = ±10V, G = 10 to 200		0.8			*		V/μs
Settling Time, 0.01%	G = 1		22			*		μs
	G = 10		25			*		μs
	G = 100		145			*		μs
	G = 1000		400			*		μs
Overload Recovery	50% Overdrive		20			*		μs
POWER SUPPLY								
Voltage Range		±4.5	±15	±18	*	*	*	V
Current	V _{IN} = 0V		±1			*		mA
TEMPERATURE RANGE								
Specification		-40		85	*	*	*	°C
Operating		-40		125	*	*	*	°C
θ _{JA}			80			*		°C/W

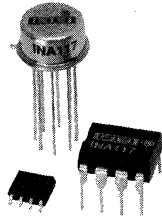
* Specification same as INA116P

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

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INA117

High Common-Mode Voltage DIFFERENCE AMPLIFIER

FEATURES

- COMMON-MODE INPUT RANGE:
 $\pm 200V$ ($V_s = \pm 15V$)
- PROTECTED INPUTS:
 $\pm 500V$ Common-Mode
 $\pm 500V$ Differential
- UNITY GAIN: 0.02% Gain Error max
- NONLINEARITY: 0.001% max
- CMRR: 86dB min

APPLICATIONS

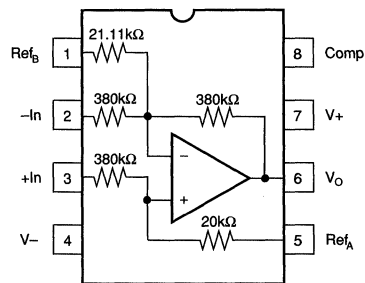
- CURRENT MONITOR
- BATTERY CELL-VOLTAGE MONITOR
- GROUND BREAKER
- INPUT PROTECTION
- SIGNAL ACQUISITION IN NOISY ENVIRONMENTS
- FACTORY AUTOMATION

DESCRIPTION

The INA117 is a precision unity-gain difference amplifier with very high common-mode input voltage range. It is a single monolithic IC consisting of a precision op amp and integrated thin-film resistor network. It can accurately measure small differential voltages in the presence of common-mode signals up to $\pm 200V$. The INA117 inputs are protected from momentary common-mode or differential overloads up to $\pm 500V$.

In many applications, where galvanic isolation is not essential, the INA117 can replace isolation amplifiers. This can eliminate costly isolated input-side power supplies and their associated ripple, noise and quiescent current. The INA117's 0.001% nonlinearity and 200kHz bandwidth are superior to those of conventional isolation amplifiers.

The INA117 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the $0^\circ C$ to $+70^\circ C$ temperature range. The metal TO-99 models are available specified for the $-25^\circ C$ to $+85^\circ C$ and $-55^\circ C$ to $+125^\circ C$ temperature range.



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	INA117AM, SM			INA117BM			INA117P, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Initial ⁽¹⁾			1			*			*		V/V
Error vs Temperature			0.01	0.05		*	0.02		*	*	%
Nonlinearity ⁽²⁾			2	10		*	*		*	*	ppm/°C
			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	$I_O = +20\text{mA}, -5\text{mA}$	10	12		*	*		*	*		V
Rated Current	$V_O = 10\text{V}$	+20, -5			*	*		*	*		mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+49, -13			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance	Differential		800			*			*		k Ω
	Common-Mode		400			*			*		k Ω
Voltage Range	Differential	± 10				*			*		V
	Common-Mode, Continuous	± 200			*	*			*		V
Common-Mode Rejection ⁽³⁾						*			*		dB
DC		70	80		86	94		*	*		dB
AC, 60Hz	$V_{CM} = 400\text{Vp-p}$	66	80		66	94		*	*		dB
vs Temperature, DC	$T_A = T_{MIN}$ to T_{MAX}	66	75		80	90		*	*		dB
AM, BM, P, KU		60	75								dB
SM											dB
OFFSET VOLTAGE											
Initial	RTO ⁽⁴⁾		120	1000		*	1000		*	*	μV
KU Grade (SO-8 Package)						*			*	*	μV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		8.5	40		*	20		*	*	$\mu\text{V}/^\circ\text{C}$
vs Supply	$V_S = \pm 5\text{V}$ to $\pm 18\text{V}$	74	90		80	*			*	*	dB
vs Time			200			*			*	*	$\mu\text{V}/\text{mo}$
OUTPUT NOISE VOLTAGE											
$f_B = 0.01\text{Hz}$ to 10Hz	RTO ⁽⁵⁾		25			*			*		$\mu\text{Vp-p}$
$f_B = 10\text{kHz}$			550			*			*		nV/ $\sqrt{\text{Hz}}$
DYNAMIC RESPONSE											
Gain Bandwidth, -3dB			200			*			*		kHz
Full Power Bandwidth	$V_O = 20\text{Vp-p}$	30			*	*		*	*		kHz
Slew Rate		2	2.6		*	*		*	*		V/ μs
Settling Time: 0.1%	$V_O = 10\text{V Step}$		6.5			*			*		μs
0.01%	$V_O = 10\text{V Step}$		10			*			*		μs
0.01%	$V_{CM} = 10\text{V Step}, V_{DIFF} = 0\text{V}$		4.5			*			*		μs
POWER SUPPLY											
Rated			± 15			*			*		V
Voltage Range	Derated Performance	± 5		± 18	*	*		*	*		V
Quiescent Current	$V_O = 0\text{V}$		1.5	2		*	*		*		mA
TEMPERATURE RANGE											
Specification: AM, BM, P, KU		-25		+85	*	*		0		+70	$^\circ\text{C}$
SM		-55		+125	*	*					$^\circ\text{C}$
Operation		-55		+125	*	*		-25		+85	$^\circ\text{C}$
Storage		-65		+150	*	*		-40		+85	$^\circ\text{C}$

*Specification same as for INA117AM.

NOTES: (1) Connected as difference amplifier (see Figure 1). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) With zero source impedance (see discussion of common-mode rejection in Application Information section). (4) Includes effects of amplifier's input bias and offset currents. (5) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

INA117

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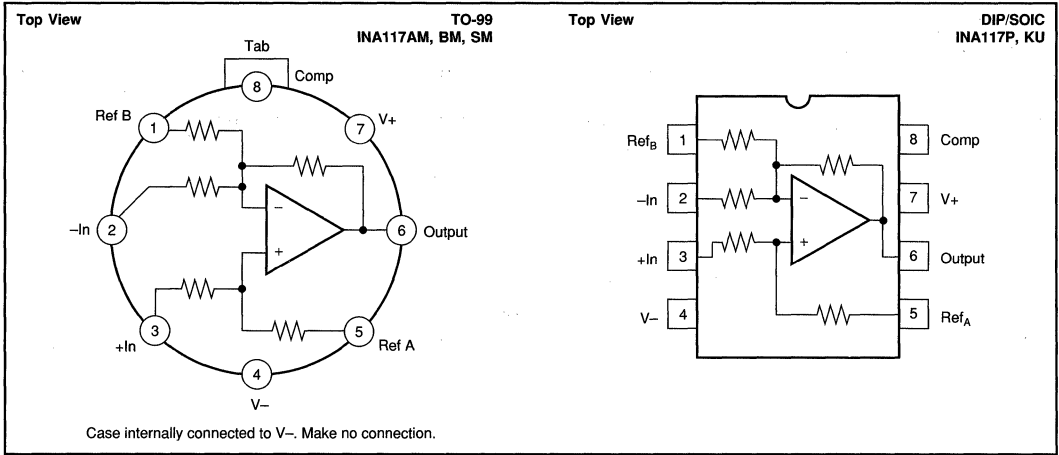
INSTRUMENTATION AMPLIFIERS

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage Range, Continuous	±200V
Common-Mode and Differential, 10s	±500V
Operating Temperature	
M Metal TO-99	-55 to +125°C
P Plastic DIP and U SO-8	-40 to +85°C
Storage Temperature	
M Package	-65 to +150°C
P Plastic DIP and U SO-8	-40 to +85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common	Continuous

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA117P	8-Pin Plastic DIP	006
INA117KU	SO-8 Surface Mount	182
INA117AM	TO-99 Metal	001
INA117BM	TO-99 Metal	001
INA117SM	TO-99 Metal	001

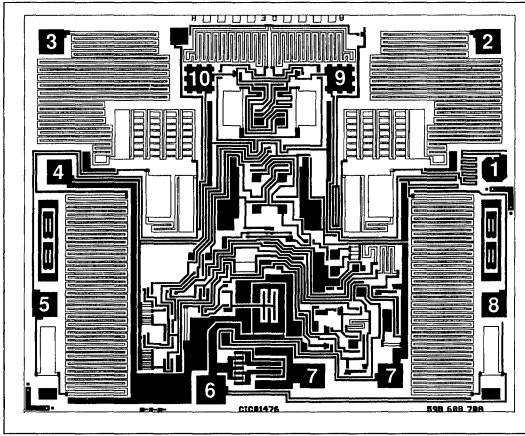
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA117P	8-Pin Plastic DIP	0°C to +70°C
INA117KU	SO-8 Surface-Mount	0°C to +70°C
INA117AM	TO-99 Metal	-25°C to +85°C
INA117BM	TO-99 Metal	-25°C to +85°C
INA117SM	TO-99 Metal	-55°C to +125°C

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DICE INFORMATION



INA117 DIE TOPOGRAPHY

PAD	FUNCTION
1	Ref B
2	-In
3	+In
4	V-
5	Ref A
6	Output
7	V+ (connect both pads)
8	Comp
9	(Op Amp -In)
10	(Op Amp +In)

Substrate Bias: Electrically connected to -V supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	85 x 103 ±5	2.16 x 2.62 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.01 x 0.01
Backing		Gold

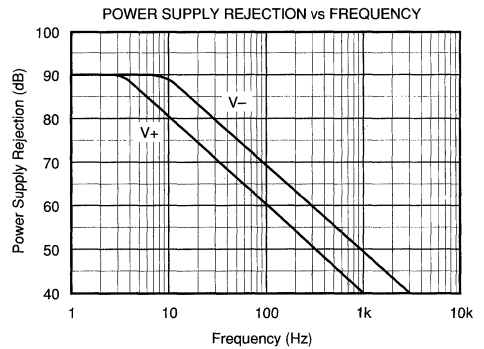
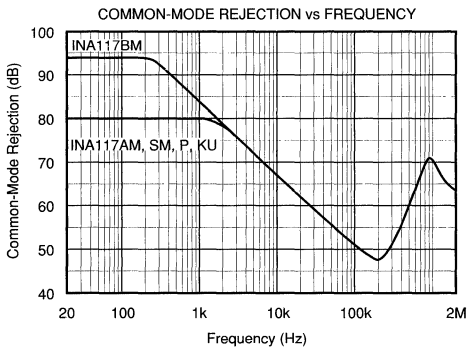
INA117

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INSTRUMENTATION AMPLIFIERS

TYPICAL PERFORMANCE CURVES

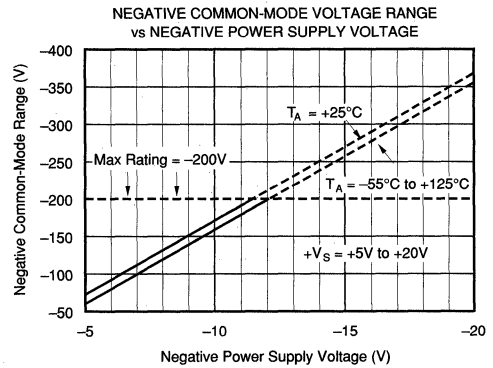
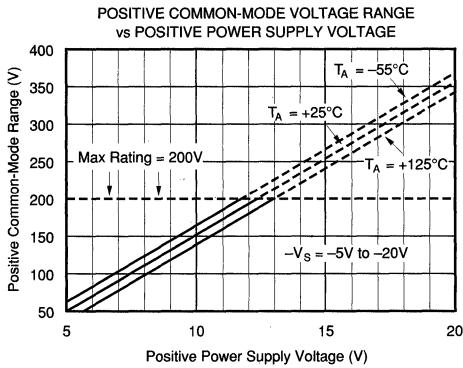
T_A = +25°C, V_S = ±15V, unless otherwise noted.



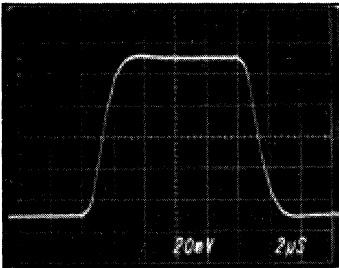
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TYPICAL PERFORMANCE CURVES (CONT)

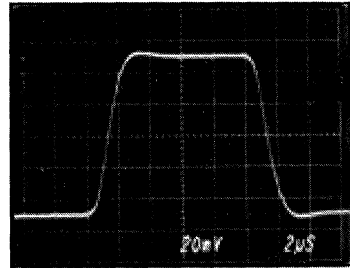
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



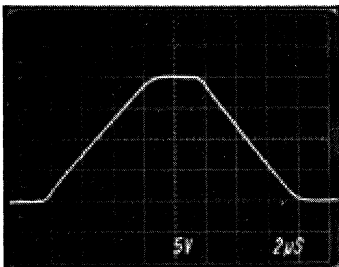
SMALL SIGNAL STEP RESPONSE
 $C_L = 0$



SMALL SIGNAL STEP RESPONSE
 $C_L = 1000\text{pF}$



LARGE SIGNAL STEP RESPONSE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation.

Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins.

The output voltage is equal to the differential input voltage between pins 2 and 3. The common mode input voltage is rejected.

Internal circuitry connected to the compensation pin 8 cancels the parasitic distributed capacitance between the feedback resistor, R_2 , and the IC substrate. For specified dynamic performance, pin 8 should be grounded or connected through a 0.1 μ F capacitor to an AC ground such as V_+ .

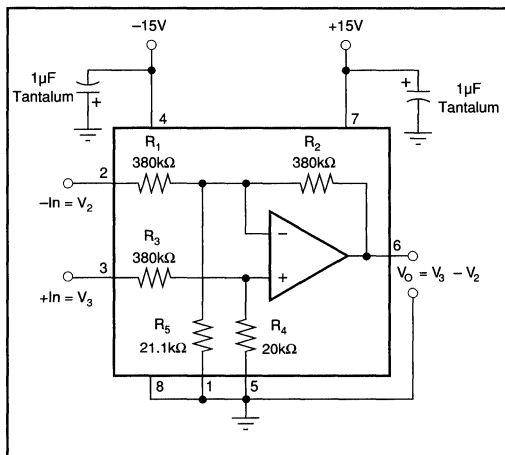


FIGURE 1. Basic Power and Signal Connections.

COMMON-MODE REJECTION

Common-mode rejection (CMR) of the INA117 is dependent on the input resistor network, which is laser-trimmed for accurate ratio matching. To maintain high CMR, it is important to have low source impedances driving the two inputs. A 75 Ω resistance in series with pin 2 or 3 will decrease CMR from 86dB to 72dB.

Resistance in series with the reference pins will also degrade CMR. A 4 Ω resistance in series with pin 1 or 5 will decrease CMRR from 86dB to 72dB.

Most applications do not require trimming. Figures 2 and 3 show optional circuits that may be used for trimming offset voltage and common-mode rejection.

TRANSFER FUNCTION

Most applications use the INA117 as a simple unity-gain difference amplifier. The transfer function is:

$$V_o = V_3 - V_2$$

V_3 and V_2 are the voltages at pins 3 and 2.

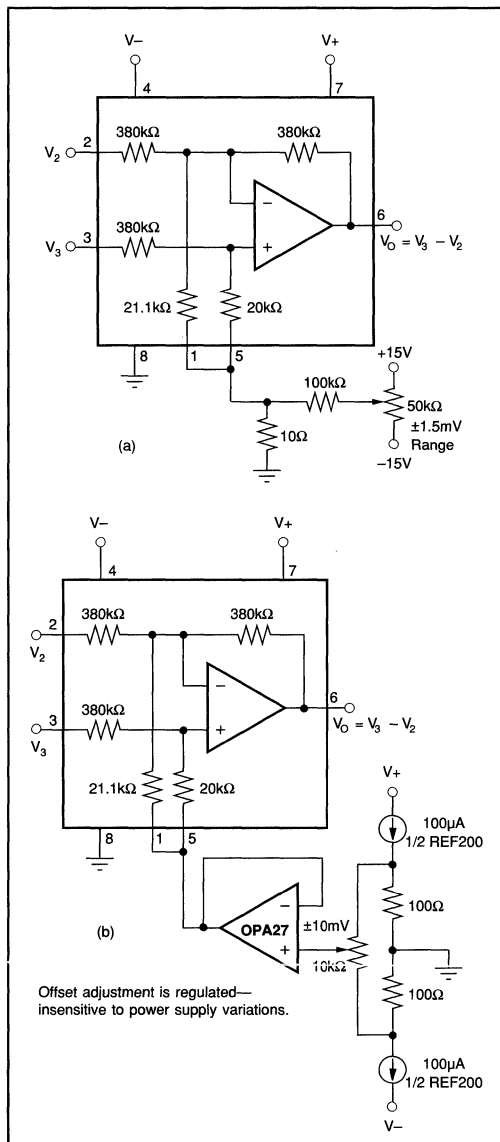


FIGURE 2. Offset Voltage Trim Circuits.

Some applications, however, apply voltages to the reference terminals (pins 1 and 5). A more complete transfer function is:

$$V_o = V_3 - V_2 + 19 \cdot V_5 - 18 \cdot V_1$$

V_5 and V_1 are the voltages at pins 5 and 1.

MEASURING CURRENT

The INA117 can be used to measure a current by sensing the voltage drop across a series resistor, R_S . Figure 4 shows the INA117 used to measure the supply currents of a device under test. The circuit in Figure 5 measures the output current of a power supply. If the power supply has a sense connection, it can be connected to the output side of R_S to eliminate the voltage-drop error. Another common application is current-to-voltage conversion as shown in Figure 6.

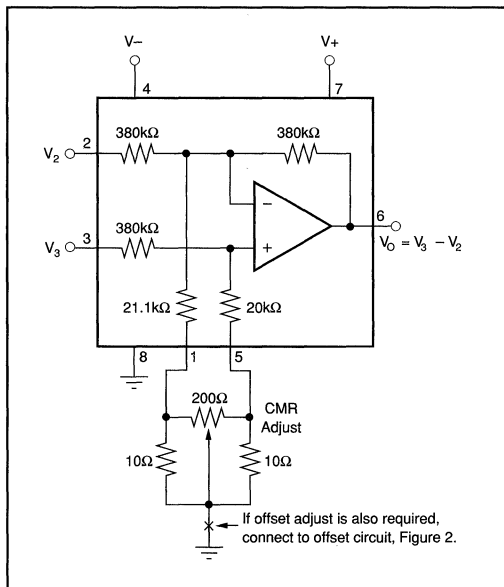


FIGURE 3. CMR Trim Circuit.

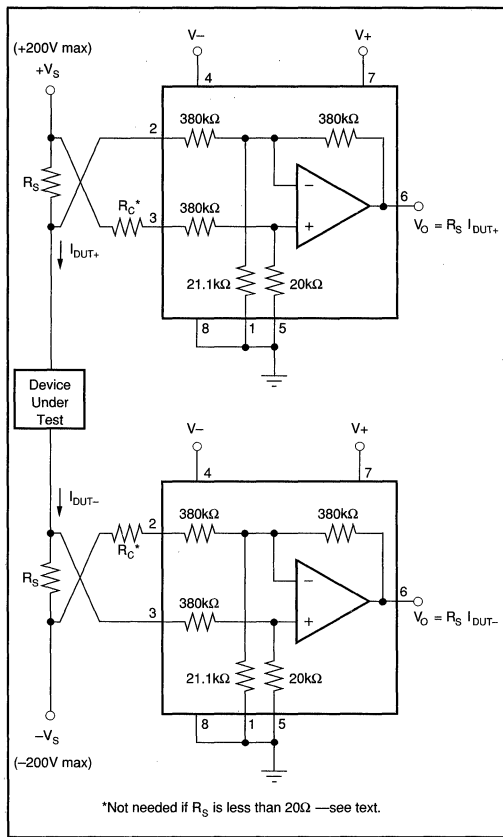


FIGURE 4. Measuring Supply Currents of Device Under Test.

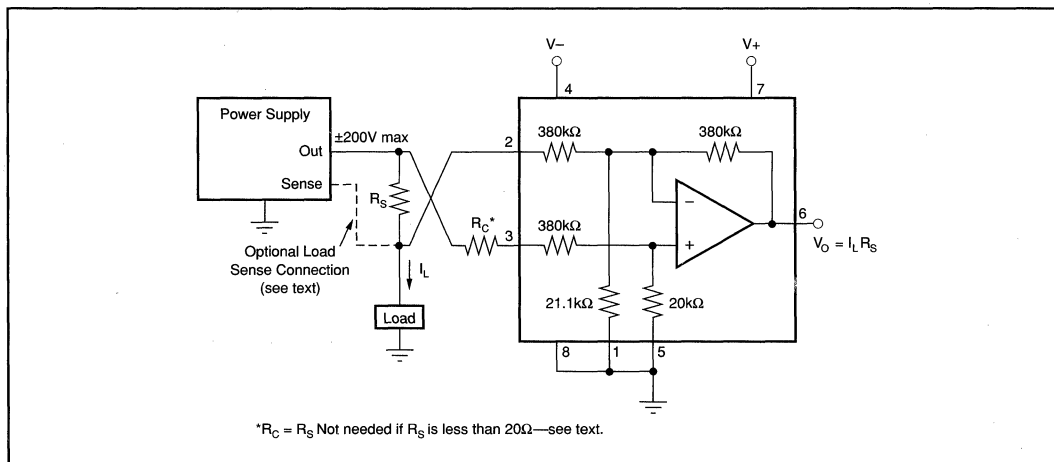


FIGURE 5. Measuring Power Supply Output Current.

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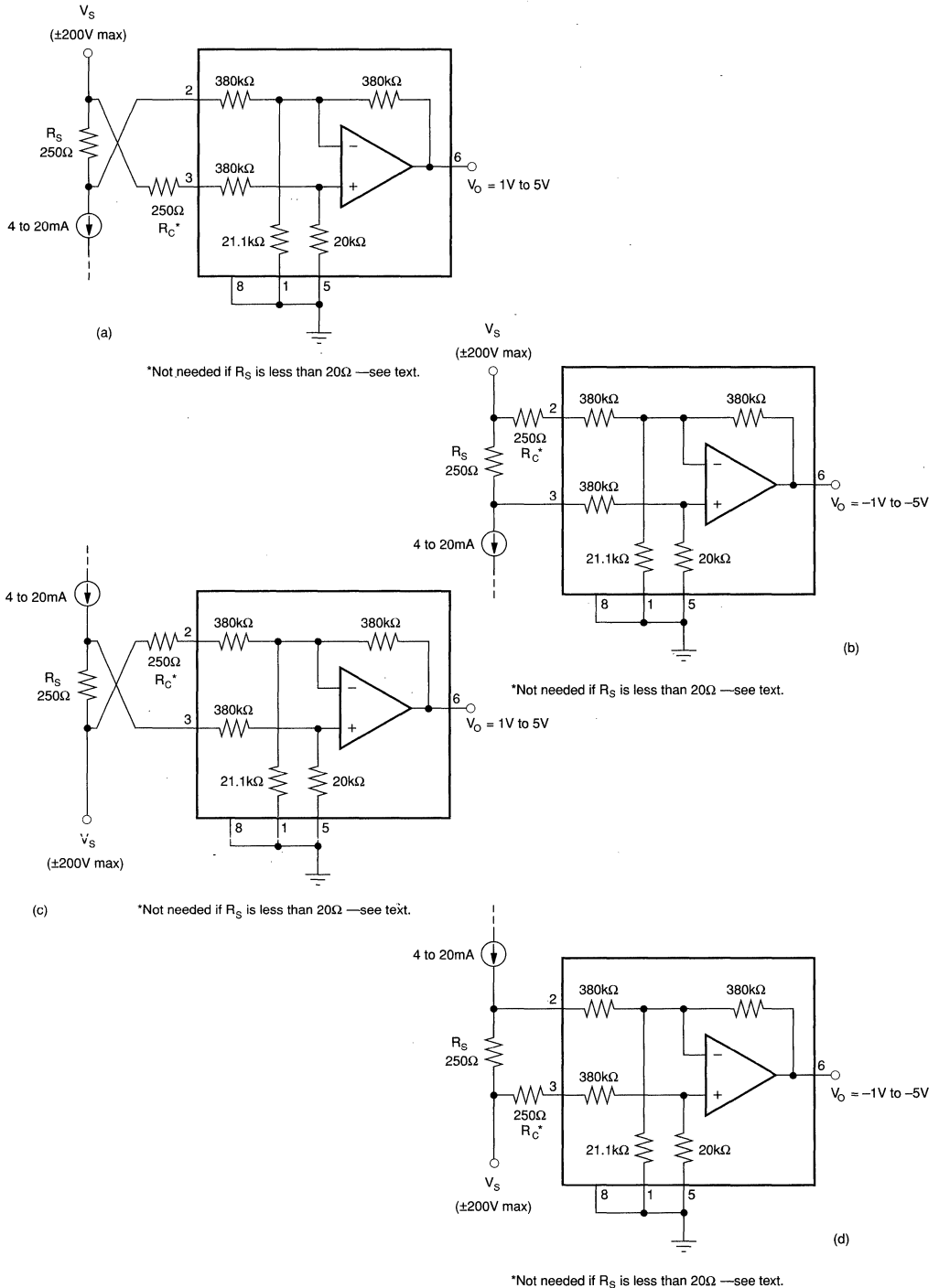


FIGURE 6. Current to Voltage Converter.



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In all cases, the sense resistor imbalances the input resistor matching of the INA117, degrading its CMR. Also, the input impedance of the INA117 loads R_s , causing gain error in the voltage-to-current conversion. Both of these errors can be easily corrected.

The CMR error can be corrected with the addition of a compensation resistor, R_c , equal in value to R_s as shown in Figures 4, 5, and 6. If R_s is less than 20Ω , the degradation in CMR is negligible and R_c can be omitted. If R_s is larger than approximately $2k\Omega$, trimming R_c may be required to achieve greater than 86dB CMR. This is because the actual INA117 input impedances have 1% typical mismatch.

If R_s is more than approximately 100Ω , the gain error will be greater than the 0.02% specification of the INA117. This gain error can be corrected by slightly increasing the value of R_s . The corrected value, R_s' , can be calculated by—

$$R_s' = \frac{R_s + 380k\Omega}{380k\Omega - R_s}$$

Example: For a 1V/mA transfer function, the nominal, uncorrected value for R_s would be $1k\Omega$. A slightly larger value, $R_s' = 1002.6\Omega$, compensates for the gain error due to loading.

The $380k\Omega$ term in the equation for R_s' has a tolerance of $\pm 25\%$, so sense resistors above approximately 400Ω may require trimming to achieve gain accuracy better than 0.02%.

Of course, if a buffer amplifier is added as shown in Figure 7, both inputs see a low source impedance, and the sense resistor is not loaded. As a result, there is no gain error or CMR degradation. The buffer amplifier can operate as a unity gain buffer or as an amplifier with noninverting gain. Gain added ahead of the INA117 improves both CMR and signal-to-noise. Added gain also allows a lower voltage drop across the sense resistor. The OPA1013 is a good choice for the buffer amplifier since both its input and output can swing close to its negative power supply.

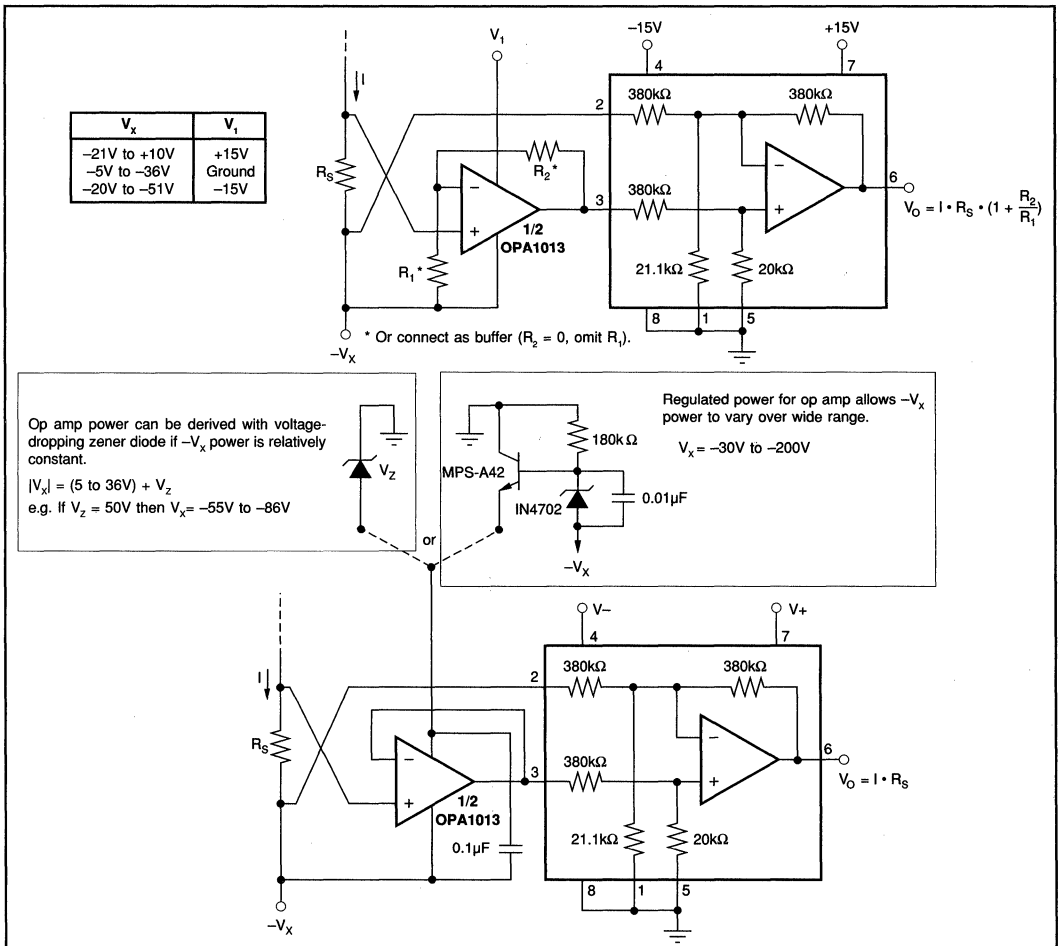


FIGURE 7. Current Sensing with Input Buffer.

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Figure 8 shows very high input impedance buffer used to measure low leakage currents. Here, the buffer op amp is powered with an isolated, split-voltage power supply. Using an isolated power supply allows full $\pm 200V$ common-mode input range.

NOISE PERFORMANCE

The noise performance of the INA117 is dominated by the internal resistor network. The thermal or Johnson noise of

these resistors produces approximately $550nV/\sqrt{Hz}$ noise. The internal op amp contributes virtually no excess noise at frequencies above 100Hz.

Many applications may be satisfied with less than the full 200kHz bandwidth of the INA117. In these cases, the noise can be reduced with a low-pass filter on the output. The two-pole filter shown in Figure 9 limits bandwidth to 1kHz and reduces noise by more than 15:1. Since the INA117 has a $1/f$ noise corner frequency of approximately 100Hz, a cutoff frequency below 100Hz will not further reduce noise.

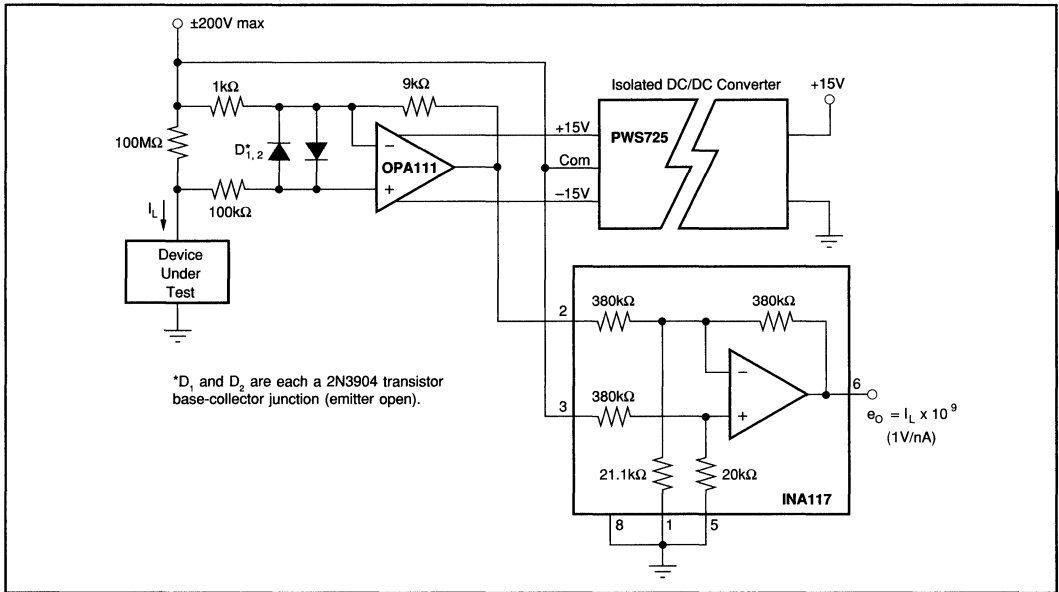
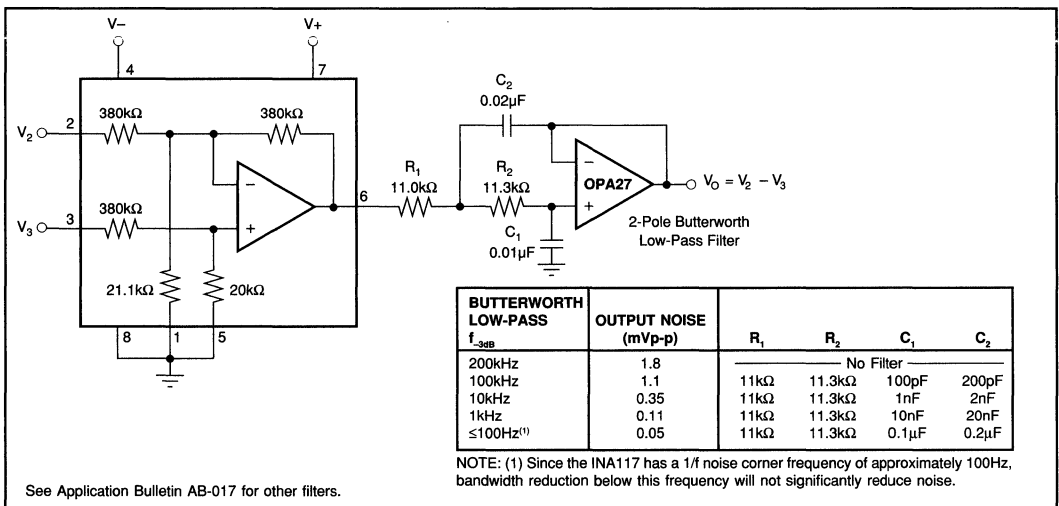


FIGURE 8. Leakage Current Measurement Circuit.



See Application Bulletin AB-017 for other filters.

FIGURE 9. Output Filter for Noise Reduction.

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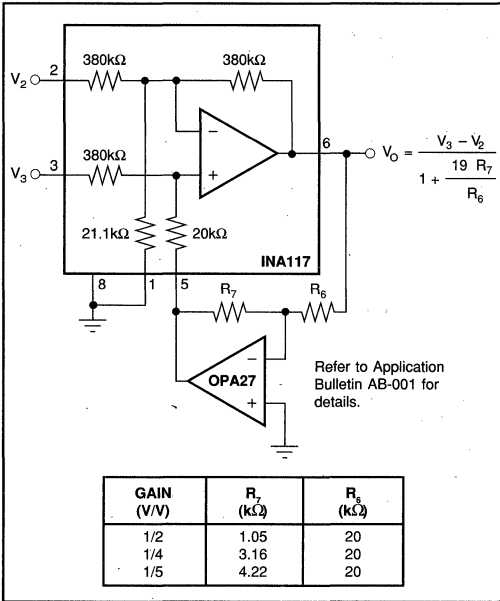


FIGURE 10. Reducing Differential Gain.

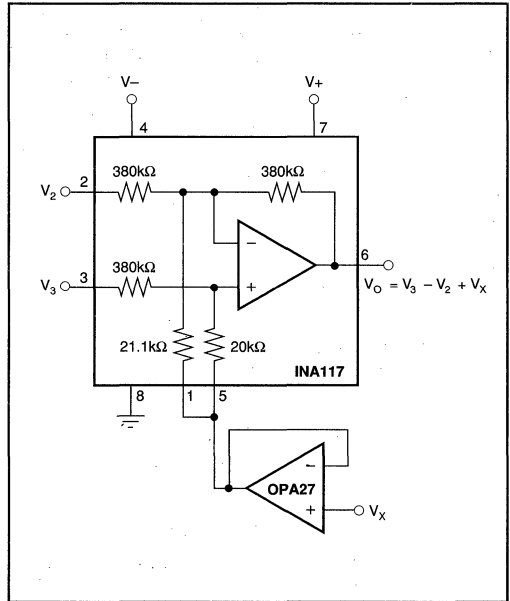


FIGURE 11. Summing V_x in Output.

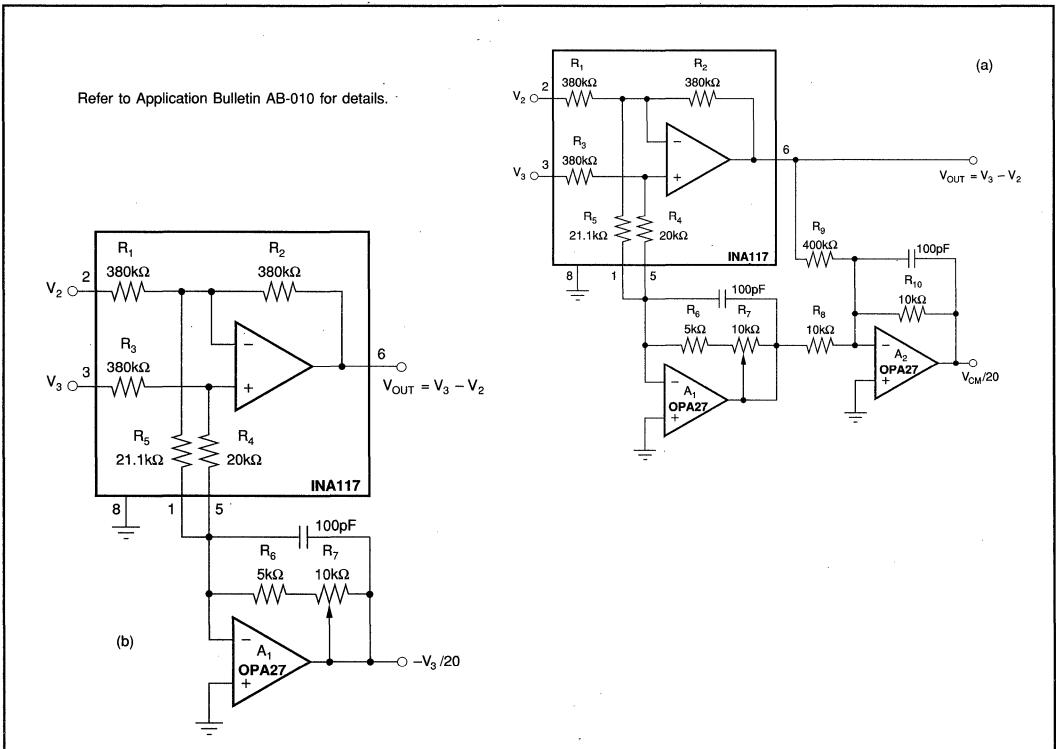


FIGURE 12. Common-Mode Voltage Monitoring.

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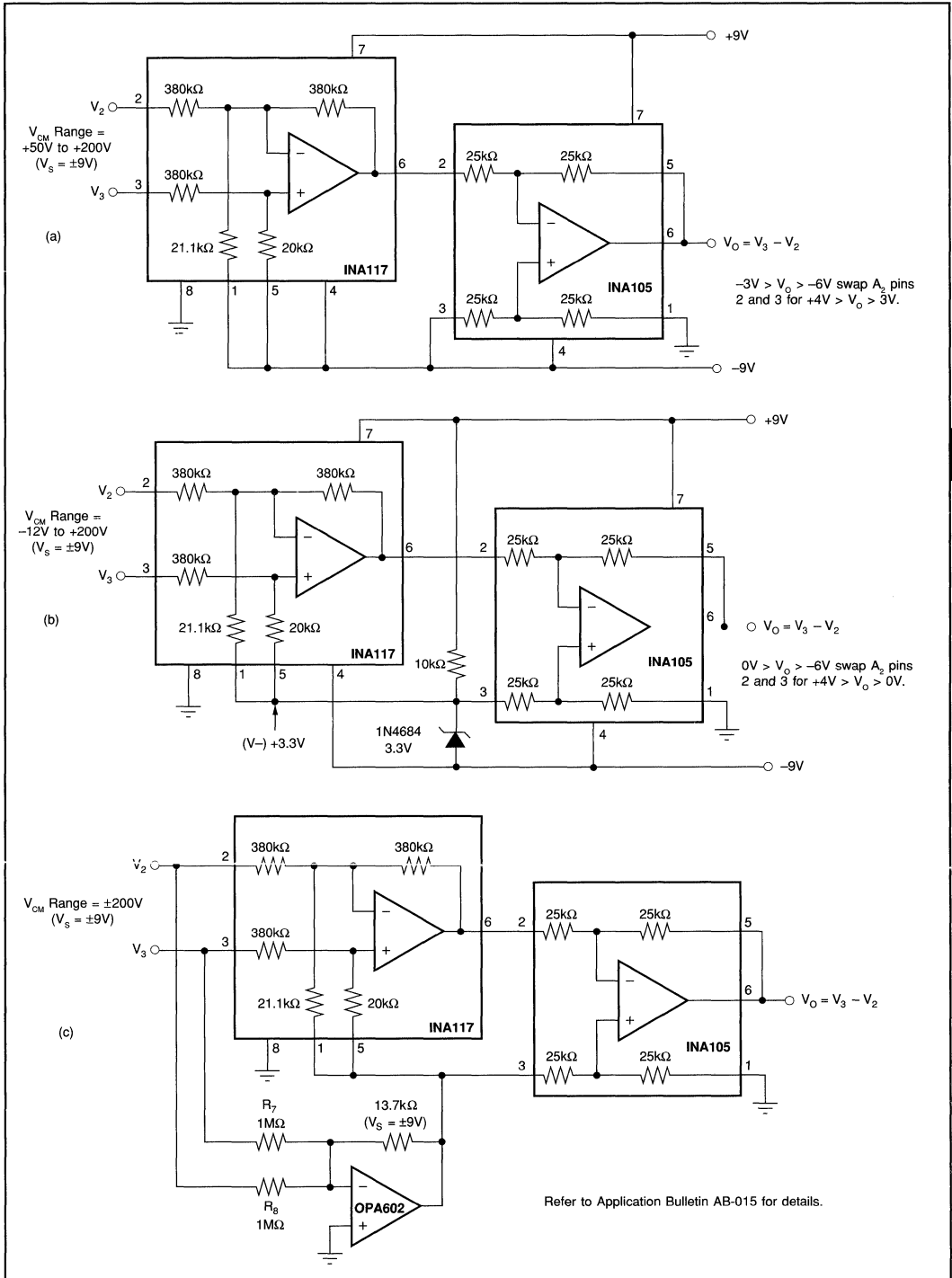


FIGURE 13. Offsetting or Boosting Common-Mode Voltage Range for Reduced Power Supply Voltage Operation.

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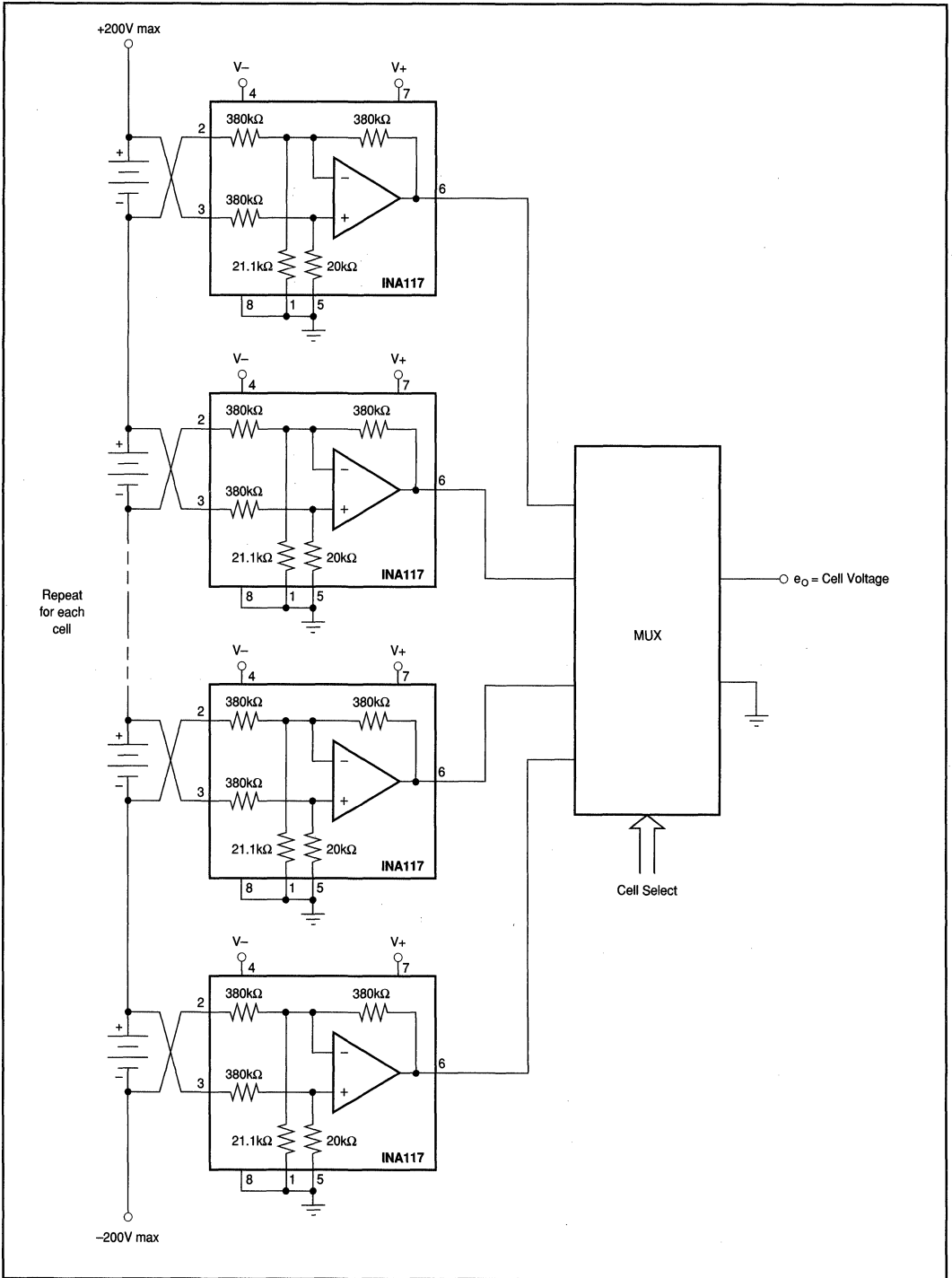


FIGURE 14. Battery Cell Voltage Monitor.

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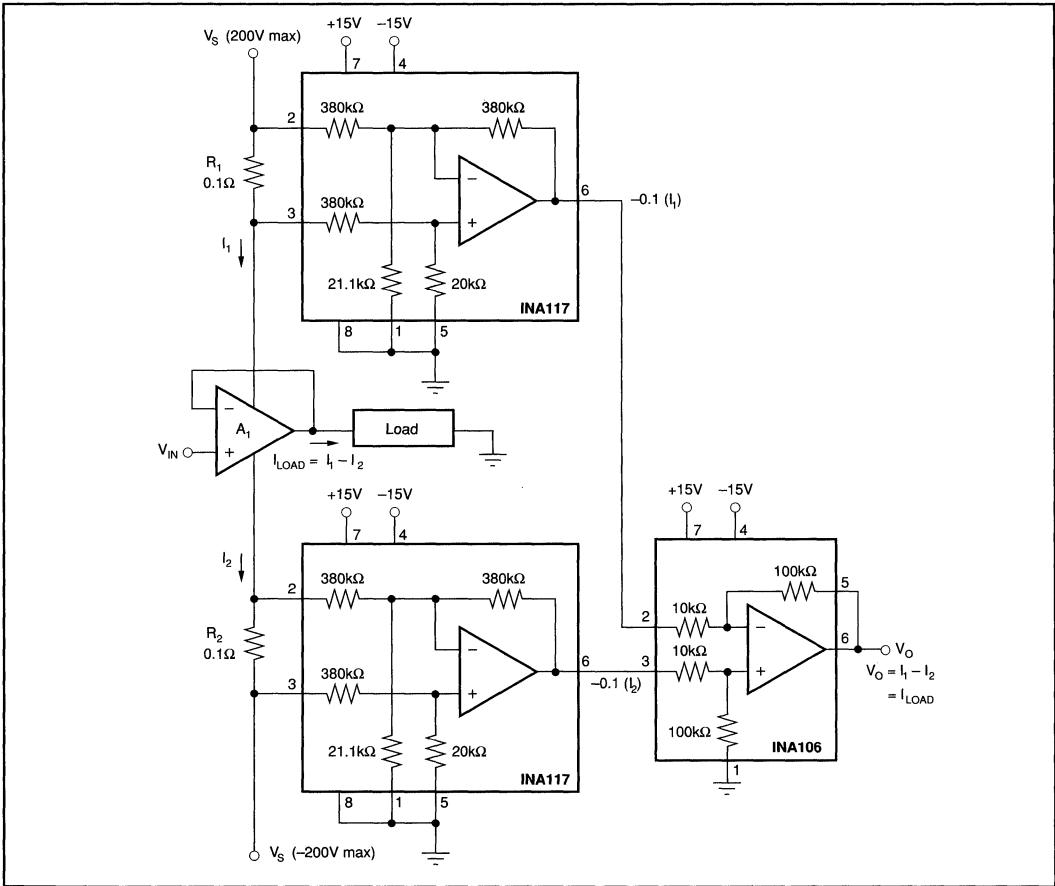


FIGURE 15. Measuring Amplifier Load Current.

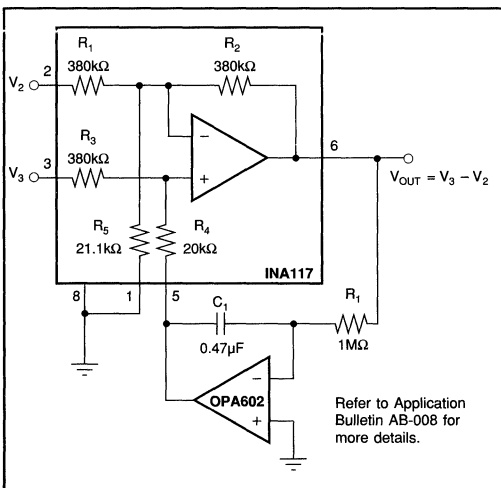


FIGURE 16. AC-Coupled INA117.

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INA118



Precision, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50 μ V max
- LOW DRIFT: 0.5 μ V/ $^{\circ}$ C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO \pm 40V
- WIDE SUPPLY RANGE: \pm 1.35 to \pm 18V
- LOW QUIESCENT CURRENT: 350 μ A
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

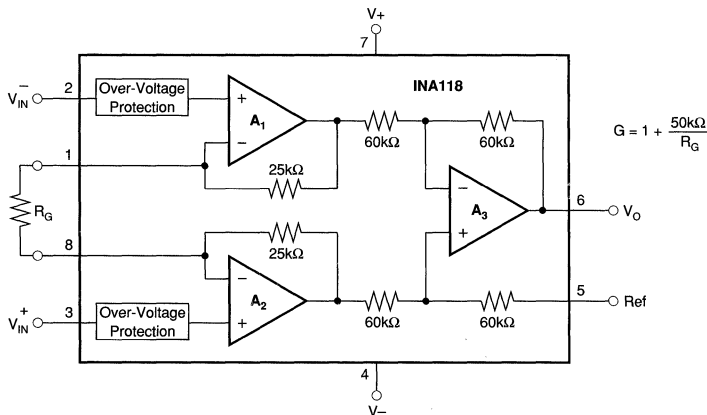
DESCRIPTION

The INA118 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (70kHz at G=100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to \pm 40V without damage.

The INA118 is laser trimmed for very low offset voltage (50 μ V), drift (0.5 μ V/ $^{\circ}$ C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as \pm 1.35V, and quiescent current is only 350 μ A—ideal for battery operated systems.

The INA118 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the -40° C to $+85^{\circ}$ C temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	INA118PB, UB			INA118P, U			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								
Initial	$T_A = +25^\circ\text{C}$		$\pm 10 \pm 50/\text{G}$	$\pm 50 \pm 500/\text{G}$		$\pm 25 \pm 100/\text{G}$	$\pm 125 \pm 1000/\text{G}$	μV
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}		$\pm 0.2 \pm 2/\text{G}$	$\pm 0.5 \pm 20/\text{G}$		$\pm 0.2 \pm 5/\text{G}$	$\pm 1 \pm 20/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 1.35\text{V}$ to $\pm 18\text{V}$		$\pm 1 \pm 10/\text{G}$	$\pm 5 \pm 100/\text{G}$		*	$\pm 10 \pm 100/\text{G}$	$\mu\text{V}/\text{V}$
Long-Term Stability			$\pm 0.4 \pm 5/\text{G}$			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^9 \parallel 1$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{10} \parallel 4$			*		$\Omega \parallel \text{pF}$
Linear Input Voltage Range		$(V+) - 1$ $(V-) + 1.1$	$(V+) - 0.65$ $(V-) + 0.95$		*	*		V
Safe Input Voltage				± 40			*	V
Common-Mode Rejection	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$							
	G = 1	80	90		73	*		dB
	G = 10	97	110		89	*		dB
	G = 100	107	120		98	*		dB
	G = 1000	110	125		100	*		dB
BIAS CURRENT								
vs Temperature			± 1 ± 40	± 5		*	± 10	nA pA/°C
OFFSET CURRENT								
vs Temperature			± 1 ± 40	± 5		*	± 10	nA pA/°C
NOISE VOLTAGE, RTI								
f = 10Hz	G = 1000, $R_S = 0\Omega$		11			*		nV/√Hz
f = 100Hz			10			*		nV/√Hz
f = 1kHz			10			*		nV/√Hz
$f_B = 0.1\text{Hz}$ to 10Hz			0.28			*		$\mu\text{Vp-p}$
Noise Current								
f = 10Hz			2.0			*		pA/√Hz
f = 1kHz			0.3			*		pA/√Hz
$f_B = 0.1\text{Hz}$ to 10Hz			80			*		pAp-p
GAIN								
Gain Equation		1	$1 + (50\text{k}\Omega/R_G)$	10000	*	*	*	V/V
Range of Gain								V/V
Gain Error	G = 1		± 0.01	± 0.024		*	± 0.1	%
	G = 10		± 0.02	± 0.4		*	± 0.5	%
	G = 100		± 0.05	± 0.5		*	± 0.7	%
	G = 1000		± 0.5	± 1		*	± 2	%
Gain vs Temperature	G = 1		± 1	± 10		*	± 10	ppm/°C
50kΩ Resistance ⁽¹⁾			± 25	± 100		*	*	ppm/°C
Nonlinearity	G = 1		± 0.0003	± 0.001		*	± 0.002	% of FSR
	G = 10		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 100		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 1000		± 0.002	± 0.01		*	± 0.02	% of FSR
OUTPUT								
Voltage: Positive	$R_L = 10\text{k}\Omega$	$(V+) - 1$	$(V+) - 0.8$		*	*		V
Negative	$R_L = 10\text{k}\Omega$	$(V-) + 0.35$	$(V-) + 0.2$		*	*		V
Single Supply High	$V_S = +2.7\text{V}/0\text{V}^{(2)}$, $R_L = 10\text{k}\Omega$	1.8	2.0		*	*		V
Single Supply Low	$V_S = +2.7\text{V}/0\text{V}^{(2)}$, $R_L = 10\text{k}\Omega$	60	35		*	*		mV
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+5/-12			*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	G = 1		800			*		kHz
	G = 10		500			*		kHz
	G = 100		70			*		kHz
	G = 1000		7			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$, G = 10		0.9			*		V/μs
Settling Time, 0.01%	G = 1		15			*		μs
	G = 10		15			*		μs
	G = 100		21			*		μs
	G = 1000		210			*		μs
Overload Recovery	50% Overdrive		20			*		μs
POWER SUPPLY								
Voltage Range		± 1.35	± 15	± 18	*	*	*	V
Current	$V_{\text{IN}} = 0\text{V}$		± 350	± 385		*	*	μA
TEMPERATURE RANGE								
Specification		-40		85	*	*	*	°C
Operating		-40		125	*	*	*	°C
θ_{JA}			80			*		°C/W

* Specification same as INA118PB, UB.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation. (2) $V_{\text{CM}} = 2\text{V}$. Common-mode input voltage range is limited. See text for discussion of low power supply and single power supply operation.

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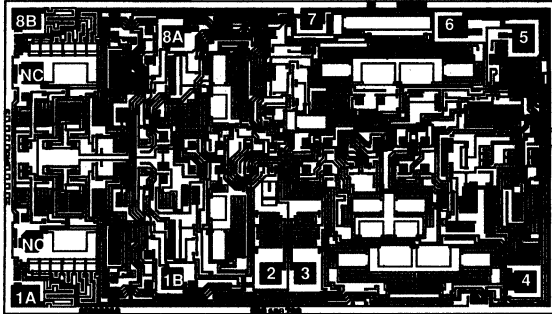
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DICE INFORMATION



INA118 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B ⁽¹⁾	R _G	6	V _O
2	V _{-IN}	7	V ₊
3	V _{+IN}	8A, 8B ⁽¹⁾	R _o
4	V ₋		
5	Ref		

NC = No Connection.

NOTES: (1) Connect both indicated pads.

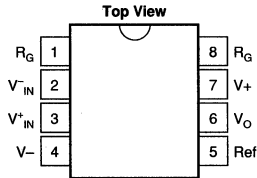
Substrate Bias: Internally connected to V₋ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	120 x 70 ±5	3.05 x 1.78 ±0.13
Die Thickness	14 ±3	0.36 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION

8-Pin DIP and SO-8



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

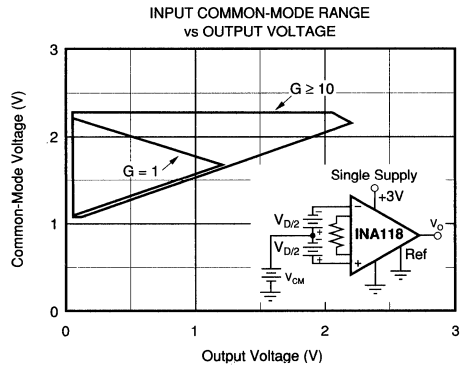
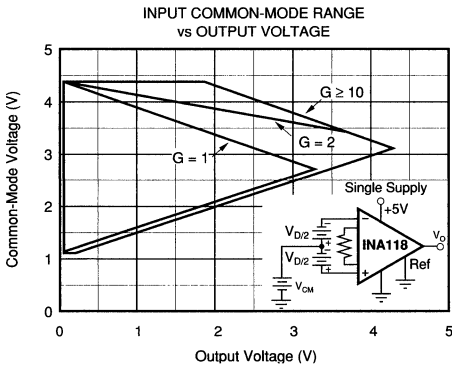
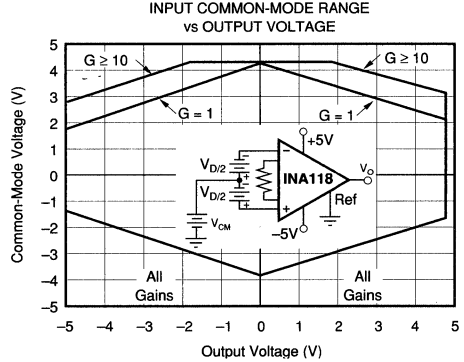
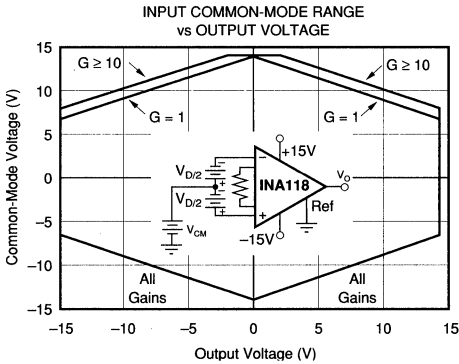
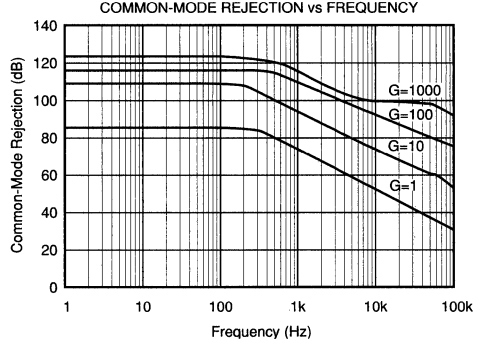
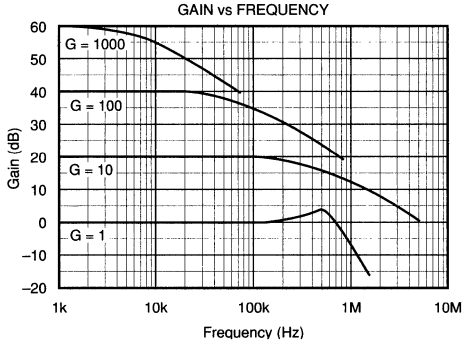
MODEL	PACKAGE	PACKAGE DRAWING NUMBER	TEMPERATURE RANGE
INA118P	8-Pin Plastic DIP	006	-40°C to +85°C
INA118PB	8-Pin Plastic DIP	006	-40°C to +85°C
INA118U	SO-8 Surface-Mount	182	-40°C to +85°C
INA118UB	SO-8 Surface-Mount	182	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

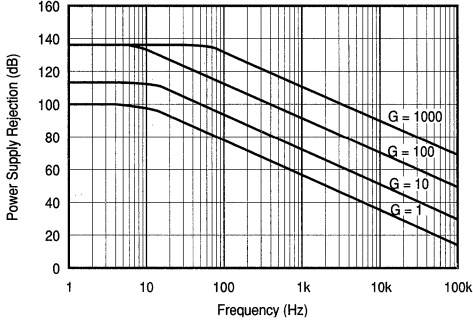


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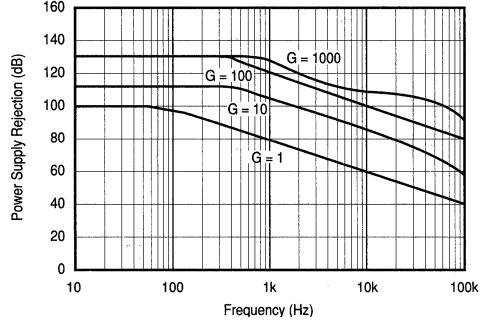
TYPICAL PERFORMANCE CURVES (CONT)

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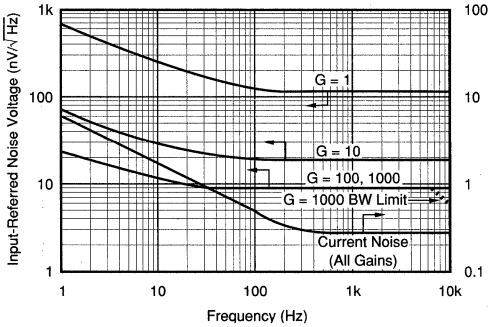
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



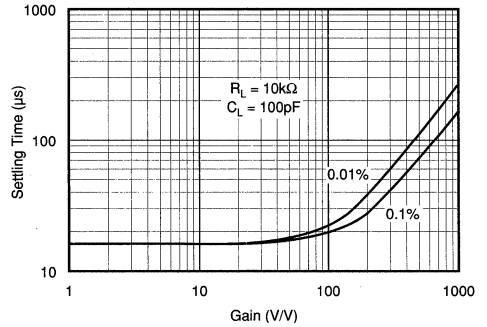
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



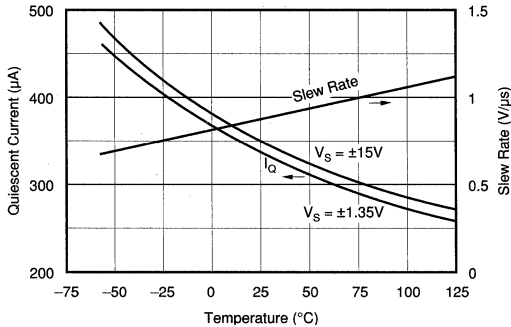
INPUT- REFERRED NOISE VOLTAGE
vs FREQUENCY



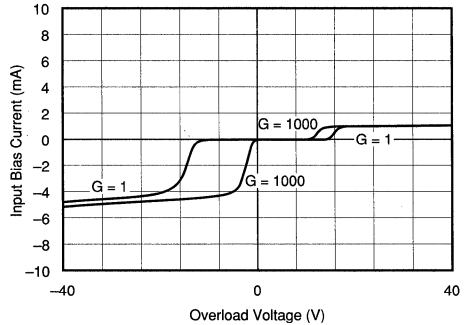
SETTLING TIME vs GAIN



QUIESCENT CURRENT and SLEW RATE
vs TEMPERATURE



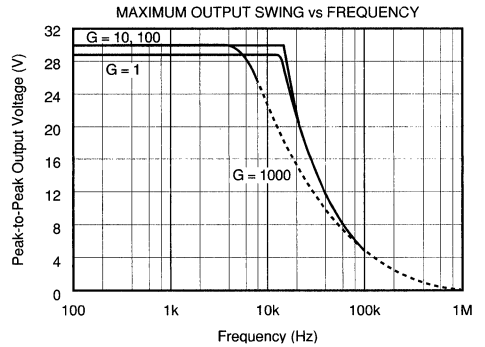
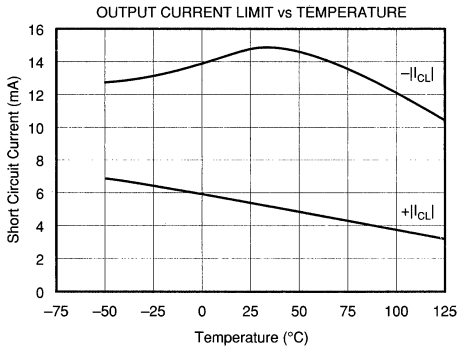
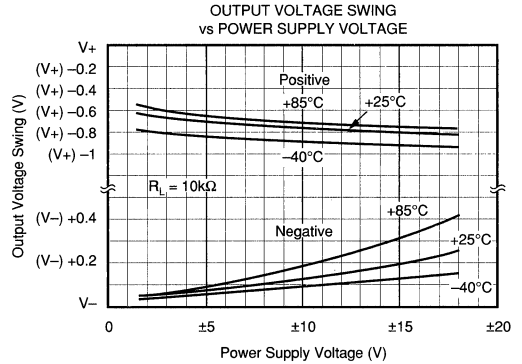
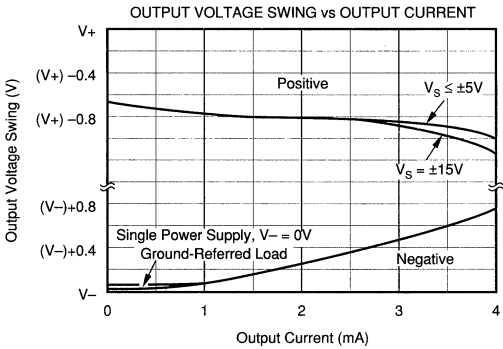
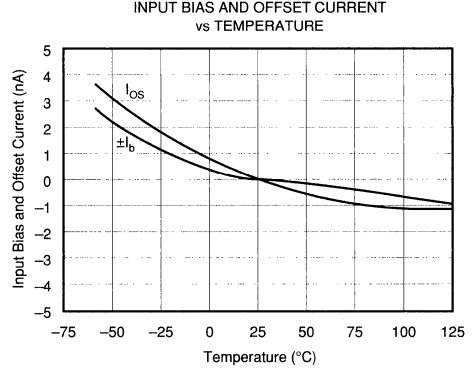
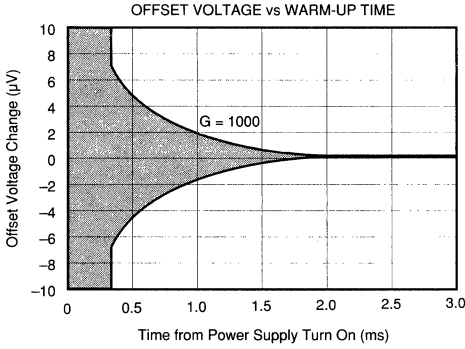
INPUT BIAS CURRENT
vs INPUT OVERLOAD VOLTAGE



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TYPICAL PERFORMANCE CURVES (CONT)

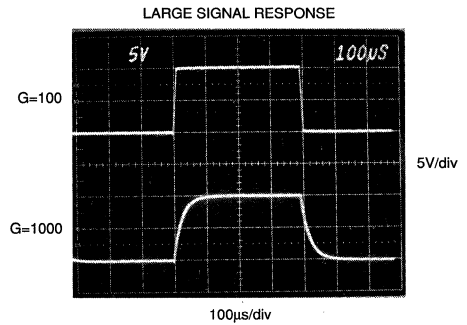
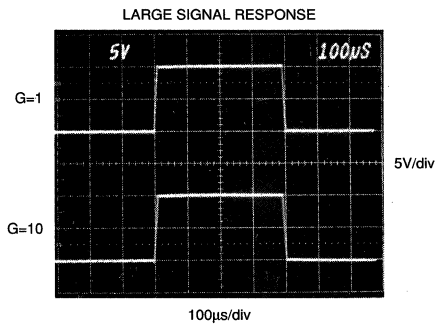
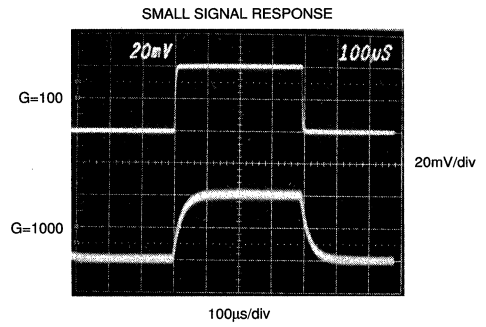
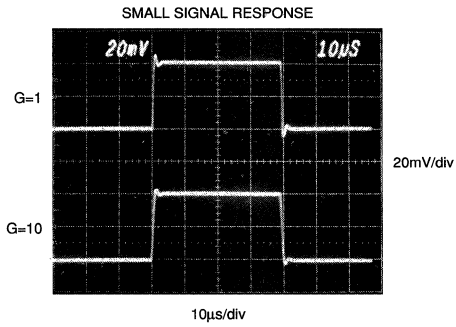
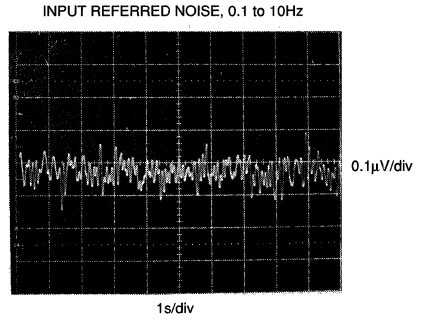
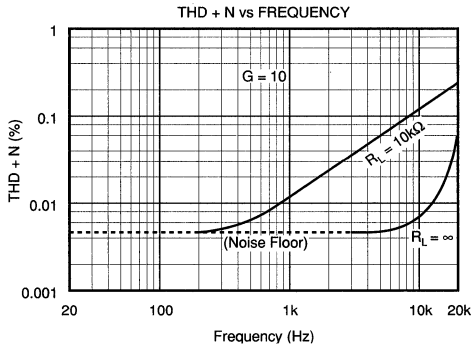
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_a = +25^\circ\text{C}$, $V_s = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA118. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 12Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G=1).

SETTING THE GAIN

Gain of the INA118 is set by connecting a single external resistor, R_G , connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2 . These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA118.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA118 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA118. Settling time also remains excellent at high gain.

The INA118 exhibits approximately 3dB peaking at 500kHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 300kHz or lower will produce a flat passband unity gain response.

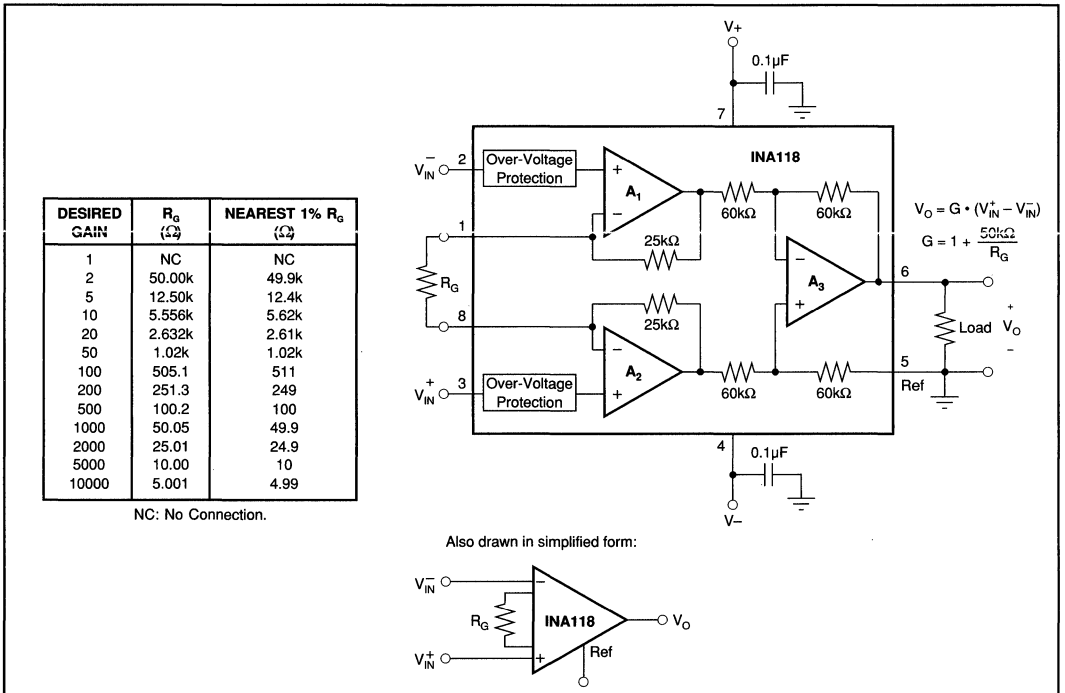


FIGURE 1. Basic Connections.

NOISE PERFORMANCE

The INA118 provides very low noise in most applications. For differential source impedances less than $1\text{k}\Omega$, the INA103 may provide lower noise. For source impedances greater than $50\text{k}\Omega$, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA118 is approximately $0.28\mu\text{Vp-p}$ measured from 0.1 to 10Hz ($G \geq 100$). This provides dramatically improved noise when compared to state-of-the-art copper-stabilized amplifiers.

OFFSET TRIMMING

The INA118 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

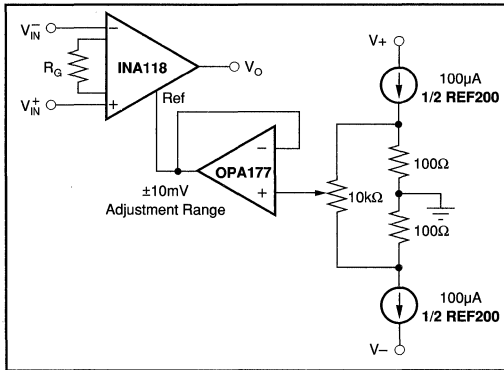


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA118 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 5\text{nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA118 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

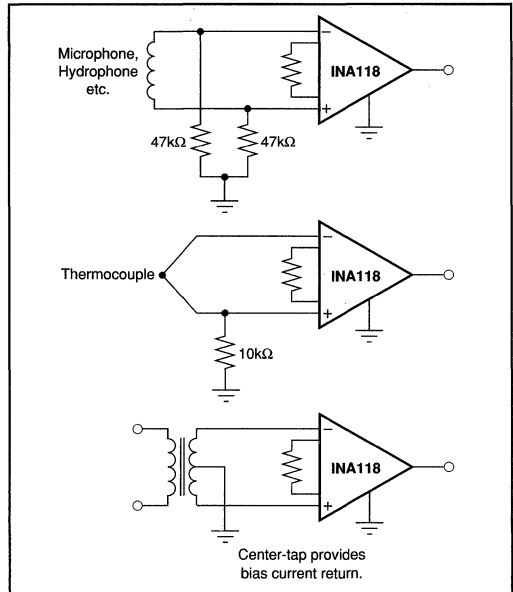


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA118 is from approximately 0.6V below the positive supply voltage to 1V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2 . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage”.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA118 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA118 can be operated on power supplies as low as $\pm 1.35\text{V}$. Performance of the INA118 remains excellent with power supplies ranging from $\pm 1.35\text{V}$ to $\pm 18\text{V}$. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for a various supply voltages and gains.

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SINGLE SUPPLY OPERATION

The INA118 can be used on single power supplies of +2.7V to +36V. Figure 5 shows a basic single supply circuit. The output Ref terminal is connected to ground. Zero differential input voltage will demand an output voltage of 0V (ground). Actual output voltage swing is limited to approximately 35mV above ground, when the load is referred to ground as shown. The typical performance curve "Output Voltage vs Output Current" shows how the output voltage swing varies with output current.

With single supply operation, V_{IN}^+ and V_{IN}^- must both be 1.1V above ground for linear operation. You cannot, for instance, connect the inverting input to ground and measure a voltage connected to the non-inverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 5. It shows the INA118, operating from a single 3V supply. A resistor in series with the low side of the bridge assures that the bridge output

voltage is within the common-mode range of the amplifier's inputs. Refer to the typical performance curve "Input Common-Mode Range vs Output Voltage" for 3V single supply operation.

INPUT PROTECTION

The inputs of the INA118 are individually protected for voltages up to $\pm 40V$. For example, a condition of $-40V$ on one input and $+40V$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The typical performance curve "Input Bias Current vs Input Overload Voltage" shows this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

INSIDE THE INA118

Figure 1 shows a simplified representation of the INA118. The more detailed diagram shown here provides additional insight into its operation.

Each input is protected by two FET transistors that provide a low series resistance under normal signal conditions, preserving excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 1.5 to 5mA.

The differential input voltage is buffered by Q_1 and Q_2 and impressed across R_G , causing a signal current to flow through R_G , R_1 and R_2 . The output difference amp, A_3 , removes the common-mode component of the input signal and refers the output signal to the Ref terminal.

Equations in the figure describe the output voltages of A_1 and A_2 . The V_{BE} and IR drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 1V lower than the input voltages.

$$A_1 \text{ Out} = V_{CM} - V_{BE} - (15\mu A \cdot 25k\Omega) - V_G/2$$

$$A_2 \text{ Out} = V_{CM} - V_{BE} - (15\mu A \cdot 25k\Omega) + V_G/2$$

Output Swing Range A_1, A_2 : $(V^+) - 0.65V$ to $(V^-) + 0.06V$
 Amplifier Linear Input Range: $(V^+) - 0.65V$ to $(V^-) + 1.1V$

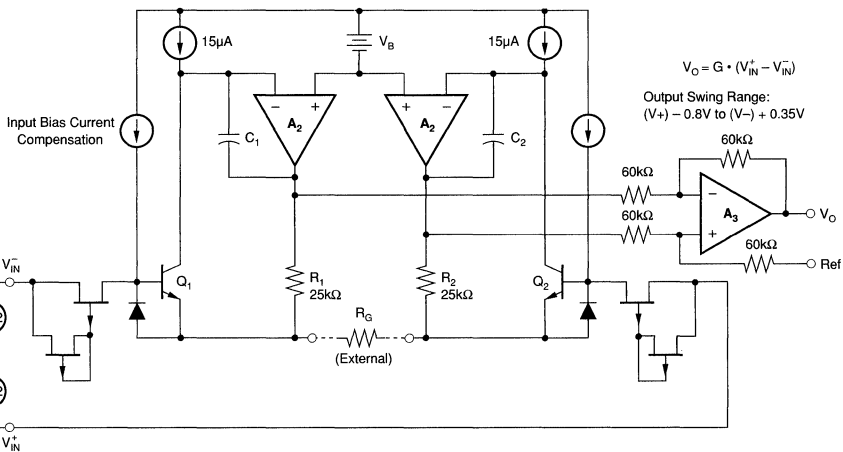


FIGURE 4. INA118 Simplified Circuit Diagram.

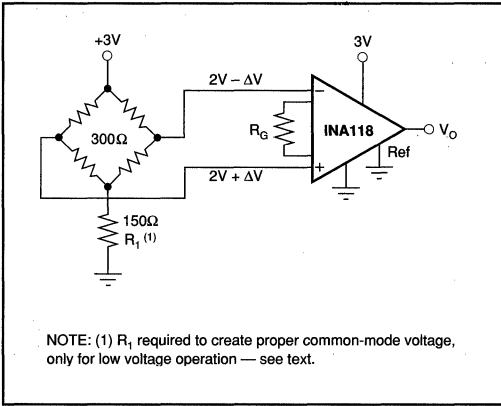


FIGURE 5. Single-Supply Bridge Amplifier.

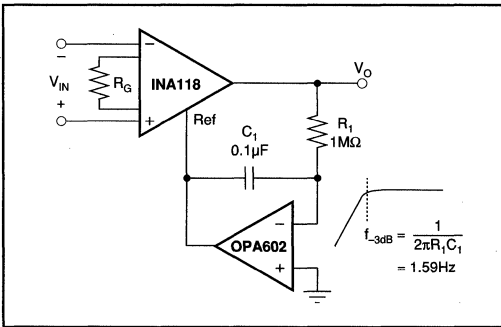


FIGURE 6. AC-Coupled Instrumentation Amplifier.

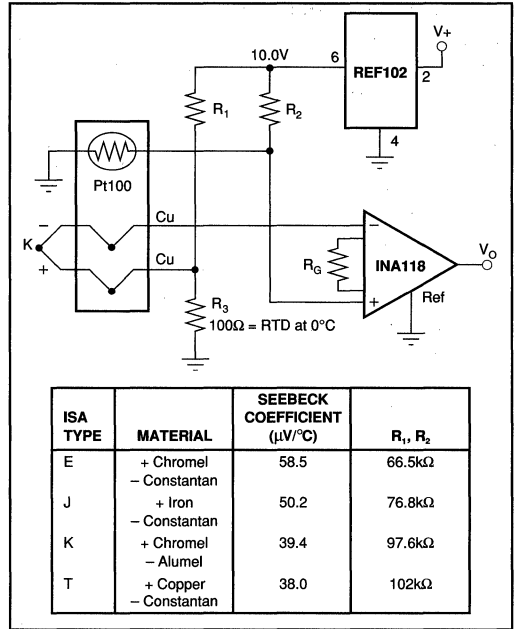


FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

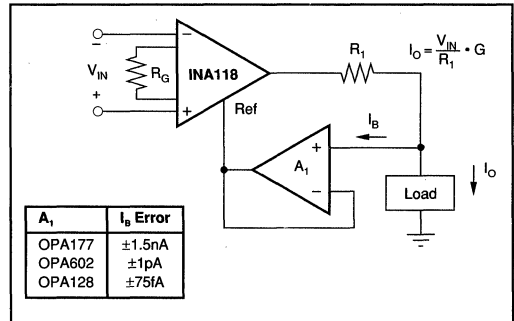


FIGURE 8. Differential Voltage to Current Converter.

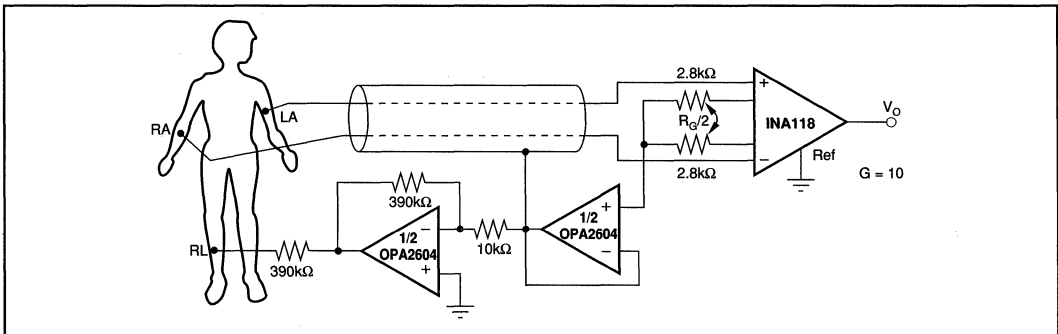
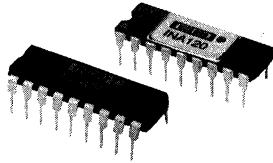


FIGURE 9. ECG Amplifier With Right-Leg Drive.

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INA120



Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 25 μ V max
- **LOW OFFSET VOLTAGE DRIFT:** 0.25 μ V/ $^{\circ}$ C max
- **PIN-STRAPPED GAINS:** 1, 10, 100, 1000
- **LOW GAIN DRIFT:** 30ppm/ $^{\circ}$ C max at G = 100
- **HIGH COMMON-MODE REJECTION:** 106dB at 60Hz, G = 100

APPLICATIONS

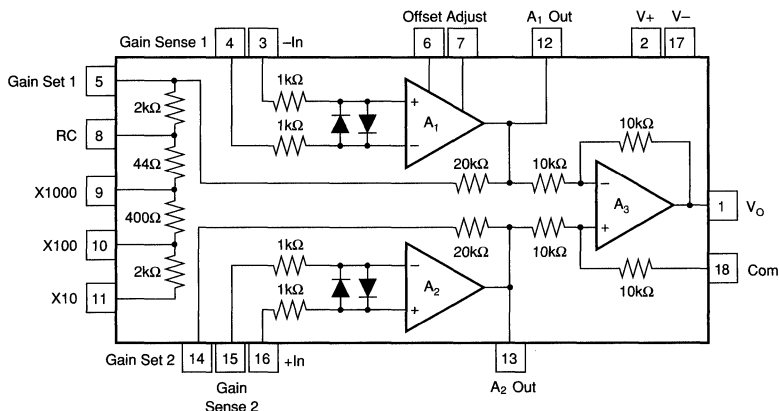
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEM
- SWITCHED-GAIN AMPLIFIER

DESCRIPTION

The INA120 is a precision instrumentation amplifier ideal for accurate signal acquisition. It combines precision, protected-input operational amplifiers, laser-trimmed gain-setting resistors, and a high common-mode rejection difference amplifier on a single chip.

Simple pin-strapped connections set precise gains of 1, 10, 100 or 1000. External resistors can be used to set any gain from one to 5000. Gains can be digitally selected with an external multiplexer. Gain-sense connections on the INA120 maintain accuracy when using multiplexer or gain-switching circuitry. Low power dissipation and careful on-chip thermal management reduce warm-up drift and assure excellent long-term stability.

The INA120 is available in both plastic and ceramic 18-pin DIP packages, specified for the industrial temperature range.



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SPECIFICATIONS

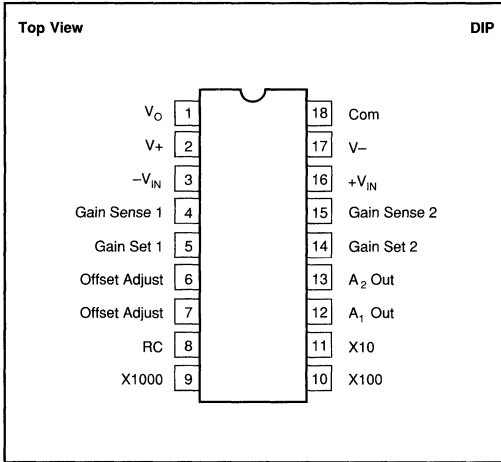
At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	CONDITIONS	INA120CG			INA120BG, BP			INA120AP			UNITS									
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX										
GAIN Range of Gain Gain Equation Gain Error Gain Temp Coefficient Nonlinearity	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$	1 $1 + (2R_f/R_g)$ 0.01 0.05 0.1 0.3 4 4 6 22 0.001 0.002 0.004 0.008	1000 0.05 0.1 0.2 0.5 10 10 30 50 0.005 0.005 0.01 0.05	1 $1 + (2R_f/R_g)$ 0.01 0.05 0.1 0.3 4 4 6 22 0.001 0.002 0.004 0.008	1000 0.05 0.1 0.2 0.5 20 20 40 50 0.01 0.01 0.02 0.1	1 $1 + (2R_f/R_g)$ 0.01 0.05 0.1 0.3 4 4 6 22 0.001 0.002 0.004 0.008	1000 0.05 0.1 0.2 0.5 20 20 40 50 0.01 0.01 0.02 0.1	1 $1 + (2R_f/R_g)$ 0.02 0.1 0.2 0.5 6 8 10 40 0.001 0.002 0.004 0.008	1000 0.1 0.2 0.5 1 20 40 60 100 0.01 0.01 0.02 0.1	V/V V/V % % % ppm/°C ppm/°C ppm/°C ppm/°C % of FS % of FS % of FS % of FS										
											OFFSET VOLTAGE Initial Offset vs Temperature vs Power Supply	$V_S = \pm 6\text{V to } \pm 18\text{V}$	$(10+300/\text{G})$	$(25+600/\text{G})$ $(25 + 10/\text{G})$	$(50+300/\text{G})$	$(100+600/\text{G})$ $(1 + 20/\text{G})$	$(50+300/\text{G})$	$(200+600/\text{G})$ $(2 + 20/\text{G})$	$(200+600/\text{G})$ $(1 + 20/\text{G})(40 + 300/\text{G})$	μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$
											INPUT BIAS CURRENT Initial Bias Current vs Temperature Initial Offset Current vs Temperature Impedance: Differential Common-Mode		± 7 ± 0.2 ± 5 ± 0.2 $10^{10} \parallel 3$ $10^{10} \parallel 3$	± 20 ± 10 	± 7 ± 0.2 ± 5 ± 0.2 $10^{10} \parallel 3$ $10^{10} \parallel 3$	± 20 ± 20 	± 20 ± 10 ± 0.2 $10^{10} \parallel 3$ $10^{10} \parallel 3$	± 50 ± 50 	nA nA/°C nA nA/°C $\mu\text{A} \parallel \text{pF}$ $\Omega \parallel \text{pF}$	
											INPUT VOLTAGE RANGE Range, Linear Response CMRR (DC, 1k Ω Source Imbalance)	$G = 1$ $G = 10$ $G = 100$ $G = 1000$	± 10 80 96 106 106	± 12.5 90 106 110 110	± 10 74 90 106 106	± 12.5 90 106 110 110		± 10 70 86 100 100	± 12.5 85 95 105 105	V dB dB dB dB
											NOISE Input Voltage Noise $f_b = 0.1\text{Hz to } 10\text{Hz}$ Density; $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1000\text{Hz}$ Input Current Noise $f_b = 0.1\text{Hz to } 10\text{Hz}$ Density; $f = 10\text{Hz}$ $f = 1\text{kHz}$ Output Voltage Noise $f_b = 0.1\text{Hz to } 10\text{Hz}$	$G = 1000$ $G = 1000$	0.7 14 11 10		0.7 14 11 10		0.7 14 11 10		$\mu\text{V p-p}$ nV/√Hz nV/√Hz nV/√Hz pA p-p pA/√Hz pA/√Hz $\mu\text{V p-p}$	
											DYNAMIC RESPONSE Small Signal Bandwidth (–3dB) Slew Rate Settling Time to 0.01% Full Power Bandwidth, $G < 200$ Overload Recovery	$G = 1$ $G = 10$ $G = 100$ $G = 1000$ $G = 1$ $G = 10$ $G = 100$ $G = 1000$ $V_O = \pm 10\text{V}, R_L = 2\text{k}\Omega$ 50% Overdrive		2 200 20 2 0.4 0.6 24 30 50 200 9 2		2 200 20 2 0.4 0.6 24 30 50 200 9 2		2 200 20 2 0.4 0.6 24 30 50 200 9 2		MHz kHz kHz kHz V/μs μs μs μs μs kHz μs
											OUTPUT Voltage, $R_L = 2\text{k}\Omega$ Current Short-Circuit Current Capacitive Load, Stable Operation	Over Temperature Over Temperature	± 10.5 5	± 12.8 15 24 4000	± 10.5 5	± 12.8 15 24 4000		± 10.5 5	± 12.8 15 24 4000	V mA mA pF
											POWER SUPPLY Rated Voltage Voltage Range Supply Current	$V_O = 0\text{V}$	± 6 ± 2.7	± 15 ± 18 ± 4	± 6 ± 18 ± 2.7	± 15 ± 18 ± 4		± 6 ± 15 ± 2.7	± 15 ± 18 ± 4	V V mA
											TEMPERATURE RANGE Specification Operation BP, AP Operation CG, BG Storage		–25 –55 –65	+85 +125 +150	–25 –40 –55 –65	+85 +85 +125 +150		–25 –40 –65	+85 +85 +150	°C °C °C °C

See Absolute Maximum Table.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	(V+) +2 to (V-) -2V
Differential Input Voltage	Total V_S +4V
Operating Temperature	
Ceramic G Package	-65°C to +150°C
Plastic P Package	-40°C to +125°C
Storage Temperature	
Ceramic G Package	-65°C to +150°C
Plastic P Package	-40°C to +125°C
Junction Temperature	
Ceramic G Package	+175°C
Plastic P Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA120AP	18-Pin Plastic DIP	218
INA120BP	18-Pin Plastic DIP	218
INA120BG	18-Pin Ceramic DIP	158
INA120CG	18-Pin Ceramic DIP	158

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA120AP	18-Pin Plastic DIP	-25°C to +85°C
INA120BP	18-Pin Plastic DIP	-25°C to +85°C
INA120BG	18-Pin Ceramic DIP	-25°C to +85°C
INA120CG	18-Pin Ceramic DIP	-25°C to +85°C

INA120

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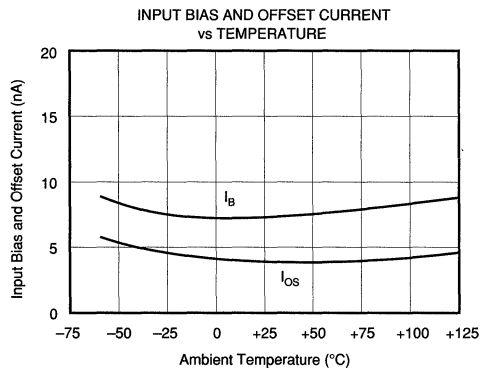
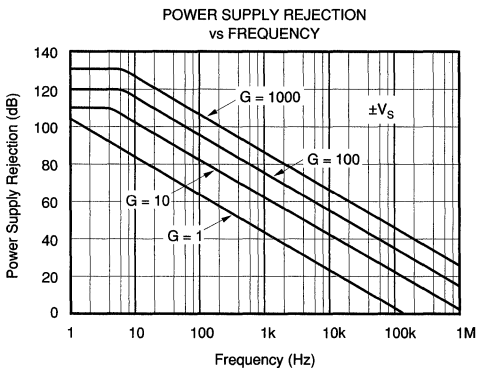
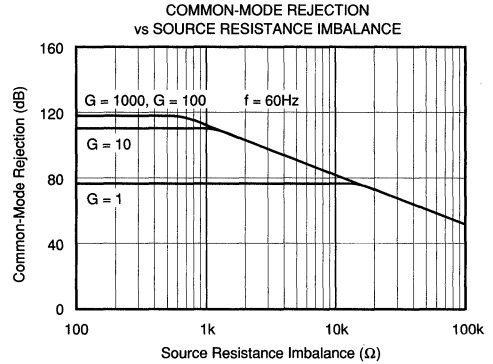
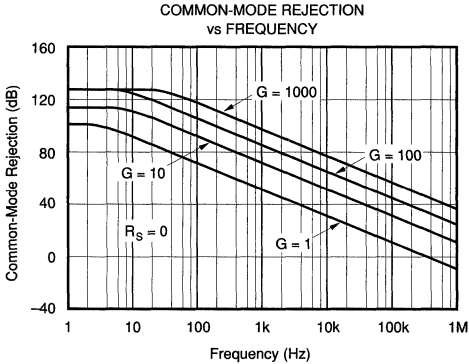
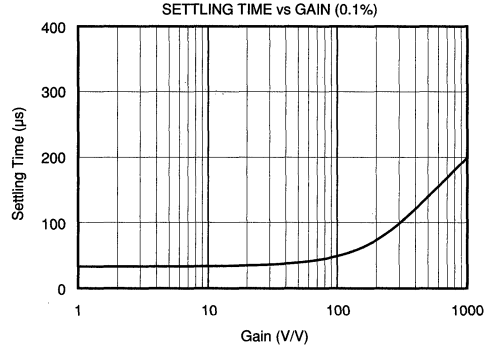
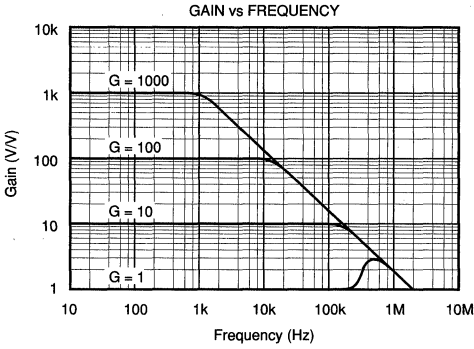
INSTRUMENTATION AMPLIFIERS

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TYPICAL PERFORMANCE CURVES

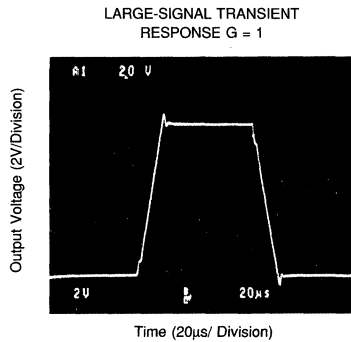
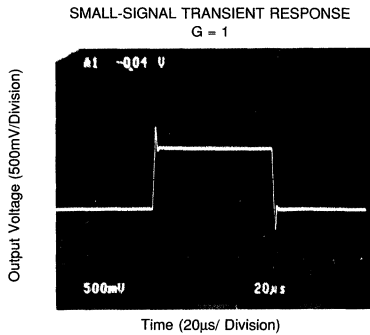
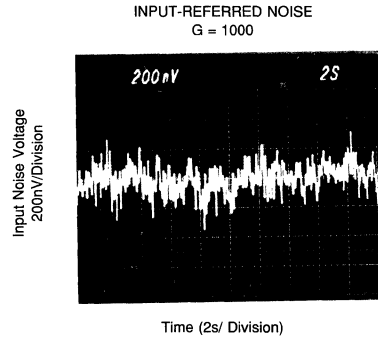
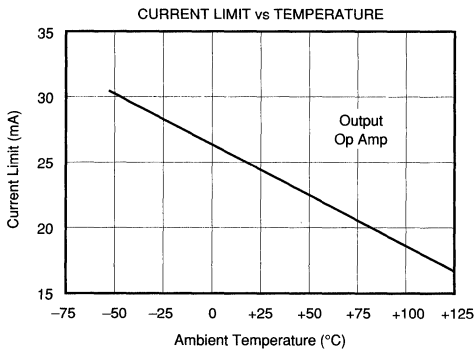
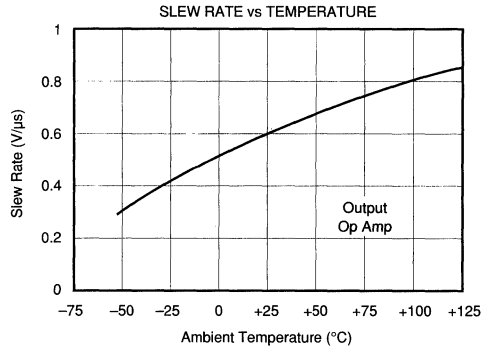
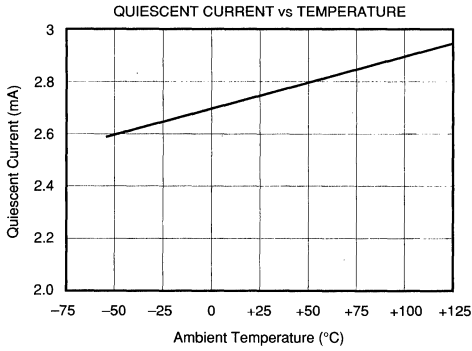
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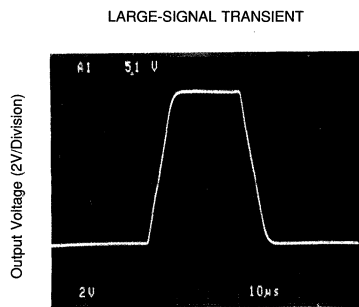
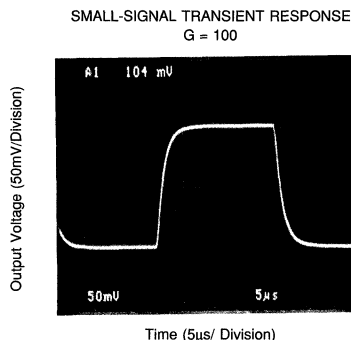
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA120. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins as shown. The differential input voltage is applied to pins 16 and 3.

The output is referred to the output common reference terminal, pin 18. This terminal must have a low-impedance connection to ground. A resistance of 1Ω or greater in series with the common terminal could degrade common-mode rejection beyond the specified value.

SETTING THE GAIN

Gains of 1, 10, 100 or 1000 can be configured by interconnecting the gain-set pins as shown in the table of Figure 1. These pin-strapped gains provide best gain accuracy and drift because they are determined by the ratios of accurately trimmed and matched on-chip resistors.

Digital gain control can be achieved using an analog multiplexer as shown in Figure 2. Since the switches are in series with the high impedance gain-sense connections, pins 4 and 15, their series resistance does not significantly affect gain error or drift. Gain error at $G = 1$ is slightly higher than with direct pin connections shown in Figure 1. The gain is selected with a two-bit address, A_0 and A_1 . The Multiplexer Enable control is directly connected to $V+$ since a logic "low" on this line would cause the input amplifiers to run open-loop.

Other gains may be set by connecting an external resistor, R_G , as shown in Figure 3a. Gain accuracy using an external gain-setting resistor is a function of R_G and the internal $20k\Omega$ resistors. The internal resistors are typically within $\pm 0.2\%$ of nominal value and their drift under $\pm 80\text{ppm}/^\circ\text{C}$. Inaccuracy and drift of R_G will contribute additional gain error and drift.

Figure 3b shows an external gain-setting resistor connected in parallel with internal resistors. By forming a portion of the

effective R_G with internal resistors, gain accuracy and drift can be somewhat improved.

Connections available on the INA120 allow all input stage gain-setting resistors to be provided externally. A custom precision resistor network could be connected to provide the highest accuracy and lowest gain drift for non-standard gains. Impedance of this external network should be made close to that of the internal network for best performance.

OFFSET TRIMMING

Many applications require no external offset voltage trimming. Figure 4 shows optional circuits for trimming offset voltage. Since the INA120 has two amplification stages, the offset voltage is comprised of two components—the input stage offset and output stage offset.

The input stage offset is equal to the combined offset of op amps A_1 and A_2 . This input stage offset dominates at high gain. When used in gains of 100 to 1000, it is often sufficient to adjust the input stage offset with a potentiometer connected to pins 6 and 7 as shown. Connect both inputs to ground and adjust for 0V at the output, pin 1. Do not use pins 6 and 7 to trim offset voltage at $G = 1$ or to correct for offset in devices following the INA120 since this can cause excessive offset voltage drift.

At $G = 1$, offset is dominated by the output stage. Output stage offset can be trimmed by applying a correction voltage at the output reference terminal, pin 18. Low impedance must be maintained at this node to preserve the high CMR of the INA120. This is achieved by buffering the trim voltage with an op amp as shown.

At intermediate gains it may be necessary to provide both input stage and output stage offset adjustments. Again, ground both inputs. Connect a jumper between pins 9 and 11 (temporarily connects the INA120 in high gain) and adjust R_1 for 0V at the output, pin 1. Then disconnect the jumper and adjust the output offset control for 0V output.

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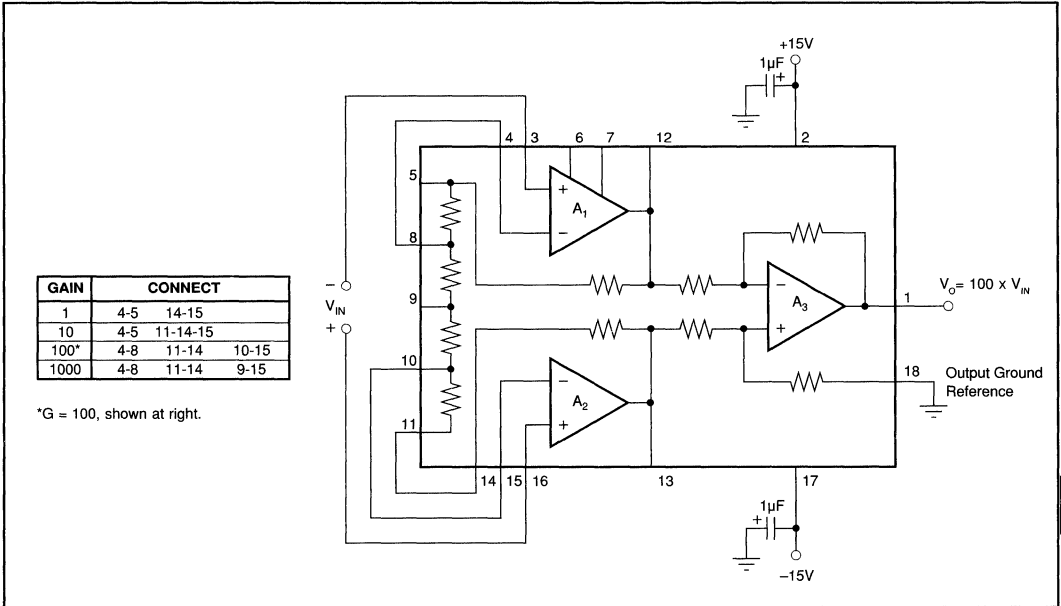


FIGURE 1. Basic Connection.

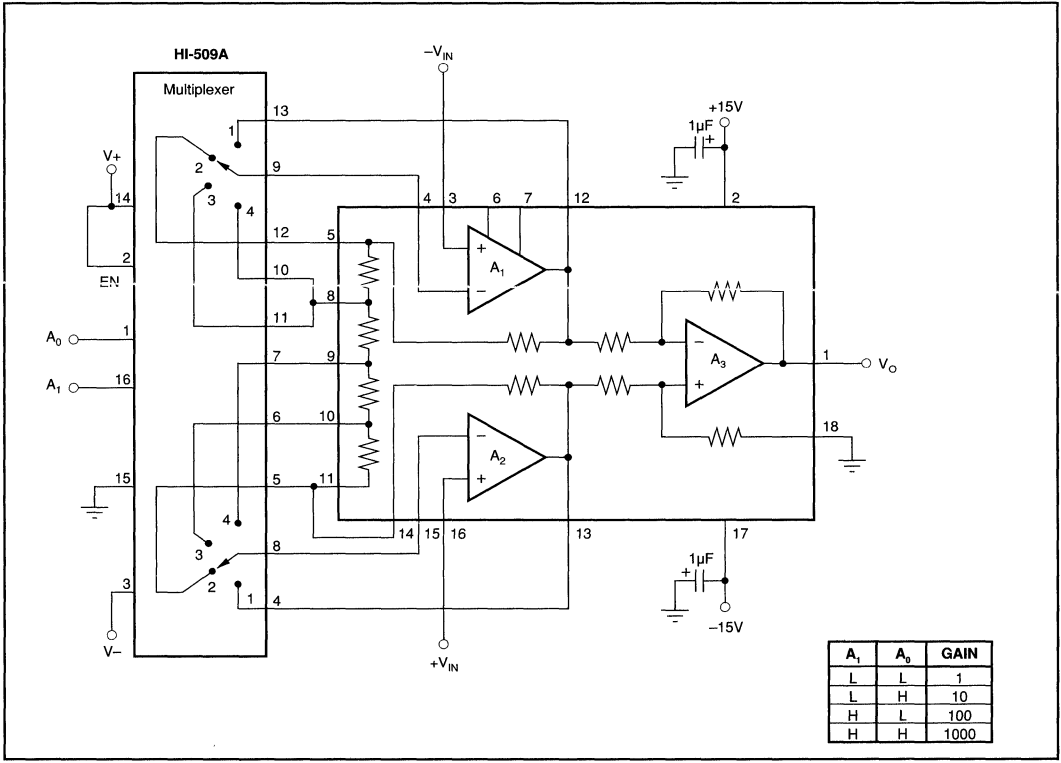


FIGURE 2. Digital Gain Control.

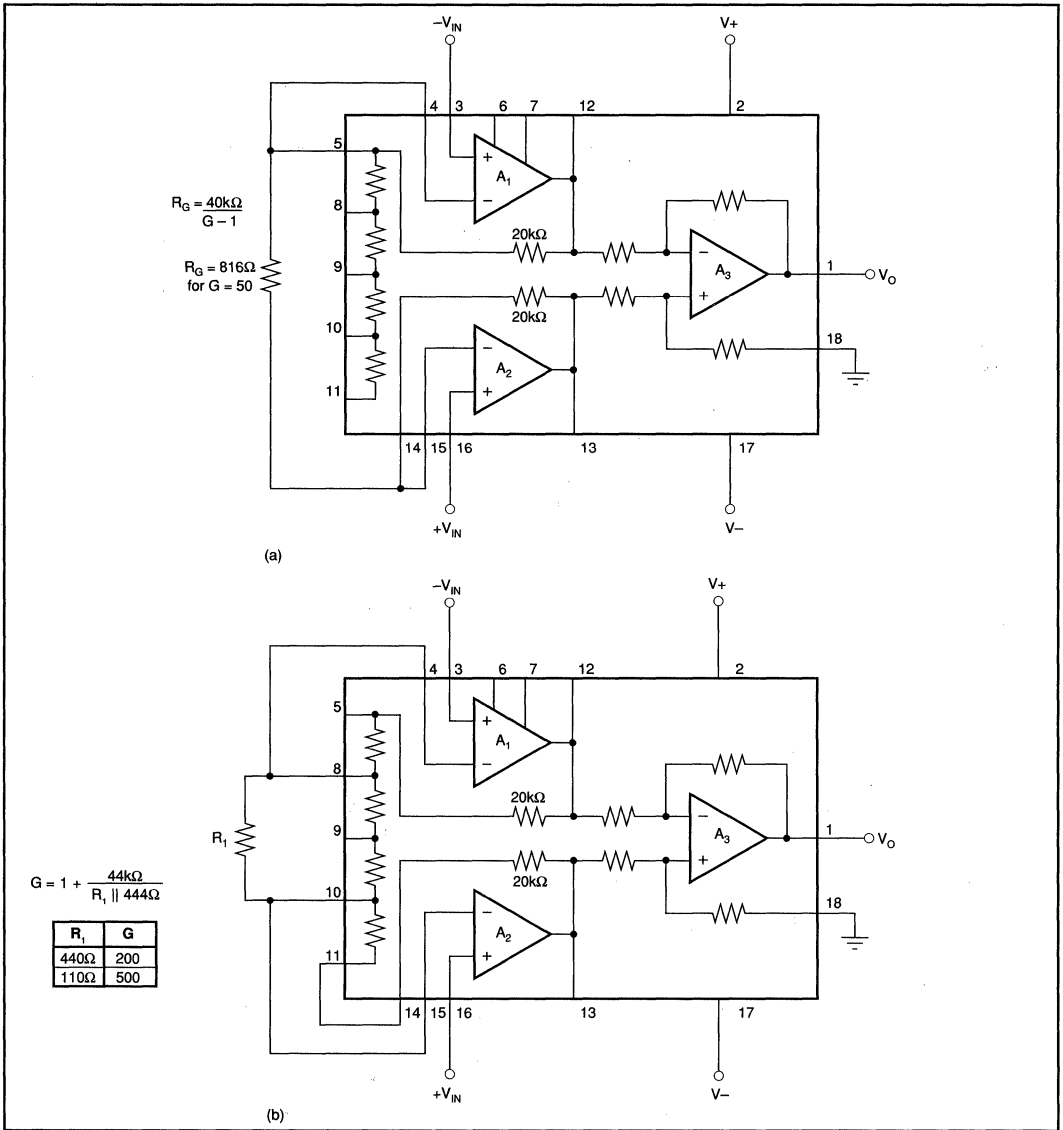


FIGURE 3. External Gain-Setting Resistors.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA120 is extremely high—approximately $10^{10}\Omega$. This does not mean, however, that no current flows in the input terminals. The input bias current of the INA120 is typically $\pm 10nA$ (it can be either polarity). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA120 is to function. Figure 5 shows various provisions for an input bias current path. Without an appropriate current path, the inputs will float to a potential which

exceeds the common-mode range of the INA120 and the input amplifiers will saturate.

INPUT PROTECTION

The inputs of the INA120 are protected for input voltages up to 2V beyond the power supply voltages. If the input can exceed these conditions, input clamp diodes should be provided as shown in Figure 6. R_S may not be required if the input cannot supply more than 100mA. If the input can supply larger currents, choose R_S according to the maximum source voltage, limiting current to under 100mA.

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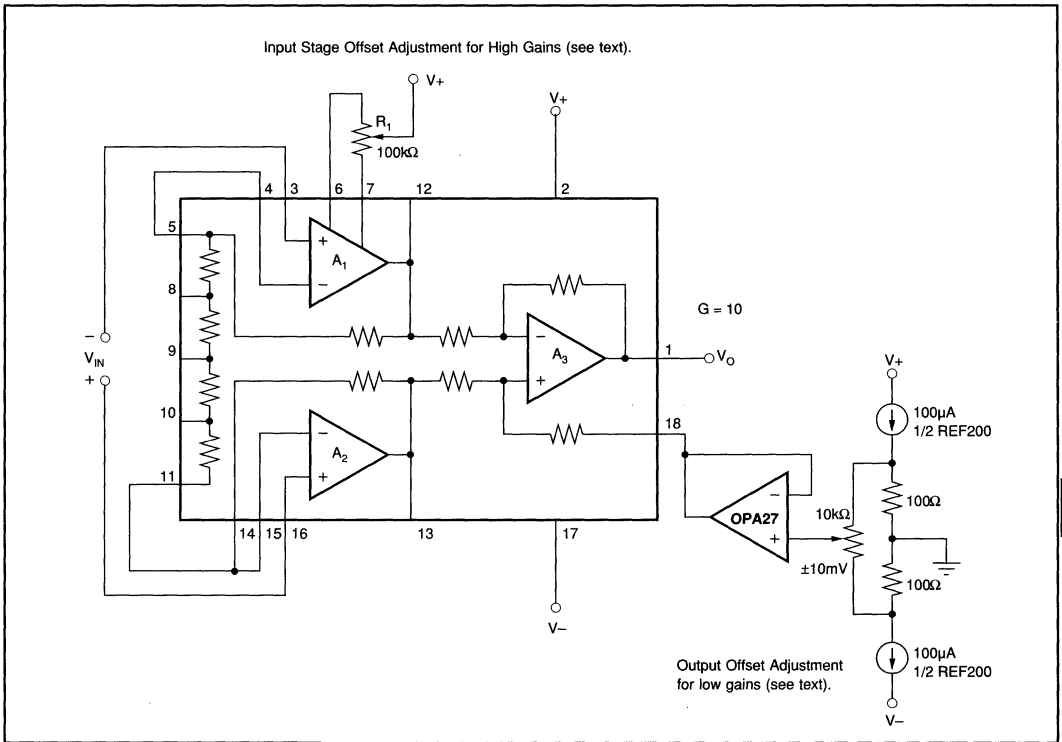


FIGURE 4. Offset Adjustment Circuits.

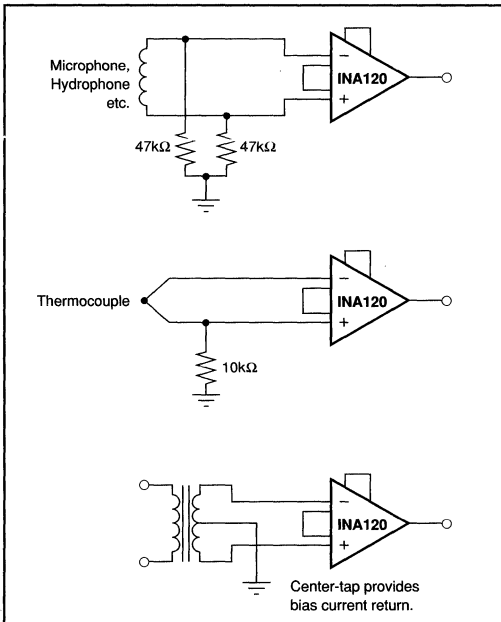


FIGURE 5. Providing an Input Bias Current Path.

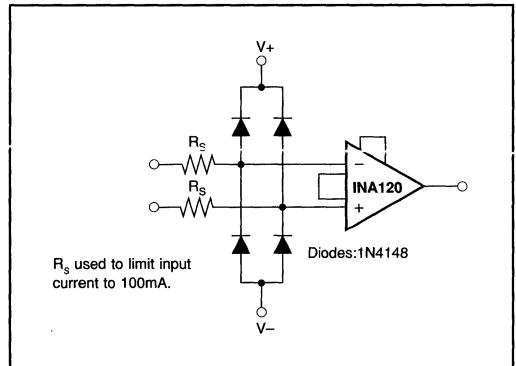


FIGURE 6. Input Protection Circuit.

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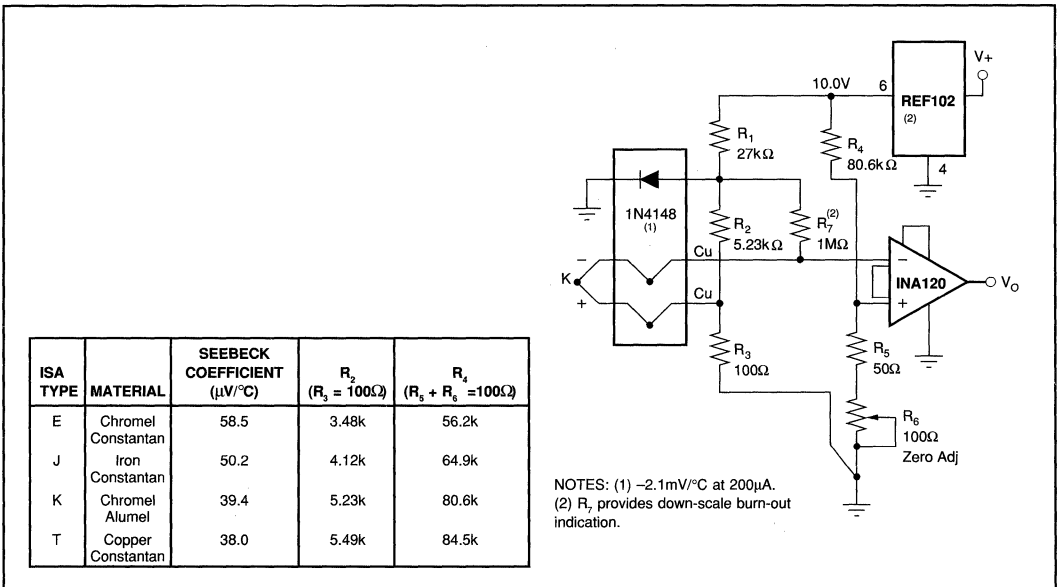


FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

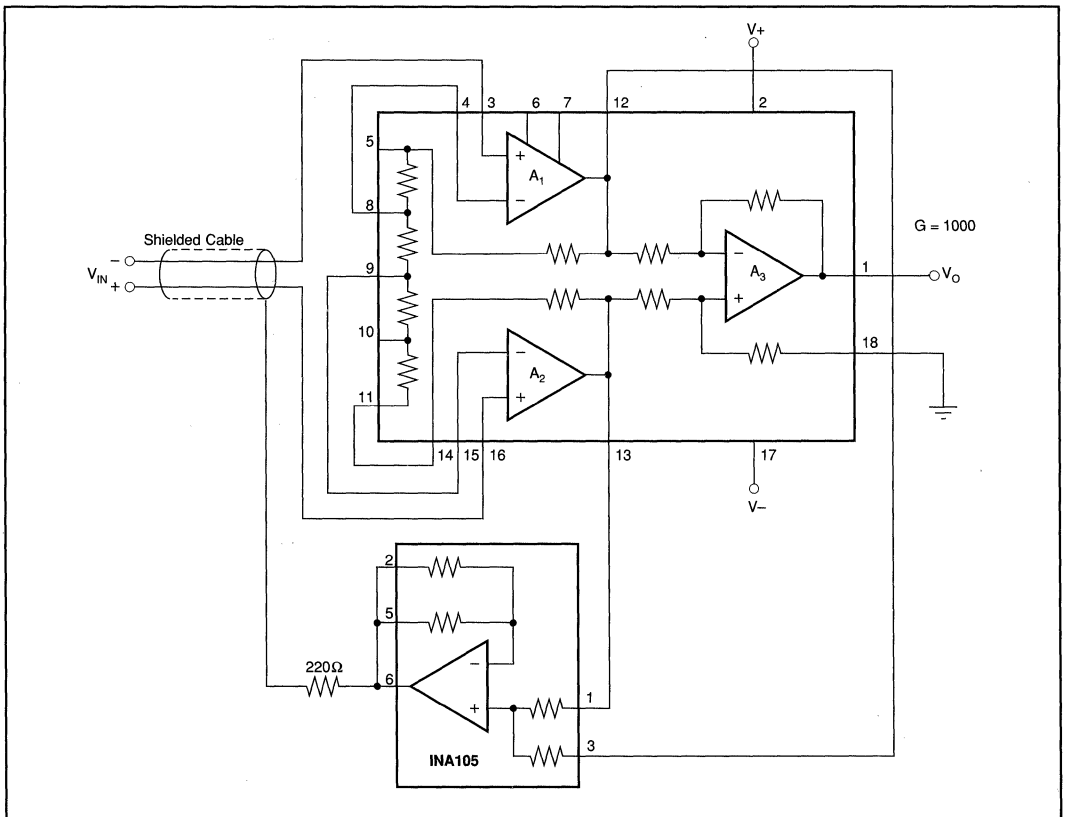
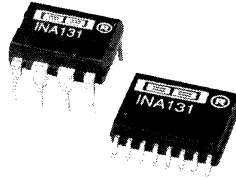


FIGURE 8. Guard Drive Circuit.

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INA131

Precision $G = 100$ INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** $50\mu\text{V}$ max
- **LOW DRIFT:** $0.25\mu\text{V}/^\circ\text{C}$ max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 110dB min
- **INPUT OVERVOLTAGE PROTECTION:** $\pm 40\text{V}$
- **WIDE SUPPLY RANGE:** ± 2.25 to $\pm 18\text{V}$
- **LOW QUIESCENT CURRENT:** 3mA
- **8-PIN PLASTIC DIP, SOL-16 SOIC**

DESCRIPTION

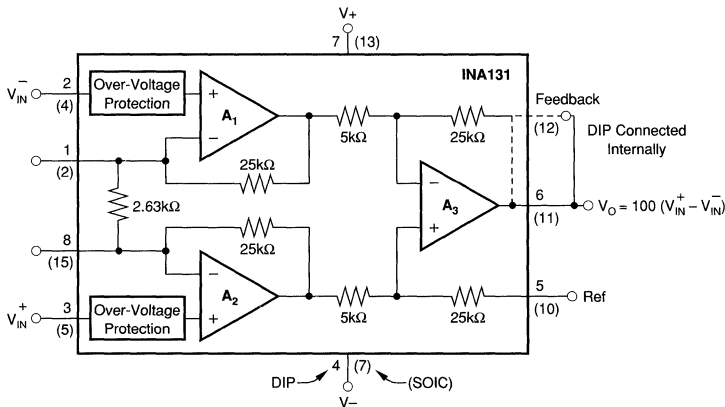
The INA131 is a low cost, general purpose $G = 100$ instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage ($50\mu\text{V}$), drift ($0.25\mu\text{V}/^\circ\text{C}$) and high CMR (110dB). Internal input protection can withstand up to $\pm 40\text{V}$ inputs without damage.

The INA131 is available in 8-pin plastic DIP and SOL-16 surface-mount packages. They are specified over the -40°C to $+85^\circ\text{C}$ temperature range.

APPLICATIONS

- **BRIDGE AMPLIFIER**
- **THERMOCOUPLE AMPLIFIER**
- **RTD SENSOR AMPLIFIER**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION**



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PDS-1144C

4.135

INA131

4

INSTRUMENTATION AMPLIFIERS

For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	INA131BP, BU			INA131AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		± 10	± 50		± 25	± 125	μV
Initial			± 0.1	± 0.25		± 0.25	± 1	$\mu\text{V}/^\circ\text{C}$
vs Temperature			0.5	3		*	*	$\mu\text{V}/\text{V}$
vs Power Supply			0.2			*	*	$\mu\text{V}/\text{mo}$
Long-Term Stability			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Impedance, Differential			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Common-Mode		± 11	± 13.5		*	*	V	
Input Common-Mode Range				± 40				V
Safe Input Voltage	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$	110	120		106	110		dB
Common-Mode Rejection								
BIAS CURRENT			± 0.5	± 2		*	± 5	nA
vs Temperature			± 8			*		$\text{pA}/^\circ\text{C}$
OFFSET CURRENT			± 0.5	± 2		*	± 5	nA
vs Temperature			± 8			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	$R_S = 0\Omega$					*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{Hz}$			16			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			12			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			12			*		$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			12			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.4			*		$\mu\text{Vp-p}$
Noise Current						*		$\text{pA}/\sqrt{\text{Hz}}$
$f = 10\text{Hz}$			0.4			*		$\text{pA}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			0.2			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 100Hz			18			*		pAp-p
GAIN								
Gain Error ⁽¹⁾			± 0.01	± 0.024		*	± 0.1	%
Resistor Value ⁽²⁾			± 10	± 40		*	*	%
Gain vs Temperature			± 5	± 10		*	± 20	$\text{ppm}/^\circ\text{C}$
Nonlinearity			± 0.0003	± 0.002		*	± 0.004	% of FSR
OUTPUT								
Voltage	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX} $V_S = \pm 11.4\text{V}$, $R_L = 2\text{k}\Omega$ $V_S = \pm 2.25\text{V}$, $R_L = 2\text{k}\Omega$ Stable Operation	± 13.5	± 13.7		*	*		V
		± 10	10.5		*	*		V
		± 1	1.5		*	*		V
			1000		*	*		pF
Load Capacitance, max								mA
Short Circuit Current				$+20/-15$				
FREQUENCY RESPONSE								
Bandwidth, -3dB	$V_O = \pm 10\text{V}$		70			*		kHz
Slew Rate			0.3	0.7		*	*	$\text{V}/\mu\text{s}$
Settling Time, 0.01%				100		*	*	μs
Overload Recovery		50% Overdrive		20		*	*	μs
POWER SUPPLY								
Voltage Range	$V_{\text{IN}} = 0\text{V}$	± 2.25	± 15	± 18	*	*	*	V
Current			± 2.2	± 3		*	*	mA
TEMPERATURE RANGE								
Specification		-40		85	*		*	$^\circ\text{C}$
Operating		-40		125	*		*	$^\circ\text{C}$
θ_{JA}			100			*		$^\circ\text{C}/\text{W}$

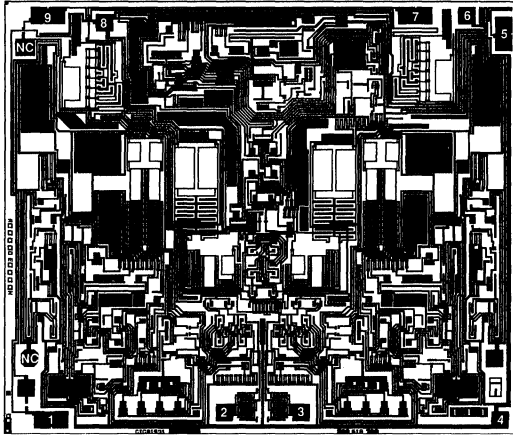
* Specification same as INA131BP/BU.

NOTES: (1) $R_L = 10\text{k}\Omega$. (2) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)

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DICE INFORMATION



INA131 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	R _G	6	V _O
2	V _{IN} ⁻	7	Feedback
3	V _{IN} ⁺	8	V ₊
4	V ₋	9	R _G
5	Ref		

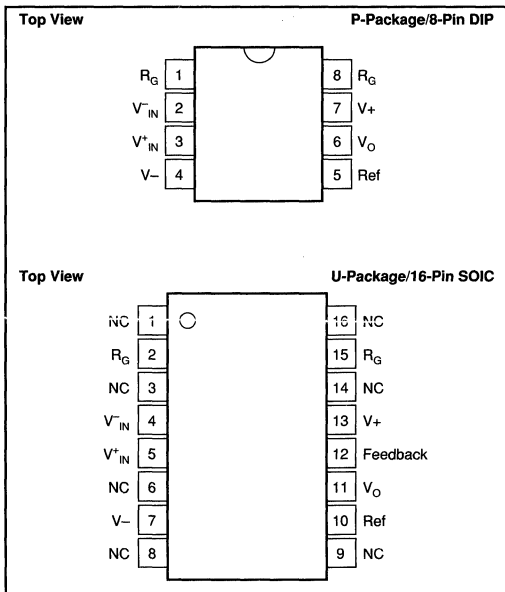
NC = No Connection.

Substrate Bias: Internally connected to V₋ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering -10s)	+300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA131AP	8-Pin Plastic DIP	-40°C to +85°C
INA131BP	8-Pin Plastic DIP	-40°C to +85°C
INA131AU	SOL-16 Surface-Mount	-40°C to +85°C
INA131BU	SOL-16 Surface-Mount	-40°C to +85°C

PACKAGE INFORMATION⁽¹⁾

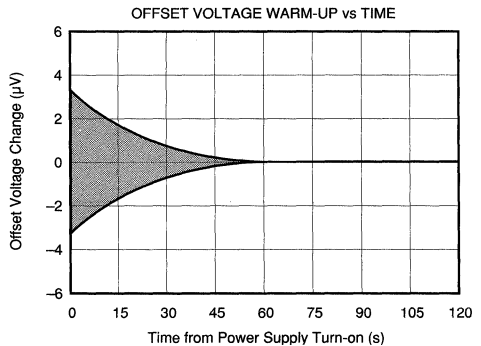
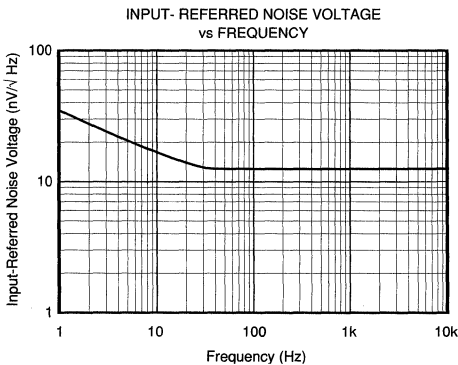
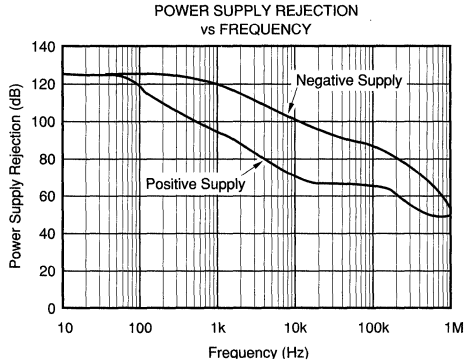
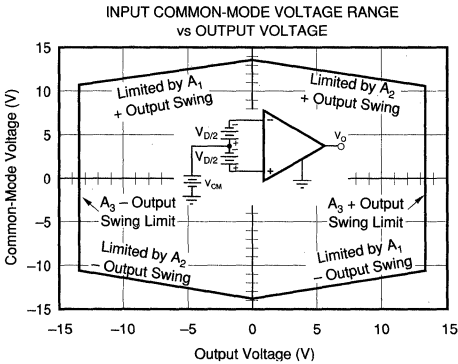
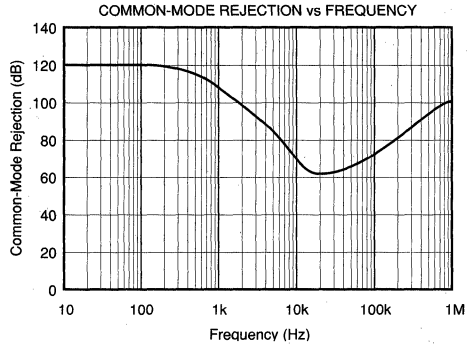
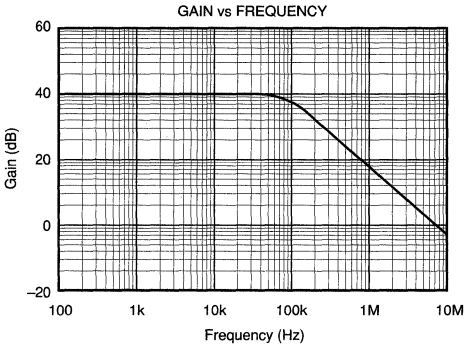
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA131AP	8-Pin Plastic DIP	006
INA131BP	8-Pin Plastic DIP	006
INA131AU	SOL-16 Surface Mount	211
INA131BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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TYPICAL PERFORMANCE CURVES

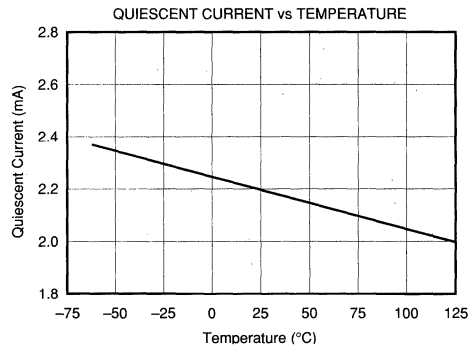
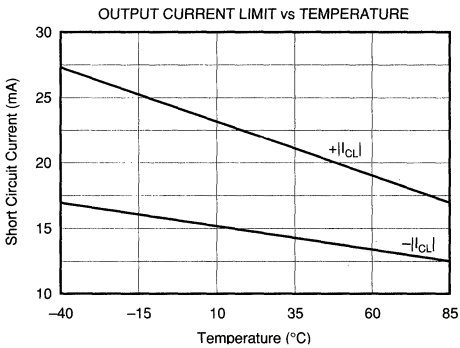
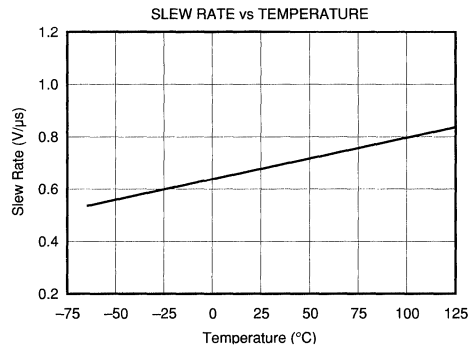
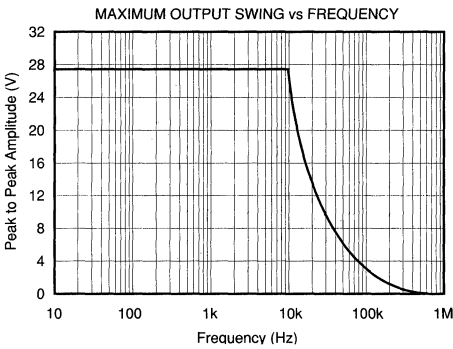
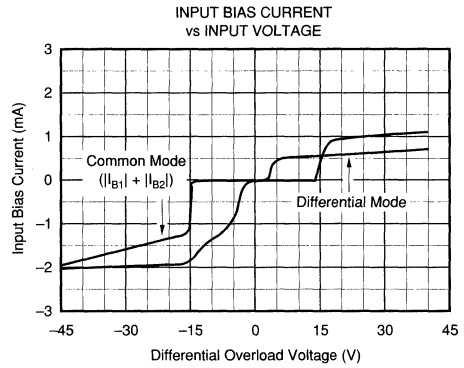
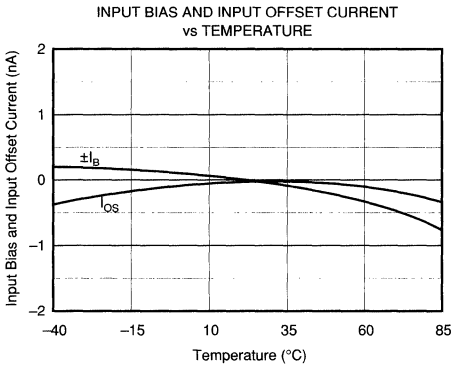
At 25°C, $V_s = \pm 15V$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

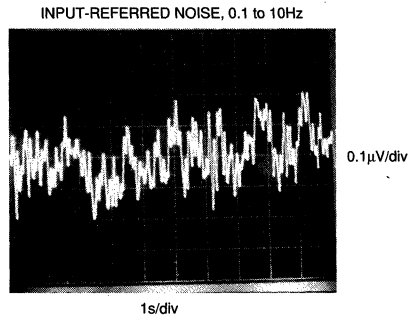
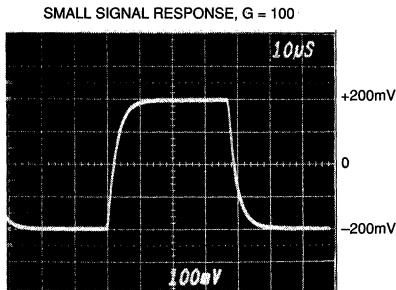
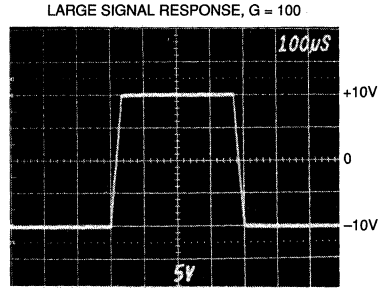
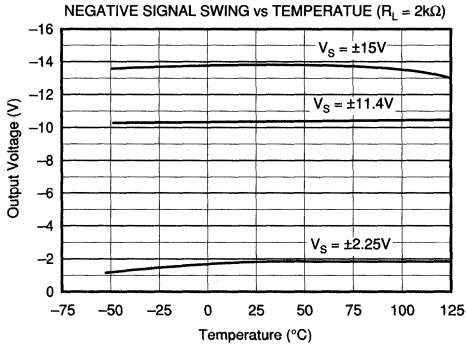
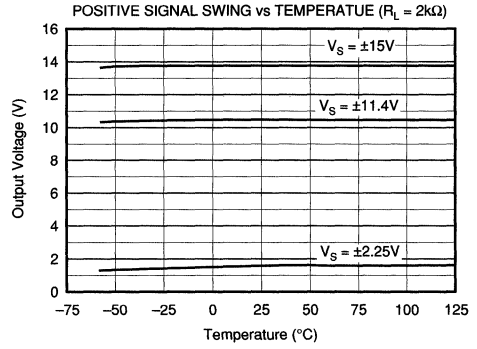
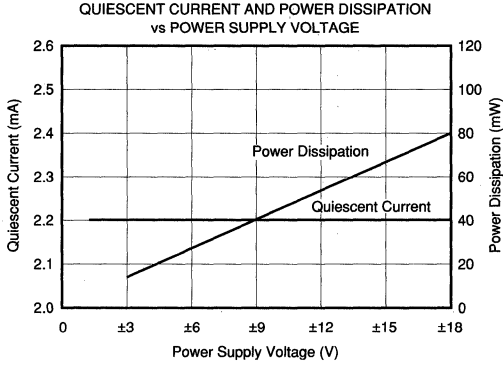
At 25°C, $V_S = \pm 15V$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, $V_S = \pm 15V$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA131. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a device with 110dB CMR to degrade to approximately 106dB CMR.

SETTING THE GAIN

No external resistors are required for $G = 100$. On-chip laser-trimmed resistors set the gain, providing excellent gain accuracy and temperature stability. Gain is distributed between the input and output stages of the INA131. Bandwidth is increased by approximately five times (compared to the INA114 in $G = 100$). Input common-mode range is also improved (see "Input Common-Mode Range").

Although the INA131 is primarily intended for fixed $G = 100$ applications, the gain can be increased by connecting an external resistor to the R_G pins. The internal resistors are trimmed for precise ratios, not to absolute values, so the influence of an external resistor will vary from device to

device. Absolute accuracy of the internal values is $\pm 40\%$. The nominal gain with an external R_G resistor can be calculated by:

$$G = 100 + \frac{250 \text{ k}\Omega}{R_G} \quad (1)$$

Where: R_G is the external gain resistor.

Accuracy of the 250kΩ term is $\pm 40\%$.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

NOISE PERFORMANCE

The INA131 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA131 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of state-of-the-art chopper-stabilized amplifiers.

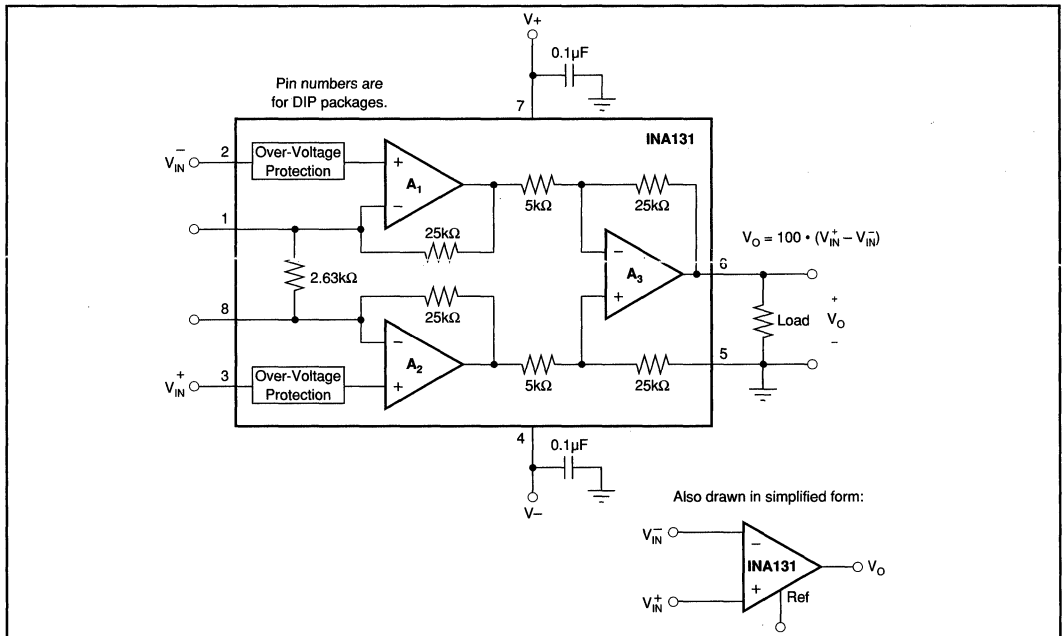


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA131 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

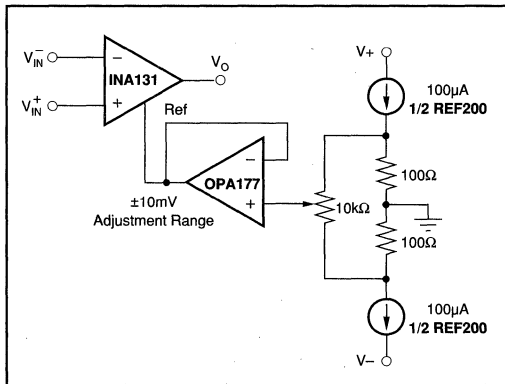


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA131 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA131 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA131 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA131 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The 5V/V output stage gain of the INA131 reduces this effect. Compared to the

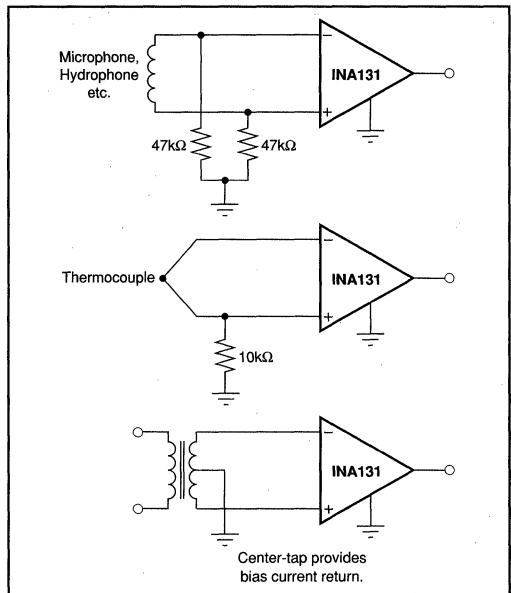


FIGURE 3. Providing an Input Common-Mode Current Path.

INA114 and other unity output gain instrumentation amplifiers, the INA131 provides several additional volts of input common-mode range with full output voltage swing. See the typical performance curve "Input Common-Mode Range vs Output Voltage".

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA131 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA131 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

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OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA131 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA131.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 4 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1 . Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 5).

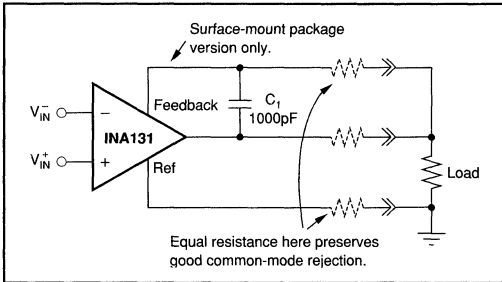


FIGURE 4. Remote Load and Ground Sensing.

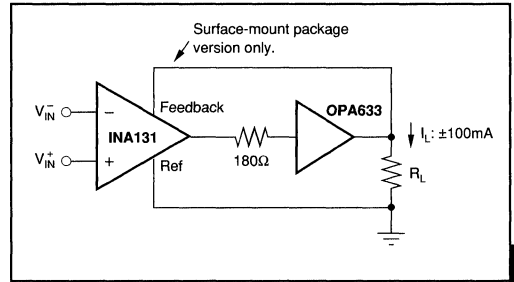


FIGURE 5. Buffered Output for Heavy Loads.

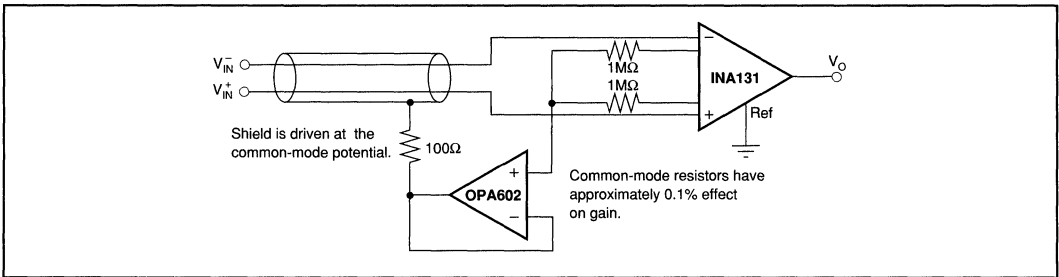


FIGURE 6. Shield Driver Circuit.

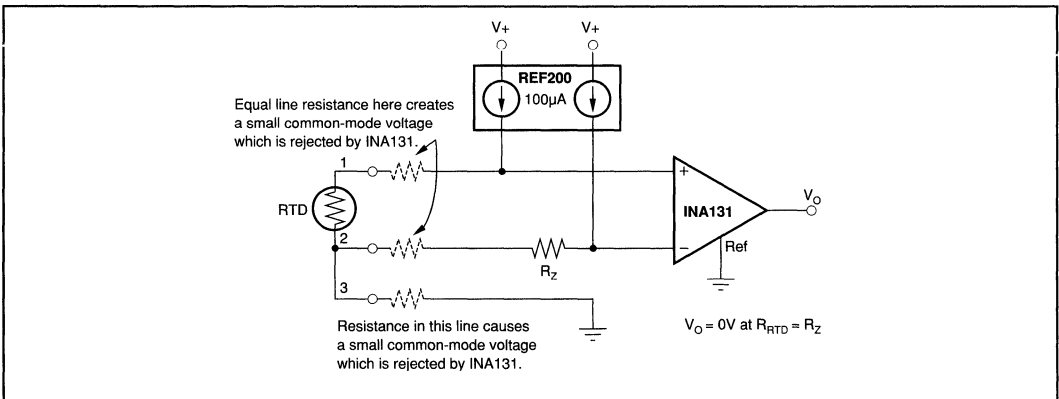


FIGURE 7. RTD Temperature Measurement Circuit.

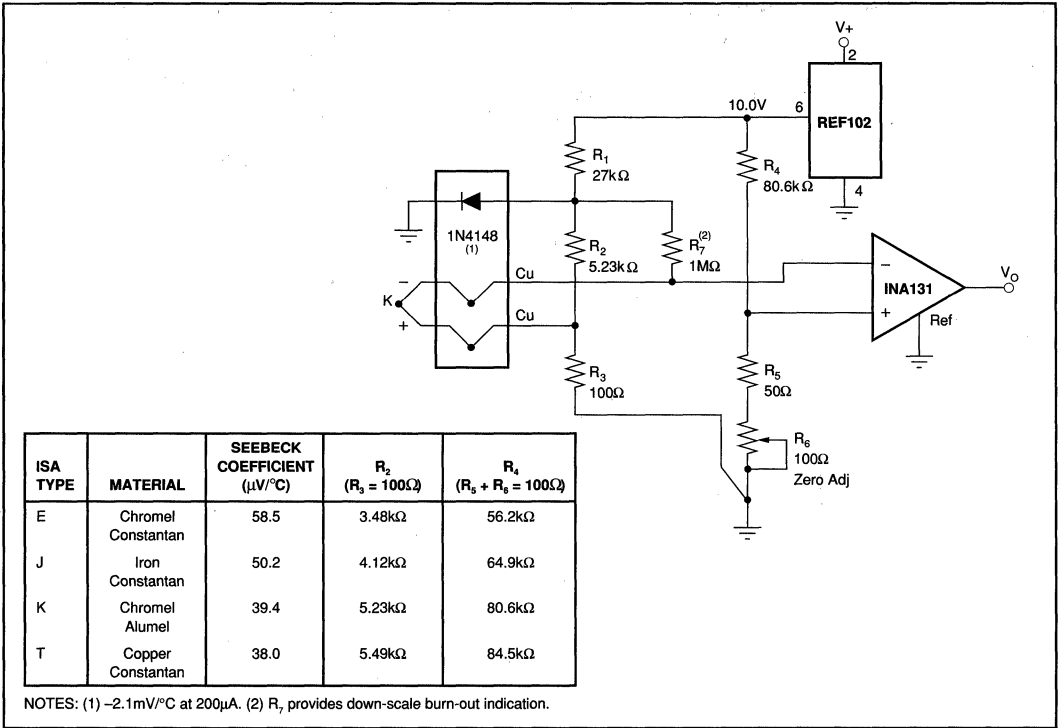


FIGURE 9. Thermocouple Amplifier with Cold Junction Compensation.

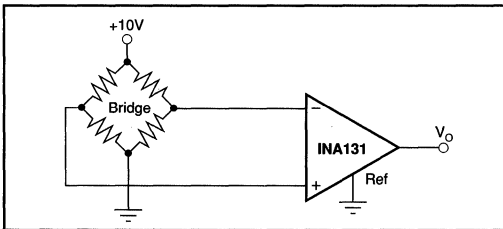


FIGURE 9. Bridge Transducer Amplifier.

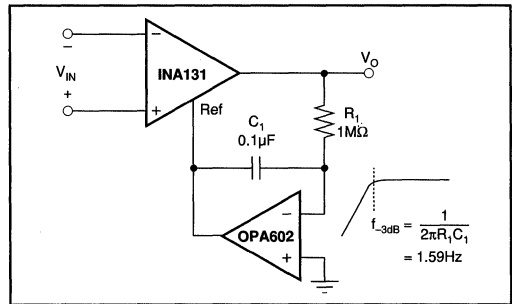


FIGURE 10. AC-Coupled Instrumentation Amplifier.

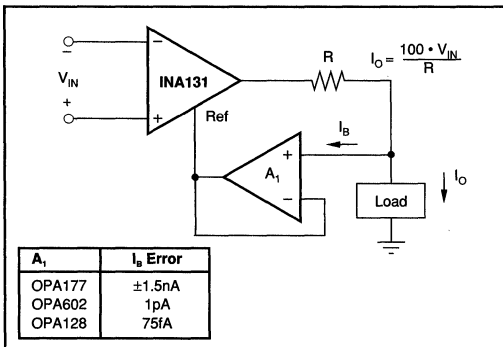
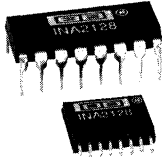


FIGURE 11. Differential Voltage to Current Converter.

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INA2128

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

Dual, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 75 μ V max
- LOW DRIFT: 0.75 μ V/ $^{\circ}$ C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH CMR: 110dB min
- INPUTS PROTECTED TO \pm 40V
- WIDE SUPPLY RANGE: \pm 2.25 to \pm 18V
- LOW QUIESCENT CURRENT: 1mA Total
- 16-PIN PLASTIC DIP, SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

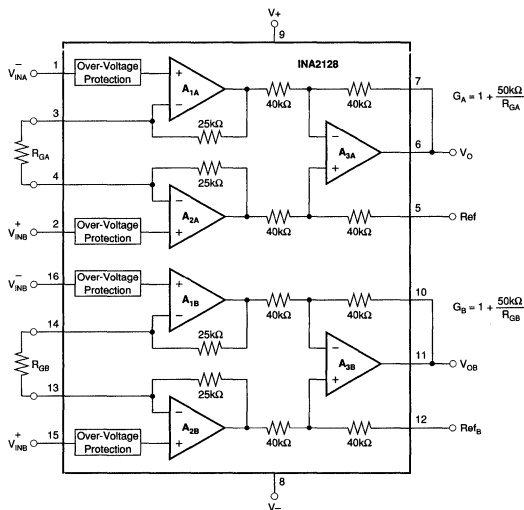
DESCRIPTION

The INA2128 is a low power, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G=100).

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to \pm 40V without damage.

The INA2128 is laser trimmed for very low offset voltage (75 μ V), drift (0.75 μ V/ $^{\circ}$ C) and high common-mode rejection (110dB at G = 1000). It operates with power supplies as low as \pm 2.25V, and quiescent current is only 500 μ A per amplifier—ideal for battery operated systems.

The INA2128 is available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the -40° C to $+85^{\circ}$ C temperature range.



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PDS-1243

4.145

INA2128

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ unless otherwise noted.

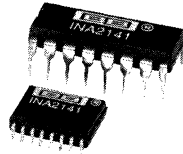
PARAMETER	CONDITIONS	INA2128P, U			INA2128PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								μV
Initial	$T_A = +25^\circ\text{C}$		$\pm 10 \pm 50/\text{G}$	$\pm 75 \pm 750/\text{G}$		$\pm 25 \pm 100/\text{G}$	$\pm 125 \pm 1000/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}		$\pm 0.2 \pm 2/\text{G}$	$\pm 0.75 \pm 20/\text{G}$		$\pm 0.2 \pm 5/\text{G}$	$\pm 1 \pm 20/\text{G}$	$\mu\text{V}/\text{mo}$
vs Power Supply	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		$\pm 1 \pm 10/\text{G}$	$\pm 5 \pm 100/\text{G}$		*	$\pm 10 \pm 100/\text{G}$	$\Omega \parallel \text{pF}$
Long-Term Stability			$\pm 0.4 \pm 5/\text{G}$			*		$\Omega \parallel \text{pF}$
Impedance, Differential			$10^{10} \parallel 1$			*		V
Common-Mode			$10^{10} \parallel 4$			*		V
Linear Input Voltage Range	$V_O = 0\text{V}$		(V+) - 2 (V-) + 2			*		V
Safe Input Voltage				± 40		*		V
Common-Mode Rejection	$V_{\text{CM}} = \pm 12.5\text{V}$, $\Delta R_S = 1\text{k}\Omega$					*		dB
	G=1	80	90		73	*		dB
	G=10	97	110		89	*		dB
	G=100	107	120		98	*		dB
	G=1000	110	125		100	*		dB
BIAS CURRENT			± 1	2		*	± 5	nA
vs Temperature			± 80			*		$\text{pA}/^\circ\text{C}$
Offset Current			± 1	2		*	± 5	nA
vs Temperature			± 80			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	G = 1000, $R_S = 0\Omega$							$\text{nV}/\sqrt{\text{Hz}}$
f = 10Hz			12			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			7			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			7			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.3			*		$\mu\text{Vp-p}$
Noise Current						*		$\text{pA}/\sqrt{\text{Hz}}$
f=10Hz			0.5			*		$\text{pA}/\sqrt{\text{Hz}}$
f=1kHz			0.3			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.5			*		pA p-p
GAIN								V/V
Gain Equation		1	$1 + (50\text{k}\Omega/R_G)$	10000	*	*	*	V/V
Range of Gain						*	*	%
Gain Error	G=1		± 0.01	± 0.024		*	± 0.1	%
	G=10		± 0.02	± 0.4		*	± 0.5	%
	G=100		± 0.05	± 0.5		*	± 0.7	%
	G=1000		± 0.5	± 1		*	± 2	%
Gain vs Temperature	G=1		± 1	± 10		*	± 10	$\text{ppm}/^\circ\text{C}$
50k Ω Resistance ⁽¹⁾			± 25	± 100		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	G=1		± 0.0003	± 0.001		*	± 0.002	% of FSR
	G=10		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G=100		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G=1000		± 0.002	± 0.01		*	± 0.02	% of FSR
OUTPUT								V
Voltage: Positive	$R_L = 10\text{k}\Omega$	(V+) - 1	(V+) - 0.8		*	*		V
Negative	$R_L = 10\text{k}\Omega$	(V-) + 1	(V-) + 0.8		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+5/-12			*		mA
FREQUENCY RESPONSE								kHz
Bandwidth, -3dB	G=1		700			*		kHz
	G=10		700			*		kHz
	G=100		200			*		kHz
	G=1000		20			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$, G=10		4.5			*		$\text{V}/\mu\text{s}$
Settling Time, 0.01%	G=1		6			*		μs
	G=10		6			*		μs
	G=100		8			*		μs
	G=1000		70			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								V
Voltage Range		± 2.25	± 15	± 18	*	*	*	V
Current, Per Amplifier	$V_{\text{IN}} = 0\text{V}$		± 500			*		μA
TEMPERATURE RANGE								$^\circ\text{C}$
Specification		-40		85	*	*	*	$^\circ\text{C}$
Operating		-40		125	*	*	*	$^\circ\text{C}/\text{W}$
θ_{JA}			80			*		$^\circ\text{C}/\text{W}$

* Specification same as INA2128PB, UB.

NOTE: (1) Temperature coefficient of the "50k Ω " term in the gain equation.

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INA2141

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

Dual, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 80 μ V max
- **LOW DRIFT:** 1 μ V/ $^{\circ}$ C max
- **EXCELLENT GAIN ACCURACY:**
 \pm 0.01% at G=10
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH CMR:** 107dB min
- **INPUTS PROTECTED TO \pm 40V**
- **WIDE SUPPLY RANGE:** \pm 2.25 to \pm 18V
- **LOW QUIESCENT CURRENT:** 1mA Total
- **16-PIN PLASTIC DIP, SOL-16**

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

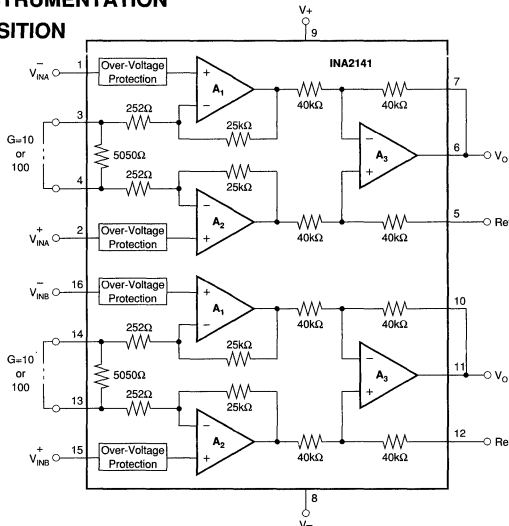
DESCRIPTION

The INA2141 is a low power, dual instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G=100).

Simple pin connections set an accurate gain of 10 or 100V/V without external resistors. Internal input protection can withstand up to \pm 40V without damage.

The INA2141 is laser trimmed for very low offset voltage (80 μ V), drift (1 μ V/ $^{\circ}$ C) and high common-mode rejection (107dB at G=100). It operates with power supplies as low as \pm 2.25V, and quiescent current is only 500 μ A per amplifier—ideal for battery operated systems.

The INA2141 is available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the -40° C to $+85^{\circ}$ C temperature range.



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PDS-1244

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INA2141

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

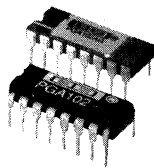
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	INA2141P, U			INA2141PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	G = 10		± 20	± 150		± 50	± 250	μV
	G = 100		± 15	± 80		± 25	± 150	μV
vs Temperature	G = 10		0.5	3		*	5	$\mu\text{V}/^\circ\text{C}$
	G = 100		0.2	1		*	2	$\mu\text{V}/^\circ\text{C}$
vs Power Supply	G = 10		2	15		*	20	$\mu\text{V}/\text{V}$
	G = 100		1	5		*	10	$\mu\text{V}/\text{V}$
Long-Term Stability	G = 10		1			*		$\mu\text{V}/\text{mo}$
	G = 100		0.5			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{10} \parallel 1$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{10} \parallel 4$			*		$\Omega \parallel \text{pF}$
Linear Input Voltage Range			(V+) - 2			*		V
			(V-) + 2			*		V
Safe Input Voltage				± 40		*		V
Common-Mode Rejection	$V_{\text{CM}} = \pm 12.5\text{V}$, $\Delta R_S = 1\text{k}\Omega$					*		
	G = 10	97	110		89	*		dB
	G = 100	107	120		98	*		dB
BIAS CURRENT								
vs Temperature			± 1	± 2		*	± 5	nA
Offset Current			± 80	± 2		*		$\text{pA}/^\circ\text{C}$
vs Temperature			± 1	± 2		*	± 5	nA
			± 80			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	G = 100, $R_S = 0\Omega$					*		
f = 10Hz			12			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			7			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			7			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.3			*		$\mu\text{Vp-p}$
	G = 10, $R_S = 0\Omega$					*		
f = 10Hz			25		*	*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			12		*	*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			12		*	*		$\text{nV}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			0.6		*	*		$\mu\text{Vp-p}$
Noise Current						*		
f = 10Hz			0.5			*		$\text{pA}/\sqrt{\text{Hz}}$
f = 1kHz			0.3			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_b = 0.1\text{Hz}$ to 10Hz			25			*		pAp-p
GAIN								
Gain Error	G = 100		± 0.02	± 0.15		*	*	%
	G = 10		0.01	0.025		*	0.05	%
Gain vs Temperature	G = 10, 100		± 1	± 10		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity	G = V10		± 0.0005	± 0.002		*	± 0.004	% of FSR
	G = 100		± 0.0005	± 0.002		*	± 0.004	% of FSR
OUTPUT								
Voltage: Positive	$R_L = 10\text{k}\Omega$	(V+) - 1	(V+) - 0.8		*	*		V
Negative	$R_L = 10\text{k}\Omega$	(V-) + 1	(V-) + 0.8		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+5/-12			*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	G = 10		700			*		kHz
	G = 100		200			*		kHz
Slew Rate	$V_O = \pm 10\text{V}$, G = 10		4.5			*		V/ μs
Settling Time, 0.01%	G = 10		6			*		μs
	G = 100		8			*		μs
Overload Recovery	50% Overdrive		4			*		μs
POWER SUPPLY								
Voltage Range		± 2.25	± 15	± 18	*	*	*	V
Current, Per Amplifier	$V_{\text{IN}} = 0\text{V}$		± 500			*		μA
TEMPERATURE RANGE								
Specification		-40		85	*	*	*	$^\circ\text{C}$
Operating		-40		125	*	*	*	$^\circ\text{C}$
θ_{JA}			80			*		$^\circ\text{C}/\text{W}$

* Specification same as INA2141P, U.

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PGA102

High Speed PROGRAMMABLE GAIN AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**
G = 1, 10, 100
- **LOW GAIN ERROR: 0.025% max**
- **FAST SETTLING: 2.8μs to 0.01%**
- **16-PIN PLASTIC AND CERAMIC DIP**

APPLICATIONS

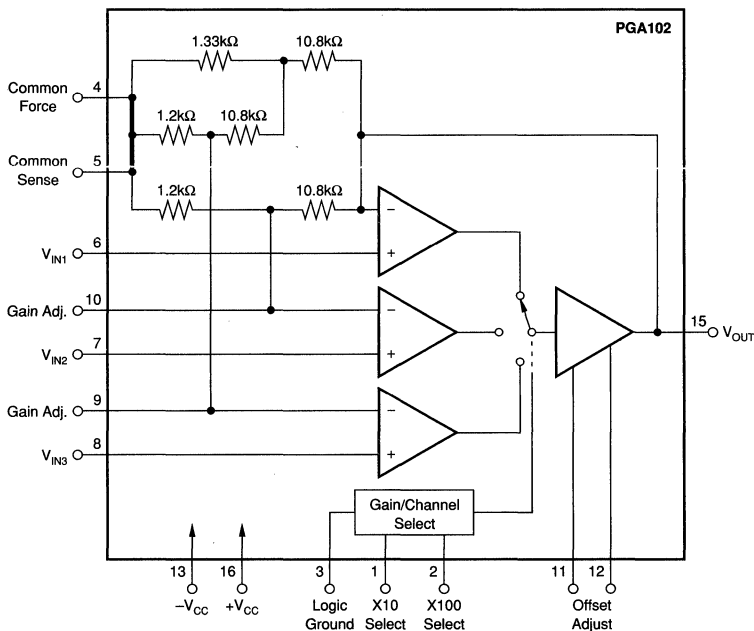
- **DATA ACQUISITION AMPLIFIER**
- **FIXED-GAIN AMPLIFIER**
- **AUTOMATIC GAIN SCALING**

DESCRIPTION

The PGA102 is a high speed, digitally programmable-gain amplifier. CMOS/TTL-compatible inputs select gains of 1, 10 or 100V/V. Each gain has an independent input terminal, providing an input multiplexer function.

On-chip metal film gain-set resistors are laser-trimmed to provide excellent gain accuracy. High speed input circuitry allows multiplexing of high speed signals.

The PGA102 is available in 16-pin plastic and ceramic DIP packages. Commercial, industrial and military temperature range models are available.



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PDS-579C

4.149

PGA102

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC} = 15\text{VDC}$ unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG			PGA102BG, SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN Inaccuracy ⁽¹⁾ vs Temperature Nonlinearity	$R_L = 2\text{k}\Omega, G = 1$		± 0.007	± 0.02		± 0.003	± 0.01		*	*	%
	$G = 10$		± 0.015	± 0.03		± 0.01	± 0.02		*	± 0.05	%
	$G = 100$		± 0.02	± 0.05		± 0.015	± 0.025		*	± 0.06	%
	$G = 1$		± 0.4	± 5		*	*		*	*	ppm/°C
	$G = 10$		± 2	± 7		*	*		*	*	ppm/°C
	$G = 100$		± 7	± 20		*	*		± 9	*	ppm/°C
	$R_L = 2\text{k}\Omega, G = 1$		0.001	0.003		*	*		*	*	% of FS
	$G = 10$		0.002	0.005		*	*		*	*	% of FS
	$G = 100$		0.003	0.01		*	*		*	*	% of FS
RATED OUTPUT Voltage Current Short Circuit Current Output Resistance Load Capacitance	$R_L = 2\text{k}\Omega$	± 10	± 12.5		*	*		*	*		V
	$V_{OUT} = 10\text{V}$	± 5	± 10		*	*		*	*		mA
		± 10	± 25		*	*		*	*		mA
			0.01		*	*		*	*		Ω
	For Stable Operation		2000		*	*		*	*		pF
INPUT OFFSET VOLTAGE Initial ⁽²⁾ vs Temperature vs Supply Voltage	$G = 1$		± 200	± 500		± 100	± 250		*	± 1500	μV
	$G = 10$		± 70	± 200		± 50	± 100		*	± 600	μV
	$G = 100$		± 70	± 200		± 50	± 100		*	± 600	μV
	$G = 1$		± 5	± 20		*	*		± 7	± 50	$\mu\text{V}/^\circ\text{C}$
	$G = 10$		± 1	± 7		*	*		± 3	± 10	$\mu\text{V}/^\circ\text{C}$
	$G = 100$		± 0.5	± 3		*	*		± 2	± 7	$\mu\text{V}/^\circ\text{C}$
	$\pm 5 < V_{CC} < \pm 18\text{V}$										
	$G = 1$		± 30	± 70		*	*		*	*	$\mu\text{V}/\text{V}$
	$G = 10$		± 8	± 30		*	*		*	*	$\mu\text{V}/\text{V}$
	$G = 100$		± 8	± 30		*	*		*	*	$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT Initial Over Temperature	$T_A = +25^\circ\text{C}$		± 20	± 50		*	*		*	*	nA
	$T_{A\text{MIN}}$ to $T_{A\text{MAX}}$		± 25	± 60		*	*		*	*	nA
ANALOG INPUT CHARACTERISTICS Voltage Range Resistance Capacitance	Linear Operation	± 10	± 12		*	*		*	*		V
			7×10^8			*			*		Ω
			4			*			*		pF
INPUT NOISE Voltage Noise Voltage Noise Density Current Noise Current Noise Density	$f_b = 0.1\text{Hz}$ to 10Hz					*			*		$\mu\text{Vp-p}$
	$G = 1$		4.5			*			*		$\mu\text{Vp-p}$
	$G = 10$		1.5			*			*		$\mu\text{Vp-p}$
	$G = 100$		0.6			*			*		$\mu\text{Vp-p}$
	$f_o = 1\text{Hz}, G = 1$		490			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 10$		178			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 100$		83			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 10\text{Hz}, G = 1$		155			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 10$		56			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 100$		20			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 100\text{Hz}, G = 1$		93			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 100$		31			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 100$		18			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$f_o = 1\text{kHz}, G = 1$		79			*			*		$\text{nV}/\sqrt{\text{Hz}}$
	$G = 10$		31			*			*		$\text{nV}/\sqrt{\text{Hz}}$
$G = 100$		18			*			*		$\text{nV}/\sqrt{\text{Hz}}$	
$f_b = 0.1\text{Hz}$ to 10Hz		76			*			*		pAp-p	
$f_o = 1\text{Hz}$		8.8			*			*		$\text{pA}/\sqrt{\text{Hz}}$	
$f_o = 10\text{Hz}$		2.8			*			*		$\text{pA}/\sqrt{\text{Hz}}$	
$f_o = 100\text{Hz}$		0.99			*			*		$\text{pA}/\sqrt{\text{Hz}}$	
$f_o = 1\text{kHz}$		0.43			*			*		$\text{pA}/\sqrt{\text{Hz}}$	
DYNAMIC RESPONSE $\pm 3\text{dB}$ Bandwidth Full Power Bandwidth Slew Rate	Small Signal, $G = 1$		1500			*			*		kHz
	$G = 10$		750			*			*		kHz
	$G = 100$		250			*			*		kHz
	$V_{OUT} = \pm 10\text{V}, R_L = 2\text{k}\Omega$		160				*		*		kHz
	$V_{OUT} = \pm 10\text{V Step}, R_L = 2\text{k}\Omega$	6	9		*	*		*	*		V/ μs

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SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, $\pm V_{CC} = 15\text{VDC}$ unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG			PGA102BG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time (0.1%)	$V_{OUT} = 10\text{V Step}, G = 1$		1.6			*			*		μs
	$G = 10$		2.2			*			*		μs
	$G = 100$		5.2			*			*		μs
Settling Time (0.01%)	$V_{OUT} = 10\text{V Step}, G = 1$		2.8			*			*		μs
	$G = 10$		2.8			*			*		μs
	$G = 100$		8.2			*			*		μs
Overload Recovery Time, 0.1%	50% Overdrive, $G = 1$ (see Performance Curve)		2.5			*			*		μs
CROSSTALK											
DC	$\pm 10\text{V}$ to Both Off Channels		-155			*			*		dB
60Hz	$\pm 10\text{V}$ to Both Off Channels		-144			*			*		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	$V_{IL}^{(3)}$ on Pin 1 or 2				VLTC+0.8				*		V
Input "Low" Current					1				*		μA
Input "High" Threshold	$V_{IH}^{(3)}$ on Pin 1 or 2	VLTC+2			1	*		*	*		V
Input "High" Current			0.1		1	*	*	*	*		μA
Logic Threshold Control	VLTC on Pin 3	$-V_{CC}$			$V_{CC} - 4$	*		*	*		V
Switching Time ⁽⁴⁾	Between Channels		1			*		*	*		μs
POWER SUPPLY											
Rated Voltage			± 15			*		*	*		VDC
Voltage Range		± 5		± 18	*	*	*	*	*		VDC
Quiescent Current	$V_{OUT} = 0\text{V}$ No External Load, $V_{OUT} = \pm 10\text{V}$		± 2.4	± 3.3						*	mA
				± 5.3			*		*		mA
TEMPERATURE RANGE											
Specification, KP Grade	$T_{A\text{ MIN}}$ to $T_{A\text{ MAX}}$					*		0		+70	°C
AG and BG Grades		-25		+85		*					°C
SG Grade						-55		+125			°C
Operating		-55		+125		*		*	-25	+85	°C
Storage		-65		+150		*		*	-55	+125	°C
Thermal Resistance	θ_{JA}		100			*		*	*		°C/W

* Specification same as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately $\pm 0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

PGA102

4

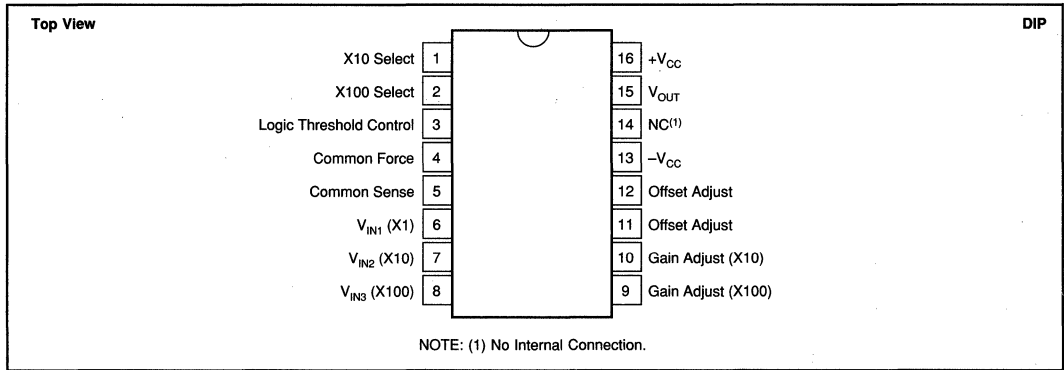
INSTRUMENTATION AMPLIFIERS

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply	±18V
Input Voltage Range: Analog	±V _{CC}
Digital	(V _{pin3} - 5.6V) to +V _{CC}
Storage Temperature Range: G Package	-65°C to +150°C
P Package	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration	Continuous to Common
Junction Temperature: G Package	+175°C
P Package	+110°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PGA102AG	16-Pin Hermetic DIP	109
PGA102BG	16-Pin Hermetic DIP	109
PGA102SG	16-Pin Hermetic DIP	109
PGA102KP	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

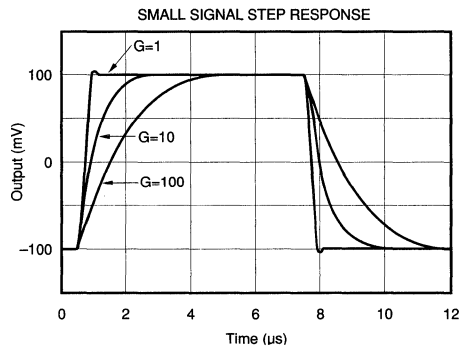
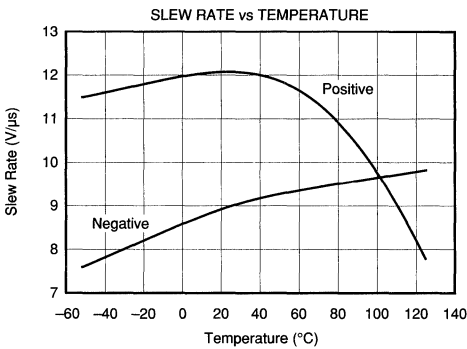
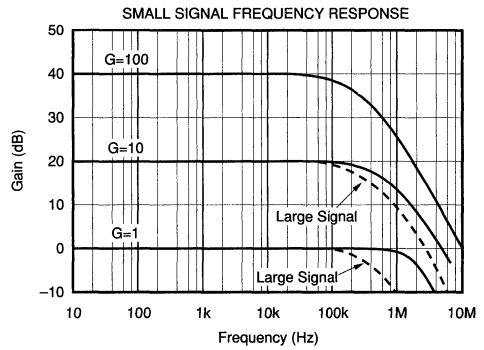
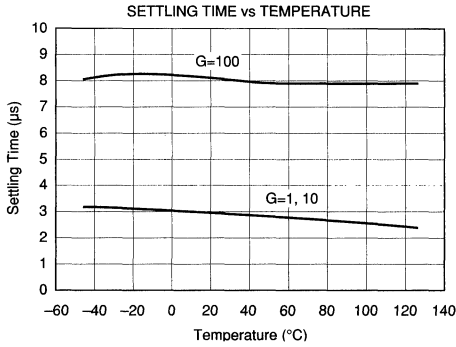
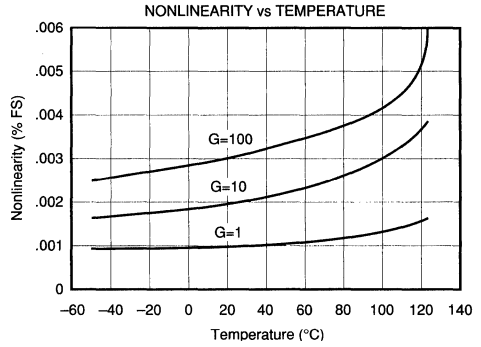
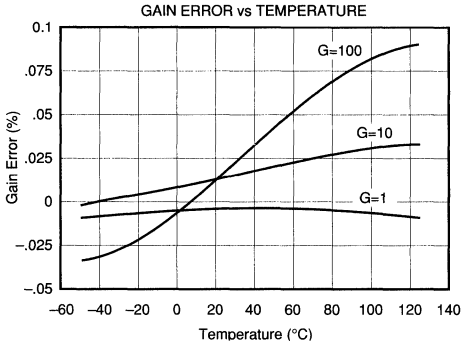
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA102AG	16-Pin Hermetic DIP	-25°C to +85°C
PGA102BG	16-Pin Hermetic DIP	-25°C to +85°C
PGA102SG	16-Pin Hermetic DIP	-55°C to +125°C
PGA102KP	16-Pin Plastic DIP	0°C to +70°C

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

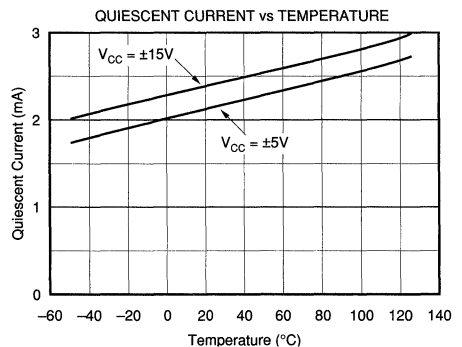
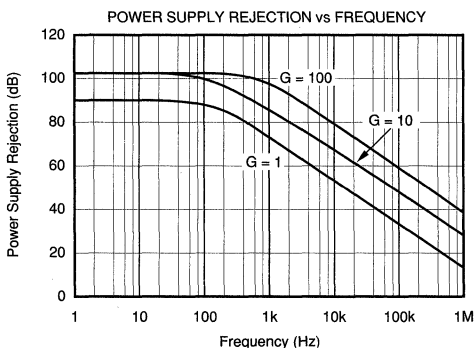
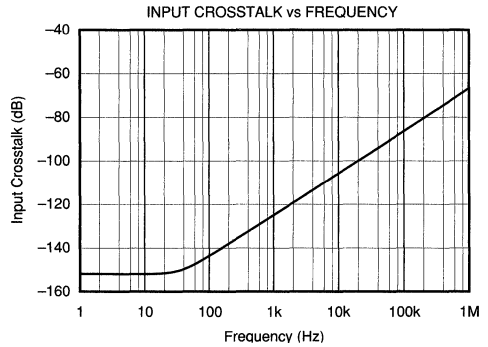
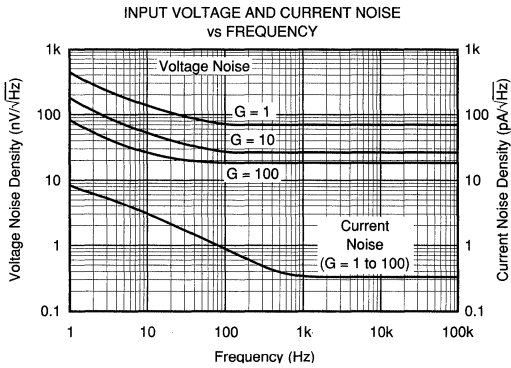
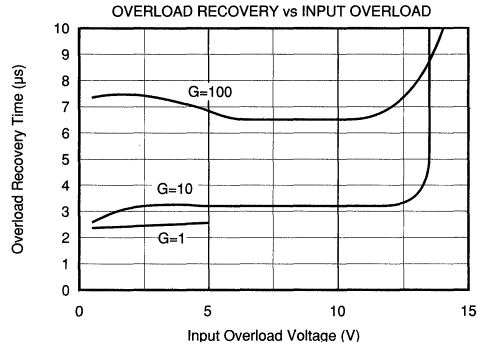
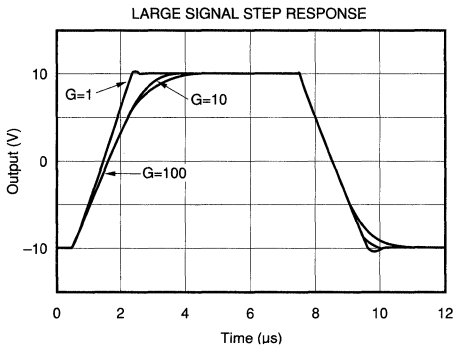
$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$ unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA102. Power supplies should be bypassed with 0.1µF capacitors located close to the device pins.

The inputs for each gain are independent and can be connected to three separate signal sources. Or, for many applications, the three inputs are connected in parallel to form a single input—see Figure 1. Only the input corresponding to the selected gain is active, operating as a non-inverting amplifier. The two inactive inputs behave as open circuits. The input bias current of the inactive inputs is negligible compared to that of the selected input.

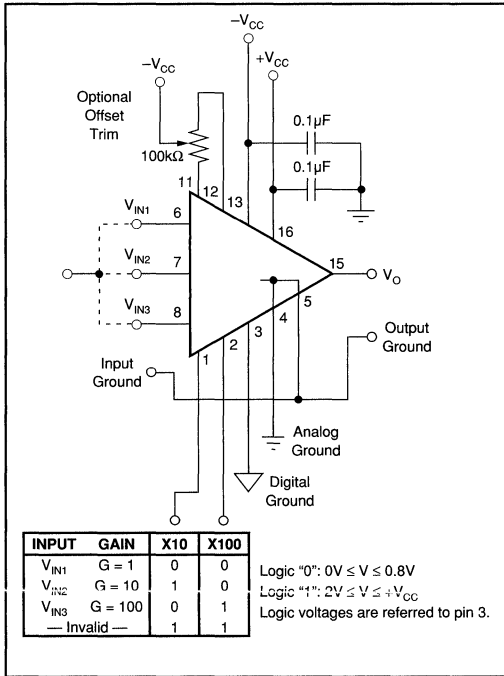


FIGURE 1. Basic Circuit Connections.

DIGITAL INPUTS

Gain is selected by the digital input pins, "X10" and "X100". The threshold of these logic inputs is approximately 1.3V above the voltage on pin 3. For CMOS or TTL logic signals, connect pin 3 to logic ground. The logic inputs are not latched. Any change logic inputs immediately selects a new gain. Switching time is approximately 1µs. This does not include the time required for the analog output to settle to a new output value (see settling time specifications).

Note that the two logic inputs allow four possible logic states—see Figure 1 for the logic table. A logic "1" on both inputs is an invalid code. This will not damage the device, but the analog output voltage will not be predictable while this code is applied.

OFFSET ADJUSTMENT

The offset voltage of each of the three input stages is laser-trimmed. Many applications require no further adjustment. The optional trim circuit shown in Figure 1 can be used to adjust the offset voltage. This adjustment affects the offset of all three gain channels. Since each gain setting may require a different adjustment of the potentiometer, this requires a compromise. Often, offset voltage of the G = 100 channel is the most important, so adjustment can be optimized for this channel only. Alternatively, Figure 2 shows a CMOS switch used to select independent offset adjustment potentiometers for each of the three channels.

Use these offset adjustment techniques only to null the offset voltage of the PGA102. Do not null offset produced by the signal source or other system offsets or this will increase the temperature drift of the PGA102.

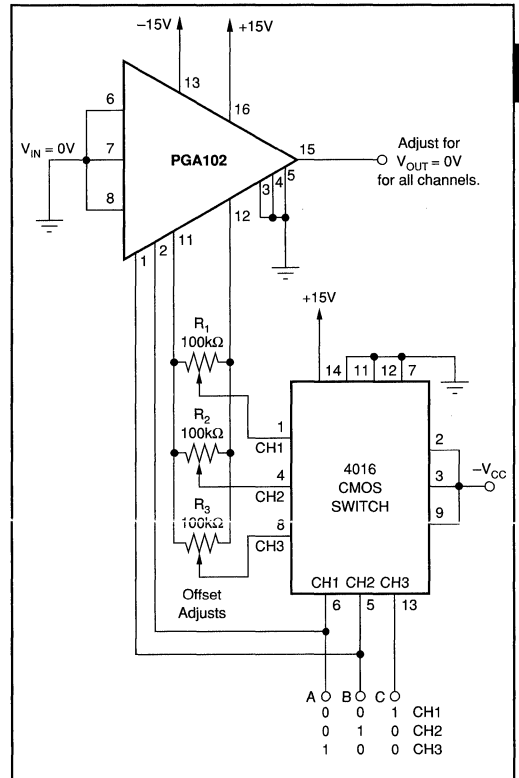


FIGURE 2. Independent Offset Adjustment of Channels 1, 2, and 3.

GAIN ADJUSTMENT

Gain of the PGA102 is accurately laser trimmed and usually requires no further adjustment. The optional circuit in Figure 3 allows independent gain adjustment of the G = 10 and G = 100 inputs.

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The gain of the $G = 10$ and $G = 100$ inputs can be changed by adding external resistors to the internal feedback network as shown in Figures 4 and 5. The internal gain-set resistors are trimmed for precise ratios, not to exact values. The internal resistor values are within approximately $\pm 30\%$ of

the nominal values shown on the front page diagram. This makes the external resistor values in Figures 4 and 5 subject to variation—especially for gains differing greatly from the initial value.

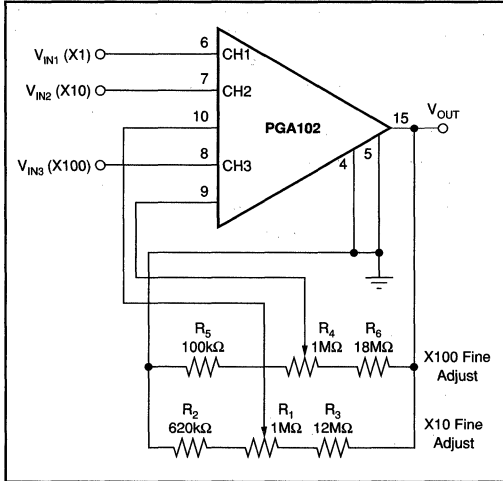


FIGURE 3. Optional Fine Gain Adjustment.

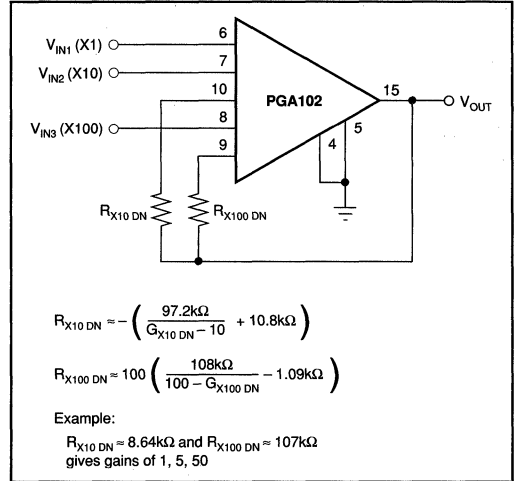


FIGURE 5. Connections for Lower Gains.

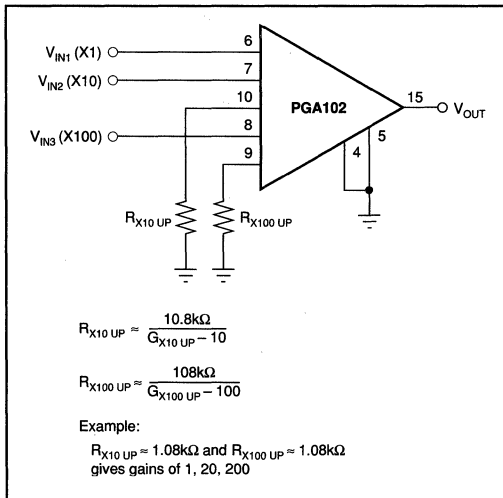


FIGURE 4. Connections for Higher Gains.

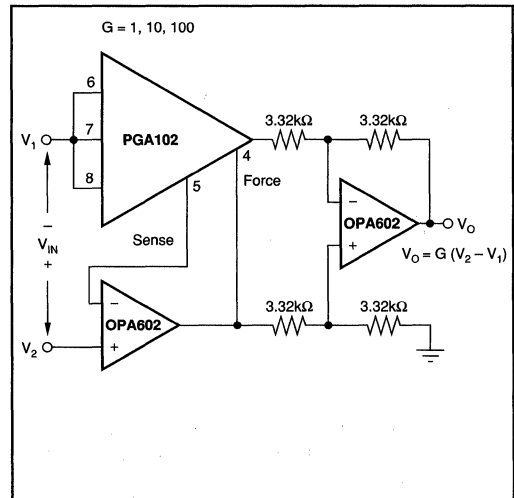
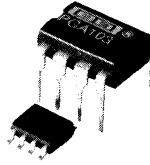


FIGURE 6. High-Speed Instrumentation Amplifier.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



PGA103



Programmable Gain AMPLIFIER

FEATURES

- DIGITALLY PROGRAMMABLE GAINS:
G=1, 10, 100V/V
- CMOS/TTL-COMPATIBLE INPUTS
- LOW GAIN ERROR: $\pm 0.05\%$ max, G=10
- LOW OFFSET VOLTAGE DRIFT: $2\mu\text{V}/^\circ\text{C}$
- LOW QUIESCENT CURRENT: 2.6mA
- LOW COST
- 8-PIN PLASTIC DIP, SO-8 PACKAGES

APPLICATIONS

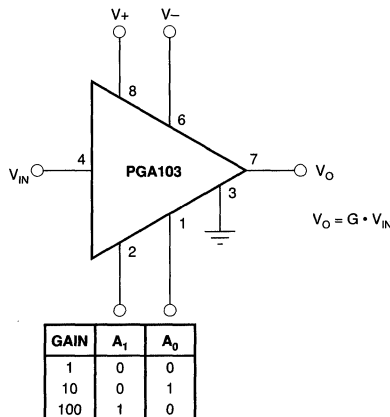
- DATA ACQUISITION SYSTEMS
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

DESCRIPTION

The PGA103 is a programmable-gain amplifier for general purpose applications. Gains of 1, 10 or 100 are digitally selected by two CMOS/TTL-compatible inputs. The PGA103 is ideal for systems that must handle wide dynamic range signals.

The PGA103's high speed circuitry provides fast settling time, even at G=100 (8 μs to 0.01%). Bandwidth is 250kHz at G=100, yet quiescent current is only 2.6mA. It operates from $\pm 4.5\text{V}$ to $\pm 18\text{V}$ power supplies.

The PGA103 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the -40°C to $+85^\circ\text{C}$ temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1208B

4.157

PGA103
4
INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise specified.

PARAMETER	CONDITIONS	PGA103P, U			UNITS
		MIN	TYP	MAX	
INPUT					
Offset Voltage, RTI					
G=1	$T_A = +25^\circ\text{C}$		± 200	± 1500	μV
G=10			± 100	± 500	μV
G=100			± 100	± 500	μV
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}				
G=1			± 5		$\mu\text{V}/^\circ\text{C}$
G=10			± 2		$\mu\text{V}/^\circ\text{C}$
G=100			± 2		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$				
G=1			30	70	$\mu\text{V}/\text{V}$
G=10			10	35	$\mu\text{V}/\text{V}$
G=100			10	35	$\mu\text{V}/\text{V}$
Impedance			$10^9 \parallel 2$		$\Omega \parallel \text{pF}$
INPUT BIAS CURRENT					
Initial Bias Current			± 50	± 150	nA
vs Temperature			± 100		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	$G=100$, $R_S = 0\Omega$				
f=10Hz			16		$\text{nV}/\sqrt{\text{Hz}}$
f=100Hz			11		$\text{nV}/\sqrt{\text{Hz}}$
f=1kHz			11		$\text{nV}/\sqrt{\text{Hz}}$
f _B =0.1Hz to 10Hz			0.6		$\mu\text{Vp-p}$
NOISE CURRENT					
f=10Hz			2.8		$\text{pA}/\sqrt{\text{Hz}}$
f=1kHz			0.3		$\text{pA}/\sqrt{\text{Hz}}$
f _B =0.1Hz to 10Hz			76		pAp-p
GAIN					
Gain Error					
G=1			± 0.005	± 0.02	%
G=10			± 0.02	± 0.05	%
G=100			± 0.04	± 0.2	%
Gain vs Temperature					
G=1			± 2		$\text{ppm}/^\circ\text{C}$
G=10			± 10		$\text{ppm}/^\circ\text{C}$
G=100			± 30		$\text{ppm}/^\circ\text{C}$
Nonlinearity					
G=1			± 0.001	± 0.003	% of FSR
G=10			± 0.002	± 0.005	% of FSR
G=100			± 0.004	± 0.01	% of FSR
OUTPUT					
Voltage, Positive		(V+) -3.5	(V+) -2.5		V
Negative		(V-) +3.5	(V-) +2.5		V
Load Capacitance, max			1000		pF
Short Circuit Current			± 25		mA
FREQUENCY RESPONSE					
Bandwidth, -3dB					
G=1	$V_O = \pm 10\text{V}$		1.5		MHz
G=10			750		kHz
G=100			250		kHz
Slew Rate			9		$\text{V}/\mu\text{s}$
Settling Time, 0.1%					
G=1			2		μs
G=10			2.2		μs
G=100			6.5		μs
Settling Time, 0.01%					
G=1			2.5		μs
G=10			2.5		μs
G=100			8		μs
Overload Recovery	50% Overdrive		2.5		μs
DIGITAL LOGIC INPUTS					
Digital Low Voltage		-5.6		0.8	V
Digital Low or High Current			1		μA
Digital High Voltage		2		V+	V

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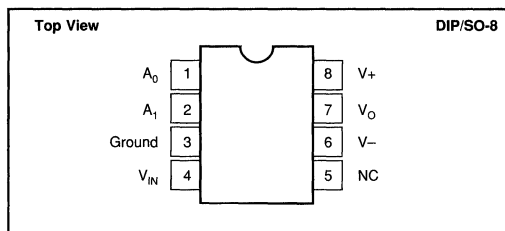
SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise specified.

PARAMETER	CONDITIONS	PGA103P, U			UNITS
		MIN	TYP	MAX	
POWER SUPPLY					
Voltage Range		± 4.5	± 15	± 18	V
Current	$V_{IN} = 0\text{V}$		± 2.6	± 3.5	mA
TEMPERATURE RANGE					
Specification		-40		+85	$^\circ\text{C}$
Operating		-40		+125	$^\circ\text{C}$
θ_{JA} : P or U Package			100		$^\circ\text{C/W}$

PIN CONFIGURATION



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA103P	8-Pin Plastic DIP	-40°C to $+85^\circ\text{C}$
PGA103U	SO-8 Surface Mount	-40°C to $+85^\circ\text{C}$



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18\text{V}$
Analog Input Voltage Range	V^- to V^+
Logic Input Voltage Range	V^- to V^+
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to $+125^\circ\text{C}$
Storage Temperature	-40°C to $+125^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PGA103P	8-Pin Plastic DIP	006
PGA103U	SO-8 Surface Mount	182

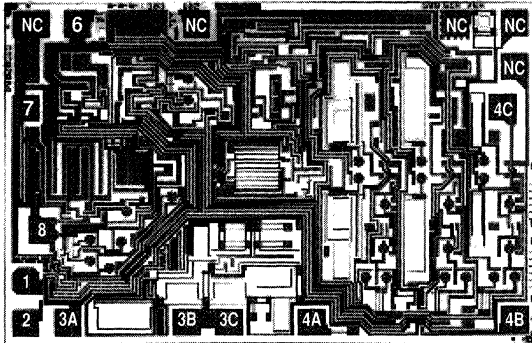
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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DICE INFORMATION



PGA103 DIE TOPOGRAPHY

PAD	FUNCTION
1	A ₀
2	A ₁
3A, 3B, 3C ⁽¹⁾	Ground
4A, 4B, 4C ⁽²⁾	V _{IN}
6	V ₋
7	V _O
8	V ₊

NC: No Connection

NOTES: (1) Connect all three indicated pads. (2) Connect all three indicated pads.

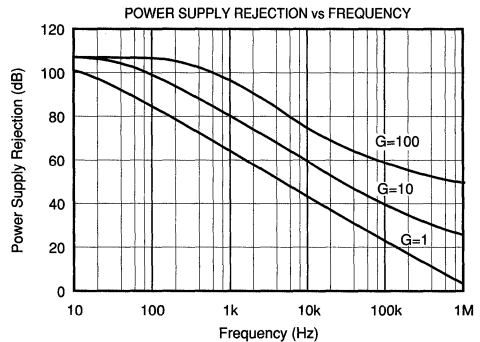
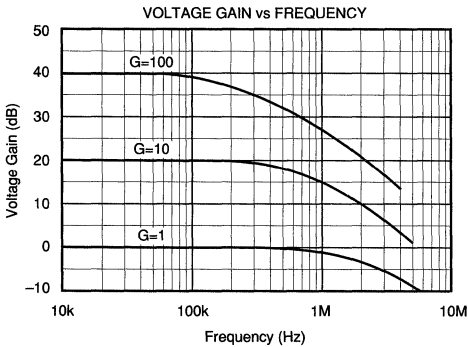
Substrate Bias: Internally connected to V₋ power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	69 x 105 ±5	1.75 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		Gold

TYPICAL PERFORMANCE CURVES

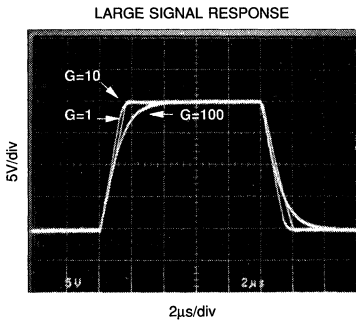
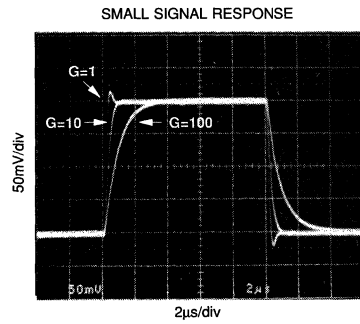
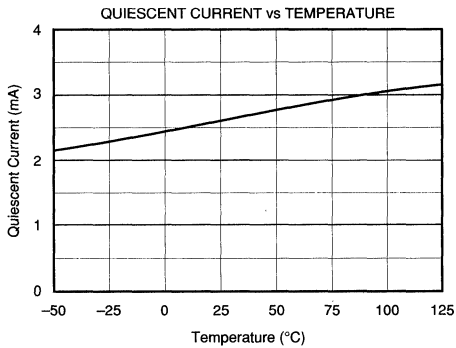
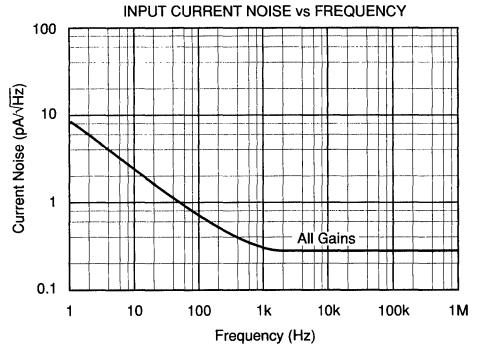
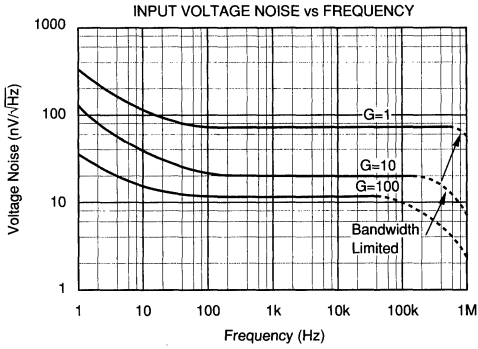
T_A = +25°C, V_s = ±15V unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA103. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

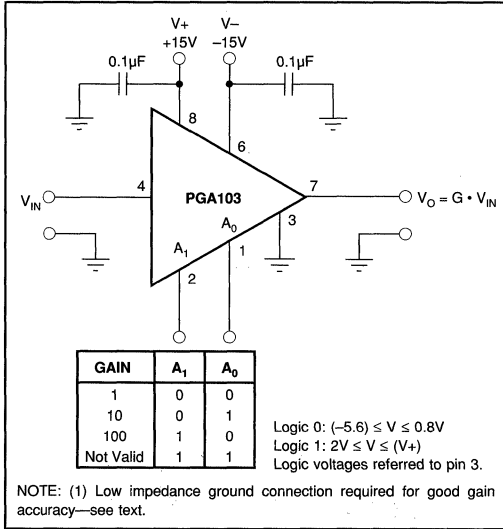


FIGURE 1. Basic Connections.

The input and output are referred to the ground terminal, pin 3. This must be a low-impedance connection to assure good gain accuracy. A resistance of 0.1Ω in series with the ground pin will cause the gain in $G=100$ to decrease by approximately 0.2%.

DIGITAL INPUTS

The digital inputs, A_0 and A_1 , select the gain according to the logic table in Figure 1. The digital inputs interface directly to common CMOS and TTL logic components. The logic inputs are referenced to the ground terminal, pin 3.

The logic table in Figure 1 shows that logic "1" on both A_0 and A_1 is invalid. This logic code will not cause damage, but the amplifier output will not be predictable while this code is selected. The output will recover when a valid code is selected.

The digital inputs are not latched, so a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately $0.5\mu s$. The time to respond to gain change is equal to the switching time plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control signals from a high speed data bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry to avoid coupling digital noise into the analog circuitry.

Some applications select gain of the PGA103 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch or jumper is off or open. Fixed-gain applications can connect the logic inputs directly to V_+ or ground (or other valid logic level) without a series resistor.

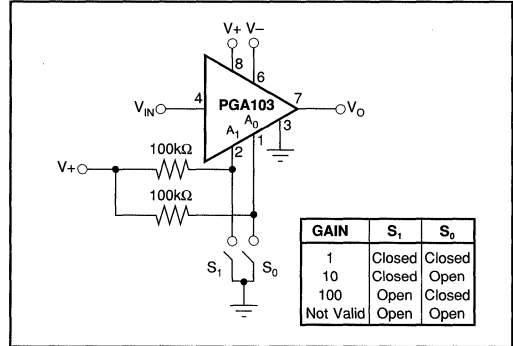


FIGURE 2. Switch or Jumper-Selected Gains.

OFFSET TRIMMING

Offset voltage is laser-trimmed to typically less than $200\mu V$ (referred to input) in all three gains. The input-referred offset voltage can be different for each gain.

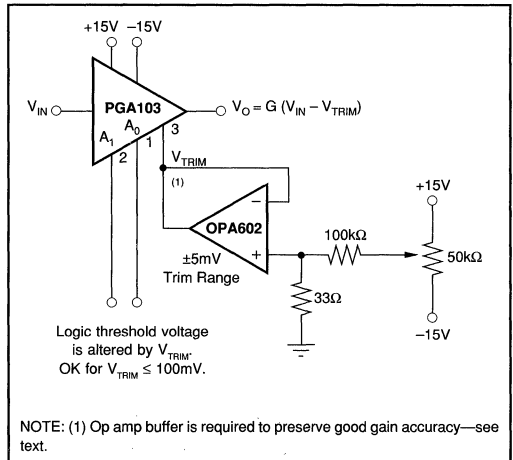


FIGURE 3. Offset Voltage Trim Circuit.

Figure 3 shows a circuit used to trim the offset voltage of the PGA103. An op amp buffers the trim voltage to provide a low impedance at the ground terminal. This is required to maintain accurate gain. Remember that the logic inputs, A_0 and A_1 , are referenced to this ground connection, so the logic threshold voltage will be affected by the trim voltage. This is insignificant if the offset adjustment is used only to trim offset voltage. If a large offset is used (greater than 0.1V), be sure that the logic input signals provide valid logic levels when referred to the voltage at the ground terminal, pin 3.

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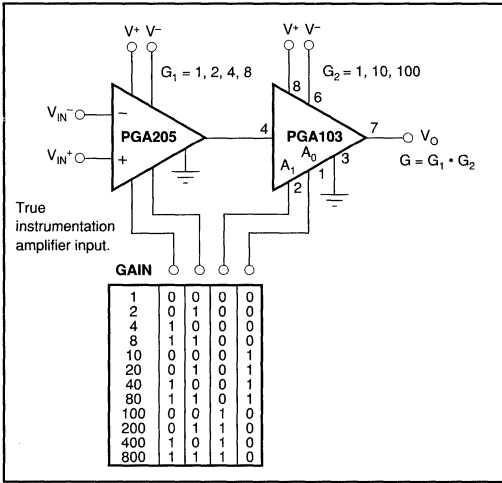


FIGURE 4. Programmable Gain Instrumentation Amplifier.

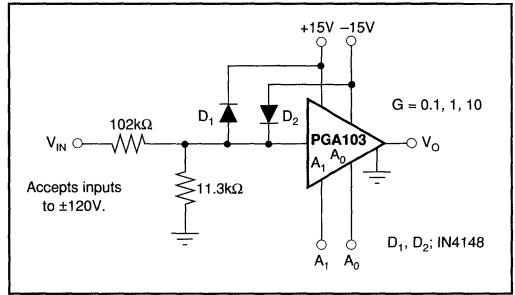


FIGURE 5. Wide Input Voltage Range Amplifier.

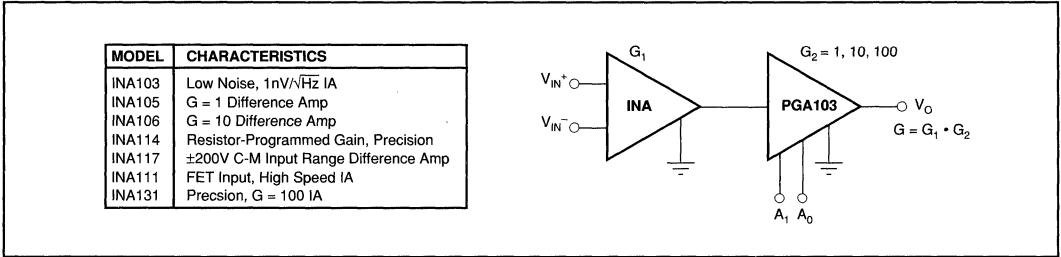
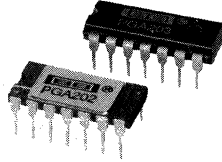


FIGURE 6. Instrumentation Amplifier with Programmable Gain Output Amp.

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PGA202/203

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

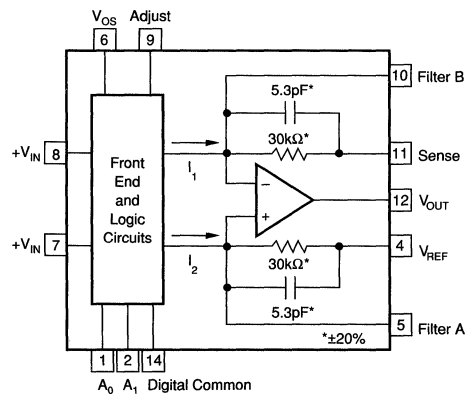
- DIGITALLY PROGRAMMABLE GAINS:
DECADE MODEL—PGA202
GAINS OF 1, 10, 100, 1000
BINARY MODEL—PGA203
GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2 μ s to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100 and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITION	PGA202/203AG ⁽¹⁾			PGA202/203BG ⁽¹⁾			PGA202/203KP ⁽¹⁾			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
GAIN Error ⁽²⁾	G < 1000		0.05	0.25		*	0.15		*	*	%	
	G = 1000		0.1	1		0.08	0.5		*	*	%	
	Nonlinearity	G < 1000		0.002	0.015		*	0.012		*	*	%
		G = 1000		0.02	0.06		*	0.04		*	*	%
Gain vs Temperature	G < 100		3	25		*	15		*	*	ppm/°C	
	G = 100		40	120		*	60		*	*	ppm/°C	
	G = 1000		100	300		*	150		*	*	ppm/°C	
RATED OUTPUT Voltage Over Specified Temperature Current Impedance	I _{OUT} ≤ 5mA See Typical Perf. Curve V _{OUT} ≤ 10V	±10	±12		*	*		*	*	*	V	
		±5	±9		*	*		*	±10	*	V	
			±10		*	*		*	*	*	mA	
			0.5		*	*		*	*	*	Ω	
ANALOG INPUTS Common-Mode Range Absolute Max Voltage ⁽³⁾ Impedance, Differential Common-Mode	No Damage	±10	±13		*	*		*	*	*	V	
				±V _{CC}		*	*		*	*	*	V
			10 3 10 1			*	*		*	*	*	GΩ pF GΩ pF
OFFSET VOLTAGE (RTI) Initial Offset at 25°C ⁽⁴⁾ vs Temperature Offset vs Time Offset vs Supply	10 ≤ V _{CC} ≤ 15		±(0.5 + 5/G)	±(2 + 24/G)		*	±(1 + 12/G)		*	*	mV	
			±(3 + 50/G)	±(24 + 240/G)		*	±(12 + 120/G)		*	*	μV/°C	
			50			*	*			*	*	μV/Month
			10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	*	μV/V
INPUT BIAS CURRENT Initial Bias Current: at 25°C at 85°C Initial Offset Current: at 25°C at 85°C			10 640 5 320	50 3200 25 1600		*	*		*	*	pA pA pA pA	
	COMMON MODE REJECTION RATIO	G = 1	80	100		*	*		*	*	*	dB
		G = 10	86	110		*	*		*	*	*	dB
		G = 100	92	120		*	*		*	*	*	dB
	G = 1000	94	120		*	*		*	*	*	dB	
INPUT NOISE Noise Voltage 0.1 to 10Hz Noise Density at 10kHz ⁽⁵⁾			1.7 12			*			*	*	μVp-p nV/√Hz	
	OUTPUT NOISE Noise Voltage 0.1 to 10Hz Density at 1kHz ⁽⁶⁾		32 400			*			*	*	μVp-p nV/√Hz	
DYNAMIC RESPONSE Frequency Response Full Power Bandwidth Slew Rate Settling Time (0.01%) ⁽⁷⁾ Overload Recovery Time ⁽⁷⁾		G < 1000		1000			*			*	*	kHz
	G = 1000		250			*			*	*	kHz	
	Full Power Bandwidth	G < 1000		400			*			*	*	kHz
		G = 1000		100			*			*	*	kHz
	Slew Rate		10	20	15		*	*	*	*	V/μs	
	Settling Time (0.01%) ⁽⁷⁾	G < 1000		2			*	*	*	*	*	μs
		G = 1000		10			*	*	*	*	*	μs
Overload Recovery Time ⁽⁷⁾	G < 1000		5			*	*	*	*	*	μs	
	G = 1000		10			*	*	*	*	*	μs	
DIGITAL INPUTS Digital Common Range Input Low Threshold ⁽⁶⁾ Input Low Current Input High Voltage Input High Current		-V _{CC}		V _{CC} - 8 0.8 10	*		*	*	*	*	V V μA V μA	
		2.4		10	*		*	*	*	*	V μA	
	POWER SUPPLY Rated Voltage Voltage Range Quiescent Current		±6	±15	±18	*	*	*	*	*	*	V V mA
				6.5			*	*	*	*	*	
							*	*	*	*	*	
TEMPERATURE RANGE Specification Operating Storage θ _{J-A}		-25		85	*		*	0		70	°C	
		-55		125	*		*	-25		85	°C	
		-65		150	*		*	-40		100	°C	
			100			*	*		*		°C/W	

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated.

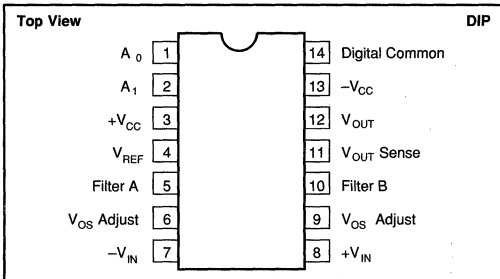
(2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) V_{NOISE (RTI)} = √(V_{N INPUT})² + (V_{N OUTPUT}/Gain)².

(6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.



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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	750mW
Analog and Digital Inputs	±(V _{CC} + 0.5V)
Operating Temperature Range:	
G Package	-55°C to +125°C
P Package	-40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PGA202KP	14-Pin Plastic DIP	010
PGA202AG	14-Pin Ceramic DIP	169
PGA202BG	14-Pin Ceramic DIP	169
PGA203KP	14-Pin Plastic DIP	010
PGA203AG	14-Pin Ceramic DIP	169
PGA203BG	14-Pin Ceramic DIP	169

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

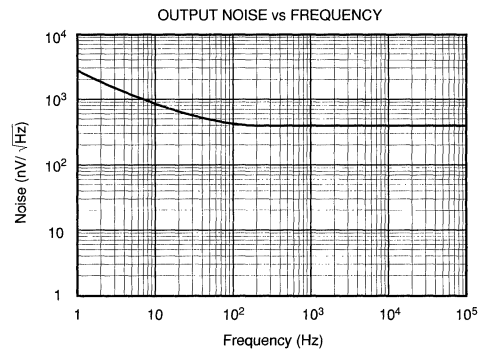
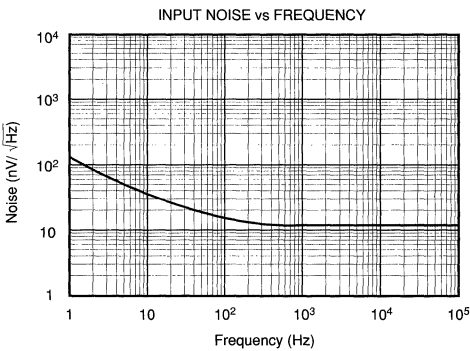
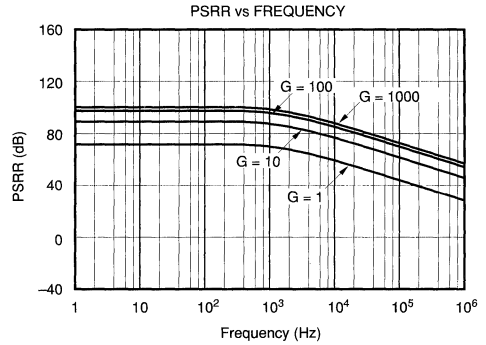
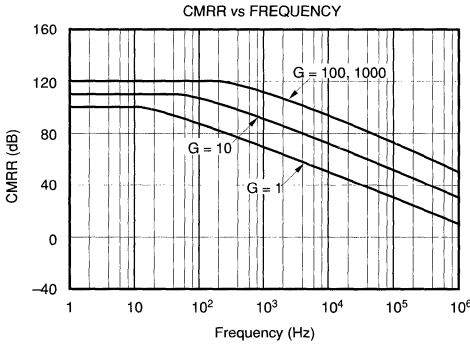
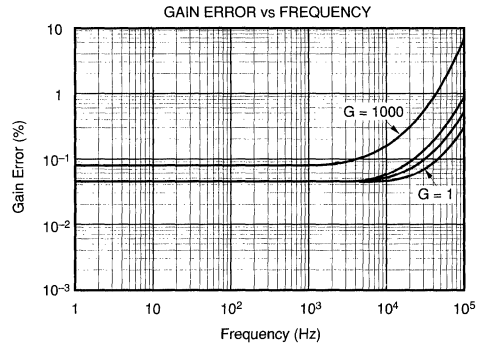
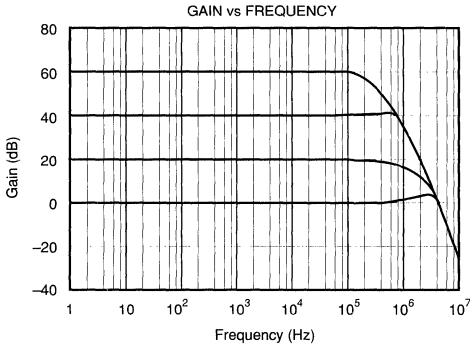
MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	-25°C to +85°C	±(2 + 24/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	-25°C to +85°C	±(1 + 12/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	-25°C to +85°C	±(2 + 24/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	-25°C to +85°C	±(1 + 12/G)

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

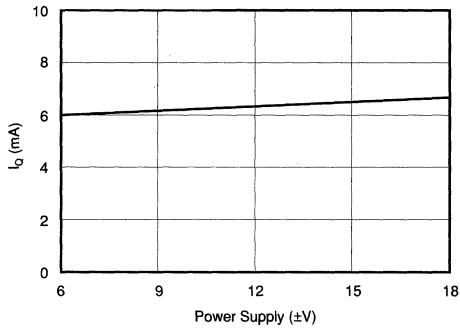


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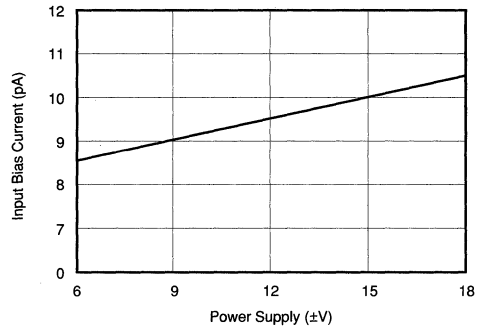
TYPICAL PERFORMANCE CURVES (CONT)

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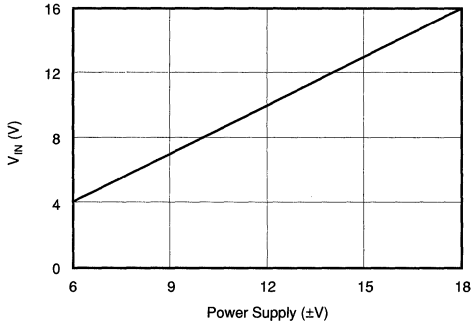
QUIESCENT CURRENT vs POWER SUPPLY



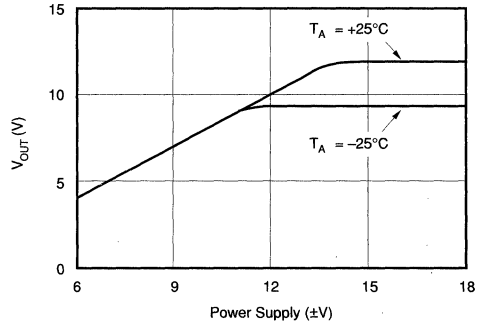
INPUT BIAS CURRENT vs POWER SUPPLY



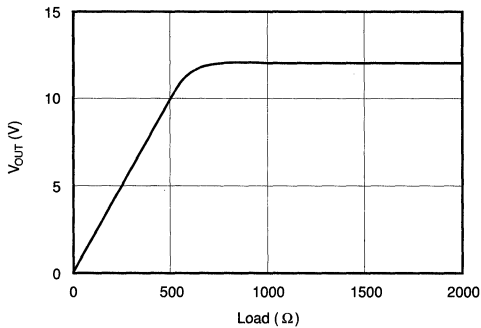
INPUT RANGE vs POWER SUPPLY



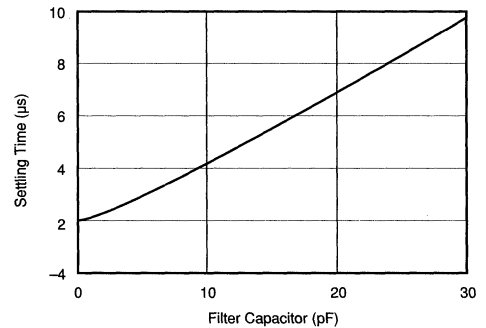
OUTPUT SWING vs POWER SUPPLY



OUTPUT SWING vs LOAD



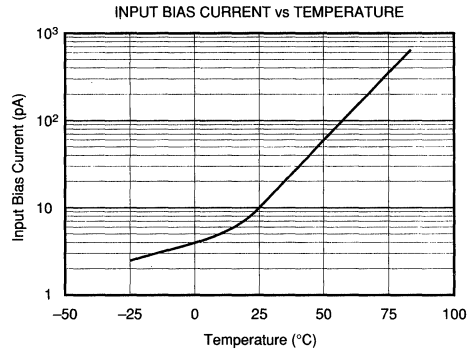
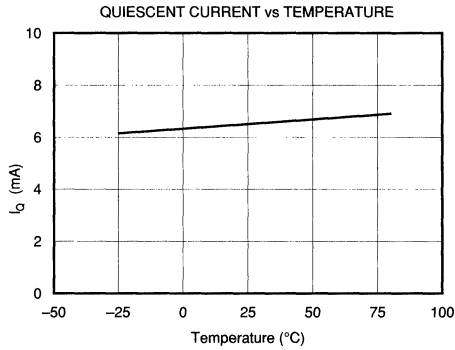
SETTLING TIME vs FILTER CAPACITOR



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TYPICAL PERFORMANCE CURVES (CONT)

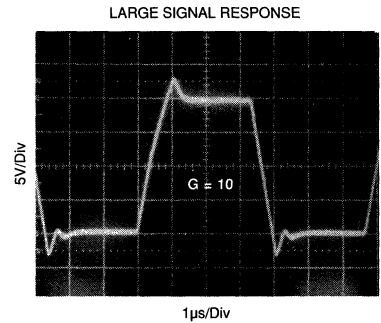
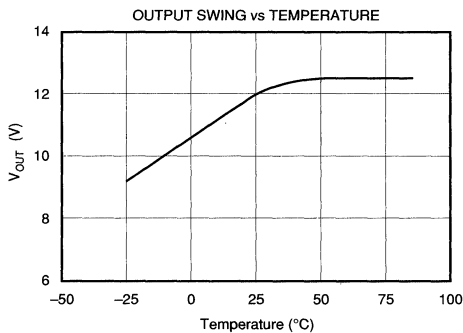
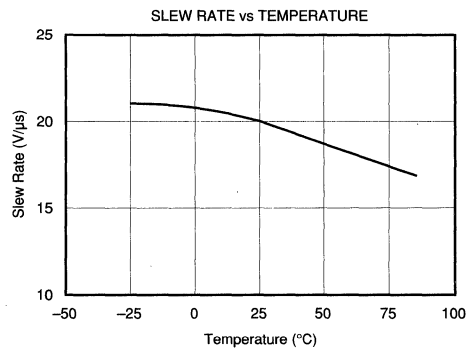
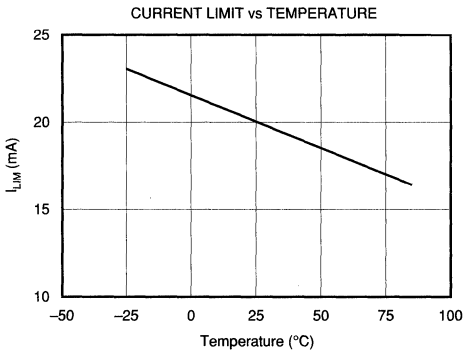
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



PGA202/203

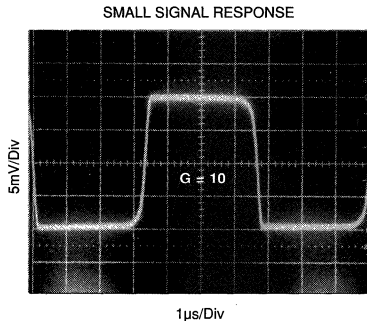
4

INSTRUMENTATION AMPLIFIERS



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise noted.



DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common mode rejection is not limited by the resistor matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with $1\mu\text{F}$ tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. Also to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

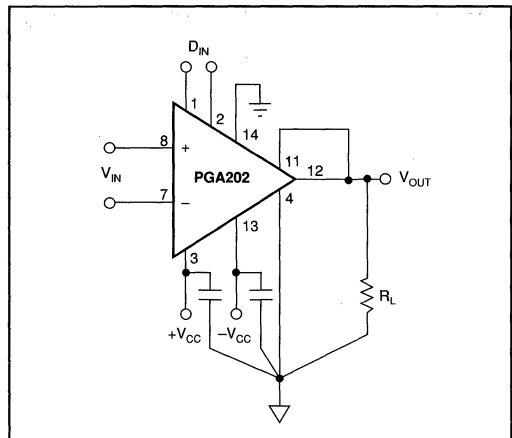


FIGURE 1. Basic Circuit Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op amp is very important. The op amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

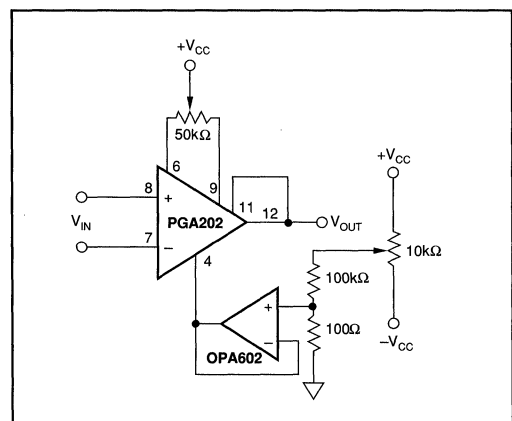


FIGURE 2. Offset Adjustment Circuits.

GAIN SELECTION

Gain selection is accomplished by the application of a 2-bit digital word to the gain select inputs. Table I shows the gains for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A ₁	A ₀	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R ₁	R ₂
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

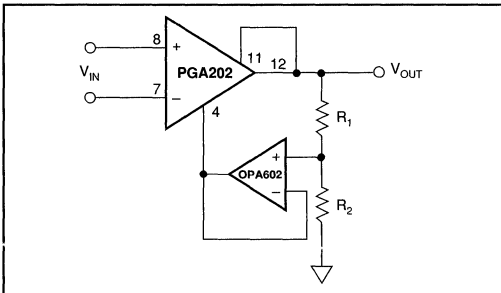


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

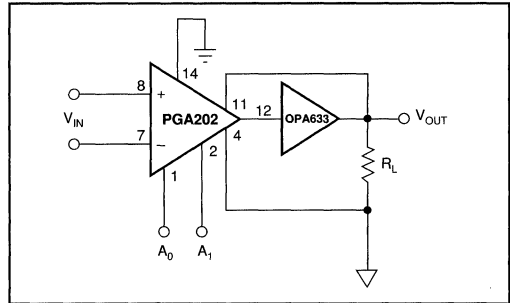


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table III.

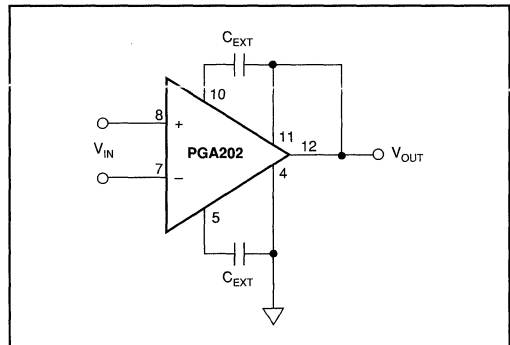


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C ₁ AND C ₂
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE III. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise the amplifier could wander and saturate. A $1\text{M}\Omega$ to $10\text{M}\Omega$ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9.)

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 12.

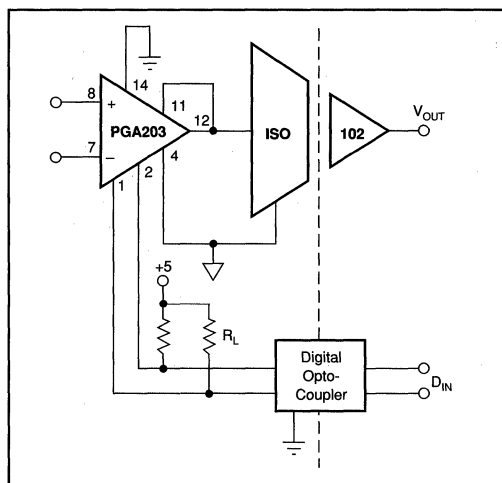


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

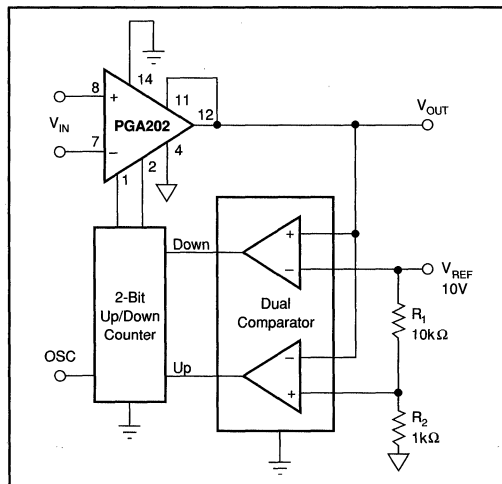


FIGURE 7. Auto Gain Ranging.

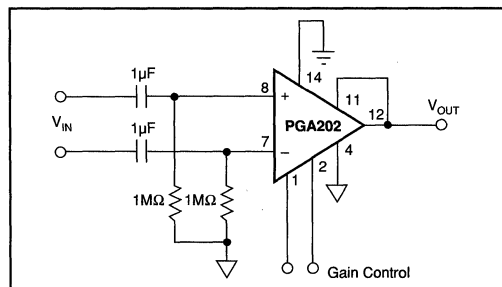


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies above 0.16Hz.

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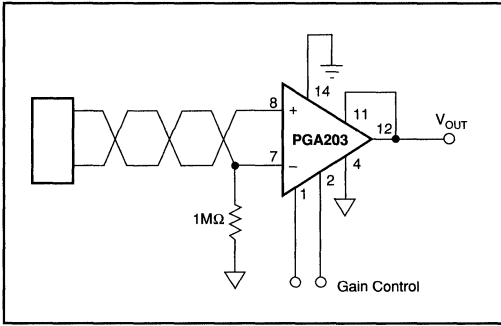


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

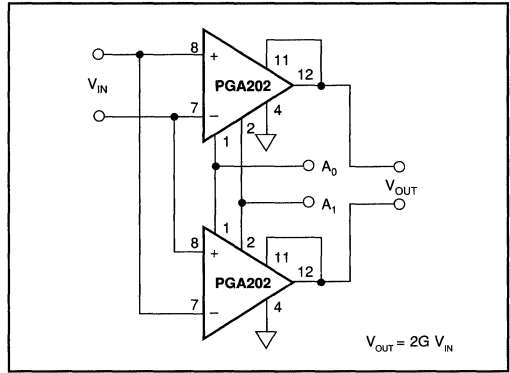


FIGURE 11. Programmable Differential In/Differential Out Amplifier.

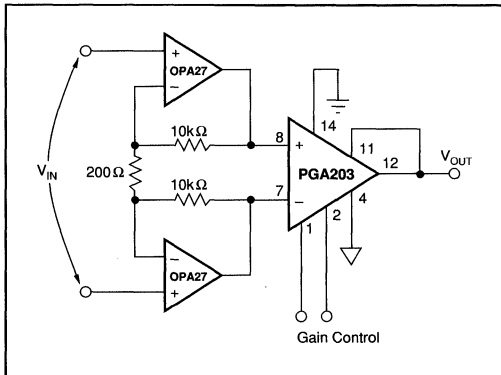


FIGURE 10. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.

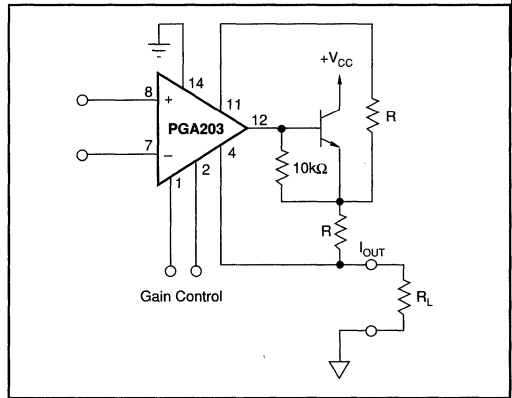


FIGURE 12. Programmable Current Source.

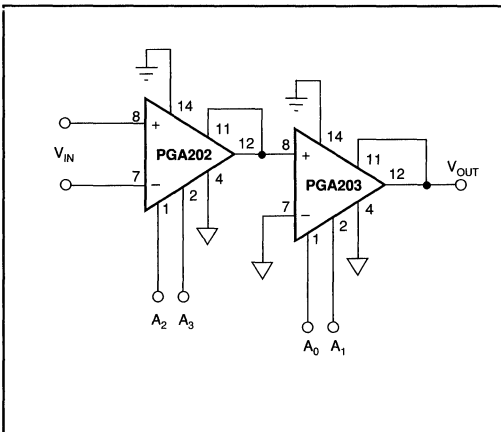
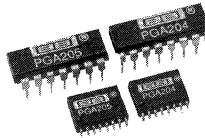


FIGURE 13. Cascaded Amplifiers.

A ₃	A ₂	A ₁	A ₀	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

For Immediate Assistance, Contact Your Local Salesperson



PGA204
PGA205

Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN:**
PGA204: $G=1, 10, 100, 1000V/V$
PGA205: $G=1, 2, 4, 8V/V$
- **LOW OFFSET VOLTAGE:** $50\mu V$ max
- **LOW OFFSET VOLTAGE DRIFT:** $0.25\mu V/^{\circ}C$
- **LOW INPUT BIAS CURRENT:** $2nA$ max
- **LOW QUIESCENT CURRENT:** $5.2mA$ typ
- **NO LOGIC SUPPLY REQUIRED**
- **16-PIN PLASTIC DIP, SOL-16 PACKAGES**

APPLICATIONS

- **DATA ACQUISITION SYSTEM**
- **GENERAL PURPOSE ANALOG BOARDS**
- **MEDICAL INSTRUMENTATION**

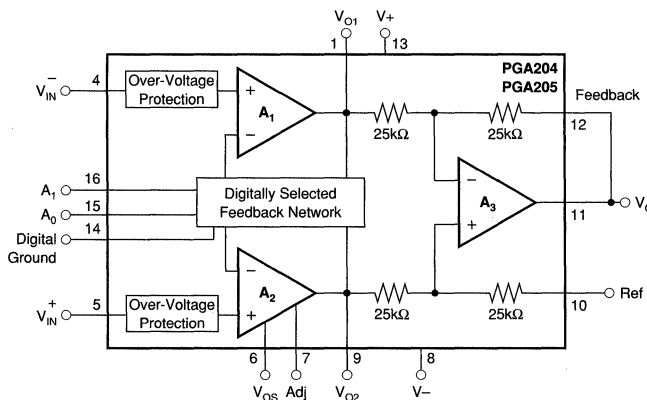
DESCRIPTION

The PGA204 and PGA205 are low cost, general purpose programmable-gain instrumentation amplifiers offering excellent accuracy. Gains are digitally selected: PGA204—1, 10, 100, 1000, and PGA205—1, 2, 4, 8V/V. The precision and versatility, and low cost of the PGA204 and PGA205 make them ideal for a wide range of applications.

Gain is selected by two TTL or CMOS-compatible address lines, A_0 and A_1 . Internal input protection can withstand up to $\pm 40V$ on the analog inputs without damage.

The PGA204 and PGA205 are laser trimmed for very low offset voltage ($50\mu V$), drift ($0.25\mu V/^{\circ}C$) and high common-mode rejection (115dB at $G=1000$). They operate with power supplies as low as $\pm 4.5V$, allowing use in battery operated systems. Quiescent current is 5mA.

The PGA204 and PGA205 are available in 16-pin plastic DIP, and SOL-16 surface-mount packages, specified for the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

PGA204 G=1, 10, 100, 1000V/V

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	PGA204BP, BU			PGA204AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI vs Temperature	$T_A = +25^\circ\text{C}$		$\pm 10 + 20/\text{G}$	$\pm 50 + 100/\text{G}$		$\pm 25 + 30/\text{G}$	$\pm 125 + 500/\text{G}$	μV
vs Power Supply	$T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		$\pm 0.1 + 0.5/\text{G}$	$\pm 0.25 + 5/\text{G}$		$\pm 0.25 + 5/\text{G}$	$\pm 1 + 10/\text{G}$	$\mu\text{V}/^\circ\text{C}$
Long-Term Stability			0.5+2/G	3+10/G		*	*	$\mu\text{V}/\text{V}$
Impedance, Differential			$\pm 0.2 + 0.5/\text{G}$			*	*	$\mu\text{V}/\text{mo}$
Common-Mode			$10^{\%}/6$			*	*	$\Omega \parallel \text{pF}$
Input Common-Mode Range	$V_{\text{CM}} = 0\text{V}$ (see text)	± 10.5	± 12.7	± 40	*	*	*	$\Omega \parallel \text{pF}$
Safe Input Voltage								V
Common-Mode Rejection	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$							V
	G=1	80	99		75	90		dB
	G=10	96	114		90	106		dB
	G=100	110	123		106	110		dB
	G=1000	115	123		106	110		dB
BIAS CURRENT								
vs Temperature			± 0.5	± 2		*	± 5	nA
Offset Current			± 8			*		$\text{pA}/^\circ\text{C}$
vs Temperature			± 0.5	± 2		*	*	nA
			± 8			*		$\text{pA}/^\circ\text{C}$
NOISE , Voltage, RTI ⁽¹⁾ : f=10Hz f=100Hz f=1kHz f _b =0.1Hz to 10Hz	G \geq 100, R _S =0 Ω G \geq 100, R _S =0 Ω G \geq 100, R _S =0 Ω G \geq 100, R _S =0 Ω		16 13 13 0.4			*		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$
Noise Current f=10Hz f=1kHz f _b =0.1Hz to 10Hz			0.4 0.2 18			*		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ pAp-p
GAIN , Error	G=1 G=10 G=100 G=1000 G=1 to 1000		± 0.005 ± 0.01 ± 0.01 ± 0.02 ± 2.5	± 0.024 ± 0.024 ± 0.024 ± 0.05 ± 10		*	± 0.05 ± 0.05 ± 0.05 ± 0.1 *	% % % % ppm/ $^\circ\text{C}$
Gain vs Temperature			± 0.0004	± 0.001		*	± 0.002	% of FSR
Nonlinearity	G=1 G=10 G=100 G=1000		± 0.0004 ± 0.0004 ± 0.0004 ± 0.0008	± 0.002 ± 0.002 ± 0.002 ± 0.01		*	± 0.004 ± 0.004 ± 0.004 ± 0.02	% of FSR % of FSR % of FSR % of FSR
OUTPUT								
Voltage, Positive ⁽²⁾ Negative ⁽²⁾	$I_{\text{O}} = 5\text{mA}$, T_{MIN} to T_{MAX} $I_{\text{O}} = -5\text{mA}$, T_{MIN} to T_{MAX}	(V+)-1.5 (V-)+1.5	(V+)-1.3 (V-)+1.3		*	*		V V
Load Capacitance Stability			1000		*	*		pF
Short Circuit Current			+23/-17		*	*		mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	G=1 G=10 G=100 G=1000		1 60 10 1			*		MHz kHz kHz kHz
Slew Rate	$V_{\text{O}} = \pm 10\text{V}$, G=10	0.3	0.7		*	*		V/ μs
Settling Time ⁽³⁾ , 0.1%	G=1 G=10 G=100 G=1000		22 23 100 1000			*		μs μs μs μs
0.01%	G=1 G=10 G=100 G=1000		23 28 140 1300			*		μs μs μs μs
Overload Recovery	50% Overdrive		70			*		μs
DIGITAL LOGIC								
Digital Ground Voltage, V _{DD}		V-		(V+)-4	*	*	*	V
Digital Low Voltage		V-		V _{DD} +0.8V	*	*	*	V
Digital Input Current			1		*	*	*	μA
Digital High Voltage		V _{DD} +2		V+	*	*	*	V
POWER SUPPLY , Voltage								
Current	V _{IN} =0V	± 4.5	± 15 $+5.2/-4.2$	± 18 ± 6.5	*	*	*	V mA
TEMPERATURE RANGE								
Specification		-40		+85	*	*	*	$^\circ\text{C}$
Operating		-40		+125	*	*	*	$^\circ\text{C}$
θ_{JA}			80			*		$^\circ\text{C}/\text{W}$

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for $\pm 10\text{V}$ min on $\pm 11.4\text{V}$ power supplies. (3) Includes time to switch to a new gain.



For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

PGA205 G=1, 2, 4, 8V/V

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	PGA205BP, BU			PGA205AP, AU			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT Offset Voltage, RTI vs Temperature vs Power Supply Long-Term Stability Impedance, Differential Common-Mode Input Common-Mode Range Safe Input Voltage Common-Mode Rejection	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$ $V_{\text{CM}} = 0\text{V}$ (see text) $V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$ G=1 G=2 G=4 G=8		$\pm 10 + 20/\text{G}$ $\pm 0.1 + 0.5/\text{G}$ $0.5 + 2/\text{G}$ $\pm 0.2 - 0.5/\text{G}$ $10^{10} 6$ $10^{10} 6$	$\pm 50 + 100/\text{G}$ $\pm 0.25 + 5/\text{G}$ $3 + 10/\text{G}$		$\pm 25 + 30/\text{G}$ $\pm 0.25 + 5/\text{G}$ * * * *	$\pm 125 + 500/\text{G}$ $\pm 1 + 10/\text{G}$ * * * *	μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{mo}$ ΩpF ΩpF V V	
		± 10.5		± 12.7					
				80	94		75	88	dB
				85	100		80	94	dB
				90	106		85	100	dB
				95	112		89	106	dB
BIAS CURRENT vs Temperature Offset Current vs Temperature			± 0.5 ± 8	± 2			± 5	nA pA/ $^\circ\text{C}$ nA pA/ $^\circ\text{C}$	
			± 0.5 ± 8	± 2			*		
Noise Voltage, RTI ⁽¹⁾ : f=10Hz f=100Hz f=1kHz f _p =0.1Hz to 10Hz Noise Current f=10Hz f=1kHz f _p =0.1Hz to 10Hz	G=8, R _S =0Ω		19					nV/ $\sqrt{\text{Hz}}$	
	G=8, R _S =0Ω		15					nV/ $\sqrt{\text{Hz}}$	
	G=8, R _S =0Ω		15					nV/ $\sqrt{\text{Hz}}$	
	G=8, R _S =0Ω		0.5					$\mu\text{Vp-p}$	
			0.4					pA/ $\sqrt{\text{Hz}}$	
			0.2					pA/ $\sqrt{\text{Hz}}$	
			18					pAp-p	
GAIN, Error Gain vs Temperature Nonlinearity	G=1		± 0.005	± 0.024		*	± 0.05	%	
	G=2		± 0.01	± 0.024		*	± 0.05	%	
	G=4		± 0.01	± 0.024		*	± 0.05	%	
	G=8		± 0.01	± 0.024		*	± 0.05	%	
	G=1 to 8		± 2.5	± 10		*	*	ppm/ $^\circ\text{C}$	
	G=1		± 0.00024	± 0.001		*	± 0.002	% of FSR	
	G=2		± 0.00024	± 0.002		*	± 0.004	% of FSR	
	G=4		± 0.00024	± 0.002		*	± 0.004	% of FSR	
G=8		± 0.00024	± 0.002		*	± 0.004	% of FSR		
OUTPUT Voltage, Positive ⁽²⁾ Negative ⁽²⁾ Load Capacitance Stability Short Circuit Current	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX}	$(V+) - 1.5$	$(V+) - 1.3$		*	*		V	
	$I_O = -5\text{mA}$, T_{MIN} to T_{MAX}	$(V-) + 1.5$	$(V-) + 1.3$		*	*		V	
			1000			*		pF	
				$+23/-17$		*		mA	
FREQUENCY RESPONSE Bandwidth, -3dB Slew Rate Settling Time ⁽³⁾ , 0.1% 0.01% Overload Recovery	G=1		1			*		MHz	
	G=2		400			*		kHz	
	G=4		200			*		kHz	
	G=8		100			*		kHz	
	$V_O = \pm 10\text{V}$, G=8	0.3	0.7		*	*	*	V/ μs	
	G=1		22			*		μs	
	G=2		22			*		μs	
	G=4		23			*		μs	
	G=8		23			*		μs	
	G=1		23			*		μs	
	G=2		23			*		μs	
	G=4		25			*		μs	
	G=8		28			*		μs	
50% overdrive		70			*		μs		
DIGITAL LOGIC INPUTS Digital Ground Voltage, V_{DG} Digital Low Voltage Digital Low Current Digital High Voltage		V-		$(V+) - 4$	*		*	V	
		V-		$V_{\text{DG}} + 0.8\text{V}$	*		*	V	
			1	V_+	*	*	*	μA	
		$V_{\text{DG}} + 2$			*		*	V	
POWER SUPPLY, Voltage Current		± 4.5	± 15	± 18	*	*	*	V	
	$V_{\text{IN}} = 0\text{V}$		$+5.2/-4.2$	± 6.5			± 7.5	mA	
TEMPERATURE RANGE Specification Operating θ_{JA}		-40		+85	*		*	$^\circ\text{C}$	
		-40		+125	*		*	$^\circ\text{C}$	
			80			*	*	$^\circ\text{C}/\text{W}$	

* Specification same as PGA204BP.

NOTES: (1) Input-referred noise voltage varies with gain. See typical curves. (2) Output voltage swing is tested for $\pm 10\text{V}$ min on $\pm 11.4\text{V}$ power supplies. (3) Includes time to switch to a new gain.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PGA204AP	16-Pin Plastic DIP	180
PGA204BP	16-Pin Plastic DIP	180
PGA204AU	SOL-16 Surface Mount	211
PGA204BU	SOL-16 Surface Mount	211
PGA205AP	16-Pin Plastic DIP	180
PGA205BP	16-Pin Plastic DIP	180
PGA205AU	SOL-16 Surface Mount	211
PGA205BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Logic Input Voltage Range	±V _S
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering -10s)	+300°C

ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE
PGA204AP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204BP	1, 10, 100, 1000V/V	16-Pin Plastic DIP	-40 to +85°C
PGA204AU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA204BU	1, 10, 100, 1000V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205AP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205BP	1, 2, 4, 8V/V	16-Pin Plastic DIP	-40 to +85°C
PGA205AU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C
PGA205BU	1, 2, 4, 8V/V	SOL-16 Surface-Mount	-40 to +85°C

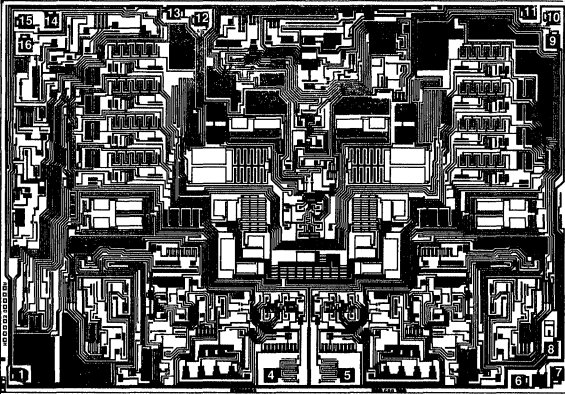
PGA204/205

4

INSTRUMENTATION AMPLIFIERS

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DICE INFORMATION



PGA204/205 DIE TOPOGRAPHY

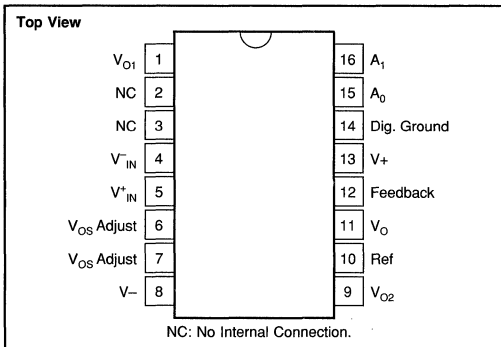
PAD	FUNCTION	PAD	FUNCTION
1	V_{O1}	9	V_{O2}
2	—	10	Ref
3	—	11	V_O
4	V_{IN}^-	12	Feedback
5	V_{IN}^+	13	V_+
6	$V_{OS} \text{ Adj}$	14	Dig. Ground
7	$V_{OS} \text{ Adj}$	15	A_0
8	V_-	16	A_1

Substrate Bias: Internally connected to V_- power supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	186 x 130 ±5	4.72 x 3.30 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

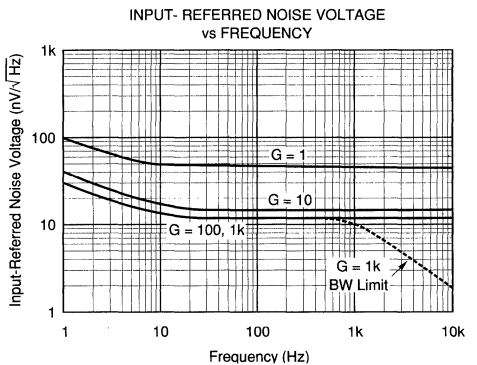
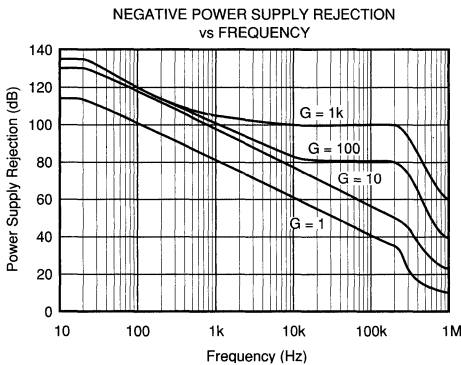
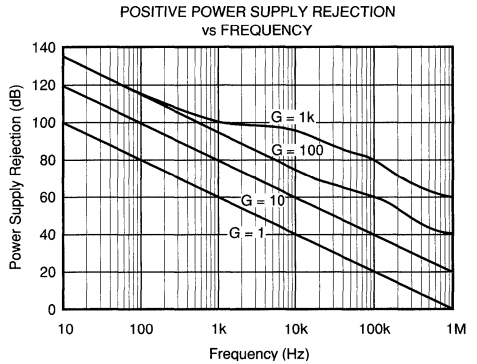
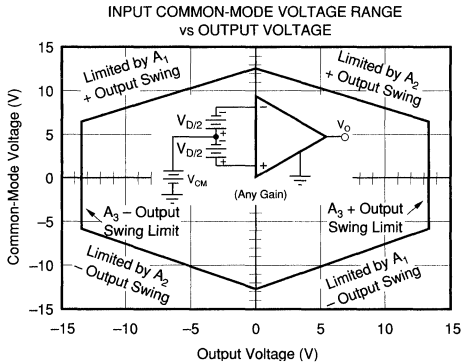
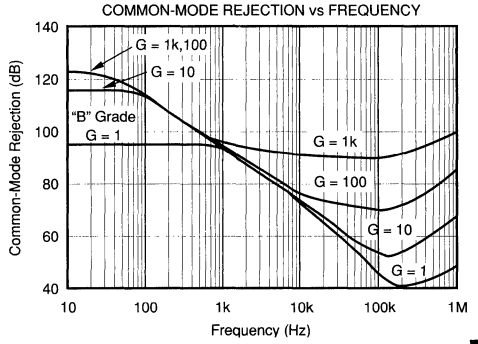
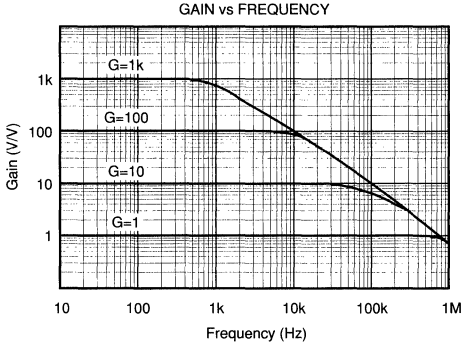
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



PGA204/205

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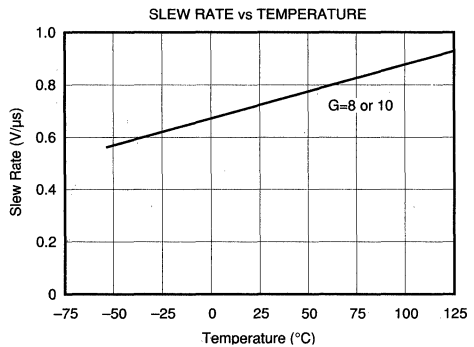
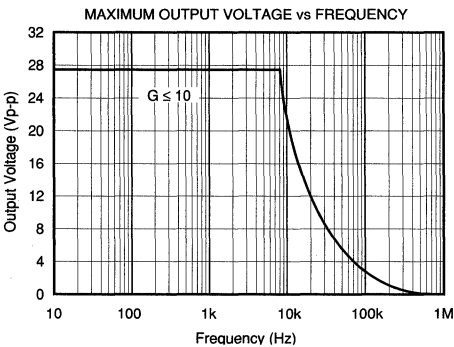
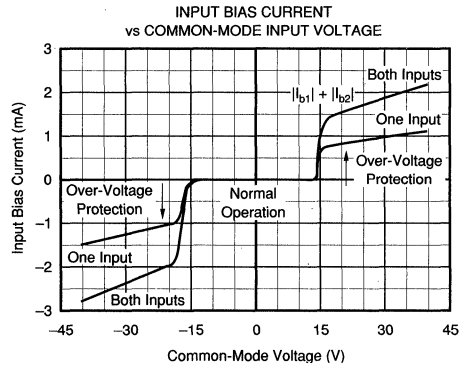
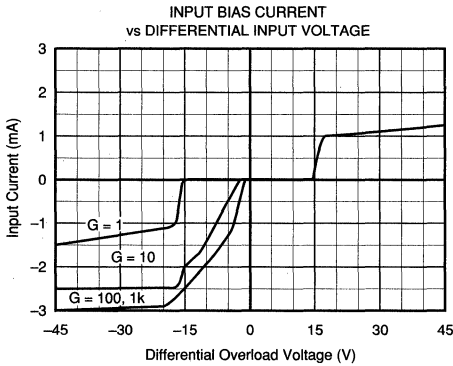
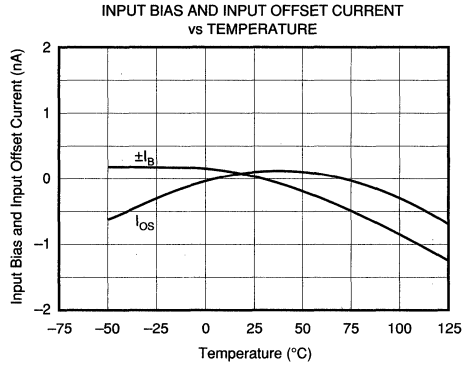
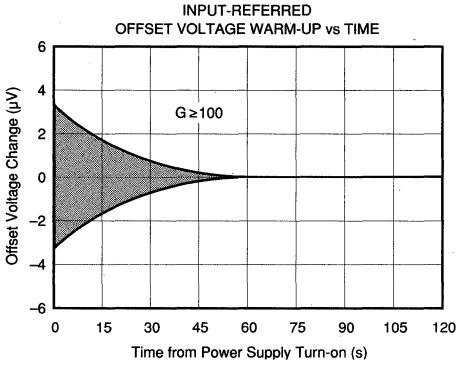
INSTRUMENTATION AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

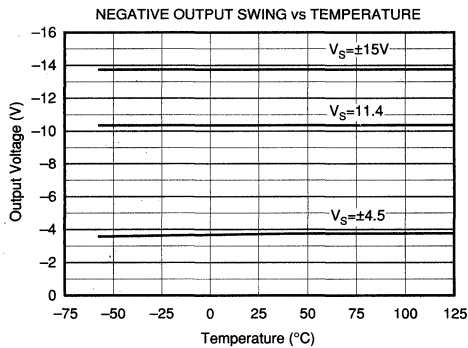
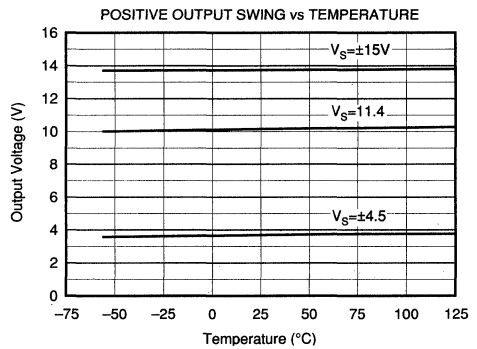
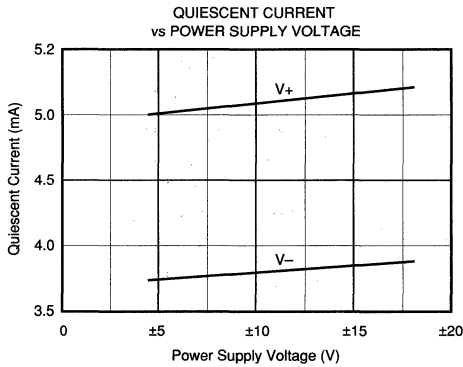
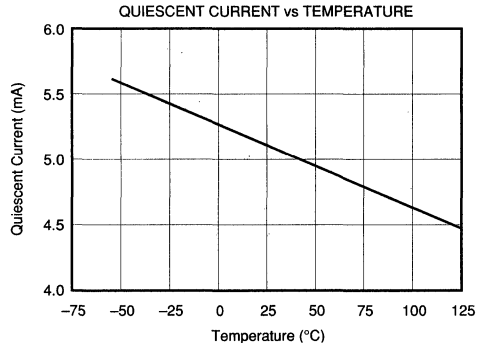
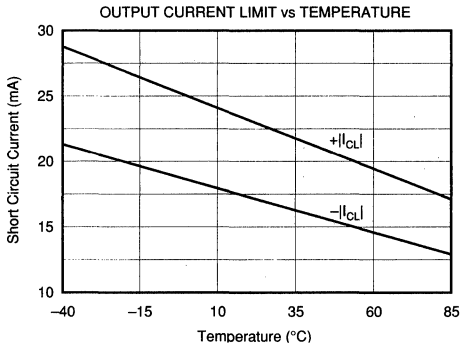
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

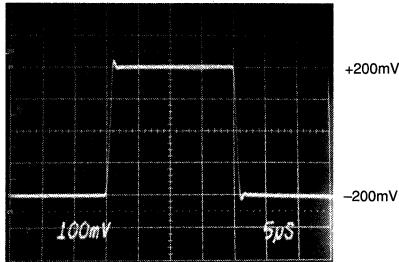


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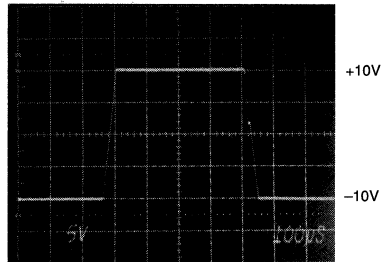
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

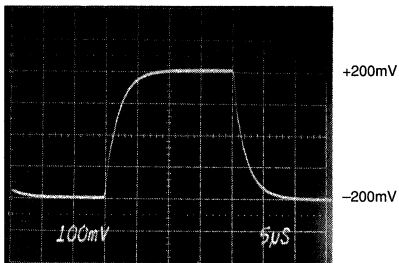
SMALL-SIGNAL RESPONSE, $G = 1$



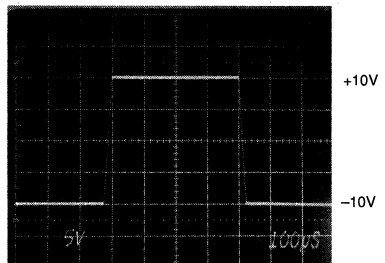
LARGE-SIGNAL RESPONSE, $G = 1$



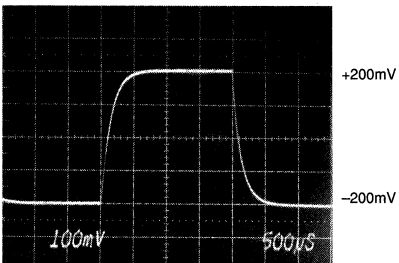
SMALL-SIGNAL RESPONSE, $G = 10$



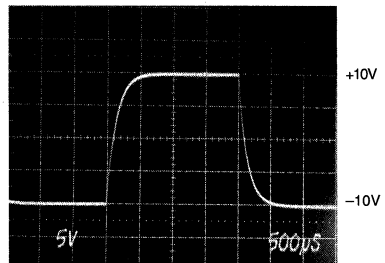
LARGE-SIGNAL RESPONSE, $G = 10$



SMALL-SIGNAL RESPONSE, $G = 1000$



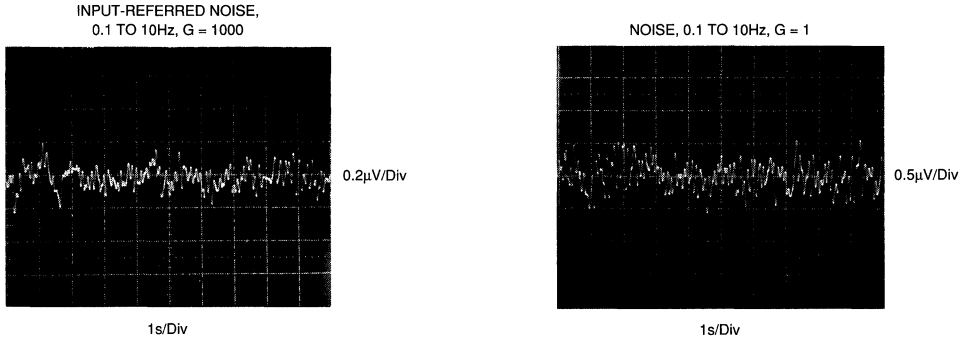
LARGE-SIGNAL RESPONSE, $G = 1000$



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA204/205. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ($G=1$).

The PGA204/205 has an output feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. The output Feedback connection can

be used to sense the output voltage directly at the load for best accuracy.

DIGITAL INPUTS

The digital inputs A_0 and A_1 select the gain according to the logic table in Figure 1. Logic "1" is defined as a voltage greater than 2V above digital ground potential (pin 14). Digital ground can be connected to any potential from the V_- power supply to 4V less than V_+ . Digital ground is normally connected to ground. The digital inputs interface directly CMOS and TTL logic components.

Approximately $1\mu\text{A}$ flows out of the digital input pins when a logic "0" is applied. Logic input current is nearly zero with

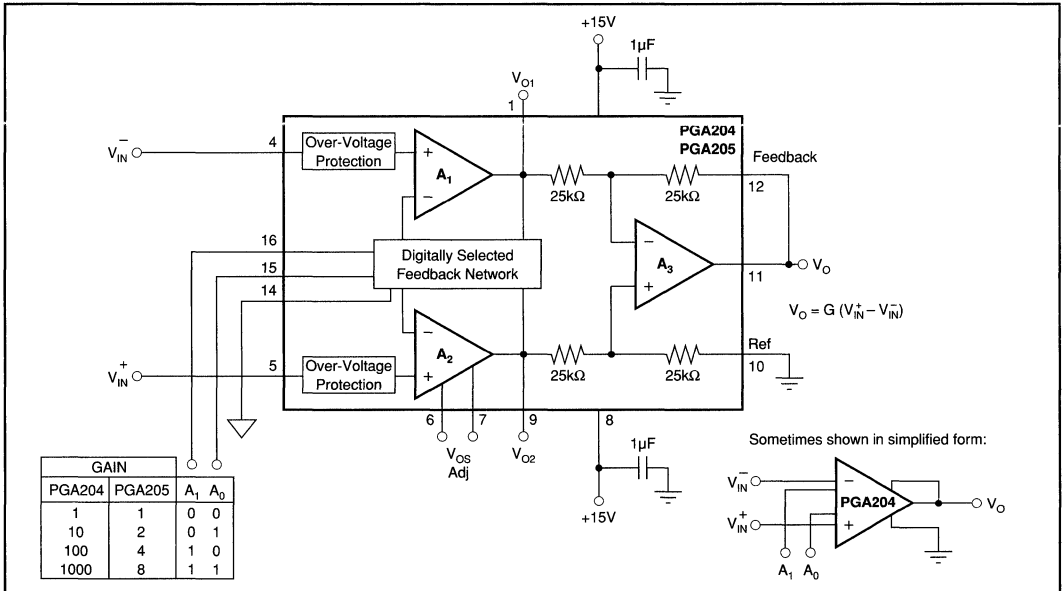


FIGURE 1. Basic Connections.

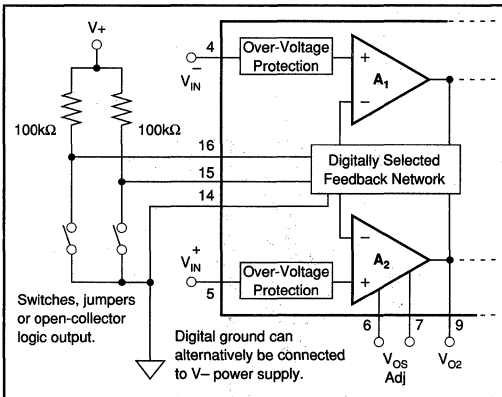


FIGURE 2. Switch or Jumper-Selected Digital Inputs.

a logic "1" input. A constant current of approximately 1.3mA flows in the digital ground pin. It is good practice to return digital ground through a separate connection path so that analog ground is not affected by the digital ground current.

The digital inputs, A_0 and A_1 , are not latched; a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 1 μ s. The time to respond to gain change is effectively the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control data from a high speed data bus (see Figure 7). Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry.

Some applications select gain of the PGA204/205 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch, jumper or open-collector logic is open or off. Fixed-gain applications can connect the logic inputs directly to V_+ or V_- (or other valid logic level); no resistor is required.

OFFSET VOLTAGE

Voltage offset of the PGA204/205 consists of two components—input stage offset and output stage offset. Both components are specified in the specification table in equation form:

$$V_{OS} = V_{OSI} + V_{OSO} / G \quad (1)$$

where:

V_{OS} total is the combined offset, referred to the input.

V_{OSI} is the offset voltage of the input stage, A_1 and A_2 .

V_{OSO} is the offset voltage of the output difference amplifier, A_3 .

V_{OSI} and V_{OSO} do not change with gain. The composite offset voltage V_{OS} changes with gain because of the gain term in equation 1. Input stage offset dominates in high gain ($G \geq 100$); both sources of offset may contribute at low gain ($G=1$ to 10).

OFFSET TRIMMING

Both the input and output stages are laser trimmed for very low offset voltage and drift. Many applications require no external offset adjustment.

Figure 3 shows an optional input offset voltage trim circuit. This circuit should be used to adjust only the input stage offset voltage of the PGA204/205. Do this by programming

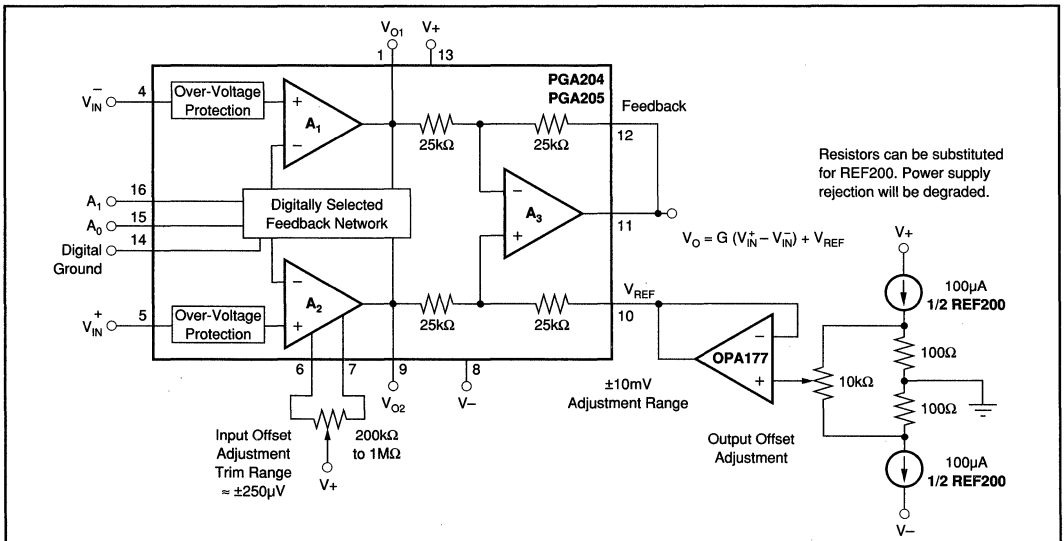


FIGURE 3. Optional Offset Voltage Trim Circuit.

it to its highest gain and trimming the output voltage to zero with the inputs grounded. Drift performance usually improves slightly when the input offset is nulled with this procedure.

Do not use the input offset adjustment to trim system offset or offset produced by a sensor. Nulling offset that is not produced by the input amplifiers will increase temperature drift by approximately $3.3\mu\text{V}/^\circ\text{C}$ per 1mV of offset adjustment.

Many applications that need input stage offset adjustment do not need output stage offset adjustment. Figure 3 also shows a circuit for adjusting output offset voltage. First, adjust the input offset voltage as discussed above. Then program the device for $G=1$ and adjust the output to zero. Because of the interaction of these two adjustments at $G=8$, the PGA205 may require iterative adjustment.

The output offset adjustment can be used to trim sensor or system offsets without affecting drift. The voltage applied to the Ref terminal is summed with the output signal. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering the trim voltage with an op amp as shown.

NOISE PERFORMANCE

The PGA204/205 provides very low noise in most applications. Low frequency noise is approximately $0.4\mu\text{Vp-p}$ measured from 0.1 to 10Hz. This is approximately one-tenth the noise of “low noise” chopper-stabilized amplifiers.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the PGA204/205 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the PGA204/205 is to operate properly. Figure 4 shows provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the PGA204/205 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 4). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due bias current and better common-mode rejection.

Many sources or sensors inherently provide a path for input bias current (e.g. the bridge sensor shown in Figure 4). These applications do not require additional resistor(s) for proper operation.

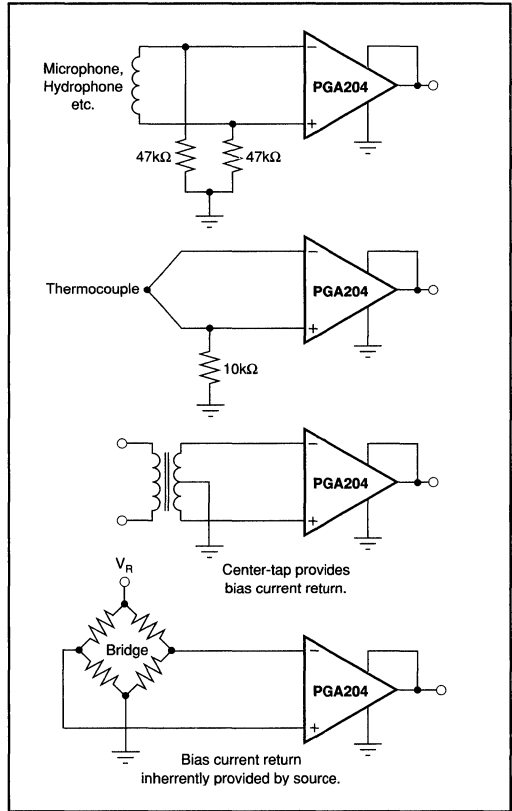


FIGURE 4. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the PGA204/205 is approximately $\pm 12.7\text{V}$ (or 2.3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The common-mode range is related to the output voltage of the complete amplifier—see performance curve “Input Common-Mode Range vs Output Voltage”.

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 5 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, A_3 . For applications where input common-mode range must be maximized, limit the output voltage swing by selecting a lower gain of the PGA204/205 (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the PGA204/205 to increase the voltage swing.

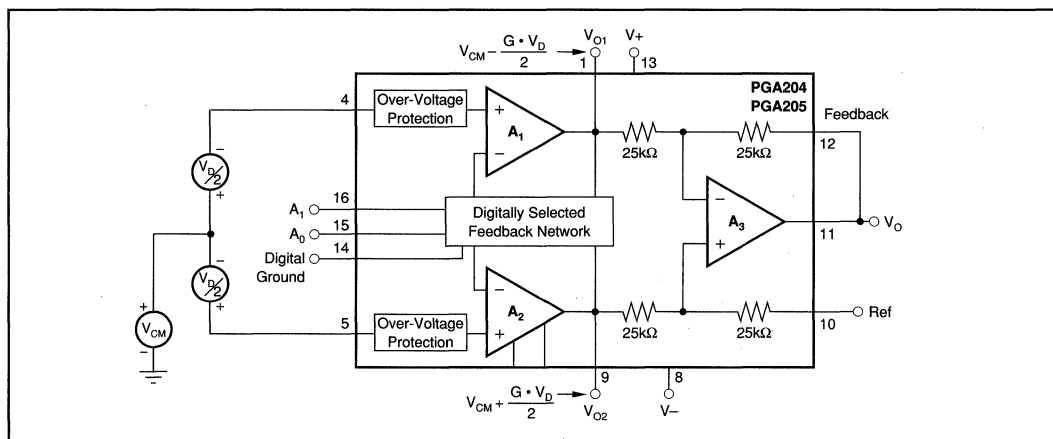


FIGURE 5. Voltage Swing of A_1 and A_2 .

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the PGA204/205 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the PGA204/205 are individually protected for voltages up to $\pm 40V$. For example, a condition of $-40V$ on one input and $+40V$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

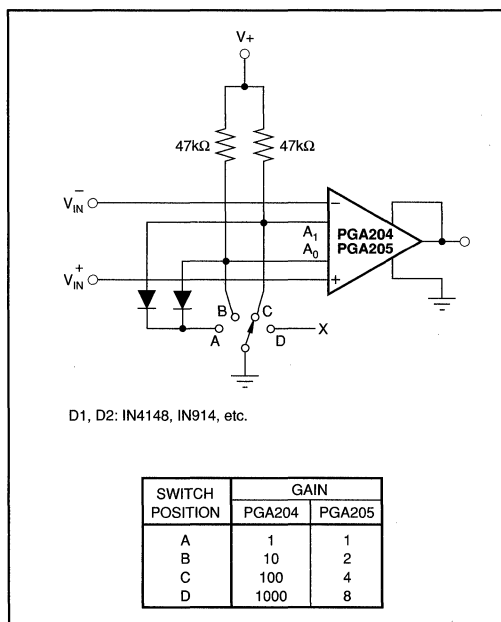


FIGURE 6. Switch-Selected PGIA.

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Or, Call Customer Service at 1-800-548-6132 (USA Only)

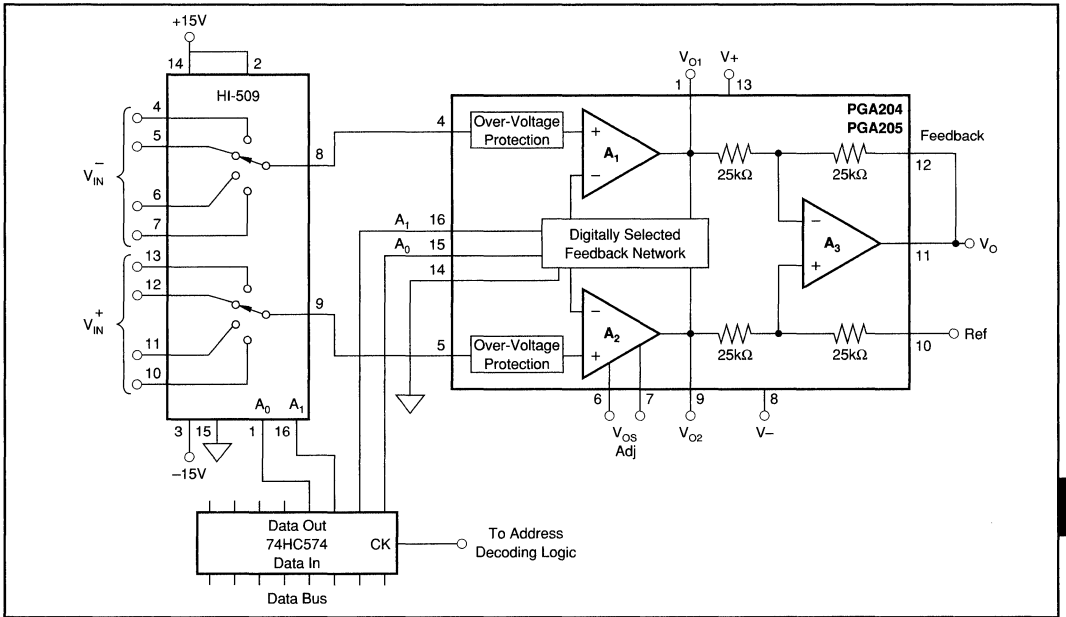


FIGURE 7. Multiplexed-Input Programmable Gain IA.

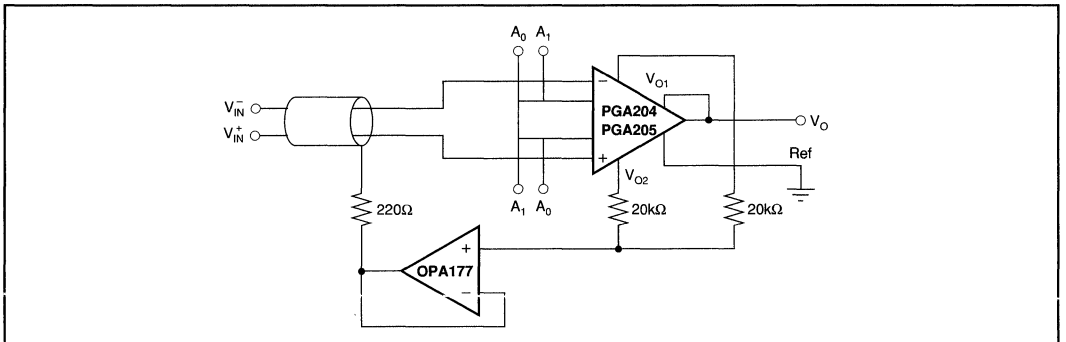


FIGURE 8. Shield Drive Circuit.

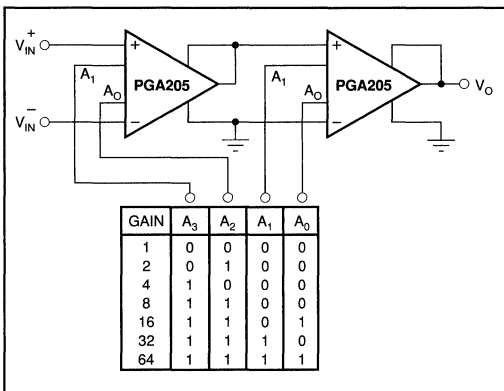


FIGURE 9. Binary Gain Steps, G=1 to G=64.

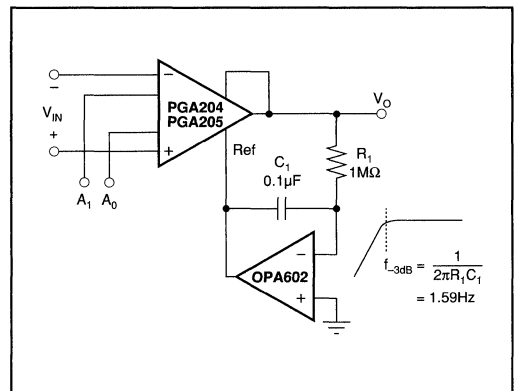
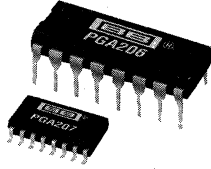


FIGURE 10. AC-Coupled PGIA.

For Immediate Assistance, Contact Your Local Salesperson



PGA206
PGA207

PRODUCT IN DEVELOPMENT
SUBJECT TO CHANGE
WITHOUT NOTICE

High-Speed Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAINS:**
PGA206: $G=1, 2, 4, 8V/V$
PGA207: $G=1, 2, 5, 10V/V$
- **TRUE INSTRUMENTATION AMP INPUT**
- **FAST SETTLING:** $3\mu s$ (0.01% ALL GAINS)
- **FET INPUT:** $I_b = 100pA$ (max)
- **INPUT OVER-VOLTAGE PROTECTION:** $\pm 40V$
- **LOW OFFSET VOLTAGE:** $250\mu V$ max
- **16-PIN DIP, SOL-16 SOIC PACKAGES**

APPLICATIONS

- **MULTIPLE-CHANNEL DATA ACQUISITION**
- **MEDICAL, PHYSIOLOGICAL AMPLIFIER**
- **PC-CONTROLLED ANALOG INPUT BOARDS**

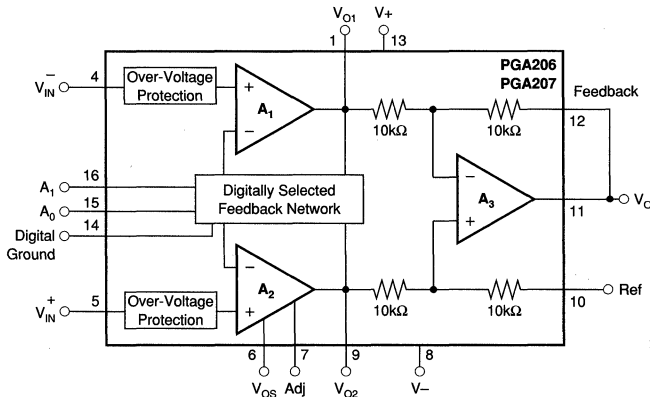
DESCRIPTION

The PGA206 and PGA207 are digitally programmable gain instrumentation amplifiers that are ideally suited for data acquisition systems.

The PGA206/207's fast settling time allows multiplexed input channels for excellent system efficiency. FET inputs eliminate I_b errors due to series resistance of common CMOS analog multiplexers.

Gains are selected by two CMOS/TTL-compatible address lines. Analog inputs are internally protected for overloads up to $\pm 40V$, even with the power supplies off. The PGA206/207 is laser-trimmed for low offset voltage and low drift.

The PGA206 and PGA207 are available in 16-pin plastic DIP and SOL-16 surface-mount packages. Both are specified for $-40^\circ C$ to $+85^\circ C$ operation.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$ unless otherwise noted.

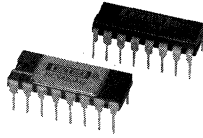
PARAMETER	CONDITIONS	PGA206P, U PGA207P, U			PGA206PA, UA PGA207PA, UA			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI								μV
Initial	$T_A = +25^\circ\text{C}$		$\pm 50 \pm 200/\text{G}$	$\pm 200 \pm 500/\text{G}$		$\pm 500 \pm 1000/\text{G}$	$\pm 200 \pm 900/\text{G}$	$\mu\text{V}/^\circ\text{C}$
vs Temperature	$T_A = T_{\text{MIN}}$ to T_{MAX}		$\pm 0.5 \pm 2/\text{G}$	$\pm 1 \pm 10/\text{G}$		$\pm 2 \pm 15/\text{G}$	$\pm 3 \pm 30/\text{G}$	$\mu\text{V}/\text{V}$
vs Power Supply	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$		$\pm 3 \pm 2/\text{G}$	$\pm 10 \pm 10/\text{G}$		*	$\pm 20 \pm 20/\text{G}$	$\mu\text{V}/\text{mV}$
Long-Term Stability			$\pm 1 \pm 20/\text{G}$			*		$\mu\text{V}/\text{mo}$
Impedance, Differential			$10^{12} \parallel 6$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{12} \parallel 6$			*		$\Omega \parallel \text{pF}$
Linear Input Voltage Range	$V_O = 0\text{V}$	$\pm(V_{\text{SI}} -4)$	$\pm(V_{\text{SI}} -3.5)$		*	*		V
Safe Input Voltage				± 40			*	V
Common-Mode Rejection	$V_{\text{CM}} = \pm 11\text{V}$, $\Delta R_S = 1\text{k}\Omega$							
	$G=1$	80	94		75	88		dB
	$G=2$	85	100		80	94		dB
	$G=4$ or 5	90	106		85	100		dB
	$G=8$ or 10	95	112		89	106		dB
BIAS CURRENT	$V_{\text{IN}} = 0$		10	100		10	100	pA
vs Temperature			Doubles Every 10°C			*	*	
Offset Current			10	100		10	200	pA
vs Temperature			Doubles Every 10°C			*	*	
NOISE VOLTAGE, RTI	$G=8, 10$; $R_S = 0\Omega$					*	*	$\text{nV}/\sqrt{\text{Hz}}$
$f = 10\text{Hz}$			18			*	*	$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			15			*	*	$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			12			*	*	$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to 10Hz			0.5			*	*	$\mu\text{Vp-p}$
Noise Current						*	*	$\text{fA}/\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			1.5			*	*	
GAIN	All Gains, $V_O = \pm 11\text{V}$, $R_L = 2\text{k}\Omega$							
Gain Error			± 0.01	± 0.024		*	± 0.05	%
Gain vs Temperature			± 2.0	± 10		*	*	$\text{ppm}/^\circ\text{C}$
Nonlinearity			± 0.0004	± 0.0025		*	± 0.005	% of FSR
OUTPUT								
Voltage, Positive	T_{MIN} to T_{MAX}		$(V_+) - 2.5$			*	*	V
Negative	T_{MIN} to T_{MAX}		$(V_-) + 2$			*	*	V
Load Capacitance Stability			1000			*	*	pF
Short-Circuit Current			± 15			*	*	mA
FREQUENCY RESPONSE								
Bandwidth, -3dB	$G=1$		3			*	*	MHz
	$G=2$		3			*	*	MHz
	$G=4, 5$		2.5			*	*	MHz
	$G=8, 10$		1.5			*	*	MHz
Slew Rate	$V_O = \pm 10\text{V}$, $G=1$ to 10		30			*	*	$\text{V}/\mu\text{s}$
Settling Time, 0.1%	20V Step, All Gains		2			*	*	μs
0.01%	20V Step, All Gains		3			*	*	μs
Output Overload Recovery	50% Overdrive		1.5			*	*	μs
DIGITAL LOGIC INPUTS								
Digital Ground Voltage, V_{DG}		V_-		$(V_+) - 4$	*	*	*	V
Digital Low Voltage		V_-		$V_{\text{DG}} + 0.8\text{V}$	*	*	*	V
Digital Input Current			1		*	*	*	μA
Digital High Voltage		$V_{\text{DG}} + 2$		V_+	*	*	*	V
Gain Switching Time			500		*	*	*	ns
POWER SUPPLY								
Voltage Range		± 4.5	± 15	± 18	*	*	*	V
Current	$V_{\text{IN}} = 0\text{V}$		$+11.6/-10.4$		*	*	*	mA
TEMPERATURE RANGE								
Specification		-40		+85	*	*	*	$^\circ\text{C}$
Operating		-40		+125	*	*	*	$^\circ\text{C}$
Thermal Resistance, θ_{JA}			80		*	*	*	$^\circ\text{C}/\text{W}$

* Specification same as PGA206P or PGA207P.

PGA206/207

4

INSTRUMENTATION AMPLIFIERS



RCV420

Precision 4mA to 20mA CURRENT LOOP RECEIVER

FEATURES

- COMPLETE 4-20mA TO 0-5V CONVERSION
- INTERNAL SENSE RESISTORS
- PRECISION 10V REFERENCE
- BUILT-IN LEVEL-SHIFTING
- $\pm 40V$ COMMON-MODE INPUT RANGE
- 0.1% OVERALL CONVERSION ACCURACY
- HIGH NOISE IMMUNITY: 86dB CMR

APPLICATIONS

- PROCESS CONTROL
- INDUSTRIAL CONTROL
- FACTORY AUTOMATION
- DATA ACQUISITION
- SCADA
- RTUs
- ESD
- MACHINE MONITORING

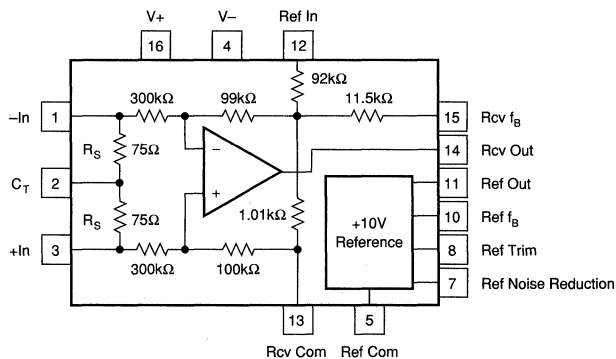
DESCRIPTION

The RCV420 is a precision current-loop receiver designed to convert a 4–20mA input signal into a 0–5V output signal. As a monolithic circuit, it offers high reliability at low cost. The circuit consists of a premium grade operational amplifier, an on-chip precision resistor network, and a precision 10V reference. The RCV420 features 0.1% overall conversion accuracy, 86dB CMR, and $\pm 40V$ common-mode input range.

The circuit introduces only a 1.5V drop at full scale, which is useful in loops containing extra instrument

burdens or in intrinsically safe applications where transmitter compliance voltage is at a premium. The 10V reference provides a precise 10V output with a typical drift of 5ppm/ $^{\circ}C$.

The RCV420 is completely self-contained and offers a highly versatile function. No adjustments are needed for gain, offset, or CMR. This provides three important advantages over discrete, board-level designs: 1) lower initial design cost, 2) lower manufacturing cost, and 3) easy, cost-effective field repair of a precision circuit.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

T = +25°C and V_S = ±15V unless otherwise noted.

CHARACTERISTICS	RCV420AG			RCV420BG			RCV420KP, JP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN										
Initial		0.3125		*	*			*		V/mA
Error		0.025	0.1	*	*	0.05		0.05	0.15	% of span
Error—JP Grade									0.25	% of span
vs Temp		15	50	*	*	25	*	*	*	ppm/°C
Nonlinearity ⁽¹⁾		0.0002	0.002	*	*	*	*	*	*	% of span
OUTPUT										
Rated Voltage (I _O = +10mA, -5mA)	10	12		*	*		*	*		V
Rated Current (E _O = 10V)	+10, -5			*	*		*	*		mA
Impedance (Differential)		0.01		*	*		*	*		Ω
Current Limit (To Common)		+49, -13		*	*		*	*		mA
Capacitive Load (Stable Operation)		1000		*	*		*	*		pF
INPUT										
Sense Resistance	74.25	75	75.75	*	*	*	*	*	*	Ω
Input Impedance (Common Mode)		200		*	*	*	*	*	*	kΩ
Common Mode Voltage			±40	*	*	*	*	*	*	V
CMR ⁽²⁾	72	80		86	94		70	*	*	dB
vs Temp (DC) (T _A = T _{MIN} to T _{MAX})	66	76		80	90		*	*	*	dB
AC 60Hz		80			94			*	*	dB
OFFSET VOLTAGE (RTO)⁽³⁾										
Initial			1			*			*	mV
vs Temp		10	50	*	*	25	*	*	*	μV/°C
vs Supply (±11.4V to ±18V)	74	90		80	*	*	*	*	*	dB
vs Time		200			*	*	*	*	*	μV/mo
ZERO ERROR⁽⁴⁾										
Initial		0.01	0.05		*	0.025		0.025	0.075	% of span
Initial—JP Grade					*	*		*	0.15	% of span
vs Temp		10	50		*	25		*	*	ppm of span/°C
OUTPUT NOISE VOLTAGE										
f _B = 0.1Hz to 10Hz		50			*	*		*	*	μVp-p
f _O = 10kHz		800			*	*		*	*	nV/√Hz
DYNAMIC RESPONSE										
Gain Bandwidth		150			*	*		*	*	kHz
Full Power Bandwidth		30			*	*		*	*	kHz
Slew Rate		1.5			*	*		*	*	V/μs
Settling Time (0.01%)		10			*	*		*	*	μs
VOLTAGE REFERENCE										
Initial	9.995		10.005	*	*	*	9.99		10.01	V
Trim Range ⁽⁵⁾		±4		*	*	*	*	*	*	%
vs Temp ⁽⁶⁾		5	20	*	*	*	*	*	*	ppm/°C
vs Supply (±11.4V to ±18V)		0.0002		*	*	*	*	*	*	%/V
vs Output Current (I _O = 0 to +10mA)		0.0002		*	*	*	*	*	*	%/mA
vs Time		15		*	*	*	*	*	*	ppm/kHr
Noise (0.1Hz to 10Hz)		5		*	*	*	*	*	*	μVp-p
Output Current	+10, -2			*	*	*	*	*	*	mA
POWER SUPPLY										
Rated		±15		*	*	*	*	*	*	V
Voltage Range ⁽⁷⁾	-5, +11.4		±18	*	*	*	*	*	*	V
Quiescent Current (V _O = 0V)		3	4	*	*	*	*	*	*	mA
TEMPERATURE RANGE										
Specification	-25		+85	*	*	*	0		+70	°C
Operation	-55		+125	*	*	*	-25		+85	°C
Storage	-65		+150	*	*	*	-40		+85	°C

*Specification same as RCV420AG.

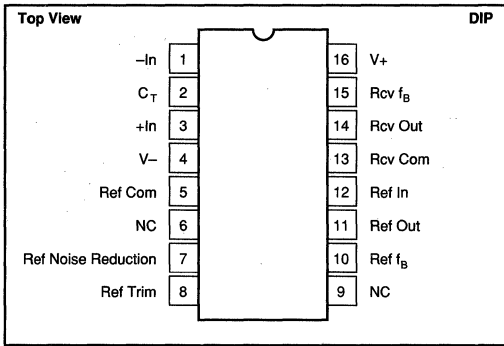
NOTES: (1) Nonlinearity is the max peak deviation from best fit straight line. (2) With 0 source impedance on Rcv Com pin. (3) Referred to output with all inputs grounded including Ref In. (4) With 4mA input signal and Voltage Reference connected (includes V_{OS}, Gain Error, and Voltage Reference Errors). (5) External trim slightly affects drift. (6) The "box method" is used to specify output voltage drift vs temperature. (7) I_O Ref = 5mA, I_O Rcv = 2mA.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±22V
Input Current, Continuous	40mA
Input Current Momentary, 0.1s	250mA, 1% Duty Cycle
Common Mode Input Voltage, Continuous	±40V
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Common (Rcv and Ref)	Continuous

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
RCV420AG	16-Pin Hermetic DIP	109
RCV420BG	16-Pin Hermetic DIP	109
RCV420KP	16-Pin Plastic DIP	180
RCV420JP	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PERFORMANCE GRADE	PACKAGE
RCV420AG	-25°C to +85°C	16-Pin Hermetic DIP
RCV420BG	-25°C to +85°C	16-Pin Hermetic DIP
RCV420KP	0°C to +70°C	16-Pin Plastic DIP
RCV420JP	0°C to +70°C	16-Pin Plastic DIP

Or, Call Customer Service at 1-800-548-6132 (USA Only)

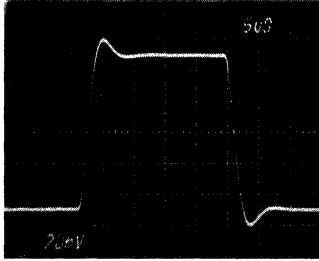
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.

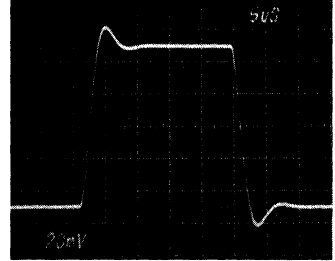
STEP RESPONSE
NO LOAD



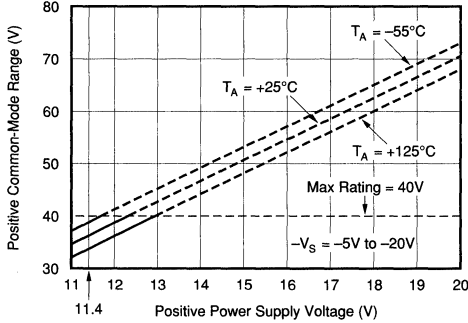
SMALL SIGNAL RESPONSE
NO LOAD



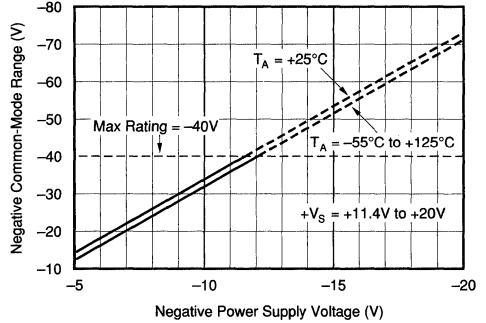
SMALL SIGNAL RESPONSE
 $R_L = \infty$, $C_L = 1000\text{pF}$



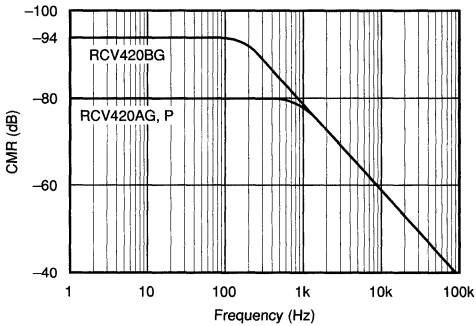
POSITIVE COMMON-MODE VOLTAGE RANGE
vs POSITIVE POWER SUPPLY VOLTAGE



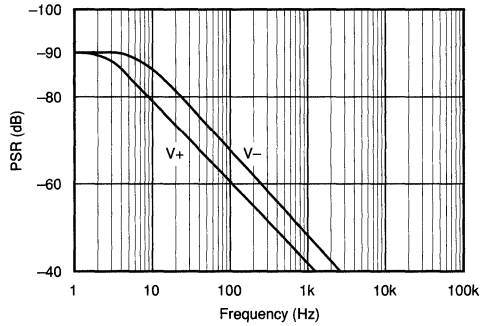
NEGATIVE COMMON-MODE VOLTAGE RANGE
vs NEGATIVE POWER SUPPLY VOLTAGE



COMMON-MODE REJECTION
vs FREQUENCY



POWER-SUPPLY REJECTION
vs FREQUENCY



RCV420

4

INSTRUMENTATION AMPLIFIERS

THEORY OF OPERATION

Refer to the figure on the first page. For 0–5V output with 4–20mA input, the required transimpedance of the circuit is:

$$V_{OUT}/I_{IN} = 5V/16mA = 0.3125V/mA.$$

To achieve the desired output (0V for 4mA and 5V for 20mA), the output of the amplifier must be offset by an amount:

$$V_{OS} = -(4mA)(0.3125V/mA) = -1.25V.$$

The input current signal is connected to either +In or –In, depending on the polarity of the signal, and returned to ground through the center tap, C_T . The balanced input—two matched 75Ω sense resistors, R_S —provides maximum rejection of common-mode voltage signals on C_T and true differential current-to-voltage conversion. The sense resistors convert the input current signal into a proportional voltage, which is amplified by the differential amplifier. The voltage gain of the amplifier is:

$$A_D = 5V/(16mA)(75\Omega) = 4.1667V/V.$$

The tee network in the feedback path of the amplifier provides a summing junction used to generate the required –1.25V offset voltage. The input resistor network provides high-input impedance and attenuates common-mode input voltages to levels suitable for the operational amplifier's common-mode signal capabilities.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Both supplies should be decoupled with $1\mu F$ tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. The input signal should be connected to either +In or –In, depending on its polarity, and returned to ground through the center tap, C_T . The output of the voltage reference, Ref Out, should be connected to Ref In for the necessary level

shifting. If the Ref In pin is not used for level shifting, then it must be grounded to maintain high CMR.

GAIN AND OFFSET ADJUSTMENT

Figure 2 shows the circuit for adjusting the RCV420 gain. Increasing the gain of the RCV420 is accomplished by inserting a small resistor in the feedback path of the amplifier. Increasing the gain using this technique results in CMR degradation, and therefore, gain adjustments should be kept as small as possible. For example, a 1% increase in gain is typically realized with a 125Ω resistor, which degrades CMR by about 6dB.

A decrease in gain can be achieved by placing matched resistors in parallel with the sense resistors, also shown in Figure 2. The adjusted gain is given by the following expression

$$V_{OUT}/I_{IN} = 0.3125 \times R_X/(R_X + R_S).$$

A 1% decrease in gain can be achieved with a $7.5k\Omega$ resistor. It is important to match the parallel resistance on each sense resistor to maintain high CMR. The TCR mismatch between the two external resistors will effect gain error drift and CMR drift.

There are two methods for nulling the RCV420 output offset voltage. The first method applies to applications using the internal 10V reference for level shifting. For these applica-

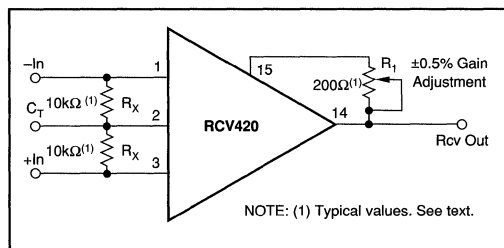


FIGURE 2. Optional Gain Adjustment.

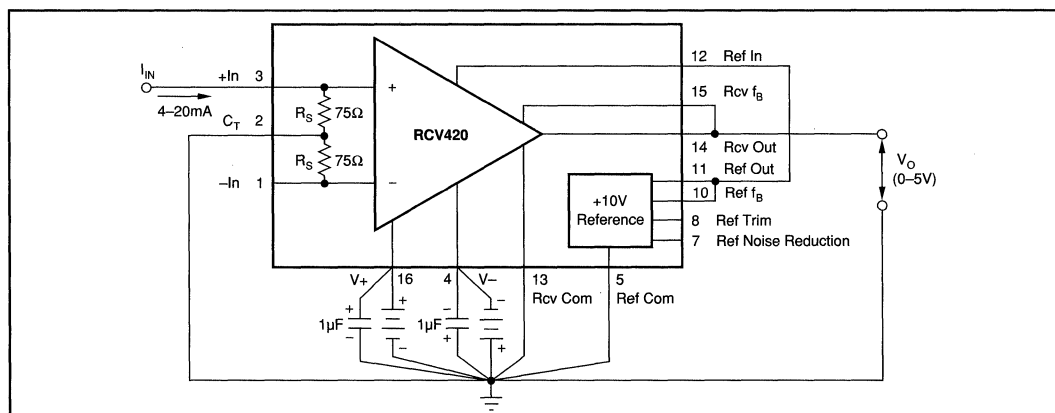


FIGURE 1. Basic Power Supply and Signal Connections.

tions, the voltage reference output trim procedure can be used to null offset errors at the output of the RCV420. The voltage reference trim circuit is discussed under "Voltage Reference."

When the voltage reference is not used for level shifting or when large offset adjustments are required, the circuit in Figure 3 can be used for offset adjustment. A low impedance on the Rcv Com pin is required to maintain high CMR.

ZERO ADJUSTMENT

Level shifting the RCV420 output voltage can be achieved using either the Ref In pin or the Rcv Com pin. The disadvantage of using the Ref In pin is that there is an 8:1 voltage attenuation from this pin to the output of the RCV420. Thus, use the Rcv Com pin for large offsets, because the voltage on this pin is seen directly at the output. Figure 4 shows the circuit used to level-shift the output of the RCV420 using the

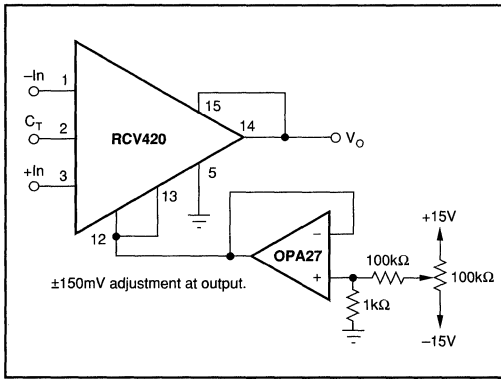


FIGURE 3. Optional Output Offset Nulling Using External Amplifier.

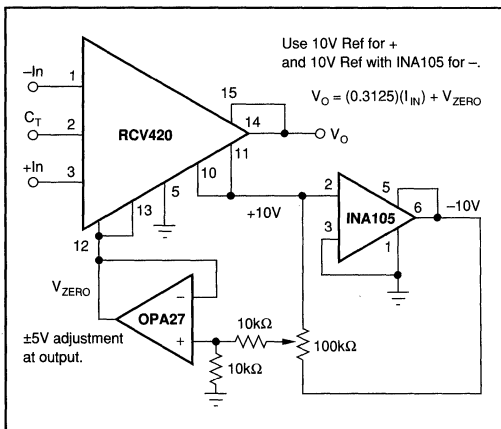


FIGURE 4. Optional Zero Adjust Circuit.

Rcv Com pin. It is important to use a low-output impedance amplifier to maintain high CMR. With this method of zero adjustment, the Ref In pin must be connected to the Rcv Com pin.

MAINTAINING COMMON-MODE REJECTION

Two factors are important in maintaining high CMR: (1) resistor matching and tracking (the internal resistor network does this) and (2) source impedance. CMR depends on the accurate matching of several resistor ratios. The high accuracies needed to maintain the specified CMR and CMR temperature coefficient are difficult and expensive to reliably achieve with discrete components. Any resistance imbalance introduced by external circuitry directly affects CMR. These imbalances can occur by: mismatching sense resistors when gain is decreased, adding resistance in the feedback path when gain is increased, and adding series resistance on the Rcv Com pin.

The two sense resistors are laser-trimmed to typically match within 0.01%; therefore, when adding parallel resistance to decrease gain, take care to match the parallel resistance on each sense resistor. To maintain high CMR when increasing the gain of the RCV420, keep the series resistance added to the feedback network as small as possible. Whether the Rcv Com pin is grounded or connected to a voltage reference for level shifting, keep the series resistance on this pin as low as possible. For example, a resistance of 20Ω on this pin degrades CMR from 86dB to approximately 80dB. For applications requiring better than 86dB CMR, the circuit shown in Figure 5 can be used to adjust CMR.

PROTECTING THE SENSE RESISTOR

The 75Ω sense resistors are designed for a maximum continuous current of 40mA, but can withstand as much as 250mA for up to 0.1s (see absolute maximum ratings). There are several ways to protect the sense resistor from overcur-

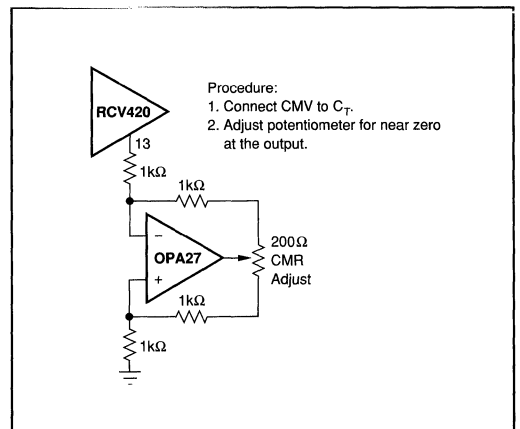


FIGURE 5. Optional Circuit for Externally Trimming CMR.

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rent conditions exceeding these specifications. Refer to Figure 6. The simplest and least expensive method is a resistor as shown in Figure 6a. The value of the resistor is determined from the expression

$$R_x = V_{CC}/40\text{mA} - 75\Omega$$

and the full scale voltage drop is

$$V_{RX} = 20\text{mA} \times R_x$$

For a system operating off of a 32V supply $R_x = 725\Omega$ and $V_{RX} = 14.5\text{V}$. In applications that cannot tolerate such a large voltage drop, use circuits 6b or 6c. In circuit 6b a power JFET and source resistor are used as a current limit. The 200Ω potentiometer, R_x , is adjusted to provide a current limit of approximately 30mA. This circuit introduces a 1-4V drop at full scale. If only a very small series voltage drop at full scale can be tolerated, then a 0.032A series 217 fast-acting fuse should be used, as shown in Figure 6c.

For automatic fold-back protection, use the circuit shown in Figure 15.

VOLTAGE REFERENCE

The RCV420 contains a precision 10V reference. Figure 8 shows the circuit for output voltage adjustment. Trimming the output will change the voltage drift by approximately 0.007ppm/°C per mV of trimmed voltage. Any mismatch in TCR between the two sides of the potentiometer will also affect drift, but the effect is divided by approximately 5. The trim range of the voltage reference using this method is typically $\pm 400\text{mV}$. The voltage reference trim can be used to trim offset errors at the output of the RCV420. There is an 8:1 voltage attenuation from Ref In to Rcv Out, and thus the trim range at the output of the receiver is typically $\pm 50\text{mV}$.

The high-frequency noise (to 1MHz) of the voltage reference is typically 1mVp-p. When the voltage reference is used for level shifting, its noise contribution at the output of the receiver is typically 125 μV p-p due to the 8:1 attenuation from Ref In to Rcv Out. The reference noise can be reduced by connecting an external capacitor between the Noise Reduction pin and ground. For example, 0.1 μF capacitor reduces the high-frequency noise to about 200 μV p-p at the output of the reference and about 25 μV p-p at the output of the receiver.

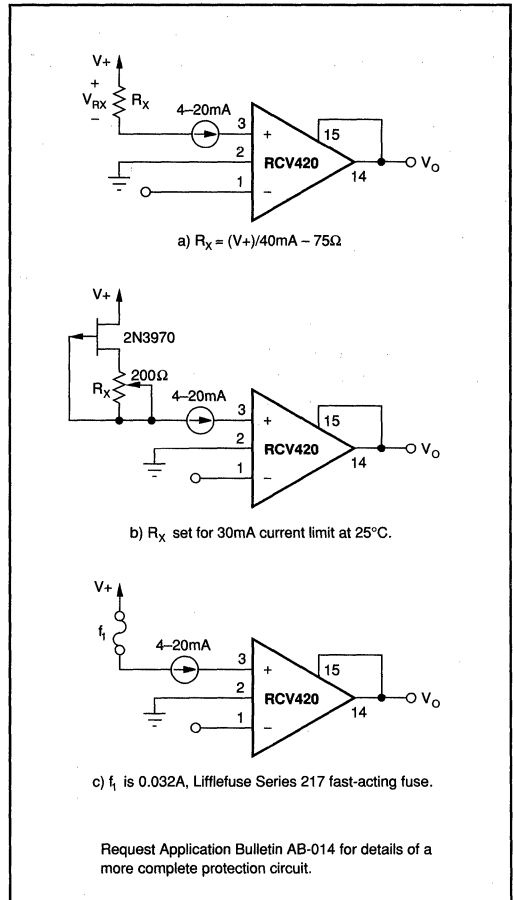


FIGURE 6. Protecting the Sense Resistors.

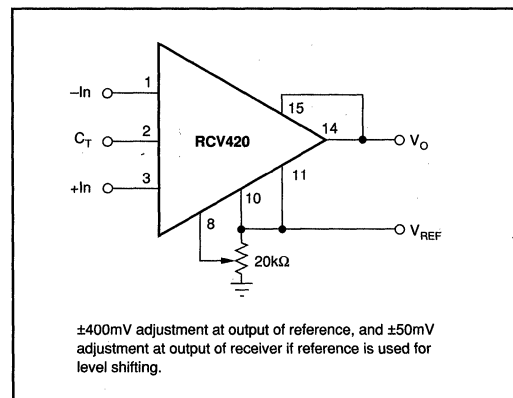


FIGURE 7. Optional Voltage Reference External Trim Circuit.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

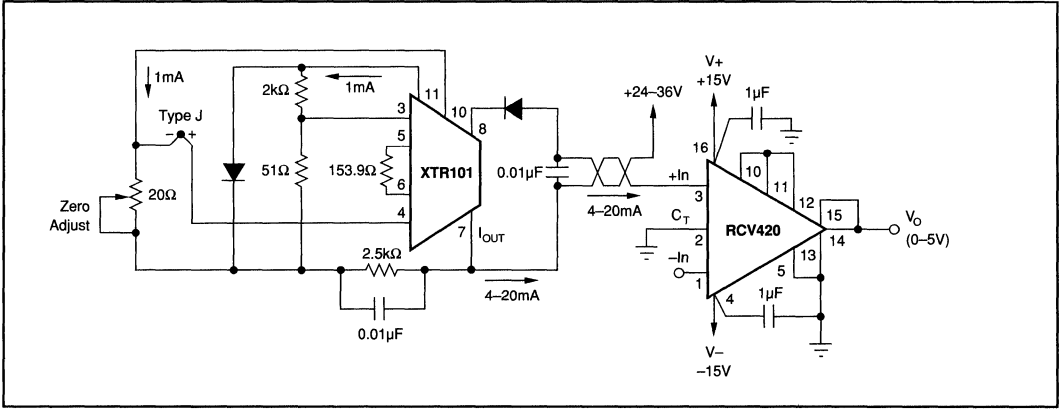


FIGURE 8. RCV420 Used in Conjunction with XTR101 to Form a Complete Solution for 4–20mA Loop.

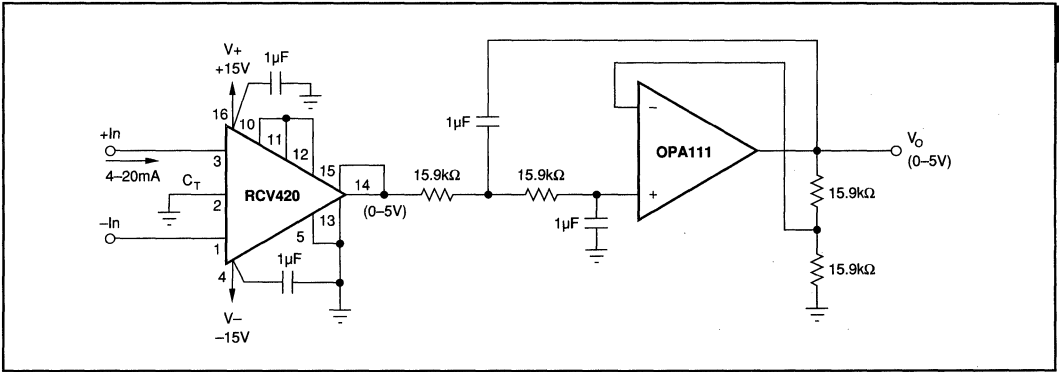


FIGURE 9. 4–20mA to 0–10V Conversion With Second-Order Active Low-Pass Filtering ($f_{-3dB} = 10\text{Hz}$).

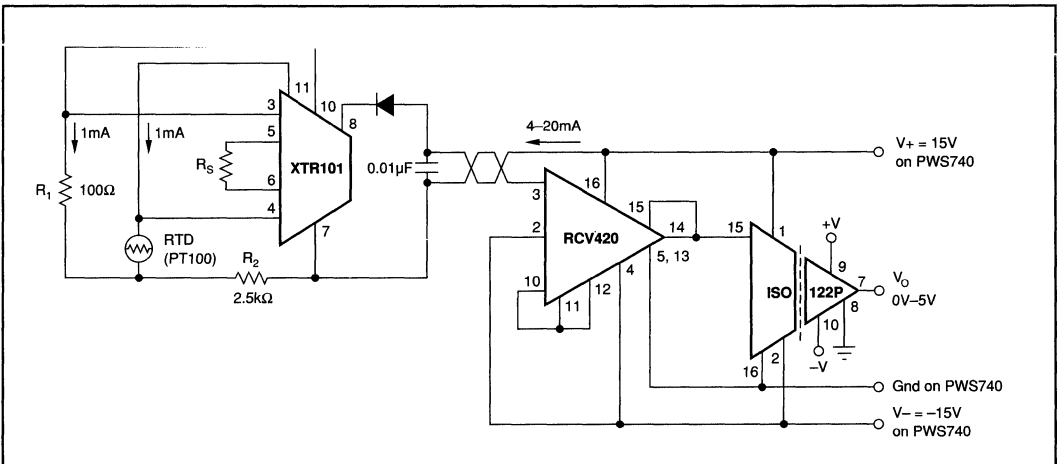
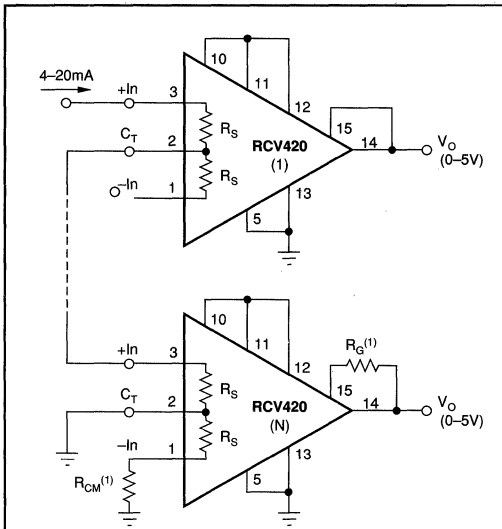


FIGURE 10. Isolated 4–20mA Instrument Loop (RTD shown).



NOTE: (1) R_{CM} and R_G are used to provide a first order correction of CMR and Gain Error, respectively. Table 1 gives typical resistor values for R_{CM} and R_G when as many as three RCV420s are stacked. Table 2 gives typical CMR and Gain Error with no correction. Further improvement in CMR and Gain Error can be achieved using a 500k Ω potentiometer for R_{CM} and a 100 Ω potentiometer for R_G .

RCV420	R_{CM} (k Ω)	R_G (Ω)
1	∞	0
2	200	7
3	67	23

TABLE 1. Typical Values for R_{CM} and R_G .

RCV420	CMR (dB)	GAIN ERROR %
1	94	0.025
2	68	0.075
3	62	0.200

TABLE 2. Typical CMR and Gain Error Without Correction.

FIGURE 11. Series 4-20mA Receivers.

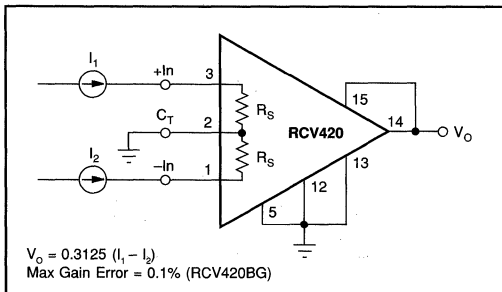


FIGURE 12. Differential Current-to-Voltage Converter.

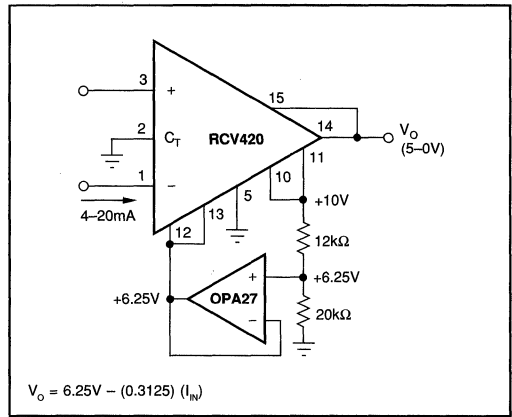


FIGURE 13. 4-20mA to 5-0V Conversion.

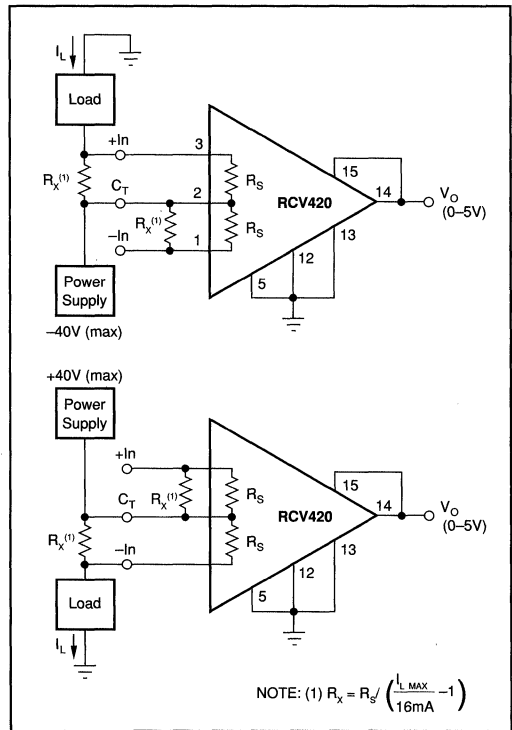


FIGURE 14. Power Supply Current Monitor Circuit.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

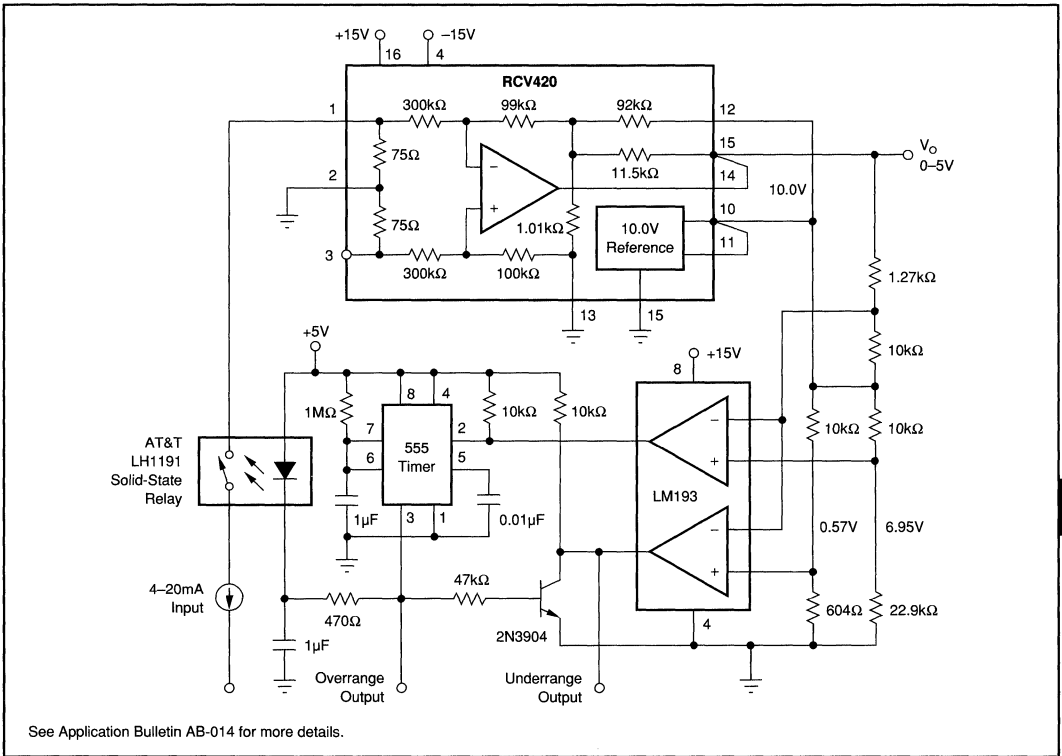


FIGURE 15. 4-20mA Current Loop Receiver with Input Overload Protection.

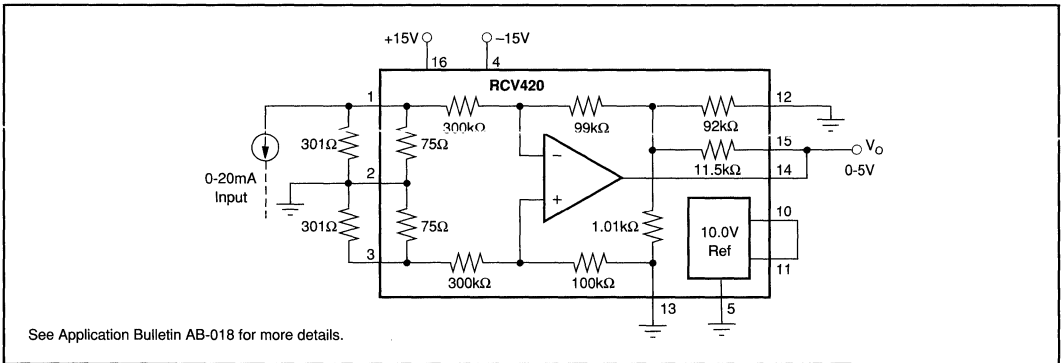
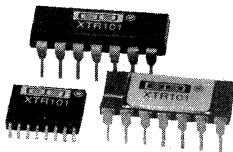


FIGURE 16. 0-20mA/0-5V Receiver Using RCV420.

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BURR-BROWN®
BB



XTR101

Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
Low Offset Voltage, 30 μ V max
Low Voltage Drift, 0.75 μ V/ $^{\circ}$ C max
Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
Power and Signal on One Wire Pair
Current Mode Signal Transmission
High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40 $^{\circ}$ C to +85 $^{\circ}$ C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC

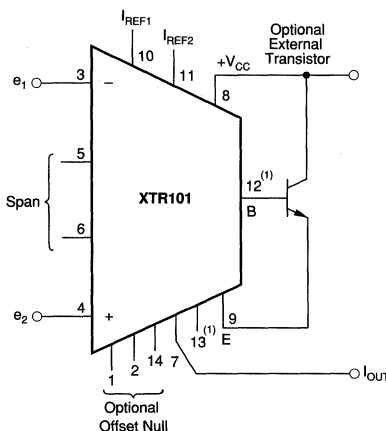
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
Pressure Transmitters
Temperature Transmitters
Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- PRECISION DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER/PLANT ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.



NOTE: (1) Pins 12 and 13 are used for optional BW control.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $+V_{CC} = 24\text{VDC}$, $R_L = 100\Omega$ with external transistor connected, unless otherwise noted

PARAMETER	CONDITIONS	XTR101AG			XTR101BG			XTR101AP			XTR101AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT AND LOAD CHARACTERISTICS														
Current	Linear Operating Region	4		20	*	*	*	*	*	*	*	*	*	mA
	Derated Performance	3.8		22	*	*	*	*	*	*	*	*	*	mA
Current Limit			28	38				31	*			31	*	mA
Offset Current Error vs Temperature	I_{OS} , $I_O = 4\text{mA}$ $\Delta I_{OS}/\Delta T$		± 3.9	± 10		± 2.5	± 6		± 8.5	± 19		± 8.5	± 19	μA
Full Scale Output Current Error	Full Scale = 20mA		± 20	± 40		± 15	± 30		± 30	± 60		± 30	± 60	ppm, FS/°C
Power Supply Voltage	V_{CC} , Pins 7 and 8, Compliance ⁽¹⁾	+11.6		± 40	*	*	*	*	*	*	*	*	*	VDC
Load Resistance	At $V_{CC} = +24\text{V}$, $I_O = 20\text{mA}$ At $V_{CC} = +40\text{V}$, $I_O = 20\text{mA}$			600 1400		*	*			600 1400		*	*	Ω
SPAN														
Output Current Equation	R_B in Ω , e_1 and e_2 in V					$I_O = 4\text{mA} + [0.016\Omega + (40/R_B)](e_2 - e_1)$								
Span Equation vs Temperature	R_B in Ω Excluding TCR of R_B		± 30	± 100		$S = [0.016\Omega + (40/R_B)]$								A/V ppm/°C
Untrimmed Error ⁽²⁾	ϵ_{SPAN}	-5	-2.5	0	*	*	*	*	*	*	*	*	*	%
Nonlinearity	$\epsilon_{NONLINEARITY}$			0.01	*	*	*	*	*	*	*	*	*	%
Hysteresis			0		*	*	*	*	*	*	*	*	*	%
Dead Band			0		*	*	*	*	*	*	*	*	*	%
INPUT CHARACTERISTICS														
Impedance: Differential			0.4 3			*	*	*	*	*	*	*	*	G Ω pF
Common-Mode			10 3			*	*	*	*	*	*	*	*	G Ω pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)^{(3)}$	0		1	*									V
Offset Voltage vs Temperature	V_{OS} $\Delta V_{OS}/\Delta T$		± 30	± 60		± 20	± 30		± 100				± 100	μV
Power Supply Rejection	$\Delta V_{CC}/\text{PSRR} = V_{OS}$ Error	110	125		*	*	*	*	*	*	110	122	*	dB
Bias Current vs Temperature	I_B $\Delta I_B/\Delta T$		60	150		*	*	*	*	*	*	*	*	nA
Offset Current vs Temperature	I_{OS} $\Delta I_{OS}/\Delta T$		10	± 30		*	*	*	*	*	*	*	*	nA
Common-Mode Rejection ⁽⁴⁾	DC	90	100		*	*	*	*	*	*	*	*	*	dB
Common-Mode Range	e_1 and e_2 with Respect to Pin 7	4		6	*	*	*	*	*	*	*	*	*	V
CURRENT SOURCES														
Magnitude			1			*	*	*	*	*	*	*	*	mA
Accuracy vs Temperature	$V_{CC} = 24\text{V}$, $V_{PIN8} - V_{PIN10,11} = 19\text{V}$ $R_B = 5\text{k}\Omega$, Fig. 5		± 0.06	± 0.17		± 0.025	± 0.075		± 0.2	± 0.37		± 0.2	± 0.37	%
vs V_{CC}			± 50	± 80		± 30	± 50		*	*		*	*	ppm/°C
vs Time			± 3		*	*	*	*	*	*	*	*	*	ppm/V
Compliance Voltage	With Respect to Pin 7	0		$V_{CC} - 3.5$	*	*	*	*	*	*	*	*	*	ppm/month
Ratio Match Accuracy	Tracking ($1 - I_{REF}/I_{REF}$) X 100%		± 0.014	± 0.06		± 0.009	± 0.04		± 0.031	± 0.088		± 0.031	± 0.088	V
vs Temperature				± 15		*	*	*	*	*	*	*	*	ppm/°C
vs V_{CC}			± 10			*	*	*	*	*	*	*	*	ppm/V
vs Time			± 1			*	*	*	*	*	*	*	*	ppm/month
Output Impedance		10	20		*	*	*	*	15	*	*	15	*	M Ω
TEMPERATURE RANGE														
Specification		-40		+85	*	*	*	*	+85	*	*	*	*	°C
Operating		-55		+125	*	*	*	*	+85	-40		+85		°C
Storage		-55		+165	*	*	*	*	+125	-55		+125		°C

4 XTR101

INSTRUMENTATION AMPLIFIERS

*Same as XTR101AG.

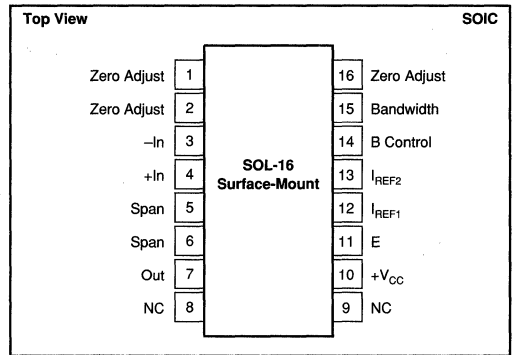
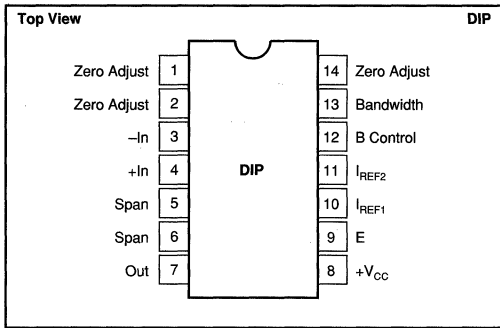
NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the -In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

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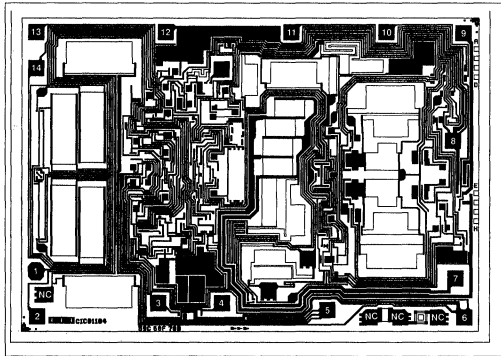


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PIN CONFIGURATION



DICE INFORMATION



XTR101 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adjust	8	+V _{CC}
2	Zero Adjust	9	E
3	-In	10	I _{REF1}
4	+In	11	I _{REF2}
5	Span	12	B Control
6	Span	13	Bandwidth
7	Out	14	Zero Adjust

NC: No Connection

Substrate Bias: Electrically connected to V- supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 105 ±5	3.81 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

ABSOLUTE MAXIMUM RATINGS

Power Supply, +V _{CC}	40V
Input Voltage, e ₁ or e ₂	≥V _{OUT} , ≤+V _{CC}
Storage Temperature Range, Ceramic	-55°C to +165°C
Plastic	-55°C to +125°C
Lead Temperature (soldering 10s) G, P	+300°C
(wave soldering, 3s) U	+260°C
Output Short-Circuit Duration	Continuous +V _{CC} to I _{OUT}
Junction Temperature	+165°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
XTR101AG	14-Pin Ceramic DIP	169
XTR101BG	14-Pin Ceramic DIP	169
XTR101AP	14-Pin Plastic DIP	010
XTR101AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

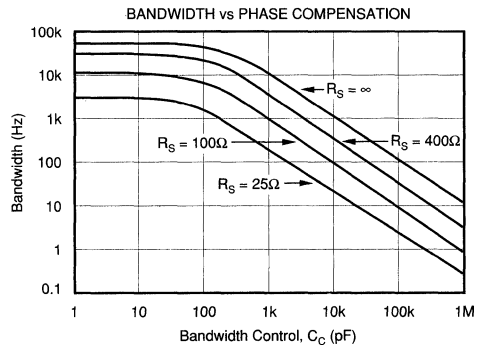
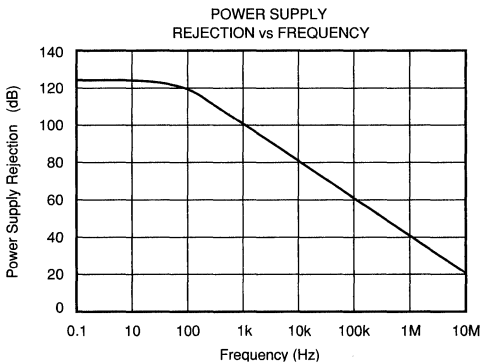
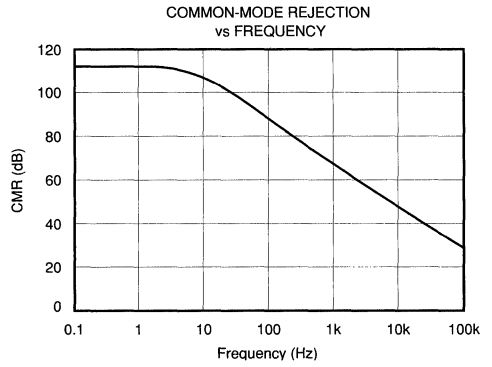
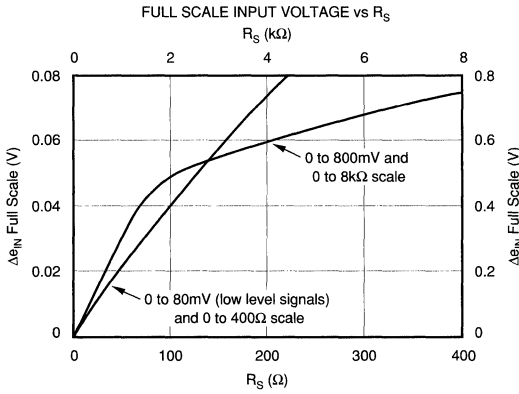
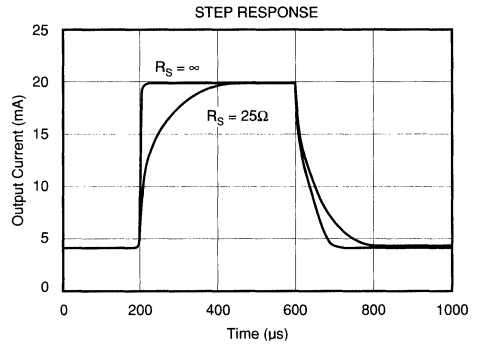
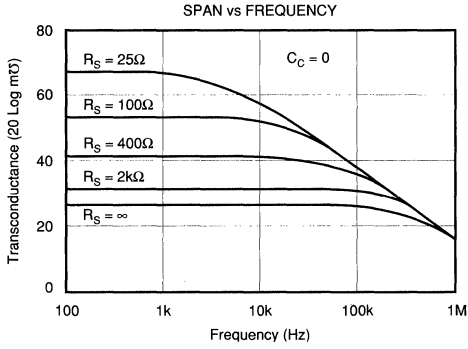
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR101AG	14-Pin Ceramic DIP	-40°C to +85°C
XTR101BG	14-Pin Ceramic DIP	-40°C to +85°C
XTR101AP	14-Pin Plastic DIP	-40°C to +85°C
XTR101AU	16-Pin SOIC	-40°C to +85°C

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $+V_{CC} = 24\text{VDC}$ unless otherwise noted.



XTR101

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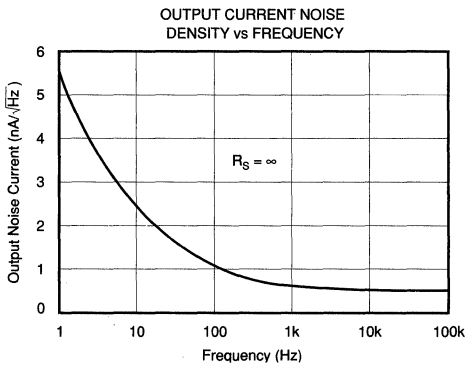
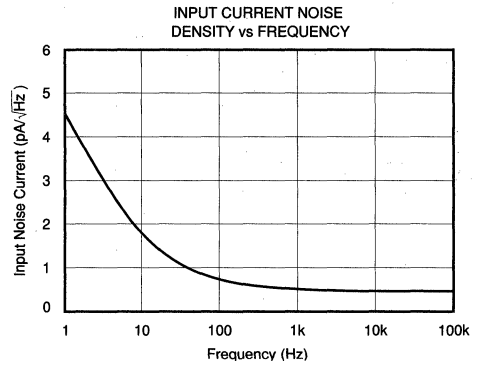
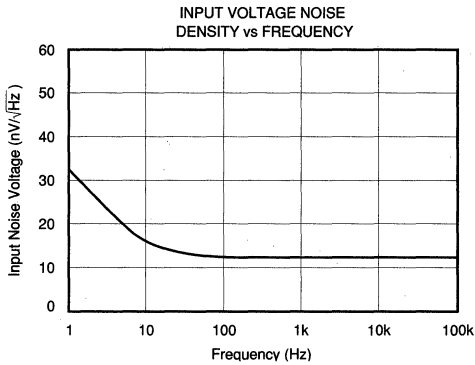
INSTRUMENTATION AMPLIFIERS



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $+V_{CC} = 24\text{VDC}$ unless otherwise noted.



THEORY OF OPERATION

A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2 , act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1 . Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S , the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3 , to form I_1 . The circuit is configured such that I_2 is 19 times I_1 . From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0\text{V}$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN} . Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\text{V} + 40/R_S)(e_{IN} \text{ full scale}) = 16\text{mA}$. Note that since I_O is unipolar e_2 must be kept larger than e_1 ;

i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4-20mA to circulate in the two-wire output loop (through R_L , V_{PS} , and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also in

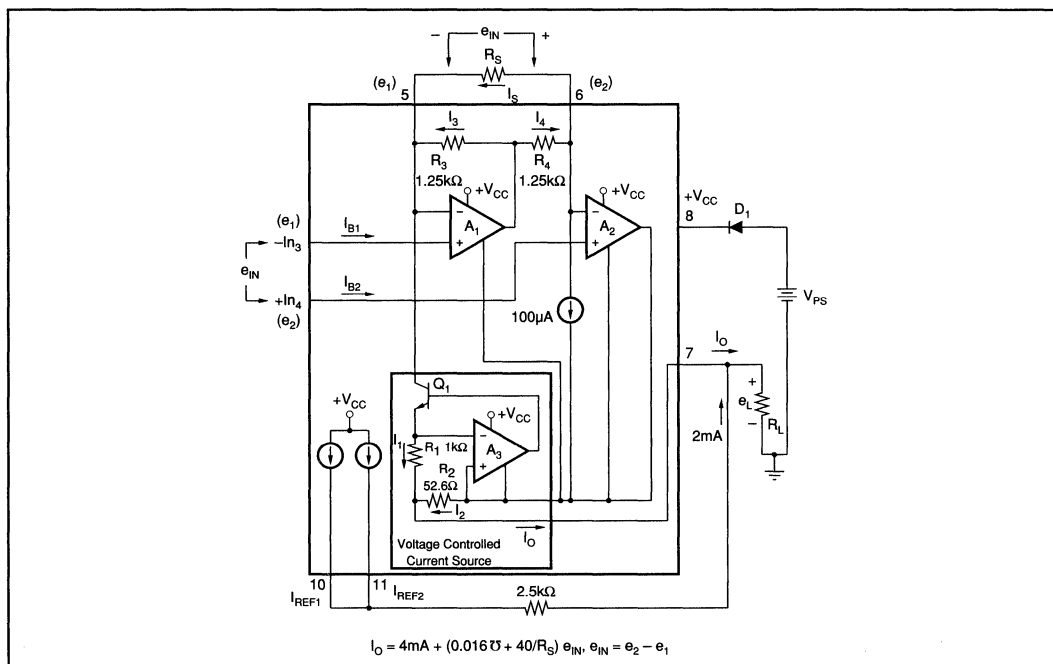


FIGURE 1. Simplified Schematic of the XTR101.

such applications where e_{IN} full scale is small ($<50\text{mV}$) and R_{SPAN} is small ($<150\Omega$), caution should be taken to consider errors from the external span circuit plus high amplification of offset drift and noise.

OPTIONAL EXTERNAL TRANSISTOR

The optional external transistor, when used, is connected in parallel with the XTR101's internal transistor. The purpose is to increase accuracy by reducing heat change inside the XTR101 package as the output current spans from 4-20mA. Under normal operating conditions, the internal transistor is never completely turned off as shown in Figure 2. This maintains frequency stability with varying external transistor characteristics and wiring capacitance. The actual "current sharing" between internal and external transistors is dependent on two factors: (1) relative geometry of emitter areas and (2) relative package dissipation (case size and thermal conductivity). For best results, the external device should have a larger base-emitter area and smaller package. It will, upon turn on, take about $[0.95 (I_0 - 3.3\text{mA})]\text{mA}$. However, it will heat faster and take a greater share after a few seconds.

Although any NPN of suitable power rating will operate with the XTR101, two readily available transistors are recommended.

1. 2N2222 in the TO-18 package. For power supply voltages above 24V, a 750Ω, 1/2W resistor should be connected in series with the collector. This will limit the power dissipation to 377mW under the worst-case condi-

tions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of $+85^\circ\text{C}$. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.

2. TIP29B in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the TIP29B will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using an external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01µF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).

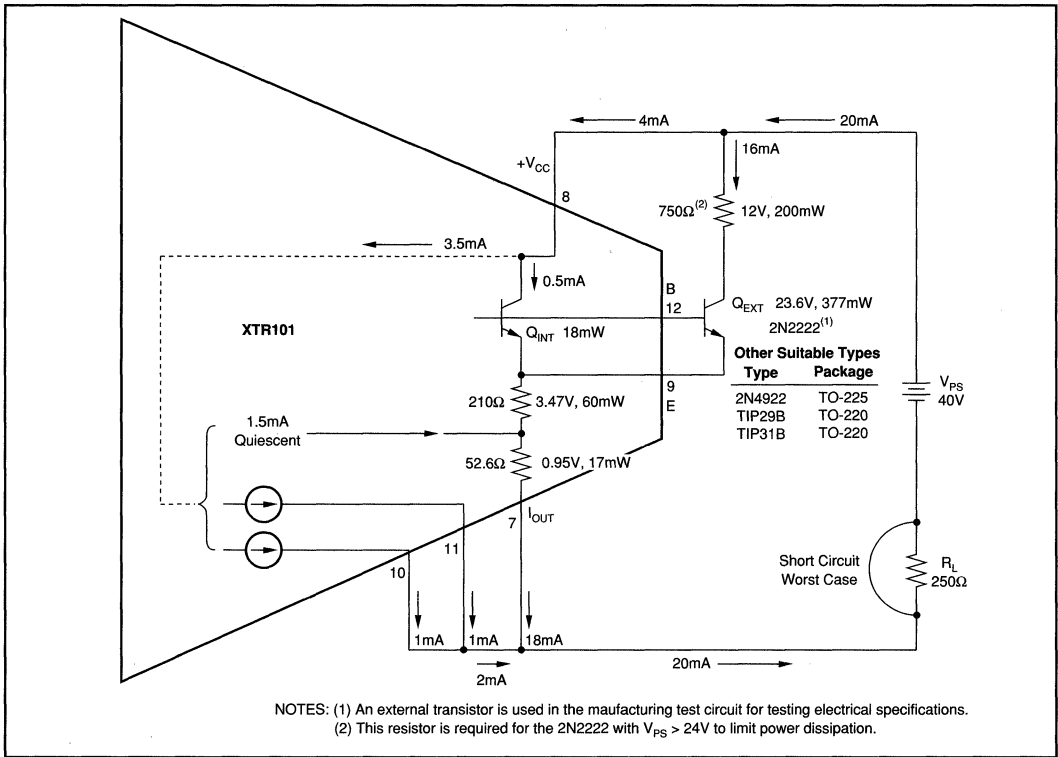


FIGURE 2. Power Calculation of XTR101 with External Transistor.

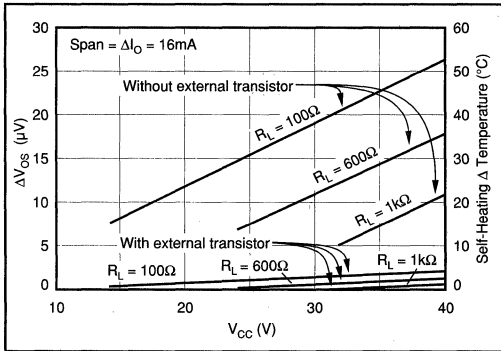


FIGURE 3. Thermal Feedback Due to Change in Output Current.

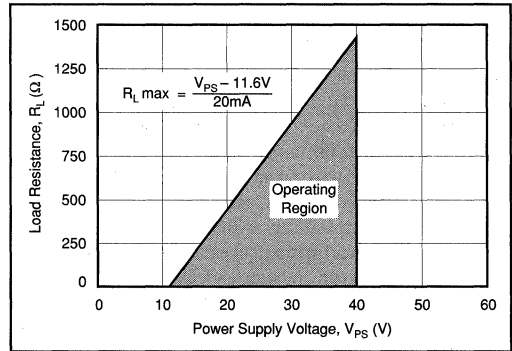


FIGURE 4. Power Supply Operating Range.

- The maximum input signal level (e_{INFS}) is 1V with $R_s = \infty$ and proportionally less as R_s decreases.
- Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and $+(V_{CC} - 4V)$ with respect to pin 7.

- Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4-20mA range (see Figure 4).
- It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.

8. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

SELECTING R_S

R_{SPAN} is chosen to that a given full scale input span e_{INFS} will result in the desired full scale output span of ΔI_{OFS} ,

$$[(0.016\zeta) + (40/R_S)] \Delta e_{IN} = \Delta I_O = 16mA.$$

Solving for R_S :

$$R_S = \frac{40}{\Delta I_O / \Delta e_{IN} - 0.016\zeta} \quad (1)$$

For example, if $\Delta e_{INFS} = 100mV$ for $\Delta I_{OFS} = 16mA$,

$$R_S = \frac{40}{16mA/100mV - 0.016} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs Δe_{INFS} . Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

Because the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin 7 to assure linear response. This is easily done by using one or both current sources and an external resistor R_2 . Figure 5 shows the simplest case—a floating voltage source e'_2 . The 2mA from the current sources flows through the 2.5k Ω value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$$\begin{aligned} +4V &\leq e_1 \leq +6V \\ +4V &\leq e_2 \leq +6V \end{aligned}$$

The offset adjustment is used to remove the offset voltage of the input amplifier. When the input differential voltage (e_{IN}) equals zero, adjust for 4mA output.

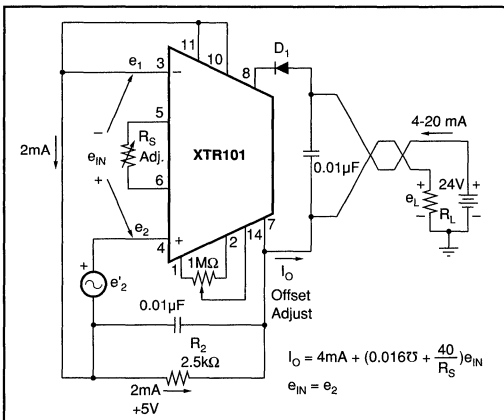


FIGURE 5. Basic Connection for Floating Voltage Source.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV then an input offset error term is $(CMV - 5)/CMRR$; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD, or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2 and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20 μ V) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by $\pm 0.3\mu V/^\circ C$ per 100 μ V or induced offset.

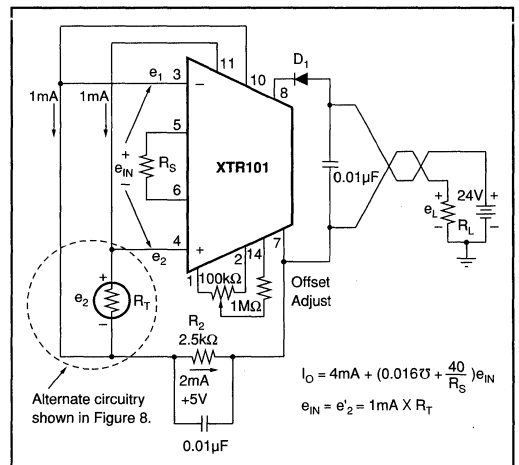


FIGURE 6. Basic Connection for Resistive Source.

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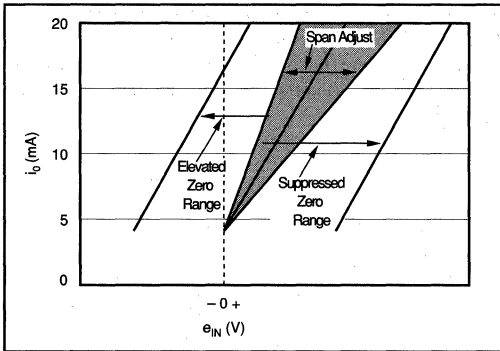


FIGURE 7. Elevation and Suppression Graph.

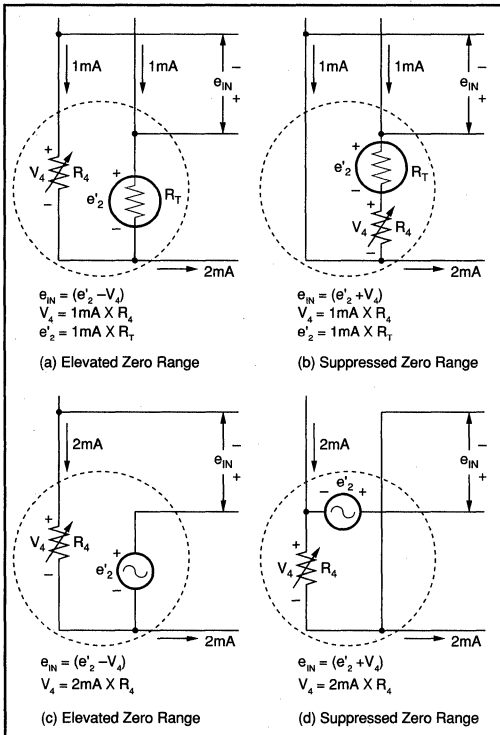


FIGURE 8. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning

at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S :

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266^\circ\text{C}$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is $1\text{mA} \times (100\Omega/266^\circ\text{C}) \times 125^\circ\text{C} = 47\text{mV} = \Delta e_{IN}$.

$$\text{From equation 1, } R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\Omega}$$

$$R_S = \frac{40}{16\text{mA}/47\text{mV} - 0.016\Omega} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S .

COMPUTING R_4 :

$$\begin{aligned} \text{At } +25^\circ\text{C, } e'_2 &= 1\text{mA} (R_T + \Delta R_T) \\ &= 1\text{mA} \left[100\Omega + \frac{100\Omega}{266^\circ\text{C}} \times 25^\circ\text{C} \right] \\ &= 1\text{mA} (109.4\Omega) = 109.4\text{mV} \end{aligned}$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN} , the XTR101 differential input, is made 0 at 25°C or

$$\begin{aligned} e'_{2,25^\circ\text{C}} - V_4 &= 0 \\ \text{thus, } V_4 &= e'_{2,25^\circ\text{C}} = 109.4\text{mV} \end{aligned}$$

$$R_4 = \frac{V_4}{1\text{mA}} = \frac{109.4\text{mV}}{1\text{mA}} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

$$\begin{aligned} \text{At } +25^\circ\text{C, } e'_2 &= 109.4\text{mV} \\ \text{At } +150^\circ\text{C, } e'_2 &= 1\text{mA} (R_T + \Delta R_T) \\ &= 1\text{mA} \left[100\Omega + \left(\frac{100\Omega}{266^\circ\text{C}} \times 150^\circ\text{C} \right) \right] \\ &= 156.4\text{mV} \end{aligned}$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

$$\begin{aligned} R_2 &= 5\text{V}/2\text{mA} = 2.5\text{k}\Omega \\ \left. \begin{aligned} e_2 \text{ min} &= 5\text{V} + 0.1094\text{V} \\ e_2 \text{ max} &= 5\text{V} + 0.1564\text{V} \\ e_1 &= 5\text{V} + 0.1094\text{V} \end{aligned} \right\} \text{The } +4\text{V to } +6\text{V CMV} \\ &\quad \text{requirement is met.} \end{aligned}$$

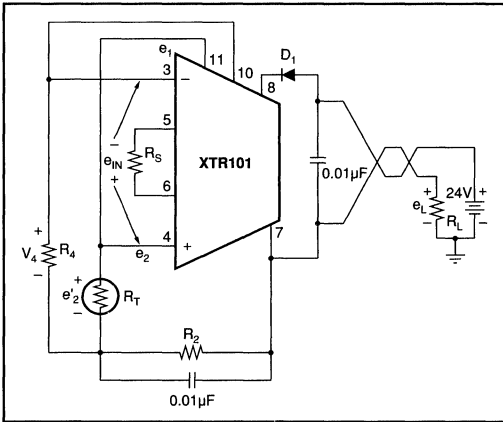


FIGURE 9. Circuit for Example 1.

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and $+1000^\circ\text{C}$, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C . This is accomplished by supplying a compensating voltage, V_{R6} , equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of $+25^\circ\text{C}$ this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for $T_1 = 0^\circ\text{C}$ and 20mA for $T_1 = +1000^\circ\text{C}$. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2 .

ESTABLISHING R_S :

The input full scale span is 58mV ($\Delta e_{INFS} = 58\text{mV}$).

R_S is found from equation (1)

$$R_S = \frac{40}{\Delta I / \Delta e_{IN} - 0.01675}$$

$$= \frac{40}{16\text{mA}/58\text{mV} - 0.01675} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4 :

R_4 is chosen to make the output 4mA at $T_{TC} = 0^\circ\text{C}$ ($V_{TC} = -1.28\text{mV}$) and $T_D = +25^\circ\text{C}$ ($V_D = 0.6\text{V}$). A circuit is shown in Figure 10.

V_{TC} will be -1.28mV when $T_{TC} = 0^\circ\text{C}$ and the reference junction is at $+25^\circ\text{C}$. e_1 must be computed for the condition of $T_D = +25^\circ\text{C}$ to make $e_{IN} = 0\text{V}$.

$$V_{D\ 25^\circ\text{C}} = 600\text{mV}$$

$$e_{1\ 25^\circ\text{C}} = 600\text{mV} (51/2051) = 14.9\text{mV}$$

$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

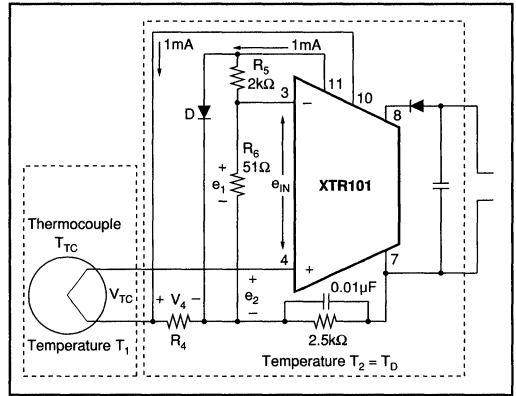


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

With $e_{IN} = 0$ and $V_{TC} = -1.28\text{mV}$,

$$V_4 = e_1 + e_{IN} - V_{TC}$$

$$= 14.9\text{mV} + 0\text{V} - (-1.28\text{mV})$$

$$1\text{mA} (R_4) = 16.18\text{mV}$$

$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = +25^\circ\text{C}$, $V_D = 0.6\text{V}$ and $\Delta V_D/\Delta T = -2\text{mV}/^\circ\text{C}$. R_5 and R_6 form a voltage divider for the diode voltage V_D . The divider values are selected so that the gradient $\Delta_V D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At $+25^\circ\text{C}$ this is approximately $52\mu\text{V}/^\circ\text{C}$ (obtained from standard thermocouple table); therefore,

$$\Delta T_C/\Delta T = \Delta_V D/\Delta T \left[\frac{R_6}{R_5 + R_6} \right] \tag{2}$$

$$52\mu\text{V}/^\circ\text{C} = 2000\mu\text{V}/^\circ\text{C} \left[\frac{R_6}{R_5 + R_6} \right]$$

R_5 is chosen as $2\text{k}\Omega$ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω .

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when

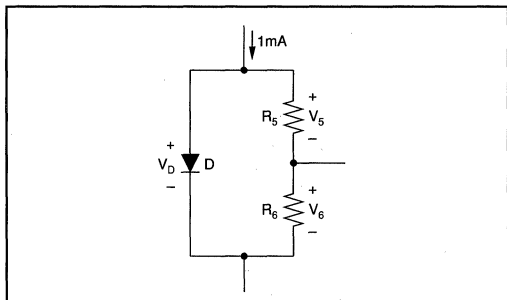


FIGURE 11. Cold Junction Compensation Circuit.

the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_o to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the T_c opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages (30 μ V max for the B grade, 60 μ V max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2 and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{co} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)(C_2 + 3pF)}$$

This method has the disadvantage of having f_{co} vary with R_1 , R_2 , R_3 , R_4 , and it may require large values of R_3 and R_4 . The other method, using C_1 , will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{co} is shown in the Typical Performance Curves.

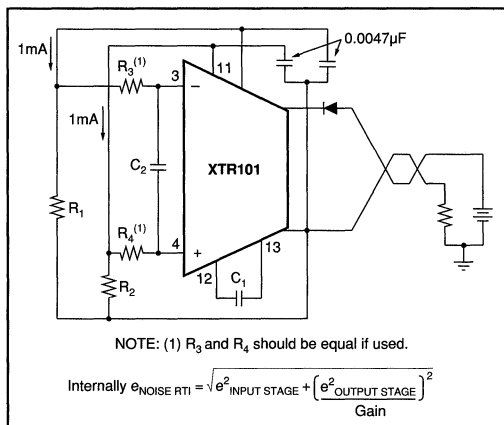


FIGURE 12. Optional Filtering.

APPLICATION CIRCUITS

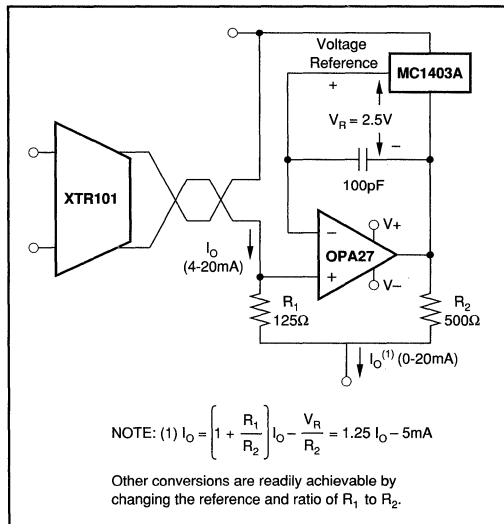


FIGURE 13. 0-20mA Output Converter.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

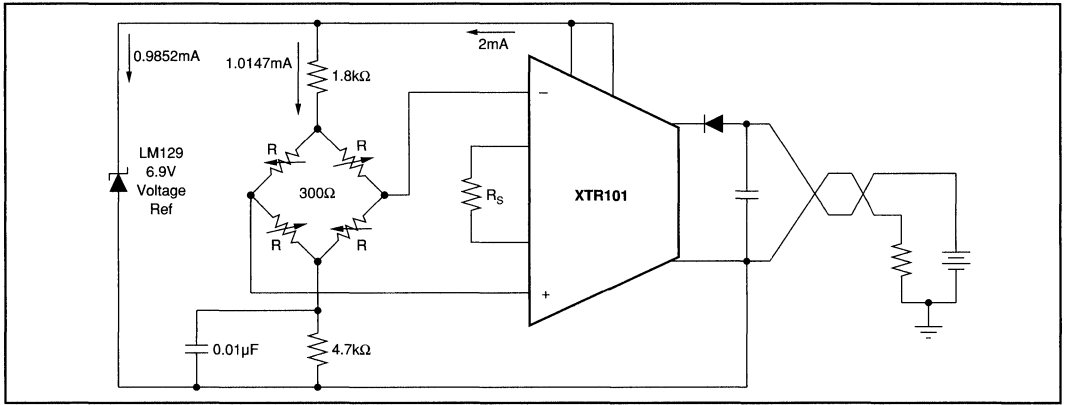


FIGURE 14. Bridge Input, Voltage Excitation.

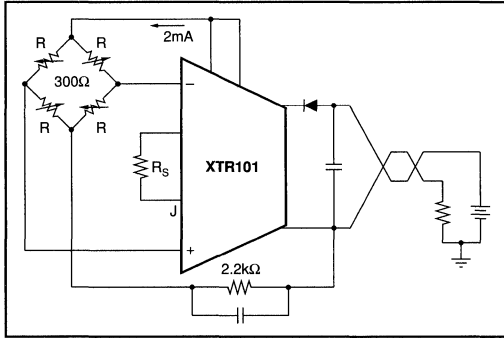


FIGURE 15. Bridge Input, Current Excitation.

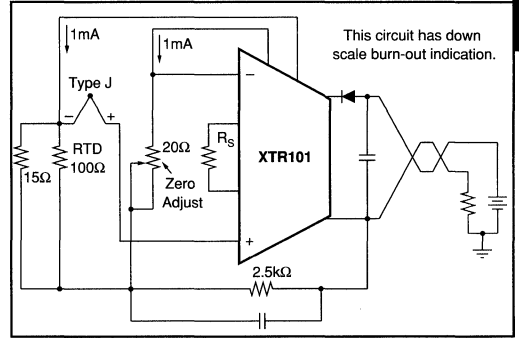


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

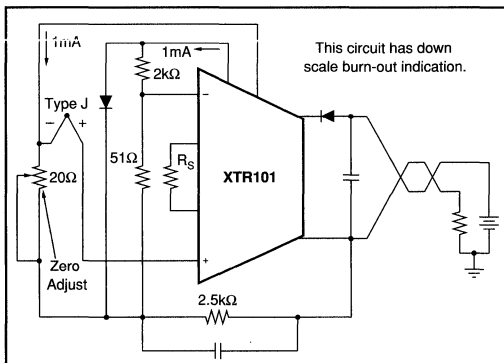


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

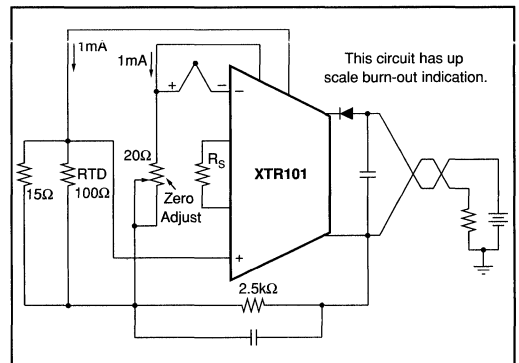


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

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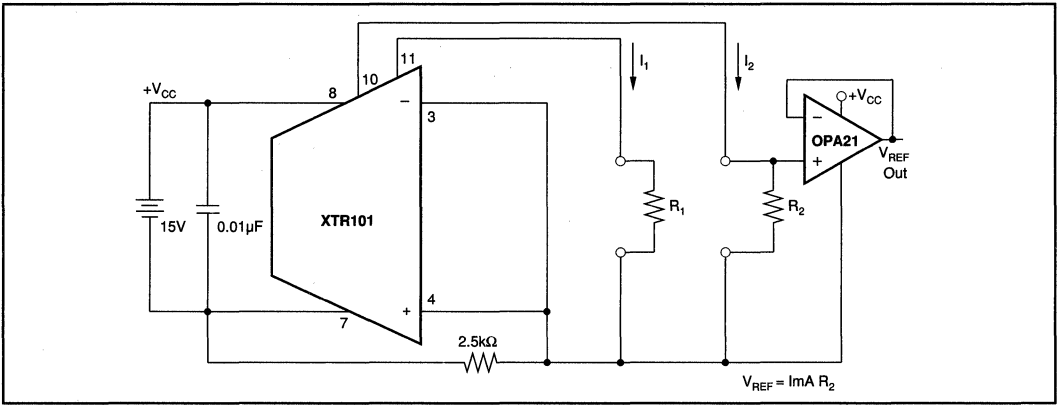


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

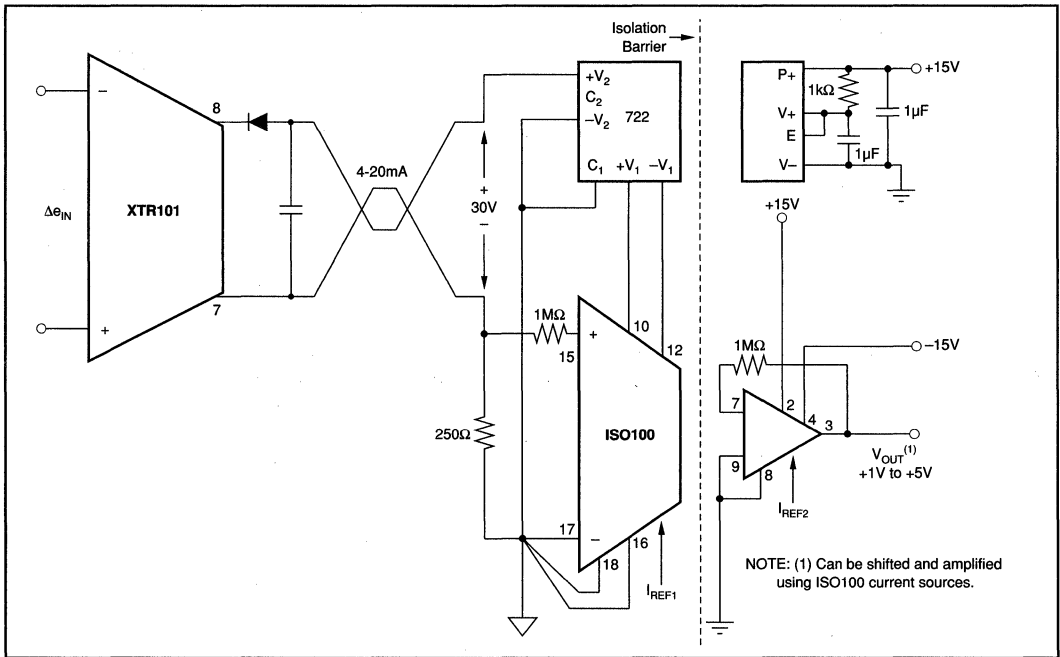


FIGURE 20. Isolated Two-Wire Current Loop.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O \text{ IDEAL}} = 4\text{mA} + K e_{\text{IN}}$$

K is the span (gain) term, $(0.016\Omega + (40/R_S))$ (3)

In the XTR101 there are three major components of error:

1. σ_O = errors associated with the output stage.
2. σ_S = errors associated with span adjustment.
3. σ_I = errors associated with the input stage.

The transfer function including these errors is

$$i_{O \text{ ACTUAL}} = (4\text{mA} + \sigma_O) + K (1 + \sigma_S)(e_{\text{IN}} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms ($\sigma_S \sigma_I$) dropped, and terms collected, the result is

$$i_{O \text{ ACTUAL}} = (4\text{mA} + \sigma_O) + K e_{\text{IN}} + K\sigma_I + K\sigma_S e_{\text{IN}} \quad (5)$$

The error in the output current is $i_{O \text{ ACTUAL}} - i_{O \text{ IDEAL}}$ and can be found by subtracting equations (5) and (3).

$$i_{O \text{ ERROR}} = \sigma_O + K\sigma_I + K\sigma_S e_{\text{IN}} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

1. $\sigma_O = I_{OS \text{ RTO}} \quad (7)$
2. $\sigma_S = \epsilon_{\text{NONLINEARITY}} + \epsilon_{\text{SPAN}} \quad (8)$

$$3. \sigma_I = V_{OSI} + (I_{B1} + R_4 - I_{B2} R_T) + \frac{\Delta V_{CC}}{\text{PSRR}} + \frac{(e_1 + e_2)/2 - 5V}{\text{CMRR}} \quad (9)$$

The term in parentheses may be written in terms of offset current and resistor mismatches as $I_{B1} \Delta R + I_{OS} R_4$.

- V_{OSI}^* = input offset voltage
- I_{B1}^*, I_{B2}^* = input bias current
- I_{OSI}^* = input offset current
- $I_{OS \text{ RTO}}^*$ = output offset current error
- $\Delta R = R_T - R_4$ = mismatch in resistor
- ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nominal
- PSRR* = power supply rejection ratio
- CMRR* = common-mode rejection ratio
- $\epsilon_{\text{NONLIN}}^*$ = span nonlinearity
- ϵ_{SPAN}^* = span equation error. Untrimmed error = 5% max. May be trimmed to zero.

Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

The circuit in Figure 9 with the XTR101BG specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_O = 4\text{mA}$ at 25°C, $I_O = 20\text{mA}$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_1 = 250\Omega$, $R_{\text{LINE}} = 100\Omega$, $V_{DI} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. AT THE LOWER RANGE VALUE (T = +25°C).

$$\sigma_O = I_{OS \text{ RTO}} = \pm 6\mu\text{A}$$

$$\sigma_I = V_{OSI} + (I_{B1} \Delta R + I_{OSI} R_4) + \frac{\Delta V_{CC}}{\text{PSRR}} + \frac{(e_1 + e_2)/2 - 5V}{\text{CMRR}}$$

$$\Delta R = R_{T \text{ 25°C}} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = (24 \times 0.005) + 4\text{mA} (250\Omega + 100\Omega) + 0.6V = 120\text{mV} + 1400\text{mV} + 600\text{mV} = 2120\text{mV}$$

$$e_1 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 109\Omega) = 5.109V$$

$$e_2 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 109.4\Omega) = 5.1094V$$

$$(e_1 + e_2)/2 - 5 = 0.1092V$$

$$\text{PSRR} = 3.16 \times 10^5 \text{ for } 110\text{dB}$$

$$\text{CMRR} = 31.6 \times 10^3 \text{ for } 90\text{dB}$$

$$\sigma_I = 30\mu\text{V} + (150\text{nA} \times 0 + 20\text{nA} \times 109\Omega)$$

$$+ \frac{2120\text{mV}}{3.16 \times 10^5} + \frac{0.1092V}{3.16 \times 10^3} \quad (10)$$

$$= 30\mu\text{V} + 2.18\mu\text{V} + 6.7\mu\text{V} + 3.46\mu\text{V} = 42.34\mu\text{V}$$

$$\sigma_S = \epsilon_{\text{NONLIN}} + \epsilon_{\text{SPAN}} = 0.0001 + 0 \text{ (assumes trim of } R_S)$$

$$I_O \text{ error} = \sigma_O + K \sigma_I + K \sigma_S e_{\text{IN}}$$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.340\Omega$$

$$e_{\text{IN}} = e_2 - V_4 = I_{\text{REF1}} R_{T \text{ 25°C}} - I_{\text{REF2}} R_4$$

since $R_{T \text{ 25°C}} = R_4$,

$$e_{\text{IN}} = (I_{\text{REF1}} - I_{\text{REF2}}) R_4 = 0.4\mu\text{A} \times 109\Omega = 43.6\mu\text{V}$$

Since the maximum mismatch of the current references is 0.04% of 1mA = 0.4μA,

$$I_O \text{ error} = 6\mu\text{A} + (0.34\Omega \times 42.34\mu\text{V}) + (0.34\Omega \times 0.0001 \times 43.6\mu\text{V}) = 6\mu\text{A} + 14.40\mu\text{A} + 0.0015\mu\text{A} = 20.40\mu\text{A}$$

$$\% \text{ error} = \frac{20.40\mu\text{A}}{16\text{mA}} \times 100\%$$

0.13% of span at lower range value.

B. AT THE UPPER RANGE VALUE (T = +150°C).

$$\Delta R = R_{T \text{ 150°C}} - R_4 = 156.4 - 109.4 = 47\Omega$$

$$\Delta V_{CC} = (24 \times 0.005) + 20\text{mA} (250\Omega + 100\Omega) +$$

$$0.6V = 7720\text{mV}$$

$$e_1 = 5.109V$$

$$e_2 = (2\text{mA} \times 2.5\text{k}\Omega) + (1\text{mA} \times 156.4\Omega) = 5.156V$$

$$(e_1 + e_2)/2 - 5V = 0.1325V$$

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$$\sigma_o = 6\mu\text{A}$$

$$\sigma_1 = 30\mu\text{V} + (150\text{nA} \times 47\Omega + 20\text{nA} \times 190\Omega)$$

$$+ \frac{7720\text{mV}}{3.16 \times 10^5} + \frac{0.1325\text{V}}{3.16 \times 10^3}$$

$$= 30\mu\text{V} + 9.23\mu\text{V} + 24\mu\text{V} + 4.19\mu\text{V}$$

$$= 67.42\mu\text{V}$$

$$\sigma_s = 0.0001$$

$$e_{\text{IN}} = e'_2 - V_4 = I_{\text{REF1}} R_{T 150^\circ\text{C}} - I_{\text{REF2}} R_4$$

$$= (1\text{mA} \times 156.4\Omega) - (1\text{mA} \times 109\Omega) = 47\text{mV}$$

$$I_o \text{ error} = \sigma_o + K \sigma_1 + K \sigma_s e_{\text{IN}} = 6\mu\text{A} +$$

$$(0.34\% \times 67.42\mu\text{V}) + (0.34\% \times 0.0001$$

$$\times 47000\mu\text{V}) = 6\mu\text{A} + 22.92\mu\text{A} + 1.60\mu\text{A}$$

$$= 30.52\mu\text{A}$$

$$\% \text{ error} = \frac{30.52\mu\text{A}}{16\text{mA}} \times 100\%$$

$$= 0.19\% \text{ of span at upper range value.}$$

CONCLUSIONS

Lower Range: From equation (10) it is observed that the predominant error term is the input offset voltage (30 μV for the B grade). This is of little consequence in many applications. $V_{\text{OS RTI}}$ can, however, be nulled using the pot shown in Figures 5 and 6. The result is an error of 0.06% of span instead of 0.13% if span.

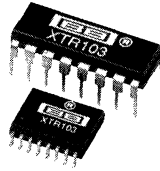
Upper Range: From equation (11), the predominant errors are $I_{\text{OS RTO}}$ (6 μA), $V_{\text{OS RTI}}$ (30 μV), and I_B (150nA), max, B grade. Both I_{OS} and V_{OS} can be trimmed to zero; however, the result is an error of 0.09% of span instead of 0.19% span.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastic, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).

Or, Call Customer Service at 1-800-548-6132 (USA Only)



XTR103

4-20mA Current Transmitter with RTD EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN $\pm 1\%$ TOTAL ADJUSTED ERROR, -40°C TO $+85^{\circ}\text{C}$
- RTD EXCITATION AND LINEARIZATION
- TWO OR THREE-WIRE RTD OPERATION
- WIDE SUPPLY RANGE: 9V to 40V
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

DESCRIPTION

The XTR103 is a monolithic 4-20mA, two-wire current transmitter designed for Platinum RTD temperature sensors. It provides complete RTD current excitation, instrumentation amplifier, linearization, and current output circuitry on a single integrated circuit.

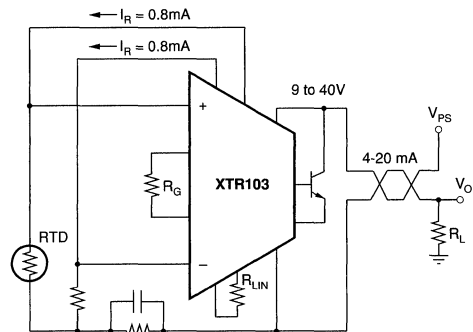
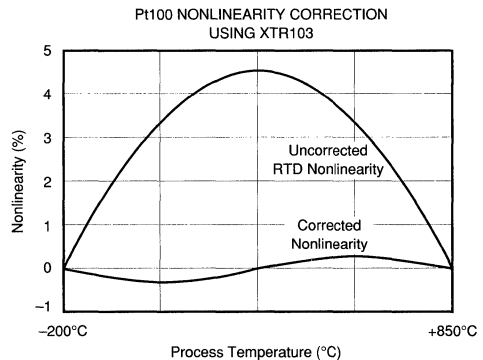
Versatile linearization circuitry provides a 2nd-order correction to the RTD, typically achieving a 40:1 improvement in linearity.

Instrumentation amplifier gain can be configured for a wide range of temperature measurements. Total adjusted error of the complete current transmitter, including the linearized RTD is less than $\pm 1\%$ over the full -40 to $+85^{\circ}\text{C}$ operating temperature range. This includes zero drift, span drift and nonlinearity. The XTR103 operates on loop power supply voltages down to 9V.

The XTR103 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the -40°C to $+85^{\circ}\text{C}$ temperature range.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA



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PDS-1145D

4.215

XTR103

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V₊ = 24V, and 2N6121 external transistor, unless otherwise noted.

PARAMETER	CONDITIONS	XTR103BP/BU			XTR103AP/AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT								
Output Current Equation		$I_o = V_{IN} \cdot (0.016 + 40/R_G) + 4mA$, V _{IN} in Volts, R _G in Ω						A
Total Adjusted Error ⁽¹⁾	T _{MIN} to T _{MAX}		±1			±2		% of FS
Output Current, Specified Range		4	20		*	*		mA
Over-Scale Limit			34	40		*		mA
Under Scale-Limit			3.6	3.8		*		mA
Full Scale Output Error	V _{IN} = 1V, R _G = ∞		±15	±50		*	±100	μA
Noise: 0.1Hz to 1kHz	R _G = 40Ω		8			*		μAp-p
ZERO OUTPUT⁽²⁾								
Initial Error	V _{IN} = 0, R _G = ∞		4			*		mA
vs Temperature			±5	±50		*	±100	μA
vs Supply Voltage, V ₊	V ₊ = 9V to 40V ⁽³⁾		±0.2	±0.5		*	±1	μA/°C
vs Common-Mode Voltage	V _{CM} = 2V to 4V ⁽³⁾		0.5	2		*	*	μA/V
			0.1	2		*	*	μA/V
SPAN								
Span Equation (Transconductance)		$S = 0.016 + 40/R_G$						A/V
Untrimmed Error	R _G ≥ 75Ω		±0.1	±1		*	*	%
vs Temperature ⁽⁴⁾			±20	±50		*	±100	ppm/°C
Nonlinearity: Ideal Input				0.01		*	*	%
RTD Input	Pt100: -200°C to +850°C R _{LIN} = 1127Ω		0.1			*	*	%
INPUT								
Differential Range	R _G = ∞			1		*	*	V
Input Voltage Range ⁽⁵⁾		2		4		*	*	V
Common-Mode Rejection	V _{IN} = 2V to 4V ⁽³⁾	80	100			*	*	dB
Impedance: Differential	Common-Mode		3			*	*	GΩ
			0.5			*	*	GΩ
Offset Voltage			±0.5	±2.5		*	*	mV
vs Temperature			±1	±2.5		±2	±5	μV/°C
vs Supply Voltage, V ₊	V ₊ = 9V to 40V ⁽³⁾	110	130		*	*	*	dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
CURRENT SOURCES⁽⁵⁾								
Current			0.8			*	*	mA
Accuracy			±0.25	±0.5		*	±1	%
vs Temperature			±25	±50		±50	±100	ppm/°C
vs Power Supply, V ₊	V ₊ = 9V to 40V ⁽³⁾		50			*	*	ppm/V
Compliance Voltage ⁽³⁾		(V _{IN}) - 0.2		(V ₊) - 5	*	*	*	V
Matching				±0.5		*	*	%
vs Temperature			±10	±25		*	±50	ppm/°C
vs Power Supply, V ₊	V ₊ = 9V to 40V ⁽³⁾		10			*	*	ppm/V
POWER SUPPLY								
Voltage Range ⁽³⁾ , V ₊		9		40	*	*	*	V
TEMPERATURE RANGE								
Specification, T _{MIN} to T _{MAX}		-40		85	*	*	*	°C
Operating		-40		125	*	*	*	°C
θ _{JA}			80			*	*	°C/W

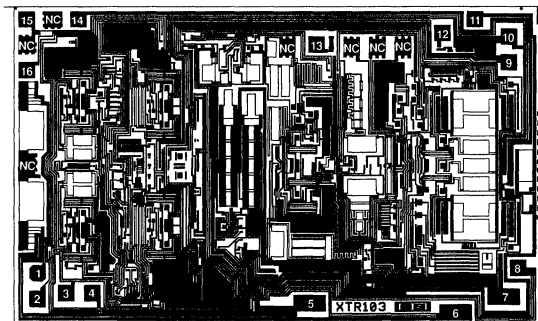
* Specification same as XTR103BP.

NOTES: (1) Includes corrected Pt100 nonlinearity for process measurement spans greater than 100°C, and over-temperature zero and span effects. Does not include initial offset and gain errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale offset current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_o pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) Measured with R_{LIN} = ∞ to disable linearization feature.

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DICE INFORMATION



XTR103 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adj.	9	R_{LIN}
2	Zero Adj.	10	V_+
3	V_{IN}^-	11	E (Emitter)
4	V_{IN}^+	12	I_{R1}
5	R_G	13	I_{R2}
6	R_G	14	E_{INT} (Int. Emit.)
7	I_O	15	B (Base)
8	R_{LIN}	16	Zero Adj.

NC: No Connection

Substrate Bias: Internally connected to the I_O terminal (#7).

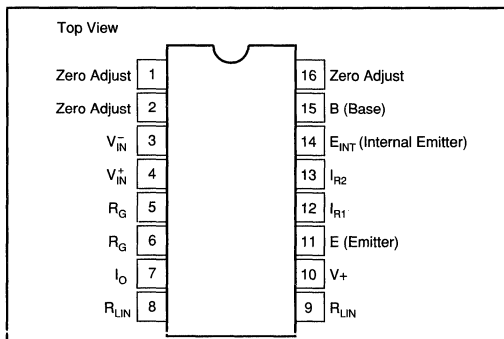
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	168 x 104 ±5	4.27 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

XTR103

4

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply, V_+ (referenced to I_O pin)	40V
Input Voltage, V_{IN}^+ , V_{IN}^- (referenced to I_O pin)	0V to V_+
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Current Limit	Continuous
Junction Temperature	+165°C

ELECTROSTATIC DISCHARGE

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specification.

INSTRUMENTATION AMPLIFIERS

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
XTR103AP	16-pin Plastic DIP	180
XTR103BP	16-pin Plastic DIP	180
XTR103AU	SOL-16 Surface Mount	211
XTR103BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

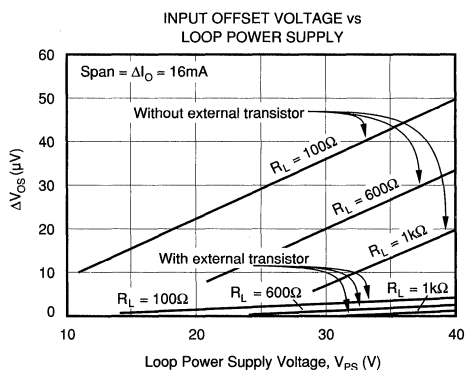
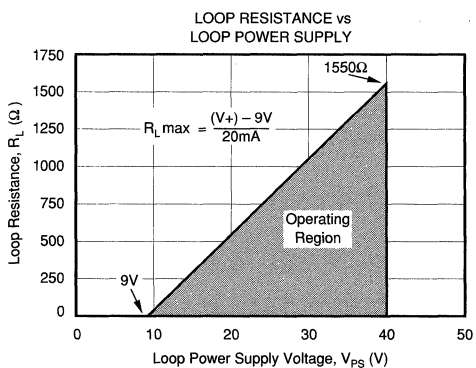
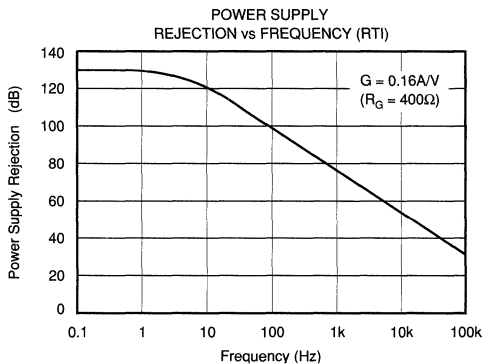
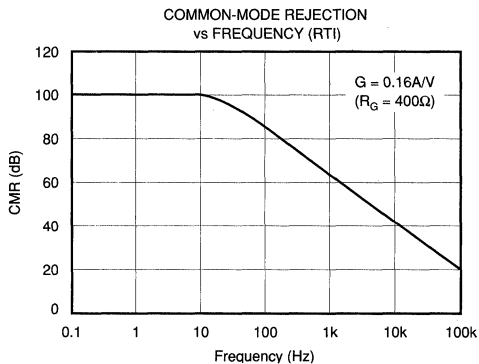
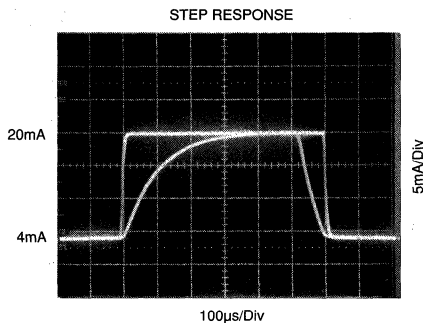
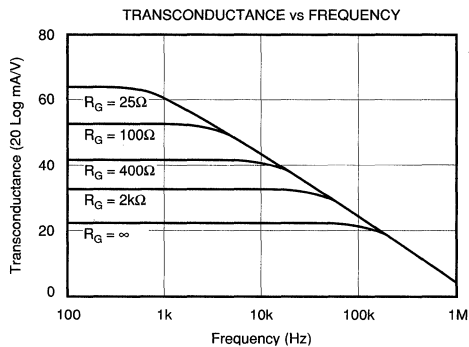
MODEL	PACKAGE	TEMPERATURE RANGE
XTR103AP	16-pin Plastic DIP	-40°C to +85°C
XTR103BP	16-pin Plastic DIP	-40°C to +85°C
XTR103AU	SOL-16 Surface Mount	-40°C to +85°C
XTR103BU	SOL-16 Surface Mount	-40°C to +85°C



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TYPICAL PERFORMANCE CURVES

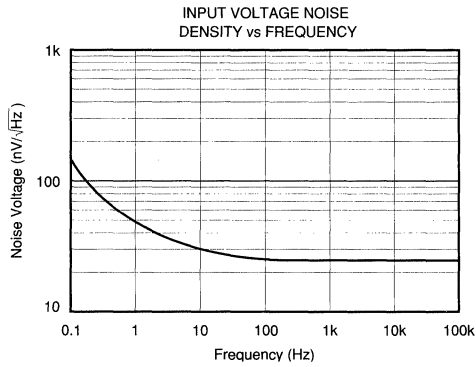
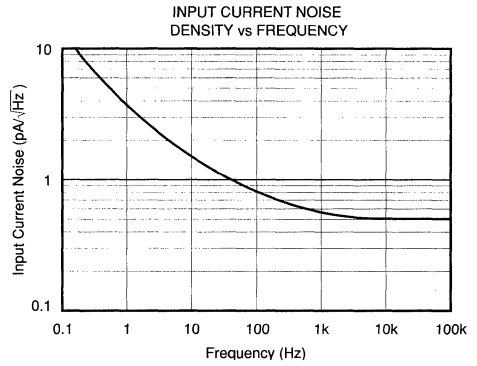
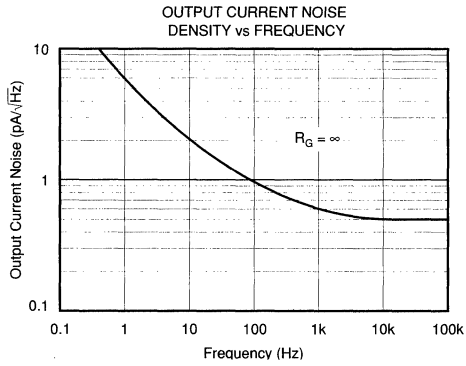
$T_A = +25^\circ\text{C}$, $V_+ = 24\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $+V = 24\text{VDC}$, unless otherwise noted.



XTR103

4

INSTRUMENTATION AMPLIFIERS

APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR103. The loop power supply, V_{FS} provides power for all circuitry. Output loop current is measured as a voltage across the series load resistor, R_L .

Two matched 0.8mA current sources drive the RTD and zero-setting resistor, R_Z . The instrumentation amplifier input of the XTR103 measures the voltage difference between the RTD and R_Z . The value of R_Z is chosen to be equal to the resistance of the RTD at the low-scale (minimum) measurement temperature. R_Z can be adjusted to achieve 4mA output at the minimum measurement temperature to correct for input offset voltage and reference current mismatch of the XTR103.

R_{CM} provides an additional voltage drop to bias the inputs of the XTR103 within their common-mode range. Resistor, R_G , sets the gain of the instrumentation amplifier according to the desired temperature measurement range.

The transfer function through the complete instrumentation amplifier and voltage-to-current converter is:

$$I_o = V_{IN} \cdot (0.016 + 40/R_G) + 4mA,$$

(V_{IN} in volts, R_G in ohms, $R_{LIN} = \infty$)

where V_{IN} is the differential input voltage. With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4-20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4-20mA output current. Other values for R_G can be calculated according to the desired full-scale input voltage, V_{FS} , with the formula in Figure 1.

Negative input voltage, V_{IN} , will cause the output current to be less than 4mA. Increasingly negative V_{IN} will cause the output current to limit at approximately 3.6mA.

Increasingly positive input voltage (greater than V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

EXTERNAL TRANSISTOR

Transistor Q_1 conducts the majority of the signal-dependent 4-20mA loop current. Using an external transistor isolates the majority of the power dissipation from the precision input and reference circuitry of the XTR103, maintaining excellent accuracy.

Since the external transistor is inside a feedback loop its characteristics are not critical. Requirements are: $V_{CEO} = 45V$ min, $\beta = 40$ min and $P_D = 800mW$. Power dissipation requirements may be lower if the loop power supply voltage is less than 40V. Some possible choices for Q_1 are listed in Figure 1.

The XTR103 can be operated without this external transistor by connecting pin 11 to 14 (see Figure 2). Accuracy will be somewhat degraded by the additional internal power dissipation. This effect is most pronounced when the input stage is set for high gain (for low full-scale input voltage). The typical performance curve "Input Offset Voltage vs Loop Supply Voltage" describes this behavior.

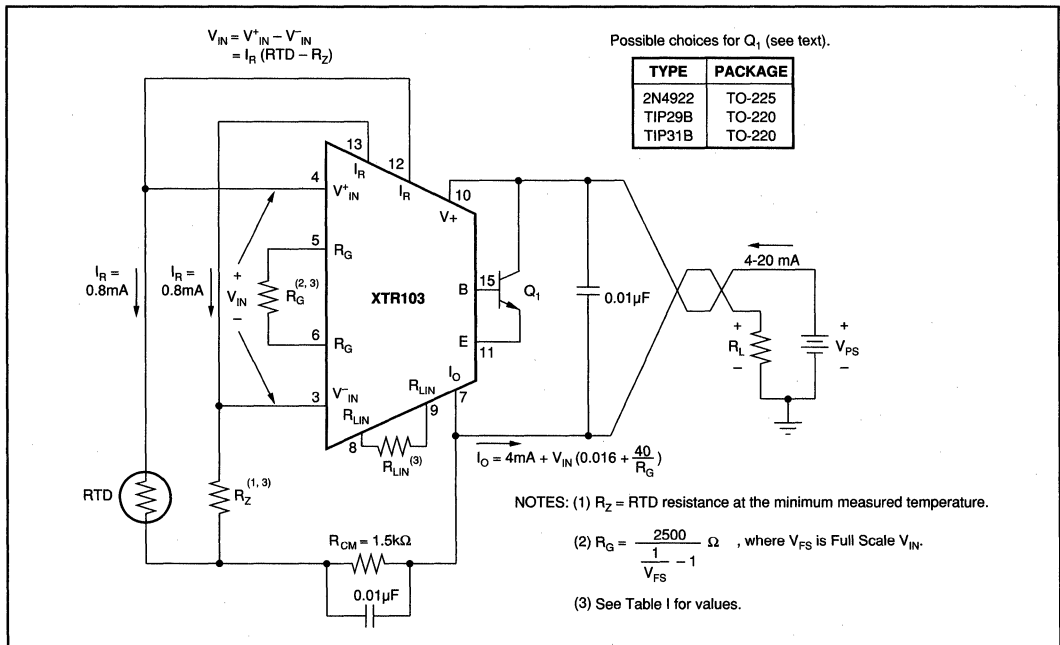


FIGURE 1. Basic RTD Temperature Measurement Circuit.

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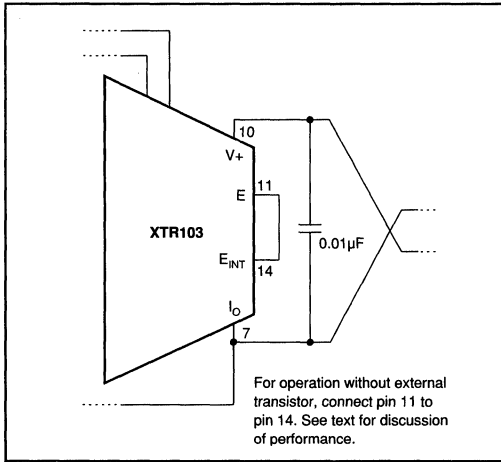


FIGURE 2. Operation Without External Transistor.

LOOP POWER SUPPLY

The voltage applied to the XTR103, V+, is measured with respect to the I_O connection, pin 7. V+ can range from 9V to 40V. The loop supply voltage, V_{PS}, will differ from the voltage applied to the XTR103 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop supply voltage is used, R_L must be made a relatively low value to assure that V+ remains 9V or greater for the maximum loop current of 20mA. It may, in fact, be prudent to design for V+ equal or greater than 9V with loop currents up to 34mA to allow for out-of-range input conditions. The typical performance curve "Loop Resistance vs Loop Power Supply" shows the allowable sense resistor values for full-scale 20mA.

The low operating voltage (9V) of the XTR103 allows operation directly from personal computer power supplies (12V ±5%). When used with the RCV420 Current Loop Receiver (Figure 8), load resistor voltage drop is limited to 1.5V.

LINEARIZATION

On-chip linearization circuitry creates a signal-dependent variation in the two matching current sources. Both current sources are varied equally according to the following equation:

$$I_{R1} = I_{R2} = 0.8 + \frac{500 \cdot V_{IN}}{R_{LIN}}$$

(I_R in mA, V_{IN} in volts, R_{LIN} in ohms)
(maximum I_R = 1.0mA)

This varying excitation provides a 2nd-order term to the transfer function (including the RTD) which can correct the RTD's nonlinearity. The correction is controlled by resistor R_{LIN} which is chosen according to the desired temperature measurement range. Table I provides the R_G, R_Z and R_{LIN} resistor values for a Pt100 RTD.

If no linearity correction is desired, do not connect a resistor to the R_{LIN} pins (R_{LIN} = ∞). This will cause the excitation current sources to remain a constant 0.8mA.

ADJUSTING INITIAL ERRORS

Most applications will require adjustment of initial errors. Offset errors can be corrected by adjustment of the zero resistor, R_Z.

Figure 3 shows another way to adjust zero errors using the output current adjustment pins of the XTR103. This provides a minimum of ±300µA (typically ±500µA) adjustment around the initial low-scale output current. This is an output current adjustment which is independent of the input stage

MEASUREMENT TEMPERATURE SPAN ΔT (°C)										
T _{MIN}	100°C	200°C	300°C	400°C	500°C	600°C	700°C	800°C	900°C	1000°C
-200°C	18/90 653	18/185 838	18/286 996	18/396 1087	18/515 1131	18/645 1152	18/788 1159	18/946 1158	18/1120 1154	18/1317 1140
-100°C	60/84 1105	60/173 1229	60/270 1251	60/374 1249	60/487 1231	60/610 1207	60/746 1181	60/895 1155	60/1061 1128	
0°C	100/81 1287	100/167 1258	100/260 1229	100/361 1201	100/469 1173	100/588 1145	100/718 1117	100/860 1089		
100°C	138/78 1211	138/162 1183	138/252 1155	138/349 1127	138/453 1100	138/567 1073	138/691 1046			
200°C	175/76 1137	175/157 1110	175/244 1083	175/337 1056	175/437 1030	175/546 1003				
300°C	212/73 1066	212/152 1039	212/235 1013	212/325 987	212/422 962					
400°C	247/71 996	247/146 971	247/227 946	247/313 921						
500°C	280/68 930	280/141 905	280/219 881							
600°C	313/66 865	313/136 841								
700°C	345/64 803									
800°C	375/61 743									

R_Z/R_G
R_{LIN} (Values are in Ω.)

NOTE: Values shown are for a Pt100 RTD.
Double (x2) all values for Pt200.

TABLE I. R_Z, R_G and R_{LIN} Resistor Values for Pt100 RTD.



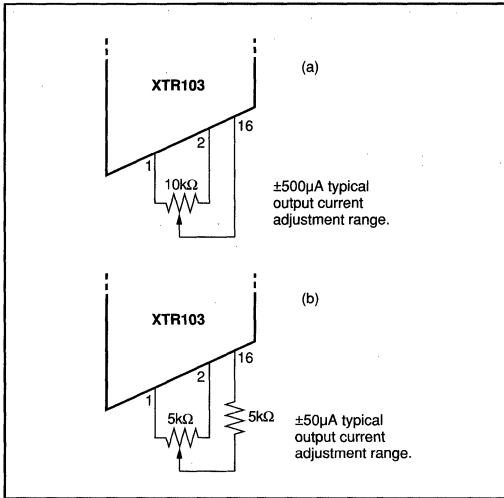


FIGURE 3. Low-scale Output Current Adjustment.

gain set with R_G . If the input stage is set for high gain (as required with narrow temperature measurement spans) the output current adjustment may not provide sufficient range. In these cases, offset can be nulled by adjusting the value of R_Z .

TWO-WIRE AND THREE-WIRE RTD CONNECTIONS

In Figure 1, the RTD can be located remotely simply by extending the two connections to the RTD. With this two-wire connection to the RTD, line resistance will introduce

error. This error can be partially corrected by adjusting the values of R_Z , R_G , and R_{LIN} .

Figure 4, shows a three-wire RTD connection for improved accuracy with remotely located RTDs. R_Z 's current is routed through a third wire to the RTD. Assuming line resistance is equal in RTD lines 1 and 2, this produces a small common-mode voltage which is rejected by the XTR103.

OPEN-CIRCUIT DETECTION

The optional transistor Q_2 in Figure 4 provides predictable behavior with open-circuit RTD connections. It assures that if any one of the three RTD connections is broken, the XTR103's output current will go to either its high current limit ($\approx 34\text{mA}$) or low current limit ($\approx 3.6\text{mA}$). This is easily detected as an out-of-range condition.

REVERSE-VOLTAGE PROTECTION

Figure 5 shows two ways to protect against reversed output connection lines. Trade-offs in an application will determine which technique is better. D_1 offers series protection, but causes a 0.7V loss in loop supply voltage. This may be undesirable if $V+$ can approach the 9V limit. Using D_2 (without D_1) has no voltage loss, but high current will flow in the loop supply if the leads are reversed. This could damage the power supply or the sense resistor, R_L . A diode with a higher current rating is needed for D_2 to withstand the highest current that could occur with reversed lines.

SURGE PROTECTION

Long lines are subject to voltage surges which can damage semiconductor components. To avoid damage, the maximum applied voltage rating for the XTR103 is 40V. A zener

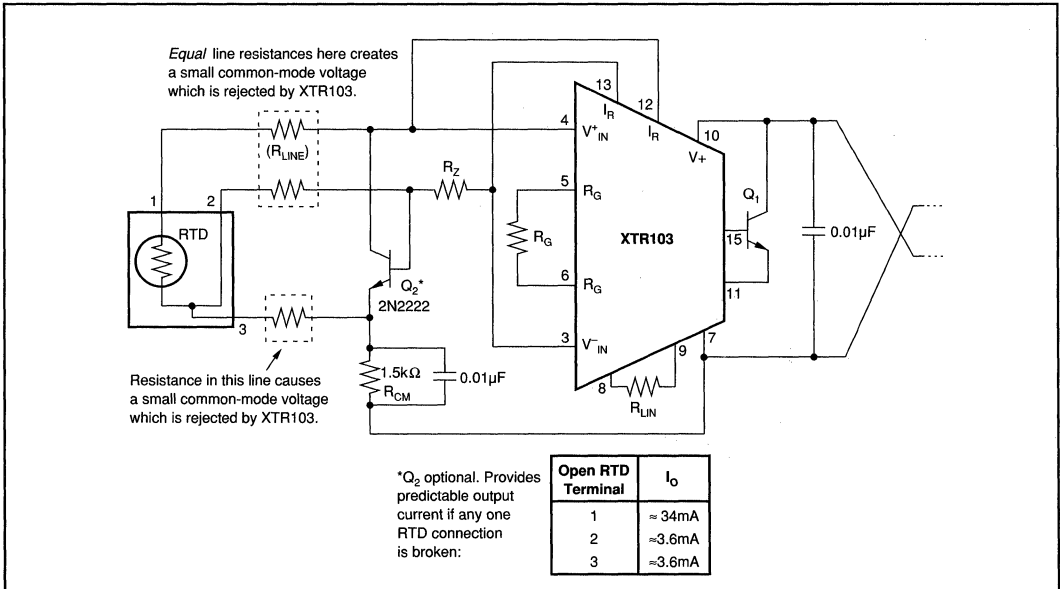


FIGURE 4. Three-Wire Connection for Remotely Located RTDs.

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diode may be used for D_2 (Figure 6) to clamp the voltage applied to the XTR103 to a safe level. The loop power supply voltage must be lower than the voltage rating of the zener diode.

There are special zener diode types specifically designed to provide a very low impedance clamp and withstand large energy surges. These devices normally have a diode characteristic in the forward direction which also protects against reversed loop connections. As noted earlier, reversed loop connections would produce a large loop current, possibly damaging R_L .

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF can be rectified by the sensitive input circuitry of the XTR103 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the RTD sensor is remotely located, the interference may enter at the input terminals. For integrated transmitter assemblies with short connection to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input often reduce or eliminate this interference. Connect these bypass capacitors to the I_O terminal as shown in Figure 7. Although the DC voltage at the I_O terminal is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter's "ground".

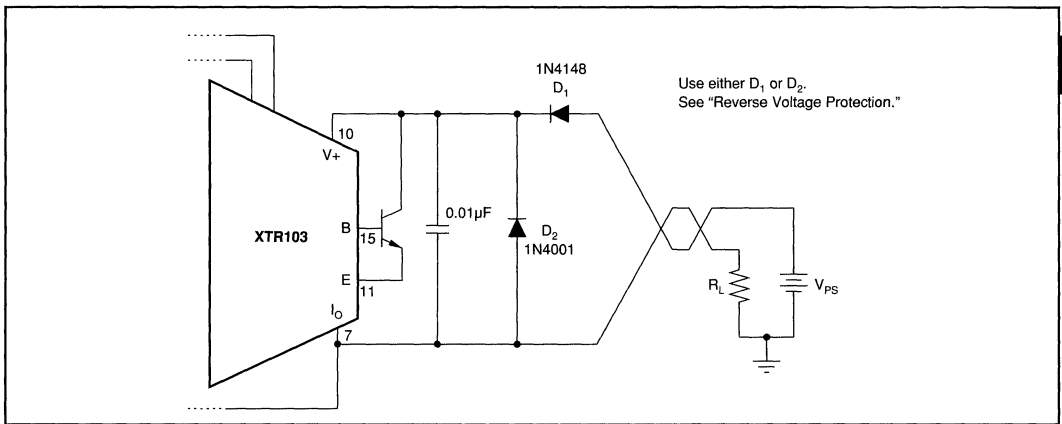


FIGURE 5. Reverse Voltage Protection.

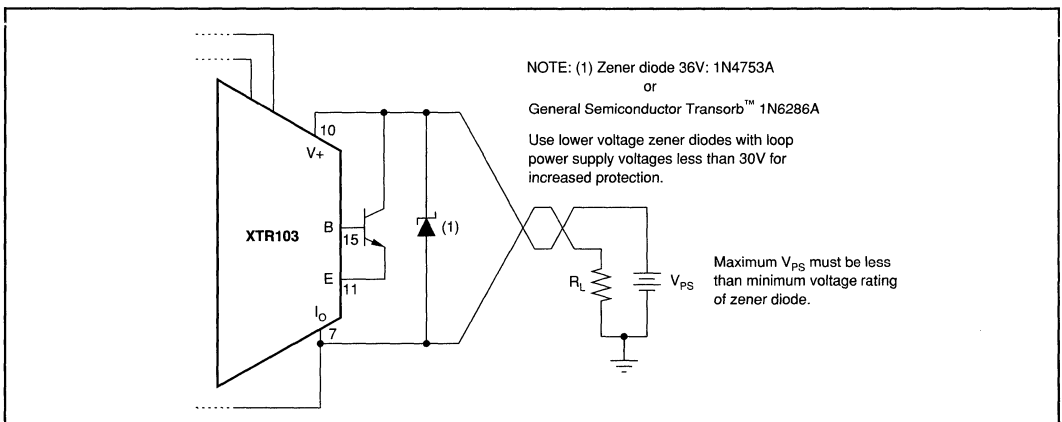


FIGURE 6. Over-Voltage Surge Protection.

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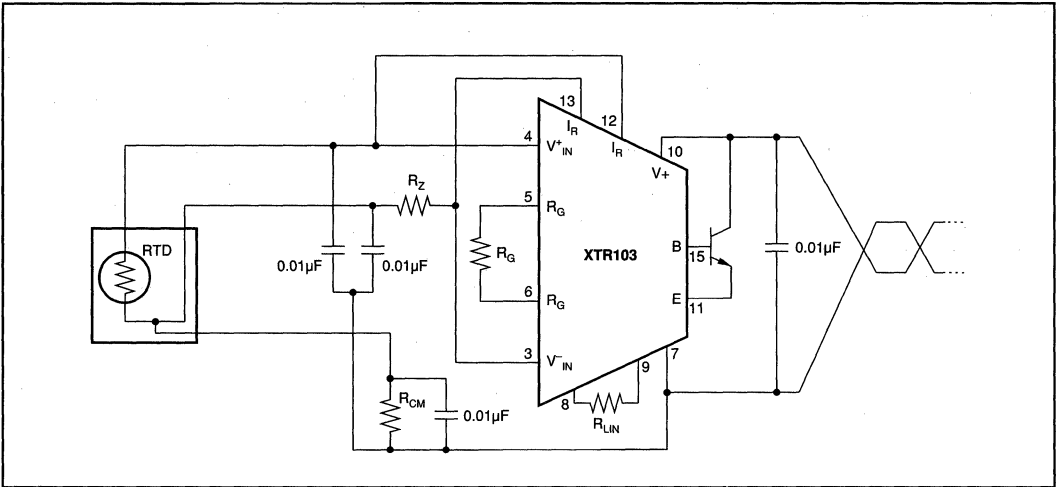


FIGURE 7. Input Bypassing Techniques.

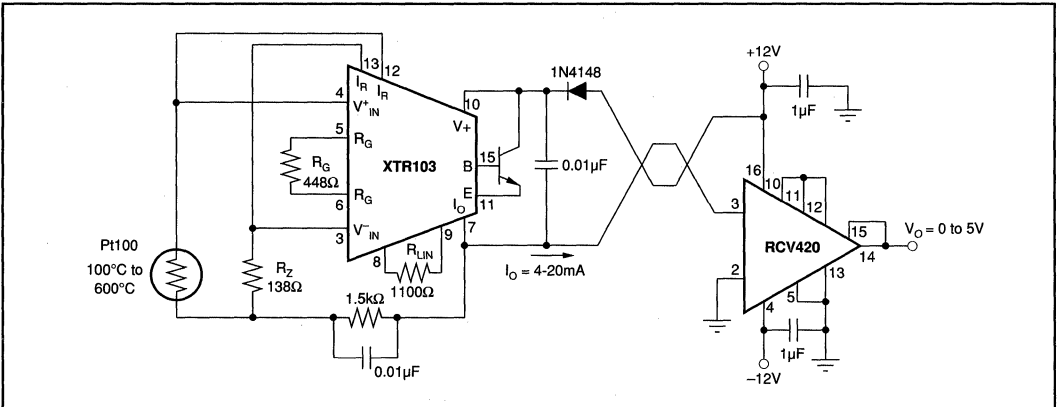


FIGURE 8. $\pm 12V$ -Powered Transmitter/Receiver Loop.

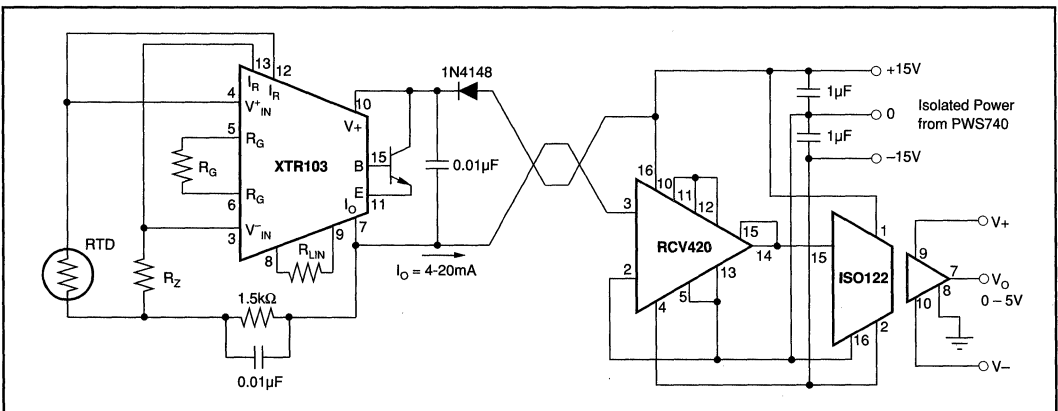
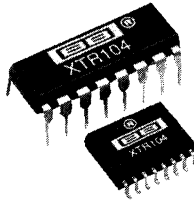


FIGURE 9. Isolated Transmitter/Receiver Loop.

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XTR104

4-20mA Current Transmitter with BRIDGE EXCITATION AND LINEARIZATION

FEATURES

- LESS THAN $\pm 1\%$ TOTAL ADJUSTED ERROR, -40°C TO $+85^{\circ}\text{C}$
- BRIDGE EXCITATION AND LINEARIZATION
- WIDE SUPPLY RANGE: 9V to 40V
- LOW SPAN DRIFT: 50ppm/ $^{\circ}\text{C}$ max
- HIGH PSR: 110dB min
- HIGH CMR: 80dB min

DESCRIPTION

The XTR104 is a monolithic 4-20mA, two-wire current transmitter integrated circuit designed for bridge input signals. It provides complete bridge excitation, instrumentation amplifier, linearization, and current output circuitry necessary for high impedance strain gage sensors.

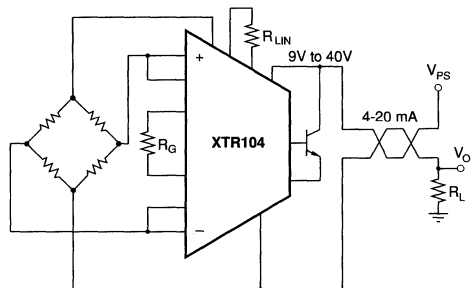
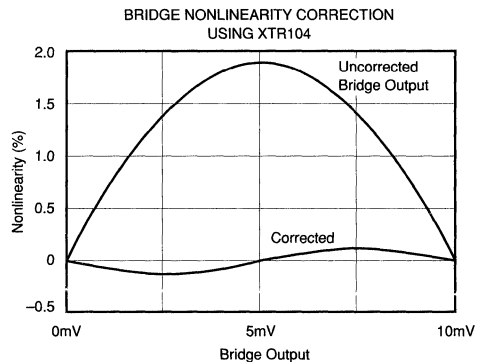
The instrumentation amplifier can be used over a wide range of gain, accommodating a variety of input signals and sensors. Total adjusted error of the complete current transmitter, including the linearized bridge is less than $\pm 1\%$ over the full -40°C to $+85^{\circ}\text{C}$ temperature range. This includes zero drift, span drift and non-linearity for bridge outputs as low as 10mV. The XTR104 operates on loop power supply voltages down to 9V.

Linearization circuitry consists of a second, fully independent instrumentation amplifier that controls the bridge excitation voltage. It provides second-order correction to the transfer function, typically achieving a 20:1 improvement in nonlinearity, even with low cost transducers.

The XTR104 is available in 16-pin plastic DIP and SOL-16 surface-mount packages specified for the -40°C to $+85^{\circ}\text{C}$ temperature range.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- FACTORY AUTOMATION
- SCADA
- WEIGHTING SYSTEMS
- ACCELEROMETERS



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PDS-1146B

4.225

XTR104

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

T_A = +25°C, V₊ = 24V, and 2N6121 external transistor, unless otherwise noted.

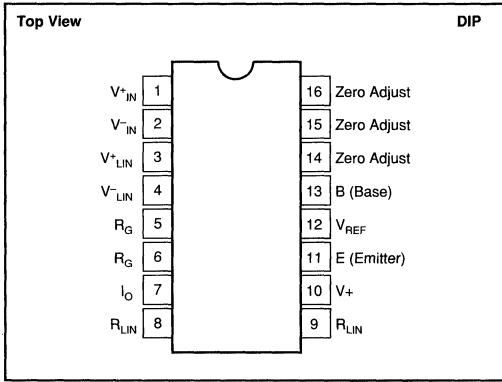
PARAMETER	CONDITIONS	XTR104BP, BU			XTR104AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT								
Output Current Equation		$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4\text{mA}$			V_{IN} in Volts, R_G in Ω			A
Total Adjusted Error ⁽¹⁾	T _{MIN} to T _{MAX} , V _{FS} ≥ 10mV, R _G = 5k Ω		±1				±2	% of FS
Current, Specified Range		4		20	*		*	mA
Over-Scale Limit			34	40		*	*	mA
Under Scale-Limit			3.6	3.8		*	*	mA
Full Scale Output Error	V _{IN} = 1V, R _G = ∞		±15	±50			±100	μ A
Noise: 0.1Hz to 1kHz	R _G = 40k Ω		8				*	μ Ap-p
ZERO OUTPUT⁽²⁾								
Initial Error	V _{IN} = 0V, R _G = ∞		4				*	mA
vs Temperature			±5	±50			±100	μ A
vs Supply Voltage, V ₊	V ₊ = 9V to 40V ⁽³⁾		±0.2	±0.5			±1	μ A/°C
vs Common-Mode Voltage	V _{CM} = 2V to 3V ⁽³⁾		0.5	2			*	μ A/V
			0.1	2			*	μ A/V
SPAN								
Span Equation (Transconductance)		$S = 0.016 + 40/R_G$					*	A/V
Untrimmed Error	R _G ≥ 75k Ω		±0.1	±1			*	%
vs Temperature ⁽⁴⁾			±20	±50			±100	ppm/°C
Nonlinearity: Ideal Input				0.01			*	%
Bridge Input ⁽⁵⁾			0.1				*	%
INPUT								
Differential Range				1			*	V
Input Voltage Range ⁽³⁾		2		3	*		*	V
Common-Mode Rejection	V _{IN} = 2V to 3V ⁽³⁾	80	100	3	*	*	*	dB
vs Temperature			3			*	*	dB
vs Supply Voltage, V ₊			0.5			*	*	G Ω
vs Common-Mode Voltage			0.5			*	*	G Ω
Offset Voltage			±0.5	±2.5			*	mV
vs Temperature			1	2.5		2	5	μ V/°C
vs Supply Voltage, V ₊	V ₊ = 9V to 40V ⁽³⁾	110	130	250	*	*	*	dB
Input Bias Current			100	250		*	*	nA
vs Temperature			0.1	2		*	*	nA/°C
Input Offset Current			2	20		*	*	nA
vs Temperature			0.01	0.25		*	*	nA/°C
VOLTAGE REFERENCE⁽⁶⁾								
Voltage Accuracy			5				*	V
vs Temperature			±0.25	±0.5			±1	%
vs Supply Voltage, V ₊	V ₊ = 9V to 40V ⁽³⁾		±10	±50			±100	ppm/°C
vs Load	I _L = 0 to 2mA		5				*	ppm/V
			50				*	ppm/mA
POWER SUPPLY								
Voltage Range ⁽³⁾ , V ₊		9		40	*		*	V
TEMPERATURE RANGE								
Specification	(T _{MIN} to T _{MAX})	-40		85	*		*	°C
Operating	Derated Performance	-40		125	*		*	°C
θ_{JA}			80				*	°C/W

* Specification same as XTR104BP.

NOTES: (1) Includes corrected second-order nonlinearity of bridge, and over-temperature zero and span effects. Does not include initial offset and span errors which are normally trimmed to zero at 25°C. (2) Describes accuracy of the 4mA low-scale current. Does not include input amplifier effects. Can be trimmed to zero. (3) Voltage measured with respect to I_O pin. (4) Does not include TCR of gain-setting resistor, R_G. (5) When configured to correct for ≤2% second-order bridge sensor nonlinearity. (6) Measured with R_{IN} = ∞ to disable linearization feature.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply, V+ (referenced to I _O pin)	40V
Input Voltage, V _{IN} , V _{INT} , V _{LIN} , V _{LN} (referenced to I _O pin)	0V to V+
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Current Limit	Continuous
Junction Temperature	+165°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
XTR104AP	16-Pin Plastic DIP	180
XTR104BP	16-Pin Plastic DIP	180
XTR104AU	SOL-16 Surface Mount	211
XTR104BU	SOL-16 Surface Mount	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR104AP	16-pin Plastic DIP	-40°C to +85°C
XTR104BP	16-pin Plastic DIP	-40°C to +85°C
XTR104AU	SOL-16 Surface Mount	-40°C to +85°C
XTR104BU	SOL-16 Surface Mount	-40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

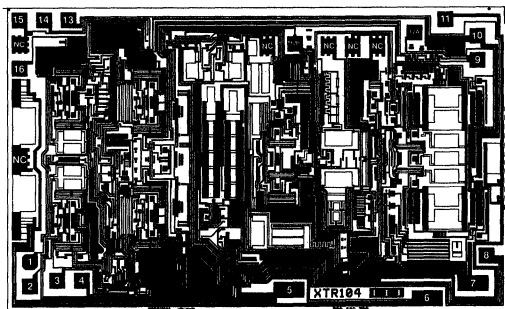
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specification.

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DICE INFORMATION



XTR104 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{IN}^-	9	R_{LIN}
2	V_{IN}^+	10	V_+
3	V_{LIN}^-	11	E (Emitter)
4	V_{LIN}^+	12A, 12B	V_{REF}
5	R_G	13	B (Base)
6	R_G	14	Zero Adj.
7	I_D	15	Zero Adj.
8	R_{LIN}	16	Zero Adj.

Pads 12A and 12B must be connected.

NC: No Connection

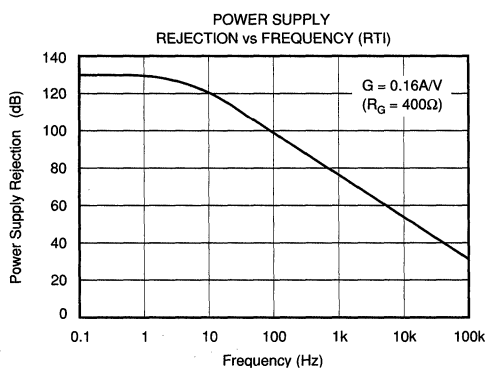
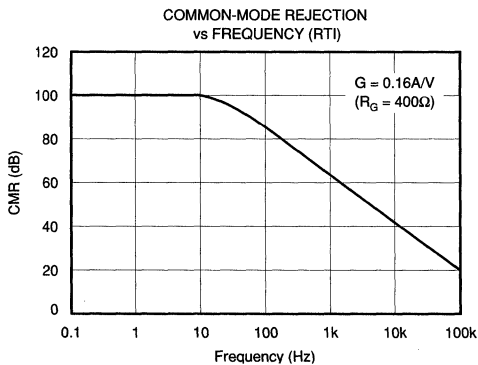
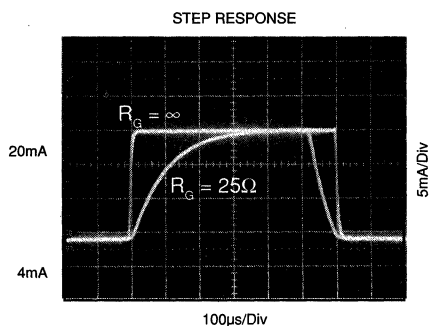
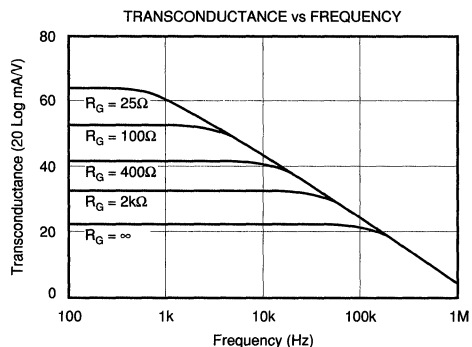
Substrate Bias: Internally connected to the I_D terminal (#7).

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	168 x 104 ±5	4.27 x 2.64 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

TYPICAL PERFORMANCE CURVES

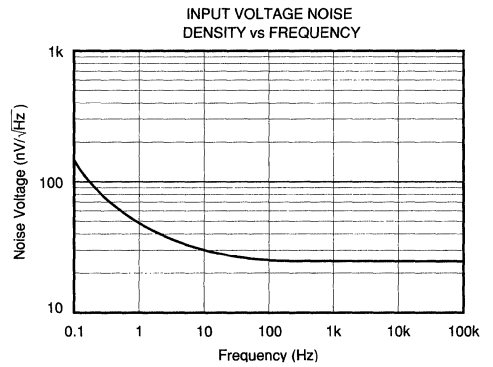
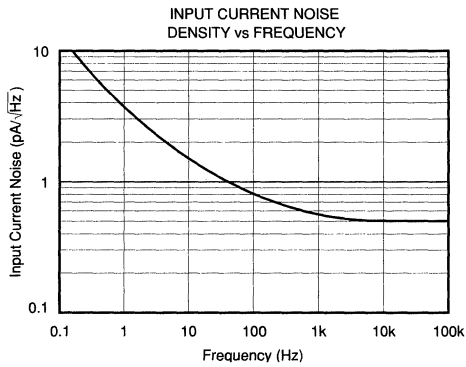
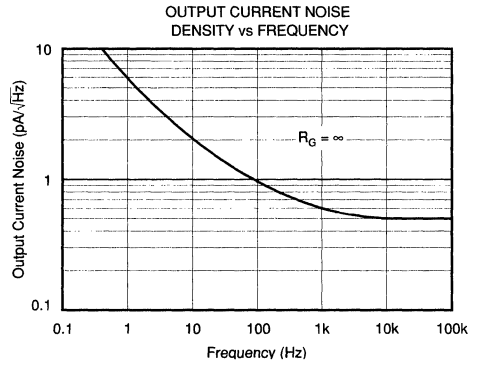
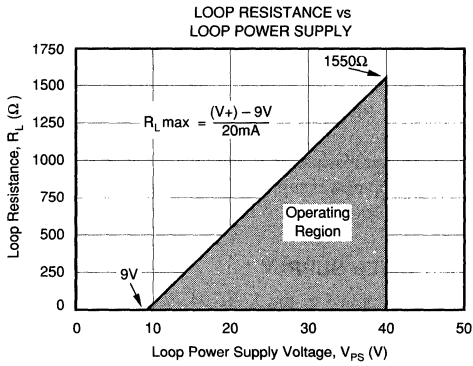
$T_A = +25^\circ\text{C}$, $V_+ = 24\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $+V = 24\text{V}$, unless otherwise noted.



XTR104

4

INSTRUMENTATION AMPLIFIERS

APPLICATION INFORMATION

Figure 1 shows the basic connection diagram for the XTR104. The loop power supply, V_{PS} , provides power for all circuitry. Loop current is measured as a voltage across the series load resistor, R_L .

A high impedance ($\geq 2750\Omega$) strain gage sensor can be excited directly by the 5V reference output terminal, V_R . The output terminals of the bridge are connected to the instrumentation amplifier inputs, V_{IN}^+ and V_{IN}^- . The resistor, R_G , sets the gain of the instrumentation amplifier as required by the full-scale bridge voltage, V_{FS} .

The transfer function is:

$$I_O = V_{IN} \cdot (0.016 + 40/R_G) + 4mA, \quad (1)$$

Where: V_{IN} is the voltage applied to the V_{IN}^+ and V_{IN}^- differential inputs (in Volts.) R_G in Ω .

With no R_G connected ($R_G = \infty$), a 0V to 1V input produces a 4 to 20mA output current. With $R_G = 25\Omega$, a 0V to 10mV input produces a 4 to 20mA output current. Other values for R_G can be calculated as follows:

$$R_G = \frac{2500}{\frac{1}{V_{FS}} - 1} \quad (2)$$

Where: V_{FS} is the full scale voltage applied to the V_{IN}^+ and V_{IN}^- differential inputs (in Volts).

R_G in Ω .

Under-scale input voltage (negative) will cause the output current to decrease below 4mA. Increasingly negative input will cause the output current to limit at approximately 3.6mA.

Increasingly positive input voltage (above V_{FS}) will produce increasing output current according to the transfer function, up to the output current limit of approximately 34mA.

EXTERNAL TRANSISTOR

Transistor Q_1 conducts the majority of the signal-dependent 4 to 20mA loop current. Using an external transistor isolates the power dissipation from the precision input and reference circuitry of the XTR104, maintaining excellent accuracy.

Since the external transistor is inside a feedback loop its characteristics are not critical. Many common NPN types can be used. Requirements for operation at the full loop supply voltage are: $V_{CEO} = 45V$ min, $\beta = 40$ min and $P_D = 800mW$. Power dissipation requirements may be lower if the maximum loop power supply voltage is less than 40V. Some possible choices for Q_1 are listed in Figure 1.

LOOP POWER SUPPLY

The voltage applied to the XTR104, $V+$, is measured with respect to the I_O connection, pin 7. $V+$ can range from 9V to 40V. The loop supply voltage, V_{PS} , will differ from the voltage applied to the XTR104 according to the voltage drop on the current sensing resistor, R_L (plus any other voltage drop in the line).

If a low loop supply voltage is used, R_L must be made a relatively low value to assure that $V+$ remains 9V or greater for the maximum loop current of 20mA. It may, in fact, be prudent to design for $V+$ equal or greater than 9V with loop currents up to 34mA to allow for out-of-range input conditions. The typical performance curve "Loop Resistance vs Loop Power Supply" shows the allowable sense resistor values for full-scale 20mA.

The low operating voltage (9V) of the XTR104 allows operation directly from personal computer power supplies ($12V \pm 5\%$). When used with the RCV420 Current Loop Receiver (see Figure 9), load resistor voltage drop is only 1.5V at 20mA.

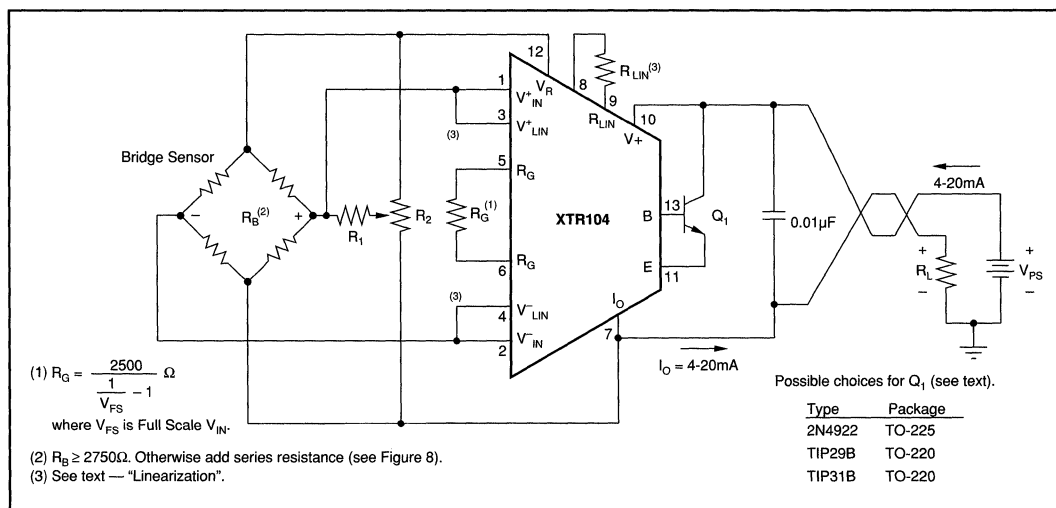


FIGURE 1. Bridge Sensor Application, Connected for Positive Nonlinearity.

BRIDGE BALANCE

Figure 1 shows a bridge trim circuit (R_1 , R_2). This adjustment can be used to compensate for the initial accuracy of the bridge and/or to trim the offset voltage of the XTR104. The values of R_1 and R_2 depend on the impedance of the bridge, and the trim range required. This trim circuit places an additional load on the V_R output. The effective load of the trim circuit is nearly equal to R_2 . Total load on the V_R output terminal must not exceed 2mA. An approximate value for R_1 can be calculated:

$$R_1 \approx \frac{5V \cdot R_B}{4 \cdot V_{TRIM}} \quad (3)$$

Where: R_B is the resistance of the bridge.

V_{TRIM} is the desired \pm voltage trim range (in V).

Make R_2 equal or lower in value to R_1 .

Figure 2 shows another way to adjust zero errors using the output current adjustment pins of the XTR104. This provides $\pm 500\mu A$ (typical) adjustment around the initial low-scale output current. This is an output current adjustment that is independent of the input stage gain set with R_G . If the input stage is set for high gain the output current adjustment may not provide sufficient range.

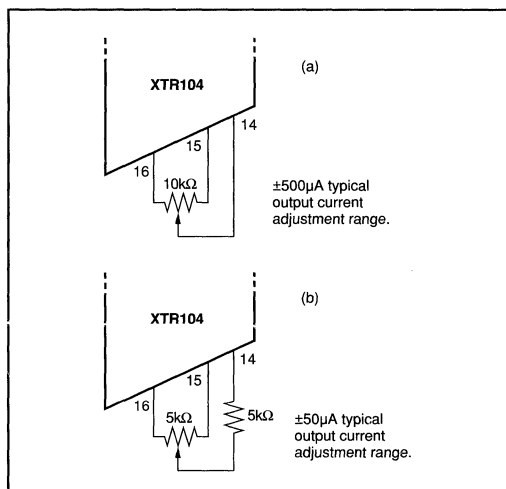


FIGURE 2. Low-scale Output Current Adjustment.

LINEARIZATION

Differential voltage applied to the linearization inputs, V_{LIN}^+ and V_{LIN}^- , causes the reference (excitation) voltage, V_R , to vary according to the following equation:

$$V_R = 5V + V_{LIN} \frac{K_{LIN}}{R_{LIN}} \quad (4)$$

Where: V_{LIN} is the voltage applied to the V_{LIN}^+ and V_{LIN}^- differential inputs (in V).

R_{LIN} in Ω .

$K_{LIN} \approx 24000$ (approximately $\pm 20\%$ depending on variations in the fabrication of the XTR104).

With V_{LIN}^+ and V_{LIN}^- connected to the bridge output, the bridge excitation voltage can be made to vary as much as $\pm 0.5V$ in response to the bridge output voltage. Be sure that the total load on the V_R output is less than 2mA at the maximum excitation voltage, $V_R = 5.5V$.

Signal-dependent variation of the bridge excitation voltage provides a second-order term to the complete transfer function (including the bridge). This can be tailored to correct for bridge sensor nonlinearity. Either polarity of nonlinearity (bowing up or down) can be compensated by proper connection of the V_{LIN} inputs. Connecting V_{LIN}^+ to V_{IN}^+ and V_{LIN}^- to V_{IN}^- (Figure 1) causes V_R to increase with bridge output which compensates for a positive bow in the bridge response. Reversing the connections (Figure 3) causes V_R to decrease with increasing bridge output, to compensate for negative-bowing nonlinearity.

To determine the required value for R_{LIN} you must know the nonlinearity of the bridge sensor with constant excitation voltage. The linearization circuitry can only compensate for the parabolic portion of a sensor's nonlinearity. Parabolic nonlinearity has a maximum deviation from linear occurring at mid-scale (see Figure 4). Sensors with nonlinearity curves similar to that shown in Figure 4, but not peaking exactly at mid-scale can be substantially improved. A nonlinearity that is perfectly "S-shaped" (equal positive and negative nonlinearity) cannot be corrected with the XTR104. It may, however, be possible to improve the worst-case nonlinearity of a sensor by equalizing the positive and negative nonlinearity.

The nonlinearity, B (in % of full scale), is positive or negative depending on the direction of the bow. A maximum of $\pm 2.5\%$ nonlinearity can be corrected. An approximate value for R_{LIN} can be calculated by:

$$R_{LIN} = \frac{K_{LIN} \cdot V_{FS}}{0.2 \cdot B} \quad (5)$$

Where: $K_{LIN} \approx 24000$.

V_{FS} is the full-scale bridge output (in Volts) with constant 5V excitation.

B is the parabolic nonlinearity in $\pm\%$ of full scale. R_{LIN} in Ω .

Methods for refining this calculation involve determining the actual value of K_{LIN} for a particular device (explained later).

B is a signed number (negative for a downward-bowing nonlinearity). This can produce a negative value for R_{LIN} . In this case, use the resistor value indicated (ignore the sign), but connect V_{LIN}^+ to V_{IN}^- and V_{LIN}^- to V_{IN}^+ as shown in Figure 3.

This approximate calculation of R_{LIN} generally provides about a 5:1 improvement in bridge nonlinearity.

Example: The bridge sensor depicted by the negative-bowing curve in Figure 4. Its full scale output is 10mV with constant 5V excitation. Its maximum nonlinearity, B, is -1.9% referred to full scale (occurring at mid-scale). Using equation 5:

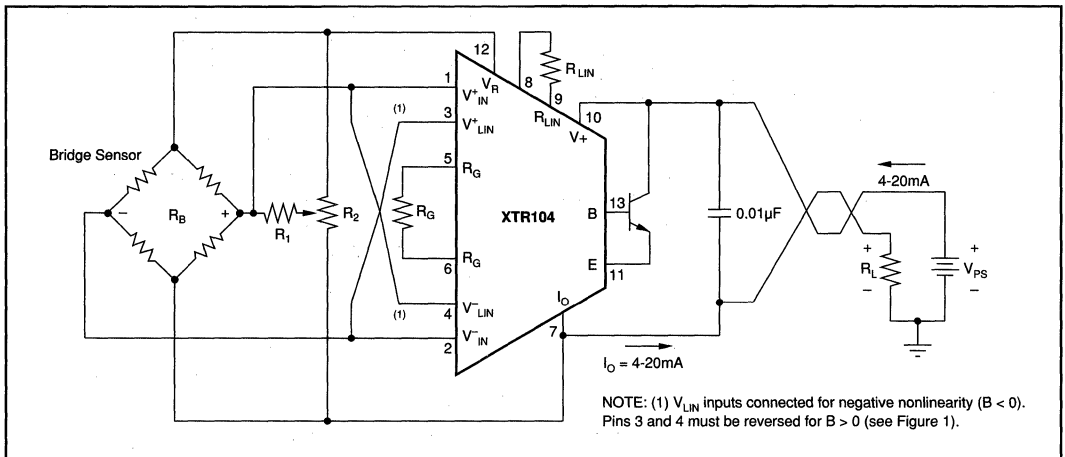


FIGURE 3. Bridge Sensor, V_{LIN} Connected for Negative Nonlinearity.

$$R_{LIN} \approx \frac{24000 \cdot 0.01}{0.2 \cdot (-1.9)} = -632 \Omega$$

Use $R_{LIN} = 632\Omega$. Because the calculation yields a negative result, connect V_{LIN}^+ to V_{IN}^- and V_{LIN}^- to V_{IN}^+ .

Gain is affected by the varying the excitation voltage. For each 1% of corrected nonlinearity, the gain must be altered by 4%. As a result, equation 2 will not provide an accurate R_G when nonlinearity correction is used. The following equation calculates the required value for R_G to compensate for this effect.

$$R_G = \frac{2500}{\frac{1}{(1 + 0.04 \cdot B) V_{IS}} - 1} \quad (6)$$

B must again be a signed number in this calculation—positive for positive bowing nonlinearity, and negative for a negative-bowing nonlinearity.

$$R_G = 23.32\Omega \text{ for the example above.}$$

A more accurate value for R_{LIN} can be determined by first measuring the actual gain constant of the linearization inputs, K_{LIN} (see equation 4). Measure the change in the reference voltage, ΔV_R , in response to a measured voltage change at the linearization inputs, ΔV_{LIN} . Make this measurement with a known, temporary test value for R_{LIN} . These measurements can be made during operation of the circuit by providing stimulus to the bridge sensor, or by temporarily unbalancing the bridge with a fixed resistor in parallel with one of the bridge resistors. Calculate the actual K_{LIN} :

$$K_{LIN} = \frac{\Delta V_R \cdot R_{TEST}}{\Delta V_{LIN}} \quad (7)$$

Where: ΔV_{LIN} is the change in voltage at V_{LIN} .
 ΔV_R is the measured change in reference voltage, V_R .
 R_{TEST} is a temporary fixed value of R_{LIN} (in Ω).

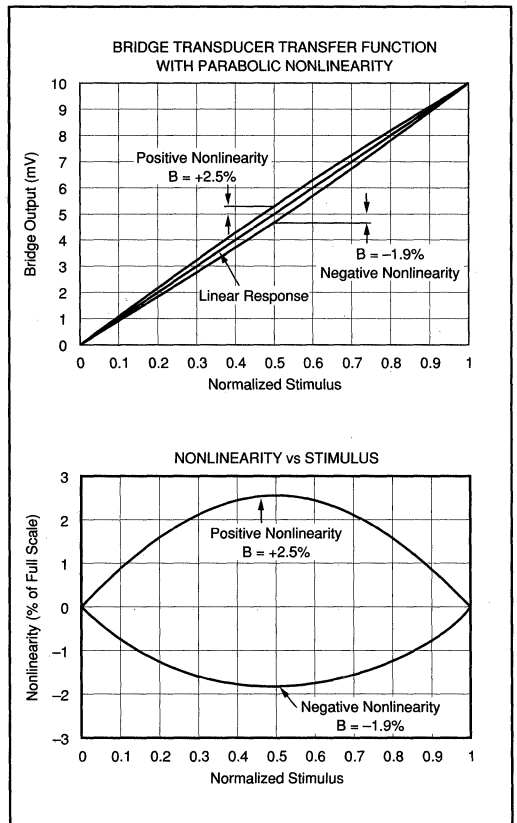


FIGURE 4. Parabolic Nonlinearity.

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Then, R_{LIN} can be calculated using equation 5 using the accurate value of K_{LIN} from equation 7. K_{LIN} can be a different value for each XTR104.

It is also possible to make a real-time adjustment of R_{LIN} with a variable resistor (active circuit trimming). This is done by measuring the change in V_R in response to a zero-to- V_{FS} change in voltage applied to the V_{LIN} inputs. To correct for each 1% of nonlinearity, the excitation voltage, V_R , must make a 4% change at full-scale input. So the change in reference voltage, ΔV_R , for a full-scale change in V_{LIN} can be calculated by:

$$\Delta V_R = 0.2 \cdot B \quad (8)$$

Example: A bridge sensor has a -1.9% nonlinearity. Apply the full-scale bridge output, V_{FS} (10mV), to the V_{LIN} inputs and adjust R_{LIN} for:

$$V_R' = 5V + 0.2 \cdot B = 4.62V$$

Note that with all the calculation and adjustment methods described above, the full-scale bridge output is no longer equal to V_{FS} because the excitation voltage at full scale is no longer 5V. All the calculations and adjustment procedures described above assume V_{FS} to be the full-scale bridge output with constant 5V excitation. It is not necessary to iterate the calculations or adjustment procedures using the new full-scale bridge output as a starting point. However, a new value for R_G must be calculated using equation 6.

A refined value for R_{LIN} , arrived at either by active circuit trimming, or by measuring linearization gain (equation 7) will improve linearity. Reduction of the original parabolic nonlinearity of the sensor can approach 40:1. Actual results will depend on higher-order nonlinearity of the sensor.

If no linearity correction is desired, make no connections to the R_{LIN} pins ($R_{LIN} = \infty$). This will cause the V_R output to remain a constant +5V. The V_{LIN}^+ and V_{LIN}^- inputs should remain connected to the bridge output to keep these inputs biased in their active region.

OTHER SENSOR TYPES

The XTR104 can be used with a wide variety of inputs. Its high input impedance instrumentation amplifier is versatile and can be configured for differential input voltages from millivolts to a maximum of 1V full scale. The linear common-mode range of the inputs is from 2V to 4V, referenced to the I_o terminal, pin 7.

You can use the linearization feature of the XTR104 with any sensor whose output is ratiometric with an excitation voltage. For example, Figure 5 shows the XTR104 used with a potentiometer position sensor.

REVERSE-VOLTAGE PROTECTION

Figure 6 shows two ways to protect against reversed output connection lines. Trade-offs in an application will determine which technique is better. D_1 offers series protection, but causes a 0.7V loss in loop supply voltage. This may be undesirable if $V+$ can approach the 9V limit. Using D_2 (without D_1) has no voltage loss, but high current will flow in the loop supply if the leads are reversed. This could damage the power supply or the sense resistor, R_L . A diode with a higher current rating is needed for D_2 to withstand the highest current that could occur with reversed lines.

SURGE PROTECTION

Long lines may be subject to voltage surges which can damage semiconductor components. To avoid damage, the maximum applied voltage rating for the XTR104 is 40V. A zener diode can be used for D_2 (Figure 7) to clamp the voltage applied to the XTR104 to a safe level. The loop power supply voltage must be lower than the voltage rating of the zener diode.

There are special zener diode types (Figure 7) specifically designed to provide a very low impedance clamp and withstand large energy surges. These devices normally have a diode characteristic in the forward direction which also

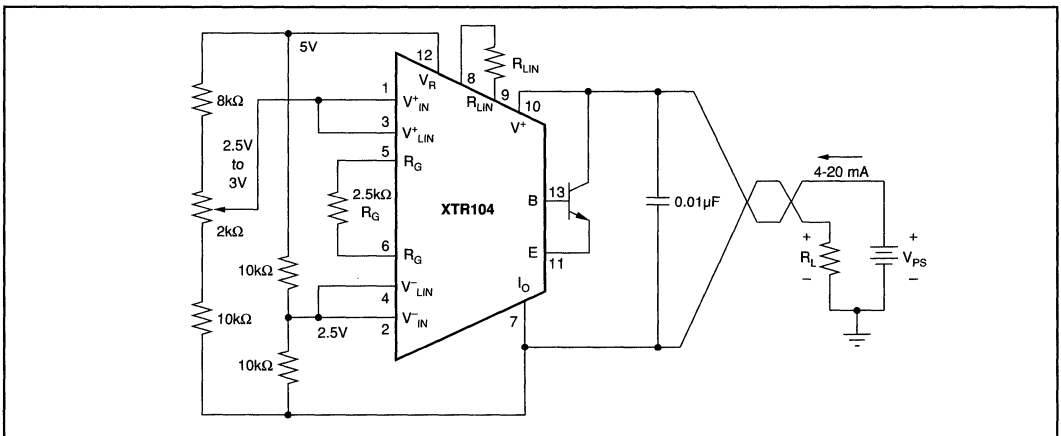


FIGURE 5. Potentiometer Sensor Application.

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protects against reversed loop connections. As noted earlier, reversed loop connections would produce a large loop current, possibly damaging R_L .

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency interference. RF can be rectified by the sensitive input circuitry of the XTR104 causing errors. This generally appears as an unstable output current that varies with the position of loop supply or input wiring.

If the bridge sensor is remotely located from the XTR104, the interference may enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections.

Bypass capacitors on the input often reduce or eliminate this interference. Connect these bypass capacitors to the I_o terminal (see Figure 7). Although the DC voltage at the I_o terminal is not equal to 0V (at the loop supply, V_{PS}) this circuit point can be considered the transmitter's "ground".

LOW-IMPEDANCE BRIDGES

Low impedance bridges can be used with the XTR104 by adding series resistance to limit excitation current to $\leq 2\text{mA}$. Equal resistance should be added to the upper and lower sides of the bridge (Figure 8) to keep the bridge output voltage centered at approximately 2.5V. Bridge output is reduced, so a preamplifier, as shown, may be needed to reduce offset and drift.

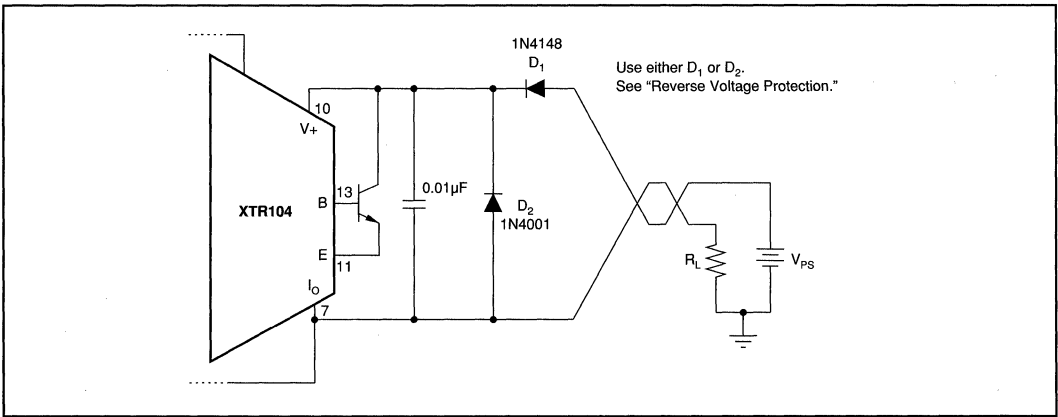


FIGURE 6. Reverse Voltage Protection.

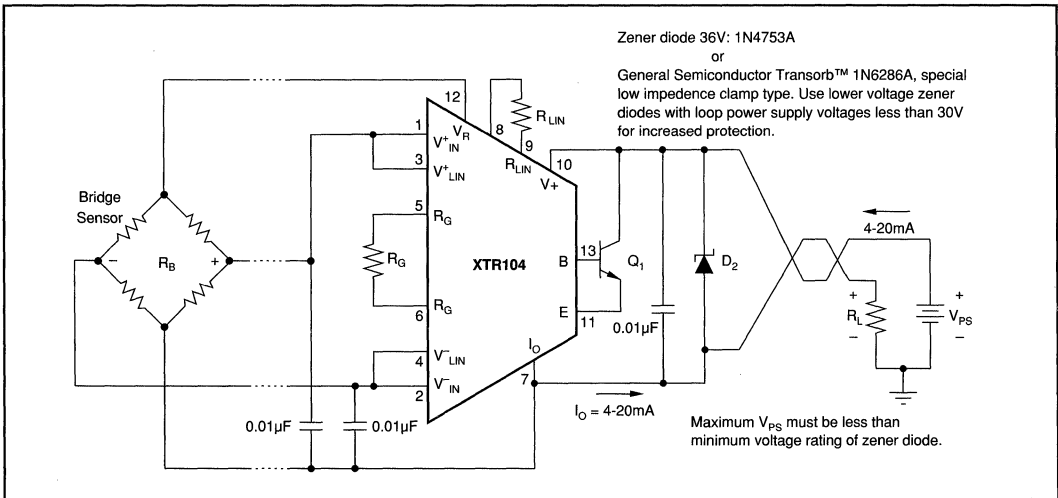


FIGURE 7. Over-Voltage Surge Protection.

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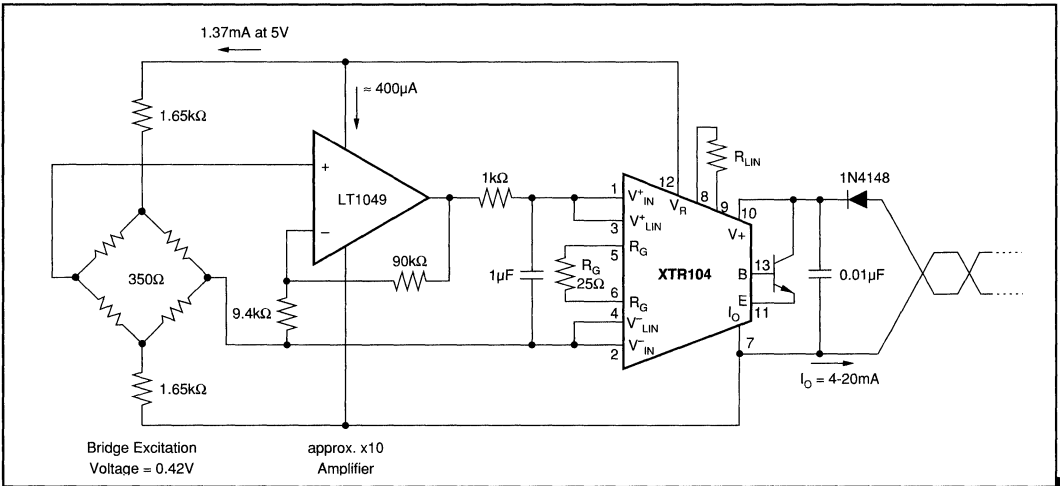


FIGURE 8. 350 Ω Bridge With X10 Preamplifier.

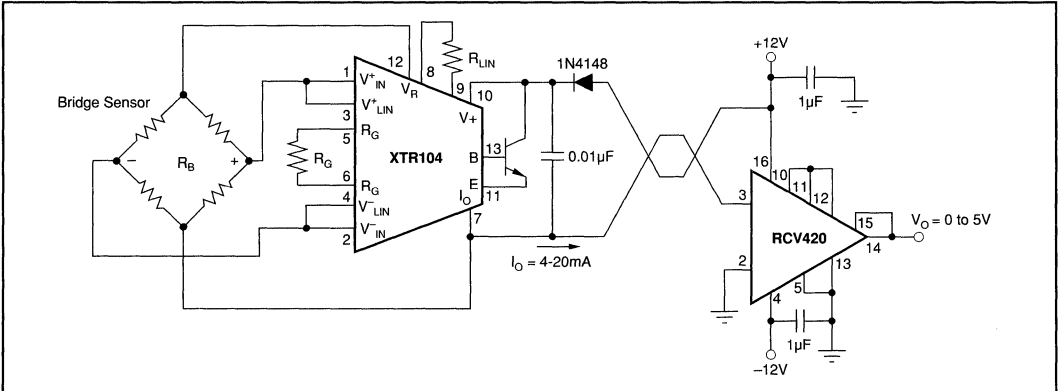


FIGURE 9. $\pm 12\text{V}$ -Powered Transmitter/Receiver Loop.

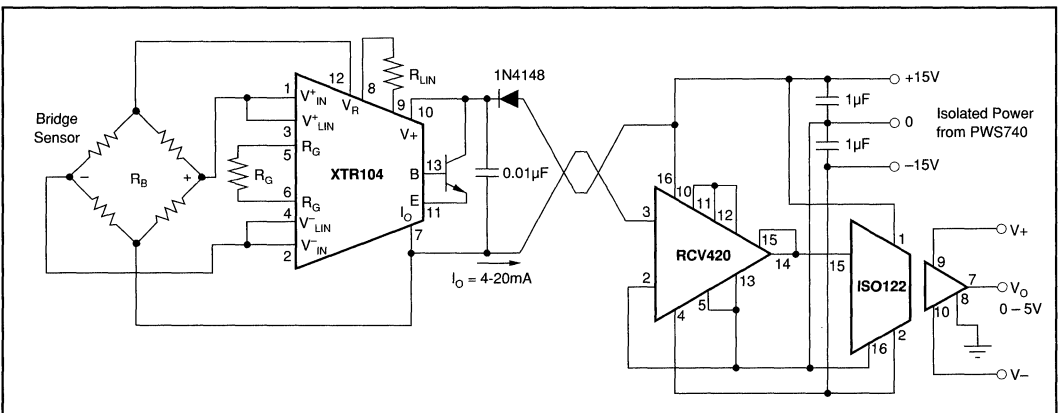
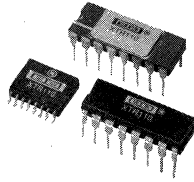


FIGURE 10. Isolated Transmitter/Receiver Loop.

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XTR110

PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
0V to +5V, 0V to +10V Inputs
0mA to 20mA, 5mA to 25mA Outputs
Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- WIDE SUPPLY RANGE: 13.5V to 40V

APPLICATIONS

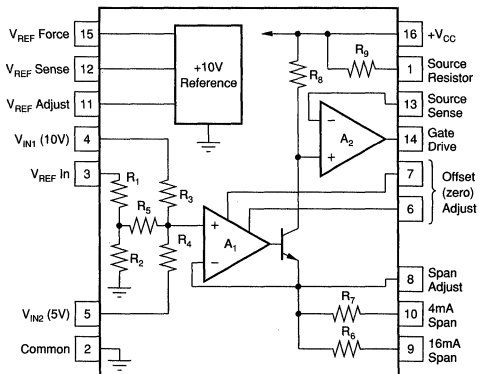
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a precision voltage-to-current converter designed for analog signal transmission. It accepts inputs of 0 to 5V or 0 to 10V and can be connected for outputs of 4 to 20mA, 0 to 20mA, 5 to 25mA and many other commonly used ranges.

A precision on-chip metal film resistor network provides input scaling and current offsetting. An internal 10V voltage reference can be used to drive external circuitry.

The XTR110 is available in 16-pin plastic DIP, ceramic DIP and SOL-16 surface-mount packages. Commercial and industrial temperature range models are available.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_{CC} = +24\text{V}$ and $R_L = 250\Omega^*$, unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG, KP, KU			XTR110BG			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
TRANSMITTER									
Transfer Function			$I_O = 10 \left[\frac{(V_{REF} \ln/16) + (V_{IN1}/4) + (V_{IN2}/2)}{R_{SPAN}} \right]$						
Input Range: $V_{IN1}^{(5)}$ V_{IN2}	Specified Performance	0	+10		*		*	V	
Current, I_O	Specified Performance	0	+5		*		*	V	
	Specified Performance ⁽¹⁾	4	20		*		*	mA	
	Derated Performance ⁽¹⁾	0	40		*		*	mA	
Nonlinearity	16mA/20mA Span ⁽²⁾		0.01	0.025		0.002	0.005	% of Span	
Offset Current, I_{OS}	$I_O = 4\text{mA}^{(1)}$								
Initial	⁽¹⁾		0.2	0.4		0.02	0.1	% of Span	
		vs Temperature	0.0003	0.005		*	0.003	% of Span/ $^\circ\text{C}$	
		vs Supply, V_{CC}	0.0005	0.005		*	*	% of Span/V	
Span Error	$I_O = 20\text{mA}$								
		Initial	⁽¹⁾	0.3	0.6		0.05	0.2	% of Span
		vs Temperature	⁽¹⁾	0.0025	0.005		0.0009	0.003	% of Span/ $^\circ\text{C}$
vs Supply, V_{CC}	⁽¹⁾	0.003	0.005		*	*	% of Span/V		
Output Resistance	From Drain of FET (Q_{EXT}) ⁽³⁾		10×10^9					Ω	
Input Resistance		V_{IN1}	27			*	*	k Ω	
		V_{IN2}	22			*	*	k Ω	
		$V_{REF} \ln$	19			*	*	k Ω	
Dynamic Response									
Settling Time	To 0.1% of Span		15			*	*	μs	
	To 0.01% of Span		20			*	*	μs	
Slew Rate			1.3			*	*	mA/ μs	
VOLTAGE REFERENCE									
Output Voltage		+9.95	+10	+10.05	+9.98	*	+10.02	V	
vs Temperature			35	50		15	30	ppm/ $^\circ\text{C}$	
vs Supply, V_{CC}	Line Regulation		0.0002	0.005		*	*	%/V	
vs Output Current	Load Regulation		0.0005	0.01		*	*	%/mA	
vs Time			100			*	*	ppm/1k hrs	
Trim Range		-0.100		+0.25	*		*	V	
Output Current	Specified Performance	10			*		*	mA	
POWER SUPPLY									
Input Voltage, V_{CC}		+13.5		+40	*		*	V	
Quiescent Current	Excluding I_O		3	4.5		*	*	mA	
TEMPERATURE RANGE									
Specification: AG, BG		-40		+85	*		*	$^\circ\text{C}$	
KP, KU		0		+70				$^\circ\text{C}$	
Operating: AG, BG		-55		+125	*		*	$^\circ\text{C}$	
KP, KU		-25		+85				$^\circ\text{C}$	

* Specifications same as AG/KP grades. ** Specifications apply to the range of R_L shown in Typical Performance Curves

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by $(+V_{CC} - 2V) + V_{DS}$ required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 3. (5) For extended I_{REF} drive circuit see Figure 4. (5) Unit may be damaged. See section, "Input Voltage Range".

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$	40V
Input Voltage, V_{IN1} , V_{IN2} , $V_{REF IN}$	$+V_{CC}$
See text regarding safe negative input voltage range.	
Storage Temperature Range: A, B	-55°C to $+125^\circ\text{C}$
K, U	-40°C to $+85^\circ\text{C}$
Lead Temperature	
(soldering, 10s) G, P	300°C
(wave soldering, 3s) U	260°C
Output Short-Circuit Duration, Gate Drive and V_{REF} Force	Continuous to common and $+V_{CC}$
Output Current Using Internal 50Ω Resistor	40mA



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

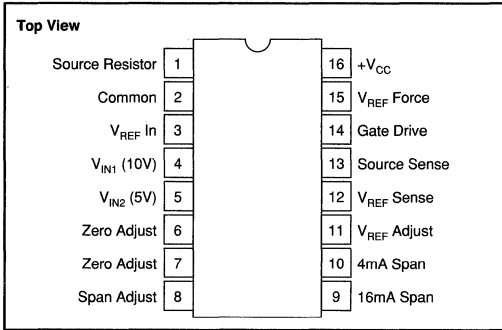
XTR110

4

INSTRUMENTATION AMPLIFIERS

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PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
XTR110AG	16-Pin Ceramic DIP	109
XTR110BG	16-Pin Ceramic DIP	109
XTR110KP	16-Pin Plastic DIP	180
XTR110KU	SOL-16 Surface-Mount	211

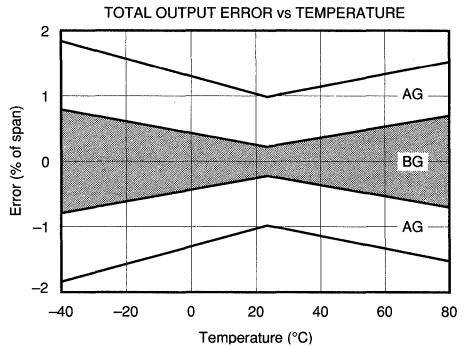
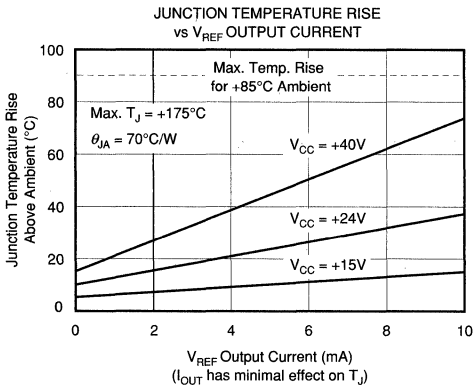
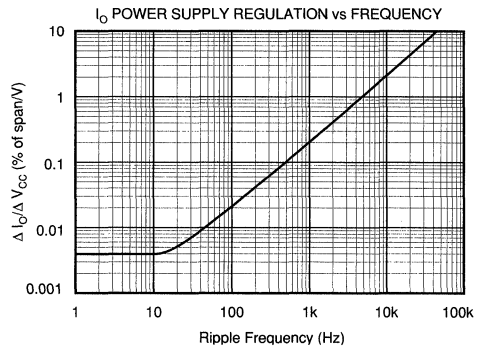
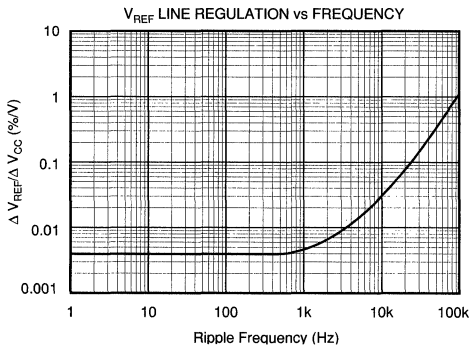
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
XTR110AG	16-Pin Ceramic DIP	-40°C to +85°C
XTR110BG	16-Pin Ceramic DIP	-40°C to +85°C
XTR110KP	16-Pin Plastic DIP	0°C to +70°C
XTR110KU	SOL-16 Surface-Mount	0°C to +70°C

TYPICAL PERFORMANCE CURVES

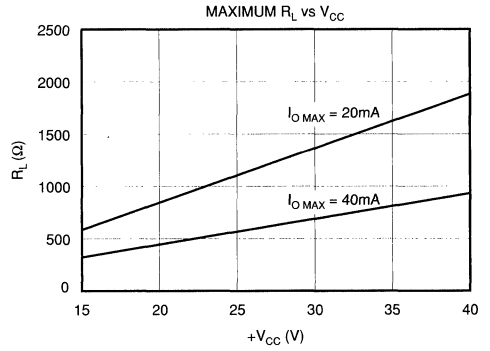
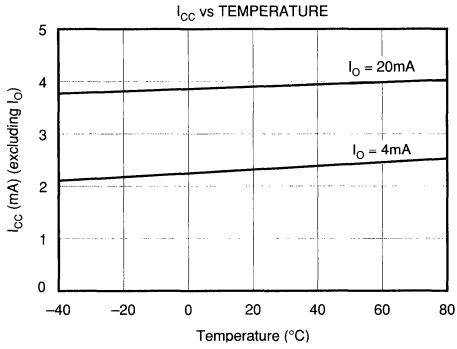
T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω, unless otherwise noted.



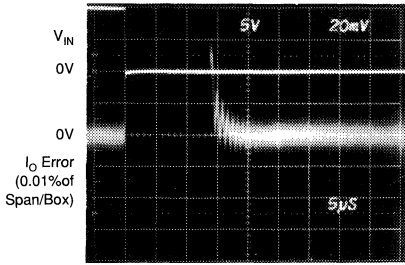
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TYPICAL PERFORMANCE CURVES (CONT)

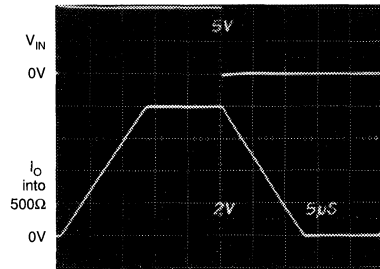
$T_A = +25^\circ\text{C}$, $V_{CC} = 24\text{VDC}$, $R_L = 250\Omega$, unless otherwise noted.



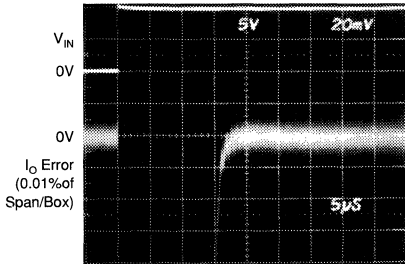
SETTLING TIME WTH NEG V_{IN} STEP



PULSE RESPONSE



SETTLING TIME WTH POS V_{IN} STEP



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APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for 0 to 10V input and 4 to 20mA output. Other input voltage and output current ranges require changes in connections of pins 3, 4, 5, 9 and 10 as shown in the table of Figure 1.

The complete transfer function of the XTR110 is:

$$I_o = \frac{10 \left[\frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \right]}{R_{SPAN}} \quad (1)$$

R_{SPAN} is the internal 50Ω resistor, R_9 , when connected as shown in Figure 1. An external R_{SPAN} can be connected for different output current ranges as described later.

EXTERNAL TRANSISTOR

An external pass transistor, Q_{EXT} , is required as shown in Figure 1. This transistor conducts the output signal current. A P-channel MOSFET transistor is recommended. It must have a voltage rating equal or greater than the maximum power supply voltage. Various recommended types are shown in Table I.

MANUFACTURER	PART NO.	BV _{DSS} ⁽¹⁾	BV _{GS} ⁽¹⁾	PACKAGE
Ferranti	ZVP1304A	40V	20V	TO-92
	ZVP1304B	40V	20V	TO-39
	ZVP1306A	60V	20V	TO-92
	ZVP1306B	60V	20V	TO-39
International Rectifier	IRF9513	60V	20V	TO-220
Motorola	MTP8P08	80V	20V	TO-220
RCA	RFL1P08	80V	20V	TO-39
	RFT2P08	80V	20V	TO-220
Siliconix (preferred)	VP0300B	30V	40V	TO-39
	VP0300L	30V	40V	TO-92
	VP0300M	30V	40V	TO-237
	VP0808B	80V	40V	TO-39
	VP0808L	80V	40V	TO-92
	VP0808M	80V	40V	TO-237
Supertex	VP1304N2	40V	20V	TO-220
	VP1304N3	40V	20V	TO-92
	VP1306N2	60V	20V	TO-220
	VP1306N3	60V	20V	TO-92

NOTE: (1) BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

TABLE I. Available P-Channel MOSFETs.

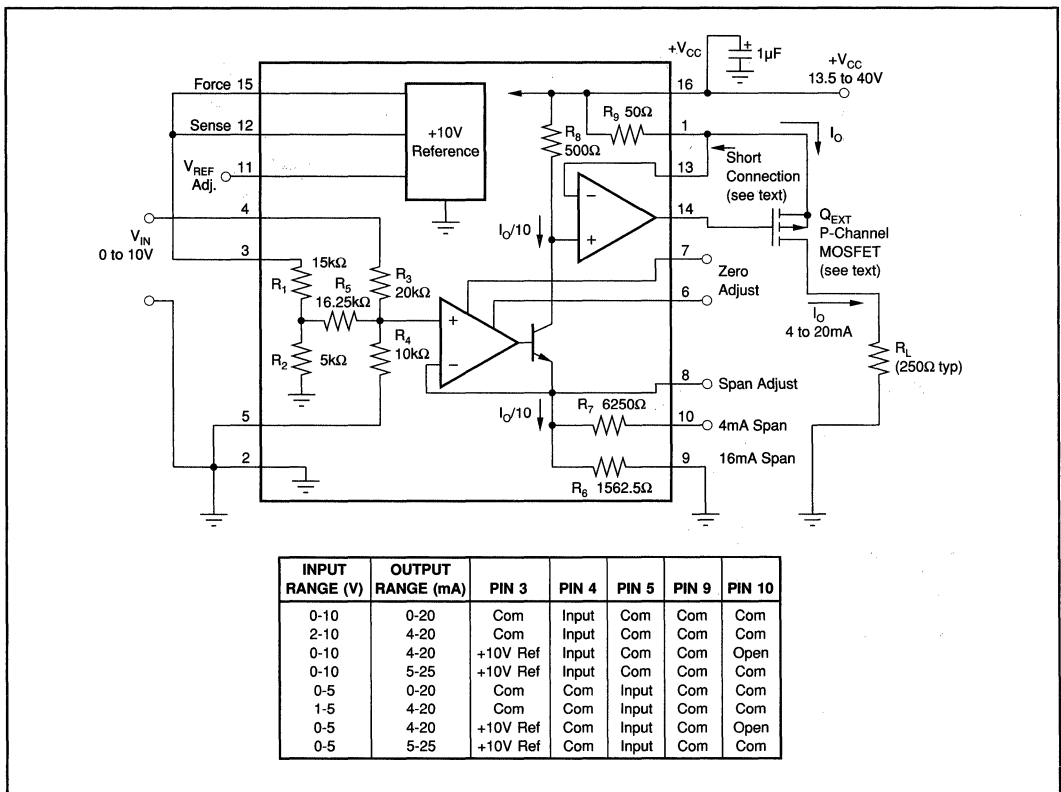


FIGURE 1. Basic Circuit Connection.

If the supply voltage, $+V_{CC}$, exceeds the gate-to-source breakdown voltage of Q_{EXT} , and the output connection (drain of Q_{EXT}) is broken, Q_{EXT} could fail. If the gate-to-source breakdown voltage is lower than $+V_{CC}$, Q_{EXT} can be protected with a 12V zener diode connected from gate to source.

Two PNP discrete transistors (Darlington-connected) can be used for Q_{EXT} —see Figure 2. Note that an additional capacitor is required for stability. Integrated Darlington transistors are not recommended because their internal base-emitter resistors cause excessive error.

TRANSISTOR DISSIPATION

Maximum power dissipation of Q_{EXT} depends on the power supply voltage and full-scale output current. Assuming that the load resistance is low, the power dissipated by Q_{EXT} is:

$$P_{MAX} = (+V_{CC}) I_{FS} \quad (2)$$

The transistor type and heat sinking must be chosen according to the maximum power dissipation to prevent overheating. See Table II for general recommendations.

PACKAGE TYPE	ALLOWABLE POWER DISSIPATION
TO-92	Lowest: Use minimum supply and at +25°C.
TO-237	Acceptable: Trade-off supply and temperature.
TO-39	Good: Adequate for majority of designs.
TO-220	Excellent: For prolonged maximum stress.
TO-3	Use if hermetic package is required.

TABLE II. External Transistor Package Type and Dissipation.

INPUT VOLTAGE RANGE

The internal op amp A_1 can be damaged if its non-inverting input (an internal node) is pulled more than 0.5V below common (0V). This could occur if input pins 3, 4 or 5 were driven with an op amp whose output could swing negative under abnormal conditions. The voltage at the input of A_1 is:

$$V_{A1} = \frac{(V_{REF IN})}{16} + \frac{(V_{IN1})}{4} + \frac{(V_{IN2})}{2} \quad (3)$$

This voltage should not be allowed to go more negative than -0.5V. If necessary, a clamp diode can be connected from the negative-going input to common to clamp the input voltage.

COMMON (Ground)

Careful attention should be directed toward proper connection of the common (grounds). All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any point where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 ($V_{REF SENSE}$). To preserve accuracy, any load including pin 3

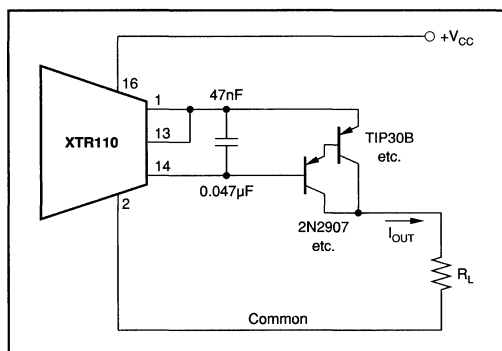


FIGURE 2. Q_{EXT} Using PNP Transistors.

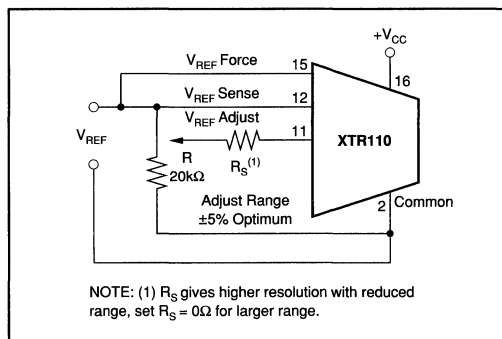


FIGURE 3. Optional Adjustment of Reference Voltage.

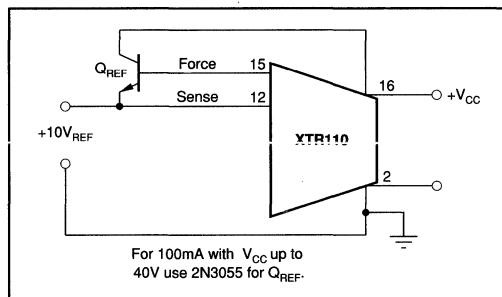


FIGURE 4. Increasing Reference Current Drive.

should be connected to this point. The circuit in Figure 3 shows adjustment of the voltage reference.

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 4.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1 , shown in Figure 5. Set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans

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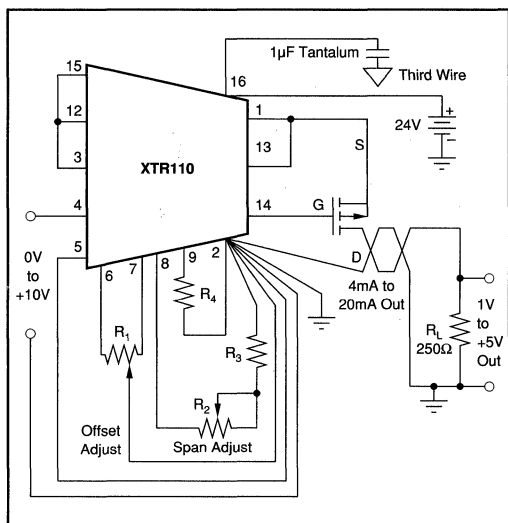


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2 , shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2 , R_3 , and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

LOW TEMPERATURE COEFFICIENT OPERATION

Although the precision resistors in the XTR110 track within 1ppm/°C, the output current depends upon the absolute temperature coefficient (TC) of any one of the resistors, R_6 , R_7 , R_8 , and R_9 . Since the absolute TC of the output current can have 20ppm/°C, maximum, the TC of the output current can have 20ppm/°C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_6 or R_7) or for the source resistor (R_9) but not both.

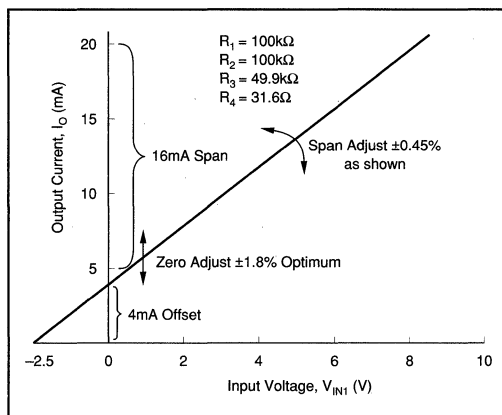


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

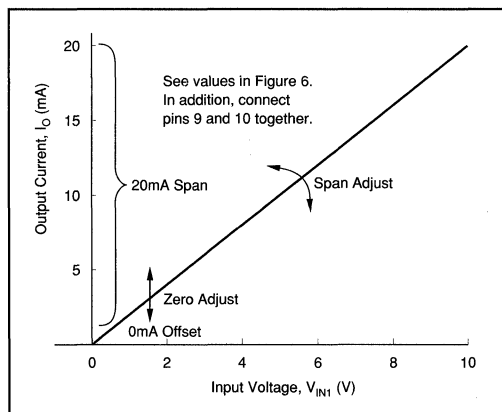


FIGURE 7. Zero and Span of 0V to +10V_{IN1} 0mA to 20mA Output Configuration (see Figure 5).

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_9) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_9 (\text{Span}_{OLD} / \text{Span}_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_9 before determining the final value of R_{EXT} . Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 10 for application.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL APPLICATIONS

The XTR110 is ideal for a variety of applications requiring high noise immunity current-mode signal transmission. The precision +10V reference can be used to excite bridges and transducers. Selectable ranges make it very useful as a precision programmable current source. The compact design

and low price of the XTR110 allow versatility with a minimum of external components and design engineering expense.

Figures 8 through 10 show typical applications of the XTR110.

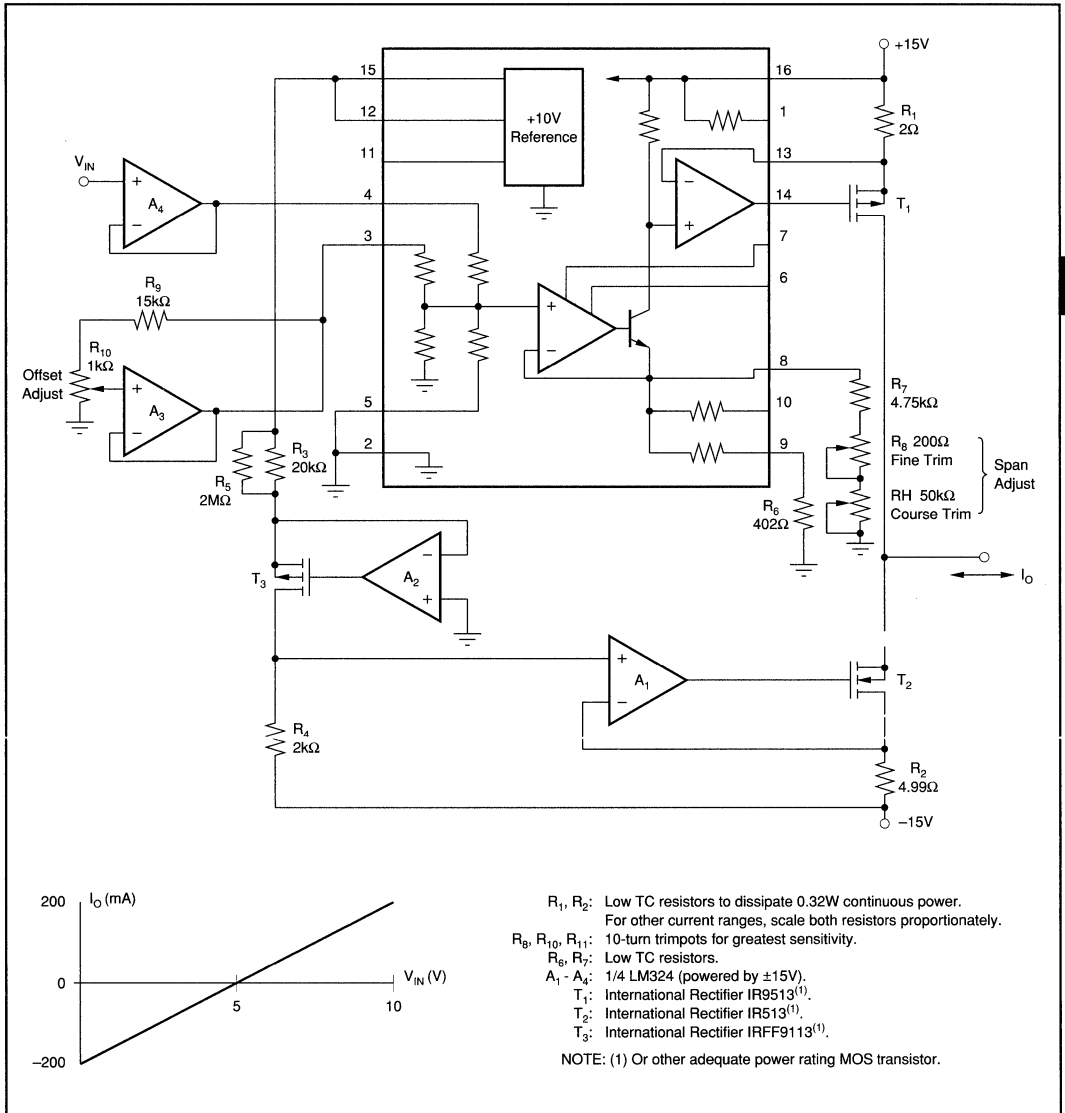


FIGURE 8. $\pm 200mA$ Current Pump.

XTR110

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INSTRUMENTATION AMPLIFIERS

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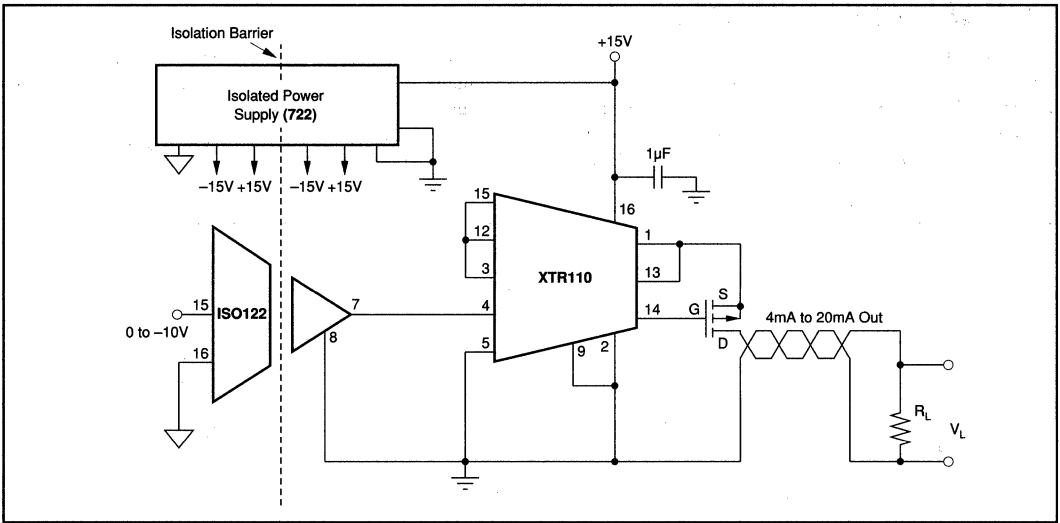


FIGURE 9. Isolated 4mA to 20mA Channel.

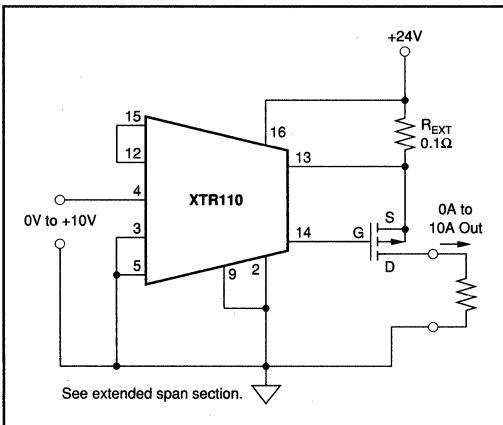


FIGURE 10. 0A to 10A Output Voltage-to-Current Converter.

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XTR501

PRELIMINARY INFORMATION
SUBJECT TO CHANGE
WITHOUT NOTICE

HIGH CURRENT BRIDGE DRIVER and 4-20mA Transmitter

FEATURES

- SENSOR EXCITATION OF 1W
- VARIABLE EXCITATION VOLTAGE:
1.5V to 5.0V
- SINGLE SUPPLY: 11.4V to 30VDC
- INRUSH CURRENT LIMITING
- 4-20mA TRANSMITTER

APPLICATIONS

- GAS DETECTION SENSORS
- PELLISTOR CATALYTIC DETECTORS
- STRAIN GAGES
- HIGH CURRENT BRIDGES
- LOAD CELLS
- HOT-WIRE ANEMOMETERS

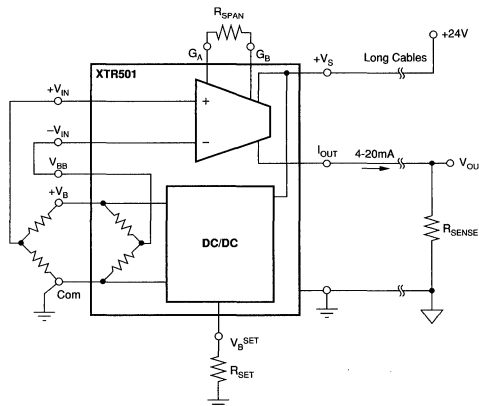
DESCRIPTION

The XTR501 contains a high efficiency DC/DC converter and 4-20mA three wire current transmitter. It provides regulated bridge excitation, optional half bridge, differential inputs and current transmitter necessary for the excitation and signal conditioning of low impedance bridge sensors and high integrity signal transmission.

The DC/DC converter is capable of supplying 1W into a regulated bridge voltage of 1.5V to 5.0V from a supply of 11.4V to 30V. The combination of a low startup current and high efficiency current step-up allows for a combined supply line resistance of up to 100Ω when exciting low impedance sensors.

The instrumentation amplifier of the current transmitter can be used over a wide range of gains, accommodating a variety of input signals and sensors.

The XTR501 is particularly suited to excitation of high current/low impedance sensors used in bridge applications allowing the use of lighter cabling leading to considerable savings on cabling costs.



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PDS-1212

4.245

XTR501

4

INSTRUMENTATION AMPLIFIERS

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = 24\text{V}$, $V_{\text{BRIDGE}} = 2\text{V}$, $I_{\text{LOAD}} = 300\text{mA}$ unless otherwise specified.

PARAMETER	CONDITIONS	XTR501			UNITS
		MIN	TYP	MAX	
INSTRUMENTATION AMPLIFIER/CURRENT TRANSMITTER					
SIGNAL OUTPUT					
Output Current Equation	R_G in Ω , V_{IN} in V	$I_O = 0.004 + 0.016 [(1 + 50\text{k}\Omega/R_G)/4.94] V_{IN}$			A
Output Current	Linear Operating Range	4	27	20	mA
Over-scale Limit		25	0		mA
Under-scale Limit					mA
ZERO					
Output Current			4		mA
Offset Error			± 50	± 100	μA
vs Temperature			0.2		$\mu\text{A}/^\circ\text{C}$
vs Supply Voltage	$V_S = 11.4\text{V}$ to 30V		0.5	2	$\mu\text{A}/\text{V}$
SPAN					
Span Equation	R_G in Ω , V_{IN} in V	Span = $0.016[(1 + 50\text{k}\Omega/R_G)/4.94]$			A/V
Untrimmed Error	$G = 1$		± 0.2	± 2.5	%
	$G = 250$		± 1.5	± 10	%
vs Temperature			50		ppm/ $^\circ\text{C}$
Nonlinearity	$G = 1$, $I_O = 4\text{mA}$ to 20mA			± 0.025	%
INPUT					
Common-Mode Range		0		$4.94^{(1)}$	V
Offset Voltage			35		mV
vs Temperature			50		$\mu\text{V}/^\circ\text{C}$
vs Supply Voltage			100		dB
Common-Mode Rejection			85		dB
Impedance; Differential, Common-Mode			$10^9 \parallel 6$		$\Omega \parallel \text{pF}$
DC/DC CONVERTER					
BRIDGE EXCITATION VOLTAGE SOURCE					
Output Voltage		1.5		5	V
vs Temperature	$V_{IN} = 0\text{V}$, $G = 1$		200		ppm/ $^\circ\text{C}$
vs Long Term Stability			100		ppm/1000hrs
Output Power				1	W
Line Voltage Regulation	$V_S = 11.4\text{V}$ to 30.0V		0.25		%
Load Voltage Regulation	Load Current 160mA to 340mA		0.25		%
Output Voltage Ripple	Load Voltage 2V Load Current 300mA Load Voltage 2V		150		mV
Output Voltage Ripple Frequency			100		kHz
Output Short-Circuit Current	Limited Duration		2.6		A
Input Current	Output Short-Circuit		150		mA
POWER SUPPLY					
Supply Voltage, V_S		11.4	24	30	V
Supply Current			See Typical Curve		
TEMPERATURE					
Operating		-40		+70	$^\circ\text{C}$
Storage		-40		+85	$^\circ\text{C}$

NOTE: (1) Common-Mode Range is based on a multiple of a bandgap reference of 1.235V.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

5 Isolation Products

Isolation amplifiers can be used to amplify and measure low level signals in the presence of high common-mode voltages, breakground loops and/or eliminate source ground connections, provide an interface between medical patient monitoring equipment and provide isolation protection to electronic instruments/equipment.

Our isolation amplifiers feature three different technologies—transformer isolation, capacitor isolation, and opto-isolation. The following selection guides will help you determine the performance and functionality that best fit your requirements.

Choose from the industry's most complete line of isolation solutions including:

ISO130—Provides high isolation-mode rejection, wide bandwidth and low cost in 8-pin DIP and surface-mount packages.

ISO122—Low cost, 1500V isolation available in 16-pin plastic DIP and 28-pin SOIC packages.

ISO120—Industry's first total hermetic isolation amplifier with 0.01% linearity. It is synchronous

and offered with specifications over the military temperature range.

ISO103—Unity-gain isolation amp combined with an internal isolated DC/DC converter in a space-saving, 24-pin ceramic DIP.

ISO212—Low cost, uncommitted input amplifier, differential output with an internal isolated DC/DC converter.

ISO100—Versatile, adjustable gain optically-coupled amplifier in a 18-pin DIP.

3656—Transformer-coupled amplifier with an internal isolated DC/DC converter that offers three port isolation.

ISO150—High speed, low cost dual digital transceiver that is TTL- and CMOS-compatible, available in a 24-pin plastic DIP and in a 28-Lead SOIC.

The selection guide also includes our versatile line of isolated DC/DC converters.

5

ISOLATION PRODUCTS

OPTICALLY-COUPLED ISOLATION AMPLIFIERS

Boldface = NEW

Descrip	Model	Isolation Voltage (V)		Isolation Mode Rejection, typ		Leakage Current (μA)	Iso Impedance (Ω) (pF)	Gain Non-linearity		Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp ⁽¹⁾	Page No.	
		Cont Peak	Pulse Test Peak	DC (dB)	60Hz (dB)			max (%)	typ (%)							
Balanced Current Input	3650	2000	5000	140	120	0.35 ⁽²⁾	10 ¹²	1.8	±0.05	±0.02	5	40nA	15	Yes	Ind	5.189
Balanced	3652	2000	5000	140	120	0.35 ⁽²⁾	10 ¹²	1.8	±0.1	±0.05	25	50pA	15	Yes	Ind	5.189
Low Drift Wide BW	ISO100	750	2500	146 ⁽³⁾	108 ⁽³⁾	0.3 ⁽²⁾	10 ¹²	2.5	0.07	0.02	2.5 ⁽³⁾	10nA	60	Yes	Ind	5.15
High IMR Wide BW	ISO130	720	960	140	140	TBO	10¹³	0.7	±0.25	±0.1	2.1⁽⁴⁾	670nA⁽⁴⁾	85	Yes	Ind	5.97

NOTES: All packages are DIPs. (1) Ind = -25°C to +85°C. (2) At 240V/60Hz. (3) R_{in} = 10kΩ (4) Typical.

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CAPACITOR-COUPLED ISOLATION AMPLIFIERS

Boldface = NEW

Descrip	Model	Isolation Voltage (V)		Isolation Mode Rejection, typ		Leakage Current (μA)	Iso Impedance		Gain Non-linearity		Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp ⁽¹⁾	Page No.
		Cont Peak	Pulse Test Peak	DC 60Hz (dB)	60Hz (dB)		Ω	pF	max (%)	typ (%)						
1500VAC Isolation	ISO102	2121	4000	160	120	1.0	10 ¹⁴	6	±0.003	±0.002	±250	—	70	Yes	Ind ⁽³⁾	5.30
	ISO120	2121	2500 ⁽²⁾	160	115	0.5	10 ¹⁴	2	±0.01	±0.005	±150	—	60	Yes	Ind ⁽³⁾	5.70
	ISO122	1500	2400 ⁽²⁾	160	140	0.5	10 ¹⁴	2	±0.02	±0.016	±200 ⁽⁴⁾	—	50	Yes	Com	5.84
3500VAC Isolation	ISO106	4950	8000	160	130	1.0	10 ¹⁴	6	±0.025	±0.007	±250	—	70	Yes	Ind ⁽³⁾	5.30
	ISO121	4950	5600 ⁽²⁾	160	115	0.5	10 ¹⁴	2	±0.01	±0.005	±150	—	60	Yes	Ind ⁽³⁾	5.70

NOTES: All packages are DIPs except ISO122 which is also available in SOIC. (1) Ind = -25°C to +85°C. Com = 0°C to +70°C. (2) Partial discharge test voltage. (3) Hermetic. (4) Typical.

TRANSFORMER-COUPLED ISOLATION AMPLIFIERS

Boldface = NEW

Descrip	Model	Isolation Voltage (V)		Isolation Mode Rejection, typ		Leakage Current (μA)	Iso Impedance		Gain Non-linearity		Voltage Drift (±μV/°C) max	Bias Current max	±3dB Freq (kHz)	Ext Iso Power Req	Temp ⁽¹⁾	Page No.
		Cont Peak	Pulse Test Peak	DC 60Hz (dB)	60Hz (dB)		Ω	pF	max (%)	typ (%)						
High Isolation Voltage	3656	3500	8000	160	125	0.5	10 ¹²	6	±0.05	±0.03	5+ (350/G _i)	100nA	30	No	Ind	5.201
Low Cost Self-Powered	ISO212	1060	1200 ⁽²⁾	160	115	2	10 ¹⁰	12	±0.025	±0.015	±30 (±30/G _i)	50nA	1	No	Com	5.117

NOTES: The package for the 3656G is a DIP, the package for the ISO212P is a SIP. (1) Ind = -25°C to +85°C, Com = 0°C to +70°C. (2) Partial discharge test voltage.

CAPACITOR-COUPLED ISOLATION AMPLIFIER, WITH POWER

Boldface = NEW

Description	Model	Isolation Voltage (V)		Isolation Mode Rejection, typ		Leakage Current (μA)	Iso Impedance		Gain Non-linearity		Voltage Drift (±μV/°C) max	Bias Current	±3dB Freq (kHz)	Temp ⁽¹⁾	Page No.
		Cont Peak	Pulse Test Peak	DC 60Hz (dB)	60Hz (dB)		Ω	pF	max (%)	typ (%)					
1500VAC Input Power	ISO103	2121	5657	160	130	2.0	10 ¹²	9	.05	.018	250	—	20	Ind	5.45
1500VAC Output Power	ISO113	2121	5657	160	130	2.0	10 ¹²	9	0.02	0.012	250	—	20	Ind	5.62
2500VAC Input Power	ISO107	3500	8000	160	100	2.0	10 ¹²	13	0.025	0.01	400	—	20	Ind	5.54

NOTES: All packages are DIPs. (1) Ind = -25°C to +85°C.

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ISOLATION POWER SUPPLIES⁽¹⁾

Boldface = NEW

Description	Model	Isolation Voltage (V)		Input Voltage (VDC)		Leakage Current 240VAC 60Hz (µA)	Iso Impedance		Current, Balanced Loads On All Outputs (mA)		Sensitivity To Input Change (V/V)	Temp ⁽²⁾	Pkg	Page No.
		Cont Peak	Pulse Test Peak	min	max		(Ω)	(pF)	Rated	Max ⁽¹⁾				
Single ±15V Output	PWS725A	2121	4000	7	18	2	10 ¹²	9	±15	±40	1.15	Ind	DIP	5.142
	PWS726A	4950	8000	7	18	2	10 ¹²	9	±15	±40	1.15	Ind	DIP	5.142
Dual ±15V Output	0722	3500	8000	5	16	1	10 ¹⁰	6	±3-40	±50	1.13	Ind	Mod	5.179
Quad ±8V Output	0724	1000	3000	5	16	1	10 ¹⁰	6	±3-16	±60	0.63	Ind	Mod	5.184
Multiple Output (1-8)	PWS740	2121	4000	7	20	1.5	10 ¹²	3	30 ⁽⁸⁾	60 ⁽³⁾	1.20	Ind	Sys ⁽⁴⁾	5.148
	PWS745 ⁽⁸⁾	1060	1200 ⁽⁸⁾	4.5 ⁽⁵⁾	18 ⁽⁶⁾	1.5	10 ¹²	8	±15	30	⁽⁷⁾	Ind	Comp	5.156
	PWS750	1060	1200 ⁽⁸⁾	4.5 ⁽⁵⁾	18 ⁽⁶⁾	1.5	10 ¹²	8	±15	30	⁽⁷⁾	Ind	Comp	5.166

NOTES: (1) See complete Product Data Sheet for full specifications, especially regarding output current capabilities. (2) Ind = -25°C to +85°C. Com = 0°C to +70°C. (3) Per channel. (4) 1 TO-3 driver per 8 channels, plus 2 DIPs per channel. (5) 5V operation. (6) 15V operation. (7) 5V operation: 4.12; 15V operation: 1.2. (8) PWS745-1 driver may also be used with PWS740 and PWS750 components. (9) Partial discharge test voltage.

CAPACITOR-COUPLED, DIGITAL COUPLER

Boldface = NEW

Description	Model	Isolation Voltage (V)		Leakage Current 240VAC 60Hz (µA)	Iso Impedance		Data Rate (MBd)	Common Mode Transient Immunity (kV/µs)	Power Consumption per Channel (mW)	Ext Power Req	Page Temp ⁽¹⁾	Pkg	No.
		Cont Peak	Pulse Test Peak		(Ω)	(pF)							
Dual Isolated Transceiver	ISO150	1500	2400 ⁽²⁾	0.6	10 ¹²	5	80 ⁽³⁾	1.6 ⁽³⁾	250	Yes	XInd	DIP, SOIC	5.108

NOTES: (1) XInd = 40°C to +85°C. (2) Partial discharge test voltage. (3) Typical.

SPECIAL FUNCTIONS

Boldface = NEW

Description	Model	Isolation Voltage	Isolation Mode	Leakage Current	Isolation Impedance	Gain Non-linearity	Frequency Response	Input Bias Current	Reference Voltage	Isolated Power Req	Temp. Range	Pkg	Page No.
Precision Measured Channel	ISC300	500rms	60Hz cont	4µArms	2GΩ 15pF	±0.01% (typ)	3.5Hz	35nA (typ)	Yes	No	0°C to +70°C	Mod	5.4

ISOLATION CURRENT TRANSMITTER

Boldface = NEW

Description	Model	Span	Temperature Drift	Input	Output	Temperature Range	Pkg	Page No.
Two-wire	IXR100	untrimmed error (max): -2.5% non-linearity (max): 0.01% (EMF), 0.1% (RTD)	50ppm (typ) 100ppm (max)	Offset Voltage 500µV (typ) Offset Voltage vs Temp 5µV/°C CMR vs Supply 100dB	Current Range 4 - 20mA Current Limit 32mA Isolation Voltage 1500rms	-20 to +70°C	Mod	5.128

5

ISOLATION PRODUCTS



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ISC300

Universal Precision Isolated MEASUREMENT CHANNEL

FEATURES

- CALIBRATION CAPABILITY
- INTEGRAL SENSOR EXCITATION
- OPEN CIRCUIT SENSOR DETECTION
- LOW POWER: 80mW
- INSTRUMENT AMPLIFIER INPUT
- PROGRAMMABLE GAIN
- 12-BIT LINEARITY
- TWO ISOLATED POWER SUPPLIES:
±13V at 5mA
- LOW DRIFT 10V REFERENCE

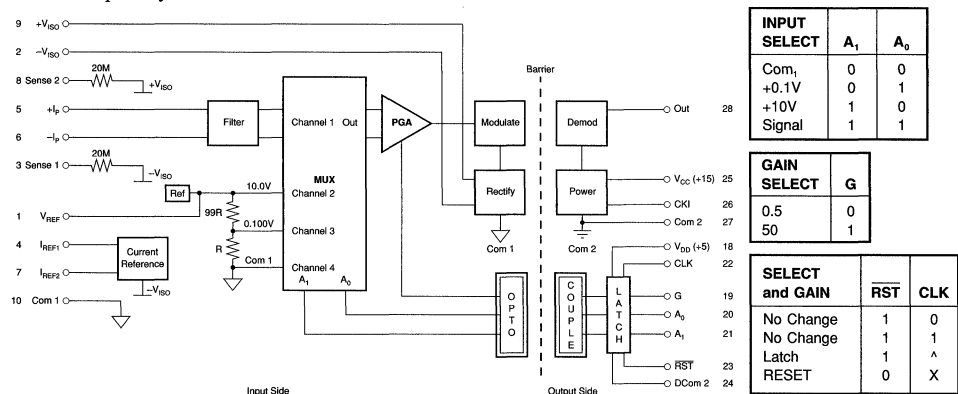
APPLICATIONS

- UNIVERSAL INPUT CHANNEL FOR PROCESS CONTROL SYSTEMS
- ISOLATED MEASUREMENT CHANNEL FOR THERMOCOUPLE, RTD AND VOLTAGE TRANSDUCERS
- CHANNEL TO CHANNEL ISOLATED MULTIPLEXED SYSTEMS
- ISOLATED 4 TO 20mA RECEIVER

DESCRIPTION

The ISC300 is an isolated measurement channel with open circuit sensor detection for use with RTD and thermocouple temperature sensors. In addition to temperature measurement, the ISC300 can accept full scale input voltages of ±100mV and ±10V which allows use with other sensors such as pressure, humidity and flow sensors. The low level resistance measurement capability also allows stimulus and measure-

ment of strain gauges. The measurement channel has a highly stable internal reference which can be selected from the output side. This allows the user to calibrate each channel at the factory, record the calibration data and periodically recalibrate the system while in use over time and ambient temperature changes.



INPUT SELECT	A ₁	A ₀
Com, +0.1V	0	0
+10V	0	1
Signal	1	0
	1	1

GAIN SELECT	G
0.5	0
50	1

SELECT and GAIN	RST	CLK
No Change	1	0
No Change	1	1
Latch	1	^
RESET	0	X

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = 15V$, $V_{DD} = 5V$, $T_A = +25^{\circ}C$ unless otherwise noted.

PARAMETER	CONDITIONS	ISC300			UNITS
		MIN	TYP	MAX	
ISOLATION Isolation Voltage (V_{ISO})	AC60Hz Continuous	500			Vrms
	AC60Hz Continuous	± 700			V_{PEAK}
	V_{ISO} , DC	700			V
	Partial Discharge ⁽¹⁾	800			Vrms
Isolation Mode Rejection (IMR)	$V_{ISO} = \text{Rated } 60\text{Hz Cont}^{(2)}$	110			dB
Barrier Impedance			2 15		G Ω pF
Leakage Current (I_{ISO})	$V_{ISO} = 240$ Vrms 60Hz			4	μArms
GAIN					
Voltage Gains			50, 0.5		V/V
Resistance Conversion			10		mV/ Ω
Initial Error				± 3	%
vs Temperature	0°C to +70°C			± 30	ppm/°C
Nonlinearity	$V_O = -5V$ to +5V ⁽⁴⁾			± 0.025	%
INPUT OFFSET VOLTAGE					
Initial Offset (Input Referred)	$V_{IN} = 0V$ G = 0.5			± 200	mV
	$V_{IN} = 0V$ G = 50			± 5	mV
vs Temperature	0°C to +70°C G = 0.5			± 200	$\mu\text{V}/^{\circ}C$
	0°C to +70°C G = 50			± 5	$\mu\text{V}/^{\circ}C$
vs Supply (V_{CC})	$V_{CC} = 14V$ to 16V		± 1.5		mV/V
INPUT CURRENT					
Initial Bias			35	50	nA
vs Temperature	-40°C to +85°C		100		pA/°C
INPUT					
Voltage Range	Rated Operation G = 0.5V Input			± 10	V
	Rated Operation G = 50V Input			± 0.1	V
Resistance Range	Rated Operation G = 50 3-wire Resistance	0		500	Ω
Peak Voltage	Applied to Any Signal Input Wrt Com 1 ⁽⁵⁾			± 380	V
Impedance: Differential		10			M Ω
Common Mode Rejection	CMR at DC Gain = 0.5 ⁽³⁾	66	75		dB
	CMR at DC Gain = 50 ⁽³⁾	75	100		dB
	CMR at 60Hz ⁽³⁾	60	70		dB
Source Impedance Imbalance	For Normal Operation < 1k Ω Imbalance			10	k Ω
OUTPUT					
Voltage Range	Min Load = 1M Ω			± 5	V
Overrange Voltage	During Input Fault ($V_{IN} < -11V$ or $V_{IN} > 11V$)	± 5.4			kV
Output Impedance			3		k Ω
Ripple Voltage	f = 0 to 5kHz Min Load 1M Ω		0.5		mVrms
	f = 0 to 100kHz Min Load 1M Ω		10		mVp-p
FREQUENCY RESPONSE					
Input Bandwidth			3.5		Hz
Input Settling Time			0.5		s
Input Overload Recovery			5		s
Output Overload Settling Time	T_{SETT} , to within 5% for $V_{IN} < 14V$		1	5	ms
Output Overload Recovery			2		ms
VOLTAGE REFERENCE					
V_{REF1} (Internal and External)			10		V
Initial Accuracy	External Loading of 100nA		± 0.1	± 1	%
vs Temperature			± 10	± 20	ppm/°C
vs Time				± 20	ppm/kHR
vs Supply (V_{CC})				± 20	%/V
V_{REF2} (Internal)			100		mV
Initial Accuracy ⁽⁶⁾			± 0.1	± 1	%
vs Temperature			± 10	± 20	ppm/°C
vs Time				± 20	ppm/kHR
vs Supply (V_{CC})				± 20	%/V
POWER SUPPLIES					
Analog Supply Range	V_{CC} Pin	14		16	V
Supply Current	No External Load		5	10	mA
Digital Supply Range	V_{DD} Pin	4		6	V
Supply Current			1	3	mA
Total Power Dissipation	No External Load		80	184	mW
Isolated Supplies: Voltage	at 5mA Each Supply	11.5	13		V
Current			5		mA

ISC300

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ISOLATION PRODUCTS

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SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = 15V$, $V_{DD} = 5V$, $T_A = +25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	ISC300			UNITS
		MIN	TYP	MAX	
INPUT O/C SENSE Sense Current	I_{S2} , Sense 1 = 0V		0.7		μA
	$-I_{S2}$, Sense 2 = 0V		0.7		μA
REFERENCE CURRENT Reference Current (I_{REF1}) Reference Currents Ratio	$I_{REF1} : I_{REF2}$	199	200	201 ± 0.5	μA %
DIGITAL INPUTS A_0, A_1, G, CLK, RST (74HC EQUIVALENT)					
High-Level Input Voltage		3.5			V
Low-Level Input Voltage				1.5	V
Input Rise and Fall Times (t_R, t_F)	CLK, \overline{RST} , A_0, A_1, G			450	ns
Pulse Width (t_W)	CLK, \overline{RST}	20			ns
Setup (t_{SU})	Data Change to CLK High	20			ns
Hold (t_{HO})	Data Change from CLK High	5			ns
Release (t_{REG})	\overline{RST} High to CLK High	5			ns
CLOCK SYNC CKI					
Input Voltage - High Level	$V_{CC} = 15V$	11			V
Input Voltage - Low Level	$V_{CC} = 15V$			4	V
Input Current - High Level	$V_{IL} = 11V, V_{CC} = 15V$		350		μA
Input Current - Low Level	$V_{IL} = 4V, V_{CC} = 15V$		350		μA
Input Frequency		45	50	55	KHz
Input Duty Cycle		45		55	%
TEMPERATURE RANGE					
Specification		0		70	$^\circ C$
Operating		0		70	$^\circ C$
Storage		-40		85	$^\circ C$
θ_{JA}			220		$^\circ C/W$
T_J max				150	$^\circ C$

NOTES: (1) See "High Voltage Testing" Section. (2) IMR is defined with respect to the voltage between Com 1 and Com 2 with both inputs tied to Com 1. (3) CMR is defined with respect to the input common, Com 1, only. (4) Deviation from a straight line between the end points of the output voltage. (5) Device output remains monotonic. (6) Limit referred to V_{REF1} .

PIN CONFIGURATION

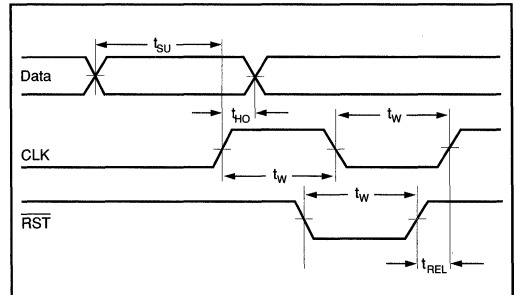
Bottom View	
1	10V Ref
2	$-V_{SS1}$
3	Sense 1
4	I_{REF1}
5	+In
6	-In
7	I_{REF2}
8	Sense 2
9	$+V_{SS1}$
10	Com 1
18	$V_{DD} (+5V)$
19	G
20	A_0
21	A_1
22	CLK
23	\overline{RST}
24	DCom 2
25	$V_{CC} (+15V)$
26	CKI
27	Com 2
28	Out

ABSOLUTE MAXIMUM RATINGS

Signal Input Voltage	$\pm 380V$
Analog Supply Voltage V_{CC}	18V
Digital Supply Voltage V_{DD}	7V
Voltage Across Barrier	800Vrms
Storage Temperature Range	$-45^\circ C$ to $+100^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$
Out Short Circuit Duration	Continuous to Com 2
Relative Humidity (non-condensing)	95% RH

NOTES: Stresses exceeding those listed above may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TIMING INFORMATION



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THEORY OF OPERATION

The ISC300 has no galvanic connection between the input and output sections. The differential input signal is multiplied by the programmable gain amplifier and accurately transferred across the isolation barrier to the output. The output section demodulates the signal transferred from the input section and transfers power to the input section.

ISC300 DESIGN

The ISC300 consists of:

- A filtered differential high impedance input.
- Precision matched current sources.
- Fault detect bias resistors.
- Digitally selectable internal calibration references.
- Digitally selectable gain.
- Isolation of all digital and analog signals.
- Isolated DC/DC converter.
- Synchronizable internal oscillator.
- Two isolated power supplies available for external circuitry.
- Externally available 10V reference.

INPUT SECTION

Filter

Since the ISC300 is designed to measure slowly changing processes, the input filter is set for a cut off frequency of 2Hz. This gives good noise rejection at power frequencies of 50Hz and 60Hz.

Sense Lines

The two sense lines can be configured to detect short or open circuits e.g. transducer burn out. This would be indicated by an out of range output (see Input Configuration in Applications section).

Multiplexer

The multiplexer is used to route either the measurement channel or the precision voltage references (used in system calibration) to the programmable gain amplifier.

Isolation Barrier

The isolation barrier consists of two transformers and three opto couplers. One transformer transmits the signal from the input side to the output side. The other transmits power from the output side to the input side. The opto-couplers are used to isolate the logic used for mux select, gain and reference voltage control.

Voltage Reference

The voltage reference provides 10V, 0.1V and 0V references for channel calibration. The 10V reference is also available externally.

Current References

Two matched 200 μ A current references are available for the excitation of RTDs or for use in external signal conditioning circuitry.

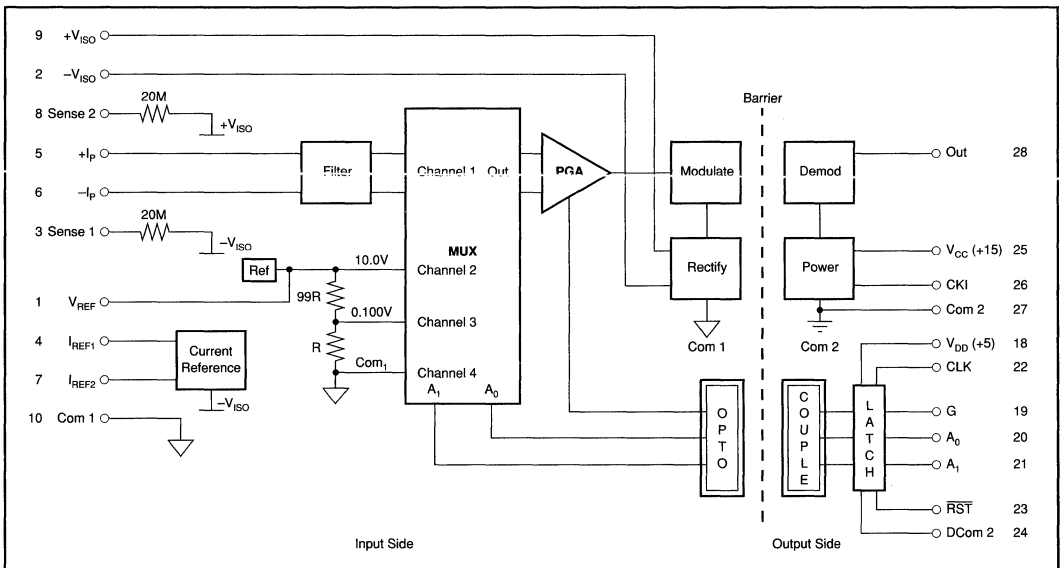


FIGURE 1. ISC300 Block Diagram.

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PGA

The programmable gain amplifier allows the user to digitally select device gains of 0.5 and 50, allowing input ranges of $\pm 0.1V$ or, $\pm 10V$ full scale. When used in conjunction with the 0.1V, 10V and common references, channel calibration can be performed.

Isolated Supplies

Two 13V isolated supplies, capable of supplying 5mA each, are available to power signal conditioning circuitry.

OUTPUT SECTION

The output section passes power across the isolation barrier to provide the isolated supplies, and demodulates the signal transmitted back across the isolation barrier.

ABOUT THE BARRIER

For any isolation product, barrier integrity is of paramount importance in achieving high reliability. The ISC300 uses miniature transformers designed to give maximum isolation performance when encapsulated in a high dielectric strength material. The device is designed so that the barrier is located at the center of the package.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses ($<5pC$) while applying 800Vrms, 60Hz high-voltage stress across every device isolation barrier. During a two second test partial discharge must occur five times on five separate half cycles of 60Hz, and each time occurrence must not be separated by a line period of more than four half cycles in order to produce a partial discharge fail. This confirms transient overvoltage ($1.6 \times V_{rated}$) protection without damage. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the “state-of-the-art” for nondestructive high voltage reliability testing. It is based on the effects of non-uniform fields existing in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of $0.01\mu s - 0.1\mu s$ current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the “inception voltage.” Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the “extinction voltage.”

We have designed and characterized the package to yield an inception voltage in excess of 800Vrms so that transient

overvoltages below this level will not cause any damage. The extinction voltage is above 500Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

As with any mixed signal analog and digital signal component, correct decoupling and signal routing precautions must be observed to optimize performance. The ISC300 has an internal $0.1\mu F$ decoupling capacitor at V_{CC} , so additional V_{CC} decoupling will not be necessary. However, a ground plane will minimize potential noise problems. If a low impedance ground plane is not used, Com 2 should be tied directly to the ground at the supply. It is not necessary to connect DCom 2 and Com 2 at the device. Layout practices associated with isolation signal conditioners are very important. The capacitance associated with the barrier and series resistance in the signal and reference leads must be minimized. Any capacitance across the barrier will increase AC leakage, and in conjunction with ground line resistance, may degrade high frequency IMR, see Figure 2.

INPUT CONFIGURATION

The ISC300 allows easy configuration for temperature measurement using an RTD. Figure 3 shows the basic connections for RTD operation. The two reference currents excite the resistance transducer and a current-to-voltage conversion is made corresponding to the resistance value of the transducer. If a gain of 50 is selected, a 10Ω resistance value results in a $(10 \cdot 200\mu A) \cdot 50 = 0.1V$ output; the 500Ω full scale value gives a $(500 \cdot 200\mu A) \cdot 50 = 5V$ output. The connection of the sense line allows open circuit sensor detection. An open circuit will give a corresponding $>5.1V$ output. A short circuit will give a corresponding $<0.1V$ output. See the Applications section under Fault Conditions for more information.

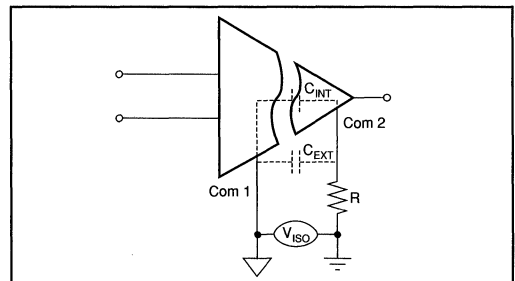


FIGURE 2. Barrier Capacitance.

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Figure 4 shows the configuration for voltage measurement. A full scale input range of $\pm 10\text{V}$ can be accepted by the ISC300. The two sense lines can be connected to give open or short circuit detection. An open circuit will result in an output of $< -5.1\text{V}$ and a short circuit will give a $< 0.1\text{V}$ output. See the Applications section under Fault Conditions for more information.

Figure 7 shows a possible circuit configuration using jumpers to select voltage or RTD operation.

ISOLATED SUPPLIES

The two isolated supplies available on the input side are capable of supplying $\pm 11.5\text{V}$ min at 5mA . These can be used to provide power for external front-end circuitry for additional signal processing. When using the isolated supplies, it is necessary to decouple them as close to the device as possible. $10\mu\text{F}$ tantalum capacitors should be used. This will also improve the signal-to-noise ratio.

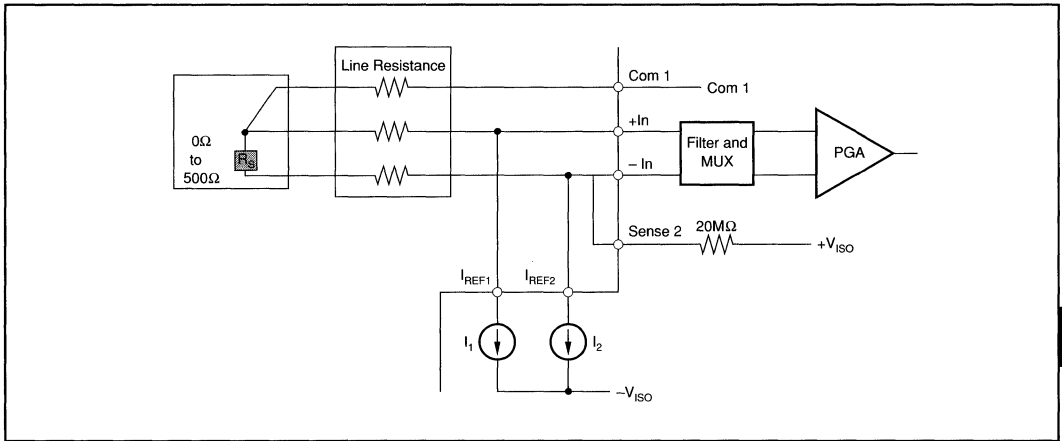


FIGURE 3. Resistance Measurement Configuration.

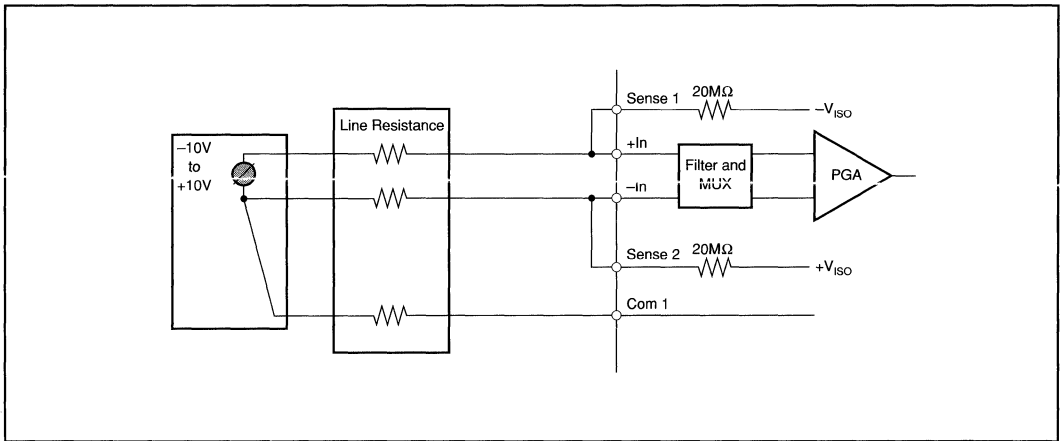


FIGURE 4. Voltage Measurement Configuration.

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MEASUREMENT CHANNEL

CALIBRATION

The ISC300 is designed to allow easy system calibration using its internal voltage reference. Programming pins A_0 , A_1 and G allows offset and full scale errors in gains of 0.5 and 50 to be measured.

INPUT SELECT	A_1	A_0	GAIN SELECT	G	SELECT AND GAIN	RST	CLK
Com 1	0	0	0.5	0	No Change	1	0
+0.1V	0	1	50	1	No Change	1	1
+10V	1	0			Latch	1	^
Signal	1	1			RESET	0	X

System calibration would typically proceed as follows:

Lab Calibration

- Set ISC300 gain.
- Set input to 0V reference, measure Offset.
- Connect external precision V reference, measure Gain.
- Remove external V reference and set input to 10V or 0.1V reference.

Offset and Gain are now calibrated to an external precision reference—record the numbers.

Field Calibration

- Set ISC300 gain.
- Set input to 0V reference, measure Offset.
- Set input to 10V or 0.1V, measure Gain.
- Recalibrate system.

SYNCHRONIZATION

As the internal modulation frequencies of several ISC300s can be marginally different, 'beat' frequencies ranging from a few Hz to a few kHz can exist in multi ISC300 applications. The internal clock (see Figure 5) starts when power is applied and runs at typically 50kHz. The ISC300 design accommodates 'internal synchronous' noise which is caused by minute timing differences, but synchronous beat frequency noise will not be strongly attenuated, especially at low frequencies if it is introduced via the power, signal or ground paths. To overcome this problem, the design allows the synchronization of each oscillator in the system to one frequency. This is done by connecting the CKI (clock in)

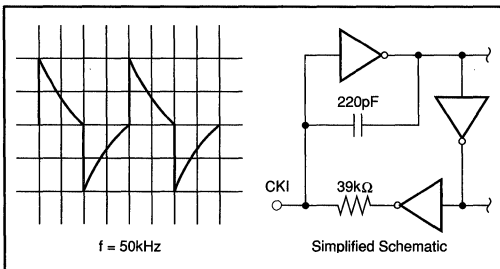


FIGURE 5. CKI Input.

pins of each ISC300 in the system together (see Figure 6). The ISC300 can also be synchronized by an external clock driver.

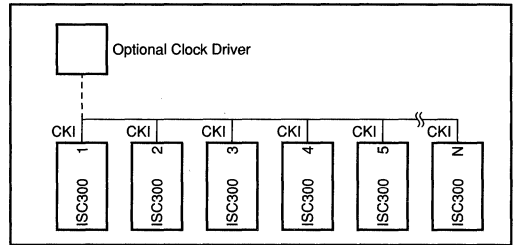


FIGURE 6. Synchronizing Multi-ISC300 Applications.

NOISE

Output noise is generated by the residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 15 for an example of a 2 pole filter with amplification, giving a $\pm 10V$ output). The filter time constants should be set below the carrier frequency. The output of the ISC300 is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than $1M\Omega$ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform.

APPLICATIONS

This section describes the design criteria of various applications of the ISC300.

2, 3 AND 4 WIRE RESISTANCE MEASUREMENTS

Two wire resistance measurements are prone to errors due to lead resistances. The voltage error can be significant since the voltmeter measures on the lines supplying the RTD

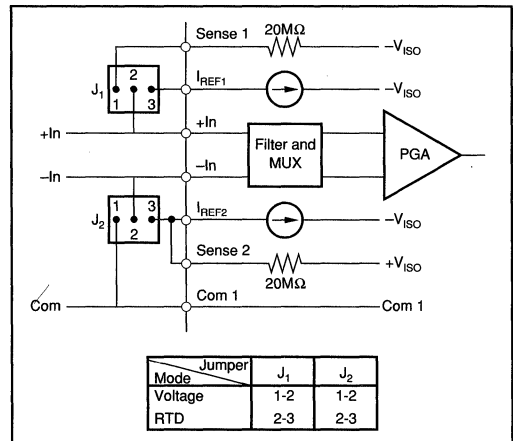


FIGURE 7. Mode Selection Jumpers.

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excitation current. Four wire measurements avoid this problem by measuring the voltage generated across the RTD on a second pair of wires. Very little current flows through the voltmeter, therefore the lead resistance error contribution is negligible. Three wire resistance measurements also avoid lead length resistance errors.

In Figure 8:

$$(+In) = -r_1 (I_1 + I_2) - r_2 I_1 \quad (1)$$

$$(-In) = -r_1 (I_1 + I_2) - R_2 I_2 - r_3 I_2 \quad (2)$$

(1) - (2)

$$= -r_2 I_2 + R_2 I_2 + r_3 I_2$$

Since $r_1 = r_2 = r_3$ (LEADS) and $I_1 = I_2$

$$V_{IN} = R_S I_2$$

FAULT CONDITIONS

The ISC300 can be configured to detect line or transducer faults which may occur in a system. Figures 8 to 14 show how the output of the ISC300 will reflect these various fault conditions by giving corresponding out of range outputs.

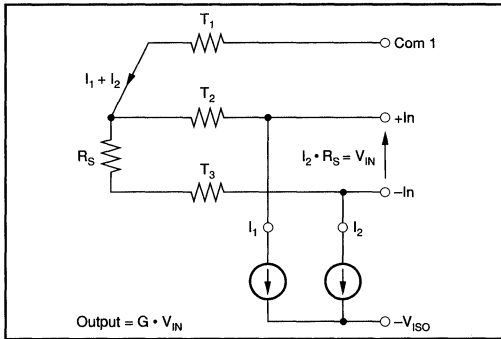


FIGURE 8. Normal Operation.

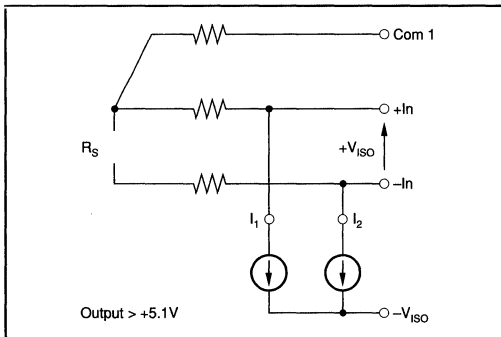


FIGURE 9. R_S Open Circuit.

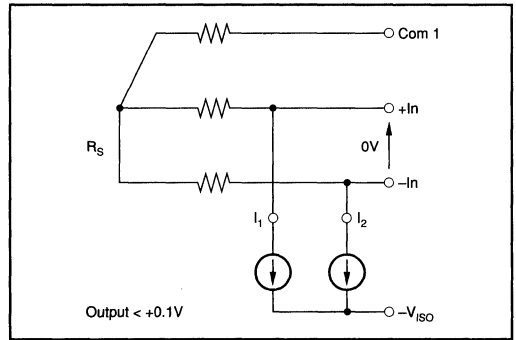


FIGURE 10. R_S Short Circuit.

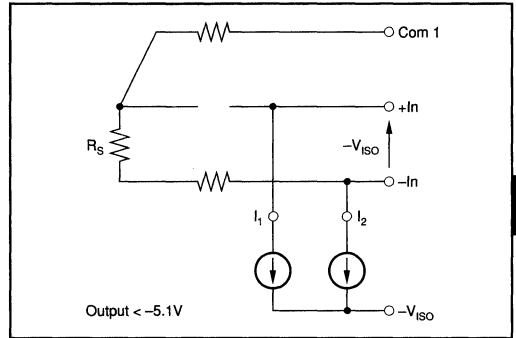


FIGURE 11. +In Open Circuit.

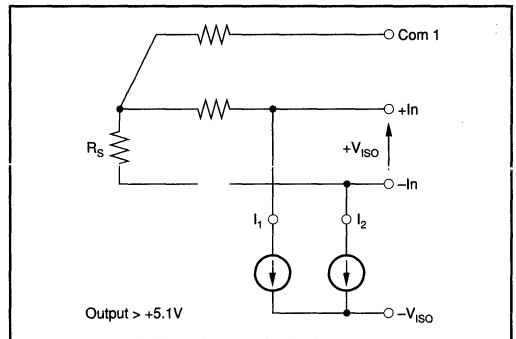


FIGURE 12. -In Open Circuit.

ISC300

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ISOLATION PRODUCTS

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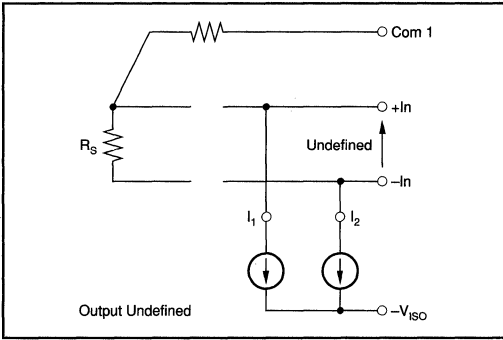


FIGURE 13. -In and +In Open Circuit.

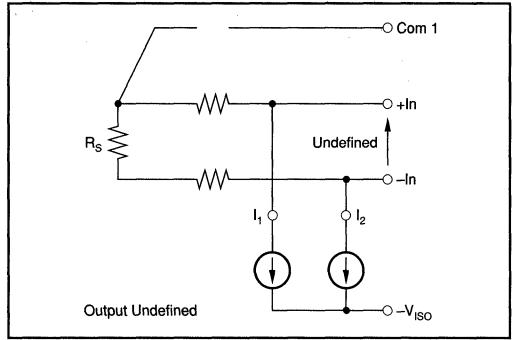


FIGURE 14. Com 1 Open Circuit.

APPLICATIONS FLEXIBILITY

ISOLATED VOLTAGE MEASUREMENT CHANNEL

Figure 15 shows the ISC300 configured for a $\pm 10\text{V}$ input. With a few external components the ISC300 can accurately convert a $\pm 10\text{V}$ input to an isolated $\pm 10\text{V}$ output with no external adjustments. The primary function of the output circuitry is to add gain to convert the $\pm 5\text{V}$ output of the ISC300 to $\pm 10\text{V}$, and to reduce output impedance. The addition of a few resistors and capacitors provides an active low pass filter with a cut off frequency of typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at -12dB per octave.

ISOLATED MEASUREMENT BRIDGE CIRCUIT

Figure 16 shows a measurement bridge circuit using the ISC300. All the input circuitry is powered by the ISC300 isolated supplies. The OPA1013 dual op amp is used to

excite the measurement bridge and the INA102 is used to amplify the bridge delta voltage. Connecting pins 4 and 7 together, and pins 5 and 6 together on the INA102 sets its gain to 1000.

ISOLATED 4 TO 20MA RECEIVER

In Figure 17, the ISC300 converts a 4 to 20mA current to an isolated 0 to 5V output. The 6.25Ω resistor converts the 4 to 20mA input to 0.025 to 0.125V. The 125Ω resistor in conjunction with the $200\mu\text{A}$ current source provides an offset of -0.025V . Fine offset and gain adjustment gives an accurate 0 to 0.1V input range.

Offset and Gain Adjustment

- Adjust R_1 for 5V change on the output corresponding to 16mA change on the input.
- Adjust R_2 with 4mA input for 0V output.

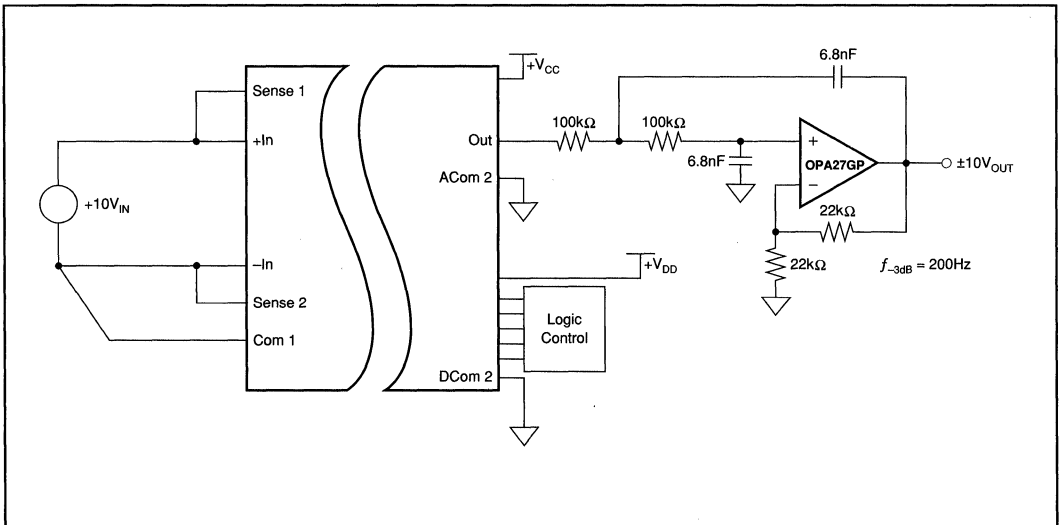


FIGURE 15. Isolated Voltage Measurement Channel with Output Filter.

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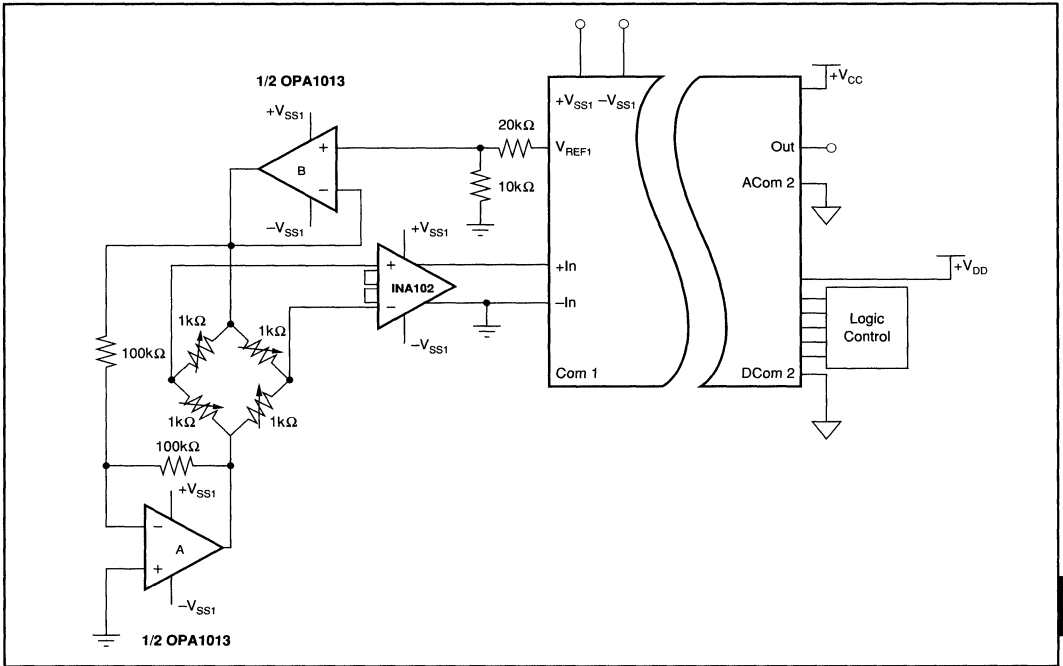


FIGURE 16. Isolated Instrument Bridge System.

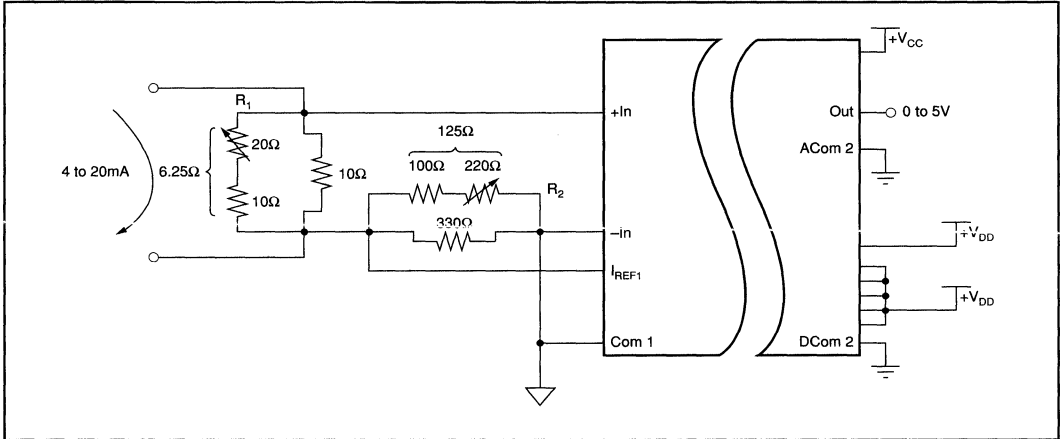


FIGURE 17. Isolated 4 to 20mA receiver (0 to 5V output).

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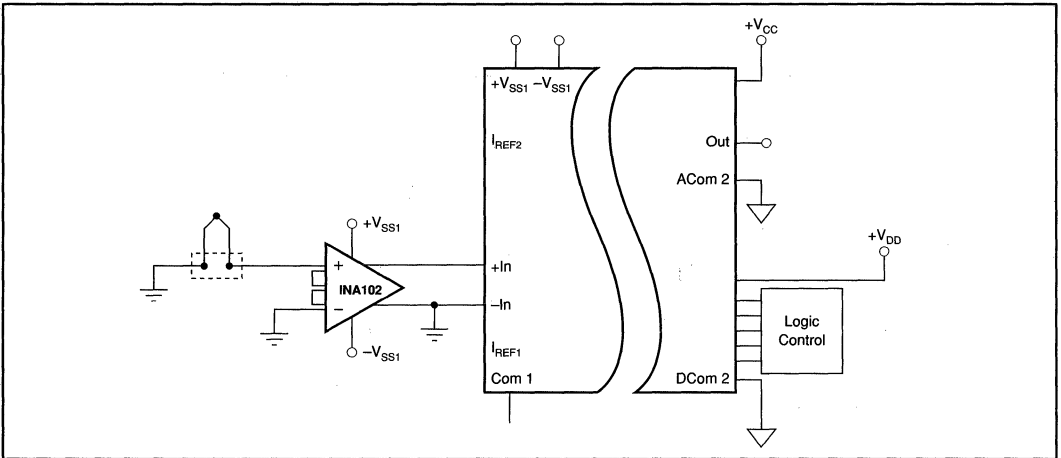


FIGURE 18. Temperature Measurement Using Thermocouple with Small Span.

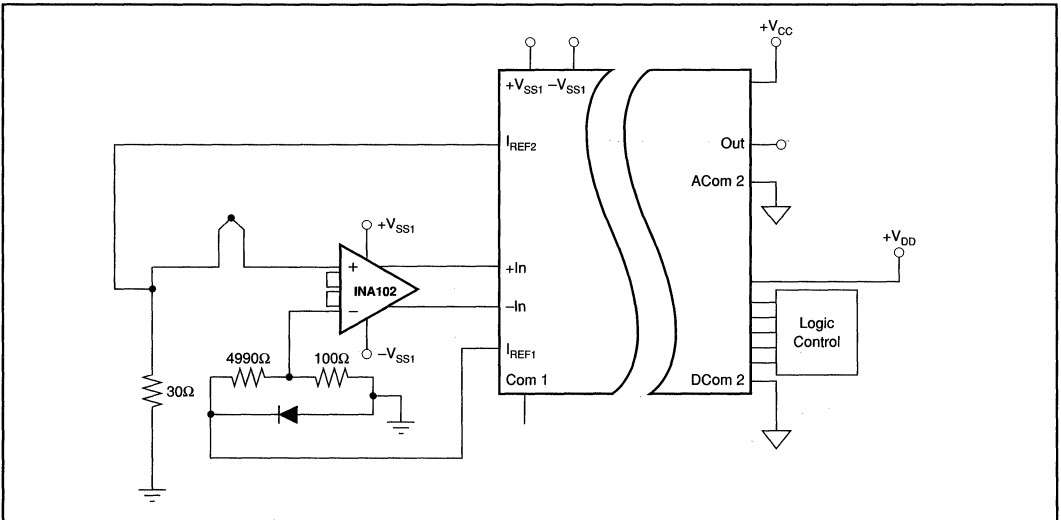
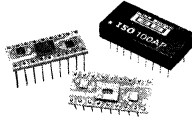


FIGURE 19. Thermocouple with Cold Junction Compensation.

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ISO100

Optically-Coupled Linear ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
 $V_{OUT}/I_{IN} = R_F$, Current Input
 $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- 100% TESTED FOR BREAKDOWN:
750V Continuous Isolation Voltage
- ULTRA-LOW LEAKAGE: 0.3 μ A, max, at
240V/60Hz
- WIDE BANDWIDTH: 60kHz
- 18-PIN DIP PACKAGE

DESCRIPTION

The ISO100 is an optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3 μ A at 250V. Voltage input operation is easily achieved by using one external resistor.

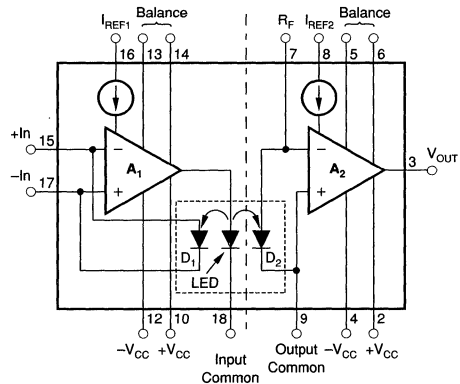
Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
Transducer Sensing
(Thermocouples, RTD, Pressure Bridges)
4mA to 20mA Loops
Motor and SCR Control
Ground Loop Elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

(see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_F$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $\pm V_{CC} = 15\text{VDC}$, unless otherwise specified.

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION											
Voltage											
Rated Continuous, AC peak or DC ⁽¹⁾		750			*			*			V
Test Breakdown, DC	10s	2500			*			*			V
Rejection ⁽²⁾ DC			5		*	*		*	*		pA/V
	$R_{IN} = 10\text{k}\Omega$, Gain = 100		146		*	*		*	*		dB
	60Hz, 480V, $R_F = 1\text{M}\Omega$		400		*	*		*	*		pA/V
AC	$R_{IN} = 10\text{k}\Omega$, Gain = 100		108		*	*		*	*		dB
Impedance			$10^{12} 2.5$		*	*		*	*		$\Omega \mu\text{F}$
Leakage Current	240Vrms, 60Hz			0.3			*			*	μA , rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	$\mu\text{V}/^\circ\text{C}$
vs Input Power Supplies				105			*			*	dB
vs Time			1		*			*		*	$\mu\text{V}/\text{kHz}$
Output Stage (V_{OSO})											
Initial Offset				500			300			200	μV
vs Temperature				5			2			2	$\mu\text{V}/^\circ\text{C}$
vs Output Power Supplies				105			*			*	dB
vs Time			1		*			*		*	$\mu\text{V}/\text{kHz}$
Common-Mode Rejection Ratio ⁽²⁾	60Hz, $R_F = 1\text{M}\Omega$		3		*	*		*	*	*	nA/V
	$R_{IN} = 10\text{k}\Omega$, Gain = 100		90		*	*		*	*	*	dB
Common-Mode Range		± 10			*			*		*	V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10.5	12	12.5	*	*	*	*	*	*	μA
vs Temperature				300	*	*	*	*	*	150	$\text{ppm}/^\circ\text{C}$
vs Power Supplies			0.3	3	*	*	*	*	*	*	nA/V
Matching											
Nominal			50		*	*	*	*	*	*	nA
vs Temperature			150		*	*	*	*	*	*	$\text{ppm}/^\circ\text{C}$
vs Power Supplies			0.3		*	*	*	*	*	*	nA/V
Compliance Voltage		-10		+15	*	*	*	*	*	*	V
Output Resistance			2×10^9		*	*	*	*	*	*	Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/ μA		60		*	*	*	*	*	*	kHz
Full Power Bandwidth	Gain = 1V/ μA , $V_O = \pm 10\text{V}$		5		*	*	*	*	*	*	kHz
Slew Rate		0.22	0.31		*	*	*	*	*	*	V/ μs
Settling Time	0.1%		100		*	*	*	*	*	*	μs
TEMPERATURE RANGE											
Specification		-25		+85	*	*	*	*	*	*	$^\circ\text{C}$
Operating		-40		+100	*	*	*	*	*	*	$^\circ\text{C}$
Storage		-55		+100	*	*	*	*	*	*	$^\circ\text{C}$
UNIPOLAR OPERATION											
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-20		-0.02	*	*	*	*	*	*	μA
Without Damage		-1		+1	*	*	*	*	*	*	mA
Input Impedance			0.1		*	*	*	*	*	*	Ω
Output Voltage Swing	$R_L = 2\text{k}\Omega$, $R_F = 1\text{M}\Omega$	-10		0	*	*	*	*	*	*	V
Output Impedance	DC, Open-Loop		1200		*	*	*	*	*	*	Ω
GAIN											
Initial Error (adjustable to zero)	$V_O = R_F (I_{IN})$		2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.07		0.01	0.05		0.005	0.03	$\%/^\circ\text{C}$
vs Time			0.05			*			*		%/kHz
Nonlinearity ⁽³⁾			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE											
0.01Hz to 10Hz	$I_{IN} = 0.2\mu\text{A}$		20			*			*		pAp-p
10Hz			1			*			*		pA/ $\sqrt{\text{Hz}}$
100Hz			0.7			*			*		pA/ $\sqrt{\text{Hz}}$
1kHz			0.65			*			*		pA/ $\sqrt{\text{Hz}}$

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SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $\pm V_{CC} = 15\text{VDC}$, unless otherwise specified.

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
INPUT OFFSET CURRENT (I_{OS}) Initial Offset vs Temperature vs Power Supplies vs Time			1	10		*	*		*	*	nA	
			0.05			*			*		nA/ $^\circ\text{C}$	
			0.1			*			*		nA/V	
			100			*			*		pA/kHr	
POWER SUPPLIES Input Stage Voltage (rated performance) Voltage (derated performance) Supply Current Output Stage Voltage (rated performance) Voltage (derated performance) Supply Current Short Circuit Current Limit	$I_{IN} = -0.02\mu\text{A}$ $I_{IN} = -20\mu\text{A}$	± 7	± 15	± 18	*	*	*	*	*	*	V	
			± 1.1	± 2	*	*	*	*	*	*	mA	
			+8, -1.1	+13, -2	*	*	*	*	*	*	mA	
	$V_O = 0$	± 7	± 15	± 18	*	*	*	*	*	*	V	
			± 1.1	± 2	*	*	*	*	*	*	V	
												mA
												mA
												mA
BIPOlar OPERATION												
GENERAL PARAMETERS Input Current Range Linear Operation Without Damage Input Impedance Output Voltage Swing Output Impedance	$R_L = 2\text{k}\Omega, R_F = 1\text{M}\Omega$	-10		+10	*	*	*	*	*	*	μA	
		-1		+1	*	*	*	*	*	*	mA	
			0.1			*	*	*	*	*	*	Ω
			-10		+10	*	*	*	*	*	*	V
				1200			*	*	*	*	*	Ω
GAIN Initial Error (Adjustable To Zero) vs Temperature vs Time Nonlinearity ⁽³⁾	$V_O = R_F (I_{IN})$		2	5		1	2		1	2	% of FS	
			0.03	0.07		0.01	0.05		0.005	0.03	%/ $^\circ\text{C}$	
			0.05			*			*			%/kHr
			0.1	0.4		0.03	0.1		0.02	0.07	%	
CURRENT NOISE 0.01Hz to 10Hz 10Hz 100Hz 1kHz	$I_{IN} = 0.2\mu\text{A}$		1.5			*			*		nA, p-p	
			17			*			*		pA/ $\sqrt{\text{Hz}}$	
			7			*			*		pA/ $\sqrt{\text{Hz}}$	
			6			*			*		pA/ $\sqrt{\text{Hz}}$	
INPUT OFFSET CURRENT (I_{OS}, bipolar⁽⁴⁾) Initial Offset vs Temperature vs Power Supplies vs Time			40	200		20	70		10	35	nA	
				3			*	*		*		nA/ $^\circ\text{C}$
				0.7			*	*		*		nA/V
				250			*	*		*		pA/kHr
POWER SUPPLIES Input Stage Voltage (rated performance) Voltage (derated performance) Supply Current Output Stage Voltage (rated performance) Voltage (derated performance) Supply Current Short Circuit Current Limit	$I_{IN} = +10\mu\text{A}$ $I_{IN} = -10\mu\text{A}$	± 7	± 15	± 18	*	*	*	*	*	*	V	
			+2, -1.1	+3, -2	*	*	*	*	*	*	mA	
			+8, -1.1	+13, -2	*	*	*	*	*	*	mA	
	$V_O = 0$	± 7	± 15	± 18	*	*	*	*	*	*	V	
			± 1.1	± 2	*	*	*	*	*	*	V	
												mA
												mA
												mA

* Same as ISO100AP.

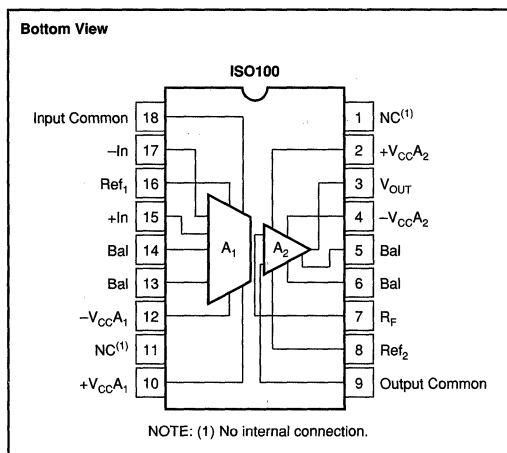
NOTES: (1) See Typical Performance Curves for temperature effects. (2) See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors. (3) Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output. (4) Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage, AC pk or DC	750V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-circuit Duration	Continuous to ground

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO100AP	18-Pin Bottom-Braze DIP	220
ISO100BP	18-Pin Bottom-Braze DIP	220
ISO100CP	18-Pin Bottom-Braze DIP	220

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

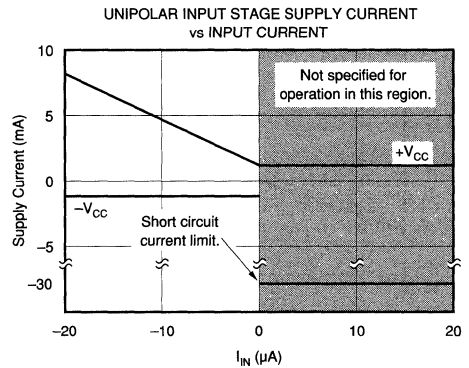
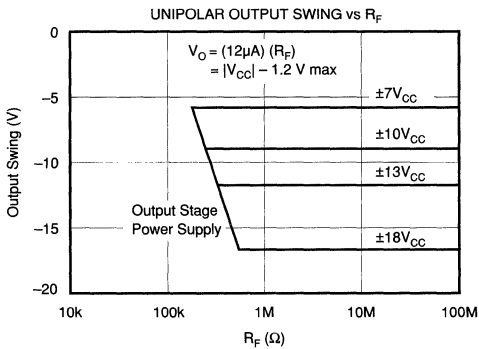
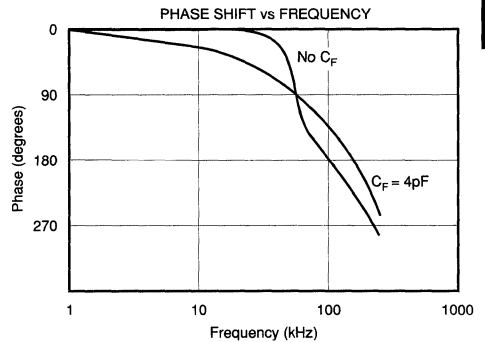
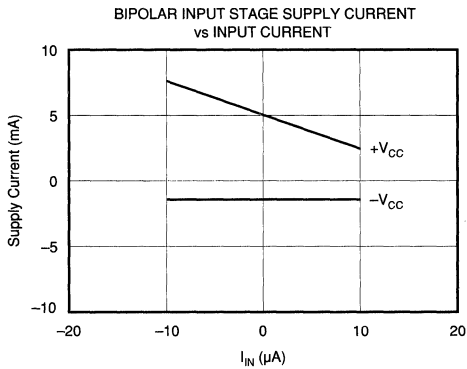
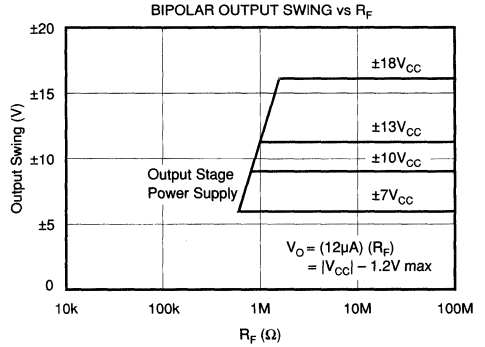
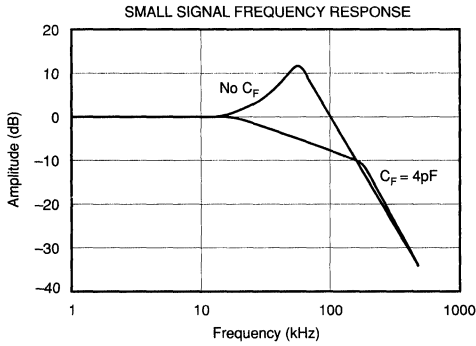
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ISO100AP	18-Pin Bottom-Braze DIP	-25°C to +85°C
ISO100BP	18-Pin Bottom-Braze DIP	-25°C to +85°C
ISO100CP	18-Pin Bottom-Braze DIP	-25°C to +85°C

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise specified.



ISO100

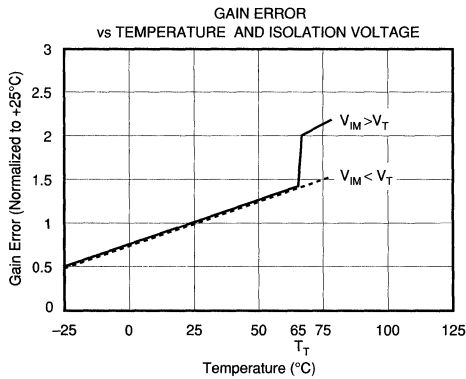
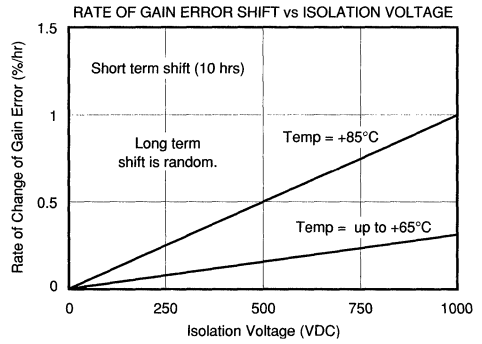
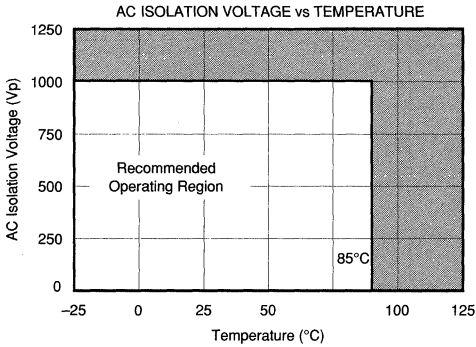
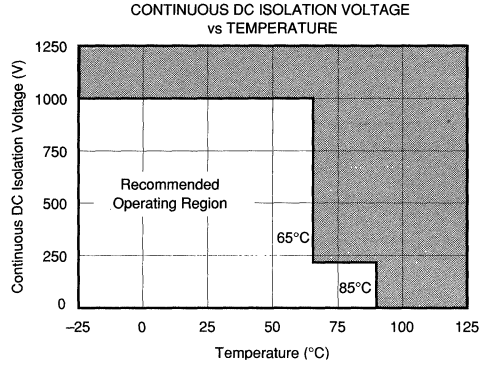
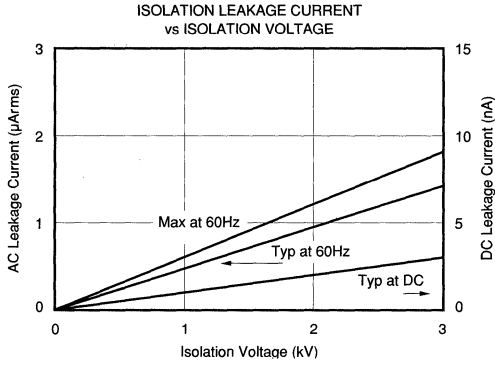
5

ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise specified.



NOTES: V_T and T_T approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.
 $T_T = +65^\circ\text{C}$, $V_T = 200\text{VDC}$. Shift does not occur for AC voltages.

V_M = Isolation-Mode Voltage
 V_T = Threshold Voltage
 T_T = Threshold Temperature

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THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications, an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors coupled together to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation to generate a midscale reference. The LED and photodiodes (D_1 and D_2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A_1 occurs through the optical path formed by the LED and D_1 . The signal is transferred across the isolation barrier by the matched light path to D_2 .

The overall isolation amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN} , flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A_1 increases, driving current through

the LED. As the LED light output increases, D_1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node ($-Input$ to A_1) is zero. At that point, the negative feedback through D_1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result, no bias current flows in the source. Since D_1 and D_2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D_2 . Thus, A_1 functions as a unity-gain current amplifier, and A_2 is a current-to-voltage converter, as described below.

Current produced by D_2 must either flow into A_2 or R_F . Since A_2 is designed for low bias current ($\approx 10nA$), almost all of the current flows through R_F to the output. The output voltage then becomes:

$$V_O = (I_{D2})R_F = (I_{D1} \pm I_{OS})R_F \approx -(-I_{IN})R_F = I_{IN}R_F \quad (1)$$

where, I_{OS} is the difference between A_1 and A_2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}), since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A_1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met, the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1 are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation.

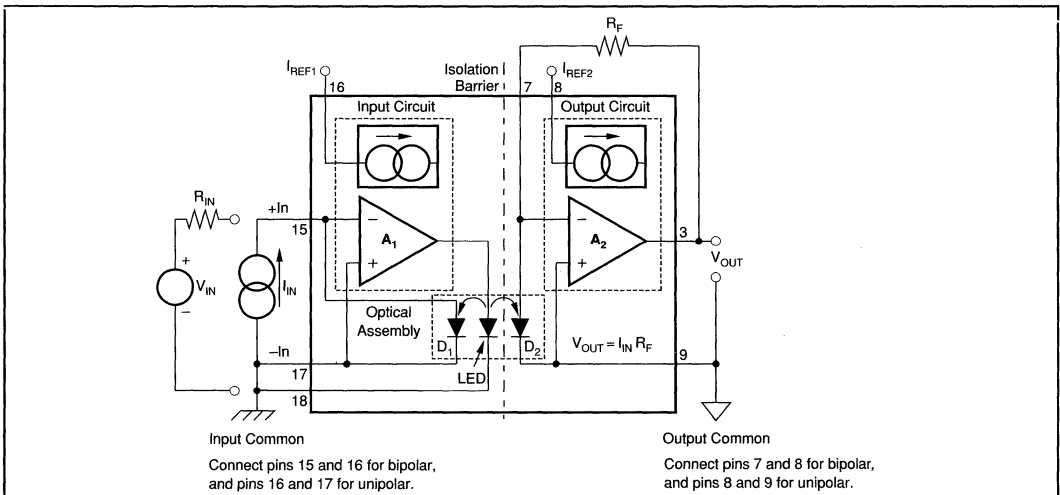


FIGURE 1. Simplified Block Diagram of the ISO100.

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Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D_2 will equal I_{REF2} . This results in no current flow in R_F , and the output voltage will be zero. When I_{IN} either adds or subtracts current from the input node, the current D_1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2} , a current equal to I_{IN} will flow in R_F . The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5 μ A, min). At this point, D_1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D_1 with maximum LED output (recommended 10 μ A, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

A_1 and A_2 —assumed to be ideal amplifiers.

V_{OSO} and V_{OSI} —the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI} \frac{R_F}{R_{IN}}, \quad (1)$$

see equation (2).

I_{OS} —the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A_1 and A_2 and the matching errors in the optical components in the unipolar mode.

I_{REF1} and I_{REF2} —reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS \text{ BIPOLAR}}$ error.

I_{D1} and I_{D2} —currents generated by each photodiode in response to the light from the LED.

A_e —gain error.

$$A_e = | \text{Ideal gain/Actual gain} | - 1$$

The output then becomes:

$$V_{OUT} = R_F \left[\left(\frac{V_{IN} \pm V_{OS}}{R_{IN}} - I_{REF1} \pm I_{OS} \right) (1 + A_e) + I_{REF2} \right] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified in the unipolar case by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F \left[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS \text{ UNIPOLAR}} \right] \pm V_{OSO} \quad (3)$$

This voltage is then referred back to the input by dividing by R_F/R_{IN} .

$$V_{OS(RTI)} = (\pm V_{OSI}) \pm R_{IN} (I_{OS \text{ UNIPOLAR}}) + V_{OSO} (R_F/R_{IN}) \quad (4)$$

Example 1. Refer to Figure 2 and Electrical Specifications Table.

Given: $I_{OS \text{ BIPOLAR}} = +35\text{nA}$

$$R_{IN} = 100\text{k}\Omega$$

$$R_F = 1\text{M}\Omega \text{ (gain} = 10\text{)}$$

$$V_{OSI} = +200\mu\text{V}$$

$$V_{OSO} = +200\mu\text{V}$$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0\text{V}$.

V_{OS} total RTI

$$\begin{aligned} &= \{ [\pm V_{OSI} \pm R_{IN} (I_{OS \text{ BIPOLAR}}) - R_{IN} (I_{REF1})] \\ & \quad [1 + A_e] + R_{IN} I_{REF2} \} \pm V_{OSO} / (R_F/R_{IN}) \\ &= \{ [+200\mu\text{V} + 100\text{k}\Omega (35\text{nA}) - 100\text{k}\Omega (12.5\mu\text{A})] \\ & \quad [1.02] + 100\text{k}\Omega (12.5\mu\text{A}) \} + \\ & \quad 200\mu\text{V} / (1\text{M}\Omega/100\text{k}\Omega) \\ &= \{ [0.2\text{mV} + 3.5\text{mV} - 1.25\text{V}] \\ & \quad [1.02] + 1.25\text{V} \} + 0.02\text{mV} \\ &= -21.2\text{mV} \end{aligned}$$

V_{OS} total RTO

$$\begin{aligned} &= V_{OS} \text{ total RTI} \times R_F/R_{IN} \\ &= -21.2\text{mV} \times 10 \\ &= -212\text{mV} \end{aligned}$$

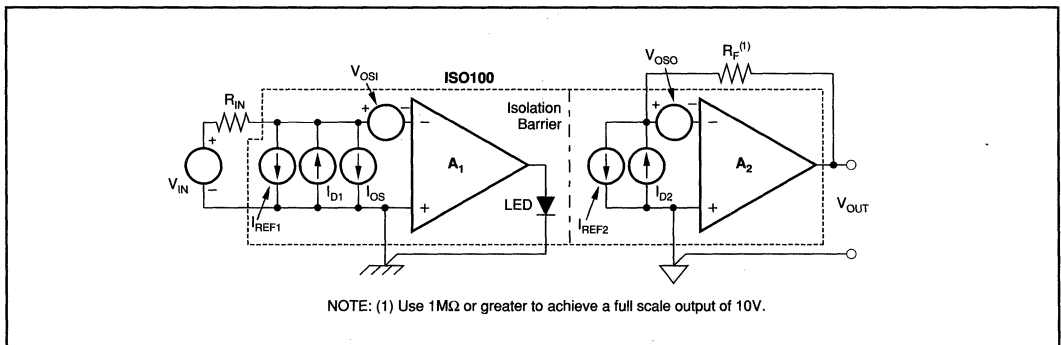


FIGURE 2. Circuit Model for DC Errors in the ISO100.

NOTE: This error is dominated by $I_{OS\ BIPOLAR}$ and the reference current times the gain error (which appears as an offset). The error for unipolar operation is much lower. The error due to offset current can be zeroed using circuits shown in Figures 6 and 7. The gain error is adjusted by trimming either R_F or R_{IN} .

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

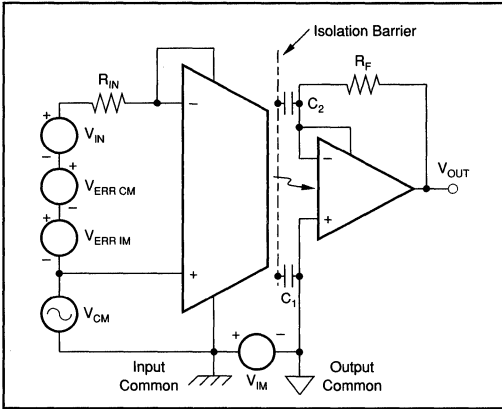


FIGURE 3. High Voltage Error Model.

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$CMRR\ (I\text{-mode}) = \frac{\Delta I_{OS}}{\Delta V_{CM}}\ \text{in}\ nA/V \tag{5}$$

$$CMRR\ (V\text{-mode}) = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}} \right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}}\ \text{in}\ V/V \tag{6}$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output to zero:

$$IMRR\ (I\text{-mode}) = \frac{\Delta I_{OS}}{\Delta V_{IM}}\ \text{in}\ pA/V \tag{7}$$

$$IMRR\ (V\text{-mode}) = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}} \right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}}\ \text{in}\ V/V \tag{8}$$

CMRR and IMRR in V/V are a function of R_{IN} .

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM} .

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

Total Capacitance (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2. Refer to Figure 3 and Electrical Specification Table.

Given: $V_{CM} = 1VAC$ peak at 60Hz, $V_{IM} = 200VDC$,
 CMRR = 3nA/V, IMRR = 5pA/V,
 $R_{IN} = 100k\Omega$, $R_F = 1M\Omega$
 (Gain = 10)

Find: The error voltage referred to the input and output when $V_{IN} = 0V$

$$\begin{aligned} V_{ERR\ RTI} &= (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN}) \\ &= 1V (3nA/V)(100k\Omega) \\ &\quad + 200V (5pA/V)(100k\Omega) \\ &= 0.3mV + 0.1mV \\ &= 0.4mV \end{aligned}$$

$$\begin{aligned} V_{ERR\ RTO} &= V_{ERR\ RTI} (R_F/R_{IN}) \\ &= 0.4mV (10) \\ &= 4mV\ \text{(with DC IMRR)} \end{aligned}$$

NOTE: This error is dominated by the CMRR term.

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

$$\begin{aligned} CMRR\ \text{in}\ V/V &= CMRR\ (I\text{-mode})(R_{IN}) \\ &= 3nA/V (100k\Omega) = 0.3mV/V \end{aligned}$$

$$CMR = 20\ LOG\ (0.3mV/V) = -70dB\ \text{at}\ 60Hz$$

$$\begin{aligned} IMRR\ \text{in}\ V/V &= IMRR\ (I\text{-mode})(R_{IN}) = 5pA/V(100k\Omega) \\ &= 0.5\mu V/V \end{aligned}$$

$$IMR = 20\ LOG\ (0.5 \times 10^{-6}V/V) = -126dB\ \text{at}\ DC$$

Example 3.

In Example 3, V_{IM} is an AC signal at 60Hz and

$$IMRR = 400pA$$

$$\begin{aligned} V_{ERR\ RTI} &= V_{ERR\ CM} + V_{ERR\ IM} \\ &= 0.3mV + 200V (400pA/V)(100k\Omega) \\ &= 8.3mV \end{aligned}$$

$$V_{ERR\ RTO} = 83mV\ \text{(with AC IMRR)}$$

Example 4.

Given: Total error RTO from Examples 1 and 3 as 378mV worst case.

Find: Percent error of +10V full scale output

$$\begin{aligned} \% \text{ Error} &= \frac{V_{\text{ERR TOTAL}}}{V_{\text{FS}}} \times 100\% \\ &= \frac{378\text{mV}}{10\text{V}} \times 100\% \\ &= 3.78\% \end{aligned}$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F , in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

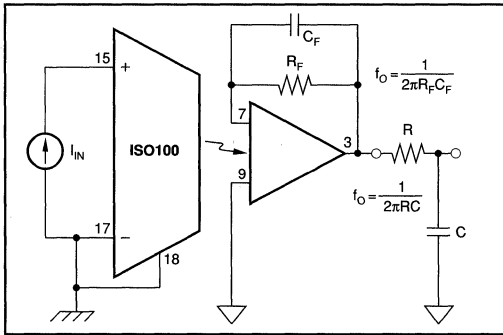


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

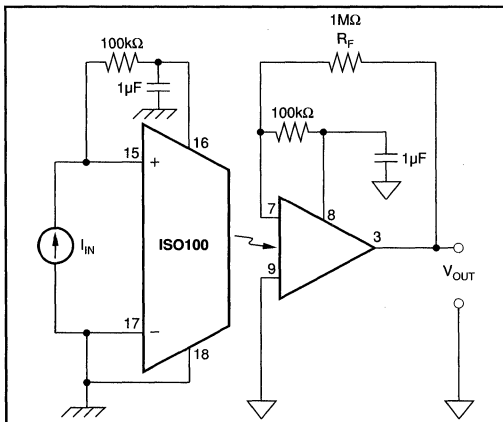


FIGURE 5. Circuit Techniques for Reducing Noise from the Current Sources in the Bipolar Mode.

OPTIONAL ADJUSTMENTS

There are two major sources of offset error: offset voltage and offset current. V_{OS1} and V_{OSO} of the input and output amplifiers can be adjusted independently using external potentiometers. An example is shown in Figure 17. Note that V_{OSO} (500 μ V, max) appears directly at the output, but V_{OS1} appears at the output multiplied by gain (R_F/R_{IN}). In general, V_{OS} is small compared to the effect of I_{OS} (see Example 1). To adjust for I_{OS} use a circuit which intentionally unbalances the offset in one direction and then allows for adjustment back to zero.

Figure 6 shows how to adjust unipolar errors at zero input. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R_5 and R_6 , the minimum current required to keep the input stage in the linear region of operation can be established. R_7 and R_8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. Although the amplifier can now operate down to zero input voltage, it has only a small portion of the current drain and noise that the true bipolar configuration would have.

Adjusting the bipolar errors is illustrated in Figure 7. Each of the errors are adjusted in turn. With V_{IN} = "open," I_{OS} is trimmed by adjusting R_{10} to make the output zero. R_G is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R_{14} .

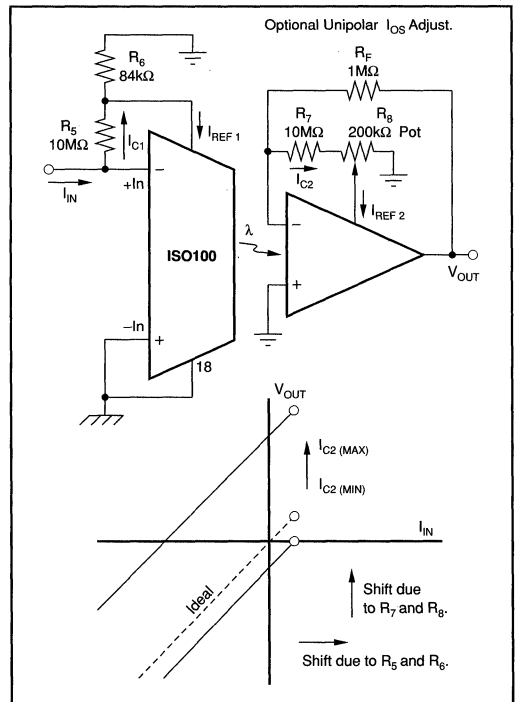


FIGURE 6. Adjusting the Unipolar Amplifier Errors at Zero Input.

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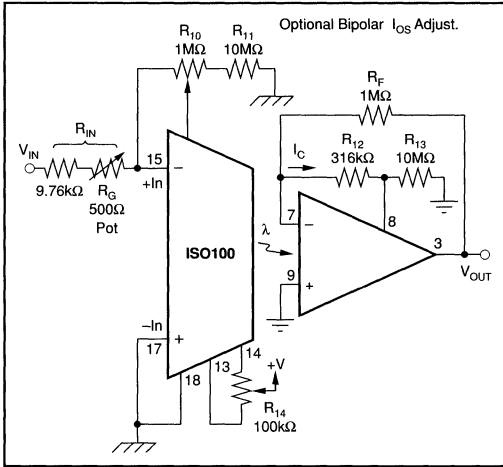


FIGURE 7. Adjusting the Bipolar Errors.

BASIC CIRCUIT CONNECTIONS

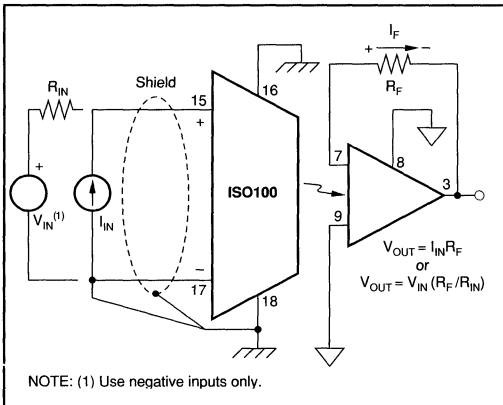


FIGURE 8. Unipolar Noninverting.

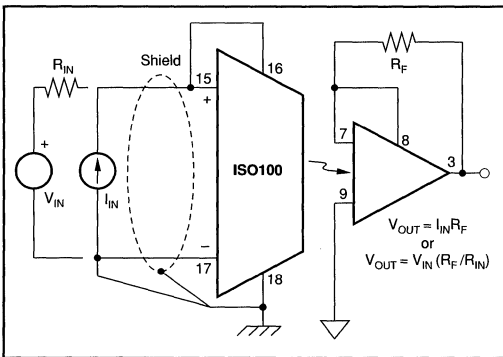


FIGURE 9. Bipolar Noninverting.

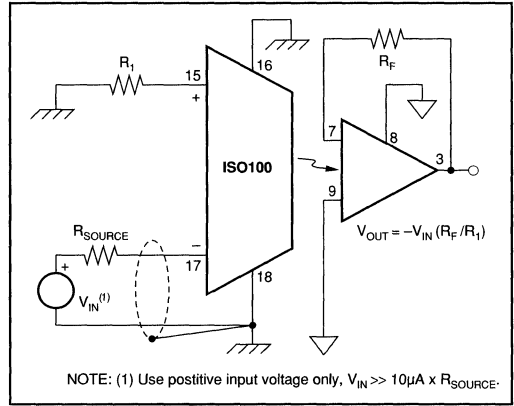


FIGURE 10. Unipolar Inverting.

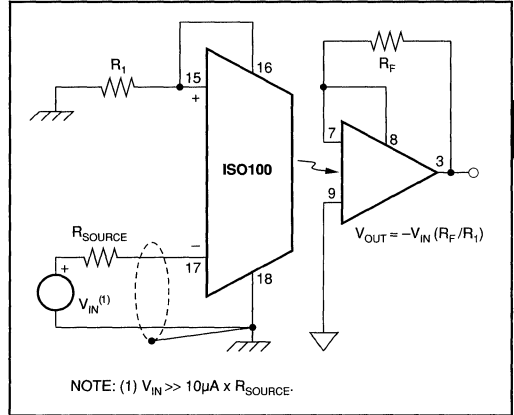


FIGURE 11. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -In (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input.
2. Use shielded or twisted pair cable at the input for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.

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4. The distance across the isolation barrier, between external components and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F .

$$V_{SWING} = I_{IN\ MAX} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figure 12 through 18 show applications of the ISO100.

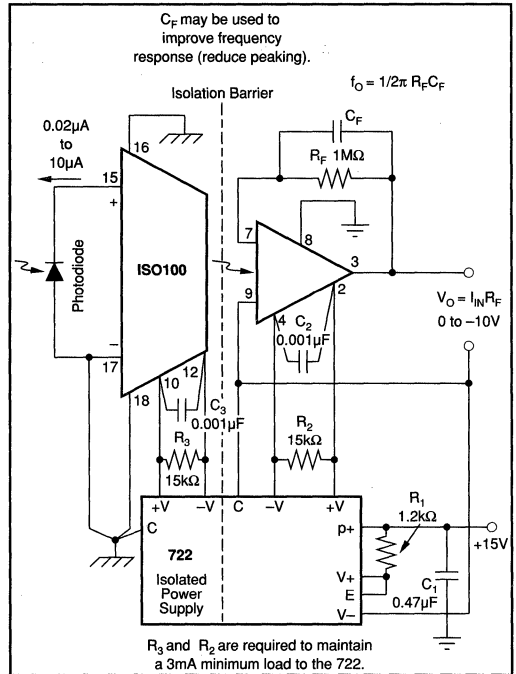


FIGURE 12. Two-Port Isolation Photodiode Amplifier Unipolar.

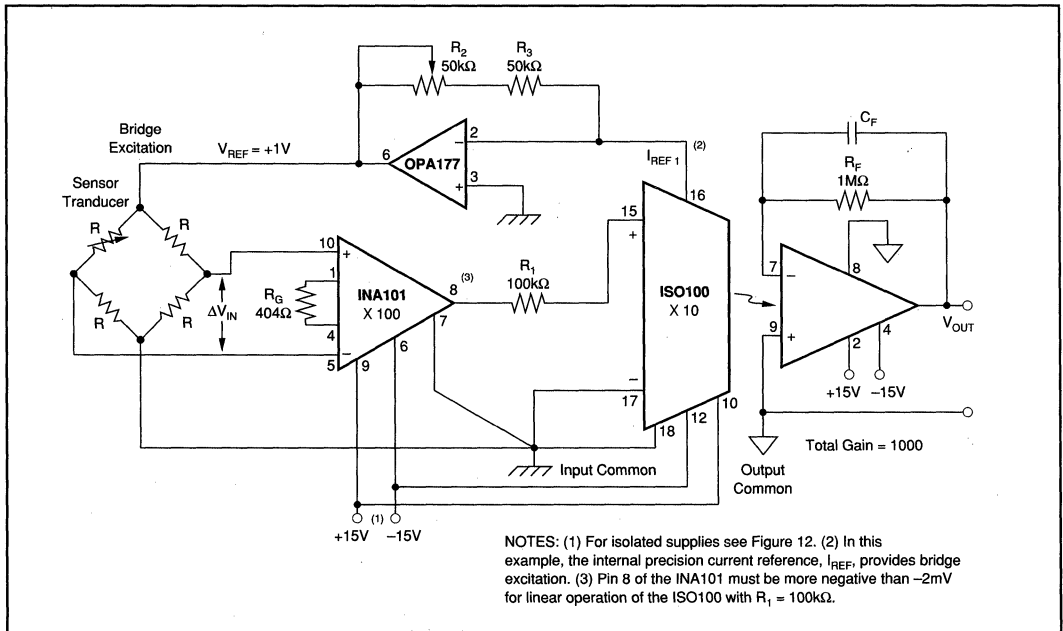


FIGURE 13. Precision Bridge Isolation Amplifier (Unipolar).

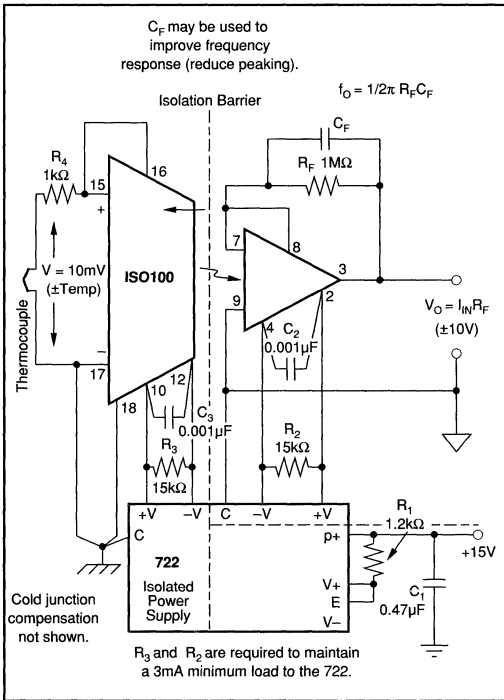


FIGURE 14. Three-Port Isolation Thermocouple Amplifier (Bipolar).

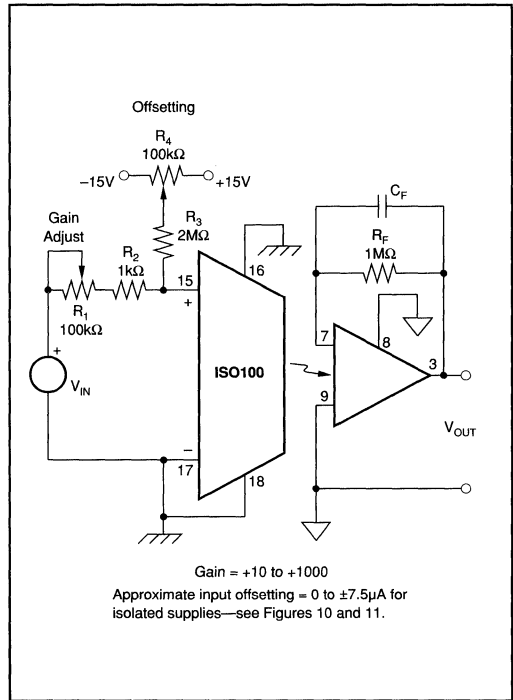


FIGURE 15. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

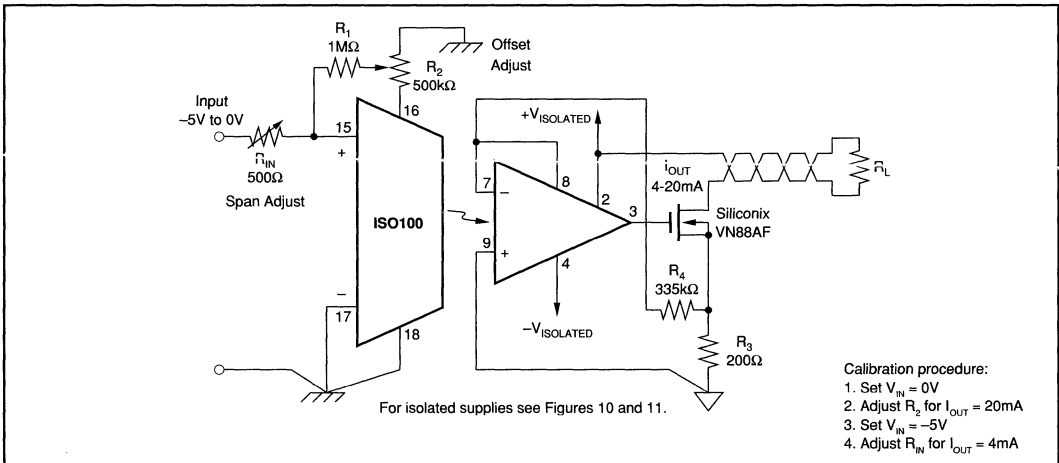


FIGURE 16. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

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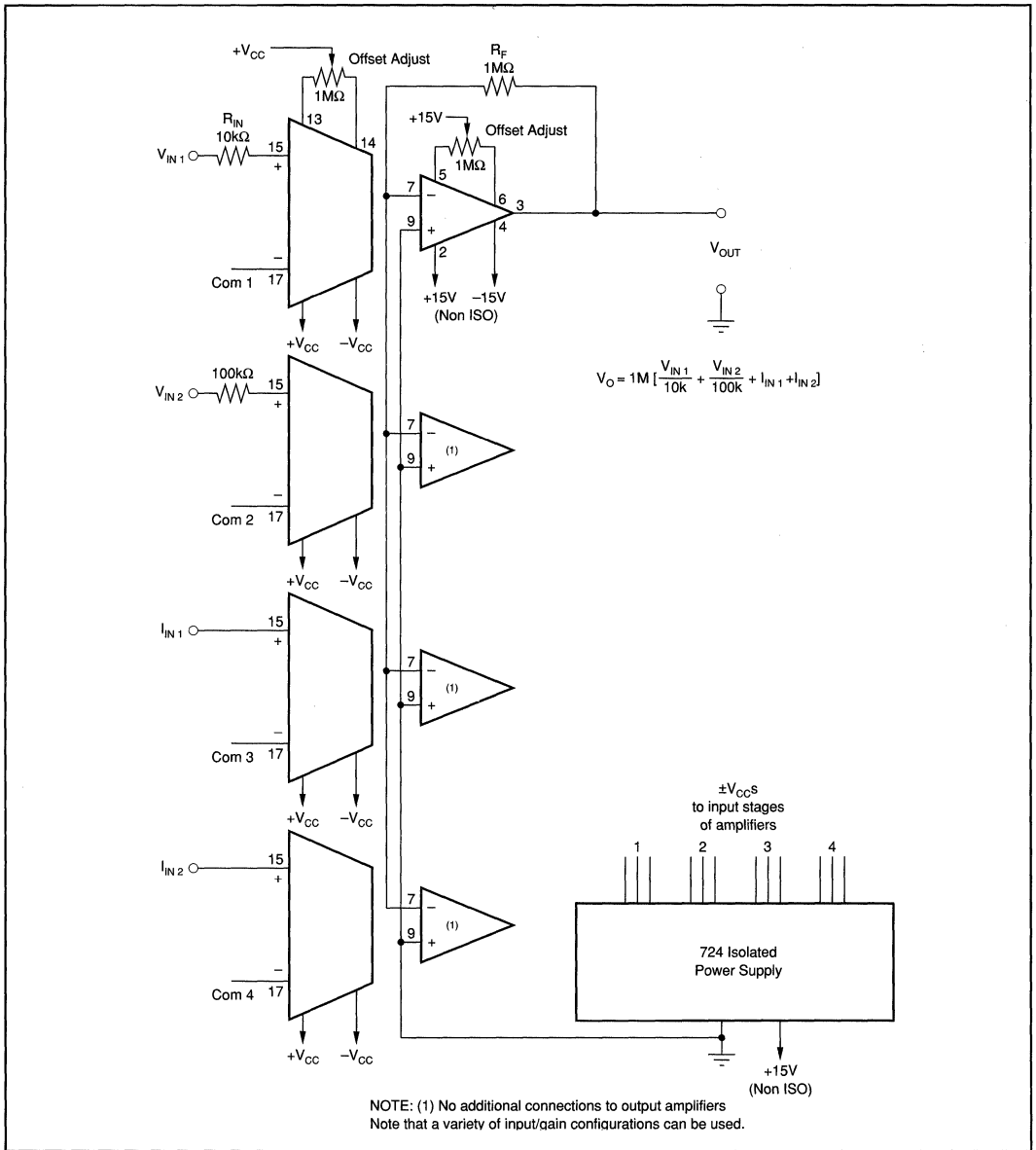


FIGURE 17. Four-Port Isolated Summing Amplifier (Unipolar).

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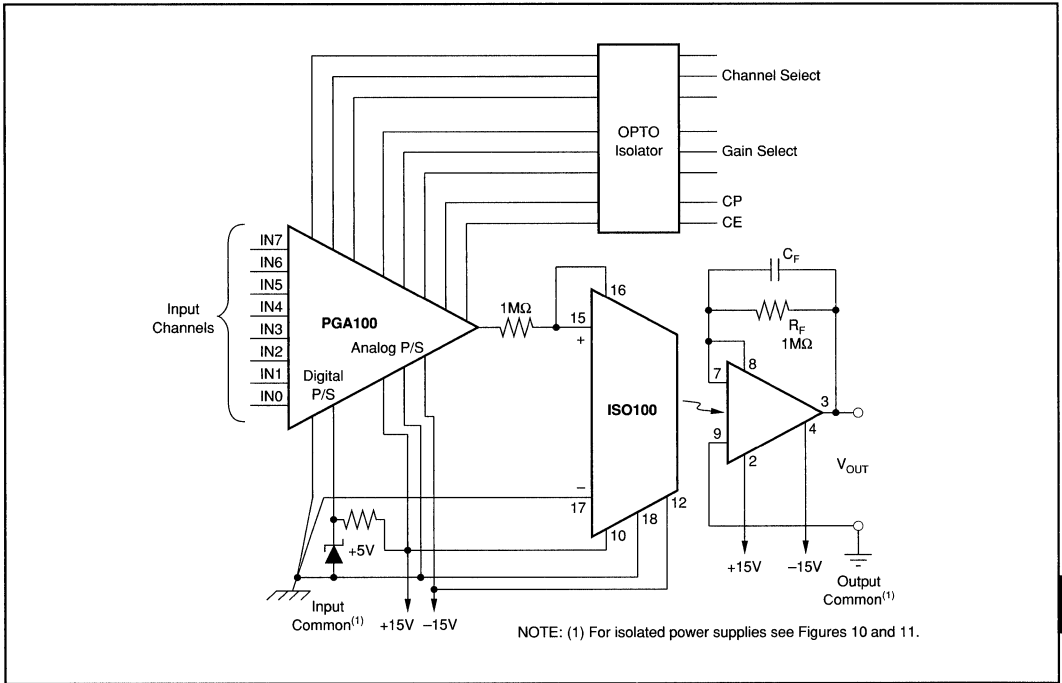
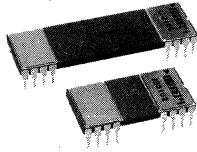


FIGURE 18. Multiple Channel Isolation Amplifier (Bipolar) with Programmable Gain (useful in data acquisition systems).

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ISO102
ISO106

SIGNAL ISOLATION BUFFER AMPLIFIERS

FEATURES

- 14-BIT LINEARITY
- INDUSTRY'S FIRST HERMETIC ISOLATION AMPLIFIERS AT LOW COST
- EASY-TO-USE COMPLETE CIRCUIT
- RUGGED BARRIER, HV CERAMIC CAPACITORS
- 100% TESTED FOR HIGH VOLTAGE BREAKDOWN
ISO102: 4000Vrms/10s, 1500Vrms/1min
ISO106: 8000Vpk/10s, 3500Vrms/1min
- ULTRA HIGH IMR: 125dB min at 60Hz, ISO106
- WIDE INPUT RANGE: -10V to +10V
- WIDE BANDWIDTH: 70kHz
- VOLTAGE REFERENCE OUTPUT: 5VDC

DESCRIPTION

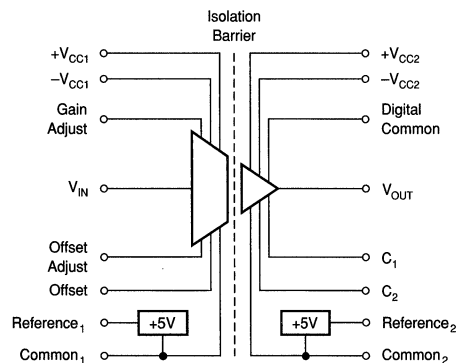
The ISO102 and ISO106 isolation buffer amplifiers are two members of our series of capacitive coupled isolation products from Burr-Brown. They have the same electrical performance and they differ in accuracy. The ISO102 is rated for 1500Vrms in a 24-pin DIP. The ISO106 is rated for 3500Vrms in a 40-pin DIP. Both side-brazed DIPs are 600mil wide and have industry standard package dimensions with the exception of missing pins between input and output stages. This permits utilization of automatic insertion techniques in production. The three-chip hybrid with its generous high voltage spacing is easy to use (no external components are required).

Each buffer accurately isolates $\pm 10V$ analog signals by digitally encoding the input voltage and uniquely coupling across a differential ceramic capacitive bar-

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
Transducer channel isolator for thermocouples, RTDs, pressure bridges, flow meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- BIOMEDICAL/ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MILITARY EQUIPMENT

rier. All elements necessary for operation are contained within the DIP. This provides compact signal isolation in a hermetic package.



Covered by patent number 4,748,419 and others pending.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_{CC1} = V_{CC2} = \pm 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS	ISO102, ISO106, ISO102B, ISO106B			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous ⁽¹⁾					Vrms
ISO102: AC, 60Hz	T_{MIN} to T_{MAX}	1500			VDC
DC	T_{MIN} to T_{MAX}	2121			Vrms
ISO106: AC, 60Hz	T_{MIN} to T_{MAX}	3500			VDC
DC	T_{MIN} to T_{MAX}	4950			
Test Breakdown, AC, 60Hz					Vrms
ISO102	10s	4000			Vpk
ISO106	10s	8000			
Isolation-Mode Rejection ⁽²⁾	$V_{ISO} = \text{Rated Continuous, 60Hz}$				dB
AC: ISO102		115	120	2	$\mu\text{Vrms/V}$
			1		dB
ISO106		125	130	0.6	$\mu\text{Vrms/V}$
			0.3		dB
DC		140	160	0.10	$\mu\text{VDC/V}$
			0.01		Ω
Barrier Resistance			10^{14}		μF
Barrier Capacitance			6		pF
Leakage Current	$V_{ISO} = 240\text{Vrms, 60Hz}$		0.5	1	μArms
INPUT					
Voltage Range	Rated Operation	-10		+10	V
Resistance		75	100		k Ω
Capacitance			5		pF
OUTPUT					
Voltage Range	Rated Operation	-10		+10	V
	Derated Operation	-12		+12	V
Current Drive		± 5			mA
Short Circuit Current		9	20	50	mA
Ripple Voltage ⁽⁶⁾	$f = 0.5\text{MHz to } 1.5\text{MHz}$		3		mVp-p
Resistance			0.3	1	Ω
Capacitive Load Drive Capability		10,000			pF
Overload Recovery Time, 0.1%	$ V_o > 12\text{V}$		30		μs
OUTPUT VOLTAGE NOISE					
Voltage: $f = 0.1\text{Hz to } 10\text{Hz}$			300		$\mu\text{Vp-p}$
$f = 0.1\text{Hz to } 70\text{kHz}$			16		$\mu\text{V}/\sqrt{\text{Hz}}$
Dynamic Range ⁽⁷⁾ : $f = 0.1\text{Hz to } 70\text{kHz}$	12-Bit Resolution, 1LSB, 20V FS		74		dB
$f = 0.1\text{Hz to } 280\text{Hz}$	16-Bit Resolution, 1LSB, 20V FS		96		dB
FREQUENCY RESPONSE					
Small Signal Bandwidth			70		kHz
Full Power Bandwidth, 0.1% THD	$V_o = \pm 10\text{V}$		5		kHz
Slew Rate	$V_o = \pm 10\text{V}$		0.5		V/ μs
Settling Time, 0.1%	$V_o = -10\text{V to } +10\text{V}$		100		μs
Overshoot, Small Signal ⁽⁸⁾	$C_1 = C_2 = 0$		40		%
VOLTAGE REFERENCES					
Voltage Output, Ref ₁ , Ref ₂	No Load	+4.975	+5	+5.025	VDC
B Grade	No Load	+4.995	+5	+5.005	VDC
vs Temperature			± 5	20	ppm/ $^\circ\text{C}$
vs Supplies			10		$\mu\text{V/V}$
vs Load			400	1000	$\mu\text{V}/\text{mA}$
Current Output		-0.1	+5		mA
Short Circuit Current		6	14	30	mA
POWER SUPPLIES					
Rated Voltage, $\pm V_{CC1}, \pm V_{CC2}$	Rated Performance		± 15		V
Voltage Range		± 10		± 20	V
Quiescent Current: $+V_{CC1}$	No Load		+11	+15	mA
$-V_{CC1}$			-9	-12	mA
$+V_{CC2}$			+25	+33	mA
$-V_{CC2}$			-15	-20	mA
Dissipation: $\pm V_{CC1}$			300	400	mW
$\pm V_{CC2}$			600	800	mW
TEMPERATURE RANGE					
Specification		-25		+85	$^\circ\text{C}$
Operating ⁽⁹⁾		-55		+125	$^\circ\text{C}$
Storage		-65		+150	$^\circ\text{C}$
Thermal Resistance, θ_{JA}			40		$^\circ\text{C}/\text{W}$
θ_{JC}			12		$^\circ\text{C}/\text{W}$

ISO102/106

5

ISOLATION PRODUCTS

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ELECTRICAL (CONT)

PARAMETER	CONDITIONS	ISO102			ISO102B			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
GAIN Nominal Gain Initial Error ⁽³⁾ Gain vs Temperature Nonlinearity ⁽⁴⁾	$V_O = -10V \text{ to } +10V$		1 ±0.1 ±20 ±0.007	±0.25 ±50 ±0.012		*	0.07 ±12 ±0.002	0.13 ±25 ±0.003	V/V % FSR ppm FSR/°C % FSR
INPUT OFFSET VOLTAGE Initial Offset vs Temperature vs Power Supplies ⁽⁵⁾	$V_{IN} = 0V$ Input Stage, $V_{CC1} = \pm 10V \text{ to } \pm 20V$ Output Stage, $V_{CC2} = \pm 10V \text{ to } \pm 20V$	0 -4	±25 ±250 1.4 -1.4	±70 ±500 4.0 0	*	±15 ±150 *	±25 ±250 *	mV μV/°C mV/V mV/V	

PARAMETER	CONDITIONS	ISO106			ISO106B			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
GAIN Nominal Gain Initial Error ⁽³⁾ Gain vs Temperature Nonlinearity ⁽⁴⁾	$V_O = -10V \text{ to } +10V$		1 ±0.1 ±20 ±0.04	±0.25 ±50 ±0.075		*	0.07 ±12 ±0.007	* ±25 ±0.025	V/V % FSR ppm FSR/°C % FSR
INPUT OFFSET VOLTAGE Initial Offset vs Temperature vs Power Supplies ⁽⁵⁾	$V_{IN} = 0V$ Input Stage, $V_{CC1} = \pm 10V \text{ to } \pm 20V$ Output Stage, $V_{CC2} = \pm 10V \text{ to } \pm 20V$		±25 ±250 3.7 -3.7	±70 ±500		*	* ±150 *	* ±250	mV μV/°C mV/V mV/V

* Specification same as model to the left.

NOTES: (1) 100% tested at rated continuous for one minute. (2) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency as shown in the Typical Performance Curves. This is specified for barrier voltage slew rates not exceeding 100V/μs. (3) Adjustable to zero. FSR = Full Scale Range = 20V. (4) Nonlinearity is the peak deviation of the output voltage from the best fit straight line. It is expressed as the ratio of deviation to FSR. (5) Power supply rejection = change in $V_{OC}/20V$ supply change. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Dynamic range = FSR/(voltage spectral noise density x square root of user bandwidth). (8) Overshoot can be eliminated by band-limiting. (9) See "Power Dissipation vs Temperature" performance curve for limitations. (10) Band limited to 10Hz, bypass capacitors located less than 0.25" from supply pins.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ISO102	Ceramic	-25°C to +85°C
ISO102B	Ceramic	-25°C to +85°C
ISO106	Ceramic	-25°C to +85°C
ISO106B	Ceramic	-25°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±20V
Input Voltage Range	±50V
Transient Immunity, dV/dt	100kV/μs
Continuous Isolation Voltage Across Barrier	
ISO102	1500Vrms
ISO106	3500Vrms
Junction Temperature	+160°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier and Reference Output	
Short Circuit Duration	Continuous to Common

PACKAGE INFORMATION⁽¹⁾

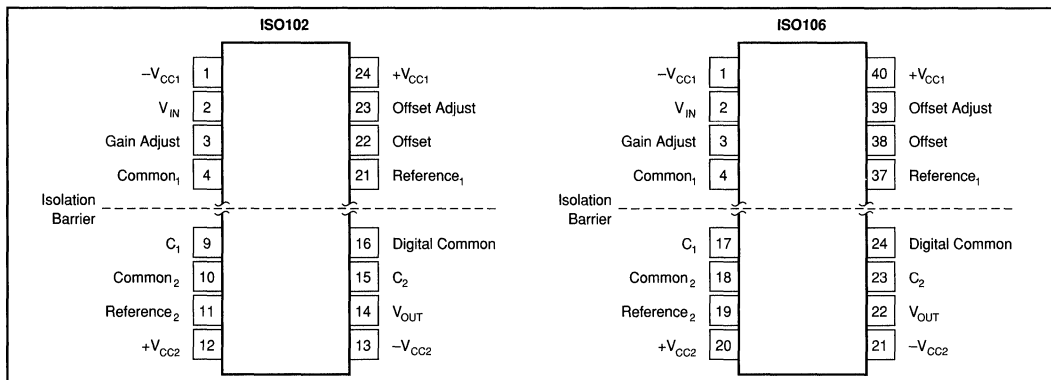
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO102	24-Pin Ceramic	208
ISO102B	24-Pin Ceramic	208
ISO106	40-Pin Ceramic	206
ISO106B	40-Pin Ceramic	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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PIN CONFIGURATION



PIN DESCRIPTIONS

$\pm V_{CC1}$, $Common_1$	Positive and negative power supply voltages and common (or ground) for the input stage. $Common_1$ is the analog reference voltage for input signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
$\pm V_{CC2}$, $Common_2$	Positive and negative power supply voltages and common (or ground) for the output stage. $Common_2$ is the analog reference voltage for output signals. The voltage between $Common_1$ and $Common_2$ is the isolation voltage and appears across the internal high voltage barrier.
V_{IN}	Signal input pin. Input impedance is typically 100k Ω . The input range is rated for $\pm 10V$. The input level can actually exceed the input stage supplies. Output signal swing is limited only by the output supply voltages.
Gain Adjust	This pin is an optional signal input. A series 5k Ω potentiometer between this pin and the input signal allows a guaranteed $\pm 1.5\%$ gain adjustment range. When gain adjustment is not required, the Gain Adjust should be left open. Figure 4 illustrates the gain adjustment connection.
$Reference_1$	+5V reference output. This low-drift zener voltage reference is necessary for setting the bipolar offset point of the input stage. This pin must be strapped to either Offset or Offset Adjust to allow the isolation amplifier to function. The reference is often useful for input signal conditioning circuits. See "Effect of Reference Loading on Offset" performance curve for the effect of offset voltage change with reference loading. $Reference_1$ is identical to, but independent of, $Reference_2$. This output is short circuit protected.
$Reference_2$	+5V reference output. This reference circuit is identical to, but independent of, $Reference_1$. It controls the bipolar offset of the output stage through an internal connection. This output is short-circuit protected.
Offset	Offset input. This input must be strapped to $Reference_1$, unless user adjustment of bipolar offset is required.
Offset Adjust	This pin is for optional offset control. When connected to the $Reference_1$ pin through a 1k Ω potentiometer, $\pm 150mV$ of adjustment range is guaranteed. Under this condition, the Offset pin should be connected to the Offset Adjust pin. When offset adjustment is not required, the Offset Adjust pin is left open. See Figure 4.
Digital Common	Digital common or ground. This separate ground carries currents from the digital portions of the output stage circuit. The best grounding practices require that digital common current does not flow in analog common connections. Both pins can be tied directly to a ground plane if available. Difference in potentials between the $Common_2$ and Digital Common pins can be $\pm 1V$. See Figure 2.
V_{OUT}	Signal output. Because the isolation amplifier has unity gain, the output signal is ideally identical to the input signal. The output is low impedance and is short-circuit protected. This signal is referenced to $Common_2$; subsequent circuitry should have a separate "sense" connection to $Common_1$, as well as V_{OUT} .
C_1 , C_2	Capacitors for small signal bandwidth control. These pins connect to the internal rolloff frequency controlling nodes of the output low-pass filter. Additional capacitance added to these pins will modify the bandwidth of the buffer. C_2 is always twice the value of C_1 . See "Bandwidth Control" performance curve for the relationship between bandwidth and C_1 and C_2 . When no connections are made to these pins, the full small-signal bandwidth is maintained. Be sure to shield C_1 and C_2 pins from high electric fields on the PC board. This preserves AC isolation-mode rejection by reducing capacitive coupling effects.

ISO102/106

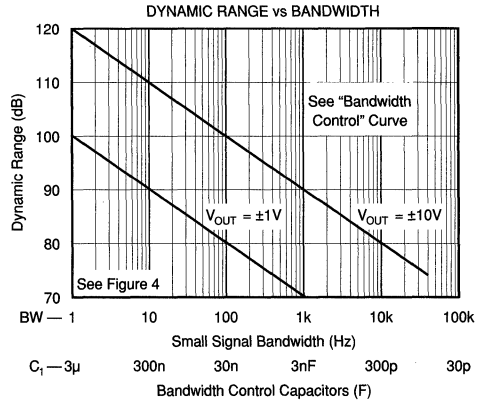
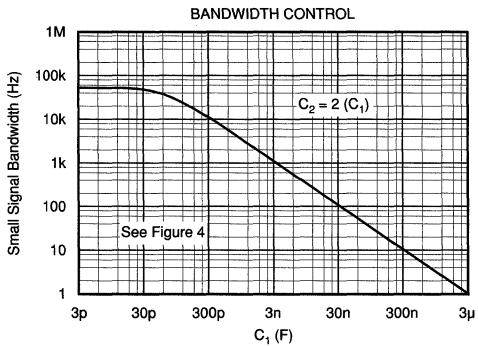
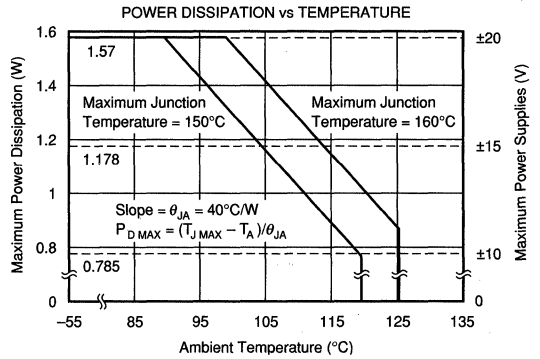
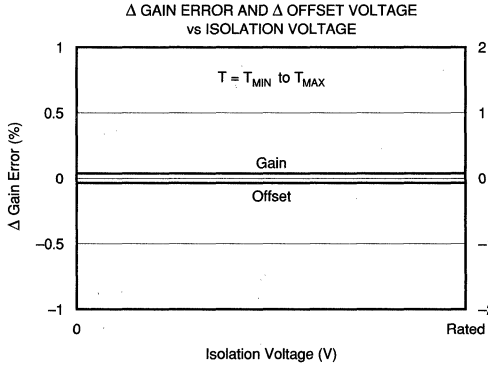
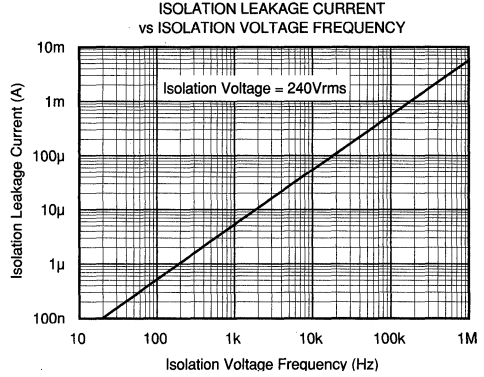
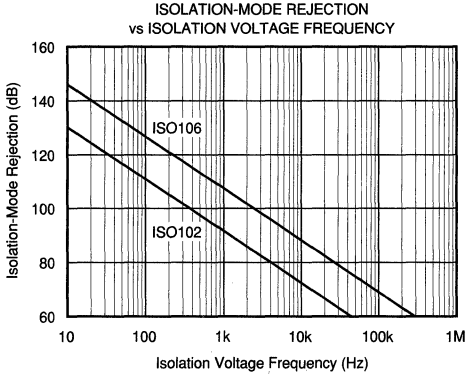
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ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES

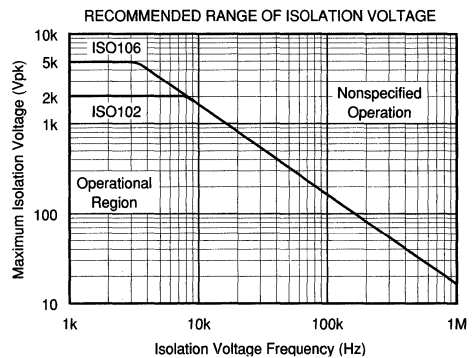
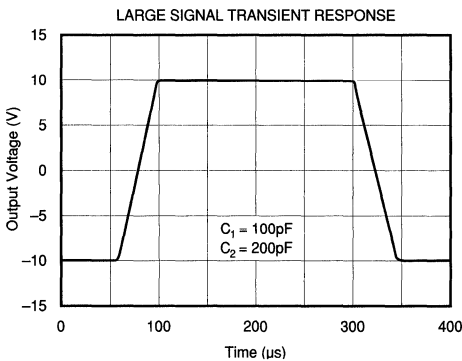
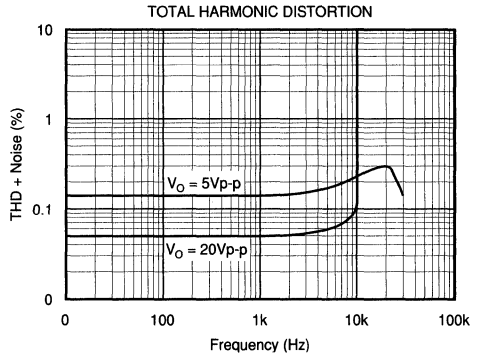
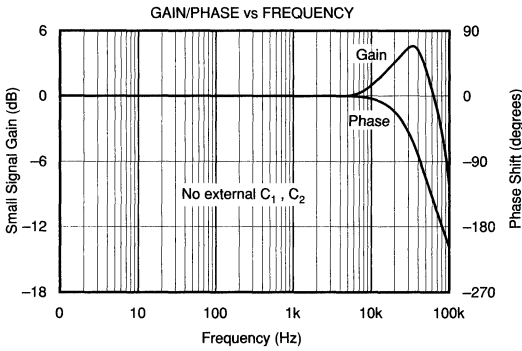
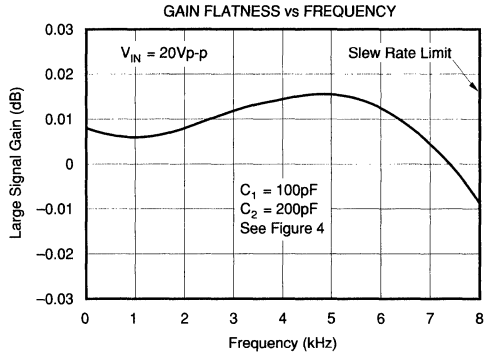
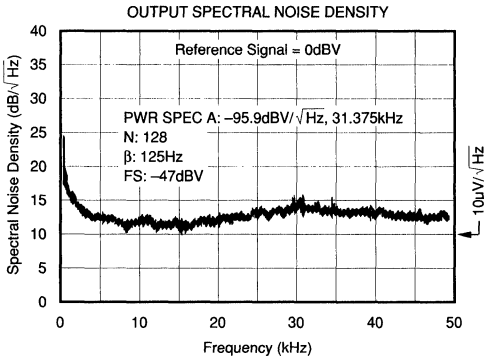
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



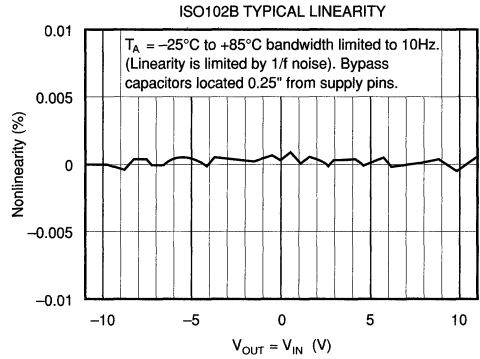
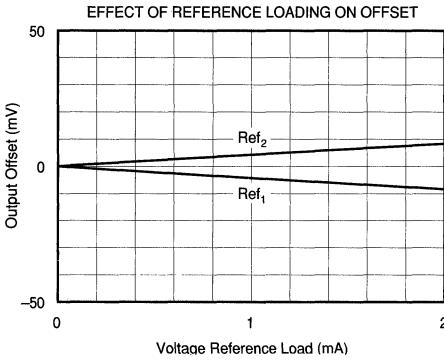
ISO102/106

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ISOLATION PRODUCTS

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



THEORY OF OPERATION

The ISO102 and ISO106 have no galvanic connection between the input and output. The analog input signal referenced to the input common is accurately duplicated at the output referenced to the output common. Because the barrier information is digital, potentials between the two commons can assume a wide range of voltages and frequencies without influencing the output signal. Signal information remains undisturbed until the slew rate of the barrier voltage exceeds $100\text{V}/\mu\text{s}$. The isolation amplifier's ability to reject fast dV/dt changes between the two grounds is specified as transient immunity. The amplifier is protected from damage for slew rates up to $100,000\text{V}/\mu\text{s}$.

A simplified diagram of the ISO102 and ISO106 is shown in Figure 1. The design consists of an input voltage-controlled oscillator (VCO) also known as a voltage-to-frequency converter (VFC), differential capacitors, and output phase lock loop (PLL). The input VCO drives digital levels directly into the two 3pF barrier capacitors. The digital signal is frequency modulated and appears differentially across the barrier, while the externally applied isolation voltage appears common-mode.

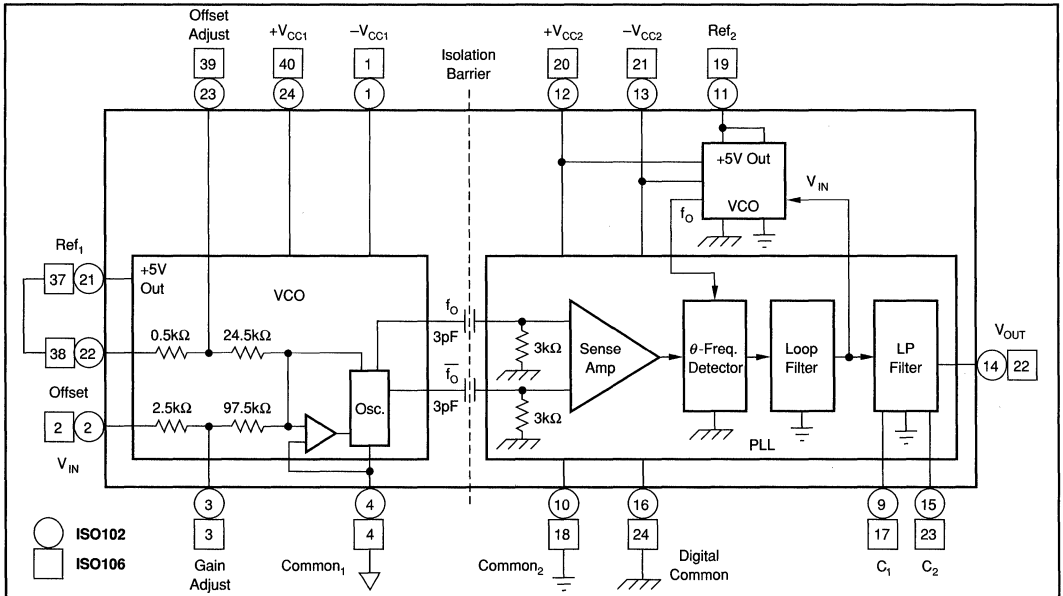


FIGURE 1. Simplified Diagram of ISO102 and ISO106.

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A sense amplifier detects only the differential information. The output stage decodes the frequency modulated signal by the means of a PLL. The feedback of the PLL employs a second VCO that is identical to the encoder VCO. The PLL forces the second VCO to operate at the same frequency (and phase) as the encoder VCO; therefore, the two VCOs have the same input voltage. The input voltage of the decoder VCO serves as the isolation buffer's output signal after passing through a 100kHz second-order active filter.

For a more detailed description of the internal operation of the ISO102 and ISO106, refer to *Proceedings of the 1987 International Symposium on Microelectronics*, pages 202-206.

ABOUT THE BARRIER

For any isolation product, barrier composition is of paramount importance in achieving high reliability. Both the ISO102 and ISO106 utilize two 3pF high voltage ceramic coupling capacitors. They are constructed of tungsten thick film deposited in a spiral pattern on a ceramic substrate. Capacitor plates are buried in the package, making the barrier very rugged and hermetically sealed. Capacitance results from the fringing electric fields of adjacent metal runs. Dielectric strength exceeds 10kV and resistance is typically $10^{14}\Omega$. Input and output circuitry are contained in separate solder-sealed cavities, resulting in the industry's first fully hermetic hybrid isolation amplifier.

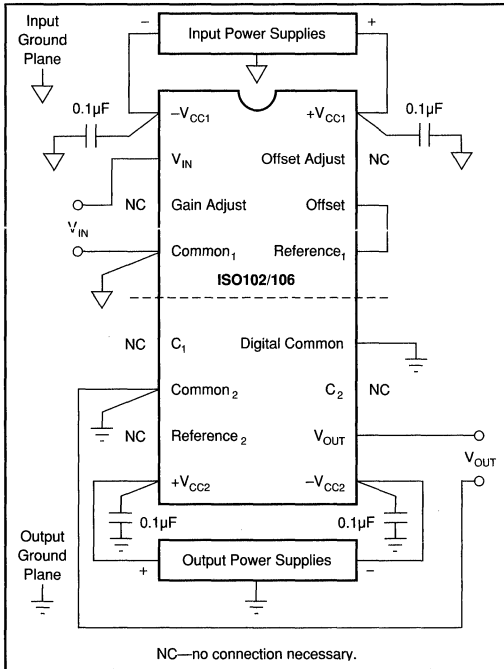


FIGURE 2. Power Supply and Signal Connection.

The ISO102 and ISO106 are designed to be free from partial discharge at rated voltages. Partial discharge is a form of localized breakdown that degrades the barrier over time. Since it does not bridge the space across the barrier, it is difficult to detect. Both isolation amplifiers have been extensively evaluated at high temperature and high voltage.

POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 2 shows the proper power supply and signal connections. Each supply should be AC-bypassed to Analog Common with 0.1µF ceramic capacitors as close to the amplifier as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. Signal common lines should tie directly to the common pin even if a low impedance ground plane is used. Refer to Digital Common in the Pin Descriptions table.

To avoid gain and isolation-mode rejection (IMR) errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Any capacitance across the barrier will increase AC leakage current and may degrade high frequency IMR. The schematic in Figure 3 shows the proper technique for wiring analog and digital commons together.

DISCUSSION OF SPECIFICATIONS

The ISO102 and ISO106 are unity gain buffer isolation amplifiers primarily intended for high level input voltages on the order of 1V to 10V. They may be preceded by operational, differential, or instrumentation amplifiers that precondition a low level signal on the order of millivolts and translate it to a high level.

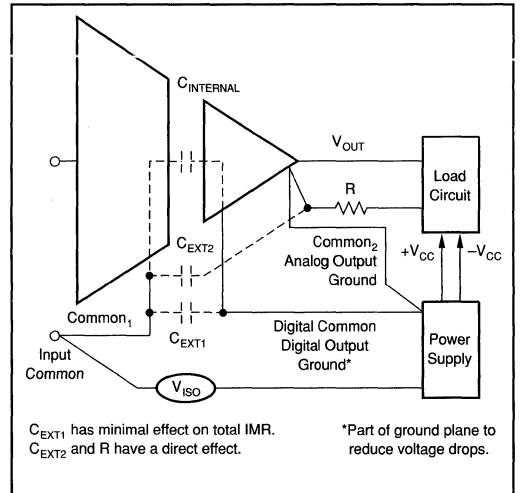


FIGURE 3. Technique for Wiring Analog and Digital Commons Together.

ISOLATION-MODE REJECTION

The IS0102 and IS0106 provide exceptionally high isolation-mode rejection over a wide range of isolation-mode voltages and frequencies. The typical performance curves should be used to insure operation within the recommended range. The maximum barrier voltage allowed decreases as the frequency of the voltage increases. As with all isolation amplifiers, a change of voltage across the barrier will induce leakage current across the barrier. In the case of the IS0102 and IS0106, there exists a threshold of leakage current through the signal capacitors that can cause over-drive of the decoder's sense amplifier. This occurs when the slow rate of the isolation voltage reaches $100\text{V}/\mu\text{s}$. The output will recover in about $50\mu\text{s}$ from transients exceeding $100\text{V}/\mu\text{s}$.

The first two performance curves indicate the expected isolation-mode rejection over a wide range of isolation voltage frequencies. Also plotted is the typical leakage current across the barrier at 240V_{rms} . The majority of the leakage current is between the input common pin and the output digital ground pin.

The IS0102 and IS0106 are intended to be continuously operated with fully rated isolation voltage and temperature without significant drift of gain and offset. See the "Gain Error/Offset Isolation Voltage" performance curve for changes in gain and offset with isolation voltage.

SUPPLY AND TEMPERATURE RANGE

The IS0102 and IS0106 are rated for +15V supplies; however, they are guaranteed to operate from $\pm 10\text{V}$ to $\pm 20\text{V}$. Performance is also rated for an ambient temperature range of -25°C to $+85^\circ\text{C}$. For operation outside this temperature range, refer to the "Power Dissipation vs Temperature" performance curve to establish the maximum allowed supply voltage. Supply currents are fairly insensitive to changes in supply voltage or temperature. Therefore, the maximum current limits can be used in computing the maximum junction temperature under nonrated conditions.

OPTIONAL BANDWIDTH CONTROL

The following discussion relates optimum dynamic range performance to bandwidth, noise, and settling time.

The outputs of the IS0102 and IS0106 are the outputs of a second-order low-pass Butterworth filter. Its low impedance output is rated for $\pm 5\text{mA}$ drive and $\pm 12\text{V}$ range with $10,000\text{pF}$ loads. The closed-loop bandwidth of the PLL is 70kHz , while the output filter is internally set at 100kHz . The output filter lowers the residual voltage of the barrier FM signal to below the noise floor of the output signal.

Two pins are available for optional modification of the filter's bandwidth. Only two capacitors are required. The "Bandwidth Control" performance curve gives the value of C_1 (C_2 is equal to twice C_1) for the desired bandwidth. Figure 4 illustrates the optional connection of both capacitors.

A tradeoff can be achieved between the required signal bandwidth and system dynamic range. The noise floor of the output limits the dynamic range of the output signal. The

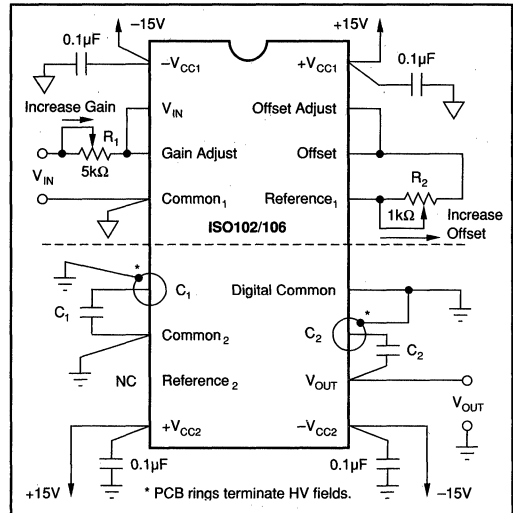


FIGURE 4. Optional Gain Adjust, Offset Adjust, and Bandwidth Control.

noise power varies with the square root of the bandwidth of the buffer. It is recommended that the bandwidth be reduced to about twice the maximum signal bandwidth for optimum dynamic range as shown in the "Dynamic Range vs Bandwidth" performance curve. The output spectral noise density measurement is displayed in the "Output Spectral Noise Density" performance curve. The noise is flat to within $5\text{dB}/\sqrt{\text{Hz}}$ between 0.1Hz to 70kHz .

The overall AC gain of the buffer amplifiers is shown in two performance curves: "Gain Flatness vs Frequency" and "Gain/Phase vs Frequency." Note that with $C_1 = 100\text{pF}$ and $C_2 = 200\text{pF}$, the AC gain remains flat within $\pm 0.01\text{dB}$ up to 7kHz . The total harmonic distortion for large-signal sine wave outputs is plotted in the "Total Harmonic Distortion" performance curve. The phase-lock-loop displays slightly nonuniform rise and fall edges under maximum slew conditions. Reducing the output filter bandwidth to below 70kHz smoothes the output signal and eliminates any overshoot. See the "Large Signal Transient Response" performance curve.

OPTIONAL OFFSET AND GAIN ADJUSTMENT

In many applications the factory-trimmed offset is adequate. For situations where reduced or modified gain and offset are required, adjustment of each is easy. The addition of two potentiometers as shown in Figure 4 provides for a two step calibration.

Offset should be adjusted first. Gain adjustment does not interfere with offset. The potentiometer's TCR adds only 2% to overall temperature drift. The offset and gain adjustment procedures are as follows:

1. Set V_{IN} to 0V and adjust R_1 to desired offset at the output.
2. Set V_{IN} to full scale (not zero). Adjust R_2 for desired gain.

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PRINTED CIRCUIT BOARD LAYOUT

The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing at high voltages. Good layout techniques that reduce stray capacitance will assure low leakage current and high AC IMR. For some applications, applying conformal coating compound such as urethane is useful in maintaining good performance. This is especially true where dirt, grease or moisture can collect on the PC board surface, component surface, or component pins. Following this industry-accepted practice will give best results, particularly when circuits are operated or tested in a moisture-condensing environment. Optimum coating can be achieved by administering urethane under vacuum conditions. This allows complete coverage of all areas. Grounded rings around the C_1 and C_2 contacts on the board greatly reduce high voltage electric fields at these pins.

APPLICATIONS

The ISO102 and ISO106 isolation amplifiers are used in three categories of applications:

1. accurate isolation of signals from high voltage ground potentials,
2. accurate isolation of signals from severe ground noise, and
3. fault protection from high voltages in analog measurement systems.

Figures 5 through 15 show a variety of application circuits. Additional discussion of applications can be found in the December 11, 1986 issue of *Electronic Design*, pages 91-96.

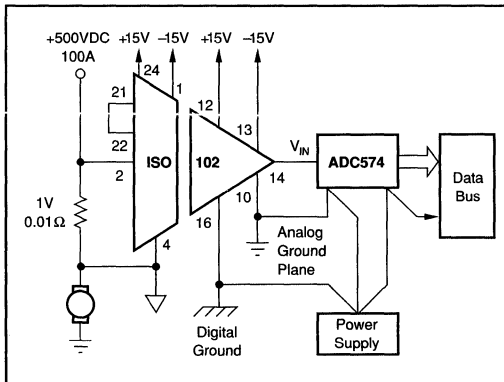


FIGURE 5. Isolated Power Current Monitor for Motor Circuit. (The ISO102 allows reliable, safe measurement at high voltages.)

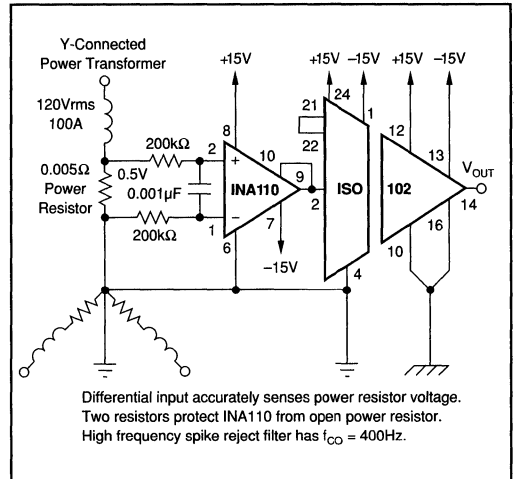


FIGURE 6. Isolated Power Line Monitor (0.5μA leakage current at 120Vrms).

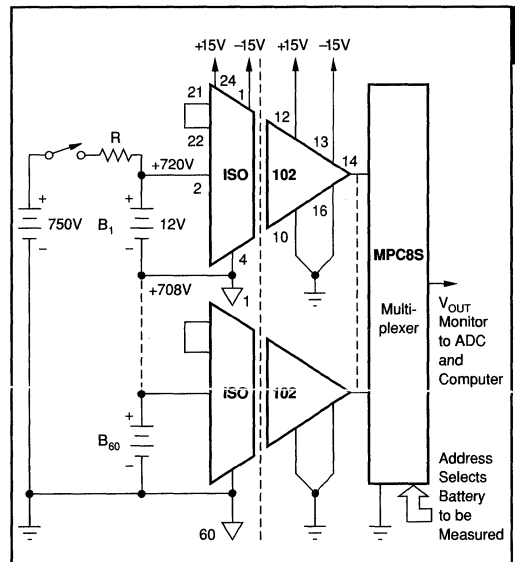


FIGURE 7. Battery Monitor for High Voltage Charging Circuit.

ISO102/106

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ISOLATION PRODUCTS

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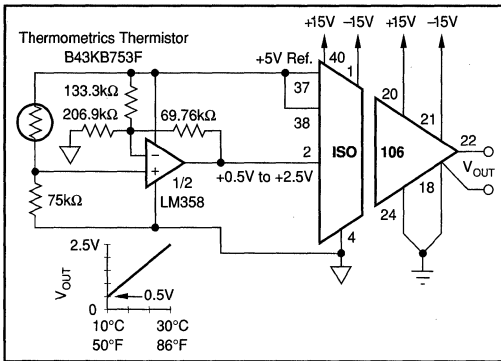


FIGURE 8. Isolated RTD Temperature Amplifier.

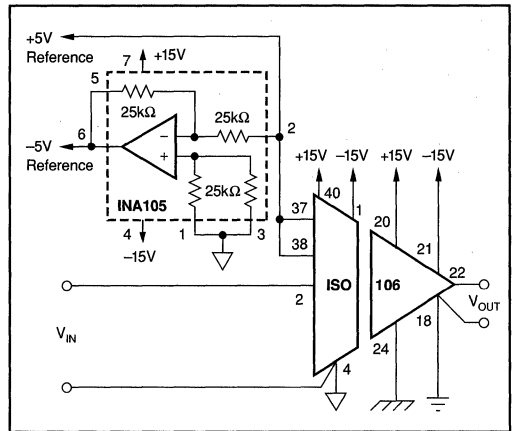


FIGURE 10. Isolation Amplifier with Isolated Bipolar Input Reference.

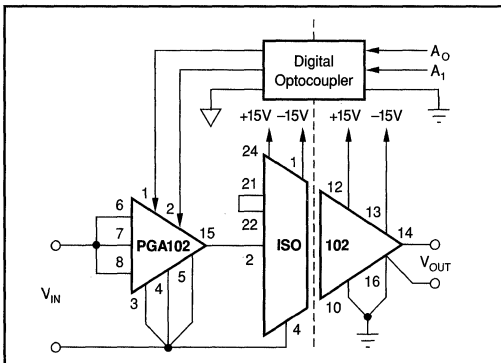


FIGURE 9. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

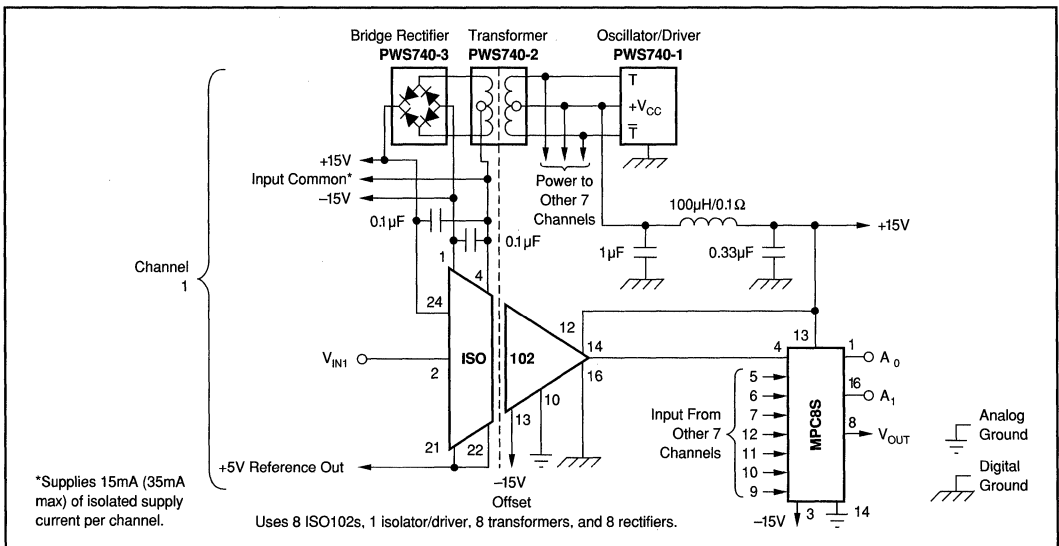


FIGURE 11. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

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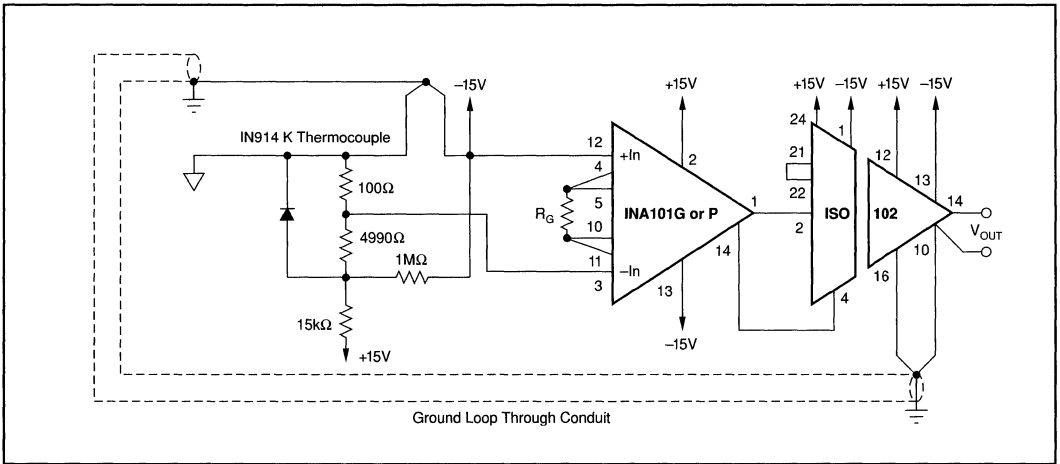


FIGURE 12. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Upscale Burn-out.

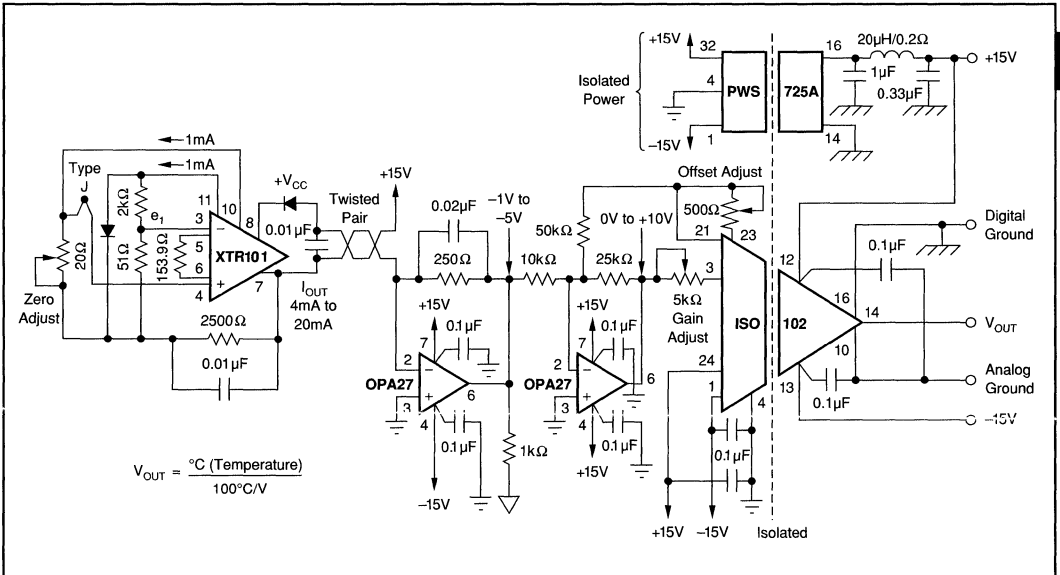


FIGURE 13. Remote Isolated Thermocouple Transmitter with Cold Junction Compensation.

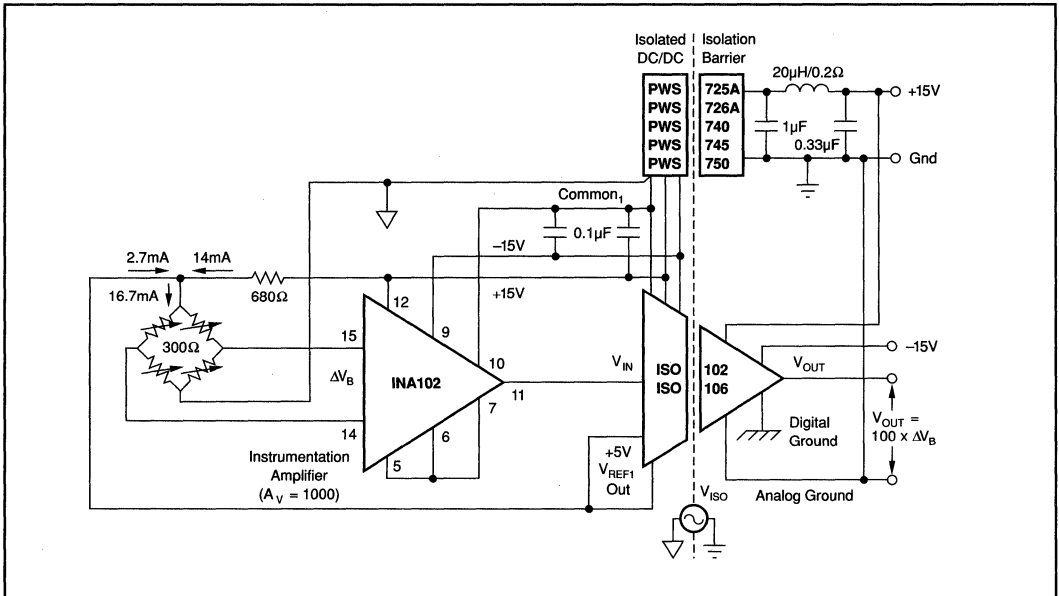


FIGURE 14. Isolated Instrumentation Amplifier for 300Ω Bridge. (Reference voltage from isolation amplifier is used to excite bridge.)

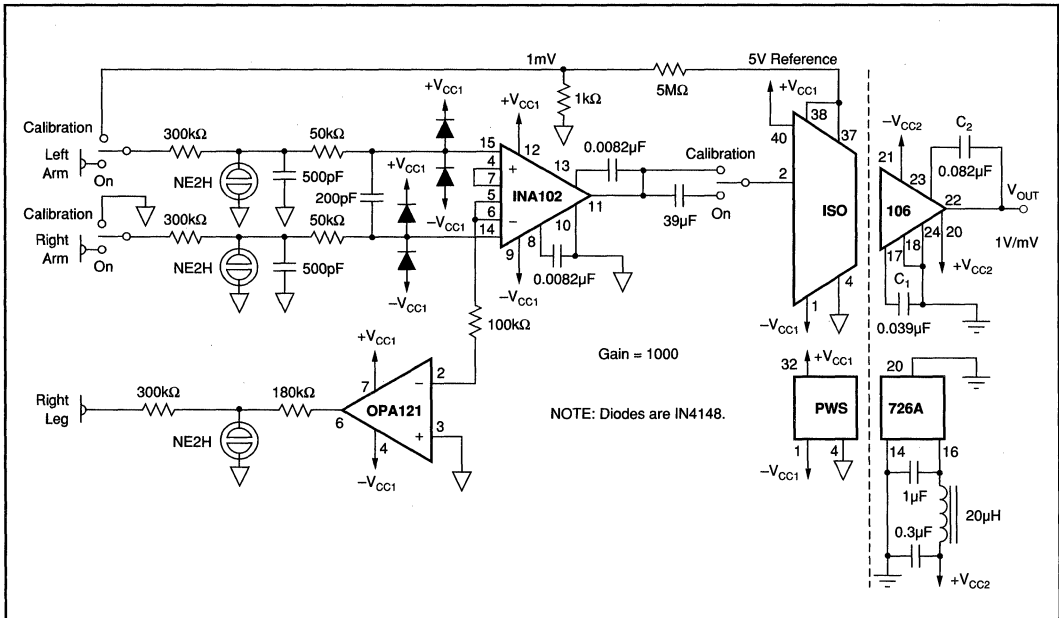


FIGURE 15. Right-Leg-Driven ECG Amplifier (with defibrillator protection and calibrator).

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AN ERROR ANALYSIS OF THE ISO102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 16, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 x to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in Discussion of Specifications.

Some Observations

The total errors of the op amp and the ISO amp combined are approximately 0.11% of full-scale range (see Figure 17). If the op amp had not been used to preamplify the signal, the errors would have been 2.6% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement. Optimum performance, therefore, is obtained when the full ±10V range of the ISO102/106 is utilized.

The rms noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full scale output. Therefore, even though the $16\mu\text{V}/\sqrt{\text{Hz}}$ noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

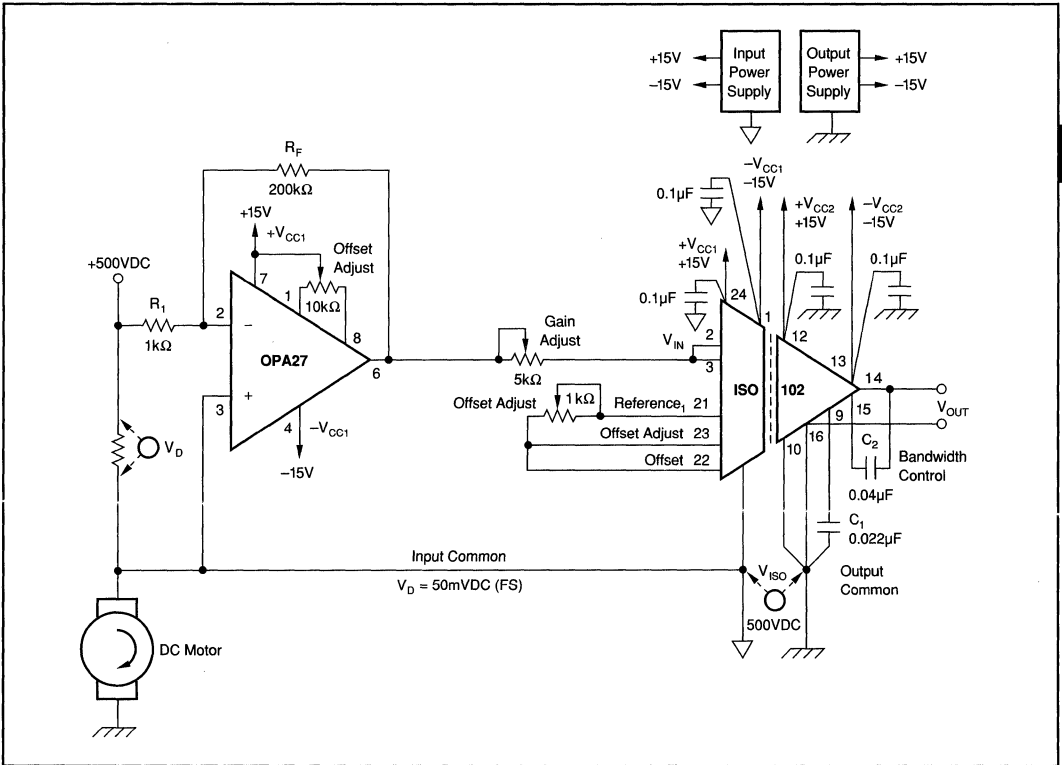


FIGURE 16. 50mV Shunt Measures Current in a 500VDC Motor.

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The Errors of the Op Amp at 25°C (Referred to Input, RTI)

$$V_{E(OPA)} = V_D \left\{ 1 - \frac{1}{\beta A_{VOL}} \right\} + V_{OS} (1 + R_i/R_f) + I_B R_i + \text{P.S.R.} + \text{Noise}$$

$V_{E(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$$\left\{ 1 - \frac{1}{\beta A_{VOL}} \right\} = \text{Gain Error Due to Finite Open Loop Gain}$$

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P.S.R. = Power Supply Rejection ($\mu\text{V/V}$) [Assuming a 5% change with $\pm 15\text{V}$ supplies. Total error is twice that due to one supply.]

Noise = $5\text{nV}/\sqrt{\text{Hz}}$ (for $1\text{k}\Omega$ source resistance and 1kHz bandwidth)

ERROR _(OPA) (RTI)	GAIN ERROR	OFFSET	P.S.R.	NOISE
$V_{E(OPA)}$	$= 50\text{mV} \left\{ 1 - \frac{1}{10^7/200} \right\}$	$\{ 0.025\text{mV} (1 + 1/200) + 40 \times 10^{-9} \times 10^3 \}$	$(20\mu\text{V/V} \times 0.75\text{V} \times 2)$	$(5\text{nV}/\sqrt{120} \text{ (nVrms)})$
	$= 0.01\text{mV}$	$(0.0251\text{mV} + 0.04\text{mV})$	$+$	$+$
Error as % of FSR	$= 0.02\%$	$(0.05\% + 0.08\%)$	$+$	$+$
After Nulling				
	$= 0.01\text{mV}$	$(0\text{mV} + 0\text{mV})$	$+$	$+$
	$= 0.10\text{mV}$			
Error as % of FSR*	$= 0.02\%$	$(0\% + 0\%)$	$+$	$+$
	$= 0.08\%$ of 50mV			

*FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

The Errors of the Iso Amp at 25°C (RTI)

$$V_{E(ISO)} = 1/200 (V_{ISO}/\text{IMR} + V_{OS} + \text{G.E.} + \text{Nonlinearity} + \text{P.S.R.} + \text{Noise})$$

$V_{E(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{INV}$ = Isolation Voltage = Isolation Mode Voltage

G.E. = Gain Error (% of FSR)

Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.

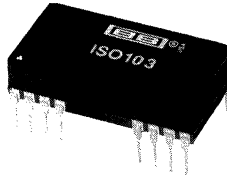
P.S.R. = Change in $V_{OS}/10\text{V} \times$ Supply Change

Noise = Spectral noise density $\times \sqrt{\text{bandwidth}}$. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

ERROR _(ISO) (RTI)	IMR	V_{OS}	G.E.	NONLINEARITY	P.S.R.	NOISE
$V_{E(ISO)}$	$= 1/200 \{ 500\text{VDC}/140\text{dB} \}$	$+ 70\text{mV}$	$+ 20\text{V} \times 0.25/100$	$+ 0.003/100 \times 20\text{V}$	$1.4\text{mV} \times 0.75\text{V} \times 2$	$+ 16\mu\text{V}/\sqrt{120} \text{ (rms)}$
	$= 1/200 \{ 0.05\text{mV} \}$	$+ 70\text{mV}$	$+ 50\text{mV}$	$+ 0.6\text{mV}$	$+ 2.1\text{mV}$	$+ 0.175\text{mVrms}$
Error as % of FSR	$= 0.0005\%$	$+ 0.7\%$	$+ 0.5\%$	$+ 0.006\%$	$+ 0.021\%$	$+ 0.00175\%$
After Nulling						
$V_{E(ISO)}$	$= 1/200 \{ 0.05\text{mV} \}$	$+ 0\text{mV}$	$+ 0\text{mV}$	$+ 0.6\text{mV}$	$+ 2.1\text{mV}$	$+ 0.175\text{mVrms}$
	$= 1/200 (3.0\text{mV})$					
	$= 0.03\text{mV}$					
Error as % of FSR	$= 0.0005\%$	$+ 0\%$	$+ 0\%$	$+ 0.006\%$	$+ 0.021\%$	$+ 0.00175\%$
	$= 0.03\%$ of 50mV					
Total Error	$= V_{E(OPA)}$	$+ V_{E(ISO)}$				
	$= 0.10\text{mV}$	$+ 0.03\text{mV}$				
	$= 0.08\%$ of 50mV	$+ 0.03\%$ of 50mV				
	$= 0.11\%$ of 50mV					

FIGURE 17. Op Amp and Iso Amp Error Analysis.

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ISO103

Low-Cost, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE DOUBLE-WIDE (0.6") SIDE-BRAZED PACKAGE
- 5600Vpk TEST VOLTAGE
- 1500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE: -10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED POWER: $\pm 10V$ to $\pm 18V$ Input, $\pm 50mA$ Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)
- BOARD AREA ONLY 0.72in.² (4.6cm²)

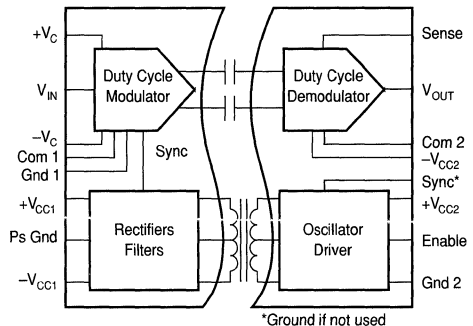
DESCRIPTION

The ISO103 isolation amplifier provides both signal and power across an isolation barrier. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable con-

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- ISOLATED 4-20mA LOOP RECEIVER AND POWER
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



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PDS-1004D

5.45

ISO103

5

ISOLATION PRODUCTS

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_{CC2} = \pm 15\text{V}$, $\pm 15\text{mA}$ output current unless otherwise noted.

PARAMETER	CONDITIONS	ISO103			ISO103B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION Rated Continuous Voltage ⁽¹⁾ AC, 60Hz DC Test Breakdown, 100% AC, 60Hz Isolation-Mode Rejection Barrier Impedance Leakage Current	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} 10s 1500Vrms, 60Hz 2121VDC 240Vrms, 60Hz	1500 2121 5657			*	*	*	Vrms VDC Vpk dB dB $\Omega \mu\text{F}$ μA
GAIN Nominal Initial Error Gain vs Temperature Nonlinearity	$V_O = -10\text{V}$ to 10V $V_O = -5\text{V}$ to 5V		1 ± 0.12 ± 60 ± 0.026 ± 0.009	± 0.3 ± 100 ± 0.075		*	± 0.08 ± 20 ± 0.018 *	V/V % FSR ppm/ $^\circ\text{C}$ % FSR %FSR
INPUT OFFSET VOLTAGE Initial Offset vs Temperature vs Power Supplies vs Output Supply Load	$V_{CC2} = \pm 10\text{V}$ to $\pm 18\text{V}$ $I_O = 0$ to $\pm 50\text{mA}$		± 20 ± 300 0.9 ± 0.3	± 60 ± 500		*	*	mV $\mu\text{V}/^\circ\text{C}$ mV/V mV/mA
SIGNAL INPUT Voltage Range Resistance	Output Voltage in Range	± 10	± 15 200		*	*		V k Ω
SIGNAL OUTPUT Voltage Range Current Drive Ripple Voltage, 800kHz Carrier Capacitive Load Drive Voltage Noise	400 Ω /4.7nF (See Figure 4)	± 10 ± 5	± 12.5 ± 15 25 5 1000 4		*	*	*	V mA mVp-p mVp-p pF $\mu\text{V}/\sqrt{\text{Hz}}$
FREQUENCY RESPONSE Small Signal Bandwidth Slew Rate Settling Time	0.1%, $-10/10\text{V}$		20 1.5 75			*	*	kHz V/ μs μs
POWER SUPPLIES Rated Voltage, V_{CC2} Voltage Range Input Current Ripple Current Rated Output Voltage Output Load Regulation Line Regulation Output Voltage vs Temperature Voltage Balance Error, $\pm V_{CC1}$ Voltage Ripple (800kHz) Output Capacitive Load Sync Frequency	$I_O = \pm 15\text{mA}$ $I_O = 0\text{mA}$ No Filter $C_W = 1\mu\text{F}$ Load = 15mA 50mA Balanced Load 100mA Single-Ended Loads Balanced Load No External Capacitors $C_{\text{EXT}} = 1\mu\text{F}$ Sync-Pin Grounded ⁽²⁾	± 10	± 15 +90/-4.5 +60/-4.5 60 3 ± 15 10 10 0.3 1.12 2.5 0.05 50 5 1.6	± 18 ± 15.75	*	*	*	V V mA mA mAp-p mAp-p V V V V %/mA V/V mV/ $^\circ\text{C}$ % mVp-p mVp-p μF MHz
TEMPERATURE RANGE Specification Operating Storage		-25 -25 -25		+85 +85 +125	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$

* Specifications same as ISO103.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

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ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V_{IN} Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	1500Vrms
$V_{ISO}^{dV/dt}$	20kV/μs
Junction Temperature	150°C
Storage Temperature	-25°C to +125°C
Lead Temperature, 10s	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

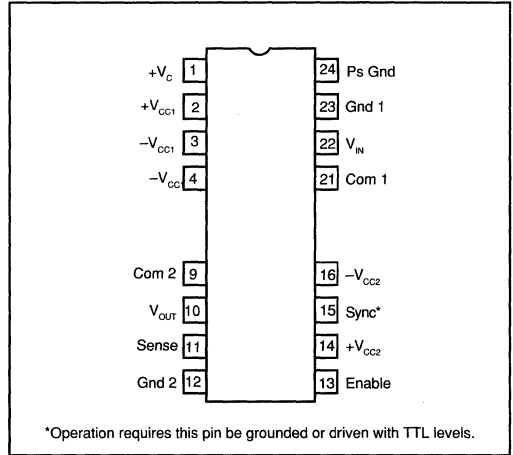


ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO103	24-Pin DIP	231

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ISO103

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ISOLATION PRODUCTS

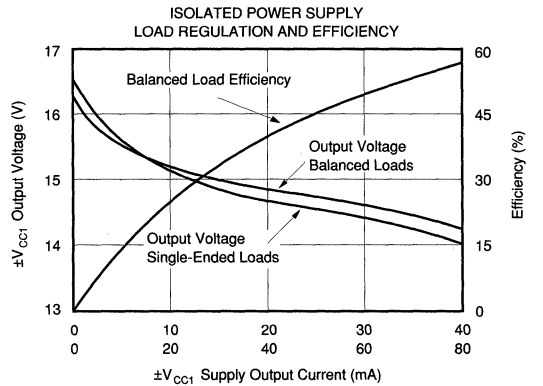
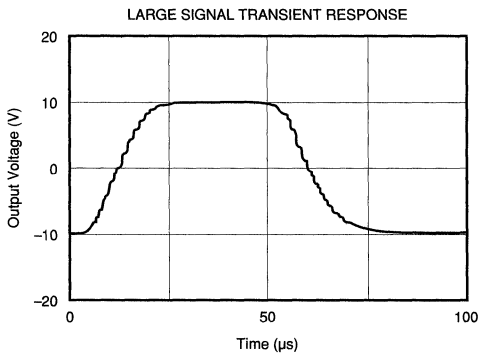
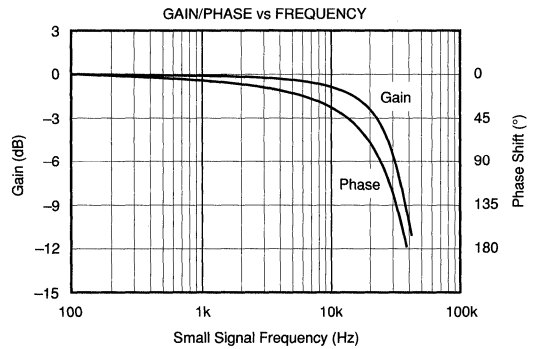
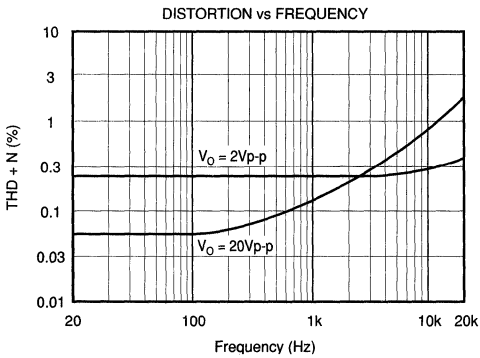
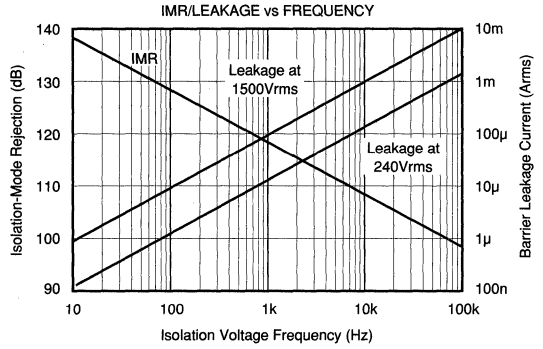
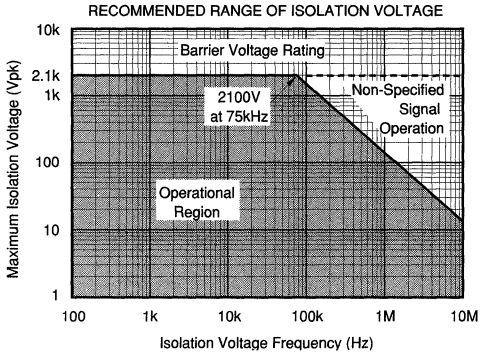
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TYPICAL PERFORMANCE CURVES

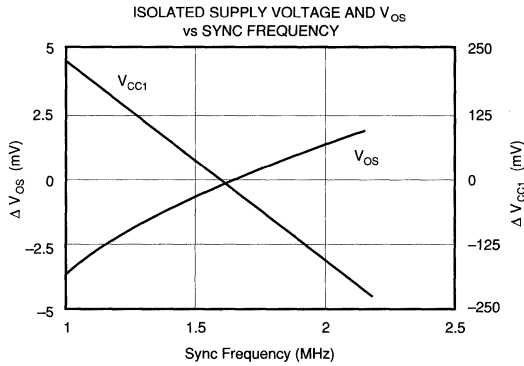
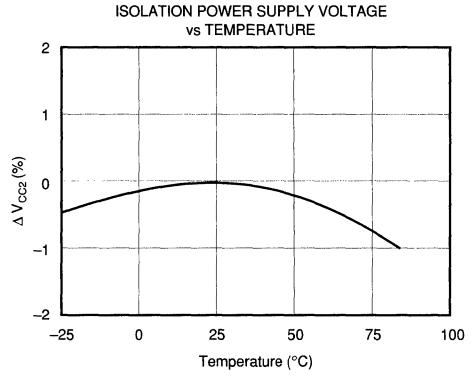
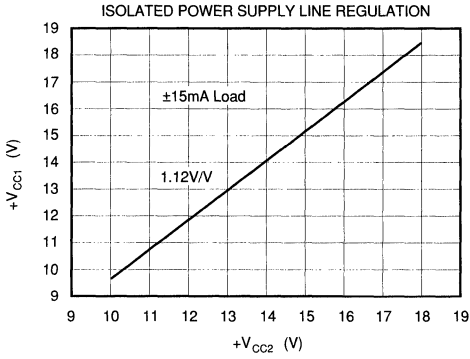
$T_A = +25^\circ\text{C}$, $V_{CC2} = \pm 15\text{VDC}$, $\pm 15\text{mA}$ output current unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC2} = \pm 15\text{VDC}$, $\pm 15\text{mA}$ output current unless otherwise noted.



ISO103

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ISOLATION PRODUCTS

THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminates beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than $\pm 15\text{mA}$ are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC1}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO103 socket. The enable pin may be left open if the ISO103 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

The ISO103 isolation amplifier contains a transformer-coupled DC/DC converter that is powered from the output side of the isolation amplifier. All power supply pins (1, 2, 3, 4, 14, and 16) of the ISO103 have an internal $0.1\mu\text{F}$ capacitor to ground. L_1 is used to slow down fast changes in the input current to the DC/DC converter. C_1 is used to help regulate the voltage ripple caused by the current demands of the converter. L_1 , C_1 , and C_2 are optional, however, recommended for low noise applications.

The DC/DC converter creates an unregulated $\pm 15\text{V}$ output to $\pm V_{CC1}$. If the ISO103 is the only device using the DC/DC converter for power, pins 1 and 2 and pins 3 and 4 can be connected directly without C_O or L_O in the circuit. If an external capacitor is used in this configuration, it should not exceed $1\mu\text{F}$. This configuration is possible because the isolation amplifier and the DC/DC converter are synchronized internally.

If additional devices are powered by the DC/DC converter of the ISO103, the application may require that the ripple voltage of the ISO103 converter be attenuated. In which case, L_O and C_O should be added to the circuit. The inductor is used to attenuate the ripple current and a higher value capacitor can be used to reduce the ripple voltage even further.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of $\pm 0.5\%$ for the values shown; greater range may be provided by increasing the size of R_1 and R_2 . Every $2\text{k}\Omega$ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

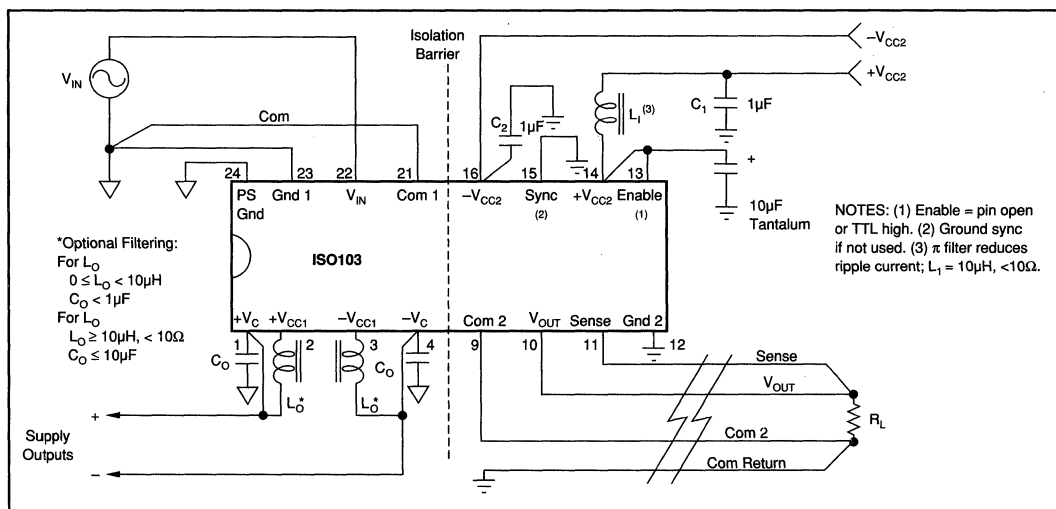


FIGURE 1. Signal and Power Connections.

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Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

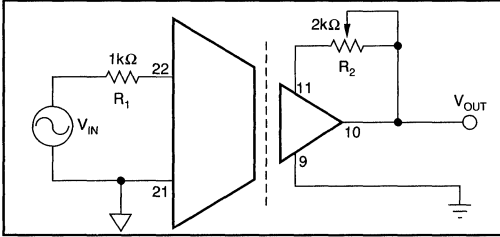


FIGURE 2a. Gain Adjust.

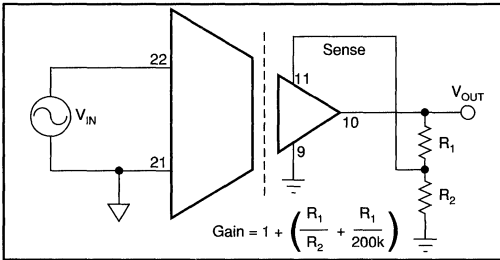


FIGURE 2b. Gain Setting.

Figure 3 shows a method for trimming V_{OS} of the ISO103. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, $\pm 15V$ supplies and unity gain, the circuit will provide $\pm 150mV$ adjustment range and $0.25mV$ resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a $\pm 100mV$ trim, power supply sensitivity is $8mV/V$ at the output.

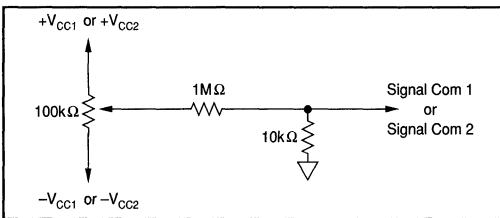


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the $800kHz$ ripple voltage to $<5mV_{p-p}$ without compromising DC performance. The small signal bandwidth is extended above $30kHz$ as a result of this compensation.

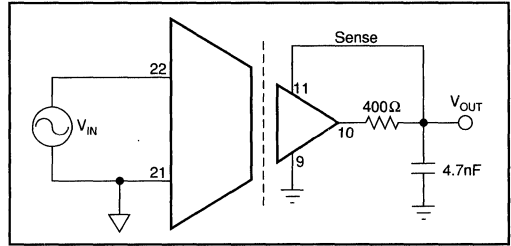


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO103s can be accomplished by connecting pin 15 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is $1.6MHz$, resulting in a $800kHz$ carrier in the ISO103 (its nominal unsynchronized value). The open collector output typically switches $7.5mA$ to a $0.2V$ low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than $1000pF$ to ensure TTL level switching at $800kHz$. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic provided the frequency is between $1.2MHz$ and $2MHz$, and the duty cycle is greater than 25%.

Multichannel synchronization with reduced power dissipation for applications requiring less than $\pm 15mA$ from V_{CC1} is accomplished by driving both the Sync input pin (15) and Enable pin (13) with the TTL oscillator as shown in Figure 5.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO103 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed $20kV/\mu s$. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO103 was designed to reliably operate with $1500V_{rms}$ continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, a $5600V$ peak, $60Hz$ barrier potential is

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applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

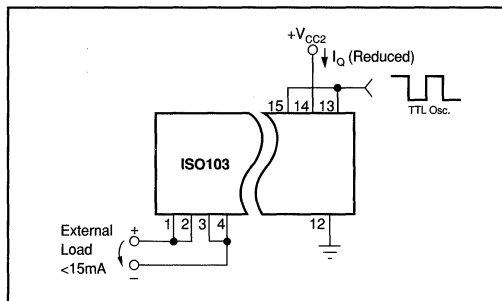


FIGURE 5. Reduced Power Dissipation.

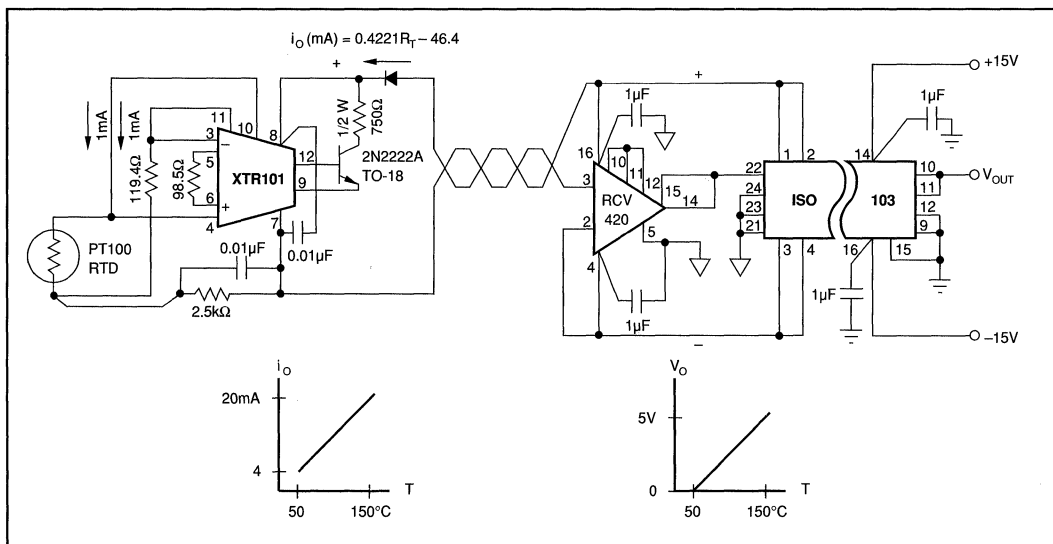


FIGURE 6. Isolated 4-20mA Instrument Loop.

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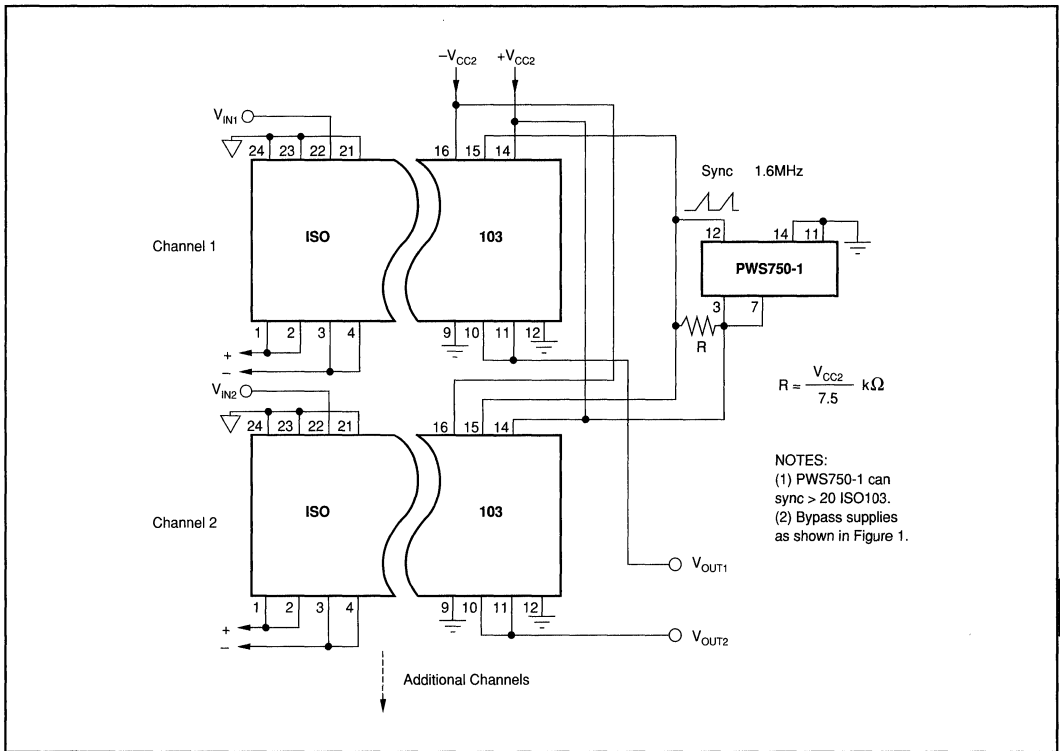
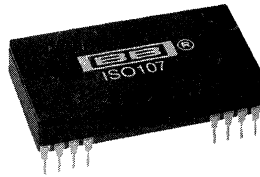


FIGURE 7. Synchronized-Multichannel Isolation.

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ISO107

High-Voltage, Internally Powered ISOLATION AMPLIFIER

FEATURES

- SIGNAL AND POWER IN ONE TRIPLE-WIDE PACKAGE
- 8000Vpk TEST VOLTAGE
- 2500Vrms CONTINUOUS AC BARRIER RATING
- WIDE INPUT SIGNAL RANGE:
-10V to +10V
- WIDE BANDWIDTH: 20kHz Small Signal,
20kHz Full Power
- BUILT-IN ISOLATED POWER:
 $\pm 10V$ to $\pm 18V$ Input, $\pm 50mA$ Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY (TTL)

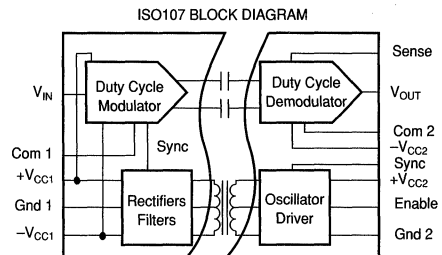
DESCRIPTION

The ISO107 isolation amplifier provides both signal and power across an isolation barrier. The ceramic side-brazed hybrid package contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated input side for external input conditioning circuitry. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable con-

APPLICATIONS

- MULTICHANNEL ISOLATED DATA ACQUISITION
- BIOMEDICAL INSTRUMENTATION
- POWER SUPPLY AND MOTOR CONTROL
- GROUND LOOP ELIMINATION



rol is used to turn off transformer drive while keeping the signal channel demodulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 2500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL544 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO107 easy to use, as well as providing for compact PC board layouts.

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_{CC2} = ±15V, ±15mA output current unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Rated Continuous Voltage ⁽¹⁾					
AC, 60Hz	T _{MIN} to T _{MAX}	2500			Vrms
DC	T _{MIN} to T _{MAX}	3500			VDC
Test Breakdown, AC, 60Hz	10s	8000			Vpk
Isolation-Mode Rejection	2500Vrms, 60Hz 2121VDC		100		dB
Barrier Impedance			160		dB
Leakage Current	240Vrms, 60Hz		10 ⁻¹² 13		Ω pF
			1.2	2	μA
GAIN					
Nominal			1		V/V
Initial Error			±0.1	±0.25	% FSR
Gain vs Temperature			±50	±120	ppm/°C
Nonlinearity			±0.01	±0.025	% FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±20	±50	mV
vs Temperature			±150	±400	μV/°C
vs Power Supplies	V _{CC2} = ±10V to ±18V		±2		mV/V
INPUT					
Voltage Range	Output Voltage in Range	±10	±15		V
Resistance			200		kΩ
SIGNAL OUTPUT					
Voltage Range		±10	±12.5		V
Current Drive		±5	±15		mA
Ripple Voltage, 800kHz Carrier (See Figure 4)			20		mVp-p
Capacitive Load Drive			1000		pF
Voltage Noise			4		μV/√Hz
FREQUENCY RESPONSE					
Small Signal Bandwidth			20		kHz
Slew Rate			1.5		V/μs
Settling Time	0.1%, -10/10V		75		μs
POWER SUPPLIES					
Rated Voltage, V _{CC2}			±15		V
Voltage Range		±10		±18	V
Input Current	I _O = ±15mA ⁽²⁾		+75/-4.5		mA
Ripple Current	No Filter		10		mAp-p
	C _{IN} = 1μF		3		mAp-p
Rated Output Voltage		±14.25	±15	±15.75	V
Output Current	Balanced Load		±15	±50	mA
	Single		30	100	mA
Load Regulation	Balanced Load		0.5		%/mA
Line Regulation			1.18		v/v
Output Voltage vs Temperature			10		mV/°C
Voltage Balance Error, ±V _{CC1}			0.05		%
Voltage Ripple	No External Capacitors		10		mVp-p
Output Capacitive Load (See Figure 1)				1	μF
Sync Frequency	Sync-Pin Grounded ⁽³⁾		1.6		MHz
TEMPERATURE RANGE					
Specification		-25		+85	°C
Operating		-25		+85	°C
Storage		-25		+125	°C

NOTES: (1) Conforms to UL544 test methods. 100% tested at 2500Vrms for 1 minute. (2) For other conditions, see Performance Curve, Input Current (+V_{CC2}) vs Output Current. Input Current (-V_{CC2}) is constant at -4.5mA (typ) for all output currents. (3) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

ISO107

5

ISOLATION PRODUCTS

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ABSOLUTE MAXIMUM RATINGS

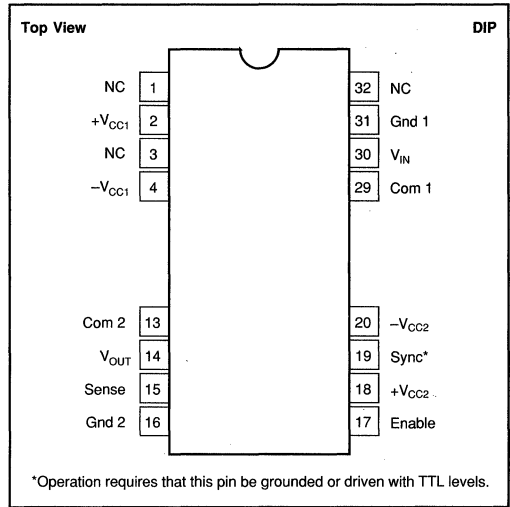
Supply Without Damage	±18V
V_{IN} Sense Voltage	±50V
Com 1 to Gnd 1 or Com 2 to Gnd 2	±200mV
Enable, Sync	0V to $+V_{CC2}$
Continuous Isolation Voltage	2500Vrms
V_{ISO} dv/dt	20kV/ μ s
Junction Temperature	150°C
Storage Temperature	-25°C to +125°C
Lead Temperature, (soldering, 10s)	300°C
Output Short to Gnd 2 Duration	Continuous
$\pm V_{CC1}$ to Gnd 1 Duration	Continuous

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO107	32-Pin Side-Braze Ceramic	210

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

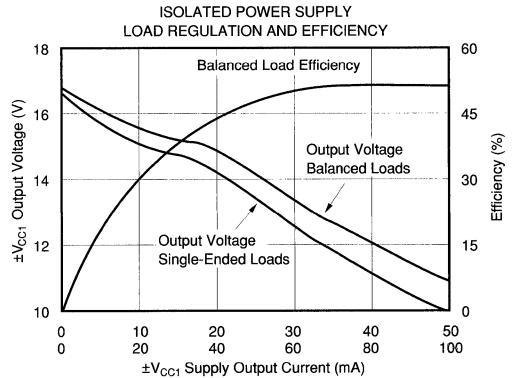
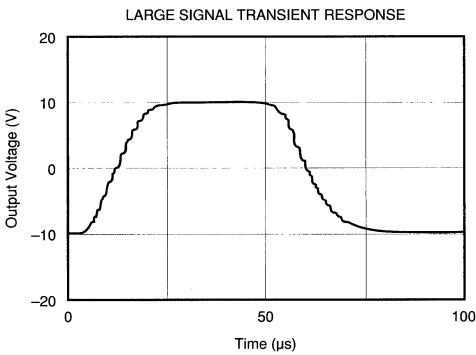
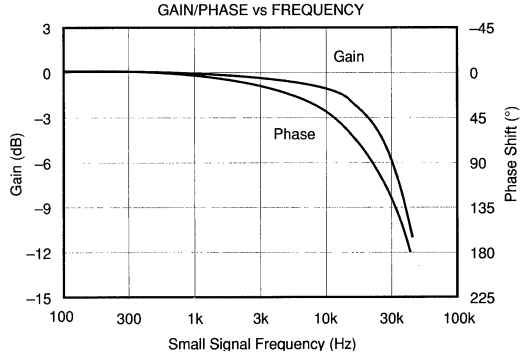
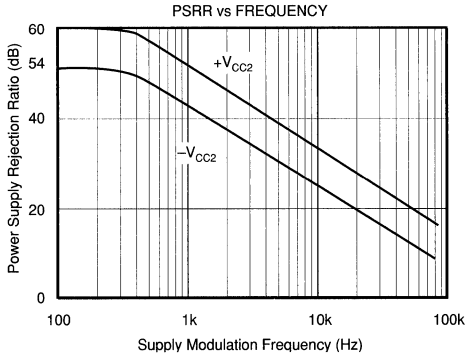
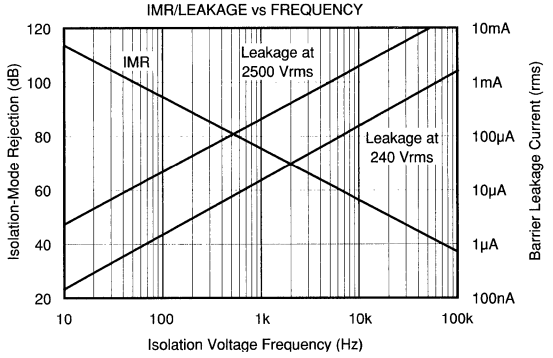
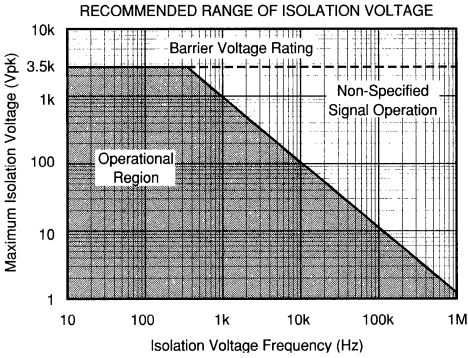
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Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC2} = \pm 15\text{VDC}$, $\pm 15\text{mA}$ output current unless otherwise noted.



ISO107

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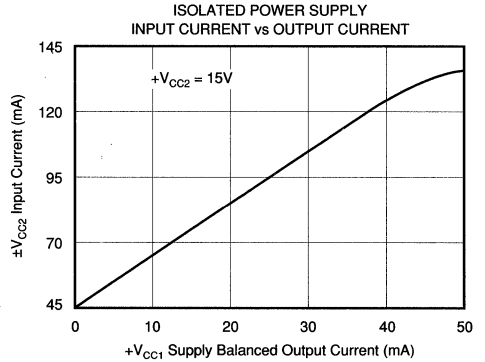
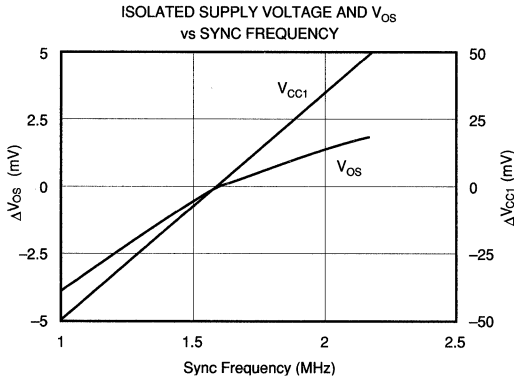
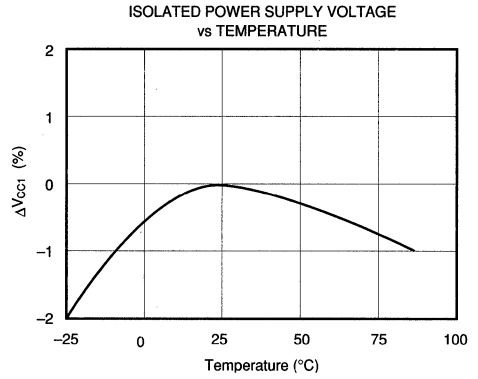
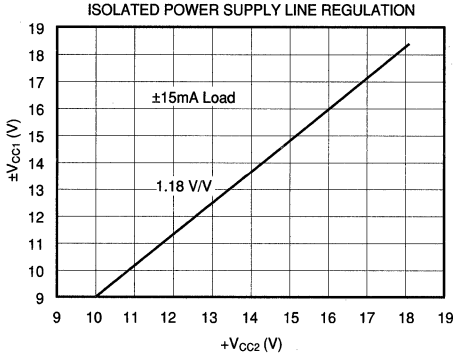
ISOLATION PRODUCTS



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC2} = \pm 15\text{VDC}$, $\pm 15\text{mA}$ output current unless otherwise noted.



THEORY OF OPERATION

The block diagram on the front page shows the isolation amplifier's synchronized signal and power configuration, which eliminates beat frequency interference. A proprietary 800kHz oscillator chip, power MOSFET transformer drivers, patented square core wirebonded transformer, and single chip diode bridge provide power to the input side of the isolation amplifier as well as external loads. The signal channel capacitively couples a duty-cycle encoded signal across the ceramic high-voltage barrier built into the package. A proprietary transmitter-receiver pair of integrated circuits, laser trimmed at wafer level, and coupled through a pair of matched "fringe" capacitors, result in a simple, reliable design.

SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC2}$, an option recommended if more than $\pm 15\text{mA}$ are drawn from the isolated supply. The separate input and output common pins and output sense are low current inputs tied to the signal source ground, output ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, Com 2 to Gnd 2, and Sense to V_{OUT} at the ISO107 socket. The enable pin may be left open if the ISO107 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of $\pm 0.5\%$ for the values shown; greater range may be provided by increasing the size of R_1 and R_2 . Every $2\text{k}\Omega$ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq R_1$. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reserved.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in in-

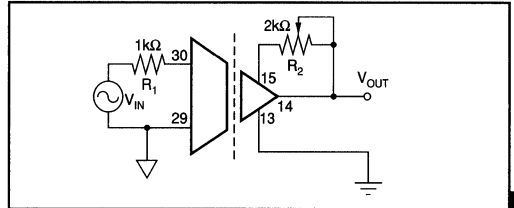


FIGURE 2a. Gain Adjust.

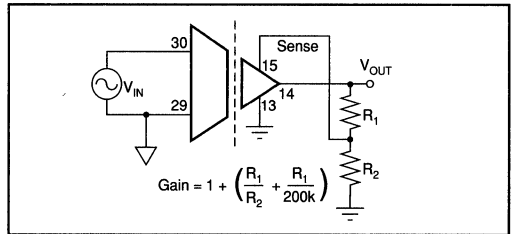


FIGURE 2b. Gain Setting.

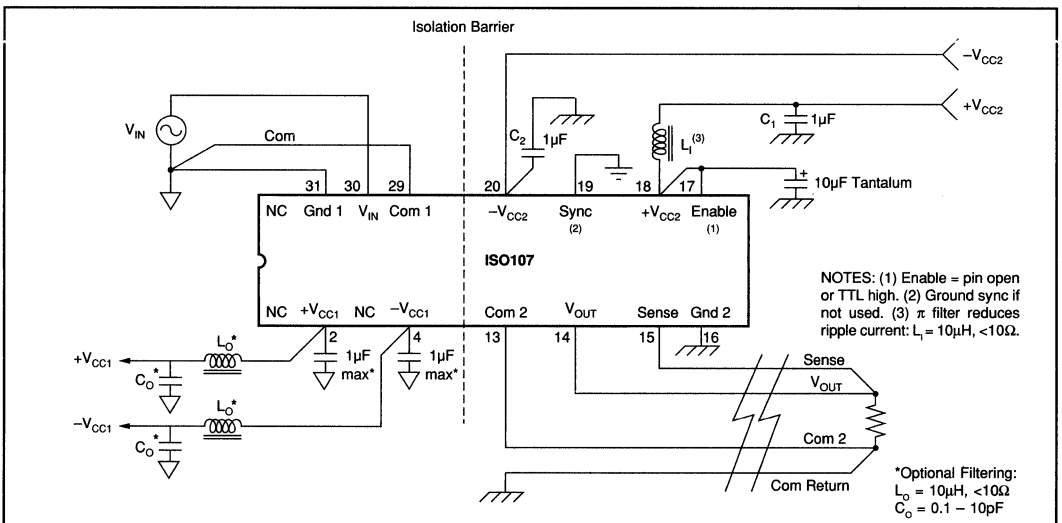


FIGURE 1. Signal and Power Connections.

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verse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO107. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, $\pm 15V$ supplies and unity gain, the circuit will provide $\pm 150mV$ adjustment range and $0.25mV$ resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a $\pm 100mV$ trim, power supply sensitivity is $8mV/V$ at the output.

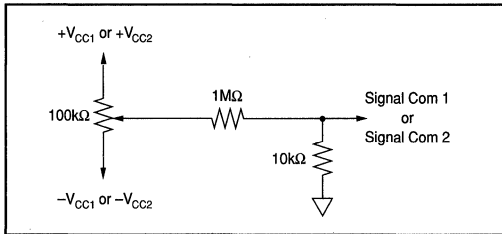


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the $800kHz$ ripple voltage to $<3mV_{p-p}$ without compromising DC performance. The small signal bandwidth is extended above $30kHz$ as a result of this compensation.

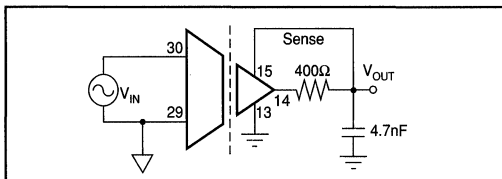


FIGURE 4. Ripple Reduction.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO107s can be accomplished by connecting pin 19 of each device to an external TTL level oscillator, as shown in Figure 6. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is $1.6MHz$, resulting in a $800kHz$ carrier in the ISO107 (its nominal unsynchronized value). The open collector output typically switches $7.5mA$ to a $0.2V$ low level so that the external pull-up resistor can be chosen for different pull-up voltages as shown in Figure 6. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than $1000pF$ to ensure TTL level switching at $800kHz$. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between $1.2MHz$ and $2MHz$, and the duty cycle is greater than 25%.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO107 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/Leakage vs Frequency. At low barrier modulation levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed $20kV/\mu s$. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO107 was designed to reliably operate with $2500V_{rms}$ continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an $8000V$ peak, $60Hz$ barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a $2500V_{rms}$, $60Hz$ potential is applied for one minute to conform to UL544. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

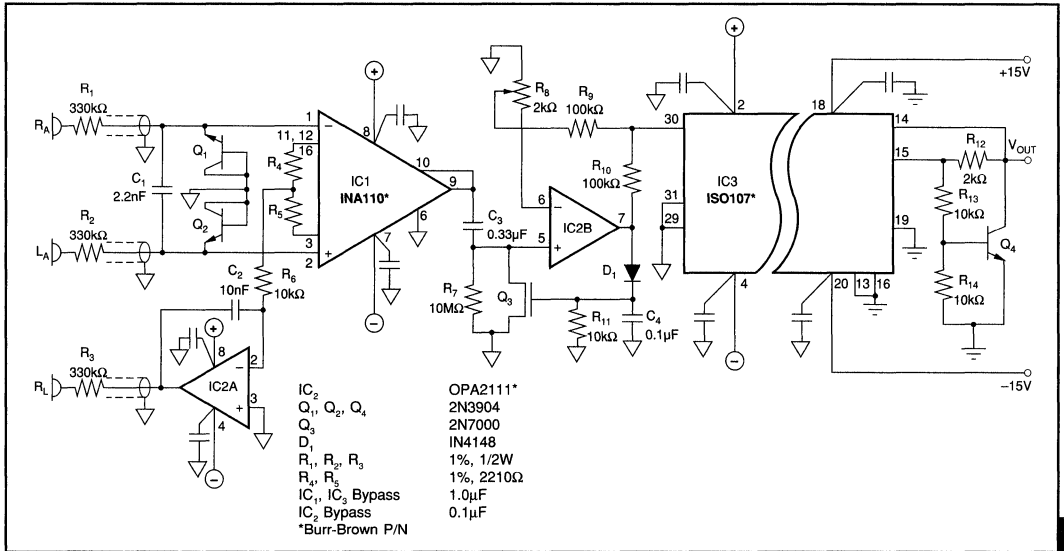


FIGURE 5. ECG Amplifier with Right Leg Drive, Defibrillator Protection, and E.S.U. Blanking.

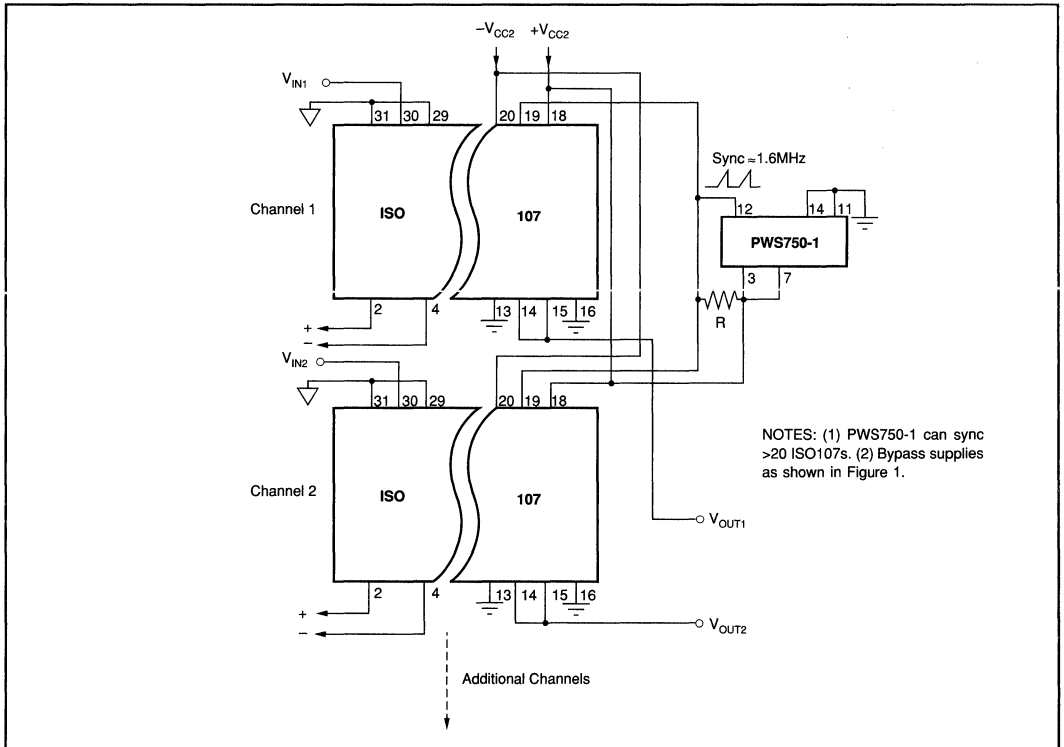
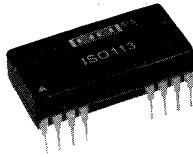


FIGURE 6. Synchronized-Multichannel Isolation.

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ISO113

Low-Cost, High-Voltage, Internally Powered OUTPUT ISOLATION AMPLIFIER

FEATURES

- SELF-CONTAINED ISOLATED SIGNAL AND OUTPUT POWER
- SMALL PACKAGE SIZE: Double-Wide (0.6") Sidebrazed DIP
- CONTINUOUS AC BARRIER RATING: 1500Vrms
- WIDE BANDWIDTH: 20kHz Small Signal, 20kHz Full Power
- BUILT-IN ISOLATED OUTPUT POWER: $\pm 10V$ to $\pm 18V$ Input, $\pm 50mA$ Output
- MULTICHANNEL SYNCHRONIZATION CAPABILITY
- BOARD AREA ONLY 0.72in.² (4.6cm²)

APPLICATIONS

- 4mA TO 20mA V/I CONVERTERS
- MOTOR AND VALVE CONTROLLERS
- ISOLATED RECORDER OUTPUTS
- MEDICAL INSTRUMENTATION OUTPUTS
- GAS ANALYZERS

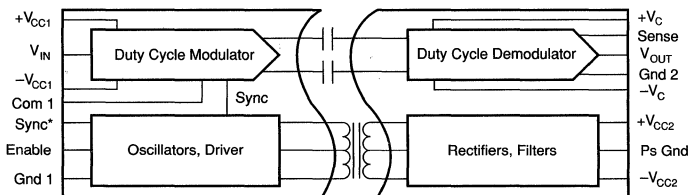
DESCRIPTION

The ISO113 output isolation amplifier provides both signal and output power across an isolation barrier in a small double-wide DIP package. The ceramic non-hermetic hybrid package with side-brazed pins contains a transformer-coupled DC/DC converter and a capacitor-coupled signal channel.

Extra power is available on the isolated output side for driving external loads. The converter is protected from shorts to ground with an internal current limit, and the soft-start feature limits the initial currents from the power source. Multiple-channel synchronization can be accomplished by applying a TTL clock signal to paralleled Sync pins. The Enable control is used to turn off transformer drive while keeping the signal channel modulator active. This feature provides a convenient way to reduce quiescent current for low power applications.

The wide barrier pin spacing and internal insulation allow for the generous 1500Vrms continuous rating. Reliability is assured by 100% barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents.

These specifications and built-in features make the ISO113 easy to use, and provides for compact PC board layout.



*Ground if not used

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_{CC1} = \pm 15\text{V}$, $\pm 15\text{mA}$ output current unless otherwise noted.

PARAMETER	CONDITIONS	ISO113			ISO113B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Rated Continuous Voltage AC, 60Hz	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX} 10s	1500			*			Vrms
DC		2121			*			VDC
Test Breakdown, 100% AC, 60Hz		5657			*			Vpk
Isolation-Mode Rejection	1500Vrms, 60Hz		130		*			dB
	2121VDC		160		*			dB
Barrier Impedance			$10^{12} \parallel 9$		*			$\Omega \parallel \text{pF}$
Leakage Current	240Vrms, 60Hz		1	2	*	*		μA
GAIN								
Nominal			1		*			V/V
Initial Error			± 0.3	± 0.5	*	*		%FSR
Gain vs Temperature			± 0.60	± 100	± 20	± 50		ppm/ $^\circ\text{C}$
Nonlinearity	$V_O = -10\text{V}$ to 10V $V_O = -5\text{V}$ to 5V		± 0.05	± 0.1	± 0.03	± 0.05		%FSR
			± 0.02	± 0.04	± 0.012	± 0.02		%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			± 20	± 60	*	*		mV
vs Temperature			± 300	± 500	± 100	± 250		$\mu\text{V}/^\circ\text{C}$
vs Power Supplies	$V_{CC2} = \pm 10$ to $\pm 18\text{V}$		0.9		*	*		mV/V
vs Output Supply Load	$I_O = 0$ to $\pm 50\text{mA}$		± 0.3		*	*		mV/mA
SIGNAL INPUT								
Voltage Range	Output Voltage in Range	± 10	± 15		*	*		V
Resistance			200		*	*		k Ω
SIGNAL OUTPUT								
Voltage Range		± 10	± 12.5		*	*		V
Current Drive		± 5	± 15		*	*		mA
Ripple Voltage, 800kHz Carrier			25		*	*		mVp-p
	400 Ω /4.7nF (See Figure 4)		5		*	*		mVp-p
Capacitive Load Drive			1000		*	*		pF
Voltage Noise			4		*	*		$\mu\text{V}/\sqrt{\text{Hz}}$
FREQUENCY RESPONSE								
Small Signal Bandwidth			20		*	*		kHz
Slew Rate			1.5		*	*		V/ μs
Settling Time	0.1%, $-10/10\text{V}$		75		*	*		μs
POWER SUPPLIES								
Rated Voltage, V_{CC1}			± 15		*	*		V
Voltage Range				± 18	*	*		V
Input Current	$I_O = \pm 15\text{mA}$ $I_O = 0\text{mA}$ No Filter	± 10	+90/-4.5 +60/-4.5		*	*		mA
Ripple Current	No Filter $C_{IN} = 1\mu\text{F}$		60 3		*	*		mA
Rated Output Voltage	Load = 15mA	± 14.25	± 15	± 15.75	*	*		mAp-p
Output	50mA Balanced Load	10			*	*		V
	100mA Single-Ended Load	10			*	*		V
	Balanced Load				*	*		V
Load Regulation			0.3		*	*		%/mA
Line Regulation			1.12		*	*		V/V
Output Voltage vs Temperature			2.5		*	*		mV/ $^\circ\text{C}$
Voltage Balance, $\pm V_{CC2}$			0.05		*	*		%
Voltage Ripple (800kHz)	No External Capacitors		50		*	*		mVp-p
	$C_{EXT} = 1\mu\text{F}$		5		*	*		mVp-p
Output Capacitive Load				1		*		μF
Sync Frequency	Sync-Pin Grounded ⁽²⁾		1.6			*		MHz
TEMPERATURE RANGE								
Specification		-25		+85	*	*		$^\circ\text{C}$
Operating		-25		+85	*	*		$^\circ\text{C}$
Storage		-25		+125	*	*		$^\circ\text{C}$

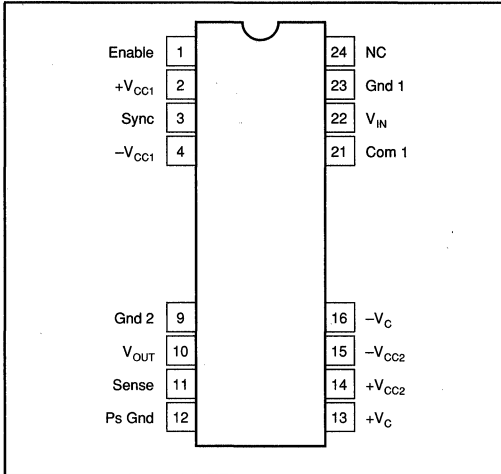
*Specifications same as ISO113.

NOTE: (1) Conforms to UL1244 test methods. 100% tested at 1500Vrms for 1 minute. (2) If using external synchronization with a TTL-level clock, frequency should be between 1.2MHz and 2MHz with a duty-cycle greater than 25%.

ISO113
5
ISOLATION PRODUCTS

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PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO113	24-Pin DIP	231

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Without Damage	±18V
V _{IN} Sense Voltage	±50V
Com ₁ to Gnd ₁	±200mV
Enable, Sync	Gnd to +V _{CC1}
Continuous Isolation Voltage	1500Vrms
V _{ISO} dv/dt	20kV/μs
Junction Temperature	+150°C
Storage Temperature	-25°C to +125°C
Lead Temperature, 10s	+300°C
Output Short to Gnd Duration	Continuous
±V _{CC2} to Gnd 2 Duration	Continuous



ELECTROSTATIC DISCHARGE SENSITIVITY

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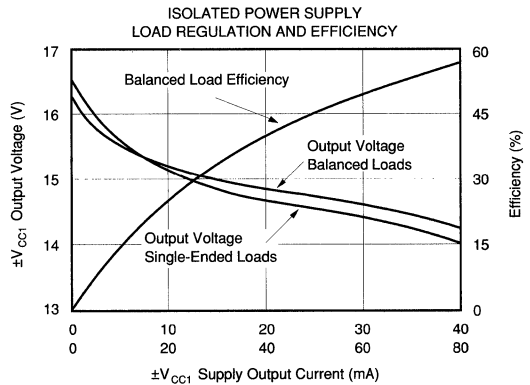
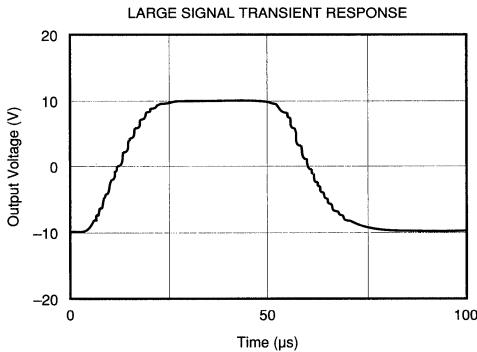
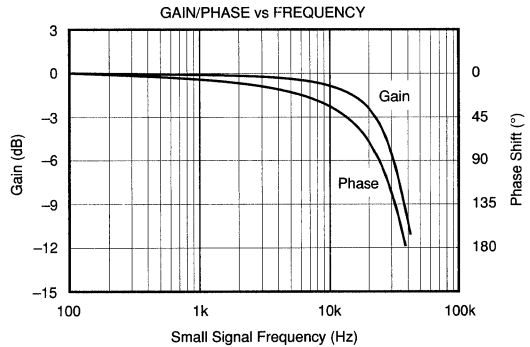
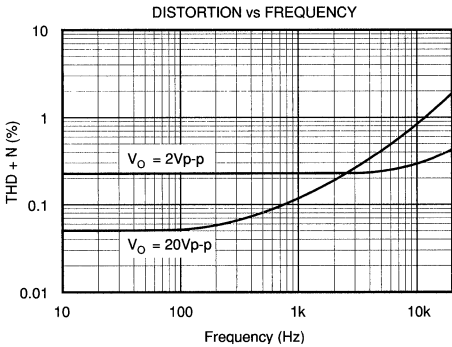
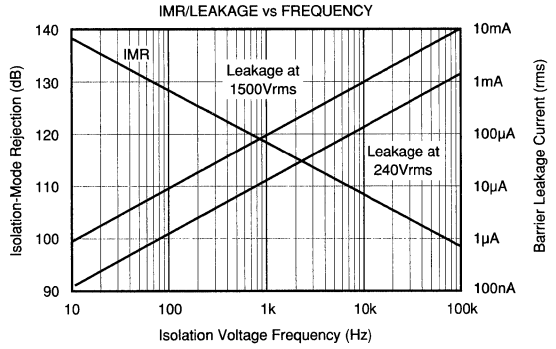
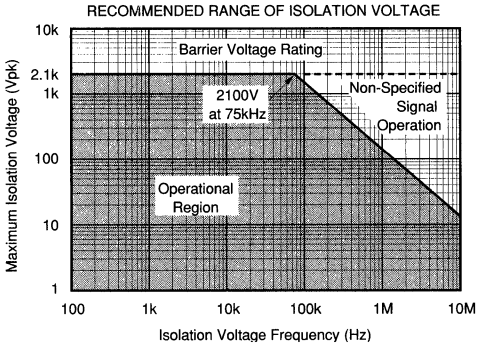
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ISO113

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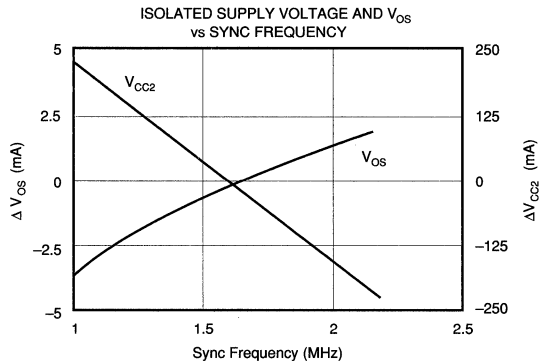
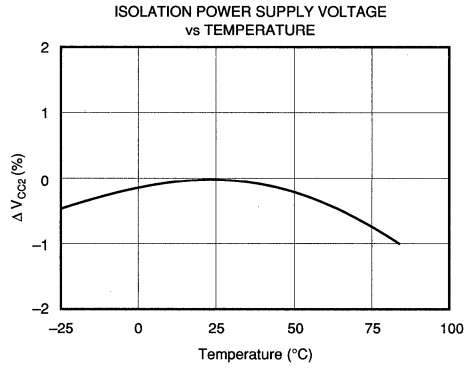
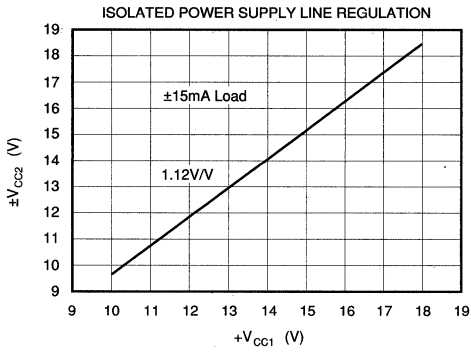
ISOLATION PRODUCTS



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TYPICAL PERFORMANCE CURVES (CONT)

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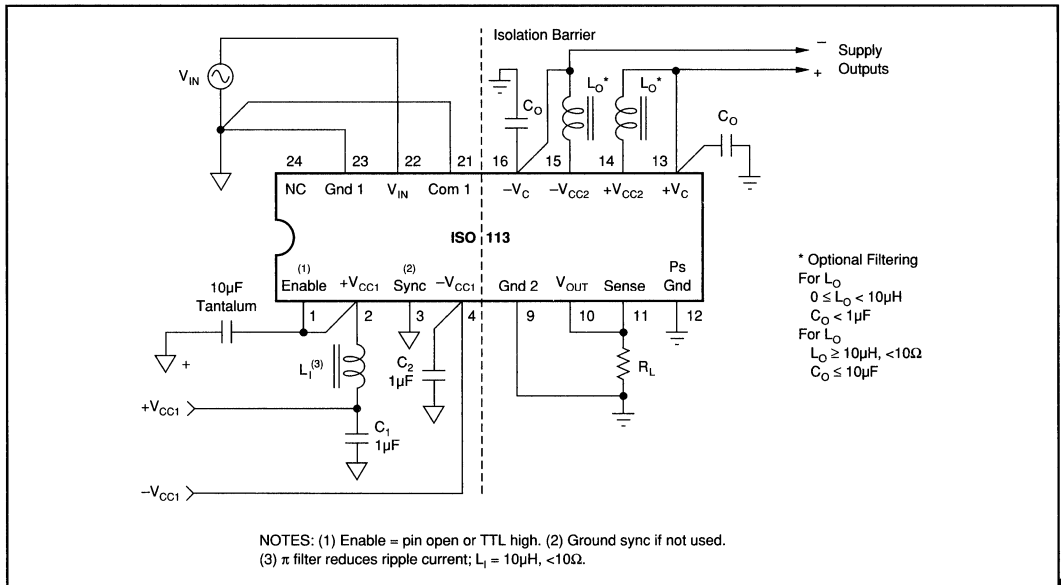


FIGURE 1. Signal and Power Connections.

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SIGNAL AND POWER CONNECTIONS

Figure 1 shows the proper power supply and signal connections. All power supply pins should be bypassed as shown with the π filter for $+V_{CC1}$, an option recommended if more than $\pm 15\text{mA}$ are drawn from the isolated supply. Separate rectifier output pins ($\pm V_{CC2}$) and amplifier supply input pins ($\pm V_C$) allow additional ripple filtering and/or regulation. The separate input common pin and output sense are low current inputs tied to the signal source ground, and output load, respectively, to minimize errors due to IR drop in long conductors. Otherwise, connect Com 1 to Gnd 1, and Sense to V_{OUT} at the ISO113 socket. The enable pin may be left open if the ISO113 is continuously operated. If not, a TTL low level will disable the internal DC/DC converter. The Sync input must be grounded for unsynchronized operation while a 1.2MHz to 2MHz TTL clock signal provides synchronization of multiple units.

The ISO113 isolation amplifier contains a transformer-coupled DC/DC converter that is powered from the input side of the isolation amplifier. All power supply pins (2, 4, 13, 14, 15, and 16) of the ISO113 have an internal $0.1\mu\text{F}$ capacitor to ground. L_1 is used to slow down fast changes in the input current to the DC/DC converter. C_1 is used to help regulate the voltage ripple caused by the current demands of the converter. L_1 , C_1 , and C_2 are optional, however, recommended for low noise applications.

The DC/DC converter creates an unregulated $\pm 15\text{V}$ output to $\pm V_{CC2}$. If the ISO113 is the only device using the DC/DC converter for power, pins 13 and 14 and pins 15 and 16 can be connected directly without C_O or L_O in the circuit. If an external capacitor is used in this configuration, it should not exceed $1\mu\text{F}$. This configuration is possible because the isolation amplifier and the DC/DC converter are synchronized internally.

If additional devices are powered by the DC/DC converter of the ISO113, the application may require that the ripple voltage of the ISO113 converter be attenuated, in which case, L_O and C_O should be added to the circuit. The inductor is used to attenuate the ripple current and a higher value capacitor can be used to reduce the ripple voltage even further.

OPTIONAL GAIN AND OFFSET ADJUSTMENTS

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 2a may be used to provide a gain trim of $\pm 0.5\%$ for the values shown. Greater range may be provided by increasing the size of R_1 and R_2 . Every $2\text{k}\Omega$ increase in R_1 will give an additional 1%

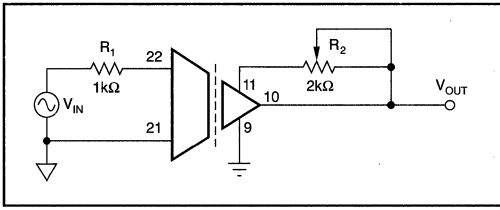


FIGURE 2a. Gain Adjust.

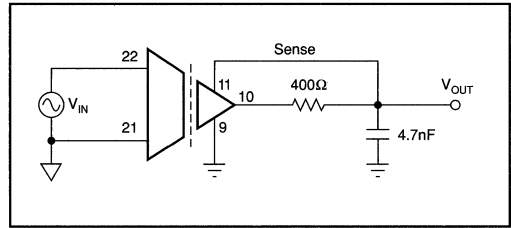


FIGURE 4. Ripple Reduction.

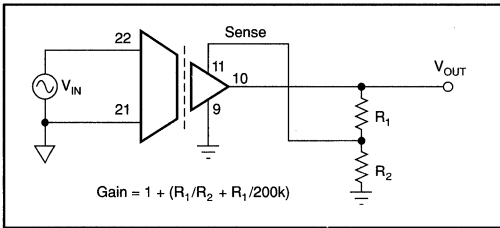


FIGURE 2b. Gain Setting.

adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictate location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 2a, the position of R_1 and R_2 may be reversed.

Gains greater than 1 may be obtained by using the circuit of Figure 2b. Note that the effect of input referred errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 3 shows a method for trimming V_{OS} of the ISO113. This circuit may be applied to Signal Com1. With the values shown, $\pm 15V$ supplies and unity gain, the circuit will provide $\pm 150mV$ adjustment range and 0.25mV resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a $\pm 100mV$ trim, power supply sensitivity is 8mV/V at the output.

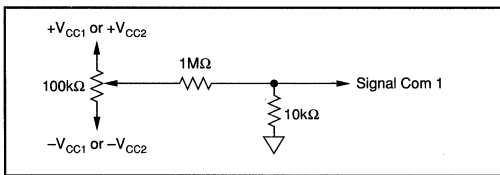


FIGURE 3. V_{OS} Adjust.

OPTIONAL OUTPUT FILTER

Figure 4 shows an optional output ripple filter that reduces the 800kHz ripple voltage to $< 5mV_{p-p}$ without compromising DC performance. The small signal bandwidth is extended above 30kHz as a result of this compensation.

MULTICHANNEL SYNCHRONIZATION

Synchronization of multiple ISO113s can be accomplished by connecting pin 3 of each device to an external TTL level oscillator, as shown in Figure 7. The PWS750-1 oscillator is convenient because its nominal synchronizing output frequency is 1.6MHz, resulting in a 800kHz carrier in the ISO113 (its nominal unsynchronized value). The open collector output typically switches 7.5mA to a 0.2V low level so that the external pull up resistor can be chosen for different pull-up voltages as shown in Figure 7. The number of channels synchronized by one PWS750-1 is determined by the total capacitance of the sync voltage conductors. They must be less than 1000pF to ensure TTL level switching at 800kHz. At higher frequencies the capacitance must be proportionally lower.

Customers can supply their own TTL level synchronization logic, provided the frequency is between 1.2MHz and 2MHz, and the duty cycle is greater than 25%.

Single or multichannel synchronization with reduced power dissipation for applications requiring less than $\pm 15mA$ from V_{CC1} is accomplished by driving both the Sync input pin (3) and Enable pin (1) with the TTL oscillator as shown in Figure 5.

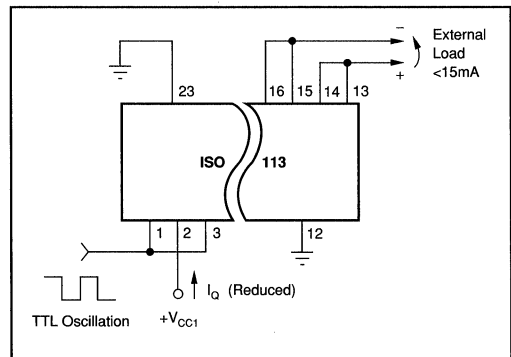


FIGURE 5. Reduced Power Dissipation.

ISOLATION BARRIER VOLTAGE

The typical performance of the ISO113 under conditions of barrier voltage stress is indicated in the first two performance curves—Recommended Range of Isolation Voltage and IMR/ Leakage vs Frequency. At low barrier modulation

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levels, errors can be determined by the IMRR characteristic. At higher barrier voltages, typical performance is obtained as long as the dv/dt across the barrier is below the shaded area in the first curve. Otherwise, the signal channel will be interrupted, causing the output to distort, and/or shift DC level. This condition is temporary, with normal operation resuming as soon as the transient subsides. Permanent damage to the integrated circuits occurs only if transients exceed $20kV/\mu s$. Even in this extreme case, the barrier integrity is assured.

HIGH VOLTAGE TESTING

The ISO113 was designed to reliably operate with 1500Vrms continuous isolation barrier voltage. To confirm barrier integrity, a two-step breakdown test is performed on 100% of the units. First, an 5657V peak, 60Hz barrier potential is applied for 10s to verify that the dielectric strength of the insulation is above this level. Following this exposure, a 1500Vrms, 60Hz potential is applied for one minute to conform to UL1244. Life-test results show reliable operation under continuous rated voltage and maximum operating temperature conditions.

APPLICATIONS

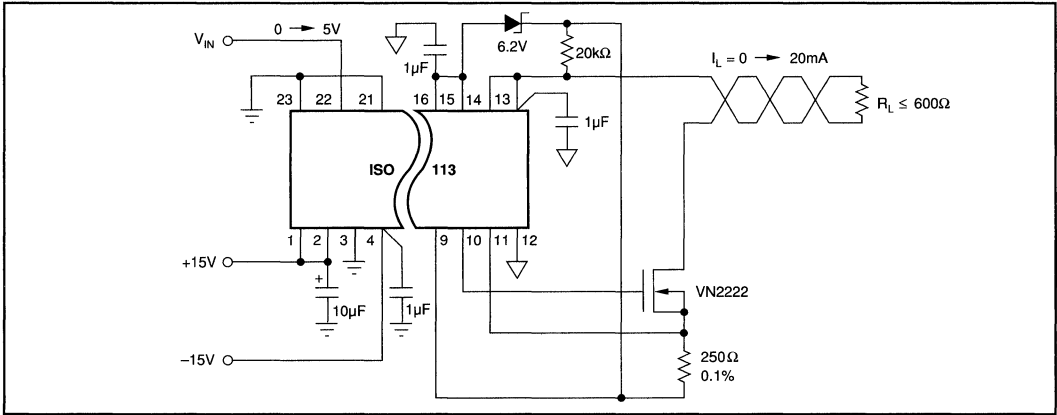
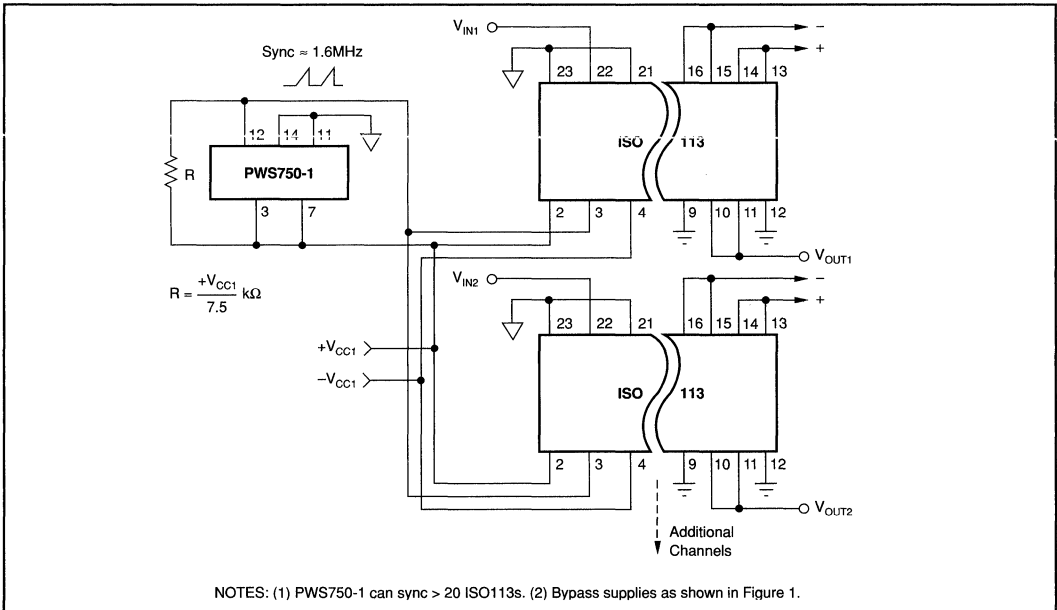


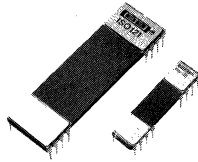
FIGURE 6. Isolated Current Loop Driver.



NOTES: (1) PWS750-1 can sync > 20 ISO113s. (2) Bypass supplies as shown in Figure 1.

FIGURE 7. Synchronized-Multichannel Isolation.

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ISO120
ISO121

Precision Low Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR PARTIAL DISCHARGE
- ISO120: Rated 1500Vrms
- ISO121: Rated 3500Vrms
- HIGH IMR: 115dB at 60Hz
- USER CONTROL OF CARRIER FREQUENCY
- LOW NONLINEARITY: $\pm 0.01\%$ max
- BIPOLAR OPERATION: $V_o = \pm 10V$
- 0.3"-WIDE 24-PIN HERMETIC DIP, ISO120
- SYNCHRONIZATION CAPABILITY
- WIDE TEMP RANGE: $-55^\circ C$ to $+125^\circ C$ (ISO120)

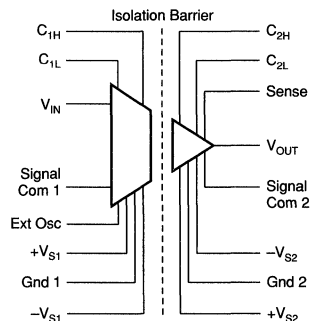
DESCRIPTION

The ISO120 and ISO121 are precision isolation amplifiers incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, which results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a hermetic DIP. The ISO120 and ISO121 differ only in package size and isolation voltage rating.

These amplifiers are easy to use. No external components are required for 60kHz bandwidth. With the addition of two external capacitors, precision specifications of 0.01% max nonlinearity and $150\mu V/^\circ C$ max V_{OS} drift are guaranteed with 6kHz bandwidth. A power supply range of $\pm 4.5V$ to $\pm 18V$ and low quiescent current make these amplifiers ideal for a wide range of applications.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- ANALYTICAL MEASUREMENTS
- BIOMEDICAL MEASUREMENTS
- DATA ACQUISITION
- TEST EQUIPMENT



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$: $V_{S1} = V_{S2} = \pm 15\text{V}$; and $R_L = 2\text{k}\Omega$, unless otherwise noted.

PARAMETER	CONDITIONS	ISO120BG, ISO121BG			ISO120G, ISO120SG ⁽⁴⁾ , ISO121G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage Rated Continuous ISO120: AC 60Hz DC	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}	1500 2121			*	*		Vrms VDC
ISO121: AC 60Hz DC	T_{MIN} to T_{MAX} T_{MIN} to T_{MAX}	3500 4950			*	*		Vrms VDC
100% Test (AC 60Hz): ISO120 ISO121	1s; Partial Discharge $\leq 5\text{pC}$ 1s; Partial Discharge $\leq 5\text{pC}$	2500 5600			*	*		Vrms Vrms
Isolation Mode Rejection ISO 120: AC 60Hz DC	1500Vrms		115 160		*	*		dB dB
ISO121: AC60Hz DC	3500Vrms		115 160		*	*		dB dB
Barrier Impedance			$10^{14} \parallel 2$		*	*		$\Omega \parallel \text{pF}$
Leakage Current	$V_{\text{ISO}} = 240\text{Vrms}, 60\text{Hz}$		0.18	0.5	*	*		μArms
GAIN⁽⁴⁾								
Nominal Gain	$V_O = \pm 10\text{V}$ $C_1 = C_2 = 1000\text{pF}$		1			1		V/V
Gain Error			± 0.04	± 0.1		± 0.05	± 0.25	%FSR
Gain vs Temperature			± 5	± 20		± 10	± 40	ppm/ $^\circ\text{C}$
Nonlinearity			± 0.005	± 0.01		± 0.01	± 0.05	%FSR
Nominal Gain	$C_1 = C_2 = 0$		1			1		V/V
Gain Error			± 0.04	± 0.25		± 0.05	± 0.25	%FSR
Gain vs Temperature			± 40			± 40		ppm/ $^\circ\text{C}$
Nonlinearity			± 0.02	± 0.1		± 0.04	± 0.1	%FSR
INPUT OFFSET VOLTAGE⁽⁴⁾								
Initial Offset vs Temperature	$C_1 = C_2 = 1000\text{pF}$		± 5	± 25		± 10	± 50	mV $\mu\text{V}/^\circ\text{C}$
Initial Offset vs Temperature	$C_1 = C_2 = 0$		± 100	± 150		± 150	± 400	mV $\mu\text{V}/^\circ\text{C}$
Initial Offset vs Supply	$\pm V_{S1}$ or $\pm V_{S2} = \pm 4.5\text{V}$ to $\pm 18\text{V}$		± 250	± 100		± 500		mV/V $\mu\text{V}/\text{VHz}$
Noise			± 2 4			± 2 4		mV/V $\mu\text{V}/\text{VHz}$
INPUT								
Voltage Range ⁽¹⁾		± 10	± 15		*	*		V
Resistance			200		*	*		k Ω
OUTPUT								
Voltage Range		± 10	± 12.5		*	*		V
Current Drive		± 5	± 15		*	*		mA
Capacitive Load Drive			0.1		*	*		μF
Ripple Voltage ⁽²⁾			10		*	*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth	$C_1 = C_2 = 0$ $C_1 = C_2 = 1000\text{pF}$		60 6 2			*		kHz kHz V/ μs
Slew Rate						*		V/ μs
Settling Time	$V_O = \pm 10\text{V}$ $C_2 = 100\text{pF}$					*		μs
0.1%	$C_1 = C_2 = 1000\text{pF}$		50			*		μs
0.01%			350			*		μs
Overload Recovery Time ⁽³⁾	50% Output Overload, $C_1 = C_2 = 0$		150			*		μs
POWER SUPPLIES								
Rated Voltage			15			*		V
Voltage Range		± 4.5		± 18		*	*	V
Quiescent Current: V_{S1} V_{S2}			± 4.0 ± 5.0	± 5.5 ± 6.5		*	*	mA mA
TEMPERATURE RANGE								
Specification: BG and G SG ⁽⁴⁾			-25 -25	85 85	-25 -55		85 125	$^\circ\text{C}$ $^\circ\text{C}$
Operating			-55	125	-55		125	$^\circ\text{C}$
Storage			-65	150	-55		150	$^\circ\text{C}$
θ_{JA} : ISO120			40			40		$^\circ\text{C}/\text{W}$
ISO121			25			25		$^\circ\text{C}/\text{W}$

*Specifications same as ISO120BG, ISO121BG.

NOTE: (1) Input voltage range = $\pm 10\text{V}$ for V_{S1} , $V_{S2} = \pm 4.5\text{VDC}$ to $\pm 18\text{VDC}$. (2) Ripple frequency is at carrier frequency. (3) Overload recovery is approximately three times the settling time for other values of C_2 . (4) The SG-grade is specified -55°C to $+125^\circ\text{C}$; performance of the SG in the -25°C to $+85^\circ\text{C}$ temperature range is the same as the BG-grade.

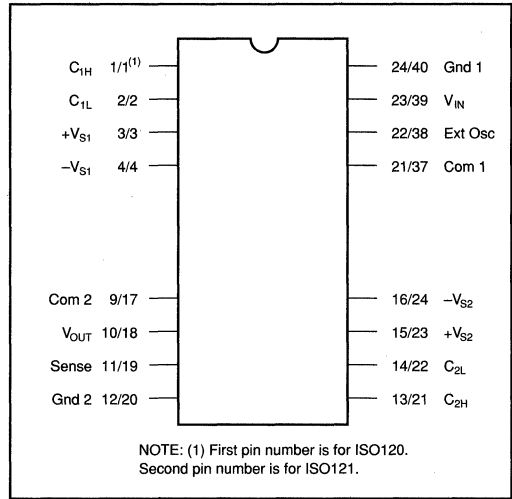
ISO120/121
5
ISOLATION PRODUCTS

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (any supply)	18V
V_{IN} Sense Voltage	$\pm 100V$
External Oscillator Input	$\pm 25V$
Signal Common 1 to Ground 1	$\pm 1V$
Signal Common 2 to Ground 2	$\pm 1V$
Continuous Isolation Voltage: ISO120	1500Vrms
ISO121	3500Vrms
V_{ISO} , dv/dt	20kV/ μs
Junction Temperature	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Duration	Continuous to Common

CONNECTION DIAGRAM



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO120G	24-Pin DIP	225
ISO120BG	24-Pin DIP	225
ISO120SG	24-Pin DIP	225
ISO121G	40-Pin DIP	206
ISO121BG	40-Pin DIP	206

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
ISO120G	-25°C to 85°C
ISO120BG	-25°C to 85°C
ISO120SG	-55°C to 125°C
ISO121G	-25°C to 85°C
ISO121BG	-25°C to 85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

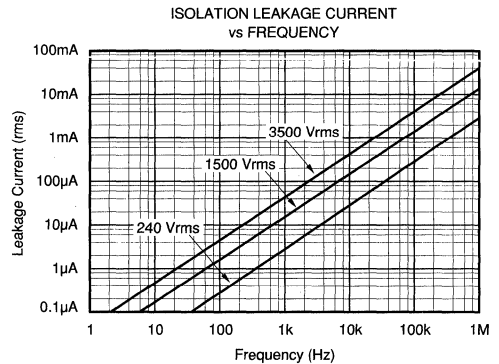
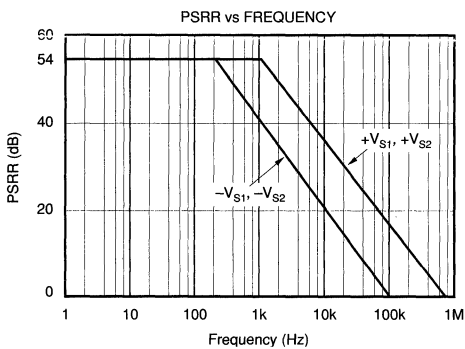
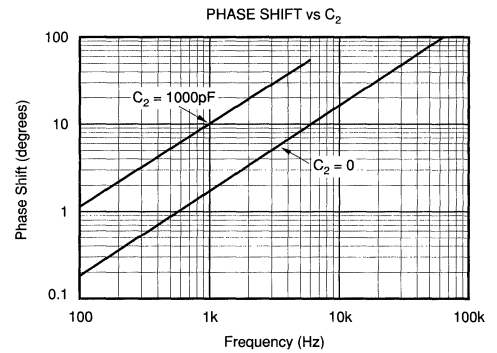
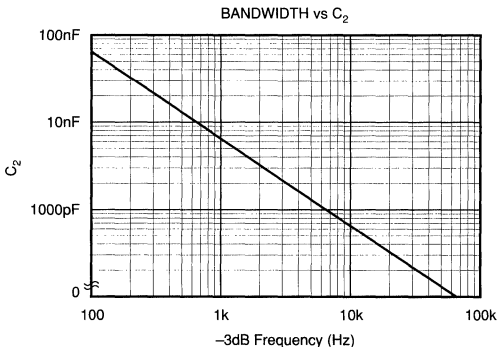
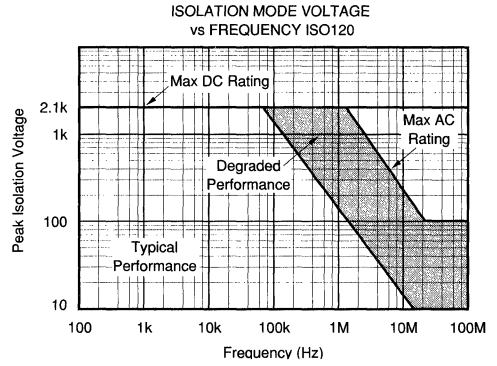
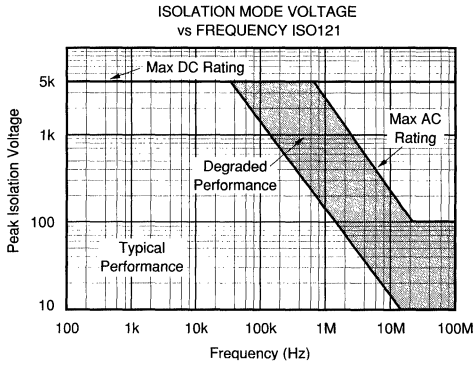
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$; $V_{S1} = V_{S2} = \pm 15\text{V}$; and $R_L = 2\text{k}\Omega$, unless otherwise noted.



ISO120/121

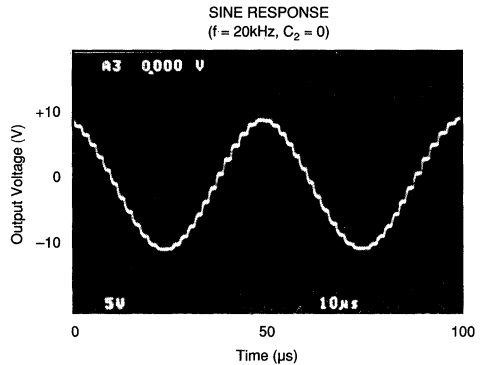
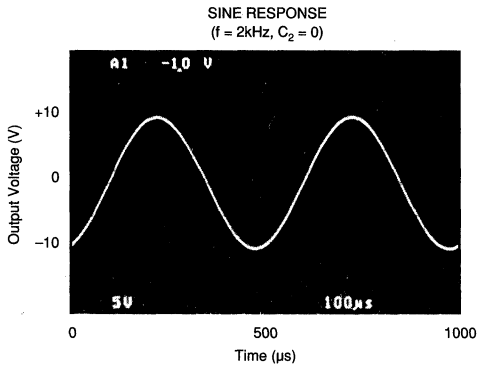
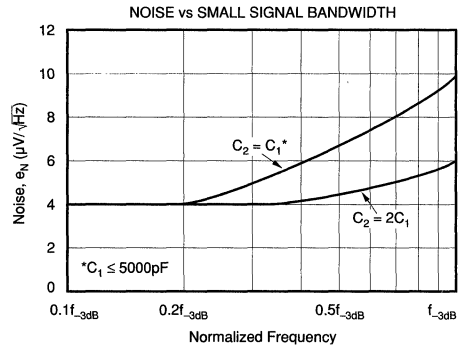
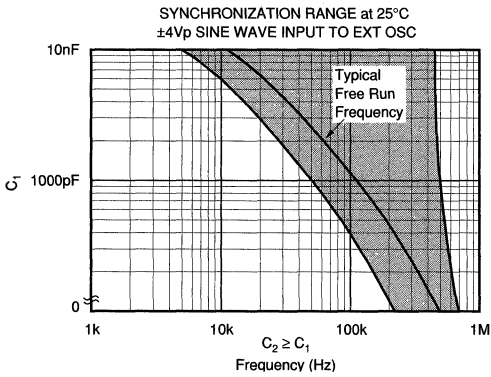
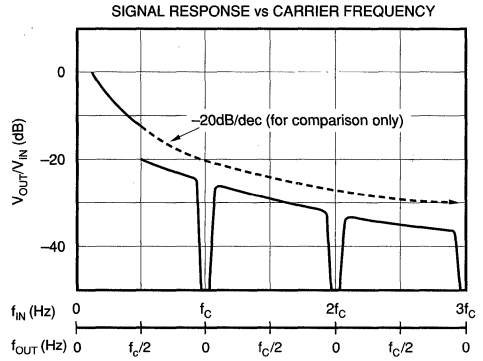
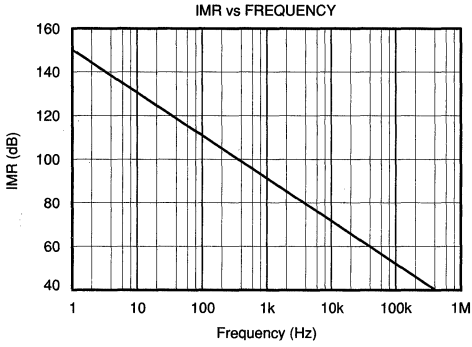
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ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES (CONT)

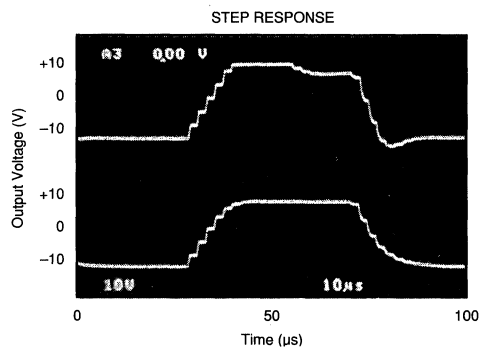
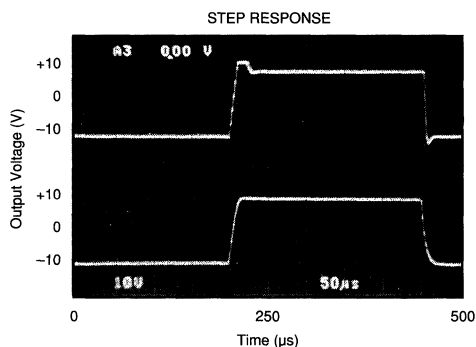
$T_A = +25^\circ\text{C}$; $V_{ST} = V_{SZ} = \pm 15\text{V}$; and $R_L = 2\text{k}\Omega$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$; $V_{S1} = V_{S2} = \pm 15\text{V}$; and $R_L = 2\text{k}\Omega$, unless otherwise noted.



THEORY OF OPERATION

The ISO120 and ISO121 isolation amplifiers comprise input and output sections galvanically isolated by matched 1pF capacitors built into the ceramic barrier. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. The input and output sections are laser-trimmed for exceptional matching of circuitry common to both input and output sections.

FREE-RUNNING MODE

An input amplifier (A1, Figure 1) integrates the difference between the input current ($V_{IN}/200\text{k}\Omega$) and a switched $\pm 100\mu\text{A}$ current source. This current source is implemented by a switchable $200\mu\text{A}$ source and a fixed $100\mu\text{A}$ current sink. To understand the basic operation of the input section, assume that $V_{IN} = 0$. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 near zero volts. This action converts the input voltage to a duty-cycle modulated triangular waveform at the output of A1 with a frequency determined by the internal 150pF capacitor. The comparator generates a fast rise time square wave that is simultaneously fed back to keep A1 in charge balance and also across the barrier to a differential sense amplifier with high common-mode rejection characteristics. The sense amplifier drives a switched current source surrounding A2. The output stage balances the duty-cycle modulated current against the feedback current through the $200\text{k}\Omega$ feedback resistor, resulting in an average value at the Sense pin equal to V_{IN} . The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

SYNCHRONIZED MODE

A unique feature of the ISO120 and ISO121 is the ability to synchronize the modulator to an external signal source. This capability is useful in eliminating trouble-some beat frequencies in multi-channel systems and in rejecting AC signals and their harmonics. To use this feature, external capacitors are connected at C_1 and C_2 (Figure 1) to change the free-running carrier frequency. An external signal is applied to the Ext Osc pin. This signal forces the current source to switch at the frequency of the external signal. If V_{IN} is zero, and the external source has a 50% duty cycle, operation proceeds as described above, except that the switching frequency is that of the external source. If the external signal has a duty cycle other than 50%, its average value is not zero. At start-up, the current source does not switch until the integrator establishes an output equal to the average DC value of the external signal. At this point, the external signal is able to trigger the current source, producing a triangular waveform, symmetrical about the new DC value, at the output of A1. For $V_{IN} = 0$, this waveform has a 50% duty cycle. As V_{IN} varies, the waveform retains its DC offset, but varies in duty cycle to maintain charge balance around A1. Operation of the demodulator is the same as outlined above.

Synchronizing to a Sine or Triangle Wave External Clock

The ideal external clock signal for the ISO120/121 is a $\pm 4\text{V}$ sine wave or $\pm 4\text{V}$, 50% duty-cycle triangle wave. The *ext osc* pin of the ISO120/121 can be driven directly with a $\pm 3\text{V}$ to $\pm 5\text{V}$ sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

Synchronizing to signals below 400kHz requires the addition of two external capacitors to the ISO120/121. Connect one capacitor in parallel with the internal modulator capacitor and connect the other capacitor in parallel with the internal demodulator capacitor as shown in Figure 1.



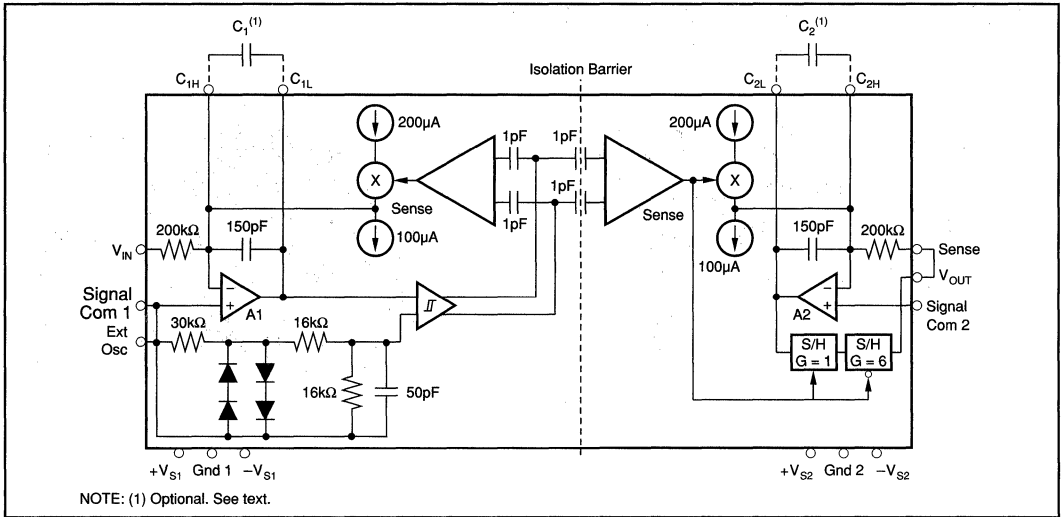


FIGURE 1. Block Diagram.

The value of the external modulator capacitor, C_1 , depends on the frequency of the external clock signal. Table I lists recommended values.

EXTERNAL CLOCK FREQUENCY RANGE	C_1, C_2 ISO120/121 MODULATOR, DEMODULATOR EXTERNAL CAPACITOR
400kHz to 700kHz	none
200kHz to 400kHz	500pF
100kHz to 200kHz	1000pF
50kHz to 100kHz	2200pF
20kHz to 50kHz	4700pF
10kHz to 20kHz	0.01μF
5kHz to 10kHz	0.022μF

TABLE I. Recommended ISO120/121 External Modulator/Demodulator Capacitor Values vs External Clock Frequency.

The value of the external demodulator capacitor, C_2 , depends on the value of the external modulator capacitor. To assure stability, C_2 must be greater than $0.8 \cdot C_1$. A larger value for C_2 will decrease bandwidth and improve stability:

$$f_{-3\text{ dB}} \approx \frac{1.2}{200\text{k}\Omega (150\text{ pF} + C_2)}$$

Where:

$f_{-3\text{ dB}}$ \approx -3dB bandwidth of ISO amp with external C_2 (Hz)
 C_2 = External demodulator capacitor (f)

For example, with $C_2 = 0.01\mu\text{F}$, the $f_{-3\text{ dB}}$ bandwidth of the ISO120/121 is approximately 600Hz.

Synchronizing to a 400kHz to 700kHz Square-Wave External Clock

At frequencies above 400kHz, an internal clamp and filter provides signal conditioning so that a square-wave signal can be used to directly drive the ISO120/121. A square-wave external clock signal can be used to directly drive the ISO120/121 *ext osc* pin if: the signal is in the 400kHz to 700kHz frequency range with a 25% to 75% duty cycle, and $\pm 3\text{V}$ to $\pm 20\text{V}$ level. Details of the internal clamp and filter circuitry are shown in Figure 1.

Synchronizing to a 10% to 90% Duty-cycle External Clock

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO120/121 *ext osc* pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X , proportionally. e.g. for a $\pm 4\text{V}$ square wave (8Vp-p) R_X should be increased to 2kΩ.

The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. Table II shows recommended capacitor values.

Note: For external clock frequencies below 400kHz, external modulator/demodulator capacitors are required on the ISO120/121 as before.

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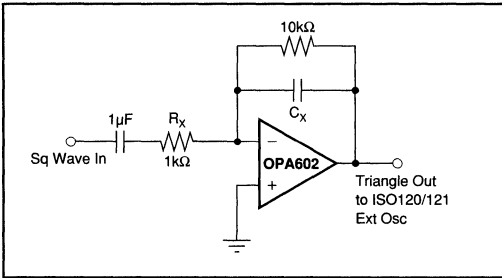


FIGURE 2. Square Wave to Triangle Wave Signal Conditioner for Driving ISO120/121 Ext Osc Pin.

EXTERNAL CLOCK FREQUENCY RANGE	C_x
400kHz to 700kHz	30pF
200kHz to 400kHz	180pF
100kHz to 200kHz	680pF
50kHz to 100kHz	1800pF
20kHz to 50kHz	3300pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE II. Recommended C_x Values vs Frequency for Figure 2 Circuit.

BASIC OPERATION

Signal and Power Connections

Figure 3 shows proper power and signal connections. Each power supply pin should be bypassed with 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Signal Common must have a path to ground for bias current return and should be maintained within ±1V of Gnd. The output sense pin may be

connected directly to V_{OUT} or may be connected to a remote load to eliminate errors due to IR drops. Pins are provided for use of external integrator capacitors. The C_{1H} and C_{2H} pins are connected to the integrator summing junctions and are therefore particularly sensitive to external pickup. This sensitivity will most often appear as degraded IMR or PSR performance. AC or DC currents coupled into these pins results in $V_{ERROR} = I_{ERROR} \times 200k\Omega$ at the output. Guarding of these pins to their respective Signal Common, or C_{1L} and C_{2L} is strongly recommended. For similar reasons, long traces or physically large capacitors are not desirable. If wound-foil capacitors are used, the outside foil should be connected to C_{1L} and C_{2L} , respectively.

Optional Gain and Offset Adjustments

Rated gain accuracy and offset performance can be achieved with no external adjustments, but the circuit of Figure 4a may be used to provide a gain trim of ±0.5% for values shown; greater range may be provided by increasing the size of R_1 and R_2 . Every 2kΩ increase in R_1 will give an additional 1% adjustment range, with $R_2 \geq 2R_1$. If safety or convenience dictates location of the adjustment potentiometer on the other side of the barrier from the position shown in Figure 4a, the positions of R_1 and R_2 may be reversed. Gains greater than one may be obtained by using the circuit of Figure 4b. Note that the effect of input offset errors will be multiplied at the output in proportion to the increase in gain. Also, the small-signal bandwidth will be decreased in inverse proportion to the increase in gain. In most instances, a precision gain block at the input of the isolation amplifier will provide better overall performance.

Figure 5 shows a method for trimming V_{OS} of the ISO120 and ISO121. This circuit may be applied to either Signal Com (input or output) as desired for safety or convenience. With the values shown, ±15V supplies and unity gain, the circuit will provide ±150mV adjustment range and 0.25mV

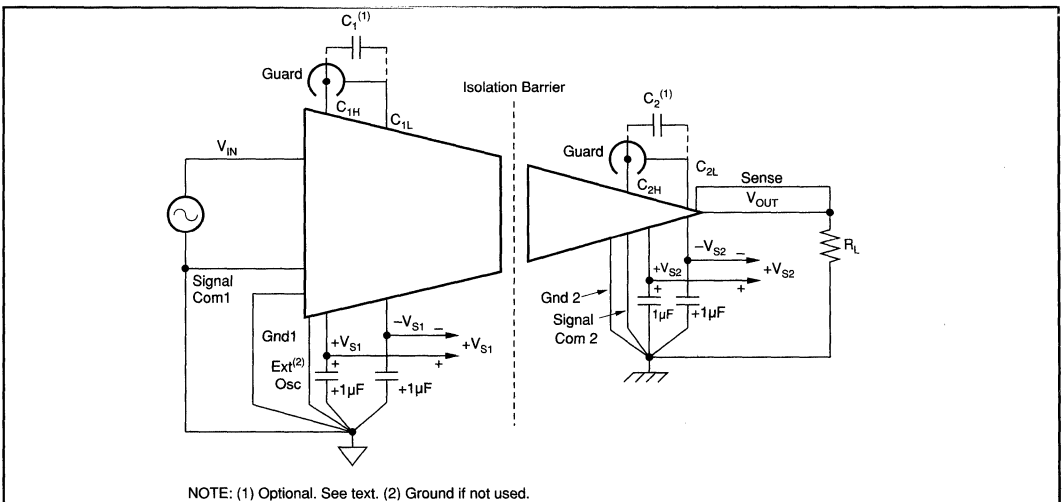


FIGURE 3. Power and Signal Connections.



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resolution with a typical trim potentiometer. The output will have some sensitivity to power supply variations. For a $\pm 100\text{mV}$ trim, power supply sensitivity is 8mV/V at the output.

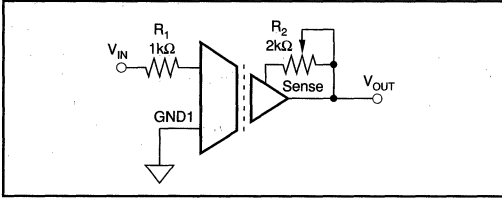


FIGURE 4a. Gain Adjust.

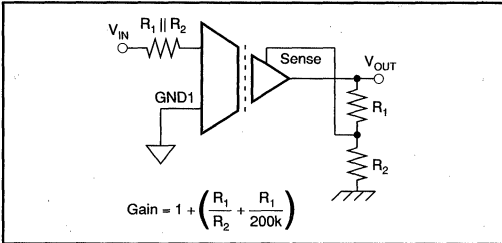


FIGURE 4b. Gain Setting.

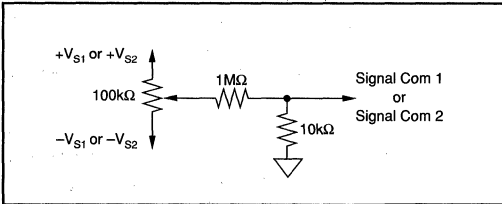


FIGURE 5. V_{OS} Adjust.

CARRIER FREQUENCY CONSIDERATIONS

As previously discussed, the ISO120 and ISO121 amplifiers transmit the signal across the iso-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency, f_c . For signal frequencies above $f_c/2$, the behavior becomes more complex. The Signal Response vs Carrier Frequency performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to $f_c/2$. At input frequencies at or above $f_c/2$, the device generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications. It should be noted that when C_1 is zero, the carrier frequency is nominally 500kHz and the -3dB point of the amplifier is 60kHz . Spurious signals at the

output are not significant under these circumstances unless the input signal contains significant components above 250kHz .

There are two ways to use these characteristics. One is to move the carrier frequency low enough that the troublesome signal components are attenuated to an acceptable level as shown in Signal Response vs Carrier Frequency. This in effect limits the bandwidth of the amplifier. The Synchronization Range performance curve shows the relationship between carrier frequency and the value of C_1 . To maintain stability, C_2 must also be connected and must be equal to or larger in value than C_1 . C_2 may be further increased in value for additional attenuation of the undesired signal components and provides the additional benefit of reducing the residual carrier ripple at the output. See the Bandwidth vs C_2 performance curve.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO120 and ISO121 can be used to reject this noise. The amplifier can be synchronized to an external frequency source, f_{EXT} , placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the Signal Response vs Carrier Frequency performance curve. For proper synchronization, choose C_1 as shown in the Synchronization Range performance curve. Remember that $C_2 \geq C_1$ is a necessary condition for stability of the isolation amplifier. This curve shows the range of lock at the fundamental frequency for a 4V sinusoidal signal source. The applications section shows the ISO120 and ISO121 synchronized to isolation power supplies, while Figure 6 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

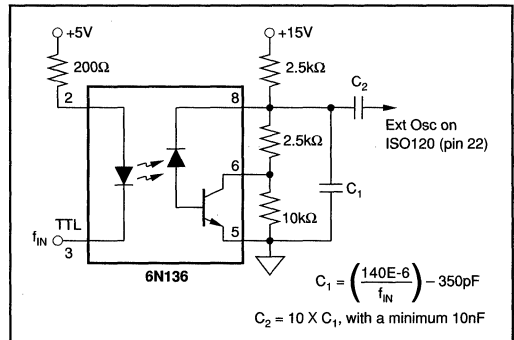


FIGURE 6. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

ISOLATION MODE VOLTAGE

Isolation mode voltage (IMV) is the voltage appearing between isolated grounds Gnd 1 and Gnd 2. IMV can induce error at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds $f_c/2$, the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the Signal Response vs Carrier Frequency performance curve. This occurs

because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in IMR vs Frequency performance curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response vs Carrier Frequency performance curve. Due to effects of very high-frequency signals, typical IMV performance can be achieved only when dV/dT of the isolation mode voltage falls below $1000V/\mu s$. For convenience, this is plotted in the typical performance curves for the ISO120 and ISO121 as a function of voltage and frequency for sinusoidal voltages. When dV/dT exceeds $1000V/\mu s$ but falls below $20kV/\mu s$, performance may be degraded. At rates of change above $20kV/\mu s$, the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below $\pm 15V$ may decrease the dV/dT to $500V/\mu s$ for typical performance, but the maximum dV/dT of $20kV/\mu s$ remains unchanged.

Leakage current is determined solely by the impedance of the 2pF barrier capacitance and is plotted in the Isolation Leakage Current vs Frequency curve.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one. Historically, Burr-Brown has chosen a deliberately conservative one: $V_{TEST} = (2 \times AC_{rms} \text{ continuous rating}) + 1000V$ for 10 seconds, followed by a test at rated AC_{rms} voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO120 and ISO121.

Partial Discharge

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize,

effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. Since the ISO120 and ISO121 do not use organic insulation, partial discharge is non-destructive.

The inception voltage for these voids tends to be constant, so that the measurement of *total charge* being redistributed within the dielectric is a very good indicator of the size of the voids and *their likelihood of becoming an incipient failure*. The *bulk inception voltage*, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the *absolute maximum voltage* (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the *bulk extinction voltage* provides a lower, more conservative voltage from which to derive a *safe continuous rating*. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

Partial Discharge Testing

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE, the national standards group in Germany and an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display $\leq 5pC$ partial discharge level in a 100% production test.

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APPLICATIONS

The ISO120 and ISO121 isolation amplifiers are used in three categories of applications:

1. Accurate isolation of signals from high voltage ground potentials,

2. Accurate isolation of signals from severe ground noise and,

3. Fault protection from high voltages in analog measurements.

Figures 7 through 12 show a variety of Application Circuits.

APPLICATION CIRCUITS

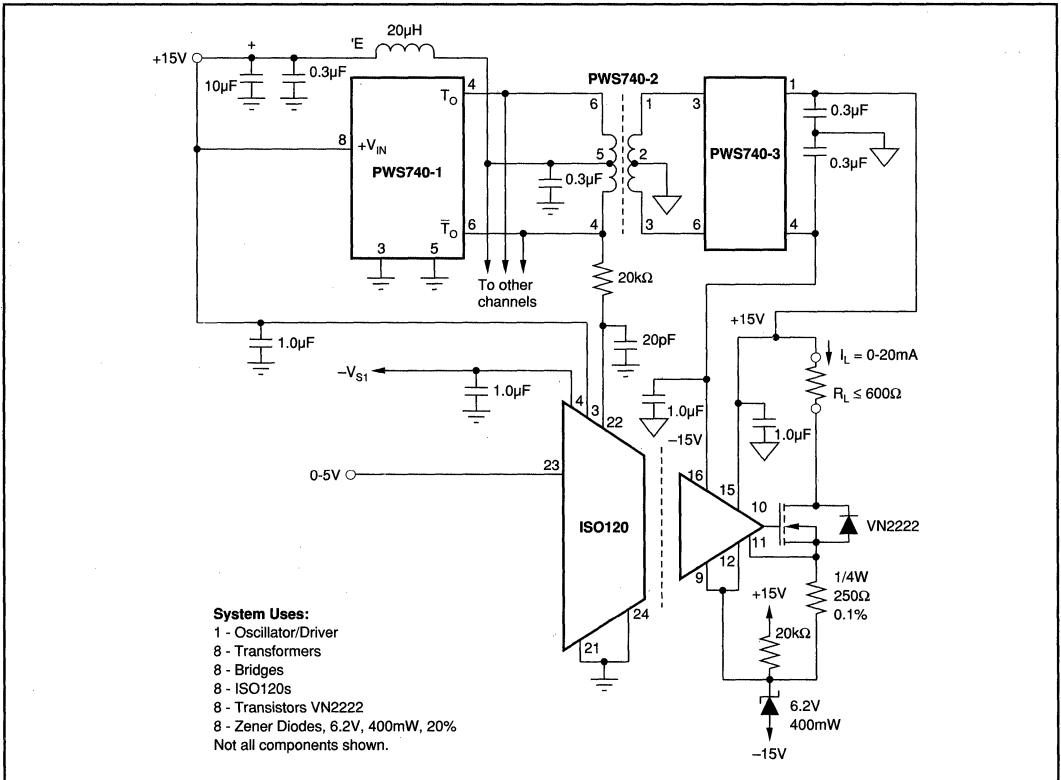


FIGURE 7. Eight-channel Isolated 0-20mA Loop Driver.

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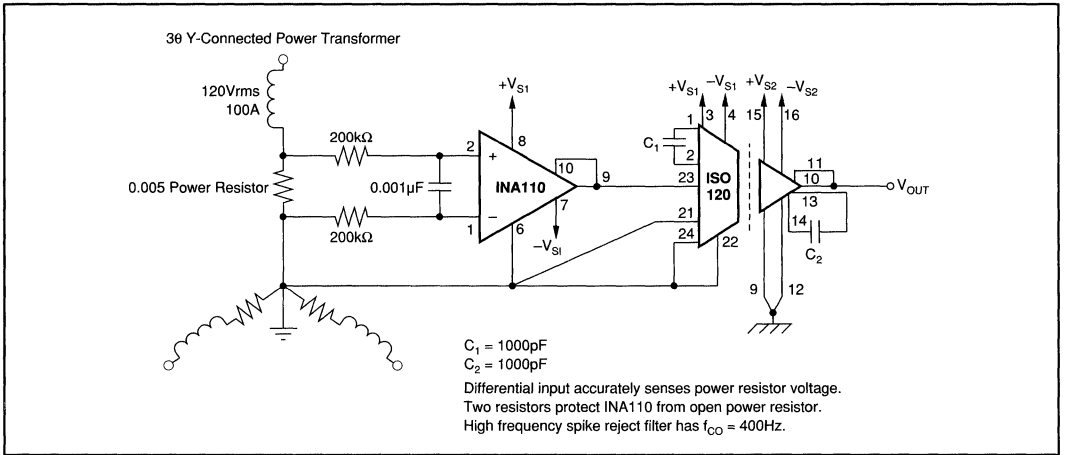


FIGURE 8. Isolated Powerline Monitor.

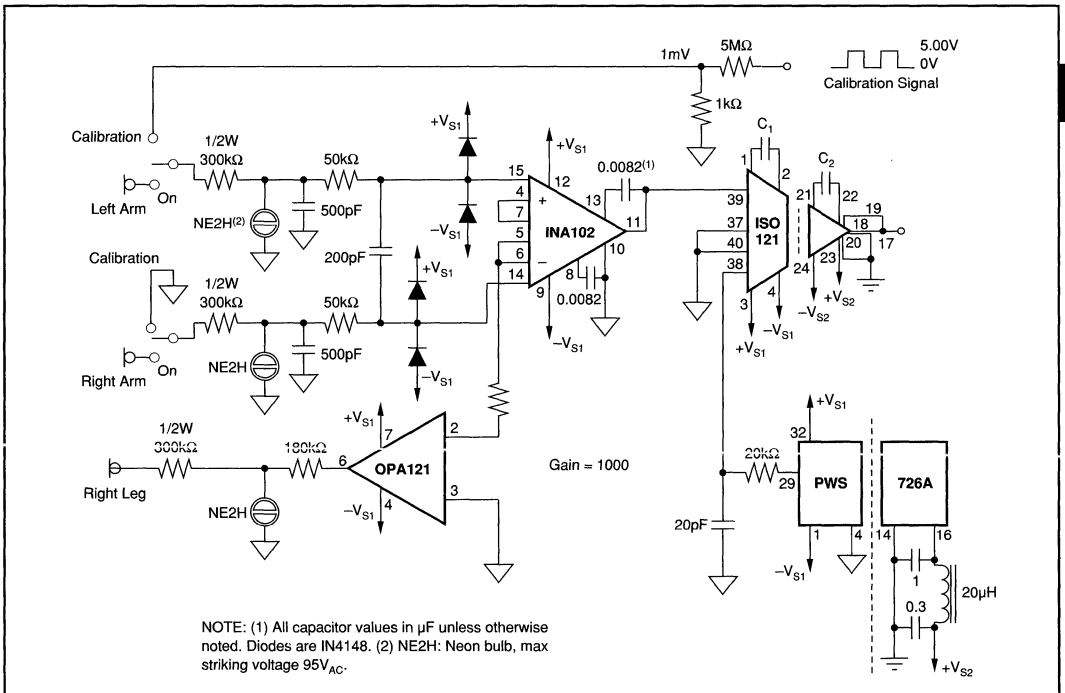


FIGURE 9. Right-Leg Driven ECG Amplifier (with defibrillator protection and calibration).

ISO120/121

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ISOLATION PRODUCTS

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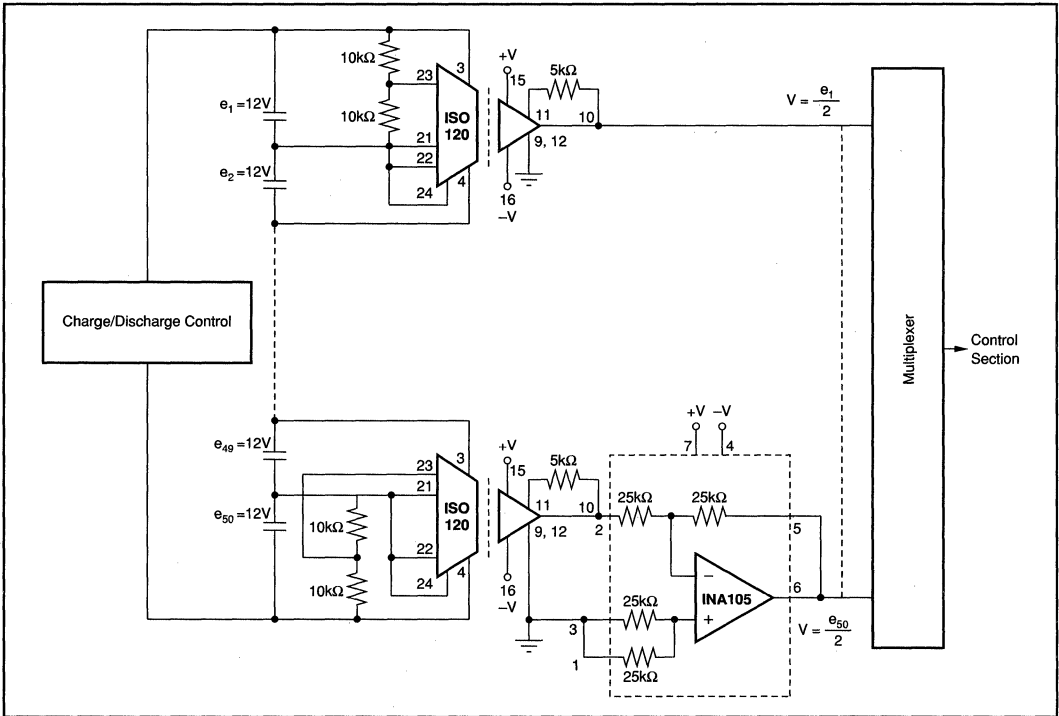


FIGURE 10. Battery Monitor for a 600V Battery Power System.

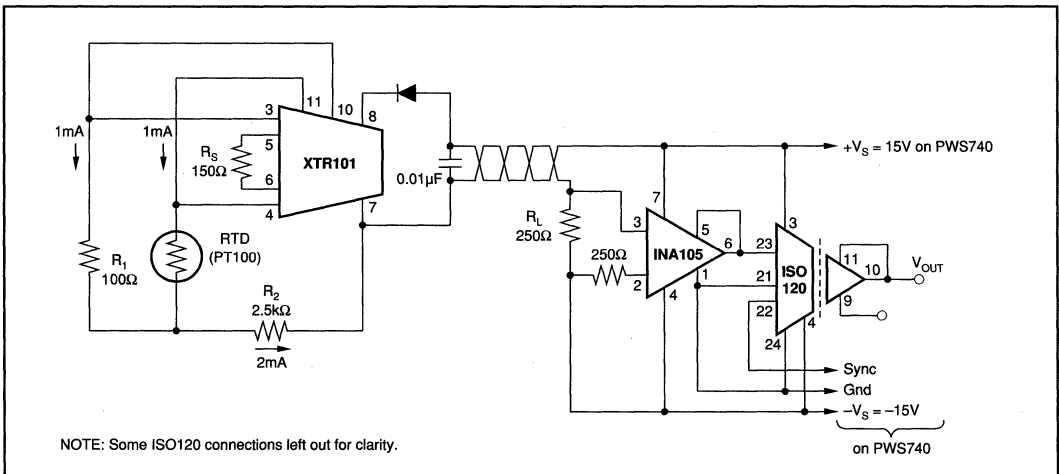
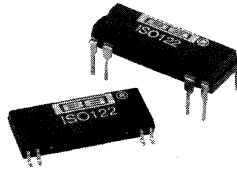


FIGURE 11. Isolated 4-20mA Instrument Loop. (RTD shown).

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ISO122

Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: $V_o = \pm 10V$
- 16-PIN PLASTIC DIP AND 28-LEAD SOIC
- EASE OF USE: Fixed Unity Gain Configuration
- 0.020% max NONLINEARITY
- $\pm 4.5V$ to $\pm 18V$ SUPPLY RANGE

APPLICATIONS

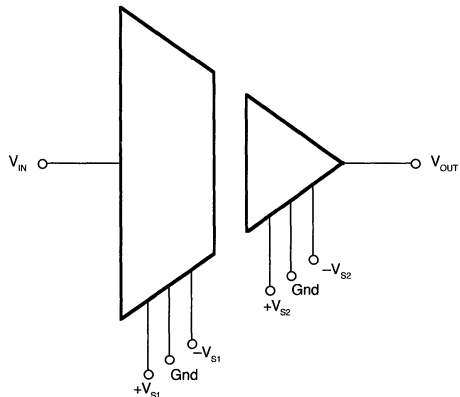
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The ISO122 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122 is easy to use. No external components are required for operation. The key specifications are 0.020% max nonlinearity, 50kHz signal bandwidth, and $200\mu V/^\circ C$ V_{OS} drift. A power supply range of $\pm 4.5V$ to $\pm 18V$ and quiescent currents of $\pm 5.0mA$ on V_{S1} and $\pm 5.5mA$ on V_{S2} make these amplifiers ideal for a wide range of applications.

The ISO122 is available in 16-pin plastic DIP and 28-lead plastic surface mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_{S1} = V_{S2} = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	ISO122P/U			ISO122JP/JU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage Rated Continuous AC 60Hz 100% Test ⁽¹⁾	1s, 5pc PD 60Hz	1500 2400			*	*		VAC VAC
Isolation Mode Rejection			140			*		dB
Barrier Impedance			$10^{14} \parallel 2$			*		$\Omega \parallel \text{pF}$
Leakage Current at 60Hz	$V_{\text{ISO}} = 240\text{Vrms}$		0.18	0.5		*	*	μArms
GAIN	$V_O = \pm 10\text{V}$							
Nominal Gain			1			*	*	V/V
Gain Error			± 0.05	± 0.50		*	*	%FSR
Gain vs Temperature			± 10			*		ppm/ $^\circ\text{C}$
Nonlinearity ⁽²⁾			± 0.016	± 0.020		± 0.025	± 0.050	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset			± 20	± 50		*	*	mV
vs Temperature			± 200			*		$\mu\text{V}/^\circ\text{C}$
vs Supply			± 2			*		mV/V
Noise			4			*		$\mu\text{V}/\sqrt{\text{Hz}}$
INPUT								
Voltage Range		± 10	± 12.5		*	*		V
Resistance			200			*		k Ω
OUTPUT								
Voltage Range		± 10	± 12.5		*	*		V
Current Drive		± 5	± 15		*	*		mA
Capacitive Load Drive			0.1			*		μF
Ripple Voltage ⁽³⁾			20			*		mVp-p
FREQUENCY RESPONSE								
Small Signal Bandwidth	$V_O = \pm 10\text{V}$		50			*		kHz
Slew Rate			2			*		V/ μs
Settling Time						*		μs
0.1%			50			*		μs
0.01%			350			*		μs
Overload Recover Time			150			*		μs
POWER SUPPLIES								
Rated Voltage			± 15			*	*	V
Voltage Range		± 4.5		± 18	*	*	*	V
Quiescent Current: V_{S1}			± 5.0	± 7.0		*	*	mA
V_{S2}			± 5.5	± 7.0		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	$^\circ\text{C}$
Operating		-25		+85	*		*	$^\circ\text{C}$
Storage		-40		+85	*		*	$^\circ\text{C}$
θ_{JA}			100			*	*	$^\circ\text{C}/\text{W}$
θ_{JC}			65			*	*	$^\circ\text{C}/\text{W}$

* Specification same as ISO122P/U.

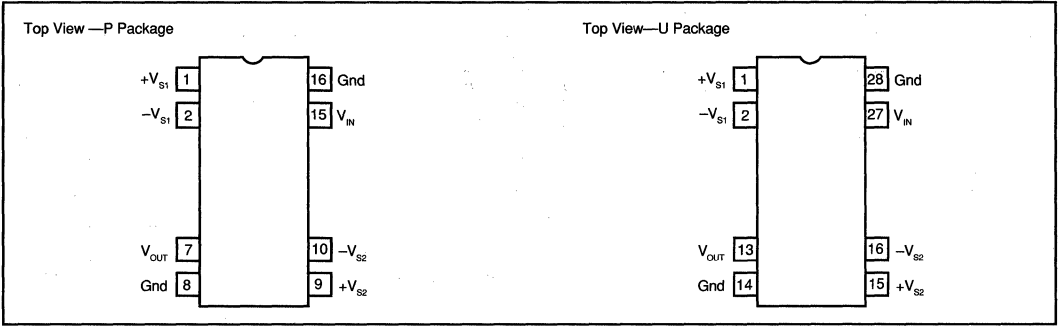
NOTES: (1) Tested at 1.6 X rated, fail on 5pC partial discharge. (2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (3) Ripple frequency is at carrier frequency (500kHz).

ISO122
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ISOLATION PRODUCTS

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CONNECTION DIAGRAM



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO122P	16-Pin Plastic DIP	238
ISO122JP	16-Pin Plastic DIP	238
ISO122U	28-Pin Plastic SOIC	217-1
ISO122JU	28-Pin Plastic SOIC	217-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

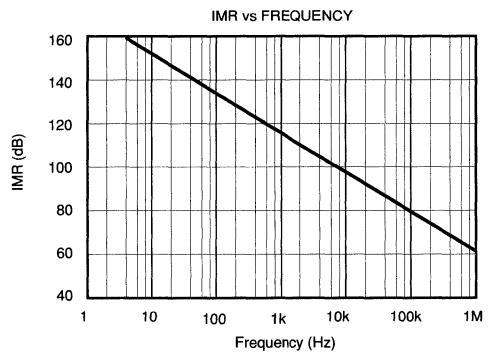
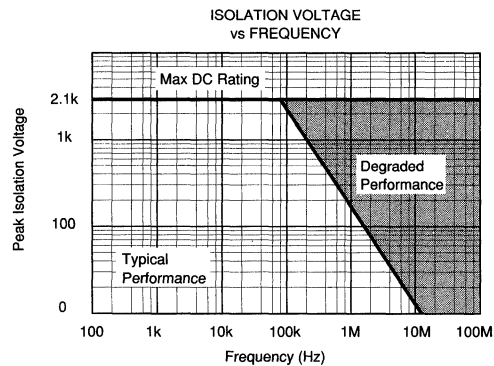
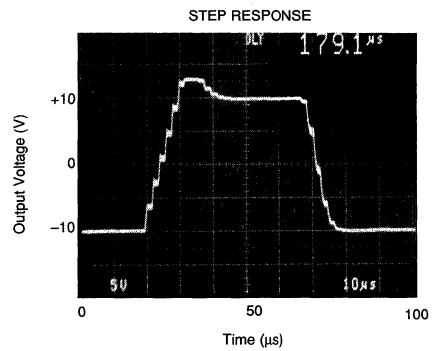
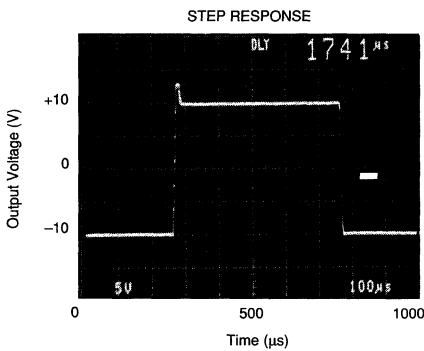
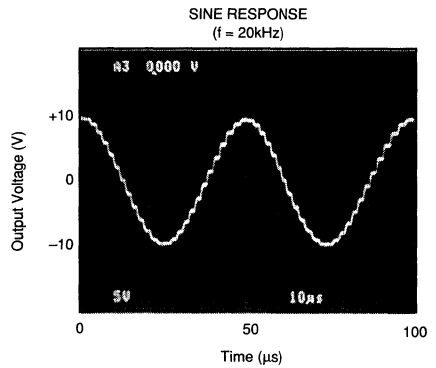
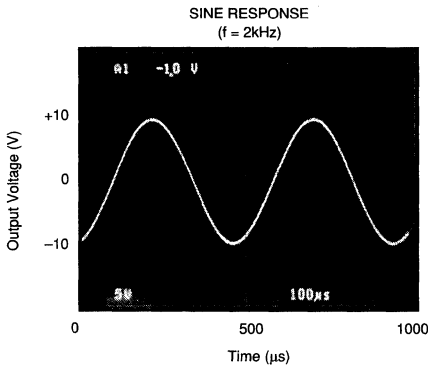
ORDERING INFORMATION

MODEL	PACKAGE	NONLINEARITY MAX %FSR
ISO122P	Plastic DIP	±0.020
ISO122JP	Plastic DIP	±0.050
ISO122U	Plastic SOIC	±0.020
ISO122JU	Plastic SOIC	±0.050

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



ISO122

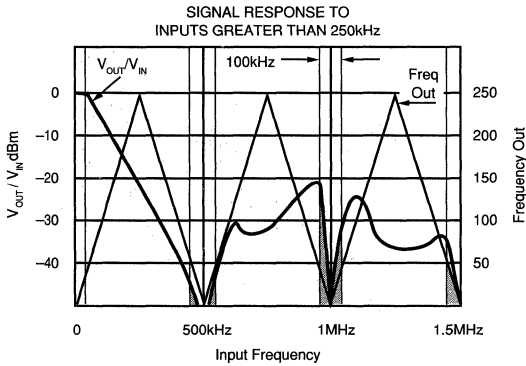
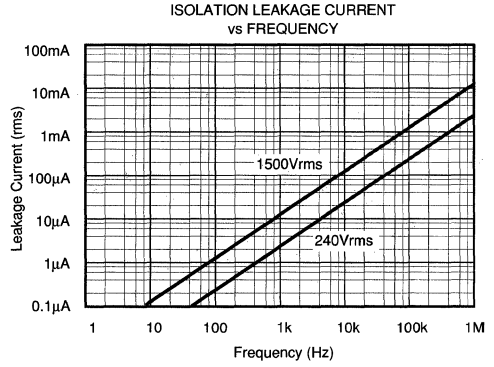
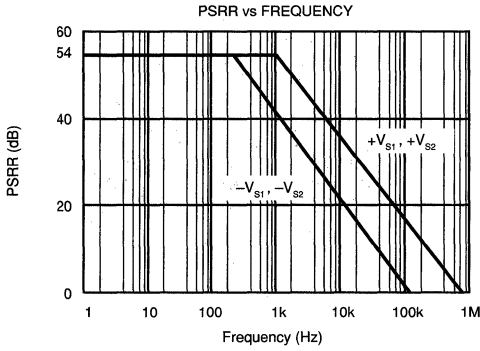
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ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_G = \pm 15\text{V}$ unless otherwise noted.



(NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.)

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THEORY OF OPERATION

The ISO122 isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections. The transistor count of the ISO122 is 250 transistors.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current ($V_{IN}/200k\Omega$) and a switched $\pm 100\mu A$ current source. This current source is implemented by a switchable $200\mu A$ source and a fixed $100\mu A$ current sink. To understand the basic operation of the modulator, assume that $V_{IN} = 0.0V$. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at 500kHz. The resultant capacitor drive is a complementary duty-cycle modulation square wave.

DEMODULATOR

The sense amplifier detects the signal transitions across the capacitive barrier and drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the $200k\Omega$ feedback resistor, resulting in an average value at the

V_{OUT} pin equal to V_{IN} . The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

BASIC OPERATION

SIGNAL AND SUPPLY CONNECTIONS

Each power supply pin should be bypassed with $1\mu F$ tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a π filter on the supplies (see Figure 4). ISO122 output has a 500kHz ripple of 20mV, which can be removed with a simple two pole low-pass filter with a 100kHz cutoff using a low cost op amp. See Figure 4.

The input to the modulator is a current (set by the $200k\Omega$ integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least $\pm 15V$. It is therefore possible when using an unregulated DC/DC converter to minimize PSR related output errors with $\pm 5V$ voltage regulators on the isolated side and still get the full $\pm 10V$ input and output swing. An example of this application is shown in Figure 10.

CARRIER FREQUENCY CONSIDERATIONS

The ISO122 amplifier transmits the signal across the isolation barrier by a 500kHz duty cycle modulation technique. For input signals having frequencies below 250kHz, this system works like any linear amplifier. But for frequencies above 250kHz, the behavior is similar to that of a sampling amplifier. The signal response to inputs greater than 250kHz

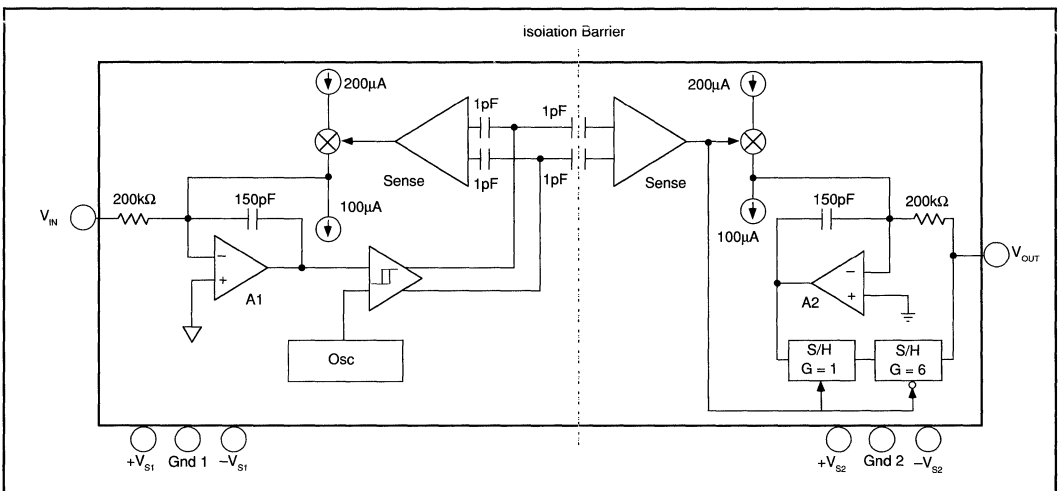


FIGURE 1. Block Diagram.

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performance curve shows this behavior graphically; at input frequencies above 250kHz the device generates an output signal component of reduced magnitude at a frequency below 250kHz. This is the aliasing effect of sampling at frequencies less than 2 times the signal frequency (the Nyquist frequency). Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

ISOLATION MODE VOLTAGE INDUCED ERRORS

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250kHz, the output also will display spurious outputs (aliasing), in a manner similar to that for $V_{IN} > 250\text{kHz}$ and the amplifier response will be identical to that shown in the Signal Response to Inputs Greater Than 250kHz performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the IMR vs Frequency curve and compute the amplifier response to this input-referred error signal from the data given in the Signal Response to Inputs Greater than 250kHz performance curve. For example, if a 800kHz 1000Vrms IMR is present, then a total of $[(-60\text{dB}) + (-30\text{dB})] \times (1000\text{V}) = 32\text{mV}$ error signal at 200kHz plus a 1V, 800kHz error signal will be present at the output.

HIGH IMV dV/dt ERRORS

As the IMV frequency increases and the dV/dt exceeds 1000V/ μs , the sense amp may start to false trigger, and the output will display spurious errors. The common mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power supply voltages below $\pm 15\text{V}$ may decrease the dV/dt to 500V/ μs for typical performance.

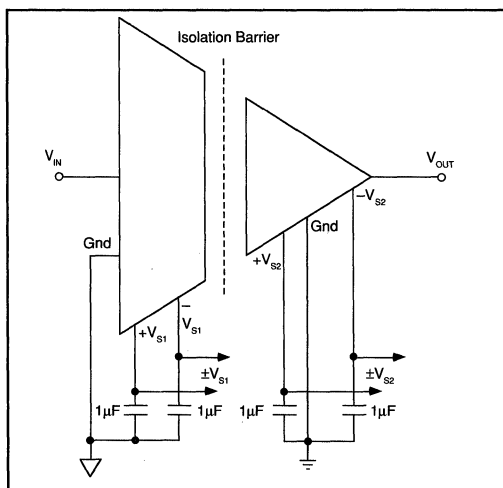


FIGURE 2. Basic Signal and Power Connections.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses ($<5\text{pC}$) while applying 2400Vrms, 60Hz high voltage stress across every ISO122 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage ($1.6 \times 1500\text{Vrms}$) protection without damage to the ISO122. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state of the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01-0.1 μs current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." We have characterized and developed the package insulation processes to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not damage the ISO122. The extinction voltage is above 1500Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500Vrms (rated) level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

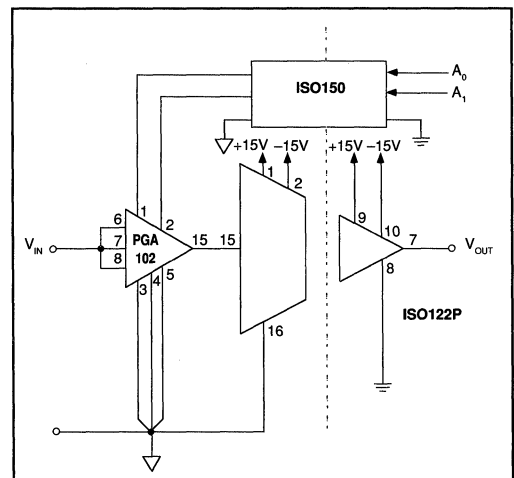


FIGURE 3. Programmable-Gain Isolation Channel with Gains of 1, 10, and 100.

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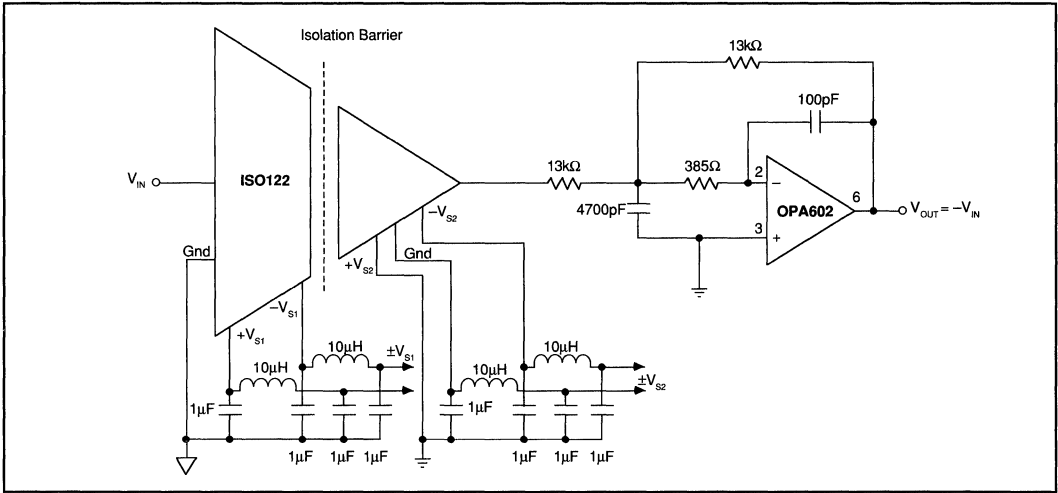


FIGURE 4. Optional π Filter to Minimize Power Supply Feedthrough Noise; Output Filter to Remove 500kHz Carrier Ripple. For more information concerning output filter refer to AB-023.

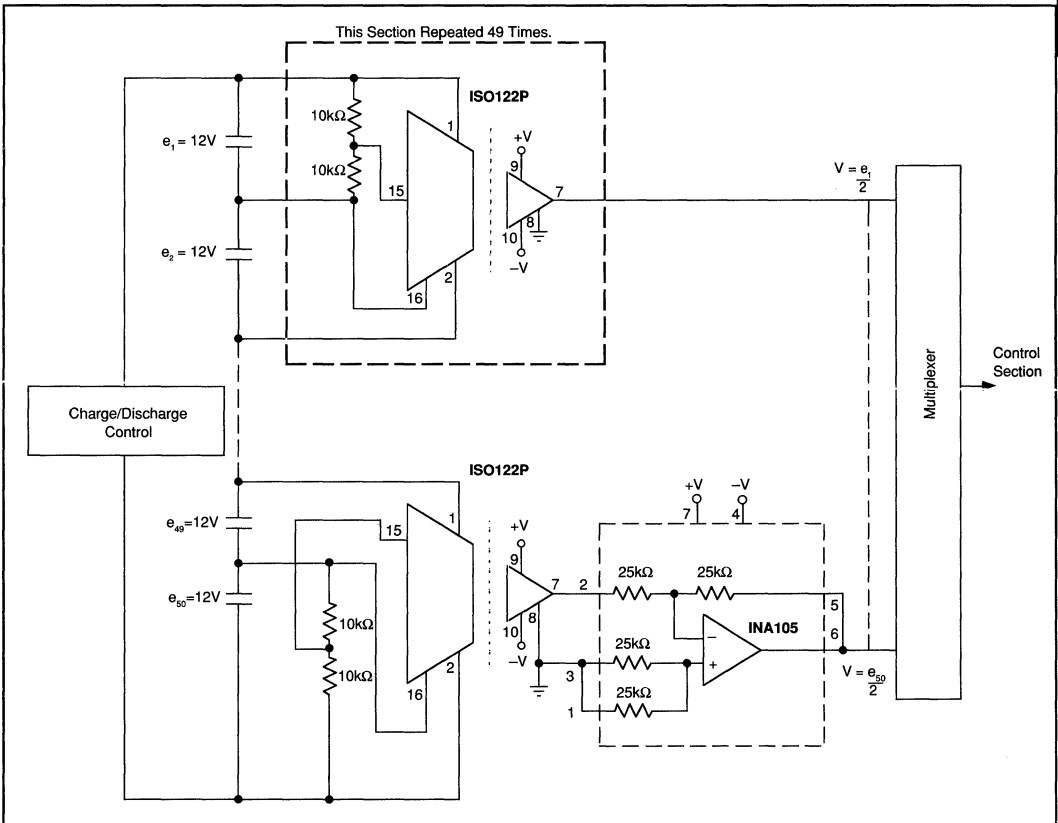


FIGURE 5. Battery Monitor for a 600V Battery Power System. (Derives Input Power from the Battery.)

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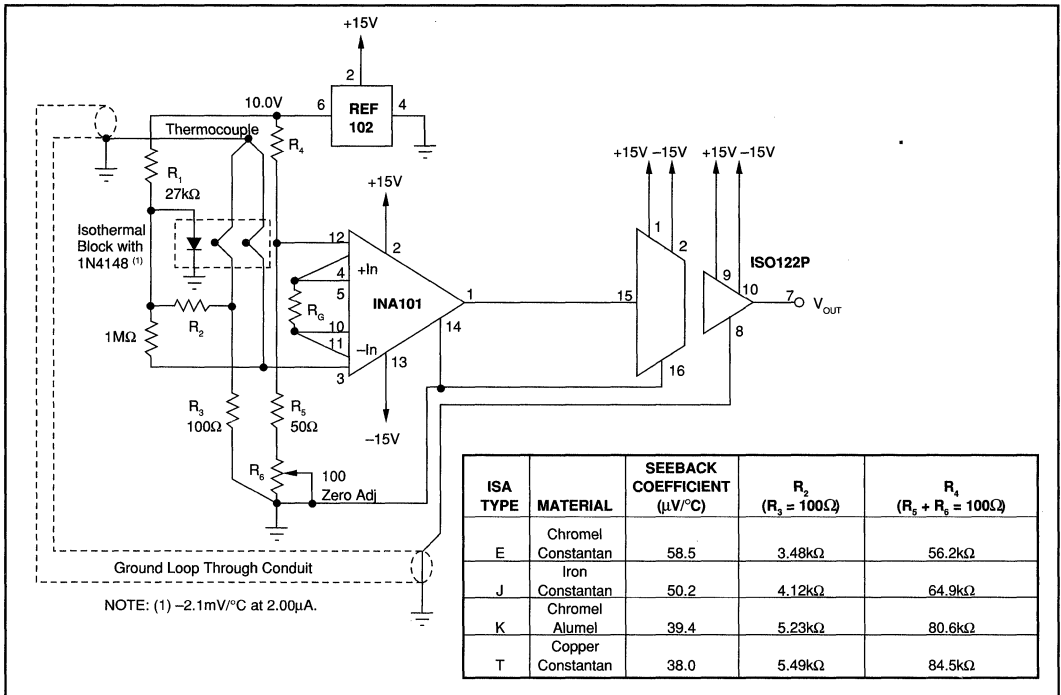


FIGURE 6. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out.

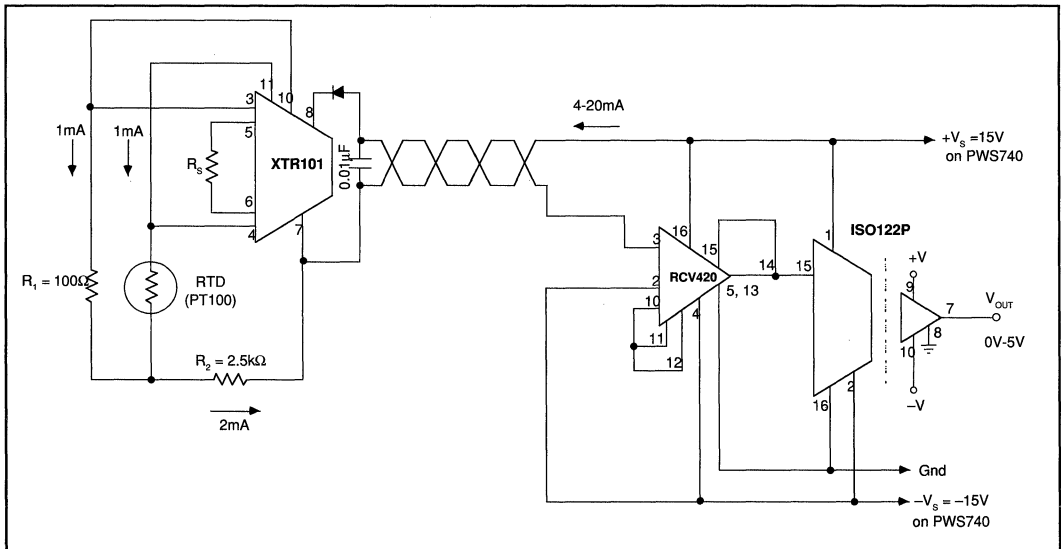


FIGURE 7. Isolated 4-20mA Instrument Loop. (RTD shown.)

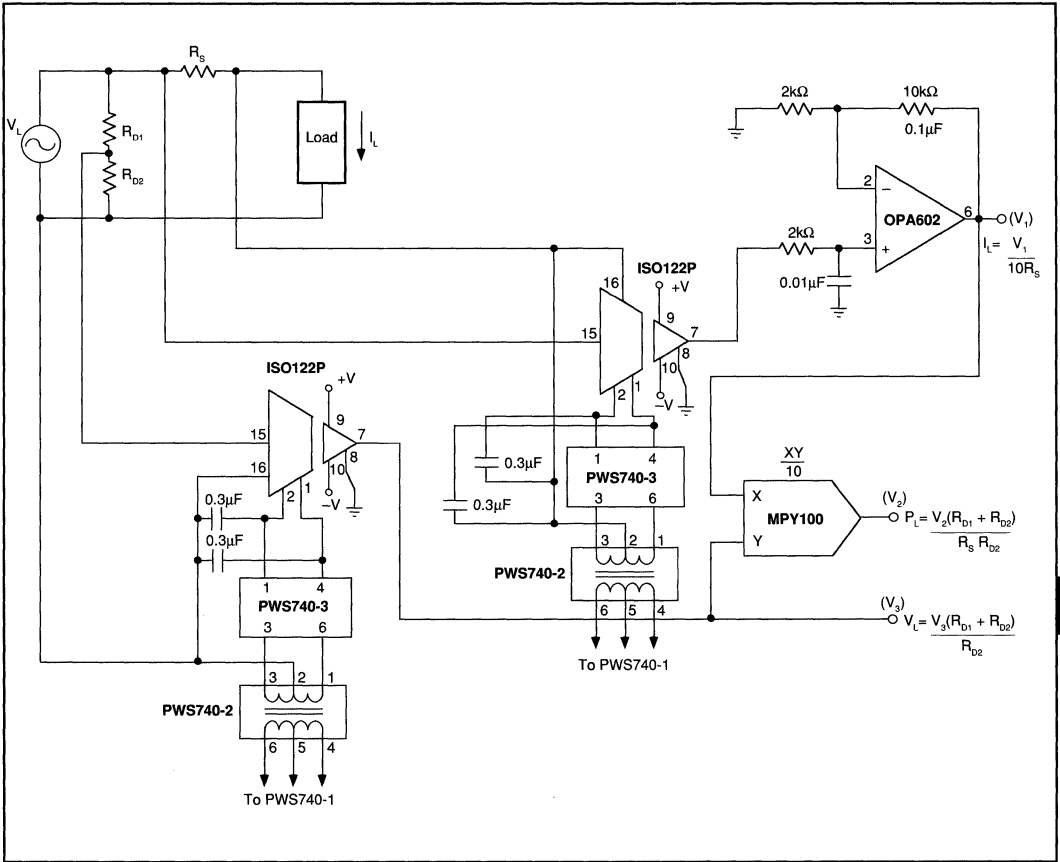


FIGURE 8. Isolated Power Line Monitor.

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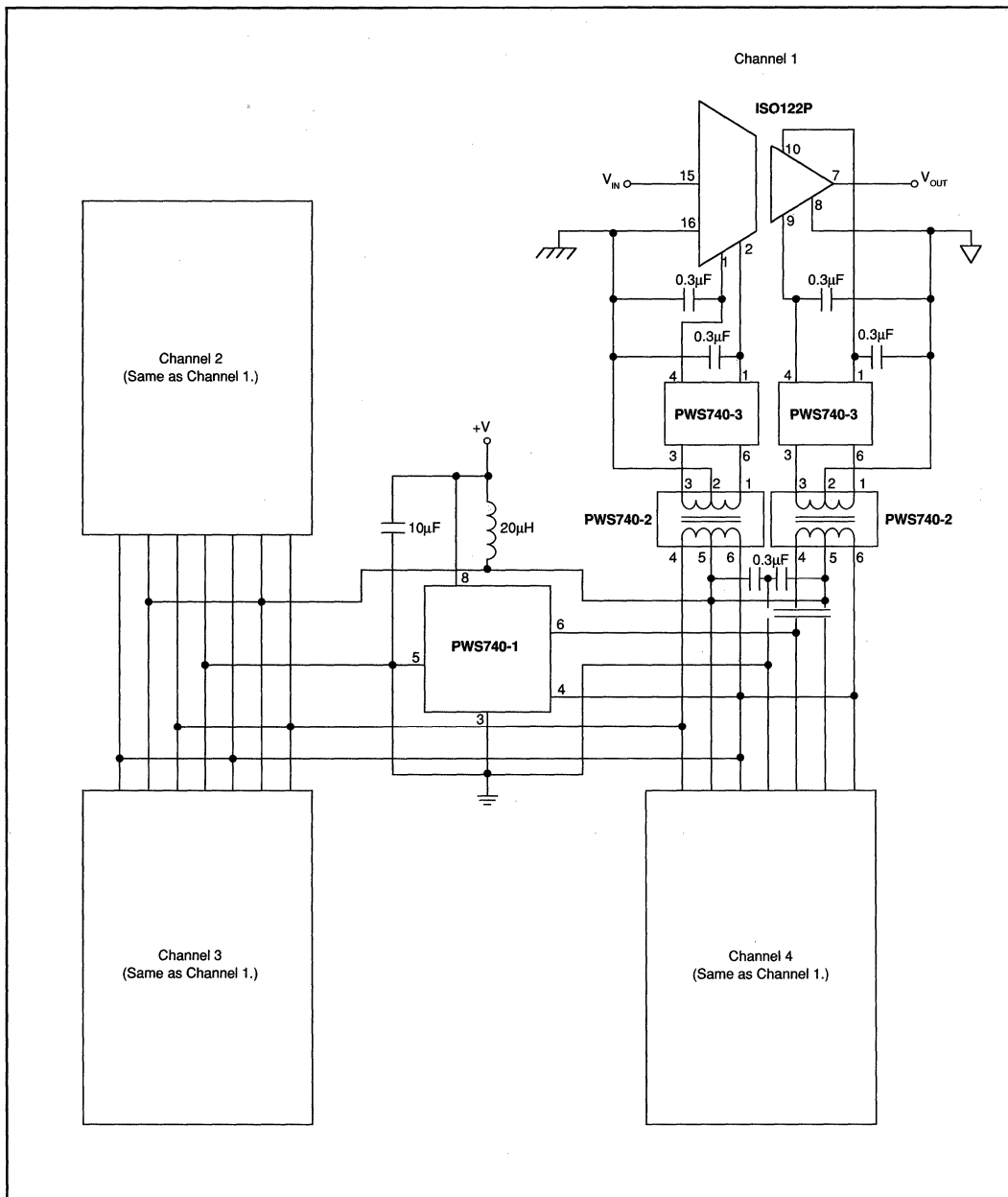


FIGURE 9. Three-Port, Low-Cost, Four-Channel Isolated, Data Acquisition System.

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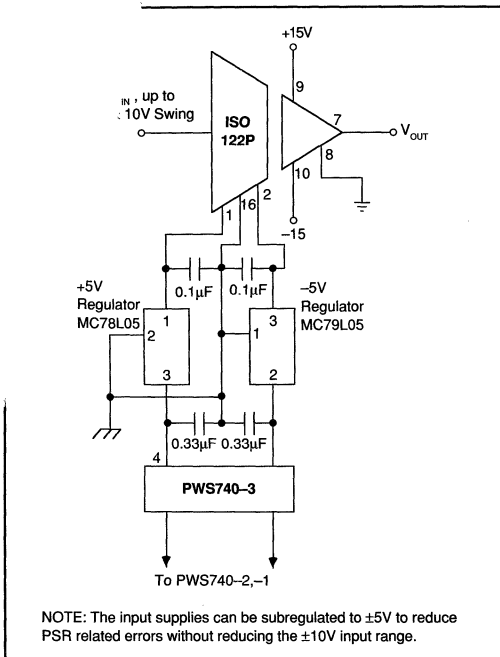


FIGURE 10. Improved PSR Using External Regulator.

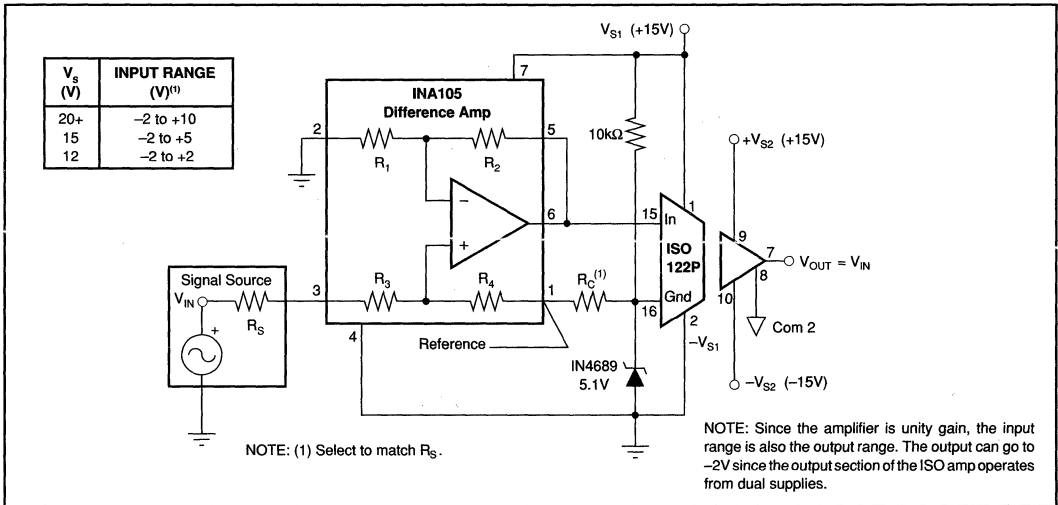


FIGURE 11. Single Supply Operation of the ISO122P Isolation Amplifier. For additional information see AB-009.

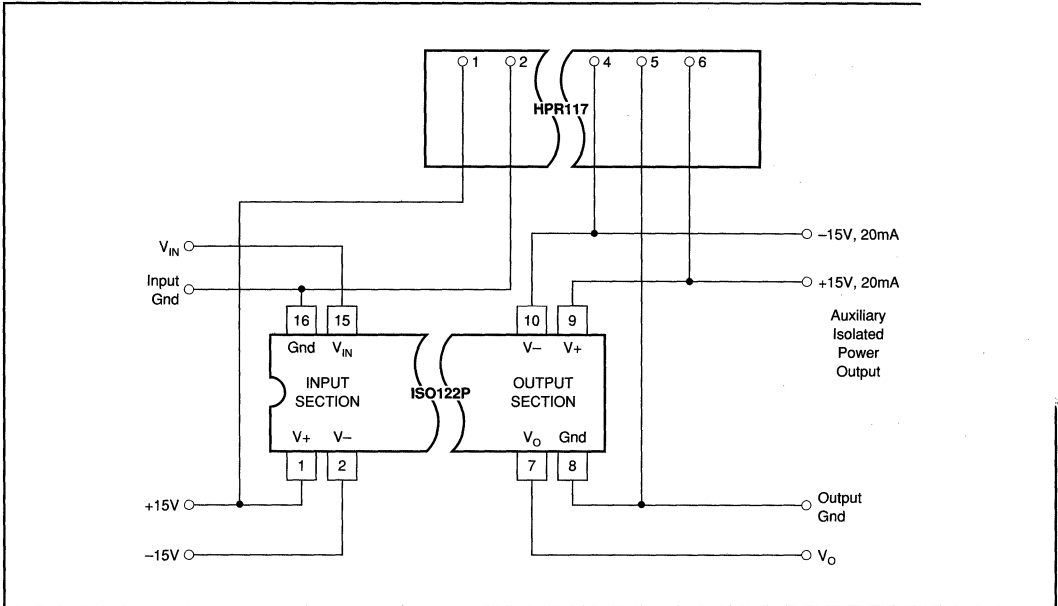


FIGURE 12. Input-Side Powered ISO Amp. For additional information refer to AB-024.

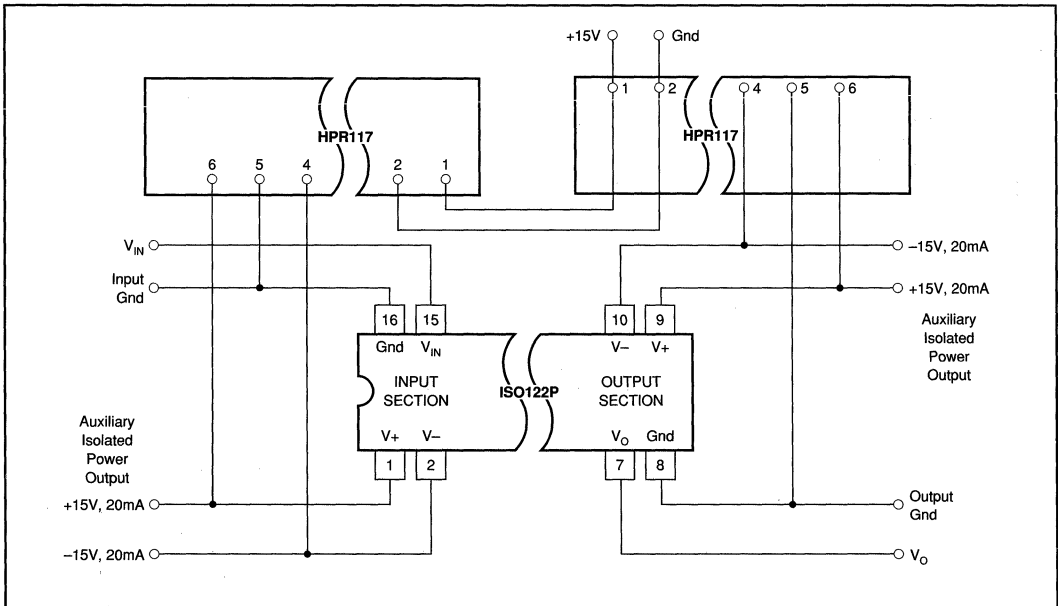
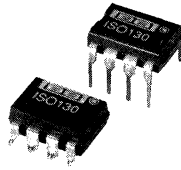


FIGURE 13. Powered ISO Amp with Three-Port Isolation. For additional information refer to AB-024.

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ISO130

High IMR, Low Cost ISOLATION AMPLIFIER

FEATURES

- HIGH ISOLATION-MODE REJECTION: 10kV/ μ s (min)
- LARGE SIGNAL BANDWIDTH: 85kHz (typ)
- DIFFERENTIAL INPUT/DIFFERENTIAL OUTPUT
- VOLTAGE OFFSET DRIFT vs TEMPERATURE: 4.6 μ V/ $^{\circ}$ C (typ)
- OFFSET VOLTAGE 1.8mV (max)
- INPUT REFERRED NOISE: 300 μ Vrms (typ)
- NONLINEARITY: 0.25% (max)
- SINGLE SUPPLY OPERATION
- SIGMA-DELTA A/D CONVERTER TECHNOLOGY
- UL1577, VDE 0884, CSA APPROVAL
- AVAILABLE IN 8-PIN PLASTIC DIP and 8-PIN GULL-WING PLASTIC SURFACE MOUNT

APPLICATIONS

- MOTOR AND SCR CONTROL
- MOTOR PHASE CURRENT SENSING
- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs
- GENERAL PURPOSE ANALOG SIGNAL ISOLATION
- POWER MONITORING
- GROUND LOOP ELIMINATION

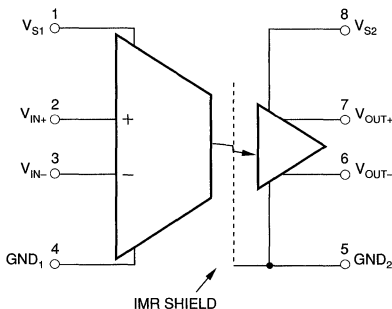
DESCRIPTION

The ISO130 is a high isolation-mode rejection, isolation amplifier suited for motor control applications. Its versatile design provides the precision and stability needed to accurately monitor motor currents in high-noise motor control environments. The ISO130 can also be used for general analog signal isolation applications requiring stability and linearity under severe noise conditions.

The signal is transmitted digitally across the isolation barrier optically, using a high-speed AlGaAs LED. The remainder of the ISO130 is fabricated on 1 μ m CMOS IC process. A sigma-delta analog-to-digital converter, chopper stabilized amplifiers and differential input and output topologies make the isolation amplifier suitable for a variety of applications.

The ISO130 is easy to use. No external components are required for operation. The key specifications are 10kV/ μ s isolation-mode rejection, 85kHz large signal bandwidth, and 4.6 μ V/ $^{\circ}$ C V_{OS} drift. A single power supply ranging from +4.5V to +5.5V makes this amplifier ideal for low power isolation applications.

The ISO130 is available in 8-pin plastic DIP and 8-pin plastic gull-wing surface mount packages.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1234A

5.97

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SPECIFICATIONS

ISOLATION SPECIFICATIONS – VDE0884 INSULATION CHARACTERISTICS

At V_{IN-} , $V_{IN+} = 0V$, $T_A = 25^{\circ}C$, V_{S1} , $V_{S2} = 5.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	ISO130P/ISO130PB ISO130U/ISO130UB	
		CHARACTERISTIC	UNITS
ISOLATION CHARACTERISTICS			
Installation Classification Table I	As Per VDE0109/12.83		
Rated Mains Voltage $\leq 300V_{rms}$		I-IV	
Rated Mains Voltage $\leq 600V_{rms}$		I-III	
Climatic Classification		40/85/21	
Pollution Degree ⁽¹⁾	As Per VDE0109/12.83	2	
Maximum Working Insulation Voltage (V_{IORM})		600	V_{rms}
Side A to Side B Test Voltage, Method b (V_{PR})			
Partial Discharge $< 5pC$	$V_{PR} = 1.6 \times V_{IORM}$, $t_p = 1s$	960	V_{rms}
Side A to Side B Test Voltage, Method a (V_{PR})	Type and Sample Test		
Partial Discharge $< 5pC$	$V_{PR} = 1.2 \times V_{IORM}$, $t_p = 60s$	720	V_{rms}
Highest Allowable Overvoltage (V_{TR})	Transient Overvoltage, $t_{TR} = 10s$	6000	V_{PEAK}
Safety-Limiting Values			
Case Temperature (T_{SI})		175	$^{\circ}C$
Input Power ($P_{SI (INPUT)}$)		80	mW
Output Power ($P_{SI (OUTPUT)}$)		250	mW
INSULATION RELATED SPECIFICATIONS			
Min. External Air Gap (clearance)		> 7	mm
Min. External Tracking Path (creepage)		8	mm
Internal Isolation Gap (clearance)		0.5	mm
Tracking Resistance (CTI)		175	V
Isolation Group	per VDE0109	III a	
Insulation Resistance	$25^{\circ}C$, $V_{ISO} = 500V$	$\geq 10^{11}$	Ω

SPECIFICATIONS

ISOLATION SPECIFICATIONS

At V_{IN+} , $V_{IN-} = 0V$, $T_A = 25^{\circ}C$, V_{S1} , $V_{S2} = 5.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	ISO130P, ISO130PB ISO130U, ISO130UP			UNITS
		MIN	TYP	MAX	
ISOLATION					
Rated Continuous (in accordance with UL1577)		3750			V_{rms}
Voltage Test Breakdown, (in accordance with UL1577)	1s, Leakage Current $< 5\mu A$	4500			V_{rms}
Barrier Impedance					
Resistance	$V_{ISO} = 500VDC$		10^{13}		Ω
Capacitance	$f = 1MHz$		0.7		pF
Isolation Mode Voltage Errors					
Rising Edge Transient Immunity	$V_{IM} = 1kV$, $\partial V_{OUT} < 50mV$	10	25		kV/ μs
Falling Edge Transient Immunity	$V_{IM} = 1kV$, $\partial V_{OUT} < 50mV$	10	15		kV/ μs
Isolation Mode Rejection Ratio ⁽²⁾			> 140		dB

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SPECIFICATIONS

ELECTRICAL

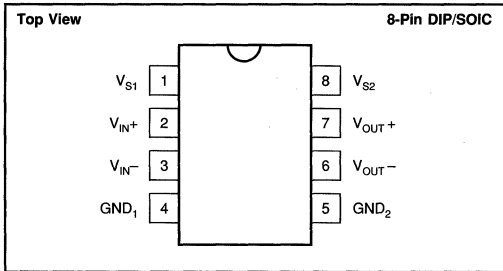
At V_{IN+} , $V_{IN-} = 0V$, $T_A = 25^\circ C$, V_{S1} , $V_{S2} = 5.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	ISO130P/ISO130PB ISO130U/ISO130UB			UNITS		
		MIN	TYP	MAX			
INPUT							
Initial Offset Voltage	1MHz Square Wave, 5ns Rise/Fall Time 0.1Hz to 100kHz	-1.8	-0.9	0.0	mV		
vs Temperature			4.6		$\mu V/^\circ C$		
vs V_{S1}			30		$\mu V/V$		
vs V_{S2}			-40		$\mu V/V$		
Power Supply Rejection; V_{S1} and V_{S2} Together				5	mV/V		
Noise				300	μV_{rms}		
Input Voltage Range			-200		mV		
Maximum Input Voltage Range before Output Clipping				± 300	mV		
Initial Input Bias Current ⁽³⁾				-670	nA		
vs Temperature				3	nA/°C		
Input Resistance ⁽³⁾			530	k Ω			
vs Temperature			0.38	%/°C			
Common-Mode Rejection Ratio ⁽⁴⁾			72	dB			
GAIN⁽⁵⁾							
Initial Gain	$-200mV < V_{IN+} < 200mV$ $-200mV < V_{IN+} < 200mV$	7.61	8.00	8.40	V/V		
ISO130P/ISO130U ISO130PB/ISO130UB			7.85	7.93	8.01	V/V	
Gain vs Temperature			10		ppm/°C		
Gain vs V_{S1}			2.1		ppm/mV		
Gain vs V_{S2}			-0.6		ppm/mV		
Gain Nonlinearity	$-200mV < V_{IN+} < 200mV$ $-100mV < V_{IN+} < 100mV$		0.2	0.35	%		
for $-200mV < V_{IN+} < 200mV$ for $-100mV < V_{IN+} < 100mV$				0.1	0.25	%	
vs Temperature ⁽⁶⁾	$-200mV < V_{IN+} < 200mV$		-0.001		% pts/°C		
vs V_{S1} ⁽⁶⁾	$-200mV < V_{IN+} < 200mV$		-0.005		% pts/V		
vs V_{S2} ⁽⁶⁾	$-200mV < V_{IN+} < 200mV$		-0.007		% pts/V		
OUTPUT							
Voltage Range	$V_{IN+} = +500mV$ $V_{IN+} = -500mV$ $-40^\circ C < T_A < 85^\circ C$, $4.5V < V_{S1} < 5.5V$		3.61		V		
High			1.18		V		
Low			2.39	2.6	V		
Common-Mode Voltage					V		
Current Drive ⁽⁷⁾			1		mA		
Short-Circuit Current	$V_{OUT} = 0V$ or $V_{OUT} = V_{S2}$		9.3		mA		
Output Resistance			11		Ω		
vs Temperature			0.6		%/°C		
FREQUENCY RESPONSE							
Bandwidth	$-40^\circ C$ to $85^\circ C$	50	85		kHz		
-3dB				35		kHz	
-45°			4.3	6.6	μs		
Rise/Fall Time (10% - 90%)	$-40^\circ C$ to $85^\circ C$				μs		
Propagation Delay	$-40^\circ C$ to $85^\circ C$		2.0	3.3	μs		
to 10%				3.4	5.6	μs	
to 50%				6.3	9.9	μs	
to 90%							
POWER SUPPLIES							
Rated Voltage	$V_{IN+} = 200mV$, $-40^\circ C < T_A < 85^\circ C$, $4.5V < V_{S1} < 5.5V$ $-40^\circ C < T_A < 85^\circ C$, $4.5V < V_{S1} < 5.5V$	4.5	5.0	5.5	V		
Voltage Range					V		
Quiescent Current							
V_{S1}					10.7	15.5	mA
V_{S2}					11.6	15.5	mA
TEMPERATURE RANGE							
Specification		-40		85	°C		
Operating		-40		100	°C		
Storage		-55		125	°C		
θ_{CA}			86		°C/W		

NOTES: (1) This part may also be used in Pollution Degree 3 environments where the rated mains voltage is 300Vrms (per DIN VDE0109/12.83). (2) IMRR = $20 \log (\partial V_{IN} / \partial V_{S2})$. (3) Time averaged value. (4) $V_{IN+} = V_{IN-} = V_{CM}$. $CMRR = 20 \log (\partial V_{CM} / \partial V_{OS})$. (5) The slope of the best-fit line of $(V_{OUT+} - V_{OUT-})$ vs $(V_{IN+} - V_{IN-})$. (6) Change in nonlinearity vs temperature or supply voltage expressed in number of percentage points per °C or volt. (7) For best offset voltage performance.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltages: V_{S1} , V_{S2}	0V to 5.5V
Steady-State Input Voltage	-2V to $V_{S1} + 0.5V$
2 Second Transient Input Voltage	-6.0V
Output Voltages: V_{OUT+} , V_{OUT-}	-0.5V to $V_{S2} + 0.5V$
Lead Temperature Solder (1.6mm below seating plane, 10s)	260°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO130P	8-Pin Plastic DIP	006-3
ISO130PB	8-Pin Plastic DIP	006-3
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	006-2
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	006-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

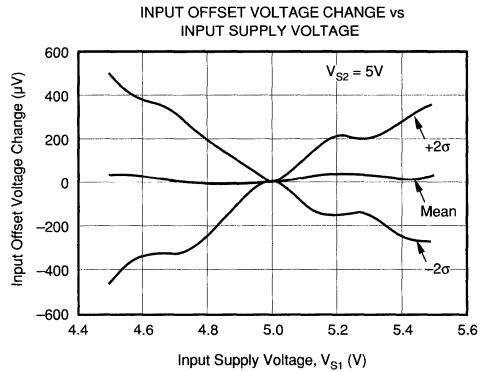
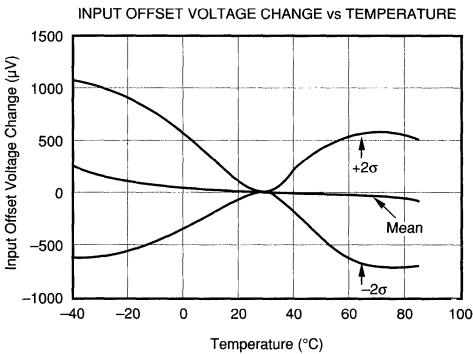
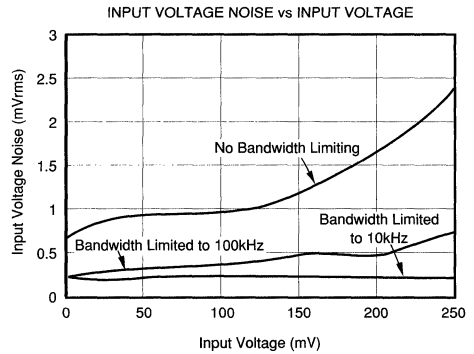
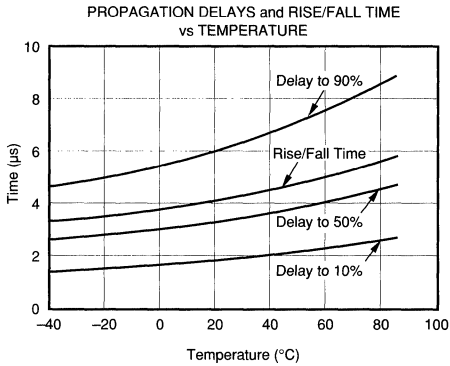
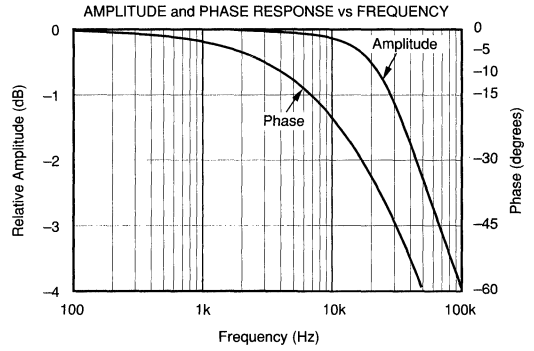
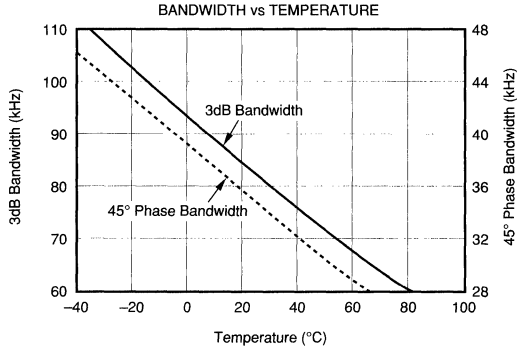
MODEL	PACKAGE	GAIN ERROR (MAX)
ISO130P	8-Pin Plastic DIP	±5% (mean value = 8.00)
ISO130PB	8-Pin Plastic DIP	±1% (mean value = 7.93)
ISO130U	8-Pin Gull-Wing Plastic Surface Mount	±5% (mean value = 8.00)
ISO130UB	8-Pin Gull-Wing Plastic Surface Mount	±1% (mean value = 7.93)

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TYPICAL PERFORMANCE CURVES

At $T_A = 25^\circ\text{C}$, $V_{S1} = V_{S2} = 5.0\text{V}_{\text{DC}}$, $V_{IN+} = V_{IN-} = 0\text{V}$, unless otherwise noted.



ISO130

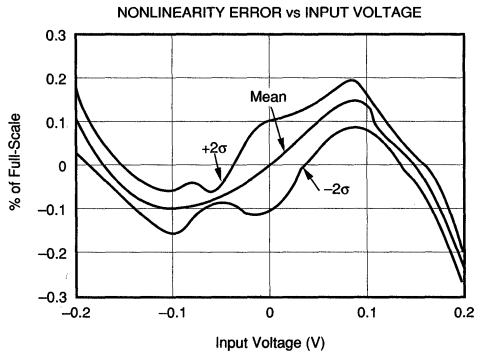
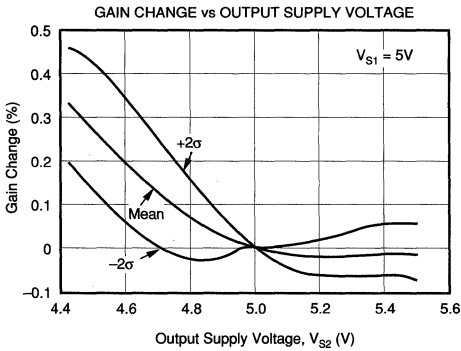
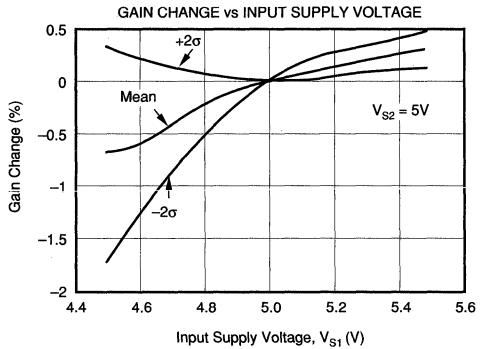
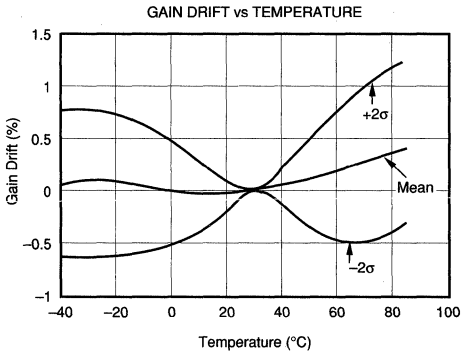
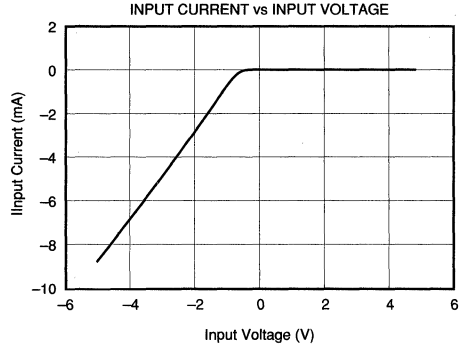
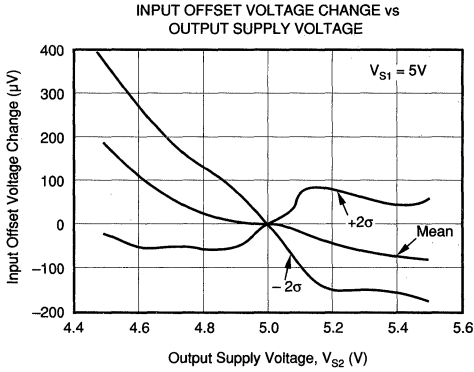
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ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES (CONT)

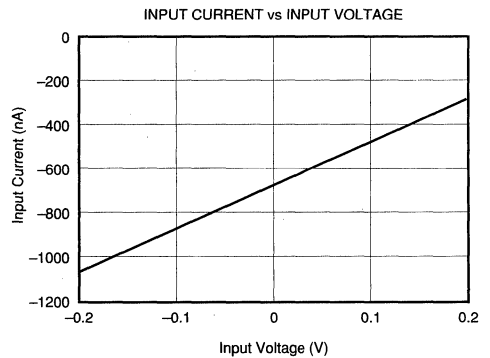
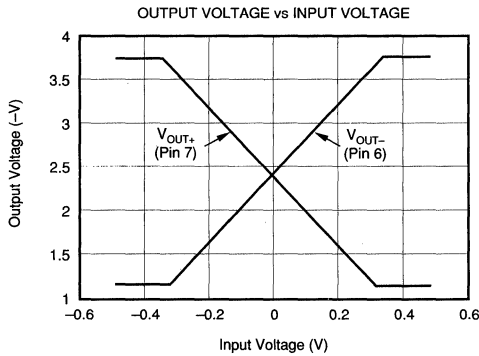
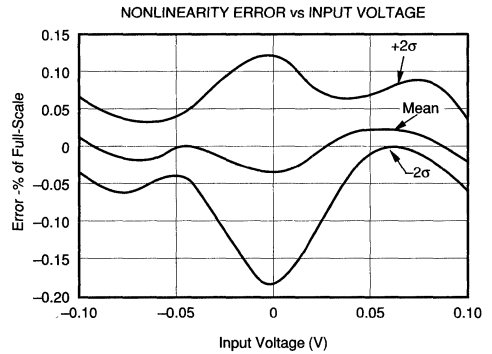
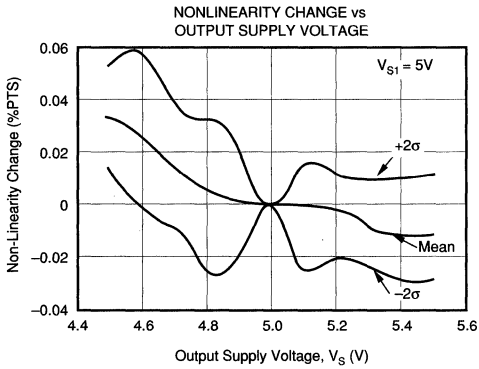
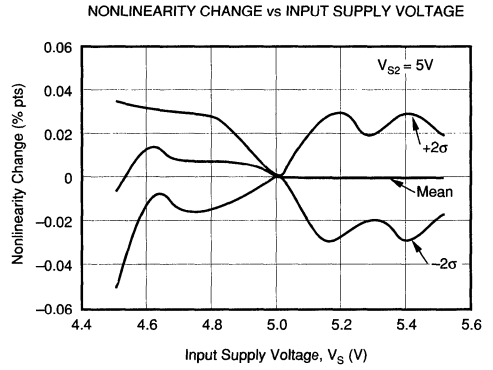
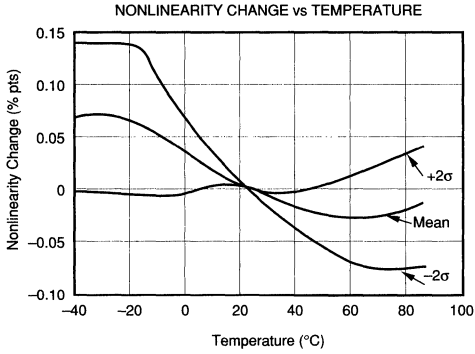
At $T_A = 25^\circ\text{C}$, V_{S1} , $V_{S2} = 5.0\text{V}_{\text{DC}}$, V_{IN+} , $V_{IN-} = 0\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

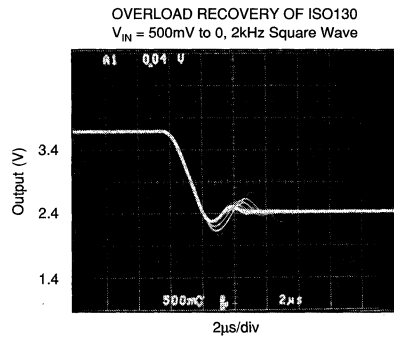
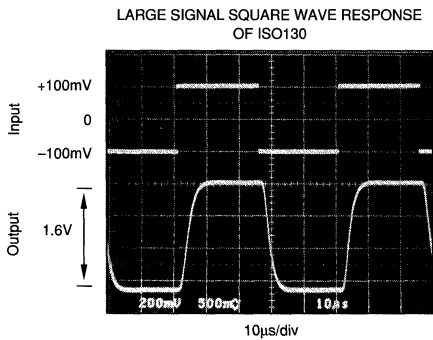
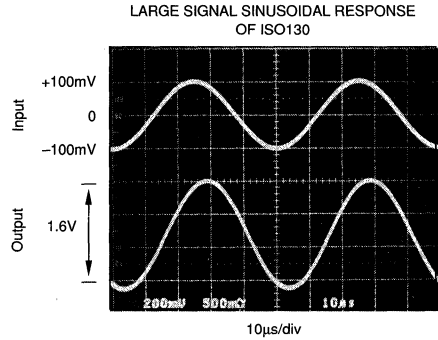
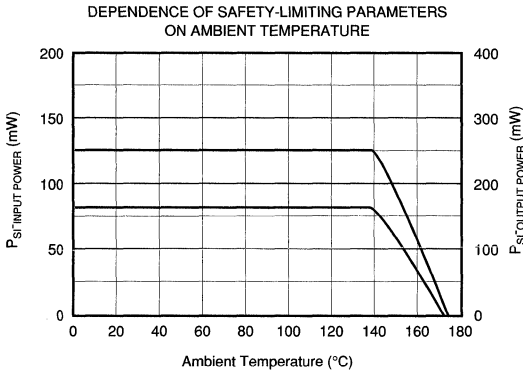
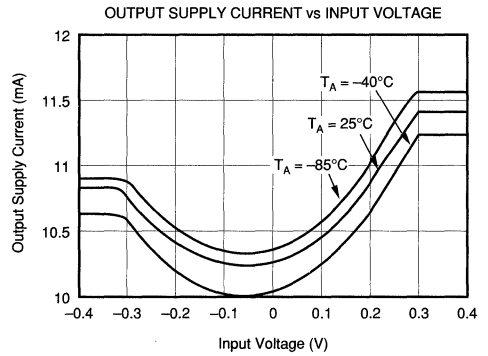
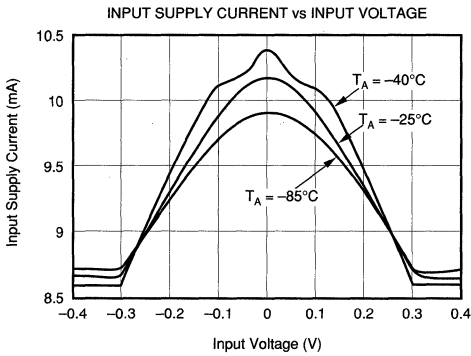
At $T_A = 25^\circ\text{C}$, $V_{S1}, V_{S2} = 5.0\text{V}_{\text{DC}}$, $V_{IN+}, V_{IN-} = 0\text{V}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES, (CONT)

At $T_A = 25^\circ\text{C}$, $V_{S1}, V_{S2} = 5.0\text{V}_{\text{DC}}$, $V_{IN+}, V_{IN-} = 0\text{V}$, unless otherwise noted.



THEORY OF OPERATION

The ISO130 isolation amplifier (Figure 1) uses an input and output section galvanically isolated by a high speed optical barrier built into the plastic package. The input signal is converted to a time averaged serial bit stream by use of a sigma-delta analog-to-digital converter and then optically transmitted digitally across the isolation barrier. The output section receives the digital signal and converts it to an analog voltage, which is then filtered to produce the final output signal.

Internal amplifiers are chopper-stabilized to help maintain device accuracy over time and temperature. The encoder circuit eliminates the effects of pulse-width distortion of the optically transmitted data by generating one pulse for every edge of the converter data to be transmitted. This coding scheme reduces the effects of the non-ideal characteristics of the LED, such as non-linearity and drift over time and temperature.

ISOLATION SPECIFICATIONS

The performance of the isolation barrier of the ISO130 is specified with three specifications, two of which require high voltage testing. The ISO130 is designed to reliably operate with 3750Vrms continuous isolation barrier voltage

(in accordance with UL1577). To confirm the barrier integrity, each isolation amplifier is proof-tested by applying an isolation test voltage greater than or equal to 4500Vrms for one second. The barrier leakage current test limit is 5 μ A.

This test is followed by the partial discharge isolation voltage test as specified in the German VDE0884. This method requires the measurement of small current pulses (<5pico Colomb) while applying 960Vrms across every ISO130 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage (1.6 X 600Vrms) protection without damage to the ISO130.

This test method represents "state of the art" for non-destructive high voltage reliability testing. It is based on the effects of non-uniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01 to 0.1 μ s current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage".

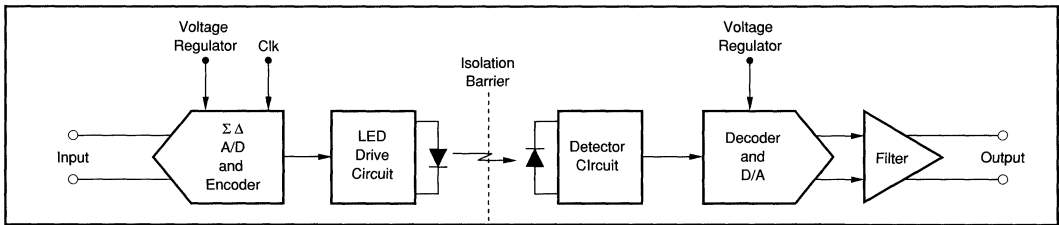


FIGURE 1. Block Diagram of ISO130 Isolation Amplifier.

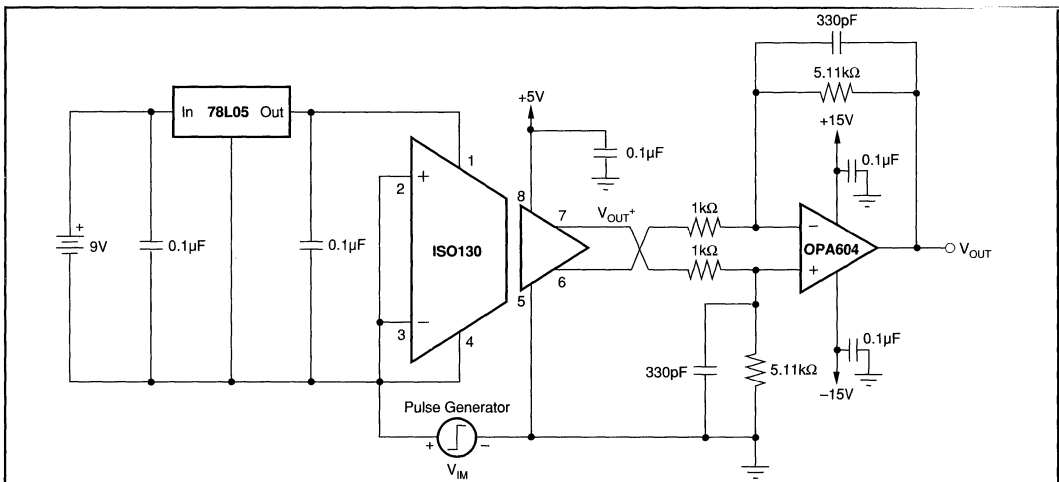


FIGURE 2. Isolation Mode Rejection and Transient Immunity Test Circuit.

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Both tests are 100% production tests. The partial discharge testing of the ISO130 is performed after the UL1577 test criterion giving more confidence in the barrier reliability.

The third guaranteed isolation specification for the ISO130 is Transient Immunity (TI), which specifies the minimum rate of rise or fall of an isolation mode noise signal at which small output perturbations begin to occur. An isolation mode signal is defined as a signal appearing between the isolated grounds, GND_1 and GND_2 . Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds. Under certain circumstances this voltage across the isolation barrier can induce errors at the output of the isolation amplifier. Figure 2 shows the Transient Immunity Test Circuit for the ISO130. In this test circuit a pulse generator is placed between the isolated grounds (GND_1 and GND_2). The inputs of the ISO130 are both tied to GND_1 . A difference amplifier is used to gain

the output signal of the ISO130. A Transient Immunity failure is determined when the output of the ISO130 changes by more than 50mV as illustrated in Figure 3.

Finally, Isolation Mode Rejection Ratio (typically >140dB for the ISO130) is defined as the ratio of differential signal gain to the isolation mode gain at 60 Hz. The magnitude of the 60Hz voltage across the isolation barrier during this test is not so large as to cause Transient Immunity errors. The Isolation Mode Rejection Ratio should not be confused with the Common Mode Rejection Ratio. The Common Mode Rejection Ratio defines the relationship of differential signal gain (signal applied differentially between pins 2 and 3) to the common mode gain (input pins tied together and the signal applied to both inputs at the same time).

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Figure 4 illustrates a typical application for the ISO130. In this motor control circuit, the current that is sent to the motor is sensed by the resistor, R_{SENSE} . The voltage drop across this resistor is gained up by the ISO130 and then transmitted across the isolation barrier. A difference amplifier, A_2 , is used to change the differential output signal of the ISO130 to a single ended signal. This voltage information is then sent to the control circuitry of the motor. The ISO130 is particularly well suited for this application because of its superior Transient Immunity (10kV/ μ s, max) and its excellent immunity to RF noise.

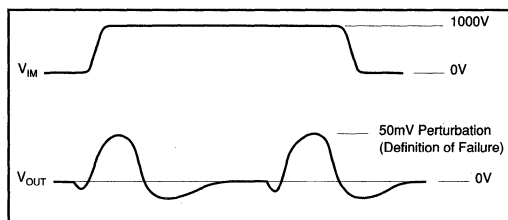


FIGURE 3. Typical Transient Immunity Failure Waveform.

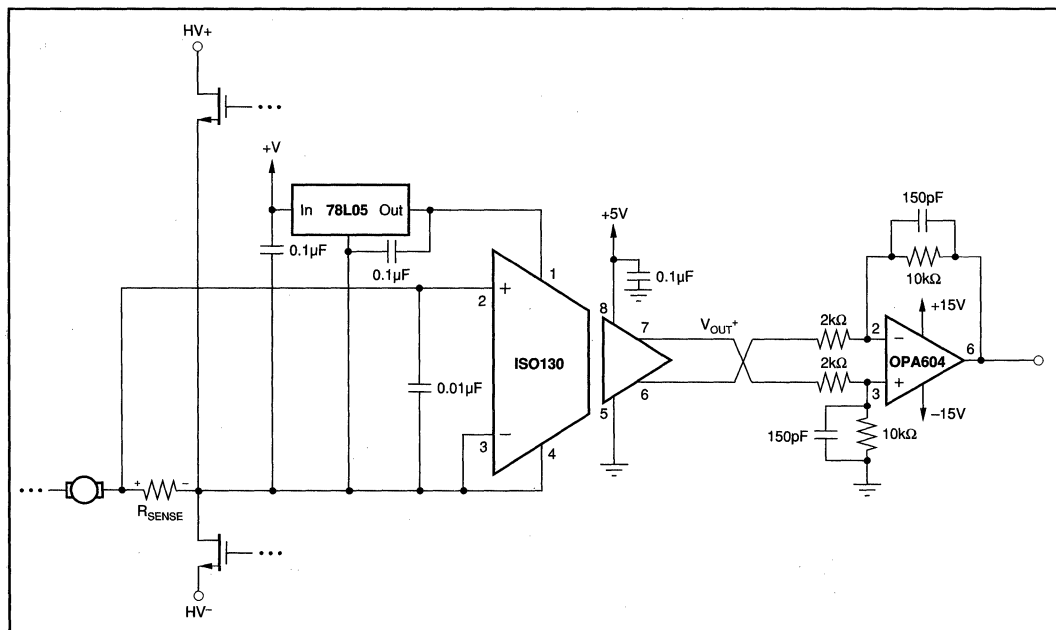


FIGURE 4. ISO130 Used to Monitor Motor Current.

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The current-sensing resistor should have a relatively low value of resistance (to minimize power dissipation), a fairly low inductance (to accurately reflect high-frequency signal components), and a reasonably tight tolerance (to maintain overall circuit accuracy).

LAYOUT SUGGESTIONS

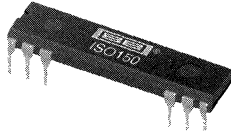
1. By-pass capacitors should be located as close as possible to the input and output power supply pins.
2. In some applications, offset voltage can be reduced by placing a 0.01 μ F capacitor from pin 2 and/or pin 3 to GND_I. This noise can be caused by the combination of long input leads and the switched-capacitor nature of the input circuit. This capacitor(s) should be placed as close to the isolation amplifier as possible.
3. The trace lengths at input should be kept short or a twisted wire pair should be used to minimize EMI and inductance effects. For optimum performance, the input signal should be as close to the input pins as possible.
4. A maximum distance between the input and output sides of the isolation amplifier should be maintained in the layout in order to minimize stray capacitance. This practice will help obtain optimal Isolation Mode performance. Ground planes should not pass below the device on the PCB.
5. Care should be taken in selecting isolated power supplies or regulators. The ISO130 can be affected by changes in the power supply voltages. Carefully regulated power supplies are recommended.
6. For improved non-linearity and non-linearity temperature drift performance, pin 3 should be tied to GND_I and the input voltage range of pin 2 should be less than 100mV.

ISO130

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ISOLATION PRODUCTS

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ISO150

Dual, Isolated, Bi-Directional DIGITAL COUPLER

FEATURES

- REPLACES HIGH-PERFORMANCE OPTOCOUPLERS
- DATA RATE: 80M Baud, typ
- LOW POWER CONSUMPTION: 25mW Per Channel, max
- TWO CHANNELS, EACH BI-DIRECTIONAL, PROGRAMMABLE BY USER
- PARTIAL DISCHARGE TESTED: 2400Vrms
- CREEPAGE DISTANCE OF 16.5mm (DIP)
- LOW COST PER CHANNEL
- PLASTIC DIP AND SOIC PACKAGES

APPLICATIONS

- DIGITAL ISOLATION FOR A/D, D/A CONVERSION
- ISOLATED UART INTERFACE
- MULTIPLEXED DATA TRANSMISSION
- ISOLATED PARALLEL TO SERIAL INTERFACE
- TEST EQUIPMENT
- MICROPROCESSOR SYSTEM INTERFACE
- ISOLATED LINE RECEIVER
- GROUND LOOP ELIMINATION

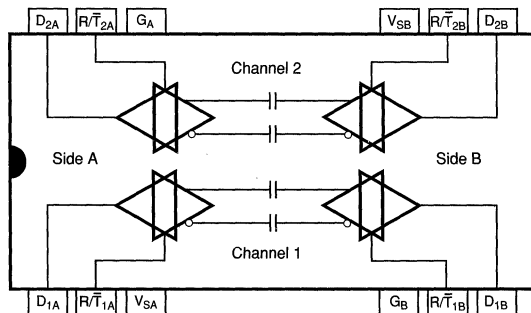
DESCRIPTION

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80MBaud, typical. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high voltage 0.4pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6kV/ μ s.

ISO150 avoids the problems commonly associated with optocouplers. Optically isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25mW per channel.

ISO150 is available in a 24-pin DIP package and in a 28-lead SOIC. Both are specified for operation from -40°C to 85°C .



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

T_A = +25°C, V_S = +5V unless otherwise noted.

PARAMETER	CONDITION	ISO150AP, AU			UNITS
		MIN	TYP	MAX	
ISOLATION PARAMETERS					
Rated Voltage, Continuous	60Hz	1500			V _{rms}
Partial Discharge, 100% Test ⁽¹⁾	1s, 5pC	2400			V _{rms}
Creepage Distance (External)					
DIP—"P" Package			16		mm
SOIC—"U" Package			7.2		mm
Internal Isolation Distance			0.10		mm
Isolation Voltage Transient Immunity ⁽²⁾			1.6		kV/μs
Barrier Impedance			>10 ¹⁴ 7		Ω pF
Leakage Current	240V _{rms} , 60Hz		0.6		μArms
DC PARAMETERS					
Logic Output Voltage, High, V _{OH}	I _{OH} = 6mA	V _S -1		V _S	V
Low, V _{OL}	I _{OL} = 6mA	0		0.4	V
Logic Output Short-Circuit Current	Source or Sink		30		mA
Logic Input Voltage, High ⁽³⁾		2		V _S	V
Low ⁽³⁾		0		0.8	V
Logic Input Capacitance			5		pF
Logic Input Current			<1		nA
Power Supply Voltage Range ⁽³⁾		3	5	5.5	V
Power Supply Current ⁽⁴⁾					
Transmit Mode	DC		0.001	100	μA
50MBaud			14		mA
DC			7.2	10	mA
Receive Mode	50MBaud		16		mA
AC PARAMETERS					
Data Rate, Maximum ⁽⁵⁾	C _L = 50pF	50	80		MBaud
Data Rate, Minimum		DC			
Propagation Time ⁽⁶⁾	C _L = 50pF	20	27	40	ns
Propagation Delay Skew ⁽⁷⁾	C _L = 50pF		0.5	2	ns
Pulse Width Distortion ⁽⁸⁾	C _L = 50pF		1.5	6	ns
Output Rise/Fall Time, 10% to 90%	C _L = 50pF		9	14	ns
Mode Switching Time					
Receive-to-Transmit			13		ns
Transmit-to-Receive			75		ns
TEMPERATURE RANGE					
Operating Range		-40		85	°C
Storage		-40		125	°C
Thermal Resistance, θ _{JA}			75		°C/W

NOTES: (1) All devices receive a 1s test. Failure criterion is ≥5 pulses of ≥5pC. (2) The voltage rate-of-change across the isolation barrier that can be sustained without data errors. (3) Logic inputs are HCT-type and thresholds are a function of power supply voltage with approximately 0.4V hysteresis—see text. (4) Supply current measured with both transceivers set for the indicated mode. Supply current varies with data rate—see typical curves. (5) Calculated from the maximum Pulse Width Distortion (PWD), where Data Rate = 0.3/PWD. (6) Propagation time measured from V_{IN} = 1.5V to V_O = 2.5V. (7) The difference in propagation time of channel A and channel B in any combination of transmission directions. (8) The difference between propagation time of a rising edge and a falling edge.

ISO150
5
ISOLATION PRODUCTS

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ABSOLUTE MAXIMUM RATINGS

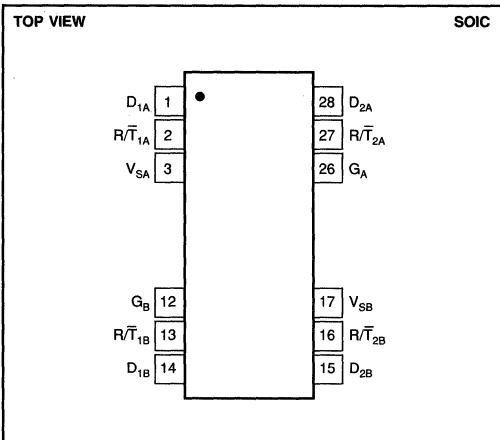
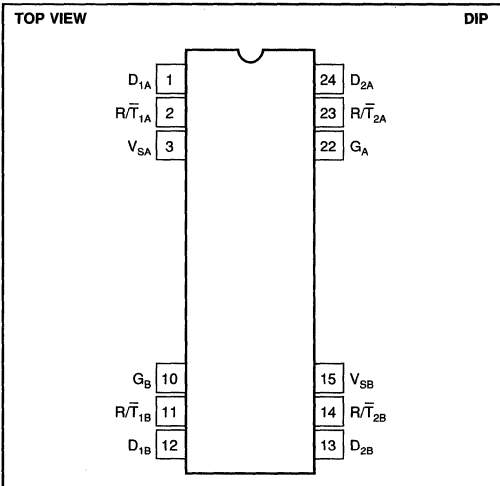
Storage Temperature	-40°C to +125°C
Supply Voltages, V_S	-0.5 to 6V
Transmitter Input Voltage, V_i	-0.5 to $V_S + 0.5V$
Receiver Output Voltage, V_o	-0.5 to $V_S + 0.5V$
R/\bar{T}_x Inputs	-0.5 to $V_S + 0.5V$
Isolation Voltage dV/dt, V_{SO}	500kV/ μ s
D_x Short to Ground	Continuous
Junction Temperature, T_j	175°C
Lead Temperature (soldering, 10s)	260°C
1.6mm below seating plane (DIP package)	300°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO150AP	24-Pin Single-Wide DIP	243-1
ISO150AU	28-Lead SOIC	217-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



PIN DESCRIPTIONS

NAME	FUNCTION
D_{1A}	Data in or data out for transceiver 1A. R/\bar{T}_{1A} held low makes D_{1A} an input pin.
R/\bar{T}_{1A}	Receive/Transmit switch controlling transceiver 1A.
V_{SA}	+5V supply pin for side A which powers transceivers 1A and 2A.
G_B	Ground pin for transceivers 1B and 2B.
R/\bar{T}_{1B}	Receive/Transmit switch controlling transceiver 1B.
D_{1B}	Data in or data out for transceiver 1B. R/\bar{T}_{1B} held low makes D_{1B} an input pin.
D_{2B}	Data in or data out for transceiver 2B. R/\bar{T}_{2B} held low makes D_{2B} an input pin.
R/\bar{T}_{2B}	Receive/Transmit switch controlling D_{2B} .
V_{SB}	+5V supply pin for side B which powers transceivers 1B and 2B.
G_A	Ground pin for transceivers 1A and 2A.
R/\bar{T}_{2A}	Receive/Transmit switch controlling transceiver 2A.
D_{2A}	Data in or data out for transceiver 2A. R/\bar{T}_{2A} held low makes D_{2A} an input pin.



ELECTROSTATIC DISCHARGE SENSITIVITY

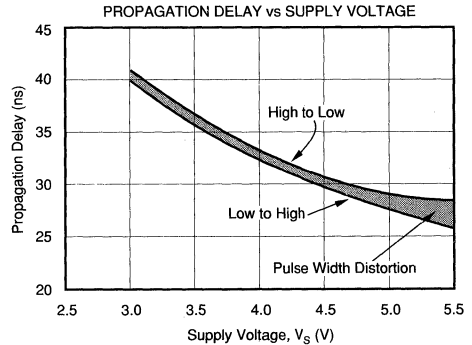
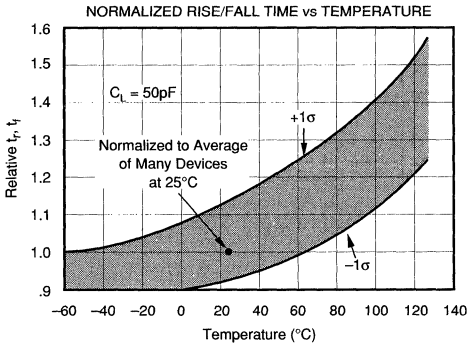
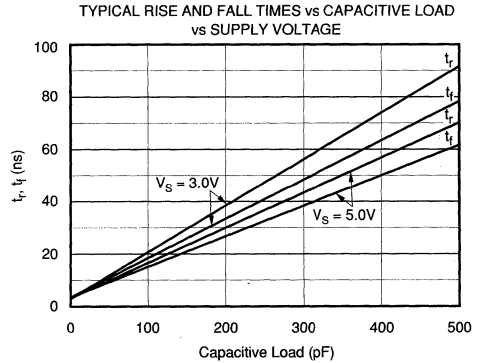
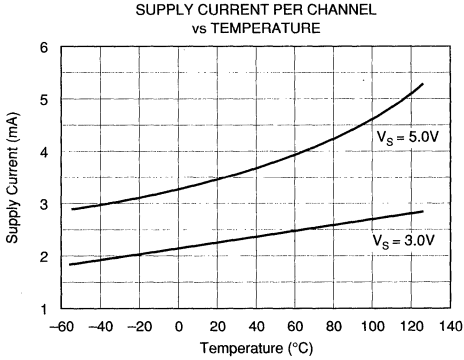
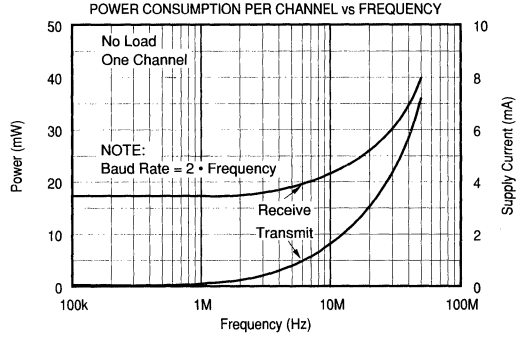
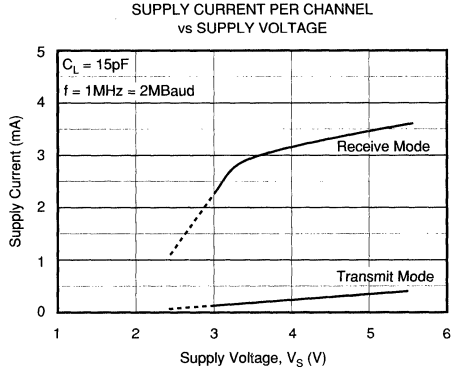
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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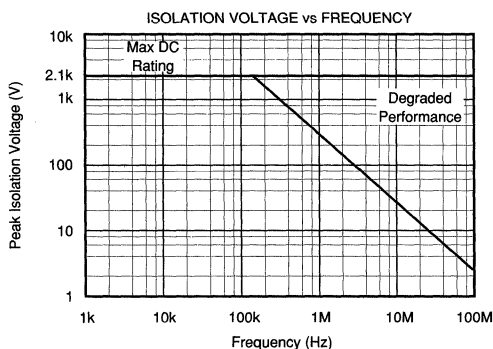
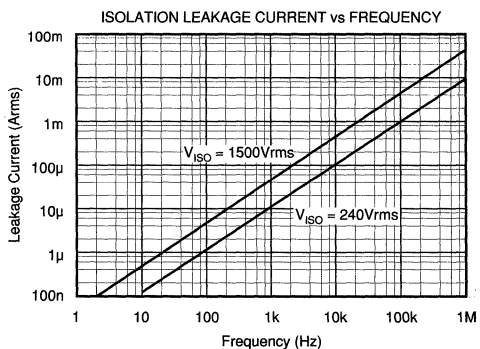
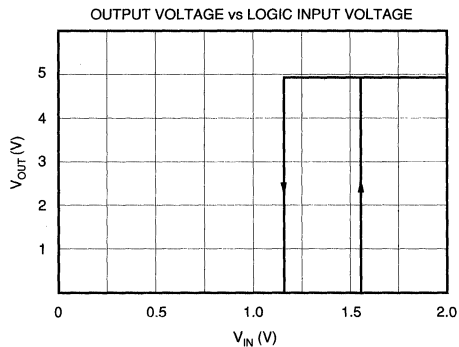
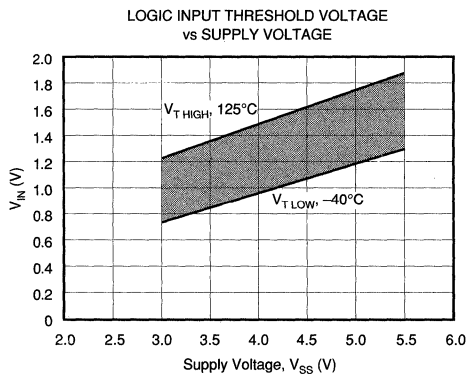
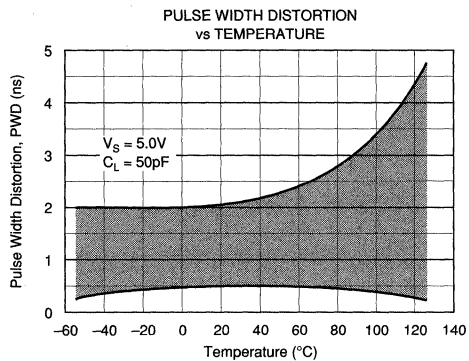
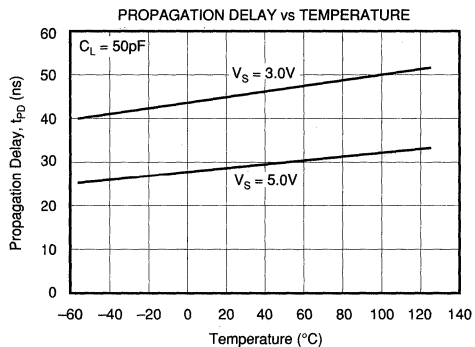
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$ unless otherwise noted.



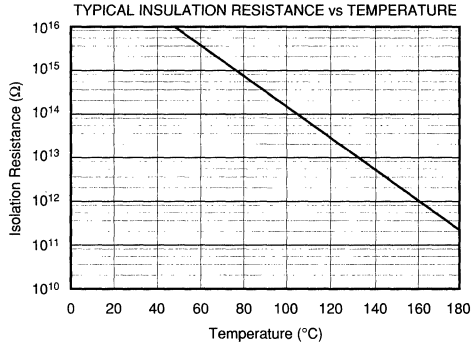
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$ unless otherwise noted.



ISOLATION BARRIER

Data is transmitted by coupling complementary logic pulses to the receiver through two 0.4pF capacitors. These capacitors are built into the ISO150 package with Faraday shielding to guard against false triggering by external electrostatic fields.

The integrity of the isolation barrier of the ISO150 is verified by partial discharge testing. 2400Vrms, 60Hz, is applied across the barrier for one second while measuring any tiny discharge currents that may flow through the barrier. These current pulses are produced by localized ionization within the barrier. This is the most sensitive and reliable indicator of barrier integrity and longevity, and does not damage the barrier. A device fails the test if five or more current pulses of 5pC or greater are detected.

Conventional isolation barrier testing applies test voltage far in excess of the rated voltage to catastrophically break down a marginal device. A device that passes the test may be weakened, and lead to premature failure.

APPLICATIONS INFORMATION

Figure 1 shows the ISO150 connected for basic operation. Channel 1 is configured to transmit data from side B to A. Channel 2 is set for transmission from side A to B. The R/T pins for each of the four transceivers are shown connected to the required logic level for the transmission direction shown. The transmission direction can be controlled by logic signals applied to the R/T pins. Channel 1 and 2 can be independently controlled for the desired transmission direction.

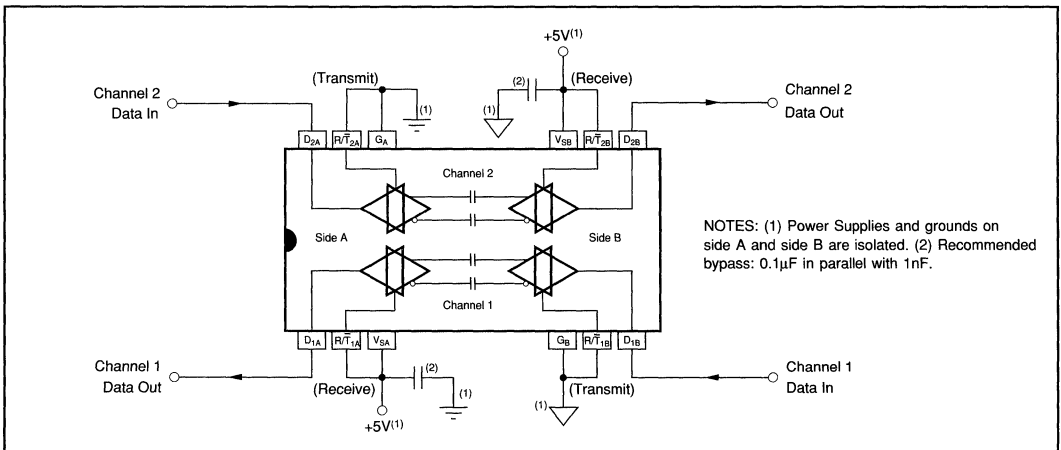


FIGURE 1. Basic Operation Diagram.

LOGIC LEVELS

A single pin serves as a data input or output, depending on the mode selected. Logic inputs are CMOS with thresholds set for TTL compatibility. The logic threshold is approximately 1.3V with 5V supplies and with approximately 400mV of hysteresis. Input logic thresholds vary with the power supply voltage. Drive the logic inputs with signals that swing the full logic voltage swing. The ISO150 will use somewhat greater quiescent current if logic inputs do not swing within 0.5V of the power supply rails.

In receive mode, the data output can drive 15 standard LS-TTL loads. It will also drive CMOS loads. The output drive circuits are CMOS.

POWER SUPPLY

Separate, isolated power supplies must be connected to side A and side B to provide galvanic isolation. Nominal rated supply voltage is 5V. Operation extends from 3V to 5.5V. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier.

The V_S pin for each side powers the transceivers for both channel 1 and 2. The specified supply current is the total of both transceivers on one side, both operating in the indicated mode. Supply current for one transceiver in transmit mode and one in receive mode can be estimated by averaging the specifications for transmit and receive operation. Supply current varies with the data transmission rate—see typical curves.

POWER-UP STATE

The ISO150 transmits information across the barrier only when the input-side data changes logic state. When a transceiver is first programmed for receive mode, or is powered-up in receive mode, its output is initialized “high”. Subsequent changes of data applied to the input side will cause the output to properly reflect the input side data.

SIGNAL LOSS

The ISO150's differential-mode signal transmission and careful receiver design make it highly immune to voltage across the isolation barrier (isolation-mode voltage). Rapidly changing isolation-mode voltage can cause data errors. As the rate of change of isolation voltage is increased, there is a very sudden increase in data errors. Approximately 50% of ISO150s will begin to produce data errors with isolation-mode transients of 1.6kV/ μ s. This may occur as low as 500V/ μ s in some devices. In comparison, a 1000Vrms, 60Hz isolation-mode voltage has a rate of change of approximately 0.5V/ μ s.

Still, some applications with large, noisy isolation-mode voltage can produce data errors by causing the receiver output to change states. After a data error, subsequent changes in input data will produce correct output data.

PROPAGATION DELAY AND SKEW

Logic transitions are delayed approximately 27ns through the ISO150. Some applications are sensitive to data skew—the difference in propagation delay between channel 1 and channel 2. Skew is less than 2ns between channel 1 and channel 2. Applications using more than one ISO150 must allow for somewhat greater skew from device to device. Since all devices are tested for delay times of 20ns min to 40ns max, 20ns is the largest device-to-device data skew.

MODE CHANGES

The transmission direction of a channel can be changed “on the fly” by reversing the logic levels at the channel's R/T pins on both side A and side B. Approximately 75ns after the transceiver is programmed to receive mode its output is initialized “high”, and will respond to subsequent input-side changes in data.

STANDBY MODE

Quiescent current of each transceiver circuit is very low in transmit mode when input data is not changing (1nA typical). To conserve power when data transmission is not required, program both side A and B transceivers for transmit mode. Input data applied to either transceiver is ignored by the other side. High speed data applied to either transceiver will increase quiescent current.

CIRCUIT LAYOUT

The high speed of the ISO150 and its isolation barrier require careful circuit layout. Use good high speed logic layout techniques for the input and output data lines. Power supplies should be bypassed close to the device pins on both sides of the isolation barrier. Use low inductance connections. Ground planes are recommended.

Maintain spacing between side 1 and side 2 circuitry equal or greater than the spacing between the missing pins of the ISO150 (approximately 16mm for the DIP version). Sockets are not recommended.

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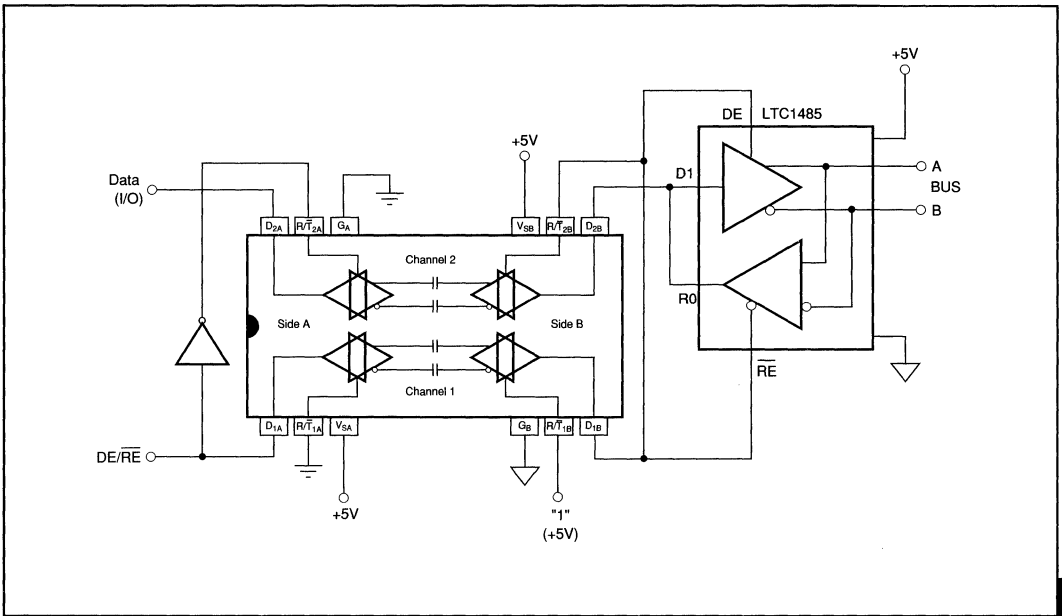


FIGURE 2. Isolated RS-485 Interface.

ISO150

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ISOLATION PRODUCTS

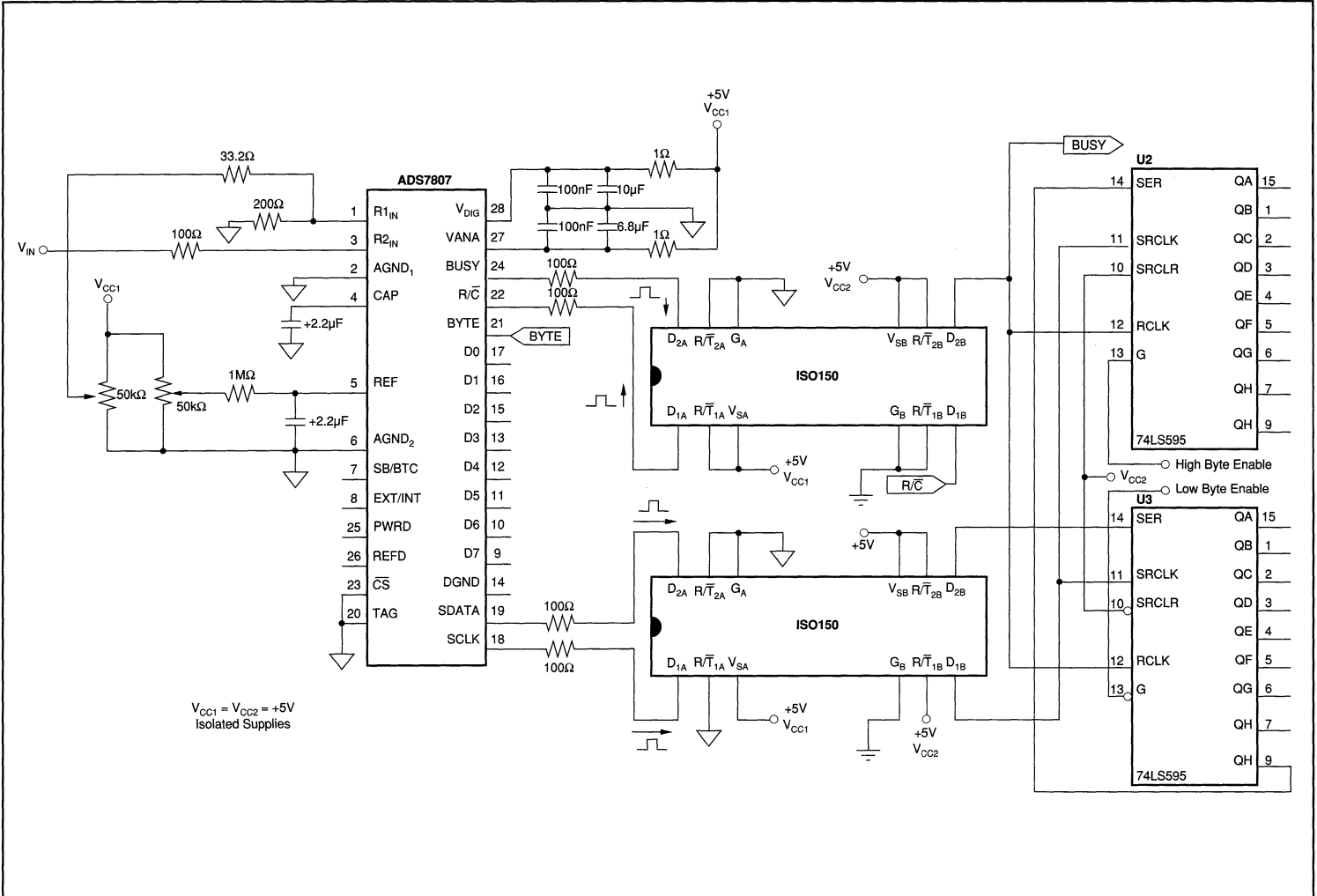


FIGURE 3. ISO150 and ADS7807 is Used to Reduce Circuit Noise in a Mixed Signal Application.

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ISO212P

Low Cost, Two-Port Isolated, Low Profile ISOLATION AMPLIFIER

FEATURES

- 12-BIT ACCURACY
- LOW PROFILE (LESS THAN 0.5" HIGH)
- SMALL FOOTPRINT
- EXTERNAL POWER CAPABILITY ($\pm 8V$ at 5mA)
- "MASTER/SLAVES" SYNCHRONIZATION CAPABILITY
- INPUT OFFSET ADJUSTMENT
- LOW POWER (75mW)
- SINGLE 10V TO 15V SUPPLY OPERATION

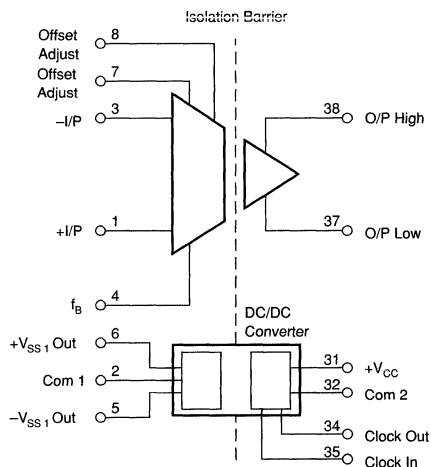
DESCRIPTION

The ISO212P signal isolation amplifier is a member of a series of low-cost isolation products from Burr-Brown. The low-profile SIL plastic package allows PCB spacings of 0.5" to be achieved, and the small footprint results in efficient use of board space.

To provide isolation, the design uses high-efficiency, miniature toroidal transformers in both the signal and power paths. An uncommitted input amplifier and an isolated external bipolar supply ensure the majority of input interfacing or conditioning needs can be met. The ISO212P accepts an input voltage range of $\pm 5V$ for single 15V supply operation or $\pm 3.0V$ for single 10V supply operation.

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Channel Isolator for Thermocouples, RTDs, Pressure Bridges, Flow Meters
- 4mA TO 20mA LOOP ISOLATION
- MOTOR AND SCR CONTROL
- GROUND LOOP ELIMINATION
- ANALYTICAL MEASUREMENTS
- POWER PLANT MONITORING
- DATA ACQUISITION/TEST EQUIPMENT ISOLATION
- MULTIPLEXED SYSTEMS WITH CHANNEL TO CHANNEL ISOLATION



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PDS-881D

5.117

ISO212P

5

ISOLATION PRODUCTS

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SPECIFICATIONS

ELECTRICAL

At $T = +25^{\circ}\text{C}$ and $V_{\text{CC}} = +15\text{V}$ unless otherwise noted.

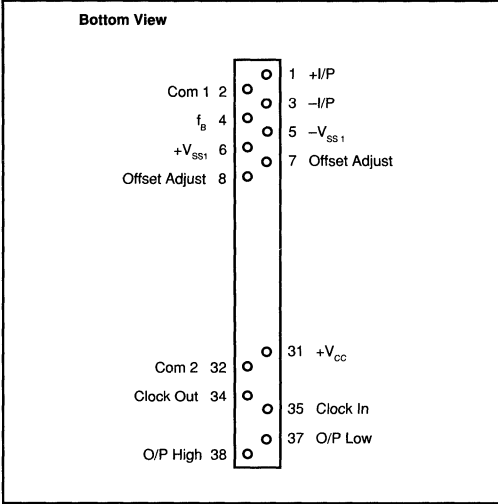
PARAMETER	CONDITIONS	ISO212JP			ISO212KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ISOLATION								
Voltage								
Rated Continuous					*			Vrms
AC, 60Hz	T_{MIN} to T_{MAX}	750			*			VDC
DC	T_{MIN} to T_{MAX}	1060			*			
100% Test (AC, 60Hz)	Partial Discharge				*			Vrms
	1s : <5pC	1200			*			
Isolation-Mode Rejection ⁽¹⁾	$V_{\text{ISO}} = \text{Rated}$							
	Continuous 60Hz							
AC			115			*		dB
DC			160			*		dB
Barrier Resistance			10^{10}			*		Ω
Barrier Capacitance			12			*		pF
Leakage Current	$V_{\text{ISO}} = 240\text{Vrms}, 60\text{Hz}$		1	2		*	*	μArms
	$V_{\text{ISO}} = 240\text{Vrms}, 50\text{Hz}$			1.6		*	*	μArms
GAIN								
Initial Error			± 1	± 2		*	*	% FSR ⁽²⁾
Gain vs Temperature			20	50		*	*	ppm of FSR/ $^{\circ}\text{C}$
Nonlinearity ⁽³⁾	$V_{\text{O}} = -5\text{V to } +5\text{V}$		0.04	0.05		0.015	0.025	%FSR
INPUT OFFSET VOLTAGE								
Initial Offset	$V_{\text{IN}} = 0\text{V}$			$\pm 10 \pm 10/\text{G}$			$\pm 7.5 \pm 7.5/\text{G}$	mV
vs Temperature			$\pm 30 \pm 30/\text{G}$	± 1.5		*	*	$\mu\text{V}/^{\circ}\text{C}$
vs Power Supply ⁽⁴⁾	$V_{\text{CC}} = 14\text{V to } 16\text{V}$					*	*	mV/V
Adjustment Range		± 20			*			mV
INPUT CURRENT								
Bias				50			*	nA
Offset				4			*	nA
INPUT								
Voltage Range ⁽⁵⁾	Rated Operation, $G = 1$	± 5			*			V
Resistance			10^{12}			*		Ω
OUTPUT								
Output Impedance				3		*		k Ω
Voltage Range	Out Hi to Out Lo	± 5			*			V
	Min Load = $1\text{M}\Omega$					*		
Ripple Voltage ⁽⁶⁾	f = 0 to 100kHz		8			*		mVp-p
	f = 0 to 5kHz		0.4			*		mVrms
Output Compliance	Out Hi or Out Lo		7.5			*		V
FREQUENCY RESPONSE								
Small Signal Bandwidth	I/P = 1Vp-p, -3dB		1			*		kHz
	G = 1					*		
Full Signal Bandwidth	I/P = 10Vp-p,		200			*		Hz
	G = 1					*		
	G = 10 (-3dB)		1.8			*		kHz
ISOLATED POWER OUTPUTS								
Voltage Outputs ($\pm V_{\text{SS}}$) ⁽⁷⁾	No Load	± 7.5	± 8		*	*	*	VDC
vs Temperature			-8		*	*	*	mV/ $^{\circ}\text{C}$
vs Load			90		*	*	*	mV/mA
Current Output ⁽⁷⁾				5		*	*	mA
(Both Loaded)				8		*	*	mA
(One Loaded)						*	*	
POWER SUPPLIES								
Rated Voltage	Rated Performance		15			*		V
Voltage Range ⁽⁶⁾		11.4		16	*	*	*	V
Quiescent Current	No Load		4.3	7		*	*	mA
TEMPERATURE RANGE								
Specification		0		+70	*	*	*	$^{\circ}\text{C}$
Operating		-25		+85	*	*	*	$^{\circ}\text{C}$

*Same as ISO212JP.

NOTES: (1) Isolation-mode rejection is the ratio of the change in output voltage to a change in isolation barrier voltage. It is a function of frequency. (2) FSR = Full Scale Range = 10V. (3) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR. (4) Power Supply Rejection is the change in V_{CC} /Supply Change. (5) At $V_{\text{CC}} = +10.0\text{V}$, input voltage range = $\pm 3.0\text{V}$ min. (6) Ripple is the residual component of the barrier carrier frequency generated internally. (7) Derated at $V_{\text{CC}} < +15\text{V}$.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Without Damage	18V
Continuous Isolation Voltage Across Barrier	750Vrms
Storage Temperature Range	-25°C to 100°C
Lead Temperature (soldering, 10s)	+300°C
Amplifier Output Short-Circuit Duration	Continuous to Common
Output Voltage Hi or Lo to Com 2	$\pm V_{CC}/2$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ISO212JP	38-Pin Plastic SIP	903
ISO212KP	38-Pin Plastic SIP	903

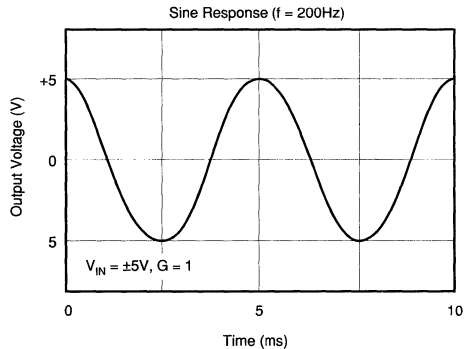
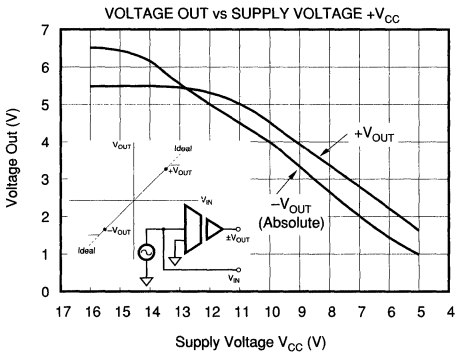
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	OPERATING TEMPERATURE RANGE
ISO212JP	38-Pin Plastic SIP	-25°C to +85°C
ISO212KP	38-Pin Plastic SIP	-25°C to +85°C

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

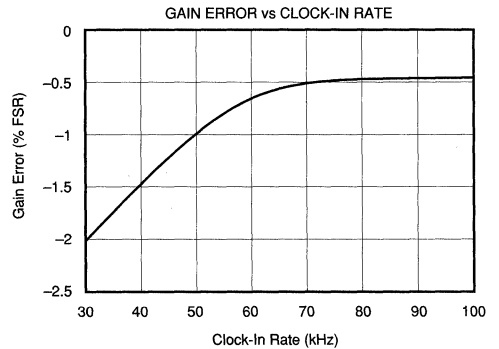
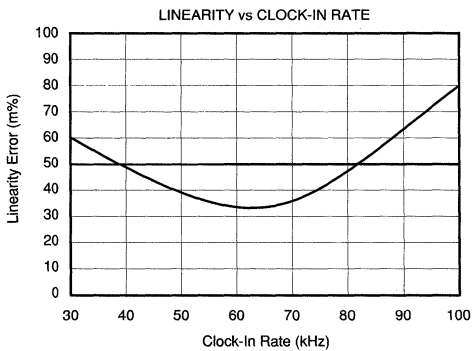
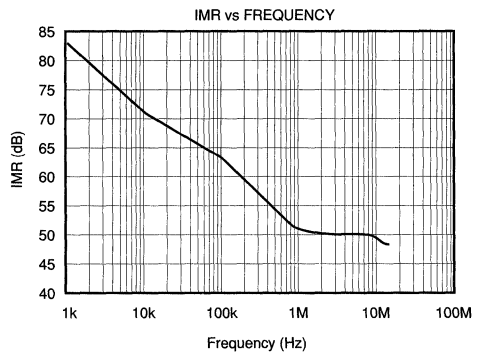
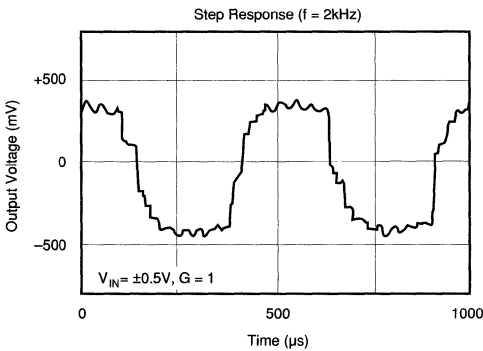
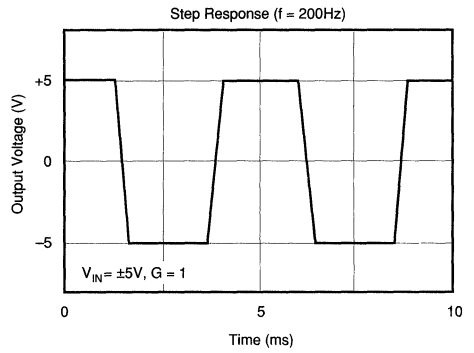
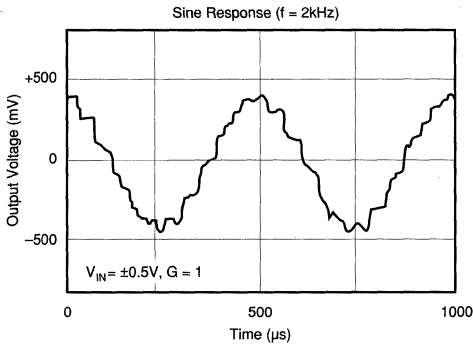


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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

The ISO212P is intended for applications where isolation and input signal conditioning are required. Best signal-to-noise performance is obtained when the input amplifier gain setting is such that the f_b pin has a full scale range of $\pm 5V$. The bandwidth is internally limited to typically 1kHz, making the device ideal for use in conjunction with sensors that monitor slowly varying processes. To power external functions or networks, 5mA at $\pm 8V$ typical is available at the isolated port.

LINEARITY PERFORMANCE

The ISO212P offers non-linearity performance compatible with 12-bit resolution systems (0.025%). Note that the specification is based on a best-fit straight line.

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

In many applications, the untrimmed input offset voltage will be adequate. For situations where it is necessary to trim the offset, a potentiometer can be used. See Figure 1 for details. It is important to keep the traces to the offset adjust pins as short as practical, because noise can be injected into the input op amp via this route.

INPUT PROTECTION

If the ISO212P is used in systems where a transducer or sensor does not derive its power from the isolated power available from the device, then some input protection must be present to prevent damage to the input op amp when the ISO212P is not powered. A resistor of 5k Ω should be included to limit the output impedance of the signal source. Where the op amp is configured for an inverting gain, then R_{IN} of the gain setting network can be used. For non-

inverting configurations, a separate resistor is required. Neglecting this point may also lead to problems when powering on the ISO212P.

USING $\pm V_{SS1}$ TO POWER EXTERNAL CIRCUITRY

The DC/DC converter in the ISO212P runs at a switching frequency of 25kHz. Internal rectification and filtering is sufficient for most applications at low frequencies or with no external networks connected.

The ripple on $\pm V_{SS1}$ will typically be 100mVp-p at 25kHz. Loading the supplies will increase the ripple unless extra filtering is added externally; a capacitor of 1 μF is normally sufficient for most applications, although in some cases 10 μF may be required. Noise introduced onto $\pm V_{SS1}$ should be decoupled to prevent degraded performance.

THEORY OF OPERATION

The ISO212P has no galvanic connection between the input and output. The analog input signal referenced to the input common (Com 1) is multiplied by the gain of the input amplifier and accurately reproduced at the output. The output section uses a differential design so either the Hi or Lo pin may be referenced to the output common (Com 2). This allows simple input signal inversion while maintaining the high impedance input configuration. A simplified diagram of the ISO212P is shown in Figure 2. The design consists of a DC/DC converter, an uncommitted input operational amplifier, a modulator circuit and a demodulator circuit. Magnetic isolation is provided by separate transformers in the power and signal paths.

The DC/DC converter provides power and synchronization signals across the isolation barrier to operate the operational amplifier and modulator circuitry. It also has sufficient capacity to power external input signal conditioning net-

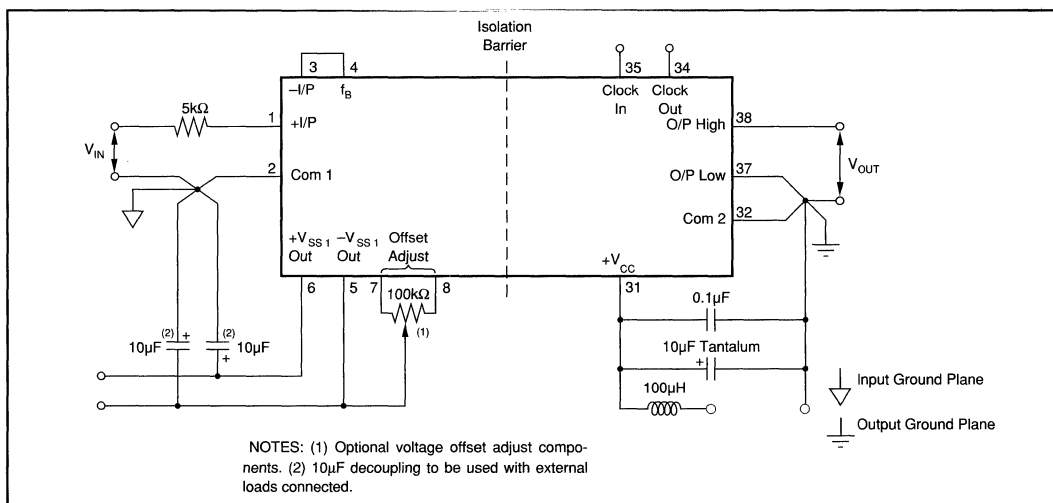


FIGURE 1. Power Supply and Signal Connections Shown for Non-Inverting, Unity Gain Configuration.

The bulk inception voltage, on the other hand, varies with the insulation system and the number of ionization defects. This directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin.

Measuring the bulk extinction voltage provides a lower, more conservative, voltage from which to derive a safe continuous rating. In production, it's acceptable to measure at a level somewhat below the expected inception voltage and then de-rate by a factor related to expectations about the system transients. The isolation amplifier has been extensively evaluated under a combination of high temperatures and high voltage to confirm its performance in this respect. The ISO212P is free of partial discharges at rated voltages.

PARTIAL DISCHARGE TESTING IN PRODUCTION

Not only does this test method provide far more qualitative information about stress withstand levels than did previous stress tests, but it also provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers such as those of high voltage power distribution equipment for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to measure partial discharge, and VDE, the German standards group, has adopted use of this method for the testing of opto-couplers. To accommodate poorly defined transients, the part under test is exposed to a voltage that is 1.6 times the continuous rated voltage and must display <5pC partial discharge level in a 100% production test.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

As with any mixed analog and digital signal component, correct decoupling and signal routing precautions must be used to optimize performance. Figure 1 shows the proper power supply and signal connections. V_{CC} should be bypassed to Com 2 with a 0.1 μ F ceramic capacitor as close to the device as possible. Short leads will minimize lead inductance. A ground plane will also reduce noise problems. If a low impedance ground plane is not used, signal common lines, and either O/P High or O/P Low pin should be tied directly to the ground at the supply and Com 2 returned via a separate trace to the supply ground.

To avoid gain and isolation mode (IMR) errors introduced by the external circuit, connect grounds as indicated in Figure 3. Layout practices associated with isolation amplifiers are very important. In particular, the capacitance associated with the barrier, and series resistance in the signal and reference leads, must be minimized. Any capacitance across

the barrier will increase AC leakage and, in conjunction with ground line resistance, may degrade high frequency IMR.

VOLTAGE GAIN MODIFICATIONS

The uncommitted operational amplifier at the input can be used to provide gain, signal inversion, active filtering or current to voltage conversion. The standard design approach for any op-amp stage can be used, provided that the full scale voltage appearing on f_b does not exceed $\pm 5V$.

If the input op-amp is overdriven, ripple at the output will result. To prevent this, the feedback resistor should have a minimum value of 10k Ω .

Also, it should be noted that the current required to drive the equivalent impedance of the feedback network is supplied by the internal DC/DC converter and must be taken into account when calculating the loading added to $\pm V_{SS1}$.

Since gain inversion can be incorporated in either the input or output stage of the ISO212P, it is possible to use the input amplifier in a non-inverting configuration and preserve the high impedance this configuration offers. Signal inversion at the output is easily accomplished by connecting O/P High to Com 2 instead of O/P Low.

ISOLATED POWER OUTPUT DRIVE CAPABILITY

On the input side of the ISO212P, there are two power supplies capable of delivering 5mA at $\pm 8V$ to power external circuitry. When using these supplies with external loads, it is recommended that additional decoupling in the form of 10 μ F tantalum bead capacitors be added to improve the voltage regulation. Loss of linearity will result if additional filtering is not used with an output load. Again, power dissipated in the feedback loop around the input op amp must be subtracted from the available power output at $\pm V_{SS1}$.

If the ISO212P is to be used in multiple applications, care should be taken in the design of the power distribution

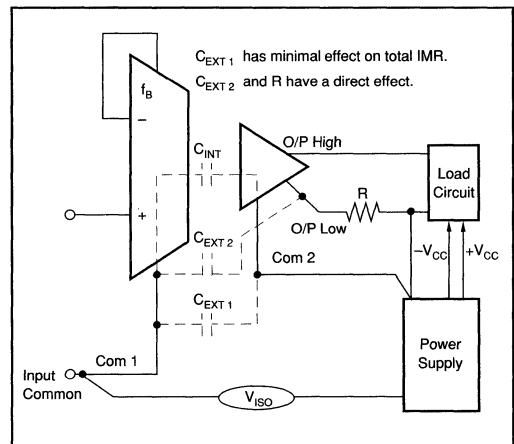


FIGURE 3. Technique for Connecting Com 1 and Com 2.

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network, especially when all ISO212Ps are synchronized. It is best to use a well decoupled distribution point and to take power to individual ISO212Ps from this point in a star arrangement as shown in Figure 4.

NOISE

Output noise is generated by residual components of the 25kHz carrier that have not been removed from the signal. This noise may be reduced by adding an output low pass filter (see Figure 8). The filter time constants should be set below the carrier frequency. The output from the ISO212P is a switched capacitor and requires a high impedance load to prevent degradation of linearity. Loads of less than $1M\Omega$ will cause an increase in noise at the carrier frequency and will appear as ripple in the output waveform. Since the output signal power is generated from the input side of the barrier, decoupling of the $\pm V_{SS1}$ outputs will improve the signal to noise ratio.

SYNCHRONIZATION OF THE INTERNAL OSCILLATOR

The ISO212P has an internal oscillator and associated timing components, which can be synchronized, incorporated into the design. This alleviates the requirement for an external high-power clock driver. The typical frequency of oscillation is 50kHz. The internal clock will start when power is applied to the ISO212P and Clk In is not connected.

Because the frequencies of several ISO212Ps can be marginally different, "beat" frequencies ranging from a few Hz to a few kHz can exist in multiple amplifier applications. The design of the ISO212P accommodates "internal synchronous" noise, but a synchronous beat frequency noise will not be strongly attenuated, especially at very low frequencies if it is introduced via the power, signal, or potential grounding paths. To overcome this problem in systems where several ISO212Ps are used, the design allows synchronization of each oscillator in a system to one frequency. Do this by forcing the timing node on the internal oscillator with an

external driver connected to Clk In. See Figure 5. The driver may be an external component with Series 4000 CMOS characteristics, or one of the ISO212Ps in the system can be used as the master clock for the system. See Figure 6 and 7 for connections in multiple ISO212P installations.

CHARGE ISOLATION

When more than one ISO212P is used in synchronous mode, the charge which is returned from the timing capacitor (220pF in Figure 5) on each transition of the clock becomes significant. Figure 7 illustrates a method of isolating the "Clk Out" clamp diodes (Figure 5) from this charge.

A $22k\Omega$ resistor (recommended maximum to use) together with the $39k\Omega$ internal oscillator timing resistor (Figure 5) forms a potential divider. The ratio of these resistors should be greater than 0.6 which ensures that the input voltage triggers the inverter connected to "Clk In". If using a single resistor, then account must be taken of the paralleled timing resistors. This means that the $22k\Omega$ resistor must be halved to drive two ISO212Ps, or divided by 8 if driving 8 ISO212Ps to insure that the ratio of greater than 0.6 is maintained. The series resistors shown in Figure 7 reduce the high frequency content of the power supply current.

APPLICATIONS

The ISO212P isolation amplifier, together with a few low cost components, can isolate and accurately convert a 4-to-20mA input to a $\pm 10V$ output with no external adjustment. Its low height (0.43" (11mm)) and small footprint (2.5" x 0.33" (57mm x 8mm)) make it the solution of choice in 0.5" board spacing systems and in all applications where board area savings are critical.

The ISO212P operates from a single +15V supply and offers low power consumption and 12-bit accuracy. On the input side, two isolated power supplies capable of supplying 5mA at $\pm 8V$ are available to power external circuitry.

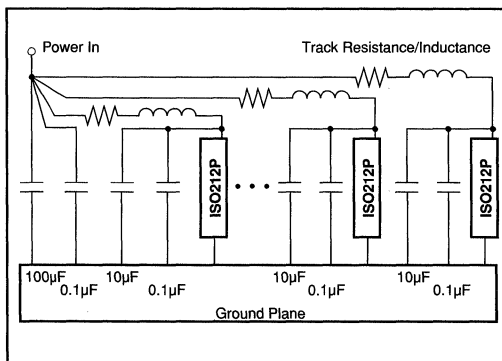


FIGURE 4. Recommended Decoupling and Power Distribution.

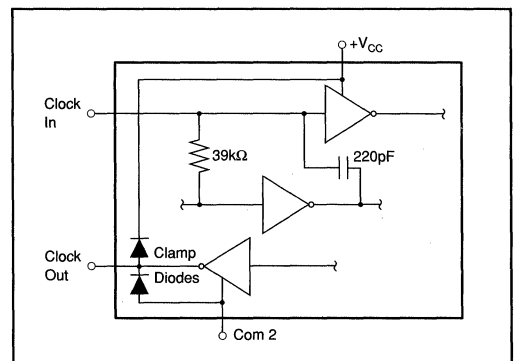


FIGURE 5. Equivalent Circuit, Clock Input/Output. Inverters are CMOS.

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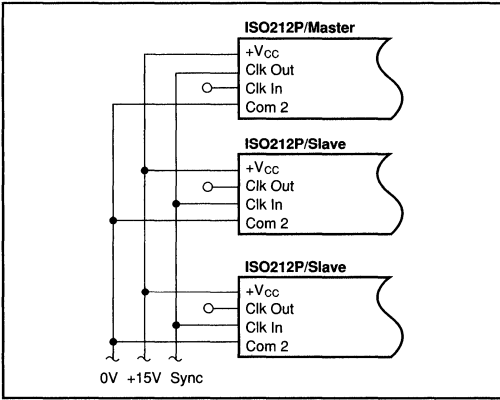


FIGURE 6. Oscillator Connections for Synchronous Operation in Multiple ISO212P Installations.

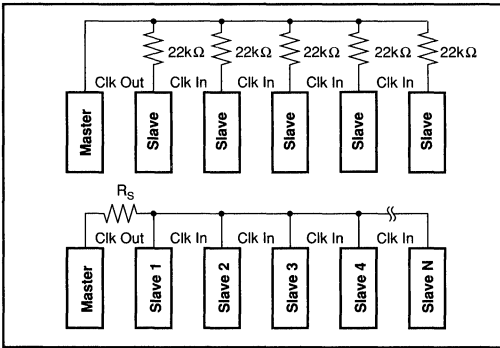


FIGURE 7. Isolating the Clk Out Node.

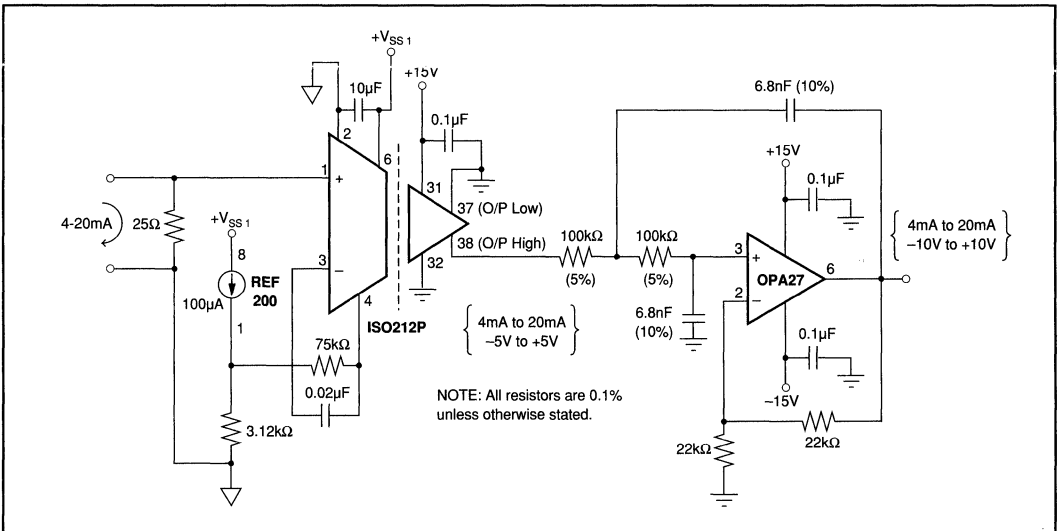


FIGURE 8. Isolated 4-20mA Current Receiver with Output Filter.

APPLICATIONS FLEXIBILITY

In Figure 8, the ISO212P's $+V_{SS1}$ isolated supply powers a REF200 to provide an accurate 100 μ A current source. This current is opposed by an equal but opposite current through the 75k Ω feedback resistor to establish an offset of -7.5V at $I_{in} = 0$ mA. With $I_{in} = 4$ -to-20mA, the output is -5 to +5V. The ratio of the 75k Ω and 3.12k Ω resistors assures the correct gain.

The polarity of the output can be reversed by simply reversing the O/P HI and O/P LO pins. This could be used in the Figure 8 circuit to change the -5V to +5V output to a +5V to -5V output range.

The primary function of the output circuitry is to add gain to produce a ± 10 V output and to reduce output impedance. The addition of a few resistors and capacitors provides a low pass filter with a cut-off frequency equal to the full signal bandwidth of the ISO212P, typically 200Hz. The filter response is flat to 1dB and rolls off from cut off at -12dB per octave.

The accuracy of the REF200 and external resistors eliminates the need for expensive trim pots and adjustments. The errors introduced by the external circuitry only add about 10% of the ISO212P's specified gain and offset voltage error.

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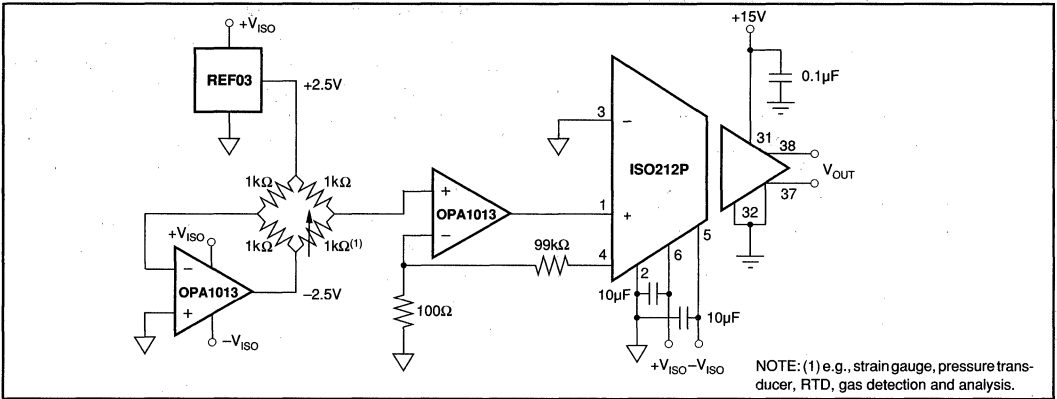


FIGURE 9. Instrument Bridge Isolation Amplifier.

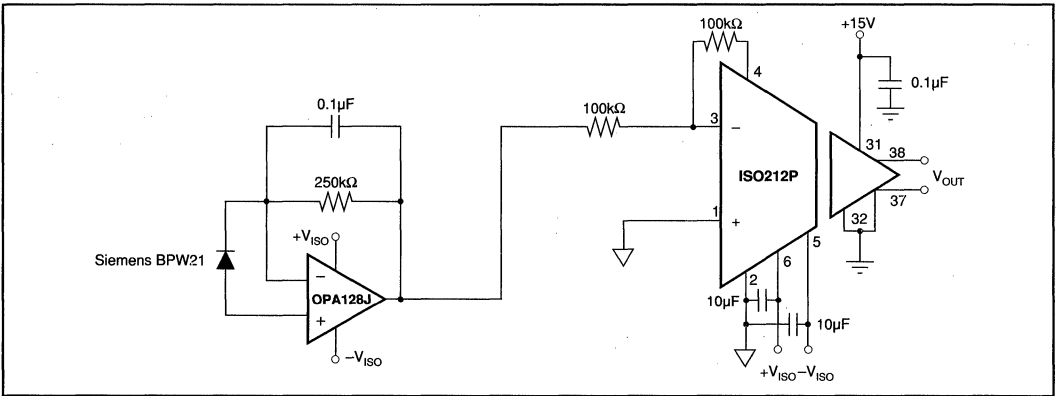


FIGURE 10. Photodiode Isolation Amplifier.

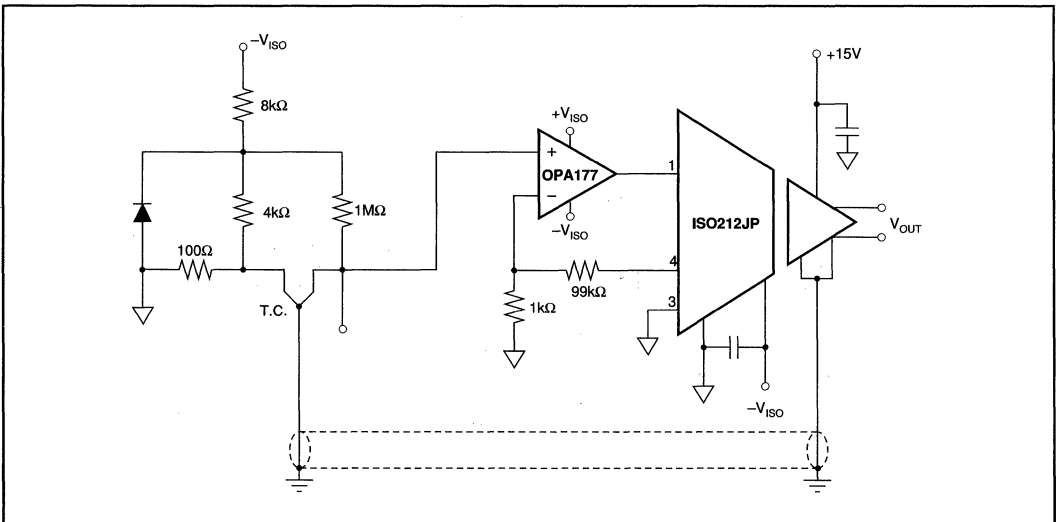


FIGURE 11. Thermocouple Amplifier with Ground Loop Elimination, Cold Junction Compensation and Down-Scale Burn-Out.

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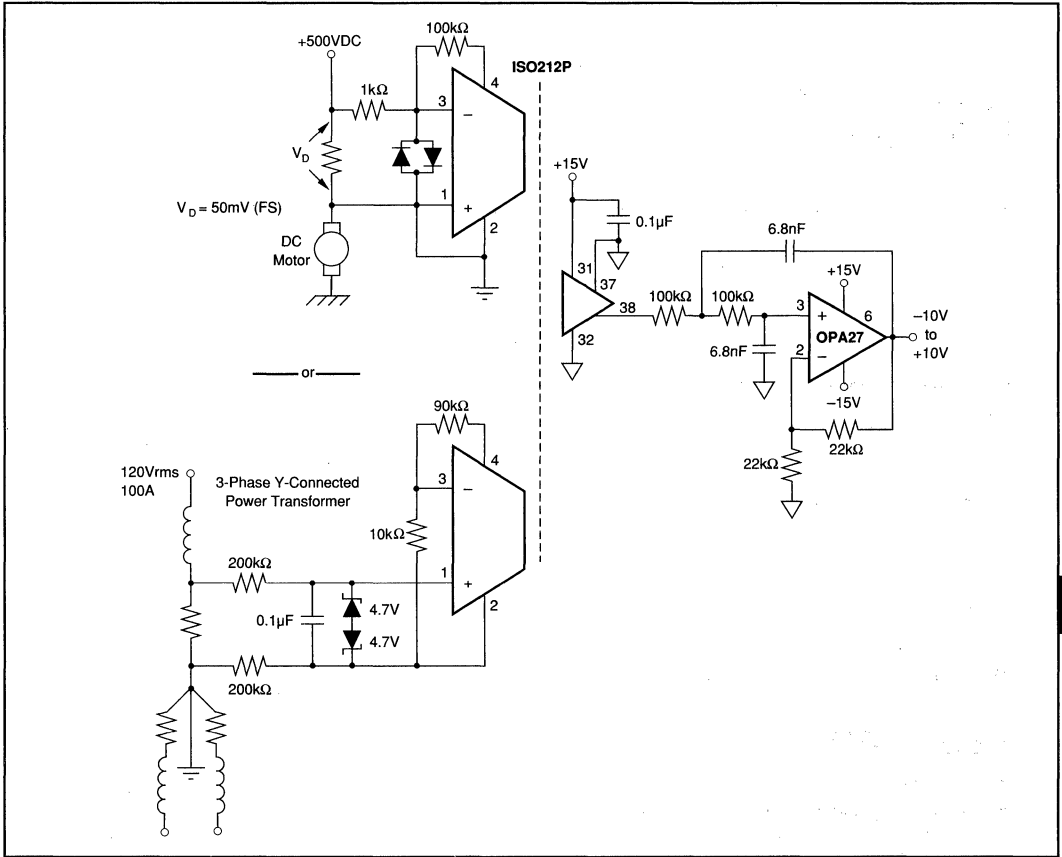


FIGURE 12. Isolated Current Monitoring Applications.

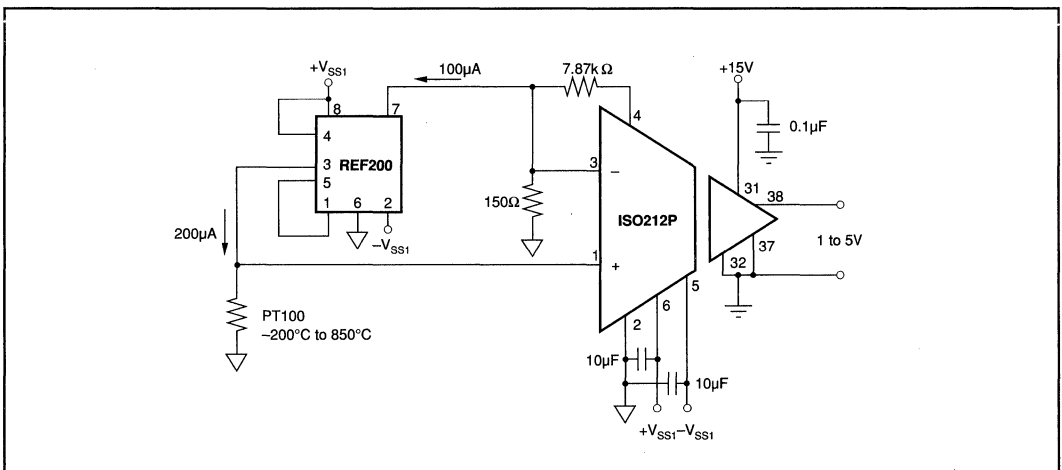


FIGURE 13. Isolated Temperature Sensing and Amplification.

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IXR100

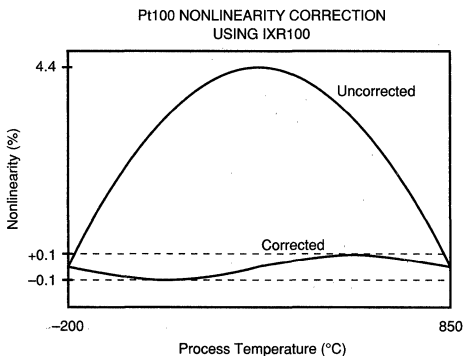
Isolated, Self-Powered, Temperature Sensor Conditioning 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- 1500Vrms ISOLATION
- TRUE TWO-WIRE OPERATION :
Power and Signal on One Wire Pair
- RESISTANCE OR VOLTAGE INPUT
- DUAL MATCHED CURRENT SOURCES:
400 μ A at 7V
- WIDE SUPPLY RANGE 12V TO 36V
- PT100 RTD LINEARIZATION

DESCRIPTION

The IXR100 is an isolated 2-wire transmitter featuring loop powered operation and resistive temperature sensor conditioning (excitation and linearization). It contains a DC/DC convertor, high accuracy instrumentation amplifier with single resistor programmable span and linearization, and dual matched excitation current sources. This combination is ideally suited to a range of transducers such as thermocouples, RTDs, thermistors and strain gages. The small size makes it ideal for use in head mounted isolated temperature transmitters as well as rack and rail mounted equipment.

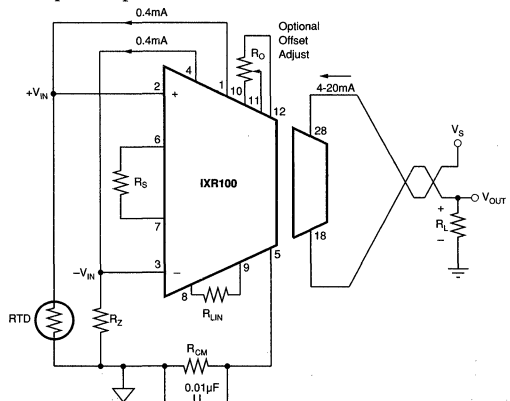


APPLICATIONS

- INDUSTRIAL PROCESS CONTROL:
All Types of Isolated Transmitters;
Pt100 RTD
Thermocouple Inputs
Current Shunt (mV) Inputs
- ISOLATED DUAL CURRENT SOURCES
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY MONITORING
- GROUND LOOP ELIMINATION

The isolated two-wire transmitter allows signal transmission and device power to be supplied on a single wire-pair by modulating the power supply current with the isolated signal source. The transmitter is resistant to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers and industrial equipment.

It can be used by OEMs producing isolated transmitter modules or by data acquisition system manufacturers. The IXR100 is also useful for general purpose isolated current transmission where the elimination of ground loops is important.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

$V_S = +24V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	IXR100			UNITS	
		MIN	TYP	MAX		
OUTPUT AND LOAD CHARACTERISTICS						
Output Current	Linear Operating Region	4		20	mA	
Output Current Limit			32		mA	
Loop Supply Voltage		11.6		36	VDC	
Load Resistance		$R_{LOAD} = (V_S - 11.6)/I_O$			Ω	
ZERO						
Initial Error ⁽¹⁾ vs Temperature	$V_{IN} = 0$, $R_S = \infty$			300 200	μA ppm FSR/ $^\circ C$	
SPAN						
Output Current Equation	R_S in Ω , V_{IN} in V	$I_O = 4mA + [0.016 + (40/R_S)] (V_{IN})$ $S = [0.016 + (40/R_S)]$				
Span Equation						
Untrimmed Error vs Temperature	Excluding TCR of R_S	⁽¹⁾ -2.5	50	0 100	A/V % ppm/ $^\circ C$	
Nonlinearity : EMF Input		⁽²⁾	0.01	0.025	%FSR	
: Pt100 Input		⁽³⁾	0.1		%FSR	
INPUT						
Voltage Range	$R_S = \infty$ V_{IN+} , V_{IN-} with Respect to COM	2	1	4	V	
Common-Mode Range						V
Offset Voltage vs Temperature			0.5	2.5	mV	
vs Supply			3 100	5	$\mu V/^\circ C$ dB	
CURRENT SOURCES						
Magnitude			0.4		mA	
Accuracy vs Temperature			50	100	% ppm/ $^\circ C$	
Match vs Temperature			25	50	% ppm/ $^\circ C$	
DYNAMIC RESPONSE						
Settling Time	To 0.1% of Span		500		ms	
TEMPERATURE RANGE						
Operating		-20		+70	$^\circ C$	
Storage		-40		+85	$^\circ C$	
ISOLATION						
Isolation Voltage	V_{ISO} V_{ISO}	1000 JP 1500 KP			Vrms Vrms	

NOTES: (1) Can be adjusted to zero. (2) End point span non-linearity. (3) End point, corrected span non-linearity with a Pt100 RTD input operated from $-200^\circ C$ to $+850^\circ C$.

ABSOLUTE MAXIMUM RATINGS

Power Supply ($+V_S$ - I_{OUT})	40V
Input Voltage (Com to V_{IN})	9V
Storage Temperature Range	$-40^\circ C$ to $+85^\circ C$
Lead Temperature (soldering 10s)	$+300^\circ C$
Output Current Limit Duration	Continuous
Power Dissipation	500mW

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
IXR100	2-wire Transmitter	901

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



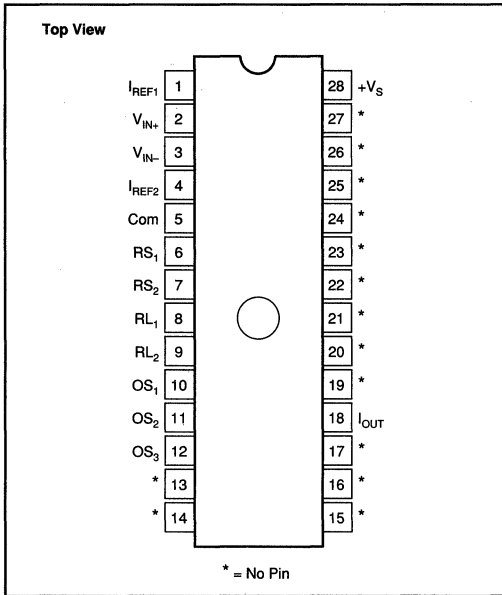
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

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PIN CONFIGURATION



DISCUSSION OF PERFORMANCE

The IXR100 makes the design of isolated two wire 4 to 20mA transmitters easy and provides exceptional performance at very low cost. It combines several unique features not previously available in a single package. These include galvanic isolation, sensor excitation and linearization, excellent DC performance, and low zero and span drift. The IXR100 functions with voltages as low as 11.6V at the device. This allows operation with power supplies at or below 15V. When used with the RCV420 the complete 4 to 20mA current loop requires only 13.1V. If series diode protection is desired the minimum loop supply voltage is still only about 13.7V. This is especially useful in systems where the available supplies are only 15V.

BASIC CONNECTION

The basic connection of the IXR100 is shown in Figure 1. A differential voltage applied between pins 2 and 3 will cause a current of 4 to 20mA to circulate in the two wire output loop pins 28 and 18. Pins 1 and 4 supply the current excitation for resistive sensors. Pins 6 and 7 are provided for the connection of an external span resistor which increases the gain. Pins 8 and 9 provide linearity correction. Pins 10, 11 and 12 adjust the output offset current.

FUNCTIONAL DESCRIPTION

The IXR100 comprises of several functions:

- Sensor excitation
- Internal voltage regulator
- Input amplifier and V/I converter
- Linearization circuit
- DC/DC Converter

SENSOR EXCITATION

Sensor Excitation consists of two matched 0.4mA current sources. One is used to excite the resistive sensor and the other is used to excite the zero balance resistor R_z . When the linearity correction feature is used these current sources are modulated together so that three wire operation of a Pt100 RTD is possible.

INTERNAL VOLTAGE REGULATOR

The circuitry within the IXR100 regulates the supply voltage to the DC/DC Converter, Input Amplifier, Linearization Amplifier and V/I Converter and removes the normal variations in V_s from these stages as the output spans from 4 to 20mA.

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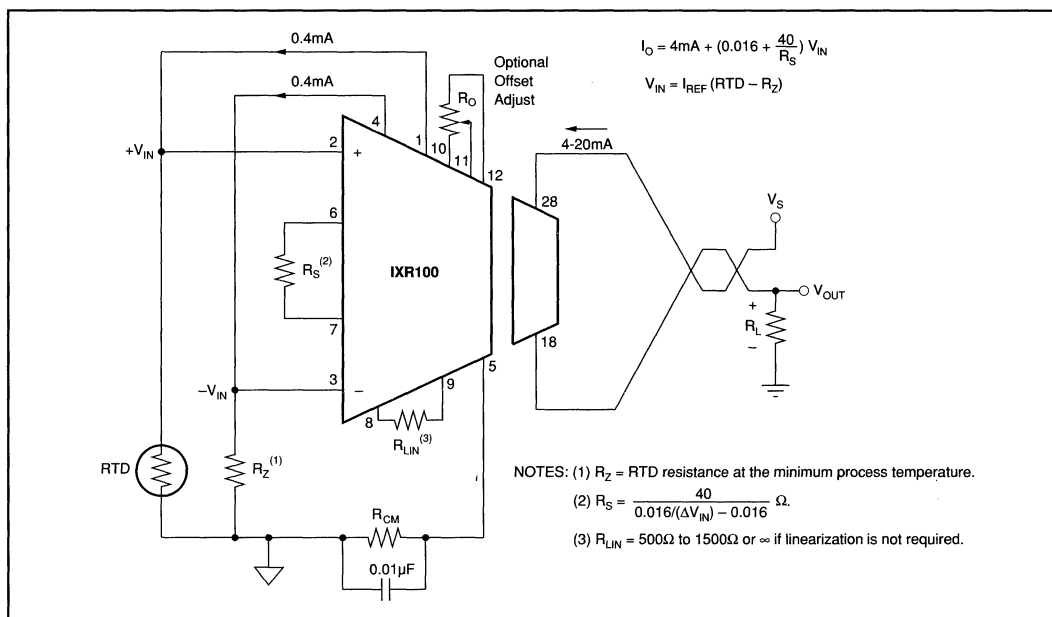


FIGURE 1. Basic Connection for RTD.

INPUT AMPLIFIER AND V/I CONVERTER

The Input Amplifier is an instrumentation amplifier whose gain is set by R_S , it drives the V/I Converter to produce a 4 to 20mA output current. The Input Amplifier has a common mode voltage range of 2 to 4V with respect to COM (pin 5). Normally this requirement is satisfied by returning the currents from the RTD and zero balance resistor R_Z to COM through a common mode resistor R_{CM} . For most applications a single value of $3.9\text{k}\Omega$ may be used. When used with RTDs having large values of resistance R_{CM} must be chosen so that the inputs of the amplifier remain within its rated common mode range. R_{CM} should be bypassed with a $0.01\mu\text{F}$ or larger capacitor.

LINEARIZATION CIRCUIT

The Linearity Correction Circuit is unique in several ways. A single external resistor will provide up to 50 times improvement in the basic RTD linearity. Terminal based non-linearity can be reduced to less than $\pm 0.1\%$ for all RTD temperature spans. The Linearization circuit also contains an instrumentation amplifier internally connected to the $\pm V_{IN}$ pins. The gain of this stage is set by R_{LIN} . The output controls the excitation current sources to produce an increasing excitation current as V_{IN} increases. An important feature is that the Linearity Correction is made directly to the RTD output independent of the gain of the Input Amplifier. This provides minimal interaction between R_S and R_Z . This feature can be useful at the systems level by reducing data acquisition system processor overhead previously used to linearize sensor response in software/firmware.

DC/DC CONVERTER

The DC/DC Converter transfers power from the 2 wire current loop across the barrier to the circuitry used on the input side of the isolation barrier.

PIN DESCRIPTIONS

I_{REF1}, I_{REF2}

These pins provide a matched pair of current sources for sensor excitation. These current sources provide excellent thermal tracking, and when the linearization feature is used, are modulated by an equal amount. Their nominal current value is 0.4mA and their compliance voltage is:

$$V_{IN} + < V_{REF} < (\text{Com} + 7\text{V})$$

$$I_{REF} = 400\mu\text{A} + \frac{V_{REF}}{2R_{LIN}}$$

$+V_{IN}, -V_{IN}$

These are the inputs to both the input amplifier and the linearization amplifier. Because the IXR100 has been optimized for RTD applications, the two sets of inputs are internally connected.

R_{S1}, R_{S2}

The resistor connected across these terminals determines the gain of the IXR100. For normal 4-20mA outputs:

$$R_S = \frac{40}{0.016/(\Delta V_{IN}) - 0.016} \Omega \quad (1)$$

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R_{L1} , R_{L2}

The resistor connected between these terminals determines the gain of the linearization circuit and the amount of correction applied to the RTD. Its value may be determined in several ways. Two of which are shown as follows.

- Empirically by interactively adjusting R_{LIN} , R_s and R_z to achieve best fit 4 to 20mA output. R_z is used to set 4mA at minimum input, R_s is adjusted for 12mA with a half span input, and R_{LIN} is adjusted to give 20mA with a full span input. This may require a few iterations but is probably the most practical method for field calibration. R_{LIN} will range between 500Ω and 1500Ω for 100Ω sensors (Pt100, D100, SAMA). Initially it may seem a little strange adjusting R_s for 12mA and R_{LIN} for 20mA. However, convergence is achieved much more quickly as the linearized curve passes through zero and has less effect at the mid span and the linearity trim resistor tends to adjust the transfer function more at the full span than the mid point.
- Using Table I and linear interpolation for values of span not given in the table. This will yield very accurate results for the Pt100 sensor and acceptable results for D100 and SAMA sensors.

ZERO ADJUST (OPTIONAL) O_{S1} , O_{S2} , O_{S3}

The IXR100 has provision for adjusting the output offset current as shown in Figure 2. In many applications the already low offset will not need to be known at all. This trim effects the V/I converter stage and does not introduce V_{OS} drift errors that occur when the trim is performed at the input stage. If possible use R_z to trim sensor output error to zero and use the offset control to trim the output to 4mA when $V_{IN} = 0V$. The offset adjustment can be made with a

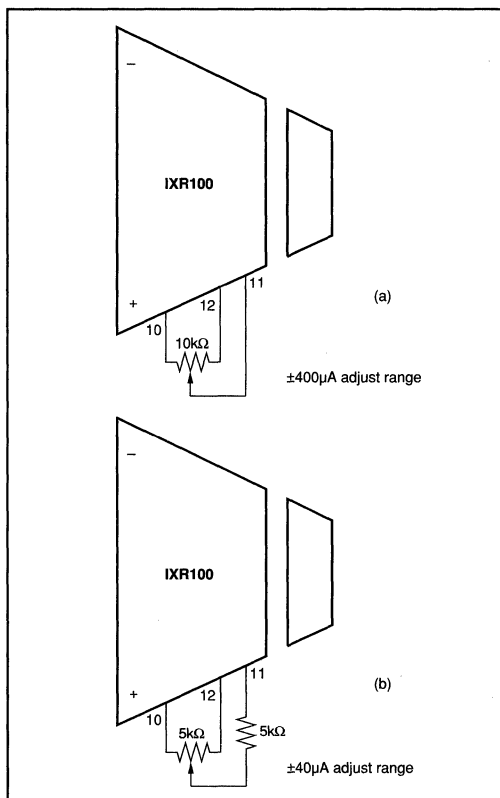


FIGURE 2. Basic Connection for Zero Adjust.

		SPAN ΔT (°C)										
T_{MIN} (°C)		50	100	200	300	400	500	600	700	800	900	1000
-200	573	653	839	995	1083	1131	1152	1159	1159	1154	1140	
-150	745	855	1059	1158	1197	1206	1205	1196	1175	1151	1127	
-100	983	1105	1228	1251	1249	1231	1207	1182	1156	1129		
-50	1233	1284	1286	1262	1236	1208	1180	1152	1125	1097		
0	1302	1287	1273	1229	1201	1173	1145	1117	1089			
50	1263	1249	1220	1192	1164	1136	1108	1081	1054			
100	1225	1211	1183	1155	1127	1100	1073	1046				
150	1188	1174	1146	1119	1091	1064	1038	1011				
200	1151	1137	1110	1083	1056	1030	1003					
250	1114	1101	1074	1048	1021	995	969					
300	1079	1066	1039	1013	987	962						
350	1044	1031	1005	979	954	928						
400	1009	996	971	946	921							
450	975	963	938	913	888							
500	942	930	905	881								
550	909	897	873	849								
600	877	865	841									
650	845	834	810									
700	814	803										
750	784	773										
800	754											

NOTES: (1) Linear interpolation between two horizontal or vertical values yields acceptable values. (2) Although not optimum, these values will also yield acceptable results with D100 and SAMA 100Ω nominal sensors. (3) Double R_{LIN} value for PT200.

TABLE I. R_{LIN} Values for Pt100 Sensor.

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potentiometer connected as shown in Figures 2a and 2b. The circuit shown in Figure 2a provides more range while the circuit in Figure 2b provides better resolution. Note, it is not recommended to use this adjusting procedure for zero elevation or suppression. See the signal suppression and elevation section for the proper techniques.

COM

This is the return for the two excitation currents I_{REF1} and I_{REF2} and is the reference point for the inputs.

V_S, I_{OUT}

These are the connections for the current loop V_S being the most positive connection. For correct operation these pins should have 11.6 to 36V between them.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses ($<5pC$) while applying 2400rms, 60Hz high-voltage stress across every device's isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage ($1.6 \times V_{RATED}$) protection without damage. Life-test results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the-art" for nondestructive high voltage reliability testing. It is based on

the effects of non-uniform fields existing in heterogeneous dielectric material during barrier degradation. In the case of void non-uniformities, electric field stress begins to ionize the void region before bridging the entire high voltage barrier.

The transient conduction of charge during and after the ionization can be detected externally as a burst of $0.01\mu s$ - $0.1\mu s$ current pulses that repeat on each AC voltage cycle. The minimum AC barrier voltage that initiates partial discharge is defined as the "inception voltage". Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage".

We have designed and characterized the package to yield an inception voltage in excess of 2400Vrms so that transient overvoltages below this level will not cause any damage. The extinction voltage is above 1500Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated level. Older high voltage test methods relied on applying a large enough overvoltage (above rating) to catastrophically break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

APPLYING THE IXR100

The IXR100 has been designed primarily to correct nonlinearities inherent in RTD sensors. It may also be used in other applications where its excellent performance makes it superior to other devices available. Examples are shown in the Applications Section.

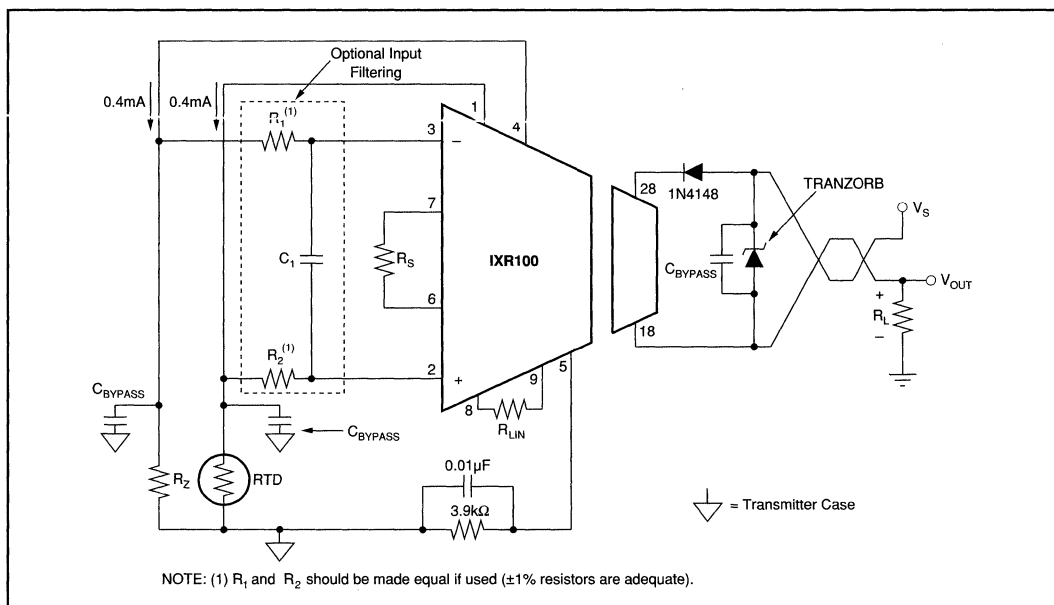


FIGURE 3. Transient and RFI Protection Circuit.

RFI AND TRANSIENT SUPPRESSION

Radio frequency interference and transients are a common occurrence in 4-20mA loops, especially when long wiring lengths are involved. RFI usually appears as a temporary change in output and results from rectification of the radio signal by one or more stages in the amplifier. For sensors which are closely coupled to the IXR100 and are contained in a common metal housing, the usual entry for RFI is via the 4-20mA loop wiring. Coaxial bypass capacitors may be used with great effectiveness to bring these leads into the transducer housing while suppressing the RFI. Values of 100 to 1000pF are generally recommended. For sensors remote from the IXR100, coaxial capacitors can also be used to filter the excitation and signal leads. Additional low-pass filtering at the IXR100 input helps suppress RFI. The easiest way to do this is with the optional differential RC filter shown in Figure 4. Typical values for R_1 and R_2 are 100-1000 Ω , and for C_1 are 100-1000pF.

Transient suppression for negative voltages can be provided by the reverse-polarity protection diodes discussed later. However, positive transients cannot be handled by these diodes and do frequently occur in field-mounted loops. A shunt zener diode is of some help, but most zener diodes suffer from limited current-handling capacity and slow turn-on. Both of these characteristics can lead to device failure before the zener conducts. One type of zener, called the TRANZORB and available from General Semiconductor Industries, is especially effective in protecting against high-energy transients such as those induced by lightning or motor contactors. Choose a TRANZORB with a voltage rating close to, but exceeding, the maximum V_s which the IXR100 will see. In combination, the coaxial bypass capacitors and TRANZORB provide a very high level of protection against transients and RFI.

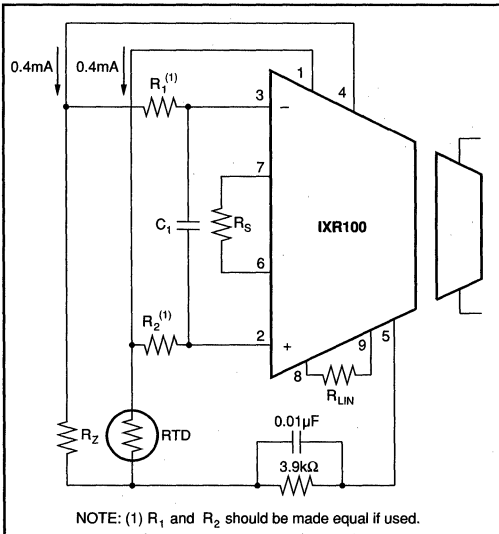


Figure 4. Optional Bandwidth-Limiting Circuitry.

INPUT BANDWIDTH LIMITING

Filtering at the input to the IXR100 is recommended where possible and can be done as shown in Figure 4. C_1 connected to pins 3 and 4 will reduce the bandwidth with a f_{-3dB} frequency given by:

$$f_{-3dB} = 0.159 / (R_1 + R_2 + RTD + R_Z) (C_1 + 3pF)$$

This method has the disadvantage of having f_{-3dB} vary with R_1 , R_2 , RTD , and R_Z may require large values of R_1 and R_2 . R_1 and R_2 should be matched to prevent zero errors due to input bias current.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (span elevation) or elevated zero range (span suppression). This is easily accomplished with the IXR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figure 5. In this example the sensor voltage is derived from RT (a thermistor, RTD or other variable resistance element) excited by one of the 0.4mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6a, 6b, 6c and 6d show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments.

NOTE: Use of the optional offset null (pins 10, 11, and 12) for elevation or suppression is not recommended. This trim technique is used only to trim the IXR100's output offset current.

MAJOR POINTS TO CONSIDER WHEN USING THE IXR100

1. The leads to R_s and R_{LIN} should be kept as short as possible to reduce noise pick-up and parasitic resistance. If the linearity correction feature is not desired, the R_{LIN} pins are left open.
2. $+V_s$ should be bypassed with a 0.01 μF capacitor as close to the unit as possible (pins 18 to 28).
3. Always keep the input voltages within their range of linear operation, +2V to +4V ($\pm V_{IN}$ measured with respect to pin 5).

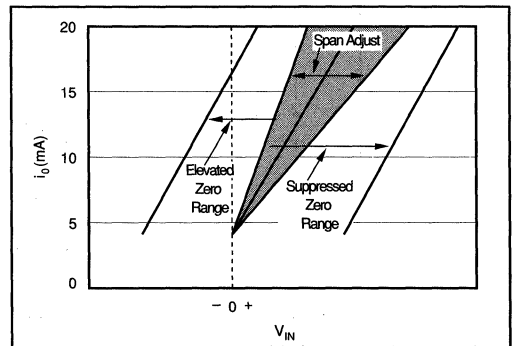


Figure 5. Elevation and Suppression Graph.

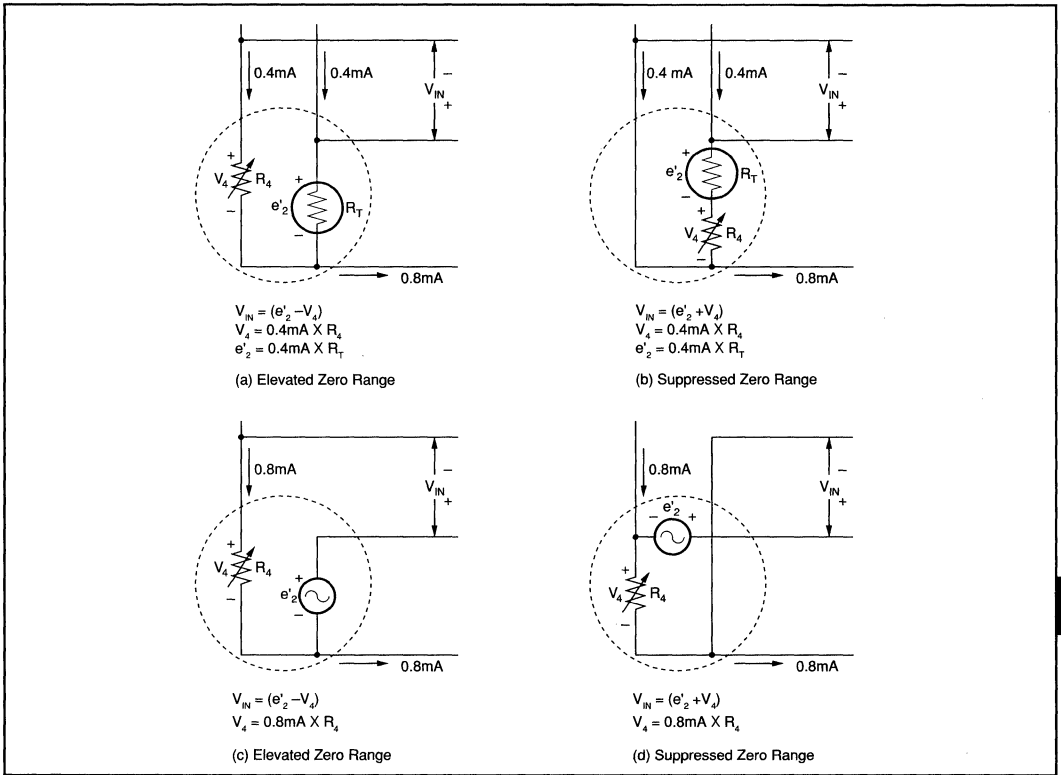


FIGURE 6. Elevation and Suppression Circuits.

- The maximum input signal level (ΔV_{IN}) is 1V with R_S open and is less as R_S decreases in value.
- Always return the current references to COM (pin 5) through an appropriate value of R_{CM} to keep V_{CM} within its operating range. Also, operate the current sources within their rated compliance voltage:

$$V_{IN} + \leq V_{REF} \leq (\text{Com} + 7V)$$

- Always choose R_L (including line resistance) so that the voltage between pins 18 and 28 ($+V_S$) remains within the 11.6V to 36V range as the output changes between 4mA and 20mA.
- It is recommended that a reverse polarity protection diode be used. This will prevent damage to the IXR100 caused by a transient or long-term reverse bias between pins 18 and 28. This diode can be connected in either of the two positions shown in Figure 7, but each connection has its trade-off. The series-connected diode will add to the minimum voltage at which the IXR100 will operate but offers loop and device protection against both reverse connections and transients. The reverse-biased diode in parallel with the IXR100 preserves 11.6V minimum operation and offers device protection, but could allow excessive current flow in the receiving instrument if the field leads are accidentally reversed. This is particularly

important if the receiving equipment has particularly low resistance or uses higher voltage supplies. In general, the series diode is recommended unless 12V operation is necessary. In either case a 1N4148 diode is suitable.

- Use a layout which minimizes parasitic inductance and capacitance, especially in high gain.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

- Remove static-generating materials, such as untreated plastic, from all areas where microcircuits are handled.
- Ground all operators, equipment, and work stations.
- Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
- Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.

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- Control relative humidity to as high a value as practical (50% recommended).

RTD APPLICATIONS

The IXR100 has been designed with RTD applications specifically in mind. The following information provides additional information for those applications.

TWO- AND THREE-WIRE CONNECTIONS

The IXR100 performs well with two-wire and three-wire RTD connections commonly encountered in industrial monitoring and control.

In two-wire applications, the voltage drop between the RTD and the IXR100 can be nulled by proper adjustment of R_z , but care must be taken that this voltage drop does not vary with ambient conditions. Such variation will appear as an apparent variation in the RTD resistance and therefore as a change in measured temperature. Also, the linearity correction will interpret this change as a variation and attempt to linearize both the actual RTD signal and the resistance changes in the signal lines. For these reasons, the line resistance between the RTD and the IXR100 should be minimized by keeping line lengths short and/or using large-gauge wires. This limitation does not apply for three-wire connections.

In three-wire applications, shown in Figure 7, the RTD and R_z lead arrangements set up a pseudo-Kelvin connection to the RTD. This occurs because the currents through the three wires are set up in opposing directions and cancel IR drops in the RTD leads. The current sources are both modulated

equally, so that use of the linearity correction does not affect the cancellation. This action is true so long as the three wires are of the same length and gauge. Because most RTD leads are twisted and bundled, this requirement is usually met with no difficulty. Care must be taken that intermediate connections such as screw terminals do not violate this assumption by introducing unequal line resistances.

RTD ZERO ELEVATION AND SUPPRESSION

The IXR100 may be operated in zero-elevated and zero-suppressed ranges by simply offsetting R_z . It may also be used in increase-decrease applications by interchanging the physical locations of the RTD and R_z as shown in Figure 8. Use the same values of R_z , R_{LIN} and R_S . Again, because the current sources are matched and are modulated equally, this connection has no effect on IXR100 performance, especially in three-wire applications.

OPEN CIRCUIT DETECTION

In some applications of the IXR100, the RTD will be located remotely. In these cases, it is possible for open circuits to develop. The IXR100 responds in the following manner to breaks in each lead. The following connections refer to the RTD connections shown in Figure 7.

TERMINAL OPEN	I_{out}^*
1	32mA
2	3.6mA
3	32mA

*approximate value

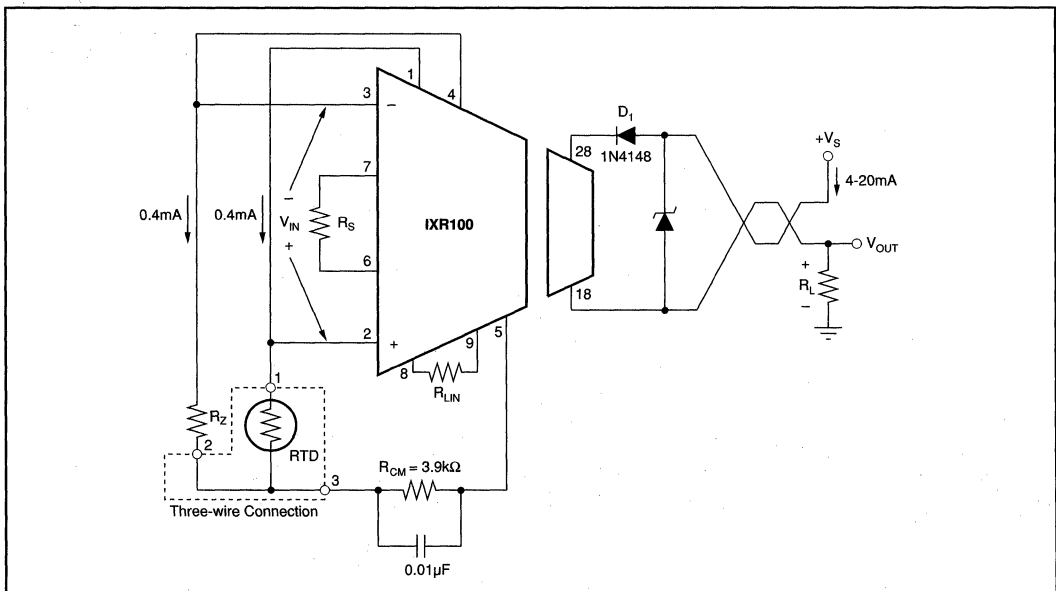


FIGURE 7. Basic 3-Wire RTD Connection for Increase-Increase Action.

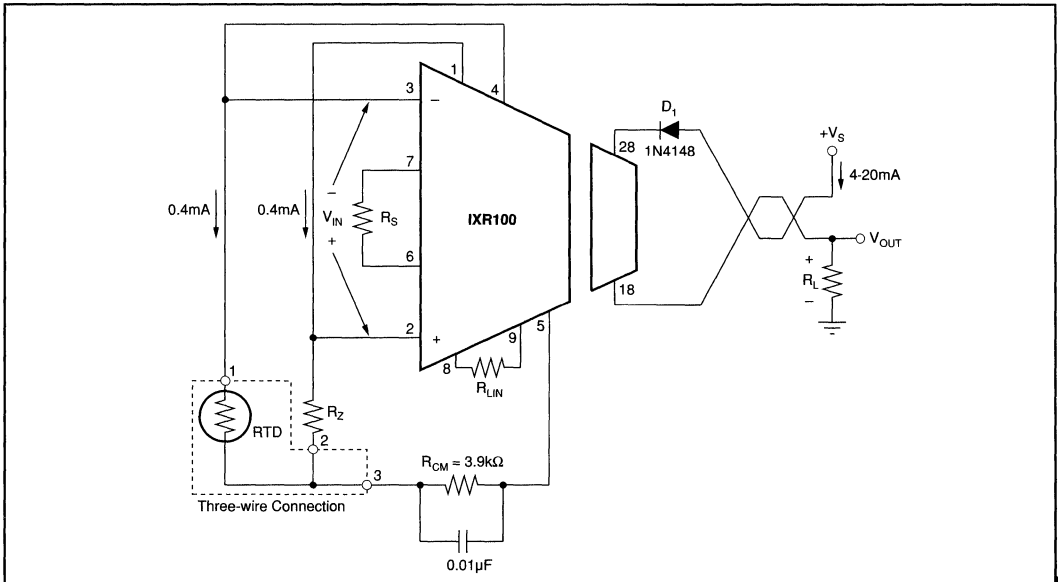


FIGURE 8. Basic 3-Wire RTD Connection for Increase-Decrease Action.

OTHER APPLICATIONS

In instances where the linearization capability of the IXR100 is not required, it can still provide improved performance in several applications. Its small size, wide compliance voltage, low zero and span drift, high PSRR, high CMRR and excellent linearity makes the IXR100 ideal for a variety of other isolated two-wire transmitter applications. It can be used by OEMs producing different types of isolated transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus, the IXR100 is, in general, very suitable for a wide variety of applications. Some examples, including an isolated non-linearized Pt100 case, follow.

EXAMPLE 1

Pt100 RTD without linearization shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the IXR100 to measure the temperature with a Pt100 RTD which produces 109.73Ω at 25°C and 157.31Ω at 150°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C. The change in resistance of the RTD is 47.6Ω. When excited with a 0.4mA current source ΔV_{IN} is $0.4\text{mA} \times 47.6\Omega = 19\text{mV}$.

$$R_s = \frac{40}{0.016/(\Delta V_{IN}) - 0.016} \Omega \quad (1)$$

From Equation (1), $R_s = 48.5\Omega$. Span adjustment (calibration) is accomplished by trimming R_s .

In order to make the lower range limit of 25°C correspond to the output lower range limit at 4mA, the input circuitry shown in Figure 9 is used. V_{IN} must be 0V at 25°C and R_z is chosen to be equal to the RTD resistance at 25°C, or 109.73Ω. Computing R_{CM} and checking CMV:

$$\text{At } +25^\circ\text{C}, V_{IN+} = 43.9\text{mV}$$

$$\text{At } +150^\circ\text{C}, V_{IN+} = 62.9\text{mV}$$

Since both V_{IN+} and V_z are small relative to the desired 2V common-mode voltage, they may be ignored in computing R_{CM} as long as the CMV is met.

$$R_{CM} = 3\text{V}/0.8\text{mA} = 3.75\text{k}\Omega$$

$$V_{IN+} \text{ min} = 3\text{V} + 0.0439\text{V}$$

$$V_{IN+} \text{ max} = 3\text{V} + 0.0629\text{V}$$

$$V_{IN-} = 3\text{V} + 0.0439\text{V}$$

EXAMPLE 2

Thermocouple shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the IXR100 to measure the temperature with a Type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At +25°C this is 1.28mV (from thermocouple tables with reference junction at 0°C). Typically, at $T_2 = +25^\circ\text{C}$, $V_D = 0.6\text{V}$ and

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$\Delta V_D/\Delta T = -2\text{mV}/^\circ\text{C}$. R_5 and R_6 form a voltage divider for the diode voltage V_D . The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At $+25^\circ\text{C}$ this is approximately $-52\mu\text{V}/^\circ\text{C}$ (obtained from standard thermocouple table); therefore,

$$\begin{aligned} \Delta V_{TC}/\Delta T &= (\Delta V_D/\Delta T)(R_6/(R_5 + R_6)) & (2) \\ -52\mu\text{V}/^\circ\text{C} &= (-2000\mu\text{V}/^\circ\text{C})(R_6/(R_5 + R_6)) \end{aligned}$$

R_5 is chosen as $3.74\text{k}\Omega$ to be much larger than the resistance of the diode. Solving for R_6 yields 100Ω .

Transmit 4mA for $T_1 = 0^\circ\text{C}$ and 20mA for $T_1 = +1000^\circ\text{C}$. Note: $V_{IN} = V_{IN+} - V_{IN-}$ indicates that T_1 is relative to T_2 . The input full scale span is 58mV . R_S is found from Equation (1) and equals 153.9Ω .

R_4 is chosen to make the output 4mA at $T_{TC} = 0^\circ\text{C}$ ($V_{TC} = 1.28\text{mV}$) and $T_D = 25^\circ\text{C}$ ($V_D = 0.6\text{V}$).

V_{TC} will be -1.28mV when $T_{TC} = 0^\circ\text{C}$ and the reference junction is at $+25^\circ\text{C}$. V_4 must be computed for $T_D = +25^\circ\text{C}$ to make $V_{IN} = 0\text{V}$.

$$V_{D(25^\circ\text{C})} = 600\text{mV}$$

$$V_{IN(25^\circ\text{C})} = 600\text{mV} (100/3740) = 16.0\text{mV}$$

$$V_{IN} = V_{IN+} - V_{IN-} = V_{TC} + V_4 - V_{IN-}$$

$$\text{With } V_{IN} = 0 \text{ and } V_{TC} = -1.28\text{mV},$$

$$V_4 = V_{IN+} - V_{TC}$$

$$V_4 = 16.0\text{mV} - (-1.28\text{mV})$$

$$0.4\text{mA} (R_4) = 17.28\text{mV}$$

$$R_4 = 43.2\Omega$$

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to the upper or lower limit when the thermocouple impedance goes very high. The circuits of Figures 10, 11 and 12 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.6mA). If up scale indication is desired, the circuit of Figure 13 should be used. When the T_C opens, the output will go to its upper range limit value (about 32mA or higher).

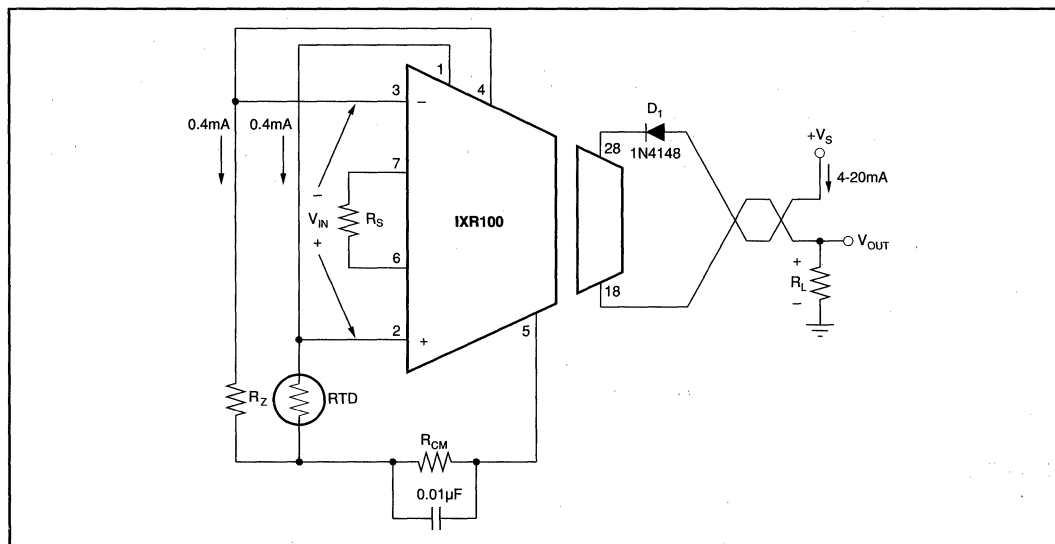


FIGURE 9. Pt100 RTD Without Linearization.

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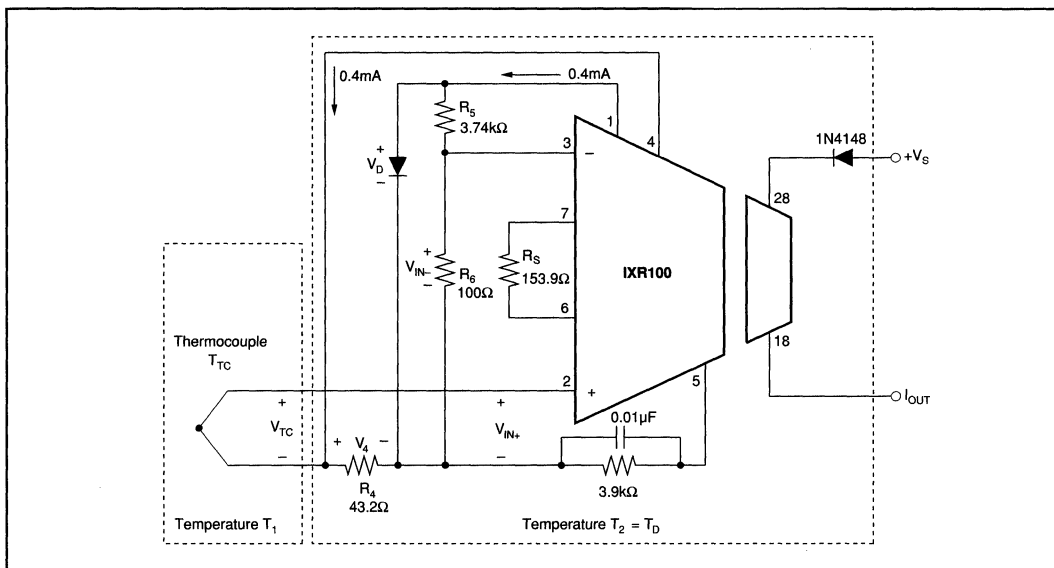


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

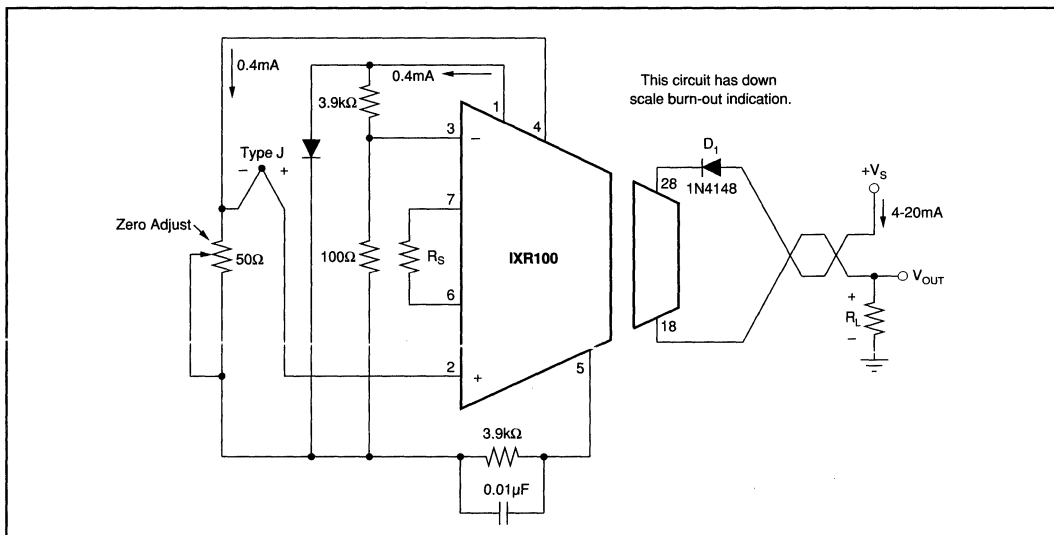


FIGURE 11. Thermocouple Input with Diode Cold Junction Compensation and Down Scale Burn-out Indication.

IXR100

5

ISOLATION PRODUCTS

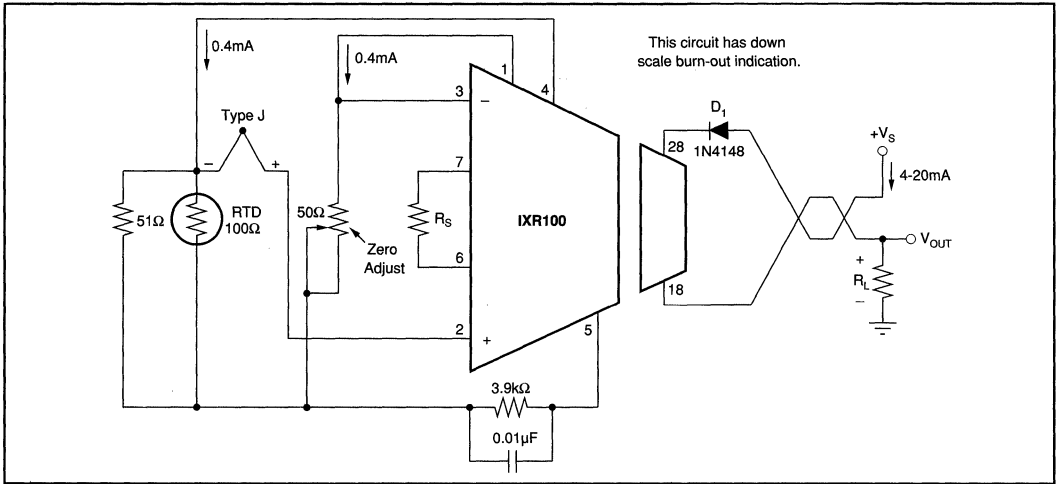


FIGURE 12. Thermocouple Input with RTD Cold Junction Compensation and Down Scale Burn-out Indication.

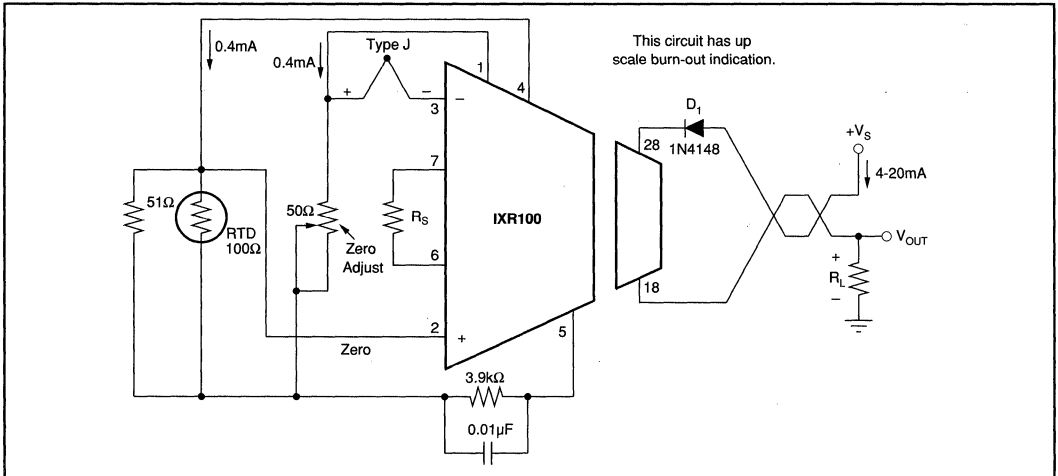


FIGURE 13. Thermocouple Input with RTD Cold Junction Compensation and Up Scale Burn-out Indication.

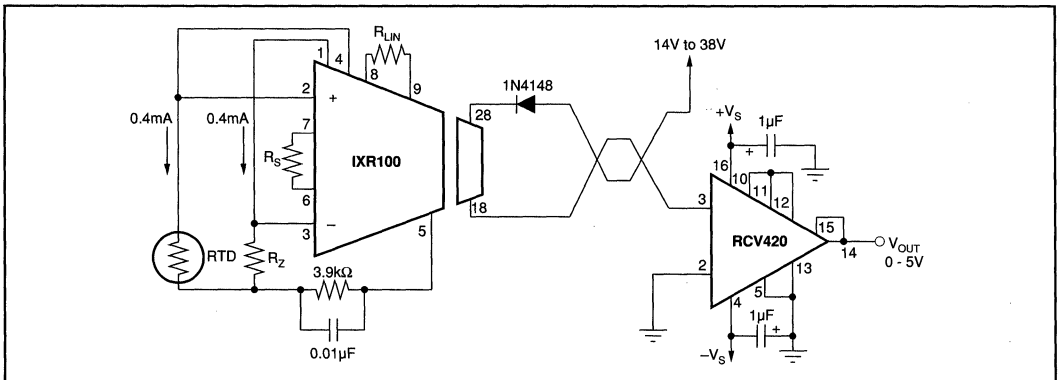


FIGURE 14. Isolated 4-20mA Instrument Loop.

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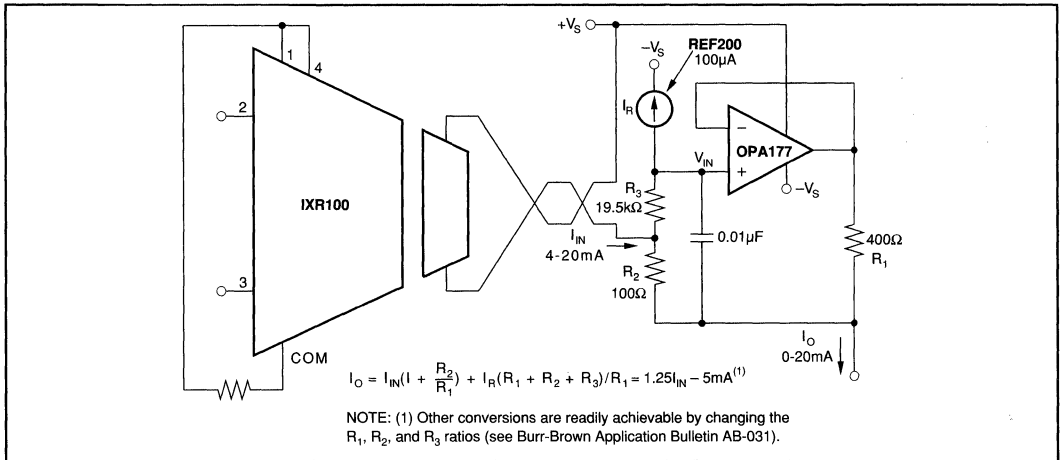
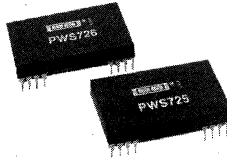


FIGURE 15. 4-20mA to 0-20mA Output Converter.

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PWS725A
PWS726A

Isolated, Unregulated DC/DC CONVERTERS

FEATURES

- ISOLATED ± 7 TO ± 18 VDC OUTPUT FROM SINGLE 7 TO 18VDC SUPPLY
- ± 15 mA OUTPUT AT RATED VOLTAGE ACCURACY
- HIGH ISOLATION VOLTAGE
PWS725A, 1500Vrms
PWS726A, 3500Vrms
- LOW LEAKAGE CAPACITANCE: 9pF
- LOW LEAKAGE CURRENT: 2 μ A max, at 240VAC 50/60Hz
- HIGH RELIABILITY DESIGN
- AVAILABLE WITH OUTPUT SYNCHRONIZATION SIGNAL FOR USE WITH ISO120 AND ISO121

- PROTECTED AGAINST OUTPUT FAULTS
- COMPACT
- LOW COST
- EASY TO APPLY—FEW EXTERNAL PARTS

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS EQUIPMENT
- TEST EQUIPMENT
- DATA ACQUISITION

DESCRIPTION

The PWS725A and PWS726A convert a single 7 to 18VDC input to bipolar voltages of the same value as the input voltage. The converters are capable of providing ± 15 mA at rated voltage accuracy and up to ± 40 mA without damage. (See Output Current Rating.)

The PWS725A and PWS726A converters provide reliable, engineered solutions where isolated power is required in critical applications. The high isolation voltage rating is achieved through use of a specially-designed transformer and physical spacing. An additional high dielectric-strength, low leakage transformer coating increases the isolation rating of the PWS726A.

Reliability and performance are designed in. The bifilar wound, wirebonded transformer simultaneously provides lower output ripple than competing designs, and a higher performance/cost ratio. The soft-start oscillator/driver design assures full operation of the

oscillator before either MOSFET driver turns on, protects the switches, and eliminates high inrush currents during turn-on. Input current sensing protects both the converter and the load from possible thermal damage during a fault condition.

Special design features make these converters especially easy to apply. The compact size allows dense circuit layout while maintaining critical isolation requirements. The Input Sync connection allows frequency synchronization of multiple converters. The Output Sync is available to synchronize ISO120 and ISO121 isolation amplifiers. The Enable input allows control over output power in instances where shutdown is desired to conserve power, such as in battery-powered equipment, or where sequencing of power turn-on/turn-off is desired.

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SPECIFICATIONS

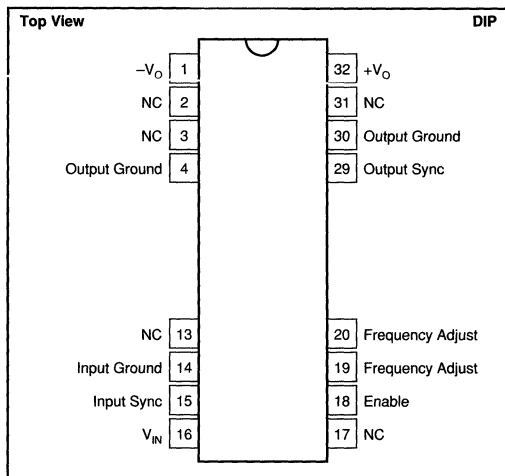
ELECTRICAL

$T_A = +25^{\circ}\text{C}$, $C_1 = 1\mu\text{F}$ ceramic, $V_{IN} = 15\text{VDC}$, operating frequency = 800kHz, $V_{OUT} = \pm 15\text{VDC}$, $C_{IN} = 1\mu\text{F}$ ceramic, $I_{OUT} = \pm 15\text{mA}$, unless otherwise specified.

PARAMETER	CONDITIONS	PWS725A			PSW726A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT									
Rated Voltage	$I_O = \pm 15\text{mA}$ No External Filtering L-C Input Filter, $L_{IN} = 100\mu\text{H}$, $C_{IN} = 1\mu\text{F}^{(1)}$ C Only, $C_{IN} = 1\mu\text{F}$	7	15	18	*	*	*	VDC	
Input Voltage Range								VDC	
Input Current				77					mA
Input Current Ripple				150					mAp-p
				5					mAp-p
			60					mAp-p	
ISOLATION									
Test Voltages	Input to Output, 10 seconds Input to Output, 60 seconds, min Input to Output, Continuous, AC 60Hz Input to Output, Continuous DC Input to Output Input to Output, 240Vrms, 60Hz	4000			8000			VDC	
Rated Voltage			1500			3500			Vrms
					1500			3500	Vrms
Isolation Impedance					2121				VDC
								4950	VDC
Leakage Current			$10^{12} \parallel 9$			*	*	$\Omega \parallel \mu\text{F}$	
			1.2	2.0		*	*	μA	
OUTPUT									
Rated Output Voltage	Balanced Loads Single-Ended Balanced Loads, $\pm 10\text{mA} < I_{OUT} < \pm 40\text{mA}$ No External Capacitor $L_O = 10\mu\text{H}$, $C_O = 1\mu\text{F}$ (Figure 1) $L_O = 0\mu\text{H}$, C_O Filter Only $L_O = 10\mu\text{H}$, $C_O = 1\mu\text{F}$ $L_O = 100\mu\text{H}$, C Filter C Filter Only	14.25	15	15.75	*	*	*	VDC	
Output Current				15	40			*	mA
					80			*	mA
Load Regulation					0.4			*	%/mA
								*	%/mA
Ripple Voltage (400kHz)				60				*	mVp-p
				10				*	mVp-p
						See Performance Curves			
Output Switching Noise				1			*	*	mVp-p
Output Capacitive Load					10			*	μF
					1			*	μF
Output Sync Signal							*	*	μF
Output Sync Signal		Square Wave, 50% Duty Cycle		0.04				*	%
				1.15				*	V/V
Output Voltage Temp. Coefficient				10				*	mV/ $^{\circ}\text{C}$
Output Sync Signal			30			*	*	Vp-p	
TEMPERATURE									
Specification		-25		+85	*		*	$^{\circ}\text{C}$	
Operating		-25		+85	*		*	$^{\circ}\text{C}$	
Storage		-25		+125	*		*	$^{\circ}\text{C}$	

* Specification same as PWS725A.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PWS725A	32-Pin Ceramic DIP	210
PSW726A	32-Pin Ceramic DIP	210

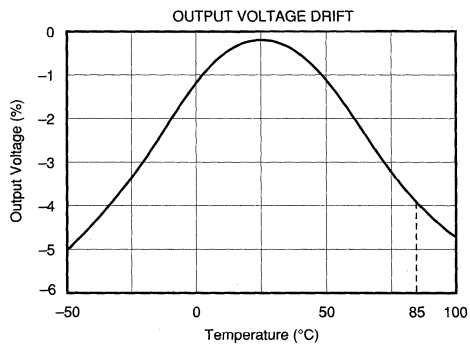
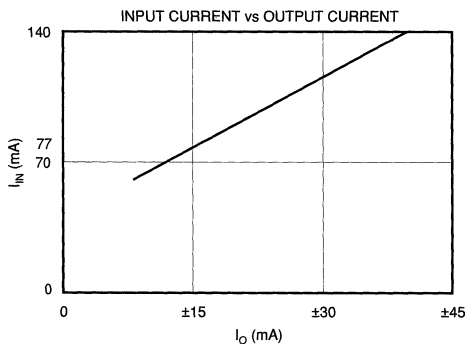
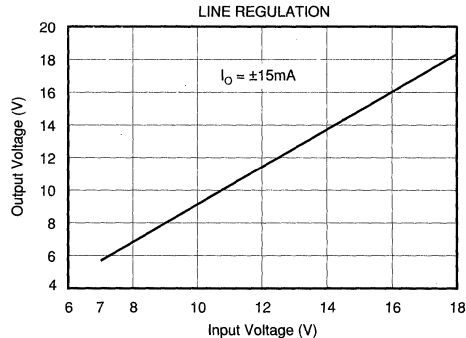
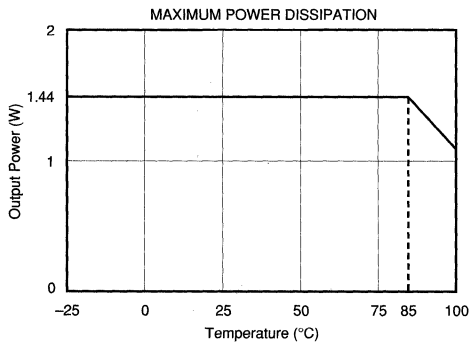
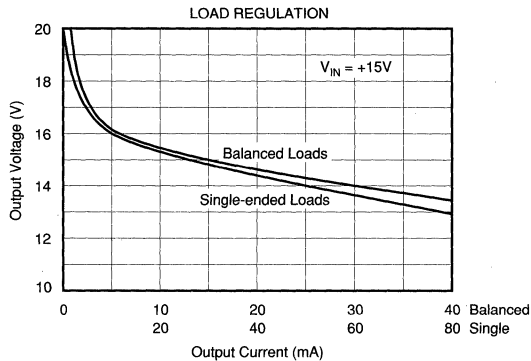
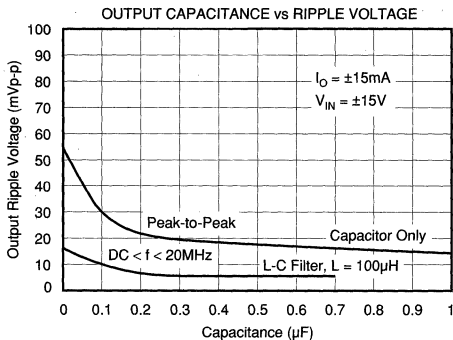
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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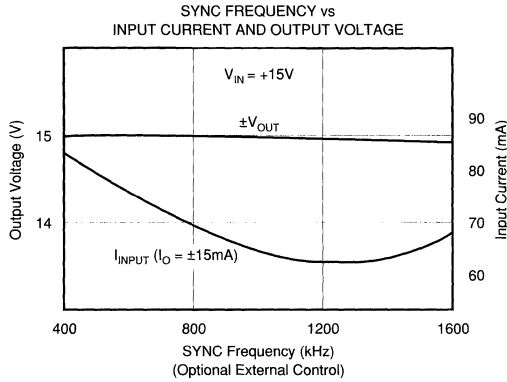
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



THEORY OF OPERATION

The PWS725A and the PWS726A DC/DC converters consist of a free-running oscillator, control and switch driver circuitry, MOSFET switches, a transformer, a bridge rectifier, and filter capacitors together in a 32-pin DIP (0.900 inches nominal) package. The control circuitry consists of current limiting, soft start, frequency adjust, enable, and synchronization features. See Figure 1. In instances where several converters are used in a system, beat frequencies developed between the converters are a potential source of low frequency noise in the supply and ground paths. This noise may couple into signal paths. See Figures 2 and 3 for connection of INPUT SYNC pin. Converters can be syn-

chronized and these beat frequencies avoided. The unit with the highest natural frequency will determine the synchronized running frequency. To avoid excess stray capacitance, the INPUT SYNC pin should not be loaded with more than 50pF. If unused, the INPUT SYNC must be left open.

Soft start circuitry protects the MOSFET switches during start up. This is accomplished by holding the gate-to-source voltage of both MOSFET switches low until the free-running oscillator is fully operational. In addition to that soft start circuitry, input current sensing also protects the MOSFET switches. This current limiting keeps the FET

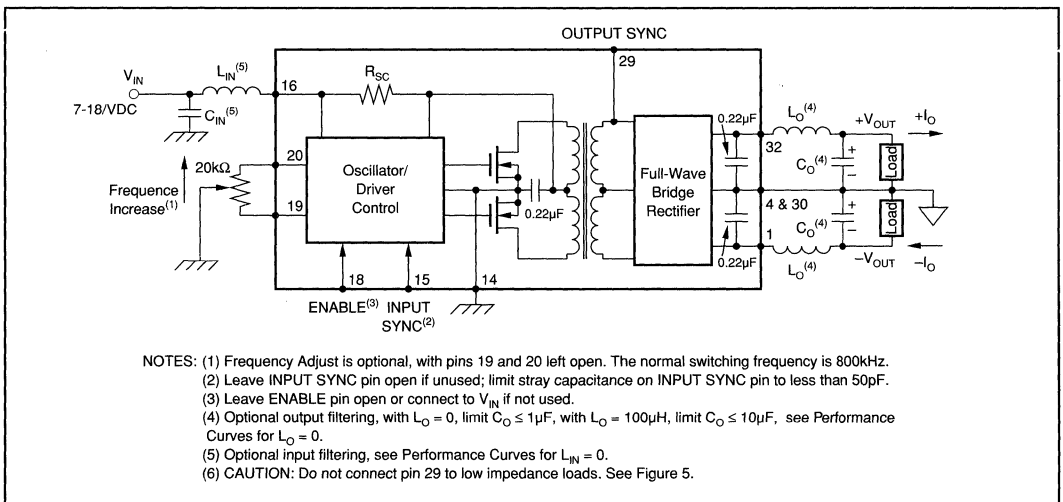


FIGURE 1. PWS725A/726A Functional Diagram.

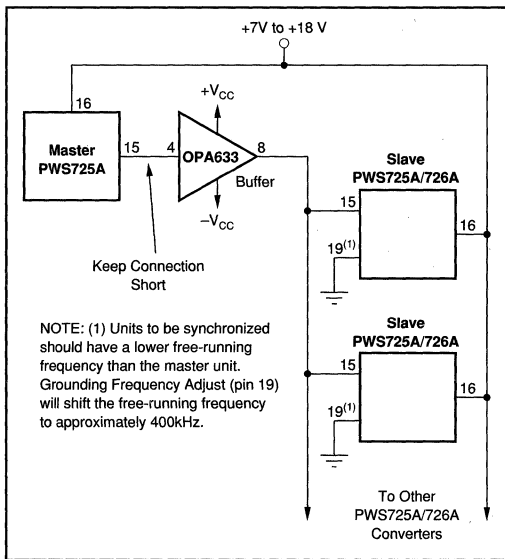


FIGURE 2. Synchronization of Multiple PWS725As or PWS726As from a Master Converter.

switches operating in their safe operating area under fault conditions or excessive loads. When either of these conditions occur, the peak input current exceeds a safe limit. The result is an approximate 5% duty cycle, 300 μ s drive period to the MOSFET switches. This protects the internal MOSFET switches as well as the external load from any thermal damage. When the fault or excessive load is removed, the converter resumes normal operation. A delay period of approximately 50 μ s incorporated in the current sensing circuitry allows the output filter capacitors to fully charge after a fault is removed. This delay period corresponds to a filter capacitance of no more than 1 μ F at either of the output pins. This provides full protection of the MOSFET switches and also sufficiently filters the output ripple voltage (see specification table). The current sensing circuitry is designed to provide thermal protection for the MOSFET switches over the operating temperature range as well. The low thermal resistance for the package ($\theta_{JC} = 10^{\circ}\text{C}/\text{W}$) ensures safe operation under rated conditions. When these rated conditions are exceeded, the unit will go into its shutdown mode.

An optional potentiometer can be connected between the two FREQUENCY ADJUST pins to trim the oscillator operating frequency $\pm 10\%$ (see Figure 4). Care should be taken when trimming the frequency near the low frequency range. If the frequency is trimmed too low, the peak inductive currents in the primary will trip the input current sensing circuitry to protect the MOSFET switches from these peak inductive currents.

The ENABLE pin allows external control of output power. When this pin is pulled low, output power is disabled. Logic thresholds are TTL compatible. When not used, the Enable input may be left open or tied to V_{IN} (pin 16).

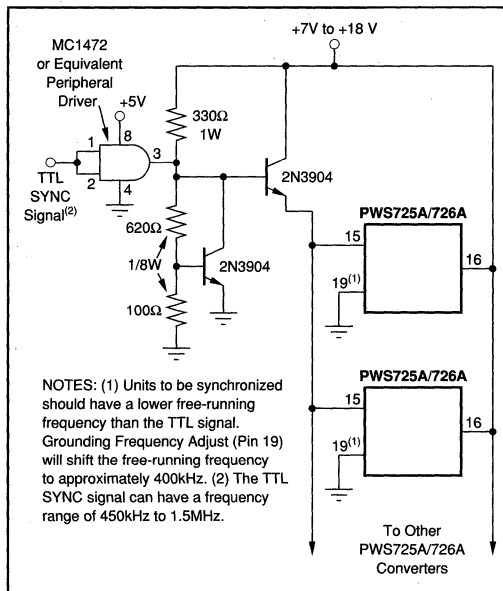


FIGURE 3. Synchronization of Multiple PWS725As or PWS726As from an External TTL Signal.

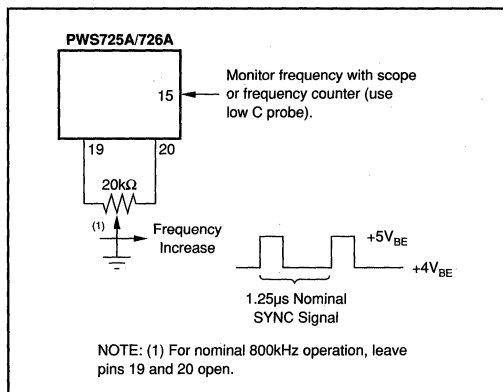


FIGURE 4. Frequency Adjustment Procedure.

OUTPUT CURRENT RATING

The total current which can be drawn from the PWS725A or PWS726A is a function of total power being drawn from both outputs (see Functional Diagram). If one output is not used, then maximum current can be drawn from the other output. If both outputs are loaded, the total current must be limited such that:

$$I_{L+} + I_{L-} \leq 80\text{mA}$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negatives supplies. For example, an operational amplifier may draw 13mA from the positive supply under

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full load while drawing only 3mA from the negative supply. Under these conditions, the PWS725A/726A could supply power for up to five devices ($80\text{mA} \div 16\text{mA} \approx 5$). Thus, the PWS725A/726A can power more circuits than is at first apparent.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: $V_{DC\text{TEST}} = (2 \times V_{AC\text{rms CONTINUOUS RATING}}) + 1000\text{V}$ for ten seconds. This choice is appropriate for conditions where system transient voltages are not well defined.⁽¹⁾ Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

NOTE: (1) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

OUTPUT SYNC SIGNAL

To allow synchronization of an ISO120 or ISO121 isolation amplifier, the PWS725A and PWS726A have an OUTPUT SYNC signal at pin 29. It should be connected as shown in Figure 5 to keep capacitive loading of pin 29 to a minimum. If output sync is not used, leave pin open.

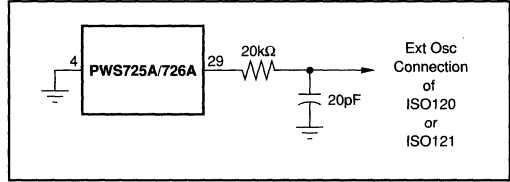


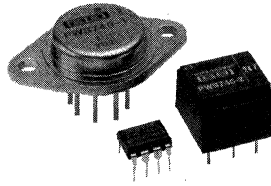
FIGURE 5. Synchronization with ISO120 or ISO121 Isolation Amplifier.

PWS725A/726A

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ISOLATION PRODUCTS

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PWS740

Distributed Multichannel Isolated DC-TO-DC CONVERTER

FEATURES

- ISOLATED ± 7 TO ± 20 VDC OUTPUTS
- BARRIER 100% TESTED AT 1500VAC, 60Hz
- LOWEST POSSIBLE COST PER CHANNEL
- MINIMUM PC BOARD SPACE
- 80% EFFICIENCY (8 CHANNELS, RATED LOADS)
- FLEXIBLE USE WITH PWS745 COMPONENTS

DESCRIPTION

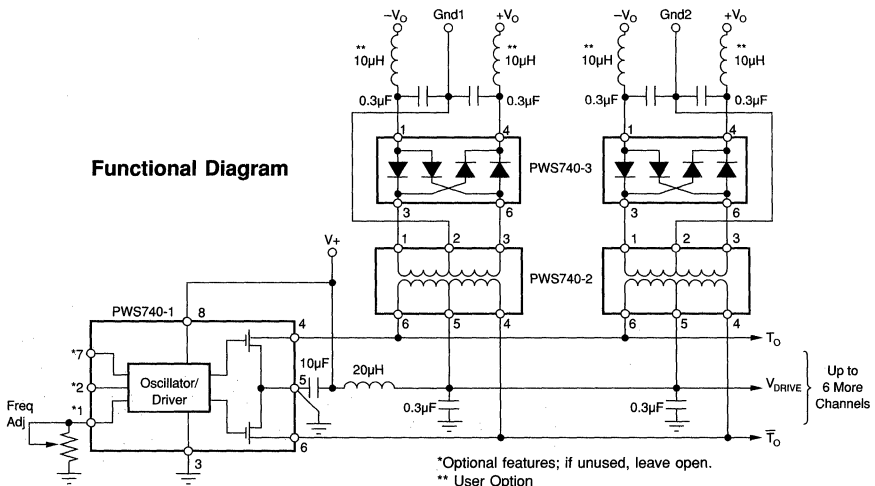
The PWS740 is a multichannel, isolated DC-to-DC converter with a 1500VAC continuous isolation rating. The outputs track the input voltage to the converter over the range of 7 to 20VDC. The converter's modular design, comprising three components, minimizes the cost of isolated multichannel power for the user.

APPLICATIONS

- INDUSTRIAL MEASUREMENT AND CONTROL
- DATA ACQUISITION SYSTEMS
- TEST EQUIPMENT

The PWS740-1 is a high-frequency (400kHz nominal) oscillator/driver, handling up to eight channels. This part is a hybrid containing an oscillator and two power FETs. It is supplied in a TO-3 case to provide the power dissipation necessary at full load. Transformer impedance limits the maximum input current to about 700mA at 15V input, well within the unit's thermal limits. A TTL-compatible ENABLE pin provides output shut-down if desired. A SYNC pin allows synchronization of several PWS740-1s.

The PWS740-2 is a trifilar-wound isolation transformer using a ferrite core and is encapsulated in a plastic package, allowing a higher isolation voltage rating. The PWS740-3 is a high-speed rectifier bridge in a plastic 8-pin mini-DIP package. One PWS740-2 and one PWS740-3 are used per isolated channel.



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SPECIFICATIONS

ELECTRICAL

$V_{IN} = 15V$, output load on each of 8 channels = $\pm 15mA$, $T_A = +25^\circ C$ unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
PWS740 SYSTEM					
ISOLATION					
Rated Voltage	Continuous, AC, 50/60Hz Continuous, DC			1500 2121	VACrms VDC
Test Voltage	10s, minimum	4000	$10^{12} \parallel 3$		VACrms
Impedance	Measured from Pin 2 to Pin 5 of the PWS740-2		0.5	1.5	$\Omega \parallel pF$
Leakage Current	240VACrms, 60Hz Per Channel				μA
INPUT					
Rated Voltage			15		VDC
Voltage Range		7		20	VDC
Current	$\pm 30mA$ Output Load on 8 Channels, $V_{IN} = 15V$ Rated Output Load on 8 Channels, $V_{IN} = 15V$		520 300		mA mA
Current Ripple	Full Output Load on 8 Channels, $V_{IN} = 15V$ with π Filter on Input		1		mA
OUTPUT					
Rated Voltage	$\pm 15mA$ Output Load on 8 Channels	14	15	16	VDC
Voltage at Min Load	$\pm 1mA$ /Channel		30		VDC
Voltage Range	$\pm 15mA$ Output Load on Each Channel	± 7		± 20	VDC
V_{OUT} vs Temp	$\pm 15mA$ Output Load on Each Channel		± 0.05		$V/^\circ C$
Load Regulation	$\pm 3mA < \text{Output Load} < \pm 30mA$		0.25		V/mA
Tracking Regulation	V_{OUT}/V_{IN}		1.2		V/V
Ripple Voltage	See Typical Performance Curves				
Noise Voltage	See Theory of Operation				
Current $ +I_{OUT} + -I_{OUT} $	Each Channel			60	mA
TEMPERATURE					
Specification		-25		+85	$^\circ C$
Operation		-25		+85	$^\circ C$
PWS740-1 OSCILLATOR/DRIVER					
Frequency	$V_{IN} = 15V$	350	400	470	kHz
Supply		7	15	20	V
Enable	Drivers On	2		V_S	V
	Drivers Off	0		0.8	V
PWS740-2 ISOLATION TRANSFORMER					
Isolation Test Voltage	10s, minimum	4000			VACrms
Rated Isolation Voltage	60s, minimum	1500			VACrms
Isolation Impedance	Continuous			1500	VACrms
Isolation Leakage	240VAC		$10^{12} \parallel 3$		$\Omega \parallel pF$
Primary Inductance	400kHz, Pin 1 to Pin 5		0.5	1.5	μA
Winding Ratio	Primary/Secondary		300		μH
			68/76		
PWS740-3 DIODE BRIDGE					
Reverse Recovery	$I_F = I_R = 50mA$		40		ns
Reverse Breakdown	$I_R = 100\mu A$	55			V
Reverse Current	$V_R = 40V$			1.5	μA
Forward Voltage	$I_F = 100mA$			1.6	V

PWS740

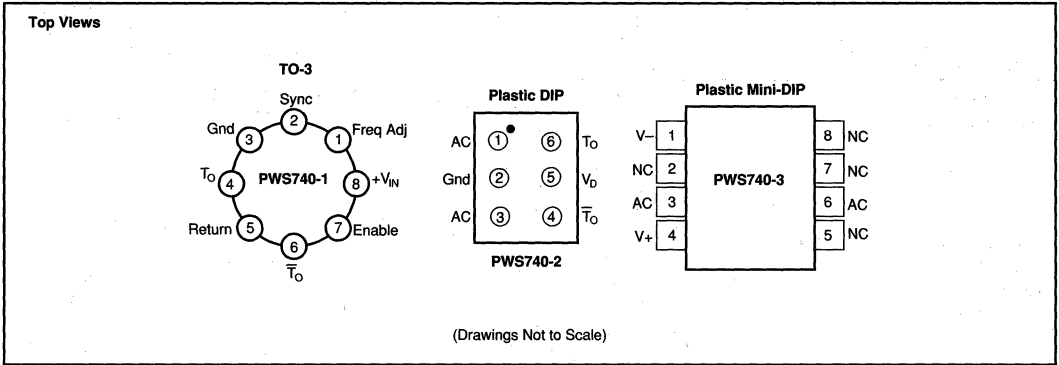
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ISOLATION PRODUCTS

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PIN CONFIGURATION



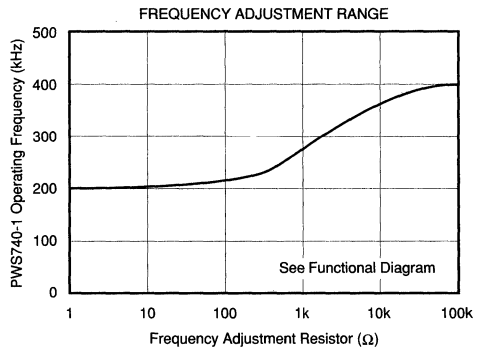
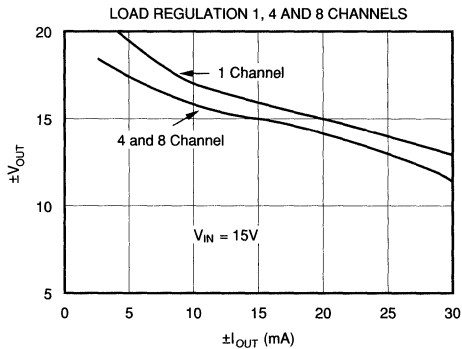
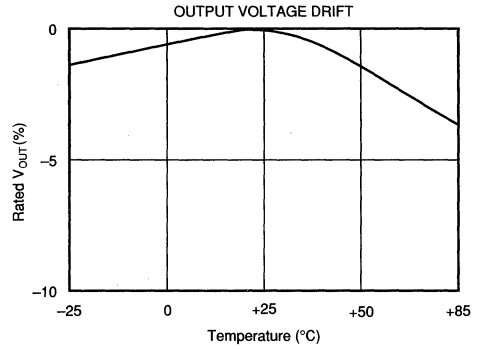
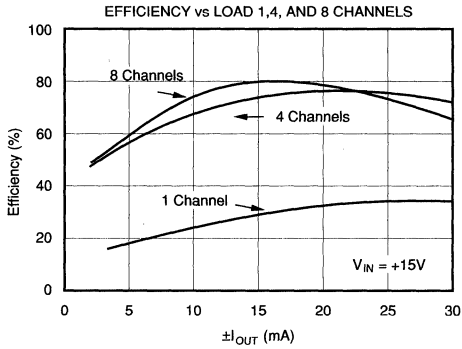
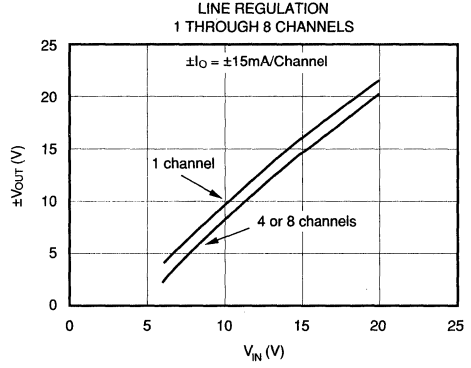
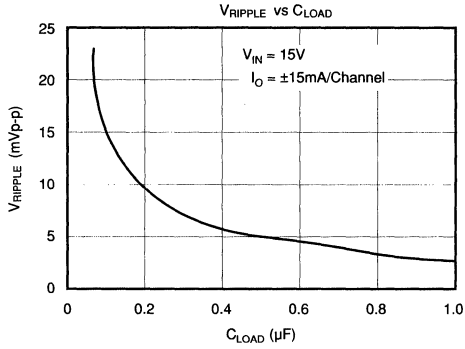
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PWS740-1 Driver	TO-3	030
PWS740-2 Transformer	6-Pin Plastic DIP	216
PWS740-3 Rectifier	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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TYPICAL PERFORMANCE CURVES



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN DESCRIPTIONS OF PWS740-1 DRIVER

+V_{IN}, RETURN, AND GND

These are the power supply pins. The ground connection, RETURN, for the N-channel MOSFET sources is brought out separately from the ground connection for the oscillator/driver chip. The waveform of the FETs' ground return current (and also the current in the V_{DRIVE} line) is an 800kHz sawtooth. A capacitor between +V_{IN} and the FET ground provides a bypass for the AC portion of this current.

The power should never be instantaneously interrupted to the PWS740 system (i.e., a break in the line from V+, either accidental or by means of a series switch). Normal power-down of the V+ supply is not considered instantaneous. Should a rapid break in input power occur, however, the transformers' voltage will rapidly increase to maintain current flow. Such a voltage spike may damage the PWS740-1. The bypass capacitors at the +V_{IN} pin of the PWS740-1 and the V_{DRIVE} pins of the transformers provide a path for the primary current if power is interrupted; however, total protection requires some type of bidirectional 1A voltage clamping at the +V_{IN} pin. A low cost SA20A TransZorb® from General Semiconductor⁽¹⁾ or equivalent, which will clamp the +V_{IN} pin between -0.6V and +23V, is recommended.

T_O AND \bar{T}_O

These pins are the drains of the N-channel MOSFET switches which drive all the transformer primaries in parallel. The signals on these pins are 400kHz complementary square waves with twice the amplitude of the voltage at +V_{IN}. It is these lines that allow the power to be distributed to the individual high voltage isolation transformers. Without proper printed circuit board layout techniques, these lines could generate interference to analog circuits. See the next section on PCB layout.

ENABLE

A high TTL logic level on this pin activates the MOSFET driver circuitry. A low TTL level applied to the ENABLE pin shuts down all drive to the transformers and the output voltages go to zero (only the oscillator is unaffected). For continuous operation, the ENABLE pin can be left open or tied to a voltage between +2V and +V.

SYNCHRONIZATION

The SYNC pin is used to synchronize up to eight PWS740-1 oscillators. Synchronization is useful to prevent beat frequencies in the supply voltages. The SYNC pins of two or more PWS740-1s are tied together to force all units to the same frequency of oscillation. The resultant frequency is slightly higher than that of the highest unsynchronized unit. If this feature is not required, leave the SYNC pin open. The SYNC pin is sensitive to capacitance loading. 150pF or less is recommended. Also external parasitic capacitive feedback between either T_O and the SYNC pin can cause unstable operation (commonly seen as jitter in the T_O outputs). Keep SYNC connections and T_O lines as physically isolated as possible. Avoid shorting the SYNC pin directly to ground or supply potentials; otherwise, damage may result.

Figure 1 shows a method for synchronizing a greater number of PWS740-1 drivers. One unit is chosen as the master. Its synchronization signal, buffered by a high-speed unity gain amplifier can synchronize up to 20 slave units. Pin 1 of each slave unit must be grounded to assure synchronization. Minimize capacitive coupling between the buffered sync line and the outputs of the drivers, especially at the end of long lines. Capacitance to ground is not critical, but total stray capacitance between the sync line and switching outputs should be kept below 50pF. Where extreme line lengths are needed, such as between printed circuit boards, additional OPA633 buffers may be added to keep drive impedance at an acceptably low value. Because of temperature-influenced shifts in the switching levels, best operation of this circuit will occur when differences in ambient temperatures between the PWS740-1 drivers are minimized, typically within a 35°C range.

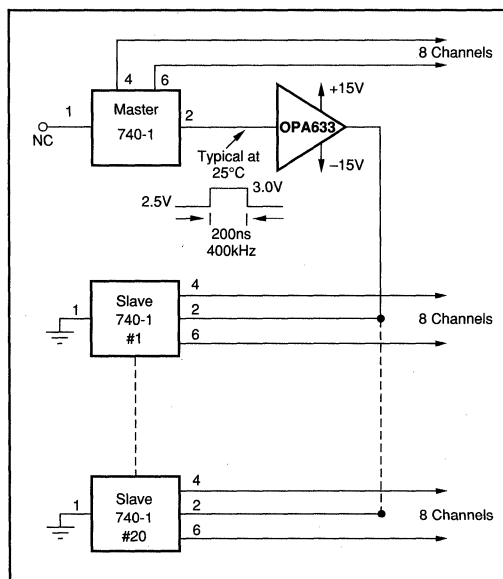


FIGURE 1. Master/Slave Synchronization of Multiple PWS740 Drivers.

(1) General Semiconductor Industries Inc., 2001 W. 10th Place, Tempe AZ 85281, 602-968-3101.

TransZorb® General Semiconductor Industries Inc.

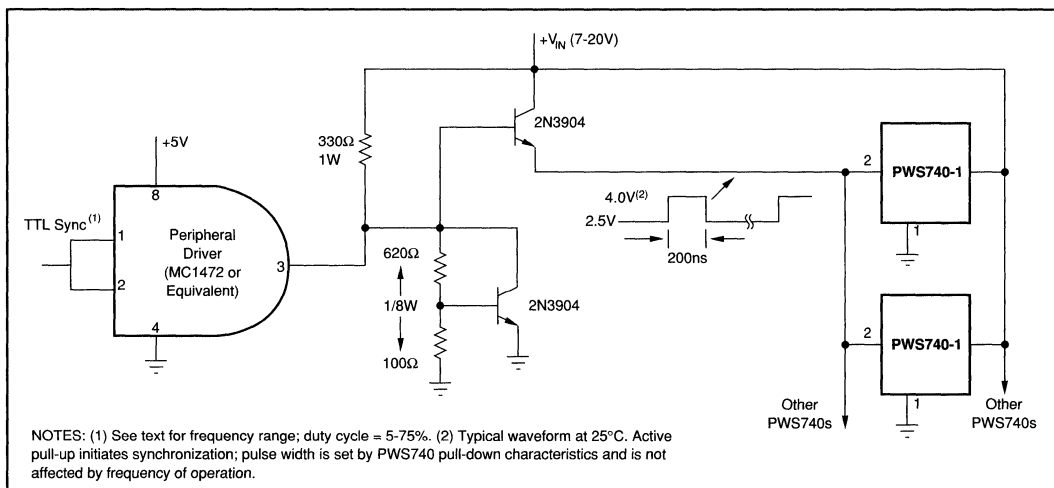


FIGURE 2. External Synchronization of Multiple PWS740 Drivers with TTL-Level Signals.

If larger temperature gradients are likely to occur, the user may wish to consider the synchronization method shown in Figure 2. This circuit is driven from an external TTL-compatible source such as a system clock or a simple free-running oscillator constructed of TTL gates. The output stage provides temperature compensation over the rated temperature range of the PWS740. The signal source frequency should be about 800kHz for rated performance, but may range from 500kHz to 2MHz with slightly reduced performance. Precautions with regard to circuit coupling and layout are the same as for the circuit of Figure 1. Repeaters using the OPA633 may be used for long line lengths. Symmetry and good high-frequency layout practice are important in successful application of both of these synchronization techniques.

FREQUENCY ADJUSTMENT

The **FREQ ADJ** pin may be connected to an external potentiometer to lower an unsynchronized PWS740-1 oscillator frequency. This may be useful if the frequency of the PWS740-1 is too close to some other signal's frequency in the system and beat interference is possible. See Typical Performance Curves. Use of this pin is not usually required; if not used, leave open for rated performance.

THEORY OF OPERATION

EXTERNAL FILTER COMPONENTS

Filter components are necessary to reduce the input ripple current and the output voltage noise. Without any input filtering, the sawtooth currents in the FET switches would flow in the +V supply line. Since this AC current can be as great as 1A peak, voltage interference with other components using this supply line would likely occur. The input ripple current can be reduced to approximately 1mA peak

with the addition of two components—a bypass capacitor between the +V_{IN} pin and ground, and a series inductor in the V_{DRIVE} line. A 10μF tantalum capacitor is adequate for bypass. A parallel 0.33μF ceramic capacitor will extend the bandwidth of the tantalum. Additional bypass capacitors at each primary center-tap of the transformers are recommended. In general, the higher the capacitance, the lower the ripple, but the parasitic series inductance of the bypass capacitors will eventually be the limiting factor. The inductor value recommended is approximately 20μH. Greater reduction in ripple current is achieved with values up to 100μH; then physical size may become a concern. The inductor should be rated for at least 2A and its DC resistance should be less than 0.1Ω. An example of a low cost inductor is part number 51591 from Pulse Engineering⁽²⁾.

Output voltage filtering is achieved with a 0.33μF capacitor connecting each V_{OUT} pin of the diode bridge to ground. Short leads and close placement of the capacitors to the unit provide optimum high frequency bypassing. The 800kHz output ripple should be below 5mVp-p. Higher frequency noise bursts are also present at the outputs. They coincide with the switch times and are approximately 20mV in amplitude. Inductance of 10μH or less in series with the output loads will significantly reduce the noise as seen by the loads.

PC BOARD LAYOUT CONSIDERATIONS

Multilayer printed circuit boards are recommended for PWS740 systems. Two-layer boards are certainly possible with satisfactory operation; however, three layers provide greater density and better control of interference from the FET switch signals. Should four-layer boards be required for other circuitry, the use of separate layers for power and ground planes, a layer for switching signals, and a layer for analog signals would allow the most straightforward layout for the PWS740 system. The following discussion pertains to a three- or four-layer board layout.

(2) Pulse Engineering, PO Box 12235, San Diego CA 92112, 619-268-2400.

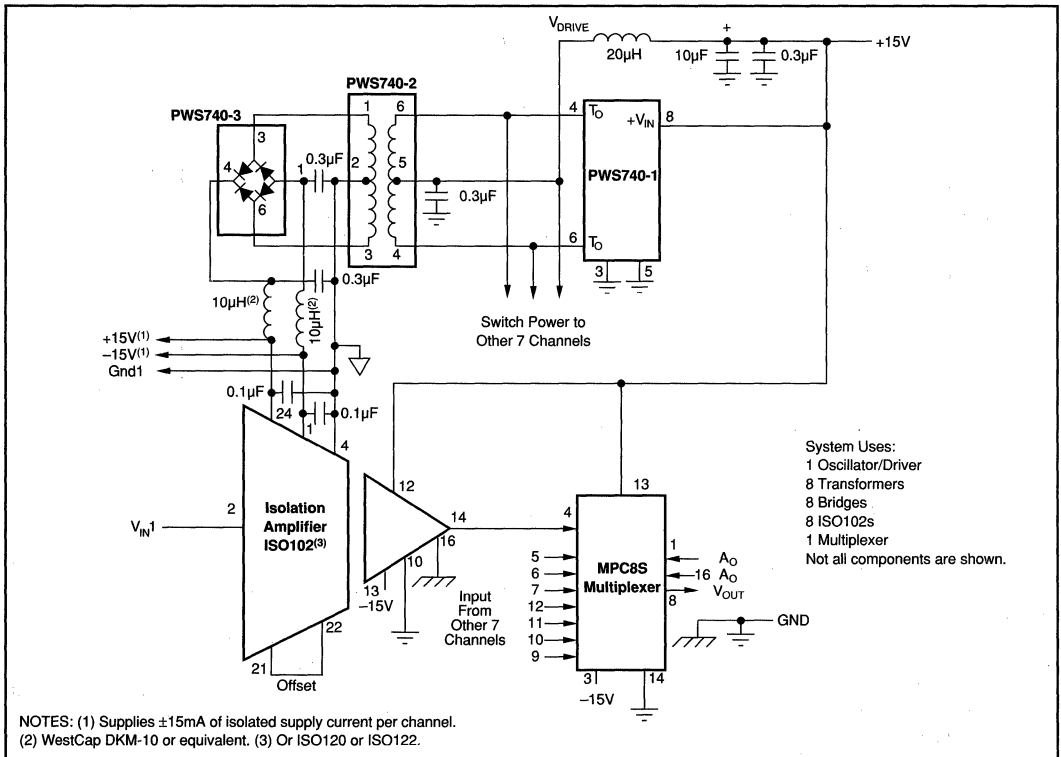


FIGURE 3. Low Cost Eight-Channel Isolation Amplifier Block with Channel-to-Channel Isolation.

Critical consideration should go to minimizing electromagnetic radiation from the switching signal's lines. T_o and \bar{T}_o . You can identify the path of the switching current by starting at the $+V_{IN}$ pin. The dynamic component of the current is supplied primarily from the bypass capacitor. The high frequency current flows through the inductor and down the V_{DRIVE} line, through one side of the transformer windings, returning in the T_o with the "on" FET switch, and then back up through the bypass capacitor. This current path defines a loop antenna which transmits magnetic energy. The magnetic field lines reinforce at the center of the loop, while the field lines reinforce at the center of the loop, while the field lines from opposite points of the loop oppose each other outside the loop. Cancellation of magnetic radiation occurs when the loop is collapsed to two tightly spaced parallel line segments, each carrying the same current in opposite directions. For this reason, the printed circuit traces for both T_o connections should lay directly over a power plane forming the V_{DRIVE} connection. This plane need not extend much wider than T_o and \bar{T}_o . All of the current in the plane will flow directly under the T_o traces because this is the path of least inductance (and least radiation).

Another potential problem with the T_o lines is electric field radiation. Fortunately, the V_{DRIVE} plane is effective at terminating most of the field lines because of its proximity to

these lines. Additional shielding can be obtained by running ground trace(s) along the T_o lines, which also facilitate minimum loop area connections for the transformer's center tap bypass capacitors.

The connections between the secondary (output side) of the transformer and the diode bridges should be kept as short as possible. Unnecessary stray capacitance on these lines could cause tuned circuit peaking to occur, resulting in a slight increase of output voltage.

The PWS740 is intended for use with the ISO102, ISO120 or ISO122 isolation amplifiers (see Figure 3). Place the PWS740-2 transformer on the V_{OUT} side of the buffer rather than on the C_1 (bandwidth control) side to prevent possible pickup of switch signal by the ISO102.

The best ground connection ties the ISO102 output analog common pin to the PWS740-1 ground pin with a ground plane. This is where a four-layer board design becomes convenient. The digital ground of the ISO102 can be connected to the ground plane or closer to the +V supply. If possible, you should include the analog components that the ISO102 drives on the same board. For example, if several ISO102s are multiplexed to an analog/digital converter, then having all components sharing the same ground plane will significantly simplify ground errors. Avoid connecting digi-

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tal ground and the PWS740 ground together locally, leaving the ISO102 analog ground to be connected off of the board; the differential voltage between analog and digital ground may become too great.

OUTPUT CURRENT RATINGS

The PWS740-1 driver contains “soft-start” driver circuitry to protect the driver FETs and eliminate high inrush currents during turn-on. Because the PWS740 can have between one and eight channels connected, it was not possible to provide a suitable internal current limit within the driver. Instead, impedance-limiting protects the driver and transformer from overload. This means that the internal impedance of each PWS740-2 transformer is high enough that, when short-circuited at its output, it limits the current drawn from the driver to a safe value. In addition, the wire size and mass of the transformer are large enough that the transformer does not receive damage under continuous short-circuit conditions.

The PWS740-1 is capable of driving up to eight individual channels to their full current rating. The total current which can be drawn from each isolation channel is a function of total power being drawn from both DC V+ and V- outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases, the maximum total current that can be drawn from any individual channel is:

$$|I_{L+}| + |I_{L-}| \leq 60\text{mA}$$

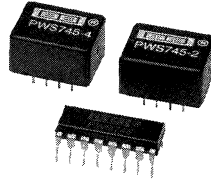
It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. Thus, the PWS740 can power more circuits per channel than is first apparent. For example, an operational amplifier does not draw maximum current from both supplies simultaneously. If a circuit draws 10mA from the positive supply and 3mA from the negative supply, the PWS740 could power $(60 \div 13)$, about four devices per channel.

ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter period of time. The relationship between actual test conditions and the continuous derated maximum specification is an important one. Burr-Brown has chosen a deliberately conservative one: $V_{\text{TEST}} = (2 \times V_{\text{CONTINUOUS RATING}}) + 1000\text{V}$. This choice is appropriate for conditions where system transient voltages are not well defined.⁽³⁾ Where the real voltages are well-defined or where the isolation voltage is not continuous, the user may choose a less conservative derating to establish a specification from the test voltage.

⁽³⁾ Reference National Electrical Manufacturers Association (NEMA) Standards part ICS 1-109 and ICS1-111.

For Immediate Assistance, Contact Your Local Salesperson



PWS745

Multi-Channel Isolated DC/DC CONVERTER COMPONENTS

FEATURES

- COMPACT SIZE
- LOW COST PER CHANNEL
- DRIVES UP TO 8 CHANNELS
- 750/1500VAC ISOLATION
- FLEXIBLE USE WITH PWS740/PWS750 COMPONENTS
- 0.4 IN. MAXIMUM MOUNTING HEIGHT

APPLICATIONS

- INDUSTRIAL CONTROL
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- POINT-OF-USE POWER CONVERSION
- 5V TO $\pm 15V$ FROM DIGITAL SUPPLIES

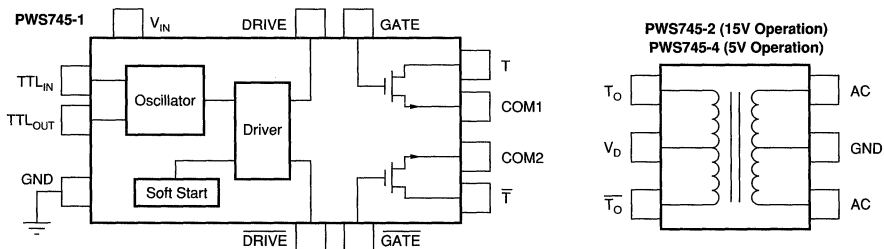
DESCRIPTION

The PWS745 is a set of components useful in the construction of single or multi-channel isolated DC/DC converters. By themselves, or in combination with the PWS740 and PWS750 families of components, they allow compact, optimal, and low-cost solutions to many power supply problems.

The PWS745-1 DIP oscillator/driver can be used to drive up to eight channels of independently isolated power. The switching MOSFETs are built into the driver to allow simple low-cost assembly of the multi-channel converter. The PWS745-1 also is capable of operating at 5VDC and can be easily synchronized with TTL level signals. While offering the user an alternative to the TO-3 package of the PWS740, the

PWS745-1 also allows the user to select varying levels of power, isolation voltage, mounting technology and system configuration by choosing among the several component families. For example, the PWS745-1 can directly drive the PWS740, PWS745, or PWS750 transformers. It also can drive the FETs of a PWS750 distributed power system. The operating frequency is compatible with the ISO120 family of isolation amplifiers and is capable of multi-channel synchronized operation to eliminate troublesome beat frequencies.

The PWS745-2 is a 15V to $\pm 15V$ output version, while the PWS745-4 is the 5V to $\pm 15V$ output version. The PWS740-3 high-speed bridge provides a convenient rectifier for the selected transformer output.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $V_{IN} = 15VDC$, Output Load = $\pm 15mA$ (PWS745-2) and $T_A = 25^\circ C$ unless otherwise noted.
 Or $V_{IN} = 5VDC$, Output Load = $\pm 12mA$ (PWS745-4) and $T_A = 25^\circ C$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS745-1 OSCILLATOR/DRIVER					
Frequency: Internal OSC	$TTL_{IN} = 0V$	550	600	650	kHz
External OSC		500	600	1000	kHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
Current	No Load		10		mA
	Max Load		650		mA
Current Ripple	$C_{BYPASS} = 1\mu F$		2.5		mAp-p
TTL_{IN} : I_{IH}				10	nA
I_{IL}			-1		μA
V_{IH}		2			V
V_{IL}				0.8	V
Frequency		1		2	MHz
TTL_{OUT} : I_{OL}				15	mA
Frequency			600		kHz
T, \bar{T} Drive Current				50	mA
T, \bar{T} Drive Voltage: High		3		7	V
Low				0.7	V
PWS745-2					
Voltage, Rated Continuous AC 60Hz	60Hz, 1s	750			Vrms
100% Test ⁽¹⁾		1200			Vrms
Barrier Impedance			$10^{12} \parallel 8$		$\Omega \parallel pF$
Leakage Current at 60Hz	$V_{ISO} = 240Vrms, 60Hz$			150	$\mu Arms$
PWS745-4					
Voltage, Rated Continuous AC 60Hz	60Hz, 1s	750			Vrms
100% Test ⁽¹⁾		1200			Vrms
Barrier Impedance			$10^{12} \parallel 8$		$\Omega \parallel pF$
Leakage Current at 60Hz	$V_{ISO} = 240Vrms, 60Hz$			150	$\mu Arms$
TEMPERATURE RANGE					
Specification		-40		85	$^\circ C$
Operation		-40		85	$^\circ C$
Storage		-40		85	$^\circ C$

NOTES: (1) Tested at 1.6 rated, fail on 5pc partial discharge leakage current on five successive pulses.

PWS745

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ISOLATION PRODUCTS

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Continuous Isolation Voltage	750Vrms
Junction Temperature	150°C
Storage Temperature	85°C
Lead Temperature (soldering, 10s)	300°C
Transformer Output Short to Common	Continuous
Max Load, Sum of All Transformer Outputs	500mA

Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION⁽¹⁾

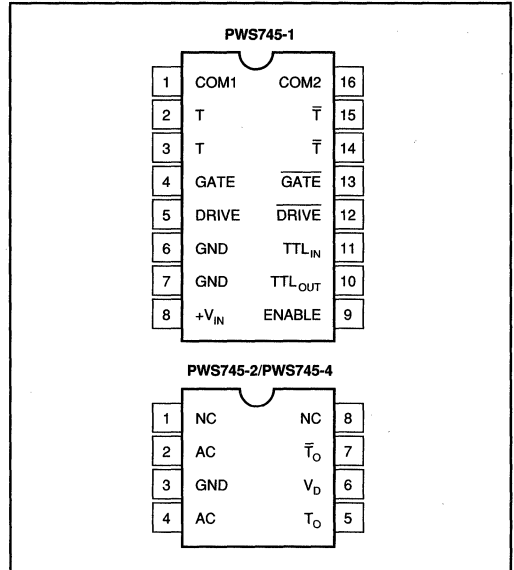
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PWS745-1	16-Pin Plastic DIP	129
PWS745-2	8-Pin Plastic	250
PWS745-4	8-Pin Plastic	250

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

 **ELECTROSTATIC DISCHARGE SENSITIVITY**

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

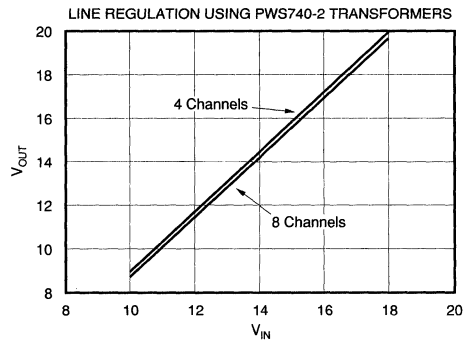
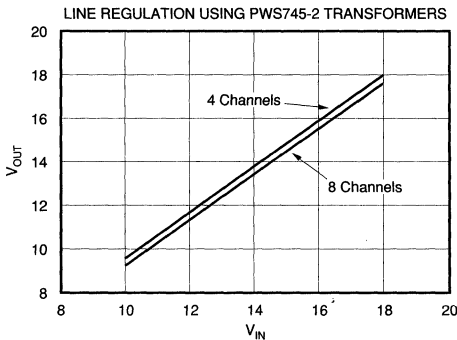
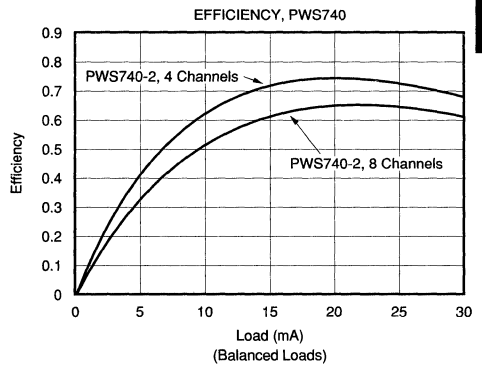
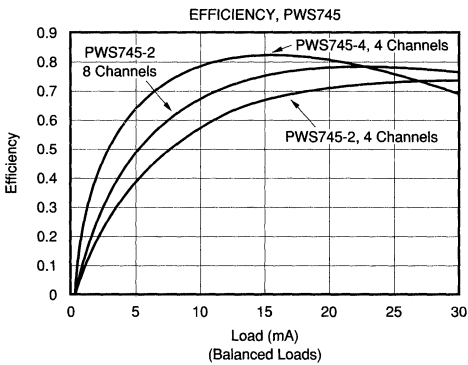
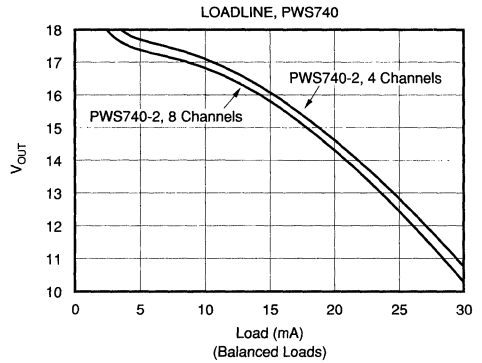
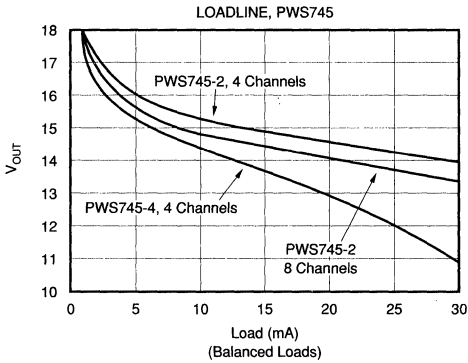
PIN CONFIGURATIONS



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TYPICAL PERFORMANCE CURVES

$T_A = 25^\circ\text{C}$, +15VDC or +5VDC unless otherwise specified.



PWS745

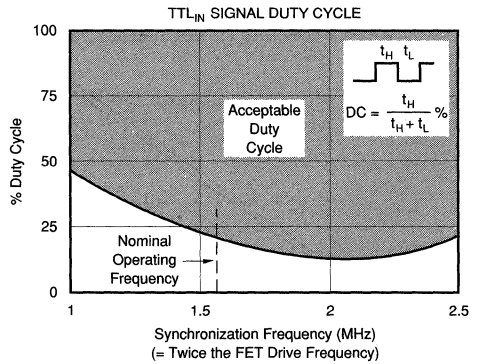
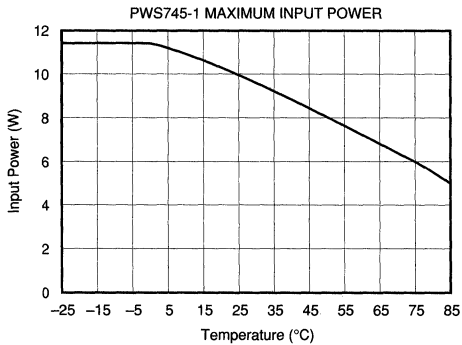
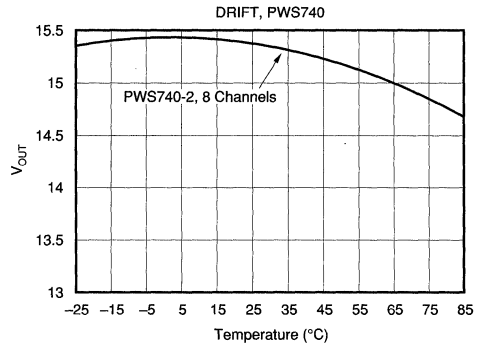
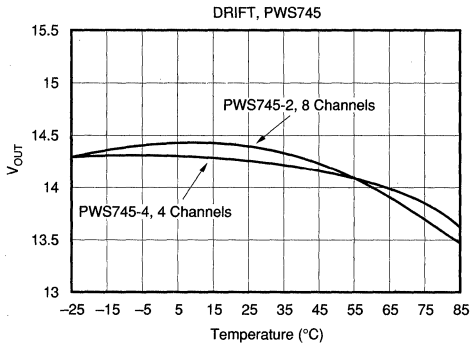
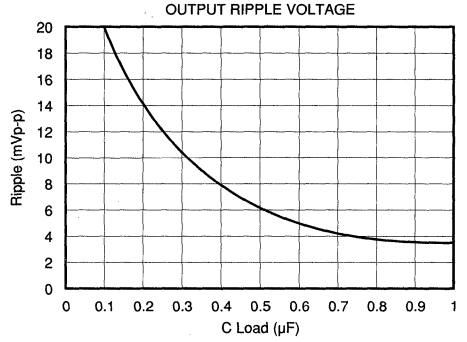
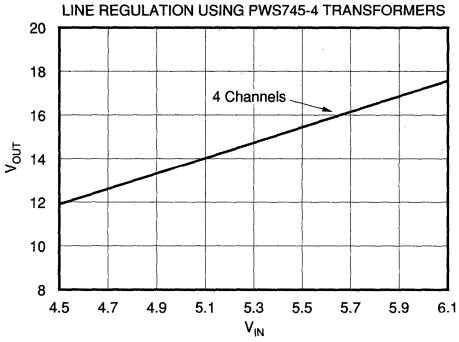
5

ISOLATION PRODUCTS

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = 25^\circ\text{C}$, +15VDC or +5VDC unless otherwise specified.



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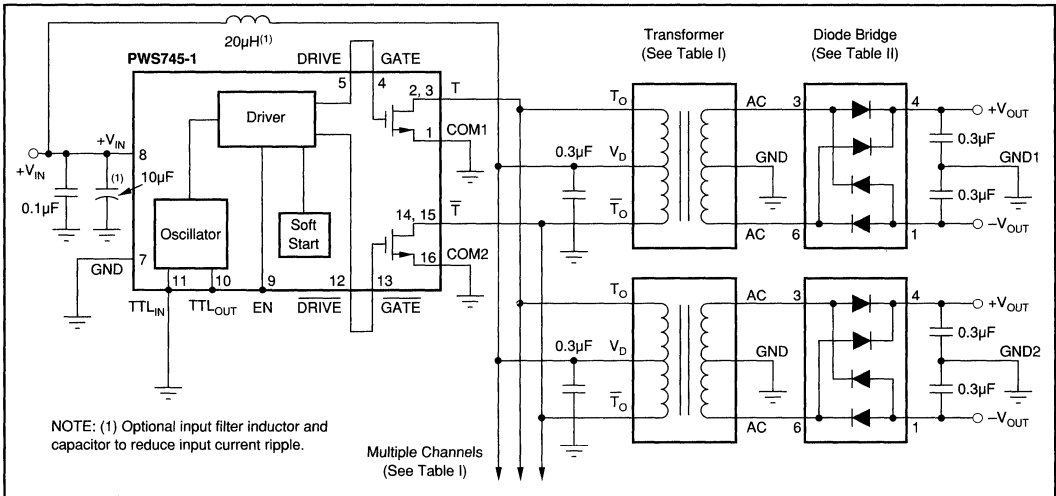


FIGURE 1. Typical Connections.

BASIC OPERATION

The PWS745 components are used to build a multichannel DC/DC converter. The oscillator runs at 600kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage. The PWS745-1 is a power oscillator/switch able to directly drive the primary side of an isolation transformer. The small size of the driver is achieved by using a multiple chip transfer molding process. The power components are mounted directly on the copper leadframe, utilizing two pins directly connected to each die pad to maximize heat sink area. The output of the transformer is rectified with a high speed diode bridge. The PWS740-2 is used when 1500Vrms isolation is required. The PWS745-2 or PWS750-2 is used when 750Vrms isolation is required. With these transformers, the output voltages directly track the input voltage. The PWS745-4 or PWS750-4 is used to step up the input voltage from 5V to $\pm 15V$. Operation at 5V makes it possible to build an isolated system for powering the analog components when only a logic supply is available. Using the PWS745-2 or -4 allows the user 0.5in. PCB spacing. The possible component combinations are summarized in Figure 1 and Tables I and II. The 600kHz operating frequency enables direct synchronization with products such as the ISO120 and ISO121. See Figure 3. The use of synchronization makes it possible to eliminate any power-supply induced ripple in the output of the isolation amplifiers and to minimize beats falling in the signal path bandwidth.

PIN DESCRIPTIONS

+V_{IN} AND GND

The +V_{IN} pin supplies power to the oscillator. The GND pins are used for the return currents of the driver chip.

TRANSFORMER	ISOLATION	CHANNELS	I/O	TECHNOLOGY
PWS745-2	750VAC	8	1:1	Thru-hole
PWS745-4	750VAC	4	1:3	Thru-hole
PWS740-2	1500VAC	8	1:1	Thru-hole
PWS750-2U	750VAC	8	1:1	Surface-mount
PWS750-4U	750VAC	4	1:3	Surface-mount

TABLE I.

DIODE BRIDGE	TECHNOLOGY
PWS740-3	Thru-hole
PWS750-3U	Surface-mount

TABLE II.

COM1, COM2

The COM pins are connected to the sources of the internal MOSFETs and each pin must be tied to ground. The current from the primary windings of the transformers flows in through the T and \bar{T} pins and then out through the COM pins.

TTL_{IN}

This pin must be tied to ground, except when it is desired to control the driver frequency with an external TTL level frequency source. The duty cycle can vary from 12% to 95% (see Typical Performance Curves). The input frequency must be twice the desired operating frequency, because an internal flip-flop is used to produce a precise 50% duty cycle signal to the drivers.

TTL_{OUT}

When multiple PWS745-1 drivers must be synchronized to minimize beat frequencies in the output, a single driver is used to synchronize with the remaining drivers. The TTL_{OUT} pin is used as the synchronizing signal from the master controller and is connected to the TTL_{IN} of the slave drivers. A standard open collector output is provided, therefore a

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330 Ω to 3.3k Ω pull-up resistor will be necessary, depending on the stray capacitance on the synchronizing line. A maximum of 8 PWS745-1s can be connected without the use of an external TTL buffer.

ENABLE

An ENABLE pin is provided so that the DRIVE and $\overline{\text{DRIVE}}$ pins can be shut down to the low state within one cycle to minimize power use if desired. A TTL low applied to the pin will shut down the driver and a TTL high will enable the driver. The TTL_{OUT} will still have the 1.2MHz signal so that a master driver can be disabled without shutting down the remaining synchronized drivers. The pin can be left open for normal operation.

DRIVE, $\overline{\text{DRIVE}}$

These pins are normally connected directly to the adjacent GATE pin and are used to drive the gates of the internally packaged MOSFETs. If desired, these pins may be used instead to drive the gates of external FETs, such as those used in the PWS750 series of power components. It is important to minimize the capacitance on these nodes to insure the rapid charging of the MOSFET gates.

GATE, $\overline{\text{GATE}}$

These pins are normally connected directly to the adjacent DRIVE pins, which are internally connected to the gates of the MOSFETs.

T, $\overline{\text{T}}$

The T and $\overline{\text{T}}$ pins are the complementary transformer drive connections. The signals on these pins are 600kHz complementary square waves with twice the amplitude of the input voltage. These lines connect MOSFET switches to the isolation transformers through the T_O and $\overline{\text{T}}_O$ pins. Without proper printed circuit board layout techniques, these lines could generate interference to analog circuits. Refer to the section on layout techniques.

T_O, $\overline{\text{T}}_O$

These pins are the primary terminals of the transformer and are connected to the T and $\overline{\text{T}}$ pins of the PWS745-1.

V_D

The center tap of the primary of the transformer is tied directly to the supply. A 0.3 μF bypass capacitor must be located as close to this pin as possible.

AC

The output of the isolation transformer which is connected to the AC inputs on the PWS740-3 or PWS750-3 diode bridge.

PC BOARD LAYOUT CONSIDERATIONS

Multilayer printed circuit boards are recommended for PWS745 systems. Two-layer boards are certainly possible

with satisfactory operation; however, three layers provide greater density and better control of interference from the power switching lines. Should a four-layer board be required for other circuitry, the use of separate layers for ground and power planes, a layer for switching signals and a layer for analog signals would allow the most straightforward layout of the PWS745 system. Critical consideration should go to minimizing electromagnetic radiation from the power switching lines T-T_O and $\overline{\text{T}}-\overline{\text{T}}_O$. The dynamic component of the current is supplied by the bypass capacitor on the V_D pin of the transformer. The high frequency AC current flows through the transformer, T_O, returning in the T pin, passing through the MOSFET and exiting through the COM pin back to the bypass capacitor. This current path defines a magnetic loop which transmits a magnetic field. The magnetic field lines reinforce at the center of the loop, while the field lines from opposite points of the loop oppose each other outside the loop. Cancellation of the magnetic radiation occurs when the loop is collapsed to two tightly spaced parallel line segments, each carrying the same current in the opposite direction. All of the current in the ground or power plane will flow directly under the T-T_O traces because this is the path of least inductance or impedance. Another potential problem with the T-T_O lines is electric field radiation. Here, the power plane is effective in terminating most of the field lines because of its proximity. Additional shielding can be obtained by running ground trace(s) along the T-T_O lines, facilitating a minimum loop area for the transformer's center-tap bypass capacitor.

The connection between the outputs of the transformer and the diode bridge should be kept as short as possible. Unnecessary stray capacitance on these lines could cause resonant peaking to occur, resulting in a slight increase in output voltage.

EXTERNAL FILTER COMPONENTS

Filter components are necessary to reduce the input ripple current and output voltage noise. Without any input filtering, the sawtooth currents of the switching power lines T-T_O and $\overline{\text{T}}-\overline{\text{T}}_O$ would flow in the supply line. Since this AC current can be as great as 1A peak, voltage interference with other components using this supply line would likely occur. Use of a pi-filter can reduce the input ripple current to about 1mA peak. Recommended values are a 20 μH inductor prior to the connection of the supply to the power plane. A 10 μF tantalum capacitor with a 0.33 μF ceramic capacitor is adequate for the input bypassing. The inductor must be rated for at least 2A or a DC resistance of 0.1 Ω . An example of a low-cost inductor is part number 51591 from Pulse Engineering. Output voltage filtering is achieved with a 0.33 μF capacitor connecting each V_{OUT} pin of the diode bridge to ground. Short leads and close placement of the capacitors to the bridge provide optimum high frequency bypassing. Using correct bypassing techniques, 600kHz ripple of less than 5mVp-p is achievable. High frequency noise bursts coinciding with the switch times are approximately 20mVp-p. Inductance of 20 μH in series with the output loads will significantly reduce the noise seen by the loads.

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5V OPERATION

With 5V operation, the transformer winding ratio is 3-to-1, generating much greater currents in the primary. Therefore, four channels are the maximum that can be powered directly by the PWS745-1.

OUTPUT CURRENT RATING

The PWS745-1 driver contains "soft start" driver circuitry to protect the driver MOSFETs and eliminate high in-rush currents during turn-on. Impedance limiting by the isolation transformers provides short circuit protection on the secondary side and limits the primary side current to a safe value.

The total current which can be drawn from each isolation channel at rated voltage is a function of total power being drawn from both V+ and V- outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases, the maximum total current that can be drawn from any individual channel is:

$$|I_{L+}| + |I_{L-}| < 60\text{mA}$$

It should be noted that many analog circuit functions do not simultaneously draw full rated current from both the positive and negative supplies. Thus the PWS745 system can power more circuits per channel than is first apparent. For example, if a circuit draws 10mA from the positive supply and 3mA from the negative supply, the PWS745 could power (60/13), or about four devices per channel.

HIGH VOLTAGE TESTING

Burr Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pc partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage (1.6 x 750Vrms) protection without damage to the PWS745-2 or PWS745-4. Life test results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature. The minimum AC voltage that initiates partial discharge above 5pc is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms so that even overvoltage induced partial discharge will cease once the barrier is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rated) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown criteria.

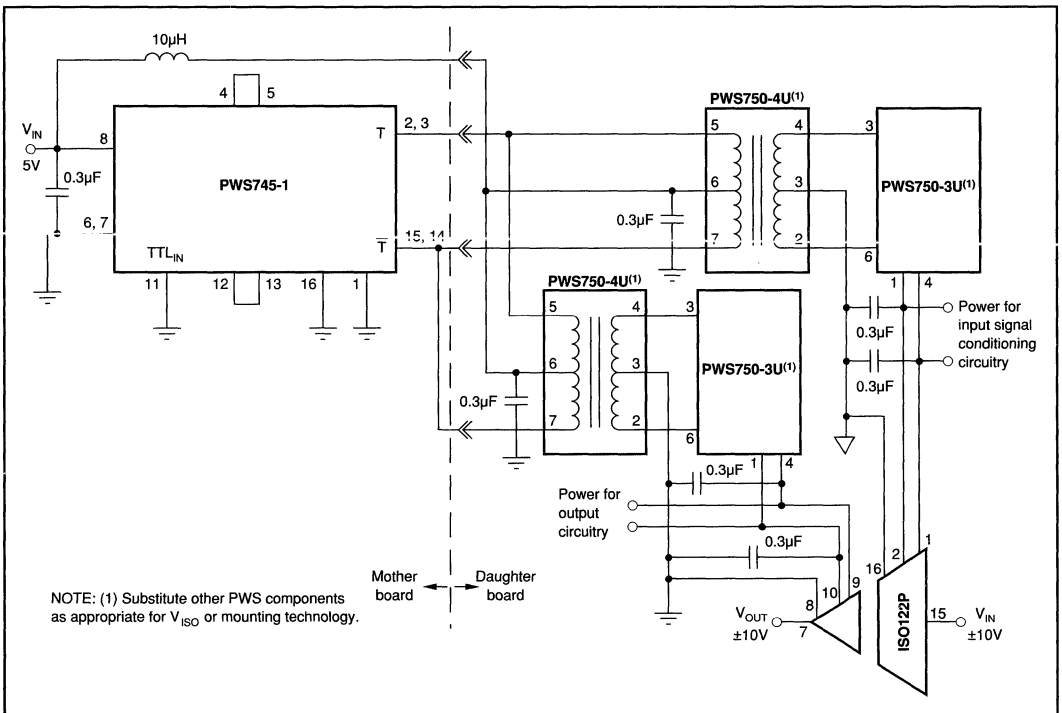


FIGURE 2. Complete $\pm 10\text{V}$ Signal Acquisition System Operating from a Single 5V Supply.

APPLICATIONS

The PWS745 components form part of a versatile collection of isolation power supply components from Burr-Brown. Figures 2, 3, and 4 illustrate only a few of the many possible combinations.

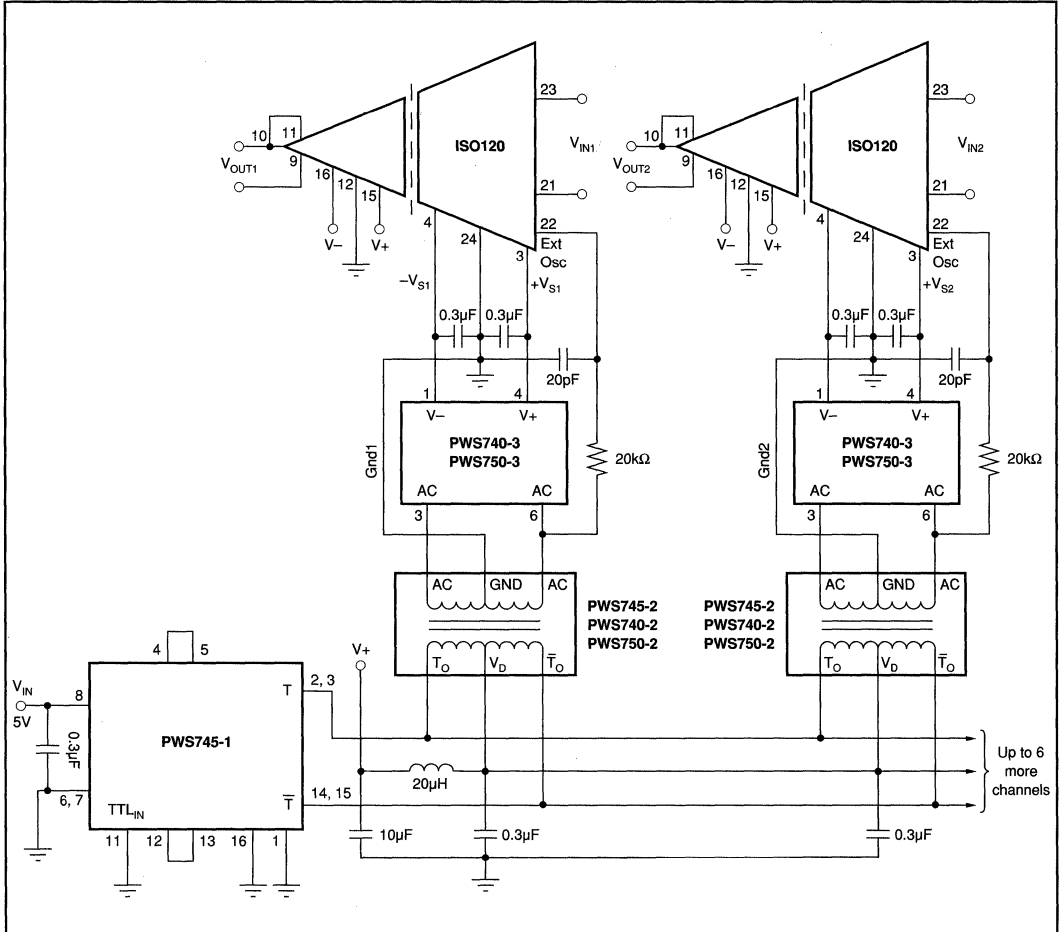


FIGURE 3. Synchronized-Multichannel Isolation System.

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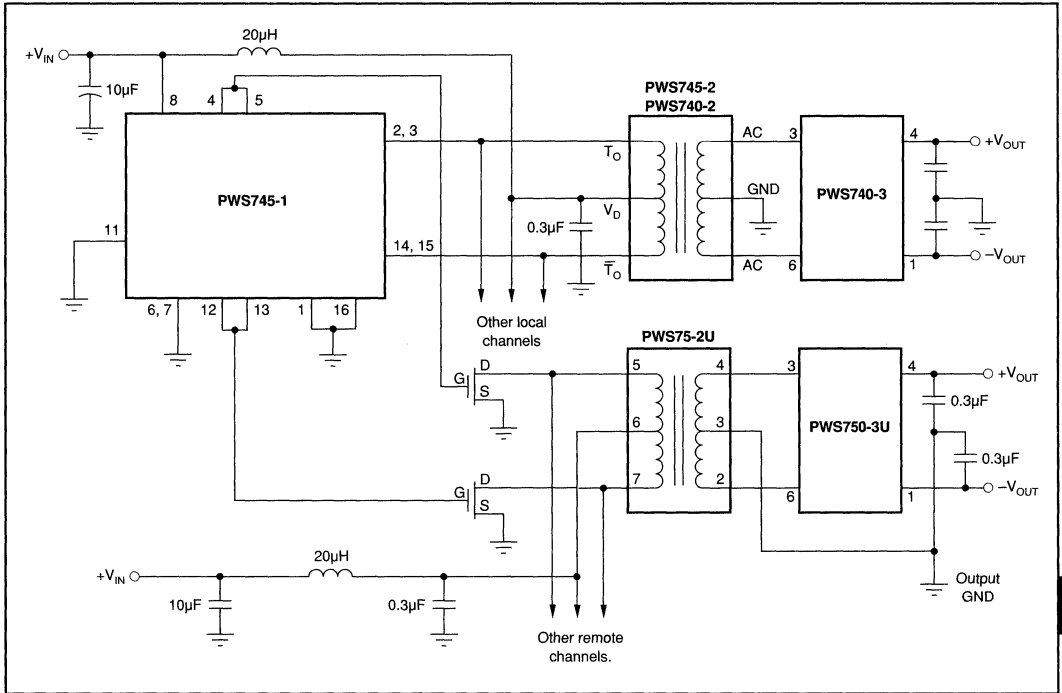


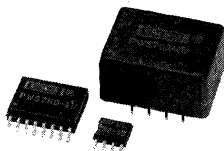
FIGURE 4. Remote and Local Operation of Isolated Power Channels.

PWS745

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ISOLATION PRODUCTS

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PWS750

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT-SURFACE MOUNT
- MULTICHANNEL OPERATION
- 5V OR 15V INPUT OPTIONS
- FLEXIBLE USE WITH PWS740/PWS745 COMPONENTS

DESCRIPTION

The PWS750 consists of three building blocks for building a low cost DC/DC converter. With them you can optimize DC/DC converter PC board layout or build a multichannel isolated DC/DC converter. All parts are surface mount, requiring minimal space to build the converter. The modular design minimizes the cost of isolated power.

The PWS750-1U is a high-frequency (800kHz nominal) driver that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drivers is the 2N7008. The PWS750-1U is supplied in a 16-pin double-wide SO package.

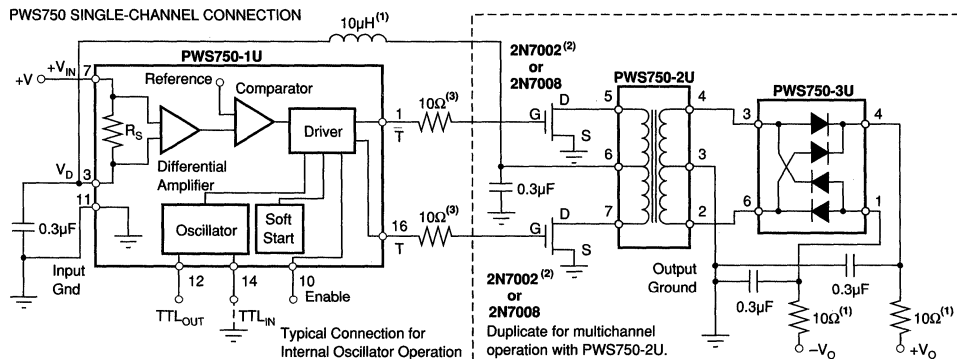
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

The PWS750-2U and PWS750-4U are split-bobbin wound isolation transformers using a ferrite core. They are encapsulated in plastic packages, allowing a high isolation voltage rating.

The PWS750-3U is a high-speed monolithic diode bridge in a plastic 8-pin SO package.

One PWS750-1U can be used to drive up to four channels (15V nominal operation). One PWS750-2U and PWS750-3U and two 2N7002 (surface mount) or 2N7008 (TO-92) MOSFETs made by Siliconix are used per isolated channel. When a PWS750-4U is used as the transformer (5V input), then two TN0604s made by Supertex must be used, due to the higher currents of the primary (lower RDS on) and the lower V_{GS} threshold. With 5V operation only one channel can be directly driven by the PWS750-1U (a simple FET booster circuit can be used for multichannel operation; see Figure 3).



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SPECIFICATIONS

ELECTRICAL

At $T_A = 25^\circ\text{C}$; $+V_{IN} = +15\text{V}$; and $I_{OUT} = \pm 15\text{mA}$ balanced loads unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency: Internal OSC	$TTL_{IN} = 0\text{V}$	725	800	875	kHz
External OSC		1		2.5	MHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
T, \bar{T} Drive Current				50	mApk
T, \bar{T} Drive Voltage, High		3		7	V
Low				0.7	V
TTL_{IN}^+ , I_{IH}			10		nA
I_{IL}			-1		μA
V_{IH}					V
V_{IL}					V
TTL_{OUT}^+ , I_{OL}				0.8	V
				15	mA
PWS750-2U $+V_{IN}$ TO $\pm V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz	60Hz, 1s, <5pC PD	750			Vrms
100% Test ⁽¹⁾		1200			Vrms
Barrier Impedance			$10^{12} \parallel 8$		$\Omega \parallel \text{pF}$
Leakage Current at 60Hz	$V_{ISO} = 240\text{Vrms}$		1	1.5	μArms
Winding Ratio	Primary/Secondary		48/48		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	$I_F = I_R = 50\text{mA}$		40		ns
Reverse Breakdown	$I_R = 100\mu\text{A}$	55			V
Reverse Current	$V_R = 40\text{V}$			1.5	μA
Forward Voltage	$I_F = 100\text{mA}$			1.6	V
PWS750-4U $+5V_{IN}$ TO $\pm 15V_{OUT}$ ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz	60Hz, 1s, <5pC PD	750			Vrms
100% Test ⁽¹⁾		1200			Vrms
Barrier Impedance			$10^{12} \parallel 8$		$\Omega \parallel \text{pF}$
Leakage Current at 60Hz	$V_{ISO} = 240\text{Vrms}$		1	1.5	μArms
Winding Ratio	Primary/Secondary		24/70		
TEMPERATURE RANGE					
Specification		0		+70	$^\circ\text{C}$
Operating	Derated performance	-40		+85	$^\circ\text{C}$
Storage		-40		+85	$^\circ\text{C}$

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on five successive pulses at 60HZ.

PWS750

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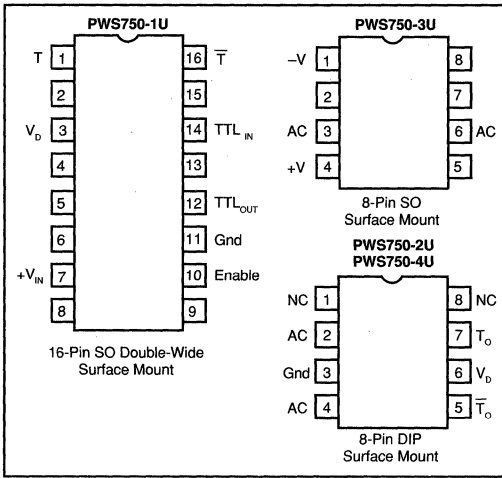
ISOLATION PRODUCTS

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PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	-40°C to +85°C
Lead temperature (soldering, SOIC, 3s)	+260°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

ORDERING INFORMATION

Basic Model Number _____	PWS750-XU
Components _____	
1U : High-Frequency Driver	
2U, 4U : Isolation Transformer	
3U : High-Speed Monolithic Diode Bridge	

PACKAGE INFORMATION⁽¹⁾

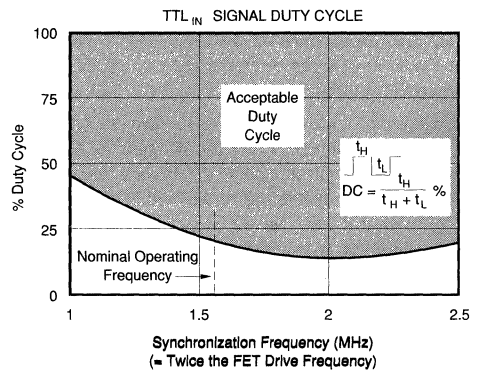
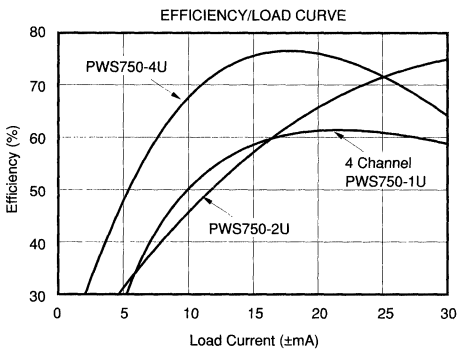
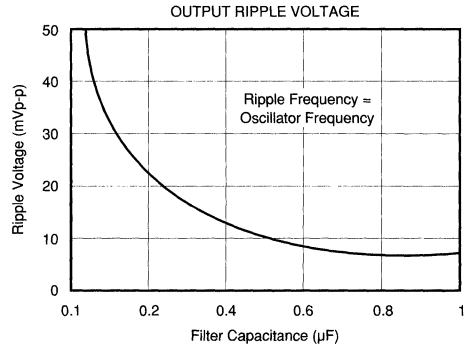
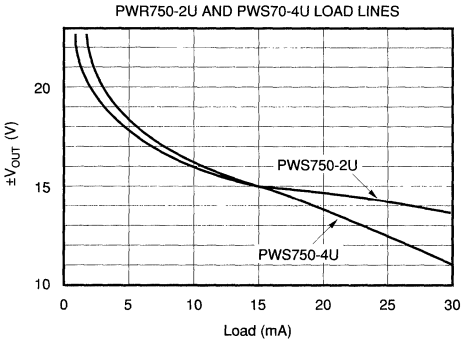
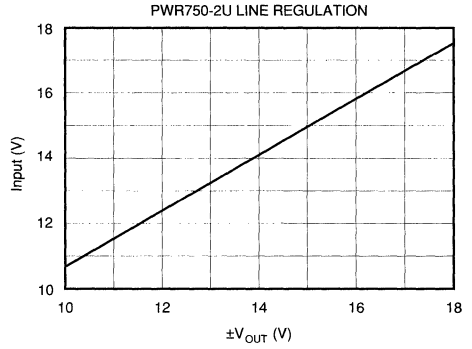
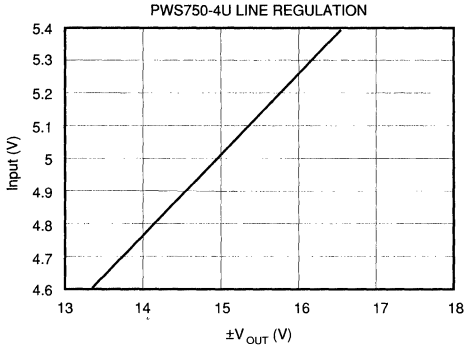
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PWS750-1U	16-Pin SOIC	258
PWS750-2U	8-Pin Plastic	226
PWS750-3U	8-Pin SO	182
PWS750-4U	8-Pin Plastic	226

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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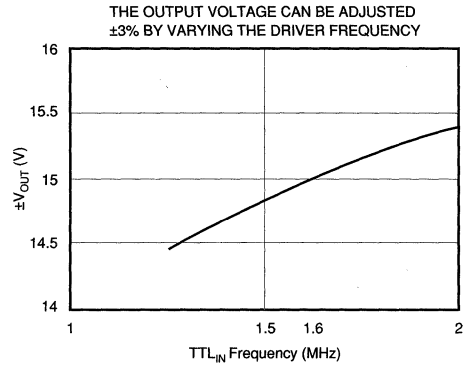
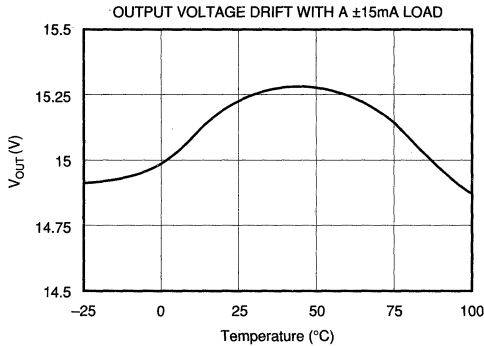
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{IN} = 15\text{VDC}$, $I_{LOAD} = \pm 15\text{mA}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{IN} = 15\text{VDC}$, $I_{LOAD} = \pm 15\text{mA}$ unless otherwise noted.



THEORY OF OPERATION

The PWS750 components are basic building blocks to be used with other standard components to build an isolated push-pull DC/DC converter. The oscillator runs at 800kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage.

PWS750-1U OSCILLATOR PIN FUNCTIONS

TTL_{IN} is used to control the driver frequency with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide-by-2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95% (see Typical Performance Curves). When in the free running mode, the TTL_{IN} pin must be tied to ground.

TTL_{OUT} is used when it is desired to synchronize the outputs of multiple PWS750-1Us to minimize beat frequency problems. A standard open collector output is provided, therefore a 330Ω to $3.3k\Omega$ pull-up resistor will be necessary depending on stray capacitance on the sync line. A maximum of eight PWS750-1Us can be connected without the use of an external TTL buffer.

An Enable pin is provided so that the driver (T , \bar{T}) can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle. A TTL high will enable the driver within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the oscillator. The V_D pin connects the power to the transformer through the internal overcurrent sense resistor. The other end of the overcurrent sense resistor is tied to $+V_{IN}$. A $0.3\mu\text{F}$ bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor; otherwise false current limit conditions can occur due to ripple voltage peaks.

During overload conditions the output drive shuts off for approximately $80\mu\text{s}$, then turns back on for $20\mu\text{s}$, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The T and \bar{T} pins are the complementary FET drive outputs and are tied directly to the corresponding FET gate. The connection must be as short as possible. For multiple channel operation they cannot be located above any ground or power planes, because capacitive loading will not allow fast enough charging of the FET gate.

PWS750-2U AND PWS750-4U TRANSFORMER PIN FUNCTIONS

On the primary side the V_D pin of the PWS750-2U is tied directly to the V_D pin of the PWS750-1U. Remember to place a $0.1\mu\text{F}$ capacitor as close to the PWS750-2U V_D pin as possible. The T_O and \bar{T}_O pins are connected to the drains of the corresponding FETs, whose sources are connected to ground. On the secondary side of the transformer, the Gnd pin is tied directly to the isolated ground. AC pins are 800kHz square wave signals at twice the output voltage, and are connected directly to the corresponding pin on the PWS750-3U. Pins 2 and 4 can be interchanged for ease of hook up. The connection to the diode bridge must be as direct as possible to minimize radiated noise.

The winding ratio for the PWS750-2U is 1:1. This means that the output would normally be less than the input due to voltage drops in the FETs, transformer and diode bridge. Since the DC/DC converter is operating at 800kHz, the transformer is starting to operate close to the resonant frequency, which causes the output to increase in magnitude.

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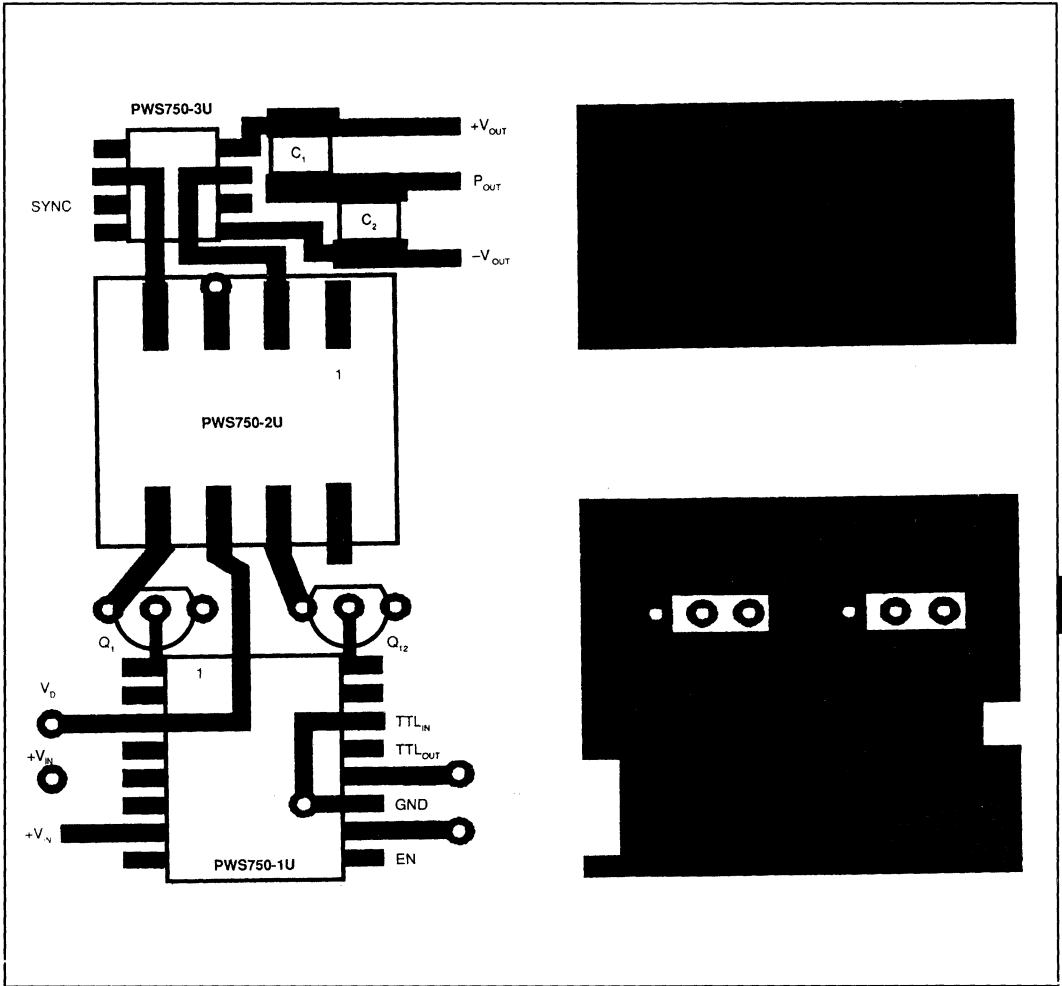


FIGURE 1. Sample PC Board Layout, 4:1.

PWS750

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ISOLATION PRODUCTS

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PWS750-3U HIGH SPEED DIODE BRIDGE PIN FUNCTIONS

The AC pins are tied directly to the AC pins of the PWS750-2U. The +V and -V pins are rectified output voltages. The filter capacitors must be located as close as possible to these pins to minimize series inductance and therefore noise. Bypass capacitors will be needed at each device in the circuit.

BASIC OPERATION

SINGLE CHANNEL OPERATION, PC BOARD LAYOUT CONSIDERATIONS

A simple two-layer board can be used on single channel applications to create a DC/DC converter with low radiated noise. A ground plane should be located directly under both the input and the output components for optimum ground return paths. The surface mount components make it easy to design with a ground plane. The output filter capacitors should be located as close to the PWS750-3U as possible. A sample layout is shown in Figure 1.

For multiple channel applications, T and \bar{T} traces must have minimum capacitive loading. Therefore, there should be no ground plane (or power plane) under these two traces. The driver signal is a 4-6V low current 800kHz signal, which will generate little radiated noise if the traces are kept short.

MULTIPLE CHANNEL OPERATION

The oscillator can drive up to four-channels (eight FETs) directly when operating at 10-18V. A 10Ω resistor must be placed in series with T and \bar{T} to stabilize the FET gate charging. For more than four-channel operation, or 5V-multiple-channel operation, the driver circuit needs a FET booster circuit, as shown in Figure 2. Large gate drive surge currents ($>100\text{mA}$) are needed to turn on the gates.

If the total output current drawn by all the channels exceeds 250mA, then it will be necessary to circumvent the current limit circuit by leaving the V_D pin of the PWS750-1U open, and connect the V_D pin of the PWS750-2U directly to the supply.

5V OPERATION

With 5V operation, the transformer winding current ratio is 3:1, therefore generating much greater currents in the primary. The input ripple voltage will be larger, so an input pi filter will be necessary to isolate the converter noise from the rest of the circuit. For example, when the output is $\pm 15\text{mA}$ the input current will be at least 120mA.

MOSFET	MAX DRIVE CURRENT	PACKAGE	BREAKDOWN
TN0604	4A	TO-92	40V
2N7002	115mA	SO-T23	60V
2N7008	500mA	TO-92	60V
2N7010	1.3A	TO-237	60V
2N7012	1.2A	4-Pin DIP	60V

TABLE I. MOSFET Selector Guide.

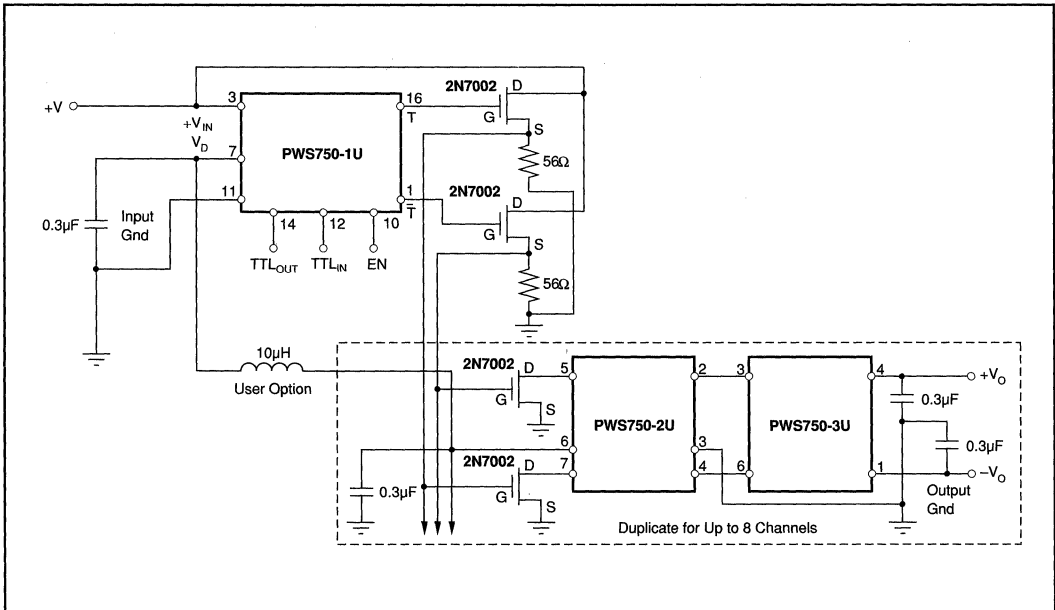


FIGURE 2. MOSFET Driver Booster Circuits.

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OUTPUT CURRENT RATING

The PWS750-1U oscillator contains soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output rating is $\pm 30\text{mA}$. Total current, which can be drawn from each isolation channel, is the total of the power being drawn from both the +V and -V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$|+I_{OUT}| + |-I_{OUT}| < 60\text{mA}$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

When multiple channel operation is used, the maximum current of all channels must be reduced to prevent the overcurrent limit to trip. Alternately, bypass the overcurrent by leaving the V_D pin of the PWS750-1U open and connecting the V_D pin of the PWS750-2U directly to the supply.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage ($1.5 \times 750\text{Vrms}$) protection without damage to the PWS750-2U or PWS750-4U. Life test results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature.

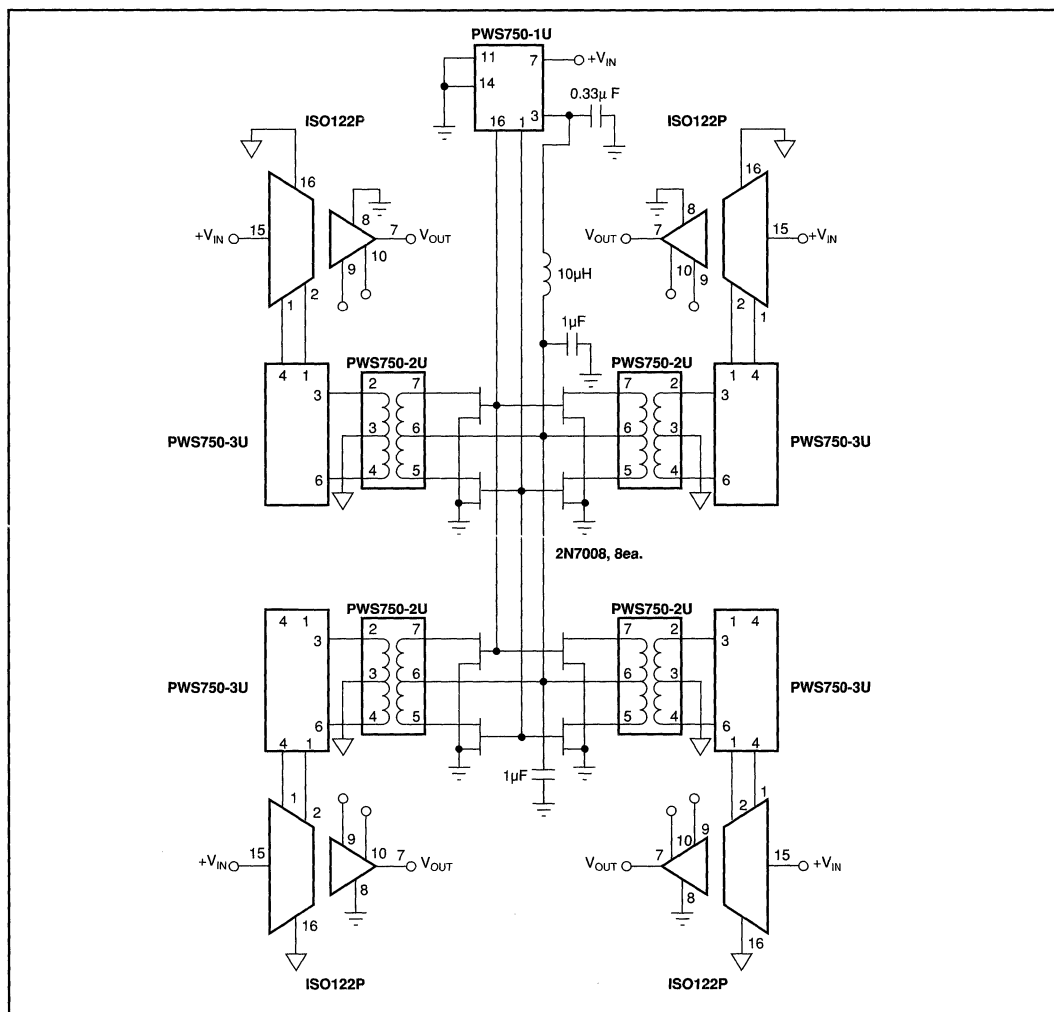


FIGURE 3. Four-Channels of $\pm 10\text{V}$ Signal Isolation with Channel-to-Channel Isolation.

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The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases; this is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms

so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

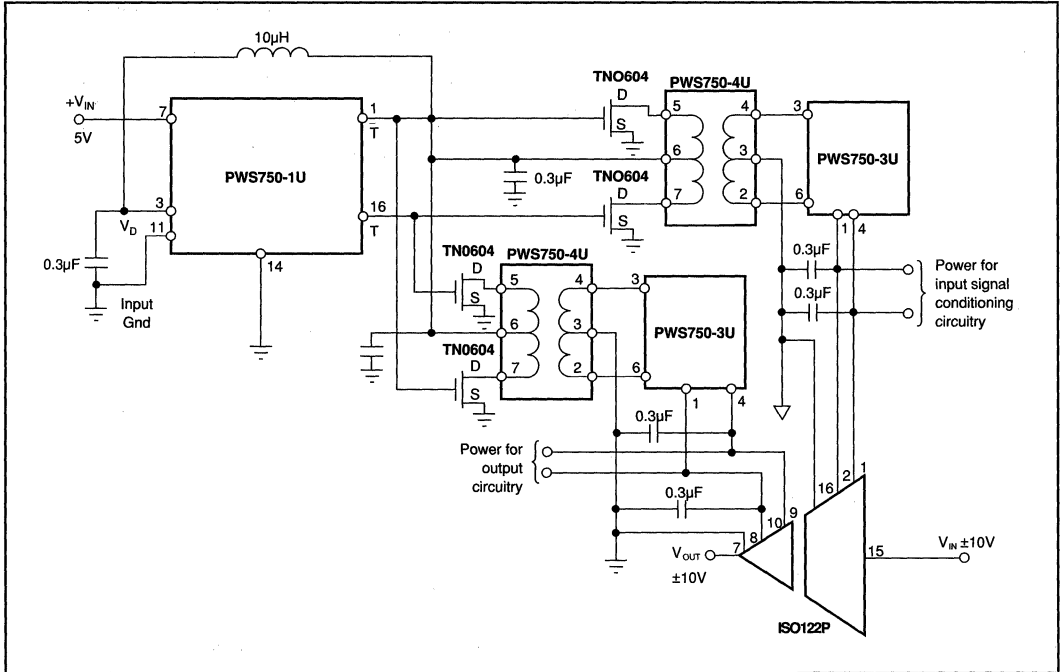


FIGURE 4. A Complete $\pm 10\text{V}$ Signal Acquisition System Operating From a Single 5V Supply.

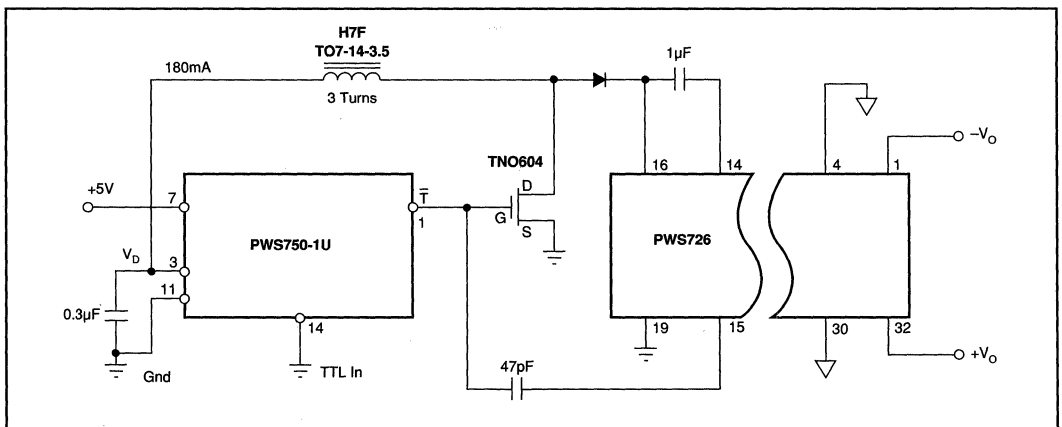


FIGURE 5. A PWS750 Driver Can Be Used to Boost the Input Voltage to 15V to Power a PWS726 From a 5V Supply.

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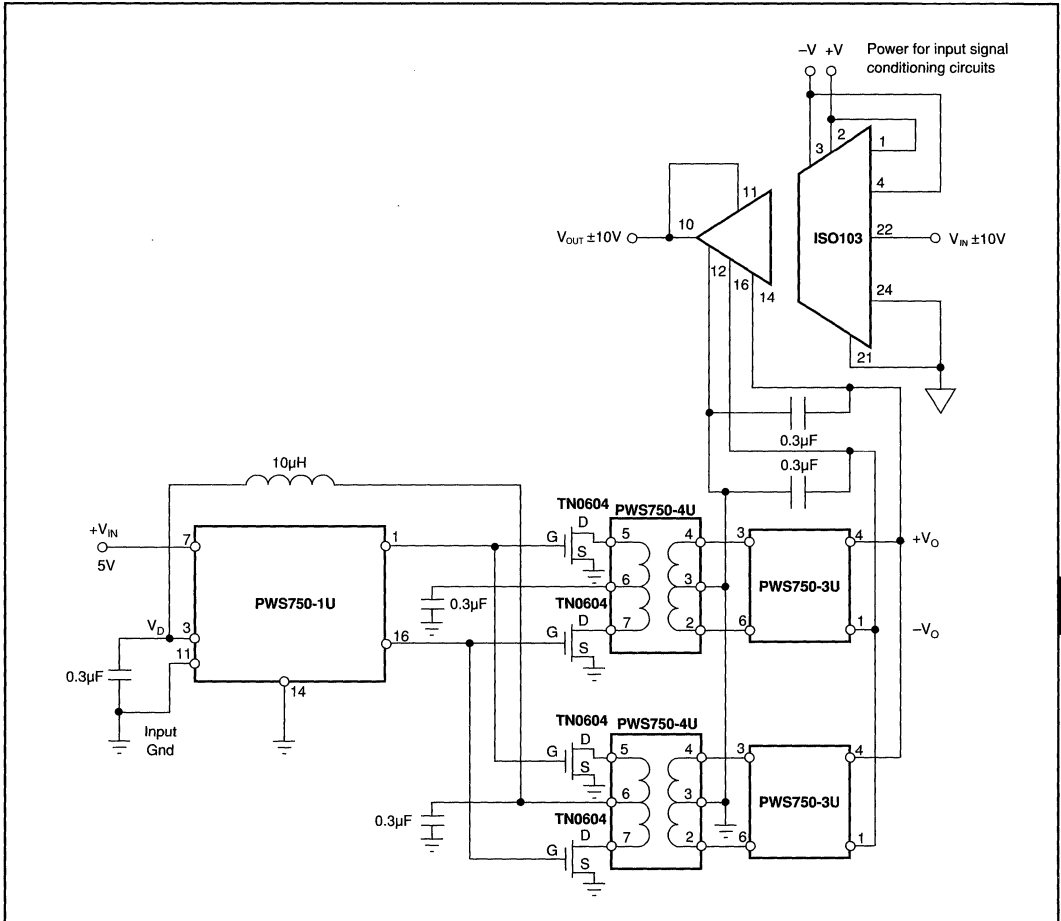


FIGURE 6. Powering the Internally Powered ISO103 Isolation Buffer From a Single 5V Supply. Two Power Channels Are Necessary to Provide the 80mA Nominal for the +V of the ISO103.

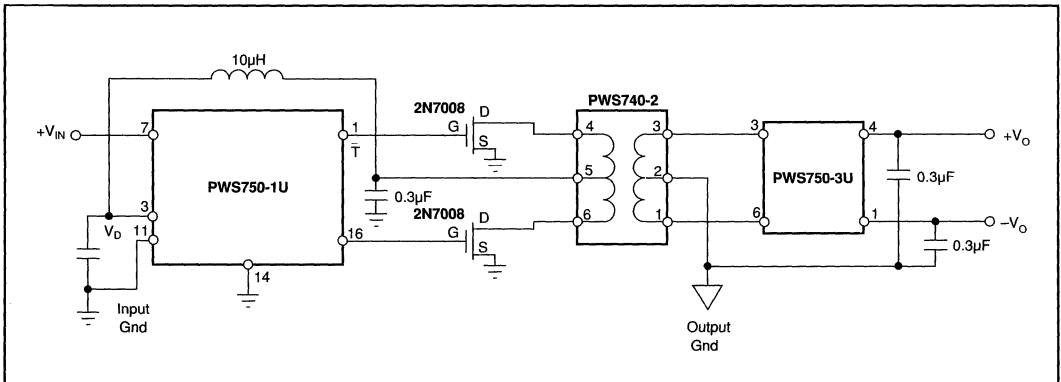


FIGURE 7. 1500VAC Isolation Using PWS740-2 Transformer.

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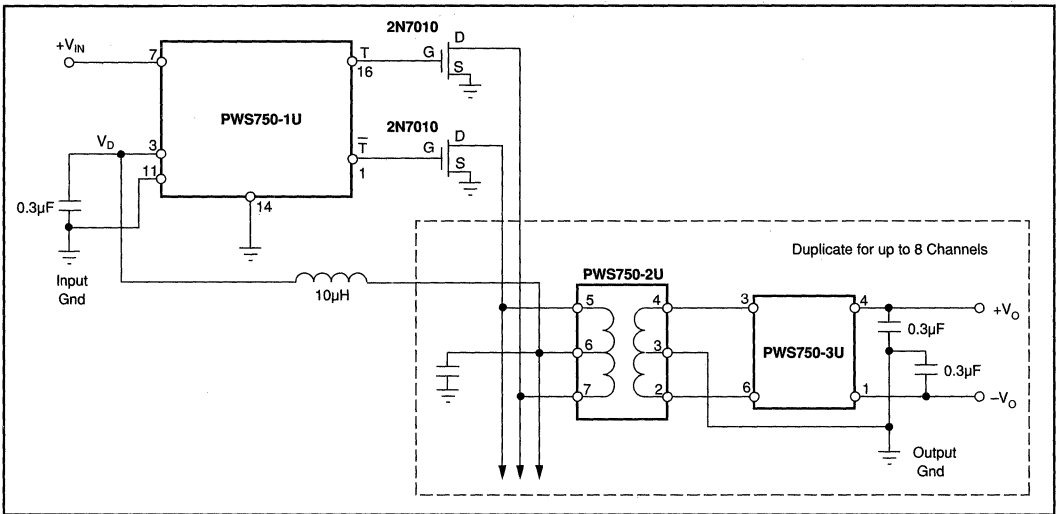


FIGURE 8. FET Pair Driving Up to Eight-Channels.

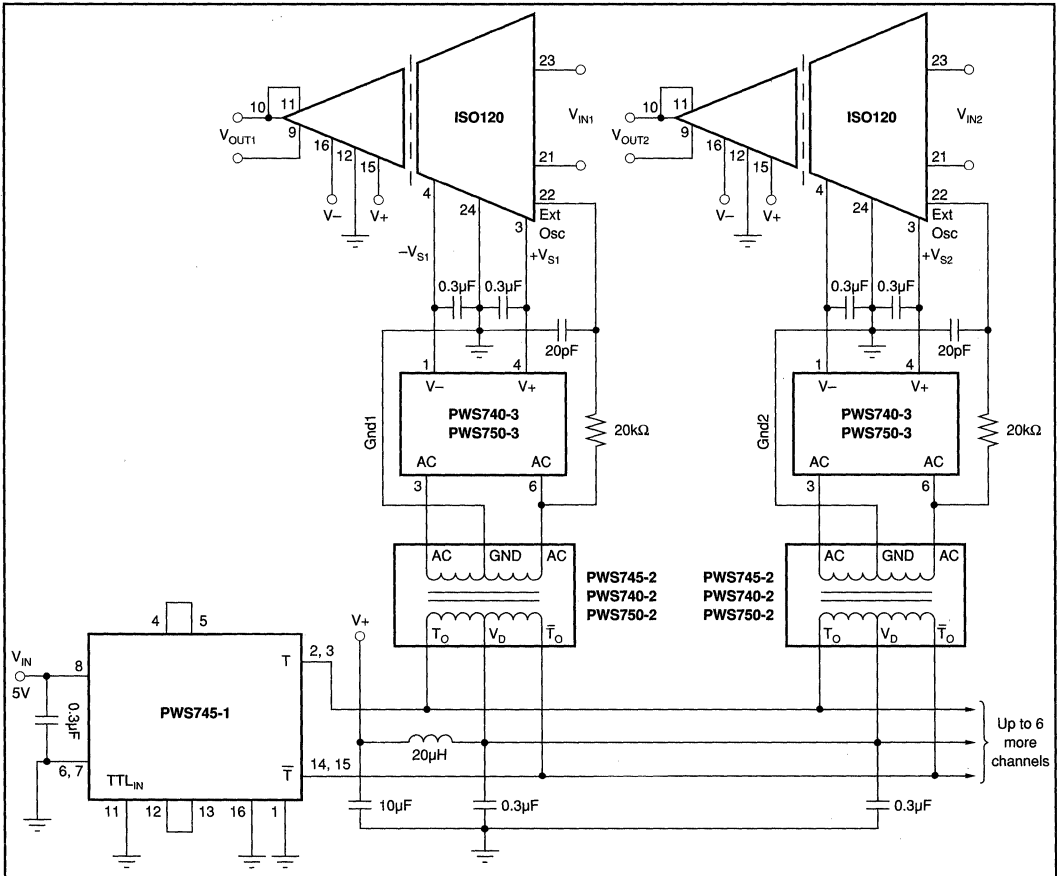
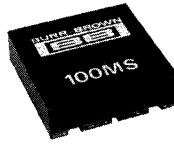


FIGURE 9. Synchronized-Multichannel Isolation System.

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100MS

EMI SHIELD

DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic/ electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover

over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

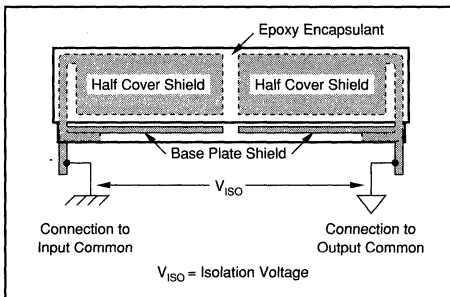


FIGURE 1. Cross-Sectional Side View of 100MS.

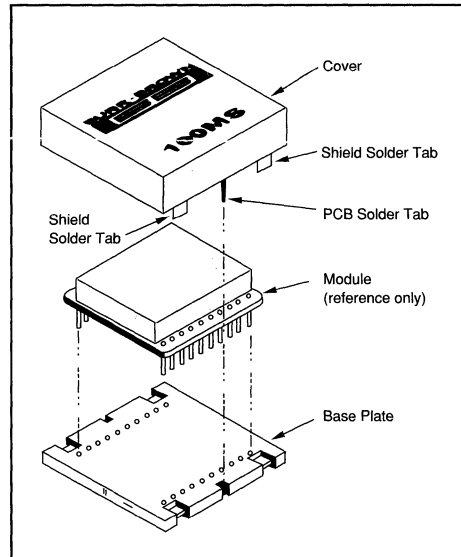
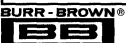


FIGURE 2. Assembly Diagram.

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SPECIFICATIONS

ELECTRICAL

Specifications apply between solder tabs.

PARAMETER	CONDITIONS	100MS			UNITS
		MIN	TYP	MAX	
Isolation Voltage					VDC
Rated Continuous, DC		3500			Vrms
Rated Continuous, AC		2000			VDC
Test	10 Seconds	8000			VDC
Capacitance			5		pF
Resistance			10^{10}		Ω
Leakage Current	120V, 60Hz		0.23		μA

NOTE: Temperature changes ($\Delta T/\Delta t$) greater than 1°C per minute below 0°C and long term storage above 100°C are not recommended.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
100MS	EMI Shield	124

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

APPLICATIONS INFORMATION

MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.

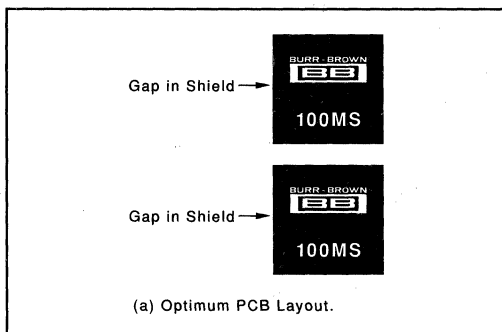


FIGURE 3a. Optimum PCB Layout. Orientation for minimum EMI.

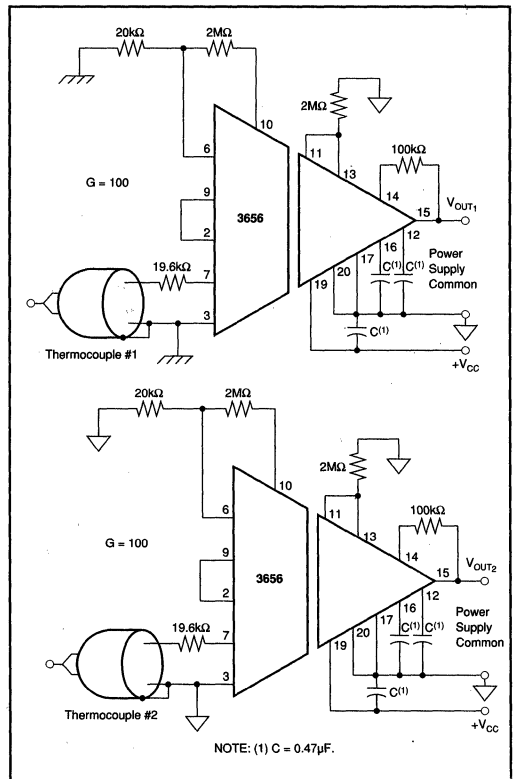
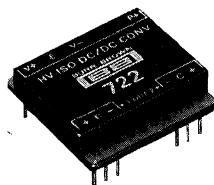


FIGURE 3b. Isolated Data Acquisition Input Circuitry. Orientation for Minimum EMI.

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722

DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED $\pm 5V$ TO $\pm 16V$ OUTPUTS
- HIGH BREAKDOWN VOLTAGE: 8000V Test
- LOW LEAKAGE CURRENT:
<1 μ A at 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm x 27.9mm x 7.6mm
(1.1" x 1.1" x 0.3")

DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 200mA without damage.

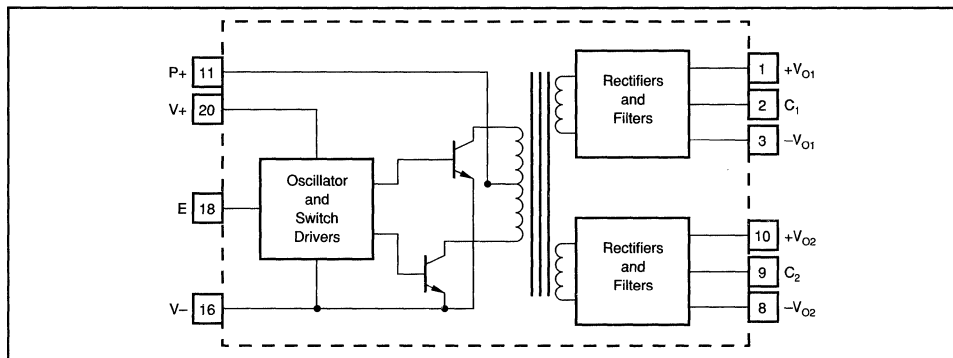
The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.



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PDS-398F

5.179

722

5

ISOLATION PRODUCTS

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_{IN} = 15\text{VDC}$, $C = 0.47\mu\text{F}$, R_L selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15			*			*		VDC
Input Voltage Range ⁽¹⁾		5		16	*		*	*		*	VDC
Input Current	Total Output Current = 12mA Total Output Current = 64mA Total Output Current = 64mA at $T_A = +85^\circ\text{C}$		50			*			*		mA
			105	120		*	*		*	*	mA
			120			*			*		mA
Input Ripple ⁽²⁾	Total Output Current = 160mA Total Output Current = 12mA Total Output Current = 64mA Total Output Current = 160mA		—	—		225	275		—	—	mA
			3			*			*		mA, pk
			6			*			*		mA, pk
			—			12			—		mA, pk
ISOLATION											
Test Voltages	Input-to-Output, 5 seconds, min Input-to-Output, 1 minute, min Channel-to-Channel, 5 seconds, min			8000			*			*	Vpk
				—			—			2500	Vrms
Rated Voltages	Input-to-Output, continuous Channel-to-Channel, continuous			5000			*			*	Vpk
				3500			*			*	V
				2000	*		*			*	V
Isolation Impedance	Input-to-Output		10 6			*			*		GΩ pF
Leakage Current ⁽³⁾	Input-to-Output, 240V, 60Hz			1			*			*	μA
OUTPUT											
Rated Output Voltages ⁽⁴⁾	$I_{LOAD} = 3\text{mA}$ per Output $I_{LOAD} = 16\text{mA}$ per Output $I_{LOAD} = 40\text{mA}$ per Output	15.4 14.3		16.2 16.2	*	*	*	*	*	*	VDC
Output Current	Total of All Outputs Any One Output ⁽⁵⁾	— 3	— 3	— 200 100	13.7 *	14.2 *	16.2 *	— *	— *	— *	VDC mA mA
Load Regulation			⁽⁵⁾			*			*		
Ripple Voltage	$I_{LOAD} = 3\text{mA}$ per Output $I_{LOAD} = 16\text{mA}$ per Output $I_{LOAD} = 40\text{mA}$ per Output		15 35 —			*	*	*	*	*	mVpk mVpk mVpk
Tracking Error between Dual Outputs	Balanced Loads		±100			*	*	*	*	*	mVDC
Sensitivity to Input Voltage Changes			1.13			*			*		V/V
Output Voltage Temperature Coefficient	$T_A = T_{\text{SPECIFICATION RANGE}}$		±0.02			*			*		%/°C
TEMPERATURE											
Specification	$I_{LOAD} \leq 16\text{mA}$ per Output $I_{LOAD} \leq 40\text{mA}$ per Output	−25 −25		+85 +60	*	*	*	*	*	*	°C °C
Storage		−55		+125	*	*	*	*	*	*	°C
Junction Temperature				+125	*	*	*	*	*	*	°C

*Specifications same as 722.

NOTES: (1) For ambient temperature above $+70^\circ\text{C}$ the input voltage is 12.5V (max). The input voltage remains 16V (max) if case temperature is kept below $+85^\circ\text{C}$. (2) External capacitor across "P+" to "V−" pins and 12" of #24 wire to V_{IN} . (3) Reference UL544, paragraph 27.5, Leakage Current. (4) See "Typical Performance Curves." (5) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
722	20-Pin	102A

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE ⁽¹⁾
722	20-Pin	−25°C to +85°C
722BG	20-Pin	−25°C to +85°C
722MG	20-Pin	−25°C to +85°C

NOTE: (1) −25°C to +60°C for $I_{LOAD} \leq 40\text{mA}$ per Output.

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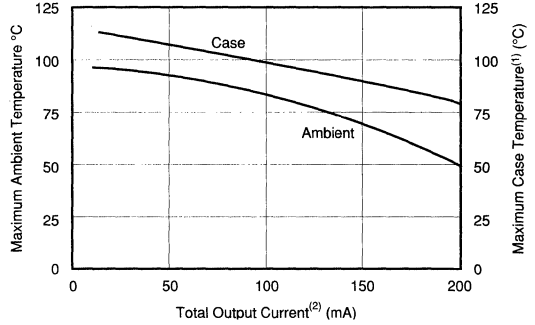
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_N = 15\text{VDC}$, $C = 0.47\mu\text{F}$, R_i selected per Typical Performance Curve.

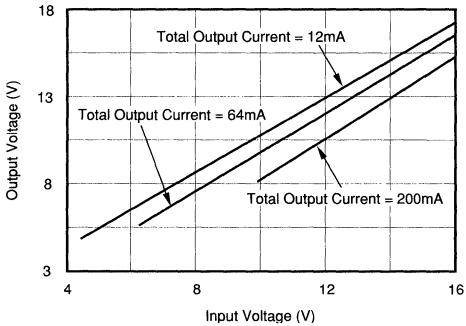
SELECTION OF R_i OR EXTERNAL VOLTAGE V_{+EXT} FOR MINIMUM INTERNAL POWER DISSIPATION

		MAXIMUM OUTPUT CURRENT FROM ANY SINGLE OUTPUT		
		<16mA	16mA to 30mA	30mA
Input Voltage (V)	>13	1.3k Ω	820 Ω	510 Ω
	11 to 13	820 Ω	510 Ω	200 Ω
	9 to 11	510 Ω	200 Ω	0 Ω
	8 to 9	200 Ω	0 Ω	—
	<8	0 Ω	—	—
	V_{+EXT}	6.5V	7.5V	9.0V

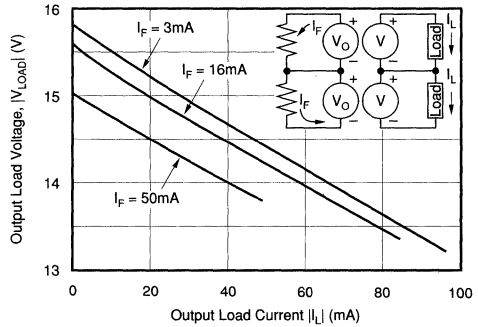
MAXIMUM SAFE OPERATING TEMPERATURE vs TOTAL OUTPUT CURRENT



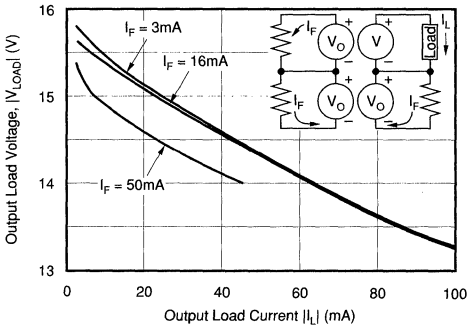
OUTPUT VOLTAGE vs INPUT VOLTAGE



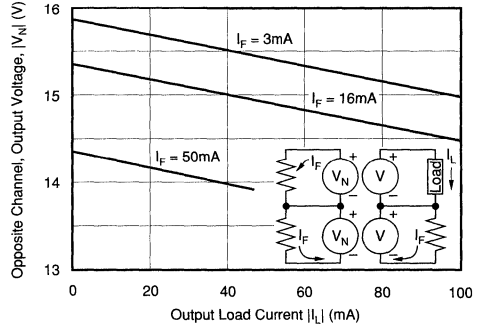
SINGLE-CHANNEL LOAD REGULATION



SINGLE OUTPUT LOAD REGULATION



CHANNEL-TO-CHANNEL INTERACTION

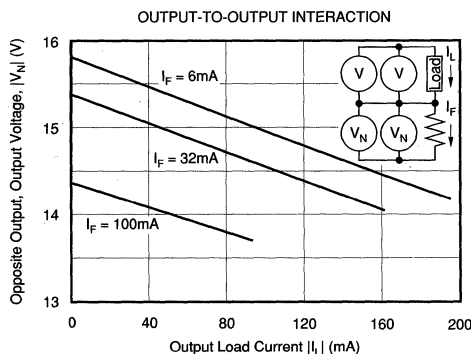
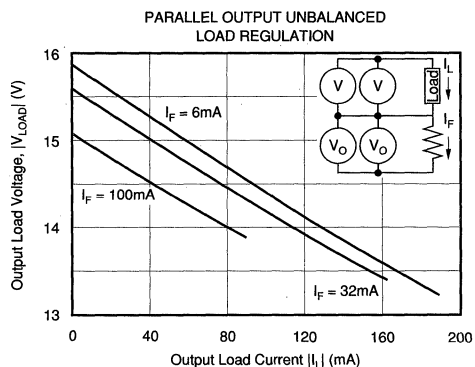
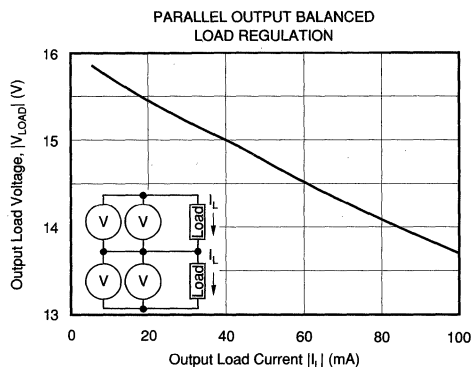


NOTES: (1) Using a 104mm x 19mm x 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound. (2) Total output current is the sum of the currents for each individual output.

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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{IN} = 15\text{VDC}$, $C = 0.47\mu\text{F}$, R_1 selected per Typical Performance Curve.



INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respects to "V-".

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor, R_1 . The value of R_1 as a function of V_{IN} is shown in the Typical Performance Curves section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V-." If a separate source is used, the "V+" input must be applied before the "P+" input to avoid possible damage to the unit. "P+" and "V+" must remain positive with respect to "V-" at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

An external capacitor, "C" ($0.47\mu\text{F}$ ceramic), is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal $0.22\mu\text{F}$ capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to $10\mu\text{F}$ between each output and its common.

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs⁽¹⁾. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels⁽²⁾ may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 optically coupled isolation amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration, the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

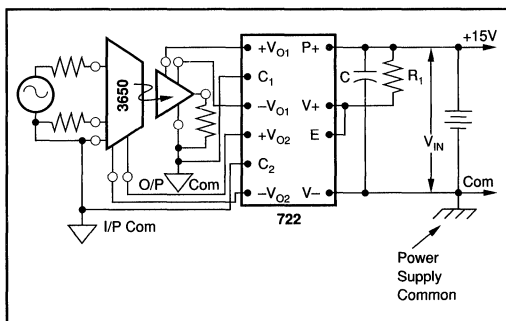


FIGURE 1. Three-Port Isolation

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation, the 722's input-to-output isolation specification applies to the amplifier's input-to-output voltages, while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com #1" and "I/P Com #2."

NOTES: (1) "Output" denotes a single output terminal (+V or -V) and its associated common. (2) "Channel" denotes a pair of outputs (+V and -V) and their associated common.

SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs—such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

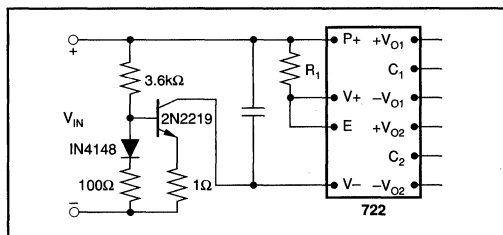


FIGURE 2. Short Circuit Protection.

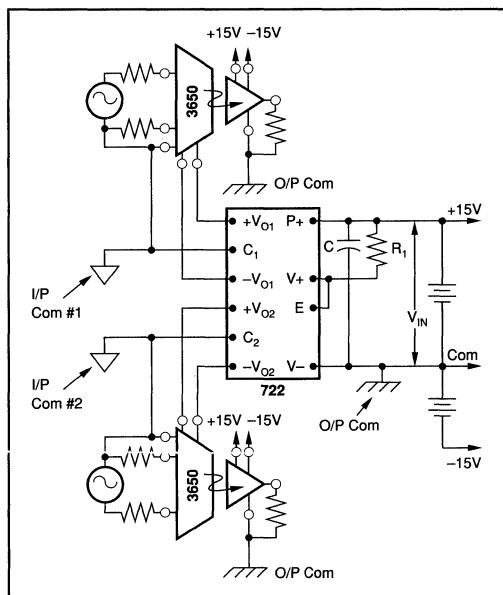
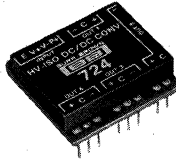


FIGURE 3. Two-Port Isolation with Two 3650's.



724

QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED $\pm 8V$ OUTPUTS
- HIGH BREAKDOWN VOLTAGE:
3000V Test
- LOW LEAKAGE CURRENT: $<1\mu A$ at
240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE: 27.9mm X 27.9mm X 6.6mm
(1.1" X 1.1" X 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION

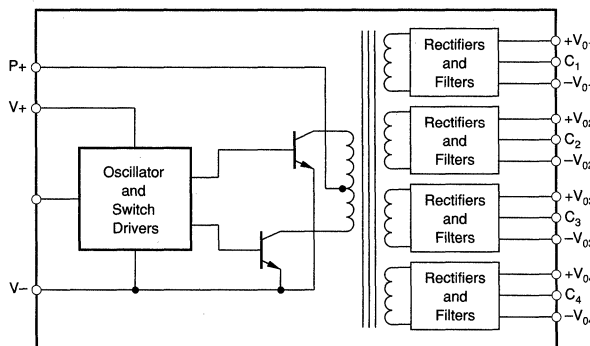
DESCRIPTION

The 724 converts a single 5VDC into four pairs of bipolar output voltages of approximately half the output voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, and low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.



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SPECIFICATIONS

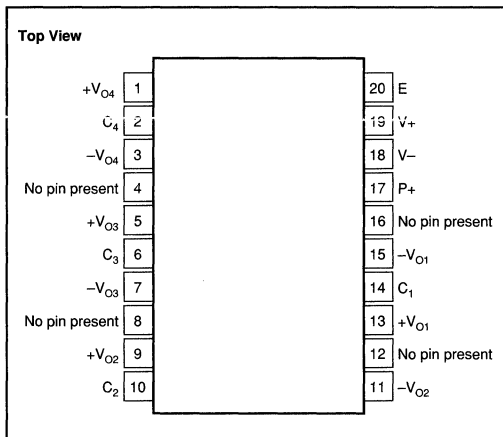
ELECTRICAL

At 25°C with $V_{IN} = 15V$, $R_I = 1.3k\Omega$, $C = 0.47\mu F$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	$\Sigma I_{OUT} = 24mA$		50		mA
	$\Sigma I_{OUT} = 128mA, 25^\circ C$		110	125	mA
	$\Sigma I_{OUT} = 128mA, 25^\circ C$		120		mA
Input Ripple ^(1,5)	$\Sigma I_{OUT} = 24mA, C = 0.47\mu F$		10		mA, pk
	$\Sigma I_{OUT} = 128mA, C = 0.47\mu F$			25	mA, pk
ISOLATION					
Test Voltage ⁽²⁾	Input-to-Output, 5s min Channel-to-Channel, 5s min			3000	VDC
Rated Voltage ⁽²⁾	Input-to-Output, Continuous Channel-to-Channel, Continuous			1000	VDC
Isolation Impedance	Input-to-Output		10 6	1000	GΩ pF
Leakage Current	Input-to-Output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage ⁽³⁾	At 15V Input $I_L = 3mA$	8.0	8.5	9.0	V
	$I_L = 16mA$	7.5	7.9	8.3	V
Current for Rated Voltage	Total of All Outputs Any One Output ⁽⁴⁾			128	mA
Total Safe Nondestructive Current	Total of All Outputs Any One Output	3		500	mA
				200	mA
Load Regulation ⁽⁵⁾			⁽⁴⁾		
Ripple Voltage ⁽⁵⁾	$I_L = 3mA$		35		mV, pk
	$I_L = 16mA$			200	mV, pk
Difference of +V _o and -V _o	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

NOTES: (1) 0.47μF external capacitor across "P+" to "V-" pins and 12" of #24 wire to V_{IN}. (2) See "Isolation Voltage Ratings" on page 5. The input to output and channel to channel continuous AC rating is 700Vrms. (3) See "Typical Performance Curves." (4) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy. (5) Test bandwidth 10MHz, max.

CONNECTION DIAGRAMS



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
724	20-Pin	102A

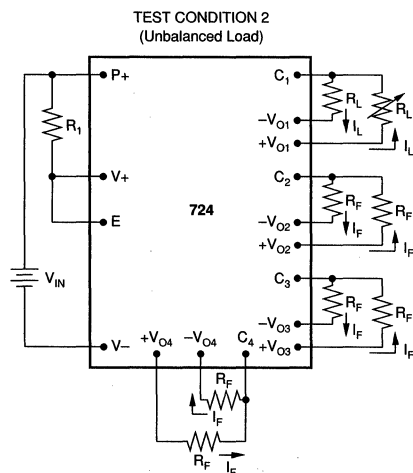
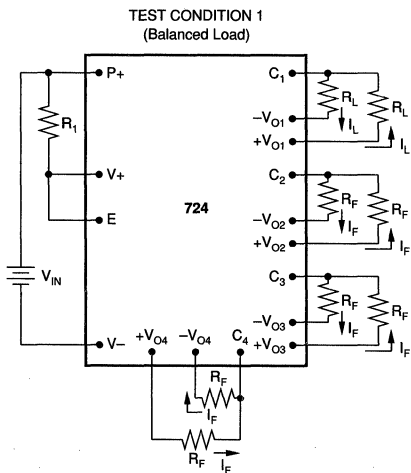
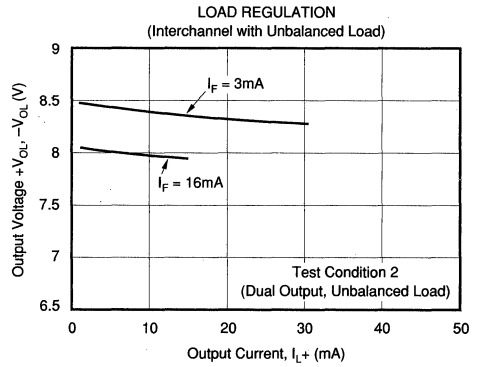
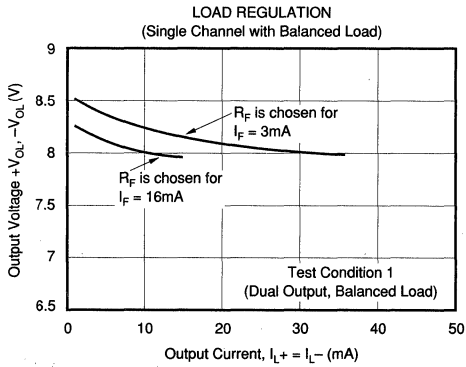
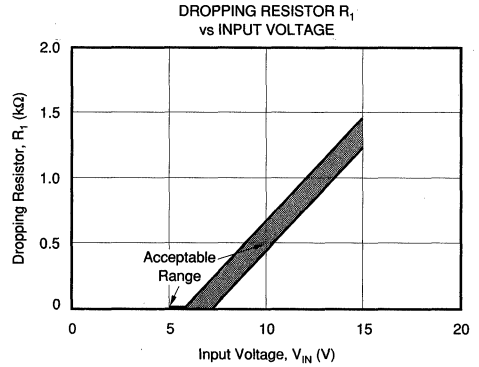
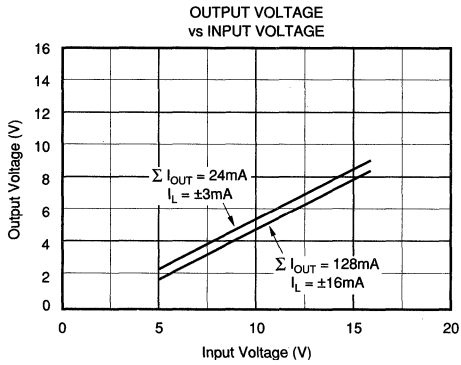
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES

All specifications typical at 25°C, unless otherwise noted.



INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-", the only requirement is that "P+" and "V+" must be positive with respect to "V-".

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor, R_1 . The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V-". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to "V-" at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-".

An external capacitor, "C" (0.47 μ F ceramic), is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem.

Each output is filtered with an internal 0.047 μ F capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10 μ F between each output and its common.

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs⁽¹⁾. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Outputs channels⁽²⁾ may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two 3650 optically coupled isolation amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

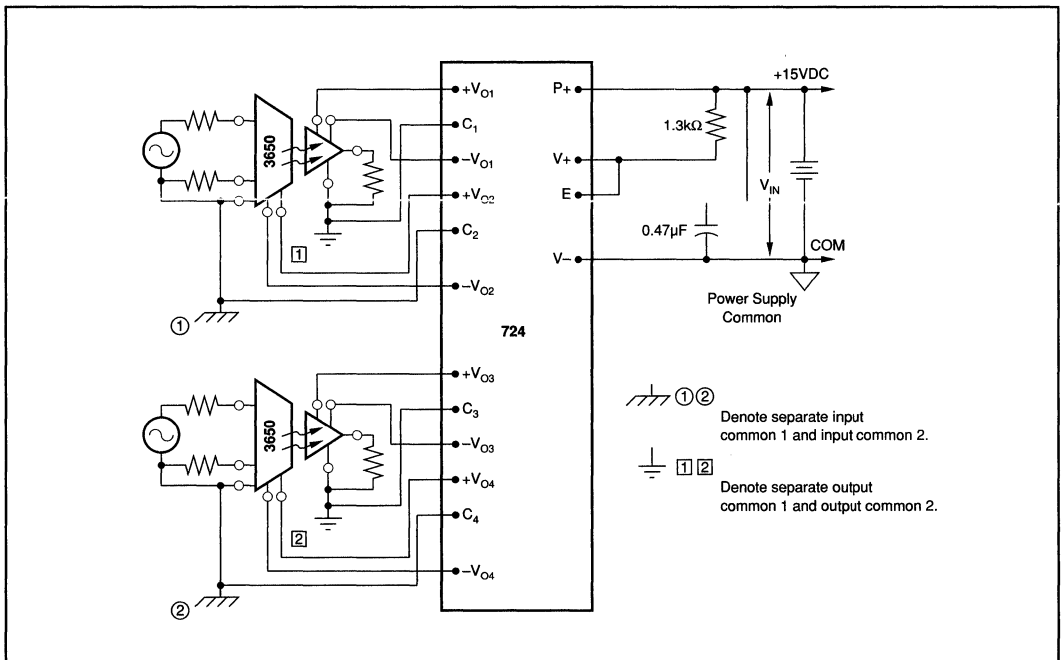


FIGURE 1. Three-Port Isolation.

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Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650s connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and -15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation, the 724's isolation specification applies to amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration), it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{TEST} = (2 \times V_{CONTINUOUS RATING}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.⁽³⁾ Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs—such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

NOTES: (1) "Output" denotes a single output terminal (+V or -V) and its associated common. (2) "Channel" denotes a pair of outputs (+V and -V) and their associated common. (3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

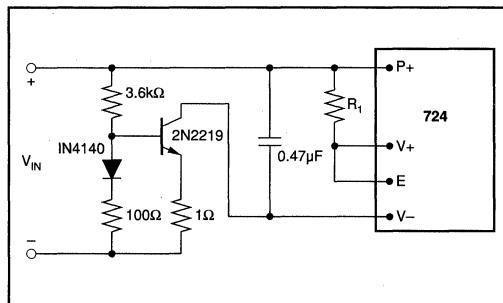


FIGURE 3. Short Circuit Protection.

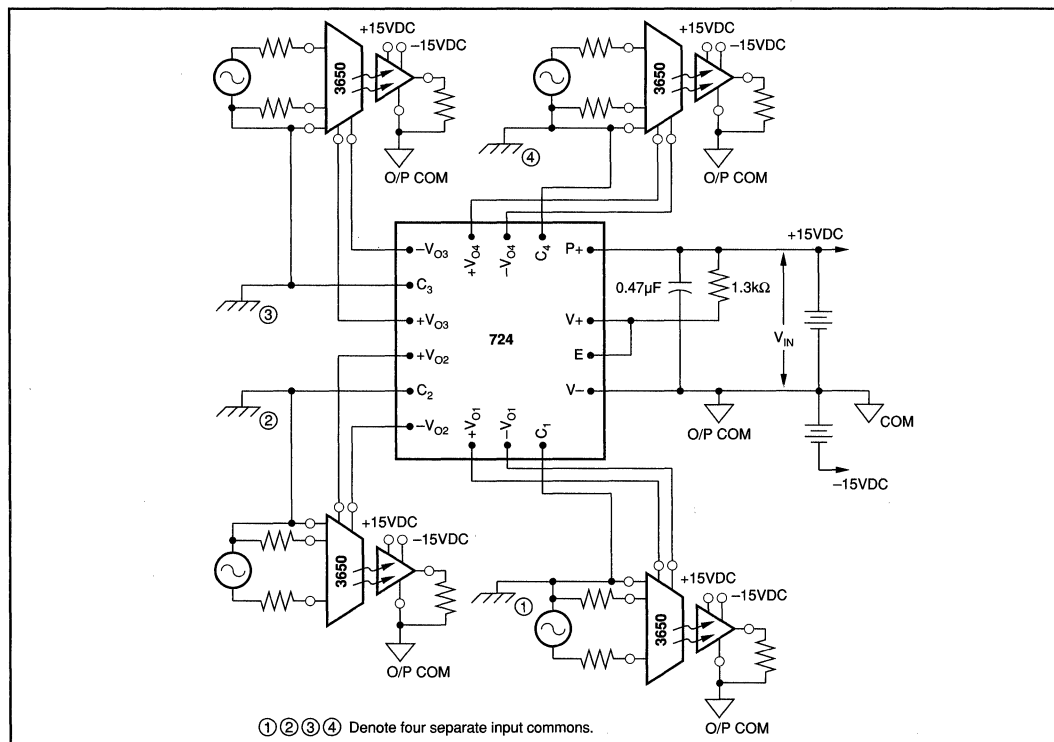


FIGURE 2. Two-Port Isolation with Four 3650s.

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3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
±2000V Continuous
140dB Rejection
- ULTRA LOW LEAKAGE
0.35μA max at 240V/60Hz
1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
0.05% Linearity
0.05%/1000Hrs Stability
- WIDE BANDWIDTH
15kHz ±3dB
1.2V/μs Slew Rate

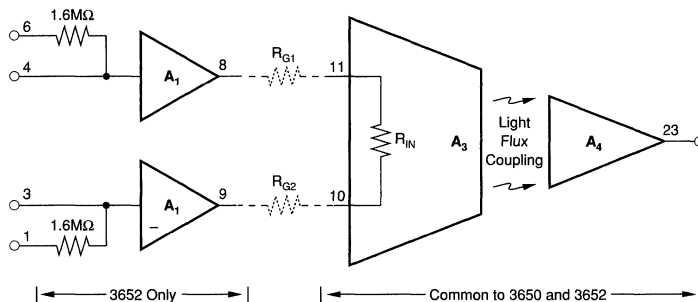
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation demodulation techniques. Compared to these earlier isolation amplifiers, the 3650 and 3652 have the advantage of smaller size,

lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier-type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



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3650/3652

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ISOLATION AMPLIFIERS

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SPECIFICATIONS

At +25°C and ±15VDC supply voltages, unless otherwise specified.

MODEL	3650MG/HG ⁽¹⁾	3650JG	3650KG	3652MG/HG ⁽¹⁾	3652JG
ISOLATION					
Isolation Voltage Rated Continuous, min Tested Voltage, min, 10s Duration	2000Vp or VDC 5000Vp				
Isolation Mode Rejection, G = 10 DC 60Hz, 5000Ω Source Unbalance Leakage Current, 240V/60Hz Isolation Impedance Capacitance Resistance	140dB 120dB 0.35μA, max 1.8pF 10 ¹² Ω				
GAIN					
Gain Equation for Current Sources for Voltage Sources	$G_v1 = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}} \text{ V/V}$ $G_i = 10^6 \text{ V/Amp}$			$G_i = 1.0057 \times 10^6 \text{ V/Amp}^{(2)}$ $\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_o} \text{ V/V}$	
Input Resistance, R _{IN} , max Buffer Output Impedance, R _O	25Ω Not Applicable			25Ω 90Ω ±30Ω	
Gain Equation Error, max ⁽³⁾ Gain Nonlinearity Gain vs Temperature Gain vs Time	1.5% ±0.05% typ ±0.2% max 300ppm/°C	0.5% ±0.03% typ ±0.1% max 100ppm/°C ±0.05%/1000hrs	0.5% ±0.02% typ ±0.05% max 50ppm/°C	1.5% ⁽⁴⁾ ±0.05% typ ±0.2% max 300ppm/°C	0.5% ⁽⁴⁾ ±0.05% typ ±0.1% max 200ppm/°C ±0.05%/1000hrs
Frequency Response Slew Rate ±3dB Frequency Settling Time to ±0.01% to ±0.1%	0.7V/μs min, 1.2V/μs typ 15kHz 400μs 200μs				
INPUT STAGE⁽⁶⁾					
Input Offset Voltage at 25°C, max ⁽³⁾ vs Temperature, max vs Supply vs Time	±5mV ±25μV/°C	±1mV ±10μV/°C 100μV/V 50μV/1000hrs	±0.5mV ±5μV/°C	±5mV ±50μV/°C	±2mV ±25μV/°C 100μV/V 100μV/1000hrs
Input Bias Current at 25°C vs Temperature vs Supply	10nA typ, 40nA max 0.3nA/°C 0.2nA/V			10pA typ, 50pA max Doubles Every +10°C 1pA/V	
Input Offset Current vs Temperature vs Supply	Effects Included In Output Offset			10pA Doubles Every +10°C 1pA/V	
Input Impedance Differential Common-Mode	"R _{IN} " = 25Ω max 10 ¹¹ Ω			10 ¹¹ Ω 10 ¹¹ Ω	
Input Noise Voltage, 0.05Hz to 100Hz 10Hz to 10kHz	4μVp-p 4μVrms			8μVp-p 5μVrms	
Input Voltage Range Common-Mode, Linear Operation, w/o damage, at +, - at +I, -I at +I _R , -I _R	±(V - 5)V ±V Not Applicable ⁽⁶⁾ Not Applicable ⁽⁶⁾			±(V - 5) ±V ±300V for 10ms ⁽⁷⁾ ±3000V for 10ms ⁽⁷⁾	
Differential, w/o damage, at +, - Differential, w/o damage, at +I, -I Differential, w/o damage, at +I _R , -I _R	±V Not Applicable Not Applicable			±V ±600V for 10ms ⁽⁷⁾ ±6000V for 10ms ⁽⁷⁾	
Common-mode Rejection, 60Hz	90dB at 60Hz, 5kΩ Imbalance			80dB at 60Hz, 5kΩ Imbalance	
Power Supply (Input Stage Only) Voltage (at "+V" and "-V") Current Quiescent with ±10V Output ⁽⁷⁾	±8V to ±18V ±1.2mA ⁽⁸⁾ +6.5mA or -6.5mA, typ +12mA or -12mA, max			±8V to ±18V ±3mA ⁽⁸⁾ +8.5mA or -8.5mA, typ +16mA, or -16mA, max	

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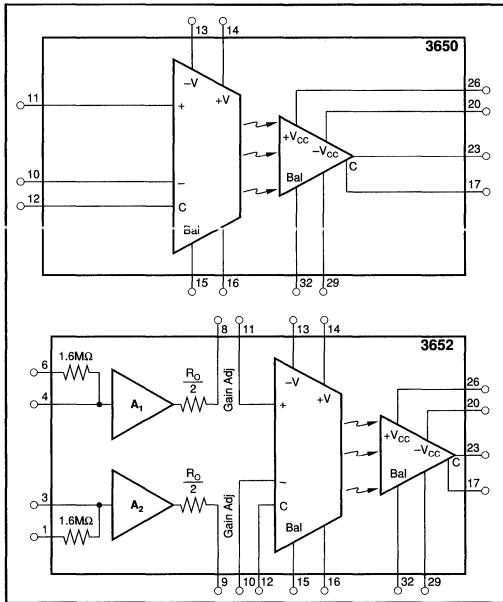
SPECIFICATIONS (CONT)

At +25°C and ±15VDC supply voltages, unless otherwise specified.

MODEL	3650MG/HG ⁽¹⁾	3650JG	3650KG	3652MG/HG ⁽¹⁾	3652JG
OUTPUT STAGE					
Output Voltage, min	±10V			±10V	
Output Current, min	±5mA			±5mA	
Output Offset Voltage at 25°C, max ⁽³⁾	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900μV/°C	±450μV/°C	±300μV/°C	±900μV/°C	±450μV/°C
vs Supply	±500μV/V			±500μV/V	
vs Time	±1mV/1000hrs			±1mV/1000hrs	
Output Noise Voltage	50μVp-p			50μVp-p	
0.05Hz to 100Hz	65μVrms			65μVrms	
10Hz to 1kHz					
Power Supply (Output Stage Only)	±8V to ±18V				
Voltage ("+"V _{cc} " and "-V _{cc} ")					
Current	±2.3mA typ, ±6mA max				
Quiescent	±11mA				
with ±5mA Output, max					
TEMPERATURE⁽⁹⁾					
Specification	0°C to +85°C				
Operating	-40°C to +100°C				
Storage	-55°C to +125°C				

NOTES: (1) All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration increased from 10 seconds minimum to 60 seconds minimum; (b) Input offset voltage at 25°C, max: ±10mV; vs temperature max: ±100μV/°C; (c) Output offset voltage at 25°C, max: ±50mV; vs temperature max: ±1.8mV/°C. (2) If used as 3650, see Installation and Operating Instructions. (3) Trimmable to zero. (4) Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±1 or ±1_n pins). (5) Input stage specifications at +1 and -1 inputs for 3652 unless otherwise noted. (6) Maximum safe input current at either input is 10mA. (7) Continuous rating is 1/3 pulse rating. (8) Load current is drawn from one supply lead at a time; other supply current at quiescent level. For 3652 add 0.2mA/V of positive CMV. (9) dT/dt < 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to +85°C temperature range.

PIN CONFIGURATIONS



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
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3652	32-Pin DIP	77A

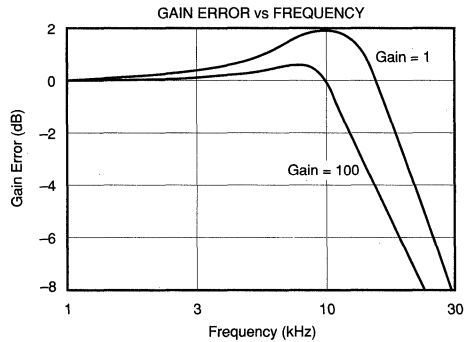
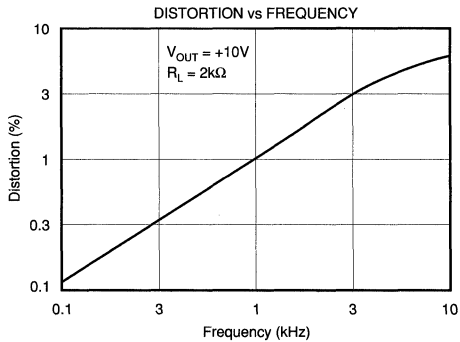
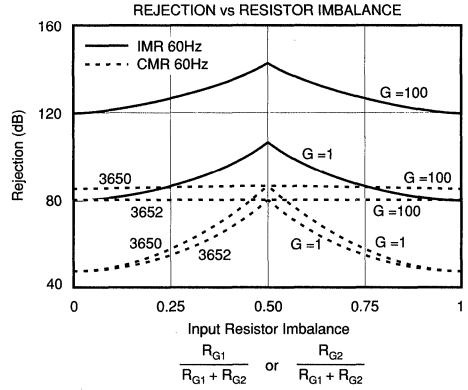
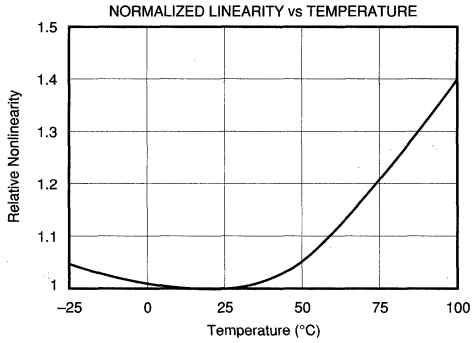
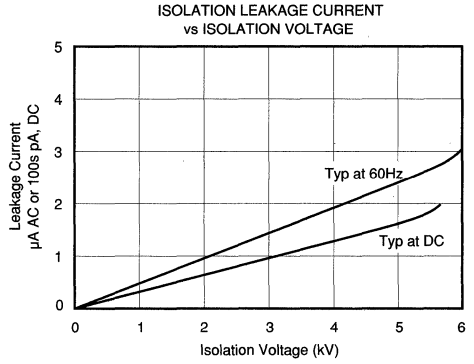
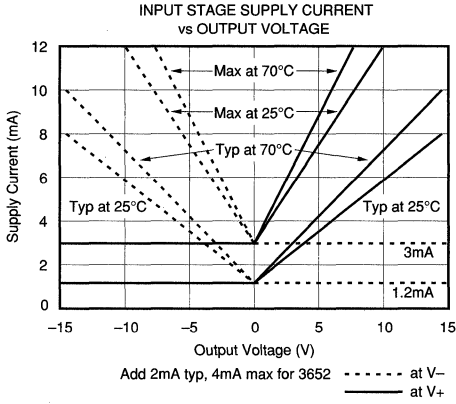
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ISOLATION AMPLIFIERS 3650/3652

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TYPICAL PERFORMANCE CURVES

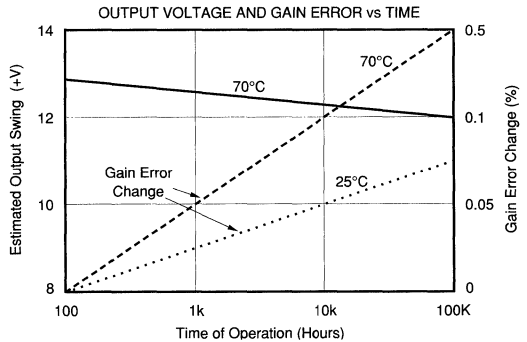
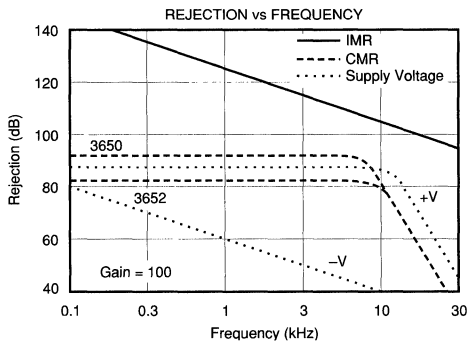
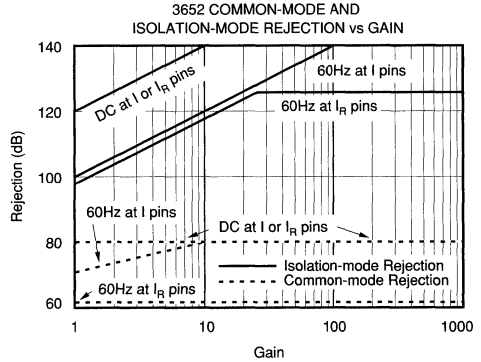
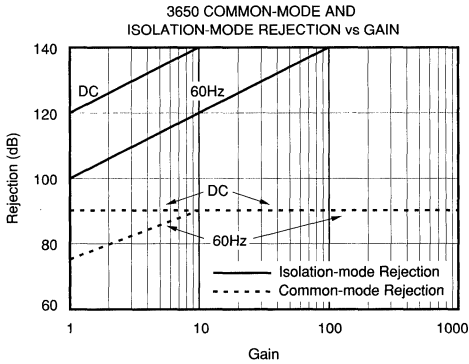
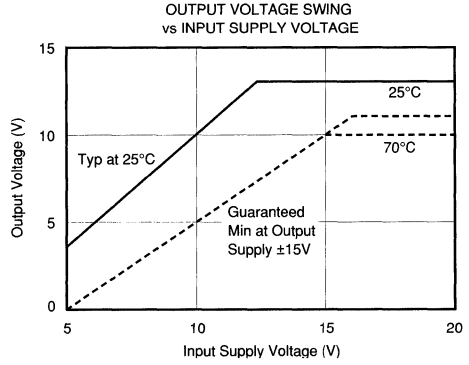
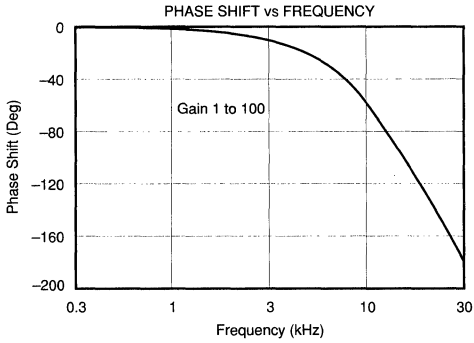
Typical at +25°C and ±15VDC power supplies, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

Typical at +25°C and ±15VDC power supplies, unless otherwise noted.



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ISOLATION AMPLIFIERS



DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications: "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is a generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and 3652, the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V, each unit is tested at 5000V.

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 1, $(V_+ + V_-)/2 = V_{CM}$. (NOTE: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as " V_{CM} " is negligible and the system "common-mode voltage" is applied to the amplifier as " V_{ISO} " in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

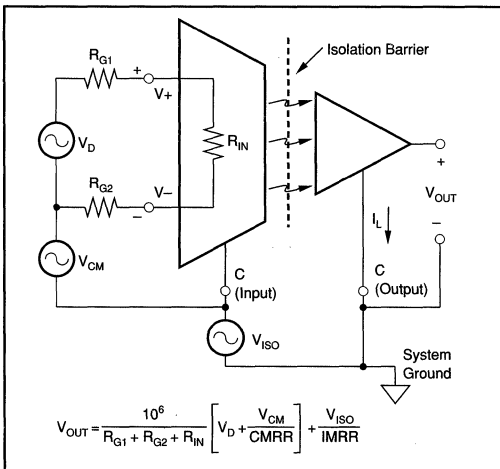


FIGURE 1. Illustration of Isolation-Mode and Common-Mode Specifications.

NOTE: (1) The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output (i.e. $\pm 10\text{mV}$ at $20\text{V}_{p-p} \approx 0.05\%$).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations—primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650, which can be used to understand the basic operation without considering the cluttering details of offset adjustment and biasing for bipolar operation.

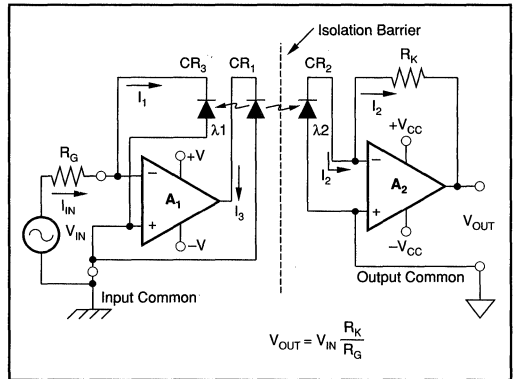


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used—one in the input (CR_3) and one in the output stage (CR_2)—to greatly reduce nonlinearities and time-temperature instabilities. Amplifier A_1 , LED CR_1 , and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{IN} R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched, and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{IN}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{OUT} = I_2 R_K$ where R_K is an internal $1\text{M}\Omega$ scaling resistor. Thus the overall transfer function is:

$$V_{OUT} = V_{IN} \frac{10^6}{R_G}, \quad (R_G \text{ in } \Omega\text{s})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched⁽¹⁾. Linearity is now a

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function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_D , whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used, the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{IN} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

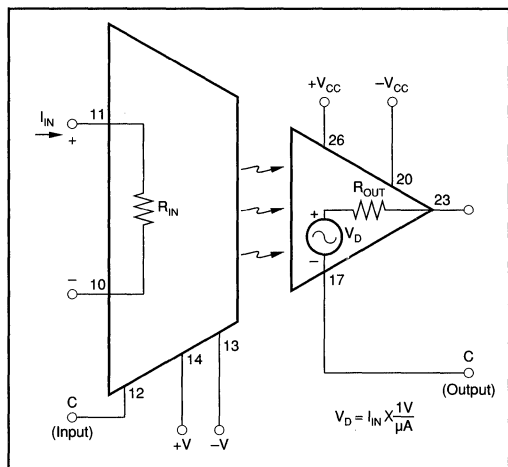


FIGURE 3. Simple Model of 3650.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$),

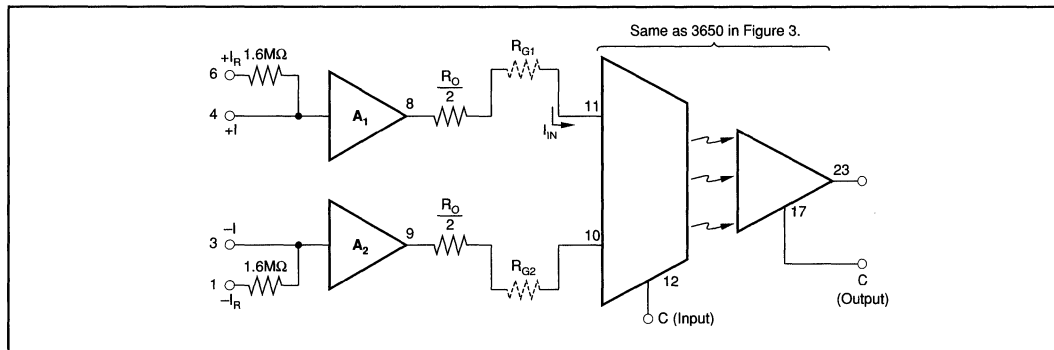


FIGURE 4. Simple Model of 3652.

lower bias currents (50pA) and overvoltage protection. The $+I_R$ and $-I_R$ inputs have a 10ms pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2} .

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC/DC converter is used for isolated power, it is placed in parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC/DC converter such as the Burr-Brown Model 722 should be used.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used: the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains, (>10).

Use the following procedure if it is desired to null both input and output components. (For example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

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ISOLATION AMPLIFIERS

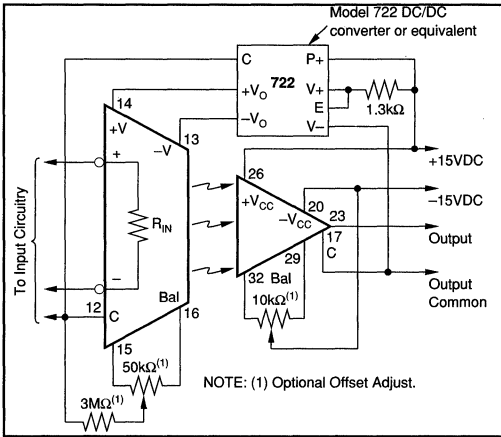


FIGURE 5. Power and Offset Adjust Connections.

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with nondifferential inputs, the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2} . As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used, it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers, A_1 and A_2 , are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential, and good common-mode and isolation-mode rejection). It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652, the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the $\pm I$ or $\pm I_R$ inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the $\pm I$ or $\pm I_R$ inputs. Figure 6c shows the $+I$ and $-I$ inputs used. If more input voltage protection is desired, then the $+I_R$ and $-I_R$ inputs should be used. This will increase the input noise due to the contribution from the $1.6M\Omega$ resistors, but will provide additional differential and common-mode protection (10ms rating of 3kV).

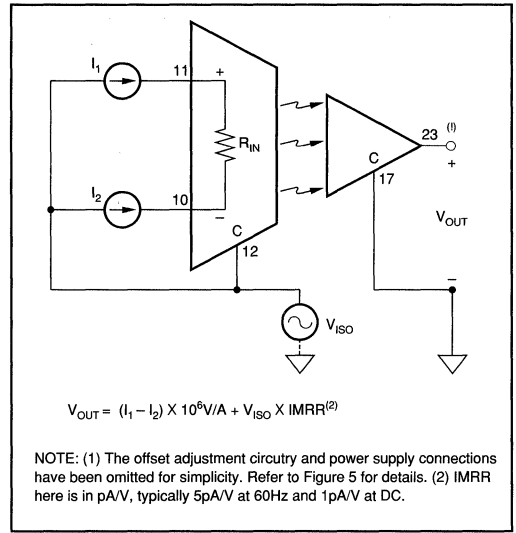


FIGURE 6a. 3650 with Differential Current Sources.

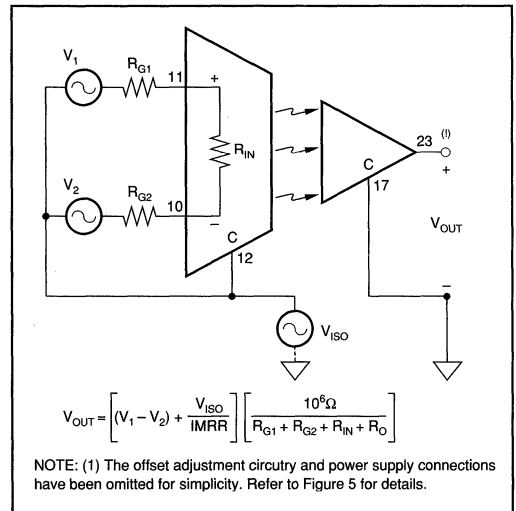


FIGURE 6b. 3650 with Differential Voltage Sources.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

A_1 and A_2 , the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{IN} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the

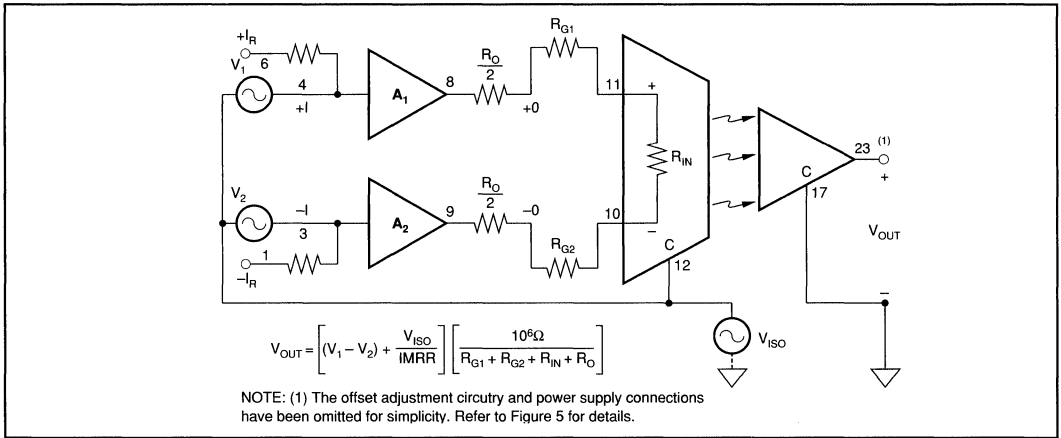


FIGURE 6c. 3652 with Differential Voltage Sources.

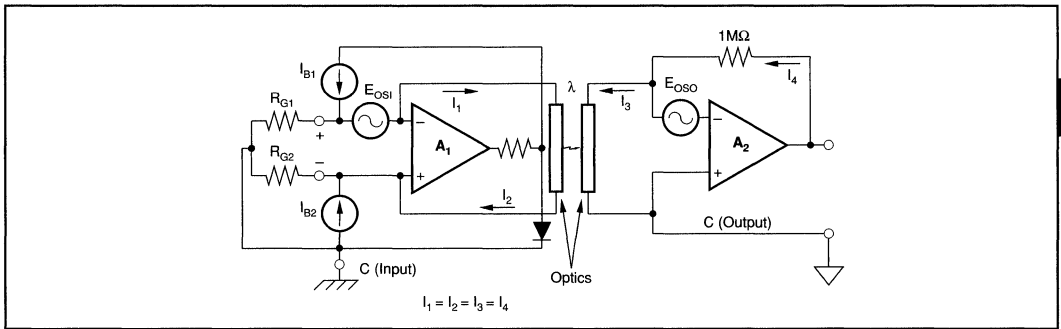


FIGURE 7. DC Error Analysis Model for 3650.

total output error voltage due to offset voltages and bias currents.

$$V_{OUT-TOTAL} = \frac{10^6}{R_{G1} + R_{G2}} [E_{OSI} + (I_{B1} R_{G1} - I_{B2} R_{G2})] + E_{OSO} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2} . If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{OSI}$

then, for $R_{G1} = R_{G2}$, $V_{OUT} - I_B = \frac{10^6 I_{OSI}}{2}$

This component of error is not a function of gain and is therefore included as a part of E_{OSO} specifications. The output errors due to the output stage bias current are also included in E_{OSO} . This results in a very simple equation for the total error:

$$V_{OUT-TOTAL} = \frac{10^6 E_{OSI}}{2R_{G1}} + E_{OSO} \quad (\text{for } R_{G1} = R_{G2}). \quad (2)$$

In summary, it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$$V_{OUT} \rightarrow \Delta V_{OUT}/\Delta T, E_{OSI} \rightarrow \Delta E_{OSI}/\Delta T, \text{ etc.}$$

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by:

$$E_N \text{ (RMS)} = \sqrt{(E_{NI}G)^2 + (E_{NO})^2}$$

where $E_N \text{ (RMS)}$ = Total output noise

E_{NI} = RMS noise of the input stage

E_{NO} = RMS noise of the output stage

$$G = 10^6/(R_{G1} + R_{G2})$$

E_{NO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE AND ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{OUT} = G \left[\frac{V_{CM}}{CMRR} + \frac{V_{ISO}}{IMRR} \right]$$

GUARDING AND PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted.

1. Use shielded twisted pair of cable at the input as with any instrumentation amplifier.
2. Care should be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR.
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

The armature current of the motor is converted to a voltage by the calibrated shunt R_s and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650s provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode impedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10ms pulse ratings of the $+I_R$ and $-I_R$ inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000Vpk continuous.

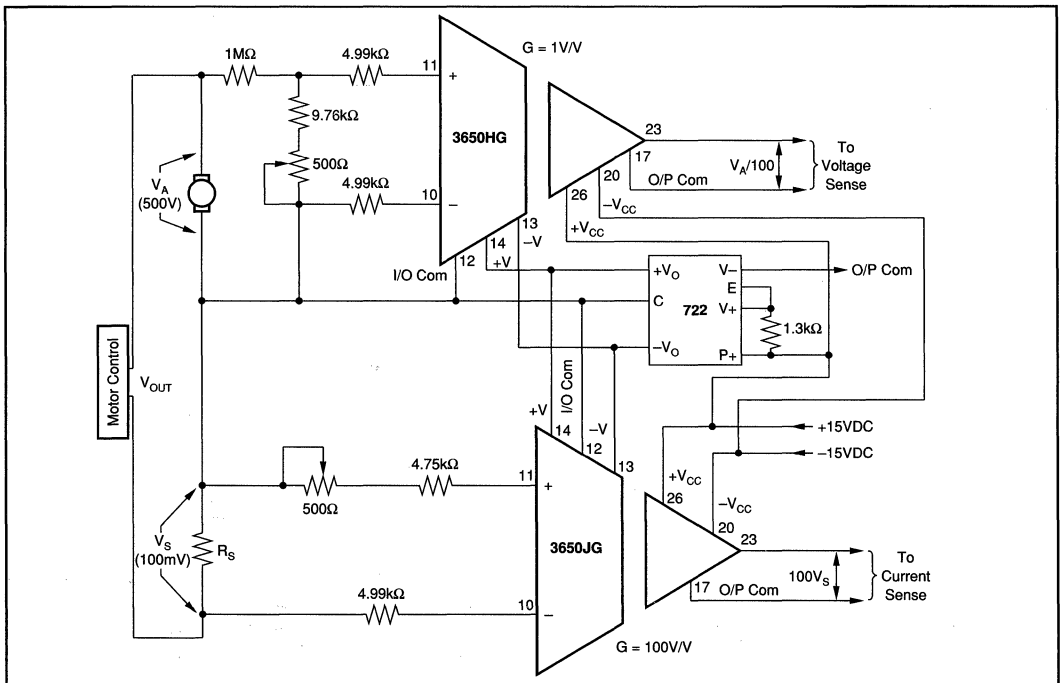


FIGURE 8. Isolated Armature Current and Voltage Sensor.

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ous. The nonrecurrent pulse rating of the isolation barrier is 5000Vpk, since each unit is factory tested at 5000Vpk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3652s can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V 60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

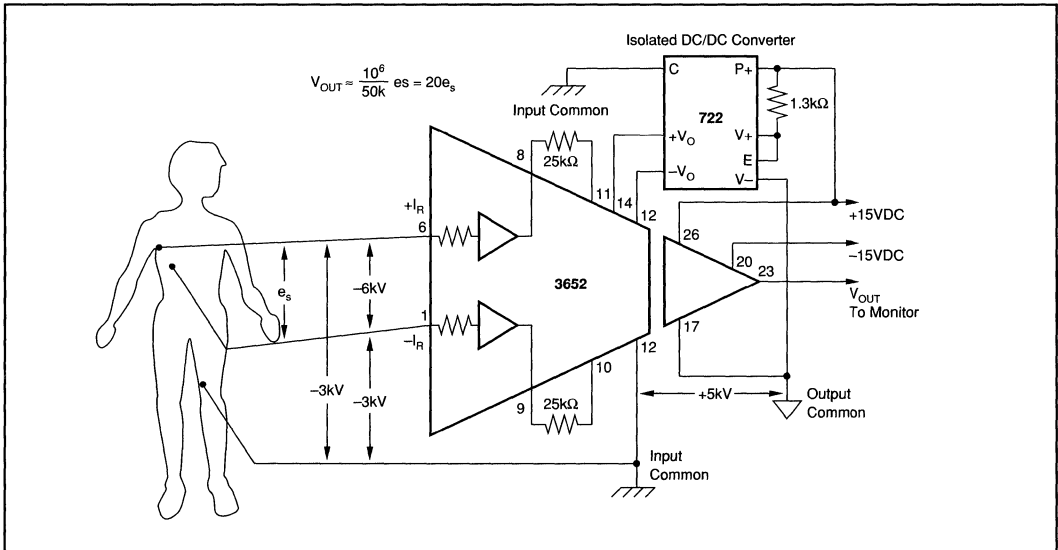


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

3650/3652

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ISOLATION AMPLIFIERS

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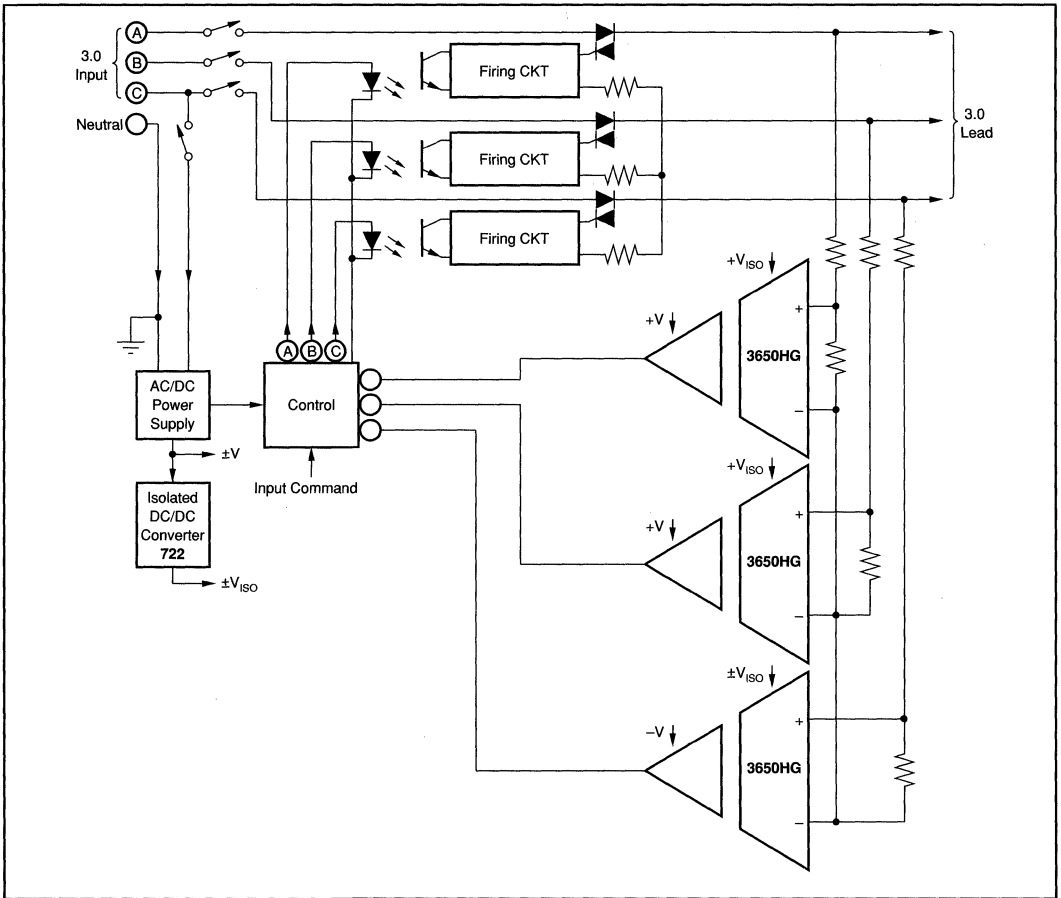
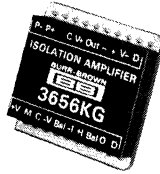


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

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3656

Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5 μ A MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- IMR: 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

APPLICATIONS

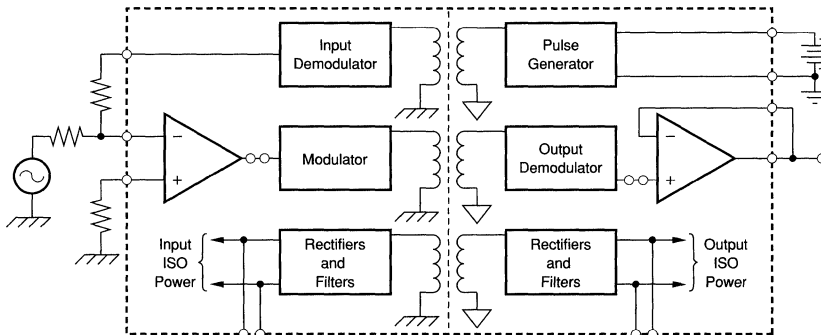
- MEDICAL
Patient Monitoring and Diagnostic Instrumentation
- INDUSTRIAL
Ground Loop Elimination and Off-ground Signal Measurement
- NUCLEAR
Input/Output/Power Isolation

DESCRIPTION

The 3656 was the first amplifier to provide a total isolation function, both signal and power isolation, in integrated circuit form. This remarkable advancement in analog signal processing capability was accomplished by use of a patented modulation technique and miniature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three

completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



This product is covered by the following United States patents: 4,066,974; 4,103,267; 4,082,908. Other patents pending may also apply upon the allowance and issuance of patents thereon. The product may also be covered in other countries by one or more international patents corresponding to the above-identified U.S. patents.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At +25°C, $V_{\pm} = 15\text{VDC}$ and 15VDC between P+ and P-, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous ⁽¹⁾ , DC		3500 (1000)			VDC
Test, 10s ⁽¹⁾		8000 (3000)			VDC
Test, 60s ⁽¹⁾		2000 (700)			Vrms
Rejection	$G_i = 10\text{V/V}$				
DC			160		dB
60Hz, < 100Ω in I/P Com ⁽²⁾			125		dB
60Hz, 5kΩ in I/P Com ⁽²⁾					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance ⁽¹⁾			6 (6.3)		pF
Resistance ⁽¹⁾			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	μA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial ⁽³⁾ 3656HG	$G < 100\text{V/V}$			1.5	%
3656AG, JG, KG				1	%
3656BG				0.3	%
vs Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2\text{M}\Omega$				
External Supplies Used at Pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies Used for Output Stage	Bipolar Output Voltage Swing, Full Load ⁽⁴⁾		±0.15		%
OFFSET VOLTAGE⁽⁵⁾, RTI					
Initial ⁽³⁾ , 3656HG	15Vp between P+ and P-			±[4 + (40/G _i)]	mV
3656AG, JG				±[2 + (20/G _i)]	mV
3656BG, KG				±[1 + (10/G _i)]	mV
vs Temperature, 3656HG				±[200 + (1000/G _i)]	μV/°C
3656JG				±[50 + (750/G _i)]	μV/°C
3656AG				±[25 + (500/G _i)]	μV/°C
3656KG				±[10 + (350/G _i)]	μV/°C
3656BG				±[5 + (350/G _i)]	μV/°C
vs Supply Voltage	Supply between P+ and P-			±[0.6 + (3.5/G _i)]	mV/V
3656HG				±[0.3 + (2.1/G _i)]	mV/V
3656AG, BG, JG, KG				±[0.2 + (20/G _i)]	mV/mA
vs Current ⁽⁶⁾			±[0.1 + (10/G _i)]		mV/mA
vs Time			±[10 + (100/G _i)] • (1 + log khrs.)		μV
AMPLIFIER PARAMETERS, Apply to A₁ and A₂					
Bias Current ⁽⁷⁾					
Initial				100	nA
vs Temperature			0.5		nA/°C
vs Supply			0.2		nA/V
Offset Current ⁽⁷⁾			5	20	nA
Impedance	Common-Mode		100 5		MΩ pF
Input Noise Voltage	$f_B = 0.05\text{Hz to }100\text{Hz}$		5		μVp-p
	$f_B = 10\text{Hz to }10\text{kHz}$		5		μVrms
Input Voltage Range ⁽⁸⁾					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply -5	V
Output Current	$V_{OUT} = \pm 5\text{V}$				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	$V_{OUT} = \pm 10\text{V}$				
	±15V External Supply	±2.5			mA
	$V_{OUT} = \pm 2\text{V}, V_{P+,P-} = 8.5\text{V}$				
	Internal Supply		±1		mA
Quiescent Current			150	450	μA

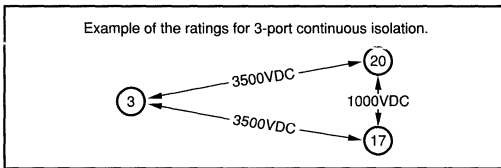
SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P-, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction Measured at Output to 0.05%	+0.1, -0.04			V/μs
Settling Time			500		μs
OUTPUT					
Noise Voltage (RTI)	f _B = 0.05Hz to 100Hz f _B = 10Hz to 10kHz		$\sqrt{(5)^2 + (22/G_s)^2}$ $\sqrt{(5)^2 + (11/G_s)^2}$		μVp-p μVrms
Residual Ripple ⁽⁹⁾			5		mVp-p
POWER SUPPLY IN, at P+, P- Rated Performance			15		VDC
Voltage Range ⁽¹⁰⁾	Derated Performance	8.5		16	VDC
Ripple Current ⁽⁹⁾			10	25	mAp-p
Quiescent Current ⁽¹¹⁾	Average		14	18	mA/DC
Current vs Load Current ⁽¹²⁾	vs Current from +V, -V, V+, V-		0.7		mA/mA
ISOLATED POWER OUT, At +V, -V, V+, V- pins⁽¹³⁾					
Voltage, No Load	15V Between P+ and P- ±15mA (10mA sum) Load ⁽¹²⁾	8.5	9	9.5	V
Voltage, Full Load	vs Supply Between P+ and P-	7	8	9	V
Voltage vs Power Supply Ripple Voltage ⁽⁹⁾			0.66		V/V
No Load			40		mVp-p
Full Load	±5mA Load		80	200	mVp-p
TEMPERATURE RANGE					
Specification 3656AG, BG		-25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation ⁽¹⁰⁾		-55		+100	°C
Storage ⁽¹⁴⁾		-65		+125	°C

NOTES: (1) Ratings in parenthesis are between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-. (2) See Performance Curves. (3) May be trimmed to zero. (4) If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used. (5) Includes effects of A₁ and A₂ offset voltages and bias currents if recommended resistors used. (6) Versus the sum of all external currents drawn from V+, V-, +V, -V (= ISO). (7) Effects of A₁ and A₂ bias currents and offset currents are included in Offset Voltage specifications. (8) With respect to I/P Com (pin 3) for A₁ and with respect to O/P Com (pin 17) for A₂. CMR for A₁ and A₂ is 100dB, typical. (9) In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 30kHz. (10) Decreases linearly from 16VDC at 85°C to 12VDC at 100°C. (11) Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50ms) and 300mA for fast rises (50μs). (12) Load current is sum drawn from +V, -V, V+, V- (= I_{ISO}). (13) Maximum voltage rating at pins 1 and 4 is ±18VDC; maximum voltage rating at pins 12 and 16 is ±18VDC. (14) Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.



PACKAGE INFORMATION⁽¹⁾

Model	Package	Package DRAWING NUMBER
3656	20-Lead ISO Omni	102A

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN DESIGNATIONS

NO.	DESCRIPTION	NO.	DESCRIPTION
1	+V	11	Output DEMOD
2	MOD Input	12	V-
3	Input DEMOD COM	13	A ₂ Noninverting Input
4	-V	14	A ₂ Inverting Input
5	Balance	15	A ₂ Output
6	A ₁ Inverting Input	16	V+
7	A ₁ Noninverting Input	17	Output DEMOD COM
8	Balance	18	No Pin
9	A ₁ Output	19	P+
10	Input DEMOD	20	P-

ABSOLUTE MAXIMUM RATINGS

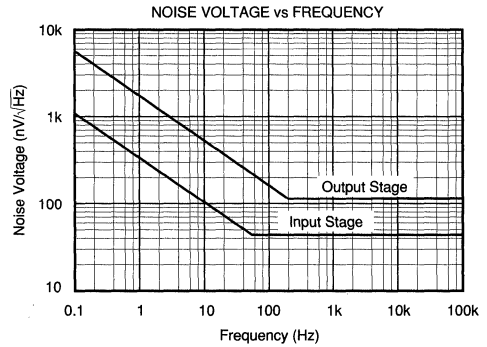
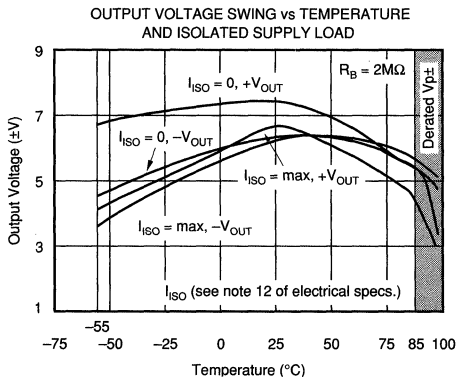
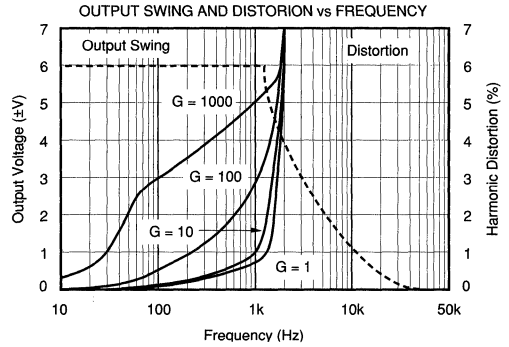
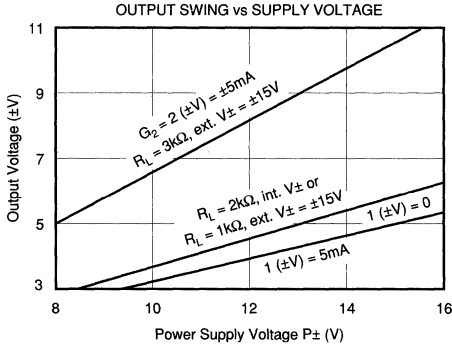
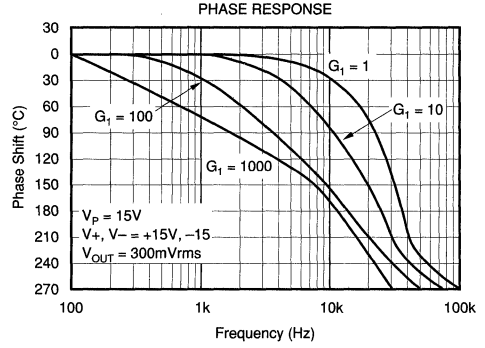
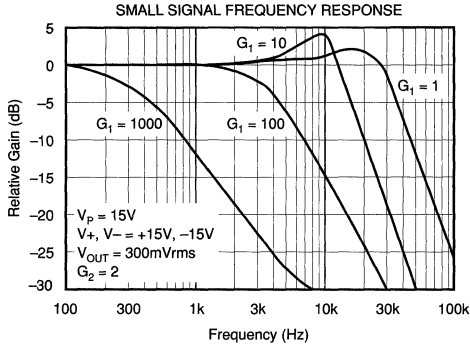
Supply Without Damage	16V
Input Voltage Range Using Internal Supply	±8V
Input Voltage Range Using External Supply	Supply
Continuous Isolation Voltage ⁽¹⁾	3500, (1000) VDC
Storage Temperature	-65°C to +125°C
Lead Temperature, (soldering, 10s)	+300°C

NOTE: (1) Ratings in parenthesis are between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-.

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TYPICAL PERFORMANCE CURVES

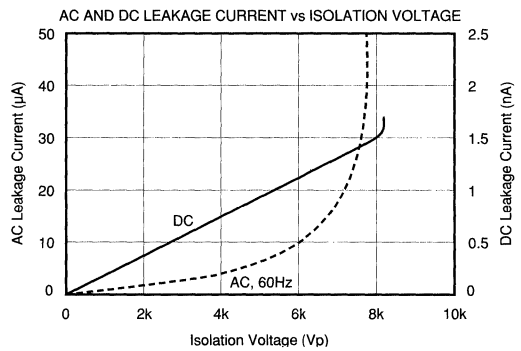
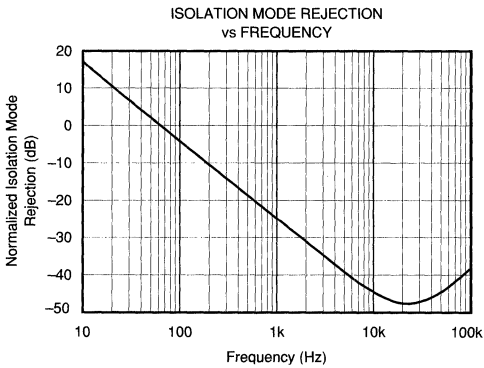
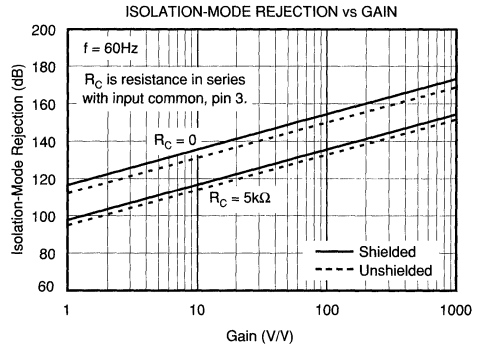
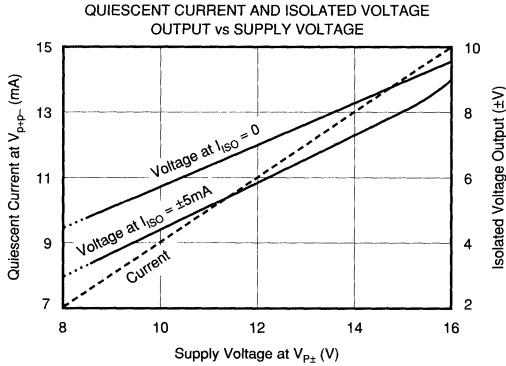
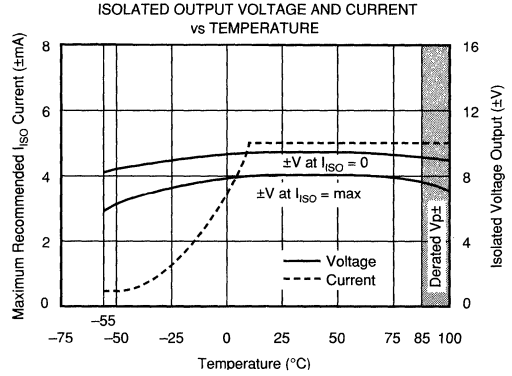
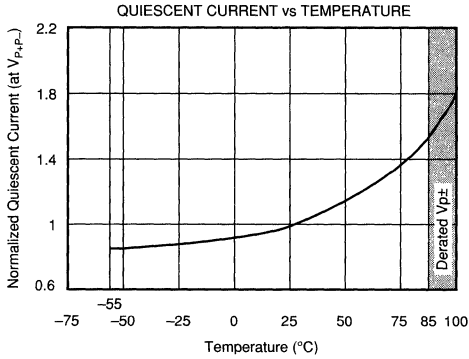
All specifications typical at +25°C, unless otherwise specified.



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TYPICAL PERFORMANCE CURVES (CONT)

All specifications typical at +25°C, unless otherwise specified.



3656

5

ISOLATION PRODUCTS

THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration—unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer, T_1 . One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages ($+V$, $-V$ and $V+$, $V-$). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators—one in the input stage and one in the output stage—which generate identical voltages at their outputs, pins 10 and 11 (Voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier, A_1 , the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage

at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100k Ω and a load resistor of 2M Ω or greater is recommended to prevent a voltage divider loading effect in excess of 5%.

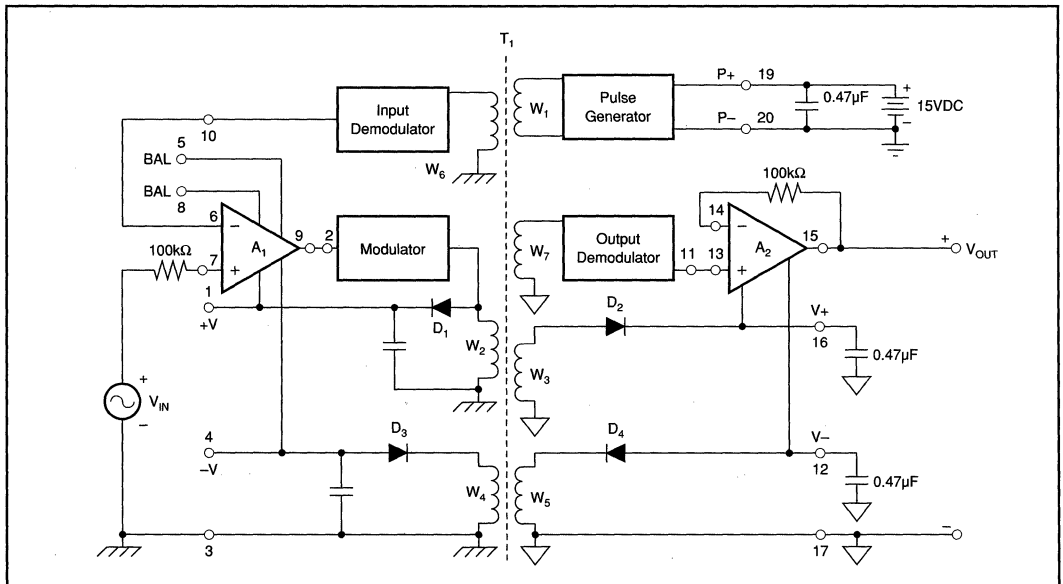


FIGURE 1. Block Diagram.

- Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the $2M\Omega$ level, a matching error of 5% will cause an additional gain error of 0.25%.
- Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with $2M\Omega$ load for a minimum of 5V.
- Total current drawn from the internal isolated supplies must be limited to less than $\pm 5\text{mA}$ per supply and limited to a total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, -V, V+ and V- pins should be limited to 5mA per supply (total current to +V, -V, V+ and V- limited to 10mA). The internal filter capacitors for $\pm V$ are $0.01\mu\text{F}$. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of $0.1\mu\text{F}/\text{mA}$ is recommended.
- The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
- Impedances seen by each amplifier's + and - input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a $100\text{k}\Omega$ output resistance, the amplifier input not connected to the demodulator should also see $100\text{k}\Omega$.
- All external filter capacitors should be mounted as close to the respective supply pins as possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5° . Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply volt-

ages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external $0.47\mu\text{F}$ capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

Two-Port Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or - could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 in its simplest gain configuration: unity gain noninverting. The two $100\text{k}\Omega$ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the output stage and noninverting gain in the input stage. The following equations apply:

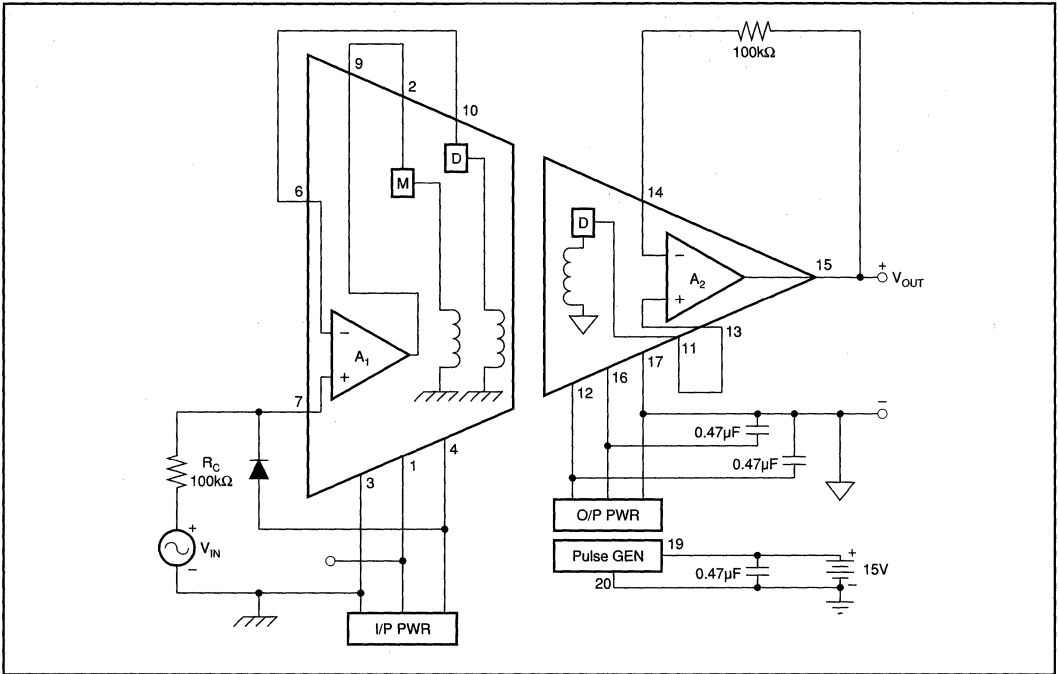


FIGURE 2. Power: Three-Port Isolation; Signal: Unity-Gain Noninverting.

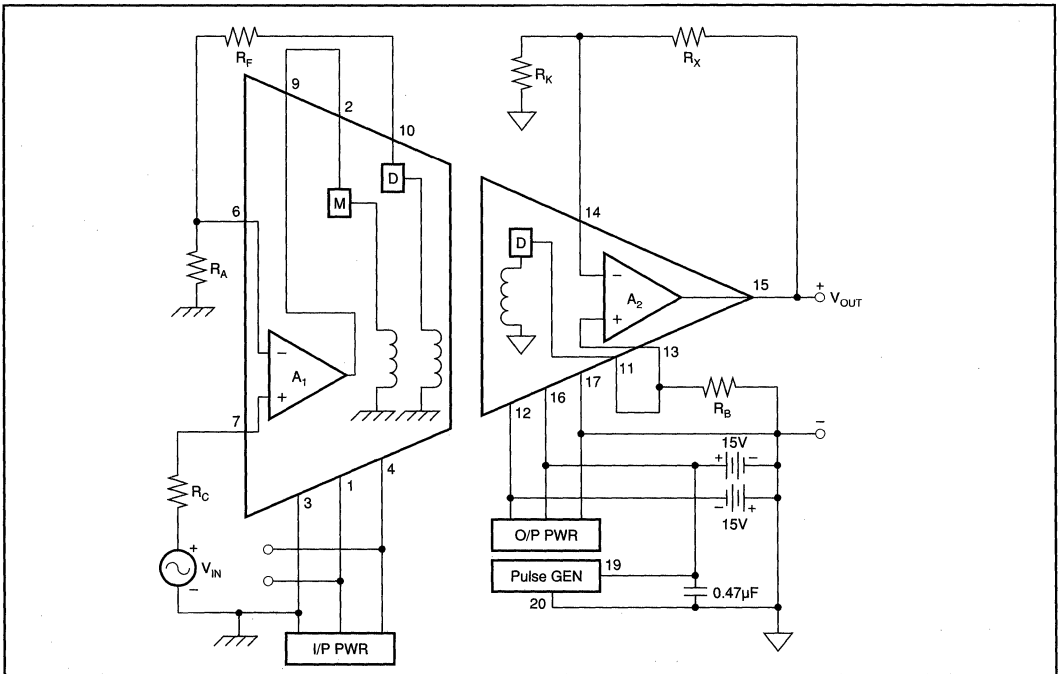


FIGURE 3. Power: Two-Port, Dual Supply; Signal: Noninverting Gain.

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Total amplifier gain:

$$G = G_1 \cdot G_2 = V_{OUT} / V_{IN} \quad (1)$$

Input Stage:

$$G_1 = 1 + (R_A / F_A) \quad (2)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit demodulator output to 5V).

$$R_A + R_F \geq 2M\Omega \quad (3)$$

(Select to load input demodulator with at least $2M\Omega$).

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A (R_F + 100k\Omega)}{R_A + R_F + 100k\Omega} \quad (4)$$

(Balance impedances seen by the + and - inputs of A_1 to reduce input offset caused by bias current).

Output Stage:

$$G_2 = 1 + (R_X / R_K) \quad (5)$$

(Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum).

$$R_X \parallel R_K = 100k\Omega \quad (6)$$

(Balance impedances seen by the + and - inputs of A_2 to reduce effect of bias current on the output offset).

$$R_B = R_A + R_F \quad (7)$$

(Load output demodulator equal to input demodulator).

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input, and voltage input.

Input Stage:

For the voltage input case:

$$G_1 = -R_F / R_S \quad (8)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V).

$$R_F = 2M\Omega \quad (9)$$

(Select to load the demodulator with at least $2M\Omega$).

$$R_C = R_S \parallel (R_1 + 100k\Omega) = \frac{R_S (R_F + 100k\Omega)}{R_S + R_F + 100k\Omega} \quad (10)$$

(Balance the impedances seen by the + and - inputs of A_1).

For the current input case:

$$V_{OUT} = -I_{IN} R_F \cdot G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than $2M\Omega$ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

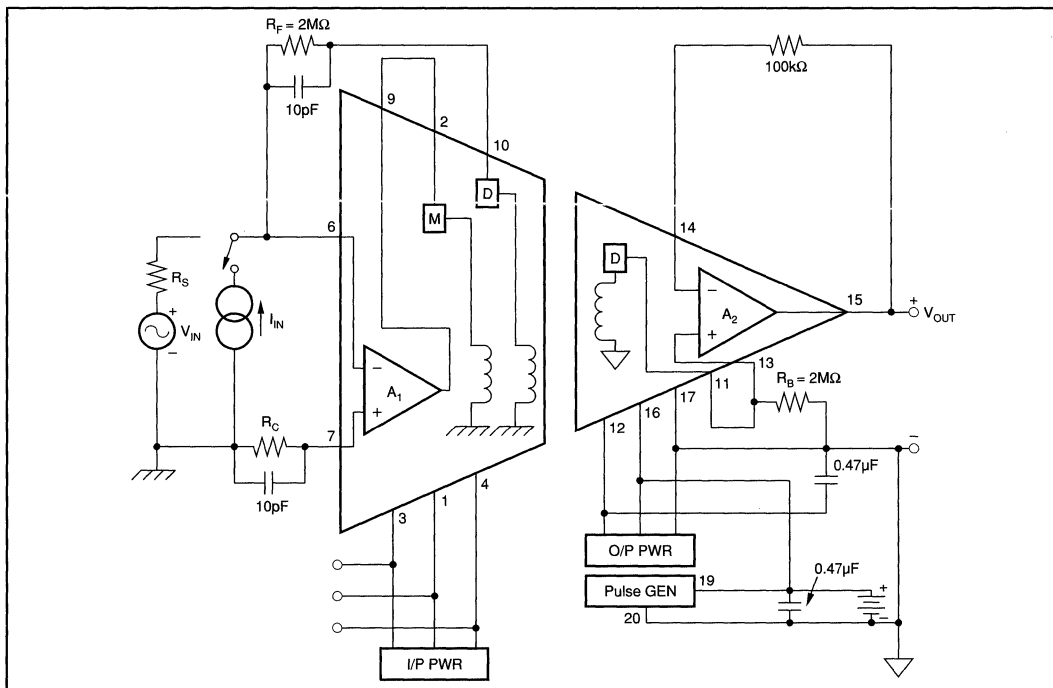


FIGURE 4. Power: Two-Port, Single Supply; Signal: Inverting Gains.



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Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Noninverting output is desired.

Input Stage:

Step 1

$$G_1 \text{ max} = 5V/\text{max Input Signal} = 5V / 0.1V = 50V/V$$

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select:

$$G_1 = 40V/V$$

$$G_1 = 1 + (R_F + R_A) = 40$$

$$\therefore R_F + R_A = 39 \quad (13)$$

Step 2

$R_A + R_F$ forms a voltage divider with the 100k Ω output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2M Ω . For most applications, the 2M Ω should be sufficiently large for $R_A + R_F$. Resistances greater than 2M Ω may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F = 2M\Omega$ is $2M\Omega / (2M\Omega + 100k\Omega) = 2 / (2 + 0.1) = 95.2\%$, i.e., the percent loading is 4.8%.

$$\text{Choose } R_A + R_F = 2M\Omega \quad (14)$$

Step 3

Solving equations (13) and (14)

$$R_A = 50k\Omega \text{ and } R_F = 1.95M\Omega$$

Step 4

The resistances seen by the + and - input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$$\begin{aligned} \therefore R_C &= R_A \parallel (R_F + 100k\Omega) \\ &= 50k\Omega \parallel (1.95M\Omega + 100k\Omega) \\ &\approx 49k\Omega \end{aligned}$$

Output Stage:

Step 5

$$V_{OUT} = V_{IN \text{ MAX}} \cdot G_1 \cdot G_2$$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$$\begin{aligned} \therefore V_{OUT} &= (1.25 \cdot 0.1)(G_1)(G_2) \\ \text{i.e., } 10V &= 0.125 \cdot 40 \cdot G_2 \\ \therefore G_2 &= 10V/5V = 2V/V \end{aligned}$$

Step 6

$$G_2 = 1 + (R_X/R_K) = 2.0$$

$$\therefore R_X/R_K = 1.0$$

$$\therefore R_X = R_K \quad (15)$$

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100k Ω of the output demodulator. The resistance seen by the (-) input terminal of A_2 (pin 14) should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K .

$$\begin{aligned} \therefore R_X \parallel R_K &= 100k\Omega \\ (R_X \cdot R_K / (R_X + R_K)) &= 100k\Omega \\ R_K / [1 + (R_K/R_X)] &= 100k\Omega \end{aligned} \quad (16)$$

Step 8

Solving equations (15) and (16) $R_K = 20k\Omega$ and $R_X = 200k\Omega$.

Step 9

The output demodulator must be loaded equal to the input demodulator.

$$\therefore R_B = R_A + R_F = 2M\Omega$$

(See equation (14) above in Step 2).

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_T = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable, but potentiometers should be stable.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_1 = R_B = 20M\Omega$, $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for $0V \pm 5mV$ or desired setting at V_{OUT} , pin 15.

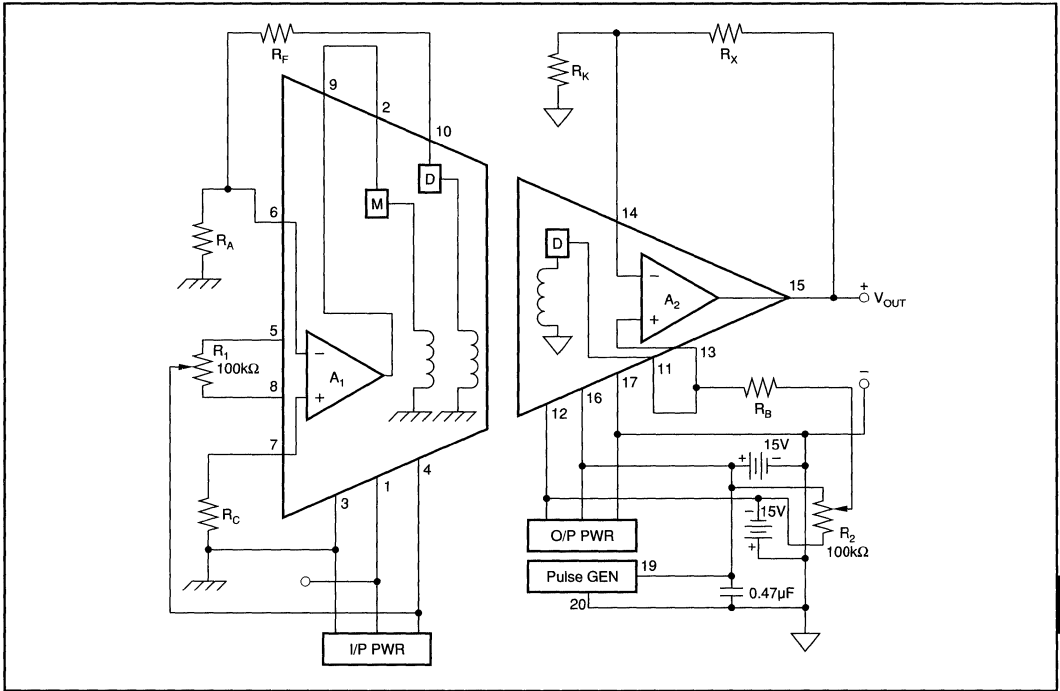


FIGURE 5. Optional Offset Voltage Trim.

Step 2: Output stage trim ($R_A = R_B = 20\text{M}\Omega$, $R_C = 100\text{k}\Omega$, $R_F = 0$, $R_X = 100\text{k}\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for $0\text{V} \pm 1\text{mV}$ or desired setting at V_{OUT} , pin 15 ($\pm 110\text{mV}$ approximate total range).

NOTE: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA177 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of -9 . R_1 and R_2 give the external amplifier a noninverting gain of $1 + 1/9$. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The $330\text{k}\Omega$, 1W , carbon resistors and diodes $D_1 - D_4$ provide protection for the input amplifiers from defibrillation pulses.

The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 ($68\text{M}\Omega/3\text{M}\Omega$). The high-

pass section (0.05Hz cutoff) is formed by the $1\mu\text{F}$ capacitor and $3\text{M}\Omega$ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the $68\text{M}\Omega$ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The $100\text{k}\Omega$ pot and the $100\text{M}\Omega$ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors, R_1 and R_2 , inverted, amplified, and fed back to the right-leg through resistor R_4 . This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3 . This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$$R_3 = (R_1/2) (V_O/V_{\text{CM}}) \text{ and } R_4 = (V_{\text{CM}} - V_O)/i_d$$

$$(-10\text{V} \leq V_O \leq +10\text{V} \text{ and } -10\text{V} \leq V_{\text{CM}} \leq +10\text{V})$$

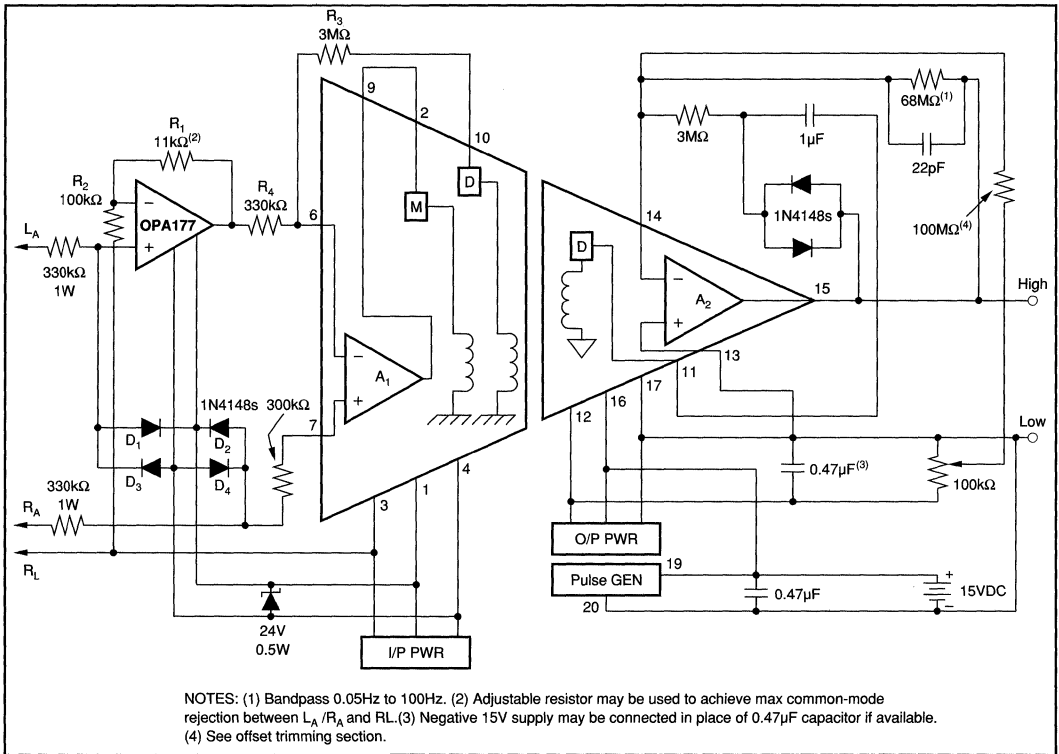


FIGURE 6. ECG Amplifier.

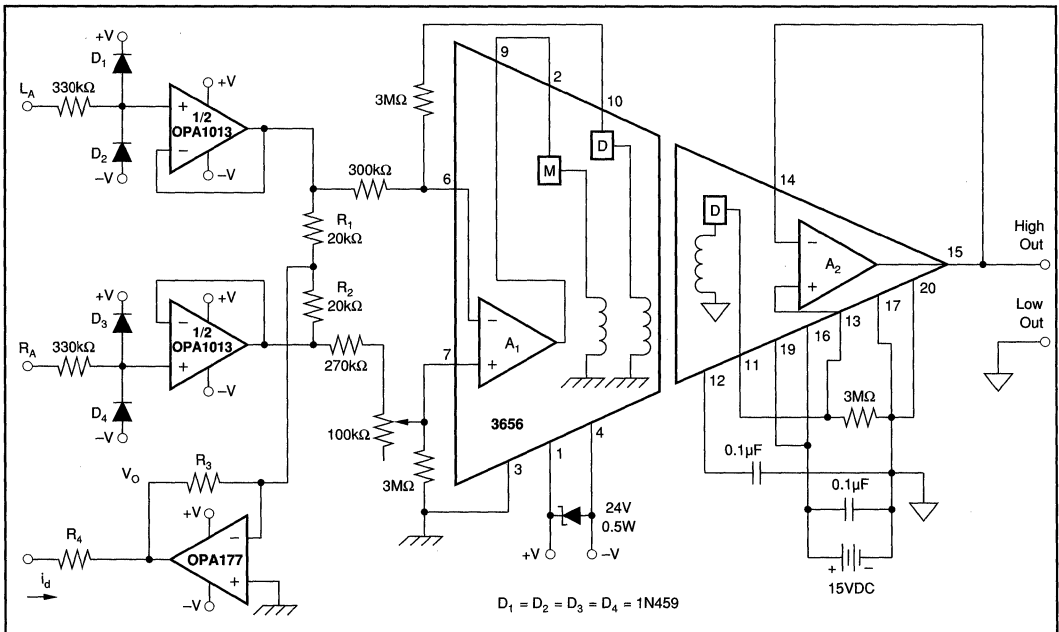


FIGURE 7. Driven Right-Leg Amplifier.

where V_O is the output voltage of A_3 , and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function—usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \cdot R_S}$$

$$I_{OUT} \leq \pm 2.5\text{mA}$$

$$V_i \leq \pm 4\text{V (compliance)}$$

$$R_L \leq 1.6\text{k}\Omega$$

$$R_F + R_A = R_1 + R_2 \leq 2\text{M}\Omega$$

CURRENT OUTPUT— LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown, a three-terminal regulator should

be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The “span” (gain) is adjusted by R_2 and the “zero” (4mA output for minimum input) is set by the 200k Ω pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2M Ω resistor used in

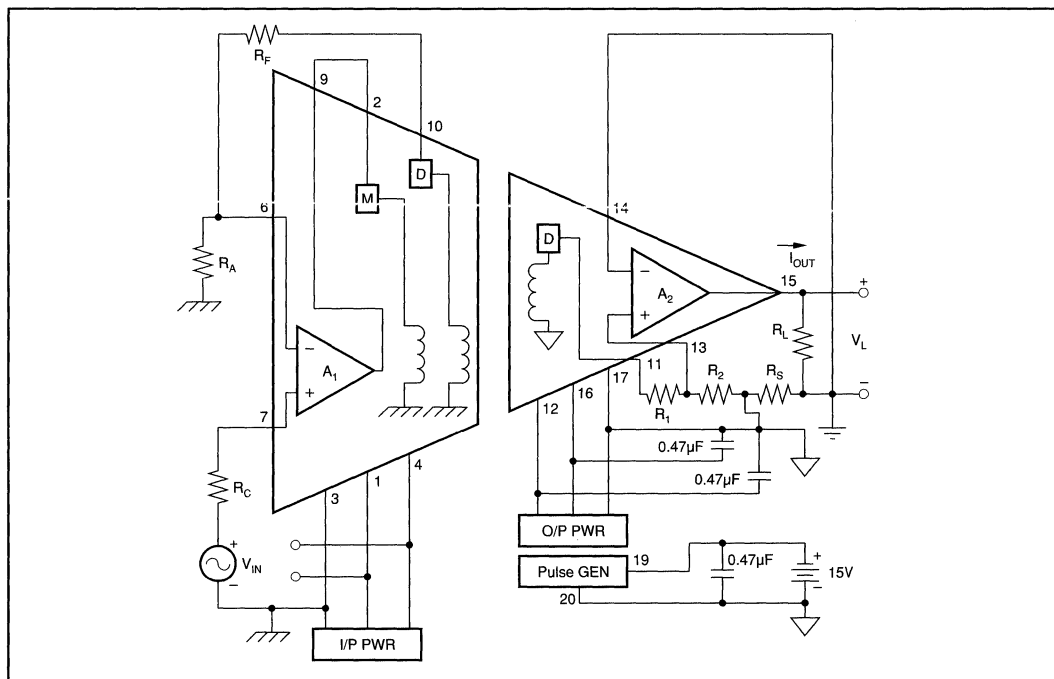


FIGURE 8. Bipolar Current Output.

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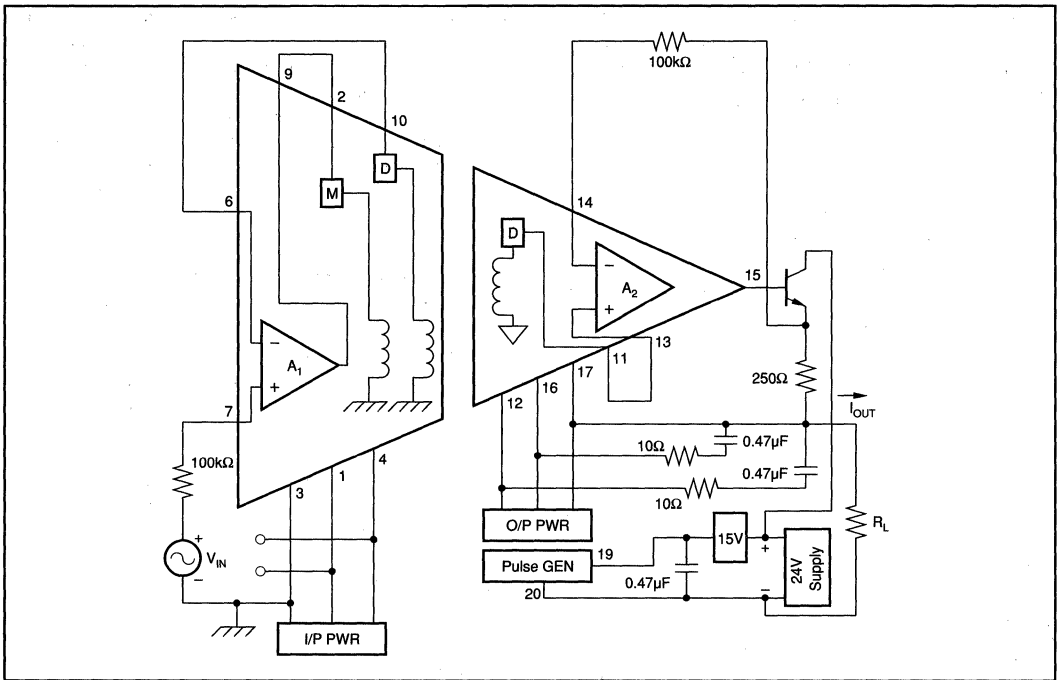


FIGURE 9. Isolated 1 to $5V_{IN}/4mA$ to $20mA I_{OUT}$

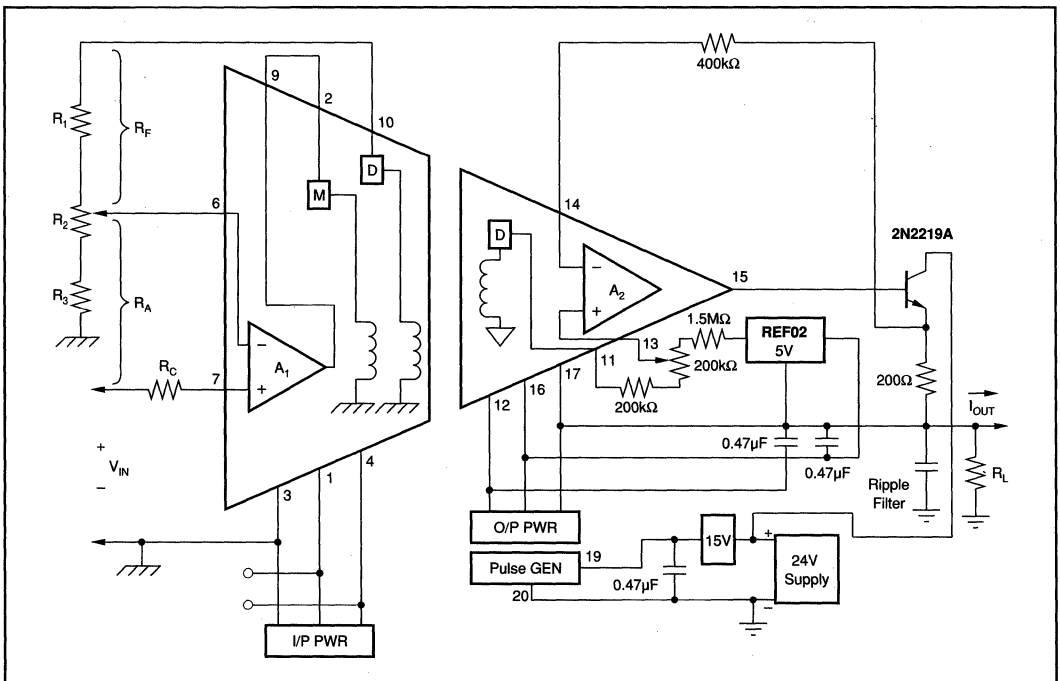


FIGURE 10. Isolated $4mA$ to $20mA I_{OUT}$

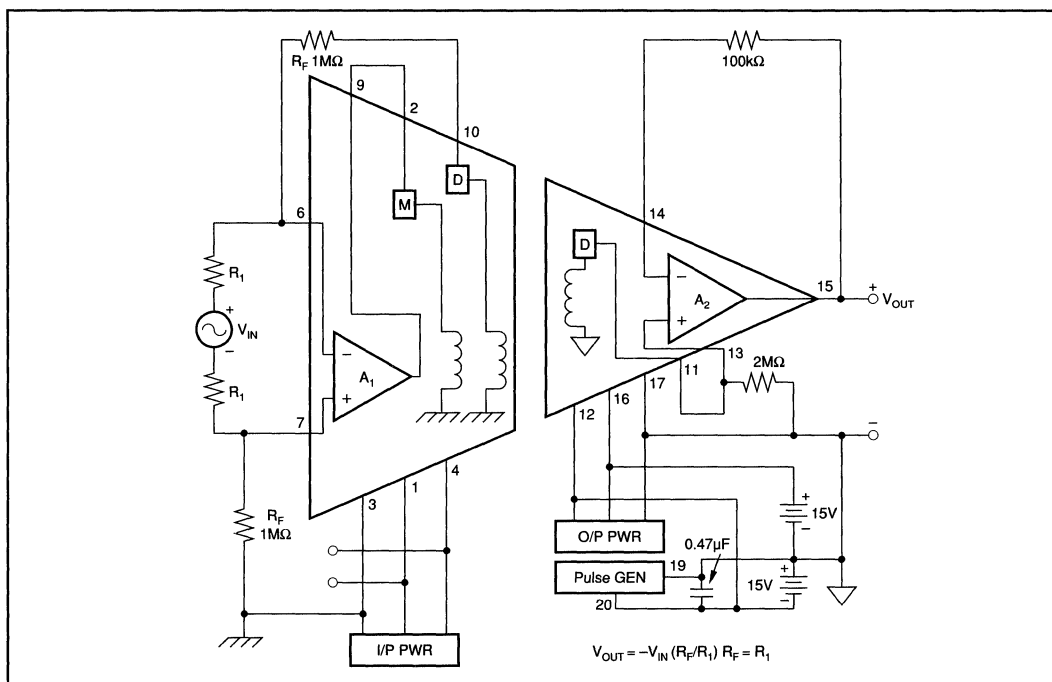


FIGURE 11. Differential Input, Floating Source.

the input stage is split into two halves, R_F and R_{F-} . The demodulator load (seen by pin 10 with respect to pin 3) is still $2M\Omega$ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides, it is possible to add a precision operational amplifier as shown

in Figure 13. Here the instrumentation grade OPA177 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the OPA177 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a significant amount of supply current, extra filtering of the input supply is required as shown ($2 \times 0.47\mu F$).

ELECTROMAGNETIC RADIATION

The transformer coupling used in 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications, the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

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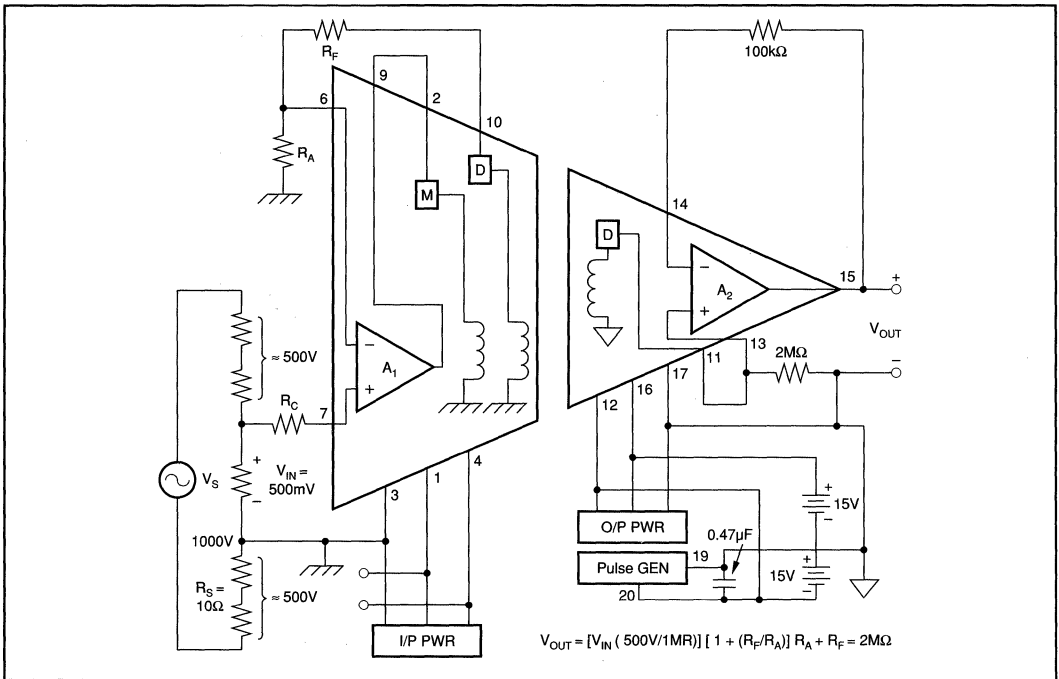


FIGURE 12. Series Source.

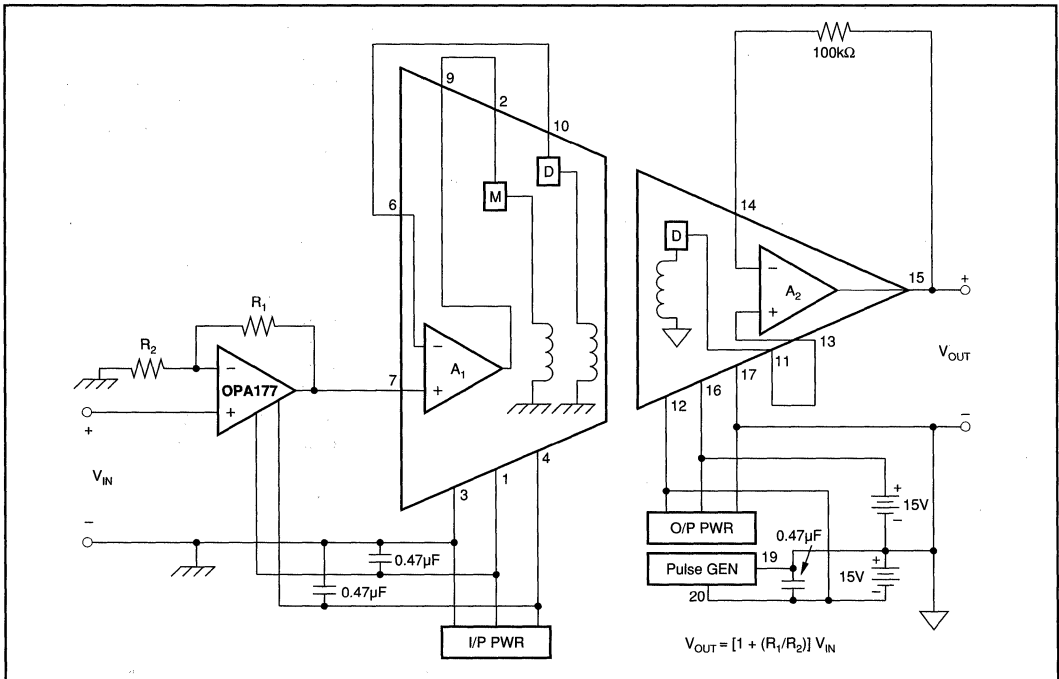


FIGURE 13. Isolator for Low-Level Signals.

6 Optical Sensors

Optical Electronic Integrated Sensors (OEICs) combine the building blocks traditionally used in a transimpedance amplifier on a single monolithic die. The photodiode; low noise, low bias current FET-input operational amplifier, and feedback network are matched to optimize performance.

Our monolithic sensor/amplifier combinations free designers from the tedious design rules necessary to optimize responsivity and speed while maintaining stability and minimal gain peaking in discrete solutions. Other errors that are reduced by a monolithic solution are leakage current errors and noise.

Light falling on the photodiode section of the die is converted to a current. The op amp is connected as a transimpedance amplifier, converting the photodiode current into an output voltage which is proportional to the intensity and wavelength of the light.

Several models and package options are available to allow flexibility in configuring light measurement systems. An external resistor can be placed

in series with the internal $1M\Omega$ to increase responsivity in all packages, or placed in parallel to reduce the overall responsivity (in all packages except the SIP).

OPT101—This device was designed to operate on a single power supply of +2.7V to +36V, with a quiescent current of only $120\mu A$ at dark. Response peaks at 850nm with a response of 0.6A/W.

OPT202—This is currently the fastest of Burr-Brown's OEICs with a 50kHz signal bandwidth. Available in clear plastic DIP and SIP packages, as well as a hermetic ceramic DIP.

OPT209—This device is available in plastic DIP, and will help to improve your signal-to-noise ratio in systems not needing the full 50kHz bandwidth of the OPT202.

OPT301—This OEIC is packaged in a hermetic TO-99 package with a glass window, and is specified over the extended industrial temperature range of $-40^{\circ}C$ to $+85^{\circ}C$. Offering a hermetic package and enhanced UV performance, the OPT301 has a 4kHz signal bandwidth.

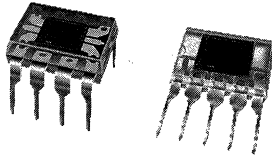
6 OPTICAL SENSORS

OPTICAL SENSORS **Boldface = NEW**

Model	Bandwidth (kHz)	Dark Errors (mV) Max	Quiescent Current at Dark (μA) Max	Power Supply (V)	Photodiode Size	DC Trans-impedance Gain (V/A) Typ	Responsivity at 650nm (A/W) Typ	Pkg	Page No.
OPT101P	20	$10^{(1)}$	+120	+2.7 to +36	0.09" x 0.09"	10^6	0.45	8-Pin PDIP	6.2
OPT101W	20	$10^{(1)}$	+120	+2.7 to +36	0.09" x 0.09"	10^6	0.45	5-Pin SIP	6.2
OPT202G	50	2	± 500	± 2.25 to ± 18	0.09" x 0.09"	10^6	0.45	8-Pin CERDIP	6.4
OPT202P	50	2	± 500	± 2.25 to ± 18	0.09" x 0.09"	10^6	0.45	8-Pin PDIP	6.4
OPT202W	50	2	± 500	± 2.25 to ± 18	0.09" x 0.09"	10^6	0.45	5-Pin SIP	6.4
OPT209P	16	2	± 500	± 2.25 to ± 18	0.09" x 0.09"	10^6	0.45	8-Pin PDIP	6.13
OPT301	4	2	± 500	± 2.25 to ± 18	0.09" x 0.09"	10^6	0.45	TO-99	6.24

NOTE: (1) Pedestal introduced for single supply operation.

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OPT101

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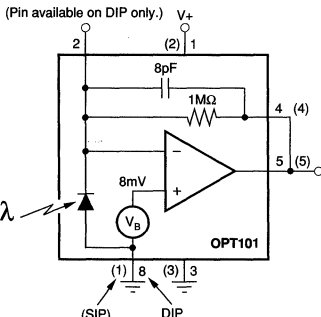
INTEGRATED PHOTODIODE AND SINGLE-SUPPLY AMPLIFIER

FEATURES

- SINGLE POWER SUPPLY:
+2.7 to +36V
- PHOTODIODE SIZE: 0.090 x 0.090 inch
(2.29 x 2.29mm)
- INTERNAL 1MΩ FEEDBACK RESISTOR
- HIGH PHOTODIODE RESPONSIVITY:
0.45A/W (650nm)
- LOW DARK ERRORS
- BANDWIDTH: 20kHz
- EXCELLENT SPECTRAL CHARACTERISTICS
- LOW QUIESCENT CURRENT: 120μA
- TRANSPARENT 8-PIN DIP AND 5-PIN SIP

APPLICATIONS

- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- BARCODE SCANNERS
- SMOKE DETECTORS



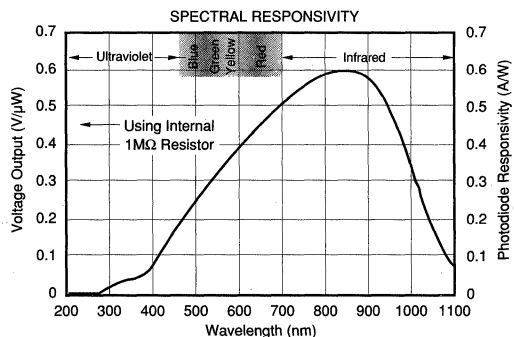
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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

DESCRIPTION

The OPT101 is a monolithic photodiode with on-chip transimpedance amplifier. The amplifier is designed for single or dual power supply operation, making it ideal for battery operated equipment.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance. The 0.09 x 0.09 inch photodiode is operated in the photoconductive mode for excellent linearity and low dark current.

The OPT101 operates over a wide supply range (+2.7V to +36V) and supply current is only 120μA. It is packaged in a transparent plastic 8-pin DIP and 5-pin SIP, specified for the 0°C to 70°C temperature range.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

$T_A = +25^\circ\text{C}$, $V_S = +2.7\text{V}$ to $+36\text{V}$, $\lambda = 650\text{nm}$, internal $1\text{M}\Omega$ feedback resistor, $R_L = 10\text{k}\Omega$ unless otherwise noted.

PARAMETER	CONDITIONS	OPT101P, W			UNITS
		MIN	TYP	MAX	
RESPONSIVITY Photodiode Current Voltage Output vs Temperature Unit to Unit Variation Nonlinearity ⁽¹⁾ Photodiode Area	650nm 650nm 650nm FS Output = 24V (0.090 x 0.090) (2.29 x 2.29)		0.45 0.45 100 ± 5 0.01 0.008 5.2		A/W V/ μW ppm/ $^\circ\text{C}$ % % of FS in ² mm ²
DARK ERRORS, RTO⁽²⁾ Offset Voltage, Output vs Temperature vs Power Supply Voltage Noise, Dark	$V_S = \pm 2.7\text{V}$ to $\pm 36\text{V}$ Dark, $f_b = 0.1\text{Hz}$ to 20kHz	+5	+7.5 ± 10 10 1	+10 100	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V/V}$ mVrms
TRANSIMPEDANCE GAIN Resistor Tolerance, P W vs Temperature			1 0.5 0.5 50	2	M Ω % % ppm/ $^\circ\text{C}$
FREQUENCY RESPONSE Bandwidth Rise Time, 10% to 90% Settling Time, 0.1% 1% 100% Overload Recovery, FS to Dark	$V_O = 10\text{Vp-p}$ FS to Dark Return to Linear Operation		20 20 140 45 50		kHz μs μs μs μs
OUTPUT Voltage Output, High Low Capacitive Load, Stable Operation Short-Circuit Current	Dark	(V+) - 1.3 5	(V+) - 1 7.5 10 15	10	V mV nF mA
POWER SUPPLY Operating Voltage Range Quiescent Current	Dark $R_L = \infty$, $V_O = 10\text{V}$	+2.7	120 220	+36 240	V μA μA
TEMPERATURE RANGE Specification Operating Storage Thermal Resistance, θ_{JA}		0 0 -25		+70 +70 +85	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

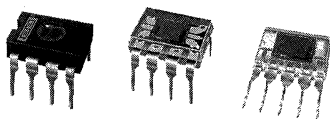
PHOTODIODE SPECIFICATIONS

$T_A = +25^\circ\text{C}$, $V_S = +2.7\text{V}$ to 36V unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT101P			UNITS
		MIN	TYP	MAX	
Photodiode Area	(0.090 x 0.090in) (2.29 x 2.29mm)		0.008		in ² mm ²
Current Responsivity	650nm		0.45 865		A/W $\mu\text{A/W}/\text{cm}^2$
Dark Current vs Temperature			2.5 doubles every 8°C		pA
Capacitance			1200		pF

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OPT202

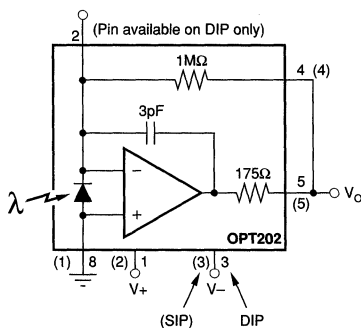
PHOTODIODE WITH ON-CHIP AMPLIFIER

FEATURES

- **BANDWIDTH:** 50kHz
- **PHOTODIODE SIZE:** 0.090 x 0.090 inch (2.29 x 2.29mm)
- **1MΩ FEEDBACK RESISTOR**
- **HIGH RESPONSIVITY:** 0.45A/W (650nm)
- **LOW DARK ERRORS:** 2mV
- **WIDE SUPPLY RANGE:** ±2.25 to ±18V
- **LOW QUIESCENT CURRENT:** 400μA
- **TRANSPARENT 8-PIN DIP AND 5-PIN SIP**
- **HERMETIC 8-PIN CERAMIC DIP**

APPLICATIONS

- **MEDICAL INSTRUMENTATION**
- **LABORATORY INSTRUMENTATION**
- **POSITION AND PROXIMITY SENSORS**
- **PHOTOGRAPHIC ANALYZERS**
- **SMOKE DETECTORS**

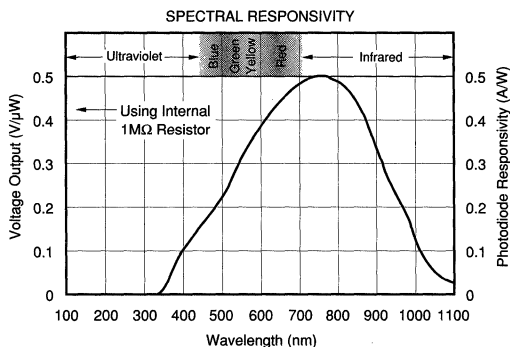


DESCRIPTION

The OPT202 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT202 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400μA. It is packaged in a transparent plastic 8-pin DIP or 5-pin SIP, specified for the 0°C to +70°C temperature range as well as a hermetic ceramic 8-pin DIP with a glass window, specified for the -40°C to +85°C temperature range.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, internal $1\text{M}\Omega$ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT202P, W, G			UNITS
		MIN	TYP	MAX	
RESPONSIVITY					
Photodiode Current	650nm		0.45		A/W
Voltage Output	650nm		0.45		V/ μW
vs Temperature			100		ppm/ $^\circ\text{C}$
Unit-to-Unit Variation	650nm		± 5		%
Nonlinearity ⁽¹⁾	FS Output = 10V (0.090 x 0.090in)		0.01		% of FS
Photodiode Area	(2.29 x 2.29mm)		0.008		in ²
			5.2		mm ²
DARK ERRORS, RTO⁽²⁾					
Offset Voltage, Output: P, W Packages			± 0.5	± 2	mV
G Package			± 0.5	± 3	mV
vs Temperature			± 10		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		10	100	$\mu\text{V}/\text{V}$
Voltage Noise	Measured BW = 0.1Hz to 100kHz		1		mVrms
RESISTOR—1MΩ Internal					
Resistance			1		M Ω
Tolerance: P, G Packages			± 0.5	± 2	%
W Package			± 0.5		%
vs Temperature			50		ppm/ $^\circ\text{C}$
FREQUENCY RESPONSE					
Bandwidth, Large or Small-Signal, -3dB			50		kHz
Rise Time, 10% to 90%			10		μs
Settling Time, 1%	FS to Dark		10		μs
0.1%	FS to Dark		20		μs
0.01%	FS to Dark		40		μs
Overload Recovery Time (to 1%)	100% Overdrive, $V_S = \pm 15\text{V}$		44		μs
	100% Overdrive, $V_S = \pm 5\text{V}$		100		μs
	100% Overdrive, $V_S = \pm 2.25\text{V}$		240		μs
OUTPUT					
Voltage Output	$R_L = 10\text{k}\Omega$	(V+) - 1.25	(V+) - 1		V
	$R_L = 5\text{k}\Omega$	(V+) - 2	(V+) - 1.5		V
Capacitive Load, Stable Operation			10		nF
Short-Circuit Current			± 18		mA
POWER SUPPLY					
Specified Operating Voltage			± 15		V
Operating Voltage Range		± 2.25		± 18	V
Quiescent Current	$V_O = 0$		± 400	± 500	μA
TEMPERATURE RANGE					
Specification: P, W Packages		0		+70	$^\circ\text{C}$
G Package		-40		+85	$^\circ\text{C}$
Operating: P, W Packages		0		+70	$^\circ\text{C}$
G Package		-55		+125	$^\circ\text{C}$
Storage: P, W Packages		-25		+85	$^\circ\text{C}$
G Package		-55		+125	$^\circ\text{C}$
Thermal Resistance, θ_{JA}			100		$^\circ\text{C}/\text{W}$

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

OPT202

6

OPTICAL SENSORS

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SPECIFICATIONS (CONT)

ELECTRICAL

Op Amp Section of OPT202⁽¹⁾

T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	OPT202 Op Amp			UNITS
		MIN	TYP	MAX	
INPUT					
Offset Voltage vs Temperature	V _S = ±2.25V to ±18V		±0.5		mV
vs Power Supply			±5		μV/°C
Input Bias Current vs Temperature			10		μV/V
			1		pA
			doubles every 10°C		
NOISE					
Input Voltage Noise					
Voltage Noise Density, f = 10Hz			30		nV/√Hz
f = 100Hz			25		nV/√Hz
f = 1kHz			15		nV/√Hz
Current Noise Density, f = 1kHz			0.8		fA/√Hz
INPUT VOLTAGE RANGE					
Common-mode Input Range			±14.4		V
Common-mode Rejection			106		dB
INPUT IMPEDANCE					
Differential			10 ¹² 3		Ω pF
Common-mode			10 ¹² 3		Ω pF
OPEN-LOOP GAIN					
Open-loop Voltage Gain			120		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			16		MHz
Slew Rate			6		V/μs
Settling Time 0.1%			4		μs
0.01%			5		μs
OUTPUT					
Voltage Output	R _L = 10kΩ	(V ₊) - 1.25	(V ₊) - 1		V
Short-Circuit Current	R _L = 5kΩ	(V ₊) - 2	(V ₊) - 1.5		V
			±18		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±2.25		±18	V
Quiescent Current	I _O = 0		±400	±500	μA

NOTE: (1) Op amp specifications provided for information and comparison only.

PHOTODIODE SPECIFICATIONS

T_A = +25°C, unless otherwise noted.

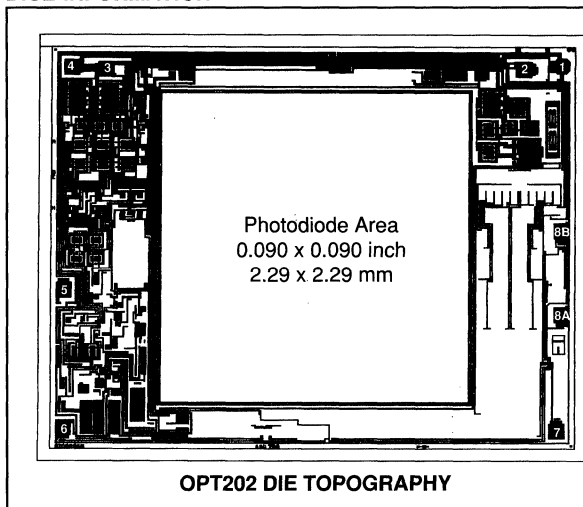
PARAMETER	CONDITIONS	Photodiode of OPT202			UNITS
		MIN	TYP	MAX	
Photodiode Area	(0.090 × 0.090in) (2.29 × 2.29mm)		0.008		in ² mm ²
Current Responsivity	650nm		5.2		A/W
Dark Current	V _D = 0V ⁽¹⁾		0.45		fA
vs Temperature			500		fA
Capacitance	V _D = 0V ⁽¹⁾		doubles every 10°C		
			600		pF

NOTE: (1) Voltage Across Photodiode.

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DICE INFORMATION



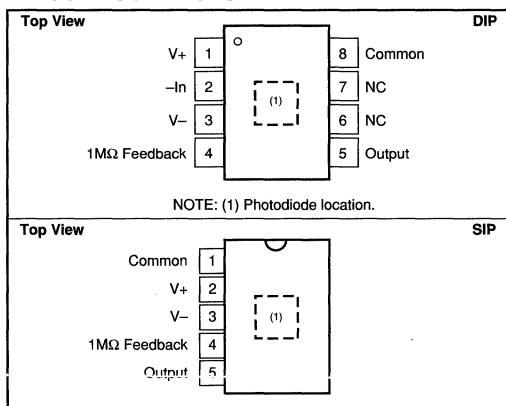
PAD	FUNCTION
1	V+
2	-In
3	V-
4	1MΩ Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 ±5	3.91 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATIONS



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



MOISTURE SENSITIVITY AND SOLDERING

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT202 plastic packages cannot meet flammability test, UL-94.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range (Common Pin)	±V _s
Output Short-Circuit (to ground)	Continuous
Operating Temperature: P, W	-25°C to +85°C
G	-55°C to +125°C
Storage Temperature: P, W	-25°C to +85°C
G	-55°C to +125°C
Junction Temperature: P, W	+85°C
G	+150°C
Lead Temperature (soldering, 10s)	+300°C
(Vapor-Phase Soldering Not Recommended on Plastic Packages)	

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPT202P	8-Pin Plastic DIP	006-1
OPT202W	5-Pin Plastic SIP	321
OPT202G	8-Pin Ceramic DIP	161-1

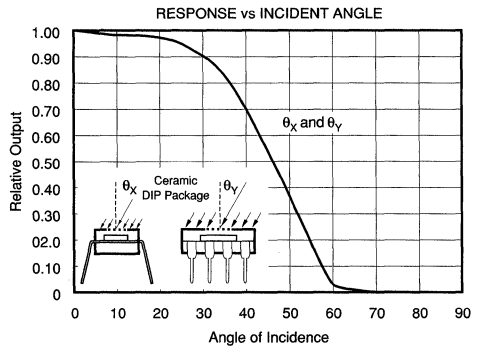
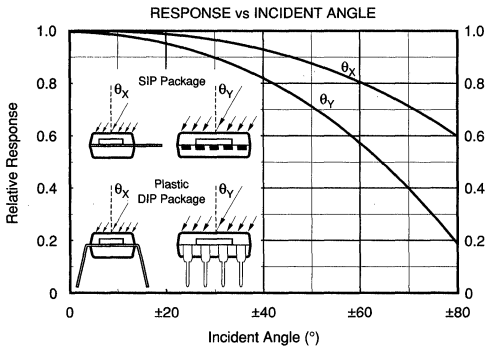
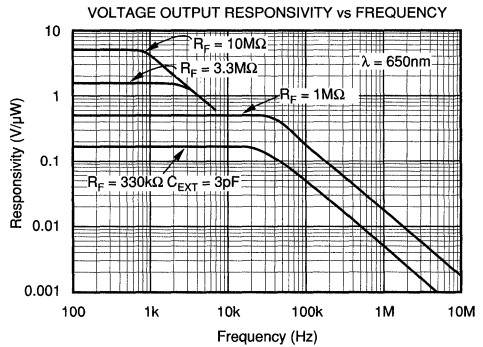
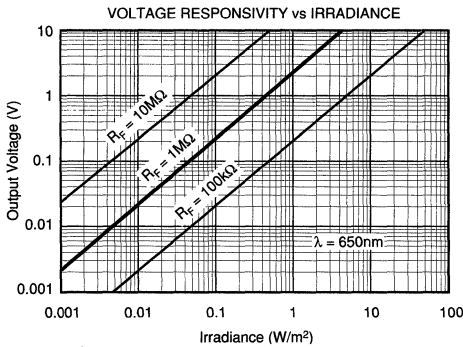
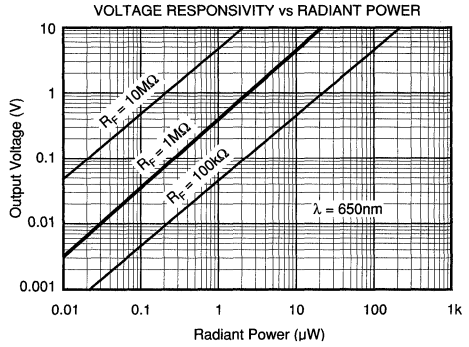
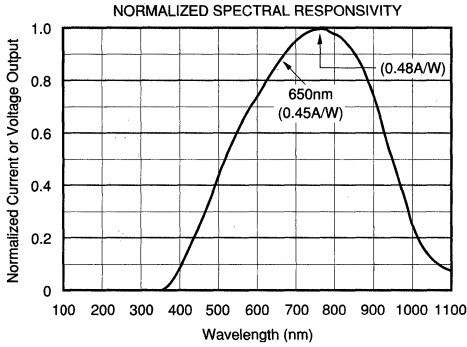
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



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TYPICAL PERFORMANCE CURVES

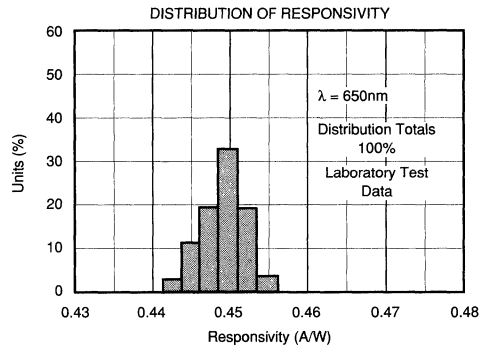
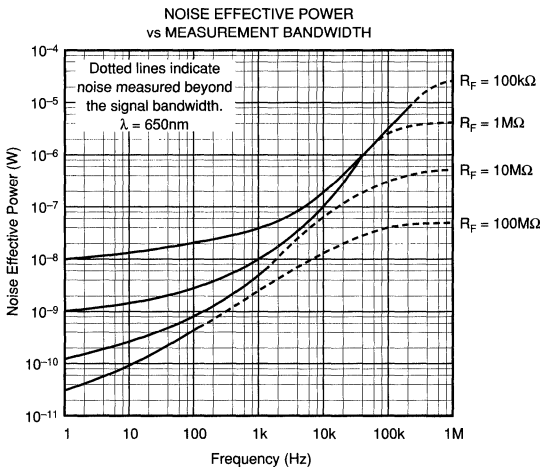
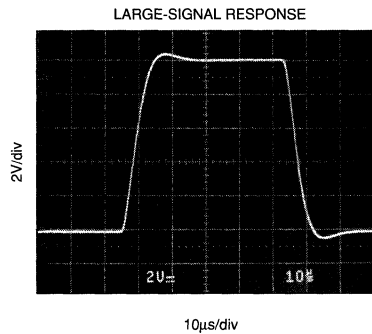
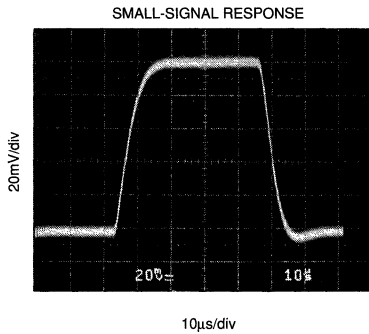
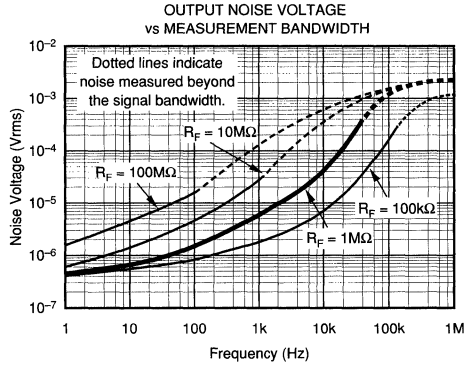
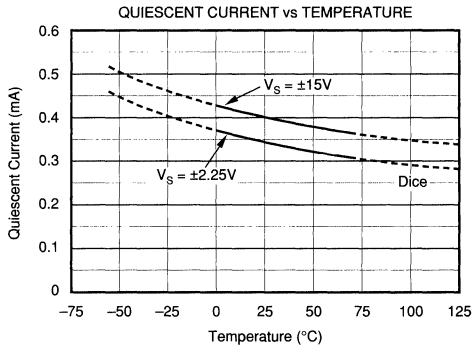
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT202. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown. Output is zero volts with no light and increases with increasing illumination.

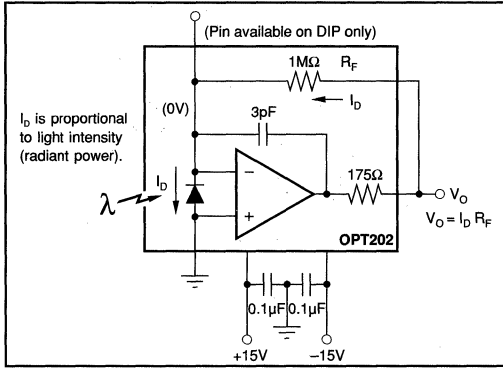


FIGURE 1. Basic Circuit Connections.

Photodiode current, I_D , is proportional to the radiant power or flux (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode Responsivity, R_F , is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.23 \times 10^{-6} \text{m}^2$.

The OPT202's voltage output is the product of the photodiode current times the feedback resistor, ($I_D R_F$). The internal feedback resistor is laser trimmed to $1\text{M}\Omega \pm 2\%$. Using this resistor, the output voltage responsivity, R_V , is approximately $0.45\text{V}/\mu\text{W}$ at 650nm wavelength.

An external resistor can be connected to set a different voltage responsivity. Best dynamic performance is achieved by connecting R_{EXT} in series (for $R_F > 1\text{M}\Omega$), or in parallel (for $R_F < 1\text{M}\Omega$), with the internal resistor as shown in Figure 2. Placing the external resistor in parallel with the internal resistor takes advantage of on-chip capacitive guarding of the internal resistor, which improves dynamic performance. For values of R_F less than $1\text{M}\Omega$, an external capacitor, C_{EXT} , should be connected in parallel with R_F (see Figure 2). This capacitor eliminates gain peaking and prevents instability. The value of C_{EXT} can be read from the table in Figure 2.

LIGHT SOURCE POSITIONING

The OPT202 is 100% tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although all IC amplifiers are light-sensitive to some degree, the OPT202 op amp circuitry is designed to

minimize this effect. Sensitive junctions are shielded with metal, and differential stages are cross-coupled. Furthermore, the photodiode area is very large relative to the op amp input circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT202 would not perform properly. The large (0.090 x 0.090 inch) photodiode area allows easy positioning of narrowly focused light sources. The photodiode area is easily visible—it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffused by the side of the package. These effects are shown in the typical performance curve "Response vs Incident Angle."

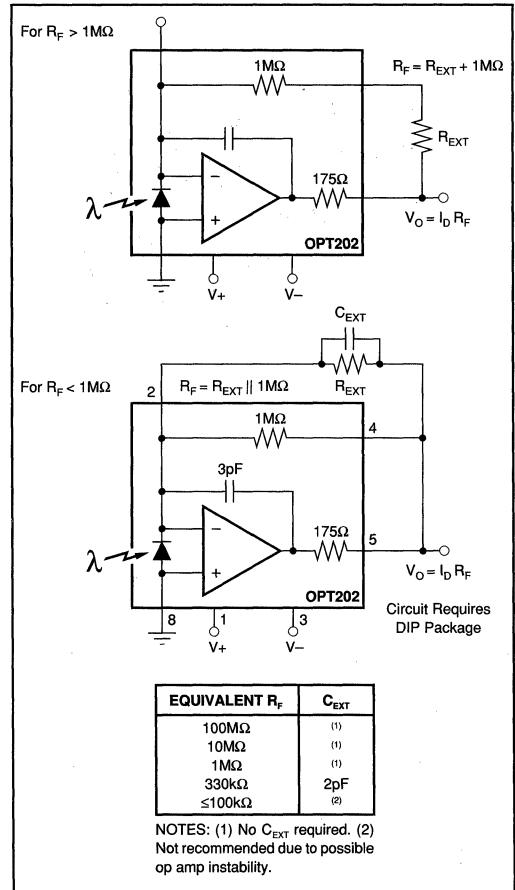


FIGURE 2. Using External Feedback Resistor.

DARK ERRORS

The dark errors in the specification table include all sources. The dominant error source is the input offset voltage of the op amp. Photodiode dark current and input bias current of the op amp are in the 2pA range and contribute virtually no offset error at room temperature. Dark current and input bias current double for each 10°C above 25°C. At 70°C, the error current can be approximately 100pA. This would produce a 1mV offset with $R_F = 10M\Omega$. The OPT202 is useful with feedback resistors of 100MΩ or greater at room temperature. The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 3.

When used with very large feedback resistors, tiny leakage currents on the circuit board can degrade the performance of the OPT202. Careful circuit board design and clean assembly procedures will help achieve best performance. A “guard ring” on the circuit board can help minimize leakage to the critical non-inverting input (pin 2). This guard ring should encircle pin 2 and connect to Common, pin 8.

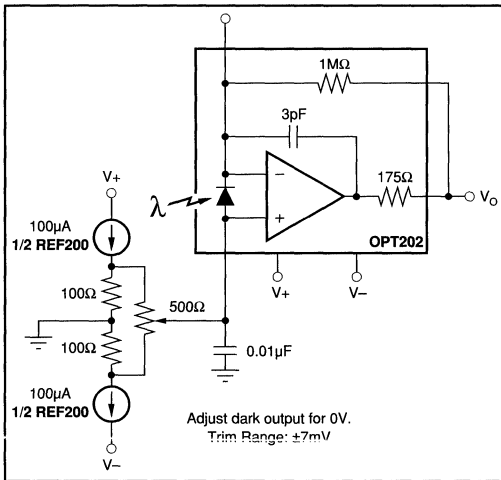


FIGURE 3. Dark Error (Offset) Adjustment Circuit.

LINEARITY PERFORMANCE

Current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains below approximately 0.01% up to 100μA photodiode current. The photodiode can produce output currents of 10mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

DYNAMIC RESPONSE

Using the internal 1MΩ resistor, the dynamic response of the photodiode/op amp combination can be modeled as a

simple R/C circuit with a -3dB cutoff frequency of 50kHz. This yields a rise time of approximately 10μs (10% to 90%). Dynamic response is not limited by op amp slew rate. This is demonstrated by the dynamic response oscilloscope photographs showing virtually identical large-signal and small-signal response.

Dynamic response will vary with feedback resistor value as shown in the typical performance curve “Voltage Output Responsivity vs Frequency.” Rise time (10% to 90%) will vary according to the -3dB bandwidth produced by a given feedback resistor value—

$$t_r \approx \frac{0.35}{f_c} \quad (1)$$

where:

- t_r is the rise time (10% to 90%)
- f_c is the -3dB bandwidth

NOISE PERFORMANCE

Noise performance of the OPT202 is determined by the op amp characteristics in conjunction with the feedback components and photodiode capacitance. The typical performance curve “Output Noise Voltage vs Measurement Bandwidth” shows how the noise varies with R_F and measured bandwidth (1Hz to the indicated frequency). The signal bandwidth of the OPT202 is indicated on the curves. Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth.

Output noise increases in proportion to the square-root of the feedback resistance, while responsivity increases linearly with feedback resistance. So best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by Noise Effective Power (NEP). This is the radiant power which would produce an output signal equal to the noise level. NEP has the units of radiant power (watts). The typical performance curve “Noise Effective Power vs Measurement Bandwidth” shows how NEP varies with R_F and measurement bandwidth.

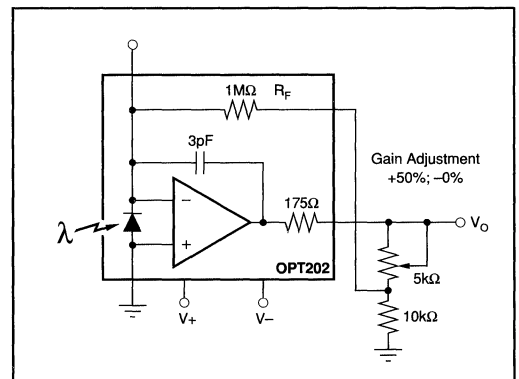


FIGURE 4. Responsivity (Gain) Adjustment Circuit.

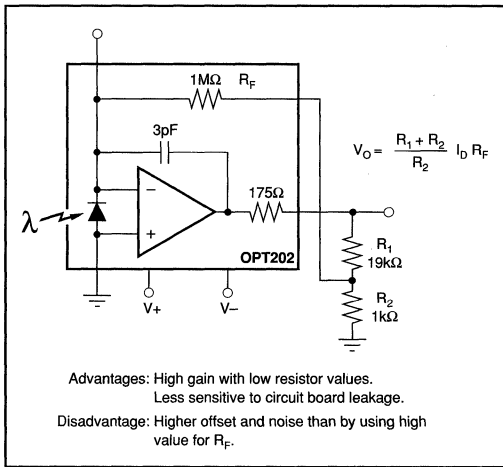


FIGURE 5. "T" Feedback Network.

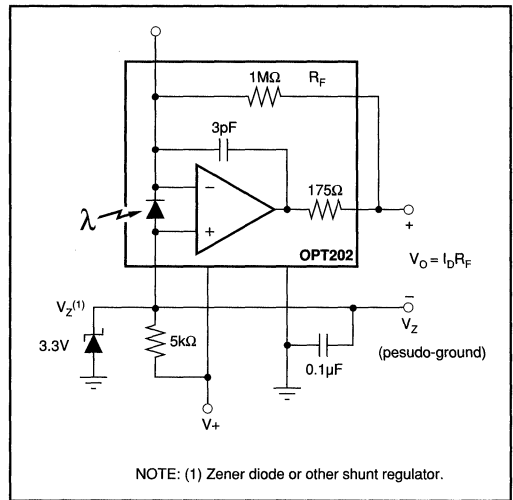


FIGURE 7. Single Power Supply Operation.

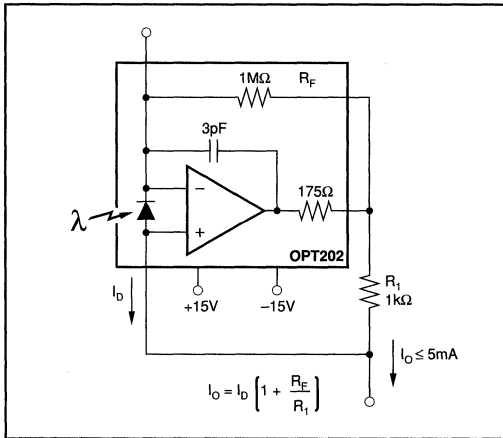


FIGURE 6. Current Output Circuit.

Other application circuits can be seen in the OPT209 data sheet.

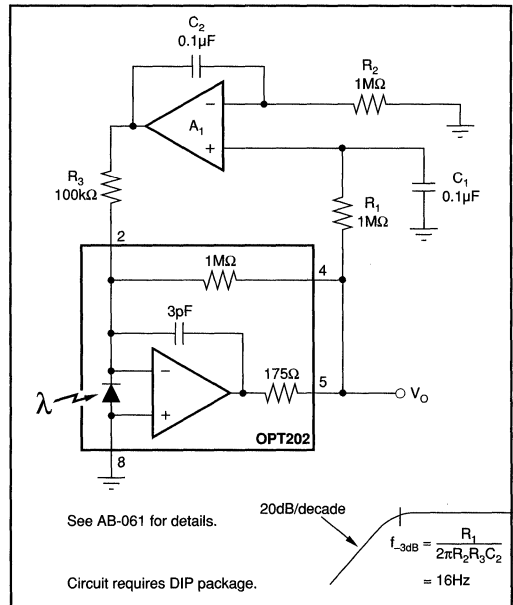
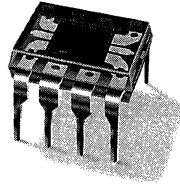


FIGURE 8. DC Restoration Rejects Unwanted Steady-State Background Light.

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OPT209

PHOTODIODE WITH ON-CHIP AMPLIFIER

FEATURES

- PHOTODIODE SIZE: 0.090 x 0.090 inch (2.29 x 2.29mm)
- 1MΩ FEEDBACK RESISTOR
- HIGH RESPONSIVITY: 0.45A/W (650nm)
- LOW DARK ERRORS: 2mV
- BANDWIDTH: 16kHz
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 400μA
- TRANSPARENT 8-PIN DIP

APPLICATIONS

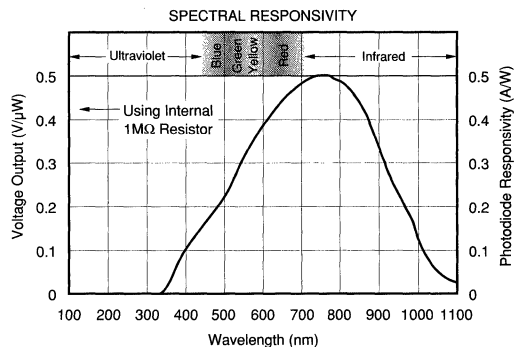
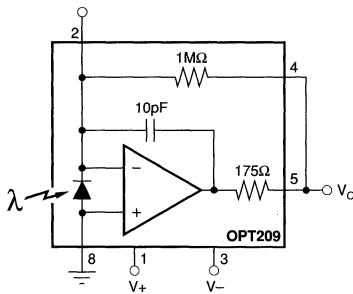
- MEDICAL INSTRUMENTATION
- LABORATORY INSTRUMENTATION
- POSITION AND PROXIMITY SENSORS
- PHOTOGRAPHIC ANALYZERS
- SMOKE DETECTORS

DESCRIPTION

The OPT209 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT209 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400μA. It is packaged in a transparent plastic 8-pin DIP, specified for the 0°C to 70°C temperature range.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-1232A

6.13

OPT209
6
OPTICAL SENSORS

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, internal $1\text{M}\Omega$ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT209P			UNITS
		MIN	TYP	MAX	
RESPONSIVITY Photodiode Current Voltage Output vs Temperature Unit-to-Unit Variation Nonlinearity ⁽¹⁾ Photodiode Area	650nm 650nm 650nm FS Output = 10V (0.090 x 0.090in) (2.29 x 2.29mm)		0.45 0.45 100 0.01 0.008 5.2		A/W V/ μW ppm/ $^\circ\text{C}$ % % of FS in ² mm ²
DARK ERRORS, RTO⁽²⁾ Offset Voltage, Output vs Temperature vs Power Supply Voltage Noise	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$ Measured BW = 0.1 to 100kHz		± 0.5 ± 10 10 350	± 2 100	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ μVrms
RESISTOR—1MΩ Internal Resistance Tolerance vs Temperature			1 ± 0.5 50	± 2	M Ω % ppm/ $^\circ\text{C}$
FREQUENCY RESPONSE Bandwidth, Large or Small-Signal, -3dB Rise Time, 10% to 90% Settling Time, 1% 0.1% 0.01% Overload Recovery Time (to 1%)	FS to Dark FS to Dark FS to Dark 100% overdrive, $V_S = \pm 15\text{V}$ 100% overdrive, $V_S = \pm 5\text{V}$ 100% overdrive, $V_S = \pm 2.25\text{V}$		16 22 60 85 100 44 100 240		kHz μs μs μs μs μs μs μs
OUTPUT Voltage Output Capacitive Load, Stable Operation Short-Circuit Current	$R_L = 10\text{k}\Omega$ $R_L = 5\text{k}\Omega$	(V_+) - 1.25 (V_+) - 2	(V_+) - 1 (V_+) - 1.5 1 ± 18		V V nF mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	$V_O = 0$	± 2.25	± 15 ± 400	± 18 ± 500	V V μA
TEMPERATURE RANGE Specification, Operating Storage Thermal Resistance, θ_{JA}		0 -25		+70 +85	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

PHOTODIODE SPECIFICATIONS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT209			UNITS
		MIN	TYP	MAX	
Photodiode Area	(0.090 x 0.090in) (2.29 x 2.29mm)		0.008 5.1		in ² mm ²
Current Responsivity	650nm		0.45		A/W
Dark Current vs Temperature	$V_O = 0\text{V}^{(1)}$		500 doubles every 10 $^\circ\text{C}$		fA
Capacitance	$V_O = 0\text{V}^{(1)}$		600		pF

NOTE: (1) Voltage Across Photodiode.

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SPECIFICATIONS (CONT)

ELECTRICAL

Op Amp Section of OPT209¹⁾

T_A = +25°C, V_S = ±15V, unless otherwise noted.

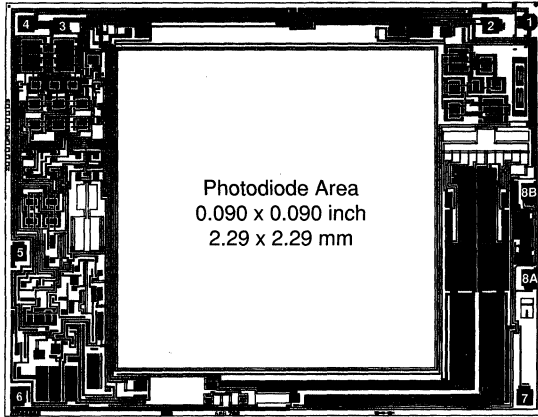
PARAMETER	CONDITIONS	OPT209 Op Amp			UNITS
		MIN	TYP	MAX	
INPUT Offset Voltage vs Temperature vs Power Supply Input Bias Current vs Temperature	V _S = ±2.25V to ±18V		±0.5 ±5 10 1 doubles every 10°C		mV μV/°C μV/V pA
NOISE Input Voltage Noise Voltage Noise Density, f=10Hz f=100Hz f=1kHz Current Noise Density, f=1kHz			30 25 15 0.8		nV/√Hz nV/√Hz nV/√Hz fA/√Hz
INPUT VOLTAGE RANGE Common-mode Input Range Common-mode Rejection			±14.4 106		V dB
INPUT IMPEDANCE Differential Common-mode			10 ⁹ 3 10 ⁹ 3		Ω pF Ω pF
OPEN-LOOP GAIN Open-loop Voltage Gain			120		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.1% 0.01%			4 6 4 5		MHz V/μs μs μs
OUTPUT Voltage Output Short-Circuit Current	R _L = 10kΩ R _L = 5kΩ	(V+) - 1.25 (V+) - 2	(V+) - 1 (V+) - 1.5 ±18		V V mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	I _O = 0	±2.25	±15 ±400	±18 ±500	V V μA

NOTE: (1) Op amp specifications provided for information and comparison only.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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DICE INFORMATION



OPT209 DIE TOPOGRAPHY

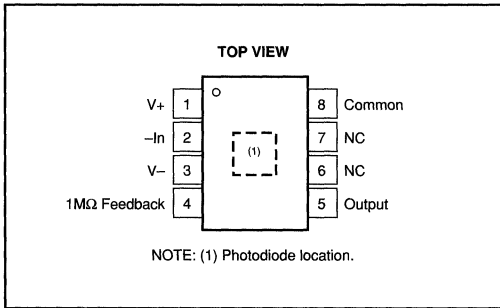
PAD	FUNCTION
1	V+
2	-In
3	V-
4	1MΩ Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 ±5	3.91 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	None	

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range (Common Pin)	±V _S
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-25°C to +85°C
Storage Temperature	-25°C to +85°C
Junction Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
(Vapor-Phase Soldering Not Recommended)	

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPT209P	8-Pin DIP	006-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



MOISTURE SENSITIVITY AND SOLDERING

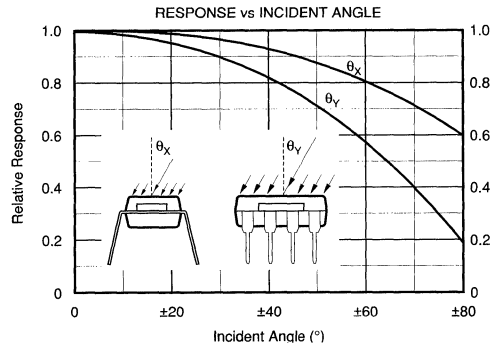
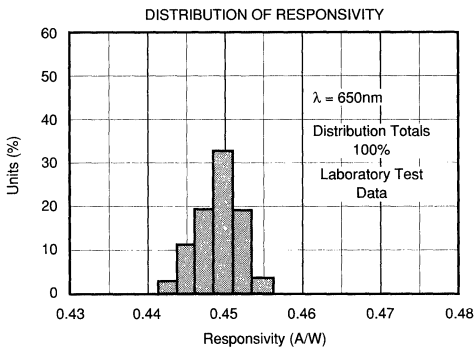
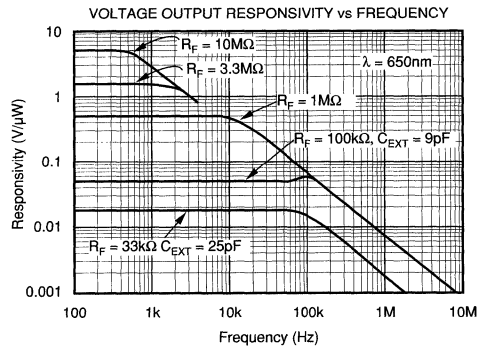
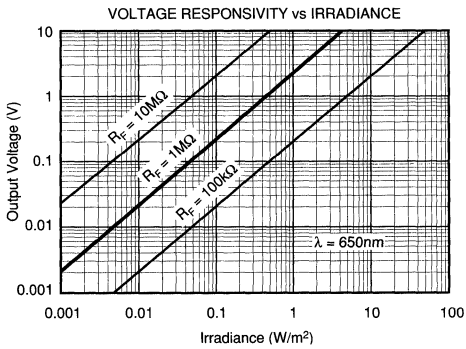
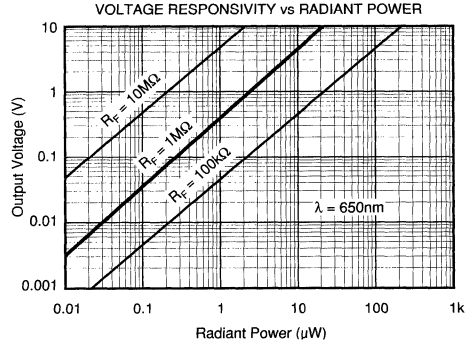
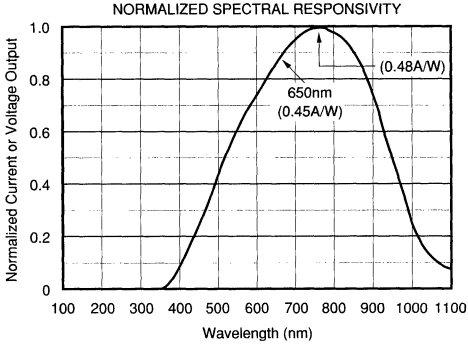
Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT209 cannot meet flammability test, UL-94.

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TYPICAL PERFORMANCE CURVES

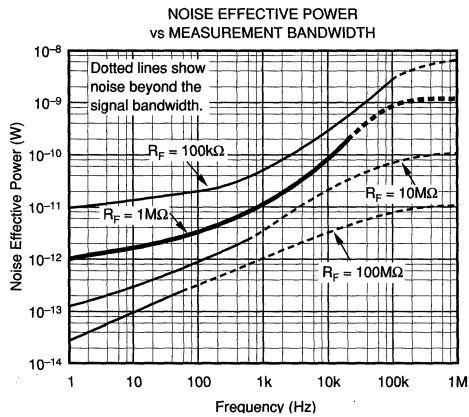
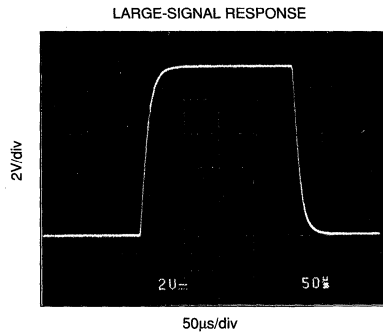
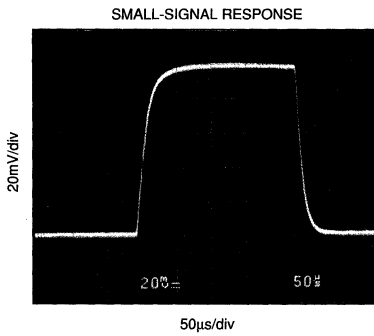
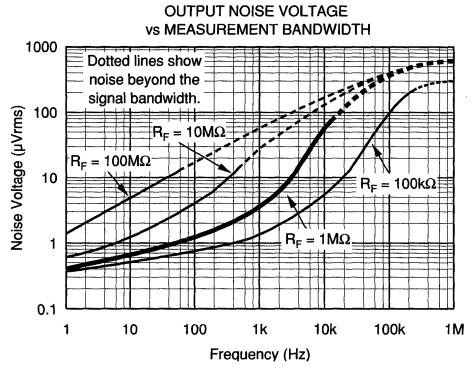
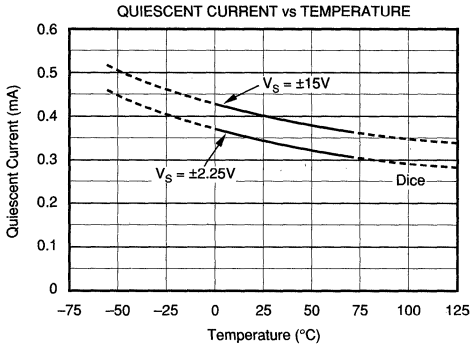
At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT209. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown. Output is zero volts with no light and increases with increasing illumination.

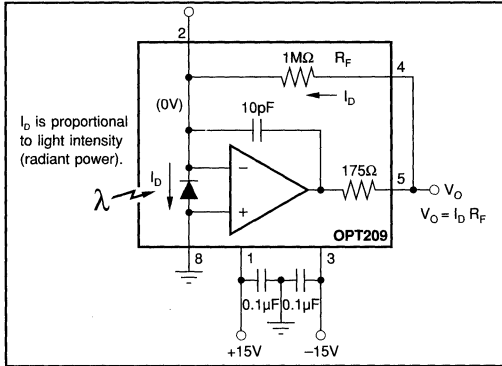


FIGURE 1. Basic Circuit Connections.

Photodiode current, I_D , is proportional to the radiant power or flux (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode Responsivity, R_r , is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.23 \times 10^{-6} \text{m}^2$.

The OPT209's voltage output is the product of the photodiode current times the feedback resistor, ($I_D R_F$). The internal feedback resistor is laser trimmed to $1\text{M}\Omega \pm 2\%$. Using this resistor, the output voltage responsivity, R_v , is approximately $0.45\text{V}/\mu\text{W}$ at 650nm wavelength.

An external resistor can be connected to set a different voltage responsivity. Best dynamic performance is achieved by connecting R_{EXT} in series (for $R_F > 1\text{M}\Omega$), or in parallel (for $R_F < 1\text{M}\Omega$), with the internal resistor as shown in Figure 2. These connections take advantage of on-chip capacitive guarding of the internal resistor, which improves dynamic performance. For values of R_F less than $1\text{M}\Omega$, an external capacitor, C_{EXT} , should be connected in parallel with R_F (see Figure 2). This capacitor eliminates gain peaking and prevents instability. The value of C_{EXT} can be read from the table in Figure 2.

LIGHT SOURCE POSITIONING

The OPT209 is 100% tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although all IC amplifiers are light-sensitive to some degree, the OPT209 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with

metal, and differential stages are cross-coupled. Furthermore, the photodiode area is very large relative to the op amp input circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT209 would not perform properly. The large (0.090×0.090 inch) photodiode area allows easy positioning of narrowly focused light sources. The photodiode area is easily visible—it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffused by the side of the package. These effects are shown in the typical performance curve "Response vs Incident Angle."

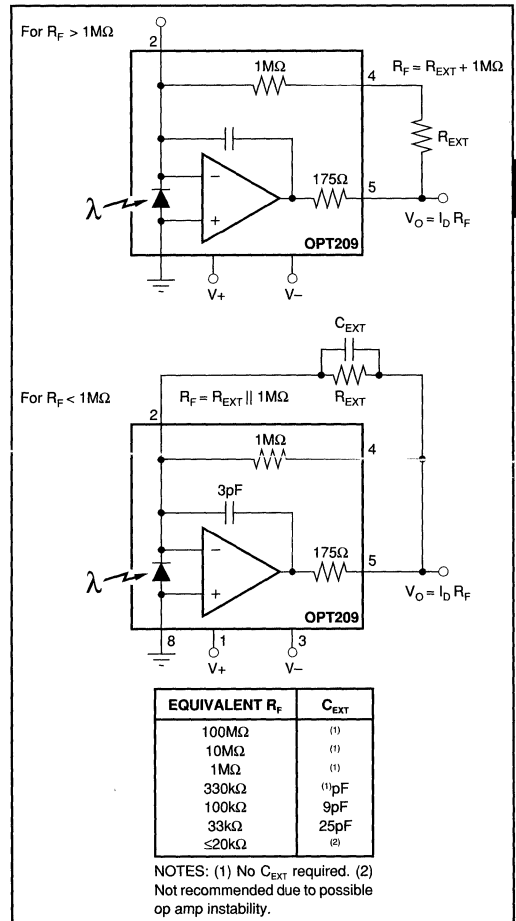


FIGURE 2. Using External Feedback Resistor.

DARK ERRORS

The dark errors in the specification table include all sources. The dominant error source is the input offset voltage of the op amp. Photodiode dark current and input bias current of the op amp are in the 2pA range and contribute virtually no offset error at room temperature. Dark current and input bias current double for each 10°C above 25°C. At 70°C, the error current can be approximately 100pA. This would produce a 1mV offset with $R_F = 10M\Omega$. The OPT209 is useful with feedback resistors of 100MΩ or greater at room temperature. The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 3.

When used with very large feedback resistors, tiny leakage currents on the circuit board can degrade the performance of the OPT209. Careful circuit board design and clean assembly procedures will help achieve best performance. A "guard ring" on the circuit board can help minimize leakage to the critical non-inverting input (pin 2). This guard ring should encircle pin 2 and connect to Common, pin 8.

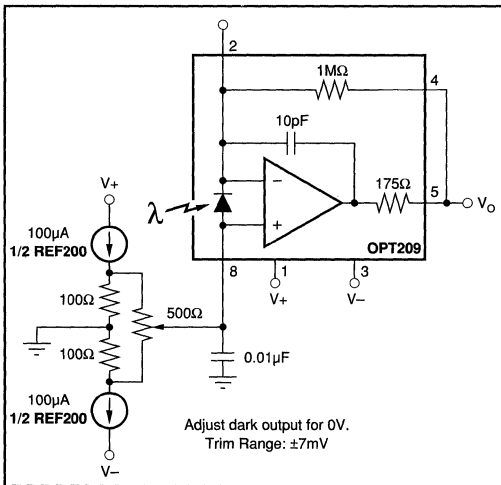


FIGURE 3. Dark Error (Offset) Adjustment Circuit.

LINEARITY PERFORMANCE

Current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains below approximately 0.01% up to 100μA photodiode current. The photodiode can produce output currents of 10mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

DYNAMIC RESPONSE

Using the internal 1MΩ resistor, the dynamic response of the photodiode/op amp combination can be modeled as a

simple R/C circuit with a -3dB cutoff frequency of 16kHz. This yields a rise time of approximately 22μs (10% to 90%). Dynamic response is not limited by op amp slew rate. This is demonstrated by the dynamic response oscilloscope photographs showing virtually identical large-signal and small-signal response.

Dynamic response will vary with feedback resistor value as shown in the typical performance curve "Voltage Output Responsivity vs Frequency." Rise time (10% to 90%) will vary according to the -3dB bandwidth produced by a given feedback resistor value—

$$t_R \approx \frac{0.35}{f_C} \quad (1)$$

where:

- t_R is the rise time (10% to 90%)
- f_C is the -3dB bandwidth

NOISE PERFORMANCE

Noise performance of the OPT209 is determined by the op amp characteristics in conjunction with the feedback components and photodiode capacitance. The typical performance curve "Output Noise Voltage vs Measurement Bandwidth" shows how the noise varies with R_F and measured bandwidth (1Hz to the indicated frequency). The signal bandwidth of the OPT209 is indicated on the curves. Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth.

Output noise increases in proportion to the square-root of the feedback resistance, while responsivity increases linearly with feedback resistance. So best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by Noise Effective Power (NEP). This is the radiant power which would produce an output signal equal to the noise level. NEP has the units of radiant power (watts). The typical performance curve "Noise Effective Power vs Measurement Bandwidth" shows how NEP varies with R_F and measurement bandwidth.

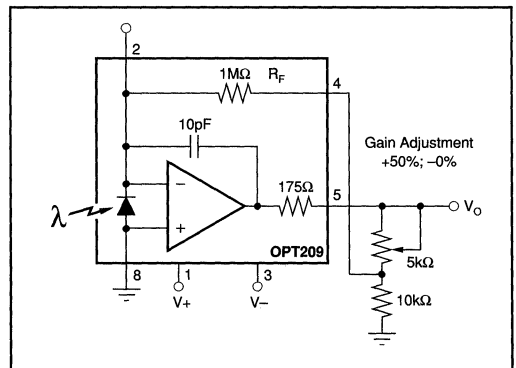


FIGURE 4. Responsivity (Gain) Adjustment Circuit.

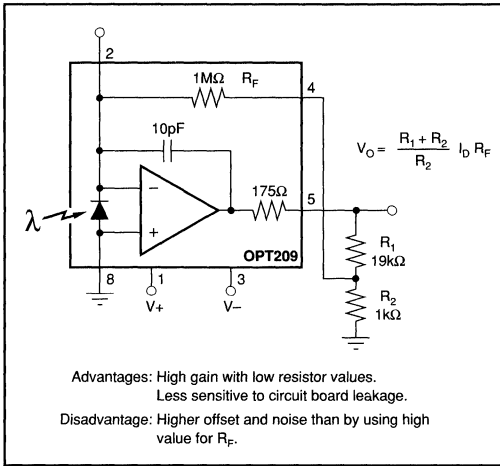


FIGURE 5. "T" Feedback Network.

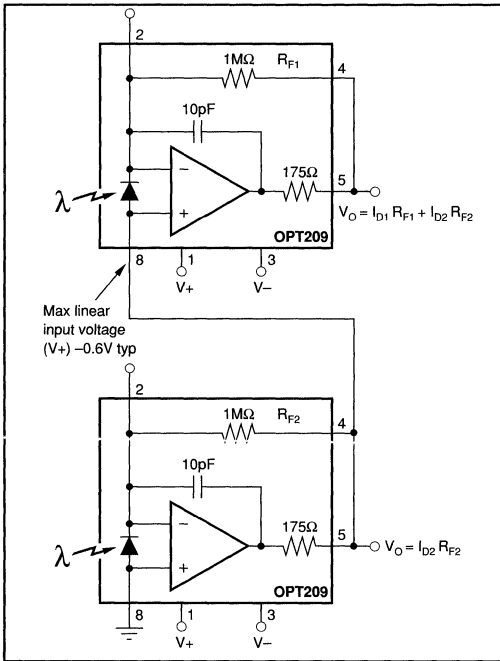


FIGURE 6. Summing Output of Two OPT209s.

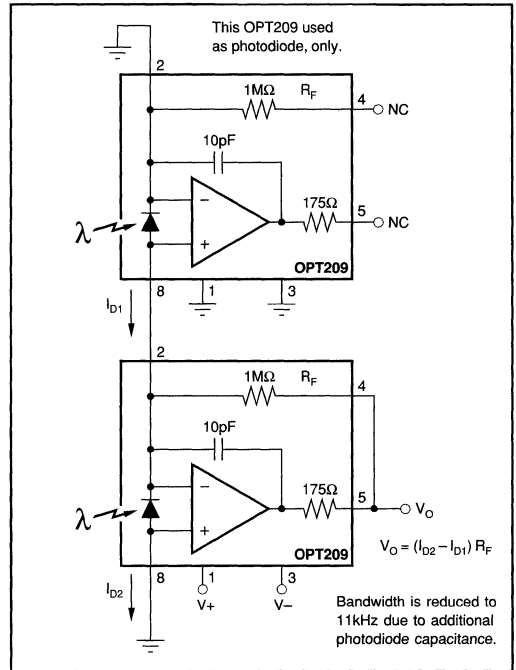


FIGURE 7. Differential Light Measurement.

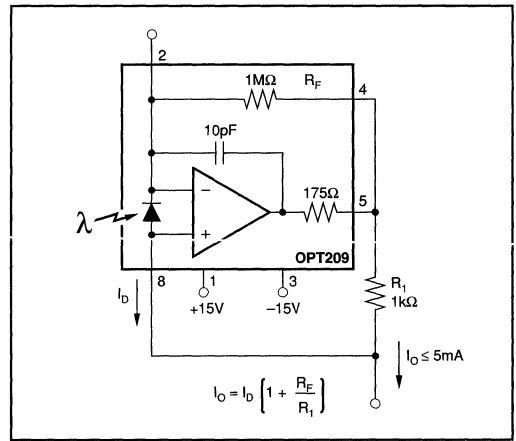


FIGURE 8. Current Output Circuit.

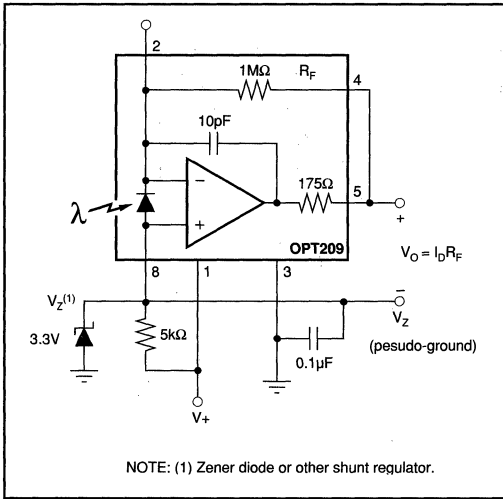


FIGURE 9. Single Power Supply Operation.

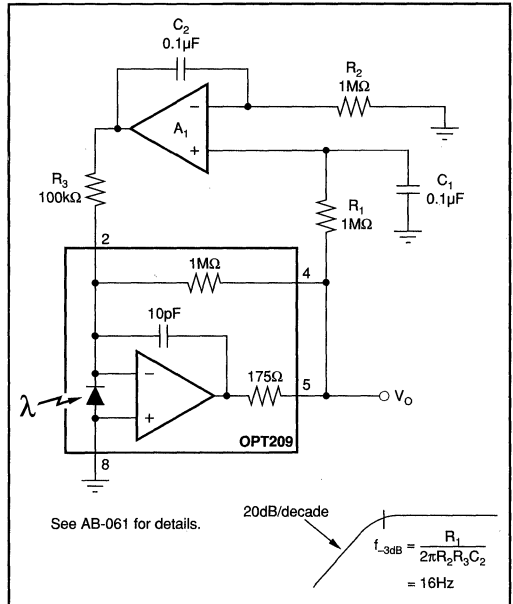


FIGURE 10. DC Restoration Rejects Unwanted Steady-State Background Light.

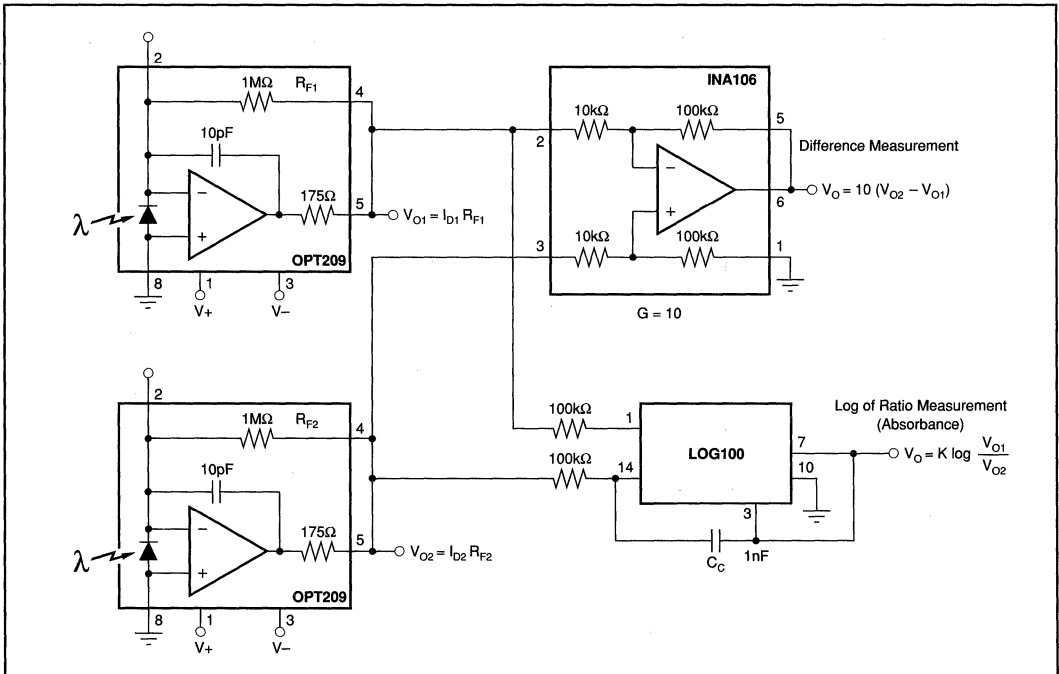


FIGURE 11. Differential Light Measurement.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

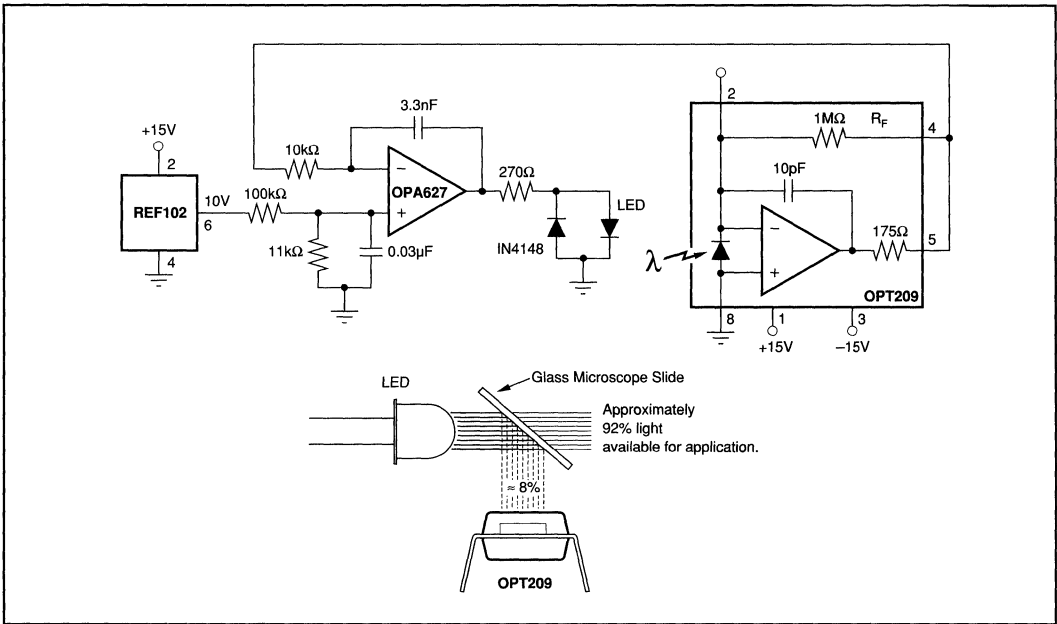


FIGURE 12. LED Output Regulation Circuit.

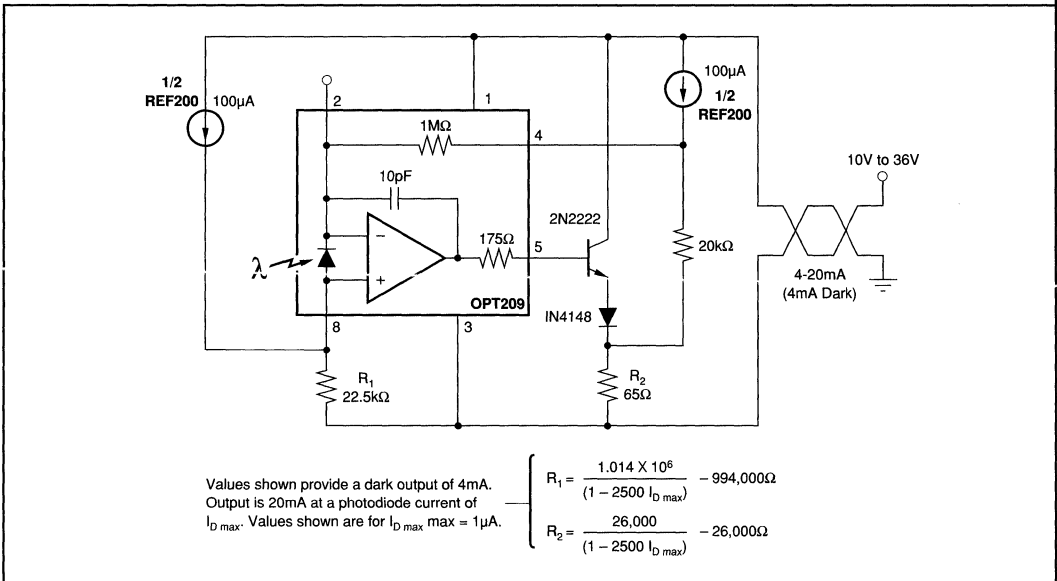


FIGURE 13. 4-20mA Current-Loop Transmitter.

OPT209

6

OPTICAL SENSORS



OPT301

INTEGRATED PHOTODIODE AND AMPLIFIER

FEATURES

- **PHOTODIODE SIZE: 0.090 x 0.090 inch**
(2.29 x 2.29mm)
- **1MΩ FEEDBACK RESISTOR**
- **HIGH RESPONSIVITY: 0.47A/W (650nm)**
- **IMPROVED UV RESPONSE**
- **LOW DARK ERRORS: 2mV**
- **BANDWIDTH: 4kHz**
- **WIDE SUPPLY RANGE: ±2.25 to ±18V**
- **LOW QUIESCENT CURRENT: 400μA**
- **HERMETIC TO-99**

APPLICATIONS

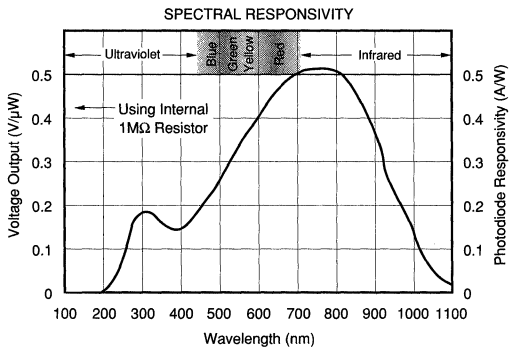
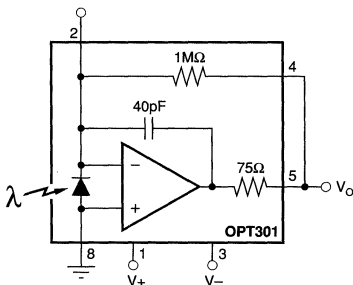
- **MEDICAL INSTRUMENTATION**
- **LABORATORY INSTRUMENTATION**
- **POSITION AND PROXIMITY SENSORS**
- **PHOTOGRAPHIC ANALYZERS**
- **SMOKE DETECTORS**

DESCRIPTION

The OPT301 is an opto-electronic integrated circuit containing a photodiode and transimpedance amplifier on a single dielectrically isolated chip. The transimpedance amplifier consists of a precision FET-input op amp and an on-chip metal film resistor. The 0.09 x 0.09 inch photodiode is operated at zero bias for excellent linearity and low dark current.

The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs such as leakage current errors, noise pick-up and gain peaking due to stray capacitance.

The OPT301 operates over a wide supply range (±2.25 to ±18V) and supply current is only 400μA. It is packaged in a hermetic TO-99 metal package with a glass window, and is specified for the -40°C to 85°C temperature range.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, internal $1\text{M}\Omega$ feedback resistor, unless otherwise noted.

PARAMETER	CONDITIONS	OPT301M			UNITS
		MIN	TYP	MAX	
RESPONSIVITY Photodiode Current Voltage Output vs Temperature Unit-to-Unit Variation Nonlinearity ⁽¹⁾ Photodiode Area	650nm 650nm 650nm FS Output = 10V (0.090 x 0.090in) (2.29 x 2.29mm)		0.47 0.47 200 ± 5 0.01 0.008 5.2		A/W V/ μW ppm/ $^\circ\text{C}$ % % of FS in ² mm ²
DARK ERRORS, RTO⁽²⁾ Offset Voltage, Output vs Temperature vs Power Supply Voltage Noise	$V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$ Measured BW = 0.1 to 100kHz		± 0.5 ± 10 10 160	± 2 100	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ μVrms
RESISTOR—1MΩ Internal Resistance Tolerance vs Temperature			1 ± 0.5 50	± 2	M Ω % ppm/ $^\circ\text{C}$
FREQUENCY RESPONSE Bandwidth, Large or Small-Signal, -3dB Rise Time, 10% to 90% Settling Time, 1% 0.1% 0.01% Overload Recovery Time	FS to Dark FS to Dark FS to Dark 100% overdrive, $V_S = \pm 15\text{V}$ 100% overdrive, $V_S = \pm 5\text{V}$ 100% overdrive, $V_S = \pm 2.25\text{V}$		4 90 240 350 900 240 500 1000		kHz μs μs μs μs μs μs μs
OUTPUT Voltage Output Capacitive Load, Stable Operation Short-Circuit Current	$R_L = 10\text{k}\Omega$ $R_L = 5\text{k}\Omega$	(V_+) - 1.25 (V_+) - 2	(V_+) - 0.65 (V_+) - 1 10 ± 18		V V nF mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	$I_o = 0$	± 2.25	± 15 ± 0.4	± 18 ± 0.5	V V mA
TEMPERATURE RANGE Specification Operating/Storage Thermal Resistance, θ_{JA}		-40 -55		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Deviation in percent of full scale from best-fit straight line. (2) Referred to Output. Includes all error sources.

PHOTODIODE SPECIFICATIONS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	CONDITIONS	Photodiode of OPT301			UNITS
		MIN	TYP	MAX	
Photodiode Area	(0.090 x 0.090in) (2.29 x 2.29mm)		0.008 5.1		in ² mm ²
Current Responsivity	650nm		0.47		A/W
Dark Current vs Temperature	$V_D = 0\text{V}^{(1)}$		500 doubles every 10°C		fA
Capacitance	$V_D = 0\text{V}^{(1)}$		4000		pF

NOTE: (1) Voltage Across Photodiode.

OPT301
6
OPTICAL SENSORS

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SPECIFICATIONS (CONT)

ELECTRICAL

Op Amp Section of OPT301⁽¹⁾

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

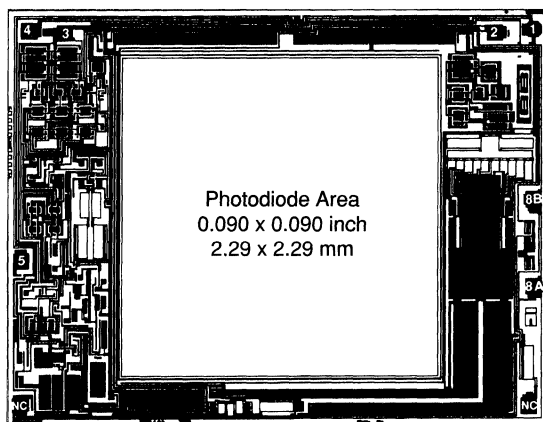
PARAMETER	CONDITIONS	OPT301 Op Amp			UNITS
		MIN	TYP	MAX	
INPUT Offset Voltage vs Temperature vs Power Supply Input Bias Current vs Temperature	$V_S = \pm 2.25\text{V to } \pm 18\text{V}$		± 0.5 ± 5 10 1 doubles every 10°C		mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V/V}$ pA
NOISE Input Voltage Noise Voltage Noise Density, $f=10\text{Hz}$ $f=100\text{Hz}$ $f=1\text{kHz}$ Current Noise Density, $f=1\text{kHz}$				30 25 15 0.8	
INPUT VOLTAGE RANGE Common-mode Input Range Common-mode Rejection			± 14.4 106		V dB
INPUT IMPEDANCE Differential Common-mode			$10^{12} 3$ $10^{12} 3$		ΩpF ΩpF
OPEN-LOOP GAIN Open-loop Voltage Gain			120		dB
FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate Settling Time 0.1% 0.01%			380 0.5 4 5		kHz $\text{V}/\mu\text{s}$ μs μs
OUTPUT Voltage Output Short-Circuit Current	$R_L = 10\text{k}\Omega$ $R_L = 5\text{k}\Omega$	$(V+) - 1.25$ $(V+) - 2$	$(V+) - 0.65$ $(V+) - 1$ ± 18		V V mA
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current	$I_O = 0$	± 2.25	± 15 ± 0.4	± 18 ± 0.5	V V mA

NOTE: (1) Op amp specifications provided for information and comparison only.

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DICE INFORMATION



OPT301 DIE TOPOGRAPHY

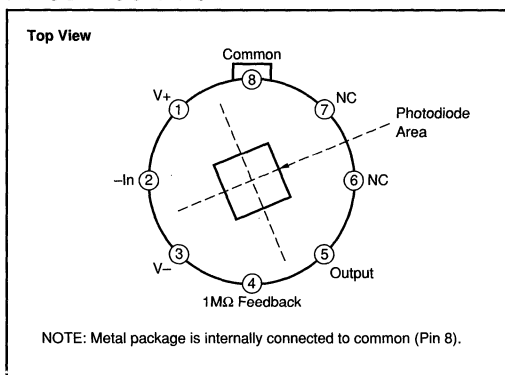
PAD	FUNCTION
1	V+
2	-In
3	V-
4	1M Ω Feedback
5	Output
6	NC
7	NC
8A, 8B	Common

NC: No Connection. Pads 8A and 8B must both be connected to common. Substrate Bias: The substrate is electrically connected to internal circuitry. Do not make electrical connection to the substrate.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	154 x 120 \pm 5	3.91 x 3.05 \pm 0.13
Die Thickness	20 \pm 3	0.51 \pm 0.08
Min. Pad Size	4 x 4	0.1 x 0.1
Backing		None

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPT301M	8-Pin TO-99	001-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

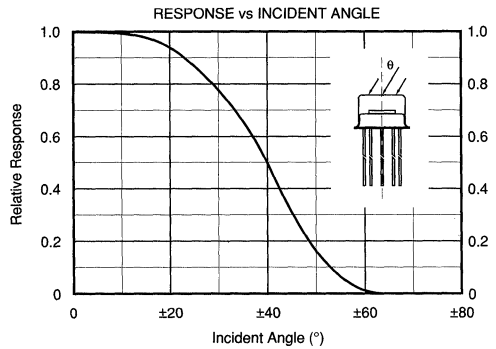
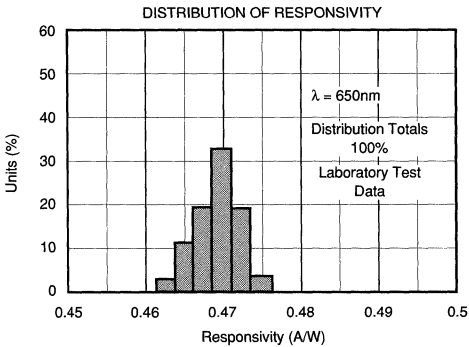
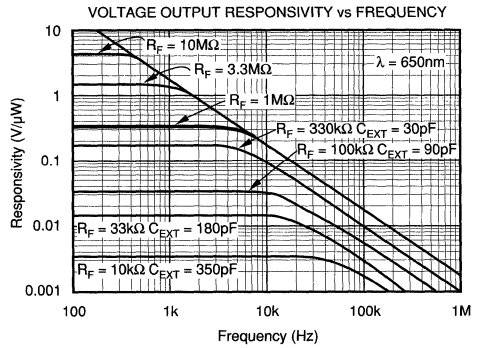
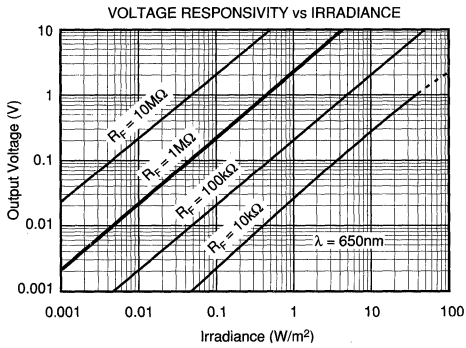
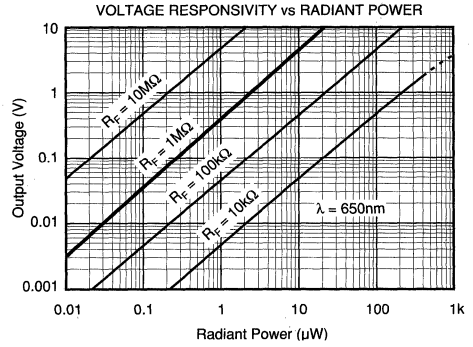
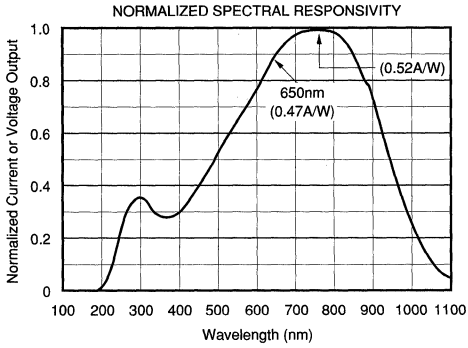
Supply Voltage	\pm 18V
Input Voltage Range (Common Pin)	\pm V _S
Output Short-Circuit (to ground)	Continuous
Operating Temperature	-55°C to +125°C
Storage Temperature	-55°C to +125°C
Junction Temperature	+125°C
Lead Temperature (soldering, 10s)	+300°C

OPT301
6
OPTICAL SENSORS

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TYPICAL PERFORMANCE CURVES

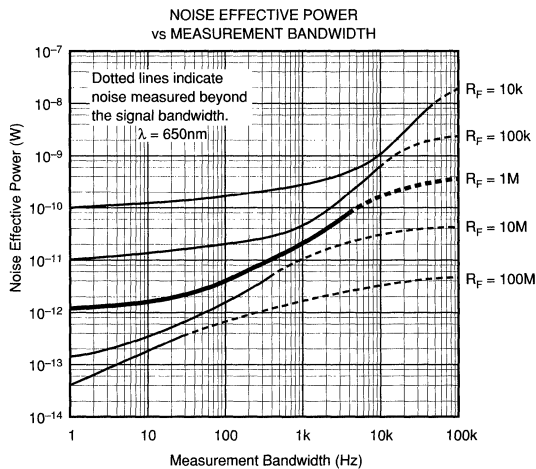
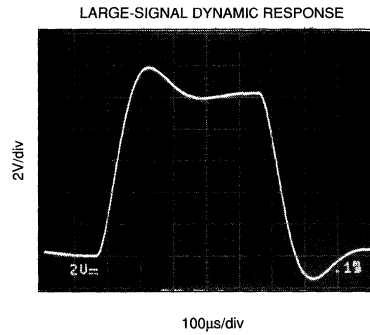
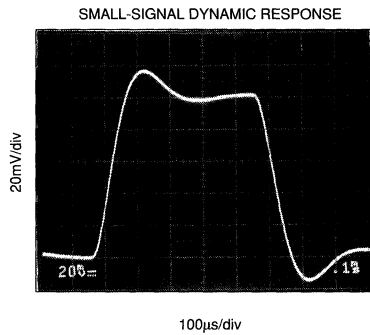
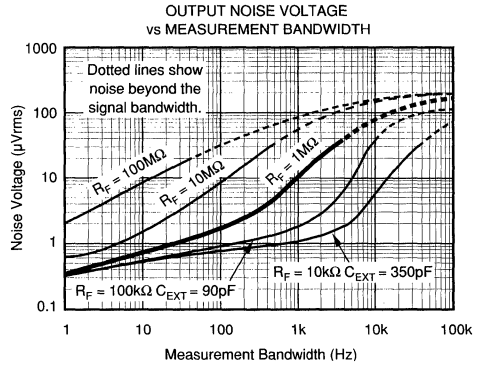
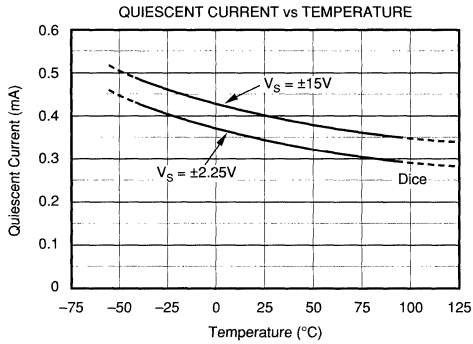
At $T_A = +25^\circ\text{C}$, $V_s = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $\lambda = 650\text{nm}$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required to operate the OPT301. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown. Output is zero volts with no light and increases with increasing illumination.

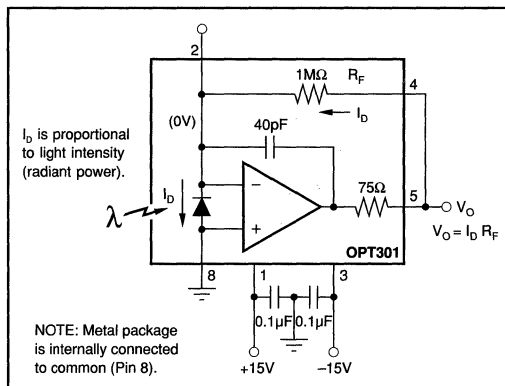


FIGURE 1. Basic Circuit Connections.

Photodiode current, I_D , is proportional to the radiant power or flux (in watts) falling on the photodiode. At a wavelength of 650nm (visible red) the photodiode Responsivity, R_p , is approximately 0.45A/W. Responsivity at other wavelengths is shown in the typical performance curve "Responsivity vs Wavelength."

The typical performance curve "Output Voltage vs Radiant Power" shows the response throughout a wide range of radiant power. The response curve "Output Voltage vs Irradiance" is based on the photodiode area of $5.23 \times 10^{-6} \text{m}^2$.

The OPT301's voltage output is the product of the photodiode current times the feedback resistor, ($I_D R_F$). The internal feedback resistor is laser trimmed to $1\text{M}\Omega \pm 2\%$. Using this resistor, the output voltage responsivity, R_v , is approximately $0.45\text{V}/\mu\text{W}$ at 650nm wavelength.

An external resistor can be used to set a different voltage responsivity. For values of R_F less than $1\text{M}\Omega$, an external capacitor, C_{EXT} , should be connected in parallel with R_F (see Figure 2). This capacitor eliminates gain peaking and prevents instability. The value of C_{EXT} can be read from the table in Figure 2.

LIGHT SOURCE POSITIONING

The OPT301 is 100% tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although all IC amplifiers are light-sensitive to some degree, the OPT301 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal, and differential stages are cross-coupled. Furthermore, the photodiode area is very large relative to the op amp input circuitry making these effects negligible.

If your light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. If a narrowly focused light source were to miss the photodiode area and fall only on the op amp circuitry, the OPT301 would not perform properly. The large (0.090 x 0.090 inch) photodiode area allows easy positioning of narrowly focused light sources. The photodiode area is easily visible—it appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also affects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is reflected and scattered by the side of the package. These effects are shown in the typical performance curve "Response vs Incident Angle."

DARK ERRORS

The dark errors in the specification table include all sources. The dominant error source is the input offset voltage of the op amp. Photodiode dark current and input bias current of the op amp are approximately 2pA and contribute virtually no offset error at room temperature. Dark current and input bias current double for each 10°C above 25°C . At 70°C , the error current can be approximately 100pA. This would produce a 1mV offset with $R_F = 10\text{M}\Omega$. The OPT301 is useful with feedback resistors of $100\text{M}\Omega$ or greater at room temperature. The dark output voltage can be trimmed to zero with the optional circuit shown in Figure 3.

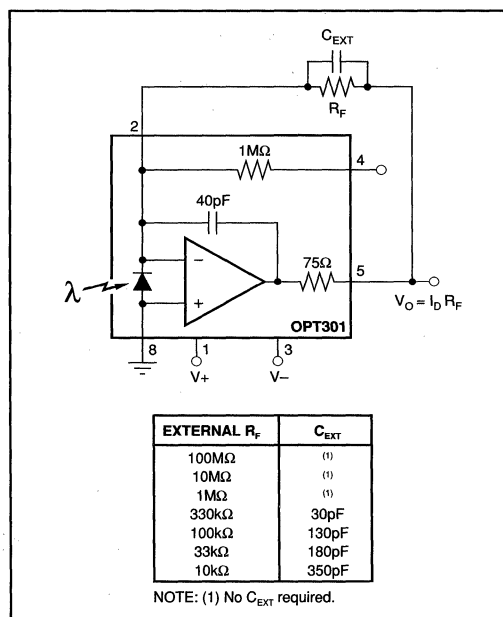


FIGURE 2. Using External Feedback Resistor.

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When used with very large feedback resistors, tiny leakage currents on the circuit board can degrade the performance of the OPT301. Careful circuit board design and clean assembly procedures will help achieve best performance. A “guard trace” on the circuit board can help minimize leakage to the critical non-inverting input (pin 2). This guard ring should encircle pin 2 and connect to Common, pin 8.

DYNAMIC RESPONSE

Using the internal $1\text{M}\Omega$ resistor, the dynamic response of the photodiode/op amp combination can be modeled as a simple R/C circuit with a -3dB cutoff frequency of 4kHz . This yields a rise time of approximately $90\mu\text{s}$ (10% to 90%). Dynamic response is not limited by op amp slew rate. This is demonstrated by the dynamic response oscilloscope photographs showing virtually identical large-signal and small-signal response.

Dynamic response will vary with feedback resistor value as shown in the typical performance curve “Voltage Output Responsivity vs Frequency.” Rise time (10% to 90%) will vary according to the -3dB bandwidth produced by a given feedback resistor value—

$$t_R \approx \frac{0.35}{f_C} \quad (1)$$

where:

t_R is the rise time (10% to 90%)
 f_C is the -3dB bandwidth

LINEARITY PERFORMANCE

Current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains below

approximately 0.02% up to $100\mu\text{A}$ photodiode current. The photodiode can produce output currents of 1mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This excellent linearity at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity will occur at lower radiant power.

NOISE PERFORMANCE

Noise performance of the OPT301 is determined by the op amp characteristics in conjunction with the feedback components and photodiode capacitance. The typical performance curve “Output Noise Voltage vs Measurement Bandwidth” shows how the noise varies with R_F and measured bandwidth (1Hz to the indicated frequency). The signal bandwidth of the OPT301 is indicated on the curves. Noise can be reduced by filtering the output with a cutoff frequency equal to the signal bandwidth.

Output noise increases in proportion to the square-root of the feedback resistance, while responsivity increases linearly with feedback resistance. So best signal-to-noise ratio is achieved with large feedback resistance. This comes with the trade-off of decreased bandwidth.

The noise performance of a photodetector is sometimes characterized by Noise Effective Power (NEP). This is the radiant power which would produce an output signal equal to the noise level. NEP has the units of radiant power (watts). The typical performance curve “Noise Effective Power vs Measurement Bandwidth” shows how NEP varies with R_F and measurement bandwidth.

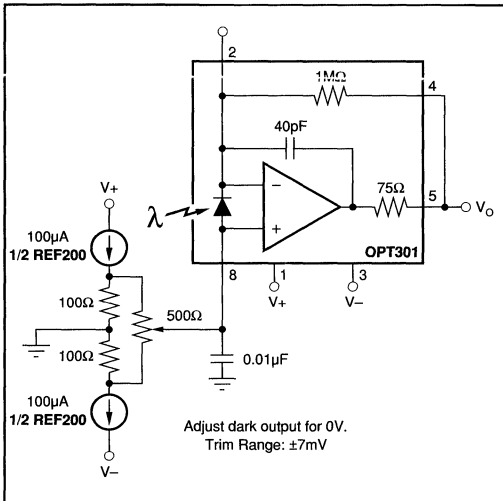


FIGURE 3. Dark Error (Offset) Adjustment Circuit.

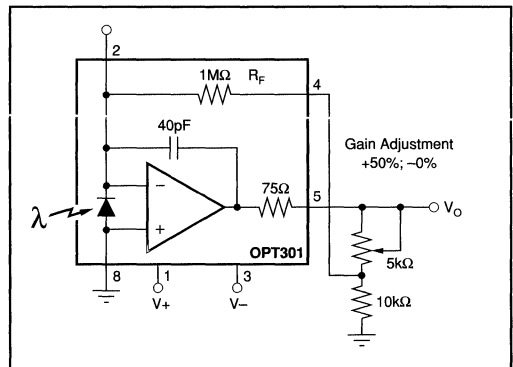


FIGURE 4. Responsivity (Gain) Adjustment Circuit.

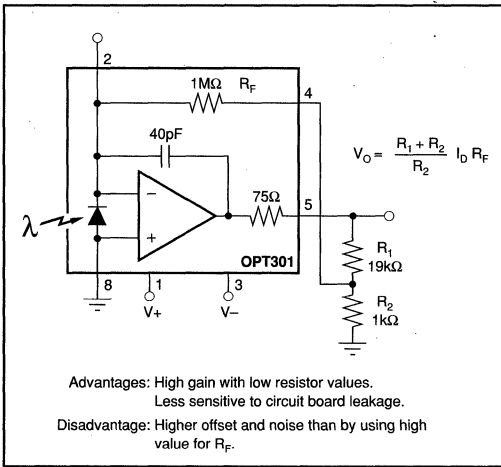


FIGURE 5. "T" Feedback Network.

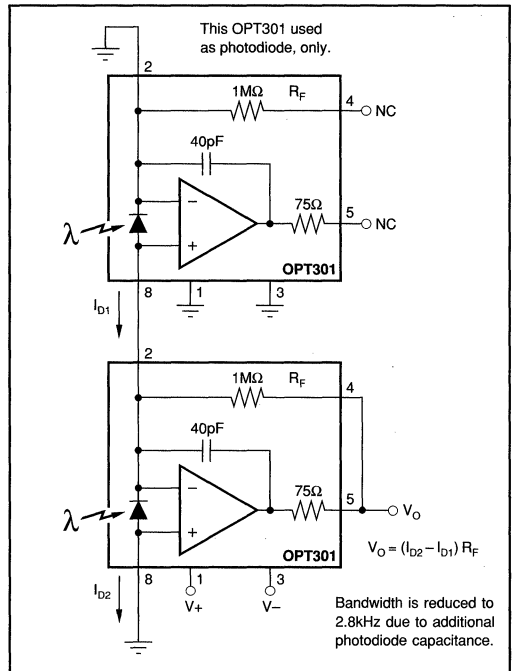


FIGURE 7. Differential Light Measurement.

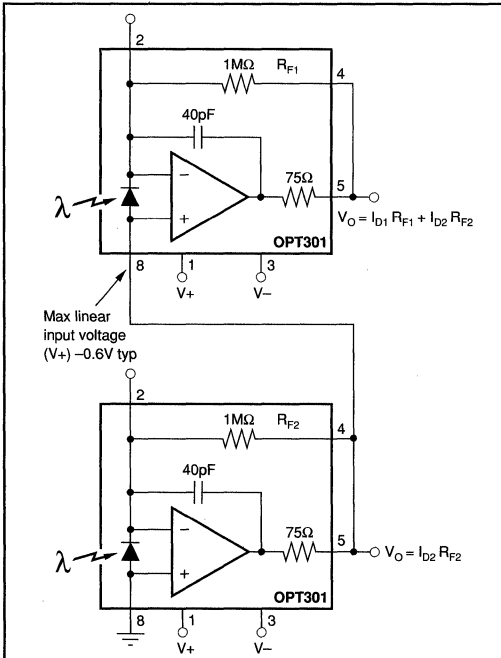


FIGURE 6. Summing Output of Two OPT301s.

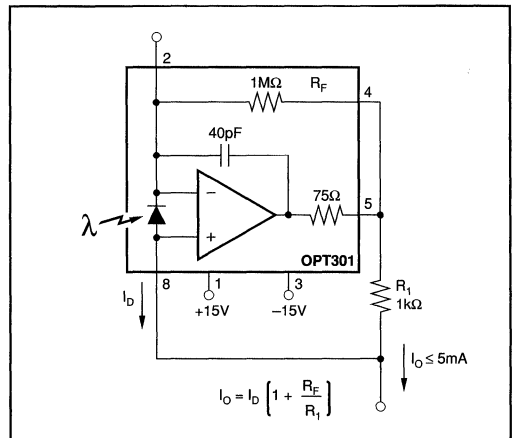


FIGURE 8. Current Output Circuit.

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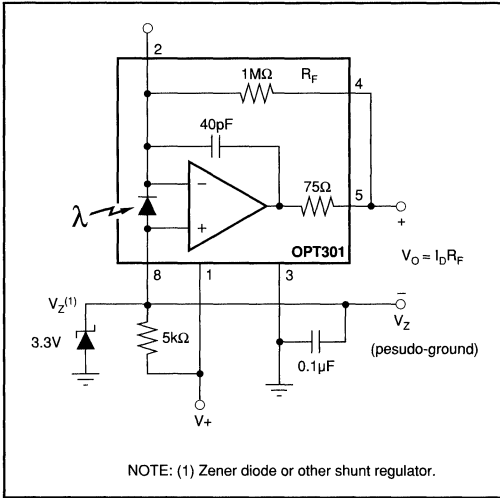


FIGURE 9. Single Power Supply Operation.

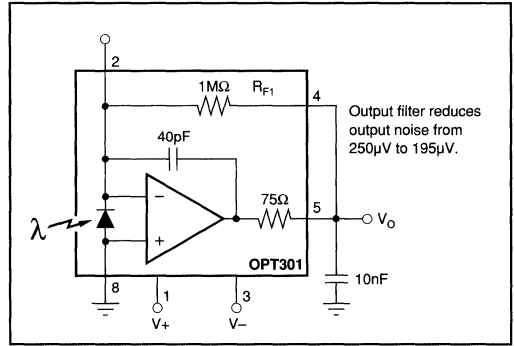


FIGURE 10. Output Filter to Reduce Noise.

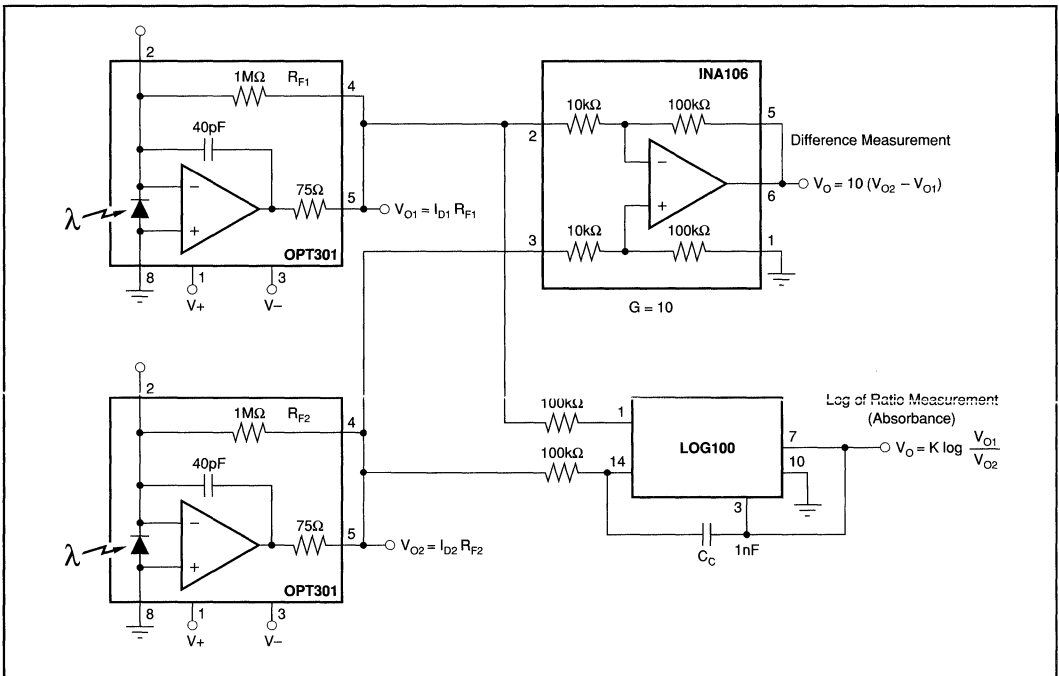


FIGURE 11. Differential Light Measurement.

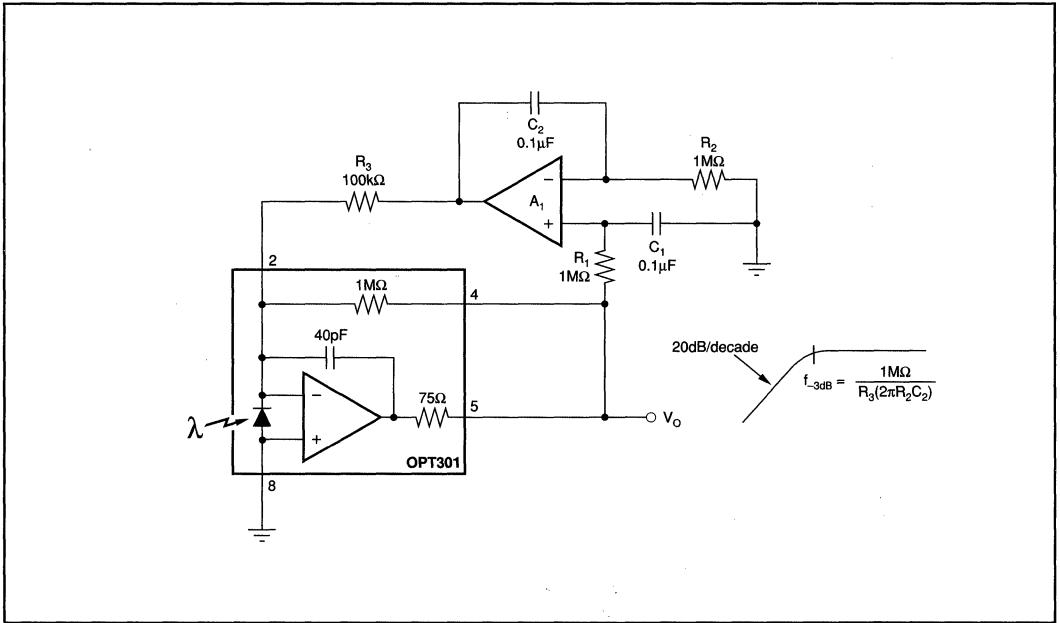


FIGURE 12. DC Restoration Rejects Unwanted Steady-State Background Light.

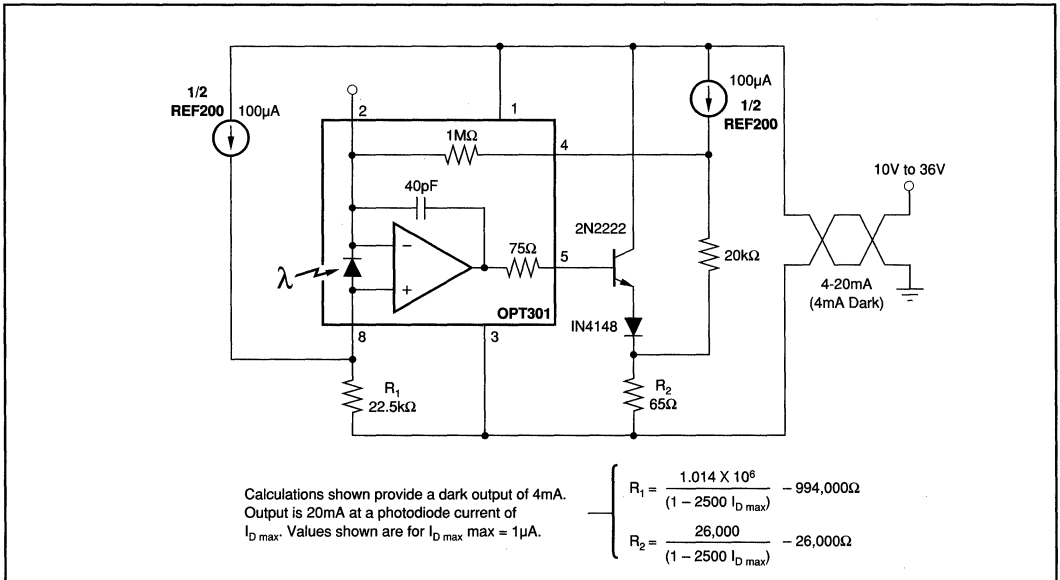


FIGURE 13. 4-20mA Current-Loop Transmitter.

7 Special Functions

Some analog circuit functions defy classification. In this section you will find a diverse assortment of circuit functions—at least one is bound to be your hidden treasure! Consider some of the possibilities:

UAF42—Universal Analog Filter. Add only external resistors and make a wide range of low-pass, high-pass, band-pass and notch filters.

ACF2101—Dual Integrating Transimpedance Amplifier. Integrates input signal currents for a user-determined period of time. Measures tiny currents without using high value resistors.

MPY634—Analog Multiplier. Output is equal to the product of two input voltages. Useful in communications (modulation and mixing), power measurement, computation and linearization.

LOG100—Logarithmic Amplifier. Output is proportional to the logarithm of the ratio of two input currents. Useful as computational element—calculating decibels, for instance.

Explore this selection guide to find your hidden treasure—

SPECIAL FUNCTIONS

Function	Model	Description	Comments	Temp Range ⁽¹⁾	Pkg	Page No.
Multifunction Converter	4302	Y (Z/X) ^m This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Plastic Package.	Ind	DIP	7.110
Logarithmic Amplifier	LOG100	K Log (I ₁ /I ₂)	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP	7.28
	4127	K Log (I ₁ /I _{REF})	A more versatile part that contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com	DIP	7.102
	4341	True rms-to-DC conversion based on a log-antilog proportional approach. Pin compatible with 4340.	Some external trimming required. Lower cost in plastic package.	Ind	DIP	7.117
Switched Integrator	ACF2101	This is a dual, integrating, transimpedance amplifier that converts an input current to an output voltage by integrating the current for a user determined period of time. Eliminates large feedback resistor of traditional I to V converters.	Includes HOLD and RESET switches and output multiplexer. $V_{OUT} = -\frac{1}{C} \int i_{IN} dt$	Ind	DIP, SOIC	7.3

NOTE: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C.

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MULTIPLIERS/DIVIDERS Boldface = NEW

Model	Transfer Function	Error at +25°C max (%)	Temp Coeff (%/°C)	Feed-through (mV)	Offset Voltage (mV)	1% BW (MHz)	Temp Range ⁽¹⁾	Pkg	Page No.
MPY100	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.5	0.008	30	7	0.07	Ind	TO-100	7.37
MPY534	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.25	0.008	0.05%	2	3	Com	TO-100	7.49
MPY600	$[(X_1 - X_2)(Y_1 - Y_2)/2] + Z_2$	±0.025	0.02	2	5	10	Ind	DIP	7.57
MPY634	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$	±0.5	0.015	0.15%	5	10	Ind	TO-100, DIP, SOIC	7.69

NOTE: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, Mil = -55°C to +125°C.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy D = 250mV max (%)	Temp Coeff (%/°C)	0.5% BW (kHz)	Rated Output, min	Temp Range ⁽¹⁾	Pkg	Page No.
DIV100	10 x N/D	250mV to 10V	0.25	0.2	15	±10V, ±5mA	Com	DIP	7.17

NOTE: (1) Com = 0°C to +70°C.

FREQUENCY PRODUCTS Boldface = NEW

Function	Model	Description	Comments	Temp Range ⁽¹⁾	Pkg	Page No.
Oscillator	4423	Very low cost in plastic package. Provides resistor-programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	A
Universal Active Filter	UAF42 UAF41	These filters provide a complex pole pair. State-variable type, low-pass, high-pass, and bandpass outputs.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind	DIP, SOIC DIP	7.96 A

NOTE: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C.

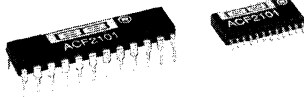
"A" indicates a product that is not included in the 1995 Data Books—contact factory for data sheet.

DC RESTORATION CIRCUIT Boldface = NEW

Function	Model	Description	Comments	Temp Range ⁽¹⁾	Pkg	Page No.
DC Restoration	SHC615	Wide Bandwidth, fast, DC-Restoration circuit for sampling or hum suppression	Bandwidth - OTA: 750kHz Comparator: 280MHz Switching Transients: +1/-7mV Feedthrough Rejection: 100dB	XInd	14-Pin DIP, SOIC	7.77

NOTE: (1) Com = 0°C to +70°C, Ind = -25°C to +85°C, XInd = -40°C to +85°C.

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ACF2101

Low Noise, Dual SWITCHED INTEGRATOR

FEATURES

- INCLUDES INTEGRATION CAPACITOR, RESET AND HOLD SWITCHES, AND OUTPUT MULTIPLEXER
- LOW NOISE: $10\mu\text{Vrms}$
- LOW CHARGE TRANSFER: 0.1pC
- WIDE DYNAMIC RANGE: 120dB
- LOW BIAS CURRENT: 100fA

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- PHOTODIODE INTEGRATOR
- CURRENT MEASUREMENT
- CHARGE MEASUREMENT
- CT SCANNER FRONT END
- MEDICAL, SCIENTIFIC, AND INDUSTRIAL INSTRUMENTATION

DESCRIPTION

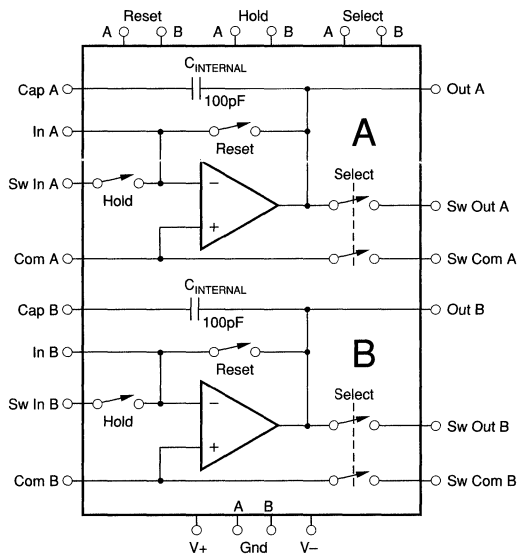
The ACF2101 is a dual switched integrator for precision applications. Each channel can convert an input current to an output voltage by integration, using either an internal or external capacitor. Included on the chip are precision 100pF integration capacitors, hold and reset switches, and output multiplexers.

As a complete circuit on a single chip, the ACF2101 eliminates many of the problems commonly encountered in discrete designs, such as leakage current errors and noise pickup. The integrating approach can provide lower noise than conventional transimpedance amplifier designs and also eliminates the need for high performance, high value feedback resistors.

The extremely low bias current and low noise of the ACF2101's *Difet*[®] amplifiers, along with active laser trimming of both offset and drift, assure precision current to voltage conversion.

Although designed for +5V, -15V supplies, the ACF2101 can be operated on supplies up to $\pm 18\text{VDC}$. It is available in both 24-pin plastic DIP and SOIC packages.

Difet[®] Burr-Brown Corp.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 899-1510 • Immediate Product Info: (800) 548-6132



PDS-1078D

7.3

ACF2101

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SPECIAL FUNCTIONS

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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_+ = +5\text{V}$, $V_- = -15\text{V}$, Internal $C_{\text{INTEGRATION}} = C_{\text{INTERNAL}} = 100\text{pF}$, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU			UNITS
		MIN	TYP	MAX	
ANALOG INPUT					
INPUT RANGE Input Current Range Switched Input (Sw In A, Sw In B) Direct Input (In A, In B)				± 100 ± 100	μA μA
INPUT IMPEDANCE Switched Input Hold Switch OFF Hold Switch ON Direct Input			1000 1.5 Virtual Ground		$\text{G}\Omega$ $\text{k}\Omega$
HOLD SWITCH VOLTAGE Hold Switch Withstand Voltage	Hold Switch OFF	-10		+0.5	V
OFFSET VOLTAGE Input Offset Voltage Average Drift			± 0.5 ± 1	± 2 ± 5	mV $\mu\text{V}/^\circ\text{C}$
DIGITAL INPUTS					
Logic Family V_{HI} (Logic 1 = Switch OFF) V_{LO} (Logic 0 = Switch ON) I_{HI} I_{LO} Switching Speed (All Switches) Switch ON Switch OFF	TTL Compatible $V_{\text{HI}} = +5\text{V}$ $V_{\text{LO}} = 0\text{V}$	2 -0.5	2 0	5.5 0.8	V V μA μA ns ns
TRANSFER CHARACTERISTICS					
TRANSFER FUNCTION			$V_{\text{OUT}} = -\frac{1}{C_{\text{INTEGRATION}}} \int I_{\text{IN}} dt$		V
DYNAMIC CHARACTERISTICS Integrate Mode Slew Rate Reset Mode Slew Rate Settling Time to 0.01%FSR ⁽¹⁾ Overload Recovery Output Multiplexer (Select Switches) Settling Time to 0.01%FSR Settling Time to 0.01%FSR	10V Step Positive or Negative $C_{\text{LOAD}} < 1000\text{pF}$ $C_{\text{LOAD}} < 100\text{pF}$	1	3 3 5 5 6.5 2	10	V/ μs V/ μs μs μs μs μs
INTEGRATION CAPACITOR (C_{INTERNAL}) Internal Capacitor Value Accuracy Temperature Coefficient Memory			100 0.5 -50	2 0 100	pF % $\text{ppm}/^\circ\text{C}$ ppm of FSR
RESET SWITCH Impedance Reset OFF Reset ON			1000 1.5		$\text{G}\Omega$ $\text{k}\Omega$
MODES OF OPERATION Switch Integrate Mode Hold Mode Reset Mode (Logic 1 = OFF, Logic 0 = ON)	Hold Reset ON OFF OFF OFF ON/OFF ON				

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ELECTRICAL (CONT)

At $T_A = +25^\circ\text{C}$, $V_+ = +5\text{V}$, $V_- = -15\text{V}$, Internal $C_{\text{INTEGRATION}} = C_{\text{INTERNAL}} = 100\text{pF}$, unless otherwise noted.

PARAMETER	CONDITIONS	ACF2101BP, BU			UNITS
		MIN	TYP	MAX	
OUTPUT					
Voltage Output Range (All Outputs)		-10	-13.5, +1.0	+0.5	V
Current Output, Direct Output (Out A, Out B)		± 5			mA
Short Circuit Current					
Direct Output			± 25		mA
Switched Output (Sw Out A, Sw Out B)			± 8		mA
Select Switch Withstand Voltage					
Switched Output		-10		+0.5	V
Switched Common (Sw Com A, Sw Com B)		-0.5		+0.5	V
Output Impedance			0.1		Ω
Direct Output					
Switched Output					
Select Switch ON			250 5		Ω pF
Select Switch OFF			1000 4		G Ω pF
Leakage Current	Select Switch OFF		10	100	pA
Load Capacitance Stability					
Direct Output			500		pF
Switched Output			Any		pF
OUTPUT ACCURACY					
Nonlinearity			± 0.005	± 0.01	%FSR
Channel Separation			-80		dB
Op Amp Bias Current					
Value			100	1000	fA
Temperature Coefficient			Doubles Each +10°C		
Hold Mode Droop			1	10	nV/ μ s
Integrate Mode Droop			1	10	nV/ μ s
Voltage Offset ⁽²⁾					
Value			3		mV
Temperature Coefficient			5		$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection	$V_S = +4.5\text{V to }+18\text{V}, -10\text{V to }-18\text{V}$	80	100		dB
OUTPUT NOISE					
Total Output Noise ⁽³⁾	BW = 0.1Hz to 10Hz		2		μVrms
Integrate Mode ⁽⁴⁾	BW = 0.1Hz to 250kHz		$10(1 + C_N/C_{\text{INTEGRATION}})$		μVrms
Hold Mode	BW = 0.1Hz to 250kHz		10		μVrms
Reset Mode	BW = 0.1Hz to 250kHz		10		μVrms
CHARGE TRANSFER ERRORS⁽⁵⁾					
Reset to Integrate Mode ⁽⁶⁾					
Charge Transfer			0.1	0.5	pC
Charge Transfer TC			0.2		fC/ $^\circ\text{C}$
Charge Offset Error			1	5	mV
Charge Offset TC			2		$\mu\text{V}/^\circ\text{C}$
Integrate to Hold Mode		$C_N > 50\text{pF}$			
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/ $^\circ\text{C}$
Charge Offset Error			2	10	mV
Charge Offset TC			4		$\mu\text{V}/^\circ\text{C}$
Hold to Integrate Mode		$C_N > 50\text{pF}$			
Charge Transfer			0.2	1	pC
Charge Transfer TC			0.4		fC/ $^\circ\text{C}$
Charge Offset Error			2	10	mV
Charge Offset TC			4		$\mu\text{V}/^\circ\text{C}$
POWER SUPPLY					
Specified Operating Voltage			+5, -15		V
Operating Voltage Range					
Positive Supply		+4.5		+18	V
Negative Supply		-10		-18	V
Current					
Positive Supply	For Dual		12	15	mA
Negative Supply	For Dual		3.5	5.2	mA
TEMPERATURE RANGE					
Specification		-40		+85	$^\circ\text{C}$
Operation		-40		+125	$^\circ\text{C}$
Storage		-40		+125	$^\circ\text{C}$
Thermal Resistance (both packages)	Junction to Ambient		100		$^\circ\text{C}/\text{W}$

NOTES: (1) FSR is Full Scale Range = 10V (0 to -10V). (2) Includes offset errors from all modes of operation. (3) Total noise is rms total of noise for the modes of operation used. (4) C_N = capacitance of sensor connected to ACF2101 input; $C_{\text{INTEGRATION}}$ = integration capacitance = $C_{\text{INTERNAL}} + C_{\text{EXTERNAL}}$. (5) Errors created when the internal switches are driven from one mode to another. (6) The charge transfer is 0.1pC; for an integration capacitance of 100pF, the resultant charge offset voltage error is 1mV.



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ABSOLUTE MAXIMUM RATINGS

Supply	±18V
Input Current	±5mA
Output Short Circuit Duration	Continuous to Ground
Power Dissipation	500mW
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
ACF2101BP	24-Pin Plastic DIP	-40°C to +85°C
ACF2101BU	24-Pin Plastic SOIC	-40°C to +85°C

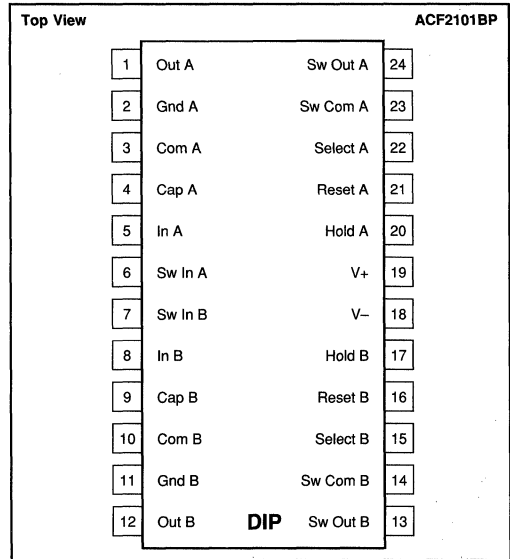
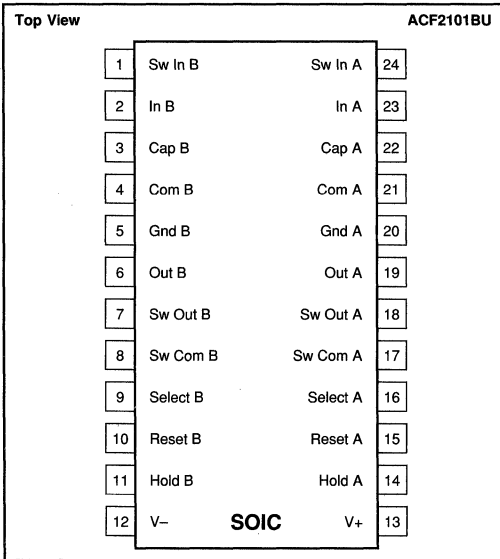
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ACF2101BP	24-Pin Plastic DIP	243
ACF2101BU	24-Pin Plastic SOIC	239

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

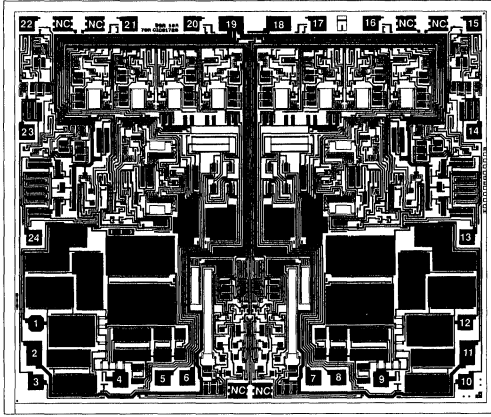
PIN CONFIGURATION

DIP and SOIC package have different pinouts.



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DICE INFORMATION



ACF2101 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	A Out	13	B Switch-Out
2	A Ground	14	B Switch-Common
3	A Common	15	B Select
4	A Cap	16	B Reset
5	A In	17	B Hold
6	A Switch-In	18	V-
7	B Switch-In	19	V+
8	B In	20	A Hold
9	B Cap	21	A Reset
10	B Common	22	A Select
11	B Ground	23	A Switch-Common
12	B Out	24	A Switch-Out

Substrate Bias: Ground.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	132 x 157 ±5	3.35 x 3.99 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

ACF2101

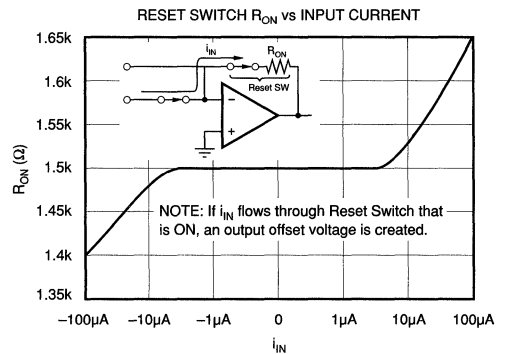
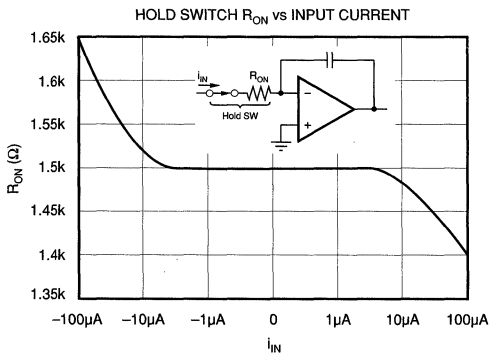
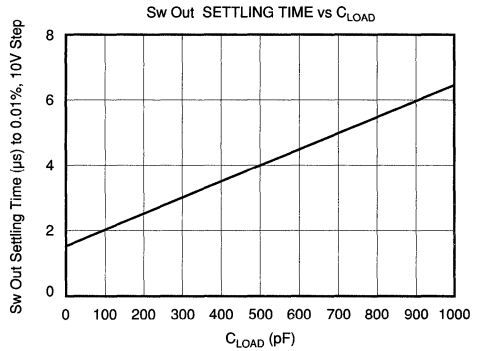
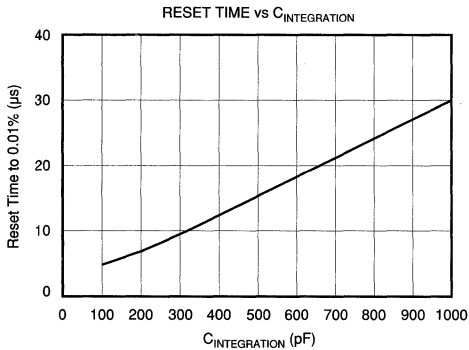
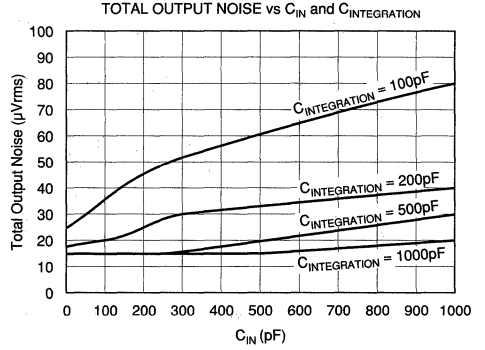
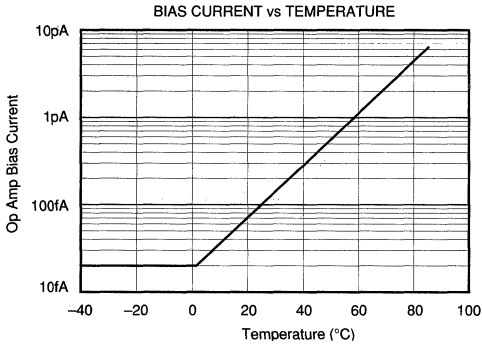
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SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, $V_+ = +5\text{V}$, $V_- = -15\text{V}$, $C_{\text{INTEGRATION}} = C_{\text{INTERNAL}} = 100\text{pF}$, unless otherwise noted.



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APPLICATIONS INFORMATION

BASIC CIRCUIT CONNECTION

Basic Layout

As with any precision circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the analog and digital input pins.

Figures 1a and 1b illustrate the basic connections needed for operation. Figures 1c and 1d illustrate the addition of external integration capacitors and input guards.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the ACF2101. A circuit board “guard” pattern reduces leakage effects by surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential. Leakage will flow harmlessly to the low impedance node. Figure 2a and 2b show printed circuit patterns that can be used to guard critical pins. Note that traces leading to these pins should also be guarded.

Improper handling or cleaning may increase droop. Contamination from handling parts and circuit boards can be removed with cleaning solvents and de-ionized water.

Pinout

The pinout for the DIP and SOIC package of the ACF2101 is different. The pinouts for the different packages are shown in several figures in this data sheet.

Power Supplies

The ACF2101 can operate from supplies that range from +4.5V and -10V to $\pm 18V$. Since the output voltage integrates negatively from ground, a positive supply of +5V is sufficient to attain specified performance. Using +5V and -15V power supplies reduces power dissipation by one-half of that at $\pm 15V$.

Power supply connections should be bypassed with good high-frequency capacitors, such as 1 μF solid tantalum capacitors, positioned close to the power supply pins.

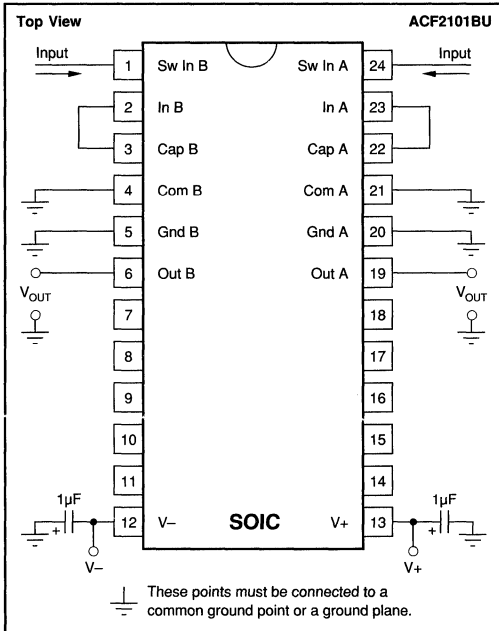


FIGURE 1a. Basic Circuit Connections, SOIC package.

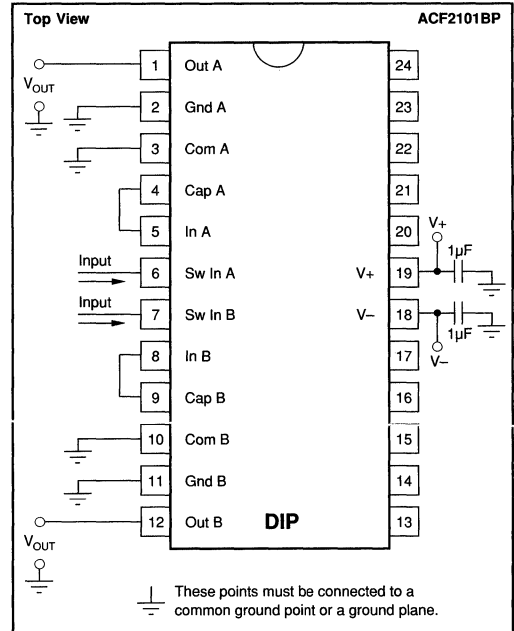


FIGURE 1b. Basic Circuit Connections, DIP.

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SPECIAL FUNCTIONS

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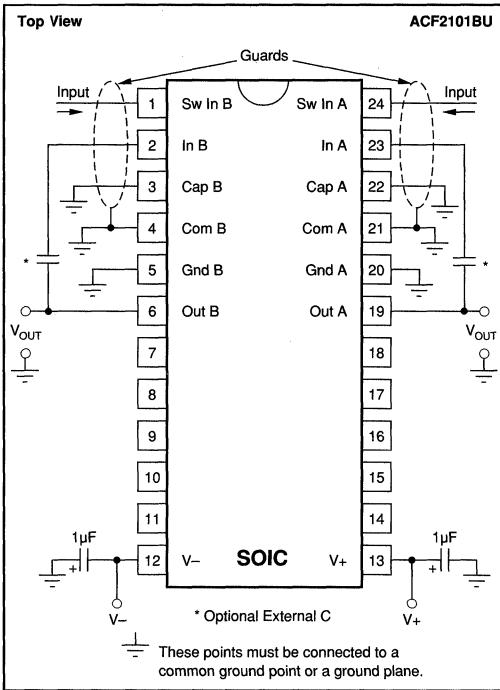


FIGURE 1c. Circuit Connections with External Capacitors and Guarding, **SOIC** package.

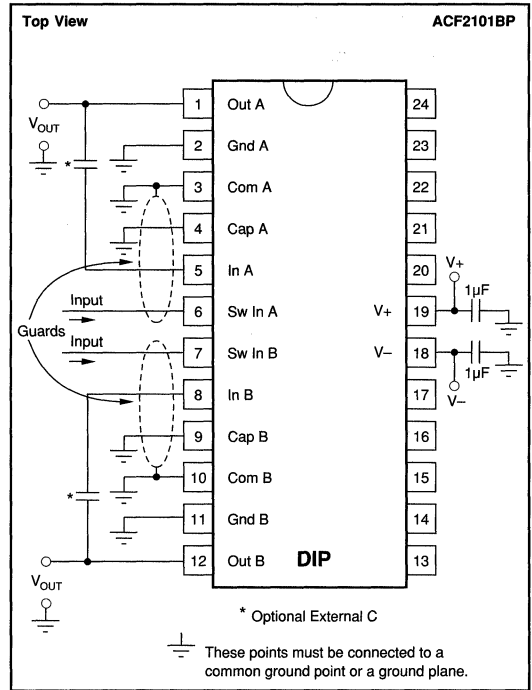


FIGURE 1d. Circuit Connections with External Capacitors and Guarding, **DIP**.

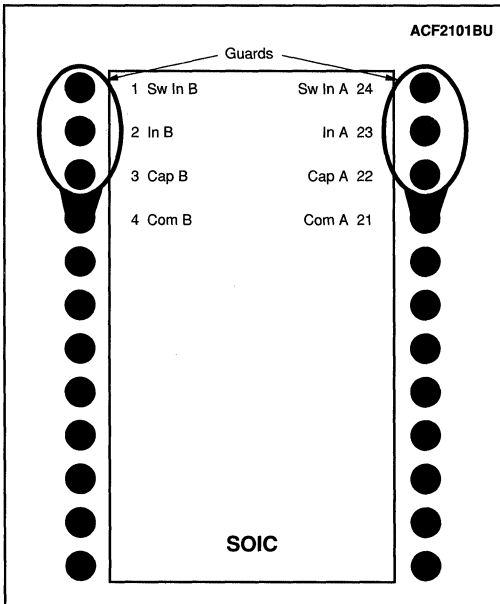


FIGURE 2a. PC Board Layout Showing “Guard” Traces for Input, **SOIC** package. Both top and bottom of board should be guarded.

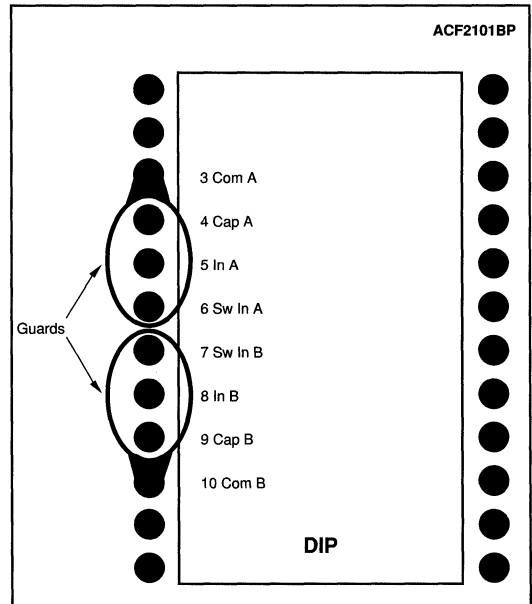


FIGURE 2b. PC Board Layout Showing “Guard” Traces for Input, **DIP**. Both top and bottom of board should be guarded.

MODES OF OPERATION

The three basic modes of operation of each integrator are controlled by the Hold and Reset switches. In Integrate mode, the output voltage integrates negatively toward $-10V$. In Hold mode, the output voltage remains at the present value, except for output droop. In Reset mode, the integration capacitor is discharged and the output voltage is driven to analog common. See Figure 4.

SWITCHES

Each integrator includes four switches: a Hold switch, a Reset switch, and two output Select switches. See Figure 3.

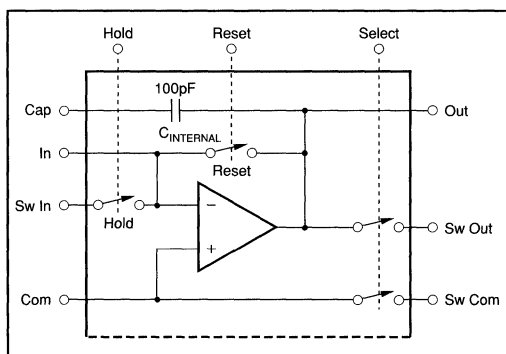


FIGURE 3. Switch Control Lines on One Channel of Two in ACF2101.

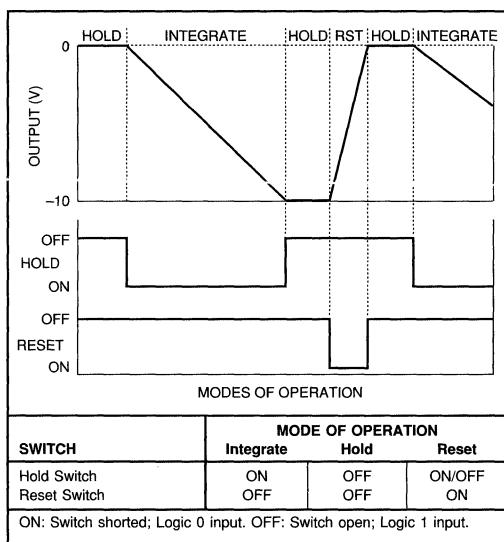


FIGURE 4. Modes of Operation.

Hold and Reset Switches

To use the Hold switch, connect the input current to the "Sw In" pin. The Hold switch disconnects the input current, and holds the output voltage at a fixed level. For direct input, connect the input current to the "In" pin that bypasses the Hold switch and connects directly to the input summing junction. If the Hold switch is not used, the switch should be in the off mode and the "Sw In" pin should be connected to analog common.

The Reset switch is used to discharge the integration capacitor before the start of a new integration period. See Typical Performance Curve showing Reset Time vs $C_{INTEGRATION}$.

Select Switches

The two Select switches can be used to multiplex the outputs when multiple integrators are connected to a common bus. Figure 5 shows a number of ACF2101s multiplexed together into an A/D converter. The output settling time is determined by the Select switch "on" resistance of 250Ω and the total output capacitance. The total output capacitance includes the ACF2101 output capacitances plus the capacitance of the interconnections to the A/D converter.

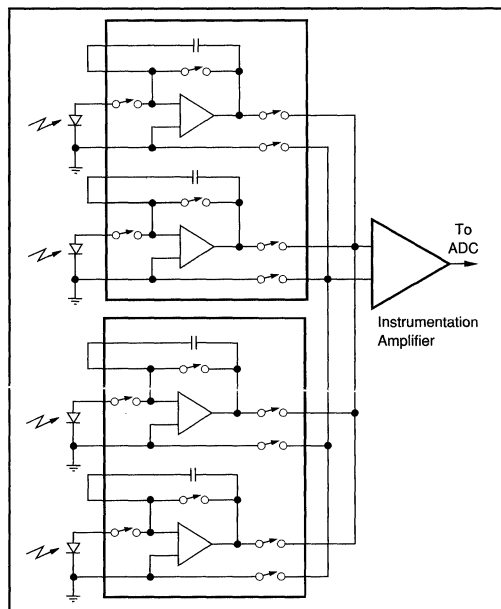


FIGURE 5. ACF2101s in Multiplexed Operation.

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OUTPUT VOLTAGE

The integrator output voltage range is from +0.5V to -10V. The output voltage (V_{OUT}) can be calculated as:

$$V_{OUT} = \frac{i_{IN} \times \Delta t}{C_{INT}}$$

- V_{OUT} = the maximum output voltage (in volts)
- C_{INT} = the integration capacitance (in farads)
- i_{IN} = the input current (in amperes)
- Δt = the integration time (in seconds)

Examples of Component Values for -10V Output

i_{IN} (μ A)	Δt (s)	C_{INT} (PF)	V_{OUT} (V)
0.01	100m	100	-10
0.1	10m	100	-10
1	1m	100	-10
10	100 μ	100	-10
100	10 μ	100	-10
10	1m	1000	-10
100	100 μ	1000	-10

OUTPUT OVERLOAD

When the output to the ACF2101 integrates to the negative limit, the output voltage smoothly limits at approximately 1.5V from the negative power supply, and reset time will increase by approximately 5 μ s for overload recovery. For fastest reset time avoid integrating to the negative limit.

EXTERNAL CAPACITOR

An external integration capacitor may be used instead of or in addition to the internal 100pF integration capacitor. Since the transfer function depends upon the characteristics of the integration capacitor, it must be carefully selected. An external integration capacitor should have low voltage coefficient, temperature coefficient, memory, and leakage current. The optimum selection depends upon the requirements of the specific application. Suitable types include NPO ceramic, polycarbonate, polystyrene, and silver mica. If the internal integration capacitor is not used, the Cap pin should be connected to common.

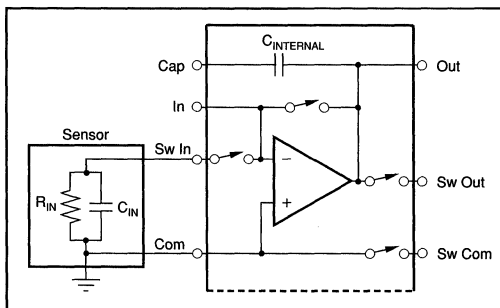


FIGURE 6. Capacitance of Circuit at Input of Integrator.

NOISE

The total output noise for a specific application of the ACF2101 is the rms total of the noise in the modes used: Integrate noise (e_{in}), Hold noise (e_{nh}) and Reset noise (e_{nr}). The noise in both the Hold (e_{nh}) and Reset (e_{nr}) modes is 10 μ Vrms. The noise in the Integrate mode (e_{in}) is directly proportional to one plus the ratio of C_{IN} to $C_{INTEGRATION}$, where C_{IN} is the capacitance of the circuit at the input of the integrator and $C_{INTEGRATION} = C_{INTERNAL} + C_{EXTERNAL}$ and is the integration capacitance:

$$\text{Integrate output noise } (e_{in}) = (10\mu\text{Vrms}) \times (1 + C_{IN}/C_{INTEGRATION})$$

Therefore, for very low C_{IN} , the Integrate noise will approach 10 μ Vrms. The total noise when in the Hold mode after proceeding through Reset and Integrate modes is approximated as shown below.

$$\text{Total Noise} = \sqrt{e_{ih}^2 + e_{ih}^2 + e_{nr}^2}$$

See Typical Performance Curve showing Total Output Noise vs C_{IN} and $C_{INTEGRATION}$ for more accurate noise data under specific circumstances. If only the Integrate and Reset modes are used, the total noise is the rms sum of the noise of the two modes as shown below.

$$\text{Total Noise} = \sqrt{e_{ih}^2 + e_{nr}^2}$$

DYNAMIC CHARACTERISTICS

Frequency Response

The ACF2101 switched integrator is a sampled system controlled by the sampling frequency (f_s), which is usually dominated by the integration time. Input signals above the Nyquist frequency ($f_s/2$) create errors by being aliased into the sampled frequency bandwidth. The sampled frequency bandwidth of the switched integrator has a -3dB characteristic at $f_s/2.26$ and a null at f_s and harmonics $2f_s$, $3f_s$, $4f_s$, etc. This characteristic is often used to eliminate known interference.

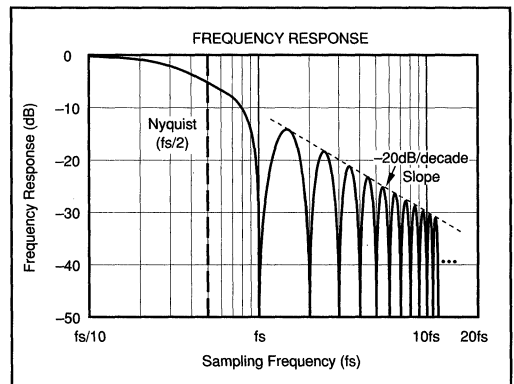


FIGURE 7. Frequency Response.

Charge Transfer

Charge transfer is the charge that is coupled from the logic control inputs through circuit capacitance to the integration capacitor when the Hold and Reset switches change mode. Careful printed circuit layout must be used to minimize external coupling from digital to analog circuitry and the resulting charge transfer. Charge transfer results in a DC charge offset error voltage. The ACF2101 switches are compensated to reduce charge transfer errors.

Since the ACF2101 switches contribute equal and opposite charge for positive and negative logic input transitions, the total error due to charge transfer is determined by the switching sequence. For each switch, a logic transition results in a specific charge (and offset voltage) while an opposite going logic transition results in an opposite charge (and opposite offset voltage). Thus, if the Hold switch is turned on and off during one integration cycle, the total charge transfer at the end of the sequence due to the Hold switch is essentially zero.

The amount of charge transfer to the integration capacitor is constant for each switch. Therefore, the charge offset error voltage is lower for larger integration capacitors. The ACF2101's 0.1pC charge transfer results in a 1mV charge offset voltage when using the 100pF internal integration capacitor. The offset voltage will change linearly with the integration capacitance. That is, 50pF will result in a 2mV charge offset and 200pF in a 0.5mV charge offset.

Droop

Droop is the change in the output voltage over time as a result of the bias current of the amplifier, leakage of the integration capacitor and leakage of the Reset and Hold switches. Droop occurs in both the Integrate and Hold modes of operation. Careful printed circuit layout must be used to minimize external leakage currents as discussed previously.

The droop is calculated by the equation:

$$\text{Droop} = \frac{100\text{fA}}{C_{\text{INTEGRATION}}}$$

where $C_{\text{INTEGRATION}} = C_{\text{INTERNAL}} + C_{\text{EXTERNAL}}$ and is the integration capacitance in farads and the result is in volts per second. For the internal integration capacitance of 100pF, the droop is calculated as:

$$\text{Droop} = \frac{100 \times 10^{-15}}{100 \times 10^{-12}} = 1\text{mV/s or } 1\text{nV}/\mu\text{s}$$

Droop increases by a factor of 2 for each 10°C increase above 25°C. See the typical performance curve showing Bias Current vs Temperature.

Capacitive Loads

Any capacitive load can be safely driven through the multiplexed output of the ACF2101. As with any op amp, however, best dynamic performance of the ACF2101 can be achieved by minimizing the capacitive load. See the typical performance curve showing settling time as a function of capacitive load for more information. A large capacitive

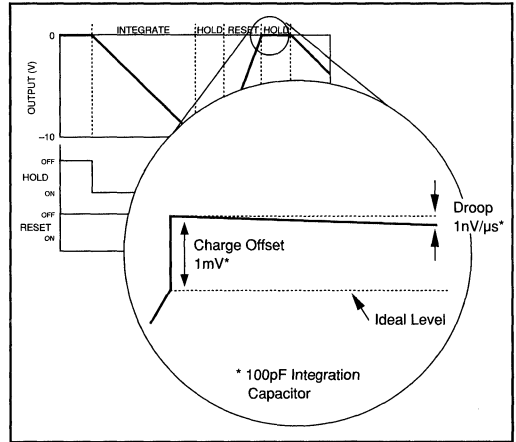


FIGURE 8. Droop and Charge Offset Effects.

load is often useful in reducing the noise of systems not requiring the full bandwidth of the ACF2101.

PROGRAMMABLE I TO V CONVERTER EXAMPLE

Figure 10 illustrates the use of the ACF2101 as a programmable current to voltage converter. The output of the circuit, V_{OUT} , is a DC level for a constant current input. The timing diagram shown in Figure 9 shows V_{OUT} for an input current that varies from one sample to the next. This circuit offers wide dynamic range without the use of extremely large resistors. An ACF2101 and an OPA2107 op amp are configured to convert a low level input current to an output voltage. The equivalent gain of the converter is determined by the frequency of the digital input signal, f_s . The inherent integrating function of the ACF2101 is very useful for rejection of noise such as power line pickup.

The ACF2101 integrates the current signal for the period of f_s . The magnitude of the ramp voltage at the output of the ACF2101 is a function of the frequency of f_s and the value of the integration capacitor, $C_{\text{INTEGRATION}}$. The ACF2101's 100pF internal capacitor is used for $C_{\text{INTEGRATION}}$ in this example. The effect is that f_s controls the equivalent feedback resistance of a transconductance (current-to-voltage) amplifier. The equivalent feedback resistance range can vary over a large range of at least 1MΩ to 1GΩ as illustrated in the accompanying table. Larger equivalent feedback resistances can be obtained if internal capacitances smaller than 100pF are used with the ACF2101.

A simplified equation for the operation of this circuit is:

$$V_{\text{OUT}} = I_{\text{SENSOR}} \times R_{\text{PROGRAM}}$$

Where:

- V_{OUT} is the voltage at the output of the OPA2107,
- I_{SENSOR} is the current into the ACF2101, and
- R_{PROGRAM} is the equivalent feedback resistance of the circuit calculated by the equation,

$$R_{\text{PROGRAM}} = 1/(f_s \times C_{\text{INTEGRATION}}) = 1/(f_s \times 100\text{pF})$$

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For $C_{\text{INTEGRATION}} = 100\text{pF}$, R_{PROGRAM} is calculated below:

f_s	R_{PROGRAM}
10kHz	1M Ω
1kHz	10M Ω
100Hz	100M Ω
60Hz	167M Ω
50Hz	200M Ω
10Hz	1G Ω

At the end of the integration cycle, the Hold switch of the ACF2101 is opened to hold a constant value at the output of the ACF2101. The constant value output voltage of the ACF2101 is transferred onto a 10nF capacitor by closing the ACF2101's Select switch. The Select switch is then opened which holds the voltage on the 10nF capacitor during the next integration cycle and creates a DC output. With this operation, the Select switch of the ACF2101 and the 10nF capacitor form a Sample/Hold (S/H) circuit. The OPA2107 is used to buffer the Sample/Hold output. The charge injection of the Select switch creates a small offset voltage, of approximately 1mV in this example. The 10nF capacitor was chosen as a large value to minimize this offset voltage.

After the Select switch opens, the ACF2101 is reset by momentarily closing the Reset switch. The ACF2101's Hold switch is then closed to begin another integration cycle. During the period of time that the Hold switch is open, the input signal current is stored on the input capacitance of the sensor (C_{IN}). During this time, the input signal current creates a voltage across the sensor. This voltage should be kept below 500mV. When the Hold switch is closed, the charge that has collected on C_{IN} will be transferred to the integration capacitor, $C_{\text{INTEGRATION}}$, with no loss of signal. Therefore, one integration cycle ends and the next integration cycle begins when the Hold switch is opened.

If 100% of signal acquisition is not required, or not wanted, the Hold switch may be left closed, or the direct input to the ACF2101 used. In this mode of operation, an integration cycle ends when the Select switch is opened and the next integration cycle begins when the Reset switch is opened.

Figure 11 shows a simple digital pattern generator which can be used to create the timing signals to control the ACF2101 circuit of Figure 10. This circuit creates signals to control the Select, Reset and Hold switches at a rate controlled by the frequency of f_s . Figure 9 shows the timing diagram for these circuits.

In a sampled data system, the output of the ACF2101 at the output of the Select switch can be converted to digital when the ACF2101 is in the Hold mode. In this situation, of course, the 10nF capacitor and the OPA2107 op amp are not required.

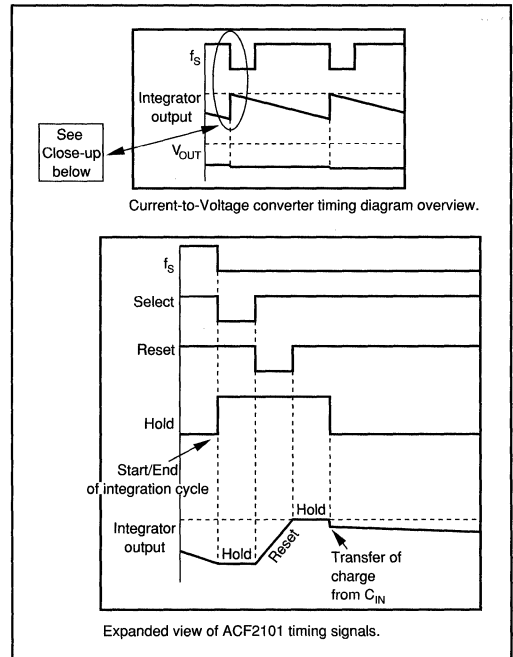


FIGURE 9. ACF2101 Current-to-Voltage Converter Timing Diagram.

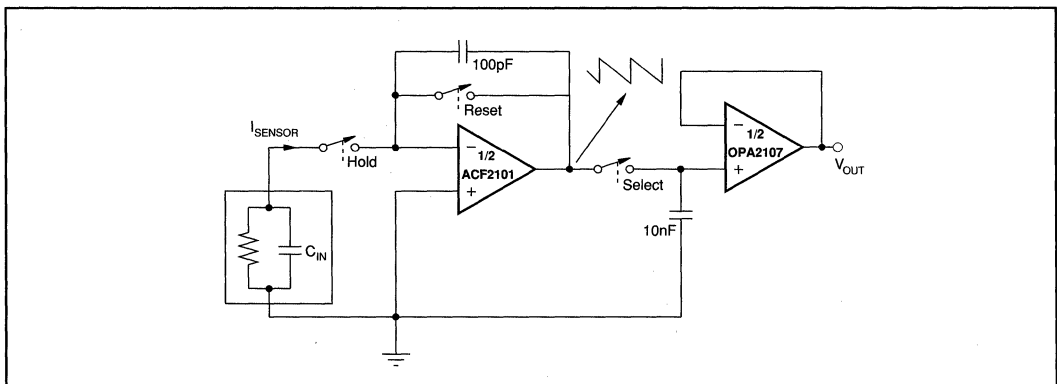


FIGURE 10. Programmable Current-to-Voltage Converter.

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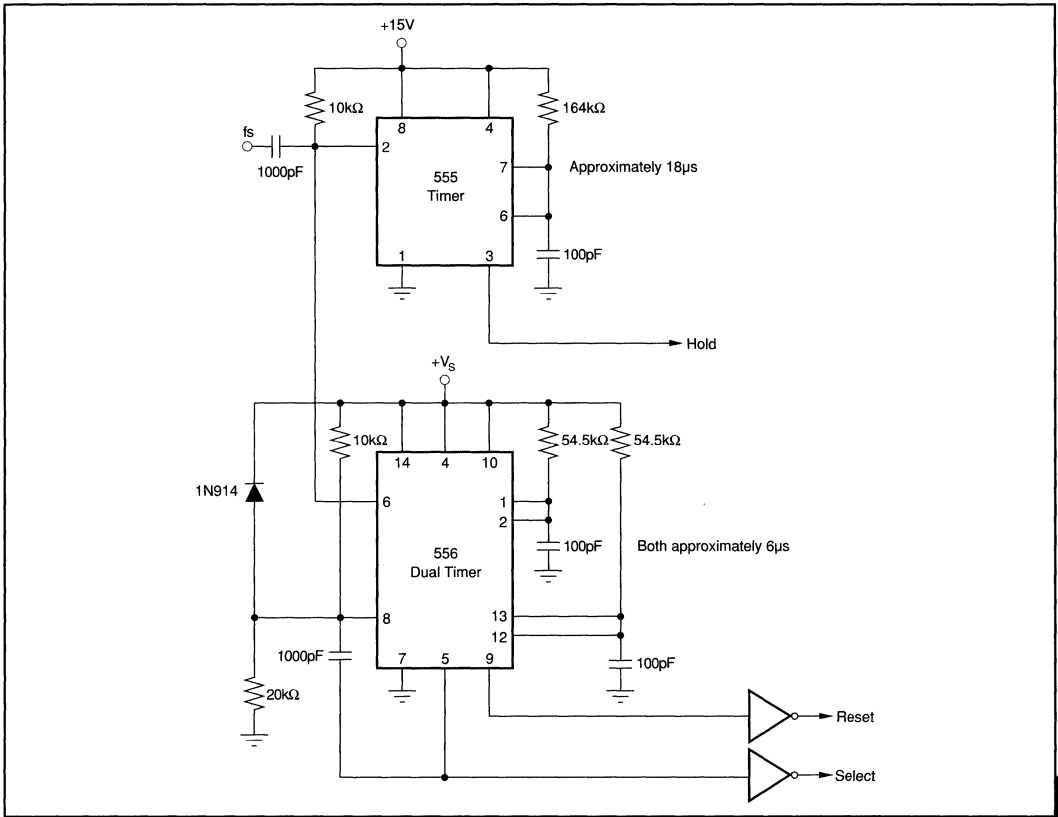


FIGURE 11. Timing Generator.

VOLTAGE INPUT EXAMPLE

Figure 12 illustrates the use of the ACF2101 with a voltage input. This approach is useful in applications where a constant current source is needed. For example, the ACF2101 can be configured in a bipolar mode by using the current generated by a voltage reference as an offset current. In the example in Figure 12, a 10V reference (REF102) is used in series with a 400kΩ resistor to generate a constant +25μA input current to the ACF2101. The ACF2101 will operate as expected in this configuration except in the Hold mode. When the Hold switch is opened, the input to the ACF2101 becomes high impedance and consequently the Sw In node will try to go to 10V. The Hold switch is specified to have a withstand voltage of +0.5V. When the voltage at the Sw In node exceeds +0.5V the Hold switch will begin to conduct again. This will not cause damage to the switch, however, the output will start to unexpectedly integrate again. The addition of either C_1 or D_1 in the circuit is critical for proper Hold mode operation. C_1 will divert the charge being gener-

ated by the voltage source in series with the resistor. C_1 is selected so that the maximum voltage does not exceed 0.4V. When the Hold switch is closed again, the charge collected by C_1 is transferred to the integration capacitor. D_1 will divert the charge being generated by the voltage source and resistor to ground. When the Hold switch closes again, the charge stored on the parasitic capacitor of the diode is transferred to the integration capacitor. D_1 should be selected so that the on voltage of the diode does not exceed 0.4V.

DEMONSTRATION BOARD AND MACROMODEL

Demonstration boards are available to speed prototyping. The demonstration timing board, DEM-ACF2101BP-C includes a programmable timing generator making it easy to do a quick evaluation.

A Spice-based macromodel is also available. Request AB-020 for application note and Burr-Brown's Spice Macromodel diskette.

ACF2101

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SPECIAL FUNCTIONS

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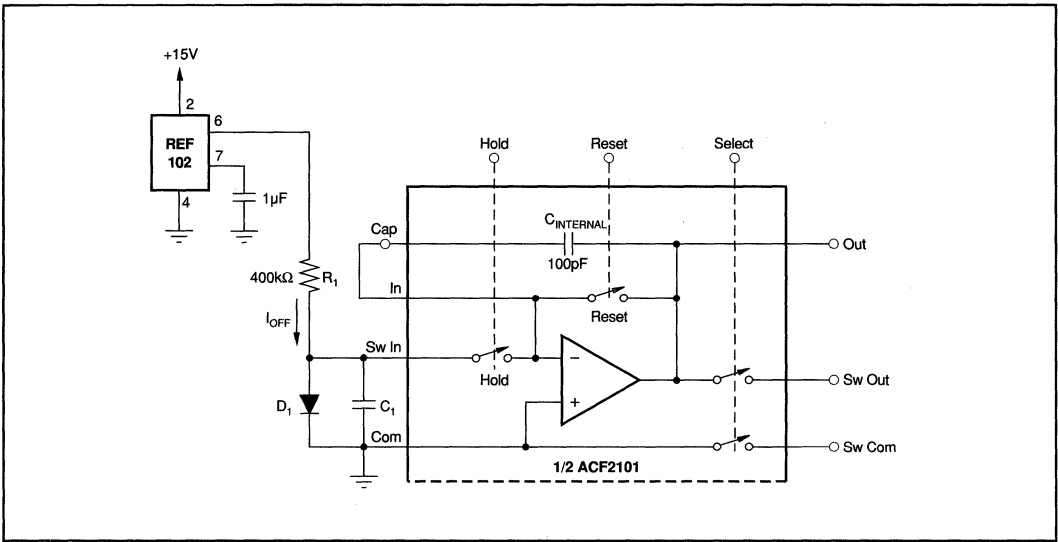
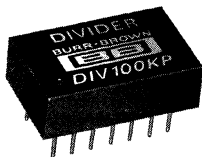


FIGURE 12. Using the ACF2101 with a Voltage Source.

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DIV100

ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY:** 0.25% Maximum Error, 40:1 Denominator Range
- **TWO-QUADRANT OPERATION**
Dedicated Log-Antilog Technique
- **EASY TO USE**
Laser-trimmed to Specified Accuracy
No External Resistors Needed
- **LOW COST**
- **DIP PACKAGE**

APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL AND GAIN CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

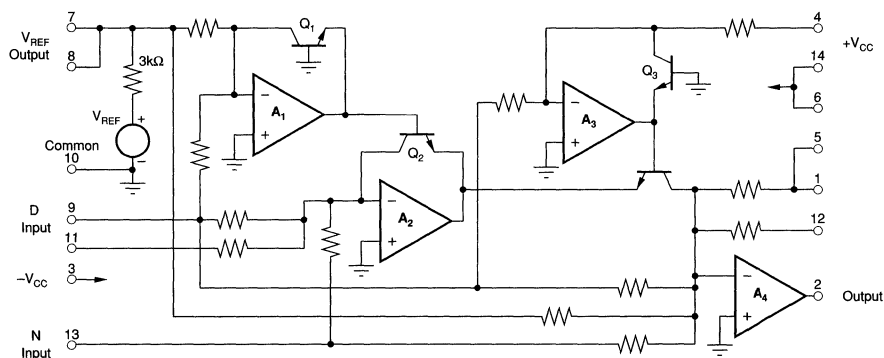
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment — the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies, the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-427B

7.17

DIV100

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SPECIAL FUNCTIONS

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_{CC} = \pm 15\text{VDC}$, unless otherwise specified.

PARAMETER	CONDITIONS	DIV100HP			DIV100JP			DIV100KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER FUNCTION		$V_O = 10\text{N/D}$									
ACCURACY	$R_L \geq 10\text{k}\Omega$										
Total Error											% FSO ⁽¹⁾
Initial	$0.25\text{V} \leq D \leq 10\text{V}, N \leq D $		0.7	1.0		0.3	0.5		0.2	0.25	% FSO/ $^\circ\text{C}$
vs Temperature	$1\text{V} \leq D \leq 10\text{V}, N \leq D $		0.02	0.05 ⁽²⁾		*	*		*	*	% FSO/ $^\circ\text{C}$
vs Supply	$0.25\text{V} \leq D \leq 1\text{V}, N \leq D $		0.06	0.2 ⁽²⁾		*	*		*	*	% FSO/ $^\circ\text{C}$
Warm-up Time to Rated Performance	$0.25\text{V} \leq D \leq 10\text{V}, N \leq D $		0.15			*	*		*	*	% FSO/Minutes
			5			*	*		*	*	
AC PERFORMANCE	$D = +10\text{V}$										
Small-Signal Bandwidth	-3dB		350			*	*		*	*	kHz
0.5% Amplitude Error	Small-Signal		15			*	*		*	*	kHz
0.57° Vector Error	Small-Signal		1000			*	*		*	*	Hz
Full-Power Bandwidth	$V_O = \pm 10\text{V}, I_O = \pm 5\text{mA}$		30			*	*		*	*	kHz
Slew Rate	$V_O = \pm 10\text{V}, I_O = \pm 5\text{mA}$		2			*	*		*	*	V/ μs
Settling Time	$\epsilon = 1\%, \Delta V_O = 20\text{V}$		15			*	*		*	*	μs
Overload Recovery	50% Output Overload		4			*	*		*	*	μs
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	$N \leq D $		± 10			*	*		*	*	V
Denominator	$D \geq +250\text{mV}$		± 10			*	*		*	*	V
Input Resistance	Either Input		25			*	*		*	*	k Ω
OUTPUT CHARACTERISTICS											
Full-Scale Output			± 10			*	*		*	*	V
Rated Output											
Voltage	$I_O = \pm 5\text{mA}$		± 10			*	*		*	*	V
Current	$V_O = \pm 10\text{V}$		± 5			*	*		*	*	mA
Current Limit											
Positive			15	20 ⁽²⁾		*	*		*	*	mA
Negative			19	23 ⁽²⁾		*	*		*	*	mA
OUTPUT NOISE VOLTAGE	$N = 0\text{V}$										
$f_B = 10\text{Hz to } 10\text{kHz}$											
$D = +10\text{V}$			370			*	*		*	*	μVrms
$D = +250\text{mV}$			1			*	*		*	*	mVrms
REFERENCE VOLTAGE CHARACTERISTICS, $R_L \geq 10\text{M}\Omega$											
Output Voltage											
Initial	At 25°C		6.5 ⁽²⁾	6.8	7.1 ⁽²⁾	*	*	*	*	*	V
vs Supply				± 25		*	*		*	*	$\mu\text{V/V}$
Temperature Coefficient				± 50		*	*		*	*	ppm/ $^\circ\text{C}$
Output Resistance				3		*	*		*	*	k Ω
POWER SUPPLY REQUIREMENTS											
Rated Voltage				± 15		*	*		*	*	VDC
Operating Range	Derated Performance		± 12	± 20		*	*		*	*	VDC
Quiescent Current											
Positive Supply			5	7 ⁽²⁾		*	*		*	*	mA
Negative Supply			8	10 ⁽²⁾		*	*		*	*	mA
TEMPERATURE RANGE											
Specification			0	+70		*	*	*	*	*	$^\circ\text{C}$
Operating Temperature	Derated Performance		-25	+85		*	*	*	*	*	$^\circ\text{C}$
Storage			-40	+85		*	*	*	*	*	$^\circ\text{C}$

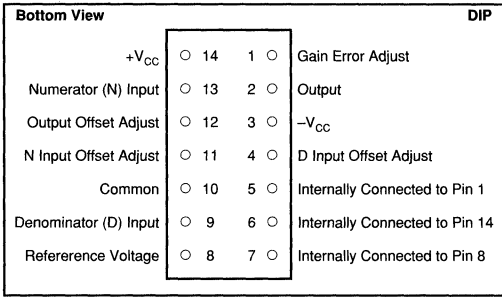
*Same as DIV100HP.

NOTES: (1) FSO is the abbreviation for Full Scale Output. (2) This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.

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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation ⁽¹⁾	600mW
Input Voltage Range ⁽²⁾	±20VDC
Storage Temperature Range	-40°C to +85°C
Operating Temperature Range	-25°C to 85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short-Circuit Duration ^(1, 3)	Continuous
Junction Temperature	+175°C

NOTES: (1) See General Information section for discussion. (2) For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	TOTAL INITIAL ERROR (% FSO)
DIV100HP	0°C to +70°C	1.0
DIV100JP	0°C to +70°C	0.5
DIV100KP	0°C to +70°C	0.25

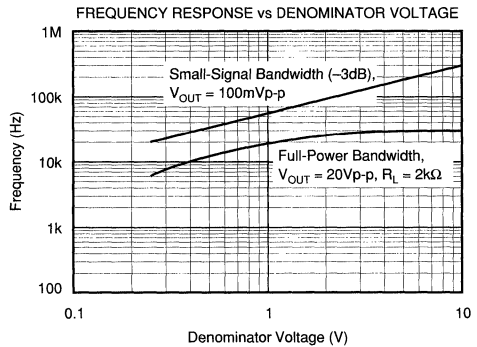
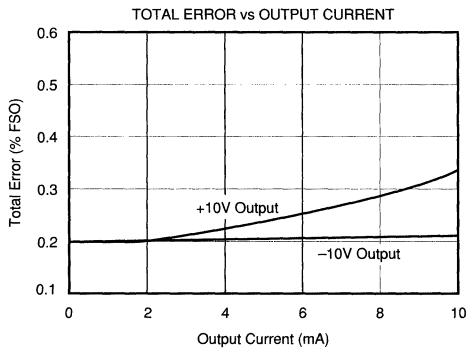
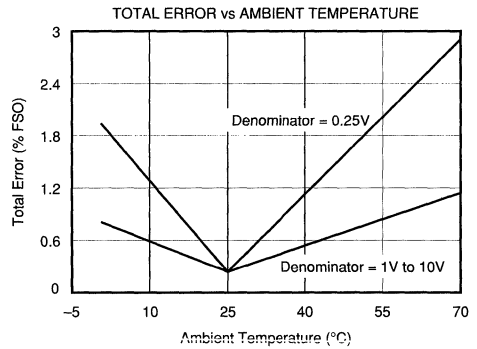
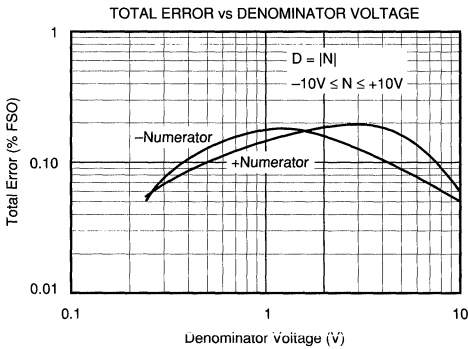
PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
DIV100HP	14-Pin DIP	105
DIV100JP	14-Pin DIP	105
DIV100KP	14-Pin DIP	105

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{cc} = ±15VDC, unless otherwise specified.

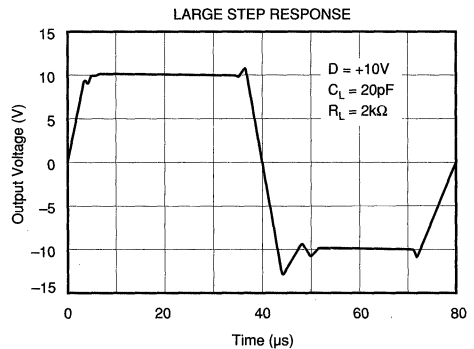
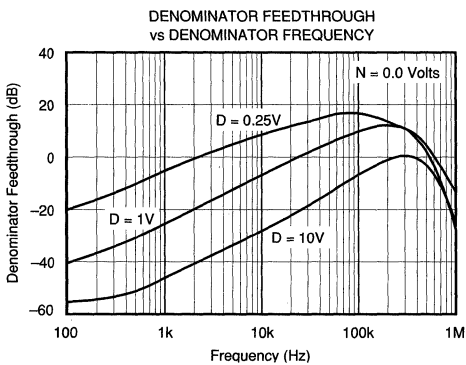
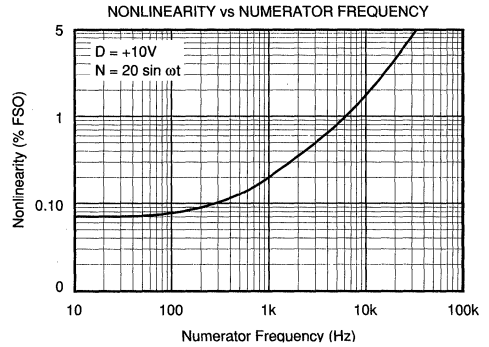
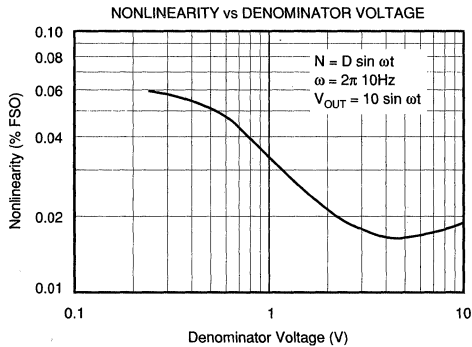
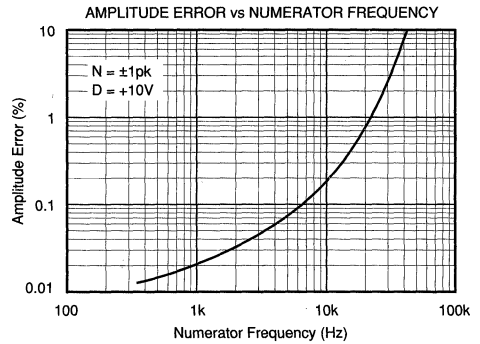
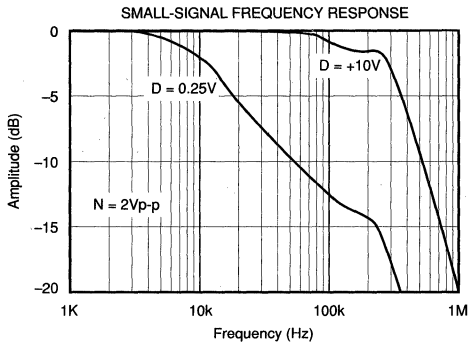


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SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES (CONT)

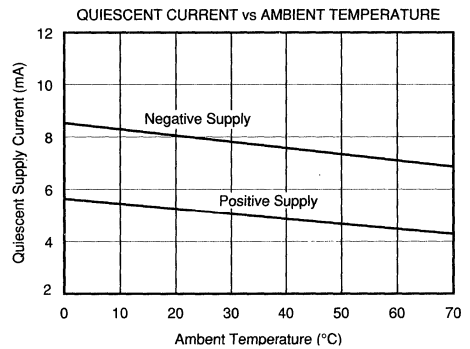
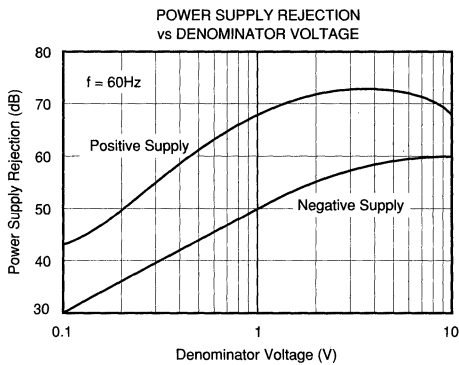
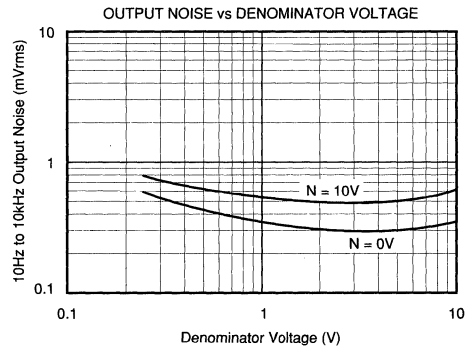
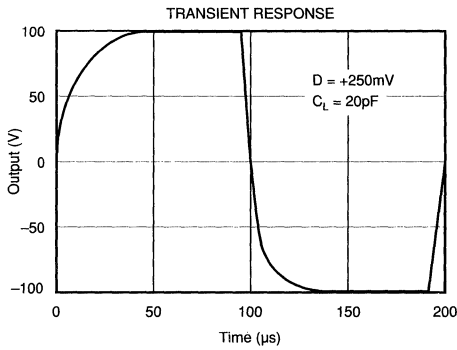
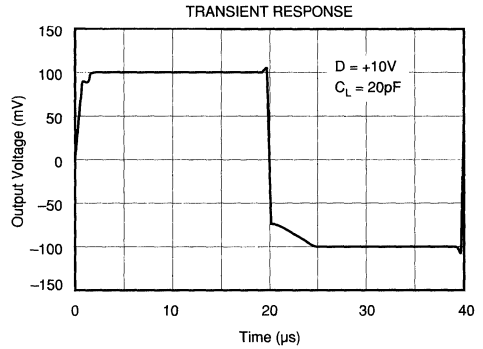
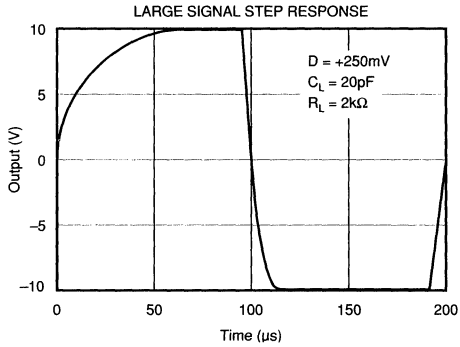
$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$, unless otherwise specified.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$, unless otherwise specified.



DIV100

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SPECIAL FUNCTIONS

DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$$V_{OUT} = 10N/D$$

where: N = Numerator input voltage
 D = Denominator input voltage
 10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

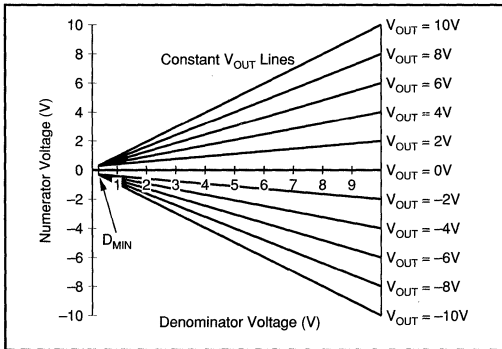


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient $10N/D$ expressed in percent of FSO (10V); e.g., for the DIV100K:

$$V_{OUT(ACTUAL)} = V_{OUT(IDEAL)} \pm \text{total error,}$$

where: Total error = 0.25%, FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mVp-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} = \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally, the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10µF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the +V_{CC} and -V_{CC} pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specifica-

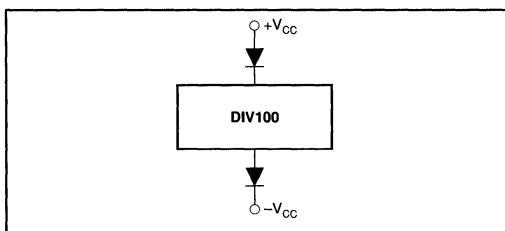


FIGURE 2. Overload Protection Circuit.

tion. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

Figure 3 is the thermal model for the DIV100 where:

- P_{DQ} = Quiescent power dissipation
 $= I+V_{CC} | I_{+QUIESCENT} + I-V_{CC} | I_{-QUIESCENT}$
- P_{DX} = Worst case power dissipation in the output transistor
 $= V_{CC}^2/4R_{LOAD}$ (for normal operation)
 $= V_{CC} I_{OUTPUT LIMIT}$ (for short-circuit)
- T_J = Junction temperature (output loaded)
- T_J^* = Junction temperature (no load)
- T_C = Case temperature
- T_A = Ambient temperature
- θ = Thermal resistance

This model is a multiple power source model to provide a more accurate simulation.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

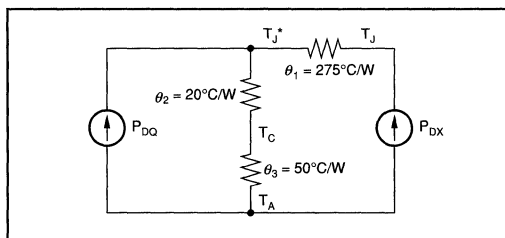


FIGURE 3. DIV100 Thermal Model.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. $V_{CC} = \pm 15VDC$.

$$P_{D(MAX)} = 600mW. T_{J(MAX)} = +175^{\circ}C.$$

$$T_A = T_{J(MAX)} - P_{DQ} (\theta_2 + \theta_3) - P_{DX(SHORT - CIRCUIT)} (\theta_1 + \theta_2 + \theta_3)$$

$$= 175^{\circ}C - 18^{\circ}C - 119^{\circ}C = 38^{\circ}C$$

$$P_{D(ACTUAL)} = P_{DQ} + P_{DX(SHORT - CIRCUIT)} \leq P_{D(MAX)}$$

$$= 255mW + 345mW = 600mW$$

The conclusion is that the device will withstand a short-circuit up to $T_A = +38^{\circ}C$ without exceeding either the $175^{\circ}C$ or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to $\pm 11V$, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

The logarithmic equation for a bipolar transistor is:

$$V_{BE} = V_T \ln(I_C/I_S), \quad (1)$$

where: $V_T = kT/q$

k = Boltzmann's constant = 1.381×10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602×10^{-19}

I_C = Collector current

I_S = Reverse saturation current

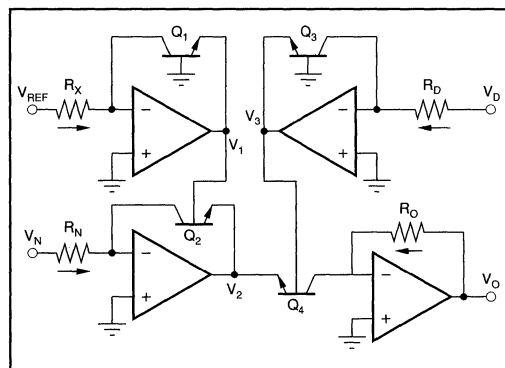


FIGURE 4. One-Quadrant Log-Antilog Divider.

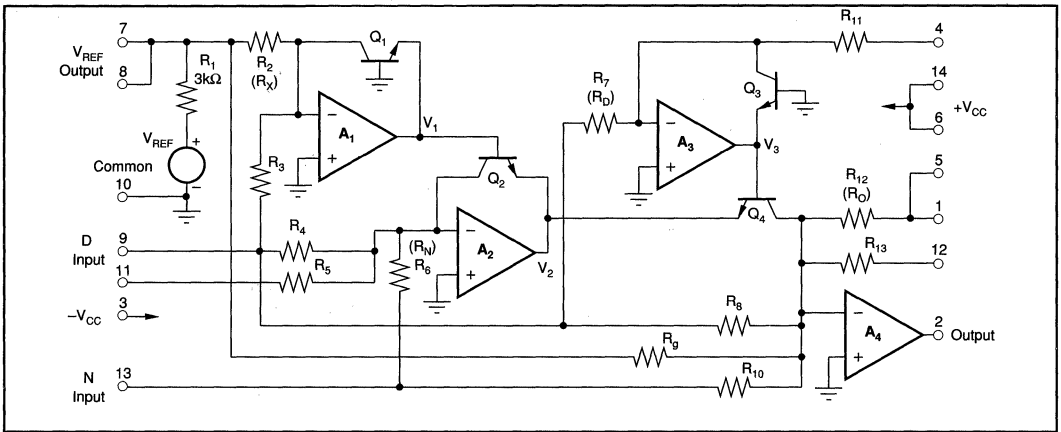


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

Applying equation (1) to the four logging transistors gives:

For Q_1 :

$$V_{BE} = V_B - V_E = V_T [\ln(V_{REF}/R_X - \ln I_S)]$$

This leads to:

$$V_1 = -V_T [\ln(V_{REF}/R_X - \ln I_S)]$$

For Q_2 :

$$V_1 - V_2 = V_T [\ln(V_N/R_N) - \ln I_S]$$

For Q_3 :

$$V_3 = -V_T [\ln(V_D/R_D) - \ln I_S]$$

We have now taken the logarithms of the input voltage V_{REF} , V_N , and V_D . Applying equation (1) to Q_4 gives:

$$V_3 - V_2 = V_T [\ln(V_O/R_O) - \ln I_S].$$

Assume V_T and I_S are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_O = \frac{V_{REF} V_N R_O R_D}{V_D R_X R_N} \quad (2)$$

In the DIV100 $V_{REF} = 6.6V$, $R_O = R_N = R_D$, and R_X is such that the transfer function is:

$$V_O = 10N/D \quad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3 , R_4 , R_8 , R_9 , and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function in equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is that the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met, V_O will try to be greater than the 10V output voltage limit of A_4 .

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With $R_{SOURCE} = 10\Omega$ and $R_{INPUT(DIV100)} = 25k\Omega$ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.8VDC, typically. Its Thevenin equivalent resistance is $3k\Omega$. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the $3k\Omega$ resistor will effect the DIV100 scale factor.

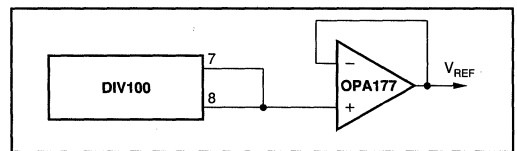


FIGURE 6. Buffered Precision Voltage Reference.

OPTION ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. Begin with R_1 , R_2 , and R_3 set to their mid-position.
2. With $|N| = D = 10.000V$, $\pm 1mV$, adjust R_1 for $V_o = +10.000V$, $\pm 1mV$. This sets the scale factor.
3. Set D to the minimum expected denominator voltage. With $N = -D$, adjust R_2 for $V_o = -10.000V$. This adjusts the output referred denominator offset errors.
4. With D still at its minimum expected value, make $N = D$. Adjust R_3 for $V_o = 10.000V$. This adjusts the output referred offset errors.
5. Repeat steps 2-4 until the best accuracy is obtained.

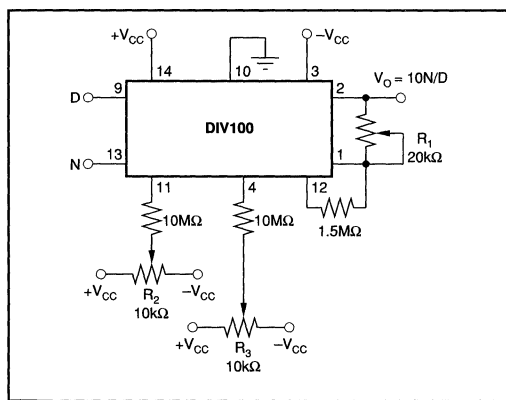


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

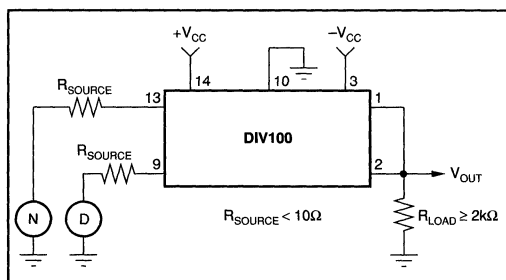


FIGURE 8. Connection Diagram—Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material

F = Force

g = Acceleration due to gravity

a = Acceleration (acting on body of weight W)

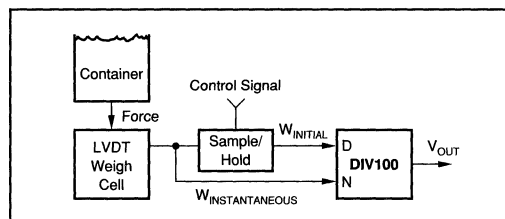


FIGURE 9. Weighing System - Fractional Loss.

In a fractional loss weighing system, the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D -input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

$$\text{Loss (L)} = W_{\text{INSTANTANEOUS}}/W_{\text{INITIAL}}$$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11, the DIV100 output varies as the percent deviation of the measured variable to the standard.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or

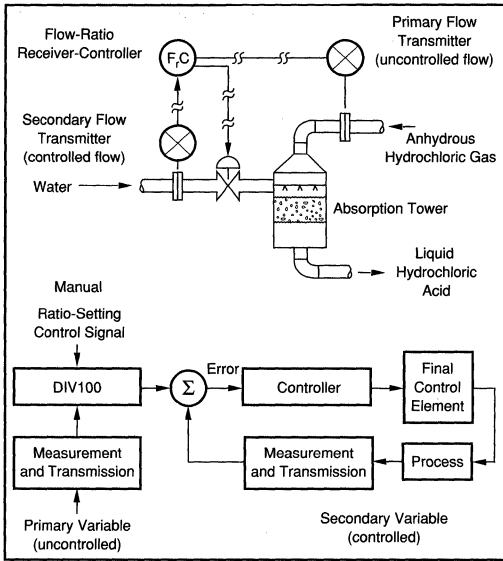


FIGURE 10. Ratio Control of Water to Hydrochloric Gas.

more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation, the bridge in Figure 13 has only one active arm.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A = \frac{-V_{EX}\delta}{2(2 + \delta)}$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps $\pm 10\%$ variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta R_{IN}}{(2R_1 + 3R_{IN})(2 + \delta)} ; \text{ and,}$$

$$D = \frac{2V_{EX} R_{ID}}{(2R_1 + 3R_{ID})(2 + \delta)}, \text{ respectively,}$$

where: R_{IN} = DIV100 numerator input resistance
 R_{ID} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_O = 10N/D = \frac{(2R_1 + 3R_{ID})(R_{IN}\delta) 10}{(2R_1 + 3R_{IN})(2R_{ID})}$$

which reduces to:

$$V_O = -5\delta$$

if the divider's input resistances are equal.

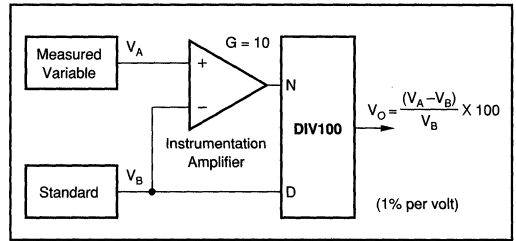


FIGURE 11. Percentage Computation.

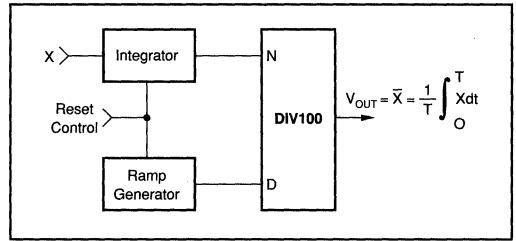


FIGURE 12. Time Averaging Computation Circuit.

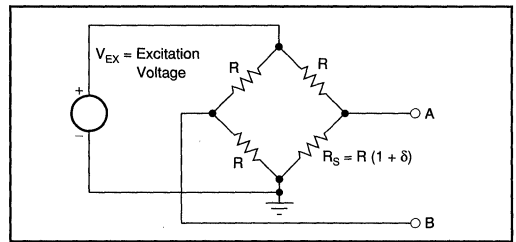


FIGURE 13. Bridge Circuit.

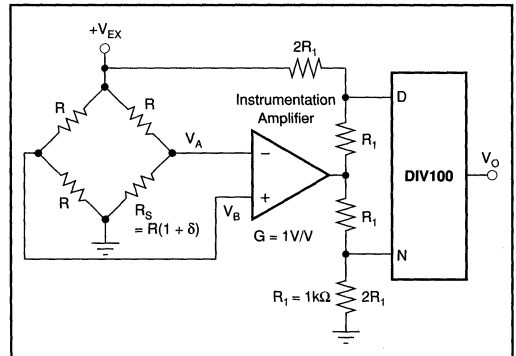


FIGURE 14. Bridge Linearization Circuit.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1 , R_3 , and C_2 . It is then compared to the DC reference voltage. If a difference exists, the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The

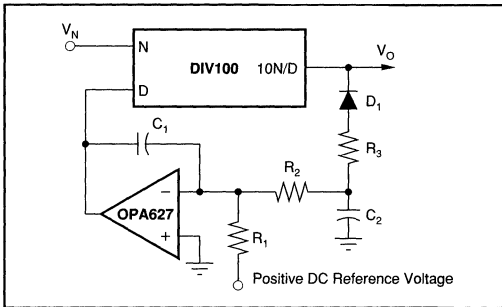


FIGURE 15. Automatic Gain Control Circuit.

transfer function is:

$$\frac{V_{OUT}(S)}{V_{IN}(S)} = \frac{K}{\tau S + 1}$$

where: $K = -R_2/R_1$

$$\tau = \frac{10 R_3 C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearly proportional to the circuit's control voltage.

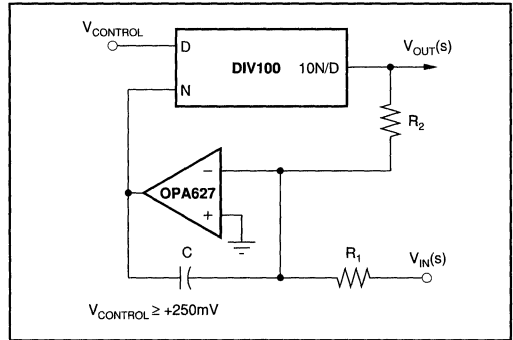


FIGURE 16. Voltage-Controlled Filter.

SQUARE ROOT

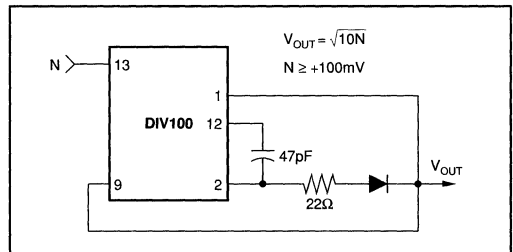
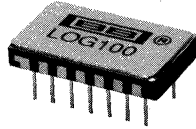


FIGURE 17. Connection Diagram for Square Root Mode.

For Immediate Assistance, Contact Your Local Salesperson



LOG100

Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- **ACCURACY**
0.37% FSO max Total Error
Over 5 Decades
- **LINEARITY**
0.1% max Log Conformity
Over 5 Decades
- **EASY TO USE**
Pin-selectable Gains
Internal Laser-trimmed Resistors
- **WIDE INPUT DYNAMIC RANGE**
6 Decades, 1nA to 1mA
- **HERMETIC CERAMIC DIP**

APPLICATIONS

- **LOG, LOG RATIO AND ANTILOG COMPUTATIONS**
- **ABSORBANCE MEASUREMENTS**
- **DATA COMPRESSION**
- **OPTICAL DENSITY MEASUREMENTS**
- **DATA LINEARIZATION**
- **CURRENT AND VOLTAGE INPUTS**

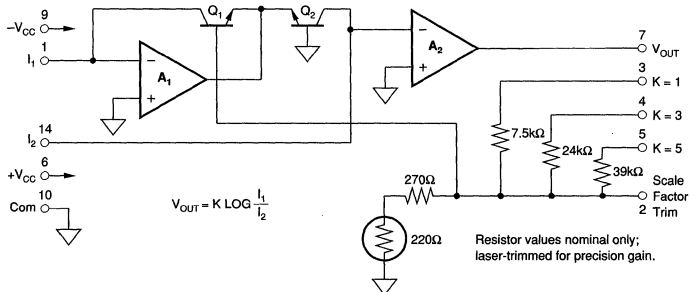
DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2 . Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film

resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-8491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$ and $\pm V_{CC} = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	CONDITIONS	LOG100JP			UNITS
		MIN	TYP	MAX	
TRANSFER FUNCTION Log Conformity Error ⁽¹⁾ Initial Over Temperature K Range ⁽²⁾ Accuracy Temperature Coefficient	Either I_1 or I_2 1nA to 100 μA (5 decades) 1nA to 1mA (6 decades) 1nA to 100 μA (5 decades) 1nA to 1mA (6 decades)	$V_{out} = K \text{ Log } (I_1/I_2)$			
			0.04 0.15 0.002 0.001 1, 3, 5 0.3 0.03	0.1 0.25	% % %/°C %/°C V/decade % %/°C
ACCURACY Total Error ⁽³⁾ Initial vs Temperature vs Supply	$K = 1$, ⁽⁴⁾ Current Input Operation $I_1, I_2 = 1\text{mA}$ $I_1, I_2 = 100\mu\text{A}$ $I_1, I_2 = 10\mu\text{A}$ $I_1, I_2 = 1\mu\text{A}$ $I_1, I_2 = 100\text{nA}$ $I_1, I_2 = 10\text{nA}$ $I_1, I_2 = 1\text{nA}$ $I_1, I_2 = 1\text{mA}$ $I_1, I_2 = 100\mu\text{A}$ $I_1, I_2 = 10\mu\text{A}$ $I_1, I_2 = 1\mu\text{A}$ $I_1, I_2 = 100\text{nA}$ $I_1, I_2 = 10\text{nA}$ $I_1, I_2 = 1\text{nA}$ $I_1, I_2 = 1\text{mA}$ $I_1, I_2 = 100\mu\text{A}$ $I_1, I_2 = 10\mu\text{A}$ $I_1, I_2 = 1\mu\text{A}$ $I_1, I_2 = 100\text{nA}$ $I_1, I_2 = 10\text{nA}$ $I_1, I_2 = 1\text{nA}$			± 55 ± 30 ± 25 ± 20 ± 25 ± 30 ± 37 ± 0.20 ± 0.37 ± 0.28 ± 0.033 ± 0.28 ± 0.51 ± 1.26 ± 4.3 ± 1.5 ± 0.37 ± 0.11 ± 0.61 ± 0.91 ± 2.6	mV mV mV mV mV mV mV mV/°C mV/°C mV/°C mV/°C mV/°C mV/°C mV/°C mV/V mV/V mV/V mV/V mV/V mV/V mV/V
INPUT CHARACTERISTICS (of Amplifiers A_1 and A_2) Offset Voltage Initial vs Temperature Bias Current Initial vs Temperature Voltage Noise Current Noise	10Hz to 10kHz, RTI 10Hz to 10kHz, RTI		± 0.7 ± 80 1 3 0.5	± 5 5 ⁽⁵⁾	mV $\mu\text{V}/^\circ\text{C}$ pA μVrms pArms
AC PERFORMANCE 3dB Response ⁽⁶⁾ , $I_2 = 10\mu\text{A}$ 1nA 1 μA 10 μA 1mA Step Response ⁽⁶⁾ Increasing 1 μA to 1mA 100nA to 1 μA 10nA to 100nA Decreasing 1mA to 1 μA 1 μA to 100nA 100nA to 10nA	$C_C = 4500\text{pF}$ $C_C = 150\text{pF}$ $C_C = 150\text{pF}$ $C_C = 50\text{pF}$ $C_C = 150\text{pF}$ $C_C = 150\text{pF}$		0.11 38 27 45 11 7 110 45 20 550		kHz kHz kHz kHz μs μs μs μs μs μs μs
OUTPUT CHARACTERISTICS Full Scale Output (FSO) Rated Output Voltage Current Current Limit Positive Negative Impedance	$I_{OUT} = \pm 5\text{mA}$ $V_{OUT} = \pm 10\text{V}$	± 10 ± 10 ± 5			V V mA mA mA mA Ω

LOG100

7

SPECIAL FUNCTIONS



For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS (CONT)

ELECTRICAL

$T_A = +25^\circ\text{C}$ and $\pm V_{CC} = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	CONDITIONS	LOG100JP			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Rated Voltage	Derated Performance		± 15		VDC
Operating Range		± 12		± 18	VDC
Quiescent Current			± 7	± 9	mA
AMBIENT TEMPERATURE RANGE					
Specification	Derated Performance	0		+70	$^\circ\text{C}$
Operating Range		-25		+85	$^\circ\text{C}$
Storage		-40		+85	$^\circ\text{C}$

NOTES: (1) Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs $\log I_{IN}$ curve expressed as a percent of peak-to-peak full scale output. (2) May be trimmed to other values. See Applications section. (3) The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately. (4) Total Error at other values of K is K times Total Error for K = 1. (5) Guaranteed by design. Not directly measurable due to amplifier's committed configuration. (6) 3dB and transient response are a function of both the compensation capacitor and the level of input current. See Typical Performance Curves.

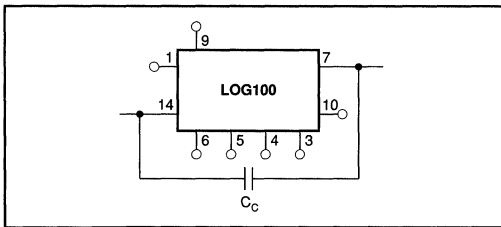
ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{V}$
Internal Power Dissipation	600mW
Input Current	10mA
Input Voltage Range	$\pm 18\text{V}$
Storage Temperature Range	-40°C to $+85^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/DECADE	CONNECTIONS
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

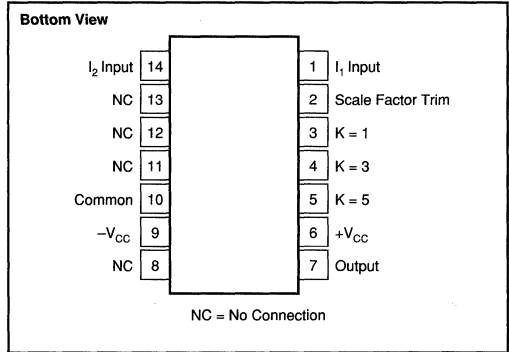
FREQUENCY COMPENSATION



ORDERING INFORMATION

MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
LOG100JP	14-Pin Hermetic Ceramic DIP	0°C to $+70^\circ\text{C}$

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integral circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION⁽¹⁾

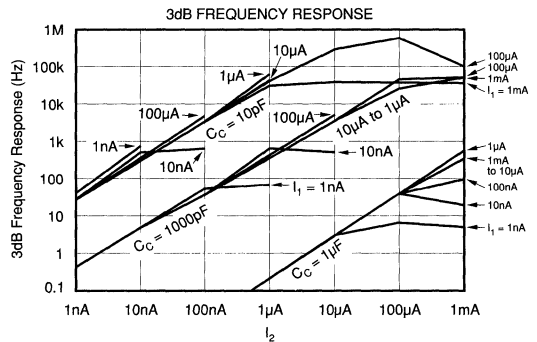
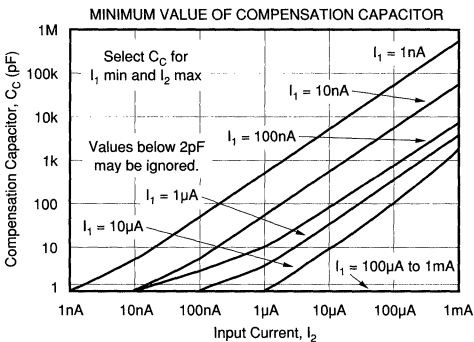
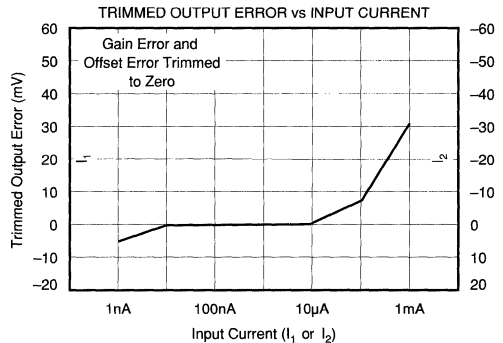
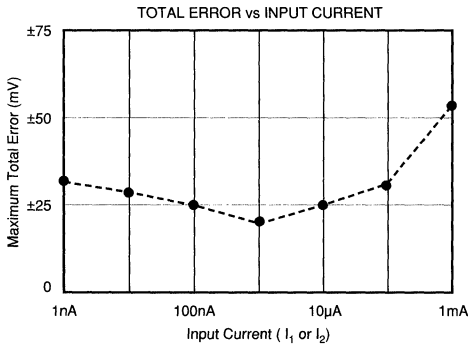
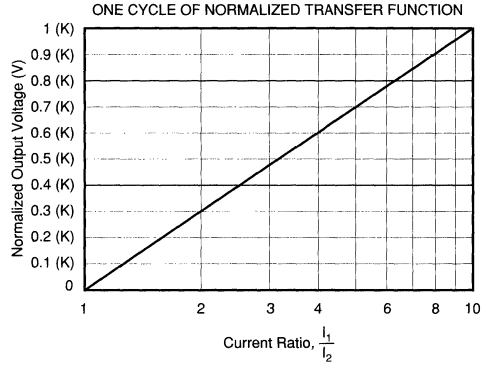
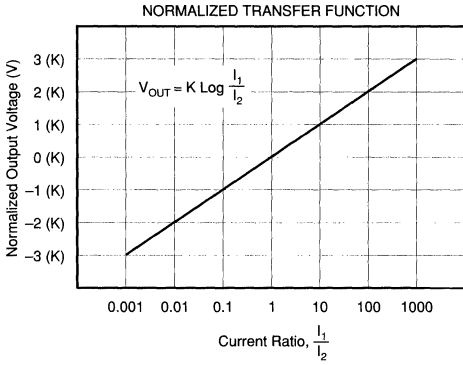
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
LOG100JP	14-Pin Hermetic Ceramic DIP	148 ⁽²⁾

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) During 1994, the package was changed from plastic to hermetic ceramic. Pinout, model number, and specifications remained unchanged.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$, unless otherwise noted.



THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ln \frac{I_C}{I_S} \quad \text{where: } V_T = \frac{KT}{q} \quad (1)$$

K = Boltzman's constant = 1.381×10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602×10^{-19} Coulombs

I_C = Collector current

I_S = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE1} - V_{BE2} \quad (2)$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T1} \ln \frac{I_1}{I_{S1}} - V_{T2} \ln \frac{I_2}{I_{S2}} \quad (3)$$

If the transistors are matched and isothermal and $V_{T1} = V_{T2}$, then (3) becomes:

$$V_{OUT}' = V_T \left[\ln \frac{I_1}{I_S} - \ln \frac{I_2}{I_S} \right] \quad (4)$$

$$V_{OUT}' = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \quad (5)$$

$$\ln x = 2.3 \log_{10} x \quad (6)$$

$$V_{OUT}' = n V_T \log \frac{I_1}{I_2} \quad (7)$$

where $n = 2.3$

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \quad (8)$$

$$= \frac{R_1 + R_2}{R_1} n V_T \log \frac{I_1}{I_2} \quad (9)$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \quad (10)$$

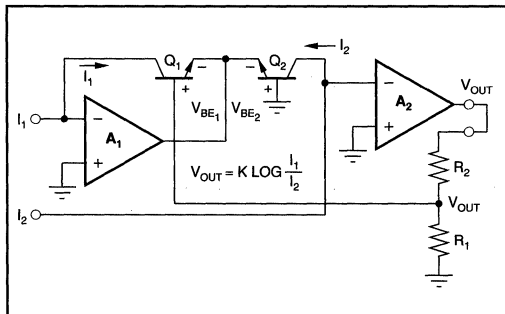


FIGURE 1. Simplified Model of Log Amplifier.

It should be noted that the temperature dependence associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$ where:

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

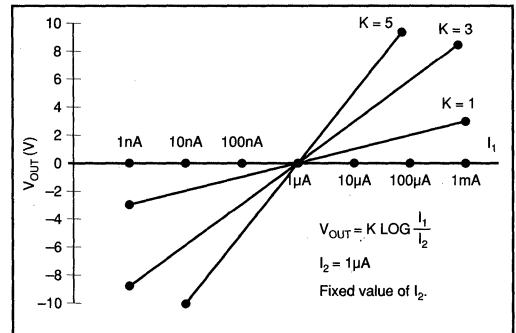


FIGURE 2. Transfer Function with Varying K and I_1 .

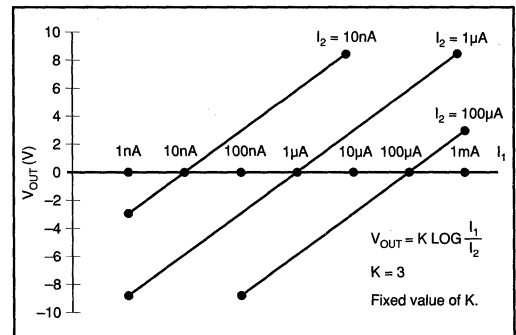


FIGURE 3. Transfer Function with Varying I_2 and I_1 .

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log(I_1/I_2)$. Thus,

$$V_{OUT(ACTUAL)} = V_{OUT(IDEAL)} \pm \text{Total Error.}$$

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example

I_1 varies over a range of 10nA to 1μA and I_2 varies from 100nA to 10μA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2 .

		I_1 (maximum error) ⁽¹⁾		
		10nA (30mV)	100nA (25mV)	1μA (20mV)
I_2 (maximum error) ⁽¹⁾	100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
	1μA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
	10μA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

NOTE: (1) Maximum errors are in parenthesis.

TABLE I. I_1/I_2 and Maximum Errors.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to -9V. The maximum total error occurs when $I_1 = 10$ nA and is equal to $K \times 30$ mV. This represents a 0.75% of peak-to-peak FSO error $3 \times 0.030/12 \times 100\% = 0.75\%$ where the full scale output is 12V (from +3V to -9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect, log amps have a unique property:

Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications, log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.



Log conformity is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus $\log(I_1/I_2)$ curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT(NONLIN)} = K \cdot 2Nm \cdot V \quad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \cdot \text{Log} \frac{I_1}{I_2} \quad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B1}}{I_2 - I_{B2}} \pm K \cdot 2Nm \pm V_{OS OUT} \quad (14)$$

The individual component of error is

- ΔK = scale factor error (0.3%, typ)
- I_{B1} = bias current of A_1 (1pA, typ)
- I_{B2} = bias current of A_2 (1pA, typ)
- N = log conformity error (0.05%, 0.1%, typ)
- $V_{OS OUT}$ = output offset voltage (1mV, typ)
- m = number of decades over which N is specified:
0.05% for m = 5, 0.1% for m = 6

Example: what is the error with $K = 3$ when

$$I_1 = 1\mu\text{A} \text{ and } I_2 = 100\text{nA}$$

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)5 \pm 1\text{mV} \quad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \quad (16)$$

$$= 3.009(1) + 0.015 + 0.001 \quad (17)$$

$$= 3.025\text{V} \quad (18)$$

Since the ideal output is 3.000V, the error as a percent of reading is

$$\% \text{ error} = \frac{0.025}{3} \times 100\% = 0.83\% \quad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B1} \pm \frac{E_{OS1}}{R_1}}{\frac{V_2}{R_2} - I_{B2} \pm \frac{E_{OS2}}{R_2}} \pm K \cdot 2Nm \pm V_{OS OUT} \quad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Typical Performance Curves for details.

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The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Typical Performance Curves. For any given application, the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1 . Larger values of C_c will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}} \quad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4), or it may be derived from a voltage source with one or more resistors.

When a single resistor is used, the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10nA} = 1500M\Omega.$$

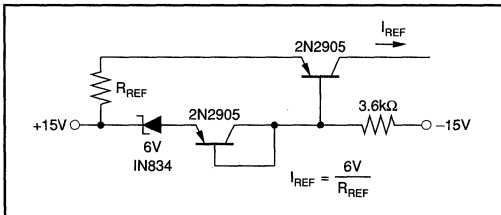


FIGURE 4. Temperature-Compensated Current Reference.

A voltage divider may be used to reduce the value of the resistor. When this is done, one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_1 , which ranges from zero to $\pm 5mV$. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

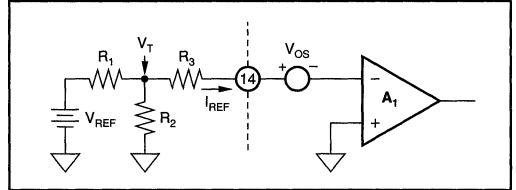


FIGURE 5. "T" Network for Reference Current.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired, the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2 . Since the amplifiers have FET inputs with the characteristic bias current doubling every $10^\circ C$, this nulling technique is practical only where the temperature is fairly stable.

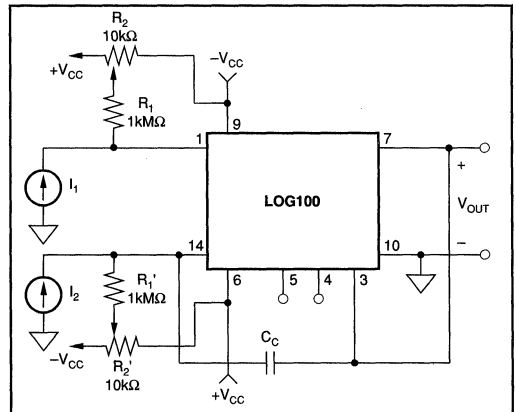


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100 μA . R_1 is then adjusted for zero output voltage.

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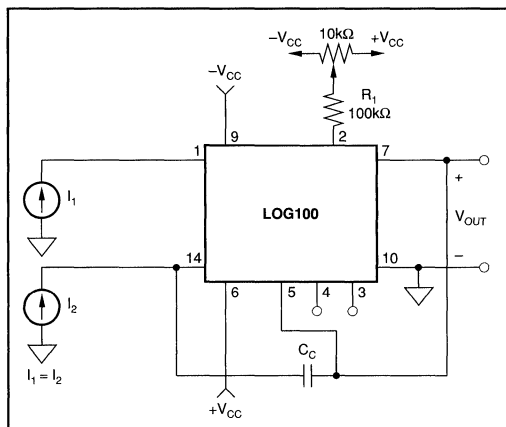


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the +V_{CC} and -V_{CC} pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling

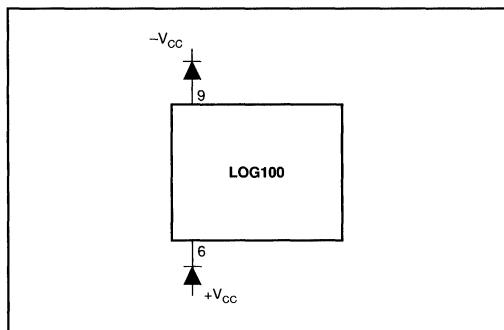


FIGURE 8. Reverse Polarity Protection.

techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

$$\text{Absorbance of the sample is } A = \log \frac{\lambda_1'}{\lambda_1} \quad (22)$$

$$\text{If } \lambda_2 = \lambda_1 \text{ and } D_1 \text{ and } D_2 \text{ are matched } A \propto K \log \frac{I_1}{I_2} \quad (23)$$

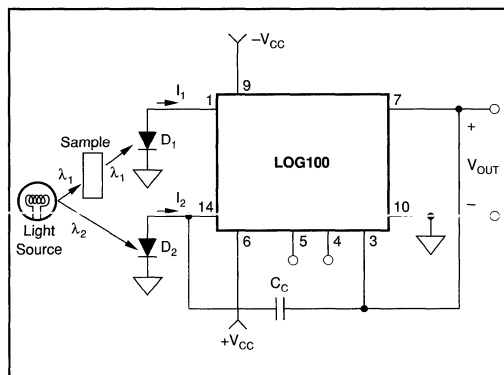


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can produce equivalent 20-bit converter operation.

SELECTING OPTIMUM VALUES OF I₂ AND K

In straight log applications (as opposed to log ratio), both K and I₂ are selected by the designer. In order to minimize errors due to output offset and noise, it is normally best to

LOG100
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scale the log amp to use as much of the $\pm 10V$ output range as possible. Thus, with the range of I_1 from $I_{1\text{ MIN}}$ to $I_{1\text{ MAX}}$:

$$\text{For } I_{1\text{ MAX}} \quad +10V = K \log I_{1\text{ MAX}}/I_2 \quad (24)$$

$$\text{For } I_{1\text{ MIN}} \quad -10V = K \log I_{1\text{ MIN}}/I_2 \quad (25)$$

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\text{ OPT}}$, is the geometric mean of $I_{1\text{ MAX}}$ and $I_{1\text{ MIN}}$.

$$I_{2\text{ OPT}} = \sqrt{I_{1\text{ MAX}} \times I_{1\text{ MIN}}} \quad (26)$$

$$K_{\text{OPT}} = \frac{10}{\log \frac{I_{1\text{ MAX}}}{I_{2\text{ OPT}}}} \quad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT} .

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations, the circuit in Figure 10 may be used.⁽¹⁾

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

NOTE: (1) More detailed information may be found in "Property Designed Log Amplifiers Process Bipolar Input Signals" by Larry McDonald, EDN, 5 Oct. 80, pp 99-102.

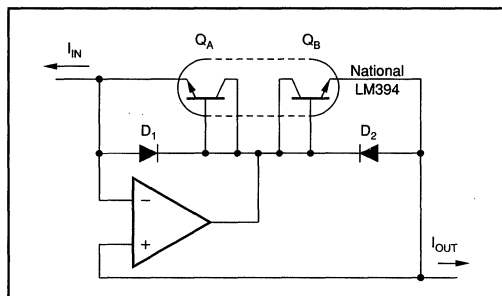


FIGURE 10. Current Inverter.

ANTILOG CONFIGURATION (an implicit technique)

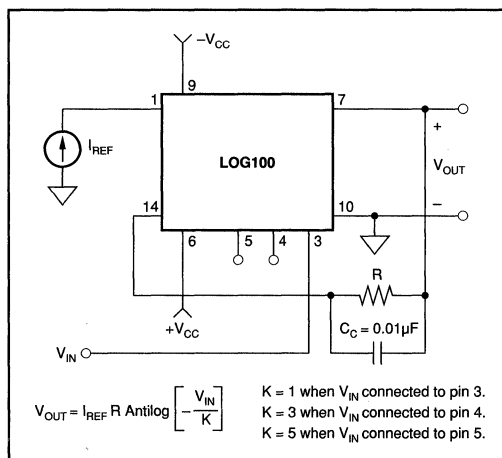
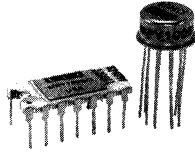


FIGURE 11. Connections for Antilog Function.

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MPY100

MULTIPLIER-DIVIDER

FEATURES

- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE: $90\mu\text{Vrms}$, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

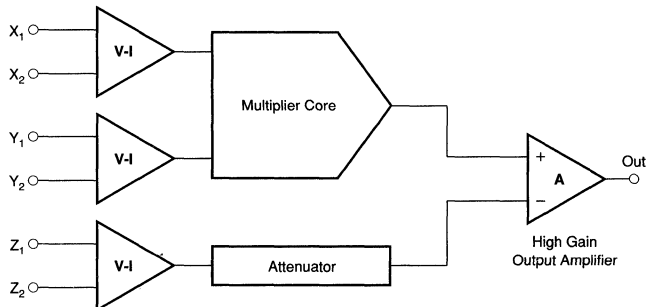
APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly

reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-412C

7.37

MPY100

7

SPECIAL FUNCTIONS

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.

PARAMETER	CONDITIONS	MPY100A			MPY100B/C			MPY100S			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE											
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$				*			*		
Total Error	$-10\text{V} \leq X, Y \leq 10\text{V}$			± 2.0			$\pm 1.0/0.5$			± 0.5	% FSR
Initial	$T_A = +25^\circ\text{C}$			± 0.017			$\pm 0.008/0.008$			± 0.025	% FSR/ $^\circ\text{C}$
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			± 0.05			*			± 0.05	% FSR/ $^\circ\text{C}$
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$								*		% FSR/%
vs Supply ⁽¹⁾											
Individual Errors											
Output Offset											
Initial	$T_A = +25^\circ\text{C}$			± 50			$\pm 10/7$			± 7	± 50
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			± 0.7			$\pm 0.7/0.3$			± 0.3	mV/ $^\circ\text{C}$
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$									± 0.3	mV/ $^\circ\text{C}$
vs Supply ⁽¹⁾				± 0.25			*			*	mV/%
Scale Factor Error											
Initial	$T_A = +25^\circ\text{C}$			± 0.12			*			*	% FSR
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			± 0.008			*			*	% FSR/ $^\circ\text{C}$
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$									± 0.008	% FSR/ $^\circ\text{C}$
vs Supply ⁽¹⁾				± 0.05			*			*	% FSR %
Nonlinearity											
X Input	$X = 20\text{Vp-p}; Y = \pm 10\text{VDC}$			± 0.08			*			*	% FSR
Y Input	$Y = 20\text{Vp-p}; X = \pm 10\text{VDC}$			± 0.08			*			*	% FSR
Feedthrough											
	$f = 50\text{Hz}$										
X Input	$X = 20\text{Vp-p}; Y = 0$			100			30/30			30	mVp-p
Y Input	$Y = 20\text{Vp-p}; X = 0$			6			*			*	mVp-p/ $^\circ\text{C}$
vs Temperature	$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			0.1			*			*	mVp-p/ $^\circ\text{C}$
vs Temperature	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$									0.1	mVp-p/%
vs Supply ⁽¹⁾				0.15			*			*	
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$	$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$				*			*		
Total Error (with external adjustments)	$X = 10\text{V}$ $-10\text{V} \leq Z \leq +10\text{V}$ $X = 1\text{V}$ $-1\text{V} \leq Z \leq +1\text{V}$ $+0.2\text{V} \leq X \leq +10\text{V}$ $-10\text{V} \leq Z \leq +10\text{V}$			± 1.5			$\pm 0.75/0.35$			± 0.35	% FSR
				± 4.0			$\pm 2.0/1.0$			± 1.0	% FSR
				± 5.0			$\pm 2.5/1.0$			± 1.0	% FSR
SQUARER PERFORMANCE											
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$				*			*		
Total Error	$-10\text{V} \leq X \leq +10\text{V}$			± 1.2			$\pm 0.6/0.3$			± 0.3	% FSR
SQUARE ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$	$+\sqrt{10(Z_2 - Z_1)} + X_2$				*			*		
Total Error	$1\text{V} \leq Z \leq 10\text{V}$			± 2			$\pm 1/0.5$			± 0.5	% FSR
AC PERFORMANCE											
Small-Signal Bandwidth				550			*			*	kHz
% Amplitude Error	Small-Signal			70			*			*	kHz
% (0.57 ^o) Vector Error	Small-Signal			5			*			*	kHz
Full Power Bandwidth	$ V_O = 10\text{V}, R_L = 2\text{k}\Omega$			320			*			*	kHz
Slew Rate	$ V_O = 10\text{V}, R_L = 2\text{k}\Omega$			20			*			*	V/ μs
Settling Time	$\epsilon = \pm 1\%, \Delta V_O = 20\text{V}$			2			*			*	μs
Overload Recovery	50% Output Overload			0.2			*			*	μs
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		± 10			*			*		*	V
Absolute Maximum				$\pm V_{CC}$			*			*	V
Input Resistance	$X, Y, Z^{(2)}$			10			*			*	M Ω
Input Bias Current	X, Y, Z			1.4			*			*	μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	$I_O = \pm 5\text{mA}$	± 10			*			*		*	V
Current	$V_O = \pm 10\text{V}$	± 5			*			*		*	mA
Output Resistance	$f = \text{DC}$		1.5				*			*	Ω

Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.

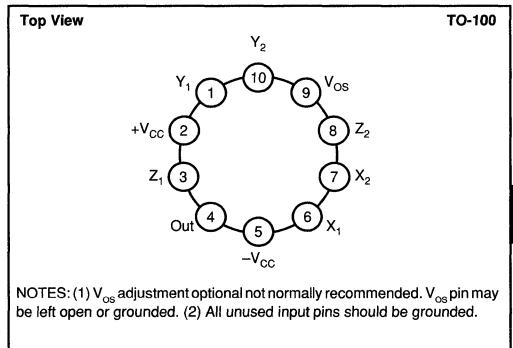
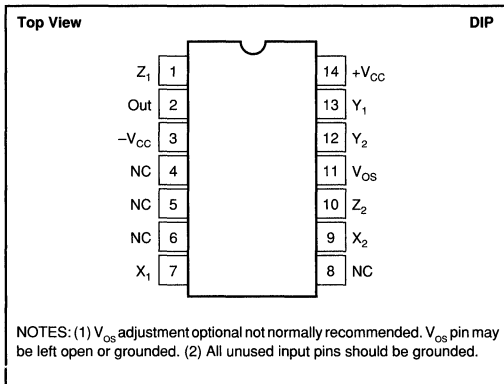
PARAMETER	CONDITIONS	MPY100A			MPY100B/C			MPY100S			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT NOISE VOLTAGE $X = Y = 0$ $f_o = 1\text{Hz}$ $f_o = 1\text{kHz}$ 1/f Corner Frequency $f_B = 5\text{Hz to } 10\text{kHz}$ $f_B = 5\text{Hz to } 5\text{MHz}$			6.2			*/			*		$\mu\text{V}/\sqrt{\text{Hz}}$
			0.6			*/			*		$\mu\text{V}/\sqrt{\text{Hz}}$
			110			*/			*		Hz
			60			*/			*		μVrms
			1.3			*/			*		mVrms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			± 15			*/			*		VDC
Operating Range	Derated Performance	± 8.5		± 20	*/		*/	*	*		VDC
Quiescent Current			± 5.5			*/			*		mA
TEMPERATURE RANGE (Ambient)											
Specification		-25		+85	*/		*/	-55		+125	$^\circ\text{C}$
Operating Range	Derated Performance	-55		+125	*/		*/	*		*	$^\circ\text{C}$
Storage		-65		+150	*/		*/	*		*	$^\circ\text{C}$

* Same as MPY100A specification.

*/ B/C grades same as MPY100A specification.

NOTES: (1) Includes effects of recommended null pots. (2) Z_2 input resistance is 10M Ω , typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25k Ω .

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 20\text{VDC}$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage ⁽²⁾	$\pm 40\text{VDC}$
Input Voltage Range ⁽²⁾	$\pm 20\text{VDC}$
Storage Temperature Range	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Operating Temperature Range	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$
Output Short-circuit Duration ⁽³⁾	Continuous
Junction Temperature	+150 $^\circ\text{C}$

NOTES: (1) Package must be derated on $\theta_{JC} = 15^\circ\text{C/W}$ and $\theta_{JA} = 165^\circ\text{C/W}$ for the metal package and $\theta_{JC} = 35^\circ\text{C/W}$ and $\theta_{JA} = 220^\circ\text{C/W}$ for the ceramic package. (2) For supply voltages less than $\pm 20\text{VDC}$, the absolute maximum input voltage is equal to the supply voltage. (3) Short-circuit may be to ground only. Rating applies to +85 $^\circ\text{C}$ ambient for the metal package and +65 $^\circ\text{C}$ for the ceramic package.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPY100AG	14-Pin Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100AM	Metal TO-100	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100BG	14-Pin Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100BM	Metal TO-100	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100CG	14-Pin Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100CM	Metal TO-100	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100SG	14-Pin Ceramic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
MPY100SM	Metal TO-100	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$

PACKAGE INFORMATION⁽¹⁾

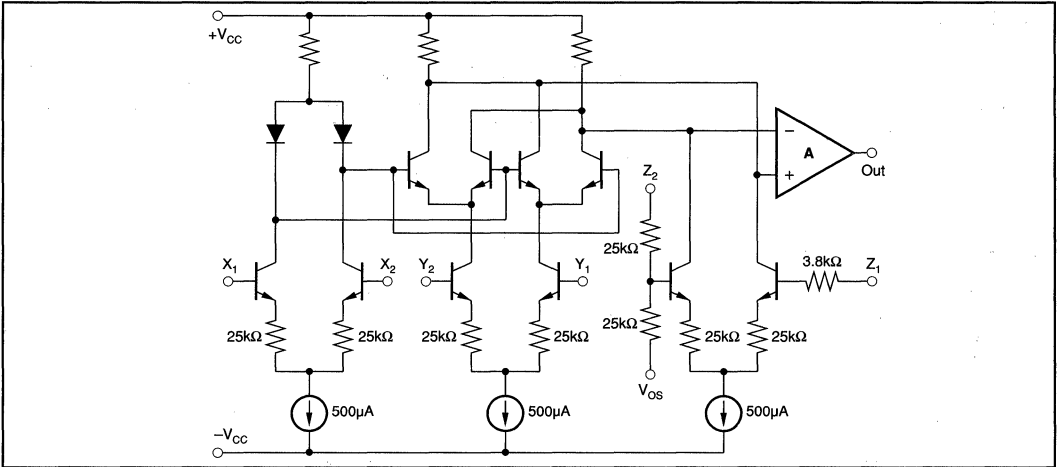
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPY100AG	14-Pin Ceramic DIP	169
MPY100AM	Metal TO-100	007
MPY100BG	14-Pin Ceramic DIP	169
MPY100BM	Metal TO-100	007
MPY100CG	14-Pin Ceramic DIP	169
MPY100CM	Metal TO-100	007
MPY100SG	14-Pin Ceramic DIP	169
MPY100SM	Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

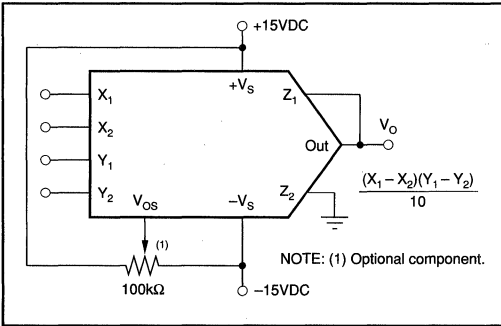


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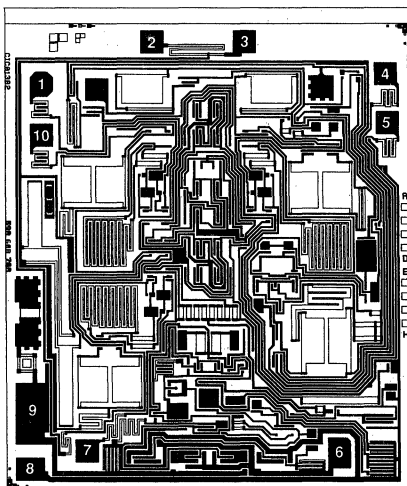
SIMPLIFIED SCHEMATIC



CONNECTION DIAGRAM



DICE INFORMATION



MPY100 DIE TOPOGRAPHY

PAD	FUNCTION
1	Y ₂
2	V _{OS}
3	Z ₂
4	X ₂
5	X ₁
6	V _O
7	Z ₁
8	+V
9	-V
10	Y ₁

Substrate Bias: -V_{cc}

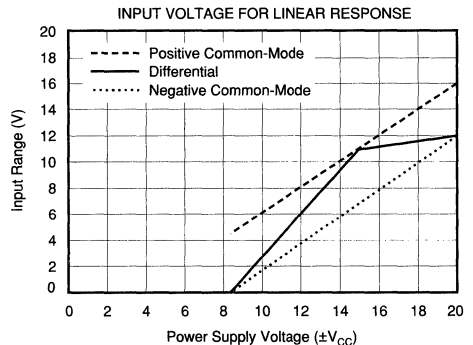
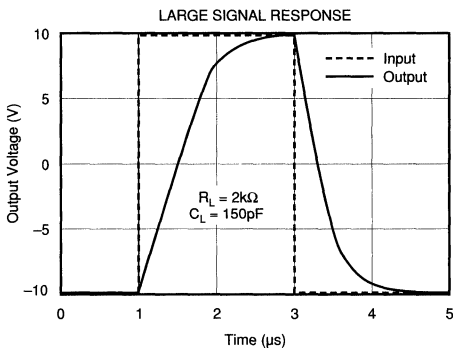
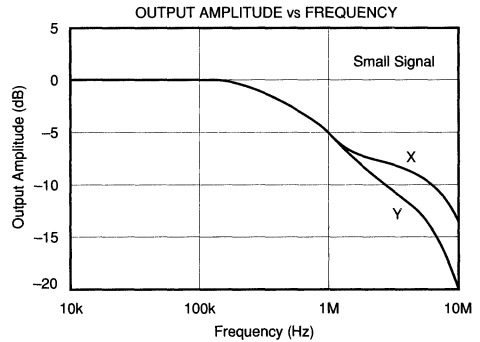
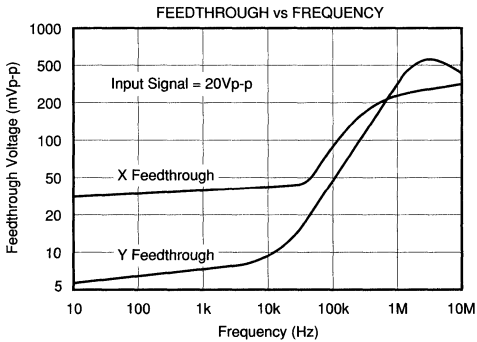
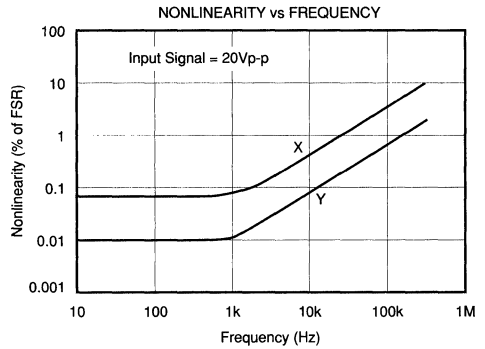
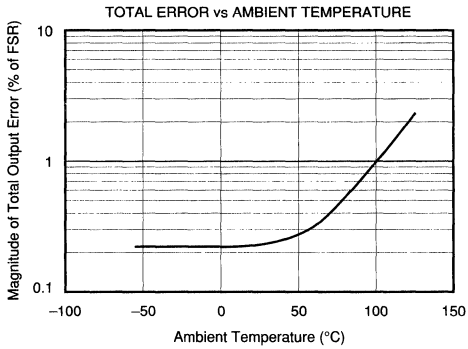
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	107 x 93 ±5	2.72 x 2.36 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

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TYPICAL PERFORMANCE CURVES

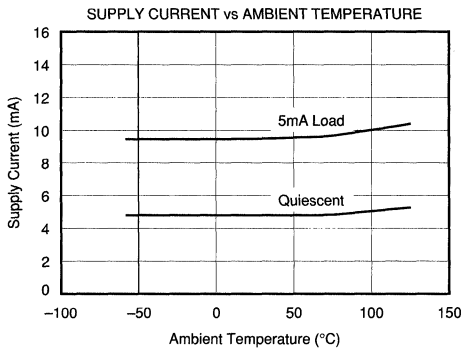
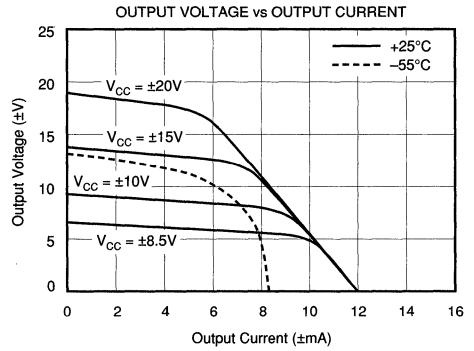
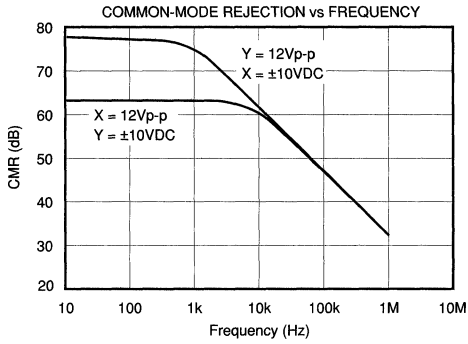
At $T_a = +25^\circ\text{C}$ and $\pm V_s = 15\text{VDC}$, unless otherwise specified.



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and $\pm V_S = 15\text{VDC}$, unless otherwise specified.



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THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

For small values of the input voltage, V_1 , that are much smaller than V_T , the transistor's thermal voltage, the differential output voltage, V_O , is:

$$V_O = g_m R_L V_1$$

The transconductance g_m of the stage is given by:

$$g_m = I_E / V_T$$

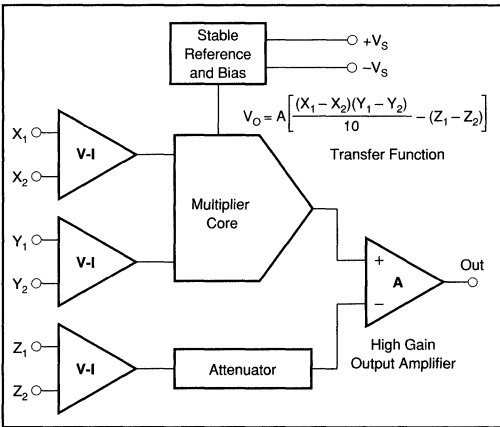


FIGURE 1. MPY100 Functional Block Diagram.

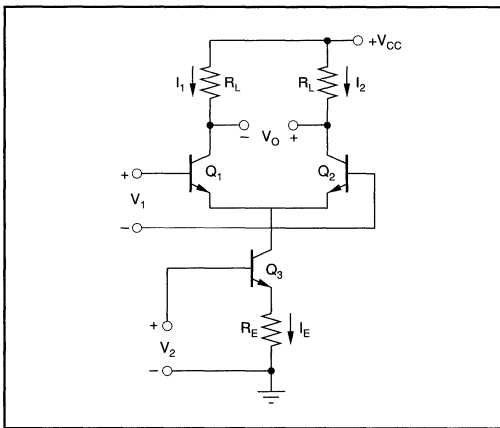


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

and is modulated by the voltage, V_2 , to give

$$g_m \approx V_2 / V_T R_E$$

Substituting this into the original equation yields the overall transfer function

$$V_O = g_m R_L V_1 = V_1 V_2 (R_L / V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2 .

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

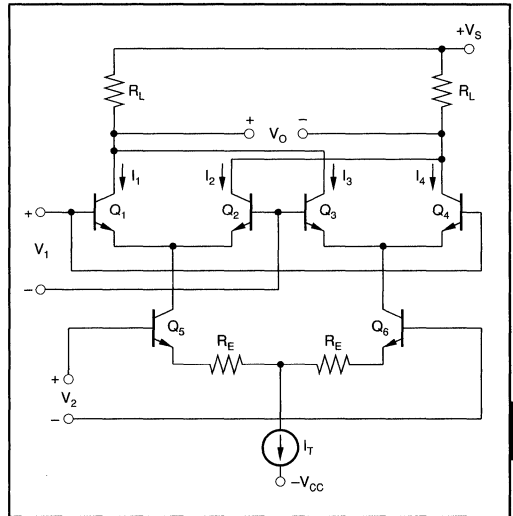


FIGURE 3. Cross-Coupled Differential Stages as a Variable-Transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_O = V_1 V_2 (R_L / V_T R_E)$$

For input voltages larger than V_T , the voltage-to-current transfer characteristics of the differential pair Q_1 , Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_T}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

The emitter degeneration resistors, R_X and R_Y , in Figure 4, provide a linear conversion of the input voltages to differential current, I_X and I_Y , where:

MPY100

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SPECIAL FUNCTIONS

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$$I_X = V_X/R_X \text{ and } I_Y = V_Y/R_Y$$

Analysis of Figure 4 shows the voltage V_A to be:

$$V_A = (2R_L/I_1)(I_X I_Y)$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y , V_A may also be written:

$$V_A = KV_X V_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to:

$$V_A = KV_X V_Y - V_Z$$

Therefore, the output of the MPY100 is:

$$V_O = A[KV_X V_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_O = A \left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2) \right]$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10 μ F tantalum capacitor in parallel with a 1000pF ceramic capacitor from the + V_{CC} and - V_{CC} pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100 Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are 0V.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

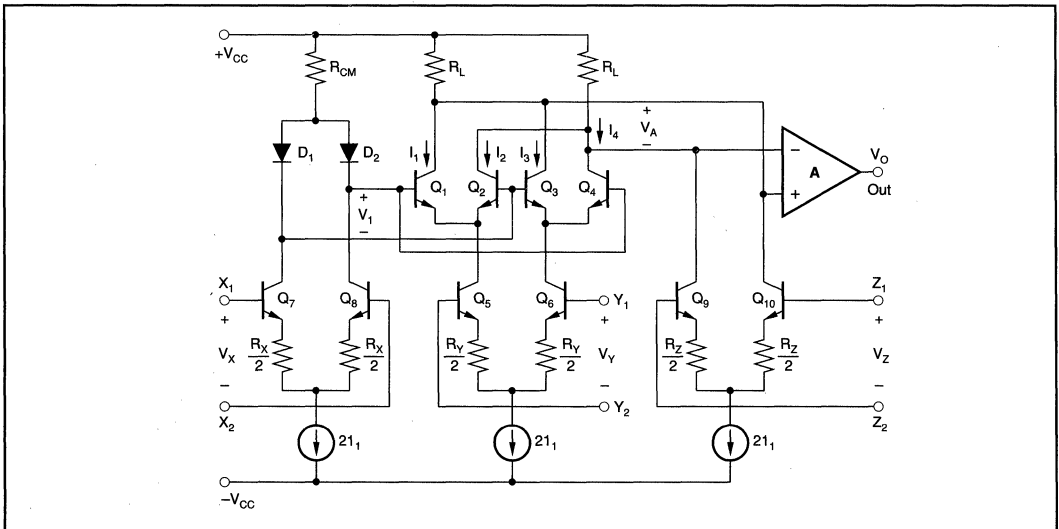


FIGURE 4. MPY100 Simplified Circuit Diagram.

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SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however be improved over a limited range by nulling the output offset voltage using the 100Ω optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z₂, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this terminal, as well as the X and Y inputs, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_x V_y = K(X_1 - X_2)(Y_1 - Y_2), \quad K = \left[\frac{1 + (R_1/R_2)}{10} \right]$$

$0.1 \leq K \leq 1$

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10, which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100, this operational amplifier is the output amplifier shown in Figure 1.

The divider error with a multiplier-inverted analog divider is approximately:

$$\epsilon_{DIVIDER} = 10 \epsilon_{MULTIPLIER} / (X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of X₁ - X₂. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be

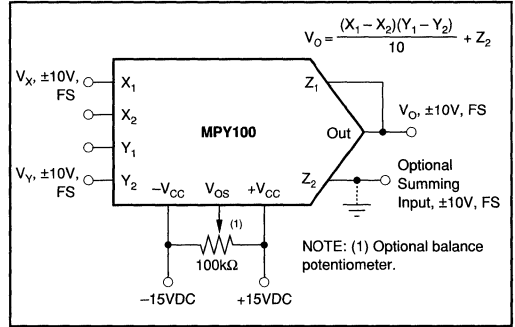


FIGURE 5. Multiplier Connection.

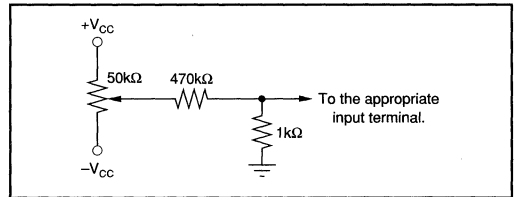


FIGURE 6. Optional Trimming Configuration.

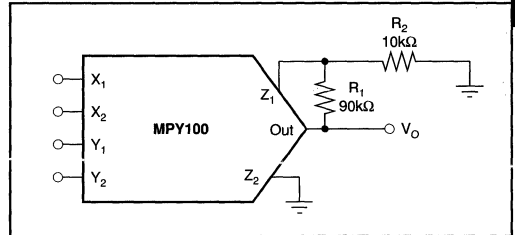


FIGURE 7. Connection for Unity Scale Factor.

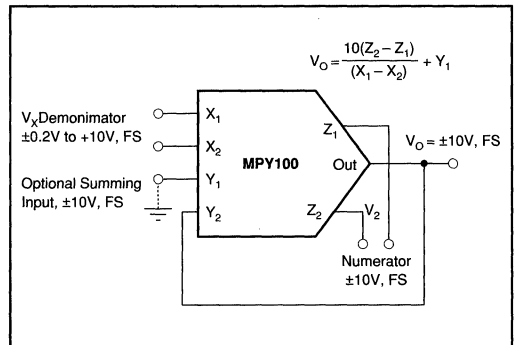


FIGURE 8. Divider Connection.

MPY100

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SPECIAL FUNCTIONS

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applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

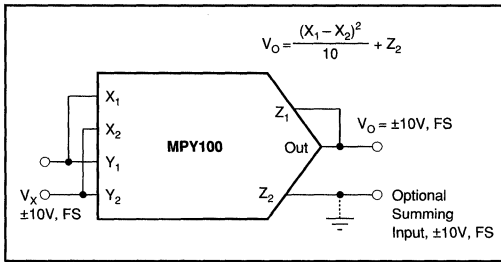


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z . The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

The load resistance, R_L , must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

PERCENTAGE COMPUTATION

The circuit of Figure 11 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1 .

BRIDGE LINEARIZATION

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_o independent of the bridge supply voltage. See Figure 12.

TRUE RMS-TO-DC CONVERSION

The rms-to-DC conversion circuit of Figure 13 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

SINE FUNCTION GENERATOR

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2) = 10 \sin(9V_1)$$

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown/McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

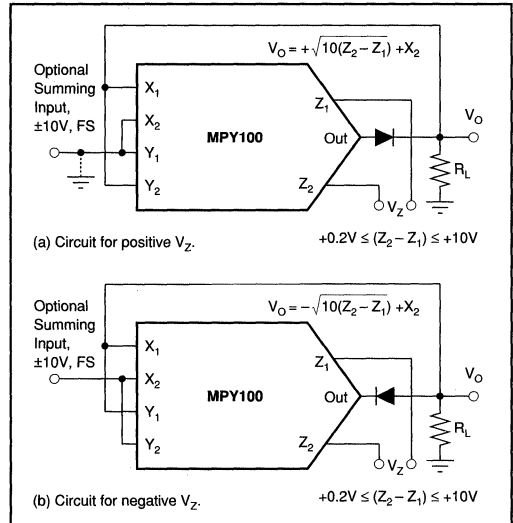


FIGURE 10. Square Root Connection.

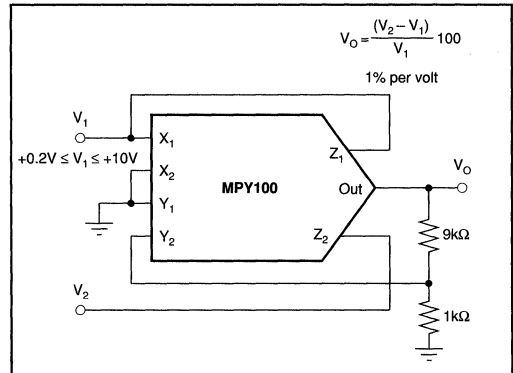


FIGURE 11. Percentage Computation.

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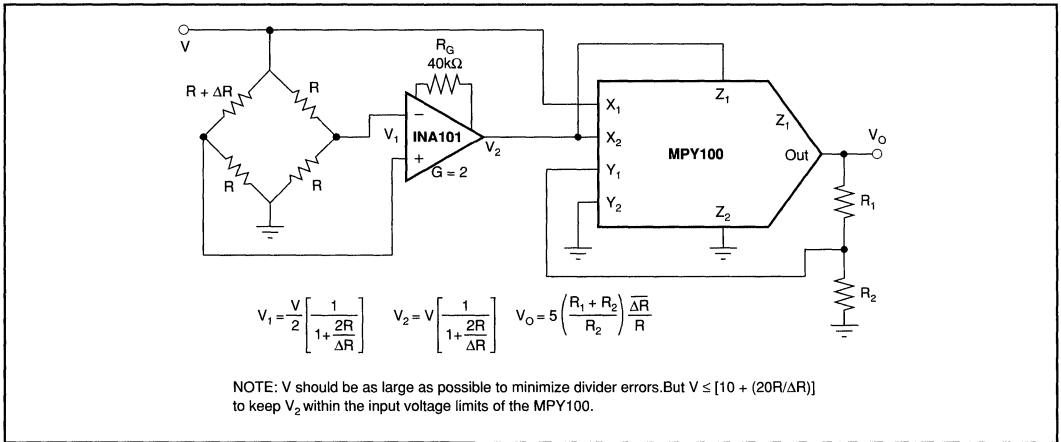


FIGURE 12. Bridge Linearization.

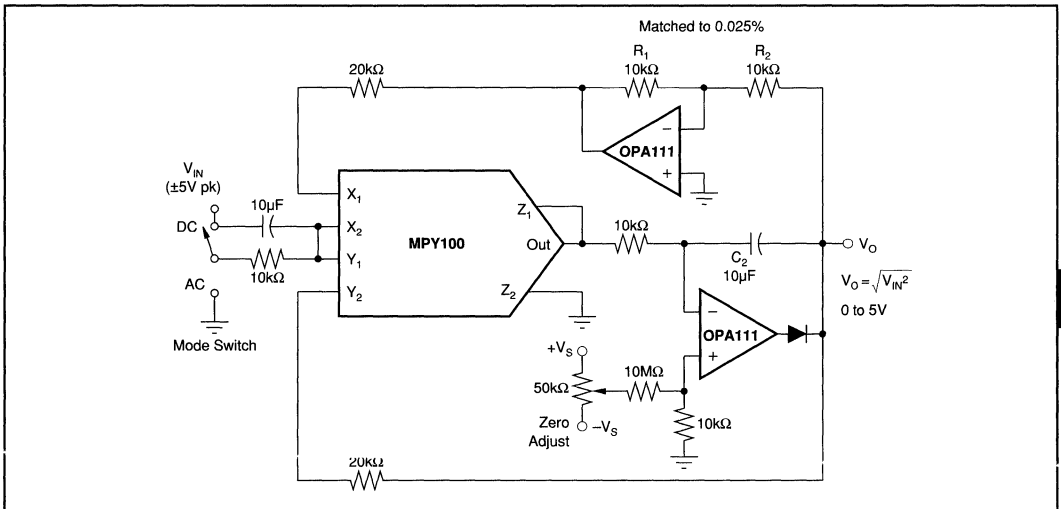


FIGURE 13. True RMS-to-DC Conversion.

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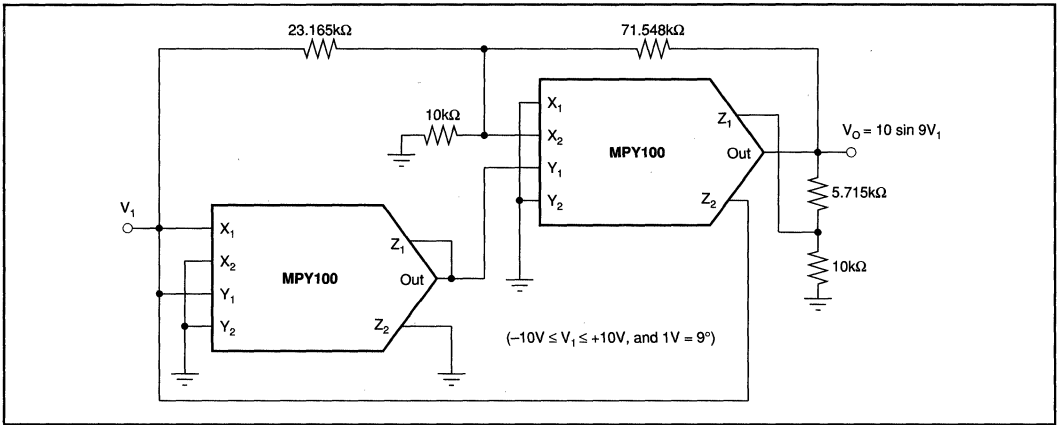


FIGURE 14. Sine Function Generator

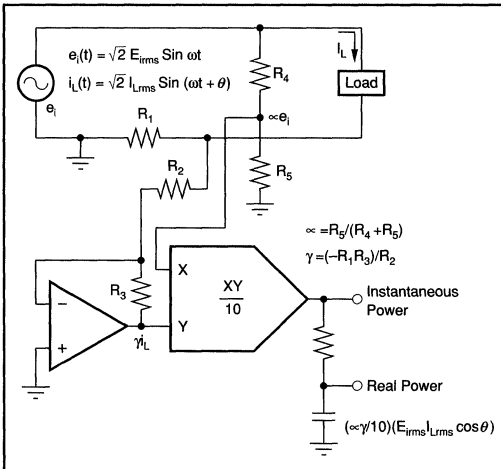
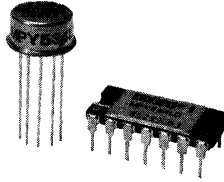


FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

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MPY534

Precision ANALOG MULTIPLIER

FEATURES

- $\pm 0.25\%$ max 4-QUADRANT ACCURACY
- WIDE BANDWIDTH: 1MHz min, 3MHz typ
- ADJUSTABLE SCALE FACTOR
- STABLE AND RELIABLE MONOLITHIC CONSTRUCTION
- LOW COST

APPLICATIONS

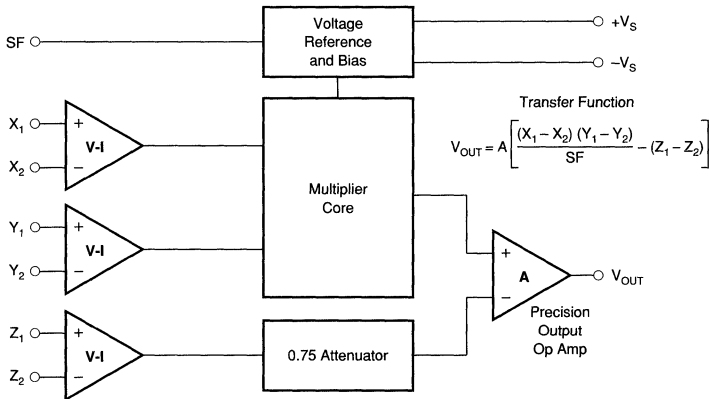
- PRECISION ANALOG SIGNAL PROCESSING
- VIDEO SIGNAL PROCESSING
- VOLTAGE CONTROLLED FILTERS AND OSCILLATORS
- MODULATION AND DEMODULATION
- RATIO AND PERCENTAGE COMPUTATION

DESCRIPTION

The MPY534 is a high accuracy, general purpose four-quadrant analog multiplier. Its accurately laser trimmed transfer characteristics make it easy to use in a wide variety of applications with a minimum of external parts and trimming circuitry. Its differential X, Y and Z inputs allow configuration as multiplier, squarer, divider, square-rooter and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows accurate signal processing at higher frequencies suitable for video signal processing. It is capable of performing IF and RF frequency mixing, modulation and demodulation with excellent carrier rejection and very simple feedthrough adjustment.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user selected scale factors from 0.1 to 10 using external feedback resistors.



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 Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_S = ±15VDC, unless otherwise specified.

PARAMETER	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE																
Transfer Function	*			$(X_1 - X_2)(Y_1 - Y_2) + Z_2$						*				*		
Total Error ⁽¹⁾ (-10V ≤ X, Y ≤ +10V)			±1.0			±0.5			±0.25			±1.0			*	%
T _A = min to max	±1.5			±1.0			±0.5			±2.0			±1.0		*	%
Total Error vs Temperature	±0.022			±0.015			±0.008			±0.02			±0.01		*	%/°C
Scale Factor Error (SF = 10.000V Nominal) ⁽²⁾	±0.25			±0.1			*			±0.25			*			%
Temperature Coefficient of Scaling Voltage	±0.02			±0.01			±0.005			±0.02			±0.005			%/°C
Supply Rejection (±15V ±1V)	*			±0.01			*			*			*			%
Nonlinearity:																
X (X = 20Vp-p, Y = 10V)	±0.4			±0.2	±0.3		±0.10	±0.12		±0.4			*	*	*	%
Y (Y = 20Vp-p, X = 10V)	*			±0.01	±0.1		±0.005	*		*			*	*	*	%
Feedthrough ⁽³⁾																
X (Y Nulled, Y = 20Vp-p 50Hz)	±0.3			±0.15	±0.3		±0.05	±0.12		±0.3			*	*	*	%
Y (X Nulled, Y = 20Vp-p 50Hz)	*			±0.01	±0.1		±0.003	*		*			*	*	*	%
Output Offset Voltage	±5		±30	±2	±15		*	±10		*		±30	*	*	*	mV
Output Offset Voltage Drift	200			100			*			*		500	*	*	*	μV/°C
DYNAMICS																
Small Signal BW, (V _{OUT} = 0.1Vrms)	*	*		1	3		*	*		*	*		*	*		MHz
1% Amplitude Error (C _{LOAD} = 1000pF)	*	*			50		*	*		*	*		*	*		kHz
Slew Rate (V _{OUT} = 20Vp-p)	*	*			20		*	*		*	*		*	*		V/μs
Settling Time (to 1%, ΔV _{OUT} = 20V)	*	*			2		*	*		*	*		*	*		μs
NOISE																
Noise Spectral Density: SF = 10V					0.8		*	*		*	*		*	*		μV/√Hz
Wideband Noise: f = 10Hz to 5MHz	*	*			1		*	*		*	*		*	*		mVrms
f = 10Hz to 10kHz	*	*			90		*	*		*	*		*	*		μVrms
OUTPUT																
Output Voltage Swing	*	*		±11			*	*		*	*		*	*		V
Output Impedance (f ≤ 1kHz)					0.1		*	*		*	*		*	*		Ω
Output Short Circuit Current (R _L = 0, T _A = min to max)	*	*			30		*	*		*	*		*	*		mA
Amplifier Open Loop Gain (f = 50Hz)	*	*			70		*	*		*	*		*	*		dB
INPUT AMPLIFIERS (X, Y and Z)																
Input Voltage Range																
Differential V _{IN} (V _{CM} = 0)	*				±12		*	*		*	*		*	*		V
Common-Mode V _{IN} (V _{DIFF} = 0) (see Typical Performance Curves)	*				±10		*	*		*	*		*	*		V
Offset Voltage X, Y	±5	±20		±2	±10		*	*		±5	±20		*	*		mV
Offset Voltage Drift X, Y	100			50			*	*		100			*	*		μV/°C
Offset Voltage Z	±5	±30		±2	±15		*	±10		±5	±30		*	*		mV
Offset Voltage Drift Z	200			100			*	*		500			*	*		μV/°C
CMRR	60	80		70	90		*	*		60	80		*	*		dB
Bias Current	*	*		0.8	2.0		*	*		*	*		*	*		μA
Offset Current	*	*		0.1			0.05	0.2		*	2.0		*	2.0		μA
Differential Resistance	*	*		10			*			*			*			MΩ
DIVIDER PERFORMANCE																
Transfer Function (X ₁ > X ₂)	*			$10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$												
Total Error ⁽¹⁾ (X = 10V, -10V ≤ Z ≤ +10V)	±0.75			±0.35			±0.2			±0.75			*			%
(X = -1V, -1V ≤ Z ≤ +1V)	±2.0			±1.0			±0.8			±2.0			*			%
(0.1V ≤ X ≤ 10V, -10V ≤ Z ≤ 10V)	±2.5			±1.0			±0.8			±2.5			*			%

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SPECIFICATIONS (CONT)

ELECTRICAL

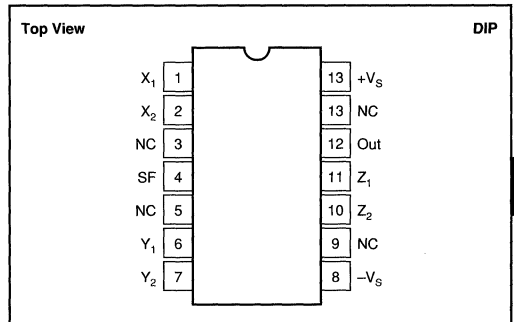
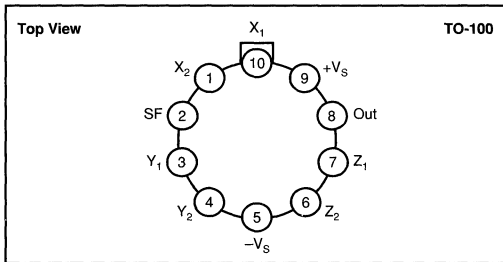
$T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{VDC}$, unless otherwise specified.

PARAMETER	MPY534J			MPY534K			MPY534L			MPY534S			MPY534T			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE PERFORMANCE		*						*			*			*		
Transfer Function				$\frac{(X_1 - X_2)^2}{10V} + Z_2$												
Total Error ($-10V \leq X \leq 10V$)		0.6		± 0.3				± 0.2		± 0.6				*		%
SQUARE-ROOTER PERFORMANCE		*						*			*			*		
Transfer Function ($Z_1 \leq Z_2$)				$\sqrt{10V(Z_2 - Z_1)} + X_2$												
Total Error ⁽¹⁾ ($1V \leq Z \leq 10V$)		± 1.0		± 0.5				± 0.25		± 1.0				± 0.5		%
POWER SUPPLY		*	*					*	*		*	*		*	*	
Supply Voltage:																
Rated Performance Operating	*	*	*	± 8	± 15	± 18	*	*	*	*	± 20	*	*	*	± 20	VDC
Supply Current, Quiescent	*	*	*	4	6	6	*	*	*	*	*	*	*	*	*	VDC mA
TEMPERATURE RANGE		*	*					*	*		*	*		*	*	
Operating	*	*	*	0	$+70$	$+150$	*	*	*	-55	$+125$	-55	$+125$	-55	$+125$	$^\circ\text{C}$
Storage	*	*	*	-65	$+70$	$+150$	*	*	*	-55	$+125$	-55	$+125$	-55	$+125$	$^\circ\text{C}$

*Specifications same as for MPY534K.

NOTES: (1) Figures given are percent of full scale, $\pm 10V$ (i.e., $0.01\% = 1\text{mV}$). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY534J, K, L	MPY534S, T
Power Supply Voltage	± 18	± 20
Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*
Operating Temperature Range	0°C to $+70^\circ\text{C}$	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$	*
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$	*

*Specification same as for MPY534K.

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPY534JD	Ceramic DIP	169
MPY534JH	Metal TO-100	007
MPY534KD	Ceramic DIP	169
MPY534KH	Metal TO-100	007
MPY534LD	Ceramic DIP	169
MPY534LH	Metal TO-100	007
MPY534SD	Ceramic DIP	169
MPY534SH	Metal TO-100	007
MPY534TD	Ceramic DIP	169
MPY534TH	Metal TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

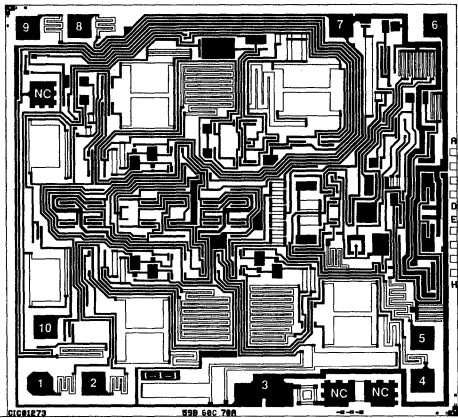


ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
MPY534JD	Ceramic DIP	0°C to $+70^\circ\text{C}$
MPY534JH	Metal TO-100	0°C to $+70^\circ\text{C}$
MPY534KD	Ceramic DIP	0°C to $+70^\circ\text{C}$
MPY534KH	Metal TO-100	0°C to $+70^\circ\text{C}$
MPY534LD	Ceramic DIP	0°C to $+70^\circ\text{C}$
MPY534LH	Metal TO-100	0°C to $+70^\circ\text{C}$
MPY534SD	Ceramic DIP	-55°C to $+125^\circ\text{C}$
MPY534SH	Metal TO-100	-55°C to $+125^\circ\text{C}$
MPY534TD	Ceramic DIP	-55°C to $+125^\circ\text{C}$
MPY534TH	Metal TO-100	-55°C to $+125^\circ\text{C}$

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DICE INFORMATION



MPY534 DIE TOPOGRAPHY

PAD	FUNCTION
1	Y_1
2	Y_2
3	$-V_S$
4	Z_2
5	Z_1
6	Output
7	$+V_S$
8	X_1
9	X_2
10	SF (Scale Factor)

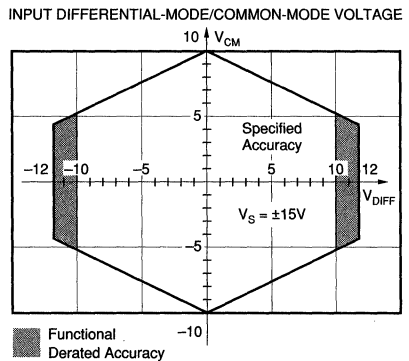
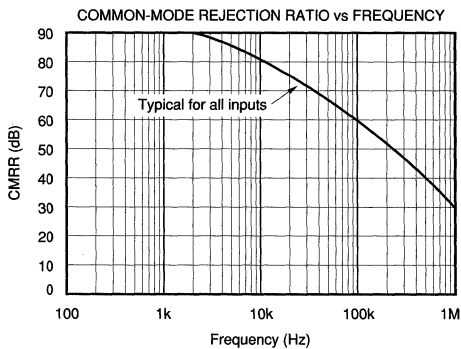
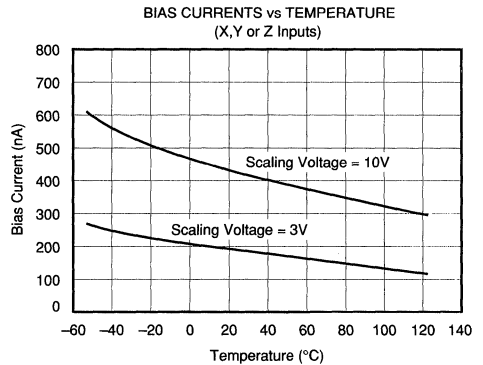
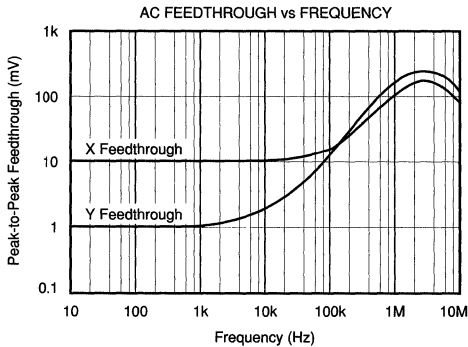
Substrate Bias: The back of the die should not be used for the $-V_S$ connection.
 NC = No Connection.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	100 x 92 ±5	2.54 x 2.34 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

TYPICAL PERFORMANCE CURVES

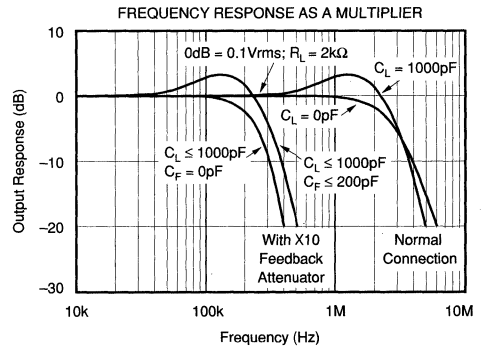
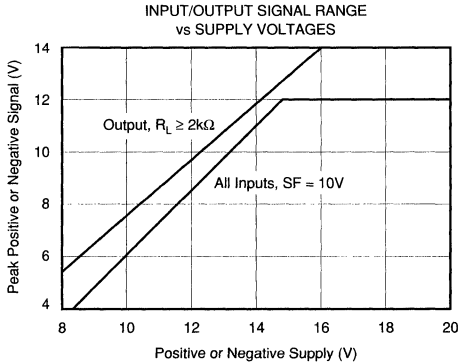
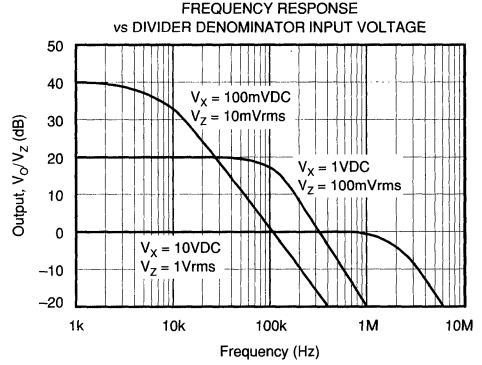
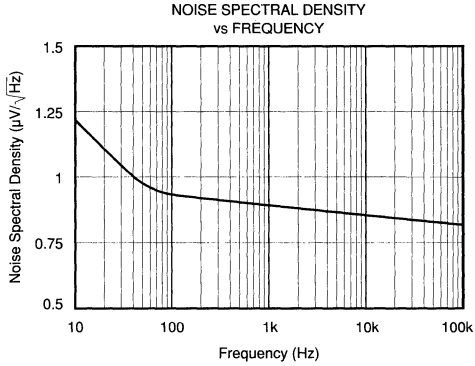
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $\pm V_{CC} = 15\text{VDC}$, unless otherwise noted.



THEORY OF OPERATION

The transfer function for the MPY534 is:

$$V_{OUT} = A \left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2) \right]$$

where:

A = Open-loop gain of the output amplifier (typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistor.

X, Y, A are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ± 1.25 SF.)

An intuitive understanding of transfer function can be gained by analogy to an op amp. By assuming that the open-loop gain, A, of the output amplifier is infinite, inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then,

an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT} .

The scale factor is accurately factory-adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4\text{k}\Omega \left[\frac{SF}{10 - SF} \right]$$

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Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

The MPY534 is fully characterized at $V_s = \pm 15V$, but operation is possible down to $\pm 8V$ with an attendant reduction of input and output range capability. Operation at voltages greater than $\pm 15V$ allows greater output swing to be achieved by using an output feedback attenuator (Figure 2).

BASIC MULTIPLIER CONNECTION

Figure 1 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user trimming circuitry. Some applications can benefit from trimming one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT} . In basic multiplier operation, the Z_2 input serves as the output voltage reference and should be connected to the ground reference of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 2 shows another method of changing the effective SF of the overall circuit using an attenuator in the feedback connection to Z_1 . This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input Z_2 .

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

SQUARER CIRCUIT

Squarer operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multiplier mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by using a reduced SF value.

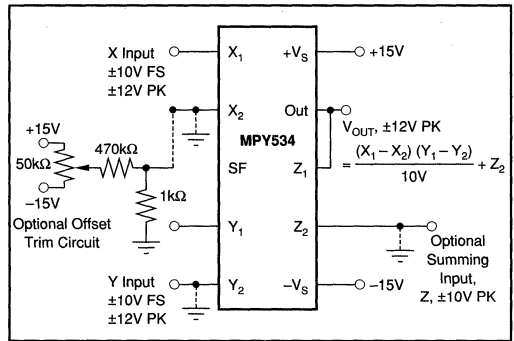


FIGURE 1. Basic Multiplier Connection.

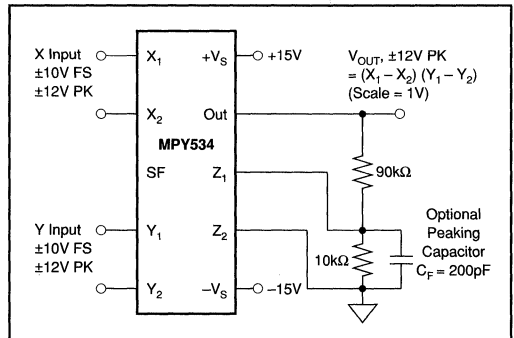


FIGURE 2. Connections for Scale-Factor of Unity.

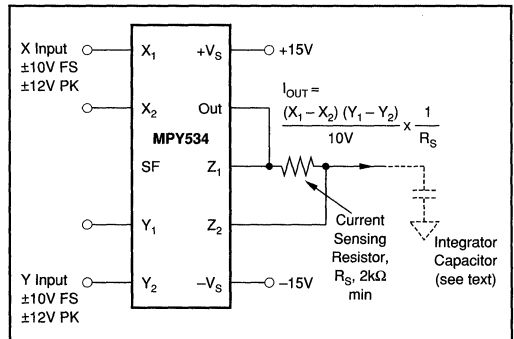


FIGURE 3. Conversion of Output to Current.

DIVIDER CIRCUIT

The MPY534 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs, respectively. Feedback is applied to the Y_2 input, and Y_1 can be summed directly into V_{OUT} . Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore, the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

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Accuracy of the divider mode typically ranges from 0.75% to 2.0% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of $\pm 3.5\text{mV}$ applied to the "low side" X input (X_2 for positive input voltages on X_1) can produce similar accuracies over a 100 to 1 denominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz) to both inputs. An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

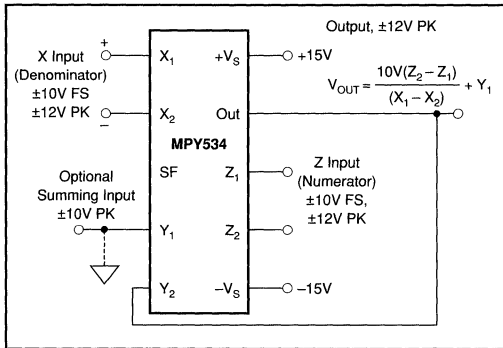


FIGURE 4. Basic Divider Connection.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately 10kΩ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

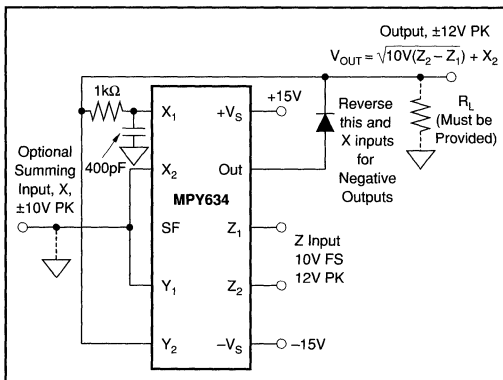


FIGURE 5. Square-Rooter Connection.

APPLICATIONS

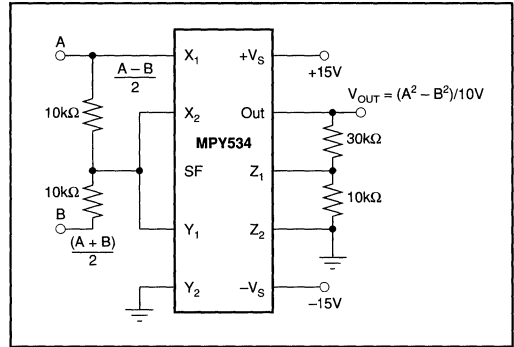
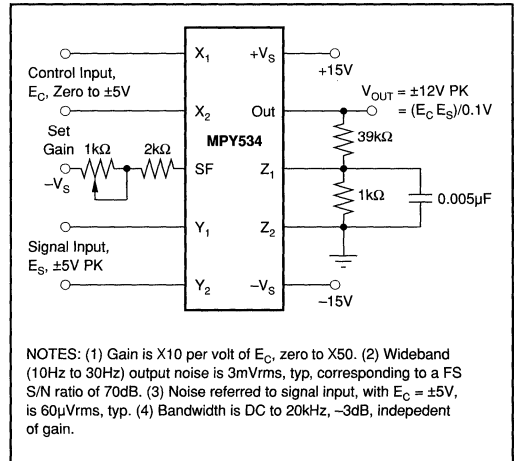


FIGURE 6. Difference-of-Squares.



NOTES: (1) Gain is X10 per volt of E_C , zero to X50. (2) Wideband (10Hz to 30Hz) output noise is 3mVrms, typ, corresponding to a FS S/N ratio of 70dB. (3) Noise referred to signal input, with $E_C = \pm 5\text{V}$, is 60μVrms, typ. (4) Bandwidth is DC to 20kHz, -3dB, independent of gain.

FIGURE 7. Voltage-Controlled Amplifier.

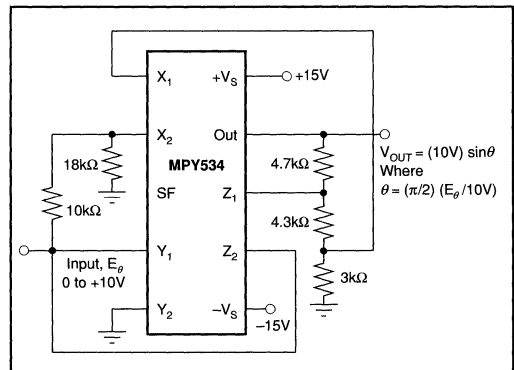


FIGURE 8. Sine-Function Generator.

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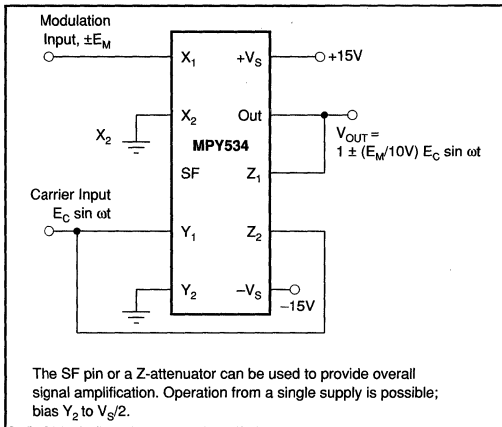


FIGURE 9. Linear AM Modulator.

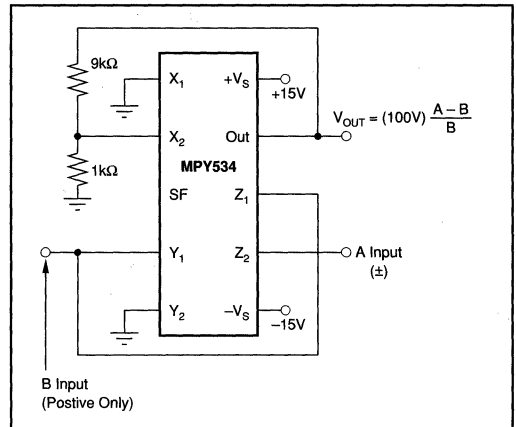


FIGURE 10. Percentage Computer.

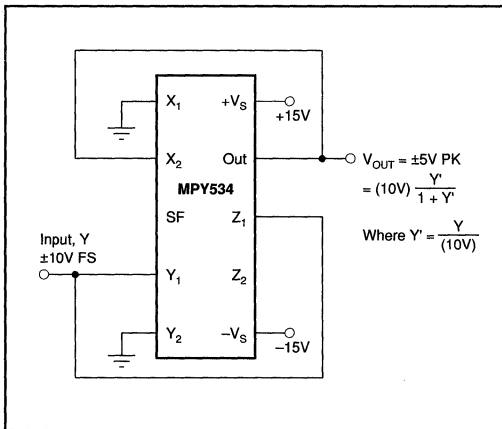
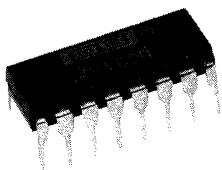


FIGURE 11. Bridge-Linearization Function.

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MPY600

Wide Bandwidth SIGNAL MULTIPLIER

FEATURES

- WIDE BANDWIDTH:
 - 75MHz — Current Output
 - 30MHz — Voltage Output
- LOW NOISE
- LOW FEEDTHROUGH: -60dB (5MHz)
- GROUND-REFERRED OUTPUT
- LOW OFFSET VOLTAGE

APPLICATIONS

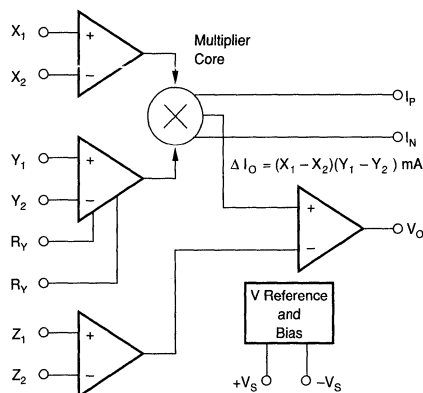
- MODULATOR/DEMODULATOR
- VIDEO SIGNAL PROCESSING
- CRT GEOMETRY CORRECTION
- CRT FOCUS CORRECTION
- VOLTAGE-CONTROLLED CIRCUITS

DESCRIPTION

The MPY600 is a wide-bandwidth four-quadrant signal multiplier. Its output voltage is equal to the algebraic product of the X and Y input voltages. For signals up to 30MHz, the on-board output op amp provides the complete multiplication function with a low-impedance voltage output. Differential current outputs extend multiplier bandwidth to 75MHz.

The MPY600 offers improved performance compared to common semiconductor modulator or multiplier circuits. It can be used for both two-quadrant (voltage-controlled amplifier) and four-quadrant (double-balanced) applications. While previous devices required cumbersome circuitry for trimming, balance and level-shifting, the MPY600 requires no external components. A single external resistor can be used to program the conversion gain for optimum spurious-free dynamic range. When used as a modulator, carrier feedthrough measures -60dB at 5MHz.

Differential X, Y and Z inputs can be connected in a variety of useful configurations, including squarer, divider, and square-rooter circuits. The MPY600 is available in 16-pin plastic DIP, specified for the industrial temperature range.



$$V_O = A \left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{2V} + Z_2 - Z_1 \right]$$

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SPECIFICATIONS

At $V_s = \pm 5V$, $T_A = +25^\circ C$ unless otherwise noted.

SPECIFICATION	CONDITIONS	MPY600AP			UNITS
		MIN	TYP	MAX	
INPUTS (X, Y, Z)					
Full-Scale Differential Input					
$X_1 - X_2$		± 1			V
$Y_1 - Y_2$		± 2			V
$Z_1 - Z_2$		± 2			V
Input Voltage Range			± 2.2		V
Differential Input Range			± 2.5		V
Input Impedance			100 1.5		k Ω pF
Input Offset Voltage			± 0.5	± 5	mV
Drift			25		$\mu V/^\circ C$
CMRR	$V_{CM} = \pm 2V$		70		dB
PSRR			70		dB
Input Bias Current (X, Y)			+15		μA
Z Input			-15		μA
VOLTAGE OUTPUT					
Transfer Function			$V_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{+ Z_2}$		V
Total Multiplier Error ⁽¹⁾	$-1V \leq X \leq 1V, -2V \leq Y \leq 2V$ $-2V \leq X \leq 2V, -2V \leq Y \leq 2V$		± 15	± 25	mV
Gain Error			± 25		mV
Gain Temperature Drift			± 1		%
Power Supply Rejection	$V_s = \pm 4$ to $\pm 6V$		± 200		ppm/ $^\circ C$
Noise	$f = 1kHz$ to $30MHz$		70		dB
Output Voltage Swing	$R_L = 100\Omega$	± 2.2	120		nV/ \sqrt{Hz}
Output Current		± 22	± 3		V
Short-Circuit Limit			± 30		mA
Bandwidth	Small Signal		50		mA
Slew Rate			30		MHz
Settling Time to 0.1%	4V Step		150		V/ μs
Differential Gain Error	3.58MHz, 0 to 0.7V		150		ns
Differential Phase Error	3.58MHz, 0 to 0.7V		0.2		%
Capacitive Load, Max	Stable Operation		0.2		Degrees
Feedthrough, X	X = 0dBm, f = 500kHz; Y Nulled		100		pF
	X = 0dBm, f = 5MHz; Y Nulled		-65		dB
Feedthrough, Y	Y = 0dBm, f = 500kHz; X Nulled		-60		dB
	Y = 0dBm, f = 5MHz; X Nulled		-70		dB
Distortion, X	X = 0dBm, f = 500kHz, Y = 2V		-50		dB
	X = 0dBm, f = 5MHz, Y = 2V		-60		dB
Distortion, Y	Y = 0dBm, f = 500kHz, X = 2V		-55		dB
	Y = 0dBm, f = 5MHz, X = 2V		-65		dB
			-55		dB
			-65		dB
			-55		dB
CURRENT OUTPUT					
Transfer Function			$\Delta I_o = (X_1 - X_2)(Y_1 - Y_2)/1000$		A
Total Multiplier Error ⁽¹⁾	$-1V \leq X \leq 1V, -2V \leq Y \leq 2V$ $-2V \leq X \leq 2V, -2V \leq Y \leq 2V$		± 20	± 80	μA
Gain Error			± 80		μA
Gain Temperature Drift			± 1		%
Power Supply Rejection	$V_s = \pm 4$ to $\pm 6V$		± 200		ppm/ $^\circ C$
Noise, Output			50		dB
Voltage Compliance Range			100		pA/ \sqrt{Hz}
Peak Output Current			± 2.5		V
Noise, Input-Referred	$f = 1kHz$ to $75MHz$		5		mA
Bandwidth, Small-Signal			50		nV/ \sqrt{Hz}
Settling Time to 0.1%	4mA Step		75		MHz
Feedthrough, X	X = 0dBm, f = 1MHz; Y Nulled		150		ns
	X = 0dBm, f = 10MHz; Y Nulled		-65		dB
Feedthrough, Y	Y = 0dBm, f = 1MHz; X Nulled		-45		dB
	Y = 0dBm, f = 10MHz; X Nulled		-75		dB
Distortion, X	X = 0dBm, f = 1MHz, Y = 2V		-65		dB
	X = 0dBm, f = 10MHz, Y = 2V		-55		dB
Distortion, Y	Y = 0dBm, f = 1MHz, X = 2V		-60		dB
	Y = 0dBm, f = 10MHz, X = 2V		-55		dB
			-65		dB
			-50		dB
POWER SUPPLY					
Rated Performance			± 5		V
Operating Current		± 4.75		± 8	V
			± 30	± 35	mA
TEMPERATURE RANGE					
Specified Temperature Range		-25		+85	$^\circ C$
Storage Temperature Range		-40		+125	$^\circ C$
Thermal Resistance, θ_{SA}			50		$^\circ C/W$

NOTE: (1) Deviation from ideal transfer function referred to full scale output. Includes gain, nonlinearity and offset errors.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Input Voltage Range	$\pm V_S$
Op Amp Output Current	100mA
Operating Temperature	+125°C
Storage Temperature	+150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

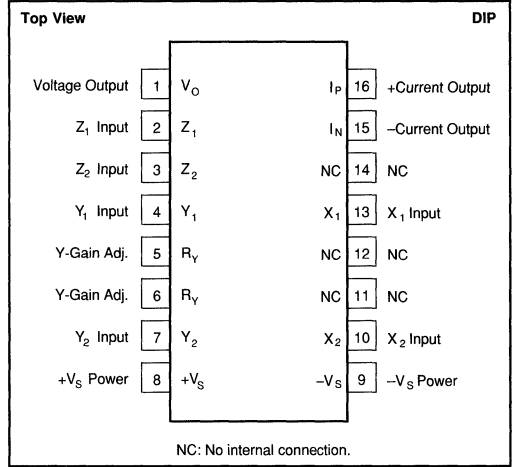
MODEL	PACKAGE	SPECIFIED TEMPERATURE RANGE
MPY600AP	16-Pin Plastic DIP	-25°C to +85°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPY600AP	16-Pin Plastic DIP	180

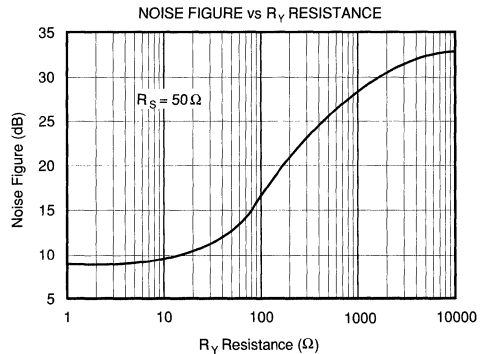
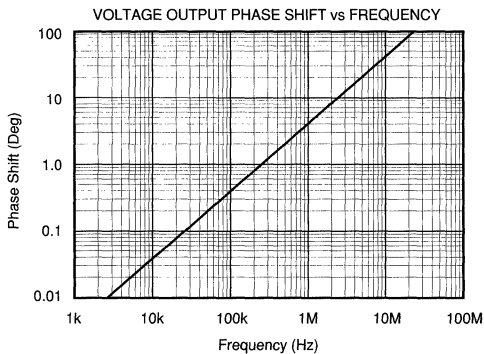
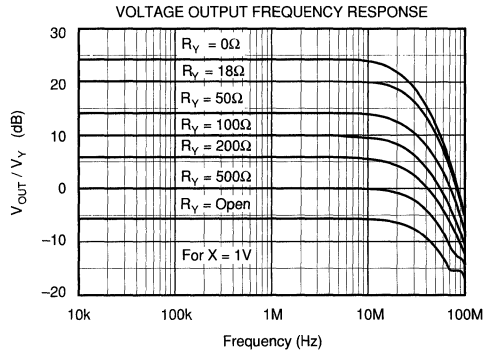
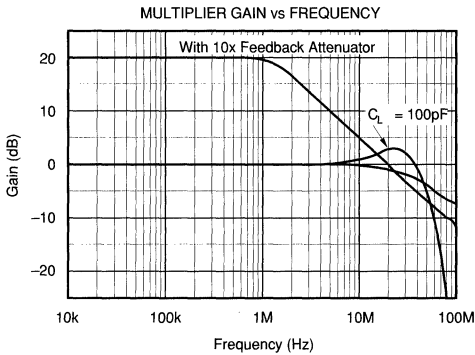
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ C$, $V_S = \pm 5V$ unless otherwise noted.

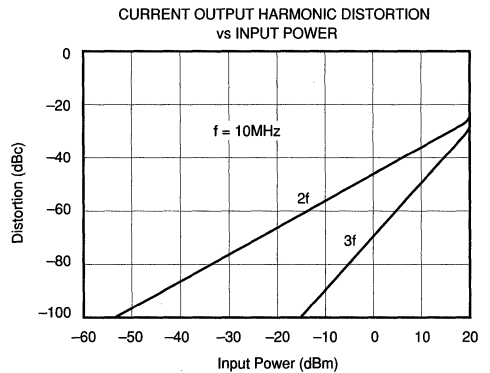
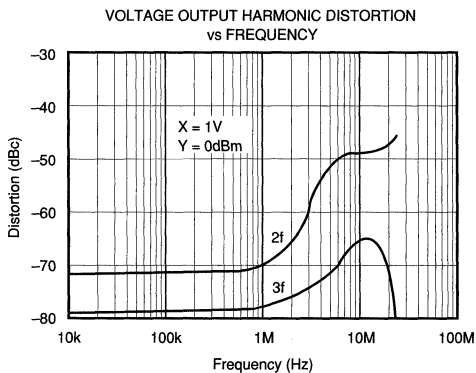
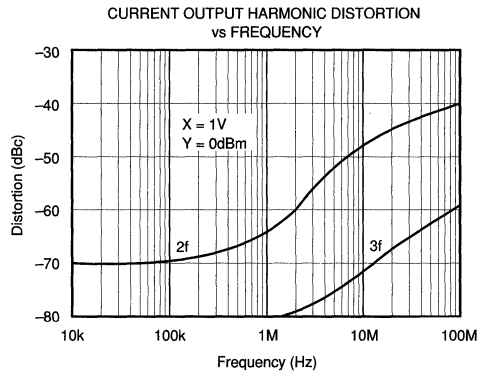
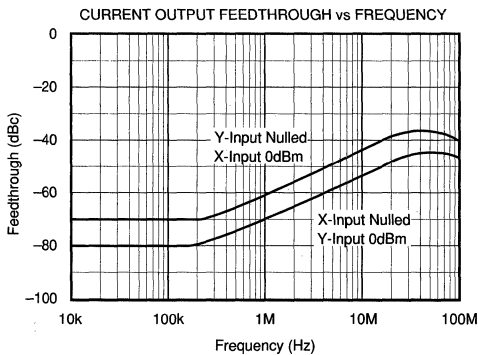
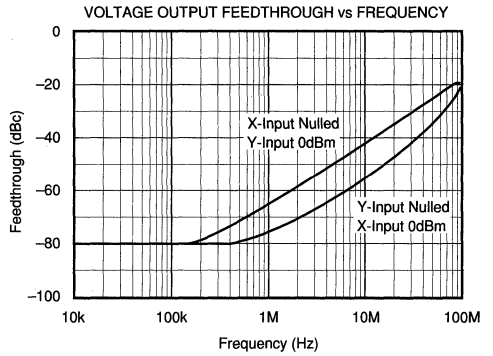
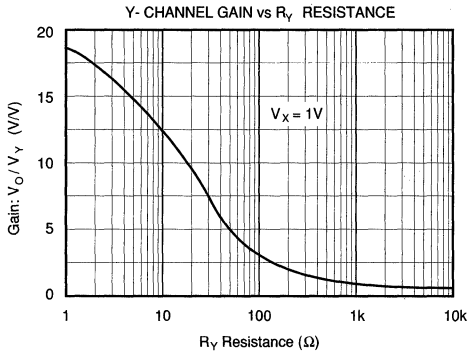


MPY600
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SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES (CONT)

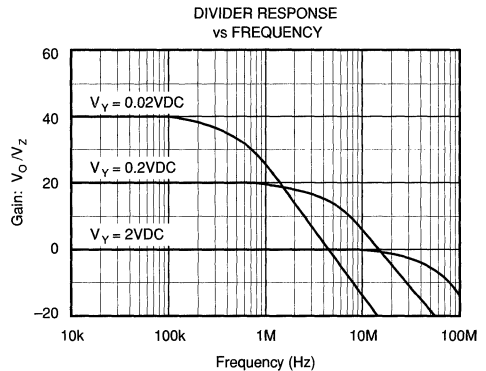
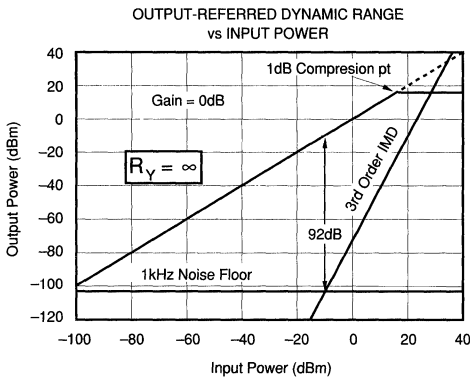
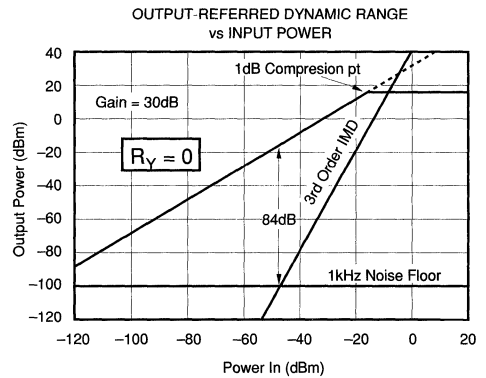
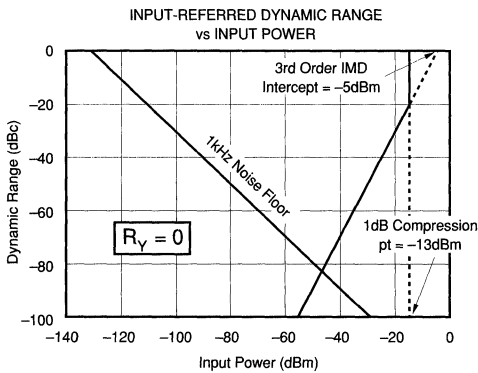
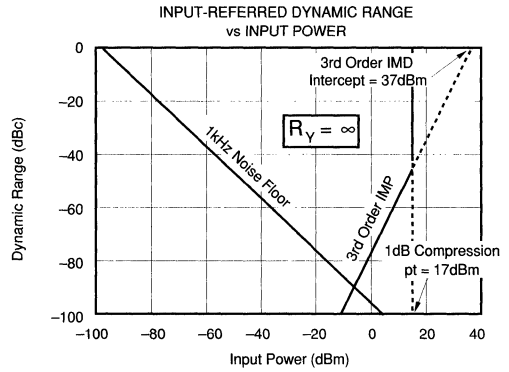
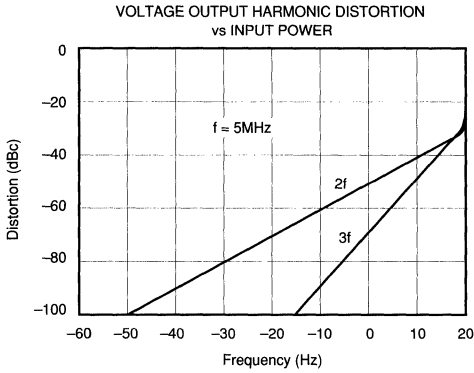
$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



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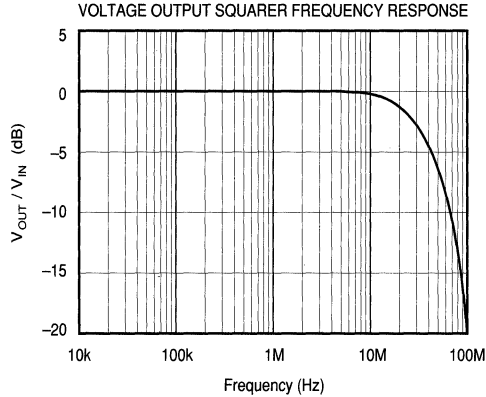
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ unless otherwise noted.



APPLICATION INFORMATION

POWER SUPPLIES

The MPY600 may be operated from power supplies from $\pm 4.75\text{V}$ to $\pm 8\text{V}$. Operation from $\pm 5\text{V}$ supplies is recommended. Since input and output levels are $\pm 2\text{V}$, larger supply voltage is not required for full output voltage swing. Furthermore, power dissipation can be minimized by using lower power supply voltage. Power supplies should be bypassed with good high-frequency capacitors such as ceramic or solid tantalum.

TRANSFER FUNCTION

The open-loop transfer function of the MPY600 is:

$$V_O = A \left[\frac{(X_1 - X_2) \cdot (Y_1 - Y_2)}{2V} - (Z_1 - Z_2) \right]$$

where A = open-loop gain of the output amplifier (typically 70dB).

X , Y , Z are differential input voltages— $\pm 2\text{V}$ max.

An intuitive understanding of the transfer function can be gained by analogy to an op amp. Assuming that the open-loop gain is infinite, any output voltage can be created by an infinitesimally small quantity with the brackets. An applications circuit can be analyzed by assigning circuit voltages to the X , Y and Z inputs and setting the bracketed quantity equal to zero.

For example, in the basic multiplier connection (Figure 1), $Z_1 = V_O$ and $Z_2 = 0$. Setting this equal to zero:

$$\left[\frac{(X_1 - X_2) \cdot (Y_1 - Y_2)}{2V} - V_O \right] = 0$$

Solving for V_O yields the transfer function of the circuit.

The X input is specified for $\pm 1\text{V}$ full-scale differential input. X inputs up to $\pm 2\text{V}$ provide useful operation with somewhat reduced accuracy and distortion performance. The Y input is rated for $\pm 2\text{V}$ full-scale input. The Y input gain (and therefore its full-scale range) can be varied with an external resistor connected to the R_Y terminals—see “Modulator/Demodulator.” Full-scale inputs ($X = \pm 1\text{V}$, $Y = \pm 2\text{V}$) produce a $\pm 1\text{V}$ output.

The differential inputs, X_1 , X_2 and Y_1 , Y_2 , make it easy to trim offset voltage. The trim voltage is applied to the X_2 or Y_2 input, which is otherwise grounded (see X_2 input, Figure 5). Polarity of the input signals can be reversed by interchanging the inputs (reversing the connections X_1 and X_2 , for instance). The unused current outputs (pins 15 and 16) must be grounded (or loaded—see discussion on current outputs).

The output amplifier is operated in unity gain. The output voltage can be increased (for small input signals) by placing the internal output op amp in higher gain (Figure 2). This reduces bandwidth and increases output offset voltage errors.

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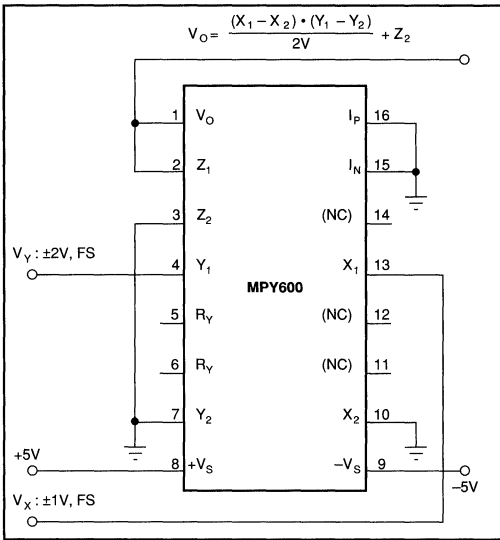


FIGURE 1. Basic Multiplier Connection.

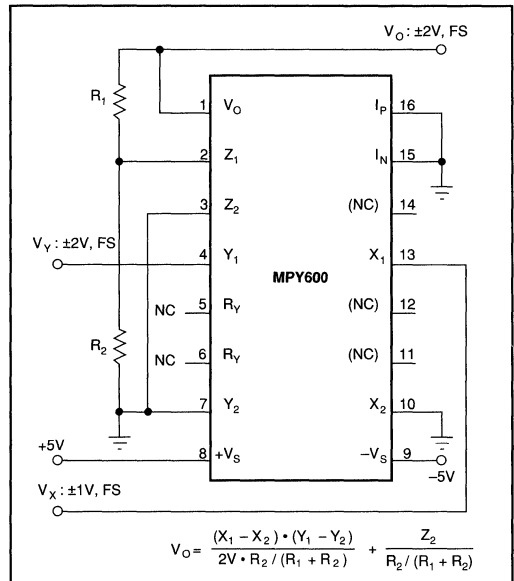


FIGURE 2. Adjusting the Scale Factor with Feedback.

CURRENT OUTPUT

The current output connections of the MPY600 can achieve wider bandwidth multiplier operation (Figure 3). The current output is determined by the X and Y inputs only, so applications which use the Z input to modify the transfer function (e.g., divider and square-root modes) cannot be used. A full-scale input of $\pm 1V$ on the X and $\pm 2V$ on the Y inputs produces a 2mA differential current at the current outputs. This consists of approximately 2.5mA quiescent current $\pm 1mA$ signal current on each output. The current outputs may be used to drive any load impedance which maintains the voltage on the current outputs within their compliance range. This compliance limit is approximately 2.5V from the power supply voltages. The current outputs and voltage output may be used simultaneously, if desired.

Output capacitance and stray capacitance at the current output terminals will limit the multiplier bandwidth. This makes large output resistors (greater than approximately $1k\Omega$) impractical. The current outputs can be used to drive 50Ω or 75Ω loads directly.

The circuit shown in Figure 4 uses the current outputs to drive an external OPA621 op amp configured as a current-difference amplifier. It operates in a noise gain of 3.5. The OPA621 is stable in a noise gain of two or greater and has a 500MHz gain-bandwidth product. It achieves the full bandwidth performance of the MPY600. R_1 determines the transfer function gain. R_3 provides a proper load to optimize high-frequency effects. R_4 is made equal to the parallel combination of R_1 and R_3 .

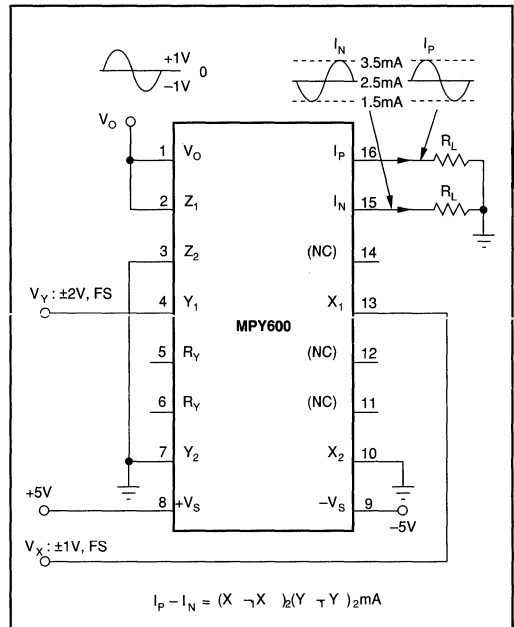


FIGURE 3. Current Output Connection.

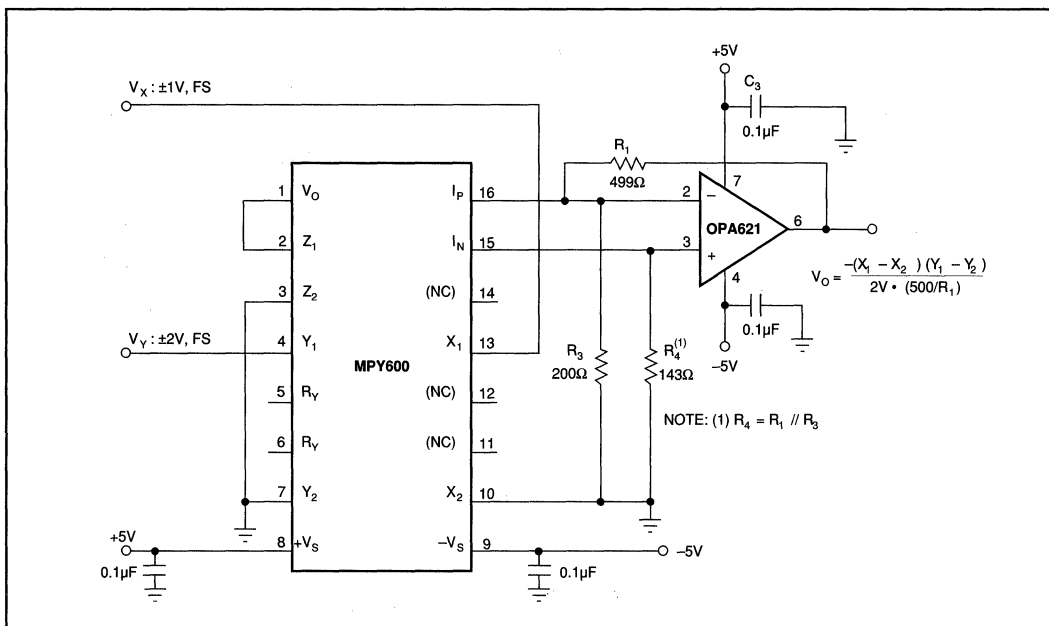


FIGURE 4. 75MHz DC-Coupled Multiplier.

MODULATOR/DEMOMULATOR

The balanced modulator or demodulator shown in Figure 5 uses the basic multiplier configuration. It shows the offset of the X input trimmed to null carrier feedthrough. It also illustrates the use of R_Y to change the gain of the Y input. This can be used to optimize the spurious-free dynamic range for a given input level. The Y input is optimized for $\pm 2V$ inputs. For lower input signals, the Y input can be programmed for higher gain by connecting an external resistor to the R_Y terminals. The conceptual diagram in Figure 6 reveals why varying the Y-channel gain can yield improved dynamic range. The R_Y selection curve in Figure 5 shows the optimum value of R_Y for a given Y-input signal level.

DIVIDER OPERATION

The MPY600 can be configured as a divider as shown in Figure 7. Numerator voltage is applied to the Z inputs; denominator voltage is applied to the Y_1 input. Since the

feedback connection is made to a multiplying input, the effective gain of the output amplifier varies as a function of the denominator input. This causes the bandwidth to vary with denominator (see Typical Performance Curves for divider bandwidth performance). Accuracy in divider operation is approximately 3% for a 10:1 denominator range. Errors grow large and will eventually saturate the output as the denominator voltage approaches 0V.

SQUARE-ROOT CIRCUIT

The circuit in Figure 8 provides an output voltage proportional to the square-root of the input (for positive input voltages). Diode D_1 prevents latch-up if the input should go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y differential inputs. The output polarity can be inverted by reversing the X input polarity and the diode. Accuracy can be improved by trimming the offset at the Z input.

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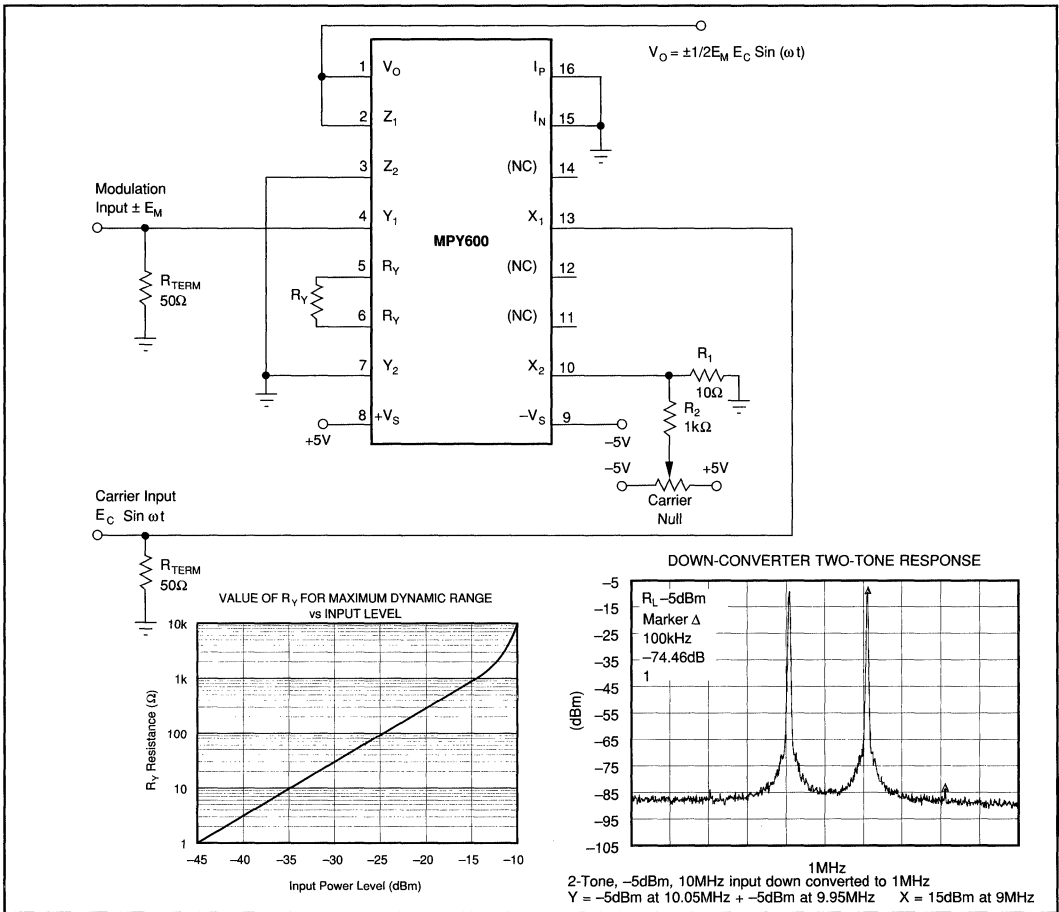


FIGURE 5. Balanced Modulator.

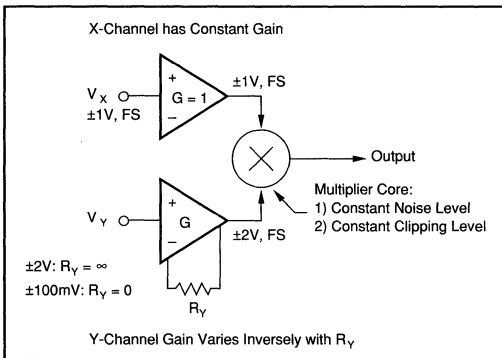


FIGURE 6. Variable Y-Channel Gain—Conceptual Model.

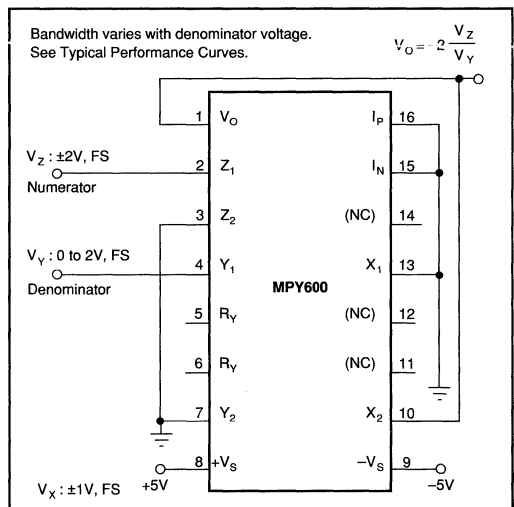


FIGURE 7. Divider Circuit.

MPY600

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SPECIAL FUNCTIONS

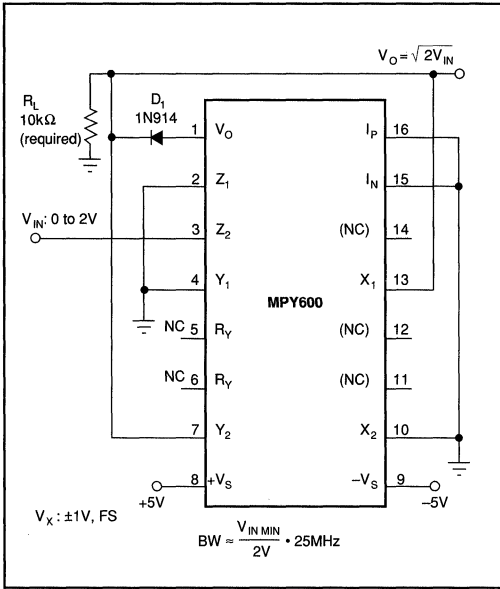


FIGURE 8. Square-Root Circuit.

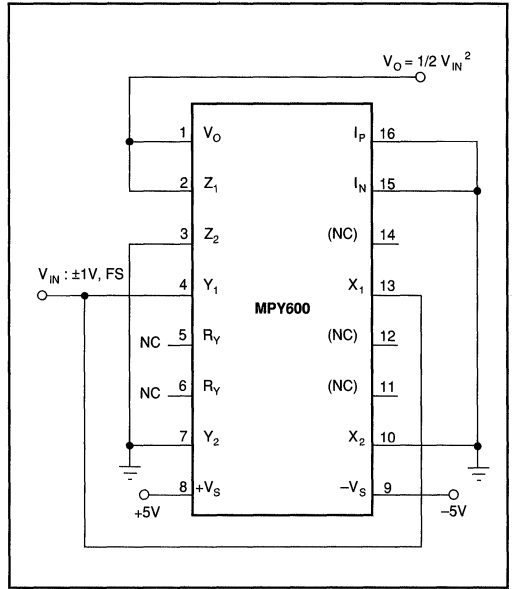


FIGURE 9. Squaring Circuit.

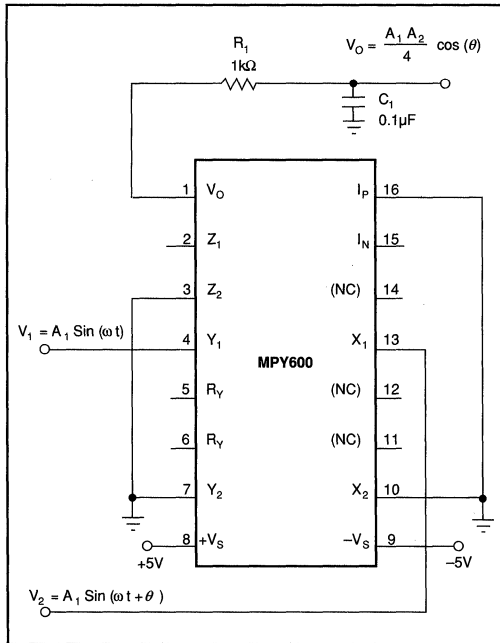


FIGURE 10. Phase Detector.

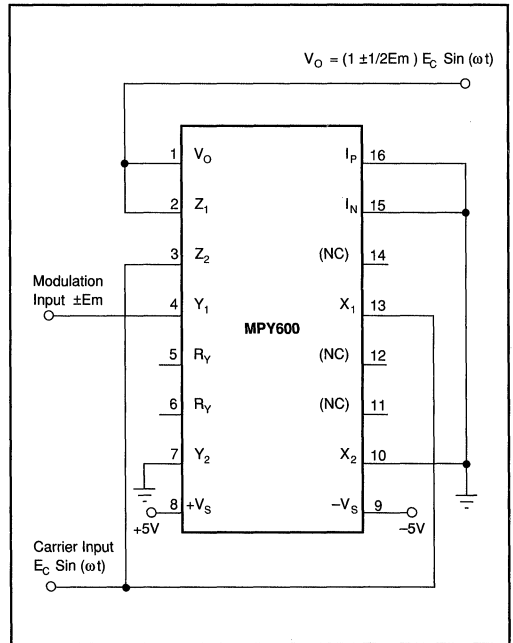


FIGURE 11. Linear AM Modulator.

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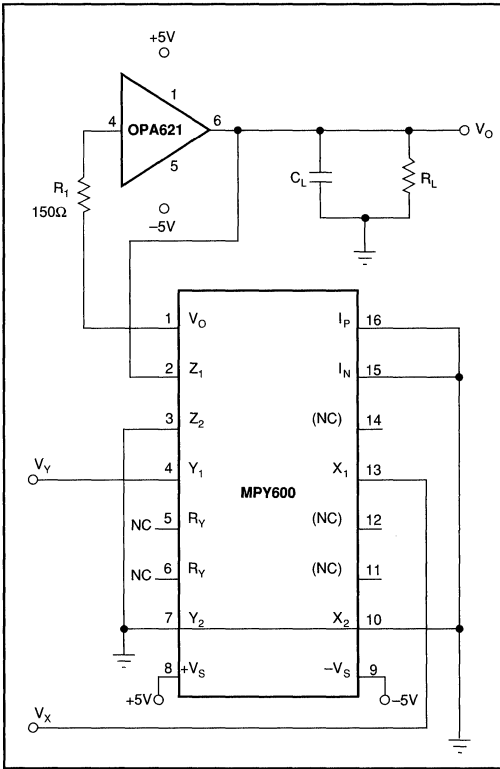


FIGURE 12. 25MHz Multiplier with Improved Load Driving Capability.

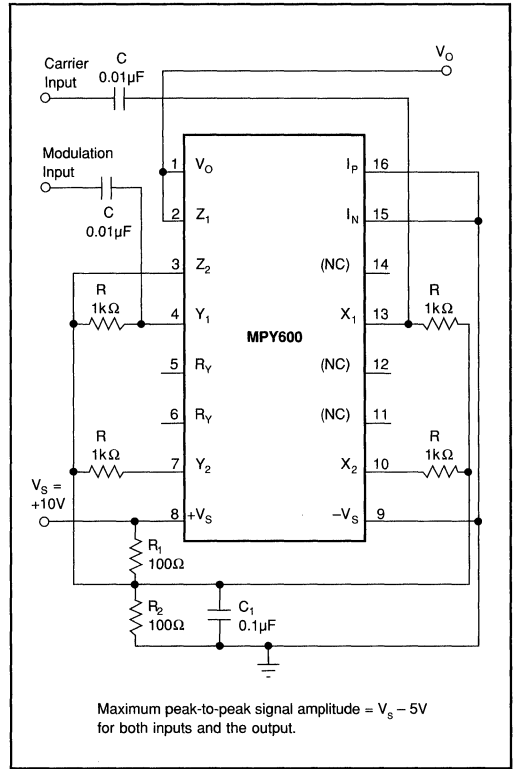


FIGURE 13. Single-Supply Balanced Modulator.

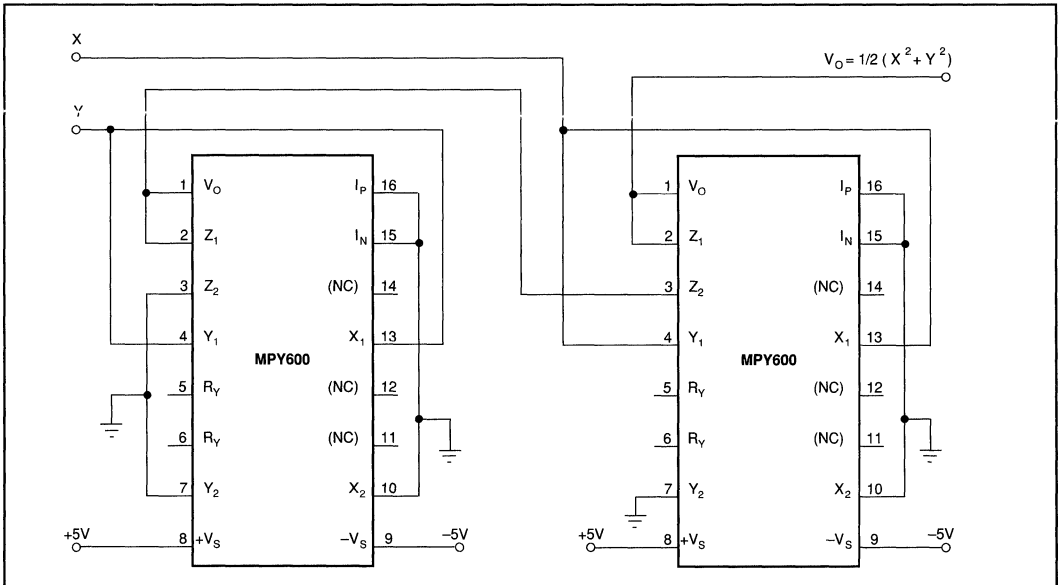


FIGURE 14. CRT Focus Correction.

MPY600

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SPECIAL FUNCTIONS

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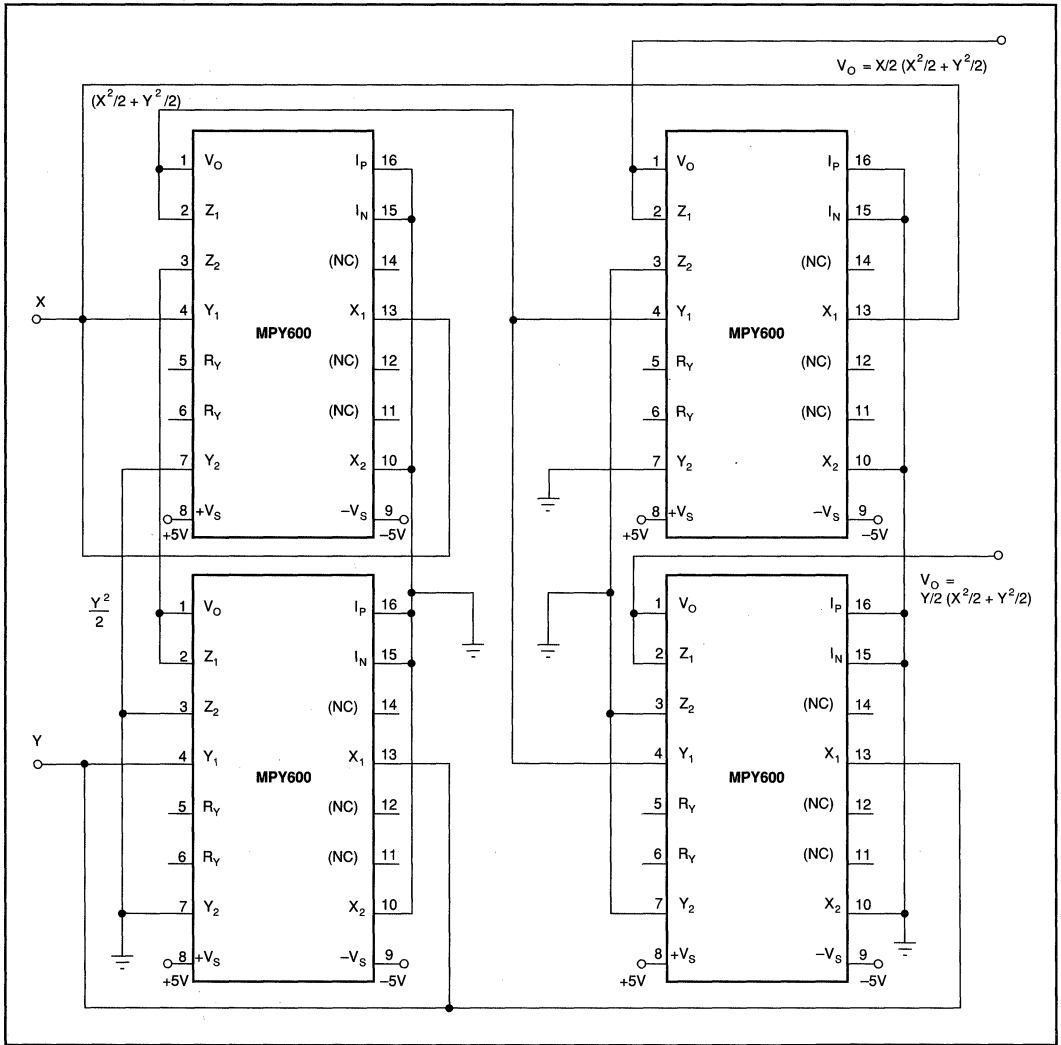
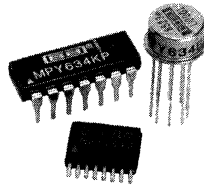


FIGURE 15. CRT Geometry Correction.

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MPY634

Wide Bandwidth PRECISION ANALOG MULTIPLIER

FEATURES

- WIDE BANDWIDTH: 10MHz typ
- ±0.5% MAX FOUR-QUADRANT ACCURACY
- INTERNAL WIDE-BANDWIDTH OP AMP
- EASY TO USE
- LOW COST

APPLICATIONS

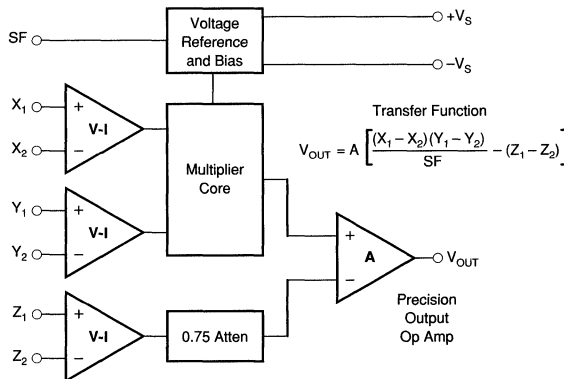
- PRECISION ANALOG SIGNAL PROCESSING
- MODULATION AND DEMODULATION
- VOLTAGE-CONTROLLED AMPLIFIERS
- VIDEO SIGNAL PROCESSING
- VOLTAGE-CONTROLLED FILTERS AND OSCILLATORS

DESCRIPTION

The MPY634 is a wide bandwidth, high accuracy, four-quadrant analog multiplier. Its accurately laser-trimmed multiplier characteristics make it easy to use in a wide variety of applications with a minimum of external parts, often eliminating all external trimming. Its differential X,Y, and Z inputs allow configuration as a multiplier, squarer, divider, square-rooter, and other functions while maintaining high accuracy.

The wide bandwidth of this new design allows signal processing at IF, RF, and video frequencies. The internal output amplifier of the MPY634 reduces design complexity compared to other high frequency multipliers and balanced modulator circuits. It is capable of performing frequency mixing, balanced modulation, and demodulation with excellent carrier rejection.

An accurate internal voltage reference provides precise setting of the scale factor. The differential Z input allows user-selected scale factors from 0.1 to 10 using external feedback resistors.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{VDC}$, unless otherwise noted.

MODEL	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE													
Transfer Function	*			$(X_1 - X_2)(Y_1 - Y_2) + Z_2$			*			*			
Total Error ⁽¹⁾ ($-10\text{V} \leq X, Y \leq +10\text{V}$) $T_A = \text{min to max}$		± 2.5	± 2.0		± 1.5	± 1.0		± 1.0	± 0.5			*	%
Total Error vs Temperature		± 0.03			± 0.022			± 0.015				± 2.0	%/°C
Scale Factor Error (SF = 10.000V Nominal) ⁽²⁾		± 0.25			± 0.1			*		*			%
Temperature Coefficient of Scaling Voltage		± 0.02			± 0.01			± 0.01		*			%/°C
Supply Rejection ($\pm 15\text{V} \pm 1\text{V}$)		*			± 0.01			*		*			%
Nonlinearity													
X ($X = 20\text{Vp-p}, Y = 10\text{V}$)		*			± 0.4			0.2	± 0.3	*			%
Y ($Y = 20\text{Vp-p}, X = 10\text{V}$)		*			± 0.01			*	± 0.1	*			%
Feedthrough ⁽³⁾													
X (Y Nulled, $X = 20\text{Vp-p}, 50\text{Hz}$)		*			± 0.3			± 0.15	± 0.3	*			%
Y (X Nulled, $Y = 20\text{Vp-p}, 50\text{Hz}$)		*			± 0.01			*	± 0.1	*			%
Both Inputs (500kHz, 1Vrms)													
Unnulled	40 ⁽⁴⁾	50		45	55		*	60		*	*		dB
Nulled	55 ⁽⁴⁾	60		55	65		60	70		*	*		dB
Output Offset Voltage		± 50	± 100		± 5	± 30		*	± 15	*	*	*	mV
Output Offset Voltage Drift		*			± 200			± 100		*	*	± 500	$\mu\text{V}/^\circ\text{C}$
DYNAMICS													
Small Signal BW, ($V_{\text{OUT}} = 0.1\text{Vrms}$)	6 ⁽⁴⁾	*		8	10		*	*		6	*		MHz
1% Amplitude Error ($C_{\text{LOAD}} = 1000\text{pF}$)		*			100			*			*		kHz
Slew Rate ($V_{\text{OUT}} = 20\text{Vp-p}$)		*			20			*			*		V/ μs
Settling Time (to 1%, $\Delta V_{\text{OUT}} = 20\text{V}$)		*			2			*			*		μs
NOISE													
Noise Spectral Density: SF = 10V		*			0.8			*			*		$\mu\text{V}/\sqrt{\text{Hz}}$
Wideband Noise: f = 10Hz to 5MHz		*			1			*			*		mVrms
f = 10Hz to 10kHz		*			90			*			*		μVrms
OUTPUT													
Output Voltage Swing	*			± 11			*			*			V
Output Impedance (f $\leq 1\text{kHz}$)		*			0.1			*		*			Ω
Output Short Circuit Current ($R_L = 0, T_A = \text{min to max}$)		*			30			*		*			mA
Amplifier Open Loop Gain (f = 50Hz)		*			85			*		*			dB
INPUT AMPLIFIERS (X, Y and Z)													
Input Voltage Range													
Differential V_{IN} ($V_{\text{CM}} = 0$)		*			± 12			*		*			V
Common-Mode V_{IN} ($V_{\text{DIFF}} = 0$) (see Typical Performance Curves)		*			± 10			*		*			V
Offset Voltage X, Y		± 25	± 100		± 5	± 20		± 2	± 10	*	*		mV
Offset Voltage Drift X, Y		200			100			50		*	*		$\mu\text{V}/^\circ\text{C}$
Offset Voltage Z		± 25	± 100		± 5	± 30		± 2	± 15	*	*		mV
Offset Voltage Drift Z		*			200			100		*	*	500	$\mu\text{V}/^\circ\text{C}$
CMRR	*	*		60	80		70	90		*	*		dB
Bias Current		*			0.8	2.0		*	*	*	*		μA
Offset Current		*			0.1			*	*	*	2.0		μA
Differential Resistance		*			10			*	*	*	*		M Ω
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		*			$10\text{V} \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*			*		
Total Error ⁽¹⁾ untrimmed ($X = 10\text{V}, -10\text{V} \leq Z \leq +10\text{V}$)		1.5			± 0.75			± 0.35			± 0.75		%
($X = 1\text{V}, -1\text{V} \leq Z \leq +1\text{V}$)		4.0			± 2.0			± 1.0			*		%
($0.1\text{V} \leq X \leq 10\text{V}, -10\text{V} \leq Z \leq 10\text{V}$)		5.0			± 2.5			± 1.0			*		%
SQUARE PERFORMANCE													
Transfer Function		*			$\frac{(X_1 - X_2)^2}{10\text{V}} + Z_2$			*			*		
Total Error ($-10\text{V} \leq X \leq 10\text{V}$)		± 1.2			± 0.6			± 0.3			*		%

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SPECIFICATIONS (CONT)

ELECTRICAL

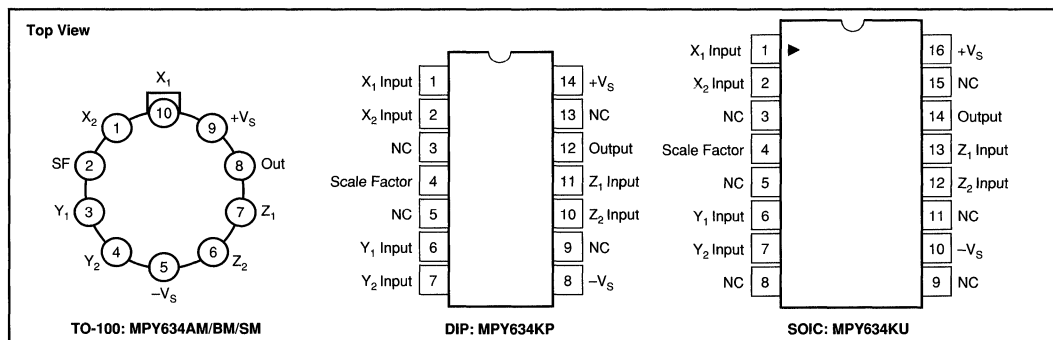
At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{VDC}$, unless otherwise noted.

MODEL	MPY634KP/KU			MPY634AM			MPY634BM			MPY634SM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SQUARE-ROOTER PERFORMANCE Transfer Function ($Z_1 \leq Z_2$) Total Error ⁽¹⁾ ($1\text{V} \leq Z \leq 10\text{V}$)		*		$\sqrt{10\text{V}(Z_2 - Z_1)} + X_2$				*			*		%
POWER SUPPLY Supply Voltage: Rated Performance Operating Supply Current, Quiescent		*	*	± 8	± 15	± 18	*	*	*	*	*	± 20	VDC VDC mA
TEMPERATURE RANGE Specification Storage	⁽⁵⁾ -40		⁽⁵⁾ +85	-25 -65	+85 +150		*	*	*	-55 *		+125 *	$^\circ\text{C}$ $^\circ\text{C}$

* Specification same as for MPY634AM.

NOTES: (1) Figures given are percent of full scale, $\pm 10\text{V}$ (i.e., $0.01\% = 1\text{mV}$). (2) May be reduced to 3V using external resistor between $-V_S$ and SF. (3) Irreducible component due to nonlinearity; excludes effect of offsets. (4) KP grade only. (5) KP grade only. 0°C to $+70^\circ\text{C}$ for KU grade.

PIN CONFIGURATIONS

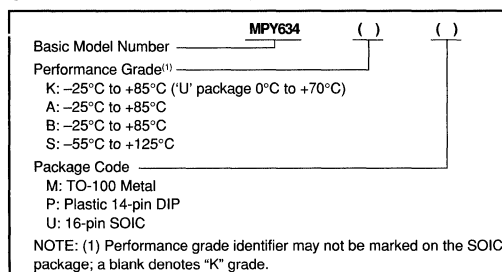


ABSOLUTE MAXIMUM RATINGS

PARAMETER	MPY634AM/BM	MPY634KP/KU	MPY634SM
Power Supply Voltage	± 18	*	± 20
Power Dissipation	500mW	*	*
Output Short-Circuit to Ground	Indefinite	*	*
Input Voltage (all X, Y and Z)	$\pm V_S$	*	*
Temperature Range: Operating Storage	$-25^\circ\text{C}/+85^\circ\text{C}$ $-65^\circ\text{C}/+150^\circ\text{C}$	*	$-55^\circ\text{C}/+125^\circ\text{C}$ *
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$	*	*
SOIC 'KU' Package		+260 $^\circ\text{C}$	

* Specification same as for MPY634AM/BM.

ORDERING INFORMATION



PACKAGE INFORMATION⁽¹⁾

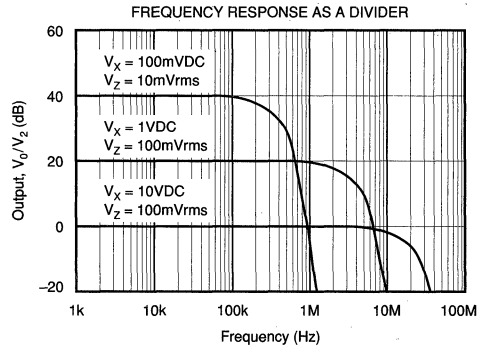
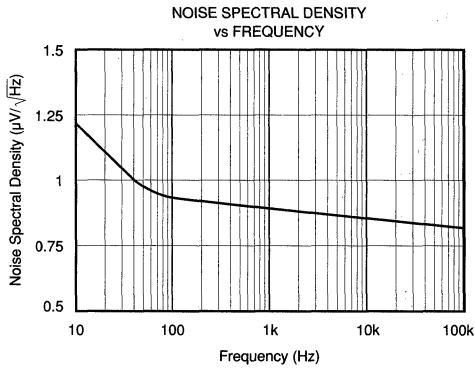
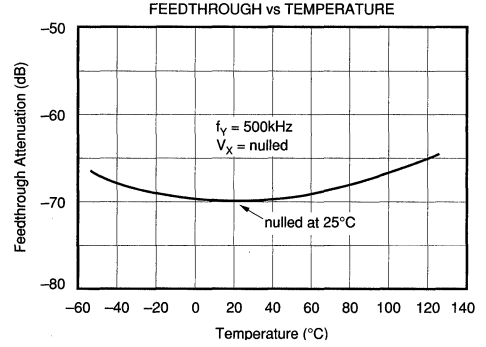
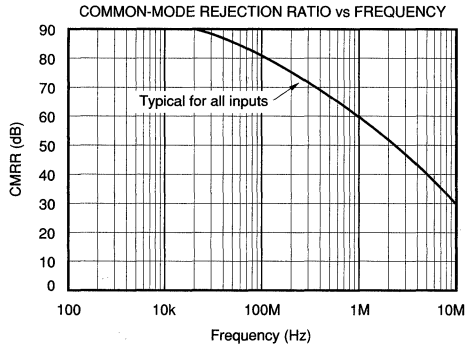
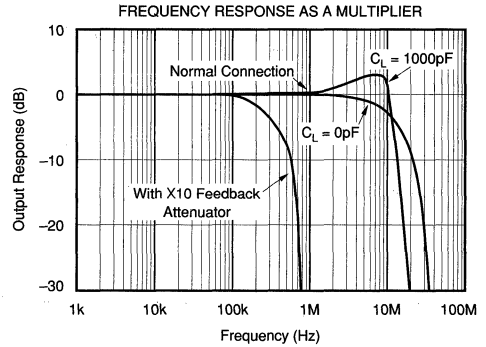
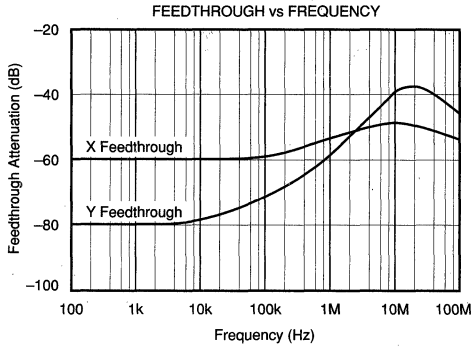
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPY634KP	14-Pin PDIP	010
MPY634KU	16-Pin SOIC	211
MPY634AM	TO-100	007
MPY634BM	TO-100	007
MPY634SM	TO-100	007

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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TYPICAL PERFORMANCE CURVES

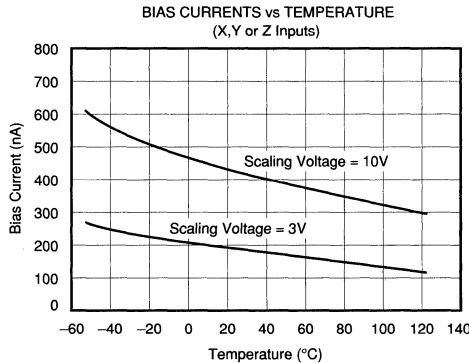
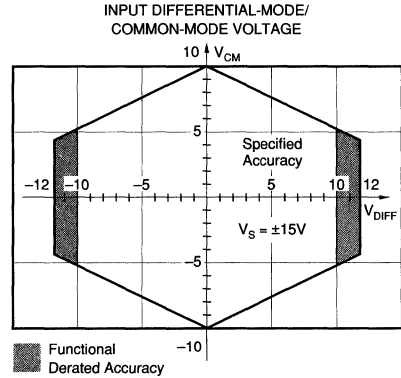
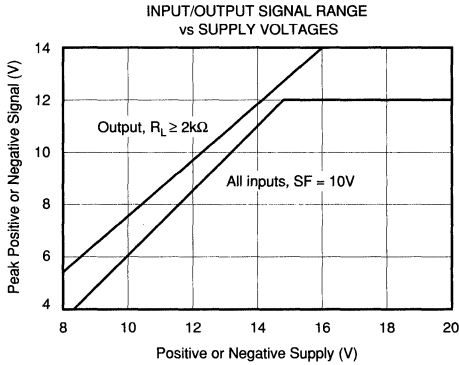
$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$, unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$, unless otherwise noted.



THEORY OF OPERATION

The transfer function for the MPY634 is:

$$V_{OUT} = A \left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2) \right]$$

where:

A = open-loop gain of the output amplifier (typically 85dB at DC).

SF = Scale Factor. Laser-trimmed to 10V but adjustable over a 3V to 10V range using external resistors.

X, Y, Z are input voltages. Full-scale input voltage is equal to the selected SF. (Max input voltage = ± 1.25 SF).

An intuitive understanding of transfer function can be gained by analogy to the op amp. By assuming that the open-loop gain, A, of the output operational amplifier is infinite,

inspection of the transfer function reveals that any V_{OUT} can be created with an infinitesimally small quantity within the brackets. Then, an application circuit can be analyzed by assigning circuit voltages for all X, Y and Z inputs and setting the bracketed quantity equal to zero. For example, the basic multiplier connection in Figure 1, $Z_1 = V_{OUT}$ and $Z_2 = 0$. The quantity within the brackets then reduces to:

$$\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (V_{OUT} - 0) = 0$$

This approach leads to a simple relationship which can be solved for V_{OUT} to provide the closed-loop transfer function.

The scale factor is accurately factory adjusted to 10V and is typically accurate to within 0.1% or less. The scale factor may be adjusted by connecting a resistor or potentiometer between pin SF and the $-V_S$ power supply. The value of the external resistor can be approximated by:

$$R_{SF} = 5.4k\Omega \left[\frac{SF}{10 - SF} \right]$$

Internal device tolerances make this relationship accurate to within approximately 25%. Some applications can benefit from reduction of the SF by this technique. The reduced input bias current, noise, and drift achieved by this technique can be likened to operating the input circuitry in a higher gain, thus reducing output contributions to these effects. Adjustment of the scale factor does not affect bandwidth.

The MPY634 is fully characterized at $V_S = \pm 15V$ but operation is possible down to $\pm 8V$ with an attendant reduction of input and output range capability. Operation at voltages greater than $\pm 15V$ allows greater output swing to be achieved by using an output feedback attenuator (Figure 1).

As with any wide bandwidth circuit, the power supplies should be bypassed with high frequency ceramic capacitors. These capacitors should be located as near as practical to the power supply connections of the MPY634. Improper bypassing can lead to instability, overshoot, and ringing in the output.

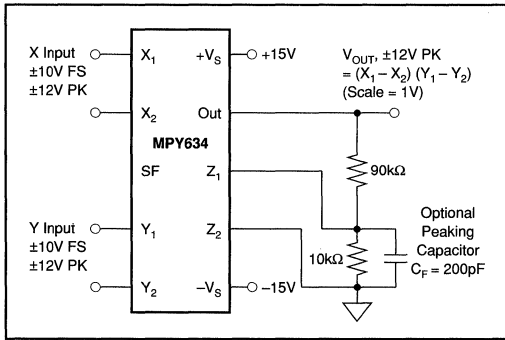


FIGURE 1. Connections for Scale-Factor of Unity.

BASIC MULTIPLIER CONNECTION

Figure 2 shows the basic connection as a multiplier. Accuracy is fully specified without any additional user-trimming circuitry. Some applications can benefit from trimming of one or more of the inputs. The fully differential inputs facilitate referencing the input quantities to the source voltage common terminal for maximum accuracy. They also allow use of simple offset voltage trimming circuitry as shown on the X input.

The differential Z input allows an offset to be summed in V_{OUT} . In basic multiplier operation, the Z_2 input serves as the output voltage ground reference and should be connected to the ground of the driven system for maximum accuracy.

A method of changing (lowering) SF by connecting to the SF pin was discussed previously. Figure 1 shows an alternative method of changing the effective SF of the overall circuit by using an attenuator in the feedback connection to Z_1 . This method puts the output amplifier in a higher gain and is thus accompanied by a reduction in bandwidth and an

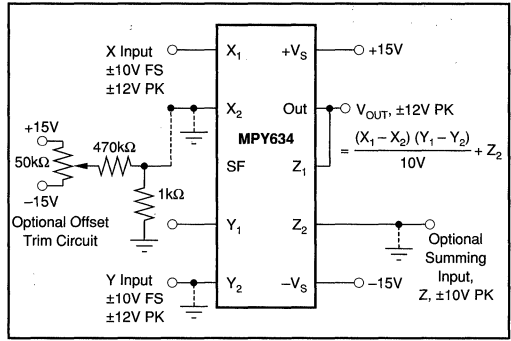


FIGURE 2. Basic Multiplier Connection.

increase in output offset voltage. The larger output offset may be reduced by applying a trimming voltage to the high impedance input, Z_2 .

The flexibility of the differential Z inputs allows direct conversion of the output quantity to a current. Figure 3 shows the output voltage differentially-sensed across a series resistor forcing an output-controlled current. Addition of a capacitor load then creates a time integration function useful in a variety of applications such as power computation.

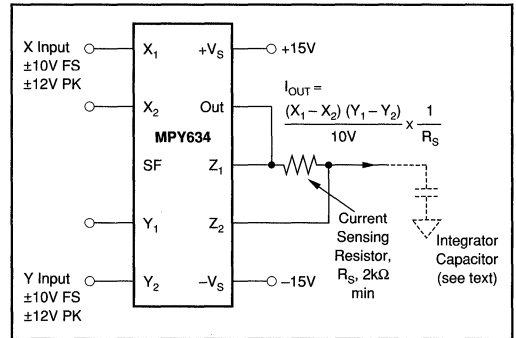


FIGURE 3. Conversion of Output to Current.

SQUARER CIRCUIT (FREQUENCY DOUBLER)

Squarer, or frequency doubler, operation is achieved by paralleling the X and Y inputs of the standard multiplier circuit. Inverted output can be achieved by reversing the differential input terminals of either the X or Y input. Accuracy in the squaring mode is typically a factor of two better than the specified multiplier mode with maximum error occurring with small (less than 1V) inputs. Better accuracy can be achieved for small input voltage levels by reducing the scale factor, SF.

DIVIDER OPERATION

The MPY634 can be configured as a divider as shown in Figure 4. High impedance differential inputs for the numerator and denominator are achieved at the Z and X inputs,

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respectively. Feedback is applied to the Y_2 input, and Y_1 is normally referenced to output ground. Alternatively, as the transfer function implies, an input applied to Y_1 can be summed directly into V_{OUT} . Since the feedback connection is made to a multiplying input, the effective gain of the output op amp varies as a function of the denominator input voltage. Therefore, the bandwidth of the divider function is proportional to the denominator voltage (see Typical Performance Curves).

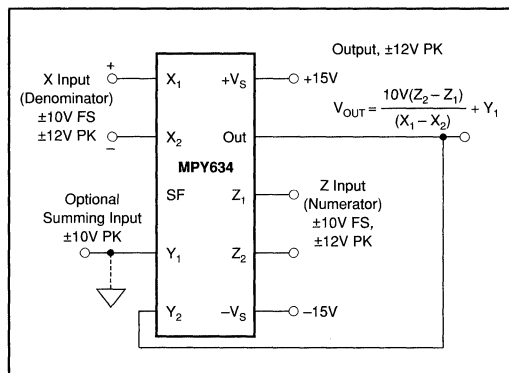


FIGURE 4. Basic Divider Connection.

Accuracy of the divider mode typically ranges from 1.0% to 2.5% for a 10 to 1 denominator range depending on device grade. Accuracy is primarily limited by input offset voltages and can be significantly improved by trimming the offset of the X input. A trim voltage of $\pm 3.5\text{mV}$ applied to the "low side" X input (X_2 , for positive input voltages on X_1) can produce similar accuracies over 100 to 1 denominator range. To trim, apply a signal which varies from 100mV to 10V at a low frequency (less than 500Hz). An offset sine wave or ramp is suitable. Since the ratio of the quantities should be constant, the ideal output would be a constant 10V. Using AC coupling on an oscilloscope, adjust the offset control for minimum output voltage variation.

SQUARE-ROOTER

A square-rooter connection is shown in Figure 5. Input voltage is limited to one polarity (positive for the connection shown). The diode prevents circuit latch-up should the input go negative. The circuit can be configured for negative input and positive output by reversing the polarity of both the X and Y inputs. The output polarity can be reversed by reversing the diode and X input polarity. A load resistance of approximately $10\text{k}\Omega$ must be provided. Trimming for improved accuracy would be accomplished at the Z input.

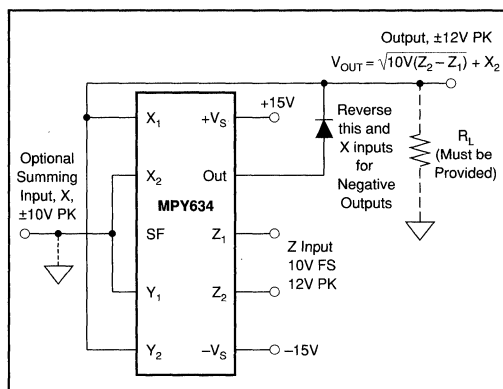


FIGURE 5. Square-Rooter Connection.

APPLICATIONS

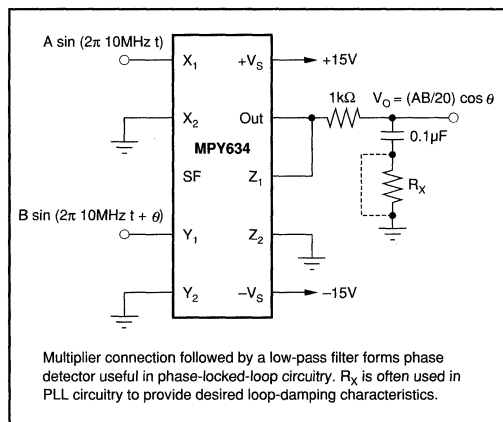


FIGURE 6. Phase Detector.

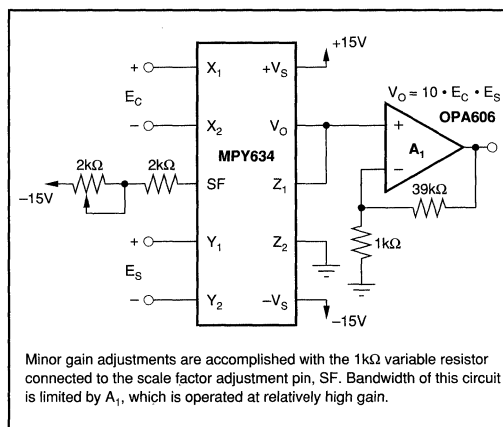


FIGURE 7. Voltage-Controlled Amplifier.

MPY634

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SPECIAL FUNCTIONS

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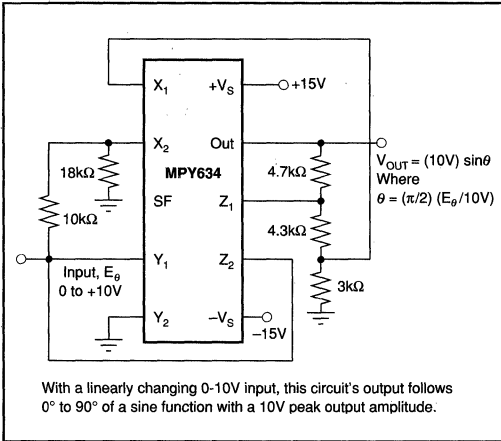


FIGURE 8. Sine-Function Generator.

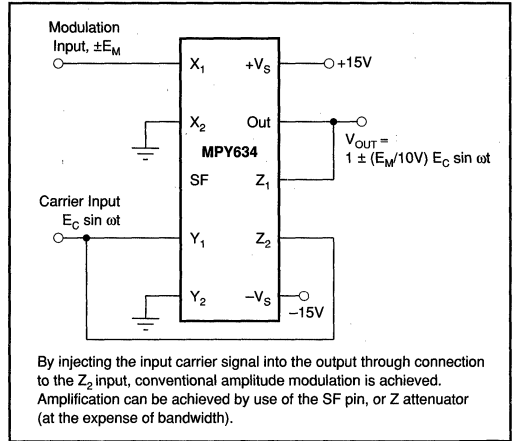


FIGURE 9. Linear AM Modulator.

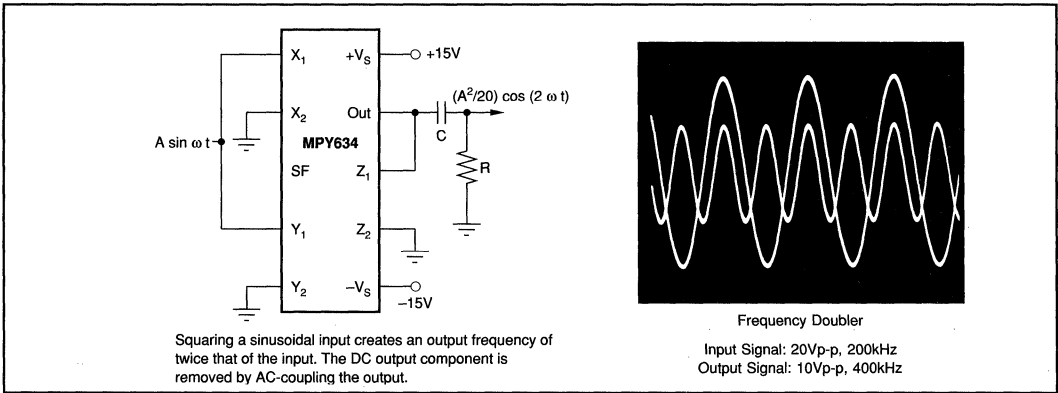


FIGURE 10. Frequency Doubler.

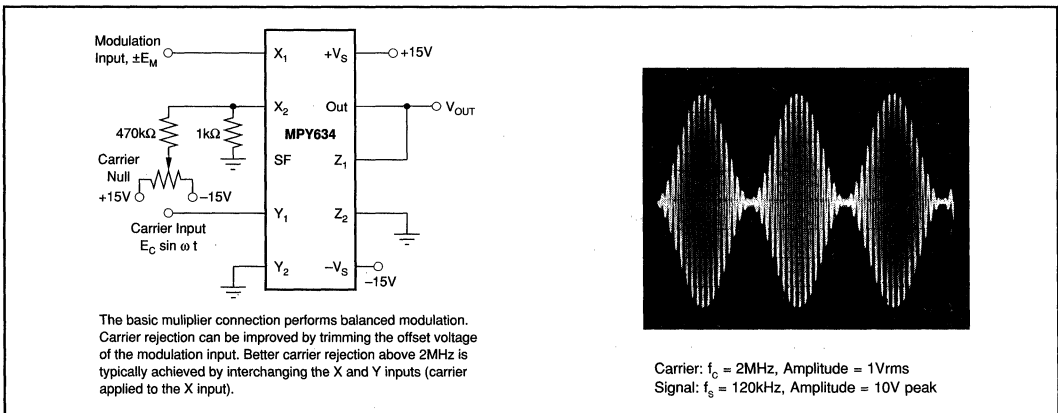


FIGURE 11. Balanced Modulator.

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SHC615

Wide-Bandwidth, DC RESTORATION CIRCUIT

FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
Comparator: 280MHz
- LOW INPUT BIAS CURRENT: $-0.3\mu\text{A}$
- SAMPLE/HOLD SWITCHING TRANSIENTS: $+1/-7\text{mV}$
- SAMPLE/HOLD FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fc
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

DESCRIPTION

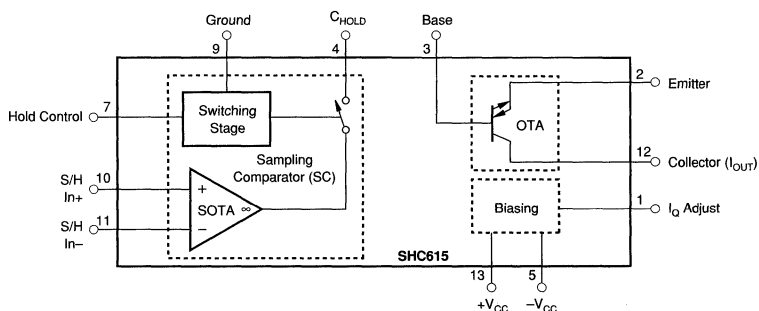
The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low-frequency hum suppression of wideband amplifiers or buffers. Although it was designed to stabilize the performance of video signals, the circuit can also be used as a sample and hold amplifier, high-speed integrator, or peak detector for nano second pulses. A wide-band Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast and precise sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal volt-

APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/PEAK DETECTORS
- PULSE CODE MODULATOR/DEMULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

age-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nano seconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is packaged in SO-14 surface mount packages and 14-pin plastic DIPs, and is specified over the extended temperature range of -40°C to $+85^{\circ}\text{C}$.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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DC SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$, $R_C = 300\Omega$, $R_M = 150\Omega$ and $T_A = +25^\circ C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
OTA					
OFFSET VOLTAGE Initial vs Temperature vs Supply (tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$		8 40 55	± 40	mV $\mu V/^\circ C$ dB
B-INPUT BIAS CURRENT Initial vs Temperature				-0.3 1	± 0.9
C-OUTPUT BIAS CURRENT Initial		-200	-77	+100	μA
B-INPUT IMPEDANCE			4.4		$M\Omega$
INPUT NOISE Voltage Noise Density, B-to-E Voltage Noise Density, B-to-C	$f_{OUT} = 100kHz$ to $100MHz$ $f_{OUT} = 100kHz$ to $100MHz$		2.2 4.5		nV/\sqrt{Hz} nV/\sqrt{Hz}
INPUT VOLTAGE RANGE			± 3.4		V
OUTPUT Output Voltage Compliance C-Current Output E-Current Output C-Output Impedance E-Output Impedance Open-Loop Gain		± 18 ± 18	± 3.2 ± 20 ± 20 0.5 12 96		V mA mA $M\Omega$ Ω dB
TRANSCONDUCTANCE	Small Signal, $<200mV$		70		mA/V



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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DC SPECIFICATIONS (CONT)

ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 1k\Omega$, $R_O = 300\Omega$, and $T_A = +25^\circ C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
COMPARATOR					
INPUT BIAS CURRENT Initial vs Temperature			1.0 -2.3	± 5	μA $nA/^\circ C$
C-OUTPUT BIAS CURRENT Initial vs Temperature			± 4 ± 13	± 25	μA $nA/^\circ C$
INPUT IMPEDANCE Input Impedance			0.2		$M\Omega$
INPUT NOISE Voltage Noise Density	$f_{OUT} = 100kHz \text{ to } 100MHz$		5		nV/\sqrt{Hz}
INPUT VOLTAGE RANGE Input Voltage Range Common-Mode Input Range			± 3.0 ± 4.0		V V
OUTPUT Output Voltage Compliance C-Current Output C-Output Impedance Open-Loop Gain		± 3.5	± 3.5 ± 4.0 620 2 83		V mA $k\Omega pF$ dB
TRANSCONDUCTANCE Transconductance			22		mA/V
HOLD CONTROL Logic 1 Voltage Logic 0 Voltage Logic 1 Current Logic 0 Current	V Hold Control = 5.0V V Hold Control = 0.8V	+2 0	1 0.05	$+V_{CC} + 0.6$ 0.8	V V μA μA
TRANSFER CHARACTERISTICS Charge Injection Feedthrough Rejection	Track-To-Hold Hold Mode		40 -100		fC dB
COMPLETE SHC615					
POWER SUPPLY Rated Voltage Derated Performance Quiescent Current Rejection Rate	Programmable (Useful Range)	± 4.5 ± 3	± 5 ± 14 -70	± 5.5 ± 36	VDC VDC mA dB
TEMPERATURE RANGE Operating Storage		-40 -40		+85 +125	$^\circ C$ $^\circ C$

SHC615

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SPECIAL FUNCTIONS

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AC SPECIFICATIONS

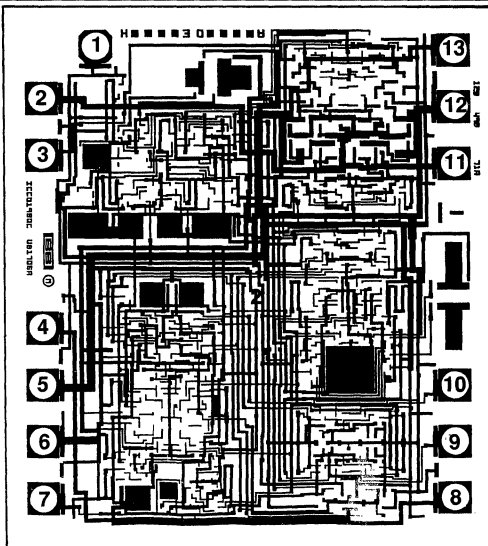
ELECTRICAL

At $V_{CC} = \pm 5VDC$, $R_{LOAD} = 100\Omega$, $R_{SOURCE} = 50\Omega$, $R_Q = 300\Omega$, and $T_A = +25^\circ C$, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
FREQUENCY DOMAIN					
OTA					
LARGE-SIGNAL BANDWIDTH (-3dB), (B-to-E)	$V_{OUT} = 5.0Vp-p$		430		MHz
	$V_{OUT} = 2.8Vp-p$		540		MHz
	$V_{OUT} = 1.4Vp-p$		620		MHz
SMALL-SIGNAL BANDWIDTH B-TO-E	$V_{OUT} = 0.2Vp-p$		520		MHz
DIFFERENTIAL GAIN (B-TO-E)	$f = 4.43MHz$, $V_{OUT} = 0.7Vp-p$, $R_L = 150\Omega$ $R_L = 500\Omega$		1.8		%
			0.1		%
DIFFERENTIAL PHASE (B-TO-E)	$f = 4.43MHz$, $V_{OUT} = 0.7Vp-p$, $R_L = 150\Omega$ $R_L = 500\Omega$		0.07		°
			0.01		°
HARMONIC DISTORTION (B-TO-E) Second Harmonic Third Harmonic	$f = 30MHz$, $V_{OUT} = 1.4Vp-p$		-50		dBc
			-46		dBc
LARGE SIGNAL BANDWIDTH (-3dB), (B-to-C)	$V_{OUT} = 5.0Vp-p$		250		MHz
	$V_{OUT} = 2.8Vp-p$		580		MHz
	$V_{OUT} = 1.4Vp-p$		750		MHz
SMALL SIGNAL BANDWIDTH B-to-C	$V_{OUT} = 0.2Vp-p$		680		MHz
COMPARATOR					
Sample Mode					
BANDWIDTH (-3dB)	$I_{OUT} = 4mA$ $I_{OUT} = 2mA$ $I_{OUT} = 1mA$		240		MHz
			270		MHz
			280		MHz
TIME DOMAIN					
OTA					
RISE TIME	2Vp-p Step, 10% to 90% B-to-E B-to-C		1.1		ns
			1.2		ns
SLEW RATE	2Vp-p, B-to-E B-to-C 5Vp-p, B-to-E B-to-C		1800		V/ μs
			1700		V/ μs
			3300		V/ μs
			3000		V/ μs
COMPARATOR					
RISE TIME (Sample Mode)	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm 2mA$ $C_{LOAD} = 1pF$		2.5		ns
SLEW RATE (Sample Mode)	10% to 90%, $R_L = 50\Omega$, $I_{OUT} = \pm 2mA$ $C_{LOAD} = 1pF$		0.95		mA/ns
DYNAMIC CHARACTERISTICS Propagation Delay Time Propagation Delay Time Delay Time	t_{PDH} , $V_{OD} = 200mV$ t_{PDL} , $V_{OD} = 200mV$ Sample-to-Hold Hold-to-Sample		2.2		ns
			2.15		ns
			3.8		ns
			3.0		ns

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DICE INFORMATION



SHC615 DIE TOPOGRAPHY

DIE PAD	FUNCTION
1	I_O Adjust
2	OTA-Emitter
3	OTA-Base
4	C_{HOLD}
5	-5V Supply, Analog
6	-5V Supply, Digital
7	Hold Control
8	Ground
9	S/H In+
10	S/H In-
11	I_{OUT} OTA-Collector
12	+5V Supply, Analog
13	+5V Supply, Digital

Substrate Bias: Negative Supply.

Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

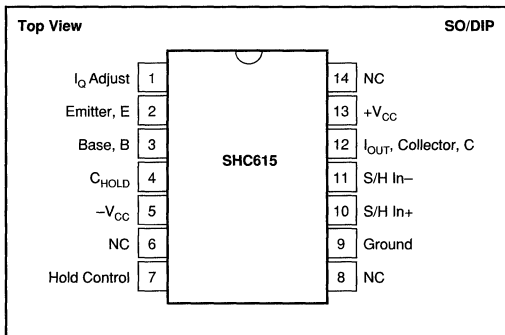
	MILS (0.001")	MILLIMETERS
Die Size	73 x 81, ± 5	1.86 x 2.06, ± 0.13
Die Thickness	14, ± 1	0.55, ± 0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, -0.0	0.0005, +0.0013, -0.0
Gold	0.30, ± 0.05	0.0076, ± 0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	$\pm 6VDC$
Input Voltage ⁽¹⁾	$\pm V_{CC} \pm 0.7V$
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Hold Control	-0.5V to $+V_{CC} + 0.7V$

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

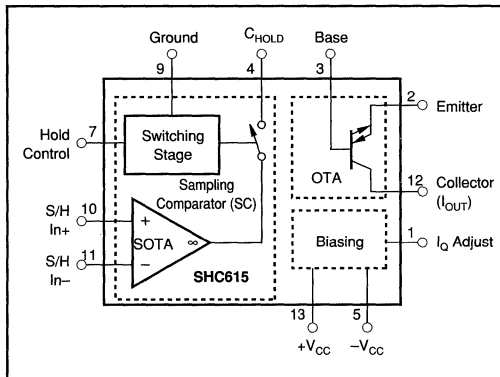
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SHC615AP	Plastic 14-Pin DIP	010
SHC615AU	SO 14-Pin Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
SHC615AP	Plastic 14-Pin DIP	-40°C to +85°C
SHC615AU	SO 14-Pin Surface Mount	-40°C to +85°C

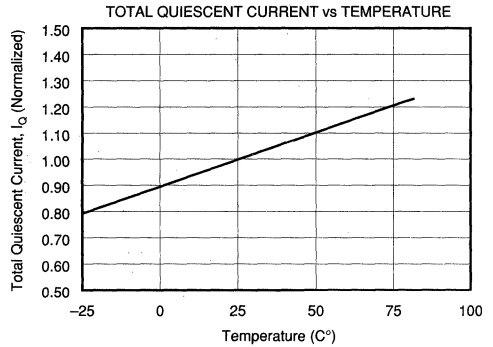
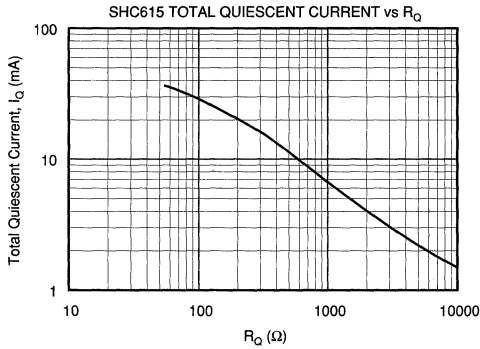
BLOCK DIAGRAM



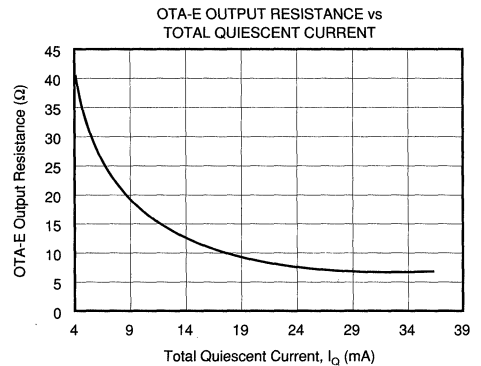
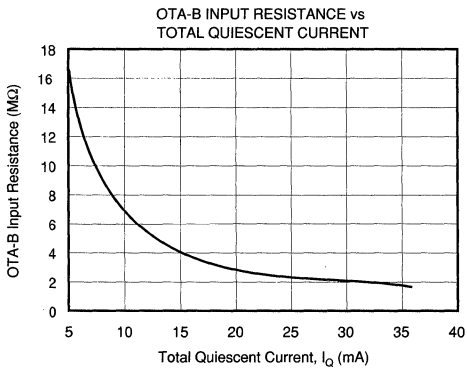
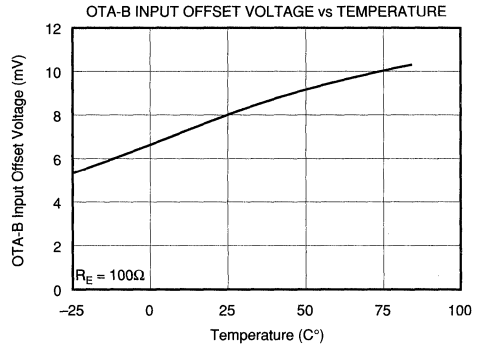
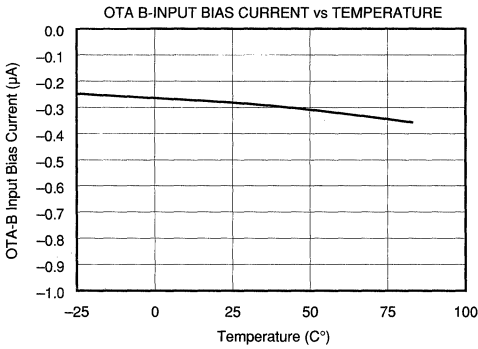
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TYPICAL PERFORMANCE CURVES

$R_O = 300\Omega$, $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 5\text{V}$ unless otherwise noted.



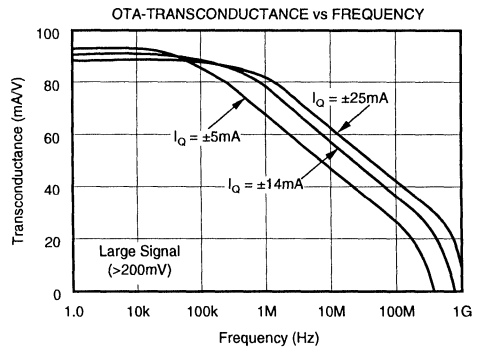
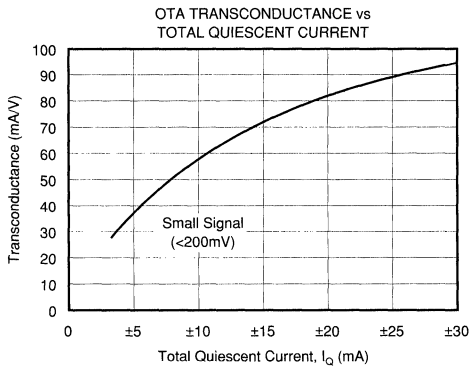
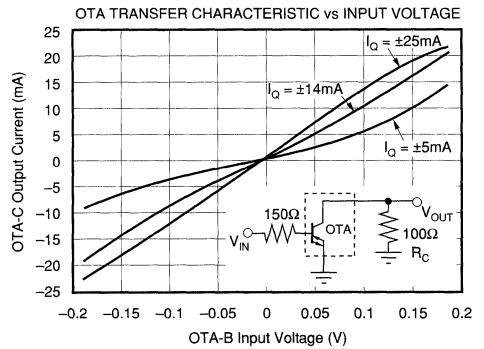
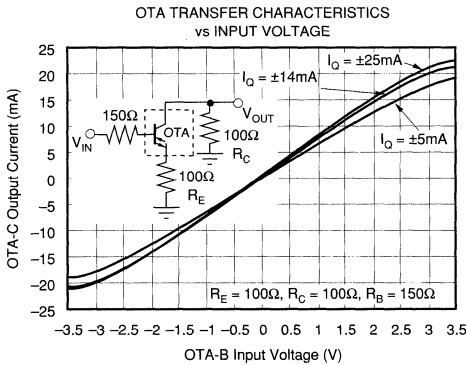
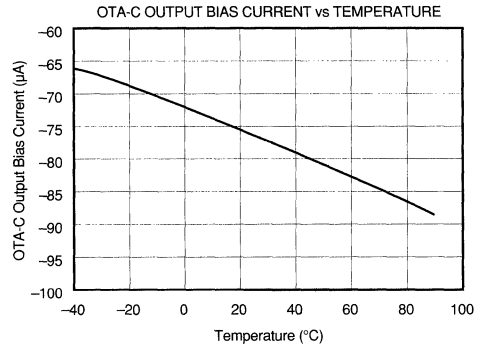
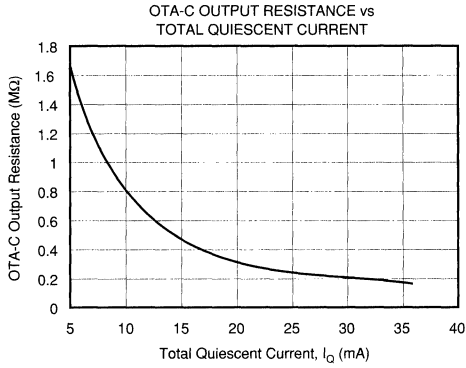
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER



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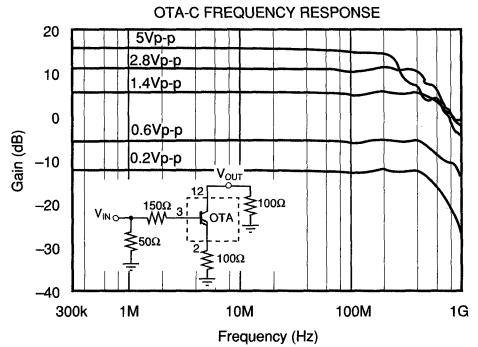
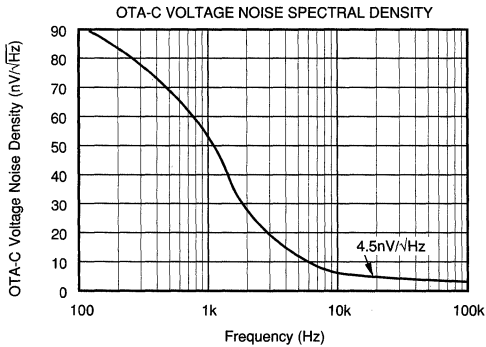
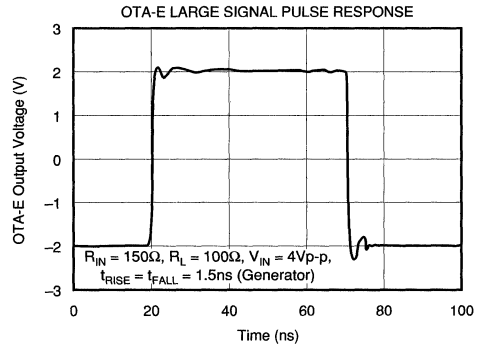
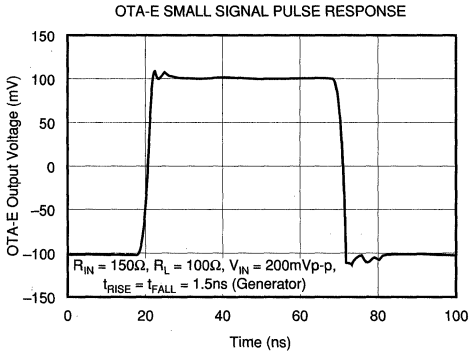
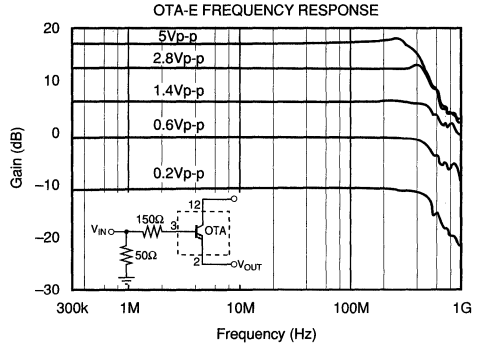
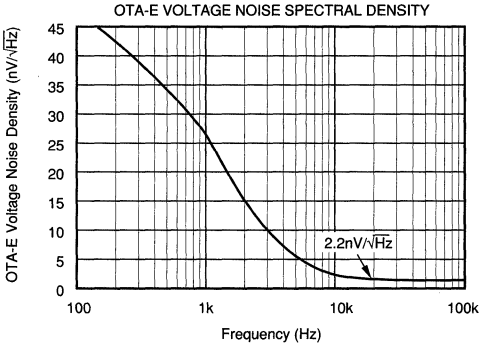
SHC615

SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES (CONT)

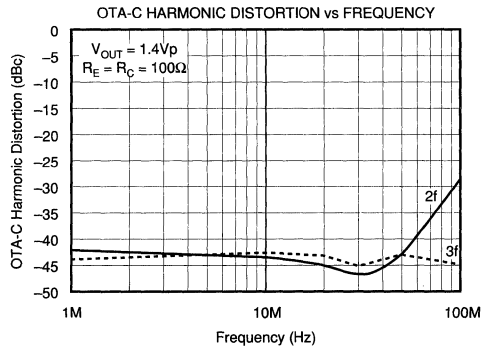
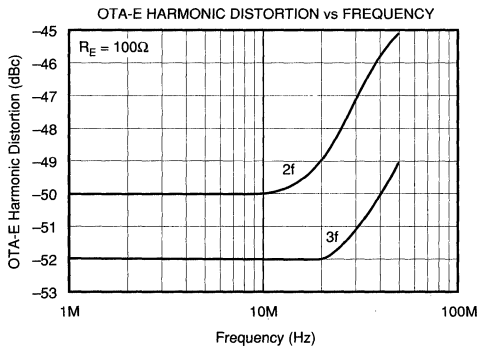
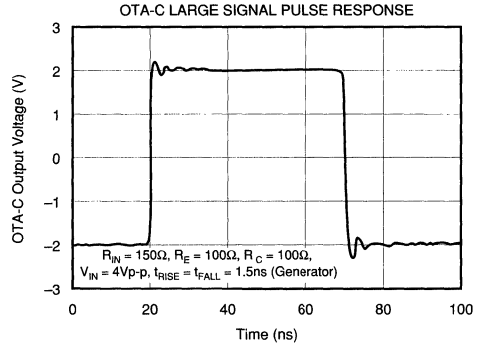
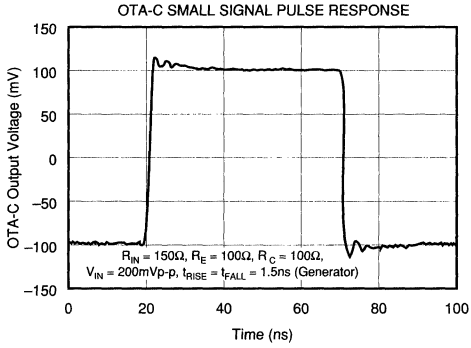
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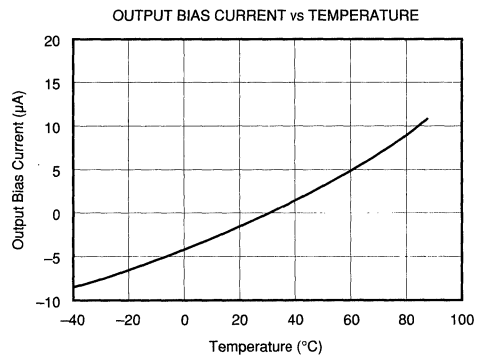
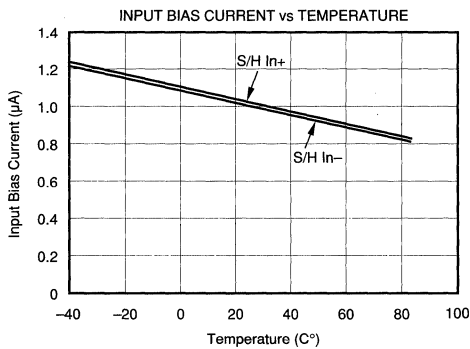
Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

$R_o = 300\Omega$, $T_A = +25^\circ\text{C}$, $V_{oc} = \pm 5\text{V}$ unless otherwise noted.



SAMPLING COMPARATOR



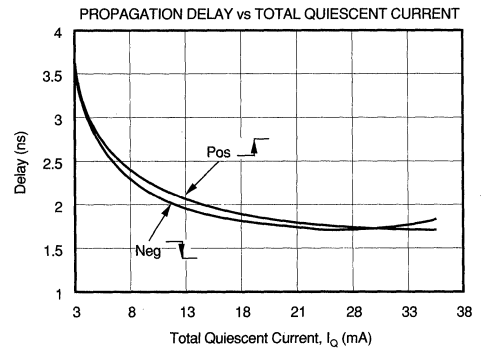
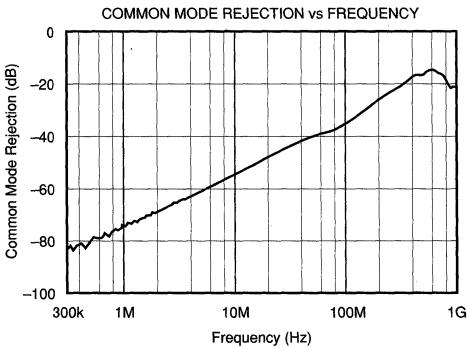
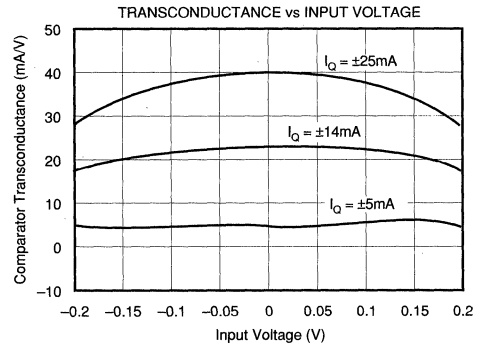
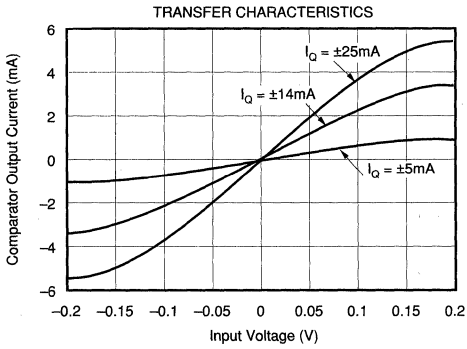
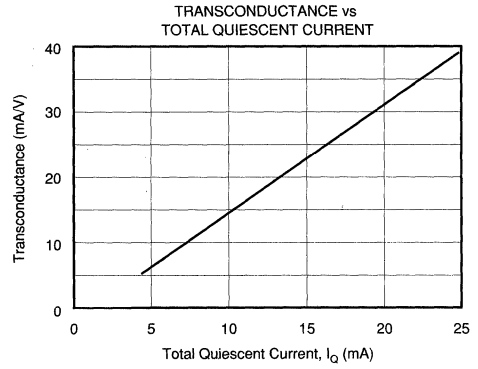
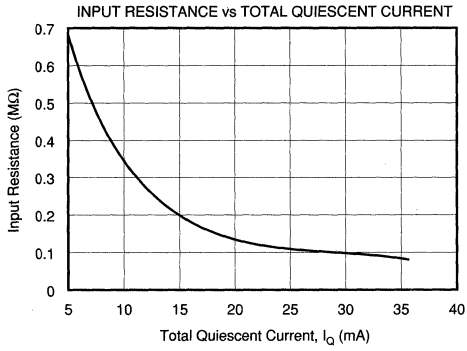
SHC615

SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES (CONT)

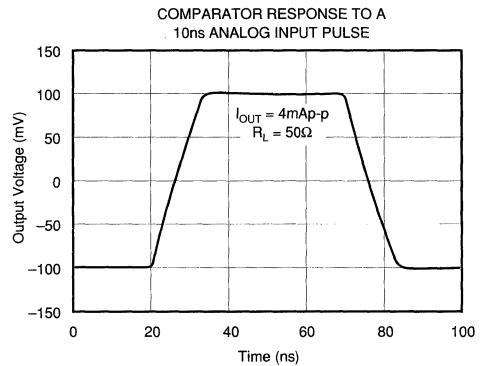
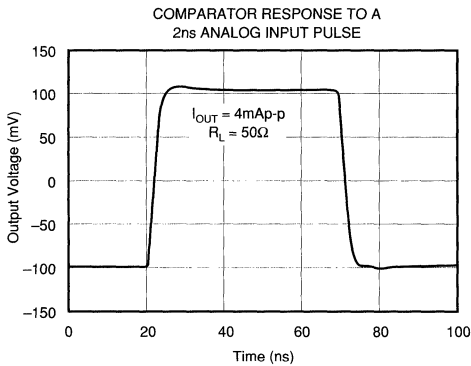
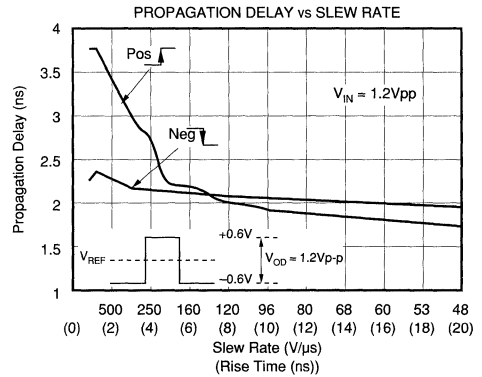
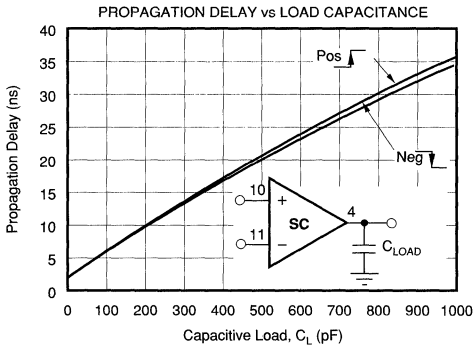
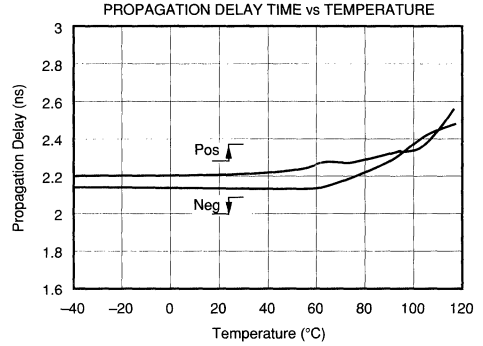
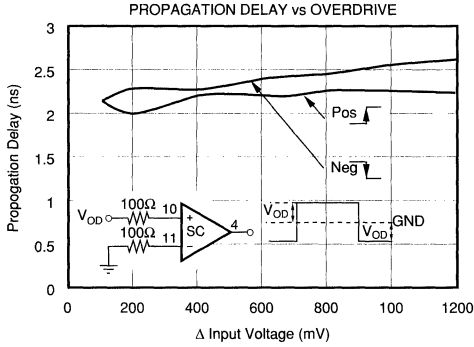
$R_O = 300\Omega$, $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 5\text{V}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

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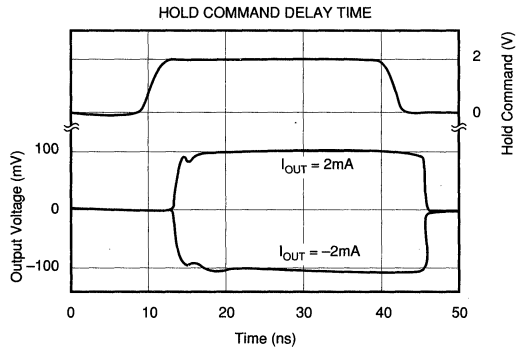
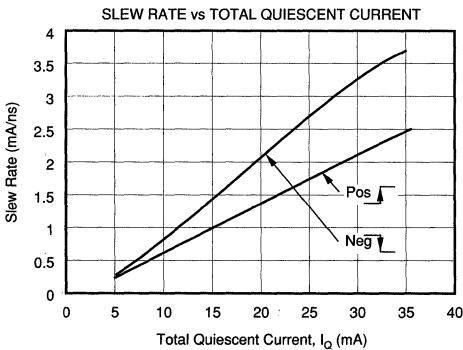
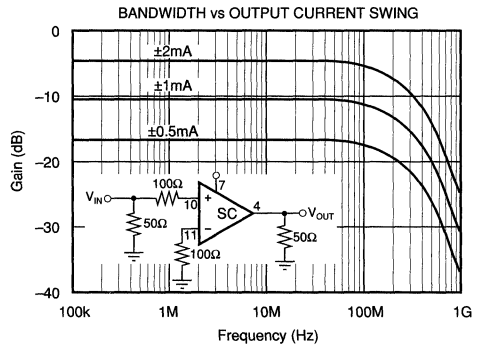
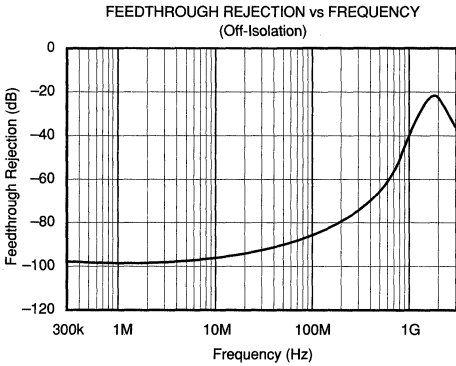
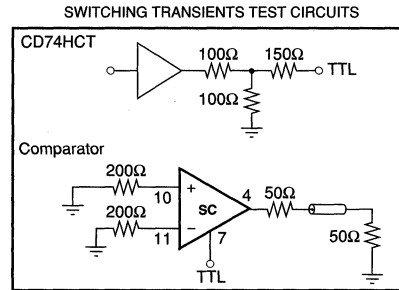
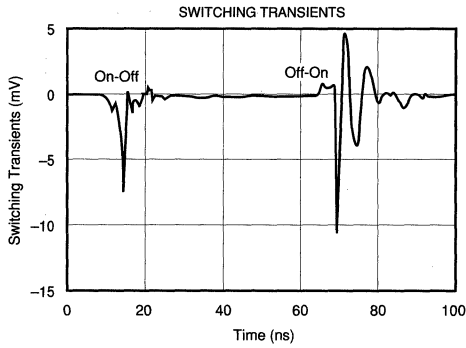
SHC615

SPECIAL FUNCTIONS

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TYPICAL PERFORMANCE CURVES (CONT)

$R_o = 300\Omega$, $T_A = +25^\circ\text{C}$, $V_{CC} = \pm 5\text{V}$ unless otherwise noted.



DISCUSSION OF PERFORMANCE

The SHC615, which contains a wide-band Operational Transconductance Amplifier and a fast sampling comparator, represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wide-band video signals, it can also be used as a sample and hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or demodulator or modulator for pulse code transmission systems. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator set a new standard for high-speed sampling applications.

Both can be used as stand-alone circuits or combined to create more complex signal processing stages like sample and hold amplifiers. The SHC615 simplifies the design of input amplifiers with high hum suppression, clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals, signal processing stages for the energy and peak value of small and fast nanoseconds pulses, and eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter.

An external resistor, R_Q , allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of both the OTA and comparator sections and controls the bandwidth and AC behavior as well as the transconductance of both sections. Besides the quiescent current setting feature, the Proportional-to-Absolute-Temperature (PTAT) supply increases the quiescent current vs temperature and keeps it constant over a wide range of input voltages. This variation holds the transconductance g_m of the OTA and comparator relatively constant vs temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω , giving a nominal quiescent current at $\pm 14\text{mA}$. The circuit can be totally switched-off with a current flowing into Pin 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

SECTION AND OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-based OTA can be viewed as a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor, also, is a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of $0.3\mu\text{A}$, a low-impedance input/

output (emitter), and the high-impedance current output (collector).

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to $1\text{M}\Omega$ and the open-loop gain to typical 96dB. Both features improve the OTAs linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams the emitter is connected to GND and then the collector current is determined by the product voltage between base and emitter times the transconductance. In application circuits (Figure 2b.), a resistor R_E between emitter and GND is used to set the OTA transfer characteristics. The following formulas describe the most important relationships. r_E is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above $\pm 5\text{mA}$, collector current, I_C , will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \quad R_E = \frac{V_{IN}}{I_C} - r_E$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high pass filter enhancing the high frequency gain. Other cases may require a RC compensation network parallel to R_E to optimize the high-frequency response. The full power bandwidth measured at the emitter achieves 620MHz. The frequency response of the collector is directly related to the resistor's value between collector and GND; it decreases with increasing resistor values, because it forms a low-pass network with the OTA C-output capacitance.

Figure 1 shows a simplified block and circuit diagram of the SHC615 OTA. Both the emitter and the collector outputs offer a drive capability of $\pm 20\text{mA}$ for driving low impedance lines or inputs. Connecting the collector to the emitter in a direct-feedback buffer configuration increases the drive capability to $\pm 40\text{mA}$. The emitter output is not current-limited or-protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

While the OTA's function and labeling looks similar to that of transistors, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) Due to the PTAT biasing characteristic the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and, 7) The output current is zero for zero differential input voltages. AC inputs centered at zero produce an output current centered at zero.

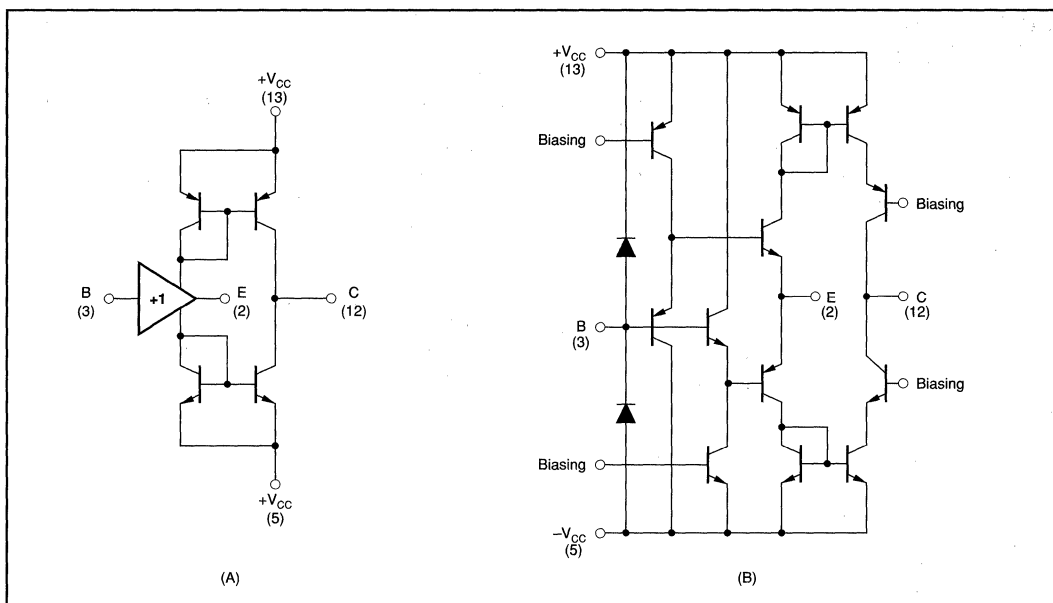


FIGURE 1. a) Simplified Block; and, b) Circuit Diagram of the OTA Section.

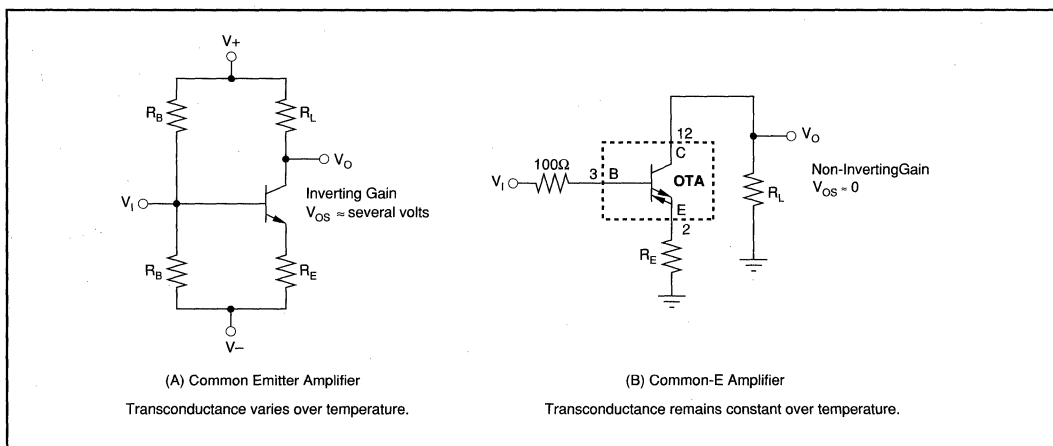


FIGURE 2. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the SHC615.

BASIC APPLICATIONS CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C (See Figures 2, 3 and 4). Figure 2 shows the OTA connected as

a Common-E amplifier which is equivalent to a common emitter transistor amplifier. Input and output can be ground referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting.

Figure 4 shows the common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier like BUF600 in series.

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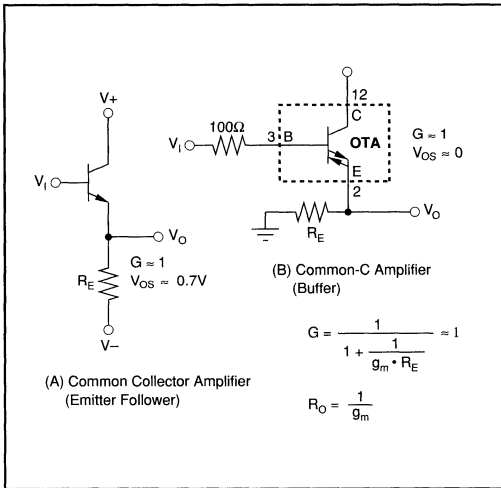


FIGURE 3. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the SHC615.

SAMPLING COMPARATOR

The SHC615 sampling comparator features a very short 2.2ns propagation delay and utilizes a new switching circuit architecture to achieve new levels of high-speed precision.

It provides high impedance inverting and non-inverting inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This is similar to the low or high status of a conventional comparator. The current source output features high output impedance, output bias compensation, and is optimized for charging a capacitor in DC restoration, ns-second integrators, peak detectors and S/H circuits. The typical comparator output current is $\pm 4\text{mA}$ and the output bias current is minimized to typically $4\mu\text{A}$ in the sampling mode.

This innovative circuit achieves the slew rate representatives of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the SHC615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching is 40fc.

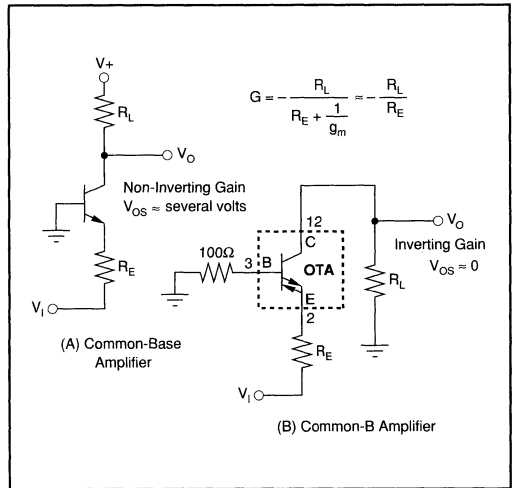


FIGURE 4. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the SHC615.

The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset (V)} = \frac{\text{Charge (pC)}}{C_H \text{ Total (pF)}}$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With a TTL logic high, the comparator is active, compares the two input voltages with each other and varies the output current accordingly. With a TTL logic low, the comparator output is switched off.

APPLICATION INFORMATION

The SHC615 operates from $\pm 5\text{V}$ power supplies ($\pm 6\text{V}$ maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the SHC615 are protected with internal diode clamps as shown in Figure 1. These protection diodes can safely conduct 10mA, continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

BASIC CONNECTIONS

Figure 6 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See “Circuit Layout” at the end of the applications discussion for further suggestions on layout.

SPECIAL FUNCTIONS 7 SHC615

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If the high speed TTL-hold command signal goes negative due to reflections for AC-coupling, the hold control input must be protected by an external reverse bias diode to ground as shown in Figure 6.

CIRCUIT LAYOUT

The high-frequency performance of the SHC615 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute requirements. Oscillations, ringing, poor bandwidth, poor settling, and peaking are all typical problems that

plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2 μ F); parallel 470pF and/or 10nF ceramic chip capacitors may be added if desired. Surface mount types are recommended because of their low lead inductance. Supply bypassing is extremely critical at high frequencies and when driving high current loads.
- PC board traces for power lines should be wide to reduce impedance or inductance.

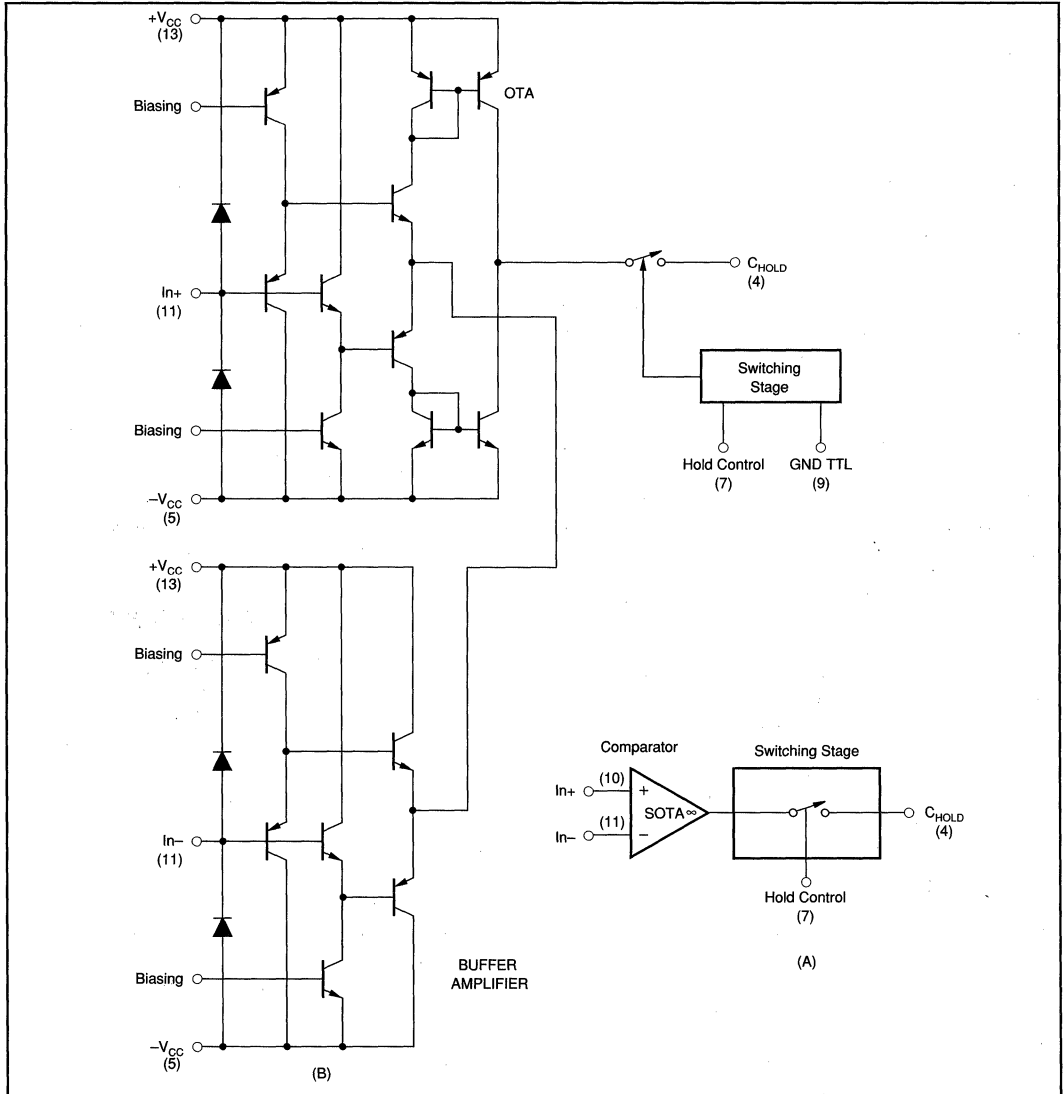


FIGURE 5. a) Simplified Block Diagram; and, b) Circuit Diagram of the Sampling Comparator which Includes the Sampling Operational Transconductance Amplifier (SOTA) and the Switching Stage.

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- Make short, low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that a low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.
- Sockets are not recommended since they add significant inductance and parasitic capacitance. If sockets must be used, consider using zero-profile sockets.
- Use low-inductance, surface-mount components. Circuits using all surface-mount components with the SHC615 will offer the best AC performance.
- A resistor of 100 to 250 Ω in series with the high-impedance inputs is recommended to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Terminate transmission line loads. Unterminated lines, such as box cables, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- Protect the hold control input with an external diode if necessary.

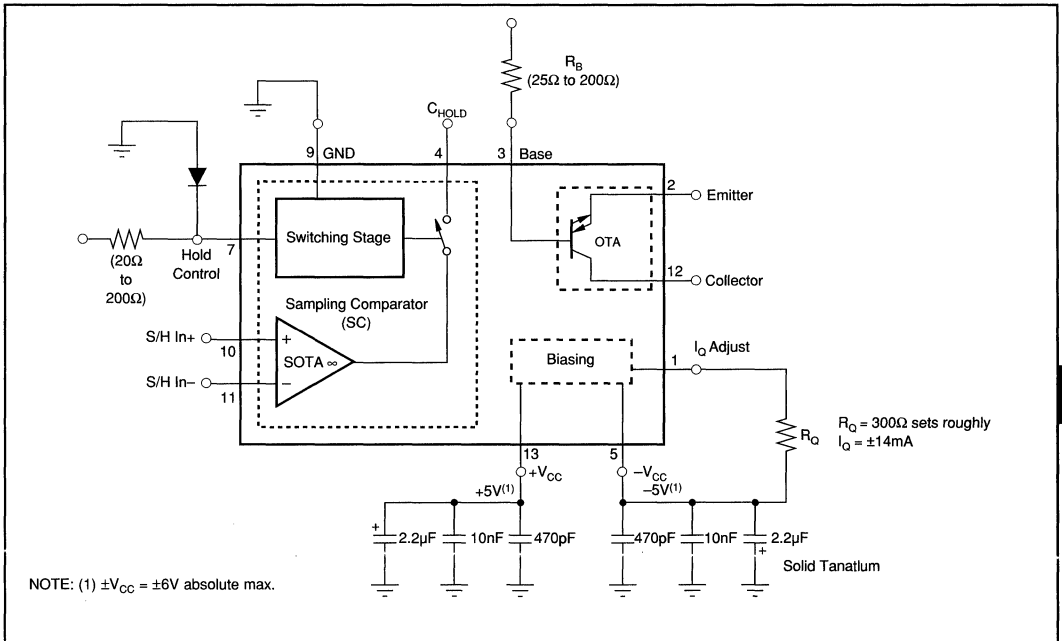


FIGURE 6. Basic Connections

TYPICAL APPLICATIONS

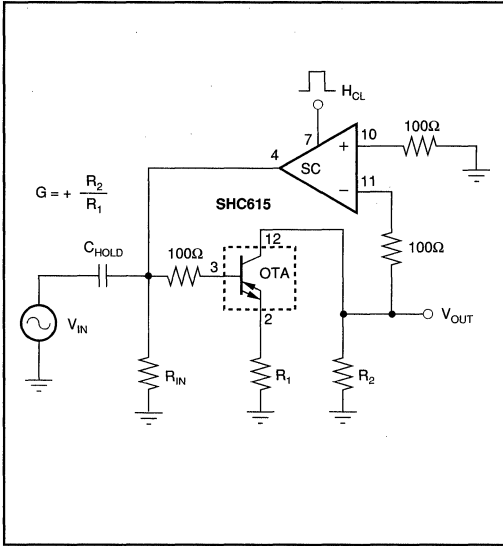


FIGURE 7. Complete DC Restoration System.

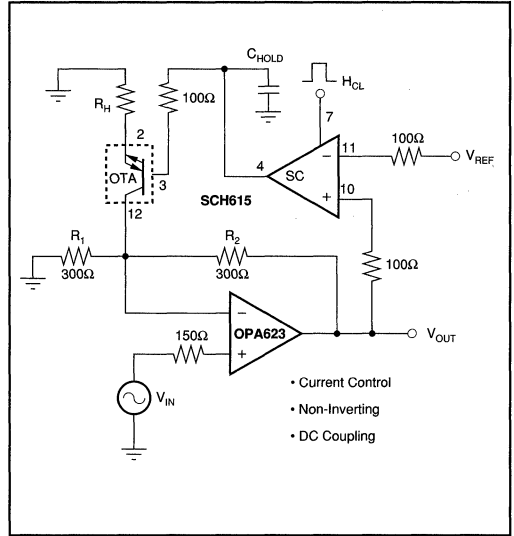


FIGURE 9. Clamped Video/RF Amplifier.

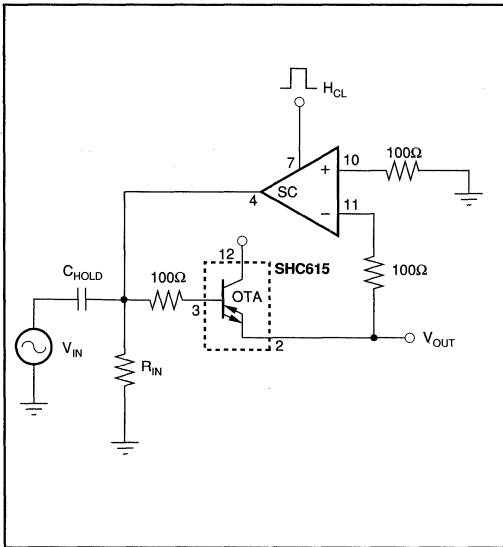


FIGURE 8. DC Restoration of a Buffer Amplifier.

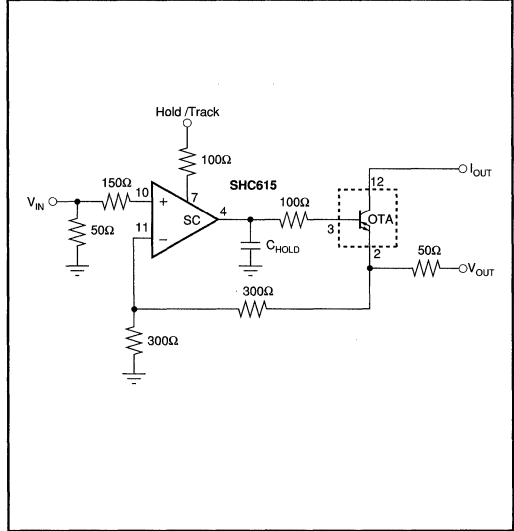


FIGURE 10. Sample/Hold Amplifier.

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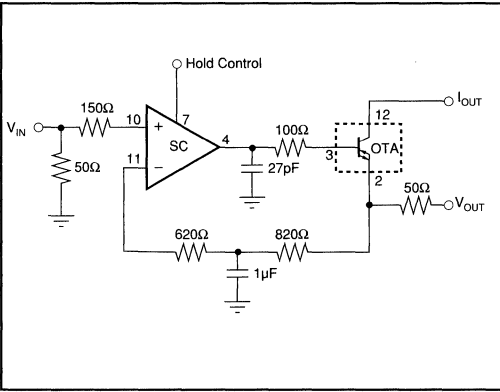


FIGURE 11. Integrator for ns-Pulses.

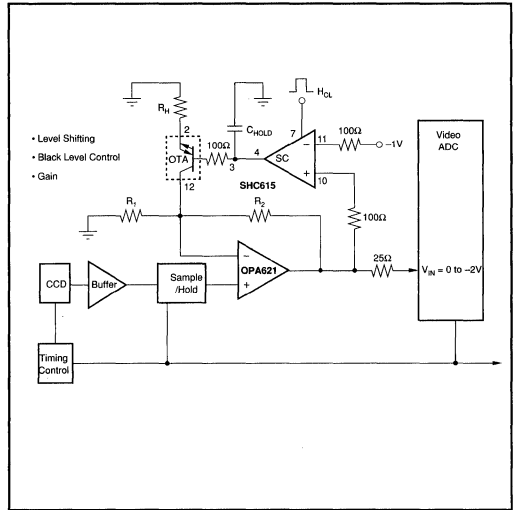


FIGURE 13. CCD Analog Front-End.

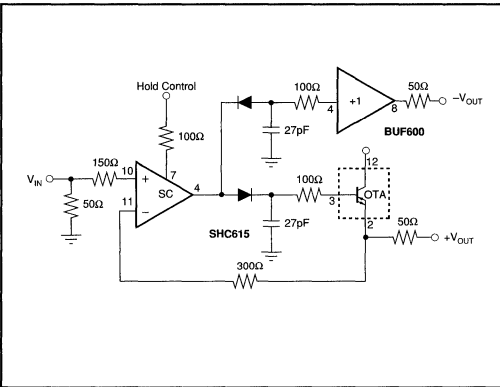


FIGURE 12. Fast Pulse Peak Detector.

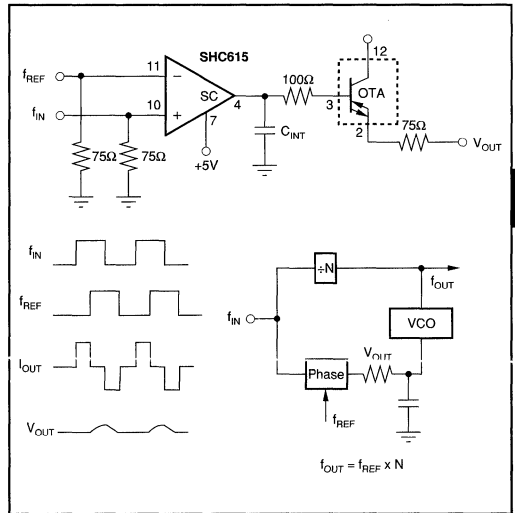


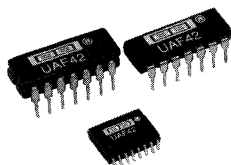
FIGURE 14. Phase Detector For Fast PLL-Systems.

SHC615

7

SPECIAL FUNCTIONS

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UAF42

UNIVERSAL ACTIVE FILTER

FEATURES

- VERSATILE—
LOW-PASS, HIGH-PASS
BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q —
INCLUDES ON CHIP 1000pF $\pm 0.5\%$
CAPACITORS

APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

DESCRIPTION

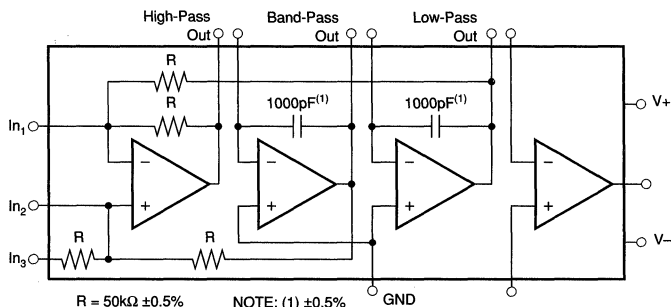
The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other

three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and ceramic packages, and SOL-16 surface-mount packages, specified for the -25°C to $+85^{\circ}\text{C}$ temperature range.



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SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS	UAF42AP, AU			UAF42AG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FILTER PERFORMANCE								
Frequency Range, f_n	$f = 1\text{kHz}$		0 to 100		*			kHz
Frequency Accuracy vs Temperature			0.01	1	*		2	%
Maximum Q			400		*			%/°C
Maximum (Q • Frequency) Product			500		*			—
Q vs Temperature	$(f_o \cdot Q) < 10^4$		0.01		*			kHz
	$(f_o \cdot Q) < 10^5$		0.025		*			%/°C
Q Repeatability	$(f_o \cdot Q) < 10^5$		2		*			%
Offset Voltage, Low-Pass Output				± 5			*	mV
Resistor Accuracy			0.5	1%	*		*	%
OFFSET VOLTAGE⁽¹⁾								
Input Offset Voltage			± 0.5	± 5		*	*	mV
vs Temperature			± 3		*			$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 6$ to $\pm 18\text{V}$	80	96		*			dB
INPUT BIAS CURRENT⁽¹⁾								
Input Bias Current	$V_{CM} = 0\text{V}$		10	50		*	*	pA
Input Offset Current	$V_{CM} = 0\text{V}$		5			*		pA
NOISE								
Input Voltage Noise						*		nV/ $\sqrt{\text{Hz}}$
Noise Density: $f = 10\text{Hz}$			25			*		nV/ $\sqrt{\text{Hz}}$
$f = 10\text{kHz}$			10			*		$\mu\text{Vp-p}$
Voltage Noise: BW = 0.1 to 10Hz			2			*		fA/ $\sqrt{\text{Hz}}$
Input Bias Current Noise						*		
Noise Density: $f = 10\text{kHz}$			2			*		
INPUT VOLTAGE RANGE⁽¹⁾								
Common-Mode Input Range			± 11.5			*		V
Common-Mode Rejection	$V_{CM} = \pm 10\text{V}$	80	96		*			dB
INPUT IMPEDANCE⁽¹⁾								
Differential			$10^{13} \parallel 2$			*		$\Omega \parallel \text{pF}$
Common-Mode			$10^{13} \parallel 6$			*		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN⁽¹⁾								
Open-Loop Voltage Gain	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	90	126		*	*		dB
FREQUENCY RESPONSE⁽¹⁾								
Slew Rate			10			*		V/ μs
Gain-Bandwidth Product	$G = +1$		4			*		MHz
Total Harmonic Distortion	$G = +1$, $f = 1\text{kHz}$		0.0004			*		%
OUTPUT⁽¹⁾								
Voltage Output	$R_L = 2\text{k}\Omega$	+11	+11.5		*	*		V
Short Circuit Current			± 25		*	*		mA
POWER SUPPLY								
Specified Operating Voltage			± 15		*	*		V
Operating Voltage Range		± 6		± 18	*	*	*	V
Current			± 6	± 7	*	*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*	*	*	°C
Operating		-25		+85	-55		+125	°C
Storage		-40		+125	-65		+150	°C
Thermal Resistance, θ_{JA}			100			*		°C/W

* Same as specification for UAF42AP.

NOTES: (1) Specifications apply to uncommitted op amp, A_4 . The three op amps forming the filter are identical to A_4 but are tested as a complete filter.

UAF42

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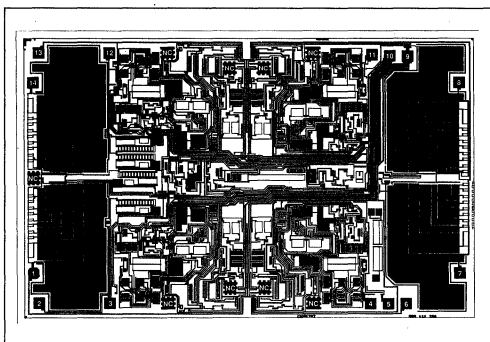
SPECIAL FUNCTIONS

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DICE INFORMATION



UAF42 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Low Pass V_O	7	Bandpass V_O
2	V_{IN3}	8	Frequency Adj ₁
3	V_{IN2}	9	V-
4	Aux. Op Amp, +In	10	V+
5	Aux. Op Amp, -In	11	Ground
6	Aux. Op Amp, V_O	12	V_{IN1}
		13	High-Pass V_O
		14	Frequency Adj ₂

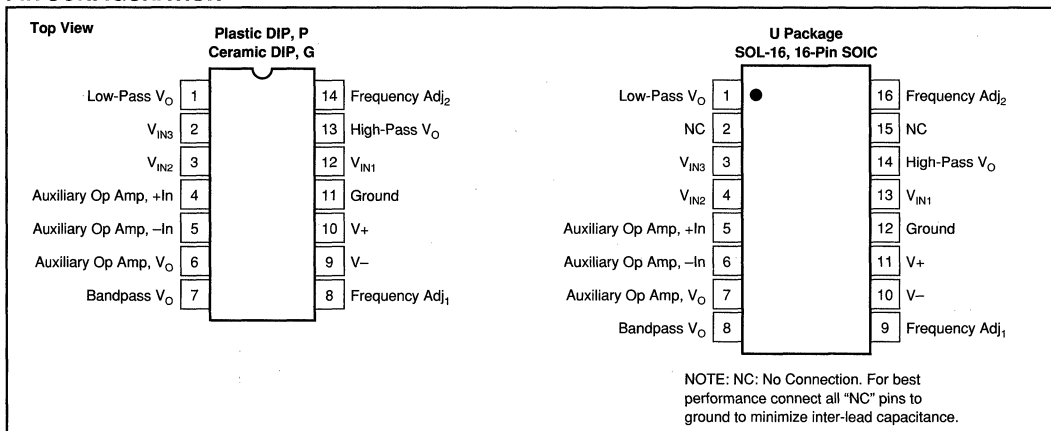
NC: No Connection.

Substrate Bias: Electrically connected to V- supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	205 x 130 ±5	5.21 x 3.30 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	± V_S ±0.7V
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP, P; SOIC, U	-40°C to +85°C
Ceramic DIP, G	-55°C to +125°C
Storage Temperature:	
Plastic DIP, P; SOIC, U	-40°C to +125°C
Ceramic DIP, G	-65°C to +150°C
Junction Temperature:	
Plastic DIP, P; SOIC, U	+125°C
Ceramic DIP, G	+150°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
UAF42AP	Plastic 14-pin DIP	-25°C to +85°C
UAF42AG	Ceramic 14-pin DIP	-25°C to +85°C
UAF42AU	SOL-16	-25°C to +85°C

PACKAGING INFORMATION ⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
UAF42AP	Plastic 14-pin DIP	010
UAF42AG	Ceramic 14-pin DIP	163
UAF42AU	SOL-16	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

APPLICATIONS INFORMATION

The UAF42 is a monolithic implementation of the proven state-variable analog filter topology. Pin-compatible with the popular UAF41 Analog Filter, it provides several improvements.

Slew Rate of the UAF42 has been increased to 10V/μs versus 1.6V/μs for the UAF41. Frequency • Q product of the UAF42 has been improved, and the useful natural frequency extended by a factor of four to 100kHz. FET-input op amps on the UAF42 provide very low input bias current. The monolithic construction of the UAF42 provides lower cost and improved reliability.

DESIGN PROGRAM

Application Bulletin AB-035 and a computer-aided design program, available from Burr-Brown, make it easy to design and implement many kinds of active filters. The DOS-compatible program guides you through the design process and automatically calculates component values.

Low-pass, high-pass, band-pass and band-reject (notch) filters can be designed. The program supports the three most commonly used all-pole filter types: Butterworth, Chebyshev and Bessel. The less-familiar Inverse Chebyshev is also supported, providing a smooth passband response with ripple in the stop-band.

With each data entry, the program automatically calculates and displays filter performance. This allows a spreadsheet-like "what if" design approach. For example, you can quickly determine, by trial and error, how many poles are required for a desired attenuation in the stopband. Gain/phase plots may be viewed for any response type.

The basic building element of the most commonly used filter types is the second-order section. This section provides a complex-conjugate pair of poles. The natural frequency, ω_n , and Q of the pole pair determines the characteristic response of the section. The low-pass transfer function is

$$\frac{V_O(s)}{V_I(s)} = \frac{A_{LP}\omega_n^2}{s^2 + s\omega_n/Q + \omega_n^2} \quad (1)$$

The high-pass transfer function is

$$\frac{V_{HP}(s)}{V_I(s)} = \frac{A_{HP}s^2}{s^2 + s\omega_n/Q + \omega_n^2} \quad (2)$$

The band-pass transfer function is

$$\frac{V_{BP}(s)}{V_I(s)} = \frac{A_{BP}(\omega_n/Q) s}{s^2 + s\omega_n/Q + \omega_n^2} \quad (3)$$

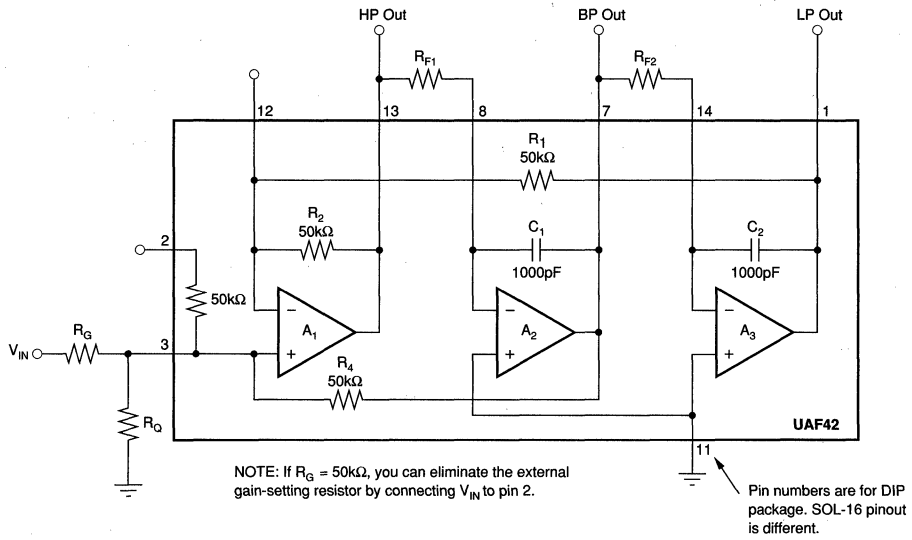
A band-reject response is obtained by summing the low-pass and high-pass outputs, yielding the transfer function

$$\frac{V_{BR}(s)}{V_I(s)} = \frac{A_{BR}(s^2 + \omega_n^2)}{s^2 + s\omega_n/Q + \omega_n^2} \quad (4)$$

The most commonly used filter types are formed with one or more cascaded second-order sections. Each section is designed for ω_n and Q according to the filter type (Butterworth, Bessel, Chebyshev, etc.) and cutoff frequency. While tabulated data can be found in virtually any filter design text, the design program eliminates this tedious procedure.

Second-order sections may be non-inverting (Figure 1) or inverting (Figure 2). Design equations for these two basic configurations are shown for reference. The design program solves these equations, providing complete results, including component values.

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Design Equations

$$1. \omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

$$2. Q = \frac{1 + \frac{R_4 (R_G + R_O)}{R_G R_O}}{1 + \frac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2} \right)^{1/2}$$

$$3. QA_{LP} = QA_{HP} \left(\frac{R_1}{R_2} \right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2} \right)^{1/2}$$

$$4. A_{LP} = \frac{1 + \frac{R_1}{R_2}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_O} + \frac{1}{R_4} \right)}$$

$$5. A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \frac{R_2}{R_1}}{R_G \left(\frac{1}{R_G} + \frac{1}{R_O} + \frac{1}{R_4} \right)}$$

$$6. A_{BP} = \frac{R_4}{R_G}$$

FIGURE 1. Non-Inverting Pole-Pair.

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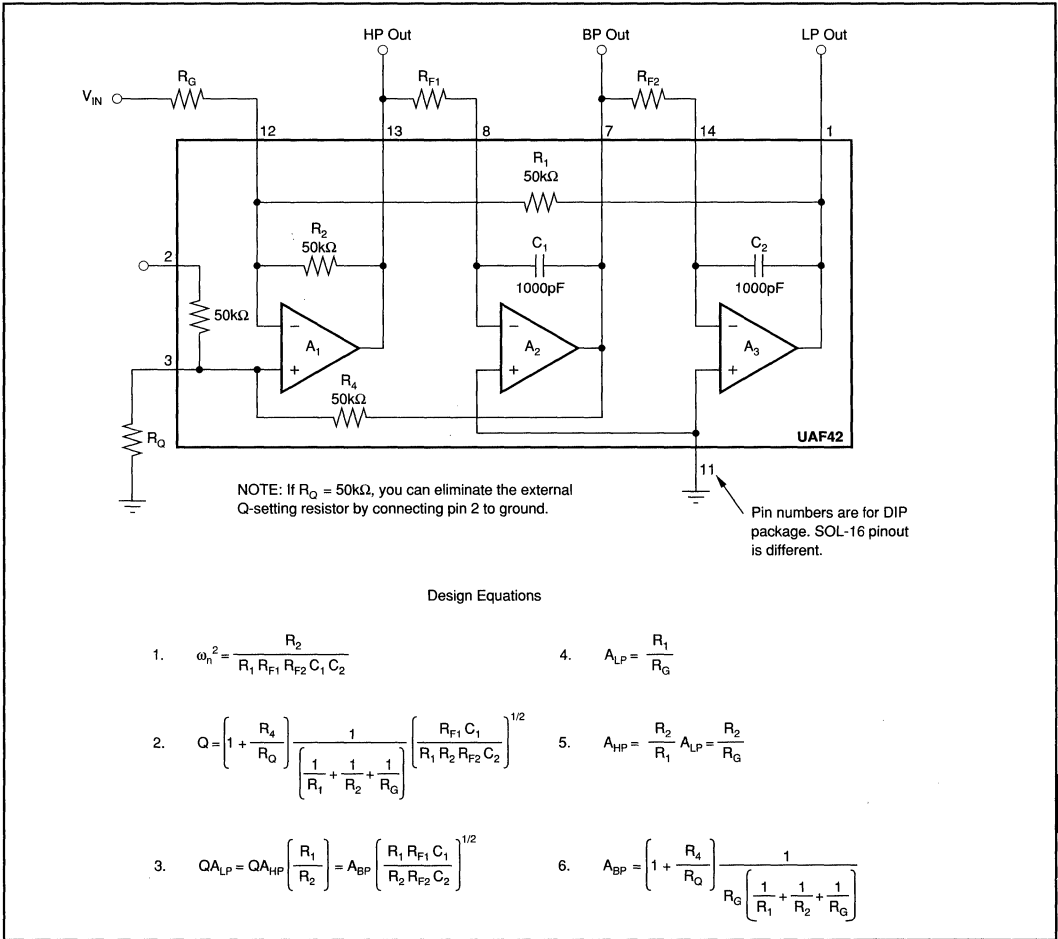
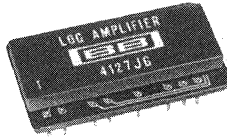


FIGURE 2. Inverting Pole-Pair.

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4127

LOGARITHMIC AMPLIFIER

FEATURES

- ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY
- WIDE INPUT DYNAMIC RANGE
6 Decades of Current
4 Decades of Voltage
- VERSATILE
Log, Antilog, and Log Ratio Capability

DESCRIPTION

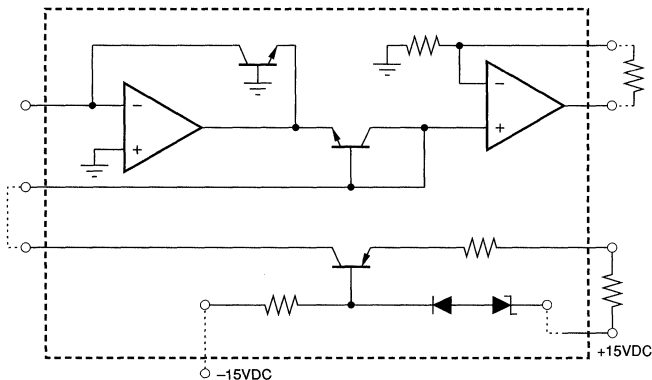
Packaged in a ceramic double wide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input

current and four decades of input voltage. In addition, a current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost, the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to $+70^{\circ}\text{C}$.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low cost solution to many signal processing problems.



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SPECIFICATIONS

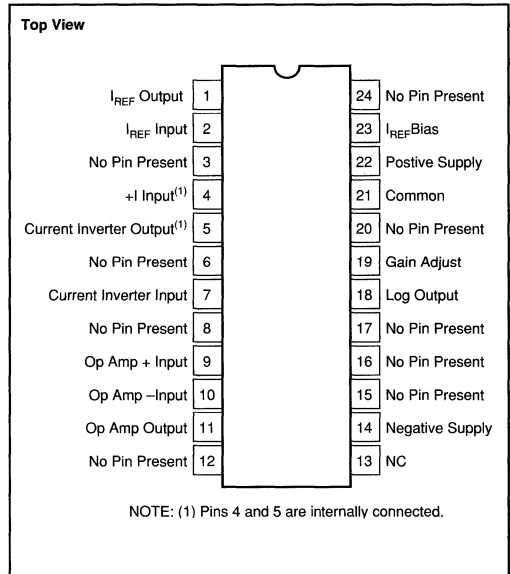
ELECTRICAL

Typical Specifications at +25°C with rated supplies, unless otherwise noted.

MODEL	4127KG	4127JG
ACCURACY⁽¹⁾, % of FSR Current Source Input: 1nA to 1mA Voltage Input: 1mV to 10V	0.5% max 0.5% max	1% max 1% max
INPUT Current Source Input, Pin 4 Current Source Input, Pin 7 Reference Current Input, Pin 2 Absolute Maximum Inputs	+1nA to +1mA -1nA to -1mA +1μA to +1mA ±10mA or ±Supply Volts	
OUTPUT Voltage Current Impedance	±10V ±5mA 10Ω	
FREQUENCY RESPONSE -3dB Small Signal at Current Input of 100μA of 10μA of 1μA of 100nA of 10nA Step Response to within ±1% of Final Value (I _i = 1μA, A = 5)	90kHz 50kHz 5kHz 250Hz 80Hz 10ms	
STABILITY Scale Factor Drift (ΔA/°C) Reference Current Drift (ΔI _r /°C) Input Offset Current Drift (ΔI _o /°C) Input Offset Voltage Drift Accuracy vs Supply Variation Reference Current Input Offset Voltage Input Noise - Current Input Input Noise - Voltage Input	±0.0005A/°C ±0.001 I _r /°C for I _r ≥ 1μA ±0.003 I _r /°C for 400nA < I _r < 1μA 10pA at +25°C, Doubles Every 10°C ±10μV/°C ±0.001I _r /V ±300μV/V 1pA, rms, 10Hz to 10kHz 10μA, rms, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS Input Offset Voltage Input Bias Current Input Impedance Large Signal Voltage Gain Output Current	5mV 40nA 1MΩ 85dB 5mA	
TEMPERATURE RANGE Specification Operating Storage	0°C to +60°C -10°C to +70°C -55°C to +125°C	
POWER SUPPLY REQUIREMENTS Rated Supply Voltages Supply Voltage Range Supply Current Drain at Quiescent, max at Full Load, max	±15VDC ±14VDC to ±16VDC ±20mA ±26mA	

NOTE: (1) Log conformity at 25°C.

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
4127KG	24-Pin	075
4127JG	24-Pin	075

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

4127

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SPECIAL FUNCTIONS

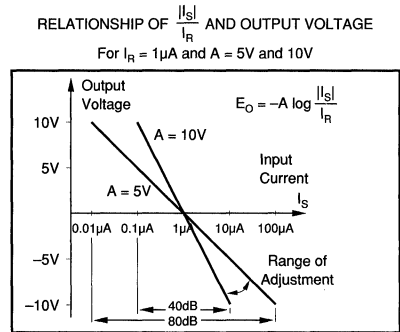
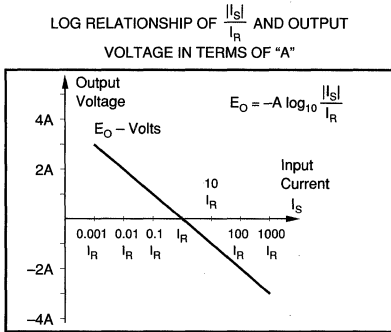
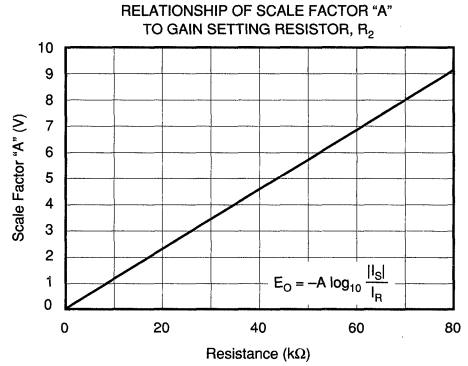
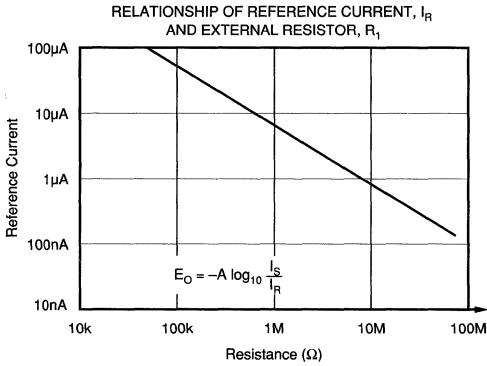
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TYPICAL PERFORMANCE CURVES

At +25°C with rated supplies, unless otherwise noted.



DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are

subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

THEORY OF OPERATION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic

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mic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1nA to 1mA, or input voltages from 1mV to 10V. Carefully matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

A functional diagram of the 4127 circuit is shown in Figure 1. In addition to the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range, good shielding practice must be followed. A current source input is, by definition, a high impedance source and is therefore subject to electrostatic pickup.

The input op amps, A₁ and A₃, have FET input stages for low noise and very-low input bias current. The op amp, A₁, will make the collector current of Q₁ equal to the signal input current I_S, and the collector current of Q₂ will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be:

$$V_{BE} \approx \frac{mKT}{q} \ln \frac{I_C}{I_L}$$

where: I_C = Collector current
 I_L = Reverse saturation current
 q, m, K = Constants
 T = Absolute temperature

$$\text{So } E_1 = -\frac{mKT_1}{q} \ln \frac{I_S}{I_{L1}} \text{ and } E_2 - E_1 = \frac{mKT_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q₁ and Q₂ are at the same temperature and have matched characteristics, then:

$$E_2 = \frac{mKT}{q} \left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L} \right]$$

$$E_2 = \frac{-mKT}{q} \ln \frac{I_S}{I_R}$$

The output op amp, A₂, provides a voltage gain of approximately (R_T + R₂)/R_T, and the value of (mKT)/q is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage, E_O, expressed as a log will be:

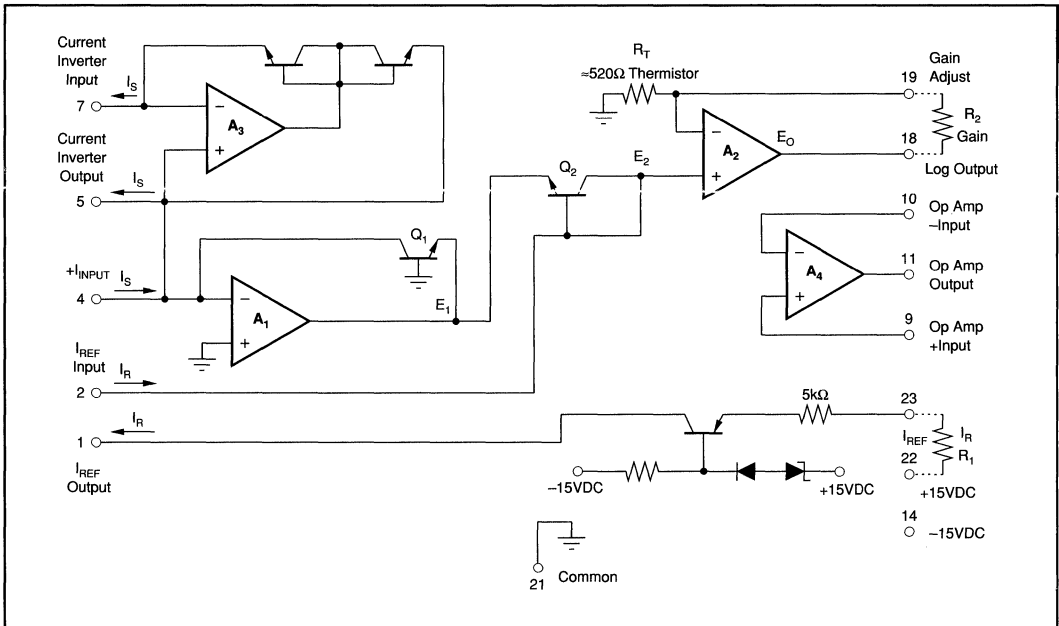


FIGURE 1. Functional Diagram.

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$$E_o = -A \log_{10} \frac{I_s}{I_R},$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T} (26\text{mV}) \frac{1}{0.434}, \quad R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". R_1 and R_2 must be trimmed to the desired values, but the approximate relationships are shown in Typical Performance Curves.

The relationship between the input current, I_s , and the output voltage, E_o , in terms of the externally adjusted parameters, I_R and "A", is illustrated in Typical Performance Curves. This relationship is, of course, restricted to values of I_s between 1nA and 1mA and output voltages of less than $\pm 10\text{V}$.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full $\pm 10\text{V}$ output range. Once an output range of $\pm 10\text{V}$ has been chosen, then "A" and I_R can be determined from the Min/Max of the input current, I_s .

$$E_o = -A \log \frac{I_s}{I_R}, \quad \text{where } I_{\text{MIN}} < I_s < I_{\text{MAX}}$$

The output range of $\pm 10\text{V}$ for an input range of I_{MIN} to I_{MAX} means that:

$$+10 = -A \log \frac{I_{\text{MIN}}}{I_R} \quad \text{and} \quad -10 = -A \log \frac{I_{\text{MAX}}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{\text{MAX}} + I_{\text{MIN}}}{I_R^2} = 0, \quad \text{or } I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{\text{MAX}}}{\sqrt{I_{\text{MAX}} I_{\text{MIN}}}}$$

In terms of the input current range for I_s , the values for I_R and A that will provide a full $\pm 10\text{V}$ output swing are:

$$I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}} \quad \text{and} \quad A = \frac{10}{\log \frac{I_{\text{MAX}}}{I_R}}$$

EXAMPLE

Assume that I_{MIN} is +10nA and I_{MAX} is +100 μA .

This is an 80dB range.

$$I_R = \sqrt{I_{\text{MAX}} I_{\text{MIN}}} = \sqrt{(10^{-4})(10^{-8})} = 10^{-6}, \quad \text{or } 1\mu\text{A}.$$

$$\frac{I_{\text{MAX}}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{\text{MAX}}}{I_R} = 2; \quad \text{So, } A = 5$$

For an I_R of 1 μA and A of 5,

$$E_o = -5 \log \frac{I_s}{1\mu\text{A}}$$

CONNECTION DIAGRAMS

Transfer function is $E_o = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current (see Figure 2).

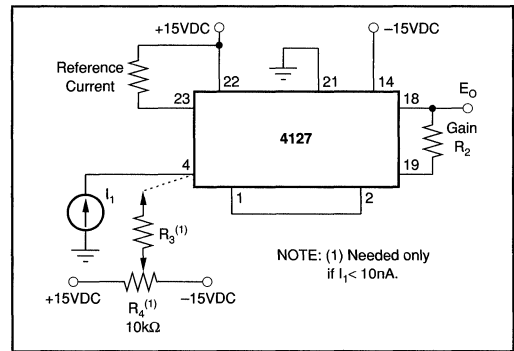


FIGURE 2. Transfer Function When I_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{\text{MAX}}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{\text{MIN}}| \geq 10\text{nA}$. Otherwise, apply $|I_1| = 1\text{nA}$, make $R_3 = 1\text{kM}\Omega$ and adjust R_4 for the proper output voltage. For R_3 , a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_o = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative

input current and I_R is the resistor-programmed internal reference current (see Figure 3).

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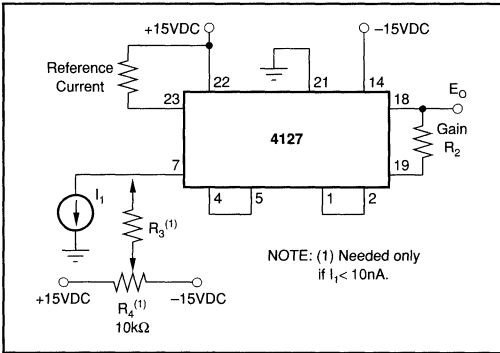


FIGURE 3. Transfer Function When I_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|I_1| = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{MAX}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1MIN}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1kM\Omega$ and adjust R_4 for the proper output voltage. For R_3 , a single resistor is recommended. A voltage divider network is difficult to use due to amplifier offset voltage.

Transfer function is $E_o = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current (see Figure 4).

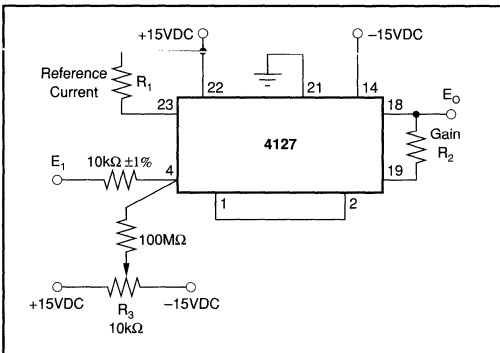


FIGURE 4. Transfer Function When E_1 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_o = 0$.
3. Apply $E_1 = E_{MAX}$, adjust R_2 for the proper output voltage.

4. Apply $E_1 = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_o = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current (see Figure 5).

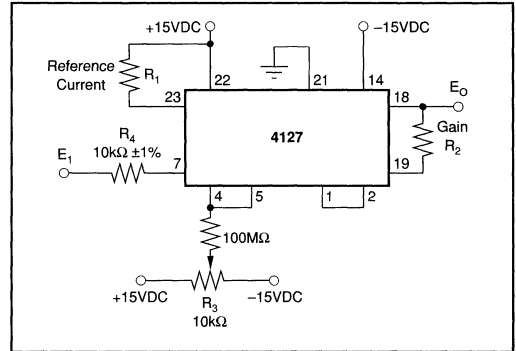


FIGURE 5. Transfer Function When E_1 is Negative.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_o = 0$.
3. Apply $|E_1| = E_{MAX}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{MIN}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_o = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA$, $|I_2| \geq 1\mu A$ (see Figure 6).

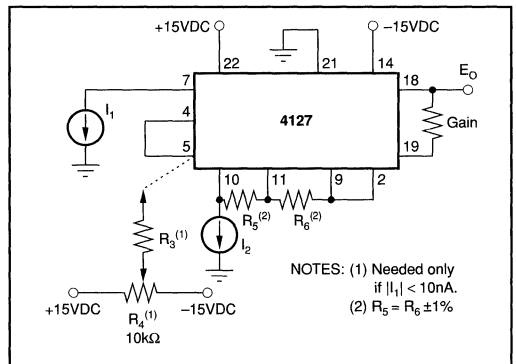


FIGURE 6. Transfer Function When I_1 and I_2 are Negative.

For Immediate Assistance, Contact Your Local Salesperson

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\text{ MIN}} \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^\circ\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

Transfer function is $E_o = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1\text{nA}$, $I_2 \geq 1\mu\text{A}$ (see Figure 7).

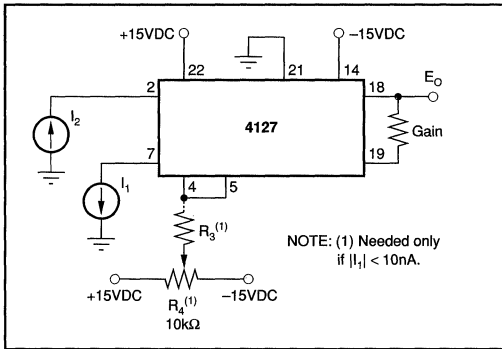


FIGURE 7. Transfer Function When I_1 is Negative, I_2 is Positive.

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $|I_{1\text{ MIN}}| \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^\circ\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

Transfer function is $E_o = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1\text{nA}$, $I_2 \geq 1\mu\text{A}$ (see Figure 8).

ADJUSTMENT PROCEDURE

1. Refer to Choosing the Optimum Scale Factor and Reference Current.
2. No further adjustment is necessary if $I_{1\text{ MIN}} \geq 10\text{nA}$, otherwise connect the R_3 and R_4 network, with $R_4 = 10\text{k}\Omega$ and $R_3 = 10^\circ\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the

range of $\pm 5\text{mV}$, it is not practical to use a T-network to replace R_3 .

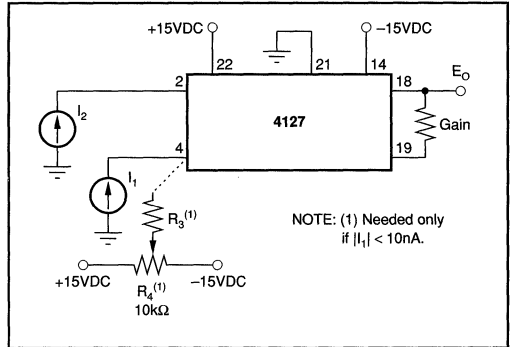


FIGURE 8. Transfer Function When I_1 and I_2 is Positive.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor, R_o , into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 9.

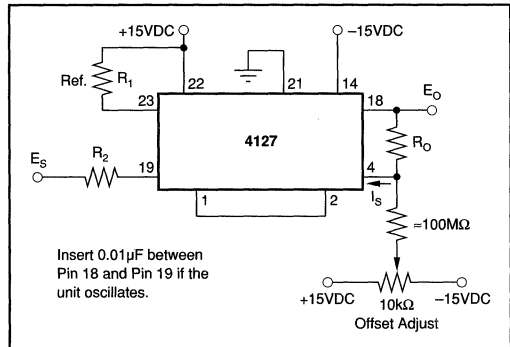


FIGURE 9. Antilog Operation.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A_2 must equal E_2 , so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, R_T \approx 520\Omega$$

Since the output is connected through R_o to pin 4, the current I_s will equal E_o/R_o and E_2 will be

$$E_2 = -\frac{mKT}{q} \ln \frac{E_o}{R_o I_R}$$

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Combining expressions for E_2 gives the relationship:

$$\frac{R_T}{R_T + R_2} E_s = - \frac{mKT}{q} \ln \frac{E_o}{R_o I_R}$$
$$- \frac{E_s}{A} = \log \frac{E_o}{R_o I_R}$$

where:

$$A \approx \frac{R_T + R_2}{R_T} (26\text{mV}) \frac{1}{0.434}$$
$$E_o = R_o I_R \text{ Antilog} - \frac{E_s}{A}$$

Setting R_o and I_R will set the scale factor. For example, an R_o of $1\text{M}\Omega$ and I_R of $1\mu\text{A}$ will give a scale factor of unity

and $E_o = \text{Antilog} - \frac{E_s}{A}$

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4302

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- VERSATILE
- SMALL PACKAGE: Dual-in-Line
- EASY TO USE

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just a multiplier/divider, the 4302 performs many analog circuit functions with a high degree of accuracy at a low total cost.

FUNCTIONS	ACCURACY
Multiply	±0.25%
Divide	±0.25%
Square	±0.03%
Square Root	±0.07%
Exponentiate	±0.15% (m = 5)
Roots	±0.2% (m = 0.2)
Sine θ	±0.5%
Cosine θ	±0.8%
Tan $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

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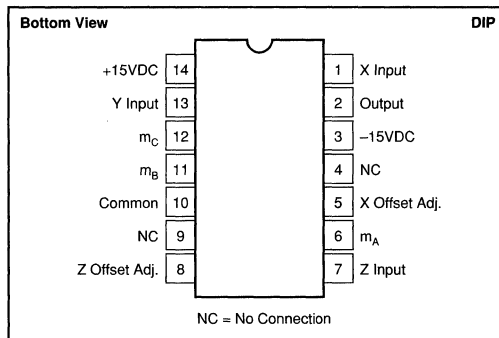
SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{VDC}$, unless otherwise noted.

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y \left[\frac{V_Z}{V_X} \right]^m$
RATED OUTPUT Voltage Current	+10.0V 5mA
INPUT Signal Range Absolute Maximum Impedance (X/Y/Z)	$0 \leq (V_X, V_Y, V_Z) \leq +10\text{V}$ $(V_X, V_Y, V_Z) \leq \pm 18\text{V}$ 100k Ω /90k Ω /100k Ω
EXPONENT RANGE Roots ($0.2 \leq m < 1$) Powers ($1 < m \leq 5$) ($m = 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram Below. $m = \frac{R_1 + R_2}{R_2}$ $R_1 = 0\Omega$, R_2 not used
POWER REQUIREMENTS Rated Supply Range Quiescent Current	$\pm 15\text{VDC}$ ± 12 to $\pm 18\text{VDC}$ $\pm 10\text{mA}$
TEMPERATURE RANGE Operating Storage	-25°C to $+85^\circ\text{C}$ -25°C to $+85^\circ\text{C}$

PIN CONFIGURATION



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
4302	14-Pin Plastic DIP	003

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

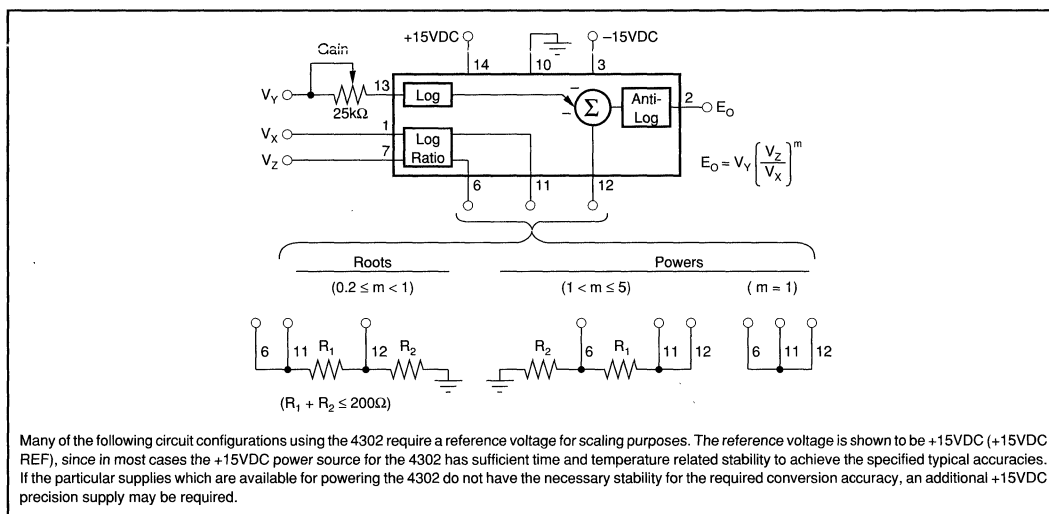
APPLICATION INFORMATION

General specifications for the 4302 multifunction converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications intended to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in

order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15VDC (+15VDC REF), since in most cases the +15VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies. If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15VDC precision supply may be required.

4302 Functional Diagram.

MULTIPLIER/ DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications, the 4302 provides high accuracy. The 4302 accepts inputs up to +10VDC and provides a typical accuracy of $\pm 0.25\%$ of full scale.

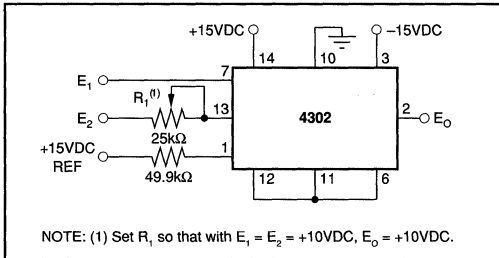


FIGURE 1. Multiplier Application.

TRANSFER FUNCTION	$E_o = + \frac{E_1 E_2}{10}$
ACCURACY Total Errors Typical at +25°C Maximum at +25°C (for input range) vs Temperature Offset Errors ($E_1 = E_2 = 0$) Output Offset (at 25°C) vs Temperature	$\pm 25\text{mV}$ $\pm 50\text{mV}$ $0.03\text{V} \leq E_1^{(1)} \leq 10\text{V}$ $0.01\text{V} \leq E_2 \leq 10\text{V}$ $\pm 1\text{mV}/^\circ\text{C}$ $\pm 10\text{mV}$ $\pm 0.2\text{mV}/^\circ\text{C}$
NOISE (10Hz to 1kHz)	100 μVrms
BANDWIDTH (E_1, E_2) Small Signal (-3dB) Full Output	500kHz 60kHz

NOTE: (1) The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

DIVIDER

As a divider, the 4302 provides a typical conversion accuracy of $\pm 0.25\%$ of full scale.

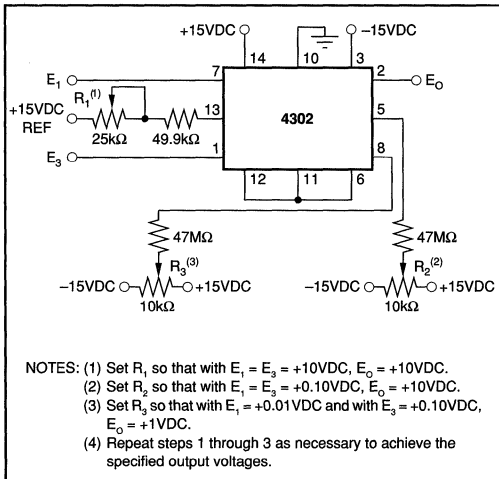


FIGURE 2. Divider Application.

TRANSFER FUNCTION	$E_o = +10 (E_1/E_3)$
ACCURACY Total Errors Typical at +25°C Maximum at +25°C (for $E_1 \leq E_3$ ad input range) vs Temperature Offset Errors ($E_1 = 0, E_3 = +10\text{V}$) Output Offset (at 25°C) vs Temperature	$\pm 25\text{mV}$ $\pm 50\text{mV}$ $0.03\text{V} \leq E_1^{(1)} \leq 10\text{V}$ $0.01\text{V} \leq E_3 \leq 10\text{V}$ $\pm 1\text{mV}/^\circ\text{C}$ $\pm 10\text{mV}$ $\pm 1\text{mV}/^\circ\text{C}$
NOISE (10Hz to 1kHz) $E_3 = +10\text{V}$ $E_3 = +0.1\text{V}$	100 μVrms 300 μVrms
BANDWIDTH (E_1, E_3) Small Signal (-3dB) Full Output ($E_3 = +10\text{V}$)	500kHz 60kHz

NOTE: (1) The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

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EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of $m = 0.2$ and $m = 5$ are presented on the right. For other values of m , the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m .

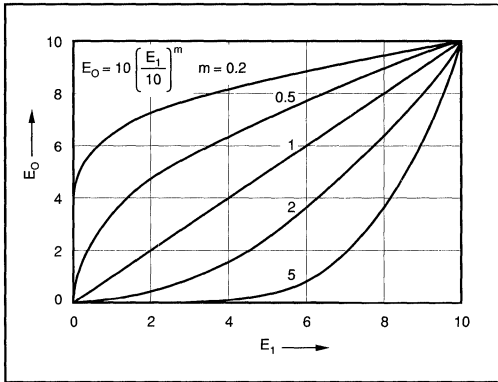


FIGURE 3. Exponentiator Transfer Characteristics.

TRANSFER FUNCTION	$E_o = 10 \left(\frac{E_i}{10} \right)^m$
Total Conversion Error (typical) $m = 0.2$ $0.5\text{VDC} < E_i \leq 10\text{VDC}$ $0.1\text{VDC} < E_i \leq 0.5\text{VDC}$ $m = 5$ $1\text{VDC} < E_i \leq 10\text{VDC}$	$\pm 2\text{mVDC}$ $\pm 25\text{mVDC}$ $\pm 15\text{mVDC}$
Exponent Range (continuous) Input Voltage Range Output Voltage Range	$0.2 \leq m \leq 5$ 0 to +10VDC 0 to +10VDC

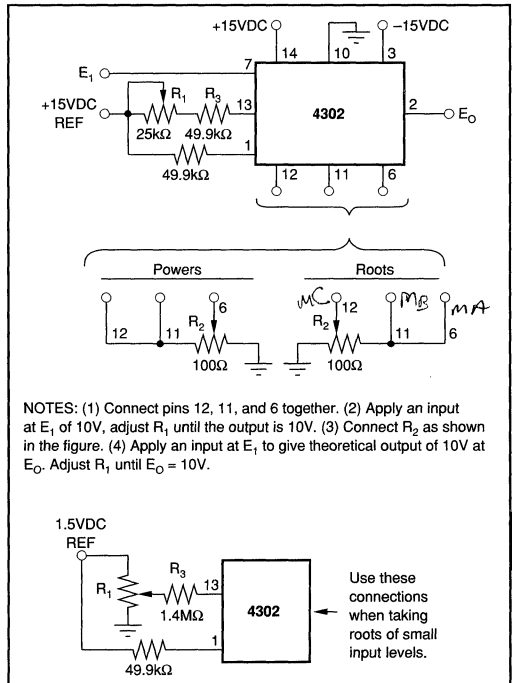


FIGURE 4. Exponential Functions.

SQUARE ROOT

As a Square Rooter ($m = 0.5$), the 4302 provides a typical total conversion accuracy of $\pm 0.07\%$. Refer to Figure 5 and notes for connections and adjustments, respectively.

TRANSFER FUNCTION	$E_o = 10 \sqrt{\frac{E_i}{10}}$
Total Conversion Error (typical) $0.5\text{VDC} < E_i \leq 10\text{VDC}$ $0.02\text{VDC} < E_i \leq 0.5\text{VDC}$	$\pm 7\text{mV}$ $\pm 55\text{mV}$
Input Voltage Range Output Voltage Range	0 to +10VDC 0 to +10VDC

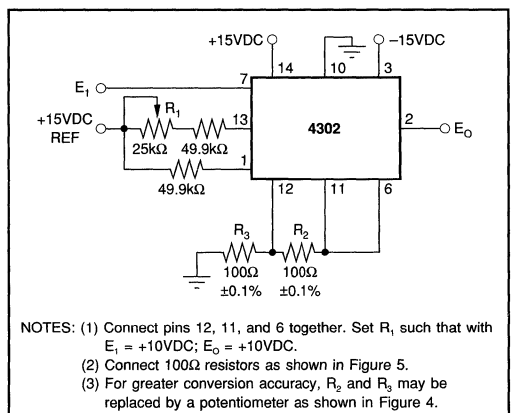


FIGURE 5. Square Root Application.

SQUARE

Configured as a Square Function Converter ($m = 2$), the 4302 produces high conversion accuracies of typically 0.03%. Refer to Figure 6 and accompanying notes.

TRANSFER FUNCTION	$E_o = 10 \left[\frac{E_i}{10} \right]^2$
Total Conversion Error (typical) $0.1\text{VDC} \leq E_i \leq 10\text{VDC}$	$\pm 3\text{mV}$
Input Voltage Range	0 to +10VDC
Output Voltage Range	0 to +10VDC

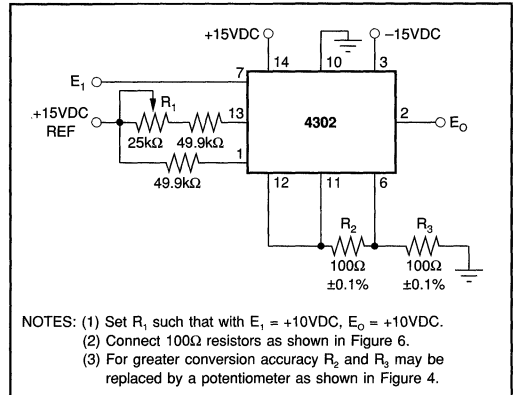


FIGURE 6. Square Application.

TRIGONOMETRIC FUNCTIONS

SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than $\pm 0.5\%$ of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_o = 0\text{VDC}$, and when $\theta = 90$, $E_o = 10\text{VDC}$.

TRANSFER FUNCTION	$E_o = 10 \sin 9E_\theta$
Power Series Approximation	$E_o = 1.5708E_\theta - 1.5924 \left[\frac{E_\theta}{6.366} \right]^{2.827}$
Total Conversion Error (typical)	$\pm 50\text{mV}$
Input Voltage Range ($0 \leq \theta \leq 90^\circ$)	0 to +10VDC
Output Voltage Range ($0 \leq \sin \theta \leq 1$)	0 to +10VDC

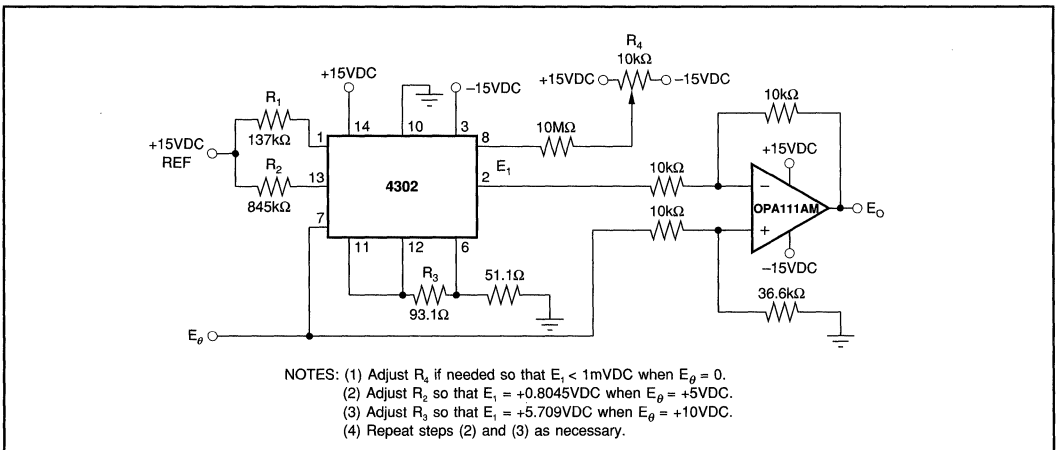


FIGURE 7. Sine Application.

COSINE

Connected as in Figure 2, 4302 will generate a cosine function of the input voltage. Typical accuracies of $\pm 0.8\%$ can be expected from this configuration.

TRANSFER FUNCTION	$E_o = 10 \cos 9E_\theta$
Power Series Approximation	$E_o = 10 + 0.3652 E_\theta - 0.4276 E_\theta^{1.504}$
Total Conversion Error (typical)	$\pm 80\text{mV}$
Input Voltage Range ($0 \leq \theta \leq 90^\circ$)	0VDC to +10VDC
Output Voltage Range ($1 \leq \cos \theta \leq 0$)	+10VDC to 0VDC

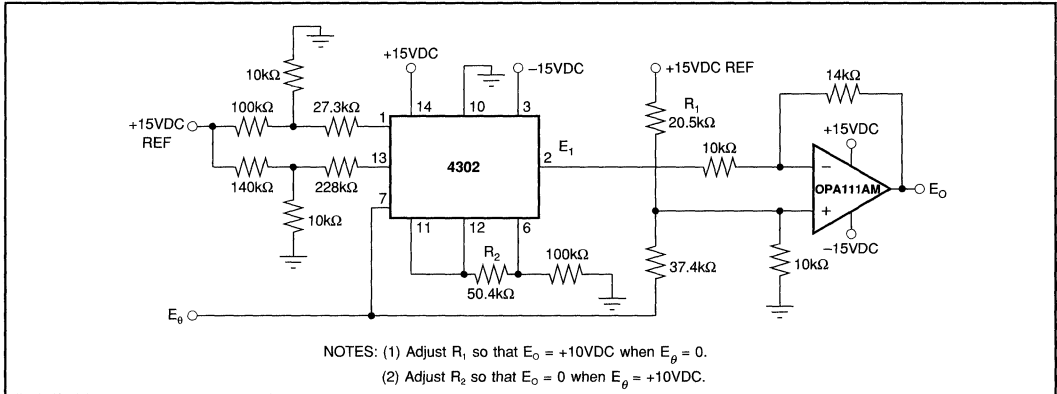


FIGURE 8. Cosine Application.

ARCTANGENT

4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

$$E_\theta = \tan^{-1} \frac{E_Y}{E_X}$$

The accuracy of conversion depends upon the levels of the input signals. Refer to table at right.

TRANSFER FUNCTION	$E_o = \tan^{-1} \left(\frac{[E_1]}{[E_2]} \right)$
Power Series Approximation	$E_o = \frac{\left(\frac{[E_1]}{[E_2]} \right)^{1.2125}}{1 + \left(\frac{[E_1]}{[E_2]} \right)^{1.2125}} (90^\circ)$
Total Conversion Error	$\pm 55\text{mVDC}$
$2 < E_1, E_2 \leq 10\text{VDC}$	$\pm 65\text{mVDC}$
$0.1 < E_1, E_2 \leq 2\text{VDC}$	$\pm 340\text{mVDC}$
$0.03 < E_1, E_2 \leq 0.1\text{VDC}$	+0.01VDC to +10VDC
Input Voltage Range (E_1, E_2)	0VDC to +9VDC
Output Voltage Range $0 \leq E_\theta \leq 90^\circ$	

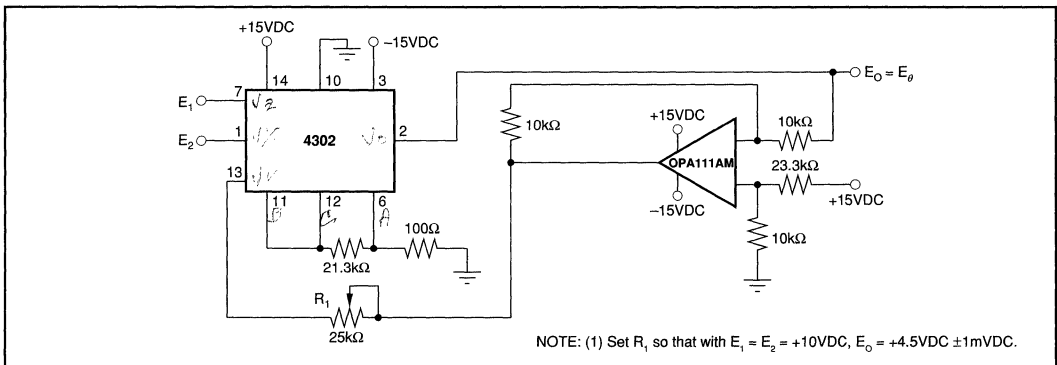


FIGURE 9. Arctangent Application.

VECTOR MAGNITUDE FUNCTION

The 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

TRANSFER FUNCTION	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2 (refer to notes 1 and 2)	0 to +10VDC -10VDC to +10VDC
Output Voltage Range	0 to +10VDC
Conversion Error	±7mVDC

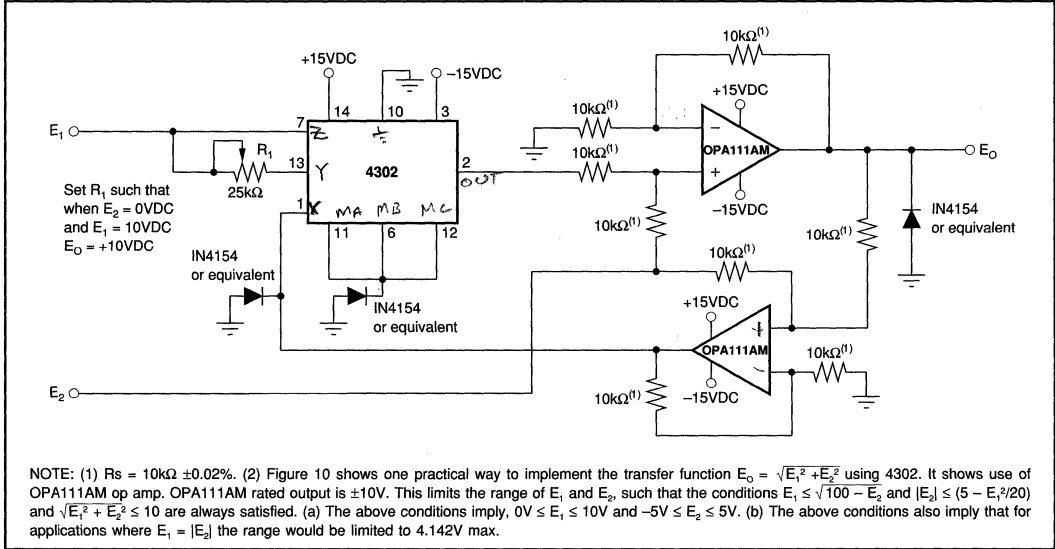


FIGURE 10. Implementation of Transfer Function.

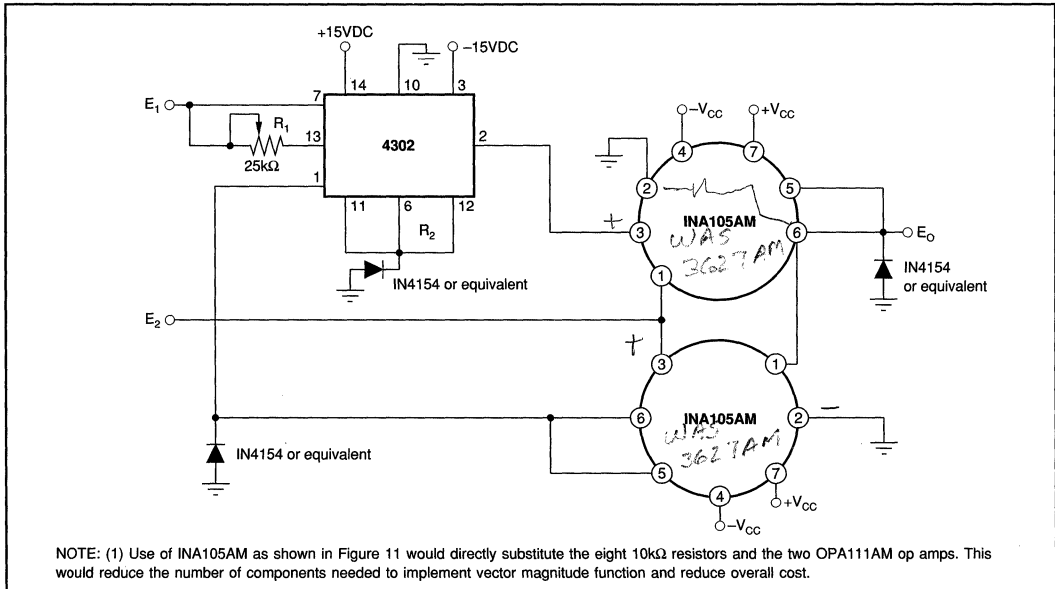


FIGURE 11. Vector Magnitude Function Application.

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4341

Low Cost TRUE RMS-TO-DC CONVERTER

FEATURES

- **LOW COST**
- **HIGH ACCURACY: $\pm 0.2\%$ $\pm 2\text{mV}$**
- **VERSATILE: AC and DC Inputs**

DESCRIPTION

The 4341 RMS-to-DC converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against over-voltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



PDS-323B

7.117

4341
7
SPECIAL FUNCTIONS

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±15VDC, unless otherwise noted.

PARAMETER	CONDITIONS
TRANSFER FUNCTION	$E_{rms}(t) = \sqrt{\frac{1}{T} \int_0^T [E_{IN}(t)]^2 dt}$
INPUT Peak Operating Voltage Absolute Maximum Voltage Impedance	±10V ±Supply 5kΩ
OUTPUT Voltage Current Resistance	0 to +10V +5mA, min 1Ω, max
BANDWIDTH ±1% of Theoretical Output -3dB	80kHz 450kHz
CONVERSION ACCURACY⁽²⁾ Input: 500mVrms to 5.0Vrms Input: DC to 10kHz Sine Wave Input: 10mVrms to 7Vrms Input: DC to 20kHz	±0.5% of Reading, max ⁽¹⁾ ±2mV ±0.2% of Reading
STABILITY Accuracy vs Temperature Accuracy vs Supply Voltage	±0.1mV ±0.01% of Reading/°C ±0.1mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE Operating Storage	-25°C to +85°C -40°C to +85°C
POWER REQUIREMENTS Rated Voltage Voltage Range Quiescent Current	±15VDC ±14VDC to ±16VDC ±12mA, typ, ±24mA, max

NOTES: (1) After standard trim procedure (see below). (2) Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (see Figure 2).

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500mVrms to 5Vrms up to 10kHz. Refer to Figure 1.

1. Set E_{IN} = 5.000Vrms ±0.02% and adjust R₁ such that E_O = 5.000VDC ±2mV.
2. Set E_{IN} = 500mVrms ±0.02% and adjust R₂ such that E_O = 500mVDC ±0.2mV.
3. Repeat Step 1.

THEORY OF OPERATION

The true rms value of a time-varying signal E (t) over a time period T is

$$E_{rms}(t) = \sqrt{\frac{1}{T} \int_0^T [E_{IN}(t)]^2 dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A₁ circuit produces a current, i₁, which is proportional to the rectified input voltage. The A₂ circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{IN} or log E_{IN}². The logarithmic gain of the A₂ circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary

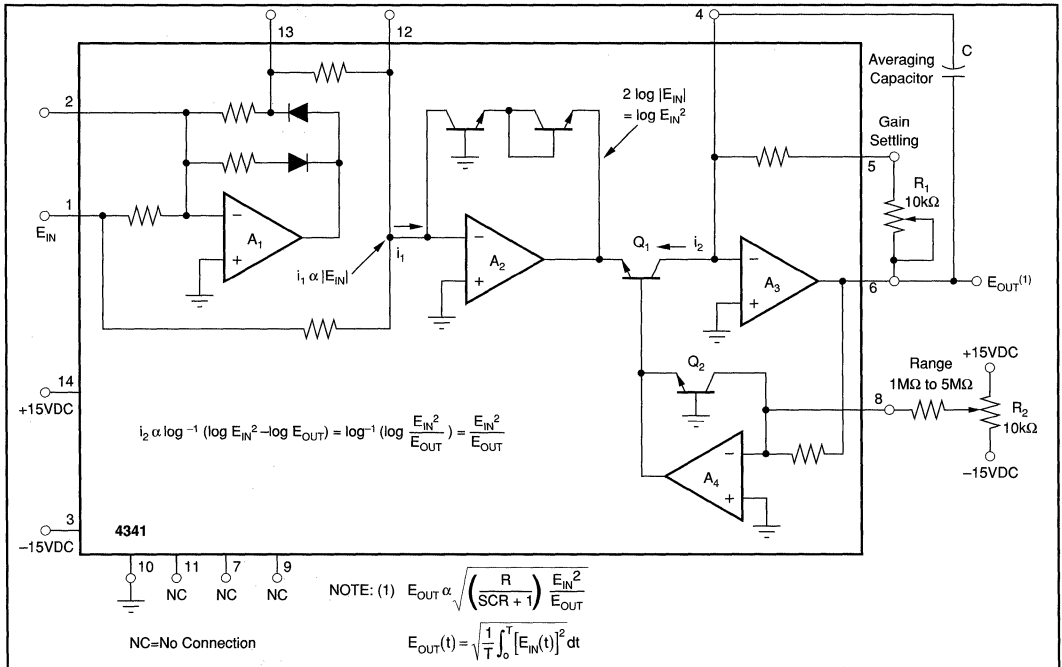


FIGURE 1. Simplified Schematic.

monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A_4 uses the same techniques as A_2 to generate $\log E_{OUT}$.

Transistor Q_1 produces a collector current, i_2 , proportional to the antilog of its base-emitter voltage such that

$$i_2 \propto \log^{-1}(\log E_{IN}^2 - \log E_{OUT})$$

$$= \log^{-1}(\log E_{IN}^2 / E_{OUT}) = E_{IN}^2 / E_{OUT}$$

The A_3 circuit, which contains the external capacitor, takes the time average of the i_2 signal and produces E_{OUT} , which is directly proportional to the rms value of E_{IN} .

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert DC input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low-pass RC filter provides the averaging function. The time constant is $1/2 RC$ where R is $10k\Omega$ when the 4341 is adjusted for unity gain. To select the best value of C , make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs frequency for several typical values of capacitor. Response time vs capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

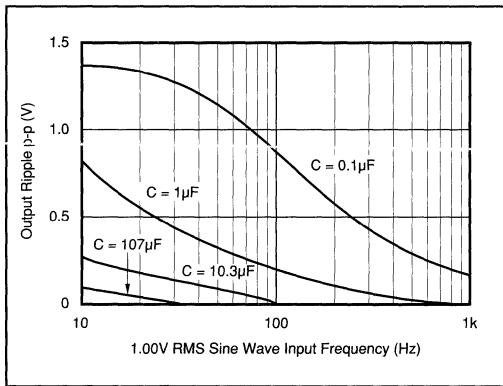


FIGURE 2. Output Ripple Magnitude vs Input Signal Frequency.

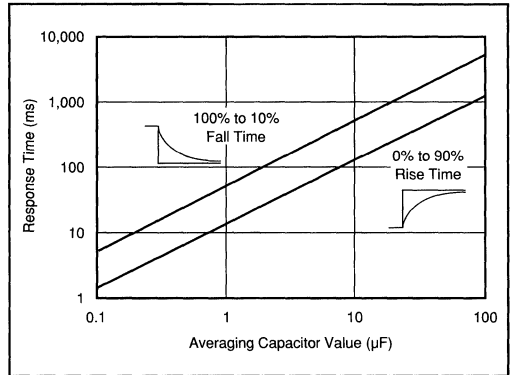


FIGURE 3. Response Time vs Value of Averaging Capacitor.

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various values of C . C can be 100s of microfarads, but should have a leakage current less than $0.1\mu A$ to minimize gain errors. With very large values of C , the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be a polar capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First, set all potentiometers at mid turn position.

1. DC Reversal Error — Apply $+10.000V \pm 1mV$ and $-10.000V \pm 1mV$ to E_{IN} alternatively, adjust R_3 such that E_o readings are the same $\pm 2mV$.
2. Gain Adjustment — Apply $E_{IN} = +10.000VDC \pm 1mV$, adjust R_1 such that $E_o = +10.000VDC \pm 1mV$.
3. Input Offset — Apply $+10.0mV \pm 0.1mV$ and $-10.0mV \pm 0.1mV$ to E_{IN} , adjust R_4 such that E_o readings are the same $\pm 0.1mV$.
4. Offset — Ground E_{IN} , adjust R_3 such that $E_o = 0 \pm 0.1mV$. Repeat Step (3).
5. Low Level Accuracy — Apply $E_{IN} = +10.0mV \pm 0.1mV$, adjust R_2 such that $E_o = +10.0mV \pm 0.1mV$.

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_X between pin 5 and pin 6. $R_X \approx (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_X is in Ω).

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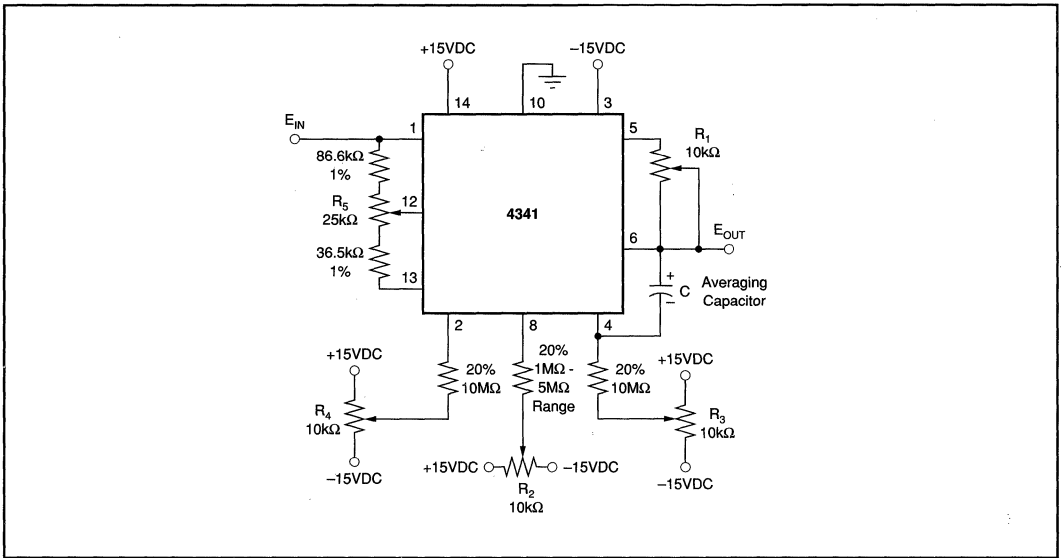


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

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8 References and Regulators

Voltage and current references are used for bridge circuits, calibration standards, D/A and A/D converter reference, sensor excitation and other applications requiring a stable voltage or current reference.

Regulators are used for battery management, distributed power, SCSI-2 termination and any other applications requiring regulated power.

Choose from our complete line of references and regulators which include:

REF1004-1.2—1.235V ± 4 mV bandgap reference that will operate from as little as 10 μ A in an 8 lead SOIC package.

REF1004-2.5—2.500V ± 20 mV bandgap reference that will operate from as little as 20 μ A in an 8 lead SOIC package.

REF02—5.0V ± 5 mV buried zener reference that will operate over an input range of 8VDC to 40VDC in an 8 lead SOIC, PDIP and TO-99 packages.

REF102—10.0V ± 2.5 mV buried zener precision reference that will operate over an input range of 11.4VDC to 36VDC in an 8 lead SOIC, PDIP and TO-99 packages.

REF200—100 μ A ± 0.5 μ A dual current reference with a compliance voltage range of 2.5VDC to 40VDC in an 8 lead SOIC, PDIP AND TO-99 packages.

REG1117—Positive 2.85V, 3.0V, 3.3V, and 5.0V regulators that will operate down to 1V input to output and up to 800mA output in an SOT-223 package.

VOLTAGE REFERENCE

Boldface = NEW

Description	Model	Output (V)	Min Output (mA)	Max Drift \pm ppm/ $^{\circ}$ C	Power Supply (V)	Power Supply (mA)	Temp Range	Pkg	Page No.
+5V Precision Voltage Reference	REF02M, G	+5.00 ± 0.09	10	10	+7/40	1.4	Mil, Ind Ceramic	TO-99	8.11
Guaranteed Long-Term Stability—25 \pm ppm/1k hrs	REF02P, U	+5.00 ± 0.03	10	8.5	+7/40	1.4	Com, Ind	PDIP, SO	8.11
	REF05M	+5.00 ± 0.03	10	8.5	+7/40	1.4	Mil	TO-99	8.19
+10V Precision Voltage Reference	REF01M, G	+10.00 ± 0.025	10	10	+11.4/40	1.4	Mil, Ind Ceramic	TO-99	8.3
Guaranteed Long-Term Stability	REF01P, U	+10.00 ± 0.020	10	8.5	+11.4/40	1.4	Ind, Com	PDIP, SO	8.3
	REF101	$\pm 10.00 \pm 0.005$	10	1	+13.5/35	4.5	Com	TO-99	8.32
	REF102	$\pm 10.00 \pm 0.0025$	10	2.5	+11.4/36	1.4	Ind, Mil	TO-99, DIP, SOIC	8.41
	REF10M	+10.00 ± 0.005	10	1	+13.5/35	4.5	Com	TO-99	8.25
Precision Micropower Voltage Reference	REF1004C	+1.235 ± 0.002	10	20ppm/ $^{\circ}$ C	—	—	Com	SOIC	8.65
	REF1004I	+1.235 ± 0.0004	10	20ppm/ $^{\circ}$ C	—	—	XInd	SOIC	8.65
	REF1004C	+2.50 ± 0.0009	20	20ppm/ $^{\circ}$ C	—	—	Com	SOIC	8.65
	REF1004I	+2.50 ± 0.018	20	20ppm/ $^{\circ}$ C	—	—	XInd	SOIC	8.65

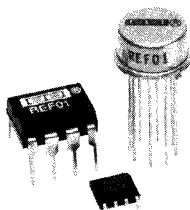
NOTE: (1) Com = 0 $^{\circ}$ C to +70 $^{\circ}$ C. Ind = -25 $^{\circ}$ C to +85 $^{\circ}$ C, Mil = -55 $^{\circ}$ C to +125 $^{\circ}$ C. XInd = -40 $^{\circ}$ C to +85 $^{\circ}$ C.

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CURRENT REFERENCE						Boldface = NEW	
Model	Output I (μ A)	Max Compliance	Drift (ppm/ $^{\circ}$ C)	Comments	Temp Range ⁽¹⁾	Pkg	Page No.
REF200	Dual 100 \pm 0.5	2.5 V to 40V	25	Includes 0.5% accurate current mirror	Ind	DIP, SO-8	8.50

NOTE: (1) Ind = -25° C to $+85^{\circ}$ C.

VOLTAGE REGULATORS								Boldface = NEW		
Description	Model	Output Voltage	Dropout Voltage at 800mA	Line Regulation (mV)	Load Regulation (mV)	Quiescent Current mA	Temperature Range	Pkg	Page No.	
+2.85V Voltage Regulator For SCSI-2 Active Termination	REG1117 REG1117-2.85	ADJ. +2.85	1.2V (max) 1.2V (max)	0.4% (max) 7 (max)	0.4% (max) 10 (max)	10 (max) 10 (max)	Com Com	SOT-223 SOT-223	8.72 8.72	
+5.0V Voltage Regulator	REG1117-5	+5	1.2V (max)	10 (max)	15 (max)	10 (max)	Com	SOT-223	8.72	
+3V/+3.3V Voltage Regulator	REG1117-3, 3.3	+3, +3.3	1.2V (max)	7 (max)	12 (max)	10 (max)	Com	SOT-223	8.72	
SCSI Terminator	REG5601	Complete 18-line SCSI Active Terminator with 2.9V reference and 100 Ω Termination.						Com	SO-28	8.79



REF01

+10V Precision VOLTAGE REFERENCE

FEATURES

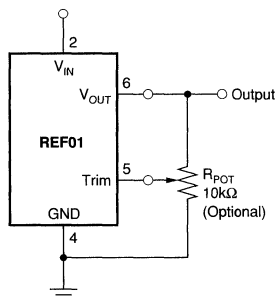
- **OUTPUT VOLTAGE:** +10V $\pm 0.2\%$ max
- **EXCELLENT TEMPERATURE STABILITY:**
8.5ppm/ $^{\circ}\text{C}$ max (-40°C to $+85^{\circ}\text{C}$)
10.0 ppm/ $^{\circ}\text{C}$ max (-55°C to $+125^{\circ}\text{C}$)
- **LOW NOISE:** 5 μV p-p typ (0.1Hz to 10Hz)
- **EXCELLENT LINE REGULATION:**
0.001%/V max
- **EXCELLENT LOAD REGULATION:**
0.002%/mA max
- **SOURCES 10mA, SINKS 5mA min**
- **LOW SUPPLY CURRENT:** 1.4mA max
- **SHORT-CIRCUIT PROTECTED**
- **WIDE SUPPLY RANGE:** 11.4VDC to 40VDC
- **PACKAGE OPTIONS:** Hermetic TO-99,
Ceramic DIP, Plastic DIP, SOIC
- **EXTENDED INDUSTRIAL TEMPERATURE
RANGE:** -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT

DESCRIPTION

The REF01 is a high performance, low price, precision pin compatible second source voltage reference. Output accuracy of $\pm 0.2\%$ is a 30% improvement over industry standard REF01s. Output noise is 5 μV p-p, which is a 75% decrease in noise over all other REF01s. Line regulation is 0.001%/V max and load regulation is 0.002%/mA max, which far exceeds the performance of our competitors. Quiescent current is a low 1.4mA. REF01 provides extended supply range when compared to industry standard devices. Burr-Brown's REF01 is the best choice for applications which requires improved accuracy, low noise, low power consumption, low drift, and the lowest price. Popular package options are available: TO-99, Ceramic DIP, plastic DIP, and SOIC. For guaranteed long-term drift see Burr-Brown's model REF10.



+10V Reference with Trimmed Output

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SPECIFICATIONS

ELECTRICAL

T_A = +25°C and V_o = +15V power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF01A, R			REF01B, S			REF01C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE (ΔV _{OT}) Change with Temperature ^(1,2) -40°C to +85°C -55°C to +125°C	I _L = 0mA	9.970	10.0	10.030	9.975	10.0	10.025	9.980	10.0	10.020	V
			0.11	0.18		0.06	0.11		0.04	0.07	%
			0.13	0.22		0.07	0.12				%
OUTPUT VOLTAGE DRIFT ⁽³⁾ -40°C to +85°C (TCV _o) -55°C to +125°C			10	25		8	15		3	8.5	±ppm/°C ±ppm/°C
OUTPUT ADJUSTMENT RANGE	R _{POT} = 10kΩ ⁽⁶⁾	±3			±3			±3			%
CHANGE IN V _o TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (-55°C to +125°C)	R _{POT} = 10kΩ		0.5			0.5			0.5		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz ⁽⁵⁾		5			5			5		μVp-p
LINE REGULATION ⁽⁴⁾ -40°C to +85°C -55°C to +125°C	V _{IN} = 11.4V to 36V	0.001	0.003		0.0007	0.002		0.0003	0.001	0.001	%V
		0.002	0.006		0.001	0.004		0.001	0.002		
LOAD REGULATION ⁽⁴⁾ -40°C to +85°C -55°C to +125°C	I _L = 0mA to +10mA I _L = 0mA to -5mA I _L = 0mA to +10mA I _L = 0mA to +10mA	0.001	0.004		0.001	0.003		0.001	0.002	0.002	%mA
		0.003	0.008		0.002	0.006		0.001	0.004	0.004	
		0.005	0.016		0.004	0.012		0.003	0.008		
		0.008	0.024		0.006	0.018					
TURN-ON SETTLING TIME	To ±0.1% of Final Value		5			5			5		μs
QUIESCENT CURRENT	No Load		1.2	1.4		1.2	1.4		1.2	1.4	mA
LOAD CURRENT		10	21		10	21		10	21		mA
SINK CURRENT		-5	-10		*	*		*	*		mA
SHORT-CIRCUIT CURRENT	V _o = 0		30			30			30		mA
POWER DISSIPATION			18			18			18		mW
TEMPERATURE RANGE Specification REF01A, B, C REF01R, S		-40 -55		+85 +125	*	*	*	*	*	*	°C °C

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 10V: $\Delta V_{OT} = \frac{|V_{MAX} - V_{MIN}|}{10V} \times 100\%$ (2) ΔV_{OT} specification applies trimmed to +10.000V or untrimmed. (3) TCV_o is defined as ΔV_{OT} divided

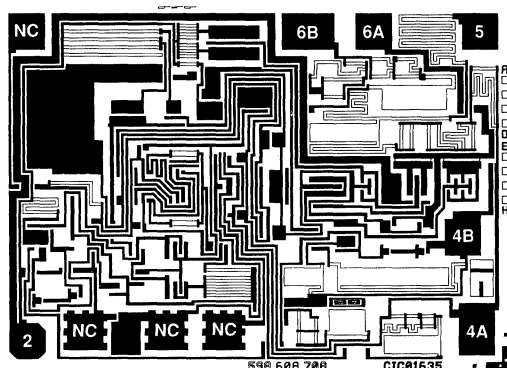
by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10kΩ potentiometer connected between V_o and ground with wiper connected to trim pin. See Figure 3.

ORDERING INFORMATION

MODEL	V _{OUT} AT 25°C	MAX DRIFT (ppm/°C)	TEMPERATURE	PACKAGE
REF01AG	10V±30mV	±25	-40°C to +85°C	8-Pin Ceramic DIP
REF01AU	10V±30mV	±25	-40°C to +85°C	8-Pin SOIC
REF01BU	10V±25mV	±15	-40°C to +85°C	8-Pin SOIC
REF01AP	10V±30mV	±25	-40°C to +85°C	8-Pin Plastic DIP
REF01BG	10V±25mV	±15	-40°C to +85°C	8-Pin Ceramic DIP
REF01BP	10V±25mV	±15	-40°C to +85°C	8-Pin Plastic DIP
REF01AM	10V±30mV	±25	-40°C to +85°C	Metal TO-99
REF01BM	10V±25mV	±15	-40°C to +85°C	Metal TO-99
REF01CM	10V±20mV	±8.5	-40°C to +85°C	Metal TO-99
REF01RM	10V±30mV	±20	-55°C to +125°C	Metal TO-99
REF01SM	10V±25mV	±10	-55°C to +125°C	Metal TO-99

Or, Call Customer Service at 1-800-548-6132 (USA Only)

DICE INFORMATION



REF01 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
2	V_{IN}	4B	GND
3A	NC	5	Trim
3B	NC	6A	V_{OUT}
3C	NC	6B	V_{OUT} (Sense)
4A	GND		

Substrate Bias: Common, pad 4B.

NOTE: Both common pads must be connected and both V_{OUT} pads must be tied together.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	55 x 75	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	5 x 5	0.10 x 0.10
Backing		Gold

REF01

8

REFERENCES AND REGULATORS

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

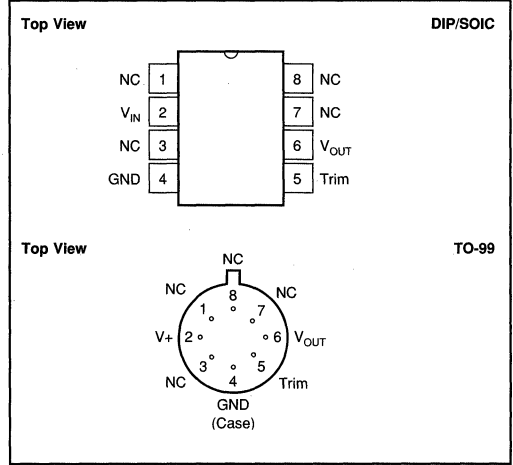
Input Voltage	+40V
Operating Temperature	
G, P, U	-40°C to +85°C
M	-55°C to +125°C
Storage Temperature Range	
G, P, U	-65°C to +125°
M	-65°C to +150°
Output Short Circuit Duration (to Ground or V_{IN})	Indefinite
Junction Temperature	-65°C to +150°
θ_{JA} P,G	120°C/W
U	80°C/W
M	150°C/W
Lead Temperature (soldering, 60s)	+300°C

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF01AG	8-Pin Ceramic DIP	161
REF01AU	8-Pin SOIC	182
REF01BU	8-Pin SOIC	182
REF01AP	8-Pin Plastic DIP	006
REF01BG	8-Pin Ceramic DIP	161
REF01BP	8-Pin Plastic DIP	006
REF01AM	Metal TO-99	001
REF01BM	Metal TO-99	001
REF01CM	Metal TO-99	001
REF01RM	Metal TO-99	001
REF01SM	Metal TO-99	001

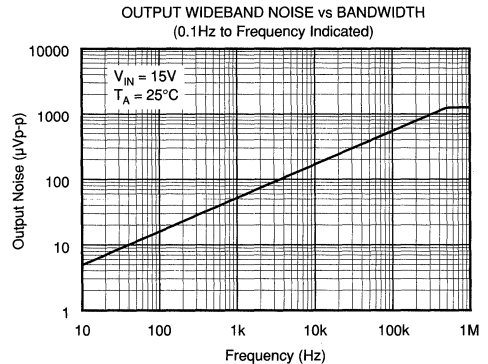
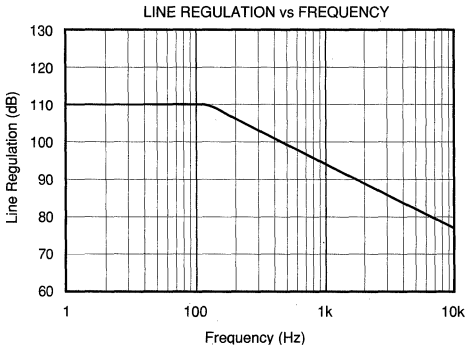
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATIONS



TYPICAL PERFORMANCE CURVES

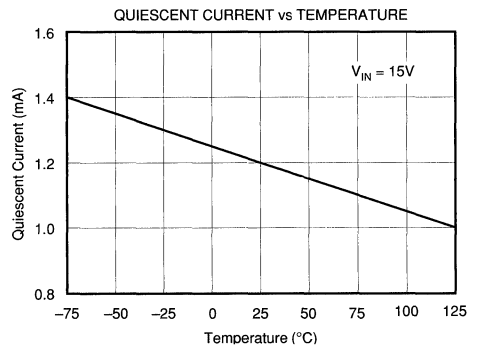
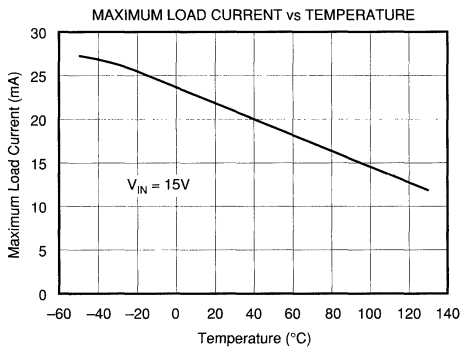
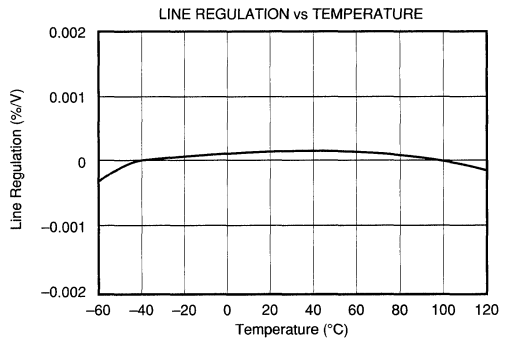
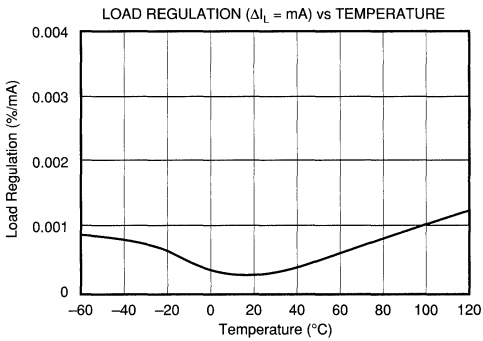
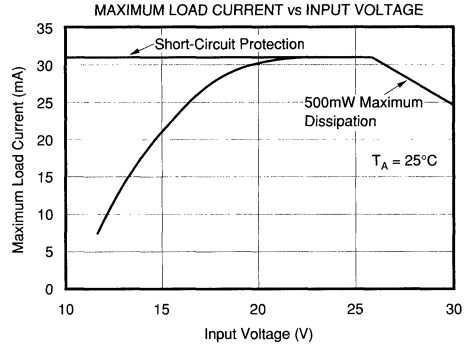
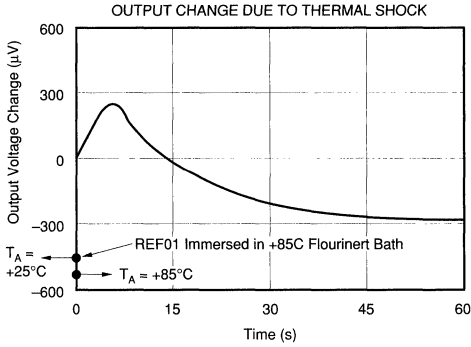
$T_A = +25^\circ\text{C}$ and $V_S = +15\text{V}$ power supply unless otherwise noted.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ and $V_S = +15\text{V}$ power supply unless otherwise noted.



REF01

8

REFERENCES AND REGULATORS

OUTPUT ADJUSTMENT

The REF01 trim terminal can be used to adjust the voltage over a 10V \pm 300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V, including 10.240V for binary applications (see circuit on the first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.5ppm/ $^{\circ}$ C for 100mV of output adjustment.

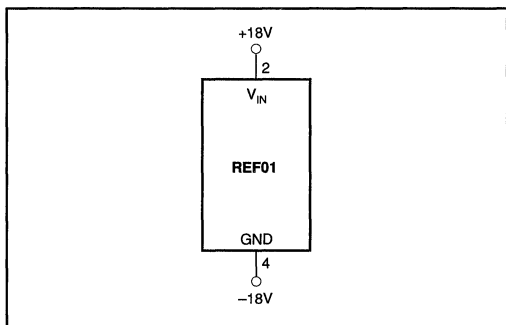


FIGURE 1. Burn-In Circuit.

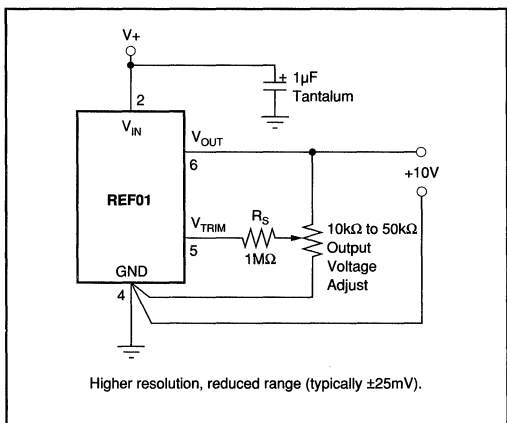


FIGURE 2. High Resolution Output Adjustment.

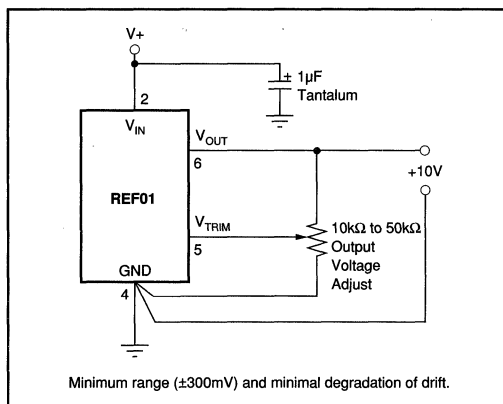


FIGURE 3. Optional Output Voltage Adjustment.

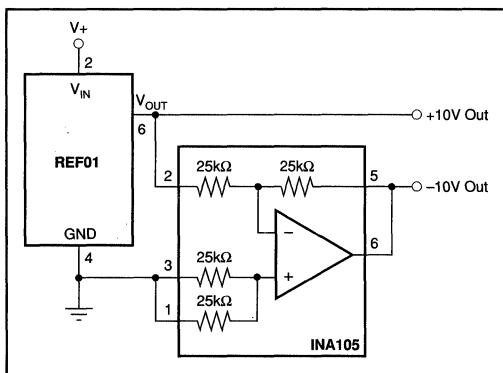


FIGURE 4. \pm 10V Reference.

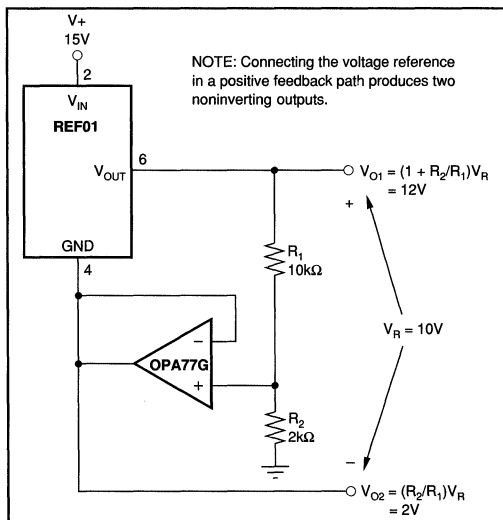


FIGURE 5. +2V and +12V Reference.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

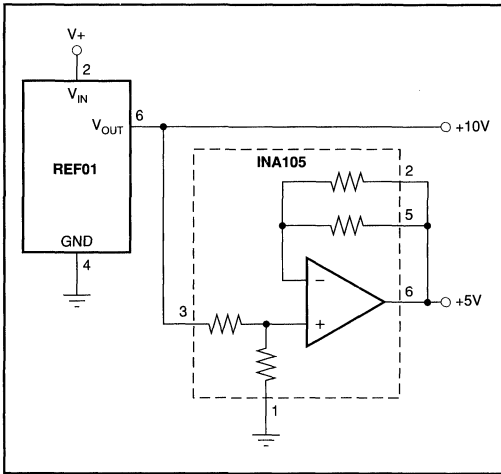


FIGURE 6. +5V and +10V Reference.

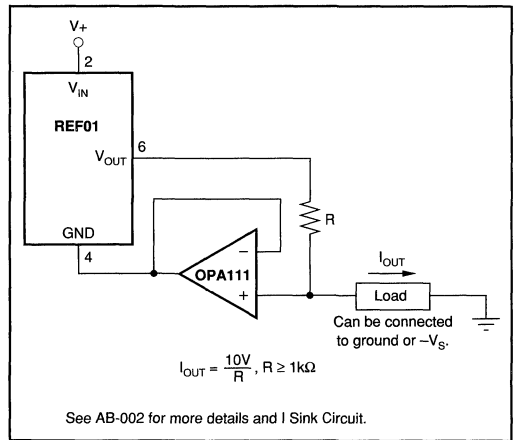


FIGURE 8. Precision Current Source.

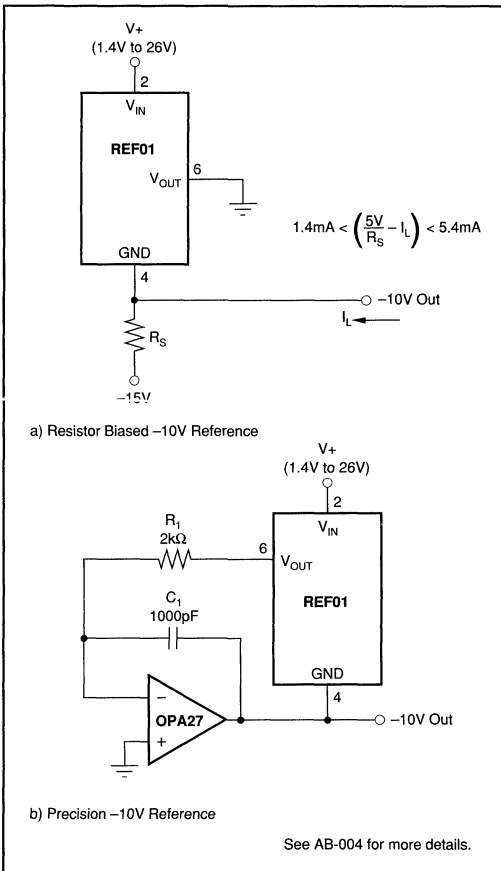


FIGURE 7. -10V Reference Using a) Resistor or b) OPA27.

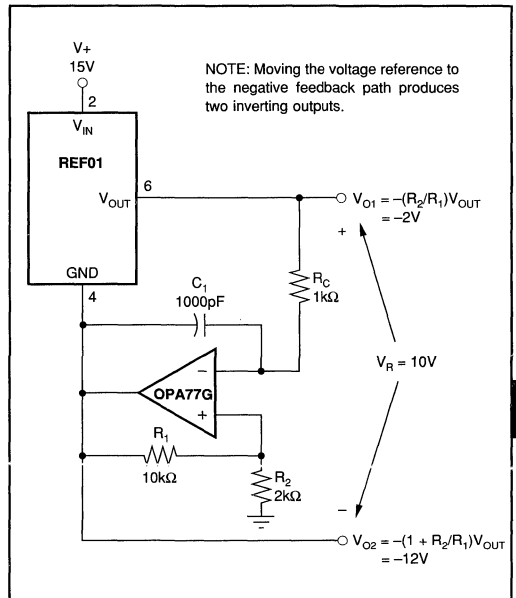


FIGURE 9. -2V and -12V Reference.

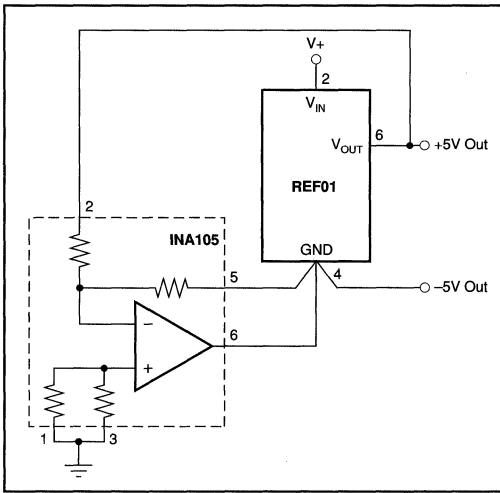


FIGURE 10. $\pm 5V$ Reference.

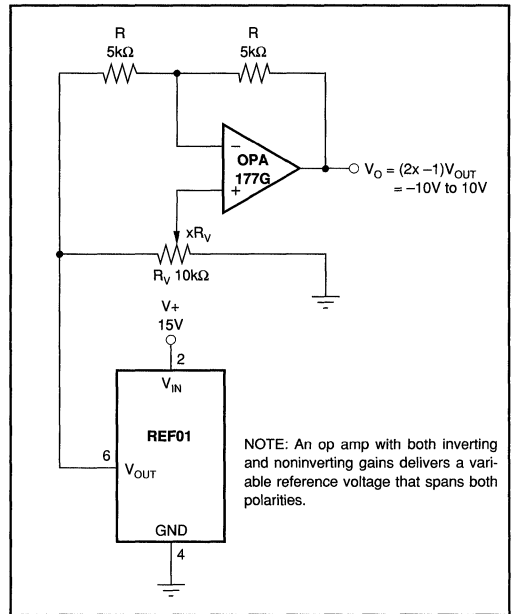


FIGURE 12. Bipolar-Output Adjustable Reference.

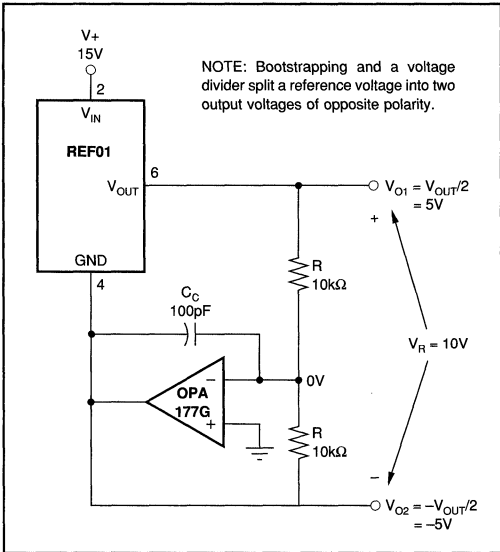
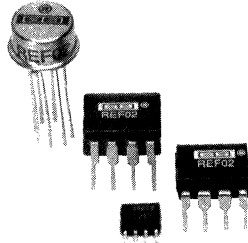


FIGURE 11. $\pm 5V$ Reference.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



REF02

+5V Precision VOLTAGE REFERENCE

FEATURES

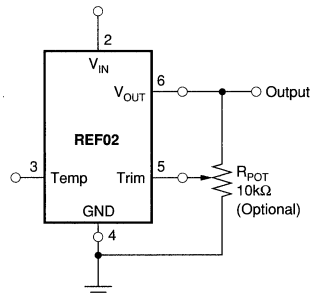
- **OUTPUT VOLTAGE:** +5V $\pm 0.1\%$ max
- **EXCELLENT TEMPERATURE STABILITY:**
8.5ppm/ $^{\circ}\text{C}$ max (-40°C to $+85^{\circ}\text{C}$)
8.5ppm/ $^{\circ}\text{C}$ max (-55°C to $+125^{\circ}\text{C}$)
- **LOW NOISE:** 10 μV p-p max (0.1Hz to 10Hz)
- **EXCELLENT LINE REGULATION:**
0.008%/V max
- **EXCELLENT LOAD REGULATION:**
0.005%/mA max
- **LOW SUPPLY CURRENT:** 1.4mA max
- **SHORT-CIRCUIT PROTECTED**
- **WIDE SUPPLY RANGE:** 8V to 40V
- **EXTENDED INDUSTRIAL TEMPERATURE RANGE:** -40°C to $+85^{\circ}\text{C}$
- **PACKAGE OPTIONS:** Hermetic TO-99, Plastic DIP, Cerdip, SOIC

APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- V/F CONVERTERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT

DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 8.5ppm/ $^{\circ}\text{C}$ max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a $\pm 6\%$ range with minimal effect on temperature stability. REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. All popular package options are available: hermetic TO-99, ceramic DIP, plastic DIP, and SOIC. The REF02 is an ideal choice for portable instrumentation, temperature transducers, A/D and D/A converters, and digital voltmeter.



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PDS-1177E

8.11

REF02
REFERENCES AND REGULATORS

For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$ and $V_{IN} = +15\text{V}$ power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF02A, R			REF02B, S			REF02C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE Change with Temperature ^(1,2) (ΔV_{OT}) -40°C to +85°C -55°C to +125°C	$I_{LOAD} = 0\text{mA}$	4.985	5.0	5.015	4.990	*	5.010	4.995	*	5.005	V
			0.05	0.19		0.05	0.13		0.05	0.11	%
			0.05	0.27		0.05	0.15				%
OUTPUT VOLTAGE DRIFT ⁽³⁾ -40°C to +85°C (TCV _O) -55°C to +125°C			4	15		4	10		4	8.5	$\pm\text{ppm}/^\circ\text{C}$
			4	15		4	8.5				$\pm\text{ppm}/^\circ\text{C}$
OUTPUT ADJUSTMENT RANGE	$R_{POT} = 10\text{k}\Omega$ ⁽⁶⁾	± 3	± 6		*	*		*	*		%
CHANGE IN V_O TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (-55°C to +125°C)	$R_{POT} = 10\text{k}\Omega$		0.7			*			*		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz ⁽⁵⁾		4	10		*	*		*	*	$\mu\text{Vp-p}$
LINE REGULATION ⁽⁴⁾ -40°C to +85°C -55°C to +125°C	$V_{IN} = 8\text{V to } 33\text{V}$ $V_{IN} = 8.5\text{V to } 33\text{V}$ $V_{IN} = 9\text{V to } 33\text{V}$		0.006	0.010		*	*		0.004	0.008	%/V
			0.008	0.012		*	*		0.005	0.010	
			0.009	0.015		*	*				
LOAD REGULATION ⁽⁴⁾ -40°C to +85°C -55°C to +125°C	$I_L = 0\text{mA to } +10\text{mA}$ $I_L = 0\text{mA to } +10\text{mA}$ $I_L = 0\text{mA to } +10\text{mA}$		0.005	0.010		*	0.008		0.003	0.005	%/mA
			0.007	0.012		*	0.010		0.004	0.005	
			0.008	0.015		*	0.012				
TURN-ON SETTLING TIME	To $\pm 0.1\%$ of Final Value		5			*			*		μs
QUIESCENT CURRENT	No Load		1.0	1.4		*	*		*	*	mA
LOAD CURRENT (SOURCE)		10	21		*	*		*	*		mA
LOAD CURRENT (SINK)		-0.3	-0.5		*	*		*	*		mA
SHORT-CIRCUIT CURRENT	$V_{OUT} = 0$		30			*			*		mA
POWER DISSIPATION	No Load		15	21		*	*		*	*	mW
TEMPERATURE VOLTAGE OUTPUT ⁽⁷⁾			630			*			*		mV
TEMPERATURE COEFFICIENT of Temperature Pin Voltage -55°C to +125°C			2.1								$\text{mV}/^\circ\text{C}$
TEMPERATURE RANGE Specification REF02A, B, C REF02R, S		-40		+85	*		*	*		*	$^\circ\text{C}$
		-55		+125	*		*				$^\circ\text{C}$

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V: $\Delta V_O = \frac{|V_{MAX} - V_{MIN}|}{5V} \times 100$ (2) ΔV_{OT} specification applies trimmed to +5.000V or untrimmed. (3) TCV_O is defined as ΔV_{OT} divided

by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10k Ω potentiometer connected between V_{OUT} and ground with wiper connected to Trim pin. See Figure on page 1. (7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each μA of loading.

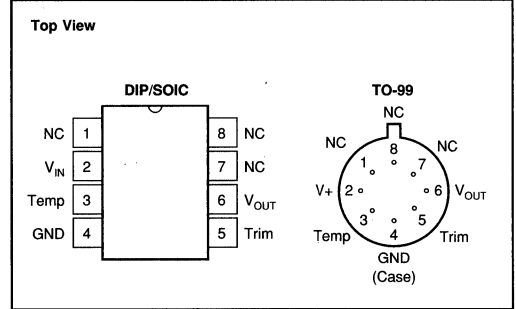
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ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
G, P, U	-40°C to +85°C
M	-55°C to +125°C
Storage Temperature Range	
G, P, U	-65°C to +125°
M	-65°C to +150°
Output Short Circuit Duration (to Ground or V_{IN})	Indefinite
Junction Temperature	-65°C to +150°
θ_{JA} P, G	120°C/W
U	80°C/W
M	150°C/W
Lead Temperature (soldering, 60s)	+300°C

PIN CONFIGURATIONS



PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF02AU	SOIC	182
REF02BU	SOIC	182
REF02AP	Plastic DIP	006
REF02BP	Plastic DIP	006
REF02AG	Cerdip	161
REF02BG	Cerdip	161
REF02AM	Metal TO-99	001
REF02BM	Metal TO-99	001
REF02CM	Metal TO-99	001
REF02RM	Metal TO-99	001
REF02SM	Metal TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

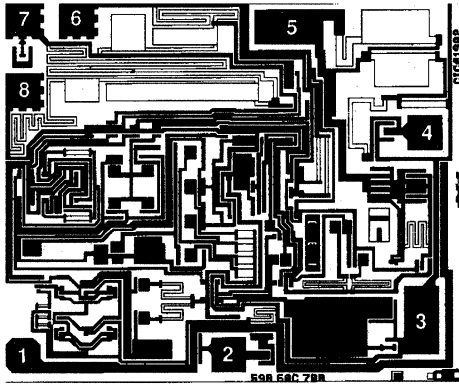
ORDERING INFORMATION

MODEL	V_{OUT} AT 25°C	MAX DRIFT (ppm/°C)	TEMPERATURE	PACKAGE
REF02AU	5V±15mV	±15	-40°C to +85°C	SOIC
REF02BU	5V±10mV	±10	-40°C to +85°C	SOIC
REF02AP	5V±15mV	±15	-40°C to +85°C	Plastic DIP
REF02BP	5V±10mV	±10	-40°C to +85°C	Plastic DIP
REF02AG	5V±15mV	±15	-40°C to +85°C	Cerdip
REF02BG	5V±10mV	±10	-40°C to +85°C	Cerdip
REF02AM	5V±15mV	±15	-40°C to +85°C	Metal TO-99
REF02BM	5V±10mV	±10	-40°C to +85°C	Metal TO-99
REF02CM	5V±5mV	±8.5	-40°C to +85°C	Metal TO-99
REF02RM	5V±15mV	±15	-55°C to +125°C	Metal TO-99
REF02SM	5V±10mV	±8.5	-55°C to +125°C	Metal TO-99

8 REF02 REFERENCES AND REGULATORS

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DICE INFORMATION



REF02 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	V_{IN}	5	V_{OUT}
2	Temp	6	NC
3	GND	7	NC
4	Trim	8	NC

Substrate Bias: -V

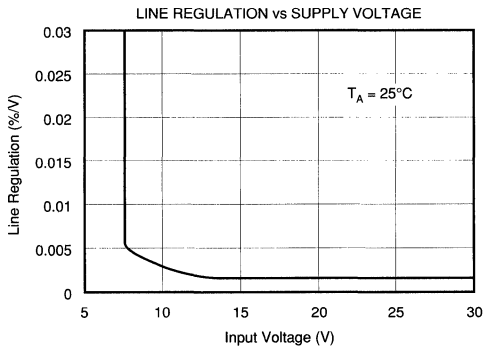
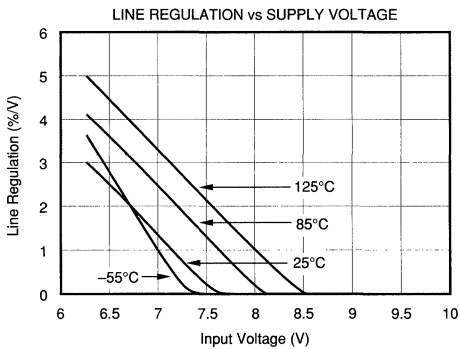
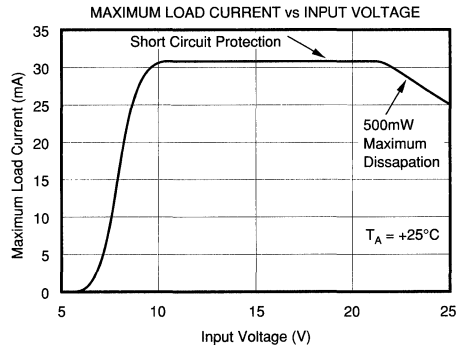
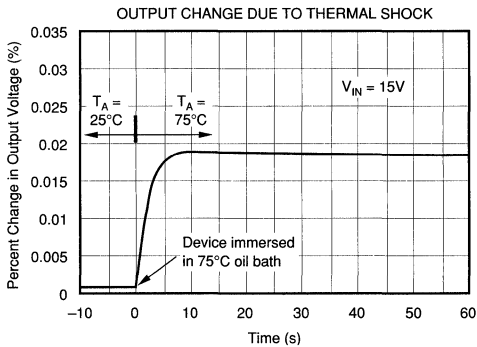
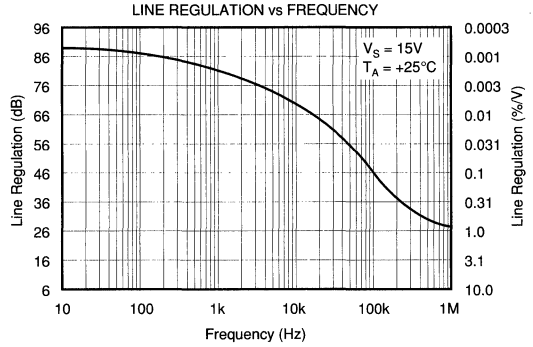
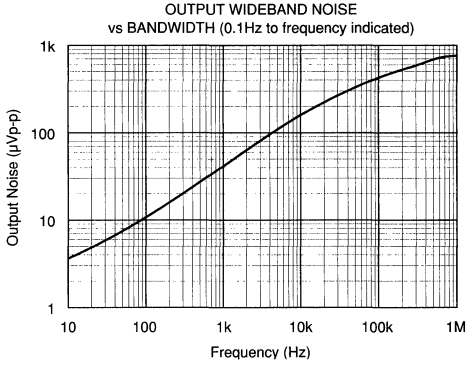
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	73 x 62	1.85 x 1.57
Die Thickness	14 ±3	0.36 ± 0.08
Min. Pad Size	5 x 5	0.10 x 0.10
Gold Backing		

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$ unless otherwise noted.



REF02

8

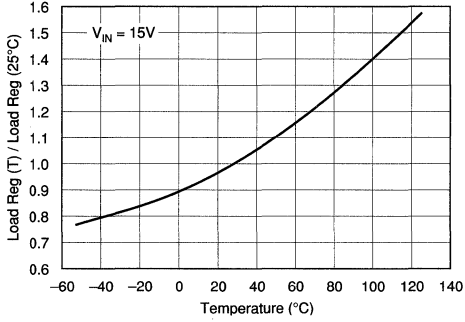
REFERENCES AND REGULATORS

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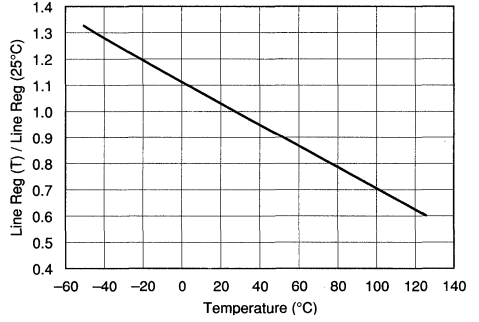
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ unless otherwise noted.

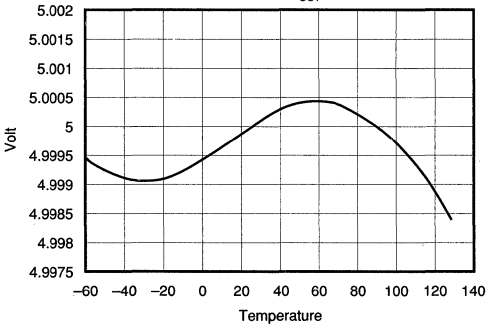
NORMALIZED LOAD REGULATION ($\Delta I_L = 10\text{mA}$)
vs TEMPERATURE



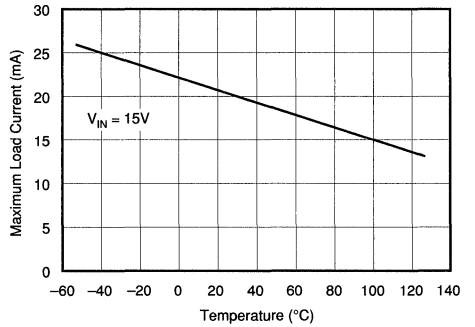
NORMALIZED LINE REGULATION vs TEMPERATURE



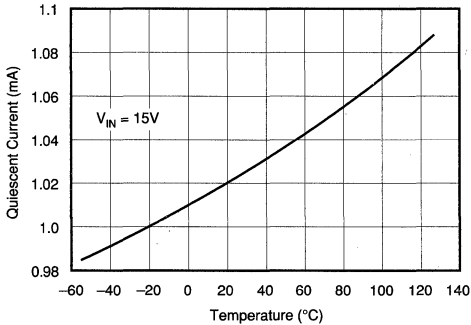
REF02 V_{OUT}



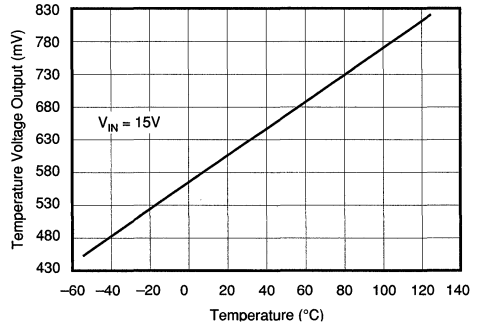
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



TYPICAL TEMPERATURE VOLTAGE OUTPUT
vs TEMPERATURE (REF02M)



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OUTPUT ADJUSTMENT

The REF02 trim terminal can be used to adjust the voltage over a $5V \pm 150mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V, including $5.12V^{(1)}$ for binary applications (see circuit on page one).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately $0.7ppm/^{\circ}C$ for $100mV$ of output adjustment.

NOTE: (1) 20mV LSB for 8-bit applications.

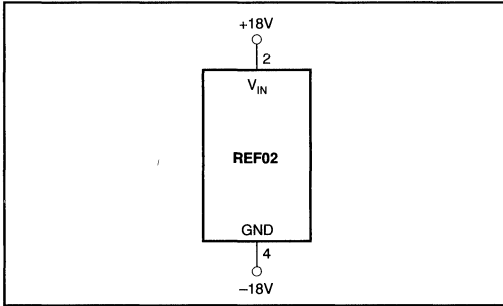


FIGURE 1. Burn-In Circuit.

TYPICAL APPLICATIONS

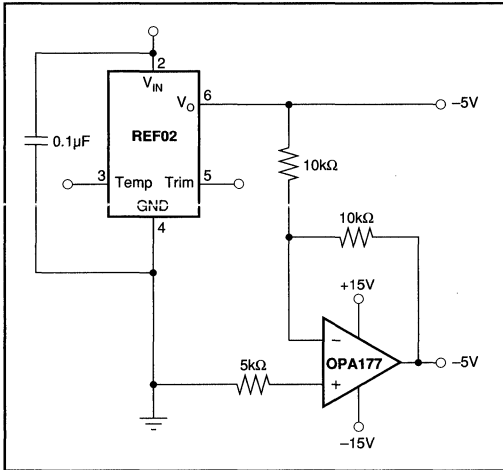


FIGURE 2. $\pm 5V$ Precision Reference.

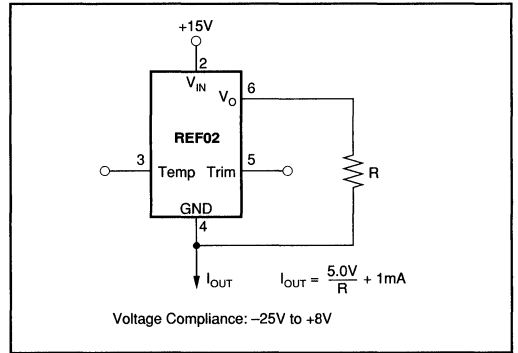


FIGURE 3. Current Source.

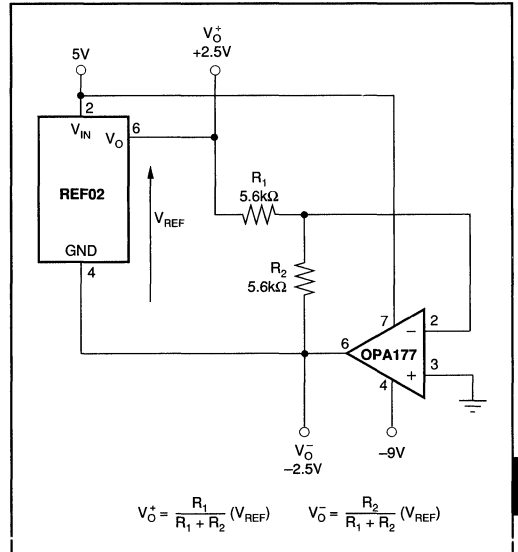


FIGURE 4. $\pm 2.5V$ Precision Reference.

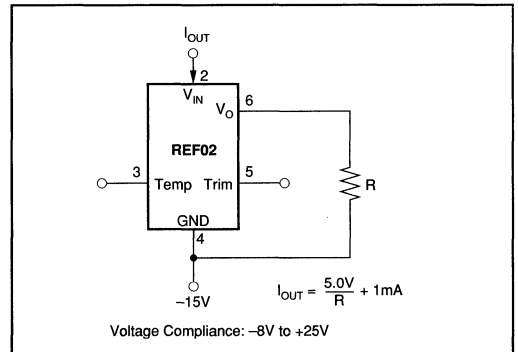


FIGURE 5. Current Sink.

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REFERENCE STACKING PROVIDES OUTSTANDING LINE REGULATION

By stacking two REF01s and one REF02, a systems designer can achieve 5V, 15V and 25V outputs. One very important advantage of this circuit is the near perfect line regulation at 5V and 15V outputs. This circuit can accept a 27V to 55V change to the input with less than the noise voltage as a change to the output voltage. (R_B), a load bypass resistor, supplies current (I_{SV}) for the 15V regulator.

Any number of REF01s and REF02s can be stacked in this configuration. If ten devices can be stacked in this configuration, for example, ten 5V or five 10V outputs are achieved. The line voltage may range from 100V to 130V. Care should be exercised to insure that the total load currents do not exceed the maximum usable current which is typically 21mA.

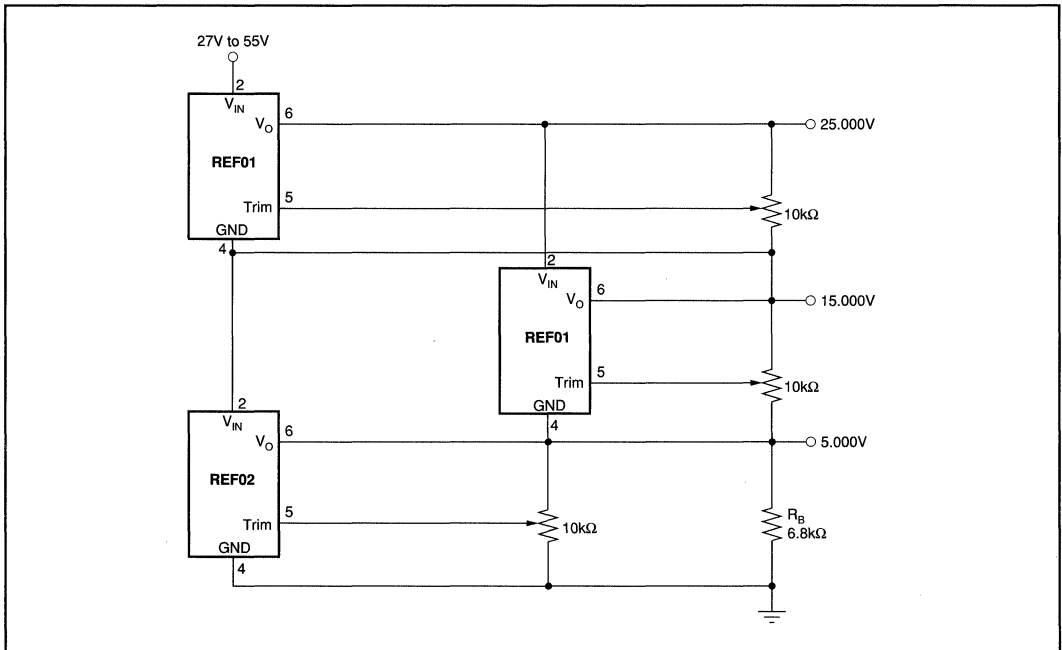


FIGURE 6. Reference Stack.

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REF05

+5V Precision VOLTAGE REFERENCE (Guaranteed Long-Term Stability)

FEATURES

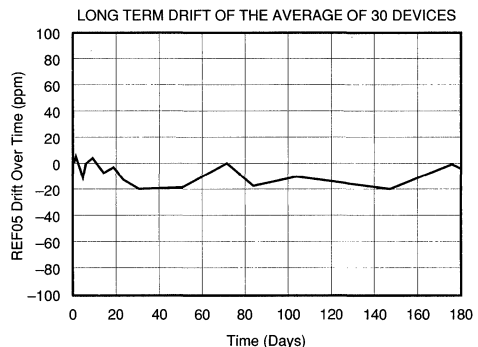
- **OUTPUT VOLTAGE:** +5V $\pm 0.1\%$ max
- **GUARANTEED LONG-TERM STABILITY:** 25ppm/1000 hrs max
- **EXCELLENT TEMPERATURE STABILITY:** 8.5ppm/ $^{\circ}\text{C}$ max (-55°C to $+125^{\circ}\text{C}$)
- **LOW NOISE:** 10 μV p-p typ (0.1Hz to 10Hz)
- **EXCELLENT LINE REGULATION:** 0.008%/V max
- **EXCELLENT LOAD REGULATION:** 0.005%/mA max
- **LOW SUPPLY CURRENT:** 1.4mA max
- **SHORT-CIRCUIT PROTECTED**
- **WIDE SUPPLY RANGE:** 8VDC to 40VDC
- **HIGH LOAD DRIVING CAPACITY:** 20mA
- **PACKAGE:** Hermetic TO-99

APPLICATIONS

- **PRECISION REGULATORS**
- **CONSTANT CURRENT SOURCE/SINK**
- **DIGITAL VOLTMETERS**
- **A/D AND D/A CONVERTERS**
- **PRECISION CALIBRATION STANDARD**
- **TEST EQUIPMENT**

DESCRIPTION

The REF05 is a precision 5V voltage reference. The drift is laser trimmed to 8.5ppm/ $^{\circ}\text{C}$ max over the extended industrial and military temperature range. The REF05 provides a stable 5V output that can be externally adjusted over a $\pm 6\%$ range with minimal effect on temperature stability. REF05 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF05 the best choice whenever a 5V voltage reference is required. The REF05 is an ideal choice for portable instrumentation, temperature transducers, A/D and D/A converters, and digital voltmeter.



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$ and $V_S = +15\text{V}$ power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF05R			REF05S			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE (ΔV_{OT}) Change with Temperature ^(1,2) -55°C to +125°C	$I_L = 0\text{mA}$	4.985	5.00	5.015	4.990	5.00	5.010	V
			0.05	0.27		0.05	0.15	%
OUTPUT VOLTAGE DRIFT ⁽³⁾ -55°C to +125°C (TCV_O)			4	15		4	8.5	$\pm\text{ppm}/^\circ\text{C}$
LONG TERM STABILITY ⁽⁴⁾			10	25		10	25	$\pm\text{ppm}/1\text{K hrs}$
OUTPUT ADJUSTMENT RANGE	$R_{POT} = 10\text{k}\Omega$ ⁽⁶⁾	± 3	± 6		± 3	± 6		%
CHANGE IN V_O TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT (-55°C to +125°C)	$R_{POT} = 10\text{k}\Omega$ ⁽⁶⁾		0.7			0.7		ppm/%
OUTPUT VOLTAGE NOISE	0.1Hz to 10Hz ⁽⁵⁾		4	10		4	10	$\mu\text{Vp-p}$
LINE REGULATION ⁽⁴⁾ -55°C to +125°C	$V_{IN} = 8\text{V to }33\text{V}$ $V_{IN} = 9\text{V to }33\text{V}$		0.006	0.010		0.006	0.010	%/V
			0.009	0.015		0.009	0.015	
LOAD REGULATION ⁽⁴⁾ -55°C to +125°C	$I_L = 0\text{mA to }+10\text{mA}$ $I_L = 0\text{mA to }+10\text{mA}$		0.005	0.010		0.005	0.008	%/mA
			0.008	0.015		0.008	0.012	
TURN-ON SETTLING TIME	To $\pm 0.1\%$ of Final Value		5			5		μs
QUIESCENT CURRENT	No Load		1.0	1.4		1.0	1.4	mA
LOAD CURRENT (Source)		10	21		10	21		mA
LOAD CURRENT (Sink)		-0.3	-0.5		*	*		mA
SHORT-CIRCUIT CURRENT	$V_O = 0$		30			30		mA
POWER DISSIPATION			15	21		15	21	mW
TEMPERATURE VOLTAGE OUTPUT ⁽⁷⁾			630			630		mV
TEMPERATURE COEFFICIENT OF TEMPERATURE PIN VOLTAGE			2.1			2.1		$\text{mV}/^\circ\text{C}$
TEMPERATURE RANGE Specification REF05R, S		-55		+125	*		*	$^\circ\text{C}$

NOTES: (1) ΔV_{OT} is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V: $\Delta V_{OT} = \frac{|V_{MAX} - V_{MIN}|}{5V} \times 100$ (2) ΔV_{OT} specification applies trimmed to +5.000V or untrimmed. (3) TCV_O is defined as ΔV_{OT} divided

by the temperature range. (4) Line and load regulation specifications include the effect of self heating. (5) Sample tested. (6) 10k Ω potentiometer connected between V_O and ground with wiper connected to Trim pin. See Figure 1. (7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each μA of loading. (8) Samples tested for long term stability are tested with continuous power applied.

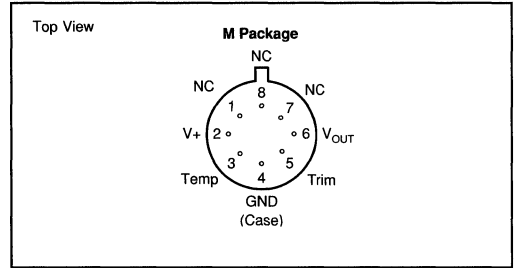
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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Input Voltage	+40V
Operating Temperature	
M	-55°C to +125°C
Storage Temperature Range	
M	-65°C to +150°C
Output Short Circuit Duration (to Ground or V_{IN})	Indefinite
Junction Temperature	-65°C to +150°C
θ_{JA} M	150°C/W
Lead Temperature (soldering, 60s)	+300°C

PIN CONFIGURATIONS



PACKAGE INFORMATION⁽¹⁾

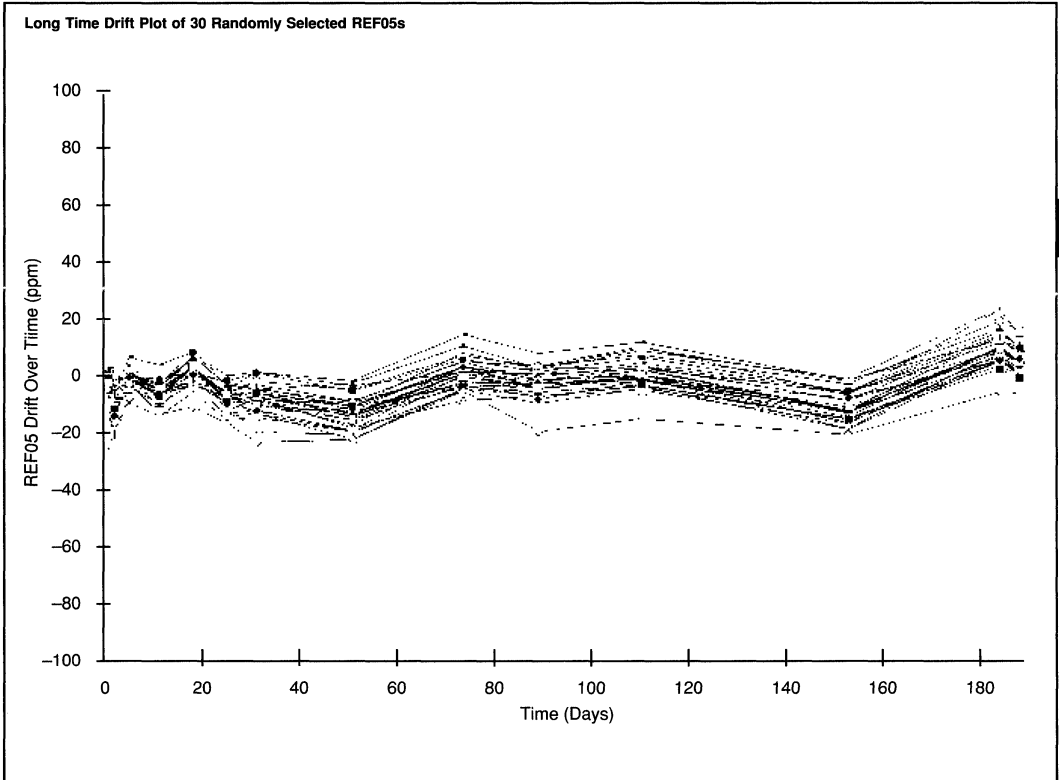
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF05RM	Metal TO-99	001
REF05SM	Metal TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	V_{OUT} AT 25°C	MAX DRIFT (ppm/°C)	TEMPERATURE	PACKAGE
REF05RM	5V ±15mV	±15	-55°C to +125°C	Metal TO-99
REF05SM	5V ±10mV	±8.5	-55°C to +125°C	Metal TO-99

PONY TAIL DRIFT PLOT



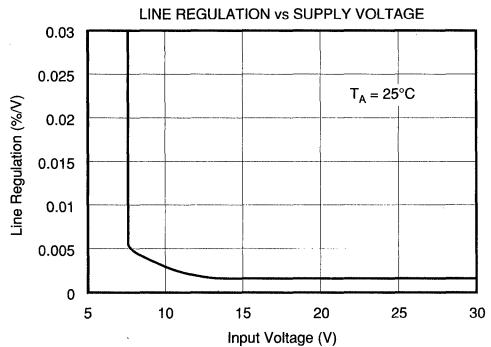
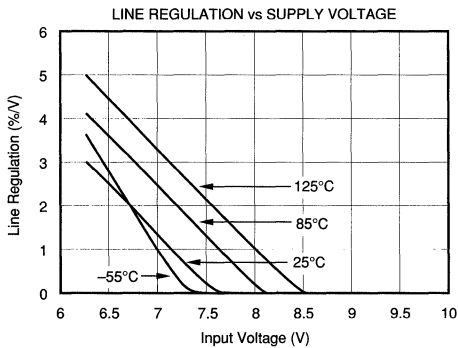
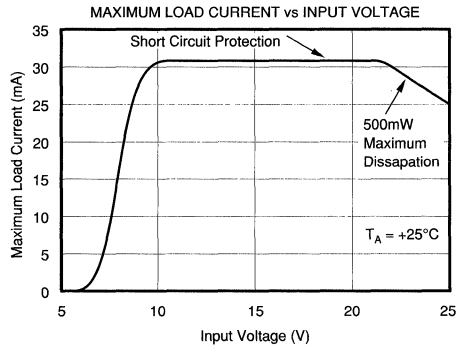
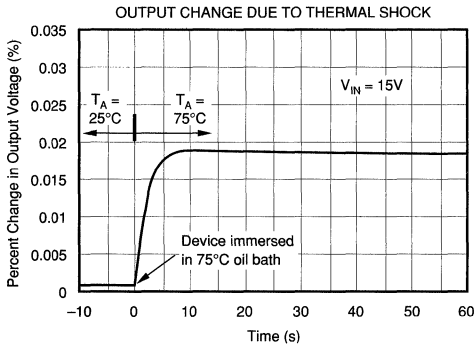
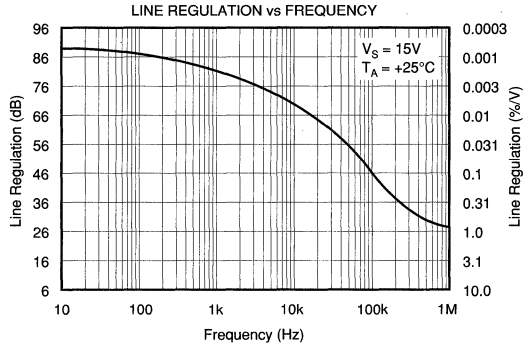
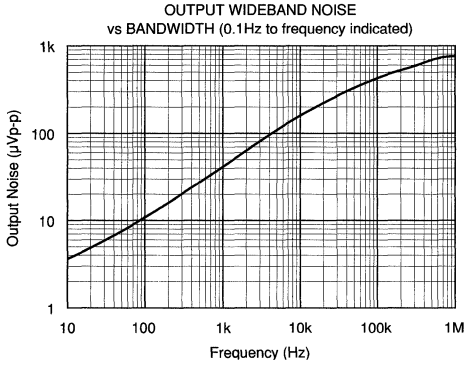
REF05

REFERENCES AND REGULATORS

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TYPICAL PERFORMANCE CURVES

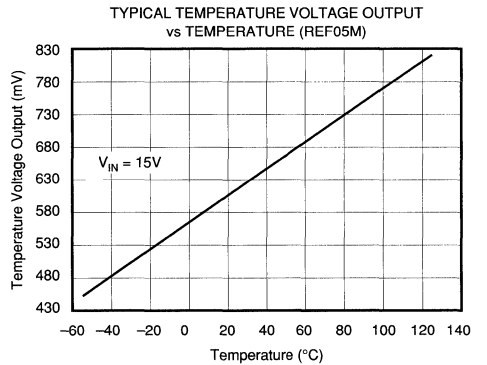
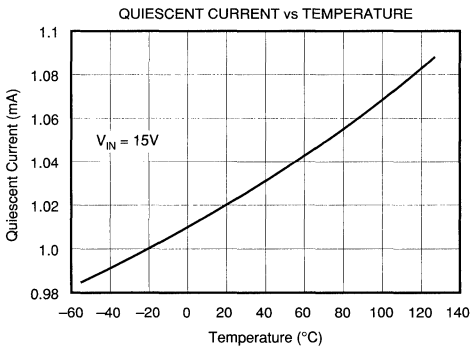
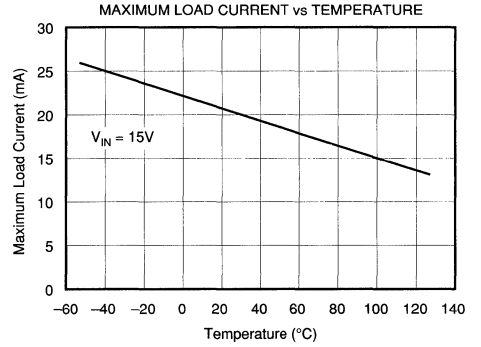
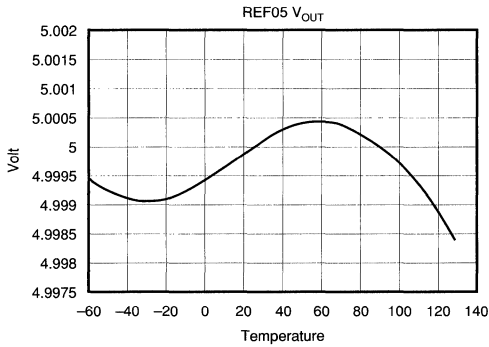
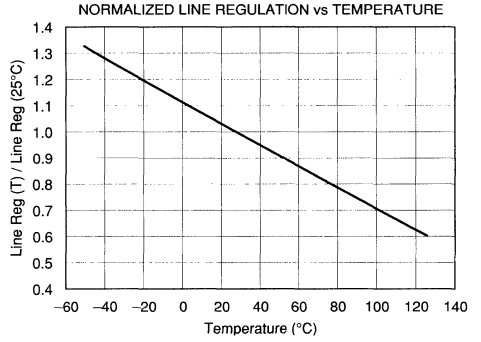
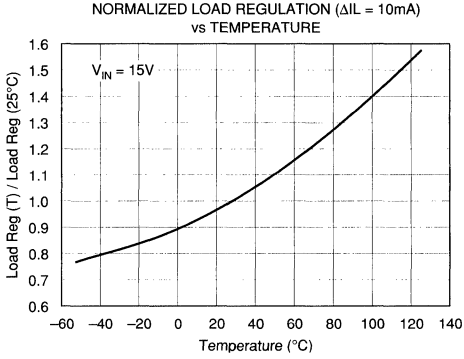
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ unless otherwise noted.



REF05

8

REFERENCES AND REGULATORS

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OUTPUT ADJUSTMENT

The REF05 trim terminal can be used to adjust the voltage over a $5V \pm 150mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V, including $5.12V^{(1)}$ for binary applications (see Figure 1).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately $0.7ppm/^{\circ}C$ for $100mV$ of output adjustment.

NOTE: (1) 20mV LSB for 8-bit applications.

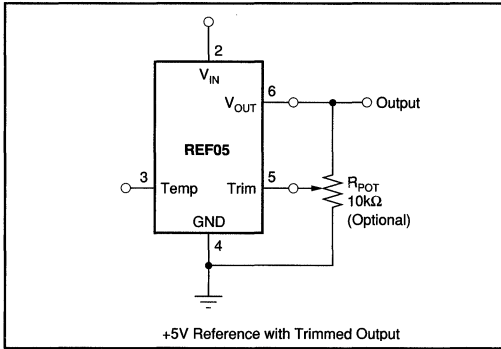


FIGURE 1.

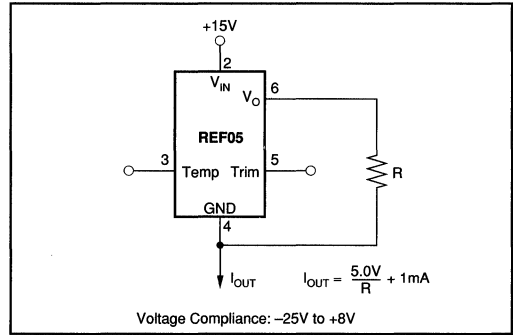


FIGURE 4. Current Source.

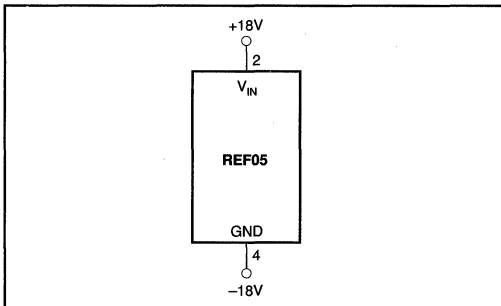


FIGURE 2. Burn-In Circuit.

TYPICAL APPLICATIONS

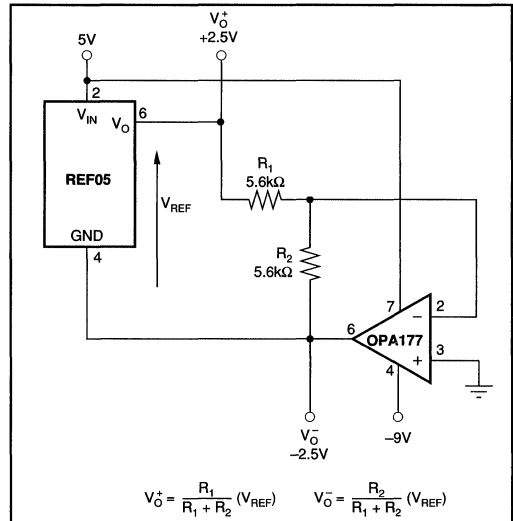


FIGURE 5. $\pm 2.5V$ Precision Reference.

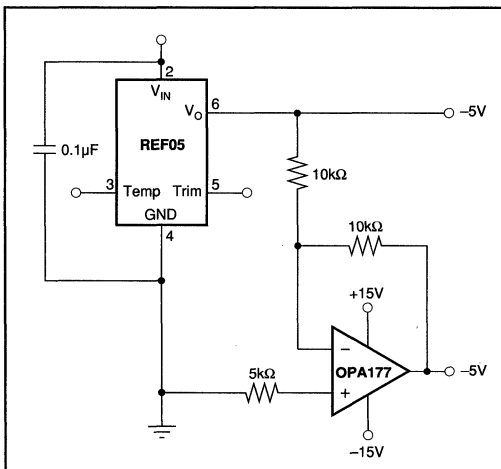


FIGURE 3. $\pm 5V$ Precision Reference.

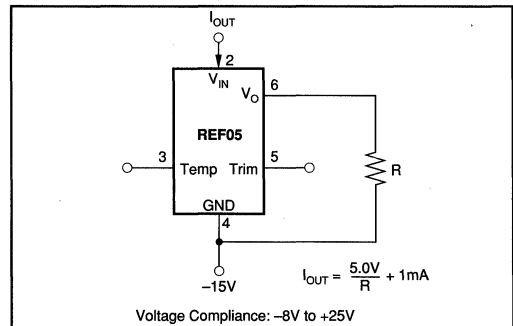


FIGURE 6. Current Sink.

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REF10

Precision VOLTAGE REFERENCE

FEATURES

- **+10.00V OUTPUT**
- **HIGH ACCURACY: $\pm 0.005V$ Untrimmed**
- **VERY-LOW DRIFT: 1ppm/°C max**
- **EXCELLENT STABILITY: 10ppm/1000hrs typ**
- **LOW NOISE: 6 μV p-p typ, 0.1Hz to 10Hz**
- **WIDE SUPPLY RANGE: Up to 35V**

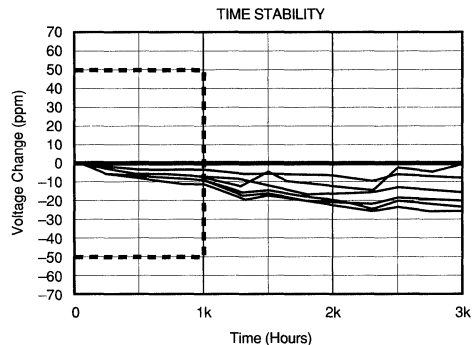
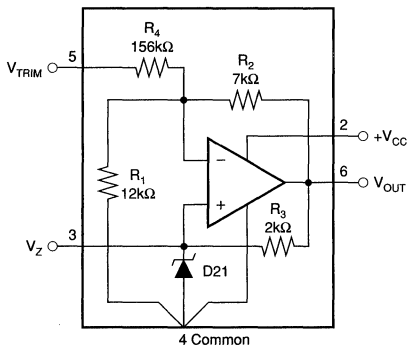
APPLICATIONS

- **PRECISION CALIBRATED VOLTAGE STANDARD**
- **TRANSDUCER EXCITATION**
- **D/A AND A/D CONVERTER REFERENCE**
- **PRECISION CURRENT REFERENCE**
- **ACCURATE COMPARATOR THRESHOLD REFERENCE**
- **DIGITAL VOLTMETERS**
- **TEST EQUIPMENT**

DESCRIPTION

The REF10 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF10 achieves its precision without a heater. This results in low quiescent current, fast warm-up, excellent stability, and low noise.

The output can be adjusted with minimal effect on drift or stability. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF10 an ideal choice for the most demanding applications such as precision system standard, D/A and A/D references, transducer excitation, etc.



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PDS-528B

8.25

REF10

REFERENCES AND REGULATORS

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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, and $\pm 15\text{VDC}$ power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF10JM, KM, RM, SM			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE					
Initial	$T_A = +25^\circ\text{C}$	9.995	10.000	10.005	V
Trim Range ⁽¹⁾		-0.100		+0.250	V
vs Temperature ⁽²⁾ : KM	0°C to $+70^\circ\text{C}$			1	ppm/ $^\circ\text{C}$
JM	0°C to $+70^\circ\text{C}$			3	ppm/ $^\circ\text{C}$
SM	-55°C to $+125^\circ\text{C}$			3	ppm/ $^\circ\text{C}$
RM	-55°C to $+125^\circ\text{C}$			6	ppm/ $^\circ\text{C}$
vs Supply (line regulation)	$V_{CC} = 13.5$ to 35V		0.001	0.002	%/V
vs Output Current (load regulation)	$I_L = 0$ to $\pm 10\text{mA}$		0.001	0.002	%/mA
vs Time ⁽³⁾	$T_A = +25^\circ\text{C}$		10	± 50	ppm/1000hr
NOISE	0.1Hz to 10Hz		6	25	$\mu\text{Vp-p}$
OUTPUT CURRENT	Source or Sink	± 10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	$I_{OUT} = 0$		4.5	6	mA
WARM-UP TIME	To 0.1%		10		μs
TEMPERATURE RANGE					
Specification: JM, KM		0		+70	$^\circ\text{C}$
RM, SM		-55		+125	$^\circ\text{C}$
Operating: JM, KM		-25		+85	$^\circ\text{C}$
RM, SM		-55		+125	$^\circ\text{C}$
Storage		-65		+125	$^\circ\text{C}$

NOTES: (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details. (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (3) Sample tested with power applied continuously.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX DRIFT (ppm/ $^\circ\text{C}$)
REF10JM	Metal TO-99	0°C to $+70^\circ\text{C}$	3
REF10KM	Metal TO-99	0°C to $+70^\circ\text{C}$	1
REF10RM	Metal TO-99	-55°C to $+125^\circ\text{C}$	6
REF10SM	Metal TO-99	-55°C to $+125^\circ\text{C}$	3

PACKAGE INFORMATION⁽¹⁾

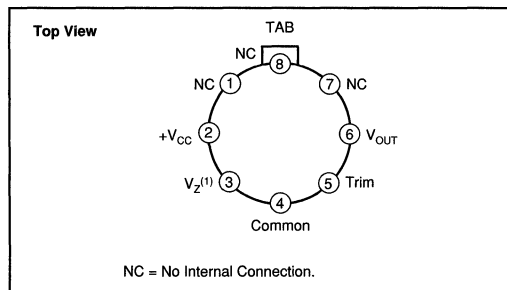
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF10JM	8-Pin Metal TO-99	001
REF10KM	8-Pin Metal TO-99	001
REF10RM	8-Pin Metal TO-99	001
REF10SM	8-Pin Metal TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Power Dissipation at $+25^\circ\text{C}$	200mW
Operating Temperature	
J, K	-25°C to $+85^\circ\text{C}$
R, S	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Short-Circuit Protection at $+25^\circ\text{C}$ to Common or $+15\text{VDC}$	Continuous

PIN CONFIGURATION



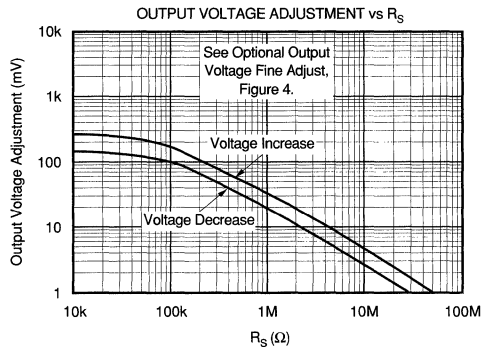
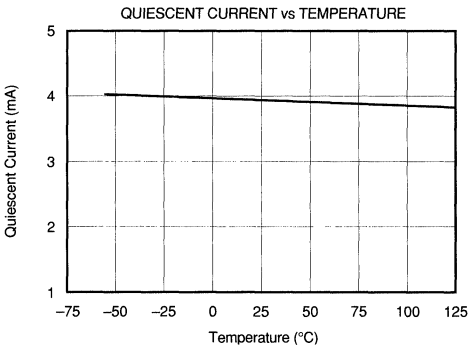
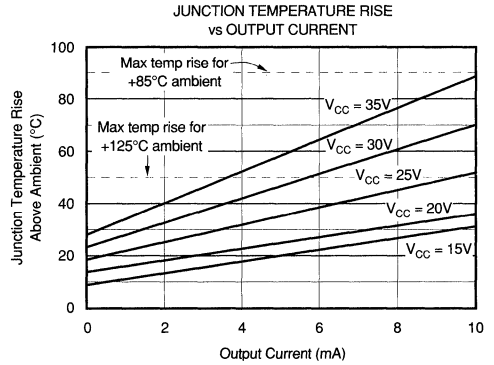
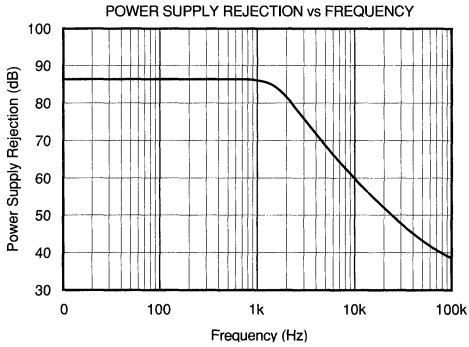
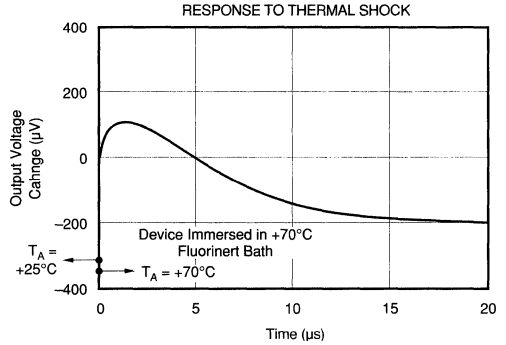
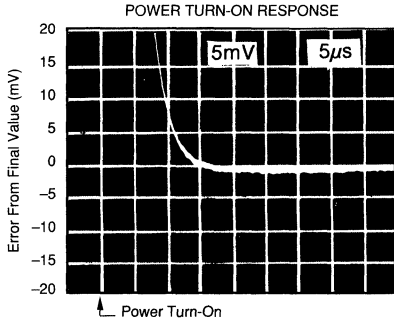
NOTE: (1) Pin 3 is an unbuffered 6.3V output. Any load will affect the output voltage and drift. A load of $1\mu\text{A}$ on pin 3 will typically change the output voltage by $50\mu\text{V}$ and the drift by $0.1\text{ppm}/^\circ\text{C}$.

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TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, and $\pm 15\text{VDC}$ power supply, unless otherwise noted.



REF10

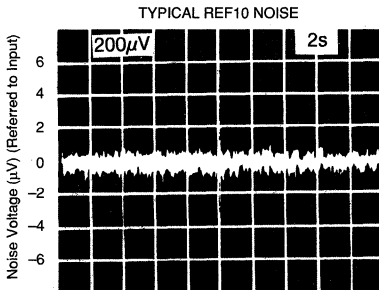
8

REFERENCES AND REGULATORS

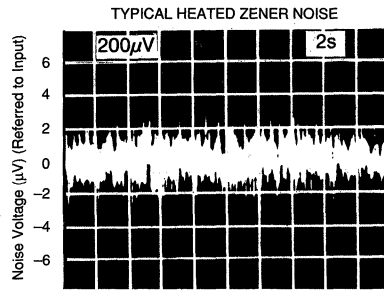
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TYPICAL PERFORMANCE CURVES (CONT)

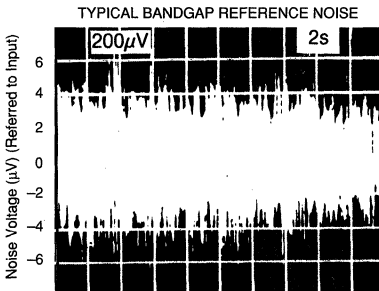
$T_A = +25^\circ\text{C}$, and $\pm 15\text{VDC}$ power supply, unless otherwise noted.



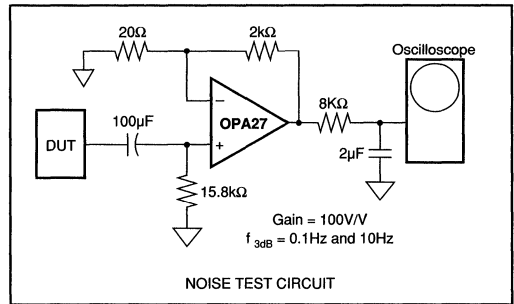
Low Frequency Noise
(see Noise Test Circuit)



Low Frequency Noise
(see Noise Test Circuit)



Low Frequency Noise
(see Noise Test Circuit)



THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode D_{z1} . This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2 : $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3 . This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1 . R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF10 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the “butterfly method” and the “box method.” The REF10 is specified with the more commonly used box method. The “box” is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF10, each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C. Each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition:

$$\left[\frac{(V_{OUT\ MAX} - V_{OUT\ MIN}) / 10V}{T_{HIGH} - T_{LOW}} \right] \times 10^6 \leq \text{Drift Specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range, T_{LOW} to T_{HIGH} , will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1).

Figure 1 uses the REF10KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The “box” height (V_1 to V_2) is 700μV, and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

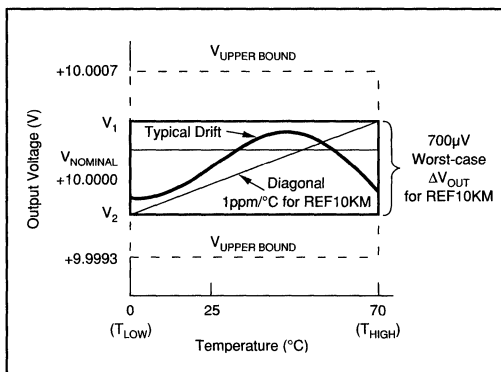


FIGURE 1. REF10KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF10. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

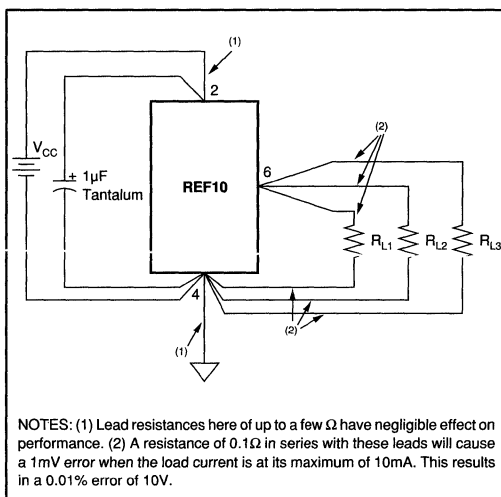


FIGURE 2. REF10 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also

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affect drift, but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 156k Ω internal resistor. A TCR of 100ppm/ $^{\circ}$ C is normally sufficient.

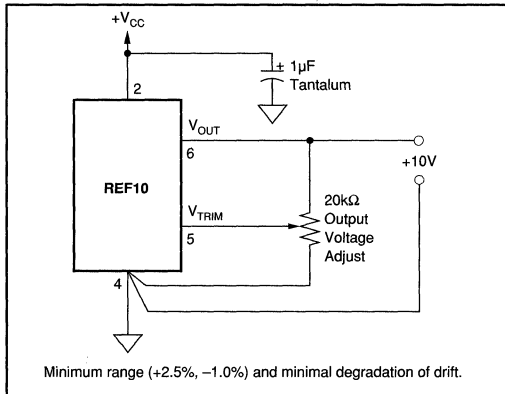


FIGURE 3. REF10 Optional Output Voltage Adjust.

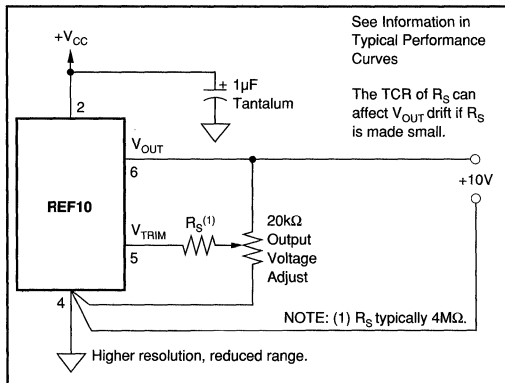


FIGURE 4. REF10 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF10 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF10 has lower output noise and much faster warm-up times than heated references, permitting high precision without extra power or additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 11.

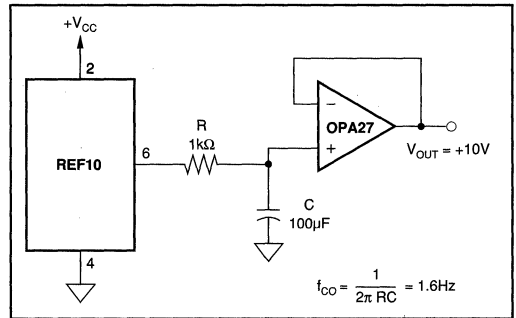


FIGURE 5. Precision Reference with Filtering.

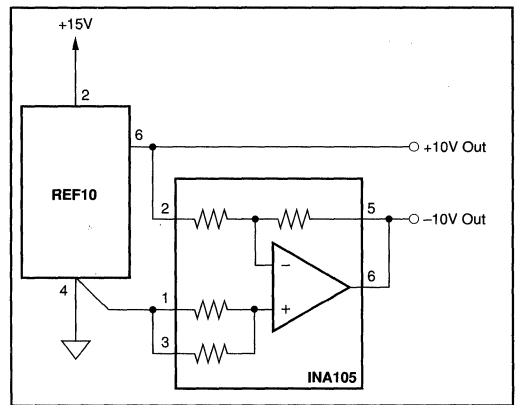


FIGURE 6. $\pm 10V$ Reference.

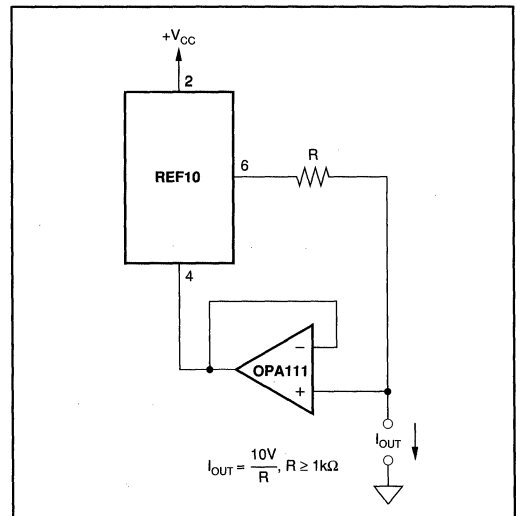


FIGURE 7. Positive Precision Current Source.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

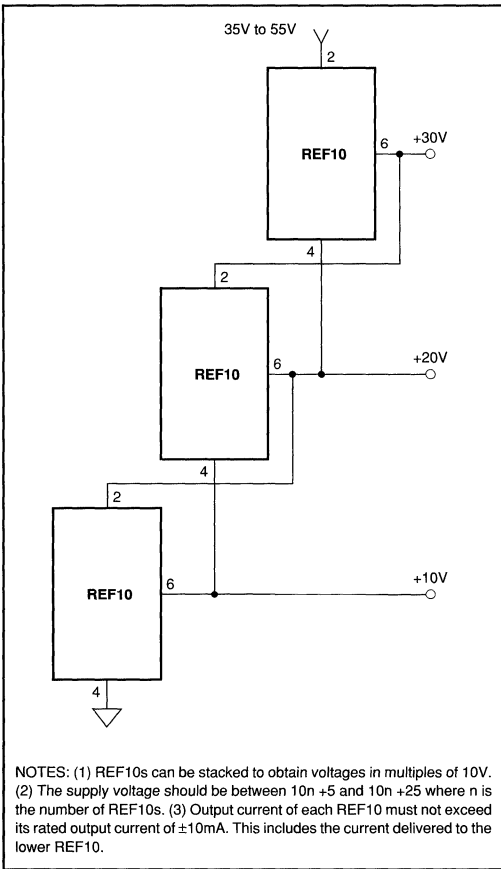


FIGURE 8. Stacked References.

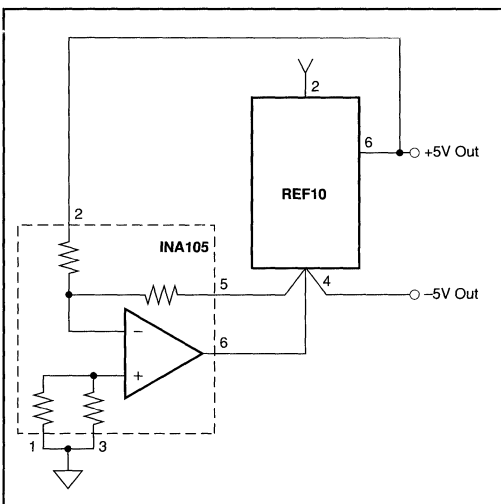


FIGURE 9. $\pm 5\text{V}$ Reference.

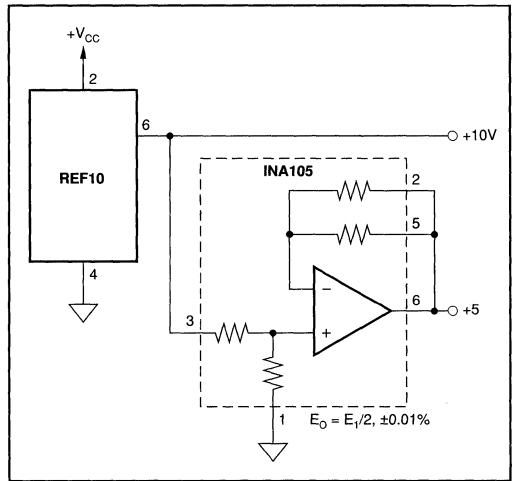


FIGURE 10. +5V and +10V Reference.

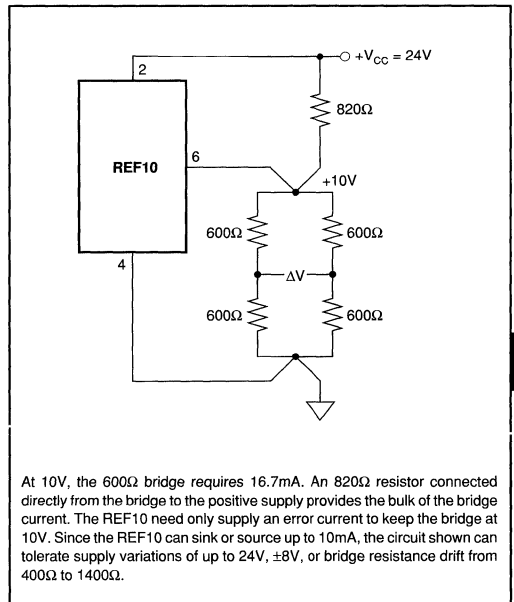


FIGURE 11. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.



REF101

Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY: $\pm 0.005V$
- VERY LOW DRIFT: 1ppm/°C max
- EXCELLENT STABILITY: 50ppm/1000hrs
- LOW NOISE: 6 μV p-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: Up to 35V
- LOW QUIESCENT CURRENT: 6mA max
- USEFUL MATCHED RESISTOR PAIR INCLUDED

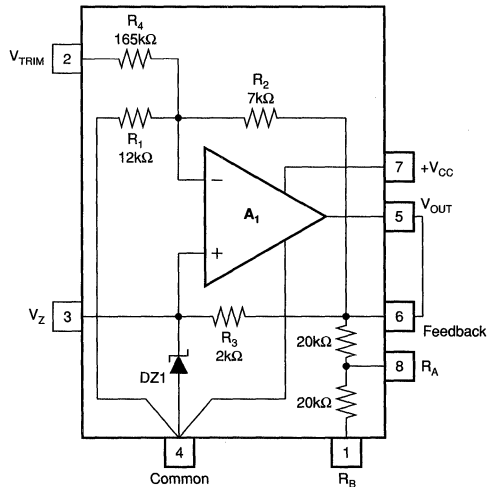
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF101 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF101 achieves its precision without a heater. This results in low quiescent current (4.5mA typ), fast warm-up (1ms to 0.1%), excellent stability (50ppm/1000hrs typ), and low noise (25 μV p-p max, 0.1Hz to 10Hz).

The output can be adjusted with minimal effect on drift or stability. Additionally, the REF101 contains a matched pair of user-accessible precision 20k Ω resistors which are useful in a variety of applications. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF101 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and +15VDC power supply, unless otherwise noted.

PARAMETER	CONDITIONS	REF101JM, KM, RM, SM			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE					
Initial	$T_A = +25^\circ\text{C}$	9.995	10.000	10.005	V
Trim Range ⁽¹⁾		-0.100		+0.250	V
vs Temperature ⁽²⁾					
KM	0°C to $+70^\circ\text{C}$			1	ppm/ $^\circ\text{C}$
JM	0°C to $+70^\circ\text{C}$			2	ppm/ $^\circ\text{C}$
SM	-55°C to $+125^\circ\text{C}$			3	ppm/ $^\circ\text{C}$
RM	-55°C to $+125^\circ\text{C}$			6	ppm/ $^\circ\text{C}$
vs Supply (line regulation)	$V_{CC} = 13.5$ to 35V		0.001	0.002	%/V
vs Output Current (load regulation)	$I_L = 0$ to $\pm 10\text{mA}$		0.001	0.002	%/mA
vs Time	$T_A = +25^\circ\text{C}$		50		ppm/1000hrs
NOISE	0.1Hz to 10Hz		6	25	$\mu\text{Vp-p}$
OUTPUT CURRENT	Source or Sink	± 10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	$I_{OUT} = 0$		4.5	6	mA
WARM-UP TIME	To 0.1%		10		μs
UNCOMMITTED RESISTORS					
Resistance Match			± 0.01	± 0.05	k Ω
TCR			50		ppm/ $^\circ\text{C}$
TCR Tracking			2		ppm/ $^\circ\text{C}$
TEMPERATURE RANGE					
Specification					
JM, KM		0		+70	$^\circ\text{C}$
RM, SM		-55		+125	$^\circ\text{C}$
Operating					
JM, KM		-25		+85	$^\circ\text{C}$
RM, SM		-55		+125	$^\circ\text{C}$
Storage				+125	$^\circ\text{C}$

NOTES : (1) Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details. (2) The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX DRIFT (ppm/ $^\circ\text{C}$)
REF101JM	Metal TO-99	0°C to $+70^\circ\text{C}$	2
REF101KM	Metal TO-99	0°C to $+70^\circ\text{C}$	1
REF101RM	Metal TO-99	-55°C to $+125^\circ\text{C}$	6
REF101SM	Metal TO-99	-55°C to $+125^\circ\text{C}$	3

PACKAGE INFORMATION⁽¹⁾

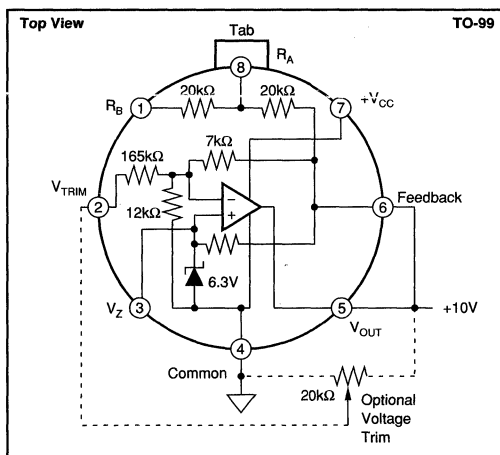
MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF101JM	Metal TO-99	001
REF101KM	Metal TO-99	001
REF101RM	Metal TO-99	001
REF101SM	Metal TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Power Dissipation at $+25^\circ\text{C}$	200mW
Operating Temperature Range	
JM, KM	-25°C to $+85^\circ\text{C}$
RM, SM	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Short-Circuit Protection at $+25^\circ\text{C}$	
To Common or +15VDC	Continuous

PIN CONFIGURATION

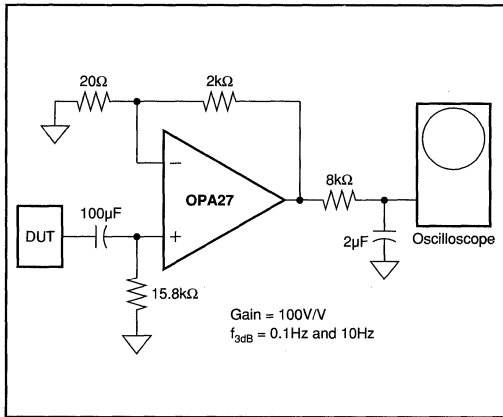


REF101

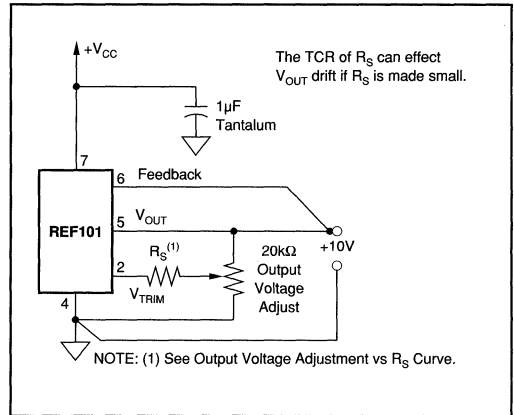
REFERENCES AND REGULATORS

For Immediate Assistance, Contact Your Local Salesperson

NOISE TEST CIRCUIT



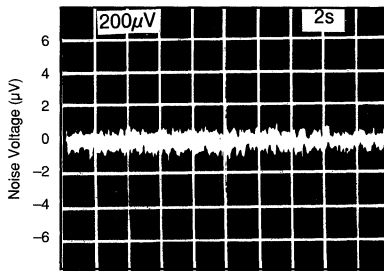
OPTIONAL OUTPUT VOLTAGE FINE ADJUSTMENT CIRCUIT



TYPICAL PERFORMANCE CURVES

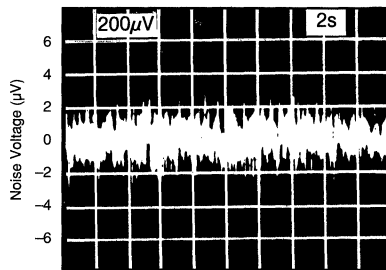
At $T_A = +25^\circ\text{C}$ and +15VDC power supply, unless otherwise noted.

TYPICAL REF101 NOISE



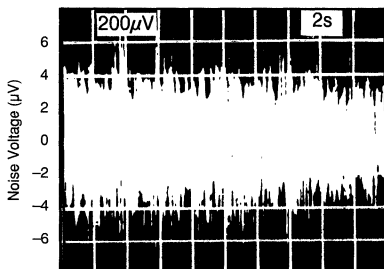
Low Frequency Noise
(see Noise Test Circuit)

TYPICAL HEATED ZENER NOISE



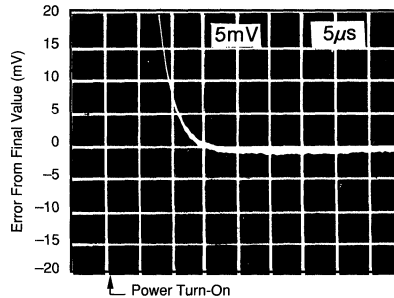
Low Frequency Noise
(see Noise Test Circuit)

TYPICAL BANDGAP REFERENCE NOISE



Low Frequency Noise
(see Noise Test Circuit)

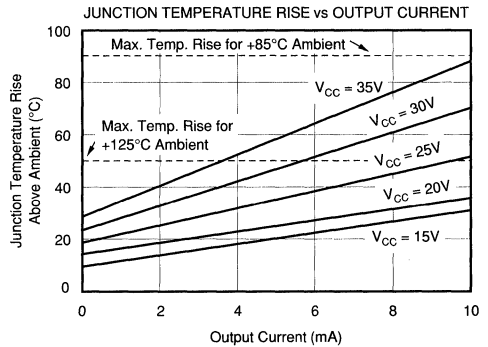
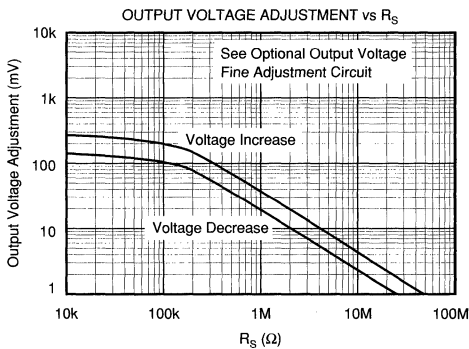
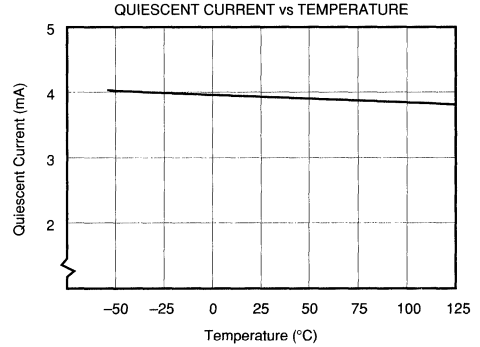
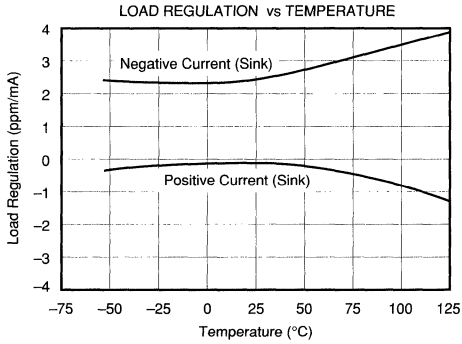
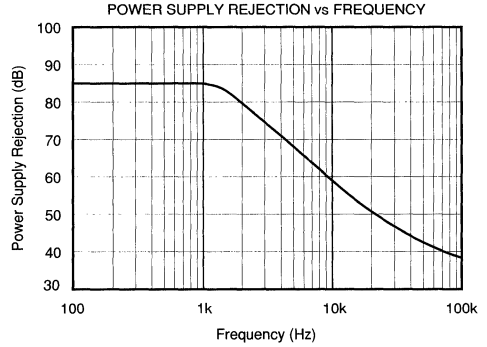
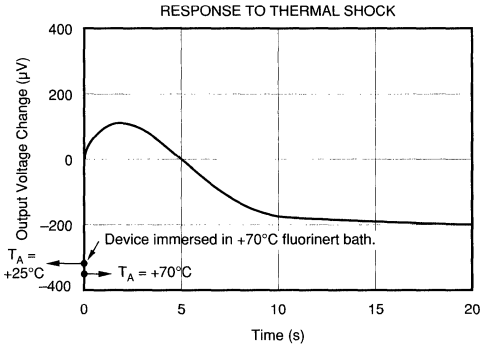
POWER TURN-ON RESPONSE



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TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$ and +15VDC power supply, unless otherwise noted.



REF101

8

REFERENCES AND REGULATORS

THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1 . This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2 : $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3 . This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1 . The adjustment of output voltage and zener current is interactive and several iterations may be used to achieve the desired results. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF101 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the “butterfly method” and the “box method”. Neither of these methods is entirely satisfactory in cases where the drift versus temperature is relatively nonlinear as is the case with most voltage references. The REF101 is specified with the more commonly used box method. The “box” is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF101, each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C, and each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition.

$$\left(\frac{V_{OUT\ MAX} - V_{OUT\ MIN}}{T_{HIGH} - T_{LOW}} \right) \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{LOW} to T_{HIGH} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1).

Figure 1 uses the REF101KM as an example. It has a drift specification of 1ppm/°C maximum and a specification

temperature range of 0°C to +70°C. The “box” height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

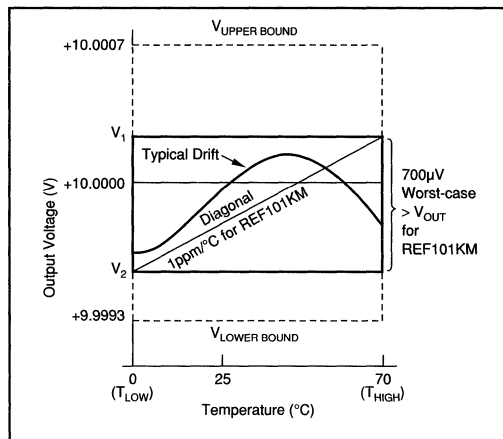
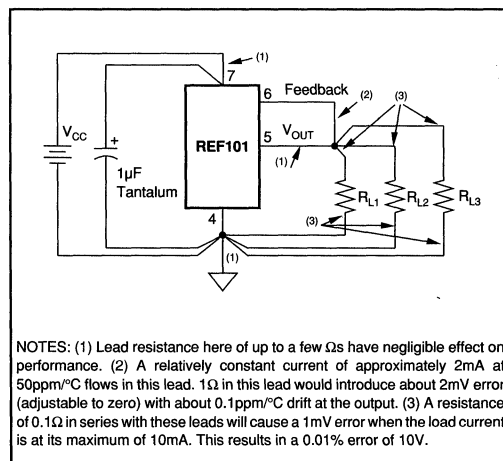


FIGURE 1. REF101KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF101. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES: (1) Lead resistance here of up to a few Ωs have negligible effect on performance. (2) A relatively constant current of approximately 2mA at 50ppm/°C flows in this lead. 1Ω in this lead would introduce about 2mV error (adjustable to zero) with about 0.1ppm/°C drift at the output. (3) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF101 Basic Circuit Connection.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01 ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 165k Ω internal resistor. A TCR of 100ppm/°C is normally sufficient.

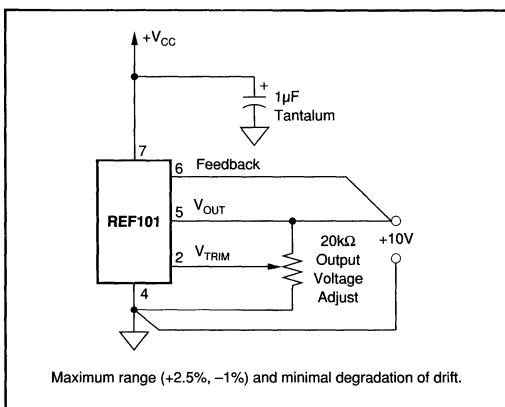


FIGURE 3. REF101 Optional Output Voltage Adjustment.

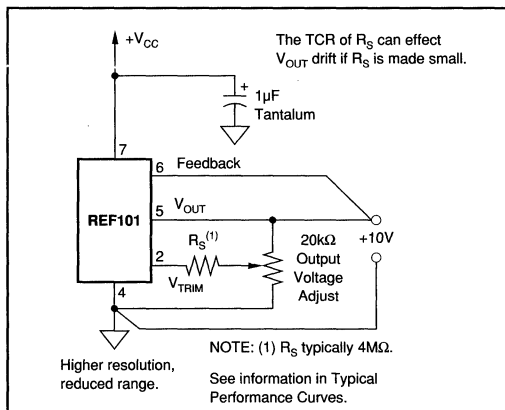


FIGURE 4. REF101 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF101 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF101 has lower output noise and much faster warm-up times (1ms to 0.1%) than heated references, permitting high precision without extra power from additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 19.

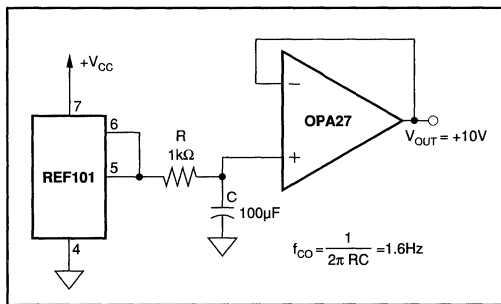


FIGURE 5. Precision Reference with Filtering.

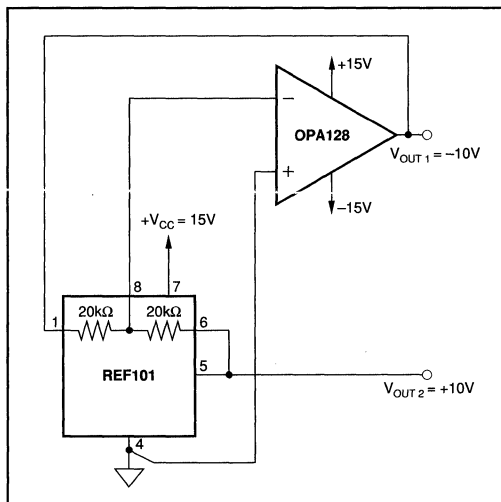


FIGURE 6. ±10V Reference.

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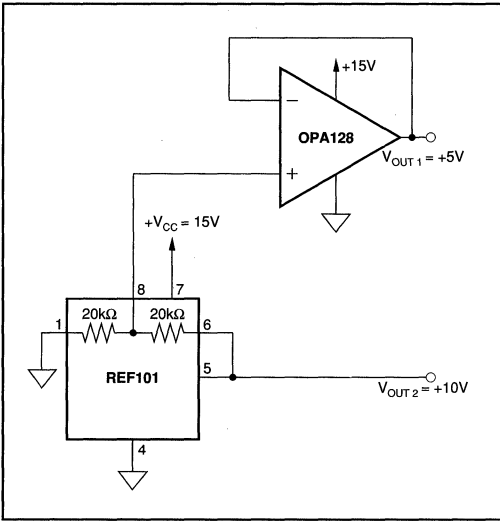


FIGURE 7. +10V and +5V Reference.

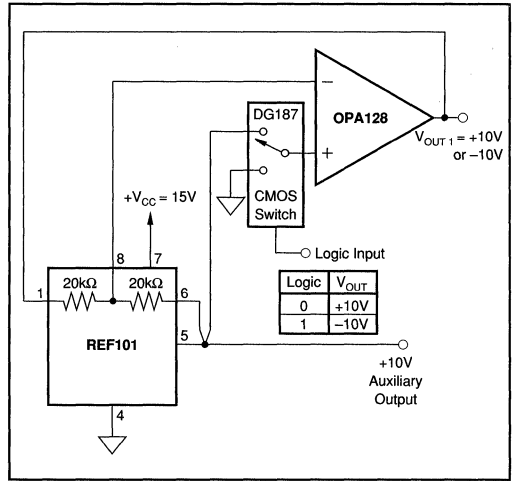


FIGURE 9. Digitally-Controlled Bipolar Precision Reference.

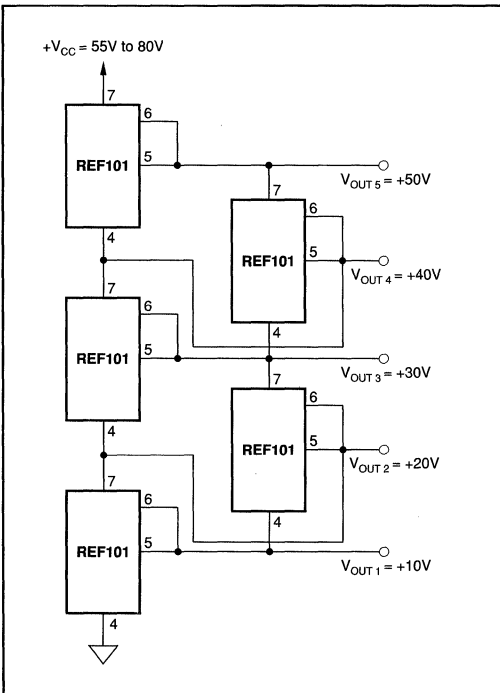


FIGURE 8. Stacked References.

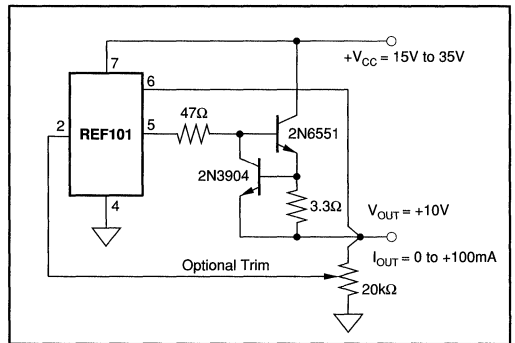


FIGURE 10. +10V Reference with Boosted Output Current to 100mA.

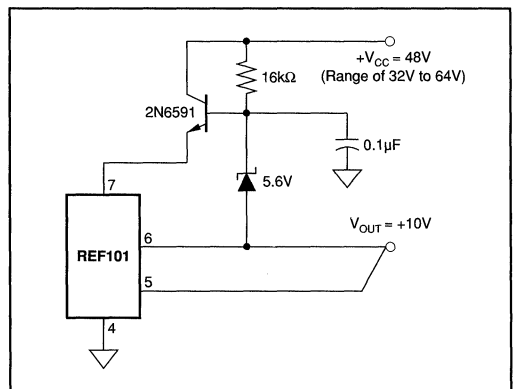


FIGURE 11. +10V Reference with Input Voltage Boost for 48V Operation.

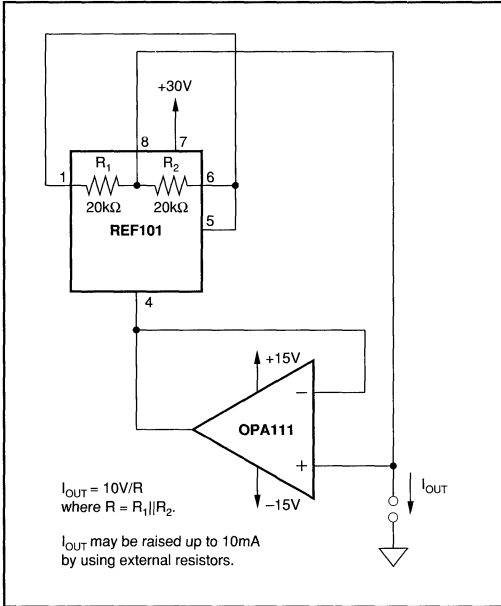


FIGURE 12. Positive Precision 1mA Current Source.

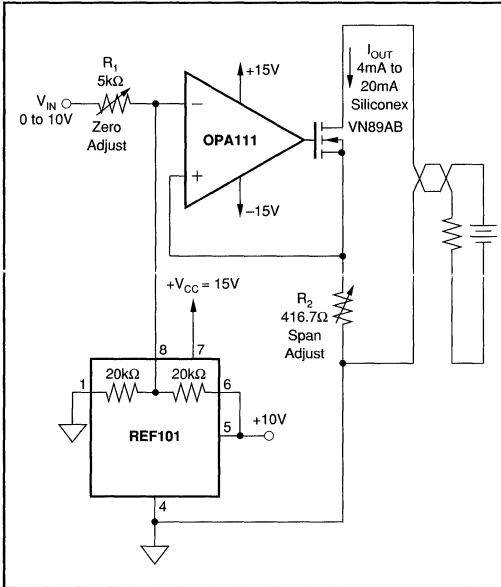


FIGURE 13. 4mA to 20mA Precision Current Transmitter.

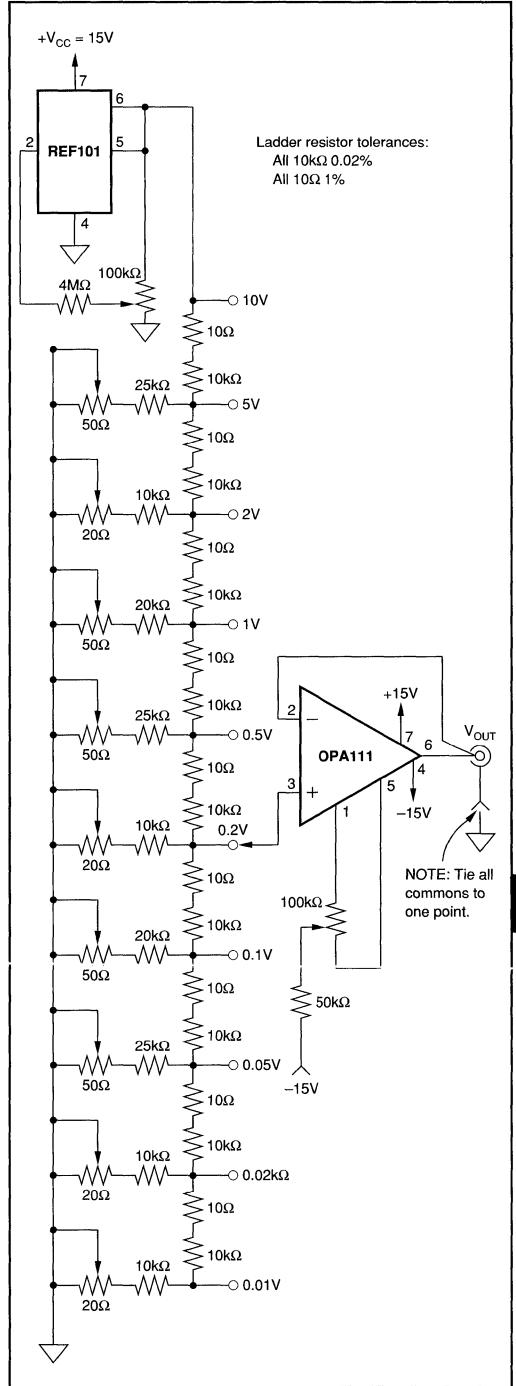


FIGURE 14. Precision Voltage Calibrator.

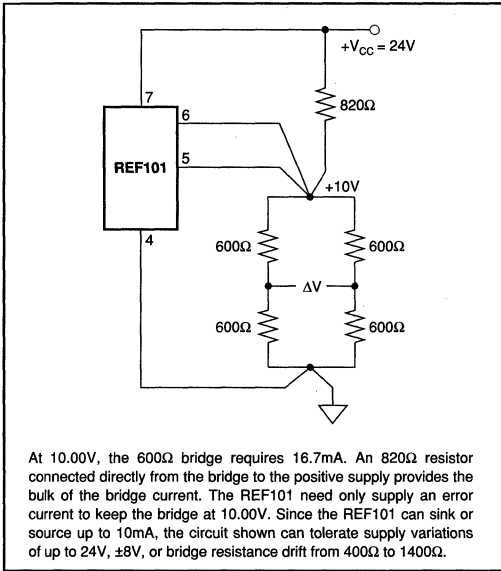


FIGURE 15. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

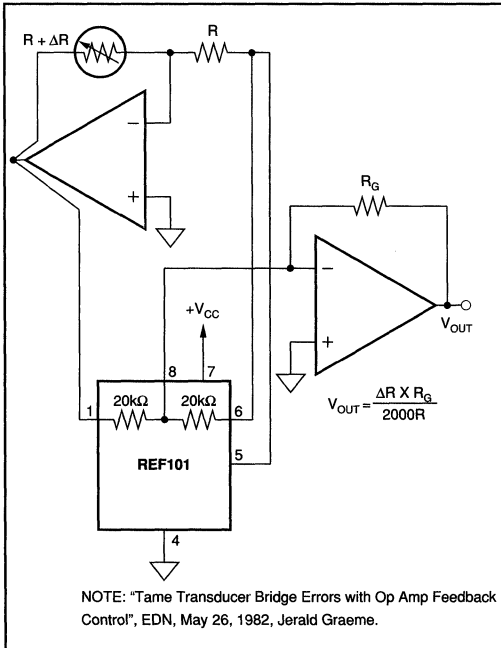


FIGURE 16. Linear Bridge Circuit Using Internal Precision Resistors of the REF101 as the Bridge Completion Network.

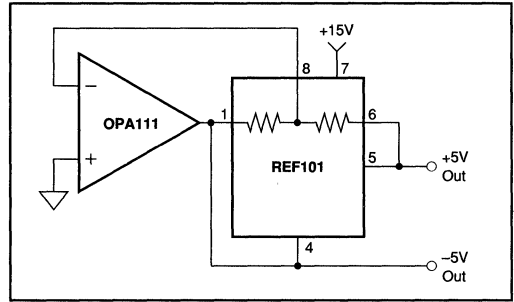


FIGURE 17. ±5V Reference.

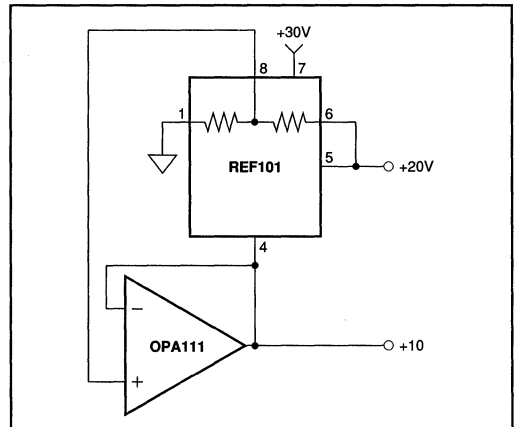


FIGURE 18. +10V and +20V Reference.

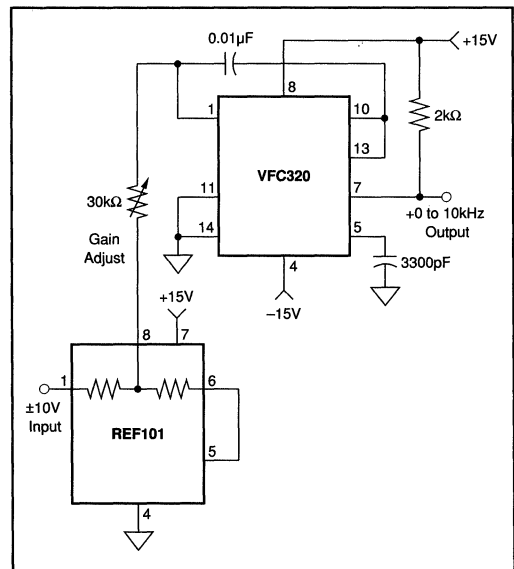
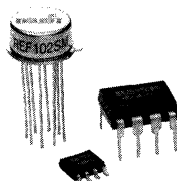


FIGURE 19. Bipolar Input Voltage-to-Frequency Converter.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



REF102

Precision VOLTAGE REFERENCE

FEATURES

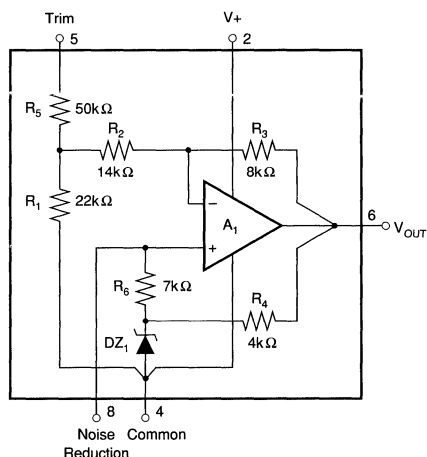
- **+10V \pm 0.0025V OUTPUT**
- **VERY LOW DRIFT: 2.5ppm/ $^{\circ}$ C max**
- **EXCELLENT STABILITY: 5ppm/1000hr typ**
- **EXCELLENT LINE REGULATION: 1ppm/V max**
- **EXCELLENT LOAD REGULATION: 10ppm/mA max**
- **LOW NOISE: 5 μ Vp-p typ, 0.1Hz to 10Hz**
- **WIDE SUPPLY RANGE: 11.4VDC to 36VDC**
- **LOW QUIESCENT CURRENT: 1.4mA max**
- **PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC**

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/ $^{\circ}$ C max (CM grade) over the industrial temperature range and 5ppm/ $^{\circ}$ C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low-power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.

APPLICATIONS

- **PRECISION-CALIBRATED VOLTAGE STANDARD**
- **D/A AND A/D CONVERTER REFERENCE**
- **PRECISION CURRENT REFERENCE**
- **ACCURATE COMPARATOR THRESHOLD REFERENCE**
- **DIGITAL VOLTMETERS**
- **TEST EQUIPMENT**
- **PC-BASED INSTRUMENTATION**



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PDS-900D

8.41

REF102

8

REFERENCES AND REGULATORS

For Immediate Assistance, Contact Your Local Salesperson

SPECIFICATIONS

ELECTRICAL

At $T_A = +25^\circ\text{C}$ and $V_S = +15\text{V}$ power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF102A, R			REF102B, S			REF102C, M			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	$T_A = 25^\circ\text{C}$	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature ⁽¹⁾				10			5			2.5	ppm/°C
vs Supply (Line Regulation)	$V_S = 11.4\text{V to }36\text{V}$			2			1			1	ppm/V
vs Output Current (Load Regulation)	$I_L = 0\text{mA to }+10\text{mA}$ $I_L = 0\text{mA to }-5\text{mA}$ $T_A = 25^\circ$			20			10			10	ppm/mA
				40			20			20	ppm/mA
vs Time											
M Package			5			*			*		ppm/1000hr
P, U Packages ⁽²⁾			20			*			*		ppm/1000hr
Trim Range ⁽³⁾		±3			*			*			%
Capacitive Load, max			1000		*			*			pF
NOISE	(0.1Hz to 10Hz)		5			*			*		μVp-p
OUTPUT CURRENT		+10, -5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	($I_{\text{out}} = 0$)			+1.4			*			*	mA
WARM-UP TIME ⁽⁴⁾	(To 0.1%)		15			*			*		μs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		-25		+85	*		*	*		*	°C
REF102R, S		-55		+125	*		*				°C

*Specifications same as REF102A/R.

NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

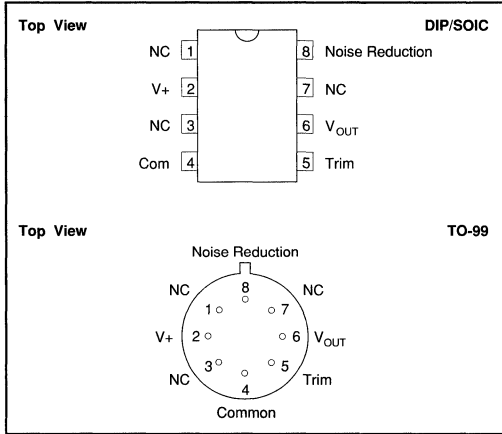
The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	MAX INITIAL ERROR (mV)	MAX DRIFT (ppm/°C)
REF102AU	8-Pin SOIC	-25°C to +85°C	±10	±10
REF102AP	8-Pin Plastic DIP	-25°C to +85°C	±10	±10
REF102BP	8-Pin Plastic DIP	-25°C to +85°C	±5	±5
REF102AM	Metal TO-99	-25°C to +85°C	±10	±10
REF102BM	Metal TO-99	-25°C to +85°C	±5	±5
REF102CM	Metal TO-99	-25°C to +85°C	±2.5	±2.5
REF102RM	Metal TO-99	-55°C to +125°C	±10	±10
REF102SM	Metal TO-99	-55°C to +125°C	±5	±5

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Input Voltage	+40V
Operating Temperature	
P,U	-25°C to +85°C
M	-55°C to +125°C
Storage Temperature Range	
P,U	-40°C to +85°C
M	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
(SOIC, 3s)	+260°C
Short-Circuit Protection to Common or V+	Continuous

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF102AU	8-Pin SOIC	182
REF102AP	8-Pin Plastic DIP	006
REF102BP	8-Pin Plastic DIP	006
REF102AM	Metal-TO-99	001
REF102BM	Metal-TO-99	001
REF102CM	Metal-TO-99	001
REF102RM	Metal-TO-99	001
REF102SM	Metal-TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

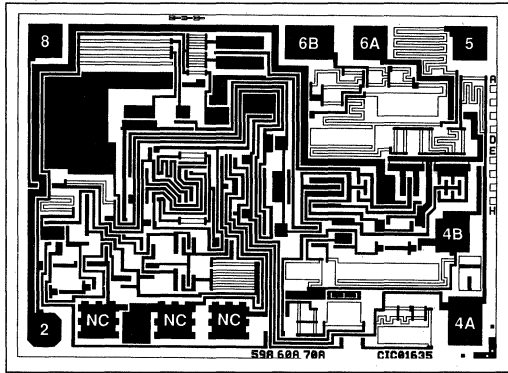
REF102

8

REFERENCES AND REGULATORS

For Immediate Assistance, Contact Your Local Salesperson

DICE INFORMATION



REF102 DIE TOPOGRAPHY

PAD	FUNCTION
2	V _{CC}
3A	NC
3B	NC
3C	NC
4A	Common (Sense)
4B	Common (Force)
5	Trim
6A	V _{OUT}
6B	V _{OUT} (Feedback)
8	Noise Reduction

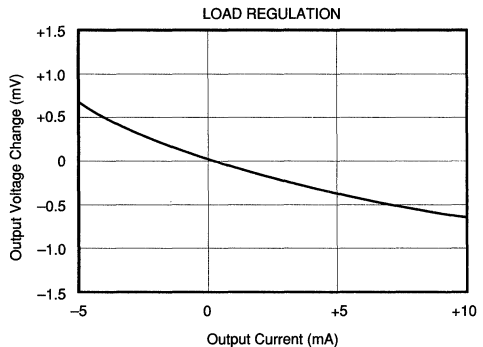
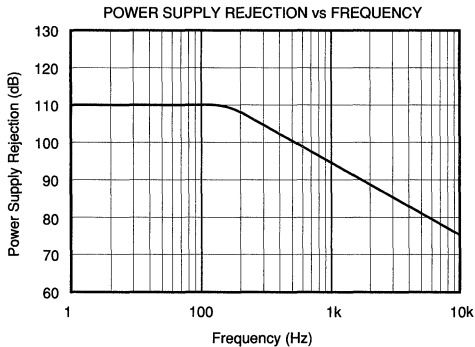
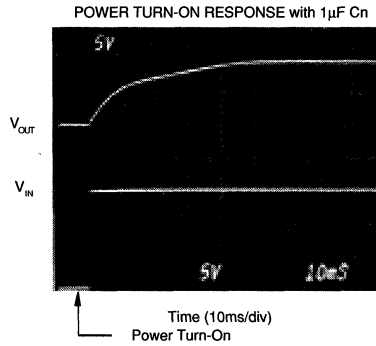
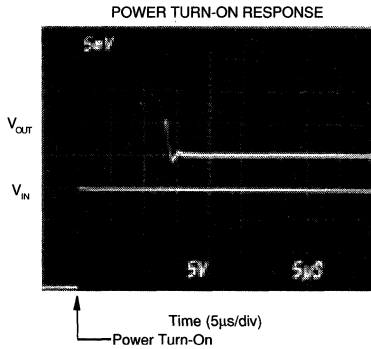
Substrate Bias: -V_{CC}.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	55 x 75 ±5	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

TYPICAL PERFORMANCE CURVES

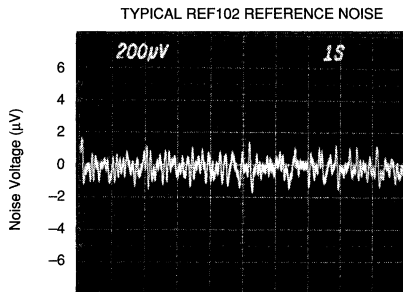
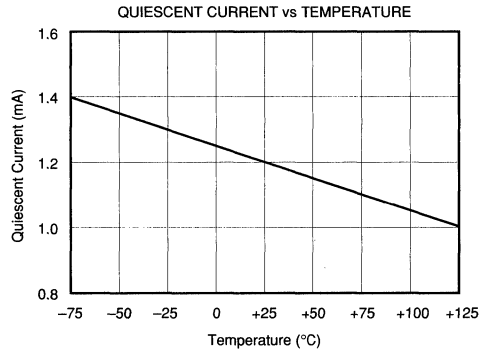
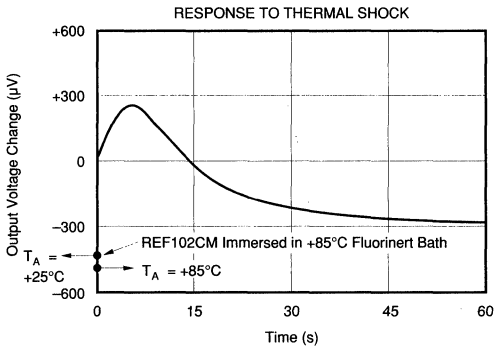
T_A = +25°C, V_S = +15V unless otherwise noted.



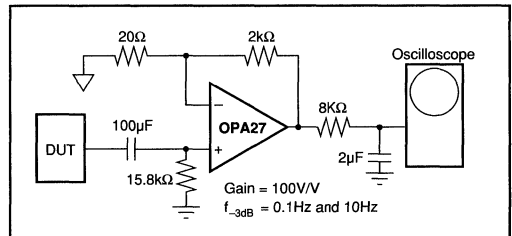
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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = +15\text{V}$ unless otherwise noted.



Low Frequency Noise (1s/div)
(See Noise Test Circuit)



Noise Test Circuit.

REF102

REFERENCES AND REGULATORS

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1 , op amp A_1 , and resistor network R_1 – R_6 .

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1 . R_1 , R_2 , and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4 . R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R_5 closely matches the TCR of R_1 , R_2 and R_3 , the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the “butterfly method” and the “box method.” The REF102 is specified with the more commonly used “box method.” The “box” is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The “box” height, V_1 to V_2 , is 2.75mV.

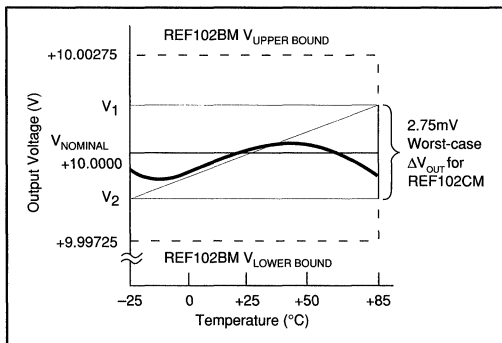


FIGURE 1. REF102CM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power-supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

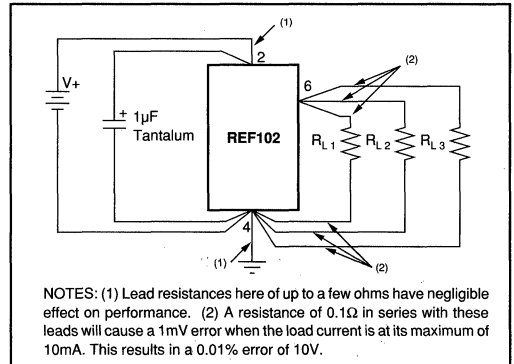


FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ± 300 mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_5 and the internal resistors can introduce some slight drift. This effect is minimized if R_5 is kept significantly larger than the 50k Ω internal resistor. A TCR of 100ppm/°C is normally sufficient.

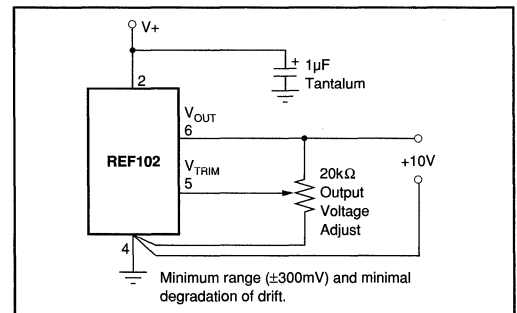


FIGURE 3. REF102 Optional Output Voltage Adjust.

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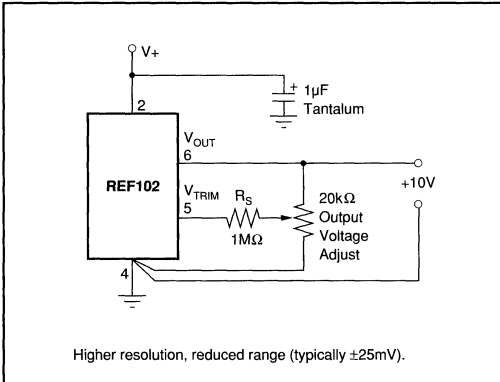


FIGURE 4. REF102 Optional Output Voltage Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with R_6 (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a $1\mu\text{F}$ noise reduction capacitor on the high frequency noise of the REF102. R_6 is typically $7\text{k}\Omega$ so the filter has a -3dB frequency of about 22Hz . The result is a reduction in noise from about $800\mu\text{Vp-p}$ to under $200\mu\text{Vp-p}$. If further noise reduction is required, use the circuit in Figure 14.

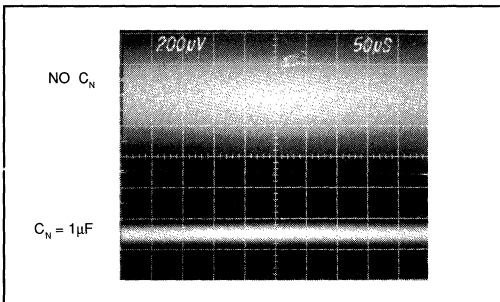


FIGURE 5. Effect of $1\mu\text{F}$ Noise Reduction Capacitor on Broadband Noise ($f_{-3\text{dB}} = 1\text{MHz}$).

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

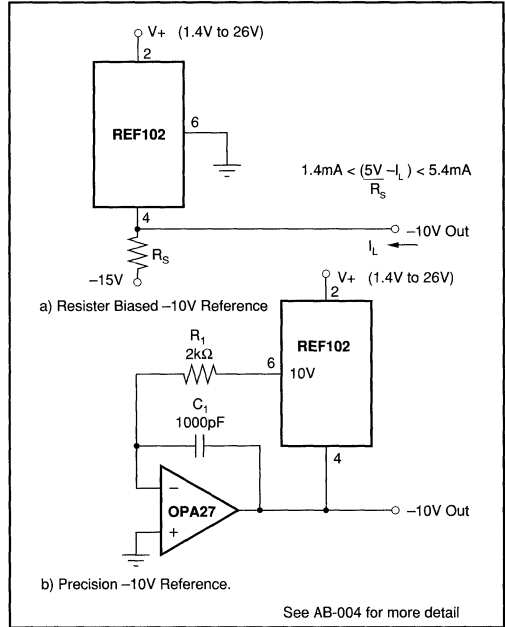


FIGURE 6. -10V Reference Using a) Resistor or b) OPA27.

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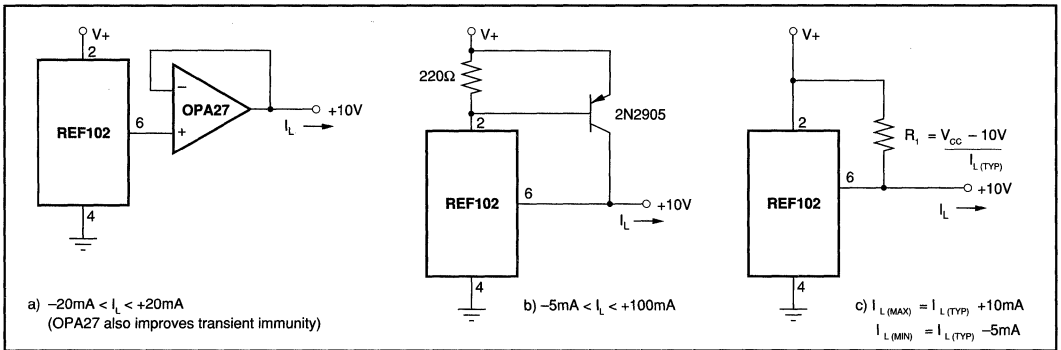


FIGURE 7. +10V Reference With Output Current Boosted to: a) $\pm 20\text{mA}$, b) $+100\text{mA}$, and c) $I_{L(\text{TYP})} + 10\text{mA}$, -5mA .

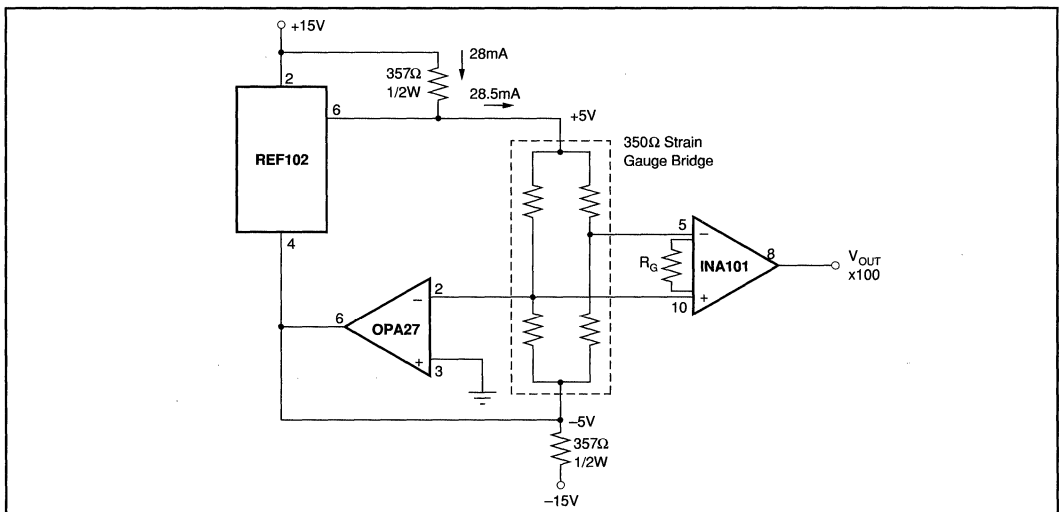


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

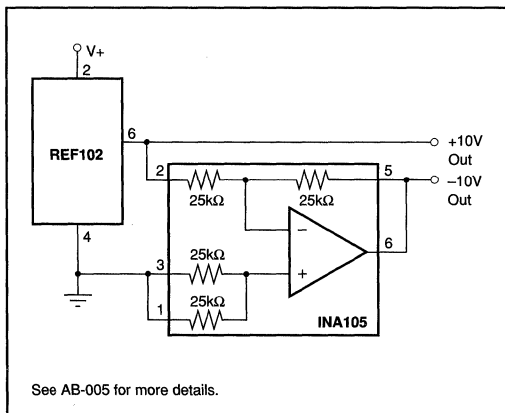


FIGURE 9. $\pm 10\text{V}$ Reference.

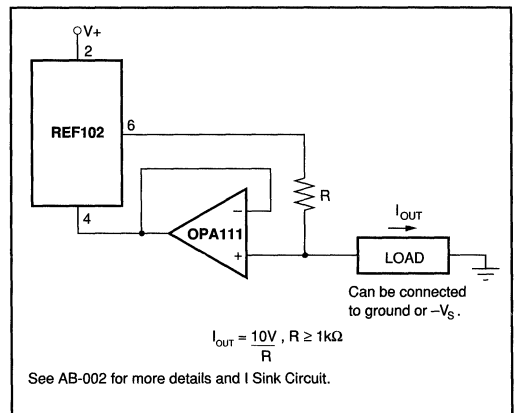


FIGURE 10. Positive Precision Current Source.

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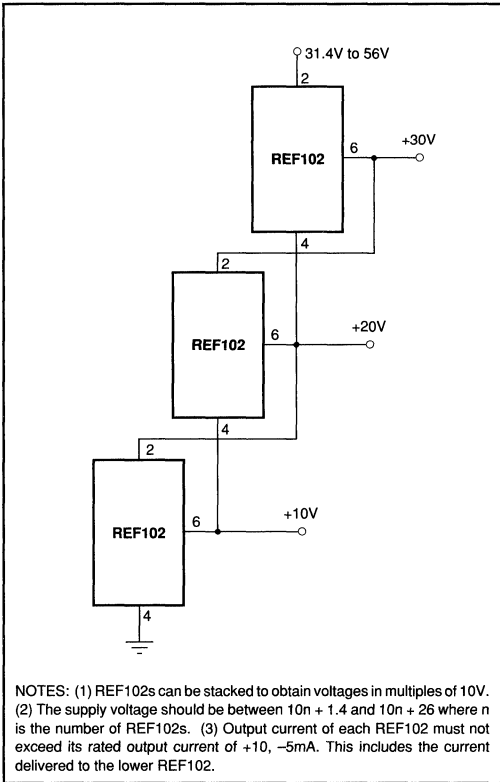


FIGURE 11. Stacked References.

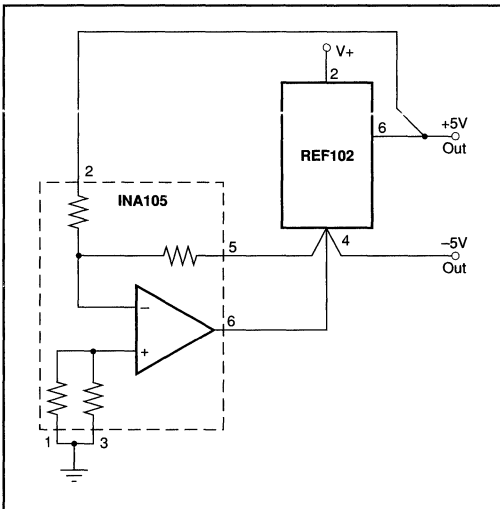


FIGURE 12. ±5V Reference.

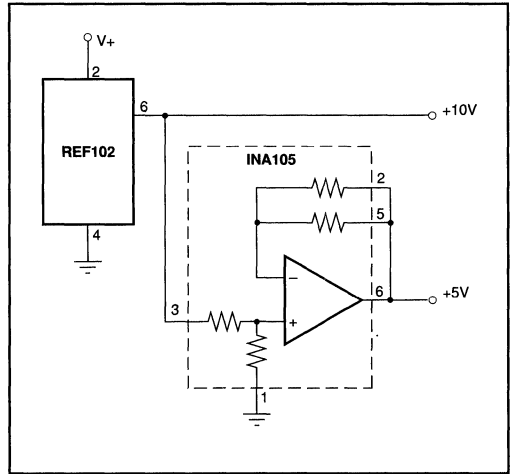


FIGURE 13. +5V and +10V Reference.

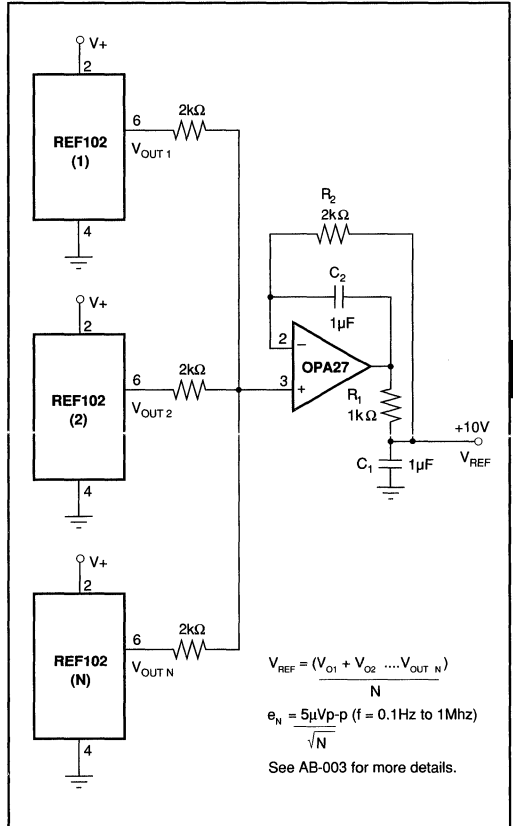
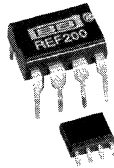


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

REF102

REFERENCES AND REGULATORS

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REF200

DUAL CURRENT SOURCE/CURRENT SINK

FEATURES

- COMPLETELY FLOATING:
No Power Supply or Ground Connections
- HIGH ACCURACY: $100\mu\text{A} \pm 0.5\%$
- LOW TEMPERATURE COEFFICIENT:
 $\pm 25\text{ppm}/^\circ\text{C}$
- WIDE VOLTAGE COMPLIANCE:
2.5V to 40V
- ALSO INCLUDES CURRENT MIRROR

APPLICATIONS

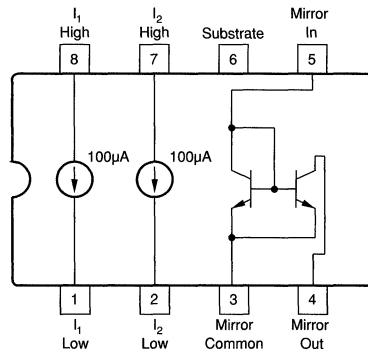
- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two $100\mu\text{A}$ current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of $50\mu\text{A}$, $100\mu\text{A}$, $200\mu\text{A}$, $300\mu\text{A}$ or $400\mu\text{A}$. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP and SOIC packages.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

Or, Call Customer Service at 1-800-548-6132 (USA Only)

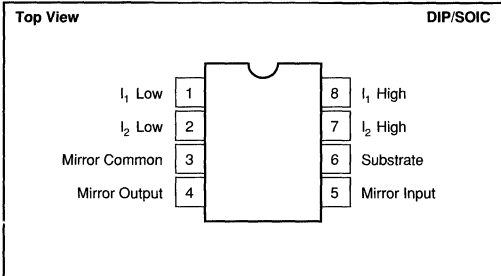
SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$, $V_S = 15\text{V}$ unless otherwise noted.

PARAMETER	CONDITION	REF200AP, AU			UNITS
		MIN	TYP	MAX	
CURRENT SOURCES					
Current Accuracy			± 0.25	± 1	%
Current Match			± 0.25	± 1	%
Temperature Drift	Specified Temp Range		25		ppm/ $^\circ\text{C}$
Output Impedance	2.5V to 40V	20	100		M Ω
	3.5V to 30V	200	500		M Ω
Noise	BW = 0.1Hz to 10Hz $f = 10\text{kHz}$		1		nA-p-p
Voltage Compliance (1%)	T_{MIN} to T_{MAX}		20	See Curves	pA/ $\sqrt{\text{Hz}}$
Capacitance			10		pF
CURRENT MIRROR					
Gain	$I = 100\mu\text{A}$ Unless Otherwise Noted	0.995	1	1.005	
Temperature Drift			25		ppm/ $^\circ\text{C}$
Impedance (output)	2V to 40V	40	100		M Ω
Nonlinearity	$I = 0\mu\text{A}$ to $250\mu\text{A}$		0.05		%
Input Voltage			1.4		V
Output Compliance Voltage			See Curves		
Frequency Response (-3dB)	Transfer		5		MHz
TEMPERATURE RANGE					
Specification		-25		+85	$^\circ\text{C}$
Operating		-40		+85	$^\circ\text{C}$
Storage		-40		+125	$^\circ\text{C}$

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Applied Voltage	-6V to +40V
Reverse Current	-350 μA
Voltage Between Any Two Sections	$\pm 80\text{V}$
Operating Temperature	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
Storage Temperature	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$
(SOIC 3s)	+260 $^\circ\text{C}$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF200AP	8-Pin Plastic DIP	006
REF200AU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL ⁽¹⁾	TEMPERATURE PACKAGE	RANGE
REF200AP	8-Pin Plastic DIP	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$
REF200AU	8-Pin Plastic SOIC	-25 $^\circ\text{C}$ to +85 $^\circ\text{C}$

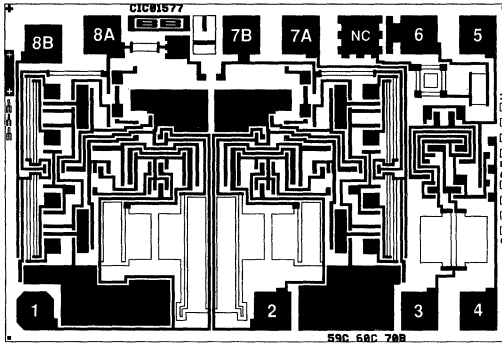
NOTE: (1) Grade designation "A" may not be marked. Absence of grade designation indicates A grade.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.



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DICE INFORMATION



REF200 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	I ₁ Low	6	Substrate
2	I ₂ Low	7A	I ₁ High
3	Mirror Common	7B	I ₁ High
4	Mirror Output	8A	I ₁ High
5	Mirror Input	8B	I ₁ High

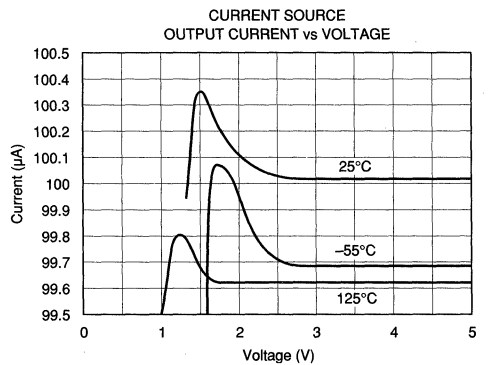
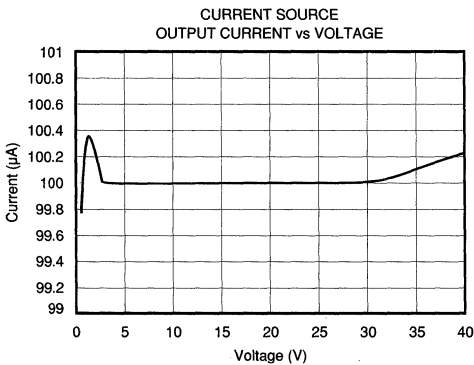
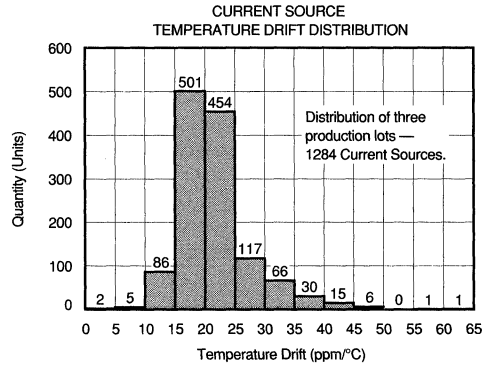
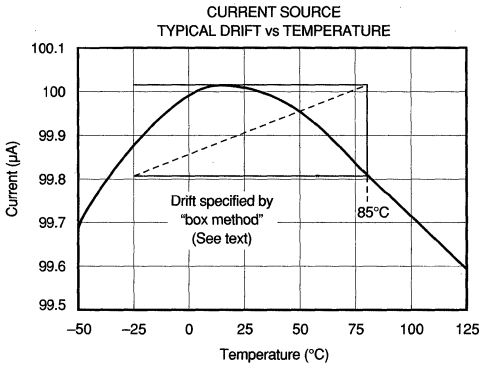
Substrate Bias: -V_{CC}

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	48 x 72 ±5	1.22 x 1.83 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None

TYPICAL PERFORMANCE CURVES

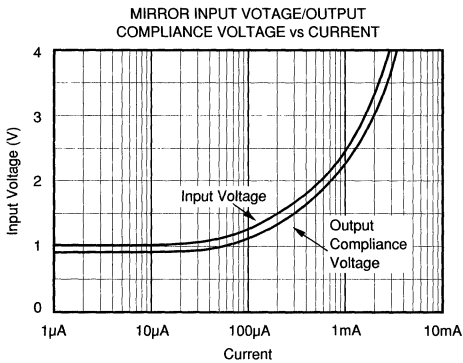
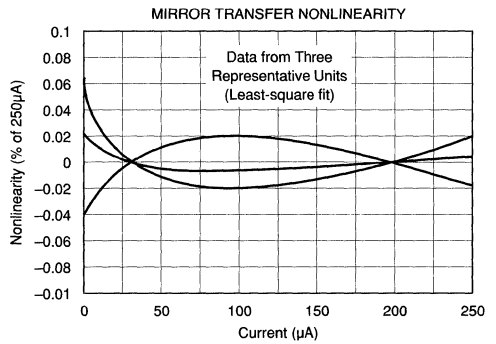
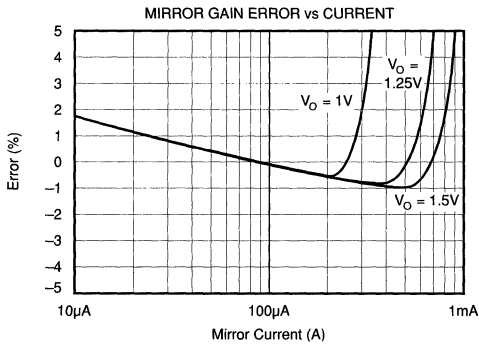
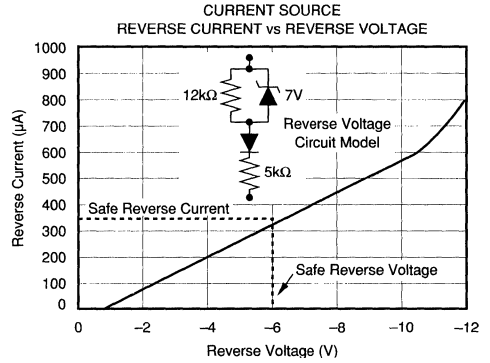
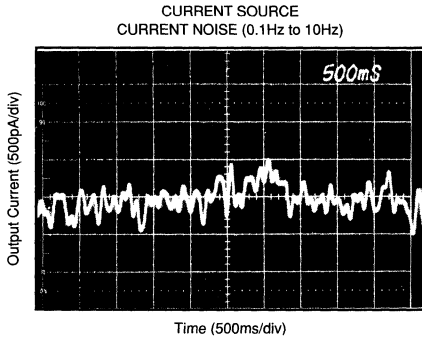
T_A = +25°C, V_S = +15V unless otherwise noted.



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TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = +15\text{V}$ unless otherwise noted.



REF200

8

REFERENCES AND REGULATORS

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APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in your system. In most analog systems this would be $-V_s$. For best AC performance, leave pin 6 open and leave unused sections unconnected.

Drift performance is specified by the "box method," as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from -25°C to $+85^{\circ}\text{C}$.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage curve. If reverse voltage is limited to less than 6V or reverse current is limited to less than $350\mu\text{A}$, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. Application guide AN-165 shows additional REF200 circuits as well as other related current source techniques. A collection of circuits is shown to illustrate some techniques. Also, see AN-165A.

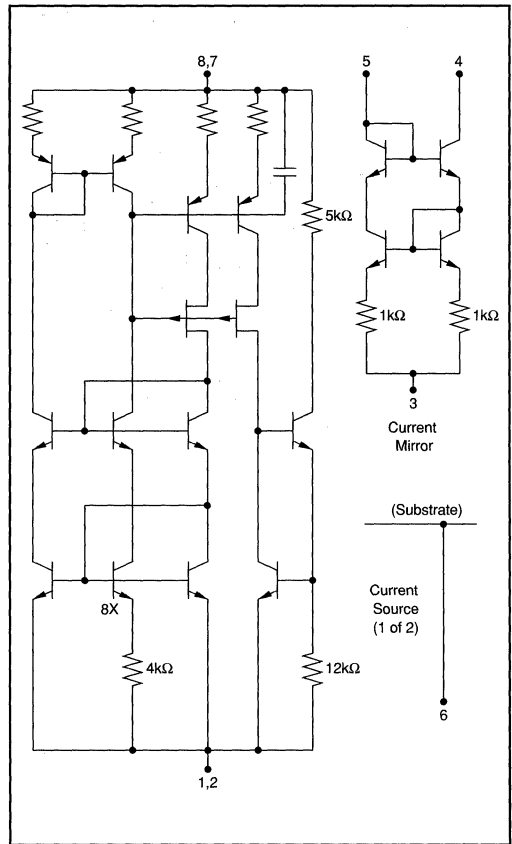


FIGURE 1. Simplified Circuit Diagram.

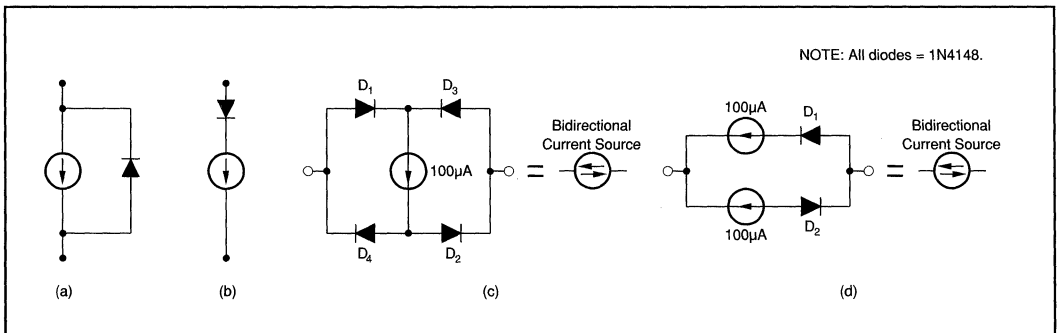


FIGURE 2. Reverse Voltage Protection.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

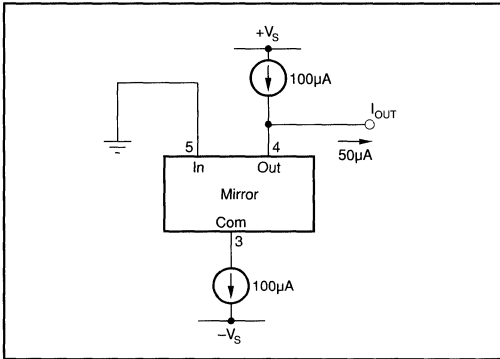


FIGURE 3. 50µA Current Source.

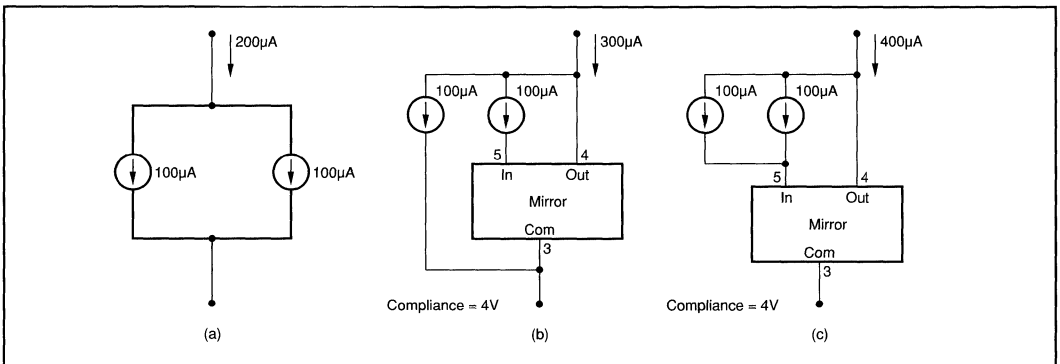


FIGURE 4. 200µA, 300µA, and 400µA Floating Current Sources.

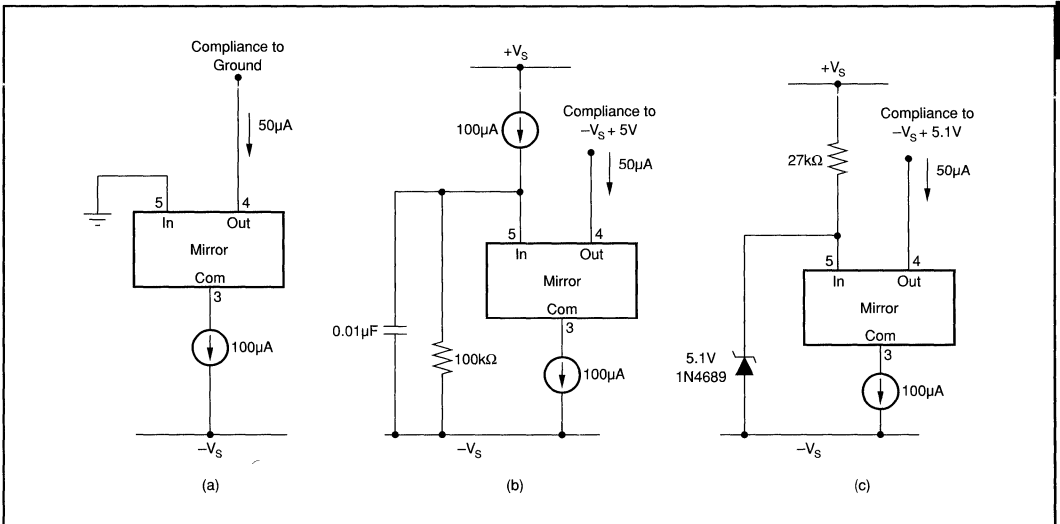


FIGURE 5. 50µA Current Sinks.

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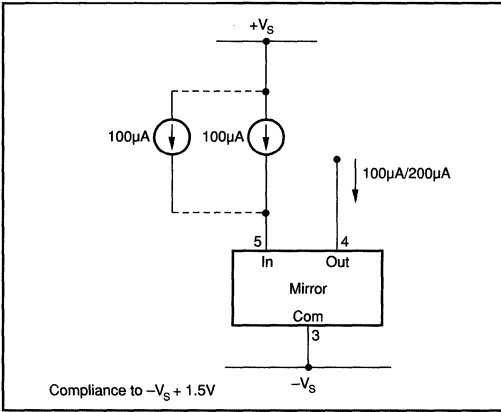


FIGURE 6. Improved Low-Voltage Compliance.

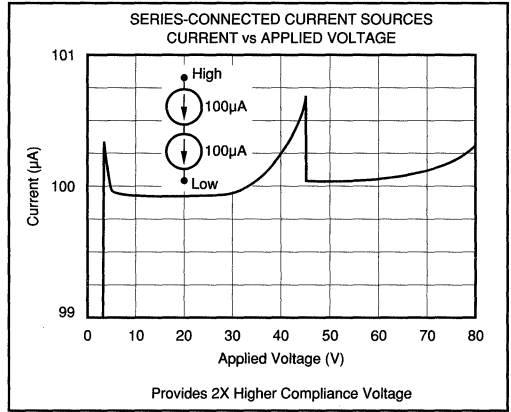


FIGURE 7. 100µA Current Source—80V Compliance.

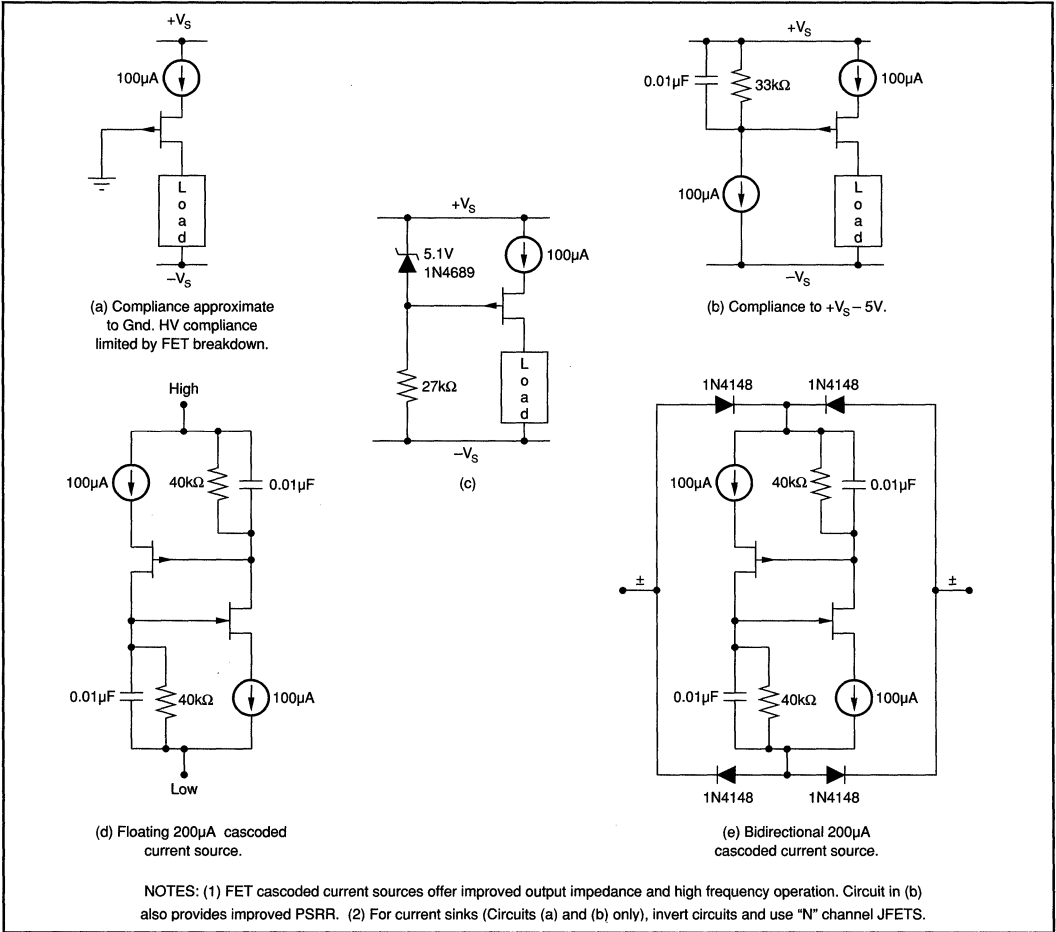


FIGURE 8. FET Cascode Circuits.

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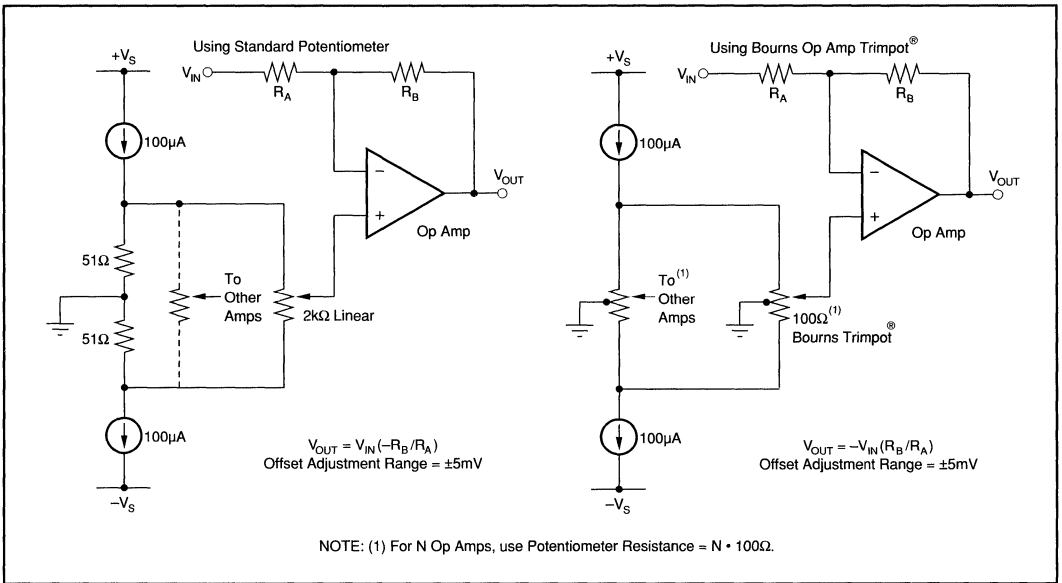
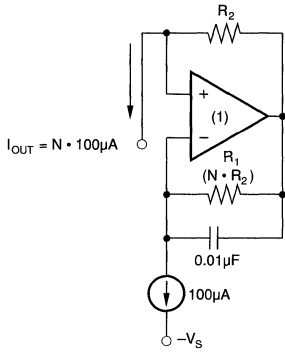


FIGURE 9. Op Amp Offset Adjustment Circuits.

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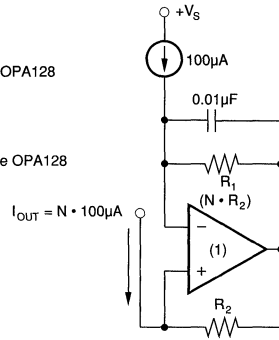
(a)

NOTE: (1) Burr Brown® OPA602 or OPA128

EXAMPLES

R ₁	R ₂	I _{OUT}
100Ω	10MΩ	1nA
10kΩ	1MΩ	1µA
10kΩ	1kΩ	1mA

→ Use OPA128



(b)

FEATURES:

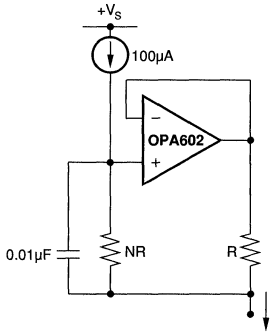
- (1) Zero volts shunt compliance.
- (2) Adjustable only to values above reference value.

NOTE:

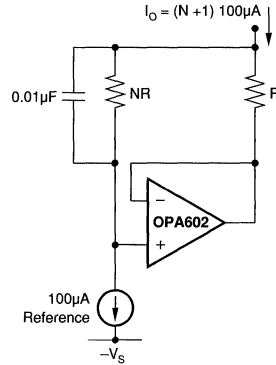
Current source/sink swing to the "Load Return" rail is limited only by the op amp's input common mode range and output swing capability. Voltage drop across "R" can be tailored for any amplifier to allow swing to zero volts from rail.

EXAMPLES

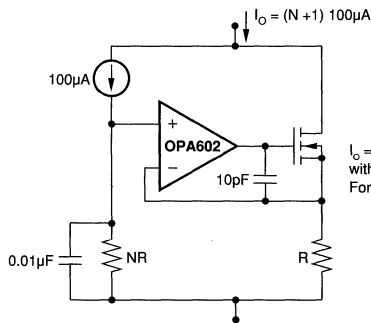
R	NR	I _{OUT}
1kΩ	4kΩ	500µA
1kΩ	9kΩ	1mA
100kΩ	9.9kΩ	10mA



(c)



(d)



(e)

I_O = 100µA (N + 1). Compliance ≈ 3.5V with 0.1V across R. Max I_O limited by FET. For I_O = 1A, R = 0.1Ω, NR = 1kΩ.

FIGURE 10. Adjustable Current Sources.

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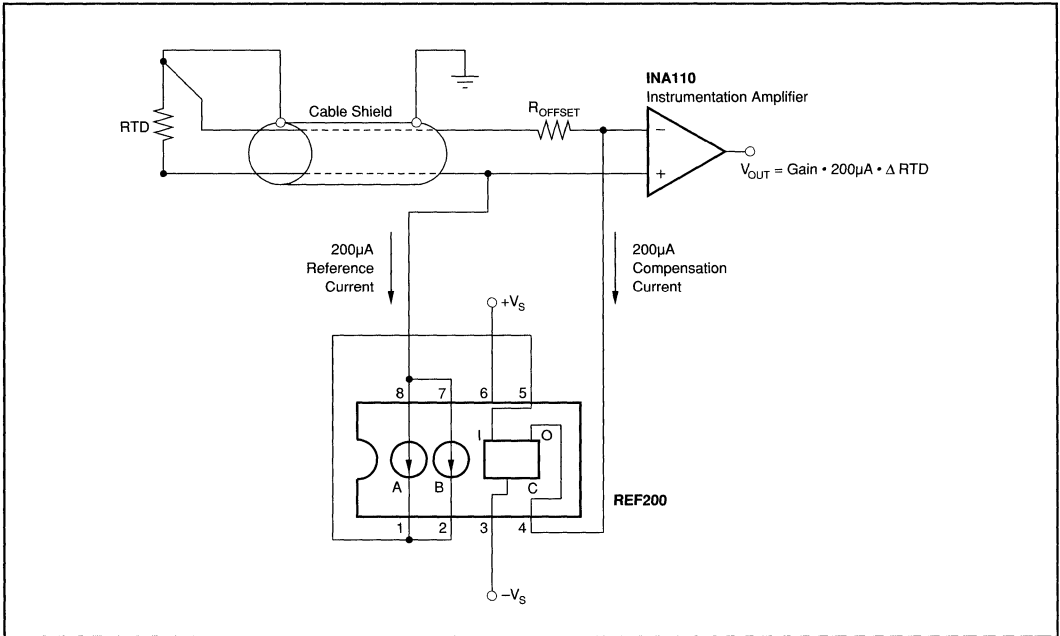


FIGURE 11. RTD Excitation With Three Wire Lead Resistance Compensation.

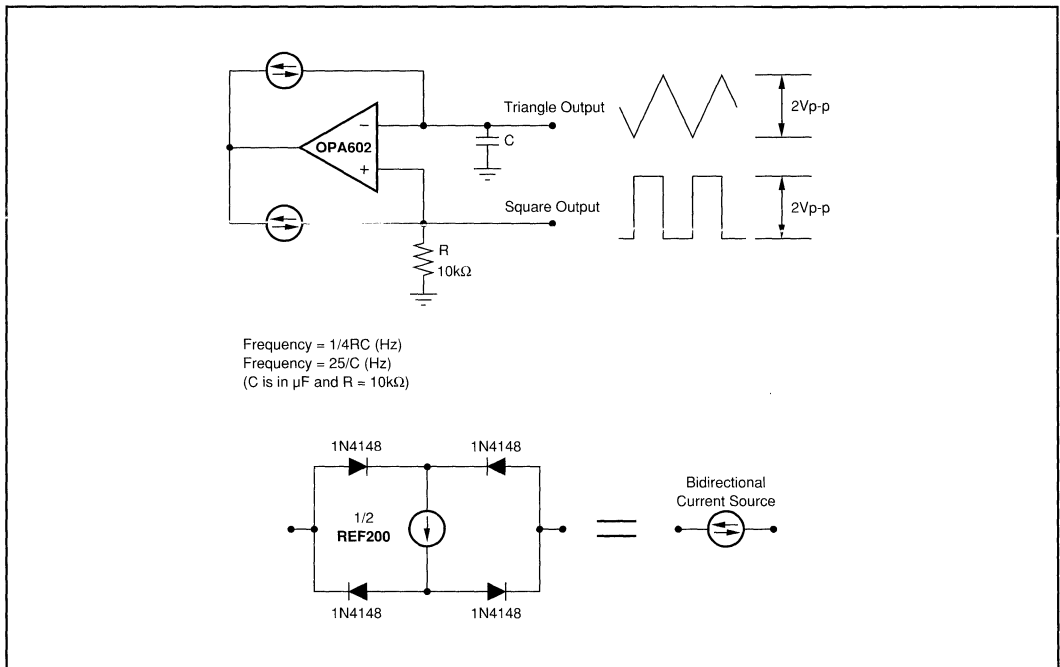


FIGURE 12. Precision Triangle Waveform Generator.

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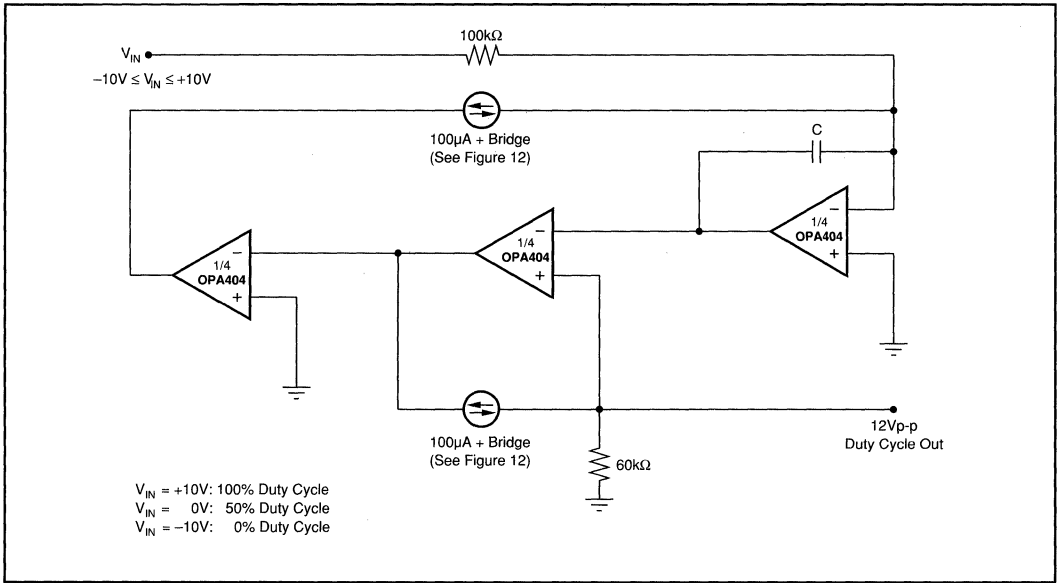


FIGURE 13. Precision Duty-Cycle Modulator.

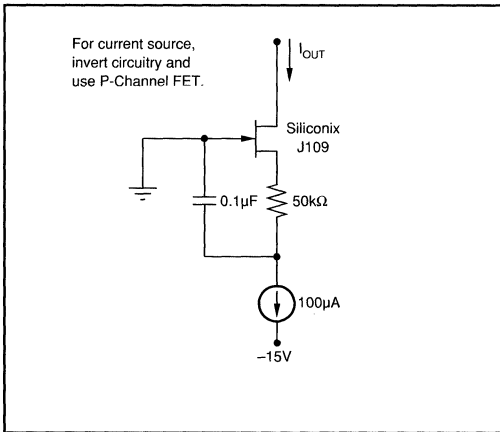


FIGURE 14. Low Noise Current Sink.

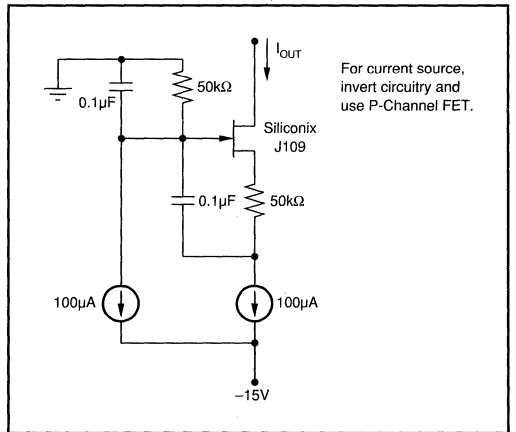


FIGURE 15. Low Noise Current Sink with Compliance Below Ground.

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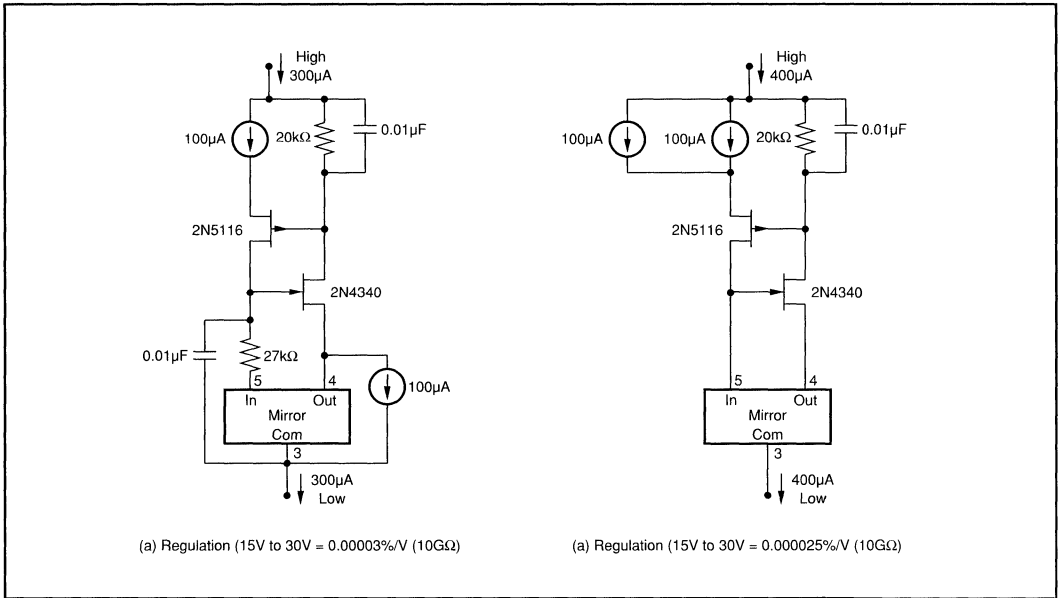


FIGURE 16. Floating 300µA and 400µA Cascoded Current Sources.

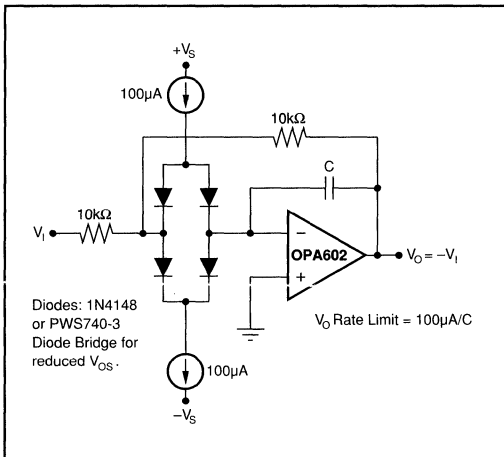


FIGURE 17. Rate Limiter.

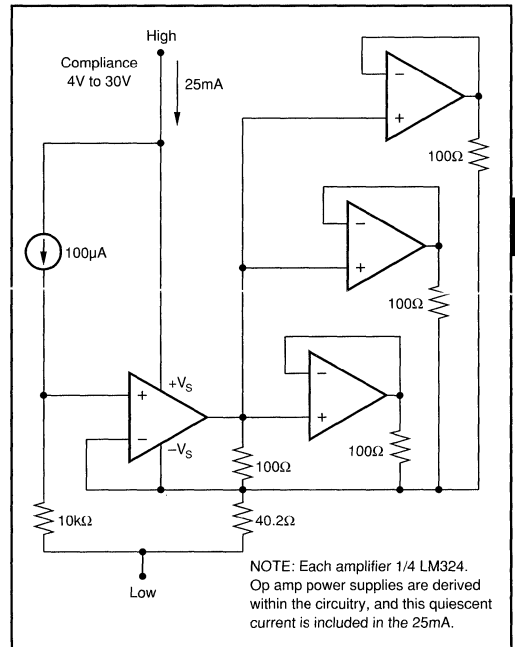


FIGURE 18. 25mA Floating Current Source.

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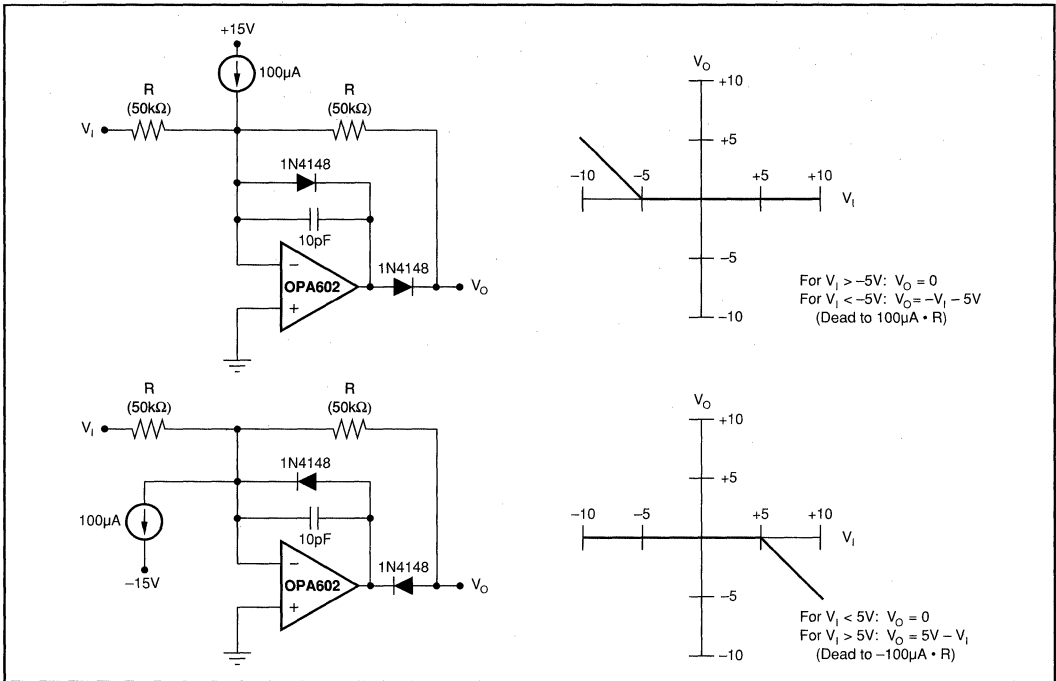


FIGURE 19. Dead-Band Circuit.

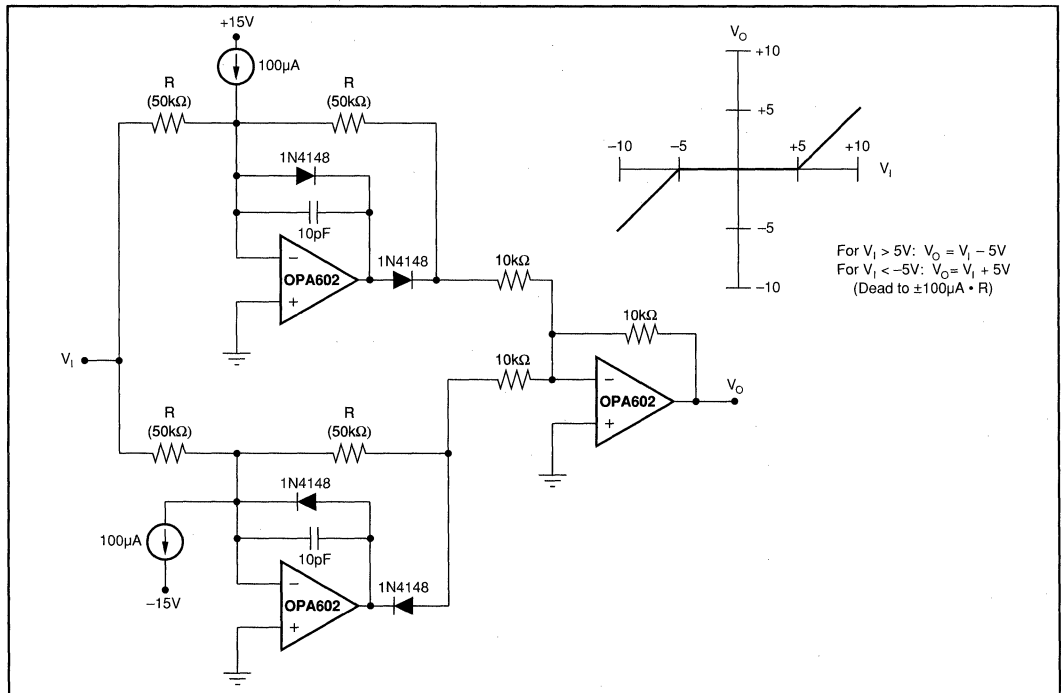


FIGURE 20. Double Dead-Band Circuit.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

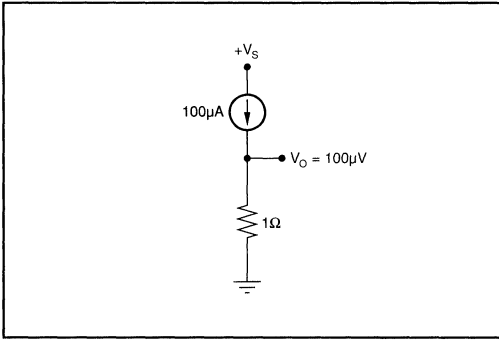


FIGURE 21. Low-Voltage Reference.

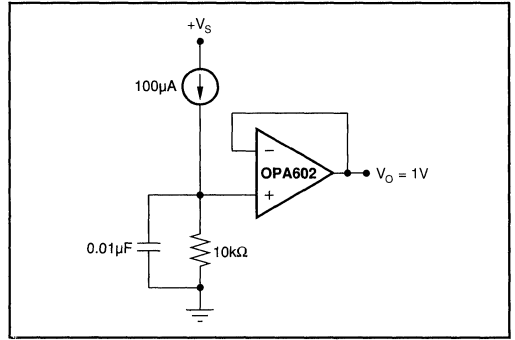


FIGURE 22. Voltage Reference.

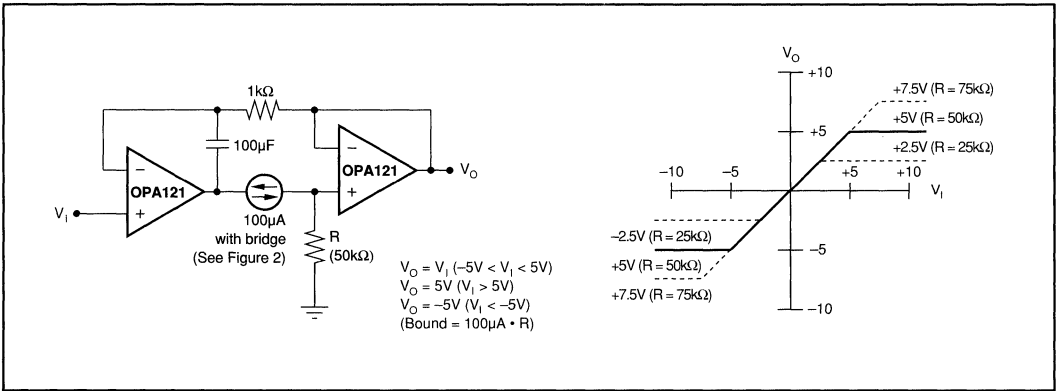


FIGURE 23. Bipolar Limiting Circuit.

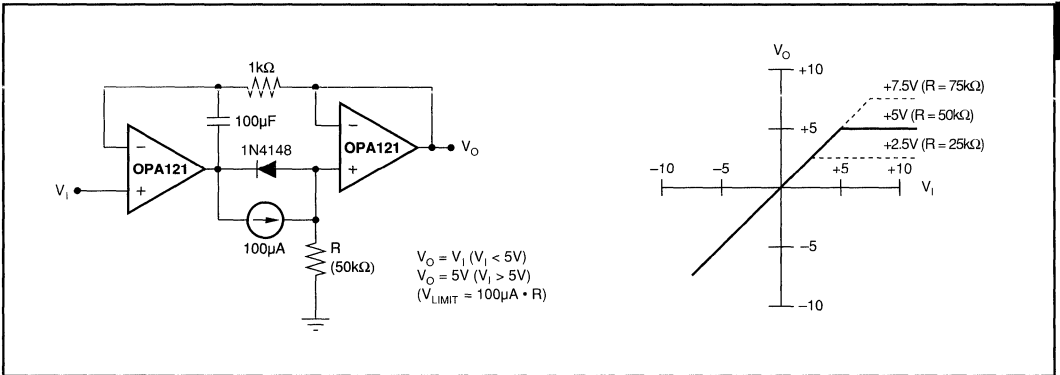


FIGURE 24. Limiting Circuit.

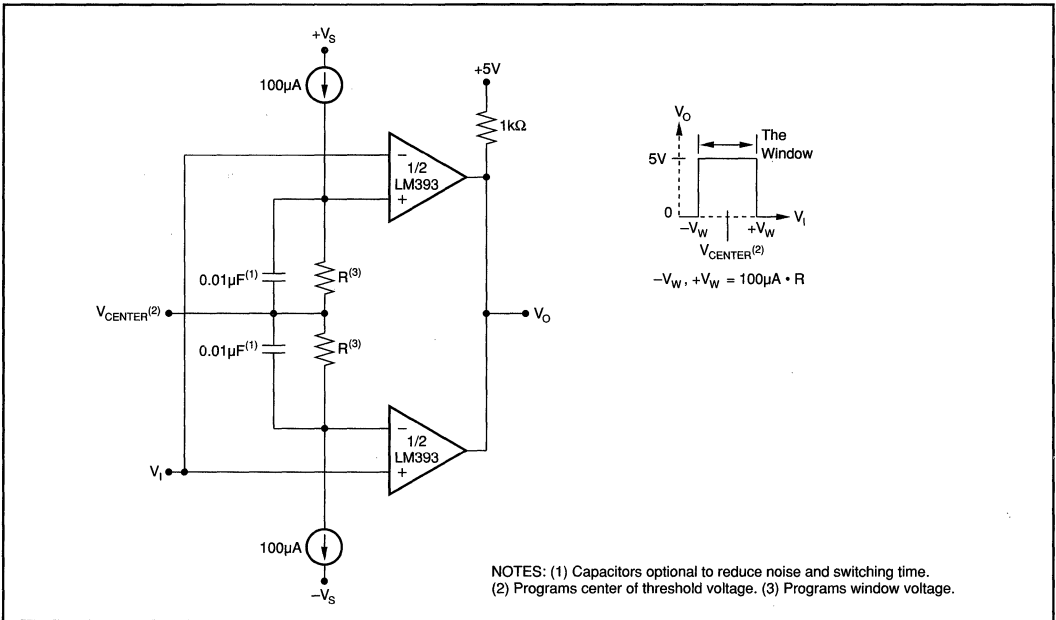


FIGURE 25. Window Comparator.

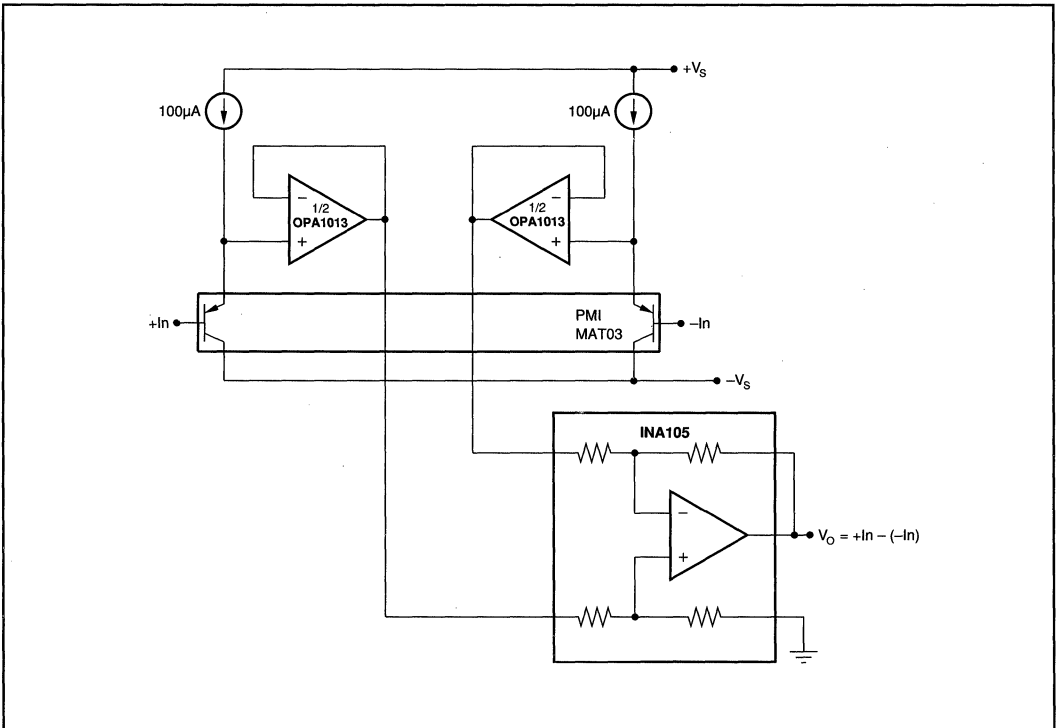
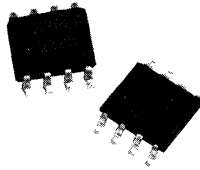


FIGURE 26. Instrumentation Amplifier with Compliance to $-V_S$.

Or, Call Customer Service at 1-800-548-6132 (USA Only)



REF1004



1.2V and 2.5V Micropower VOLTAGE REFERENCE

FEATURES

- INITIAL ACCURACY:
REF1004-1.2 $\pm 4\text{mV}$
REF1004-2.5 $\pm 20\text{mV}$
- MINIMUM OPERATING CURRENT:
REF1004-1.2 $10\mu\text{A}$
REF1004-2.5 $20\mu\text{A}$
- EXCELLENT LONG TERM
TEMPERATURE STABILITY
- VERY LOW DYNAMIC IMPEDANCE
- OPERATES UP TO 20mA
- PACKAGE: 8-Lead SOIC

APPLICATIONS

- BATTERY POWERED TEST EQUIPMENT
- PORTABLE MEDICAL INSTRUMENTATION
- PORTABLE COMMUNICATIONS DEVICES
- A/D AND D/A CONVERTERS
- NOTEBOOK AND PALMTOP COMPUTERS

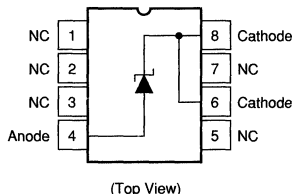
DESCRIPTION

The REF1004-1.2 and REF1004-2.5 are two terminal bandgap reference diodes designed for high accuracy with outstanding temperature characteristics at low operating currents. Prior to the introduction of the REF1004 Micropower Voltage References, accuracy and stability specifications could only be attained by expensive screening of standard devices. The REF1004 is a cost effective solution when reference voltage accuracy, low power, and long term temperature stability are required.

REF1004 is a drop-in replacement for the LT1004 as well as an upgraded replacement of the LM185/385 series references. The REF1004C is characterized for operation from 0°C to 70°C and the REF1004I is characterized for operation from -40°C to $+85^{\circ}\text{C}$.

The REF1004 is offered in an 8-lead Plastic SOIC package and shipped in anti-static rails or tape and reel.

Typical Operating Circuit



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132



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SPECIFICATIONS

ELECTRICAL

$T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	REF1004-1.2			REF1004-2.5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE VOLTAGE REF1004C ⁽¹⁾ REF1004I ⁽²⁾	$I_R = 100\mu\text{A}$	1.231 1.229 1.225	1.235 1.235 1.235	1.239 1.239 1.239	2.490 2.487 2.480	2.500 2.500 2.500	2.511 2.511 2.511	V
AVERAGE TEMPERATURE COEFFICIENT	$I_{\text{MIN}} \leq I_R \leq 20\text{mA}$		20			20		ppm/ $^\circ\text{C}$
MINIMUM OPERATION CURRENT ⁽³⁾			8	10		12	20	μA
REVERSE BREAKDOWN VOLTAGE CHANGE WITH CURRENT	$I_{\text{MIN}} \leq I_R \leq 1\text{mA}$ $1\text{mA} \leq I_R \leq 20\text{mA}$			1 1.5 ⁽³⁾ 10 20 ⁽³⁾			1 1.5 ⁽³⁾ 10 20 ⁽³⁾	mV
REVERSE DYNAMIC IMPEDANCE ⁽³⁾	$I_R = 100\mu\text{A}$		0.2	0.6		0.2	0.6	Ω
WIDE BAND NOISE (RMS) 10Hz $\leq I_R \leq 10\text{kHz}$	$I_R = 100\mu\text{A}$		60			120		μV
LONG TERM STABILITY $T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$	$I_R = 100\mu\text{A}$		20			20		ppm/KHr

NOTES: (1) This specification applies over the full operating temperature range of $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. (2) This specification applies over the full operating temperature range of $40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$. (3) Denotes the specifications which apply over the full operating temperature range.

ORDERING INFORMATION

MODEL	T_A	V_Z	PACKAGE
REF1004C-1.2	0°C to $+70^\circ\text{C}$	1.2V	8-Lead SOIC
REF1004C-2.5	0°C to $+70^\circ\text{C}$	2.5V	8-Lead SOIC
REF1004I-1.2	-40°C to $+85^\circ\text{C}$	1.2V	8-Lead SOIC
REF1004I-2.5	-40°C to $+85^\circ\text{C}$	2.5V	8-Lead SOIC

NOTE: Available in Tape and Reel, Add -TR to Model Number.

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	10mA
Operating Temperature Range	
REF1004C	0°C to $+70^\circ\text{C}$
REF1004I	-40°C to $+85^\circ\text{C}$
Storage Temperature	
REF1004C	-65°C to $+150^\circ\text{C}$
REF1004I	-65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$

ORDERING INFORMATION

MODEL	PART MARKING
REF1004C-1.2	BBREF0412
REF1004C-2.5	BBREF0425
REF1004I-1.2	BBREF0412
REF1004I-2.5	BBREF0425

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REF1004C-1.2	8-Pin SOIC	182
REF1004C-2.5	8-Pin SOIC	182
REF1004I-1.2	8-Pin SOIC	182
REF1004I-2.5	8-Pin SOIC	182

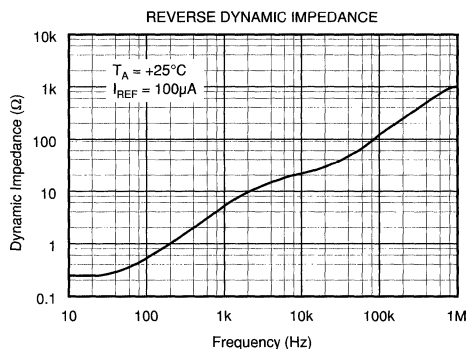
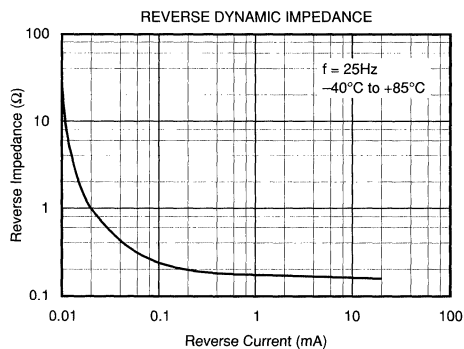
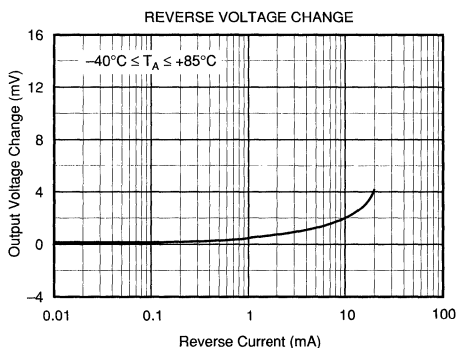
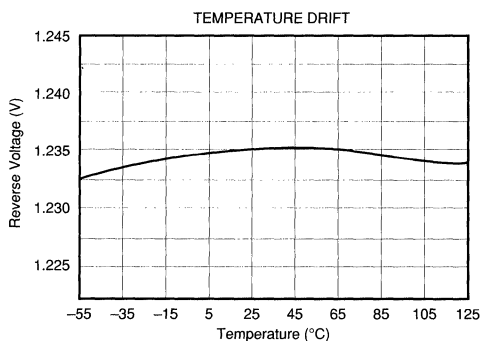
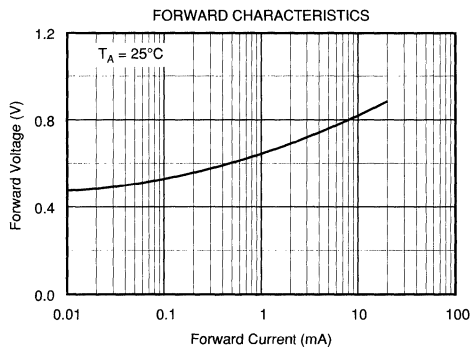
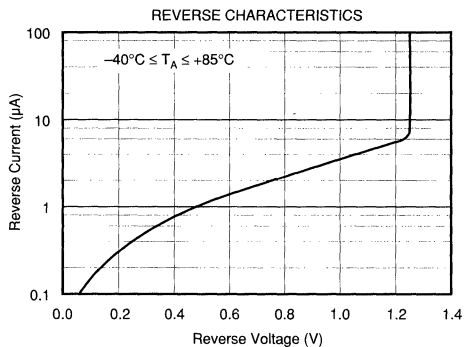
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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TYPICAL PERFORMANCE CURVES 1.2V

$T_A = +25^\circ\text{C}$ unless otherwise noted.



REF1004

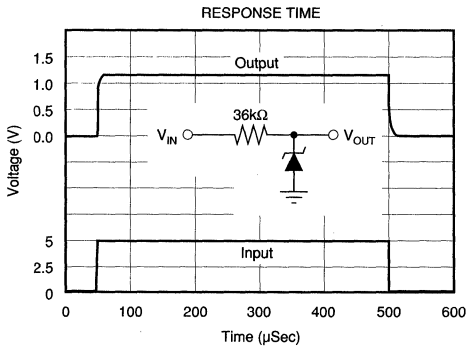
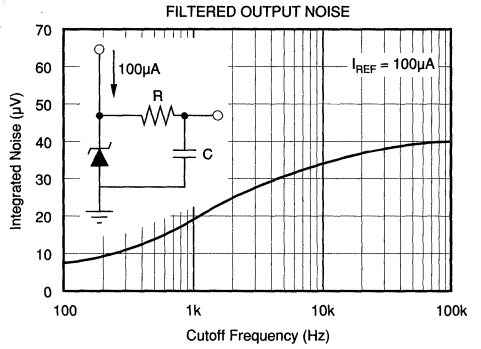
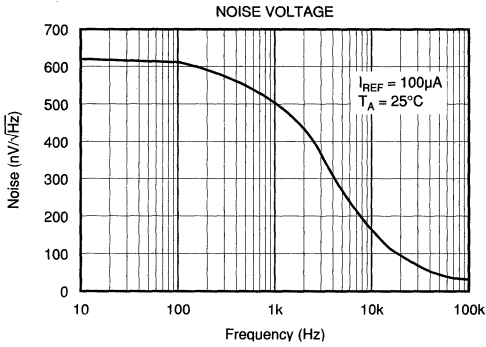
8

REFERENCES AND REGULATORS

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TYPICAL PERFORMANCE CURVES 1.2V (CONT)

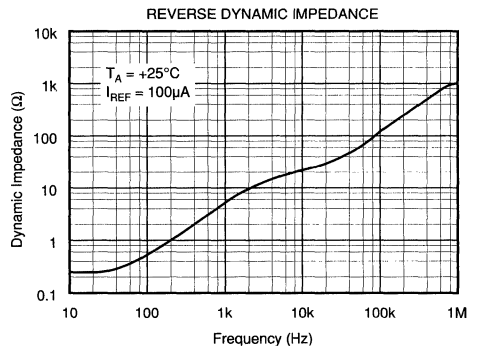
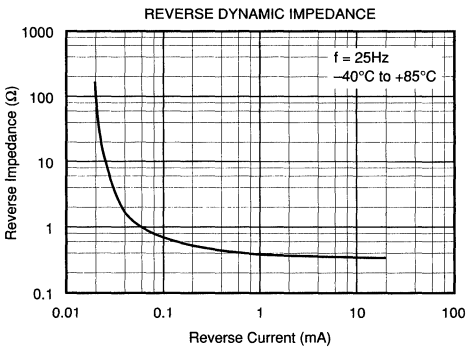
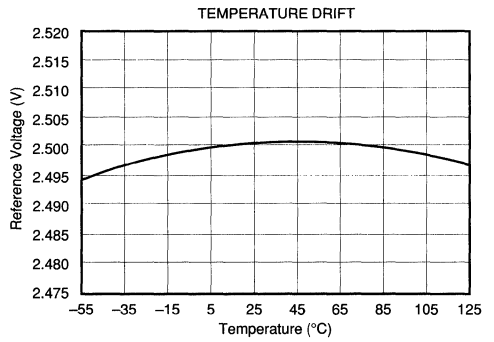
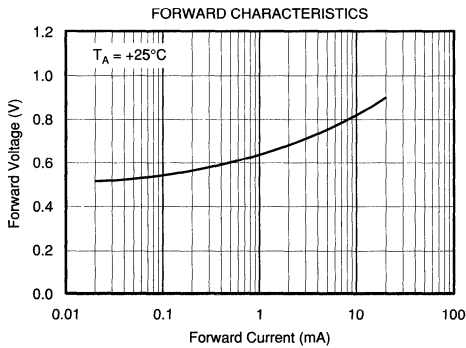
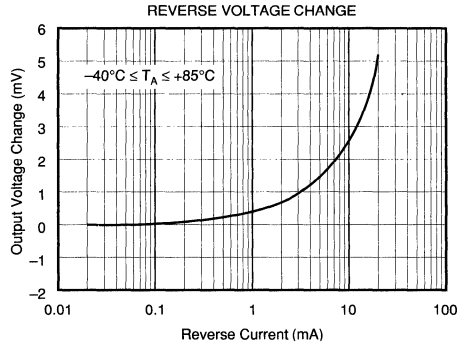
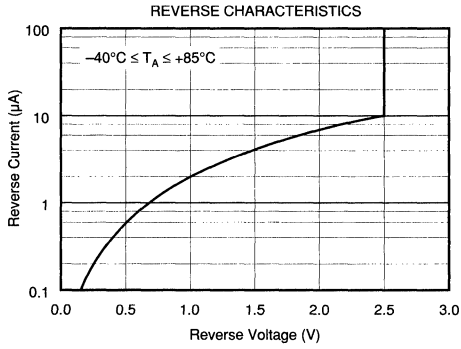
$T_A = +25^\circ\text{C}$ unless otherwise noted.



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TYPICAL PERFORMANCE CURVES 2.5V

$T_A = +25^\circ\text{C}$ unless otherwise noted.



REF1004

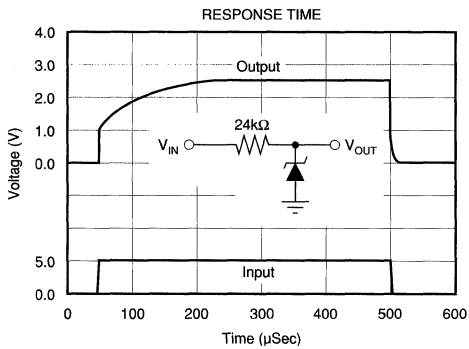
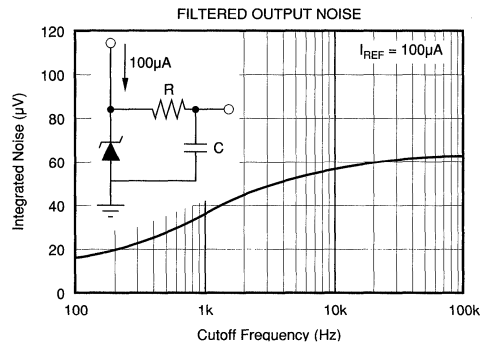
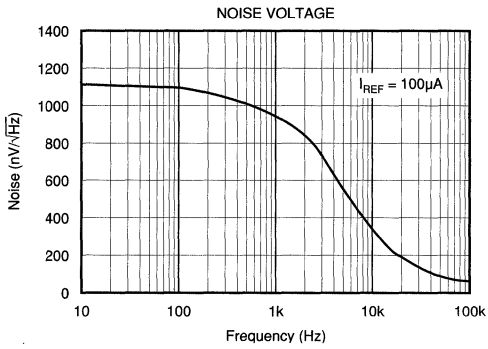
REFERENCES AND REGULATORS



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TYPICAL PERFORMANCE CURVES 2.5V (CONT)

$T_A = +25^\circ\text{C}$ unless otherwise noted.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

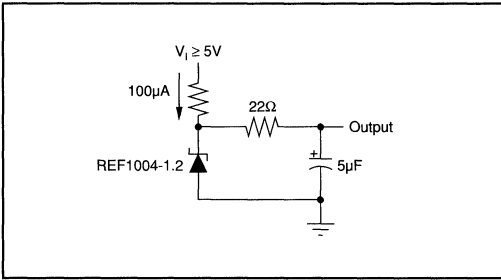


FIGURE 1. Low-Noise Reference.

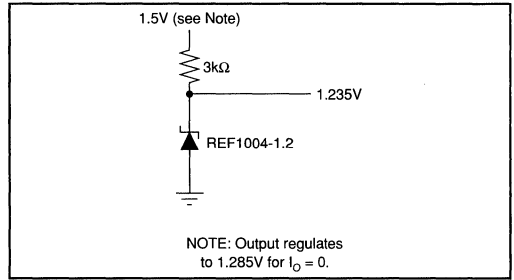


FIGURE 3. 1.2V Reference from 1.5V Battery.

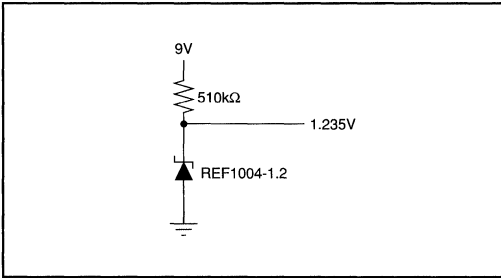


FIGURE 2. Micropower Reference from 9V Battery.

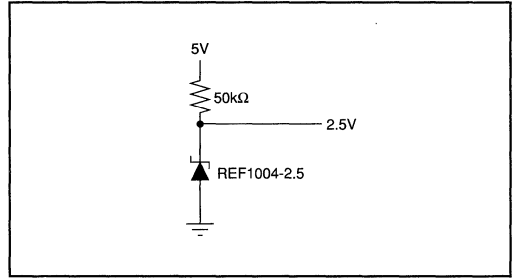


FIGURE 4. 2.5V Reference.

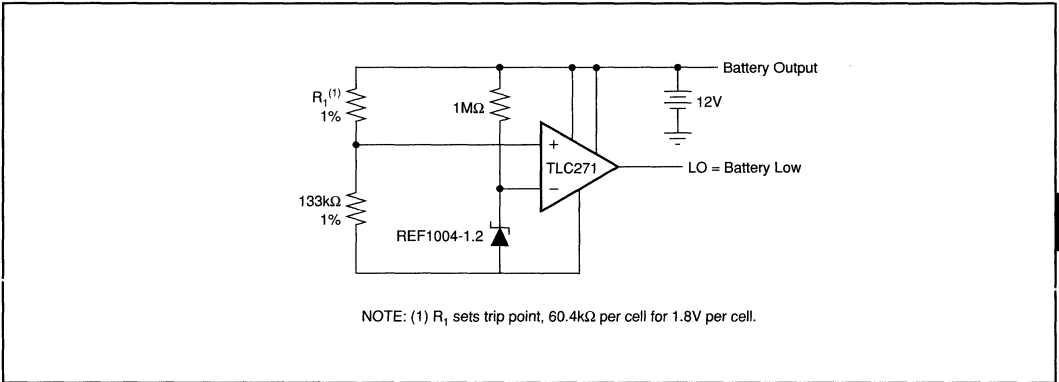


FIGURE 5. Lead-Acid Low-Battery-Voltage Detector.

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REG1117

800mA Low Dropout Positive Regulator 2.85V, 3V, 3.3V, 5V, and Adjustable

FEATURES

- 2.85V, 3V, 3.3V, 5V, and ADJUSTABLE VERSIONS
- 2.85V MODEL FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT: 800mA max
- OUTPUT TOLERANCE: $\pm 1\%$ max
- TOTAL OUTPUT VARIATION: $\pm 2\%$
- 1.2V max DROPOUT VOLTAGE AT $I_o = 800\text{mA}$
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 SURFACE MOUNT PACKAGE

DESCRIPTION

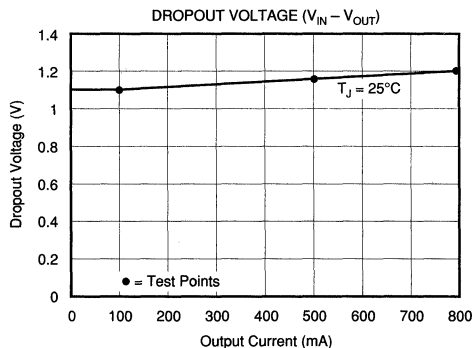
The REG1117 is a family of three-terminal voltage regulators capable of up to 800mA output. Fixed output models include 2.85V, 3V, 3.3V and 5V versions. Output voltage of the adjustable version is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input-output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

REG1117 is packaged in an SOT-223 surface-mount package, suitable for reflow soldering techniques.

APPLICATIONS

- SCSI-2 ACTIVE TERMINATION
- HAND-HELD DATA COLLECTION DEVICES
- HIGH EFFICIENCY LINEAR REGULATORS
- 5V LINEAR REGULATORS
- BATTERY POWERED INSTRUMENTATION
- BATTERY MANAGEMENT CIRCUITS FOR NOTEBOOK AND PALMTOP PCs



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SPECIFICATIONS

$T_j = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
REG1117-2.85	Note 1	$I_o = 10\text{mA}, V_{IN} = 4.85\text{V}$ $I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.05 \text{ to } 10\text{V}$	2.82 2.79	2.85 2.85	2.88 2.91	V V
REG1117-3	Note 1	$I_o = 10\text{mA}, V_{IN} = 5\text{V}$ $I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.5 \text{ to } 10\text{V}$	2.97 2.94	3.00 3.00	3.03 3.06	V V
REG1117-3.3	Note 1	$I_o = 10\text{mA}, V_{IN} = 5.3\text{V}$ $I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.8 \text{ to } 10\text{V}$	3.27 3.24	3.30 3.30	3.33 3.36	V V
REG1117-5	Note 1	$I_o = 10\text{mA}, V_{IN} = 7\text{V}$ $I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 6.5 \text{ to } 10\text{V}$	4.95 4.90	5.00 5.00	5.05 5.10	V V
REFERENCE VOLTAGE						
REG1117 (Adjustable)	Note 1	$I_o = 10\text{mA}, V_{IN} = 3.25\text{V}$ $I_o = 10 \text{ to } 800\text{mA}, V_{IN} - V_o = 1.4 \text{ to } 10\text{V}$	1.238 1.225	1.250 1.250	1.262 1.280	V V
LINE REGULATION						
REG1117-2.85	Note 1	$I_o = 0, V_{IN} = 4.25 \text{ to } 10\text{V}$		1	7	mV
REG1117-3	Note 1	$I_o = 0, V_{IN} = 4.5 \text{ to } 10\text{V}$		2	7	mV
REG1117-3.3	Note 1	$I_o = 0, V_{IN} = 4.8 \text{ to } 10\text{V}$		2	7	mV
REG1117-5	Note 1	$I_o = 0, V_{IN} = 6.5 \text{ to } 15\text{V}$		3	10	mV
REG1117 (Adjustable)	Note 1	$I_o = 10\text{mA}, V_{IN} - V_o = 1.5 \text{ to } 13.75\text{V}$		0.1	0.4	%
LOAD REGULATION						
REG1117-2.85	Note 1	$I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.25\text{V}$		2	10	mV
REG1117-3	Note 1	$I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.5\text{V}$		2	12	mV
REG1117-3.3	Note 1	$I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 4.8\text{V}$		3	12	mV
REG1117-5	Note 1	$I_o = 0 \text{ to } 800\text{mA}, V_{IN} = 6.5\text{V}$		3	15	mV
REG1117 ⁽³⁾ (Adjustable)	Note 1	$I_o = 10 \text{ to } 800\text{mA}, V_{IN} - V_o = 3\text{V}$		0.1	0.4	%
DROPOUT VOLTAGE⁽³⁾						
All Models	Note 1	$I_o = 100\text{mA}$		1.00	1.10	V
	Note 1	$I_o = 500\text{mA}$		1.05	1.15	V
	Note 1	$I_o = 800\text{mA}$		1.10	1.20	V
CURRENT LIMIT						
All Models		$V_{IN} - V_o = 5\text{V}$	800	950	1200	mA
MINIMUM LOAD CURRENT						
REG1117 (Adjustable)	Note 1	$V_{IN} - V_o = 13.75\text{V}$		1.7	5	mA
QUIESCENT CURRENT						
Fixed-Voltage Models	Note 1	$V_{IN} - V_o = 5\text{V}$		4	10	mA
REG1117 Adjust Pin Current ⁽²⁾ vs Load Current	Note 1	$I_o = 10\text{mA} \text{ to } 800\text{mA}, V_{IN} - V_o = 1.4 \text{ to } 10\text{V}$		50 0.5	120 5	μA μA
THERMAL REGULATION⁽⁴⁾						
All Models		30ms Pulse		0.01	0.1	%/W
RIPPLE REJECTION						
All Models		$f = 120\text{Hz}, V_{IN} - V_{OUT} = 3\text{V} + 1V_{PP}$ Ripple		62		dB
TEMPERATURE DRIFT						
Fixed-Voltage Models		$T_j = 0^\circ\text{C} \text{ to } +125^\circ\text{C}$		0.5		%
REG1117 (Adjustable)		$T_j = 0^\circ\text{C} \text{ to } +125^\circ\text{C}$		2		%
LONG-TERM STABILITY						
All Models		$T_A = +125^\circ\text{C}, 1000\text{Hr}$		0.3		%
OUTPUT NOISE						
RMS noise All Models		$f = 10\text{Hz} \text{ to } 10\text{kHz}$		0.003		%
THERMAL RESISTANCE						
θ_{JC} All Models		(Junction-to-Case at Tab)		15		$^\circ\text{C}/\text{W}$

NOTES: (1) Specification applies over the full operating Junction temperature range, 0°C to 125°C . (2) REG1117 adjustable version requires a minimum load current for $\pm 2\%$ load regulation. (3) Dropout voltage is the Input voltage minus output voltage that produces a 1% decrease in output voltage. (4) Percentage change in unloaded output voltage before vs after a 30ms power pulse of $I_o = 800\text{mA}, V_{IN} - V_o = 1.4\text{V}$.

REG1117

8

REFERENCES AND REGULATORS

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ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally Limited
Input Voltage	15V
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	-40°C to +150°C
Lead Temperature (soldering, 10s) ⁽¹⁾	+300°C

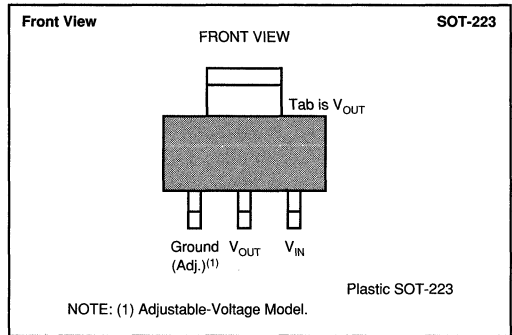
NOTE: (1) See "Soldering Methods."

ORDERING INFORMATION

MODEL ⁽¹⁾	PART MARKING	PACKAGE
REG1117-2.85	BB11172	Plastic SOT-223
REG1117-3	BB11173	Plastic SOT-223
REG1117-3.3	BB11174	Plastic SOT-223
REG1117-5	BB11175	Plastic SOT-223
REG1117	BB1117	Plastic SOT-223

NOTE: (1) Available in Tape and Reel, add -TR to Model Number.

CONNECTION DIAGRAM

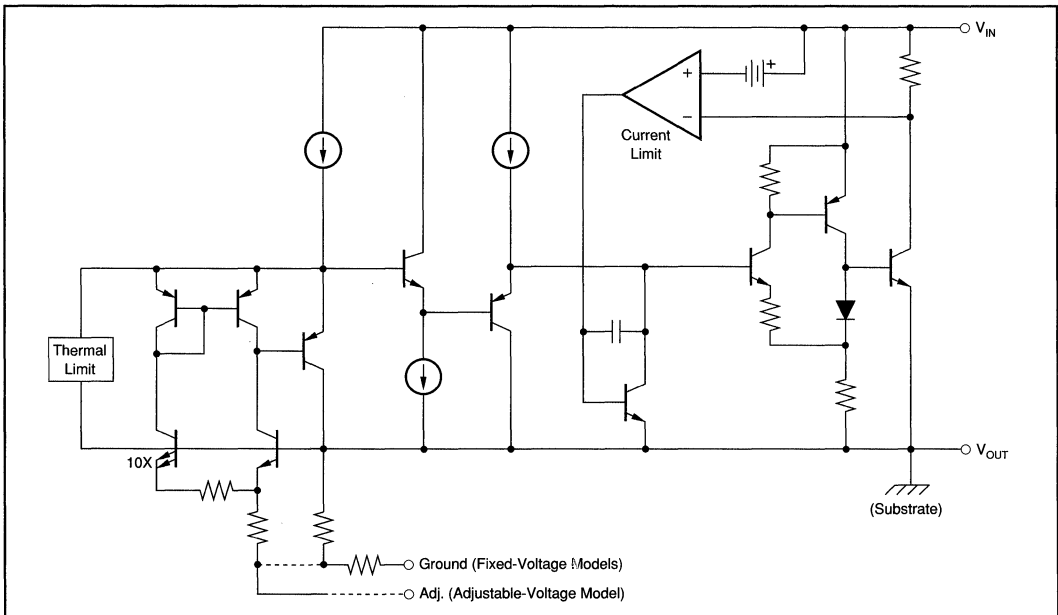


PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REG1117-2.85	Plastic SOT-223	311
REG1117-3	Plastic SOT-223	311
REG1117-3.3	Plastic SOT-223	311
REG1117-5	Plastic SOT-223	311
REG1117	Plastic SOT-223	311

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

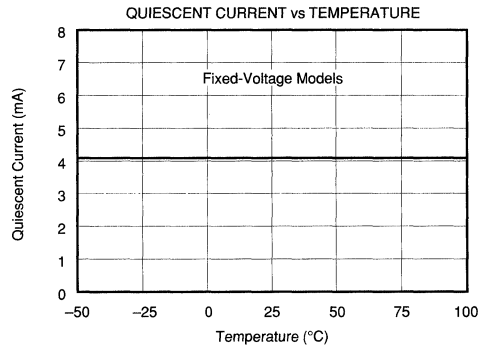
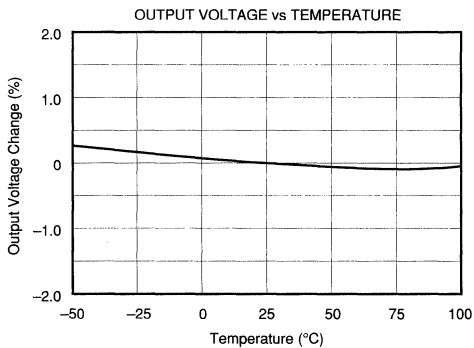
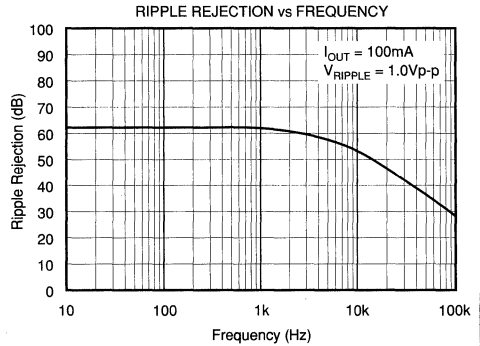
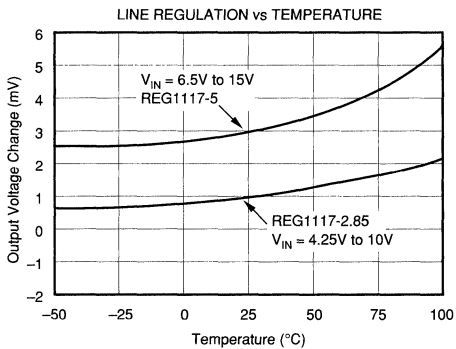
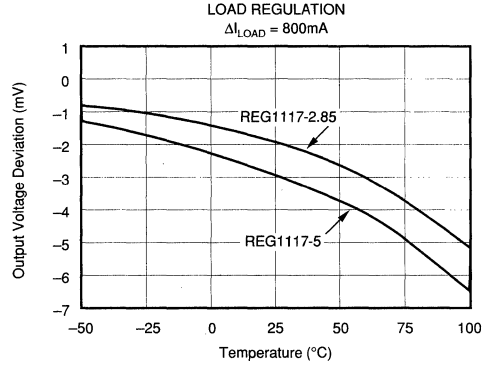
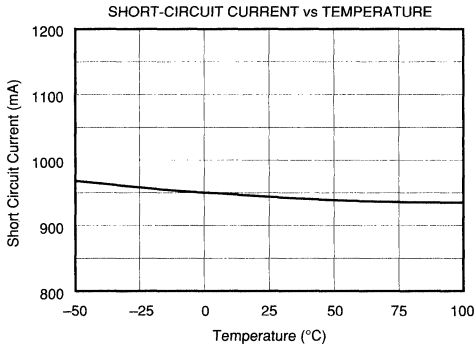
SIMPLIFIED SCHEMATIC



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TYPICAL PERFORMANCE CURVE

$T_j = +25^\circ\text{C}$, unless otherwise specified.



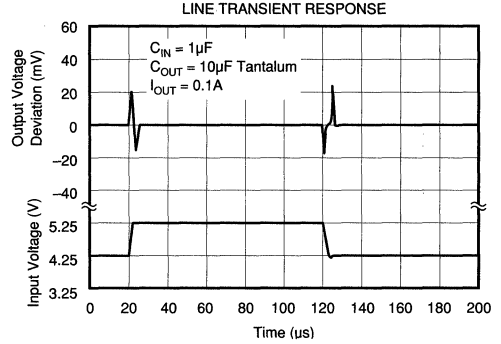
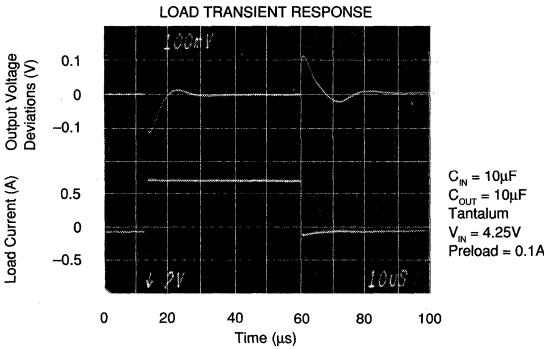
REG1117



REFERENCES AND REGULATORS

TYPICAL PERFORMANCE CURVE (CONT)

$T_J = +25^\circ\text{C}$, unless otherwise specified.



APPLICATIONS INFORMATION

Figure 1 shows the basic hookup diagram for fixed-voltage models. All models require an output capacitor for proper operation and to improve high frequency load regulation. A $10\mu\text{F}$ tantalum capacitor is recommended. Aluminum electrolytic types of $50\mu\text{F}$ or greater can also be used. A high quality capacitor should be used to assure that the ESR (effective series resistance) is less than 0.5Ω .

Figure 2 shows a the hookup diagram for the adjustable voltage model. Resistor values are shown for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2. For best load regulation, connect R_1 close to the output pin and R_2 close to the ground side of the load as shown.

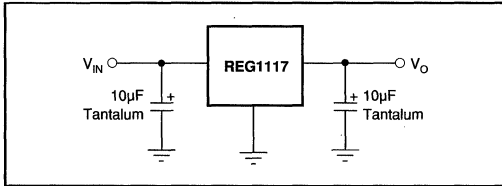


FIGURE 1. Fixed-Voltage Model—Basic Connections.

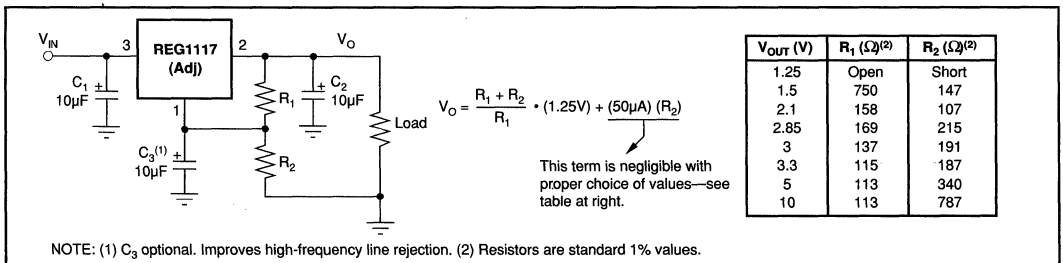


FIGURE 2. Adjustable-Voltage Model—Basic Connections.

THERMAL CONSIDERATIONS

The REG1117 has current limit and thermal shutdown circuits that protect it from overload. The thermal shutdown activates at approximately $T_J = 165^\circ\text{C}$. For continuous operation, however, the junction temperature should not be allowed to exceed 125°C . Any tendency to activate the thermal shutdown in normal use is an indication of an inadequate heat sink or excessive power dissipation. The power dissipation is equal to:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT}$$

The junction temperature can be calculated by:

$$T_J = T_A + P_D (\theta_{JA})$$

where T_A is the ambient temperature, and

θ_{JA} is the junction-to-ambient thermal resistance

The REG1117 derives heat sinking from conduction through its copper leads, especially the large mounting tab. These must be soldered to a circuit board with a substantial amount of copper remaining (see Figure 3). Circuit board traces connecting to the tab and the leads should be made as large as practical. Other nearby circuit traces, including those on the back side of the circuit board, help conduct heat away

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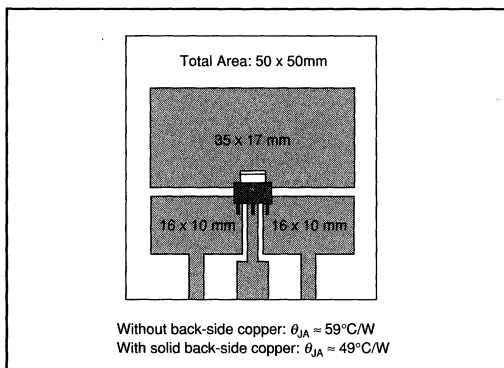


FIGURE 3. Circuit Board Layout Example.

from the device, even though they are not electrically connected. Make all nearby copper traces as wide as possible and leave only narrow gaps between traces.

Table I shows approximate values of θ_{JA} for various circuit board and copper areas. Nearby heat dissipating components, circuit board mounting conditions and ventilation can dramatically affect the actual θ_{JA} .

A simple experiment will determine whether the maximum recommended junction temperature is exceeded in an actual circuit board and mounting configuration: Increase the ambient temperature above that expected in normal operation until the device's thermal shutdown is activated. If this occurs at more than 40°C above the maximum expected ambient temperature, then the T_J will be less than 125°C during normal operation.

SOLDERING METHODS

The REG1117 package is suitable for infrared reflow and vapor-phase reflow soldering techniques. The high rate of temperature change that occurs with wave soldering, or hand soldering can damage the REG1117.

TOTAL PC BOARD AREA	TOPSIDE ⁽¹⁾ COPPER AREA	BACKSIDE COPPER AREA	THERMAL RESISTANCE JUNCTION-TO-AMBIENT
2500mm ²	2500mm ²	2500mm ²	46°C/W
2500mm ²	1250mm ²	2500mm ²	47°C/W
2500mm ²	950mm ²	2500mm ²	49°C/W
2500mm ²	2500mm ²	0	51°C/W
2500mm ²	1800mm ²	0	53°C/W
1600mm ²	600mm ²	1600mm ²	55°C/W
2500mm ²	1250mm ²	0	58°C/W
2500mm ²	915mm ²	0	59°C/W
1600mm ²	600mm ²	0	67°C/W
900mm ²	340mm ²	900mm ²	72°C/W
900mm ²	340mm ²	0	85°C/W

NOTE: (1) Tab is attached to the topside copper.

TABLE I.

INSPEC Abstract Number: B91007604, C91012627
 Kelly, E.G. "Thermal Characteristics of Surface 5WK9Ω Packages." The Proceedings of SMTCON. Surface Mount Technology Conference and Exposition: *Competitive Surface Mount Technology*, April 3-6, 1990, Atlantic City, NJ, USA. Abstract Publisher: IC Manage, 1990, Chicago, IL, USA.

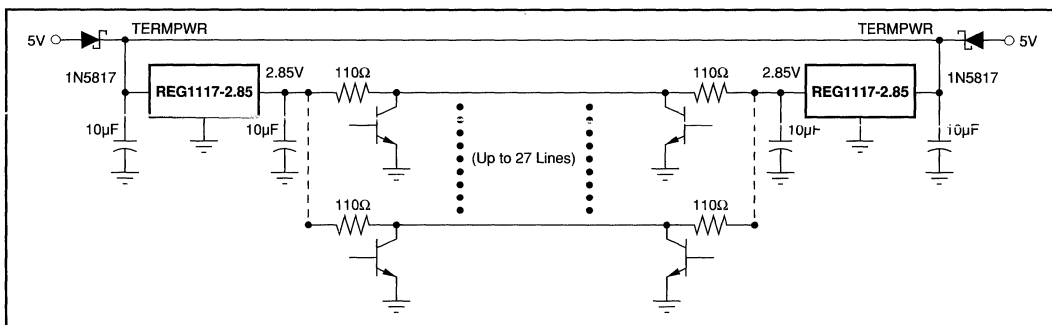


FIGURE 4. SCSI Active Termination Configuration.

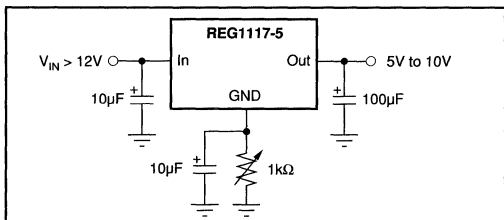


FIGURE 5. Adjusting Output of Fixed Voltage Models.

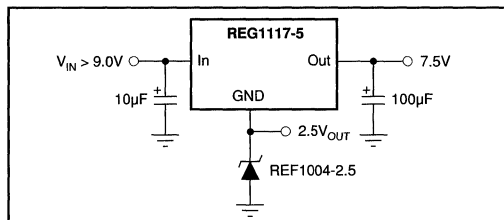


FIGURE 6. Regulator with Reference.

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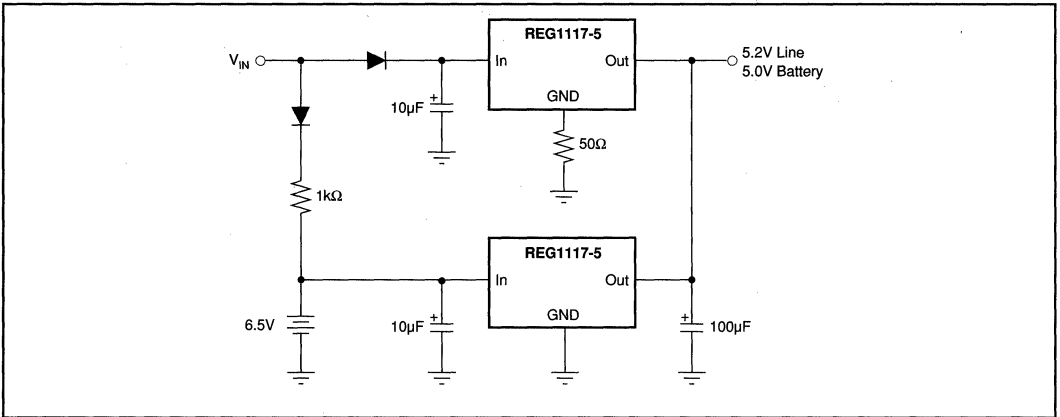


FIGURE 7. Battery Backed Up Regulated Supply.

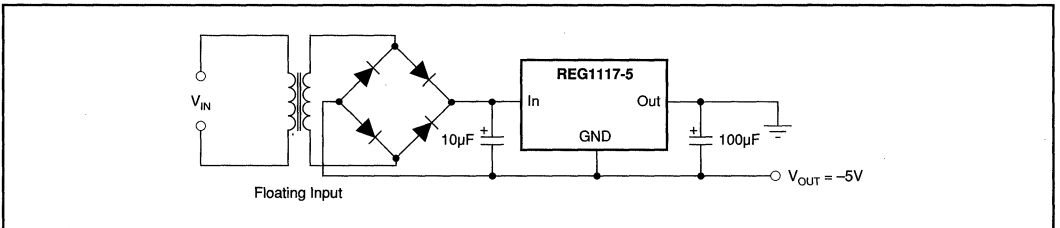
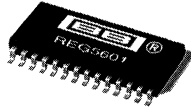


FIGURE 8. Low Dropout Negative Supply.

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REG5601

SCSI 18-LINE ACTIVE TERMINATOR

FEATURES

- FULLY COMPLIANT WITH SCSI-2 SPECIFICATIONS
- ACTIVE 18-LINE TERMINATOR
- INTERNAL 2.9V REGULATOR
- ON-CHIP TERMINATION RESISTORS
- DISCONNECT ALL TERMINATION RESISTORS WITH A SINGLE LOGIC COMMAND
- POWER-DOWN MODE: 150 μ A max
- OUTPUT CAPACITANCE IN DISCONNECT MODE: 10pF typ
- CURRENT LIMIT AND THERMAL SHUT-DOWN PROTECTION
- 28-Lead SOIC PACKAGE
- SECOND SOURCE FOR UC5601DWP

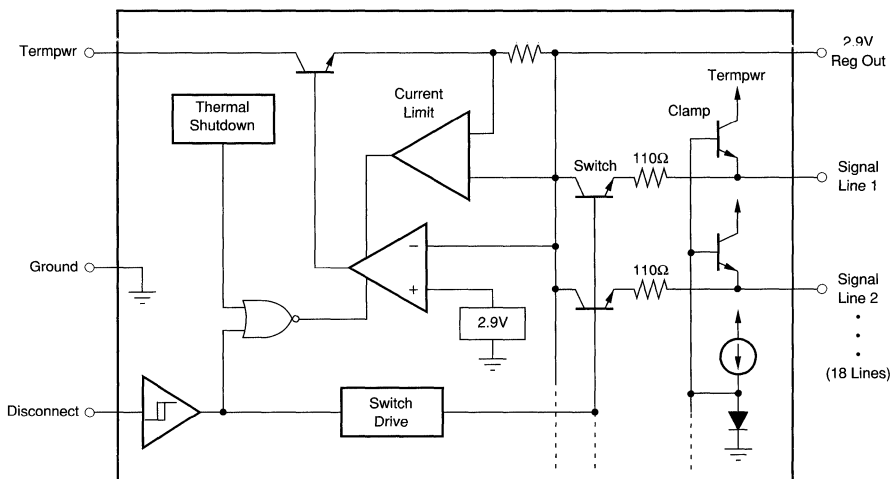
DESCRIPTION

The REG5601 is an 18-line active terminator for SCSI-2 (Small Computer Systems Interface) circuitry. On-chip resistors and 2.9V regulator provide the prescribed 110 Ω termination for low power dissipation and high speed data transmission.

All line connections can be disconnected from the bus with a single logic control line to reduce standby power consumption. Output lines remain high impedance without power applied. Each line is individually clamped at ground to dissipate negative-going glitches.

The 2.9V regulator is current-limited and thermally protected. Regulated output is available for external circuitry.

The REG5601 is packaged in a 28-lead surface-mount package and is specified for operation over the 0 to 70 $^{\circ}$ C temperature range.



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SPECIFICATIONS

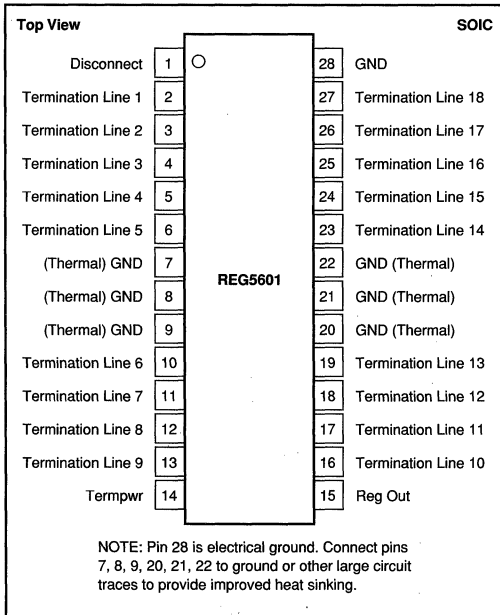
ELECTRICAL

T_A = 0°C to +70°C, Tempwpr = 4.75V, Disconnect = 0V, unless otherwise specified.

PARAMETERS	CONDITIONS	REG5601U			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Tempwpr Supply Voltage	All Termination Lines = Open All V _{TERM} = 0.5V Disconnect = Open (High)	4.0	14	5.25	V
Tempwpr Supply Current			385	430	mA
Power-Down Mode			100	150	μA
TERMINATION LINES					
Termination Impedance	ΔI _{TERM} = 5mA to 15mA	107	110	115	Ω
Output High Voltage	Tempwpr = 4V, Note 1	2.65	2.8		V
Maximum Output Current	V _{TERM} = 0.5V	20.5	21.7	22.4	mA
	V _{TERM} = 0.5V, Tempwpr = 4V, Note 1	19.4	21	22.4	mA
Output Clamp Level	I _{TERM} = -30mA	-0.2	-0.05	0.1	V
Output Leakage	Disconnect = Open (High), Tempwpr = 0V to 5.25V		20	400	nA
Output Capacitance	Disconnect = Open (High)		10		pF
REGULATOR					
Regulator Output Voltage	Tempwpr = 4V to 6V I _{REG} = 0 to 400mA All V _{TERM} = 0.5V, ΔV _{REG} = 100mV	2.8	2.9	3.0	V
Line Regulation			6	20	mV
Load Regulation			20	50	mV
Drop-Out Voltage			1.0	1.2	V
Short-Circuit Current	V _{REG} = 0V	450	1350	1650	mA
Current Sink	V _{REG} = 3.5V	8	11		mA
Thermal Shutdown			170		°C
DISCONNECT LOGIC INPUT					
Disconnect Threshold	Disconnect = 0V	0.8	1.6	2.0	V
Threshold Hysteresis			200		mV
Input Current (Internal Pull-Up)			6	15	μA
TEMPERATURE RANGE					
Operating		0		70	°C
Storage		-40		150	°C
θ _{JL} (junction-to-lead)			18		°C/W
θ _{JM} (junction-to-ambient)			38		°C/W

NOTE: (1) Measurement of each termination line while the other 17 lines are held low (0.5V).

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Tempwpr Voltage	+7V
Signal Line Voltage	0V to +7V
Regulator Output Current	1.65A
Power Dissipation	2.5W
Operating Junction Temperature	-40°C to +150°C
Storage Temperature	-40°C to +150°C

ORDERING INFORMATION

MODEL	PART MARKING	PACKAGE
REG5601U	REG5601U	28-Lead SOIC
REG5601U-TR	REG5601U	28-Lead SOIC on Tape & Reel

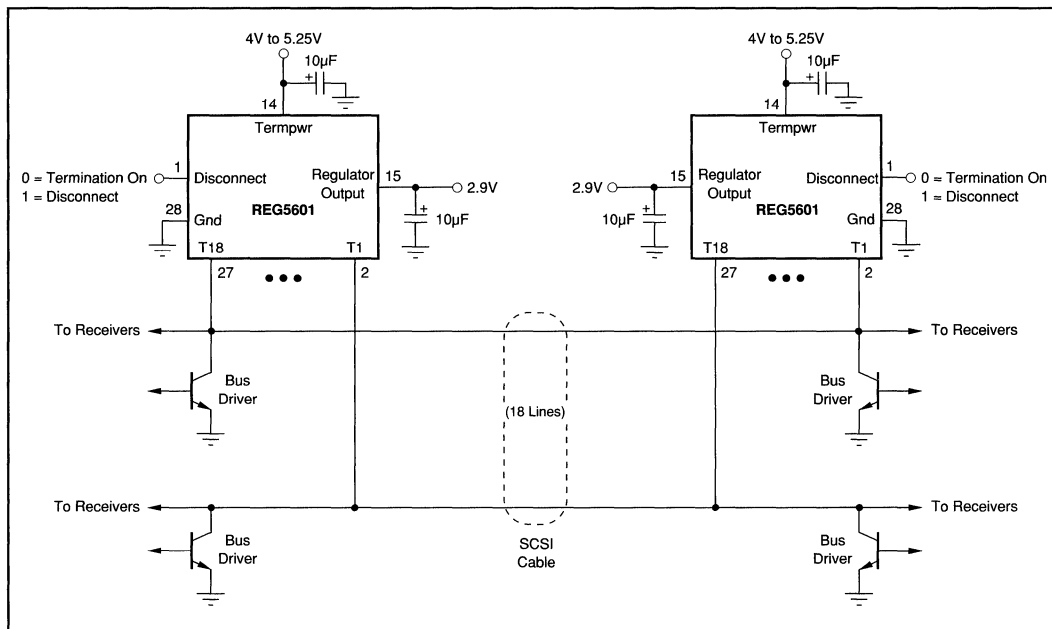
NOTE: Tape and reel conforms to EIA-481 standards. Reel diameter is 360mm, tape width is 24mm, part pitch is 16. Standard quantity is 1000 per reel.

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
REG5601U	Plastic 28-Lead SOIC	217

Or, Call Customer Service at 1-800-548-6132 (USA Only)

PRODUCT APPLICATION FOR STANDARD SCSI CONFIGURATION



REG5601



REFERENCES AND REGULATORS

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Appendix A

Demonstration Boards

Burr-Brown offers a wide variety of demonstration boards for both its Linear and Data Conversion Products. New boards for new products are continually being added to the selection— contact the factory your local salesperson for availability.

NOTE: All evaluation fixtures whose model number ends with a 'C' include the product or products mentioned. All other do not include the product, except where specifically noted.

MODEL	PRODUCT	DESCRIPTION
DEM-ACF2101BP-C	ACF2101BP	Evaluation Fixture with Programmable Timing Generator
DEM-ADC614-E	ADC603/614	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1123)
DEM-ADC701-E	ADC701/SHC702	Evaluation Fixture—Digital/Analog Output (Formerly DEM 1113)
DEM-ADS7804/05C	ADS7804/05	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7806/07C	ADS7806/07	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7808/09C	ADS7808/09	Evaluation Fixture—Analog Input and Digital Output
DEM-ADS7810/19C	ADS7810/19	Evaluation Fixture—Analog Input and Digital Output
DEM-BUF600-1GC	BUF600AP	Evaluation Fixture—900MHz Buffer Amplifier
DEM-BUF601-1GC	BUF601AP	Evaluation Fixture—650MHz Buffer Amplifier
DEM-DAC600-E	DAC600	Evaluation Fixture—SMA Digital Inputs and Analog SMA Output (an external reference can be provided via a BNC input). The fixture provides a socket for the DAC600, which must be ordered separately.
DEM-DAC650J-E	DAC650JL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DAC650K-E	DAC650KL	Evaluation Fixture—Digital Input and Analog Output (all SMA connectors). The part is included and soldered to the board.
DEM-DDC101P-C	DDC101P	Evaluation Fixture, includes the DDC101 board, interface board to connect to parallel PC-port and software. Supports all DDC101 options plus FFT.
DEM-DSP102/202C	DSP102/202	Evaluation Fixture—DSP Interface with Programmable Timing Generator
DEM-ISC300-SC	ISC300	Evaluation Fixture—Universal Precision Isolated Measurement Channel.
DEM-ISO212-8-GC	ISO212	Evaluation Fixture—8 Input Channels, Tri-port isolation
DEM-IXR100-SC	IXR100	Evaluation Fixture—Isolated, self-powered 4-20mA two-wire transmitter

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MODEL	PRODUCT	DESCRIPTION
DEM-MPC100-1GC	MPC100AU	Evaluation Fixture—4 to 1 High Speed Multiplexer and Output Buffer BUF601AU
DEM-MPC102-1GC	MPC102AU	Evaluation Fixture—Dual 2 to 1 High Speed Multiplexer and optional output buffer, BUF601AU
DEM-OPA620G/P-C	OPA620/621	Evaluation Fixture Kit for DIP packages—Generic Op Amp Configurations (Formerly DEM 1135)
DEM-OPA622-1GC	OPA622AP	Evaluation Fixture—For voltage and current feedback configuration
DEM-OPA623-1GC	OPA623AP	Evaluation Fixture—High Speed current feedback Op Amp
DEM-OPA628AP-C	OPA628AP	Evaluation Fixture—User selectable configuration for the DIP package
DEM-OPA628AU-C	OPA628AU	Evaluation Fixture—User selectable configuration for the SOIC package
DEM-OPA64XP-Y	OPA64XP	Evaluation Fixture—Three boards are offered for the DIP package of the OPA64X series of operational amplifiers. DEM-OPA64XP-F: follower configuration; DEM-OPA64XP-N: noninverting configuration; DEM-OPA64XP-I: inverting configuration. (Note: each board will operate with any OPA64XP series op-amp. No component is included—it must be ordered separately.)
DEM-OPA64XU-Y	OPA64XU	Evaluation Fixture—Three boards are offered for the SOIC package of the OPA64X series of operational amplifiers. DEM-OPA64XU-F: follower configuration; DEM-OPA64XU-N: noninverting configuration; DEM-OPA64XU-I: inverting configuration. (Note: each board will operate with any OPA64XU series op-amp. No component is included—it must be ordered separately.)
DEM-OPA660-XXX	OPA660	Evaluation Fixture—Five boards are offered for five different configurations. DEM-OPA660-1GC: Diamond transistor and buffer; DEM-OPA660-2GC: Current-feedback operational amplifier; DEM-OPA660-3GC: Direct-feedback amplifier; DEM-OPA660-4G: Layouts for all applications using SOIC (unassembled); DEM-OPA660-5G: Layouts for all applications using DIP packages (unassembled)
DEM-OPA2662-1GC	OPA2662	Evaluation Fixture—High speed voltage controlled current source
DEM-PCM1700P-C	PCM1700	Evaluation Fixture—Serial/SPDIF Inputs (Formerly DEM-1143). Includes product.
DEM-PCM1702	PCM1702	Evaluation Fixture—Serial digital input, 8X digital interpolator (NPC5842), and analog output. A PCM1702P is included. The board will interface directly to the DEM-1760. The fixture does not accept SPDIF input.
DEM-PCM1710	PCM1710U	Evaluation Fixture—Serial Digital Audio In. Left and Right channel analog out.

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MODEL	PRODUCT	DESCRIPTION
DEM-DAI1710	PCM1710U	Evaluation Fixture—Includes Digital Audio Interface (DAI) receiver chip and dual 2nd-order lowpass output filters
DEM-PCM1715	PCM1715U	Evaluation Fixture—Serial digital audio in. Left and right channel analog out
DEM-PCM1750P-C	PCM1750	Evaluation Fixture—Serial/Parallel Output, SPDIF Out (Formerly DEM 1133). Includes product.
DEM-PCM1760	PCM1760/DF1760	Evaluation Fixture—Analog input and serial digital output. A PCM1760P and DF1760P are included. The board will interface directly to the DEM-1702. The fixture does not provide SPDIF output.
DEM-PCM63P-C	PCM63P	Evaluation Fixture—Includes Dual PCM63s, SPDIF Input
DEM-PCM67P-C	PCM67P	Evaluation Fixture—Includes Dual PCM67s (single/dual supply operation), SPDIF Input
DEMPCM78P-C	PCM78P	Evaluation Fixture—Analog Input, Parallel Data Output. Includes SHC5320 sample hold and PCM56 as a reconstruction ADC (formerly DEM-1122).
DEM-SHC605AU	SCH605AU	Evaluation Fixture—Analog input, digital control input, and sample/hold output (all SMA connectors). A SHC605AU is included and is soldered to the board.
DEM-SDM862/863-1-SC		SDM862/863 Evaluation Fixture—LCC package, also covers SDM872/873
DEM-SDM862/863-2-SC		SDM862/863 Evaluation Fixture—PGA package, also covers SDM872/873
DEM-VCA610AP-C	VCA610AP	Evaluation Fixture—Voltage Controlled Amplifier

DEMONSTRATION BOARDS

A

Appendix B

Cross Reference Guide

Definitions of pin compatibility: P/P = Pin for Pin. A true second source. F/E = Functional Equivalent. Very similar function and performance, but

not pin for pin. C/P = Closest Part. Similar function and performance, but with significant differences.

Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility	
1480	Teledyne-Philbrick	3583JM	P/P
175	Calex	INA101AM	F/E
175L	Calex	INA101AM	F/E
176J	Calex	INA101AM	F/E
176K	Calex	INA101AM	F/E
176L	Calex	INA101AM	F/E
178	Calex	INA101AM	F/E
286J	Analog Devices	3656	F/E
290A	Analog Devices	ISO122P	C/P
433	Analog Devices	4302	F/E
436	Analog Devices	MPY100AG	F/E
6M4314	Gennum	MPC100AP	C/P
6M8108	Gennum	MPC100AP	C/P
6X414A	Gennum	MPC100AP	F/E
6X4201	Gennum	MPC100AP	C/P
6X4304	Gennum	MPC100AP	C/P
6X434	Gennum	MPC100AP	F/E
757	Analog Devices	LOG100JP	F/E
7580	Beckman	DAC80-CBI-V	P/P
877-80	Beckman	DAC80-CBI-V	P/P
877-85	Beckman	DAC85H-CBI-V	P/P
AD OP-27	Analog Devices	OPA27	P/P
AD OP-37	Analog Devices	OPA37	P/P
AD101A	Analog Devices	3507J	C/P
AD101	Intersil (Harris)	3507J	C/P
AD1139	Analog Devices	DAC729JH	F/E
AD1145	Analog Devices	DAC709KH	F/E
AD1147	Analog Devices	DAC729JH	C/P
AD1148	Analog Devices	DAC729JH	C/P
AD1154	Analog Devices	SHC702JM	F/E
AD1201	Intech	ADC601JG	F/E
AD1341	Analog Devices	SDM862	F/E
AD1376	Analog Devices	ADC76JG	P/P
AD1376	Analog Devices	PCM75	P/P
AD1380	Analog Devices	ADC700JH	C/P
AD1674	Analog Devices	ADS774JP	F/E
AD1678	Analog Devices	ADS7800AH	F/E
AD171	Analog Devices	3582J	C/P
AD1856	Analog Devices	PCM56P	P/P
AD1860	Analog Devices	PCM61P	P/P
AD1862	Analog Devices	PCM63P	F/E
AD1864	Analog Devices	PCM1700P	F/E
AD1865	Analog Devices	PCM1700P	F/E
AD1876	Analog Devices	PCM78P	F/E
AD202	Analog Devices	ISO212JP	C/P
AD203	Analog Devices	ISO103	C/P
AD203N	Analog Devices	ISO103	F/E

Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility	
AD204	Analog Devices	ISO212JP	C/P
AD208	Analog Devices	ISO212JP	C/P
AD210	Analog Devices	3656	F/E
AD210	Analog Devices	ISO103	C/P
AD2700	Analog Devices	REF10JM	C/P
AD2701	Analog Devices	REF101JM	C/P
AD2702	Analog Devices	REF101JM	C/P
AD2710	Analog Devices	REF10JM	C/P
AD2712	Analog Devices	REF101JM	F/E
AD289	Analog Devices	ISO102	C/P
AD293	Analog Devices	ISO102	C/P
AD294	Analog Devices	ISO102	C/P
AD295	Analog Devices	3656MG	F/E
AD346	Analog Devices	SHC5320	F/E
AD346	Analog Devices	SHC804BM	F/E
AD3554	Analog Devices	3554AM	C/P
AD363	Analog Devices	SDM872JH	C/P
AD364	Analog Devices	SDM873JH	C/P
AD376	Analog Devices	ADC76JG	P/P
AD380	Analog Devices	OPA605AM	C/P
AD380	Analog Devices	OPA654	F/E
AD381	Analog Devices	OPA606KM	P/P
AD382	Analog Devices	OPA605AM	C/P
AD3860	Analog Devices	DAC811AH	P/P
AD386	Analog Devices	SHC702	F/E
AD386	Analog Devices	SHC76	F/E
AD389	Analog Devices	SHC76KM	P/P
AD390	Analog Devices	DAC4813	F/E
AD503	Analog Devices	OPA121KM	P/P
AD503	Intersil (Harris)	OPA101	P/E
AD504	Analog Devices	OPA27GJ	F/E
AD506	Analog Devices	OPA121KM	P/P
AD507	Analog Devices	3507J	P/P
AD509	Analog Devices	3507J	P/P
AD510	Analog Devices	OPA27GJ	P/P
AD515	Analog Devices	AD515JH	P/P
AD517	Analog Devices	OPA27GJ	F/E
AD518	Analog Devices	3507J	F/E
AD521	Analog Devices	INA101AG	F/E
AD522	Analog Devices	INA101AM	F/E
AD5240	Analog Devices	ADC84KG-12	P/P
AD5240	Analog Devices	ADC85	P/P
AD524	Analog Devices	INA110AG	F/E
AD526	Analog Devices	PGA102	F/E
AD526	Analog Devices	PGA203KP	C/P
AD532	Analog Devices	MPY100AM	P/P
AD533	Analog Devices	MPY100AM	F/E

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
AD534	Analog Devices	MPY534JD	P/P	AD650	Analog Devices	VFC110AP	C/P
AD535	Analog Devices	MPY534JD	F/E	AD651	Analog Devices	VFC100AG	P/P
AD536	Analog Devices	4341	F/E	AD652	Analog Devices	VFC101N	P/P
AD537	Analog Devices	VFC32BM	C/P	AD654	Analog Devices	VFC121AP	C/P
AD538	Analog Devices	4302	F/E	AD662	Analog Devices	DAC667JP	C/P
AD539	Analog Devices	MPY634AM	C/P	AD667	Analog Devices	DAC667JP	P/P
AD542	Analog Devices	OPA121KM	F/E	AD671	Analog Devices	ADC601JG	F/E
AD544	Analog Devices	OPA606KM	F/E	AD671	Analog Devices	ADS602	F/E
AD545A	Analog Devices	OPA111	P/P	AD671	Analog Devices	ADS7800	F/E
AD545	Analog Devices	OPA111AM	P/P	AD674A	Analog Devices	ADC674AJH	P/P
AD546	Analog Devices	OPA121KM	P/P	AD676	Analog Devices	ADS7805	C/P
AD547	Analog Devices	OPA111AM	F/E	AD677	Analog Devices	ADS7809	C/P
AD548	Analog Devices	OPA111AM	F/E	AD678	Analog Devices	ADS7800AH	F/E
AD549	Analog Devices	OPA128JM	F/E	AD679	Analog Devices	ADC700KH	F/E
AD5539	Analog Devices	OPA621KP	F/E	AD683	Analog Devices	SHC804BM	F/E
AD562	Analog Devices	DAC80-CBI-V	C/P	AD693	Analog Devices	XTR101AG	F/E
AD562	Analog Devices	DAC85	C/P	AD694	Analog Devices	XTR110KP	F/E
AD563	Analog Devices	DAC80-CBI-V	C/P	AD704	Analog Devices	OPA404KP	C/P
AD563	Analog Devices	DAC85	C/P	AD705	Analog Devices	OPA177GP	C/P
AD565A	Analog Devices	DAC80-CBI-I	C/P	AD706	Analog Devices	OPA2111KP	C/P
AD565A	Analog Devices	DAC85	C/P	AD707	Analog Devices	OPA177EZ	P/P
AD565	Analog Devices	DAC65	C/P	AD708	Analog Devices	OPA1013AM	C/P
AD565	Analog Devices	DAC80-CBI-I	C/P	AD711	Analog Devices	OPA602AM	P/P
AD565	Maxim	DAC80-CBI-I	C/P	AD711	Analog Devices	OPA604AP	P/P
AD566A	Analog Devices	DAC80-CBI-I	C/P	AD712	Analog Devices	OPA2107AM	C/P
AD566A	Analog Devices	DAC85	C/P	AD712	Analog Devices	OPA2604AP	C/P
AD566	Analog Devices	DAC80-CBI-I	C/P	AD713	Analog Devices	OPA404KP	C/P
AD567	Analog Devices	DAC811AH	F/E	AD7245	Analog Devices	DAC667JP	P/P
AD568	Analog Devices	DAC812BM	F/E	AD7247	Analog Devices	DAC2815	C/P
AD569	Analog Devices	DAC709KH	C/P	AD7248	Analog Devices	DAC667JP	C/P
AD572	Analog Devices	ADC84KG-12	F/E	AD734	Analog Devices	MPY600AP	C/P
AD573	Analog Devices	ADC574AJH	C/P	AD736	Analog Devices	4341	C/P
AD573	Analog Devices	ADS574	C/P	AD737	Analog Devices	4341	C/P
AD574	Analog Devices	ADC574AJH	P/P	AD741	Analog Devices	OPA177GP	P/P
AD578	Analog Devices	ADC80AG-12	F/E	AD743	Analog Devices	OPA627AP	F/E
AD579	Analog Devices	ADC601JG	C/P	AD744	Analog Devices	OPA602	F/E
AD581	Analog Devices	REF102AM	C/P	AD744	Analog Devices	OPA606	F/E
AD582	Analog Devices	SHC298AM	C/P	AD744	Analog Devices	OPA627AP	C/P
AD583	Analog Devices	SHC5320KH	F/E	AD745	Analog Devices	OPA637	P/E
AD584	Analog Devices	REF101JM	C/P	AD746	Analog Devices	OPA2107AP	P/P
AD585	Analog Devices	SHC5320KH	F/E	AD871	Analog Devices	ADS605	C/P
AD587	Analog Devices	REF102BM	P/P	AD872	Analog Devices	ADS805	C/P
AD588	Analog Devices	REF101JM	C/P	AD7501	Analog Devices	MPC508	F/E
AD600	Analog Devices	VCA610	C/P	AD7501	Analog Devices	MPC508	F/E
AD6012	Analog Devices	DAC80-CBI-V	C/P	AD7502	Analog Devices	MPC509	F/E
AD602	Analog Devices	VCA610	C/P	AD7502	Analog Devices	MPC509	F/E
AD606	Analog Devices	INA101AM	F/E	AD7503	Analog Devices	MPC508	C/P
AD611	Analog Devices	OPA121KM	F/E	AD7503	Analog Devices	MPC508	F/E
AD612	Analog Devices	PGA200AG	F/E	AD7503	Analog Devices	MPC508	C/P
AD614	Analog Devices	PGA200AG	F/E	AD7506	Analog Devices	MPC16	P/P
AD620	Analog Devices	INA114	P/E	AD7506	Analog Devices	MPC506	P/P
AD621	Analog Devices	INA131	C/P	AD7506	Analog Devices	MPC506	P/P
AD624	Analog Devices	INA110AG	P/P	AD7507	Analog Devices	MPC507	P/P
AD625	Analog Devices	INA103KP	F/E	AD7507	Analog Devices	MPC507	P/P
AD632	Analog Devices	MPY534	P/E	AD7507	Analog Devices	MPC8	P/P
AD633	Analog Devices	MPY634AM	C/P	AD7521	Analog Devices	DAC7541AJP	P/P
AD642	Analog Devices	OPA2111AM	C/P	AD7521	Intersil (Harris)	DAC7541AJP	P/P
AD644	Analog Devices	OPA2111AM	C/P	AD7521	Maxim	DAC7541AJP	P/P
AD645	Analog Devices	OPA111BM	P/P	AD7521	National Semiconductor	DAC7541AJP	P/P
AD645	Analog Devices	OPA627	F/E	AD7524	Analog Devices	DAC7801	C/P
AD647	Analog Devices	OPA2111AM	F/E	AD7528	Analog Devices	DAC7528	P/P
AD648	Analog Devices	OPA2107AM	F/E	AD7531	Analog Devices	DAC7541AJP	P/P

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Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility		
AD7531	Intersil (Harris)	DAC7541AJP	P/P	ADA160Q	Zeltex	DAC729JH	F/E
AD7531	Maxim	DAC7541AJP	P/P	ADADC80	Analog Devices	ADC80AG-12	P/P
AD7531	National Semiconductor	DAC7541AJP	P/P	ADADC84	Analog Devices	ADC84KG-12	P/P
AD7537	Analog Devices	DAC7801KP	F/E	ADADC85	Analog Devices	ADC85H-12	P/P
AD7538	Analog Devices	DAC702	C/P	ADC-EH12B3	Datel	ADC80AG-12	C/P
AD7541A	Analog Devices	DAC7541AJP	P/P	ADC-HX12B	Datel	ADC84KG-12	P/P
AD7541A	Maxim	DAC7541AJP	P/P	ADC00401	DDC	ADC80AG-12	F/E
AD7541	Analog Devices	DAC7541AJP	P/P	ADC00403	DDC	ADC80AG-12	F/E
AD7541	Intersil (Harris)	DAC7541AJP	P/P	ADC1080	National Semiconductor	ADC80AG-12	P/P
AD7541	Maxim	DAC7541AJP	P/P	ADC1103	Analog Devices	ADC80AG-12	F/E
AD7542	Analog Devices	DAC811AH	C/P	ADC1130	Analog Devices	ADC71JG	C/P
AD7543	Analog Devices	DAC7800KP	C/P	ADC1131	Analog Devices	ADC71JG	C/P
AD7545A	Analog Devices	DAC7545AH	P/P	ADC1140	Analog Devices	ADC71JG	C/P
AD7545	Analog Devices	DAC7545AH	P/P	ADC1280	National Semiconductor	ADC80AG-12	P/P
AD7545	Maxim	DAC7545AH	P/P	ADC386	National Semiconductor	SHC702JM	F/E
AD7546	Analog Devices	DAC707KH	F/E	ADC4450	DDC	ADC80AG-12	F/E
AD7547	Analog Devices	DAC7802KP	F/E	ADC511	Datel	ADC601JG	F/E
AD7548	Analog Devices	DAC811AH	C/P	ADC810	Datel	ADC80AG-12	F/E
AD7549	Analog Devices	DAC7802KP	F/E	ADC811	Datel	ADC80AG-12	F/E
AD7572	Analog Devices	ADC774JH	F/E	ADC817	Datel	ADC80AG-12	F/E
AD7572	Analog Devices	ADS774	F/E	ADC827	Datel	ADC80AG-12	F/E
AD7578	Analog Devices	ADC7802BP	C/P	ADC910	PMI (Analog Devices)	ADS7800	C/P
AD7579	Analog Devices	ADS574JP	C/P	ADC912	PMI (Analog Devices)	ADS774	C/P
AD7580	Analog Devices	ADS574JP	C/P	ADC922	PMI (Analog Devices)	ADS7800	C/P
AD7582	Analog Devices	ADC7802BP	F/E	ADCHX12	Datel	ADC84	P/P
AD759	Analog Devices	LOG100	C/P	ADDAC71	Analog Devices	DAC71-COB-V	P/P
AD766	Analog Devices	PCM56P	F/E	ADDAC72	Analog Devices	DAC72BH-COB-V	P/P
AD7672	Analog Devices	ADS7800JP	F/E	ADDAC80	Analog Devices	DAC80-CBI-V	P/P
AD767	Analog Devices	DAC667JP	F/E	ADDAC85	Analog Devices	DAC85H-CBI-V	P/P
AD767	Analog Devices	DAC811	F/E	ADDAC87	Analog Devices	DAC87H-CBI-V	P/P
AD795	Analog Devices	OPA124	P/P	ADG506A	Analog Devices	MPC506	C/P
AD7772	Analog Devices	ADC804BH	C/P	ADG506A	Analog Devices	MPC506	C/P
AD7845	Analog Devices	DAC667JP	C/P	ADG507A	Analog Devices	MPC507	C/P
AD7848	Analog Devices	DAC667JP	C/P	ADG507A	Analog Devices	MPC507	C/P
AD7870	Analog Devices	ADS774JP	F/E	ADG508A	Analog Devices	MPC508	C/P
AD7878	Analog Devices	ADS774JP	F/E	ADG508A	Analog Devices	MPC508	C/P
AD811	Analog Devices	BUF634	C/P	ADG509A	Analog Devices	MPC509	C/P
AD829	Analog Devices	OPA620KP	F/E	ADG509A	Analog Devices	MPC509	C/P
AD829	Analog Devices	OPA621	F/E	ADH-051	DDC	ADC80AG-12	C/P
AD834	Analog Devices	MPY600AP	C/P	ADH8516	DDC	ADC80AG-12	F/E
AD840	Analog Devices	OPA621KP	C/P	ADH8585	DDC	ADC85H-12	P/P
AD841	Analog Devices	OPA620KP	F/E	ADH8586	DDC	ADC85H-12	F/E
AD842	Analog Devices	OPA621KP	F/E	ADLH0032	Analog Devices	OPA605AM	C/P
AD843	Analog Devices	OPA671AP	F/E	ADLH0033	Analog Devices	OPA633KP	F/E
AD844	Analog Devices	3554AM	C/P	ADOP-07	Analog Devices	OPA177GJ	F/E
AD844	Analog Devices	OPA603	C/P	ADOP-27	Analog Devices	OPA27GJ	P/P
AD845	Analog Devices	OPA637AP	F/E	ADOP-37	Analog Devices	OPA37GJ	P/P
AD846	Analog Devices	OPA603AP	F/E	ADREF01	Analog Devices	REF102AP	P/P
AD847	Analog Devices	OPA671	C/P	ADS130	Datel	ADC603JH	F/E
AD848	Analog Devices	OPA620	C/P	ADVFC32	Analog Devices	VFC32BM	P/P
AD849	Analog Devices	OPA621	C/P	AM6012	Maxim	DAC80-CBI-V	C/P
AD9003	Analog Devices	ADS602JG	F/E	AMP-01	PMI (Analog Devices)	INA101AM	F/E
AD9005	Analog Devices	ADC603JH	F/E	AMP-01	PMI (Analog Devices)	INA104	F/E
AD9300	Analog Devices	MPC100AP	C/P	AMP-02	PMI (Analog Devices)	INA103KP	C/P
AD9610	Analog Devices	OPA600	C/P	AMP-02	PMI (Analog Devices)	INA111	P/P
AD9617	Analog Devices	OPA603AP	F/E	AMP-02	PMI (Analog Devices)	INA114	P/P
AD9617	Analog Devices	OPA644	P/P	AMP-02	PMI (Analog Devices)	INA114	P/E
AD9618	Analog Devices	OPA603AP	F/E	AMP-03	PMI (Analog Devices)	INA105KP	P/E
AD9620	Analog Devices	OPA633KP	C/P	AMP-05	PMI (Analog Devices)	INA110AG	F/E
AD9630	Analog Devices	BUF601	P/E	BB3553	Maxim	3553AM	P/P
AD9712	Analog Devices	DAC65JP	F/E	BB3554	Maxim	3554AM	P/P
AD9713	Analog Devices	DAC65	F/E	BT104	Brooktree	DAC65JP	C/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
BT105	Brooktree	DAC65JP	C/P	DAC377	Sipex	DAC729JH	C/P
BUF-03	PMI (Analog Devices)	BUF634	C/P	DAC391	Hybrid	DAC812BM	C/P
BUF-03	PMI (Analog Devices)	OPA633		DAC612	Datel	DAC811AH	C/P
CAV1210	Analog Devices	ADC603JH	C/P	DAC7528	Analog Devices	DAC7528	P/P
CLC400	Comlinear	OPA620KG	C/P	DAC8043	Analog Devices	DAC8043	P/P
CLC401	Comlinear	OPA620KG	C/P	DAC8221	PMI (Analog Devices)	DAC7802KP	F/E
CLC404	Comlinear	OPA623	C/P	DAC8222	PMI (Analog Devices)	DAC7802KP	F/E
CLC409	Comlinear	OPA623	P/E	DAC87	DDC	DAC87H-CBI-V	P/P
CLC411	Comlinear	OPA623	C/P	DAC9332-16	Hybrid	DAC709KH	F/E
CLC500	Comlinear	OPA620KG	F/E	DAC9349	Hybrid	DAC80-CBI-V	C/P
CLC501	Comlinear	OPA620KG	F/E	DAC9377	Hybrid	DAC707KH	F/E
CLC520	Comlinear	VCA610	C/P	DACHK	Micro Networks	DAC811AH	F/E
CLC912	Comlinear	DAC65JP	F/E	DACHP16	Datel	DAC701	P/P
CLC925	Comlinear	ADC603	C/P	DACHP16	Datel	DAC703	P/P
CLC925	Comlinear	ADC603JH	F/E	DACHZ12	Datel	DAC85	P/P
CLC926	Comlinear	ADC603JH	F/E	DAS1128	Analog Devices	SDM873JH	F/E
CS5102A	Crystal	ADS7807	C/P	DG506A	Maxim	MPC506	P/E
CS5101A	Crystal	ADS7809	C/P	DG506	Silconix	MPC506	P/P
CS5326	Crystal Semiconductor	PCM1750P	C/P	DG506	Silconix	MPC16	P/P
CS5327	Crystal Semiconductor	PCM1750P	C/P	DG506	Silconix	MPC506	P/P
CS5328	Crystal Semiconductor	PCM1750P	C/P	DG507A	Maxim	MPC507	P/E
CS5329	Crystal Semiconductor	PCM1750P	C/P	DG507	Silconix	MPC507	P/P
CS5336	Crystal Semiconductor	PCM1750P	C/P	DG507	Silconix	MPC507	P/P
CS5337	Crystal Semiconductor	PCM1750P	C/P	DG507	Silconix	MPC8	P/P
CS5338	Crystal Semiconductor	PCM1750P	C/P	DG508A	Maxim	MPC508	P/E
CS533P	Crystal Semiconductor	PCM1750P	C/P	DG508	Silconix	MPC508	P/P
D6534	Silconix	MPC100AP	C/P	DG508	Silconix	MPC508	P/P
D6538	Silconix	MPC100AP	C/P	DG508	Silconix	MPC8	P/P
D6884	Silconix	MPC100AP	C/P	DG509A	Maxim	MPC509	P/E
D6894	Silconix	MPC100AP	C/P	DG509	Silconix	MPC509	P/P
DAC-01	PMI (Analog Devices)	NONE		DG509	Silconix	MPC509	P/P
DAC-02	PMI (Analog Devices)	NONE		DG509	Silconix	MPC4	P/P
DAC-03	PMI (Analog Devices)	NONE		EL2001	Elantek	BUF634	C/P
DAC-08	PMI (Analog Devices)	NONE		EL2002	Elantek	BUF634	C/P
DAC-10	PMI (Analog Devices)	NONE		EL2003	Elantek	OPA633KP	P/P
DAC-20	PMI (Analog Devices)	NONE		EL2007	Elantek	OPA541AM	C/P
DAC-71	Datel	DAC71-COB-V	P/P	EL2008	Elantek	BUF634	C/P
DAC-72	Datel	DAC72BH-COB-V	P/P	EL2009	Elantek	BUF634	C/P
DAC-86	PMI (Analog Devices)	NONE		EL2020	Elantek	OPA603AP	C/P
DAC-HF12B	Datel	DAC812BM	C/P	EL2030	Elantek	OPA603AP	C/P
DAC-HF12	Datel	DAC65JP	F/E	EL2072	Elantek	BUF601	P/P
DAC-HK12B	Datel	DAC811AH	F/E	GX434	Gennum	MPC100	C/P
DAC-HP16	Datel	DAC71-COB-V	P/P	HA-2400	Harris	OPA676JG	F/E
DAC-HY12	Datel	DAC80-CBI-V	P/P	HA-2420	Harris	SHC5320KH	C/P
DAC-HZ12B	Datel	DAC85H-CBI-V	P/P	HA-2425	Harris	SHC5320KH	C/P
DAC-S	DDC	DAC85H-CBI-V	P/P	HA-2500	Harris	3507J	F/E
DAC-SL	DDC	DAC811AH	F/E	HA-2505	Harris	OPA602	P/E
DAC02701	DDC	DAC811AH	F/E	HA-2510	Harris	3507J	F/E
DAC1136	Analog Devices	DAC729JH	P/P	HA-2520	Harris	3507J	P/P
DAC1138	Analog Devices	DAC729KH	F/E	HA-2525	Harris	3507	P/P
DAC1208	National Semiconductor	DAC811AH	F/E	HA-2539	Harris	OPA605AM	C/P
DAC1218	National Semiconductor	DAC7541AJP	F/E	HA-2540	Harris	OPA605AM	C/P
DAC1219	National Semiconductor	DAC7541AJP	F/E	HA-2541	Harris	OPA605AM	C/P
DAC1230	National Semiconductor	DAC811AH	F/E	HA-2542	Harris	OPA605AM	C/P
DAC1280	National Semiconductor	DAC80-CBI-V	P/P	HA-2546	Harris	MPY600AP	C/P
DAC1285	National Semiconductor	DAC85H-CBI-V	P/P	HA-2547	Harris	MPY600AP	C/P
DAC1286	National Semiconductor	DAC80-CBI-V	P/P	HA-2600	Harris	3507J	C/P
DAC1287	National Semiconductor	DAC87H-CBI-V	P/P	HA-2605	Harris	3507	P/E
DAC331	Hybrid	DAC7541AJP	F/E	HA-2620	Harris	3507J	P/P
DAC336-12	Hybrid	DAC811AH	F/E	HA-2625	Harris	3507	P/E
DAC347	Hybrid	DAC7541AJP	F/E	HA-2630	Harris	3553AM	C/P
DAC377	Hybrid	DAC729JH	C/P	HA-2640	Harris	OPA445M	P/E

Or, Call Customer Service at 1-800-548-6132 (USA Only)

Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number	Burr-Brown Part Number	Pin Compatibility		
HA-2645	Harris	OPA445AP	P/E	HI-547-5	Harris	MPC8D	P/P
HA-2645	Harris	OPA445BM	C/P	HI-548-5	Harris	MPC8S	P/P
HA-2650	Harris	OPA2111AM	C/P	HI-549-5	Harris	MPC4D	P/P
HA-4156	Harris	OPA404AG	C/P	HI-5660	Harris	DAC80-CBI-V	C/P
HA-4741	Harris	OPA404AG	C/P	HI-5680	Harris	DAC80-CBI-V	P/P
HA-5002	Harris	OPA633KP	C/P	HI-5685	Harris	DAC85H-CBI-V	P/P
HA-5004	Harris	OPA603AP	C/P	HI-5687	Harris	DAC87H-CBI-V	P/P
HA-5033	Harris	OPA633KP	P/P	HI-5690	Harris	DAC80-CBI-V	C/P
HA-5062	Harris	OPA2111AM	C/P	HI-5695	Harris	DAC85H-CBI-V	C/P
HA-5064	Harris	OPA404AG	F/E	HI-574A	Harris	ADC574AJH	P/P
HA-5082	Harris	OPA2111AM	F/E	HI-5811	Harris	DAC811AH	P/P
HA-5084	Harris	OPA404AG	F/E	HI-674A	Harris	ADC674A	P/P
HA-5100	Harris	OPA606KM	C/P	HI-774A	Harris	ADC774JP	P/P
HA-5102	Harris	OPA2111AM	C/P	HI-774	Harris	ADC774JP	P/P
HA-5104	Harris	OPA404AG	F/E	HI-DAC16	Harris	DAC71-COB-V	F/E
HA-5110	Harris	3551J	F/E	HI518	Harris	MPC801	P/P
HA-5112	Harris	OPA2111AM	C/P	HI574	Harris	ADC574	P/P
HA-5114	Harris	OPA404AG	F/E	HI674	Harris	ADC674	P/P
HA-5130	Harris	OPA27GJ	F/E	HOS-050	Analog Devices	3554AM	C/P
HA-5135	Harris	OPA27GJ	F/E	HOS-060	Analog Devices	3554AM	C/P
HA-5142	Harris	OPA2111AM	C/P	HOS-100	Analog Devices	OPA633KP	P/P
HA-5144	Harris	OPA404AG	C/P	HOS-200	Analog Devices	OPA633KP	F/E
HA-5147	Harris	OPA37GJ	F/E	HS3120	Hybrid	DAC811AH	F/E
HA-5160	Harris	OPA602AM	F/E	HS3160	Hybrid	DAC703KH	C/P
HA-5170	Harris	OPA111AM	F/E	HS346	Hybrid	SHC5320KH	C/P
HA-5180	Harris	OPA111AM	P/P	HS3860	Hybrid	DAC811AH	F/E
HA-5190	Harris	OPA605AM	C/P	HS7541	Hybrid	DAC7541AJP	P/P
HA-5320	Harris	SHC5320KH	P/P	HS7545	Hybrid	DAC7545AH	P/P
HA-5330	Harris	SHC803BM	C/P	HS9338	Hybrid	DAC811AH	F/E
HA-OP07	Harris	OPA177GZ	P/P	HS9377	Hybrid	DAC707KH	F/E
HA-OP27	Harris	OPA27GJ	P/P	HS9378	Hybrid	DAC707KH	F/E
HA-OP37	Harris	OPA37GJ	P/P	HS9393	Hybrid	DAC65JP	F/E
HA6033	Harris	BUF634	C/P	HS9394	Hybrid	DAC65JP	F/E
HAS-050	Analog Devices	3554AM	C/P	HS9410	Hybrid	SDM872JH	C/P
HAS-1202A	Analog Devices	ADC80AG-12	C/P	HS9576	Hybrid	ADC76JG	P/P
HAS-1202	Analog Devices	ADC80AG-12	F/E	HSDAC80	Hybrid	DAC80-CBI-V	P/P
HDAS-16	Datel	SDM857JG	F/E	HSDAC87	Hybrid	DAC87H-CBI-V	P/P
HDAS-8	Datel	SDM857JG	F/E	HT0025	Analog Devices	SHC600BH	F/E
HDS1240	Analog Devices	DAC65JP	F/E	HTC0300	Analog Devices	SHC804BM	P/P
HFA1100	Harris	BUF600	C/P	HTS0010	Analog Devices	SHC600BH	F/E
HFA1100	Harris	OPA623	C/P	HY6110	Hytek	PGA200AG	C/P
HFA1112	Harris	BUF601	C/P	ICH8515	Intersil (Harris)	OPA541AM	C/P
HFA1120	Harris	OPA623	C/P	ICL7134	Intersil (Harris)	DAC709KH	C/P
HFA5033	Harris	BUF600	C/P	ICL7145	Intersil (Harris)	DAC707KH	C/P
HI-0508	Maxim	MPC508	P/P	ICL7146	Intersil (Harris)	DAC811AH	C/P
HI-0508	Maxim	MPC508	P/P	ICL7605	Intersil (Harris)	INA101AM	F/E
HI-0509	Maxim	MPC509	P/P	ICL7606	Intersil (Harris)	INA101AM	F/E
HI-0509	Maxim	MPC509	P/P	ICL8013	Intersil (Harris)	MPY100	F/E
HI-506	Harris Semiconductor	MPC16	P/P	IH5108	Harris	MPC8	P/P
HI-506	Harris	MPC506	P/P	IH5108	Harris	MPC801	P/P
HI-507	Harris	MPC507	P/P	IH5108	Intersil (Harris)	MPC508	P/P
HI-507	Harris	MPC8	P/P	IH5110-15	Intersil (Harris)	SHC298AM	C/P
HI-508	Harris	MPC508	P/P	IH5208	Harris	MPC4	P/P
HI-508	Harris	MPC8	P/P	IH5208	Harris	MPC801	P/P
HI-508	Maxim	MPC508	P/P	IH5208	Intersil (Harris)	MPC507	P/P
HI-509	Harris	MPC509	P/P	IH6108	Harris	MPC8	P/P
HI-5127	Harris	OPA27	P/E	IH6108	Harris	MPC801	P/P
HI-5137	Harris	OPA37	P/E	IH6108	Intersil (Harris)	MPC508	P/P
HI-516	Harris	MPC800	P/P	IH6116	Harris	MPC800	P/P
HI-516	Harris	MPC800KG	P/P	IH6116	Intersil (Harris)	MPC506	P/P
HI-518	Harris	MPC801KG	P/P	IH6216	Harris	MPC8	P/P
HI-546-5	Harris	MPC16S	P/P	IH6216	Intersil (Harris)	MPC507	P/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
LF11508	National Semiconductor	MPC508	P/P	LH740A	National Semiconductor	OPA121KM	P/P
LF11509	National Semiconductor	MPC509	P/P	LM101A	LTC	OPA27GJ	C/P
LF13741	National Semiconductor	OPA121KM	P/P	LM101A	National Semiconductor	OPA27GJ	C/P
LF155A	LTC	OPA606KM	F/E	LM107	LTC	OPA177GP	C/P
LF155A	National Semiconductor	OPA606KM	F/E	LM107	National Semiconductor	OPA177GP	C/P
LF156A	LTC	OPA606KM	F/E	LM112	LTC	OPA27EJ	C/P
LF156A	National Semiconductor	OPA606KM	F/E	LM112	National Semiconductor	OPA27EJ	C/P
LF157A	National Semiconductor	OPA606KM	F/E	LM118	Harris	3507J	C/P
LF198	National Semiconductor	SHC298AM	P/P	LM118	LTC	3507	C/P
LF198	Texas Instruments	SHC298	P/P	LM118	National Semiconductor	3507J	C/P
LF298	National Semiconductor	SHC298	P/P	LM11C	Motorola	OPA602	P/E
LF351	Motorola	OPA604	P/E	LM12	National Semiconductor	OPA541AM	C/P
LF351	Motorola	OPA604	P/E	LM131	National Semiconductor	VFC32BM	C/P
LF351	National Semiconductor	OPA156AM	P/P	LM143	National Semiconductor	OPA445BM	C/P
LF353	Harris	OPA2111AM	P/P	LM144	National Semiconductor	OPA445BM	C/P
LF353	Motorola	OPA2111	P/P	LM1558	National Semiconductor	OPA2111AM	C/P
LF353	National Semiconductor	OPA2111AM	P/P	LM158A	National Semiconductor	OPA2111AM	C/P
LF355	LTC	OPA121	P/E	LM163	National Semiconductor	INA101AM	F/E
LF356	LTC	OPA121	P/E	LM185	LTC	REF1004	F/E
LF356	Motorola	OPA602	P/E	LM208	Intersil (Harris)	ISO212JP	C/P
LF357	Motorola	OPA637	C/P	LM2904	National Semiconductor	OPA2111AM	C/P
LF398A	National Semiconductor	SHC298AM	P/P	LM307	Motorola	OPA77	P/P
LF398	National Semiconductor	SHC298AM	P/P	LM318	LTC	3507	C/P
LF398	Texas Instruments	SHC298	P/P	LM324	National Semiconductor	OPA1013	C/P
LF400C	National Semiconductor	OPA606KM	F/E	LM331	National Semiconductor	VFC32BM	C/P
LF411	National Semiconductor	OPA602AM	P/P	LM334	National Semiconductor	REF200AM	C/P
LF412A	National Semiconductor	OPA2111AM	F/E	LM343	National Semiconductor	OPA445BM	C/P
LF412	National Semiconductor	OPA2111	P/P	LM358	Motorola	OPA1013	C/P
LF441	Motorola	OPA606	P/E	LM358	National Semiconductor	OPA2111AM	C/P
LF442A	National Semiconductor	OPA2111AM	F/E	LM363	National Semiconductor	INA101HP	F/E
LF444A	National Semiconductor	OPA404AG	P/P	LM607	National Semiconductor	OPA27GJ	C/P
LH0002	National Semiconductor	3553AM	C/P	LM6125	National Semiconductor	BUF634	C/P
LH0003	National Semiconductor	3507J	C/P	LM627	National Semiconductor	OPA627	P/P
LH0004	National Semiconductor	3580J	C/P	LM6361	National Semiconductor	3507	F/E
LH0005	National Semiconductor	OPA605AM	C/P	LM637	National Semiconductor	OPA637	P/P
LH0021	National Semiconductor	3571	C/P	LM675	National Semiconductor	OPA511AM	C/P
LH0022	National Semiconductor	OPA121KM	P/P	LM709A	National Semiconductor	3507J	C/P
LH0023	National Semiconductor	SHC298AM	C/P	LM725A	National Semiconductor	OPA27EJ	C/P
LH0024	National Semiconductor	3551J	F/E	LM747A	National Semiconductor	OPA2111AM	C/P
LH0032	National Semiconductor	OPA605AM	C/P	LM748	National Semiconductor	OPA27EJ	C/P
LH0033	National Semiconductor	OPA633KP	F/E	LM833	Motorola	OPA2107	C/P
LH0036	National Semiconductor	INA114	C/P	LM837	National Semiconductor	OPA404AG	C/P
LH0038	National Semiconductor	INA114	C/P	LMC660	National Semiconductor	OPA404AG	C/P
LH0042	National Semiconductor	OPA121KM	P/P	LT1001CN8	LTC	OPA177GP	P/P
LH0043	National Semiconductor	SHC298AM	C/P	LT1001	LTC	OPA27GJ	F/E
LH0044	National Semiconductor	OPA27GJ	F/E	LT1002	LTC	OPA2111AM	C/P
LH0052	National Semiconductor	OPA111AM	P/P	LT1004	LTC	REF1004	P/P
LH0053	National Semiconductor	SHC5320KH	C/P	LT1007	LTC	OPA27GJ	P/P
LH0053	National Semiconductor	SHC85	C/P	LT1010	Linear Technology	BUF634	C/P
LH0063	National Semiconductor	3553AM	F/E	LT1010	LTC	OPA633KP	C/P
LH0070	LTC	REF10	C/P	LT1013	LTC	OPA1013ACH	P/P
LH0084	National Semiconductor	PGA200AG	F/E	LT1013	Texas Instruments	OPA1013	P/P
LH0086	National Semiconductor	PGA102AG	F/E	LT1014	LTC	OPA404AG	C/P
LH0091	National Semiconductor	4341	C/P	LT1019	LTC	REF10JM	C/P
LH0094	National Semiconductor	4302	F/E	LT1021	LTC	REF102AM	P/P
LH0101	Maxim	OPA541AM	C/P	LT1022	LTC	OPA606KM	P/P
LH0101	National Semiconductor	OPA541AM	C/P	LT1023	LTC	OPA606KM	C/P
LH2011	National Semiconductor	OPA2111AM	C/P	LT1024	LTC	OPA2111AM	C/P
LH2101A	National Semiconductor	OPA2111AM	C/P	LT1025	LTC	OPA603	C/P
LH2108A	LTC	OPA2111AM	C/P	LT1027	LTC	REF02	C/P
LH2108A	National Semiconductor	OPA2111AM	C/P	LT1028	LTC	OPA27GJ	C/P
LH4001	National Semiconductor	OPA633KP	C/P	LT1031	LTC	REF10	C/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
LT1037	LTC	OPA37GJ	P/P	MN5291	Micro Networks	ADC76JG	C/P
LT1055	LTC	OPA606KM	P/P	MN5610	Micro Networks	ADC84KG-12	F/E
LT1056	LTC	OPA606KM	P/P	MN574A	Micro Networks	ADC574AJH	P/P
LT1057	LTC	OPA2111AM	C/P	MN7100	Micro Networks	SDM872JH	F/E
LT1058	LTC	OPA404AG	F/E	MN7130	Micro Networks	SDM862JH	F/E
LT1117	LTC	REG1117	P/P	MN7150	Micro Networks	SDM873JH	F/E
LT118A	LTC	3507J	F/E	MNADC80	Micro Networks	ADC80AG-12	P/P
LT1223	LTC	OPA623	C/P	MNADC84	Micro Networks	ADC84KG-12	P/P
LT581	LTC	REF10	C/P	MNADC85	Micro Networks	ADC85H-12	P/P
LTC1272	LTC	ADS7800	C/P	MNADC87	Micro Networks	ADC87H-12	P/P
LTC1278	LTC	ADS7810	C/P	MNDAC80	Micro Networks	DAC80-CBI-V	P/P
MAX195	Maxim	ADS7809	C/P	MNDAC85	Micro Networks	DAC85H-CBI-V	P/P
MAX310	Maxim	MPC100AP	C/P	MNDAC87	Micro Networks	DAC87H-CBI-V	P/P
MAX311	Maxim	MPC100AP	C/P	MNDAC88	Micro Networks	DAC811AH	F/E
MAX358	Maxim	MPC508	P/P	MP574	Micro Power Systems	ADC574AJH	P/P
MAX359	Maxim	MPC509	P/P	MP6812	Analogic	SDM863JH	F/E
MAX450	Maxim	MPC100AP	C/P	MP7506	Micro Power Systems	MPC16	P/P
MAX453	Maxim	MPC100AP	C/P	MP7506	Micro Power Systems	MPC506	P/P
MAX454	Maxim	MPC100AP	F/E	MP7507	Micro Power Devices	MPC8	P/P
MAX456	Maxim	MPC100AP	C/P	MP7507	Micro Power Systems	MPC507	P/P
MAX543	Maxim	DAC8043	P/P	MP7508	Micro Power Devices	MPC8	P/P
MAX7528	Maxim	DAC7528	P/P	MP7508	Micro Power Systems	MPC508	P/P
MAX7537	Maxim	DAC7801KP	F/E	MP7509	Micro Power Devices	MPC4	P/P
MAX7547	Maxim	DAC7802KP	F/E	MP7509	Micro Power Systems	MPC509	P/P
MC1456	Motorola	OPA2604	C/P	MP7531	Micro Power Systems	DAC7541AJP	P/P
MC1458	Motorola	OPA2604	C/P	MP7541A	Micro Power Systems	DAC7541AJP	P/P
MC1595	Motorola	MPY600AP	C/P	MP7542	Micro Power Systems	DAC7545AH	C/P
MC1596	Motorola	MPY600AP	C/P	MP7545	Micro Power Systems	DAC7541AJP	P/P
MC1741	Motorola	OPA177	P/P	MP7616	Micro Power Systems	DAC703KH	C/P
MC1747	Motorola	OPA1013	C/P	MP7621	Micro Power Systems	DAC7541AJP	P/P
MC34001	Motorola	OPA602	P/P	MP7622	Micro Power Systems	DAC7545AH	C/P
MC34002	Motorola	OPA2604	C/P	MP7623	Micro Power Systems	DAC7541AJP	P/P
MC34080	Motorola	OPA602	C/P	MP8014	Analogic	ADC76JG	F/E
MC34080	Motorola	OPA606	C/P	MP8016	Analogic	ADC76JG	F/E
MC34081	Motorola	OPA602	P/P	MP8116	Analogic	DAC729JH	F/E
MC34082	Motorola	OPA2604	C/P	MP9331-16	Micro Power Systems	DAC709KH	F/E
MC34083	Motorola	OPA2107	P/P	MP9377-16	Micro Power Systems	DAC707KH	F/E
MC34181	Motorola	OPA111	F/E	MP1814	Analogic	DAC70BH-COB-I	F/E
MC34182	Motorola	OPA2111	C/P	MP1914	Analogic	DAC70BH-COB-I	F/E
MC3458	Motorola	OPA1013	C/P	MUX08	Analog Devices	MPC8	C/P
MC4558	Motorola	OPA2604	C/P	MUX08	PMI (Analog Devices)	iMPC508	P/P
MDAS-16	Datel	SDM872JG	C/P	MUX16	Analog Devices	MPC16	P/P
MDAS-8D	Datel	SDM873JH	F/E	MUX16	PMI (Analog Devices)	MPC506	P/P
MN0300A	Micro Networks	SHC804BM	F/E	MUX24	PMI (Analog Devices)	MPC4	P/P
MN2020	Micro Networks	PGA102AG	C/P	MUX24	PMI (Analog Devices)	MPC509	P/P
MN3210	Micro Networks	DAC71-COB-V	P/P	MUX28	Analog Devices	MPC8	C/P
MN3300	Micro Networks	DAC71-COB-V	P/P	MUX28	PMI (Analog Devices)	MPC507	P/P
MN3310	Micro Networks	DAC703KH	P/P	MX-1606	Datel	MPC506	P/P
MN3660	Micro Networks	DAC811AH	C/P	MX-808	Datel	MPC508	P/P
MN375	Micro Networks	SHC804BM	F/E	MX-818	Datel	MPC801KG	P/P
MN376	Micro Networks	SHC804BM	F/E	MX1606	Datel	MPC16	P/P
MN379	Micro Networks	SHC600BH	F/E	MX1616	Datel	MPC800	P/P
MN3850	Micro Networks	DAC85H-CBI-V	P/P	MX1616	Datel	MPC800KG	P/P
MN3860	Micro Networks	DAC811AH	F/E	MX808	Datel	MPC508	P/P
MN5200	Micro Networks	ADC84KG-12	F/E	MX808	Datel	MPC8S	P/P
MN5210-14	Micro Networks	ADC84KG-12	F/E	MX818	Datel	MPC801	P/P
MN5245	Micro Networks	ADC80AG-12	F/E	MXD-409	Datel	MPC509	P/P
MN5246	Micro Networks	ADC601JG	F/E	MXD-807	Datel	MPC507	P/P
MN5248	Micro Networks	ADC601	P/P	MXD409	Datel	MPC4	P/P
MN5280	Micro Networks	ADC71JG	C/P	MXD409	Datel	MPC509	P/P
MN5282	Micro Networks	ADC71JG	C/P	MXD807	Datel	MPC507	P/P
MN5290	Micro Networks	ADC76JG	C/P	MXD807	Datel	MPC8	P/P

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Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
NE5532	Signetics	OPA2604	P/P	OP-420	PMI (Analog Devices)	OPA404AG	C/P
NE5534	Signetics	OPA604	P/P	OP-421	PMI (Analog Devices)	OPA404AG	C/P
OMA2541	Omnirel	OPA2541	P/P	OP-42	PMI (Analog Devices)	OPA101	C/P
OMA501	Omnirel	OPA501	P/P	OP-42	PMI (Analog Devices)	OPA602AM	F/E
OMA502	Omnirel	OPA502	P/P	OP-43	PMI (Analog Devices)	OPA111AM	F/E
OMA511	Omnirel	OPA511	P/P	OP-44	PMI (Analog Devices)	OPA602AM	C/P
OMA512	Omnirel	OPA512	P/P	OP-470	PMI (Analog Devices)	OPA404AG	C/P
OMA541	Omnirel	OPA541M	P/P	OP-47	Raytheon	OPA37GJ	F/E
MP7610AN	MicroPower Systems	DAC7610P	P/P	OP-50	PMI (Analog Devices)	OPA27GJ	C/P
MP7610AS	MicroPower Systems	DAC7610U	P/P	OP-77	PMI (Analog Devices)	OPA77EZ	P/P
MP7610BN	MicroPower Systems	DAC7610PB	P/P	OP-80	PMI (Analog Devices)	OPA128JM	F/E
MP7610BS	MicroPower Systems	DAC7610UB	P/P	OP-80	PMI (Analog Devices)	OPA128JM	F/E
MP7611AE	MicroPower Systems	DAC7611U	P/P	OP07	LTC	OPA177	P/E
MP7611BE	MicroPower Systems	DAC7611UB	P/P	OP471	PMI (Analog Devices)	OPA404	F/E
MP7612AN	MicroPower Systems	DAC7612P	P/P	PA01	Apex	OPA511AM	P/P
MP7612AS	MicroPower Systems	DAC7612U	P/P	PA02	Apex	OPA541AM	C/P
MP7612BN	MicroPower Systems	DAC7612PB	P/P	PA07	Apex	OPA512BM	C/P
MP7612BS	MicroPower Systems	DAC7612UB	P/P	PA08	Apex	3583JM	C/P
MP7613AE	MicroPower Systems	DAC7613U	P/P	PA10	Apex	OPA512BM	F/E
MP7613BE	MicroPower Systems	DAC7613UB	P/P	PA11	Apex	OPA511AM	P/P
OP-01	PMI (Analog Devices)	OPA606KM	C/P	PA12A	Apex	OPA512SM	P/P
OP-04	PMI (Analog Devices)	OPA2111AM	C/P	PA12	Apex	OPA502	P/P
OP-05	LTC	OPA27GJ	F/E	PA12	Apex	OPA512BM	P/P
OP-05	PMI (Analog Devices)	OPA27GJ	F/E	PA25	Apex	OPA2541	C/P
OP-05	Raytheon/LTC	OPA27GJ	F/E	PA51	Apex	OPA501AM	P/P
OP-05	Raytheon	OPA27GJ	F/E	PA61	Apex	OPA512BM	C/P
OP-06	PMI (Analog Devices)	OPA37GJ	C/P	PA73	Apex	3573AM	P/P
OP-07	LTC	OPA177GZ	P/P	PA80	Apex	3580J	P/P
OP-07	PMI (Analog Devices)	OPA177GZ	P/P	PA81	Apex	3581J	P/P
OP-07	Raytheon/LTC	OPA177GZ	P/P	PA82	Apex	3582J	P/P
OP-07	Raytheon	OPA177GZ	P/P	PA83	Apex	3583JM	P/P
OP-08	PMI (Analog Devices)	OPA1111AM	C/P	PA84	Apex	3584JM	P/P
OP-10	PMI (Analog Devices)	OPA2111AM	C/P	PM155A	PMI (Analog Devices)	OPA156AM	P/P
OP-111	PMI (Analog Devices)	OPA1111AM	P/P	PM156A	PMI (Analog Devices)	OPA156AM	P/P
OP-14	PMI (Analog Devices)	OPA2111AM	C/P	PM157A	PMI (Analog Devices)	OPA606KM	F/E
OP-15	LTC	OPA606KM	P/P	PM2108A	PMI (Analog Devices)	OPA2111AM	C/P
OP-15	PMI (Analog Devices)	OPA606KM	P/P	PM725	PMI (Analog Devices)	OPA27GJ	F/E
OP-16	LTC	OPA606KM	P/P	PM747	PMI (Analog Devices)	OPA2111AM	C/P
OP-16	PMI (Analog Devices)	OPA606KM	P/P	PM7541	PMI (Analog Devices)	DAC7541AJP	P/P
OP-177	PMI (Analog Devices)	OPA177GP	P/P	PM7545	PMI (Analog Devices)	DAC7545AH	P/P
OP-17	LTC	OPA606KM	F/E	PM8012	PMI (Analog Devices)	DAC7545AH	F/E
OP-17	PMI (Analog Devices)	OPA606KM	F/E	RC1458	Raytheon	OPA2111AM	C/P
OP-200	PMI (Analog Devices)	OPA1013	C/P	RC2041	Raytheon	OPA2111AM	C/P
OP-207	PMI (Analog Devices)	OPA2111AM	C/P	RC2043	Raytheon	OPA2111AM	C/P
OP-215	PMI (Analog Devices)	OPA2111AM	C/P	RC4136	Raytheon	OPA404AG	C/P
OP-220	PMI (Analog Devices)	OPA1013	C/P	RC4153	Raytheon	VFC320BM	C/P
OP-220	PMI (Analog Devices)	OPA2111AM	C/P	RC4156	Raytheon	OPA404AG	C/P
OP-221	PMI (Analog Devices)	OPA2111AM	C/P	RC4558	Raytheon	OPA2111AM	C/P
OP-227	LTC	OPA2111AM	C/P	RC4559	Raytheon	OPA2111AM	C/P
OP-227	PMI (Analog Devices)	OPA2111AM	C/P	RC4560	Raytheon	OPA2111AM	C/P
OP-237	LTC	OPA2111AM	C/P	RC4562	Raytheon	OPA2111AM	C/P
OP-260	PMI (Analog Devices)	OPA603AP	C/P	RC4739	Raytheon	OPA2111AM	C/P
OP-275	PMI (Analog Devices)	OPA2604	F/E	RC5532	Raytheon	OPA2111AM	C/P
OP-27	PMI (Analog Devices)	OPA27GJ	P/P	RC5534	Raytheon	OPA37GJ	F/E
OP-27	Raytheon	OPA27GJ	P/P	RC714	Raytheon	OPA27GJ	P/P
OP-285	PMI (Analog Devices)	OPA2107	F/E	RC747	Raytheon	OPA2111AM	C/P
OP-297	PMI (Analog Devices)	OPA1013	C/P	REF-01	LTC	REF102AM	F/E
OP-37	PMI (Analog Devices)	OPA37GJ	P/P	REF01	Maxim	REF102AM	P/P
OP-37	Raytheon	OPA37GJ	P/P	REF01	PMI (Analog Devices)	REF102AM	P/P
OP-400	PMI (Analog Devices)	OPA404AG	C/P	REF02AH	LTC	REF02RM	P/P
OP-41	PMI (Analog Devices)	OPA103	F/E	REF02AJ	Analog Devices	REF02RM	P/P
OP-41	PMI (Analog Devices)	OPA1111AM	F/E	REF02AJ	Maxim	REF02RM	P/P

Or, Call Customer Service at 1-800-548-6132 (USA Only)

Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility	Competitor and Part Number		Burr-Brown Part Number	Pin Compatibility
REF02CCSA	Maxim	REF02AU	P/P	SMP-10	PMI (Analog Devices)	SHC298AM	F/E
REF02CH	LTC	REF02AM	P/P	SMP-11	PMI (Analog Devices)	SHC298AM	F/E
REF02CJ8	LTC	REF02AG	P/P	SMP-81	PMI (Analog Devices)	SHC5320KH	C/P
REF02CJ	Analog Devices	REF02AM	P/P	SP9345	Sipex	DAC4813	F/E
REF02CJ	Analog Devices	REF02AM	P/P	SP7920	SPT	ADS605	C/P
REF02CJ	Maxim	REF02AM	P/P	SSM-2015	PMI (Analog Devices)	INA103AG	F/E
REF02CN8	LTC	REF02AP	P/P	SSM-2016	PMI (Analog Devices)	INA103AG	F/E
REF02CP	Analog Devices	REF02BP	P/P	SSM-2017	PMI (Analog Devices)	INA103AG	F/E
REF02CP	Maxim	REF02BP	P/P	SSM-2141	Analog Devices	INA105	P/P
REF02CS	Analog Devices	REF02BU	P/P	TDC1012	PMI (Analog Devices)	DAC65JP	F/E
REF02CZ	Analog Devices	REF02AG	P/P	TEA2114	Thomson	MPC100AP	C/P
REF02CZ	Maxim	REF02AG	P/P	TEA6415	Thomson	MPC100AP	C/P
REF02DCSA	Maxim	REF02AU	P/P	THA-0523	DDC	SHC804BM	P/P
REF02DH	LTC	REF02AM	P/P	THC1201	TRW	ADC603JH	F/E
REF02DJ8	LTC	REF02AG	P/P	TL071	Texas Instruments	OPA604	P/E
REF02DJ	Analog Devices	REF02AM	P/P	TL072	Texas Instruments	OPA2604	P/E
REF02DJ	Maxim	REF02AM	P/P	TL072	Texas Instruments	OPA2604	P/E
REF02DN8	LTC	REF02AP	P/P	TL081	Motorola	OPA604	P/P
REF02DP	Analog Devices	REF02AP	P/P	TL082	Texas Instruments	OPA2604	P/P
REF02DP	Maxim	REF02AP	P/P	TL084	Texas Instruments	OPA404KP	P/P
REF02DZ	Analog Devices	REF02AG	P/P	TL087	Texas Instruments	OPA604	F/E
REF02DZ	Maxim	REF02AG	P/P	TL088	Texas Instruments	OPA604	F/E
REF02EH	LTC	REF02CM	P/P	TLO71	Motorola	OPA604	P/P
REF02EH	LTC	REF02CM	P/P	TLO72	Motorola	OPA2107	C/P
REF02EJ8	LTC	REF02BG	P/P	TP4002	Teledyne-Philbrick	DAC71-COB-V	F/E
REF02EJ	Analog Devices	REF02CM	P/P	TP4855	Teledyne-Philbrick	SHC803BM	F/E
REF02EJ	Maxim	REF02CM	P/P	TP4860	Teledyne-Philbrick	SHC804BM	P/P
REF02EN8	LTC	REF02BP	P/P	TPADC85	Teledyne-Philbrick	ADC85H-12	P/P
REF02EZ	Analog Devices	REF02BG	P/P	TPADC87	Teledyne-Philbrick	ADC87H-12	P/P
REF02EZ	Maxim	REF02BG	P/P	VA033	VTC	OPA633KP	P/P
REF02HCSA	Maxim	REF02BU	P/P	VLN-3755	Sprague	OPA2541AM	C/P
REF02HH	LTC	REF02BM	P/P	ZAD354	Zeltex	DAC71-C0B-V	F/E
REF02HJ8	LTC	REF02BG	P/P	ZAD7100	Zeltex	ADC80AG-12	F/E
REF02HJ	Analog Devices	REF02BM	P/P	ZAD7400	Zeltex	ADC76JG	F/E
REF02HJ	Analog Devices	REF02BM	P/P	ZAD8000	Zeltex	DAC70BH-COB-I	F/E
REF02HJ	Maxim	REF02BM	P/P	ZD354	Zeltex	DAC71-C0B-V	F/E
REF02H	LTC	REF02SM	P/P	ZD364	Zeltex	DAC71-C0B-V	F/E
REF02HN8	LTC	REF02BP	P/P	ZD384	Zeltex	DAC71-C0B-V	F/E
REF02HP	Analog Devices	REF02BP	P/P	ZD394	Zeltex	DAC71-C0B-V	F/E
REF02HP	Maxim	REF02BP	P/P	ZDA160	Zeltex	DAC729JH	F/E
REF02HZ	Analog Devices	REF02BG	P/P	VC5601DWP	Unitrode	REG5601	P/P
REF02HZ	Maxim	REF02BG	P/P				
REF02J	Analog Devices	REF02SM	P/P				
REF02J	Maxim	REF02SM	P/P				
REF02		REF02	P/P				
REF05		REF05	P/P				
REF10	Micro Power Systems	REF10KM	P/P				
REF10	PMI (Analog Devices)	REF10KM	P/P				
SHA1A	Analog Devices	SHC85	F/E				
SHA21	Analog Devices	SHC803BM	F/E				
SHA2A-5A	Analog Devices	SHC804BM	F/E				
SHC85	Analog Devices	SHC85	P/P				
SHM-20	Datel	SHC5320KH	P/P				
SHM-4860	Datel	SHC804BM	P/P				
SHM-6	Datel	SHC5320KH	C/P				
SHM-9	Datel	SHC5320KH	C/P				
SHM-HU	Datel	SHC804BM	C/P				
SHM-IC-1	Datel	SHC298AM	C/P				
SHM-LM-2	Datel	SHC298AM	P/P				
SHM360	Datel	SHC600	F/E				
SHM361	Datel	SHC601BH	F/E				
SM5813	NPC	DF1700	P/P				

Appendix C

Tape and Reel Specifications

For users of automatic pick and place equipment, surface mount devices are available in embossed carrier tape and reel.

Burr-Brown uses the highest quality materials available in its Tape and Reel packaging. The documented packaging process meets EIA481-A requirements.

The following illustrates tape sizes, mechanical orientation (polarization), quantity per 13" reel and reel dimensions.

Use Table I to determine tape and reel sizes and quantities.

PACKAGE NUMBER ⁽¹⁾	TAPE WIDTH W (mm)	PART PITCH P (mm)	DEVICES PER 13" Reel
178	24	16	1000
182	12	8	2500
211	16	12	1000
217	24	12	1000
219	24	16	1000
221	24	12	1000
235	16	8	2500
239	24	12	1000
248	24	12	1000
311	12	8	2500

NOTE: (1) Package number for any Burr-Brown product can be found in each product data sheet in the table titled, "Package Information".

TABLE I.

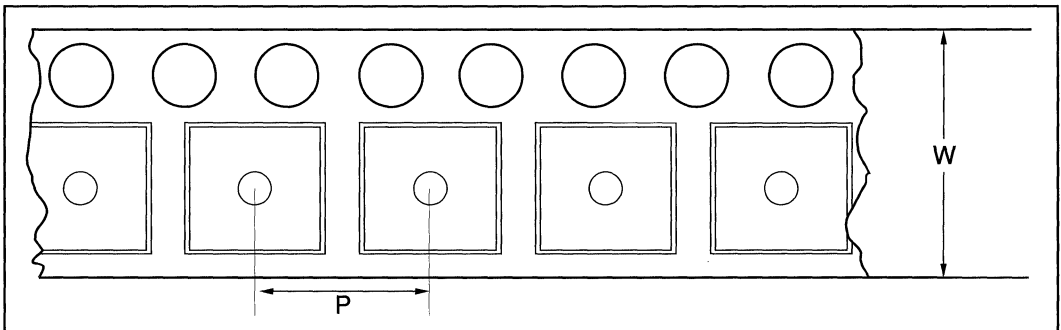


FIGURE 1.

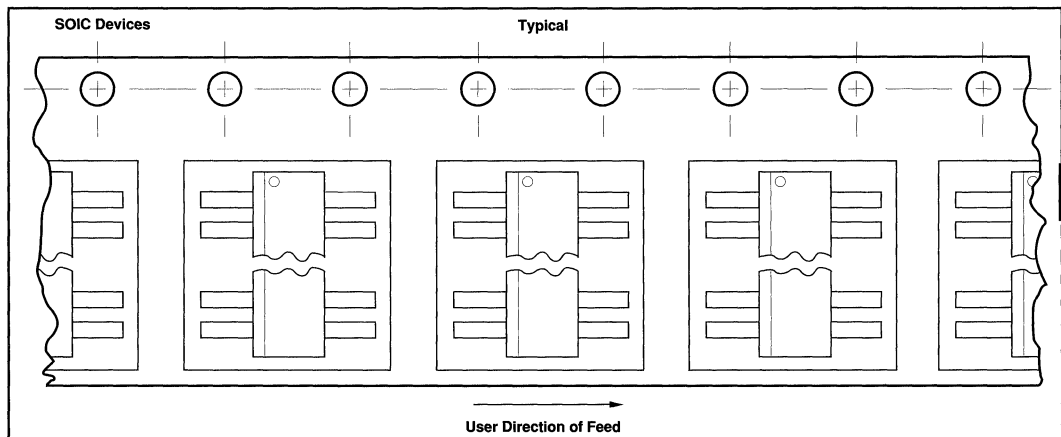


FIGURE 2.



For Immediate Assistance, Contact Your Local Salesperson

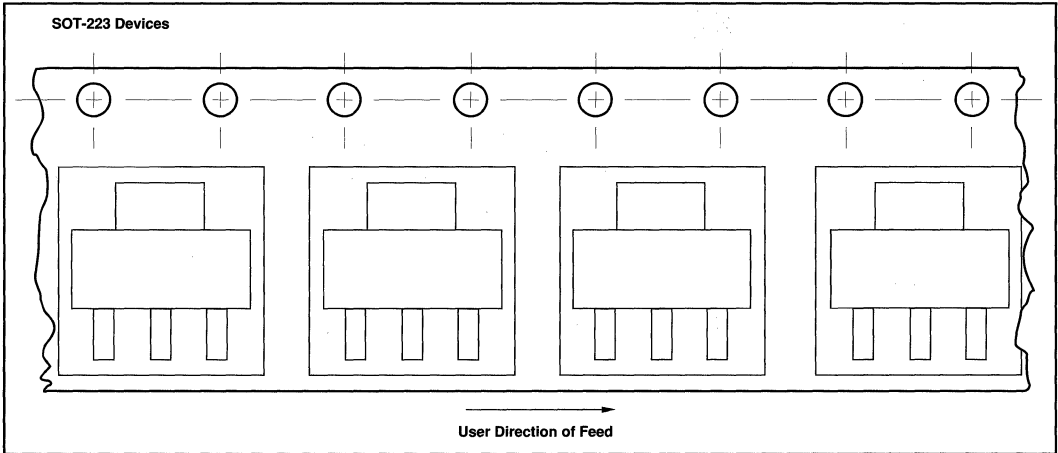


FIGURE 3.

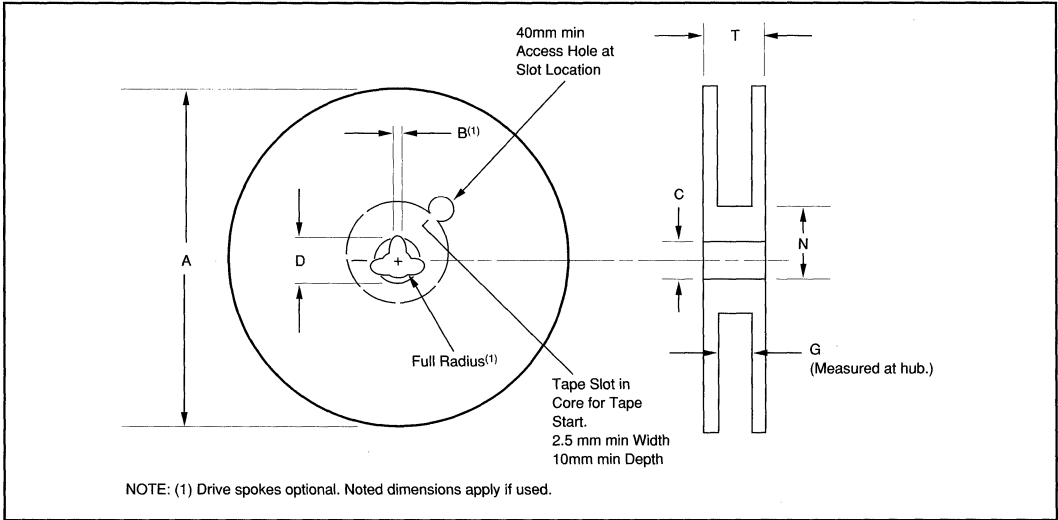


FIGURE 4.

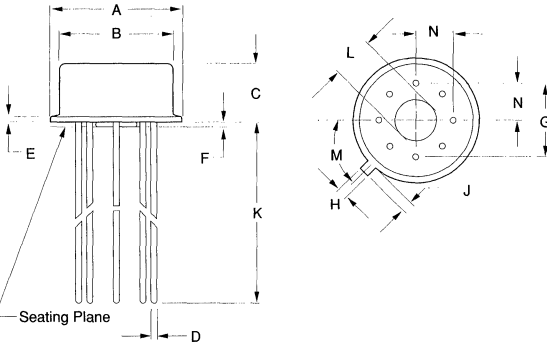
TAPE SIZE	A MAX	B MAX	C	D MIN	N MIN	G	T MAX
12mm	330mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	12.4 + 1.0 (-0.0mm)	18.4mm
16mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	16.4 + 1.0 (-0.08mm)	22.4mm
24mm	360mm	1.5mm	13.0 ±0.20mm	20.2mm	50mm	24.4 + 1.0 (-0.00mm)	30.4mm

TABLE II.

Appendix D

Package Drawings (Mechanicals)

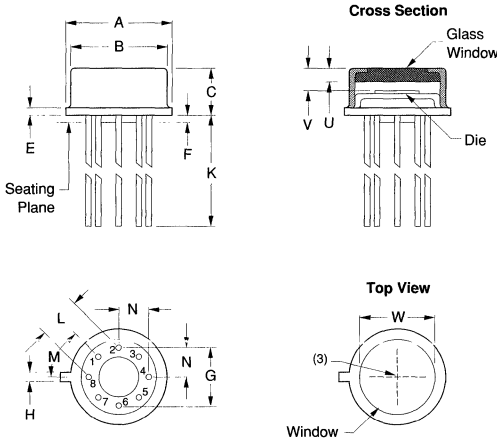
Package Number 001 — Metal TO-99



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

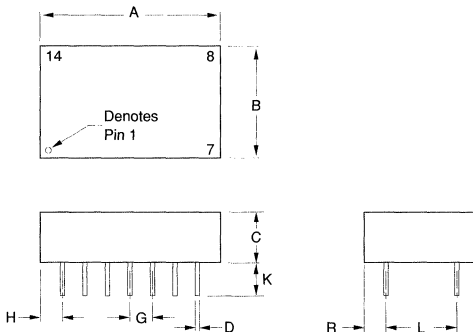
Package Number 001-1 — Metal TO-99



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.149	.165	3.79	4.19
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67
U	.040	.050	1.02	1.27
V	.058	.077	1.47	1.96
W	.246	.254	6.25	6.45

NOTE: (1) Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. (2) Pin numbers shown for reference only. Numbers may not be marked on package. (3) Die may be rotated with respect to indicated axis.

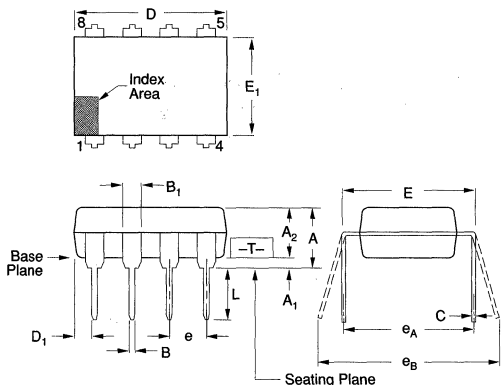
Package Number 003 — 14-Pin



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

NOTE: Leads in true position within 0.10" (.25mm) R @ MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 006 — 8-Pin Plastic Single-Wide DIP

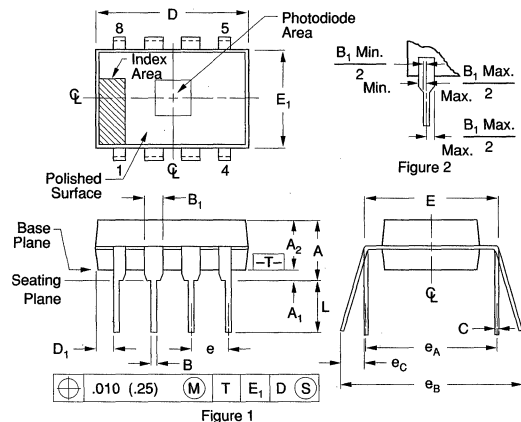


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽¹⁾	—	.210	—	5.33
A1 ⁽⁶⁾	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.348	.430	8.84	10.92
D1	.005	—	0.13	—
E ⁽⁶⁾	.300	.325	7.62	8.26
E1 ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC	—	2.54 BASIC	—
eA ⁽⁶⁾	.300 BASIC	—	7.63 BASIC	—
eB ⁽⁶⁾	—	.430	—	10.92
L ⁽³⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	8	—	8	—

(1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

- (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
- (3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- (4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- (5) E and eA measured with the leads constrained to be perpendicular to plane T.
- (6) eB is measured at the lead tips with the leads unconstrained.
- (7) N is the maximum number of terminal positions.
- (8) Corner leads (1, 4, 5, and 8) may be configured as shown in Figure 2.
- (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

Package Number 006-1 — 8-Pin Clear Plastic Single-Wide DIP

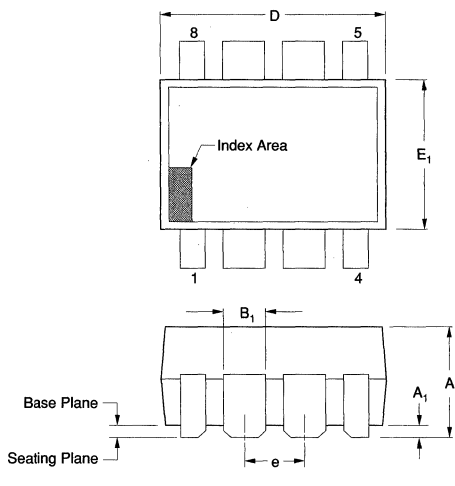


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽¹⁾	—	.210	—	5.33
A1 ⁽⁶⁾	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.348	.430	8.84	10.92
D1	.005	—	0.13	—
E ⁽⁶⁾	.300	.325	7.62	8.26
E1 ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC	—	2.54 BASIC	—
eA ⁽⁶⁾	.300 BASIC	—	7.63 BASIC	—
eB ⁽⁶⁾	—	.430	—	10.92
L ⁽³⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	8	—	8	—

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
 (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.

- (3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- (4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- (5) E and e_A measured with the leads constrained to be perpendicular to plane T.
- (6) e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- (7) N is the maximum number of terminal positions.
- (8) Corner leads (1, 4, 5, and 8) may be configured as shown in Figure 2.
- (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.
- (10) Center of photodiode must be within .01" of center of photodiode area.

Package Number 006-2 — 8-Pin Plastic Single-Wide DIP with Gull Wing Leads



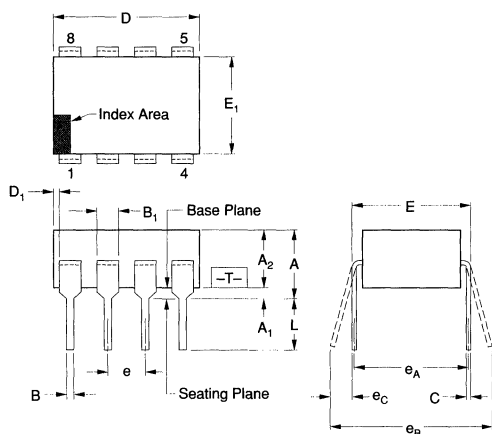
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	.185	—	4.70
A1	.020	—	0.51	—
B1	—	.070	—	1.78
C	.007	.013	0.18	0.33
D	.370	.390	9.40	9.91
E	.290	.310	7.37	7.87
E1	.240	.260	6.10	6.60
E2	.370	.390	9.40	9.91
e	.090	.110	2.29	2.79
eA	.015	.035	0.38	0.89
eB	.015	.025	0.38	0.64
N	8	—	8	—

- NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, inch dimensions control.
- (2) Dimensioning and tolerancing per ANSI Y14.5-1982.
- (3) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- (4) N is the maximum number of terminal positions.
- (5) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.



Or, Call Customer Service at 1-800-548-6132 (USA Only)

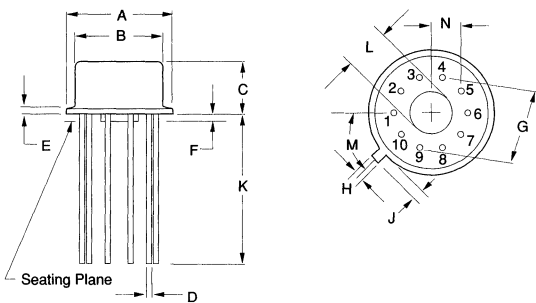
Package Number 006-3 — 8-Pin Plastic Single-Wide DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽²⁾	—	.210	—	5.33
A1 ⁽³⁾	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.025	0.36	0.635
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.348	.430	8.84	10.92
D1	.005	—	0.13	—
E ⁽⁵⁾	.300	.325	7.62	8.26
E1 ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC	—	2.54 BASIC	—
eA ⁽⁶⁾	.300 BASIC	—	7.63 BASIC	—
eB ⁽⁶⁾	—	.430	—	10.92
L ⁽³⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	8	—	8	—

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
 (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 (4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (5) E and eA measured with the leads constrained to be perpendicular to plane T.
 (6) eB is measured at the lead tips with the leads unconstrained.
 (7) N is the maximum number of terminal positions.
 (8) Corner leads (1, 4, 5, and 8) may be configured as shown in Figure 2.
 (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

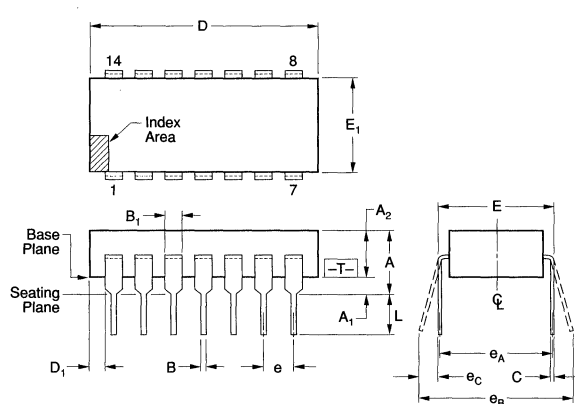
Package Number 007 — TO-100 Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC	—	5.84 BASIC	—
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC	—	36° BASIC	—
N	.110	.120	2.79	3.05

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

Package Number 010 — 14-Pin Plastic Single Wide DIP



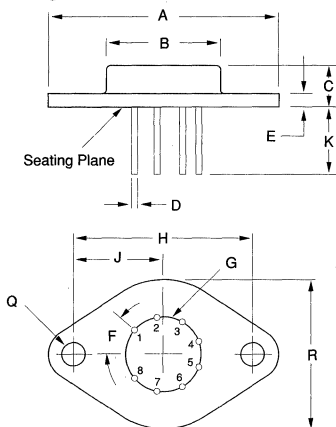
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽²⁾	—	.210	—	5.33
A1 ⁽³⁾	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.725	.795	18.42	20.19
D1	.005	—	0.13	—
E ⁽⁵⁾	.300	.325	7.62	8.26
E1 ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC	—	2.54 BASIC	—
eA ⁽⁶⁾	.300 BASIC	—	7.63 BASIC	—
eB ⁽⁶⁾	—	.430	—	10.92
L ⁽³⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	14	—	14	—

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
 (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.

(3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 (4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (5) E and eA measured with the leads constrained to be perpendicular to plane T.
 (6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
 (7) N is the maximum number of terminal positions.
 (8) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

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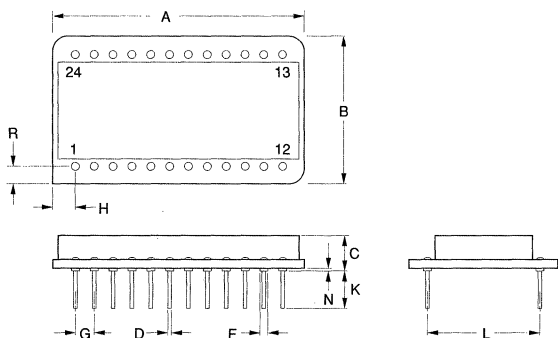
Package Number 030 — 8-Pin Metal TO-3



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.260	.300	6.60	7.62
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.70 BASIC	
H	1.182	1.192	30.02	30.28
J	.591	.596	15.01	15.14
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

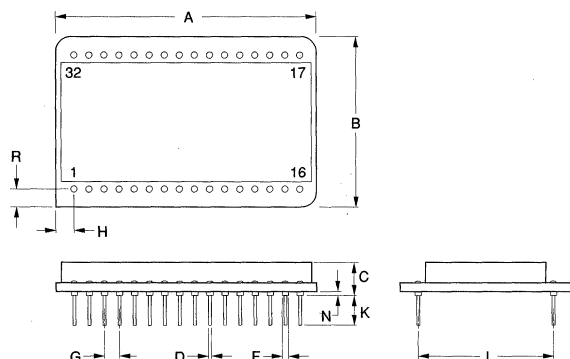
Package Number 075 — 24-Pin



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 077 — 32-Pin Omnipak

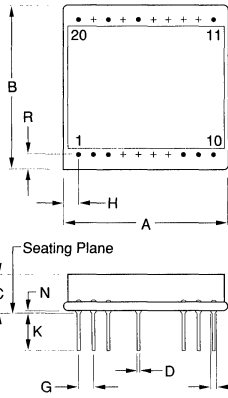


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.160	.180	4.06	4.57
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

NOTES: (1) Leads in true position within .010" (0.25mm) R at MMC at seating plane. (2) Pin numbers shown for reference only. Numbers may not be marked on package.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

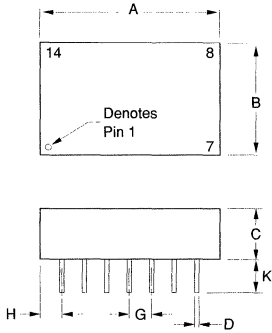
Package Number 102 — 20-Lead ISO Omni



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

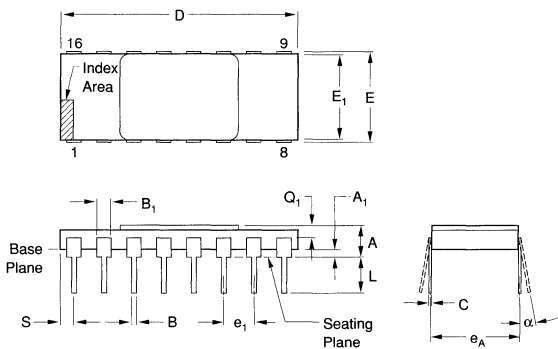
Package Number 105 — 14-Pin DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 109 — 16-Lead, Ceramic Side-Braze DIP, .300 Row Spacing Hermetic DIP

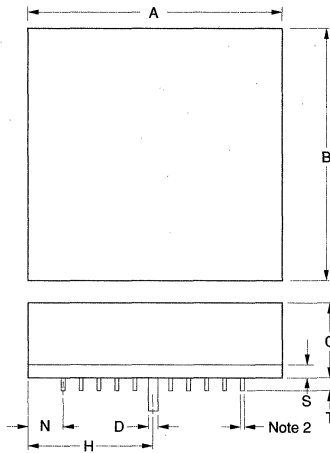


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.105	.175	2.68	4.45
A ₁	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B ₁	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.770	.830	19.56	21.08
E	.290	.325	7.37	8.26
E ₁ ⁽⁶⁾	.280	.310	7.11	7.87
e ₁ ⁽²⁾	.100 TYPICAL		2.54 TYPICAL	
e _A ⁽²⁾	.300 TYPICAL		7.62 TYPICAL	
L	.125	.175	3.18	4.45
N ⁽⁴⁾	16		16	
Q ₁	.010	—	0.25	—
s	.020	.065	0.51	1.65
α ⁽³⁾	0°	15°	0°	15°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5-1973. (2) Leads within .13mm (.005in) radius of true position (TP) with maximum material condition. (3) α applies to spread leads prior to installation. (4) N is the number of terminal positions. (5) Outlines on which the seating plane is coincident with the base plane (A₁ = 0), terminals lead standoffs are not required, and B₁ may equal B along any part of the lead above the seating/base plane. (6) E₁ does not include particles of packing materials. (7) Controlling dimension: Inch.

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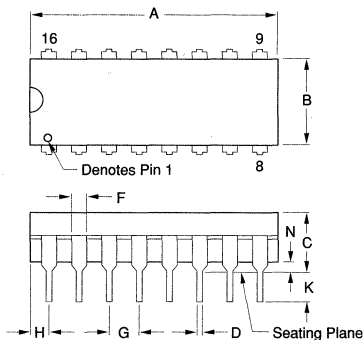
Package Number 124 — EMI Shield



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.320	1.380	33.53	35.05
B	1.320	1.380	33.53	35.05
C	.350	.450	8.89	11.43
D	.040	.060	1.02	1.52
H	.600	.700	15.24	17.78
J	.015	.025	0.38	0.64
L	1.180	1.280	29.97	32.51
N	.150	.250	3.81	6.35
P	.150	.250	3.81	6.35
R	.015	.055	0.38	1.40
T	.130	.230	3.30	5.84
S	.060	.080	1.52	2.03

NOTE: (1) Enclosed module lead length minus .050" to .100" (1.27mm to 2.54mm).
 (2) Pin diameter determined by enclosed module.

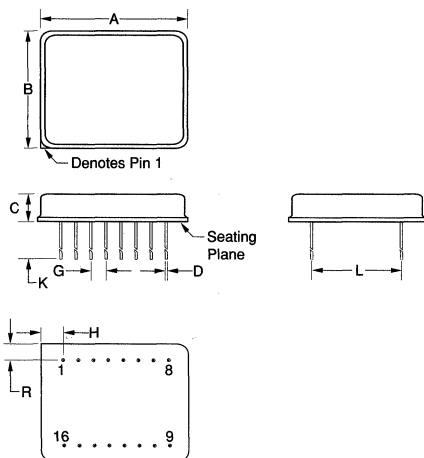
Package Number 129 — 16-Pin Ceramic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.885	19.30	22.48
B	.280	.295	7.11	7.50
C	—	.200	—	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC	—	2.54 BASIC	—
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	—	2.54	—
L	.300 BASIC	—	7.62 BASIC	—
M	—	15°	—	15°
N	.020	.050	0.51	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on the package.

Package Number 142 — 16-Pin

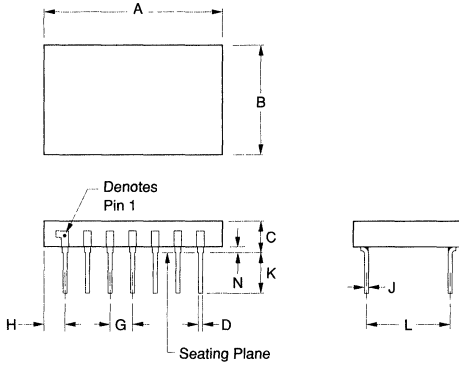


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.963	.980	24.46	24.89
B	.760	.805	19.30	20.45
C	.175	.190	4.45	4.83
D	.014	.022	0.36	0.56
G	.100 BASIC	—	2.54 BASIC	—
H	.135	.155	3.43	3.94
K	.230	.270	5.84	6.86
L	.600 BASIC	—	15.24 BASIC	—
R	.095	.115	2.41	2.92

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

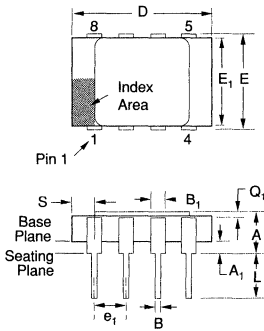
Package Number 148—14-Pin



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	0.41	0.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	0.23	0.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	0.38	0.89

NOTE: Leads in true position within 0.10" (.25mm) R at MMC at seating plane.

Package Number 157 — 8-Pin Ceramic Side-Brace DIP

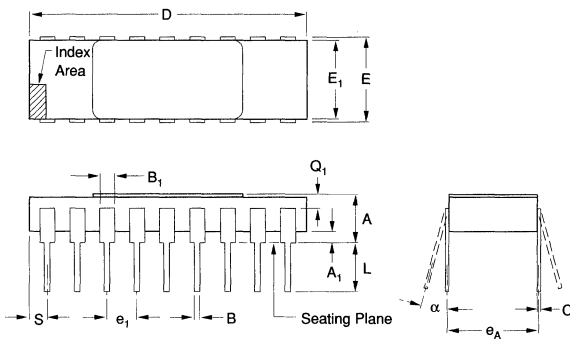


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.105	.175	2.67	4.45
A ₁	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B ₁	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.380	.550	9.65	13.97
E	.290	.325	7.37	8.26
E ₁ ⁽¹⁾	.280	.310	7.11	7.87
e ₁ ⁽²⁾	.100 TYP		2.54 TYP	
e _A ⁽³⁾	.300 TYP		7.62 TYP	
L	.125	.175	3.18	4.45
N ⁽⁴⁾	8		8	
Q ₁	.010	—	2.54	—
S	.030	.120	0.76	3.05
α ⁽⁵⁾	0°	15°	0°	15°

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5-1973.
2. Leads within 0.13mm (0.005) radius of true position (TP) with maximum material condition.
3. α applies to spread leads prior to installation.
4. N is the number of terminal positions.
5. Outlines on which the seating plane is coincident with the base plane (A₁ = 0). Terminals lead standoffs are not required, and B₁ may equal B along any part of the lead above the seating base plane.
6. E₁ does not include particles of package materials.
7. Controlling dimension: inch.

Package Number 158 — 18-Lead, Ceramic Side-Brace DIP, .300 Row Spacing



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.105	.175	2.68	4.45
A ₁	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B ₁	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.880	.930	22.35	23.62
E	.290	.325	7.37	8.26
E ₁	.280	.310	7.11	7.87
e ₁	.100 TYPICAL		2.54 TYPICAL	
e _A	.300 TYPICAL		7.62 TYPICAL	
L	.125	.175	3.18	4.45
N	18		18	
Q ₁	.010	—	0.25	—
S	.030	.065	0.76	1.65
α	0°	15°	0°	15°

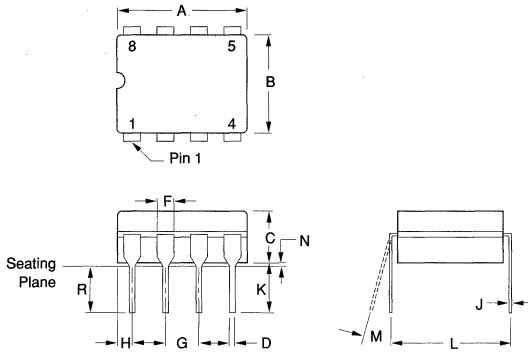
NOTE: (1) Dimensioning and tolerancing per ANSI Y14.5-1973.
 (2) Leads within .13mm (.005in) radius of true position (TP) with maximum material condition.
 (3) α applies to spread leads prior to installation.
 (4) N is the number of terminal positions.
 (5) Outlines on which the seating plane is coincident with the base plane (A₁ = 0), terminals lead standoffs are not required, and B₁ may equal B along any part of the lead above the seating/base plane.
 (6) E₁ does not include particles of packing material.
 (7) Controlling dimension: Inch.

MECHANICALS

D

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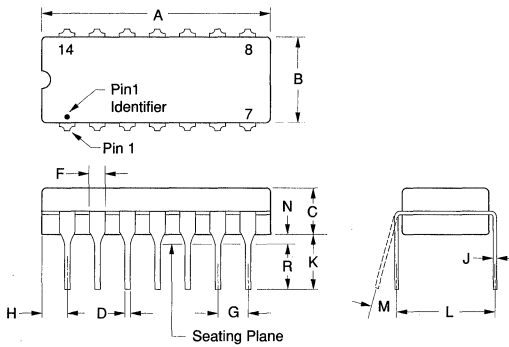
Package Number 161 — 8-Pin Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.280	.295	7.11	7.50
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.098	—	2.49
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on the package.

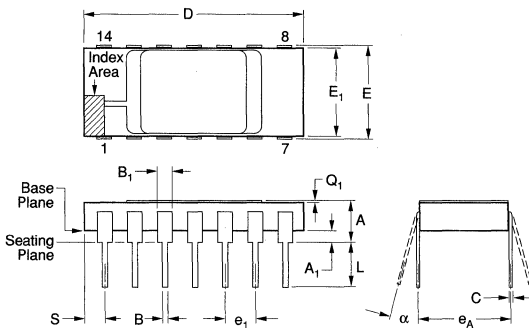
Package Number 163 — 14-Pin Side-Brace Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.767	19.13	19.48
B	.280	.295	7.12	7.50
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.085	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

NOTES: (1) Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. (2) Pin numbers shown for reference only. May not be marked on the package.

Package Number 169 — 14-Pin Ceramic Side Ledged DIP, .300 Row Spacing

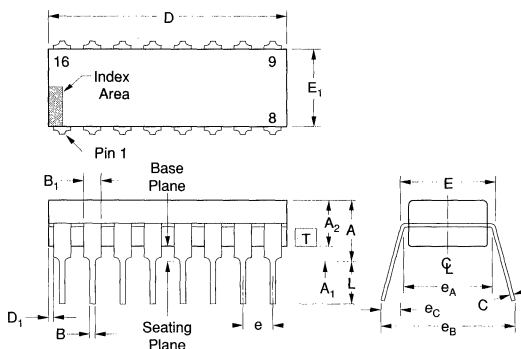


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.105	.175	2.68	4.45
A ₁	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B ₁	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.690	.770	17.53	19.56
E	.290	.325	7.37	8.26
E ₁ ⁽⁶⁾	.280	.310	7.11	7.87
e ₁ ⁽²⁾	.100 BASIC		2.54 BASIC	
ea ⁽²⁾	.300 BASIC		7.62 BASIC	
L	.125	.175	3.18	4.45
N ⁽⁴⁾	14		14	
Q ₁	.010	—	0.25	—
S	.030	.095	0.76	2.41
α ⁽³⁾	0°	15°	0°	15°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5-1973. (2) Leads within 0.13mm (.005in) radius of true position (TP) with maximum material condition. (3) α applies to spread leads prior to installation. (4) N is the number of terminal positions. (5) Outlines on which the seating plane is coincident with the plane (A₁ = 0), terminals lead standoffs are not required, and B₁ may equal B along any part of the lead above the seating/base plane. (6) E₁ does not include particles of packing materials. (7) Controlling dimension: Inch.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

Package Number 180 — 16-Pin Plastic, Single-Wide DIP



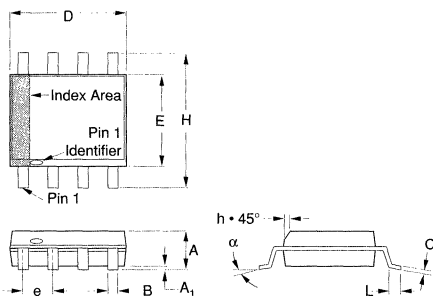
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽¹⁾	—	.210	—	5.33
A ₁ ⁽¹⁾	.015	—	0.38	—
A ₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B ₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽²⁾	.745	.840	18.92	21.34
D ₁	.005	—	0.13	—
E ⁽³⁾	.300	.325	7.62	8.26
E ₁ ⁽²⁾	.240	.280	6.10	7.11
e	.100 BASIC	2.54 BASIC	—	—
e _A ⁽³⁾	.300 BASIC	7.62 BASIC	—	—
e _B ⁽⁴⁾	—	.430	—	10.92

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
L ⁽¹⁾	.115	.160	2.92	4.06
N ⁽⁵⁾	16	16	—	—

- (1) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 (2) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (3) E and e_A are measured with the leads constrained to be perpendicular to plane T.
 (4) e_B and e_C are measured at the lead tips with the leads unconstrained. e_B must be zero or greater.
 (5) N is the maximum number of terminal positions.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

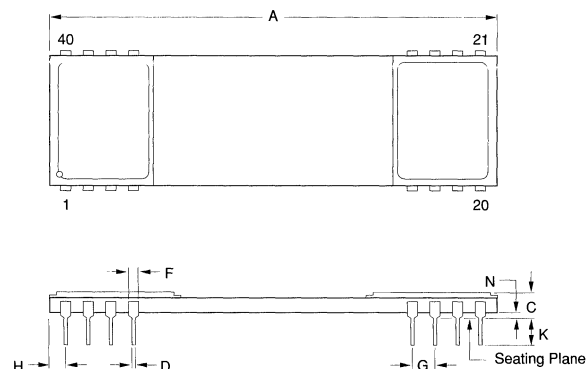
Package Number 182 — 8-Pin SO-8 Surface Mount



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.054	.068	1.37	1.73
A ₁	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC	1.27 BASIC	—	—
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	B	—	B	—
α	0°	8°	0°	8°

- NOTES:
 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.).
 3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
 4. "L" is the length of the terminal for soldering to a substrate.
 5. "N" is the number of terminal positions.

Package Number 206 — 40-Pin Double-Wide Hermetic DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.980	2.020	50.29	51.31
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC	2.54 BASIC	—	—
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC	15.24 BASIC	—	—
M	—	10°	—	10°
N	.025	.060	0.64	1.52

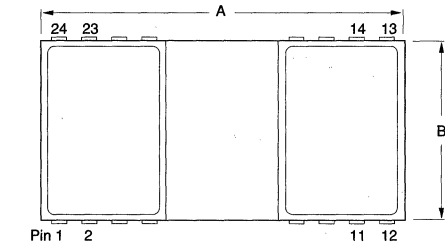
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

MECHANICALS

D

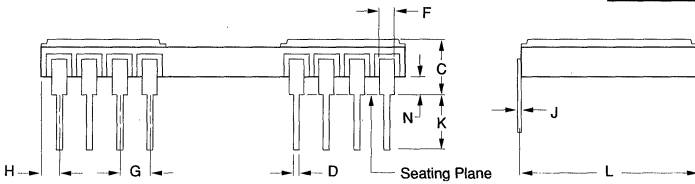
For Immediate Assistance, Contact Your Local Salesperson

Package Number 208 — 24-Pin Double-Wide Hermetic DIP

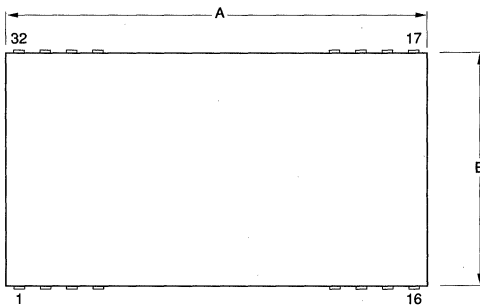


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.190	1.210	30.23	30.73
B	.580	.600	14.73	15.24
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

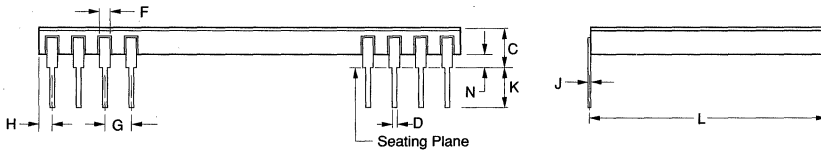


Package Number 210 — 16-Lead Ceramic DIP

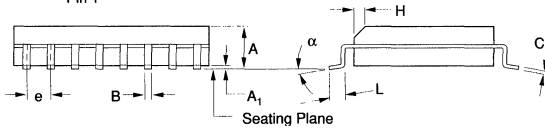
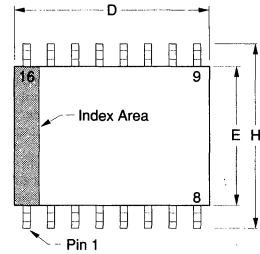


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.590	1.630	40.39	41.40
B	.910	.930	23.11	23.62
C	.310	.370	7.87	9.40
D	.016	.020	0.41	0.51
F	.040 TYPICAL		1.02 TYPICAL	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.900	.920	22.86	23.37
N	.040	.060	1.02	1.52

NOTE: (1) Leads in true position within .010" (0.25mm) R at MMC at seating plane. (2) Pin numbers shown for reference only. Numbers may not be marked on package.



Package Number 211 — 16-Lead SOIC

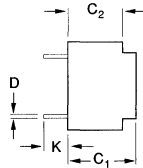
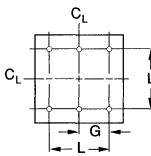
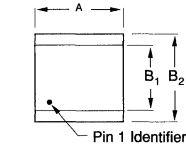


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A ₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D ⁽¹⁾	.398	.413	10.11	10.49
E ⁽²⁾	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h ⁽³⁾	.010	.029	0.25	0.74
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	16		16	
α	0°	8°	0°	8°

- (1) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006in.).
- (2) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- (3) L is the length of terminal for soldering to a substrate.
- (4) N is the number of terminal positions.

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

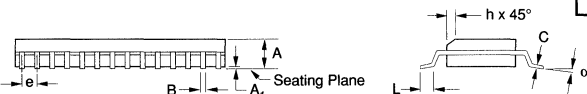
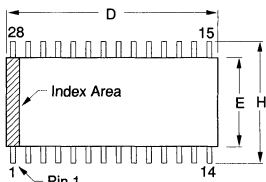
Package Number 216 — 6-Pin Distributed Power Transformer



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.54	0.64	13.72	16.26
B ₁	0.39	0.49	9.91	12.45
B ₂	0.54	0.64	13.72	16.26
C ₁	0.39	0.52	9.91	13.21
C ₂	0.29	0.44	7.37	11.18
D	.020	.030	0.50	0.76
G	.177	.217	4.50	5.12
K	0.11	0.21	2.79	5.33
L	.375	.425	9.53	10.80

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Package Number 217 — 28-Lead SOIC

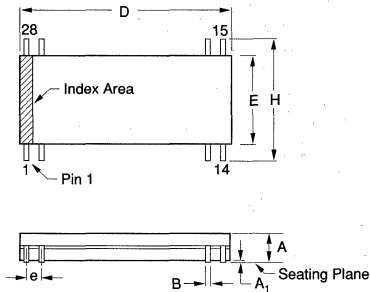


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A ₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D ⁽¹⁾	.697	.712	17.70	18.08
E ⁽²⁾	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h ⁽³⁾	.010	.029	0.25	0.74
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	28		28	
α	0°	8°	0°	8°

- NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982
- (2) "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006 in.).
- (3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- (4) "L" is the length of terminal for soldering to a substrate.
- (5) "N" is the number of terminal positions.
- (6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

For Immediate Assistance, Contact Your Local Salesperson

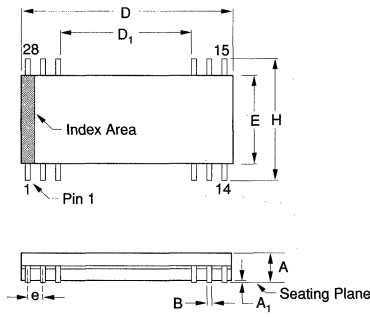
Package Number 217-1 — 28-Lead SOIC, ISO Package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A ₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D ⁽²⁾	.697	.712	17.70	18.08
E ⁽²⁾	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h ⁽³⁾	.010	.029	0.25	0.74
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	8		8	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (2) "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006 in).
 (3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
 (4) "L" is the length of terminal for soldering to a substrate.
 (5) "N" is the number of terminal positions.
 (6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

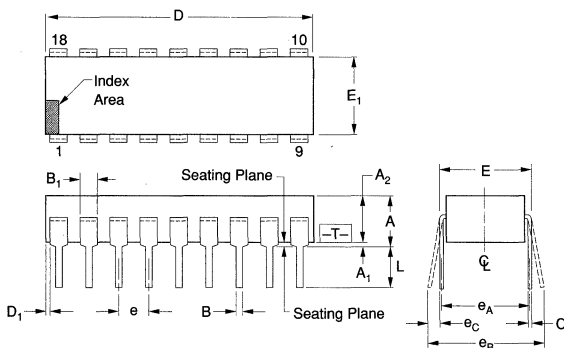
Package Number 217-2 — 28-Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A ₁	.004	.011	0.10	0.28
B	.014	.019	0.36	0.48
C	.0095	.012	0.24	0.30
D ⁽²⁾	.697	.712	17.70	18.08
D ₁	.426	.441	10.82	11.20
E ⁽²⁾	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.394	.419	10.01	10.64
h ⁽³⁾	.010	.029	0.25	0.74
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	12		12	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (2) "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006 in).
 (3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
 (4) "L" is the length of terminal for soldering to a substrate.
 (5) "N" is the number of terminal positions.
 (6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.

Package Number 218 — 18-Pin Plastic Single-Wide DIP



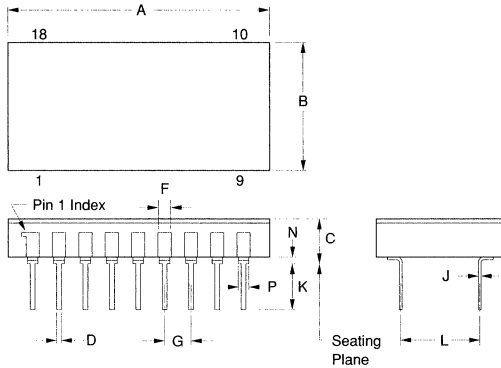
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽³⁾	—	.210	—	5.33
A ₁ ⁽³⁾	.015	—	0.38	—
A ₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B ₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.845	.925	21.46	23.50
D ₁	.005	—	0.13	—
E ⁽⁵⁾	.300	.325	7.62	8.26
E ₁ ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e _A ⁽⁶⁾	.300 BASIC		7.63 BASIC	
e _B ⁽⁶⁾	—	.430	—	10.92
L ⁽⁸⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	18		18	

JEDEC seating plane gauge GS-3.
 (4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (5) E and e_A measured with the leads constrained to be perpendicular to plane T.
 (6) e_A and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
 (7) N is the maximum number of terminal positions.
 (8) Corner leads (1, 9, 10, and 18) may be configured as shown in Figure 2.
 (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
 (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (3) Dimensions A, A₁, and L are measured with the package seated in

Or, Call Customer Service at 1-800-548-6132 (USA Only)

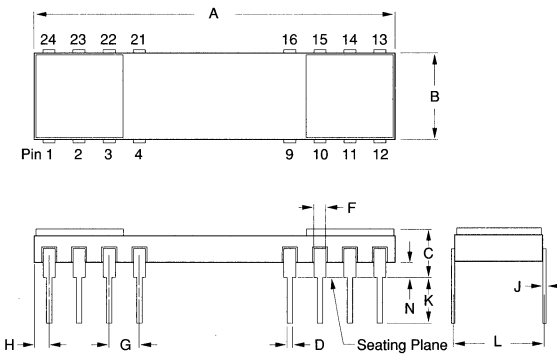
Package Number 220 — 18-Pin Bottom-Braze DIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.982	1.002	24.94	25.45
B	.480	.500	12.19	12.70
C	.148	.197	3.76	5.00
D	.016	.020	0.41	0.51
F	.050 TYPICAL		1.27 TYPICAL	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.30
K	.150	.200	3.81	5.08
L	.290	.310	7.37	7.87
N	.015	.035	0.38	0.89
P	.040 TYPICAL		1.02 TYPICAL	

NOTE: Leads in true position within 0.10" (.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

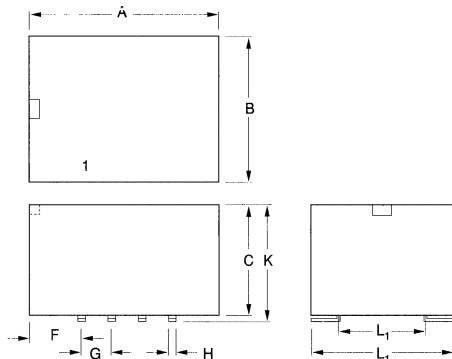
Package Number 225 — 24-Pin Single-Wide Hermetic Dip



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.190	1.210	30.23	30.73
B	.280	.300	7.11	7.62
C	.140	.185	3.56	4.70
D	.016	.020	0.41	0.51
F	.030	.050	0.76	1.27
G	.100 BASIC		2.54 BASIC	
H	.035	.065	0.89	1.65
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.300 BASIC		7.62 BASIC	
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 226 — 8-Pin Plastic DIP

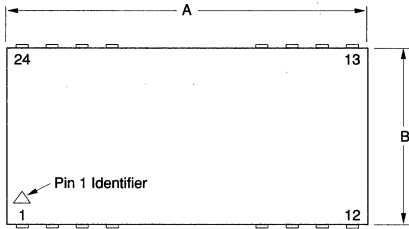


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC		2.54 BASIC	
H	.025 SQ		.635 SQ	
K	.370	.390	9.40	9.91
L1	.280	.300	7.11	7.62
L2	.465	.485	11.81	12.32

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

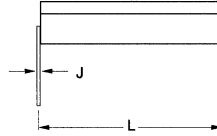
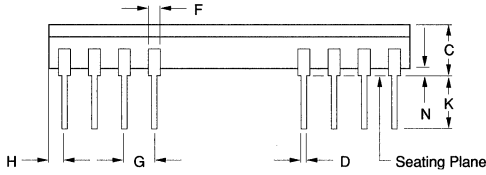
For Immediate Assistance, Contact Your Local Salesperson

Package Number 231 — 24-Pin Ceramic DIP

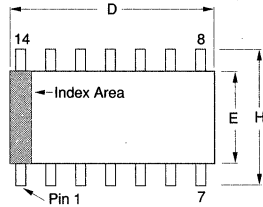


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.180	1.265	29.97	32.13
B	.570	.610	14.48	15.49
C	.310	.375	7.87	9.52
D	.016	.020	0.41	0.51
F	.040 TYP		1.02 TYP	
G	.100 BASIC		2.54 BASIC	
H	.044	.056	1.12	1.42
J	.009	.012	0.23	0.30
K	.125	.180	3.18	4.57
L	.580	.620	14.73	15.75
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.



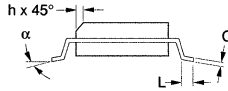
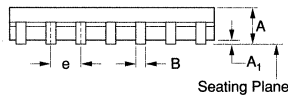
Package Number 235 — 14-Lead SOIC



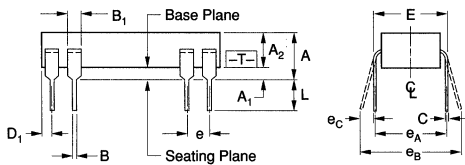
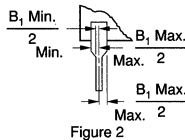
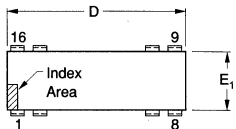
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.054	.068	1.37	1.73
A ₁	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D ⁽²⁾	.337	.344	8.56	8.74
E ⁽²⁾	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h ⁽³⁾	.010	.019	0.25	0.48
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	14		14	
α	0°	8°	0°	8°

NOTES:

- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006 in.)
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the shaded area.
- L is the length of the terminal for soldering to a substrate.
- N is the number of terminal positions.
- Lead to lead coplanarity shall be less than 0.004 inches from the seating plane.



Package Number 238 — 16-Pin Single Wide DIP, ISO Package



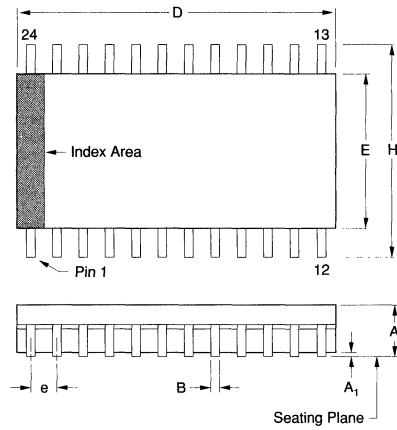
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽²⁾	—	.210	—	5.33
A ₁ ⁽³⁾	.015	—	0.38	—
A ₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B ₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	.745	.840	18.92	21.34
D ₁	.005	—	0.13	—
E ⁽⁵⁾	.300	.325	7.62	8.26
E ₁ ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e _A ⁽⁶⁾	.300 BASIC		7.63 BASIC	
e _B ⁽⁶⁾	.430		10.92	
L ⁽⁷⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	8		8	

- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- E and e_A measured with the leads constrained to be perpendicular to plane T.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- N is the maximum number of terminal positions.
- Corner leads (1, 8, 9, and 16) may be configured as shown in Figure 2.
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

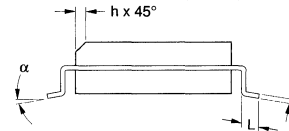


Package Number 239 — 24-Lead SOIC

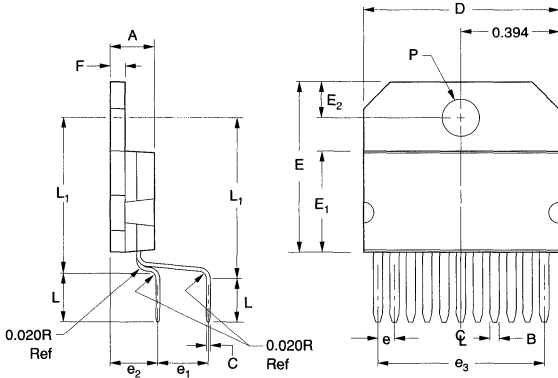


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.36	2.64
A ₁	.0040	.0118	0.10	0.30
B	.014	.019	0.36	0.48
C	.009	.012	0.23	0.30
D ⁽²⁾	.5985	.6140	15.20	15.60
E ⁽²⁾	.292	.299	7.42	7.59
e	.050 BASIC		1.27 BASIC	
H	.395	.418	10.03	10.62
h ⁽³⁾	.010	.029	0.25	0.74
L ⁽⁴⁾	.016	.050	0.41	1.27
N ⁽⁵⁾	24		24	
α	0°	8°	0°	8°

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (2) D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006in).
 (3) The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
 (4) L is the length of terminal for soldering to a substrate.
 (5) N is the number of terminal positions.
 (6) Lead to lead coplanarity shall be less than .004 inches from the seating plane.



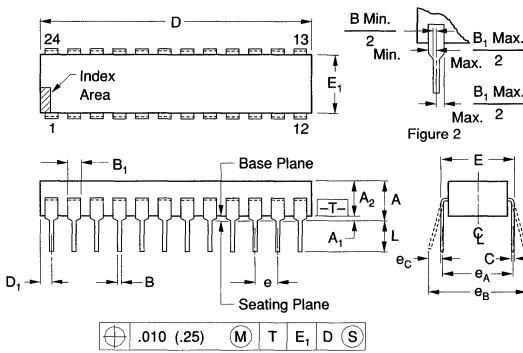
Package Number 242 — 11-Pin Plastic SIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.172	.182	4.37	4.62
B	.035	.041	0.89	1.04
C	.014	.024	0.36	0.61
D	.778	.798	19.76	20.27
E	.684	.694	17.37	17.63
E ₁	.416	.426	10.57	10.82
E ₂	.110 BASIC		2.79 BASIC	
e	.067 BASIC		1.70 BASIC	
e ₁	.200 BASIC		5.08 BASIC	
e ₂	.169 BASIC		4.29 BASIC	
e ₃	.670 BASIC		17.02 BASIC	
F	.057	.063	1.45	1.60
L	.150	.176	3.81	4.47
L _r	.690	.710	17.53	18.03
N ⁽³⁾	11		11	
P	.148	.152	3.76	3.86
R ₁	.065	.080	1.65	2.03

NOTES: (1) Dimensioning and tolerancing per ANSI Y14.5-1982.
 (2) Controlling Dimension: Inch.
 (3) N is the maximum quantity of lead positions.

Package Number 243 — 24-Pin Plastic Single Wide DIP



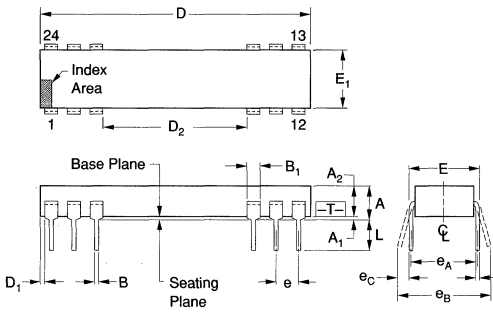
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽³⁾	—	.210	—	5.33
A ₁ ⁽³⁾	.015	—	0.38	—
A ₂	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B ₁	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	1.125	1.275	28.58	32.39
D ₁	.005	—	0.13	—
E ⁽⁵⁾	.300	.325	7.62	8.26
E ₁ ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e _A ⁽⁶⁾	.300 BASIC		7.63 BASIC	
e _B ⁽⁶⁾	.430		10.92	
L ⁽³⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	24		24	

(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (3) Dimensions A, A₁, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 (4) D and E, dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (5) E and e_A measured with the leads constrained to be perpendicular to plane T.
 (6) e_A and e_B are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
 (7) N is the maximum number of terminal positions.
 (8) Corner leads (1, 12, 13, and 24) may be configured as shown in Figure 2.
 (9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

⊕ .010 (.25) (M) T E₁ D (S)

For Immediate Assistance, Contact Your Local Salesperson

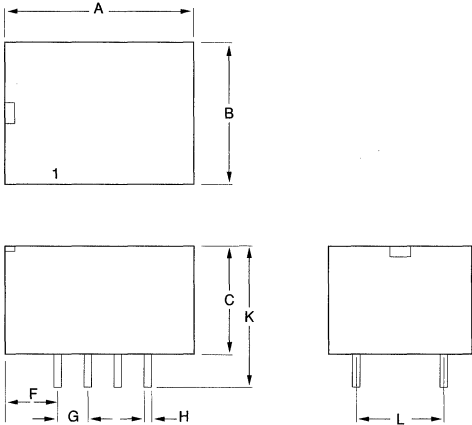
Package Number 243-1—24-Lead Single-Wide PDIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽⁸⁾	—	.210	—	5.33
A1 ⁽⁸⁾	.015	—	0.38	—
A2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D ⁽⁴⁾	1.125	1.275	28.58	32.39
D1	.005	—	0.13	—
D2	.630	.655	16.00	16.64
E ⁽⁸⁾	.300	.325	7.62	8.26
E1 ⁽⁴⁾	.240	.280	6.10	7.11
e	.100 BASIC	—	2.54 BASIC	—
eA ⁽⁸⁾	.300 BASIC	—	7.62 BASIC	—
eB ⁽⁸⁾	—	.430	—	10.92
L ⁽⁸⁾	.115	.160	2.92	4.06
N ⁽⁷⁾	12	—	12	—

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
 (2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
 (3) Dimensions A, A1, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
 (4) D and E1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 (5) E and eA measured with the leads constrained to be perpendicular to plane T.
 (6) eA and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.
 (7) N is the maximum number of terminal positions.
 (8) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

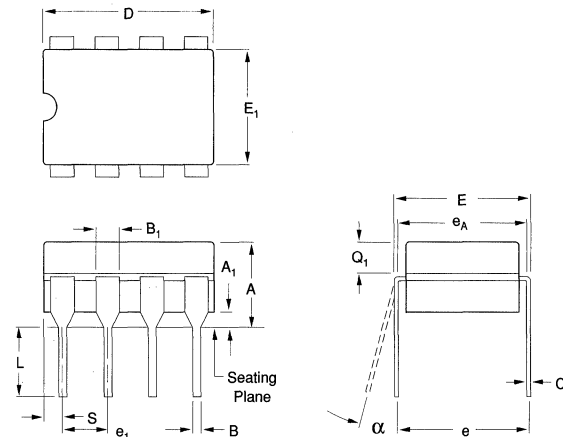
Package Number 250 — 8-Pin Plastic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.620	.640	15.78	16.26
B	.465	.485	11.81	12.32
C	.350	.370	8.89	9.40
F	.165	.185	4.19	4.70
G	.100 BASIC	—	2.54 BASIC	—
H	.025 SQ.	—	.635 SQ.	—
K	.470	.490	11.94	12.45
L	.280	.300	7.11	7.62

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

Package Number 254 — 8-Pin SSI Ceramic DIP

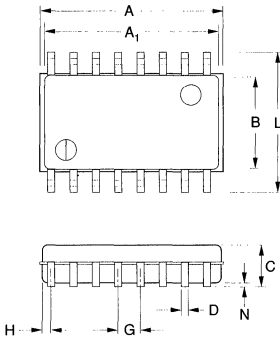


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.214	4.07	5.44
A1	.009	.060	0.23	1.52
B	.015	.021	.38	.54
B1	.045	.060	1.14	1.52
C	.008	.012	0.20	0.30
D	.365	.395	9.27	10.03
E	.290	.320	7.37	8.13
E1	.245	.255	6.22	6.48
e1	.100 BASIC	—	2.54 BASIC	—
eA	.268	.288	6.81	7.31
L	.125	.175	3.18	4.45
Q1	0°	15°	0°	15°
S	.180	.220	4.57	5.59
S	—	.098	—	2.49
e	.290	.320	7.37	8.13

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Or, Call Customer Service at 1-800-548-6132 (USA Only)

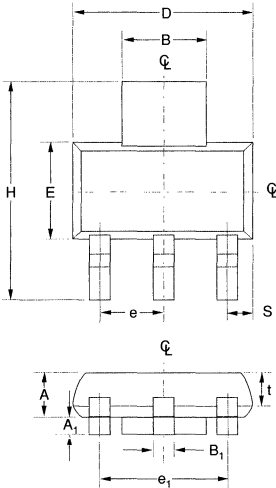
Package Number 258 — 16-Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.400	.415	10.16	10.54
A ₁	.395	.400	10.03	10.16
B	.205	.214	5.21	5.44
C	—	.090	—	2.29
D	.012	.020	0.30	0.51
G	.044	.055	1.12	1.40
H	.020	.031	0.51	0.79
J	.005	.008	0.13	0.20
L	.300	.324	7.62	8.23
N	.004	.008	0.10	0.20
Z	.012	.036	0.30	0.91

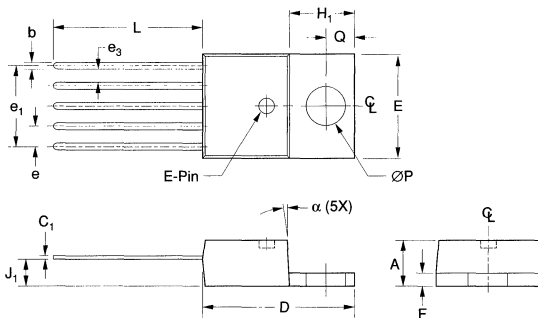
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Package Number 311 — 4LD SOT



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.060	.067	1.50	1.70
A ₁	.0008	.004	0.02	0.10
B	.116	.124	2.95	3.15
B ₁	.026	.033	0.66	0.73
C	.010	.014	0.25	0.35
D	.248	.264	6.30	6.70
E	.130	.146	3.30	3.70
E ₁	.012 MIN		0.30 MIN	
e	.0905 NOM		2.30 NOM	
e ₁	.181 NOM		4.60 NOM	
H	.264	.287	6.70	7.30
S	.033	.041	0.85	1.05
t	.043	.051	1.10	1.30
θ	10° MAX		10° MAX	
θ ₁	10°	16°	10°	16°
θ ₂	10°	16°	10°	16°

Package Number 315 — TO-220, 5-Lead



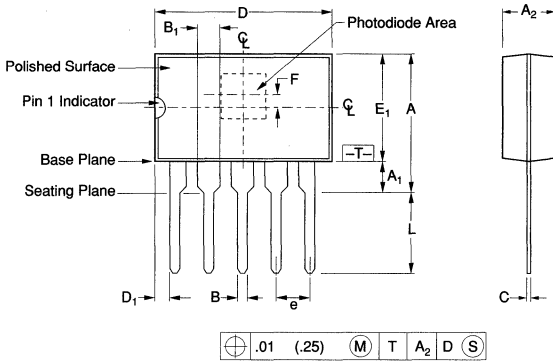
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.160	.190	4.06	4.83
b	.025	.040	0.63	1.02
C ₁	.014	.022	0.36	0.56
D	.560	.590	14.22	14.99
E	.385	.415	9.78	10.54
e	.062	.072	1.57	1.83
e ₁	.263	.273	6.68	6.93
e ₃	.030	.040	0.76	1.02
F	.045	.055	1.14	1.40
H ₁	.234	.258	5.94	6.55
J ₁	.090	.115	2.29	2.92
∅P	.146	.156	3.71	3.96
Q	.103	.113	2.62	2.87
L	.540	.560	13.72	14.22
α	3°	7°	3°	7°

MECHANICALS

D

For Immediate Assistance, Contact Your Local Salesperson

Package Number 321 — 5-Pin Clear Plastic SIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A ⁽³⁾	—	.360	—	9.14
A ₁ ⁽³⁾	.070	—	1.78	—
A ₂	.115	.195	2.92	4.95
B	.014	.022	.036	.056
B ₁	.040	.050	1.02	1.27
C	.008	.015	.020	.038
D ⁽⁴⁾	.348	.430	8.84	10.92
D ₁	.005	—	0.13	—
E ₁ ⁽⁴⁾	.240	.280	6.10	7.11
e	.075 BASIC	—	1.91 BASIC	—
F	.025	.035	0.64	0.89
L ⁽⁵⁾	.140	.180	3.56	4.57
N ⁽⁶⁾	5	—	5	—

the package seated in JEDEC seating plane gauge GS-3.

(4) D and E₁ dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).

(5) N is the maximum number of terminal positions.

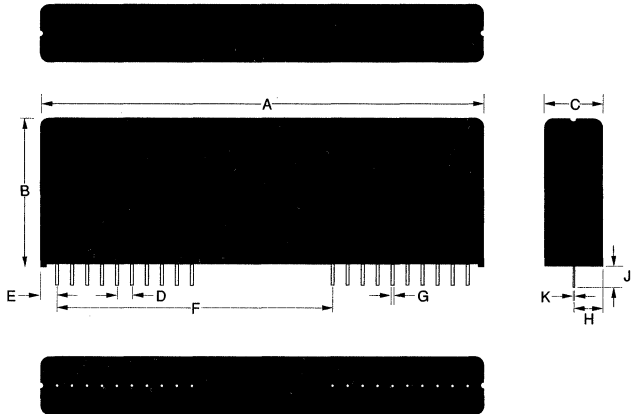
(6) Center of photodiode must be within .01" of center of photodiode area.

NOTES: (1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.

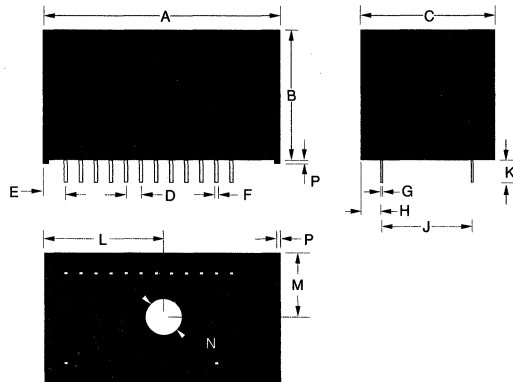
(3) Dimensions A, A₁, and L are measured with

Package Number 900



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.998	3.010	76.15	76.45
B	.994	1.006	25.25	25.55
C	.327	.350	8.30	8.90
D	.093	.106	2.35	2.70
E	.146	.158	3.71	4.01
F	1.693	1.707	43.00	43.35
G	.019	.021	0.48	0.53
H	.163	.175	4.15	4.45
J	.120	.160	3.05	4.06
K	.009	.011	0.23	0.28
L	.014	.026	0.35	0.65

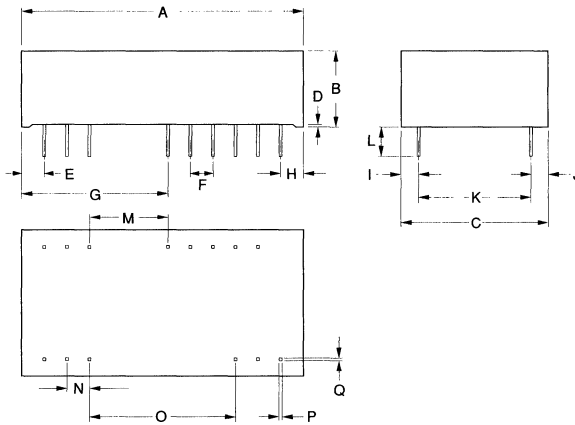
Package Number 901



DIM	MILLIMETERS		INCHES	
	TYP	TYP	TYP	TYP
A	40.00	—	1.58	—
B	22.00	—	0.87	—
C	22.60	—	0.89	—
D	2.54	—	0.10	—
E	3.49	—	0.14	—
F	0.58	—	.023	—
G	0.25	—	.011	—
H	3.38	—	0.13	—
J	15.24	—	0.60	—
K	3.81	—	0.15	—
L	20.00	—	0.79	—
M	11.30	—	0.44	—
N	6.00	—	0.24	—
P	0.60	—	0.024	—

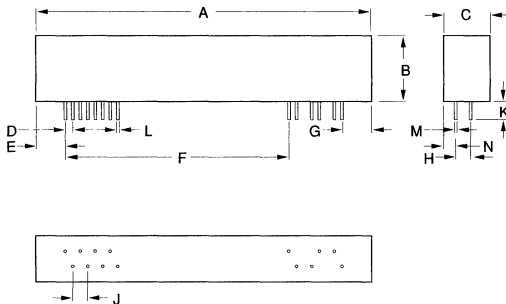
Or, Call Customer Service at 1-800-548-6132 (USA Only)

Package Number 902 — 24-Pin Plastic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.505		63.63	
B	.681		17.30	
C	1.306		33.17	
D	.024		0.60	
E	.202		5.14	
F	.200		5.08	
G	1.302		33.08	
H	.203		5.15	
I	.153		3.885	
J	.153		3.885	
K	1.000		25.40	
L	.256		6.50	
M	.700		17.78	
N	.200		5.08	
O	1.300		33.02	
P	.025		0.64	
Q	.025		0.64	

Package Number 903 — 38-Lead Plastic SIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.220	2.246	56.39	57.05
B	.415	.463	10.54	11.76
C	.295	.325	7.49	8.26
D	.050 TYPICAL		1.27 TYPICAL	
E	.195 TYPICAL		4.95 TYPICAL	
F	1.500 TYPICAL		38.10 TYPICAL	
G	.188 TYPICAL		4.78 TYPICAL	
H	.100 TYPICAL		2.54 TYPICAL	
J	.100 TYPICAL		2.54 TYPICAL	
K	.125 TYPICAL		3.18 TYPICAL	
L	.018 TYPICAL		0.46 TYPICAL	
M	.010 TYPICAL		0.25 TYPICAL	
N	.080	—	2.03	—

MECHANICALS

D

Burr-Brown International

Sales Offices and Sales Representatives

BURR-BROWN CORPORATION

International Sales
PO Box 11400
Tucson, AZ 85734
Telephone (1) 602-746-1111
Fax (1) 602-741-3895
Telex 066-6491 BURRBROWN ATU

AUSTRALIA

Kenelec Pty. Ltd.
Victoria (61) 3 878 2700

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Sao Paulo (55) 11 231-0277

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613-596-9800

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DENMARK

Ditz Schweitzer
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FINLAND

Bexab Finland Oy
Espoo (358) 05023200

FRANCE

Burr-Brown International S.A.
Le Chesnay (33) 1 39 54 35 58
Lyon (33) 78 34 88 33
Toulouse (33) 61 40 03 06

GERMANY

Burr-Brown Int. GmbH
Filderstadt (49) 711 77040
Bremen (49) 421 25 39 31
Düsseldorf (49) 21 54 85 83
Erlangen (49) 91 31 2 40 36
Frankfurt (49) 61 54 8 20 81
München (49) 89 61 77 37

GREECE

Peter Caritato and Assoc. S.A.
Athens (301) 9020115

HONG KONG

Jetronic Technology Ltd.
Kowloon (852) 763-6806

HUNGARY

Sieux Elektronikelemente
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INDIA

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Bombay (91) 22 511 9940

ISRAEL

Gallium Electronics (1986) Ltd.
Ramat-Hasharon
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ITALY

Burr-Brown Int. S.r.l.
Milano (02) 5801 05 04

JAPAN

Burr-Brown Japan Ltd.
Atsugi (81) 462 48 4695
Osaka (81) 6 305 3287
Nagoya (81) 52 775 6761
Tokyo (81) 33 586 8141

MALAYSIA

Serial System Pte. Ltd.
Singapore (65) 280-0200

MEXICO

Borcla, S.A. de C.V.
Mexico City
(52) 5 703 0885

NETHERLANDS

Burr-Brown International B.V.
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Enertec Services Ltd.
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Serial System Pte. Ltd.
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I & R Electronic
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Johannesburg (27) 11 444-2333

SOUTH KOREA

KML Corporation
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SPAIN

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SWEDEN

Bexab Sweden AB
Taebby (46) 8 630 8800

SWITZERLAND

Burr-Brown AG
Rueschlikon (ZH) (41) 1 724 09 28

TAIWAN

Alpha Precision
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TURKEY

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UNITED KINGDOM

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Watford (44) 1923 233837
Abacus Electronics
Newbury (44) 1635 362222

VENEZUELA

Autotrol Tecnologia C.A.
Caracas (58) 2 241-6214

Burr-Brown North American Sales Offices and Sales Representatives

BURR-BROWN CORPORATION

PO Box 11400
Tucson, AZ 85734
Telephone: 602-746-1111

Fast Product Info:

800-548-6132
Fax: 602-741-3895

ALABAMA

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OPA511	High Current, High Power Operational Amplifier	10599	6
OPA512	Very High Current, High Power Operational Amplifier	10600	7
OPA541	High Power Monolithic Operational Amplifier	10737	8
OPA541AD DIE	High Power Monolithic Operational Amplifier Die	11086	2
OPA544	High-Voltage, High-Current Operational Amplifier	11250	8
OPA600	Fast-Settling Wideband Operational Amplifier	10672	8
OPA602	High Speed Precision <i>Difet</i> [®] Operational Amplifier	10753	10
OPA602AD	High Speed Precision <i>Difet</i> [®] Operational Amplifier Die	10875	2
OPA603	High Speed, Current-Feedback Operational Amplifier	11026	13
OPA604	FET-Input, Audio Operational Amplifier	11161	13
OPA606	Wide-Bandwidth <i>Difet</i> [®] Operational Amplifier	10598	8

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OPA606 DIE	Wide-Bandwidth <i>Difet</i> ® Operational Amplifier Die	10660	2
OPA620	Wideband Precision Operational Amplifier	10872	17
OPA620 DIE	Wideband Precision Operational Amplifier Die	11073	2
OPA621	Wideband Precision Operational Amplifier	10939	16
OPA621 DIE	Wideband Precision Operational Amplifier Die	11090	2
OPA622	Wide-Bandwidth Operational Amplifier	11131	19
OPA623	Wide Bandwidth, Current-Feedback Operational Amplifier	11132	17
OPA627/637	Precision High-Speed <i>Difet</i> ® Operational Amplifier	10998	14
OPA628	Low Distortion Wideband Operational Amplifier	11204	16
OPA633	High Speed Buffer Amplifier	10699	10
OPA633 DIE	High Speed Buffer Amplifier Die	10926	2
OPA640	Wideband Voltage Feedback Operational Amplifier	11179	14
OPA641	Wideband Voltage Feedback Operational Amplifier	11189	14
OPA642	Wideband Low Distortion Operational Amplifier	11190	16
OPA643	Wideband Low Distortion Operational Amplifier	11191	14
OPA644	Low Distortion Current Feedback Operational Amplifier	11187	14
OPA646	Low Power, Wide Bandwidth Operational Amplifier	11192	14
OPA648	Ultra-Wideband Current Feedback Operational Amplifier	11253	12
OPA650	Wideband, Low Power Voltage Feedback Operational Amplifier	11264	12
OPA654	Wide Bandwidth, High Output Current Op Amp <i>Difet</i> ®	11098	9
OPA658	Wideband, Low Power Current Feedback Operational Amplifier	11268	14
OPA660	Wide Bandwidth Operational Transconductance Amp and Buffer	11072	19
OPA671	Wide Bandwidth, Fast Setting <i>Difet</i> ® Operational Amplifier	11120	7
OPA675/676	Wideband Switched-Input Operational Amplifier	10864	13
OPA678	Wideband Switched-Input Operational Amplifier	11136	15
OPA1013	Precision, Single-Supply Dual Operational Amplifier	11059	10
OPA2107	Precision Dual <i>Difet</i> ® Operational Amplifier	10863	8
OPA2111	Dual Low-Noise <i>Difet</i> ® Operational Amplifier	10540	10
OPA2111 DIE	Precision Dielectrically-Isolated FET <i>Difet</i> ® Dual Operational Amp Die	10578	2
OPA2111L	LCC Low-Noise Precision <i>Difet</i> ® Operational Amplifier	10803	4
OPA2541	Dual High Power Operational Amplifier	10768	8
OPA2544	High-Voltage, High-Current Dual Operational Amplifier	11249	9
OPA2604	Dual FET-Input, Audio Operational Amplifier	11069	13
OPA2650	Dual Wideband, Low Power Voltage Feedback Operational Amplifier	11266	13
OPA2658	Dual Wideband, Low Power, Current Feedback Op Amp	11269	14
OPA2662	Wide Bandwidth, Dual, Power Operational Transconductance	11129	20
OPA4658	Quad Wideband, Low Power Current Feedback Op Amp	11270	15
OPT101	Monolithic Photodiode and Single-Supply Transimpedance Amp	11257	12
OPT201	Integrated Photodiode and Amplifier	11180	12
OPT202	Photodiode with On-Chip Amplifier	11200	10
OPT209	Photodiode with On-Chip Amplifier	11232	12
OPT211	Monolithic Photodiode and Amplifier	11258	10
OPT301	Integrated Photodiode and Amplifier	11228	12
PCM51JG	16-Bit Digital-to-Analog Converter	10462	8
PCM53JP, KP	16-Bit Monolithic Digital-to-Analog Converter	10575	12
PCM54/55	16-Bit Monolithic Digital-to-Analog Converter	10619	8
PCM56P	Series Input 16-Bit Monolithic Digital-to-Analog Converter	10700	9
PCM58P	Precision 18-Bit Monolithic Audio D/A Converter	10868	6
PCM61	18-Bit Monolithic Audio D/A Converter	10972	5
PCM64P	18-Bit Audio Digital-to-Analog Converter	10786	4
PCM66P	16-Bit Digital-to-Analog Converter	11051	8
PCM67/69	Advanced 1-Bit BiCMOS Dual 18-Bit Digital-to-Analog Converter	11168	13
PCM63P	Colinear™ 20-Bit Monolithic Audio D/A Converter	11083	10
PCM75	16-Bit Hybrid Analog-to-Digital Converter	10624	9
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PCM1715U	Dual Voltage Output CMOS Delta-Sigma Digital-to-Analog Converter with On-Chip Digital Filter	11217	10
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PCM1760/DF1760	Multi-Bit Enhanced Noise Shaping 20-Bit A/D Conversion System	11174	15
PGA100	Digitally-Controlled Programmable Gain/Multiplexed Input Opamp	10457	8
PGA102	High Speed Programmable Gain Amplifier	10579	9
PGA102 DIE	Digitally-Controlled Programmable Gain/Fast Settling Amplifier	10709	2
PGA103	Programmable Gain Amplifier	11208	8
PGA200/201	Digitally Controlled Programmable-Gain Instrumentation Amp	10522	6
PGA202/203	Digitally Controlled Programmable-Gain Instrumentation Amp	11006	11
PGA204/205	Digitally Programmable Gain Instrumentation Amp	11176	14
PWS725/726	Isolated, Unregulated DC/DC Converter	10736	4
PWS727/728	Isolated, Unregulated DC/DC Converters	10987	7
PWS740	Distributed Multichannel Isolated DC-to-DC Converter	10758	7
PWS745	Multi-Channel DC/DC Converter Components	11095	9
PWS750	Isolated, Unregulated DC/DC Converter Components	10838	11
RCV420	Precision 4mA to 20mA Current Loop Receiver	10837	12
REF01	+10V Precision Voltage Reference	11171	10
REF02	+5V Precision Voltage Reference	11177	10
REF05	+5V Precision Voltage Reference (Guaranteed Long-Term Stability)	11178	7
REF10	Precision Voltage Reference	10528	8
REF10L	LCC Precision Voltage Reference	10804	4
REF101	Precision Voltage Reference	10485	8
REF102	Precision Voltage Reference	10900	9
REF200	Dual Current Source	10851	16
REF1004	Micropower Voltage Reference	11172	8
REG1117	800mA Low Dropout Positive Regulator Fixed 2.85V, 3V, 3.3V, 5V, and Adjustable	11162	8
REG5601	SCSI 18-Line Active Terminator	11216	4
SDM854	Hybrid Data Acquisition System	10423	16
SDM856/857	Hybrid Data Acquisition System	10402	19
SDM862/863 872/873	16 Single Ended/8 Differential Input 12-Bit Data Acq. Systems	10686	27
SHC76	Sample/Hold Amplifier	10641	4
SHC85/85ET	Fast IC Sample/Hold Amplifiers	10321	4
SHC298AM	Low-Cost Monolithic IC Sample/Hold	10373	7
SHC600BH	Ultra-High Speed Sample/Hold Amplifier	10644	3
SHC601BH	Ultra-High Speed Sample/Hold Amplifier	10784	4
SHC605	High-Speed Operational Track-And-Hold Amplifier	11165	15
SHC615	Wide-Bandwidth, DC Restoration Circuit	11214	20
SHC803/804	Ultra-High Speed Sample/Hold Amplifier	10512	6
SHC5320	Bipolar Monolithic Sample/Hold Amplifier	10585	12
UAF11/21	Universal Active Filters	10295	8
UAF41	Universal Active Filters	10359	12
UAF42	Universal Action Filter	11070	7
VCA610	Wideband Voltage Controlled Amplifier	11140	13
VFC32	Voltage-to-Frequency and Frequency-to-Voltage Converter	10372	8
VFC32 DIE	Voltage-to-Frequency and Frequency-to-Voltage Converter Die	10604	2
VFC42/52	Voltage-to-Frequency and Frequency-to-Voltage Converter	10390	6
VFC62	Voltage-to-Frequency and Frequency-to-Voltage Converter	10484	8
VFC62L	LCC Voltage-to-Frequency and Frequency-to-Voltage Converter	10807	4

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VFC320L	LCC Voltage-to-Frequency and Frequency-to-Voltage Converter	10805	4
XTR101	Precision, Low-Drift 4mA to 20mA Two-Wire Transmitter	10627	14
XTR101 DIE	Precision, Low-Drift 4mA to 20mA Two-Wire Transmitter Die	10708	2
XTR101L	LCC Precision, Low-Drift 4mA to 20mA Two-Wire Transmitter	10811	4
XTR103	4-20mA Current Transmitter/RTD Excitation And Linearization	11145	11
XTR104	4-20mA Current Transmitter/Bridge Excitation And Linearization	11146	11
XTR110	Precision Voltage-to-Current Converter/Transmitter	10555	10
XTR110 DIE	Precision Voltage-to-Current Converter/Transmitter Die	10605	2
XTR501	High Current Bridge Driver and 4-20mA Transmitter	11212	2
100MS	Magnetic Shield	10421	2
722	Dual-Isolated DC/DC Converter	10398	6
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3528	Ultra Low Bias Current FET Operational Amplifier	10389	6
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3551 SERIES	Wideband and Fast-Settling FET Operational Amplifiers	10301	4
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3554	Wideband Fast-Settling Operational Amplifier	10331	8
3573	High Current — High Power Operational Amplifier	10393	4
3580/3581/3582	High Voltage Operational Amplifiers	10313	4
3583	High-Voltage, High-Current Operational Amplifier	10343	4
3584	High-Voltage Operational Amplifier	10376	4
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DEM-ADS7806/O7C	40447	12
DEM-ADS7808/O9C	40457	13
DEM-ADS7810/19C	40454	12
DEM-DAC600-E	40425	8
DEM-DAC650J-E, K-E	40441	8
DEM-DA1710	40463	4
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DEM-OPA660-3GC	40405	2
DEM-OPA660-4G	40418	6
DEM-OPA660-5G	40417	6
DEM-PCM1702	40429	6
DEM-PCM1710	40442	4
DEM-PCM1760	40428	6
DEM-VCA610AP-C	40430	6



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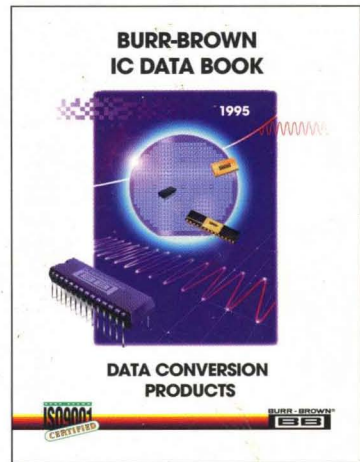
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Tel: (602) 746-1111*
Worldwide Fax (602) 889-1510*
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**Note: As of March 19, 1995, the area code for Arizona
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