CIRRUS LOGIC

CL-SH265

Advance Data Sheet

FEATURES

- Fully hardware- and software-compatible with PC XT/AT computers
- Pin-and-plug-compatible with the CL-SH260
- Proprietary split data field support for recording formats
- Provides direct bus interface logic with on-chip 24-mA drivers
- Low-power or 'sleep' mode
- Contains the logic for daisy chaining two embedded disk controller drives on a PC XT as well as a PC AT
- Supports host data transfer under DMA or Programmed I/O for both PC XT and PC AT modes
- Fast microcontroller interface — 16-MHz 8051, 12-MHz 68HC11
- Provides logic to speed up PC AT command response
- Provides on-chip registers to emulate the IBM® Task File for PC AT, IBM Command Descriptor Block for PC XT
- 84-pin PLCC or 100-pin QFP
- Low-power CMOS technology

Supports:

- direct buffer memory addressing up to 64 KBytes of static RAM
- 8- and 16-bit data transfer on the host bus
- any XT/AT interface speed with programmable and auto-inserted wait states
- interrupt or polled microcontroller interface

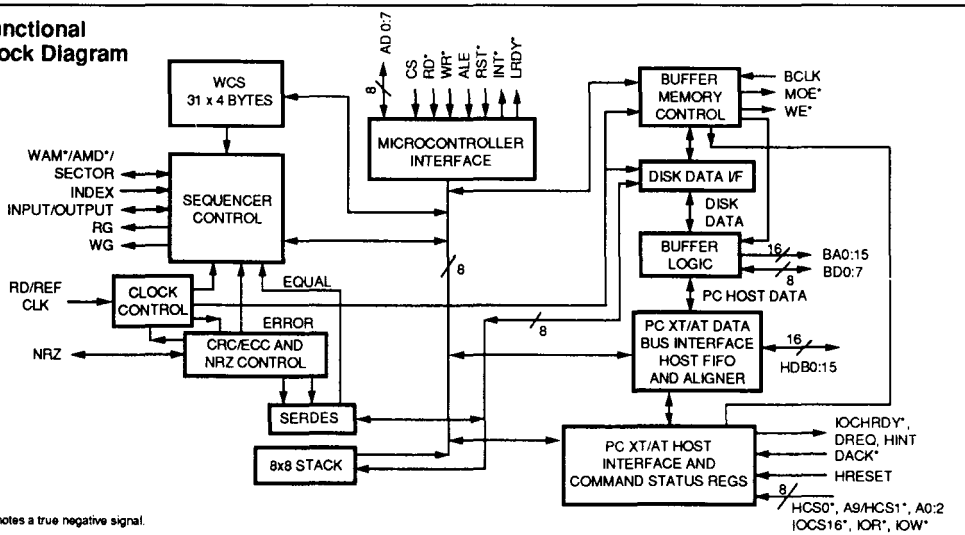
Enhanced PC XT/AT™ Disk Controller

OVERVIEW

The highly integrated CL–SH265 provides a large portion of the hardware necessary to build a Winchester disk controller for the PC XT/AT or other compatible interface. The CL-SH265 includes an advanced Winchester Disk Formatter, a dual-port Buffer Manager, and a host bus interface.

Pin-and-plug-compatible with the CL-SH260, the enhanced CL-SH265 supports disk data rates up to 25 Mbits/sec., a requirement in high-performance disk drives. A proprietary split data field technique optimizes disk capacity, enables faster access times, and increases data rates. A power-down mode makes the CL-SH265 ideal for laptop and power-sensitive applications.

Functional Block Diagram



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OVERVIEW (cont.)

Because the controller is fully compatible with the CL-SH260, it provides an easy upgrade for existing designs and higher-performance systems. Several enhancements have been made to the CL-SH265's Disk Formatter that reduce system component count and eliminate real-time processing constraints.

The CL-SH265's Disk Formatter consists of a serializer/deserializer, a flexible RAM-based Sequencer, and CRC/ECC generation circuitry. The industry standard 16-bit CCITT-CRC, conventional 32-bit AT ECC polynomial, and a computer-generated 56-bit ECC polynomial are all supported in hardware. The ECC circuitry includes hardware correction assist logic to speed the correction process. The CL-SH265 Buffer Manager will control up to 64 KBytes of SRAM buffer memory as a dual ported circular buffer. It also supports a segmented buffer with 4-Kbyte increments.

The CL-SH265 works with a local microcontroller; it has a multiplexed address and data bus similar to that provided by the Intel 8051 family of microcontrollers and the Motorola 68HC11. Also provided is a READY signal interface for high-speed microcontrollers. It supports both interrupt and polled processor interfaces. The maskable interrupts include many disk and host interface events. The CL-SH265 also has hardware to speed up microcontroller access of the Buffer Memory.

ADVANTAGES

Unique Features	Benefits
• *Pin-and-plug-compatible with the CL-SH260*	Easy upgrade path for existing designs.
• *Proprietary Split Data Field support*	Optimizes disk capacity, enables faster access times and data rates.
• *Low-power or 'sleep' mode*	Reduces power consumption with power-down mode.
• *Provides automatic wait states or pre-programmed wait states for extended cycle transfers*	Can be compatible with any host CPU speeds. Prevents host overrun or underrun conditions.
• *Provides logic for daisy-chaining two embedded controller drives on the AT or XT bus in a Master/Slave configuration*	Allows the use of two embedded disk controllers in a system.
• *Supports 10 MBytes/sec buffer memory throughput*	Can be used in high-performance applications.
• *31 Words of Writable Control Store*	Provides great flexibility to implement various formats and defect management schemes.
• *Computer-generated 56/32-bit ECC polynomial embedded in hardware*	Single-burst error correction up to 23 bits. Probability of miscorrection as low as 10^{-14} per bit corrected with the 56-bit polynomial.
• *ECC circuitry provides logic to speed up the correction process*	Hardware correction with minimal MPU intervention. Can correct within a single sector time.
• *Data rate up to 25 Mbits/sec.*	Can be used in high-performance applications.
• *Maskable microcontroller interrupt capability*	Relieves the microcontroller from polling to perform other tasks. Provides status information to the microprocessor when interrupts are disabled.
• *Sector Size Counter*	Reads and writes sectors larger than 512 bytes without microcontroller intervention.
• *Provides on-chip 24 mA-drivers with 300-pF drive capability for XT/AT interface*	Eliminates external hardware interface drivers.

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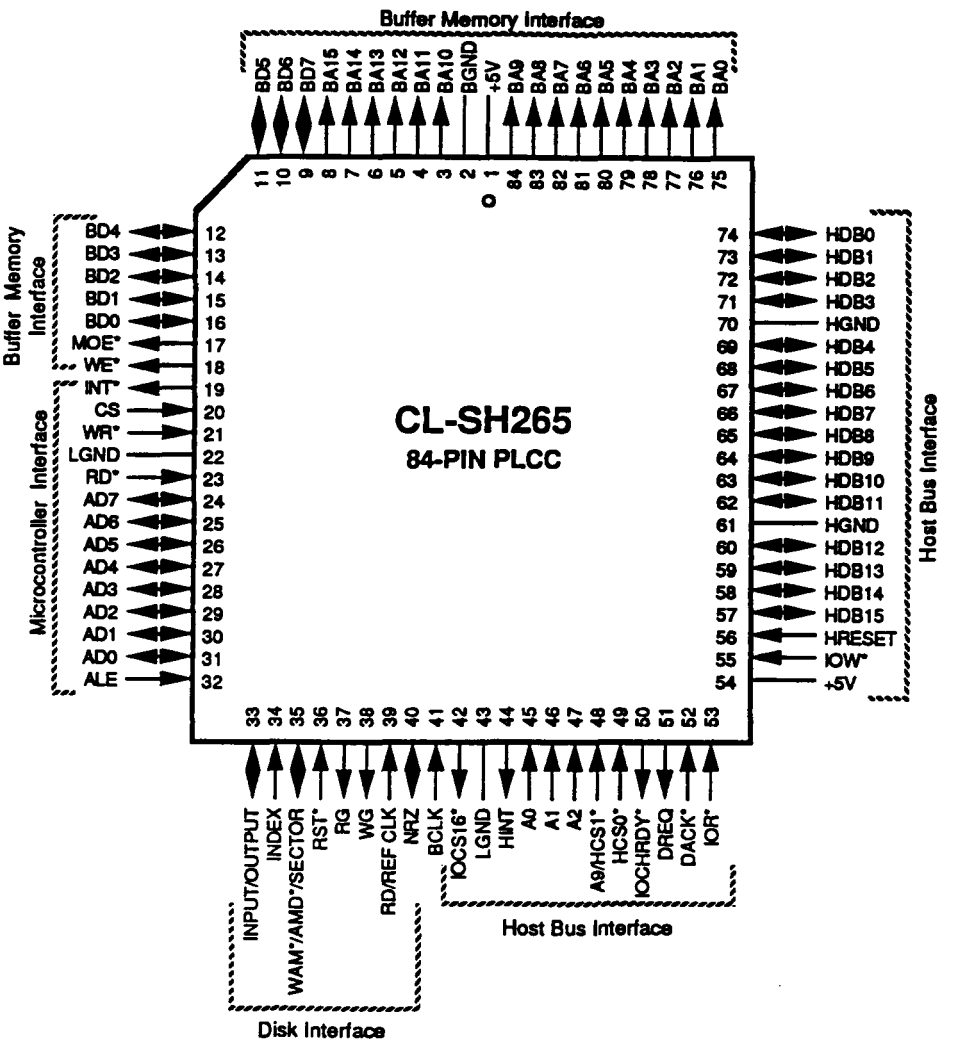
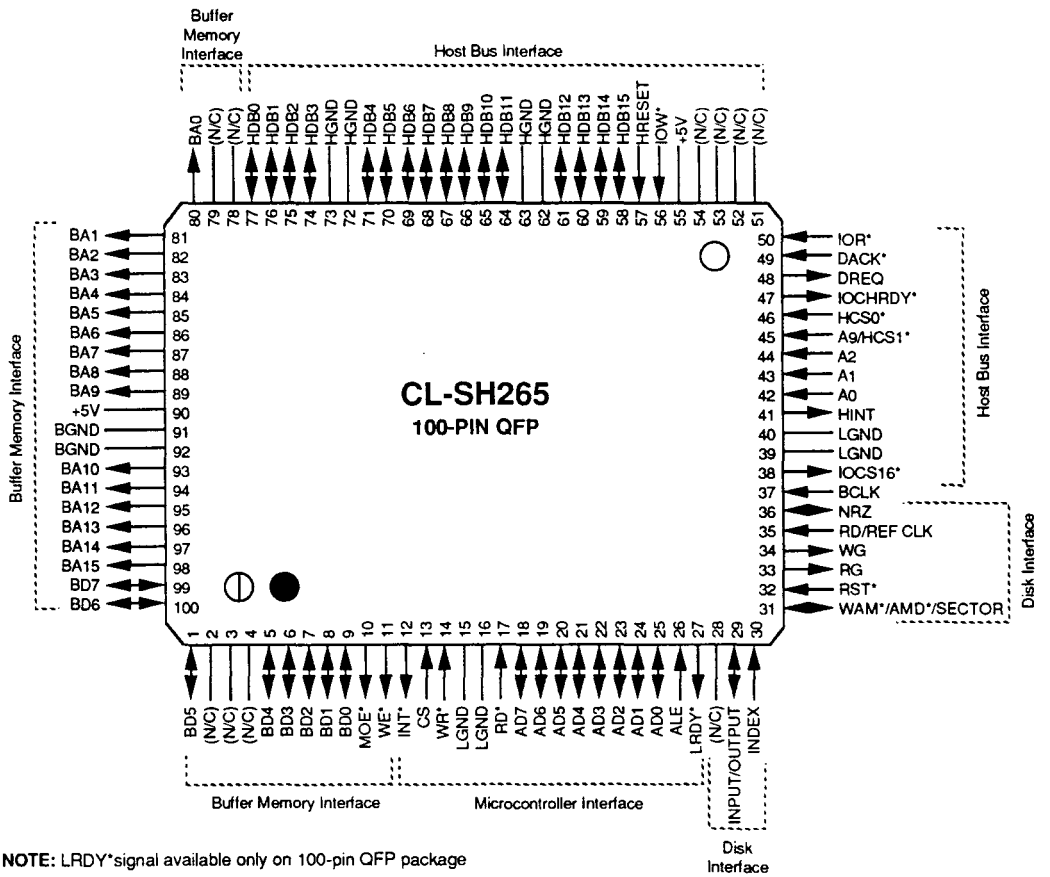
1. PIN INFORMATION

The CL-SH265 is available in either an 84-pin Plastic Leaded Chip Carrier (PLCC) or a 100-pin Quad Flat Pack (QFP) package. **Pin numbers mentioned throughout the text refer to the 84-pin PLCC package unless otherwise noted.** The diagram below shows the pin-out of the 84-pin package. All unused inputs must be tied to their inactive state to VCC or GND respectively.

1.1 Pin Diagram for the 84-Pin Plastic Leaded Chip Carrier (PLCC)



1.2 Pin Diagram for the 100-Pin Quad Flat Pack (QFP)



NOTE: LRDY*signal available only on 100-pin QFP package

1.3 Pin Assignments

The following conventions are used on the pin assignment tables. An asterisk (*) denotes a negative true signal. An (I) indicates an input pin. An (O) indicates an output pin. An input/output pin is indicated by (I/O). A (Z) indicates a tri-state output or input/output pin. Open drain output pins are indicated by (OD). **The pin numbers throughout this data sheet refer to the 84-pin PLCC package unless otherwise noted.**

BUFFER MEMORY INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
BA[15:0]	8-3, 84-75	98-93, 89-80	O	**BUFFER MEMORY ADDRESS LINES:** Bits 0-15.
BD[7:0]	9-16	99-100,1,5-9	I/O	**BUFFER MEMORY DATA BUS:** These eight signals are Bits 0-7 of the 8-bit parallel data lines to/from the buffer memory.
MOE*	17	10	O	**MEMORY OUTPUT ENABLE:** This signal is asserted low when a buffer memory operation is active.
WE*	18	11	O	**WRITE ENABLE:** This signal is asserted low when a buffer memory Write operation is active.
BCLK	41	37	I	**SYSTEM CLOCK:** This is a clock input which is used to generate buffer memory access cycles.

MICROCONTROLLER INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
INT*	19	12	O,OD	**LOCAL MICROCONTROLLER INTERRUPT**: This signal is programmable for either push-pull or open-drain output circuitry.
CS	20	13	I	**CHIP SELECT**: This signal must be asserted to access the CL-SH265 registers.
WR*	21	14	I	**WRITE**: When the WR* signal is asserted low and the CHIP SELECT signal (Pin 20) is asserted high, the data on the A/D lines will be written into the specified register.
RD*	23	17	I	**READ**: When the RD* signal is asserted low and the CHIP SELECT signal (Pin 20) is asserted high, the data from the specified register will be read on to the A/D lines.
AD[7:0]	24-31	18-25	I/O	**LOCAL MICROCONTROLLER ADDRESS/ DATA**: These are tri-state Address/Data lines which interface with a multiplexed microcontroller Address/Data bus.
LRDY*	N/A	27	O	**LOCAL MICROCONTROLLER READY**: This signal is driven low during every access to the CL-SH265 by the local microcontroller. The duration of the low or wait period is programmable.
ALE	32	26	I	**ADDRESS LATCH ENABLE**: This control signal latches the address on the A/D lines.
RST*	36	32	I	**RESET**: When this signal is asserted low, it stops all operations within the chip and deasserts the READ GATE (Pin 37) and the WRITE GATE (Pin 38) signals. All I/O signals and Host outputs are set to a high-impedance state. See the section on register initialization (Section 5.3).

DISK INTERFACE PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
INPUT/ OUTPUT	33	29	I/O	**INPUT/OUTPUT**: This is a general-purpose control and status signal. It can be configured to be an input or an output in the SEQUENCER OUT ENABLE bit (Bit 6) of the FORMATTER MODE SELECTION Register (77H). When configured as an input, this signal is available to synchronize the Sector Format Sequencer to an external event. When configured as an output, this signal is controlled by Bit 2 of the CONTROL FIELD (A0H thru BEH) of the Writable Control Store (WCS). At power-on, this signal is configured as an input.
INDEX	34	30	I	**INDEX** : This is input for the INDEX pulse received from the disk drive.
WAM*/ AMD*/ SECTOR	35	31	I/O	**WRITE ADDRESS MARK / ADDRESS MARK DETECT/ SECTOR:** This signal can be configured to operate in Hard or Soft Sector mode by initializing the HARD/SOFT* SECTOR MODE CONTROL bit (Bit 7) of the FORMATTER MODE SELECTION Register (77H). The default is Soft Sector mode. Also, in Soft Sector mode, when the READ GATE signal (Pin 37) is asserted, a low level input on this signal indicates Address Mark detected. In Hard Sector mode, this is the input for the SECTOR pulse.
RG	37	33	O	**READ GATE**: This signal is asserted when the CL-SH265 is reading NRZ data from the disk interface.
WG	38	34	O	**WRITE GATE**: This signal is asserted when the CL-SH265 is writing NRZ data to the disk interface.
RD/REF CLK	39	35	I	**READ/REFERENCE CLOCK**: This signal is used in conjunction with the NRZ signal (Pin 40) to clock data in and out of the chip.
NRZ	40	36	I/O	**NRZ**: Read data input from the disk when the READ GATE signal (Pin 37) is asserted; write data output to the disk when the WRITE GATE signal (Pin 38) is asserted.

HOST BUS PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
IOCS16*	42	38	OD	**16-BIT DATA TRANSFER**: This signal indicates that a 16-bit sector buffer transfer is active on the PC bus.
HINT	44	41	O,Z	**HOST INTERRUPT**: This signal is asserted to indicate to the Host that the disk controller needs attention.
A[2:0]	47-45	44-42	I	**HOST ADDRESS LINES**: The Host address lines A[2:0] and A9 are used to access the various PC AT/XT control, status, and data registers. Only the A[1:0] lines are used for PC XT operation.
A9/HCS1*	48	45	I	**A9/HCS1***: This is a multiplexed input signal. When the HCS1 MODE ENABLE bit (Register 52H, Bit 3) is reset, this input is HOST ADDRESS LINE A9. When the HCS1 MODE ENABLE bit (Register 52H, Bit 3) is set, this input is HOST CHIP SELECT 1. When this signal is configured as HCS1*, this input is ignored when the DACK* signal (Pin 52) is asserted low.
HCS0*	49	46	I	**HOST CHIP SELECT 0**: When this signal is asserted low, this input selects access to the control, status and data registers. This input is ignored when the DACK* signal (Pin 52) is asserted low.
IOCHRDY*	50	47	O,Z	**I/O CHANNEL READY**: This signal is asserted low to extend Host transfer cycles when the disk controller is not ready to respond.
DREQ	51	48	O,Z	**DMA REQUEST**: This signal is used during DMA transfer between the Host and the CL-SH265.
DACK*	52	49	I	**DMA ACKNOWLEDGE**: This signal is used during DMA to complete the DMA handshake for data transfer between the Host and the CL-SH265. In a typical AT application, this input signal is not used and should be pulled up to power through a 10 K ohm resistor.
IOR*	53	50	I	**INPUT READ SELECT**: This signal is asserted low by the Host during a Host Read operation. When this signal is asserted low with the HCS0*/HCS1* or the DACK* signal (Pin 52), status or data is enabled onto the Host data bus.

HOST BUS PINS (cont.)

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
IOW*	55	56	I	**INPUT WRITE SELECT**: This signal is asserted low by the Host during a Host Write operation. When this signal is asserted low with the HCS0*/HCS1* or the DACK* signal (Pin 52), data from the Host data bus is strobed into the CL-SH265.
HRESET	56	57	I	**HOST RESET**: When this signal is asserted, it initializes the Control/Status Registers and stops any command in process. See the section on register initialization (Section 5.3).
HDB[15:0]	57-60, 62-69, 71-74	58-61 64-71 74-77	I/O	**HOST DATA BUS**: During PC AT operations, Host data bus signals HDB[15:0] are used for transfers between the buffer memory and the Host data bus signals HDB[7:0] are used for control, status, and ECC byte access. During PC XT operation only the HDB[7:0] lines are used; the HDB[15:8] lines are tri-state.

POWER AND GROUND PINS

SYMBOL	PIN NUMBER PLCC	QFP	TYPE	DESCRIPTION
+5V	1,54	55,90	N/A	POWER SUPPLY (+5).
BGND	2	91-92	N/A	BUFFER BUS GROUND.
LGND	22,43	15-16, 39-40	N/A	LOGIC GROUND.
HGND	61,70	62-63,72-73	N/A	HOST GROUND.

2. MICROCONTROLLER-ACCESSIBLE REGISTER TABLES

2.1 Buffer Manager and PC Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
50H	R	HOST INTERRUPT STATUS
51H	R/W	HOST INTERRUPT ENABLE
52H	R/W	UNIQUE FEATURES CONTROL/STATUS
53H	R/W	DMA CONTROL
54H	R/W	STATIC RAM BUFFER SIZE/SEGMENT ADDRESS
58H	R/W	PC MODE CONTROL
59H	R/W	BUFFER MANAGER/PC RESET CONTROL
5AH, 5BH	R/W	READ ADDRESS POINTER (RAP) (16 bits)
5CH, 5DH	R/W	WRITE ADDRESS POINTER (WAP) (16 bits)
5EH, 5FH	R/W	PC STOP POINTER (PC-SP) (16 bits)

2.2 Formatter Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
4EH	R/W	SECTOR SIZE
71H	R/W	ECC CONTROL
72H	R/W	ECC CORRECTION SHIFT-REGISTER/COUNTER
73H - 76H	R	ECC STATUS
77H	R/W	FORMATTER MODE SELECTION
78H	R	NEXT ACTIVE SEQUENCER ADDRESS
78H	W	BRANCH ADDRESS
79H	R	SEQUENCER STATUS
79H	W	SEQUENCER START ADDRESS
7AH	R/W	OPERATION CONTROL / STATUS
7BH	R/W	WAM CONTROL
7CH	R/W	SYNC PATTERN
7DH	R	FORMATTER INTERRUPT STATUS
7EH	R/W	FORMATTER INTERRUPT ENABLE
7FH	R	FORMATTER STACK READ
7FH	W	CLOCK/SYNC CONTROL

2.3 External Access Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
4DH	R	SHADOW LATCH
70H	R/W	BUFFER MEMORY ACCESS

2.4 Writable Control Store (WCS)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
80H-9EH	R/W	NEXT ADDRESS FIELD
A0H-BEH	R/W	CONTROL FIELD
C0H-DEH	R/W	COUNT FIELD
E0H-FEH	R/W	DATA FIELD

2.5 Sequencer Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
49H-4CH	R/W	CURRENT SEQUENCER WORD

2.6 Auxiliary Control Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
48H	R/W	AUXILIARY CONTROL REGISTER 0
4FH	R/W	AUXILIARY CONTROL REGISTER 1

2.7 Microcontroller–Host Interface Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
40H-47H or 60H-67H	R/W	HOST REGISTER FILE
55H-57H	R/W	HOST CONTROL/STATUS
73H	W	AUTOCOMMAND/POWER DOWN "LOCK" RELEASE

3. FUNCTIONAL DESCRIPTION

The CL-SH265 is designed to be used with a low-cost microcontroller, which allows it to maintain a "loose" synchronization with the real-time disk operation. The CL-SH265 maintains "close" synchronization with the data to and from the disk drive and provides the signals necessary to control this path. Using the CL-SH265 means a lower total-part count for the intelligent disk drive design with the PC XT/AT interface.

The CL-SH265 is divided into four major functional blocks:

- **Microcontroller Interface**
- **Disk Formatter**
- **Buffer Memory Interface**
- **Host Interface**

3.1 Microcontroller Interface

The microcontroller interface is based on an eight-bit multiplexed address and data bus found on popular microcontrollers, such as the Intel 8085/8031/8051 and the Motorola 68HC11.

The CL-SH265 decodes addresses from 40H to FFH. In order to prevent erroneous operations, the disk controller board design should reserve the decoding of addresses 40H to FFH for the CL-SH265 only. However, the CL-SH265 does not decode addresses 68H to 6FH; the decoding of addresses 40H-47H, as well as 60H-67H, can be totally disabled by resetting the HOST REGISTER FILE ACCESS ENABLE bit (Register 77H, Bit 1). In that case, the CL-SH265 will not decode addresses 40H-47H and 60H-67H, as well.

The CL-SH265 provides a register file which the microcontroller can access to interface with the Host. This register file can be mapped to either 40H-47H or 60H-67H (when access to the register file is enabled — Register 77H, Bit 1 is set) by programming the HOST REGISTER FILE DECODE SELECT bit (Register 77H, Bit 2). Mapping these registers into addresses 40H-47H will disable the CL-SH265 from decoding addresses 60H-67H (which can be used for external system use). Mapping them into 60H-67H will make addresses 40H-47H available for external system use.

The definition of these registers is also different when the CL-SH265 is programmed to operate in the PC XT mode versus the PC AT mode. For detailed descriptions, see the Microcontroller Host Interface section (Section 14).

The CL-SH265 has a programmable interrupt circuit available. The interrupt sources are: PC Selection, PC Transfer Done, PC Reset, PC Transfer Overrun, Post Transfer Status Read Detected, INDEX Past, SECTOR Past, Disk Data Transfer Detected, ECC Error, Sequencer Stopped, Input Detected, and Sequencer Output Detected. The interrupt capability can be completely disabled (by resetting Register 77H, Bit 3), or the individual interrupt sources can be masked. Four interrupt registers provide the status and mask programmability for interrupt sources. Even when the interrupts are disabled (Register 77H, Bit 3 is reset), the Interrupt Status Registers may be used as a focal point for microcontroller control, when the CL-SH265 is being used in a polled mode.

The CL-SH265 provides the microcontroller read access to external switch settings. The microcontroller accesses these switches by reading Register 70H, with the MOE* DISABLE bit (Register 52H, Bit 0) set to logical 1. The microcontroller-readable switches connect to the buffer memory data bus. These switches must be installed with relatively high impedance pull-ups and pull-downs, so that the resistor impedance does not affect buffer memory performance. (It is recommended that 150 KΩ pull-up and 15 KΩ pull-down resistors be used, then wait 25 µsec after the last buffer memory access for stability).

3.2 Disk Formatter

The operation of the Disk Formatter is controlled by the contents of the Sequencer Writable Control Store (WCS). A Sequencer program must be entered into the WCS before the

CL-SH265 Disk Formatter can function properly. Under firmware control, the Disk Formatter can be made to sequence through different types of operations, such as: Read ID, Read ID and Read Data, Read ID and Write Data, and Write ID and Write Data.

The Sequencer controls the timing relationships between the disk interface output signals and monitors disk interface input lines to branch to different Sequencer locations. The track layout, such as gap lengths, sector size, and sector data fill character, can be flexibly defined in the WCS. The CL-SH265 Disk Formatter also has other registers that can be used to control the definition of the track format, such as the SYNC character or the ADDRESS MARK.

The WCS consists of 124 bytes, organized as 31 words, each four bytes wide. The WCS word can be broken down into DATA, COUNT, NEXT ADDRESS and CONTROL FIELDS.

The DATA FIELD contains data which may be used to initialize the track format, including gap, ID field, and sector data fill characters. This data can also be compared to the NRZ data-in to identify various fields in a sector or to execute sector-data comparisons.

The COUNT FIELD specifies the initial value, minus one of the Sequencer counter for the current word. The Sequencer counter is decremented once every eight READ/-REFERENCE CLOCK (RD/REF CLK) cycles. When the count reaches zero, the Sequencer will go to the next address.

The next address will be based on the contents of the NEXT ADDRESS FIELD of the WCS word, unless a branch condition has been programmed and met during the last byte of the current WCS word.

The CONTROL FIELD is used to generate and initiate all synchronous NRZ data handling operations.

The microcontroller's control of the Sequencer revolves around the SEQUENCER START ADDRESS (Register 79H) and the BRANCH ADDRESS (Register 78H) or WCS DATA FIELD BRANCH. Writing to Register 79H loads the starting address (where the Sequencer is to begin execution), and causes the four bytes at that WCS word to be fetched and written into the Current Sequencer Word Registers (Registers 49H-4CH).

The serial-data-flow portion of the Disk Formatter consists of a CRC/ECC generator and a serializer/deserializer. Data to be written to the disk enters the CL-SH265 in a byte-wide format. It is serialized and processed through a CRC/ECC generator. An NRZ serial bit stream is then shifted out to the disk drive. Note that the NRZ serial bit stream will include serialized constants required for Address Marks, gaps, and ID fields, as well, as the serialized data and ECC generated output.

The CL-SH265 can be programmed (in the WCS COUNT FIELD) for CRC or an ECC polynomial. It can be fully suppressed to use external ECC circuitry.

The CRC polynomial used is the CCITT-CRC code:

$$X^{16} + X^{12} + X^{5} + 1$$

The CL-SH265 provides the option of using a 56-bit or a 32-bit ECC polynomial by programming the COUNT FIELD of the appropriate WCS word. The forward and reverse 56-bit ECC polynomial is a computer-generated code. The forward polynomial is:

$$X^{56}+X^{52}+X^{50}+X^{43}+X^{41}+X^{34}+X^{30}+X^{26}+X^{24}+X^{8}+1$$

The reverse polynomial is:

$$X^{56}+X^{48}+X^{32}+X^{30}+X^{26}+X^{22}+X^{15}+X^{13}+X^{6}+X^{4}+1$$

This polynomial can detect single-burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length. The 32-bit ECC polynomial is the standard polynomial found in IBM PC AT controllers.

The forward polynomial is:

$$X^{32}+X^{28}+X^{26}+X^{19}+X^{17}+X^{10}+X^{6}+X^{2}+1$$

The reverse polynomial is:

$$X^{32}+X^{30}+X^{26}+X^{22}+X^{15}+X^{13}+X^{6}+X^{4}+1$$

The forward and reverse polynomial is selected by programming ECC CONTROL (Register 71H, Bit 7). Whichever polynomial is selected, the ECC/CRC shift registers are preset to all 1's or 0's, based on the ECC preset control bit (Register 4FH, Bit 5).

Data read from the disk enters the CL-SH265 as an NRZ serial-bit stream. The input data stream is processed through the ECC generator and deserialized into a byte-wide format. The syndrome is saved in the ECC registers.

If an ECC error is detected after a Read Data operation, the microcontroller uses Registers 71H - 76H to determine if the error is correctable, and to calculate the error pattern and displacement from the beginning of the sector. After this, the error can be corrected in the data bytes in the buffer memory. The CL-SH265 has hardware-assist circuitry to speed up the correction process.

During a read process from the device, the CL-SH265 also has the ability to compare the data being received on a byte-by-byte basis, with information either from the data field of the WCS (such as verifying the ID field) or from the external buffer memory (such as during a data-field-search operation).

The CL-SH265 also has a circular stack eight bytes deep. By enabling this (setting Bit 4 of the WCS CONTROL FIELD) during the Read operation, information read from the disk drive can be pushed onto the stack to be examined later at a lower speed by the microcontroller (Register 7FH). This capability can be used to pass the ID field to the microcontroller for defect management, seek verification and other disk controller tasks.

3.3 Buffer Memory Interface

Byte-wide data transferred by the CL-SH265 is passed to and from the buffer memory on the BUFFER MEMORY DATA BUS BD[7:0].

The CL-SH265 Buffer Manager is capable of controlling buffer sizes from 512 to 64K bytes of static RAM. The buffer can be configured in normal or segmentation mode. In segmentation mode, segments from 4K to 32K may be accessed. The chip provides 16 buffer memory address lines BA[15:0] along with a Memory-Output-Enable (MOE*) signal (Pin 17) and a Write-Enable (WE*) signal (Pin 18), for the static buffer memory.

The period of the buffer memory access cycles is determined by programming Bits 6 and 7 of the CLOCK/SYNC CONTROL Register (7FH) and is based on the BCLK input (Pin 41). The CL-SH265 can support up to 10 MBytes/sec of buffer memory throughput. The period of the buffer memory access cycles, along with other CL-SH265 specifications, determines the access time requirement for the buffer memory. The CL-SH265 samples the data from the RAM at the falling (trailing) edge of BCLK. The equations below can be used to determine the buffer memory throughput and the RAM speeds to be used.

Buffer Memory Throughput =

$$\frac{1}{\text{Period of memory access cycle}}$$

T_1 = Period of buffer memory access cycle = Bacc

For Buffer Memory Read

Max. Read Access Time = $T_1 - Mh_{max} - Dis_{min}$

Min. Output Enable = $Mw_{max} - Dis_{min}$

For Buffer Memory Write

Address set up to WE*↓ = $T_1 - Ww_{max} - Wh_{max}$

Data set up to WE*↑ = Dov_{min}

NOTE: For Mh_{max}, Dis_{min}, Mw_{max}, Wh_{max}, Dov_{min} and Bacc definitions, refer to the buffer memory Read/Write timing parameters (Section 15.3 A.C. Characteristics).

Register 70H decode is provided for the microcontroller to gain access to the buffer memory. The buffer memory data bus and the microcontroller data bus are internally bridged accordingly. Register 70H should not be accessed during Host or Disk transfers with the buffer memory.

Register 70H buffer memory access locations are based upon the contents of the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) if the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0 (WOP*); and on the contents of the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) if the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1 (ROP). The READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) will be incremented by an access to Register 70H, if Register 48H, Bit 0, BUFFER POINTER AUTO-INCREMENT ENABLE is set.

Disk Transfer

In case of disk transfers, a byte is transferred as the Disk Formatter requires service (for a deserialized byte or a byte to serialize). The direction of the transfer is determined by the value of ROP/WOP* bit (Register 53H, Bit 4). For a Disk Read operation, the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1 and the NRZ data is deserialized and written to the buffer memory at the location specified by the contents of the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH). For a Disk Write operation, the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0 and the data read from the buffer memory at the location specified by the contents of the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) is serialized and written to the disk.

Host Data Transfer

In case of transfers between the Host bus and the buffer memory, data is transferred under DMA or Programmed I/O (PIO) control. The direction of transfer is determined by the contents of the HOST WRITE ENABLE and the HOST READ ENABLE bits (Register 53H, Bits 2 & 3 respectively), along with the ROP/WOP* bit (Register 53H, Bit 4).

NOTE: For correct operation of the CL-SH265, the ROP/WOP* bit (Register 53H, Bit 4) MUST be set to logical 1 when the HOST READ ENABLE bit (Register 53H, Bit 3) is set. Also, the ROP/WOP* bit (Register 53H, Bit 4) MUST be reset to logical 0 when the HOST WRITE ENABLE bit (Register 53H, Bit 2) is set.

If the HOST READ ENABLE bit (Register 53H, Bit 3) and the ROP/WOP* bit (Register 53H, Bit 4) are set to logical 1, the READ ADDRESS POINTER (RAP—Registers 5AH and 5BH) is used during transfers from the buffer memory to the Host.

If the HOST WRITE ENABLE bit (Register 53H, Bit 2) is set to logical 1 and the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0, the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) is used during transfers from the Host to the buffer memory.

During Host data transfers, the last buffer memory address that can be accessed is controlled by the PC STOP POINTER (Registers 5EH and 5FH). This PC STOP POINTER (Registers 5EH and 5FH) is compared with the appropriate Address Pointer (the READ ADDRESS POINTER—RAP (Registers 5AH and 5BH), or the WRITE ADDRESS POINTER —WAP (Registers 5CH and 5DH)), masked by the contents of the BUFFER SIZE Register (54H). When a match occurs, the HOST TRANSFER DONE bit

(Register 53H, Bit 5) is set, signifying the completion of the transfer to or from the Host.

3.4 PC Host Interface

The CL-SH265 provides the capability for direct connection to the Host bus. The drivers can sink up to 24mA current and drive a load up to 300pf.

The CL-SH265 also provides circuitry to extend the Host I/O cycle and insert Wait states by asserting low the IOCHRDY* signal (Pin 50). This circuit is only active during Programmed I/O Host transfers. The CL-SH265 inserts Wait states in the following two ways:

(1) It can be programmed in PC WAIT STATE (Register 58H, Bits 0 and 1) to insert Wait states on any Host I/O transfer. This can be used to extend the width of the IOR*/IOW* pulse, in case of a fast CPU with short IOR*/IOW* pulses.

(2) When a Wait state is enabled (Register 58H, Bit 2 is set), it will be automatically inserted by asserting low the IOCHRDY* signal (Pin 50) (only during Host I/O transfers to/from buffer memory) when the CL-SH265 is not ready for the transfer.

If programmed Wait states (as in 1) are enabled, the automatic Wait state circuit will be activated (after the programmed number of Wait states have been inserted), if additional Wait states are necessary.

The CL-SH265 has circuitry to speed up the performance of the disk controller by decoding Write commands requiring data transfer from the Host to the buffer memory, i.e., Format (5XH), Write Buffer (E8H), Write or Write Long (3XH). The CL-SH265 will automatically start accepting data from the Host, without local microcontroller control, when the AT HOST COMMAND Register is loaded by the Host. If interrupts are enabled, the CL-SH265 then generates an interrupt to the local microcontroller. The PC STOP POINTER (Registers 5EH and 5FH) is initialized to 01FFH. If the DISABLE STOP POINTER COMPARE bit (Register 52H, Bit 6) is set, the local microcontroller must initialize the PC STOP POINTER (Registers 5EH and 5FH) to enable the comparison of the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) with the PC STOP POINTER (Registers 5EH and 5FH). The CL-SH265 Disk Formatter will disconnect from the Buffer Manager, upon receipt of one of these commands. It will also disable write access by the local microcontroller to Registers 53H, 5CH-5FH, and read/write access to Register 70H. Access to these registers will be enabled when the local microcontroller writes to Register 73H. The local microcontroller must write to Register 73H, to enable transfers between the Disk Formatter and the buffer memory.

If Bit 1 of the command byte is set (for Read/Write Long commands), then all buffer memory transfers to/from the Host will exceed the PC STOP POINTER (Registers 5EH and 5FH) by the count of ECC bytes. Initially, the PC STOP POINTER (Registers 5EH and 5FH) is set at the end of the data field. When the active READ ADDRESS POINTER (RAP — Registers 5AH and 5BH) or WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH) matches the PC STOP POINTER (Registers 5EH and 5FH), the internal FIFO will be emptied of the word-width data. The ECC bytes will then be transferred in byte mode, and the respective address pointer will be incremented by the number of ECC bytes.

The CL-SH265 provides circuitry to support two embedded AT or XT disk controller drives in a system. There are two bits (Bits 1 and 2) in Register 52H for this configuration. The MASTER/SLAVE MODE ENABLE bit (Register 52H, Bit 1) must be set to enable the two disk drive Master/Slave configuration. The MASTER/SLAVE SELECT bit (Register 52H, Bit 2) configures the disk drive as a Master or Slave. For the PC AT, if this bit is set, the disk controller responds as a Slave (i.e., it responds when the disk drive number in the AT HOST DRIVE/HEAD Register [Port 1F6H] is set to 1). In general, the register files in both controllers (configured as Master and Slave) will be written to by the Host, no matter which disk drive is selected in the AT HOST DRIVE/HEAD Register. Only the selected disk drive, however, will execute the command. The only exception is during Power-up or Diagnostic commands. In that case, both the Master and the Slave will run the diagnostics, but the Master will return the status to the Host. For the PC XT, the controller responds as a slave

if Bit 2 of the host DRV/DMA/IRQ ENABLE register is set, and Register 52H, Bit 2 is set.

4. FUNCTIONAL OPERATION

The CL-SH265 performs two basic disk operations, reading NRZ data in and writing NRZ data out. These two operations can be combined easily into the following four major functions:

- Read ID or Sector Identification
- Read ID and Write Data or Sector Write
- Read ID and Read Data or Sector Read
- Write ID and Write Data or Format Sector

These can be further modified to perform the Search Data and Verify Data functions.

Read Operation

One of the requirements of the Read operation is to synchronize the incoming data on byte boundaries, and then either process the data or pass the data through to the buffer memory.

Data synchronization occurs when a specific incoming data stream compares to the sync pattern programmed in the SYNC PATTERN Register (7CH). The number of bits used in the synchronization comparison is specified by the contents of the CLOCK/SYNC CONTROL Register (7FH), Bits 0-2. The process begins when the CONTROL FIELD of the Current Sequencer Word activates the READ GATE (RG) signal (Pin 37). The serial data passes through a programmable-synchronization comparator until a match is found with the contents of the SYNC PATTERN Register (7CH). If the CL-SH265 is in soft-sectored mode, the comparison must be qualified by the assertion low of the WAM*/AMD*/SECTOR signal (Pin 35) by the time the last NRZ bit of the sync pattern is read into the CL-SH265.

Typically, for soft-sectored formats, the first byte after the synchronization byte is used to differentiate between Sector ID and Data Fields. After synchronization, the Sequencer has the ability to enable the comparison of the incoming data against the DATA FIELD of the WCS, as well as capture the incoming data on the stack. The comparison and branch capability of the Sequencer allows the incoming data to be recognized and acted upon. The programmable compare capability can be used to access the correct sector automatically, by recognizing the proper Sector ID. If the Sector ID does not match the DATA FIELD of the Current Sequencer Word, then the Sequencer can be programmed to stop, and can be restarted by the microcontroller to find the sector again.

Write Operation

The other disk operation of the CL-SH265 is writing NRZ data. This operation begins when the CONTROL FIELD in the Current Sequencer Word activates the WRITE GATE (WG) signal (Pin 38). The WRITE GATE signal (Pin 38) is typically switched on at a specific place in the track layout: during a Write splice after the sector ID ECC (for a Write Sector Data operation), or after INDEX (for a Track Format operation). Data from the Current Sequencer Word's DATA FIELD or from the buffer memory data bus is passed through the serializer, then through the ECC circuitry, and out the NRZ data signal (Pin 40).

Power-down Mode

The CL-SH265 can operate in a power-down mode. This mode is entered whenever the local microprocessor sets Register 48H, Bit 1. Once this bit is set, the CL-SH265 disables all non-essential clocking within the chip. The normal power mode (Register 48H, Bit 1 = 0) is entered when the host writes to the command register, assertion of HRESET (Pin 57), RST* (Pin 32), or a Host-programmed reset. If the normal mode is entered by the host writing to the command register, then the local microprocessor is locked out from re-entering the power-down mode. To clear this lockout condition, the local microprocessor issues a write to Register 73H.

4.1 Sector Identification

The Sector Identification function consists of reading the Sector ID field to identify to the microcontroller the current sector address. This function is typically performed with a comparison of the Sector ID field Address Mark, a capture of the Sector ID field in the stack, and an ECC/CRC

the Sector ID field in the stack, and an ECC/CRC verification of data integrity. Any of the incoming data bytes may be captured in the stack by programming the STACK ENABLE bit (Bit 4) in the WCS CONTROL FIELD. Also, any of the incoming data bytes may be compared against the WCS DATA FIELD by programming both the WCS DATA FIELD and the COMPARE ENABLE bit (Bit 1) in the WCS CONTROL FIELD.

After the Sector Identification function is completed, the microcontroller can then read the SEQUENCER STATUS Register (79H). If there was no ECC error, the microcontroller can then read the stack to identify the current sector address, or it may repeat the function.

4.2 Sector Read

The Sector Read function typically consists of two parts. The first is reading and identifying the desired Sector ID field. This is described in the Sector Identification section (Section 4.1); however, the desired sector address will also be included in the comparison. A branch condition is often programmed at the end of the Sector Identification function, such that if the compared bytes match, and there was no ECC error, the sequencer will automatically execute the second half of the Sector Read function.

After the sector has been positively identified, the second half of the Sector Read function is to transfer the Sector Data field to the buffer memory. After the read, the microcontroller may then read the SEQUENCER STATUS Register (79H) and determine the completion status of the Sector Read. If the read was successful, then the microcontroller will typically program the CL-SH265 to transfer this sector from the buffer memory to the Host. If the read was not successful, the microcontroller may try to correct the data or attempt to re-read this sector.

4.3 Sector Write

The Sector Write function typically consists of two parts. The first is identical to the first part of the Sector Read, i.e., reading the Sector ID field. The same Sequencer routine should be used; the only difference is that after a successful Sector ID read, the next address should be the address of the Write Sector routine. This can usually be accomplished by changing the address in the BRANCH ADDRESS Register (78H) after a successful ID read.

After the sector has been positively identified, the second half of the Sector Write function is to transfer the data from the buffer memory to the disk, as explained above in the Write operation.

4.4 Format Sector

The Format Sector function consists of a Write operation that will write both the Sector ID field and the Sector Data field. This function is normally started with the Sequencer waiting for the INDEX pulse to branch into the Write operation routine. The microcontroller can update the Sector ID field information in the WCS, while the Sector Data field is being written on the disk. This allows a full-track format, with a minimum of microcontroller intervention.

The CL-SH265 allows the Sector Data field to be generated from the WCS instead of from the buffer memory, through the use of the SUPPRESS TRANSFER bit (Register 7AH, Bit 5).

4.5 Search Data

The Sector Read function can be modified into a Search Data function. When the second half of the Sector Read function is entered, the contents of the buffer memory will be compared, byte-for-byte, with the incoming data from the disk drive. This comparison of the DATA FIELD is enabled by setting the SEARCH OPERATION bit (Bit 4) of the OPERATION CONTROL/STATUS Register (7AH), and the COMPARE ENABLE bit (Bit 1) in the CONTROL FIELD of the WCS word, which starts the data transfer.

The result of this comparison is latched into the SEQUENCER STATUS Register (79H, Bits 0 and 1). Be sure to reset both the SEARCH OPERATION bit (Register 7AH, Bit 4) and the COMPARE ENABLE bit (CONTROL FIELD, Bit 1) after the completion of the Search Data function.

4.6 Verify Sector

By setting the SUPPRESS TRANSFER bit in the OPERATION CONTROL/STATUS Register, (7AH, Bit 5) and performing a Read Sector function, the incoming data will be verified for good ECC, but will not be transferred to the buffer memory.

4.7 Extended Data Handling

Variable Sector Size

The CL-SH265 has an eight-bit Sector Data field length counter, loadable from the COUNT FIELD of the WCS. The COUNT FIELD is programmable. By setting it to any value from 00H to FFH, any block length up to 256 bytes can be transferred. The value of the COUNT FIELD should be one less than the actual sector length. For sector sizes greater than 256 bytes, several different methods can be used.

The simplest approach is to use as many Sequencer words as required to implement the count for the data field.

The next approach uses the INHIBIT CARRY bit in the OPERATION CONTROL/STATUS Register (7AH, Bit 7). By setting the INHIBIT CARRY bit (Register 7AH, Bit 7), before the count of the WCS word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set has expired, the Sequencer will be inhibited from going onto the next WCS word, and another 256 bytes of data will be transferred. The INHIBIT CARRY bit (Register 7AH, Bit 7) will be automatically reset on the next carry of the word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set (underflow of the current control word's count field). By testing and setting this bit, additional counts of 256 byte segments may be transferred. For odd-sized data fields, initialize the COUNT FIELD with the remainder, and use the modulo-256 counter for the bulk of the counting. For example, for 532 bytes, start with a count of 19, and set the INHIBIT CARRY bit (Register 7AH, Bit 7) twice.

The final approach uses the COUNT FIELD and the INHIBIT CARRY bit (Register 7AH, Bit 7), as well as the SECTOR SIZE Register (4EH) to program how many 256-byte counts the INHIBIT CARRY bit (Register 7AH, Bit 7) should suppress. The number initialized in the SECTOR SIZE Register (4EH) should be one less than the number of multiples of 256-byte segments to be transferred. For example, for 532 bytes, start with the SECTOR SIZE Register (4EH) initialized to 01H, an initial count of 13H in the WCS COUNT FIELD, and set the INHIBIT CARRY bit (Register 7AH, Bit 7).

In addition to setting the INHIBIT CARRY bit from Register 7AH, it may be set directly under WCS control without local microprocessor intervention. From the WCS, the INHIBIT CARRY bit can be set whenever DATA TRANSFER is set, and bits 7,6,5 of the NEXT ADDRESS field equals 100.

Split Data Field Operations

For high density drives, it is desirable to have more embedded servo fields on a track to keep the head well-centered above the track. The Split Data Field operation allows the data field of a sector to be split into multiple sections, so that servo fields can be inserted in between, as needed. Split data field can also be used for flaw management.. The programmability of the CL-SH265 sequencer RAM provides flexible handling of split-data fields. This feature is enabled by setting the ENABLE SPLIT DATA FIELD bit in the Auxiliary Control Register 0 (Register 48H, Bit 7). When this bit is set, Bit 3 of the sequencer RAM control field is used as a PROCESS SPLIT bit to freeze or resume ECC computation. The PROCESS SPLIT bit is set identically in both disk read and disk write operations. The byte count of the split -data field is specified by the count field of the sequencer RAM. The sizes of servo fields between split data fields are also specified by the sequencer RAM count field.

At the beginning of a split-data field is a sync byte and an optional address mark. Only the address mark of the very first split-data field of a sector is included in the ECC computation. Within each split-data field, data and ECC computation are processed normally. At the end

a sector must be programmed as a normal data field, so that the ECC computation can be terminated for the sector. ECC correction procedures are identical to sectors with a single data field.

To freeze the ECC computation, the PROCESS SPLIT bit must be set in the WCS instruction word with the DATA TRANSFER bit set. If more than one WCS instruction word with the DATA TRANSFER bit set is used, the PROCESS SPLIT bit is set only in the last word with DATA TRANSFER bit set. To resume the ECC computation, the PROCESS SPLIT bit must be set twice. The first is in the WCS instruction word, when the READGATE or WRITEGATE is turned on. The second is in the WCS instruction word, right before the first instruction word with DATA TRANSFER bit set. To have a normal termination of ECC computation, the PROCESS SPLIT bit should not be set.

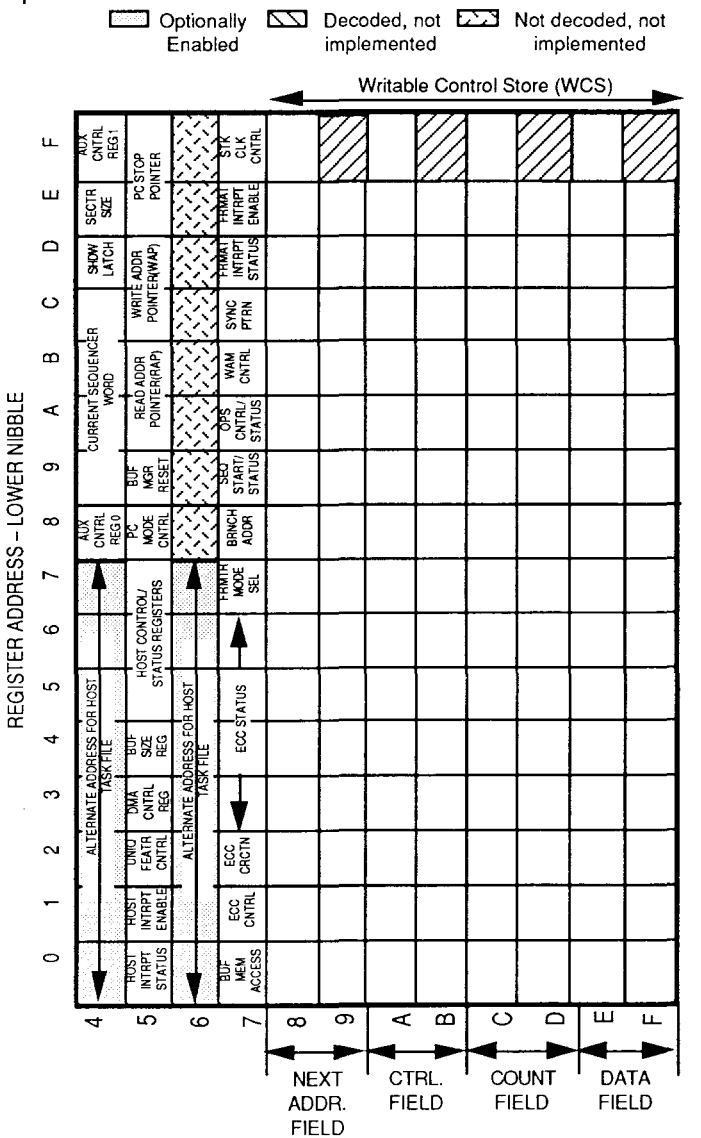
Multi-Sector Read/Write Operations

Multi-sector Read or Write operations can be accomplished by two methods. The simplest method is to load the next sector ID to be accessed, while the DATA TRANSFER STATUS bit (Register 79H, Bit 6) is set for the present sector, and to restart the Read or Write operation immediately after the end of the present sector.

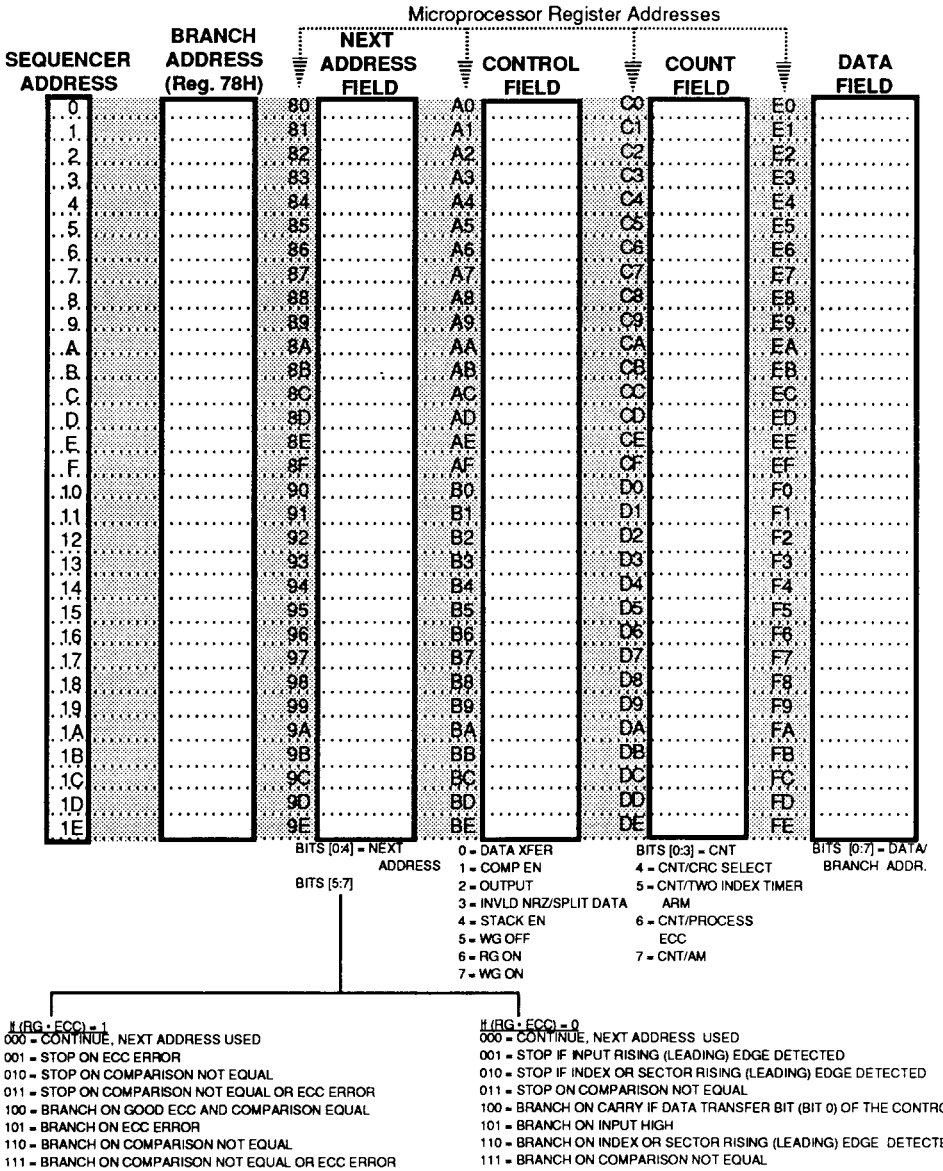
The next approach loads multiple ID field read subroutines and a single read/write data field subroutine into the thirty-one word WCS. The BRANCH ADDRESS (Register 78H) can then be used to jump between the subroutines.

5. REGISTER ADDRESSES

5.1 Memory Map



5.2 Writable Control Store (WCS) Worksheet



5.3 Register Initialization

REG #	HRESET (Pin 56)	RST* (Pin 36)	HOST PROGRAM RESET	WRITE REG 59H	REG 59H Bit 0=1	REG 71H Bit 5=1	REGISTER VALUE 7	6	5	4	3	2	1	0	NOTES
40/60							X	X	X	X	X	X	X	X	
41/61							X	X	X	X	X	X	X	X	
42/62							X	X	X	X	X	X	X	X	
42/62							X	X	X	X	X	X	X	X	
43/63							X	X	X	X	X	X	X	X	
44/64							X	X	X	X	X	X	X	X	
45/65							X	X	X	X	X	X	X	X	
46/66	+	+	+				0	0	0	0	0	0	0	0	
47/67							X	X	X	X	X	X	X	X	
48		+					0	0	0	0	0	0	0	0	(1)
49		+				+	0	0	0	1	1	1	1	1	
4A		+				+	0	0	0	0	0	0	0	0	
4B		+				+	0	0	0	0	0	0	0	0	
4C		+				+	0	0	0	0	0	0	0	0	
4D		+				+	0	0	0	0	0	0	0	0	
4E		+				+	0	0	0	0	0	0	0	0	
4F		+					1	1	0	0	0	X	X	X	
50		+					0	X	X	0	0	0	0	0	(1)
51		+					X	X	X	0	0	0	0	0	
52		+					0	0	0	0	0	0	0	0	(1)
53		+			+		X	X	0	0	0	0	X	X	
54		+					0	0	0	0	0	0	0	1	
55XT mode	+	+	+				0	0	0	0	0	0	0	0	(1)
56XT mode							X	X	X	X	X	X	X	X	
57XT mode	+		+				X	X	X	X	X	0	0	0	
55AT mode	+	+					1	0	0	0	0	0	0	0	(1)
56AT mode		+					X	X	X	0	0	0	0	0	
57AT mode		+					X	X	X	0	0	0	0	0	
58		+					0	1	0	1	1	0	0	0	
59		+					X	X	X	X	X	X	X	1	
5A		+		+	+		0	0	0	0	0	0	0	0	
5B		+		+	+		0	0	0	0	0	0	0	0	
5C		+		+	+		0	0	0	0	0	0	0	0	(2)
5D		+		+	+		0	0	0	0	0	0	0	0	(2)
5E		+		+	+		1	1	1	1	1	1	1	1	(3)
5F		+		+	+		0	0	0	0	0	0	0	1	(3)
70							X	X	X	X	X	X	X	X	
71		+					0	0	1	0	0	0	0	0	(1)
72		+				+	0	0	0	0	0	0	0	0	
73		+					1	1	1	1	1	1	1	1	
74		+					1	1	1	1	1	1	1	1	
75		+					1	1	1	1	1	1	1	1	
76		+					1	1	1	1	1	1	1	1	
77		+					0	0	0	0	0	0	0	0	
78		+				+	X	X	X	0	0	0	0	0	
79R		+				+	0	0	0	1	0	0	0	0	
7A		+				+	0	X	0	0	0	0	0	0	
7B		+					0	0	0	0	0	0	0	0	
7C		+					0	0	0	0	0	0	0	0	
7D		+					0	0	0	0	0	0	0	0	
7E		+					X	0	0	0	0	0	0	0	
7F		+					1	0	0	0	X	0	0	0	
80-9E							X	X	X	X	X	X	X	X	
A0-BE							X	X	X	X	X	X	X	X	
C0-DE							X	X	X	X	X	X	X	X	
E0-FE							X	X	X	X	X	X	X	X	

NOTE:

(1) This table only lists reset conditions that are common to all bits in each register. For reset conditions of individual bits in these registers, see the detail register descriptions in Sections 8 through 14.

(2) Reg 5C and 5D are also reset by AUTO COMMAND.

(3) Reg 5E and 5F are also set to 0FFH and 01H, respectively, by AUTO COMMAND.

6. XT HOST-ACCESSIBLE REGISTERS

The CL-SH265 supports the standard XT hardware/BIOS protocol plus has enhanced the interface by adding the ability to daisy chain two embedded drives. The XT Host transfers data to/from the disk controller through a combination of I/O ports and DMA data transfers. These registers can be accessed by the XT Host when the XT/AT SELECT bit (Bit 7) in the PC MODE CONTROL Register (58H) is set. There are three read ports and four write ports. The ports are as follows: Read/Write Data, Status, Programmed Reset, Drive Type, and DRV/DMA/IRQ Enable.

DACK*	HCS0*	A1	A0	IOR* = 0	IOW* = 0
0	1	x	x	Read Data	Write Data
1	0	0	0	Read Data	Write Data
1	0	0	1	Status	Program Reset
1	0	1	0	Drive Type	Select
1	0	1	1	Reserved	DRV/DMA/IRQ Enable

NOTE: x = Don't Care

6.1 Port 0 – Read Data (Read Only)

Data transferred from the disk controller to the XT Host comes from this register. Data is defined as sector bytes, configuration, and command completion information. This data is transferred by either Programmed I/O (PIO) or DMA. However, DMA data transfers may only occur if the disk controller is in the DATA phase. See the STATUS Register (Section 6.3).

6.2 Port 0 – Write Data (Write Only)

Data transferred from the XT Host to the disk controller goes through this write-only register. Data is defined as command, sector bytes, and configuration information. This data is transferred either by Programmed I/O (PIO) or DMA. However, DMA transfers may only occur if the disk controller is in the DATA phase. See the STATUS Register (Section 6.3).

6.3 Port 1 – Status (Read Only)

This register contains information regarding the present state of the disk controller. This read-only register contains the following bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	INTRQ	DMARQ	BUSY	C/D*	I/O*	REQ

6.3 Port 1 – Status (Read Only) *(cont.)*

Bit 0	**REQ:** When this bit is set, it indicates that the disk controller wants to send or receive a byte. The type and direction of transfer depends on the state of the disk controller which is defined by the C/D* and I/O* status bits. This bit is set and cleared for each byte transferred between the Host and the disk controller. This bit is valid, even if the data transfers are being done by DMA.
Bit 1	**I/O***: This bit determines the direction of transfer when the REQ bit (Bit 0) is set. See the following table.
Bit 2	**C/D***: This bit determines the type of information being transferred, either Command, Data, or Status. See the following table.
Bit 3	**BUSY**: This bit indicates that the disk controller is executing a command. When this bit is set, no new commands are accepted until the disk controller goes idle by resetting this bit. This bit is set during the Selection phase and should be reset at the end of the command.
Bit 4	**DMARQ**: This bit is set only during the data transfers between the Host and the disk controller, (i.e. C/D*=0, and REQ=1). In addition, the disk controller must be programmed to generate DMA transfers by setting the DMAEN bit (Bit 0) in the XT DRV/DMA/IRQ ENABLE Register. This bit is the direct image of the DREQ line on the Host bus interface. When this bit is set, it indicates that the CL–SH265 is ready for a DMA transfer. It is set for each byte transfer and cleared by the Host bus signal DACK* (Pin 52).
Bit 5	**INTRQ**: This bit indicates that an interrupt has been issued to the Host. This bit directly reflects the Host bus signal HINT (Pin 44). This bit is set during the Command Completion phase. During this phase, the completion status byte is available to the Host. In order for this bit to be set, the Host must set the IRQEN bit (Bit 1) in the XT DRV/DMA/IRQ ENABLE Register (57H) before the Command Completion phase. It may be cleared by the XT Host resetting the IRQEN bit (Bit 1) in the XT DRV/DMA/IRQ ENABLE Register, or by the XT Host writing to Port 1 (Host Programmed Reset), or by asserting the HOST RESET signal (HRESET—Pin 56).
Bits 6-7	— **RESERVED**. These bits will read 0.

BUSY	C/D*	I/O*	STATE OF DISK CONTROLLER	DIRECTION OF TRANSFER
0	x	x	IDLE	
1	0	0	DATA PHASE	PC to Disk Controller
1	0	1	DATA PHASE	Disk Controller to PC
1	1	0	COMMAND PHASE	PC to Disk Controller
1	1	1	STATUS PHASE	Disk Controller to PC

6.4 Port 1 – Reset (Write Only)

The XT Host may reset the disk controller at any time by writing to this register. This will immediately cause the disk controller to enter the idle state, if the disk controller is busy. See the section on register initialization (Section 5.3).

6.5 Port 2 – Drive Type (Read Only)

This register contains information used by the XT Host to identify the drive characteristics. Since the XT interface supports two drives, the bits in this register are divided into two separate drive types (drive 0 = bits 0-3, drive 1 = bits 4-7). The information contained in this register is written by the local microcontroller and is used by the XT Host BIOS driver program. The CL-SH265 does not interpret or use these bits in any respect.

6.6 Port 2 – Controller Select (Write Only)

Writing to this register starts the command process. When the disk controller is idle and the XT Host writes to this address, the BUSY bit (Port 1 - STATUS, Bit 3) is set and CL–SH265 enters the Command phase. Any data can be written to this register to cause the CL–SH265 to set the BUSY bit (Port 1 - STATUS, Bit 3). When the BUSY bit (Port 1 - STATUS, Bit 3) is set, a write to this port has no effect.

6.7 Port 3 – DRV/DMA/IRQ Enable (Write Only)

This register allows the Host to control both DMA transfers and interrupts to the Host plus, for the embedded two drive configuration (optional), control the selected drive through the DRV bit. This write only register can be loaded at any time. The DMA request Enable bit allows the disk controller to drive the Host DREQ signal during "DATA" phase transfers. The DREQ signal (Pin 51) is set and cleared on each data transfer forming an interlocked handshake. The DMAEN bit should be set right after the "Select" sequence and reset at the Command Completion phase. The IRQEN bit (Bit 1) in the XT DRV/DMA/IRQ ENABLE Register controls the enable for the XT Host signal HINT (Pin 44). When the IRQEN bit (XT DRV/DMA/IRQ ENABLE Register, Bit 1) is reset, no interrupts will be issued to the XT Host. When the IRQEN bit (XT DRV/DMA/IRQ ENABLE Register, Bit 1) is set, it allows the disk controller to interrupt the XT Host at the Command Completion phase. To reset the interrupt once it is set, the XT Host must reset the IRQEN bit (Bit 1) in the XT DRV/DMA/IRQ ENABLE Register, or write to Port 1 (Host Programmed Reset), or assert the HOST RESET signal (HRESET—Pin 56). The DRV/DMA/IRQ Enable register bit definition is shown below. Bits 3-7 are "don't care" bits, but it is recommended that these bits be set to logical zero.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	DRV	INTEN	DMAEN

NOTE: X = Don't Care

7. AT HOST-ACCESSIBLE REGISTERS

The CL–SH265 has on-chip registers for an AT Host to communicate with a hard disk controller. Register access is accomplished through Programmed I/O (PIO) or DMA (Read/Write Data only). These registers can be accessed by the AT Host when the XT/AT SELECT bit (Bit 7) in the PC MODE CONTROL Register (58H) is reset. All registers are eight bits, except the read/write data, which can be 8/16 bits. The table below shows the state of various signals for accessing these registers when Pin 48 is programmed as A9 or as HCS1*.

HCS1* MODE DISABLED (Register 52H, Bit 3 is reset; Pin 48 is A9)

DREQ	BUSY	HCS0*	A9	A2	A1	A0	IOR*	IOW*
1	0	0	0	0	0	0	Read Data	Write Data
x	0	0	0	0	0	1	Error Status	Write Precomp.
x	0	0	0	0	1	0	Sector Count	Sector Count
x	0	0	0	0	1	1	Sector Number	Sector Number
x	0	0	0	1	0	0	Cylinder Low	Cylinder Low
x	0	0	0	1	0	1	Cylinder High	Cylinder High
x	0	0	0	1	1	0	Drive/Head Number	Drive/Head Number
x	0	0	0	1	1	1	Contr./Drive Status	Command
0	1	0	0	x	x	x	Contr./Drive Status	Not Allowed
x	x	0	1	1	1	0	Alt. Contr./Dr. Status	Fixed Disk
x	x	0	1	1	1	1	Digital Input	Reserved

x = Don't Care

HCS1* MODE ENABLED (Register 52H, Bit 3 is set; Pin 48 is HCS1*)

DREQ	BUSY	HCS0*	HCS1*	A2	A1	A0	IOR*	IOW*
1	0	0	1	0	0	0	Read Data	Write Data
x	0	0	1	0	0	1	Error Status	Write Precomp.
x	0	0	1	0	1	0	Sector Count	Sector Count
x	0	0	1	0	1	1	Sector Number	Sector Number
x	0	0	1	1	0	0	Cylinder Low	Cylinder Low
x	0	0	1	1	0	1	Cylinder High	Cylinder High
x	0	0	1	1	1	0	Drive/Head Number	Drive/Head Number
x	0	0	1	1	1	1	Contr./Drive Status	Command
0	1	0	1	x	x	x	Contr./Drive Status	Not Allowed
x	x	1	0	1	1	0	Alt. Contr./Dr. Status	Fixed Disk
x	x	1	0	1	1	1	Digital Input	Reserved

x = Don't Care

7.1 AT Host Read Data (Read Only)

This register transfers sector and ECC data from the buffer memory to the AT Host. The register is 16 bits wide except when transferring Read ECC data, when it is eight bits. The AT Host may only access this register during data transfers in which the DREQ bit (Bit 3) is set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.2 AT Host Write Data (Write Only)

This register transfers sector and ECC data from the AT Host to the buffer memory. This register is 16 bits wide, except when transferring Write ECC data, when it is eight bits. The AT Host may only access this register during data transfers in which the DREQ bit (Bit 3) is set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.3 AT Host Error Status (Read Only)

The local microcontroller can write detailed error status of the last command failure to this register. This register can also be used to set disk controller diagnostic errors during the Diagnostic command or on power-up. When an error occurs, this register can be loaded by the microcontroller and the ERROR bit (Bit 0) is set in the AT HOST CONTROLLER/DRIVE STATUS Register. The Error bit is cleared whenever the Host writes to the Command register. This register may only be read by the AT Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

7.4 AT Host Write Precompensation (Write Only)

This register sets the boundary at which the disk controller will start precompensating the data written to the disk drive. The value in this register is the cylinder address divided by four. This register may only be written to by the AT Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

7.5 AT Host Sector Count (Read/Write)

This register specifies the number of sectors to be transferred during a Read/Write Sector command. This register is decremented by the microcontroller, as each sector is transferred. If this register is loaded with 0, then 256 sectors are transferred. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.6 AT Host Sector Number (Read/Write)

This register contains the starting sector number for the current Read/Write Sector command. This register is incremented by the microcontroller, as each sector is transferred between the AT Host and the disk controller. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.7 AT Host Cylinder Low (Read/Write)

This register contains the lower eight bits of the disk cylinder address. This register, in conjunction with the AT HOST CYLINDER HIGH Register, constitutes a 16-bit cylinder address. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.8 AT Host Cylinder High (Read/Write)

This register contains the upper eight bits of the disk cylinder address. This register, in conjunction with the AT HOST CYLINDER LOW Register, constitutes a 16-bit cylinder address. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

7.9 AT Host Drive/Head (Read/Write)

This register contains the sector size, drive and head number. This register may only be accessed when the BUSY bit (Bit 7) is not set in the AT HOST CONTROLLER/DRIVE STATUS Register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	SECTOR SIZE		DRV#	HEAD NUMBER			

Bit 7 should be set to 1. This register is reset when the RST* signal (Pin 36) is asserted low, or the HOST RESET signal (HRESET—Pin 56) is asserted. It is also reset when the RESET bit (AT HOST FIXED DISK Register, Bit 2) is set, or when a Diagnostic command (90H) is issued by the AT Host.

7.10 AT Host Controller/Drive Status (Read Only)

This register specifies the state of the disk controller/drive. This register may be accessed by the AT Host at any time; however, when the BUSY bit (Bit 7) is set, no other bits in the register are valid. Also by reading this register, any pending interrupts to the AT Host are cleared.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUSY	READY	FAULT	SKCOMPL	DREQ	CDATA	INDEX	ERROR

Bit 0	**ERROR**: This bit is set when an error occurred on the last command or power-up diagnostics. The Error bit is cleared whenever the Host writes to the Command register. The error code is stored in the AT HOST ERROR STATUS Register.
Bit 1	**INDEX**: This bit reflects the status of INDEX signal (Pin 34) from the selected disk drive. This signal is asserted once per revolution of the disk. This bit will never be set if the drive is not ready (i.e., if Bit 6 is reset).
Bit 2	**CDATA**: This bit is set whenever, on the previous read sector transfer, a sector read off the disk had a correctable ECC error which was corrected. The CDATA bit is cleared whenever the Host writes to the command register.
Bit 3	**DREQ**: This bit is set for data transfers to/from the sector buffer. This includes both sector and ECC data. The disk controller is considered "busy" whenever this bit or the BUSY bit (Bit 7) is set. When this bit is set, the AT Host may also read/write any of the AT-Host Registers, including the AT HOST COMMAND Register.
Bit 4	**SKCOMPL**: This bit indicates the state of the Seek Complete signal from the selected disk drive. This bit is set when the disk drive is not seeking.
Bit 5	**FAULT**: This bit reflects the state of the Write Fault signal from the selected disk drive. When this bit is set, it indicates that the disk drive is unsafe for read/write access.
Bit 6	**READY**: This bit reflects the state of the Ready signal from the selected disk drive. When this bit is set, the disk drive is present, but may not be ready for read/write transfers.
Bit 7	**BUSY**: When this bit is set, the disk controller is executing a command. Also, when this bit is set, the AT Host may not read or write any other registers except the AT HOST CONTROLLER/DRIVE STATUS Register, the AT HOST ALTERNATE CONTROLLER/DRIVE STATUS Register, the AT HOST FIXED DISK Register, and the AT HOST DIGITAL INPUT Register. This bit is set when the RST* signal (Pin 36) is asserted low, or the HOST RESET signal (HRESET—Pin 56) is asserted. It is also set when AT HOST FIXED DISK Register, Bit 2 is set or when the AT HOST COMMAND Register is loaded by the AT Host.

7.11 AT Host Command (Write Only)

The AT Host issues a new command to the disk controller through this register. The AT Host must ensure that the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is reset and all other registers must be set up prior to loading this register. The AT Host may abort the current data transfer and start a new command by writing to this register only when the DREQ bit (Bit 3) in the AT HOST CONTROLLER/DRIVE STATUS Register is set.

7.12 AT Host Alternate Controller/Drive Status (Read Only)

This register contains the same bit definition as the AT HOST CONTROLLER/DRIVE STATUS Register. This alternate register is used for systems that do not want to reset pending interrupts by reading the AT HOST CONTROLLER/DRIVE STATUS Register. This register may be read at any time.

7.13 AT Host Fixed Disk (Write Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	HD3EN	RESET	INTEN*	DMAEN

Bit 0	**DMAEN:** This bit is an extra feature which the CL-SH265 supports for the AT, that is not part of the generic AT interface. This feature allows a DMA channel to be multiplexed between multiple peripherals directly by the AT Host, without local microcontroller intervention. To enable this feature, first the AT HOST FIXED DISK REGISTER DMAENB bit (Register 52H, Bit 4) must be set; and second, the DMA SELECT must be reset (Register 58H, Bit 3). With these two control bits initialized, this bit controls the enabling of the DMA channel.
Bit 1	**INTEN***: When this bit is reset to logical 0, it enables the HINT (HOST INTERRUPT—Pin 44) output. When this bit is set to logical 1, the HINT (HOST INTERRUPT—Pin 44) output is tri-stated, regardless of the presence or absence of a pending interrupt. The value of this bit is determined by reading Bit 1 of Register 55H. The internal signal and the status will still be valid even when re-enabling the output.
Bit 2	**RESET**: The AT Host interface will be held in the Reset condition when this bit is set. If two disk drives are daisy chained, the AT Host interface on both disk drives will be reset. See the section on register initialization (Section 5.3).
Bit 3	**HEAD SELECT 3 ENABLE**: This bit selects whether the status of HEAD SELECT 3 (Register 46H/66H, Bit 3) or the status of RWC0 or RWC1 (depending on the drive selected) (Register 56H/57H, Bit 3) is returned as Bit 5 of the AT HOST DIGITAL INPUT Register. This bit can be overridden by Register 56H/57H, Bit 4. In that case, the CL-SH265 always shows the status of HEAD SELECT 3.
Bits 4-7	**Don't Care Bits**, but it is recommended that the user program these bits to logical zero.

7.14 AT Host Digital Input (Read Only)

This register is a diagnostic loopback register that indicates the present state of Disk Drive Select 0/1, Head Select 0 - 2, Head Select 3/Reduced Write Current, and the WRITE GATE signal (Pin 38). The AT Host may read this register at any time. The bits in this register are negative true.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HiZ	WGATE*	H3*/RWC*	H2*	H1*	H0*	DS1*	DS0*

NOTE: HiZ denotes high impedance

Bits 0-1 **DS0*, DS1***: These two bits are Disk Drive Select 0/1. They will always be the complement of each other. The state of these bits is defined by the AT HOST DRIVE/HEAD Register, Bit 4. The relationship between these bits is shown in the following table:

AT HOST DRIVE/ HEAD REGISTER Bit 4	DS0*	DS1*
0	0	1
1	1	0

Bits 2-4 **H0*, H1*, H2***: These bits reflect the complement of the Head Number Bits (0-2) in the AT HOST DRIVE/HEAD Register.

Bit 5 **H3*/RWC***: This bit reflects either Head Number 3 (Bit 3 of the AT HOST DRIVE/HEAD Register) or Reduced Write Current (Bit 3 of the AT DRIVE 0/1 CONTROL/STATUS Registers (56H/57H)). If Bit 3 of the AT HOST FIXED DISK Register, or Bit 4 of the AT DRIVE 0/1 CONTROL/STATUS Registers (56H/57H) is set then this bit reflects the complement of the AT HOST DRIVE/HEAD Register, Bit 3. Otherwise, this bit reflects the complement of Bit 3 of the AT DRIVE 0/1 CONTROL/STATUS Registers.

Bit 6 **WRITE GATE***: This bit reflects the complement of the WRITE GATE signal (Pin 38).

Bit 7 **RESERVED**. Tri-state at the data pin, when read.

8. BUFFER MANAGER AND PC REGISTERS

8.1 50H – Host Interrupt Status (Read Only)

This register, except Bit 7, is reset when the HOST RESET signal (HRESET—Pin 56) is asserted, when the RST* signal (Pin 36) is asserted low, or by a Host Programmed Reset. Bit 4 of this register is reset by the RST* signal (Pin 36) if the HOST RESET signal (HRESET—Pin 56) is not asserted and the Host Programmed Reset is not set. All bits, except Bit 7, are reset by a read of this register.

Bit 0	**HOST TRANSFER DONE**: When this bit is set, it indicates completion of a Host transfer (the PC STOP POINTER (Registers 5EH and 5FH) is equal to the appropriate Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH)). After this bit is set, the appropriate Address Pointer will read one byte more than the value of the PC STOP POINTER (Registers 5EH and 5FH). This bit is reset when the Host writes to the Command register. In the MASTER/SLAVE mode, this bit is only reset by a write to the Command register, if the DRV SELECT bit matches the MASTER/SLAVE SELECT configuration. This bit is the same as Register 53H, Bit 5.
Bit 1	**PC TRANSFER OVERRUN/UNDERRUN DETECTED**: When this bit is set, it indicates that a data transfer between the Host and the buffer memory did not function properly. This bit is set when the IOCHRDY* signal (Pin 50) is asserted low, and the rising (trailing) edge of the IOW* signal (Pin 55) or the IOR* signal (Pin 53) was detected. This bit is reset when the Host writes to the Command register.
Bit 2	**PC SELECTION PHASE DETECTED**: In the PC XT mode, this bit is set when the Host writes to Port 2. In PC AT mode, this bit is set when the Host writes to the AT COMMAND Register (47H/67H).
Bit 3	**AT STATUS READ DETECTED:** In AT mode, this bit is set if the Host reads the Primary Controller/Drive Status register (1F7H or 177H) the first time after data transfers between the Host and the FIFO have completed. It is not set if the Host reads the Alternate Controller/Drive Status register (3F6H). Besides the reset conditions described above, it is also reset when the Host writes to the Command register.
Bit 4	**PC RESET DETECTED**: This bit is set by assertion of the HOST RESET signal (HRESET—Pin 56) or a Host Programmed Reset, i.e., when the XT Host writes to Port 1 or the AT Host sets the RESET bit (AT HOST FIXED DISK Register, Bit 2). It remains set for the duration of the Host Reset condition.
Bit 5	**RESERVED**.
Bit 6	**RESERVED**.
Bit 7	**INTERRUPT STATUS REGISTER SET**: This bit is the logical OR of Bits 0-6 in the FORMATTER INTERRUPT STATUS Register (7DH).

8.2 51H - Host Interrupt Enable (Read/Write)

This register is reset only when the RST* signal (Pin 36) is asserted low.

Bit 0	**HOST TRANSFER DONE ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low ,when the HOST TRANSFER DONE bit (Register 50H, Bit 0 and Register 53H, Bit 5) is set.
Bit 1	**PC TRANSFER OVERRUN ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low, when the PC TRANSFER OVERRUN/UNDERRUN DETECTED bit (Register 50H, Bit 1) is set.
Bit 2	**PC SELECTION PHASE ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low, when the PC SELECTION PHASE DETECTED bit (Register 50H, Bit 2) is set.
Bit 3	**AT STATUS READ DETECTED ENABLE:** When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low, when the AT STATUS READ DETECTED bit (Register 50H, Bit 3) is set.
Bit 4	**PC RESET ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low, when the PC RESET DETECTED bit (Register 50H, Bit 4) is set.
Bit 5	**RESERVED**.
Bit 6	**RESERVED**.
Bit 7	**RESERVED**.

8.3 52H – Unique Features Control/Status (Read/Write)

This register is reset only when the RST* signal (Pin 36) is asserted low.

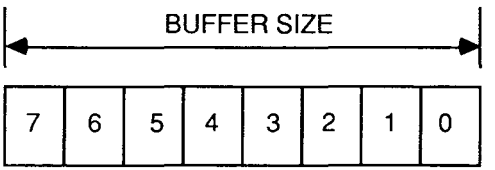
Bit 0	**MOE* DISABLE**: When this bit is set to logical 1, the MOE* signal (Pin 17) is disabled from being asserted low. This is intended to support reading switch settings (via Register 70H) on the buffer memory data bus.
Bit 1	**MASTER/SLAVE MODE ENABLE**: When this bit is set, it enables the ability to daisy chain two separate XT or AT interfaces together, one configured as MASTER and the other as SLAVE.
Bit 2	**MASTER/SLAVE SELECT:** With Register 52H, Bit 1 set then this bit configures the CL-SH265 as MASTER or SLAVE. When this bit is reset the CL-SH265 is configured as MASTER, and when set, the CL-SH265 is configured as SLAVE. MASTER responds to drive 0 select, and the SLAVE responds to drive 1 select. For AT, on a Diagnostic Command, both the MASTER and SLAVE respond, but only the MASTER is enabled to report status to the Host.
Bit 3	**HCS1 MODE ENABLE**: This bit is valid in the PC AT mode only (i.e., Register 58H, Bit 7 is reset). When this bit is set, Pin 48 is HCS1* input. When this bit is reset, Pin 48 is PC ADDRESS LINE 9.
Bit 4	**AT HOST FIXED DISK REGISTER DMAENB**: This bit is valid only in the PC AT mode, and when the DMA mode is enabled (i.e. Register 58H, Bits 3 and 7 are reset). When this bit is set, it allows Bit 0 of the AT HOST FIXED DISK Register to control the enabling of the DMA channel. This bit should be set prior to enabling the DMA mode (Register 58H, Bit 3).
Bit 5	**AT DMAEN**: This bit reflects Bit 0 of AT HOST FIXED DISK Register. (Read Only)
Bit 6	**DISABLE STOP POINTER COMPARE**: When this bit is set, it disables the comparison of the PC STOP POINTER (Registers 5EH and 5FH), until Register 5FH is loaded.
Bit 7	**TEST MODE ENABLE**: This bit is reserved for test purposes. The user must program this bit to a logical zero.

8.4 53H – DMA Control (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low, or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset by HRESET or HOST PROGRAM RESET.

Bit 0	**RESERVED.**
Bit 1	**RESERVED.**
Bit 2	**HOST WRITE ENABLE**: Setting this bit will start transfer from the Host to the buffer memory. In addition, the ROP/WOP* bit (Bit 4) must be reset to logical 0 when this bit is set. This bit is also reset by HRESET or HOST PROGRAM RESET. It is set when an auto command is received.
Bit 3	**HOST READ ENABLE**: Setting this bit will start transfer from the buffer memory to the Host. In addition, the ROP/WOP* bit (Bit 4) must be set to logical 1, when this bit is set. This bit is also reset by HRESET, HOST PROGRAM RESET, or a Host command.
Bit 4	**ROP/WOP***: Set this bit to logical 1 for a Disk Read operation. This will cause data transfer from the disk to the buffer memory. With the HOST READ ENABLE bit (Bit 3) set, data is transferred from the buffer memory to the Host. Reset this bit to logical 0 for a Disk Write operation. This will cause data transfer from the buffer memory to the disk. With the HOST WRITE ENABLE bit (Bit 2) set, data is transferred from the Host to the buffer memory. This bit is also reset when an auto command is received.
Bit 5	**HOST TRANSFER DONE**: When this bit is set, it indicates completion of a Host transfer (the PC STOP POINTER (Registers 5EH and 5FH) is equal to the appropriate Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH)). After this bit is set, the appropriate Address Pointer will read one byte more than the value of the PC STOP POINTER (Registers 5EH and 5FH). This bit is the same as Register 50H, Bit 0. (Read Only). In MASTER/SLAVE mode, a write to the AT HOST COMMAND Register only resets this bit if the DRV SELECT bit corresponds to the MASTER or SLAVE configuration bit. This bit is also reset by HRESET, HOST PROGRAM RESET, or WRITE REG 59H.
Bit 6	**RESERVED.**
Bit 7	**RESERVED.**

8.5 54H – Buffer Size (Read/Write)



0	0	0	0	0	0	0	X	=	512 BYTES
0	0	0	0	0	0	1	X	=	1K BYTES
0	0	0	0	0	1	1	X	=	2K BYTES
0	0	0	0	1	1	1	X	=	4K BYTES
0	0	0	1	1	1	1	X	=	8K BYTES
0	0	1	1	1	1	1	X	=	16K BYTES
0	1	1	1	1	1	1	X	=	32K BYTES
1	1	1	1	1	1	1	X	=	64K BYTES

Bit 0 **ENABLE AUTO INTERRUPT RESET:** This bit, when set, enables the automatic reset of the HOST INTERRUPT SIGNAL HINT* (Pin 44), after data transfer with the Host. When reset, the HOST INTERRUPT SIGNAL HINT* (Pin 44) is not reset after data transfers with the Host. This bit is set by assertion of RST* (Pin 32).

Bits 1-7 This register specifies the size of the physical buffer memory (in bytes) where the codes for a given buffer size are in the table above. The upper byte of the PC STOP POINTER (Register 5FH) is bit compared with the upper byte of the appropriate Host Address Pointer (the WRITE ADDRESS POINTER — WAP (Registers 5CH and 5DH), or the READ ADDRESS POINTER — RAP (Registers 5AH and 5BH)). The result of the bit compare is logically 'ANDed' with the contents of this register. Bit locations that are zero in this register have the bit-compare results masked. After the bit-compare masking, when the PC STOP POINTER (Registers 5EH and 5FH) equals the appropriate Host Address Pointer (the WRITE ADDRESS POINTER — WAP (Registers 5CH and 5DH), or the READ ADDRESS POINTER — RAP (Registers 5AH and 5BH)), the DMA transfer is terminated and the WAP or the RAP will be pointing to one byte higher than the PC STOP POINTER (Registers 5EH and 5FH). The HOST TRANSFER DONE bit (Register 50H, Bit 0 and Register 53H, Bit 5) will be set. The Buffer Size/Segment Address register of the CL-SH265 can operate in two modes. In the first mode, the value stored in this register represents the maximum external Static RAM size to be controlled by the CL-SH265. For example, if a 32K buffer is attached, then this register is loaded with 7FH. The RAP and WAP pointers accesses the buffer using BA0-14. When the RAP or WAP reaches 7FFFH, on the next access, the pointer will roll over to 0000H. BA15 will always be zero in this example. In the second mode, this register specifies a buffer segmentation size. The smallest segment size is 4K. For example, with an attached buffer size of 32K and segment sizes of 4K, this register would be loaded with 0FH. This would create 8 4K segments 0000-0FFFH,1000-1FFFH, 2000-2FFFH, 3000-3FFFH, 4000-4FFFH, 5000-5FFFH, 6000-6FFFH, 7000-7FFFH. Each segment may be accessed by setting the upper 4 bits of the WAP and RAP to the desired segment address. In this configuration, once the address pointer reaches XFFFH, the next address will roll over to X000H. Note that for an AT interface Auto Command sequence, the WAP pointer will be set to 0000H, regardless of the previous segment address. These seven bits are reset by assertion of RST* (Pin 32).

8.6 58H – PC Mode Control (Read/Write)

This register is initialized only when the RST* signal (Pin 36) is asserted low.

Bits 0-1	**PC WAIT STATE**: These bits specify the number of buffer memory cycles for which the IOCHRDY* signal (Pin 50) will be asserted low for Programmed I/O (PIO) transfers. These bits are reset when the RST* signal (Pin 36) is asserted low. 00 = No buffer memory cycles (Disables any Wait states). 01 = 1-2 Buffer memory cycles. 10 = 2-3 Buffer memory cycles. 11 = 3-4 Buffer memory cycles.
Bit 2	**AUTO WAIT STATE GENERATION ENABLE**: When this bit is set, the IOCHRDY* signal (Pin 50) is asserted low to introduce Wait states automatically, for Programmed I/O (PIO) transfers between the Host and the buffer memory when the CL-SH265 is not ready to transfer data. These Wait states are in addition to the programmed number of Wait states specified by Bits 0-1. This bit is reset when the RST* signal (Pin 36) is asserted low.
Bit 3	**PIO/DMA SELECT**: (PC AT mode only) This bit is set when the RST* signal (Pin 36) is asserted low. When this bit is set, Programmed I/O (PIO) mode is selected. When in the AT DMA mode (this bit is reset), by setting the AT HOST FIXED DISK REGISTER DMAENB bit (Register 52H, Bit 4), the PC can directly control the enabling of the DMA channel through Bit 0 of the AT HOST FIXED DISK Register (the local microcontroller can monitor this bit through the AT DMAEN bit — Bit 5 of Register 52H). Also, in the AT DMA mode (this bit is reset), the Host can respond to a DREQ (DMA REQUEST) with either DACK* (DMA ACKNOWLEDGE) or a Programmed I/O Host data access.
Bit 4	**ENABLE AUTO INTERRUPT**: (PC AT mode only) This bit is set when the RST* signal (Pin 36) is asserted low. When this bit is set, the CL–SH265 generates an interrupt to the Host, when the local microcontroller initiates a Host data transfer. This is done by setting either the HOST WRITE ENABLE bit (Bit 2) or the HOST READ ENABLE bit (Bit 3) in the DMA CONTROL Register (53H); if these bits are set, it is done by writing to Register 5FH.
Bit 5	**DISABLE AUTO COMMAND EXECUTION**: (PC AT mode only) When this bit is set, it disables the automatic execution of Write, Write Long, Write Buffer, and Format commands. This bit is reset when the RST* signal (Pin 36) is asserted low.
Bit 6	**8/16 BIT DATA**: (PC AT mode only) When this bit is set, it selects 16-bit data transfer to/from the Host. This bit is set when the RST* signal (Pin 36) is asserted low.
Bit 7	**XT/AT SELECT**: This bit controls which Host interface is active, XT or AT. When this bit is set, the PC XT mode is selected. This bit is reset when the RST* signal (Pin 36) is asserted low.

8.7 59H – Buffer Manager/PC Reset Control (Read/Write)

Any write to this register resets the READ ADDRESS POINTER (RAP) and the WRITE ADDRESS POINTER (WAP) Registers (5AH-5DH) and sets the PC STOP POINTER (Registers 5EH and 5FH) to a 01FFH. **CAUTION: Any write to this register also resets the PC interface operation. Bit 0 must be reset to execute PC AT Auto commands.**

Bit 0	**RESET**: When this bit is set, all registers associated with Buffer Manager and Host functions are held in the reset state until this bit is reset. This bit will also be set when the RST* signal (Pin 36) is asserted low.
Bits 1-7	**RESERVED.**

8.8 5AH – Read Address Pointer [0:7] [RAPL] (Read/Write)

Bits 0-7	These bits are the low-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set.

8.9 5BH – Read Address Pointer [8:15] [RAPH] (Read/Write)

Bits 0-7	These bits are the high-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set.

8.10 5CH – Write Address Pointer [0:7] [WAPL] (Read/Write)

Bits 0-7	These bits are the low-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset when one of the Auto commands is issued.

8.11 5DH – Write Address Pointer [8:15] [WAPH] (Read/Write)

Bits 0-7	These bits are the high-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also reset when one of the auto commands is issued.

8.12 5EH – PC Stop Pointer [0:7] [PC-SPL] (Read/Write)

Bits 0-7 These bits are the low-order byte of the PC Stop Pointer. It is used to detect the end of the Host data transfer. It is compared with the READ or WRITE ADDRESS POINTER (RAPL/WAPL) (Register 5AH or 5CH). This register is set when the RST* signal (Pin 36) is asserted low, when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also set to FFH when one of the Auto commands is issued.

8.13 5FH – PC Stop Pointer [8:15] [PC-SPH] (Read/Write)

Bits 0-7 These bits are the high-order byte of the PC Stop Pointer. It is used to detect the end of the Host data transfer. It is compared with the READ or WRITE ADDRESS POINTER (RAPH/WAPH) (Register 5BH or 5DH) masked by the contents of the BUFFER SIZE Register (54H). When they are equal, the HOST TRANSFER DONE bit (Register 53H, Bit 5, Register 50H, Bit 0) is set and the transfer is halted. If a new value is programmed in this register, a new transfer cycle will begin again if the appropriate HOST READ ENABLE bit (Register 53H, Bit 3) or HOST WRITE ENABLE bit (Register 53H, Bit 2) is still set. If the HOST READ ENABLE bit (Bit 3) or the HOST WRITE ENABLE bit (Bit 2) in Register 53H is set, a microcontroller write to this register restarts the PC data transfer. This register is set to 01H when the RST* signal (Pin 36) is asserted low, or when the microcontroller writes to the BUFFER MANAGER/PC RESET CONTROL Register (59H), or when the RESET bit (Register 59H, Bit 0) is set. This register is also set to 01H when one of the Auto commands is issued.

9. FORMATTER REGISTERS

9.1 4EH – Sector Size (Read/Write)

Bits 0-7 Writing to this register sets the number of 256-byte data blocks to be transferred by the Disk Formatter, when the INHIBIT CARRY bit (Register 7AH, Bit 7) is used. The value programmed, should be one less than the number of underflows of the Current Sequencer Word [COUNT FIELD] that will be inhibited. With this register set to 00H and the INHIBIT CARRY bit (Register 7AH, Bit 7) set, only one underflow of the Current Sequencer Word will be inhibited. For a 532-byte Sector Data field, set the COUNT FIELD of the Writable Control Store (WCS) to 13H, set the SECTOR SIZE (Register 4EH) to 01H, and set the INHIBIT CARRY bit (Register 7AH, Bit 7).

For a 4096-byte Sector Data field, set the COUNT FIELD of the Writable Control Store (WCS) to FFH, set the SECTOR SIZE (Register 4EH) to 0EH, and set the INHIBIT CARRY bit (Register 7AH, Bit 7). This register is reset when the RST* signal (Pin 36) is asserted low..

9.2 71H – ECC Control (Read/Write)

This register, except Bit 5, is reset when RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.

Bit 0	**ECC SYNDROME REVERSAL/CORRECTION CONTROL**: Setting this bit will select the correction operation. Resetting this bit will select the ECC Syndrome Reversal function. To start any of these functions, the ECC SHIFT CONTROL bit (Bit 1) should be set.
Bit 1	**ECC SHIFT CONTROL**: Setting this bit starts the function selected in ECC SYNDROME REVERSAL/CORRECTION CONTROL (Bit 0). If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Bit 0) is reset, setting this bit will start shifting data from the ECC CORRECTION SHIFT-REGISTER/COUNTER (Register 72H) into the ECC circuit. This bit is cleared automatically after the shift is completed. If the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Bit 0) is set, the correction function is selected, and setting this bit will start the correction process. In this case, this bit is cleared if a correctable error is found, or the ECC circuit is shifted 256 bytes. ECC CORRECTION SHIFT REGISTER/COUNTER (Register 72H) is a byte counter and, in case of a correctable error, will provide the error offset. Note that all shifts are performed on byte boundaries. During normal Read/Write operations, this bit should be set to zero.
Bit 2	**DISABLE ECC FEEDBACK:** When this bit is set, the ECC circuit functions as a 56/32-bit shift register.
Bit 3	**CLEAR ECC**: ECC syndrome will be cleared when this bit is set and no Read or Write operation is in progress. If this bit is set during a Read or Write operation, the ECC syndrome will be cleared at the end of that operation.
Bit 4	**ENABLE SECTOR BRANCH**: When this bit is set, it enables the SECTOR signal (Pin 35) input as a condition for Sequencer branching, along with the INDEX signal (Pin 34) input so that Sequencer branches may begin at INDEX or SECTOR.
Bit 5	**FORMATTER RESET**: When the RST* signal (Pin 36) is asserted low, it sets this bit and generates a hardware reset condition. When set by the microcontroller, a software reset condition is generated. Either reset stops all operations in the Disk Formatter. The software reset condition resets Registers 49H-4DH, 71H-76H, 78H-7AH, 7DH-7EH, deasserts the READ GATE signal (37), the WRITE GATE signal (Pin 38) and switches the NRZ signal (Pin 40), the WAM*/AMD*/SECTOR signal (Pin 35), and AD0-AD7 lines (Pins 24-31) to a high-impedance state. The Disk Formatter will remain in the reset condition as long as this bit is set. The reset condition can be removed by resetting this bit. Refer to the section on register initialization (Section 5.3). **Note: This bit should be reset immediately after power-up because most register bit values and CL-SH265 functions are inhibited when this bit is set.**
Bit 6	**32/56 BIT ECC SELECT**: When this bit is set, the 56-bit ECC polynomial is selected. When this bit is reset, the 32-bit ECC polynomial is selected.
Bit 7	**ECC POLYNOMIAL DIRECTION**: When this bit is reset, it selects the forward poly nomial. When this bit is set, it selects the reverse polynomial for the correction process.

9.3 72H – ECC Correction Shift-Register/Counter (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.

Bits 0-7	When the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Register 71H, Bit 0) is set, this is an eight-bit counter. When the ECC SYNDROME REVERSAL/-CORRECTION CONTROL bit (Register 71H, Bit 0) is reset, this is a shift register.

9.4 73H – ECC Status [31:24]/[7:0] (Read Only)

This register is set when the RST* signal (Pin 36) is asserted or when Register 4FH, Bit 5 is reset, and Register 71H, Bit 5 is set. It is reset when Register 4FH, Bit 5 is set and Register 71H, Bit 5 is set.

Bits 0-7	**ECC STATUS BITS [31:24]/[7:0]**: When 56-bit ECC is selected, these are ECC Bits 31:24 (Bit 0 = ECC Bit 31). When 32-bit ECC is selected, these are ECC Bits 7:0 (Bit 0 = ECC Bit 7). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low . When the FORMATTER RESET bit (Register 71H, Bit 5) is set, this register is set, if the ECC PRESET CONTROL is reset; this register is reset if the ECC PRESET CONTROL is set.

9.5 REGISTER 73H – Auto Command "Lock" Release (Write Only)

Bits 0-7	**AUTO COMMAND "LOCK" RELEASE:** When the Host issues a command, the CL-SH265 locks or disables functions within the chip from being accessed by the local microcontroller or formatter section. The areas affected are: 1) Buffer manager registers (53H, 5CH-5FH, 70H); 2) Buffer to formatter data transfer mechanism; and 3) power-down control bit (48H, Bit 1). Items 1 and 2 are locked only during a PC AT "auto command". Item 3 is locked for all commands in both PC AT or PC XT modes. A write to Register 73H will enable or unlock these functions.

9.6 74H – ECC Status [39:32]/[15:8] (Read Only)

This register is set when the RST* signal (Pin 36) is asserted or when Register 4FH, Bit 5 is reset, and Register 71H, Bit 5 is set. It is reset when Register 4FH, Bit 5 is set and Register 71H, Bit 5 is set.

Bits 0-7	**ECC STATUS BITS [39:32]/[15:8]**: When 56-bit ECC is selected, these are ECC Bits 39:32 (Bit 0 = ECC Bit 39). When 32-bit ECC is selected, these are ECC Bits 15:8 (Bit 0 = ECC Bit 15). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low. When the FORMATTER RESET bit (Register 71H, Bit 5) is set, this register is set, if the ECC PRESET CONTROL is reset; this register is reset if the ECC PRESET CONTROL is set.

9.7 75H – ECC Status [47:40]/[23:16] (Read Only)

This register is set when the RST* signal (Pin 36) is asserted or when Register 4FH, Bit 5 is reset, and Register 71H, Bit 5 is set. It is reset when Register 4FH, Bit 5 is set and Register 71H, Bit 5 is set.

Bits 0-7	**ECC STATUS BITS [47:40]/[23:16]**: When 56-bit ECC is selected, these are ECC Bits 47:40 (Bit 0 = ECC Bit 47). When 32-bit ECC is selected, these are ECC Bits 23:16 (Bit 0 = ECC Bit 23). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low. When the FORMATTER RESET bit (Register 71H, Bit 5) is set, this register is set, if the ECC PRESET CONTROL is reset; this register is reset if the ECC PRESET CONTROL is set.

9.8 76H – ECC Status [55:48]/[31:24] (Read Only)

This register is set when the RST* signal (Pin 36) is asserted or when Register 4FH, Bit 5 is reset, and Register 71H, Bit 5 is set. It is reset when Register 4FH, Bit 5 is set and Register 71H, Bit 5 is set.

Bits 0-7	**ECC STATUS BITS [55:48]/[31:24]**: When 56-bit ECC is selected, these are ECC Bits 55:48 (Bit 0 = ECC Bit 55). When 32-bit ECC is selected, these are ECC Bits 31:24 (Bit 0 = ECC Bit 31). The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 36) is asserted low. When the FORMATTER RESET bit (Register 71H, Bit 5) is set, this register is set, if the ECC PRESET CONTROL is reset; this register is reset if the ECC PRESET CONTROL is set.

9.9 77H – Formatter Mode Selection (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**HOST STATUS READ DETECTED**: When this bit is set, it indicates that the CL-SH265 has detected a read of the AT HOST CONTROLLER/DRIVE STATUS Register by the Host since the last time this bit was polled. This bit is cleared by a read from the local microcontroller. This bit is reset only by a power-on Reset condition on the RST* signal (Pin 36).
Bit 1	**HOST REGISTER FILE ACCESS ENABLE**: When this bit is set, it allows the Host Interface Registers to be accessed by the local microcontroller. The address space is specified by bit 2. When this bit is reset, addresses 40H - 47H and 60H - 67H are available for external system use.
Bit 2	**HOST REGISTER FILE DECODE SELECT**: When this bit is set (and Bit 1 is set), the address space for the Host register file is 40H-47H (Addresses 60H - 67H are available for external system use). When this bit is reset (and Bit 1 is set), the address space for the Host register file is 60H-67H (Addresses 40H - 47H are available for external system use).

Microcontroller-Host Register File Decode Table

Reg. 77H Bit 1	Bit 2	CL–SH265 Decodes:	Available to MPU:
0	x	Neither	40H–47H and 60H–67H
1	1	Decodes 40H-47H	60H-67H
1	0	Decodes 60H–67H	40H-47H

9.9 77H – Formatter Mode Selection (Read/Write) *(cont.)*

Bit 3	**LOCAL INT* ENABLE**: When this bit is set to logical 1, it enables local interrupt capability. The individual sources of interrupt can still be disabled by the Interrupt Enable Registers (Registers 51H and 7EH).
Bit 4	**LOCAL INT* PIN PULLUP DISABLE**: When this bit is set to logical 1, it disables the pull-up on the INT* signal (Pin 19), leaving an open drain output. This is intended to support multiple interrupt sources.
Bit 5	**PROGRAMMED CONTROL INDEX**: When this bit is set, it simulates an active index condition. This bit can be used in place of the INDEX signal (Pin 34).
Bit 6	**SEQUENCER OUTPUT ENABLE:** When this bit is set, the INPUT/OUTPUT signal (Pin 33) is configured as an output. The value actually driven on the pin will be specified by the Current Sequencer Word CONTROL FIELD, Bit 2.
Bit 7	**HARD/SOFT* SECTOR MODE CONTROL**: When this bit is set to logical 1, it selects the Hard Sector mode. In this mode, the WAM*/AMD*/SECTOR signal (Pin 35) functions as a SECTOR input signal. The SECTOR PAST bit (Register 7AH, Bit 1) and Branch on Sector circuit will be triggered by the rising (leading) edge of the SECTOR signal. When this bit is reset to logical 0, it selects the Soft Sector mode. In this mode, the WAM*/AMD*/SECTOR signal (Pin 35) functions as the WAM*/AMD* signal.

9.10 78H – Next Sequencer Address (Read Only)

Bits 0-4	**NEXT ACTIVE SEQUENCER ADDRESS**: Bits 0-4 provide the next Writable Control Store (WCS) address to be executed by the Sequencer. This address could be the contents of the SEQUENCER START ADDRESS Register (79H), or the BRANCH ADDRESS Register (78H), or the CURRENT SEQUENCER WORD — NEXT ADDRESS Register (49H), or the CURRENT SEQUENCER WORD — DATA Register (4CH). This register is set to 01FH when the RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.
Bits 5-7	**RESERVED.**

9.11 78H – Branch Address (Write Only)

Bits 0-4	The Sequencer will jump to the address specified in Bits 0-4 if Register 48H, Bit 5, (WCS DATA FIELD BRANCH ENABLE bit) is reset, and a branch condition is programmed and met. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.
Bits 5-7	**RESERVED.**

9.12 79H – Sequencer Status (Read Only)

Bit 0	**COMPARE EQUAL**: This bit is set when the result of the compare operation is equal. The comparison is done between the Read Data and either the Buffer Memory Data or the Writable Control Store (WCS) DATA FIELD (determined by the SEARCH OPERATION bit – Register 7AH, Bit 4), on all bytes where comparison was enabled in the COMPARE ENABLE bit (Bit 1) of the Writable Control Store (WCS) CONTROL FIELD. COMPARE EQUAL is not valid until the Sequencer is in the ECC FIELD. This bit is reset when RST* is low or when Register 71H, Bit 5 is set.
Bit 1	**COMPARE LOW**: This bit is the same as Bit 0 above; however, this bit is set when the Read Data is lower than the other comparison source data. This bit is reset when RST* is low or when Register 71H, Bit 5 is set.
Bit 2	**ECC ERROR**: This bit will be set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error. This bit is reset when RST* is low, Register 71H, Bit 5 is set, or Register 79H is written.
Bit 3	**CORRECTABLE ERROR FOUND**: When this bit is set, it indicates that the interactive ECC correction circuit has found a correctable error and has shifted the error burst to a byte boundary. This bit is valid after the ECC SHIFT CONTROL bit (Register 71H, Bit 1) has gone from set to reset. This bit is reset when RST* is low, Register 71H, Bit 5 is set, or Register 71H, Bit 0 is reset.
Bit 4	**SEQUENCER STOPPED**: When this bit is set, it indicates the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 37) and the WRITE GATE signal (Pin 38) are reset. This bit is set when the RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.
Bit 5	**BRANCH ACTIVE**: This bit is set when a branch condition is met. Reading this register will reset this bit. It is also reset when the RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.
Bit 6	**DATA TRANSFER STATUS**: This bit indicates the status of the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, Bit 0). It is set during data transfer between the buffer memory and the disk, regardless of the state of SUPRESS TRANSFER. It is reset when the Sequencer stops.
Bit 7	**AM ACTIVE**: This bit is set when the DATA TRANSFER bit (Writable Control Store (WCS) CONTROL FIELD, Bit 0) is reset and the COUNT/AM bit (Writable Control Store (WCS) COUNT FIELD, Bit 7) is set. It is reset after reading or writing the ECC bytes. It is also reset when the Sequencer stops.

9.13 79H – Sequencer Start Address (Write Only)

The Sequencer can be stopped by writing 1FH to this register.

Bits 0-4	**START ADDRESS**: A write to this register will start the Sequencer at the latched address. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.
Bits 5-7	**RESERVED**.

9.14 7AH – Operation/Control Status (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low or when Register 71H, Bit 5 is set.

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk drive. Reading this register will reset this bit. (Read only). This bit is also reset when this register is read.
Bit 1	**SECTOR PAST**: This bit is valid in Hard Sector mode only. It is set by the rising (leading) edge of the pulse on the WAM*/AMD*/SECTOR signal (Pin 35). Reading this register will reset this bit. (Read only). This bit is also reset when this register is read.
Bit 2	**NRZ DATA IN**: This bit is set when a rising (leading) edge is detected at the NRZ signal (Pin 40). Reading the register will reset this bit, but due to the asynchronous relationship between the NRZ signal and the microcontroller, race conditions may interfere with the reset. It is suggested that this bit be read until it reports as reset. (Read only). This bit is also reset when this register is read.
Bit 3	**SYNC DETECT**: This bit is set during a Disk Read operation when the internal serializer/deserializer has been synchronized with the incoming NRZ data and matches the preprogrammed sync character in Register 7CH. This bit is cleared on the falling (trailing) edge of the READ GATE signal (Pin 37). (Read only)
Bit 4	**SEARCH OPERATION**: Setting this bit selects the source of the data for the compare operation. When this bit is set, Read Data is compared to Buffer Memory Data. When this bit is reset, Read Data is compared to the Writable Control Store (WCS) DATA FIELD.
Bit 5	**SUPPRESS TRANSFER**: When this bit is set, serialized or deserialized data will not be read or written to the buffer memory (disabling the buffer memory access mechanism). During a Write operation, the NRZ data will be written with the contents of the Writable Control Store (WCS) DATA FIELD. During a Read operation, the incoming data will have the ECC verified but no data will be transferred to the buffer memory.
Bit 6	**RESERVED**.
Bit 7	**INHIBIT CARRY**: When this bit is set, the carry/load of the Writable Control Store (WCS) COUNT FIELD for the data transfer will be inhibited. This bit will be automatically reset whenever the Sector Size Counter is zero and there is an underflow from the current COUNT FIELD.

9.15 7BH – WAM Control (Read/Write)

Bits 0-7	**WRITE ADDRESS MARK CONTROL**: In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) will be asserted low for each bit cell time corresponding to the bits set in this register during a Write Address Mark operation. Output at the WAM*/AMD*/SECTOR signal (Pin 35) is shifted 3 bits toward the LSB at the output. In Hard Sector mode, the signal will not be asserted. This register is reset when the RST* signal (Pin 36) is asserted low.

9.16 7CH – SYNC Pattern (Read/Write)

Bits 0-7	**SYNC PATTERN**: This register is to be compared with NRZ read data when the READ GATE signal (Pin 37) and, if in Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) are asserted. A match between this register and the serial NRZ read data input will set the SYNC DETECT bit (Register 7AH, Bit 3), and will cause NRZ read data to be gated into the ECC. Only those bits in this Register which are enabled by the CLOCK/SYNC CONTROL Register (7FH) will be used for comparison. In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 35) must also be asserted for the SYNC DETECT bit (Register 7AH, Bit 3) to be set. This register is reset when the RST* signal (Pin 36) is asserted low.

9.17 7DH – Formatter Interrupt Status (Read Only)

A microcontroller read of this register will reset any bits that were set except Bit 7. Bits 0-6 are also reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk drive. This bit is the same as Register 7AH, Bit 0.
Bit 1	**SECTOR PAST**: This bit is valid in Hard Sector mode only. It is set by the rising (leading) edge of the pulse on the WAM*/AMD*/SECTOR signal (Pin 35). This bit is the same as Register 7AH, Bit 1.
Bit 2	**INPUT DETECTED**: This bit will be set by the rising (leading) edge of the INPUT signal (Pin 33).
Bit 3	**SEQUENCER STOPPED**: When this bit is set, it indicates that the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 37) and the WRITE GATE signal (Pin 38) are deasserted. This bit is the same as Register 79H, Bit 4.
Bit 4	**ECC ERROR**: This bit is set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error. This bit is the same as Register 79H, Bit 2.
Bit 5	**DATA TRANSFER STATUS**: This bit will be set by the rising (leading) edge of the DATA TRANSFER STATUS bit (Register 79H, Bit 6).
Bit 6	**SEQUENCER OUTPUT DETECTED**: This bit will be set by the rising (leading) edge of the OUTPUT signal (Pin 33).
Bit 7	**PC INTERRUPT REGISTER SET:** This bit is the logical OR of bits 0 through 4 in the PC Interrupt Register, Register 50H.

9.18 7EH Formatter Interrupt Enable (Read/Write)

This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**INDEX ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the INDEX PAST bit (Register 7DH, Bit 0) is set.
Bit 1	**SECTOR ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SECTOR PAST bit (Register 7DH, Bit 1) is set.
Bit 2	**INPUT DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 19) to be asserted low when the INPUT DETECTED bit (Register 7DH, Bit 2) is set.
Bit 3	**SEQUENCER STOPPED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SEQUENCER STOPPED bit (Register 7DH, Bit 3) is set.
Bit 4	**ECC ERROR ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the ECC ERROR bit (Register 7DH, Bit 4) is set.
Bit 5	**DATA TRANSFER DETECTED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the DATA TRANSFER STATUS bit (Register 7DH, Bit 5) is set.
Bit 6	**SEQUENCER OUTPUT DETECTED ENABLE**: When this bit is set, it will cause the INT* signal (Pin 19) to be asserted low when the SEQUENCER OUTPUT DETECTED bit (Register 7DH, Bit 6) is set.
Bit 7	**RESERVED**.

9.19 7FH – Formatter Stack Enable (Read Only)

Bits 0-7	A read of this register reads the last byte that was enabled (by the STACK ENABLE bit (Bit 4 of the Writable Control Store (WCS) CONTROL FIELD)) onto the stack. The Address Pointer, in ring fashion, moves around the 8-byte circular stack. As the byte is read, the Address Pointer moves to the previous location. The data during a read is never 'popped' from the stack; it is not lost or removed, and a continuous read of eight locations would bring one back around to the original location, reading the same data. If 10 bytes in a field were enabled to the stack, the last eight bytes would be captured as the first two bytes would be overwritten. The first byte read would be the tenth byte enabled onto the stack. In reverse order, all of the last eight bytes could then be read continuously, in a circular manner.

9.20 7FH – CLOCK/SYNC Control (Write Only)

This register, except Bit 7, is reset when the RST* signal (Pin 36) is asserted low.

Bits 0-2 **SYNC COMPARE CONTROL**: These bits specify the number of bits to be used in the compare for the sync byte programmed in the SYNC PATTERN Register (7CH).

Bits 2	1	0	
0	0	0	= Only Bit 7 is compared.
0	0	1	= Only Bits 7 and 6 are compared.
0	1	0	= Only Bits 7 – 5 are compared.
0	1	1	= Only Bits 7 – 4 are compared.
1	0	0	= Only Bits 7 – 3 are compared
1	0	1	= Only Bits 7 –2 are compared.
1	1	0	= Only Bits 7 –1 are compared.
1	1	1	= All bits are compared.

Bit 3 **RESERVED.**

Bit 4 **BUFFER WRITE MOE* DISABLE:** This bit, when set, will disable the signal MOE* (Pin 17), during buffer write operations. This includes both formatter and Host buffer writes, as well as local microcontroller Register 70H.

Bit 5 **BCLK DISABLE**: The user **must** program this bit to be reset. When this bit is set, the internal clock will be disabled. It is used for test purposes.

Bits 6-7

Bits 7	6	
0	0	= Allows one buffer memory access cycle per four BCLK cycles.
0	1	= Allows one buffer memory access cycle per two BCLK cycles.
1	0	= Allows one buffer memory access cycle per BCLK cycle.
1	1	= Allows one buffer memory access cycle per three BCLK cycles.

Bit 7 is set and Bit 6 is reset when the RST* signal (Pin 36) is asserted low .

10. EXTERNAL ACCESS REGISTERS

10.1 4DH – Shadow Latch (Read Only)

Bits 0-7	**DATA**: When the microcontroller reads Register 70H, the content of the buffer memory data bus will be captured in this register. This register is reset when the RST* signal (Pin 36) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

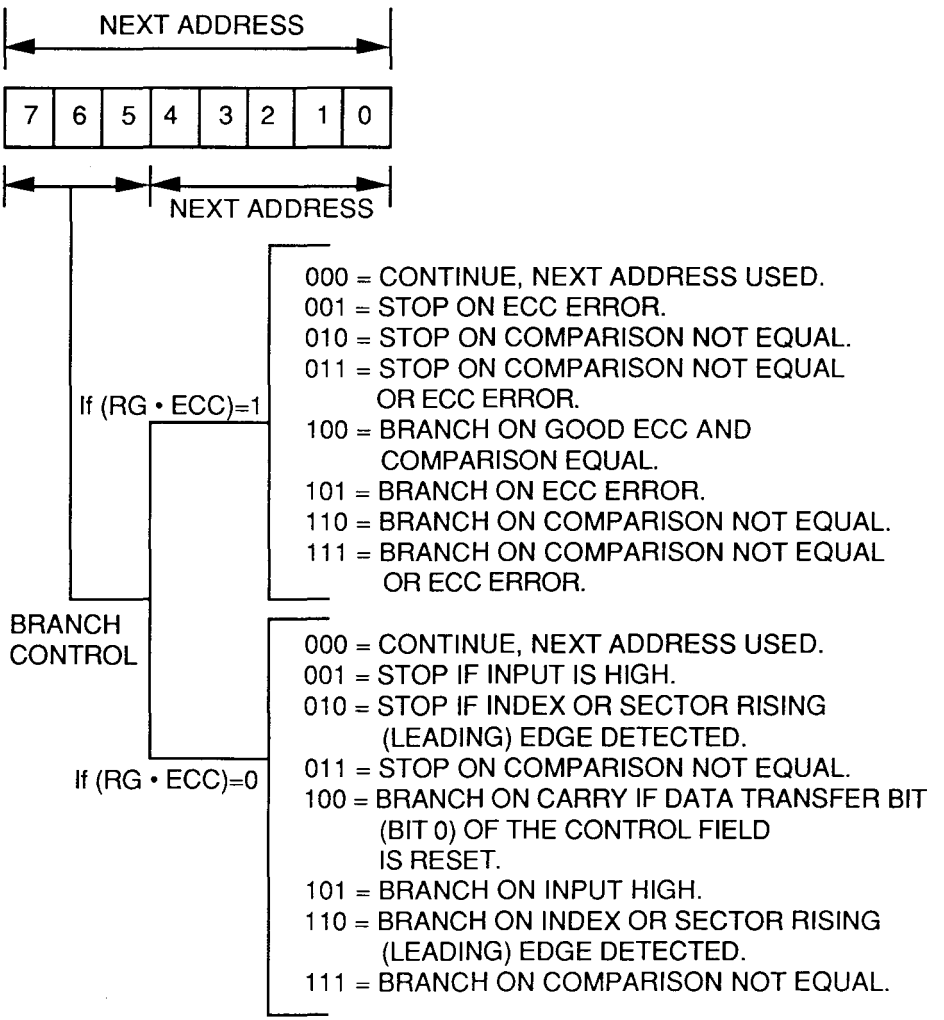
10.2 70H – Buffer Memory Access (Read/Write)

Bits 0-7	**BUFFER MEMORY ACCESS**: Register 70H decode internally bridges the buffer memory data bus and the microcontroller bus (allowing the microcontroller to access the buffer memory) and causes the CL–SH265 to assert buffer memory address lines, the MOE* signal (Pin 17), and the WE* signal (Pin 18). Read data from the buffer memory will also be latched into the SHADOW LATCH Register (4DH). If the MOE* DISABLE bit (Register 52H, Bit 0) is set to logical 1, the MOE* signal (Pin 17) is not asserted, so that the microcontroller can read external switch settings on the buffer memory data bus. If the BUFFER POINTER AUTO-INCREMENT ENABLE bit (Register 48H, Bit 0) is reset, the appropriate address pointer, RAP or WAP, will not change. If the BUFFER POINTER AUTO-INCREMENT ENABLE bit is set, the appropriate address pointer will increment for each microcontroller access to this port, whether it is a read or write access. Both disk and host transfers must be halted before the microcontroller attempts any access to this port.

11. WRITABLE CONTROL STORE (WCS) FIELDS

The Writable Control Store (WCS) (addresses 80H-9EH, A0H-BEH, C0H-DEH, and E0H-FEH) may only be written to by the support microcontroller when there is no risk of the contents being accessed by the Sequencer. This is normally true only during long data transfers or when the Sequencer is stopped.

11.1 80H-9EH – Next Address Field (Read/Write)



11.1 80H-9EH – Next Address Field (Read/Write) *(cont.)*

Bits 0-4 **NEXT ADDRESS**: This is the address the Sequencer will go to after the decrementing byte counter has reached zero and a branch has not been taken. There are 31 possible next-address locations (00H-1EH). Address 1FH establishes the stopped condition.

Bits 5-7 **BRANCH CONDITION/CONTROL:** These three bits are mainly used to specify branch conditions. However, in some cases, they are also used to control formatter operations.

The following are branch conditions when both the READ GATE signal (Pin 37) is asserted and the PROCESS ECC bit (Bit 6) of the Current Sequencer Word COUNT FIELD is set. All these branch conditions are evaluated during the last byte of execution of the Current Sequencer Word.

000 = Continue, next address used.
001 = Stop on ECC error.
010 = Stop on comparison not equal.
011 = Stop on comparison not equal or ECC error.
100 = Branch on good ECC and comparison equal.
101 = Branch on ECC error.
110 = Branch on comparison not equal.
111 = Branch on comparison not equal or ECC error.

The following are branch conditions at all other times:

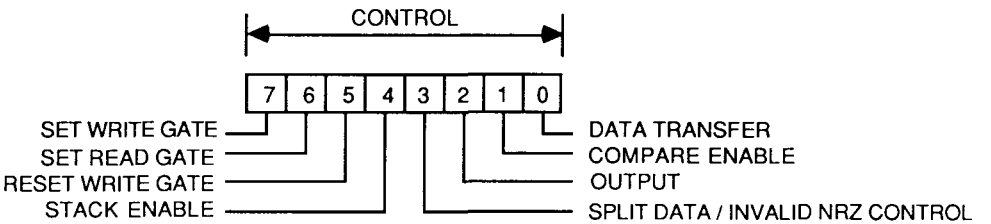
000 = Continue, next address used.
001 = Stop if INPUT is high
010 = Stop if INDEX or SECTOR rising (leading) edge detected.
011 = Stop on comparison not equal.
100 = Branch on carry if DATA TRANSFER bit (Bit 0) of the Current Sequencer Word CONTROL FIELD is reset.
101 = Branch on INPUT high.
110 = Branch on INDEX or SECTOR rising (leading) edge detected.
111 = Branch on comparison not equal.

When the DATA TRANSFER bit (Bit 0) of the Current Sequencer Word CONTROL FIELD is set, then:

100 = Set INHIBIT CARRY.

CIRRUS LOGIC

11.2 A0H-BEH – Control Field (Read/Write)

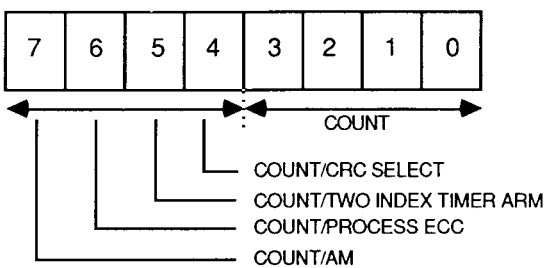


Bit 0	**DATA TRANSFER**: When this bit is set, the COUNT FIELD is used as an eight-bit counter. Each byte time that this bit is set, a byte of data will be accessed from buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the WRITE GATE signal (Pin 38) is asserted, then a byte of data is read from the buffer memory (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset) or from the Writable Control Store (WCS) DATA FIELD (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set), and is serialized and sent to the NRZ signal (Pin 40). If the READ GATE signal (Pin 37) is asserted, then a byte of data is deserialized from the NRZ signal and is then written to the buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set, then no data is written to the buffer memory.
Bit 1	**COMPARE ENABLE**: When this bit is set and the READ GATE signal (Pin 37) is asserted, it will allow a comparison between Read Data and the Writable Control Store (WCS) DATA FIELD, or the buffer memory data (if the SEARCH OPERATION bit (Register 7AH, Bit 4) is set).
Bit 2	**OUTPUT**: This bit drives the OUTPUT signal (Pin 33) and is used to synchronize external logic functions to the state of the Writable Control Store (WCS).
Bit 3	**SPLIT DATA FIELD/INVALID NRZ CONTROL**: If Bit 7 of Register 48H is set, this bit is used to indicate split or contiguous data field. If this bit is set, it is a split data field. Otherwise, it is a contiguous data field. If Bit 7 of Register 48H is reset, this bit is used to suspend the synchronization circuit between the programmed sync character and the NRZ data. Setting this bit to 1 will block the NRZ data input when the read gate is set. This allows for VFO settling, after the assertion of read gate.
Bit 4	**STACK ENABLE**: When this bit is set, Read Data is pushed on the eight-byte circular stack.
Bit 5	**RESET WRITE GATE**: This bit is used to deassert the WRITE GATE signal (Pin 38). The WRITE GATE signal (Pin 38) will be deasserted on the last byte count of the Sequencer word with this bit set. The WRITE GATE signal (Pin 38) is also deasserted when the Sequencer comes to the stopped state.
Bit 6	**SET READ GATE**: The READ GATE signal (Pin 37) will be asserted when the Sequencer word with this bit set is executed. The READ GATE signal (Pin 37) will be deasserted at the end of ECC or when the Sequencer goes to the stopped state. The READ GATE signal (Pin 37) will not be asserted if the WRITE GATE signal (Pin 38) is already asserted.

11.2 A0H-BEH – Control Field (Read/Write) *(cont.)*

Bit 7 **SET WRITE GATE**: The WRITE GATE signal (Pin 38) will be asserted when the Sequencer word with this bit set is executed. After this bit is set, WRITE GATE control will be reset by executing a Sequencer word with the RESET WRITE GATE bit (Bit 5) set or when the Sequencer goes to the stopped state. The WRITE GATE signal (Pin 38) will not be asserted if the READ GATE signal (Pin 37) is already asserted.

11.3 C0H-DEH – Count Field (Read/Write)



COUNT FIELD FUNCTIONALITY

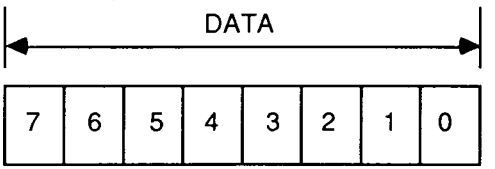
WG On	RG On	Data Transfer	Bit 7	Bit 6	Bit 5	Bit 4	Bits 3-0	Max Count
0	0	0	AM	PROCESS ECC	ARM TIMER	COUNT	COUNT	32
0	0	1	COUNT	COUNT	COUNT	COUNT	COUNT	256
0	1	0	AM	PROCESS ECC	RESERVED	CRC SELECT	COUNT	16
0	1	1			ILLEGAL			
1	0	0	AM	PROCESS ECC	ARM TIMER	CRC SELECT	COUNT	16
1	0	1			ILLEGAL			
1	1	0			ILLEGAL			
1	1	1			ILLEGAL			

11.3 C0H-DEH – Count Field (Read/Write) *(cont.)*

This sets the initial value of the Sequencer counter when a new state is entered.

Bits 0-3	**COUNT**: These bits are always used for the initial value of the Sequencer byte counter when a new state is entered. When it reaches zero, a new instruction word will be accessed from the Disk Formatter Writable Control Store (WCS).
Bit 4	**COUNT/CRC SELECT**: In the Current Sequencer Word, when the SET WRITE GATE and the SET READ GATE bits (CONTROL FIELD, Bits 7 and 6 respectively) are reset, or if the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is set, this is a count bit (for a 5-bit, or an 8-bit count field). (Note that the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set and the SET WRITE GATE or the SET READ GATE bit (CONTROL FIELD, Bits 7 and 6 respectively) set is an illegal selection.) If in the Current Sequencer Word, either the SET WRITE GATE or SET READ GATE bit (CONTROL FIELD, Bits 7 and 6 respectively) is set, and the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, then the CRC SELECT function is active. With this function active, this bit set initializes the ECC function to the CRC polynomial and when this bit is cleared, the ECC function is initialized to the 32/56-bit computer generated polynomial.
Bit 5	**COUNT/TWO INDEX TIMER ARM**: When the DATA TRANSFER bit of the Current Sequencer Word is set, this is a count bit (for an eight-bit count field). The Two Index Timer is armed by the WCS whenever the SET READ GATE bit and DATA TRANSFER bit are reset, and this bit is set.
Bit 6	**COUNT/PROCESS ECC**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, this bit treats the incoming NRZ data (if the READGATE is active), or the outgoing NRZ data (if the WRITE GATE signal (Pin 38) is asserted) as an ECC or CRC field.
Bit 7	**COUNT/AM**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, and the READ GATE signal (Pin 37) is asserted, this bit will set the AM ACTIVE bit (Register 79H, Bit 7). When the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, and the WRITE GATE signal (Pin 38) is asserted, this bit will set the AM ACTIVE bit (Register 79H, Bit 7), and will be used to initialize the CRC/ECC Registers. If in the Soft Sector mode (Register 77H, Bit 7 is reset), the WAM* output will be asserted low as programmed in the WAM CONTROL Register (7BH).

11.4 E0H-FEH – Data Field (Read/Write)



Bits 0-7	This register is the source for all overhead bytes of data used by the device during Write operations. During Read operations, it is one of the operands to the comparison logic. When the DATA TRANSFER bit in Current Sequencer Word (CONTROL FIELD, Bit 0) is set with the WRITE GATE signal (Pin 38) asserted, the source for write data will be the external buffer memory. When SUPPRESS TRANSFER bit (Register 7HA, Bit 5), is on with WRITE GATE signal (Pin 38) asserted, the source for write data will be the content of this register. This register can also be the branch address source if Register 48H, Bit 5 (WCS Data Field Branch Enable) is set.

12. SEQUENCER REGISTERS

The Writable Control Store (WCS) word being executed is stored in these registers. These registers should only be written to by the microcontroller when the Sequencer is stopped. These registers can be read anytime.

12.1 49H – Current Sequencer Word - Next Address Field (Read/Write)

This register allows the microcontroller to access the NEXT ADDRESS FIELD of the Current Sequencer Word.

12.2 4AH – Current Sequencer Word - Count Field (Read/Write)

This register allows the microcontroller to access the COUNT FIELD of the Current Sequencer Word.

12.3 4BH – Current Sequencer Word - Control Field (Read/Write)

This register allows the microcontroller to access the CONTROL FIELD of the Current Sequencer Word.

12.4 4CH – Current Sequencer Word - Data Field (Read/Write)

This register allows the microcontroller to access the DATA FIELD of the Current Sequencer Word.

13. AUXILIARY CONTROL REGISTERS

13.1 48H – Auxiliary Control 0

This register is reset by assertion of RST* (Pin 32).

Bit 0	R/W	**BUFFER POINTER AUTO-INCREMENT ENABLE:** This bit, when set, allows auto-incrementing of the buffer address when the microprocessor reads or writes Register 70H for buffer accesses. In this mode, if ROP=1, WAP is auto-incremented for every Register 70H access. If ROP=0, RAP is auto-incremented for every Register 70H access.
Bit 1	R/W	**POWER DOWN ENABLE:** This bit, when set, will turn off all unused internal clocking of logic to save power. This bit can only be set by firmware. Before firmware sets this bit, it must make sure that there are no disk or Host activities pending, and the chip can enter the power-down state. This bit is reset by assertion of HRESET (Pin 57), RST* (Pin 32), a Host Programmed Reset, or when the Host issues a command to the chip. When the Host issues a command to the chip, the local microprocessor is locked out from setting this bit until a write to Register 73H is performed.
Bit 2	R	**DATA FIELD ECC ERROR:** When this bit is set, an ECC error has been detected. When this bit is reset, no ECC error has occurred. The combination of this bit and Register 7DH, Bit 4, allows the local microprocessor to determine whether the error is in the sector ID field or in the data field. This bit is reset by RST* (Pin 57), formatter reset (Register 71H, Bit 5 = 1), when the formatter starts a new ECC calculation, or when Register 79H is written.
Bit 3	R	**TWO INDEX DETECTED STATUS:** This bit is set when the Two Index Detection circuit has been enabled and two index edges have been detected without a data transfer between the formatter and buffer. This bit is reset when the Two Index Detection mode is disabled (Register 48, Bit 6 = 0) or when the Two Index Detection circuit is armed by the WCS.
Bit 4	R/W	**CLEAR FIXED DISK REGISTER, BIT 0:** This bit is used to reset the DMA Enable control bit in the Fixed Disk Register. To reset Fixed Disk Register, Bit 0, set and clear this bit. This bit is reset by HRESET (Pin 57), RST* (Pin 32), and Host Programmed reset.
Bit 5	R/W	**WCS DATA FIELD BRANCH ENABLE:** When set, this bit selects the lower 5 bits of the WCS Data Field as the branch address. When this bit is reset, the branch address is the lower 5 bits of Register 78H. This bit is reset by RST* (Pin 57).

Bit 6	R/W	**TWO INDEX DETECTION MODE ENABLE:** When this bit is set, the Two Index Detection mode is enabled. When the Two Index Detection mode is enabled, the index detection circuit is armed or re-armed by the WCS. The detection circuit is armed if the WCS Control field has both READGATE and DATA TRANSFER off and Bit 5 of the Count field is set. Once the circuit is armed, it remains armed until one of following three events happens: 1) data transfer happens between the formatter and buffer, 2) two index pulses are detected and the formatter is stopped, or 3) Two Index Detection Mode Enable bit is reset. When the detection circuit is armed, and two index edges are detected, the Two Index Detected status bit is set (Register 48H, Bit 3). The status bit remains set until the detection circuit is re-armed or the Two Index Detection Mode is disabled. When the Two Index Detected status bit is set, it asserts the "stopped" signal to stop formatter operation. This, in turn, disarms the detection circuit.
Bit 7	R/W	**ENABLE SPLIT DATA FIELD:** When this bit is set, the split data field operation is enabled, i.e., Bit 3 of the WCS control field is used to indicate a split data field. When this bit is reset, the Invalid NRZ operation is enabled.

13.2 4FH – Auxiliary Control 1 (Read/Write)

Bits 0-2	**RESERVED.**
Bit 3	**CLEAR XT/AT BUSY ENABLE**: This bit, when set, will allow the automatic clear of the BUSY bit (Register 55H, Bit 7) in the XT mode when the Host reads the Completion Status Byte at the end of all commands. In the AT mode, the BUSY bit is cleared on the last sector of a READ command after the FIFO has been filled and DREQ is asserted. This bit is reset by RST*.
Bit 4	**RRC FILTER DISABLE:** This bit, when set, disables the filter circuit for the RD/REF CLK (Pin 35) input signal. This will allow up to 25 Mbits/Sec data rates to be supported by the CL-SH265. When reset, this bit will enable the filter circuit. With the filter circuit enabled, the CL-SH265 can tolerate 10 ns pulse widths, high or low, during READGATE transitions on RD/REF CLK, but limiting data rate to 16 Mbits/Sec. With the filter disabled, no short pulses on the RD/REF CLK will be permissable. This bit is reset by RST*.
Bit 5	**ECC PRESET CONTROL:** This bit, when set, will preset the ECC generator to all "0's" during generator operation. When this bit is reset the generator will be preset to all "1's". This bit is reset by RST*.
Bit 7-6	**LOCAL MICROPROCESSOR WAIT STATE, BITS 1-0:** These two bits control the assertion time of the LRDY* (Pin 27) signal during a local microprocessor access to the CL-SH265. Each waitstate is equal to one BUFCLK period. A BUFCLK period is equal to the divided down buffer access time specified by Register 7FH, Bits 7-6. These two bits are set to 11 by RST*. The wait state selection options are: Bits 7 6 --- 0 0 no wait states 0 1 1-2 wait states 1 0 2-3 wait states 1 1 3-4 wait states

14. MICROCONTROLLER-HOST INTERFACE

The local microcontroller interface to the Host is programmed through a set of command, status, and control registers. Many of these registers are shared for XT and AT applications. The registers are configured to operate in PC XT or PC AT mode by programming the XT/AT SELECT bit (Register 58H, Bit 7). This configuration has to be done on power-up, or after any assertion low of the RST* signal (Pin 36). Host resets will not change this configuration. Eight of these registers can be mapped to locations 40H-47H or 60H-67H, by programming the HOST REGISTER FILE DECODE SELECT bit (Register 77H, Bit 2). In general, these registers may be accessed at any time, except when noted.

14.1 XT Mode Registers

These registers are configured for the XT Command Blocks, Status and Configuration information transfer when the XT/AT SELECT bit (Register 58H, Bit 7) is set. In this mode, the register file has eight Command/General Purpose Registers and three Control/Status Registers. The registers are as follows:

ADDRESS	READ	WRITE
40H or 60H	Command/General Byte 0	Command/General Byte 0
41H or 61H	Command/General Byte 1	Command/General Byte 1
42H or 62H	Command/General Byte 2	Command/General Byte 2
43H or 63H	Command/General Byte 3	Command/General Byte 3
44H or 64H	Command/General Byte 4	Command/General Byte 4
45H or 65H	Command/General Byte 5	Command/General Byte 5
46H or 66H	General Byte 6	General Byte 6
47H or 67H	General Byte 7	General Byte 7
55H	Mode/Status	Mode/Status
56H	Drive Type	Drive Type
57H	DRV/DMA/IRQ ENABLE Status	Reserved

14.1.1 40H-47H (60H-67H) – XT Command/General Purpose Registers (Read/Write)

Bits 0-7	The Command/General Purpose Registers allow the local microcontroller to transfer bytes between the Host and the disk controller, without going through the buffer memory. These registers are used to receive the six command or configuration bytes and to send sense status or command completion status. The local microcontroller is locked out of these registers during transfers with the Host involving these registers. Host access to these registers are controlled by the local microcontroller through XT MODE/STATUS Register (55H). The microcontroller has read/write access to all the Command/General Purpose Registers. However, for the Host access, the read/write direction is controlled by the I/O* bit (Bit 5) in the XT MODE/STATUS Register (55H). These registers are not affected by any Reset condition.

14.1.2 55H – XT Mode/Status

This register contains control and status information for the XT interface. All transfers between the Host and the local register file are controlled by this register. This register is reset when the HOST RESET signal (HRESET—Pin 56) is asserted, or when the RST* signal (Pin 36) is asserted low, or by a Host Programmed Reset.

Bits 0-2	R/W	**LRTC0:2**: These bits represent the number of bytes to be transferred between the Host and the Command/General Purpose Registers (40H-47H/60H-67H). Up to 8 bytes may be transferred each time. These bits contain the transfer length minus one (i.e., LRTC0:2=0 for a transfer of 1). The Transfer Address Pointer for the Command/General Purpose Registers always start with register 0 and is incremented on each byte transfer. A read of these bits represents the number of bytes minus one that is left to be transferred.
Bit 3	R/W	**LRTNS**: When this bit is set, it initiates a transfer between the Host and the Command/General Purpose Registers (40H-47H/60H-67H). This bit will be reset when the Host transfer is completed. The local microcontroller should not access the Command/General Purpose Registers when this bit is set. This bit may be set by the local microcontroller only when there are no active transfers between the Host and buffer memory (i.e., when the BTRNS bit [Bit 4] is reset).
Bit 4	R	**BTRNS**: This bit represents the state of Host-buffer memory access. When this bit is set, it indicates that transfers are active between the Host and the buffer memory. When this bit is set, the local microcontroller may not initiate a transfer between the Command/General Purpose Registers (40H-47H/60H-67H) and the Host.
Bit 5	R/W	**I/O***: This bit determines the direction of Host data transfer when the BTRNS bit or the LRTNS bit (Bit 3 or 4 respectively) is asserted. See the following PC/XT I/O Bus Phase table.
Bit 6	R/W	**C/D***: This bit determines the type of information being requested, i.e. Command, Status, or Data. See the following PC/XT I/O Bus Phase table.

14.1.2 55H – XT Mode/Status *(cont.)*

Bit 7	R/W	**BUSY:** The Busy bit indicates that the controller is busy executing a command. The Busy bit is set during the Selection Phase by the Host; if CLEAR XT/AT BUSY ENABLE bit (Register 4FH, Bit 3) is set, this bit is automatically reset at the end of the command, during the Status Phase when the Host reads the Status Byte.

PC/XT I/O Bus Phase Table

BUSY	C/D*	I/O*	STATE OF CONTROLLER	DIRECTION OF TRANSFER
0	x	x	IDLE	
1	0	0	DATA PHASE	PC to Disk Controller
1	0	1	DATA PHASE	Disk Controller to PC
1	1	0	COMMAND PHASE	PC to Disk Controller
1	1	1	STATUS PHASE	Disk Controller to PC

14.1.3 56H – XT Drive Type (Read/Write)

This register may be accessed by the local microcontroller at any time. Generally, this register contains information required by the XT BIOS driver to configure the physical attributes of the drive (i.e., cylinders, heads, sectors/track). From the Host, this register appears as a read-only register which can be accessed by a Port 2 read. In PC XT MASTER/SLAVE mode, only 4 bits of this register are driven to the Host. For the MASTER, bits 0-3 are driven. For the SLAVE, bits 4-7 are driven. If the CL-SH265 is not configured for MASTER/SLAVE mode, then all 8 bits of this register are driven to the Host. This register is not affected by any Reset condition.

14.1.4 57H – XT DRV/DMA/IRQ ENABLE (Read Only)

This register reflects the contents of the DRV/DMA/IRQ ENABLE Register (Port 3) which is written to by the Host. This register can be accessed at any time. This register is reset when the HOST RESET signal (HRESET—Pin 56) is asserted or under a Host Program Reset.

Bit 0	R	**DMAEN**: This bit is the same as Port 3, Bit 0. It allows driving the Host DREQ signal (Pin 51) during DATA phase transfers.
Bit 1	R	**IRQEN**: This bit controls the enable for the tri-stated Host Bus HINT signal (Pin 44). When this bit is reset, no interrupts will be issued to the Host microcontroller. When this bit is set, it allows the disk controller to interrupt the Host at the Command Completion phase.
Bit 2	R	**DRV**. This bit, in MASTER/SLAVE mode, enables the Host to select a controller prior to issuing a command. If this bit is 0, MASTER is selected; if this bit is 1, SLAVE is selected. If not in MASTER/SLAVE mode, this bit is a "don't care".
Bits 3-7	R	**RESERVED.**

14.2 AT Mode Registers

These registers are configured for the PC AT Task File when the XT/AT SELECT bit (Register 58H, Bit 7) is reset. In this mode, the register file has eight Command/Parameter Registers and three Control/Status Registers. These registers are as follows:

ADDRESS	READ	WRITE
40H or 60H	Error Status	Error Status
41H or 61H	Write Precompensation	Write Precompensation
42H or 62H	Sector Count	Sector Count
43H or 63H	Sector Number	Sector Number
44H or 64H	Cylinder Low	Cylinder Low
45H or 65H	Cylinder High	Cylinder High
46H or 66H	Drive/Head Number	Drive/Head Number
47H or 67H	Command	Command
55H	Control/Status	Control/Status
56H	Drive 0 Status	Drive 0 Status
57H	Drive 1 Status	Drive 1 Status
73H	ECC Status [31:24]/[7:0]	Autocommand "LOCK" Release

These registers may be accessed by the local microcontroller, after setting the XT/AT SELECT bit (Register 58H, Bit 7) to 0. (See the PC MODE CONTROL Register (58H), Section 8.6). The local microcontroller has write access to Registers 40H/60H - 47H/67H only when the BUSY bit (Register 55H, Bit 7) is set, and the BTRANS bit (Register 55H, Bit 4) is reset. The local microcontroller always has read access to Registers 40H-47H or 60H-67H. The registers, except the AT DRIVE/HEAD NUMBER Register (46H/66H), are not affected by any Reset condition.

14.2.1 40H (60H) – AT ERROR STATUS (Read/Write)

The local microcontroller can write detailed error status of the last command failure to this register. This register can also be used to set disk controller diagnostic errors during the Diagnostic command or on power-up. When an error occurs, this register can be loaded and the ERROR bit (Bit 0) set in the the AT CONTROL/STATUS Register (55H).

14.2.2 41H (61H) – AT WRITE PRECOMPENSATION (Read/Write)

This register sets the boundary at which the disk controller will start precompensating the data written to the disk drive. The value in this register is the cylinder address divided by four. This register may only be read by the Host when the BUSY bit (Bit 7) in the AT HOST CONTROLLER/DRIVE STATUS Register is not set.

14.2.3 42H (62H) – AT SECTOR COUNT (Read/Write)

This register is used to specify the number of sectors to be transferred during a Read/Write Sector command. This register is decremented by the local microcontroller as each sector is transferred. If this register is loaded with 0 then 256 sectors are transferred.

14.2.4 43H (63H) – AT SECTOR NUMBER (Read/Write)

This register is used to specify the starting sector number for the current Read/Write Sector command. This register is incremented by the local microcontroller as each sector is transferred between the Host and the disk controller.

14.2.5 44H (64H) – AT CYLINDER LOW (Read/Write)

This register is used to specify the lower eight bits of the disk cylinder address. This register, in conjunction with the AT CYLINDER HIGH Register (45H/65H), constitutes a 16-bit cylinder address. This register is incremented by the local microcontroller as each cylinder boundary is crossed.

14.2.6 45H (65H) – AT CYLINDER HIGH (Read/Write)

This register is used to specify the upper eight bits of the disk cylinder address. This register, in conjunction with the AT CYLINDER LOW Register (44H/64H), constitutes a 16-bit cylinder address. This register is incremented by the local microcontroller as each cylinder boundary is crossed, if the lower cylinder value overflows.

14.2.7 46H (66H) – AT Drive/Head Number (Read/Write)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT	Sector Size		Drv #	Head Number			

This register is used to specify the sector size, drive and head number. The local microcontroller changes the head address as each track or cylinder boundary is crossed. This register is reset by assertion of the HOST RESET signal (HRESET—Pin 56), by assertion low of the RST* signal (Pin 36), by a Host Programmed Reset, or by a Diagnostic command (90H). The format of the register is shown above.

14.2.8 47H (67H) – AT Command (Read/Write)

A new command issued by the Host to the disk controller is loaded in to this register.

14.2.9 55H – AT Control/Status

This register is reset when the RST* signal (Pin 36) is asserted low, or when the HOST RESET signal (HRESET—Pin 56) is asserted, or under Host program reset. Bits 1,2, and 3 of this register, however, are only reset by the HOST RESET signal (HRESET—Pin 56).

Bit 0	R/W	**ERROR**: This bit is set when an error occurred on the last command or power-up diagnostics. The error code is stored in the Error Status register. This Error bit is cleared whenever the Host writes to the AT Command register.
Bit 1	R	**INTEN***: This bit reflects the status of the INTEN* bit (Bit 1) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit. When this bit is reset to logical 0, the tri-state interrupt line to the Host bus is enabled.
Bit 2	R	**RESET**: This bit reflects the status of the RESET bit (Bit 2) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit. When this bit is set, the Host is issuing a programmed reset to the disk controller. This condition can be sensed by the local microcontroller through the PC RESET DETECTED bit (Bit 4) of the HOST INTERRUPT STATUS Register (50H).
Bit 3	R	**HD3EN**: This bit reflects the HEAD SELECT 3 ENABLE bit (Bit 3) of the AT HOST FIXED DISK Register. The local microcontroller can only monitor this bit.
Bit 4	R/W	**INT**: The Interrupt Request (INT) bit allows the local processor to set a interrupt to the Host by writing a one to this bit. The read of this bit returns the status of PC interrupt line, HINT (Pin 41). If interrupt is enabled, the controller asserts the HINT signal to request each sector of data transfer between the Host and the FIFO. HINT is deasserted at the end of every sector transfer except the very last sector. At the end of the last sector transfer, HINT remains asserted to indicate the end of multiple sector transfers until the interrupt is serviced by the Host. However, if an error occurs during multiple sector transfers, the HINT signal is asserted upon the error detection and stays asserted through the end of the last sector transfer. The automatic reset of the HINT signal can be disabled by Register 54H, Bit 0.
Bit 5	R/W	**CDATA**: This bit is set by the local microcontroller whenever, on the previous read sector transfer, a data error had been corrected. The CDATA bit is cleared whenever the Host writes to AT command register.
Bit 6	R	**BTRNS**: This bit indicates the state of Host buffer memory access. When this bit is set, it indicates that transfers are active between the Host and the buffer memory. In a disk read, this bit is reset when the last data is transferred to the Host. In a disk write, this bit is reset when the last data is transferred to the buffer memory.
Bit 7	R/W	**BUSY:** The Busy bit indicates that the controller is executing a command. The Busy bit is set by the Host writing to the command register. The Busy bit is automatically cleared, if CLEAR XT/AT BUSY ENABLE (Register 4FH, Bit 3) is set on the last sector of a READ command after the FIFO has been filled and DREQ is asserted. The definition of the last sector is: the only sector in the case of a single sector read, the actual last sector of a multi-sector read if no errors, or the sector in error regardless of the sector count. (A sector in error is indicated by the assertion of Register 55H, Bit 0). This bit is also set when a Diagnostic command is issued, the

14.2.9 55H – AT Control/Status *(cont.)*

Bit 7	R/W	Host writes to the Command register, or when RST* (Pin 32), HRESET (Pin 57), or a Host Programmed Reset is active.

14.2.10 56H – AT Drive 0 Control/Status (Read/Write)

This register contains drive-related status information that is part of the AT HOST CONTROL/STATUS Register, when Disk Drive 0 is selected in the DRIVE NUMBER field (Bit 4) of the AT HOST DRIVE/HEAD Register. This register may be accessed by the local microcontroller at any time. The XT/AT SELECT bit (Register 58H, Bit 7) must be reset for AT operation. This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**SKCMP0**: This bit reflects the state of the Seek Complete signal from Disk Drive 0. When the disk drive is not seeking, this bit is set.
Bit 1	**FAULT0**: This bit reflects the state of the Write Fault signal from Disk Drive 0. When this bit is set, it indicates that the disk drive is unsafe for access.
Bit 2	**READY0**: This bit reflects the state of the Ready signal from Disk Drive 0. When this bit is set, the disk drive is present, but may not be ready for read/write transfers.
Bit 3	**RWC0**: This bit reflects the state of the Reduced Write Current signal from Disk Drive 0. When this bit is set, the current to the disk drive write heads has been reduced.
Bit 4	**OVERRIDE HD3EN0**: When this bit is set, the HD3EN Bit (Bit 3) of the AT HOST FIXED DISK Register for Disk Drive 0 is forced to logical 1.
Bits 5-7	**RESERVED**.

14.2.11 57H – AT Drive 1 Control/Status (Read/Write)

This register contains drive-related status information that is part of the AT HOST CONTROL/STATUS Register, when Disk Drive 1 is selected in the DRIVE NUMBER field (Bit 4) of the AT HOST DRIVE/HEAD Register. This register may be accessed by the local microcontroller at any time. The XT/AT SELECT bit (Register 58H, Bit 7) must be reset for AT operation. This register is reset when the RST* signal (Pin 36) is asserted low.

Bit 0	**SKCMP1**: This bit reflects the state of the Seek Complete signal from Disk Drive 1. When the disk drive is not seeking, this bit is set.
Bit 1	**FAULT1**: This bit reflects the state of the Write Fault signal from Disk Drive 1. When this bit is set, it indicates that the disk drive is unsafe for access.
Bit 2	**READY1**: This bit reflects the state of the Ready signal from Disk Drive 1. When this bit is set, the disk drive is present, but may not be ready for read/write transfers.
Bit 3	**RWC1**: This bit reflects the state of the Reduced Write Current signal from Disk Drive 1. When this bit is set, the current to the disk drive write heads has been reduced.
Bit 4	**OVERRIDE HD3EN1**: When this bit is set, the HD3EN bit (Bit 3) of the AT HOST FIXED DISK Register for Disk Drive 1 is forced to logical 1.
Bits 5-7	**RESERVED**.

15. ELECTRICAL SPECIFICATIONS

15.1 Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0° C to 70° C
Storage Temperature ..... -65° C to 150° C
Voltage On Any Pin With Respect To Ground ..... GND-0.5 to VCC+0.5 Volts
Power Supply Voltage ..... 7 Volts
Power Dissipation ..... 0.750 Watt
Injection Current (Latch-up) at Room Temperature ..... 50 mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

15.2 D.C. Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VCC	Power Supply Voltage	4.75		5.25	V	Operating
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage	2.0		VCC+0.5	V	
VOL(1)†	Output Low Voltage			0.4	V	IOL = 2 mA
VOL(2)	Output Low Voltage			0.5	V	IOL = 24 mA
VOH	Output High Voltage	2.4			V	IOH = –400 µA
ICC(OP)	Supply Current (Operating)		15	50	mA	RRCLK=12.5MHz BCLK=6.25MHz
IL	Input Leakage	-10		10	µA	0<VIN<VCC
IOZ(1)	Tri-state Leakage	-10		10	µA	0<VIN<VCC
IOZ(2)	Tri-state Leakage	-50		50	µA	0<VIN<VCC
CIN	Input Capacitance			10	pF	
COUT	Output Capacitance			10	pF	

NOTE: (1) All output pins except for PC signals
(2) PC outputs
† IOL = 4mA for RG and WG

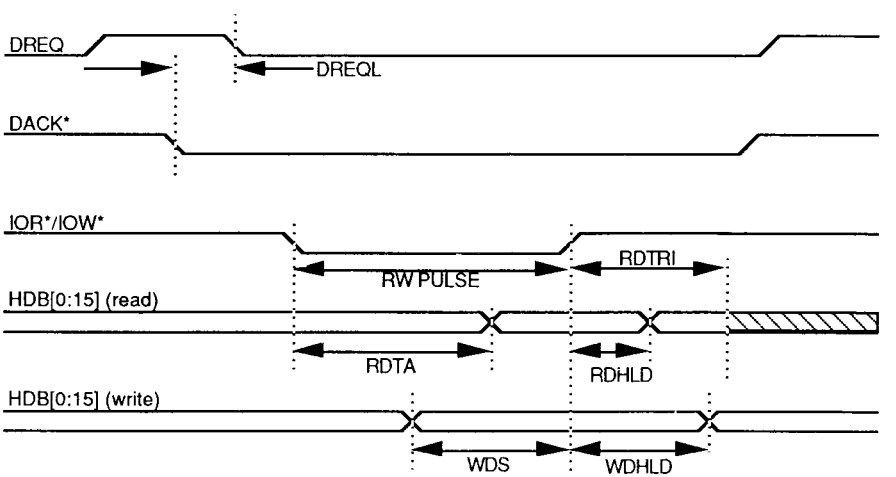
15.3 A.C. Characteristics/Timing Information

The following timings assume that all non-PC outputs will drive one Schottky TTL load in parallel with 50 pF; all Host bus output pins will drive a 300 pF load, and all inputs are at TTL levels. The MIN and MAX timings conform to the operating ranges of a power supply voltage of 5V ±5% and an ambient temperature of 0°C to 70°C. A slash (/) indicates rising edge of signal, while a backslash (\) indicates falling edge of signal.

Host DMA 8/16-Bit Interface Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
DREQL	DREQ \ from DACK* \		80	ns
RDTA	IOR* \ to HDB[0:15] valid		50	ns
RDHLD	IOR* / to HDB[0:15] invalid	0		ns
RDTRI	IOR* high to HDB[0:15] tri-state		40	ns
WDS	HDB[0:15] setup to IOW*/	30		ns
WDHLD	HDB[0:15] hold from IOW*/	10		ns
RWPULSE	IOR*/IOW* pulse width	60		ns

Host DMA 8/16-Bit Interface Timing



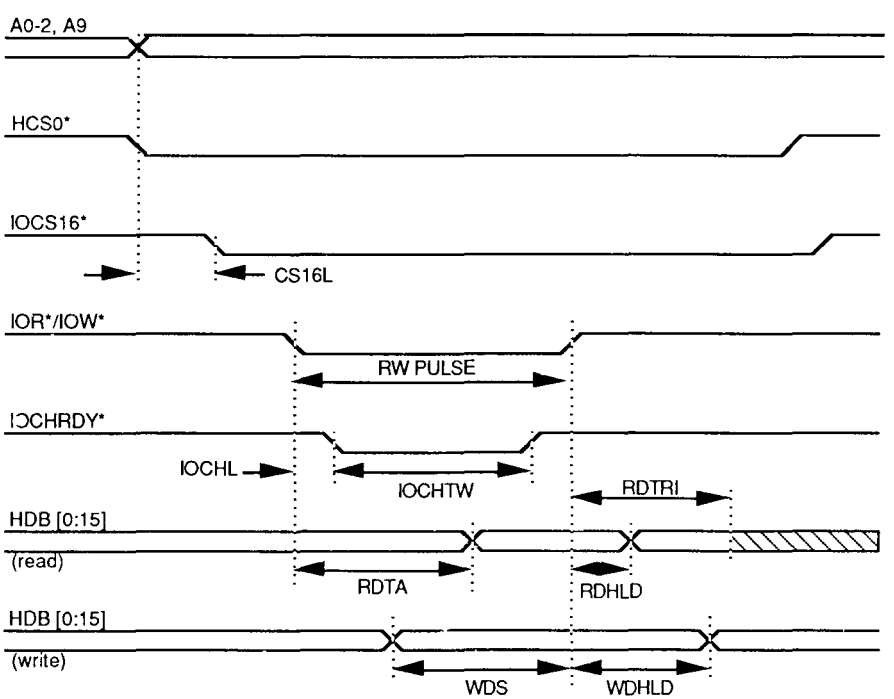
Host Programmed I/O 8/16-Bit Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
CS16L	HCS0* \, A0:2,A9 to IOCS16* \		20	ns
IOCHL	IOR*/IOW* \ to IOCHRDY \		25	ns
IOCHTW	IOCHRDY pulse width	0	5 *BUFCLK	ns
RDTA	IOR* \ to HDB[0:15] valid		50	ns
RDHLD	IOR* / to HDB[0:15] invalid	0		ns
RDTRI	IOR* / to HDB[0:15] tri-state		40	ns
WDS	HDB[0:15] setup to IOW* /.	30		ns
WDHLD	HDB[0:15] hold from IOW* /	10		ns
RWPULSE	IOR*/IOW* pulse width	60		ns

NOTE: BUFCLK is the internal Buffer Clock which indicates the period of Buffer Access Cycle derived from BCLK in appropriate divide by mode. The minimum Buffer Access Cycle (BUFCLK) is 100ns.

These specifications can be tested when the period of BCLK pin is the same as the period of Buffer Access Cycles (i.e. Register 7FH, Bits 6 and 7 are set to 0 and 1 respectively).

Host Programmed I/O 8/16-Bit Timing

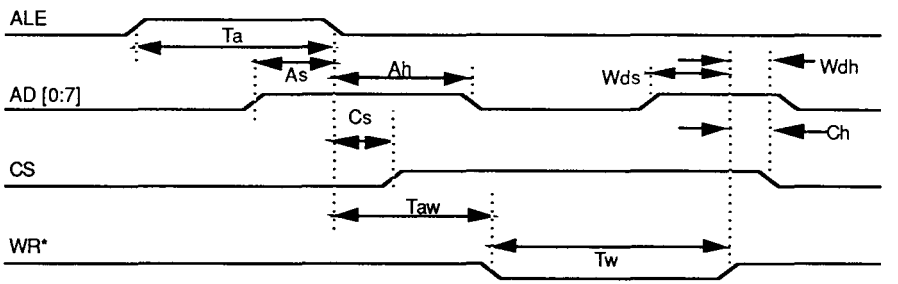


Microcontroller Interface Timing Parameters

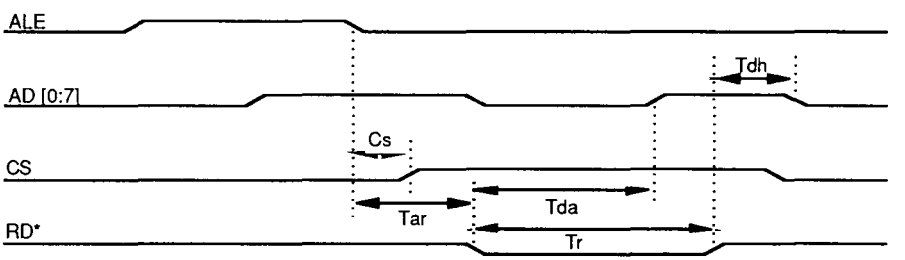
SYMBOL	PARAMETER	MIN	MAX	UNITS
Ta	ALE Width	15		ns
Taw	ALE \ to WR* \	15		ns
Tar	ALE \ to RD* \	15		ns
Tw	WR* Width	110		ns
Tr	RD* Width	110		ns
As	Address valid to ALE \	5		ns
Ah	ALE \ to Address invalid	15		ns
Cs	ALE \ to CS /		5	ns
Ch	RD* / or WR* / to CS \	0		ns
Wds	Write Data valid to WR* /	25		ns
Wdh	WR* / to Write Data invalid	10		ns
Tda	RD* \ to Read Data valid		100	ns
Tdh	RD* / to Read Data invalid		50	ns
Tdrdy	ALE \ and CS / to LRDY*\		30	ns

Microcontroller Interface Timing

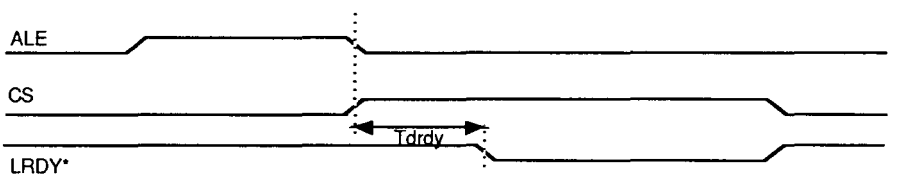
Register Write Timing



Register Read Timing



Ready Timing



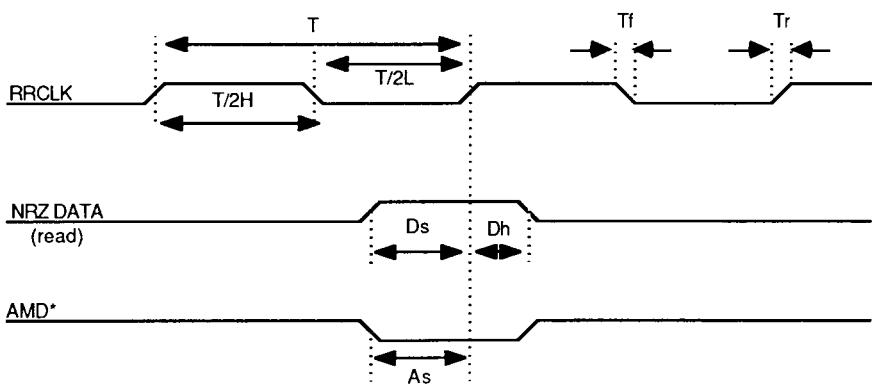
Disk Read/Write Timing Parameters

SYMBOL	PARAMETER	15 MHz (1) MIN	15 MHz (1) MAX	25 MHz (2) MIN	25 MHz (2) MAX	UNITS
T	RRCLK Period	62		40		ns
T/2H	RRCLK High Time	23		16		ns
T/2L	RRCLK Low Time	23		16		ns
Tr=Tf	RRCLK Rise and Fall Time		5		5	ns
Ds	NRZ In valid to RRCLK /	5		5		ns
Dh	RRCLK / to NRZ In valid	5		5		ns
As †	AMD* valid to RRCLK /	10		10		ns
Dv	RRCLK / to NRZ valid	10	25	10	25	ns
Wv †	RRCLK / to WAM* valid	10	25	10	25	ns

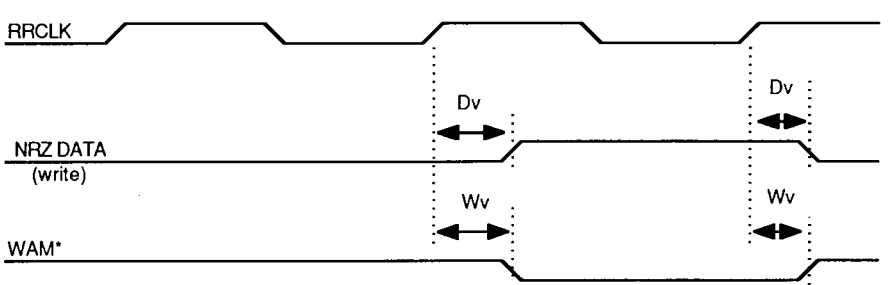
(1) The 15 MHz specification is with the RRCLK filter enabled (Register 4FH, Bit 4 = 0).
(2) The 25 MHz specification is with the RRCLK filter disabled (Register 4FH, Bit 4 = 1).

† These specifications are only applicable in the Soft Sector mode.

Disk Read Timing



Disk Write Timing

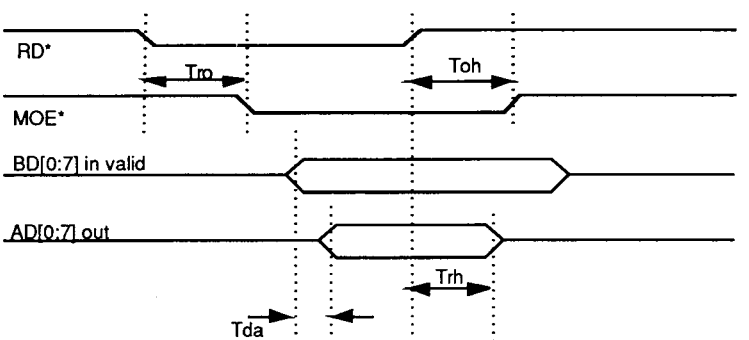


Register 70H Access Timing Parameters

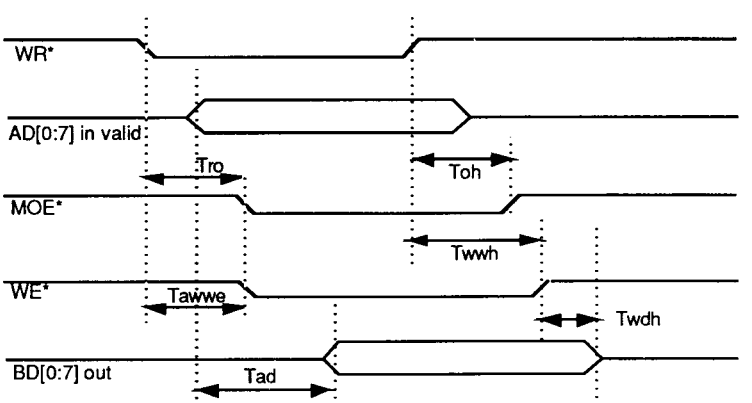
SYMBOL	PARAMETER	MIN	MAX	UNITS
Tro	RD* \ or WR* \ to MOE* \		40	ns
Tda	BD[0:7] In valid to AD[0:7] Out		45	ns
Trh	RD* / to AD[0:7] invalid		50	ns
Toh	RD* / or WR* / to MOE* /		40	ns
Tawwe	WR*\ to WE*\		40	ns
Tad	AD[0:7] In valid to BD[0:7] Out		55	ns
Twwh	WR* / to WE* /		40	ns
Twdh	WE* / to BD[0:7] Out invalid	10		ns

NOTE: BA [0:15] is valid from the previous cycles.

Register 70H Read Timing



Register 70H Write Timing



Buffer Memory Read/Write Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_B	BCLK Period	25		ns
$T_B/2$	BCLK High/Low Time	10		ns
$T_Br=T_Bf$	BCLK Rise and Fall Time		5	ns
Av	BCLK\ to Address valid		80	ns
Dov	Data Out valid to WE* /	1/2 BUFCLK Period -20		ns
Doh	WE* / to Data Out invalid	5		ns
Mh	MOE* / to Address Hold	5	30	ns
Wh	WE* / to Address Hold	5	30	ns
Dis	Data In valid to MOE* /	20		ns
Dih	MOE* / to Data In invalid	5		ns
Bacc	Buffer Access Period	1 BUFCLK Period		
Ww	WE* Low Time	1/2 BUFCLK Period		
Mw	MOE* Low Time	1/2 BUFCLK Period		

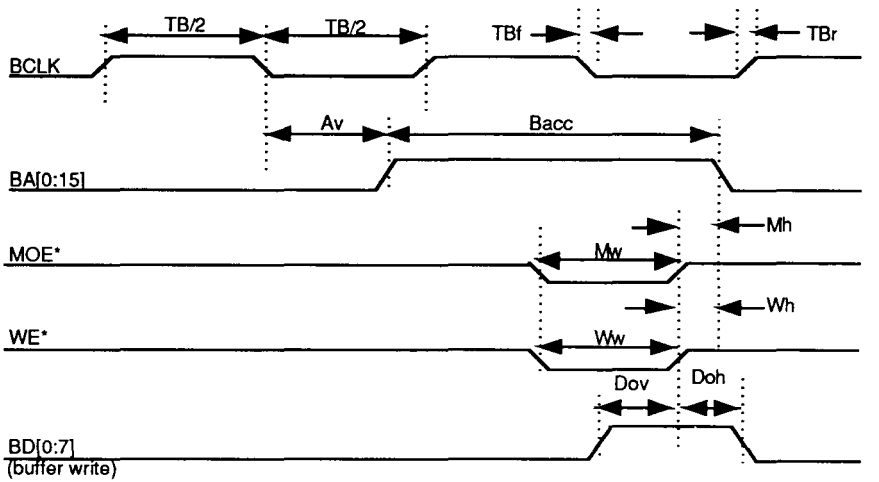
NOTE: BUFCLK is an internal Buffer Clock which indicates the period of Buffer Access Cycle. BUFCLK is derived from BCLK in appropriate divide by mode. The minimum Buffer Access Cycle (BUFCLK) is 100ns.

These specifications can be tested when the period of BCLK is the same as the period of Buffer Access Cycles (i.e., Register 7FH, Bits 6 and 7 are 0 and 1 respectively).

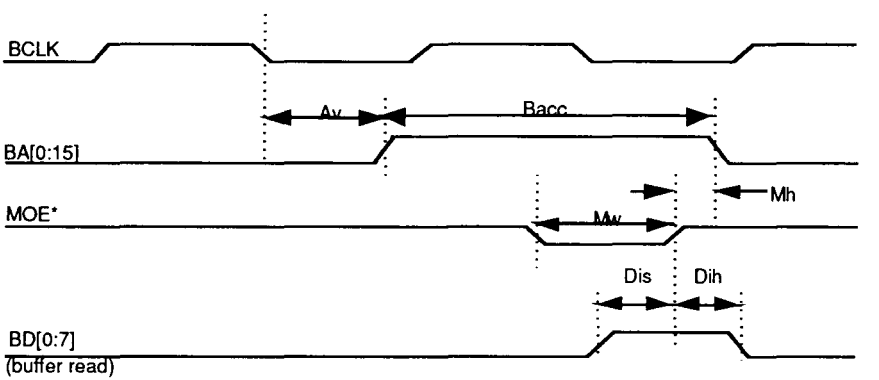
The Av parameter is used for test purposes only.

Buffer Memory Read/Write Timing

WRITING TO THE BUFFER

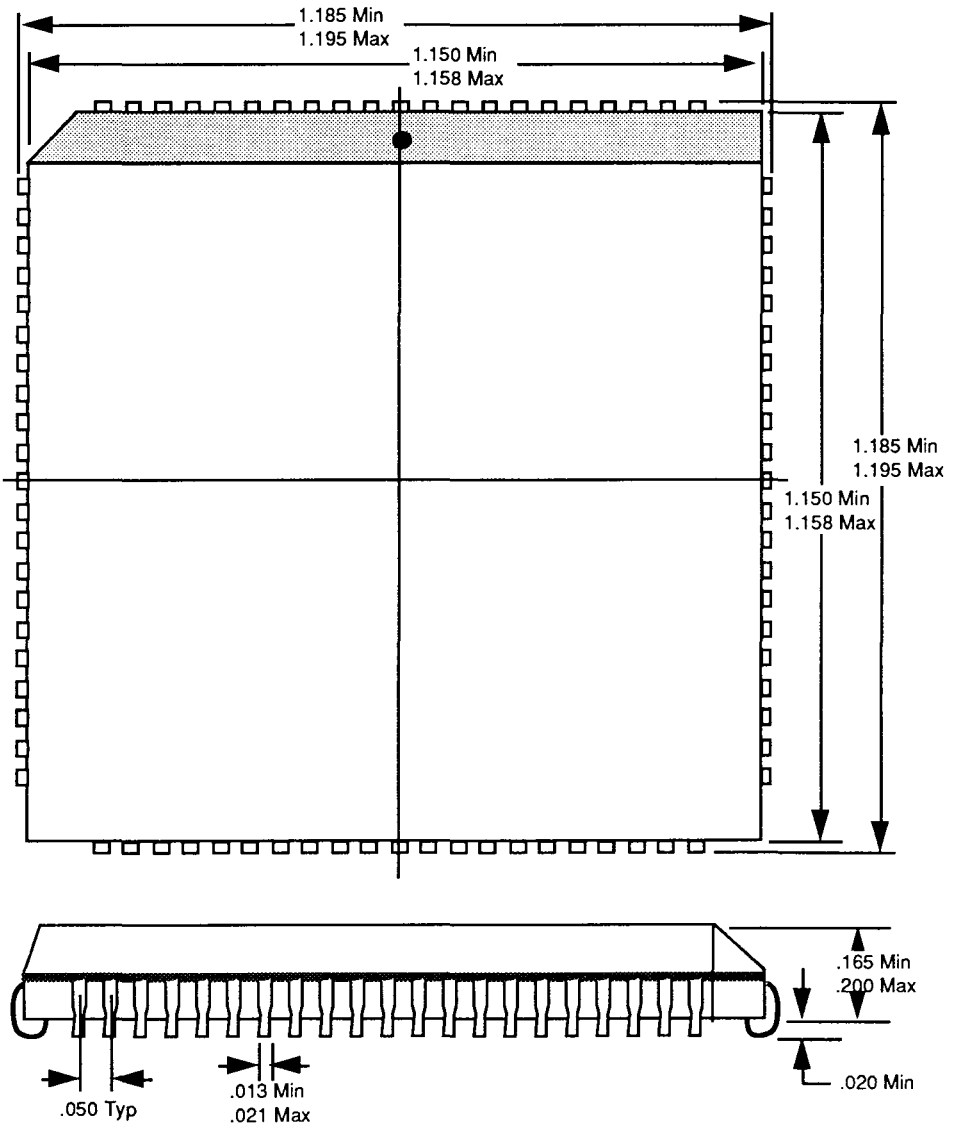


READING FROM THE BUFFER



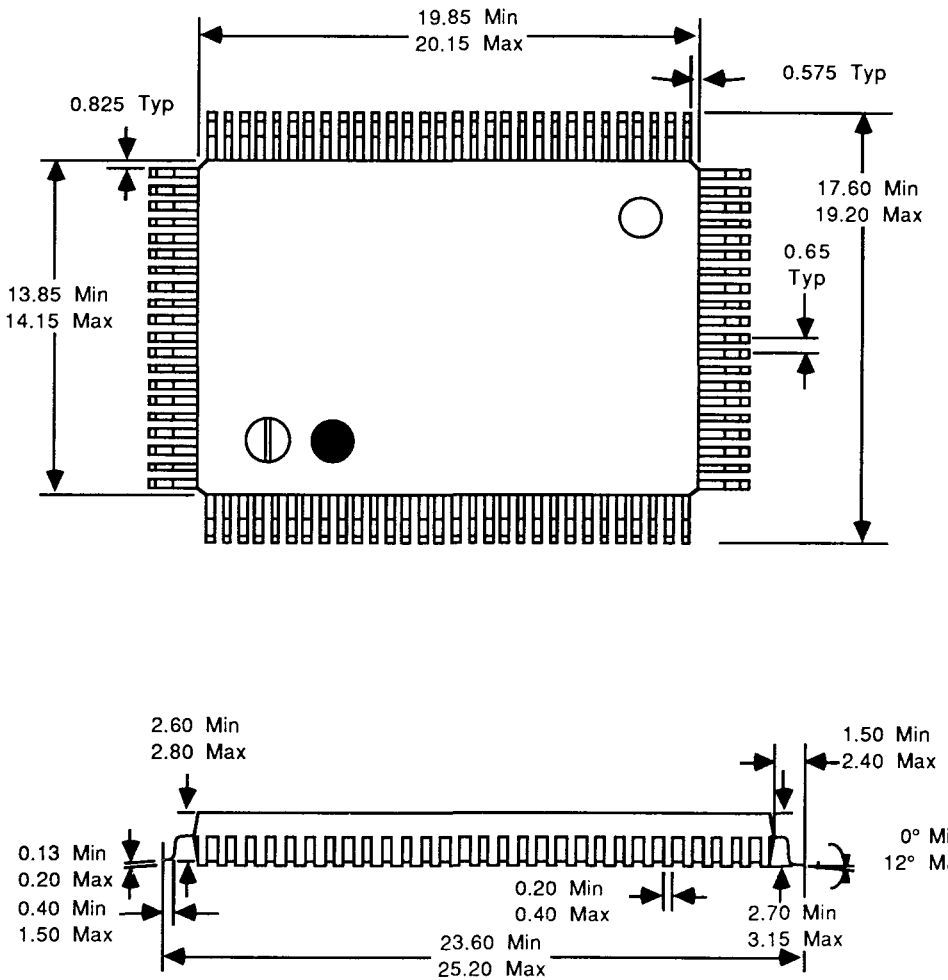
16. SAMPLE PACKAGE

16.1 84-Pin Plastic Leaded Chip Carrier (PLCC) Sample Package



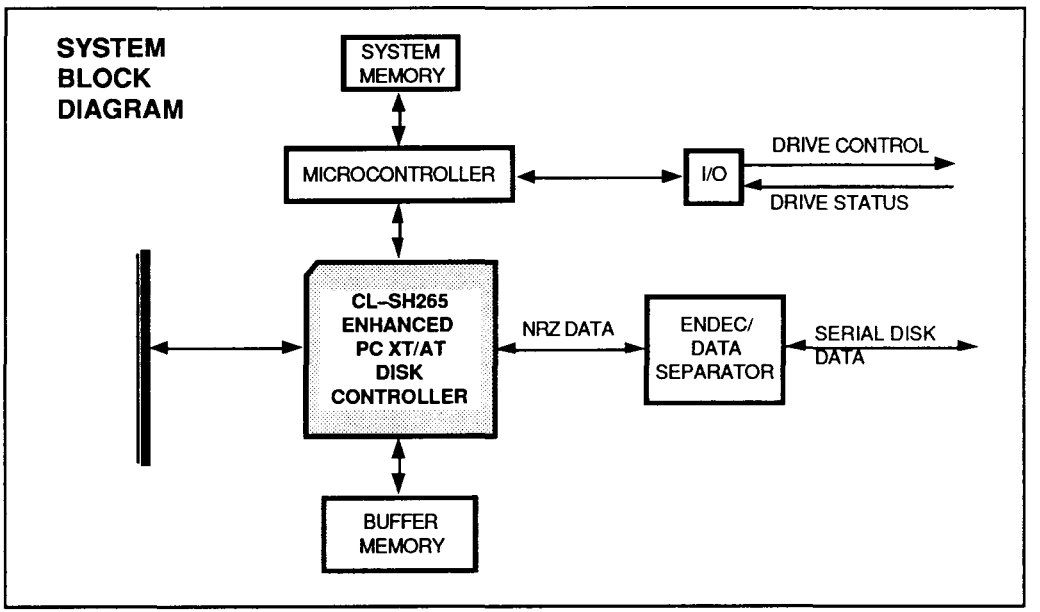
NOTE: Dimensions for the PLCC package are in inches.

16.2 100-Pin Quad Flat Pack (QFP) Sample Package



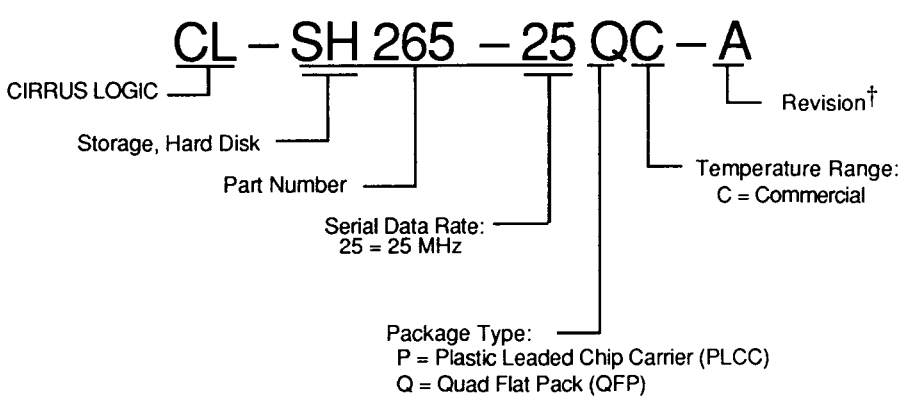
NOTE: Dimensions for the QFP package are in millimeters.

17. TYPICAL APPLICATION



18. ORDERING INFORMATION

CIRRUS LOGIC Numbering Guide



† Contact CIRRUS LOGIC for up-to-date information on revisions.

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

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Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

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