CL-GD543X/'4X

Preliminary Data Book

FEATURES

CL-GD543X/'4X Family

- **Pin- and software-compatible VGA graphics accelerators**
- **Integrated dual-clock synthesizer and 24-bit DAC**
  - — Pixel clock programmable to 135 MHz (CL-GD5434/'36), and to 86 MHz (CL-GD5430/'40)
  - — Memory clock programmable to 60 MHz (CL-GD5430/'34/'40), and to 80 MHz (CL-GD5436)
- **32-bit direct-connect CPU interface**
  - — PCI bus (v2.0) with burst-cycle support (CL-GD5436)
  - — VESA® VL-Bus™ (v2.0 with 50 MHz) (not CL-GD5436)
  - — ISA bus (12.5 MHz) (CL-GD5434 only)
  - — Zero-wait-state write buffer for CPUs to 33 MHz
- **64-bit DRAM display memory interface**
  - — 1-, 2-, and 4-Mbyte display memory support (CL-GD5434/'36)
  - — 1/2-, 1-, and 2-Mbyte display memory support (CL-GD5430/'40)
  - — Optimized EDO (extended data out) DRAM support (CL-GD5436)
- **64 × 64 hardware cursor**
- **Glueless PCI bus interface with VGA BIOS ROM support for single 8-bit EPROM**
- **Low-power 5-V CMOS, 208-pin PQFP package**

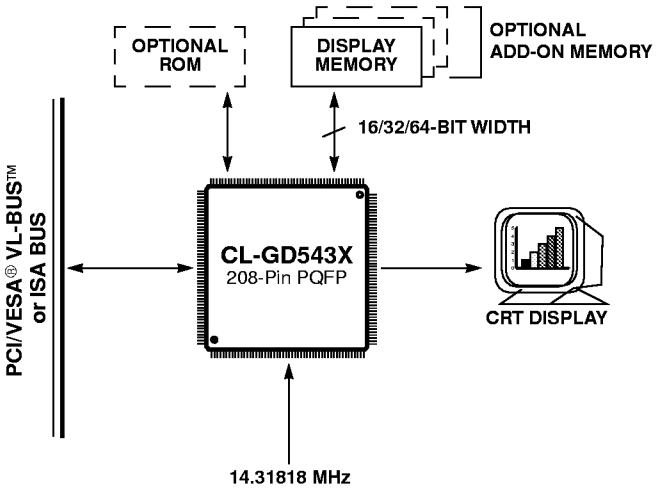
VGA GUI Accelerators

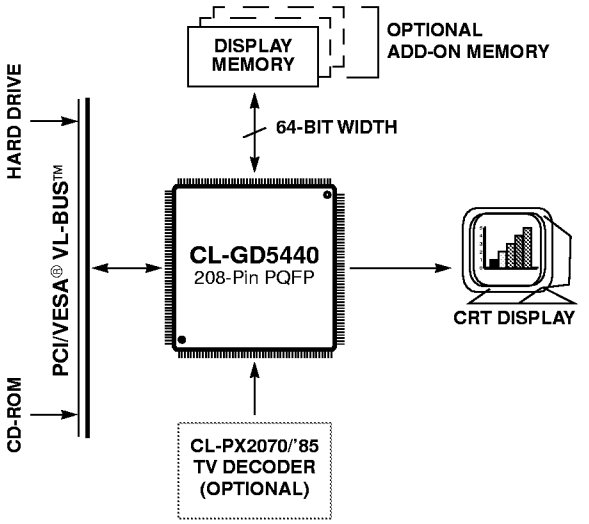
CL-GD5440	— Video Accelerator
CL-GD5434/'36	— 64-bit GUI Accelerators
CL-GD5430	— 32-bit GUI Accelerator

- **'Green PC' power-saving features**
  - — VESA® support for DPMS (display power-management signalling)
  - — Internal DAC with Power-Down mode
  - — Low-frequency DRAM refresh (CL-GD5430/'36/'40)
  - — Static monitor sync signals
- **100% hardware- and BIOS-compatible with IBM® VGA display standard**
- **Programmable dual-clock synthesizer**
- **Multimedia-ready *CL-GD5430/'34/'36***
  - — Video overlay with external video data and 'Color Keying'
  - — GENLOCK support with external HSYNC and/or VSYNC
  - — VAFC (VESA® advanced feature connector) Baseline support (CL-GD5430/'36)
  - — Horizontal pixel interpolation for baseline VAFC 2× mode (CL-GD5436)
- **CL-GD5428/'29 register- and software-compatible**

(cont.)

System Block Diagrams





DEVICE-SPECIFIC FEATURES

CL-GD5430/'34

- **Enhanced GUI acceleration**
  - — 64-bit BitBLT (bit block transfer) engine (CL-GD5434)
  - — 32-bit BitBLT engine (CL-GD5430)
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 64K colors, non-interlaced
  - — Up to 800 × 600 × 16M colors, non-interlaced
  - — Up to 1280 × 1024 × 256 colors, non-interlaced
- **VESA® DDC2B monitor support *(CL-GD5434)***
- **Integrated clock filter and current reference *(CL-GD5434-I)***

CL-GD5436

- **64-bit GUI acceleration**
  - — Double-buffered, memory-mapped BitBLT registers
  - — Color expansion for all data widths
  - — Efficient use of DRAM Fast-Page mode cycles
  - — Large BitBLT data buffers
- **Accelerated support for Packed-24 modes**
  - — Better performance than 32-bit true color
  - — Supports Microsoft® Windows® 95
  - — Allows 1024 × 768 × 16M colors at 85 Hz with DRAM
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 16M colors, non-interlaced
  - — Up to 1280 × 1024 × 256 colors, non-interlaced
- **Integrated clock filter and current reference**
- **PCI byte-swapping for PowerPC™**
- **VESA® DDC2B monitor support**

CL-GD5440

- **Cost-effective hardware-accelerated video playback**
  - — High-quality video playback from CD-ROM and disk-based files
  - — High-quality video playback in 256 and 64K color modes
  - — Indeo™ and Cinepack™ file playback to 30 fps
- **Continuous hardware-interpolated zoom (CD-Zoom™)**
  - — X-interpolated zoom from 1× to 4×
  - — Y-interpolated zoom from 2× to 4×
  - — Full-screen playback to 1024 × 768
- **Integrated color space converter**
  - — On-the-fly YUV-to-RGB conversion
  - — YUV 4:2:2 (CCIR601)
- **Error-diffusion filtering offers color enhancement for video**
  - — 'High color' quality playback in 8- and 16-bit color graphic modes
- **Unique 32-bit multimedia frame buffer**
  - — Video (YUV) and graphics (RGB) share one frame buffer
  - — Allows different color depths between video and graphics
  - — Full operation with 512-Kbyte, 1-Mbyte, or 2-Mbyte DRAM
- **Video data encoding reduces frame-buffer bandwidth requirement**
  - — High-quality video playback of 1024 × 768 in 256 colors, and 800 × 600 in 64K colors with only 1 Mbyte of DRAM
- **Resolutions to 1280 × 1024**
  - — Up to 1024 × 768 × 256 colors, non-interlaced
  - — Up to 800 × 600 × 64K colors, non-interlaced
  - — Up to 1280 × 1024 × 16 colors, interlaced
- **Direct TV-decoder interface**
- **VESA® DDC2B monitor support**
- **Integrated clock filter and current reference**

FAMILY OVERVIEW

Based on a 64-bit GUI engine, the CL-GD543X/'4X incorporates a BitBLT (bit block transfer) VGA controller with a 24-bit true-color DAC, dual-clock synthesizer, and direct-connect 32-bit PCI and VESA® VL-Bus™ interface. Optimized for Microsoft Windows®, Windows 95, Windows NT™, OS/2®, and other graphical interfaces, the Alpine family offers performance, surpassing current DRAM and many VRAM-based GUI accelerators.

The CL-GD543X/'4X forms the heart of a cost-effective, high-performance DRAM-based graphics system. By combining a 32-bit external local bus interface with a 64-bit path to the DRAM frame buffer, the CL-GD543X/'4X eliminates the video-memory bottleneck found in traditional DRAM architectures. This combination also maximizes system-to-video bandwidth critical for outstanding graphics acceleration.

BitBLT support, linear addressing, hardware cursor, color expansion, and memory-mapped I/O are some of the many built-in CL-GD543X/'4X features that ensure outstanding GUI performance. The internal palette DAC can be configured for industry-standard 16- or 256-color VGA modes, or extended to high- and true-color modes (32K, 64K, or 16M colors).

The CL-GD5434-I, CL-GD5436, and CL-GD5440-I devices have an integrated clock filter and current reference that allow a low-cost board solution.

The highly integrated 208-pin PQFP package makes the CL-GD543X/'4X ideal for both motherboard systems and add-in cards. The only external support needed is cost-effective DRAM memory and a 14.31818-MHz frequency reference.

CL-GD5430/'34

The software- and pin-compatible CL-GD5430/'34 allow OEMs to meet different price and performance targets with one graphic subsystem design. Built on a 1-Mbyte frame buffer, the CL-GD5430 can be quickly upgraded to the higher-performance CL-GD5434. With a 2-Mbyte frame buffer, the CL-GD5434 offers performance beyond current 32-bit standard and interleaved architectures.

Operating at pixel clock rates programmable to 135 MHz (CL-GD5434) and 86 MHz (CL-GD5430), the CL-GD543X devices supports standard and VESA high-resolution extended modes. Display resolutions up to 1280 × 1024 are supported.

CL-GD5436

The CL-GD5436 is a high-performance accelerated super VGA controller. The CL-GD5436 features a 64-bit BitBLT engine and a 64-bit display memory interface with support for EDO DRAMs.

Operating at pixel clock rates programmable to 135 MHz and memory clock rates programmable to 80 MHz, the CL-GD5436 supports resolutions and color depths at the following standard refresh rates:

Resolution	256 Colors	64K Colors	16M Colors
640 × 480	85 Hz	85 Hz	85 Hz
800 × 600	85 Hz	85 Hz	85 Hz
1024 × 768	85 Hz	85 Hz	85 Hz
1152 × 864	75 Hz	–	–
1280 × 1024	75 Hz	43i Hz	–

The CL-GD5436 supports Packed-24 RGB video modes, providing 16M colors at only 3 bytes per pixel. This allows 1024 × 768 true color at a 85-Hz refresh rate with DRAMs. The CL-GD5436 also supports three types of byte-swapping on the PCI bus, which provide PowerPC™ support.

CL-GD5440

The CL-GD5440 is the first product in its class to integrate on a single chip the CL-GD5430 (32-bit graphics accelerator) and the CL-PX2070/'85 video-processor accelerator (video technology from Pixel Semiconductor). Hardware-accelerated zoom with X and Y linear interpolation and color space conversion are combined with an enhanced BitBLT accelerator, integrated 24-bit RAMDAC, and a dual-clock synthesizer.

The CL-GD5440 accelerates both graphics and video playback for Microsoft Windows and Windows NT, OS/2, and other graphical interfaces. High-quality video playback is supported in both 64K, and the popular 256-color modes, allowing video playback without compromising graphics performance.

Operating at pixel clock rates programmable to 86 MHz, the CL-GD5440 supports standard and VESA high-resolution extended modes. Display resolutions up to 1280 × 1024 are supported.

A flexible 512-Kbyte to 2-Mbyte frame buffer, glueless PCI and VESA VL-Bus interface, and direct interface to NTSC/PAL decoder (and fully integrated video/graphics accelerator) provides OEMs with a cost-effective multimedia solution.

CD-Zoom, 'on-the-fly' color space conversion, video data encoding/decoding, and a multi-format frame buffer are integrated features that ensure high-performance video playback.

UNIQUE FEATURES

BENEFITS

Cost Effectiveness

- Interface to as few as one DRAM (CL-GD5430/'34/'40) or two DRAMs (CL-GD5434/'36), built-in true-color palette DAC and dual-frequency synthesizer
  - ❒ Minimizes chip count, system cost, and board space for cost-effective solution.
- Interface to ×4, ×8, ×16 DRAMs
  - ❒ Allows design flexibility for appropriate type and amount of memory.

High Performance

- Hardware BitBLT for Microsoft® Windows®
  - ❒ Accelerates GUIs such as Microsoft® Windows® and similar applications.
- 32-bit PCI, VESA® VL-Bus™, and local bus interface
  - ❒ Increases system throughput.
- 64-bit-wide DRAM interface (CL-GD5434/'36 only)
  - ❒ Eliminates display-memory bottleneck.
- Independent video and DRAM timing
  - ❒ Optimizes timing for increased performance.
- Maximum Fast-Page mode access to display-memory DRAMs
  - ❒ Improves CPU performance by accessing maximum bandwidth available from DRAM display memory.
- Host access to DRAMs through advanced write buffers
  - ❒ Provides fast host access for writes to display memory.
- EDO DRAM support (CL-GD5436)
  - ❒ Uses latest DRAM technology.
- 32-bit memory-mapped BitBLT Control registers
  - ❒ Improves graphics-application performance.
- 15-, 16-, or 24-bit true-color palette DAC
  - ❒ Provides high-color and true-color display for photo-realistic images. 32K, 64K, or 16M colors on screen at once for lifelike images.

Multimedia

- Overlay, color keying, and GENLOCK
  - ❒ Allows 16-bit-pixel interfacing through the VESA® connector for multimedia applications.

CL-GD5440–Specific

- Hardware-interpolated video zoom
  - ❒ Increases speed and quality of video playback at full screen.
- Single video-and-graphics frame buffer
  - ❒ Increases DRAM efficiency — RGB and YCrCb share one frame buffer.
- Hardware YUV-to-RGB conversion
  - ❒ Reduces CPU overhead with a multiformat frame buffer.
- Video data encoding converts 16-bit YUV pixels into 8-bit data
  - ❒ Reduces frame buffer bandwidth requirement.
- Vision Port™ enhanced feature connector
  - ❒ Enables CD-Zoom™ functionality on the VAFC or 8-bit standard feature connector; this eliminates need for an additional frame buffer and controller.
- Direct TV-decoder interface
  - ❒ Removes need for separate video frame buffer.

Compatibility

- Compatible with VGA and VESA® standards
  - ❒ Allows compatibility with installed base of systems and software.
- Drivers supplied at various resolutions for Windows® 3.1, Windows NT™, Windows® 95, AutoCAD7®, OS/2®, and other key applications
  - ❒ Provides a 'ready-to-go' solution that minimizes the need for additional driver development.
- Connects directly to IBM® PS/2® and multifrequency analog monitors
  - ❒ Drives all industry-standard, high-resolution PC-monitors to ensure compatibility.

SOFTWARE SUPPORT

CL-GD543X VGA Software Drivers

Cirrus Logic provides an extensive and expanding range of software drivers to enhance the resolution and performance of many software packages. However note, that the CL-GD543X/'4X VGA graphics portion of a system *does not* require software drivers to run applications in standard-resolution mode.

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® Windows® v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
Microsoft® Windows NT™ v3.1	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 and 256
Microsoft® Windows NT™ v3.5	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
Microsoft® Windows NT™ v3.5 for PowerPC™	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16 256 65,536
OS/2® v2.1, v2.1.1, v3.0	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536
	640 × 480	16.8 million
AutoCAD® v11, v12 Autoshade® v2.0 w/ Renderman, 3D Studio v1, v2	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	256
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	32,768
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536
	640 × 480, 800 × 600, 1024 × 768	16.8 million
WordStar® v5.5–7.0	800 × 600, 1024 × 768	16
SCO[b] UNIX®	640 × 480, 800 × 600, 1024 × 768	16 and 256

[a] All resolutions may not run on all monitor types; 640 × 480 drivers will run on IBM® PS/2®-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

[b] Shipped by Santa Cruz Operations.

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **Relocatable, 32 Kbytes with VESA® VL-Bus™ and PCI local bus support**
- **VBE (VESA® BIOS extensions) support in ROM**
- **Support for DPMS (display power management signaling) in ROM**
- **VESA® monitor timing-compliant**

UTILITIES

- **Manufacturing test**
- **Windows DOS utilities**
- **Video mode configuration utility — CLMODE**
- **Set resolution in Windows — WINMODE**
- **Configured OEM system integration — OEMSI**

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Revision History

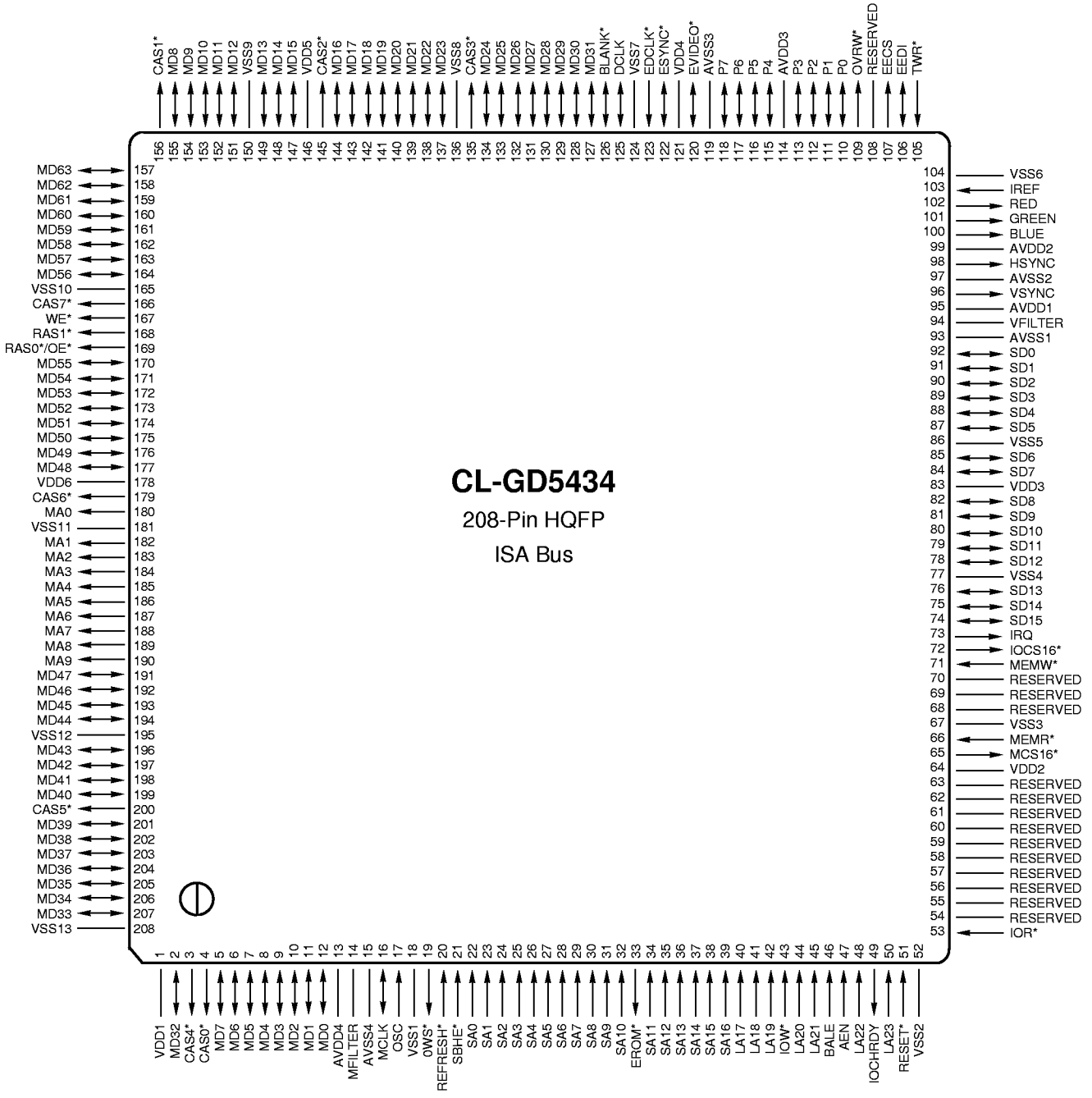
Major changes between the previons version of this data book, dated February 1995, and this version are:

- The CL-GD5436 now supports 85 Hz refresh rates.
- Figure 7-27 on page 3-84 and Figure 7-30 on page 3-88 present current timing information.

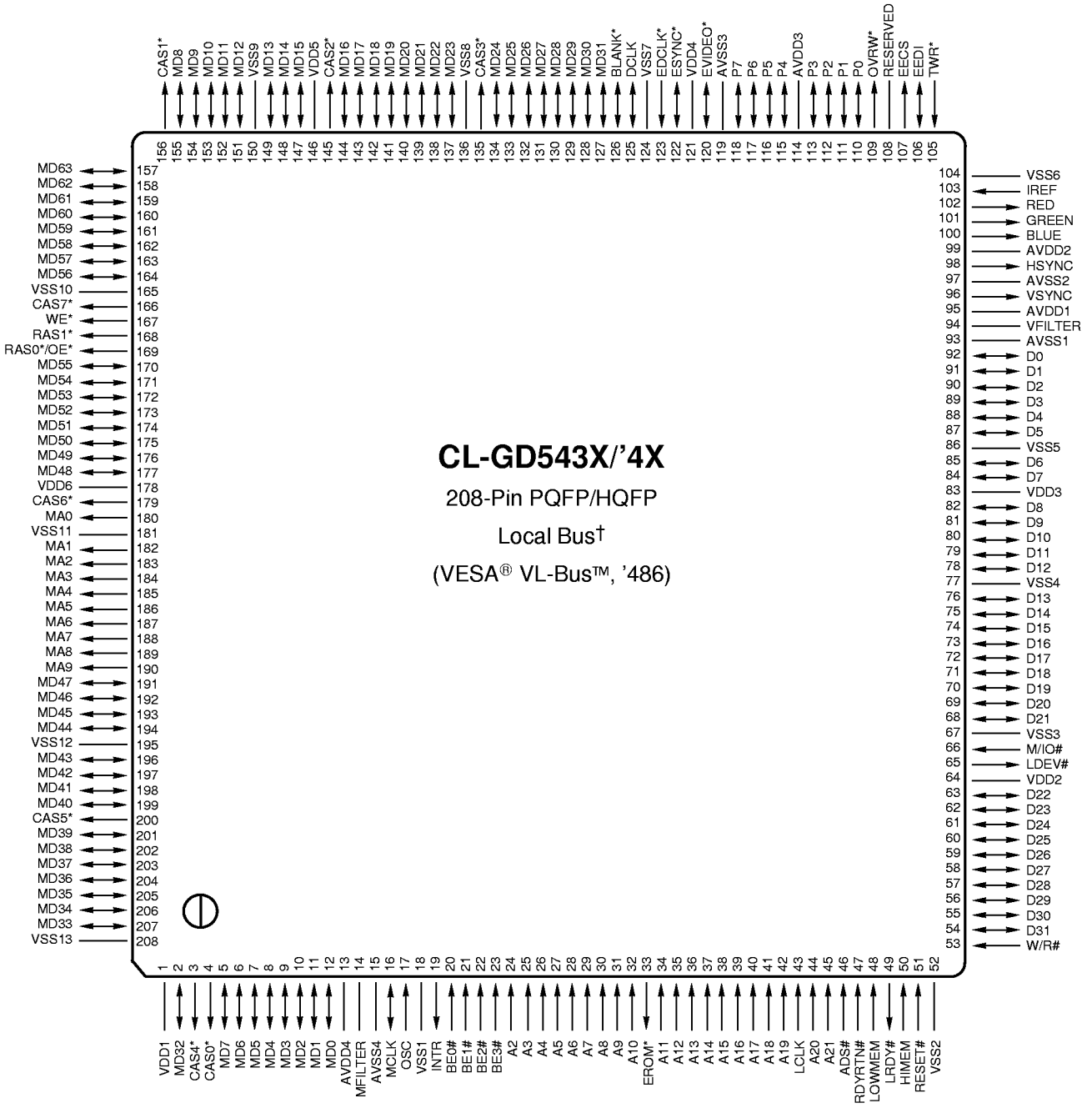
1. PIN INFORMATION

The CL-GD543X/'4X VGA GUI controllers are available in a 208-pin PQFP (plastic quad flat pack) or HQFP (high-performance quad flat pack) configuration. The CL-GD5430/'36/'40 devices can be configured for the VESA VL-Bus or PCI bus only. Additionally, the CL-GD5434 can be configured for the VESA VL-Bus, PCI, or ISA bus.

1.1 Pin Diagram — ISA Bus (CL-GD5434 Only)

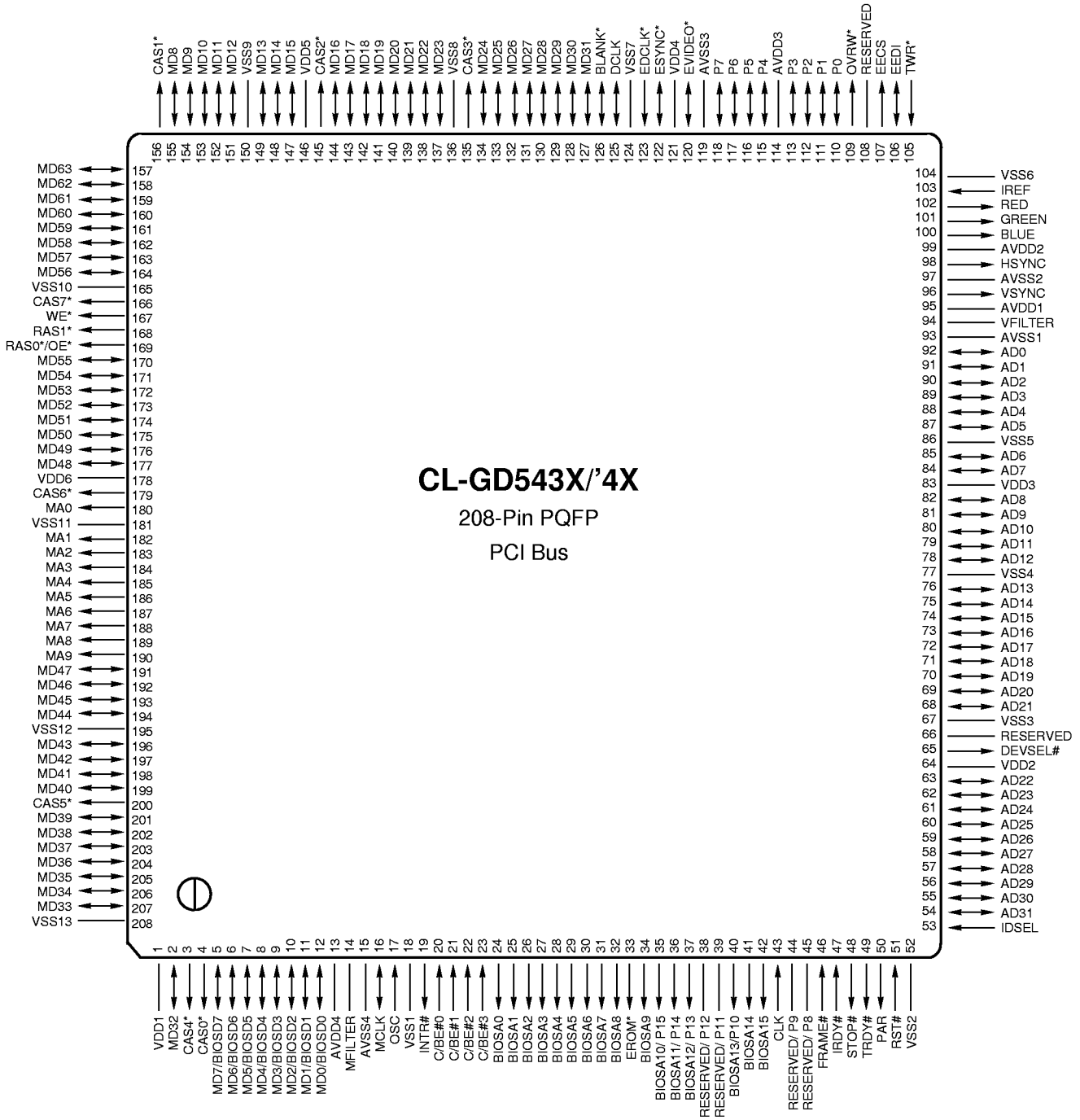


1.2 Pin Diagram — Local Bus (VESA® VL-Bus™, '486)



NOTE: † This pin diagram defines the pins forthe VESA VL-Bus and '486 local bus interfaces.

1.3 Pin Diagram — PCI Bus



1.4 Pin Summary

The following abbreviations are used for pin types in the following tables: (I) indicates input; (O) indicates output; (TS) indicates three-state; (OC) indicates open collector, I/O indicates input or output depending on how the device is configured.

Table 1-1. Host Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	VESA® VL-Bus™	PCI	ISA *(CL-GD5434 only)*
50	I					HIMEM	–	LA23
50	O		–3	8	240	–	PAR	–
48	I					LOWMEM	–	LA22
48	O		–3	8	240	–	STOP#	–
45	I					A21	Reserved/P8[b]	LA21
44	I					A20	Reserved/P9[b]	LA20
42	I/O		–3	8	50	A19	BIOSA15	LA19
41	I/O		–3	8	50	A18	BIOSA14	LA18
40	I/O		–3	8	50	A17	BIOSA13/P10[b]	LA17
39	I/O			8	50	A16	Reserved /P11[b]	SA16
38	I/O					A15	Reserved/P12[b]	SA15
37	I/O					A14	BIOSA12/P13[b]	SA14
36	I/O		–3	8	50	A13	BIOSA11/P14[b]	SA13
35	I/O		–3	8	50	A12	BIOSA10/P15[b]	SA12
34	I/O		–3	8	50	A11	BIOSA9	SA11
32	I/O		–3	8	50	A10	BIOSA8	SA10
31	I/O		–3	8	50	A9	BIOSA7	SA9
30	I/O		–3	8	50	A8	BIOSA6	SA8
29	I/O		–3	8	50	A7	BIOSA5	SA7
28	I/O		–3	8	50	A6	BIOSA4	SA6
27	I/O		–3	8	50	A5	BIOSA3	SA5
26	I/O		–3	8	50	A4	BIOSA2	SA4
25	I/O		–3	8	50	A3	BIOSA1	SA3
24	I/O		–3	8	50	A2	BIOSA0	SA2
23	I					BE3#	C/BE#3	SA1
22	I					BE2#	C/BE#2	SA0
54	I/O	❍[c]	–3	12	240	D31	AD31	Reserved
55	I/O	❍	–3	12	240	D30	AD30	Reserved
56	I/O	❍	–3	12	240	D29	AD29	Reserved
57	I/O	❍	–3	12	240	D28	AD28	Reserved
58	I/O	❍	–3	12	240	D27	AD27	Reserved
59	I/O	❍	–3	12	240	D26	AD26	Reserved
60	I/O	❍	–3	12	240	D25	AD25	Reserved
61	I/O	❍	–3	12	240	D24	AD24	Reserved

Table 1-1. Host Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	VESA® VL-Bus™	PCI	ISA *(CL-GD5434 only)*
62	I/O	❍	–3	12	240	D23	AD23	Reserved
63	I/O	❍	–3	12	240	D22	AD22	Reserved
68	I/O	❍	–3	12	240	D21	AD21	Reserved
69	I/O	❍	–3	12	240	D20	AD20	Reserved
70	I/O	❍	–3	12	240	D19	AD19	Reserved
71	I/O		–3	12	240	D18	AD18	MEMW*
72	I/O		–3	12	240	D17	AD17	IOCS16*
73	I/O		–3	12	240	D16	AD16	IRQ
74	I/O		–3	12	240	D15	AD15	SD15
75	I/O		–3	12	240	D14	AD14	SD14
76	I/O		–3	12	240	D13	AD13	SD13
78	I/O		–3	12	240	D12	AD12	SD12
79	I/O		–3	12	240	D11	AD11	SD11
80	I/O		–3	12	240	D10	AD10	SD10
81	I/O		–3	12	240	D9	AD9	SD9
82	I/O		–3	12	240	D8	AD8	SD8
84	I/O		–3	12	240	D7	AD7	SD7
85	I/O		–3	12	240	D6	AD6	SD6
87	I/O		–3	12	240	D5	AD5	SD5
88	I/O		–3	12	240	D4	AD4	SD4
89	I/O		–3	12	240	D3	AD3	SD3
90	I/O		–3	12	240	D2	AD2	SD2
91	I/O		–3	12	240	D1	AD1	SD1
92	I/O		–3	12	240	D0	AD0	SD0
21	I					BE1#	C/BE#1	SBHE*
20	I					BE0#	C/BE#0	REFRESH*
46	I					ADS#	FRAME#	BALE
47	I	●				RDYRTN#	IRDY#	AEN
53	I					W/R#	IDSEL	IOR*
43	I					LCLK	CLK	IOW*
66	I	●				M/IO#	Reserved	MEMR*
51	I					RESET#	RST#	RESET*[d]
49	TS		–3	8	240	LRDY#	TRDY#	IOCHRDY
65	O		–3	24	200	LDEV#	DEVSEL#	MCS16*
19	TS		(OC)	24	200	INTR	INTR#	0WS*

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

[b] For the CL-GD5436 only, pins 35:40,44,45 can be redefined as P[15:8] inputs.

[c] ❍ indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor when the CL-GD5434 is configured for ISA bus.

[d] An inverter is required to generate an active-low RESET* for ISA bus.

Table 1-2. Clock Synthesizer Interface

Pin Number	Pin Type	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
17	I				OSC
14	Analog				MFILTER
94	Analog				VFILTER
16	I/O	–12	12	20	MCLK

Table 1-3. Video Interface

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
96	TS		–12	24	50	VSYNC
98	TS		–12	24	50	HSYNC
126	I/O		–12	12	50	BLANK*
35	I/O		–3	8	50	P15[b]
36	I/O		–3	8	50	P14[b]
37	I/O		–3	8	50	P13[b]
38	I/O		–3	8	50	P12[b]
39	I/O		–3	8	50	P11[b]
40	I/O		–3	8	50	P10[b]
44	I/O		–3	8	50	P9[b]
45	I/O		–3	8	50	P8[b]
118	I/O		–12	12	50	P7
117	I/O		–12	12	50	P6
116	I/O		–12	12	50	P5
115	I/O		–12	12	50	P4
113	I/O		–12	12	50	P3
112	I/O		–12	12	50	P2
111	I/O		–12	12	50	P1
110	I/O		–12	12	50	P0
125	I/O		–12	12	50	DCLK
122	I/O	●	–12	12		ESYNC* [c]
120	I/O	●	–12	12		EVIDEO* [d]
123	In	●				EDCLK*
102	Analog Out					RED
101	Analog Out					GREEN
100	Analog Out					BLUE
103	Analog In					IREF

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

[b] For the CL-GD5436 only, P[15:8] are redefined PCI pins. See the definition of register GR18[6].

[c] ESYNC* is redefined as EEPROM SK if EEPROM interface is enabled.

[d] EVIDEO* is redefined as EEPROM DI if EEPROM interface is enabled.

Table 1-4. Display Memory Interface

Pin Number	Pin Type	Pull-up [a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
168	O		–12	12	50	RAS1*
169	O		–12	12	50	RAS0*/OE*
166	O		–12	12	50	CAS7* [b]
179	O		–12	12	50	CAS6* [b]
200	O		–12	12	50	CAS5* [b]
3	O		–12	12	50	CAS4* [b]
135	O		–12	12	50	CAS3* [b]
145	O		–12	12	50	CAS2* [b]
156	O		–12	12	50	CAS1* [b]
4	O		–12	12	50	CAS0* [b]
167	O		–12	12	150	WE* [c]
190	O		–12	12	150	MA9
189	O		–12	12	150	MA8 [d]
188	O		–12	12	150	MA7
187	O		–12	12	150	MA6
186	O		–12	12	150	MA5
185	O		–12	12	150	MA4
184	O		–12	12	150	MA3
183	O		–12	12	150	MA2
182	O		–12	12	150	MA1
180	O		–12	12	150	MA0 [e]
157	I/O	●	–8	8	50	MD63
158	I/O	●	–8	8	50	MD62
159	I/O	●	–8	8	50	MD61
160	I/O	●	–8	8	50	MD60
161	I/O	●	–8	8	50	MD59
162	I/O	●	–8	8	50	MD58
163	I/O	●	–8	8	50	MD57
164	I/O	●	–8	8	50	MD56
170	I/O	●	–8	8	50	MD55
171	I/O	●	–8	8	50	MD54
172	I/O	●	–8	8	50	MD53
173	I/O	●	–8	8	50	MD52
174	I/O	●	–8	8	50	MD51
175	I/O	●	–8	8	50	MD50
176	I/O	●	–8	8	50	MD49
177	I/O	●	–8	8	50	MD48
191	I/O	●	–8	8	50	MD47
192	I/O	●	–8	8	50	MD46

Table 1-4. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
193	I/O	●	–8	8	50	MD45
194	I/O	●	–8	8	50	MD44
196	I/O	●	–8	8	50	MD43
197	I/O	●	–8	8	50	MD42
198	I/O	●	–8	8	50	MD41
199	I/O	●	–8	8	50	MD40
201	I/O	●	–8	8	50	MD39
202	I/O	●	–8	8	50	MD38
203	I/O	●	–8	8	50	MD37
204	I/O	●	–8	8	50	MD36
205	I/O	●	–8	8	50	MD35
206	I/O	●	–8	8	50	MD34
207	I/O	●	–8	8	50	MD33
2	I/O	●	–8	8	50	MD32
127	I/O	●	–8	8	50	MD31
128	I/O	●	–8	8	50	MD30
129	I/O	●	–8	8	50	MD29
130	I/O	●	–8	8	50	MD28
131	I/O	●	–8	8	50	MD27
132	I/O	●	–8	8	50	MD26
133	I/O	●	–8	8	50	MD25
134	I/O	●	–8	8	50	MD24
137	I/O	●	–8	8	50	MD23
138	I/O	●	–8	8	50	MD22
139	I/O	●	–8	8	50	MD21
140	I/O	●	–8	8	50	MD20
141	I/O	●	–8	8	50	MD19
142	I/O	●	–8	8	50	MD18
143	I/O	●	–8	8	50	MD17
144	I/O	●	–8	8	50	MD16
147	I/O	●	–8	8	50	MD15
148	I/O	●	–8	8	50	MD14
149	I/O	●	–8	8	50	MD13
151	I/O	●	–8	8	50	MD12
152	I/O	●	–8	8	50	MD11
153	I/O	●	–8	8	50	MD10
154	I/O	●	–8	8	50	MD9
155	I/O	●	–8	8	50	MD8
5	I/O	●	–8	8	50	MD7/BIOSD7[f]

Table 1-4. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
6	I/O	●	–8	8	50	MD6/BIOSD6[f]
7	I/O	●	–8	8	50	MD5/BIOSD5[f]
8	I/O	●	–8	8	50	MD4/BIOSD4[f]
9	I/O	●	–8	8	50	MD3/BIOSD3[f]
10	I/O	●	–8	8	50	MD2/BIOSD2[f]
11	I/O	●	–8	8	50	MD1/BIOSD1[f]
12	I/O	●	–8	8	50	MD0/BIOSD0[f]

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.
[b] CAS[7:0]* are redefined as WE[7:0]* for dual-WE* 256K × 16 DRAMs.
[c] WE* is redefined as CAS* for dual-WE* 256K × 16 DRAMs.
[d] MA8 is connected to Memory Address 0 for asymmetric DRAMs.
[e] MA0 is connected to Memory Address 8 for asymmetric DRAMs.
[f] For the PCI bus, MD[7:0] can also be configured as BIOSD[7:0].

Table 1-5. Miscellaneous Pins

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
107	O		–12	12	35	EECS
106	I/O		–12	12	35	EEDI
33	O		–12	12	35	EROM*
109	O		–12	12	35	OVRW*
105	I	●				TWR*
108	–					Reserved

[a] ● indicates the presence of an internal 250 kΩ +/– 50% pull-up resistor.

Table 1-6. Power and Ground

Pin Number	Pin Type	Name	Note
178	Power	VDD6	Digital
146	Power	VDD5	Digital
121	Power	VDD4	Digital
83	Power	VDD3	Digital
64	Power	VDD2	Digital
1	Power	VDD1	Digital
208	Ground	VSS13	Digital
195	Ground	VSS12	Digital
181	Ground	VSS11	Digital
165	Ground	VSS10	Digital
150	Ground	VSS9	Digital
136	Ground	VSS8	Digital
124	Ground	VSS7	Digital
104	Ground	VSS6	Digital
86	Ground	VSS5	Digital
77	Ground	VSS4	Digital
67	Ground	VSS3	Digital
52	Ground	VSS2	Digital
18	Ground	VSS1	Digital
95	Power	AVDD1	VCLK
93	Ground	AVSS1	VCLK
13	Power	AVDD4	MCLK
15	Ground	AVSS4	MCLK
114	Power	AVDD3	DAC
99	Power	AVDD2	DAC
119	Ground	AVSS3	DAC
97	Ground	AVSS2	DAC

2. DETAILED PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections: (I) indicates input, (O) indicates output, (TS) indicates three-state, (OC) indicates open collector, I/O indicates input or output depending on how the chip is configured.

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only)

Name	Type	Description
LA[23:17]	I	**ADDRESS [23:17]:** These inputs, in conjunction with SA[16:0], are used to select the resource to be accessed during memory operations. These address bits are latched with the falling edge of BALE.
SA[16:0]	I	**ADDRESS [16:0]:** These inputs, in conjunction with LA[23:17], are used to select the resource to be accessed during any memory or I/O operation. These address bits must remain valid throughout the cycle.
SD[15:8]	TS	**SYSTEM DATA [15:8]:** These bidirectional pins are used to transfer data during 16-bit memory or I/O operations. These pins can be connected directly to the corresponding ISA bus pins.
SD[7:0]	TS	**SYSTEM DATA [7:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins can be connected directly to the corresponding ISA bus pins.
SBHE*	I	**SYSTEM BYTE HIGH ENABLE*:** This input is used in conjunction with A0 to determine the width and alignment of a data transfer. SBHE* and A0 are decoded as shown in Table 2-1 below:
BALE	I	**BUS ADDRESS LATCH ENABLE:** This active-high input is used to latch LA[23:17] on the high-to-low transition.
AEN	I	**ADDRESS ENABLE:** If this input is high, it indicates that the current cycle is a DMA cycle. In this case, the CL-GD5434 will not respond to I/O cycles. There is no effect on memory cycles.

Table 2-1. SBHE*/A0 Decoding

SBHE*	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer
1	1	Lower-byte Transfer *(on odd address)*

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
IOR*	I	**I/O READ*:** This active-low input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD5434, it will respond by placing the contents of the appropriate register on the System Data bus.
IOW*	I	**I/O WRITE*:** This active-low input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD5434, it will respond by transferring the contents of the System Data bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal. A list of I/O addresses to which the CL-GD5434 will respond appears in Section 5, "VGA Register Port Map". When a 16-bit I/O write is done, the address specified will be the Index register for one of the VGA groups. The index must appear on SD[7:0] and the data must appear on SD[15:8].
MEMR*	I	**MEMORY READ*:** This active-low input is used to indicate that a memory read is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMR*. If linear addressing is not being used, this pin can be connected to ISA signal SMEMR*. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a display memory read is occurring. If so, data is placed on the System Data pins according to the Read mode and the contents of display memory. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a BIOS read is occurring. If so, the CL-GD5434 makes EROM* active for the duration of MEMR*.
MEMW*	I	**MEMORY WRITE*:** This active-low input is used to indicate that a memory write is occurring. If linear addressing is being used, this pin must be connected to ISA signal MEMW*. If linear addressing is not being used, this pin can be connected to ISA signal SMEMW*. The CL-GD5434 decodes LA[23:17] and SA[16:15] to determine if a display memory write is occurring. If so, data is written into display memory according to the Write mode and the data on SD[15:0]. The data is latched in the CL-GD5434 on the rising edge of this signal, and is actually transferred to display memory later.
RESET*	I	**RESET*:** This active-low signal is used to initialize the CL-GD5434 to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors. An inverter is required to generate an active-low RESET*.
REFRESH*	I	**REFRESH*:** This active-low signal indicates that a DRAM refresh is occurring. The CL-GD5434 ignores memory read operations occurring when REFRESH* is active since it explicitly controls the refresh of display memory.

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
IOCHRDY	TS	**I/O CHANNEL READY:** This output, when driven low, indicates that additional wait states are to be inserted into the current display memory read or write cycle. This output is never driven low during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven low as soon as MEMR* goes active. When the data are ready to be placed on the System Data bus, this signal is driven high. It remains high until MEMR* goes inactive; it then goes high-impedance. During a display memory write cycle, this signal is driven high as soon as MEMW* goes active if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven low as soon as MEMW* goes active and remains low until there is space. Once there is space in the Write Buffer, this signal is driven high. It will remain high until MEMW* goes inactive; it then goes high-impedance.
IOCS16*	OC	**I/O CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD5434 can execute an I/O operation at the address currently on the bus in 16-bit mode. This signal is generated from a decode of SA[15:0] and AEN. Table 2-2 indicates the range of addresses for which the CL-GD5434 will generate IOCS16*:

Table 2-2. IOCS16* Addresses

Address	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics controller
3B4/3D4, 3B5/3D5	CRT controller
3BA/3DA	Input Status register 1

2.1 Host Interface — ISA Bus Mode (CL-GD5434 only) *(cont.)*

Name	Type	Description
MCS16*	OC	**MEMORY CHIP SELECT 16*:** This open-collector output is driven low to indicate that the CL-GD5434 can execute a memory operation at the address currently on the bus in 16-bit mode. Table 2-3 summarizes the conditions under which MCS16* is made active.

Table 2-3. MSC16* Addresses

Resource	Address Bits	Address Range	Qualifier
Display Memory	LA[23:17]	A000:0–BFFF:F	SR8[6] = 0 (No other VGA card)
Display Memory	LA[23:17]	1–4 Mbyte	SR7[7:4] ≠ 0 Linear Addressing
BIOS	LA[23:17] and SA[16:15]	C000:0–C7FF:F	CF[6] = 0 (16-bit BIOS)

NOTE: The SA bits are generated late, and cannot be used for generating MCS16* unless special provisions are made. The CL-GD5434 uses a fast path from SA[16:15] to MCS16*.

0WS*	OC	**ZERO WAIT STATE*:** This open-collector output is driven low to indicate that the current cycle can be completed without any additional wait states. This is typically connected to SRDY* with a jumper.
IRQ	TS	**INTERRUPT REQUEST:** This active-high output indicates the CL-GD5434 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically unused in PC/AT add-in cards, but can be connected to IRQ2/IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin.

2.2 Host Interface — Local Bus Mode

A number of bus interface pins are redefined according to the local bus type to which the CL-GD543X/'4X is connected. VESA VL-bus is not supported by the CL-GD5436. These are listed in Table 2-4, which is ordered by CL-GD543X/'4X pin number.

Table 2-4. Redefined Host Interface Pins

Pin Number	VESA® VL-Bus™	PCI™
20	BE0#	C/BE#0
21	BE1#	C/BE#1
22	BE2#	C/BE#2
23	BE3#	C/BE#3
43	LCLK	CLK
46	ADS#	FRAME#
47	RDYRTN#	IRDY#
48	LOWMEM	STOP#
49	LRDY#	TRDY#
50	HIMEM	PAR
51	RESET#	RST#
53	W/R#	IDSEL
65	LDEV#	DEVSEL#
66	M/IO#	LOCK#

2.2.1 VESA® VL-Bus™ and '486 Bus Interface (CL-GD5430/'34/'40 only)

Name	Type	Description
HIMEM	I	**HIGH MEMORY:** This active-high input signal is used in conjunction with LOWMEM to indicate the address space being used. See Table 2-5 with LOWMEM.
LOWMEM	I	**LOW MEMORY:** This active-high input signal is used in conjunction with HIMEM to indicate the address space being used as defined in Table 2-5.
A[21:2]	I	**ADDRESS [21:2]:** These inputs are used to select the resource to be accessed during memory or I/O operation. A[21:17] have internal pull-up resistors; A[16:2] do not.
D[31:0]	TS	**DATA[31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. These pins are directly connected to D[31:0] of the VESA VL-Bus or the '486 bus.
BE[3:0]#	I	**BYTE ENABLE [3:0]#:** These active-low inputs are connected directly to the VESA VL-Bus or the '486 Byte Enable outputs. BE0# applies to byte 0 and BE3# to byte 3.
ADS#	I	**ADDRESS STROBE#:** This active-low input indicates that a new cycle has begun. It must be connected directly to the ADS# pin on the VESA VL-Bus or the '486 bus.

Table 2-5. Memory Area

HIMEM	LOWMEM	Comments
0	0	No response
0	1	Standard VGA Map A000:0–BFFF:F SR7[7:4] = 0
1	0	No response
1	1	Linear display memory SR7[7:4] ≠ 0

2.2.1 VESA® VL-Bus™ and '486 Bus Interface (CL-GD5430/'34/'40 only) *(cont.)*

Name	Type	Description
RDYRTN#	I	**READY RETURN#:** This input establishes a handshake between the CL-GD543X/'4X and VESA VL-Bus, so the CL-GD543X/'4X is informed when the cycle has ended. RDYRTN# is typically asserted in the same LCLK cycle as LRDY# is asserted. If LCLK is higher than 33 MHz, RDYRTN# may trail LRDY# by one LCLK cycle. During DMA or system I/O bus master signals, RDYRTN# is asserted for one LCLK cycle when the DMA or system I/O bus masters command ends. This pin is connected to RDYRTN# of the VESA VL-Bus.
LRDY#	TS	**READY#:** This active-low signal is used as an output to terminate a CL-GD543X/'4X bus cycle. This pin is connected to LRDY# for the VESA VL-Bus and RDY# of the '486 bus.
W/R#	I	**WRITE/READ#:** This input indicates whether a write or read operation is to occur. It must be connected directly to the W/R# pin on the CPU or VESA bus. If W/R# is high, a write will occur. If W/R# is low, a read will occur.
M/IO#	I	**MEMORY/IO#:** This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO# pin on the CPU or VESA bus. If M/IO# is high, a memory operation will occur. If it is low, an I/O operation will occur.
LCLK	I	**CLOCK:** This input is the timing reference for the CL-GD543X/'4X. It must be connected directly to the corresponding CPU Clock pin. For VESA VL-Bus, this pin is connected to LCLK. For '486 bus, this pin is connected to CLK.
RESET#	I	**RESET#:** This active-low input initializes the CL-GD543X/'4X to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors.
LDEV#	O	**LOCAL DEVICE#:** This open-collector output is driven low to indicate that the CL-GD543X/'4X will respond to the current cycle. This pin is connected to LDEV#.
INTR	TS	**INTERRUPT REQUEST:** This active-high output indicates that CL-GD543X/'4X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of controls for this pin.

2.2.2 PCI Bus Interface

Name	Type	Description
PAR	TS	**PARITY:** This signal provides even parity across AD[31:0] and C/BE#[3:0]. The CL-GD543X/'4X will sample this signal during write cycles and assert the correct parity for read cycles to the CL-GD543X/'4X.
STOP#	TS	**STOP#:** This active-low output indicates a current request to the PCI Bus Master to stop the current transaction.
AD[31:0]	TS	**ADDRESS AND DATA [31:0]:** These multiplexed and bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI bus. These pins directly connect to AD[31:0] of the PCI bus Interface. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data.
BIOSA[15:0]	O/I	**BIOS ADDRESS [15:0]:** These output pins are latched from the AD[31:0] bus, and are used to address the video system BIOS. These signals are directly connected to the address inputs of the 8-bit ROM. BIOSA[13:10] can be redefined as Pixel bus inputs, P10–P15, for the the CL-GD5436.
BIOSD[7:0]	I	**BIOS DATA [7:0]:** These input pins are used to transfer data during a video system BIOS operation. These pins are directly connected to data outputs of an 8-bit ROM. These pins are multiplexed with MD[7:0].

2.2.2 PCI™ Bus Interface *(cont.)*

Name	Type	Description
C/BE#[3:0]	–	**COMMAND AND BYTE ENABLE#[3:0]:** These multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI bus. These pins directly connect to C/BE#[3:0] of the PCI bus interface. During the address phase of the operation, C/BE#[3:0] define the bus command (refer to the Table 2-6). During the data phase, they are used as Byte Enable outputs. C/BE#0 applies to byte 0 and C/BE#3 applies to byte 3.
FRAME#	I	**FRAME#:** This active-low input indicates the beginning and duration of an access. FRAME# will be asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. The transaction is in its final data phase when FRAME# is deasserted.

Table 2-6. Command and Byte Enable

C/BE#3	C/BE#2	C/BE#1	C/BE#0	Command Type	Comments
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Valid
0	0	1	1	I/O Write	Valid
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Valid
0	1	1	1	Memory Write	Valid
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Valid
1	0	1	1	Configuration Write	Valid
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.2.2 PCI™ Bus Interface *(cont.)*

Name	Type	Description
IRDY#	I	**INITIATOR READY#:** This input establishes a handshake between the CL-GD543X/'4X and PCI bus so the CL-GD543X/'4X is informed when the cycle has ended. Wait states are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	TS	**TARGET READY#:** This active-low signal is used as an output to terminate a CL-GD543X/'4X bus cycle. This pin is connected to TRDY# for the PCI bus.
IDSEL	I	**INITIALIZATION DEVICE SELECT:** This input signal is used as a chip select in lieu of the upper 24 address lines during configuration read and write cycles.
CLK	I	**CLOCK:** This is the timing reference for the CL-GD543X/'4X when connected to a local bus. It must be connected directly to the CLK pin of the PCI bus.
RST#	I	**RESET#:** This active-low input initializes the CL-GD543X/'4X to a known state. The trailing (rising) edge of this input loads the Configuration register CF[15:0] with the data on MD[63:48], determined by internal pull-up resistors and optional external pull-down resistors.
DEVSEL#	TS	**DEVICE SELECT#:** This open-collector output is driven low to indicate that the CL-GD543X/'4X will respond to the current cycle. This pin is connected to DEVSEL# of the PCI bus.
INTR#	TS	**INTERRUPT REQUEST#:** This active-low output indicates that CL-GD543X/'4X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of controls for this pin.

2.3 Dual-Frequency Synthesizer Interface

Name	Type	Description
OSC	I	**OSCILLATOR INPUT:** This TTL-input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 ± 0.01% MHz with a duty cycle of 50 ± 10%. This input can be supplied from the appropriate pin on the ISA bus, or from a crystal oscillator. For products with integrated synthesizer filters, this pin can connect to a 14.3 MHz crystal; the other connection is MFILTER.
MFILTER	O	**MEMORY CLOCK FILTER:** This pin must be connected to a π-RC filter returned to AVSS4. The values of the two capacitors and the resistor are shown in Appendixes B1–B3 in the *CL-GD543X/'4X Technical Reference Manual*. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin. For products with integrated synthesizer filters, this pin is either a n/c or the second connection to a 14.3 MHz crystal.
VFILTER	O	**VIDEO CLOCK FILTER:** This pin must be connected to a π-RC filter returned to AVSS1. The values of the two capacitors and the resistor are shown in Appendixes B1–B3 in the *CL-GD543X/'4X Technical Reference Manual*. The filter components, especially the input capacitor and the resistor, must be placed as close as possible to this pin. For products with integrated current reference, this pin is connected to a resistor in parallel with a capacitor to AVSS[3:2]. The resistor value is typically 135 ohms. The capacitor is typically 0.1 µF. See Appendix B8 for additional information.
MCLK	I/O	**MEMORY CLOCK:** This pin is normally an output and can be used to monitor the internal MCLK.Typically, it would not be connected. If CF[5] is a '0', MCLK will be an input and the internal MCLK oscillator will be disabled. This configuration is intended for testing only. For the CL-GD5430/'36/'40 only, this pin can be configured to output the VCLK synthesizer.

2.4 Video Interface

Name	Type	Description
VSYNC	TS	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC* is low, or when vertical GENLOCK is enabled for those devices that support it. This pin can be connected directly to the corresponding pin on the feature connector.
HSYNC	TS	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC* is low, or when horizontal GENLOCK is enabled for those devices that support it. This pin can be connected directly to the corresponding pin on the feature connector.
BLANK*	I/O	**BLANK*:** This is a bidirectional pin. If ESYNC* is high, BLANK* is an output. As an output, it supplies a blanking signal to the feature connector. If ESYNC* is low, BLANK* is an input. As an active-low input, it forces the RED, GREEN, and BLUE outputs to a '0' current. This pin can be connected directly to the corresponding pin on the feature connector. For the CL-GD5440 only, this pin is used as a handshake signal for Video Port mode.
P[7:0]	I/O	**PIXEL BUS [7:0]:** These are bidirectional pins. If EVIDEO* is high, these pins are outputs and reflect the address into the palette DAC. If EVIDEO* is low, these pins are inputs and can be used to drive pixel values into the palette DAC. These pins can be connected directly to the corresponding pins on the feature connector.
P[15:8]	I	**PIXEL BUS [15:8]** ***(CL-GD5436 only)*:** These pins are redefined PCI interface pins for the CL-GD5436 only. When the appropriate conditions are met, BIOSA[13:10] and four reserved pins are redefined as eight additional P-bus pins. See the description of register GRE[7].
DCLK	I/O	**DOT CLOCK:** This is a bidirectional pin. If EDCLK* is high, this is an output and can be used to externally latch the data on the Pixel bus. If EDCLK* is low, this is an input and can be used to clock data on the Pixel bus into the CL-GD543X/'4X. This pin can be connected directly to the corresponding pin on the feature connector.
ESYNC*	I/O	**ENABLE SYNC AND BLANK*:** This input is used to control the buffers on HSYNC, VSYNC, and BLANK*. If ESYNC* is high, the controlled pins are outputs. If ESYNC* is low, BLANK* is an input. HSYNC and VSYNC are not driven by the CL-GD543X/'4X, and *must* be driven externally to valid input levels. This pin can be connected directly to the corresponding pin on the feature connector. This pin is also an output where it is used to control the shift clock of the optional EEPROM, and should be connected directly to the SK pin.

2.4 Video Interface *(cont.)*

Name	Type	Description
EVIDEO*	I/O	**ENABLE VIDEO*:** This input controls the buffers on P[7:0]. If EVIDEO* is high, P[7:0] are outputs. If EVIDEO* is low, P[7:0] are inputs. This pin can be connected directly to the corresponding pin on the feature connector. This pin is not limited to static operation; it can switch at the DCLK rate. This pin is also an output where it is used to provide data for the optional EEPROM, and should be connected directly to the DI pin. This pin is also an output when color key overlay is enabled.
EDCLK*	I/O	**ENABLE DOT CLOCK*:** This input is used to control the buffer on DCLK. If EDCLK* is high, DCLK is an output. If EDCLK* is low, DCLK is an input. This pin can be connected directly to the corresponding pin on the feature connector.
RED	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the LUT or an appropriately-sized true-color value is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $If = (63/30) \times IREF$ Each DAC output is typically terminated to monitor ground with a 75-Ω 2% resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 37.5-Ω impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 18.7 mA, and IREF should be 8.9 mA.
GREEN	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
BLUE	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
IREF	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD through this pin determines the full-scale output of each DAC. This pin should be connected to a constant current source. A recommended circuit is provided in Appendixes B1, B2, and B3 of the *CL-GD543X/'4X Technical Reference Manual*. For products with integrated current reference, this pin should be connected to a capacitor returned to AVSS[3:2]. The capacitor value is not specified at this time, but will be on the order of a few microfarads. See Appendix B8 for additional information.

2.5 Display Memory Interface

Name	Type	Description
RAS1*	O	**ROW ADDRESS STROBE*:** This active-low output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of the first bank of DRAMs in the display memory array. For the CL-GD5434, the first bank is the first two Mbytes. For the CL-GD5430, the first bank is the first one Mbyte. These pads, and those for the other DRAM controls, are matched for one to four loads. If eight DRAMs are used, damping resistors may be required to control edge rates and undershoot on these and other control pins. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*.
RAS0*/OE*	O	**ROW ADDRESS STROBE*/OUTPUT ENABLE*:** For the CL-GD543X/'4X, this active-low output can be configured as the RAS0* signal or the OE* signal. This pin must be connected to the RAS* pins of the second bank of DRAMs. For the CL-GD5434, the second bank is the second two Mbytes. For the CL-GD5430, the second bank is the second Mbyte. If CF[10] = 1, this output is configured as OE* and only one bank of DRAM is supported. This output controls the output enable inputs of the DRAMs in the display memory array. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*.
CAS[7:0]*	O	**COLUMN ADDRESS STROBE[7:0]*:** This active-low output is used to latch the Column Address from MA[9:0] into the DRAMs. These pins must be connected to the CAS* pins of all the DRAMs in the display memory array. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*. **NOTE**: If CF[10] = 1 (dual-WE* DRAMs), these pins become WE[7:0]*.
WE*	O	**WRITE ENABLE*:** This active-low output is used to control the Write Enable inputs of the DRAMs. This pin must be connected to the WE* pins of the DRAMs. See DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*. **NOTE:** If CF[10] = 1 (dual-WE* DRAMs), this pin becomes CAS*.
MA[9:0]	O	**MEMORY ADDRESS [9:0]:** These pins control the address inputs of the DRAMs. These pins must be connected to the address pins of the DRAMs. Typically, MA[9] is connected to Address 9, and MA[0] to Address 0 of the DRAMs. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*. **NOTE:** If CF[11] = (asymmetric DRAMs), MA8 is connected to Address 0 and MA0 to Address 8 of the asymmetric DRAMs.

2.5 Display Memory Interface *(cont.)*

Name	Type	Description
MD[63:0]	TS	**MEMORY DATA [63:0]:** These bidirectional pins are used to transfer data between the CL-GD543X/'4X and the display memory. These pins must be connected to the data pins of the DRAMs. See the DRAM Configuration Appendix B7 in the *CL-GD543X/'4X Technical Reference Manual*. MD[63:48] are forced into high-impedance when RESET is active; this allows the configuration pull-down resistors to override the weak pull-ups and be loaded into the Configuration register (CF). MD[7:0] are also used as the BIOSD[7:0] inputs for PCI configuration only.

2.6 Miscellaneous Pins

Name	Type	Description
EECS	O	**EEPROM CHIP SELECT:** This pin is used to control the Chip Select of the optional configuration EEPROM, and should be connected directly to that pin. This pin is also used for DDC2B support. See the description of register SR8 in Chapter 9 of the *CL-GD543X/'4X Technical Reference Manual*.
EEDI	I	**EEPROM DATA IN:** This pin is used to read the data from the optional configuration EEPROM, and should be connected directly to the Data Out pin. This pin is also used for DDC2B support. See the description of register SR8 in Chapter 9 of the *CL-GD543X/'4X Technical Reference Manual*.
EROM*	O	**ENABLE ROM BUFFERS*:** This active-low output is used to control the Output Enable pins of up to two 8-bit bus drivers. These buffers are used to connect the data pins of the BIOS EPROMs to the System Data bus. This output is forced high when RESET is active. This output goes active only for memory read cycles to the Address Range C000:0 through C7FF:F. This output is gated with MEMR* in ISA mode, and is un-latched Local Bus Address decode in local bus modes. For local bus only, this signal is active for I/O Addresses 3C6–3C9 when CF[12] = 0.
OVRW*	O	**OVERLAY WINDOW*:** This signal is active-low. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix B14 in the *CL-GD543X/'4X Technical Reference Manual*.
TWR*	I	**TEST LATCH LOAD ENABLE*:** This pin is intended for factory testing and must be pulled up for normal operation. It can be used in board-level testing to disable most of the CL-GD543X/'4X output pins. For additional information, see Appendix B13 in the *CL-GD543X/'4X Technical Reference Manual*.

2.7 Power Pins

Name	Type	Description
VDD[6:1]	Power	**+5V (LOGIC):** These six pins are used to supply +5 volts to the digital logic of the CL-GD543X/'4X. Each pin must be connected to the VCC plane as described in Appendix B12 in the *CL-GD543X/'4X Technical Reference Manual*. Each pin must be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible.
VSS[13:1]	Ground	**GROUND (LOGIC):** These 13 pins are used to supply ground reference to the digital logic of the CL-GD543X/'4X. Each VSS pin must be connected to the ground plane.
AVDD[1]	Power	**+5V (VCLK):** This pin is used to supply +5 volts to the Video Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS1 with a 10-µF capacitor.
AVSS[1]	Ground	**GROUND (VCLK):** This pin is used to supply ground reference to the Video Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the GND rail.
AVDD[4]	Power	**+5V (MCLK):** This pin is used to supply +5 volts to the Memory Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[4]	Ground	**GROUND (MCLK):** This pin is used to supply ground reference to the Memory Clock Synthesizer of the CL-GD543X/'4X. This pin must be connected to the GND rail.
AVDD[3:2]	Power	**+5V (DAC):** These two pins are used to supply +5 volts to the palette DAC of the CL-GD543X/'4X. Each pin must be connected directly to the VCC plane. Each pin must be bypassed as close to the pin as possible with a 0.1-µF capacitor that has proper high-frequency characteristics.
AVSS[3:2]	Ground	**GROUND (DAC):** These two pins are used to supply ground reference to the palette DAC of the CL-GD543X/'4X. Each pin must be connected to the GND plane. See Appendixes B1, B2, and B3 for various adapter board and motherboard solutions in the *CL-GD543X/'4X Technical Reference Manual*.

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD543X/'4X offers a solution that is totally compatible with the IBM VGA standard. The CL-GD543X/'4X includes all of the necessary hardware for CPU updates to memory, screen refresh, and DRAM refresh. A complete VGA motherboard solution can be implemented by using two 256K × 16 DRAMs with the CL-GD5434 or CL-GD5436, or a single 256K × 16 DRAM with the CL-GD5430 or CL-GD5440.

Figure 3-1 shows the CL-GD543X/'4X connection to the host, display memory, and monitor.

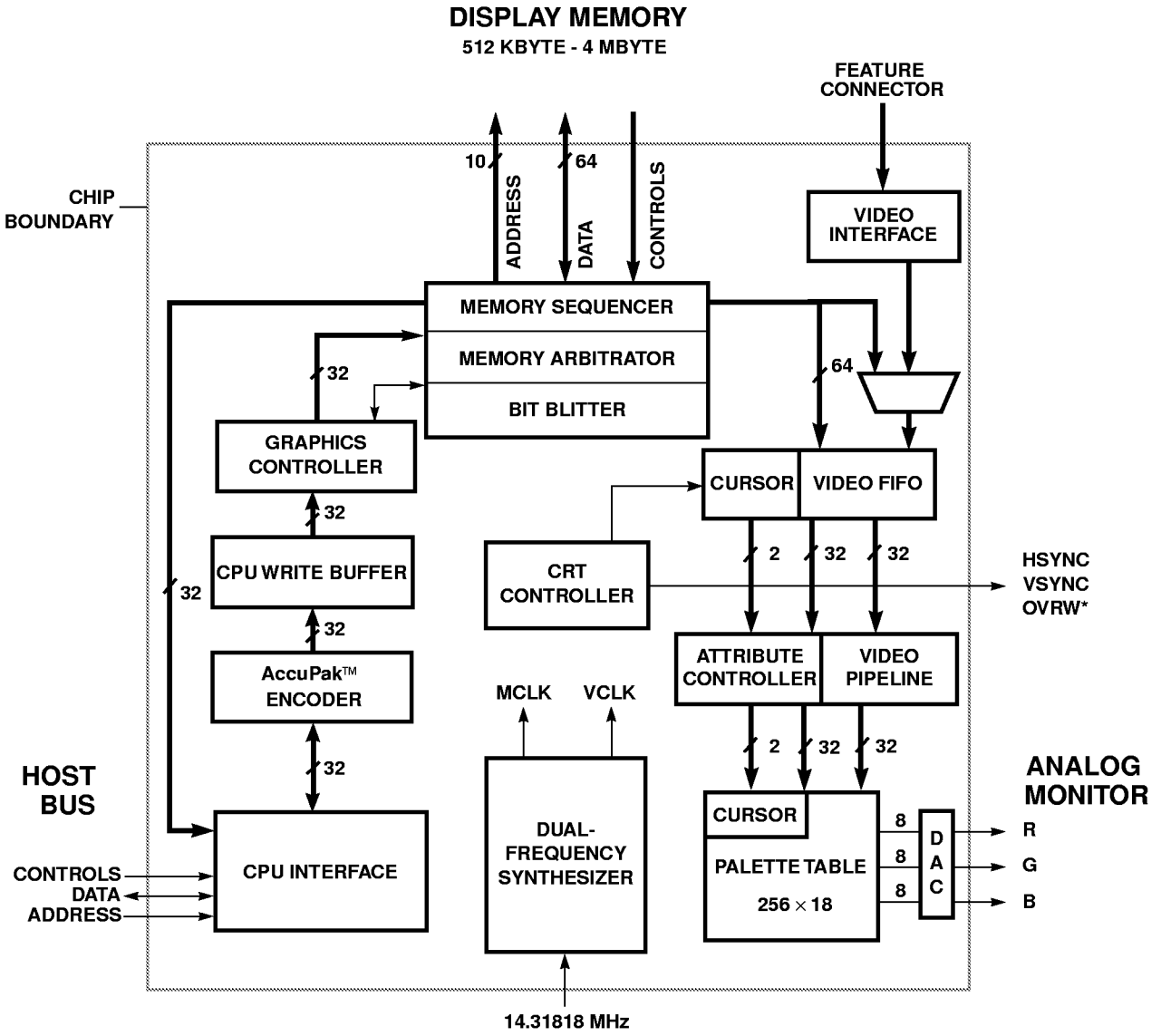


Figure 3-1. CL-GD543X/'4X Chip Block Diagram

3.2 Functional Blocks

The following sections describe functional blocks that are integrated into the CL-GD543X/'4X.

3.2.1 CPU Interface

The CL-GD543X/'4X connects directly to any '486, VESA VL-Bus, or PCI local bus. The CL-GD5434 also connects to the industry-standard ISA bus. No glue logic is required to implement any of these bus interfaces, except for a single inverter for ISA bus. The CL-GD543X/'4X internally decodes a 16- or 24-bit address and responds to the applicable control lines. It executes both I/O accesses and memory accesses as either an 8-, 16-, or 32-bit device.

'486/VESA® VL-Bus™

The CL-GD543X/'4X can interface with '486 microprocessors, and the VESA VL-Bus, at speeds of up to 50 MHz. The CL-GD543X/'4X provides single-clock support, which eliminates additional circuitry for a local bus subsystem design. The CL-GD543X/'4X also supports linear memory addressing to take full advantage of the local bus interface.

PCI Bus

The CL-GD543X/'4X is a highly integrated VGA controller that can interface with the PCI bus directly without any additional logic to support its multiplexed address and data pins. The CL-GD543X/'4X interface executes 32-bit I/O and memory accesses at a speed of up to 33 MHz. The CL-GD543X/'4X also supports memory burst cycles. The CL-GD543X/'4X is fully compliant with the single-load specification of PCI.

ISA Bus (CL-GD5434 only)

The CL-GD5434 supports the 16-bit ISA bus. The CL-GD5434 will execute either 8- or 16-bit I/O and memory accesses, and has a highly-integrated ISA interface so that no additional logic is required except for a single inverter.

3.2.2 CPU Write Buffer

The CL-GD543X/'4X has a multi-level 32-bit CPU write buffer, which dramatically increases GUI acceleration and enhances CPU performance. The CPU write buffer contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining a queue allows the CL-GD543X/'4X to release the CPU as soon as it has recorded the address and data, and then to execute the operation when display memory cycles are available.

3.2.3 Graphics Controller

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

3.2.4 BitBLT Engine

The CL-GD543X/'4X has a two-operand BitBLT engine. The BitBLT engine is designed to move data in packed-pixel modes with ROP (raster operations). The ROPs are defined in terms of function and Microsoft equivalents. The BitBLT function is designed to accelerate Microsoft Windows 3.1, Windows NT, Windows95, and OS/2 2.1. Other optional features (for example, color expansion and transparency) enhance the BitBLT function to offer GUI acceleration surpassing other DRAM- or VRAM-based GUI accelerators.

3.2.5 Memory Arbitrator

The memory arbitrator allocates bandwidth to the four functions that compete for the limited bandwidth of display memory: CPU access, screen refresh, DRAM refresh, and BitBLT. DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU/BitBLT access are allocated cycles according to the FIFO-control parameters. Priority given is to screen refresh.

3.2.6 Memory Sequencer

The memory sequencer generates timing for display memory. This includes RAS*, CAS*, and multiplexed-address timing, as well as WE* timing. The Sequencer generates CAS*-before-RAS* refresh cycles, Random Read and Random Early Write cycles, and Fast-page mode Read and Early Write cycles. The memory sequencer generates multiple CAS* or WE* signals according to the memory type used. EDO (extended data output) DRAMs are supported.

3.2.7 CRT Controller

The CRT controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the palette DAC. The CL-GD5434/'36 support both horizontal and vertical GENLOCK. The CL-GD5440 supports a hardware video window.

3.2.8 Video FIFO

The video FIFO allows the memory sequencer to execute display memory accesses needed for screen refresh at maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and to execute them in Fast-page mode rather than Random-read mode. The CL-GD5440 has two video FIFOs for video playback.

3.2.9 Attribute Controller

The attribute controller formats the display for the screen. Display color selection, text blinking, and underlining are performed by the attribute controller. Alternate font selection also occurs in the attribute controller.

3.2.10 Video Pipeline (CL-GD5440)

The CL-GD5440 video pipeline performs format conversion, interpolated X and Y zooming, and color space conversion for a rectangular region of the display called the 'video window'.

3.2.11 Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue. Alternatively, the CL-GD543X/'4X can be configured for 15-, 16-, or 24-bit pixels. This allows 32K, 64K, or 16M simultaneous colors to be displayed on the screen. The 24 bits are allocated as 8-8-8 for 16M colors, 5-6-5 for 64K Color mode, or 5 to each (red, green, and blue) DAC for 32K Color mode. The CL-GD5440 also supports YCrCb and AccuPak formats.

The CL-GD5434 has a 32-bit data path width which supports direct 24/32-bit-per-pixel clock modes. The high byte of the 32-bit pixel (the 'alpha' byte) can be used for 'color key' overlay control. Refer to Appendix B14 in the *CL-GD543X/'4X Technical Reference Manual* for more detailed information. The CL-GD5436 supports Packed-24 modes for increased true color performance.

The palette DAC supports Power-down mode which temporarily turns the palette DAC off to conserve power.

3.2.12 Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the memory sequencer and video display clocks from a single reference frequency. The frequency of each clock is independently programmable. The maximum memory sequencer clock and video display clock is listed on page 3-1. The reference frequency of 14.31818 MHz must be supplied from an external TTL source.

3.2.13 VESA®/VGA Pass-through Connector

The CL-GD543X/'4X is designed to connect directly to a VESA connector. The device supports the three enable/disable inputs; the Pixel bus can drive the connector directly. Through this connector, the overlay feature can be used in multimedia applications. This allows for internal DAC utilization in 16-bit-per-pixel mode. The CL-GD5430/'40 supports VAFC Baseline input and output. The CL-GD5436 supports direct 16-bit input when configured for the PCI bus.

3.3 Functional Operation

The following sections discuss the four major operations handled by the CL-GD543X/'4X.

CPU Access to Registers

The host can be any processor controlling any '486-based local bus architecture (for example, VESA VL-Bus or PCI interfaces). The host accesses CL-GD543X/'4X registers by setting up 16- or 24-bit addresses and making the appropriate controls active. The CL-GD543X/'4X can respond as either an 8- or 16-bit peripheral, depending on how it has been configured in the system.

DRAM and screen refresh occur concurrently with, and independently of, register access (unless the host is changing display parameters or has suppressed refresh). These registers are described in the *CL-GD543X/'4X Technical Reference Manual*.

CPU Access to Display Memory

The CL-GD543X/'4X can manage all host accesses to display memory. The host first sets up certain parameters (for example, color and write masks) then generates a memory access in the range where the CL-GD543X/'4X is programmed to respond. The CL-GD543X/'4X will transfer 32-bit-wide data for any of the local bus interfaces. The CL-GD5434 will transfer 16-bit-wide data for the ISA bus.

Display Memory Refresh

The CL-GD543X/'4X automatically generates a selectable number of CAS*-before-RAS* refresh cycles during each horizontal timing period.

Screen Refresh

The CRT monitor requires near-constant rewriting since its only memory is the phosphor persistence. The CL-GD543X/'4X fetches information from display memory for each scanline as quickly as possible, using Fast-page mode cycles to fill the video FIFO. This allows the maximum possible time for the host and BitBLT engine to access display memory.

3.4 Performance

The CL-GD543X/'4X is designed with the following performance-enhancing features:

- 64-bit display memory data bus for faster access to display memory (CL-GD5430/'40 has an effective 32-bit display memory data bus)
- Memory-mapped 32-bit BitBLT registers
- DRAM Fast-page mode operations for faster access to display memory
- Zero-wait-state performance and a CPU write buffer that allows faster CPU access for writes to display memory
- Accelerated Microsoft® Windows® with BitBLT
- Increased throughput with '486/VESA® local bus interface
- Increased throughput with PCI local bus interface with Burst mode
- 32-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 16- or 32-bit CPU interface to I/O registers for faster host access
- Multi-level, 32-bit system memory write cache
- 32-bit internal data inputs for internal DAC
- Video FIFO to minimize memory contention
- 32 × 32 and 64 × 64 hardware cursor to improve Microsoft® Windows® performance

3.5 Compatibility

The CL-GD543X/'4X includes all registers and data paths required for VGA controllers, and is upward-compatible with the CL-GD542X family.

The CL-GD543X/'4X supports extensions to VGA, including 1024 × 768 × 16M interlaced, 1024 × 768 × 64K interlaced and non-interlaced, and 1280 × 1024 × 256 interlaced and non-interlaced modes. Additionally, various 132-column text modes are supported.

3.6 Board Testability

The CL-GD543X/'4X device is testable, even when installed on a printed circuit board. By using Pin-Scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace, will be detected. The Signature Generator allows the entire system, including the display memory, to be tested at speed.

4. CONFIGURATION TABLES

4.1 Video Modes

Table 4-1. IBM Standard VGA Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
6	6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
E	E	16/256K	80 × 25	8 × 14	640 × 200	Graphics	25	31.5	70
F	F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
11+	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12	12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12+	12+	16/256K	80 × 30	8 × 16	640 × 480	Graphics	36.0	43.3	85
13	13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70

NOTE: The EGA-compatible text modes (which use an 8 × 14 font) and graphics modes 10 and F use a 16-dot high font, with the bottom two lines truncated, in the absence of TSRFONT (8 × 14 font TSR). This creates some errors when displaying characters with descenders, but does not restrict operation of programs using these modes. In text modes using the 8 × 14 font, the characters 'g', 'j', 'p', 'q', 'y', and 'ÿ' are truncated using a middle- and bottom-line algorithm to avoid truncation of descenders. For compatibility with some DOS applications using the 8 × 14 font, the TSRFONT utility should be used. Applications such as DOSSHELL in Graphics 25 or 34 line display modes require the TSRFONT utility be loaded.

Table 4-2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14	–	16/256K	132 × 25	8 × 16	1056 × 400	Text	41.5	31.5	70
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	Text	41.5	31.5	70
55	109	16/256K	132 × 25	8 × 14	1056 × 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	56.25	53.7	85
5D†	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	36.0	43.3	85
60†	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	77	58	72
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	94.5	68.7	85
64	111	64K	–	–	640 × 480	Graphics	25	31.5	60
64	111	64K	–	–	640 × 480	Graphics	31.5	37.9	72
64	111	64K	–	–	640 × 480	Graphics	31.5	37.5	75
64	111	64K	–	–	640 × 480	Graphics	36.0	43.3	85
65	114	64K	–	–	800 × 600	Graphics	36	35.2	56
65	114	64K	–	–	800 × 600	Graphics	40	37.8	60
65	114	64K	–	–	800 × 600	Graphics	50	48.1	72
65	114	64K	–	–	800 × 600	Graphics	49.5	46.9	75
65	114	64K	–	–	800 × 600	Graphics	56.25	53.7	85
66	110	32K‡	–	–	640 × 480	Graphics	25	31.5	60

Table 4-2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.9	72
66	110	32K‡	–	–	640 × 480	Graphics	31.5	37.5	75
66	110	32K‡	–	–	640 × 480	Graphics	36.0	43.3	85
67	113	32K‡	–	–	800 × 600	Graphics	36	35.2	56
67	113	32K‡	–	–	800 × 600	Graphics	40	37.8	60
67	113	32K‡	–	–	800 × 600	Graphics	50	48.1	72
67	113	32K‡	–	–	800 × 600	Graphics	49.5	46.9	75
67	113	32K‡	–	–	800 × 600	Graphics	56.25	53.7	85
68†	116	32K‡	–	–	1024 × 768	Graphics	44.9	35.5	43i†
68	116	32K‡	–	–	1024 × 768	Graphics	65	48.3	60
68	116	32K‡	–	–	1024 × 768	Graphics	75	56	70
68	116	32K‡	–	–	1024 × 768	Graphics	78.7	60	75
68	116	32K‡	–	–	1024 × 768	Graphics	94.5	68.7	85
69†	119	32K‡	–	–	1280 × 1024	Graphics	75	48	43i†
6C†	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D†	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i†
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	108	65	60
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	126	76	71.2
6D	107	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	135	80	75
71	112	16M	–	–	640 × 480	Graphics	25	31.5	60
71	112	16M	–	–	640 × 480	Graphics	31.5	37.9	72
71	112	16M	–	–	640 × 480	Graphics	31.5	37.5	75
71	112	16M	–	–	640 × 480	Graphics	36.0	43.3	85
72↕	–	16M + A	–	–	800 × 600	Graphics	36	35.2	56
72↕	–	16M + A	–	–	800 × 600	Graphics	40	37.8	60
73↕	–	16M + A	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74†	117	64K	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74	117	64K	–	–	1024 × 768	Graphics	65	48.3	60
74	117	64K	–	–	1024 × 768	Graphics	75	56	70
74	117	64K	–	–	1024 × 768	Graphics	78.7	60	75
74	117	64K	–	–	1024 × 768	Graphics	94.5	68.7	85
75†	11A	64K	–	–	1280 × 1024	Graphics	75	48	43i†
76↕	–	16M + A	–	–	640 × 480	Graphics	25	31.5	60
76↕	–	16M + A	–	–	640 × 480	Graphics	31.5	37.9	72
76↕	–	16M + A	–	–	640 × 480	Graphics	31.5	37.5	75
78	115	16M	–	–	800 × 600	Graphics	36	35.2	56
78	115	16M	–	–	800 × 600	Graphics	40	37.8	60

Table 4-2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
78	115	16M	–	–	800 × 600	Graphics	50	48.1	72
78	115	16M	–	–	800 × 600	Graphics	49.5	46.9	75
78	115	16M	–	–	800 × 600	Graphics	56.25	53.7	85
79	118	16M	–	–	1024 × 768	Graphics	44.9	35.5	43i†
79	118	16M	–	–	1024 × 768	Graphics	65	48.3	60
79	118	16M	–	–	1024 × 768	Graphics	75	56	70
79	118	16M	–	–	1024 × 768	Graphics	78.7	60	75
79	118	16M	–	–	1024 × 768	Graphics	94.5	68.7	85
7C	–	256/256K	–	–	1152 × 864	Graphics	94.5	63.9	70
7C	–	256/256K	–	–	1152 × 864	Graphics	108	67.5	75

NOTES:

1) '‡' character indicates 32K Direct-Color/256-color Mixed mode.
2) '†' character indicates Interlaced mode.
3) '↕' character indicates 16M colors, but with 32-bit-per-pixel format.
4) '16M + A' indicates 16M colors + Alpha channel
5) Some modes and some refresh rates are not supported by all CL-GD543X/'4X controllers. Refer to the CL-GD543X Software Release Kit for the list of video modes supported by the CL-GD543X/'4X BIOS. Also see the table on the inside front cover of the *CL-GD543X/'4X Technical Reference Manual*.
6) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected will be automatically used.
7) An 8 × 14 font for mode 55h may be provided with a DOS TSR. If the TSR has not been loaded when the mode is set, the 8 × 16 font will be used with the two bottom rows deleted. This causes truncation of characters with descenders, but does not restrict program operation nor does it make characters particularly difficult to read. For absolute compatibility with some DOS applications which use the 8 × 14 font, the TSR should be used.

4.2 Configuration Register, CF

When RESET (system power-on reset) goes active, the CL-GD543X/'4X samples the levels on several of the Display Memory Data (MD[63:48]) pins. These levels are latched into a write-only Configuration register (CF1). This register specifies the configuration of the CL-GD543X/'4X.

The levels on the Memory Data bus default to a logic '1' during power-on reset because of internal 250-kΩ pull-up resistors. A logic '0' is achieved by installing an external 6.8-kΩ pull-down resistor on the memory data line corresponding to the appropriate bit in the Configuration register. Refer to Appendix B9 in the *CL-GD543X /'4XTechnical Reference Manual*. Table 4-3 summarizes the Configuration register. The bits are described in detail in Appendix B9.

Table 4-3. Configuration Register Bits

CF Bits	Level	Description	Memory Data Bit	Pin Number
15	0 1	Enable Pin-Scan test Disable Pin-Scan test	MD63	157
14	0 1	PCI3C[8] = 1 (CL-GD5436/'40 only) PCI3C[8] = 0 (CL-GD5436/'40 only)	MD62	158
13	0 1	3c3[0] reset state = 0 (CL-GD5436 only) 3c3[0] reset state = 1 (CL-GD5436 only)	MD61	159
12	0 1 0 1	Source VCLK on MCLK (CL-GD5430/'36/'40 only) Source MCLK on MCLK (CL-GD5430/'36/'40 only) Disable internal DAC (CL-GD5434 only) Enable internal DAC (CL-GD5434 only	MD60	160
11	0 1	Asymmetric DRAM (RAS*/CAS* addressing) Symmetric DRAM (RAS*/CAS* addressing)	MD59	161
10	0 1	Multiple-CAS*, single-WE* Multiple-WE*, single-CAS*	MD58	162
9	0 1	7-MCLK RAS* cycle 6-MCLK RAS* cycle	MD57	163
8	0 1 0 1	50.11363-MHz MCLK default (except CL-GD5436) 41.16477-MHz MCLK default (except CL-GD5436) Enable byte swapping (PCI configured CL-GD5436 only) Disable byte swapping (PCI configured CL-GD5436 only)	MD56	164
7	0 1	64K ROM BIOS @ C0000h–CFFFFh 32K ROM BIOS @ C0000h–C7FFFh	MD55	170
6	0 1 0 1	16-bit BIOS ROM (ISA bus configuration) 8-bit BIOS ROM (ISA bus configuration) Zero-wait Write not supported (VESA VL-Bus configuration) Zero-wait Write supported (VESA VL-Bus configuration)	MD54	171
5	0 1	External MCLK (pin 16 is an input) Internal MCLK (pin 16 is an output)	MD53	172
4	0 1	I/O port 94h enables POS 102 access (video enable) I/O port 3C3h used for video enable	MD52	173
3	0 1	Port 3C3h is Video System Sleep register Port 46E8h is Video System Sleep register	MD51	174
2, 1, 0	000 001 010 011 100 110 111	Reserved Reserved VESA VL-Bus or '486 (> 33 MHz) Reserved PCI bus VESA® VL-Bus™ or '486 (≤ 33 MHz) ISA bus (CL-GD5434 only)	MD50, MD49, MD48	141, 142, 143

4.3 Host Interface Signals

With the pin connections listed in Table 4-4, the CL-GD543X/'4X will interface directly to an ISA or local bus.

Table 4-4. Bus Connections

CL-GD543X/'4X Pin	ISA Bus (CL-GD5434 only)	VESA® VL-Bus™	PCI Bus
50	LA23	HIMEM	PAR
48	LA22	LOWMEM	STOP#
[45..44]	LA[21:20]	A[21:20]	(unused)
[42..40]	LA[19:17]	A[19:17]	BIOSA[15:13]
39	SA[16]	A[16]	(unused)
38	SA[15]	A[15]	(unused)
37	SA[14]	A[14]	BIOSA12
[36..34], [32..24]	SA[13:2]	A[13:2]	BIOSA[11:0]
23	SA1	BE3#	C/BE#3
22	SA0	BE2#	C/BE#2
[54..63], [68..70]	(unused)	D[31:19]	AD[31:19]
71	MEMW*	D18	AD18
72	IOCS16*	D17	AD17
73	IRQ	D16	AD16
[74..76], [78..82], [84..85], [87..92]	SD[15:0]	D[15:0]	AD[15:0]
21	SBHE*	BE1#	C/BE#1
20	REFRESH*	BE0#	C/BE#0
46	BALE	ADS#	FRAME#
47	AEN	RDYRTN#	IRDY#
53	IOR*	W/R#	IDSEL
43	IOW*	LCLK	CLK
66	MEMR*	M/IO#	(unused)
51	RESET	RESET	RST
49	IOCHRDY	LRDY#	TRDY#
65	MCS16*	LDEV#	DEVSEL#
19	0WS	INTR	INTR
17	OSC	OSC	OSC
33	EROM*	EROM*	EROM*

NOTES:

1) For ISA bus applications, note that SA[19:17] are not found on the CL-GD5434; this means that an adapter board will only function in a 16-bit slot.
2) The OSC and EROM* pins are common in all configurations.

5. VGA REGISTER PORT MAP

Table 5-1. VGA Register Port Map

Address	Port
94	POS 102 Access Control (3C3 sleep)
102	POS102 register
3B4	CRT Controller Index (R/W — monochrome)
3B5	CRT Controller Data (R/W — monochrome)
3BA	Feature Control (W), Input Status register 1 (R — monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status register 0 (R)
3C3	Motherboard Sleep
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC register (R/W)
3C7	Pixel Address Read Mode (W), DAC State (R)
3C8	Pixel Mask Write Mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3D4	CRT Controller Index (R/W — color)
3D5	CRT Controller Data (R/W — color)
3DA	Feature Control (W), Input Status register 1 (R — color)
46E8	Adapter Sleep

6. CL-GD543X/'4X REGISTERS

External/General Registers

Abbreviation	Register Name	Index	Port
POS94	POS102 Access Control	–	94
POS102	POS102	–	102
VSSM	Motherboard Sleep	–	3C3
VSSM	Adapter Sleep	–	46E8
MISC	Miscellaneous Output	–	3C2 (Write)
MISC	Miscellaneous Output	–	3CC (Read)
FC	Feature Control	–	3?A (Write)
FC	Feature Control	–	3CA (Read)
FEAT	Input Status Register 0	–	3C2 (Read)
STAT	Input Status Register 1	–	3?A
3C6	Pixel Mask	–	3C6
3C7	Pixel Address Read Mode	–	3C7 (Write)
3C7	DAC State	–	3C7 (Read)
3C8	Pixel Address Write Mode	–	3C8
3C9	Pixel Data	–	3C9
PCI00	PCI Device/Vendor ID	–	00
PCI04	PCI Command	–	04 (Write)
PCI04	PCI Status	–	04 (Read)
PCI08	PCI Class Code	–	08 (Read)
PCI10	PCI Display Memory Base Address	–	10
PCI14	PCI Relocatable I/O Base Address	–	14
PCI30	PCI ROM Base Address Enable	–	30
PCI3C	PCI Interrupt Line/ Interrupt Pin	–	3C

NOTE: '?' in the above address is 'B' in Monochrome mode and 'D' in Color mode.

VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5
CRA	Text Cursor Start	A	3?5
CRB	Text Cursor End	B	3?5
CRC	Screen Start Address High	C	3?5
CRD	Screen Start Address Low	D	3?5
CRE	Text Cursor Location High	E	3?5
CRF	Text Cursor Location Low	F	3?5
CR10	Vertical Sync Start	10	3?5
CR11	Vertical Sync End	11	3?5
CR12	Vertical Display End	12	3?5
CR13	Offset	13	3?5
CR14	Underline Row Scan	14	3?5
CR15	Vertical Blanking Start	15	3?5
CR16	Vertical Blanking End	16	3?5
CR17	Mode Control	17	3?5
CR18	Line Compare	18	3?5
CR22	Graphics Data Latches Readback	22	3?5
CR24	Attribute Controller Toggle Readback	24	3?5
CR26	Attribute Controller Index Readback	26	3?5

NOTE: '?' in the above address is 'B' in Monochrome mode and 'D' in Color mode.

VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GRX	Graphics Controller Index	–	3CE
GR0	Set/Reset	0	3CF
GR1	Set/Reset Enable	1	3CF
GR2	Color Compare	2	3CF
GR3	Data Rotate	3	3CF
GR4	Read Map Select	4	3CF
GR5	Mode	5	3CF
GR6	Miscellaneous	6	3CF
GR7	Color Don't Care	7	3CF
GR8	Bit Mask	8	3CF

VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port
ARX	Attribute Controller Index	–	3C0/3C1
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1
AR10	Attribute Controller Mode	10	3C0/3C1
AR11	Overscan (Border) Color	11	3C0/3C1
AR12	Color Plane Enable	12	3C0/3C1
AR13	Pixel Panning	13	3C0/3C1
AR14	Color Select	14	3C0/3C1

Extended Sequencer Registers

Abbreviation	Register Name	Index	Port
SR2	Enable Writing Pixel Extension	2	3C5
SR6	Unlock ALL Extensions	6	3C5
SR7	Extended Sequencer Mode	7	3C5
SR8	EEPROM Control	8	3C5
SR9	Scratch-Pad 0	9	3C5
SRA	Scratch-Pad 1	A	3C5
SRB	VCLK0 Numerator	B	3C5
SRC	VCLK1 Numerator	C	3C5
SRD	VCLK2 Numerator	D	3C5
SRE	VCLK3 Numerator	E	3C5
SRF	DRAM Control	F	3C5
SR10	Graphics Cursor X Position	10	3C5
SR11	Graphics Cursor Y Position	11	3C5
SR12	Graphics Cursor Attributes	12	3C5
SR13	Graphics Cursor Pattern Address Offset	13	3C5
SR14	Scratch-Pad 2	14	3C5
SR15	Scratch-Pad 3	15	3C5
SR16	Performance Tuning	16	3C5
SR17	Configuration Read Back and Extended Control	17	3C5
SR18	Signature Generator Control	18	3C5
SR19	Signature Generator Result Low Byte	19	3C5
SR1A	Signature Generator Result High Byte	1A	3C5
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5
SR1F	MCLK Select	1F	3C5

Extended Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GR0	Write Mode 5 Background Extension	0	3CF
GR1	Write Mode 4, 5 Foreground Extension	1	3CF
GR9	Offset Register 0	9	3CF
GRA	Offset Register 1	A	3CF
GRB	Graphics Controller Mode Extensions	B	3CF
GRC	Color Key	C	3CF
GRD	Color Key Mask	D	3CF
GRE	Miscellaneous Control	E	3CF
GR10	Background Color Byte 1	10	3CF
GR11	Foreground Color Byte 1	11	3CF

BitBLT Registers

Abbreviation	Register Name	Index	Port
GR12	Background Color Byte 2 *(CL-GD5434/'36 only)*	12	3CF
GR13	Foreground Color Byte 2 *(CL-GD5434/'36 only)*	13	3CF
GR14	Background Color Byte 3 *(CL-GD5434/'36 only)*	14	3CF
GR15	Foreground Color Byte 3 *(CL-GD5434/'36 only)*	15	3CF
GR20	BLT Width Byte 0	20	3CF
GR21	BLT Width Byte 1	21	3CF
GR22	BLT Height Byte 0	22	3CF
GR23	BLT Height Byte 1	23	3CF
GR24	BLT Destination Pitch Byte 0	24	3CF
GR25	BLT Destination Pitch Byte 1	25	3CF
GR26	BLT Source Pitch Byte 0	26	3CF
GR27	BLT Source Pitch Byte 1	27	3CF
GR28	BLT Destination Start Byte 0	28	3CF
GR29	BLT Destination Start Byte 1	29	3CF
GR2A	BLT Destination Start Byte 2	2A	3CF
GR2B	Reserved	2B	3CF
GR2C	BLT Source Start Byte 0	2C	3CF
GR2D	BLT Source Start Byte 1	2D	3CF
GR2E	BLT Source Start Byte 2	2E	3CF
GR2F	BLT Destination Write Mask *(CL-GD5430/'36 only)*	2F	3CF
GR30	BLT Mode	30	3CF
GR31	BLT Start/Status	31	3CF
GR32	BLT Raster Operation	32	3CF
GR33	BLT Mode Extensions *(CL-GD5436 only)*	33	3CF

Extended CRTC Registers

Abbreviation	Register Name	Index	Port
CR19	Interlace End	19	3?5
CR1A	Miscellaneous Control	1A	3?5
CR1B	Extended Display Controls	1B	3?5
CR1C	Sync Adjust and GENLOCK *(CL-GD5434 only)*	1C	3?5
CR1D	Overlay Extended Control	1D	3?5
CR25	Part Status	25	3?5
CR27	ID	27	3?5
CR28	CL-GD5430 Class ID	28	3?5
HDR	Hidden DAC	–	3C6

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

Extended CDX Registers (CL-GD5440 only)

Abbreviation	Register Name	Index	Port
CR1F	Video Capture and Video Port Configuration	1F	3?5
CR31	Video Window Horizontal Zoom Control	31	3?5
CR32	Video Window Vertical Zoom Control	32	3?5
CR33	Video Window Horizontal Region 1 Size	33	3?5
CR34	Video Window Horizontal Region 2 Active Size	34	3?5
CR35	Video Window Horizontal Region 2 Skip Size	35	3?5
CR36	Video Window Horizontal Overflow	36	3?5
CR37	Video Window Vertical Start	37	3?5
CR38	Video Window Vertical End	38	3?5
CR39	Video Window Vertical Overflow	39	3?5
CR3A	Video Window Start Address Byte 0	3A	3?5
CR3B	Video Window Start Address Byte 1	3B	3?5
CR3C	Video Window Start Address Byte 2	3C	3?5
CR3D	Video Window Address Offset	3D	3?5
CR3E	Video Window Master Control	3E	3?5
CR3F	Host Video Data Path Control	3F	3?5

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° to 70° C

Storage temperature ..... -65° to 150° C

Voltage on any pin ..... V_{SS} -0.5 V to V_{CC} + 0.5 V

Operating power dissipation ..... 2.0 watts

Power supply voltage ..... 7 volts

Injection current (latch-up testing) ..... 100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Specifications (Digital)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{CC}	Power Supply Voltage	4.75	5.25	Volts	Normal Operation	
V_{IL}	Input Low Voltage	0	0.8	Volts		
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts		
V_{OL}	Output Low Voltage		0.5	Volts	I_{OL} = 4 mA	1
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = 400 µA	2
I_{CC}	Supply Current				V_{CC} = Nominal	3
I_{IH}	Input High Current		10	µA	$V_{IN} = V_{CC}$	
I_{IL}	Input Low Current	–10		µA	V_{CC} = 5.25, V_{IN} = 0	
I_{IHP}	Input High Current (Pull-up)	–10	10	µA	$V_{IN} = V_{CC}$	
I_{ILP}	Input Low Current (Pull-up)	–45	–12	µA	V_{CC} = 5.25, V_{IN} = 0	
I_{OZ}	Input Leakage	–10	10	µA	$0 < V_{IN} < V_{CC}$	
C_{IN}	Input Capacitance		10	pF		4
C_{OUT}	Output Capacitance		10	pF		4

NOTES:

1) I_{OL} is specified for a standard buffer. See Section 1.4, Pin Summary, for further information.
2) I_{OH} is specified for a standard buffer. See Section 1.4, Pin Summary, for further information.
3) I_{CC} is measured with VCLK and MCLK as indicated in the table below:

Device	VCLK	MCLK	I_{CC} (mA)
CL-GD5430	78 MHz	60 MHz	327
CL-GD5434	108 MHz	50 MHz	296
CL-GD5436	135 MHz	80 MHz	tbd
CL-GD5440	78 MHz	60 MHz	tbd

4) This is not 100% tested, but is periodically sampled.

7.3 DC Specifications (Palette DAC)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation	
I_{REF}	DAC Reference Current	–3	–10	mA		1

NOTE: 1)The nominal I_{REF} is 8.9 mA. See Appendix B8 for products with integrated I_{REF}.

7.4 DC Specifications (Frequency Synthesizer)

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	Synthesizer Supply Voltage	4.75	5.25	Volts		

7.5 DAC Characteristics

(V_{CC} = 5 V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MAX	Units	Test Conditions	Note
R	Resolution	8	Bits		
IO	Output Current	30	mA	VO < 1V	
TR	Analog Output Rise/Fall Time	8	ns		2, 3, 4
TS	Analog Output Settling Time	15	ns		2, 3, 5
TSK	Analog Output Skew	tbd	ns		2, 3, 6
FDT	DAC-to-DAC Correlation	2.5	%		6, 7
GI	Glitch Impulse	Typical	pV–sec.		2, 3, 6
IL	Integral Linearity	1.5	LSB		
DL	Differential Linearity	1.5	LSB		2

NOTES:
2) Load is 50 ohms and 30 pF per analog output.
3) I_{REF} = –6.67 mA.
4) TR is measured from 10% to 90% full-scale.
5) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.
8) 'tbd' means 'to be determined'.

7.6 List of Waveforms

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Table 7-1. I/O Write Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOW* active	5	–	ns
t_2	IOW* pulse width	40	–	ns
t_3	Data setup to IOW* inactive	5	–	ns
t_4	Data hold from IOW* inactive	0	–	ns
t_5	Address, SBHE* hold from IOW* inactive	0	–	ns
t_6	IOW* inactive to any command active	80	–	ns

[a] AEN must be inactive

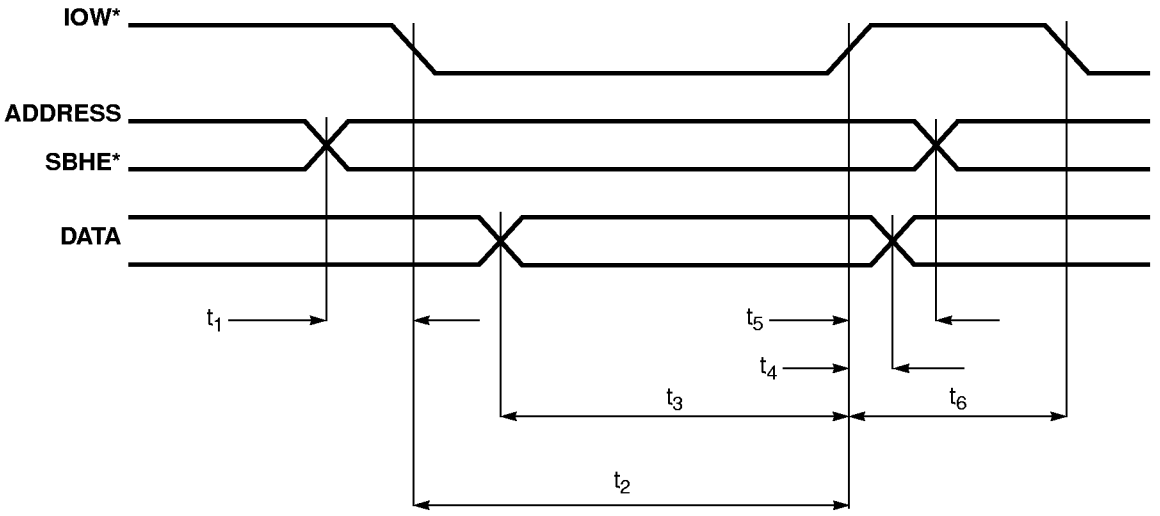


Figure 7-1. I/O Write Timing (ISA Bus — CL-GD5434 only)

Table 7-2. I/O Read Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* setup to IOR* active	5	–	ns
t_2	IOR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOR* active	–	60	ns
t_4	IOR* pulse width	70	–	ns
t_5	Data hold from IOR* inactive	0	20	ns
t_6	Address, SBHE* hold from IOR* inactive	0	–	ns
t_7	IOR* inactive to high-impedance delay	0	20	ns

[a] AEN must be inactive

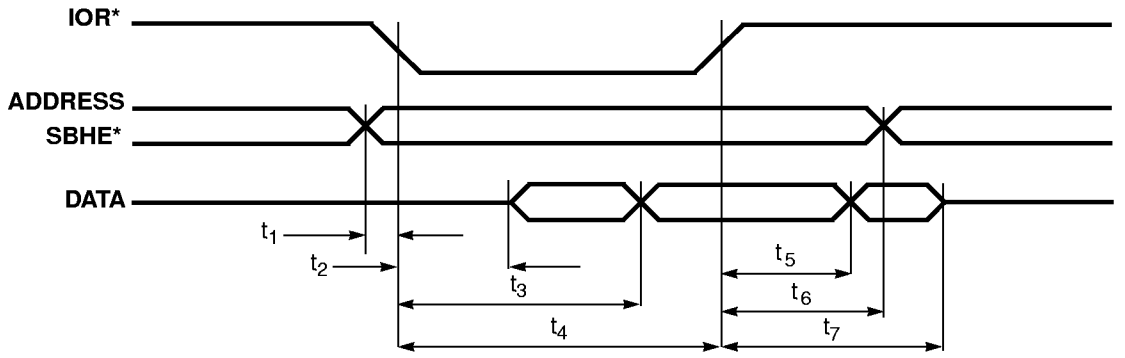


Figure 7-2. I/O Read Timing (ISA Bus — CL-GD5434 only)

Table 7-3. Memory Write Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMW* active setup	5	–	ns
t_2	SMEMW* pulse width	3	–	MCLK
t_3	Data valid from SMEMW* active	–	3	MCLK
t_4	Data hold from SMEMW* inactive	10	–	ns
t_5	Address, SBHE* hold from SMEMW* inactive	0	–	ns
t_6	SMEMW* inactive to next SMEMW*	3	–	MCLK

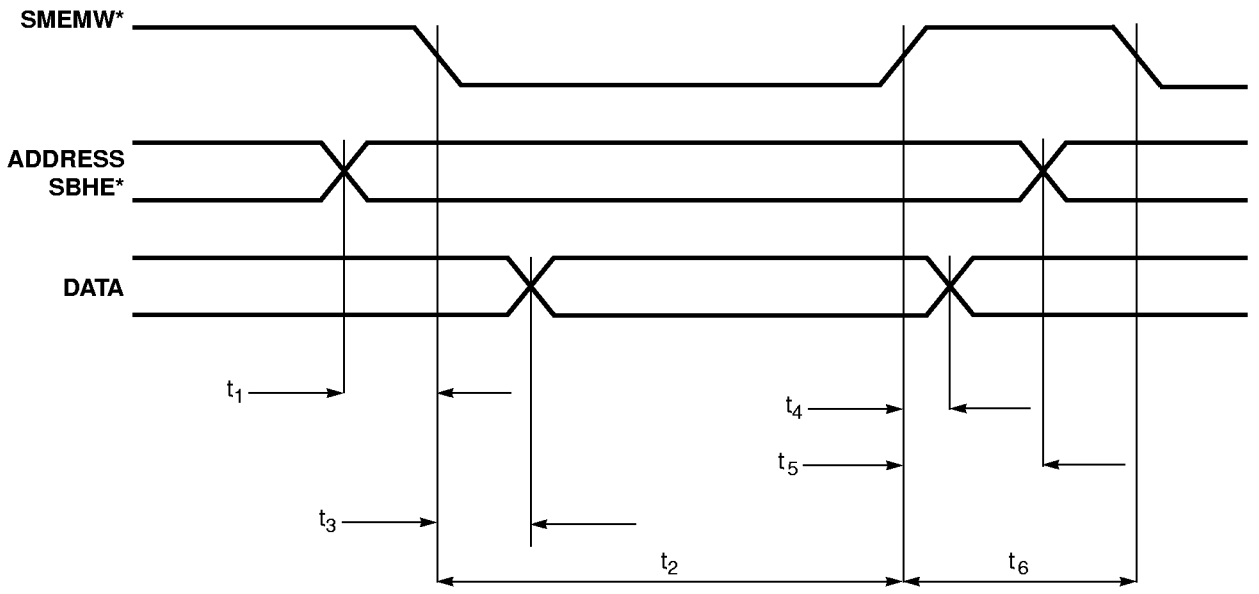


Figure 7-3. Memory Write Timing (ISA Bus — CL-GD5434 only)

Table 7-4. Memory Read Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMR* active	5	–	ns
t_2	SMEMR* active to low-impedance delay	0	–	ns
t_3	Data delay from IOCHRDY active	–	15	ns
t_4	SMEMR* pulse width	–	[a]	ns
t_5	Data hold from SMEMR* inactive	0	20	ns
t_6	Address, SBHE* hold from SMEMR* inactive	0	–	ns
t_7	SMEMR* inactive to high-impedance delay	–	20	ns

[a] SMEMR* active-pulse width is determined by IOCHRDY.

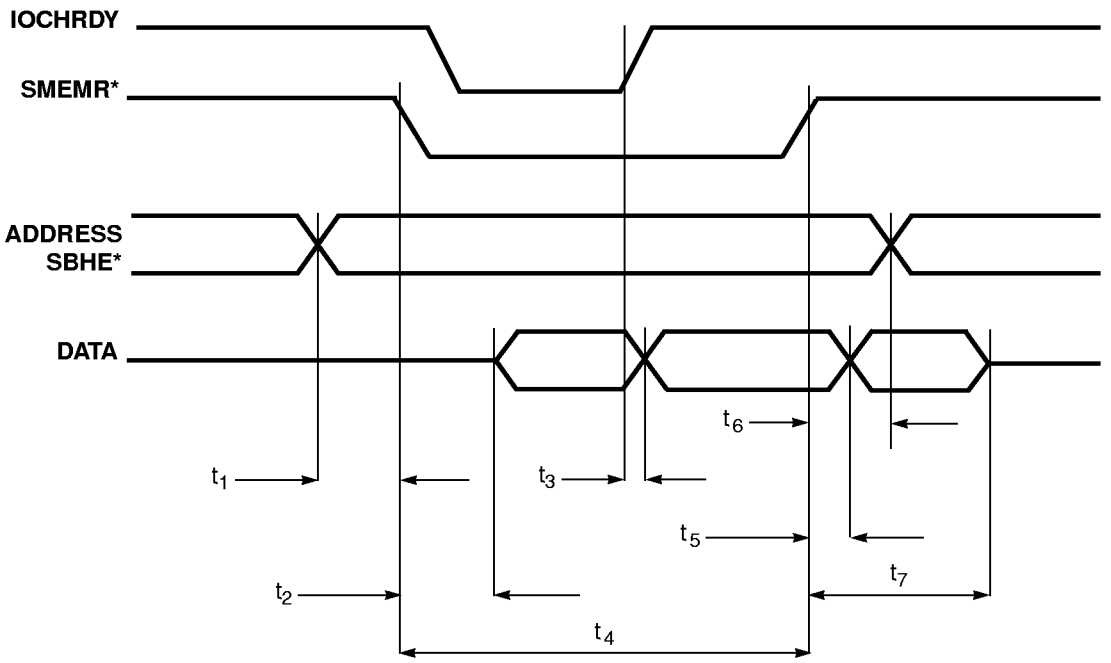


Figure 7-4. Memory Read Timing (ISA Bus — CL-GD5434 only)

Table 7-5. MCS16* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	MCS16* active delay from LA[23:17] valid	–	20	ns
t_{1b}	MCS16* active delay from SA[16:15] valid	–	14	ns
t_2	MCS16* inactive delay from address invalid	–	25	ns

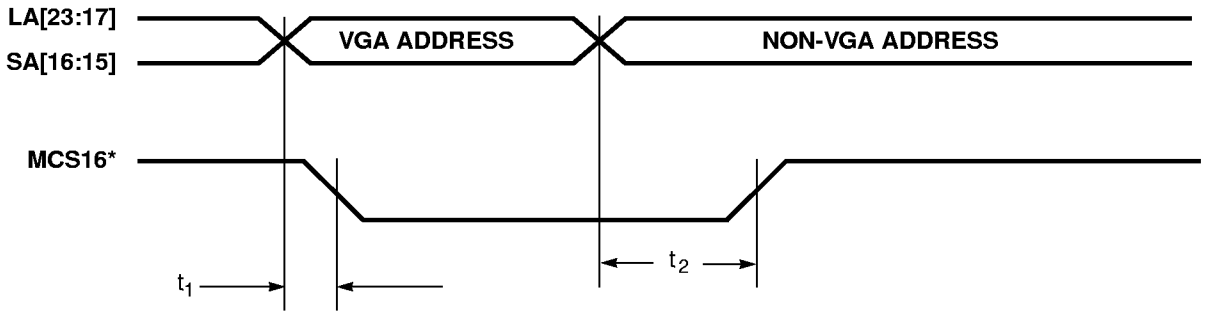


Figure 7-5. MCS16* Timing (ISA Bus — CL-GD5434 only)

Table 7-6. IOCS16* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	IOCS16* active delay from address	–	25	ns
t_2	IOCS16* inactive delay from address	–	30	ns

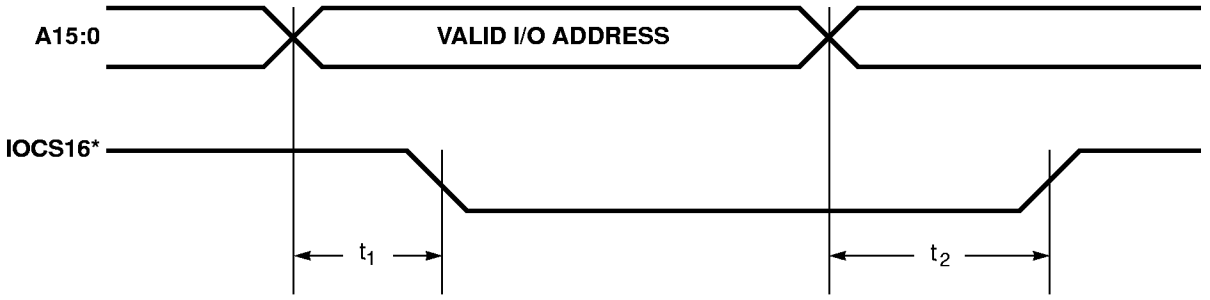


Figure 7-6. IOCS16* Timing (ISA Bus — CL-GD5434 only)

Table 7-7. BALE Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	LA[23:17] setup to BALE negative transition	20	–	ns
t_2	SBHE* setup to BALE negative transition	20	–	ns
t_3	LA[23:17] hold from BALE negative transition	20	–	ns
t_4	SBHE* hold from BALE negative transition	20	–	ns
t_5	BALE pulse width	20	–	ns

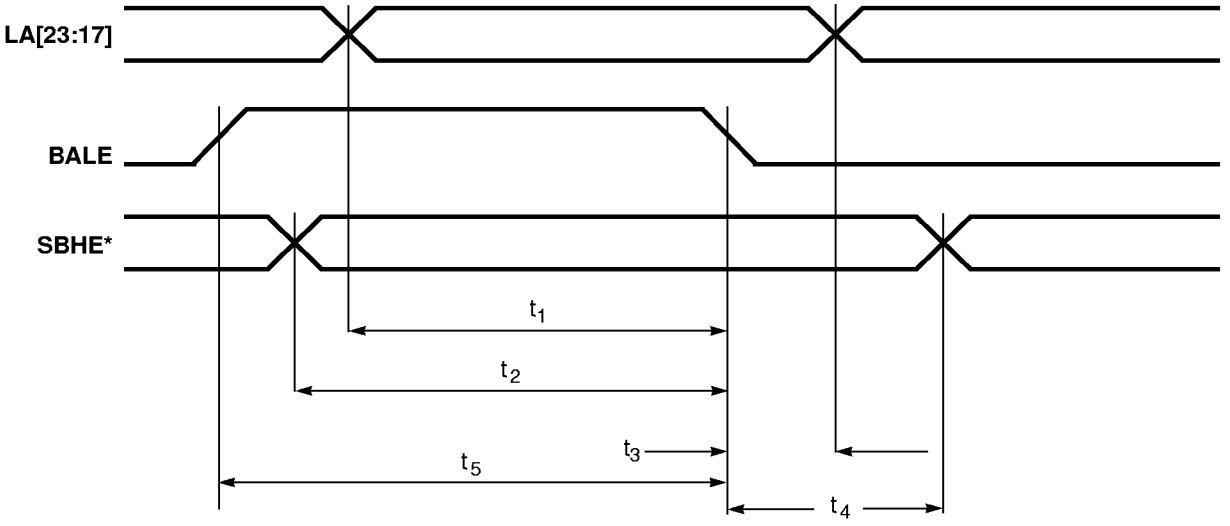


Figure 7-7. BALE Timing (ISA Bus — CL-GD5434 only)

Table 7-8. IOCHRDY for Memory Access Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	SMEMR* or SMEMW* active to IOCHRDY inactive low	–	28	ns
t_2	IOCHRDY inactive low pulse width	10	[a]	ns

[a] Video mode dependent.

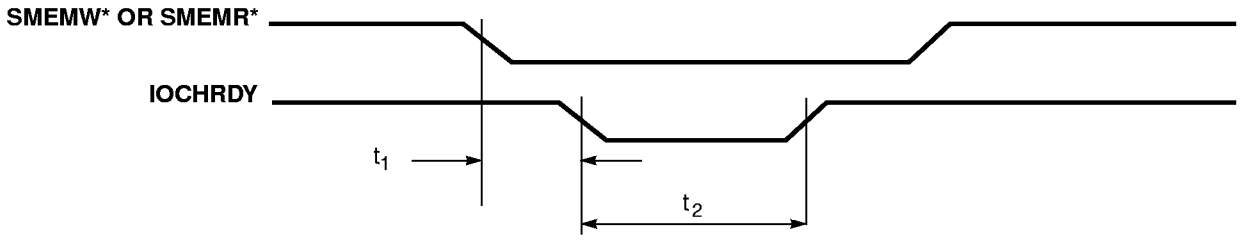
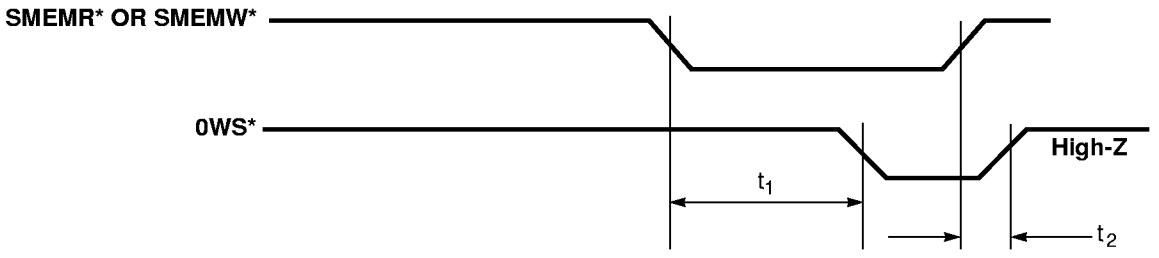


Figure 7-8. IOCHRDY for Memory Access Timing (ISA Bus — CL-GD5434 only)

Table 7-9. 0WS* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	0WS* active delay from SMEMR* (BIOS access)	–	22	ns
t_{1b}	0WS* active delay from SMEMW* (Display Memory write)	–	18	ns
t_{2a}	0WS* high-impedance delay from SMEMR*	–	18	ns
t_{2b}	0WS* high-impedance delay from SMEMW*	–	19	ns



High-Z = High-impedance

Figure 7-9. 0WS* Timing (ISA Bus — CL-GD5434 only)

Table 7-10. Refresh Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	REFRESH* active setup to SMEMR* active	20	–	ns
t_2	REFRESH* active hold from SMEMR* active	0	–	ns

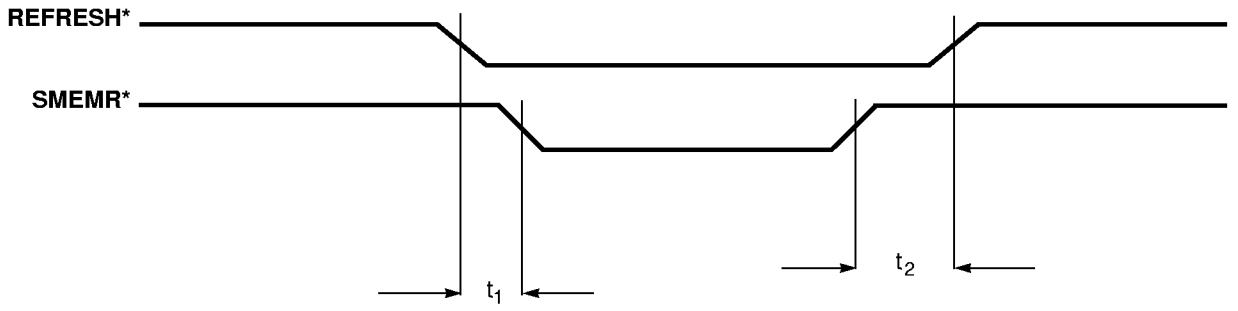


Figure 7-10. Refresh Timing (ISA Bus — CL-GD5434 only)

Table 7-11. EROM* Timing (ISA Bus — CL-GD5434 only)

Symbol	Parameter	MIN	MAX	Units
t_1	EROM* active delay from SMEMR* active	–	30	ns
t_2	EROM* inactive delay from SMEMR* inactive	–	20	ns

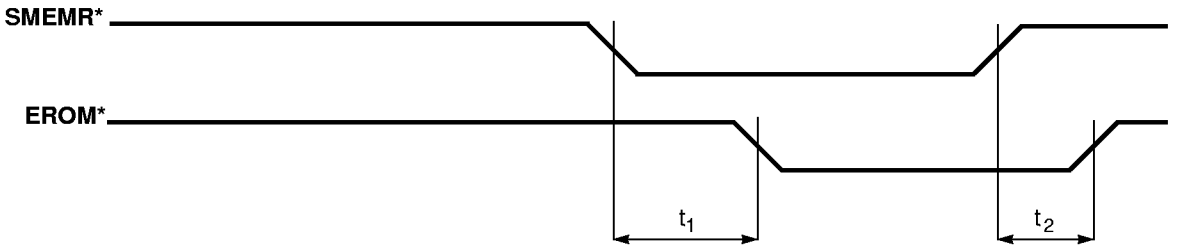


Figure 7-11. EROM* Timing (ISA Bus — CL-GD5434 only)

Table 7-12. AEN Timing (ISA Bus — CL-GD5434 only)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	AEN setup to IOR* or IOW* active	5	–	ns
t_2	AEN hold from IOR* or IOW* inactive	5	–	ns

[a] AEN high, as shown below, will cause the CL-GD543X/'4X to **ignore** the I/O cycle.

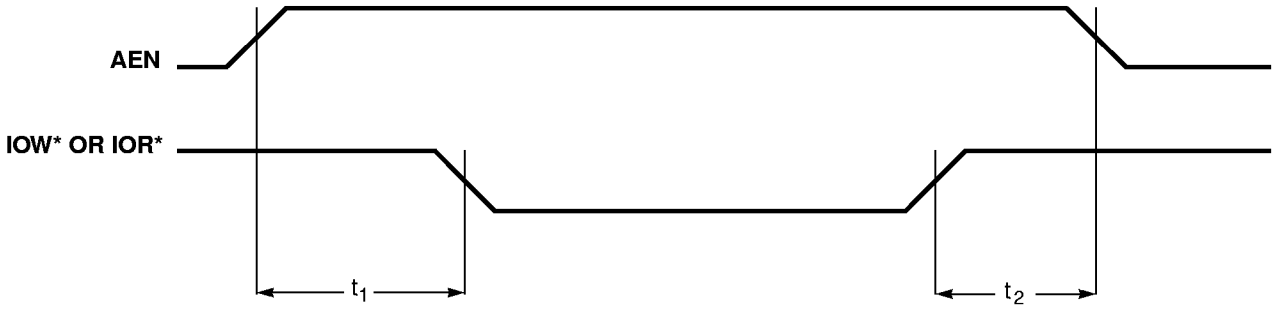


Figure 7-12. AEN Timing (ISA Bus — CL-GD5434 only)

Table 7-13. LCLK, CLK Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time (LCLK) VESA VL-Bus (CL-GD5430/'34/'40 only)	–	4	ns
t_2	Fall time (LCLK) VESA VL-Bus (CL-GD5430/'34/'40 only)	–	4	ns
t_3	High period (LCLK) VESA VL-Bus (CL-GD5430/'34/'40 only)	40	60	% t_5
t_4	Low period (LCLK) VESA VL-Bus (CL-GD5430/'34/'40 only)	40	60	% t_5
t_5	Period (LCLK) VESA VL-Bus (CL-GD5430/'34/'40 only)	20	–	ns
t_1	Rise time (CLK) PCI bus	–	4	ns
t_2	Fall time (CLK) PCI bus	–	4	ns
t_3	High period (CLK) PCI bus	40	60	% t_5
t_4	Low period (CLK) PCI bus	40	60	% t_5
t_5	Period (CLK) PCI bus	30	–	ns

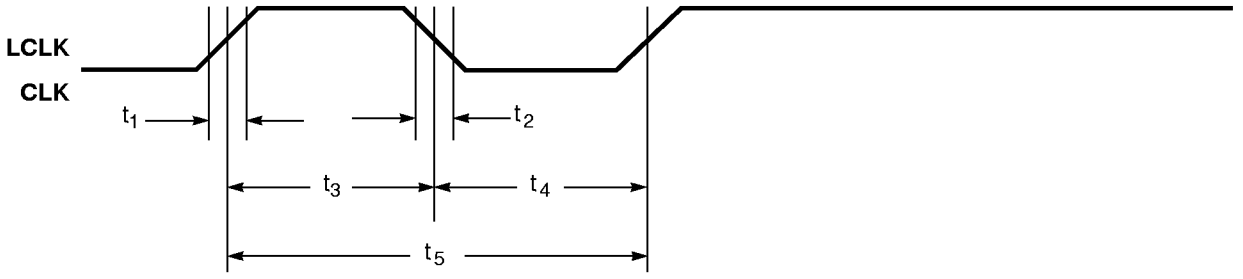
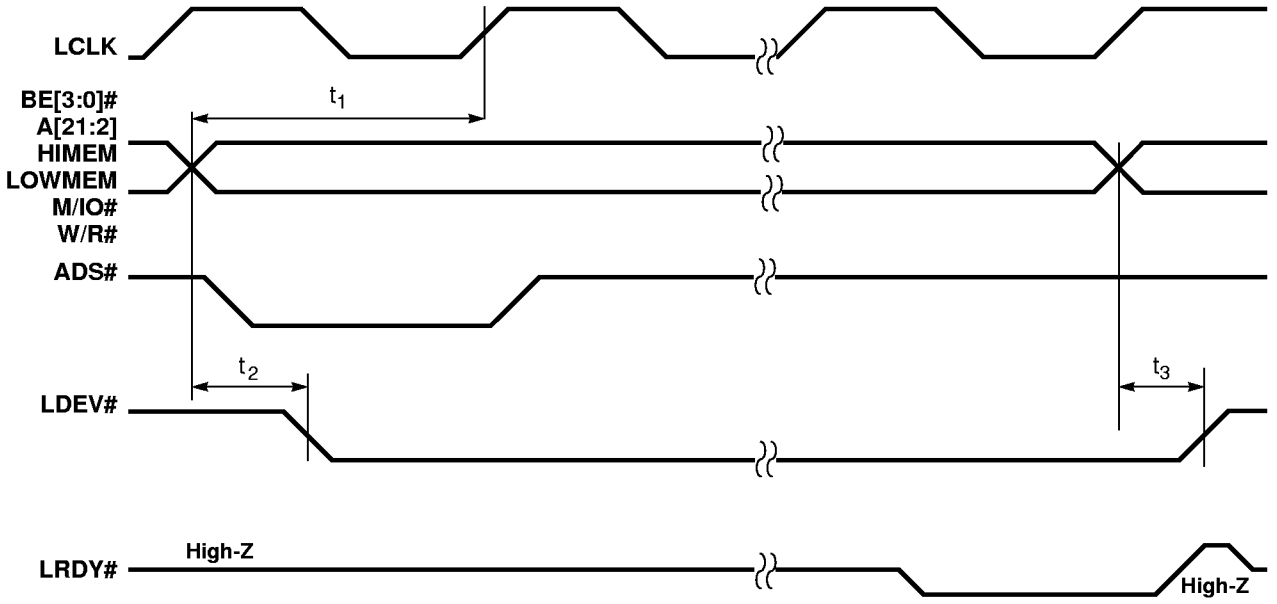


Figure 7-13. LCLK, CLK Timing

Table 7-14. ADS# and LDEV# Timing ('486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, Status, ADS# setup to LCLK	7	–	ns
t_2	LDEV# active delay from Address, Status (20-pF loading)	0	20	ns
t_3	LDEV# inactive delay from Address, Status	0	20	ns

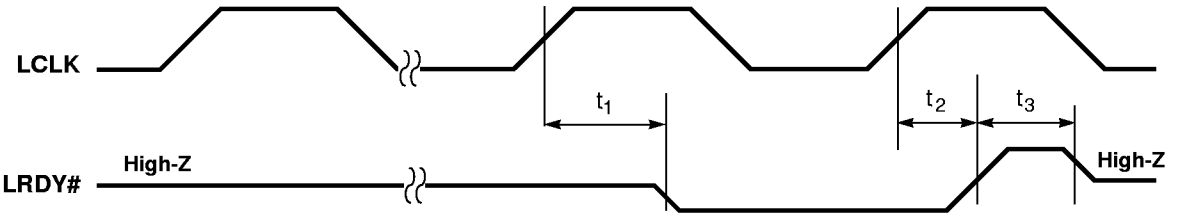


High-Z = High-impedance

Figure 7-14. ADS#, and LDEV# Timing ('486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Table 7-15. LRDY# Delay ('486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Symbol	Parameter	MIN	MAX	Units
t_1	LRDY# active delay from LCLK	–	13	ns
t_2	LRDY# inactive delay from LCLK	–	13	ns
t_3	LRDY# high before high-impedance	0.4	0.5	LCLK



High-Z = High-impedance

Figure 7-15. LRDY# Delay (486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Table 7-16. Read Data/RDYRTN# Timing ('486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup to LCLK	4	–	ns
t_2	Read data hold from LCLK	2	–	ns
t_3	RDYRTN# setup to LCLK	5	–	ns
t_4	LRDY high	0.4	0.5	LCLK

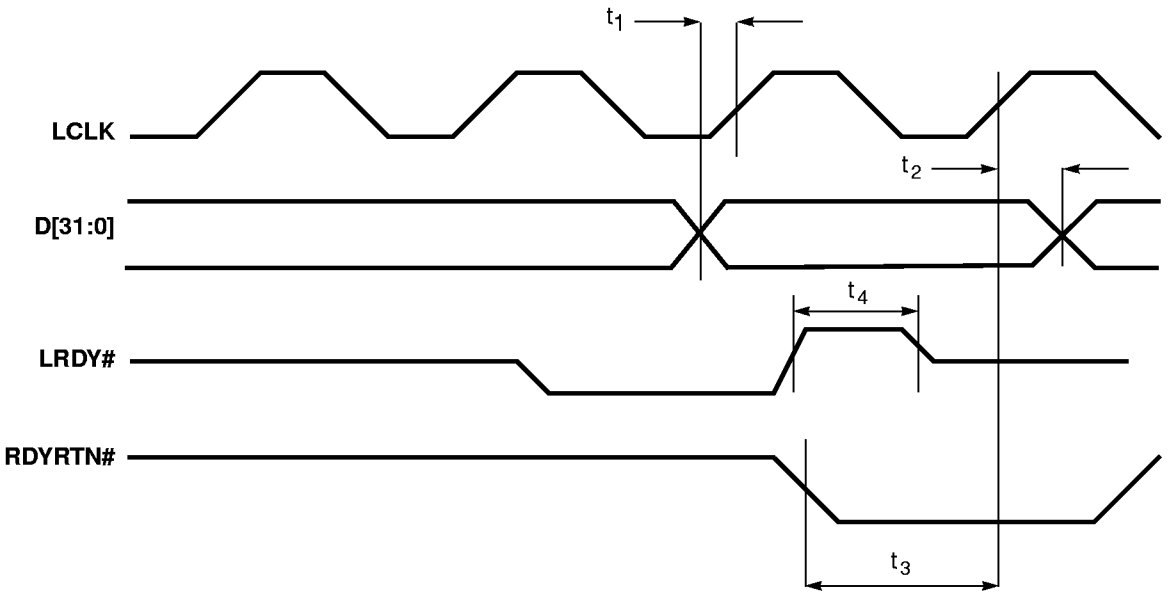


Figure 7-16. Read Data/RDYRTN# Timing ('486/VESA® VL-Bus™) (CL-GD5430/'34/'40 only)

Table 7-17. FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	FRAME# setup to CLK	7	–	ns
t_2	AD[31:0] (Address) setup to CLK	7	–	ns
t_3	AD[31:0] (Address) hold from CLK	0	–	ns
t_4	AD[31:0] (Data) setup to CLK	7	–	ns
t_5	AD[31:0] (Data) hold from CLK	0	–	ns
t_6	AD[31:0], C/BE[3:0]# high-impedance from CLK	0	28	ns
t_7	C/BE[3:0]# (bus CMD) setup to CLK	7	–	ns
t_8	C/BE[3:0]# (bus CMD) hold from CLK	0	–	ns
t_{8a}	C/BE[3:0]# (byte enable) setup to CLK	7	–	ns
t_9	DEVSEL# delay from CLK	–	15	ns
t_{10}	DEVSEL# high before high-impedance	1	–	CLK

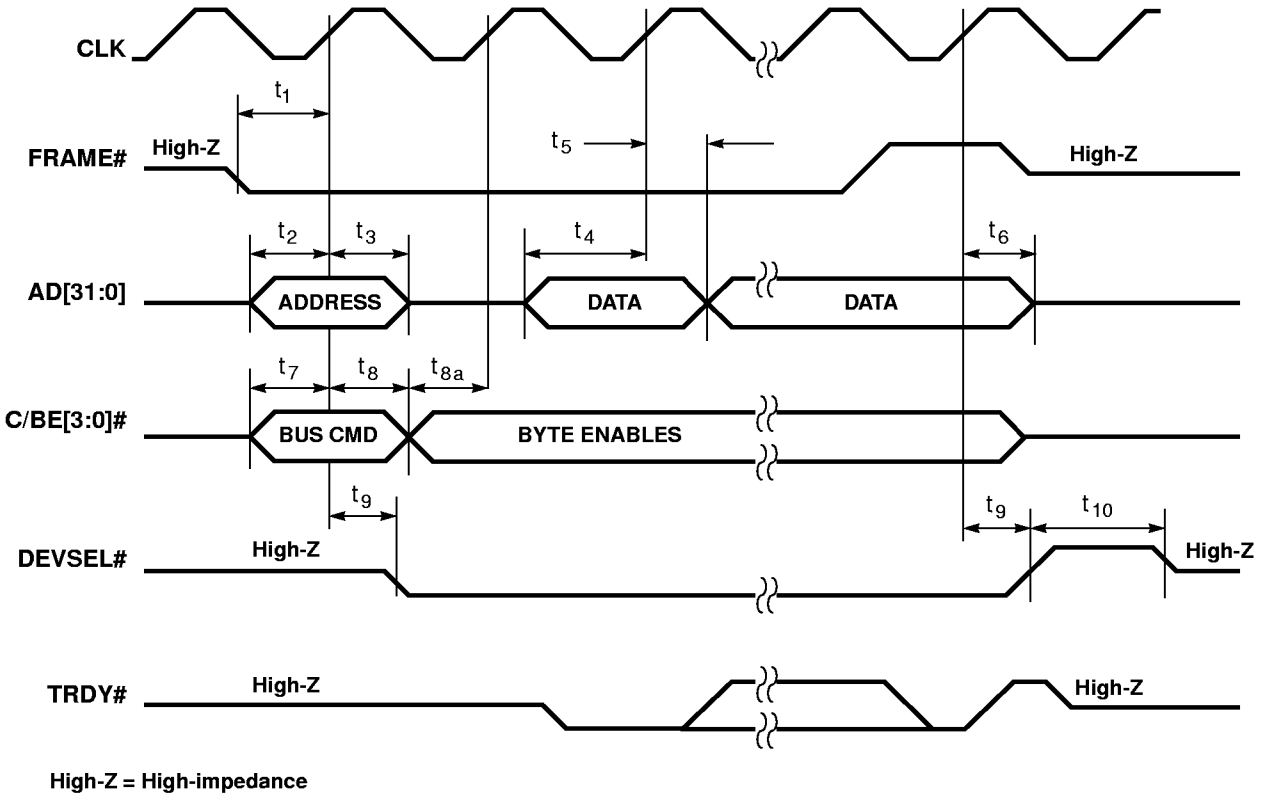
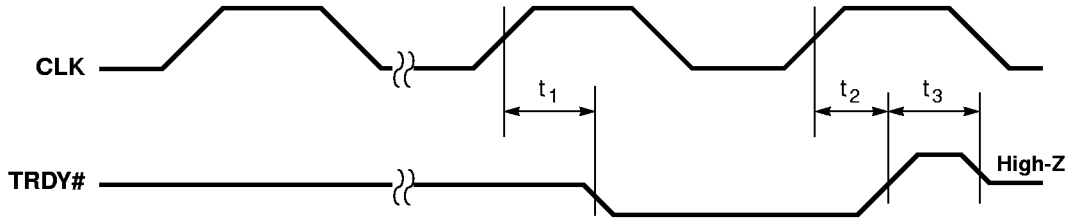


Figure 7-17. FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# (PCI Bus)

Table 7-18. TRDY# Delay (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	TRDY# active delay from CLK	–	12	ns
t_2	TRDY# inactive delay from CLK	–	12	ns
t_3	TRDY# high before high-impedance	1	–	CLK



High-Z = High-impedance

Figure 7-18. TRDY# Delay (PCI Bus)

Table 7-19. Read Data/IRDY# Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup to TRDY# active	7	–	ns
t_2	Read data hold from TRDY# inactive	0	–	ns
t_3	IRDY# setup to CLK	7	–	ns
t_4	IRDY# hold from CLK	0	–	ns

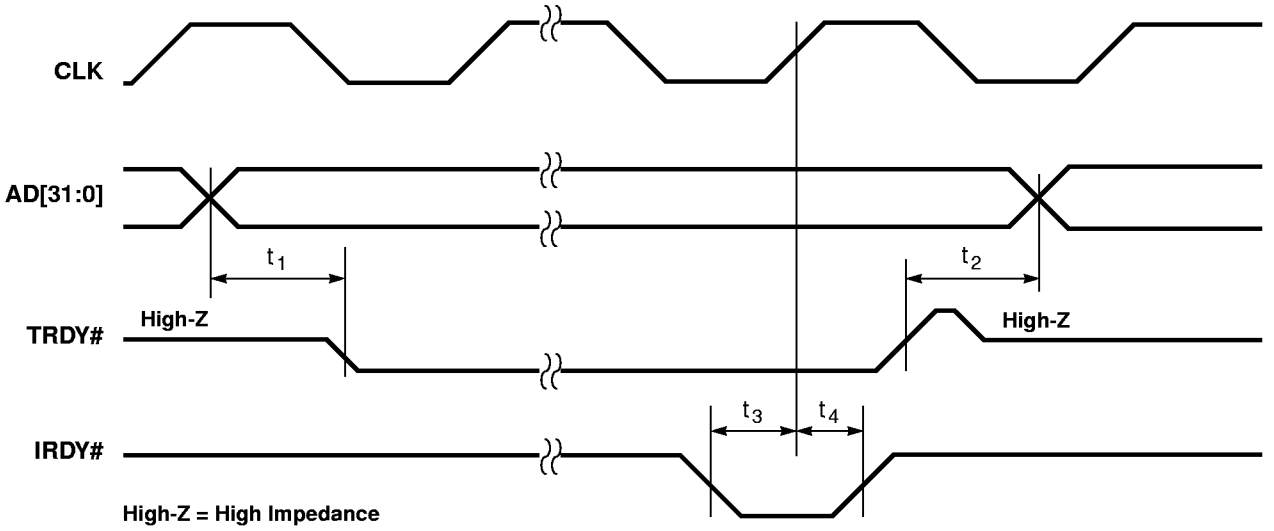
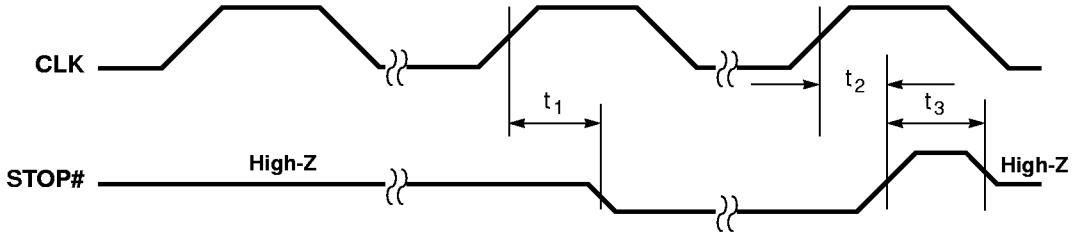


Figure 7-19. Read Data/IRDY# (PCI Bus)

Table 7-20. STOP# Delay (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	STOP# active delay from CLK	–	15	ns
t_2	STOP# inactive delay from CLK	–	15	ns
t_3	STOP# high before high-impedance	1	–	CLK



High-Z = High Impedance

Figure 7-20. STOP# Delay (PCI Bus)

Table 7-21. IDSEL Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	IDSEL setup to CLK	–	15	ns

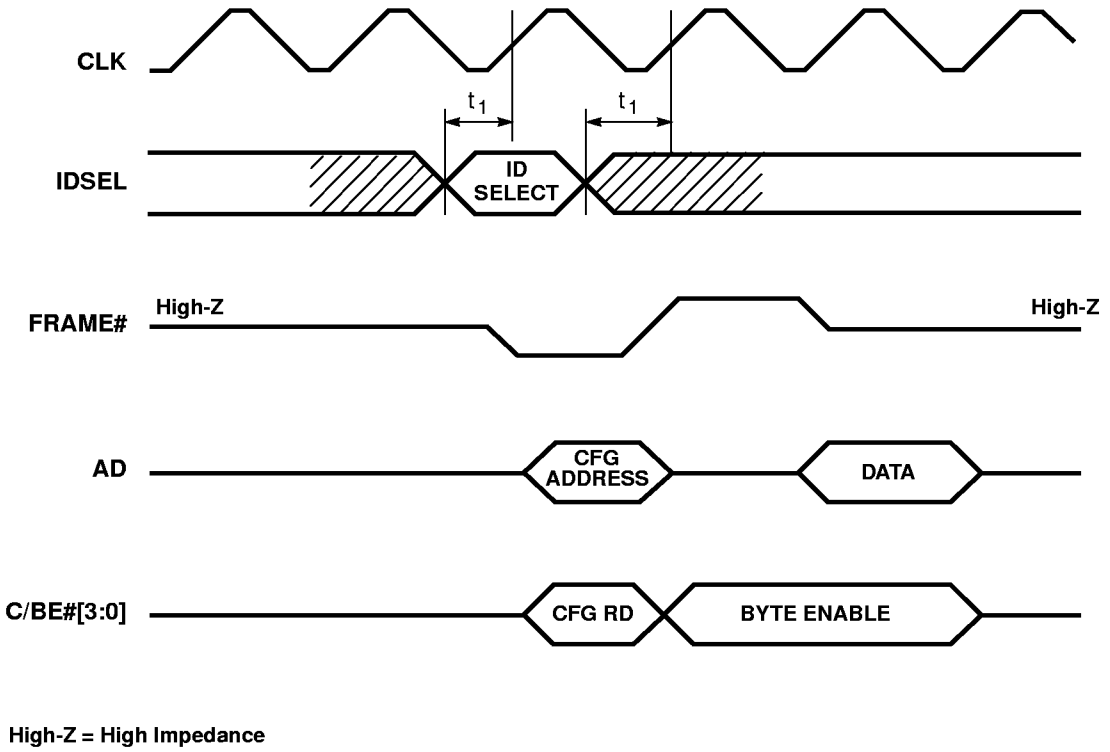
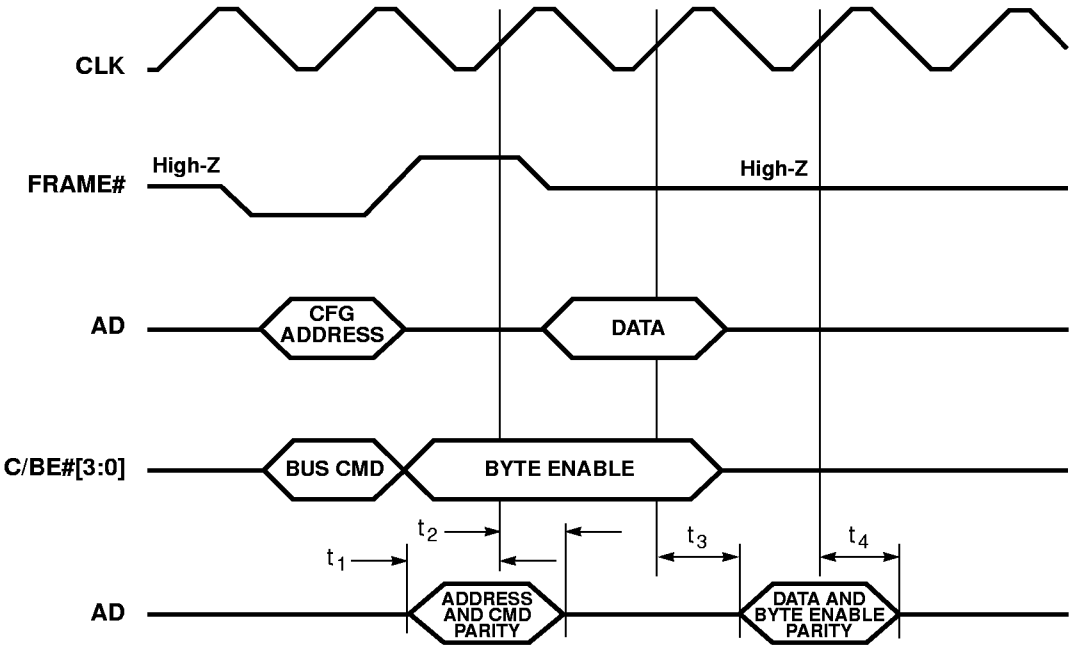


Figure 7-21. IDSEL Timing (PCI Bus)

Table 7-22. PAR Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	PAR setup from CLK (input to CL-GD543X/'4X)	7	–	ns
t_2	PAR hold from CLK (input to CL-GD543X/'4X)	0	–	ns
t_3	PAR delay from CLK (output from CL-GD543X/'4X)	7	–	ns
t_4	PAR hold from CLK (output from CL-GD543X/'4X)	0	–	ns

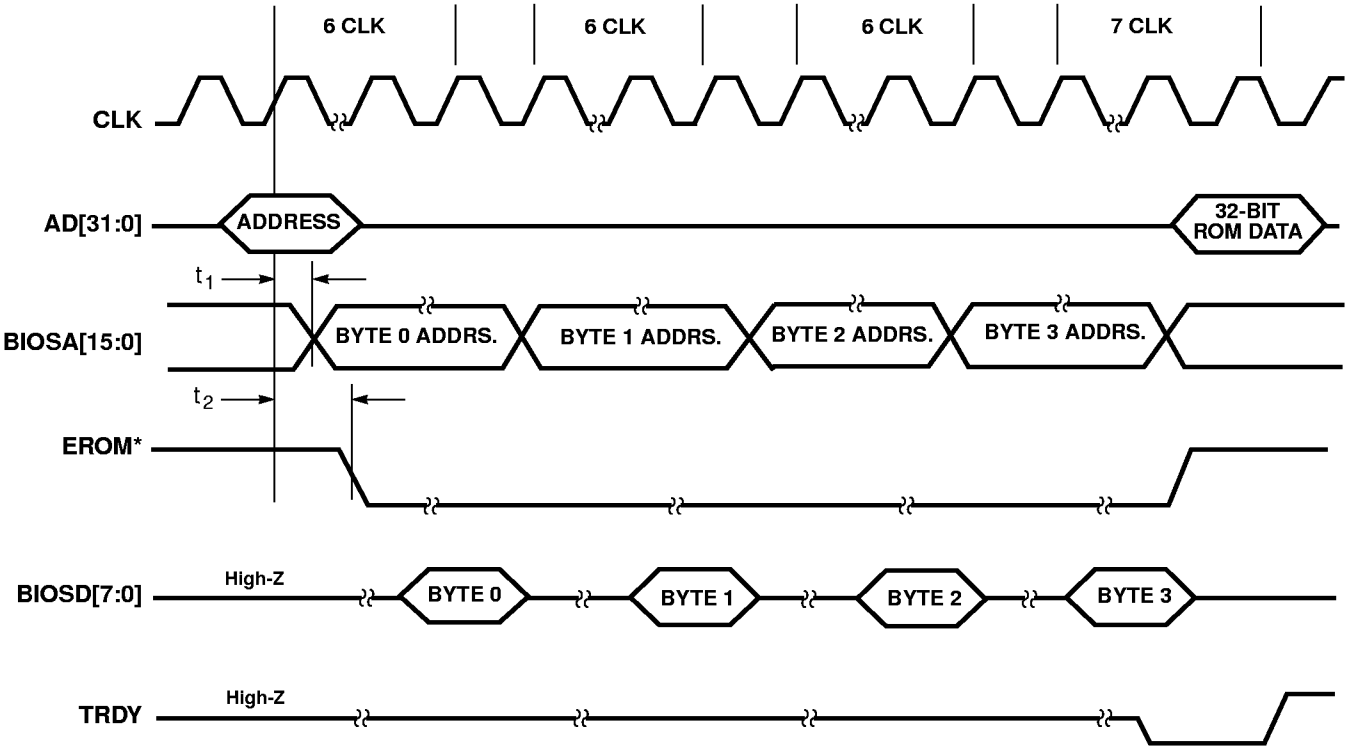


High-Z = High Impedance

Figure 7-22. PAR Timing (PCI Bus)

Table 7-23. EROM*, BIOSA[15:0] Timing (PCI Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	BIOSA[15:0] delay from CLK	–	80	ns
t_2	EROM* delay from CLK	–	50	ns



High-Z = High impedance

Figure 7-23. EROM*, BIOSA[15:0] Timing (PCI Bus)

Table 7-24. CAS*-before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX
t_1	t_{CSR}: CAS* active setup to RAS* active	1 m[b]	–
t_2	t_{RAS}: RAS* low pulse width	4 m	–
t_3	t_{RP}: RAS* high pulse width	3 m	–

[a] There will be either three or five RAS* pulses while CAS* remains low. On the CL-GD5436, GR18[3] can be programmed to '1' for a single RAS* pulse.

[b] m = MCLK

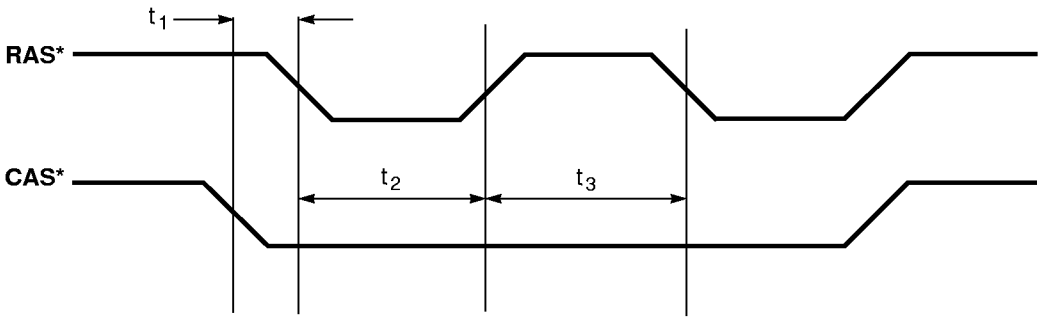


Figure 7-24. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 7-25. Display Memory Bus: Common Parameters

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: Address setup to RAS* active	1.5 m – 9 ns [a]	–
t_2	t_{RAH}: Row Address hold from RAS* active	1.5 m – 5 ns	–
t_3	t_{ASC}: Address Setup to CAS* active	1 m – 3 ns	–
t_4	t_{CAH}: Column Address hold from CAS* active	1 m	–
t_5	t_{RCD}: RAS* active to CAS* active delay (standard RAS)	2.5 m – 7.5 ns	–
t_5	t_{RCD}: RAS* active to CAS* active delay (extended RAS)	3 m	–
t_6	t_{RAS}: RAS* pulse width low (standard RAS)	3.5 m	–
t_6	t_{RAS}: RAS* pulse width low (extended RAS)	4 m – 1 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — standard RAS)	2.5 m – 2 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high — extended RAS)	3 m – 1.5 ns	–
t_8	t_{CAS}: CAS* pulse width low	1 m + 3 ns	1m + 6 ns
t_9	t_{CP}: CAS* precharge (CAS* pulse width high)	1 m – 6 ns	1m – 3 ns
t_{10}	t_{RC}: Random cycle (standard RAS)	6 m	–
t_{10}	t_{RC}: Random cycle (extended RAS)	7 m	–
t_{11}	t_{PC}: Page mode cycle	2 m	–

[a] m = MCLK

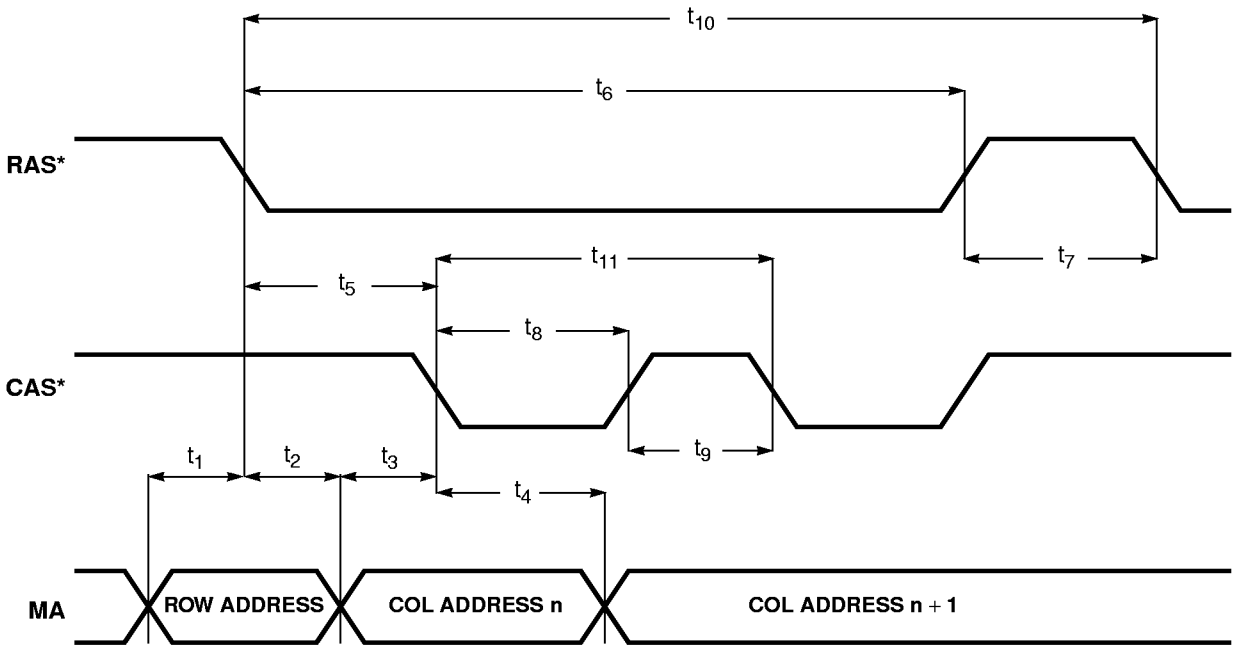


Figure 7-25. Display Memory Bus: Common Parameters

Table 7-26. Display Memory Bus: Read Cycles

Symbol	Parameter	MIN	MAX
t_1	Read data setup to CAS* rising edge	0	–
t_2	Read data hold from CAS* high	10 ns	–

Only parameters t_1 and t_2 are defined for the CL-GD543X/'4X. The remaining parameters in this table are calculated from parameters from this table and the previous table. These parameters are provided so that system designers can easily determine DRAM requirements.

t_3	DRAM access time from RAS* (standard RAS)	–	3.5 m – 1 ns
t_3	DRAM access time from RAS* (extended RAS)	–	4 m – 1 ns
t_4	DRAM access time from Column Address	–	2 m
t_5	DRAM access time from CAS* active	–	1 m + 3 ns
t_6	DRAM access time from CAS* precharge	–	2 m

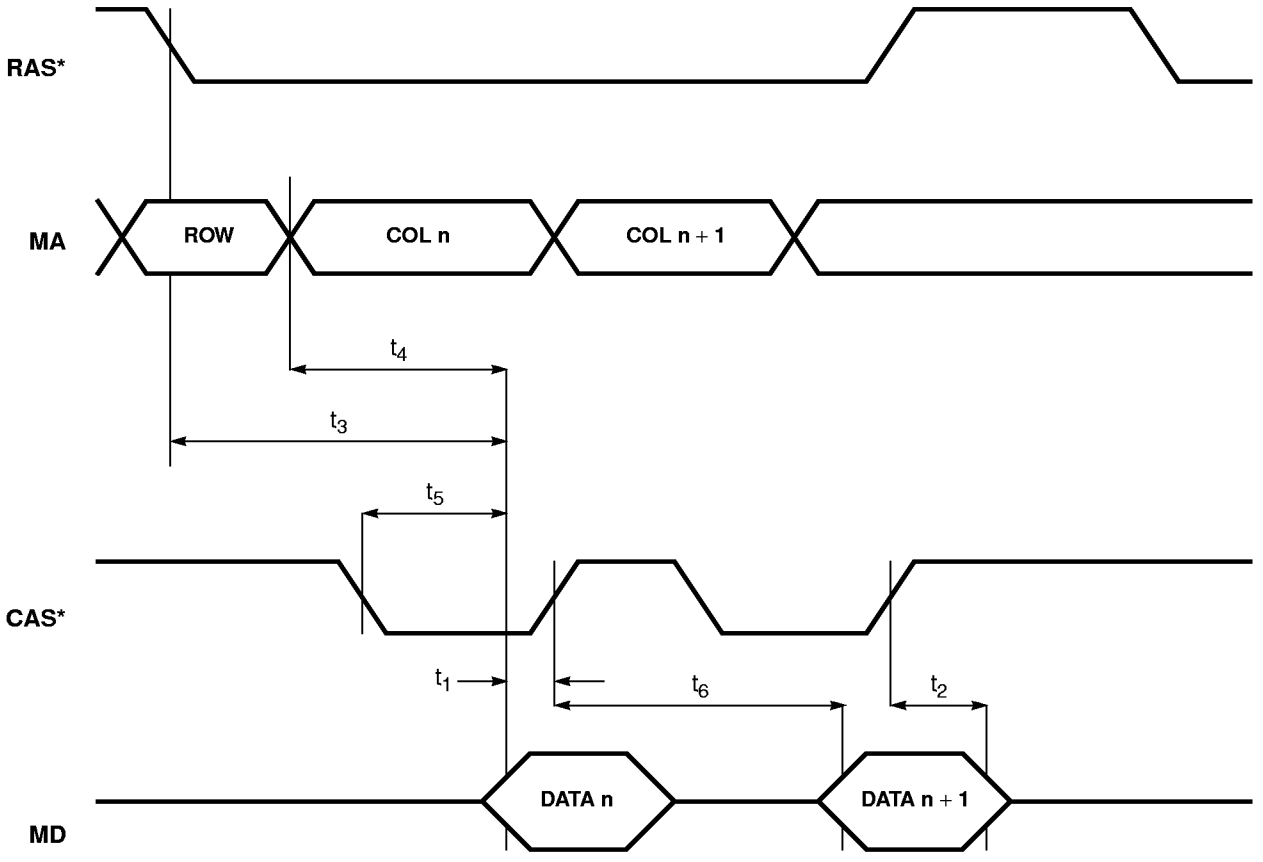


Figure 7-26. Display Memory Bus: Read Cycles

Table 7-27. Display Memory Bus: Write Cycles[a]

Symbol	Parameter	MIN	MAX
t_1	t_{CWL}: WE* active setup to CAS* active	1 m + 0.5 ns[b]	–
t_2	t_{DS}: Write data setup to CAS* active (GR18[1:0] = 00)	1 m – 2 ns	–
t_2	t_{DS}: Write data setup to CAS* active (GR18[1:0] = 11)	0.5 m – 2 ns	–
t_3	t_{DH}: Write data hold from CAS* active	1 m + 1 ns	–
t4	t_{WCH}: WE active hold from CAS* active	1.5 m – 2 ns	–

[a] GR18[1:0] must always be programmed identically.
[b] m = MCLK

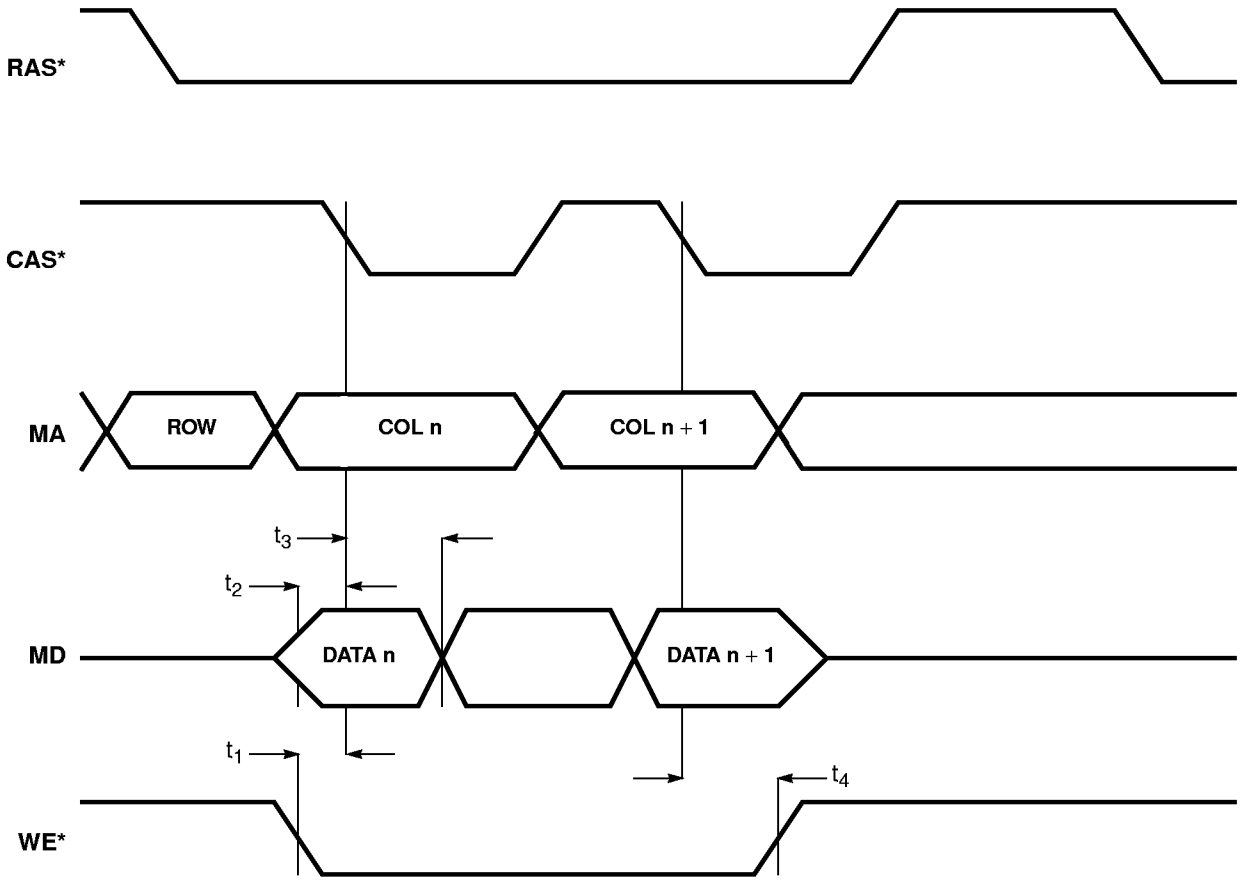


Figure 7-27. Display Memory Bus: Write Cycles

Table 7-28. Display Memory Bus: Common Parameters (EDO Timing — CL-GD5436)

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: Address setup to RAS* active	1.5 m – 9 ns [a]	–
t_2	t_{RAH}: Row Address hold from RAS* active	1.5 m – 5 ns	–
t_3	t_{ASC}: Address setup to CAS* active	1m – 3 ns	–
t_4	t_{CAH}: Column Address hold from CAS* active	1 m	–
t_5	t_{RCD}: RAS* active to CAS* active delay (EDO timing)	4 m	–
t_6	t_{RAS}: RAS* pulse width low (EDO timing)	5 m – 1 ns	–
t_7	t_{RP}: RAS* precharge (RAS* pulse width high) (EDO timing)	3 m + 1.5 ns	–
t_8	t_{CAS}: CAS* pulse width low	1m + 3 ns	1m + 6 ns
t_9	t_{CP}: CAS* precharge (CAS* pulse width high)	1m – 6 ns	1m – 3 ns
t_{10}	t_{RC}: Random cycle (EDO timing)	8 m	–
t_{11}	t_{PC}: Page mode cycle	2 m	–
t_{12}	t_{CAS}: CAS* pulse width low (last CAS* of Page mode read burst)	3 m	–
t_{13}	t_{CRP}: CAS* to RAS* precharge	1 m	–

[a] m = MCLK

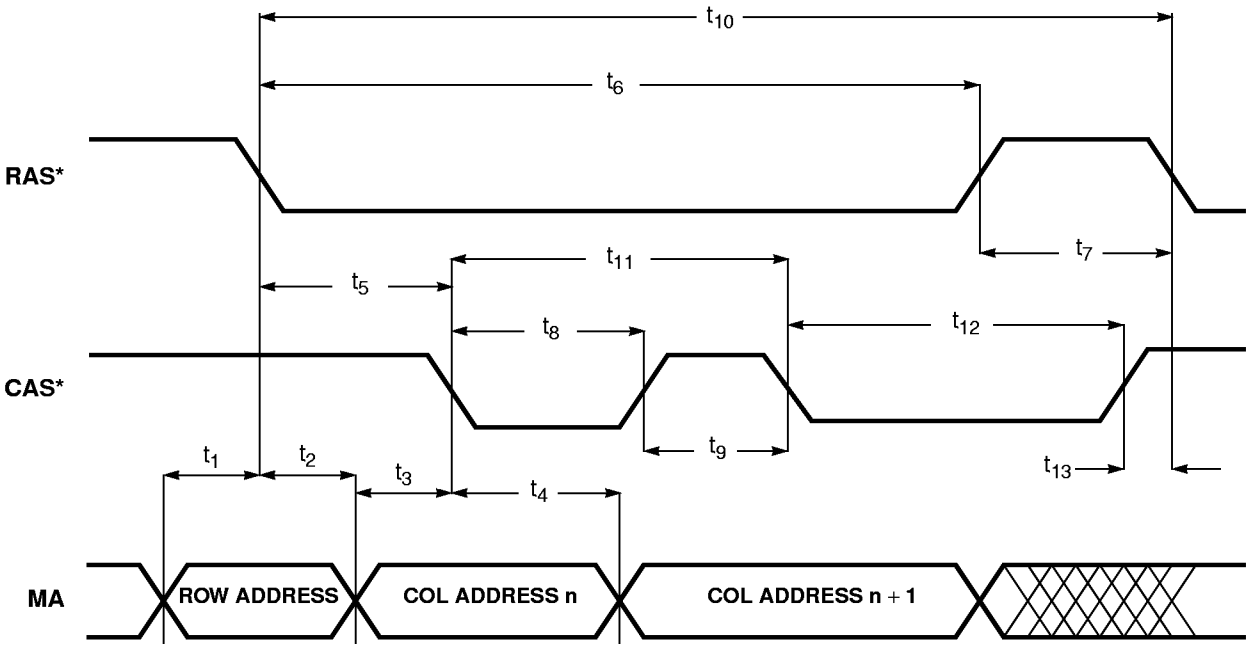


Figure 7-28. Display Memory Bus: Common Parameters (EDO Timing — CL-GD5436)

Table 7-29. Display Memory Bus: Read Cycles (EDO Timing — CL-GD5436)

Symbol	Parameter	MIN	MAX
t_1	Read data setup to CAS* falling edge	1 ns	–
t_2	Read data hold from CAS* falling edge	5 ns	–

The timing shown in this table and figure are for EDO Mode DRAM timing. See the description of register GR18[2]. This timing requires the display memory be populated with EDO DRAMs. These devices hold their read data valid past the rising edge of CAS*.

Depending on the cycle being executed, the read data setup and hold times may be defined with respect to CAS* falling edge (Page mode cycle other than last), WE* falling edge (read followed by write), or a timing term that is available only internally (Last Page mode cycle). If the DRAM can meet the timing requirements of the falling CAS* edge case, it will meet the other two cases.

Only parameters t_1 and t_2 are defined for the CL-GD543X/'4X. The remaining parameters in this table are calculated from parameters from this table and the previous table. These parameters are provided so that system designers can easily determine DRAM requirements.

t_3	DRAM access time from RAS* (EDO timing)	–	5 m
t_4	DRAM access time from column address (EDO timing)	–	3 m
t_5	DRAM access time from CAS* active (EDO timing)	–	2 m
t_6	DRAM access time from CAS* precharge (EDO timing)	–	3 m

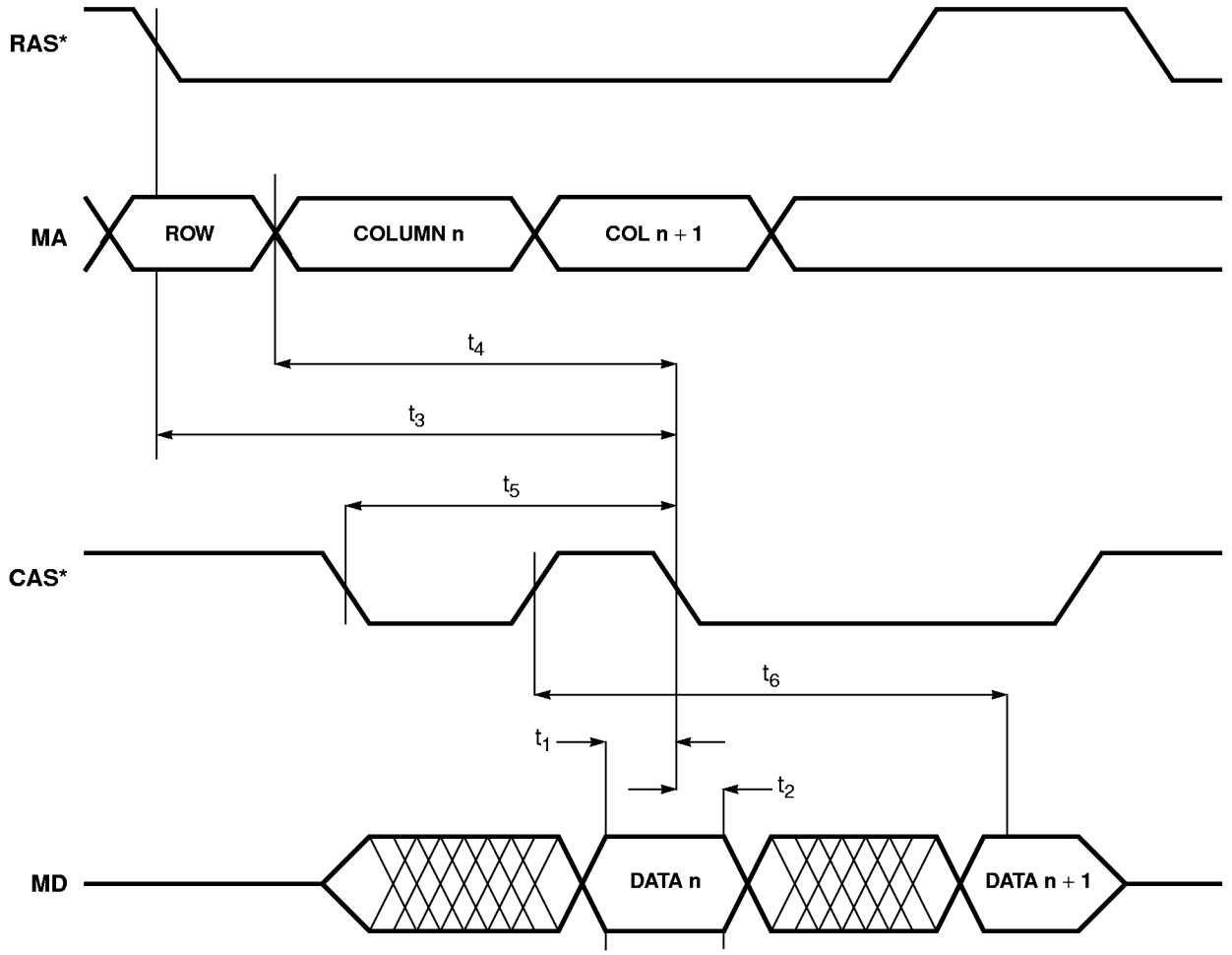


Figure 7-29. Display Memory Bus: Read Cycles (EDO Timing — CL-GD5436)

Table 7-30. Display Memory Bus: BitBLT R/W Cycle (CL-GD5436 only)

Symbol	Parameter	Nominal	
		Non-EDO GR18[2] = 0	EDO GR18[2] = 1
t_1	Write data setup to CAS# active (GR18[1:0] = 00)	1 m[a]	1 m
t_1	Write data setup to CAS# active (GR18[1:0] = 11)	0.5 m	0.5 m
t_2	t_{CP}: read CAS# to write CAS# delay (GR18[1:0] = 00)	3 m	4 m
t_2	t_{CP}: read CAS# to write CAS# delay (GR18[1:0] = 11)	2 m	3 m
t_3	WE# active delay from CAS# inactive	1 m	1 m

[a] m = MCLK

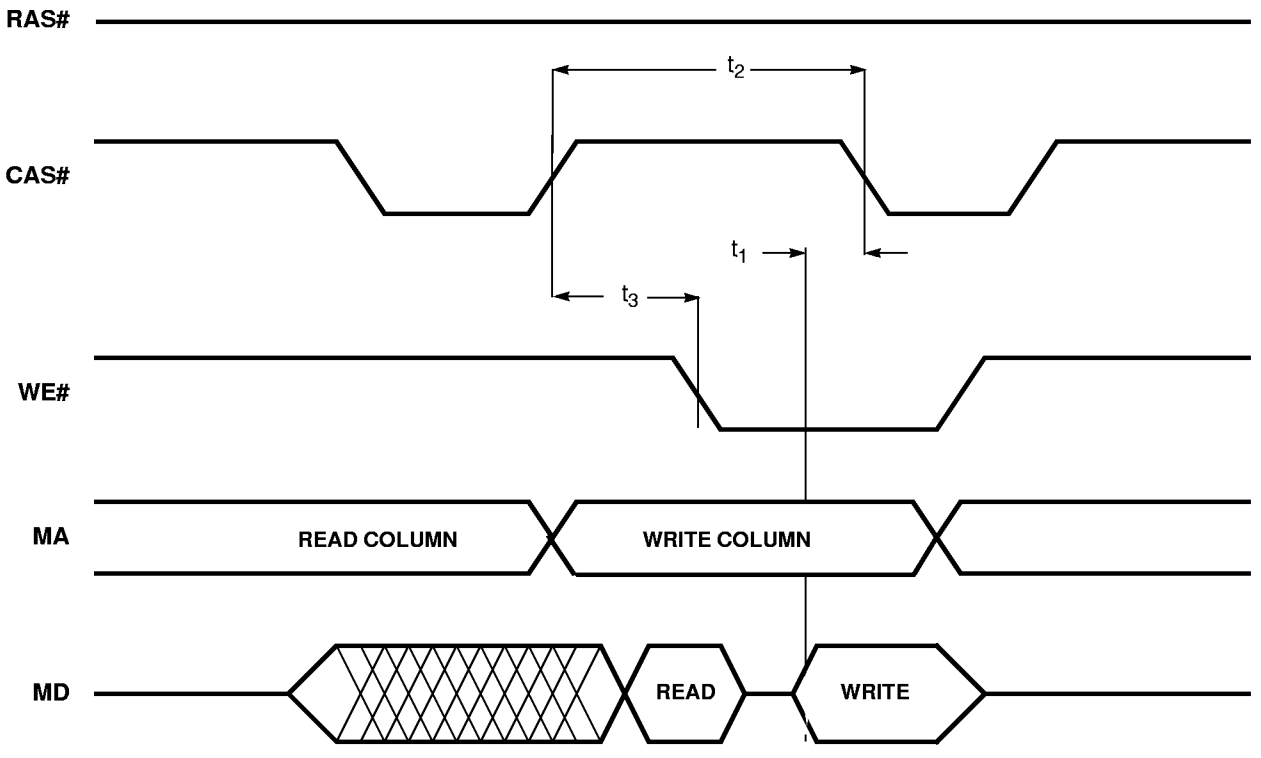


Figure 7-30. Display Memory Bus: BitBLT R/W Cycle (CL-GD5436 only)

Table 7-31. P-Bus as Inputs: 8-Bit Mode (DCLK input as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* setup to DCLK	0	–	ns
t_2	P[7:0], BLANK* hold from DCLK	6	–	ns

NOTE: The CL-GD543X/'4X RAMDAC is driven externally. For CL-GD543X/'4X Overlay modes, BLANK* is an output.

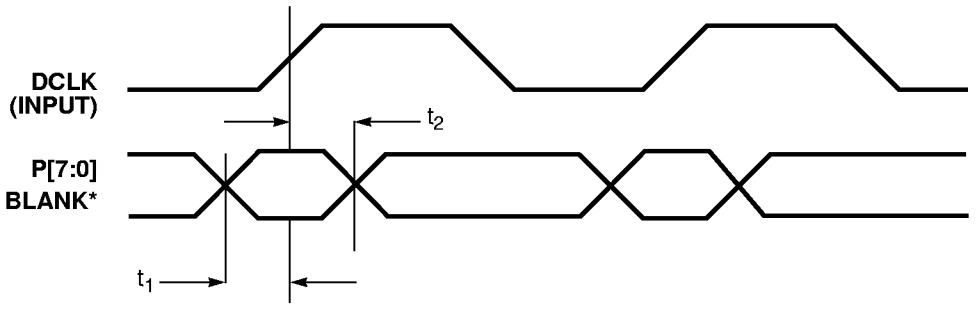


Figure 7-31. P-Bus as Inputs: 8-Bit Mode (External DCLK)

Table 7-32. Feature Bus Timing: 8-Bit Mode, Outputs (DCLK output as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK* delay	–1	1	ns
t_2	DCLK to HSYNC, VSYNC delay	1	3	ns
t_3	DCLK to P[7:0] delay	–2	0	ns
t_4	DCLK to OVRW* delay	–1	1	ns

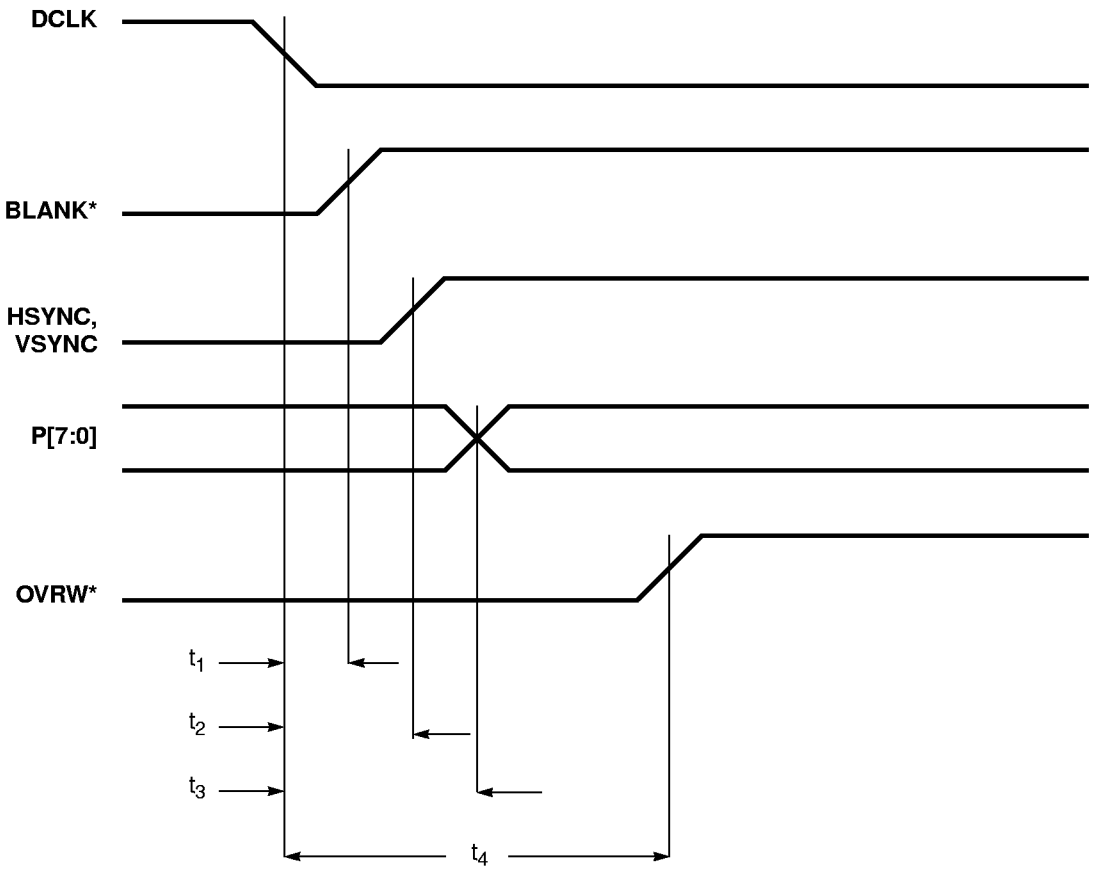


Figure 7-32. Feature Bus Timing: 8-Bit Mode, Outputs (Internal DCLK)

Table 7-33. P-Bus as Outputs: 16-Bit Mode (DCLK output as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK (rising edge) to P[7:0] delay	–2	0	ns
t_2	DCLK (falling edge) to P[7:0] delay	–1	1	ns

NOTE: Register SR7[2:1] = '0,1' and register GRE[0] = '1'.

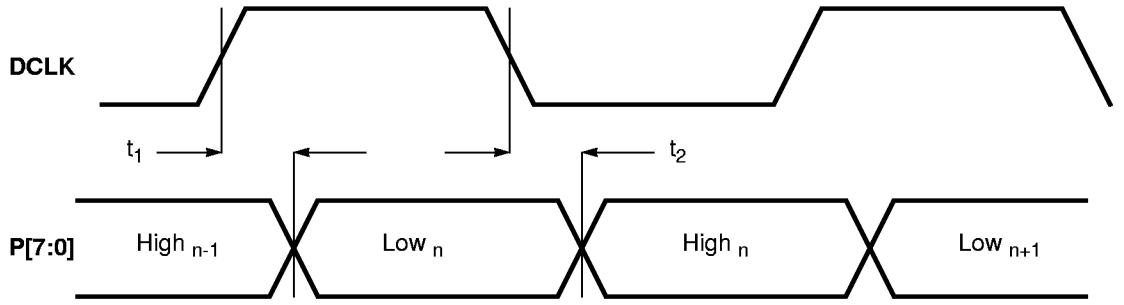


Figure 7-33. P-Bus as Outputs: 16-Bit Mode (Internal DCLK)

Table 7-34. P-Bus as Inputs: 16-Bit Mode (DCLK input as reference)

Symbol	Parameter	MIN 'GD5430	MIN 'GD5434	MIN 'GD5436	Units
t_1	P[7:0] setup to DCLK (rising edge — external DCLK)	–4	–2	tbd	ns
t_2	P[7:0] hold from DCLK (rising edge — external DCLK)	8	5	tbd	ns
t_3	P[7:0] setup to DCLK (falling edge — external DCLK)	–4	–2	tbd	ns
t_4	P[7:0] hold from DCLK (rising edge — external DCLK)	8	5	tbd	ns

NOTE: Clock mode 1 selected in Hidden DAC register (D5 = '0').

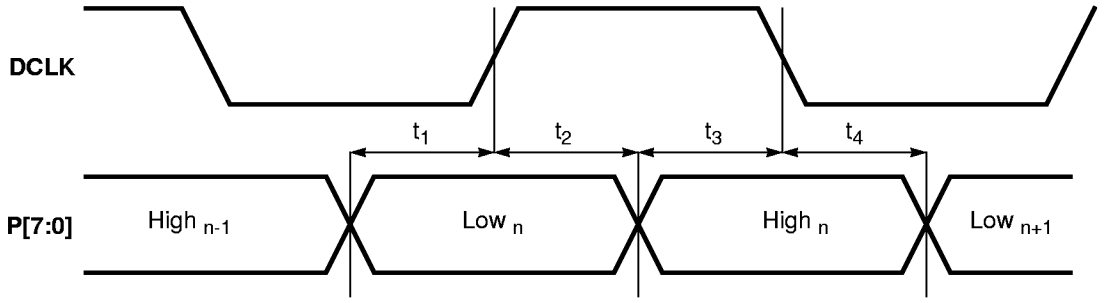


Figure 7-34. P-Bus as Inputs: 16-Bit Mode (External DCLK)

Table 7-35. P-Bus as Inputs: 16-Bit Mode, Clock Mode 2 (DCLK input as reference)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* setup to DCLK	–2	–	ns
t_2	P[7:0], BLANK* hold from DCLK	5	–	ns

NOTES:

1) Clock mode 2 selected in HIdden DAC register (D5 = '1').
2) The first low byte of 16-bit data input must be synchronized with BLANK* or the start of the overlay window, whichever is later. The first high byte will be clocked on the next rising edge of DCLK.
3) For CL-GD543X/'4X Overlay modes, BLANK* will be an output.

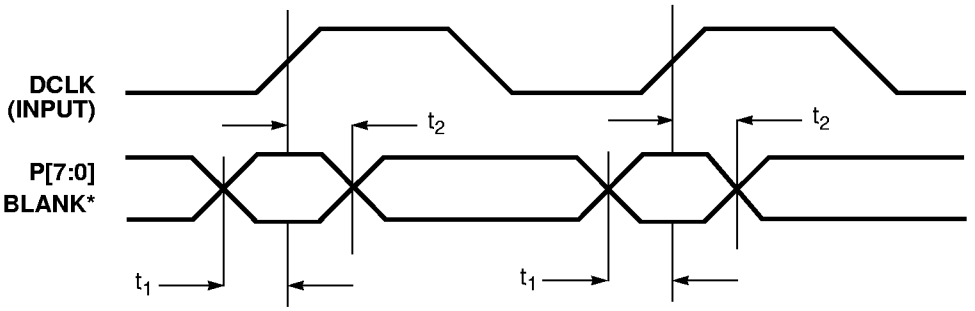


Figure 7-35. P-Bus as Inputs: 16-Bit Mode, Clock Mode 2 (External DCLK)

Table 7-36. P-Bus as Inputs: 16-Bit Mode (DCLK output as reference)

Symbol	Parameter	MIN	Units
t_1	P[7:0] setup to DCLK (rising edge — internal DCLK)	4	ns
t_2	P[7:0] hold from DCLK (rising edge — internal DCLK)	2	ns
t_3	P[7:0] setup to DCLK (falling edge — internal DCLK)	4	ns
t_4	P[7:0] hold from DCLK (rising edge — internal DCLK)	2	ns

NOTE: Clock mode selected in Hidden DAC register (D5 = '0').

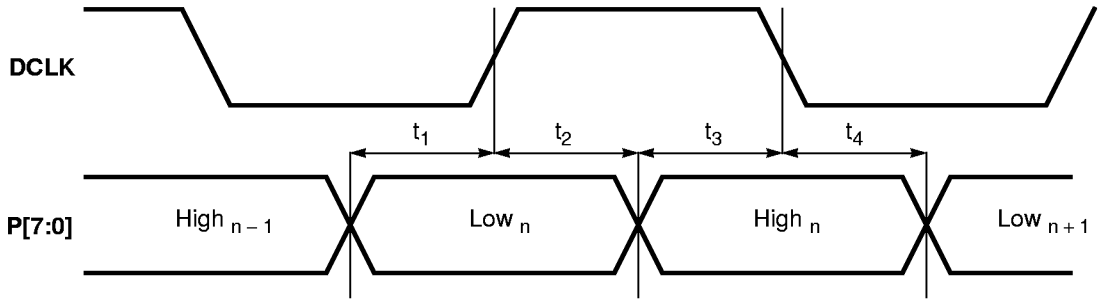


Figure 7-36. P-Bus as Inputs: 16-Bit Mode (External DCLK)

Table 7-37. Video Port Timing (CL-GD5440 only)

Symbol	Parameter	MIN	Units
t_1	Back porch	16	Pixel clocks

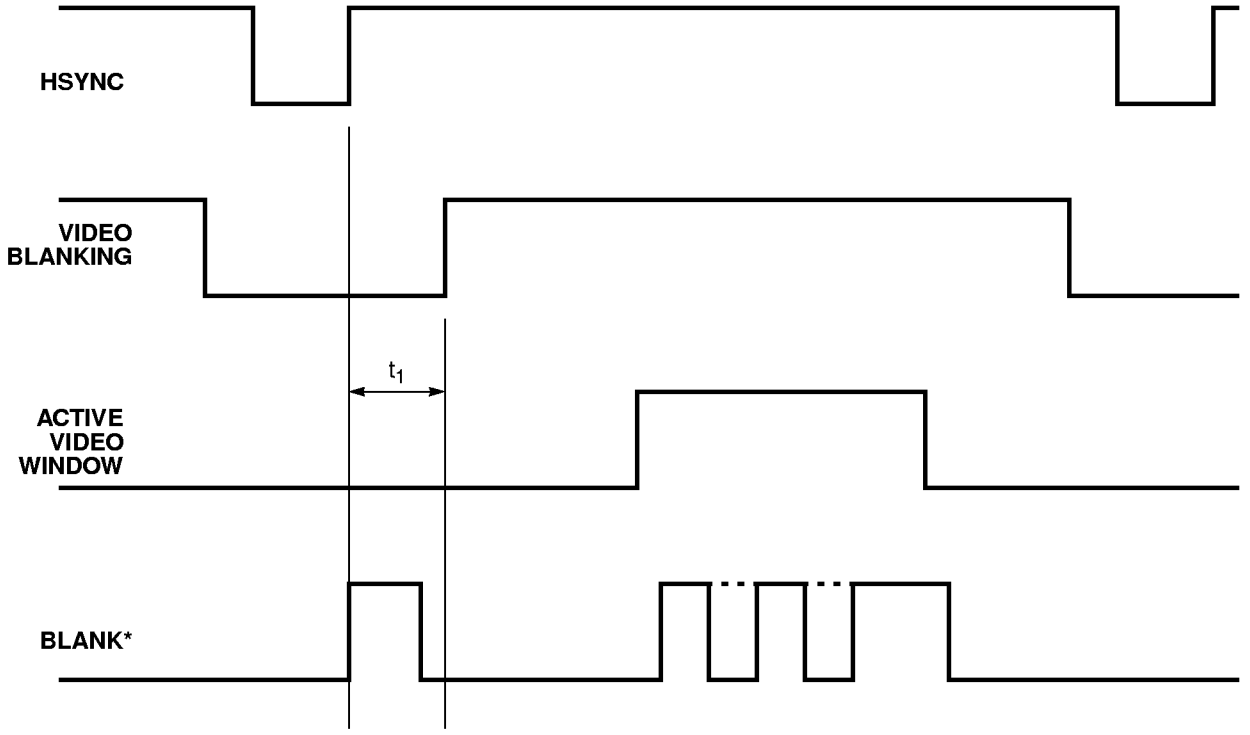


Figure 7-37. Video Port Timing (CL-GD5440 only)

Table 7-38. Video Port Timing: Detail (CL-GD5440 only)

Symbol	Parameter	MIN	MIN	Units
t_1	DCLK period	12	–	ns
t_2	BLANK* delay from DCLK rising edge	–	7	ns
t_3	P[7:0] setup to DCLK rising edge	5	–	ns
t_4	P[7:0] hold from DCLK rising edge	0	–	ns

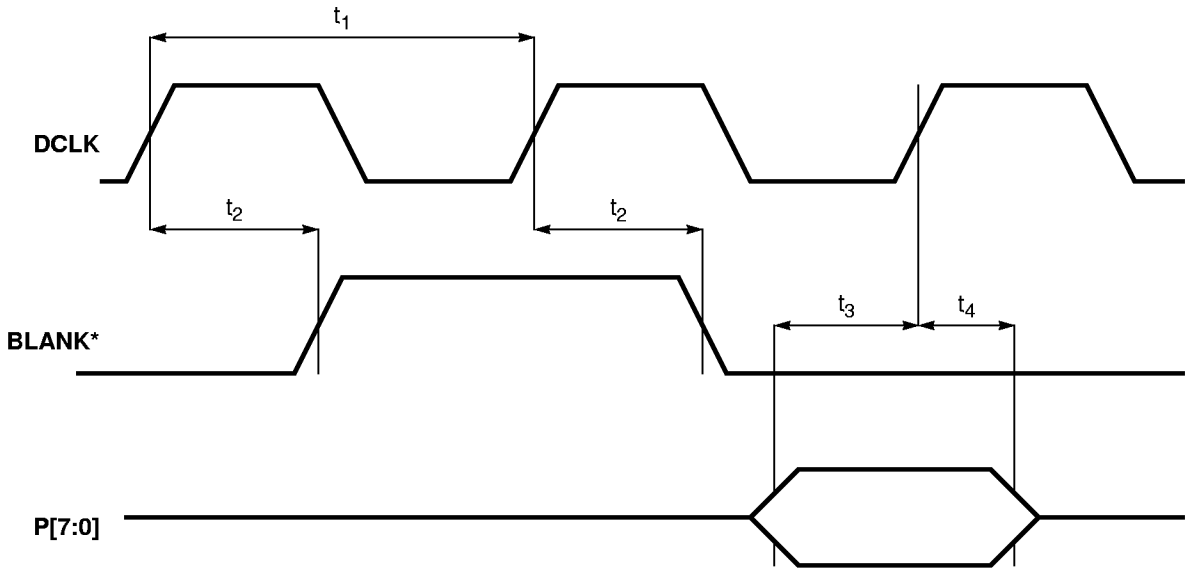


Figure 7-38. Video Port Timing: Detail (CL-GD5440 only)

Table 7-39. DCLK as Input

Symbol	Parameter: CL-GD5434	MIN	MAX	Units
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period	40	60	% of t_5
t_4	Low period	40	60	% of t_5
t_5	Period	17	–	ns
Parameter: CL-GD5430/'40				
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period: Clock mode 1	45	55	% of t_5
t_3	High period: Clock mode 2	30	70	% of t_5
t_4	Low period: Clock mode 1	45	55	% of t_5
t_4	Low period: Clock mode 2	30	70	% of t_5
t_5	Period	12.5	–	ns

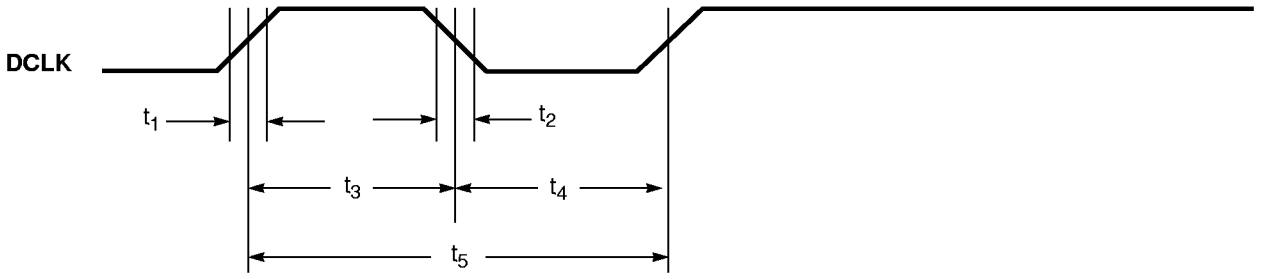


Figure 7-39. DCLK as Input

Table 7-40. RESET Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RST# pulse width	12	–	MCLK
t_2	MD[CONFIG] setup to RST# falling edge	2	–	ns
t_3	MD[CONFIG] hold from RST# falling edge	25	–	ns
t_4	RST# inactive to first command	12	–	MCLK

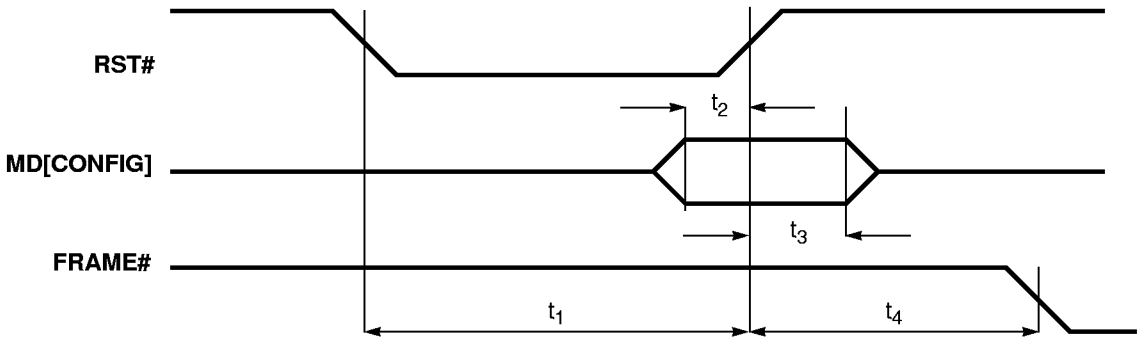
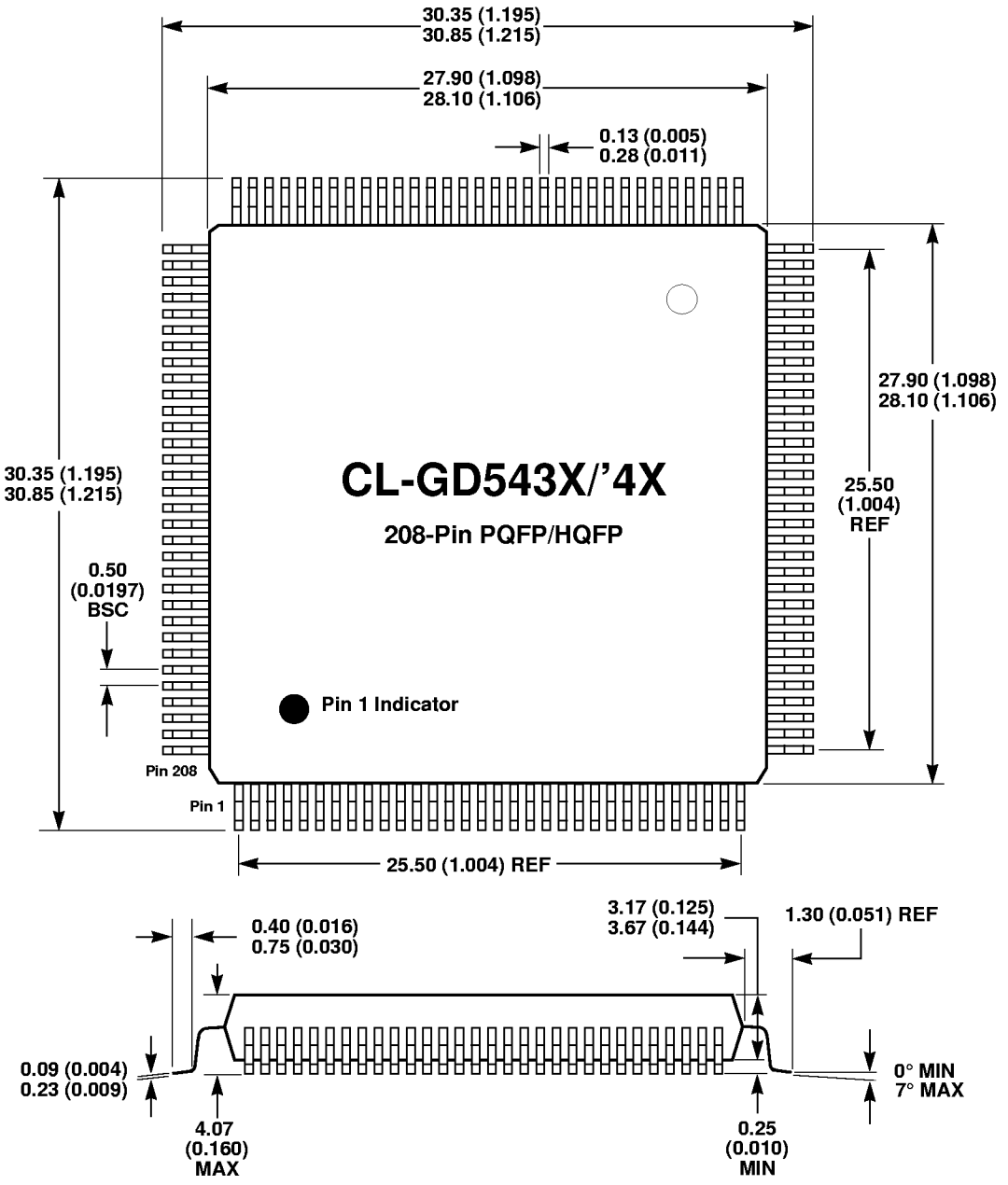


Figure 7-40. RESET Timing

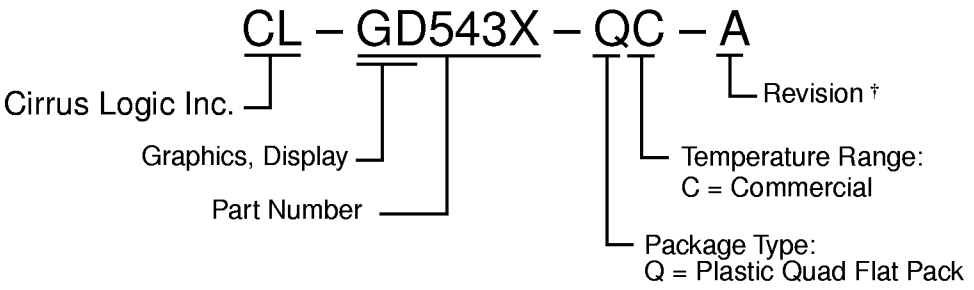
8. PACKAGE SPECIFICATIONS



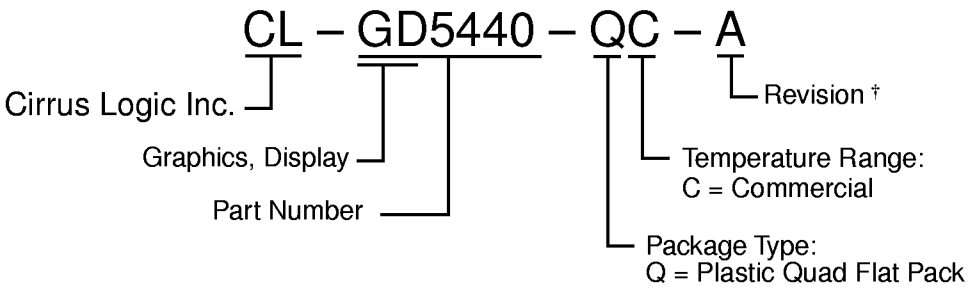
NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) HQFP is a high-performance QFP with an exposed or unexposed heat sink.

9. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic. for up-to-date information on revisions.



† Contact Cirrus Logic for up-to-date information on revisions.