FAIRCHILD

BIPOLAR MICROPROCESSOR DATABOOK

$3.00

MACROLOGIC BIPOLAR MICROPROCESSOR DATABOOK

FAIRCHILD

464 Ellis Street, Mountain View, California 94042

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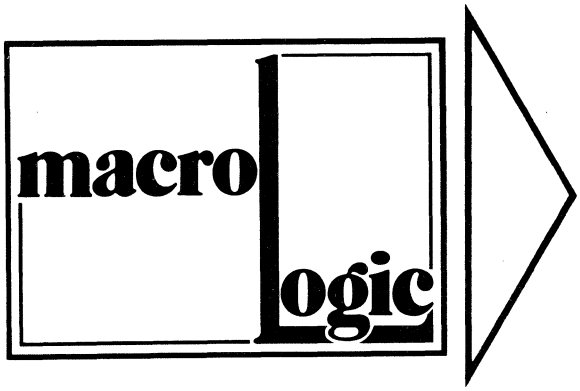


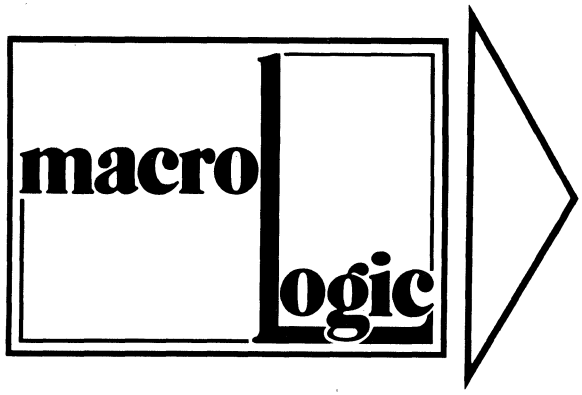
INTRODUCTION

Microprogramming is a practical method for implementing as many system functions as possible in one "centralized" logic block that is controlled by "instructions" stored in a memory. This is accomplished using a mixture of hardware and software techniques. Since designing microprogrammed systems with SSI/MSI is rather difficult and tedious, in the past there has been only limited use of microprogramming except by sophisticated users. Recently, however, the dramatic increase in digital-system complexity has opened up the field of microprogramming and the proliferation of available microprocessors has greatly simplified the designer's task. While focus has been on the MOS microprocessor families, interest is now moving toward the higher speed bipolar bit-slice microprocessors for microprogrammed system design. Where ultra-low power consumption and high noise margin are crucial factors, CMOS bit-slice microprocessors are gaining popularity.

Fairchild Macrologic is an LSI bit-slice family designed for optimum performance, versatility and system-cost effectiveness. The main goal in its development was to provide a set of functional building blocks that the typical design engineer frequently required but formerly had to implement with SSI and MSI. In some cases, this amounted to a straightforward combination of a number of existing MSI onto a single chip; for example, the ALRS – the foundation of the bipolar microprocessor chip set. The ALRS combines ALU, RAM, 3-state registers, and decode logic to form a fast 4-bit CPU. Other functions, however, differed considerably from existing SSI and MSI devices and consequently were difficult and expensive to implement. An example of this is the cyclic redundancy checker – a combination of shift register, ROM and exclusive-OR logic that provides the error-detecting function on one chip.

Once the functions were determined, the most appropriate technology for a particular function was selected. In some cases, low power Schottky was chosen; in some, Isoplanar Integrated Injection Logic (I^3L^{TM}); in others, CMOS or Isoplanar Schottky. Certain functions turned out to be feasible in two or more of these advanced technologies.

This databook is divided into four major sections. The first (Section 2) includes selector information for locating functions and available technologies for a given function. Also, since all Macrologic applications require memory circuits, a list of Fairchild memories is included. Section 3 contains bipolar Macrologic (advanced Schottky TTL and I^3L) data sheets. Section 4 includes the CMOS Macrologic data sheets. To illustrate the versatility of this bit-slice family, the final technical section (Section 5) introduces the reader to a few of the many Macrologic applications. It is important to realize that Macrologic can be used to implement highly sophisitcated microprogrammed digital systems, and the list of applications is virtually endless.



NUMERICAL INDEX OF DEVICES

DEVICE SELECTOR GUIDE BY FUNCTION

FUNCTION	DEVICE NO.	TECHNOLOGY
Address Arithmetic	4707, 9407	CMOS, LS
Arithmetic Logic Unit (ALU)	4705, 9405, 9405A	CMOS, LS
Bit-Rate Generator	4702	CMOS
Byte Masking	4704, 9404	CMOS, LS
Cyclic Redundancy Checks	9401	LS
FIFO, 16 x 4 Expandable	4703, 9403	CMOS, LS
FIFO, 64 x 4 Expandable	9423*	I^3L^{TM}
LIFO Stack	4706, 9406	CMOS, LS
Microprogram Sequencer	4708, 9408	CMOS, I^3L^{TM}
Multiplexing	4704, 9404	CMOS, LS
Program Counter	4706, 9406 4707, 9407	CMOS, LS
Registers, Intelligent	4705, 9405, 9405A 4707, 9407	CMOS, LS
Registers, Not Intelligent	4710, 9410	CMOS, LS
Sign Extension	4704, 9404	CMOS, LS
Stack Pointer	4707, 9407	CMOS, LS

*To be announced

FUNCTIONAL BUILDING BLOCKS BY TECHNOLOGY

	LS	I^3L^{TM}	CMOS
MICROPROCESSOR ELEMENTS	ALU/Register Unit (9404, 9405)	Microprogram Sequencer (9408)	ALU/Register Unit (4704, 4705)
	LIFO Stack (9406)		LIFO Stack (4706)
	Address Arithmetic Unit (9407)		Address Arithmetic Unit (4707)
	Compatible Scratchpad Memory (9410)		Compatible Scratchpad Memory (4710)
			Microprogram Sequencer (4708)
PERIPHERAL ELEMENTS	16 x 4 FIFO (9403)	64 x 4 FIFO*	Bit-Rate Generator (4702)
	CRC Generator/ Checker (9401)	CRT Controller*	16 x 4 FIFO (4703)

*To be announced

MEMORY PRODUCTS SELECTOR GUIDE

The following selector guide lists Fairchild memory products which will be useful when designing with Fairchild Macrologic. Device specifications for Fairchild memory products are available either as separate data sheets or within their respective technology data books – Bipolar Memory Data Book and MOS/CCD Data Book.

STATIC RAMS

TECHNOLOGY	DEVICE NO.	ORGANIZATION	ACCESS TIME t_{AA} MAX (TYP) ns	POWER DISSIPATION P_D MAX (TYP) mW	NO. OF PINS
CMOS	4720	256 x 1	100		16
CMOS	4721* **	256 x 4	(450)		22
CMOS	4736* **	1024 x 1	(500)		16
ECL	10145A	16 x 4	9.0	(500)	16
ECL	10405	128 x 1	15	(470)	16
ECL	10410	256 x 1	30	(475)	16
ECL	10411	256 x 1	35	(360)	16
ECL	10415	1024 x 1	60	(475)	16
ECL	10415A	1024 x 1	35	(475)	16
ECL	100415	1024 x 1	(20)	(500)	24
MOS	2102	1024 x 1	1000	160	16
MOS	2102-1	1024 x 1	450	160	16
MOS	2102-2	1024 x 1	650	160	16
MOS	2102F	1024 x 1	350	160	16
MOS	2102F2	1024 x 1	250	110	16
MOS	2102LF	1024 x 1	350	110	16
MOS	2102LF2	1024 x 1	250	110	16
MOS	2102L1	1024 x 1	450	110	16
MOS	2102L2	1024 x 1	650	110	16
MOS	3539	256 x 8	650	275	22
MOS	3539-1	256 x 8	400	275	22
MOS	3539-2	256 x 8	500	275	22
MOS	3542	1024 x 1	150	200	16
MOS	3542-2	1024 x 1	120	200	16
MOS	3544**	1024 x 4	250	450	18
TTL	93419	64 x 9	40	(725)	28
TTL	93410	256 x 1	60	(450)	16
TTL	93410A	256 x 1	45	(450)	16
TTL	93411	256 x 1	55	(475)	16
TTL	93411A	256 x 1	45	(475)	16
TTL	93L420	256 x 1	45	(275)	16
TTL	93421	256 x 1	50	(475)	16
TTL	93421A	256 x 1	40	(475)	16
TTL	93L421	256 x 1	90	(275)	16
TTL	93L412	256 x 4	70	(250)	22,24
TTL	93L422	256 x 4	70	(250)	22,24
TTL	93415	1024 x 1	70	(475)	16
TTL	93415A	1024 x 1	45	(475)	16
TTL	93L415	1024 x 1	95	(200)	16
TTL	93425	1024 x 1	70	(475)	16
TTL	93425A	1024 x 1	45	(475)	16
TTL	93L425	1024 x 1	95	(200)	16
TTL	93470**	4096 x 1		(950)	18
TTL	93471**	4096 x 1		(950)	18

*5.0 V V_{DD} **Available 4th quarter 1976

MEMORY PRODUCTS SELECTOR GUIDE (Cont'd)

DYNAMIC RAMS

TECHNOLOGY	DEVICE NO.	ORGANIZATION	ACCESS TIME t_{AA} MAX (TYP) ns	POWER DISSIPATION P_D MAX (TYP) mW	NO. OF PINS
I^3L	93481	4096 x 1	(90)	(400)	16
MOS	4096-2	4096 x 1	200	350	16
MOS	4096-3	4096 x 1	250	300	16
MOS	4096-4	4096 x 1	300	250	16
MOS	4096-5	4096 x 1	350	250	16
MOS	4027-3**	4096 x 1	200	450	16
MOS	4027-4**	4096 x 1	250	450	16
MOS	F16K**	16,384 x 1	200	600	16

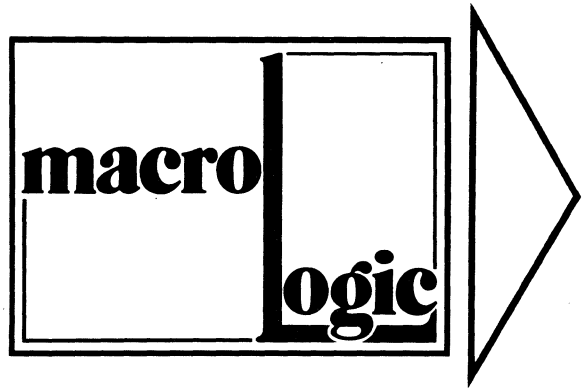
ROMS

TECHNOLOGY	DEVICE NO.	ORGANIZATION	ACCESS TIME t_{AA} MAX (TYP) ns	POWER DISSIPATION P_D MAX (TYP) mW	NO. OF PINS
CMOS	4735* **	256 x 8	(250)		24
MOS	3515	512 x 8	600		24
TTL	93457	256 x 4	45	(425)	16
TTL	93467	256 x 4	45	(425)	16
TTL	93431	512 x 4	50	(475)	16
TTL	93441	512 x 4	50	(475)	16
TTL	93432	512 x 8	55	(650)	24
TTL	93442	512 x 8	55	(650)	24
TTL	93454	1024 x 8	45	(550)	24
TTL	93464	1024 x 8	45	(550)	24

PROMS

TECHNOLOGY	DEVICE NO.	ORGANIZATION	ACCESS TIME t_{AA} MAX (TYP) ns	POWER DISSIPATION P_D MAX (TYP) mW	NO. OF PINS
ECL	10416**	256 x 4	(15)	(500)	16
TTL	93417	256 x 4	45	(425)	16
TTL	93427	256 x 4	45	(425)	16
TTL	93436	512 x 4	50	(475)	16
TTL	93446	512 x 4	50	(475)	16
TTL	93438	512 x 8	55	(650)	24
TTL	93448	512 x 8	55	(650)	24
TTL	93452**	1024 x 4	(35)	(650)	18
TTL	93453**	1024 x 4	(35)	(650)	18

*5.0 V V_{DD}
**Available 4th quarter 1976



9400
BIPOLAR MACROLOGIC SERIES

GENERAL DESCRIPTION

Fairchild 9400 Macrologic Series utilizes advanced Schottky and I^3L^{TM} technology to provide high performance peripheral and processor oriented LSI. The design of 9400 ensures maximum design flexibility with no performance loss. The Bipolar Macrologic elements may be used with any bit length, instruction set or organization. Devices may be expanded with little or no extra components. Where applicable, bus oriented, 3-state outputs are provided. A new, slim 24-pin package reduces PC board real estate by a third.

- **150–180 GATE COMPLEXITY**
- **COMPATIBLE WITH ALL TTL FAMILIES**
- **PERFORMANCE EQUIVALENT TO SCHOTTKY IMPLEMENTATION**
- **14, 18, SLIM 24 AND 40-PIN PACKAGES**
- **INPUTS ABOUT 1/4 NORMAL TTL LOAD, i.e., 360–400 μA**
- **OUTPUTS DRIVE 16 mA (10 U.L.) OR 8 mA (5 U.L.) DEPENDING ON APPLICATION**
- **DESIGNED FOR MAXIMUM FLEXIBILITY**
- **OPERATES OVER COMMERCIAL OR MILITARY TEMPERATURE RANGE**

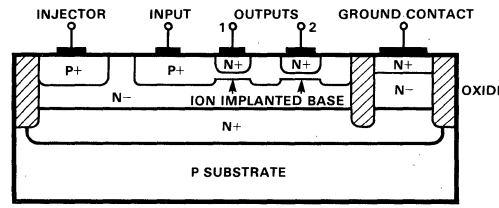
I^3L TECHNOLOGY

I^3L^{TM} (Isoplanar Integrated Injection Logic) combines the low power and high packing density advantages of I^2L (Integrated Injection Logic) with the high speed and high packing density advantages of Fairchild's Isoplanar technology. The result is a process which offers low power (160 μW per gate), high speed (4 ns per gate) and extremely high packing density. I^3L is used whenever high speed is required, but high complexity makes low power Schottky processing undesirable from a cost standpoint.

When designing with I^3L Macrologic devices, TTL interface is not a problem as I^3L Macrologic has standard on-chip TTL inputs and outputs. An I^3L current source also is contained on-chip, therefore only a single 5 V power supply is required and the chip appears to be TTL to the user. However, because internal logic is implemented with I^3L, the chip is smaller, uses less power and is less expensive than a TTL equivalent.

3

I^3L CROSS SECTION



DESIGN CONSIDERATIONS

TTL Macrologic has been designed so that its input and output levels and thresholds are equivalent to standard TTL when fan-out is no greater than 10. Therefore, the design considerations delineated on the following pages apply to Macrologic as well as any other TTL.

Supply Voltage and Temperature Range

The nominal supply voltage (V_{CC}) for all TTL, including 9400 Macrologic, is +5.0 V. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250 mV) over an ambient temperature range of 0°C to +75°C. MIL-grade parts are guaranteed to perform with a ±10% supply tolerance (±500 mV) over an ambient temperature range of −55°C to +125°C.

TTL families may be mixed for optimum system design. The following tables specify the worst case noise immunity in mixed systems.

Worst Case TTL DC Noise Immunity / Noise Margins

Electrical Characteristics

Symbol	Fairchild TTL Families	Military (−55 to +125°C)				Commercial (0 to 75°C)				Units
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{OL}	V_{OH}	
TTL	Standard TTL 9000, 9N (54/74)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
HTTL	High Speed TTL 9H (54H/74H)	0.8	2.0	0.4	2.4	0.8	2.0	0.4	2.4	V
LPTTL	Low Power TTL, 93L00 (MSI)	0.7	2.0	0.3	2.4	0.8	2.0	0.3	2.4	V
STTL	Schottky TTL 9S (54S/74S), 93S00	0.8	2.0	0.5	2.5	0.8	2.0	0.5	2.7	V
LSTTL	Low Power Schottky TTL 9LS (54LS/74LS)	0.7	2.0	0.4	2.5	0.8	2.0	0.5	2.7	V

V_{OL} and V_{OH} are the voltages generated at the output. V_{IL} and V_{IH} are the voltage required at the input to generate the appropriate output levels. The numbers given above are guaranteed worst-case values.

LOW Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	300	400	300	mV
HTTL	400	400	300	400	300	mV
LPTTL	500	500	400	500	400	mV
STTL	300	300	200	300	200	mV
LSTTL	400	400	300	400	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Military)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	500	500	500	500	500	mV
LSTTL	500	500	500	500	500	mV

From "V_{OH}" to "V_{IH}"

LOW Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	500	500	500	500	500	mV
STTL	300	300	300	300	300	mV
LSTTL	300	300	300	300	300	mV

From "V_{OL}" to "V_{IL}"

HIGH Level Noise Margins (Commercial)

From \ To	TTL	HTTL	LPTTL	STTL	LSTTL	Units
TTL	400	400	400	400	400	mV
HTTL	400	400	400	400	400	mV
LPTTL	400	400	400	400	400	mV
STTL	700	700	700	700	700	mV
LSTTL	700	700	700	700	700	mV

From "V_{OH}" to "V_{IH}"

Fan-in and Fan-out

In order to simplify designing with Fairchild TTL devices, the input and output loading parameters of all families are normalized to the values shown at the right.

Input loading and output drive factors of all products described in this handbook are related to these definitions.

1 TTL Unit Load (U.L.) = 40 μA
in the HIGH state (logic "1")

1 TTL Unit Load (U.L.) = 1.6 mA
in the LOW state (logic "0")

Examples - Input Load

1. A 9N00/7400 gate, which has a maximum I_{IL} of 1.6 mA and I_{IH} of 40 μA is specified as having an input load factor of 1 U.L. (Also called a fan-in of 1 load.)

2. The 9LS95 which has a value of I_{IL} = 0.8 mA and I_{IH} of 40 μA on the CP terminal, is specified as having an input LOW load factor of

$$\frac{0.8\ mA}{1.6\ mA} \text{ or } 0.5\ U.L.$$

and an input HIGH load factor of

$$\frac{40\ \mu A}{40\ \mu A} \text{ or } 1\ U.L.$$

3. The 9LS00 gate which has an I_{IL} of 0.36 mA and an I_{IH} of 20 μA, has an input LOW load factor of

$$\frac{0.36\ mA}{1.6\ mA} \text{ or } 0.225\ U.L.$$

(normally rounded to 0.25 U.L.) and an input HIGH load factor of

$$\frac{20\ \mu A}{40\ \mu A} \text{ or } 0.5\ U.L.$$

Examples - Output Drive

1. The output of the 9N00/7400 will sink 16 mA in the LOW (logic "0") state and source 800 μA in the HIGH (logic "1") state. The normalized output LOW drive factor is therefore

$$\frac{16\ mA}{1.6\ mA} = 10\ U.L.$$

and the output HIGH drive factor is

$$\frac{800\ \mu A}{40\ \mu A} \text{ or } 20\ U.L.$$

2. The output of the 9LS00XC (Commercial Grade) will sink 8.0 mA in the LOW state and source 400 μA in the HIGH state. The normalized output LOW drive factor is

$$\frac{8.0\ mA}{1.6\ mA} \text{ or } 5\ U.L.$$

and the output HIGH drive factor is

$$\frac{400\ \mu A}{40\ \mu A} \text{ or } 10\ U.L.$$

Relative load and drive factors for the basic TTL families are given in *Table I*.

TABLE I

FAMILY	INPUT LOAD		OUTPUT DRIVE	
	HIGH	LOW	HIGH	LOW
9LS00	0.5 U.L.	0.25 U.L.	10 U.L.	5 U.L.
9N00/7400	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9000	1 U.L.	1 U.L.	20 U.L.	10 U.L.
9H00/74H00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.
9S00/74S00	1.25 U.L.	1.25 U.L.	25 U.L.	12.5 U.L.

Values for MSI devices vary significantly from one element to another. Consult the appropriate data sheet for actual characteristics.

Wired-OR Applications

Certain TTL devices are provided with an "open" collector output to permit the Wired-OR (actually Wired-AND) function. This is achieved by connecting open collector outputs together and adding an external pull-up resistor.

The value of the pull-up resistor is determined by considering the fan-out of the OR tie and the number of devices in the OR tie. The pull-up resistor value is chosen from a range between a maximum value (established to maintain the required V_{OH} with all the OR tied outputs HIGH) and a minimum value (established so that the OR tie fan-out is not exceeded when only one output is LOW).

Minimum and Maximum Pull-Up Resistor Values

$$R_{X(MIN)} = \frac{V_{CC(MAX)} - V_{OL}}{I_{OL} - N_2(LOW) \bullet 1.6\ mA}$$

$$R_{X(MAX)} = \frac{V_{CC(MIN)} - V_{OH}}{N_1 \bullet I_{OH} + N_2(HIGH) \bullet 40\ \mu A}$$

where:

R_X = External Pull-up Resistor
N_1 = Number of Wired-OR Outputs
N_2 = Number of Input Unit Loads being Driven
$I_{OH} = I_{CEX}$ = Output HIGH Leakage Current
I_{OL} = LOW Level Fan-out Current of Driving Element
V_{OL} = Output LOW Voltage Level (0.5 V)
V_{OH} = Output HIGH Voltage Level (2.4 V)
V_{CC} = Power Supply Voltage

Example: Four 9LS03 gate outputs driving four other 9LS gates or MSI inputs.

$$R_{X(MIN)} = \frac{5.25\ V - 0.5\ V}{8\ mA - 1.6\ mA} = \frac{4.75\ V}{6.4\ mA} = 742\ \Omega$$

$$R_{X(MAX)} = \frac{4.75\ V - 2.4\ V}{4 \bullet 100\ \mu A + 2 \bullet 40\ \mu A} = \frac{2.35\ V}{0.48\ mA} = 4.9\ k\Omega$$

where:

N_1 = 4
$N_2(HIGH)$ = 4 • 0.5 U.L. = 2 U.L.
$N_2(LOW)$ = 4 • 0.25 U.L. = 1 U.L.
I_{OH} = 100 μA
I_{OL} = 8 mA
V_{OL} = 0.5 V
V_{OH} = 2.4 V

Any value of pull-up resistor between 742 Ω and 4.9 kΩ can be used. The lower values yield the fastest speeds; the higher values yield the lowest power dissipation.

Unused Inputs

For best noise immunity and switching speed, unused TTL inputs should not be left floating. These inputs should be held between 2.4 V and the absolute maximum input voltage.

Two possible ways of handling unused inputs are:

1. Connect unused input to V_{CC}. Most 9LS inputs have a breakdown voltage > 15 V and require, therefore, no series resistor. For all multi-emitter conventional TTL inputs, a 1 to 10 kΩ current limiting series resistor is recommended, to protect against V_{CC} transients that exceed 5.5 V.

2. Connect the unused input to the output of un unused gate that is forced HIGH.

CAUTION: Do not connect an unused LSTTL input to another input of the same NAND or AND function. This method, recommended for normal TTL, increases the input coupling capacitance and thus reduces the ac noise immunity.

Interconnection Delays

For those parts of a system in which timing is critical, designers should take into account the finite delay along the interconnections. This delay ranges from about 0.12 to 0.15 ns/inch for the type of interconnections normally used in TTL systems. Exceptions occur in systems using ground planes with STTL to reduce ground noise during a logic transition; ground planes give higher distributed capacitance and delays of about 0.15 to 0.22 ns/inch.

Most interconnections on a logic board are short enough that the wiring and load capacitance can be treated as a lumped capacitance for purposes of estimating their effect on the propagation delay of the driving circuit. When an interconnection is long enough that its delay is one-fourth to one-half of the signal transition time, the driver output waveform exhibits noticeable slope changes during a transition. This is evidence that during the initial portion of the output voltage transition the driver sees the characteristic impedance of the interconnection (normally 150 Ω to 200 Ω), which for transient conditions appears as a resistor returned to the quiescent voltage existing just before the beginning of the transition. This characteristic impedance forms a voltage divider with the driver output impedance, tending to produce a signal transition having the same rise or fall time as in the no-load condition but with a reduced amplitude. This attenuated signal travels to the far end of the interconnection, which is essentially an unterminated transmission line, whereupon the signal starts doubling. Simultaneously, a reflection voltage is generated which has the same amplitude and polarity as the original signal, *e.g.,* if the driver output signal is positive-going the reflection will be positive-going, and as it travels back toward the driver it adds to the line voltage. At the instant the reflection arrives at the driver it adds algebraically to the still-rising driver output, accelerating the transition rate and producing the noticeable change in slope.

If an interconnection is of such length that its delay is longer than half the signal transition time, the attenuated output of the driver has time to reach substantial completion before the reflection arrives. In the limit, the waveform observed at the driver output is a 2-step signal with a pedestal. In this circumstance the first load circuit to receive a full signal is the one at the far end, because of the doubling effect, while the last one to receive a full signal is the one nearest the driver since it must wait for the reflection to complete the transition. Thus, in a worst-cast situation, the net contribution to the overall delay is twice the delay of the interconnection because the initial part of the signal must travel to the far end of the line and the reflection must return.

When load circuits are distributed along an interconnection, the input capacitance of each will cause a small reflection having a polarity opposite that of the signal transition, and each capacitance also slows the transition rate of the signal as it passes by. The series of small reflections, arriving back at the driver, is subtractive and has the effect of reducing the apparent amplitude of the signal. The successive slowing of the transition rate of the transmitted signal means that it takes longer for the signal to rise or fall to the threshold level of any particular load circuit. A rough but workable approach is to treat the load capacitances as an increase in the intrinsic distributed capacitance of the interconnection. Increasing the distributed capacitance of a transmission line reduces its impedance and increases its delay. A good approximation for ordinary TTL interconnections is that distributed load capacitance decreases the characteristic impedance by about one-third and increases the delay by one-half.

Another advantage of LSTTL has to do with its output impedance during a positive-going transition. Whereas the low output impedance of STTL and HTTL allows these circuits to force a larger initial swing into a low impedance interconnection, the low output impedance also has a disadvantage. It makes the reflection coefficient negative at the driven end of the interconnection, a circumstance that exists any time a transmission line is terminated by an impedance lower than its characteristic impedance. This means that when the reflection from the (essentially) open end of the interconnection arrives back at the driver it will be re-reflected with the opposite polarity. The result is a sequence of reflected signals which alternate in sign and decrease in magnitude, commonly known as ringing. The lower the driver output impedance, the greater the amplitude of the ringing and the longer it takes to damp out.

The output impedance of LSTTL, on the other hand, is closer to the characteristic impedance of the interconnections commonly used with TTL, and ringing is practically non-existent. Thus no special packaging is required. This advantage, combined with excellent speed, modest edge rates and very low transient currents, are some of the reasons that designers have found LSTTL extremely easy to work with and very cost effective.

DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA BOOK

CURRENTS – Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current** – The current flowing into the V_{CC} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst case operation.

I_{IH} **Input HIGH current** – The current flowing into an input when a specified HIGH voltage is applied.

I_{IL} **Input LOW current** – The current flowing out of an input when a specified LOW voltage is applied.

I_{OH} **Output HIGH current** – The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.

I_{OL} **Output LOW current** – The current flowing into an output which is in the LOW state.

I_{OS} **Output short circuit current** – The current flowing out of an output which is in the HIGH state when that output is short circuited to ground (or other specified potential).

I_{OZH} **Output off HIGH current** – The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.

I_{OZL} **Output off LOW current** – The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

VOLTAGES – All voltages are referenced to ground. Negative voltage limits are specified as absolute values (*i.e.*, −10 V is greater than −1.0 V).

V_{CC} **Supply voltage** – The range of power supply voltage over which the device is guaranteed to operate within the specified limits.

$V_{CD(MAX)}$ **Input clamp diode voltage** – The most negative voltage at an input when 18 mA is forced out of that input terminal. This parameter guarantees the integrity of the input diode which is intended to clamp negative ringing at the input terminal.

V_{IH} **Input HIGH voltage** – The range of input voltages that represents a logic HIGH in the system.

$V_{IH(MIN)}$ **Minimum input HIGH voltage** – The minimum allowed input HIGH in a logic system. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} **Input LOW voltage** – The range of input voltages that represents a logic LOW in the system.

$V_{IL(MAX)}$ **Maximum input LOW voltage** – The maximum allowed input LOW in a system. This value represents the guaranteed input LOW threshold for the device.

$V_{OH(MIN)}$ **Output HIGH voltage** – The minimum voltage at an output terminal for the specified output current I_{OH} and at the minimum value of V_{CC}.

$V_{OL(MAX)}$ **Output LOW voltage** – The maximum voltage at an output terminal sinking the maximum specified load current I_{OL}.

V_{T+} **Positive-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IH} as the input transition rises from below $V_{T-(MIN)}$.

V_{T-} **Negative-going threshold voltage** – The input voltage of a variable threshold device (*i.e.,* Schmitt Trigger) that is interpreted as a V_{IL} as the input transition falls from above $V_{T+(MAX)}$.

AC SWITCHING PARAMETERS

f_{MAX} **Toggle frequency/operating frequency** – The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} **Propagation delay time** – The time between the specified reference points, normally 1.3 V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_W **Pulse width** – The time between 1.3 V amplitude points on the leading and trailing edges of a pulse.

t_h **Hold time** – The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s **Set-up time** – The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} **Output disable time (of a 3-state output) from HIGH level** – The time between the 1.3 V level on the input and a voltage 0.5 V below the steady state output HIGH level with the 3-state output changing from the defined HIGH level to a high-impedance (off) state.

t_{PLZ} **Output disable time (of a 3-state output) from LOW level** – The time between the 1.3 V level on the input and a voltage 0.5 V above the steady state output LOW level with the 3-state output changing from the defined LOW level to a high-impedance (off) state.

t_{PZH} **Output enable time (of a 3-state output) to a HIGH level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a HIGH level.

t_{PZL} **Output enable time (of a 3-state output) to a LOW level** – The time between the 1.3 V levels of the input and output voltage waveforms with the 3-state output changing from a high-impedance (off) state to a LOW level.

t_{rec} **Recovery time** – The time between the 1.3 V level on the trailing edge of an asynchronous input control pulse and the 1.3 V level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

9401

CRC GENERATOR/CHECKER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disc and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is fully compatible with all TTL families.

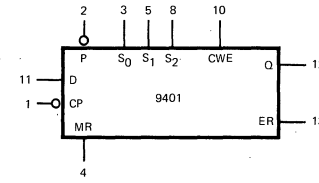
- **GUARANTEED 10 MHz DATA RATE**
- **EIGHT SELECTABLE POLYNOMIALS**
- **ERROR INDICATOR**
- **SEPARATE PRESET AND CLEAR CONTROLS**
- **AUTOMATIC RIGHT JUSTIFICATION**
- **FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES**
- **14-PIN PACKAGE**
- **TYPICAL APPLICATIONS:**
  - **FLOPPY AND OTHER DISC STORAGE SYSTEMS**
  - **DIGITAL CASSETTE AND CARTRIDGE SYSTEMS**
  - **DATA COMMUNICATION SYSTEMS**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	1.0 U.L.	0.23 U.L.
D	Data Input	1.0 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH-to-LOW Transition) Input	1.0 U.L.	0.23 U.L.
CWE	Check Word Enable Input	1.0 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	1.0 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	1.0 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

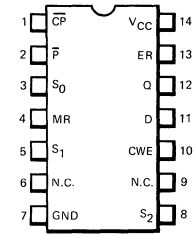
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

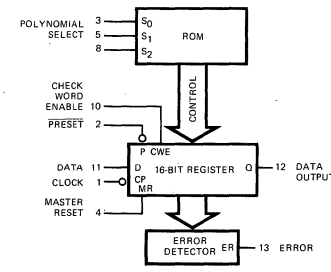
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

3

FUNCTIONAL DESCRIPTION – The 9401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in *Table 1* by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates *(Figure 1).* The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating *(Figure 2).*

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

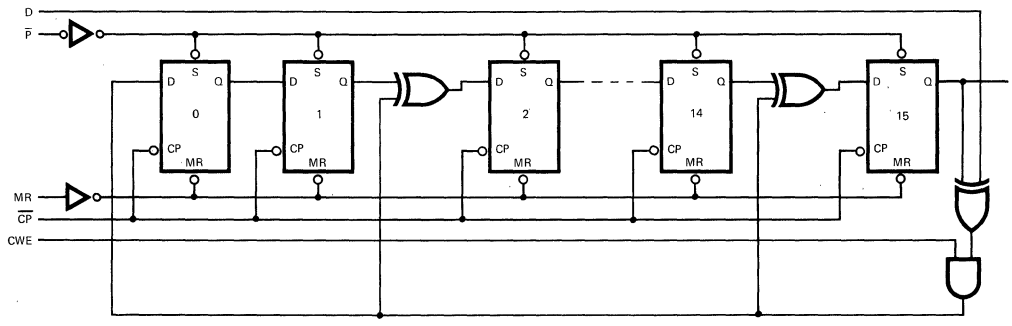


Fig. 1
EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage	XM & XC		0.35	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.45	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current			−0.22	−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			70	110	mA	V_{CC} = MAX, Inputs Open

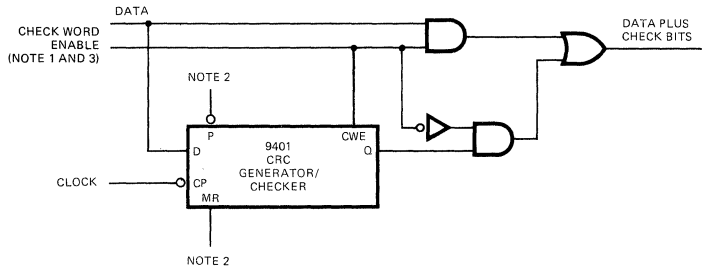
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 2)	LIMITS MAX	UNITS	CONDITIONS	
f_{max}	Maximum Clock Frequency	10	18		MHz	Fig. 3, 4, 5	C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR to Data Output		30	55	ns		
t_{PHL} t_{PLH}	Propagation Delay, Preset to Data Output		40	60	ns		
t_{PHL} t_{PLH}	Propagation Delay, Clock, MR or Preset to Error Output		40	60	ns		

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS	
$t_w\overline{CP}$ (L)	Clock Pulse Width (LOW)	35			ns	Fig. 2	C_L = 15 pF
t_sD	Set-up Time, Data to Clock	55	35		ns	Fig. 6	
t_sCWE	Set-up Time, CWE to Clock	55	35		ns		
t_h	Hold Time, Data and CWE to Clock	0	−10		ns		
t_wP (L)	Preset Pulse Width (LOW)	40	30		ns	Fig. 4	
t_wMR (H)	Master Reset Pulse Width (HIGH)	35	25		ns	Fig. 6	
t_{rec}	Recovery Time, MR and Preset to Clock	50	25		ns	Fig. 4, 5	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.



NOTES:
1. Check word Enable is HIGH while data is being clocked, LOW during transmission of check bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Fig. 2
CHECK WORD GENERATION

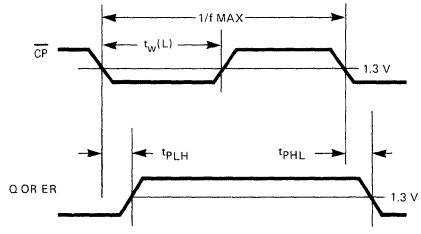


Fig. 3
PROPROPAGATION DELAYS, $\overline{CP}$ TO Q AND $\overline{CP}$ TO ER

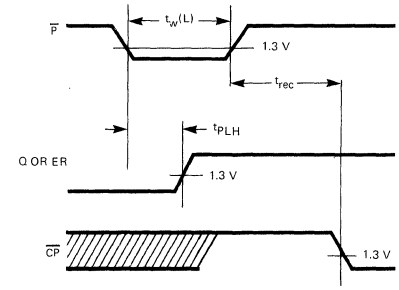


Fig. 4
PROPAGATION DELAYS, $\overline{P}$ TO Q AND ER PLUS RECOVERY TIME $\overline{P}$ TO $\overline{CP}$

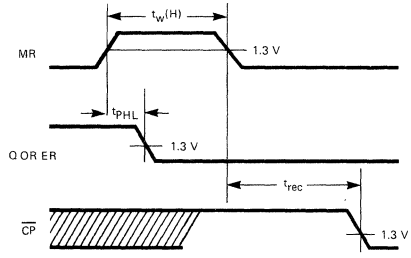


Fig. 5
PROPAGATION DELAYS, MR TO Q AND ER PLUS RECOVERY TIME, MR TO $\overline{CP}$

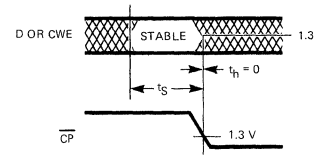


Fig. 6
SET-UP AND HOLD TIMES, D TO $\overline{CP}$ AND CWE TO $\overline{CP}$

9403

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

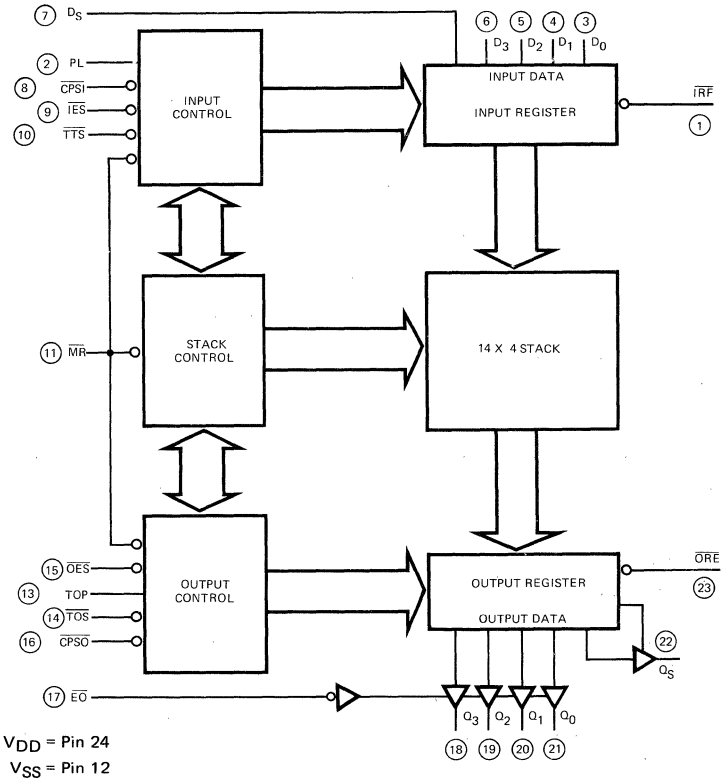
FAIRCHILD TTL MACROLOGIC

DESCRIPTION - The 9403 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

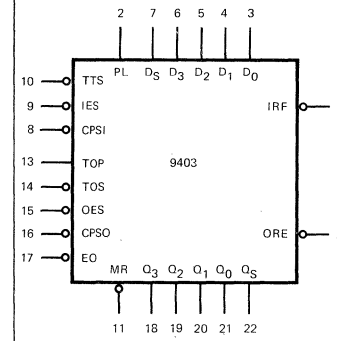
- **10 MHz SERIAL OR PARALLEL DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL TTL FAMILIES**
- **SLIM 24-PIN PACKAGE**

BLOCK DIAGRAM



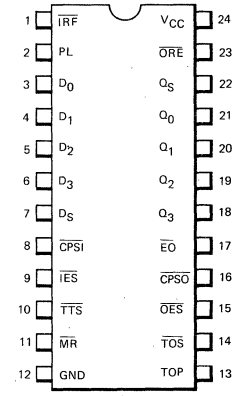
V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

PIN NAMES

PIN NAME	DESCRIPTION	LOADING (Note a)		COMMENTS
		HIGH	LOW	
$D_0 - D_3$	Parallel Data Inputs	1.0 U.L.	0.23 U.L.	
D_S	Serial Data Input	1.0 U.L.	0.23 U.L.	
PL	Parallel Load Input	1.0 U.L.	0.23 U.L.	HIGH on PL enables $D_0 - D_3$. Not edge triggered. Ones catching.
$\overline{CPSI}$	Serial Input Clock	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$\overline{IES}$	Serial Input Enable	1.0 U.L.	0.23 U.L.	Enables serial and parallel input when LOW.
$\overline{TTS}$	Transfer to Stack Input	1.0 U.L.	0.23 U.L.	A LOW on this pin initiates fall through.
$\overline{OES}$	Serial Output Enable Input	1.0 U.L.	0.6 U.L.	Enables serial and parallel output when LOW.
$\overline{TOS}$	Transfer Out Serial Input	1.0 U.L.	0.23 U.L.	A LOW on this pin enables a word to be transferred from the stack to the output register. (TOP must be HIGH also for the transfer to occur). Not edge triggered.
TOP	Transfer Out Parallel Input	1.0 U.L.	0.23 U.L.	A HIGH on this pin enables a word to be transferred from the stack to the output register. ($\overline{TOS}$ must be LOW for the transfer to occur). Not edge triggered.
$\overline{MR}$	Master Reset	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{EO}$	Output Enable	1.0 U.L.	0.23 U.L.	Active LOW.
$\overline{CPSO}$	Serial Output Clock Input	1.0 U.L.	0.23 U.L.	Edge triggered. Activates on falling edge.
$Q_0 - Q_3$	Parallel Data Outputs	130 U.L.	10 U.L.	(Note b)
Q_S	Serial Data Output	10 U.L.	10 U.L.	(Note b)
$\overline{IRF}$	Input Register Full Output	10 U.L.	5 U.L.	LOW when input register is full (Note b).
$\overline{ORE}$	Output Register Empty Output	10 U.L.	5 U.L.	HIGH when output register contains valid data.

NOTE: a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V.

FUNCTIONAL DESCRIPTION – As shown in the block diagram the 9403 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.
Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the D_0 - D_3 inputs into the F_0 - F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

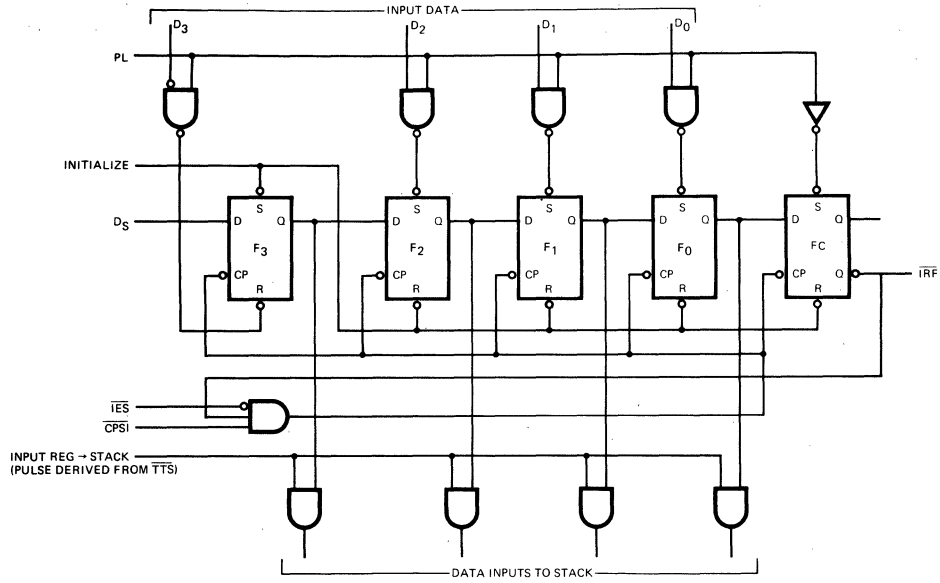


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry – Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0 – F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack –The outputs of Flip-Flops F_0 – F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

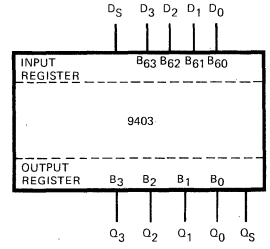


Fig. 2
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

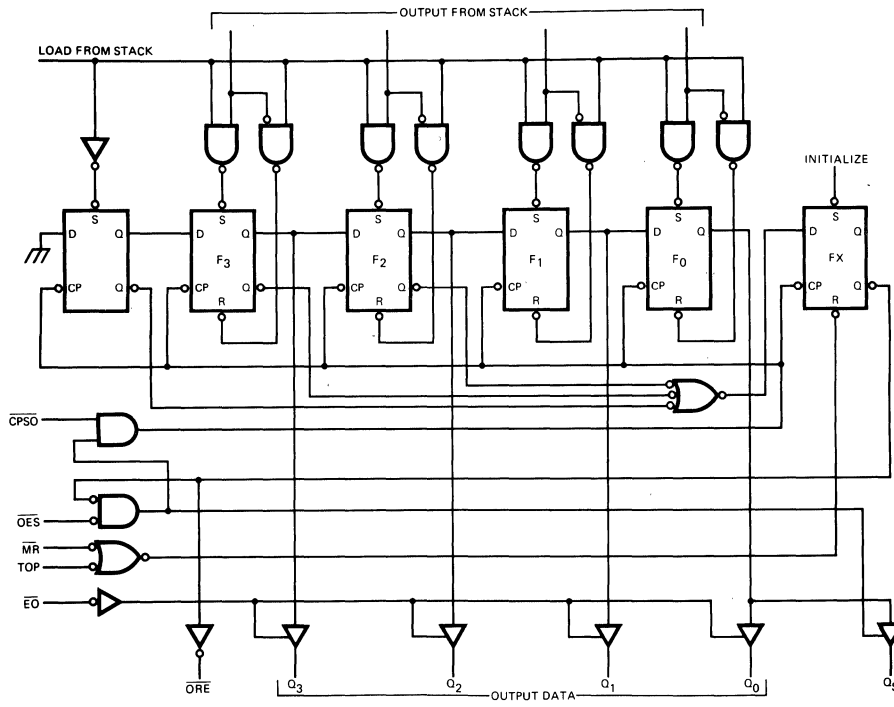


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. $\overline{TOS}$ should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, ORE remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

EXPANSION –

Vertical Expansion – The 9403 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4.* Using the same technique, any FIFO of (15n + 1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 9403's flexibility for serial/parallel input and output. For other expansion schemes, refer to the applications section of this book.

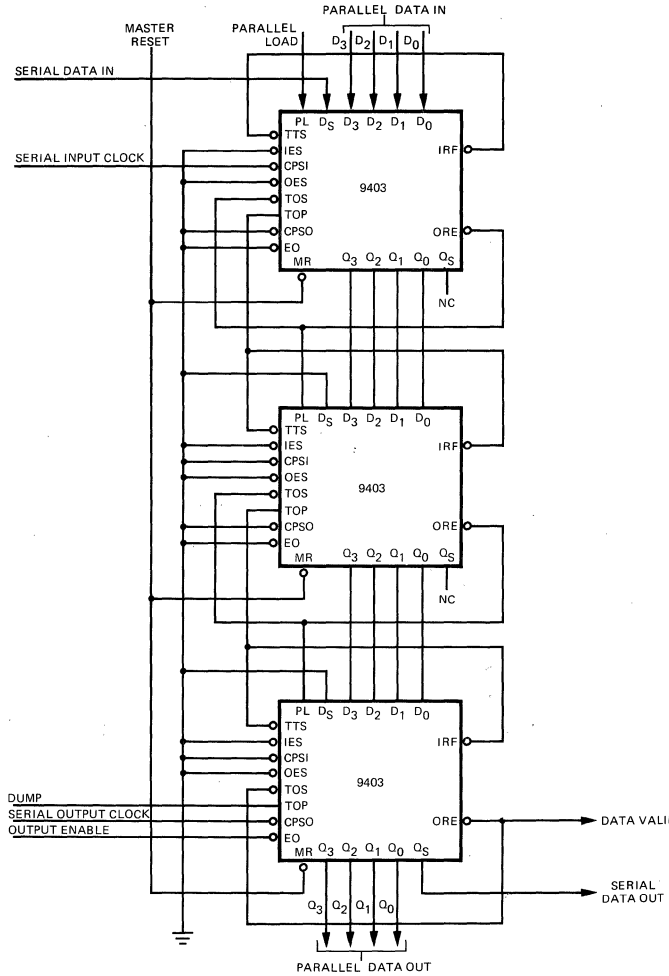


Fig. 4
A VERTICAL EXPANSION SCHEME

Horizontal Expansion – The 9403 can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in *Figure 5.* Using the same technique, any FIFO of 16 words by 4n bits can be constructed, where n is the number of devices. The $\overline{IRF}$ output of the right most device (most significant device) is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 9403's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. A single FIFO is guaranteed to operate at 10 MHz; an array of four FIFOs connected in the above manner is guaranteed at 4.3 MHz. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of this book.

Horizontal and Vertical Expansion – The 9403 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6.* Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 7 and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6.* The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9.*

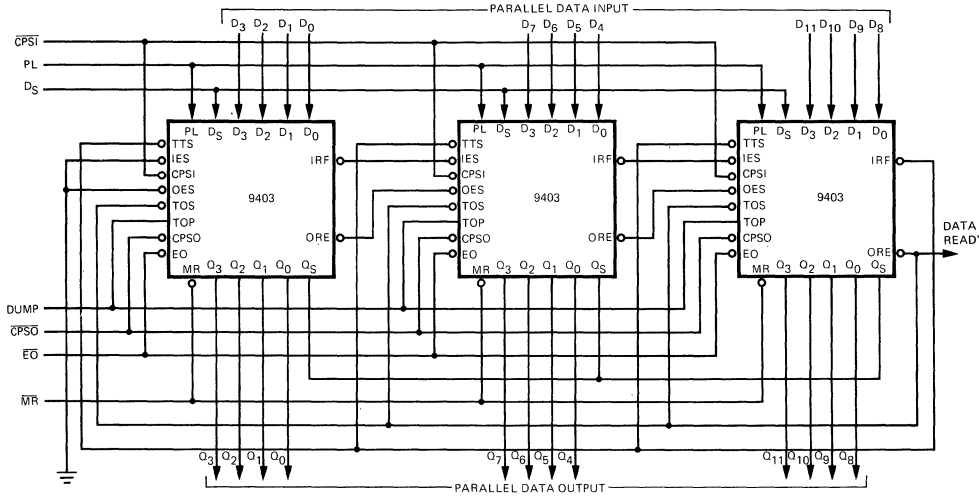


Fig. 5
A HORIZONTAL EXPANSION SCHEME

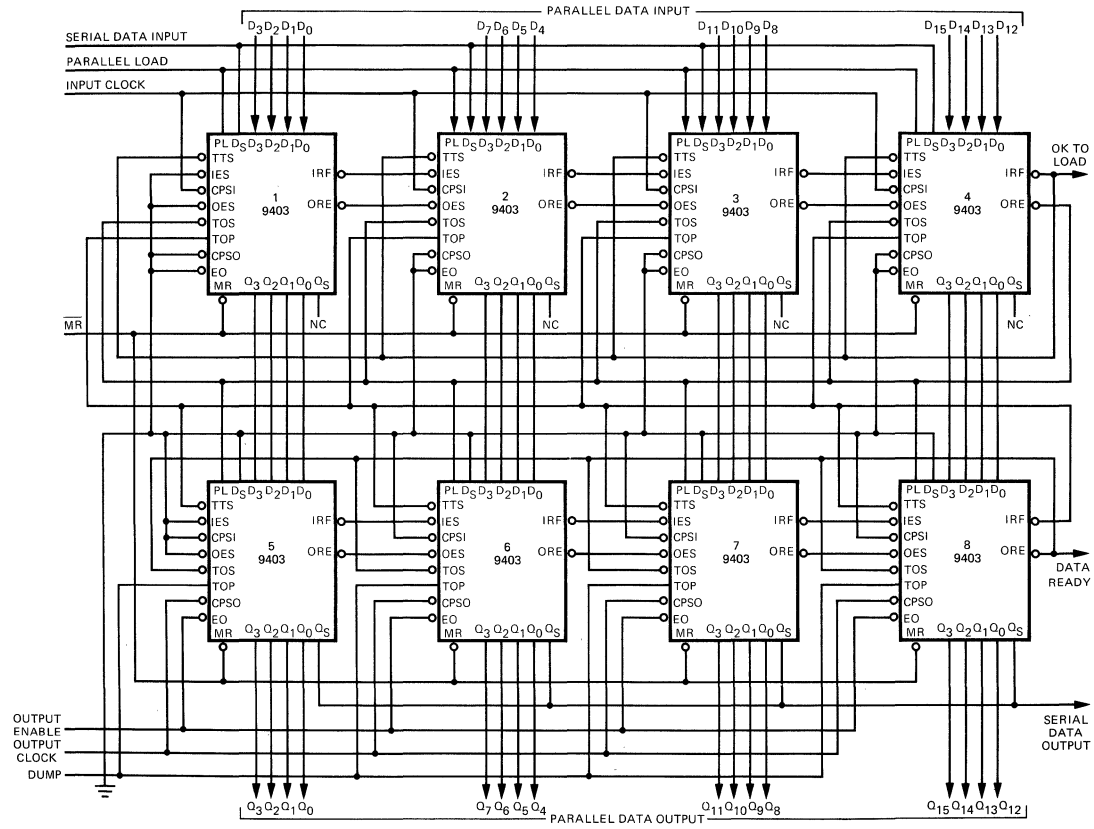


Fig. 6
A 31 X 16 FIFO ARRAY

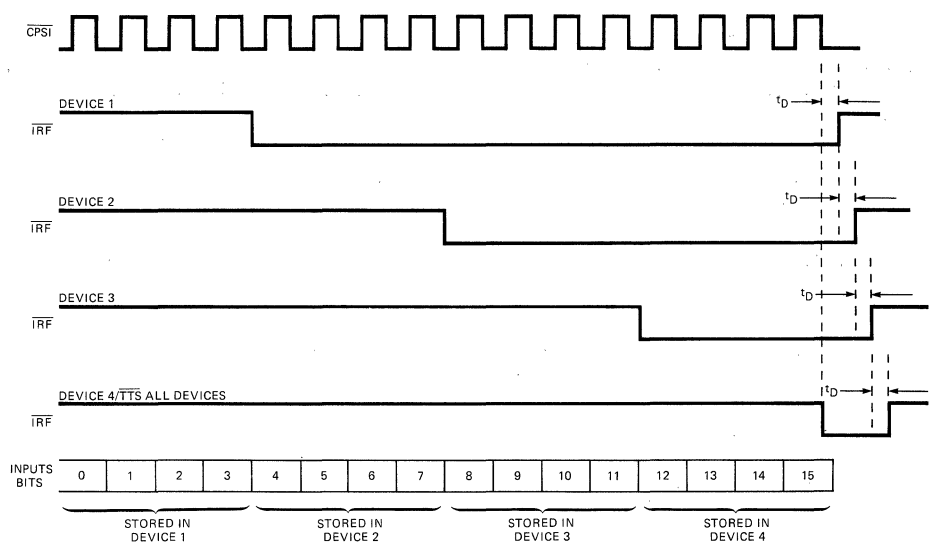


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

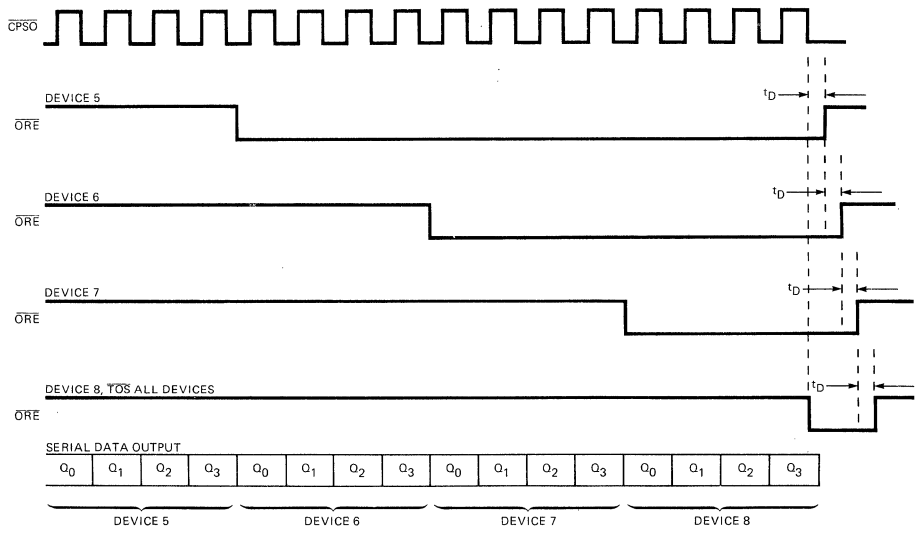


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

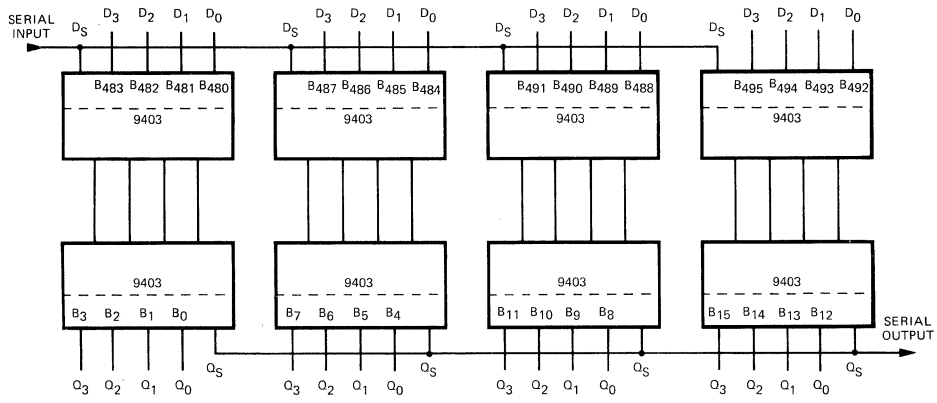


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

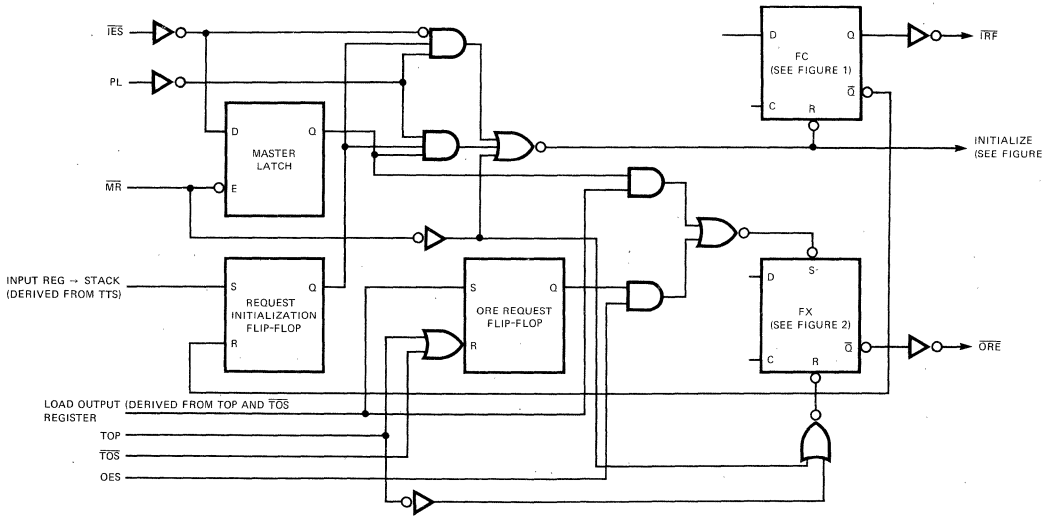


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, $\overline{ORE}$, $\overline{IRF}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage, Q_0-Q_3, Q_S	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA
V_{OL}	Output LOW Voltage, Q_0-Q_3, Q_S	XM		0.25	0.4	V	I_{OL} = 8.0 mA, V_{CC} = MIN
		XC		0.35	0.5	V	I_{OL} = 16 mA
V_{OL}	Output LOW Voltage, $\overline{ORE}$, $\overline{IRF}$	XM		0.25	0.4	V	I_{OL} = 4.0 mA, V_{CC} = MIN
		XC		0.35	0.5		I_{OL} = 8.0 mA
I_{OZH}	Output Off HIGH Current Q_0-Q_3, Q_S				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Output Off LOW Current Q_0-Q_3, Q_S				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, all except $\overline{OES}$				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Input LOW Current, $\overline{OES}$				−0.96		
I_{OS}	Output Short Circuit Current Q_0-Q_3, Q_S, $\overline{ORE}$, $\overline{OES}$		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0, (Note 3)
I_{CC}	Supply Current	XM		115	155	mA	V_{CC} = MAX, Inputs Open
		XC		115	170		

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PHL}	Propagation Delay, Negative-Going CP to $\overline{IRF}$ Output		18	25	ns	Stack not Full, PL LOW, Figures 11 and 12
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$		48	64	ns	
t_{PLH}, t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output		30	40	ns	$\overline{OES}$ LOW, TOP HIGH, Figures 13 and 14
			17	23	ns	
t_{PLH}, t_{PHL}	Propagation Delay, Positive-Going TOP to Outputs Q_0 − Q_3		40	56	ns	$\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
			31	45	ns	
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$		32	42	ns	$\overline{OES}$ LOW, TOP HIGH, Figures 13 and 14
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$		40	54	ns	Parallel Output, $\overline{EO}$, $\overline{CPSO}$ LOW, Figure 15
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$		51	68		
t_{DFT}	Fall Through Time		450	600	ns	$\overline{TTS}$ Connected to $\overline{IRF}$, $\overline{TOS}$ Connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH, Figure 16
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$		41	53	ns	Data in stack, TOP HIGH, Figures 13 and 14

AC CHARACTERISTICS (Cont'd): V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PHL}	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$		33	44	ns	Stack not Full, Figures 17 and 18
t_{PLH}	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$		20	28	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$		26	38	ns	
t_{PLH}	Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$		31	40	ns	Figure 18
t_{PZL}, t_{PZH}	Propagation Delay, $\overline{OE}$ to Q_0,Q_1,Q_2,Q_3		9.0	14	ns	Propagation Delay Out of the High Impedance State
t_{PHZ}, t_{PLZ}	Propagation Delay, $\overline{OE}$ to Q_0,Q_1,Q_2,Q_3		7.0	14	ns	Propagation Delay Into the High Impedance State
t_{PZL}, t_{PZH}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		13	18	ns	Propagation Delay Out of the High Impedance State
t_{PLZ}, t_{PHZ}	Propagation Delay, Negative-Going $\overline{OES}$ to Q_S		7.0	14	ns	Propagation Delay Into the High Impedance State
t_{AP}	Parallel Appearance Time, $\overline{ORE}$ to $Q_0 - Q_3$		−12	−5.0	ns	Time elapsed between $\overline{ORE}$ going HIGH and valid data appearing at output. Negative number indicates data available before $\overline{ORE}$ goes HIGH.
t_{AS}	Serial Appearance Time, $\overline{ORE}$ to Q_S		6.0	10	ns	

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{PWH}	$\overline{CPSI}$ Pulse Width (HIGH)	25	19		ns	Stack not full, PL LOW,
t_{PWL}	$\overline{CPSI}$ Pulse Width (LOW)	20	11		ns	Figures 11 and 12
t_{PWH}	PL Pulse Width (HIGH)	40	29		ns	Stack not full, Figures 17 and 18
t_{PWL}	$\overline{TTS}$ Pulse Width (LOW) Serial or Parallel Mode	20	9.0		ns	Stack not full, Figures 11, 12, 17, 18
t_{PWL}	$\overline{MR}$ Pulse Width (LOW)	25	13		ns	Figure 16
t_{PWH}	TOP Pulse Width (High)	20	13		ns	$\overline{CPSO}$ LOW, data available in stack,
t_{PWL}	TOP Pulse Width (LOW)	30	17		ns	Figure 15
t_{PWH}	$\overline{CPSO}$ Pulse Width (HIGH)	32	18		ns	TOP HIGH, data in stack,
t_{PWL}	$\overline{CPSO}$ Pulse Width (LOW)	30	16		ns	Figures 13 and 14
t_s	Set-up Time, D_S to Negative $\overline{CPSI}$	28	17		ns	PL LOW, Figures 11 and 12
t_h	Hold Time, D_S to $\overline{CPSI}$	0	−6.0		ns	PL LOW, Figures 11 and 12
t_s	Set-up Time, $\overline{TTS}$ to $\overline{IRF}$ Serial or Parallel Mode	0	−20		ns	Figures 11, 12, 17, 18
t_s	Set-up Time Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$	0	−24		ns	TOP HIGH, Figures 13 and 14
t_{rec}	Recovery Time $\overline{MR}$ to any Input	10	5.0		ns	Figure 16
t_s	Set-up Time, Negative-Going $\overline{IES}$ to $\overline{CPSI}$	32	23		ns	Figure 12
t_s	Set-up Time, Negative-Going $\overline{TTS}$ to $\overline{CPSI}$	76	58		ns	Figure 12
t_s	Set-up Time, Parallel Inputs to PL	0	−22		ns	Length of time parallel inputs must be applied prior to rising edge of PL.
t_h	Hold Time, Parallel Inputs to PL	0			ns	Length of time parallel inputs must reamin applied after falling edge of PL.

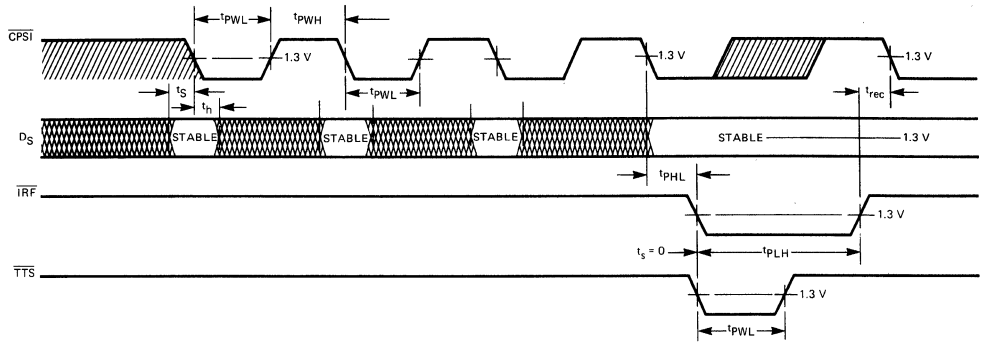


Fig. 11
SERIAL INPUT, UNEXPANDED OR MASTER OPERATION
Conditions: stack not full, $\overline{IES}$, PL LOW

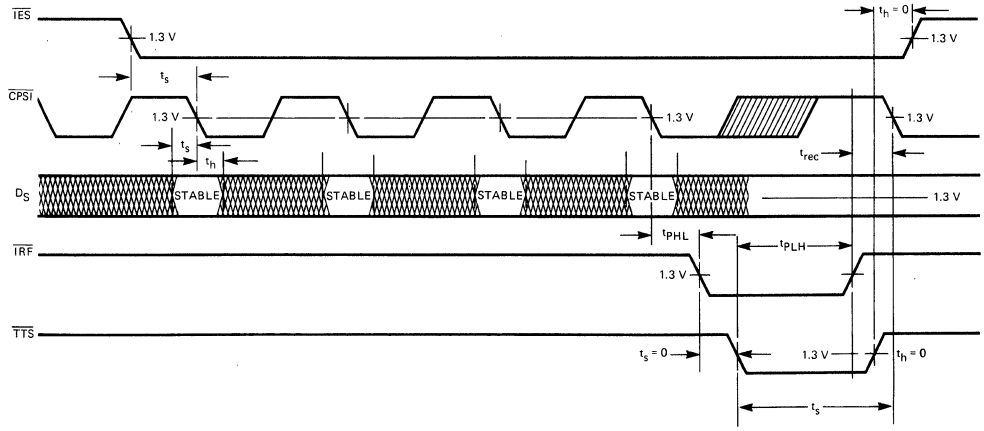


Fig. 12
SERIAL INPUT, EXPANDED SLAVE OPERATION
Conditions: stack not full, $\overline{IES}$ HIGH when initiated, PL LOW

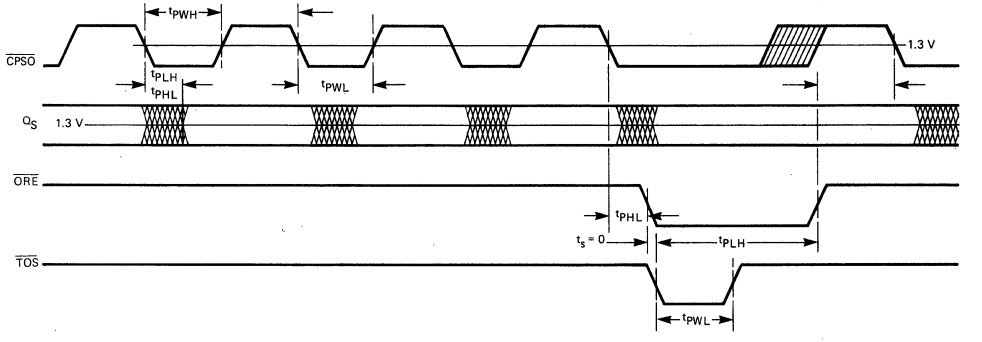


Fig. 13
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION
Conditions: data in stack, TOP HIGH, $\overline{IES}$ LOW when initiated, $\overline{OES}$ LOW

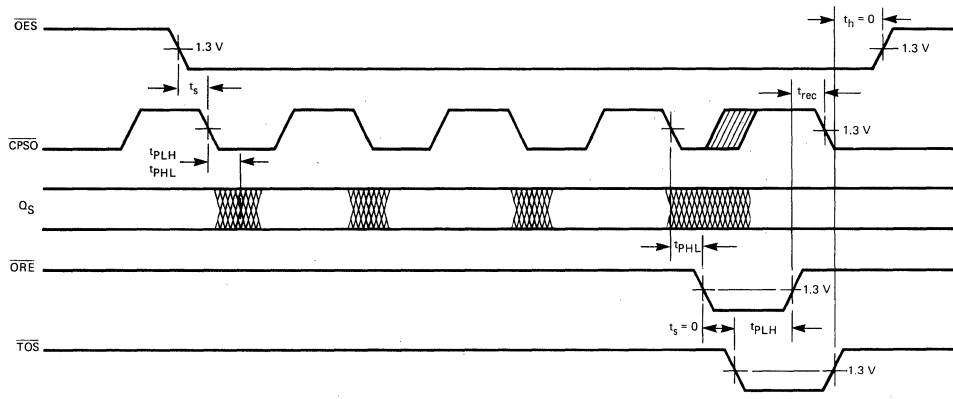


Fig. 14
SERIAL OUTPUT, SLAVE OPERATION

Conditions: data in stack, TOP HIGH, $\overline{IES}$ HIGH when initiated

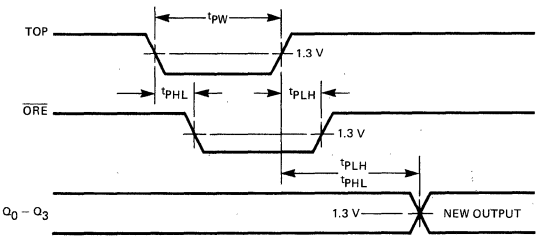


Fig. 15
PARALLEL OUTPUT, 4-BIT WORD OR MASTER IN PARALLEL EXPANSION

Conditions: $\overline{IES}$ LOW when initiated, $\overline{EO}$, $\overline{CPSO}$ LOW; data available in stack

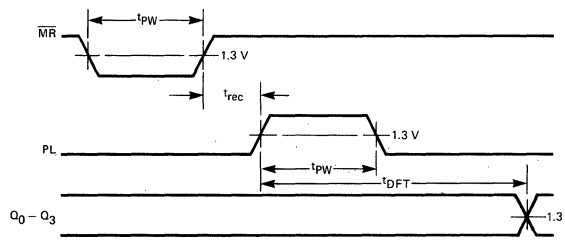


Fig. 16
FALL THROUGH TIME

Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ LOW, TOP HIGH

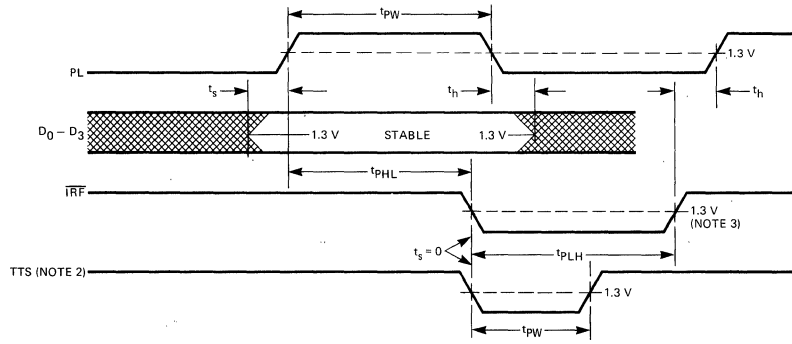


Fig. 17
PARALLEL LOAD MODE, 4-BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION
Conditions: stack not full, $\overline{IES}$ LOW when initialized

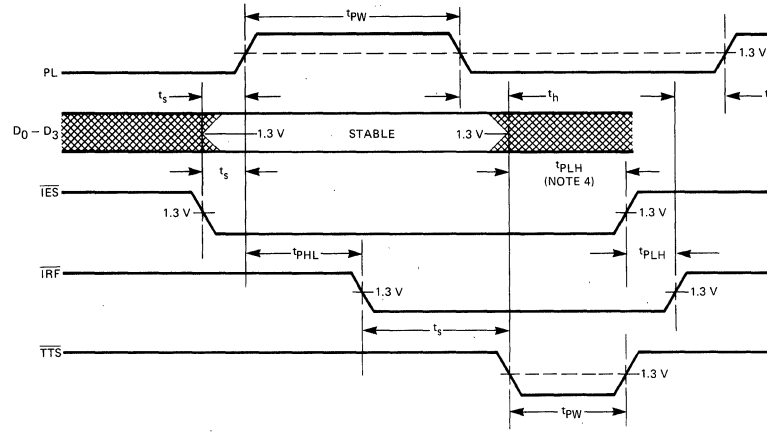


Fig. 18
PARALLEL LOAD, SLAVE MODE
Conditions: stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, IRF will stay LOW.

9404
DATA PATH SWITCH
FAIRCHILD TTL MACROLOGIC

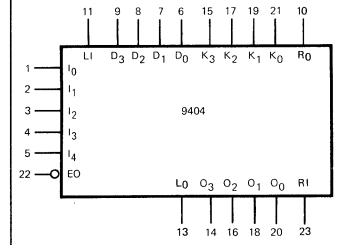
DESCRIPTION – The 9404 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the 9405A (Arithmetic Logic Register Stack). A total of 30 instructions (see Table 1) facilitate logic shifting, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction (I_0–I_4) selects one of the 30 instructions operating on two sets of 4-bit data inputs (D_0–D_3, K_0–K_3). Left Input (LI), Left Output (LO), Right Input (RI) and Right Output (RO) are available for expansion in 4-bit increments. An active LOW Output Enable input ($\overline{EO}$) provides 3-state control of the Data Outputs (O_0–O_3) for bus oriented applications.

The 9404 is fully compatible with all TTL families.

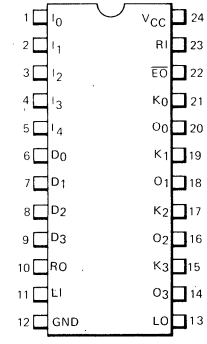
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **20 ns DELAY OVER 16-BIT WORD (EXCEPT SIGN EXTEND FUNCTION)**
- **TWO 4-BIT DATA INPUT BUSSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0–D_3	D-Bus Inputs (active LOW)	1.0 U.L.	0.23 U.L.
K_0–K_3	K-Bus Inputs (active LOW)	1.0 U.L.	0.23 U.L.
I_0–I_4	Instruction Input	1.0 U.L.	0.23 U.L.
LI	Shift Left Input (active LOW)	1.0 U.L.	0.23 U.L.
LO	Shift Left Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
RI	Shift Right Input (active LOW)	1.0 U.L.	0.23 U.L.
RO	Shift Right Output (active LOW) (Note b)	10 U.L.	5.0 U.L.
$\overline{EO}$	Output Enable Input (active LOW)	1.0 U.L.	0.23 U.L.
O_0–O_3	Data Output (Note b)	130 U.L.	10 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V

BLOCK DIAGRAM

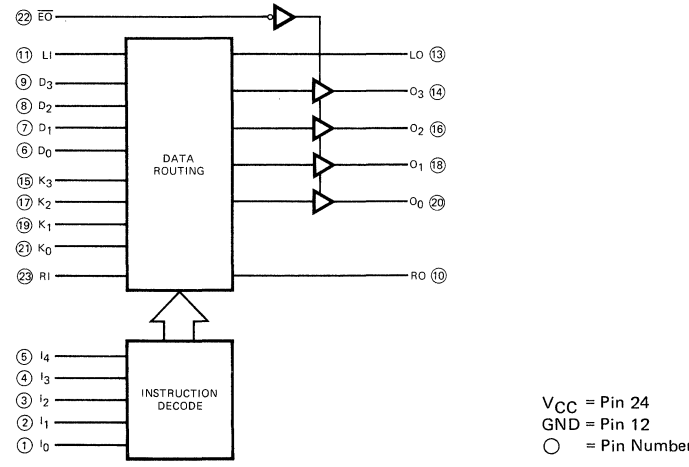


TABLE 1
INSTRUCTION SET FOR THE 9404

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS						FUNCTION
I_4	I_3	I_2	I_1	I_0	O_3	O_2	O_1	O_0		I_4	I_3	I_2	I_1	I_0	LO	O_3	O_2	O_1	O_0	RO	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	RI	RI	RI	RI	RI		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	K_3	K_3	K_2	K_1	K_0		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)	H	L	L	H	L	RI	RI	RI	RI	RI		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)	H	L	L	H	H	D_3	D_3	D_2	D_1	D_0		D-Bus Sign Extend
L	L	H	L	L	D_3	D_2	D_1	D_0	Byte Mask, D-Bus	H	L	H	L	L	D_3	D_2	D_1	D_0	RI		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask, D-Bus	H	L	H	L	H	K_3	K_2	K_1	K_0	RI		K-Bus Shift Left
L	L	H	H	L	D_3	D_2	D_1	D_0	Byte Mask, D-Bus	H	L	H	H	L		LI	D_3	D_2	D_1	D_0	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask, D-Bus	H	L	H	H	H		D_3	D_3	D_2	D_1	D_0	D-Bus Shift Right Arith(2)
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		LI	K_3	K_2	K_1	K_0	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		K_3	K_3	K_2	K_1	K_0	K-Bus Shift Right Arith(2)
L	H	L	H	L	K_3	K_2	K_1	K_0	Byte Mask, K-Bus	H	H	L	H	L		K_3	K_2	K_1	K_0		Byte Mask, K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask, K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask, K-Bus
L	H	H	L	L	D_3	D_2	D_1	D_0	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	K_3	K_2	K_1	K_0	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined (Reserved)
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined (Reserved)

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

FUNCTIONAL DESCRIPTION – The 9404 combines the functions of a dual 4-input multiplexer, a true/complement one/zero generator, and a shift left/shift right array.

As shown in *Table 1*, there are two shift right modes. The arithmetic right shift preserves the sign bit in the most significant position while the logic shift moves all positions. Right shift is defined as a 1-bit shift toward the least significant position.

For half-word arithmetic the 9404 provides instructions which extend the sign bit left through the more significant slices. Shift linkages are available as individual inputs and outputs for complete flexibility.

The 9404 may be used to generate constants +1, 0, –1 and –2 in 2's complement notation.

EXPANSION – Arrays of larger than 4-bit word lengths are easily obtained. *Figure 1* illustrates a 16-bit array constructed using four devices; device 1 is the least significant and device 4 is the most significant slice. Within each slice, inputs and outputs with '0' subscript are the least significant bits.

The I_1 through I_4 inputs of all devices are bussed. These four bus lines together with the I_0 inputs of the devices form an 8-bit instruction bus to control the array. In some applications, it may be possible to connect the I_0 inputs of devices 1 and 2 together and the I_0 inputs of devices 3 and 4 together, so that only six bits are needed to control the arrays. Connecting the LO of device 1 to RI of device 2, LO of device 2 to RI of device 3, etc., provides left shift (*i.e.*, shift towards most significant bit) and sign extension. In a similar fashion right shift operation is accomplished by connecting the LI input of a device to the RO of the next more significant device.

The sign-extend group consists of two adjacent instructions differing only in I_0 (refer to *Table 1*). When the code HLLHH is placed on the instruction inputs (D-Bus Sign Extend), the most significant bit of the D bus (D3) is available on the LO output. The companion code HLLHL will copy the RI input (connected to LO of the previous stage) onto the output bus (D_0 – D_3) and to its own LO output. Thus when a sign extend function is desired (e.g., arithmetic operations on the eight least significant bits in a 16-bit machine) the code HLLH will be applied to instruction inputs (I_4,I_3,I_2,I_1) of all the 9404s. I_0 of the most significant byte will be LOW and I_0 of the least significant byte will be HIGH. In a similar fashion sign-extend function on a number present on the K-Bus is executed by the code HLLL on I_4,I_3,I_2, and I_1.

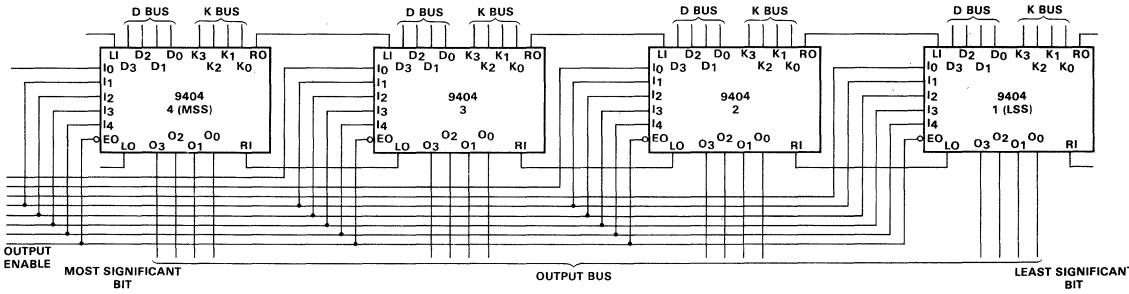


Fig. 1
16-BIT 9404 ARRAY

The 9404 provides several options for masking operations. For example, Byte Mask operation (LLLL on I_4,I_3,I_2,I_1) will force the output bus either HIGH or LOW depending on I_0. Connecting I_0 of the most significant byte HIGH and I_0 of the least significant byte LOW will force the outputs of the DPS array to a state of (00FF) 16. A LOW on any output is assumed as logic 1. When the output bus of the 9404 is used as an input to a 16-bit Arithmetic Logic Register Stack (ALRS) network (see *Figure 2*), the ALRS can execute a logic AND function between its input bus and one of its registers, thus masking the least significant byte of that register. More complex masking operation can be executed using the Byte AND Mask and Byte OR Mask operations (see *Table 1*).

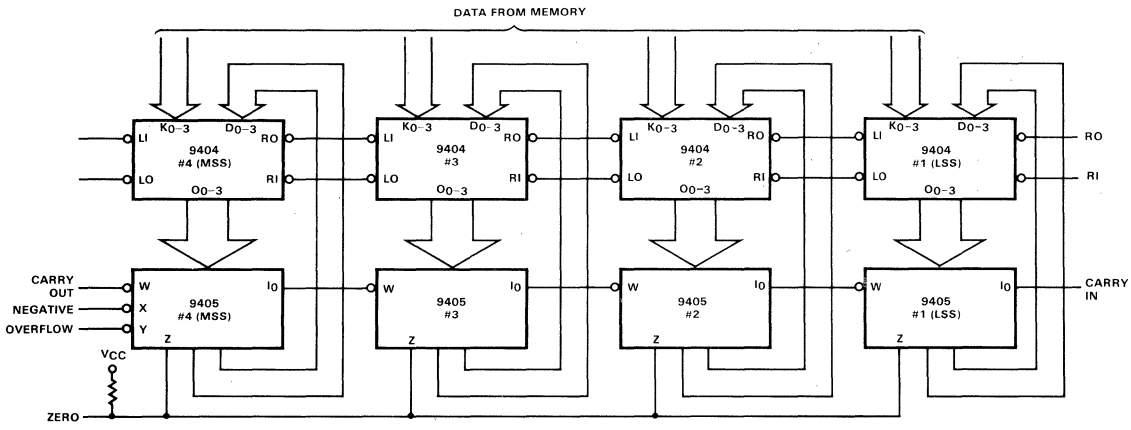


Fig. 2
16-BIT DATA PATH

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage LO, RO	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage O_0-O_3	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage LO, RO	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage O_0-O_3	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2.0 V
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2.0 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			60	90	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs (D_0-D_3, K_0-K_3) to Output (O_0-O_3)		18	25	ns	$\overline{EO}$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs (D_0-D_3, K_0-K_3) to Shift Outputs (LO, RO)		12	17	ns	
t_{PLH} t_{PHL}	Propagation Delay, RI to LO		12	17	ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction (I_0-I_5) to Data Outputs (O_0-O_3)		19	27	ns	
t_{PLH} t_{PHL}	Propagation Delay, Instruction (I_0-I_5) to Shift Outputs (RO, LO)		19	27	ns	
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs (O_0-O_3)		12	17	ns	
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}$ to Outputs (O_0-O_3)		9	15	ns	

9405
ARITHMETIC LOGIC REGISTER STACK
FAIRCHILD TTL MACROLOGIC

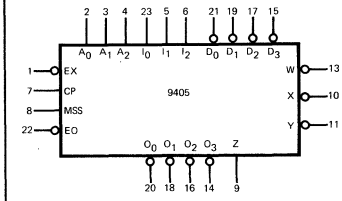
DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement accumulators in high performance microprogrammed digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0–A_2). The result of the operation is loaded into the same RAM location and simultaneously, is loaded into the Output Register making it available at the 3-state output data bus.

The 9405 operates on four bits of data but features are provided for expansion to longer word lengths. Carry propagate and carry generate facilities are provided for an external carry lookahead where maximum operating speed is required. In applications where high speed arithmetic is not needed, ripple expansion may also be implemented. The 9405 provides three status signals: Zero, Negative and Overflow. These qualify the result of an operation. The 9405 is fully compatible with all TTL families.

Note: The 9405A is recommended for all new designs. See the 9405A data sheet.

- **EIGHT ACCUMULATORS IN A SINGLE PACKAGE**
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES STATUS – ZERO, NEGATIVE, AND OVERFLOW**
- **3-STATE OUTPUTS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



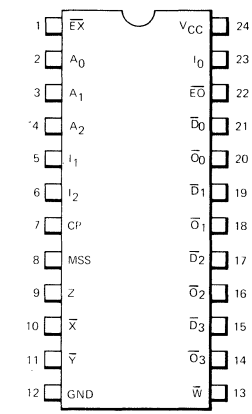
V_{CC} = Pin 24
GND = Pin 12

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0$-$\overline{D}_3$	Data Inputs	1.0 U.L.	0.23 U.L.
A_0-A_2	Address Instruction Inputs	1.0 U.L.	0.23 U.L.
I_0-I_2	ALU Instruction Inputs (Note b)	1.0 U.L.	0.23 U.L.
MSS	Most Significant Slice Input (Active HIGH)	1.0 U.L.	0.23 U.L.
CP	Clock Input	1.0 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{O}_0$-$\overline{O}_3$	Data Outputs (Active LOW)	130 U.L.	10 U.L.
$\overline{W}$	Ripple Carry Output (Active LOW) (Note c)	10 U.L.	5 U.L.
$\overline{X}$	Carry Propagate Output (Note d)	10 U.L.	5 U.L.
$\overline{Y}$	Carry Generate Output (Note e)	10 U.L.	10 U.L.
Z	Zero Status Output (Active HIGH, Open Collector) (Note f)		5 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW (0.5 V).
b) I_0 used also for Carry Input on lesser significant slices.
c) $\overline{W}$ Output also carries instruction information.
d) $\overline{X}$ Output provides Negative Status (active LOW) on most significant slice.
e) $\overline{Y}$ Output provides Overflow Status (active LOW) on most significant slice.
f) An external pull-up resistor is required to supply HIGH level drive capability.

CONNECTION DIAGRAM
DIP (TOP VIEW)



3

BLOCK DIAGRAM

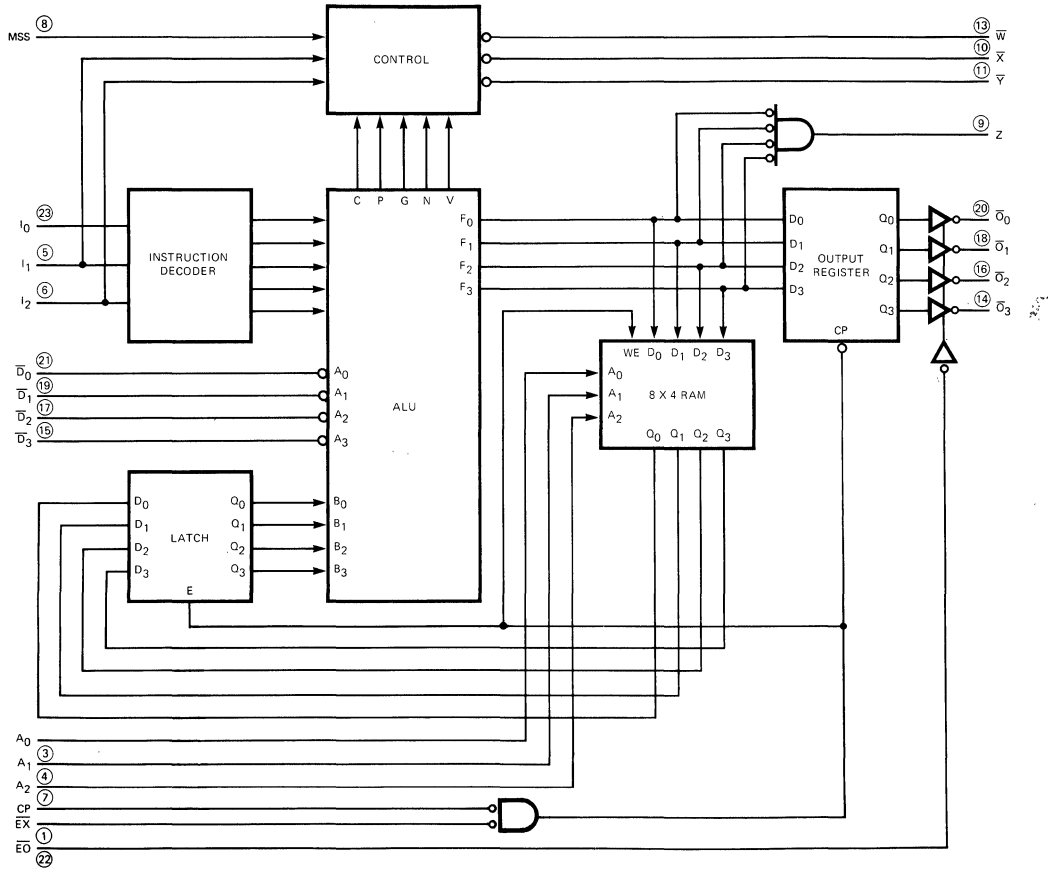


TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2 I_1 I_0	INTERNAL OPERATION	
L L L	R_X plus $\overline{\text{D-Bus}}$ plus 1 → R_X	Accumulate
L L H	R_X plus $\overline{\text{D-Bus}}$ → R_X	Accumulate
L H L	$R_X \cdot \overline{\text{D-Bus}} \rightarrow R_X$	Logical AND
L H H	$\overline{\text{D-Bus}} \rightarrow R_X$	Load
H L L	R_X → Output Register	Output
H L H	$R_X + \overline{\text{D-Bus}} \rightarrow R_X$	Logical OR
H H L	$R_X \oplus \overline{\text{D-Bus}} \rightarrow R_X$	Exclusive OR
H H H	D-Bus → R_X	Load Complement

NOTES:
1. R_X is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

FUNCTIONAL DESCRIPTION – As shown in the block diagram the 9405 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an Instruction Decoder, control logic and a 4-bit Output Register.

The ALU receives the active LOW input data ($\overline{D}_0$–$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and Output Register. The active LOW output data ($\overline{O}_0$–$\overline{O}_3$) is obtained from the Output Register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level $\overline{EO}$ disables the buffers (high impedance state).

The instruction bus for the 9405 consists of two fields, A and I; A_0–A_2 specify the desired location of the RAM and I_0–I_2 specify the desired function to be performed. *Table 1* lists instruction code assignments. Thus, the 9405 provides eight accumulators (R_0–R_7) and eight different operations may be performed on any of these accumulators. The I_0–I_2 inputs are decoded by the Instruction Decoder to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: Carry Out (C), Carry Propagate (P), Carry Generate (G), Negative (N) and Overflow (V) status. The control logic manipulates the status signals as a function of I_0–I_2 and a control input MSS. A HIGH on the MSS input declares the most significant slice in a 9405 array (the MSS can be tied directly to V_{CC}). All devices, except the most significant 9405 should have a LOW level (ground) on the MSS input. The control logic generates three device outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$ for arrayed operation. An all zero result from the ALU is decoded and presented at the open collector Zero (Z) output.

The I_0 input serves a dual purpose. For arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 9405 expansion schemes.

Operation – The 9405 operates on a single clock. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$–$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0–I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. The A lines must obviously be held stable during this time. On the LOW-to-HIGH transition of the CP, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

EXPANSION – The 9405 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 9405 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Progagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 9405s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices. The Z output is open collector and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four 9405s. The MSS input is tied to V_{CC} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-field and I-field. A-field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, it assumes the state of the I_0 input. Thus, in *Figure 1*, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 inputs together to form the I-field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

The $\overline{X}$ output of device 4 is LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP. *Figure 2* shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 93S42/74S182 in addition to the four 9405s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs together with the I_0 input of device 1 form the I-field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the 93S42/74S182 carry outputs (C_{n+x}, C_{n+y}, and C_{n+z} respectively). Also the P

and G inputs of 93S42/74S182 are connected to $\overline{X}$ and $\overline{Y}$ outputs of the 9405s as shown. The control logic in the 9405 (see block diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs as well as the Carry Generate and Carry Propagate outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output reflects Carry Propagate and $\overline{Y}$ reflects Carry Generate outputs from that slice. For an arithmetic instruction the I_0 input is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ output of device 4 is the carry output from the array. Also, note that the I_0 input of device 1 is not only an instruction input but also provides the carry input to the array so the I_0 input of device 1 must be connected to the appropriate 93S42/74S182 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 9405 forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ outputs on all except the most significant slice. An examination of the 93S42/74S182 logic reveals that whenever P is LOW and G is HIGH the associated carry output is the same as the carry input. Thus, in *Figure 2* devices 2, 3, and 4 will assume the logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent Negative and Overflow from the array.

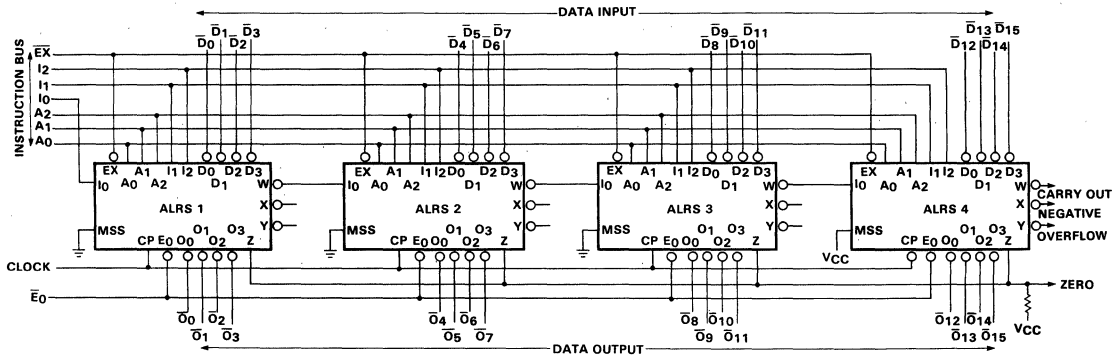


Fig. 1
RIPPLE CARRY EXPANSION

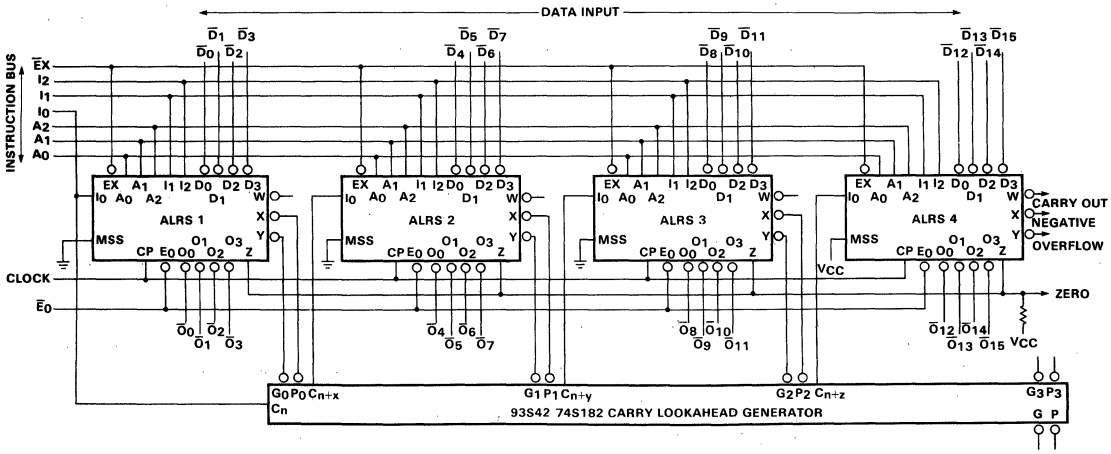


Fig 2.
CARRY LOOKAHEAD EXPANSION

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{W}$, $\overline{X}$ Outputs	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current Z Output				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{W}$, $\overline{X}$, Z	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$, $\overline{Y}$	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off Current HIGH				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off Current LOW				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30	−60	−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			110	160	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Positive Going CP to $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		18	25	ns	$\overline{EO}$, $\overline{EX}$ LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		15	20	ns	I_1 or I_2 HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to $\overline{W}$		30	40	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to $\overline{X}$, $\overline{Y}$		36	54	ns	MSS HIGH, I_1, I_2 LOW
			30	40	ns	MSS LOW, I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Dealy, I_1, I_2 to $\overline{X}$, $\overline{Y}$		36	48	ns	MSS LOW
t_{PLH}, t_{PHL}	Propagation Delay, Data ($\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$) to Z		53	70	ns	1 kΩ External Load Resistor to V_{CC}
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		33	44	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to $\overline{W}$		17	26	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{D}_3$ to $\overline{X}$		46	60	ns	I_1, I_2 HIGH, MSS HIGH

3

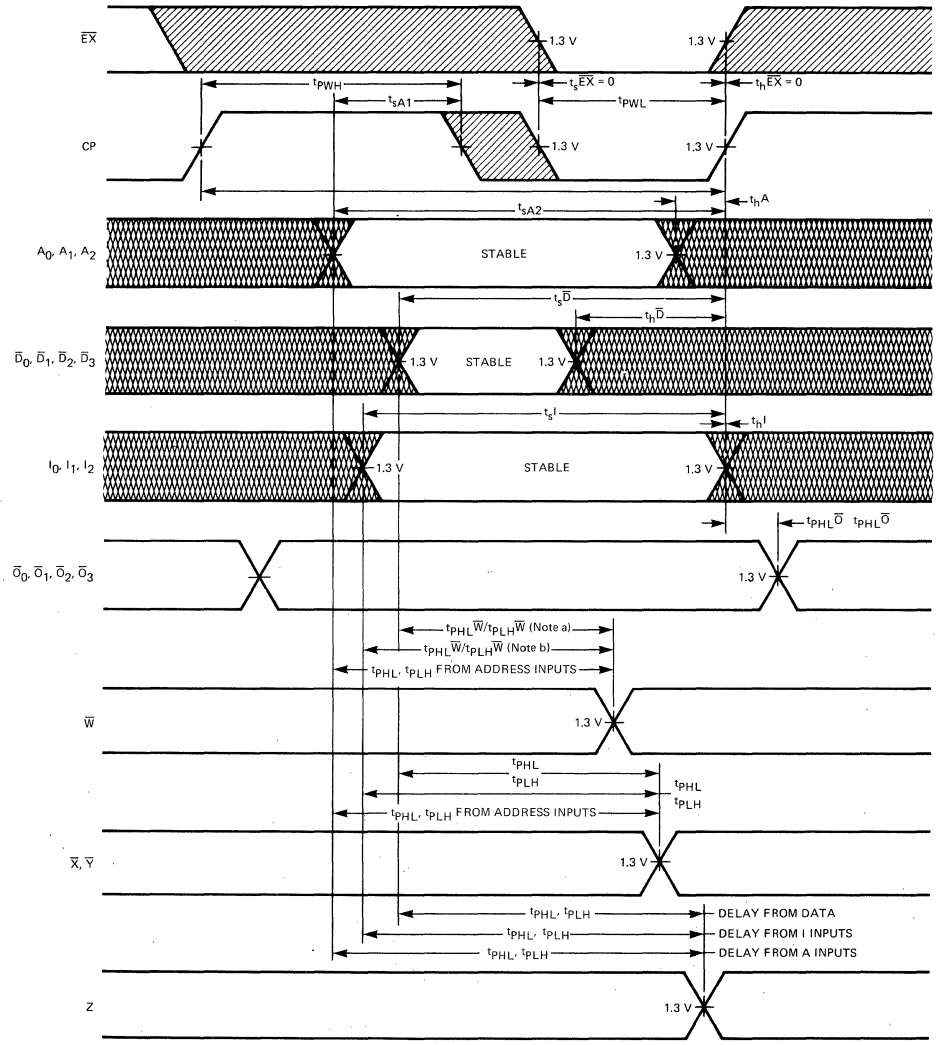
AC CHARACTERISTICS (Cont'd): V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$, $\overline{Y}$		49	64	ns	I_1, I_2 LOW, MSS LOW
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$, $\overline{Y}$		72	95	ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{X}$		72	95	ns	I_1, I_2 HIGH, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to $\overline{W}$		50	65	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to Z		61	80	ns	I_1, I_2 LOW
t_{PLH} t_{PHL}	Propagation Delay, I_1, I_2 to $\overline{X}$, $\overline{Y}$		23 48	31 63	ns ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to $\overline{X}$, $\overline{Y}$		43	57	ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to Z		42	60	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to Z		28	40	ns	I_1, I_2 LOW
t_{PZH}, t_{PZL}	Enable Delay, $\overline{EO}$ to Outputs $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		10	16	ns	
t_{PLZ}, t_{PHZ}	Disable Display, $\overline{EO}$ to $\overline{O}_0$, $\overline{O}_1$, $\overline{O}_2$, $\overline{O}_3$		10	16	ns	

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{CW}	Clock Period	90	60		ns	
t_{PWH}	Clock Pulse Width (HIGH)	40	25		ns	
t_{PWL}	Clock Pulse Width (LOW)	25	15		ns	
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Rising Edge	35	20		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP Rising Edge	0			ns	
t_{sA1}	Set-Up Time, A_0, A_1, A_2 to Negative Going CP (Note 1)	45	28		ns	
t_{sA2}	Set-Up Time, A_0, A_1, A_2 to Positive Going CP (Note 1)	90	60		ns	
t_hA	Hold Time, A_0, A_1, A_2 to Positive Going CP	0	−3.0		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive Going CP	50	33		ns	$\overline{EX}$ LOW
$t_h\overline{D}$	Hold Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive Going Clock	0	−25		ns	
t_sI1	Set-Up Time, I_0, I_1, I_2 to Negative Going Clock	8.0	4.0		ns	
t_hI	Hold Time, I_0 I_1, I_2 to Positive Going Clock	0	−12		ns	
t_sI2	Set-Up Time, I_1, I_2 to Positive Going Clock	70	50		ns	
t_sI3	Set-Up Time I_0 to Positive Going Clock	36	24		ns	

NOTE:
1. Both set-up times must be met simultaneously.



NOTES:
a) Delay for logical operation (I_1 or I_2 HIGH)
b) Delay for arithmetic operation ($I_1 = I_2$ = LOW)

Fig. 3
ALRS TIMING DIAGRAM

9405A

ARITHMETIC LOGIC REGISTER STACK

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9405A Arithmetic Logic Register Stack (ALRS) is designed to implement accumulators/general registers in high performance, microprogrammed digital systems (microprocessors). The 9405A is a 4-bit slice with expansion features for larger word lengths.

The device contains a 4-bit ALU, 8-word by 4-bit RAM, a 4-bit edge-triggered output register and associated control logic. The ALU implements eight arithmetic and logic functions on two 4-bit operands. The desired function is specified by three instruction inputs (I-field). One of the operands is supplied from an external source (D-Bus). The second operand is supplied internally from one of the eight RAM locations. The desired RAM location is specified by the address inputs (A-field) when the clock input is HIGH. The result from the ALU is loaded into a RAM location during the period when the clock input is LOW. The address for the desired RAM location for writing is also specified by the A-field. Moreover, the result from the ALU is also loaded into the output register on LOW-to-HIGH transistion of the clock input. The output register provides the 4-bit output (O-Bus) through 3-state buffers.

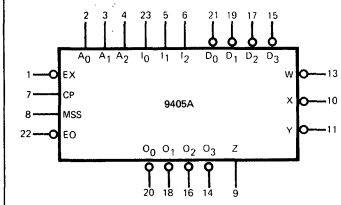
For accumulator oriented microprocessor architectures, the A-field inputs to the 9405A remain the same during the HIGH and LOW period of the clock cycle. However, in general register oriented architectures, the A-field inputs are changed appropriately to realize the source and destination registers during HIGH and LOW period of the clock respectively.

Carry propagate and carry generate outputs are provided by the 9405A to facilitate carry lookahead expansion. The industry standard 93S42/74S182 carry lookahead unit can be used for this purpose. If high speed arithmetic is not needed, ripply carry expansion can be used. The ripple expansion eliminates the need for an external carry lookahead unit. The 9405A also provides four status signals (condition codes) to characterize the result of an operation – Zero, Negative, Overflow and Carry.

The 9405A is downward compatible with the 9405 and should be used in new designs. The 9405A is fully compatible with all TTL families.

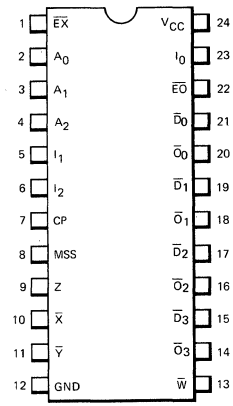
- **EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE**
- **OPTIMIZED FOR MICROPROGRAMMED OPERATION**
- **HIGH SPEED - 13 MHz MICROINSTRUCTION RATE (SINGLE SLICE)**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **PROVIDES STATUS - CARRY, ZERO, NEGATIVE AND OVERFLOW**
- **3-STATE OUTPUTS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)

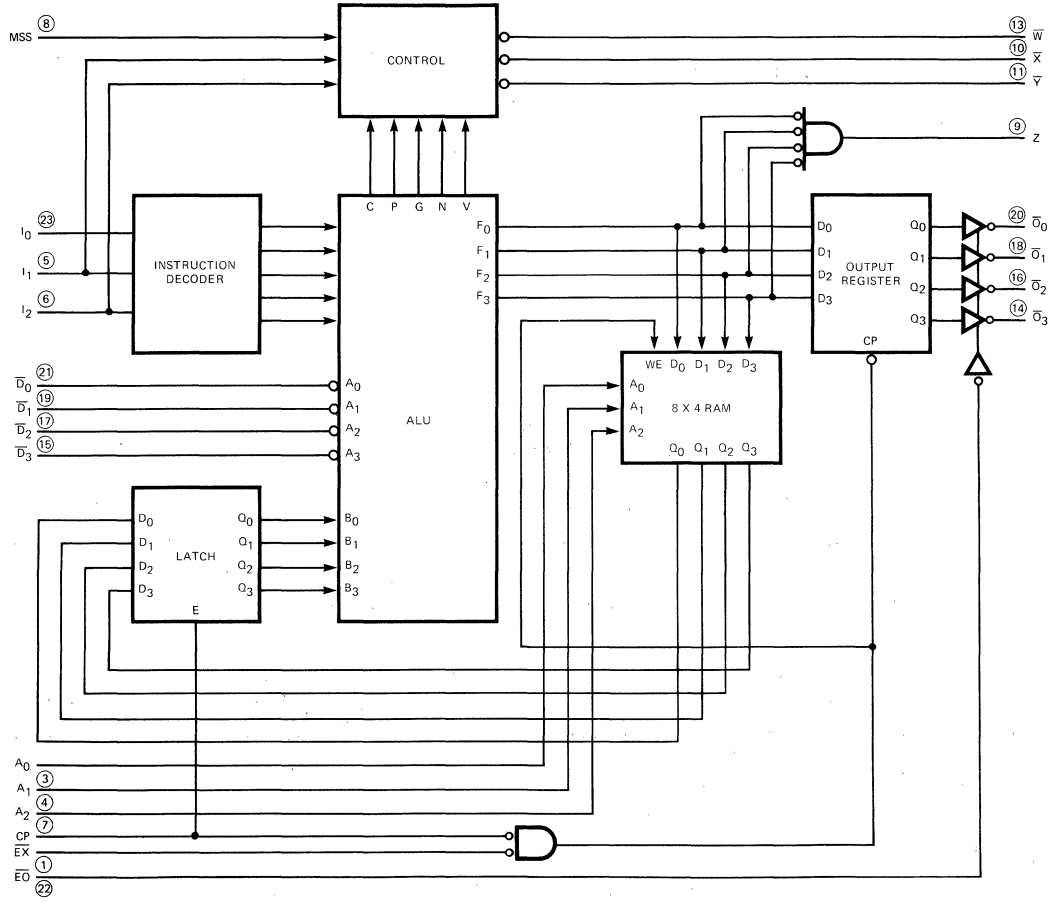


PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	1.0 U.L.	0.23 U.L.
$A_0 - A_2$	Address Inputs	1.0 U.L.	0.23 U.L.
$I_0 - I_2$	Instruction Inputs (Note b)	1.0 U.L.	0.23 U.L.
MSS	Most Significant Slice Input (Active HIGH)	1.0 U.L.	0.23 U.L.
CP	Clock Input	1.0 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active LOW)	130 U.L.	10 U.L.
$\overline{W}$	Ripple Carry Output (Active LOW) (Note c)	10 U.L.	5.0 U.L.
$\overline{X}$	Carry Propagate Output (Note d)	10 U.L.	5.0 U.L.
$\overline{Y}$	Carry Generate Output (Note e)	10 U.L.	5.0 U.L.
Z	Zero Status Output (Active HIGH, Open Collector)(Note f)		5.0 U.L.

NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW (0.5 V).
b) I_0 used also for carry input.
c) W output also carries instruction information.
d) X output provides Negative status (active LOW) on most significant slice.
e) Y output provides Overflow status (active LOW) on most significant slice.
f) An external pull-up resistor is required to supply HIGH drive capability.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 9405A consists of a 4-bit ALU, 8-word by 4-bit RAM with latches, an Instruction Decoder, control logic and a 4-bit Output Register.

The ALU receives the active LOW data ($\overline{D}_0 - \overline{D}_3$) as one operand while the RAM provides the second operand through its latches. The ALU output is fed as input to the RAM and the Output Register. The active LOW output bus ($\overline{O}_0 - \overline{O}_3$) is from the Output Register through 3-state buffers. A HIGH on the $\overline{EO}$ input disables the buffers (high impedance state) while a LOW enables them.

The 6-bit instruction input for the 9405A consists of two 3-bit fields: A-field and I-field. $A_0 - A_2$ specifies the operation to be performed. The 8-word RAM can be considered to be providing eight registers ($R_0 - R_7$) and eight different operations can be performed on these registers. The I-field inputs are decided by the Instruction Decoder to generate necessary control signals for the ALU. The ALU generates Carry (C), Carry Propagate (P), Carry Generate (G), Negative (N) and Overflow (V) signals to be used by the control logic. The control logic manipulates these signals as a function of the I-field inputs and an external control input signal MSS. The MSS input separates the most significant slice in an array of 9405As from the remaining slices. A HIGH on the MSS denotes the most significance (MSS input may be tied directly to V_{CC}). In general, all except the most significant 9405A will have a LOW on the MSS input. The control logic generates three user outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$. The significance of these outputs is discussed under the Expansion section. The Zero output (Z) is provided by an open collector transistor.

Table 1 lists the I-field assignment for the 9405A. There are only two arithmetic instructions in the table which require carry. It can also be noticed that the I_0 is the carry input. In the 9405A operation I_0 plays a dual role and will be discussed in the Expansion section.

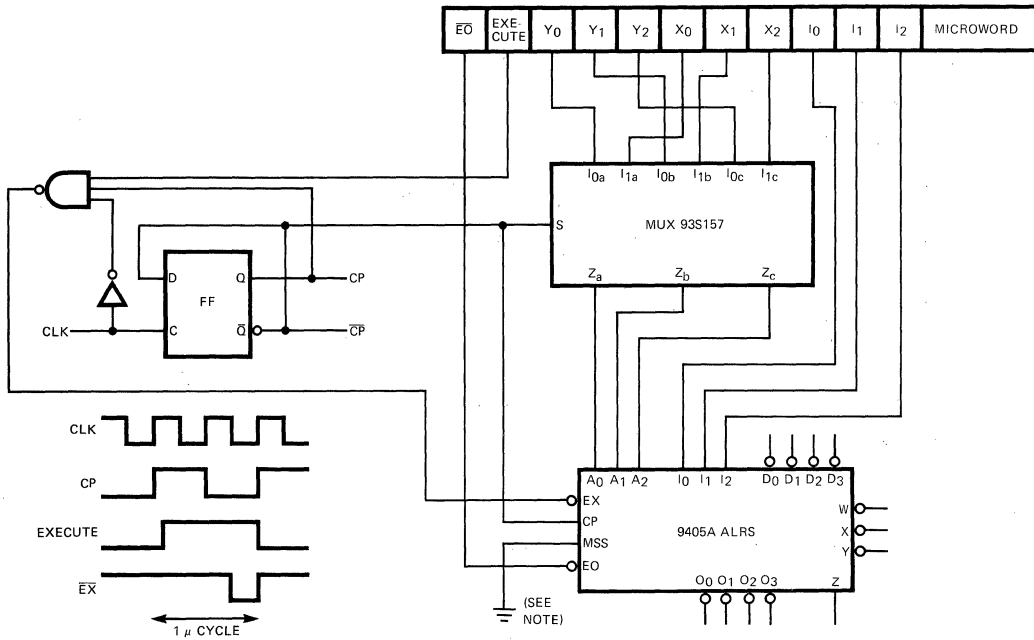
The CP input is used to clock the 9405A. The content of the specified RAM location is read into the output latches whenever the CP input is HIGH. These latches are disabled when the CP is LOW. Thus, the information that was presented when CP was HIGH will be stored in the latches. Writing of the ALU result occurs whenever the CP and $\overline{EX}$ inputs are LOW. If the CP or $\overline{EX}$ input becomes HIGH, writing into the RAM will be terminated and the result will be loaded into the Output Register on the transition.

Operation - The 9405A can be used in two modes: general register and accumulator. In the general register mode, one address (R_X) is used to select a register ($R_0 - R_7$) for the source operand and another address (R_Y) is used to select a register ($R_0 - R_7$) as the destination for the result. This is accomplished by changing the A-field during the negative half cycle of the clock. In the accumulator mode, a single address is used to select a register ($R_0 - R_7$) for the source operand and the result is loaded back into the same register (implied destination). This mode is achieved by keeping the A-field unchanged for the entire clock cycle. The following page describes these modes in more detail.

TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2	I_1	I_0	ACCUMULATOR MODE ($R_X = R_Y$)		GENERAL REGISTER MODE ($R_X \neq R_Y$)	
L	L	L	R_X *plus* $\overline{\text{D-Bus}}$ *plus* 1 → R_X	Accumulate and Increment	R_X *plus* $\overline{\text{D-Bus}}$ *plus* 1 → R_Y	Add with Carry
L	L	H	R_X *plus* $\overline{\text{D-Bus}}$ → R_X	Accumulate	R_X *plus* $\overline{\text{D-Bus}}$ → R_Y	Add
L	H	L	$R_X \cdot \overline{\text{D-Bus}}$ → R_X	Logical AND	$R_X \cdot \overline{\text{D-Bus}}$ → R_Y	Logical AND
L	H	H	$\overline{\text{D-Bus}}$ → R_X	Load	$\overline{\text{D-Bus}}$ → R_Y	Load
H	L	L	R_X → Output Register	Read	R_X → R_Y	Transfer
H	L	H	$R_X + \overline{\text{D-Bus}}$ → R_X	Logical OR	$R_X + \overline{\text{D-Bus}}$ → R_Y	Logical OR
H	H	L	$R_X \oplus \overline{\text{D-Bus}}$ → R_X	Exclusive OR	$R_X \oplus \overline{\text{D-Bus}}$ → R_Y	Exclusive OR
H	H	H	D-Bus → R_X	Load Complement	D-Bus → R_Y	Load Complement

NOTES:
1. R_X is the RAM location addressed by $A_0 - A_2$ when CP is HIGH.
2. R_Y is the RAM location addressed by $A_0 - A_2$ when CP is LOW.
3. The result of any operation is always loaded into the Output Register at the end of the cycle provided that $\overline{EX}$ is LOW.



NOTE: MSS is connected to V_{CC} for most significant slice, otherwise grounded.

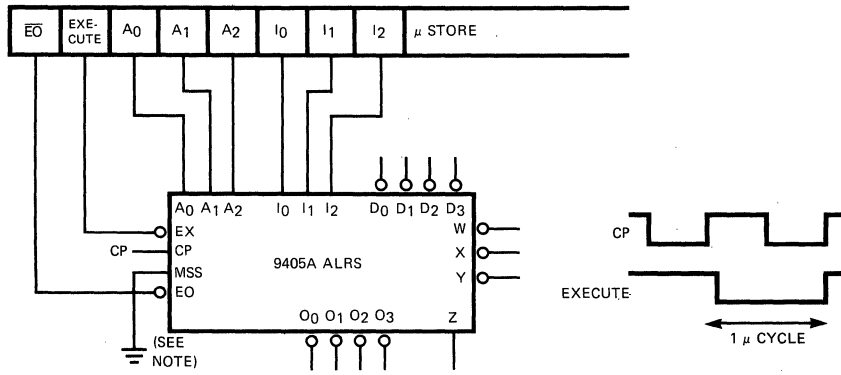
Fig. 1
GENERAL REGISTER MODE

3

General Register Mode – The general register mode of operation is depicted in *Figure 1*. A microcycle starts when the CP makes a LOW-to-HIGH transition. During the period when the clock is HIGH, data from the RAM is read into the latches. The A-field specifies the source register address for this operation. The latch outputs provide the source operand to the ALU. Inputs $\overline{D}_0$ – $\overline{D}_3$ are the second operand to the ALU. The ALU will generate the result of the selected operation specified by the I-field. When the CP goes LOW, the latches are disabled, thus the source operand is stored in the latches. Because the $\overline{EX}$ input is not LOW, writing into the RAM has not yet started. The A-field is changed to reflect the address of the destination register. When the $\overline{EX}$ goes LOW, writing into RAM is started and the output of the ALU will be written into the destination register. When the CP and/or $\overline{EX}$ goes HIGH, writing into the RAM will be terminated and the result will be loaded into the Output Register.

Switching the A-field is straightforward (see *Figure 1*). A quad 2-input multiplexer (93S157) is used to drive the A-field. One set of inputs (X_0 – X_2) to the multiplexer are the address bits corresponding to the source register address and the second set of inputs (Y_0 – Y_2) are the destination register address bits. The CP input for the 9405A is the output of a flip-flop connected in the complementing mode. The select input of the multiplexer is also controlled by the flip-flop output. The $\overline{EX}$ input to the 9405A is obtained by gating the clock signal with the flip-flop output.

Accumulator Mode – The accumulator mode of operation is shown in *Figure 2*. As before, a microcycle starts when the CP makes a LOW-to-HIGH transition. Data is read from the specified RAM location into the latches and applied to the ALU. The A-field inputs specify the address of the desired location. The ALU performs the operation specified by the I-field on D_0 – D_3 inputs and the latch outputs. When the CP goes LOW, the latches are disabled from tracking the RAM output. If the $\overline{EX}$ input and CP are LOW writing into the RAM is initiated. In the accumulator mode, the A-field remains unchanged and the result from the ALU will be written into the same location and loaded into the Output Register on the LOW-to-HIGH transition of CP provided that $\overline{EX}$ is LOW.



NOTE: MSS IS CONNECTED TO V_{CC} FOR MOST SIGNIFICANT SLICE, OTHERWISE GROUNDED.

NOTE: MSS is connected to V_{CC} for most significant slice, otherwise grounded.

Fig. 2
ACCUMULATOR MODE

EXPANSION – The 9405A is organized as a 4-bit slice and can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 9405A provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 9405As. When speed is not a prime consideration, it is also possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices to form a fixed word length array. The Z outputs are connected together through a load resistor to V_{CC} so that a HIGH indicates a "zero" result from an operation in the array.

Figure 3 shows a 16-bit array with ripple carry expansion using four 9405As. The MSS input is tied to V_{CC} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-field and I-field. A-field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry output (see block diagram). The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, the $\overline{W}$ output of a device assumes the state of its I_0 input. Thus, in *Figure 3*, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 inputs together to form the I-field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when external carry lookahead is used. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

The $\overline{X}$ output of device 4 is LOW if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP.

Figure 4 shows a 16-bit array with external carry lookahead expansion. Implementing the lookahead scheme requires the use of an external 93S42/74S182 in addition to the four 9405As in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs, together with the I_0 input of device 1, form the I-field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the 93S42/74S182 carry outputs (C_{n+x}, C_{n+y}, and C_{n+z} respectively). Also the $\overline{P}$ and $\overline{G}$ inputs of 93S42/74S182 are connected to $\overline{X}$ and $\overline{Y}$ outputs of the 9405As as shown. The control logic in the 9405A (see block diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs, as well as the Carry Generate and Carry Propagate

outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output reflects Carry Propagate and $\overline{Y}$ reflects Carry Generate outputs from that slice. For an arithmetic instruction the I_0 input is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ output of device 4 is the carry output from the array. Also, note that the I_0 input of device 1 is not only an instruction input but also provides the carry input to the array. The I_0 input of device 1 must be connected to the appropriate 93S42/74S182 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 9405A forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ outputs on all except the most significant slice. An examination of the 93S42/74S182 logic reveals that whenever $\overline{P}$ is LOW and $\overline{G}$ is HIGH the associated carry output is the same as the carry input. Thus, in *Figure 4* devices 2, 3, and 4 will assume the same logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions. This effectively connects I_0 through all four devices. As in the case of ripple expansion, $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent Negative and Overflow from the array.

Figures 3 and *4* both illustrate 16-bit arrays where the D-Bus ($\overline{D}_0 - \overline{D}_{15}$) represents the 16-bit input to the array, and the O-Bus ($\overline{O}_0 - \overline{O}_{15}$) represents the 16-bit 3-state output from the array. $\overline{D}_0$ and $\overline{O}_0$ represent the low order bits of the input and output respectively.

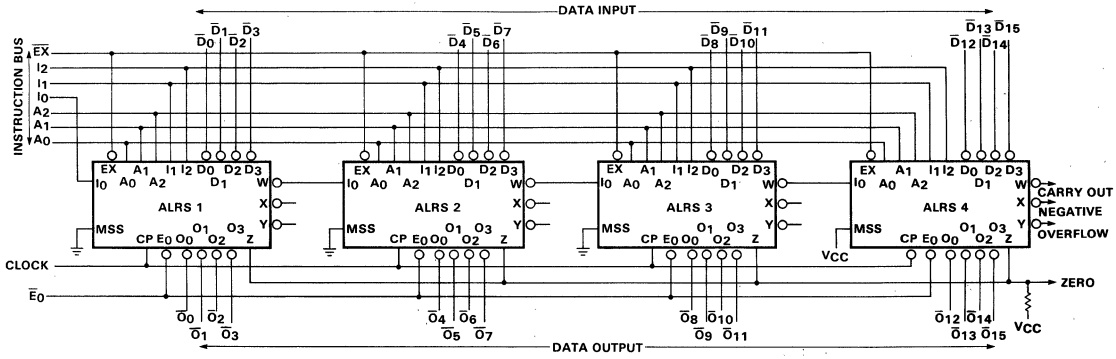


Fig. 3
RIPPLE CARRY EXPANSION

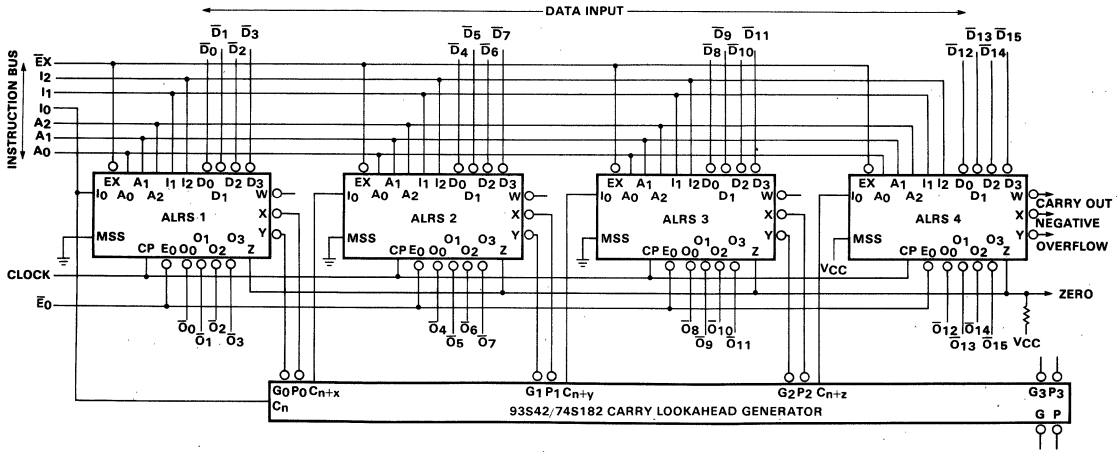


Fig. 4
CARRY LOOKAHEAD EXPANSION

3

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage $\overline{W}$, $\overline{X}$, $\overline{Y}$ Outputs	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage O_0, O_1, O_2, O_3	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
I_{OH}	Output HIGH Current Z Output				100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
V_{OL}	Output LOW Voltage $\overline{W}$, $\overline{X}$, Z	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage O_0, O_1, O_2, O_3, $\overline{Y}$	XM		0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
		XC		0.4	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			110	160	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Positive Going CP to O_0, O_1, O_2, O_3		18	25	ns	EO, EX LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		10	16	ns	I_1 or I_2 HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Data (D_0, D_1, D_2, D_3) to $\overline{W}$		30	40	ns	I_1 or I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, Data (D_0, D_1, D_2, D_3,)to $\overline{X}$, $\overline{Y}$		48	54	ns	MSS HIGH, I_1, I_2 LOW
			30	40	ns	MSS LOW, I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to $\overline{X}$, $\overline{Y}$		22	30	ns	MSS LOW
t_{PLH}, t_{PHL}	Propagation Delay, Data (D_0, D_1, D_2, D_3) to Z		48	60	ns	1 kΩ External Load Resistor to V_{CC}
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		16	22	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to $\overline{W}$		13	18	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, D_3 to $\overline{X}$		32	44	ns	I_1, I_2 HIGH, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to X, Y		42	58	ns	I_1, I_2 LOW, MSS LOW
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to X, Y		57	75	ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to X		53	70	ns	I_1, I_2 HIGH, MSS HIGH

AC CHARACTERISTICS (Cont'd): V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, See Fig. 3 and 5

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to W		44	60	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, Address (A_0, A_1, A_2) to Z		61	75	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to X, Y		39 28	55 55	ns ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to X, Y		30	40	ns	I_1, I_2 LOW, MSS HIGH
t_{PLH}, t_{PHL}	Propagation Delay, I_1, I_2 to Z		44	60	ns	I_1, I_2 LOW
t_{PLH}, t_{PHL}	Propagation Delay, I_0 to Z		30	40	ns	I_1, I_2 LOW
t_{PZH}, t_{PZL}	Enable Delay, EO to Outputs O_0, O_1, O_2, O_3		11	16	ns	
t_{PLZ}, t_{PHZ}	Disable Display, EO to O_0, O_1, O_2, O_3		10	16	ns	

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF,
See Fig. 5 for One Address Mode, Fig. 6 for Two Address Mode.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{CW}	Clock Period	75	50		ns	
t_{PWH}	Clock Pulse Width (HIGH)	35	23		ns	
t_{PWL}	Clock Pulse Width (LOW)	25	14		ns	
$t_s\overline{EX}_1$	Set-Up Time, Positive-Going $\overline{EX}$ to Negative-Going CP (Note 1)	0	–9		ns	
$t_s\overline{EX}_2$	Set-Up Time, Negative-Going $\overline{EX}$ to Positive-Going CP (Note 1)	15	10		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP	0			ns	
t_sA_1	Set-Up Time, A_0, A_1, A_2 to Negative-Going CP (Note 1) (Source Address)	35	22		ns	
t_sA_2	Set-Up Time, A_0, A_1, A_2 to Positive-Going CP (Note 1) (Source Address)	75	50		ns	
t_sA_2	Set-Up Time, A_0, A_1, A_2 to Negative-Going $\overline{EX}$ (Note 1) (Destination Address)	13	7		ns	
t_hA	Hold Time, A_0, A_1, A_2 to Positive-Going CP (Destination Address)	0			ns	
t_hA_1	Hold Time, A_0, A_1, A_2 to Negative-Going CP (Note 2) (Source Address)	0			ns	
t_hA_2	Hold Time, A_0, A_1, A_2 to Positive-Going CP (Note 2) (Destination Address)	0	–4		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive-Going CP	45	30		ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0$, $\overline{D}_1$, $\overline{D}_2$, $\overline{D}_3$ to Positive-Going CP	0	–10		ns	

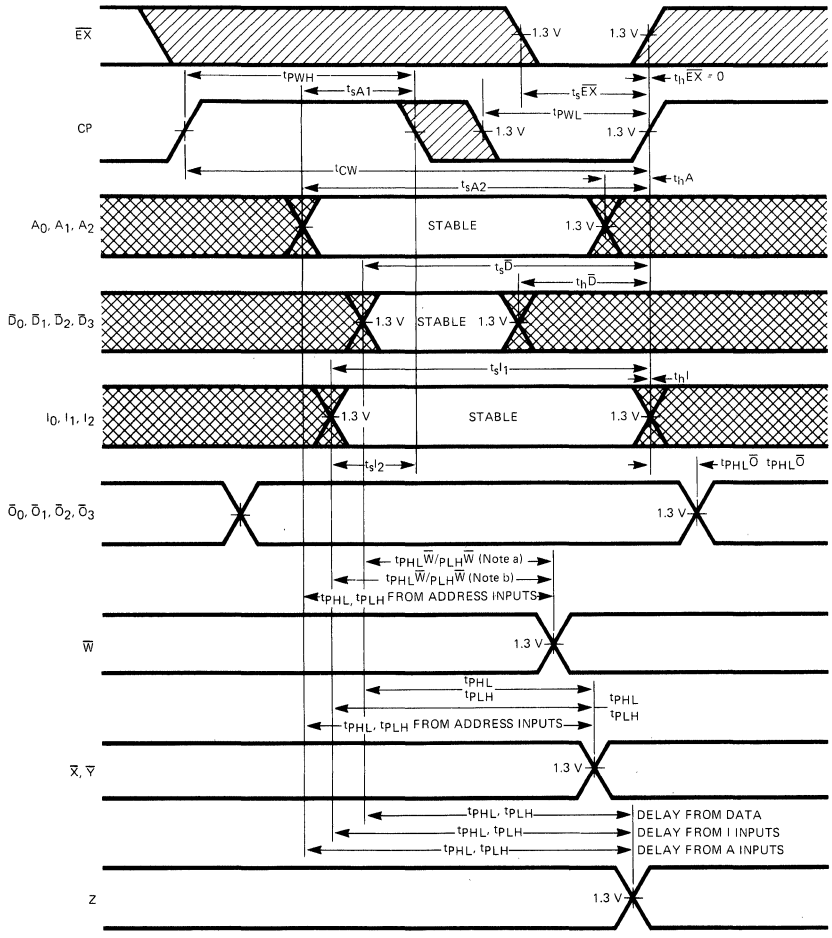
NOTES:
1. Both set-up times must be met.
2. Both hold times must be met.

3

INSTRUCTION SET-UP REQUIREMENTS: V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF,
See Fig. 4 for Multiple Slice Array Configuration

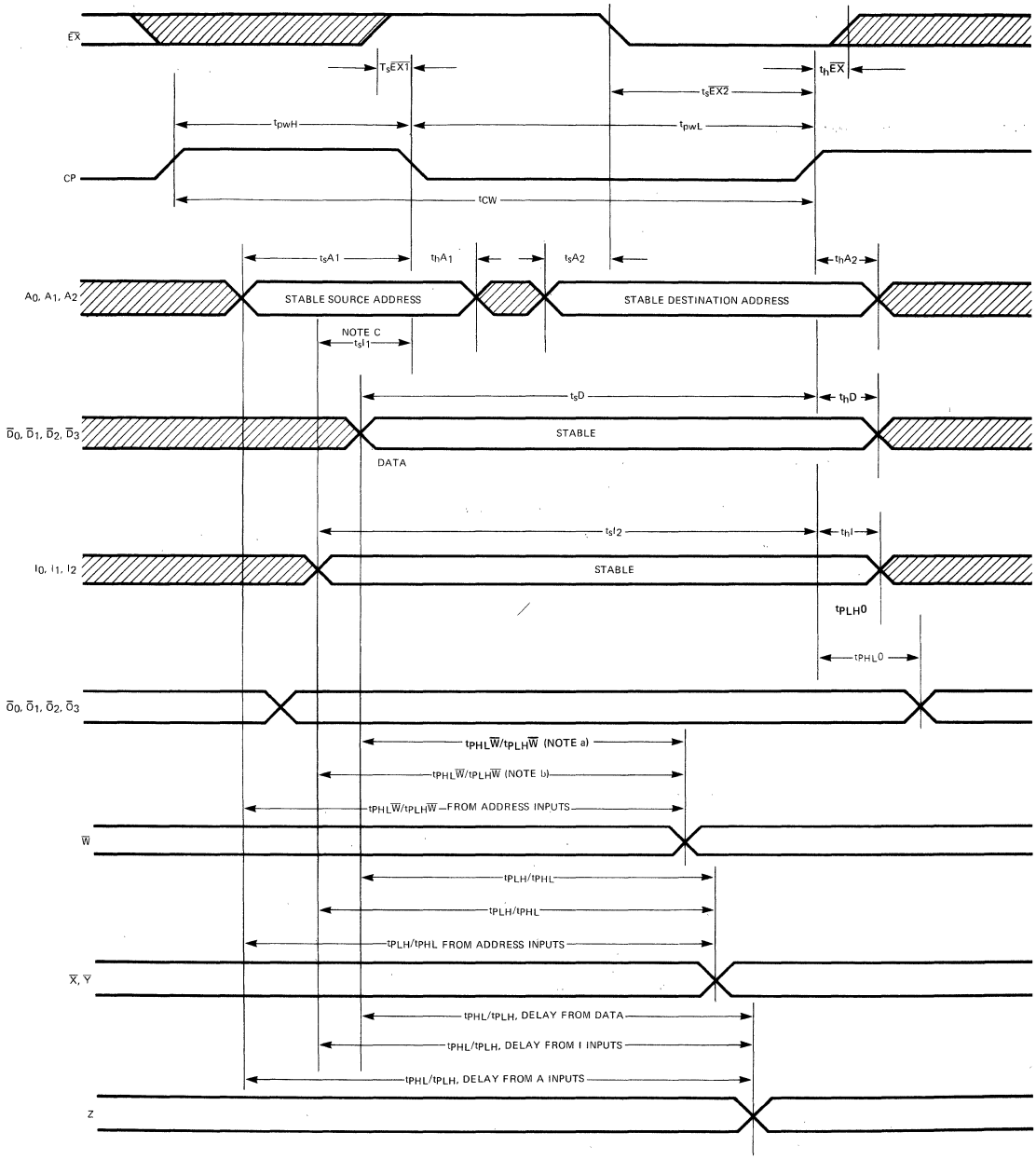
SYMBOL	PARAMETER	SINGLE SLICE			LEAST SIGNIFICANT SLICE OF MULTIPLE SLICE ARRAY			NON LEAST SIGNIFICANT SLICES			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_s I_1$	Set-Up Time, I_0, I_1, I_2 to Negative-Going Clock (Note 1)	8	4		8+$t_{(max)}$	4+$t_{(typ)}$		Note 2	Note 2		ns
$t_s I_2$	Set-Up Time, I_1, I_2 to Positive-Going Clock	40	25		40	25		40	25		ns
$t_s I_3$	Set-Up Time, I_0 to Positive-Going Clock	40	25		40	25		18	10		ns
$t_h I$	Hold Time, I_0, I_1, I_2 to Positive-Going Clock	0			0			0			ns

NOTE:
1. t = propagation delay of carry lookahead unit. i.e., t_{pd} C_{IN} to C_{n+x}. In the case of the 93S42/74S182, t_{max} = 11.5 ns and t_{typ} = 9.0 ns.
2. There is no $t_s I_1$ set-up requirement for non least significant slices. However, the set-up requirement for the least significant slice must be met.



NOTES:
a) Delay for logical operation (I_1 or I_2 HIGH)
b) Delay for arithmetic operation (I_1 = I_2 = LOW)

Fig. 5
ALRS TIMING DIAGRAM, SINGLE ADDRESS MODE



NOTES:
a. Delay for logical operation (I_1 or I_2 HIGH)
b. Delay for arithmetic operation ($I_1 = I_2$ = LOW)

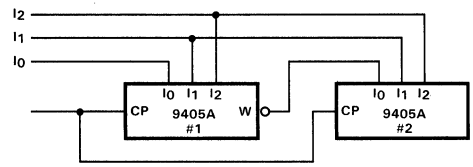
Fig. 6
ALRS TIMING DIAGRAM–TWO ADDRESS MODE

3

AC CHARACTERISTICS: MULTIPLE SLICE OPERATION

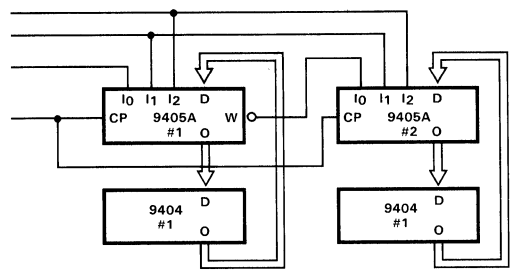
A single 9405A slice operating without overhead is guaranteed to operate at 13.3 MHz (75 ns). Such a configuration, however, would be extremely rare. AC guarantees for multiple slice operation depend on the configuration actually used. Several examples follow.

8-bit Machine with Ripple Carry



DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9405A inputs		
t_{pd}-Address to $\overline{W}$ of 9405A # 1 ($\overline{W}$ is the carry-out pin)	44 ns	60 ns
t_{pd}-9405A # 2, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	74 ns	100 ns
Frequency	13.5 MHz	10 MHz

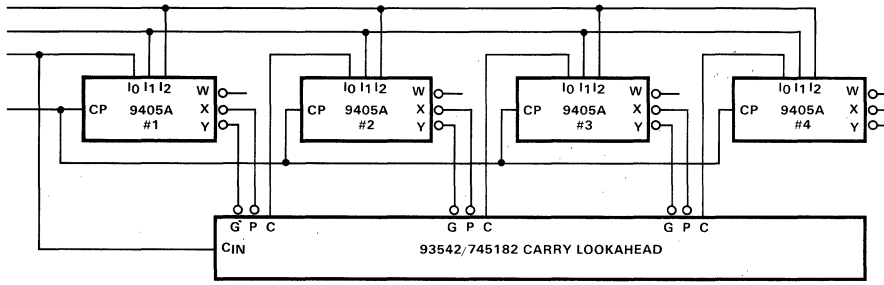
8-bit Machine with Ripple Carry and DPS in Data Path (Note 2)



DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs		
t_{pd}-Rising edge of clock to $\overline{O}$ outputs of 9405A # 1	18 ns	25 ns
t_{pd}-9404 # 1, $\overline{D}$ inputs to 9404 #1, O outputs (See 9404 data sheet)	15 ns	25 ns
t_{pd}-9405A # 1, $\overline{D}$ inputs to $\overline{W}$ ($\overline{W}$ is the carry-out pin)	30 ns	40 ns
t_{pd}-9405A # 2, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	93 ns	130 ns
Frequency	10.7 MHz	7.7 MHz

Notes on following pages.

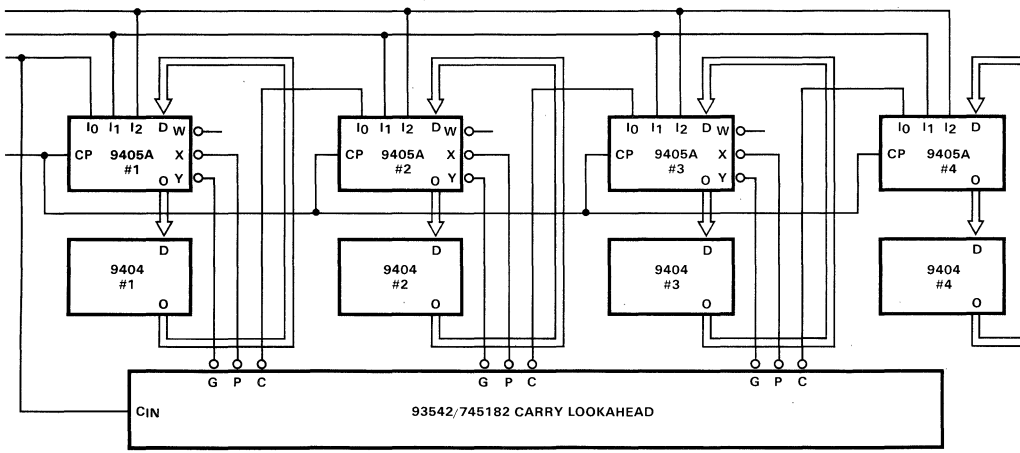
16-bit Machine with Carry Lookahead



DESCRIPTION	TYP	MAX
Assume that at time, t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs		
t_{pd}-Address inputs to $\overline{X}$, $\overline{Y}$ outputs of 9405A # 1	42 ns	58 ns
t_{pd}-G and P inputs of carry lookahead (Note: All G and P outputs are generated simultaneously. Therefore, 9405A # 2, # 3, # 4 set-up simultaneously.)	5 ns	7 ns
t_{pd}-9405A # 4, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	77 ns	105 ns
Frequency	13 MHz	9.5 MHz

3

16-bit Machine with Carry Lookahead and DPS in Data Path (Note 3)



Notes on following pages.

16-bit Machine with Carry Lookahead and DPS in Data Path (Cont'd)

DESCRIPTION	TYP	MAX
Assume that at t = 0, the clock goes HIGH and the instruction and address information appear at the 9404 and 9405A inputs.		
t_{pd}-Rising edge of clock to $\overline{O}$ output of 9405A # 1	18 ns	25 ns
t_{pd}-9404 # 1, $\overline{D}$ inputs to $\overline{O}$ outputs	15 ns	25 ns
t_{pd}-9405A # 1, $\overline{D}$ inputs to $\overline{X}$, $\overline{Y}$ outputs (X, Y are carry propagate and generate)	30 ns	40 ns
t_{pd}-Carry propagate and generate inputs of carry lookahead to carry out. (Note that all carry outs are generated simultaneously.)	5 ns	7 ns
t_{pd}-9405A # 4, I_0 to Status Flags (See Note 1)	30 ns	40 ns
Total clock period required	98 ns	137 ns
Frequency	10 MHz	7.3 MHz

Architectures with Finite Delay between Rising Clock and the Appearance of Instructions and Address Information

Consider the previous case (16-bit with carry lookahead and DPS). After the clock rises, 25 ns is required before data appears at the input of the 9404. During this 25 ns there is no need for instruction or address information. Therefore, so long as the address and instructions appear within this 25 ns, no time is lost. Consequently, a pipeline system where the propagation delay of the pipeline register is less than 25 ns will operate at the speed guaranteed for the data path alone; *i.e.*, 7.3 MHz guaranteed for a 16-bit machine employing carry lookahead, 9404s in the data path, and a pipeline register with propagation delay less than 25 ns.

NOTES:
1. The 9405s could actually respond to a rising clock after the 18 ns (the I_0 to rising clock set-up time max). However, the status flags are not available until 40 ns have elapsed.
2. In this configuration, carry out for 9405A # 1 cannot be generated until the D inputs are present. These originate from the 9405A # 1 output register and must pass through 9404 # 1 before reaching the 9405A # 1 inputs.
3. In this configuration, carry propagate and generate outputs from 9405A # 1 cannot be generated until the D inputs are present. These originate from 9405A # 1 outputs register and must pass through 9404 # 1 before reaching the 9405A # 1 inputs.

9406
PROGRAM STACK
FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9406 is a 16-word by 4-bit "push-down pop-up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 9406 executes 4 instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, PC is in the top location of the stack. As a new PC value is "pushed" into the stack (Call operation), all previous PC values effectively move down one level. The top location of the stack is the current PC. Up to 16 new Program Counter values can be stored, which gives the 9406 a 15 level nesting capability. "Popping" the stack (Return operation) brings the most recent PC to the top of the stack. The remaining two instructions affect only the top location of the stack. In the Branch operation a new PC value is loaded into the top location of the stack from the $\overline{D}_0 - \overline{D}_3$ Inputs. In the Fetch operation, the contents of the top stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 9406 may be expanded to any word length without additional logic. 3-state output drivers are provided on the 4-bit address outputs ($X_0 - X_3$) and data outputs ($\overline{O}_0 - \overline{O}_3$); the X-Bus outputs are enabled internally during the Fetch instruction while the O-Bus outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 9406 is fully compatible with all TTL families.

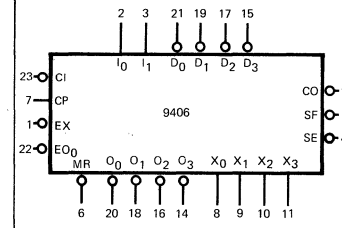
- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **10 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADS FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **SLIM 24-PIN PACKAGE**
- **3-STATE OUTPUTS**

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	1.0 U.L.	0.23 U.L.
I_0, I_1	Instruction Inputs	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
CP	Clock Input	1.0 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}_0$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{O}_0 - \overline{O}_3$	Output Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{CO}$	Carry Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SF}$	Stack Full Output (Active LOW) (Note b)	10 U.L.	5 U.L.
$\overline{SE}$	Stack Empty Output (Active LOW) (Note b)	10 U.L.	5 U.L.

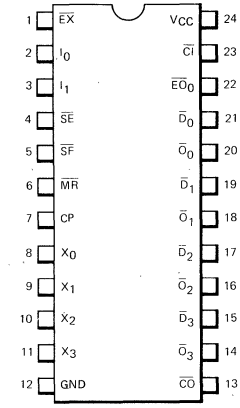
NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output fan-out with $V_{OL} \leq 0.5$ V.

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

3

BLOCK DIAGRAM

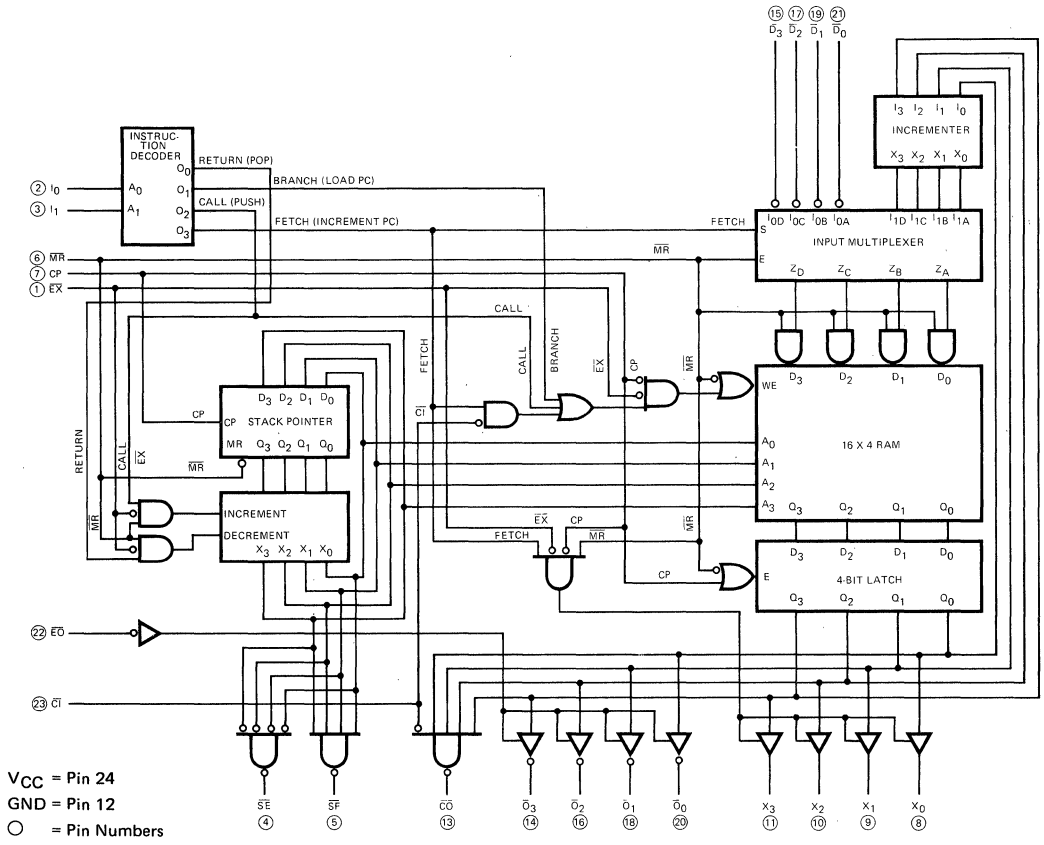


TABLE 1
INSTRUCTION SET FOR THE 9406

I_1 I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH EO_0 LOW)
L L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L H	Branch (Load PC)	Load D-Bus into Current Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H L	Call (Push)	Increment Stack Pointer and Load D-Bus into New Program Counter Location	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Figure 9 for details.
H H	Fetch (Increment PC)	Increment Current Program Counter if $\overline{CI}$ is LOW	Current Program Counter while both CP and $\overline{EX}$ are LOW, disabled while CP or $\overline{EX}$ is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level L = LOW Level

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 9406 consists of an Input Multiplexer, a 16 X 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 9406 is organized around three 4-bit busses; the input data bus ($\overline{D}_0 - \overline{D}_3$), output data bus ($\overline{O}_0 - \overline{O}_3$) and the address bus ($X_0 - X_3$). The 9406 implements four instructions as determined by Inputs I_0 and I_1 (see *Table 1*). The O-Bus is derived from the RAM output latches and enabled by a LOW on the Output Enable ($\overline{EO}_0$) input. The X-Bus is also derived from the output latches; it is enabled internally during the Fetch instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) inputs.

Fetch Operation - The Fetch operation places the content of the current Program Counter (PC) on the X-Bus. If the Carry In (CI) is LOW, the current PC is incremented in preparation for the next Fetch. If CI is HIGH, the value of the current PC is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The Execute ($\overline{EX}$) is normally LOW at this time. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the Input Multiplexer. The current PC value is loaded into the latches and is available on the O-Bus if $\overline{EO}_0$ is LOW. When CP is LOW the latches are disabled from following the RAM output, when both CP and $\overline{EX}$ are LOW, buffers are enabled, applying the current PC to the X-Bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out ($\overline{CO}$) is LOW when the content of the current PC is at its maximum, i.e., all ones and the Carry In ($\overline{CI}$) is LOW. When CP or $\overline{EX}$ goes HIGH, writing into the RAM is inhibited and the address buffers ($X_0 - X_3$) are disabled.

Branch Operation – During a Branch operation, the data inputs ($\overline{D}_0 - \overline{D}_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. The Stack Pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into the current PC. The X-Bus drivers are not enabled during a Branch operation.

Call Operation - During a Call operation the content of the data bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the Stack Pointer value thus incrementing the RAM address. Since the output latches go to the nontransparent or store mode when CP is LOW, the O-Bus outputs will reflect the RAM output at the CP negative-going transition. If EX goes LOW considerably before CP goes LOW, the O-Bus will correspond to the previous contents of the incremented RAM address after CP goes LOW. If CP goes LOW a very short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

When CP is LOW (assuming $\overline{EX}$ is LOW) the D-Bus inputs are written into this new RAM location. On the LOW-to-HIGH transition of CP, the incremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs reflect the newly entered data. When the RAM address is "1111" the Stack Full output ($\overline{SF}$) is LOW, indicating that no further Call operations should be initiated. If an additional Call operation is performed SP is incremented to (0000), the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-Bus drivers are not enabled during a Call operation.

Return Operation – During the Return operation the previous PC is "popped" to become the current PC.

The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the Stack Pointer value, thus decrementing the RAM address. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the new value after $\overline{EX}$ goes LOW. If CP goes LOW a short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW-to-HIGH transition of CP.

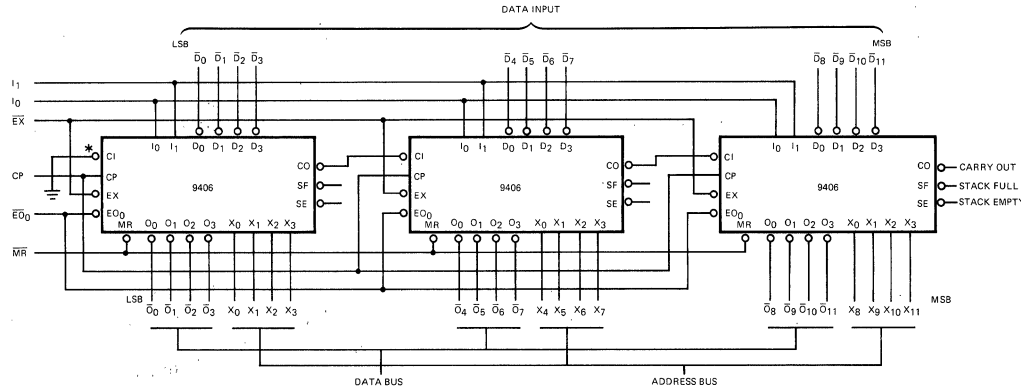
On the LOW-to-HIGH transition of CP the decremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs correspond to the new "popped" value.

The X-Bus drivers are not enabled during a Return operation. When the RAM address is "0000", the Stack Empty output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full output ($\overline{SF}$) will go LOW. A LOW on the Master Reset ($\overline{MR}$) causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

EXPANSION – The 9406 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in *Figure 1.* Carry In ($\overline{CI}$) and Carry Out ($\overline{CO}$) are connected to provide automatic increment of the current program counter during Fetch. The $\overline{CI}$ input of the least significant 9406 is tied LOW to ground.

If automatic increment during Fetch is not desired, the $\overline{CI}$ input of the least significant 9406 is held HIGH.

3



*Tie to V_{CC} to disable automatic increment.

Fig. 1
16 BY 12 PROGRAM STACK

DC CHARACTERISTICS OVER OPERATION TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
	$\overline{CO}$, $\overline{SE}$, $\overline{SF}$	XC	2.4	3.4			
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
	$X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$	XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
V_{OL}	Output LOW Voltage			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
	$\overline{CO}$, $\overline{SE}$, $\overline{SF}$			0.35	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage			0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
	$X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$			0.35	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CCH}	Supply Current			100	160	mA	V_{CC} = MAX

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25° C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS – ALL MODES OF OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
t_{CW}	Clock Period	100	70		ns	
t_{PWH}	Clock Pulse Width (HIGH)	60	40		ns	
t_{PWL}	Clock Pulse Width (LOW)	40	25		ns	
$t_s\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP		0		ns	
$t_h\overline{EX}$	Hold Time, $\overline{EX}$ to CP		0		ns	Figure 2
t_sI	Set-Up Time, I_0, I_1 to Negative-Going Clock		20		ns	
t_hI	Hold Time, I_0, I_1 to Positive-Going Clock		0		ns	
$t_s\overline{CI}$	Set-Up Time, $\overline{CI}$ to Negative-Going Clock		5		ns	
$t_h\overline{CI}$	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0$–$\overline{D}_3$ to Positive-Going Clock		20		ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0$ – $\overline{D}_3$ to Positive-Going Clock		0		ns	
$t_{PWL}\overline{MR}$	$\overline{MR}$ Pulse Width (LOW)	40	25		ns	Figure 3
t_{rec}	$\overline{MR}$ to Negative-Going Clock	45	30		ns	

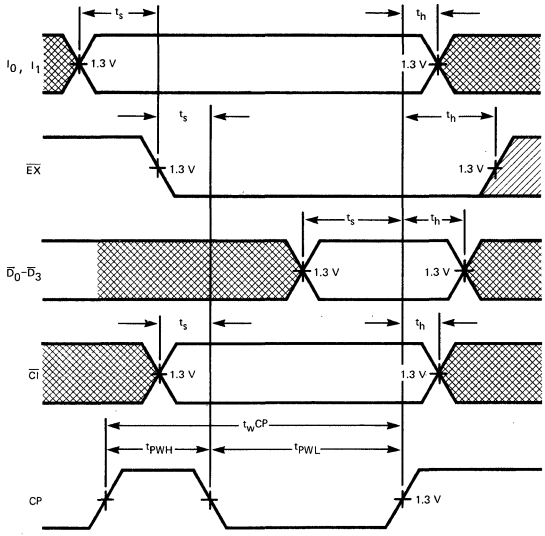


Fig. 2
WAVEFORMS FOR ALL OPERATIONS

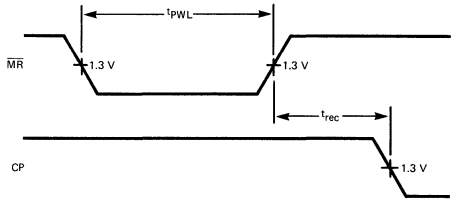


Fig. 3
RESET OPERATION

Refer to individual timing diagrams for each operation to determine output response.

AC CHARACTERISTICS - FETCH OPERATION: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Carry In ($\overline{CI}$) to Carry Out ($\overline{CO}$)		11 7	16 12	ns	Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Carry Out ($\overline{CO}$)		28 46	41 66	ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Carry Out ($\overline{CO}$)		34 38	45 60	ns	Figure 6

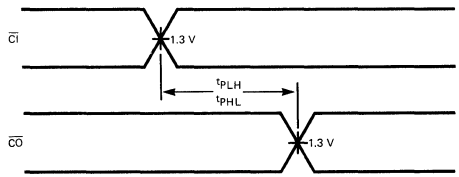


Fig. 4
CARRY-IN TO CARRY-OUT

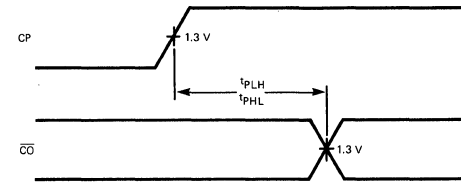


Fig. 5
CLOCK TO CARRY-OUT

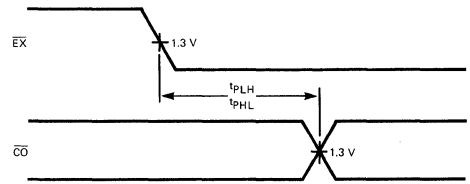


Fig. 6
EXECUTE TO CARRY-OUT

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - BRANCH (LOAD PC) OPERATION:
V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to Outputs ($\overline{O}_0 - \overline{O}_3$)		28 45	41 66	ns	$\overline{EO}_0$ LOW Figures 7 and 8
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$	30	20		ns	
t_h	Hold Time I_0, I_1 to Positive-Going $\overline{EX}$	0	0		ns	$\overline{EX}$ goes HIGH before CP, Figure 8
t_h	Hold Time, I_0, I_1 to Positive-Going CP	0	0		ns	CP goes HIGH before $\overline{EX}$, Figure 7
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	25	16		ns	Figures 7 and 8
t_h	Hold Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	0	0		ns	
t_{PWL}	$\overline{EX}$ Pulse Width	45	30		ns	$\overline{EX}$ Goes HIGH Before CP, Figure 8

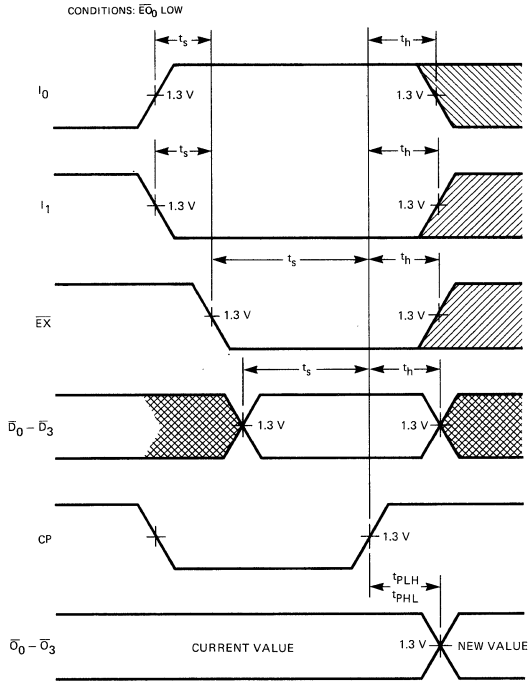


Fig. 7
BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

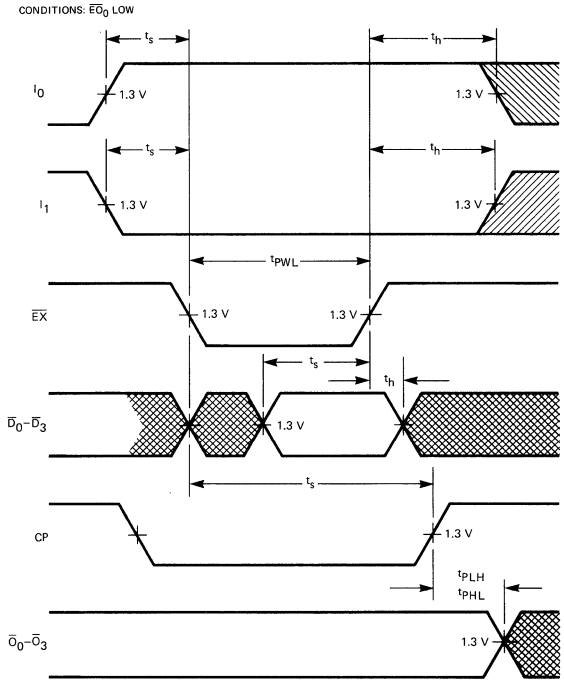


Fig. 8
BRANCH OPERATION, $\overline{EX}$ GOES HIGH BEFORE CP

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - CALL (PUSH) OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 9)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		25 75	40 130	ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to Intermediate Value of $\overline{O}_0 - \overline{O}_3$		22 64	35 85	ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		18 43	28 59	ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1	30	20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1	0			ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees Intermediate Data on $\overline{O}_0 - \overline{O}_3$ while CP is LOW	65	45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees no Change in $\overline{O}_0 - \overline{O}_3$ While CP is LOW	0			ns	
$t_h\overline{EX}$	Hold Time, Positive-Going CP to Positive-Going $\overline{EX}$	0			ns	
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$ to Positive-Going CP	30	20		ns	
t_h	Hold Time, Positive-Going CP to $\overline{D}_0 - \overline{D}_3$	0			ns	

3

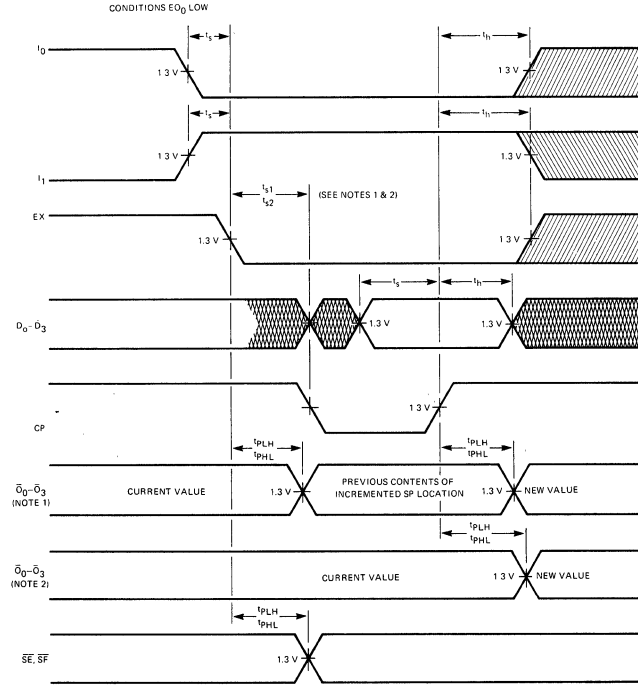


Fig. 9
CALL (PUSH) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW ($t_{s2}\overline{EX}$ is met).

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - RETURN (POP) OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF (Figure 10)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to New Value of $\overline{O}_0 - \overline{O}_3$		25 103	40 130	ns	$\overline{EO}_0$ LOW
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to New Value of $\overline{O}_0 - \overline{O}_3$		23 101	40 130	ns	$\overline{EO}_0$ LOW, Set-Up Requirements $t_{s1}\overline{EX}$ must be met
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{EX}$ to $\overline{SE}$, $\overline{SF}$		18 43	28 59	ns	
t_s	Set-Up Time, Negative-Going $\overline{EX}$ to I_0, I_1	30	20		ns	
t_h	Hold Time, Positive-Going CP to I_0, I_1	0			ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP which Guarantees the New Value on $\overline{O}_0 - \overline{O}_3$ While CP is LOW	65	45		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to Negative-Going CP. Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ must be met for Proper Operation	0			ns	
$t_{s3}\overline{EX}$	Set-Up Time, EX to Positive-Going CP. Either $t_{s3}\overline{EX}$ or $t_{s2}\overline{EX}$ (Above) must be met for Proper Operation.	45	30		ns	

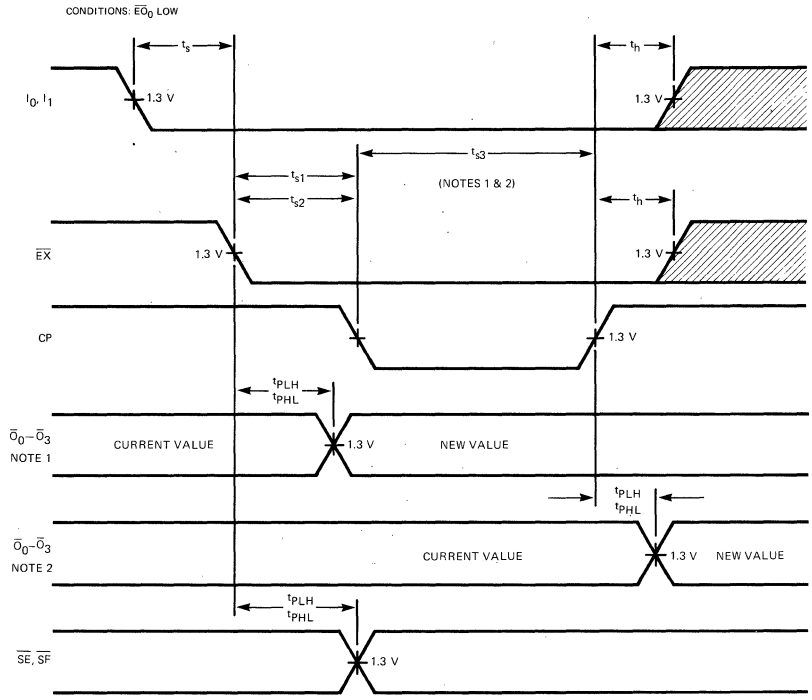


Fig. 10
RETURN (POP) OPERATION

NOTES:
1. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($t_{s1}\overline{EX}$ is met).
2. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (either $t_{s2}EX$ or $t_{s3}\overline{EX}$ are met).

3

AC CHARACTERISTICS AND SET-UP REQUIREMENTS - FETCH OPERATION:

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay Positive-Going CP to Incremented Value of $\overline{O}_0 - \overline{O}_3$		22 59	30 80	ns	$\overline{EO}_0$, $\overline{CI}$ LOW, Figures 13 and 14
t_{PZL} t_{PZH}	Turn-On Delay, from CP or $\overline{EX}$ Whichever goes LOW last to $X_0 - X_3$		13 12	18 17	ns	$\overline{EO}_X$ LOW, Figures 11, 12, 13 and 14
t_{PLZ} t_{PHZ}	Delay Going into HIGH Impedance State		7 10	12 16	ns	
t_s	Set-Up Time, I_0, I_1 to Negative-Going $\overline{EX}$	30	20		ns	Figures 11, 12, 13 and 14
t_h	Hold Time , I_0, I_1 to CP or $\overline{EX}$ whichever goes HIGH first	0			ns	
t_s	Set-Up Time, Negative Going $\overline{EX}$ to Positive-Going CP	40	25		ns	
t_s	Negative-Going $\overline{CI}$ to Positive-Going CP	30	20		ns	Fetch with Increment, Figures 13 and 14
t_h	Positive-Going $\overline{CI}$ to Negative-Going $\overline{EX}$	0				Iterative Fetch, Figures 11 and 12

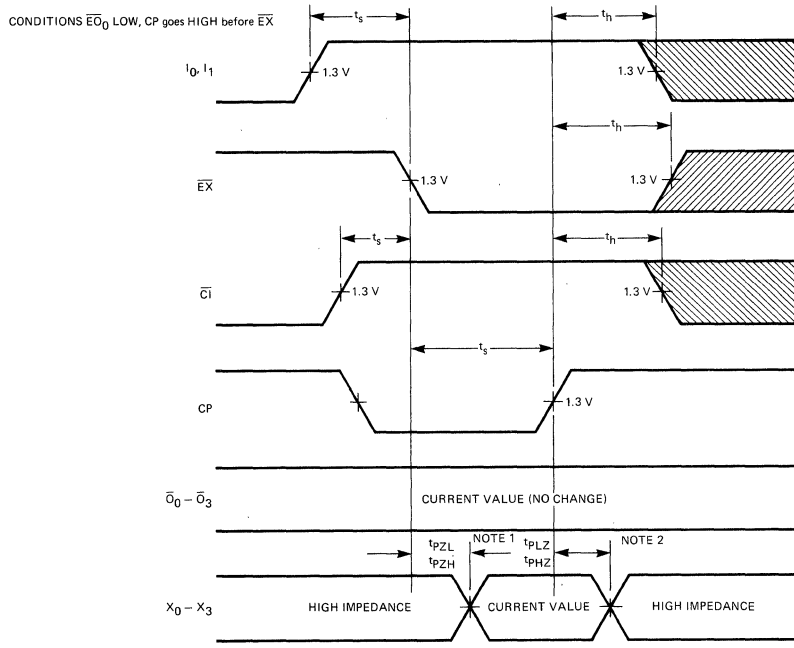


Fig. 11
ITERATIVE FETCH

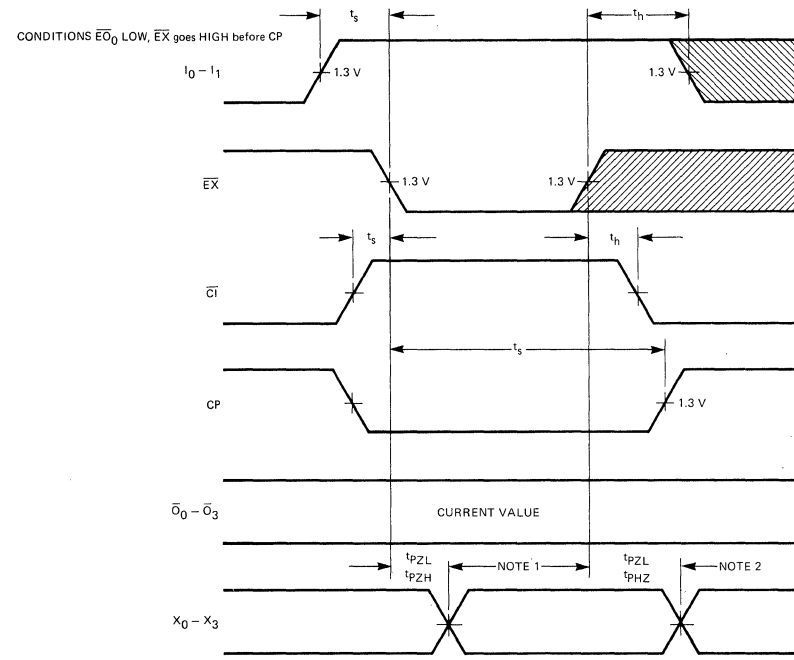


Fig. 12
ITERATIVE FETCH

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

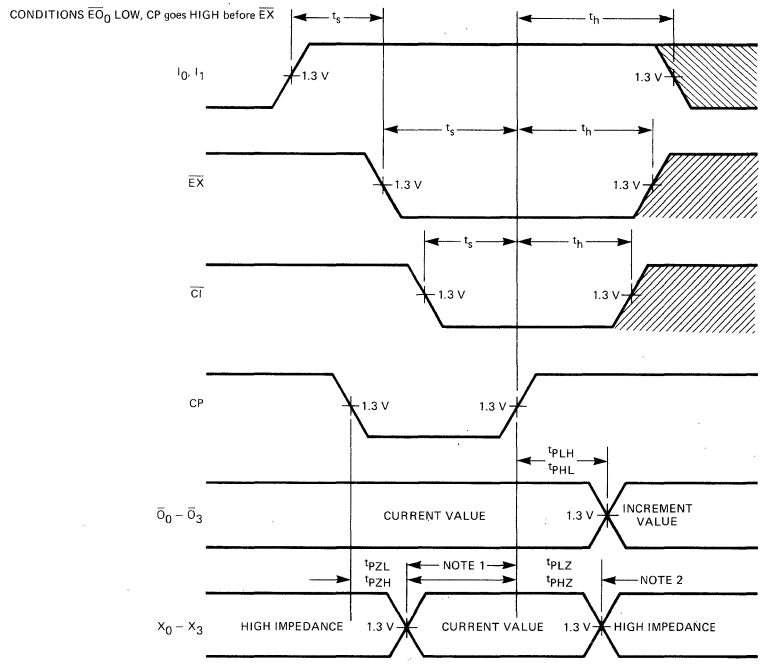


Fig. 13
FETCH WITH INCREMENT PC

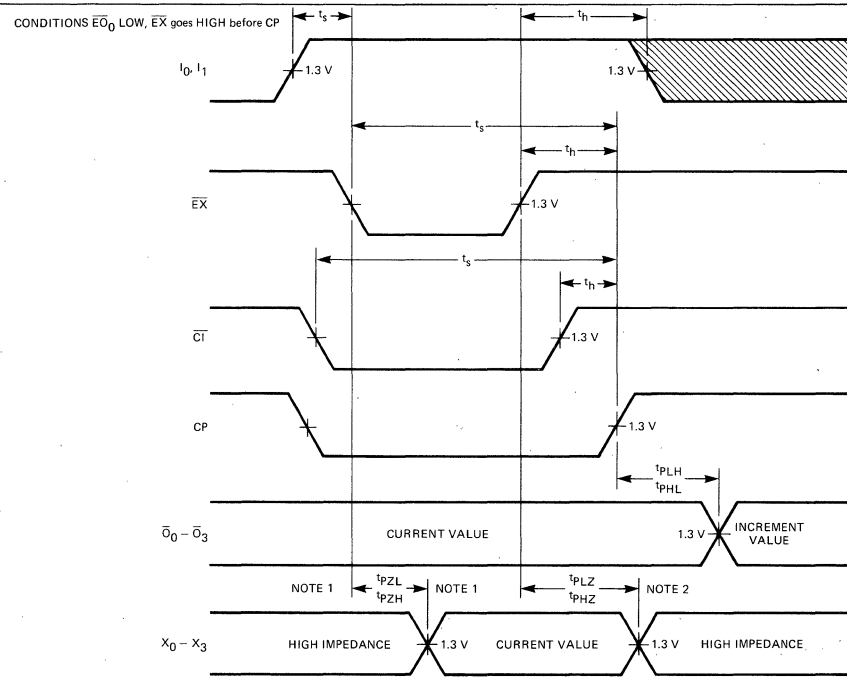


Fig. 14
FETCH OPERATION WITH INCREMENT PC

NOTES:
1. $X_0 - X_3$ Turn-On Delay measured from the time both $\overline{EX}$ and CP go LOW.
2. $X_0 - X_3$ Turn-Off Delay measured from the time either $\overline{EX}$ or CP goes HIGH.

3

9407

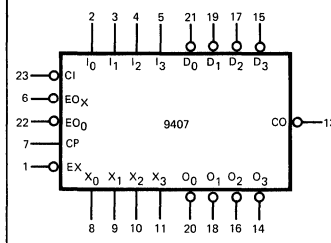
DATA ACCESS REGISTER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION – The 9407 Data Access Register (DAR) is designed to perform the memory address functions for RAM resident stack applications. The DAR can implement general registers with an adder network in programmable digital systems. The 9407 contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1) and Operand Address (R_2). It implements 16 instructions (see *Table 1*) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 10 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The 9407 is fully compatible with all TTL families.

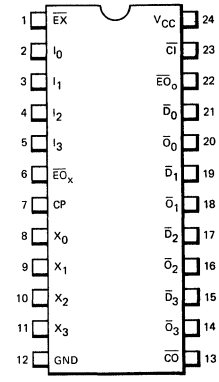
- **HIGH SPEED – 10 MHz MICROINSTRUCTION RATE**
- **THREE 4-BIT REGISTERS**
- **16 INSTRUCTIONS FOR REGISTER MANIPULATION**
- **TWO SEPARATE OUTPUT PORTS, ONE TRANSPARENT**
- **RELATIVE ADDRESSING CAPABILITY**
- **3-STATE OUTPUTS**
- **OPTIONAL PRE OR POST ARITHMETIC**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



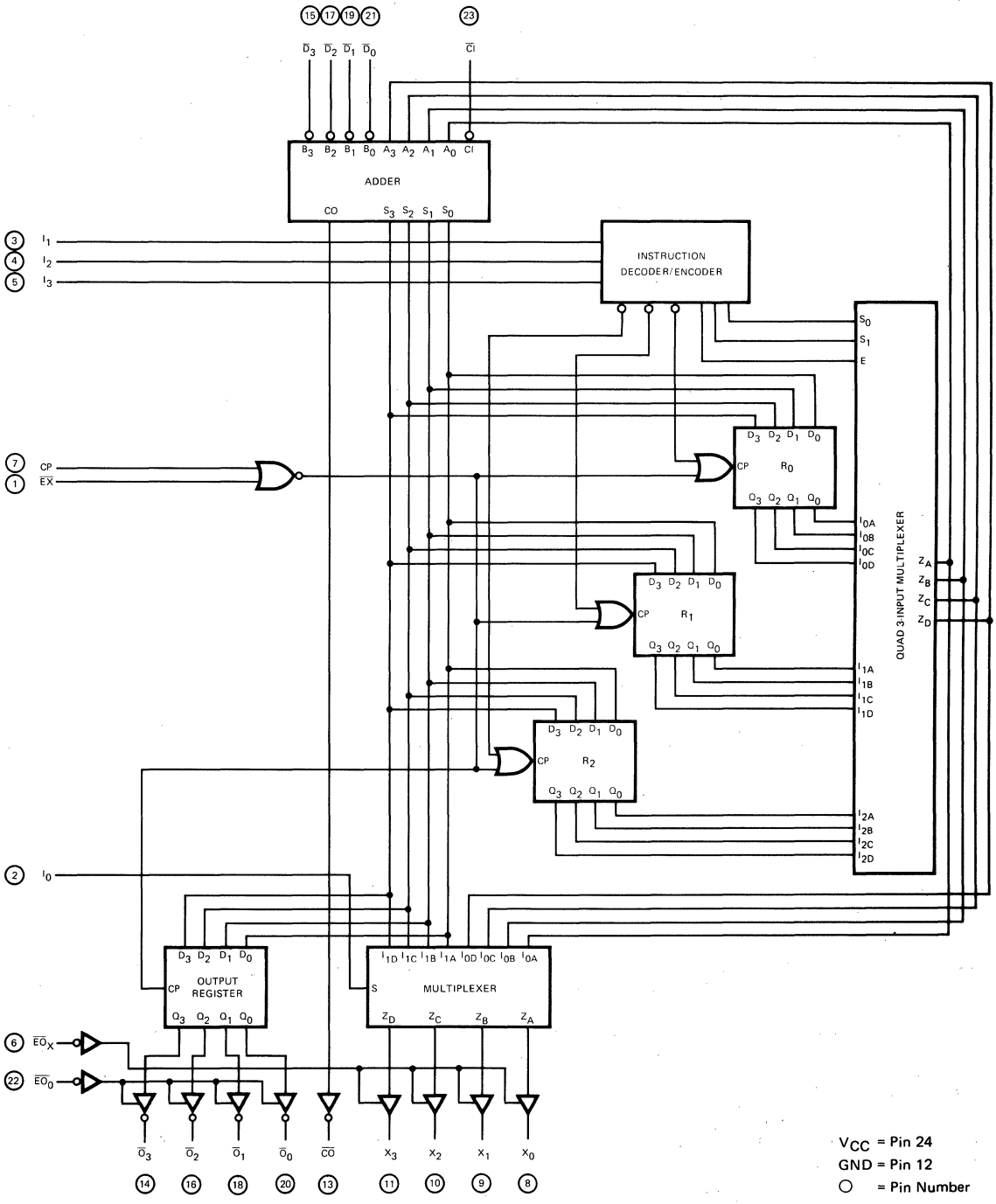
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)	1.0 U.L.	0.23 U.L.
$I_0 - I_3$	Instruction Word Inputs	1.0 U.L.	0.23 U.L.
$\overline{CI}$	Carry Input (Active LOW) (Note b)	1.0 U.L.	0.23 U.L.
$\overline{CO}$	Carry Output (Active LOW)	10 U.L.	5 U.L.
CP	Clock Input (L → H Edge-Triggered)	1.0 U.L.	0.23 U.L.
$\overline{EX}$	Execute Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}_X$	Address Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}_0$	Data Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$X_0 - X_3$	Address Outputs (Note b)	130 U.L.	10 U.L.
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active LOW) (Note b)	130 U.L.	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. Output Current measured at V_{OUT} = 0.5 V.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 9407 contains a 4-bit slice of three registers (R_0–R_2), a 4-Bit Adder, 3-state address output buffers (X_0–X_3) and a separate Output Register with 3-state buffers ($\overline{O}_0$–$\overline{O}_3$), allowing output of the register contents on the data bus (refer to the block diagram). The DAR performs 16 instructions, selected by I_0–I_3 inputs, as listed in *Table 1.*

Operation – For normal operation $\overline{EX}$ is brought LOW while CP is HIGH. A microcycle starts as the clock goes HIGH. Data inputs $\overline{D}_0$–$\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines (I_1,I_2,I_3) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH transition of the CP input writes the result from the Adder into a register (R_0–R_2) and into the Output Register provided $\overline{EX}$ is LOW. If the I_0 input is HIGH, the multiplexer routes the result from the Adder to the 3-state buffer controlling the address bus (X_0–X_3) independent of $\overline{EX}$ and CP. If I_0 is LOW, the multiplexer routes the output of the selected register directly into the 3-state buffer controlling the address bus (X_0–X_3), independent of $\overline{EX}$ and CP.

TABLE 1
INSTRUCTION SET FOR THE 9407

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$→R_0 and Output Register
L	L	L	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	L	H	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$→R_1 and Output Register
L	L	H	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	H	L	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$→R_2 and Output Register
L	H	L	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	H	H	L	R_1	R_1 *plus* $\overline{D}$ *plus* $\overline{CI}$→R_1 and Output Register
L	H	H	H	R_1 *plus* $\overline{D}$ *plus* $\overline{CI}$	
H	L	L	L	R_2	$\overline{D}$ *plus* $\overline{CI}$→R_2 and Output Register
H	L	L	H	$\overline{D}$ *plus* $\overline{CI}$	
H	L	H	L	R_0	$\overline{D}$ *plus* $\overline{CI}$→R_0 and Output Register
H	L	H	H	$\overline{D}$ *plus* $\overline{CI}$	
H	H	L	L	R_2	R_2 *plus* $\overline{D}$ *plus* $\overline{CI}$→R_2 and Output Register
H	H	L	H	R_2 *plus* $\overline{D}$ *plus* $\overline{CI}$	
H	H	H	L	R_1	$\overline{D}$ *plus* $\overline{CI}$→R_1 and Output Register
H	H	H	H	$\overline{D}$ *plus* $\overline{CI}$	

L = LOW Level
H = HIGH Level

9407 EXPANSION – The 9407 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – The 9407 is organized as a 4-bit register slice. The $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths. *Figure 1* is a block diagram of a typical application. Each block of the Macrologic parts represents four identical slices, thus creating a 16-bit array. For this application the register utilizations in the DAR may be as follows:
R_0 is the program counter (PC), R_1 is the Stack Pointer (SP) for memory resident stack and R_2 contains the operand address. For an instruction fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for calculation, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

A different type of application using the DAR is shown in *Figure 2.* Four 9407s are used here as the major elements in a data path loop closed by four 9404s (DPS). This data path can be used for dedicated multiply/divide function. The DAR register utilization in this application can be as follows :

R_0 is the multiplicand in case of multiply or the divisor in case of divide;
R_1 is the temporary result in case of multiply or the dividand/quotient in case of divide;
R_2 is the product in case of multiply or a temporary register in case of divide.

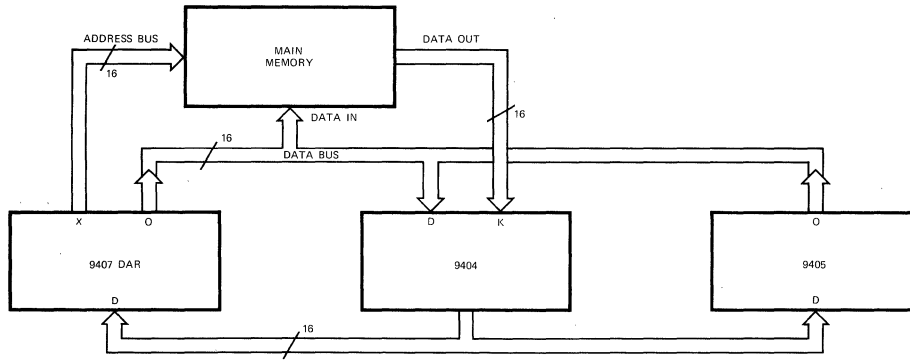


Fig. 1
TYPICAL MEMORY ADDRESS APPLICATION

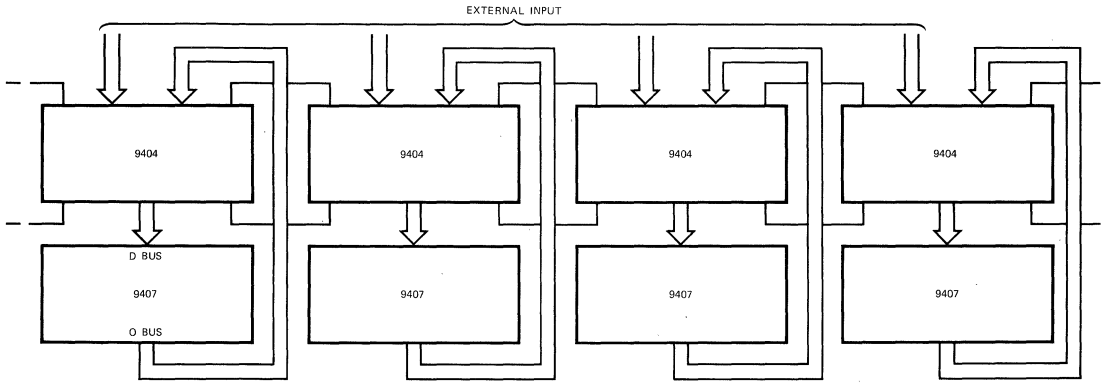


Fig. 2
TYPICAL DATA PATH APPLICATION

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, $\overline{CO}$	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OH}	Output HIGH Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_1$	XM	2.4	3.4		V	I_{OH} = −2.0 mA, V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = −5.7 mA, V_{CC} = MIN
V_{OL}	Output LOW Voltage, $\overline{CO}$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA
				0.4	0.5		V_{CC} = MIN, I_{OL} = 8.0 mA
V_{OL}	Output LOW Voltage $X_0 - X_3$, $\overline{O}_0 - \overline{O}_3$			0.3	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
				0.4	0.5		V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 2 V
I_{OZL}	Output Off LOW Current				−100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 2 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				−0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−30		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CC}	Supply Current			90	145	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC SET-UP REQUIREMENTS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
t_{CW}	Clock Period (Note)	90	60		ns	
t_{PWH}	Clock Pulse Width (HIGH) (Note)	60	40		ns	
t_{PWL}	Clock Pulse Width (LOW) (Note)	30			ns	
t_s	Set-Up Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	20			ns	
t_h	Hold Time, $I_0 - I_3$ to Positive-Going Clock	0			ns	
$t_s\overline{D}$	Set-Up Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	20			ns	
$t_h\overline{D}$	Hold Time, $\overline{D}_0 - \overline{D}_3$, $\overline{CI}$ to Negative-Going Clock	0			ns	
$t_s I$	Set-Up Time, $\overline{CI}$ to Positive-Going Clock	5			ns	
$t_h I$	Hold Time, $\overline{CI}$ to Positive-Going Clock		0		ns	

AC CHARACTERISTICS: V_{CC} = 5.0 V, C_L = 15 pF, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	COMMENTS
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going CP to $\overline{O}_0 - \overline{O}_3$ (Note)		17 22	24 29	ns	$\overline{EO}_0$ LOW, Figure 5
t_{PLH} t_{PHL}	Instruction Code, $I_1 - I_3$ to $X_0 - X_3$		22 22	29 29	ns	$\overline{EO}_X$ LOW, I_0 LOW, Figure 3
t_{PLH} t_{PHL}	Instruction Code, $I_1 - I_3$ to $X_0 - X_3$		42 37	58 51	ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 3
t_{PLH} t_{PHL}	Positive-Going Clock to $X_0 - X_3$		35 29	48 39	ns	$\overline{EO}_X$, I_0 LOW Figure 5
t_{PLH} t_{PHL}	Positive-Going Clock to $X_0 - X_3$		51 51	68 68	ns	$\overline{EO}_X$ LOW, I_0 HIGH, Figure 5
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs to $X_0 - X_3$		19 19	26 26	ns	I_0 HIGH, $I_1 - I_3$ Stable, EO_X LOW, Figure 6
t_{PLH} t_{PHL}	Propagation Delay $\overline{CI}$ to $X_0 - X_3$		16 19	24 26	ns	I_0 HIGH, $I_1 - I_3$ Stable, $\overline{EO}_X$ LOW, Figure 7
t_{PLH} t_{PHL}	Propagation Delay I_0 to $X_0 - X_3$		14 14	19 19	ns	$\overline{EO}_X$ LOW, Figure 4
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going Clock to $\overline{CO}$		35 41	48 56	ns	Figure 5
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$		9 16	15 25	ns	Figure 7
t_{PLH} t_{PHL}	Propagation Delay, Data Inputs $\overline{D}_0 - \overline{D}_3$ to $\overline{CO}$		9 14	15 21	ns	Figure 6
t_{PLH} t_{PHL}	Propagation Delay, Instruction Inputs $I_1 - I_3$ to $\overline{CO}$		25 39	33 53	ns	Figure 3
t_{PZH} t_{PZL}	Enable Delay, $\overline{EO}_0$ to Outputs $\overline{O}_0 - \overline{O}_3$, $\overline{EO}_X$ to $X_0 - X_3$		11	18	ns	
t_{PLZ} t_{PHZ}	Disable Delay, $\overline{EO}_0$ to $\overline{O}_0$, $\overline{O}$ $\overline{EO}_X$ to $X_0 - X_3$		9	15	ns	

TIMING DIAGRAMS

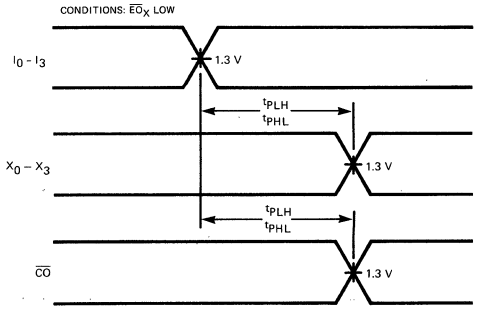
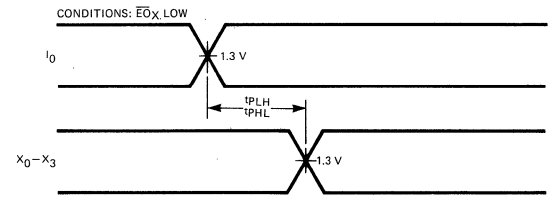


Fig. 3



NOTE:
The internal clock is generated from CP and $\overline{EX}$. The internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW.

Fig. 4

3

TIMING DIAGRAMS (Cont'd)

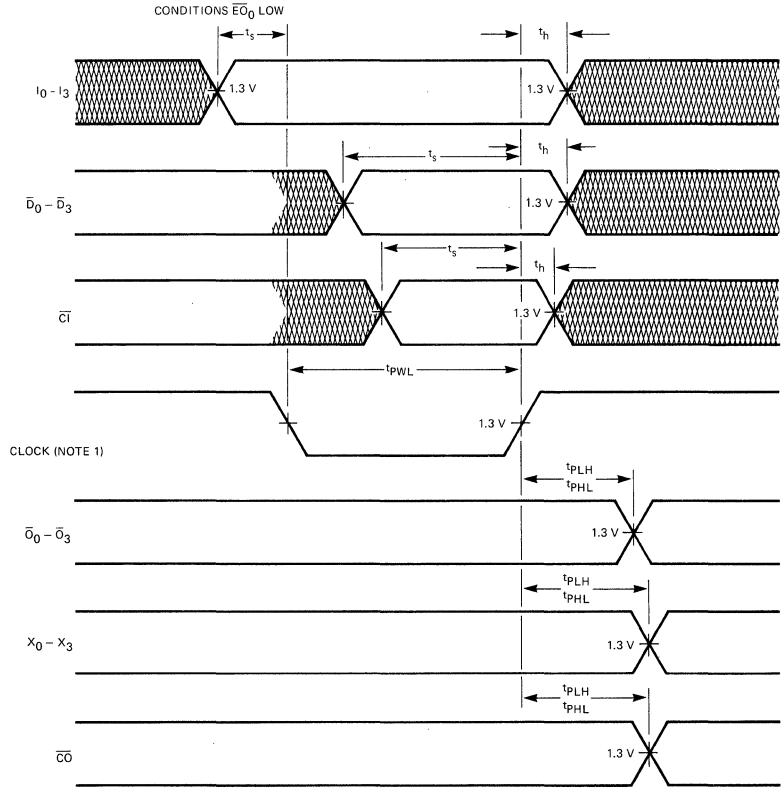


Fig. 5

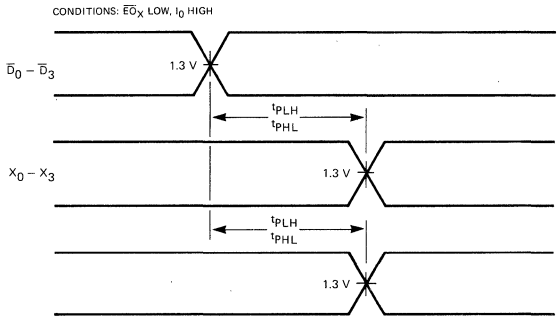


Fig. 6

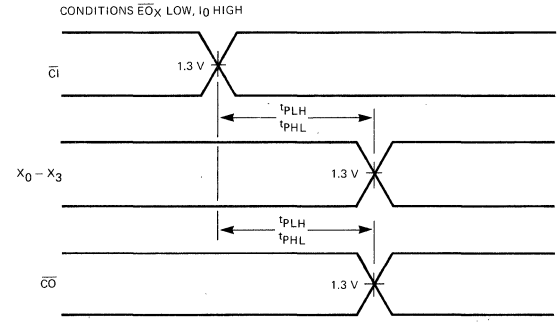


Fig. 7

9408
MICROPROGRAM SEQUENCER
FAIRCHILD I^3L^{TM} MACROLOGIC

DESCRIPTION – The 9408 Microprogram Sequencer controls the order in which microinstructions are fetched from the control memory. It contains a 10-bit program counter, a 4-level last-in first-out stack and associated control logic. It can control up to a maximum of 1024 words of memory. For larger word capacities external paging can be used. The 9408 is controlled by a 4-bit instruction input. The instruction set includes Fetch, Conditional and Unconditional Branches, Branch to Subroutine and Return from Subroutine.

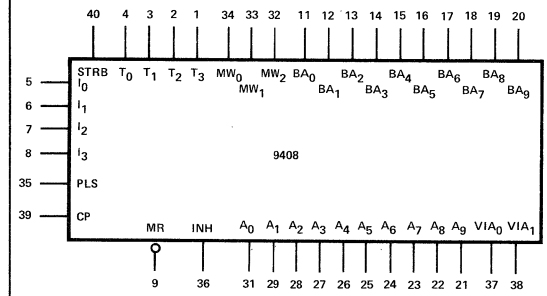
There are seven test inputs – four participate in conditional branches, and three in multiway branches. The conditional test lines are flip-flop buffered. These flip-flops can be tested individually by appropriate branch instructions. The three multiway test inputs are used to form the least significant three bits of the branch address for a multiway branch. Thus, branching occurs at one of eight unique locations depending on the bit pattern present on these three inputs.

The 9408 is designed to operate in pipeline or non-pipeline mode as desired by the user. The device operates synchronously with the clock input and can be initialized using the Master Reset input.

The 9408 is fabricated using Integrated Injection Logic (I^3L^{TM}) technology and fully compatible with all TTL families.

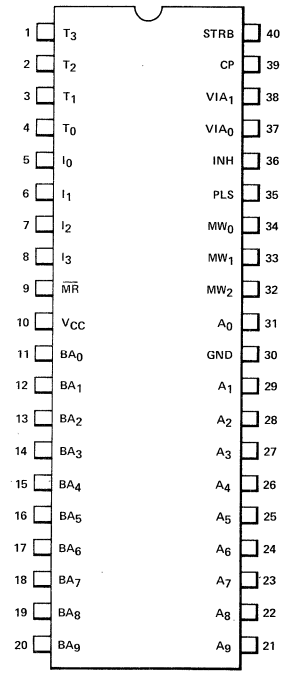
- **CONTROLS 1024 WORDS OF MICROPROGRAM MEMORY (10-BIT ADDRESS)**
- **UNRESTRICTED BRANCHING WITHIN 10-BIT ADDRESS SPACE**
- **16 INSTRUCTIONS**
- **FOUR FLIP-FLOP BUFFERED TEST INPUTS FOR CONDITIONAL BRANCHES**
- **8-WAY BRANCH CAPABILITY**
- **PIPELINE/NON-PIPELINE MODE OF OPERATION**

LOGIC SYMBOL



V_{CC} = Pin 10
GND = Pin 30

CONNECTION DIAGRAM
DIP (TOP VIEW)



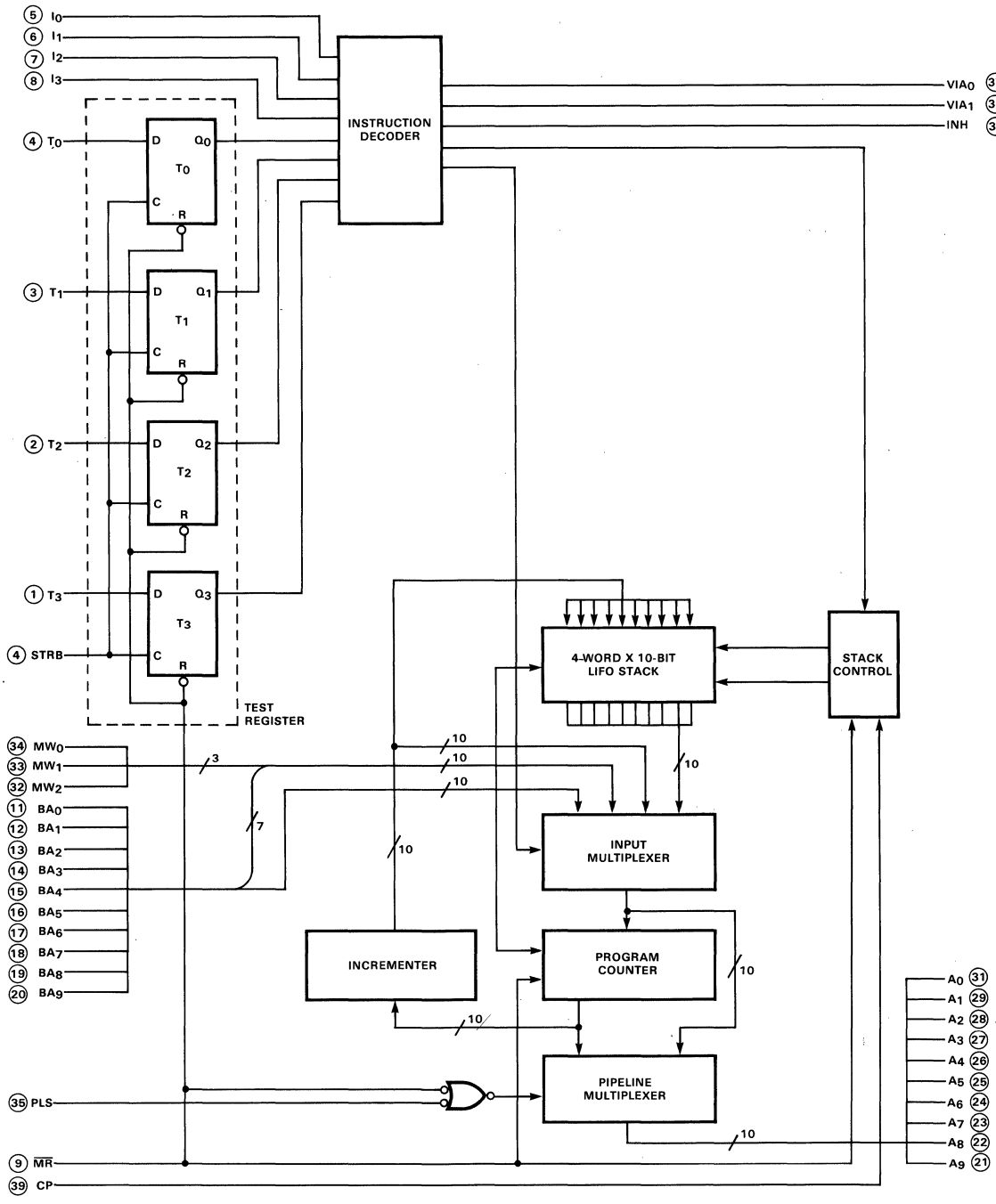
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
BA_0–BA_9	Branch Address Inputs	0.5 U.L.	0.23 U.L.
T_0–T_3	Test Inputs	0.5 U.L.	0.23 U.L.
MW_0–MW_2	Multiway Branch Inputs	0.5 U.L.	0.23 U.L.
I_1	Instruction Input	0.5 U.L.	0.23 U.L.
I_0, I_2, I_3	Instruction Inputs	1.0 U.L.	0.46 U.L.
PLS	Pipeline Select Input	0.5 U.L.	0.23 U.L.
$\overline{MR}$	Master Reset Input (Active LOW)	0.5 U.L.	0.23 U.L.
CP	Clock Pulse Input	1.0 U.L.	0.46 U.L.
STRB	Strobe Input	0.5 U.L.	0.23 U.L.
A_0–A_9	Address Outputs	10 U.L.	5.0 U.L.
VIA_0, VIA_1	VIA Outputs	10 U.L.	5.0 U.L.
INH	Inhibit Output	10 U.L.	5.0 U.L.

Note a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

3

BLOCK DIAGRAM



V_{CC} = Pin 10

GND = Pin 30

◯ = Pin Number

TABLE 1
9408 INSTRUCTION SET

	MNEMONIC	DEFINITION	$I_3I_2I_1I_0$	$T_3T_2T_1T_0$	$O_9O_8O_7$---$O_2O_1O_0$	VIA_1VIA_0	INH	DESCRIPTION OF OPERATION
Unconditional Branch Instructions	BRV_0	Branch VIA_0	L H L L	X X X X	BA_9 BA_8--BA_1 BA_0	L L	H	BA_0 - BA_9 →PC
	BRV_1	Branch VIA_1	L H L H	X X X X	BA_9 BA_8--BA_1 BA_0	L H	H	BA_0 - BA_9 →PC
	BRV_2	Branch VIA_2	L H H L	X X X X	BA_9 BA_8--BA_1 BA_0	H L	H	BA_0 - BA_9 →PC
	BRV_3	Branch VIA_3	L H H H	X X X X	BA_9 BA_8--BA_1 BA_0	H H	H	BA_0 - BA_9 →PC
	BMW	Branch Multiway	L L H H	X X X X	BA_9 BA_3--MW_2 MW_0	L L	H	MW_0 - MW_2, BA_3 - BA_9 →PC
	BSR	Branch to Subroutine	L L L H	X X X X	BA_9 BA_8--BA_1 BA_0	L L	H	BA_0 - BA_9 →PC & Push the Stack
Conditional Branch Instructions	BTH_0	Branch on T_0 HIGH	H H L L	X X X H X X X L	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 0 is HIGH: BA_0 - BA_9 →PC If Test Register 0 is LOW: PC+1→ PC
	BTH_1	Branch on T_1 HIGH	H H L H	X X H X X X L X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 1 is HIGH: BA_0 - BA_9 →PC If Test Register 1 is LOW: PC+1→ PC
	BTH_2	Branch on T_2 HIGH	H H H L	X H X X X L X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 2 is HIGH: BA_0 - BA_9 →PC If Test Register 2 is LOW: PC+1→ PC
	BTH_3	Branch on T_3 HIGH	H H H	H X X X L X X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 3 is HIGH: BA_0 - BA_9 →PC If Test Register 3 is LOW: PC+1→ PC
	BTL_0	Branch on T_0 LOW	H L L L	X X X L X X X H	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 0 is LOW: BA_0 - BA_9 →PC If Test Register 0 is HIGH: PC+1→ PC
	BTL_1	Branch on T_1 LOW	H L L H	X X L X X X H X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 1 is LOW: BA_0 - BA_9 → PC If Test Register 1 is HIGH: PC+1→ PC
	BTL_2	Branch on T_2 LOW	H L H L	X L X X X H X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 2 is LOW: BA_0 - BA_9 →PC If Test Register 2 is HIGH: PC+1→PC
	BTL_3	Branch on T_3 LOW	H L H H	L X X X H X X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 3 is LOW: BA_0 - BA_9 →PC If Test Register 3 is HIGH: PC+1→PC
Miscellaneous Instructions	RTS	Return from Subroutine	L L L L	X X X X	Contents of the Stack Addressed by Read Pointer	L L	L	Pop the Stack
	FTCH	FETCH	L L H L	X X X X	PC+1	L L	L	PC+1→PC

L = LOW Level
H = HIGH Level
X = Don't Care

FUNCTIONAL DESCRIPTION – The 9408 Microprogram Sequencer, shown in the block diagram consists of a 10-bit Program Counter (PC), a 4-word by 10-bit Last-In First-Out (LIFO) Stack with associated control, an Input Multiplexer, a Pipeline Multiplexer, an Instruction Decoder, a 10-bit Incrementer, and a 4-bit Test Register comprised of four edge-triggered D flip-flops.

The Pipeline Multiplexer has two ports – the PC output provides the input port for the non-pipeline mode and the Input Multiplexer output provides the input port for the pipeline mode. Port selection is controlled by the Pipeline Select (PLS) and Master Reset ($\overline{MR}$) inputs. A LOW level on the $\overline{MR}$ input forces the non-pipeline mode of operation and clears the PC. Thus when the 9408 is initialized by the $\overline{MR}$ input the A_0 through A_9 outputs are LOW regardless of the state of the PLS input. A LOW level on the PLS input specifies non-pipeline mode and a HIGH specifies pipeline mode.

The Program Counter is a 10-bit edge-triggered register. The LOW-to-HIGH transition on the Clock (CP) input loads the Input Multiplexer output into the PC. Because of the edge-triggered nature of the PC register, the PC output remains static for a full clock cycle. Thus, in the non-pipeline mode, the PC output can be used to address a control memory built with static devices without storing the memory output in an external microinstruction register. However, in the pipeline mode, the 9408 provides the next address information as soon as available; therefore, execution of a microinstruction can be overlapped with the fetching of the next microinstruction. To ensure microinstruction stability for a full clock cycle, the control-memory output should be buffered with an external microinstruction register.

The Input Multiplexer receives data from four different sources. One port is the output of the LIFO Stack; a second is the output of the 10-bit Incrementer. The Incrementer always adds one to the PC contents. The third and fourth ports are the branch and multiway-branch ports, the latter comprised of the seven most significant Branch Address inputs (BA_3 through BA_9) and the three Multiway inputs, (MW_0 through MW_2).

The 4-word by 10-bit LIFO Stack is a RAM and receives data from the Incrementer output. The stack control logic generates the appropriate control signals, while stack pointers in the Stack Control generate the read and write addresses.

The 4-bit Test Register consists of four type-D flip-flops. The data inputs, which are the four Test inputs (T_0 through T_3), are loaded on the LOW-to-HIGH transition of the Strobe input (STRB).

The Instruction Decoder receives the 4-bit Instruction input (I_0 through I_3) and the Test Register output and generates the VIA_0, VIA_1 and Inhibit (INH) outputs of the 9408. In addition, it generates appropriate logic signals for the Stack Control and Input Multiplexer.

Stack Control – The 9408 has a 4-level subroutine nesting capability as detailed in *Figure 1*. The R_0 and R_1 (Read Address) inputs to the 4-word by 10-bit LIFO Stack specify the address from which information will be read. The W_0 and W_1 (Write Address) inputs specify the address into which information will be written; and the 9408 Incrementer output provides the information to be written into the stack (see block diagram). In addition, writing into the memory is controlled by the Write Enable ($\overline{WE}$) and $\overline{CP}$ inputs.

The R_0, R_1 and W_0, W_1 inputs of the LIFO Stack are derived from the outputs of a 3-bit edge-triggered register called the Stack Pointer (SP). The least significant two bits (SP_0 and SP_1) of this register are the read address inputs to the memory. The SP outputs are also connected to a Stack-Pointer Incrementer and a Decrementer that generate SP + 1 and SP – 1 respectively. The least significant two bits of the Incrementer are the write address bits for the memory.

The outputs of the Incrementer, Decrementer and the Stack Pointer are fed as inputs to a 3-port Stack-Pointer Multiplexer which, in turn, feeds the Stack Pointer inputs. Stack pointer loading always occurs on the LOW-to-HIGH transition of the $\overline{CP}$ input. The $\overline{MR}$ input clears the Stack Pointer. The Stack Pointer Control receives two inputs from the 9408 Instruction Decoder – the BSR input, which is active whenever a Branch-to-Subroutine (BSR) instruction is present on the I_0 through I_3 inputs, and the RTS input, which is active whenever a Return-from-Subroutine (RTS) instruction is specified. The port selection of the Stack Pointer Multiplexer is controlled by the outputs of the Stack Pointer Control. For all 9408 instructions except BSR and RTS, the Stack Pointer Multiplexer selects the Stack Pointer outputs as the instruction source.

Writing into the memory takes place whenever the $\overline{WE}$ and $\overline{CP}$ inputs are LOW. Note that the most significant register bit, SP_2, controls the $\overline{WE}$ input to prevent writing into the memory when all four locations are filled with return addresses. Thus the 9408 does not store and return addresses beyond four nesting levels.

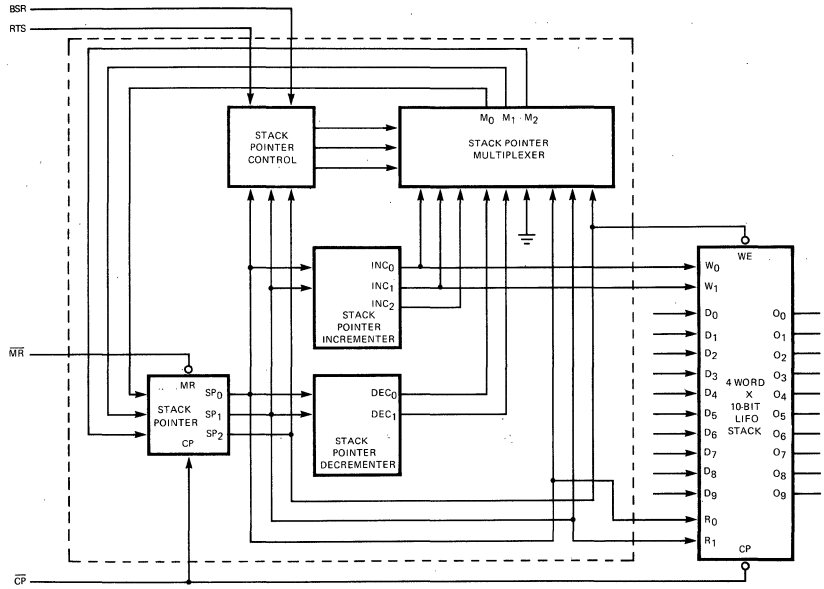


Fig. 1
STACK CONTROL

9408 INSTRUCTIONS

The 9408 instruction set has 16 instructions (*Table 1*). These instructions can be divided into three groups – unconditional branches, conditional branches and miscellaneous – and are specified by appropriate logic levels on the $I_0 - I_3$ inputs.

The unconditional branch group consists of four Branch VIA instructions ($BRV_0 - BRV_3$), Branch Multiway (BMW) and Branch to Subroutine (BSR). This group requires that the next address be explicitly specified on the BA inputs.

The conditional branch group consists of eight instructions, Branch Test HIGH ($BTH_0 - BTH_3$) and Branch Test LOW ($BTL_0 - BTL_3$), for interrogating the four test flip-flops of the 9408 individually. The $BTH_0 - BTH_3$ instructions test flip-flops $T_0 - T_3$ respectively for a HIGH on the Q output (see block diagram). Similarly $BTL_0 - BTL_3$ test for a LOW on the corresponding Q output. If the test condition is satisfied, the next address is taken from the Branch Address ($BA_0 - BA_9$) inputs. If the test condition is not satisified the 9408 performs a Fetch operation.

The miscellaneous group consists of two instructions – Fetch (FTCH) and Return from Subroutine (RTS). These instructions do not require explicit specification of the next address. For the FTCH instruction, the next address is assumed to be the address of the current microinstruction + 1. For RTS, the next address is taken from the Stack. *The Inhibit (INH) output of the 9408 is LOW only for FTCH and RTS instructions. For all other instruction, the INH output is HIGH.*

The VIA outputs of the 9408 (VIA_0, VIA_1) are LOW for all instructions except $BRV_1 - BRV_3$. For BRV_1, the VIA_0 is HIGH and VIA_1 LOW. For BRV_2, the VIA_0 is LOW and VIA_1 HIGH. For BRV_3, both VIA_0 and VIA_1 are HIGH.

Unconditional Branches

$BRV_0 - BRV_3$ – Whenever a Branch VIA instruction code is present on the $I_0 - I_3$ inputs, the Instruction Decoder (see block diagram) establishes the appropriate HIGH/LOW pattern on the VIA_0 and VIA_1 outputs per *Table 1*. The Instruction Decoder also forces the INH output HIGH. Moreover, the $BA_0 - BA_9$ inputs are selected as the source of the next address by the Input Multiplexer.

If the 9408 is in the pipeline mode (PLS input HIGH), the Pipeline Multiplexer transfers the $BA_0 - BA_9$ inputs to the $A_0 - A_9$ outputs. The $BA_0 - BA_9$ inputs are loaded into the PC on the LOW-to-HIGH transition of the CP input. On the other hand, if the non-pipeline mode of operation is selected, the $BA_0 - BA_9$ inputs appear on the output only after the LOW-to-HIGH transition of the CP input.

BMW – For a Branch Multiway instruction, the Instruction Decoder forces the VIA_0 and VIA_1 outputs LOW and INH output HIGH. The Input Multiplexer selects the $BA_3 - BA_9$ inputs as the most significant seven bits and $MW_0 - MW_2$ inputs as the least significant three bits of the next address. If the pipeline mode of operation is selected, the next address formed by the Input Multiplexer ($BA_3 - BA_9$ and $MW_0 - MW_2$ inputs) is transferred to the $A_0 - A_9$ outputs. On the LOW-to-HIGH transition of the CP input, this next address is also leaded into the PC. For non-pipeline mode, the next address is available on the $A_0 - A_9$ output only after the CP transition.

BSR – During a Branch-to-Subroutine instruction, the Instruction Decoder forces a LOW on the VIA_0 and VIA_1 outputs and a HIGH on the INH output. The Input Multiplexer selects the $BA_0 - BA_9$ inputs as the source for the next address. If the pipeline mode is selected, this next address is transferred to the $A_0 - A_9$ outputs by the Pipeline Multiplexer. As usual, the PC is updated with this next address on the LOW-to-HIGH transition of the CP input. During non-pipeline operation, the next address appears on the output only after the CP transition.

The PC holds the address of the current microinstruction. For the BSR instruction, the return address must be stored in the Stack, which is fed by the PC through an Incrementer (see block diagram). When the CP input is LOW, the incremented value is written into the Stack as a return address. The LOW-to-HIGH transition of the CP input not only loads the PC with the next address, *i.e.,* $BA_0 - BA_9$ inputs, but also increments the Stack Pointer as explained above.

Conditional Branches

$BTH_0 - BTH_3$ – For a Branch Test HIGH instruction, the Instruction Decoder establishes a LOW on VIA_0 and VIA_1 outputs and HIGH on the INH output. It then tests for a HIGH on the Q output of the corresponding flip-flop in the test register. If a HIGH level is found, the Input Multiplexer selects the $BA_0 - BA_9$ inputs as the source for the next address.

On the other hand, if the tested Q output of the flip-flop is LOW, the Incrementer output is selected as the source of the next address by the Input Multiplexer. In either case, the PC is loaded with the next address on the LOW-to-HIGH transition of the CP input. As usual, if the pipeline mode is selected, the next address is transferred to the $A_0 - A_9$ outputs. For non-pipeline mode, the next address appears on the output after the clock transition.

$BTL_0 - BTL_3$ – Operation of the Branch Test LOW instructions is identical to $BTH_0 - BTH_3$ except that Q outputs of the test register flip-flops are tested for a LOW. If the tested output is LOW, a branch occurs. If tested output is HIGH the Incrementer output is the next address.

Miscellaneous

FTCH – For a Fetch instruction, the Instruction Decoder establishes a LOW on the VIA_0 and VIA_1 outputs. In addition, the INH output is also LOW. The Input Multiplexer selects the Incrementer output as the next address. If pipeline mode is selected, the Incrementer output is transferred to the $A_0 - A_9$ outputs. For non-pipeline mode, the incremented address appears at the output only after the clock transition.

RTS – For a Return-from-Subroutine instruction, the Instruction Decoder establishes a LOW on the VIA_0, VIA_1 and the INH outputs. The Input Multiplexer selects the Stack output as the source of the next address. As usual, for the pipeline mode, the next address is transferred to the output by the Pipeline Multiplexer. For non-pipeline operation, the next address appears on the output only after the clock transition. In addition, this instruction also decrements the Stack Pointer as described above.

DC CHARACTERISTICS: (Over Operating Temperature Range unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (2)	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.9	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA
		XC	2.4	3.4			
V_{OL}	Output LOW Voltage			0.25	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current, All except CP, I_0, I_2, I_3			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current, CP, I_0, I_2, I_3			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Input HIGH Current, All Inputs				1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, All except CP, I_0, I_2, I_3			0.21	0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
	Input LOW Current, CP, I_0, I_2, I_3			0.42	0.72		
I_{OS}	Output Short Circuit Current, Q_0–Q_3, Q_S		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 (Note 3)
I_{CC}	Supply Current			130		mA	V_{CC} = MAX, MR LOW

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PHH}	Propagation Delay,		35		ns	I_1, I_2 HIGH, I_3 LOW
t_{PLL}	Instruction to VIA		35		ns	I_0 = Input, VIA_0 = Output
t_{PHH}	Propagation Delay,		35		ns	I_1 HIGH, I_2, I_3 LOW
t_{PLL}	Instruction to INHIBIT		35		ns	I_0 = Input, I_{NH} = Output
t_{PHH}	Propagation Delay, Positive		45		ns	I_1 HIGH, PL, I_0, I_2, I_3 LOW
t_{PHL}	Going CP to Any A (Non-Pipeline)		52		ns	
t_{PHH}	Propagation Delay, Positive		98		ns	PL, I_1 HIGH,
t_{PHL}	Going CP to Any A (Pipeline)		98		ns	I_0, I_2, I_3 LOW
t_{PHH}	Propagation Delay,		22		ns	PL, I_0, I_1, I_2 HIGH
t_{PLL}	BA to A (Pipeline)		28		ns	I_3 LOW
t_{PHH}	Propagation Delay,		72		ns	I_0, I_1, BA_0, PL HIGH I_3, MW_0 LOW, A_0 = Output
t_{PLL}	Instruction to Any A (Pipeline)		72		ns	I_2 = Input, A_0 = Output
t_{PWH}	Min CP Pulse Width (HIGH)		18		ns	I_1 HIGH
t_{PWL}	Min CP Pulse Width (LOW)		30		ns	I_0, I_2, I_3, PL LOW
t_s	Set-up Time, BA to CP		15		ns	I_2 HIGH, I_0, I_1, I_3, PL LOW BA_0 = Input, A_0 = Output
t_h	Hold Time, BA to CP		5		ns	I_2 HIGH, I_0, I_1, I_3 PL LOW BA_0 = Input, A_0 = Output
t_s	Set-up Time, Instruction to CP		90		ns	I_0, I_1, BA_0 HIGH I_3, MW_0, PL LOW
t_h	Hold Time, Instruction to CP		−20		ns	I_2 = Input, A_0 = Output
t_s	Set-up Time, Strobe to CP (Required to achieve conditional branch in the same microcycle)		60		ns	I_3, $TEST_0$ HIGH I_0, I_1, I_2, PL, BA_0 LOW Strobe = Input, A_0 = Output
t_s	Set-up Time, Test to Strobe		5		ns	I_2, I_3, PL HIGH I_0, I_1, BA_0 LOW $TEST_0$ = Input, A_0 = Output
t_h	Hold Time, Test to Strobe		15		ns	I_2, I_3, PL HIGH I_0, I_1, BA_0 LOW $TEST_0$ = Input, A_0 = Output
t_{rec}	Recovery Time, MR to CP		20		ns	

3

9410

REGISTER STACK • 16×4 RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD TTL MACROLOGIC

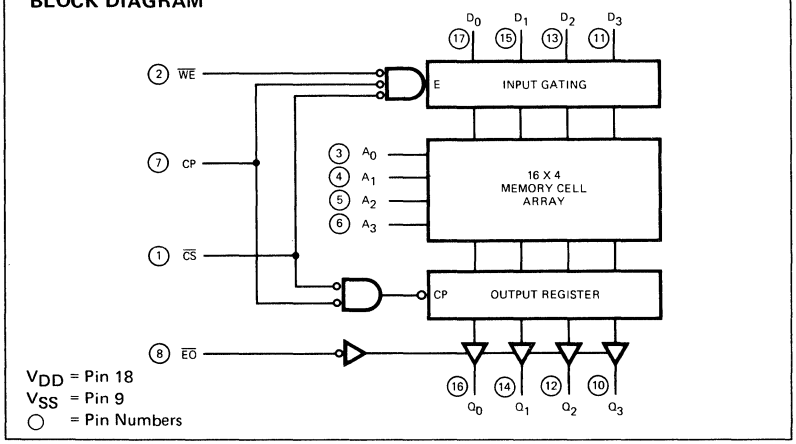
DESCRIPTION – The 9410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 9410 is fully compatible with all TTL families.

- **EDGE-TRIGGERED OUTPUT REGISTER**
- **TYPICAL ACCESS TIME OF 35 ns**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **TYPICAL POWER OF 375 mW**
- **18-PIN PACKAGE**

PIN NAMES		LOADING (Note a) HIGH	LOW
A_0-A_3	Address Inputs	1.0 U.L.	0.23 U.L.
D_0-D_3	Data Inputs	1.0 U.L.	0.23 U.L.
$\overline{CS}$	Chip Select Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{EO}$	Output Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
$\overline{WE}$	Write Enable Input (Active LOW)	1.0 U.L.	0.23 U.L.
CP	Clock Input (Outputs Change on LOW to HIGH Transition)	1.0 U.L.	0.23 U.L.
Q_0-Q_3	Outputs	130 U.L.	10 U.L. (Note b)

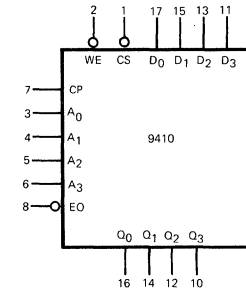
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) 10 LOW Unit Loads measured at 0.5 V.

BLOCK DIAGRAM



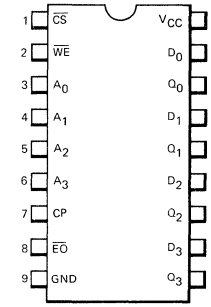
V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION

Write Operation – When the three control inputs: Write Enable (WE), Chip Select (CS), and Clock (CP), are LOW the information on the data inputs (D_0 - D_3) is written into the memory location selected by the address inputs (A_0 - A_3). If the input data changes while WE, CS, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

Read Operation – Whenever CS is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs ($A_0 - A_3$) is edge-triggered into the Output Register.

A 3-State Output Enable (EO) controls the output buffers. When EO is HIGH the four outputs (Q_0 - Q_3) are in a high impedance or OFF state; when EO is LOW, the outputs are determined by the state of the Output Register.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	XM			0.7	V	Guaranteed Input LOW Voltage
		XC			0.8		
V_{CD}	Input Clamp Diode Voltage			–0.9	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	XM	2.4	3.4			I_{OH} = –2.0 mA; V_{CC} = MIN
		XC	2.4	3.1			I_{OH} = –5.2 mA; V_{CC} = MIN
V_{OL}	Output LOW Voltage	XM & XC		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
		XC		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 16 mA
I_{OZH}	Output Off HIGH Current				100	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = 3 V
I_{OZL}	Output Off LOW Current				–100	μA	V_{CC} = MAX, V_{OUT} = 0.5 V, V_E = 3 V
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input LOW Current				–0.36	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		–30		–100	mA	V_{CC} = MAX, V_{OUT} = 0 V (Note 3)
I_{CCH}	Supply Current			75	110	mA	V_{CC} = MAX, Inputs Open

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

3

AC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
READ MODE						
t_{PZH}	Enable Delay, Output Enable to Output		9	15	ns	Figure 1
t_{PZL}			9	15	ns	
t_{PHZ}	Disable Time, Output Enable to Output		10	16	ns	Figure 1
t_{PLZ}			10	16	ns	
t_{PLH}	Propagation Delay, Clock to Output		14	20	ns	Figure 2
t_{PHL}			14	20	ns	
t_sAR	Set-up Time to Read from Address to Clock	38	25		ns	Figure 2
t_hAR	Hold Time to Read from Address to Clock	0			ns	Figure 2
WRITE MODE						
t_W	Write Enable, Chip Select, or Clock Pulse Width Required to Write (Note a)	21	12		ns	Figure 3
t_sAW	Set-up Time Address to Write Enable (Note b)	5			ns	Figure 3
t_hAW	Hold Time Address to Write Enable (Note b)	0			ns	Figure 3
t_sDW	Set-up Time Data to Write Enable (Note b)	16	9		ns	Figure 3
t_hDW	Hold Time Data to Write Enable	0			ns	Figure 3

NOTES:

a) Writing occurs when $\overline{WE}$, $\overline{CE}$ and CP are LOW.
b) Assuming $\overline{WE}$ is utilized as Writing Strobe.

READ MODE AC PARAMETERS

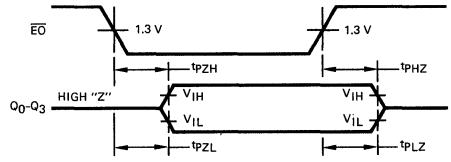
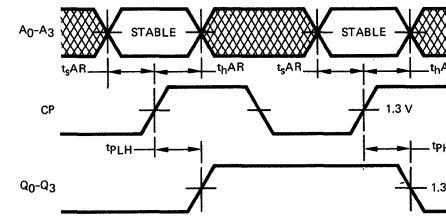


Fig. 1

PROPAGATION DELAY OUTPUT ENABLE TO DATA OUTPUTS

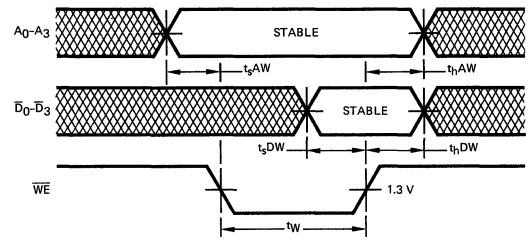


Other Conditions: $\overline{CS} = \overline{OE}$ = LOW

Fig. 2

PROPAGATION DELAY CLOCK TO DATA OUTPUTS, AND SET-UP AND HOLD TIMES ADDRESS TO CLOCK TO READ

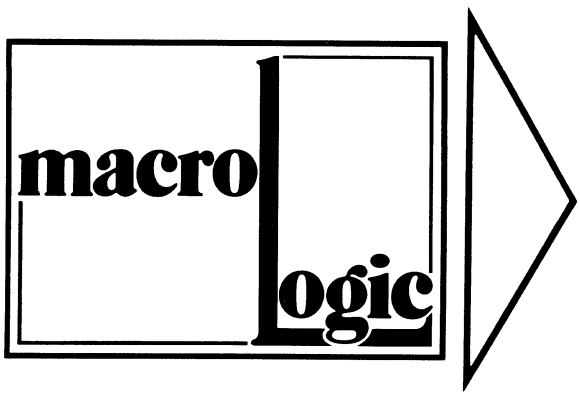
WRITE MODE AC PARAMETERS



Other Conditions: $\overline{CS}$ = CP = LOW

Fig. 3

WRITE ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES ADDRESS AND DATA TO WRITE ENABLE



4700
CMOS MACROLOGIC SERIES

GENERAL DESCRIPTION

Fairchild CMOS logic combines popular CMOS functions with the advanced Isoplanar C process. The result is a logic family with a superior combination of noise immunity and standardized drive characteristics. At static conditions, these devices dissipate very low power, typically 10 nW per gate. The low power combined with the wide (3 to 15 V) recommended operating supply voltage requirement greatly minimizes power supply costs. The CMOS family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

- **LOW POWER – TYPICALLY 10 nW PER GATE STATIC**
- **WIDE OPERATING SUPPLY VOLTAGE RANGE –**
  3 TO 15 V RECOMMENDED
  18 V ABSOLUTE MAXIMUM
- **HIGH NOISE IMMUNITY**
- **BUFFERED OUTPUTS STANDARDIZE OUTPUT DRIVE AND REDUCE VARIATION OF PROPAGATION DELAY WITH OUTPUT CAPACITANCE**
- **WIDE OPERATING TEMPERATURE RANGE**
  COMMERCIAL –40°C TO +85°C
  MILITARY –55°C TO +125°C
- **HIGH DC FAN-OUT – GREATER THAN 50**

ISOPLANAR C TECHNOLOGY

The Fairchild CMOS logic family uses Isoplanar C for high performance. This technology combines local oxidation isolation techniques with silicon gate technology to achieve an approximate 35% to 100% savings in area as shown in *Figure 4-1.* Operating speeds are increased due to the self-alignment of the silicon gate and reduced sidewall capacitance.

Conventional CMOS circuits are fabricated on an n-type substrate as shown in *Figure 4-2.* The p-type substrate required for complementary n-channel MOS is obtained by diffusing a lightly doped p-region into the n-type substrate. Conventional CMOS fabrication requires more chip area and has slower circuit speeds than Isoplanar C CMOS. This is a result of the n+ or p+ channel stop which surrounds the p- or n-channels respectively in conventional metal gate CMOS, Silicon gate CMOS *(Figure 4-3)* has a negligible reduction in area, though transient performance is improved.

DESIGN CONSIDERATIONS

Fairchild Isoplaner F4000 Series CMOS is a complete family of SSI, MSI, and LSI silicon gate CMOS. The 4700 CMOS Macrologic series is the LSI segment of this family. The following discussion of design considerations covers Fairchild's entire F4000 series CMOS family.

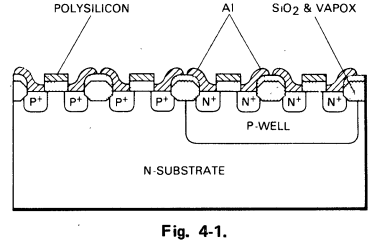


Fig. 4-1.
ISOPLANAR C CMOS STRUCTURE REDUCES AREA 35%

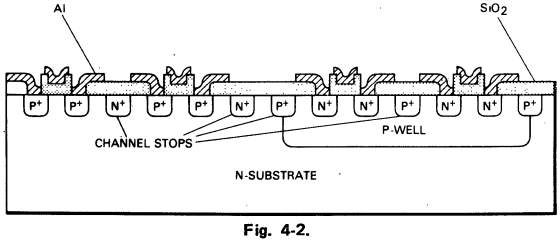


Fig. 4-2.
CONVENTIONAL METAL GATE CMOS STRUCTURE

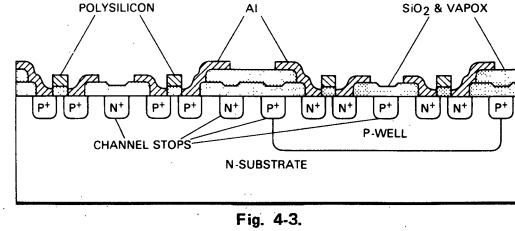


Fig. 4-3.
CONVENTIONAL SILICON GATE CMOS STRUCTURE REDUCES AREA 8%

Originally designed for aerospace applications, CMOS now finds its way into portable instruments, industrial and medical electronics, automotive applications and computer peripherals, besides dominating the electronic watch market.

In late 1973, Fairchild introduced the F4000 CMOS family, using Isoplanar technology to achieve superior electrical performance. Most of these devices are functional equivalents and pin-for-pin replacements of the well-known 4000 series; some are equivalent to TTL circuits and some are proprietary logic designs.

A few CMOS devices, such as bidirectional analog switches, exploit the unique features of CMOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity; but most of the available CMOS elements today are of SSI and MSI complexity and perform logic functions that have been available in DTL or TTL for many years. Therefore, it is both helpful and practical to compare the performance of CMOS with that of the more familiar DTL/TTL *(Figure 4-4).*

CMOS speed is comparable to 74L-TTL and DTL, and about three to six times slower than TTL or Low Power Schottky (LS-TTL). Voltage noise immunity and fan out are almost ideal, supply voltage is noncritical, and the quiescent power consumption is close to zero-several orders of magnitude lower than for any competing technology.

Power Consumption

Under static conditions, the p-channel (top) and the n-channel (bottom) transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0.5 nA per gate, resulting in very attractive low power consumption of 2.5 nW per gate (at 5 V).

Whenever a CMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the top and the bottom transistors are partially conducting. This dynamic power consumption is obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in *Figure 4-5,* the power consumption of a CMOS gate exceeds that of a low power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency.

At 100 transitions per second, the dynamic power consumption is far greater than the static dissipation; at one million transitions per second, it exceeds the power consumption of LS-TTL. Comparing the power consumption of more complex devices (MSI or LSI) in various technologies may show a different result. In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and consume, therefore, much less power.

A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit. The small static supply current, I_{DD} is specified on individual data sheets for 5, 10 and 15 V. The dynamic power dissipation for 5, 10 and 15 V, 15 and 50 pF may be found in graph form for frequencies of 100 Hz to 10 MHz. The total power may be calculated, $P_T = (I_{DD} \times V_{DD})$ + dynamic power dissipation.

Supply Voltage Range

CMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4.5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ >20 V), causing SCR latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to TTL. The F4049, F4050 and F4104 provide level translation between TTL and CMOS when CMOS supply

PARAMETER	STANDARD TTL	74L	DTL	LOW POWER SCHOTTKY	F4000 CMOS 5 V SUPPLY	F4000 CMOS 10 V SUPPLY
PROPAGATION DELAY (GATE)	10 ns	33 ns	30 ns	5 ns	40 ns	20 ns
FLIP-FLOP TOGGLE FREQUENCY	35 MHz	3 MHz	5 MHz	45 MHz	8 MHz	16 MHz
QUIESCENT POWER (GATE)	10 mW	1 mW	8.5 mW	2 mW	10 nW	20 nW
NOISE IMMUNITY	1 V	1 V	1 V	0.8 V	2 V	4 V
FAN-OUT	10	10	8	20	50*	50*

*OR AS DETERMINED BY ALLOWABLE PROPAGATION DELAY

Fig. 4-4
CMOS COMPARED TO OTHER LOGIC FAMILIES

voltages over 5 V are used. While devices are usable to 18 V, operation above 12 V is discouraged for reasons of power dissipation.

Low static power consumption combined with wide supply voltage range make CMOS the ideal logic family for battery operated equipment.

Propagation Delay

Compared to TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading. See *Figure 4-6.* The Fairchild F4000 family uses both advanced processing (Isoplanar) and improved circuit design (buffered gates) to achieve propagation delays and output rise times that are superior to any other junction-isolated CMOS design. (Silicon-on-sapphire, SOS, can achieve similar performance but at a substantial cost penalty).

Isoplanar processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum toggle frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

Capacitance Loading Effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because anybody considers this a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. TTL with an output impedance less than 100 Ω is little affected by an increase in capacitive loading; a 100 pF load increases the delay by only about 4 ns. CMOS, however, with an output impedance of 1 kΩ (worst case at 5 V) is 10 times more sensitive to capacitance loading. *Figures 4-7* and *4-8* show the positive- and negative-going delays as a function of load capacitance. It should be noted that the older, unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

Supply Voltage Effect

Figures 4-9 and *4-10* show propagation delay as a function of supply voltage and again indicate the symmetry of the positive- and negative-going delays. Increasing the supply voltage from 5 to 10 V more than doubles the speed of CMOS gates. Increasing the supply voltage to 15 V almost doubles the speed again, but, as mentioned before, results in a significant increase in dynamic power dissipation.

TYPICAL POWER DISSIPATION VERSUS INPUT FREQUENCY FOR SEVERAL POPULAR LOGIC FAMILIES

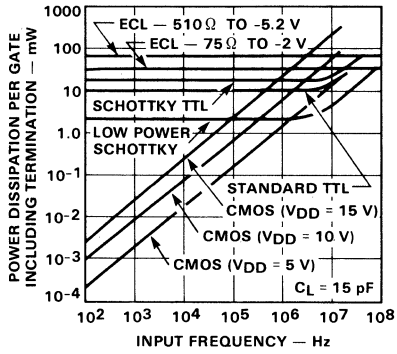


Fig. 4-5

NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE FOR TTL AND CMOS

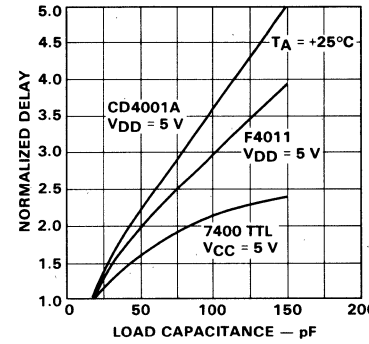


Fig. 4-6

POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

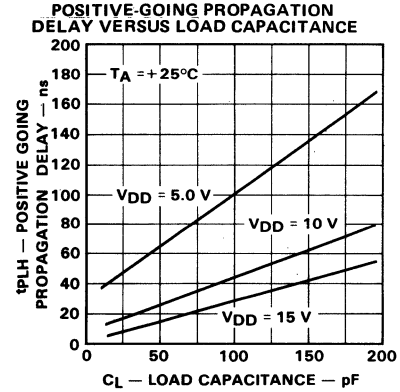


Fig. 4-7

NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

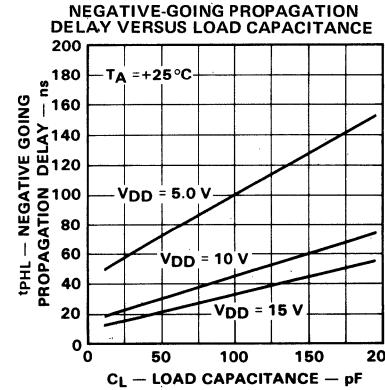


Fig. 4-8

4

The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.

Temperature Effect

Figures 4-11 and *4-12* show propagation delay as a function of ambient temperature. The temperature dependence of CMOS is much simpler than with TTL, where three factors contribute - increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In CMOS, essentially only the carrier mobility changes, thus increasing the impedance and hence the delay with temperature. For F4000 devices, this temperature dependence is less than 0.3% per ^{o}C, practically linear over the full temperature range. Note that the commercial temperature range is -40 to +85^{o}C rather than the usual 0 to +75^{o}C.

CMOS delays increase with temperature. They are very sensitive to capacitive loading but can be reduced by increasing the supply voltage to 10 or even 15 V.

To determine propagation delays, the effects of capacitive loading, supply voltage, manufacturing tolerances and ambient temperature must be considered. Start with the values of t_{PLH} (propagation delay, a LOW-to-HIGH output transition) and t_{PHL} (propagation delay, a HIGH-to-LOW output transition) given in the individual data sheets. Delay values for V_{DD} at 5, 10 and 15 V and output capacity of 15 and 50 pF are provided. Manufacturing tolerances account for the differences between MIN, TYP and MAX.

Noise Immunity

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, CMOS can claim very good voltage noise immunity, typically 45% of the supply voltage, *i.e.,* 2.25 V in a 5 V system, 4.5 V in a 10V system. Compare this with the TTL transfer curve in *Figure 4-13* and its resultant 1 V noise immunity in a lightly loaded system and only 0.4 V worst case.

Since CMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a CMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent CMOS delays act as a

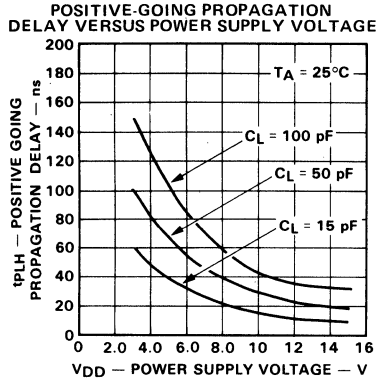


Fig. 4-9

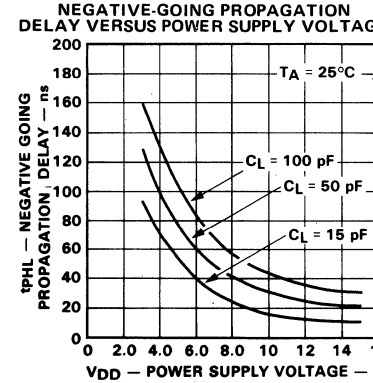


Fig. 4-10

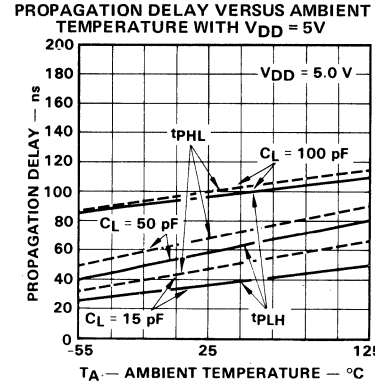


Fig. 4-11

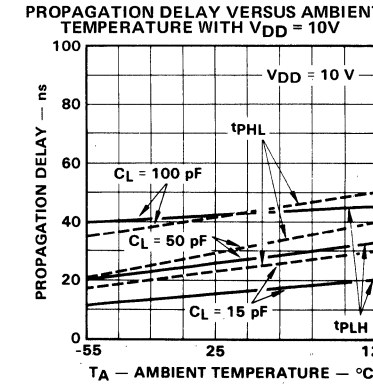


Fig. 4-12

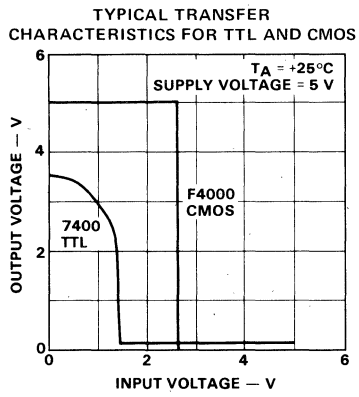


Fig. 4-13

noise filter; 10 ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of CMOS is 10 to 100 times higher than that of TTL. CMOS interconnections are therfore less "stiff" and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, CMOS has about six times *less* noise margin than TTL. It takes more than 20 mA to pull a TTL output into the threshold region, but it takes only 3 mA to pull a CMOS output into the threshold of a 5 V system.

The nearly ideal transfer characteristic and the slow response of CMOS circuits make them insensitive to low voltage, magnetically coupled noise. The high output impedance, however, results in a poor rejection of capacitively coupled noise.

Interface to TTL

When CMOS is operated with a 5 V power supply, interface to TTL is straightforward. The input impedance of CMOS is very high, so that any form of TTL will drive CMOS without loss of fan-out in the LOW state. Unfortunately, most TTL has insufficient HIGH state voltage (typically 3.5 V) to drive CMOS reliably. A pull up resistor (1 kΩ to 10 kΩ) from the output of the TTL device to the 5 V power supply will effectively pull the HIGH state level to 4.5 V or above. Alternately, DTL Hex inverters may be used between the TTL and CMOS. 9LS Low Power Schottky and 93L00 Low Power TTL/MSI utilize the unique output configuration shown in *Figure 4-14* to pull its output to $V_{CC} - V_{BC}$ or approximately 4.3 V when lightly loaded.

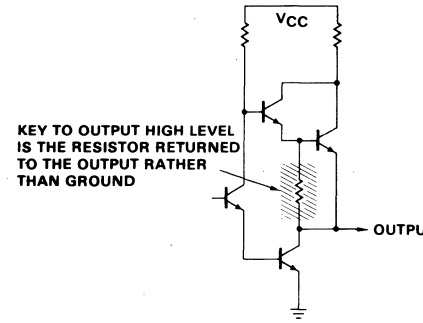


Fig. 4-14

THE 93L00 AND 9LS00 TTL FAMILIES WILL DRIVE CMOS DIRECTLY WITHOUT RESISTORS AS LONG AS THERE ARE ONLY CMOS DEVICES BEING DRIVEN FROM THE OUTPUT.

All F4000 logic elements will drive a single 9LS low power Schottky input fan in directly. A 9LS Hex inverter such as the 9LS04 makes an excellent low cost TTL buffer with a fan out of 20 into 9LS or 5 into standard TTL. Alternately, the F4049 and F4050 Hex buffers may be used to drive a fan out of 8 into 9LS or 2 into standard TTL.

When operating CMOS at voltages higher than 5 V, direct interface to TTL cannot be used. The F4104 Quad Level Translator converts TTL levels to high voltage CMOS up to 15 V. The F4049 and F4050 Hex Buffers will accept high voltage CMOS levels up to 15 V and drive 2 standard TTL loads.

Input/Output Capacity

CMOS devices exhibit input capacities in the 1.5 to 5 pF range and output capacity in the 3 to 7 pF range.

Output Impedance

All F4000 logic devices employ standardized output buffers. It should be noted that these impedances do not change with input pattern as do conventional CMOS gates. Buffers, analog switches and analog multiplexers employ special output configurations which are detailed in individual data sheets.

Input Protection

The gate input to any MOS transistor appears like a small (<1 pF) very low leakage ($<10^{-12}$ A) capacitor. Without special precautions, these inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

Each member of the F4000 family utilizes a series resistor, nominally 200 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} *(Figure 4-15).* The resistor is a poly-silicon "true resistor" without a parasitic substrate diode. This ensures that the input impedance is always at least 200 Ω under all biasing conditions, even when V_{DD} is short circuited to V_{SS}. A

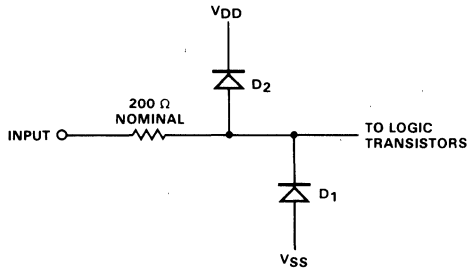


Fig. 4-15
F4000 SERIES CMOS
INPUT PROTECTION CIRCUIT

parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0.9 V at 1 mA and reverse breakdowns of 20 V for D_1 and 20 V for D_2. For certain special applications such as oscillators, the diodes actually conduct during normal operation. However, currents must be limited to 10 mA.

Handling Precautions

All MOS devices are subject to damage by large electrostatic charges. All F4000 devices employ the input protection described in *Figure 4-15,* however, electrostatic damage can still occur. The following handling precautions should be observed.

1. All F4000 devices are shipped in conducting foam or tubes. They should be removed for inspection or assembly using proper precautions.
2. Ionized air blowers are recommended when automatic incoming inspection is performed.
3. F4000 devices, after removal from their shipping material, should be placed leads down on a grounded surface. Conventional cookie tins work well. Under no circumstances should they be placed in polystyrene foam or plastic trays used for shipment and handling of conventional ICs.
4. Individuals and tools should be grounded before coming in contact with F4000 devices.
5. Do not insert or remove devices in sockets with power applied. Ensure power supply transients, such as occur during power turn-on or off; do not exceed maximum ratings.
6. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{SS}, V_{DD} or the output of a logic element.
7. After assembly on PC boards, ensure that static discharge cannot occur during storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam. Board input/output pins may be protected with large value resistors (10 MΩ) to ground.
8. In extremely hostile environments, an additional series input resistor (10 to 100 kΩ) provides even better protection at a slight speed penalty.

A Word to the TTL Designer

Designing with CMOS is generally an easy transition and allows the designer to discard many of the old design inhibitions for new found freedoms. A few of these are:

Fan-out - It is practically unlimited from a dc point of view and is restricted only by delay and rise time considerations.

Power Supply Regulation - Anything between 3 V and 15 V goes, as long as all communicating circuits are fed from the same voltage.

Ground and V_{CC} Line Drops - The currents are normally so small that there is no need for heavy supply line bussing.

V_{CC} Decoupling - It can be reduced to a few capacitors per board.

Heat Problems - They do not exist, unless an attempt is made to run CMOS very fast and from more than 10 V.

It should also be noted that there are a few warnings called for when designing with CMOS and that many of the hard-earned good engineering basics cannot be forgotten. A few of the new design challenges include:

Unused Inputs - They must be connected to V_{SS} or V_{DD} (V_{CC} or ground) lest they generate a logical "maybe". The bad TTL habit of leaving unused inputs open is definately out.

Oscillations - Slowly rising or falling inputs signals can lead to oscillations and multiple triggering. A poorly regulated and decoupled power supply magnifies this problem since the CMOS input threshold varies with the supply voltage.

Timing Details - Even slow systems require a careful analysis of worst case timing delays, derated for maximum temperature, minimum supply voltage and maximum capacitive loading. Many CMOS flip-flops, registers and latches have a real hold time requirement, *i.e.,* inputs must remain stable even after the active clock edge; some require a minimum clock rise time. This hasn't been a problem with TTL. CMOS systems, even slow ones, are prone to unsuspected clock skew problems, especially since a heavily loaded clock generator can have a poor rise time.

JEDEC INDUSTRY STANDARD "B" SERIES CMOS

Throughout first quarter of 1976 the CMOS vendor industry, in total, was invited to participate in the generation of a new JEDEC Industry Standard CMOS "B" Series specification. Unanimous agreement was reached in April of 1976 and confirmed by industry wide ballot in May.

This section is meant to extend knowledge of the new Industry Standard "B" Series specification to the customer and ensure that all Fairchild CMOS products meet or exceed all specifications of the new JEDEC standard.

In fact, since first introduction of the Isoplanar CMOS Family in 1973, all Fairchild CMOS products have been designed and tested to meet or exceed the recently announced JEDEC specifications as listed in the JEDEC "Standard Specification for description of "B" Series CMOS devices" dated June, 1976.

STANDARD SPECIFICATION FOR DESCRIPTION OF "B" SERIES CMOS DEVICES

(Formulated under the cognizance of the JEDEC JC-40.2 Committee on CMOS Standardization)

1. Purpose

1.1 *Purpose*

To develop a standard of "B" Series CMOS Specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and system design by users.

1.2 *Scope*

This tentative Standard covers standard specifications for description of "B" Series CMOS devices.

2. Definitions

2.1 *"B" Series*

"B" Series CMOS includes both buffered and unbuffered devices.

2.2 *"Buffered"*

A buffered output is one that has the characteristic that the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present.

3. Standard Specifications

3.1 *Listing of Standard Specifications*

Table 1 lists the standard specifications for "B" Series CMOS devices.

3.2 *Absolute Maximum Ratings*

In the maximum ratings listed below voltages are referenced to V_{SS}.

DC Supply Voltage	V_{DD}	-0.5 V to +18 V
Input Voltage	V_{IN}	-0.5 V to V_{DD} +0.5 V
DC Input Current (any one input)	I_{IN}	±10 mA
Storage Temperature Range	T_S	-65°C to +150°C

3.3 *Recommended Operating Conditions*

Recommended operating conditions are listed below.

DC Supply Voltage	V_{DD}	+3 V to +15 V
Operatings Temperature Range	T_A	
Military-Range Devices		-55°C to +125°C
Commercial-Range Devices		-40°C to +85°C

3.4 *Designation of "B" Series CMOS Devices*

Those parts which have analog inputs and/or outputs shall be included in the "B" Series providing those parts' maximum ratings and logical input and output parameters conform to the "B" Series, such as (including, but not limited to):

4046B	4066B
4051B	4511B
4053B	4528B
4053B	

Products that meet "B" Series specifications except that the logical outputs are not buffered and the V_{IL} and V_{IH} specifications are 20% and 80% of V_{DD} respectively shall be marked with the UB designation, such as (including, but not limited to):

4000UB	4012UB
4001UB	4023UB
4002UB	4025UB
4011UB	

As defined by the previous Industry Standard Specification, Fairchild offers immediate availability of the following devices:

4001B	4025B	4068B	4520B	4731B
4002B	4027B	4069UB	4528B	40014B
4006B	4028B	4070B	4539B	40085B
4007UB	4029B	4071B	4555B	40097B
4008B	4030B	4073B	4556B	40098B
4011B	4035B	4075B	4582B	40160B
4012B	4040B	4076B	4702B	40161B
4013B	4041B	4077B	4703B	40162B
4014B	4042B	4078B	4704B	40163B
4015B	4043B	4081B	4705B	40174B
4016B	4044B	4085B	4706B	40175B
4017B	4046B	4086B	4707B	40192B
4018B	4049B	4104B	4710B	40193B
4019B	4050B	4510B	4720B	40194B
4020B	4051B	4511B	4721B	40195B
4021B	4052B	4512B	4723B	
4023B	4053B	4516B	4724B	
4024B	4066B	4518B	4725B	

Available Soon:

4022B	4072B	4519B	4553B	4735B
4031B	4082B	4522B	4583B	4736B
4034B	4093B	4526B	4708B	
4047B	4514B	4531B	4722B	
4067B	4515B	4532B	4734B	

TABLE 1

	PARAMETER	TEMP. RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS T_{LOW}* MIN	T_{LOW}* MAX	+25°C MIN	+25°C MAX	T_{HIGH}* MIN	T_{HIGH}* MAX	UNITS
I_{DD}	Quiescent Device Current	Mil	5			0.25		0.25		7.5	
			10	$V_{IN} = V_{SS}$ or V_{DD}		0.5		0.5		15	μA
			15			1.0		1.0		30	
	GATES	Comm	5	All valid input		1.0		1.0		7.5	
			10	combinations		2.0		2.0		15	μA
			15			4.0		4.0		30	
	BUFFERS, FLIP-FLOPS	Mil	5			1.0		1.0		30	
			10	$V_{IN} = V_{SS}$ or V_{DD}		2.0		2.0		60	μA
			15			4.0		4.0		120	
		Comm	5	All valid input		4		4		30	
			10	combinations		8		8		60	μA
			15			16		16		120	
	MSI	Mil	5			5		5		150	
			10	$V_{IN} = V_{SS}$ or V_{DD}		10		10		300	μA
			15			20		20		600	
		Comm	5	All valid input		20		20		150	
			10	combinations		40		40		300	μA
			15			80		80		600	
V_{OL}	Output LOW Voltage	All	5			0.05		0.05		0.05	
			10	$V_{IN} = V_{SS}$ or V_{DD}		0.05		0.05		0.05	V
			15	$\|I_O\| < 1$ μA		0.05		0.05		0.05	
V_{OH}	Output HIGH Voltage	All	5		4.95		4.95		4.95		
			10	$V_{IN} = V_{SS}$ or V_{DD}	9.95		9.95		9.95		V
			15	$\|I_O\| < 1$ μA	14.95		14.95		14.95		
V_{IL}	Input LOW Voltage	All	5	$V_O = 0.5$ V or 4.5 V		1.5		1.5		1.5	
			10	$V_O = 1.0$ V or 9.0 V		3.0		3.0		3.0	V
			15	$V_O = 1.5$ V or 13.5 V $\|I_O\| < 1$ μA		4.0		4.0		4.0	
V_{IH}	Input HIGH Voltage	All	5	$V_O = 0.5$ V or 4.5 V	3.5		3.5		3.5		
			10	$V_O = 1.0$ V or 9.0 V	7.0		7.0		7.0		V
			15	$V_O = 1.5$ V or 13.5 V $\|I_O\| < 1$ μA	11.0		11.0		11.0		
I_{OL}	Output LOW (Sink) Current	Mil	5	$V_O = 0.4$ V, $V_{IN} = 0$ or 5 V	0.64		0.51		0.36		
			10	$V_O = 0.5$ V, $V_{IN} = 0$ or 10 V	1.6		1.3		0.9		mA
			15	$V_O = 1.5$ V, $V_{IN} = 0$ or 15 V	4.2		3.4		2.4		
		Comm	5	$V_O = 0.4$ V, $V_{IN} = 0$ or 5 V	0.52		0.44		0.36		
			10	$V_O = 0.5$ V, $V_{IN} = 0$ or 10 V	1.3		1.1		0.9		mA
			15	$V_O = 1.5$ V, $V_{IN} = 0$ or 15 V	3.6		3.0		2.4		
I_{OH}	Output HIGH (Source) Current	Mil	5	$V_O = 4.6$ V, $V_{IN} = 0$ or 5 V	−0.25		−0.2		−0.14		
			10	$V_O = 9.5$ V, $V_{IN} = 0$ or 10 V	−0.62		−0.5		−0.35		mA
			15	$V_O = 13.5$ V, $V_{IN} = 0$ or 15 V	−1.8		−1.5		−1.1		
		Comm	5	$V_O = 4.6$ V, $V_{IN} = 0$ or 5 V	−0.2		−0.16		−0.12		
			10	$V_O = 9.5$ V, $V_{IN} = 0$ or 10 V	−0.5		−0.4		−0.3		mA
			15	$V_O = 13.5$ V, $V_{IN} = 0$ or 15 V	−1.4		−1.2		−1.0		
I_{IN}	Input Current	Mil	15	$V_{IN} = 0$ or 15 V		±0.1		±0.1		±1.0	μA
		Comm	15	$V_{IN} = 0$ or 15 V		±0.3		±0.3		±1.0	μA
C_{IN}	Input Capacitance per Unit Load	All	–	Any input				7.5			pF

*T_{LOW} = −55°C for Military Temp. Range device, −40°C for Commercial Temp. Range device

*T_{HIGH} = +125°C for Military Temp. Range device, +85°C for Commercial Temp. Range device

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} — (Input Current) — The current flowing into a device at specified input voltage and V_{DD}.

I_{OH} — (Output HIGH Current) — The drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} — (Output LOW Current) — The drive current flowing into the device at specified LOW output voltage and V_{DD}.

I_{DD} — (Quiescent Power Supply Current) — The current flowing into the V_{DD} pin at specified input and V_{DD} conditions.

I_{OZH} — (Output OFF HIGH Current) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{OZL} — (Output OFF LOW Current) — The leakage current flowing out of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{IL} — (Input LOW Current) — The current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} — (Input HIGH Current) — The current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} — (Quiescent Power Supply LOW Current) — The current flowing into the V_{DD} pin with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} — (Quiescent Power Supply HIGH Current) — The current flowing into the V_{DD} pin with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z — (OFF State Leakage Current) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified output voltage and V_{DD}.

VOLTAGES — All voltages are referenced to V_{SS} (or V_{EE}) which is the most negative potential applied to the device.

V_{DD} — (Drain Voltage) — The most positive potential on the device.

V_{IH} — (Input HIGH Voltage) — The range of input voltages that represents a logic HIGH level in the system.

V_{IL} — (Input LOW Voltage) — The range of input voltages that represents a logic LOW level in the system.

V_{IH} (min) — (Minimum Input HIGH Voltage) — The minimum allowed input HIGH level in a logic system.

V_{IL} (max) — (Maximum Input LOW Voltage) — The maximum allowed input LOW level in a system.

V_{OH} — (Output HIGH Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} — (Output LOW Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{SS} — (Source Voltage) — For a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.

V_{EE} — (Source Voltage) — One of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supplies, the most negative power supply used as a reference level for other voltages.

ANALOG TERMS

R_{ON} — (ON Resistance) — The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V_{DD}.

ΔR_{ON} — ("Δ" ON Resistance) — The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and V_{DD}.

AC SWITCHING PARAMETERS

f_{MAX} — (Toggle Frequency/Operating Frequency) — The maximum rate at which clock pulses may be applied to a sequential circuit with the output of the circuit changing between 30% of V_{DD} and 70% of V_{DD}. Above this frequency the device may cease to function. See Figure 4-17.

t_{PLH} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level. See Figure 3-1.

t_{PHL} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level. See Figure 3-1.

t_{TLH} — (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform, normally 10% to 90% of V_{DD}, which is changing from LOW to HIGH. See Figure 4-16.

t_{THL} — (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform, normally 90% to 10% of V_{DD}, which is changing from HIGH to LOW. See Figure 4-16.

t_w — (Pulse Width) — The time between 50% amplitude points on the leading and trailing edges of pulse.

t_h — (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s — (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} — (3-State Output Disable Time, HIGH to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} drop on the output voltage waveform of a 3-state device, with the output changing from the defined HIGH level to a high impedance OFF state.

t_{PLZ} — (3-State Output Disable Time, LOW to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} rise on the output voltage waveform of a 3-state device, with the output changing from the defined LOW level to a high impedance OFF state.

t_{PZH} — (3-State Output Enable Time, Z to HIGH) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined HIGH level.

t_{PZL} — (3-State Output Enable Time, Z to LOW) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined LOW level.

t_{rec} — (Recovery Time) — The time between the end of an overriding asynchronous input, typically a Clear or Reset input, and the earliest allowable beginning of a synchronous control input, typically a Clock input, normally measured at 50% points on both input voltage waveforms.

t_{CW} — (Clock Period) — The time between 50% amplitude points on the leading edges of a clock pulse.

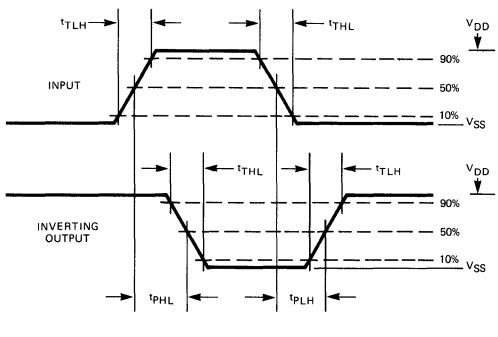


Fig. 4-16
Propagation Delay, Transition Time

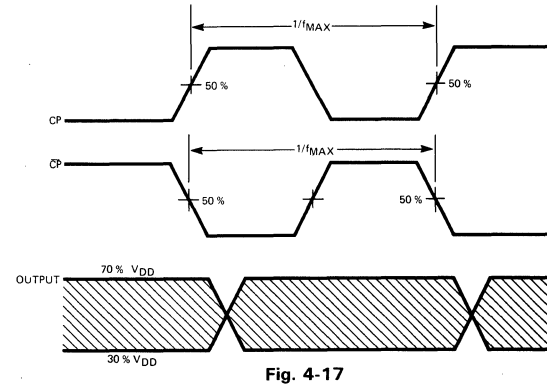


Fig. 4-17
Maximum Operating Frequency

4700
SERIES CMOS FAMILY CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Non-operating) above which useful life may be impaired. All voltages are referenced to V_{SS}:

Supply Voltage V_{DD}	-0.5 to 18 V
Voltage on any Input	-0.5 to V_{DD} +0.5 V
Current into any Input	±10 mA
Maximum Power Dissipation	400 mW
Storage Temperature	-65°C to +150°C
Pin Temperature (Soldering, 10 s)	300°C

RECOMMENDED OPERATING CONDITIONS

Fairchild CMOS will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} equal to 5, 10 and 15 V. Where low power dissipation is required, the lowest power supply voltage, consistent with required speed, should be used. For larger noise immunity, higher power supply voltages should be specified. Because of its wide operating range, power supply regulation and filtering are less critical than with other types of logic. The lower limit of supply regulation is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic.The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic.

Unused inputs must by connected to V_{DD}, V_{SS} or another input.

Care should be used in handling CMOS devices; large static charges may damage the device.

Operating temperature ranges are -40°C to +85°C for Commercial and -55°C to +125°C for Military.

PARAMETER	4700XC			4700XM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage, V_{DD}	3		15	3		15	V
Operating Free Air Temperature Range	−40	+25	+85	−55	+25	+125	°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Ordering Information section.

DC CHARACTERISTICS FOR THE 4700 MACROLOGIC SERIES CMOS FAMILY

Parametric Limits listed below are guaranteed for the entire Fairchild CMOS Family unless otherwise specified on the individual data sheets.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	3.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			1.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	4.95			V	MIN, 25°C	I_{OH} < 1 µA, Inputs at 0 or 5 V per the Logic Function or Truth Table
		4.95				MAX	
		4.5			V	All	I_{OH} < 1 µA, Inputs at 1.5 or 3.5 V
V_{OL}	Output LOW Voltage			0.05	V	MIN, 25°C	I_{OL} < 1 µA, Inputs at 0 or 5 V per the Logic Function or Truth Table
				0.05		MAX	
				0.5	V	All	I_{OL} < 1 µA, Inputs at 1.5 or 3.5 V
I_{OH}	Output HIGH Current	−1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V; Inputs at 0 or 5 V per the Logic Function or Truth Table
		−1.0				MAX	
		−0.7			mA	MIN, 25°C	V_{OUT} = 4.5 V
		−0.4				MAX	
I_{OL}	Output LOW Current	1.0			mA	MIN	V_{OUT} = 0.4 V
		0.8				25°C	
		0.4				MAX	
C_{IN}	Input Capacitance Per Unit Load			7.5	pF	25°C	Any Input

DC CHARACTERISTICS: V_{DD} = 10 V, V_{SS} = 0 V

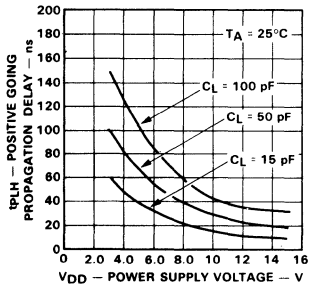
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage	7.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage			3.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	9.95			V	MIN, 25°C	I_{OH} < 1 μA, Inputs at 0 or 10 V per the Logic Function or Truth Table
		9.95				MAX	
		9.0			V	All	I_{OH} < 1 μA, Inputs at 3 or 7 V
V_{OL}	Output LOW Voltage			0.05	V	MIN, 25°C	I_{OL} < 1 μA, Inputs at 0 or 10V per the Logic Function or Truth Table
				0.05		MAX	
				1.0	V	All	I_{OL} < 1 μA, Inputs at 3 or 7 V
I_{OH}	Output HIGH Current	−1.4			mA	MIN, 25°C	V_{OUT} = 9.5 V; Inputs at 0 or 10 V per the Logic Function or Truth Table
		−0.8				MAX	
I_{OL}	Output LOW Current	2.6			mA	MIN	V_{OUT} = 0.5 V; Inputs at 0 or 10 V per the Logic Function or Truth Table
		2.0				25°C	
		1.2				MAX	
C_{IN}	Input Capacitance Per Unit Load			7.5	pF	25°C	Any Input

DC CHARACTERISTICS: V_{DD} = 15 V, V_{SS} = 0 V

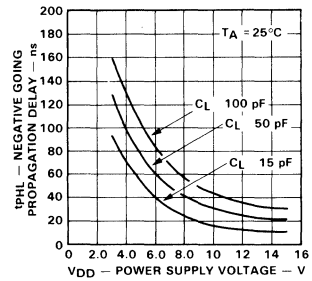
SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		11.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				4.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		14.95			V	MIN, 25°C	I_{OH} < 1 μA, Inputs at 0 or 15 V per the Logic Function or Truth Table
			14.95				MAX	
			13.5			V	All	I_{OH} < 1 μA, Inputs at 4 or 11 V
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25°C	I_{OL} < 1 μA, Inputs at 0 or 15 V per the Logic Function or Truth Table
					0.05		MAX	
					1.5	V	All	I_{OL} < 1 μA, Inputs at 4 or 11 V
I_{IN}	Input Current	XC			0.3	μA	MIN, 25°C	Pin under Test at 0 or 15 V; All other inputs simultaneously at 0 or 15 V
					1.0		MAX	
		XM			0.1	μA	MIN, 25°C	
					1.0		MAX	
I_{OH}	Output HIGH Current		−2.2			mA	MIN, 25°C	V_{OUT} = 14.5 V; Inputs at 0 or 15 V per the Logic Function or Truth Table
			−1.4				MAX	
I_{OL}	Output LOW Current		3.6			mA	MIN, 25°C	V_{OUT} = 0.5 V
			2.0				MAX	
C_{IN}	Input Capacitance Per Unit Load				7.5	pF	25°C	Any Input

TYPICAL 4700 SERIES CHARACTERISTICS

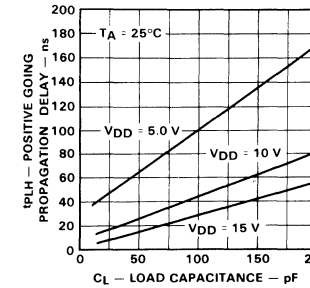
POSITIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE



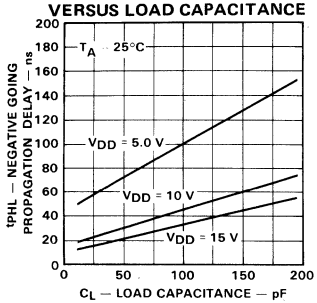
NEGATIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE



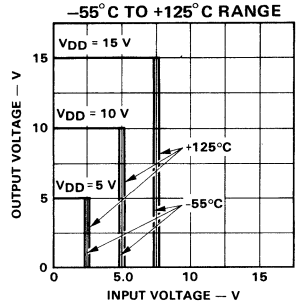
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE



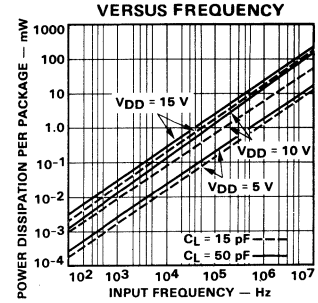
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE



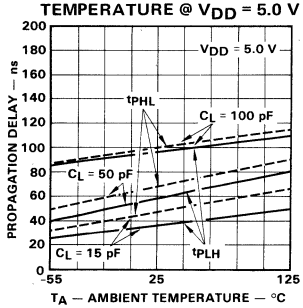
VOLTAGE TRANSFER CHARACTERISTICS OVER −55°C TO +125°C RANGE



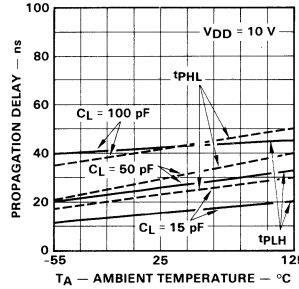
GATE POWER DISSIPATION VERSUS FREQUENCY



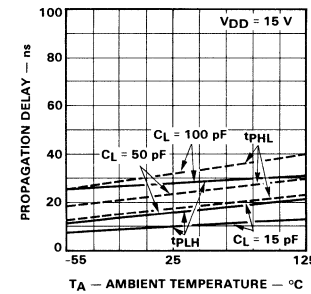
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 5.0 V



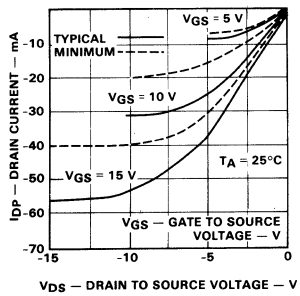
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 10 V



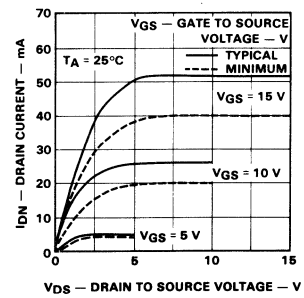
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 15 V



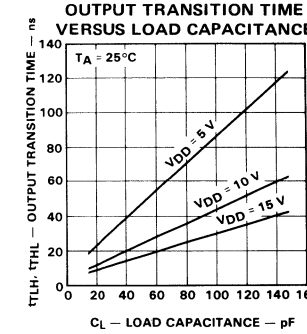
p-CHANNEL DRAIN CHARACTERISTICS



n-CHANNEL DRAIN CHARACTERISTICS

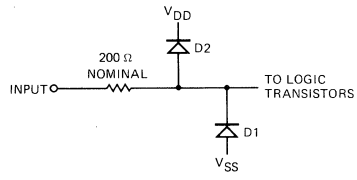


OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



4

INPUT PROTECTION CIRCUIT



INPUT CIRCUITRY

All inputs are protected by the network of Figure 3-13; a series input resistor plus diodes D1 and D2 clamp input voltages between V_{SS} and V_{DD}. Forward conduction of these diodes is typically 0.9 V at 1 mA. When V_{SS} or V_{DD} is not connected, avalanche breakdown of the diodes limit input voltage; D1 typically breaks down at 20 V, D2 at 20 V. In normal logic operation the diodes never conduct, but for certain special applications such as oscillators, circuit operation may actually depend on diode conduction. Operation in this mode is permissible so long as input currents do not exceed 10 mA.

Input capacitance is typically 5 pF across temperature for any input.

4702/4702B

PROGRAMMABLE BIT-RATE GENERATOR

FAIRCHILD CMOS MACROLOGIC

DESCRIPTION – The 4702 Bit-Rate Generator provides the necessary clock signals for digital data transmission systems, such as Universal Asynchronous Receiver and Transmitter circuits (UARTs). It generates any of the 14 commonly used bit rates using an on-chip crystal oscillator, but its design also provides for easy and economical multichannel operation, where any of the possible frequencies must be made available on any output channel.

One 4702 can control up to eight output channels. When more than one bit-rate generator is required, they can still be operated from one crystal.

- **PROVIDES 14 COMMONLY USED BIT-RATES**
- **ONE 4702 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS**
- **USES 2.4576 MHz INPUT FOR STANDARD FREQUENCY OUTPUTS (16 TIMES BIT RATE)**
- **CONFORMS TO EIA RS-404**
- **ON-CHIP INPUT PULL UP CIRCUITS**
- **TTL COMPATIBLE–OUTPUTS WILL SINK 1.6 mA**
- **INITIALIZATION CIRCUIT FACILITIES DIAGNOSTIC FAULT ISOLATION**
- **LOW POWER DISSIPATION – 1.35 mA POWER DISSIPATION AT 5 V AND 2.4576 MHz**
- **16-PIN DUAL IN-LINE PACKAGE**

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	$\bar{E}_{CP}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎺⎍	Reset During First CP = HIGH Time

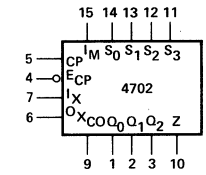
H = HIGH Level
L = LOW Level
X = Don't Care
⎍⎺⎍ = 1st HIGH Level Clock Pulse After $\bar{E}_{CP}$ Goes LOW
⎍⎍⎍ Clock Pulses

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

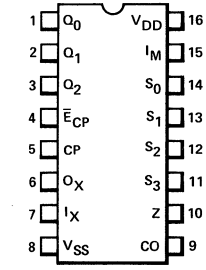
S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



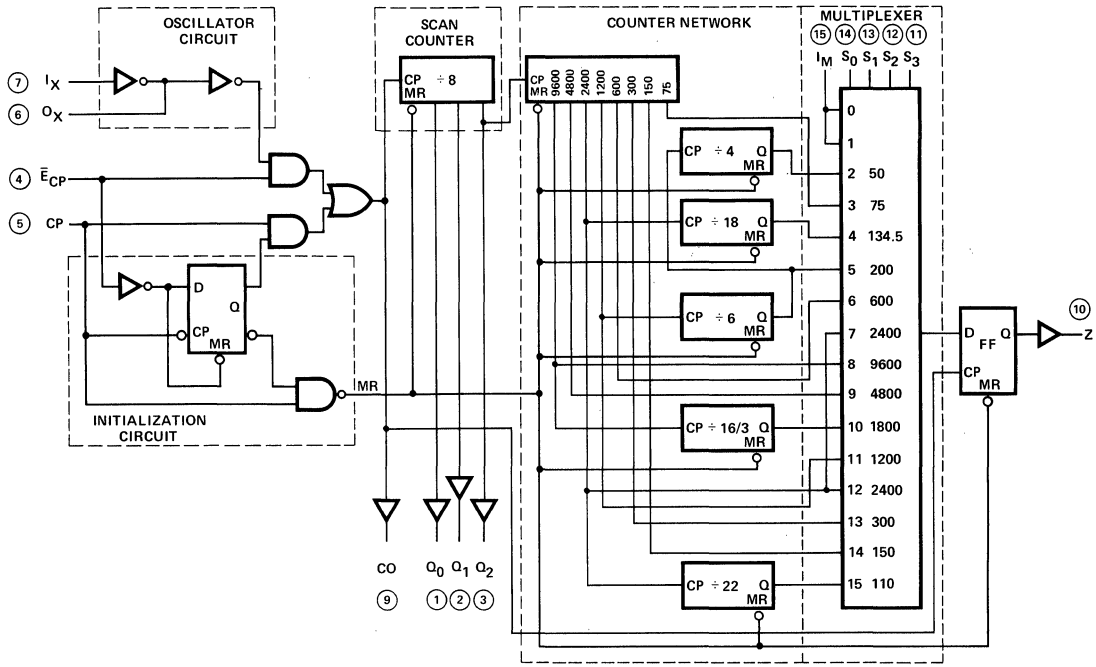
NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP	External Clock Input
$\bar{E}_{CP}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

4

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

FUNCTIONAL DESCRIPTION – Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud interfacing with electromechanical devices, to 9600 baud for high speed modems. Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate that is a multiple of the incoming bit rate. Popular MOS-LSI UART circuits use a clock that is 16 times the transmitted bit rate. The 4702 can generate 14 standardized clock rates from one common high frequency input.

The 4702 contains the following five functional subsystems which are discussed in detail below:

1. An Oscillator Circuit with associated gating.
2. A prescaler used as Scan Counter for multichannel operation (described in the applications section).
3. A Counter Network to generate the required standardized frequencies.
4. An output Multiplexer (frequency selector) with resynchronizing output flip-flop.
5. An Initialization (reset) Circuit.

Oscillator – For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576 MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will obviously result in a proportionally lower output frequency.

The 4702 can be driven from two alternate clock sources: (1) When the $\overline{E}_{CP}$ (active LOW External Clock Enable) input is LOW, the CP input is the clock source. (2) When the $\overline{E}_{CP}$ input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input, is the clock source.

Prescaler (Scan Counter) – The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0, Q_1, and Q_2. This prescaler is of no particular advantage in single frequency applications, but it is essential for the simple economical multichannel scheme described in the Applications section of this data book.

Counter Network – The prescaler output Q_2 is a square wave of 1/8 the input frequency and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576 MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6 kHz = 153.6 kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of –0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of –0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78%, irrespective of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer – The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs (Q_0-Q_2). *Table 2* lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, nonstandardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) – The initialization circuit generates a common master reset signal for all flip-flops in the 4702. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E}_{CP}$ input goes LOW. When $\overline{E}_{CP}$ is HIGH, selecting the Crystal input, CP must be LOW. A HIGH level on CP would apply a continuous reset.

All inputs to the 4702, except I_X have on-chip pull-up circuits which improve TTL compatibility and eliminate the need to tie a permanently HIGH input to V_{DD}.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input High Voltage
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.95			V	MIN, 25°C	$I_{OH} < 1\ \mu A$, Inputs at 0 or 5 V per the Logic Function or Truth Table
			4.95				MAX	
			4.5				All	$I_{OH} < 1\ \mu A$, Inputs at 1.5 or 3.5 V
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25°C	$I_{OL} < 1\ \mu A$, Inputs at 0 or 5 V per the Logic Function or Truth Table
					0.05		MAX	
					0.5		All	$I_{OL} < 1\ \mu A$, Inputs at 1.5 or 3.5 V
I_L (See Note 5)	Input LOW Current for Input I_X	XC			0.3	μA	MIN, 25°C	Pin under Test at 0 V All other Inputs Simultaneously at 5 V
					1.0		MAX	
		XM			0.1	μA	MIN, 25°C	
					1.0		MAX	
	Input LOW Current for all Other Inputs	XC		−30		μA	25°C	
		XM		−30				
I_{IH}	Input HIGH Current for all Inputs	XC			0.3	μA	MIN, 25°C	Pin Under Test at 5 V All other Inputs Simultaneously at 0 V
					1.0		MAX	
		XM			0.1	μA	MIN, 25°C	
					1.0		MAX	
I_{OH}	Output HIGH Current for Output O_X		−0.3			mA	MIN, 25°C	V_{OUT} = 4.5 V Inputs at 0 or 5 V per Logic Function or Truth Table
			−0.1				MAX	
	Output HIGH Current for Output O_X		−1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V
			−1.0				MAX	
			−0.5			mA	MIN, 25°C	V_{OUT} = 4.5 V
			−0.3				MAX	
I_{OL}	Output LOW Current for Output O_X		0.2			mA	MIN, 25°C	V_{OUT} = 0.4 V
			0.1				MAX	
	Output LOW Current for all Other Outputs		3.2			mA	MIN, 25°C	
			1.6				MAX	
I_{DD}	Quiescent Power Supply Current	XC			100	μA	MIN, 25°C	$\overline{E}_{CP} = V_{DD}$, CP = 0 V, All other Inputs at 0 V or V_{DD}
					1000		MAX	
		XM			10	μA	MIN, 25°C	
					150		MAX	

See Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} = 5.0 V, V_{SS} = 0 V, T_A = 25°C (Note 1)

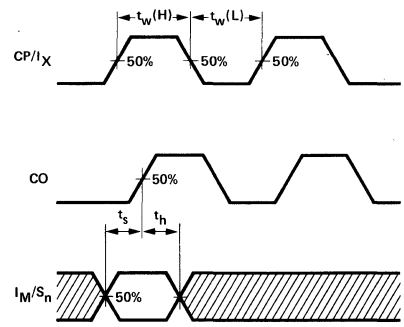
SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_X to CO		150 125	300 250	ns	C_L = 15 pF Input Transition Times ≤ 20 ns $C_L \leq 7$ pF ON O_X
t_{PLH} t_{PHL}	Propagation Delay CP to CO		112 100	215 195	ns	
t_{PLH} t_{PHL}	Propagation Delay CO to Q_n		45 40	Note 6	ns	
t_{PLH} t_{PHL}	Propagation Delay CO to Z		35 30	75 65	ns	
t_{TLH} t_{THL}	Output Transition Time (Except O_X)		40 20	80 40	ns	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} = 5.0 V, V_{SS} = 0.V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay I_X to CO		175 135	350 275	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to CO		130 110	260 220	ns	C_L = 50 pF Input Transition Times ≦ 20 ns C_L ≦ 7 pF on O_X
t_{PLH} t_{PHL}	Propagation Delay CO to Q_n		53 45	Note 6	ns	
t_{PLH} t_{PHL}	Propagation Delay CO to Z		37 32	85 75	ns	
t_{TLH} t_{THL}	Output Transition Time (Except O_X)		80 35	160 75	ns	
t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0	185 −182		ns	
t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0	−190 −182		ns	C_L = 15 pF Input Transition Times ≦ 20 ns C_L ≦ 7 pF on O_X
$t_wCP(L)$ $t_wCP(H)$	Minimum Clock Pulse Width LOW and HIGH	120 120	60 60		ns	
$t_wI_X(L)$ $t_wI_X(H)$	Minimum I_X Pulse Width LOW and HIGH	160 160	75 75		ns	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described under 4700 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L) Set-Up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. The first HIGH level Clock Pulse after $\overline{E}_{CP}$ goes LOW must be at least 350 ns long to guarantee reset of all Counters.
4. It is recommeded that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15 μs and V_{PO} pin should be decoupled.
5. Input current and quiescent power supply current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
6. For multichannel operation, propagation delay, CO to Q_n, plus set-up time, select to CO, is guaranteed to ⩽367 ns.

SWITCHING WAVEFORMS



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES, SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

APPLICATIONS

Single Channel Bit Rate Generator – *Figure 1* shows the simplest application of the 4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The bit rate output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals these five bit rates are adequate.

Simultaneous Generation of Several Bit Rates:
Fixed Programmed Multichannel Operation – Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one 4702 and one 93L34 8-Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter outputs back to the Select inputs of the multiplexer causes the 4702 to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter outputs, reconverts the multiplexed single output (Z) of the F4702 into eight parallel output frequency signals. In the simple scheme of *Figure 2*, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0:	110 Baud,	Q_1:	9600 Baud,	Q_2:	4800 Baud,	Q_3:	1800 Baud,
Q_4:	1200 Baud,	Q_5:	2400 Baud,	Q_6:	300 Baud,	Q_7:	150 Baud.

Other bit rate combinations can be generated by changing the Scan Counter to selector interconnection or by inserting logic gates into this path.

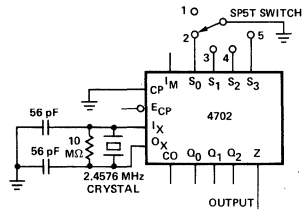
Fully Programmable Multichannel Operation – Figure 3 shows a fully programmable 8-channel bit rate generator system that, under computer control, generates arbitrarily assigned bit rates on all eight outputs simultaneously. The basic operation is similar to the previously described fixed programmed system, but two 9LS170 4 x 4 Register File MSI packages are connected as programmable look-up tables between the Scan Counter outputs (Q_0 to Q_2) and the multiplexer Select inputs (S_0 to S_3). The content of this 8-word by 4-bit memory determines which frequency appears at what output.

19200 Baud Operation –Though a 19200 Baud signal is not internally routed to the multiplexer, the 4702 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code 0 or 1. An additional 2-input NAND gate can be used to retain the "Zero Baud" feature on select code 0. Any multichannel operation that involves 19200 Baud must be limited to four outputs as shown in *Figure 4*. Only the two least significant Scan Counter outputs are used, so that the scan is completed within one half period of the 19200 output frequency.

Clock Expansion –One 4702 can control up to eight output channels. For more than eight channels, additional bit rate generators are required. These bit rate generators can all be run from the same crystal or clock input. *Figure 5* shows one possible expansion scheme. One 4702 is provided with a crystal. All other devices derive their clock from this master. *Figure 6* shows a different scheme where the master clock output feeds into the I_X input of all slaves and all $\overline{E}_{CP}$ inputs are normally held HIGH. This scheme retains the reset feature and the selection between two different clock sources of the basic 4702 circuit.

During normal operation, the common $\overline{E}_{CP}$ line is HIGH and the common clock line (CP) is LOW. For diagnostic purposes the common $\overline{E}_{CP}$ is forced LOW. This deselects the crystal frequency and initiates the diagnostic mode. When CP goes HIGH for the first time, all 4702s are reset through their individual on-chip initialization circuitry. Subsequent LOW-to-HIGH clock transitions on the common CP line advance the scan counter, causing all 4702s to operate synchronously.

TYPICAL APPLICATIONS



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

Fig. 1
SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

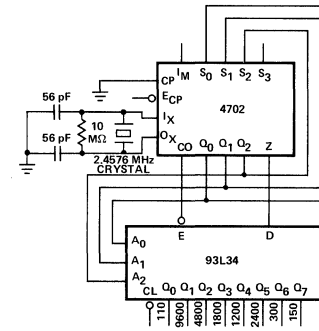


Fig. 2
BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

TYPICAL APPLICATIONS (Cont'd)

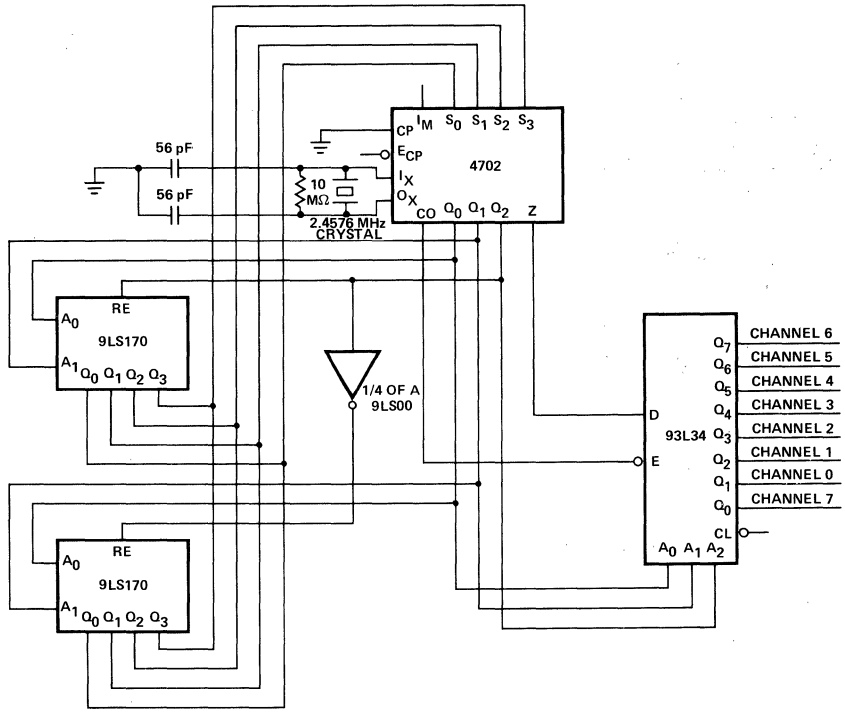


Fig. 3

FULLY PROGRAMMABLE 8-CHANNEL BIT RATE GENERATOR SYSTEM

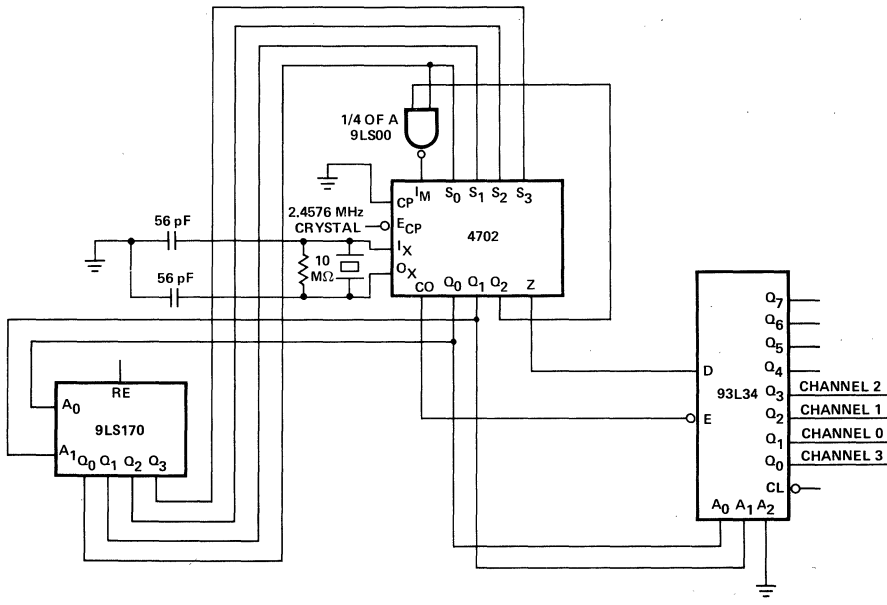


Fig. 4

FULLY PROGRAMMABLE 4-CHANNEL BIT RATE GENERATOR SYSTEM WITH THE 19.2k BAUD FEATURE

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TYPICAL APPLICATIONS (Cont'd)

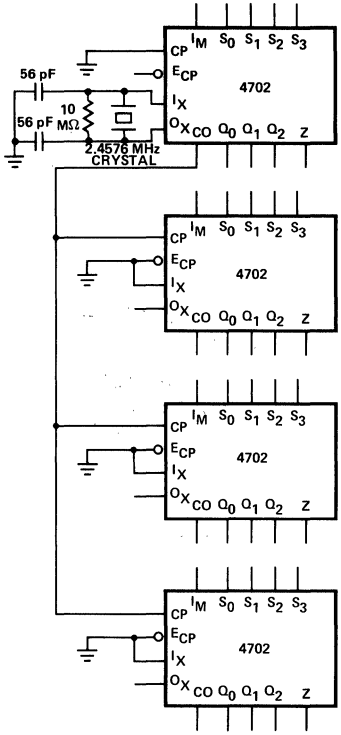


Fig. 5
CASCADE CLOCK EXPANSION SCHEME

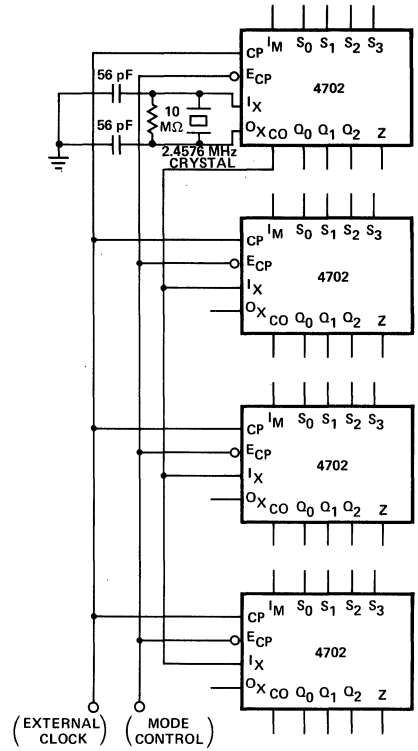


Fig. 6
TANDEM CLOCK EXPANSION SCHEME

CRYSTAL SPECIFICATION RECOMMENDATIONS – Table 3 is a convenient listing of recommended crystal specifications. Crystal manufacturers are also listed below.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	–6.0 dB (Min)
Type of Operation	Parallel
Load Capacitance	32 pF ±0.5

CRYSTAL MANUFACTURERS

CTS Knights, Inc.
Sandwich, Ill. 60548
(815) 786-8411
Crystal #F1004

X - Tron Electronics
1869 National Ave.
Hayward, Calif.
(415) 783-2145

Erie Frequency Control
499 Lincoln St.
Carlisle, Pa. 17013
(717) 249-2232

International Crystal Mfg. Company
10 No. Lee
Oklahoma City, Okla. 73102
(405) 236-3741

Sentry Manufacturing Co.
Crystal Park
Chickasha, Oklahoma 73018
(405) 224-6780
Crystal # SGP 6-2.4576 or
Crystal # SGP-7-2.4576

4703/4703B

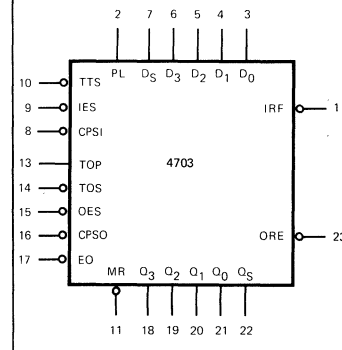
FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

FAIRCHILD CMOS MACROLOGIC

DESCRIPTION — The 4703 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.
The 4703 has 3-state outputs which provide added versatility and is fully compatible with all CMOS families.

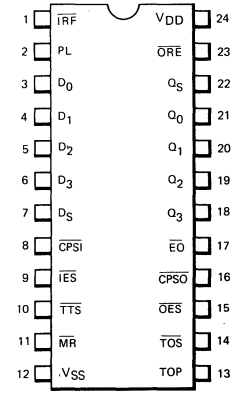
- **2.3 MHz SERIAL OR PARALLEL DATA RATE, TYPICALLY**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE OUTPUTS**
- **FULLY COMPATIBLE WITH ALL CMOS FAMILIES**
- **SLIM 24-PIN PACKAGE**

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



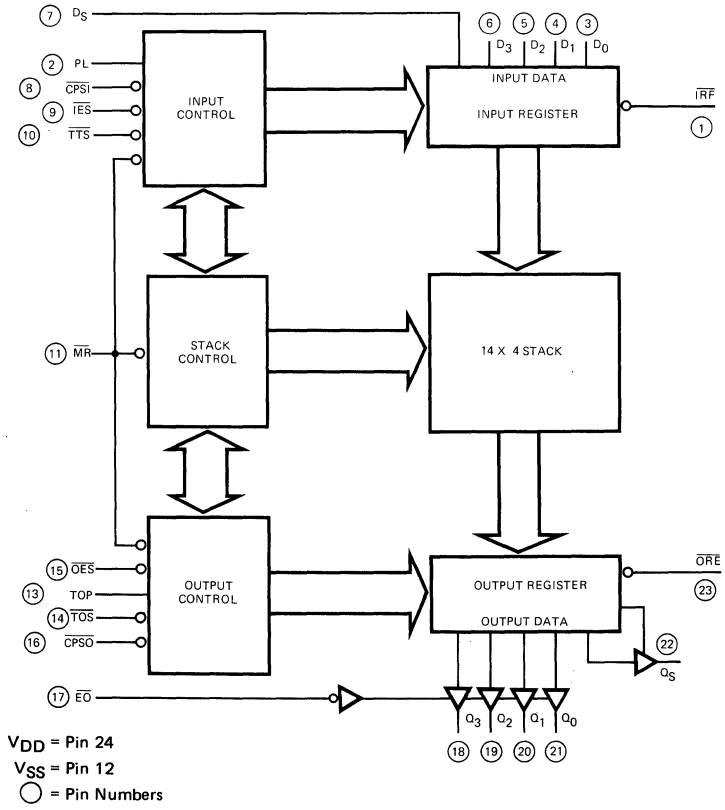
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$D_0 - D_3$	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
$Q_0 - Q_3$	Parallel Data Outputs
Q_S	Serial Data Output

4

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the block diagram the 4703 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry – A HIGH on the PL input loads the D_0 – D_3 inputs into the F_0 – F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

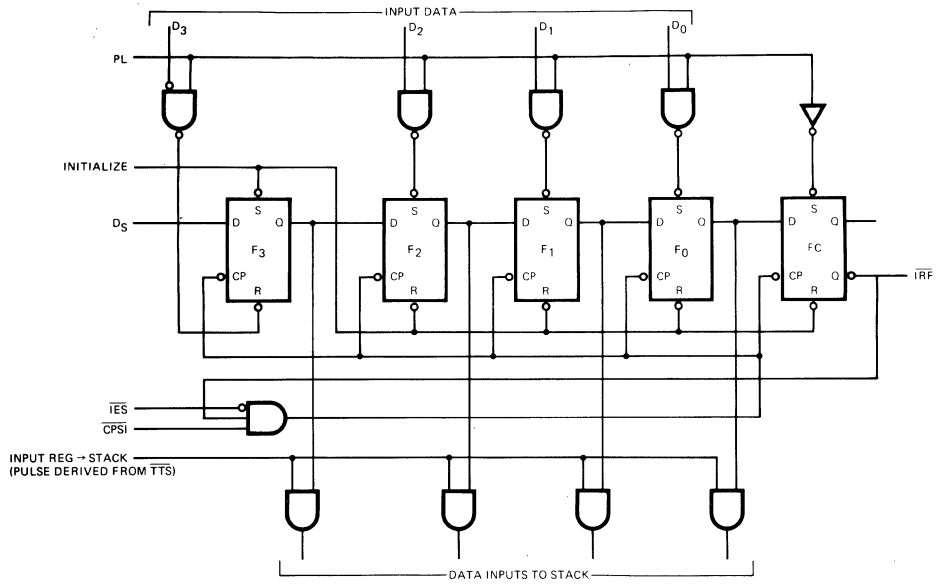


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry – Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0 – F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 4703 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

Transfer to the Stack –The outputs of Flip-Flops F_0 – F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 4703, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

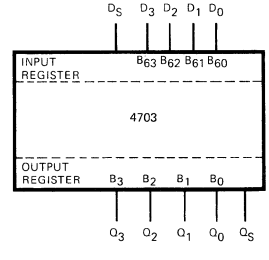


Fig. 2
FINAL POSITIONS IN A 4703 RESULTING FROM A 64-BIT SERIAL TRAIN

4

EXPANSION

Vertical Expansion - The 4703 may be vertically expanded to store more words without external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4.* Using the same technique, any FIFO of (15n + 1) words by four bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 4703's flexibility for serial/parallel input and output. For other expansion schemes, refer to the Applications section of this book.

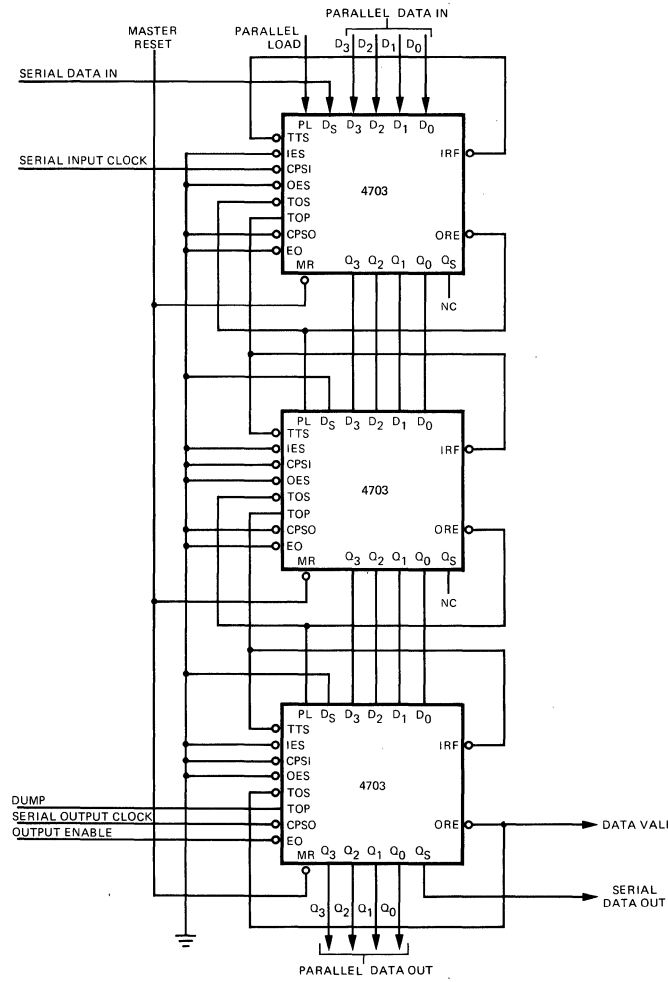


Fig. 4
A VERTICAL EXPANSION SCHEME

Output Register (Data Extraction) - The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

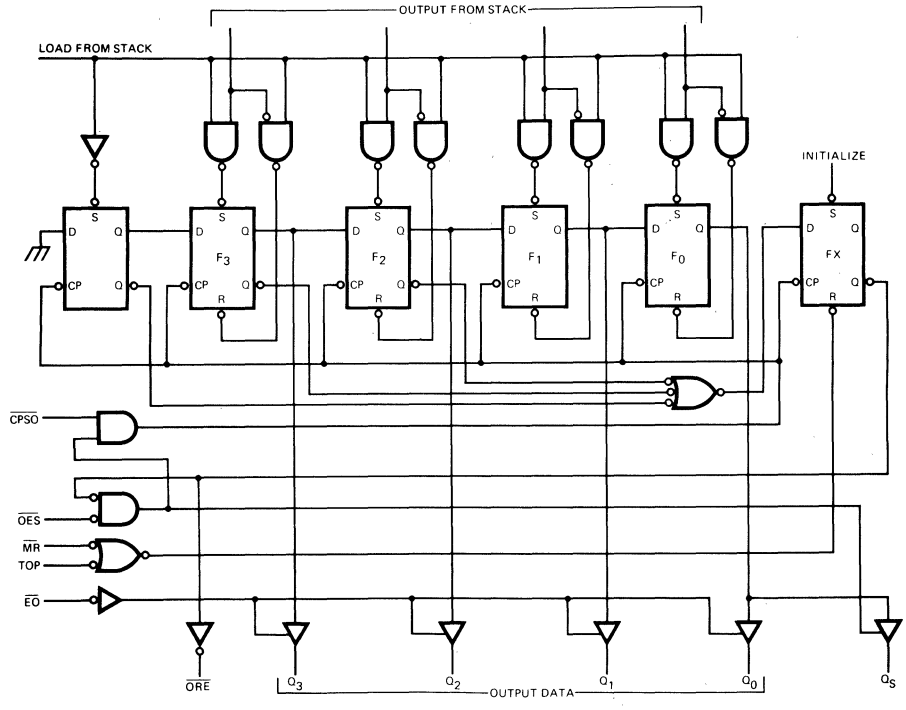


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction - When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. $\overline{TOS}$ should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, ORE remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction - When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Horizontal Expansion – The 4703 can also be horizontally expanded to store long words (in multiples of four bits) without external logic. The interconnections necessary to form a 16-word by 12-bit FIFO are shown in *Figure 5.* Using the same technique, any FIFO of 16 words by 4n bits can be constructed, where n is the number of devices. The $\overline{IRF}$ output of the right most device (most significant device) is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 4703's flexibility for serial/parallel input and output.

It should be noted that this form of horizontal expansion extracts a penalty in speed. A single FIFO is guaranteed to operate at 10 MHz; an array of four FIFOs connected in the above manner is guaranteed at 4.3 MHz. An expansion scheme that provides higher speed but requires additional components is shown in the Applications section of this book.

Horizontal and Vertical Expansion – The 4703 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6.* Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 7 and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6.* The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9.*

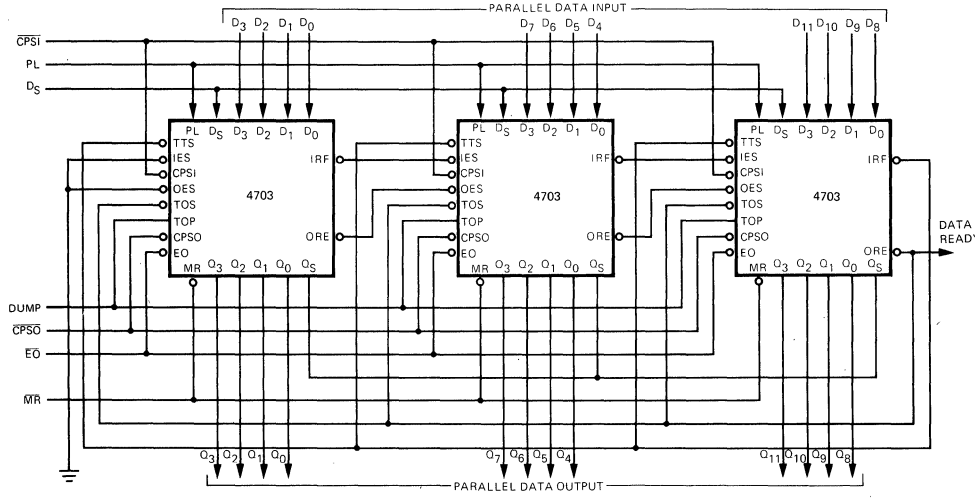


Fig. 5
A HORIZONTAL EXPANSION SCHEME

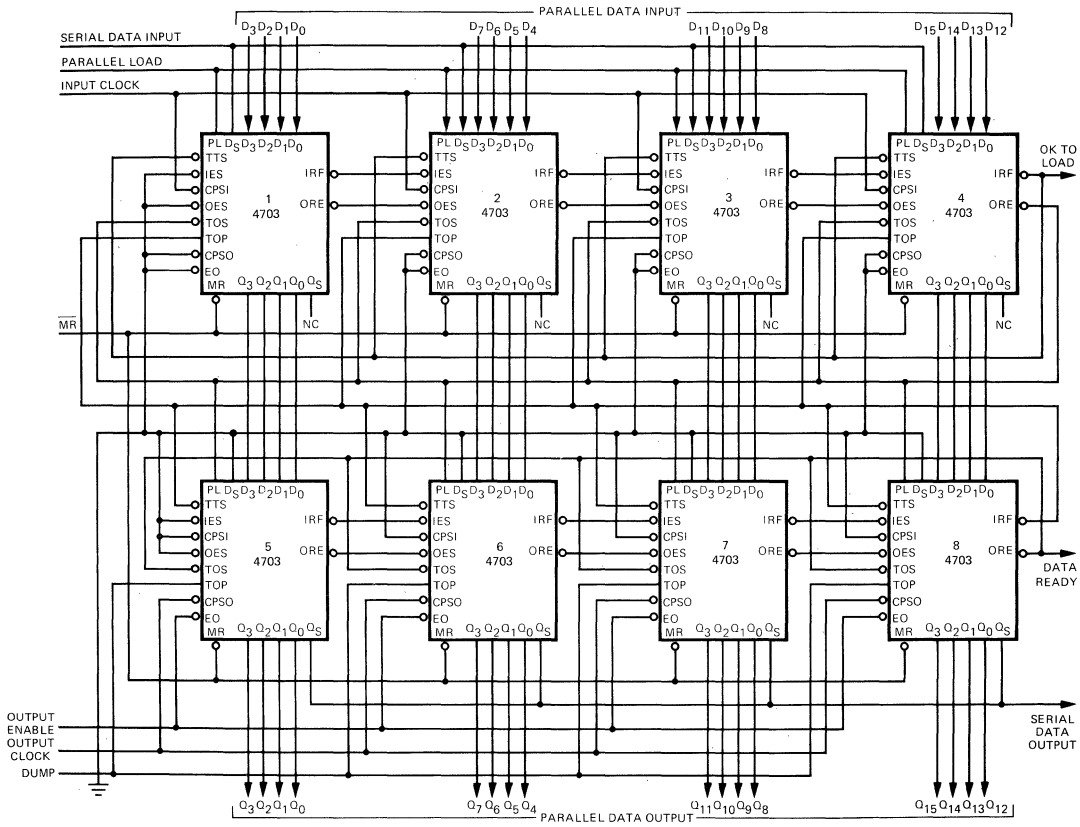


Fig. 6
A 31 X 16 FIFO ARRAY

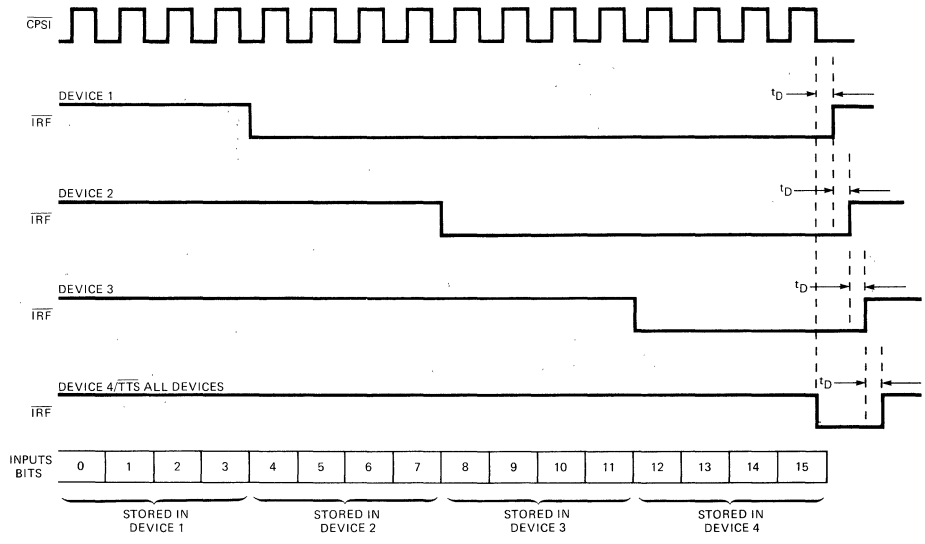


Fig. 7
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

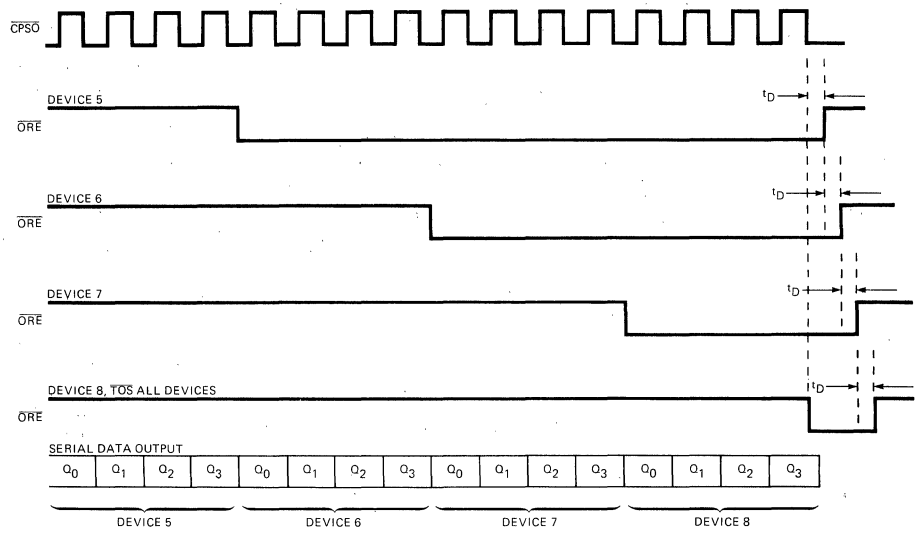


Fig. 8
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

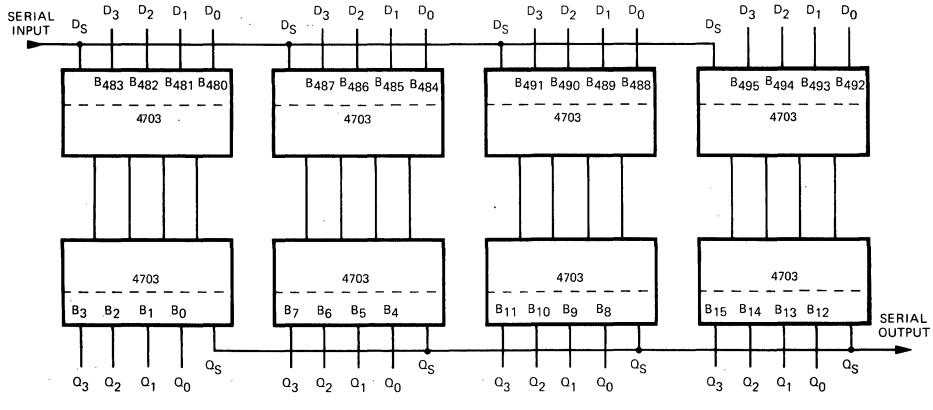


Fig. 9
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 4703 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 4703 array of *Figure 6* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 4703 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

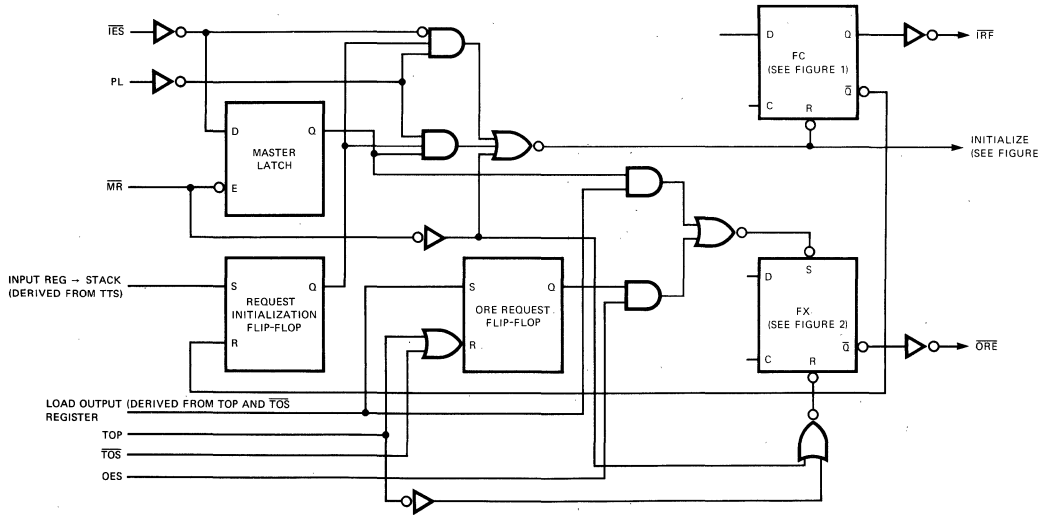


Fig. 10
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF HIGH Current	XC			0.5			1.0			0.2	μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60			12		MAX	
		XM			0.05			0.1			0.02		MIN, 25°C	
					3.0			6.0			1.2		MAX	
I_{OZL}	Output OFF LOW Current	XC			−0.5			−1.0			−0.2	μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60			−12		MAX	
		XM			−0.05			−0.1			−0.02		MIN, 25°C	
					−3.0			−6.0			−1.2		MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35	μA	MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$		172	344		65	130		46	92	ns	
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$		351	702		105	210		74	148	ns	
t_{PLH}	Propagation Delay,		245	490		54	108		38	76	ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}	$\overline{CPSO}$ to Q_S		239	478		63	126		45	90		
t_{PLH}	Propagation Delay,		260	520		102	204		72	144	ns	
t_{PHL}	TOP to Q_n		234	468		91	182		64	128		
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$		127	254		59	118		42	84	ns	
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$		256	512		91	182		64	128	ns	
t_{PLH}	Propagation Delay,		321	642		107	214		75	150	ns	
t_{PHL}	TOP to $\overline{ORE}$		205	410		87	174		61	122		
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$		95	190		35	70		25	50	ns	
t_{FT}	Fall Through Time		2000	4000		800	1600		560	1120	ns	
t_{PZH}	Output Enable Time		41	82		19	38		14	28	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			68	136		26	52		19	38		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		51	102		27	54		19	38	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			64	128		31	62		22	44		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		37	74		20	40		14	28	ns	
t_{THL}			27	54		14	28		10	20		
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$		215	430		81	162		57	114	ns	
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$		439	878		131	262		92	184	ns	
t_{PLH}	Propagation Delay,		306	612		68	136		48	96	ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}	$\overline{CPSO}$ to Q_S		299	598		79	158		56	112		
t_{PLH}	Propagation Delay,		325	650		128	256		90	180	ns	
t_{PHL}	TOP to Q_n		293	586		114	228		80	160		

Notes on following page.

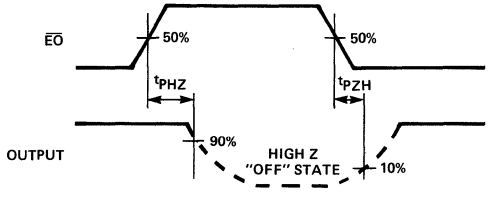
AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$		159	318		74	148		52	104	ns	C_L = 50 pF Input Transition Times ⩽20 ns
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$		320	640		114	228		80	160	ns	
t_{PLH} t_{PHL}	Propagation Delay, TOP to $\overline{ORE}$		401 256	802 512		134 109	268 218		94 77	188 154	ns	
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$		119	238		44	88		31	62	ns	
t_{FT}	Fall Through Time		2020	4040		820	1640		574	1148	ns	
t_{PZH} t_{PZL}	Output Enable Time		51 85	102 170		24 33	48 66		17 24	34 48	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		64 80	128 160		34 39	68 78		24 28	48 56	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		46 34	92 68		25 18	50 36		18 13	36 26	ns	
$t_w\overline{CP}(H)$	Min $\overline{CPSI}$ Pulse Width (HIGH)	118	59		44	22		31	16		ns	C_L = 15 pF Input Transition Times ⩽20 ns
$t_w\overline{CP}(L)$	Min $\overline{CPSI}$ Pulse Width (LOW)	220	110		108	54		76	38		ns	
$t_w\overline{CP}(L)$	Min $\overline{CPSO}$ Pulse Width (LOW)	120	60		60	30		42	21		ns	
$t_w\overline{CP}(H)$	Min $\overline{CPSO}$ Pulse Width (HIGH)	110	55		72	36		51	26		ns	
$t_wPL(H)$	Min PL Pulse Width (HIGH)	122	61		44	22		31	16		ns	
$t_w\overline{TTS}(L)$	Min $\overline{TTS}$ Pulse Width (LOW)	160	80		124	62		87	44		ns	
$t_w\overline{TOS}(L)$	Min $\overline{TOS}$ Pulse Width (LOW)	182	91		60	30		42	21		ns	
$t_wTOP(L)$	Min TOP Pulse Width (LOW)	142	71		52	26		37	19		ns	
$t_w\overline{MR}(L)$	Min $\overline{MR}$ Pulse Width (LOW)	192	96		108	54		76	38		ns	
t_{rec}	$\overline{MR}$ Recovery Time	44	22		36	18		26	13		ns	
t_s t_h	Set-Up and Hold Times, D_s to $\overline{CPSI}$	104 −8	52 −15		40 24	20 12		28 18	14 9		ns	
t_s t_h	Set-Up and Hold Times, $\overline{TTS}$ to $\overline{IRF}$, Serial or Parallel Mode	186 76	93 38		98 52	49 26		70 38	35 19		ns	
t_s	Set-Up Time, $\overline{ORE}$ to $\overline{TOS}$	−151	−302		−21	−42		−15	−30		ns	
f_{MAX}	Input CLOCK Frequency (Note 4)	1.1	2.3		2.6	5.3		3.4	6.9		ns	

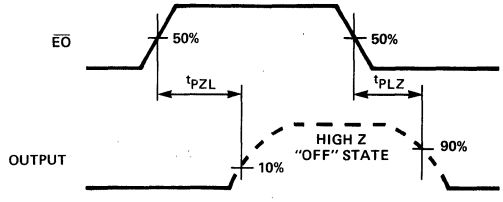
NOTES:
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4700 Series CMOS Fmily Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L).
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

4

SWITCHING WAVEFORMS



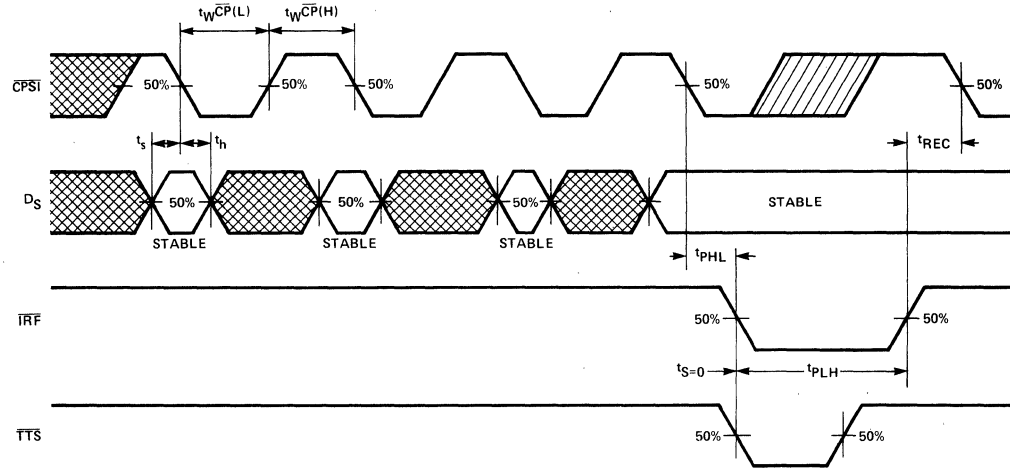
OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

SWITCHING WAVEFORMS (Cont'd)

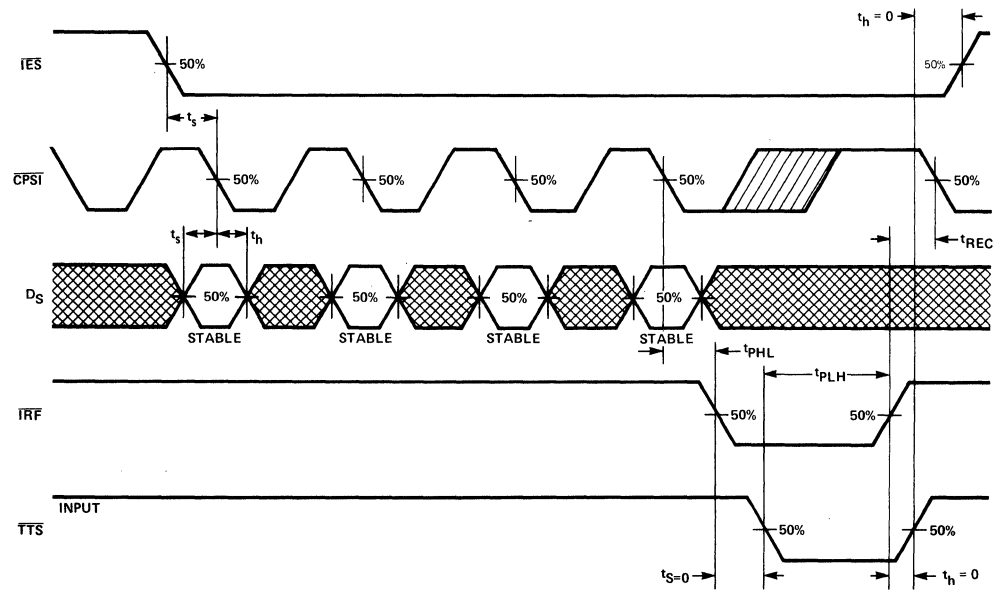
SERIAL INPUT UNEXPANDED OR MASTER OPERATION



MINIMUM $\overline{CPSI}$ PULSE WIDTH, PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$, AND SET-UP AND HOLD TIMES, D_S TO $\overline{CPSI}$, AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$, = PL = LOW

SERIAL INPUT EXPANDED SLAVE OPERATION



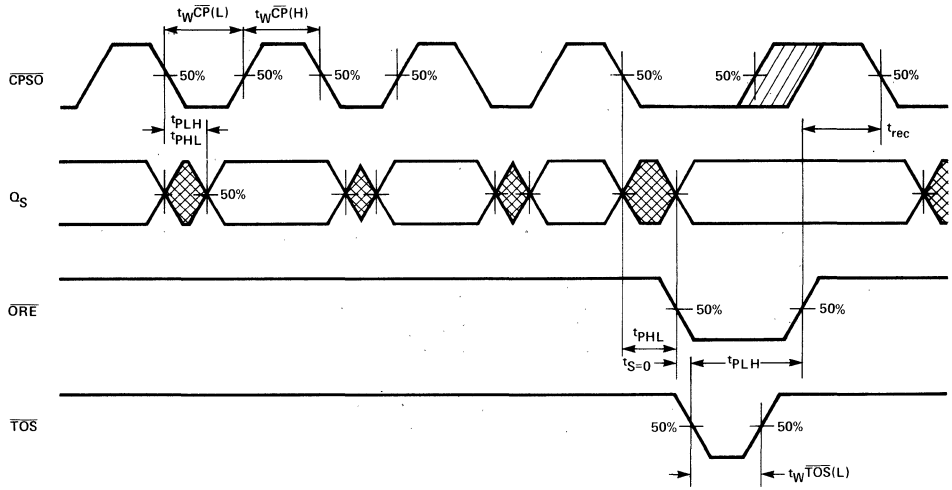
PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$ AND SET-UP AND HOLD TIMES, $\overline{IES}$ TO $\overline{CPSI}$, D_S TO $\overline{CPSI}$ AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL $\overline{IES}$ = HIGH
WHEN INITIALIZED, PL = LOW

NOTE:
Set-up and hold times are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (Cont'd)

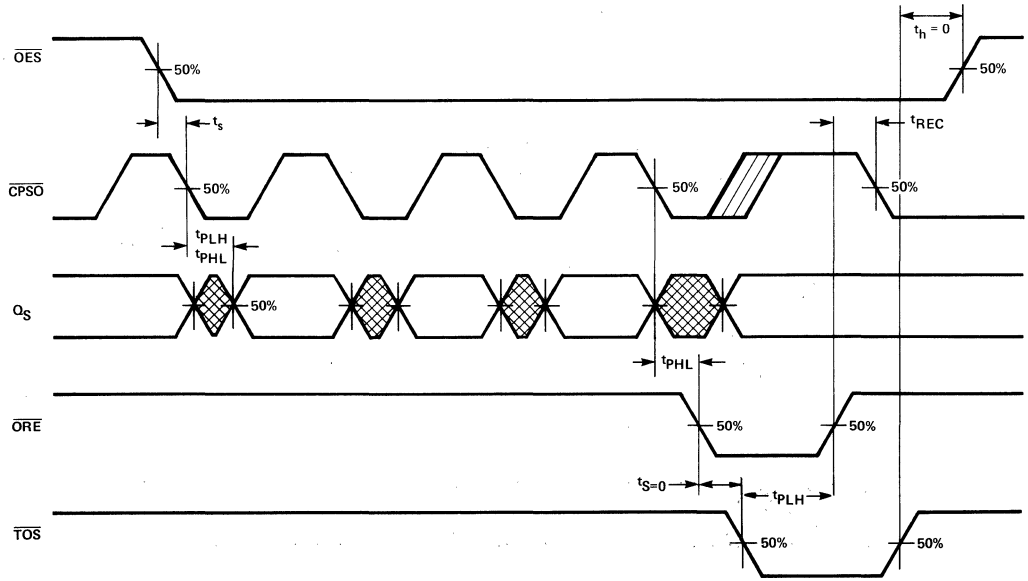
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION



$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO Q_S, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, MINIMUM $\overline{CPSO}$ PULSE WIDTH, MINIMUM $\overline{TOS}$ PULSE WIDTH AND SET-UP TIME $\overline{ORE}$ TO $\overline{TOS}$.

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{IES}$ = LOW
WHEN INITIALIZED, $\overline{OES}$ = LOW

SERIAL OUTPUT, SLAVE OPERATION



$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO Q_S, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, AND SET-UP AND HOLD TIMES, $\overline{OES}$ TO $\overline{CPSO}$, $\overline{ORE}$ TO $\overline{TOS}$, $\overline{TOS}$ TO $\overline{OES}$

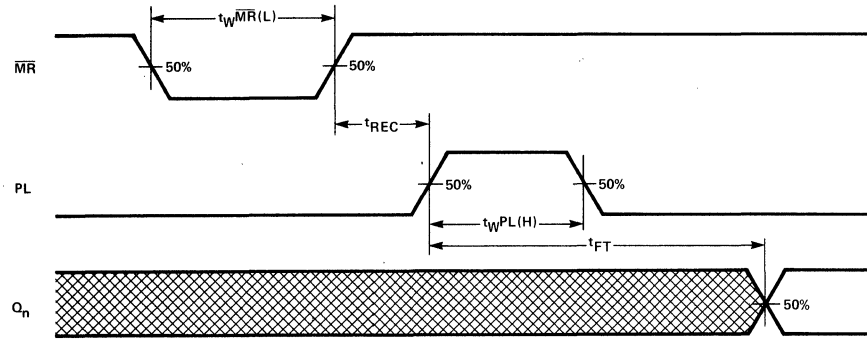
CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{IES}$ = HIGH
WHEN INITIALIZED

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

4

SWITCHING WAVEFORMS (Cont'd)

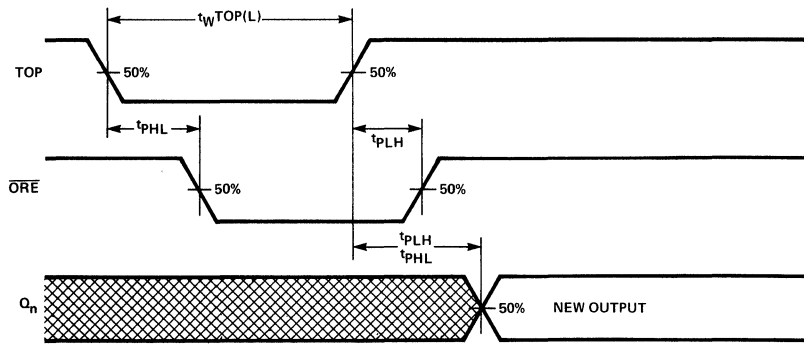
FALL THROUGH TIME



MINIMUM $\overline{MR}$ AND PL PULSE WIDTHS, RECOVERY TIME FOR $\overline{MR}$ AND FALL THROUGH TIME

CONDITIONS: $\overline{TTS}$ CONNECTED TO $\overline{IRF}$, $\overline{TOS}$ CONNECTED TO $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ = LOW. TOP = HIGH

PARALLEL OUTPUT, FOUR BIT WORD OR MASTER IN PARALLEL EXPANSION

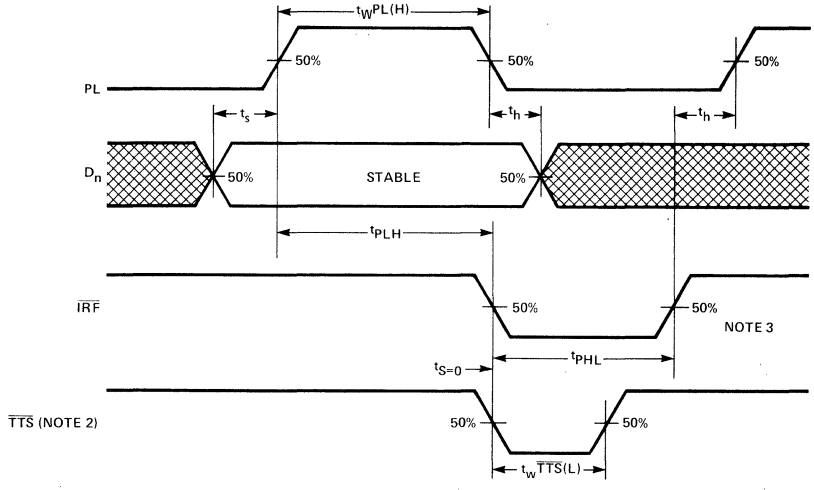


PROPAGATION DELAY, TOP TO $\overline{ORE}$, TOP TO Q_n, AND MINIMUM TOP PULSE WIDTH

CONDITIONS: $\overline{IES}$ = LOW WHEN INITIALIZED, $\overline{EO}$ = $\overline{CPSO}$ = LOW. DATA AVAILABLE IN STACK

SWITCHING WAVEFORMS (Cont'd)

PARALLEL LOAD MODE, FOUR BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

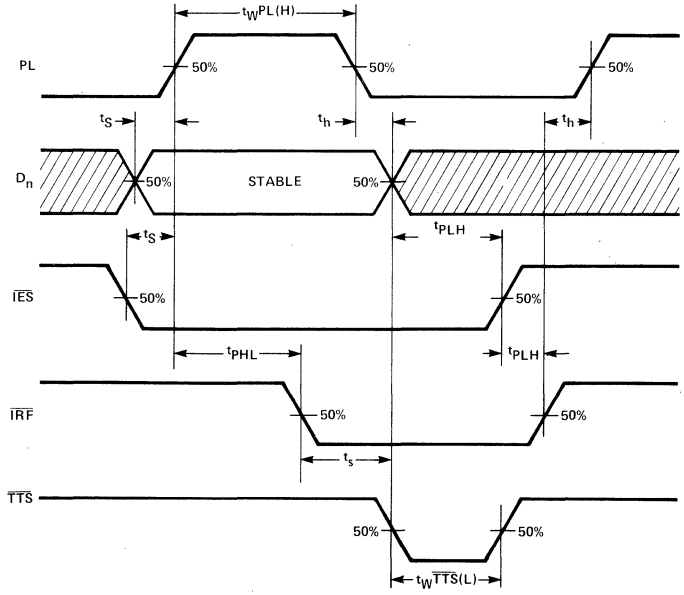


PROPAGATION DELAY PL TO $\overline{IRF}$, $\overline{TTS}$ TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES D_n TO PL, $\overline{IRF}$ TO PL, $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$ = LOW WHEN INITIALIZED

NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, $\overline{IRF}$ will stay LOW.

PARALLEL LOAD, SLAVE MODE



PROPAGATION DELAY, $\overline{TTS}$ TO $\overline{IES}$, $\overline{IES}$ TO $\overline{IRF}$, PL TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES, D_n TO PL, $\overline{IRF}$ TO $\overline{TTS}$, $\overline{IRF}$ TO PL

CONDITIONS: STACK NOT FULL, DEVICE INITIALIZED WITH $\overline{IES}$ HIGH

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

4

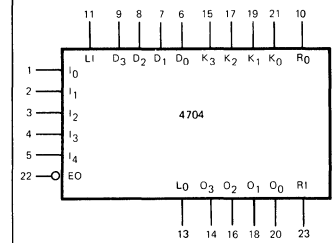
4704/4704B
DATA PATH SWITCH
FAIRCHILD CMOS MACROLOGIC

DESCRIPTION — The 4704 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the 4705 (Arithmetic Logic Register Stack). A total of 30 instructions (see *Table 1*) facilitate logic shifting, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction (I_0-I_4) selects one of the 32 instructions operating on two sets of 4-bit data inputs (D_0-D_3, K_0-K_3). Left Input (LI) and Left Output (LO) and Right Input (RI) and Right Output (RO) are available for expansion in 4-bit increments. An active LOW Output Enable input ($\overline{EO}$) provides 3-state control of the data outputs (O_0-O_3) for bus oriented applications.

The 4704 is fully compatible with all CMOS families.

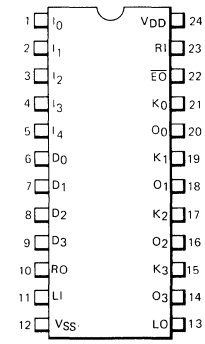
LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **TWO 4-BIT DATA INPUT BUSSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **SLIM 24-PIN PACKAGE**

CONNECTION DIAGRAM
DIP (TOP VIEW)

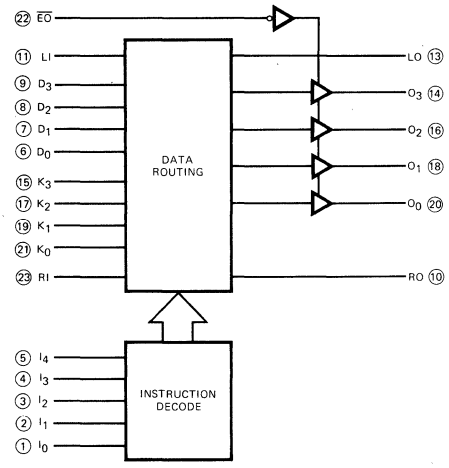


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

D_0 - D_3	D-Bus Inputs
K_0 - K_3	K-Bus Inputs
I_0 - I_4	Instruction Input
LI	Shift Left Input
LO	Shift Left Output
RI	Shift Right Input
RO	Shift Right Output
$\overline{EO}$	Output Enable Input (Active LOW)
O_0 - O_3	Data Outputs

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
O = Pin Number

TABLE 1
INSTRUCTION SET FOR THE 4704

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS						FUNCTION
I_4	I_3	I_2	I_1	I_0	O_3	O_2	O_1	O_0		I_4	I_3	I_2	I_1	I_0	LO	O_3	O_2	O_1	O_0	RO	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	RI	RI	RI	RI	RI		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	K_3	K_3	K_2	K_1	K_0		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp(1)	H	L	L	H	L	RI	RI	RI	RI	RI		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp(1)	H	L	L	H	H	D_3	D_3	D_2	D_1	D_0		D-Bus Sign Extend
L	L	H	L	L	D_3	D_2	D_1	D_0	Byte Mask, D-Bus	H	L	H	L	L	D_3	D_2	D_1	D_0	RI		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask, D-Bus	H	L	H	L	H	K_3	K_2	K_1	K_0	RI		K-Bus Shift Left
L	L	H	H	L	D_3	D_2	D_1	D_0	Byte Mask, D-Bus	H	L	H	H	L		LI	D_3	D_2	D_1	D_0	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask, D-Bus	H	L	H	H	H		D_3	D_3	D_2	D_1	D_0	D-Bus Shift Right Arith(2)
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		LI	K_3	K_2	K_1	K_0	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		K_3	K_3	K_2	K_1	K_0	K-Bus Shift Right Arith(2)
L	H	L	H	L	K_3	K_2	K_1	K_0	Byte Mask, K-Bus	H	H	L	H	L		K_3	K_2	K_1	K_0		Byte Mask, K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask, K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask, K-Bus
L	H	H	L	L	D_3	D_2	D_1	D_0	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	K_3	K_2	K_1	K_0	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined (Reserved)
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined (Reserved)

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

FUNCTIONAL DESCRIPTION - The 4704 combines the functions of a dual 4-input multiplexer, a true/complement one/zero generator, and a shift left/shift right array.

As shown in *Table 1*, there are two shift right modes. The arithmetic right shift preserves the sign bit in the most significant position while the logic shift moves all positions. Right shift is defined as a 1-bit shift toward the least significant position.

For half-word arithmetic the 4704 provides instructions which extend the sign bit left through the more significant slices. Shift linkages are available as individual inputs and outputs for complete flexibility.

The 4704 may be used to generate constants +1, 0, −1 and −2 in 2's complement notation.

EXPANSION – Arrays of larger than 4-bit word lengths are easily obtained. *Figure 1* illustrates a 16-bit array constructed using four devices; device 1 is the least significant and device 4 is the most significant slice. Within each slice, inputs and outputs with '0' subscript are the least significant bits.

The I_1 through I_4 inputs of all devices are bussed. These four bus lines together with the I_0 inputs of the devices form an 8-bit instruction bus to control the array. In some applications, it may be possible to connect the I_0 inputs of devices 1 and 2 together and the I_0 inputs of devices 3 and 4 together, so that only six bits are needed to control the arrays. Connecting the LO of device 1 to RI of device 2, LO of device 2 to RI of device 3, etc., provides left shift (*i.e.*, shift towards most significant bit) and sign extension. In a similar fashion right shift operation is accomplished by connecting the LI input of a device to the RO of the next more significant device.

The sign-extend group consists of two adjacent instructions differing only in I_0 (refer to *Table 1*). When the code HLLHH is placed on the instruction inputs (D-Bus Sign Extend), the most significant bit of the D bus (D_3) is available on the LO output. The companion code HLLHL will copy the RI input (connected to LO of the previous stage) onto the output bus (D_0 – D_3) and to its own LO output. Thus when a sign extend function is desired (e.g., arithmetic operations on the eight least significant bits in a 16-bit machine) the code HLLH will be applied to instruction inputs (I_4,I_3,I_2,I_1) of all the 4704s. I_0 of the most significant byte will be LOW and I_0 of the least significant byte will be HIGH. In a similar fashion sign-extend function on a number present on the K-Bus is executed by the code HLLL on I_4,I_3,I_2, and I_1.

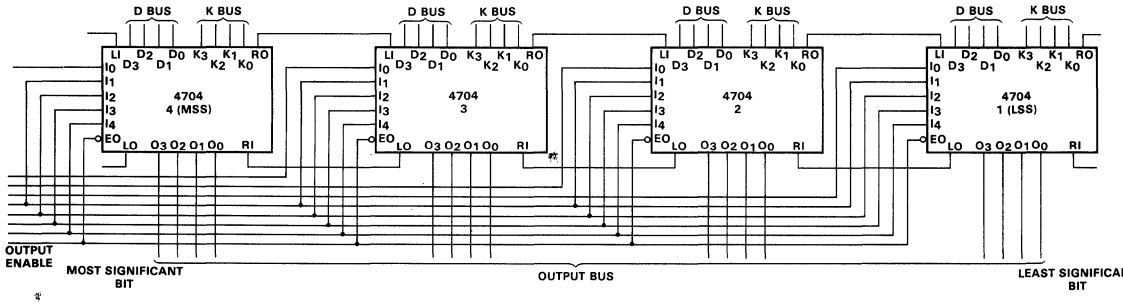


Fig. 1
16-BIT 4704 ARRAY

The 4704 provides several options for masking operations. For example, Byte Mask operation (LLLL on I_4,I_3,I_2,I_1) will force the output bus either HIGH or LOW depending on I_0. Connecting I_0 of the most significant byte HIGH and I_0 of the least significant byte LOW will force the outputs of the DPS array to a state of 00FF (in hexadecimal notation) 16. A LOW on any output is assumed as logic 1. When the output bus of the 4704 is used as an input to a 16-bit Arithmetic Logic Register Stack (ALRS) network (see *Figure 2*), the ALRS can execute a logic AND function between its input bus and one of its registers, thus masking the least significant byte of that register. More complex masking operation can be executed using the Byte AND Mask and Byte OR Mask operations (see *Table 1*):

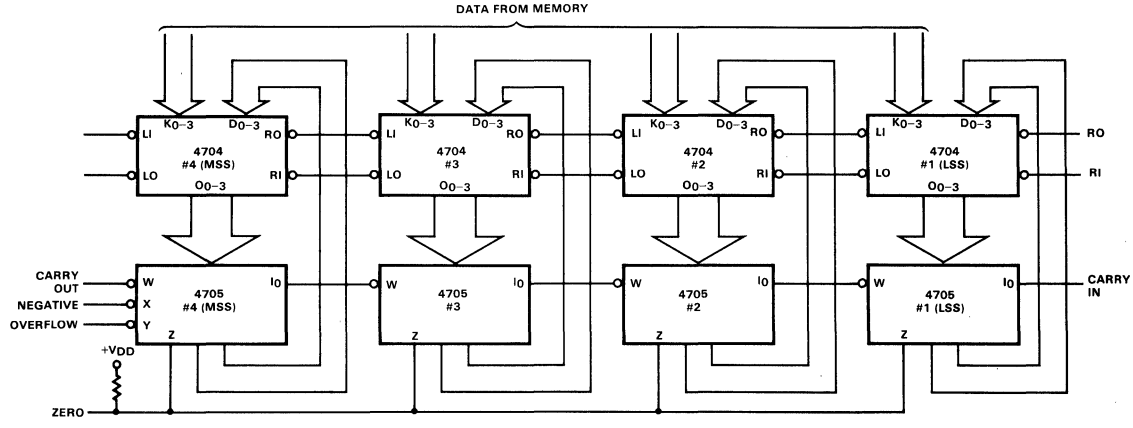


Fig. 2
16-BIT DATA PATH

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF HIGH Current	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF LOW Current	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35	μA	MIN, 25°C	
					250			500			1000		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		166	332		65	130		45	90	ns	
t_{PHL}	D_n, K_n to O_n		197	384		73	146		48	96		
t_{PLH}	Propagation Delay,		91	182		44	88		32	64	ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}	D_n, K_n to L_O, R_O		100	200		46	92		33	66		
t_{PLH}	Propagation Delay,		101	202		57	114		42	84	ns	
t_{PHL}	R_I to L_O		114	228		49	98		41	82		
t_{PLH}	Propagation Delay,		114	228		46	92		31	62	ns	
t_{PHL}	L_I to R_O		122	244		51	102		33	66		
t_{PLH}	Propagation Delay,		188	376		75	150		49	98	ns	
t_{PHL}	I_n to O_n		201	402		74	148		50	100		
t_{PLH}	Propagation Delay,		106	212		57	114		41	82	ns	
t_{PHL}	I_n to R_O, L_O		152	304		57	114		41	82		
t_{PZH}	Output Enable		44	88		15	30		11	22	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	Time		56	112		24	48		17	34		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable		38	76		35	70		26	52	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	Time		39	78		27	54		19	38		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition		43	86		22	44		17	34	ns	
t_{THL}	Time, O_n		53	106		20	40		15	30		
t_{TLH}	Output Transition		41	82		19	38		16	32	ns	
t_{THL}	Time, R_O and L_O		55	110		22	44		15	30		

Notes on following page.

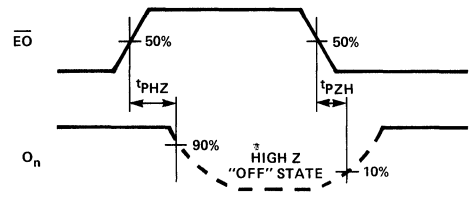
4

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

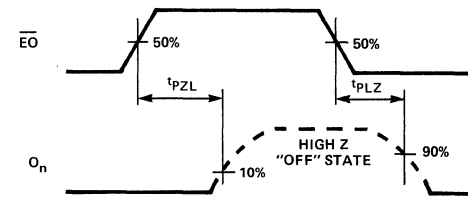
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		192	384		76	152		53	106	ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}	D_n, K_n to O_n		232	464		85	170		56	112		
t_{PLH}	Propagation Delay,		100	200		56	112		41	82	ns	
t_{PHL}	D_n, K_n to L_O, R_O		162	324		55	110		42	84		
t_{PLH}	Propagation Delay,		106	212		63	126		49	98	ns	
t_{PHL}	R_I to L_O		178	356		61	122		49	98		
t_{PLH}	Propagation Delay,		133	266		56	112		37	74	ns	
t_{PHL}	L_I to R_O		166	332		61	122		41	82		
t_{PLH}	Propagation Delay,		204	408		83	166		57	114	ns	
t_{PHL}	I_n to O_n		245	490		87	174		59	118		
t_{PLH}	Propagation Delay,		122	244		66	132		48	96	ns	
t_{PHL}	I_n to R_O, L_O		199	398		69	138		50	100		
t_{PZH}	Output Enable		47	94		19	38		15	30	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PZL}	Time		68	136		29	58		21	42		
t_{PHZ}	Output Disable		46	92		41	82		34	68	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}	Time		47	94		31	62		20	40		
t_{TLH}	Output Transition		80	160		43	86		32	64	ns	
t_{THL}	Time, O_n		129	258		38	76		26	52		
t_{TLH}	Output Transition		74	148		42	84		32	64	ns	
t_{THL}	Time, R_O and L_O		76	152		40	80		27	54		

NOTES:
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000 Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

4705/4705B
ARITHMETIC LOGIC REGISTER STACK
FAIRCHILD CMOS MACROLOGIC

DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement accumulators in high performance microprogrammed digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM, and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0-A_2). The result of the operation is loaded into the same RAM location and simultaneously, is loaded into the Output Register making it available at the 3-state output data bus.

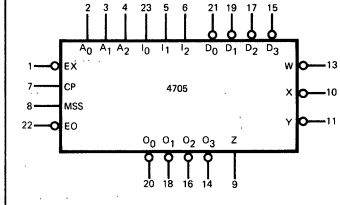
The 4705 operates on four bits of data but features are provided for expansion to longer word lengths. Carry propagate and carry generate facilities are provided for an external carry lookahead where maximum operating speed is required. In applications where high-speed arithmetic is not needed, ripple expansion may also be implemented. The 4705 provides three status signals: Zero, Negative and Overflow. These qualify the result of an operation. The 4705 is fully compatible with all CMOS families.

- **VERY LOW POWER DISSIPATION**
- **EIGHT ACCUMULATORS IN A SINGLE PACKAGE**
- **HIGH SPEED – 2 MHz MICROINSTRUCTION RATE**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES STATUS – ZERO, NEGATIVE, AND OVERFLOW**
- **3-STATE OUTPUTS**
- **SLIM 24-PIN PACKAGE**

PIN NAMES

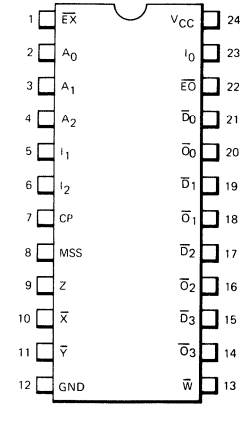
$\overline{D}_0$ - $\overline{D}_3$	Data Inputs (Active LOW)
A_0 - A_2	Address Instruction Inputs
I_0 - I_2	ALU Instruction Inputs
MSS	Most Significant Slice Input (Active HIGH)
CP	Clock Input
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Data Outputs (Active LOW)
$\overline{W}$	Ripple Carry Outputs (Active LOW)
$\overline{X}$	Carry Propagate Output
$\overline{Y}$	Carry Generate Output
Z	Zero Status Output (Active HIGH, Open Collector)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



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BLOCK DIAGRAM

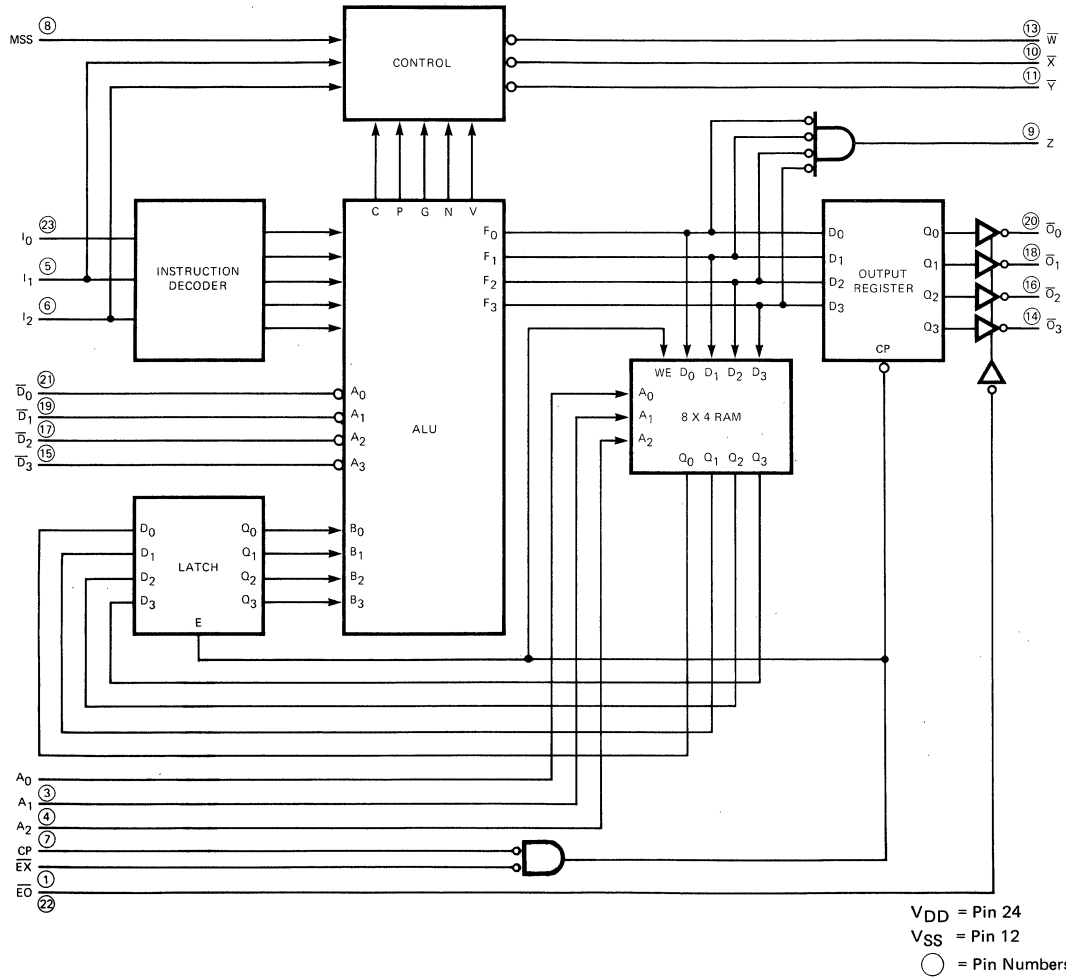


TABLE 1
INSTRUCTION FIELD ASSIGNMENT

I_2 I_1 I_0	INTERNAL OPERATION	
L L L	R_X plus D-Bus plus 1 → R_X	Accumulate
L L H	R_X plus D-Bus → R_X	Accumulate
L H L	R_X • D-Bus → R_X	Logical AND
L H H	D-Bus → R_X	Load
H L L	R_X → Output Register	Output
H L H	R_X + D-Bus →	Logical OR
H H L	R_X ⊕ D-Bus → R_X	Exclusive OR
H H H	D-Bus → R_X	Load Complement

H = HIGH Level L = LOW Level

NOTES:

1. R_X is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 4705 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an Instruction Decoder, Control Logic and a 4-bit Output Register.

The ALU receives the active LOW input data ($\overline{D}_0$–$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and Output Register. The active LOW output data ($\overline{O}_0$–$\overline{O}_3$) is obtained from the Output Register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level $\overline{EO}$ disables the buffers (high impedance state).

The instruction bus for the 4705 consists of two fields, A and I; A_0–A_2 specify the desired location of the RAM and I_0–I_2 specify the desired function to be performed. *Table 1* lists instruction code assignments. Thus, the 4705 provides eight accumulators (R_0–R_7) and eight different operations may be performed on any of these accumulators. The I_0–I_2 inputs are decoded by the Instruction Decoder to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: Carry Out (C), Carry Propagate (P), Carry Generate (G), Negative (N) and Overflow (V) status. The control logic manipulates the status signals as a function of I_0–I_2 and a control input MSS. A HIGH on the MSS input declares the most significant slice in a 4705 array (the MSS can be tied directly to V_{DD}). All devices, except the most significant 4705 should have a LOW level (ground) on the MSS input. The control logic generates three device outputs ($\overline{W}$, $\overline{X}$ and $\overline{Y}$) for arrayed operation. An all zero result from the ALU is decoded and presented at the open collector Zero (Z) output.

The I_0 input serves a dual purpose. For arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in 4705 expansion schemes.

Operation – The 4705 operates on a single clock. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$–$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0–I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. The A lines must obviously be held stable during this time. On the LOW-to-HIGH transition of the CP, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

EXPANSION – The 4705 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The 4705 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Progagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four 4705s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus the $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices. The Z output is open collector and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four 4705s. The MSS input is tied to V_{DD} on the most significant slice (ALRS 4); the MSS inputs of the other devices are tied to ground. The instruction bus of this array consists of A-field and I-field. A-field is obtained by connecting corresponding A inputs of all four devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, it assumes the state of the I_0 input. Thus, in *Figure 1*, if an arithmetic instruction is specified, carry propagates through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions effectively connect all I_0 inputs together to form the I-field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. In the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to Negative and Overflow status signals.

The $\overline{X}$ output of device 4 is LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has opposite sign, then it is assumed that an overflow has occurred. It should be noted that $\overline{W}$, $\overline{X}$ and $\overline{Y}$ are not controlled by $\overline{EX}$ or CP. *Figure 2* shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external 4582 in addition to the four 4705s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH at this input. The A-field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs together with the I_0 input of device 1 form the I-field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the 4582 Carry Outputs (C_{n+x}, C_{n+y} and C_{n+z} respectively). Also the P and G in-

4

puts of 4582 are connected to $\overline{X}$ and $\overline{Y}$ outputs of the 4705 as shown. The control logic in the 4705 (see block diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs as well as the Carry Generate and Carry Propagate outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output is treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ output of device 4 is the carry output from the array. Also note that the I_0 input of device 1 is not only an instruction input but also provides the carry input to the array so the I_0 input of device 1 must be connected to the appropriate 4582 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the 4705 forces a LOW on $\overline{X}$ and a HIGH on $\overline{Y}$ outputs on all except the most significant slice. An examination of the 4582 logic reveals that whenever P is LOW and G is HIGH the associated carry output is the same as the carry input. Thus, in *Figure 2* devices 2, 3, and 4 will assume the logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent Negative and Overflow from the array.

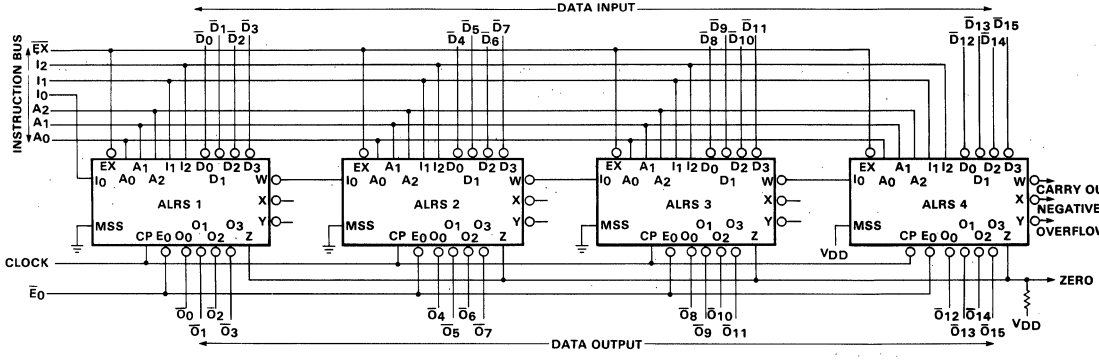


Fig. 1
RIPPLE CARRY EXPANSION

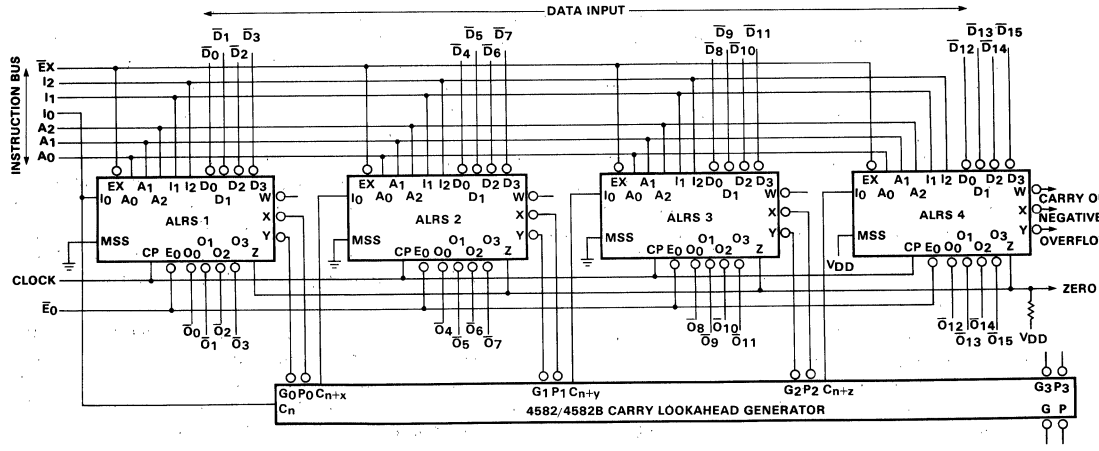


Fig. 2
CARRY LOOKAHEAD EXPANSION

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 3)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35		MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 15 pF (See Note 4)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS (Note 6)
t_{PLH}	Propagation Delay,		140	280		61	122		43	86	ns	$\overline{EO}$ = $\overline{EX}$ = V_{SS}
t_{PHL}	CP to $\overline{O}_n$		145	290		61	122		43	86		
t_{PLH}	Propagation Delay,		99	198		45	90		32	64	ns	I_1 or I_2 = V_{DD}
t_{PHL}	I_0 to $\overline{W}$		115	230		48	96		34	68		
t_{PLH}	Propagation Delay,		241	482		92	184		65	130	ns	I_1 or I_2 = V_{SS}
t_{PHL}	$\overline{D}_n$ to $\overline{W}$		168	336		51	102		36	72		
t_{PLH}	Propagation Delay,		360	720		143	286		101	202	ns	MSS = V_{DD}
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		339	678		133	266		94	188		I_1 = I_2 = V_{SS}
t_{PLH}	Propagation Delay,		143	286		48	96		34	68	ns	MSS = I_1 = I_2 =
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		220	440		80	160		56	112		V_{SS}
t_{PLH}	Propagation Delay,		198	396		89	178		63	126	ns	MSS = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{X}$, $\overline{Y}$		236	472		99	198		70	140		
t_{PLH}	Propagation Delay,		322	644		140	280		98	196	ns	R_L = 1 kΩ to
t_{PHL}	$\overline{D}_n$ to Z		239	478		89	178		63	126		V_{DD}
t_{PLH}	Propagation Delay,		174	348		73	146		52	104	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to $\overline{W}$		201	402		77	154		54	108		
t_{PLH}	Propagation Delay,		130	260		64	128		45	90	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{W}$		227	454		93	186		66	132		
t_{PLH}	Propagation Delay,		295	590		114	228		80	160	ns	I_1 = I_2 = MSS =
t_{PHL}	$\overline{D}_3$ to $\overline{X}$		373	746		143	286		101	202		V_{DD}
t_{PLH}	Propagation Delay,		378	756		151	302		106	212	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		507	1014		205	410		144	288		V_{SS}
t_{PLH}	Propagation Delay,		509	1018		196	392		138	276	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		647	1294		258	516		181	362		MSS = V_{DD}
t_{PLH}	Propagation Delay,		500	1000		191	382		134	268	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$		670	1340		269	538		189	378		V_{DD}
t_{PLH}	Propagation Delay,		537	1074		219	438		154	308	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{W}$		394	788		151	302		106	212		
t_{PLH}	Propagation Delay,		490	980		209	418		147	294	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to Z		600	1200		238	476		167	334		

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd):

V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 15 pF (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (Note 6)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		123	246		61	122		43	86	ns	$I_1 = I_2 = V_{SS}$
t_{PHL}	I_1, I_2 to $\overline{X}, \overline{Y}$		316	632		126	252		89	178		MSS = V_{DD}
t_{PLH}	Propagation Delay,		151	302		74	148		52	104	ns	$I_1 = I_2 = V_{SS}$
t_{PHL}	I_0 to $\overline{X}, \overline{Y}$		277	554		108	216		76	152		MSS = V_{DD}
t_{PLH}	Propagation Delay,		335	670		148	296		104	208	ns	$I_1 = I_2 = V_{SS}$
t_{PHL}	I_1, I_2 to Z		261	522		104	208		73	146		
t_{PLH}	Propagation Delay,		258	516		117	234		82	164	ns	$I_1 = I_2 = V_{SS}$
t_{PHL}	I_0 to Z		162	324		64	128		45	90		
t_{PZH}	Output Enable		67	134		33	66		24	48	ns	(R_L = 1kΩ to V_{SS})
t_{PZL}	Time		51	102		25	50		18	36		(R_L = 1kΩ to V_{DD})
t_{PHZ}	Output Disable		64	128		33	66		24	48	ns	(R_L = 1kΩ to V_{SS})
t_{PLZ}	Time		74	148		37	74		26	52		(R_L = 1kΩ to V_{DD})
t_{TLH}	Output Transition		46	92		26	52		19	38	ns	C_L = 15 pF
t_{THL}	Time		32	64		14	28		10	20		
t_{CW}	Minimum Clock Period	1018	509		526	263		370	185		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns $\overline{EX}$ = V_{SS}
$t_wCP(L)$	CP Minimum Pulse Width,LOW	214	107		102	51		72	36		ns	
$t_wCP(H)$	CP Minimum Pulse Width,HIGH	484	242		222	111		156	78		ns	
t_s	Set-Up Time, $\overline{EX}$ to CP	326	163		198	99		134	67		ns	
t_h	Hold Time, $\overline{EX}$ to CP	20	0		15	0		10	0			
t_s	Set-Up Time, A_n to CP	452	226		168	84		118	59		ns	
t_h	Hold Time, A_n to CP	20	0		15	−1		10	0			
t_s	Set-Up Time, $\overline{D}_n$ to CP	500	250		198	99		140	70		ns	
t_h	Hold Time, $\overline{D}_n$ to CP	−35	−69		−11	−21		−8	−15			
t_s	Set-Up Time, I_n to CP	502	251		224	112		158	79		ns	
t_h	Hold Time, I_n to CP	−29	−57		−12	−23		−9	−17			
f_{MAX}	Input Count Frequency (Note 1)	0.98	1.97		1.9	3.8		2.47	4.94		MHz	

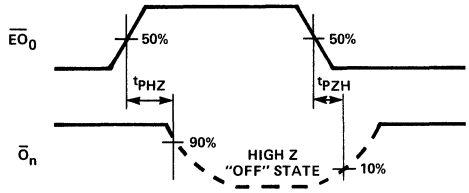
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 50 pF

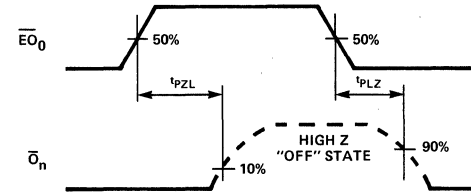
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (Note 6)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		163	326		71	142		50	100	ns	$\overline{EO}$ = $\overline{EX}$ = V_{SS}
t_{PHL}	CP to $\overline{O}_n$		174	348		70	140		49	98		
t_{PLH}	Propagation Delay,		120	240		55	110		39	78	ns	I_1 or I_2 = V_{DD}
t_{PHL}	I_0 to $\overline{W}$		139	278		56	112		40	80		
t_{PLH}	Propagation Delay,		251	502		101	202		71	142	ns	I_1 or I_2 = V_{SS}
t_{PHL}	$\overline{D}_n$ to $\overline{W}$		186	372		61	122		43	86		
t_{PLH}	Propagation Delay,		382	764		150	300		105	210	ns	MSS = V_{DD}
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		363	726		140	280		98	196		I_1 = I_2 = V_{SS}
t_{PLH}	Propagation Delay,		161	322		58	116		41	82	ns	MSS = I_1 = I_2 =
t_{PHL}	$\overline{D}_n$ to $\overline{X}$, $\overline{Y}$		239	478		90	180		63	126		V_{SS}
t_{PLH}	Propagation Delay,		211	422		96	192		68	136	ns	MSS = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{X}$, $\overline{Y}$		266	532		109	218		77	154		
t_{PLH}	Propagation Delay,		360	720		179	358		126	262	ns	R_L = 1kΩ to
t_{PHL}	$\overline{D}_n$ to Z		251	502		95	190		67	134		V_{DD}
t_{PLH}	Propagation Delay,		198	396		83	166		59	118	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to $\overline{W}$		226	452		87	174		61	122		
t_{PLH}	Propagation Delay,		152	304		73	146		52	104	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{W}$		252	504		104	208		73	146		
t_{PLH}	Propagation Delay,		317	634		123	246		87	174	ns	I_1 = I_2 = MSS =
t_{PHL}	$\overline{D}_3$ to $\overline{X}$		401	802		152	304		107	214		V_{DD}
t_{PLH}	Propagation Delay,		397	794		161	322		113	226	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		538	1076		213	426		150	300		V_{SS}
t_{PLH}	Propagation Delay,		527	1054		205	410		144	288	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{X}$, $\overline{Y}$		668	1336		269	538		189	378		MSS = V_{DD}
t_{PLH}	Propagation Delay,		519	1038		202	404		142	284	ns	I_1 = I_2 = MSS =
t_{PHL}	A_n to $\overline{X}$		695	1380		279	558		196	392		V_{DD}
t_{PLH}	Propagation Delay,		556	1112		229	458		161	322	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to $\overline{W}$		415	830		161	322		113	226		
t_{PLH}	Propagation Delay,		512	1024		236	472		166	332	ns	I_1 = I_2 = V_{SS}
t_{PHL}	A_n to Z		618	1236		245	490		172	344		
t_{PLH}	Propagation Delay,		143	286		71	142		50	100	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to $\overline{X}$, $\overline{Y}$		338	676		134	268		94	188		MSS = V_{DD}
t_{PLH}	Propagation Delay,		171	342		85	170		60	120	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to $\overline{X}$, $\overline{Y}$		304	608		118	236		83	166		MSS = V_{DD}
t_{PLH}	Propagation Delay,		370	740		186	392		131	262	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_1, I_2 to Z		276	552		109	218		77	154		
t_{PLH}	Propagation Delay,		298	596		155	310		109	218	ns	I_1 = I_2 = V_{SS}
t_{PHL}	I_0 to Z		177	354		70	140		49	98		
t_{PZH}	Output Enable		71	142		36	72		26	52	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}	Time		58	116		27	54		19	38		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable		71	142		40	80		28	56	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}	Time		79	158		42	84		30	60		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition		95	190		54	108		38	76	ns	C_L = 50 pF
t_{THL}	Time		67	134		27	54		19	38		

NOTES:
1. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
2. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.
3. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
4. Propagation Delays and Output transition times are graphically described in this section under 4700 Series CMOS Family Characteristics.
5. The Internal Clock is generated from CP and $\overline{EX}$. The Internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW. For timing considerations the $\overline{EX}$, CP two input active LOW AND gate is considered to exhibit no propagation delay. Actual timing requirements are referenced to the external CP and $\overline{EX}$ inputs.
6. Input Transition Times ≤ 20 ns.

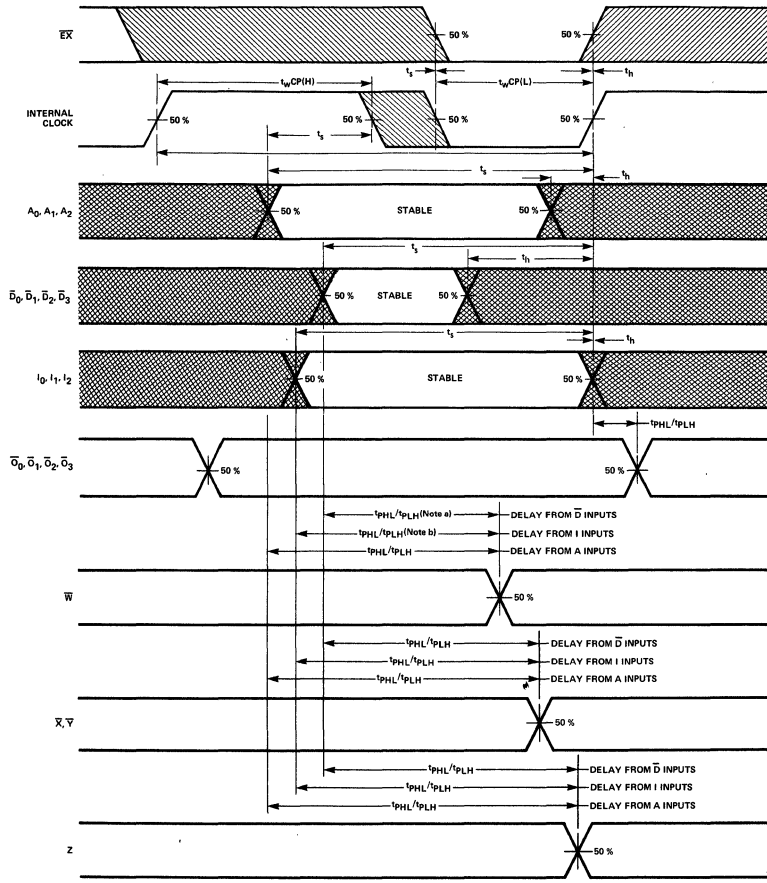
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



PROPAGATION DELAYS, A_n to Z, I_n to Z, $\overline{B}_n$ to Z, A_n to $\overline{X}$, $\overline{Y}$, I_n to $\overline{X}$, $\overline{Y}$, $\overline{B}_n$ to $\overline{X}$, $\overline{Y}$, A_n to $\overline{W}$, I_n to $\overline{W}$, $\overline{B}_n$ to $\overline{W}$, I_n to $\overline{O}_n$ SET-UP AND HOLD TIMES $\overline{EX}$ TO CP, A_n TO CP, $\overline{B}_n$ to CP, I_n to CP, MINIMUM INTERNAL CLOCK PULSE

NOTES:
a. Delay for logical operation (I_1 or I_2 = HIGH)
b. Delay for arithmetic operation (I_1 = I_2 = LOW)
c. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

4706/4706B

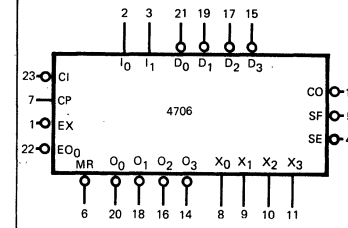
PROGRAM STACK

FAIRCHILD CMOS MACROLOGIC

DESCRIPTION – The 4706 is a 16-word by 4-bit "push-down pop-up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The 4706 executes 4 instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, PC is in the top location of the stack. As a new PC value is "pushed" into the stack (Call operation), all previous PC values effectively move down one level. The top location of the stack is the current PC. Up to 15 new program counter values can be stored, which gives the 4706 a 15 level nesting capability. "Popping" the stack (Return operation) brings the most recent PC to the top of the stack. The remaining two instructions affect only the top location of the stack. In the Branch operation a new PC value is loaded into the top location of the stack from the $\overline{D}_0 - \overline{D}_3$ inputs. In the Fetch operation, the contents of the top stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

The 4706 may be expanded to any word length without additional logic. 3-state output drivers are provided on the 4-bit address outputs ($X_0 - X_3$) and data outputs, ($\overline{O}_0 - \overline{O}_3$); the X-Bus outputs are enabled internally during the Fetch instruction while the O-bus outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The 4706 is fully compatible with all CMOS families.

LOGIC SYMBOL

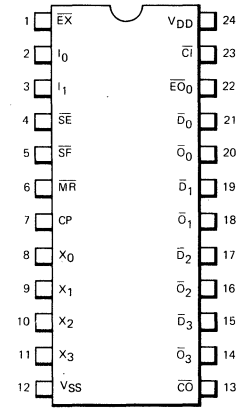


V_{DD} = Pin 24

V_{SS} = Pin 12

- **16-WORD BY 4-BIT LIFO**
- **15-LEVEL NESTING CAPABILITY**
- **2 MHz MICROINSTRUCTION RATE**
- **PROGRAM COUNTER LOADS FROM DATA BUS**
- **OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER**
- **STACK LIMIT STATUS INDICATORS**
- **SLIM 24-PIN PACKAGE**
- **3-STATE OUTPUTS**
- **VERY LOW POWER DISSIPATION**

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)
I_0, I_1	Instruction Inputs
$\overline{EX}$	Execute Input (Active LOW)
CP	Clock Input
$\overline{MR}$	Master Reset Input (Active LOW)
CI	Carry Input (Active LOW)
$\overline{EO}_0$	Output Enable Input (Active LOW)
$\overline{O}_0 - \overline{O}_3$	Output Data Outputs (Active LOW)
$X_0 - X_3$	Address Outputs
$\overline{CO}$	Carry Output (Active LOW)
$\overline{SF}$	Stack Full Output (Active LOW)
$\overline{SE}$	Stack Empty Output (Active LOW)

4

BLOCK DIAGRAM

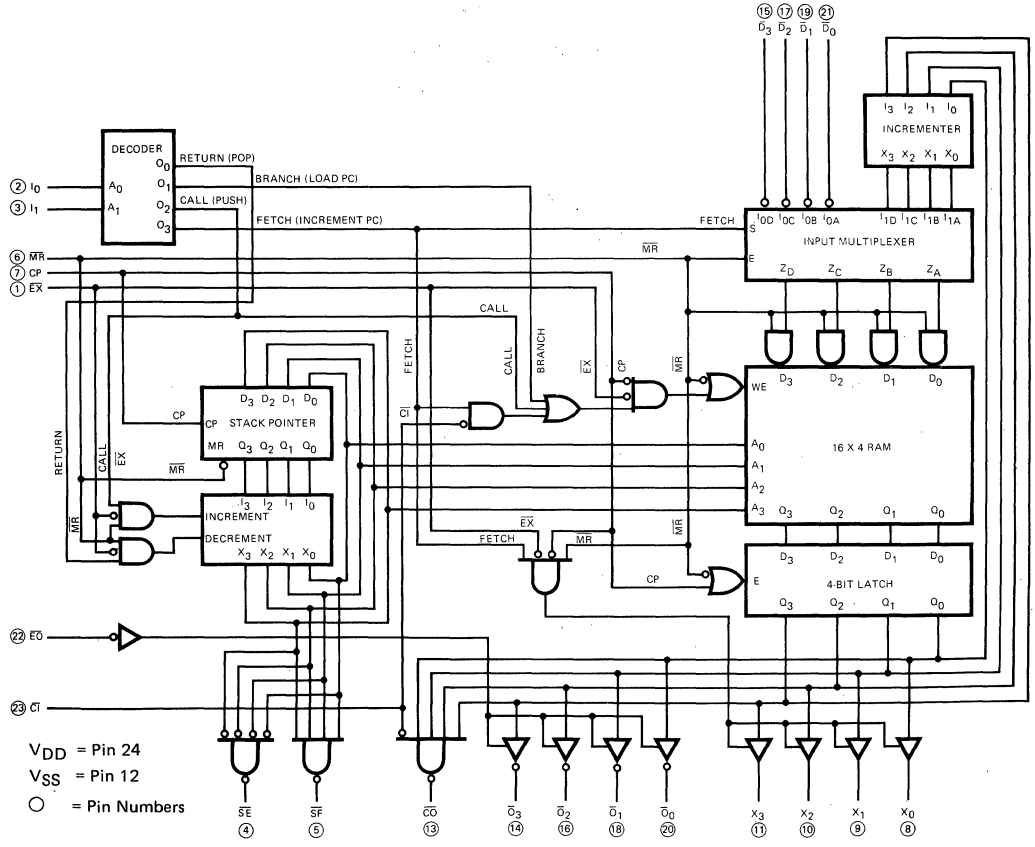


TABLE 1
INSTRUCTION SET FOR THE 4706

I_1 I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH $\overline{EO}_0$ LOW)
L L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L H	Branch (Load PC)	Load D-Bus into Current Program Counter Location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H L	Call (Push)	Increment Stack Pointer and Load D-Bus into New Program Counter Location	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Switching Waveforms for details.
H H	Fetch (Increment PC)	Increment Current Program Counter if $\overline{CI}$ is LOW	Current Program Counter while both CP and $\overline{EX}$ are LOW, disabled while CP or $\overline{EX}$ is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level L = LOW Level

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the 4706 consists of an Input Multiplexer, a 16 X 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The 4706 is organized around three 4-bit busses; the input data bus ($\overline{D}_0 - \overline{D}_3$), output data bus ($\overline{O}_0 - \overline{O}_3$) and the address bus ($X_0 - X_3$). The 4706 implements four instructions as determined by Inputs I_0 and I_1 (see Table 1). The O-Bus is derived from the RAM output latches and enabled by a LOW on the Output Enable ($\overline{EO}_0$) input. The X-Bus is also derived from the output latches; it is enabled internally during the Fetch instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) inputs.

Fetch Operation – The Fetch operation places the content of the current Program Counter (PC) on the X-Bus. If the Carry In ($\overline{CI}$) is LOW, the current PC is incremented in preparation for the next Fetch. If $\overline{CI}$ is HIGH, the value of the current PC is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The Execute ($\overline{EX}$) is normally LOW at this time. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the Input Multiplexer. The current PC value is loaded into the latches and is available on the O-Bus if $\overline{EO}_0$ is LOW. When CP is LOW the latches are disabled from following the RAM output, when both CP and $\overline{EX}$ are LOW, buffers are enabled, applying the current PC to the X-Bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out ($\overline{CO}$) is LOW when the content of the current PC is at its maximum, i.e., all ones and the Carry In ($\overline{CI}$) is LOW. When CP or $\overline{EX}$ goes HIGH, writing into the RAM is inhibited and the address buffers ($X_0 - X_3$) are disabled.

Branch Operation – During a Branch operation, the data inputs ($\overline{D}_0 - \overline{D}_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ Input are set up when CP is HIGH. The Stack Pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW) the D-Bus Inputs are written into the current PC. The X-Bus drivers are not enabled during a Branch operation.

Call Operation – During a Call operation the content of the data bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the Stack Pointer value thus incrementing the RAM address. Since the output latches go to the nontransparent or store mode when CP is LOW, the O-Bus outputs will reflect the RAM output at the CP negative-going transition. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the previous contents of the incremented RAM address after CP goes LOW. If CP goes LOW a very short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW to HIGH transition of CP.

When CP is LOW (assuming $\overline{EX}$ is LOW) the D-Bus inputs are written into this new RAM location. On the LOW-to-HIGH transition of CP, the incremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs reflect the newly entered data. When the RAM address is "1111" the Stack Full output ($\overline{SF}$) is LOW, indicating that no further Call operations should be initiated. If an additional Call operation is performed SP is incremented to (0000), the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-Bus drivers are not enabled during a Call operation.

Return Operation – During the Return operation the previous PC is "popped" to become the current PC.

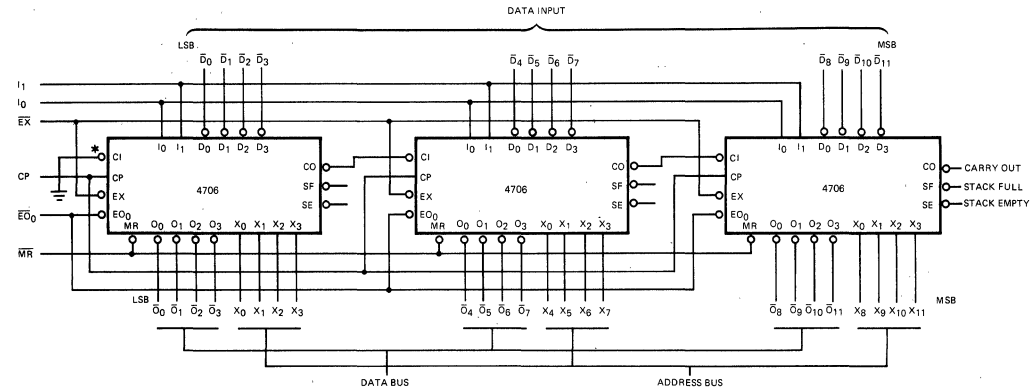
The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the Stack Pointer value, thus decrementing the RAM address. If $\overline{EX}$ goes LOW considerably before CP goes LOW, the O-Bus will correspond to the new value after $\overline{EX}$ goes LOW. If CP goes LOW a short time after $\overline{EX}$, the O-Bus will remain unchanged until the LOW-to-HIGH transition of CP.

On the LOW-to-HIGH transition of CP the decremented Stack Pointer value is loaded into the Stack Pointer and the O-Bus outputs correspond to the new "popped" value.

The X-Bus drivers are not enabled during a Return operation. When the RAM address is "0000", the Stack Empty output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full output ($\overline{SF}$) will go LOW. A LOW on the Master Reset ($\overline{MR}$) causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

EXPANSION – The 4706 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in *Figure 1.* Carry In ($\overline{CI}$) and Carry Out ($\overline{CO}$) are connected to provide automatic increment of the current program counter during Fetch. The $\overline{CI}$ input of the least significant 4706 is tied LOW to ground.

If automatic increment during Fetch is not desired, the $\overline{CI}$ input of the least significant 4706 is held HIGH.



*Tie to V_{DD} to disable automatic increment.

Fig. 1
4706 EXPANSION A 16 BY 12-PROGRAM STACK

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}_0 = V_{DD}$
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}_0 = V_{DD}$
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35		MIN, 25°C	
					250			500			1000		MAX	

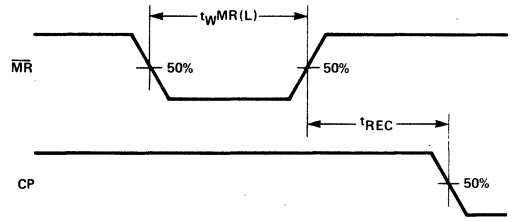
Notes on following pages.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C
(ALL MODES OF OPERATION)

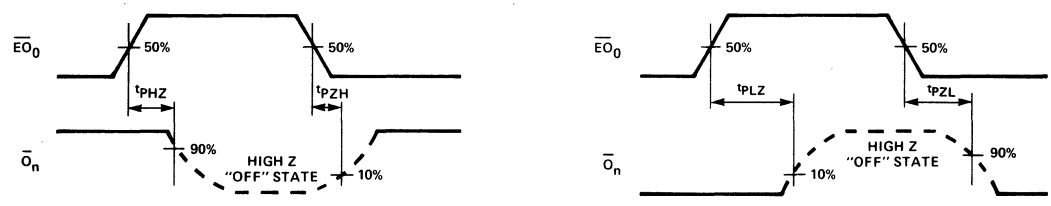
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PZH}	Output Enable Time		121	242		50	100		38	76	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			103	206		38	76		29	58		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		136	272		54	108		36	72	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			99	198		47	94		32	64		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		30	60		15	30		12	24	ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{THL}			30	60		15	30		12	24		
t_{PZH}	Output Enable Time		144	288		62	124		47	94	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			126	252		48	96		34	68		(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		162	324		67	134		45	90	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			121	242		59	118		38	76		(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		60	120		30	60		20	40	ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{THL}			60	120		30	60		20	40		
t_{rec}	$\overline{MR}$ Recovery Time	538	269		440	220		296	148		ns	
$t_W\overline{MR}(L)$	$\overline{MR}$ Minimum Pulse Width	314	157		116	58		74	37		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_WCP(L)$	CP Minimum Pulse Width, LOW	520	260		142	71		80	40		ns	
$t_WCP(H)$	CP Minimum Pulse Width, HIGH	622	311		196	98		90	45			
t_{CW}	Clock Period	1142	571		558	279		440	220		ns	

Notes on following pages.

RESET OPERATION



MINIMUM $\overline{MR}$ PULSE WIDTH AND $\overline{MR}$ RECOVERY TIME



$\overline{EO}_0$ TO OUTPUT ENABLE AND DISABLE TIMES

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

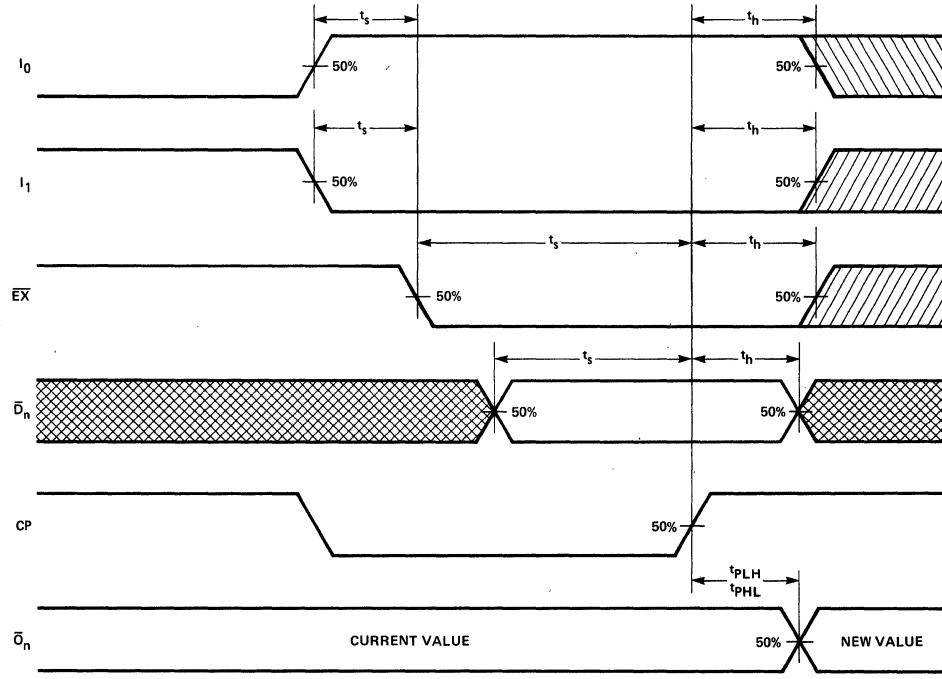
4

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (BRANCH OPERATION)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		236	472		97	194		68	136	ns	C_L = 15 pF Input Transition Times ⩽20 ns
t_{PHL}	CP to $\overline{O}_n$		181	362		68	136		47	194		
t_{PLH}	Propagation Delay,		287	574		109	218		78	156	ns	C_L = 50 pF Input Transition Times ⩽20 ns
t_{PHL}	CP to $\overline{O}_n$		238	476		84	168		61	122		
t_s	Set-Up Time, I_n to $\overline{EX}$	172	86		58	29		42	21		ns	C_L = 15 pF Input Transition Times ⩽20 ns
t_h	Hold Time, I_n to $\overline{EX}$	20	0		15	0		10	0			
t_s	Set-Up Time, $\overline{D}_n$ to CP	182	91		106	53		64	32		ns	
t_h	Hold Time, $\overline{D}_n$ to CP	20	0		15	0		10	0			
t_h	Hold Time, I_n to CP	20	0		15	0		10	0		ns	
$t_w\overline{EX}$	Min. $\overline{EX}$ Pulse Width	188	94		74	37		50	25		ns	

Notes on following pages.

BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

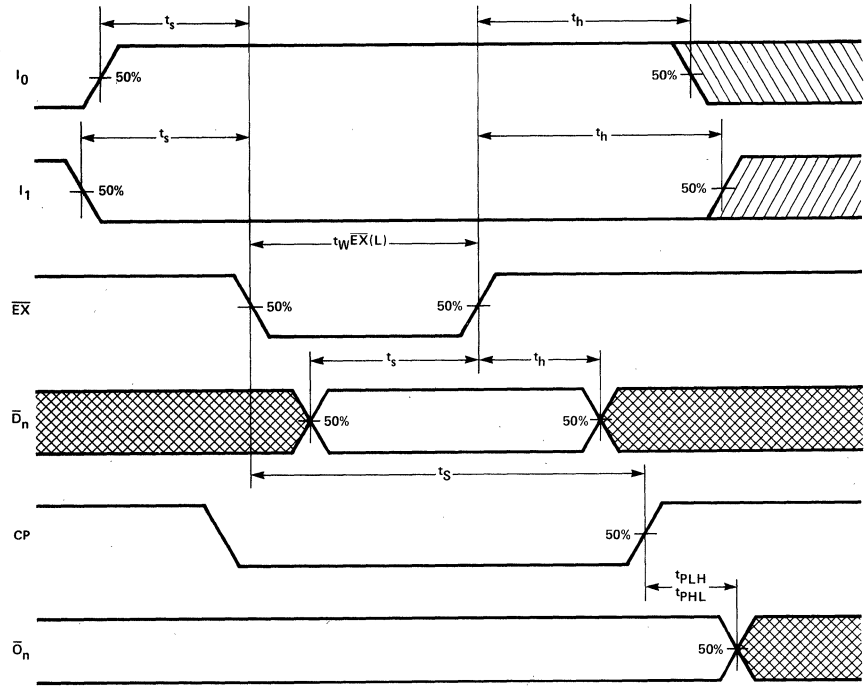


PROPAGATION DELAY CP TO $\overline{O}_n$ AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{D}_n$ TO CP AND I_n TO CP

CONDITIONS: $\overline{EO}_0$ = LOW

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS FOR A BRANCH OPERATION
$\overline{EX}$ GOES HIGH BEFORE CP



PROPAGATION DELAY, CP TO $\overline{O}_n$, MINIMUM $\overline{EX}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{EX}$ TO CP AND I_n TO CP

CONDITIONS: $\overline{EO}_0$ = LOW

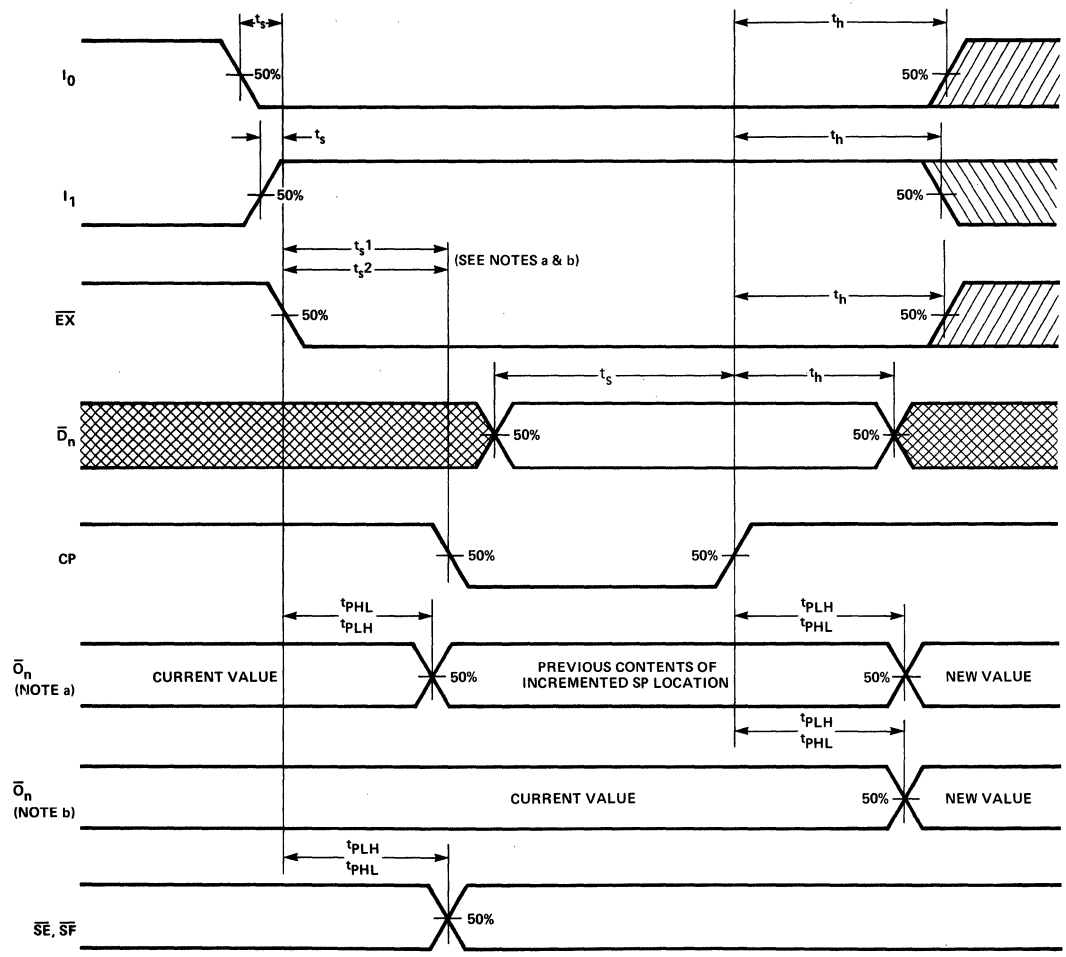
NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (CALL OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O}_n$		481 435	962 870		172 152	344 304		114 98	228 196	ns	C_L = 15 pF Input Transition Times ⩽20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O}_n$		421 570	842 1140		127 171	254 342		93 120	186 240	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$		191 225	382 450		103 120	206 240		73 84	146 168	ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O}_n$		513 461	1026 922		182 161	364 322		121 104	242 208	ns	C_L = 50 pF Input Transition Times ⩽20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O}_n$		480 505	960 1010		134 180	268 360		99 127	198 254	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$		202 240	404 480		110 127	220 254		77 89	154 178	ns	
t_s	Set-Up Time, $\overline{EX}$ to I_n	96	48		48	24		34	17		ns	C_L = 15 pF Input Transition Times ⩽20 ns
t_h	Hold Time, CP to I_n	20	0		15	0		10	0		ns	
$t_{s1}EX$	Set-Up Time, $\overline{EX}$ to CP With Data On $\overline{O}_n$ While CP = LOW	848	424		324	162		186	93		ns	
$t_{s2}EX$	Set-Up Time, $\overline{EX}$ to CP With No Change In $\overline{O}_n$ While CP = LOW	20	0		15	0		10	0		ns	
t_hEX	Hold Time, CP to $\overline{EX}$	20	0		15	0		10	0		ns	
t_s	Set-Up Time, $\overline{D}_n$ to CP	426	213		194	97		128	64		ns	
t_h	Hold Time, $\overline{D}_n$ to CP	20	0		15	0		10	0		ns	

Notes on following pages.

SWITCHING WAVEFORMS FOR A CALL (PUSH) OPERATION



PROPAGATION DELAY, CP TO $\overline{O}_n$, $\overline{EX}$ TO $\overline{O}_n$, $\overline{EX}$ TO $\overline{SE}$ OR $\overline{SF}$, AND SET-UP AND HOLD TIMES, $\overline{EX}$ TO I_n, CP TO I_n, $\overline{D}_n$ TO CP, CP TO $\overline{EX}$.

CONDITIONS: $\overline{EO}_0$ = LOW

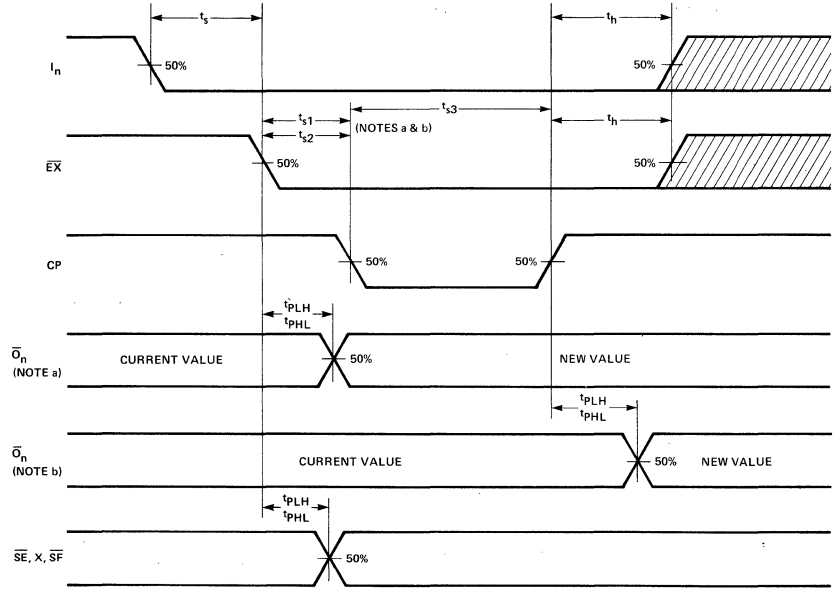
NOTES: a. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW (t_{s1} EX is met).
b. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW (t_{s2} EX is met).
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SWITCHING REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C
(RETURN OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O}_n$		480 445	960 890		181 161	363 322		120 113	240 226	ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O}_n$		479 546	958 1092		141 192	282 384		133 141	266 282	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$		204 220	408 440		98 92	196 184		74 72	148 144	ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O}_n$		510 475	1020 950		193 172	386 344		130 120	260 240	ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O}_n$		505 580	1010 1160		150 205	300 410		142 150	282 300	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$		216 233	432 466		105 78	210 156		79 77	158 154	ns	
t_s	Set-Up Time, $\overline{EX}$ to I_n	62	31		18	9		10	5		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_h	Hold Time, I_n to CP	20	0		15	0		10	0		ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Which Guarantees a New Value On $\overline{O}_n$ While CP is LOW	540	270		266	133		148	74		ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ Must Be Met For Proper Operation	20	0		15	0		10	0		ns	
$t_{s3}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ Must Be Met For Proper Operation	280	140		186	93		70	35		ns	

Notes on following pages.

SWITCHING WAVEFORMS FOR A RETURN (POP) OPERATION



PROPAGATION DELAY, CP TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{SE}$ OR $\overline{SF}$, AND SET-UP AND HOLD TIMES, $\overline{EX}$ TO I_n, I_n TO CP, $\overline{EX}$ TO CP

CONDITIONS: $\overline{EO}_0$ = LOW

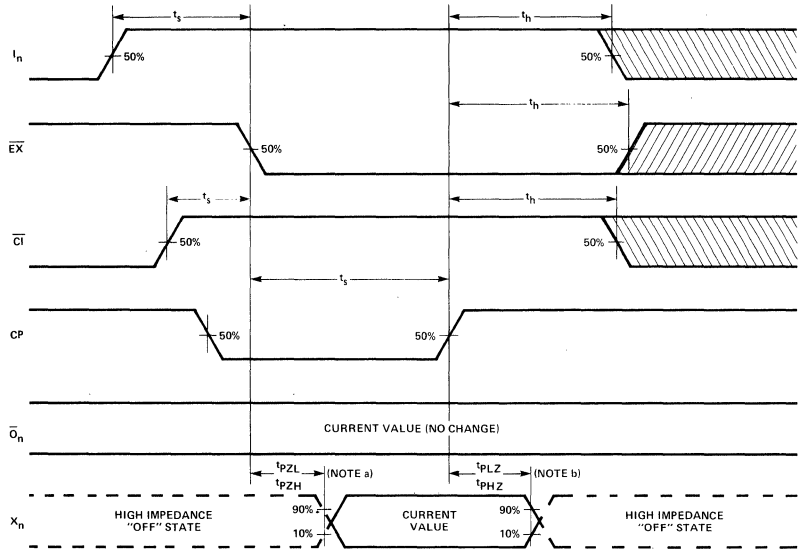
NOTES: a. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($T_{s1}\overline{EX}$ is met).
b. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ are met).
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C
(FETCH OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS (See Note 2)
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		234	468		92	184		65	130	ns	C_L = 15 pF Input Transition Times ⩽20 ns (R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHL}	CP to $\overline{O}_n$		174	348		67	134		47	94		
t_{PZH}	Output Enable		121	242		50	100		38	76	ns	
t_{PZL}	Time (X_n)		103	206		38	76		29	58		
t_{PHZ}	Output Disable		136	272		54	108		36	72	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}	Time (X_n)		99	198		47	94		32	64		
t_{PLH}	Propagation Delay,		274	548		108	216		77	154	ns	C_L = 50 pF Input Transition Times ⩽20 ns (R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHL}	CP to $\overline{O}_n$		215	430		82	164		57	114		
t_{PZH}	Output Enable		144	288		62	124		47	94	ns	
t_{PZL}	Time (X_n)		126	252		48	96		34	68		
t_{PHZ}	Output Disable		162	324		67	134		45	90	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}	Time (X_n)		121	242		59	118		38	76		
t_s	Set-Up Time, I_n to $\overline{EX}$	488	244		134	67		90	45		ns	C_L = 15 pF Input Transition Times ⩽20 ns
t_h	Hold Time, I_n to CP or $\overline{EX}$	20	0		15	0		10	0		ns	
t_s	Set-Up Time, $\overline{EX}$ to CP	644	322		170	85		148	74		ns	
t_s	Set-Up Time, $\overline{CI}$ to CP	570	285		132	66		90	45		ns	
t_h	Hold Time, $\overline{CI}$ to $\overline{EX}$	20	0		15	0		10	0		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4700 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS FOR AN ITERATIVE FETCH

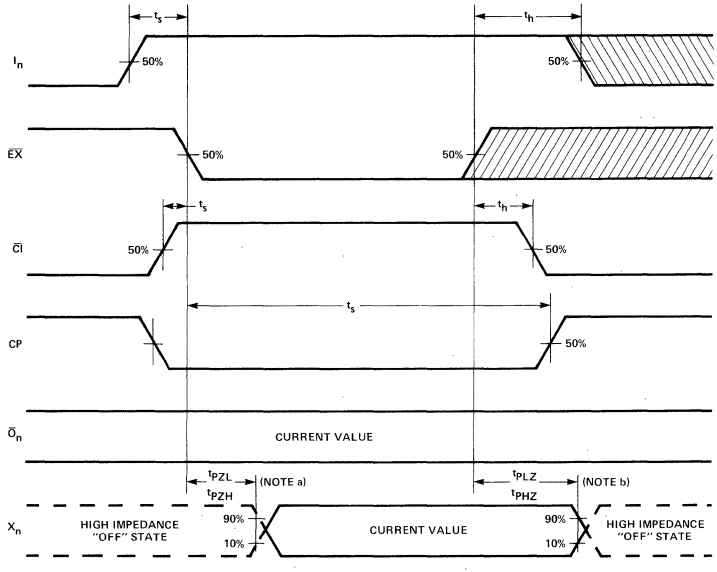


OUTPUT X_n DISABLE DELAY, OUTPUT X_n ENABLE DELAY, AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, I_n TO CP, $\overline{EX}$ TO CP, AND $\overline{CI}$ TO $\overline{EX}$.

CONDITIONS: $\overline{EO}_0$ = LOW, CP GOES HIGH BEFORE $\overline{EX}$

NOTES: a. $X_0 - X_3$ turn on delay measured from time both EX and CP go LOW.
b. $X_0 - X_3$ turn off delay measured from time either EX or CP goes HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

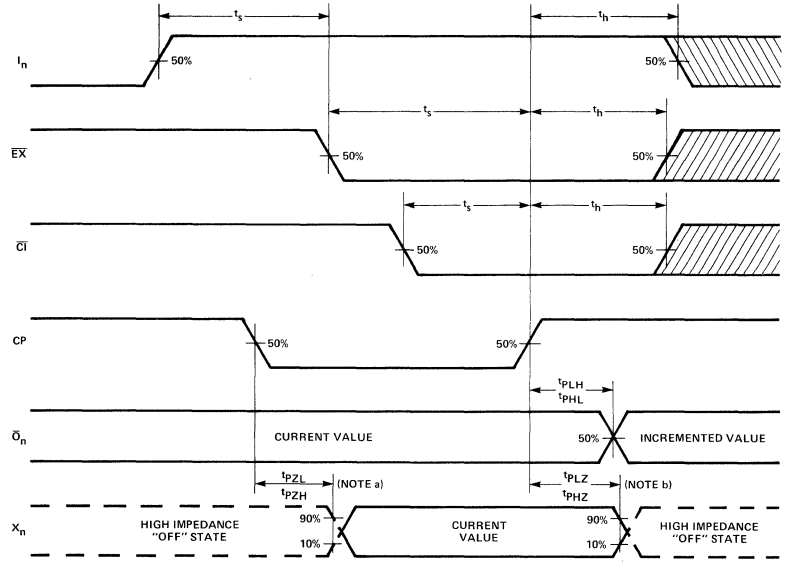
SWITCHING WAVEFORMS FOR AN ITERATIVE FETCH (Cont'd)



OUTPUT X_n ENABLE AND DISABLE TIMES AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{CI}$ TO $\overline{EX}$ AND $\overline{EX}$ TO CP.

CONDITIONS: $\overline{EO}_0$ = LOW, $\overline{EX}$ GOES HIGH BEFORE CP

SWITCHING WAVEFORMS FOR A FETCH OPERATION WITH INCREMENT PC



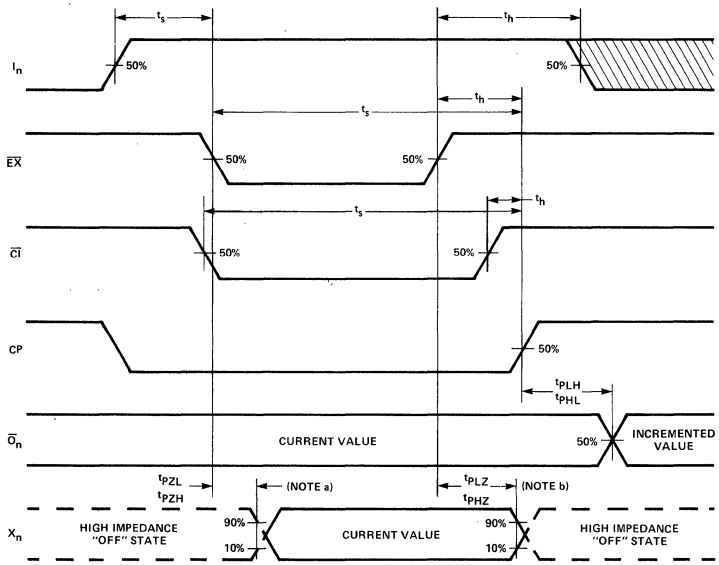
PROPAGATION DELAY, CP TO $\overline{O}_n$, OUTPUT X_n ENABLE AND DISABLE TIMES AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{EX}$ TO CP, AND $\overline{CI}$ TO CP

CONDITIONS: $\overline{EO}_0$ = LOW, CP GOES HIGH BEFORE $\overline{EX}$

NOTES: a. $X_0 - X_3$ turn on delay measured from time both $\overline{EX}$ and CP go LOW.
b. $X_0 - X_3$ turn off delay measured from time either $\overline{EX}$ or CP goes HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

4

SWITCHING WAVEFORMS FOR A FETCH OPERATION WITH INCREMENT PC



PROPAGATION DELAY CP TO $\overline{O}_n$, OUTPUT X_n ENABLE AND DISABLE TIMES, AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{EX}$ TO CP AND $\overline{CI}$ TO CP

CONDITIONS: $\overline{EO}_0$ = LOW, $\overline{EX}$ GOES HIGH BEFORE CP

NOTES: a. $X_0 - X_3$ turn on delay measured from the time both $\overline{EX}$ and CP go LOW.
b. $X_0 - X_3$ turn on delay measured from the time either $\overline{EX}$ or CP go HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

4707/4707B

DATA ACCESS REGISTER

FAIRCHILD CMOS MACROLOGIC

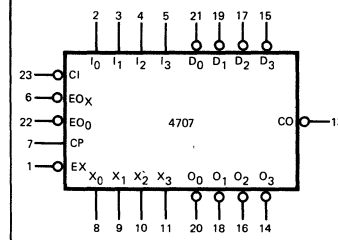
DESCRIPTION – The 4707 Data Access Register (DAR) is designed to perform the memory address functions for RAM resident stack applications. The DAR can implement general registers with an adder network in programmable digital systems. The 4707 contains three 4-bit registers intended for Program Counter (R_0), Stack Pointer (R_1), and Operand Address (R_2). The 4707 implements 16 instructions (see *Table 1*) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 5.3 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The 4707 is fully compatible with all CMOS families.

- **HIGH SPEED – 5.2 MHz MICROINSTRUCTION RATE, TYPICALLY**
- **THREE 4-BIT REGISTERS**
- **16 INSTRUCTIONS FOR REGISTER MANIPULATION**
- **TWO SEPARATE OUTPUT PORTS, ONE TRANSPARENT**
- **RELATIVE ADDRESSING CAPABILITY**
- **3-STATE OUTPUTS**
- **OPTIONAL PRE OR POST ARITHMETIC**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **SLIM 24-PIN PACKAGE**

PIN NAMES

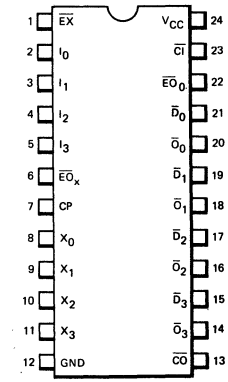
$\overline{D}_0 - \overline{D}_3$	Data Inputs (Active LOW)
$I_0 - I_3$	Instruction Word Inputs
$\overline{CI}$	Carry Input (Active LOW)
$\overline{CO}$	Carry Output (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{EO}_X$	Address Output Enable Input (Active LOW)
$\overline{EO}_0$	Data Output Enable Input (Active LOW)
$X_0 - X_3$	Address Outputs
$\overline{O}_0 - \overline{O}_3$	Data Outputs (Active Low)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

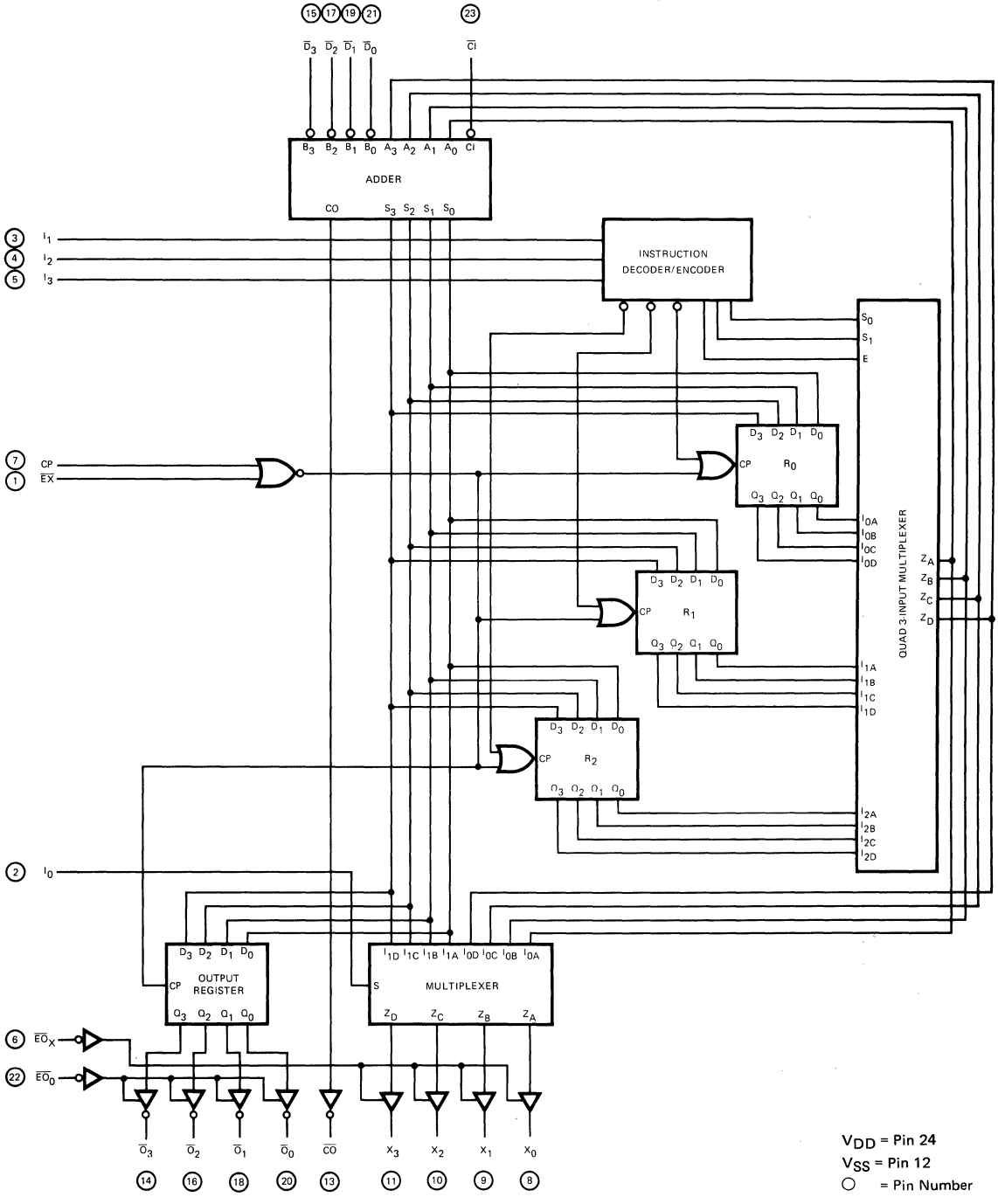
CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 4707 contains a 4-bit slice of three registers (R_0 – R_2), a 4-Bit Adder, 3-state address output buffers (X_0 – X_3) and a separate Output Register with 3-state buffers ($\overline{O}_0$ – $\overline{O}_3$), allowing output of the register contents on the data bus (refer to the block diagram). The DAR performs 16 instructions, selected by I_0 – I_3 inputs, as listed in *Table 1.*

Operation – A microcycle starts as the clock goes HIGH. Data inputs $\overline{D}_0$ – $\overline{D}_3$ are applied to the Adder as one of the operands. Three of the four instruction lines (I_1, I_2, I_3) select which of the three registers, if any, is to be used as the other operand. The LOW-to-HIGH transition of the CP Input writes the result from the Adder into a register (R_0 – R_2) and into the Output Register provided EX is LOW. If the I_0 input is HIGH, the multiplexer routes the result from the Adder to the 3-state buffer controlling the address bus (X_0 – X_3) independent of EX and CP. If I_0 is LOW, the multiplexer routes the output of the selected register directly into the 3-state buffer controlling the address bus (X_0 – X_3), independent of EX and CP.

TABLE 1
INSTRUCTION SET FOR THE 4707

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$
L	L	L	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	L	H	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$ → R_1 and Output Register
L	L	H	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	H	L	L	R_0	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$ → R_2 and Output Register
L	H	L	H	R_0 *plus* $\overline{D}$ *plus* $\overline{CI}$	
L	H	H	L	R_1	R_1 *plus* $\overline{D}$ *plus* $\overline{CI}$ → R_1 and Output Register
L	H	H	H	R_1 *plus* $\overline{D}$ *plus* $\overline{CI}$	
H	L	L	L	R_2	$\overline{D}$ *plus* $\overline{CI}$ → R_2 and Output Register
H	L	L	H	$\overline{D}$ *plus* $\overline{CI}$	
H	L	H	L	R_0	$\overline{D}$ *plus* $\overline{CI}$ → R_0 and Output Register
H	L	H	H	$\overline{D}$ *plus* $\overline{CI}$	
H	H	L	L	R_2	R_2 *plus* $\overline{D}$ *plus* $\overline{CI}$ → R_2 and Output Register
H	H	L	H	R_2 *plus* $\overline{D}$ *plus* $\overline{CI}$	
H	H	H	L	R_1	$\overline{D}$ *plus* $\overline{CI}$ → R_1 and Output Register
H	H	H	H	$\overline{D}$ *plus* $\overline{CI}$	

L = LOW Level
H = HIGH Level

4

4707 EXPANSION – The 4707 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – The 4707 is organized as a 4-bit register slice. The $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths. *Figure 1* is a block diagram of a typical application. Each block of the Macrologic parts represents four identical slices, thus creating a 16-bit array. For this application the register utilizations in the DAR may be as follows: R_0 is the Program Counter (PC), R_1 is the Stack Pointer (SP) for memory resident stack and R_2 contains the operand address. For an instruction fetch, PC can be gated on the X-Bus while it is being incremented (i.e., D-Bus = 1). If the fetched instruction calls for an effective address for calculation, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

A different type of application using the DAR is shown in *Figure 2.* Four 4707s are used here as the major elements in a data path loop closed by four 4704s (DPS). This data path can be used for dedicated multiply/divide function. The DAR register utilization in this application can be as follows :

R_0 is the multiplicand in case of multiply or the divisor in case of divide;
R_1 is the temporary result in case of multiply or the dividand/quotient in case of divide;
R_2 is the product in case of multiply or a temporary register in case of divide.

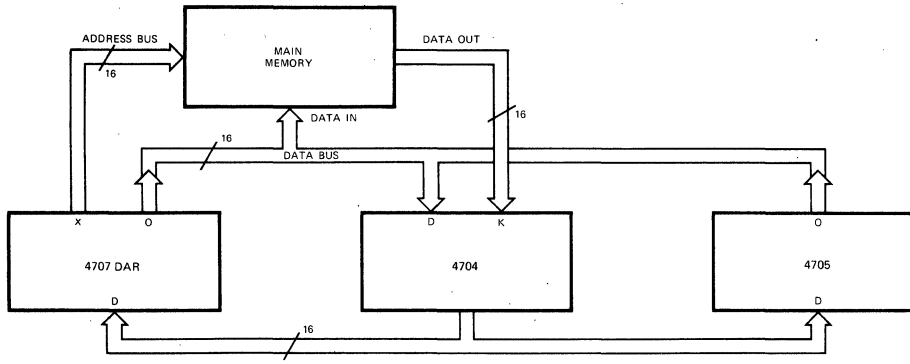


Fig. 1
TYPICAL MEMORY ADDRESS APPLICATION

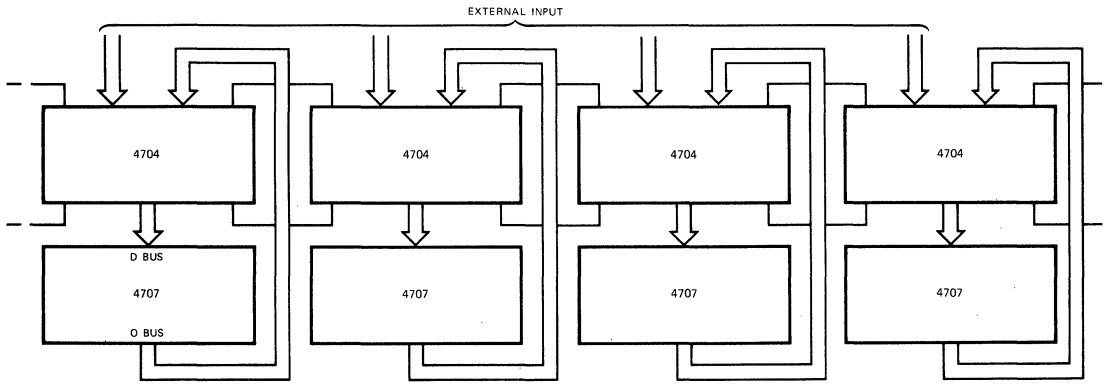


Fig. 2
TYPICAL DATA PATH APPLICATION

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF HIGH Current	XC			0.5 30			1.0 60		0.2 12		μA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{EO}_0 = V_{DD}$, $\overline{EO}_X = V_{DD}$
		XM			0.05 3.0			0.1 6.0		0.02 1.2			MIN, 25°C MAX	
I_{OZL}	Output OFF LOW Current	XC			−0.5 −30			−1.0 −60		−0.2 −12		μA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{EO}_0 = V_{DD}$, $\overline{EO}_X = V_{DD}$
		XM			−0.05 −3.0			−0.1 −6.0		−0.02 −1.2			MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			32.5 250			65 500			130 1000	μA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			8.75 250			17.5 500			35 1000	μA	MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to $\overline{Q}_n$		189 203	378 406		84 86	168 172		64 63	128 126	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to X_n With I_0 = LOW		265 215	530 430		113 82	226 164		95 62	190 124	ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to X_n With I_0 = HIGH		286 272	572 544		130 113	260 226		107 75	214 150	ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n with I_0 = LOW		259 217	518 434		101 83	202 166		82 72	164 144	ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = HIGH		331 343	662 686		131 131	262 262		99 101	198 202	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D}_n$ to X_n		190 177	380 354		82 66	164 172		62 48	124 96	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to X_n		235 235	470 470		116 125	232 250		76 81	152 162	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_0 to X_n		137 126	274 252		63 52	126 104		47 37	94 74	ns	
t_{PLH} t_{PHL}	Propagation Delay, Positive-going Internal Clock to $\overline{CO}$		232 286	464 572		104 119	208 238		70 81	140 162	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$		102 113	204 226		38 41	76 82		26 28	52 56	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D}_n$ to $\overline{CO}$		126 130	252 260		46 51	92 102		35 37	70 74	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to $\overline{CO}$		219 244	438 488		113 126	226 252		68 68	136 136	ns	
t_{PZH} t_{PZL}	Output Enable Time		77 87	154 174		28 31	56 62		19 21	38 42	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		49 58	98 116		24 24	48 48		20 20	40 40	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		54 33	108 66		31 20	62 40		27 18	54 36	ns	

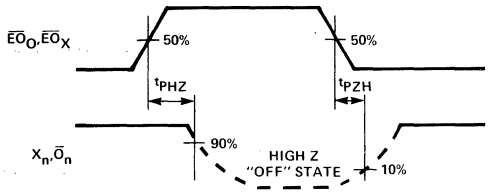
4

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

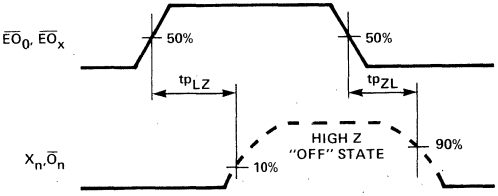
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to $\overline{Q}_n$		243 232	486 464		113 99	226 198		68 70	136 140	ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to X_n With I_0 = LOW		288 243	576 486		134 93	268 186		125 70	250 140	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to X_n With I_0 = HIGH		383 302	766 604		139 119	278 238		126 91	252 182	ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = LOW		288 244	576 488		134 93	268 186		125 63	250 126	ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = HIGH		221 358	442 716		97 146	194 292		69 110	138 220	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D}_n$ to X_n		221 211	442 422		97 79	194 158		69 55	138 110	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to X_n		276 277	552 554		136 146	272 292		89 95	178 190	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_0 to X_n		168 137	336 274		82 63	164 126		59 47	118 94	ns	
t_{PLH} t_{PHL}	Propagation Delay, Positive-going Internal Clock to $\overline{CO}$		258 325	516 650		127 141	254 282		80 91	160 182	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$		132 143	264 286		51 53	102 106		32 35	64 70	ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D}_n$ to $\overline{CO}$		152 149	304 298		63 65	126 130		46 46	92 92	ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1 - I_3 to $\overline{CO}$		274 305	548 610		142 158	284 316		85 85	170 170	ns	
t_{PZH} t_{PZL}	Output Enable Time		79 90	158 180		30 34	60 68		14 23	28 46	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		53 61	106 122		26 28	52 56		22 23	44 46	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		105 62	210 124		54 31	108 62		45 22	90 44	ns	
$t_wCP(H)$	Internal CP minimum Pulse Width (HIGH)	282	141		240	120		176	88		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_wCP(L)$	Internal CP Minimum Pulse Width (LOW)	102	51		48	24		44	22		ns	
t_s	Set-up Time, I_1 - I_3 to Internal Clock	218	109		82	41		60	30		ns	
t_h	Hold Time, I_1 - I_3 to Internal Clock	−48	−96		−17	−34		−12	−24		ns	
t_s	Set-up Time, $\overline{D}_n$, $\overline{CI}$ to Internal Clock	170	85		88	44		58	29		ns	
t_h	Hold Time, $\overline{D}_n$, $\overline{CI}$ to Internal Clock	28	14		30	15		28	14		ns	
t_s	Set-up Time, $\overline{CI}$ to Internal Clock	82	41		44	22		38	19		ns	
t_h	Hold Time, $\overline{CI}$ to Internal Clock	112	56		58	29		42	21		ns	
t_{CW}	Internal Clock Period (Note 3)	388	194		170	85		146	73		ns	
f_{MAX}	Input Count Frequency (Note 5)	2.6	5.2		5.9	11.8		6.8	13.7		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. The Internal Clock is generated from CP and $\overline{EX}$. The Internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW. For timing considerations the $\overline{EX}$, CP two input active LOW NAND gate is considered to exhibit no propagation delay. Actual timing requirements are referenced to the external CP and $\overline{EX}$ inputs.
4. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
5. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
6. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

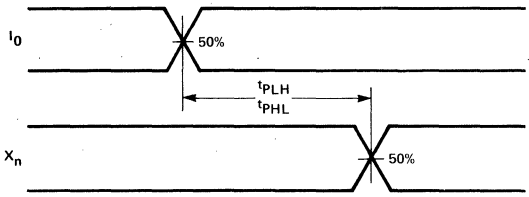
SWITCHING WAVEFORMS



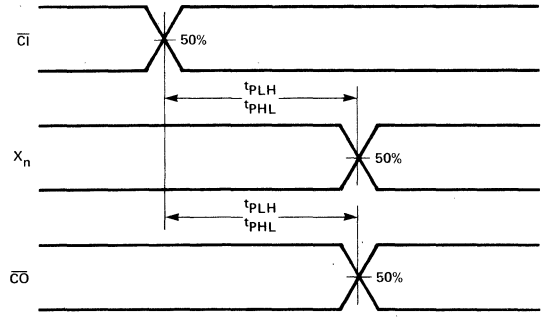
OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



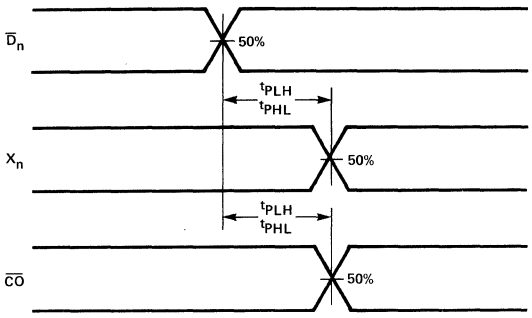
OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



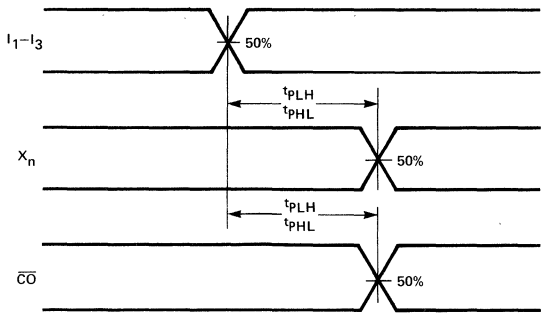
PROPAGATION DELAY, I_0 TO X_n
CONDITIONS: $\overline{EO}_X$ = LOW



PROPAGATION DELAY, $\overline{CI}$ TO X_n AND $\overline{CI}$ TO $\overline{CO}$
CONDITIONS: $\overline{EO}_X$ = LOW, I_0 = HIGH



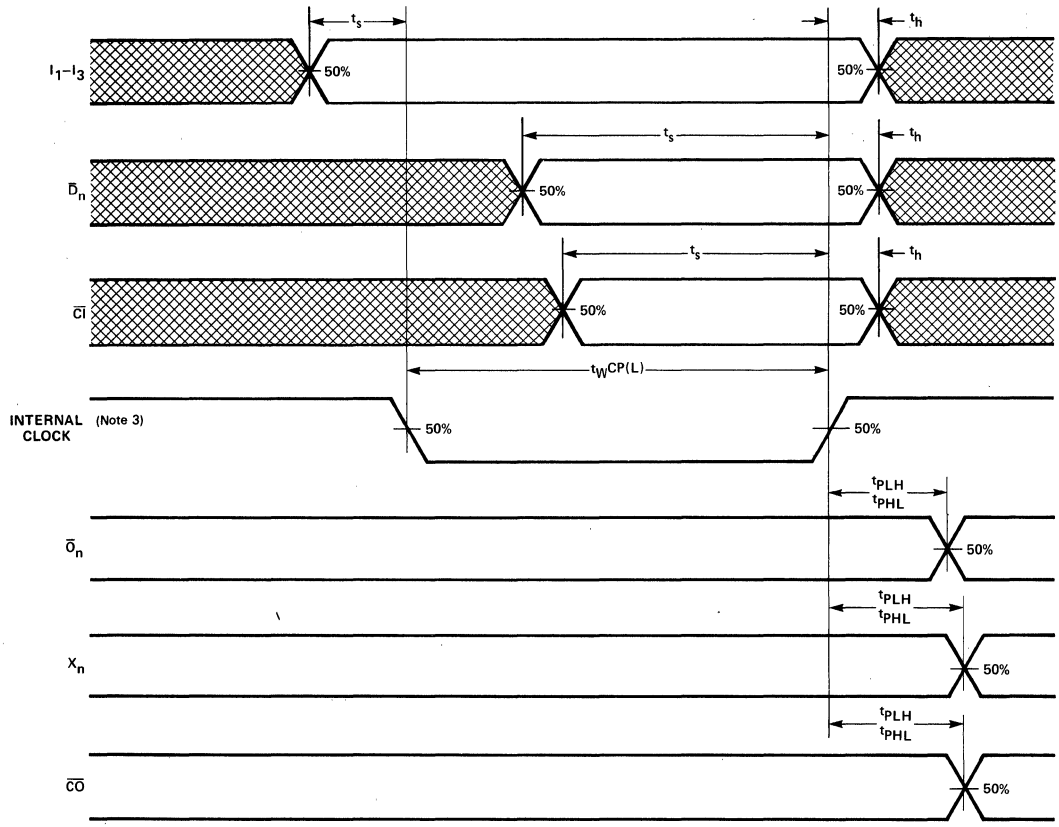
PROPAGATION DELAY, $\overline{D}_n$ TO X_n AND $\overline{D}_n$ TO $\overline{CO}$
CONDITIONS: $\overline{EO}_X$ = LOW, I_0 = HIGH



PROPAGATION DELAY, I_1–I_3 TO $\overline{CO}$ AND I_1–I_3 TO X_n
CONDITIONS: $\overline{EO}_X$ = LOW

4

SWITCHING WAVEFORMS (Cont'd)



PROPAGATION DELAYS, INTERNAL CLOCK TO $\overline{O}_n$, INTERNAL CLOCK TO X_n, INTERNAL CLOCK TO $\overline{CO}$, SET-UP AND HOLD TIMES, I_1–I_3 TO INTERNAL CLOCK, $\overline{D}_n$ TO INTERNAL CLOCK, $\overline{CI}$ TO INTERNAL CLOCK, AND MINIMUM INTERNAL CLOCK PULSE WIDTH

CONDITIONS: $\overline{EO}_X = \overline{EO}_O$ = LOW

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

4708/4708B
MICROPROGRAM SEQUENCER
FAIRCHILD CMOS MACROLOGIC

DESCRIPTION – The 4708 Microprogram Sequencer controls the order in which microinstructions are fetched from the control memory. It contains a 10-bit program counter, a 4-level last-in first-out stack with associated stack control logic, an Input Multiplexer, an Instruction Decoder, a 10-bit Incrementer and a 4-bit Test Register. It can control up to a maximum of 1024 words of memory. For larger word capacities, external paging can be used. The 4708 is controlled by a 4-bit instruction input. The instruction set includes Fetch, Conditional and Unconditional Branches, Branch to Subroutine and Return from Subroutine.

There are seven test inputs – four participate in conditional branches (T_0–T_3), and three in multiway branches (MW_0–MW_2). The conditional test inputs (T_0–T_3) are flip-flop buffered. These flip-flops can be tested individually by appropriate branch instructions. The three multiway-test inputs (MW_0–MW_2) are used to form the least significant three bits of the branch address for a multiway branch. Thus, branching occurs at one of eight unique locations depending on the bit pattern present on these three inputs.

The 4708 is designed to operate in pipeline or non-pipeline mode as specified by the user. The device operates synchronously with the Clock input (CP) and can be initialized using the Master Reset input ($\overline{MR}$).

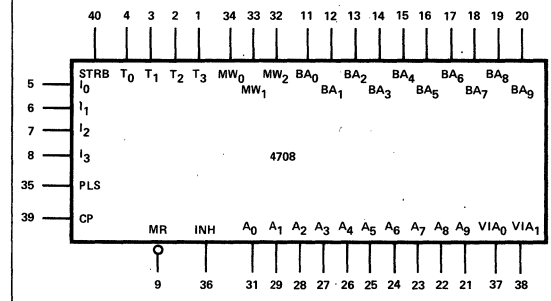
The 4708 is fabricated using Isoplanar C CMOS technology and is fully compatible with all CMOS families.

- **CONTROLS 1024 WORDS OF MICROPROGRAM MEMORY (10-BIT ADDRESS)**
- **UNRESTRICTED BRANCHING WITHIN 10-BIT ADDRESS SPACE**
- **16 INSTRUCTIONS**
- **FOUR FLIP-FLOP BUFFERED TEST INPUTS FOR CONDITIONAL BRANCHES**
- **8-WAY BRANCH CAPABILITY**
- **PIPELINE/NON-PIPELINE MODE OF OPERATION**

PIN NAMES

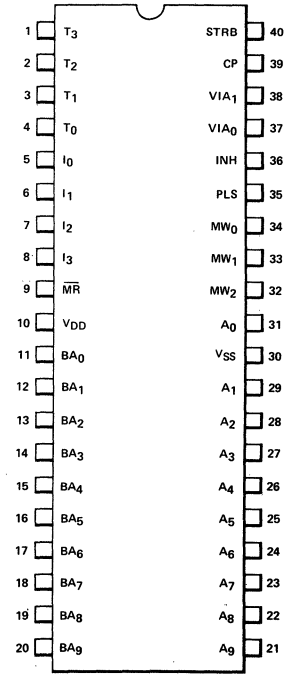
BA_0 – BA_9	Branch Address Inputs
T_0 – T_3	Test Inputs
MW_0 – MW_2	Multiway Branch Inputs
I_0 – I_3	Instruction Inputs
PLS	Pipeline Select Input
$\overline{MR}$	Master Reset Input (Active LOW)
CP	Clock Pulse Input
STRB	Strobe Input
A_0 – A_9	Address Outputs
VIA_0, VIA_1	VIA Outputs
INH	Inhibit Output

LOGIC SYMBOL

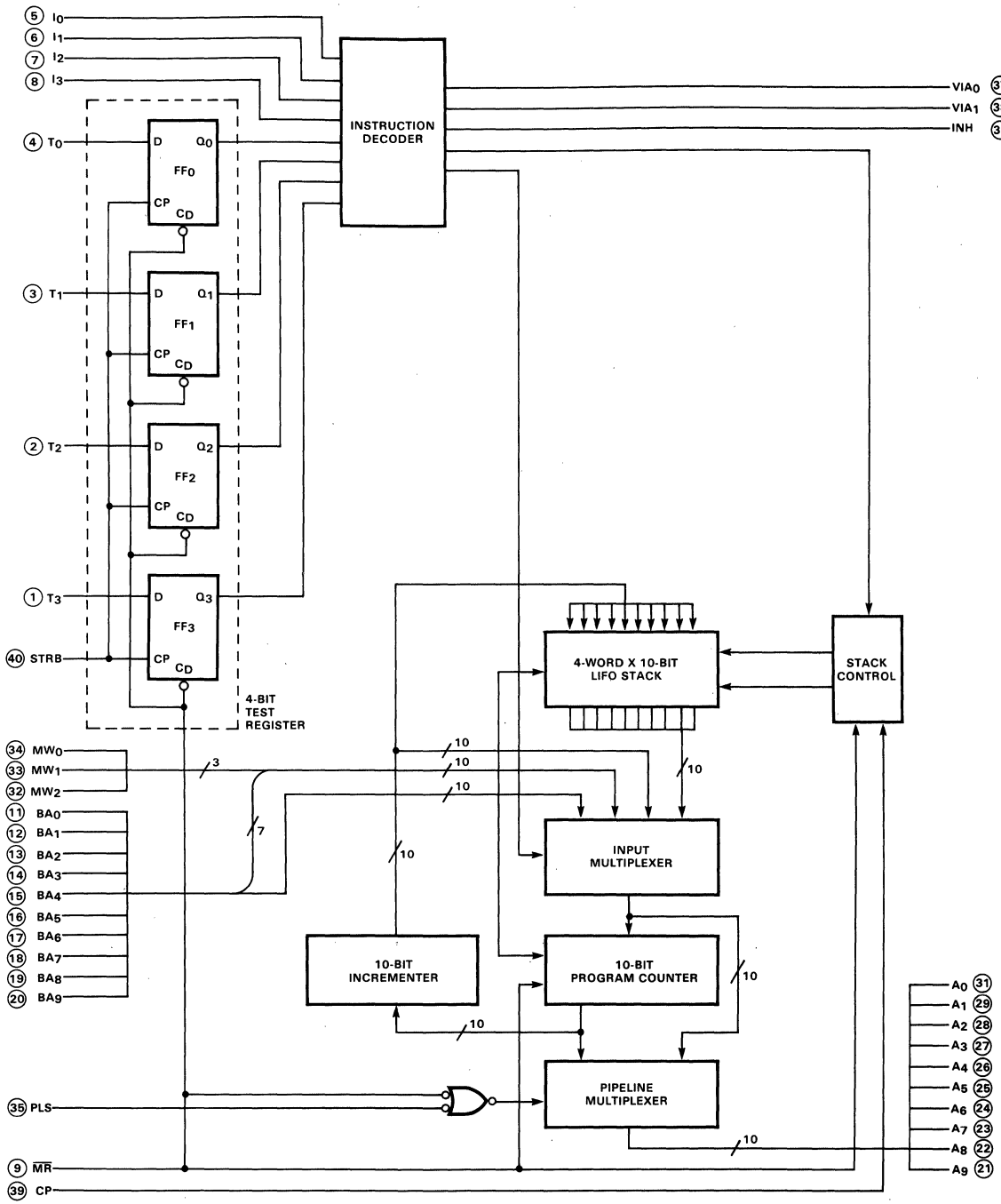


V_{DD} = Pin 10
V_{SS} = Pin 30

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



V_{DD} = Pin 10

V_{SS} = Pin 30

◯ = Pin Number

TABLE 1
4708 INSTRUCTION SET

	MNEMONIC	DEFINITION	$I_3I_2I_1I_0$	$T_3T_2T_1T_0$	$O_9O_8O_7$---$O_2O_1O_0$	VIA_1VIA_0	INH	DESCRIPTION OF OPERATION
Unconditional Branch Instructions	BRV_0	Branch VIA_0	L H L L	X X X X	BA_9 BA_8--BA_1 BA_0	L L	H	BA_0 - BA_9 → PC
	BRV_1	Branch VIA_1	L H L H	X X X X	BA_9 BA_8--BA_1 BA_0	L H	H	BA_0 - BA_9 → PC
	BRV_2	Branch VIA_2	L H H L	X X X X	BA_9 BA_8--BA_1 BA_0	H L	H	BA_0 - BA_9 → PC
	BRV_3	Branch VIA_3	L H H H	X X X X	BA_9 BA_8--BA_1 BA_0	H H	H	BA_0 - BA_9 → PC
	BMW	Branch Multiway	L L H H	X X X X	BA_9 BA_3--MW_2 MW_0	L L	H	MW_0 - MW_2, BA_3 - BA_9 → PC
	BSR	Branch to Subroutine	L L L H	X X X X	BA_9 BA_8--BA_1 BA_0	L L	H	BA_0 - BA_9 → PC & Push the Stack
Conditional Branch Instructions	BTH_0	Branch on T_0 HIGH	H H L L	X X X H X X X L	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 0 is HIGH: BA_0 - BA_9 → PC If Test Register 0 is LOW: PC+1 → PC
	BTH_1	Branch on T_1 HIGH	H H L H	X X H X X X L X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 1 is HIGH: BA_0 - BA_9 → PC If Test Register 1 is LOW: PC+1 → PC
	BTH_2	Branch on T_2 HIGH	H H H L	X H X X X L X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 2 is HIGH: BA_0 - BA_9 → PC If Test Register 2 is LOW: PC+1 → PC
	BTH_3	Branch on T_3 HIGH	H H H	H X X X L X X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 3 is HIGH: BA_0 - BA_9 → PC If Test Register 3 is LOW: PC+1 → PC
	BTL_0	Branch on T_0 LOW	H L L L	X X X L X X X H	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 0 is LOW: BA_0 - BA_9 → PC If Test Register 0 is HIGH: PC+1 → PC
	BTL_1	Branch on T_1 LOW	H L L H	X X L X X X H X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 1 is LOW: BA_0 - BA_9 → PC If Test Register 1 is HIGH: PC+1 → PC
	BTL_2	Branch on T_2 LOW	H L H L	X L X X X H X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 2 is LOW: BA_0 - BA_9 → PC If Test Register 2 is HIGH: PC+1 → PC
	BTL_3	Branch on T_3 LOW	H L H H	L X X X H X X X	BA_9 BA_8--BA_1 BA_0 PC+1	L L	H	If Test Register 3 is LOW: BA_0 - BA_9 → PC If Test Register 3 is HIGH: PC+1 → PC
Miscellaneous Instructions	RTS	Return from Subroutine	L L L L	X X X X	Contents of the Stack Addressed by Read Pointer	L L	L	Pop the Stack
	FTCH	FETCH	L L H L	X X X X	PC+1	L L	L	PC+1 → PC

L = LOW Level
H = HIGH Level
X = Don't Care

4

FUNCTIONAL DESCRIPTION – The 4708 Microprogram Sequencer, shown in the block diagram consists of a 10-bit Program Counter (PC), a 4-word by 10-bit Last-In First-Out (LIFO) Stack with associated Stack Control, an Input Multiplexer, a Pipeline Multiplexer, an Instruction Decoder, a 10-bit Incrementer, and a 4-bit Test Register comprised of four edge-triggered D flip-flops.

The Pipeline Multiplexer has two ports – the PC output provides the input port for the non-pipeline mode and the Input Multiplexer output provides the input port for the pipeline mode. Port selection is controlled by the Pipeline Select (PLS) and Master Reset (MR) inputs. A LOW level on the MR input forces the non-pipeline mode of operation and clears the PC. Thus when the 4708 is initialized by the MR input, the A_0 through A_9 outputs are LOW regardless of the state of the PLS input. A LOW level on the PLS input specifies non-pipeline mode and a HIGH specifies pipeline mode.

The Program Counter is a 10-bit edge-triggered register. The LOW-to-HIGH transition on the Clock (CP) input loads the Input Multiplexer output into the PC. The PC input is always the address of the next microinstruction. Because of the edge-triggered nature of the PC register, the PC output remains static for a full clock cycle. Thus, in the non-pipeline mode, the PC output can be used to address a control memory built with static devices without storing the memory output in an external microinstruction register. However, in the pipeline mode, the 4708 provides the next address information as soon as available; therefore, execution of a microinstruction can be overlapped with the fetching of the next microinstruction. To ensure microinstruction stability for a full clock cycle, the control-memory output should be buffered with an external microinstruction register.

The Input Multiplexer receives data from four different sources. One port is the output of the LIFO Stack; a second is the output of the 10-bit Incrementer. The Incrementer always adds one to the PC contents. The third and fourth ports are the branch and multiway-branch ports, the former comprised of the Branch Address inputs (BA_0 – BA_9) and the latter comprised of the seven most significant Branch Address inputs (BA_3 through BA_9) and the three Multiway inputs (MW_0 through MW_2).

The 4-word by 10-bit LIFO Stack is a RAM and receives data from the Incrementer output. The Stack Control logic generates the appropriate control signals, while stack pointers in the Stack Control generate the read and write addresses.

The 4-bit Test Register consists of four type-D flip-flops. The data inputs, which are the four Test inputs (T_0 through T_3), are loaded on the LOW-to-HIGH transition of the Strobe input (STRB).

The Instruction Decoder receives the 4-bit Instruction input (I_0 through I_3) and the Test Register output and generates the VIA_0, VIA_1 and Inhibit (INH) outputs of the 4708. In addition, it generates appropriate logic signals for the Stack Control and Input Multiplexer.

Stack Control – The 4708 has a 4-level subroutine nesting capability as detailed in *Figure 1*. The R_0 and R_1 (Read Address) inputs to the 4-word by 10-bit LIFO Stack specify the address from which information will be read. The W_0 and W_1 (Write Address) inputs specify the address into which information will be written; and the 4708 Incrementer output provides the information to be written into the stack (see block diagram). In addition, writing into the memory is controlled by the Write Enable ($\overline{WE}$) and $\overline{CP}$ inputs.

The R_0, R_1 and W_0, W_1 inputs of the LIFO Stack are derived from the outputs of a 3-bit edge-triggered register called the Stack Pointer (SP). The least significant two bits (SP_0 and SP_1) of this register are the read address inputs to the memory. The SP outputs are also connected to a Stack-Pointer Incrementer and a Decrementer that generate SP + 1 and SP – 1 respectively. The least significant two bits of the Incrementer are the write address bits for the memory.

The outputs of the Incrementer, Decrementer and the Stack Pointer are fed as inputs to a 3-port Stack-Pointer Multiplexer which, in turn, feeds the Stack Pointer inputs. Stack pointer loading always occurs on the LOW-to-HIGH transition of the CP input. The MR input clears the Stack Pointer. The Stack Pointer Control receives two inputs from the 4708 Instruction Decoder – the BSR input, which is active whenever a Branch-to-Subroutine (BSR) instruction is present on the I_0 through I_3 inputs, and the RTS input, which is active whenever a Return-from-Subroutine (RTS) instruction is specified. The port selection of the Stack Pointer Multiplexer is controlled by the outputs of the Stack Pointer Control. For all 4708 instructions except BSR and RTS, the Stack Pointer Multiplexer selects the Stack Pointer outputs as the instruction source.

Writing into the memory takes place whenever the $\overline{WE}$ and $\overline{CP}$ inputs are LOW. Note that the most significant register bit, SP_2, controls the $\overline{WE}$ input to prevent writing into the memory when all four locations are filled with return addresses. Thus the 4708 does not store and return addresses beyond four nesting levels.

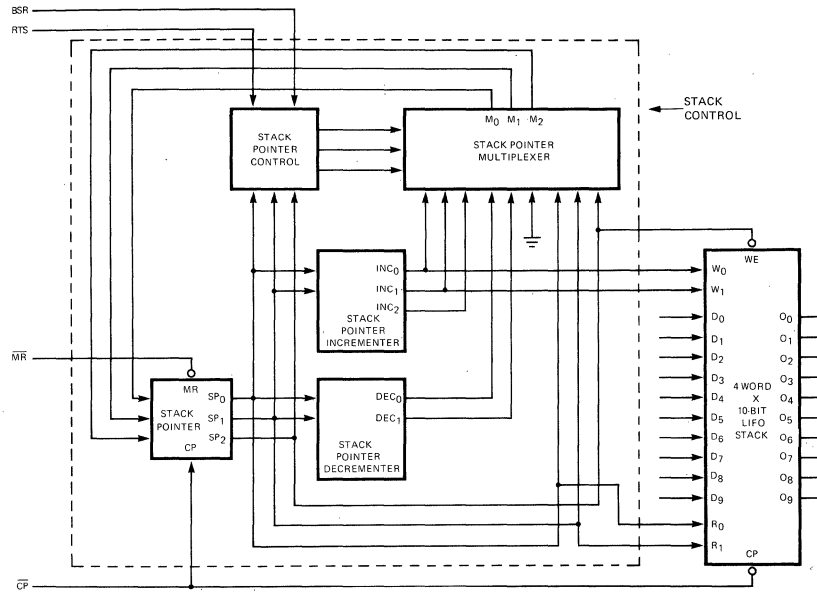


Fig. 1
STACK CONTROL

4708 INSTRUCTIONS

The 4708 instruction set has 16 instructions (*Table 1*). These instructions can be divided into three groups – unconditional branches, conditional branches and miscellaneous – and are specified by appropriate logic levels on the $I_0 - I_3$ inputs.

The unconditional branch group consists of four Branch VIA instructions ($BRV_0 - BRV_3$), Branch Multiway (BMW) and Branch to Subroutine (BSR). This group requires that the next address be explicitly specified on the BA inputs.

The conditional branch group consists of eight instructions, Branch Test HIGH ($BTH_0 - BTH_3$) and Branch Test LOW ($BTL_0 - BTL_3$), for interrogating the four test flip-flops of the 4708 individually. The $BTH_0 - BTH_3$ instructions test flip-flops $T_0 - T_3$ respectively for a HIGH on the Q output (see block diagram). Similarly $BTL_0 - BTL_3$ test for a LOW on the corresponding Q output. If the test condition is satisfied, the next address is taken from the Branch Address ($BA_0 - BA_9$) inputs. If the test condition is not satisified the 4708 performs a Fetch operation.

The miscellaneous group consists of two instructions – Fetch (FTCH) and Return from Subroutine (RTS). These instructions do not require explicit specification of the next address. For the FTCH instruction, the next address is assumed to be the address of the current microinstruction + 1. For RTS, the next address is taken from the Stack. *The Inhibit (INH) output of the* 4708 *is LOW only for FTCH and RTS instructions. For all other instruction, the INH output is HIGH.*

The VIA outputs of the 4708 (VIA_0, VIA_1) are LOW for all instructions except $BRV_1 - BRV_3$. For BRV_1, the VIA_0 is HIGH and VIA_1 LOW. For BRV_2, the VIA_0 is LOW and VIA_1 HIGH. For BRV_3, both VIA_0 and VIA_1 are HIGH.

Unconditional Branches

$BRV_0 - BRV_3$ – Whenever a Branch VIA instruction code is present on the $I_0 - I_3$ inputs, the Instruction Decoder (see block diagram) establishes the appropriate HIGH/LOW pattern on the VIA_0 and VIA_1 outputs per *Table 1*. The Instruction Decoder also forces the INH output HIGH. Moreover, the $BA_0 - BA_9$ inputs are selected as the source of the next address by the Input Multiplexer.

If the 4708 is in the pipeline mode (PLS input HIGH), the Pipeline Multiplexer transfers the $BA_0 - BA_9$ inputs to the $A_0 - A_9$ outputs. The $BA_0 - BA_9$ inputs are loaded into the PC on the LOW-to-HIGH transition of the CP input. Conversely, if the non-pipeline mode of operation is selected, the $BA_0 - BA_9$ inputs appear on the output only after the LOW-to-HIGH transition of the CP input.

BMW – For a Branch Multiway instruction, the Instruction Decoder forces the VIA_0 and VIA_1 outputs LOW and INH output HIGH. The Input Multiplexer selects the $BA_3 - BA_9$ inputs as the most significant seven bits and $MW_0 - MW_2$ inputs as the least significant three bits of the next address. If the pipeline mode of operation is selected, the next address formed by the Input Multiplexer ($BA_3 - BA_9$ and $MW_0 - MW_2$ inputs) is transferred to the $A_0 - A_9$ outputs. On the LOW-to-HIGH transition of the CP input, this next address is also leaded into the PC. For non-pipeline mode, the next address is available on the $A_0 - A_9$ output only after the CP transition.

BSR – During a Branch-to-Subroutine instruction, the Instruction Decoder forces a LOW on the VIA_0 and VIA_1 outputs and a HIGH on the INH output. The Input Multiplexer selects the $BA_0 - BA_9$ inputs as the source for the next address. If the pipeline mode is selected, this next address is transferred to the $A_0 - A_9$ outputs by the Pipeline Multiplexer. As usual, the PC is updated with this next address on the LOW-to-HIGH transition of the CP input. During non-pipeline operation, the next address appears on the output only after the CP transition.

The PC holds the address of the current microinstruction. For the BSR instruction, the return address must be stored in the Stack, which is fed by the PC through an Incrementer (see block diagram). When the CP input is LOW, the incremented value is written into the Stack as a return address. The LOW-to-HIGH transition of the CP input not only loads the PC with the next address, *i.e.*, $BA_0 - BA_9$ inputs, but also increments the Stack Pointer as explained above.

Conditional Branches

$BTH_0 - BTH_3$ – For a Branch Test HIGH instruction, the Instruction Decoder establishes a LOW on VIA_0 and VIA_1 outputs and HIGH on the INH output. It then tests for a HIGH on the Q output of the corresponding flip-flop in the test register. If a HIGH level is found, the Input Multiplexer selects the $BA_0 - BA_9$ inputs as the source for the next address.

On the other hand, if the tested Q output of the flip-flop is LOW, the Incrementer output is selected as the source of the next address by the Input Multiplexer. In either case, the PC is loaded with the next address on the LOW-to-HIGH transition of the CP input. As usual, if the pipeline mode is selected, the next address is transferred to the $A_0 - A_9$ outputs. For non-pipeline mode, the next address appears on the output after the clock transition.

$BTL_0 - BTL_3$ – Operation of the Branch Test LOW instructions is identical to $BTH_0 - BTH_3$ except that Q outputs of the test register flip-flops are tested for a LOW. If the tested output is LOW, a branch occurs. If tested output is HIGH the Incrementer output is the next address.

Miscellaneous

FTCH – For a Fetch instruction, the Instruction Decoder establishes a LOW on the VIA_0 and VIA_1 outputs. In addition, the INH output is also LOW. The Input Multiplexer selects the Incrementer output as the next address. If pipeline mode is selected, the Incrementer output is transferred to the $A_0 - A_9$ outputs. For non-pipeline mode, the incremented address appears at the output only after the clock transition.

RTS – For a Return-from-Subroutine instruction, the Instruction Decoder establishes a LOW on the VIA_0, VIA_1 and the INH outputs. The Input Multiplexer selects the Stack output as the source of the next address. As usual, for the pipeline mode, the next address is transferred to the output by the Pipeline Multiplexer. For non-pipeline operation, the next address appears on the output only after the clock transition. In addition, this instruction also decrements the Stack Pointer as described above.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			32.5			65			130	μA	MIN, 25°C	All Inputs at 0 V or V_{DD}
					250			500			1000		MAX	
		XM			8.75			17.5			35	μA	MIN, 25°C	
					250			500			1000		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 15 pF, Input Transition ⩽ 20 ns. (Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		240			120			96		ns	I_1=I_2=V_{DD}, I_3=V_{SS}
t_{PHL}	I_n to VIA_n		320			160			128			Input=I_0, Output=VIA_0
t_{PLH}	Propagation Delay,		240			120			96		ns	I_1=V_{DD}, I_2=I_3=V_{SS}
t_{PHL}	I_n to INH		320			160			128			Input=I_0, Output=INH
t_{PLH}	Propagation Delay,		360			180			144		ns	I_1=V_{DD}, PLS=I_0=
t_{PHL}	CP to A_n(Non-Pipeline)		400			200			160			I_2=I_3=V_{SS}
t_{PLH}	Propagation Delay,		720			360			288		ns	PLS=I_1=V_{DD}
t_{PHL}	CP to A_n (Pipeline)		784			392			314			I_0=I_2=I_3=V_{SS}
t_{PLH}	Propagation Delay,		240			120			96		ns	PLS=I_0=I_1=I_2=V_{DD}
t_{PHL}	BA_n to A_n (Pipeline)		320			160			128			I_3=V_{SS}

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 15 pF, Input Transition ⩽ 20 ns. (Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_n to A_n (Pipeline)		640 720			320 360			256 288		ns	I_0=I_1=BA_0=PLS=V_{DD} I_3=MW_0=V_{SS} Output=A_0, Input=I_2
t_{TLH} t_{THL}	Output Transition Time		50 50			30 30			24 24		ns	
t_{rec}	$\overline{MR}$ Recovery Time		120			120			96		ns	
$t_W\overline{MR}$(L)	$\overline{MR}$ Minimum Pulse Width		280			140			112		ns	
t_WCP(H)	CP Minimum Pulse Width (HIGH)		280			140			112		ns	I_1=V_{DD}, I_0=I_2=
t_WCP(L)	CP Minimum Pulse Width (LOW)		240			120			96		ns	I_3=PLS=V_{SS}
t_s t_h	Set-Up Time, BA_n to CP Hold Time, BA_n to CP		240 −10			120 −5			96 −3		ns	I_2=V_{DD}, I_0=I_1=I_3= PLS=V_{SS}, Input=BA_0, Output=A_0
t_s t_h	Set-Up Time, I_n to CP Hold Time, I_n to CP		720 −10			360 −5			288 −3		ns	I_0=I_1=BA_0=V_{DD}, I_0= MW_0, PLS=V_{SS}, Input=I_2, Output=A_0
t_s t_h	Set-Up Time, T_n to STRB Hold Time, T_n to STRB		120 −10			60 −5			48 −3		ns	I_2=I_3=PLS=V_{DD}, I_0=I_1=BA_0=V_{SS}, Input=T_0, Output=A_0
t_s	Set-Up Time, STRB to CP (Required to achieve a conditional branch in the same microcycle)		480			240			192		ns	I_3=T_0=V_{DD}, I_0=I_1= I_2=PLS=BA_0=V_{SS}, Input=STRB, Output=A_0
f_{MAX}	Input Count Frequency (Note 4)										MHz	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, C_L = 50 pF, Input Transition Times ⩽ 20 ns (Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_n to VIA_n		290 385			145 195			116 156		ns	I_1=I_2=V_{DD}, I_3=V_{SS} Input=I_0, Output=VIA_0
t_{PLH} t_{PHL}	Propagation Delay, I_n to INH		290 385			145 195			116 156		ns	I_1=V_{DD}, I_2=I_3=V_{SS} Input=I_0, Output=INH
t_{PLH} t_{PHL}	Propagation Delay, CP to A_n (Non-Pipeline)		430 480			215 240			172 192		ns	I_1=V_{DD}, PLS=I_0= I_2=I_3=V_{SS}
t_{PLH} t_{PHL}	Propagation Delay, CP to A_n (Pipeline)		860 945			430 475			344 380		ns	PLS=I_1=V_{DD}, I_0=I_2=I_3=V_{SS}
t_{PLH} t_{PHL}	Propagation Delay, BA_n to A_n (Pipeline)		290 385			145 195			116 156		ns	PLS=I_0=I_1=I_2= V_{DD}, I_3=V_{SS}
t_{PLH} t_{PHL}	Propagation Delay, I_n to A_n(Pipeline)		770 870			385 435			308 348		ns	I_0=I_1=BA_0=PLS=V_{DD}, I_3=MW_0=V_{SS} Output=A_0, Input=I_2
t_{TLH} t_{THL}	Output Transition Time		60 60			40 40			32 32		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4700 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_W), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

4710/4710B

REGISTER STACK • 16×4 RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD CMOS MACROLOGIC

DESCRIPTION – The 4710 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 4710 is fully compatible with all CMOS families.

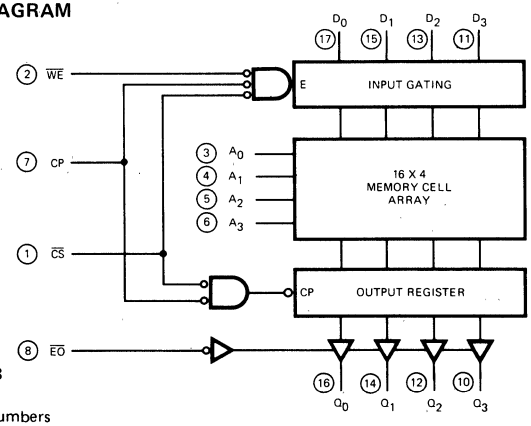
- **EDGE-TRIGGERED OUTPUT REGISTER**
- **TYPICAL ACCESS TIME OF 48 ns at V_{DD} = 10 V**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **18-PIN PACKAGE**

PIN NAMES

A_0-A_3	Address Inputs
D_0-D_3	Data Inputs
$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
CP	Clock Input (Outputs Change on LOW to HIGH Transition)
Q_0-Q_3	Outputs

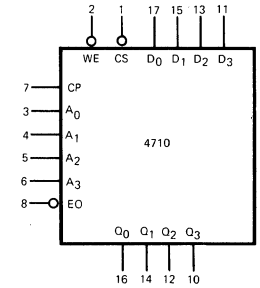
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) 10 LOW Unit Loads measured at 0.5 V.

BLOCK DIAGRAM



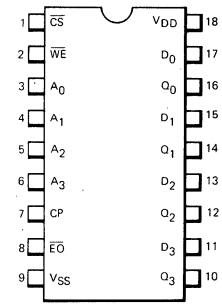
V_{DD} = Pin 18
V_{SS} = Pin 9
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 18
V_{SS} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION – The 4710 consists of a 16 X 4-bit RAM selected by four address inputs (A_0 – A_3) and an edge-triggered 4-bit Output Register with 3-state Output Buffers.

Write Operation – When the three control inputs: Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the data inputs (D_0 – D_3) is written into the memory location selected by the address inputs (A_0 – A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes provided set-up time criteria are met.

Read Operation – Whenever $\overline{CS}$ is LOW and CP goes from LOW-to-HIGH, the contents of the memory location selected by the address inputs (A_0 – A_3) is edge triggered into the Output Register.

A 3-State Output Enable ($\overline{EO}$) controls the output buffers. When $\overline{EO}$ is HIGH the four outputs (Q_0 – Q_3) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the outputs are determined by the state of the Output Register.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			60		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			–0.5			–1.0		–0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					–30			–6.0		–12			MAX	
		XM			–0.05			–0.1		–0.02			MIN, 25°C	
					–3.0			–6.0		–1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All Inputs at at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5.0			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

4

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

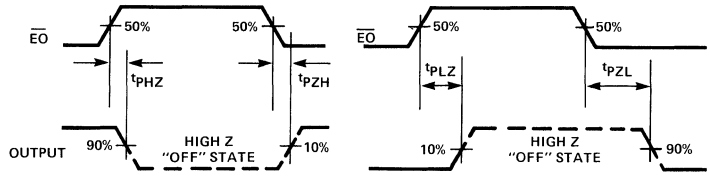
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
	READ MODE											C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH}	Propagation Delay, CP to Output		120	240		48	96		36	72	ns	
t_{PHL}			109	218		43	86		31	62		
t_{PZH}	Enable Time, $\overline{EO}$ to Output		52	104		19	38		15	30	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PZL}			81	162		28	56		20	40		
t_{PHZ}	Disable Time, $\overline{EO}$ to Output		52	104		26	52		20	40	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}			66	132		29	58		20	40		
t_{TLH}	Output Transition Time		45	90		25	50		17	34	ns	
t_{THL}			50	100		25	50		17	34		
	READ MODE											C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH}	Propagation Delay, CP to Output		146	292		56	112		40	80	ns	
t_{PHL}			125	250		49	98		34	68		
t_{PZH}	Enable Time, $\overline{EO}$ to Output		57	114		20	40		16	32	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PZL}			81	162		31	62		23	46		
t_{PHZ}	Disable Time, $\overline{EO}$ to Output		57	114		29	58		23	46	ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}			72	144		31	62		25	50		
t_{TLH}	Output Transition Time		75	150		45	90		35	70	ns	
t_{THL}			80	160		45	90		35	70		
	WRITE MODE											C_L = 15 pF Input Transition Times ≤ 20 ns
$t_W\overline{WE}$	Minimum $\overline{WE}$ Pulse Width (Note 4)	218	109		104	52		62	31		ns	
$t_W\overline{CS}$	Minimum $\overline{CS}$ Pulse Width (Note 4)	226	113		124	62		74	37		ns	
t_WCP	Minimum CP Pulse Width (Note 4)	240	120		124	62		74	37		ns	
t_s	Set-Up Time $\overline{CS}$ to $\overline{WE}$ (Note 5)	326	163		198	99		134	67		ns	
t_h	Hold Time, $\overline{CS}$ to $\overline{WE}$ (Note 5)	0	−15		0	−10		0	−5		ns	
t_s	Set-Up Time, $\overline{CS}$ to CP	186	93		104	52		68	34		ns	
t_h	Hold Time, $\overline{CS}$ to CP	0	−15		0	−10		0	−5		ns	
t_s	Set-Up Time, $\overline{D}_n$ to $\overline{WE}$ (Note 5)	176	68		70	35		48	24		ns	
t_h	Hold Time, $\overline{D}_n$ to $\overline{WE}$ (Note 5)	0	−15		0	−10		0	−5		ns	
t_s	Set-Up Time, Address to $\overline{WE}$ (Note 5)	206	103		100	50		58	29		ns	
t_h	Hold Time, Address to $\overline{WE}$ (Note 5)	0	−15		0	−10		0	−5		ns	
	READ MODE											
t_s	Set-Up Time Address to CP	706	353		372	186		208	104		ns	
t_h	Hold Time Address to CP	0	−15		0	−10		0	−5		ns	

NOTES:

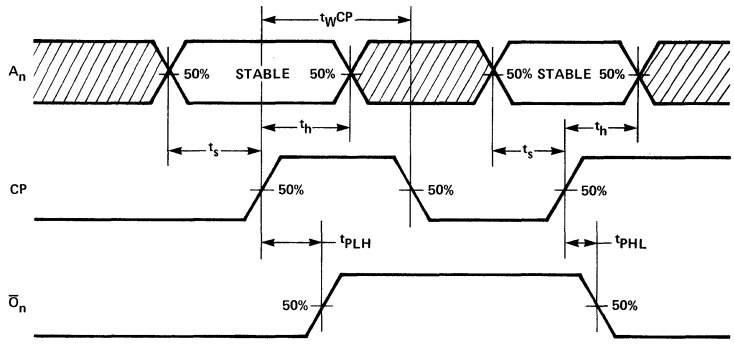
1. Additional DC Characteristics are listed in this section under 4700 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition times are graphically described in this section under 4700 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and Output Transition Times (t_{TLH} and t_{THL}) will change with output load capacities (C_L). Set-up Times (t_s). Hold Times (t_h), Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. Writing occurs when $\overline{WE}$, $\overline{CE}$, and CP are LOW.
5. Assuming $\overline{WE}$ is utilized as a Writing STROBE.

SWITCHING WAVEFORMS

READ MODE



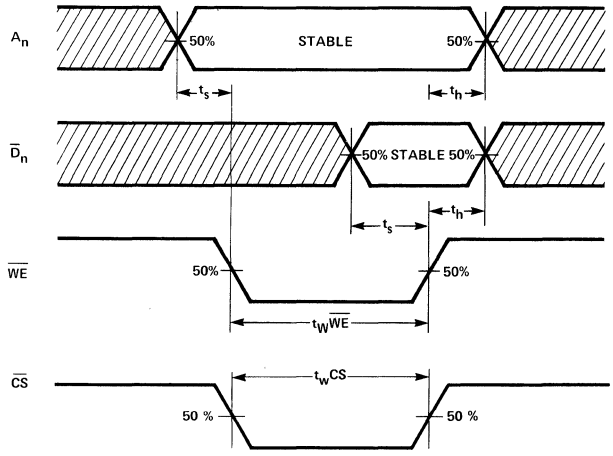
$\overline{EO}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM CP PULSE WIDTH, PROPAGATION DELAY CLOCK TO OUTPUT, AND SET-UP AND HOLD TIMES ADDRESS TO CLOCK

CONDITIONS: $\overline{CS}$ = $\overline{EO}$ = LOW, $\overline{WE}$ = HIGH

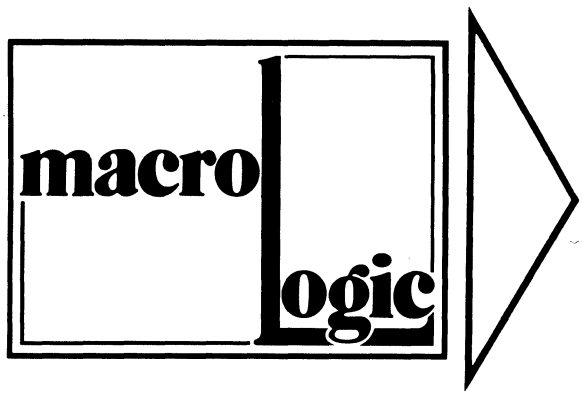
WRITE MODE



MINIMUM $\overline{CS}$ PULSE WIDTH, MINIMUM WRITE ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES ADDRESS TO $\overline{WE}$, DATA TO $\overline{WE}$, AND $\overline{CS}$ TO WE

CONDITIONS: CP = LOW

NOTE: Set-Up (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.



MACROLOGIC APPLICATIONS

MICROPROGRAMMING WITH MACROLOGIC

Microprogram Execution Modes

Any microprogrammed system, in effect, consists of two major elements—a controller and controllee (data path). The data path usually consists of ALUs, general registers, stacks etc., and can readily be implemented with Macrologic devices (ALRS, DPS etc.). The controller for operating the data path can be designed to perform in either pipeline or non-pipeline mode. The non-pipeline controller is simply a 9408 and a control store that usually consists of a PROM (ROM) or RAM *(Figure 5-1).* In a pipeline system, an edge-triggered microinstruction register is needed in addition to the memory and the 9408 *(Figure 5-2).*

In a non-pipeline system, a microinstruction is read from the control store and executed in the same clock cycle. No attempt is made to read the control store for the next microinstruction until the execution of the current instruction is complete.

Most microprogrammed systems are designed as synchronous machines. The actual data-path logic dictates the maximum frequency at which the data path will operate properly. However, a non-pipeline system cannot be run at this speed because of the overhead imposed by the controller. Reading a microinstruction involves setting up the address and accessing the memory. Because of the synchronous nature of the system, setting up the address is in sympathy with the clock. The sum of the 9408 propagation delay (CP to Address outputs) and the read access time of the memory should be added to the allowable clock cycle time of the data path to arrive at the actual system speed. The overhead imposed by the microprogram controller could be a significant percentage of the data-path speed. This is an inefficient use of the data-path resources. Also, the total system may not have the desired operating speed. However, the pipeline mode can overcome this disadvantage.

In a pipeline system, reading the next microinstruction overlaps the execution of the current instruction. This requires holding the current microinstruction in a microinstruction register as shown in *Figure 5-2.* If the sum of 9408 propagation delay (Instruction input to Address output in pipeline mode), the read access time of the memory, set-up and propagation-delay times of the microinstruction register is less than the intrinsic data-path clock period, then a full overlap can be achieved and the actual system speed is not affected by the controller overhead. Otherwise, the system speed is determined by propagation, set-up and access times of the controller alone. In practice, pipeline systems achieve much higher operating speeds than non-pipeline systems.

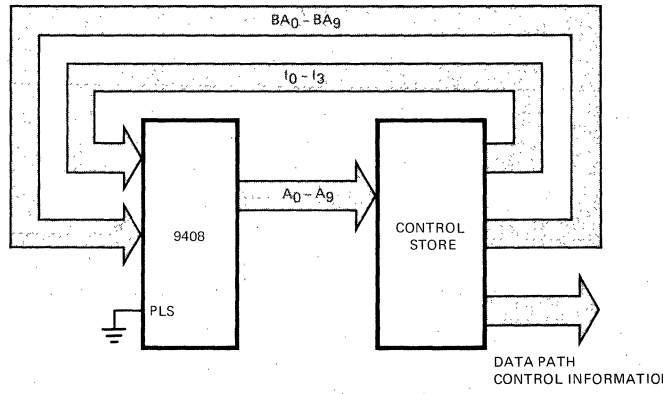


Fig. 5-1 Non-Pipeline System

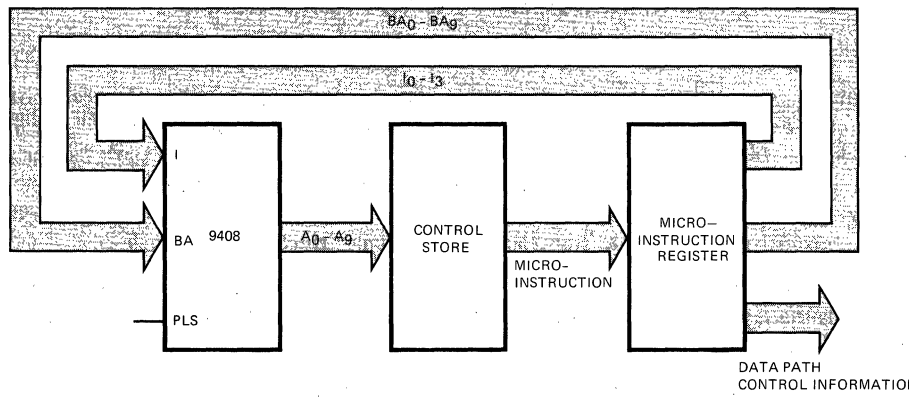


Fig. 5-2 Pipeline System

In many instances, a microprogram written for non-pipeline system cannot be executed in pipeline mode. However, 9408 architecture is designed so that the same microprogram can be executed in pipeline or non-pipeline mode without any modification. This feature gives the user a distinct advantage since he can design his high end product with pipeline execution and lower end product with non-pipeline. No microprogram changes are required thus significant cost advantages can be realized.

Initializing The Microprogram

In microprogrammed systems, the current control-memory address identifies the current control state, while the contents of the addressed location, i.e. microinstruction, provides the information required to establish proper control-signal combinations for the data path and to choose the next address. A microprogrammed system is inherently a sequential machine and initialization of the controller is necessary for proper system operation.

Initialization of the non-pipeline systems is rather straightforward. Whenever the 9408 $\overline{MR}$ input is LOW, the program counter (PC) is cleared and hence all the Address outputs of the 9408 will be LOW. This address then defines the starting location for the microprogram execution. The PC is held clear as long as the $\overline{MR}$ input is LOW. A simple initialization scheme is shown in *Figure 5-3.* The flip-flop is held clear by a low-level Reset input. The $\overline{Q}$ output of this flip-flop is connected to the $\overline{MR}$ input of the 9408. As long as the reset signal is LOW, the Raw Clock signal is blocked by the OR gate, due to the HIGH level from the $\overline{Q}$ output, thus the System Clock output will be HIGH. When the Reset input goes HIGH, the following LOW-to-HIGH transition of the Raw Clock sets the flip-flop. The OR gate passes the Raw Clock input as the System Clock which then can be used to drive the data path and the CP input of the 9408.

In a pipeline system, merely addressing the starting location is not enough. The first microinstruction must be loaded into the microinstruction register to prime the pipe. The Raw Clock can be used for this purpose—a LOW-to-HIGH transition loads the microinstruction register. As before, the System Clock operates on the data path and the 9408.

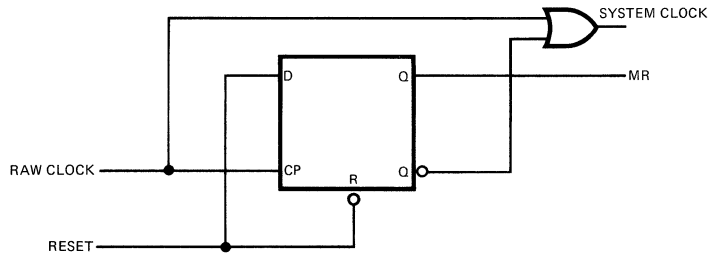


Fig. 5-3 Initialization Circuit

Sharing The Control Fields For Next Address

A straightforward microinstruction consists of fields for specifying data-path control and an explicit specification of the next address. An explicit next-address specification is mandatory in many microprogram sequencer architectures. However, in the 9408, a Fetch instruction is provided to facilitate writing a microprogram where a large number of instructions fit naturally into sequential memory locations. The next address for a Fetch instruction need not be explicit; it is always implied to be PC + 1. In general, the total number of bits required for the data-path control (total control-field width) is more than the number of bits needed to explicitly specify the next address. Thus, if there is an easy way to use the control fields, or part of them, to specify the address, significant reduction of the microinstruction width can be achieved. The Inhibit output of the 9408 is provided to facilitate sharing of microinstruction fields.

There are two 9408 instructions that do not require next-address specification, FTCH and RTS. The remaining 14 instructions fall into a branch class requiring an external next address. The Inhibit output is LOW for FTCH and RTS only and HIGH for all other instructions. Thus, if the system clock can be inhibited from operating the data path whenever the Inhibit output is HIGH, then the microinstruction field that normally operates on the data path can be fed into the 9408 as the next address. Inhibiting the data path operation is extremely simple with the Macrologic processor elements. In some Macrologic systems, the devices are connected as a bussed system; an example is shown in *Figure 5-4*. Although the 9405A and 9406 devices derive their instructions from the same microinstruction field, either the 9405A or the 9406 can be individually selected to respond to an instruction by controlling the $\overline{EX}$ inputs. Macrologic systems can employ an encoded field in the microinstruction, called destination field, for this purpose. A decoder is commonly used to drive the individual $\overline{EX}$ inputs. Now, if the Inhibit output of the 9408 is connected to the Enable input of the decoder, all $\overline{EX}$ inputs are HIGH for branch-class instructions. Thus clocking would not affect the devices. This technique of sharing fields is beneficial only if a large percentage of the operations is from sequential memory locations with an occasional random branch. If a microprogram has many branch instructions, the extra clock cycle needed for branch operation may affect the system speed.

Handling The Test Inputs

In microprogrammed systems, it is often necessary to test the status of external conditions. Often, these inputs are derived from the ALU of the data path as condition codes. For example, the ALRS (9405A) provides four status signals—Carry ($\overline{W}$), Negative ($\overline{X}$), Overflow ($\overline{Y}$), and Zero (Z). These signals can be connected to the $T_0 - T_3$ inputs of 9408 so that a LOW-to-HIGH transistion of the STRB will load them

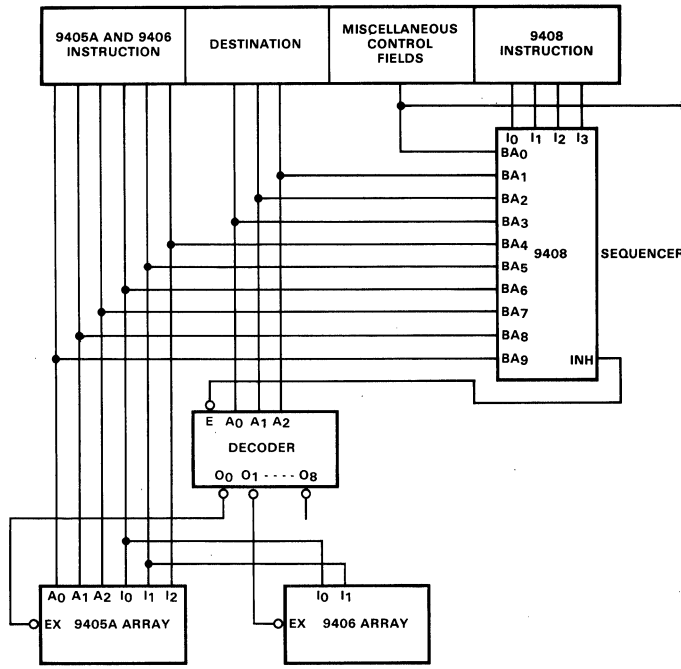
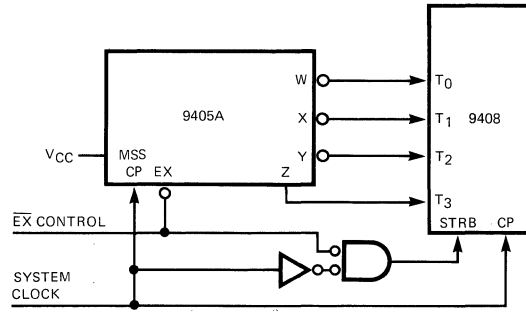


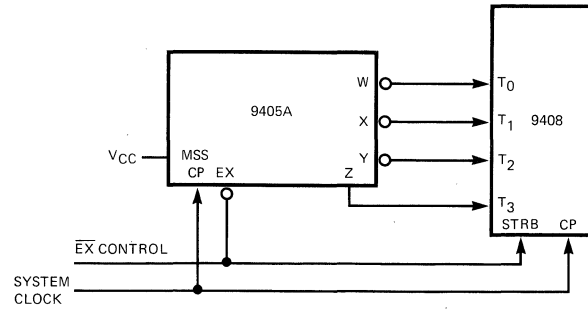
Fig. 5-4 Sharing the Control Fields

into the 4-bit test register. Although the STRB and CP inputs of the 9408 can be connected together, in most systems, the STRB input is derived from the system clock by appropriate gating. This is done so that the test register is only affected during those microinstructions that involve an ALU operation. *Figure 5-5* illustrates test-input handling. In both modes of operation, the ALRS status can be stored in the 9408 during a microcycle and tested during subsequent microcycles using appropriate conditional branch instructions.

It should be noted that the 9405A provides the status signals towards the end of the microcycle and the system clock should be chosen so that the 9408 set up (test-to-strobe) time is satisfied. In *Figure 5-5a*, gating the system clock with $\overline{EX}$ inputs of the 9405A assures that the test register operates only for those microcycles that affect the 9405A. Also note that the 9405A is operating in accumulator mode. If the 9405A is operating in the general register mode *(Figure 5-5b)* the $\overline{EX}$ is a negative pulse; hence, it can be connected to the STRB input of the 9408. (Refer to the 9405A data sheet for operation details.)



(a) 9405A Operated in Accumulator Mode



(b) 9405A Operated in General Register Mode

Fig. 5-5 Handling the 9408 Test Inputs

Expanding The Multiway Inputs

Three 9408 inputs participate in multiway branch operation. This gives eight individual branch addresses depending on the bit pattern present on the $MW_0 - MW_2$ inputs during a BMW instruction. Although the 9408 provides only three inputs for this purpose, they can be readily expanded. For example, in *Figure 5-6*, the $MW_0 - MW_2$ are obtained from three 8-input multiplexers. During a BMW instruction, the 9408 ignores the $BA_0 - BA_2$ inputs; thus these three bits can be used to control the multiplexers and increase the Branch Multiway inputs.

Using the VIA Outputs

Since a microinstruction contains information relating to the address of the next microinstruction, it would seem that the $BA_0 - BA_9$ inputs of the 9408 are derived from the next address field. However, in most practical systems, the $BA_0 - BA_9$ inputs must be obtained from other sources in addition to the next microinstruction address field.

For example, a system designed to emulate the instruction set of a target computer contains a "macroinstruction register" to hold the bit patterns corresponding to the target instruction that currently requires execution. There is a routine in the control store starting at a certain address which corresponds to the current macroinstruction. It is simple to connect an address mapper, consisting of PROMS or PLAs, to the macroinstruction register. The address inputs (input variables) are the outputs of the macroinstruction register and the mapper output is the starting address of the microsequence for the current target instruction. Thus, if the mapper output is used as another source of next address, a very fast macroinstruction decoding can be accomplished. This source selection could easily be accomplished by feeding the addresses from different sources into a 4-input multiplexer and using the VIA outputs of the 9408 to select the appropriate sets of inputs.

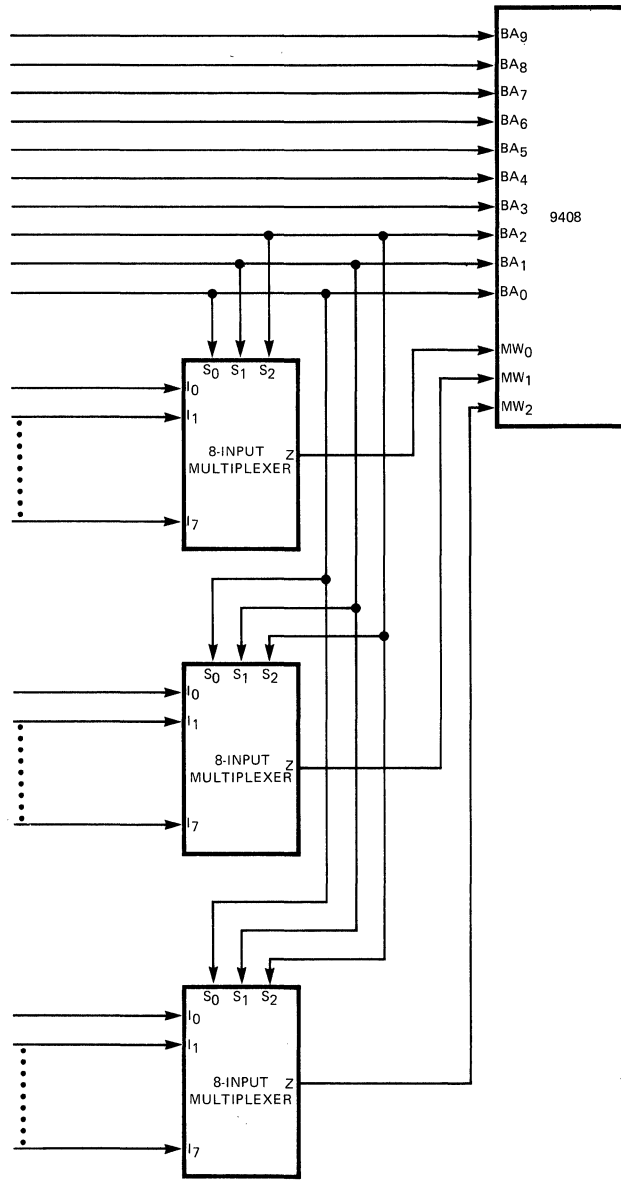


Fig. 5-6 Expanding Multiway Inputs

A Microprogram Example

The simple microprogram example, shown in *Figure 5-7* and *Table 5-1*, is an assembly of a 7-bit word from a serial data stream (SER DATA) using the associated clock (SER CLK). *Figure 5-8* illustrates the assumed timing relationship between SER DATA and SER CLK signals. Consider an 8-bit wide data path using two 9405A and two 9404 devices as shown in *Figure 5-7a*. A 6-bit instruction bus is obtained (9405A field) by appropriate connections of the 9405A instruction inputs. These six bits are controlled by an appropriate field in the microinstruction, bit 4 through bit 9 of the control store *(see Figure 5-7b)*. The 6-bit 9404 field is obtained by connecting I_1 through I_4 of 9404 devices and using I_0 of each device separately. These six bits are also controlled by an appropriate field in the microinstruction, bit 10 through bit 15 of the control store. In this illustration, the 9404 and 9405A control fields of the microinstruction are also used to provide the 10-bit branch address for the 9408. The instruction inputs for the 9408 are provided by the appropriate microinstruction field, bit 0 through bit 3 of the control store.

ADDRESS (Octal)	9408 FIELD				9405A FIELD						9404 FIELD					
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
10	FTCH				RO			LOAD			PLUS 1					
	L	H	L	L	L	L	L	L	H	H	L	H	H	H	L	H
11	BMW				X	X	2X									
	H	H	L	L			L	L	L	L	L	H	L	X	X	X
12	FTCH				RO			LOAD			SHIFT LEFT D-BUS					
	L	H	L	L	L	L	L	L	H	H	H	L	H	L	L	L
13	BMW				X	X	3X									
	H	H	L	L			L	L	L	L	L	H	H	X	X	X
14	BTL_1				X	X	16									
	H	L	H	H			L	L	L	L	L	L	H	H	H	L
15	BRV_0				X	X	11									
	L	L	H	L			L	L	L	L	L	L	H	L	L	H
16	RTS				RO			EXCLUSIVE-OR			BYTE SIGN MASK					
	L	L	L	L	L	L	L	H	H	L	L	H	L	L	H	L
20	BRV_0				X	X	11									
	L	L	H	L			L	L	L	L	L	L	H	L	L	H
21	BRV_0				X	X	12									
	L	L	H	L			L	L	L	L	L	L	H	L	H	L
30	BRV_0				X	X	14									
	L	L	H	L			L	L	L	L	L	L	H	H	L	L
31	BRV_0				X	X	13									
	L	L	H	L			L	L	L	L	L	L	H	L	H	H

X = Don't Care

Table 5-1 Control Store Listing

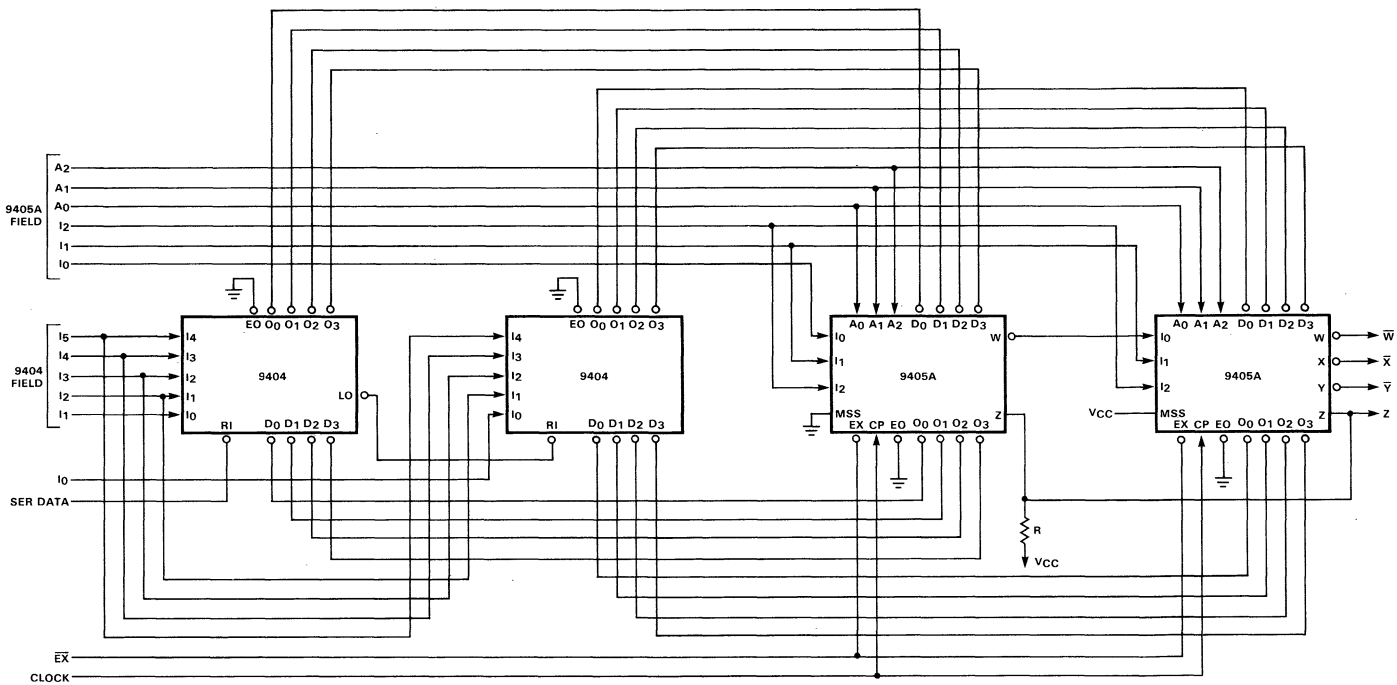


Fig. 5-7a Data Path Example

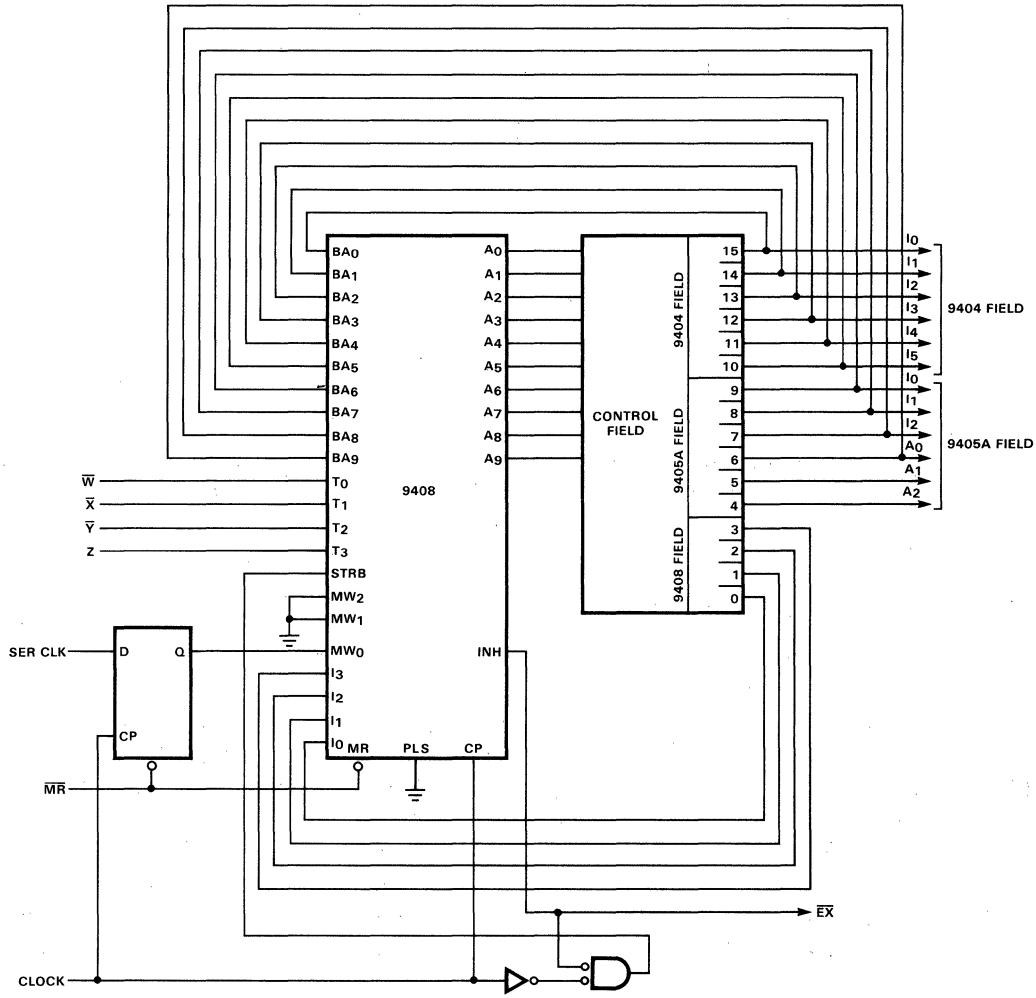


Fig. 5-7b Microprogrammed Controller

5

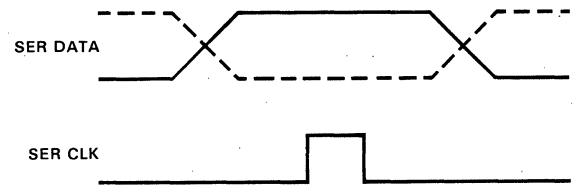


Fig. 5-8 Timing Relationship between SER DATA and SER CLK

The status outputs from the most significant 9405A, $\overline{W}$, $\overline{X}$, $\overline{Y}$ and Z, are connected to the $T_0 - T_3$ inputs of the 9408 although only the $\overline{X}$ output is used in this example. The $\overline{EX}$ inputs of both 9405As are connected to the INH output of the 9408. The Clock signal operates the 9405As and the 9408. In addition, the Clock is gated with the INH output to operate the STRB input of the 9408.

The SER CLK input is synchronized to the Clock input by using a synchronizing flip-flop with the Q output connected to the MW_0 input of the 9408 while MW_1 and MW_2 inputs are grounded. The $A_0 - A_9$ outputs of the 9408 are used to address the control store. The SER DATA is fed into the right shift input of the least significant 9404.

The flow chart in *Figure 5-9* shows the sequence of operations assuming the sequence is a subroutine starting at location $(10)_8$ in the control store. The program for implementing this flow chart is shown in *Table 5-1*. Note that register R_0, the first of the eight general purpose registers of the 9405A, is used for the serial-to-parallel conversion. Thus bit 4 through bit 6 (address bits of the 9405A field) are L L L. To indicate that a load operation into R_0 is desired, bit 7 through bit 9 (9405A instruction field) are L H H.

Bit 10 through bit 15 of the microinstruction (9404 instruction field) is L H H H L H so that bit pattern 0 0 0 0 0 0 0 1 is present at the inputs of the 9405A. This becomes apparent when the 9404 truth table in the data sheet is consulted. (The 9405A treats a LOW level data input as logic "1".) Bit 0 through bit 3 (9408 instruction field) require the 9408 to perform a Fetch for the next instruction.

Location $(11)_8$ contains a Branch Multiway, BMW, instruction to determine whether or not the synchronization flip-flop is set. Bit 6 through bit 15 of the microinstruction is specified as L L L L L H L X X X where X indicates "don't care". Thus, if the synchronization flip-flop is not set, the 9408 generates L L L L L H L L L L as the next address $(20)_8$. At location $(20)_8$, there is a Branch VIA, BRV_0, to location $(11)_8$ instruction. Thus, the microprogram loops between locations $(11)_8$ and $(20)_8$ testing for a HIGH on the SER CLK input. When the synchronization flip-flop is set, the BMW instruction at location $(11)_8$ results in $(21)_8$ as the next address instead of $(20)_8$. Location $(21)_8$ contains the instruction "BRV_0 to location $(12)_8$".

The instruction in $(12)_8$ shifts the contents of the 9405A to the left and loads the shifted value back into R_0. Because the SER DATA input is connected to the shift input of the 9404, the information present as the SER DATA input is loaded into R_0. Thus after taking the first data bit, R_0 reads 0 0 0 0 0 01 B_1,

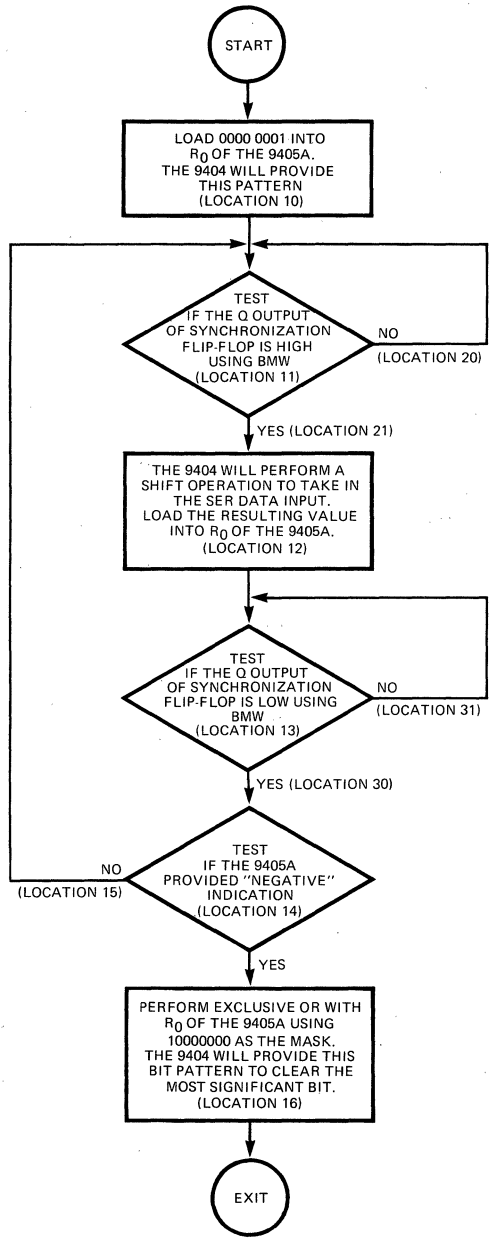


Fig. 5-9 Sequence of Operation

where B_1 is the first bit assembled. The instruction in location $(12)_8$ specifies a Fetch for the 9408, thus the INH output is LOW. This activates the $\overline{EX}$ inputs of the 9405As. Moreover, the LOW level also enables the gate; thus, the Clock activates the STRB input of the 9408 so that the 9405A status outputs can be loaded into the 9408 test register. As long as the result of an ALU operation is positive, i.e., most significant bit HIGH, the negative status ($\overline{X}$ output of the 9405A) is HIGH.

Location $(13)_8$ contains BMW with $(3X)_8$ as the next address. Thus if MW_0 input is HIGH, the next address is $(31)_8$; if MW_0 is LOW, the next address is $(30)_8$. Location $(30)_8$ contains "BRV_0 to location $(13)_8$" and $(31)_8$ contains "BRV_0 to $(14)_8$." Thus, as long as SER CLK input is HIGH, the program loops between locations $(13)_8$ and $(31)_8$. When the synchronizing flip-flop is cleared, the program goes to location $(14)_8$ due to the instruction in location $(30)_8$.

At location $(14)_8$, the "Branch Test LOW, BTL_1, to location $(16)_8$" is used to determine when the T_1 input of the 9408 is LOW. It will not be LOW until seven SER DATA bits have been shifted. Instead of branching to $(16)_8$, the program goes to location $(15)_8$, which contains "BRV_0 to location $(11)_8$". The program loops around until seven data bits have been shifted in. At this time, the 9405A has indicated a LOW on its $\overline{X}$ output and the BTL results in a branch to location $(16)_8$.

At location $(16)_8$, the 9404 provides 1 0 0 0 0 0 0 0 as a mask and an exclusive OR is performed in R_0 of the 9405A to eliminate the marker bit that was previously loaded into R_0. R_0 then contains seven data bits assembled from the SER DATA bit stream. It has been assumed that this small program is a subroutine. Therefore, by specifying RTS to the 9408 in location $(16)_8$, a return to the main program is effected.

IMPLEMENTING DATA PATHS WITH MACROLOGIC

Individual Macrologic data sheets indicate how each 4-bit slice may be expanded into arrays to handle larger word lengths; these different arrays *(Figure 5-10)* can be configured to develop the data paths. Since Macrologic elements are designed to be used in bus-organized systems, all devices are provided with 3-state data outputs and an Output Enable ($\overline{EO}$) input to control them. Therefore, the data outputs from the arrays can be bussed together to obtain the output bus *(Figure 5-11)*. With a LOW level on the appropriate $\overline{EO}$ input, an array can be made to source data on to the output bus. For example, in *Figure 5-11*, a LOW on the $\overline{EO_1}$ input selects the ALRS array as the source. The data inputs can also be bussed together to obtain the input bus.

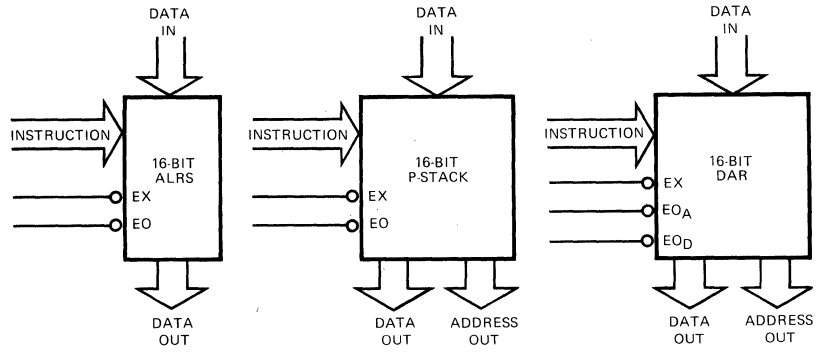


Fig. 5-10 Typical Macrologic Arrays

The instruction inputs of the arrays must be controlled by the microinstruction fields. However, what are the chances of two different Macrologic arrays performing two different operations on the same input data during the same clock cycle? This situation occurs very rarely; therefore, individual control fields are seldom needed.

The Macrologic elements are provided with individual $\overline{EX}$ inputs. A device does not respond to the clock unless its $\overline{EX}$ input is LOW. Thus, the instruction inputs can be bussed together to obtain an instruction bus *(Figure 5-12)*. The individual $\overline{EX}$ inputs are used to control the array chosen to perform the current microinstruction, i.e., the destination. Thus, in *Figure 5-12,* a 6-bit field is sufficient for the instruction inputs.

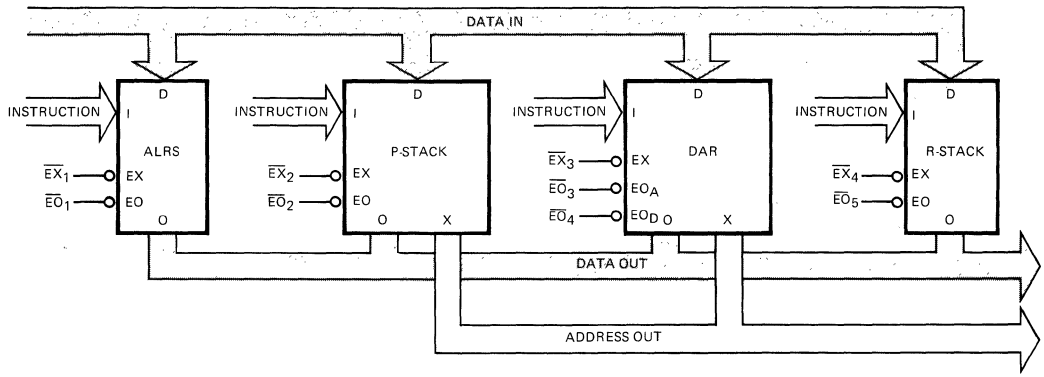


Fig. 5-11 Bussing Macrologic Arrays

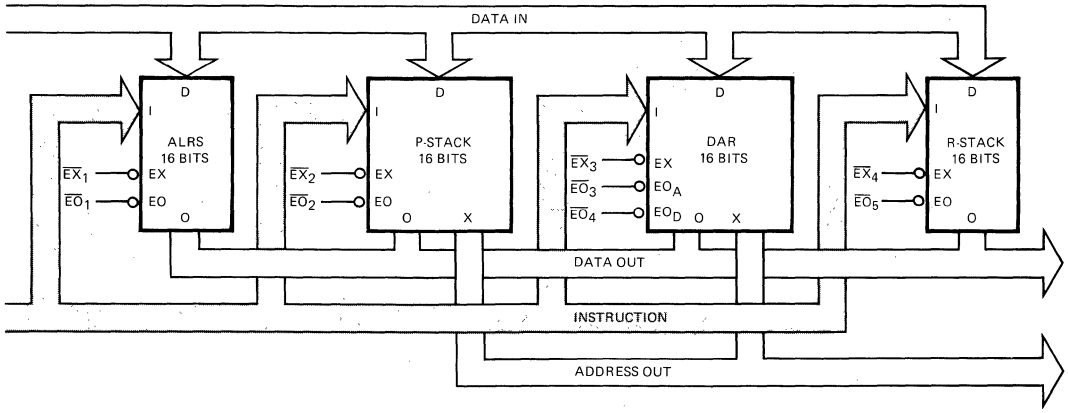


Fig. 5-12 Bussing Macrologic Instruction Inputs

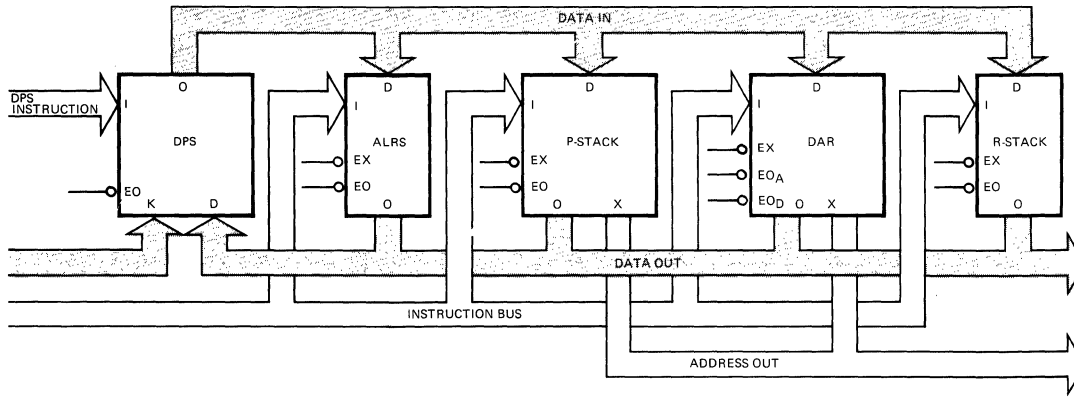


Fig. 5-13 Closed Data-Path Loop

Experience indicates that data paths in microprogrammed systems are closed loop, therefore, a means should be provided for the output bus to communicate with the input bus. The Macrologic DPS element is ideally suited for this purpose *(Figure 5-13)* since it has two identical input ports. One port can be used to close the data-path loop while the other is used to introduce data from external sources into the data paths. The DPS is a combinatorial device and hence will always operate on the data; in many cases the operation may be just to pass the input to the output. Thus it will always require an instruction input and cannot be bussed with the instruction bus.

It can be concluded that the basic steps involved in data path configuration are, first, choose arrays of desired word lengths and desired functions, then arrange them into a bus organization similar to *Figure 5-13.*

A SIMPLE PROCESSOR EXAMPLE

One of the many possible Macrologic applications is to implement emulators for existing instruction sets. These complex functional LSIs offer improved cost and performance while retaining software compatibility with the target machine. A simple 16-bit processor is a good example to demonstrate the ease of use and versatility of Macrologic.

The 16-bit fixed word-length processor, with four accumulators (AC_0 – AC_3) and 2s complement arithmetic, has a 16-word push/pop stack for subroutine nesting, as well as general use. The memory reference instruction format is shown in *Figure 5-14*. The 2-bit index field in the instruction specifies four addressing modes–base page, PC relative, AC_2 and AC_3 relative. For the base-page mode, the 8-bit displacement field of the instruction is taken as the absolute address i.e., first 256 memory locations. For the relative mode, the 8-bit displacement is treated as a signed number in 2s complement notation and added to the Program Counter (PC relative) or one of the specified accumulators (AC_2 or AC_3 relative). The result then is used as the effective address for the operand.

A data path suitable for this processor is shown in *Figure 5-15*. It consists of a 16-bit ALRS array, 16-bit P-Stack array and 16-bit DPS array. The ALRS and DPS can perform all the arithmetic logic operations needed. The P-Stack provides the required 16-level stack function. The ALRS has eight built-in accumulators but only four are needed for this processor. The P-Stack has the necessary features to implement the PC, however, if this feature is used, only 15 levels of nesting remain. This processor requires 16. Because the ALRS has four spare accumulators, one of these can be used as the PC, thus leaving three spares. Thus the PC feature of the P-Stack is not needed and therefore the address outputs are not used. The storage in the ALRS is allocated as follows: $R_0 = AC_0$, $R_1 = AC_1$, $R_2 = AC_2$, $R_3 = AC_3$, $R_4 = PC$, $R_5 = TEMP\ 1$, $R_6 = TEMP\ 2$ and $R_7 = TEMP\ 3$. An edge-triggered memory address register (MAR) on the output bus is provided. Data from the memory is introduced into the data path using one of the input ports of the DPS array. Data to the memory is obtained directly from the output bus. An edge-triggered instruction register (IR) is also provided to hold the OP code bits and index bits of the macroinstruction.

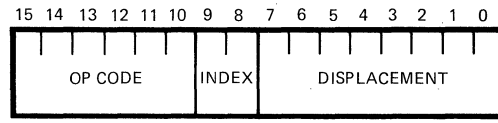


Fig. 5-14 Memory Reference Instruction Format

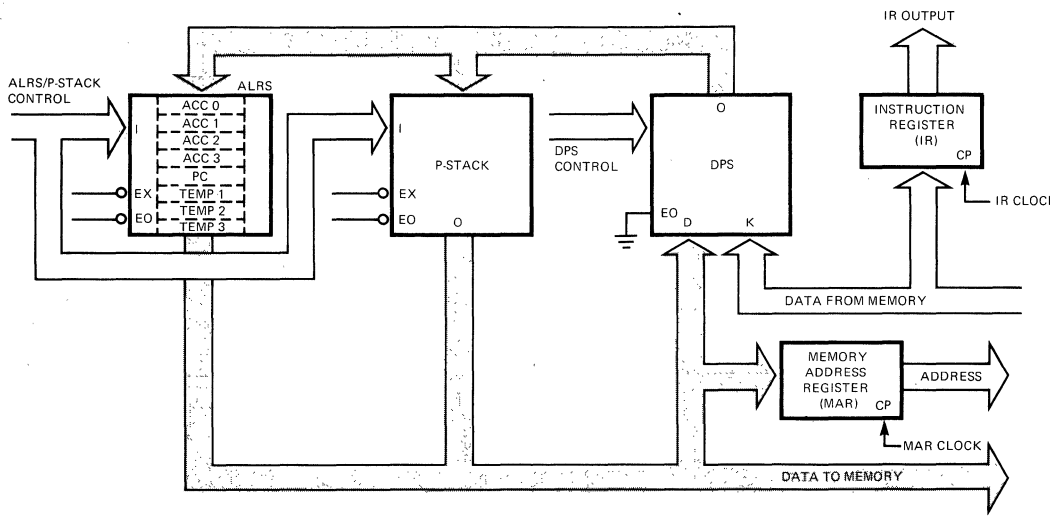


Fig. 5-15 Data Path for the Processor

Figure 5-16 illustrates the microprogram control section for the data path. This control is centered around the 9408 sequencer operating in the pipeline mode (see page 5-3). The INH output of the 9408 is used to share the control fields. Thus, the source, destination, and ALRS/P-stack control fields provide the 10-bit address for branching when needed. A 6-bit DPS control field provides the instruction inputs for the DPS array while the 4-bit SEQ field provides the instruction inputs for the 9408. Other fields lumped as miscellaneous are used to control the memory etc.

The Source and Destination fields are decoded to activate the $\overline{EO}$ and $\overline{EX}$ inputs *(see Figure 5-16)*. Note that the IR Clock and MAR Clock signals are generated by gating the system clock with the appropriate destination decoder outputs. The branch address inputs ($BA_0 - BA_9$) are obtained from a 4-way input multiplexer which, in turn, is controlled by the VIA_0 and VIA_1 outputs of the 9408. One of the inputs to this multiplexer consists of the address inputs for branching from the microinstruction register. The second port is fed by a mapper that may be a PROM or FPLA. It receives the IR outputs and translates them into a starting address in the control memory for emulation. *Figure 5-17* is a flow chart for the sequence of operations to accomplish macroinstruction fetch while *Table 5-2* lists the operations performed by various data path elements and the 9408.

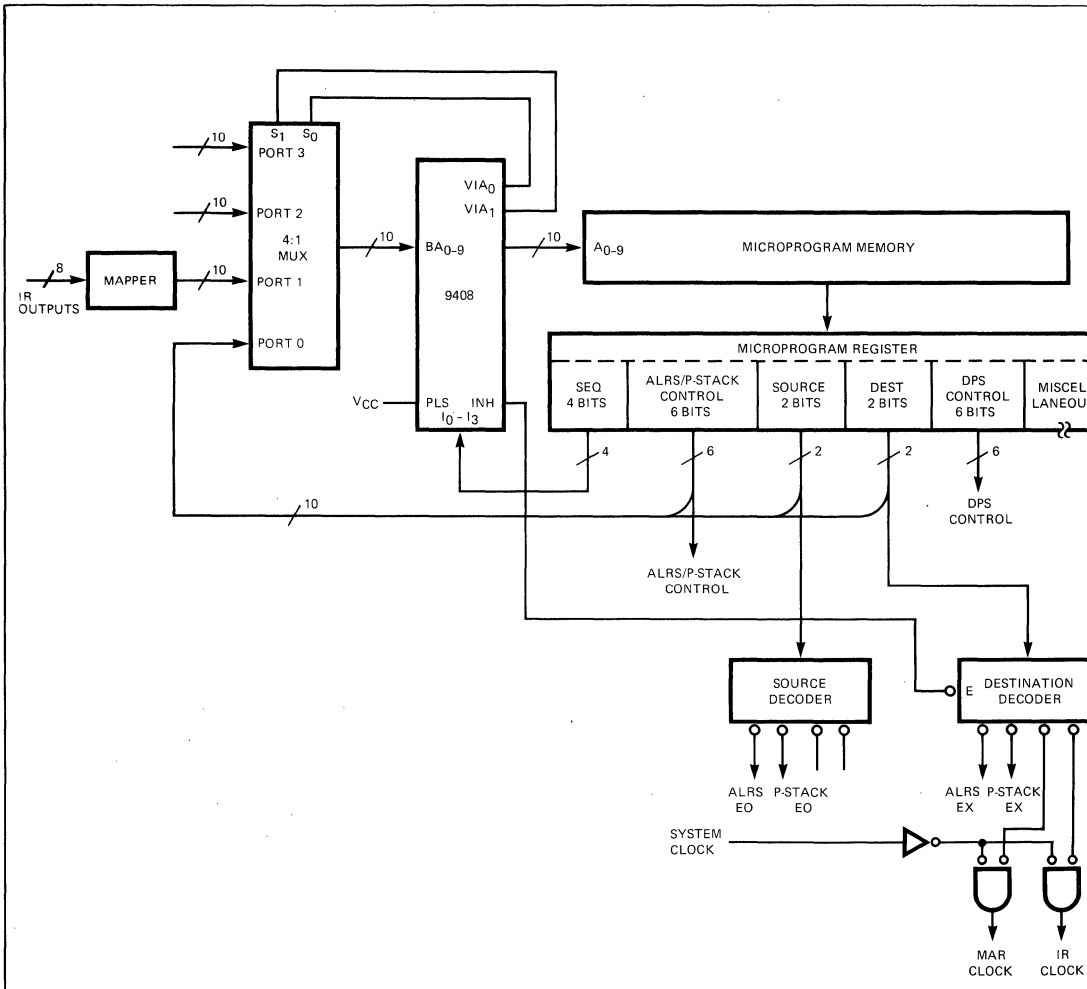


Fig. 5-16 Microprogram Control

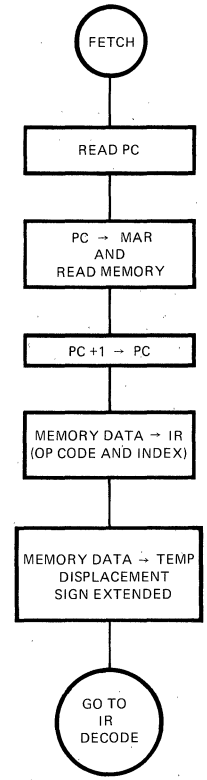


Fig. 5-17 Flow Chart for Fetch Operation

SOURCE	DESTINATION	ALRS/ P-STACK CONTROL	DPS CONTROL	SEQ	MISCELLANEOUS
DON'T CARE	ALRS	READ R_4 (PC)	DON'T CARE	FTCH	- - -
ALRS	MAR	DON'T CARE	DON'T CARE	FTCH	READ MEMORY
DON'T CARE	ALRS	ADD WITH CARRY TO R_4	ALL ZEROS	FTCH	- - -
DON'T CARE	IR	DON'T CARE	DON'T CARE	FTCH	- - -
DON'T CARE	ALRS	LOAD R_5 (TEMP 1)	K-BUS SIGN EXTEND	FTCH	- - -
DON'T CARE	DON'T CARE	DON'T CARE	DON'T CARE	BRV_1	- - -

Table 5-2 Operations for FETCH Instruction

The first operation is to read the PC. Thus, the destination field specifies the ALRS and the destination decoder drives the $\overline{EX}$ input of the ALRS LOW. The ALRS/P-stack control field specifies "read R_4". At the end of the microcycle, the contents of R_4, i.e., the PC, are in the output register of the ALRS. The SEQ field of the first microinstruction is FTCH, therefore, the 9408 generates the address of the second microinstruction.

Here, the ALRS is specified as the source and the MAR as the destination. The source decoder activates the $\overline{EO}$ input of the ALRS, the destination decoder enables the gating for the MAR Clock, and the microinstruction loads the PC into the MAR. In the miscellaneous field, a memory Read is initiated. The third microinstruction is made to increment R_4 by selecting ALRS as the destination specifying Add with Carry. The DPS outputs (ALRS inputs) are forced HIGH. This incrementation is in preparation for the next macroinstruction fetch. The result from the memory read operation, initiated during the second microinstruction, is now available on the K-bus of the DPS. The fourth microinstruction activates the IR clock so that the eight most significant bits of the memory data are loaded into the IR. Assuming the data is still on the bus, the sign extended displacement is loaded into R_5 (TEMP 1) of the ALRS in the fifth microcycle by selecting "Load R_5" as the ALRS operation and selecting the "K-bus sign extend" for the DPS. It should be recalled that the data path has a 16-bit fixed word length and the displacement must be treated as a 2s complement number. By using the sign extension capabilities of the DPS, the sign bits, i.e., most significant bits, can be aligned. At this point, the instruction is in the IR and the sign extended displacement is in TEMP 1. The sign of the least significant eight bits of the macroinstruction is extended in anticipation of a memory reference instruction. The sixth microcycle is intended to decode the IR. By specifying a BRV_1 in the SEQ field, the VIA outputs of the 9408 select the mapper output as the source for next address. The mapper is designed to provide the starting address of the routine to emulate the instruction currently residing in the IR.

The total microprogram really consists of several simple routines. These easy steps can be converted into binary patterns to be loaded into the control store. Once a data path architecture and microinstruction format has been chosen for a given system design, the microprogram can be written to realize the desired function. It can then be assembled, using the microprogram assembler, to get the binary listing that specifies the control store address and contents. Using this information, the control store can be loaded with the program and the system is ready for operation.

MACROLOGIC ASSEMBLERS

Macrologic users, designing programmed logic systems, find a need for a microprogram assembler to aid in software development. To fill that need, Fairchild offers a choice of assembler software, the microprogram assembler and DAPL, available through two different worldwide time share networks.

Microprogram Assembler

The microprogram assembler is an aid in the preparation of a microcode. The user defines his own mnemonics to represent meaningful binary bit patterns and using the symbolic language thus created, writes the program. The microprogram assembler translates the symbolic language into binary code and produces punched card, disk or tape output for each program step. The same information is also printed along with indications of errors that were present in the input statements. Access to the microprogram assembler is easily arranged from anywhere in the world.

The microprogram assembler is available at the Computer Useage Company, Data Center, Sunnyvale, California. (408-738-4300).

DAPL

DAPL is a highly modular microprogramming language for the Fairchild Macrologic series. Constructed in four concentric and compatible levels, the microprogrammer selects the DAPL feature that provides a con-

venient symbolic representation of a particular microprogram. Macros and symbolic values may be used at all DAPL levels. Level 0 essentially permits the microinstructions to be formed by sequences of symbolic names and binary, octal, decimal, and hexadecimal numbers. In Level 1, microinstructions are defined as a series of fields with each field sequentially assigned a value as in Level 0. Additionally, label tables can be incorporated for mapping ROMs and PLAs. Level 2 extends the microinstruction field definition to include symbolic names and default values. Finally, Level 3 allows the expression of microprograms in register transfer notation.

Other DAPL features include:

- Microprogram accommodation up to 8192 words by 256 bits.
- Free form input with comments arbitrarily interspersed for documentation.
- An interlist command that lists the generated microcode directly beneath the associated micro-instruction.
- A complete variable cross-reference listing.
- Extensive error detection and debugging aids.
- Optional hexadecimal or binary object format.
- A use map showing those locations actually used.

DAPL is available under a one-time license from Zeno Systems Inc., 2210 3rd St., Santa Monica Ca., (213) 396-6020 or on a timesharing basis from Remote Computing Corporation, One Wilshire, Los Angeles, Ca. 90015, (213) 629-2532.

CYCLIC CHECKS FOR ERROR DETECTION

Error detection schemes using parity checks are well known. A parity check on a character is called "vertical" parity and a check on corresponding bits of every character in a message (data block) is called "longitudinal" parity. Used together, they provide a satisfactory checking scheme; the measure of protection provided is better than using vertical or longitudinal parity alone. However, the level of redundancy to achieve this protection is relatively high. For example, if there are x bytes in a message each consisting of seven data bits and one parity bit, the ratio of number of check bits to data bits is (x+8)/7x. As x increases, the ratio reaches a limit of 1/7.

Another checking scheme exists called polynomial or cyclic coding that can be designed to perform with higher efficiencies than traditional parities. The level of protection achieved with a 16-bit cyclic check is probably satisfactory for most practical purposes; when used with a data block consisting of 7x data bits, ratio of check to data bits is only 16/7x. The ratio reaches a limit of zero as x increases. This high efficiency is inducing designers to incorporate cyclic check schemes in modern data communication and peripheral equipment such as tapes and discs. Theoretical knowledge necessary for cyclic check implementation existed for several years. However, widespread use is only in recent designs using integrated circuits. Because it is relatively new, many designers do not have the needed exposure to cyclic schemes and tend to shy away.

This discussion is intended to familiarize uninitiated readers with the algebraic concepts required to design circuits for implementing cyclic check schemes. Not only are these concepts of value to the hardware designer, but also to the diagnostic programmer who must generate the code to check the implemented logic for validity and failures.

Polynomial Notation and Manipulation

A very convenient way of expressing a bit stream (message) consisting of K bits is to think of it as a polynomial in a dummy variable x with K terms. The bits of the message are the coefficients in the

polynomial. Thus, if 100100011011 is the message, it may be written as:

$$M(x) = 1 \cdot x^{11} + 0 \cdot x^{10} + 0 \cdot x^9 + 1 \cdot x^8 + 0 \cdot x^7 + 0 \cdot x^6 + 0 \cdot x^5 + 1 \cdot x^4 + 1 \cdot x^3 + 0 \cdot x^2 + 1 \cdot x^1 + 1 \cdot x^0$$

or

$$M(x) = x^{11}+x^8+x^4+x^3+x+1$$

To compute the cyclic check on a message, another polynomial P(x) called a generating polynomial is chosen. The degree "r" of the P(x) is such that it is greater than zero but less than the degree of M(x). Moreover, P(x) has a non-zero coefficient in the x^0 term. It is clear then that for a given message length, more than one generating polynomial of desired length can be specified. Fortunately, several accepted standard generating polynomials exist; most common are CRC-16 and CRC-12 which were originally proposed for the IBM binary synchronous communications.

CRC-16 is a 16-bit check resulting from a generating polynomial $x^{16}+x^{15}+x^2+1$ and CRC-12 is a 12-bit check resulting from $x^{12}+x^{11}+x^3+x^2+x+1$. Theory suggests that use of CRC-16 and CRC-12 will catch all messages with an odd number of errors, all with a single burst of less than 16 or 12 bits respectively and most of the few messages with larger bursts.

Cyclic check computation involves manipulating M(x) and P(x) using laws of ordinary algebra, except that modulo 2 arithmetic is used. Because modulo arithmetic yields the same result for addition and subtraction, it is necessary only to consider three operations involving polynomials—addition, multiplication and division.

Addition of two polynomials $x^6+x^5+x^2+1$ and $x^5+x^4+x^3+x^2$ yields $x^6+x^4+x^3+1$ as shown below:

$x^6+x^5+0+0+x^2+0+1$	=	1100101
$x^5+x^4+x^3+x^2+0+0$	=	111100
$x^6+0+x^4+x^3+0+0+1$		1011001

Multiplication of two polynomials $x^7+x^6+x^5+x^2+1$ and $x+1$ results in $x^8+x^5+x^3+x^2+x+1$

$(x^7+x^6+x^5+x^2+1)(x+1)$	=	(11100101) x 11
$x^8+x^7+x^6+0+0+x^3+0+x+0$	=	111001010
$x^7+x^6+x^5+0+0+x^2+0+1$	=	011100101
$x^8+0+0+x^5+0+x^3+x^2+x+1$		100101111

It is interesting to note that multiplication of a polynomial by x^m results in a shifted bit pattern which is identical to the original except for zeros in the lower m positions. For example:

$x^5(x^{11}+x^{10}+x^8+x^4+x^3+x+1) = x^{16}+x^{15}+x^{13}+x^9+x^8+x^6+x^5$ where $x^{11}+x^{10}+x^8+x^4+x^3+x+1$ = 110100011011 and

$$x^{16}+x^{15}+x^{13}+x^9+x^8+x^6+x^5 = 11010001101100000$$

Dividing $x^{13}+x^{11}+x^{10}+x^7+x^4+x^3+x+1$ by $x^6+x^5+x^4+x^3+1$ results in a quotient of $(x^7+x^6+x^5+x^2+x+1)$ and a remainder of (x^4+x^2) as shown below. Practically, it might be easier to divide by longhand if the bit pattern is used rather than the polynomial.

$x^{13}+x^{11}+x^{10}+x^7+x^4+x^3+x+1 = 10110010011011$ $x^6+x^5+x^4+x^3+1 = 1111001$

```
          11100111
1111001 ) 10110010011011
          1111001
           1000000
           1111001
            1110010
            1111001
              1011110
              1111001
               1001111
               1111001
                1101101
                1111001
                  10100
```

Thus, Q(x) = 11100111 = $x^7+x^6+x^5+x^2+x+1$ R(x) = 10100 = x^4+x^2

Cyclic Check – Computing Procedure

To compute a check on M(x), a generating polynomial P(x) is chosen as mentioned earlier. Steps involved in check computation are as follows:

a) Message polynomial M(x) is multiplied by x^r where r is the degree of P(x). As noted earlier, this process yields zeros in the lower r positions of M(x). These vacated positions are in preparation for the r check bits that will be appended to the message. Also note that this process does not alter the message bit pattern.

b) The result obtained from step (a) is divided by P(x). This gives a quotient Q(x) and a remainder R(x). The remainder will be r bits or less.

c) The quotient is discarded and the remainder is added to the result of step (a). The remainder is the check. The message with this remainder at the tail end constitutes the transmitted polynomial T(x).

The following example illustrates the computation procedure. Let M(x) = $x^{11}+x^{10}+x^8+x^4+x^3+x+1$ = 110100011011 and P(x) = $x^5+x^4+x^2+1$ = 110101. Thus, r = 5 and $x^rM(x) = x^{16}+x^{15}+x^{13}+x^9+x^8+x^6+x^5$ = 11010001101100000

$$\frac{x^r\,M(x)}{P(x)} = \frac{11010001101100000}{110101}$$

Carrying this division, Q(x) = 100001100111 and R(x) = 1011.

Transmitted message T(x) is obtained by adding R(x) to $x^rM(x)$

x^r M(x) = 11010001101100000

R(x) = 01011

T(x) 11010001101101011

Data Check

Note that transmission occurs from left to right; data thus is unmodified and check bits follow at the end.

Data Validation at the Receiver

The transmitted polynomial arrives at the receiver modified or unmodified depending on whether transmission has encountered errors or not. Clearly, one of the ways by which the receiver can ensure data validity is to recompute the check bits on the message using the same generator polynomial and compare them with the received check bits. If they agree, it is assumed that received data is good.

Instead, the receiver can divide the complete received polynomial by the same generator polynomial P(x). If there are no errors, it can be shown that this divison results in zero remainder. This property can be easily verified by long division of T(x) = 1101000110110101 by P(x) = 110101. If the division results in a non-zero remainder, it can be assumed that T(x) has been modified by errors. This may be verified by introducing error and performing the division. The process of dropping and picking bits can be viewed as adding another polynomial E(x) (error polynomial) to T(x).

For example, if T'(x) = 1001000110110101 1 is received, instead of T(x), T'(x) = T(x)⊕E(x) can be written where E(x) = 0101000110110101 1. It follows then that if T'(x) is exactly divisible by P(x), the receiver is blind and indicates no errors. This only happens if E(x) is exactly divisible by P(x). Knowing the characteristics of the transmission medium, it is advisable to choose such a generating polynomial that the probability of error patterns occurring that are divisible by P(x) is extremely low. The process of not detecting such errors is somewhat analogous to the erroneous validity indication in normal parity schemes where multiple bit errors may cancel each others contribution to the check.

Basic Polynomial Divider

Consider long hand division of the polynomial $x^{16}+x^{15}+x^{13}+x^{9}+x^{8}+x^{6}+x^{5}$, *i.e.*, 1101000110110000 0, by another polynomial $x^{5}+x^{4}+x^{2}+1$, *i.e.*, 110101.

```
                 100001100111
          ┌──────────────────
110101    ) 1101000110110000 0
            110101
            ------
                101101
                110101
                ------
                 110001
                 110101
                 ------
                    100000
                    110101
                    ------
                     101010
                     110101
                     ------
                      111110
                      110101
                      ------
                        1011
```

From this example, long hand division procedure can be summarized; align the most significant bits of the partial remainder and divisor borrowing from the dividend as required. This implies aligning the divisor and dividend to start the division process. Then, subtract the divisor from the partial product using modulo 2 arithmetic. When all bits in the dividend are processed, the result is the remainder.

Subtraction in modulo 2 of two bits is the same as performing an Exclusive-OR operation and alignment of bits suggests a shift operation. Consider two registers as shown in *Figure 5-18.*

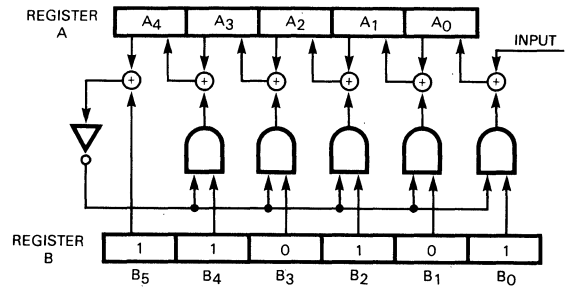


Fig. 5-18 Conceptual Polynomial Divider

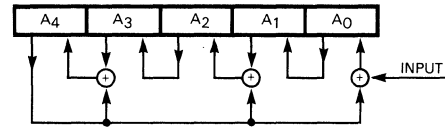


Fig. 5-19 Polynomial Divider for $x^5+x^6+x^2+1$

Assume that register A is initially clear and register B contains 110101, which is the divisor bit pattern. Also imagine that the dividend serially enters the network as input (most significant bit first), in response to a clock signal that operates register A. As long as A_4 is cleared and B_5 is set, the AND gates are inhibited. This establishes a connection between A_4 input and A_3 output, A_3 input and A_2 output etc. Thus, register A serves as a "shift left" register. When clocked with the dividend as serial input, the most significant bit eventually appears in A_4. At this point, A_4 and B_4 are both set, *i.e.*, the most significant bits of divisor and dividend are aligned. This alignment enables the AND gates. However, this has no effect on the Exclusive-OR gates with inputs derived from Zero bit positions of register B. The "shift left" nature of register A at bit locations fed by these Exclusive-OR gates is preserved. Thus in *Figure 5-18*, the A_1 input comes from A_0 and A_3 input from A_2. On the other hand, the remaining bit positions receive the result of modulo 2 subtraction between appropriate bits. In summary, when register A is clocked after bit alignment, the partial remainder is loaded into it. If clocking is continued until all dividend bits are processed, the content of register A is the required remainder. *Table 5-3* illustrates the register contents through this process; it is instructive to compare it with the long division.

Closer examination of *Figure 5-18* suggests that it can be greatly simplified. *Figure 5-19* shows a functionally identical scheme similar to that used for cyclic checking purposes.

Input	Register				
	A_4	A_3	A_2	A_1	A_0
1	0	0	0	0	1
1	0	0	0	1	1
0	0	0	1	1	0
1	0	1	1	0	1
0	1	1	0	1	0
0	0	0	0	0	1
0	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	1	1
0	1	0	1	1	0
1	1	1	0	0	0
1	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	1	1	1
0	0	1	0	1	1

Table 5-3 Bit Patterns Through Division Process

Discussion on basic polynomial division circuits can now be concluded with these observations—the division algorithm can be implemented by suitable interconnection of shift registers and Exclusive-OR gates. The total number of register positions equals the degree of the divisor polynomial. The total number of Exclusive-OR gates is equal to one less than the number of non-zero terms in the divisor.

Polynomial Divider for Cyclic Checks

But for one drawback, the polynomial divider could be used as a cyclic check generator. Imagine that the dividend polynomial $x^{16}+x^{15}+x^{13}+x^9+x^8+x^6+x^5$ is the result of multiplying $(x^{11}+x^{10}+x^8+x^4+x^3+x+1)$ by x^5, and the divisor $x^5+x^4+x^2+1$ is the generating polynomial. From the cyclic check coding scheme, remember that $x^{11}+x^{10}+x^8+x^4+x^3+x+1$ is the actual data stream. The divider circuit discussed so far does not provide the remainder until the trailing zeros have been processed. Thus, if the remainder is to be appended as a check to the data stream, there is a delay before it is available for transmission. In almost all applications, such a gap between data and check bits is undesirable. This deficiency could easily be rectified if a circuit were possible which could multiply two polynomials while dividing by a third simultaneously.

Polynomial multiplication circuits can be derived using analogous arguments that result in the division circuit. For example, the arrangement shown in *Figure 5-20* multiplies an incoming polynomial by $x^6+x^5+x^4+x^3+1$. Fortunately, for cyclic check applications, multiplication by a single term of the form x^r,

where 'r' is the degree of the generator polynomial, is sufficient. To implement a "multiply by x^5" circuit, only a 5-bit shift register and one Exclusive-OR gate are needed as shown in *Figure 5-21.*

It is possible to combine the multiplier shown in *Figure 5-21* and the divider in *Figure 5-18* to implement a simultaneous multiply by x^5 and divide by $x^5+x^4+x^2+1$ circuit as shown in *Figure 5-22.* As before, *Figure 5-22* may be simplified to arrive at *Figure 5-23* which can be used as a cyclic check generator for the generating polynomial $P(x) = x^5+x^4+x^2+1$. *Table 5-4* lists the register content as each bit of the dividend (message polynomial) is processed.

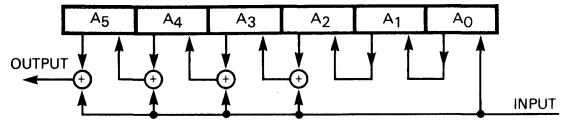


Fig. 5-20 Circuit for Multiplying by $(x^6+x^5+x^4+x^3+1)$

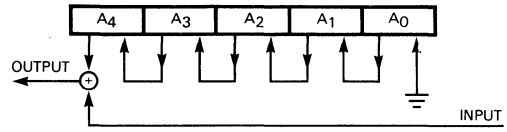


Fig. 5-21 Circuit for Multiplying by x^5

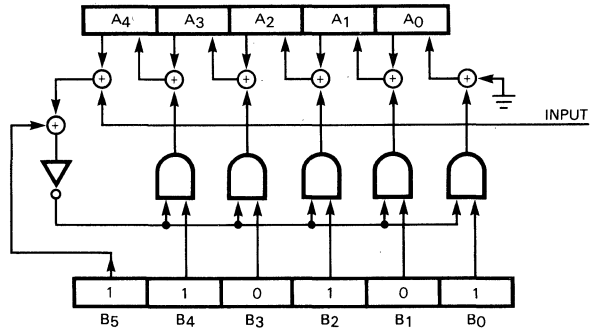


Fig. 5-22 Conceptual Cyclic Check Generator

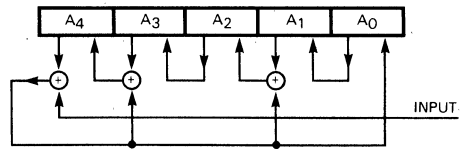


Fig. 5-23 Basic Cyclic Check Circuit for $P(x) = x^5+x^4+x^2+1$

Input	Register				
	A_4	A_3	A_2	A_1	A_0
1	1	0	1	0	1
1	0	1	0	1	0
0	1	0	1	0	0
1	0	1	0	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	1	1	1
1	1	1	1	1	0
1	1	1	1	0	0
0	0	1	1	0	1
1	0	1	1	1	1
1	0	1	0	1	1

Table 5-4 Bit Pattern Through the Check Circuit

From *Table 5-4,* it is clear that the remainder is available as soon as the last data bit is processed. Also note that the quotient bit pattern appears in A_0. If it is desired to transmit the remainder from the register of *Figure 5-23* in a serial fashion, the connections must be established to make the register a straight shift from right to left by disabling the feedback through the Exclusive-OR gates.

Reverse Polynomials

Cyclic checks are often used in magnetic tape systems. Many of these have capabilities to read data in both forward and reverse directions. One of the reasons for this capability is to combat the overhead required to position the tape in front of the data block for a re-read operation in the event of an error. When "data followed by check bits" format is used to write on the tape, the check character is encountered first while reading in the opposite direction and the bit order for the whole block is reversed. Clearly, if the same check circuitry is used for error detection in both directions, erroneous indications are inevitable when reading in the opposite direction. This situation can be avoided by utilizing a reverse polynomial for checking in the opposite direction. The reverse polynomial is obtained by writing a polynomial bit pattern backwards. For example, the bit pattern for CRC-16 (forward) is 11000000000000101, *i.e.*, $x^{16}+x^{15}+x^2+1$. The reverse polynomial for this pattern is 10100000000000011 or $x^{16}+x^{14}+x+1$.

PROGRAMMABLE BIT-RATE GENERATOR

The industry standard Universal Asynchronous Receiver/Transmitter (UART), an MOS/LSI subsystem, has had a considerable impact on data-communication system design. Not only has the UART dramatically reduced chip counts and increased reliability, etc., but it has also provided an incentive to integrate the remaining support functions.

One such subsystem is the 4702 programmable bit-rate generator, designed to provide the necessary clocking signals to operate asynchronous transmitter and receiver circuits. Several standardized signaling rates are used for start-stop communication depending on the transmission medium and other system requirements. The equipment must be capable of generating all the necessary frequencies and provide a way to select the desired one. In the past, this required several SSI/MSI circuits. Now, the 4702 can perform the task more easily and economically.

The 4702 provides any one of the 13 common bit rates on a selectable basis using an on-board oscillator and an external crystal; it also is expandable for multichannel applications. In its most general form, multichannel clocking requires that any of the possible frequencies must be available on any channel. Expansion up to eight channels is accomplished without device duplication. In multiple-device systems, there is no need to use a crystal with every device. *Figure 5-24* shows the block diagram of the 4702 which consists of the following major parts:

- Oscillator and associated gating
- Scan counter
- Count chains
- Initialization circuit
- Multiplexer and output storage

Oscillator and Associated Gating

The oscillator circuit together with an external crystal generates the master timing. A 2.4576 MHz crystal provides 16 times the frequency of the baud values marked; for example, 9600 baud corresponds to 153.6 kHz. If the External Clock Enable ($\overline{E}_{CP}$) is HIGH, the oscillator output signal drives the count chain. On the other hand, if it is LOW, the External Clock (CP) signal is enabled and is then the timing source. The External Clock input also participates in the device initialization scheme. The master timing signal, either from the external source or the local oscillator, is available on the Clock Output pin (CO). This signal can be used to drive other 4702s in a multiple device system, thus eliminating the need to provide more than one crystal.

Scan Counter

The master timing drives a 3-bit binary scan counter which, in turn, drives the remaining counter chains on the chip. The scan counter allows expansion to eight channels as described later. The prescaling feature of

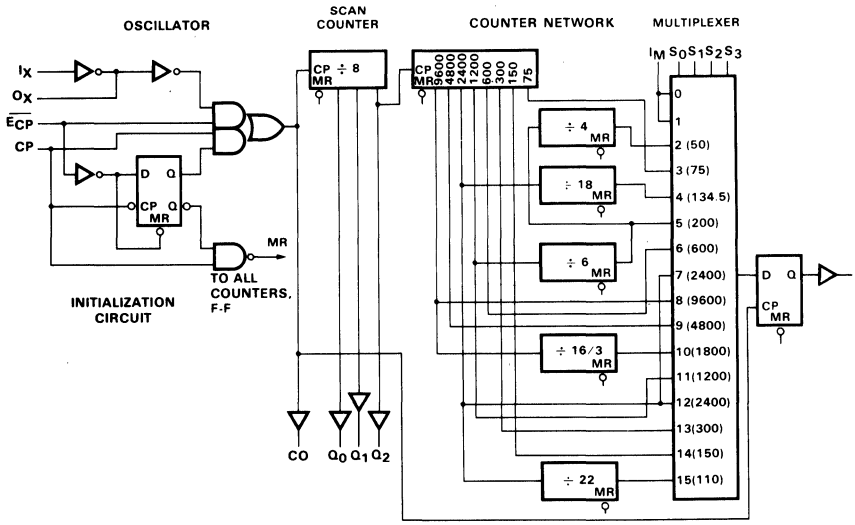


Fig. 5-24 4702 Block Diagram

this counter provides another benefit, *i.e.*, it moves the input frequency to 2.4576 MHz which is ideal for low-cost crystals. If it were not for the scan counter, the 4702 would require a more expensive crystal of about 300 kHz.

Count Chains

The scan counter output drives an 8-bit binary counter which provides the frequencies corresponding to 9600, 4800, 2400, 1200, 600, 300, 150 and 75 baud. The 1800-baud signal is generated by dividing 9600 by 16/3. The 110 and 134.5 baud signals are approximated by dividing 2400 by 22 and 18 respectively. Dividing 1200 by 6 gives the 200 baud signal, while 50 baud is generated by dividing 200 baud by 4. All division factors except 16/3 are even; thus, all outputs except 1800 baud have a 50% duty cycle.

The actual division by 16/3 is achieved by using a sequence of integers 5 and 6 such that cumulative error after every three cycles is zero. This scheme, in conjunction with the divide by 16 performed in the UART, achieves good timing accuracy demanded by high speed communication equipment. Calculations indicate that the maximum distortion introduced does not exceed 0.78% regardless of the number of elements in a character.

Initialization Circuit

This circuit generates a Master Reset signal to initialize the flip-flops on the 4702 to a known state. If the External Clock Enable ($\overline{E}_{CP}$) is LOW, the local oscillator output is inhibited and timing is derived from the External Clock (CP). The first positive half cycle of the External Clock is used to generate the Master Reset and all succeeding clock signals are used for timing. This initialization scheme allows software-controlled diagnosis for fault isolation.

Multiplexer and Output Storage

All the desired outputs from the count chains are fed as data inputs to a multiplexer. The select inputs for this multiplexer are brought out as Rate Select input (S_0-S_3). *Table 5-5* shows the correspondence between this code and the resulting frequency. The multiplexer output is fed as data input to a resynchronizing flip-flop that is clocked by the leading edge of the master timing.

If only single-channel applications of the 4702 were considered, the output flip-flop would be unnecessary. In multichannel applications, however, the Rate Select inputs change as a function of the Scan Counter outputs ($Q_0 - Q_2$). The resynchronizing flip-flop assures a fixed timing relationship between $Q_0 - Q_2$ and the Bit Rate output (Z).

Three important features should be noted from *Table 5-5.* First, two of the select codes specify Multiplexed Input (I_M) signal as the data source to the multiplexer. The user can feed a signal into this input, however, the primary intent was to feed a static logic level to achieve a "zero baud" situation. Secondly, the codes corresponding to 110, 150, 300, 1200 and 2400 baud each have a maximum of only one LOW level. These are the most commonly used rates in contemporary data terminals. Thus the rate select mechanism on these terminals need only be a single-pole 5-position switch with the common terminal grounded. Thirdly, 2400 baud is selected by two different codes so that the whole spectrum of modern communication rates will have a HIGH code in the most significant bit position.

Typical Applications

In those applications where the Rate Select inputs are static levels, operation of the 4702 is rather straightforward. The multiplexer connects the specified counter output to the data input of the output flip-flop. Because the flip-flop is clocked by the master timing, its output reflects the selected frequency.

Single-Channel Bit-Rate Generator

Figure 5-25 shows the simplest of all 4702 applications. This circuit provides one of five possible bit rates as determined by the setting of the 5-position switch. The generated frequencies correspond to 110, 150, 300, 1200 and 2400 baud depending on the switch setting. For many low cost terminal applications, these five selectable bit rates are adequate. The 4702 is not only intended for single-channel but also for multi-channel operation, as illustrated in the following applications.

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MULTIPLEXED INPUT (I_M)
L	L	L	H	MULTIPLEXED INPUT (I_M)
L	L	H	L	50 BAUD
L	L	H	H	75 BAUD
L	H	L	L	134.5 BAUD
L	H	L	H	200 BAUD
L	H	H	L	600 BAUD
L	H	H	H	2400 BAUD
H	L	L	L	9600 BAUD
H	L	L	H	4800 BAUD
H	L	H	L	1800 BAUD
H	L	H	H	1200 BAUD
H	H	L	L	2400 BAUD
H	H	L	H	300 BAUD
H	H	H	L	150 BAUD
H	H	H	H	110 BAUD

Table 5-5 Truth Table for Rate Select Inputs

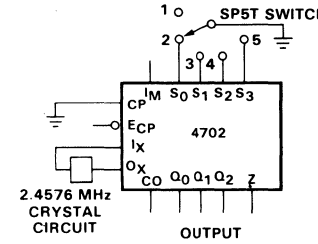


Fig. 5-25 Switch Selectable Bit-Rate Generator Configuration Providing 5 Bit Rates

Multichannel Bit-Rate Generation

Figure 5-26 illustrates a fully programmable 8-channel bit-rate generator system. Two 4 x 4 register file devices (9LS170) can be loaded with information (rate select codes from *Table 5-5*) relating to the desired frequency on a per-channel basis. For clarity, circuits for writing into the files are not shown.

The least significant Scan Counter outputs (Q_0, Q_1) control the Read Address of the 9LS170s while the most significant output (Q_2) controls the Read Enable (RE) inputs. Thus, as the counter advances, file locations are read out sequentially. The Scan Counter outputs are also the Address inputs for the 93L34 addressable latch. The Bit Rate output (Z) of the 4702 is the Data input to the 93L34 while the Clock Output is the Enable input.

To understand the operation, consider the instant when the Scan Counter outputs become Zero ($Q_0 - Q_2$ = LOW). The same clock that incremented this counter to Zero also

clocked the counter output, corresponding to the selected frequency for channel 7 into the output flip-flop, and

disabled the 93L34 latch via the Clock Output (CO), thus preventing any change in the latch outputs while the Scan Counter outputs and the Bit Rate output (Z) are changing.

During the second half of the clock cycle, when the Clock Output (CO) is LOW, the counter output representing the selected frequency for channel 7 is loaded into the 93L34 latch and is locked up on the Q_0 output.

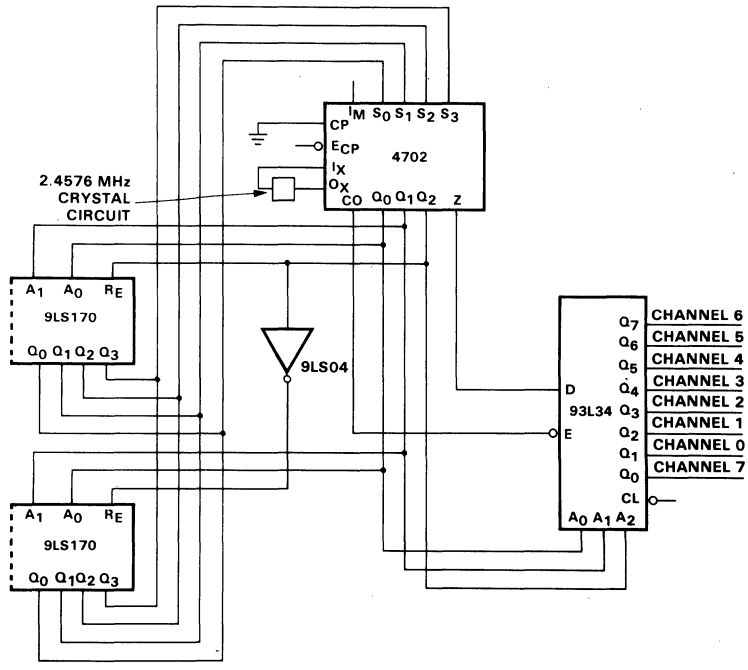


Fig. 5-26 A Fully Programmable 8-Channel Bit-Rate Generator System

The Scan Counter outputs ($Q_0 - Q_2$), which represent the selected channel, are used to interrogate the register file to determine the assigned bit rate for channel 0. The stored code for channel 0 is routed to the Rate Select inputs ($S_0 - S_3$) to select the appropriate internal frequency, so that during the next LOW-to-HIGH clock transition, the state of this internal signal is clocked into the output flip-flop. Thus, each channel is sequentially interrogated and the 93L34 latch is updated at least once during each half cycle of the highest output frequency (9600 baud).

By connecting the Scan Counter output Q_2 to the Multiplexed input (I_M) a similar technique can be used to implement a system with a maximum output frequency of 19,200 baud, however, the number of channels must be limited to four. This ensures that the output will be interrogated and updated at least once during each half cycle of the highest output frequency (19,200 baud).

Jumper Programmable 8-Channel Bit-Rate Generator

In systems where channel-speed assignments remain relatively fixed, software-controlled channel assignment is not necessary or practical. It may be simpler to program with "jumpers" at appropriate places in the system. See *Figure 5-27.*

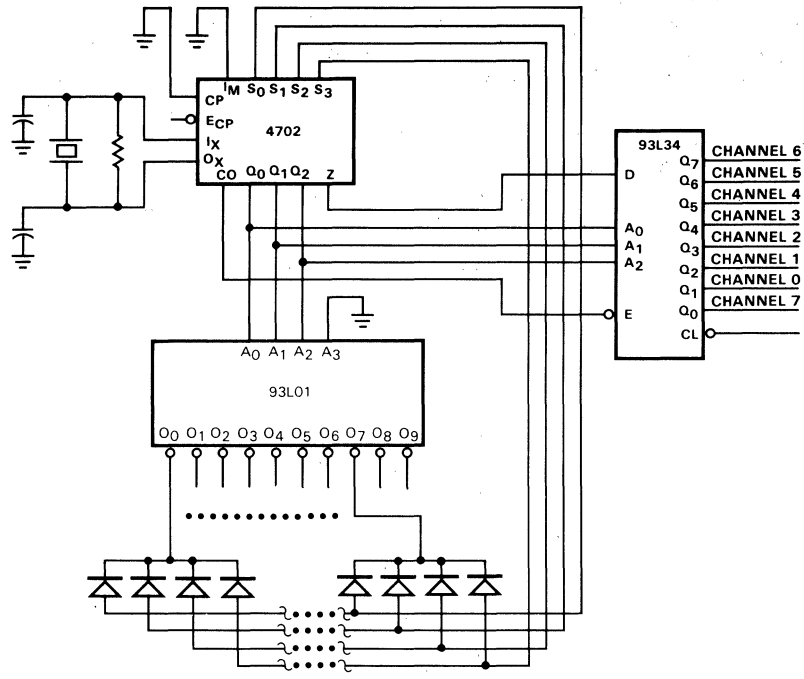


Fig. 5-27 Jumper Programmable 8-Channel Bit-Rate Generator

In the jumper programmable 8-channel bit-rate generator, the scan counter outputs ($Q_0 - Q_2$) are fed as Address inputs to a 93L01 decoder and a 93L34 addressable latch. The decoder outputs drive the diode clusters which contain four diodes for each channel. All four diode cathodes in a cluster are connected together to a decoder output; the anodes of corresponding diodes in every cluster are connected together to the appropriate Rate Select inputs of the 4702. Presence of a diode results in a LOW on the particular 4702 input; when a diode is absent, a HIGH results. As the scan counter advances, the decoder outputs activate the desired bit-rate code for that channel. The 93L34 synchronously demultiplexes the 4702 output (Z) and reconstructs the specified bit rates at its output.

Clock Expansion

The basic 4702 can be expanded to a maximum of eight channels. In applications where more than eight channels are needed, the 4702 must be duplicated. The device is designed with a clock-expansion feature; therefore only one crystal is required to operate all the channels.

The most economical expansion scheme provides one 4702 with a crystal and all other devices derive their timing from this master. The device wiring is such that the External Clock Enable input and I_X input of all but the master device feeds into the External Clock input of all the other devices. The Clock output of each device is connected to its associated 93L34 Enable input as before. An alternative scheme is shown in *Figure 5-28.*

The advantage of this scheme is that it can be conveniently used to implement the software external clock feature mentioned previously. Imagine that the External Clock Enable ($\overline{E}_{CP}$) inputs of all the 4702s in the system are controlled by the output of a flip-flop (mode) and the External Clock inputs (CP) of all the devices are tied together and software driven, possibly by operating another flip-flop. During normal operation, the mode control is HIGH, thus selecting the crystal oscillator for timing. Also, the external Clock input of each device is held LOW. When the External Clock Enable goes LOW, in preparation for the diagnostic mode, all devices receive their timing from the External Clock input. When this input goes HIGH for the first time, all devices generate an internal Master Reset signal clearing their counter chains. The next HIGH-to-LOW transition sets the internal control flip-flop and thus terminates the Reset; all counters are free to start counting in response to the External Clock signal.

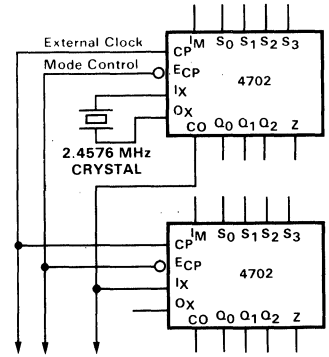


Fig. 5-28 Tandem Clock Expansion Scheme

USING THE 9403 AND 4703 FIFOs

The First-In First-Out (FIFO) memory is a read/write memory which automatically stacks the words in the same order as they were entered and makes them available at the output in the same sequence, thus its name first-in first-out. In the past, MOS technology has been the dominant manufacturing process for FIFOs. Now, however, there are two new members of the Macrologic family that utilize advanced Schottky TTL and Isoplanar CMOS technologies, the 9403 and the 4703 respectively. These two FIFOs are functionally identical and offer several unique features other than those directly attributable to the manufacturing techniques.

Description

The 9403/4703 FIFO is a 16 x 4 parallel/serial memory consisting of the following *(Figure 5-29).*

- An input register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
- A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
- An output register with parallel and serial data outputs, control inputs and outputs for output handshaking and expansion.

Parallel data is entered into the input register by using D_0 through D_3 as data inputs and Parallel Load (PL) as the strobe. A HIGH at the PL input operates the direct set and clear inputs of the input-register flip-flops. The quiescent state of the PL input is LOW.

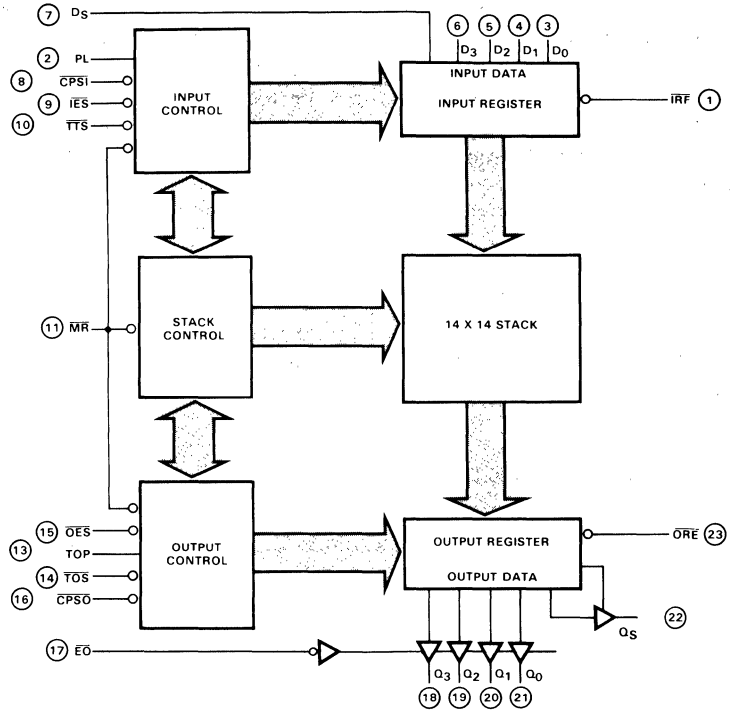
To enter data serially, the D_S is used as the data input and CPSI as the clock. The input register responds to the HIGH-to-LOW clock transition and the quiescent state of the CPSI input is LOW. For the CPSI to effect shifting, the Input Expand Serial (IES) input must be LOW.

Whenever the input register receives four data bits whether by serial or parallel entry, the status output signal, Input Register Full (IRF), goes LOW. If the Transfer to Stack (TTS) input is activated with a LOW pulse, data from the input register is transferred into the first stack location (provided it is empty). As soon as data is transferred, the control logic attempts to initialize the input register so that it can accept another word; however, the initialization is postponed until the PL input is LOW. The device is designed so that the IRF output can be connected to the TTS input. Thus, when a data word is received by the input register, it automatically enters the stack and falls through toward the output, pausing only as needed for an "empty" location.

Normally, the Output Register Empty (ORE) is LOW, indicating that the output register does not contain valid data. As soon as a data word arrives in the register, the ORE output goes HIGH, indicating the presence of valid data. If the Output Enable (EO) input is LOW, the 3-state buffers are enabled and data is available on the O_0 through O_3 outputs.

Data can be extracted either serially or in parallel. The Q_S is used for serial data output and CPSO for the clock input. The Q_S output is also available through a 3-state buffer; however its enabling is controlled internally. Output register shifting occurs on the HIGH-to-LOW transition of the CPSO whose quiescent state is LOW. As soon as the last data bit is shifted out, the ORE output goes LOW, indicating that the output register is empty.

The quiescent state of the TOS input is LOW. A HIGH-to-LOW transition on this input causes new data to be loaded from the stack into the output register (provided data is available). The ORE output can be connected to the TOS input so that as soon as the last bit is shifted out, new data is automatically demanded.



V_{DD} = Pin 24
V_{SS} = Pin 12

PIN NAMES

$D_0 - D_3$	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
$Q_0 - Q_3$	Parallel Data Outputs
Q_S	Serial Data Output

Fig. 5-29 9403/4703 Block Diagram

The quiescent state of the TOP input is HIGH and a LOW-to-HIGH transition causes new data to be loaded into the output register. Moreover, a HIGH level on the TOP input causes the ORE to go LOW. The TOP input can be connected to the EO input so that the output data can be enabled when EO is LOW. When the output is disabled, new data is automatically demanded. It should be noted that the TOS input does not affect the ORE output.

The FIFO is initialized by a LOW signal on the Master Reset (MR). This causes the status outputs, IRF and ORE, to assume an empty state; *i.e.*, IRF is then HIGH and ORE LOW. It is important to remember that the MR does not clear all the data flip-flops; it only initializes the control. Specifically, the $O_0 \ldots O_3$ outputs are not affected by the Master Reset.

Expansion

The 9403/4703 can be vertically expanded to store more words or horizontally expanded to store longer words (in multiples of four bits) without external logic. Also, the expansion scheme fully preserves the parallel/serial data features. To illustrate the expansion connections, a FIFO array consisting of eight devices is shown in *Figure 5-30.* If there are m devices in a row and n rows, the array provides (15n + 1) words of storage with 4m bits in each word. The reduction in storage to (15n + 1) words instead of 16n is quite common in such expansion (see explanation at end of this section). Data is entered into devices 1 through 4 and extracted from devices 5 through 8.

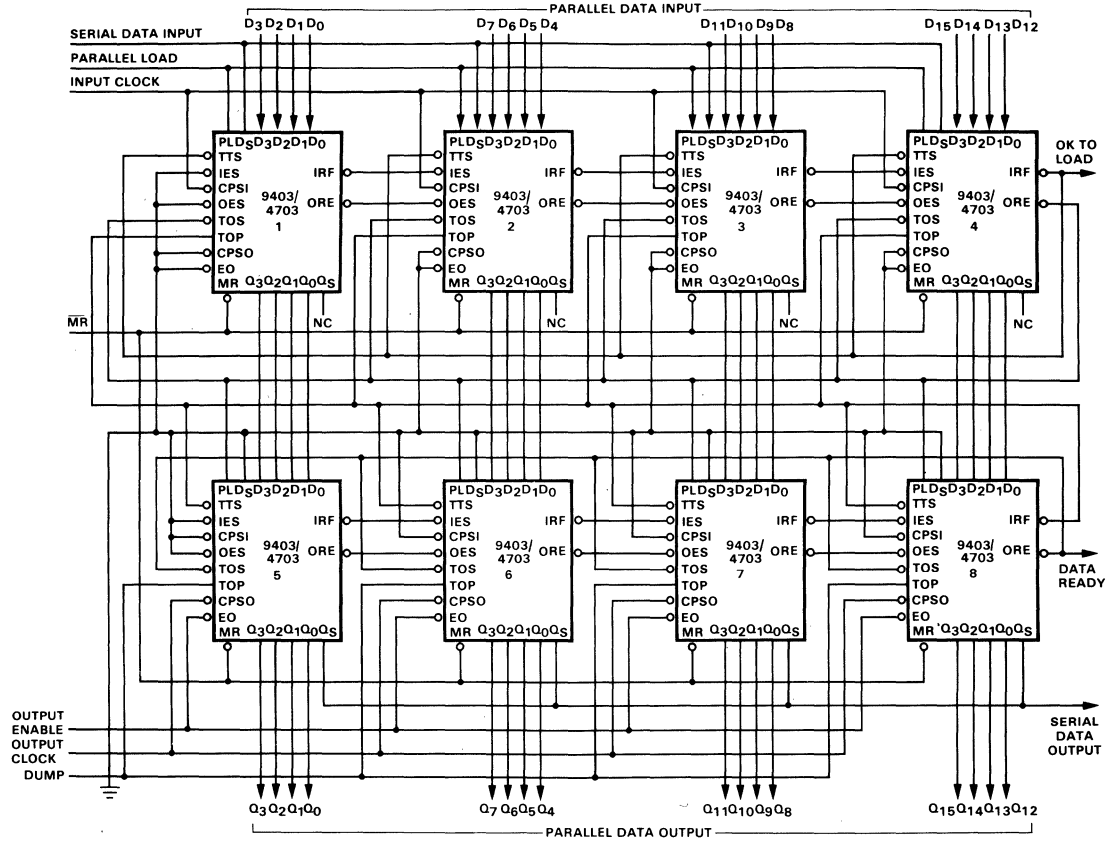


Fig. 5-30 31 x 16 FIFO Array

The D_S inputs of the first four devices are bussed together and serial data is entered on this line. The CPSI inputs are also connected together for clocking the serial data. The IES input of device 1 is connected to ground, while the IES inputs of devices 2, 3 and 4 are each connected to the IRF output of the preceding device. The IRF output of device 4 feeds into the TTS inputs of all four devices.

After initialization by a LOW level on the MR input, the IRF output of all four devices are HIGH. Under these conditions, only device 1 responds to the CPSI because its IES input is LOW. The first four clock pulses shift four data bits into the device-1 input register; its IRF output then becomes LOW. The first data bit is located in a flip-flop corresponding to the D_0 input of device 1. Control logic inhibits the CPSI from further affecting this device.

Because the IES input of device 2 is now LOW, the clock starts shifting data into the input register of device 2. On the eighth clock pulse, the IRF output of device 2 goes LOW and disables shifting of device 2. This process continues on devices 3 and 4. Therefore, on the 16th clock pulse, the IRF output of device 4 becomes LOW and activates the TTS inputs of all devices. The stack control logic in each device responds by transferring data into each stack from the respective input register, and the input registers are initialized. Thus the IRF outputs of all devices become HIGH once again. An automatic priority scheme assures that if the IRF output of device 4 is HIGH, the input registers of all four devices have been initialized. The timing diagram for 16 bits of serial entry into the array is shown in *Figure 5-31.*

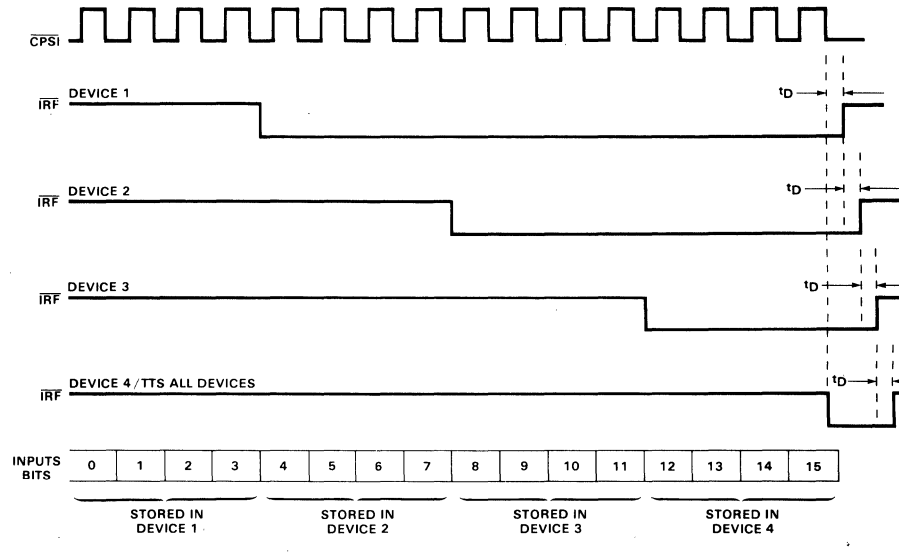


Fig. 5-31 Serial Data Entry for FIFO Array

Parallel entry into the array is made with a HIGH level on the PL inputs. The same conditions prevail in the input section that exist after the 16th clock pulse in the serial entry mode. The stack controls do not initialize the input registers until the PL inputs are LOW to assure proper device operation.

Data loaded into the stacks eventually arrives at the output registers of the first four devices. Normally, the ORE outputs are LOW due to initialization; however, as soon as data is loaded into each output register, the ORE goes HIGH. An automatic priority scheme, similar to the one for data entry, also exists at the output. Thus a HIGH level on the ORE output of device 4 guarantees that valid data is present in all the output registers.

The ORE output of device 4 is connected to the PL inputs of devices 5 through 8, as well as to the TOS inputs of the first four devices. It should be noted that if serial extraction from the output is not desired, the TOS inputs can be connected to ground instead. The EO inputs of the first four devices are connected to ground; thus the contents of an output register are available on the appropriate outputs.

The HIGH level on the ORE output of device 4 activates the PL inputs of devices 5 . . . 8, thus forcing the data outputs from each device in the first row into the input register of the corresponding device in the second row. The IRF output of device 8 is connected to the TOP inputs of devices 1 . . . 4 and to the TTS inputs of devices 5 . . . 8. Because the PL inputs are HIGH, the IRF outputs of devices 5 . . . 8 are LOW, therefore establishing a LOW on the TOP inputs of devices 1 . . . 4. This causes the ORE of devices 1 . . . 4 to go LOW and hence the PL inputs to devices 5 . . . 8. Furthermore, the LOW on the IRF output of device 8 also activates the TTS inputs of devices 5 . . . 8, thus initiating a fall-through action. The stack controls in devices 5 . . . 8 initialize their respective registers and the IRF outputs go HIGH. An automatic priority scheme is also present at the inputs of devices 5 . . . 8. The HIGH on the IRF output of device 8 restores the TOP inputs of devices 1 . . . 4 to the quiescent state.

If the stacks of devices 5 . . . 8 are full, activating the TTS inputs by the LOW IRF output of device 8 would not initiate a data transfer from the input registers. The IRF output of device 8 would remain LOW until the data can be successfully transferred into the stacks. Thus, as long as devices 5 . . . 8 are holding 16 words, the IRF output of device 8 remains LOW. This also holds the TOP inputs of devices 1 . . . 4 LOW. As long as they remain LOW, data cannot be loaded into the output registers from the stacks because a LOW-to-HIGH transition at the TOP inputs is needed to demand new data. Under these circumstances, devices 1 . . . 4 temporarily lose the ability to use their output registers and hence can hold only 15 words. As a result, the two rows have a storage capacity of 31 words instead of 32; and, for the general case, the storage capacity of an n-row array is (15n + 1) instead of 16n.

The data loaded into the stacks eventually arrives at the output registers of devices 5 . . . 8, at which time the ORE outputs go HIGH from the LOW state originally initialized by the MR input. The automatic priority scheme is still in effect, and the data from the output can be extracted either in serial or parallel format.

The Q_S outputs of devices 5 . . . 8, each available through a 3-state buffer, are connected together and the serial data output from the array appears on this line. The CPSO inputs are also connected together and the line driven by the output clock. When there is no valid data in the output register, Q_S is disabled and is therefore in a high impedance state.

The OES input of device 5 is connected to ground and devices 6, 7 and 8 each receives its OES input from the preceding device. As soon as data arrives in the output registers of devices 5 . . . 8, the ORE outputs go HIGH and the 3-state buffer of device 5 is enabled so that its Q_S output becomes identical to tis Q_0 output. The Q_S outputs of devices 5 . . . 8 are in a high impedance state. The clock on the CPSO input shifts the device-5 output register and data is shifted out in the same bit order as entered at the array input. After the fourth clock pulse, the ORE output of device 5 goes LOW and its Q_S output is disabled into the high impedance state.

The ORE output of device 5 establishes a LOW on the OES input of device 6. This enables its Q_S output buffer and a signal, corresponding to that of the Q_0 output, appears on the serial output line. Device 6 now

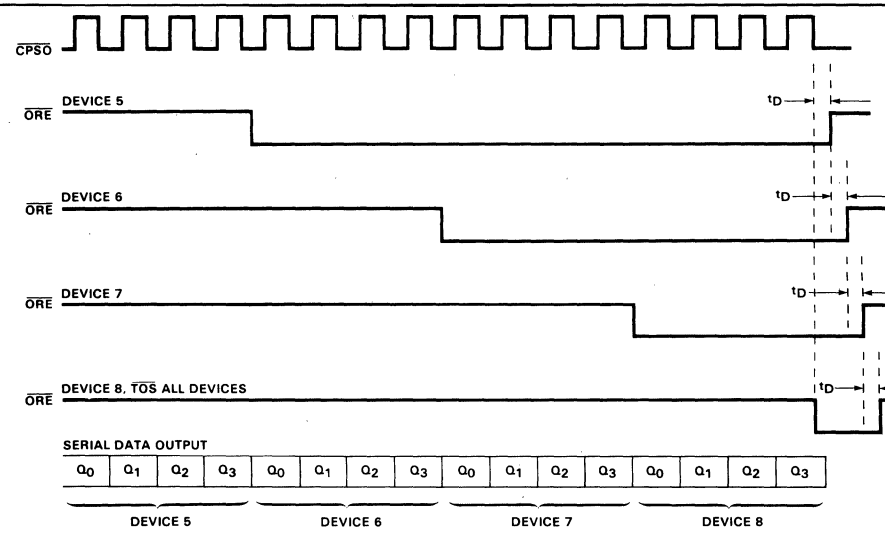


Fig. 5-32 Serial Data Extraction for FIFO Array

responds to the clock inputs and, after shifting the data out, its Q_S output goes into a high impedance mode. The LOW on the ORE output of device 6 enables device 7. This process continues until the last data bit has been shifted out of device 8, at which time its ORE output goes LOW. This activates the TOS inputs of devices 5 . . . 8 and new data can then be loaded from the stack when available. The timing diagram for 16 bits of serial data extraction is shown in *Figure 5-32.*

Data can be extracted from the array in parallel by activating the TOP inputs of device 5 . . . 8 LOW. New data is loaded into the output registers on the LOW-to-HIGH transition of this input. The TOP and EO inputs can be connected together so that data can be automatically extracted.

Automatic Priority Scheme

Most conventional FIFO designs provide status signals analogous to the IRF and ORE outputs. However, when these devices are operated in arrays, unit-to-unit delay variations require external gating to avoid transient false-status indications. This is commonly referred to as composite-status signal generation. The design of the 9403/4703 FIFO eliminates this problem. An automatic priority feature is built in to assure that a slow device will automatically predominate, irrespective of location in the array.

In *Figure 5-30,* devices 1 and 5 are defined as "row masters". Devices 2, 3 and 4 are "slaves" to device 1 while devices 6, 7 and 8 are slaves to device 5. The row master is established by sensing the IES input during the period when the MR input is LOW. Because of the initialization, the IRF outputs of all devices are HIGH for a short time after the HIGH-to-LOW transition of the MR input. Thus IES inputs of all devices except 1 and 5 are HIGH. This condition is sensed by the device logic to establish the row mastership.

All devices in any given row transfer data from their input registers into the corresponding stacks simultaneously. However, no slave can initialize its input register until its IES input goes HIGH. Thus initialization starts with the row master and eventually ends at the last slave in the row.

A similar situation occurs at the output registers of all devices in a row. They are loaded simultaneously from corresponding stacks; however, the ORE output of a slave cannot go HIGH until its OES input is HIGH. Thus the row master is the first to indicate a HIGH on its ORE and eventually the slaves will follow. It should be pointed out that this automatic priority scheme reduces the maximum operation speed of the array. If speed is essential, the master-slave hierarchy can be replaced by the traditional composite-status signal-generation scheme, which requires external gating.

Other Expansion Schemes

The expansion scheme illustrated in *Figure 5-30* is quite simple and straightforward. It does not require any external support logic to achieve the desired expansion and retains all the serial/parallel features. However, these advantages are not without sacrifice—one storage location is eliminated at the interface between rows—and the n-row array has a storage capacity of 15n+1 instead of 16n words. Moreover, the automatic priority scheme results in a ripple action from row master to the last slave in that row for the status signaling. This reduces the maximum operation frequency of an array and the inherent speed of the individual devices is not fully utilized.

The 9403/4703 FIFO, because of its versatility, can be used to overcome both above disadvantages with minimum external logic. A vertically expanded array, consisting of three FIFOs, yields 16n words of storage for an n-row array *(Figure 5-33)*. After initialization by a LOW level on the $\overline{MR}$ inputs, the $\overline{IRF}$ outputs of all three devices are HIGH and the $\overline{ORE}$ outputs LOW. The AND gates at the row interface are thus disabled. The PL inputs of devices 2 and 3 are LOW. Now, if the input register of device 1 receives four bits of data, then $\overline{IRF}$ output goes LOW. This activates the $\overline{TTS}$ input and the data falls through into the output register of device 1 and the $\overline{ORE}$ output becomes HIGH. Since the $\overline{IRF}$ output of device 2 is HIGH from initialization, the AND gate between devices 1 and 2 is enabled and the PL input of device 2 becomes HIGH. Data from device 1 is loaded into the input register of device 2 causing the $\overline{IRF}$ output of device 2 to go LOW. Moreover, a HIGH level on the PL input of device 2 results in a LOW level on the TOP input of device 1. As a result, the $\overline{ORE}$ output of device 1 also becomes LOW. Either way, the AND gate is disabled and the PL input of device 2 goes LOW and the TOP input of device 1 becomes HIGH.

The LOW level on the $\overline{IRF}$ output of device 2 activates its $\overline{TTS}$ input and initiates a fall-through action; the data appears at the output register. Because the TOP input of device 1 is HIGH, new data arrives at the device-2 output register. When data appears at the output of device 2, the AND gate at the interface of devices 2 and 3 is enabled. By a similar action described above, device 3 takes the data word into its input register and passes it on to the output. Thus, if 16 words are loaded at the input to the array, the 1st word is located in the output and the 16th word is in the input register of device 3. Device 3 is full now and its $\overline{IRF}$ output remains LOW until data is extracted. This LOW level disables the AND gate between devices 2 and 3 and hence any arrival of new data into the output register of device 2 does not activate the PL input of device 3. As new data is received, it is arranged in devices 1 and 2 so that the 17th data word falls into the device 2 output register and the 48th word remains in the input register of device 1. Forty-eight data words fill all devices in the array. Under these conditions, the status output is as follows: the $\overline{IRF}$ outputs of devices 1, 2, and 3 are LOW and the $\overline{ORE}$ outputs of devices 1, 2 and 3 HIGH.

The data extraction takes place when the TOP input of device 3 is activated; normally it is HIGH. To extract data, TOP is made LOW and then HIGH. When the TOP input is LOW, the $\overline{ORE}$ of device 3 goes LOW. When TOP is returned HIGH, data is demanded from the stack.

The internal control in device 3 loads the second data word into the output register and the $\overline{ORE}$ goes HIGH. The internal control also initiates a fall through action in device 3. Thus, the 16th data word that was located in the input register is transferred into the device -3 stack and the input register is initialized. Thus, the $\overline{IRF}$ output of device 3 becomes HIGH.

The 17th data word is located in the output register of device 2, hence the $\overline{ORE}$ output is HIGH. When the $\overline{IRF}$ output of device 3 becomes HIGH, the AND gate at the interface causes the PL input of device 3 to go HIGH and the TOP input of device 2 LOW. The 17th data word then goes into the input register of device 3. The internal control of device 2 initiates fall-through action so that the 18th word falls into the output and the 32nd word is transferred into the stack. This results in a HIGH at the $\overline{IRF}$ output of device 2. Similar action takes place between devices 1 and 2 with the net result that all data has fallen one location creating a vacancy in the input register of device 1. It is now clear that this FIFO array has a 48-word capacity without affecting the serial/parallel data feature at the input or the output. It can then be concluded that if an array of n rows is constructed using the proposed scheme, the effective storage capacity of the FIFO is 16n words.

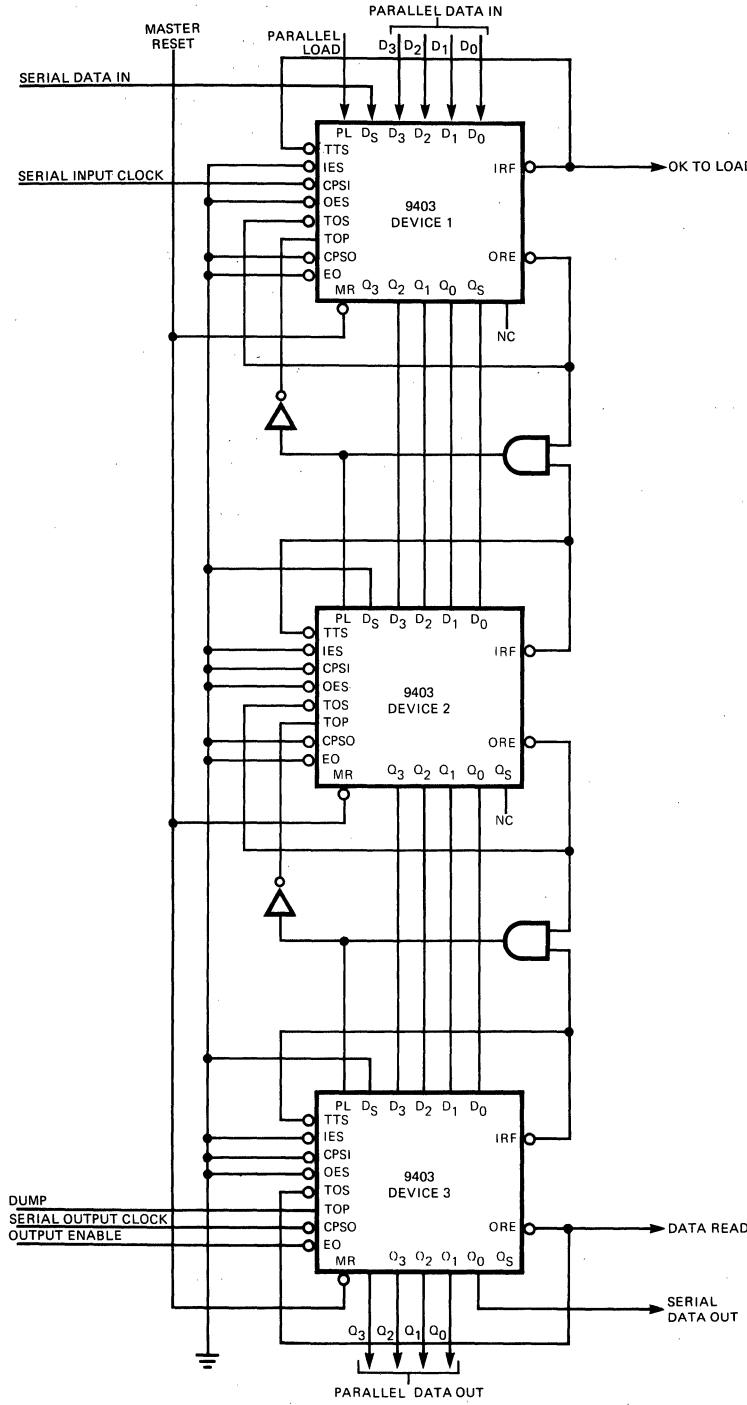


Fig. 5-33 Expansion without Sacrificing a Storage Location at the Interface

The array of *Figure 5-34* has all the features and yet operates at a higher speed than the array shown in *Figure 5-30*. Whenever the $\overline{IRF}$ output of device 1 is HIGH, the $\overline{IES}$ inputs of devices 2, 3 and 4 are also HIGH. Therefore, when the array is initialized by a LOW level on the $\overline{MR}$ inputs, device 1 is the row master and devices 2, 3 and 4 are the slaves. In the second row of devices, the $\overline{IRF}$s and $\overline{IES}$s are interconnected so that device 5 is also a row master and devices 6, 7 and 8 are slaves.

When serial data is entered into the array, device 1 receives the first four bits of data. Devices 2, 3 and 4 do not respond to the clock since all three $\overline{IES}$ inputs are HIGH. After the 4th bit, the $\overline{IRF}$ output of device 1 is LOW. This disables device 1 from responding to the clock and enables device 2 so that the next four bits are entered into device 2. Devices 3 and 4 remain disabled by a HIGH level on the $\overline{IES}$ inputs. After the 8th bit, the $\overline{IRF}$ of device 2 becomes LOW, thus disabling device 2 and enabling device 3. After the 12th bit, the $\overline{IRF}$ output of device 3 is LOW and thus device 4 is enabled. After the 16th bit, the $\overline{IRF}$ output of device 4 is LOW. So far, the serial data entry into this array is identical to that for the array in *Figure 5-30.*

The LOW level on the $\overline{IRF}$ output of device 4 activates the $\overline{TTS}$ inputs of all 4 devices, causing the transfer of data into the stacks. Although all devices transfer data into the stack simultaneously, device 1 (row master) is the first to initialize its input register. Since devices 2, 3 and 4 are slaves, they need a HIGH on their $\overline{IES}$ inputs for input-register initialization. As soon as the $\overline{IRF}$ output of device 1 goes HIGH due to initialization, the $\overline{IES}$ inputs of devices 2, 3 and 4 become HIGH and their input registers are initialized simultaneously. This is in contrast to *Figure 5-30* where device 3 has to wait for device 2 to initialize, etc. The ripple action of input initialization has been overcome by simple gating. The $\overline{IRF}$ outputs of devices 1, 2, 3 and 4 are fed into 4-input AND gates to generate the composite input status. To obtain an indication that the input register of the array is empty, the input register of each device in the first row should be empty.

The $\overline{ORE}$ and $\overline{OES}$ interconnections for the second row are essentially similar to the input section. This gating at the output section eliminates the rippling effect of the output status indication. If the gating arrangement used in *Figure 5-33* is incorporated into the array of *Figure 5-34,* the result is a 32 word x 16-bit FIFO network.

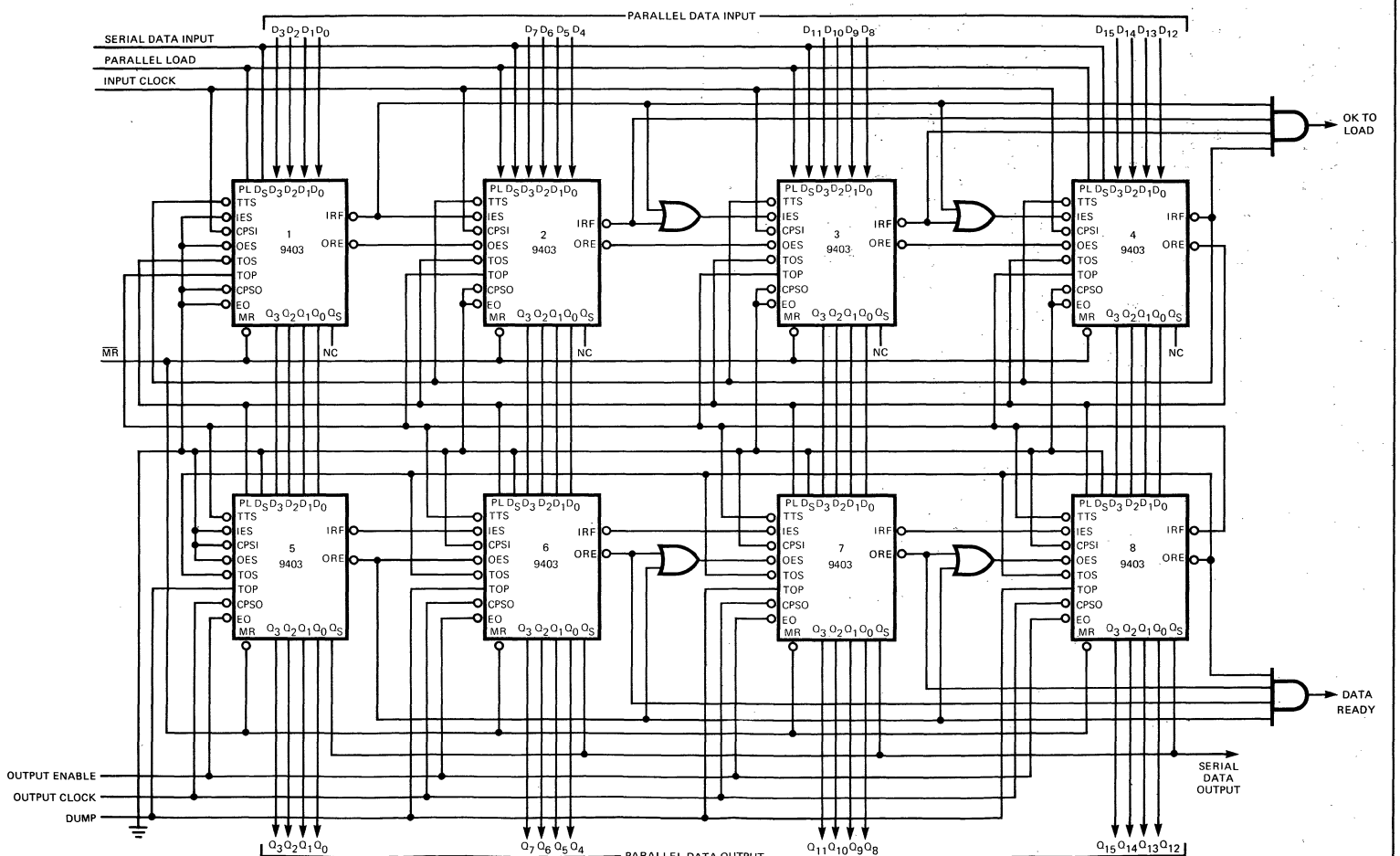
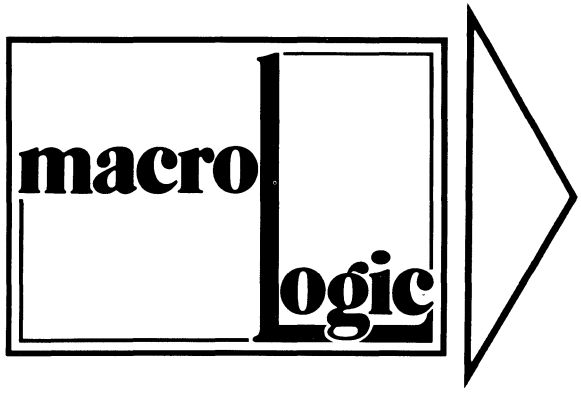


Fig. 5-34 Expansion with Priority Defeated for Faster Operation



MACROLOGIC ORDERING INFORMATION

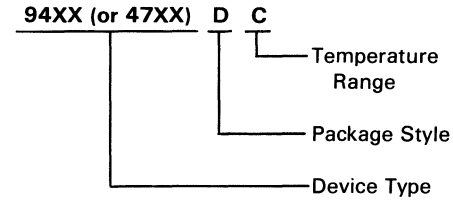
Fairchild Macrologic circuits may be ordered using a simplified purchasing code in which the package style and temperature range are defined below.

TEMPERATURE RANGE

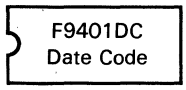
M = Military −55°C to +125°C
C = Commercial 0°C to +75°C (Bipolar),
−40°C to +85°C (CMOS)

PACKAGE STYLE

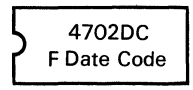
D = Dual In-line – Ceramic (Hermetic)
P = Dual In-line – Plastic



BIPOLAR MACROLOGIC DEVICE MARKING EXAMPLE



CMOS MACROLOGIC DEVICE MARKING EXAMPLE



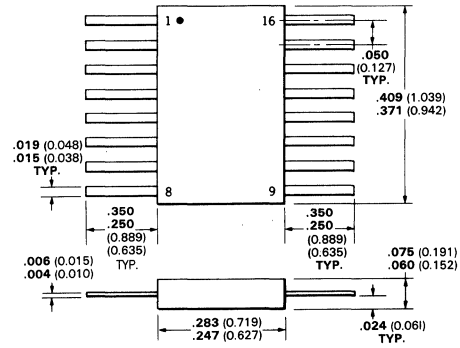
In order to accommodate varying die sizes (MSI, LSI, etc.), numbers of pins (16, 18, 24, etc.), and package outlines, a number of different package forms are required in each of the three package style categories.

The following list indicates the specific package dimensions currently used for each device type. The detailed outline corresponding to each package code is shown at the end of this section.

DEVICE	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
Bipolar			
9401	7A	9A	
9403	6Q	9U	
9404	6Q	9U	
9405	6Q	9U	
9405A	6Q	9U	
9406	6Q	9U	
9407	6Q	9U	
9408	6I	8P	
9410	7D	9M	
CMOS			
4702	6B	9B	4L
4703	6Q	9U	4M
4704	6Q	9U	4M
4705	6Q	9U	4M
4706	6Q	9U	4M
4707	6Q	9U	4M
4708	6I	8P	
4710	7D	9M	

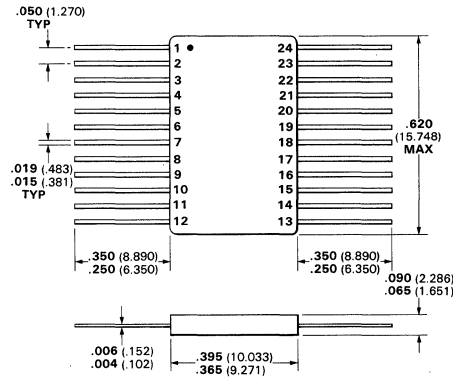
PACKAGE OUTLINES

16-Pin Cerpak 4L



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are gold-plated kovar
Package weight is 0.4 gram

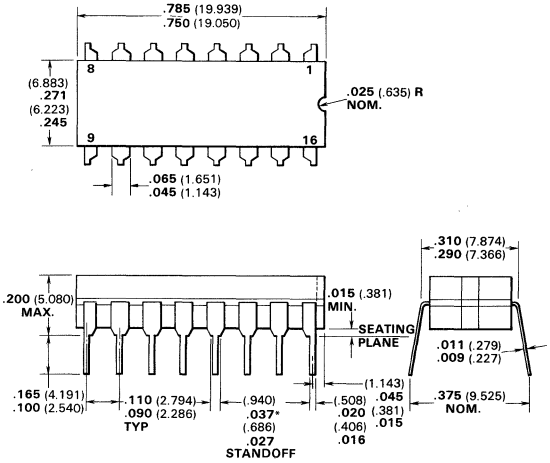
24-Pin BeO Cerpak 4M



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are gold-plated kovar
Package weight is 0.8 gram

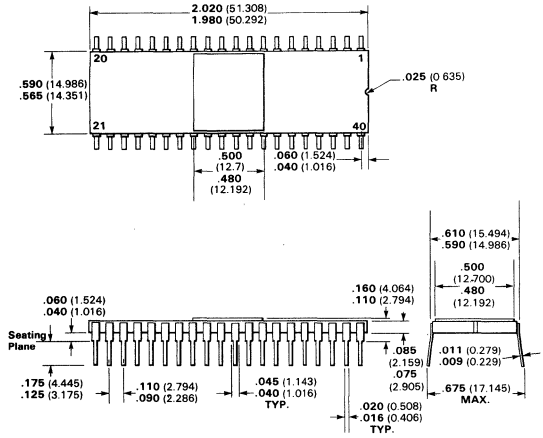
PACKAGE OUTLINES

16-Pin Ceramic Dual In-line 6B



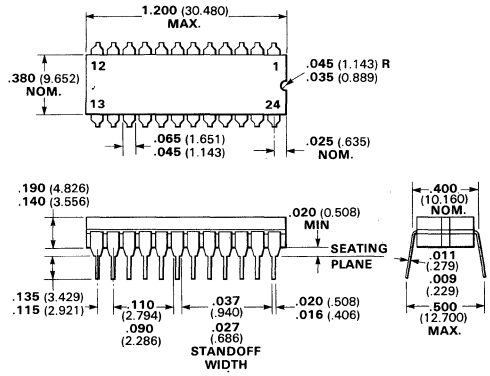
NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .400" (10.16) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin
Pins are tin-plated kovar

40-Pin Dual In-line Side-Brazed Package (Large Cavity) 6I



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pin material nickel gold-plated kovar
Cap is kovar
Base is ceramic
Package weight is 6.5 grams

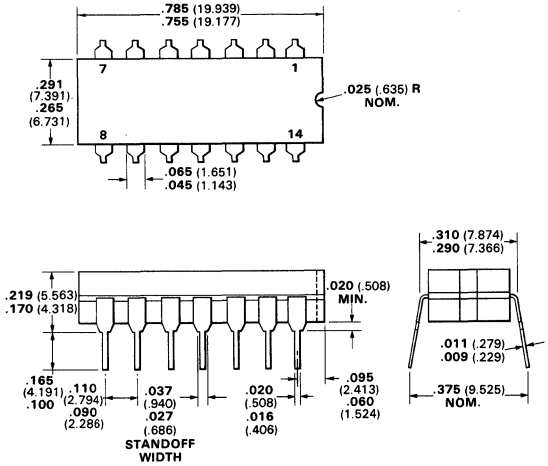
24-Pin Ceramic Dual In-line 6Q



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pins
Pins are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner pins

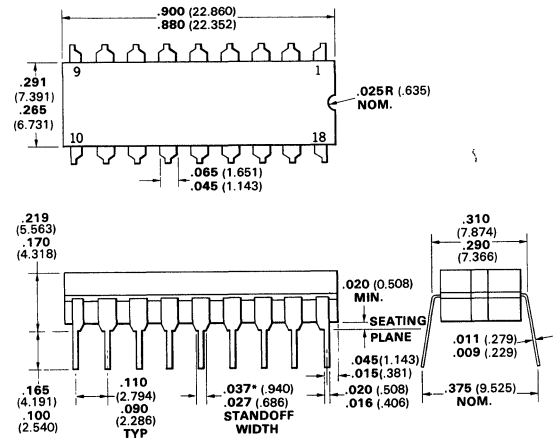
PACKAGE OUTLINES

14-Pin Ceramic Dual In-line 7A



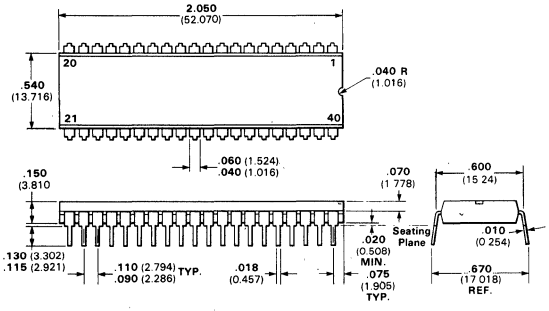
NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin
Pins are tin-plated kovar
Package weight is 2.0 grams

18-Pin Ceramic Dual In-line 7D



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin
Pins are tin-plated kovar
*The .037/.027 dimension does not apply to the corner pins

40-Pin Plastic Dip (Production Mold) 8P

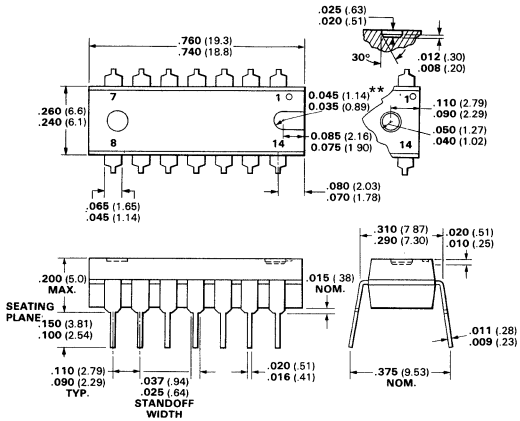


NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .600" (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

PACKAGE OUTLINES

14-Pin Plastic Dual In-line *

9A



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated kovar

*Package material varies depending on the product line

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

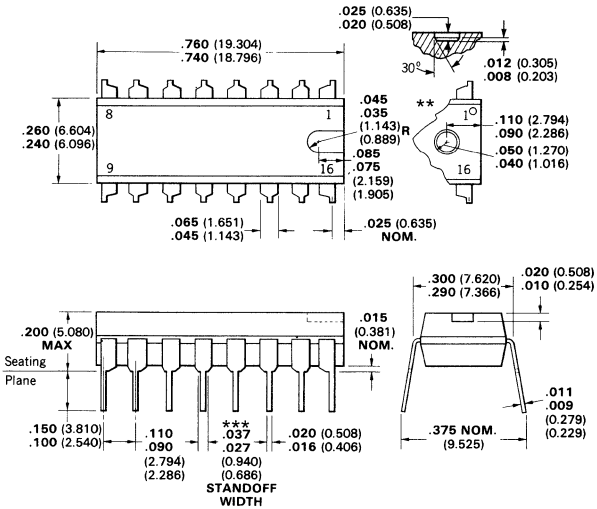
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

**Notch or ejector hole varies depending on the product line

Package weight is 0.9 gram

16-Pin Plastic Dual In-line *

9B



NOTES:

All dimensions in inches (bold) and millimeters (parentheses)

Pins are tin-plated kovar or alloy 42 nickel

*Package material varies depending on the product line

Pins are intended for insertion in hole rows on .300" (7.62) centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin

**Notch or ejector hole varies depending on the product line

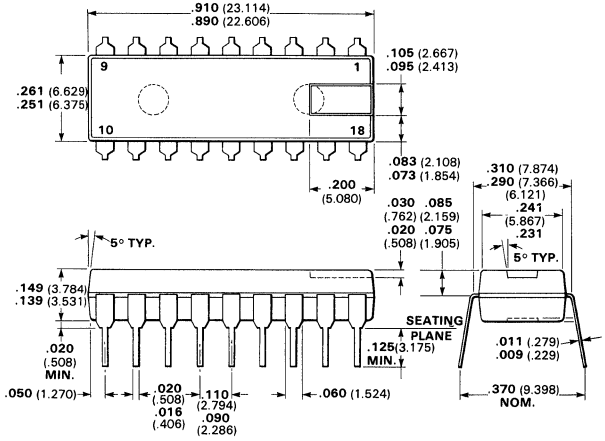
***The .037/.027 dimension does not apply to the corner pins

Package weight is 0.9 gram

6

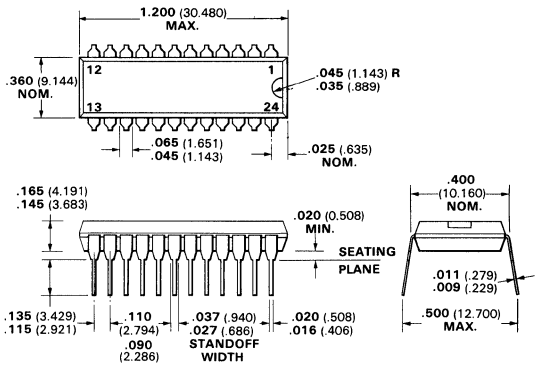
PACKAGE OUTLINES

18-Pin Plastic Dual In-line 9M

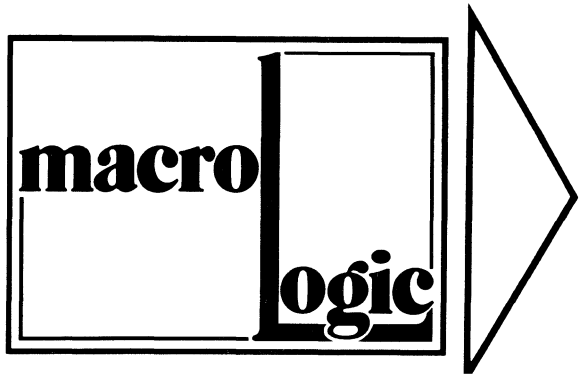


NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin
Pins are tin-plated kovar

24-Pin Plastic Dual In-line 9U



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.51) diameter pin
Pins are tin-plated kovar



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Printed in U.S.A./212-12-0001-056/30M