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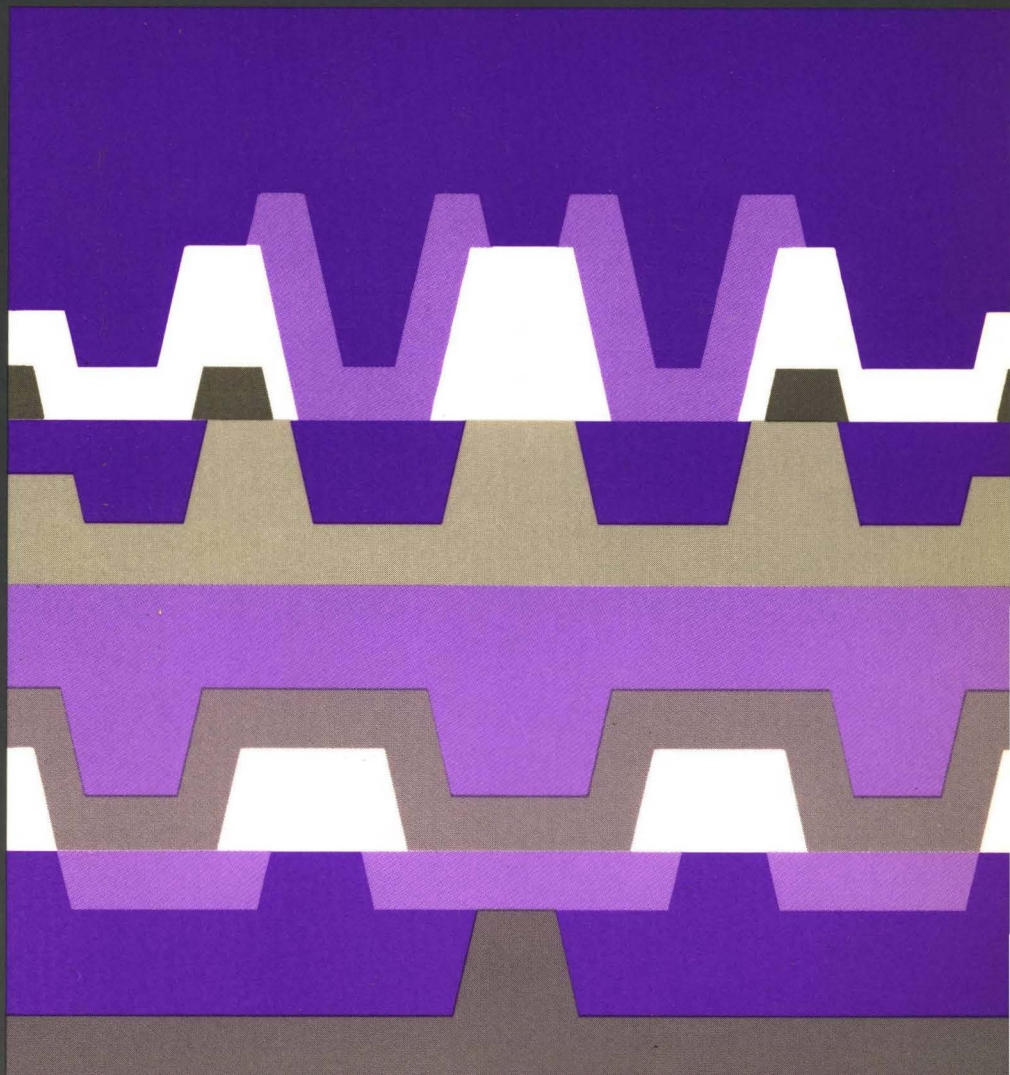
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4-BIT SINGLE-CHIP
MICROCOMPUTER DATA BOOK

4-BIT SINGLE-CHIP MICROCOMPUTER DATA BOOK

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4-BIT SINGLE CHIP MICROCOMPUTER DATA BOOK

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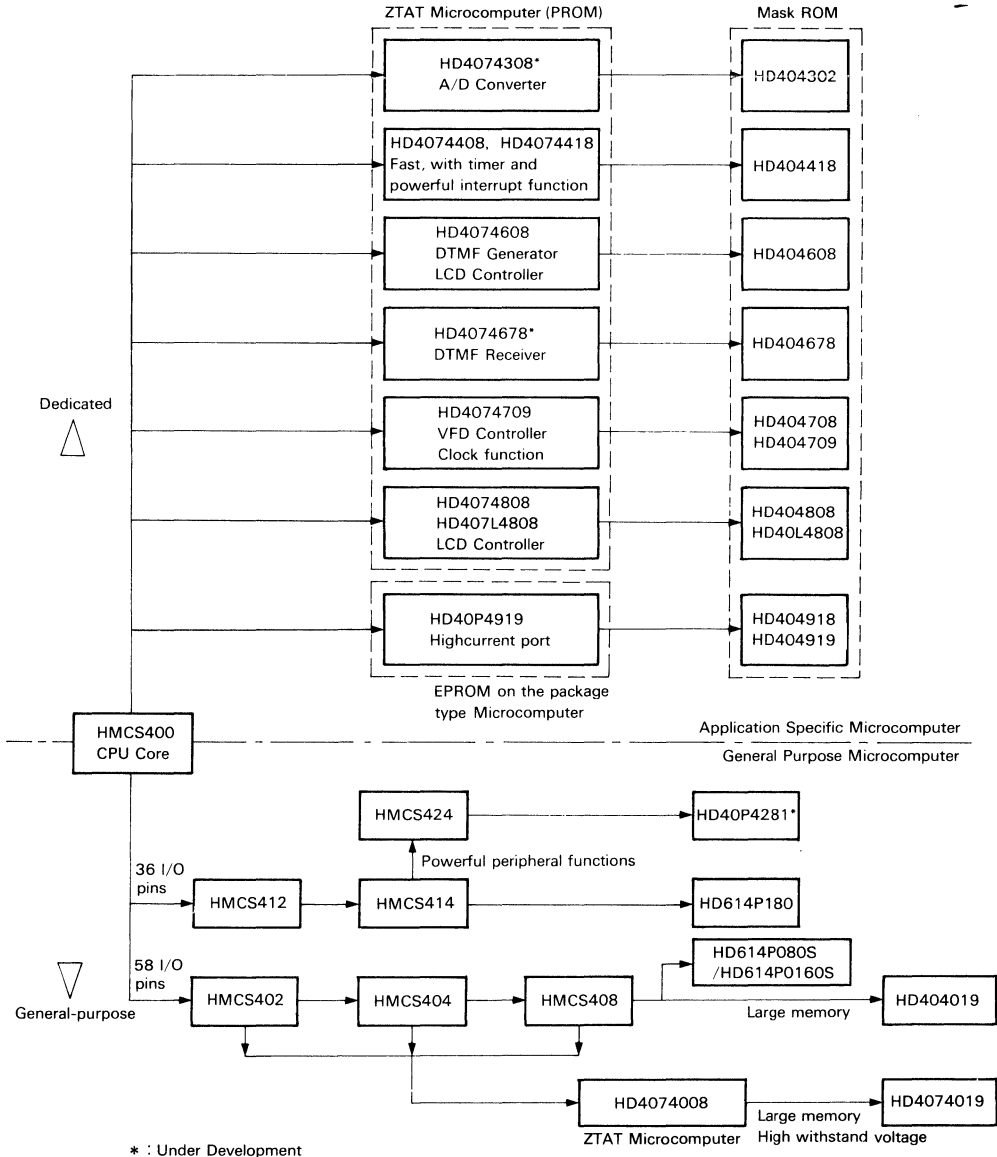
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General Information

- **Quick Reference Guide**
- **Introduction of Packages**
- **Reliability and Quality Assurance**
- **Reliability Test Data of Microcomputer**
- **Program Development Procedure and Support Systems**

Quick Reference Guide

HMCS400 Series Line up



Quick Reference Guide

HMCS400 Series Application Specific Microcomputer

Specific Feature Part No.	A/D Converter		Multi function Timer		
	HD404302	HD4074308*	HD404418	HD4074418	HD4074408
Supply voltage (V)	5	5	5	5	5
Operating Temperature Range (°C)	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
Package	DP-42	DP-42,DC-42	DP-64S,FP-64, FP-64A	DP-64S,DC-64S FP-64,FP-64A	DP-64S,DC-64S FP-64,FP-64A
ROM (bits)	2048 x 10	8192 x 10	8192 x 10	8192 x 10	8192 x 10
RAM (bits)	160 x 4	160 x 4	512 x 4	512 x 4	512 x 4
I/O port	33	33	58	58	58
Interrupts	external	2	2	6	6
	internal	3	3	6	6
Timer	8bit timer x 2 〔auto-reload timer/event counter free running timer/watchdog timer		8bit timer x 4 〔auto-reload timer/event counter/PWM free-running timer/watchdog timer		
Serial Interface	—	—	8bit x 2 (clock synchronous)		
Others	A/D converter (8bit x 4 channel) Tone Generator Watchdog Timer 26 high voltage ports (40 V) Low power dissipation modes 〔stop mode/standby mode		PWM output Watchdog timer 8 high voltage ports (+12 V) (HD4074408 only) Low power dissipation mode 〔stop mode/standby mode		

* : Under development



Quick Reference Guide

DTMF Generator HD404608		PRELIMINARY	
		Phase Lock Loop	
HD4074608		HD404508*	HD4074509*
5	5	5	5
-20 to +75	-20 to +75	-40 to +70	-40 to +70
FP-80B,FP-80A	FP-80B,FP-80A	FP-80B	FP-80B
8192 × 10	8192 × 10	8192 × 10	16384 × 10
1184 × 4	1184 × 4	512 × 4	512 × 4
30	30	29	29
2	2	5	5
4	4	6	6
8 bit timer × 3 free-running timer/time base auto-reload timer/event counter auto-reload timer/watchdog timer		8 bit timer × 2 20 bit timer × 1 8-bit multiplexed w/reload, event, PWM 8-bit multiplexed w/reload, event 20-bit free running	
8-bit × 1 (clock synchronous)		8-bit × 2 (clock synchronous)	
DTMF generator LCD controller/driver Watchdog timer Clock function (32 kHz crystal oscillator) Low power dissipation modes stop mode/standby mode watch mode/subactive mode		PLL with prescaler (max 160 MHz) LCD controller/driver A/D converter (8-bit × 2 channel) IF counter (15 MHz max. input)	

Quick Reference Guide

Specific Feature Part No.	DTMF Receiver HD404678	VFD controller/driver HD404708 HD404709 HD4074709		
Supply voltage (V)	5	5	5	5
Operating Temperature Range (°C)	-20 to +75	-20 to +75	-20 to +75	-20 to +75
Package	FP-64A	DP-64S FP-64B	DP-64S FP-64B* FP-64A*	DP-64S, FP-64A* FP-64B*, DC-64S
ROM (bits)	8192 x 10	8192 x 10	16384 x 10	16384 x 10
RAM (bits)	512 x 4	576 x 4	576 x 4	576 x 4
I/O port	52	56	56	56
Interrupts	external	4	4	4
	internal	7	5	5
Timer	8bit timer x 4 <ul style="list-style-type: none"> ┌ free-running timer ├ auto-reload timer ├ event counter └ timer-output circuits 	8bit timer x 3 <ul style="list-style-type: none"> ┌ free-running timer/timer base ├ auto-reload timer/event counter └ auto-reload timer/watchdog timer 		
Serial Interface	8bit x 2 (clock synchronous)	8bit x 1 (clock synchronous)		
Others	DTMF receiver Reset voltage variable function Low power dissipation modes <ul style="list-style-type: none"> ┌ standby mode/stop mode 	VFD controller/driver Clock function (32 kHz crystal oscillator) Watchdog timer Low power dissipation modes <ul style="list-style-type: none"> ┌ stop mode/watch mode └ standby mode/subactive mode 		

* : Under development



LCD Controller/Driver			
HD404808	HD4074808	High Current Port	
HD40L4808	HD407L4808	HD404918	HD404919
5	5	5	5
-20 to +75	-20 to +75	-20 to +75	-20 to +75
FP-80B,FP-80A	FP-80B,FP-80A	DP-42	DP-42
8192 x 10	8192 x 10	8192 x 10	16384 x 10
1184 x 4	1184 x 4	512 x 4	992 x 4
30	30	35	35
2	2	2	2
4	4	1	1
8bit timer x 3 { free-running timer/time base auto-reload timer/event counter auto-reload timer/watchdog timer		8bit timer x 1 { auto-reload timer/event counter	
8bit x 1 (clock synchronous)		-	-
LCD controller/driver		27 high voltage ports (+12 V)	
Clock function (32 kHz crystal oscillator)		8 high current port (25 mA)	
Watchdog timer		Low power dissipation modes	
Low power dissipation modes { stop mode/watch mode standby mode/subactive mode		Low power dissipation modes { stop mode/standby mode	

Quick Reference Guide

HMCS400 Series General Purpose Microcomputer

Part No.		HMCS402AC/C/CL	HMCS404AC/C/CL	HMCS408AC/C/CL	HMCS412AC/C/CL
Clock Frequency (MHz)		6/4/2	6/4/2	4/4/2	4/4/2
Supply voltage (V)		5/5/3	5/5/3	5/5/3	5/5/3
Power dissipation (max) (mW)	operate	27/10/9	27/10/9	22.5/11.5/5.5	15/9/4
	standby	9/6/3	9/6/3	8.5/6/2.5	7/5/2.5
	stop	0.06	0.06	0.05	0.05
Operating Temperature Range (°C)		-20 to +75	-20 to +75	-20 to +75	-20 to +75
Package		DP-64S,FP-64	DP-64S,FP-64	DP-64S,FP-64 FP-64A	DP-42,DP-42S FP-44A
Memory	ROM	2048 x 10	4096 x 10	8192 x 10	2048 x 10
	RAM	160 x 4	256 x 4	512 x 4	160 x 4
	I/O	36	36	36	31
I/O	input	6	6	6	1
	output	16	16	16	4
Interrupts	external	2	2	2	2
	timer/counter	2	2	2	1
	serial	1	1	1	-
Timer	Timer A	8bit free-running timer/counter			-
	Timer B	8bit auto-reload timer/event counter			8bit auto-reload timer/event counter
Serial Interface		8bit x 1 (clock synchronous)			-
Instruction execution time (μs)		1.33/2/4	1.33/2/4	1/2/4	1/2/4
Others		Low power dissipation modes standby mode, stop mode 58 I/O pins including 26 high voltage			Low power dissipation modes standby mode/stop mode 36 I/O pins including 24 high voltage

HMCS400 Series EPROM on the Package Type

Part No.	HD614P080S	HD614P016S	HD614P180	HD40P4281*	HD40P42161*	HD40P4919
Supply voltage (V)	5	5	5	5	5	5
Operating Temperature Range (°C)	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
Package	DC-64SP	DC-64SP	DC-42P	DC-42P	DC-42P	DC-42P
Equivalent Device	HMCS402C/AC HMCS404C/AC	HMCS408C/AC	HMCS412C HMCS414C	HMCS424C/AC	HMCS424C/AC	HD404918 HD404919
Mountable EPROM	HN482764 HN27C64 HN4827128	HN27C256	HN482764 HN27C64 HN4827128	HN482764 HN27C64 HN4827128	HN27256	HN27C256

* : Under development



Quick Reference Guide

HMCS414AC/C/CL	HMCS424AC/C/CL	HD4074008	HD4074019	HD404019
4/4/2	4/4/2	8	4	4
5/5/3	5/5/3	5	5	5
15/9/4	16/10/3.5	22.5	TBD	TBD
7/5/2.5	8.5/6/2.5	8.5	TBD	TBD
0.05	0.05	0.05	TBD	TBD
-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
DP-42, DP-42S FP-44A	DP-42, DP-42S FP-44A	DC-64S, DP-64S FP-64, FP-64A	DC-64S, DP-64S FP-64B*, FP-64A*	DP-64S, FP-64B*, FP-64A*
4096 x 10	4096 x 10	8192 x 10	16384 x 10	16384 x 10
160 x 4	256 x 4	512 x 4	992 x 4	992 x 4
31	31	36	52	52
1	1	6	6	6
4	4	16	-	-
2	2	2	2	2
1	2	2	2	2
-	1	1	1	1
-	8bit free-running timer/counter	8bit free-running timer/counter		
		8bit auto-reload timer/event counter		
-	8bit x 1 (clock synchronous)	8bit x 1 (clock synchronous)		
1/2/4	1/2/4	1	1	1
		Low power dissipation modes standby mode/stop mode		

*: Under Development



Quick Reference Guide

CMOS 4-Bit Single-Chip Microcomputer HMCS40 Series

Family Name (Type Name)		HMCS42CL (HD44708) HMCS42C (HD44700)	HMCS43CL (HD44758) HMCS43C (HD44750)	HMCS44CL (HD44808) HMCS44C (HD44801)
Supply Voltage	(V)	3/5	3/5	3/5
Power Dissipation (typ.)	(mW)	0.23/1.5	0.24/1.5	0.32/2
Max. I/O Terminal Voltage	(V)	10	10	10
Operating Temperature Range **1	(°C)	-20 to +75	-20 to +75	-20 to +75
Package		DP-28, DP-28S**4	DP-42, DP-42S**4	DP-42, DP-42S**4
Memory	ROM	(bits) 512 x 10 32 x 10 ^{*2}	1,024 x 10 64 x 10 ^{*2}	2,048 x 10 128 x 10 ^{*2}
	RAM	(bits) 32 x 4	80 x 4	160 x 4
Registers		4	6	8
Stack Registers		2	3	4
I/O Ports	4-Bit Data Input	4 x 1	4 x 1	—
	4-Bit Data Output	4 x 2	4 x 2	—
	Discrete Output	22 1 x 6	32 1 x 12	32 —
	4-Bit Data Input/Output	—	4 x 1	4 x 4
	Discrete Input/Output	1 x 4	1 x 4	1 x 16
Interrupts	External	—	2	2
	Timer/Counter	—	1	1
Instructions	Number of Instructions	52	87	87
	Cycle Time (μs)	20/10	20/10	20/10
Built-in Clock Pulse Generator			Yes	
Power on Reset		No/Yes	No/Yes	No/Yes
Battery Back-up		Halt	RAM Hold	Halt
Evaluation Chip		HD44850E HD44857E	HD44850E HD44857E	HD44850E HD44857E

* 1 Wide Temperature Range (-40 to +85°C) version is available.

* 2 Pattern Memory

* 3 LCD DRIVE FUNCTION

LCD Drive	Common	4
	Segment	32
	Duty	Static, 1/2, 1/3, 1/4
	Bias	1/2, 1/3
Display Capability	4 x 32 Matrix (1/4 Duty)	

Expandable using the LCD Driver HD44100H.

* 4 As for low-voltage operation version, a shrink package isn't prepared.



Quick Reference Guide

HMCS45CL (HD44828) HMCS45C (HD44820)	HMCS46CL (HD44848) HMCS46C (HD44840)	HMCS47CL (HD44868) HMCS47C (HD44860)	LCD-III*3 (HD44795, HD44790)	LCD-IV*3 (HD613901)
3/5	3/5	3/5	3/5	3/5
0.32/2	0.32/4	0.32/4	0.36/2.4	0.9/5.0
10	10	10	10	Vcc +0.3
-20 to +75	-20 to +75	-20 to +75	-20 to +75	-20 to +75
FP-54, DP-64S	DP-42, DP-42S*4	FP-54, DP-64S	FP-80	FP-80
2,048 x 10 128 x 10*2	4,096 x 10	4,096 x 10	2,048 x 10 128 x 10*2	4,096 x 10
160 x 4	256 x 4	256 x 4	160 x 4	256 x 4
6	8	6	6	6
4	4	4	4	4
—	—	—	4 x 1	4 x 1
4 x 1	—	4 x 1	4 x 1	4 x 1
44 —	32 —	44 —	32 —	32 —
4 x 6	4 x 4	4 x 6	4 x 2	4 x 2
1 x 16	1 x 16	1 x 16	1 x 16	1 x 16
2	2	2	2	2
1	1	1	1	1
71	87	87	87	87
20/10	20/5	20/5	20/10	20/5
Yes				
No/Yes	No/Yes	No/Yes	Yes	No
Halt	Halt	Halt	Halt	Halt
HD44850E HD44857E	HD44857E	HD44857E	HD44797E	HD44797E



Introduction of Packages

Hitachi microcomputer devices include various types of package which meet a lot of requirements such as ever smaller, thinner and more versatile electric appliances. When selecting a package suitable for the customers' use, please refer to the following for Hitachi microcomputer packages.

1. Package Classification

There are pin insertion types, surface mounting types and multi-function types, applicable to each kind of mounting method. Also plastic and ceramic materials are offered according to use. Figure 1 shows the package classification according to the mounting types on the Printed Circuit Board (PCB) and the materials.

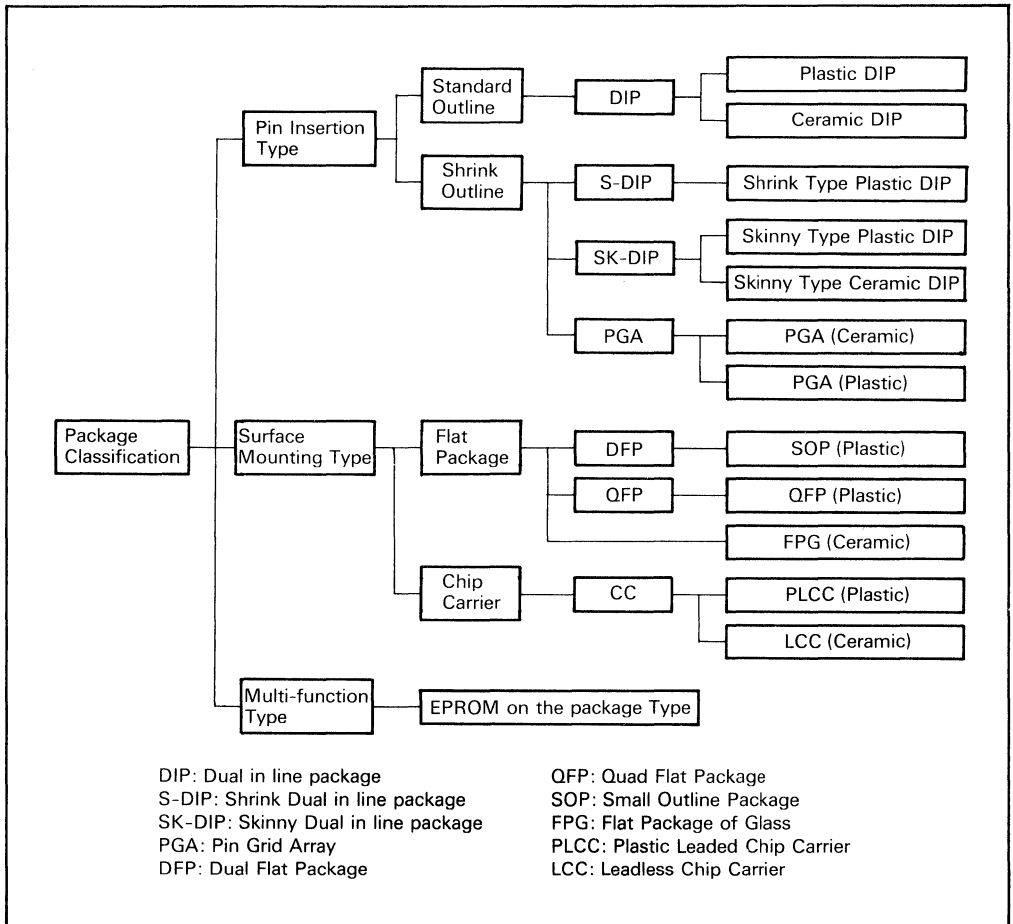


Figure 1. Package Classification according to the Mounting Type on the Printed Circuit Board and the Materials

Introduction of Packages

2. Type No. and Package Code Indication

Type No. of Hitachi 4-bit single-chip micro-computer device is followed by package material and outline specifications, as shown below. The package type used for each

device is identified by code as follows, illustrated in the data sheet of each device.

When ordering, please write the package code beside the type number.

Type No. Indication

HDXXXXXS

Note HDXXXPXXXX stands for Type No. of EPROM on the package type microcomputer device.

Package classification
HMCS 40 series
No Indication; Plastic DIP
S; Shrink Type Plastic DIP
F; QFP
HMCS 400 series
F; QFP
H; QFP
P; Plastic DIP
S; Shrink Type Plastic DIP
C; Ceramic DIP

Package Code Indication

DP-64SA

Outline
D; DIP
F; FLAT

Number of pins

Materials
P; Plastic
C; Ceramic
G; Glass sealed Ceramic

Additional outline 1
S; Shrink Type
P; EPROM on the package
SP; EPROM on the shrink package

Additional outline 2



3. Package Dimensional Outline

Hitachi 4-bit single-chip microcomputer

device employs the packages shown in Table 1 according to the mounting method on the PCB.

Table 1. Package List

Mounting method	Package classification	Package material	Package code
Pin insertion type	Standard Outline (DIP)	Plastic	DP-28 DP-42
		Ceramic	DC-42
	Shrink Outline (S-DIP)	Plastic	DP-28S DP-42S DP-64S
		Ceramic	DC-64S
Surface mounting type	Flat package QFP	Plastic	FP-44A FP-80 FP-54 FP-80B FP-64 FP-80A FP-64B FP-100 FP-64A
		FPG Ceramic	FG-80
Multi-function type	EPROM on the package type	Ceramic	DC-64SP DC-42P

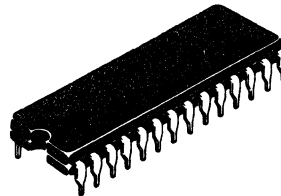
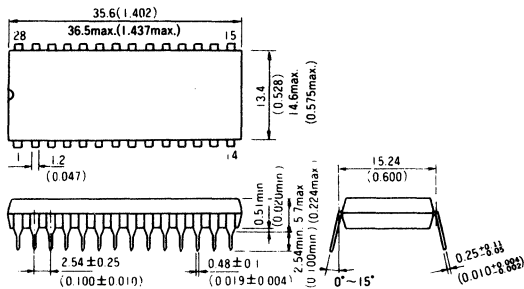
Introduction of Packages

Plastic DIP

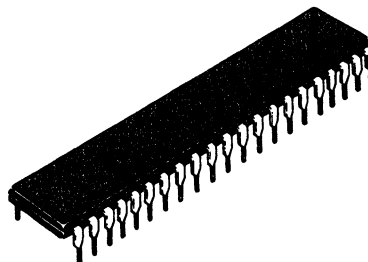
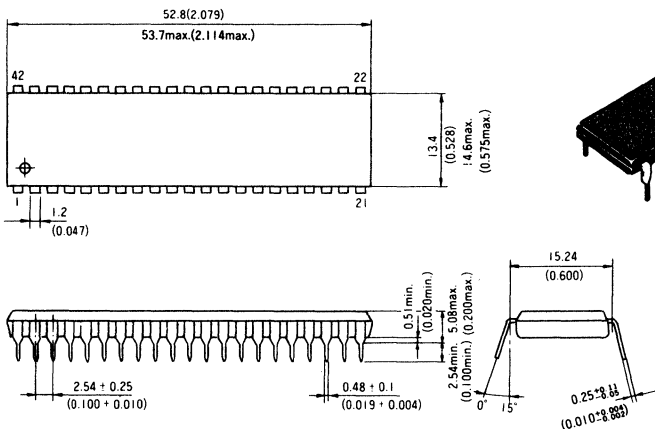
Unit : mm (inch)

Scale : 1/1

DP-28



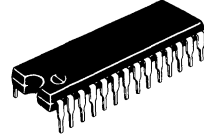
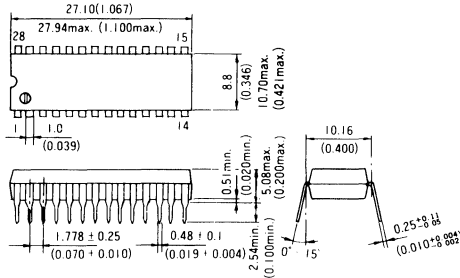
DP-42



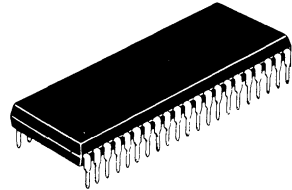
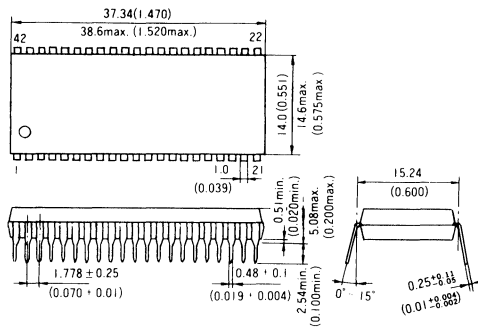
Shrink Type Plastic DIP

Unit : mm (inch)
Scale : 1/1

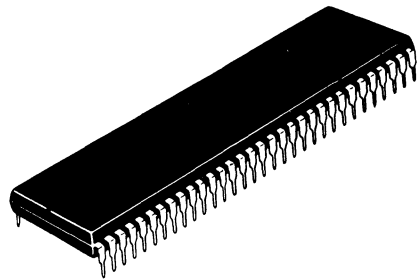
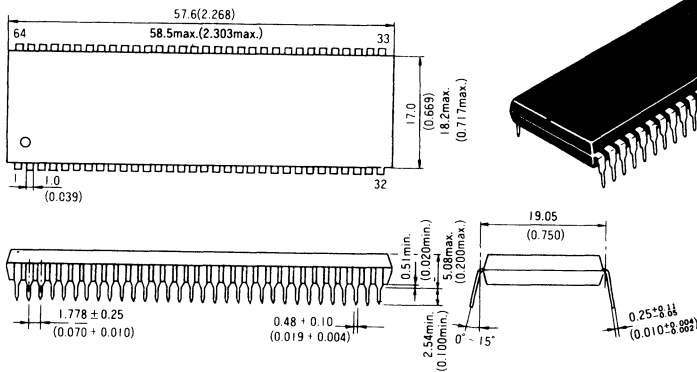
DP-28S



DP-42S



DP-64S

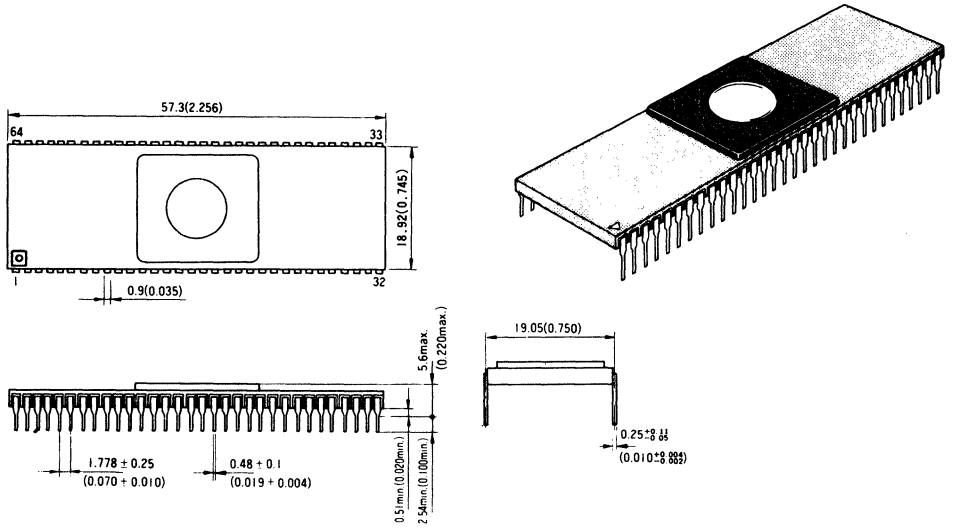


Introduction of Packages

Shrink Type Ceramic DIP

Unit : mm (inch)
Scale : 1/1

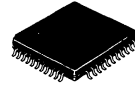
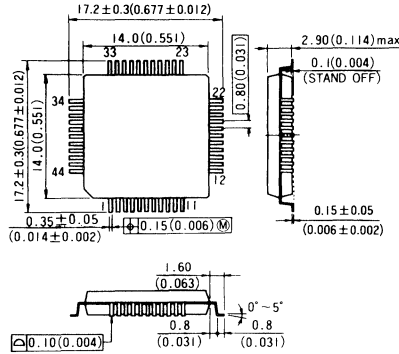
DC-64S



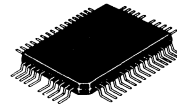
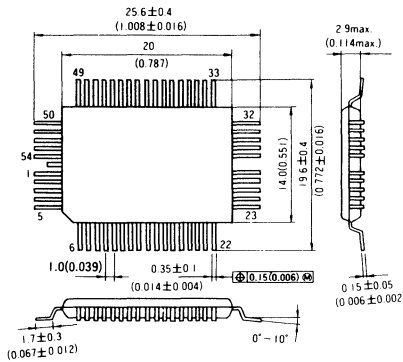
Flat Plastic Package

Unit : mm (inch)
Scale : 3/2

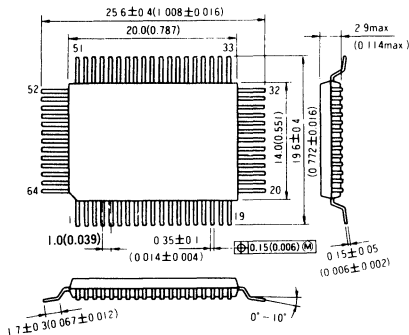
FP-44A



FP-54

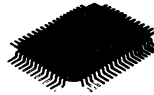
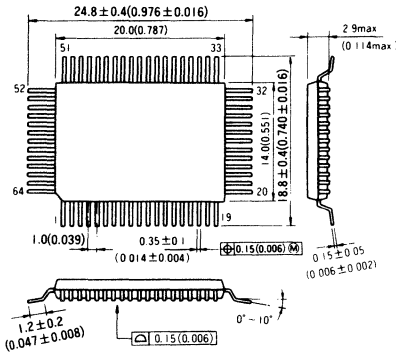


FP-64

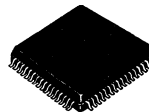
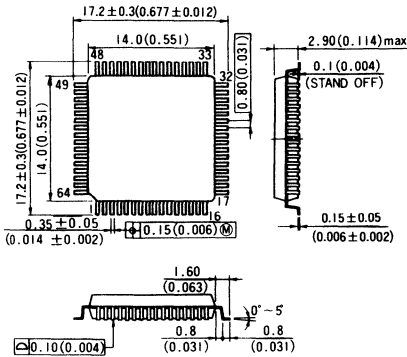


Introduction of Packages

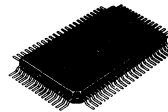
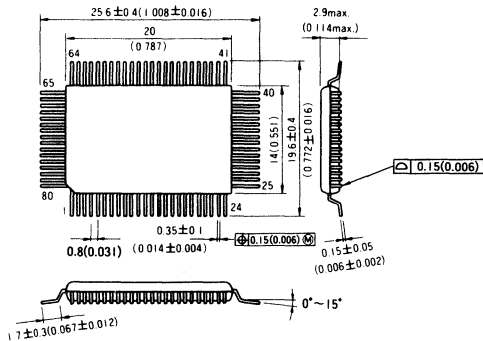
FP-64B



FP-64A



FP-80

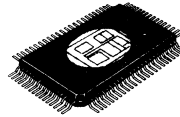
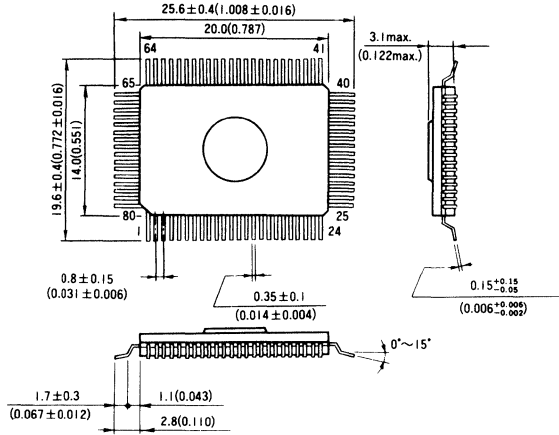


Introduction of Packages

Flat Ceramic Package

Unit : mm (inch)
Scale : 3/2

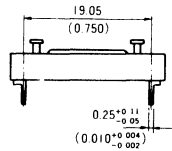
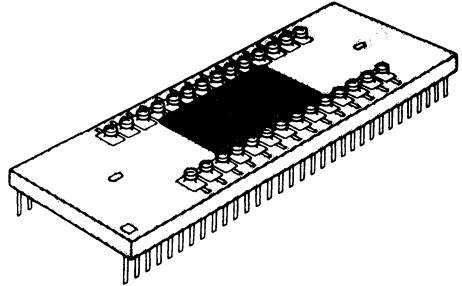
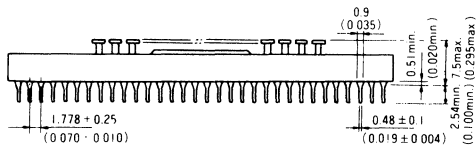
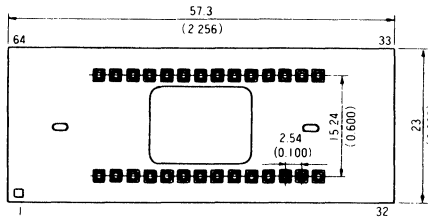
FG-80



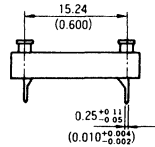
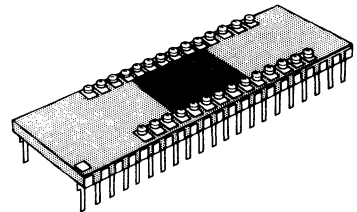
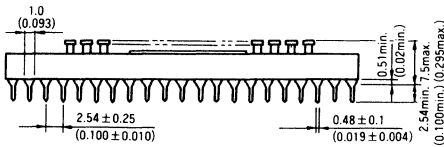
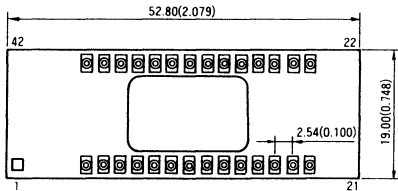
EPROM on the package

Unit : mm (inch)
Scale : 3/2

DC-64SP



DC-42P



Reliability and Quality Assurance

1. Views on Quality and Reliability

Basic views on quality in Hitachi are to meet individual user's purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize such quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality.

In addition, quality required by users on semiconductor devices is going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

- (1) Build the reliability in design at the stage of new product development.
- (2) Build the quality at the sources of manufacturing process.
- (3) Execute the harder inspection and reliability confirmation of final products.
- (4) Make quality level higher with field data feed back.
- (5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely study and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Vehicle

Test vehicle is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Vehicle are as follows:

- Making clear about fundamental failure mode
- Analysis of relation between failure mode and manufacturing process condition
- Search for failure mechanism analysis
- Establishment of QC point in manufacturing

2. Effectiveness of evaluation by Test Vehicle are as follows;

- Common fundamental failure mode and failure mechanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.



- Easy to run tests.
- etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

- (1) Description of the products based on specified design documents.
- (2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.
- (3) Determine contents of reliability and methods, etc. based on design document and drawing.
- (4) Check process ability of manufacturing line to achieve design goal.
- (5) Discussion about preparation for production.
- (6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
- (7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

- (1) Problems in individual process should be solved in the process. Therefore, at final product stage, the potential failure factors have been already removed.
- (2) Feedback of information should be made to ensure satisfied level of process ability.
- (3) To assure reliability required as a result of the things mentioned above is the

purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

- (1) The third party performs approval objectively from the standpoint of customers.
- (2) Fully consider past failure experiences and information from field.
- (3) Approval is needed for design change and work change.
- (4) Intensive approval is executed on parts material and process.
- (5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Fig. 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, Key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

Reliability and Quality Assurance

The other activities of quality assurance are as follows:

- (1) Outside Vendor Technical Information Meeting
- (2) Approval on outside vendors, and guidance of outside vendors
- (3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments, circumstances and sub-materials. The quality control in the manufacturing process is shown in Fig. 3 corresponding to the manufacturing process.

- (1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor

devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed — rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of countermeasures

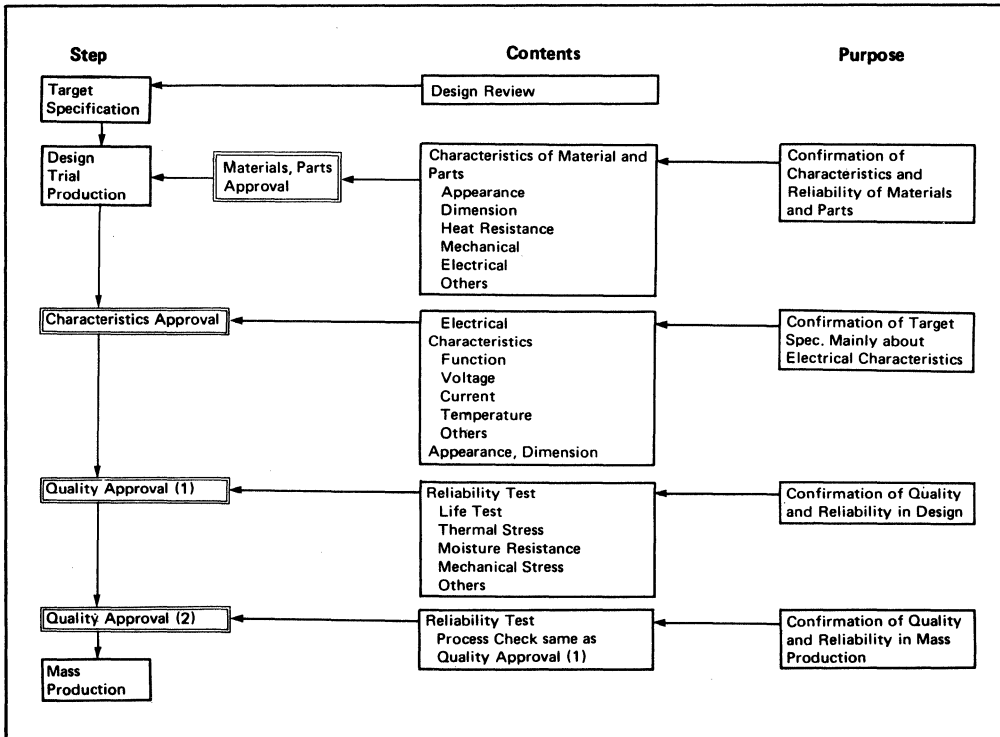


Figure 1. Flow Chart of Quality Approval



- Transmission of information about quality
- (2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of

manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and

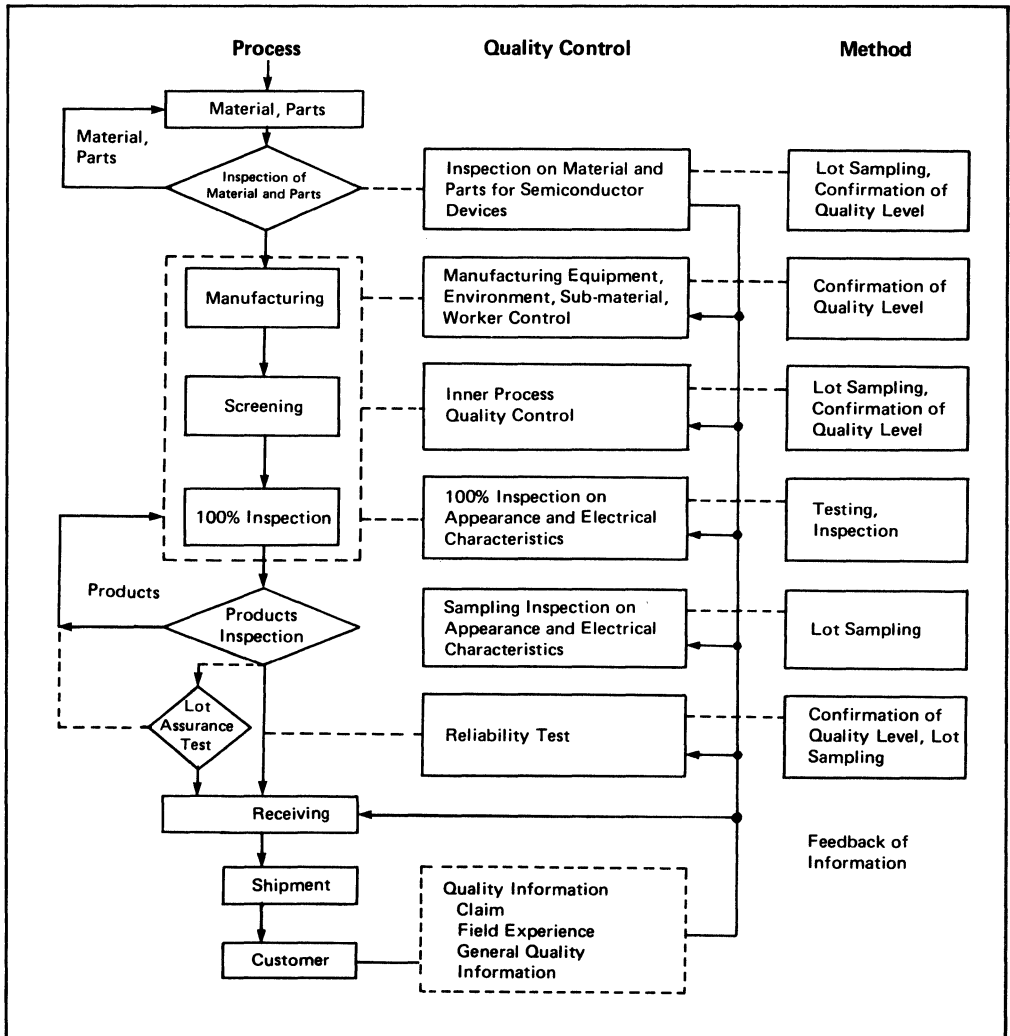


Figure 2. Flow Chart of Quality Control in Manufacturing Process



Reliability and Quality Assurance

maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Submaterials.

Quality and reliability of semiconductor device is highly affected by manufacturing process. Therefore, the controls of manufac-

turing circumstances — temperature, humidity, dust — and the control of submaterials — gas, pure water — used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings,

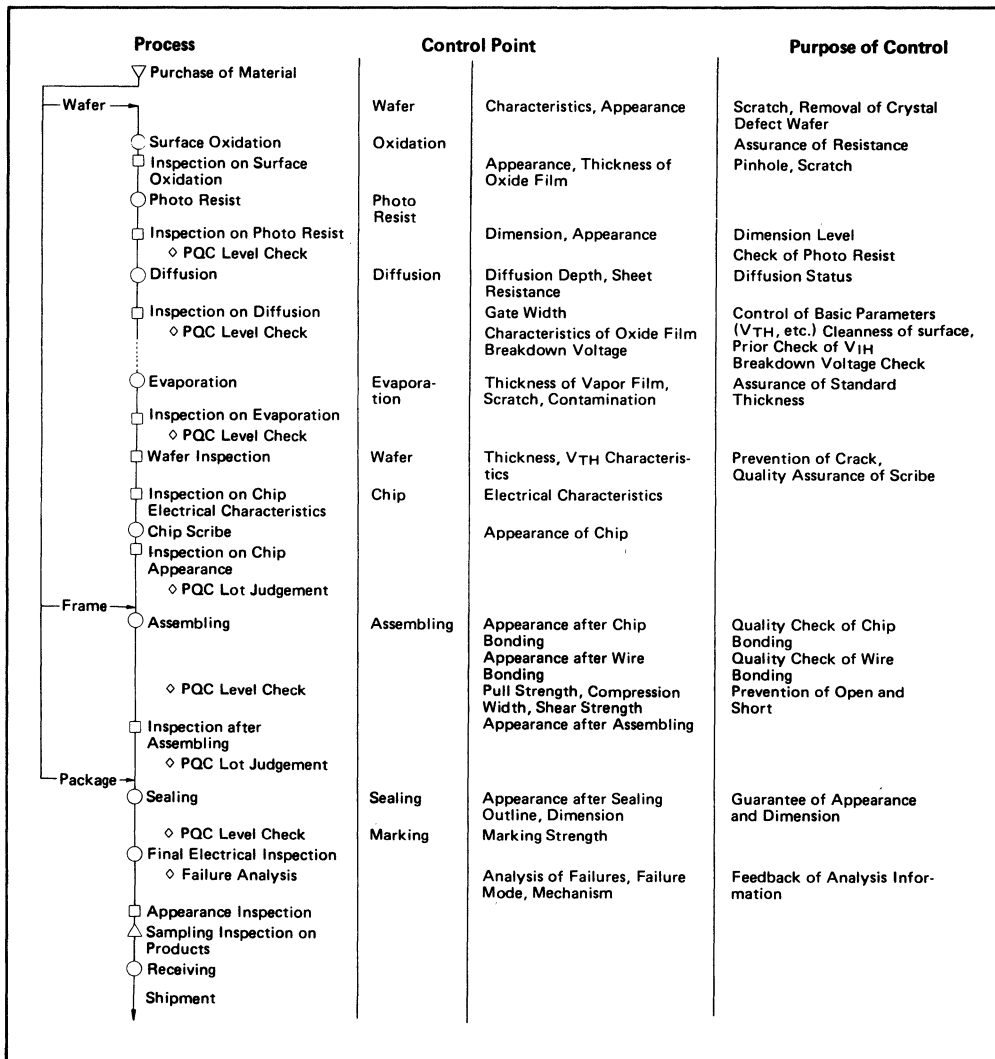


Figure 3. Example of Inner Process Quality Control



facilities, airconditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1. Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density Crystal Axis	Defect Numbers
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Restoration Gradation	Uniformity of Gradation.
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension Purity Elongation Ratio	Purity Level Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension Processing Accuracy Plating	Dimension Level
	Mounting Characteristics	Bondability, Solderability Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics Electrical Characteristics Mechanical	Heat Resistance
	Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding	Molding Performance
	Performance Mounting Characteristics	Mounting Characteristics

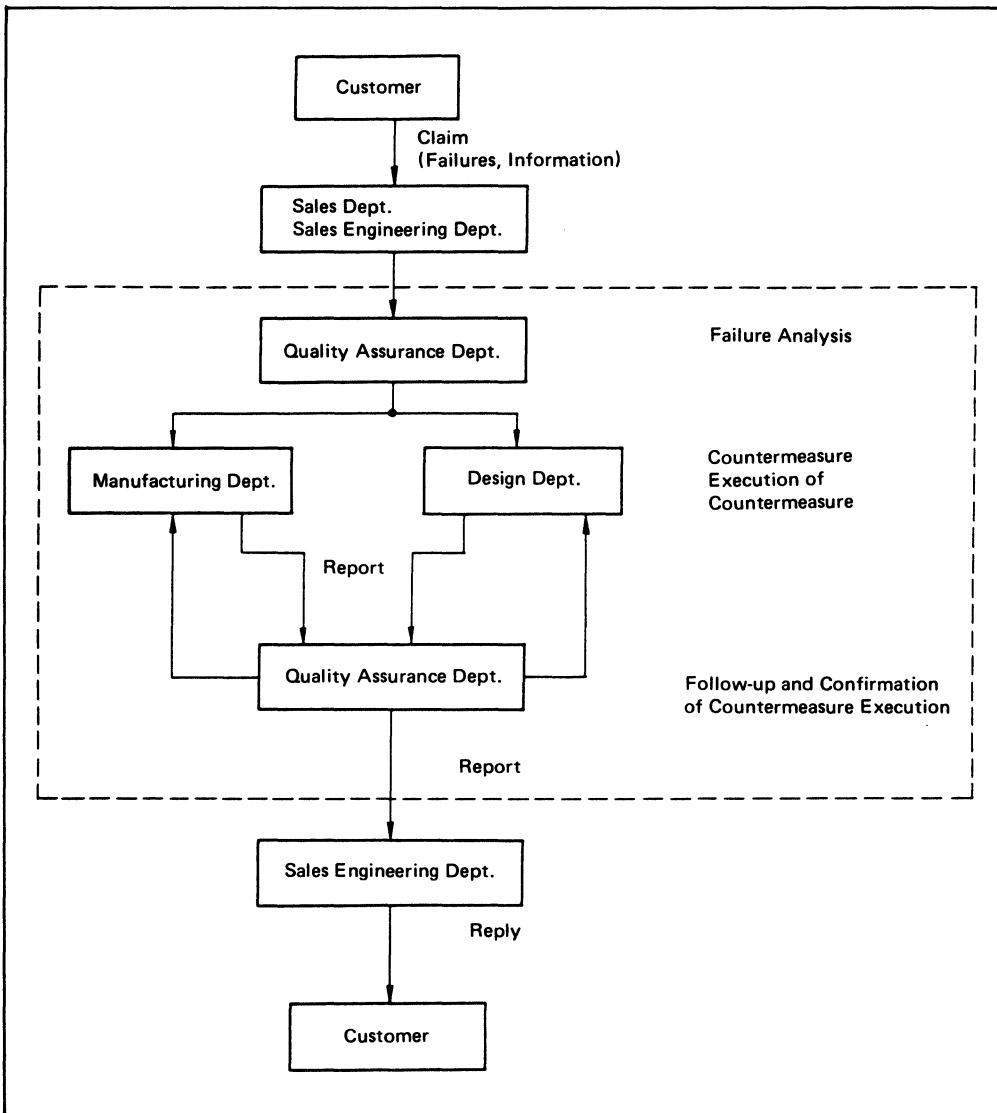


Figure 4. Process Flow Chart of Field Failure

Reliability Test Data of Microcomputer

1. Introduction

Microcomputer is required to provide higher reliability and quality with increasing function, enlarging scale and widening application. To meet this demand, Hitachi is improving the quality by evaluating reliability, building up quality in process, strengthening inspection and analyzing field data etc..

This chapter describes reliability and quality assurance data for Hitachi 4-bit single-chip microcomputer based on test and failure analysis results. More detail data and new information will be reported in another reliability data sheet.

2. Package and Chip Structure

2.1 Package

The reliability of plastic molded type has been greatly improved, recently their appli-

cations have been expanded to automobiles measuring and control systems, and computer terminal equipment operated under relatively severe conditions and production output and application of plastic molded type will continue to increase.

To meet such requirements, Hitachi has considerably improved moisture resistance, operation stability, and chip and plastic manufacturing process.

Plastic package type structure is shown in Figure 1 and Table 1.

2.2 Chip Structure

Hitachi 4-bit single-chip microcomputer are produced in PMOS E/D technology or low power CMOS technology. Si-gate process is used in both types because of high reliability

Table 1. Package Material and Properties

Item	Plastic DIP	Plastic Flat Package
Package	Epoxy	Epoxy
Lead	Solder dipping Alloy 42	Solder plating Alloy 42
Die bond	Au-Si or Ag paste	Au-Si or Ag paste
Wire bond	Thermo compression	Thermo compression
Wire	Au	Au

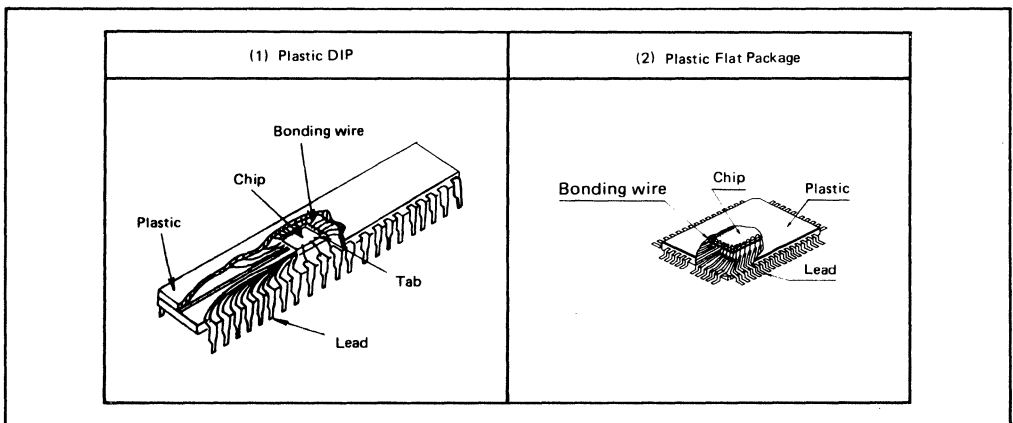


Figure 1. Package Structure

Reliability Test Data of Microcomputer

and high density.

Chip structure and basic circuit are shown in Figure 2.

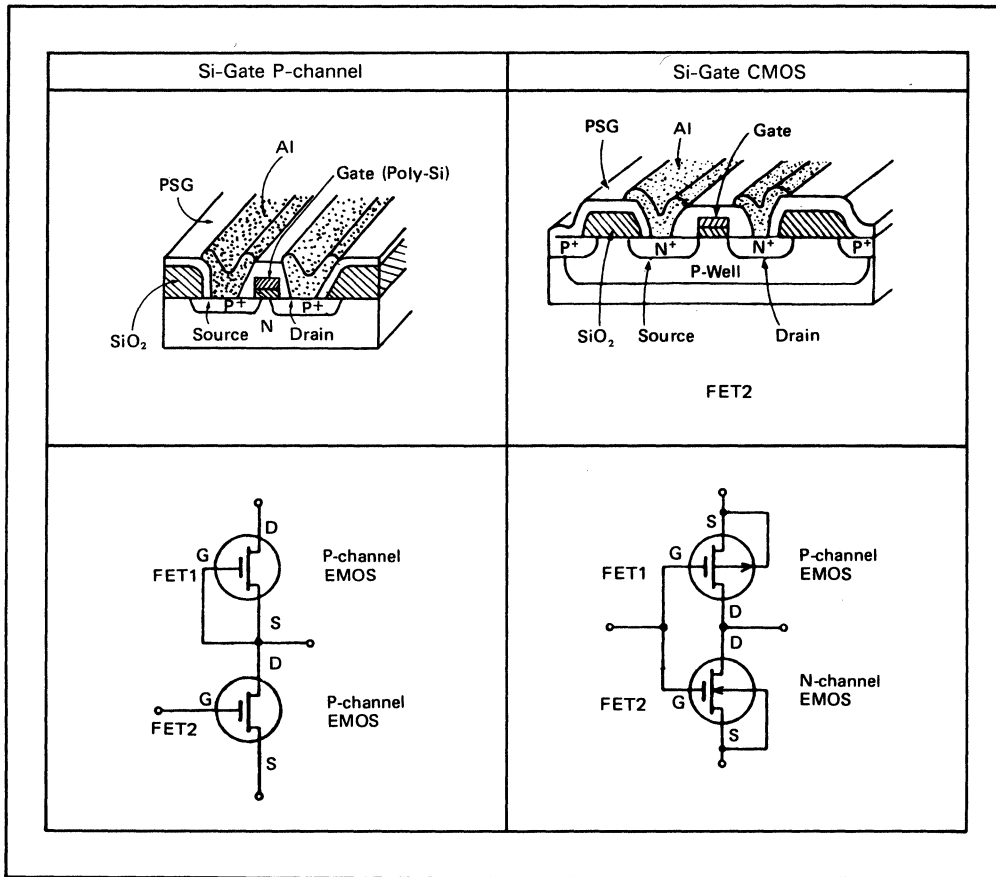


Figure 2. Chip Structure and Basic Circuit

3. Quality Qualification and Evaluation

3.1 Reliability Test Methods

Reliability test methods shown in Table 2 are used to qualify and evaluate the new products and new process.

Table 2. Reliability Test Methods

Test Items	Test Condition	MIL-STD-883 B Method No.
Operating Life Test	125°C, 1000hr	1005,2
High Temp, Storage	Tstg max, 1000hr	1008, 1
Low Temp, Storage	Tstg min, 1000hr	
Steady State Humidity	65°C 95%RH, 1000hr	
Steady State Humidity Biased	85°C 85%RH, 1000hr	
Temperature Cycling	-55°C~150°C, 10 cycles	1010,4
Temperature Cycling	-20°C~125°C, 200 cycles	
Thermal Shock	0°C~100°C, 100 cycles	1011,3
Soldering Heat	260°C, 10 sec	
Mechanical Shock	1500G 0.5 msec, 3 times/X, Y, Z	2002,2
Vibration Fatigue	60Hz 20G, 32hrs/X, Y, Z	2005,1
Variable Frequency	20~2000Hz 20G, 4min/X, Y, Z	2007,1
Constant Acceleration	2000G, 1 min/X, Y, Z	2001,2
Lead Integrity (DIP)	225gr, 90° 3 times	2004,3
Lead Integrity (QFP)	225gr, 90° 1 time	2004

Reliability Test Data of Microcomputer

3.2 Reliability Test Results

Reliability Test Result of 4-bit single-chip microcomputer device is shown in Table 3 to

Table 14, There is little difference according to device series, as the design and production process, etc. are standardized.

3.2.1 HMCS40 Series (HMCS40 Series)

Table 3. Dynamic Life Test

(1) PMOS

(Condition; $-V_{DD}=11V$, $-V_{disp}=50V$, $T_a=125^\circ C$)

Device Type	Package	Sample Size	Component Hours	Failure
HMCS47A	DP-64S	45	45000	0
	FP-54	45	45000	0
HMCS45A	DP-64S	90	90000	0
	FP-54	405	405000	2*
HMCS44A	DP-42	313	313000	1**
	DP-42S	45	45000	0
HMCS43	DP-42	116	116000	0
	DP-42S	45	45000	0
HMCS42	DP-28	106	106000	0
Total		1210	1210000	3

* Surface contamination

** Aluminum metallization open

(2) CMOS

(Condition; $V_{CC}=5.5V$, $T_a=125^\circ C$)

Device Type	Package	Sample Size	Component Hours	Failure
HMCS47C	DP-64S	90	90000	0
	FP-54	90	90000	0
HMCS46C	DP-42	90	90000	0
	DP-42S	45	45000	0
HMCS45C	DP-64S	45	45000	0
	FP-54	120	120000	1*
HMCS44C	DP-42	162	162000	1**
	DP-42S	45	45000	0
HMCS43C	DP-42	120	120000	0
	FP-54	90	90000	0
HMCS42C	DP-28	60	60000	0
	DP-28S	45	45000	0
LCD-III	FP-80	90	90000	0
LCD-IV	FP-80	90	90000	0
Total		1182	1182000	2

* Surface contamination

** Aluminum metallization open

Estimated Failure Rate=0.018%/1000 hrs at $T_a=75^\circ C$ for PMOS

0.014%/1000 hrs at $T_a=75^\circ C$ for CMOS

(Activation Energy 0.7eV, Confidence Level 60%)

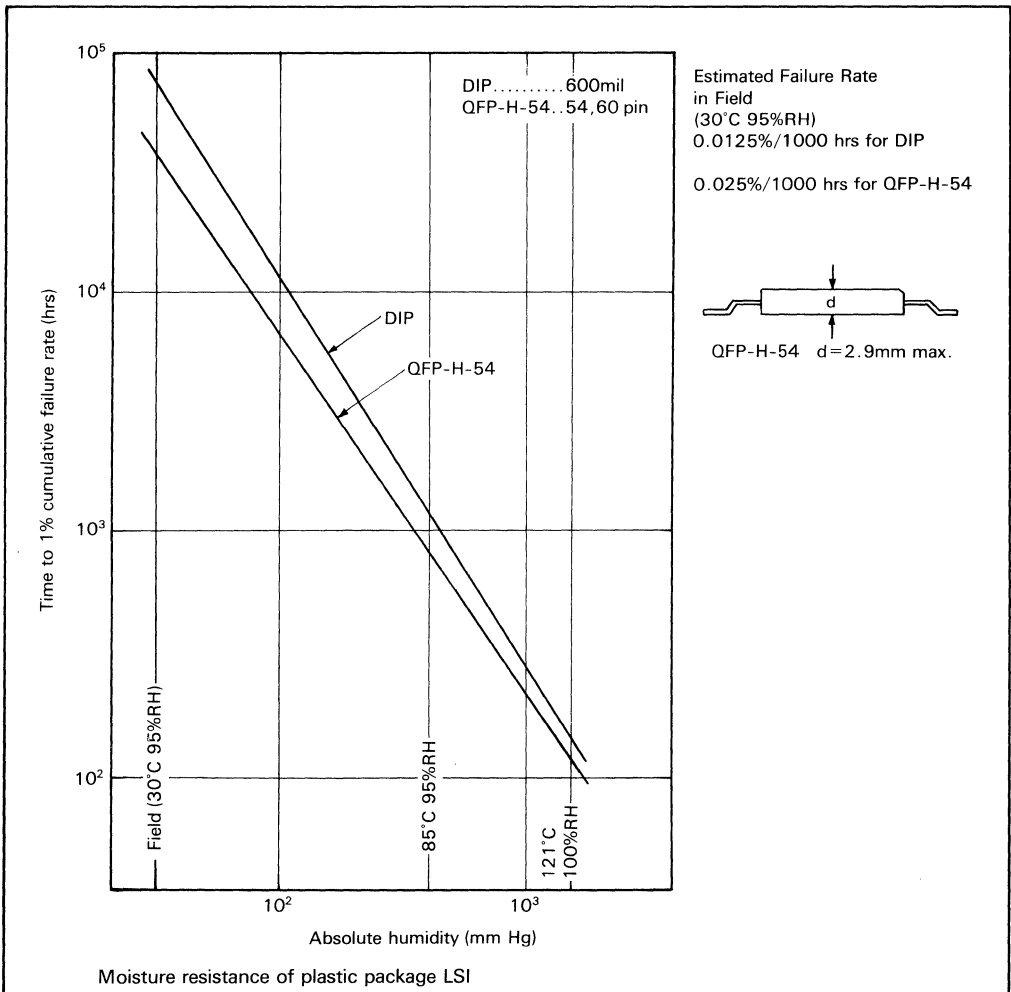


Reliability Test Data of Microcomputer

Table 4. Moisture Resistance

Test Item	Condition	Plastic Package Type			
		DIP		QFP	
		Sample	Failure	Sample	Failure
High Temp. High Humidity	65°C 95%RH, 1000hrs	870	1	545	1
Storage	85°C 95%RH, 1000hrs	220	1	165	1
High Temp. High Humidity Bias	85°C 85%RH, 1000hrs	205	1	185	1
Pressure Cooker Test	121°C 2 atm, 96hrs	55	0	55	0

Failure mode : Aluminum corrosion 6 pcs.



Reliability Test Data of Microcomputer

Table 5. Mechanical and Environmental Test Results

Test Item	Test Condition	DIP Type		QFP Type	
		Sample	Failure	Sample	Failure
High Temperature Storage	Ta = 150°C, 1000hrs	43	0	53	0
Low Temperature Storage	Ta = -55°C, 1000hrs	50	0	40	0
Temperature Cycling	-55°C~25°C~150°C 10 cycles	1637	0	1514	0
Thermal Shock	0°C~100°C 10 cycles	150	0	100	0
Soldering Heat	260°C, 10 sec	140	0	160	0
Solderability	230°C, 5 sec	34	0	34	0
Mechanical Shock	1500G, 0.5 msec 3 times/X, Y, Z	45	0	45	0
Vibration	60 Hz, 20G	120	0	45	0
Fatigue	32 hrs/X, Y, Z				

3.2.2 HMCS400 Series

Table 6. Dynamic Life Test (HMCS400 Series)

(Condition : V_{CC} = 6.0V, T_a = 125°C)

Device Type	Package	Sample Size	Component Hours	Failure
HMCS404	DIP	55	55,000	0
	QFP	77	77,000	0
HMCS408	DIP	78	78,000	0
	QFP	55	55,000	0
HMCS412	DIP	55	55,000	0
	QFP	32	16,000	0
HMCS414	DIP	55	55,000	0
	QFP	32	32,000	0
HMCS424	DIP	55	55,000	0

Reliability Test Data of Microcomputer

Table 7. Moisture Resistance (HMCS400 Series)

(1) High Temp. High Humidity Storage

Device Type	Package	Condition	168 hrs.	500 hrs.	1000 hrs.
HMCS404	DIP	65°C 95%RH	0/176	0/176	0/176
	QFP	65°C 95%RH	0/176	0/176	0/176*
HMCS408	DIP	65°C 95%RH	0/45	0/45	0/45
	DIP	85°C 95%RH	0/45	0/45	0/45
	QFP	65°C 95%RH	0/116	0/116	0/116
	QFP	85°C 95%RH	0/70	0/70	0/70
HMCS412	QFP	65°C 95%RH	0/50	0/50	0/50
	QFP	85°C 95%RH	0/50	0/50	0/50

* Aluminum Corrosion

(2) Pressure Cooker Test
(Condition : 121°C, 2 atm.)

Device Type	Package	40 hrs.	60 hrs.	100 hrs.
HMCS404	DIP	0/45	0/45	0/45
	QFP	0/45	0/45	0/45
HMCS408	DIP	0/22	0/22	0/22
	QFP	0/45	0/45	0/45
HMCS412	QFP	0/45	0/45	0/45

(3) High Temp. High Humidity Bias
(Condition : 85°C, 85%RH, V_{CC}=5.5V)

Device Type	Package	168 hrs.	500 hrs.	1000 hrs.
HMCS404	DIP	0/32	0/32	0/32
	QFP	0/22	0/22	0/22
HMCS414	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22

Reliability Test Data of Microcomputer

Table 8. Temperature Cycling (HMCS400 Series)

Device Type	Package	10 cycles	100 cycles	200 cycles
HMCS404	DIP	0/295	0/90	0/90
	QFP	0/210	0/45	0/45
HMCS408	DIP	0/90	0/45	0/45
	QFP	0/45	0/45	0/45
HMCS412	DIP	0/287	0/77	0/77
	QFP	0/45	0/45	0/45
HMCS414	DIP	0/77	0/77	0/77
	QFP	0/45	0/45	0/45
HMCS424	DIP	0/45	0/45	0/45

Table 9. High Temp. Low Temp. Storage (HMCS400 Series)

(1) High Temp. Storage (Condition : 150°C)

Device Type	Package	168 hrs.	500 hrs.	1000 hrs.
HMCS404	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HMCS408	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HMCS414	DIP	0/22	0/22	0/22

(2) Low Temp. Storage (Condition : -55°C)

Device Type	Package	168 hrs.	500 hrs.	1000 hrs.
HMCS404	QFP	0/22	0/22	0/22
HMCS408	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HMCS414	DIP	0/22	0/22	0/22

Reliability Test Data of Microcomputer

3.2.3 4-bit ZTAT

Table 10. Dynamic Life Test (ZTAT)

(Condition : $V_{CC}=6.0V$, $T_a=125^{\circ}C$)

Device Type	Package	Sample Size	Component Hours	Failures
HD4074008	DIP (ceramic)	55	55,000	0
	DIP	55	55,000	0
HD4074408	DIP (ceramic)	55	55,000	0
	DIP	100	100,000	0
	QEP	32	32,000	0

Table 11. Moisture Resistance (ZTAT)

(1) High Temp. High Humidity Storage

Device Type	Package	Condition	168 hrs.	500 hrs.	1000 hrs.
HD4074008	DIP	65°C 95%RH	0/77	0/77	0/77
		QFP	0/55	0/55	0/55
		85°C 95%RH	0/49	0/49	0/49
HD4074408	DIP	65°C 95%RH	0/116	0/116	0/116
		QFP	0/45	0/45	0/45
		85°C 95%RH	0/26	0/26	0/26

(2) Pressure Cooker Test
(Condition : 121°C, 2 atm.)

Device Type	Package	40 hrs.	60 hrs.	100 hrs.
HD4074008	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074408	DIP	0/45	0/45	0/45
	QFP	0/22	0/22	0/22

Table 12. Temperature Cycling (ZTAT)

(Condition : $-55^{\circ}C \sim 150^{\circ}C$)

Device Type	Package	10 cycles	100 cycles	200 cycles
HD4074008	DIP	0/150	0/45	0/45
	QFP	0/100	0/45	0/45
HD4074408	DIP	0/120	0/45	0/45
	QFP	0/130	0/45	0/45



Reliability Test Data of Microcomputer

Table 13. High Temp. Low Temp. Storage (ZTAT)

(1) High Temp. Storage
(Condition : 150°C)

Device Type	Package	48 hrs.	168 hrs.	500 hrs.	1000 hrs.
HD4074008	DIP (ceramic)	0/221	0/35	0/35	0/35
	DIP	0/79	0/79	0/79	0/79
	QFP	0/189	0/45	0/45	0/45
HD4074408	DIP (ceramic)	0/255	0/104	0/104	0/104
	DIP	0/260	0/44	0/44	0/44
	QFP	0/103	0/32	0/32	0/32

(2) Low Temp. Storage
(Condition : -55°C)

Device Type	Package	168 hrs.	500 hrs.	1000 hrs.
HD4074008	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22
HD4074408	DIP	0/22	0/22	0/22
	QFP	0/22	0/22	0/22

Table 14. Mechanical and Environment Test Results (HMCS400 Series)

Test Item	Condition	DIP		QFP	
		Samples	Failures	Samples	Failures
Thermal Shock	0°C~100°C, 10 cycles	210	0	150	0
Soldering Heat	260°C, 10 sec	246	0	86	0
Solderability	230°C, 5 sec, Rosin flux	132	0	88	0
Salt Water Spray	35°C, NaCl 5%, 24 hrs.	110	0	66	0
Drop Test	75cm, maple board 3 times	44	0	40	0
Lead Integrity	Stretching, 250g, 30 sec.	60	0	40	0
	Banding, 225g, 90°, 3 times	160	0	22	0



4. Precaution

4.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and appearance, or breakage.

- (1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.
- (2) Store in a clean air environment, free from dust and active gas.
- (3) Store in a container which does not induce static electricity.
- (4) Store without any physical load.
- (5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.
- (6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.
- (7) Take care not to allow condensation during storage due to rapid temperature changes.

4.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

- (1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
- (2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.
- (3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being elec-

trically charged by applying some surface treatment.

- (4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

4.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchrosopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge or foreign matter exists before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

4.4 Soldering

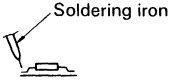
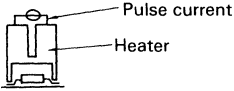
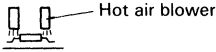
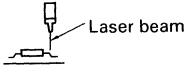
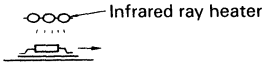
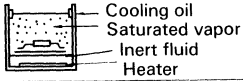

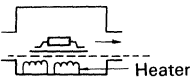
4.4.1 Methods and Standard Conditions for Soldering

Table 15 lists the major methods for soldering surface mount packages. The methods can be grouped into two broad categories: partial heat application methods whereby the outer leads are heated, and overall heat application methods by which the PCB assembly including the packages, are heated.

The standard conditions with brief descriptions of each method are given in 4.4.1.1 and 4.4.1.2. When selecting the best method, consider all advantages and disadvantages. Refer to the recommended method in 4.4.2 for each particular package type.

Reliability Test Data of Microcomputer

Table 15. Methods for Soldering Surface Mount Packages

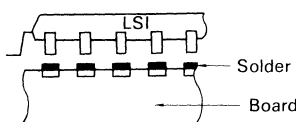
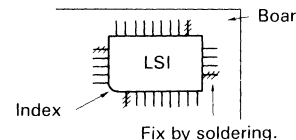
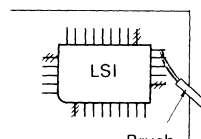
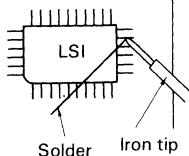
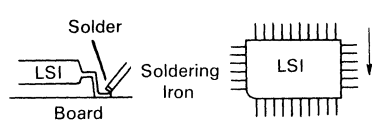
	Method Name	Setup	Reference
Partial Heat Application Methods	Manual soldering	 Soldering iron	4.2.1
	Pulse heater solder soldering	 Pulse current Heater	
	Hot air soldering	 Hot air blower	
	Laser soldering	 Laser beam	
Overall Heat Application Methods	Infrared reflow soldering	 Infrared ray heater	4.2.2
	Vapor phase reflow soldering	 Cooling oil Saturated vapor Inert fluid Heater	
	Dip soldering	 Wave solder (solder vessel for surface mounting)	
	Furnace soldering	 Heater	

4.4.1.1 Partial Heat Application Methods

Manual Soldering: A package is fixed to the predetermined position with flux or adhesive. With the package held in place, the leads are soldered. A pointed tip iron at 350°C is used with solder in narrow wire form

typically 0.5 Mm or less in diameter. Soldering time should be three seconds or less per pin. Table 16 shows typical processes for soldering an QFP.

Table 16. Typical Processes for QFP Soldering

Process	Procedure
<p style="text-align: center;">Presoldering</p> 	<ol style="list-style-type: none"> 1. Solder-sip the footprint on the board. 2. Remove all bridges developed in dipping.
<p style="text-align: center;">Positioning and temporary fixing</p> 	<ol style="list-style-type: none"> 1. Align the index markings. 2. Place a package on the footprint. 3. Check that the leads on four sides have been placed accurately on the footprint. 4. Fix four corners of the package by soldering. Any bridges between leads may be left as they are.
<p style="text-align: center;">Flux application</p> 	<ol style="list-style-type: none"> 1. Using a brush, apply flux (rosin-based) to the leads and pattern. 2. Put a small quantity of flux into a container for use in each short session of flux application (approx. 4 hours). 3. At the end of each applying session, discard all the flux left in the container. Do not mix residual with replenished flux.
<p style="text-align: center;">Soldering</p> 	<ol style="list-style-type: none"> 1. Move the soldering iron across leads while melting the solder.  <p style="text-align: center;">Move soldering iron this way.</p>

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Pulse Heater Soldering: (source: Textbook for Internepcon JAPAN Seminar No 10, Jan. 26, 1985). A pulse current is allowed to flow in a heater chip (collet). As Joule heat develops and flows in the chip, a prepared solder piece is melted instantaneously and pressed onto the required position by the chip. This method is noted for a minimum rise in temperature of

the entire package, but may not be suitable for mass production. It is suited for packages with their leads extending outward (gull-wing type), but not for those with leads bent inward (J-bend leads). Figure 13 shows typically structures of heater chips, and Table 17 lists representative conditions for pulse heater soldering.

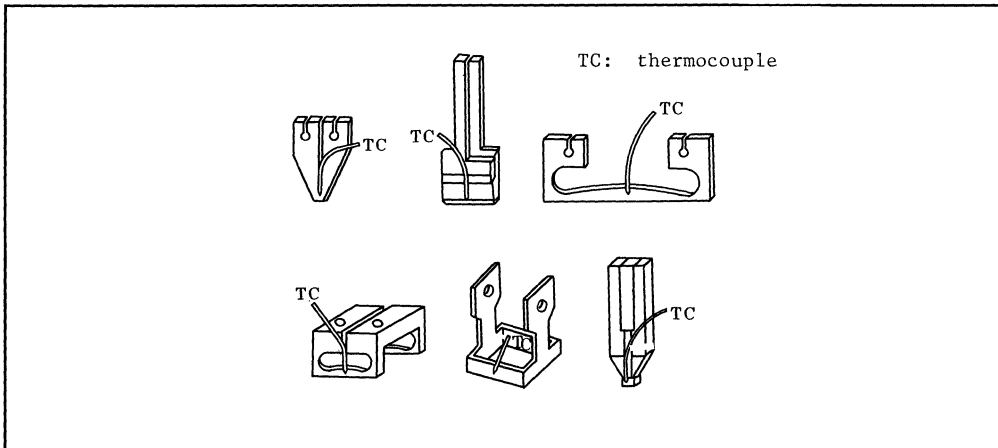


Figure 3. Typical Heater Chip Structures

Table 17. Typical Conditions for Pulse Heater Soldering

Item	Condition
Heating temperature	100-260°C
Heating Time	5-10 sec.
Cooling Time	5-10 sec.
Soldering Pressure	8-28 kg*
Stroke	50 mm

*: From a compressed-air source of 4 kg/cm²

Hot Air Soldering: Air or nitrogen gas is heated, and hot blasts are applied through a nozzle to melt-solder devices in place. This method requires gas at high flow rates because gas as a heat medium has low

thermal conductivity and heat capacity. It is difficult to apply hot air under stabilized conditions. Figure 4 sketches a hot air soldering setup, and table 18 lists typical conditions for hot air soldering.

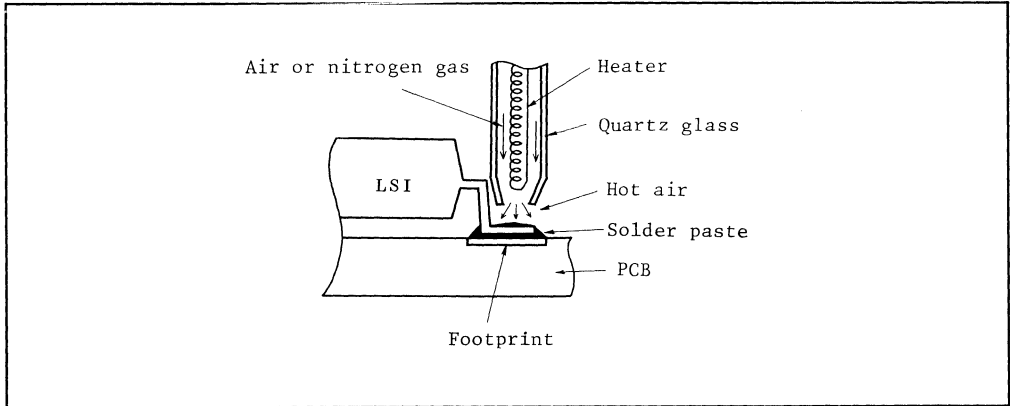


Figure 4. Setup for Hot Air Soldering

Table 18. Typical Conditions for Hot Air Soldering

Item	Condition
Hot Air temperature	230–260°C
Air Flow Rate	25–30 l/min.
Soldering Time*	3–10 s
Cooling Time	5–10 s

*: Duration of hot air application

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Laser Soldering: (source: Textbook for Internepon JAPAN Seminar No. 10, Jan. 26, 1985) A laser beam is applied to the target position to melt solder. Laser sources include a ruby type, YAG (yttrium aluminum garnet) type, glass-fixed laser, and CO₂ (carbon dioxide gas) laser. Currently, CO₂ and YAG lasers are used. Table 19 compares the characteristics of the two laser types. The YAG laser may be more suitable than the

CO₂ type since it provides higher heat exchange effectiveness over the metal surface to be soldered and a lower absorption factor for the board than the CO₂ laser.

Figure 5 illustrates a typical YAG laser soldering arrangement. The YAG laser output in continuous oscillation is from 50 W to 600 W depending on the lamp capacity and the volume of YAG crystal.

Table 19. Comparing the CO₂ Laser and YAG Laser Characteristics

	Polyimide Substrate	Tin-lead Solder	Initial Investment	Laser Efficiency
CO ₂ Laser (10.6 μm)	2% in reflection factor (98% in absorption factor)	74% in reflection factor (26% in absorption factor)	1	20-25%
YAG Laser (1.06 μm)	27% in reflection factor (73% in absorption factor)	21% in reflection factor (79% in absorption factor)	2	1%

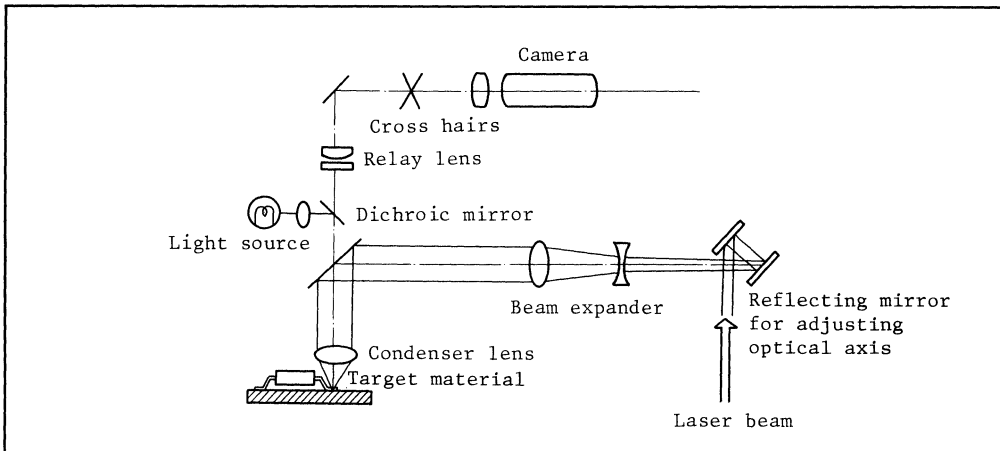


Figure 5. Typical YAG Laser Soldering Arrangement

4.4.1.2 Overall Heat Application Methods

Infrared Reflow Soldering: The infrared ray from a halogen lamp is condensed by a reflecting mirror into a hot beam for soldering. Because both point and line ray sources can be used, this method allows a large number of packages to be soldered at the same time. It is therefore suitable for mass production.

Infrared rays are divided into three groups: far infrared radiation ($\gamma = 5.6\text{--}1000\ \mu\text{m}$), intermediate infrared radiation ($\gamma = 1.5\text{--}5.6\ \mu\text{m}$) and near infrared radiation ($\gamma\ 0.7\text{--}1.5\ \mu\text{m}$). In many infrared ray reflow soldering setups, the preliminary heater emits far infrared (or intermediate) rays infrared and the main heater releases near infrared (or immediate) rays.

Reflow conditions vary with the package shape, board configuration and soldering equipment. Figure 6 shows an example of infrared ray reflow soldering conditions for IC/LSI packages. The temperature measurement point in infrared reflow soldering varies depending on the package type and application chip. At Hitachi, the criteria for determining the position are set forth as follows:

- For temperature measurement on the package surface, the measuring position is a MOS package that incorporates a relatively large chip.
- For measurement on the board or lead surfaces, the measuring position is a bipolar package that incorporates a relatively small chip.
- Where MOS and bipolar packages coexist, the temperature is to be measured on MOS package surfaces.

Since plastic molded surface mount packages are black, the portion exposed to infrared rays readily absorbs heat, boosting the temperature of that portion higher than that of the leads. This problem is bypassed by two measures: cooling the package during reflowing, or placing a white metal reflector on the surface of the package to subdue the energy absorption and created a lower temperature inside the package. Figure 7 illustrates a typical temperature profile when a reflector is used.

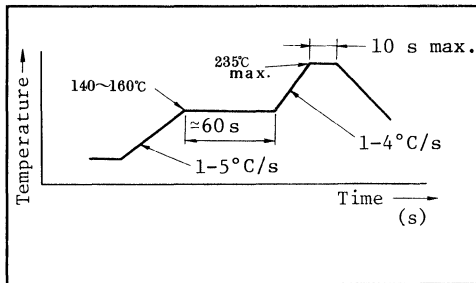


Figure 6. Typical Conditions for Infrared Reflow Soldering

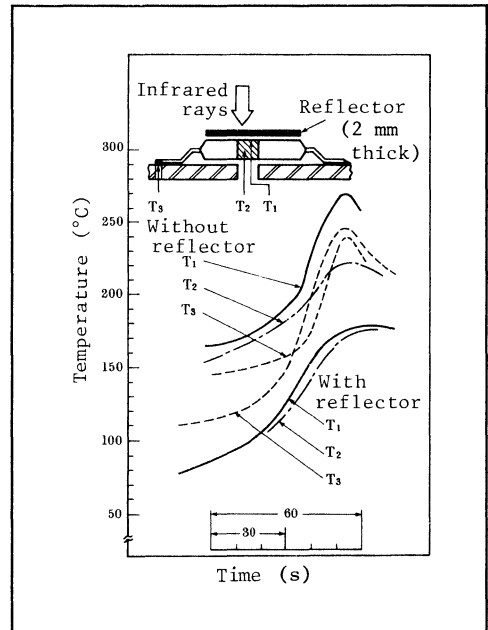


Figure 7. Typical Temperature Profile with Reflector Used

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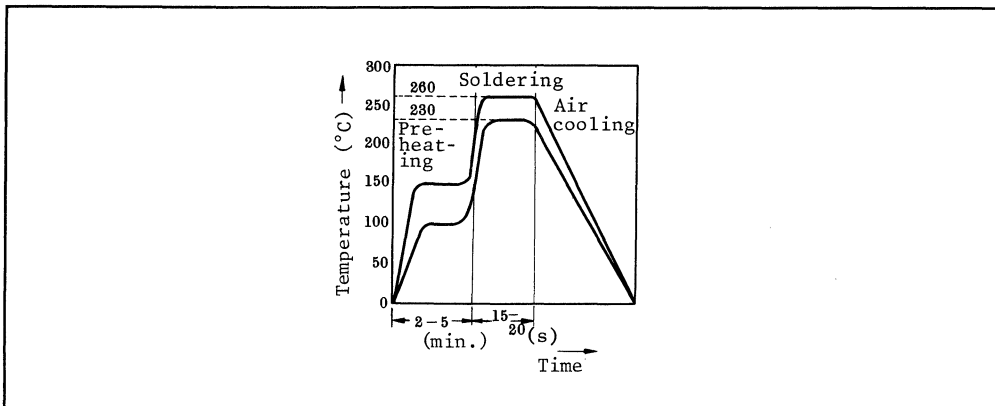


Figure 8. Example of Temperature Profile

Table 20. Typical Reflow Conditions

Item	CMPAK, MPAK, MPAK-4, FPAK, UPAK	DPAK
Soldering Temperature (board temperature)	230–260°C (reference solder melting point + 50°C)	220°C max.
Soldering Time	15–20 sec.	40 s. max.
Preheating Temperature	100–150°C	160°C
Preheating Time	2–5 min.	5 min.

Vapor Phase Reflow Soldering: A special high boiling point solvent (for example fluorocarbon type) is heated to generate a vapor layer. As the entire board is passed through the layer, the latent heat of vaporation causes the solder to reflow. This method offers the following advantages:

- The temperature can be kept constant. Since the solvent vapor is used, the reflow temperature is determined by the boiling point of the solvent to eliminate the likelihood of overheating.
- Damage to components and boards can be avoided due to virtually uniform thermal conduction regardless of the configuration of the solderable assemblies.

- Numerous components of different shapes can be subjected to simultaneous reflow soldering. The use of solvent vapor permits reflow soldering at multiple positions simultaneously that eliminate most constraints from different component shapes. This feature applies particularly to J-bend type devices whose leads are partially located under the package.
- The inert reflow atmosphere prevents solder oxidation or flux baking. Any residual flux can be readily removed by conventional techniques.

Figure 9 shows typical conditions for vapor phase reflow soldering.

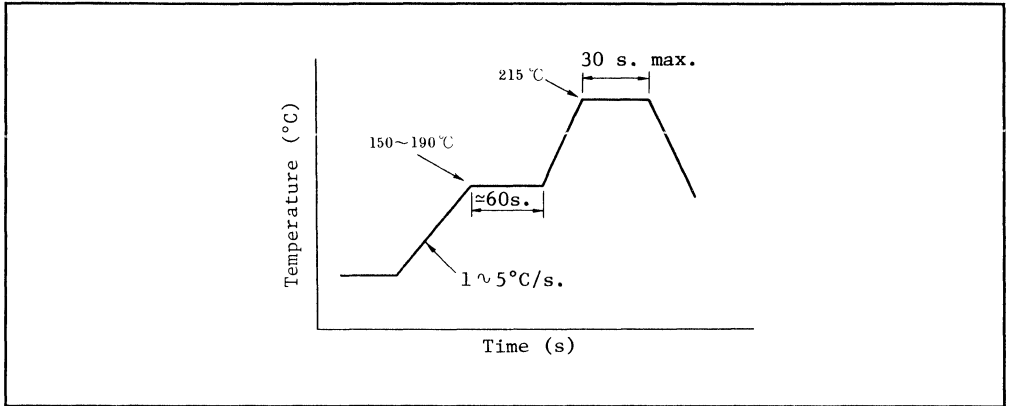


Figure 9. Typical Conditions for Vapor Phase Reflow Soldering

Table 21. Properties of Solvents for Vapor Phase Reflow Soldering (source: manufacturers catalogs)

Product Name	FC-70	FC 5311	GALDEN LS230	GALDEN HS260
Manufacturer	3M (U.S.A.)	ISC Chemical (UK)	Montefluos S.P.A. (Italy)	Montefluos S.P.A. (Italy)
Distributor	Sumitomo 3M	Sumitomo 3M	Montedison Japan	Montedison Japan
Molecular Formula	(C ₅ F ₁₁) ₃ N Tributylamine		CF ₃ -(O-CF ₂) _n -(O-CF ₂) _m -OCF ₃ Perfluoralkyl-polyether	
Molecular Weight	820	624	800	900
Boiling Point (°C)	215	215	220-235	250-265
Specific Gravity (g/ml)	1.94	2.03	1.824	1.840
Vapor Pressure (mmHg)	<0.1	<0.1	5 × 10 ⁻³	5 × 10 ⁻⁴
Specific Heat (cal/°C.g)	0.25	0.25	0.24	0.24
Thermal Conductivity (cal/g.°C.s)	1.6 × 10 ⁻⁴	1.26 × 10 ⁻⁴	1.67 × 10 ⁻⁴	1.67 × 10 ⁻⁴
Surface Tension (dyne/cm)	18	19	18	18
PFIB Generation	Less than 5 ppm in solvent, less than 0.03 ppm at opening	< 1 ppb	< 0.5 ppb	< 0.5 ppb

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Figure 10 sketches two types of vapor phase reflow soldering equipment (in-line and batch type), and table 9 lists the properties of solvents available for vapor phase reflow soldering. The in-line type is suited for mass production, and the batch type for low or medium production as well as for research and development purposes. Both types need adequate ventilation during operation. Consult the equipment manufacturer, material vendor and appropriate occupational operating standards for ventilation requirements.

Dip Soldering: A package is fixed temporarily on the board by adhesive. With the component side facing

downward, the package is passed through molten solder. Figure 11 depicts the process flow for dip-soldering 18- and 28-pin MSPs. Compared with reflow methods, this method exerts extremely high thermal stress on semiconductor chips. Adverse effects from the stress should be avoided by providing a preheating zone to soften thermal shock and minimizing the soldering time. Figure 12 shows a typical temperature profile for dip soldering.

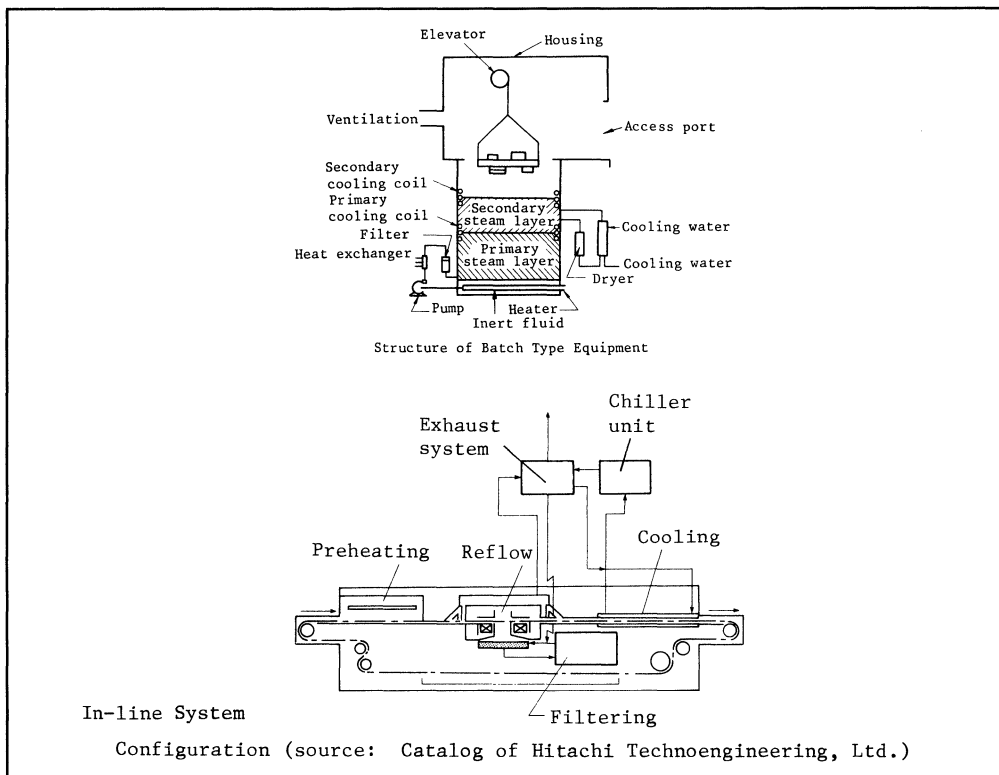


Figure 10. Vapor Phase Reflow System

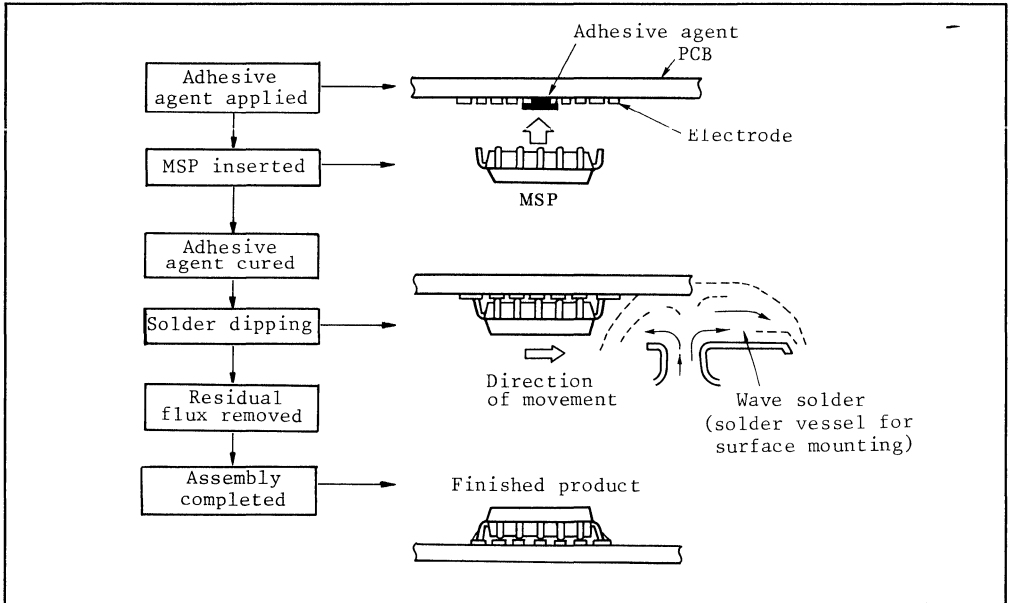


Figure 11. Flow of Process for Solder-Dipping 18- and 28-Pin MSPs

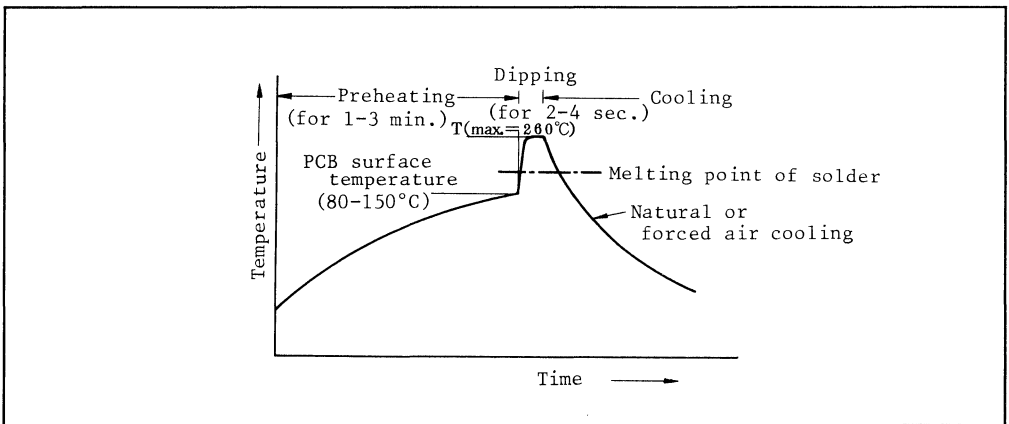


Figure 12. Temperature Profile of Solder-Dipped Soldering

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Furnace Soldering: (source: technical information from Senju Metal Co.) The PCB is placed on a thin heat resistant belt. As the PCB advances, the belt is heated from below by hot plates to reflow the solder. This method provides high processing capacity, and the equipment required is relatively inexpensive. This

method, however, is not suitable for boards with low resistance to heat, poor thermal conductivity or complicated shapes. Figure 13 outlines a typical furnace soldering setup, and Figure 14 depicts a typical temperature profile of this method.

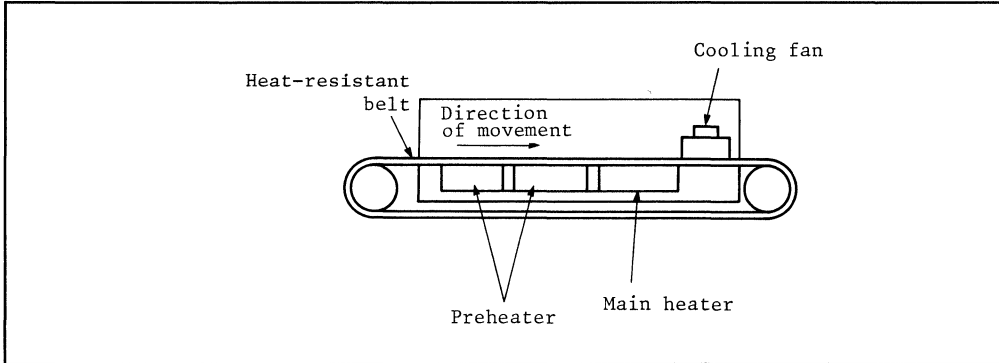


Figure 13. Furnace Soldering Setup

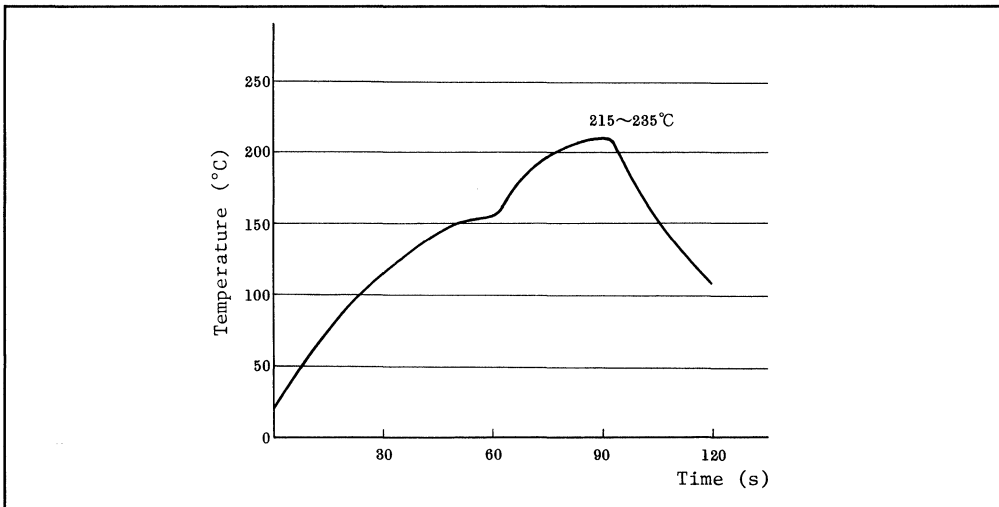


Figure 14. Typical Temperature Profile of Furnace Soldering

4.4.2 Recommended Mounting Methods for Each Package Type

Table 22 lists the recommended mounting methods for each of the package types now on the market.

When determining conditions for the mounting method selected, refer to the temperature profile examples in 4.2 and the notes in 4.4. The symbols used in the table have the following meanings:

○ (suitable): Use this method by considering the temperature profile inside the package, temperature rise gradient, change in soldering conditions, and solderability.

× (unsuitable): Do not use this method.

The soldering methods are divided into the three groups above with emphasis placed on thermal stress on components and solderability. Productivity and the costs also be analyzed.

Notice that methods are recommended for each package type. Where different package types coexist, select the soldering method suitable for the package type most vulnerable to thermal stress.

Table 22. Recommended Mounting Methods for Each Package

Mounting Methods	IC/LSI Packages						Discrete Packages					
	QFP (plastic)	SOP	MSP	PLCC/SOJ	QFP (ceramic)	LCC	MPAK	UPAK	FPAK	DPAK	LLD	SRP
Partial Heat Application Methods	Manual Soldering	○	○	○	○	○	×	○	○	○	○	○
	Pulse Heater Soldering	○	○	×	×	○	×	○	○	○	○	○
	Hot Air Soldering	○	○	○	○	○	○	○	○	○	○	○
	Laser Soldering	○	○	○	○	○	×	○	○	○	○	○
Overall Heat Application Methods	Infrared Reflow Soldering	○	○	○	○	○	○	○	○	○	○	○
	Vapor Phase Reflow Soldering	○	○	○	○	○	○	○	○	○	○	○
	Dip-soldering	×	Note 1	Note 2	×	×	×	○	○	○	×	Note 3
	Furnace Soldering	○	○	○	○	○	○	○	○	○	○	○

- Notes:
1. Recommended for SOPs with 20 pins or less, but unsuitable for SOPs with 24 or 28 pins.
 2. Recommended, or possible for MSPs with 44 or more pins.
 3. Methods indicated as unsuitable may apply depending on the specific product. For more information, consult your Hitachi representative.
 4. (○ : Suitable; × : Unsuitable)

4.5 Removing Residual Flux

To ensure the reliability of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If chloric detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures will cause swollen chip coating due to solvent

permeation, select the type of detergent and cleaning condition carefully. Lotus Solvent and Dyfron Solvent are recommended as a detergent. Do not use any trichloroethylene solvent. For ultrasonic cleaning, the following conditions are advisable:

- Frequency: 28 to 29 kHz (to avoid device resonance)
- Ultrasonic output: 15W/l
- Keep the devices out of direct contact with the power generator.
- Cleaning time: Less than 30 seconds

ZTAT MCU On-Chip PROM Characteristics and Precautions

Principles of Programming/Erasing: The ZTAT micros' memory cells are the same as an EPROM's. Therefore they are programmed by applying high voltage to control gates and drains, which injects hot electrons into the floating gate. They are stable, surrounded by an energy barrier of SiO_2 film. Such a cell becomes a 0 bit due to the memory threshold voltage change. A cell with no condensed electrons at its floating gate appears as a 1 bit (figure 15).

The electron charge in memory cells may

decrease as time goes by. This can be caused by:

- Ultraviolet light: discharged by photo-emitted electrons (erasure principle)
- Heat: discharged by thermal emitted electrons
- High voltage: discharged by a high electric field at the control gate or drain

If the oxide film covering a floating gate is defective, the erasure rate is great. Normally, electron erasure does not occur, because such defective devices are found and removed during testing.

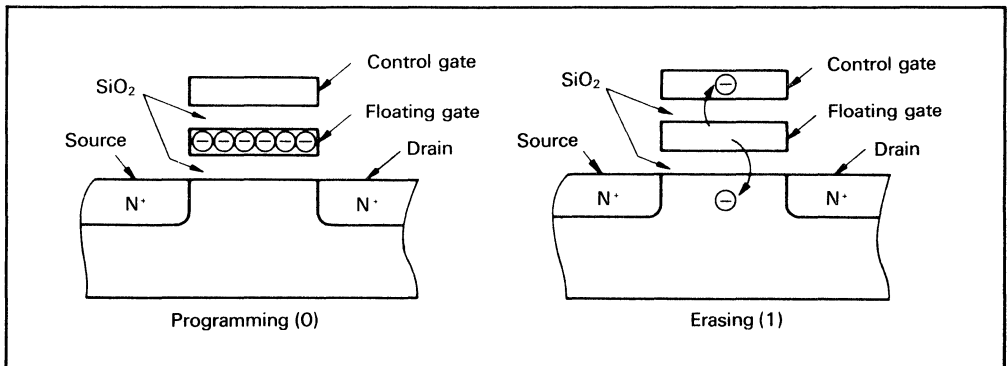


Figure 15. Cross-section of EPROM Memory Cell

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Programming Precautions: The EPROM memory cells should be programmed under specific voltage and timing conditions. The higher the program voltage and the longer the program pulse is applied, the more electrons will be injected into the floating gate. However, if an overvoltage is applied to V_{PP} , the p-n junction may be permanently damaged. Pay particular attention to PROM programmer overshoot. Negative voltage noise will cause a parasitic transistor effect, which may reduce break-down voltage.

The ZTAT micros are connected electrically to the PROM programmer through a socket adapter. Therefore, pay attention to the following:

- Confirm that the socket adapter is firmly fixed on the PROM programmer.

- Do not touch the socket adapter or the LSI during programming.

- Misprogramming can be caused by poor contacts.

On-Chip EPROM Reliability after Programming: Generally, semiconductors are reliable except for initial failures. Parts can be screened to avoid failures. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold characteristics are high. Exposing the LSI to 150°C after user programming can effectively upgrade these characteristics. Figure 16 shows the recommended screening flow.

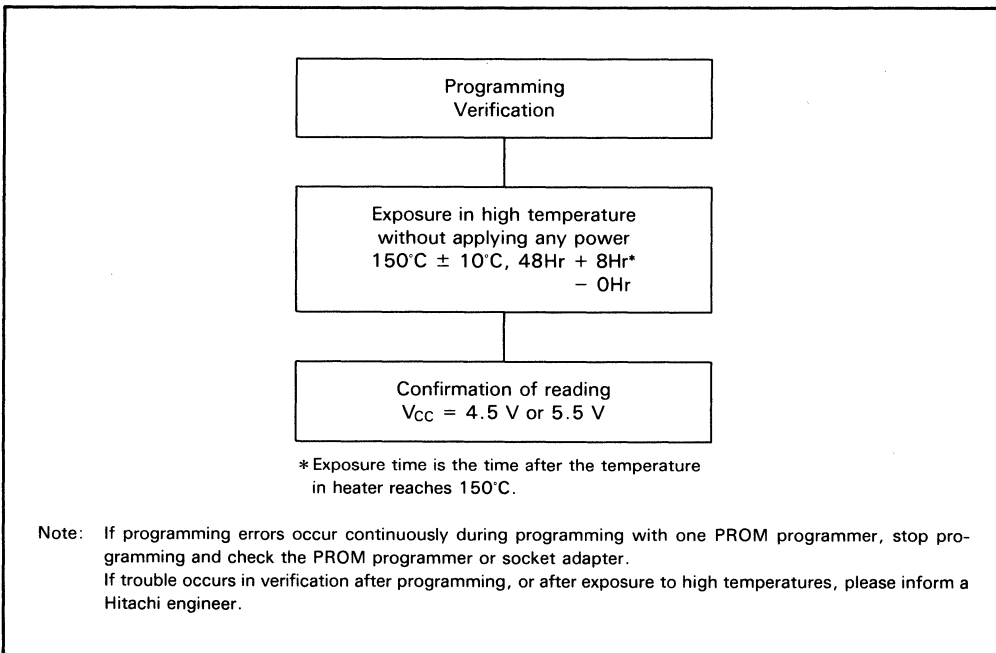


Figure 16. Recommended Screening Flow

Program Development Procedure and Support Systems

1. General Description

The cross assembler and the hardware emulator using various types of computers are prepared by Hitachi as supporting systems to develop the user's programs. User programs are mask programmed into the ROM and shipped as LSI by Hitachi. Figure 1

shows the typical program design procedure and Table 1 shows the system development support tools for HMCS 40 and HMCS 400 series microcomputers which are used in these processes.

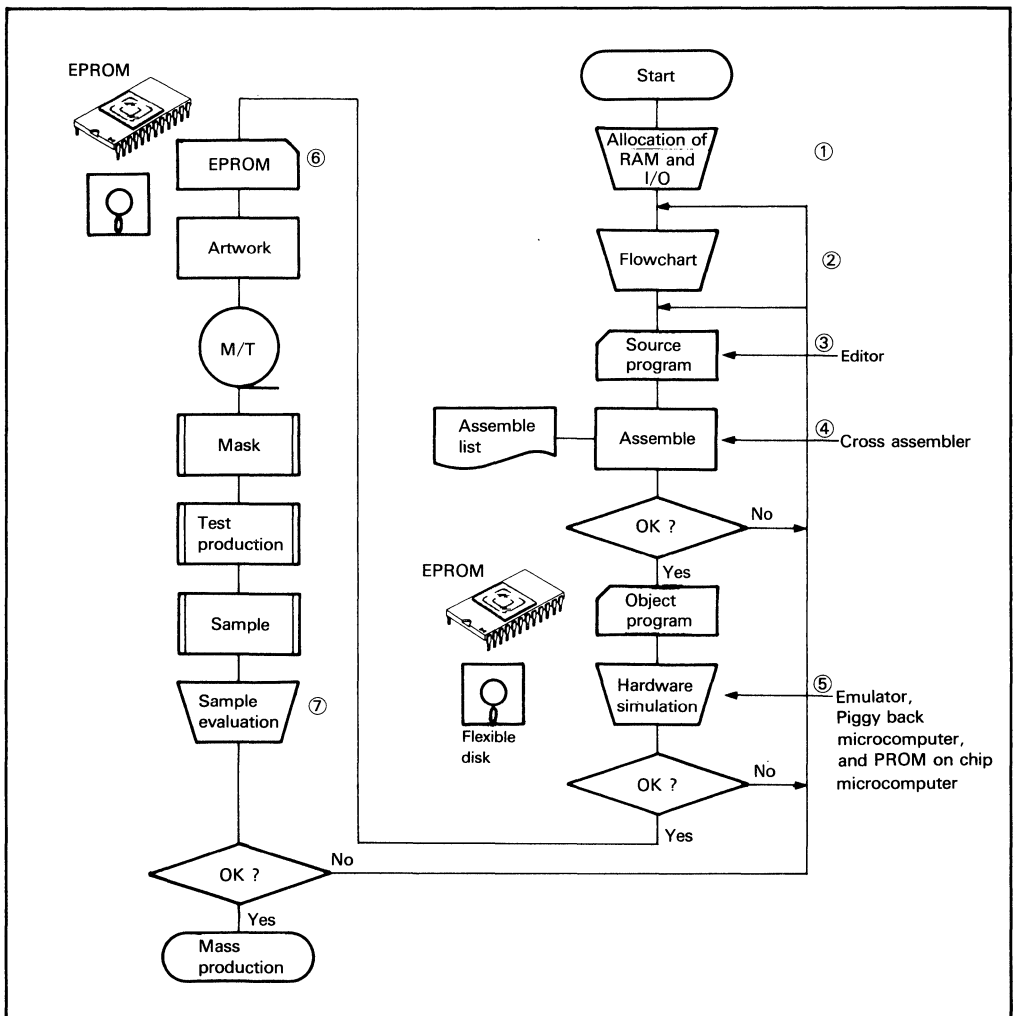


Figure 1. Program Design Procedure



Program Development Procedure and Support Systems

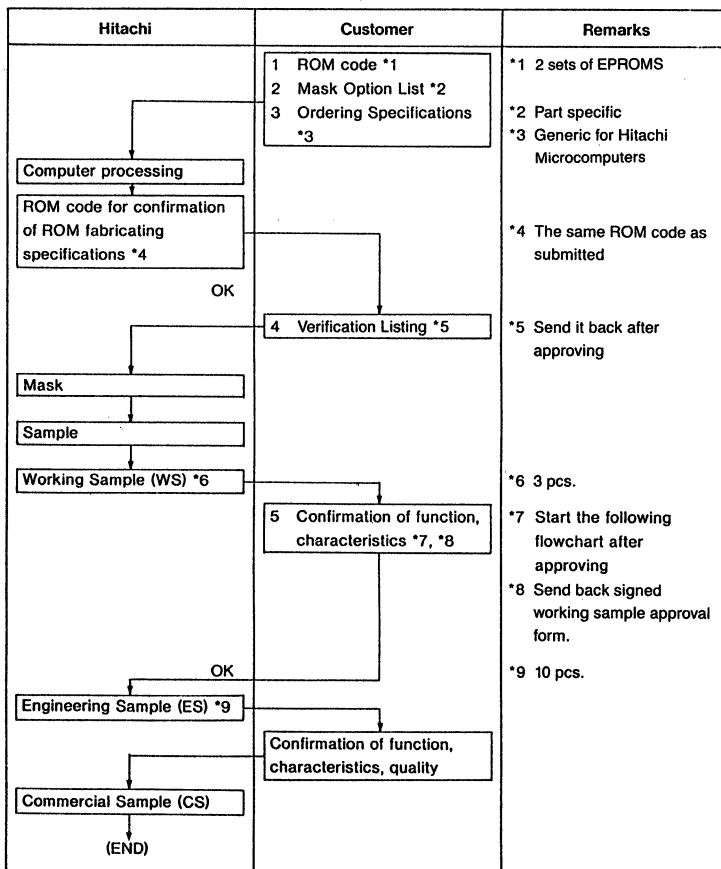
(Description)

- ① When the user programs the system, pre-determined functions are assigned to the I/O pins and the RAM area is estimated before actual programming.
- ② A flowchart is designed to achieve the predetermined functions.
- ③ The coded flowchart is written onto floppy disk using HMCS 400 series mnemonic code to make a source program.
- ④ The source program is assembled using host computer to generate the object program. Errors during the assembling are also detected.
- ⑤ Hardware emulation is performed to check the program. Hitachi provides the emulator, which may be connected to host computers such as an IBM PC, for debugging, as well as the piggyback microcomputer and EPROM on chip microcomputers to verify the program.
- ⑥ The completed program is sent to Hitachi in the form of EPROMs along with the appropriate "Ordering Specifications", "Marking Option", and "Mask Option List" documents.
- ⑦ The ROM and mask options are masked by the company, LSI is tentatively produced and the sample is handed to the user. After the user has evaluated the sample and confirmed that the program is correct, mass production can be started.

Development Flowchart

Single chip microcomputer device is developed according to the following flowchart after program development.

Device Development Flowchart



Note: Please send in 1, 2, and 3 at ROM ordering, and send back 4, 5 after approving.



Table 1. Support tools for HMCS400 Series, LCD III, and LCD IV

Description	Part No.	HMCS402/404 408/412/424/ HD4074408	HD404019 HD4074019	HD404302 HD4074308*	HD4074408 HD4044418 HD4074418	HD404508* HD4074509*	HD404608 HD4074608	HD404678 HD4074678*	HD404708 HD404709 HD4074709	HD404808 HD4074808 HD404L4808 HD407L4808	HD404918 HD404919	LCD III (HD44790) (HD44795)	LCD IV (HD613901)
Emulator	H400CMIX2 ⁽¹⁾ (HS408EML02H) ⁽¹⁾	•											
	HS440EML01H ⁽¹⁾				•								
	HS40LEMLD01H ⁽¹⁾											•	•
Emulator unit	HS400EUA01H ⁽¹⁾		•	•		•		•	•	•			
Target probe	*HS409ETA01H ⁽²⁾		•										
	*HS430ETA01H ⁽²⁾			•									
	*HS450ETA01H ⁽²⁾					•							
	HS460ETA01H ⁽²⁾						•						
	*HS467ETA01H ⁽²⁾							•					
	HS470ETA01H ⁽²⁾								•				
	HS480ETA01H ⁽²⁾									•			
	*HS491ETA01H ⁽²⁾										•		
User system interface cable	HS400ECA80H		•			•	•	•	•	•			
	*HS430ECD42H			•							•		
	*HS470ECS84H		•						•				
Programming Socket Adapter	HS408ESS11H ⁽³⁾	•											
	HS408ESF01H ⁽⁴⁾	•											
	HS408ESF03H ⁽⁵⁾	•											
	HS409ESS11H ⁽³⁾												
	*HS409ESF01H ⁽⁴⁾		•										
	*HS409ESH01H ⁽⁶⁾		•										
	*HS430ESD01H ⁽³⁾			•									
	HS446ESS11H ⁽³⁾				•								
	HS440ESF01H ⁽⁴⁾				•								
	HS440ESF03H ⁽⁵⁾				•								
	*HS450ESF01H ⁽⁴⁾					•							
	HS460ESF01H ⁽⁴⁾						•			•			
	HS460ESH01H ⁽⁶⁾							•		•			
	*HS467ESH01H ⁽⁶⁾								•				
	HS470ESS11H ⁽³⁾								•				
HS470ESF01H ⁽⁴⁾								•					
HS470ESH01H ⁽⁶⁾								•					
Assembler (IBM PC)	AS400PUT11SF ⁽⁸⁾	•	•	•	•	•	•	•	•	•	•		
	AS40PUT11SF ⁽⁸⁾											•	•
Simulator (IBM PC)	S400SIMPC ⁽⁹⁾	•	•	•	•	•	•	•	•	•	•		

* Under development
 Notes: (1) All emulators and emulator units include RS-232C port for connection to IBM PC.
 (2) Requires HS400EUA01H emulator unit and applicable user system interface cable.
 (3) For dual inline package (DIP).
 (4) For rectangular outline quad flat package (QFP).
 (5) For square outline quad flat package (SQFP).
 (6) Developed by one of Hitachi's overseas engineering subsidiaries.



2. Emulator

■ Emulator for 4-bit Single-Chip General-Purpose Microcomputer:

The emulator for 4-bit single-chip general-purpose microcomputers is an incircuit emulator to develop application systems incorporating a 4-bit single-chip microcomputer. The emulator efficiently supports system development in both software and hardware, as well as software debugging.

Features

- Effective as a software development system, as well as helping hardware development with a user prototype system connected.
- Efficient development enabled by various kinds of emulation commands.
- Memory address corresponding to the microcomputer internal ROM (Mask ROM), or EPROM, can be switched to the RAM on the emulator (described as "User RAM") or to EPROM for emulation.
- Allows easy serial interface selection (setting interface levels, baud rate).
- HMCS series mask option functions can be used by manual operation during emulation.

Functions

- Real-time execution
Executes a user program from the address specified until 1 or 2 occurs.
 1. A breakpoint is detected.
 2. The RESET or ABORT switch is pressed.

- Single-step execution

Executes an instruction at the address specified, and displays contents of the MCU register, RAM, or I/O port. Sequential execution is possible.

- Real-time trace

Executes a user program in real-time while tracing the user program address, data, interrupt generation, and contents of 8-bit data detected by external probes.

- Sets, displays, and cancels breakpoint
Breakpoints can be set in the following modes.

1. Address specified
2. Pattern detected by external probes
3. Opcode specified
4. Number of execution cycles after the above conditions are detected.
Note. Combination of 1-3 can be set for 4 points. 4 can be set for 1 point.

- Coverage function (C0 coverage)

- Displays and modifies the object program and contents of the MCU register and RAM

- Line assemble

Writes an instruction to the address specified in mnemonic using CRT

- Line disassemble

Disassembles and displays the object program in the address range specified

4-bit Single-chip Microcomputer Supporting Systems

Product to debug	Emulator only
HMCS402, HMCS404, HMCS408	H400CMIX2 (HS408EML02H)
HMCS412, HMCS414, HMCS424	
HD4074008	

ZTAT Microcomputer

Product to debug	Package	Maker	Socket adapter for ZTAT Microcomputers
HD4074008	DP-64S	DATA I/O	HS408ESS11H
	FP-64		HS408ESF01H
	FP-64A	DATA I/O	HS408ESF03H



Program Development Procedure and Support Systems

Selected by a Host Computer

Host Computer (manufacturer)	OS	Cross Assembler	Host Interface Software Simulator
IBM PC or Compatibles	PC-DOS	AS400PUT1SF	SUTLIBMPC** S400SIMPC

**Included with Cross Assembler

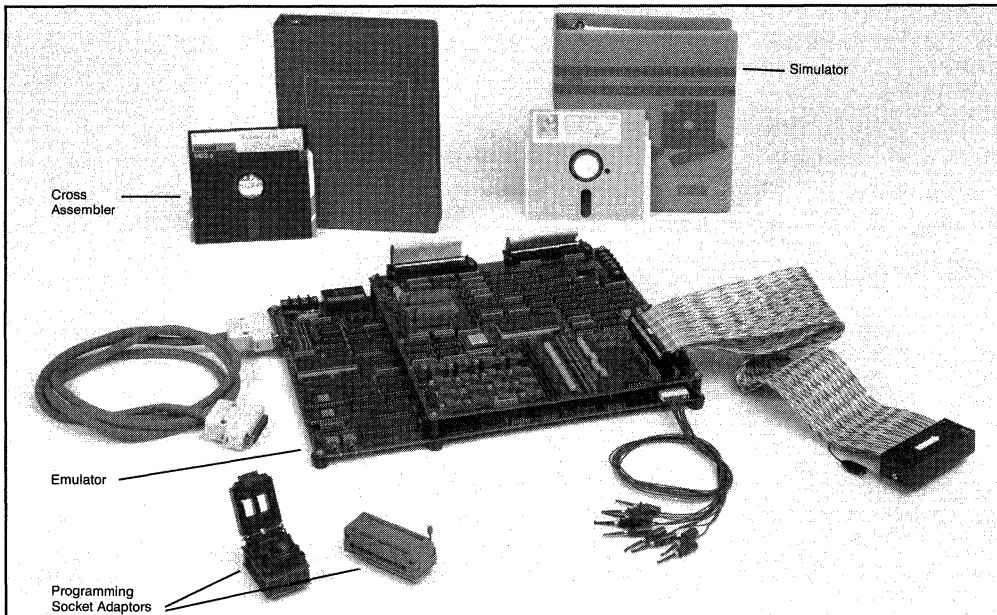
Emulator Commands

Category	Command	Function
File management	L	Loads object program and loads symbol information
	V	Verifies object program
	P	Saves object program
Execution	G	Executes user program
	S	Traces user program in single step
Setting break conditions	TR	Sets, displays and cancels combination break conditions
	BR1	
	BR2	
	BR3	
Management of memory and registers	I	Displays and modifies program memory contents
	ID	Dumps program memory contents
	T	Transfers object program
	C	Compares object program
	M	Displays and modifies data memory contents
	MD	Dumps data memory contents
	R	Displays and modifies register values
	IO	Displays and modifies I/O port contents
	U	Sets and displays EPROM/user RAM
Support of debugging	Q	Displays real-time trace results
	HE	Displays all emulator commands
	A	Line assemble
	DA	Disassemble
	O	Searches for bit pattern
	CO	Displays and clears coverage data
	F	Sets and displays MCU clock mode
	N	Designates transfer rate

Program Development Procedure and Support Systems

Specifications

Item	Emulator product No.	
	HS440EML01H	H400CMIX2 (HS408EML02H)
Support clock	8 MHz External clock	0.4, 0.8, 1.14, 1.6, 2, 2.67, 4, 6.01, 8 MHz External clock
Emulation memory	16kW	8kW
Break	Combination break: 4 points PC break: Entire program memory area	Combination break: 4 points
Real-time trace capacity	2047 cycles	2048 cycles
Serial interface	Interface level	RS-232C, TTL
	Baud rate	300, 1200, 4800, 9600, 19200 BPS
User interface (Support package)	DP-64S	DP-64S
		DP-42
Emulator dimension	W : 440 mm	W : 365 mm
	L : 275 mm	L : 275 mm



HMCS400 Series General Purpose Microcomputer Development Tools



■ Emulator for 4-bit Single-chip AS Microcomputer:

The emulator for 4-bit single-chip AS (Application Specific) microcomputers powerfully supports system development in software and hardware.

Features

HS400EUA01H main features are as follows:

- Efficient development enabled by various kinds of emulation commands
- Adapts easily to different HMCS 400 series microcomputers by exchanging the target probe and user system interface cables. (Note that this cannot be used for developed emulator support products.)
- Contains emulator RAM (called "Program Memory") which includes a memory area corresponding to the HMCS400 series microcomputer internal ROM (Mask ROM) or EPROM
- Allows easy serial interface selection (setting interface levels, baud rate)
- Can evaluate the microcomputer mask option

Functions

HS400EUA01H main functions are as follows:

- Executes the user program in real-time
- Sets breakpoints
 - Combination breakpoints: 4 points (Can be specified with program counter, address/data bus, data memory information, external probe signal, pass count, etc.)

- PC breakpoints: Entire memory area (Can be specified with program counter)
- Displays trace results in trace stop mode without halting program execution
- Real-time trace
 - Memorizes and displays bus information and external signals before/after trace is stopped by breakpoints to a maximum of 2000 steps
- Symbolic debugging
 - Debugs by symbolic information (break, trace)
- Execution time measurement
 - Measures program execution time in microseconds to a maximum of one hour
- Line assemble
 - Modifies memory contents in assembly languages
- Disassemble
- Single-step trace
 - Traces a user program and displays contents of the MCU register and data memory at the address specified after each instruction is executed.
- Displays and modifies register contents
- Displays and modifies contents of program memory and data memory
- Coverage function (C0 coverage)
- Self-diagnostic function

Program Development Procedure and Support Systems

AS Microcomputer Supporting Systems

Product to debug	Package	Components			Socket adapter for ZTAT Microcomputer
		Emulator unit for HMCS 400 Series	Target Probe	User System interface Cable	
HD404608, HD4074608	FP-80B FP-80A	HS400EUA01H	HS460ETA01H	HS400ECA80H	HS460ESF01H HS460ESH01H*
HD404708, HD404709, HD4074709	DP-64S DC-64S FP-64B FP-64A		HS470ETA01H	HS470ECS64H* HS400ECA80H	HS470ESS11H HS470ESF01H HS470ESH01H
HD4074808, HD404808, HD407L4808, HD40L4808	FP-80B FP-80A		HS480ETA01H	HS400ECA80H	HS460ESF01H HS460ESH01H
HD404302, HD4074308	DP-42		HS430ETA01H	HS430ECD42H*	HS430ESD01H*
HD404678 HD4074678	FP-64A		HS467ETA01H*	HS400ECA80H	HS467ESH01H*
HD404019, HD4074019	DP-64S DC-64S FP-64B FP-64A		HS409ETA01H*	HS470ECS64H* HS400ECA80H	HS409ESS11H HS409ESF01H* HS409ESH01H*
HD404508, HD4074509	FP-80B		HS450ETA01H**	HS400ECA80H	HS450ESF01H**
HD404918, HD404919	DP-42		HS491ETA01H*	HS430ECD42H*	—
HD404418, HD4074408, HD4074418	DP-64S DC-64S FP-64 FP-64A	HS440EML01H	—		HS448ESS11H HS440ESF01H HS440ESF03H

* Under development

**Preliminary

Selected by a host computer

Host computer (manufacturer)	OS	Cross Assembler	Host interface program	Simulator
IBM PC or compatibles	PC-DOS	AS400PUT11SF	SUTLIBMPC**	S400SIMPC

**Included with cross assembler



Program Development Procedure and Support Systems

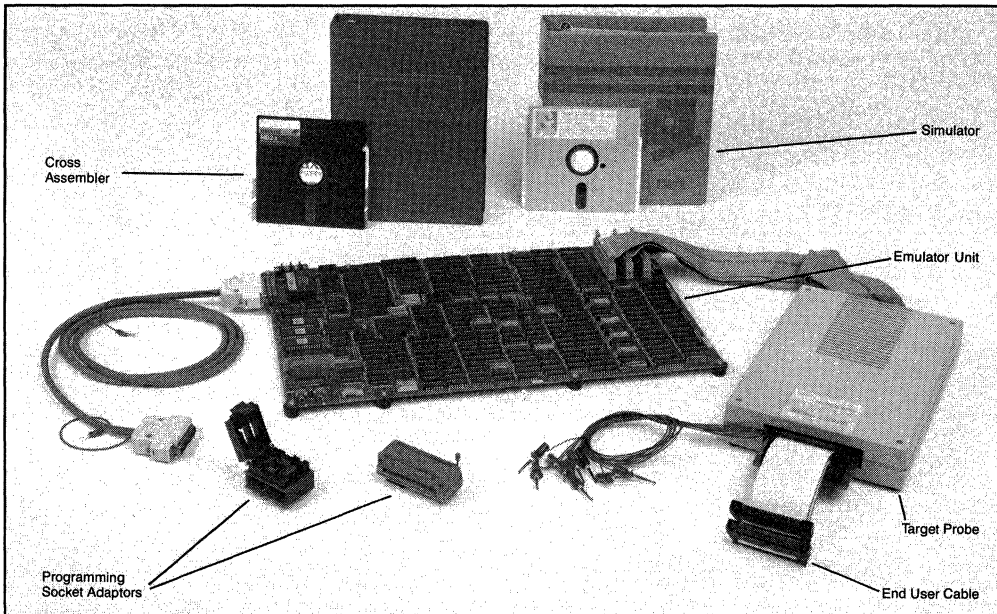
Emulator Commands

Category	Command	Function
File management	L	Loads object program and loads symbol information
	V	Verifies object program
	P	Saves object program
Execution	G	Executes user program
	S	Traces user program in single step
Setting break conditions	BP	Sets, displays and cancels program counter (PC) break
	TR	Sets, displays and cancels combination break conditions
	BR1	
	BR2	
	BR3	
Management of memory and registers	I	Displays and modifies program memory contents
	ID	Dumps program memory contents
	IMAP	Sets and displays the program memory area
	T	Transfers object program
	C	Compares object program
	M	Displays and modifies data memory contents
	MD	Dumps data memory contents
	MMAP	Sets and displays data memory area
	DEF	Sets address to display data memory contents during halt of user program execution
	R	Displays and modifies register values
IO	Displays and modifies I/O port contents	
Support of debugging	CONT	Restarts real-time trace from subcommand wait
	Q	Displays real-time trace results
	HE	Displays all emulator commands
	A	Line assemble
	DA	Disassemble
	SYM	Defines, clears and displays symbols, and selects the attribute of the symbols to be loaded
	O	Searches for bit pattern
	CO	Displays and clears coverage data
	F	Sets and displays MCU clock mode
	TIM	Sets and displays MCU timer operation
N	Designates transfer rate	

Program Development Procedure and Support Systems

Specifications

Item	Emulator product No.				
	HS400EUA01H +HS460ETA01H	HS400EUA01H +HS470ETA01H	HS400EUA01H +HS480ETA01H	HS400EUA01H +HS430ETA01H	HS400EUA01H +HS450ETA01H
Support clock	800 kHz External clock	4 MHz External clock	800 kHz External clock	4 MHz External clock	4.5 MHz External clock
Emulation memory	16 kW				
Break	Combination break: 4 points PC break: entire program memory area				
Real-time trace capacity	2047 cycles				
Serial interface	Interface level	RS-232C, TTL			
	Baud rate	300, 1200, 4800, 9600, 19200 BPS			
User interface (Support package)	FP-80A/B	DP-64S FP-64A/B	FP-80A/B	DP-4	FP-80B
Dimension	Emulator unit	W : 440 mm, L : 275 mm			
	Target probe	W : 258 mm, L : 169 mm			



HMCS400 Series Application Specific (AS) Microcomputer Development Tools



Data Sheets

HMCS400 Series General Purpose Microcomputer



HMCS402C(HD614022)/ HMCS402CL(HD614025)/ HMCS402AC(HD614028)

DESCRIPTION

The HMCS402C/CL/AC are CMOS 4-bit single-chip micro-computers with high performance and low power dissipation. They have efficient and powerful architecture same as HMCS400 series basically.

These microcomputers provide variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide user's applications. I/O pins of HMCS402C/CL/AC are able to drive fluorescent display tube directly.

The HMCS402CL is able to operate in low voltage and has the characteristics of wide-range operation voltage.

HMCS402AC is a high-speed version of HMCS402C.

■ HARDWARE FEATURES

- 4-bit Architecture
- 2048 Words x 10-bit ROM
- 160 Digits x 4-bit RAM
- 58 I/O Pins, Including 26 High Voltage I/O Pins (40V Max)
- Two Timer/Counters
 - 11-bit Prescaler
 - 8-bit Free Running Timer
 - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupts
 - External 2
 - Timer/Counter 2
 - Serial Interface 1
- Subroutine Stack
 - Up to 16 Levels Including Interrupt
- Two Low Power Dissipation Modes
 - Standby — Stops instruction execution while keeping clock oscillation and interrupt functions in operation
 - Stop — Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
 - External Connection of Crystal, Ceramic Filter or Resistor (externally drivable)
 - (Resistor Oscillator is available only to the HMCS402C)

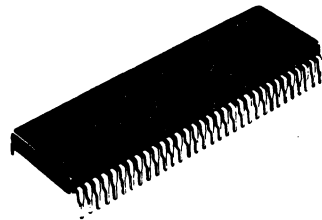
■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single-word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation — Table Look Up Capability —
- Bit Manipulation for Both RAM and I/O

■ PROGRAM DEVELOPMENT SUPPORT TOOLS

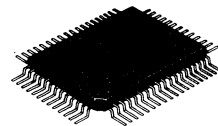
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

HMCS402C, HMCS402CL, HMCS402AC



(DP-64S)

HMCS402C, HMCS402CL, HMCS402AC



(FP-64)

- EPROM On Package Microcomputer; HD614P080S

Mask options are fixed as follows:

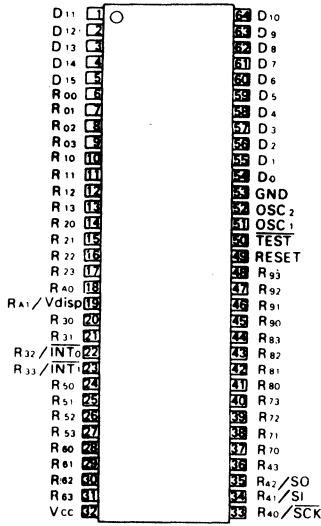
- I/O pin : Open Drain
- Oscillator : Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)
- Divider : Divided-by-8

■ HMCS402C/CL/AC CLASSIFICATIONS

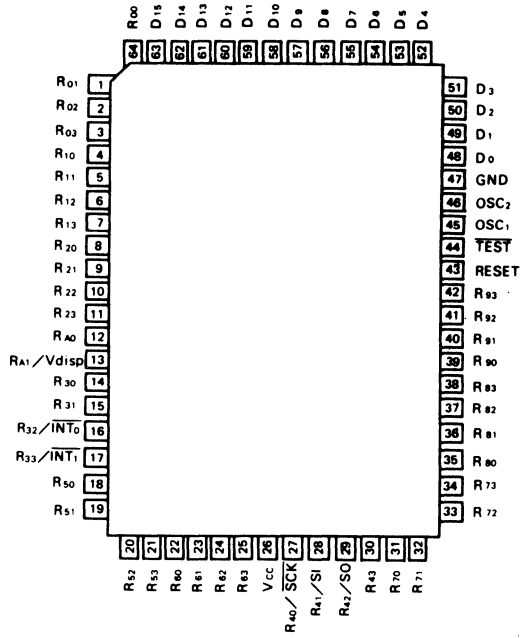
Type Name	HMCS402C (HD614022)	HMCS402CL (HD614025)	HMCS402AC (HD614028)
V _{CC} (V)	4 ~ 6	2.7 ~ 6	4.5 ~ 6
Minimum Instruction Execution Time (μs)	2	4	1.33

HMCS402C/HMCS402CL/HMCS402AC

■ PIN ARRANGEMENT

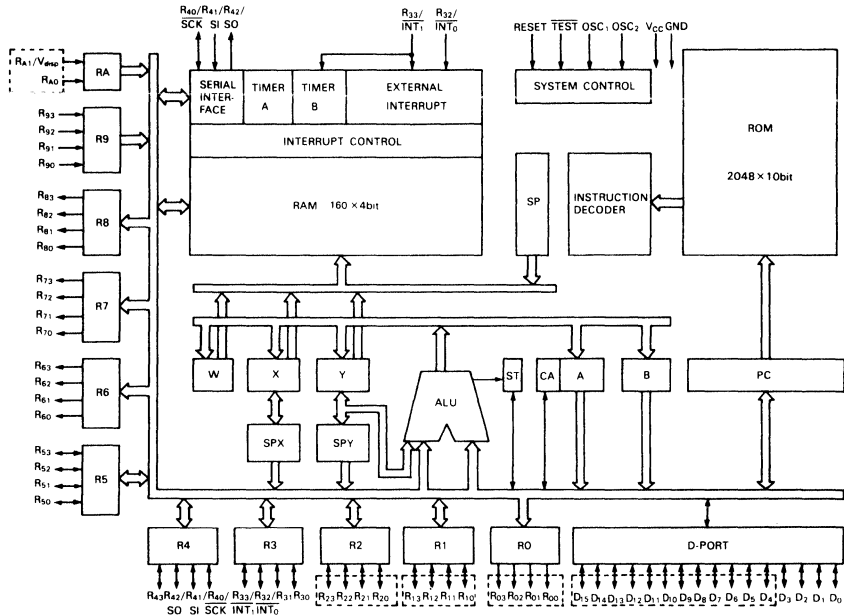


(Top View)



(Top View)

■ BLOCK DIAGRAM



□ High Voltage Pins

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC}+0.3$	V	3
		$V_{CC}-45$ to $V_{CC}+0.3$	V	4
Total Allowance of Input Currents	$\sum I_O$	50	mA	5
Total Allowance of Output Currents	$-\sum I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
		4	mA	9, 10
		6	mA	9, 11
Maximum Output Current	$-I_O$	30	mA	9, 12
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.

(Note 2) All voltages are with respect to GND.

(Note 3) Applied to standard pins.

(Note 4) Applied to high voltage pins.

(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.

(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.

(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.

(Note 8) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.

(Note 10) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 11) Applied to $R0 \sim R2$.

(Note 12) Applied to $D_0 \sim D_{15}$.

HMCS402C/HMCS402CL/HMCS402AC

■ HMCS402C ELECTRICAL CHARACTERISTICS

- DC CHARACTERISTICS ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Input "High" Voltage	V_{IH}	RESET, SCK, INT ₀ , INT ₁		$0.7V_{CC}$	—	$V_{CC}+0.3$	V		
		SI		$0.7V_{CC}$	—	$V_{CC}+0.3$	V		
		OSC ₁		$V_{CC}-0.5$	—	$V_{CC}+0.3$	V		
Input "Low" Voltage	V_{IL}	RESET, SCK, INT ₀ , INT ₁		-0.3	—	$0.22V_{CC}$	V		
		SI		-0.3	—	$0.22V_{CC}$	V		
		OSC ₁		-0.3	—	0.5	V		
Output "High" Voltage	V_{OH}	SCK, SO	$-I_{OH} = 1.0$ mA	$V_{CC}-1.0$	—	—	V		
			$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	—	—	V		
Output "Low" Voltage	V_{OL}	SCK, SO	$I_{OL} = 1.6$ mA	—	—	0.4	V		
Input/Output Leakage Current	I_{IL}	RESET, SCK, INT ₀ , INT ₁ , SI, SO, OSC ₁	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	1	
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC}=5V$	Crystal or Ceramic Filter Oscillator Option $f_{osc} = 4MHz$	—	—	2.0	mA	2, 6
				Resistor Oscillator Option $f_{osc} = 4MHz$	—	—	2.4	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Oscillator Option $f_{osc} = 4MHz$	—	—	1.2	mA	3, 6
				Resistor Oscillator Option $f_{osc} = 4MHz$	—	—	1.6	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Oscillator Option $f_{osc} = 4MHz$	—	—	0.9	mA	4, 6
				Resistor Oscillator Option $f_{osc} = 4MHz$	—	—	1.3	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in}(TEST) = V_{CC}-0.3V$ to V_{CC} $V_{in}(RESET) = 0V$ to $0.3V$	—	—	10	μA	5	
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	—	—	V		

(Note 1) Pull-up MOS current and output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; • Reset state in Operation Mode
 Pin state; • RESET, TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R_3 \sim R_9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R_0 \sim R_2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2 prescaler divide ratio
 • TIMER-B; ± 2 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R_3 \sim R_9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R_0 \sim R_2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2048 prescaler divide ratio
 • TIMER-B; ± 2048 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R_3 \sim R_9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R_0 \sim R_2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 5) Pull-down MOS current is excluded.

(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value (} f_{osc}=x \text{ [MHz])} = \frac{x}{4} \times \text{max. value (} f_{osc}=4 \text{ [MHz])}$$

• INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN
 ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3, R_3 \sim R_5, R_9$		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3, R_3 \sim R_5, R_9$		-0.3	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3, R_3 \sim R_8$	$-I_{OH} = 1.0 \text{ mA}$	$V_{CC}-1.0$	—	—	V	1
		$D_0 \sim D_3, R_3 \sim R_8$	$-I_{OH} = 0.01 \text{ mA}$	$V_{CC}-0.3$	—	—	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3, R_3 \sim R_8$	$I_{OL} = 1.6 \text{ mA}$	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	$D_0 \sim D_3, R_3 \sim R_9$	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3, R_3 \sim R_9$	$V_{CC} = 5V$ $V_{in} = 0V$	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.

(Note 2) Pull-up MOS current and output buffer current are excluded.

(Note 3) Applied to I/O pins with "with Pull-up MOS" selected by mask option.

HMCS402C/HMCS402CL/HMCS402AC

- INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN
($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC}-40$	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH}=15mA, V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH}=9mA$	$V_{CC}-2.0$	—	—	V	
		R0 ~ R2	$-I_{OH}=3mA, V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH}=1.8mA$	$V_{CC}-2.0$	—	—	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	—	—	$V_{CC}-37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC} - 40V$	—	—	$V_{CC}-37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	—	—	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

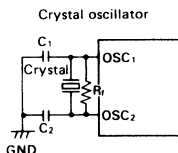
- (Note 1) Applied to I/O pins with "with Pull-down MOS" selected by mask option.
 (Note 2) Applied to I/O pins with "without Pull-down MOS (PMOS Open Drain)" selected by mask option.
 (Note 3) Pull-down MOS current and output buffer current are excluded.
 (Note 4) Applied to I/O pins with "with Pull-down MOS" selected by mask option.

HMCS402C/HMCS402CL/HMCS402AC

● **AC CHARACTERISTICS** ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

	Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
					min	typ	max		
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂		0.4	4	4.5	MHz	
	Instruction Cycle Time	t_{cyc}			1.78	2	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂		—	—	20	ms	1
Resistor Oscillator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	$R_f = 20k\Omega \pm 2\%$	1.8	3.0	4.2	MHz	
	Instruction Cycle Time	t_{cyc}		$R_f = 20k\Omega \pm 2\%$	1.9	2.66	4.44	μs	
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂	$R_f = 20k\Omega \pm 2\%$	—	—	0.5	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC ₁		0.4	—	4.5	MHz	2
	External Clock "High" Level Width	t_{CPH}	OSC ₁		100	—	—	ns	2
	External Clock "Low" Level Width	t_{CPL}	OSC ₁		100	—	—	ns	2
	External Clock Rise Time	t_{CPr}	OSC ₁		—	—	20	ns	2
	External Clock Fall Time	t_{CPf}	OSC ₁		—	—	20	ns	2
	Instruction Cycle Time	t_{cyc}			1.78	—	20	μs	2
	INT ₀ "High" Level Width	t_{I0H}	INT ₀		2	—	—	t_{cyc}	3
INT ₀ "Low" Level Width	t_{I0L}	INT ₀		2	—	—	t_{cyc}	3	
INT ₁ "High" Level Width	t_{I1H}	INT ₁		2	—	—	t_{cyc}	3	
INT ₁ "Low" Level Width	t_{I1L}	INT ₁		2	—	—	t_{cyc}	3	
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4	
Input Capacitance	C_{in}	all pins		$f = 1MHz$ $V_{in} = 0V$	—	—	15	pF	
RESET Fall Time	t_{RSTf}				—	—	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.0V at "Power-on", or after RESET input level goes to "High" by resetting to quit the stop mode by MCU reset on the circuits below. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

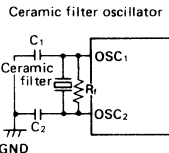


Crystal: 4.194304MHz NC-18C(Nihon Denpa Kogyo)

$R_f : 1M\Omega \pm 2\%$

$C_1 : 22pF \pm 20\%$

$C_2 : 22pF \pm 20\%$

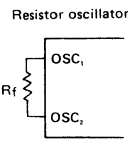


Ceramic filter: CSA4.00MG (Murata)

$R_f : 1M\Omega \pm 2\%$

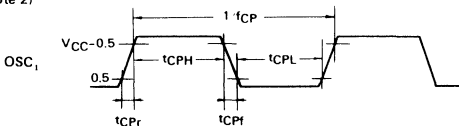
$C_1 : 30pF \pm 20\%$

$C_2 : 30pF \pm 20\%$

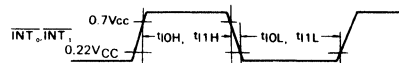


$R_f : 20k\Omega \pm 2\%$

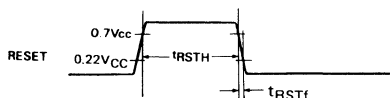
(Note 2)



(Note 3)



(Note 4)



HMCS402C/HMCS402CL/HMCS402AC

● SERIAL INTERFACE TIMING CHARACTERISTICS

($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{diSP} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

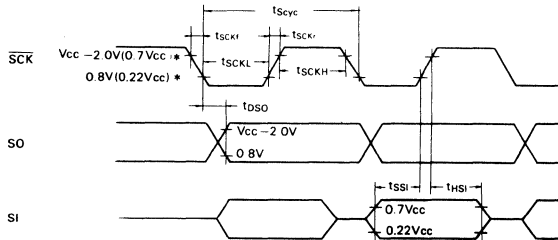
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	$t_{S_{cyc}}$	SCK	(Note 2)	1	—	—	t_{cyc}	1, 2
Transfer Clock "High" Level Width	$t_{S_{CKH}}$	SCK	(Note 2)	0.5	—	—	$t_{S_{cyc}}$	1, 2
Transfer Clock "Low" Level Width	$t_{S_{CKL}}$	SCK	(Note 2)	0.5	—	—	$t_{S_{cyc}}$	1, 2
Transfer Clock Rise Time	$t_{S_{CKr}}$	SCK	(Note 2)	—	—	100	ns	1, 2
Transfer Clock Fall Time	$t_{S_{CKf}}$	SCK	(Note 2)	—	—	100	ns	1, 2
Serial Output Data Delay Time	$t_{D_{SO}}$	SO	(Note 2)	—	—	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSi}	SI		500	—	—	ns	1
Serial Input Data Hold Time	t_{HSi}	SI		150	—	—	ns	1

- At Transfer Clock Input

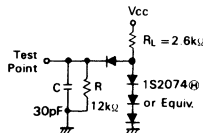
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	$t_{S_{cyc}}$	SCK		1	—	—	t_{cyc}	1
Transfer Clock "High" Level Width	$t_{S_{CKH}}$	SCK		0.5	—	—	$t_{S_{cyc}}$	1
Transfer Clock "Low" Level Width	$t_{S_{CKL}}$	SCK		0.5	—	—	$t_{S_{cyc}}$	1
Transfer Clock Rise Time	$t_{S_{CKr}}$	SCK		—	—	100	ns	1
Transfer Clock Fall Time	$t_{S_{CKf}}$	SCK		—	—	100	ns	1
Serial Output Data Delay Time	$t_{D_{SO}}$	SO	(Note 2)	—	—	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSi}	SI		500	—	—	ns	1
Serial Input Data Hold Time	t_{HSi}	SI		150	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface

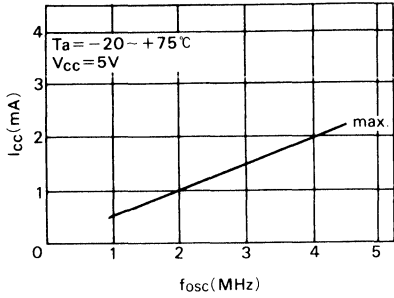


* $V_{CC} - 2.0V$ and $0.8V$ are the threshold voltage for transfer clock output.
 $0.7 V_{CC}$ and $0.22 V_{CC}$ are the threshold voltage for transfer clock input.

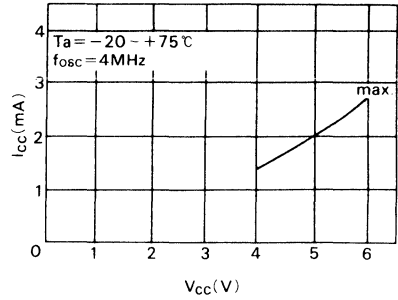
(Note 2) Timing Load Circuit



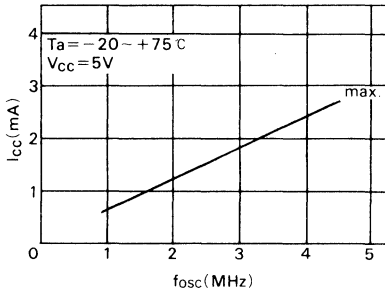
● CHARACTERISTICS CURVE (REFERENCE DATA)



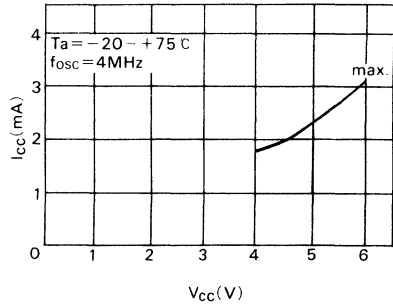
I_{CC} vs. f_{OSC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



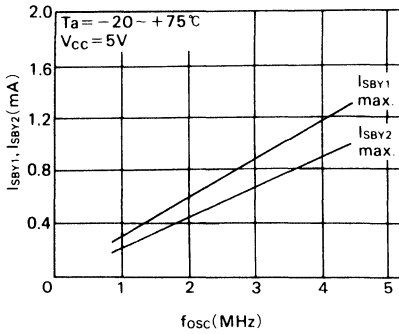
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



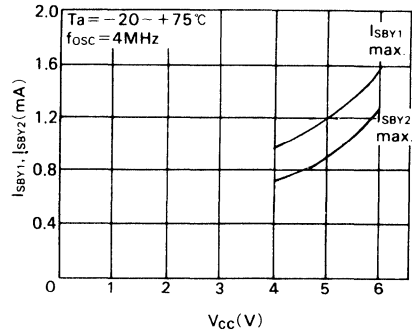
I_{CC} vs. f_{OSC} Characteristics
(Resistor Oscillator Option)



I_{CC} vs. V_{CC} Characteristics
(Resistor Oscillator Option)

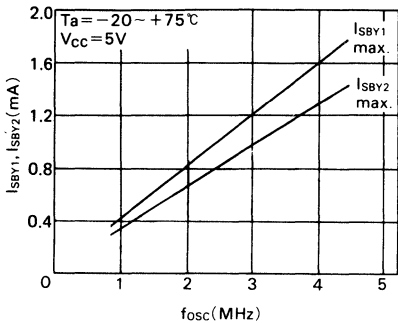


I_{SBV1}, I_{SBV2} vs. f_{OSC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)

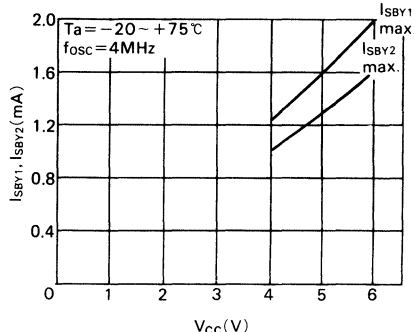


I_{SBV1}, I_{SBV2} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)

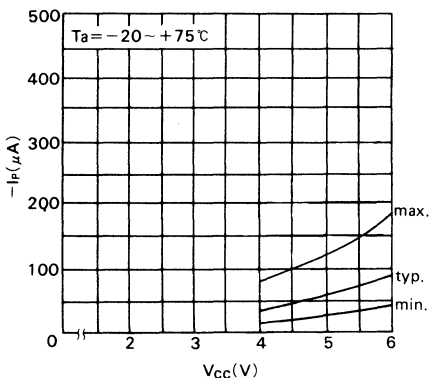
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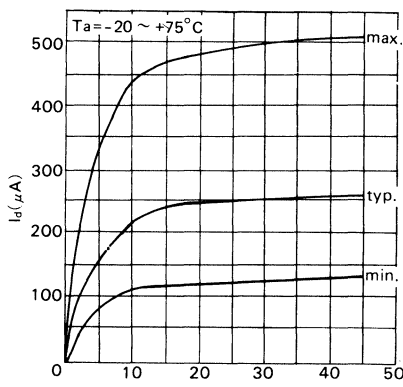
I_{SBY} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



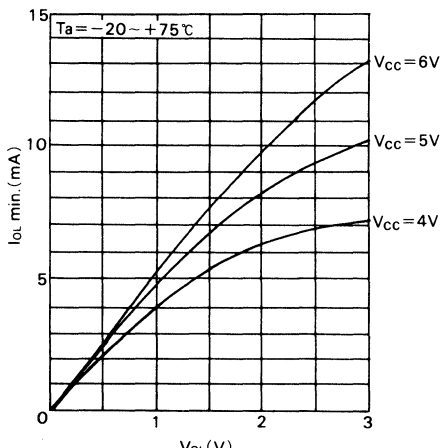
I_{SBY} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



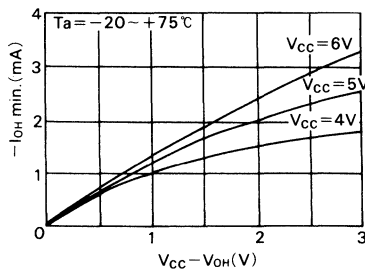
$-I_P$ (Pull-up MOS Current) vs. V_{CC} Characteristics



I_d (Pull-down MOS Current) vs. $(V_{CC} - V_{disp})$ Characteristics

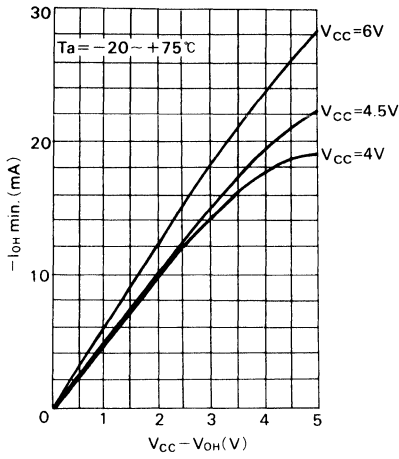


$I_{OL \text{ min.}}$ vs. V_{OL} Characteristics
(Standard Pin)

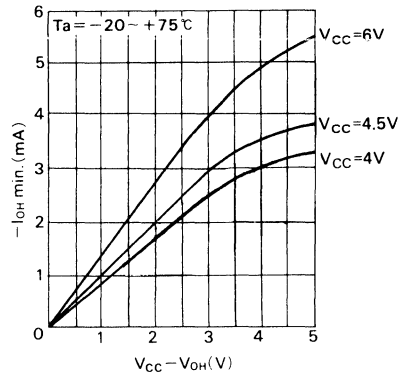


$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")





$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($D_4 \sim D_{15}$ Pins)



$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($RO \sim R_2$ Pins)

HMCS402C/HMCS402CL/HMCS402AC

■ HMCS402CL ELECTRICAL CHARACTERISTICS

- DC CHARACTERISTICS ($V_{CC}=2.7V$ to $6V$, $GND=0V$, $V_{disp}=V_{CC}-40V$ to V_{CC} , $T_a=-20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, \overline{SCK} , $\overline{INT0}$, $\overline{INT1}$		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
		SI		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
		OSC ₁		$V_{CC}-0.3$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	RESET, \overline{SCK} , $\overline{INT0}$, $\overline{INT1}$		-0.3	—	$0.15V_{CC}$	V	
		SI		-0.3	—	$0.15V_{CC}$	V	
		OSC ₁		-0.3	—	0.3	V	
Output "High" Voltage	V_{OH}	\overline{SCK} , SO	$-I_{OH} = 0.1$ mA	$V_{CC}-0.5$	—	—	V	
Output "Low" Voltage	V_{OL}	\overline{SCK} , SO	$I_{OL} = 0.4$ mA	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , $\overline{INT0}$, $\overline{INT1}$, SI, SO, OSC ₁	$V_{in} = 0$ V to V_{CC}	—	—	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.6	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.5	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.4	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in}(\overline{TEST}) = V_{CC}-0.2V$ to V_{CC} $V_{in}(\text{RESET}) = 0V$ to 0.2 V	—	—	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	—	—	V	



(Note 1) Pull-up MOS current and output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; • Reset state in Operation Mode
 Pin state; • RESET, TEST ... V_{CC} voltage
 • D₀ ~ D₃, R3 ~ R9 ... V_{CC} voltage
 • D₄ ~ D₁₅, R0 ~ R2, R_{AG}, R_{A1} ... V_{disp} voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ÷2 prescaler divide ratio
 • TIMER-B; ÷2 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • D₀ ~ D₃, R3 ~ R9 ... V_{CC} voltage
 • D₄ ~ D₁₅, R0 ~ R2, R_{AG}, R_{A1} ... V_{disp} voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ÷2048 prescaler divide ratio
 • TIMER-B; ÷2048 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • D₀ ~ D₃, R3 ~ R9 ... V_{CC} voltage
 • D₄ ~ D₁₅, R0 ~ R2, R_{AG}, R_{A1} ... V_{disp} voltage

(Note 5) Pull-down MOS current is excluded.

(Note 6) When f_{osc}=x[MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

[When Divide-by-8 (D-8) option is selected.] max. value (f_{osc}=x[MHz]) = $\frac{x}{2}$ x max. value (f_{osc}=2[MHz])

● **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**

(V_{CC} = 2.7V to 6V, GND = 0V, V_{disp} = V_{CC} - 40V to V_{CC}, T_a = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₀ ~ D ₃ , R3 ~ R5, R9		0.85V _{CC}	-	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₀ ~ D ₃ , R3 ~ R5, R9		-0.3	-	0.15 V _{CC}	V	
Output "High" Voltage	V _{OH}	D ₀ ~ D ₃ , R3 ~ R8	-I _{OH} = 0.1 mA	V _{CC} -0.5	-	-	V	1
Output "Low" Voltage	V _{OL}	D ₀ ~ D ₃ , R3 ~ R8	I _{OL} = 0.4 mA	-	-	0.4	V	
Input/Output Leakage Current	I _{IL}	D ₀ ~ D ₃ , R3 ~ R9	V _{in} = 0V to V _{CC}	-	-	1	μA	2
Pull-Up MOS Current	-I _p	D ₀ ~ D ₃ , R3 ~ R9	V _{CC} = 3V V _{in} = 0V	3	15	40	μA	3
		D ₀ ~ D ₃ , R3 ~ R9	V _{CC} = 5V V _{in} = 0V	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" output selected by mask option.

(Note 2) Pull-up MOS current and output buffer current are excluded.

(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

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● INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN
($V_{CC} = 2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC}-40$	—	$0.15V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH} = 15mA$, $V_{CC} = 5V \pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH} = 2.5mA$	$V_{CC}-1.0$	—	—	V	
		R0 ~ R2	$-I_{OH} = 3mA$, $V_{CC} = 5V \pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH} = 0.5mA$	$V_{CC}-1.0$	—	—	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	—	—	$V_{CC}-37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC} - 40V$	—	—	$V_{CC}-37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	—	—	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.

(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.

(Note 3) Pull-down MOS current and output buffer current are excluded.

(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

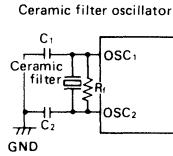
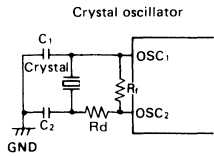


HMCS402C/HMCS402CL/HMCS402AC

- AC CHARACTERISTICS ($V_{CC}=2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC1, OSC2		0.4	2	2.25	MHz	
Instruction Cycle Time	t_{cyc}			3.55	4	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC1, OSC2		—	—	60	ms	1
External Clock "High" Level Width	t_{CPH}	OSC1		205	—	—	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC1		205	—	—	ns	2
External Clock Rise Time	t_{CPr}	OSC1		—	—	20	ns	2
External Clock Fall Time	t_{CPf}	OSC1		—	—	20	ns	2
$\overline{INT_0}$ "High" Level Width	t_{I0H}	$\overline{INT_0}$		2	—	—	t_{cyc}	3
$\overline{INT_0}$ "Low" Level Width	t_{I0L}	$\overline{INT_0}$		2	—	—	t_{cyc}	3
$\overline{INT_1}$ "High" Level Width	t_{I1H}	$\overline{INT_1}$		2	—	—	t_{cyc}	3
$\overline{INT_1}$ "Low" Level Width	t_{I1L}	$\overline{INT_1}$		2	—	—	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4
Input Capacitance	C_{in}	all pins	$f = 1\text{ MHz}$ $V_{in} = 0\text{ V}$	—	—	15	pF	
RESET Fall Time	t_{RSTf}			—	—	15	ms	4

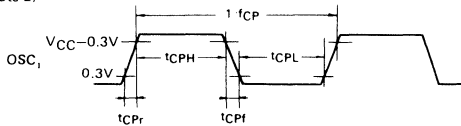
(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.



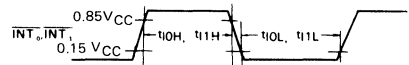
Crystal: 2.097152MHz DS-MGQ308 (Seiko Denshi)
 $R_f = 2M\Omega \pm 2\%$, $R_d = 2.2k\Omega \pm 2\%$
 $C_1 = 10pF \pm 20\%$
 $C_2 = 10pF \pm 20\%$

Ceramic filter: CSA2.000MK (Murata)
 $R_f = 1M\Omega \pm 2\%$, $C_1 = C_2 = 30pF \pm 20\%$

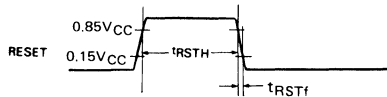
(Note 2)



(Note 3)



(Note 4)



HMCS402C/HMCS402CL/HMCS402AC

• SERIAL INTERFACE TIMING CHARACTERISTICS

($V_{CC}=2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC}-40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

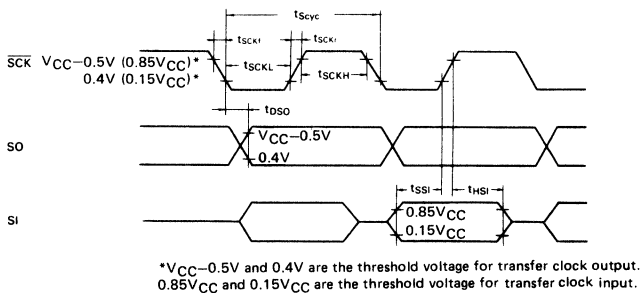
• At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	\overline{SCK}	(Note 2)	1	—	—	t_{CYC}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	\overline{SCK}	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	\overline{SCK}	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock Rise Time	t_{SCKr}	\overline{SCK}	(Note 2)	—	—	300	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	\overline{SCK}	(Note 2)	—	—	300	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	—	—	ns	1

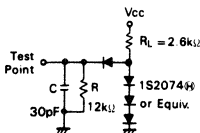
• At Transfer Clock Input

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	SCK		1	—	—	t_{CYC}	1
Transfer Clock "High" Level Width	t_{SCKH}	SCK		0.5	—	—	t_{SCYC}	1
Transfer Clock "Low" Level Width	t_{SCKL}	SCK		0.5	—	—	t_{SCYC}	1
Transfer Clock Rise Time	t_{SCKr}	SCK		—	—	300	ns	1
Transfer Clock Fall Time	t_{SCKf}	SCK		—	—	300	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	—	—	ns	1

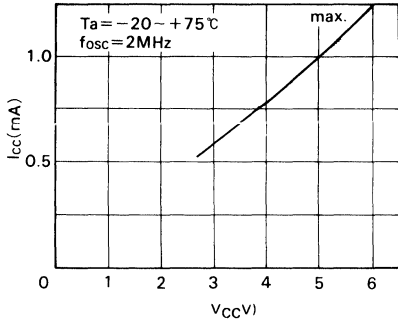
(Note 1) Timing Diagram of Serial Interface



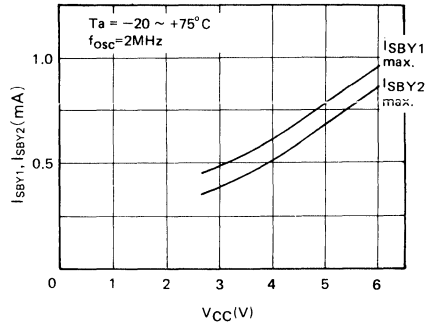
(Note 2) Timing Load Circuit



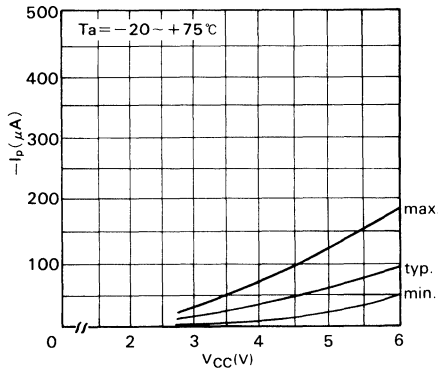
● CHARACTERISTICS CURVE (REFERENCE DATA)



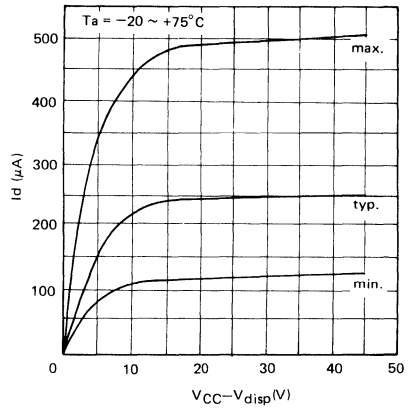
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



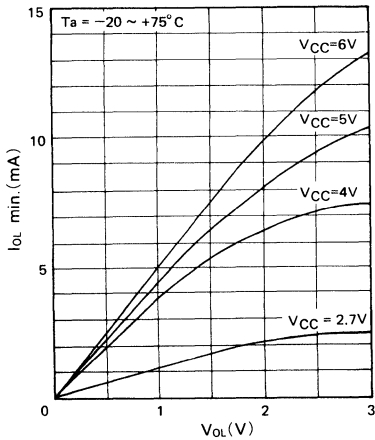
I_{SBY} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



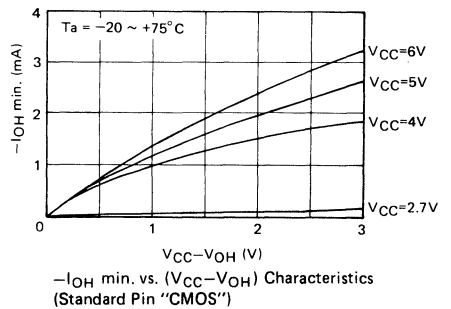
$-I_P$ (Pull-up MOS Current) vs. V_{CC} Characteristics



I_D (Pull-down MOS Current) vs. $(V_{CC} - V_{disp})$ Characteristics



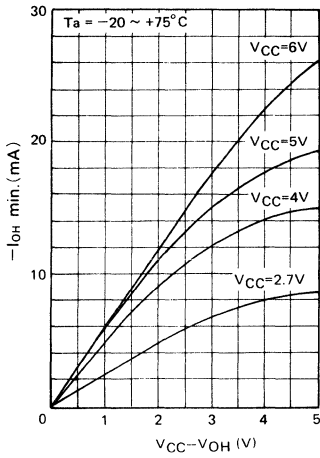
I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



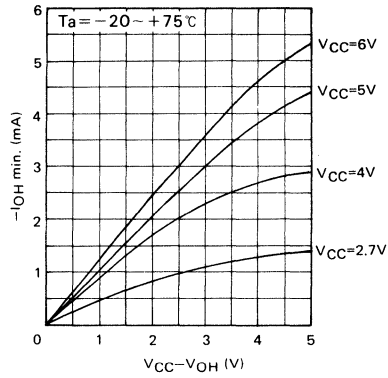
$-I_{OH}$ min. vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")



HMCS402C/HMCS402CL/HMCS402AC



$-I_{OH} \text{ min. vs. } (V_{CC} - V_{OH}) \text{ Characteristics}$
($D_4 \sim D_{1s}$ Pins)



$-I_{OH} \text{ min. vs. } (V_{CC} - V_{OH}) \text{ Characteristics}$
($R_0 \sim R_2$ Pins)



HMCS402C/HMCS402CL/HMCS402AC

■ **HMCS402AC ELECTRICAL CHARACTERISTICS**

● **DC CHARACTERISTICS** ($V_{CC} = 4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, \overline{SCK} , INT ₀ , INT ₁		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
		SI		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
		OSC ₁		$V_{CC}-0.5$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	RESET, \overline{SCK} , INT ₀ , INT ₁		-0.3	—	$0.22V_{CC}$	V	
		SI		-0.3	—	$0.22V_{CC}$	V	
		OSC ₁		-0.3	—	0.5	V	
Output "High" Voltage	V_{OH}	\overline{SCK} , SO	$-I_{OH} = 1.0$ mA	$V_{CC}-1.0$	—	—	V	
			$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	—	—	V	
Output "Low" Voltage	V_{OL}	\overline{SCK} , SO	$I_{OL} = 1.6$ mA	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , INT ₀ , INT ₁ , SI, SO, OSC ₁	$V_{in} = 0$ V to V_{CC}	—	—	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	3.0	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	1.8	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	1.35	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in} (\overline{TEST}) = V_{CC} - 0.3$ V to V_{CC} $V_{in} (RESET) = 0$ V to 0.3 V	—	—	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	—	—	V	

HMCS402C/HMCS402CL/HMCS402AC

(Note 1) Pull-up MOS current and output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; • Reset state in Operation Mode
Pin state; • RESET, TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2 prescaler divide ratio
 • TIMER-B; ± 2 prescaler divide ratio
 • SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2048 prescaler divide ratio
 • TIMER-B; ± 2048 prescaler divide ratio
 • SERIAL Interface ; Stop
Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 5) Pull-down MOS current is excluded.

(Note 6) When $f_{osc} = x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc} = x \text{ [MHz]}) = \frac{x}{6} \times \text{max. value } (f_{osc} = 6 \text{ [MHz]})$$

• **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
($V_{CC} = 4.5V$ to $6V, GND = 0V, V_{disp} = V_{CC} - 40V$ to $V_{CC}, T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3, R3 \sim R5, R9$		$0.7V_{CC}$	—	$V_{CC} + 0.3$	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3, R3 \sim R5, R9$		-0.3	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3, R3 \sim R8$	$-I_{OH} = 1.0 \text{ mA}$	$V_{CC} - 1.0$	—	—	V	1
		$D_0 \sim D_3, R3 \sim R8$	$-I_{OH} = 0.01 \text{ mA}$	$V_{CC} - 0.3$	—	—	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3, R3 \sim R8$	$I_{OL} = 1.6 \text{ mA}$	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	$D_0 \sim D_3, R3 \sim R9$	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3, R3 \sim R9$	$V_{CC} = 5V$ $V_{in} = 0V$	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.

(Note 2) Pull-up MOS current and output buffer current are excluded.

(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.



● **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**

($V_{CC} = 4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.7V_{CC}$	—	$V_{CC} + 0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC} - 40$	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH} = 15mA, V_{CC} = 5V \pm 10\%$	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 9mA$	$V_{CC} - 2.0$	—	—	V	
		R0 ~ R2	$-I_{OH} = 3mA, V_{CC} = 5V \pm 10\%$	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 1.8 mA$	$V_{CC} - 2.0$	—	—	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	—	—	$V_{CC} - 37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC} - 40V$	—	—	$V_{CC} - 37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	—	—	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.

(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.

(Note 3) Pull-down MOS current and output buffer current are excluded.

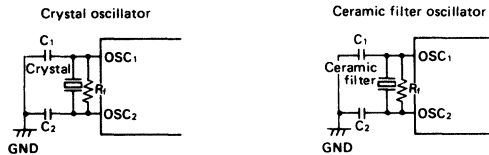
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

HMCS402C/HMCS402CL/HMCS402AC

● AC CHARACTERISTICS ($V_{CC}=4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC}-40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC1, OSC2		0.4	6	6.2	MHz	
Instruction Cycle Time	t_{cyc}			1.29	1.33	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC1, OSC2		—	—	20	ms	1
External Clock "High" Level Width	t_{CPH}	OSC1		70	—	—	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC1		70	—	—	ns	2
External Clock Rise Time	t_{CPr}	OSC1		—	—	20	ns	2
External Clock Fall Time	t_{CPf}	OSC1		—	—	20	ns	2
\overline{INT}_0 "High" Level Width	t_{I0H}	\overline{INT}_0		2	—	—	t_{cyc}	3
\overline{INT}_0 "Low" Level Width	t_{I0L}	\overline{INT}_0		2	—	—	t_{cyc}	3
\overline{INT}_1 "High" Level Width	t_{I1H}	\overline{INT}_1		2	—	—	t_{cyc}	3
\overline{INT}_1 "Low" Level Width	t_{I1L}	\overline{INT}_1		2	—	—	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4
Input Capacitance	C_{in}	all pins	$f = 1\text{ MHz}$ $V_{in} = 0\text{ V}$	—	—	15	pF	
RESET Fall Time	t_{RSTf}			—	—	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.



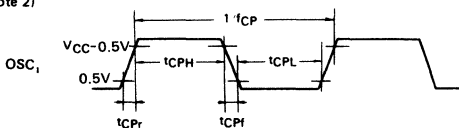
Crystal: 6.0MHz NC-18C (Nihon Denpa Kogyo)

R_f : $1M\Omega \pm 2\%$
 C_1 : $20pF \pm 20\%$
 C_2 : $20pF \pm 20\%$

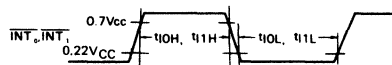
Ceramic filter: CSA6.00MG (Murata)

R_f : $1M\Omega \pm 2\%$
 C_1 : $30pF \pm 20\%$
 C_2 : $30pF \pm 20\%$

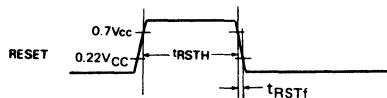
(Note 2)



(Note 3)



(Note 4)



• **SERIAL INTERFACE TIMING CHARACTERISTICS**

($V_{CC}=4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

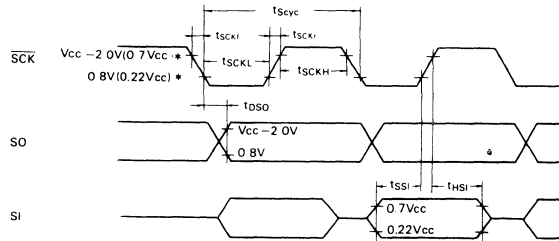
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Scyc}	\overline{SCK}	(Note 2)	1	—	—	t_{cyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	\overline{SCK}	(Note 2)	0.5	—	—	t_{Scyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	\overline{SCK}	(Note 2)	0.5	—	—	t_{Scyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	\overline{SCK}	(Note 2)	—	—	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	\overline{SCK}	(Note 2)	—	—	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

- At Transfer Clock Input

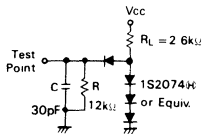
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Scyc}	\overline{SCK}		1	—	—	t_{cyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	\overline{SCK}		0.5	—	—	t_{Scyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	\overline{SCK}		0.5	—	—	t_{Scyc}	1
Transfer Clock Rise Time	t_{SCKr}	\overline{SCK}		—	—	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	\overline{SCK}		—	—	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface

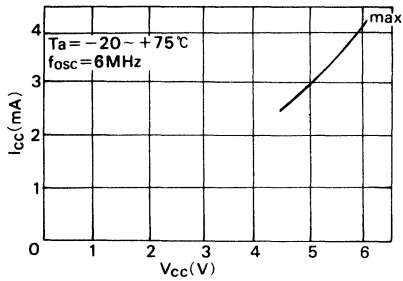


* $V_{CC} = 2.0V$ and $0.8V$ are the threshold voltage for transfer clock output.
 $0.7 V_{CC}$ and $0.22 V_{CC}$ are the threshold voltage for transfer clock input.

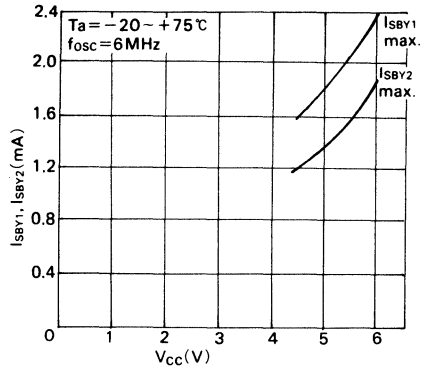
(Note 2) Timing Load Circuit



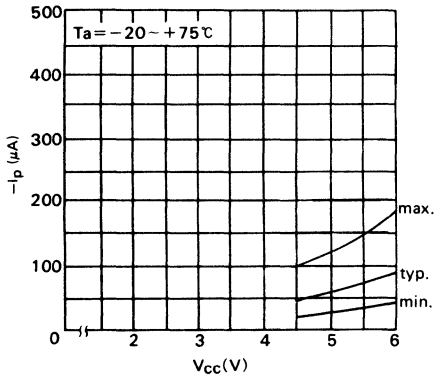
● CHARACTERISTICS CURVE (REFERENCE DATA)



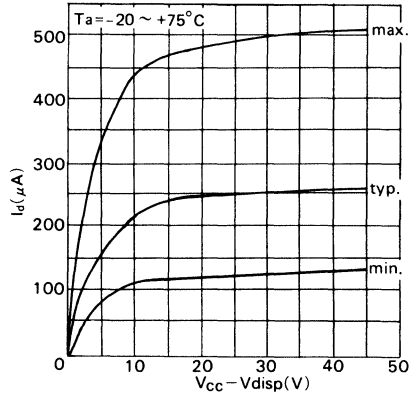
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



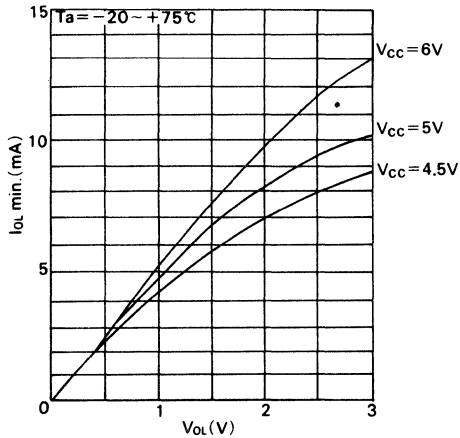
I_{SBY1}, I_{SBY2} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



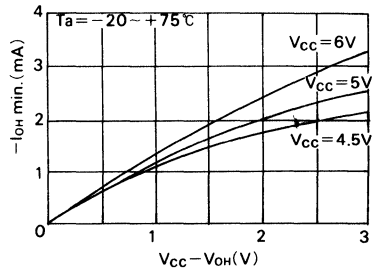
$-I_p$ (Pull-up MOS Current) vs. V_{CC} Characteristics



I_d (Pull-down MOS Current) vs. $(V_{CC} - V_{disp})$ Characteristics

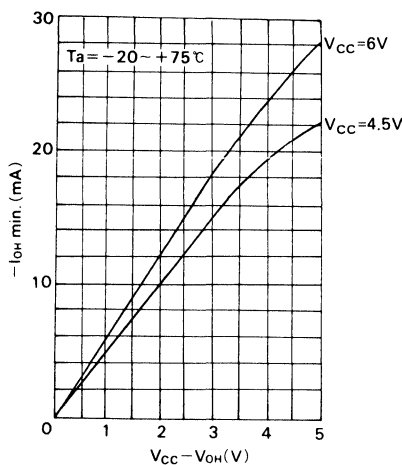


I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)

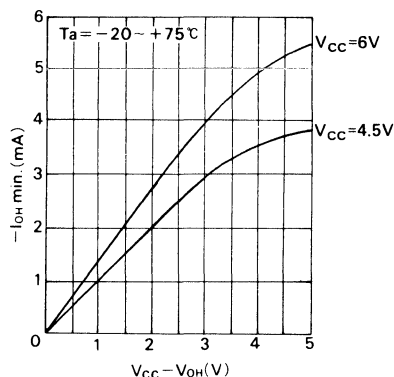


$-I_{OH}$ min. vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")





$-I_{OH\ min.}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($D_4 \sim D_{15}$ Pins)



$-I_{OH\ min.}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($R0 \sim R2$ Pins)

DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

GND, V_{CC} , V_{disp}

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is a power supply for high voltage Input/Output pins with maximum voltage of $V_{CC} - 40V$. V_{disp} pin can be also used as R_{A1} pin by mask option. For details, see "INPUT/OUTPUT".

TEST

TEST pin is not for user's application. TEST must be connected to V_{CC} .

RESET

RESET pin is used to reset MCU. For details, see "RESET".

OSC₁, OSC₂

These are Input pins to the internal oscillator circuit. They can be connected to crystal resonator, ceramic filter resonator R_f oscillator (applicable only to the HMCS402C), or external oscillator circuit. Select the circuit of MCU by mask option corresponding to the oscillator type. For details, see "INTERNAL OSCILLATOR CIRCUIT".

D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

R-port ($R0$ to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) $R0$ and $R6$ to $R8$ are output ports, $R9$ to RA are input ports, and $R1$ to $R5$ are Input/Output common ports. $R0$ to $R2$ and RA are the high voltage ports, $R3$ to $R9$ are the standard ports. Each pin has the mask option to select its cir-

cuit type. R_{32} , R_{33} , R_{40} , R_{41} and R_{42} are also available as INT_0 , INT_1 , SCK , SI and SO respectively. For details, see "INPUT/OUTPUT".

INT_0 , INT_1

These are the input pins to interrupt MCU operation externally. INT_1 can be used as an external event input pin for TIMER-B. INT_0 and INT_1 are also available as R_{32} , and R_{33} respectively. For details, See "INTERRUPT".

SCK, SI, SO

These are Transfer clock I/O pin (SCK), serial data input pin (SI) and serial data output pin (SO) used for serial interface. SCK, SI, and SO are also available as R_{40} , R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

ROM MEMORY MAP

MCU includes 2048 words \times 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

Vector Address Area \$0000 to \$000F

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMWL instructions branching to the starting addresses of reset routine or of interrupt routines.

Zero-Page Subroutine Area \$0000 to \$003F

CAL instruction allows to branch to the subroutines in \$0000 to \$003F.

Pattern Area \$0000 to \$07FF

P instruction allows referring to the ROM data in \$0000 to \$07FF as a pattern.

Program Area \$0000 to \$07FF



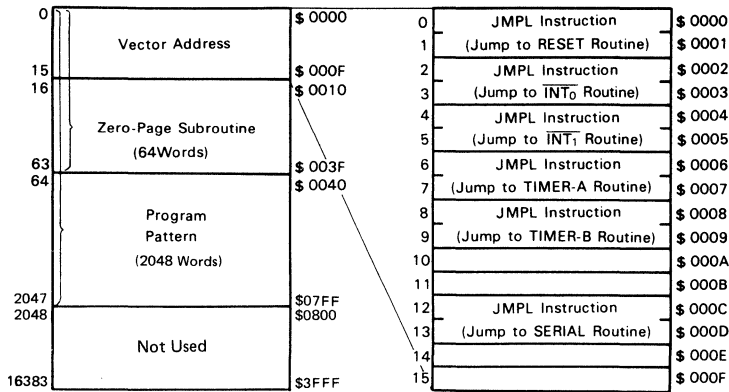
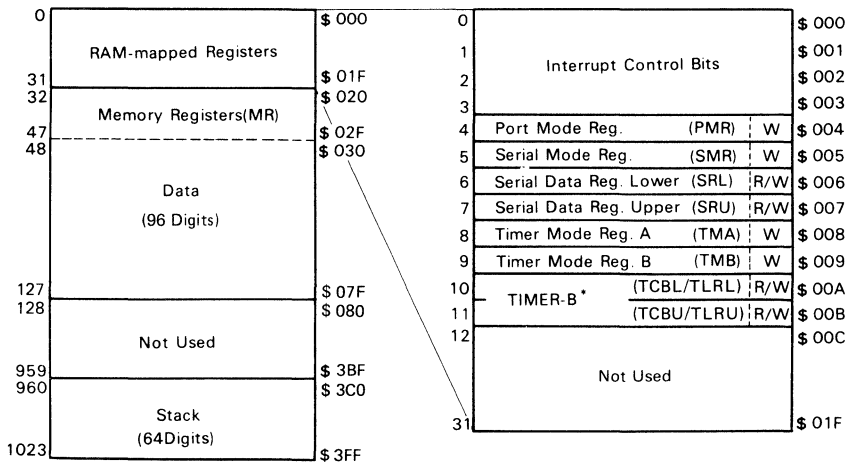


Fig. 1 ROM Memory Map

■ **RAM MEMORY MAP**

MCU includes 160 digits × 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits

and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



* Two registers are mapped on same address.

R :Read Only
W :Write Only
R/W:Read/Write

10	Timer/Event Counter B Lower (TCBL)	R	Timer Load Reg. Lower (TLRL)	W	\$ 00A
11	Timer/Event Counter B Upper (TCBU)	R	Timer Load Reg. Upper (TLRU)	W	\$ 00B

Fig. 2 RAM Memory Map

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of INT ₀)	IFO (IF of INT ₀)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of INT ₁)	IF1 (IF of INT ₁)	\$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	\$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	\$003

IF : Interrupt Request Flag
 IM : Interrupt Mask
 I/E : Interrupt Enable Flag
 SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invalid when "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

● **Interrupt Control Bit Area \$000 to \$003**

This area is used for interrupt controls, and is illustrated in Fig. 3. It is accessible only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software.

● **Special Register Area \$004 to \$00B**

Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

● **Data Area \$020 to \$07F**

16 digits of \$020 to \$02F are called memory register (MR) and accessible by LAMR and XMRA instructions.

● **Stack Area \$3C0 to \$3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.

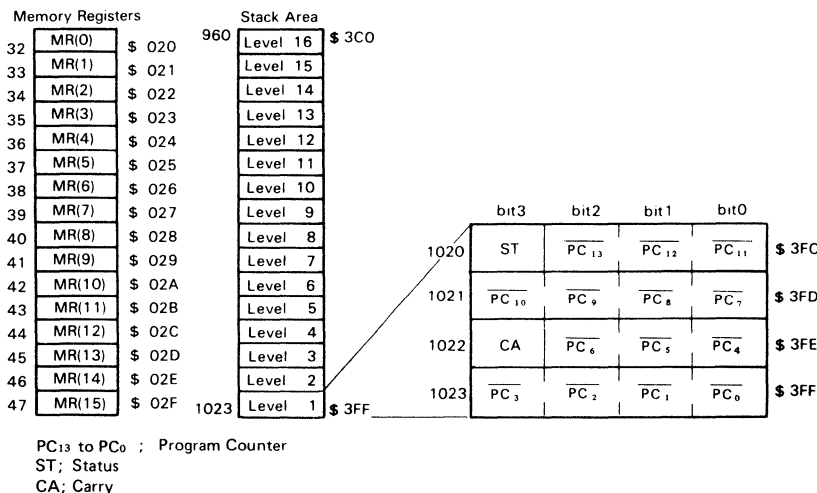


Fig. 4 Configuration of Memory Register, Stack Area and Stack Position



REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing. W Register is write only and cannot be read.

SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the

stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate \$3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

INTERRUPT

The MCU can be interrupted by five different sources: the external signals (INT_0 , INT_1), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on \$000 to \$003 of the RAM address and accessible by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

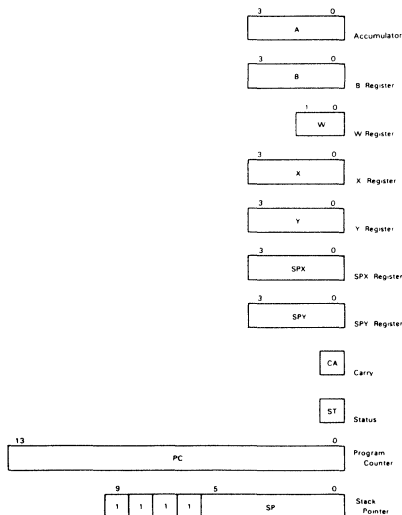


Fig. 5 Register and Flags

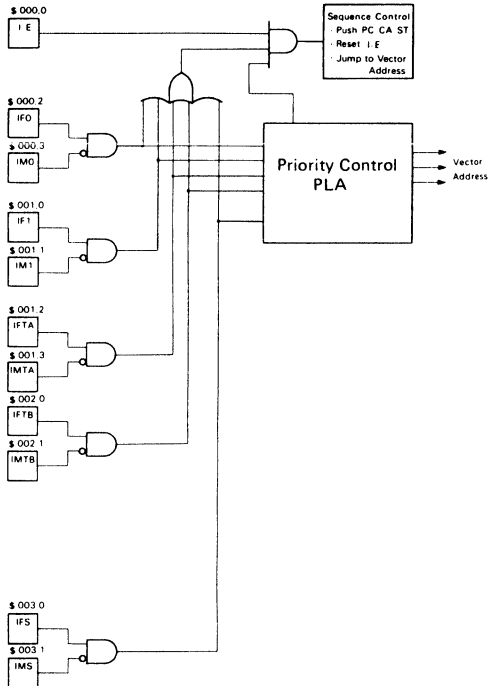


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset / Interrupt	Priority	Vector addresses
RESET	-	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
TIMER-A	3	\$0006
TIMER-B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt source	\overline{INT}_0	\overline{INT}_1	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IFO · \overline{IM}_0	1	0	0	0	0
IF1 · \overline{IM}_1	*	1	0	0	0
IFTA · \overline{IMTA}	*	*	1	0	0
IFTB · \overline{IMTB}	*	*	*	1	0
IFS · \overline{IMS}	*	*	*	*	1

* Don't care

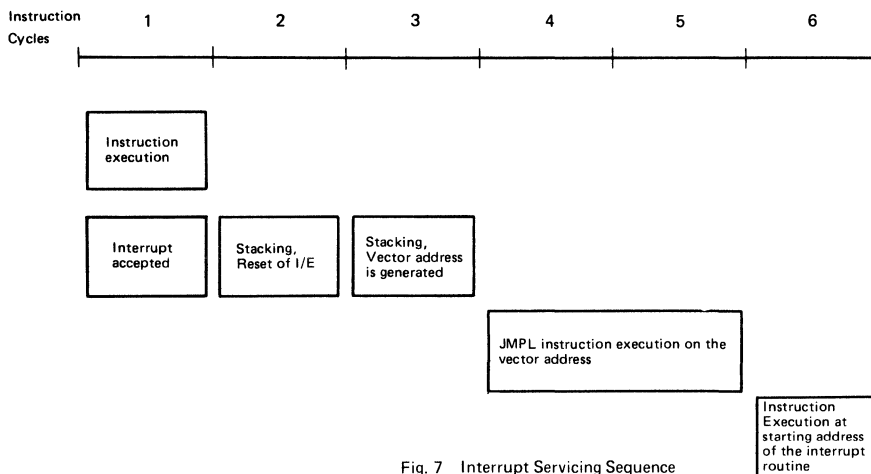


Fig. 7 Interrupt Servicing Sequence

● **Interrupt Enable Flag (I/E: \$000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

● **External Interrupt (\overline{INT}_0 , \overline{INT}_1)**

To use external interrupt, select R_{32}/\overline{INT}_0 , R_{33}/\overline{INT}_1 port for \overline{INT}_0 , \overline{INT}_1 mode by setting the Port Mode Register (PMR: \$004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 , \overline{INT}_1 inputs.

\overline{INT}_1 input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using \overline{INT}_1 as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted.

● **External Interrupt Request Flag (IF0: \$000,2, IF1: \$001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of \overline{INT}_0 , \overline{INT}_1 inputs respectively.

● **External Interrupt Mask (IM0: \$000,3, IM1: \$001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

● **Port Mode Register (PMR: \$004)**

The Port Mode Register is a 4-bit write-only register which controls the R_{32}/\overline{INT}_0 pin, R_{33}/\overline{INT}_1 pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to \$0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	R_{33}/\overline{INT}_1 pin
0	Used as R_{33} port input/output pin
1	Used as \overline{INT}_1 input pin

PMR bit 2	R_{32}/\overline{INT}_0 pin
0	Used as R_{32} port input/output pin
1	Used as \overline{INT}_0 input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

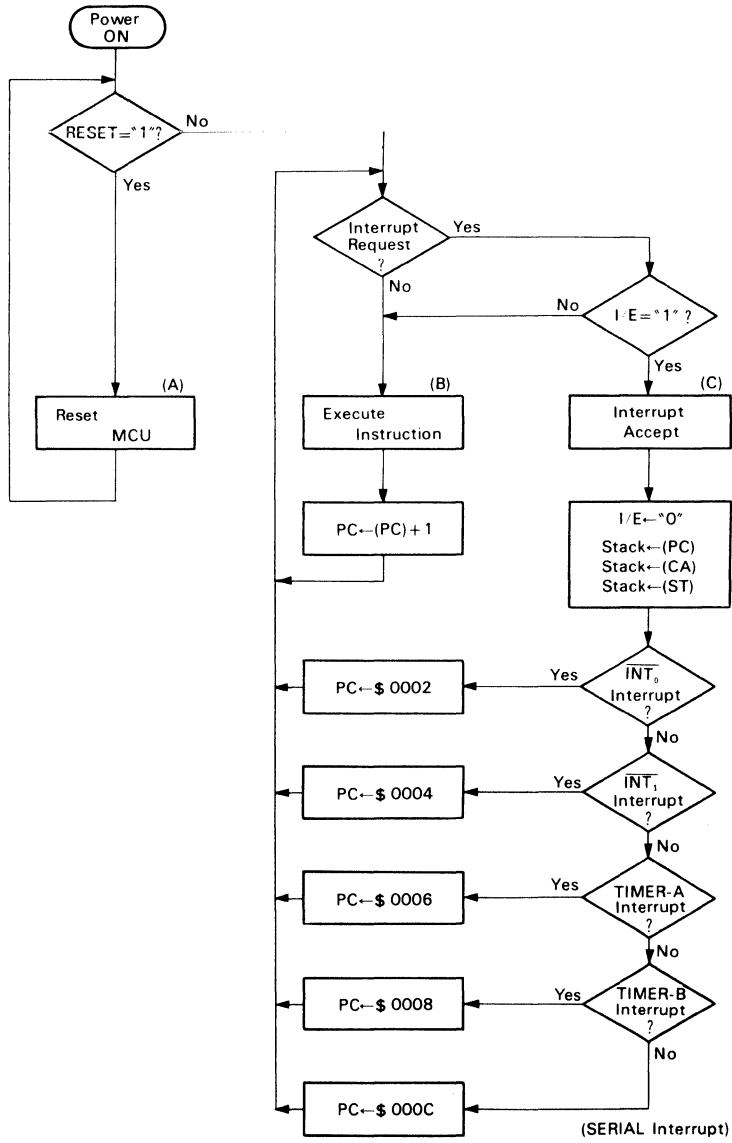


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin R_{40}/\overline{SCK} and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronously

ly with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to \$0 by STS instruction. It starts to count at the falling edge of the transfer clock (\overline{SCK}) signal and increments by one at the rising edge of the \overline{SCK} . When the Octal Counter is reset to \$0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

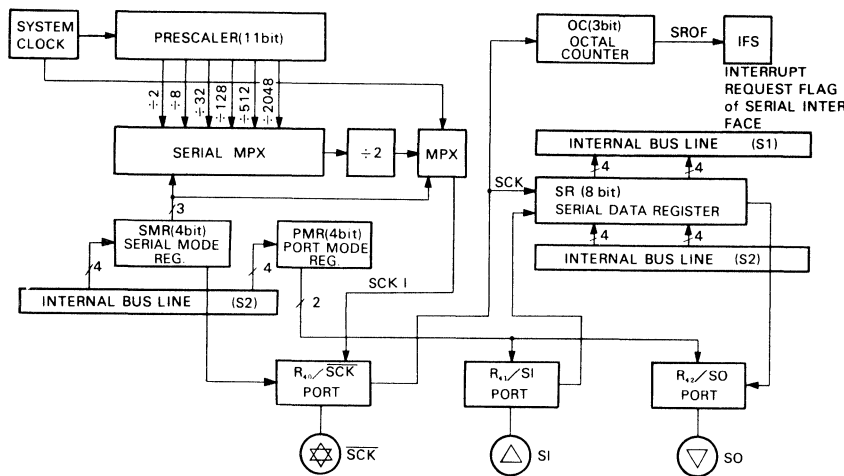


Fig. 9 Serial Interface Block Diagram

● Serial Mode Register (SMR: \$005)

The Serial Mode Register is a 4-bit write-only register. This register controls the R_{40}/\overline{SCK} and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to \$0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to \$0 by MCU reset.

● Serial Data Register (SRL: \$006, SRU: \$007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:\$006) and a high-order digit (SRU:\$007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR	R ₄₀ / $\overline{\text{SCK}}$
Bit 3	
0	Used as R ₄₀ port input/output pin
1	Used as $\overline{\text{SCK}}$ input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	R ₄₀ / $\overline{\text{SCK}}$ Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	$\overline{\text{SCK}}$ Output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{\text{SCK}}$ Output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{\text{SCK}}$ Output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{\text{SCK}}$ Output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{\text{SCK}}$ Output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{\text{SCK}}$ Output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{\text{SCK}}$ Output	System Clock	—	÷ 1
1	1	1	$\overline{\text{SCK}}$ Input	External Clock	—	—

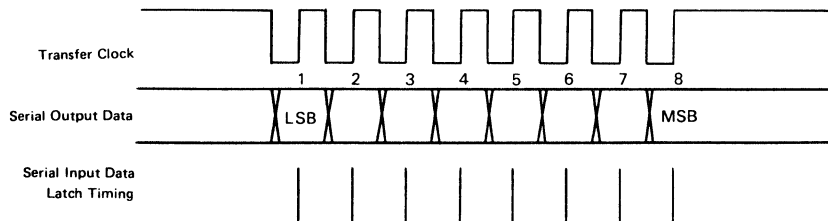


Fig. 10 Serial Interface I/O Timing Chart

● **SERIAL Interrupt Request Flag (IFS: \$003, 0)**

The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.

● **SERIAL Interrupt Mask (IMS: \$003, 1)**

The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

● **Selection of the Operation Mode**

Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10.

Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.

● **Operating State of Serial Interface**

The serial interface has 3 operating states as shown in Fig. 11. The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

● **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer

clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR Bit 3	PMR		Serial Interface Operating Mode
	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

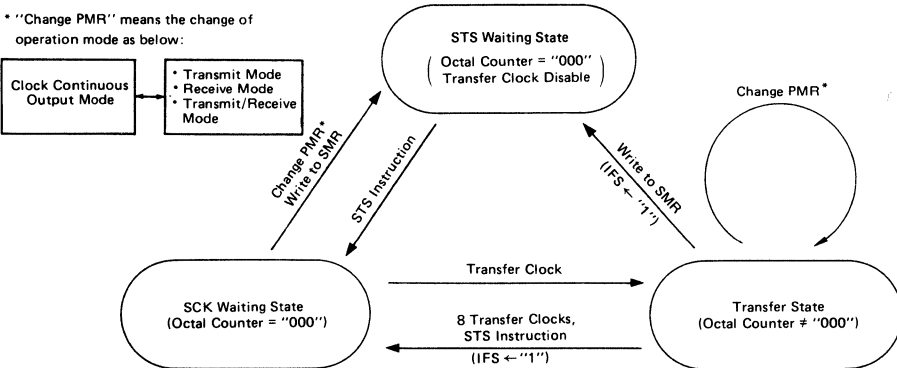


Fig. 11 Serial Interface Operation State

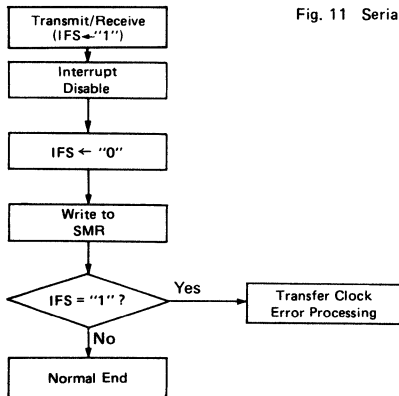


Fig. 12 Example of Transfer Clock Error Detection

■ **TIMER**

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B). Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

● **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler divide ratio of the clock signals are selected according to the content of the mode registers such as - Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

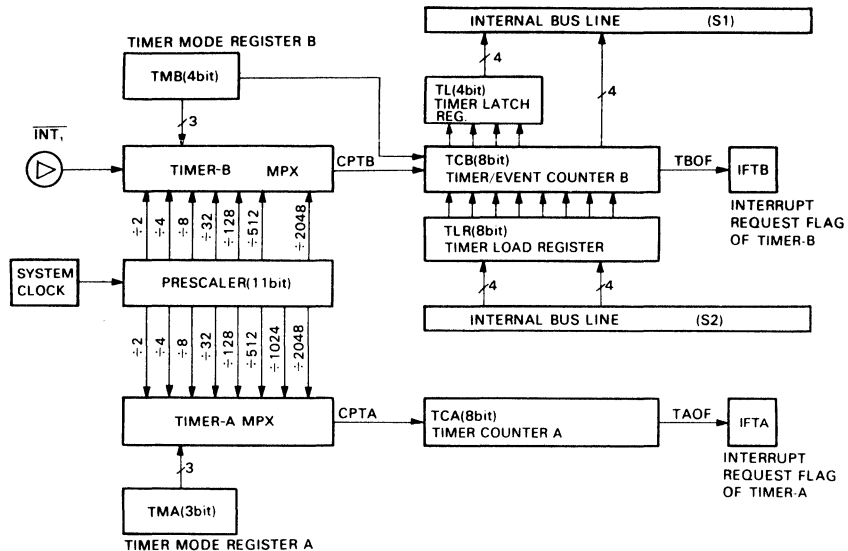


Fig. 13 Timer/Counter Block Diagram

● **TIMER-A Operation**

After **TIMER-A** is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after **TIMER-A** is counted up to \$FF, **TIMER-A** is set to \$00 again, and generating overflow output. This leads to setting **TIMER-A** Interrupt Request Flag (IFTA: \$001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to **TIMER-A** are selected by the Timer Mode Register A (TMA: \$008).

● **TIMER-B Operation**

Timer Mode Register B (TMB: \$009) is used to select the auto-reload function and the prescaler divide ratio of **TIMER-B** as the input clock source. When the external event input is used as an input clock signal to **TIMER-B**, select the R_{33}/\overline{INT}_1 as \overline{INT}_1 and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. **TIMER-B** counts up at every clock input signal. When the next clock signal is applied to **TIMER-B** after **TIMER-B** is set to \$FF, **TIMER-B** will be initialized again and generate overflow output. In this case if the auto-reload function is selected, **TIMER-B** is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, **TIMER-B** goes to \$00. **TIMER-B** Interrupt Request Flag (IFTB: \$002,0) will be set at this overflow output.

● **Timer Mode Register A (TMA: \$008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of **TIMER-A** clock input, as shown in Table 11.

The Timer Mode Register A is initialized to \$0 by MCU reset.

● **Timer Mode Register B (TMB: \$009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of **TIMER-B** and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to \$0 by MCU reset.

The operation mode of **TIMER-B** is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB		Auto-reload Function
Bit 3		
0		No
1		Yes

TMB			Prescaler Divide Ratio, Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

• **TIMER-B (TCBL: \$00A, TCBU: \$00B)
(TLRL: \$00A, TLRU: \$00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to \$00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading

the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

• **TIMER-A Interrupt Request Flag (IFTA: \$001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

• **TIMER-A Interrupt Mask (IMTA: \$001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

• **TIMER-B Interrupt Request Flag (IFTB: \$002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

• **TIMER-B Interrupt Mask (IMTB: \$002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

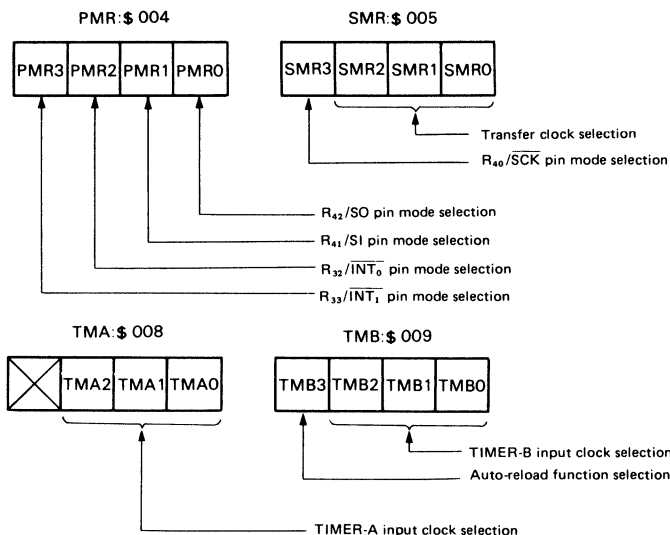


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

■ **INPUT/OUTPUT**

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins and 26 high voltage pins. Each standard pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS". And also each high voltage pin may have one of two mask options: (D) "Without pull-down MOS (PMOS

open drain)", or (E) "With pull-down MOS". As pull-down MOS is connected to internal V_{disp} line, select R_{A1}/V_{disp} pin as V_{disp} with mask option when at least one high voltage pin is selected as "With pull-down MOS" option.

When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 18.

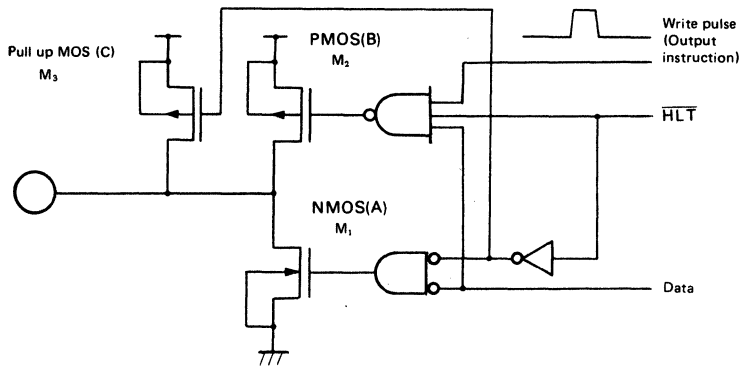
● **Output Circuit Operation of Standard Pins with "With pull-up MOS" Option**

Fig. 15 shows the circuit used in the standard pins with "with pull-up MOS" option.

By execution of the output instruction, the write pulse will be generated, and be applied to the addressed port. This pulse will turn "ON" the PMOS (B) to make the transient time shorten to obtain "High level", if the output data is changed from "0" to "1". In this case, the "write pulse" allows the PMOS (B) to turn "ON" as long as 1/8 instruction cycle. While "write pulse" is "0", pull-up MOS (C) may retain the output in high level.

The \overline{HLT} signal becomes "0" in stop mode, so that MOS (A) (B) (C) turn "OFF".

HMCS402C/HMCS402CL/HMCS402AC



MOS Buffer	Features	ON Resistance Value	
		HMCS402C, HMCS402AC	HMCS402CL
M_1		approx. 250 Ω	approx. 1k Ω
M_2		approx. 1k Ω	approx. 5k Ω
M_3		approx. 40k Ω to 160k Ω ($V_{CC} = 5V$)	approx. 75k Ω to 1M Ω ($V_{CC} = 3V$), approx. 40k Ω to 160k Ω ($V_{CC} = 5V$)

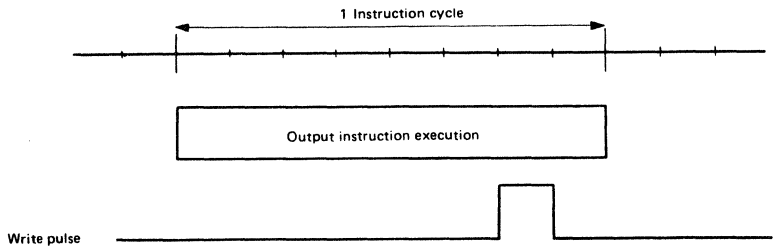


Fig. 15 Output Circuit Operation of Standard Pins with "with Pull-up MOS" Option

HMCS402C/HMCS402CL/HMCS402AC

Table 17 I/O Pin Circuit Type

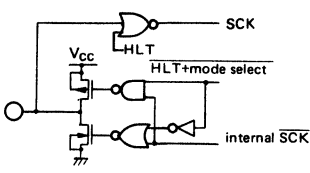
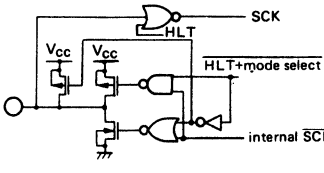
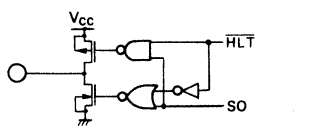
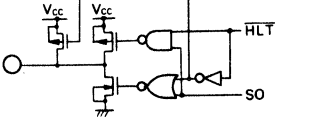
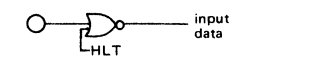
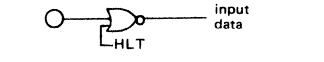
		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applied pins
Standard pins	I/O common pins				D ₀ ~ D ₃ , R ₃₀ ~ R ₃₃ , R ₄₀ ~ R ₄₃ , R ₅₀ ~ R ₅₃
	Output pins				R ₆₀ ~ R ₆₃ , R ₇₀ ~ R ₇₃ , R ₈₀ ~ R ₈₃
	Input pins				R ₉₀ ~ R ₉₃
High voltage pins	I/O common pins				D ₄ ~ D ₁₅ , R ₁₀ ~ R ₁₃ , R ₂₀ ~ R ₂₃
	Output pins				R ₀₀ ~ R ₀₃
	Input pins				R _{A0} , R _{A1} /V _{disp}

(Note). In the stop mode, HLT signal is "0" and I/O pins are in high impedance state.

(to be continued)



HMCS402C/HMCS402CL/HMCS402AC

	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applied pins
Standard pins	I/O common pins 		$\overline{\text{SCK}}$ (Note 2) (Output mode)
	Output pins 		SO
	Input pins 		$\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, SI, $\overline{\text{SCK}}$ (Note 2) (Input mode)

(Note 1) In the stop mode, $\overline{\text{HLT}}$ signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

(Note 2) If the MCU is interrupted by serial interface in the external clock input mode, the $\overline{\text{SCK}}$ terminal becomes input only.

Table 18 Data Input from Input/Output Common Pins

I/O pin circuit type		Possibility of Input	Available pin condition for input
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	"1"
	With pull-up MOS	Yes	"1"
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	"0"
	With pull-down MOS	Yes	"0"

● **D-port**

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

● **R-port**

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the

output-only and/or non-existing ports.

The R₃₂, R₃₃, R₄₀, R₄₁ and R₄₂ pins are also used as the $\overline{INT_0}$, INT₁, SCK, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

■ **RESET**

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

Table 19 Initial Value by MCU Reset

Items		Initial value by MCU reset	Contents	
Program counter (PC)		\$0000	Execute program from the top of ROM address.	
Status (ST)		"1"	Enable to branch with conditional branch instructions.	
Stack pointer (SP)		\$3FF	Stack level is 0.	
I/O pin output register	Standard pin	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input
		(C) CMOS	"1"	-
	High voltage pin	(D) Without pull-down MOS	"0"	Enable to input.
		(E) With pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)		"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)		"0"	No interrupt request.
	Interrupt Mask (IM)		"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)		"0000"	See Item "Port Mode Register".
	Serial Mode Register (SMR)		"0000"	See Item "Serial Mode Register".
	Timer Mode Register A (TMA)		"000"	See Item "Timer Mode Register A".
	Timer Mode Register B (TMB)		"0000"	See Item "Timer Mode Register B".
Timer/Counter, Serial interface	Prescaler		\$000	-
	Timer/Counter A (TCA)		\$00	-
	Timer/Event Counter B (TCB)		\$00	-
	Timer Load Register (TLR)		\$00	-
	Octal Counter		"000"	-

(Note) MCU reset affects to the rest of registers as follows:

Item	After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry (CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator (A)		
B Register (B)		
W Register (W)		
X/SPX Registers (X/SPX)		
Y/SPY Registers (Y/SPY)		
Serial Data Register (SR)	Same as above	Same as above
RAM	The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above



HMCS402C/HMCS402CL/HMCS402AC

INTERNAL OSCILLATOR CIRCUIT

Fig. 16 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal oscillator, ceramic

filter oscillator, or resistor oscillator as shown in Table 20. In any cases, external clock operation is available.

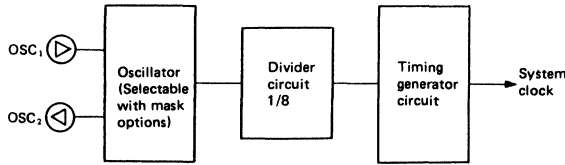


Fig. 16 Internal Oscillator Circuit

Internal Oscillator Circuit Mask Option

		HMCS402C	HMCS402CL	HMCS402AC
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○
	Resistor	○	—	—
Divider	1/8	○	○	○

● Oscillator Circuit

Table 20 Examples of Oscillator Circuit

	Circuit configuration	Circuit constants		
		HMCS402C	HMCS402CL	HMCS402AC
External clock operation				
Resistor oscillator		$R_f = 20k\Omega \pm 2\%$	/	/
Ceramic filter oscillator		Ceramic filter CSA4.00MG (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$	Ceramic filter CSA2.000MK (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$	Ceramic filter CSA6.00MG (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$
Crystal oscillator	<p style="text-align: center;">AT cut parallel resonance crystal</p>	$R_f : 1M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 60\Omega \text{ max.}$ $f : 2.0 \sim 4.5MHz$	/	$R_f : 1M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 100\Omega \text{ max.}$ $f : 2.0 \sim 6.2MHz$
	<p style="text-align: center;">GT cut parallel resonance crystal</p>	/	$R_f : 2M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 100\Omega \text{ max.}$ $f : 2.0 \sim 2.25MHz$	/

- (Note 1) On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
- (Note 2) Wiring among OSC₁, OSC₂ and elements should be as short as possible, and never cross the other wirings. Refer to the recommendable layout of crystal and ceramic filter.

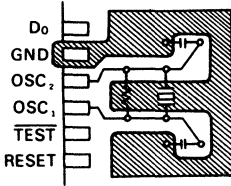


Fig. 17 Recommendable Layout of Crystal and Ceramic Filter

■ **LOW POWER DISSIPATION MODE**

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 18 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/Output pin	Timer/Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ^{*1)}	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ^{*1)}	Stop	Retained	High ^{*2)} impedance	Stop	RESET Input

- *1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 19.
- *2) A high voltage pin with a pull-down MOS option is pulled down to the V_{diss} power supply by the pull-down MOS. As the MOS is ON, a pull-down MOS current flows when a voltage difference between the pin and the V_{diss} voltage exists. This is the additional current to the current dissipation in Stop Mode (I_{stop}).
- *3) As a I/O circuit is active, a I/O current possibly flows according to the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (I_{SBY1} , I_{SBY2}).

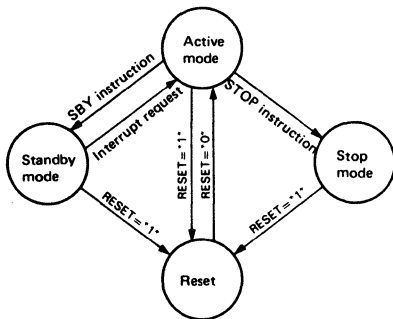


Fig. 18 MCU Operation Mode Transition

● **Standby Mode**

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/

counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 19 shows the flowchart of the Standby Mode.

● **Stop Mode**

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 20, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode. The other hand, Accumulator, B Register, W Register, X/SPX Registers, Y/SPY Registers, Carry and Serial Data Register don't retain the contents.

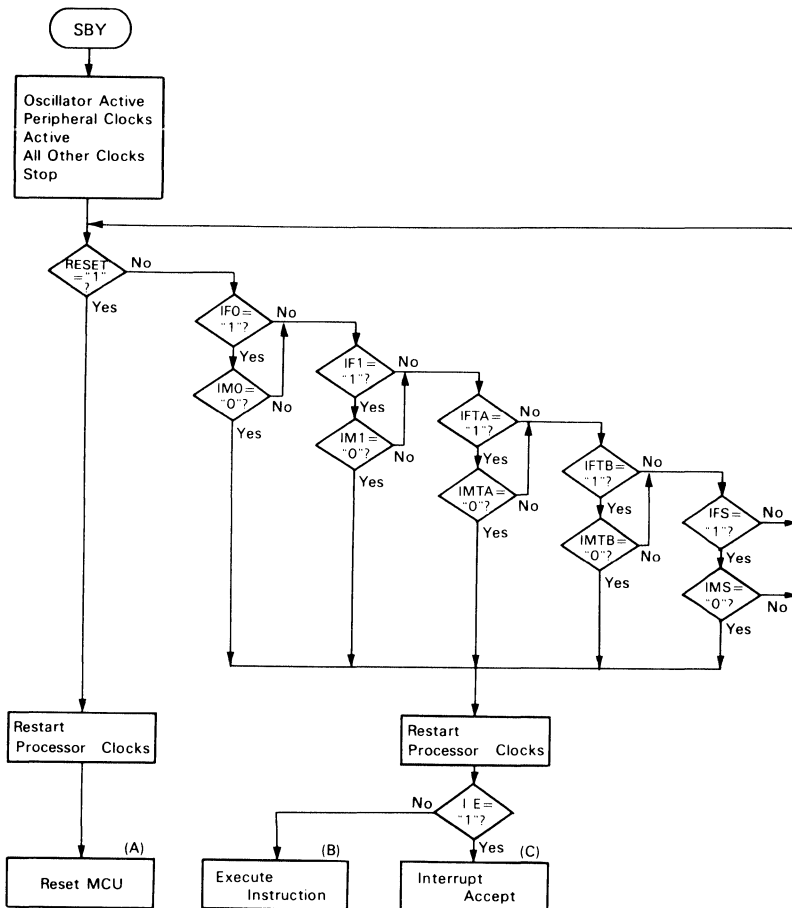


Fig. 19 MCU Operating Flowchart

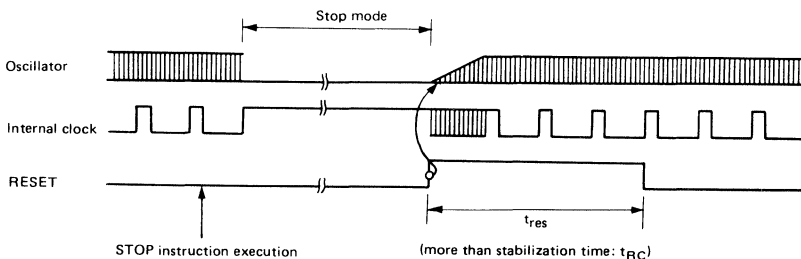


Fig. 20 Timing Chart of Recovering from Stop Mode

HMCS402C/HMCS402CL/HMCS402AC

RAM ADDRESSING MODE

As shown in Fig. 21, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

Register Indirect Addressing

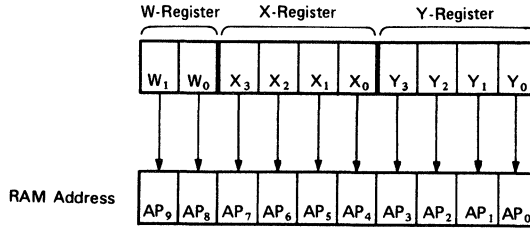
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

Direct Addressing

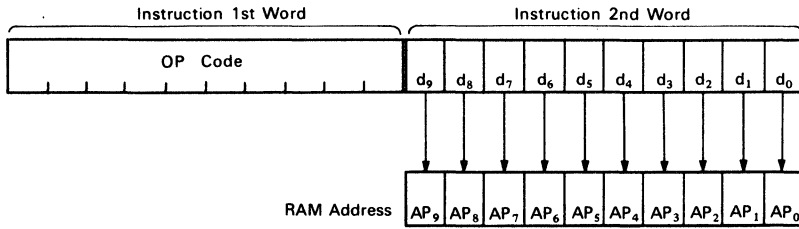
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

Memory Register Addressing

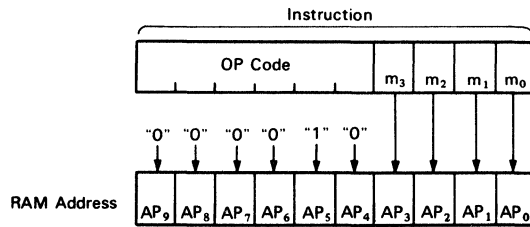
The Memory Register Addressing can access 16 digits (Memory Register: MR) from \$020 to \$02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 21 RAM Addressing Mode

■ ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 22.

● Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMWL, BRL or CALL instruction. These instruction replace 14-bit program counter (PC₁₃ to PC₀) with 14-bit immediate data.

● Current Page Addressing Mode

ROM memory space is divided into 256 words in each page starting from 80000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC₇ to PC₀) with 8-bit

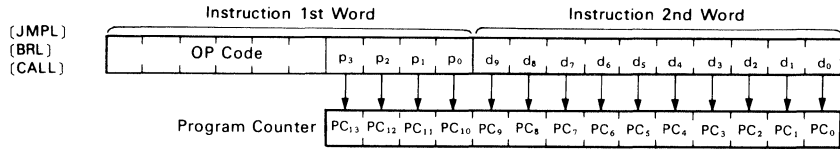
immediate data. The branch destination by BR instruction on the boundary between pages is given in Fig. 24.

● Zero Page Addressing Mode

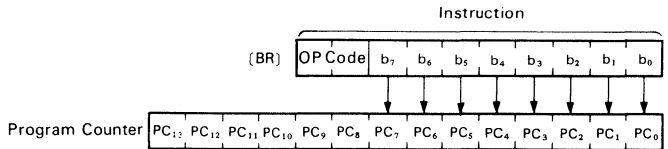
The program branches to the zero page subroutine area, which is located on the address from 80000 to 8003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC₅ to PC₀) and "0's" are placed in high-order eight bits (PC₁₃ to PC₆).

● Table Data Addressing

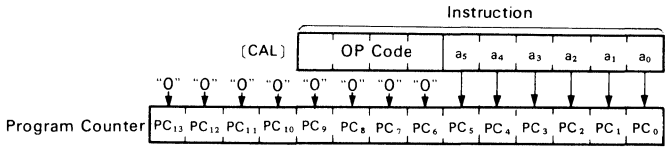
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



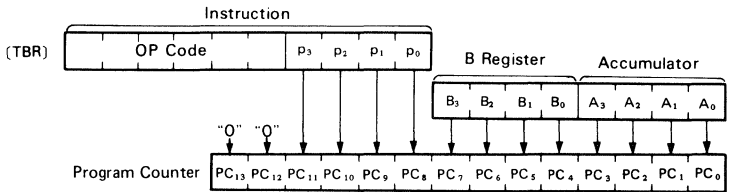
(a) Direct Addressing



(b) Current Page Addressing

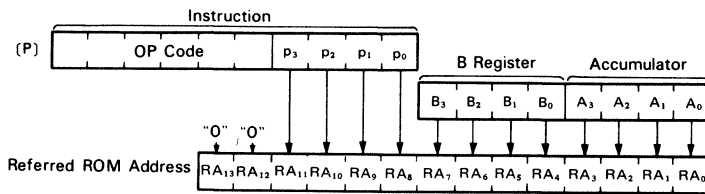


(c) Zero Page Addressing

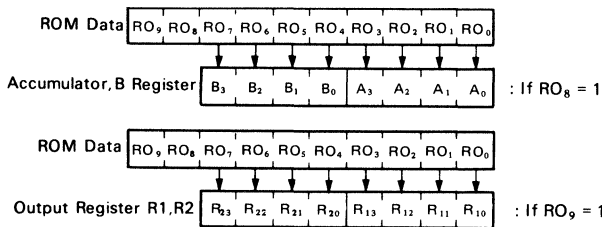


(d) Table Data Addressing

Fig. 22 ROM Addressing Mode



(a) Address Designation



(b) Pattern Output

Fig. 23 P Instruction

● P Instruction

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred

ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

● Description of the branch destination on page boundary

When BR is on page boundary (256n + 255), BR instruction transfers the contents of PC to the next page with hardware architecture. Therefore, the program branches to the next page when using BR on page boundary.

The HMCS400 series cross macro assembler has automatic paging facility for ROM page.

■ INSTRUCTION SET

The HMCS402C/CL/AC provide 99 instructions. These instructions are classified into 10 groups as follows;

- (1) Immediate Instruction
- (2) Register-to-Register Instruction
- (3) RAM Address Instruction
- (4) RAM Register Instruction
- (5) Arithmetic Instruction
- (6) Compare Instruction
- (7) RAM Bit Manipulation Instruction
- (8) ROM Address Instruction
- (9) Input/Output Instruction
- (10) Control Instruction

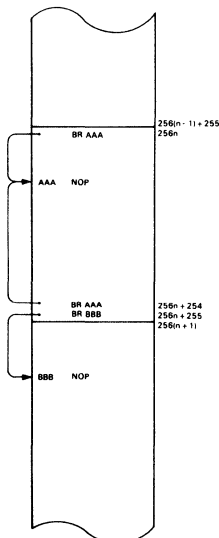


Fig. 24 The Branch Destination by BR Instruction on the Boundary between Pages

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y + 1 → Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y + 1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y - 1 → Y	NB	1/1
Add A to Y	AAY	0 0 0 1 0 1 0 1 0 0	Y + A → Y	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	Y - A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X ↔ SPX) (Y ↔ SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X ↔ SPX) (Y ↔ SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X ↔ SPX) (Y ↔ SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X ↔ SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X ↔ SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X ↔ SPX) (Y ↔ SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X ↔ SPX) (Y ↔ SPY)		1/1

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Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY (X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A + i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B - 1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M + A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M + A + CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M - A - CA → A NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M - A - CA → A NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 1 1 0 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2



Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i / M	NZ	1 / 1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i / M	NZ	2 / 2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1 / 1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A / M	NZ	2 / 2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B / M	NZ	1 / 1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1 / 1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1 / 1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2 / 2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1 / 1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2 / 2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1 / 1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1 / 1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₃ n ₀	1 → M(n)		1 / 1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₃ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2 / 2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₃ n ₀	0 → M(n)		1 / 1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₃ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2 / 2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₃ n ₀		M(n)	1 / 1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₃ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		M(n)	2 / 2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1 / 1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		1	2 / 2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀			2 / 2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₃ a ₂ a ₁ a ₀		1	1 / 2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		1	2 / 2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1 / 1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1 / 3
Return from interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA RESTORE	ST	1 / 3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1 / 1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1 / 1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1 / 1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1 / 1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1 / 1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1 / 1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1 / 1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1 / 1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1 / 1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1 / 1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1 / 2

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Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1 / 1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1 / 1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1 / 1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1 / 1

Table 32. Op-Code Map

RB	0																1																					
	R9	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F				
			0	NOP	XSP	XSP	XSP	AN	EM			AM			ORM								ANMC			AMD				ORMC								
			1	RTN	RTN		AEM				AMC				EORM								ALEM			AMCD				ORMC								
			2					INEM				i(4)											INEMD				i(4)											
			3					ILEM				i(4)												ILEMD				i(4)										
			4	LBM(XY)		BNEM				LAR			IB			COMB							OR			STS			SBY	STOP								
			5	LMAY(X)		AYY				LASPI			IY													JMPL	p(4)											
			6	NEGA		RED				LASPI						TC										CALL	p(4)											
			7				YNEI				i(4)																	BRL	p(4)									
			8	XMA(XY)			SEM		n(2)			REM		n(2)			TM		n(2)			XMAD			SEMD		n(2)			REMD		n(2)			TMD		n(2)	
			9	LAM(XY)			LMA		XY			SMC			ANM								LAMD			LAMD			SMCD			ANMD						
			A	ROTR	ROTL			DAA				DAS				LAY										LMID		i(4)										
			B				TBR				p(4)																	P	p(4)									
			C	XMB(XY)		BLEM				LBA																												
			D	LMADY(X)		SYX				LVA																												
			E	TD		SED				LXA						REC											CALL										a(6)	
			F	LWI				i(2)																														
			0				LBI				i(4)																											
			1				LYI				i(4)																											
			2				LXI				i(4)																											
			3				LAI				i(4)																											
			4				LBR				m(4)																											
			5				LAR				m(4)																											
			6				REDD				m(4)																											
			7				LAMR				m(4)																											
			8				AI				i(4)																											
			9				LMHIY				i(4)																											
			A				TDD				m(4)																											
			B				ALEI				i(4)																											
			C				LRB				m(4)																											
			D				LRA				m(4)																											
			E				SEDD				m(4)																											
			F				XMRA				m(4)																											

... 1-word/2-cycle Instruction
 ... 1-word/3-cycle Instruction
 ... RAM Direct Address Instruction (2-word/2-cycle)
 ... 2-word/2-cycle Instruction



HMCS402C/HMCS402CL/HMCS402AC

**HMCS402C/CL/AC
MASK OPTION LIST**

5V Operation	: <input type="checkbox"/> HMCS402C
3V Operation	: <input type="checkbox"/> HMCS402CL
High Speed Operation	: <input type="checkbox"/> HMCS402AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

* Please enter check marks in (■, X, √).

(1) I/O Option

Note (I/O options masked by ■ are not available.)

PIN	INPUT/OUTPUT	I/O OPTION					PIN	INPUT/OUTPUT	I/O OPTION					
		A	B	C	D	E			A	B	C	D	E	
D ₀	Input/Output						R3	R ₃₀	Input/Output					
D ₁	Input/Output							R ₃₁	Input/Output					
D ₂	Input/Output							R ₃₂	Input/Output					
D ₃	Input/Output						R ₃₃	Input/Output						
D ₄	Input/Output						R ₄₀	Input/Output						
D ₅	Input/Output						R ₄₁	Input/Output						
D ₆	Input/Output						R ₄₂	Input/Output						
D ₇	Input/Output						R ₄₃	Input/Output						
D ₈	Input/Output						R ₅₀	Input/Output						
D ₉	Input/Output						R ₅₁	Input/Output						
D ₁₀	Input/Output						R ₅₂	Input/Output						
D ₁₁	Input/Output						R ₅₃	Input/Output						
D ₁₂	Input/Output						R ₆₀	Output						
D ₁₃	Input/Output						R ₆₁	Output						
D ₁₄	Input/Output						R ₆₂	Output						
D ₁₅	Input/Output						R ₆₃	Output						
							R ₇₀	Output						
							R ₇₁	Output						
							R ₇₂	Output						
							R ₇₃	Output						
							R ₈₀	Output						
							R ₈₁	Output						
							R ₈₂	Output						
							R ₈₃	Output						
							R ₉₀	Input						
							R ₉₁	Input						
							R ₉₂	Input						
							R ₉₃	Input						
							RA ₀	Input						
							RA ₁	Input						

- * Please enter "C" in applicable item for I/O option selection.
- A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
- C: CMOS (not be used as Input) D: Without Pull-down MOS (PMOS Open Drain) E: With Pull-down MOS

(2) RA₁/V_{disp}

RA ₁ /V _{disp}	
<input type="checkbox"/> RA ₁ : Without Pull-down MOS (D)	
<input type="checkbox"/> V _{disp}	

(3) Package

Package	
<input type="checkbox"/> DP-64S (shrink package)	
<input type="checkbox"/> FP-64	

* Please enter check marks (■, X, √) in applicable item. * Please enter check marks (■, X, √) in applicable item.

Note) RA₁/V_{disp} has to be selected as V_{disp} pin except for the case that all High Pins are option D.

(4) Divider (DIV)

Clock Divide Ratio	
<input checked="" type="checkbox"/> Divided-by-8	

(5) ROM Code Media

ROM Code Media	
<input type="checkbox"/> EPROM: Emulator Type	
<input type="checkbox"/> EPROM: EPROM On-Package Microcomputer Type	

Check List of Application

(A) Oscillator (CPG option)

CPG Option	<input type="checkbox"/> 402C (5V Operation)	<input type="checkbox"/> 402CL (3V Operation)	<input type="checkbox"/> 402AC (High Speed Operation)
	<input type="checkbox"/> Resistor (R _f = 20kΩ±2%)	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> Crystal	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock

* Please enter check marks (■, X, √) in applicable item.



HMCS404C(HD614042)/ HMCS404CL(HD614045)/ HMCS404AC(HD614048)

DESCRIPTION

The HMCS404C/CL/AC are CMOS 4-bit single-chip microcomputers which are members of the HMCS400 series.

The HMCS404C/CL/AC have efficient and powerful architecture and its software is very similar to the HMCS40 series.

These microcomputers provide variety of on-chip resources such as ROM, RAM, I/O, two timer/counters and a serial interface to perform in wide users' applications. I/O pins of HMCS404C/CL/AC are able to drive fluorescent display tube directly.

The HMCS404CL is able to operate in low voltage and has the characteristics of wide-range operation voltage.

The HMCS404AC is a high-speed version of HMCS404C.

■ HARDWARE FEATURES

- 4-bit Architecture
- 4,096 Words x 10-bit ROM
- 256 Digits x 4-bit RAM
- 58 I/O Pins, Including 26 High Voltage I/O Pins (40V Max)
- Two Timer/Counters
 - 11-bit Prescaler
 - 8-bit Free Running Timer
 - 8-bit Auto-Reload Timer/Event Counter
- Clock Synchronous 8-bit Serial Interface
- Five Interrupts
 - External 2
 - Timer/Counter 2
 - Serial Interface 1
- Subroutine Stack
 - Up to 16 Levels Including Interrupt
- Two Low Power Dissipation Modes
 - Standby — Stops instruction execution while keeping clock oscillation and interrupt functions in operation
 - Stop — Stops instruction execution and clock oscillation while retaining RAM data
- On-Chip Oscillator
 - External Connection of Crystal, Ceramic Filter or Resistor (externally drivable)
 - (Resistor oscillator is available only to the HMCS404C)

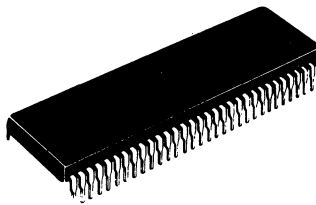
■ SOFTWARE FEATURES

- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single-word instructions
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logical Arithmetic Operation
- Pattern Generation — Table Look Up Capability —
- Bit Manipulation for Both RAM and I/O

■ PROGRAM DEVELOPMENT SUPPORT TOOLS

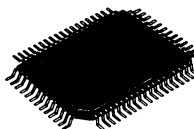
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

HMCS404C, HMCS404CL, HMCS404AC



(DP-64S)

HMCS404C, HMCS404CL, HMCS404AC



(FP-64)

- EPROM On Package Microcomputer; HD614P080S

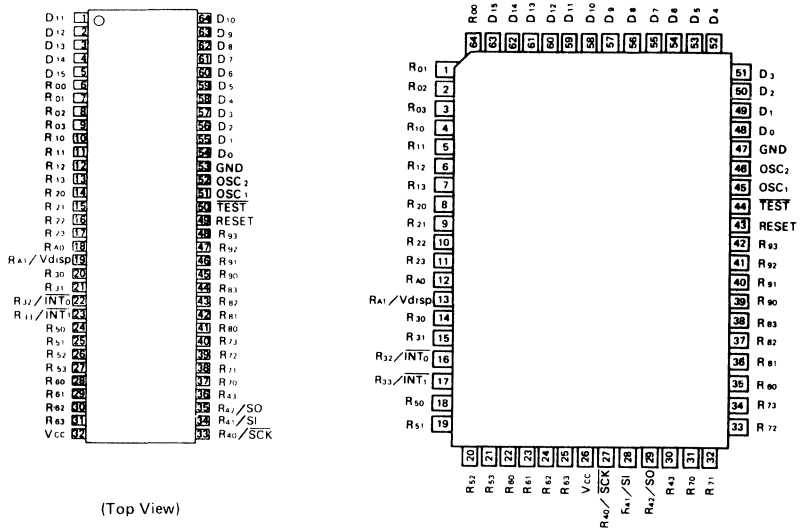
Mask options are fixed as follows:

- I/O pin : Open Drain
- Oscillator : Crystal Oscillator or Ceramic Filter Oscillator (externally drivable)
- Divider : Divided-by-8

■ HMCS404C/CL/AC CLASSIFICATIONS

Type Name	HMCS404C (HD614042)	HMCS404CL (HD614045)	HMCS404AC (HD614048)
Item			
V _{CC} (V)	4 ~ 6	2.7 ~ 6	4.5 ~ 6
Minimum Instruction Execution Time (μs)	2	4	1.33

■ PIN ARRANGEMENT



HMCS404C/HMCS404CL/HMCS404AC

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
		4	mA	9, 10
Maximum Output Current	$-I_O$	6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.

(Note 2) All voltages are with respect to GND.

(Note 3) Applied to standard pins.

(Note 4) Applied to high voltage pins.

(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.

(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.

(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.

(Note 8) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.

(Note 10) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 11) Applied to $R0 \sim R2$.

(Note 12) Applied to $D_4 \sim D_{15}$.



HMCS404C/HMCS404CL/HMCS404AC

■ **HMCS404C ELECTRICAL CHARACTERISTICS**

- **DC CHARACTERISTICS** ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Input "High" Voltage	V_{IH}	RESET, SCK, INT ₀ , INT ₁		$0.7V_{CC}$	–	$V_{CC}+0.3$	V		
		SI		$0.7V_{CC}$	–	$V_{CC}+0.3$	V		
		OSC ₁		$V_{CC}-0.5$	–	$V_{CC}+0.3$	V		
Input "Low" Voltage	V_{IL}	RESET, SCK, INT ₀ , INT ₁		–0.3	–	$0.22V_{CC}$	V		
		SI		–0.3	–	$0.22V_{CC}$	V		
		OSC ₁		–0.3	–	0.5	V		
Output "High" Voltage	V_{OH}	SCK, SO	$-I_{OH} = 1.0$ mA	$V_{CC}-1.0$	–	–	V		
			$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	–	–	V		
Output "Low" Voltage	V_{OL}	SCK, SO	$I_{OL} = 1.6$ mA	–	–	0.4	V		
Input/Output Leakage Current	I_{IL}	RESET, SCK, INT ₀ , INT ₁ , SI, SO, OSC ₁	$V_{in} = 0V$ to V_{CC}	–	–	1	μA	1	
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC}=5V$	Crystal or Ceramic Filter Oscillator Option $f_{OSC} = 4MHz$	–	–	2.0	mA	2, 6
				Resistor Oscillator Option $f_{OSC} = 4MHz$	–	–	2.4	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Oscillator Option $f_{OSC} = 4MHz$	–	–	1.2	mA	3, 6
				Resistor Oscillator Option $f_{OSC} = 4MHz$	–	–	1.6	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Oscillator Option $f_{OSC} = 4MHz$	–	–	0.9	mA	4, 6
				Resistor Oscillator Option $f_{OSC} = 4MHz$	–	–	1.3	mA	4, 6
Current Dissipation in Stop Mode	I_{STOP}	V_{CC}	$V_{in}(\overline{TEST}) = V_{CC}-0.3V$ to V_{CC} $V_{in}(RESET) = 0V$ to $0.3V$	–	–	10	μA	5	
Stop Mode Retain Voltage	V_{STOP}	V_{CC}		2	–	–	V		

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- (Note 1) Pull-up MOS current and output buffer current are excluded.
 (Note 2) The MCU is in the reset state. The input/output current does not flow.
 Test Conditions: MCU state;
 Pin state;
 - Reset state in Operation Mode
 - RESET, TEST ... V_{CC} voltage
 - D₀~D₃, R3~R9 ... V_{CC} voltage
 - D₄~D₁₅, R0~R2, R_{AD}, RA1 ... V_{disp} voltage
- (Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.
 Test Conditions: MCU state;
 Pin state;
 - Standby Mode
 - Input/Output; Reset state
 - TIMER-A; ±2 prescaler divide ratio
 - TIMER-B; ±2 prescaler divide ratio
 - SERIAL Interface ; Stop
 - RESET ... GND voltage
 - TEST ... V_{CC} voltage
 - D₀~D₃, R3~R9 ... V_{CC} voltage
 - D₄~D₁₅, R0~R2, R_{AD}, RA1 ... V_{disp} voltage
- (Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.
 Test Conditions: MCU state;
 Pin state;
 - Standby Mode
 - Input/Output; Reset state
 - TIMER-A; ±2048 prescaler divide ratio
 - TIMER-B; ±2048 prescaler divide ratio
 - SERIAL Interface ; Stop
 - RESET ... GND voltage
 - TEST ... V_{CC} voltage
 - D₀~D₃, R3~R9 ... V_{CC} voltage
 - D₄~D₁₅, R0~R2, R_{AD}, RA1 ... V_{disp} voltage
- (Note 5) Pull-down MOS current is excluded.
 (Note 6) When f_{osc}=x[MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value (f}_{\text{osc}}=x[\text{MHz}]) = \frac{x}{4} \times \text{max. value (f}_{\text{osc}}=4[\text{MHz}])$$

• **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
 (V_{CC} = 4V to 6V, GND = 0V, V_{disp} = V_{CC} -40V to V_{CC}, Ta = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₀ ~ D ₃ , R3 ~ R5, R9		0.7V _{CC}	—	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₀ ~ D ₃ , R3 ~ R5, R9		-0.3	—	0.22V _{CC}	V	
Output "High" Voltage	V _{OH}	D ₀ ~ D ₃ , R3 ~ R8	-I _{OH} = 1.0 mA	V _{CC} -1.0	—	—	V	1
		D ₀ ~ D ₃ , R3 ~ R8	-I _{OH} = 0.01 mA	V _{CC} -0.3	—	—	V	1
Output "Low" Voltage	V _{OL}	D ₀ ~ D ₃ , R3 ~ R8	I _{OL} = 1.6 mA	—	—	0.4	V	
Input/Output Leakage Current	I _{IL}	D ₀ ~ D ₃ , R3 ~ R9	V _{in} = 0V to V _{CC}	—	—	1	μA	2
Pull-Up MOS Current	-I _P	D ₀ ~ D ₃ , R3 ~ R9	V _{CC} = 5V V _{in} = 0V	30	60	120	μA	3

- (Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.
 (Note 2) Pull-up MOS current and output buffer current are excluded.
 (Note 3) Applied to I/O pins with "with Pull-up MOS" selected by mask option.



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● **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
 ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC}-40$	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH}=15mA$, $V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH}=9mA$	$V_{CC}-2.0$	—	—	V	
		R0 ~ R2	$-I_{OH}=3mA$, $V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	—	—	V	
			$-I_{OH}=1.8mA$	$V_{CC}-2.0$	—	—	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	—	—	$V_{CC}-37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC} - 40V$	—	—	$V_{CC}-37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	—	—	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

(Note 1) Applied to I/O pins with "with Pull-down MOS" selected by mask option.

(Note 2) Applied to I/O pins with "without Pull-down MOS (PMOS Open Drain)" selected by mask option.

(Note 3) Pull-down MOS current and output buffer current are excluded.

(Note 4) Applied to I/O pins with "with Pull-down MOS" selected by mask option.



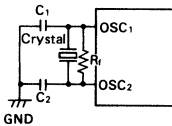
HMCS404C/HMCS404CL/HMCS404AC

● AC CHARACTERISTICS ($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz		
	Instruction Cycle Time	t_{cyc}		1.78	2	20	μs		
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂	—	—	20	ms	1	
Resistor Oscillator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	$R_f=20k\Omega\pm 2\%$	1.8	3.0	4.2	MHz	
	Instruction Cycle Time	t_{cyc}		$R_f=20k\Omega\pm 2\%$	1.9	2.66	4.44	μs	
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂	$R_f=20k\Omega\pm 2\%$	—	—	0.5	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC ₁	0.4	—	4.5	MHz	2	
	External Clock "High" Level Width	t_{CPH}	OSC ₁	100	—	—	ns	2	
	External Clock "Low" Level Width	t_{CPL}	OSC ₁	100	—	—	ns	2	
	External Clock Rise Time	t_{CPr}	OSC ₁	—	—	20	ns	2	
	External Clock Fall Time	t_{CPf}	OSC ₁	—	—	20	ns	2	
	Instruction Cycle Time	t_{cyc}			1.78	—	20	μs	2
INT ₀ "High" Level Width	t_{I0H}	INT ₀		2	—	—	t_{cyc}	3	
INT ₀ "Low" Level Width	t_{I0L}	INT ₀		2	—	—	t_{cyc}	3	
INT ₁ "High" Level Width	t_{I1H}	INT ₁		2	—	—	t_{cyc}	3	
INT ₁ "Low" Level Width	t_{I1L}	INT ₁		2	—	—	t_{cyc}	3	
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4	
Input Capacitance	C_{in}	all pins	$f=1MHz$ $V_{in}=0V$	—	—	15	pF		
RESET Fall Time	t_{RSTf}			—	—	20	ms	4	

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.0V at "Power-on", or after RESET input level goes to "High" by resetting to quit the stop mode by MCU reset on the circuits below. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.

Crystal oscillator



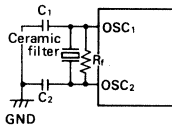
Crystal: 4.194304MHz NC-18C (Nihon Denpa Kogyo)

$R_f : 1M\Omega \pm 2\%$

$C_1 : 22pF \pm 20\%$

$C_2 : 22pF \pm 20\%$

Ceramic filter oscillator



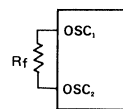
Ceramic filter: CSA4.00MG (Murata)

$R_f : 1M\Omega \pm 2\%$

$C_1 : 30pF \pm 20\%$

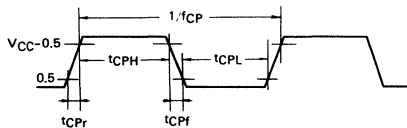
$C_2 : 30pF \pm 20\%$

Resistor oscillator

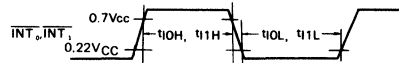


$R_f : 20k\Omega \pm 2\%$

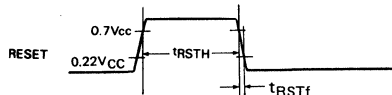
(Note 2)



(Note 3)



(Note 4)



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● SERIAL INTERFACE TIMING CHARACTERISTICS

($V_{CC} = 4V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

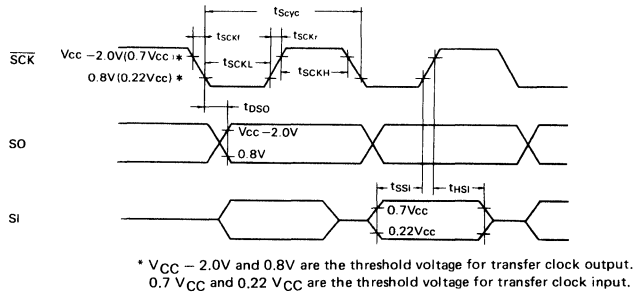
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Seyc}	SCK	(Note 2)	1	—	—	t_{eyc}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	SCK	(Note 2)	0.5	—	—	t_{seyc}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	SCK	(Note 2)	0.5	—	—	t_{seyc}	1, 2
Transfer Clock Rise Time	t_{SCKr}	SCK	(Note 2)	—	—	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	SCK	(Note 2)	—	—	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

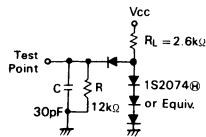
- At Transfer Clock Input

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{Seyc}	SCK		1	—	—	t_{eyc}	1
Transfer Clock "High" Level Width	t_{SCKH}	SCK		0.5	—	—	t_{seyc}	1
Transfer Clock "Low" Level Width	t_{SCKL}	SCK		0.5	—	—	t_{seyc}	1
Transfer Clock Rise Time	t_{SCKr}	SCK		—	—	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	SCK		—	—	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	300	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		500	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface

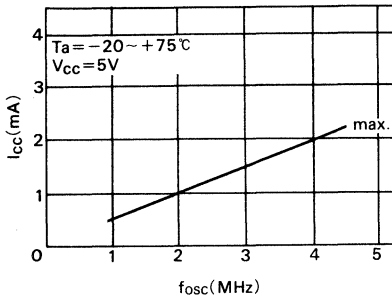


(Note 2) Timing Load Circuit

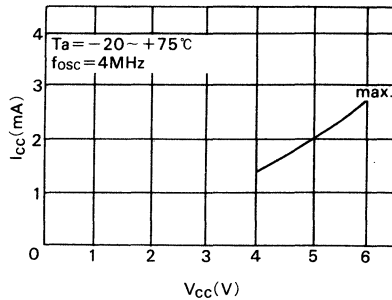


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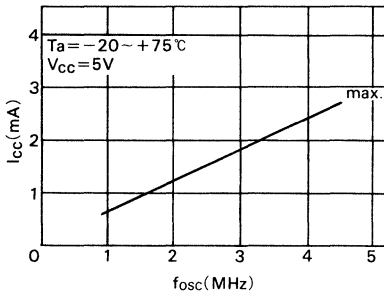
CHARACTERISTICS CURVE (REFERENCE DATA)



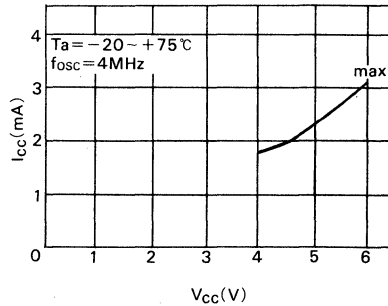
I_{CC} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



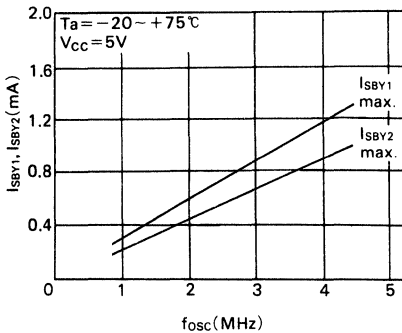
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



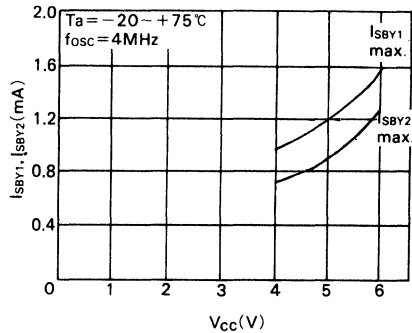
I_{CC} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



I_{CC} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



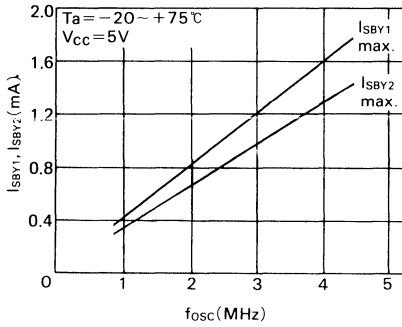
I_{SBV} vs. f_{osc} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



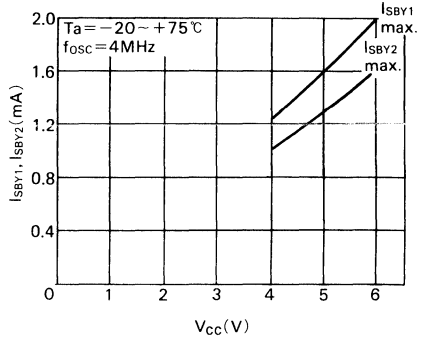
I_{SBV} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator Option)



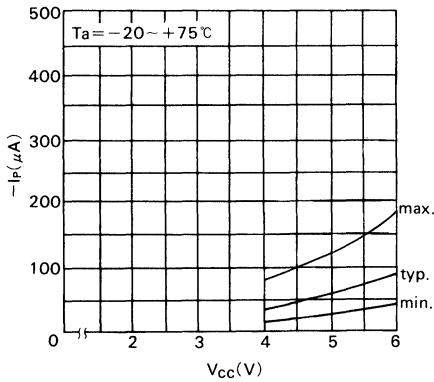
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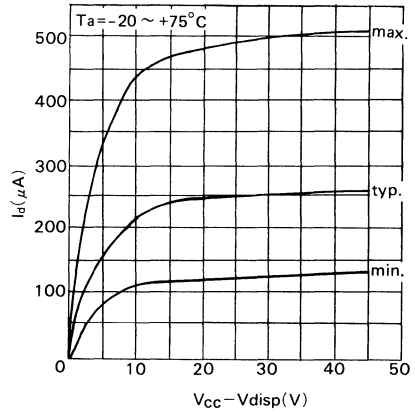
I_{SBY} vs. f_{osc} Characteristics
(Resistor Oscillator Option)



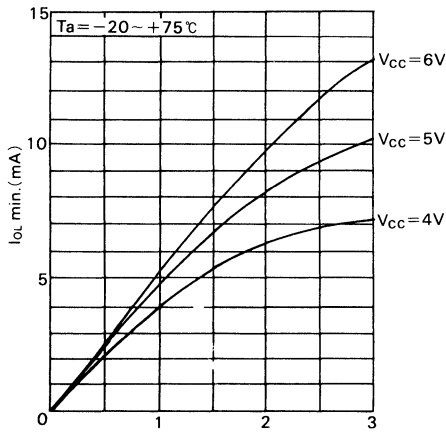
I_{SBY} vs. V_{CC} Characteristics
(Resistor Oscillator Option)



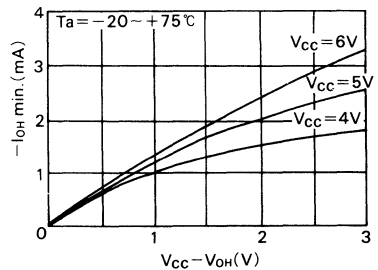
$-I_P$ (Pull-up MOS Current) vs.
 V_{CC} Characteristics



I_d (Pull-down MOS Current) vs.
 $(V_{CC} - V_{disp})$ Characteristics

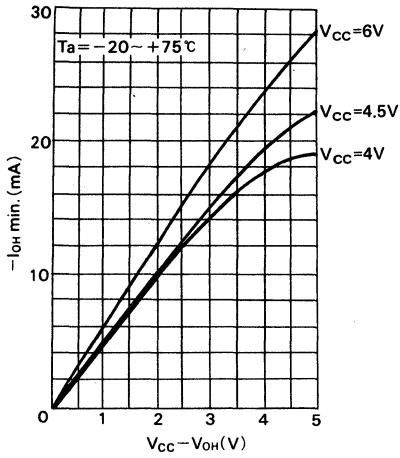


$I_{OL \text{ min.}}$ vs. V_{OL} Characteristics
(Standard Pin)

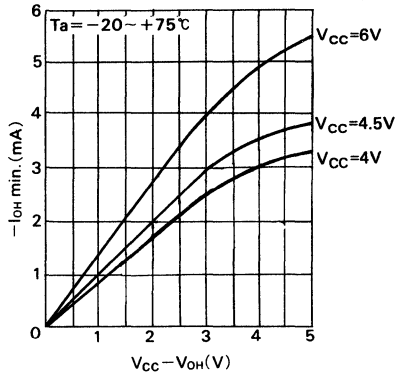


$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")

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$-I_{OH} \text{ min. vs. } (V_{CC} - V_{OH}) \text{ Characteristics}$
($D_4 \sim D_{15}$ Pins)



$-I_{OH} \text{ min. vs. } (V_{CC} - V_{OH}) \text{ Characteristics}$
($RO \sim R_2$ Pins)



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■ **HMCS404CL ELECTRICAL CHARACTERISTICS**

- **DC CHARACTERISTICS** ($V_{CC}=2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC}-40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, \overline{SCK} , INT0, INT1		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
		SI		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
		OSC1		$V_{CC}-0.3$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	RESET, \overline{SCK} , INT0, INT1		-0.3	—	$0.15V_{CC}$	V	
		SI		-0.3	—	$0.15V_{CC}$	V	
		OSC1		-0.3	—	0.3	V	
Output "High" Voltage	V_{OH}	\overline{SCK} , SO	$-I_{OH} = 0.1$ mA	$V_{CC}-0.5$	—	—	V	
Output "Low" Voltage	V_{OL}	\overline{SCK} , SO	$I_{OL} = 0.4$ mA	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , INT0, INT1, SI, SO, OSC1	$V_{in} = 0$ V to V_{CC}	—	—	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.6	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.5	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 3$ V $f_{osc} = 2$ MHz	—	—	0.4	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in} (\overline{TEST}) = V_{CC}-0.2V$ to V_{CC} $V_{in} (RESET) = 0V$ to 0.2 V	—	—	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	—	—	V	

HMCS404C/HMCS404CL/HMCS404AC

(Note 1) Pull-up MOS current and output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; • Reset state in Operation Mode
 Pin state; • RESET, TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2 prescaler divide ratio
 • TIMER-B; ± 2 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2048 prescaler divide ratio
 • TIMER-B; ± 2048 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9$... V_{CC} voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1}$... V_{disp} voltage

(Note 5) Pull-down MOS current is excluded.

(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

[When Divide-by-8 (D-8) option is selected.] $\max. \text{value} (f_{osc}=x[\text{MHz}]) = \frac{x}{2} \times \max. \text{value} (f_{osc}=2[\text{MHz}])$

● INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN

($V_{CC} = 2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3, R3 \sim R5, R9$		$0.85V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3, R3 \sim R5, R9$		-0.3	—	$0.15 V_{CC}$	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3, R3 \sim R8$	$-I_{OH} = 0.1 \text{ mA}$	$V_{CC}-0.5$	—	—	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3, R3 \sim R8$	$I_{OL} = 0.4 \text{ mA}$	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	$D_0 \sim D_3, R3 \sim R9$	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3, R3 \sim R9$	$V_{CC} = 3V$ $V_{in} = 0V$	3	15	40	μA	3
		$D_0 \sim D_3, R3 \sim R9$	$V_{CC} = 5V$ $V_{in} = 0V$	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" output selected by mask option.

(Note 2) Pull-up MOS current and output buffer current are excluded.

(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.



HMCS404C/HMCS404CL/HMCS404AC

- **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
($V_{CC} = 2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.85V_{CC}$	–	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC}-40$	–	$0.15V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH}=15mA, V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	–	–	V	
			$-I_{OH}=2.5mA$	$V_{CC}-1.0$	–	–	V	
		R0 ~ R2	$-I_{OH}=3mA, V_{CC}=5V\pm 10\%$	$V_{CC}-3.0$	–	–	V	
			$-I_{OH}=0.5mA$	$V_{CC}-1.0$	–	–	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	–	–	$V_{CC}-37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC}-40V$	–	–	$V_{CC}-37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	–	–	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.

(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.

(Note 3) Pull-down MOS current and output buffer current are excluded.

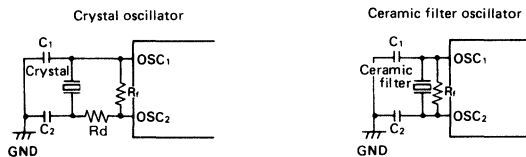
(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

HMCS404C/HMCS404CL/HMCS404AC

● AC CHARACTERISTICS ($V_{CC}=2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC1, OSC2		0.4	2	2.25	MHz	
Instruction Cycle Time	t_{cyc}			3.55	4	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC1, OSC2		—	—	60	ms	1
External Clock "High" Level Width	t_{CPH}	OSC1		205	—	—	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC1		205	—	—	ns	2
External Clock Rise Time	t_{CPr}	OSC1		—	—	20	ns	2
External Clock Fall Time	t_{CpF}	OSC1		—	—	20	ns	2
\overline{INT}_0 "High" Level Width	t_{i0H}	\overline{INT}_0		2	—	—	t_{cyc}	3
\overline{INT}_0 "Low" Level Width	t_{i0L}	\overline{INT}_0		2	—	—	t_{cyc}	3
\overline{INT}_1 "High" Level Width	t_{i1H}	\overline{INT}_1		2	—	—	t_{cyc}	3
\overline{INT}_1 "Low" Level Width	t_{i1L}	\overline{INT}_1		2	—	—	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4
Input Capacitance	C_{in}	all pins	$f = 1\text{ MHz}$ $V_{in} = 0\text{ V}$	—	—	15	μF	
RESET Fall Time	t_{RSTf}			—	—	15	ms	4

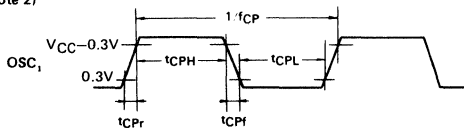
(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.



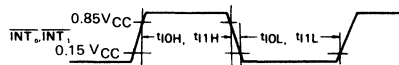
Crystal: 2.097152MHz DS-MGQ308 (Seiko Denshi)
 $R_f = 2M\Omega \pm 2\%$, $R_d = 2.2k\Omega \pm 2\%$
 $C_1 = 10pF \pm 20\%$
 $C_2 = 10pF \pm 20\%$

Ceramic filter: CSA2.000MK (Murata)
 $R_f = 1M\Omega \pm 2\%$, $C_1 = C_2 = 30pF \pm 20\%$

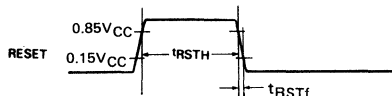
(Note 2)



(Note 3)



(Note 4)



HMCS404C/HMCS404CL/HMCS404AC

● **SERIAL INTERFACE TIMING CHARACTERISTICS**

($V_{CC}=2.7V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

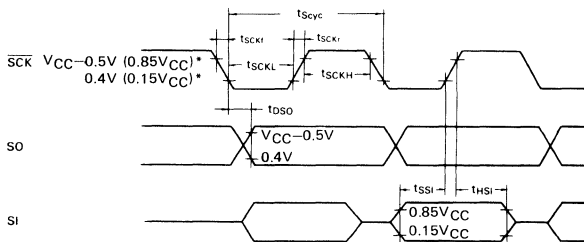
• At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	SCK	(Note 2)	1	—	—	t_{CYC}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	SCK	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	SCK	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock Rise Time	t_{SCKr}	SCK	(Note 2)	—	—	300	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	SCK	(Note 2)	—	—	300	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	—	—	ns	1

• At Transfer Clock Input

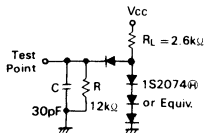
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	SCK		1	—	—	t_{CYC}	1
Transfer Clock "High" Level Width	t_{SCKH}	SCK		0.5	—	—	t_{SCYC}	1
Transfer Clock "Low" Level Width	t_{SCKL}	SCK		0.5	—	—	t_{SCYC}	1
Transfer Clock Rise Time	t_{SCKr}	SCK		—	—	300	ns	1
Transfer Clock Fall Time	t_{SCKf}	SCK		—	—	300	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	600	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		1000	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		500	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface

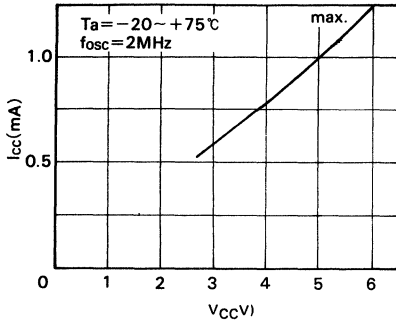


* $V_{CC}-0.5V$ and $0.4V$ are the threshold voltage for transfer clock output. $0.85V_{CC}$ and $0.15V_{CC}$ are the threshold voltage for transfer clock input.

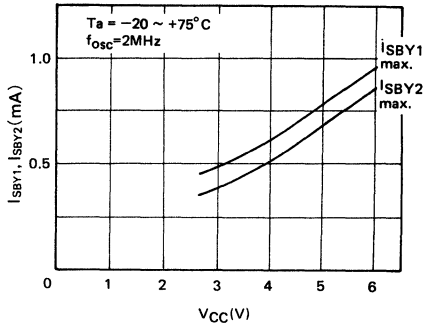
(Note 2) Timing Load Circuit



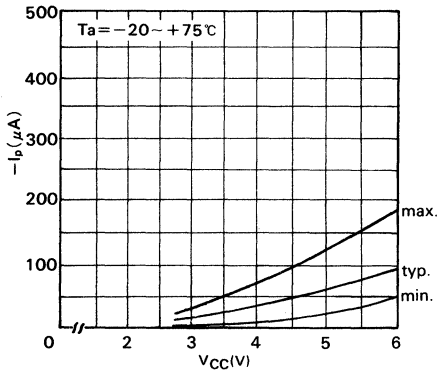
● CHARACTERISTICS CURVE (REFERENCE DATA)



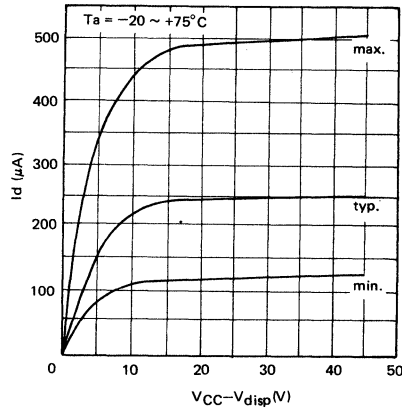
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



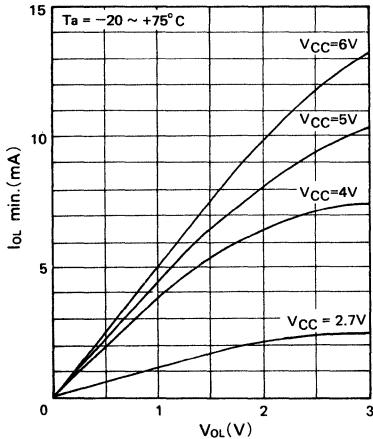
I_{SBY1} , I_{SBY2} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



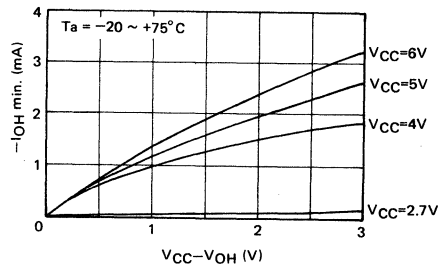
$-I_p$ (Pull-up MOS Current) vs. V_{CC} Characteristics



I_d (Pull-down MOS Current) vs. $(V_{CC} - V_{disp})$ Characteristics

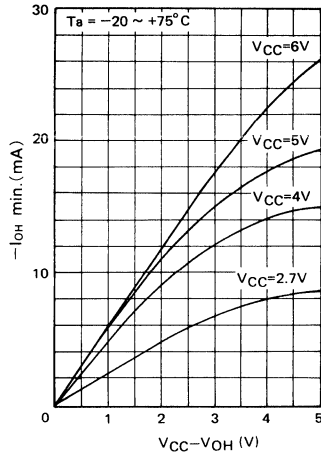


I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)

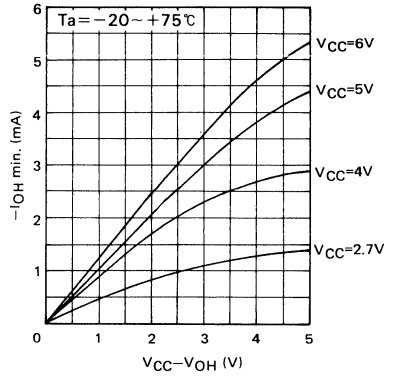


$-I_{OH}$ min. vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")





$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($D_4 \sim D_{1s}$ Pins)



$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ Characteristics
($R_0 \sim R_2$ Pins)

HMCS404C/HMCS404CL/HMCS404AC

■ HMCS404AC ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{CC} = 4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	RESET, SCK, INT ₀ , INT ₁		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
		SI		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
		OSC ₁		$V_{CC}-0.5$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	RESET, SCK, INT ₀ , INT ₁		-0.3	—	$0.22V_{CC}$	V	
		SI		-0.3	—	$0.22V_{CC}$	V	
		OSC ₁		-0.3	—	0.5	V	
Output "High" Voltage	V_{OH}	SCK, SO	$-I_{OH} = 1.0$ mA	$V_{CC}-1.0$	—	—	V	
			$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	—	—	V	
Output "Low" Voltage	V_{OL}	SCK, SO	$I_{OL} = 1.6$ mA	—	—	0.4	V	
Input/Output Leakage Current	I_{IL}	RESET, SCK, INT ₀ , INT ₁ , SI, SO, OSC ₁	$V_{in} = 0$ V to V_{CC}	—	—	1	μA	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}	$V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	3.0	mA	2, 6
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	1.8	mA	3, 6
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 5$ V $f_{osc} = 6$ MHz	—	—	1.35	mA	4, 6
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in} (\overline{TEST}) = V_{CC} - 0.3$ V to V_{CC} $V_{in} (RESET) = 0$ V to 0.3 V	—	—	10	μA	5
Stop Mode Retain Voltage	V_{stop}	V_{CC}		2	—	—	V	



(Note 1) Pull-up MOS current and output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; • Reset state in Operation Mode
 Pin state; • RESET, TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 3) The timer/counter operate with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2 prescaler divide ratio
 • TIMER-B; ± 2 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 4) The timer/counter operate with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; • Standby Mode
 • Input/Output; Reset state
 • TIMER-A; ± 2048 prescaler divide ratio
 • TIMER-B; ± 2048 prescaler divide ratio
 • SERIAL Interface ; Stop
 Pin state; • RESET ... GND voltage
 • TEST ... V_{CC} voltage
 • $D_0 \sim D_3, R3 \sim R9 \dots V_{CC}$ voltage
 • $D_4 \sim D_{15}, R0 \sim R2, R_{A0}, R_{A1} \dots V_{disp}$ voltage

(Note 5) Pull-down MOS current is excluded.

(Note 6) When $f_{osc}=x$ [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value } (f_{osc}=x[\text{MHz}]) = \frac{x}{6} \times \text{max. value } (f_{osc}=6[\text{MHz}])$$

● **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
 ($V_{CC} = 4.5V$ to $6V, GND = 0V, V_{disp} = V_{CC} - 40V$ to $V_{CC}, T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	$D_0 \sim D_3, R3 \sim R5, R9$		$0.7V_{CC}$	—	$V_{CC}+0.3$	V	
Input "Low" Voltage	V_{IL}	$D_0 \sim D_3, R3 \sim R5, R9$		-0.3	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	$D_0 \sim D_3, R3 \sim R8$	$-I_{OH} = 1.0 \text{ mA}$	$V_{CC}-1.0$	—	—	V	1
		$D_0 \sim D_3, R3 \sim R8$	$-I_{OH} = 0.01 \text{ mA}$	$V_{CC}-0.3$	—	—	V	1
Output "Low" Voltage	V_{OL}	$D_0 \sim D_3, R3 \sim R8$	$I_{OL} = 1.6 \text{ mA}$	—	—	0.4	V	
Input/Output Leakage Current	$ I_{IL} $	$D_0 \sim D_3, R3 \sim R9$	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	2
Pull-Up MOS Current	$-I_p$	$D_0 \sim D_3, R3 \sim R9$	$V_{CC} = 5V$ $V_{in} = 0V$	30	60	120	μA	3

(Note 1) Applied to I/O pins with "CMOS" Output selected by mask option.

(Note 2) Pull-up MOS current and output buffer current are excluded.

(Note 3) Applied to I/O pins "with Pull-up MOS" selected by mask option.

HMCS404C/HMCS404CL/HMCS404AC

● INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN

($V_{CC} = 4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V_{IH}	D4 ~ D15, R1 R2, RA0, RA1		$0.7V_{CC}$	—	$V_{CC} + 0.3$	V	
Input "Low" Voltage	V_{IL}	D4 ~ D15, R1 R2, RA0, RA1		$V_{CC} - 40$	—	$0.22V_{CC}$	V	
Output "High" Voltage	V_{OH}	D4 ~ D15	$-I_{OH} = 15mA, V_{CC} = 5V \pm 10\%$	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 9mA$	$V_{CC} - 2.0$	—	—	V	
		R0 ~ R2	$-I_{OH} = 3mA, V_{CC} = 5V \pm 10\%$	$V_{CC} - 3.0$	—	—	V	
			$-I_{OH} = 1.8 mA$	$V_{CC} - 2.0$	—	—	V	
Output "Low" Voltage	V_{OL}	D4 ~ D15 R0 ~ R2	$V_{disp} = V_{CC} - 40V$	—	—	$V_{CC} - 37$	V	1
		D4 ~ D15 R0 ~ R2	$150k\Omega$ to $V_{CC} - 40V$	—	—	$V_{CC} - 37$	V	2
Input/Output Leakage Current	$ I_{IL} $	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{in} = V_{CC} - 40V$ to V_{CC}	—	—	20	μA	3
Pull Down MOS Current	I_d	D4 ~ D15 R0 ~ R2 RA0, RA1	$V_{disp} = V_{CC} - 35V$ $V_{in} = V_{CC}$	125	250	500	μA	4

(Note 1) Applied to I/O pins "with Pull-down MOS" selected by mask option.

(Note 2) Applied to I/O pins "without Pull-down MOS (PMOS Open Drain)" selected by mask option.

(Note 3) Pull-down MOS current and output buffer current are excluded.

(Note 4) Applied to I/O pins "with Pull-down MOS" selected by mask option.

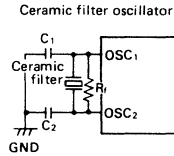
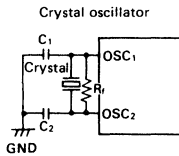


HMCS404C/HMCS404CL/HMCS404AC

● AC CHARACTERISTICS ($V_{CC}=4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC}-40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Oscillation Frequency	f_{osc}	OSC1, OSC2		0.4	6	6.2	MHz	
Instruction Cycle Time	t_{cyc}			1.29	1.33	20	μs	
Oscillator Stabilization Time	t_{RC}	OSC1, OSC2		—	—	20	ms	1
External Clock "High" Level Width	t_{CPH}	OSC1		70	—	—	ns	2
External Clock "Low" Level Width	t_{CPL}	OSC1		70	—	—	ns	2
External Clock Rise Time	t_{CPr}	OSC1		—	—	20	ns	2
External Clock Fall Time	t_{CPf}	OSC1		—	—	20	ns	2
INT ₀ "High" Level Width	t_{I0H}	INT ₀		2	—	—	t_{cyc}	3
INT ₀ "Low" Level Width	t_{I0L}	INT ₀		2	—	—	t_{cyc}	3
INT ₁ "High" Level Width	t_{I1H}	INT ₁		2	—	—	t_{cyc}	3
INT ₁ "Low" Level Width	t_{I1L}	INT ₁		2	—	—	t_{cyc}	3
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4
Input Capacitance	C_{in}	all pins	$f = 1\text{ MHz}$ $V_{in} = 0\text{ V}$	—	—	15	pF	
RESET Fall Time	t_{RSTf}			—	—	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5V at "Power-on", or after RESET input level goes "High" by resetting to quit the stop mode by MCU reset. At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. The circuits used to measure the value are described below. When using crystal or ceramic filter oscillator, please ask a crystal oscillator maker's or ceramic filter maker's advice because oscillator stabilization time depends on the circuit constant and stray capacity.



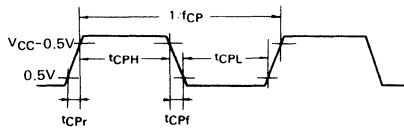
Crystal : 6.0MHz NC-18C (Nihon Denpa Kogyo)

R_f : $1M\Omega \pm 2\%$
 C_1 : $20pF \pm 20\%$
 C_2 : $20pF \pm 20\%$

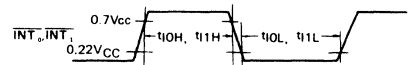
Ceramic filter : CSA6.00MG (Murata)

R_f : $1M\Omega \pm 2\%$
 C_1 : $30pF \pm 20\%$
 C_2 : $30pF \pm 20\%$

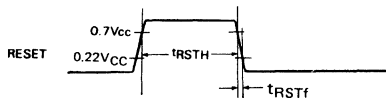
(Note 2)



(Note 3)



(Note 4)



HMCS404C/HMCS404CL/HMCS404AC

SERIAL INTERFACE TIMING CHARACTERISTICS

($V_{CC}=4.5V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC}-40V$ to V_{CC} , $T_a = -20$ to $+75^{\circ}C$, if not specified.)

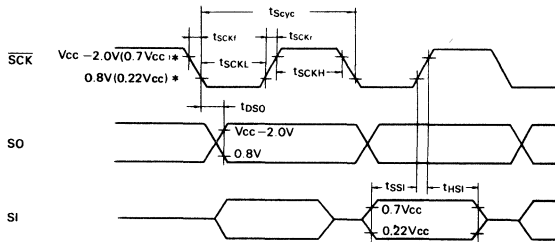
At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	$t_{S_{cyc}}$	SCK	(Note 2)	1	—	—	t_{cyc}	1, 2
Transfer Clock "High" Level Width	$t_{S_{CKH}}$	SCK	(Note 2)	0.5	—	—	$t_{S_{cyc}}$	1, 2
Transfer Clock "Low" Level Width	$t_{S_{CKL}}$	SCK	(Note 2)	0.5	—	—	$t_{S_{cyc}}$	1, 2
Transfer Clock Rise Time	$t_{S_{CKr}}$	SCK	(Note 2)	—	—	100	ns	1, 2
Transfer Clock Fall Time	$t_{S_{CKf}}$	SCK	(Note 2)	—	—	100	ns	1, 2
Serial Output Data Delay Time	$t_{D_{SO}}$	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSi}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSi}	SI		150	—	—	ns	1

At Transfer Clock Input

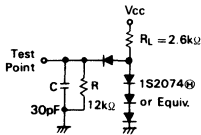
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	$t_{S_{cyc}}$	SCK		1	—	—	t_{cyc}	1
Transfer Clock "High" Level Width	$t_{S_{CKH}}$	SCK		0.5	—	—	$t_{S_{cyc}}$	1
Transfer Clock "Low" Level Width	$t_{S_{CKL}}$	SCK		0.5	—	—	$t_{S_{cyc}}$	1
Transfer Clock Rise Time	$t_{S_{CKr}}$	SCK		—	—	100	ns	1
Transfer Clock Fall Time	$t_{S_{CKf}}$	SCK		—	—	100	ns	1
Serial Output Data Delay Time	$t_{D_{SO}}$	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSi}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSi}	SI		150	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface

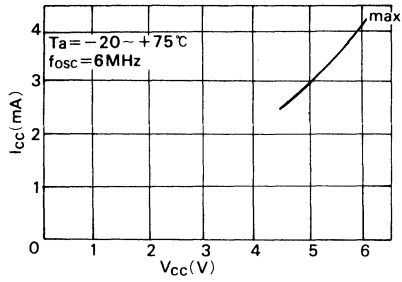


* $V_{CC} - 2.0V$ and $0.8V$ are the threshold voltage for transfer clock output.
 $0.7 V_{CC}$ and $0.22 V_{CC}$ are the threshold voltage for transfer clock input.

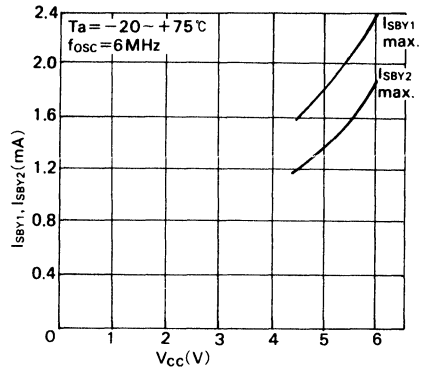
(Note 2) Timing Load Circuit



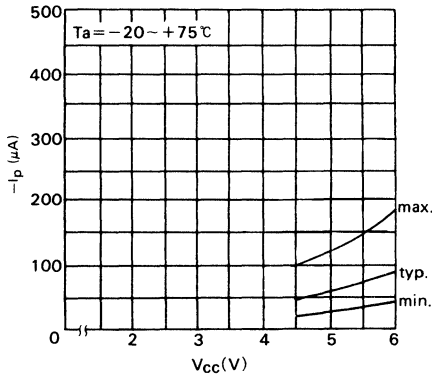
● CHARACTERISTICS CURVE (REFERENCE DATA)



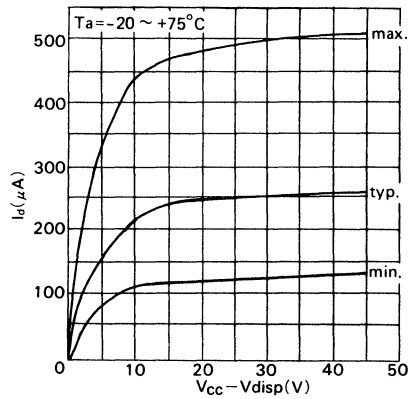
I_{CC} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



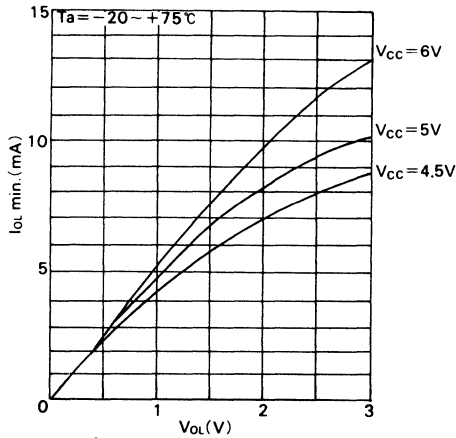
I_{SBV1}, I_{SBV2} vs. V_{CC} Characteristics
(Crystal, Ceramic Filter Oscillator)



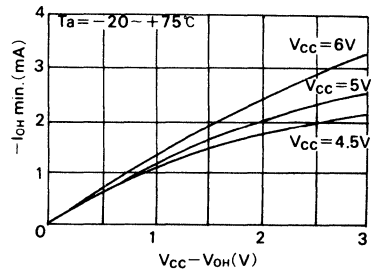
$-I_P$ (Pull-up MOS Current) vs. V_{CC} Characteristics



I_d (Pull-down MOS Current) vs. $(V_{CC} - V_{disp})$ Characteristics

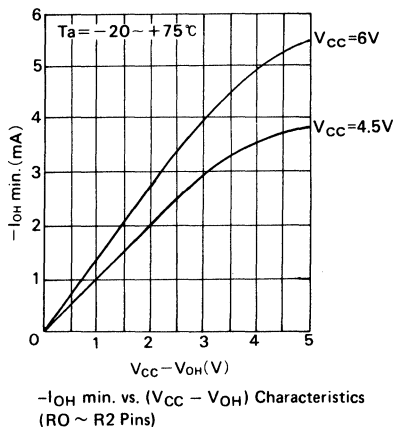
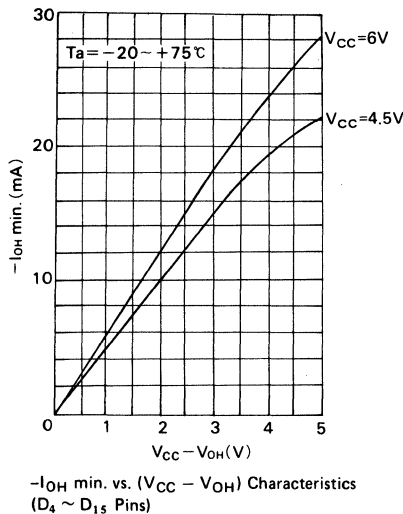


I_{OL} min. vs. V_{OL} Characteristics
(Standard Pin)



$-I_{OL}$ min. vs. $(V_{CC} - V_{OH})$ Characteristics
(Standard Pin "CMOS")





DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

GND, V_{CC} , V_{disp}

These are Power Supply Pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. V_{disp} is a power supply for high voltage Input/Output pins with maximum voltage of $V_{CC} - 40\text{V}$. V_{disp} pin can be also used as RA_1 pin by mask option. For details, see "INPUT/OUTPUT".

TEST

TEST pin is not for user's application. TEST must be connected to V_{CC} .

RESET

RESET pin is used to reset MCU. For details, see "RESET".

OSC₁, OSC₂

These are Input pins to the internal oscillator circuit. They can be connected to crystal resonator, ceramic filter resonator, R_f oscillator (applicable only to the HMCS404C), or external oscillator circuit. Select the circuit of MCU by mask option corresponding to the oscillator type. For details, see "INTERNAL OSCILLATOR CIRCUIT."

D-port (D_0 to D_{15})

D-port is a 1-bit Input/Output common port. D_0 to D_3 are standard type, D_4 to D_{15} are for high voltage. Each pin has the mask option to select its circuit type. For details, See "INPUT/OUTPUT".

R-port (R_0 to RA)

R-port is a 4-bit Input/Output port. (only RA is 2-bit construction.) R_0 and R_6 to R_8 are output ports, R_9 to RA are input ports, and R_1 to R_5 are Input/Output common ports. R_0 to R_2 and RA are the high voltage ports, R_3 to R_9 are the standard ports. Each pin has the mask option to select its circuit type.

R_{32} , R_{33} , R_{40} , R_{41} and R_{42} are also available as \overline{INT}_0 , \overline{INT}_1 , \overline{SCK} , SI and SO respectively. For details, see "INPUT/OUTPUT".

\overline{INT}_0 , \overline{INT}_1

These are the input pins to interrupt MCU operation externally. \overline{INT}_1 can be used as an external event input pin for TIMER-B. \overline{INT}_0 and \overline{INT}_1 are also available as R_{32} , and R_{33} respectively. For details, See "INTERRUPT".

\overline{SCK} , SI , SO

These are Transfer clock I/O pin (\overline{SCK}), serial data input pin (SI) and serial data output pin (SO) used for serial interface. \overline{SCK} , SI , and SO are also available as R_{40} , R_{41} and R_{42} respectively. For details, see "SERIAL INTERFACE".

ROM MEMORY MAP

MCU includes 4096 words \times 10 bits ROM. ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

Vector Address Area \$0000 to \$000F

When MCU is reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

Zero-Page Subroutine Area \$0000 to \$003F

CAL instruction allows to branch to the subroutines in \$0000 to \$003F.

Pattern Area \$0000 to \$0FFF

P instruction allows referring to the ROM data in \$0000 to \$0FFF as a pattern.

Program Area \$0000 to \$0FFF

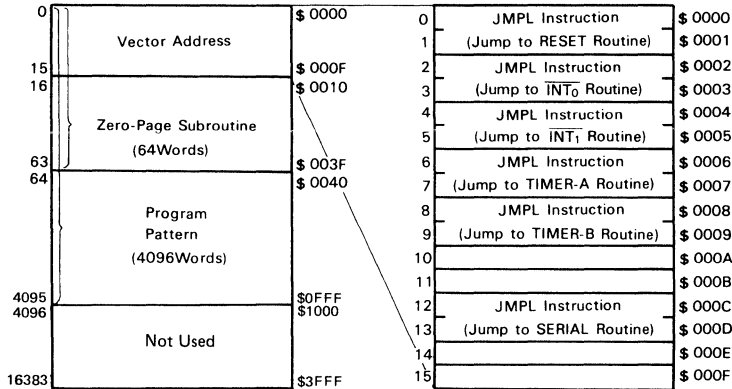
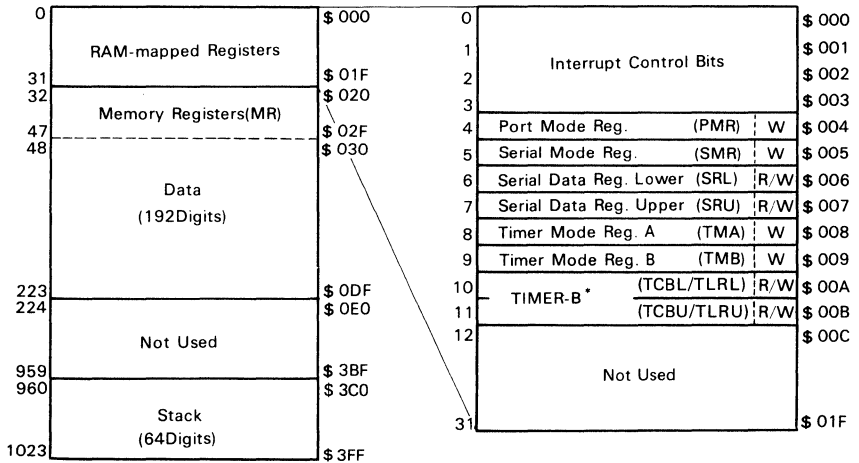


Fig. 1 ROM Memory Map

RAM MEMORY MAP

MCU includes 256 digits × 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits

and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



* Two registers are mapped on same address.

R :Read Only
W :Write Only
R/W:Read/Write

10	Timer, Event Counter B Lower (TCBL)	R	Timer Load Reg. Lower (TLRL)	W	\$ 00A
11	Timer, Event Counter B Upper (TCBU)	R	Timer Load Reg. Upper (TLRU)	W	\$ 00B

Fig. 2 RAM Memory Map

HMCS404C/HMCS404CL/HMCS404AC

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of INT ₀)	IFO (IF of INT ₀)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	IMTA (IM of TIMER-A)	IFTA (IF of TIMER-A)	IM1 (IM of INT ₁)	IF1 (IF of INT ₁)	\$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	\$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	\$003

IF : Interrupt Request Flag
 IM : Interrupt Mask
 I/E : Interrupt Enable Flag
 SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invarid when "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

● **Interrupt Control Bit Area \$000 to \$003**

This area is used for interrupt controls, and is illustrated in Fig.3. It is accessible only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software.

● **Special Register Area \$004 to \$00B**

Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

● **Data Area \$020 to \$0DF**

16 digits of \$020 to \$02F are called memory register (MR) and accessible by LAMR and XMRA instructions.

● **Stack Area \$3C0 to \$3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction. The area, not used for stacking, is available as a data area.

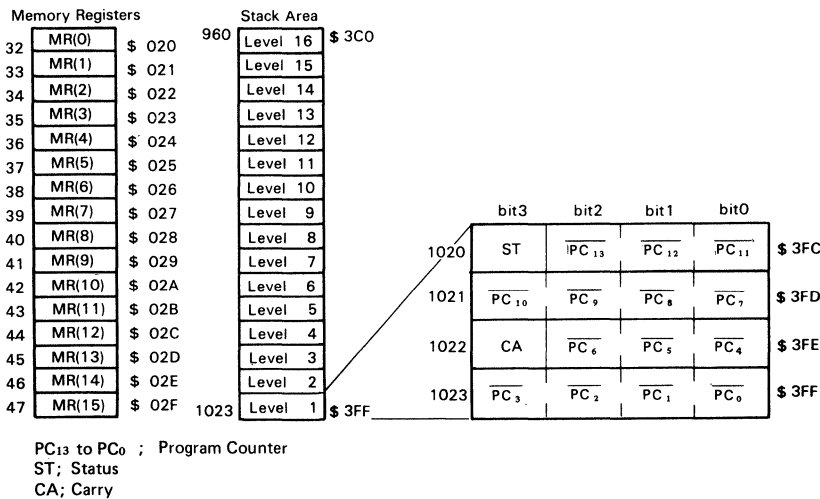


Fig. 4 Configuration of Memory Register, Stack Area and Stack Position



■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

● Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

● W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y register is also used for D-port addressing.

● SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

● Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

● Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the

stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

● Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

● Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate \$3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by five different sources: the external signals (INT₀, INT₁), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

● Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on \$000 to \$003 of the RAM address and accessible by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

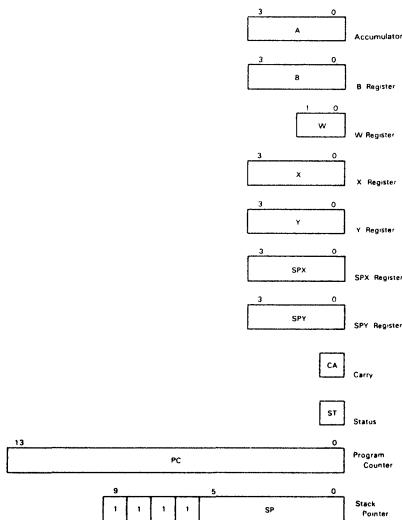


Fig. 5 Register and Flags

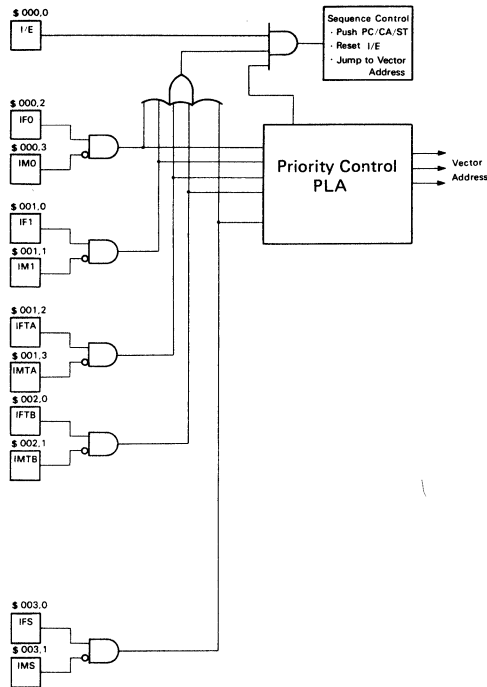


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset / Interrupt	Priority	Vector addresses
RESET	-	\$0000
INT ₀	1	\$0002
INT ₁	2	\$0004
TIMER-A	3	\$0006
TIMER-B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt source Interrupt control bits	INT ₀	INT ₁	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IFO · IMO	1	0	0	0	0
IF1 · IM1	*	1	0	0	0
IFTA · IMTA	*	*	1	0	0
IFTB · IMTB	*	*	*	1	0
IFS · IMS	*	*	*	*	1

* Don't care

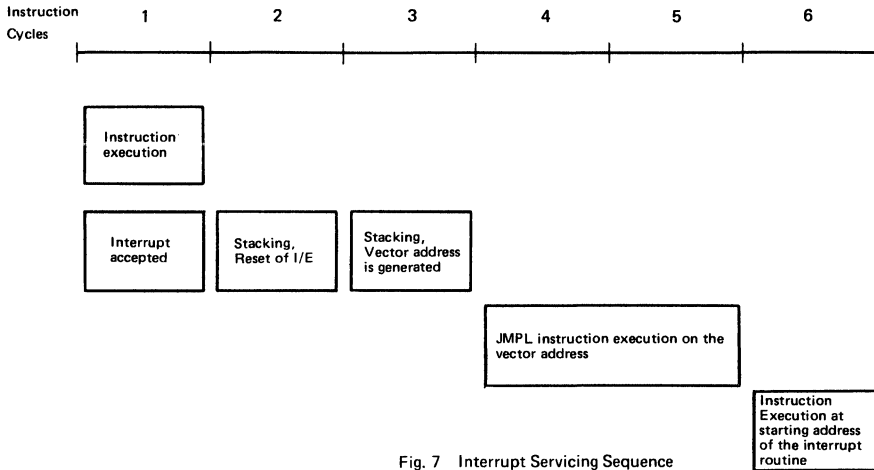


Fig. 7 Interrupt Servicing Sequence

- Interrupt Enable Flag (I/E: \$000,0)**
 The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

- External Interrupt ($\overline{INT_0}$, $\overline{INT_1}$)**
 To use external interrupt, select $R_{32}/\overline{INT_0}$, $R_{33}/\overline{INT_1}$ port for $\overline{INT_0}$, $\overline{INT_1}$ mode by setting the Port Mode Register (PMR: \$004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$, $\overline{INT_1}$ inputs.

$\overline{INT_1}$ input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using $\overline{INT_1}$ as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by $\overline{INT_1}$ will not be accepted.

- External Interrupt Request Flag (IF0: \$000,2, IF1: \$001,0)**
 The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of $\overline{INT_0}$, $\overline{INT_1}$ inputs respectively.

- External Interrupt Mask (IMO: \$000,3, IM1: \$001,1)**
 The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

- Port Mode Register (PMR: \$004)**
 The Port Mode Register is a 4-bit write-only register which controls the $R_{32}/\overline{INT_0}$ pin, $R_{33}/\overline{INT_1}$ pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to \$0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	$R_{33}/\overline{INT_1}$ pin
0	Used as R_{33} port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR bit 2	$R_{32}/\overline{INT_0}$ pin
0	Used as R_{32} port input/output pin
1	Used as $\overline{INT_0}$ input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

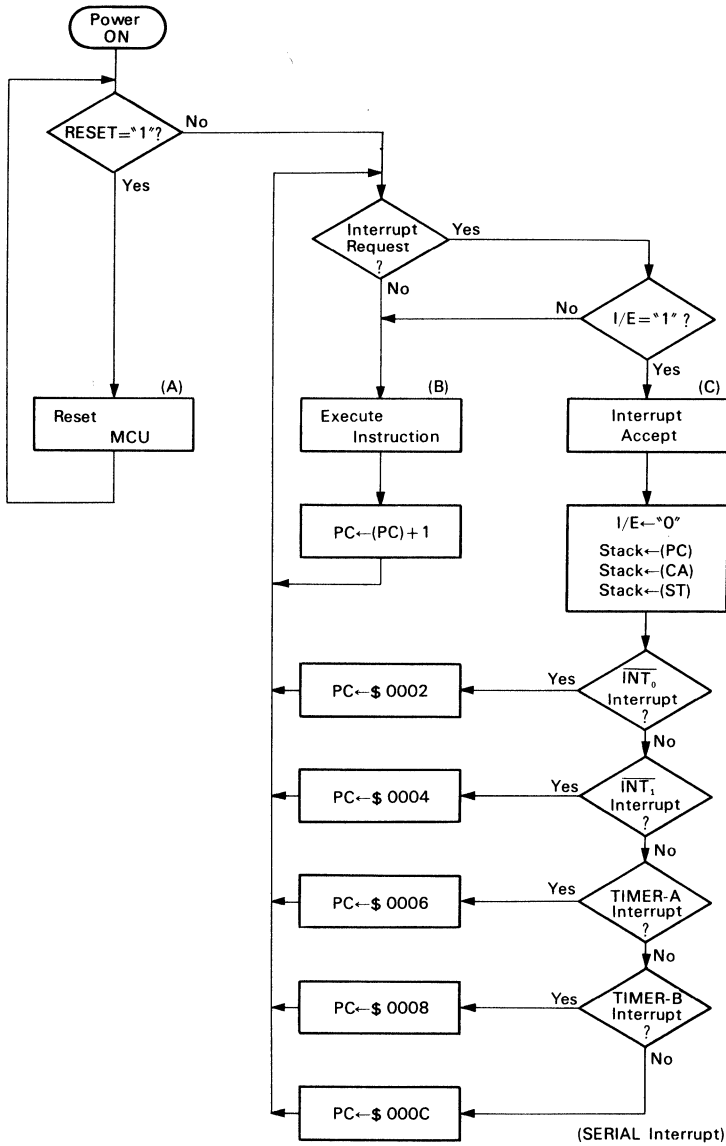


Fig. 8 Interrupt Servicing Flowchart



■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin R_{40}/\overline{SCK} and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronous-

ly with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to \$0 by STS instruction. It starts to count at the falling edge of the transfer clock (\overline{SCK}) signal and increments by one at the rising edge of the \overline{SCK} . When the Octal Counter is reset to \$0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

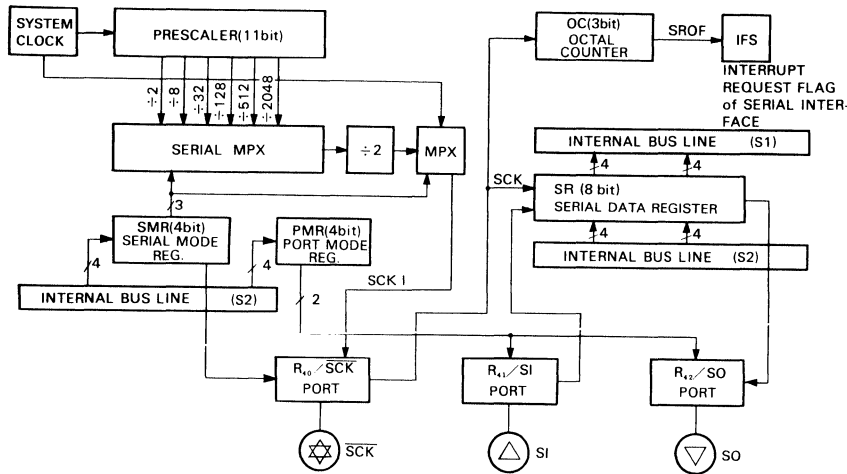


Fig. 9 Serial Interface Block Diagram

● Serial Mode Register (SMR: \$005)

The Serial Mode Register is a 4-bit write-only register. This register controls the R_{40}/\overline{SCK} and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to \$0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to \$0 by MCU reset.

● Serial Data Register (SRL: \$006, SRU: \$007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL:\$006) and a high-order digit (SRU: \$007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	R ₄₀ /SCK
0	Used as R ₄₀ port input/output pin
1	Used as SCK input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	R ₄₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	SCK Output	Prescaler	÷ 2048	÷ 4096
0	0	1	SCK Output	Prescaler	÷ 512	÷ 1024
0	1	0	SCK Output	Prescaler	÷ 128	÷ 256
0	1	1	SCK Output	Prescaler	÷ 32	÷ 64
1	0	0	SCK Output	Prescaler	÷ 8	÷ 16
1	0	1	SCK Output	Prescaler	÷ 2	÷ 4
1	1	0	SCK Output	System Clock	—	÷ 1
1	1	1	SCK Input	External Clock	—	—

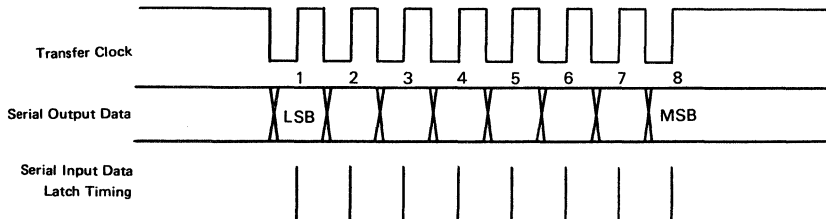


Fig. 10 Serial Interface I/O Timing Chart

- SERIAL Interrupt Request Flag (IFS: \$003, 0)**
 The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.
- SERIAL Interrupt Mask (IMS: \$003, 1)**
 The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

- Selection of the Operation Mode**
 Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10. Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.
- Operating State of Serial Interface**
 The serial interface has 3 operating states as shown in Fig. 11. The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

● **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer

clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "SCK waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR Bit 3	PMR		Serial Interface Operating Mode
	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

* "Change PMR" means the change of operation mode as below:

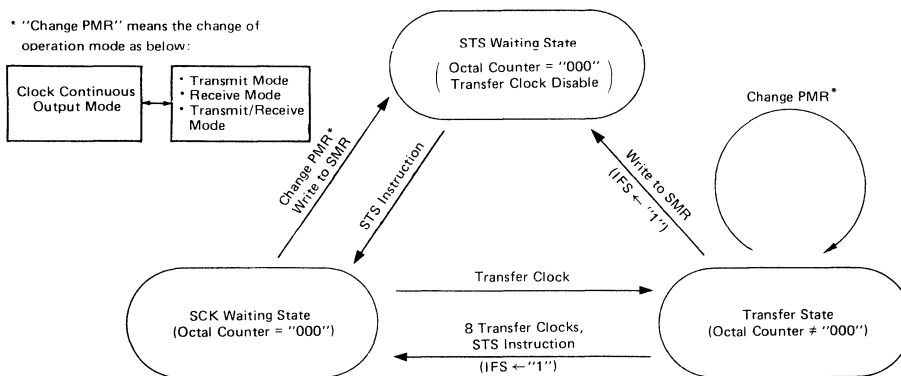


Fig. 11 Serial Interface Operation State

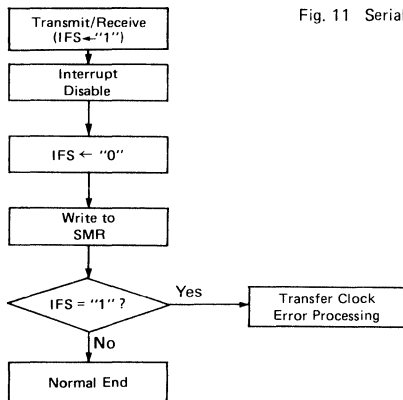


Fig. 12 Example of Transfer Clock Error Detection

■ **TIMER**

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B), Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-running timer. TIMER-B is an 8-bit auto-reload timer/event counter.

● **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler divide ratio of the clock signals are selected according to the content of the mode registers such as - Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

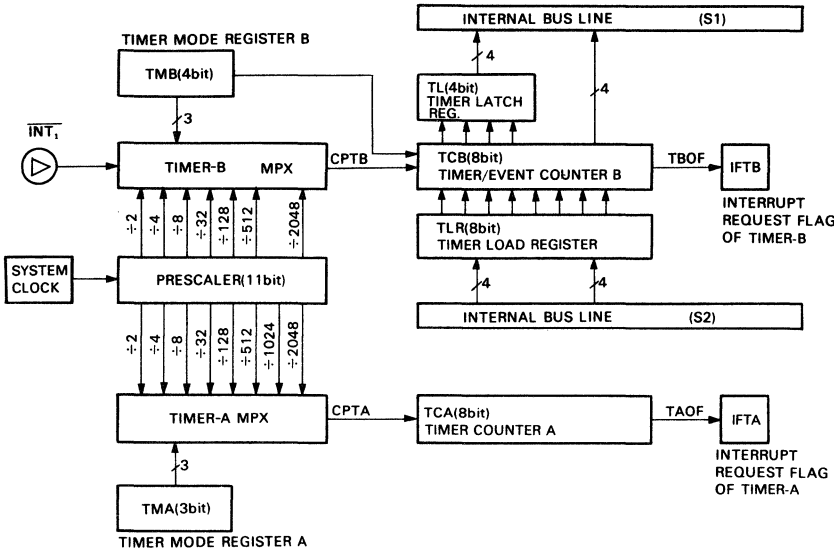


Fig. 13 Timer/Counter Block Diagram

• **TIMER-A Operation**

After TIMER-A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after TIMER-A is counted up to \$FF, TIMER-A is set to \$00 again, and generating overflow output. This leads to setting TIMER-A Interrupt Request Flag (IFTA: \$001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to TIMER-A are selected by the Timer Mode Register A (TMA: \$008).

• **TIMER-B Operation**

Timer Mode Register B (TMB: \$009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the R_{33}/INT_1 as INT_1 and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to \$FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected, TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to \$00. TIMER-B Interrupt Request Flag (IFTB: \$002,0) will be set at this overflow output.

• **Timer Mode Register A (TMA: \$008)**

The Timer Mode Register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of TIMER-A clock input, as shown in Table 11.

The Timer Mode Register A is initialized to \$0 by MCU reset.

• **Timer Mode Register B (TMB: \$009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The Timer Mode Register B is initialized to \$0 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 11. Timer Mode Register A

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB		Auto-reload Function
Bit 3		
0		No
1		Yes

TMB			Prescaler Divide Ratio, Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

• **TIMER-B (TCBL: \$00A, TCBU: \$00B)
(TLRL: \$00A, TLRU: \$00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to \$00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading

the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

• **TIMER-A Interrupt Request Flag (IFTA: \$001, 2)**
The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

• **TIMER-A Interrupt Mask (IMTA: \$001, 3)**
TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

• **TIMER-B Interrupt Request Flag (IFTB: \$002, 0)**
The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

• **TIMER-B Interrupt Mask (IMTB: \$002, 1)**
TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

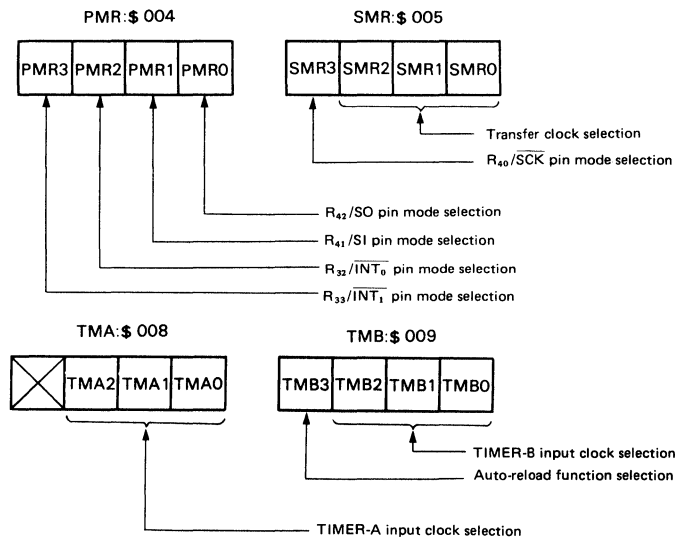


Fig. 14 Mode Register Configuration and Function

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

INPUT/OUTPUT

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins and 26 high voltage pins. Each standard pin may have one of three mask options: (A) "Without pull-up MOS (NMOS open drain)", (B) "With pull-up MOS", or (C) "CMOS". And also each high voltage pin may have one of two mask options: (D) "Without pull-down MOS (PMOS

open drain)", or (E) "With pull-down MOS". As pull-down MOS is connected to internal V_{disp} line, select R_{A1}/V_{disp} pin as V_{disp} with mask option when at least one high voltage pin is selected as "With pull-down MOS" option.

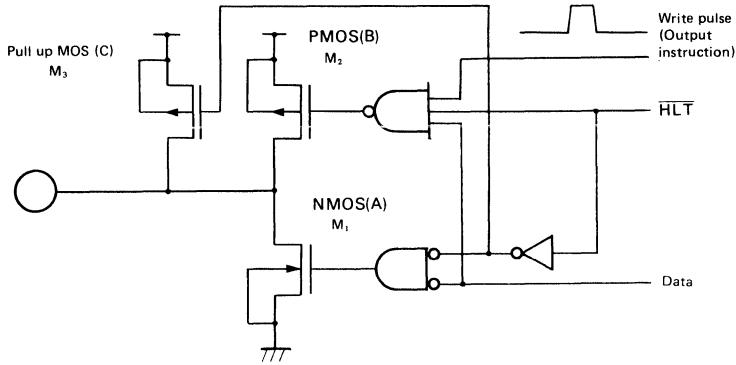
When any Input/Output common pin is used as input pin, it is necessary to select the mask option and output data as shown in Table 18.

Output Circuit Operation of Standard Pins with "With pull-up MOS" Option

Fig. 15 shows the circuit used in the standard pins with "with pull-up MOS" option.

By execution of the output instruction, the write pulse will be generated, and be applied to the addressed port. This pulse will turn "ON" the PMOS (B) to make the transient time shorten to obtain "High level", if the output data is changed from "0" to "1". In this case, the "write pulse" allows the PMOS (B) to turn "ON" as long as 1/8 instruction cycle. While "write pulse" is "0", pull-up MOS (C) may retain the output in high level.

The HLT signal becomes "0" in stop mode, so that MOS (A) (B) (C) turn "OFF".



MOS Buffer	Features	ON Resistance Value	
		HMCS404C, HMCS404AC	HMCS404CL
M ₁		approx. 250Ω	approx. 1kΩ
i _v ₂		approx. 1kΩ	approx. 5kΩ
M ₃		approx. 40kΩ to 160kΩ (V _{CC} = 5V)	approx. 75kΩ to 1MΩ (V _{CC} = 3V), approx. 40kΩ to 160kΩ (V _{CC} = 5V)

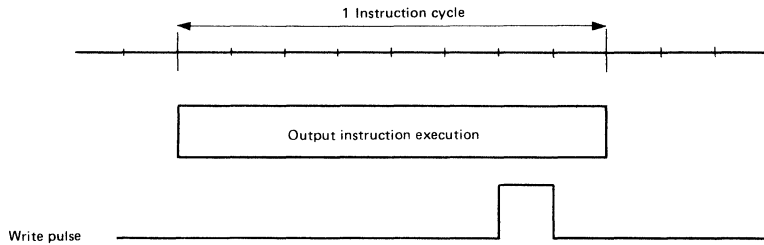


Fig. 15 Output Circuit Operation of Standard Pins with "with Pull-up MOS" Option

HMCS404C/HMCS404CL/HMCS404AC

Table 17 I/O Pin Circuit Type

	Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applied pins
Standard pins	I/O common pins 			D ₀ ~ D ₃ , R ₃₀ ~ R ₃₃ , R ₄₀ ~ R ₄₃ , R ₅₀ ~ R ₅₃
	Output pins 			R ₆₀ ~ R ₆₃ , R ₇₀ ~ R ₇₃ , R ₈₀ ~ R ₈₃
	Input pins 			R ₉₀ ~ R ₉₃
High voltage pins	I/O common pins 			D ₄ ~ D ₁₅ , R ₁₀ ~ R ₁₃ , R ₂₀ ~ R ₂₃
	Output pins 			R ₀₀ ~ R ₀₃
	Input pins 			R _{A0} , R _{A1} /V _{disp}

(Note) In the stop mode, HLT signal is "0" and I/O pins are in high impedance state.

(to be continued)



HMCS404C/HMCS404CL/HMCS404AC

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applied pins
Standard pins	I/O common pins			SCK (Note 2) (Output Mode)
	Output pins			SO
	Input pins			$\overline{INT_0}$, $\overline{INT_1}$, SI, SCK (Note 2) (Input Mode)

(Note 1) In the stop mode, \overline{HLT} signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

(Note 2) If the MCU is interrupted by serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 18 Data Input from Input/Output Common Pins

I/O pin circuit type		Possibility of Input	Available pin condition for input
Standard pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	"1"
	With pull-up MOS	Yes	"1"
High voltage pins	Without pull-down MOS (PMOS open drain)	Yes	"0"
	With pull-down MOS	Yes	"0"

HMCS404C/HMCS404CL/HMCS404AC

● D-port

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

● R-port

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the

output-only and/or non-existing ports.

The R₃₂, R₃₃, R₄₀, R₄₁ and R₄₂ pins are also used as the $\overline{INT0}$, INT1, \overline{SCK} , SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

■ RESET

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

Table 19 Initial Value by MCU Reset

Items		Initial value by MCU reset	Contents	
Program counter (PC)		\$0000	Execute program from the top of ROM address.	
Status (ST)		"1"	Enable to branch with conditional branch instructions.	
Stack pointer (SP)		\$3FF	Stack level is 0.	
I/O pin output register	Standard pin	(A) Without pull-up MOS	"1"	Enable to input.
		(B) With pull-up MOS	"1"	Enable to input
		(C) CMOS	"1"	—
	High voltage pin	(D) Without pull-down MOS	"0"	Enable to input.
		(E) With pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)	"0"	Inhibit all interrupts.	
	Interrupt Request Flag (I/F)	"0"	No interrupt request.	
	Interrupt Mask (IM)	"1"	Mask interrupt request.	
Mode register	Port Mode Register (PMR)	"0000"	See Item "Port Mode Register".	
	Serial Mode Register (SMR)	"0000"	See Item "Serial Mode Register".	
	Timer Mode Register A (TMA)	"000"	See Item "Timer Mode Register A".	
	Timer Mode Register B (TMB)	"0000"	See Item "Timer Mode Register B".	
Timer/Counter, Serial interface	Prescaler	\$000	—	
	Timer/Counter A (TCA)	\$00	—	
	Timer/Event Counter B (TCB)	\$00	—	
	Timer Load Register (TLR)	\$00	—	
	Octal Counter	"000"	—	

(Note) MCU reset affects to the rest of registers as follows:

Item	After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry (CA)		
Accumulator (A)		
B Register (B)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
W Register (W)		
X/SPX Registers (X/SPX)		
Y/SPY Registers (Y/SPY)		
Serial Data Register (SR)	Same as above	Same as above
RAM	The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

■ **INTERNAL OSCILLATOR CIRCUIT**

Fig. 16 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal oscillator, ceramic

filter oscillator, or resistor oscillator as shown in Table 20. In any cases, external clock operation is available.

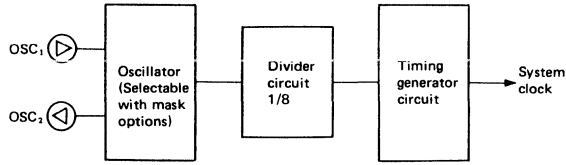


Fig. 16 Internal Oscillator Circuit

Internal Oscillator Circuit Mask Option

		HMCS404C	HMCS404CL	HMCS404AC
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○
	Resistor	○	—	—
Divider	1/8	○	○	○

HMCS404C/HMCS404CL/HMCS404AC

• Oscillator Circuit

Table 20 Examples of Oscillator Circuit

	Circuit configuration	Circuit constants		
		HMCS404C	HMCS404CL	HMCS404AC
External clock operation				
Resistor oscillator		$R_f = 20k\Omega \pm 2\%$		
Ceramic filter oscillator		Ceramic filter CSA4.00MG (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$	Ceramic filter CSA2.000MK (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$	Ceramic filter CSA6.00MG (Murata) $R_f : 1M\Omega \pm 2\%$ $C_1 : 30pF \pm 20\%$ $C_2 : 30pF \pm 20\%$
Crystal oscillator	<p>AT cut parallel resonance crystal</p>	$R_f : 1M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 60\Omega \text{ max.}$ $f : 2.0 \sim 4.5MHz$		$R_f : 1M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 100\Omega \text{ max.}$ $f : 2.0 \sim 6.2MHz$
	<p>GT cut parallel resonance crystal</p>		$R_f : 2M\Omega \pm 2\%$ $C_1 : 10 \sim 22pF \pm 20\%$ $C_2 : 10 \sim 22pF \pm 20\%$ Crystal: equivalent circuit to the left $C_0 : 7pF \text{ max.}$ $R_s : 100\Omega \text{ max.}$ $f : 2.0 \sim 2.25MHz$	

- (Note 1) On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
- (Note 2) Wiring among OSC₁, OSC₂ and elements should be as short as possible, and never cross the other wirings. Refer to the recommendable layout of crystal and ceramic filter.

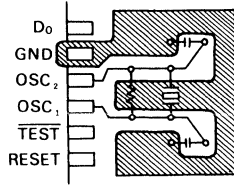


Fig. 17 Recommendable Layout of Crystal and Ceramic Filter

■ **LOW POWER DISSIPATION MODE**

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 18 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/Output pin	Timer/Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ^{*3)}	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ^{*1)}	Stop	Retained	High ^{*2)} impedance	Stop	RESET Input

- *1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 19.
- *2) A high voltage pin with a pull-down MOS option is pulled down to the V_{disp} power supply by the pull-down MOS. As the MOS is ON, a pull-down MOS current flows when a voltage difference between the pin and the V_{disp} voltage exists. This is the additional current to the current dissipation in Stop Mode (I_{stop}).
- *3) As a I/O circuit is active, a I/O current possibly flows according to the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (I_{SBY1} , I_{SBY2}).

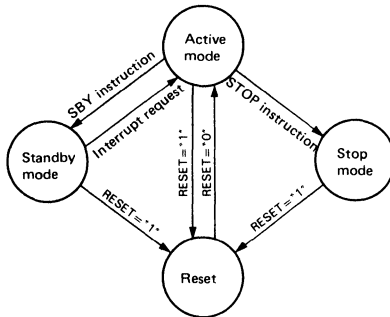


Fig. 18 MCU Operation Mode Transition

- **Standby Mode**
The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/

counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 19 shows the flowchart of the Standby Mode.

● **Stop Mode**

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 20, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode. The other hand, Accumulator, B Register, W Register, X/SPX Registers, Y/SPY Registers, Carry and Serial Data Register don't retain the contents.

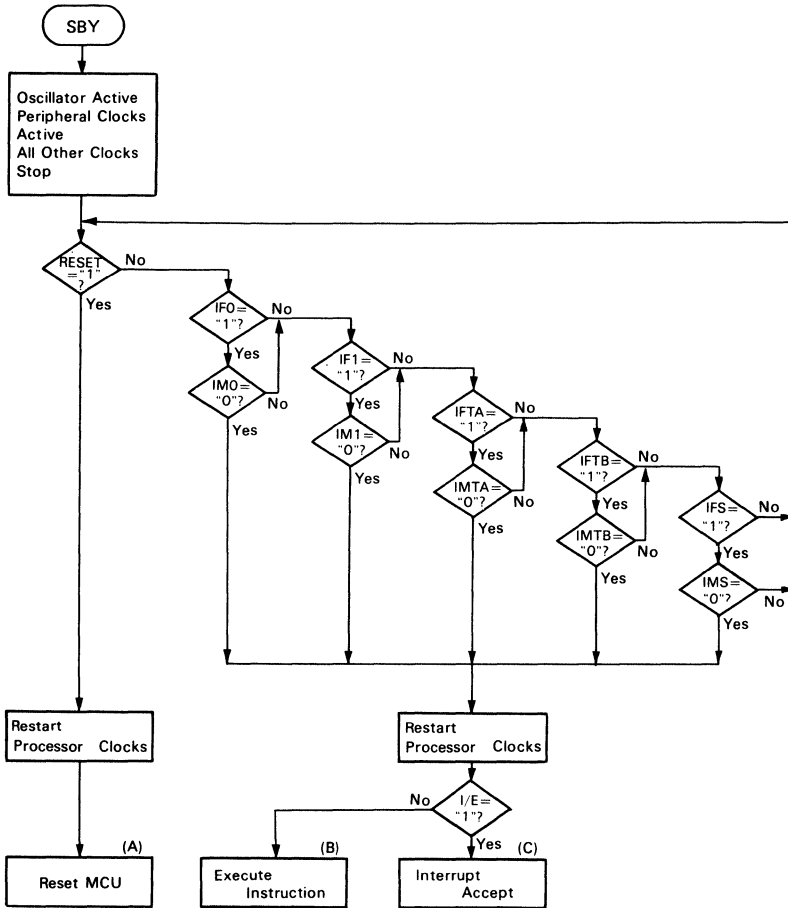


Fig. 19 MCU Operating Flowchart

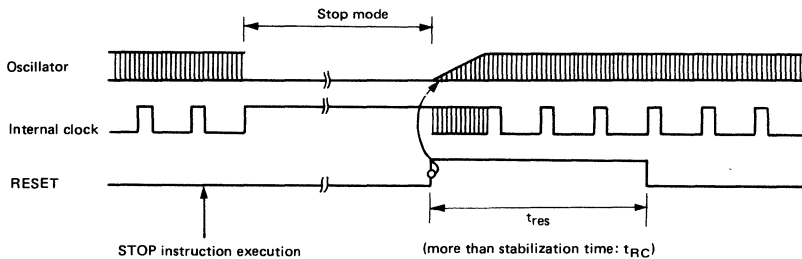


Fig. 20 Timing Chart of Recovering from Stop Mode

■ **RAM ADDRESSING MODE**

As shown in Fig. 21, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

● **Register Indirect Addressing**

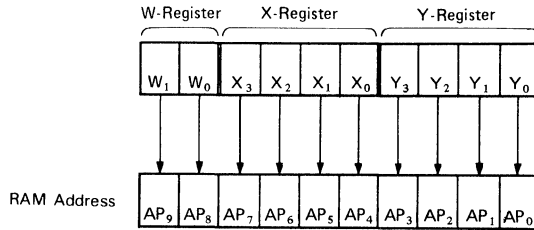
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

● **Direct Addressing**

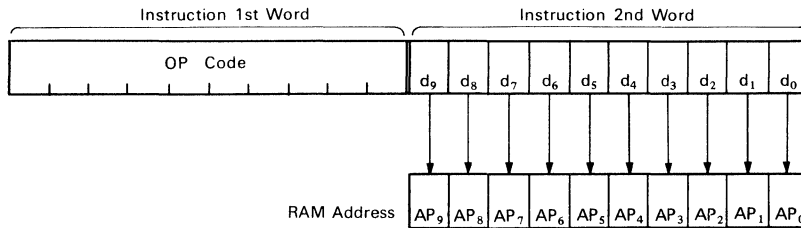
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

● **Memory Register Addressing**

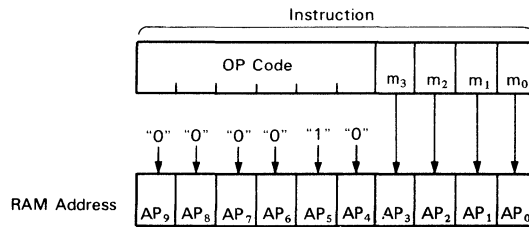
The Memory Register Addressing can access 16 digits (Memory Register: MR) from \$020 to \$02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 21 RAM Addressing Mode

HMCS404C/HMCS404CL/HMCS404AC

ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 22.

Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instruction replace 14-bit program counter (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode

ROM memory space is divided into 256 words in each page starting from \$0000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC₇ to PC₀) with

8-bit immediate data. The branch destination by BR instruction on the boundary between pages is given in Fig. 24.

Zero Page Addressing Mode

The program branches to the zero page subroutine area, which is located on the address from \$0000 to \$003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC₅ to PC₀) and "0's" are placed in high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing

The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.

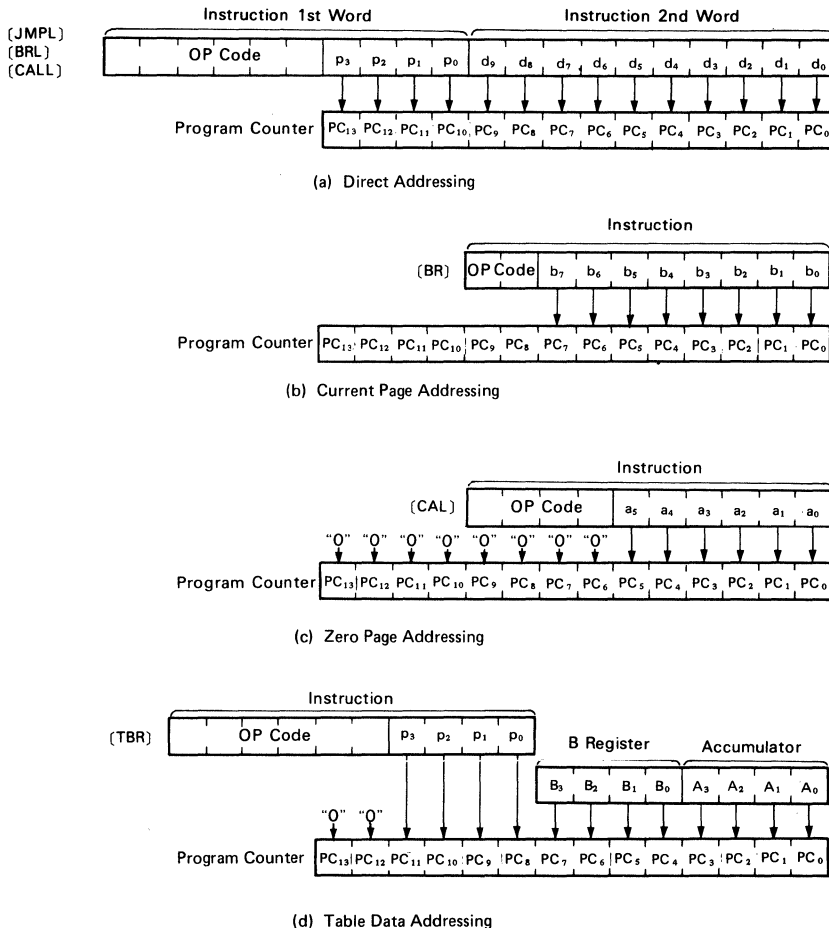


Fig. 22 ROM Addressing Mode



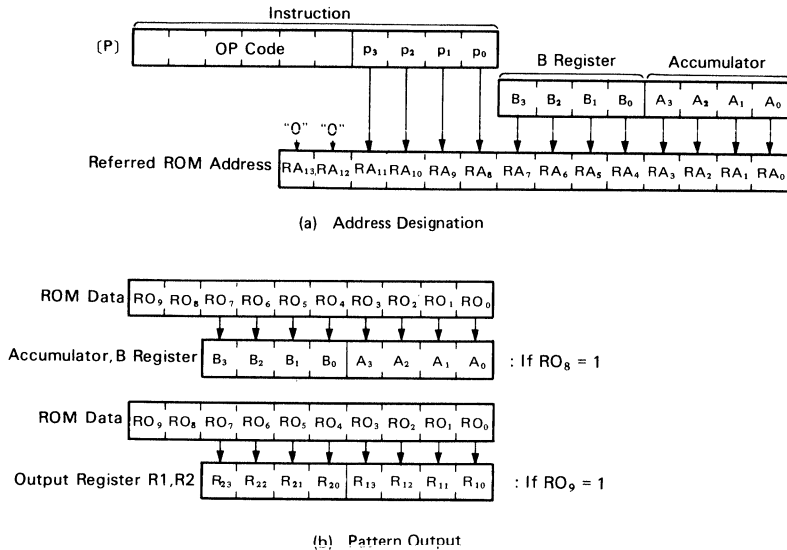


Fig. 23 P Instruction

● P Instruction

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred

ROM data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

● Description of the branch destination on page boundary

When BR is on page boundary ($256n + 255$), BR instruction transfers the contents of PC to the next page with hardware architecture. Therefore, the program branches to the next page when using BR on page boundary.

The HMCS400 series cross macro assembler has automatic paging facility for ROM page.

■ INSTRUCTION SET

The HMCS404C/CL/AC provide 99 instructions. These instructions are classified into 10 groups as follows;

- (1) Immediate Instruction
- (2) Register-to-Register Instruction
- (3) RAM Address Instruction
- (4) RAM Register Instruction
- (5) Arithmetic Instruction
- (6) Compare Instruction
- (7) RAM Bit Manipulation Instruction
- (8) ROM Address Instruction
- (9) Input/Output Instruction
- (10) Control Instruction

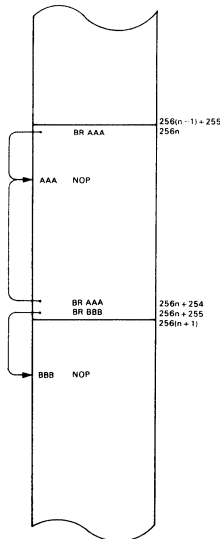


Fig. 24 The Branch Destination by BR Instruction on the Boundary between Pages

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i→A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i→B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i→M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i→M,Y+1→Y	NZ	1/1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B→A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A→B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y→A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX→A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY→A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m)→A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m)↔A		1/1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i→W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i→X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i→Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A→X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A→Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1→Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1→Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A→Y	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	Y-A→Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X↔SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y↔SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X↔SPX,Y↔SPY		1/1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M,Y+1→Y(X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M,Y-1→Y(X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX, Y→SPY)		1/1



HMCS404C/HMCS404CL/HMCS404AC

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY (X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A + i → A	OVF	1 / 1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1 / 1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B - 1 → B	NB	1 / 1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1 / 1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1 / 1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		i / i
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1 / 1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1 / 1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1 / 1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1 / 1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1 / 1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1 / 1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1 / 1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A → A	OVF	2 / 2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A OVF → CA	OVF	1 / 1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A + CA → A OVF → CA	OVF	2 / 2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M - A - CA → A NB → CA	NB	1 / 1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M - A - CA → A NB → CA	NB	2 / 2
OR A and B	OR	0 1 0 1 0 0 0 0 1 0	A ∪ B → A		1 / 1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1 / 1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2 / 2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1 / 1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2 / 2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1 / 1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2 / 2



HMCS404C/HMCS404CL/HMCS404AC

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1 / 1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2 / 2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1 / 1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2 / 2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1 / 1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1 / 1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1 / 1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2 / 2
A Less or Equal to Memory	ALEM	0 0 0 0 1 0 1 0 0	A ≤ M	NB	1 / 1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2 / 2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1 / 1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1 / 1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1 / 1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2 / 2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1 / 1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2 / 2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1 / 1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2 / 2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1 / 1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2 / 2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2 / 2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1 / 2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2 / 2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1 / 1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1 / 3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA RESTORE		1 / 3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1 / 1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1 / 1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1 / 1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1 / 1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1 / 1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1 / 1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1 / 1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1 / 1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1 / 1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1 / 1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1 / 2



HMCS404C/HMCS404CL/HMCS404AC

Table 31. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD/ CYCLE
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1 / 1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1 / 1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1 / 1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1 / 1

Table 32. Op-Code Map

R9	0																1															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	XSPX	XSPY	XSPY	AN	EM				AM											ANEM											
1	RTN	RTN		ALEM					AMC												ALEM											
2										INEM												INEMD										
3										ILEM													ILEMD									
4	LBM(XY)			BNEM						LAB											COMB			OR		STS			SBY	STOP		
5	LMAY(X)			AAY						LSPY													JMPL									
6	NEGA			RED						LSPX														CALL								
7										YNEI														BRL								
8	XMA(XY)									SEM n(2)														SEMD n(2)								
9	LAM(XY)									REM n(2)														LAMD								
A	LAM(XY)									SMC														LMAD								
B										UAA																						
C	XMB(XY)									LBA																						
D	LMADY(X)									SY																						
E	TD									SED																						
F										LXA																						
1										LWI i(2)																						

 ... 1-word/2-cycle Instruction
 ... 1-word/3-cycle Instruction
 ... RAM Direct Instruction (2-word/2-cycle)
 ... 2-word/2-cycle Instruction

HMCS404C/HMCS404CL/HMCS404AC

HMCS404C/CL/AC
MASK OPTION LIST

5V Operation : HMCS404C
3V Operation : HMCS404CL
High Speed Operation : HMCS404AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

* Please enter check marks in (■, X, ✓).

(1) I/O Option

Note (I/O options masked by ■ are not available.)

PIN	INPUT/OUTPUT	I/O OPTION					PIN	INPUT/OUTPUT	I/O OPTION				
		A	B	C	D	E			A	B	C	D	E
D ₀	Input/Output				■	■	R ₃₀	Input/Output				■	■
D ₁	Input/Output				■	■	R ₃₁	Input/Output				■	■
D ₂	Input/Output				■	■	R ₃₂	Input/Output				■	■
D ₃	Input/Output				■	■	R ₃₃	Input/Output				■	■
D ₄	Input/Output				■	■	R ₄₀	Input/Output				■	■
D ₅	Input/Output				■	■	R ₄₁	Input/Output				■	■
D ₆	Input/Output				■	■	R ₄₂	Input/Output				■	■
D ₇	Input/Output				■	■	R ₄₃	Input/Output				■	■
D ₈	Input/Output				■	■	R ₅₀	Input/Output				■	■
D ₉	Input/Output				■	■	R ₅₁	Input/Output				■	■
D ₁₀	Input/Output				■	■	R ₅₂	Input/Output				■	■
D ₁₁	Input/Output				■	■	R ₅₃	Input/Output				■	■
D ₁₂	Input/Output				■	■	R ₆₀	Output				■	■
D ₁₃	Input/Output				■	■	R ₆₁	Output				■	■
D ₁₄	Input/Output				■	■	R ₆₂	Output				■	■
D ₁₅	Input/Output				■	■	R ₆₃	Output				■	■
							R ₇₀	Output				■	■
							R ₇₁	Output				■	■
							R ₇₂	Output				■	■
							R ₇₃	Output				■	■
							R ₈₀	Output				■	■
							R ₈₁	Output				■	■
							R ₈₂	Output				■	■
							R ₈₃	Output				■	■
							R ₉₀	Input				■	■
							R ₉₁	Input				■	■
							R ₉₂	Input				■	■
							R ₉₃	Input				■	■
							RA0	Input				■	■
							RA1	Input				■	■

* Please enter "O" in applicable item for I/O option selection.

- A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
C: CMOS (not be used as Input) D: Without Pull-down MOS (PMOS Open Drain) E: With Pull-down MOS

(2) RA1/V_{disp}

RA1/V _{disp}	
<input type="checkbox"/> RA1: Without Pull-down MOS (D)	
<input type="checkbox"/> V _{disp}	

(3) Package

Package	
<input type="checkbox"/> DP-64S (shrink package)	
<input type="checkbox"/> FP-64	

* Please enter check marks (■, X, ✓) in applicable item. * Please enter check marks (■, X, ✓) in applicable item.

Note) RA1/V_{disp} has to be selected as V_{disp} pin except for the case that all High Pins are option D.

(4) Divider (DIV)

Clock Divide Ratio	
<input checked="" type="checkbox"/> Divided-by-8	

(5) ROM Code Media

ROM Code Media	
<input type="checkbox"/> EPROM: Emulator Type	
<input type="checkbox"/> EPROM: EPROM On-Package Microcomputer Type	

Check List of Application

(A) Oscillator (CPG option)

	<input type="checkbox"/> 404C (5V Operation)	<input type="checkbox"/> 404CL (3V Operation)	<input type="checkbox"/> 404AC (High Speed Operation)
	<input type="checkbox"/> Resistor (R _f = 20k.Ω±2%)		
CPG Option	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock

* Please enter check marks (■, X, ✓) in applicable item.



HMCS408C/HMCS408CL/ HMCS408AC (HD614080/HD614085/HD614088)

Description

The HMCS408C/CL/AC are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, Serial Interface and 2 timer/counter and contain high-voltage I/O pins including high-current output pins to drive fluorescent display tube directly.

Features

- 4-bit architecture
- 8192 words of 10-bit ROM
- 512 digits of 4-bit RAM
- 58 I/O pins, including 26 high-voltage I/O pins (40 V max)
- 2 Timer/counter
 - 11-bit prescaler
 - 8-bit free running timer/counter
 - 8-bit auto-reload timer/event counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
 - External: 2
 - Timer/counter: 2
 - Serial interface: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time
 - 0.89 μ s: HMCS408AC
 - 1.78 μ s: HMCS408C
 - 3.55 μ s: HMCS408CL
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate.
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data.
- On-chip oscillator
 - Crystal or ceramic filter (externally drivable)
- Package
 - 64-pin shrink dual in-line plastic package
 - 64-pin flat plastic package
- Instruction set compatible with HMCS 404; 101 instructions
- word ROM: 79 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts

- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD614P080S/HD614P0160S with the following fixed options:
 - I/O pin: open drain
 - Oscillator: crystal or ceramic filter oscillator (externally drivable)
 - Divider: Divided by 8
 - Package:
 - 64-pin shrink dual in-line plastic package
 - 64-pin flat plastic package
- Programming socket adapter for programming the EPROM-on-chip device

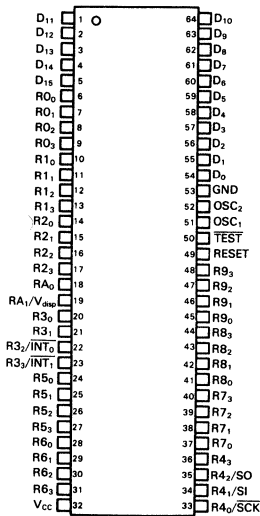
Type of Products

Item	HMCS408C	HMCS408CL	HMCS408AC
Power Supply (V)	3.5 to 6	2.5 to 6	4.5 to 6
Typical instruction Cycle Time (μ s)	2	4	1

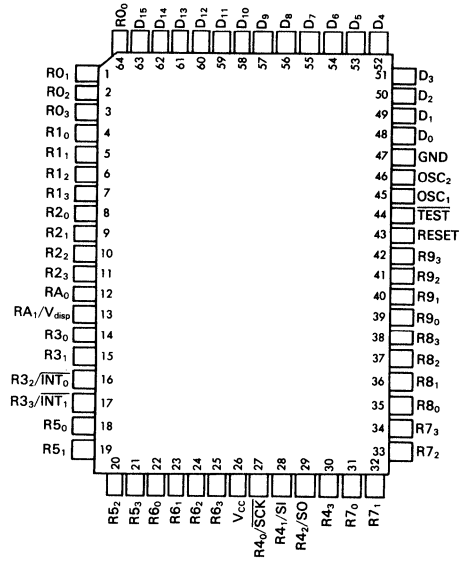


HMCS408C/HMCS408CL/HMCS408AC

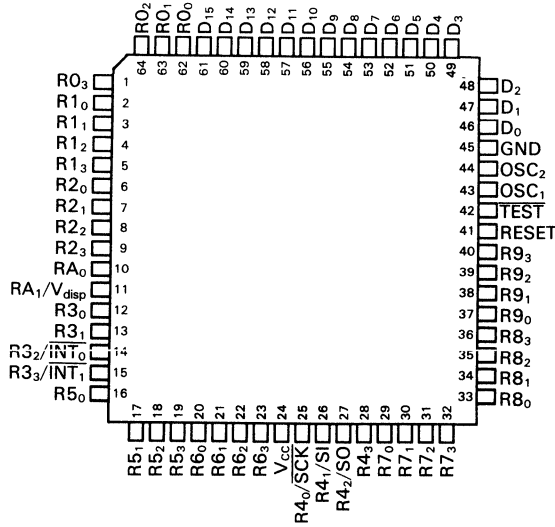
Pin Arrangement



(DP-64S, DC-64S)



(FP-64)

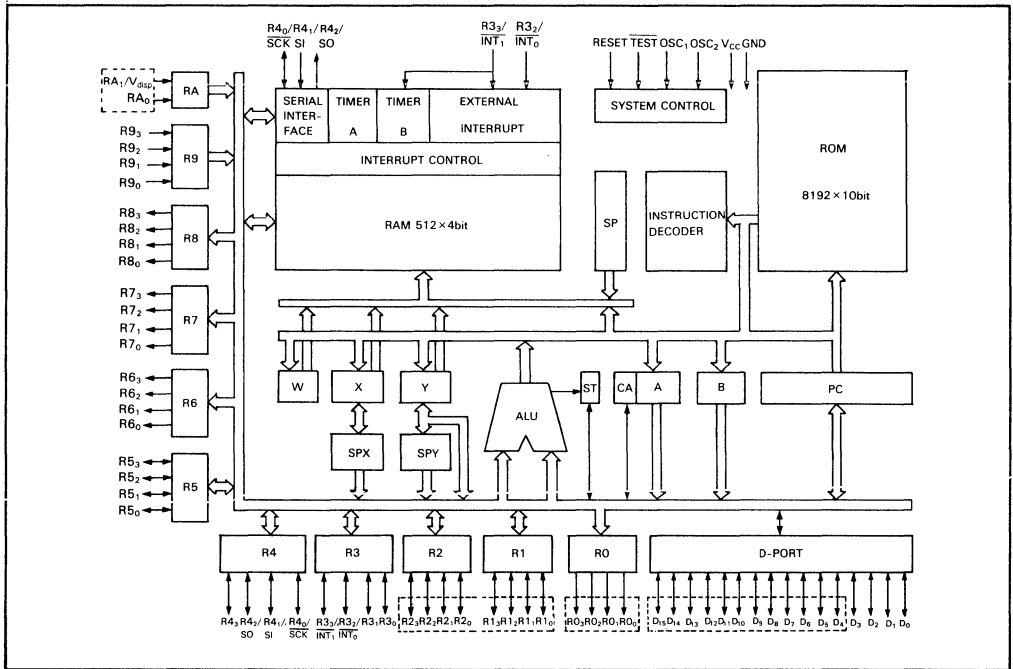


(FP-64A)

(Top View)



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC}-40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀-D₁₅ (D Port)

The D port is an input/output port addressed by the bit. These 16 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₅ are high-voltage pins. The circuit type for each

pin can be selected using a mask option. For details, see Input/Output section.

R0₀-R0₃, R1₀-R1₃, R2₀-R2₃, R3₀-R3₃, R4₀-R4₃, R5₀-R5₃, R6₀-R6₃, R7₀-R7₃, R8₀-R8₃, R9₀-R9₃, RA₀, RA₁ (R Ports)

R0 to R9 are 4-bit I/O ports. RA is a 2-bit port. R0, R6, R7 and R8 are an output port, R9 and RA are an input port, and R1 to R5 I/O ports. R0, R1, R2, and RA are high-voltage ports, and R3 to R9 are standard ports. Each pin has a mask option which selects its circuit type. The pins R3₂, R3₃, R4₀, R4₁ and R4₂ are multiplexed with INT₀, INT₁, SCK, SI and SO respectively. For details, see Input/ Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R3₂ and R3₃ respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI) and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R4₀, R4₁ and R4₂ respectively. For details, see Serial interface.

Functional Description

ROM Memory Map

The MCU includes 8,192 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations

\$0000 through \$0FFF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

RAM Memory Map

The MCU includes 512 digits of 4-bits RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible

only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Special Function Registers Area (\$004 to \$00B): The special function registers are the

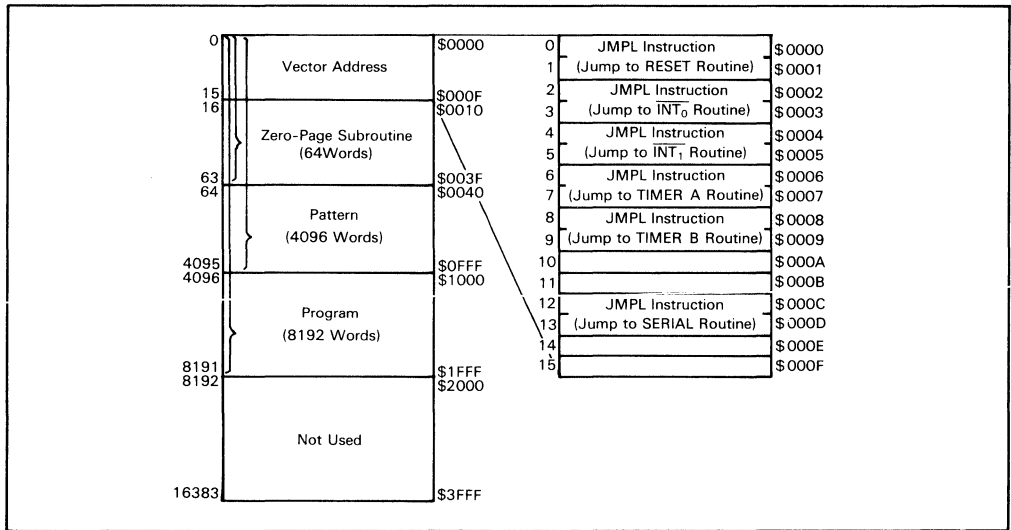
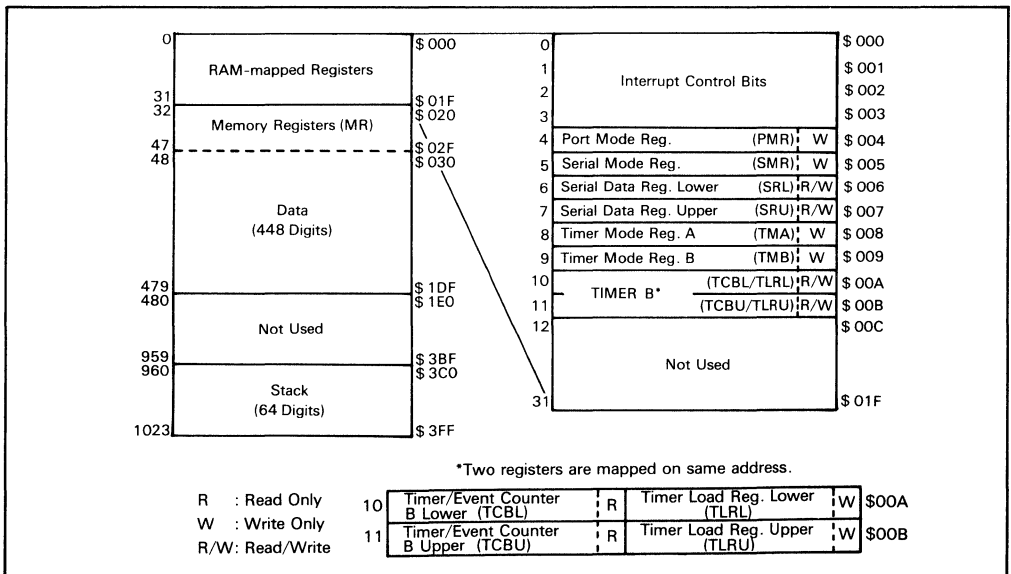


Figure 1. ROM Memory Map



HMCS408C/HMCS408CL/HMCS408AC

Data Area (\$020 to \$1DF): 16 digits of \$020 through \$02F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

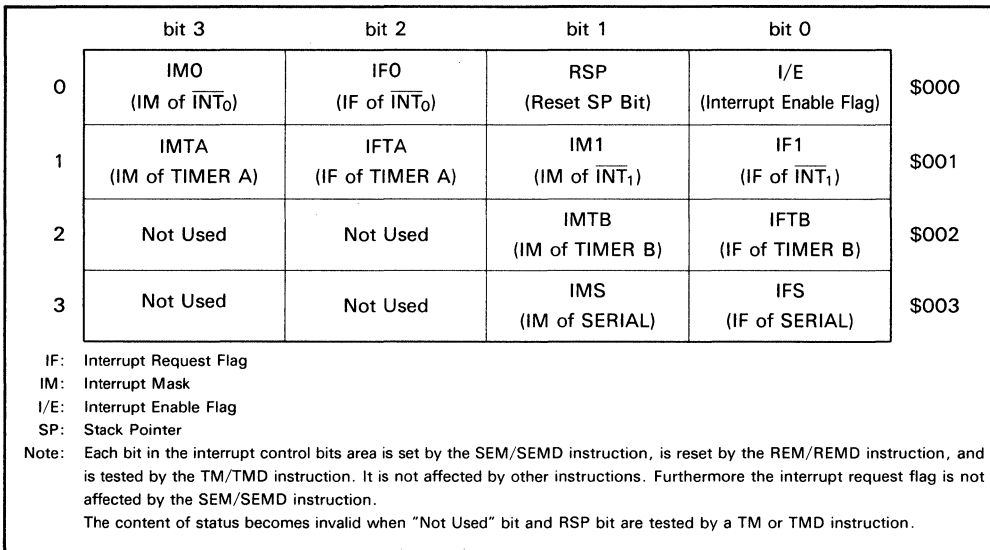


Figure 3. Configuration of Interrupt Control Bit Area

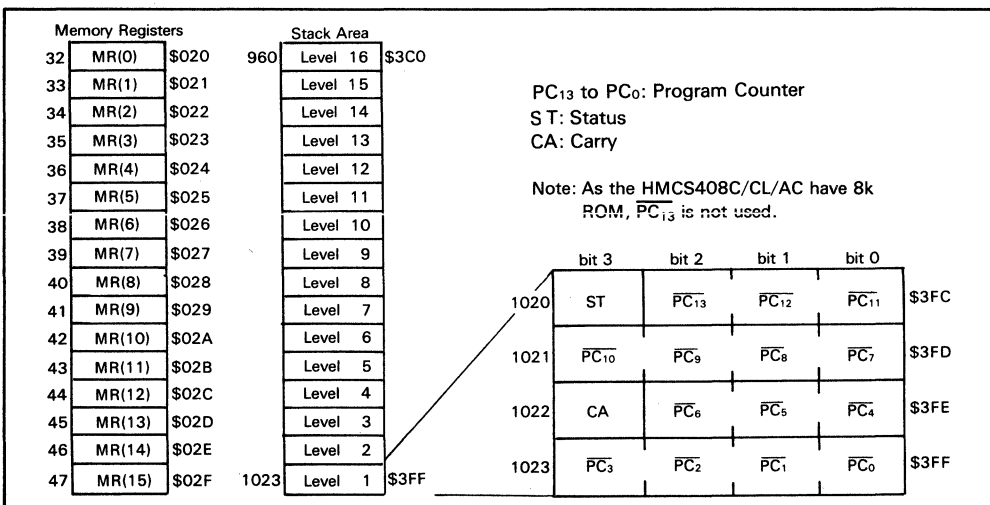


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W register is a write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI

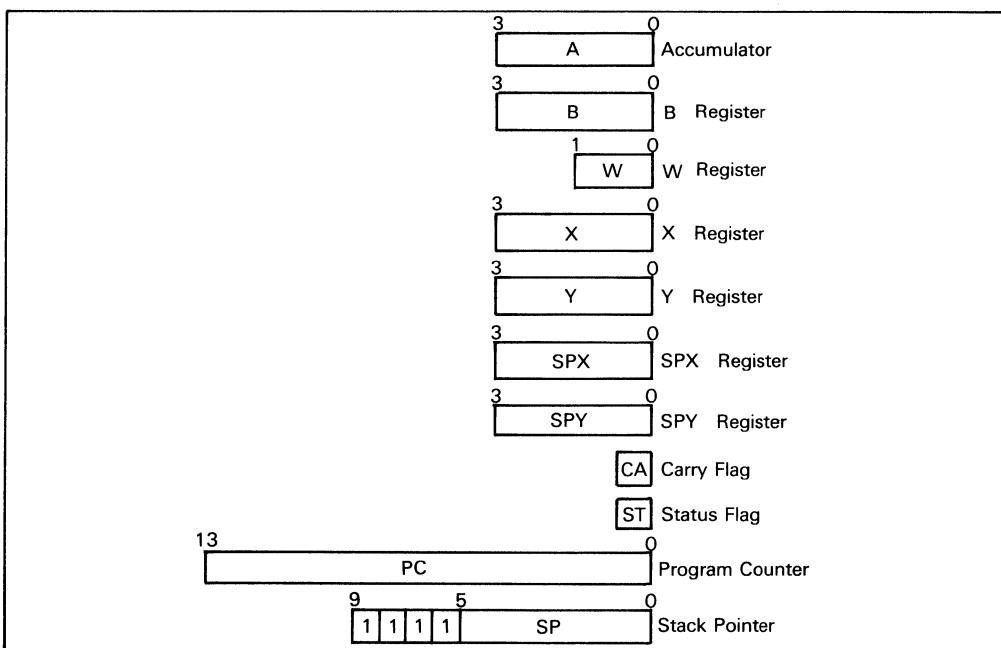
instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it.



The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timer A, timer B), and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and

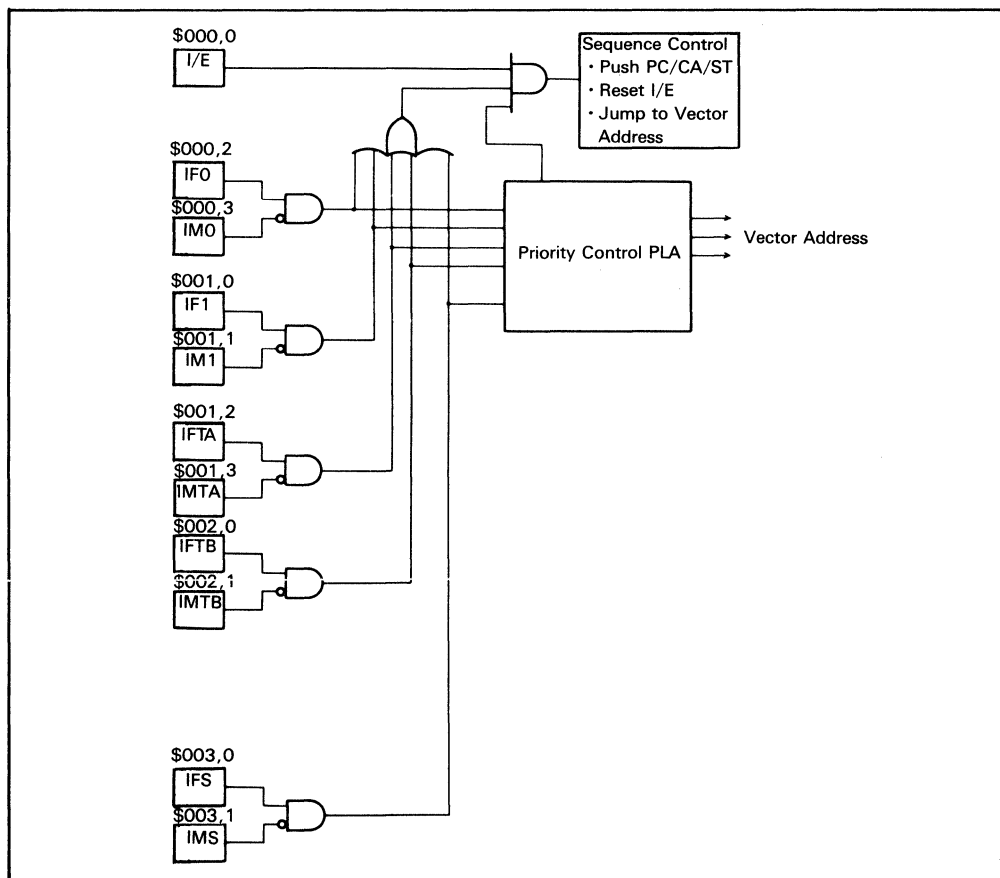


Figure 6. Interrupt Control Circuit Block Diagram



vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is

reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF_0 , IF_1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF_0 : \$000 bit 2, IF_1 : \$001 bit 0): The external interrupt request flags (IF_0 , IF_1) are set at the

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer A	Timer B	Serial
I/E	1	1	1	1	1
$IF_0 \cdot \overline{IM_0}$	1	0	0	0	0
$IF_1 \cdot \overline{IM_1}$	*	1	0	0	0
$IFTA \cdot \overline{IMTA}$	*	*	1	0	0
$IFTB \cdot \overline{IMTB}$	*	*	*	1	0
$IFS \cdot \overline{IMS}$	*	*	*	*	1

* Don't care



falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, $R3_3/\overline{INT}_1$ pin, $R4_1/SI$ pin, and $R4_2/SO$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin

PMR1	$R4_1/SI$ Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2/SO$ Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

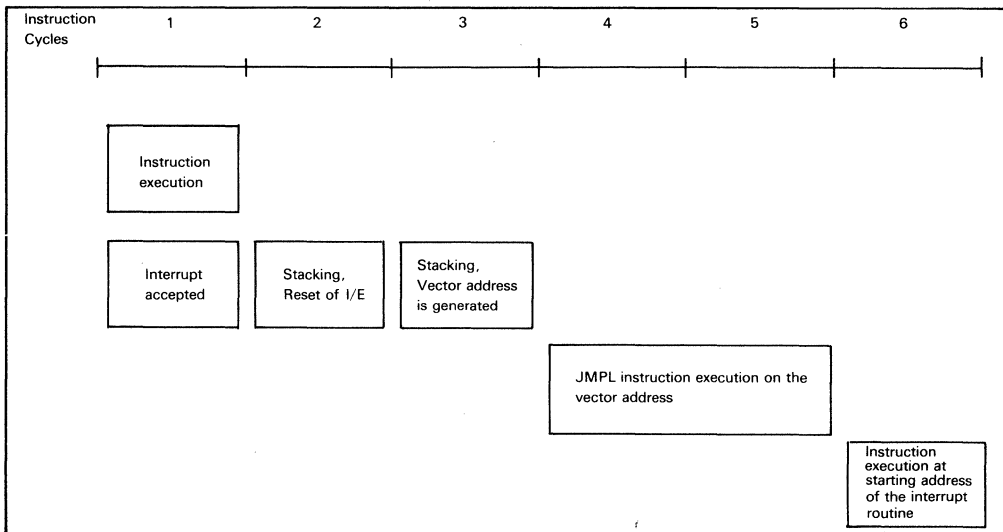


Figure 7. Interrupt Servicing Sequence

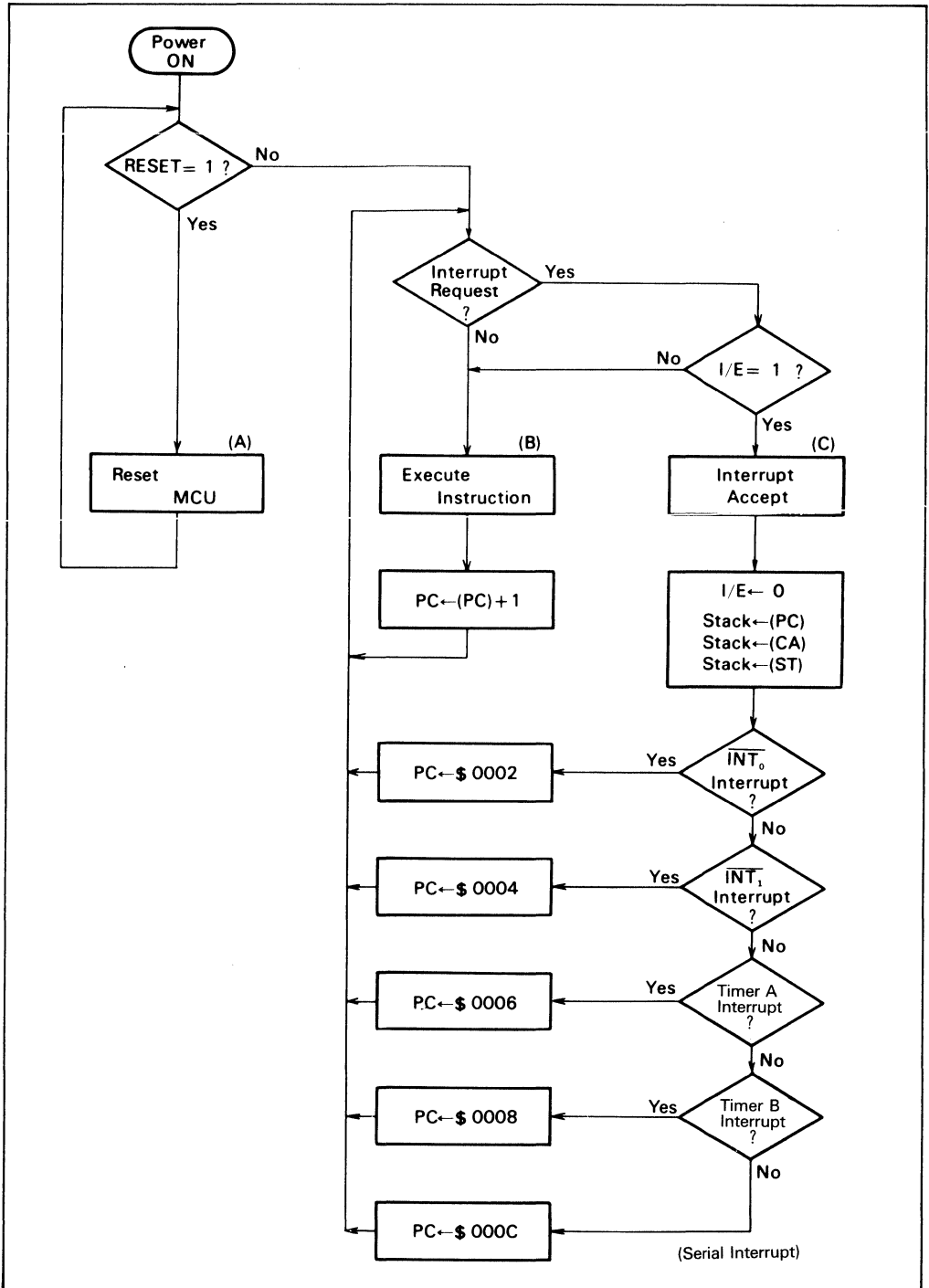


Figure 8. Interrupt Servicing Flowchart



Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. This consists of the serial data register, the serial mode register, the octal counter and the multiplexer as illustrated in figure 9. Pin R4₀/SCK and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

STS instruction is used to initiate serial interface operations and to reset the octal counter to \$0. The counter starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of the SCK. When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the R4₀/SCK, prescaler divide ratio, and transfer clock source as shown in table 7. The write signal to the serial mode register controls the operating state of the serial

interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it will be necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SDR: \$006, SRU: \$007): The 8-bit read/write serial data register consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register will be output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the SI pin to the serial data register, to MSB first, synchronously with the rising edge of the

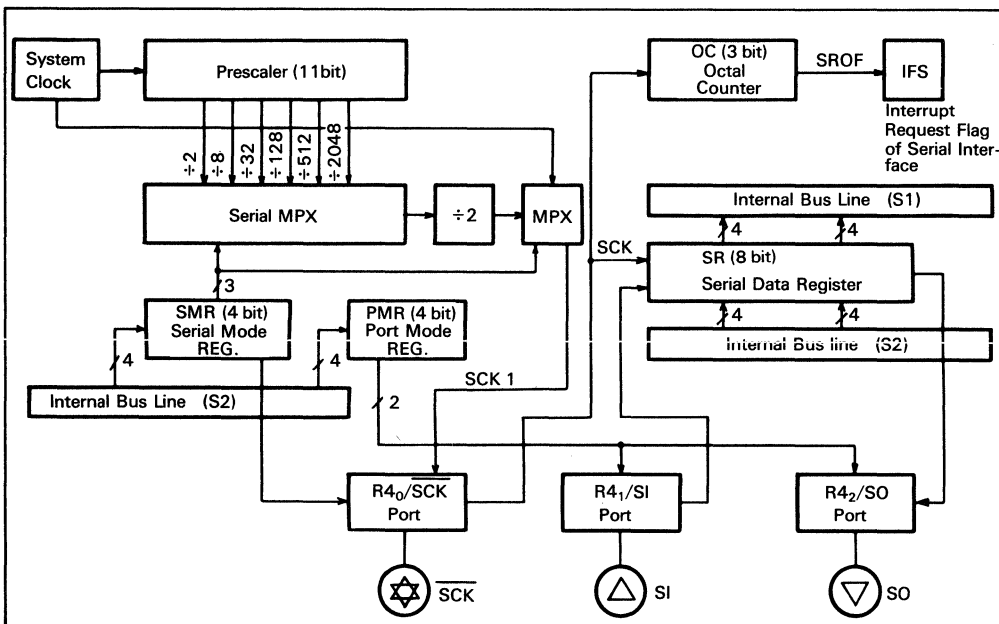


Figure 9. Serial Interface Block Diagram



transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Serial Interrupt Request Flag (IFS: S003 bit 0): The serial Interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: S003 bit 1): The serial Interrupt mask masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register. Initialize the serial interface by the write signal to the serial mode register, when the operation mode is changed.

Table 7. Serial Mode Register

SMR3	R4 ₀ /SCK
0	Used as R4 ₀ port input/output pin
1	Used as SCK input/output pin

Transfer Clock							
SMR2	SMR1	SMR0	R4 ₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio	
0	0	0	SCK Output	Prescaler	÷ 2048	÷	4096
0	0	1	SCK Output	Prescaler	÷ 512	÷	1024
0	1	0	SCK Output	Prescaler	÷ 128	÷	256
0	1	1	SCK Output	Prescaler	÷ 32	÷	64
1	0	0	SCK Output	Prescaler	÷ 8	÷	16
1	0	1	SCK Output	Prescaler	÷ 2	÷	4
1	1	0	SCK Output	System Clock	—	÷	1
1	1	1	SCK Input	External Clock	—	—	—

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

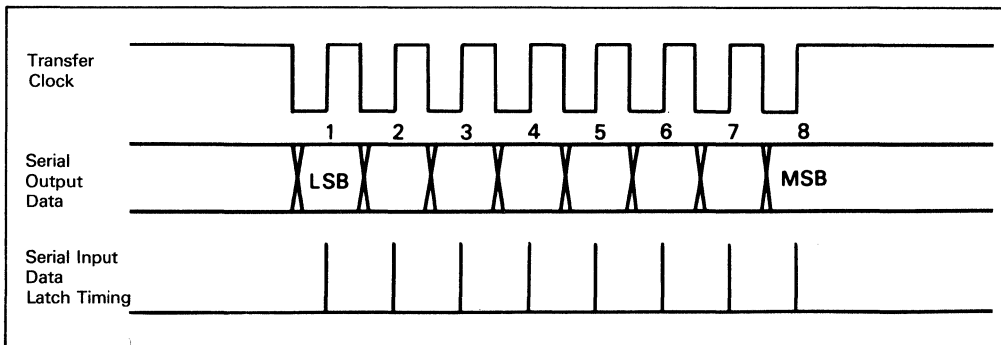


Figure 10. Serial Interface I/O Timing Chart

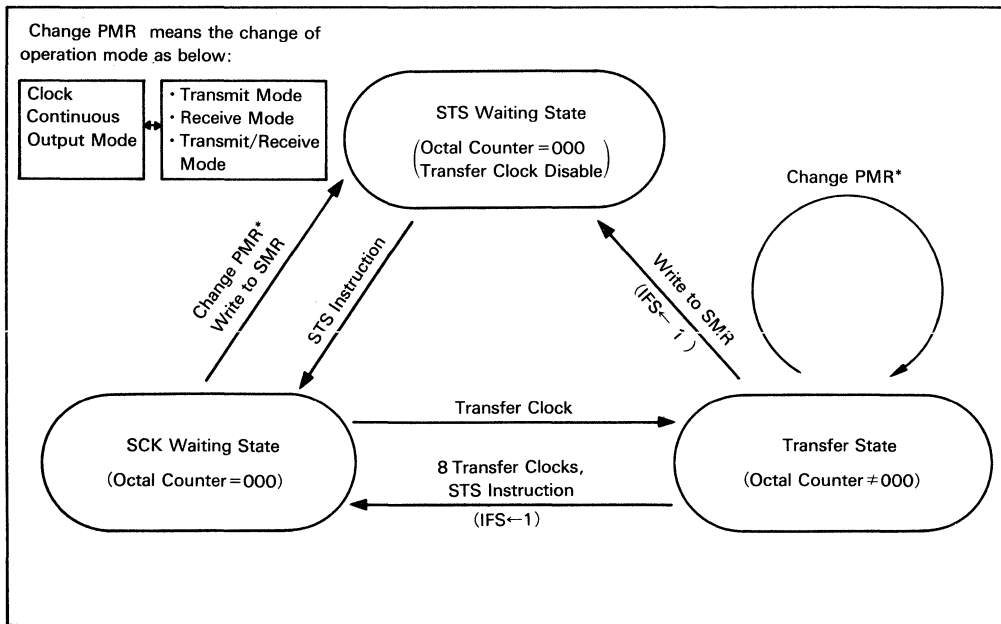


Figure 11. Serial Interface Operation State



Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK waiting state.

In this state the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the Octal Counter counts-up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.

The octal counter becomes 000 again by 8 transfer clocks or by execution of STS instruction, so that the serial interface returns to SCK waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops after 8 clocks.

Example of Transfer Clock Error Detection: The serial interface functions abnormally when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 12.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts as the following sequence: first, transfer state, second, SCK waiting state and third, transfer state again. The serial Interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial Interface Request Flag to be set again.

Timer

The MCU contains a prescaler and a timer/counter (timer A, timer B, figure 13) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial inter-

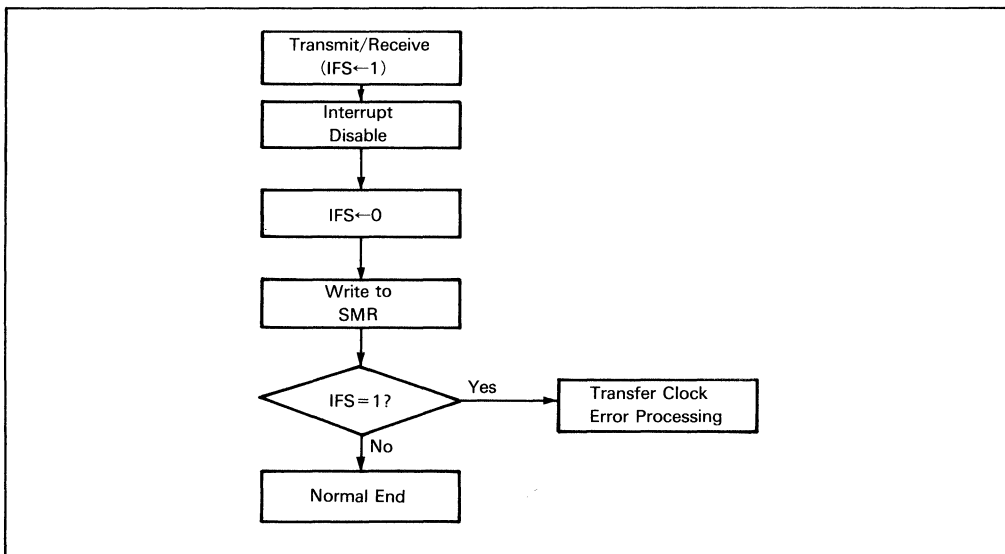


Figure 12. Example of Transfer Clock Error Detection



face. The prescaler divide ratio is selected by the timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up to \$FF, timer A is set to \$00 again, and generating overflow output. This leads to setting timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from oc-

curing.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: \$008): The timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input, as shown in Table 11.

The timer mode register A is initialized to \$0 by MCU reset.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initial-

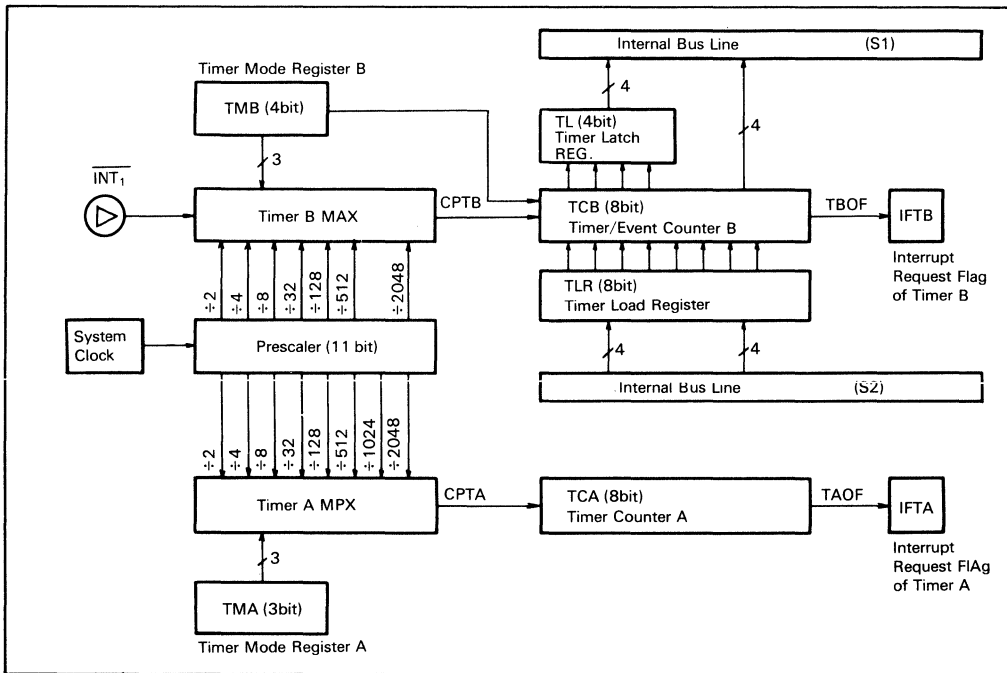


Figure 13. Timer Block Diagram



ized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set by the overflow output to time A (table 13).

Timer A Interrupt Mask (IMTA: \$001 bit 3): Timer A interrupt mask prevents an interrupt request generated by timer A Interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B Interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 16).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler	Divide Ratio
0	0	0	÷	2048
0	0	1	÷	1024
0	1	0	÷	512
0	1	1	÷	128
1	0	0	÷	32
1	0	1	÷	8
1	1	0	÷	4
1	1	1	÷	2

Table 12. Timer Mode Register B

TMB3			Auto-reload Function
0			No
1			Yes

			Prescaler	Divide Ratio,	Clock Input Source
TMB2	TMB1	TMB0	÷	2048	
0	0	0	÷	512	
0	0	1	÷	128	
0	1	0	÷	32	
0	1	1	÷	8	
1	0	0	÷	4	
1	0	1	÷	2	
1	1	0	÷		
1	1	1			INT ₁ (External Event Input)

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

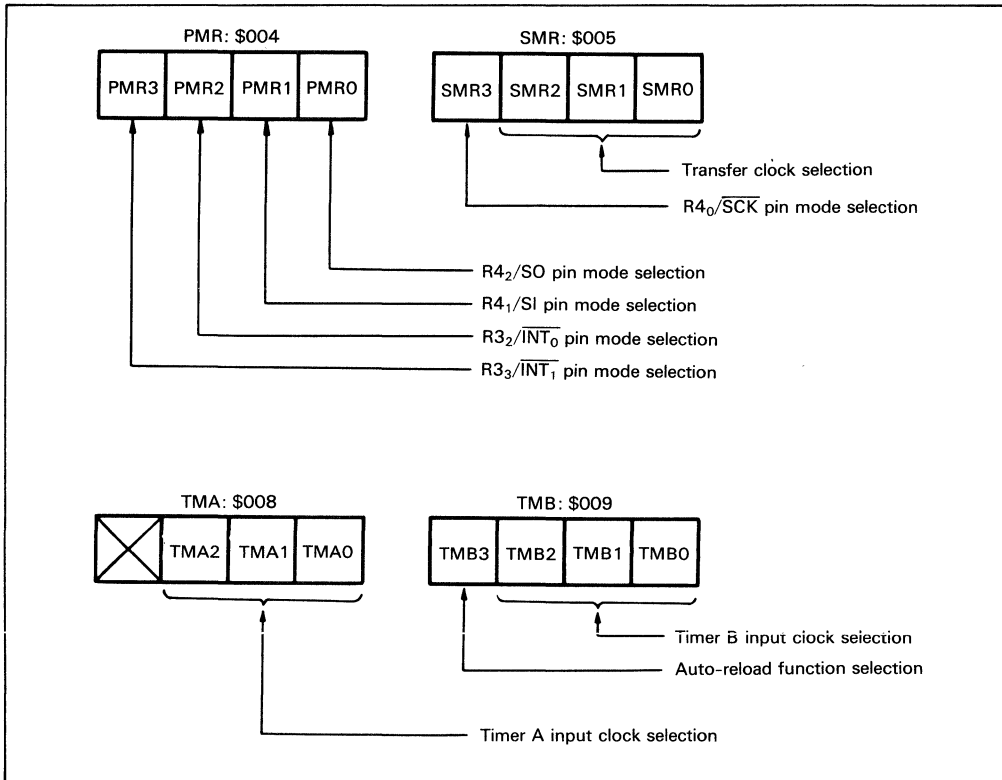


Figure 14. Mode Register Configuration and Function

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_1/V_{disp} pin via mask option when at least one high-voltage pin is selected as with pull-down MOS option. See table 17 as for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the \overline{HLT} signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D port is an I/O port which has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 17 as for the classifica-

tion of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports in the HMCS408 are composed of 20 I/O pins, 16 output-only pins, and 6 input-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read by reading from the output-only and/or non-existing ports.

The R_{3_2} , R_{3_3} , R_{4_0} , R_{4_1} , and R_{4_2} pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, \overline{SCK} , \overline{SI} , and \overline{SO} pins respectively. See table 17 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-down MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

R_{4_0}/\overline{SCK} and R_{4_2}/\overline{SO} should be used as R_{4_0} and R_{4_2} by serial mode register and port mode register respectively.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 19 shows the parts initialized by MCU reset, and the status of each.

Table 17. I/O Pin Circuit Types

	Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable pins
Standard Pins	<p>I/O Common Pins</p>			<p>D₀ - D₃ R₃₀ - R₃₃ R₄₀ - R₄₃ R₅₀ - R₅₃</p>
	<p>Output pins</p>			<p>R₆₀ - R₆₃ R₇₀ - R₇₃ R₈₀ - R₈₃</p>
	<p>Input pins</p>			<p>R₉₀ - R₉₃</p>

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applicable pins
High Voltage Pins	I/O Common Pins			D ₄ - D ₁₅ R ₁₀ - R ₁₃ R ₂₀ - R ₂₃
	Output Pins			R ₀₀ - R ₀₃
	Input Pins			RA ₀
	Input Pins			RA ₁

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applicable pins
Standard Pins	I/O Common Pins			SCK (Note 2) (Output mode)
	Output pins			SO
	Input Pins			$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$ SI $\overline{\text{SCK}}$ (Input mode)

- Notes: 1. In the stop mode, HLT signal is 0, HLT signal is 1 and I/O pins are in high impedance state.
 2. If the MCU is interrupted by serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 18. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0

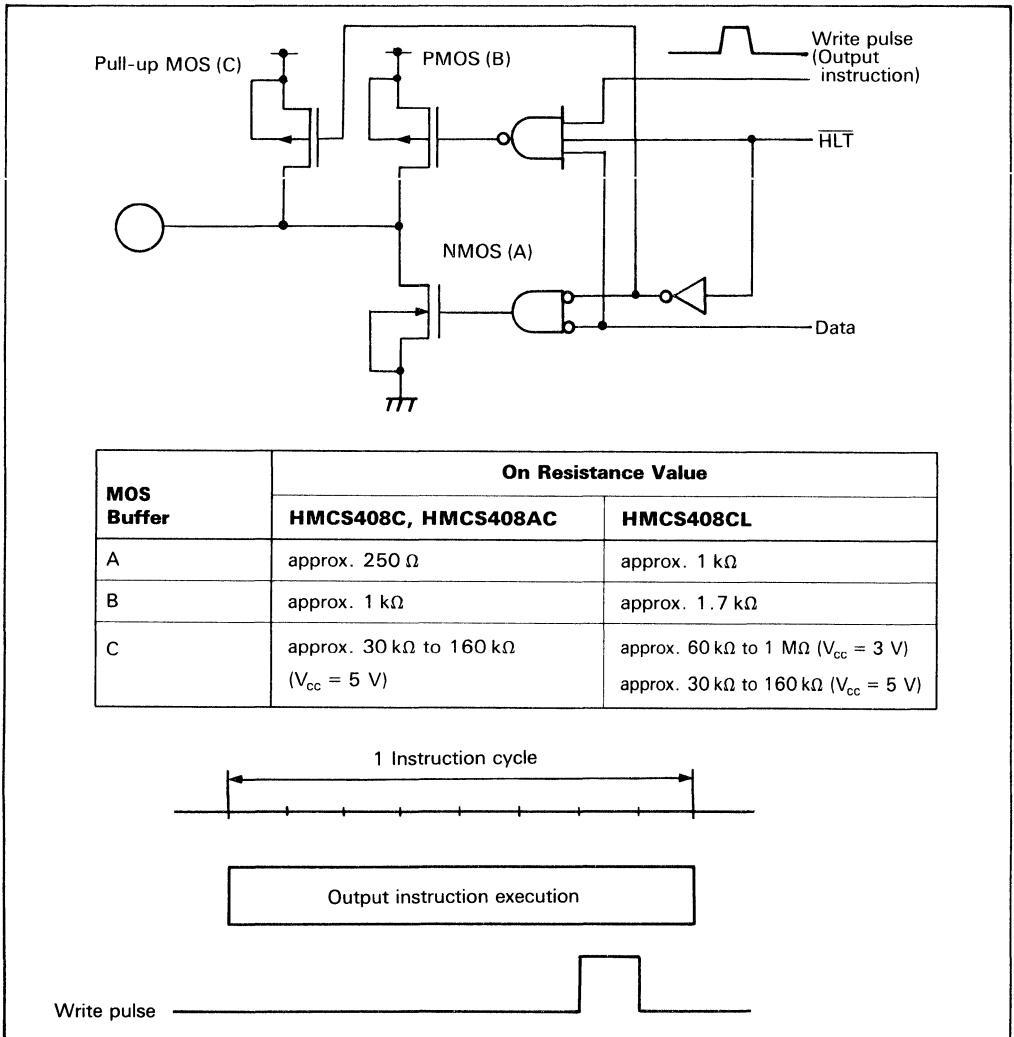


Figure 15. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Table 19. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional/ branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin (A) Without Pull-Up MOS	1	Enable to input
	(B) With Pull-Up MOS	1	Enable to input
	(C) CMOS	1	—
	High Voltage Pin (D) Without Pull-Down MOS	0	Enable to input
	(E) With Pull-Down MOS	0	Enable to input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Serial Mode Register (SMR)	0000	See serial mode register
	Timer Mode Register A (TMA)	000	See timer mode register A
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Counter A (TCA)	\$00	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—
	Octal Counter	000	—

Note: MCU reset affects the rest of registers as follows:

HMCS408C/HMCS408CL/HMCS408AC

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Through mask option, either crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table

21 for selection of the type. In addition, see figure 17 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available. Three divide ratios, 1/16, 1/8, and 1/4, are selectable via mask option (table 20).

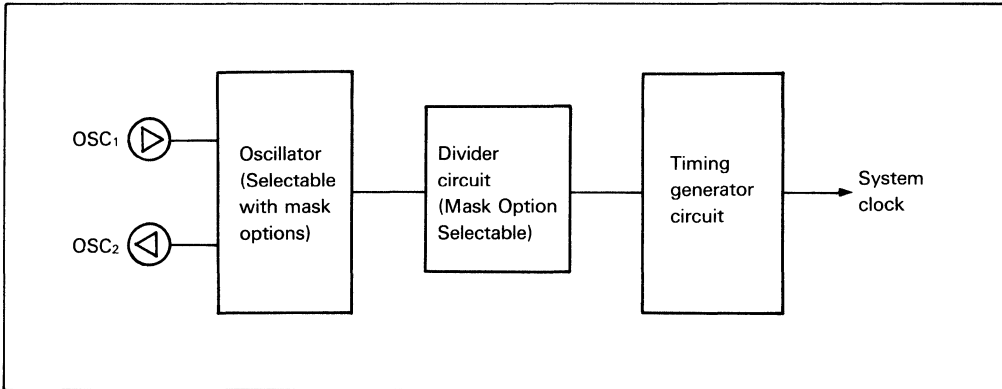


Figure 16. Internal Oscillator Circuit

Table 20. Internal Oscillation Circuit Mask Option

		HMCS 408C	HMCS 408CL	HMCS 408AC
Divider	1/16	—	○	—
	1/8	○	○	○
	1/4	○	—	○
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○

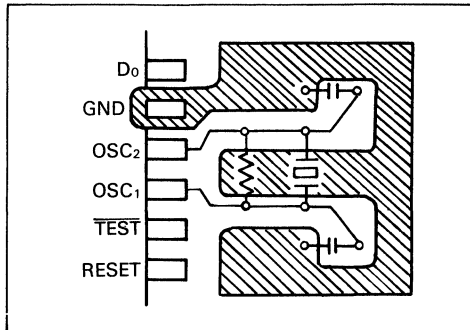
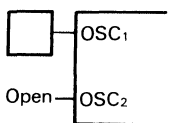
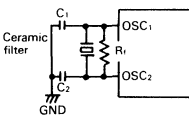
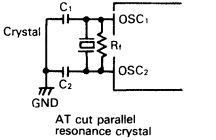
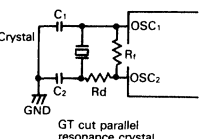


Figure 17. Layout of Crystal and Ceramic Filter

Table 21. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants		
		HMCS408C	HMCS408CL	HMCS408AC
External Clock Operation				
Ceramic Filter Oscillator		Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA 8.00MT CSA 4.00MG (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$
Crystal Oscillator	 <p>AT cut parallel resonance crystal</p>	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}9.0\text{ MHz}$
	 <p>GT cut parallel resonance crystal</p>		$R_f: 2\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}2.25\text{ MHz}$	

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 17).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 22). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 22. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Condition			Input/Output Pin	Timer/Counter, Serial Interface	Recovery Method
				Register, Flag	Interrupt Function	RAM			
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ³	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ¹	Stop	Retained	High impedance ²	Stop	RESET input

- Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to table 19 for the contents of the flags and registers.
 2. A high-voltage pin with a pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is the additional current to the current dissipation in stop mode (I_{stop}).
 3. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

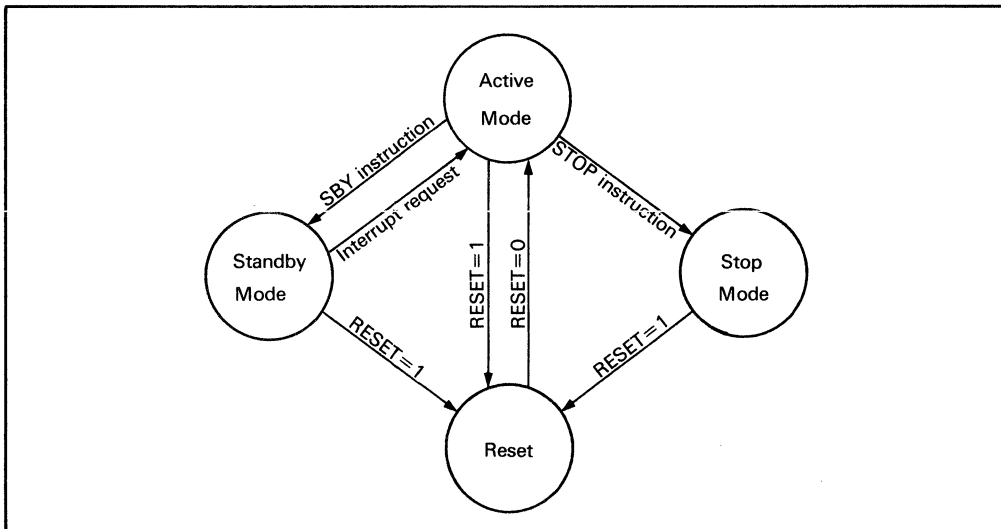


Figure 18. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 19 shows the flowchart of the standby

mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM

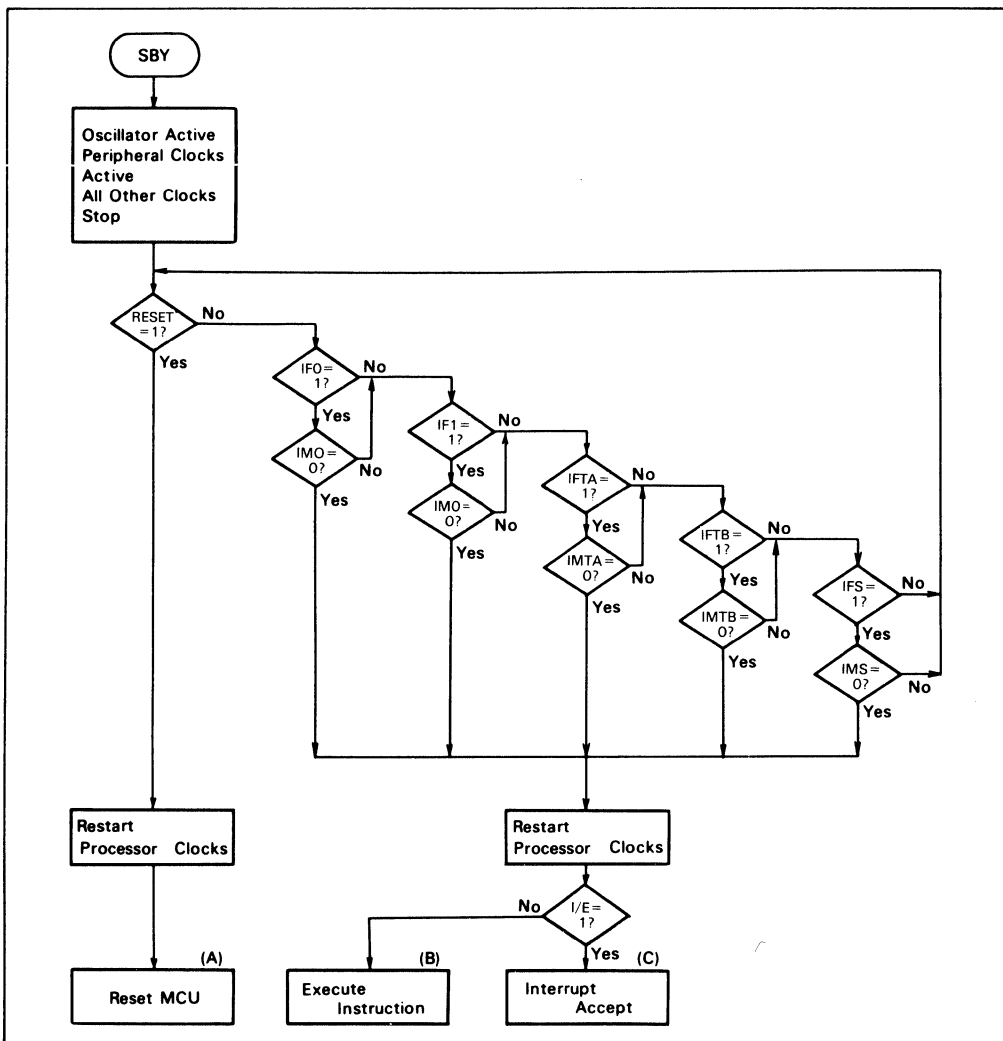


Figure 19. MCU Operating Flowchart in Standby Mode

retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

RAM Addressing Mode

As shown in Figure 21, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 22.

Direct addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page.

This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on page boundary (256n + 255) (figure 23), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 24). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

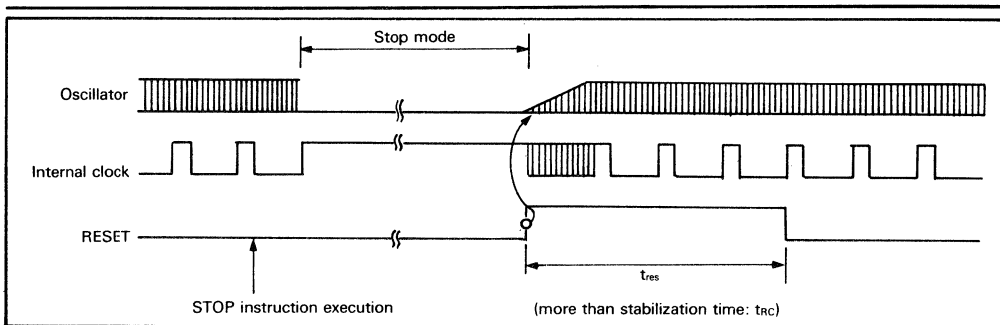


Figure 20. Timing Chart of Recovering from Stop Mode



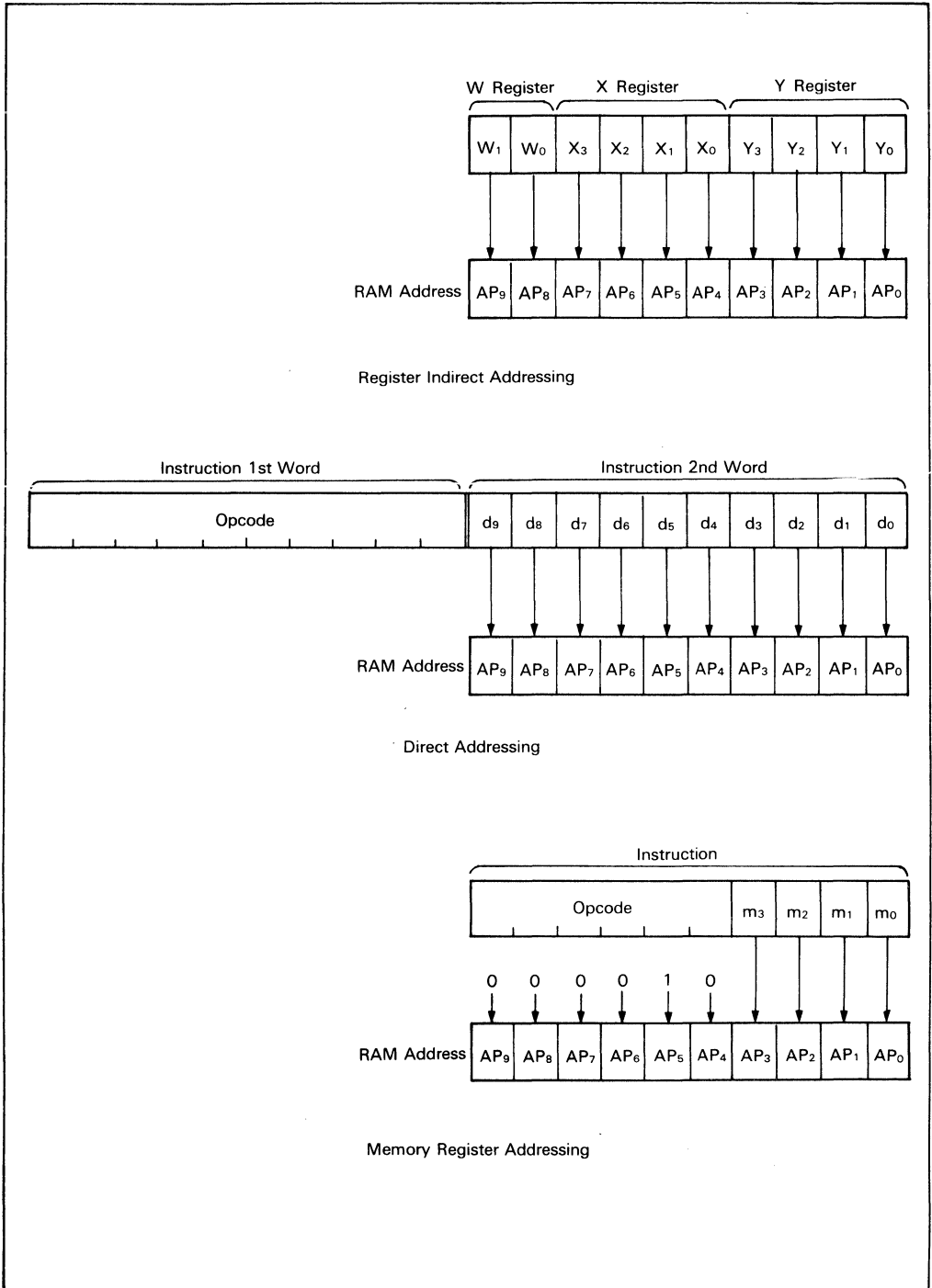


Figure 21. RAM Addressing Mode



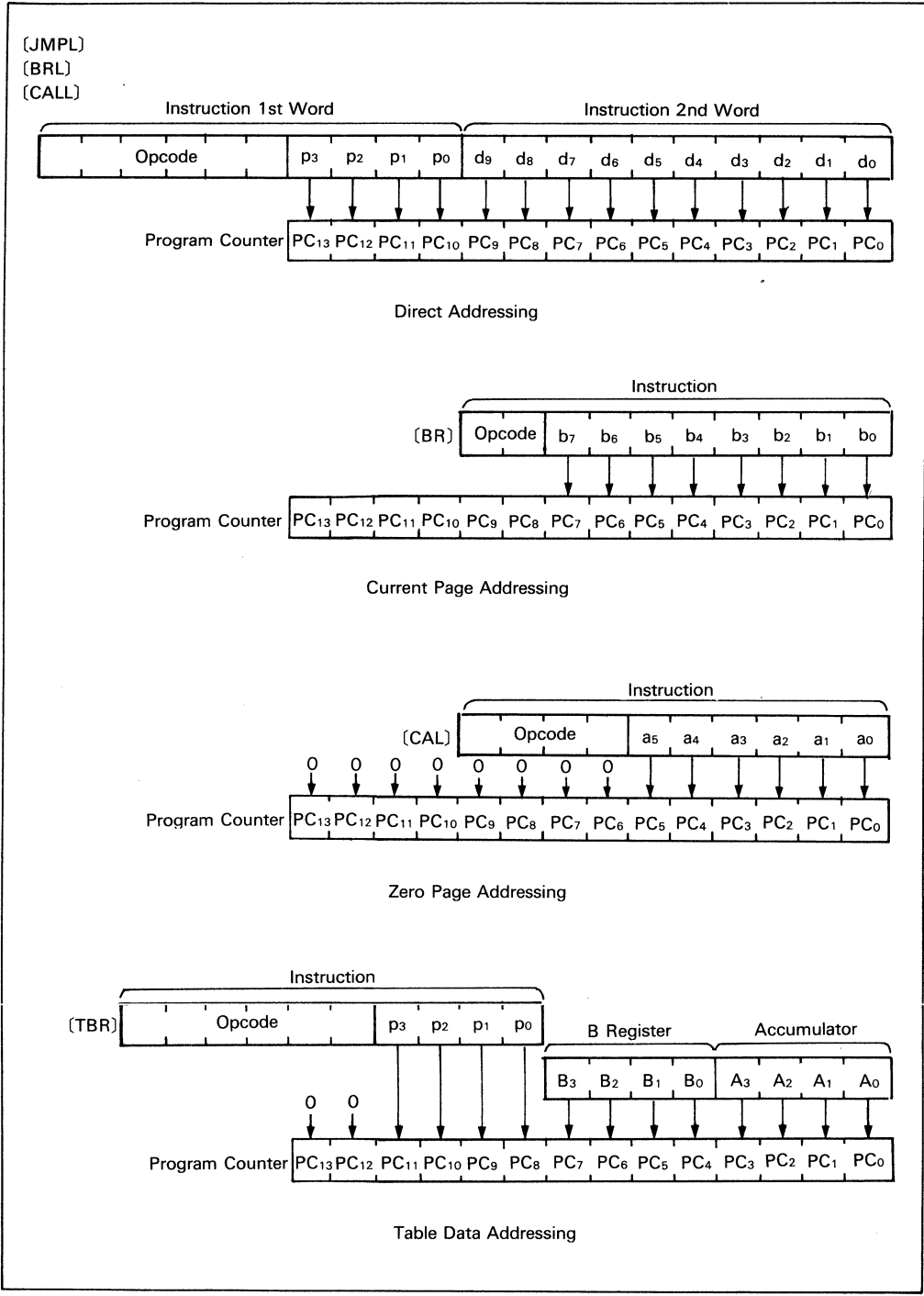


Figure 22. ROM Addressing Mode



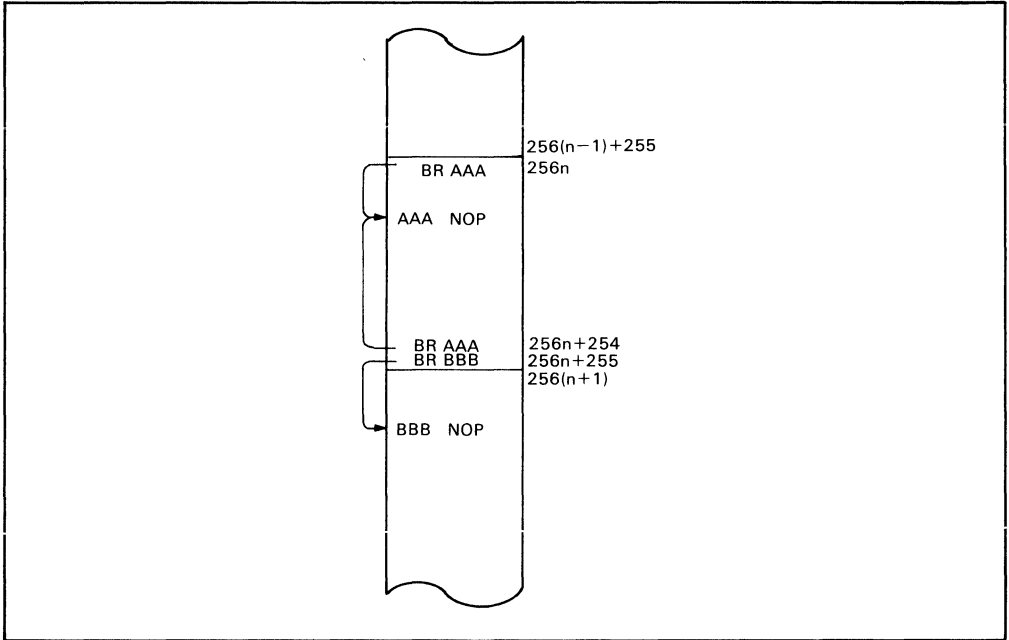


Figure 23. The Branch Destination by BR Instruction on the Boundary between Pages

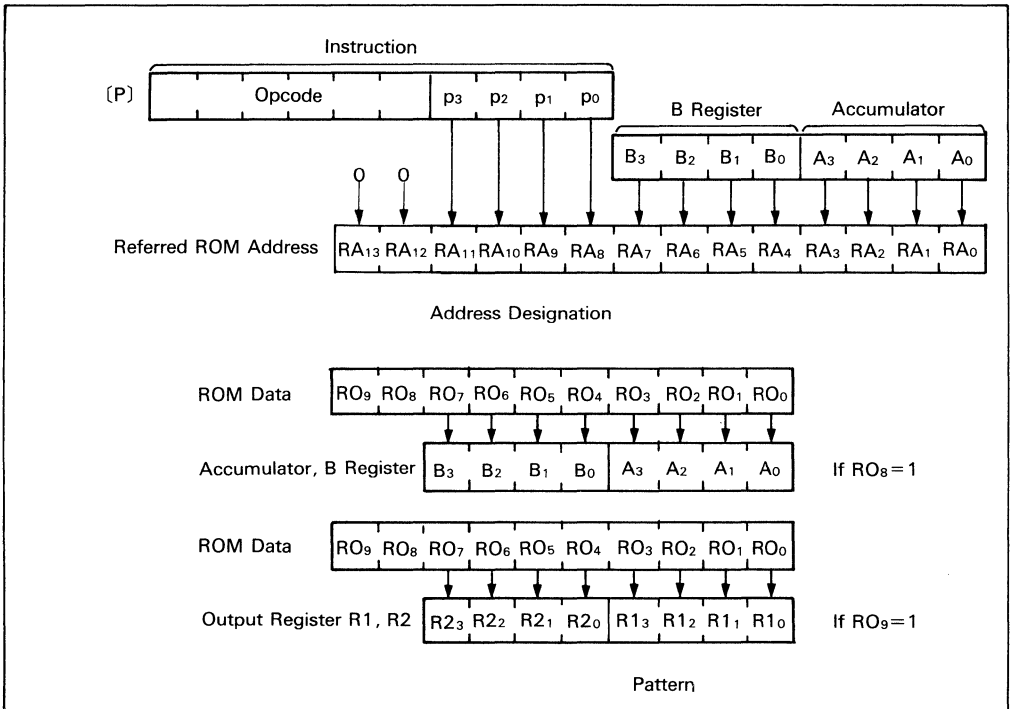


Figure 24. P Instruction

HMCS408C/HMCS408CL/HMCS408AC

Instruction Set

The HMCS408C/CL/AC provide 99 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction

5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 23-32 list their functions, and table 33 is an opcode map.

Table 23. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 24. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.



Table 25. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

HMCS408C/HMCS408CL/HMCS408AC

Table 26. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X → SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 27. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ OVF $\rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ OVF $\rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ NB $\rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ NB $\rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

HMCS408C/HMCS408CL/HMCS408AC

Table 28. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≦ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≦ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≦ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≦ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≦ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≦ i	NB	1/1

Table 29. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2



Table 30. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 -I/E CA Restore	ST	1/3

Table 31. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 32. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

HMCS408C/HMCS408CL/HMCS408AC

Table 33. Opcode Map

R8		0																1															
R9	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	NOP	XSP	XSP	XSP	XSP	AN	EM	/	AM	/	/	/	ORM	/	/	/	/	/	/	/	ANEMD	/	/	AMCD	/	/	/	ORMD	/	/	/	
	1	RTN	RTN	/	/	ALEM	/	/	AMC	/	/	/	EORM	/	/	/	/	/	/	/	ALEMCD	/	/	AMCD	/	/	/	EORMD	/	/	/		
	2	INEM								i(4)								INEMD								i(4)							
	3	ILEM								i(4)								ILEMD								i(4)							
	4	LBM(XY)	/	/	ENEM	/	/	/	LAB	/	/	/	IB	/	/	/	COMB	/	/	OR	/	/	STS	/	/	/	SBY	STOP	/	/	/		
	5	LMAY(X)	/	/	AYY	/	/	/	LASY	/	/	/	IY	/	/	/	JMPL								p(4)								
	6	NEGA	/	/	RED	/	/	/	LASX	/	/	/	/	/	/	TC	CALL								p(4)								
	7	YNEI								i(4)								BRL								p(4)							
	8	XMA(XY)	/	/	SEM	n(2)	/	/	REM	n(2)	/	/	TM	n(2)	XVAD	/	/	/	SEMD	n(2)	/	/	REMD	n(2)	/	/	TMD	n(2)	/	/	/		
	9	LAM(XY)	/	/	LMA(XY)	/	/	/	SMC	/	/	/	ANM	/	/	/	LAMD	/	/	LMAD	/	/	/	SMCD	/	/	ANMD	/	/	/			
	A	ROTR	ROTL	/	/	/	DAA	/	/	DAS	/	/	/	/	LAY	LMID								i(4)									
	B	TBR								p(4)								P								p(4)							
	C	XMB(XY)	/	/	BLEM	/	/	/	LBA	/	/	/	/	/	DB	CAL								a(6)									
	D	LMADY(X)	/	/	SY	/	/	/	LYA	/	/	/	/	DY																			
	E	TD	/	/	SED	/	/	/	LXA	/	/	/	REC	/	SEC																		
	F	LWI				i(2)																											
1	0	LBI								i(4)																							
	1	LYI								i(4)																							
	2	LXI								i(4)																							
	3	LAI								i(4)																							
	4	LBR								m(4)																							
	5	LAR								m(4)																							
	6	REDD								m(4)																							
	7	LAMR								m(4)								BR				b(8)											
	8	AI								i(4)																							
	9	LMIIY								i(4)																							
	A	TDD								m(4)																							
	B	ALEI								i(4)																							
	C	LRB								m(4)																							
	D	LRA								m(4)																							
	E	SEDD								m(4)																							
	F	XMRA								m(4)																							

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction
 2-word/2-cycle Instruction (2-word/2-cycle)



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V	
Terminal Voltage	V_T	- 0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	- I_O	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Total Allowance of Output Current	- ΣI_O	150	mA	6
Operating Temperature	T_{opr}	- 20 to + 75	°C	
Storage Temperature	T_{stg}	- 55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. D₀-D₃ and R3-R8.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. D₀-D₃ and R3-R8.
 11. R0-R2.
 12. D₄-D₁₅.

HMCS408C/HMCS408CL/HMCS408AC

Electrical Characteristics

DC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,

HMCS408C: $V_{CC} = 3.5$ V to 6 V,

HMCS408CL: $V_{CC} = 2.5$ V to 6 V,

HMCS408AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, $\overline{\text{SCK}}$ R3 ₂ /INT ₀ , R3 ₃ /INT ₁	0.8 V_{CC}		$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V	HMCS408C/AC	
			$V_{CC} - 0.3$		$V_{CC} + 0.3$	V	HMCS408CL	
Input Low Voltage	V_{IL}	RESET, $\overline{\text{SCK}}$ R3 ₂ /INT ₀ , R3 ₃ /INT ₁	- 0.3		0.2 V_{CC}	V		
		SI	- 0.3		0.3 V_{CC}	V		
		OSC ₁	- 0.3		0.5	V	HMCS408C/AC	
			- 0.3		0.3	V	HMCS408CL	
Output High Voltage	V_{OH}	$\overline{\text{SCK}}$, SO	$V_{CC} - 1.0$			V	HMCS408C/AC; - $I_{OH} = 1.0$ mA	
			$V_{CC} - 0.5$			V	HMCS408C/AC; - $I_{OH} = 0.5$ mA HMCS408CL; - $I_{OH} = 0.3$ mA	
Output Low Voltage	V_{OL}	$\overline{\text{SCK}}$, SO			0.4	V	HMCS408C/AC; $I_{OL} = 1.6$ mA HMCS408CL; $I_{OL} = 0.4$ mA	
Input/Output Leakage Current	$ I_{IL} $	RESET, $\overline{\text{SCK}}$ R3 ₂ /INT ₀ , R3 ₃ /INT ₁ , SI, SO, OSC ₁			1	μA	$V_{in} = 0$ V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			2.3	mA	HMCS408C; $V_{CC} = 5$ V; 2,5 $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	
					1.1	mA	HMCS408CL; $V_{CC} = 3$ V; 2,5 $f_{osc} = 4$ MHz, $\div 16$, or $f_{osc} = 2$ MHz, $\div 8$	
					4.5	mA	HMCS408AC; $V_{CC} = 5$ V; 2,5 $f_{osc} = 4$ MHz, $\div 4$	



HMCS408C/HMCS408CL/HMCS408AC

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Current Dissipation in Standby Mode	I _{SBY}	V _{CC}			1.2	mA	HMCS408C; V _{CC} = 5 V; f _{osc} = 4 MHz, ÷ 8, or f _{osc} = 2 MHz, ÷ 4	3,5
					0.5	mA	HMCS408CL; V _{CC} = 3 V; f _{osc} = 4 MHz, ÷ 16, or f _{osc} = 2 MHz, ÷ 8	3,5
					1.7	mA	HMCS408AC; V _{CC} = 5 V; f _{osc} = 4 MHz, ÷ 4	3,5
Current Dissipation in Stop Mode	I _{stop}	V _{CC}			10	μA	HMCS408C/AC; V _{in} (TEST) = V _{CC} - 0.3 V to 0 V to 0.3 V HMCS408CL; V _{in} (TEST) = V _{CC} - 0.2 V to 0 V to 0.2 V	4
Stop Mode Retain Voltage	V _{stop}	V _{CC}	2			V		

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R3-R9: V_{CC}
 - D₄-D₁₅, R0-R2, RA₀, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R3-R9: V_{CC}
 - D₄-D₁₅, R0-R2, RA₀, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When f_{osc} = x MHz, estimate the current dissipation as follows:
 HMCS408C/AC; Max value @ x MHz = x/4 × (max value @ 4 MHz)
 HMCS408CL; Max value @ x MHz = x/2 × (max value @ 2 MHz)

HMCS408C/HMCS408CL/HMCS408AC

Input/Output Characteristics for Standard Pin

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,

HMCS408C: $V_{CC} = 3.5$ V to 6 V,

HMCS408CL: $V_{CC} = 2.5$ V to 6 V,

HMCS408AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R3-R5, R9	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R3-R5, R9	- 0.3		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₀ -D ₃ , R3-R8	$V_{CC} - 1.0$			V	HMCS408C/AC; - $I_{OH} = 1.0$ mA	1
		D ₀ -D ₃ , R3-R8	$V_{CC} - 0.5$			V	HMCS408C/AC; - $I_{OH} = 0.5$ mA HMCS408CL; - $I_{OH} = 0.3$ mA	1
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R3-R8		0.4		V	HMCS408C/AC; $I_{OL} = 1.6$ mA HMCS408CL; $I_{OH} = 0.4$ mA	
Input/Output Leakage Current	$ I_{II} $	D ₀ -D ₃ , R3-R9			1	μA	$V_{in} = 0$ V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D ₀ -D ₃ , R3-R9	30	60	150	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	3
		D ₀ -D ₃ , R3-R9	3	15	50	μA	HMCS408CL only; $V_{CC} = 3$ V, $V_{in} = 0$ V	3

- Notes: 1. Applied to I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins with pull-up MOS selected by mask option.



Input/Output Characteristics for High Voltage Pin

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
 HMCS408C: $V_{CC} = 3.5$ V to 6 V,
 HMCS408CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS408AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D4-D15, R1, R2, RA0, RA1	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D4-D15, R1, R2, RA0, RA1	$V_{CC} - 40$		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D4-D15	$V_{CC} - 3.0$			V	$- I_{OH} = 15$ mA, $V_{CC} = 5$ V \pm 20%	
			$V_{CC} - 2.0$			V	$- I_{OH} = 10$ mA, $V_{CC} = 5$ V \pm 20%	
			$V_{CC} - 1.0$			V	HMCS408C/AC; $- I_{OH} = 4$ mA HMCS408CL; $- I_{OH} = 2.5$ mA	
		R0-R2	$V_{CC} - 3.0$			V	$- I_{OH} = 3$ mA, $V_{CC} = 5$ V \pm 20%	
			$V_{CC} - 2.0$			V	$- I_{OH} = 2$ mA, $V_{CC} = 5$ V \pm 20%	
			$V_{CC} - 1.0$			V	HMCS408C/AC; $- I_{OH} = 0.8$ mA HMCS408CL; $- I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	D4-D15, R0-R2			$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40$ V	1
		D4-D15, R0-R2			$V_{CC} - 37$	V	150k Ω to $V_{CC} - 40$ V	2
Input/Output Leakage Current	$ I_{IL} $	D4-D15, R0-R2, RA0, RA1			20	μA	$V_{in} = V_{CC} - 40$ V to V_{CC}	3
Pull-Down MOS Current	I_d	D4-D15, R0-R2, RA0, RA1	125	250	600	μA	$V_{disp} = V_{CC} - 35$ V, $V_{in} = V_{CC}$	4

- Notes: 1. Applied to I/O pins with pull-down MOS selected by mask option.
 2. Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. Applied to I/O pins with pull-down MOS selected by mask option.

HMCS408C/HMCS408CL/HMCS408AC

AC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40 \text{ V}$ to V_{CC} , $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$,

HMCS408C: $V_{CC} = 3.5 \text{ V}$ to 6 V ,

HMCS408CL: $V_{CC} = 2.5 \text{ V}$ to 6 V ,

HMCS408AC: $V_{CC} = 4.5 \text{ V}$ to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	HMCS408C; divide by 8	
			0.2	2	2.25	MHz	HMCS408C; divide by 4	
			0.8	4	4.5	MHz	HMCS408CL; divide by 16	
			0.4	2	2.25	MHz	HMCS408CL; divide by 8	
			0.4	4	4.5	MHz	HMCS408AC; divide by 4	
			0.4	8	9	MHz	HMCS408AC; divide by 8	
Instruction Cycle Time	t_{cyc}		1.78	2	20	μs	HMCS408C	
			3.55	4	20	μs	HMCS408CL	
			0.89	1	20	μs	HMCS408AC	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms	HMCS408C/AC	1
					60	ms	HMCS408CL	1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	HMCS408C; divide by 8 HMCS408CL; divide by 16 HMCS408AC; divide by 4	2
			203			ns	HMCS408C; divide by 4 HMCS408CL; divide by 8	2
			41			ns	HMCS408AC; divide by 8	

(continued)

AC Characteristics (Cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			20	ns		2
\overline{INT}_0 High Level Width	t_{0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms	HMCS408C/AC	4
					15	ms	HMCS408CL	4

- Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (HMCS408C:3.5 V, HMCS408CL; 2.5V, HMCS408AC; 4.5 V) after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.
2. See figure 25.
 3. See figure 26.
 4. See figure 27.

HMCS408C/HMCS408CL/HMCS408AC

Serial Interface Timing Characteristics

AT Transfer Clock Output

(GND = 0 V, $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$,
 HMCS408C: $V_{CC} = 3.5 \text{ V to } 6 \text{ V}$,
 HMCS408CL: $V_{CC} = 2.5 \text{ V to } 6 \text{ V}$,
 HMCS408AC: $V_{CC} = 4.5 \text{ V to } 6 \text{ V}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{scyc}	$\overline{\text{SCK}}$	1			t_{cyc}		1.2
Transfer Clock High, Low Level Width	t_{sckH} t_{sckL}	$\overline{\text{SCK}}$	0.5			t_{scyc}		1.2
Transfer Clock Rise, Fall Time	t_{sckr} t_{sckf}	$\overline{\text{SCK}}$			100	ns	HMCS408C/AC	1.2
					300	ns	HMCS408CL	1.2
Serial Output Data Delay time	t_{dso}	SO			300	ns	HMCS408C	1.2
					600	ns	HMCS408CL	1.2
					250	ns	HMCS408AC	1.2
Serial Input Data Set-up Time	t_{ssi}	SI	500			ns	HMCS408C	1
			1000			ns	HMCS408CL	1
			300			ns	HMCS408AC	1
Serial Input Data Hold Time	t_{hsi}	SI	150			ns	HMCS408C/AC	1
			500			ns	HMCS408CL	1



AT Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK}	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	\overline{SCK}	0.5			t_{scyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	\overline{SCK}			100	ns	HMCS408C/AC	1
					300	ns	HMCS408CL	1
Serial Output Data Delay Time	t_{DSO}	SO			300	ns	HMCS408C	1.2
					600	ns	HMCS408CL	1.2
					250	ns	HMCS408AC	1.2
Serial Input Data Set-up Time	t_{SSI}	SI	500			ns	HMCS408C	1
			1000			ns	HMCS408CL	1
			300			ns	HMCS408AC	1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns	HMCS408C/AC	1
			500			ns	HMCS408CL	1

Notes: 1. See figure 28.
2. See figure 29.

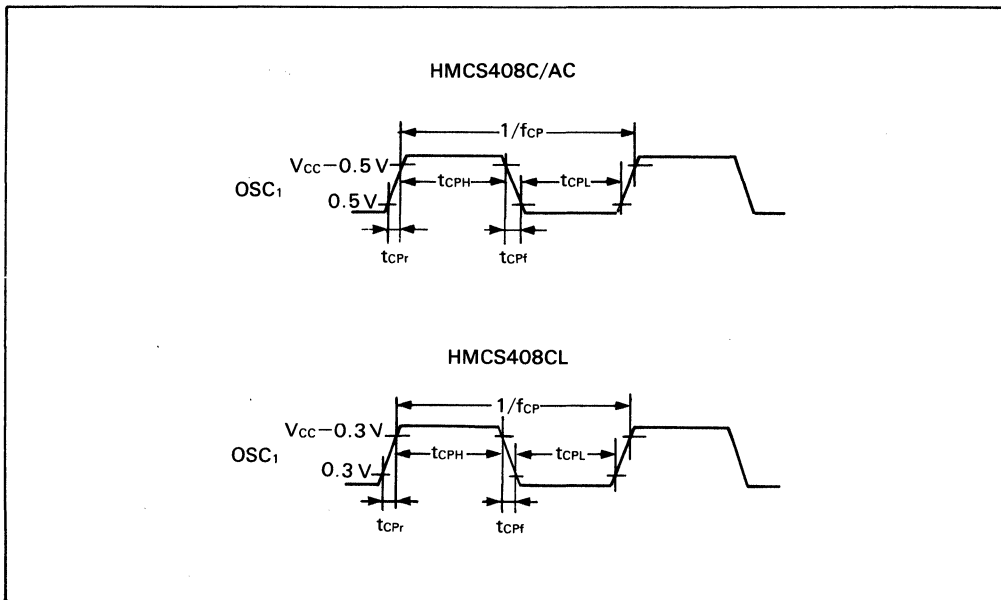


Figure 25. Oscillator Timing

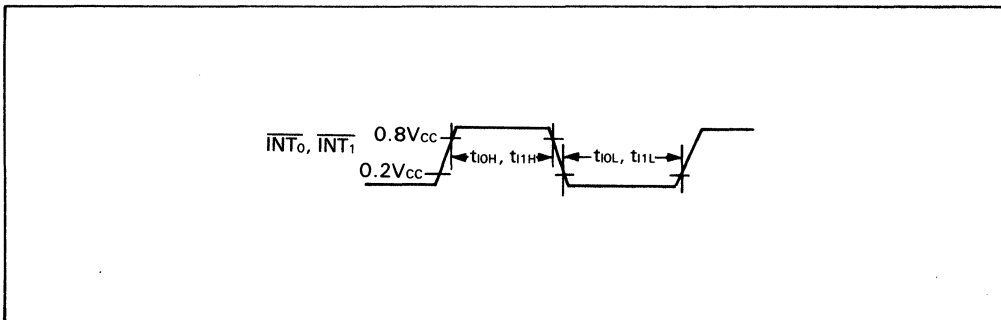


Figure 26. Interrupt Timing

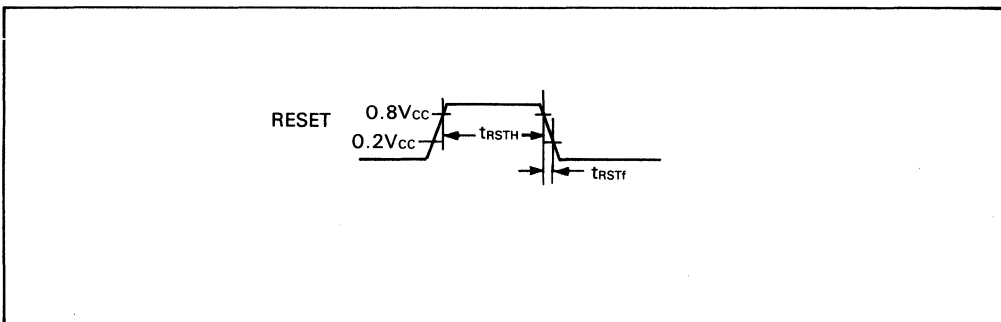


Figure 27. Reset Timing

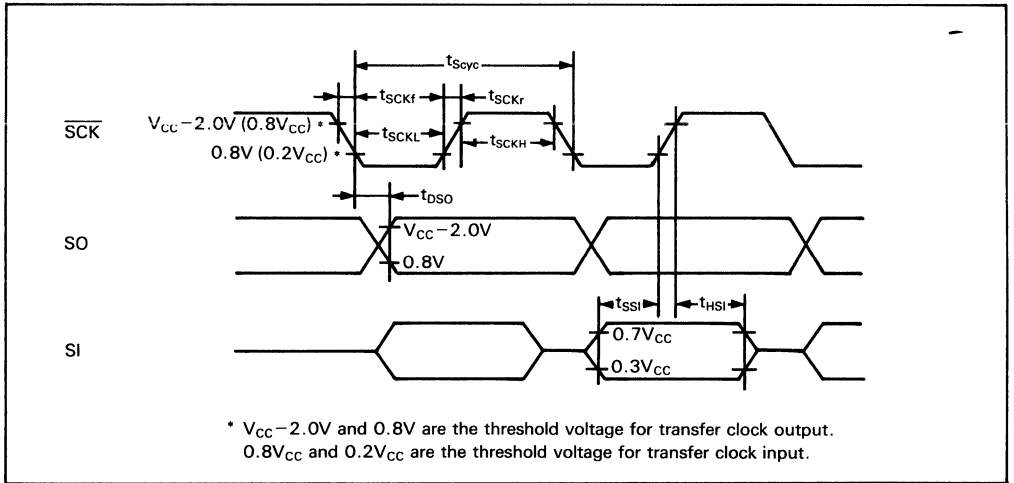


Figure 28. Timing Diagram of Serial Interface

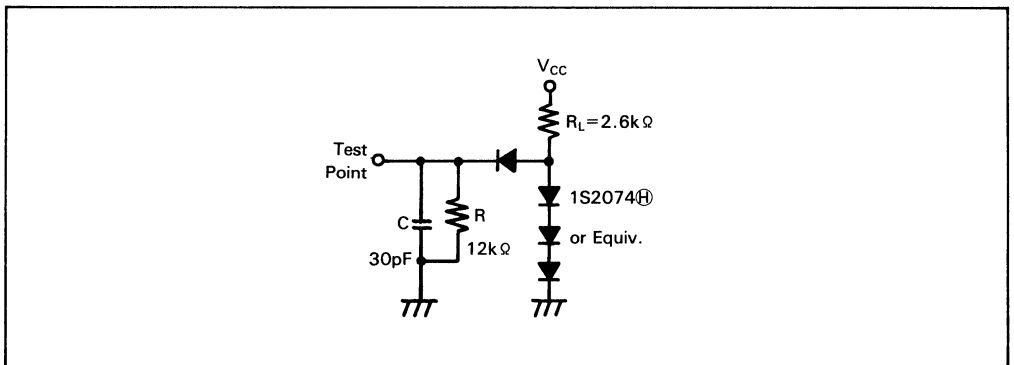


Figure 29. Timing Load Circuit

HMCS408C/HMCS408CL/HMCS408AC

HMCS408C/AC/CL
MASK OPTION LIST

5V Operation	: <input type="checkbox"/> HMCS408C
3V Operation	: <input type="checkbox"/> HMCS408CL
High Speed Operation	: <input type="checkbox"/> HMCS408AC

* Please enter check marks in
(■, x, ✓).

(1) I/O Option

Please enter 0 in applicable item for I/O option selection.
 A; Without Pull-up MOS (NMOS Open Drain) B; With Pull-up MOS
 C; CMOS (not be used as Input) D; Without Pull-down MOS (PMOS Open Drain) E; With Pull-down MOS

Note (I/O options masked by ■ are not available.)

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

Pin	Input/Output	I/O Option					Pin	Input/Output	I/O Option										
		A	B	C	D	E			A	B	C	D	E						
D ₀	Standard Pins Input/Output				■	■	R3 ₀	Standard Pins Input/Output				■	■						
D ₁					■	■	R3 ₁		Standard Pins Input/Output				■	■					
D ₂					■	■	R3 ₂			Standard Pins Input/Output				■	■				
D ₃					■	■	R3 ₃				Standard Pins Input/Output				■	■			
D ₄	High Voltage Pins Input/Output		■	■			R4 ₀	High Voltage Pins Input/Output							■	■			
D ₅			■	■			R4 ₁		High Voltage Pins Input/Output						■	■			
D ₆			■	■			R4 ₂			High Voltage Pins Input/Output					■	■			
D ₇			■	■			R4 ₃				High Voltage Pins Input/Output				■	■			
D ₈			■	■			R5 ₀					High Voltage Pins Input/Output				■	■		
D ₉			■	■			R5 ₁						High Voltage Pins Input/Output				■	■	
D ₁₀			■	■			R5 ₂							High Voltage Pins Input/Output				■	■
D ₁₁			■	■			R5 ₃								High Voltage Pins Input/Output				■
D ₁₂		■	■			R6 ₀	High Voltage Pins Output											■	■
D ₁₃		■	■			R6 ₁		High Voltage Pins Output										■	■
D ₁₄		■	■			R6 ₂			High Voltage Pins Output									■	■
D ₁₅		■	■			R6 ₃				High Voltage Pins Output								■	■
						R7 ₀					High Voltage Pins Output							■	■
						R7 ₁						High Voltage Pins Output						■	■
						R7 ₂							High Voltage Pins Output					■	■
						R7 ₃								High Voltage Pins Output				■	■
						R8 ₀	High Voltage Pins Output											■	■
						R8 ₁		High Voltage Pins Output										■	■
						R8 ₂			High Voltage Pins Output									■	■
						R8 ₃				High Voltage Pins Output								■	■
						R9 ₀					High Voltage Pins Input							■	■
						R9 ₁						High Voltage Pins Input						■	■
						R9 ₂							High Voltage Pins Input					■	■
						R9 ₃								High Voltage Pins Input				■	■
						RA ₀	High Voltage Pins Input											■	■
						RA ₁		High Voltage Pins Input										■	■

Please Mark as RA₁ / V_{dis}



(2) RA₁/V_{disp}

RA ₁ /V _{disp}
<input type="checkbox"/> RA ₁ : Without Pull-down MOS (D)
<input type="checkbox"/> V _{disp}

* Please enter check marks (■, X, ✓) in applicable item.

(3) Package

Package
<input type="checkbox"/> DP-64S (shrink package)
<input type="checkbox"/> FP-64
<input type="checkbox"/> FP-64A

* Please enter check marks (■, X, ✓) in applicable item.

Note) RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high pins are option D.

(4) Divider (DIV)

Products divider	HMCS408C	HMCS408CL	HMCS408AC
16		<input type="checkbox"/>	
8	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4	<input type="checkbox"/>		<input type="checkbox"/>

(5) ROM Code Media

ROM Code Media
<input type="checkbox"/> EPROM: Emulator Type
<input type="checkbox"/> EPROM: EPROM On-Package Microcomputer Type

Check List of Application

(A) Oscillator (CPG option)

CPG option	<input type="checkbox"/> HMCS408C (5V Operation)	<input type="checkbox"/> HMCS408CL (3V Operation)	<input type="checkbox"/> HMCS408AC (High Speed Operation)
	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock

* Please enter check marks (■, X, ✓) in applicable item.

HD4074008

Description

The HD4074008 is a ZTAT microcomputer incorporating 8 kwords of programmable ROM and 512 digits of RAM. It is a CMOS 4-bit single-chip HMCS400-series microcomputer providing the high programming productivity, high-speed operation, and low power dissipation.

Ordering Information

Part No.	Clock Freq. (MHz)	Package
HD4074008S	8	DP-64S
HD4074008C		DC-64S
HD4074008F		FP-64
HD4074008H		FP-64A

Features

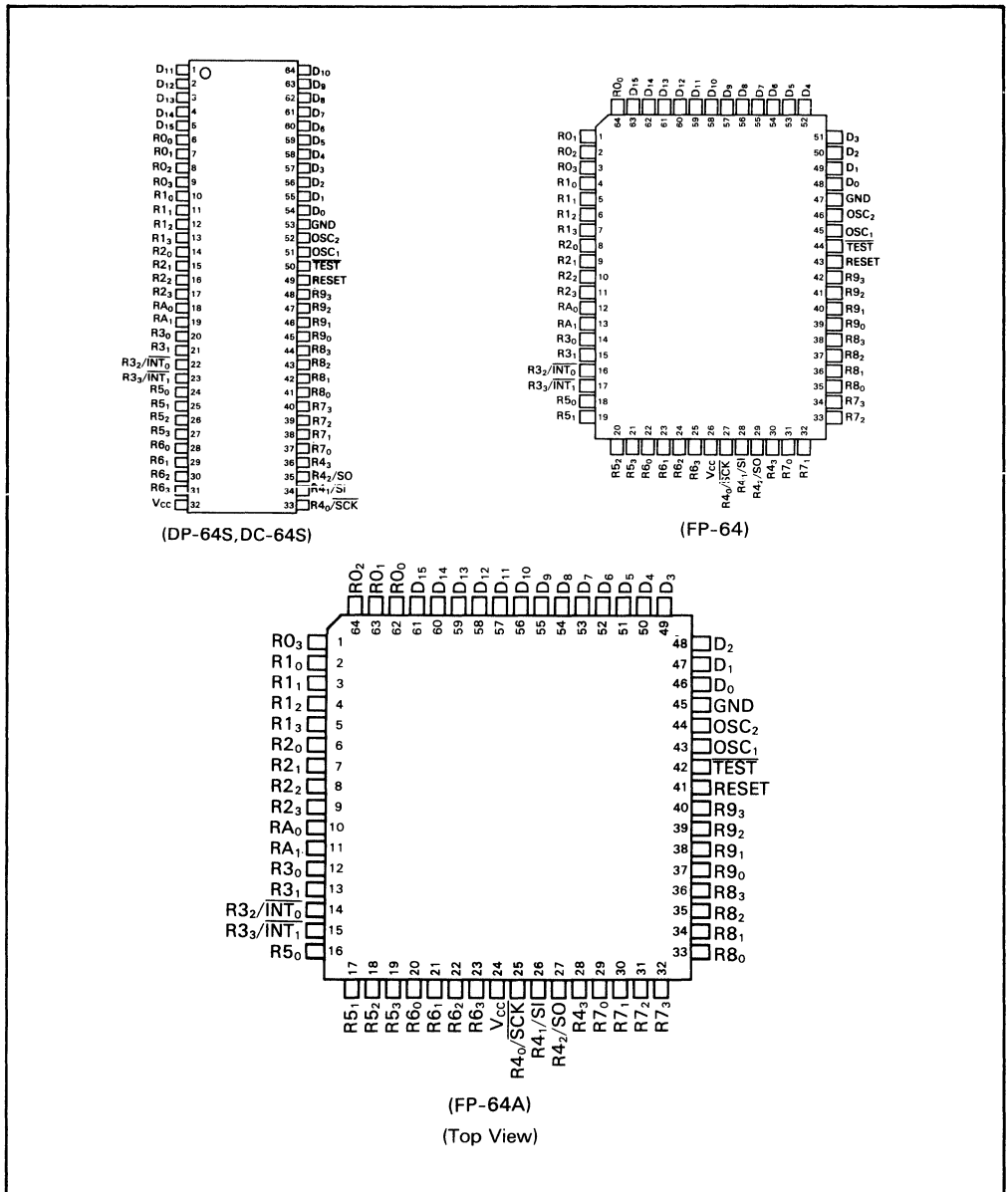
- 8,192 words × 10 bits programmable ROM (Programming spec is compatible with the 27256 type)
- 512 digits × 4 bits RAM
- 58 I/O lines including 12 high current pins (15-mA), I/O pin circuit type; open drain
- Two on-chip timer/counters
- Clock synchronous 8-bit serial interface
- Five interrupt sources
 - External 2
 - Internal 3
- Subroutine stack: Up to 16 levels including interrupts
- Two low power dissipation mode
 - Standby mode
 - Stop mode
- On-chip oscillator: Crystal or ceramic filter (Externally drivable)
- Minimum instruction cycle time 0.89 μ s
- Operation modes
 - MCU mode
 - PROM mode
- Package
 - 64-pin shrink type plastic DIP
 - 64-pin shrink type ceramic DIP with window
 - 64-pin flat plastic package

Program Development Support Tools

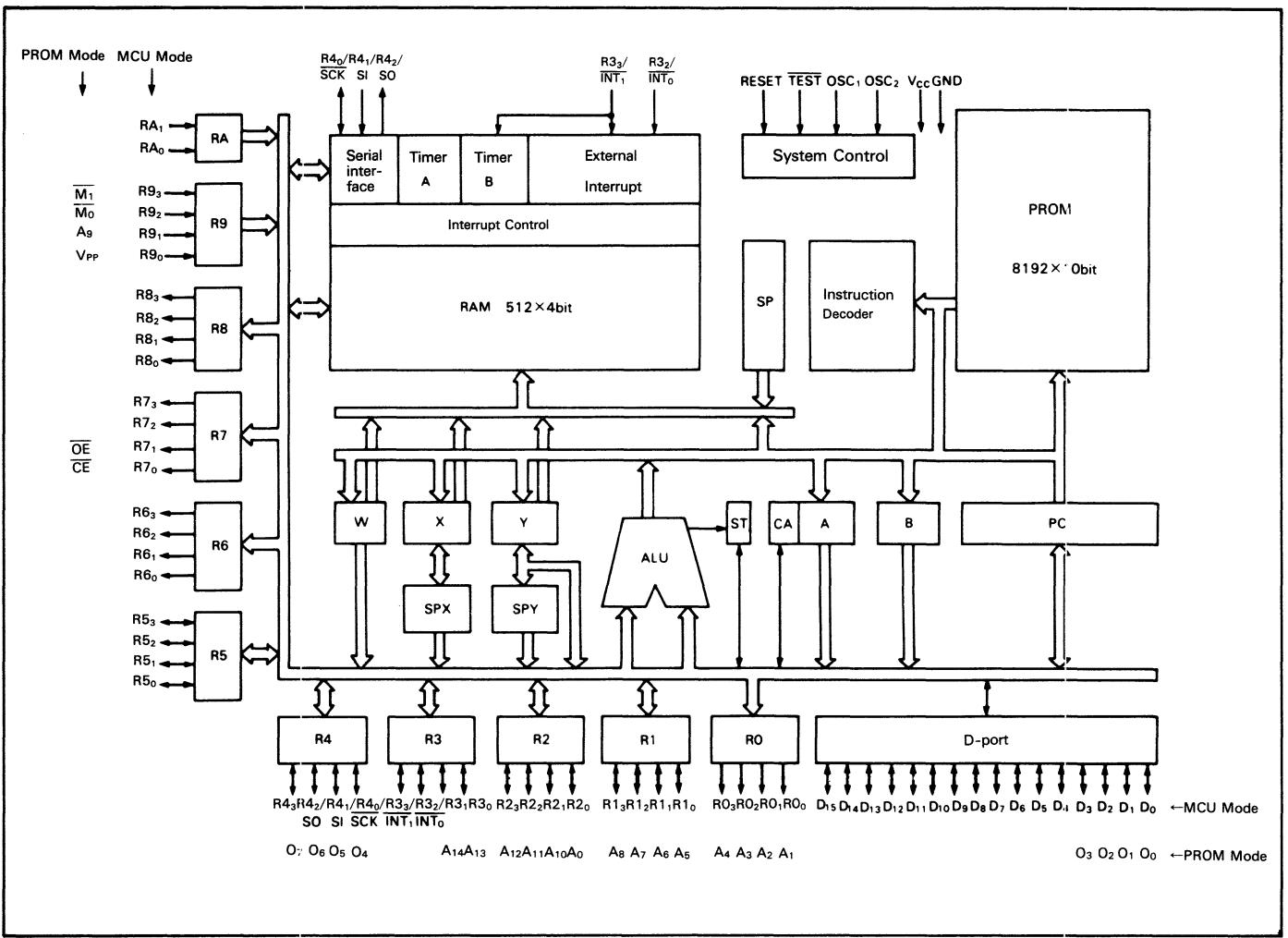
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device



Pin Arrangement



Block Diagram



Pin Description

Pin No.			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64	FP-64A	Symbol	I/O	Symbol	I/O
1	59	57	D ₁₁	I/O	V _{CC}	
2	60	58	D ₁₂	I/O		
3	61	59	D ₁₃	I/O		
4	62	60	D ₁₄	I/O		
5	63	61	D ₁₅	I/O		
6	64	62	RO ₀	O	A ₁	I
7	1	63	RO ₁	O	A ₂	I
8	2	64	RO ₂	O	A ₃	I
9	3	1	RO ₃	O	A ₄	I
10	4	2	R1 ₀	I/O	A ₅	I
11	5	3	R1 ₁	I/O	A ₆	I
12	6	4	R1 ₂	I/O	A ₇	I
13	7	5	R1 ₃	I/O	A ₈	I
14	8	6	R2 ₀	I/O	A ₀	I
15	9	7	R2 ₁	I/O	A ₁₀	I
16	10	8	R2 ₂	I/O	A ₁₁	I
17	11	9	R2 ₃	I/O	A ₁₂	I
18	12	10	RA ₀	I		
19	13	11	RA ₁	I		
20	14	12	R3 ₀	I/O	A ₁₃	I
21	15	13	R3 ₁	I/O	A ₁₄	I
22	16	14	R3 ₂ /INT ₀	I/O		
23	17	15	R3 ₃ /INT ₁	I/O		
24	18	16	R5 ₀	I/O		
25	19	17	R5 ₁	I/O		
26	20	18	R5 ₂	I/O		
27	21	19	R5 ₃	I/O		
28	22	20	R6 ₀	O		
29	23	21	R6 ₁	O		
30	24	22	R6 ₂	O		
31	25	23	R6 ₃	O		
32	26	24	V _{CC}		V _{CC}	

Pin No.			MCU Mode		PROM Mode	
DC-64S, DP-64S	FP-64	FP-64A	Symbol	I/O	Symbol	I/O
33	27	25	R4 ₀ /SCK	I/O	O ₄	I/O
34	28	26	R4 ₁ /SI	I/O	O ₅	I/O
35	29	27	R4 ₂ /SO	I/O	O ₆	I/O
36	30	28	R4 ₃	I/O	O ₇	I/O
37	31	29	R7 ₀	O	CE	I
38	32	30	R7 ₁	O	OE	I
39	33	31	R7 ₂	O		
40	34	32	R7 ₃	O		
41	35	33	R8 ₀	O		
42	36	34	R8 ₁	O		
43	37	35	R8 ₂	O		
44	38	36	R8 ₃	O		
45	39	37	R9 ₀	I	V _{PP}	
46	40	38	R9 ₁	I	A ₉	I
47	41	39	R9 ₂	I	M ₀	I
48	42	40	R9 ₃	I	M ₁	I
49	43	41	RESET	I	RESET	I
50	44	42	TEST	I	TEST	I
51	45	43	OSC ₁	I		
52	46	44	OSC ₂	O		
53	47	45	GND		GND	
54	48	46	D ₀	I/O	O ₀	I/O
55	49	47	D ₁	I/O	O ₁	I/O
56	50	48	D ₂	I/O	O ₂	I/O
57	51	49	D ₃	I/O	O ₃	I/O
58	52	50	D ₄	I/O		
59	53	51	D ₅	I/O		
60	54	52	D ₆	I/O		
61	55	53	D ₇	I/O		
62	56	54	D ₈	I/O		
63	57	55	D ₉	I/O		
64	58	56	D ₁₀	I/O	V _{CC}	

(Note) I/O : Input/Output Pins
 I : Input Pins
 O : Output Pins

Pin Function

GND, V_{CC} (Power)

GND and V_{CC} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are the connected pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits.

D₀-D₁₅ (D Port)

The D port is an input/output port addressed by one bit. These 16 pins are all input D₀ to D₃ are standard and D₄ to D₁₅ are large current standard pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R0-RA (R Port)

R0-R9 are 4-bit I/O ports. RA is a 2-bit I/O port. R0, R6, R7, and R8 are output ports, R9 and RA are input ports, and R1 to R5 are I/O ports. All pins of port R0-RA are standard pins. The circuit type of D₄-D₁₅ and R0-R2 is PMOS open drain, and that of D₀-D₃ and R3-R8 is NMOS open drain. R3₂, R3₃ and R4₀, R4₁, R4₂ are multiplexed with INT₀, INT₁, SCK, SI, and SO respectively. The RA₁ pin should be used as RA₁ since it is PMOS open drain (MOS without pull-down). For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R3₂ and R3₃ respectively. For details, see Interrupt section.

SCK, SI, SO (Serial Interface)

The transfer clock I/O pin (SCK), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R4₀, R4₁, and R4₂ respectively. For details, see Serial Interface section.

V_{PP} (Program Voltage)

V_{PP} is the input for the program voltage (12.5 V ± 0.3 V) for programming the PROM.

CE (Chip Enable)

CE is the input for programming and verifying internal PROM.

OE (Output Enable)

OE is the input of data output control signal for verify.

A₀-A₁₄ (Address Bus)

A₀-A₁₄ are address input pins for internal PROM.

O₀-O₇ (PROM Data Bus)

These are data bus for internal PROM.

M₀, M₁ (Mode)

M₀ and M₁, set PROM mode. PROM mode is set when M₀, M₁, and TEST pins are low level and RESET pin high level.

Functional Description

ROM Memory Map

The MCU includes 8,192 words × 10 bits of PROM. It is described in the following paragraphs and the PROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for PROM data. P instructions can refer to the PROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

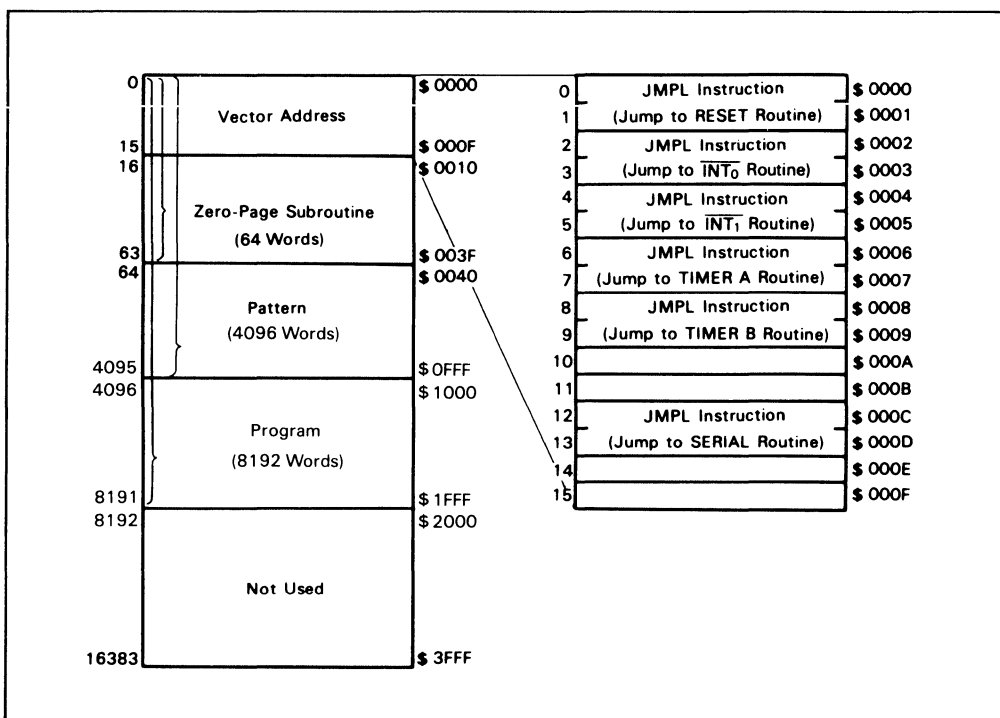


Figure 1. PROM Memory Map

RAM Memory Map

The MCU includes 512 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction.

However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

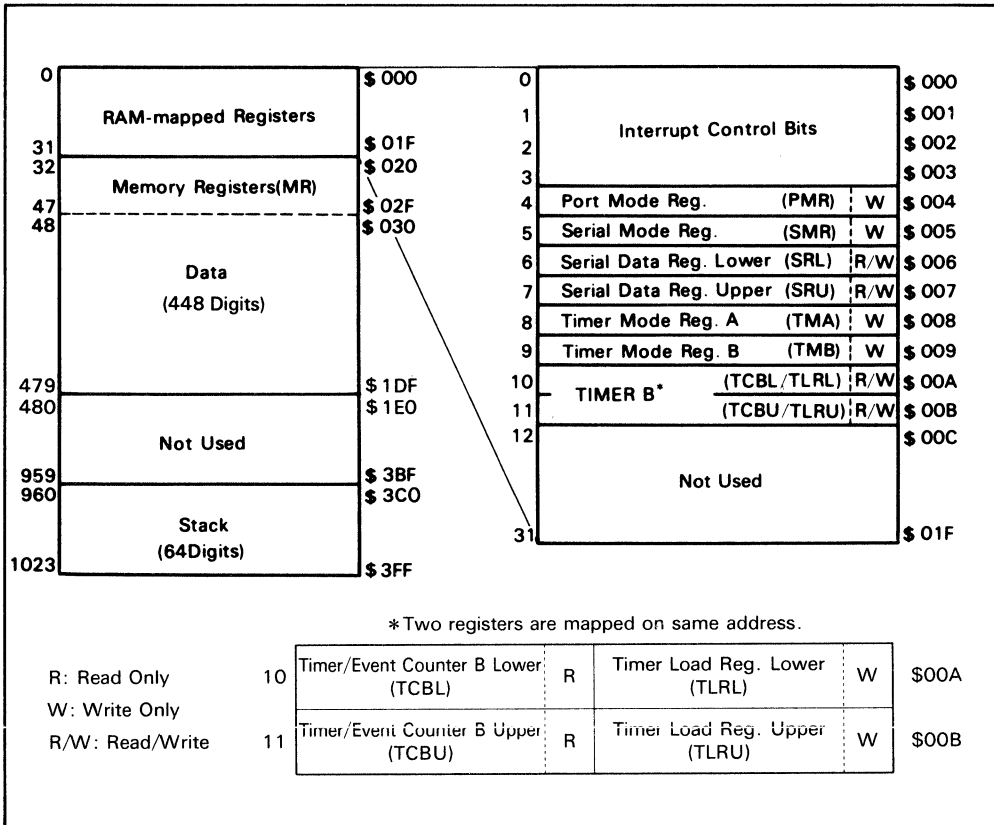


Figure 2. RAM Memory Map

Data Area (\$020 to \$1DF): 16 digits of \$020 through \$02F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when su-

broutine calls (CAL instruction, CALL instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of $\overline{INT_0}$)	IFO (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	IMTA (IM of TIMER A)	IFTA (IF of TIMER A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	\$001
2	Not Used	Not Used	IMTB (IM of TIMER B)	IFTB (IF of TIMER B)	\$002
3	Not Used	Not Used	IMS (IM of SERIAL)	IFS (IF of SERIAL)	\$003

IF: Interrupt Request Flag
 IM: Interrupt Mask
 I/E: Interrupt Enable Flag
 SP: Stack Pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
 The contents of status becomes invalid when a "Not Used" bit is tested.

Figure 3. Configuration of Interrupt Control Bit Area

Memory Registers			Stack Area		
32	MR(0)	\$020	960	Level 16	\$3C0
33	MR(1)	\$021		Level 15	
34	MR(2)	\$022		Level 14	
35	MR(3)	\$023		Level 13	
36	MR(4)	\$024		Level 12	
37	MR(5)	\$025		Level 11	
38	MR(6)	\$026		Level 10	
39	MR(7)	\$027		Level 9	
40	MR(8)	\$028		Level 8	
41	MR(9)	\$029		Level 7	
42	MR(10)	\$02A		Level 6	
43	MR(11)	\$02B		Level 5	
44	MR(12)	\$02C		Level 4	
45	MR(13)	\$02D		Level 3	
46	MR(14)	\$02E		Level 2	
47	MR(15)	\$02F	1023	Level 1	\$3FF

PC₁₃ to PC₀: Program Counter
 ST: Status
 CA: Carry

Note: As the HD4074008 is an 8 k PROM version, PC₁₃ is not used.

	bit 3	bit 2	bit 1	bit 0	
1020	ST	PC ₁₃	PC ₁₂	PC ₁₁	\$3FC
1021	PC ₁₀	PC ₉	PC ₈	PC ₇	\$3FD
1022	CA	PC ₆	PC ₅	PC ₄	\$3FE
1023	PC ₃	PC ₂	PC ₁	PC ₀	\$3FF

Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register, and the 4-bit X and Y registers indirectly address RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value for the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack. It is restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels

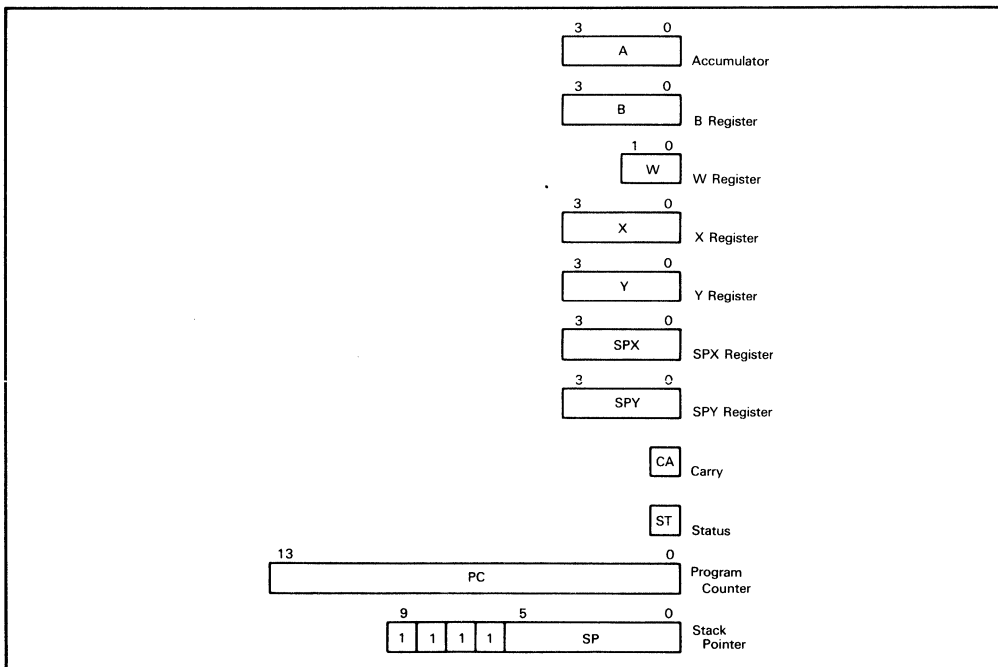


Figure 5. Registers and Flags



deep because the high four bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit, reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timer A, timer B), and serial port (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector address (IV), interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

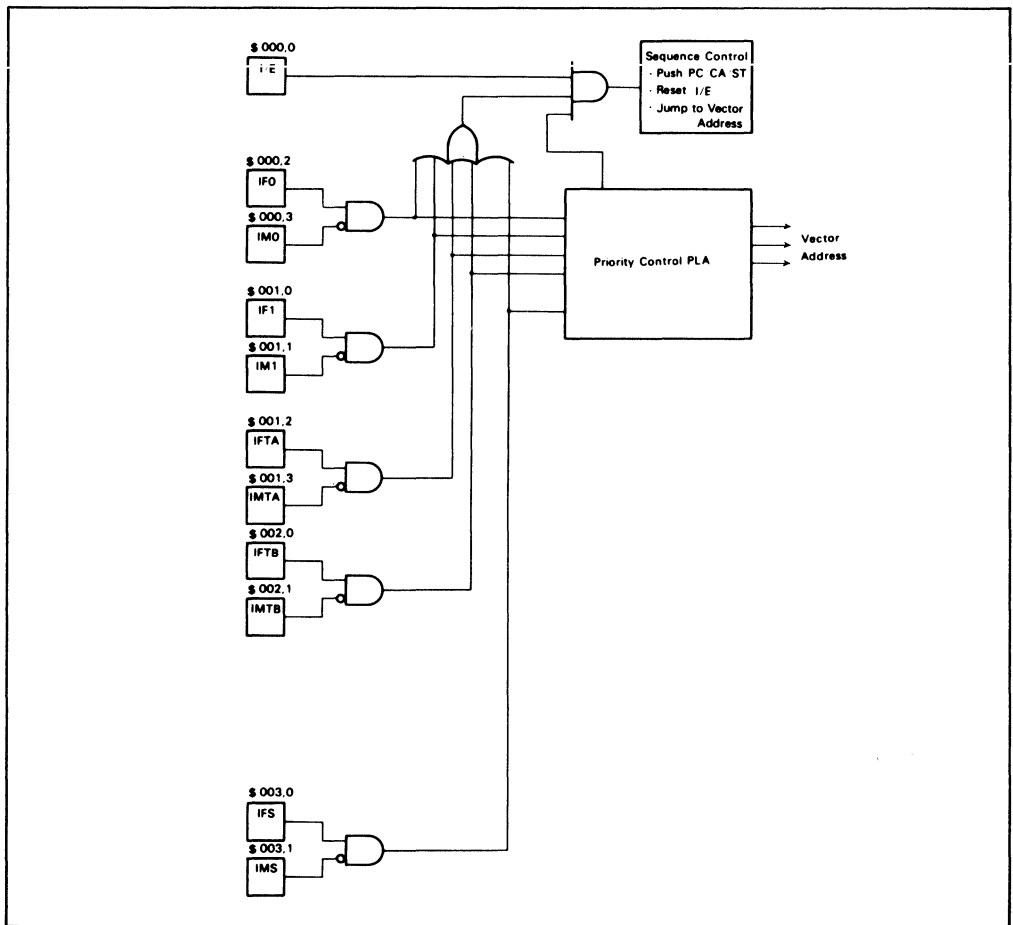


Figure 6. Interrupt Control Circuit Block Diagram



An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service

sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	TimerA	TimerB	SERIAL
I/E	1	1	1	1	1
IF0· $\overline{IM0}$	1	0	0	0	0
IF1· $\overline{IM1}$	*	1	0	0	0
IFTA· \overline{IMTA}	*	*	1	0	0
IFTB· \overline{IMTB}	*	*	*	1	0
IFS· \overline{IMS}	*	*	*	*	1

* Don't care

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)



address.

In each vector address, program JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR

causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs

Table 6. Port Mode Register

PMR3	R3 ₃ / \overline{INT}_1 Pin	PMR1	R4 ₁ /SI Pin
0	Used as R3 ₃ port input/output pin	0	Used as R4 ₁ port input/output pin
1	Used as \overline{INT}_1 input pin	1	Used as SI input pin

PMR2	R3 ₂ / \overline{INT}_0 Pin	PMR0	R4 ₂ /SO Pin
0	Used as R3 ₂ port input/output pin	0	Used as R4 ₂ port input/output pin
1	Used as \overline{INT}_0 input pin	1	Used as SO output pin

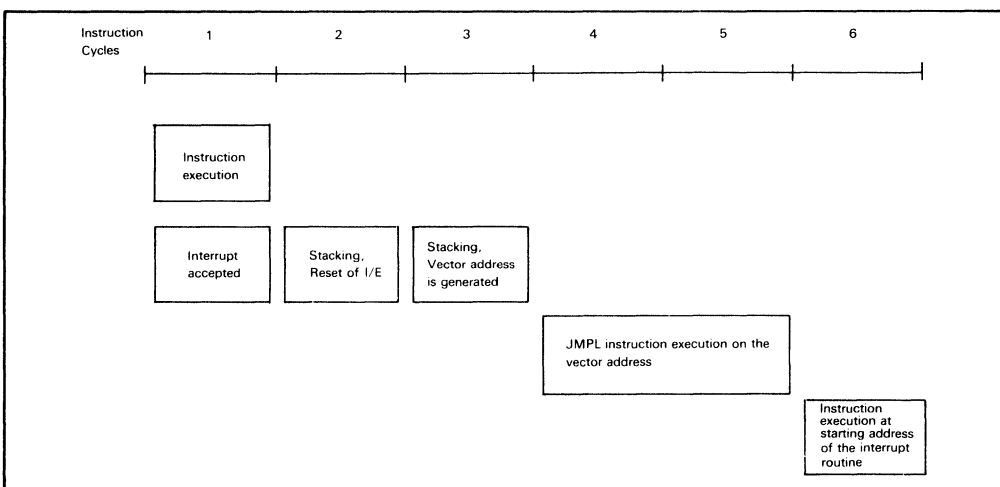


Figure 7. Interrupt Servicing Sequence



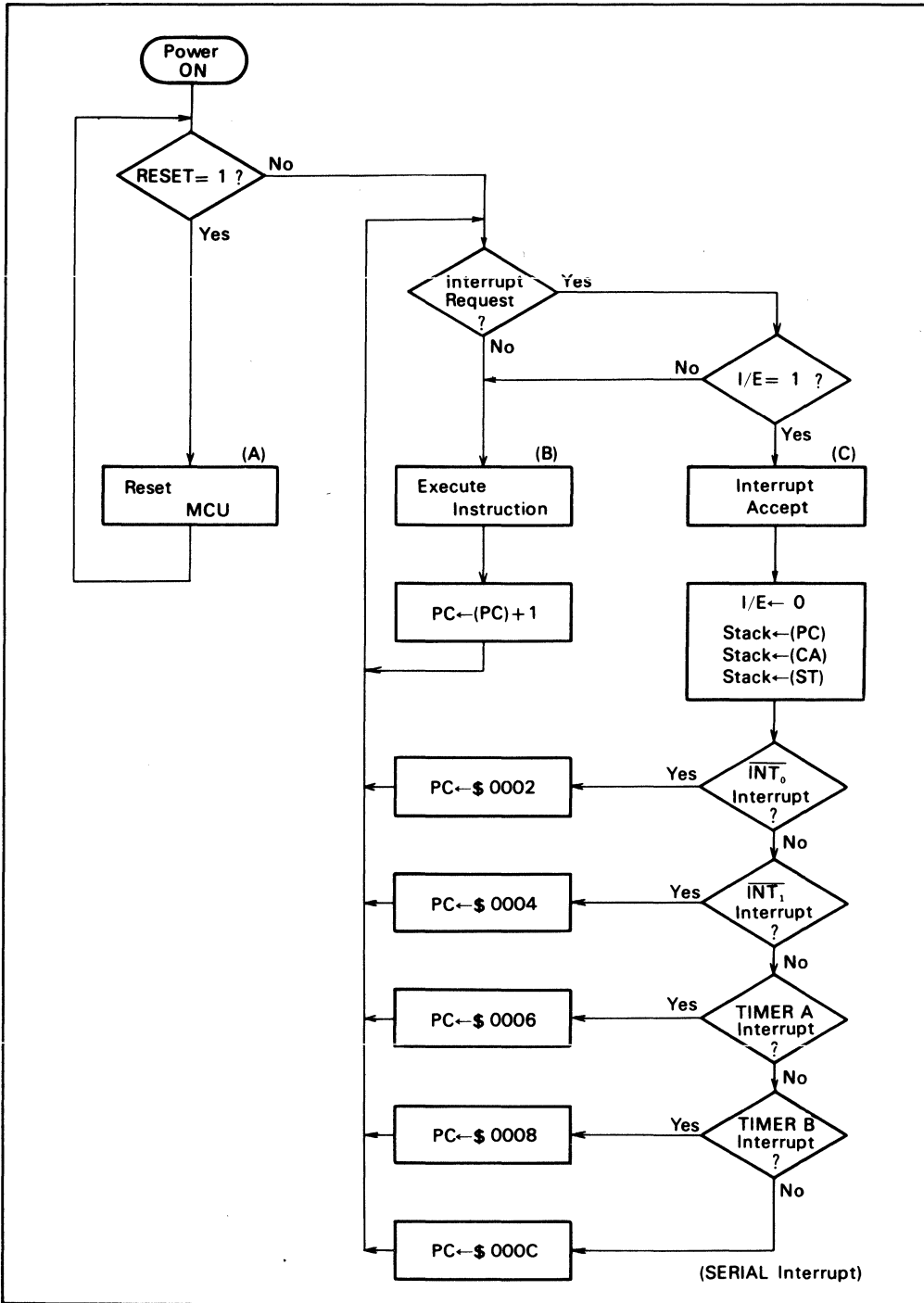


Figure 8. Interrupt Servicing Flowchart



respectively.

External Interrupt Masks (IMO: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, $R3_3/\overline{INT}_1$ pin, $R4_1/\overline{SI}$ pin, and $R4_2/\overline{SO}$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

STS instruction is used to initiate serial interface operations and to reset the octal counter to \$0. The counter starts to count at the falling edge of the transfer clock (\overline{SCK}) signal and increments by one at the rising edge of \overline{SCK} . When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$, prescaler divide ratio, and transfer clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from accepting transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes

the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after the serial mode register has been written to. Therefore, it will be necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SRL: \$006, SRU: \$007): The 8-bit read/write serial data register consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register will be output from the \overline{SO} pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the \overline{SI} pin to the serial data register, MSB first, synchronously with the rising edge of the transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Serial Interrupt Request Flag (IFS: \$003 bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: \$003 bit 1): The serial interrupt masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by a write signal to the serial mode register, when the operation mode is changed.

Table 7. Serial Mode Register

SMR3	R4 ₀ /SCK
0	Used as R4 ₀ port input/output pin
1	Used as SCK input/output pin

Transfer Clock						
SMR 2	SMR 1	SMR 0	R4 ₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	SCK Output	Prescaler	÷ 2048	÷ 4096
0	0	1	SCK Output	Prescaler	÷ 512	÷ 1024
0	1	0	SCK Output	Prescaler	÷ 128	÷ 256
0	1	1	SCK Output	Prescaler	÷ 32	÷ 64
1	0	0	SCK Output	Prescaler	÷ 8	÷ 16
1	0	1	SCK Output	Prescaler	÷ 2	÷ 4
1	1	0	SCK Output	System Clock	—	÷ 1
1	1	1	SCK Input	External Clock	—	—

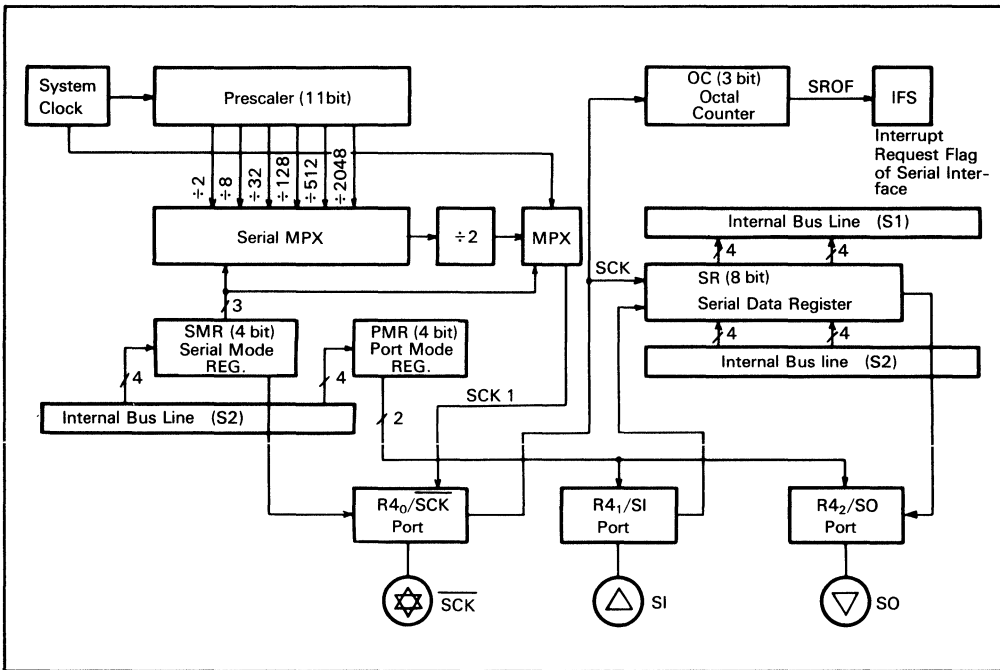


Figure 9. Serial Interface Block Diagram

Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK waiting state.

In this state the falling edge of the first trans-

fer clock causes the serial interface shift to transfer state. While the octal counter counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.

The octal counter becomes 000 again after 8 transfer clocks or by execution of an STS instruction, so that serial interface returns to SCK waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output triggered by the execution of an STS instruction, and it stops after 8 clocks.

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR2	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

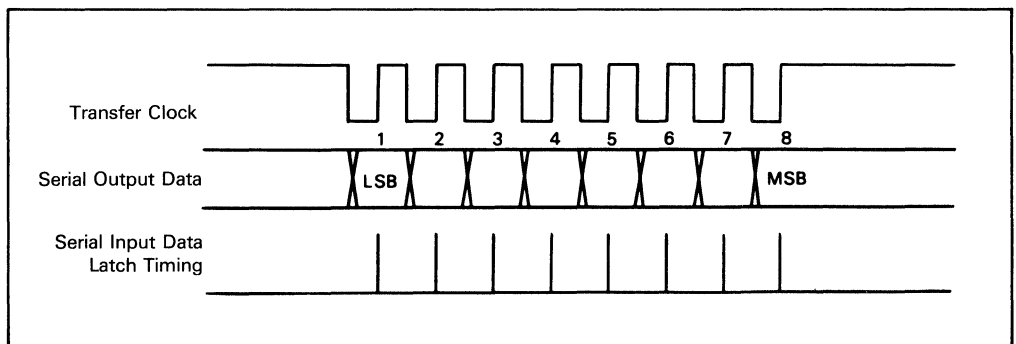


Figure 10. Serial Interface I/O Timing Chart

Example of Transfer Clock Errors

Detection: The serial interface functions abnormally when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 12.

SCK waiting state, the state of the serial interface shifts as follows: first, transfer state, second, SCK waiting state and third, transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial IRF to be set again.

If more than 8 transfer clocks occur in the

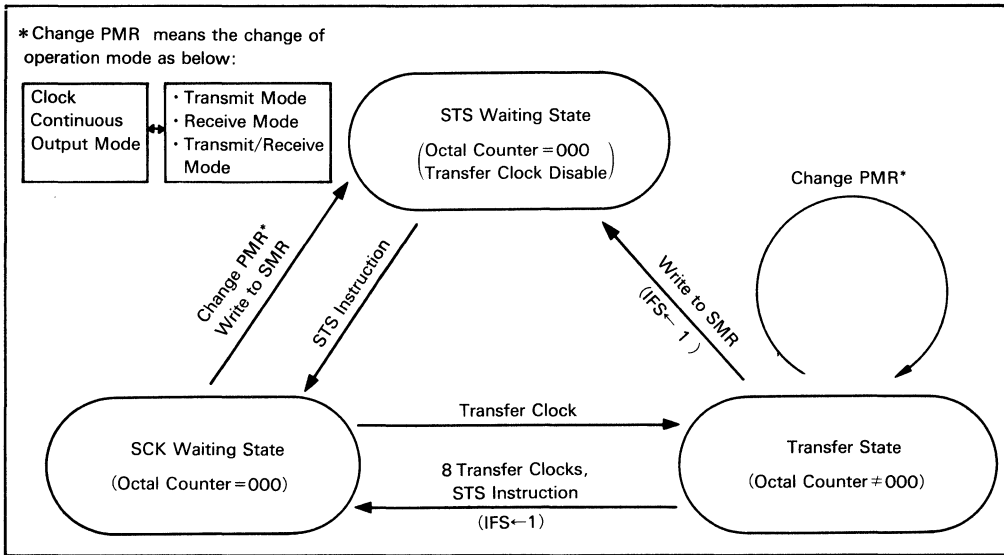


Figure 11. Serial Interface Operation State

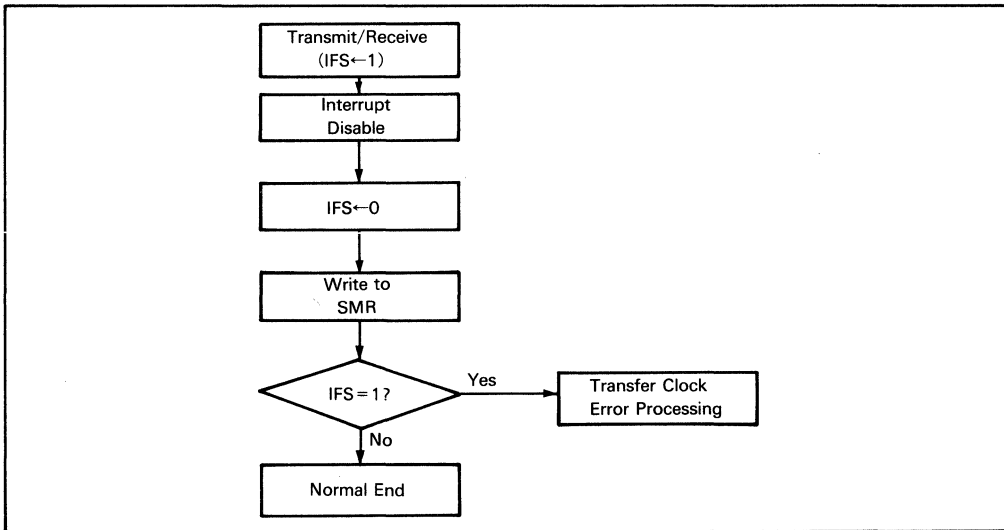


Figure 12. Example of Transfer Clock Error Detection



Timer

The MCU contains a prescaler and two timer/counters: (timer A, timer B). A block diagram is shown in figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter, and timer B an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to \$0000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by the timer mode register A (TMA), timer mode register B (TMB), serial mode register (SMR).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A becomes \$FF, it will generate an overflow and become \$00. This overflow causes the timer A interrupt request flag (IFTA: \$001 bit 2) to go to 1. This

timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio of timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB:

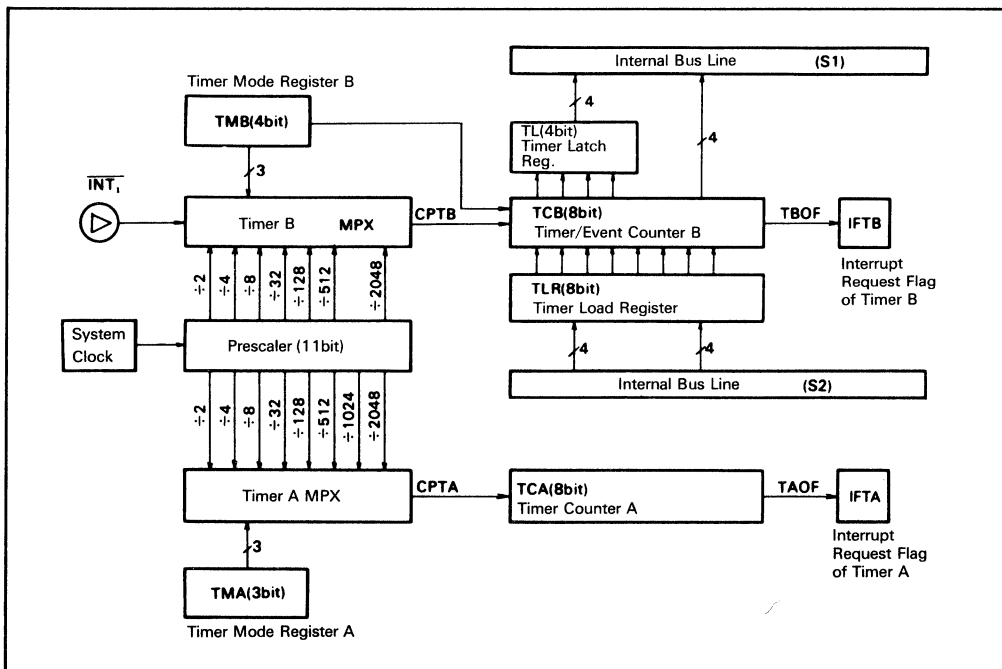


Figure 13. Timer/counter Block Diagram



\$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: \$008): The timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input, as shown in table 11. The timer mode register A is initialized to \$0 by MCU reset.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selection the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of

TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then

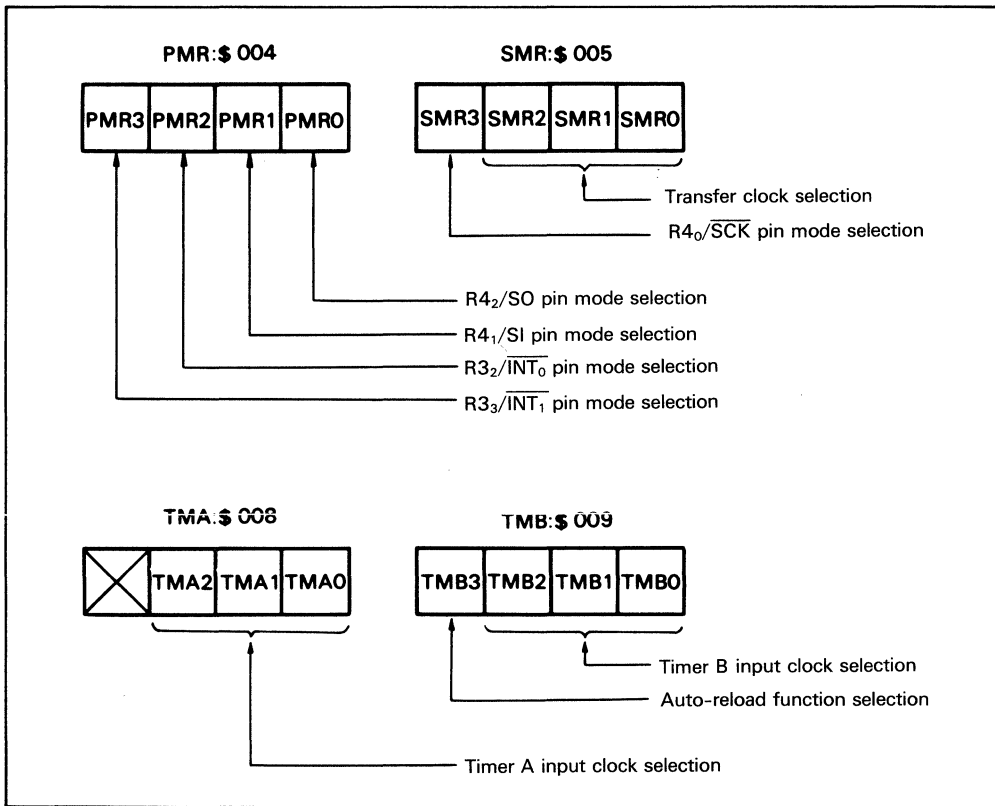


Figure 14. Mode Register Configuration and Function



the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA : \$001 bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 13).

Timer A Interrupt Mask (IMTA : \$001 bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{\text{INT}}_1$ (External Event Input)

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 16).

Input/Output

The MCU has 58 I/O pins including 12 high current standard pins (15 mA). If I/O pin is used as input pin, output data should be in the state shown in table 18.

D Port: The D port is an I/O port which has 16 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 17 for I/O pin circuit types.

R Ports: The eleven R ports in the HD4074008 are composed of 20 I/O pins, 16 output-only pins, and 6 input-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions.

The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read by reading from the output-only and/or non-existing ports.

The R₃₂, R₃₃, R₄₀, R₄₁ and R₄₂ pins are multiplexed with the \overline{INT}_0 , \overline{INT}_1 , SCK, SI and SO pins respectively. See table 17 for I/O pin circuit types.

How to Deal with Unused I/O Pins: If the I/O pins not used in the user system are in floating state, the LSI may malfunction because of noise. Electric potential of the I/O pins should be fixed as follows to prevent the malfunction.

For PMOS open drain output pins, connect the pin to the V_{CC} on the printed circuit of the user system.

For NMOS open drain output pins, connect the pin to GND on the printed circuit of the user system. Input pins should be connected

Table 17. I/O Pin Circuit Types

		MOS Without Pull-Up (NMOS Open Drain)	Pins	MOS Without Pull-Up (NMOS Open Drain)	Pins
Standard Pins (I)	I/O Pins		D ₀ -D ₃ R ₃₀ -R ₃₃ R ₄₀ -R ₄₃ R ₅₀ -R ₅₃		\overline{SCK} (Note 2) Output mode
	Output Pins		R ₆₀ -R ₆₃ R ₇₀ -R ₇₃ R ₈₀ -R ₈₃		SO
	Input Pins		R ₉₀ -R ₉₃		\overline{INT}_0 \overline{INT}_1 SI \overline{SCK} (Note 2) Input mode

- Notes : 1. In stop mode \overline{HLT} is 0 and HLT is 1. Then I/O Pin is in high-impedance state.
 2. In serial interface interrupt, SCK pin is input pin if external clock input mode is selected.

to V_{CC} on the printed circuit of the user system.

$R4_0/\overline{SCK}$ and $R4_2/\overline{SO}$ should be set to $R4_0$ and $R4_2$ by serial mode register and port mode register, respectively.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 19 shows the parts to be initialized by MCU reset, and the status of each.

		MOS Without Pull-Down (PMOS Open Drain)	Pins
Standard Pins (II)	I/O Pins		D_4-D_{15} $R1_0-R1_3$ $R2_0-R2_3$
	Output Pins		RO_0-RO_3
	Input Pins		RA_0, RA_1

Note: In stop mode, \overline{HLT} is 0. Then I/O pins are in high-impedance state.

Table 18. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins (I)	CMOS	No	—
	MOS without pull-up (NMOS open drain)	Yes	1
Standard Pins (II)	MOS without pull-down (PMOS open drain)	Yes	0

Table 19. Initial Value at MCU Reset

Items		Initial Value at MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin (I) NMOS Open Drain { MOS Without Pull-Up }	1	Enable input
	Standard Pin (II) PMOS Open Drain { MOS Without Pull-Down }	0	Enable input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register.
	Serial Mode Register (SMR)	0000	See serial mode register.
	Timer Mode Register A (TMA)	000	See timer mode register A.
	Timer Mode Register B (TMB)	0000	See timer mode register B.
Timer/Counter, Prescaler	\$000	—	
Serial interface	Timer/Counter A (TCA)	\$00	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—
	Octal Counter	000	—

Note: MCU reset affects the rest of registers as follows:

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software again.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above



Internal Oscillator Circuit

Figure 15 outlines the internal oscillator circuit. Crystal oscillator or ceramic filter oscil-

lator can be selected as the oscillator type. Refer to table 20 to select the type. In addition, see figure 16 for layout of the crystal or ceramic filter.

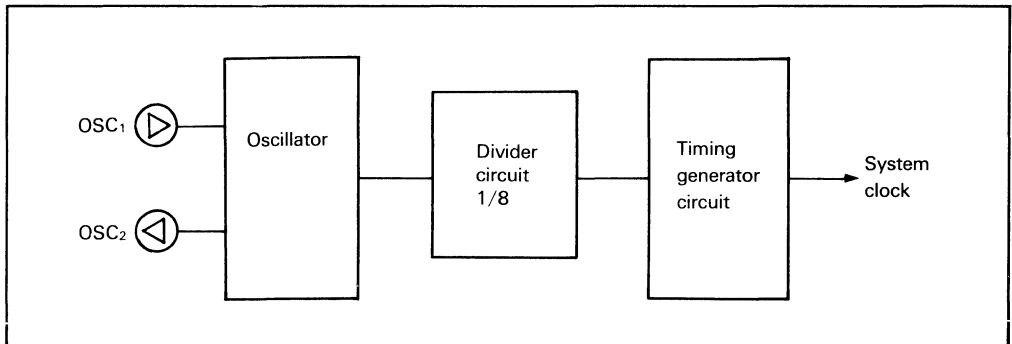


Figure 15. Internal Oscillator Circuit

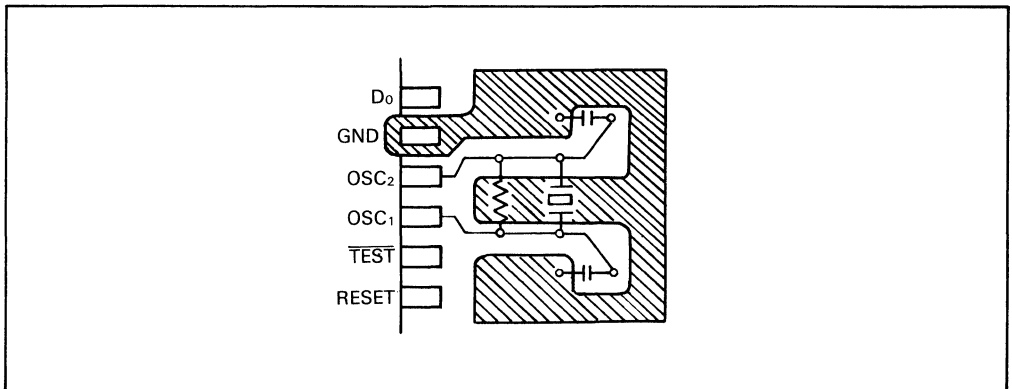
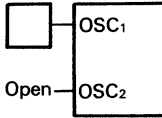
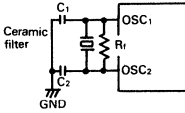
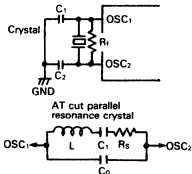


Figure 16. Layout of Crystal and Ceramic Filter

Table 20. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation	<p>Oscillator</p> 	
Ceramic Filter Oscillator		<p>Ceramic filter CSA8.00MT (Murata) R_f: 1 MΩ ± 20% C₁: 30 pF ± 20% C₂: 30 pF ± 20%</p>
Crystal Oscillator		<p>R_f: 1 MΩ ± 20% C₁: 10-22 pF ± 20% C₂: 10-22 pF ± 20% Crystal: equivalent to circuit shown C₀: 7 pF max. R_S: 100 Ω max. f: 1.0-9 MHz</p>

- Notes :
1. Since the circuit constant changes according to the crystal and ceramic filter resonator and stray capacitance of the board, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
 2. Wiring among OSC₁, OSC₂, and elements should be as short as possible, and never cross other wiring. Refer to figure 16.

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 21). Figure 17 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruction puts the MCU into standby mode. In

standby mode, the oscillator circuit is active and interrupts, timer/counter and serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Condition		
							Input/Output Pin	Timer/Counter, Serial Interface	Recovery Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ²	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ¹	Stop	Retained	High impedance	Stop	RESET input

Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to table 19 for the contents of the flags and registers.

2. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

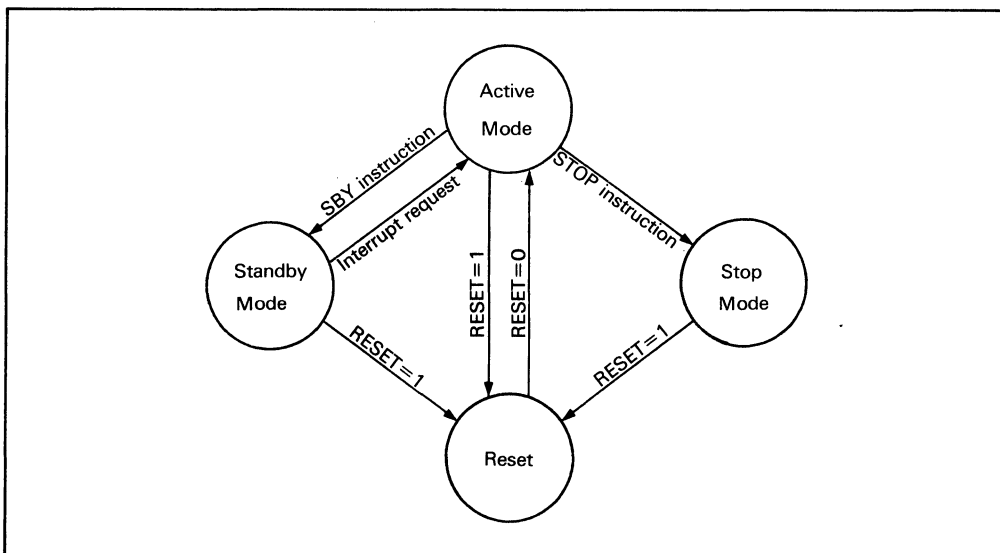


Figure 17. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 18 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 19, reset input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers,

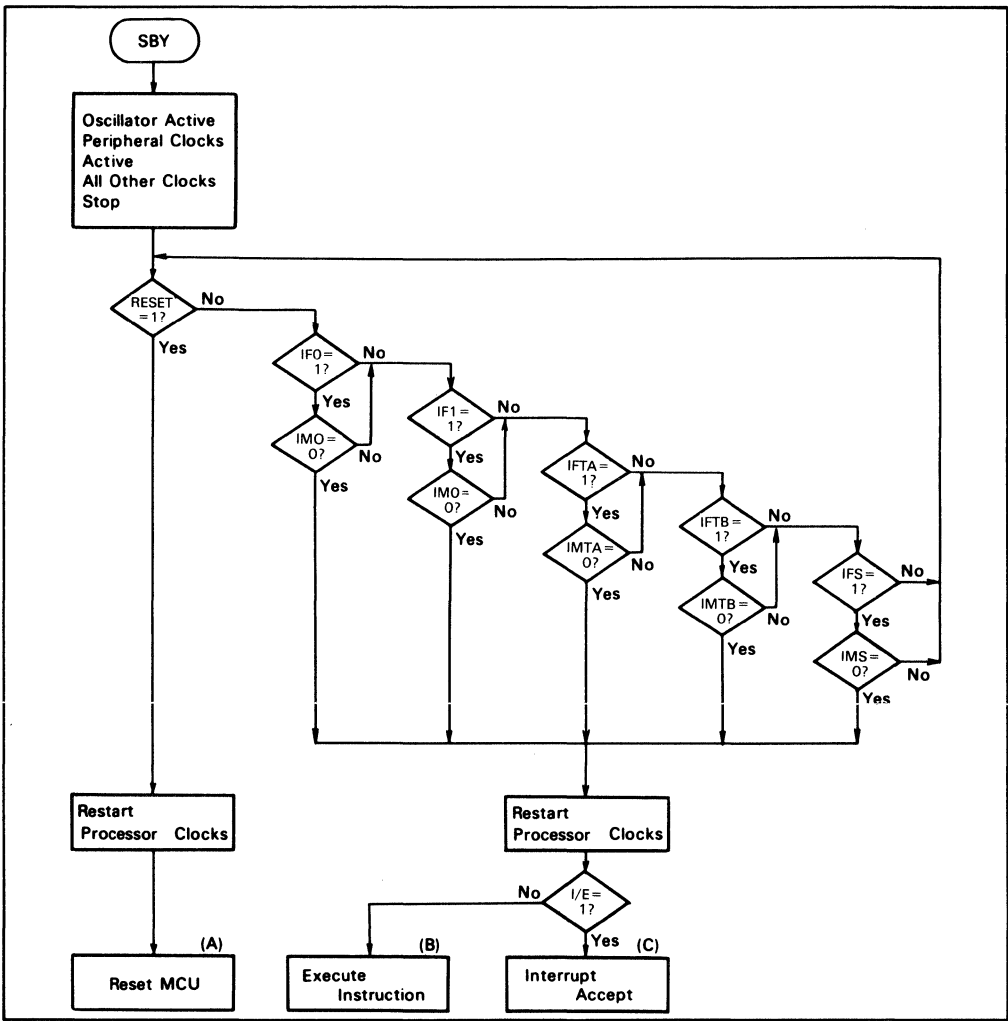


Figure 18. MCU Operating Flowchart in Standby Mode

Y/SPY registers, carry, and serial data register may not retain their contents.

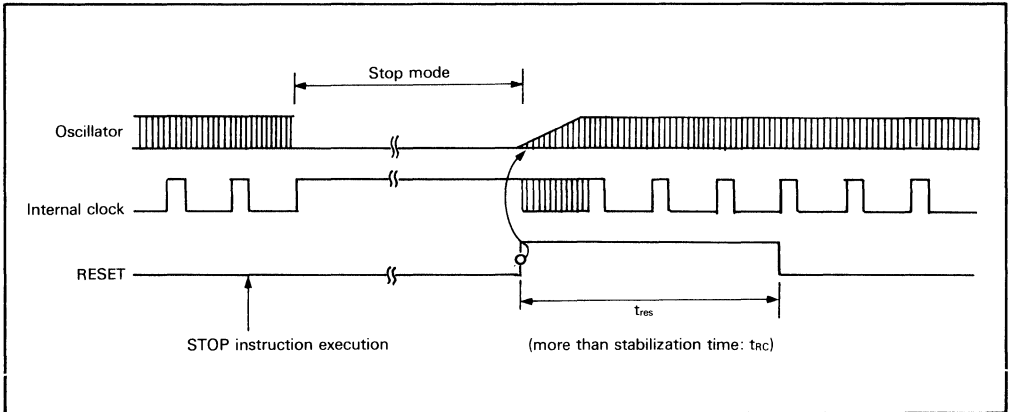


Figure 19. Timing Chart of Recovering from Stop Mode

Programmable ROM Operation

The HD4074008's on-chip PROM is programmed in PROM mode (figures 20, 21 and 22). PROM mode is set by bringing TEST, \overline{M}_0 , and \overline{M}_1 low, and RESET high as shown in figure 21. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 23 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporate conversion circuit to use a general perpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 22. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The HD4074008 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 22 shows how programming and verification modes are selected.

Figure 23 is a programming flowchart, and figure 33 is a timing chart. For precautions on PROM programming, refer to ZTAT MCU On-Chip PROM Characteristics and Precautions for Applications.

Erasing

The PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are : ultraviolet (UV) light with wavelength 2537Å with a minimum irradiation of 15W·sec/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. Addresses \$0000 to \$3FFF should be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. Data in unused addresses should be set to \$FF. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.)
2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer of socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with V_{pp}=12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074008, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{pp}.

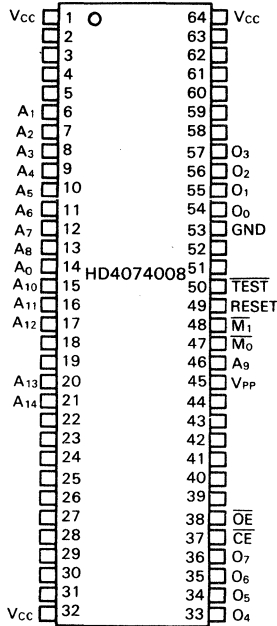
Table 22. PROM Mode Selection

Mode	Pin			
	CE	OE	V _{pp}	
Programming	low	High	V _{pp}	Data input
Verify	High	Low	V _{pp}	Data output
Programming inhibited	High	High	V _{pp}	High impedance

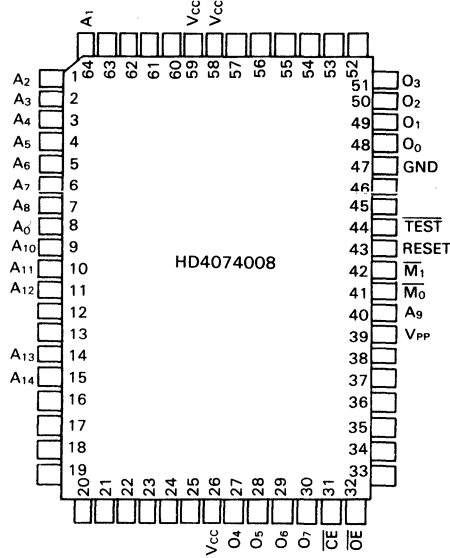
Table 23. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type Name	Maker	Type Name	Package
DATA I/O	22B 29B	Hitachi	HS408ESS11H	DP-64S DC-64S
			HS408ESF01H	FP-64
			HS408ESF03H	FP-64A
AVAL Corp	PKW-1000 PKW-7000	Hitachi	HS408ESS21H	DP-64S DC-64S
			HS408ESF01H	FP-64
			HS408ESF03H	FP-64A

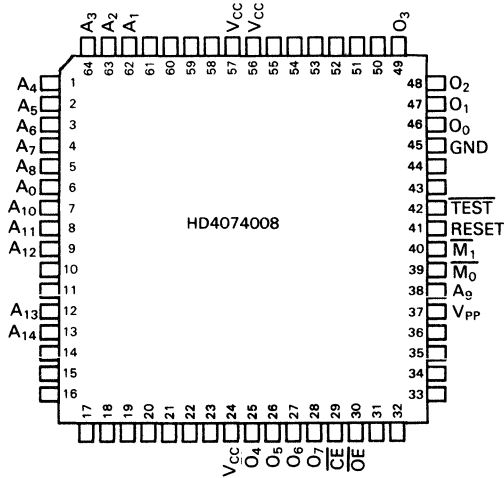
HD4074008



(DP-64S, DC-64S)



(FP-64)



(FP-64A)
(Top View)

G: GND (V_{SS} level)
Nomark: open

Figure 20. PROM Mode Pin Arrangement



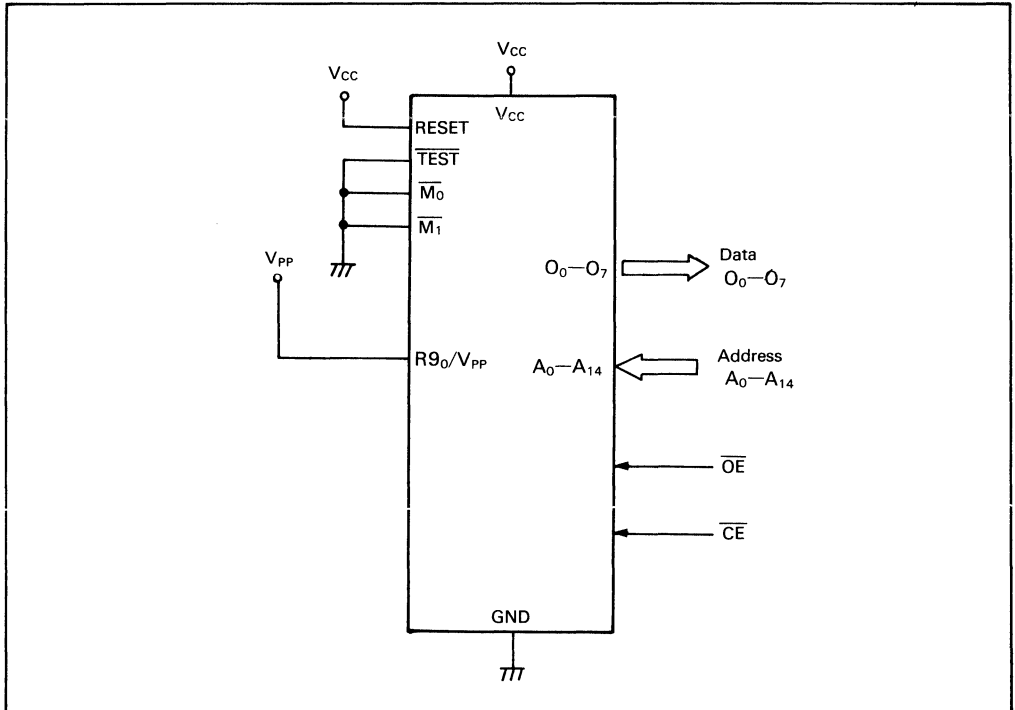


Figure 21. PROM Mode Function Diagram

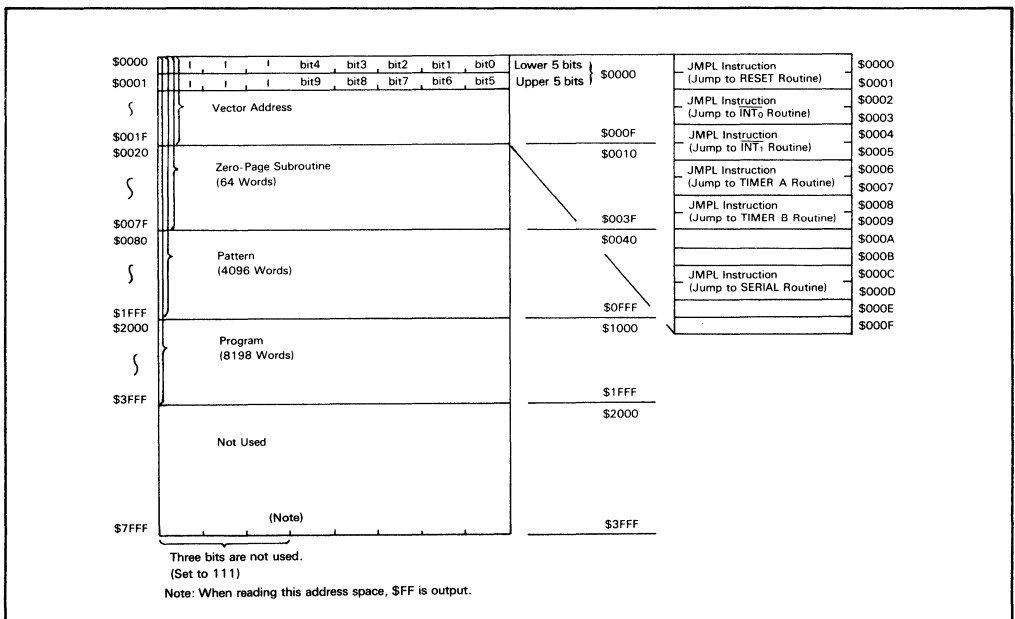


Figure 22. PROM Mode Memory Map



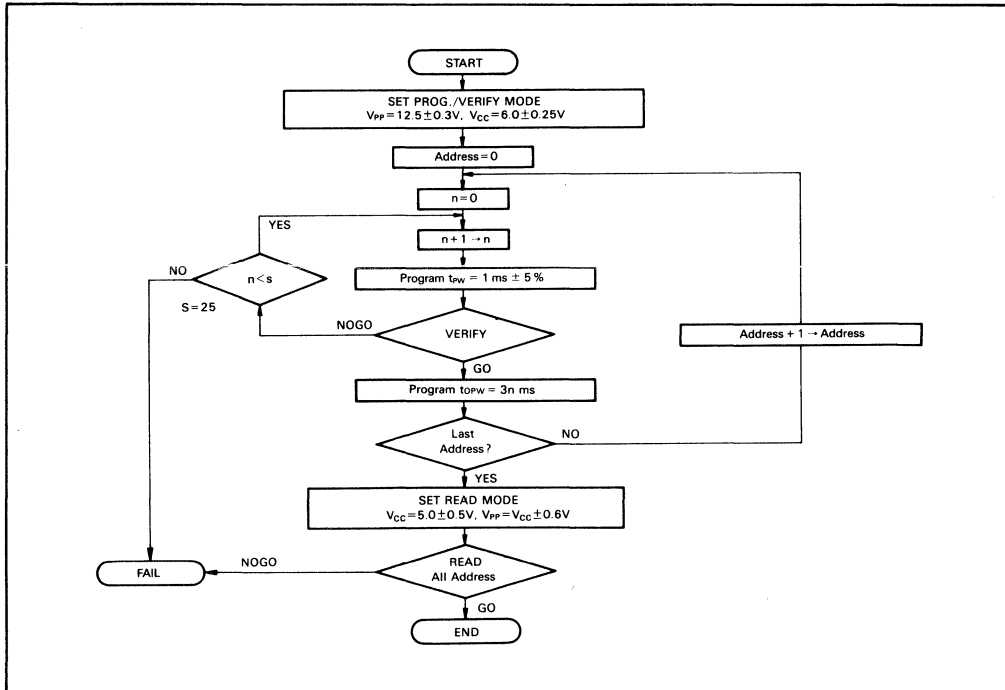


Figure 23. High Speed Programming Flowchart

Addressing Modes

RAM Addressing Mode

As shown in figure 24, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 25.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_{13} to PC_0) with the 8-bit immediate data.

When BR is on page boundary ($256n + 255$) (figure 26), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 27). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

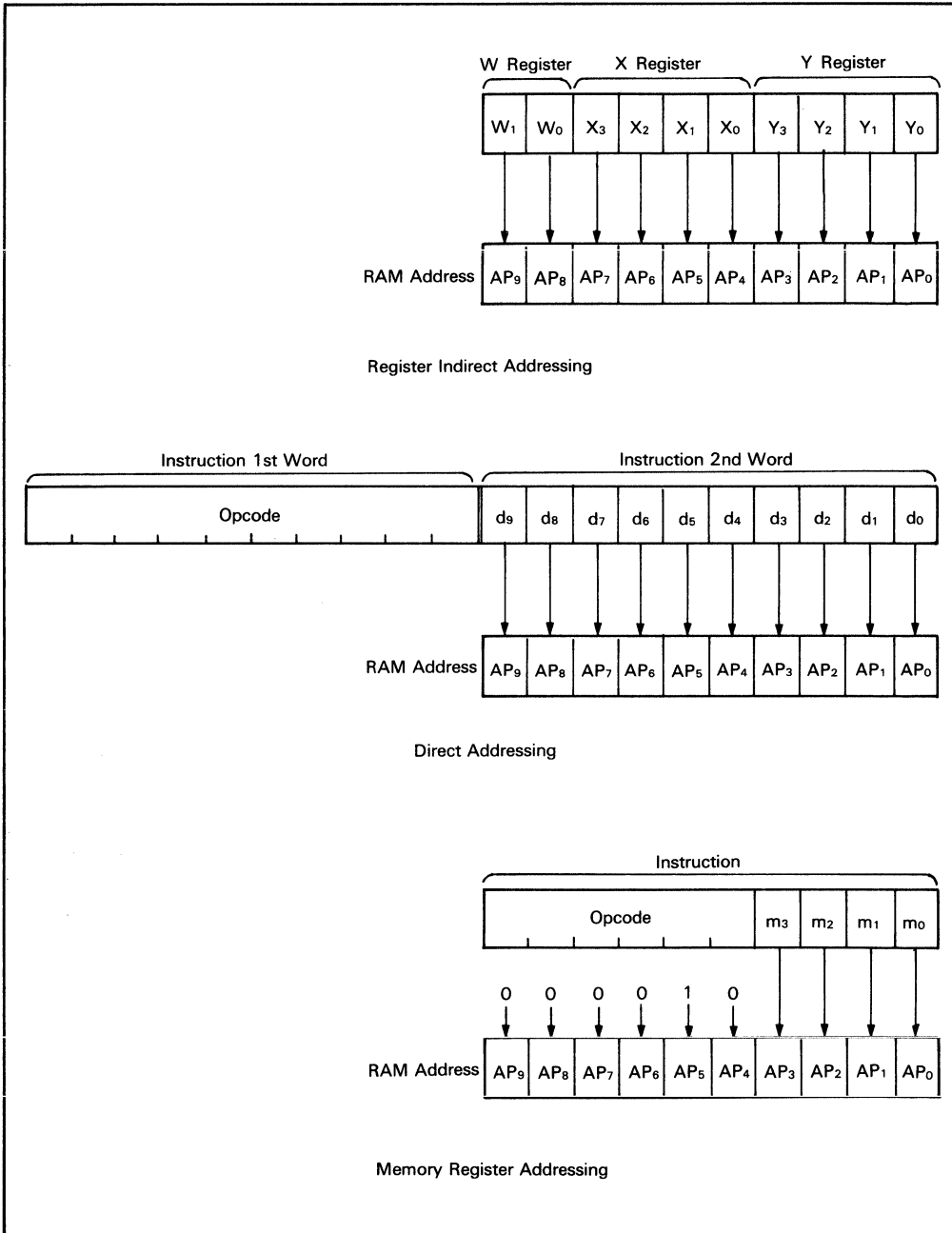


Figure 24. RAM Addressing Mode

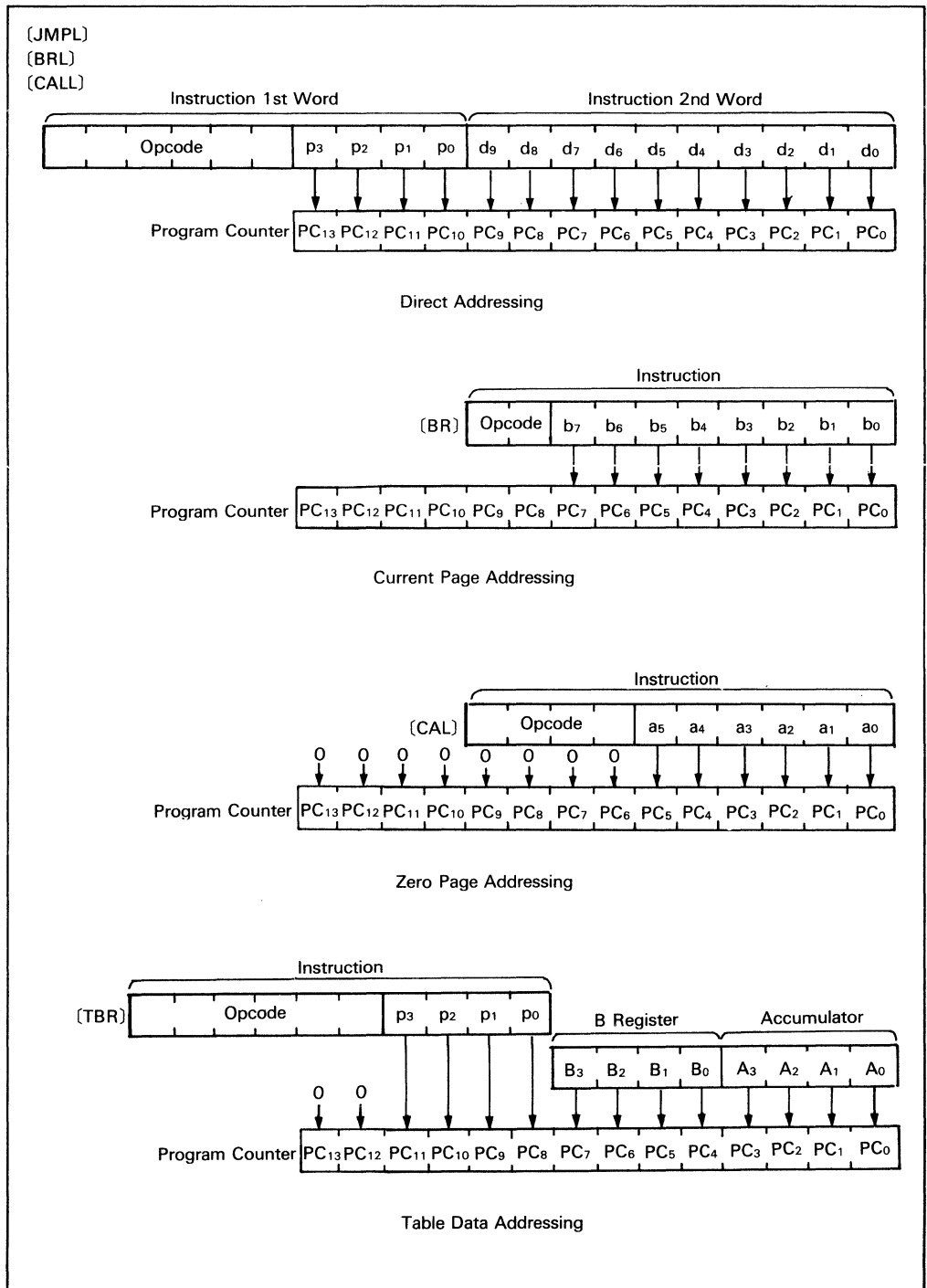


Figure 25. ROM Addressing Mode



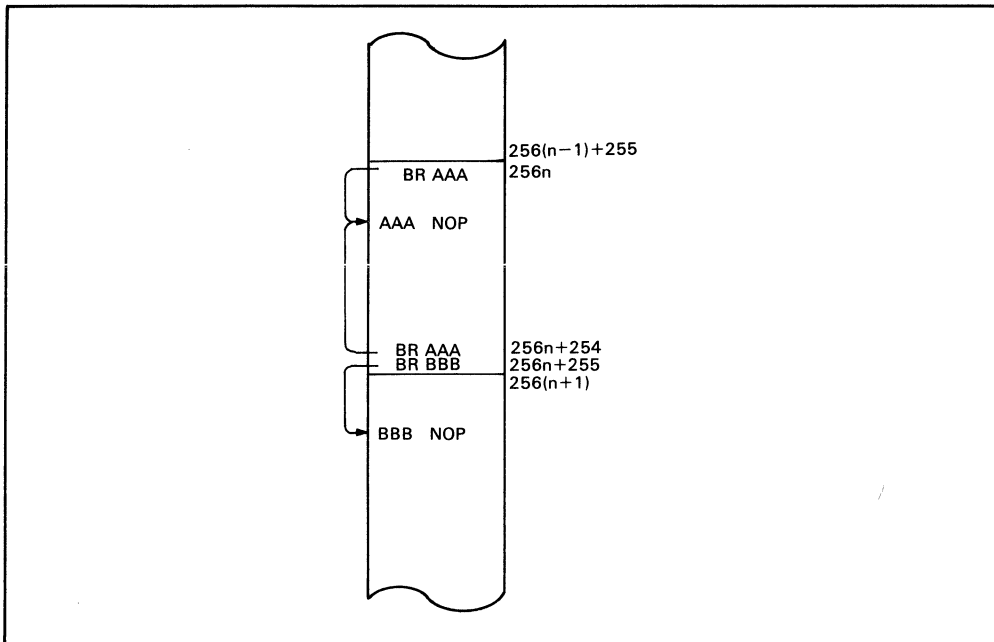


Figure 26. The Branch Destination by BR Instruction on the Boundary between Pages

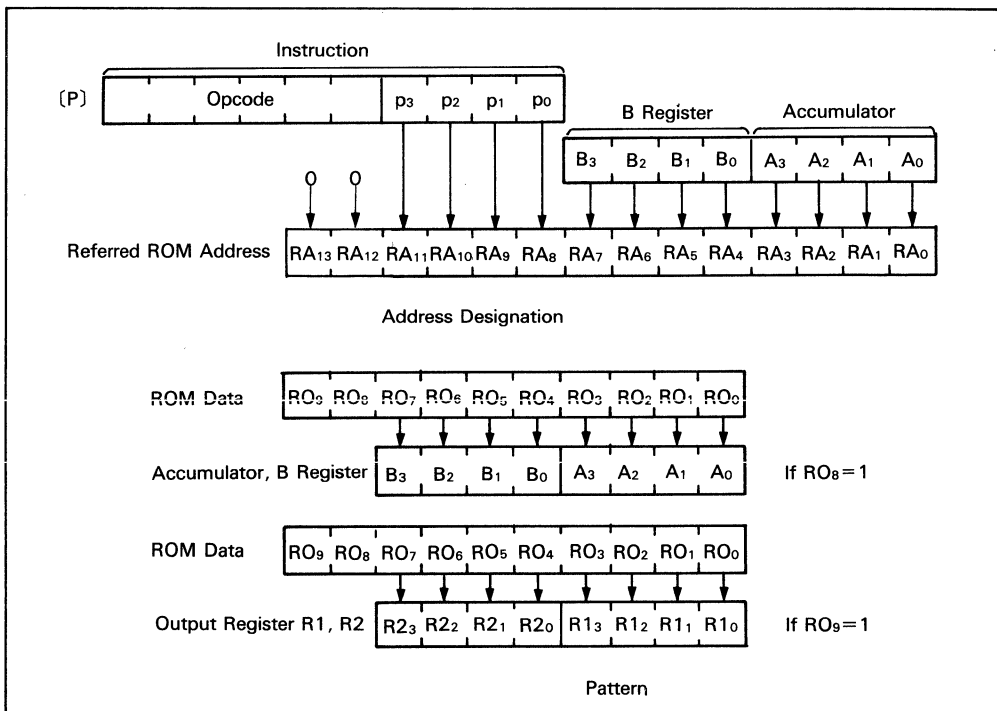


Figure 27. P Instruction



Instruction Set

The HD4074008 provides 101 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 24-33 list their functions, and table 34 is an opcode map.

Table 24. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 25. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 26. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 0 1	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 27. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y+1 → Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y-1 → Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).
The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 28. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

Table 29. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 30. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 31. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 32. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 33. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 34. Opcode Map

R8		0																1															
R9	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	NOP	XSP	XSP	XSP	ANXY	EM			AM				ORM			LAW				ANEMD				AMD				ORMD				
	1	RTN	RTN			ALEM				AMC				EORM			LWA				ALEMCD				AMCD				EORMD				
	2	INEM								i(4)				INEMD								i(4)											
	3	ILEM								i(4)				ILEMD								i(4)											
	4	LBM(XY)		BNEM				LAB				IB				COMB				OR			STS				SBYSTOP						
	5	LMAY(X)				AYY				LASY			Y																	JMPL	p(4)		
	6	NEGA				RED				LASPY																				CALL	p(4)		
0	7	YNEI								i(4)				BRL								p(4)											
	8	XMA(XY)				SEM	n(2)			REM	n(2)			TM	n(2)		XMAD				SEMD	n(2)			REMD	n(2)			TMD	n(2)			
	9	LAM(XY)				LMA(XY)			SMC				ANM				LAMD				LAMD				SMCD				ANMD				
	A	ROT	ROT					DAA					DAS				LAY													LMID	i(4)		
	B	TBR								p(4)				P								p(4)											
	C	XMB(XY)				BLEM				LBA							DB																
	D	LMADY(X)				SY				LYA							DY																
	E	TD				SED				LXA				REC			SEC													CAL	a(6)		
	F	LWI		i(2)																													
1	0	LBI		i(4)																													
	1	LYI		i(4)																													
	2	LXI		i(4)																													
	3	LAI		i(4)																													
	4	LBR		m(4)																													
	5	LAR		m(4)																													
	6	REDD		m(4)																													
	7	LAMR		m(4)																											BR	b(8)	
	8	AI		i(4)																													
	9	LMIIY		i(4)																													
	A	TDD		m(4)																													
	B	ALEI		i(4)																													
	C	LRB		m(4)																													
	D	LRA		m(4)																													
	E	SEDD		m(4)																													
F	XMRA		m(4)																														

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction
 2-word/2-cycle Instruction (2-word/2-cycle)



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14	V	3
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Total Allowance of Output Current	$-\Sigma I_O$	150	mA	6
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Applied to R9₀ (V_{PP})
 4. Standard pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. D₀ - D₃ and R3 - R8.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. D₀ - D₃ and R3 - R8.
 11. R0 - R2.
 12. D₄ - D₁₅.

Electrical Characteristics

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, \overline{SCK} , INT ₀ , INT ₁	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
		SI	$0.7V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, \overline{SCK} , INT ₀ , INT ₁	- 0.3		$0.2 V_{CC}$	V		
		OSC ₁	- 0.3		0.5	V		
		SI	- 0.3		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	\overline{SCK} , SO	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{mA}$	
			$V_{CC} - 0.5$			V	$-I_{OH} = 0.5\text{mA}$	
Output Low Voltage	V_{OL}	\overline{SCK} , SO		0.4		V	$I_{OL} = 1.6\text{mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , INT ₀ , INT ₁ , OSC ₁ , SI, SO			1	μA	$V_{in} = 0\text{ V}$ to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			4.5	mA	$V_{CC} = 5\text{ V}$	2, 5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}			1.7	mA	Maximum logic operation $V_{CC} = 5\text{ V}$	3, 5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}			10	μA	$V_{in}(\overline{TEST}) = V_{CC} - 0.3\text{V}$ to V_{CC} , $V_{in}(\text{RESET}) = 0\text{ V}$ to 0.3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, \overline{TEST} : V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: GND
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - \overline{TEST} : V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: GND
 - Excluding pull-down MOS current.
 - When $f_{osc} = x\text{ MHz}$, estimate the current dissipation as follows:
 Max value @ $x\text{ MHz} = x/8 \times (\text{max value @ } 8\text{ MHz})$



Input/Output Characteristics for Standard Pin (I) : NMOS Open Drain
($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R3-R5 R9	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R3-R5 R9	- 0.3		0.3 V_{CC}	V		
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R3-R8			0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₃ , R3-R9			1	μA	$V_{in} = 0\text{ V}$ to V_{CC}	1

Note: 1. Pull-up MOS current and output buffer current are excluded.

Input/Output Characteristics for Standard Pin (II) : PMOS Open Drain
($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₄ -D ₁₅ , R1, R2, RA ₀ , RA ₁	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₄ -D ₁₅ , R1, R2, RA ₀ , RA ₁	- 0.3		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₄ -D ₁₅	$V_{CC} - 3.0$			V	- $I_{OH} = 15\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 2.0$			V	- $I_{OH} = 10\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 1.0$			V	- $I_{OH} = 4\text{ mA}$, $V_{CC} = 5\text{ V}$	
		R0-R2	$V_{CC} - 3.0$			V	- $I_{OH} = 3\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 2.0$			V	- $I_{OH} = 2\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 1.0$			V	- $I_{OH} = 0.8\text{ mA}$, $V_{CC} = 5\text{ V}$	
Input/Output Leakage Current	$ I_{IL} $	D ₄ -D ₁₅ , R0-R2, RA ₀ , RA ₁			1	μA	$V_{in} = 0$ to V_{CC}	1

Note: 1. Pull-down MOS current and output buffer current are excluded.

AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	8	9	MHz	divide by 8	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs		
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	41			ns	divide by 8	2
External Clock Rise Time	t_{CPr}	OSC ₁			15	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			15	ns		2
\overline{INT}_0 High Level Width	t_{0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms		4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.

2. See figure 28.
3. See figure 29.
4. See figure 30.

Serial Interface Timing Characteristics

AT Transfer Clock Output

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{cyc}	SCK	1			t_{cyc}		1.2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK	0.5			t_{scyc}		1.2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK			100	ns		1.2
Serial Output Data Delay Time	t_{DSO}	SO			250	ns		1.2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns		1

AT Transfer Clock Input

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{cyc}	SCK	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK	0.5			t_{scyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK			100	ns		1
Serial Output Data Delay Time	t_{DSO}	SO			250	ns		1.2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns		1

- Notes: 1. See figure 31
2. See figure 32

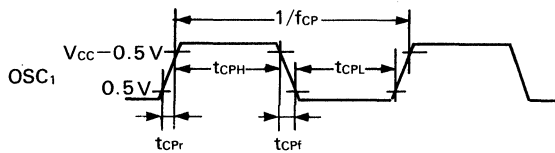


Figure 28. Oscillator Timing

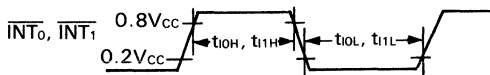


Figure 29. Interrupt Timing

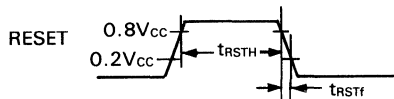


Figure 30. Reset Timing

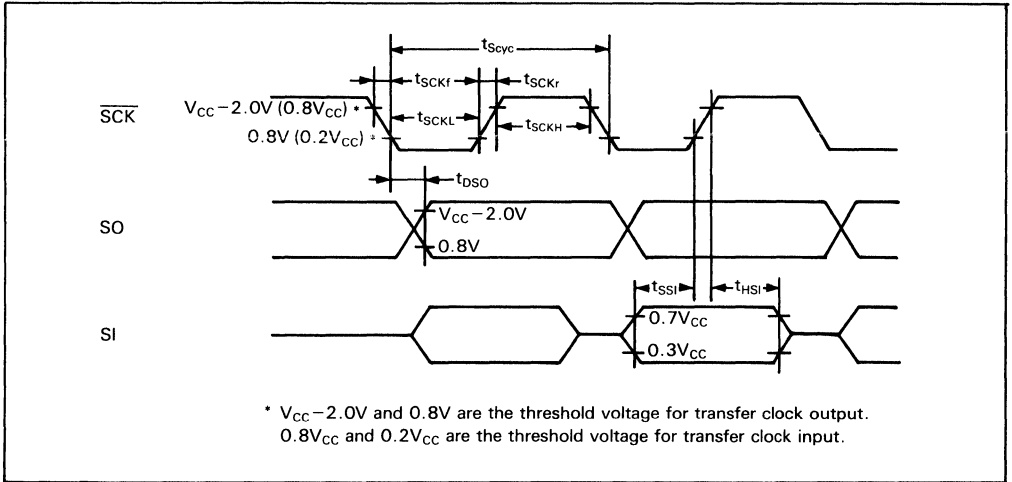


Figure 31. Timing Diagram of Serial Interface

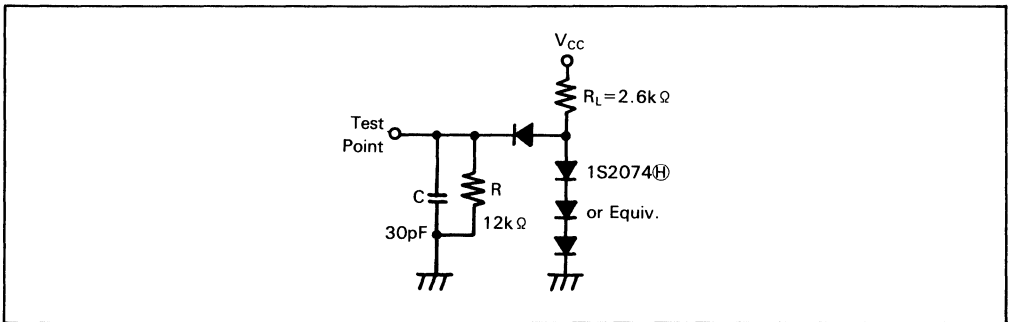


Figure 32. Timing Load Circuit

**Programming Electrical Characteristics
Write and Verify Mode**

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{V}/0.5\text{V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time		t_{AS}	2			μs	Fig. 33*
\overline{OE} set-up time		t_{OES}	2			μs	
Data set-up time		t_{DS}	2			μs	
Address hold time		t_{AH}	0			μs	
Data hold time		t_{DH}	2			μs	
Output disable delay time		t_{DF}			130	ns	
V_{PP} set-up time		t_{VPS}	2			μs	
Program pulse width		t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming		t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time		t_{VCS}	2			μs	
Data output delay time		t_{OE}	0		500	ns	

Note : * Input Pulse level 0.8~2.2V

Input rising/falling time $\leq 20\text{ns}$

Timing reference level { input : 1.0V, 2.0V
output : 0.8V, 2.0V



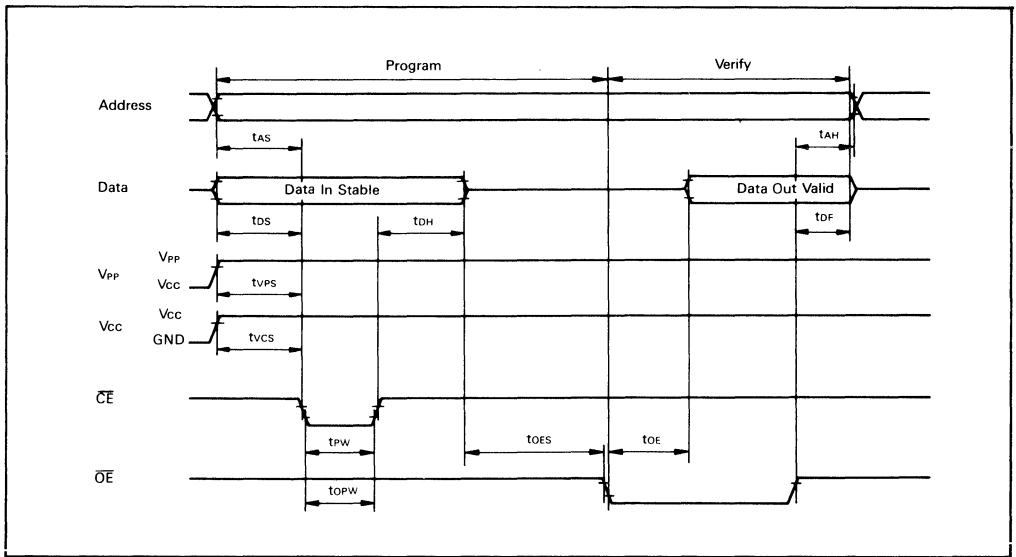


Figure 33. PROM Programming/Verify Timing

Read Mode

DC Characteristics

($V_{SS} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Leakage Current	I_{LI}			1	μA	$V_{CC} = 5.5\text{ V}$, $V_{in} = \text{GND to } V_{CC}$
Output Leakage Current	I_{LO}			1	μA	$V_{CC} = 5.5\text{ V}$, $V_{out} = \text{GND to } V_{CC}$
Program Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC} + 0.6\text{ V}$
Current Dissipation Active Mode	I_{CC}			30	mA	
Input Voltage	V_{IL}	-0.3		0.8	V	
	V_{IH}	2.2		$V_{CC} + 0.3$	V	
Output Voltage	V_{OL}			0.40	V	$I_{OL} = 1.6\text{ mA}$
	V_{OH}	2.4			V	$I_{OH} = -200\ \mu\text{A}$

AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Max	Unit	Test Condition	Note
Access Time	t_{ACC}		500	ns	$\overline{CE} = \overline{OE} = V_{IL}$	
\overline{CE} Output Delay Time	t_{CE}		500	ns	$\overline{OE} = V_{IL}$	
\overline{OE} Output Delay Time	t_{OE}	10	150	ns	$\overline{CE} = V_{IL}$	
Output Disable Delay Time	t_{DF}	0	105	ns	$\overline{CE} = V_{IL}$	1
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$	

Note: 1. T_{DF} is defined when output becomes open because output level can not be referred.

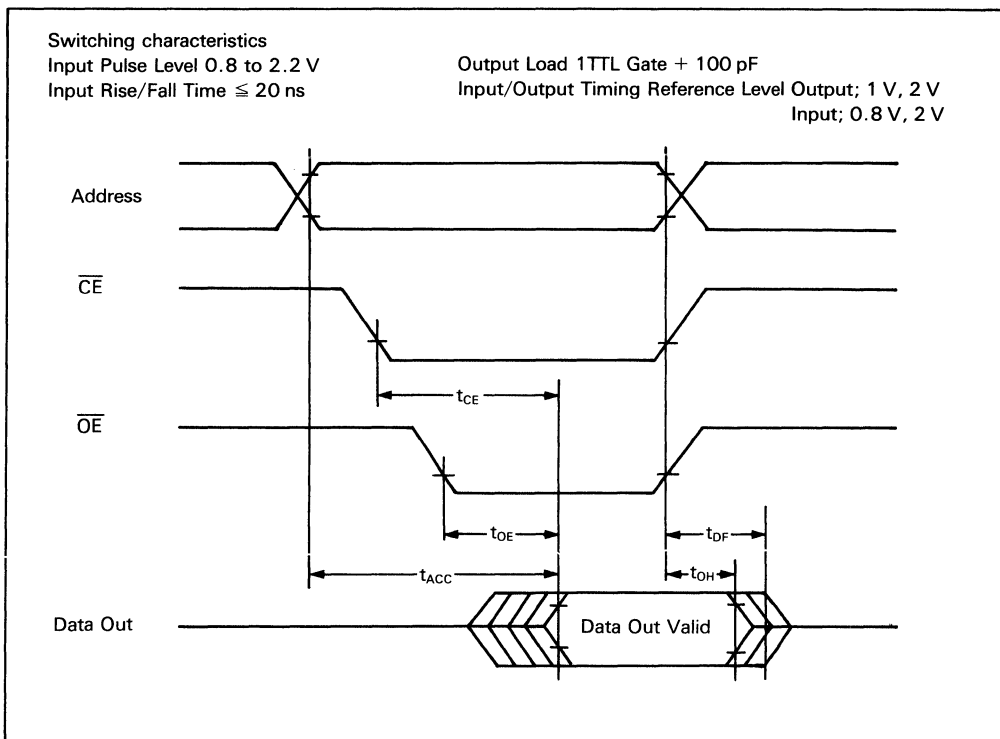


Figure 34. PROM Read Timing

HD404019/HD4074019

—Preliminary—

Description

The HD404019, HD4074019 are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, serial interface, and 2 timer/counters and contains high-voltage I/O pins, including high-current output pins to drive fluorescent displays directly.

Features

- 4-bit architecture
- 16384 words of 10-bit ROM
 - Mask ROM: HD404019
 - PROM: HD4074019
- 992 digits of 4-bit RAM
- 58 I/O pins, including 26 high-voltage I/O pins (40 V max)
- 2 timer/counters
 - 11-bit prescaler
 - 8-bit free running timer/counter
 - 8-bit auto-reload timer/event counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
 - External: 2
 - Timer/counter: 2
 - Serial interface: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time
 - 0.89 μ s
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Crystal or ceramic filter
 - External clock

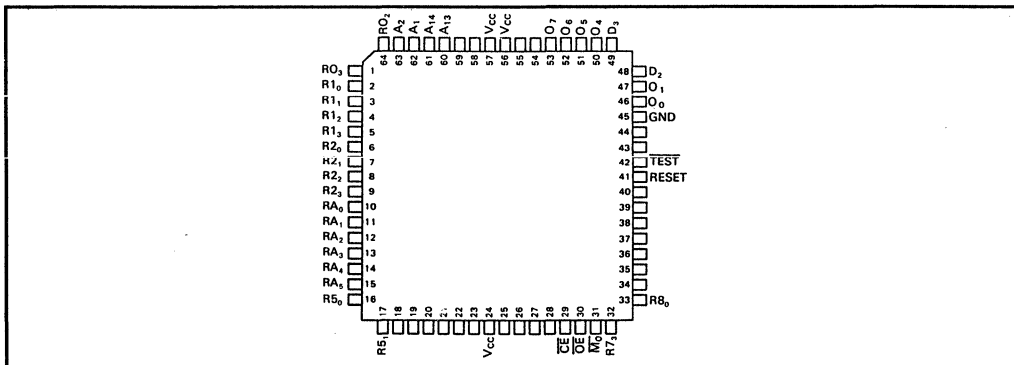
- Packages
 - 64-pin shrink type plastic DIP
 - 64-pin flat plastic package
 - 64-pin shrink type ceramic DIP with window
- Instruction set compatible with HMCS408: 101 instructions
- High programming efficiency with 10-bit/word ROM: 79 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Ordering Information

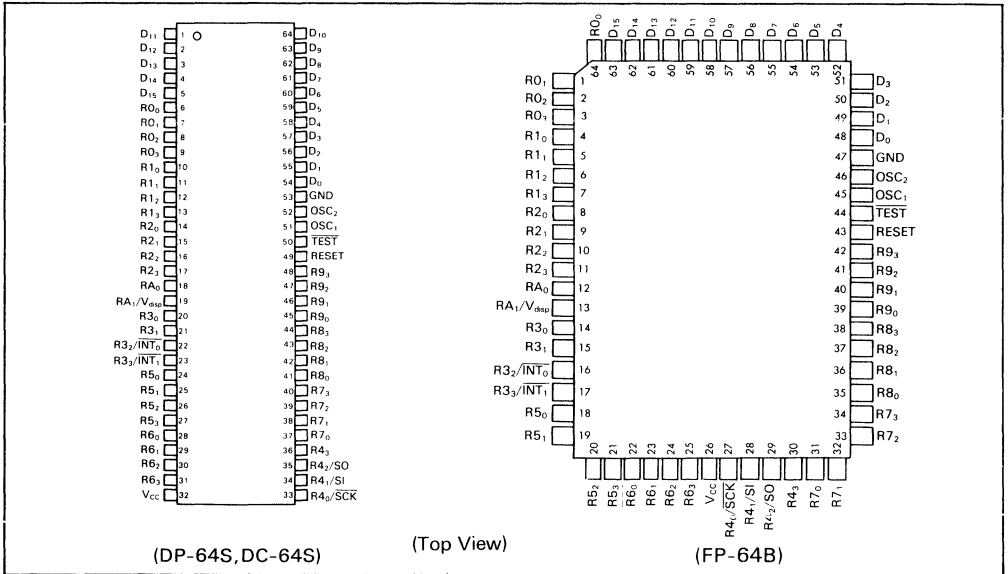
	Part No.	Package
Mask ROM type	HD404019S	DP-64S
	HD404019F	FP-64B
	HD404019H	FP-64A
ZTAT type	HD4074019S	DP-64S
	HD4074019F	FP-64B
	HD4074019C	DC-64S
	HD4074019H	FD-64A



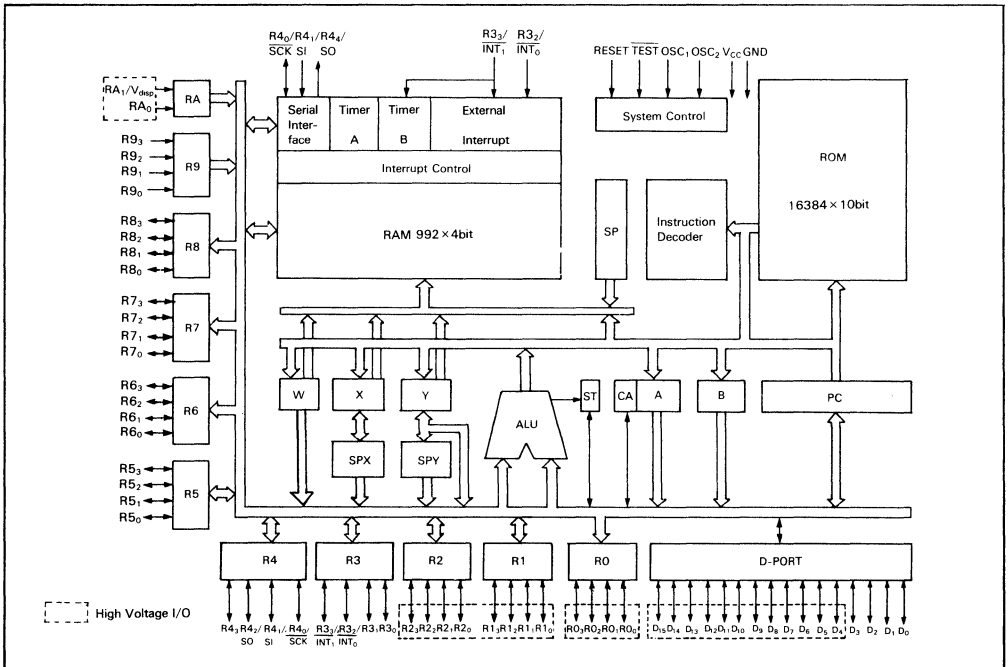
FP-64A



Pin Arrangement



Block Diagram





Differences between PROM in Package, EPROM on Package and Mask ROM Types

Item	PROM in Package ZTAT						EPROM on Package			Mask ROM							
	HD4074019		HD4074008		HD614PO80S HD614PO160S		HD404019	HMCS408AC/C/CL		HMCS404AC/C/CL		HMCS402AC/C/CL					
Typical instruction execution time	1 μ s		1 μ s		1.33 μ s		1 μ s	1 μ s	2 μ s	4 μ s	1 μ s	2 μ s	4 μ s	1 μ s	2 μ s	4 μ s	
Power supply voltage (V)	4.5-5.5		4.5-5.5		4.5-5.5		3.5-6	4.5-6	3.5-6	2.5-6	4.5-6	4-6	2.7-6	4.5-6	4-6	2.7-6	
ROM	16,384 words × 10 bit		8,192 words × 10 bit		HN27C64: 4,096 × 10 bit HN4827128: 8,192 × 10 bit HN27C256: 16,384 × 10 bit		16,384 words × 10 bit	8,192 words × 10 bit	4,096 words × 10 bit		2,048 words × 10 bit						
RAM	992 × 4 bit		512 × 4 bit		576 × 4 bit		992 × 4 bit	512 × 4 bit		256 × 4 bit		160 × 4 bit					
I/O pin circuit	Standard pins	NMOS open drain		NMOS open drain		NMOS open drain		Each pin can be without pull-up MOS (NMOS open drain), with pull-up MOS, or CMOS									
	High voltage pins	PMOS open drain		PMOS open drain (Typical 5 V use)		PMOS open drain		Each pin can be without pull-down MOS (PMOS open drain) or with pull-down MOS									
Clock generation	Crystal	○		○		○		○		○		○		○		○	
	Ceramic Resistance	○		○		○		○		○		○		○		○	
Package	Type	DC-64S (Window)	DP-64S FP-64A	FP-64B	DC-64S (Window)	DP-64S	FP-64 FP-64A	DC-64SP	DP-64S	FP-64B FP-64A	DP-64S	FP-64	DP-64S	FP-64	DP-64S	FP-64	
	Occupied area (mm ²)	18.8 × 57.3	17 × 58	18.8 × 24.8	18.8 × 57.3	17 × 58	19.6 × 25.6	23 × 57.3	17 × 58	18.8 × 24.8	17 × 58	19.6 × 25.6	17 × 58	19.6 × 25.6	17 × 58	19.6 × 25.6	
	Height from stand off (mm)	5.6 (Max)	5.1 (Max)	2.9 (Max)	5.6 (Max)	5.1 (Max)	2.9 (Max)	7.5 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	5.1 (Max)	2.9 (Max)	

Notes: DC-64S: 64-pin shrink type ceramic DIP with window
 DP-64S: 64-pin shrink type DIP
 FP-64: 64-pin flat plastic package (rectangular shape)
 FP-64A: 64-pin flat plastic package (square shape)
 FP-64B: 64-pin flat plastic package (rectangular shape)

DC-64SP: 64-pin shrink type ceramic piggy back
 ○: Available
 —: Not available

Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the power supply pins for the MCU.

Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC} - 40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₅ (D Port)

The D port is an input/output port addressed by the bit. These 16 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₅ are

high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁–R₁₃, R₂–R₂₃, R₃–R₃₃, R₄–R₄₃, R₅–R₅₃, R₆–R₆₃, R₇–R₇₃, R₈–R₈₃, R₉–R₉₃, RA₀, RA₁ (R Ports)

R₀ to R₉ are 4-bit I/O ports. RA is a 2-bit port. R₉ and RA are input ports, and R₀ to R₈ I/O ports. R₀, R₁, R₂, and RA are high-voltage ports, and R₃ to R₉ are standard ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, R₃₃, R₄₀, R₄₁, and R₄₂ are multiplexed with INT₀, INT₁, SCK, SI, and SO respectively. For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R₄₀, R₄₁, and R₄₂ respectively. For details, see Serial Interface Section.

Functional Description

ROM Memory Map

The MCU includes 16384 words × 10 bits of ROM (mask ROM or PROM). It is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions can refer to the ROM data as a pattern.

Program Area (\$0000 to \$3FFF): Locations from \$0000 to \$1FFF can be used for program code.

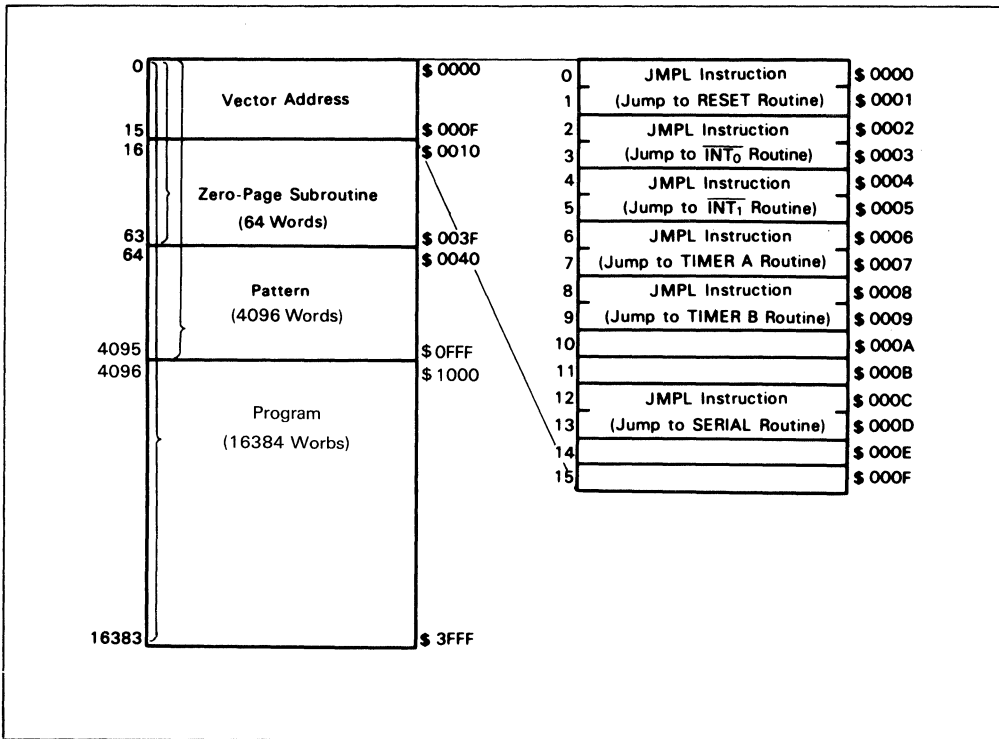


Figure 1. ROM Memory Map



RAM Memory Map

The MCU includes 992 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction.

However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

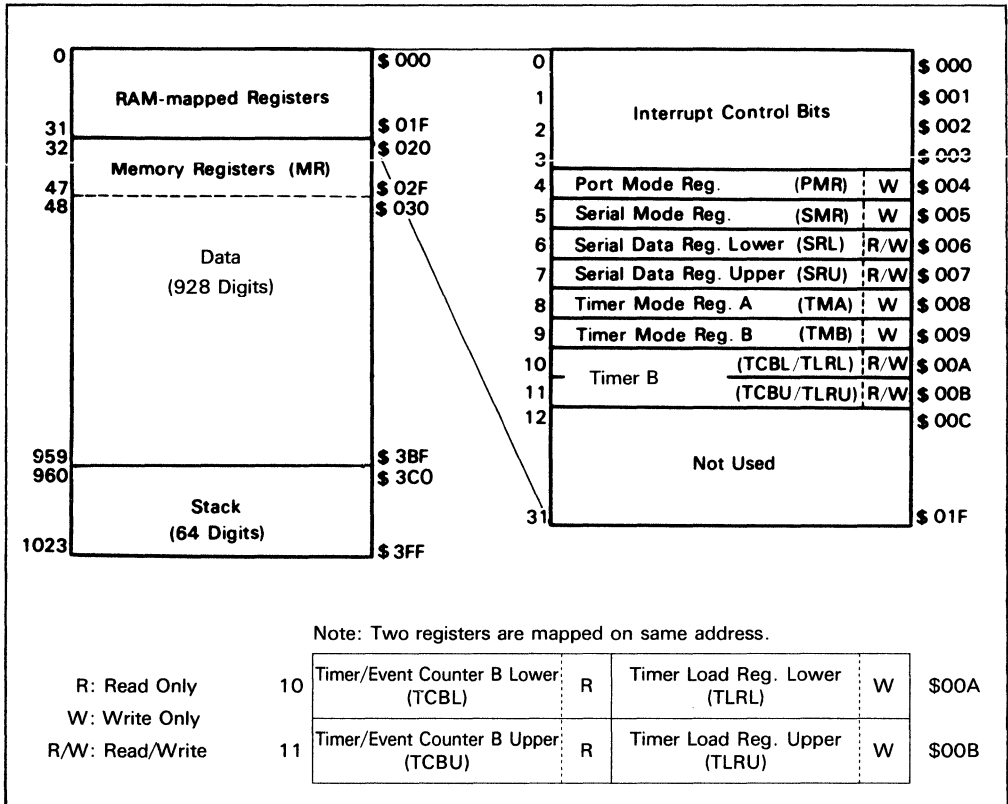


Figure 2. RAM Memory Map



Data Area (\$020 to \$3BF): 16 digits, \$020 through \$02F, of the data area are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when su-

broutine calls (CAL instruction, CALL instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

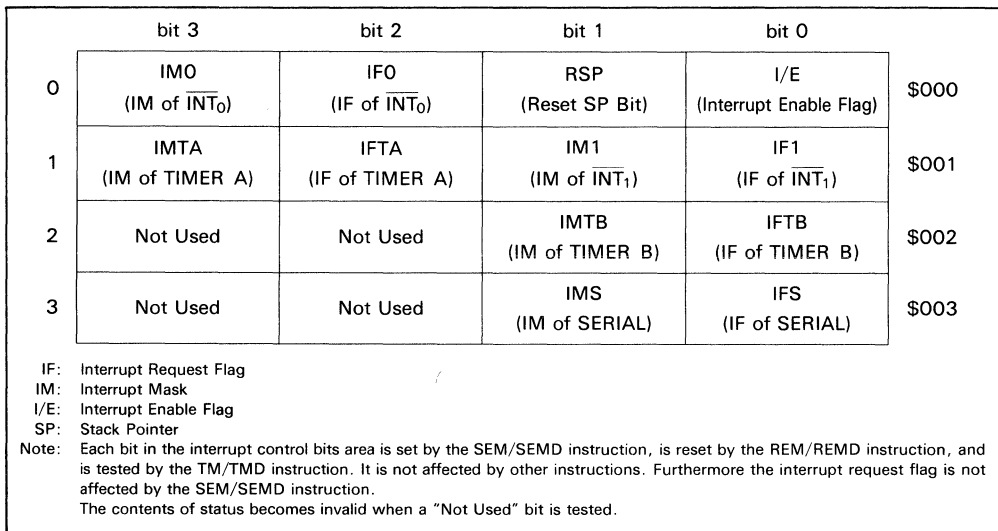


Figure 3. Interrupt Control Bit Area Configuration

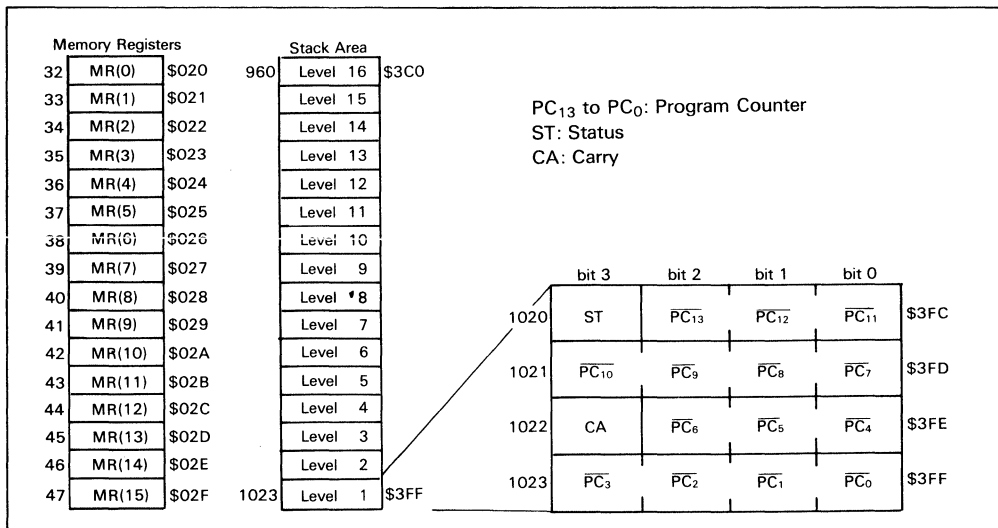


Figure 4. Configuration of Memory Register, Stack Area, and Stack Position



Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register, and the 4-bit X and Y registers indirectly address RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU

overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value for the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack. It is restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) points to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the high four bits of the stack pointer are fixed at 1111.

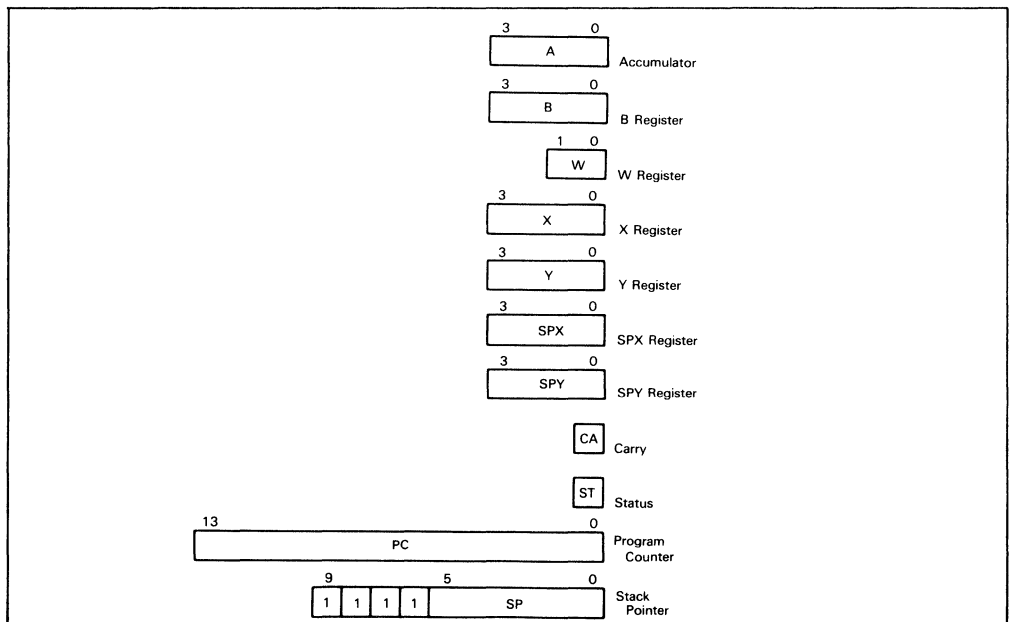


Figure 5. Registers and Flags



The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit, reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timer A, timer B), and serial port (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses control and maintain the interrupt request. The interrupt enable flag (IE) also controls interrupt operations.

Interrupt Control Bits and Interrupt Service:

The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

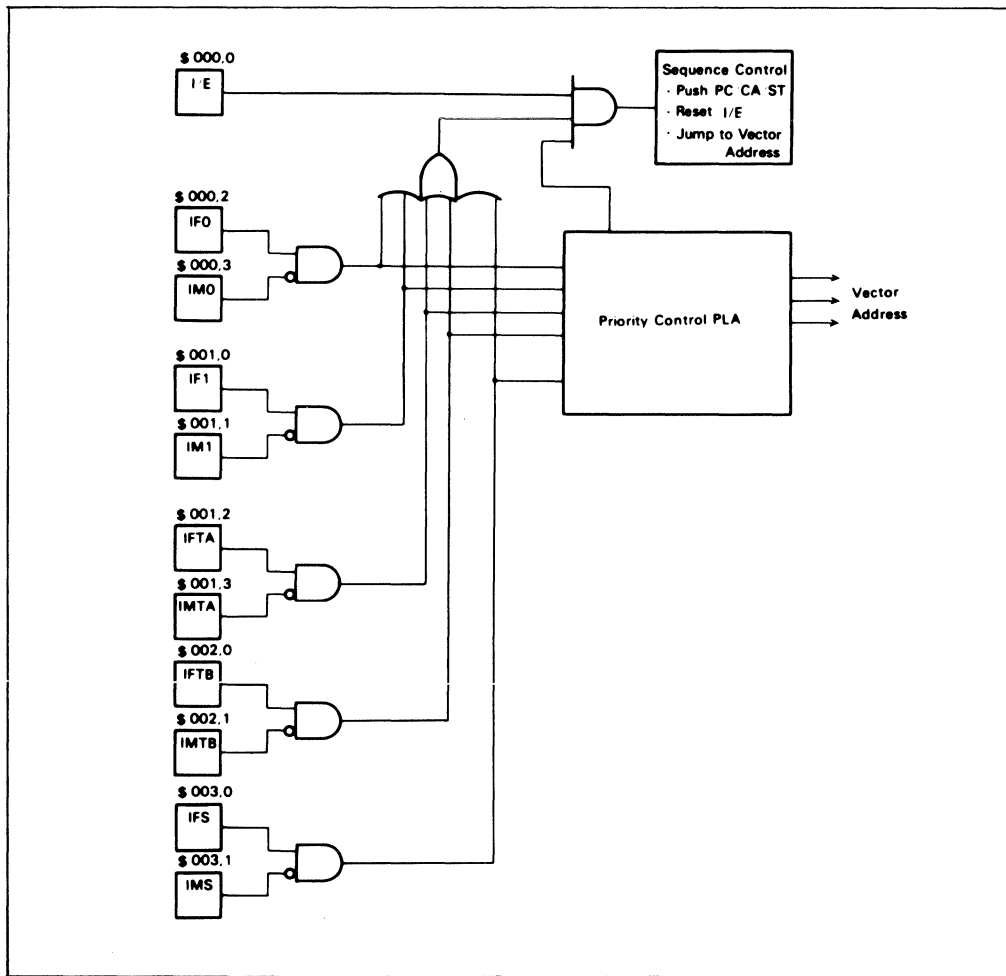


Figure 6. Interrupt Control Circuit Block Diagram



An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle.

In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	TimerA	TimerB	SERIAL
I/E	1	1	1	1	1
IF0· $\overline{IM0}$	1	0	0	0	0
IF1· $\overline{IM1}$	*	1	0	0	0
IFTA· \overline{IMTA}	*	*	1	0	0
IFTB· \overline{IMTB}	*	*	*	1	0
IFS· \overline{IMS}	*	*	*	*	1

Note: * Don't care

Interrupt Enable Flag (I/E: \$000 Bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then timer B counts up at each falling edge of the \overline{INT}_1 input. When \overline{INT}_1 is used as timer B external event input,

external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 Bit 2, IF1: \$001 Bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 Bit 3, IM1: \$001 Bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, $R3_3/\overline{INT}_1$ pin, $R4_1/SI$ pin, and $R4_2/SO$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (mask)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin

PMR1	$R4_1/SI$ Pin
0	Used as $R4_1$ port input/output pin
1	Used as SI input pin

PMR0	$R4_2/SO$ Pin
0	Used as $R4_2$ port input/output pin
1	Used as SO output pin

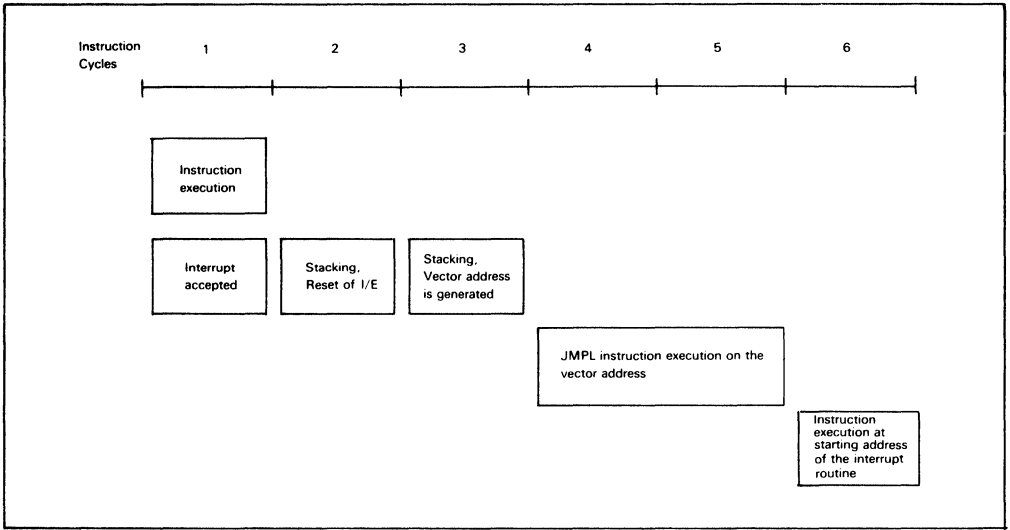


Figure 7. Interrupt Servicing Sequence

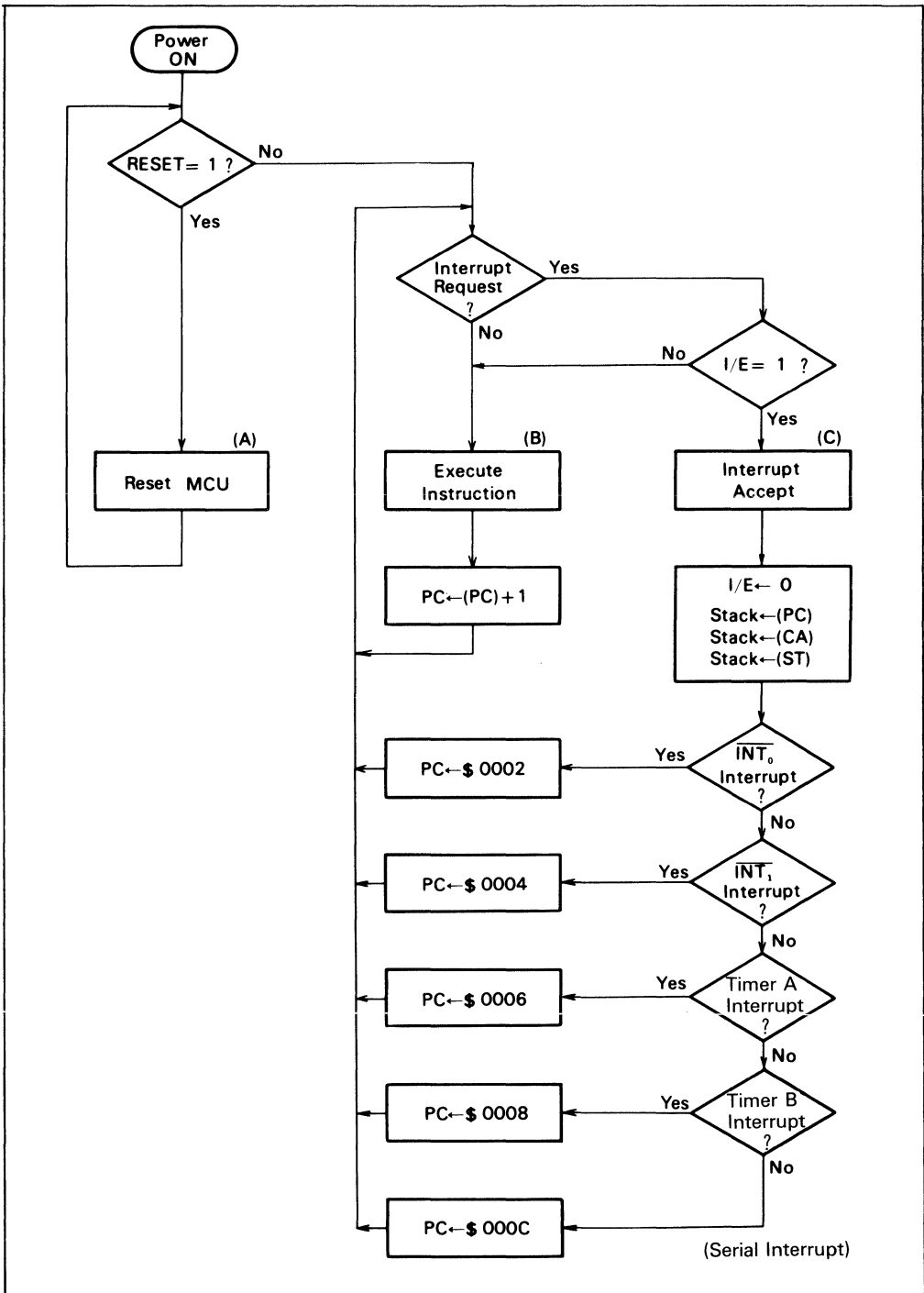


Figure 8. Interrupt Servicing Flowchart



Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register, the octal counter, and the multiplexer as illustrated in figure 9. Pin $R4_0/\overline{SCK}$ and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

STS instruction initiates serial interface operations and resets the octal counter to \$0. The counter starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of SCK. When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued when the octal counter is reset, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the $R4_0/\overline{SCK}$, prescaler divide ratio, and transfer clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from accepting transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after the serial mode register has been written to.

Therefore, the STS instruction must be executed after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SRL: \$006, SRU: \$007): The 8-bit read/write serial data register consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time, external data is input from the SI pin to the serial data register, MSB first, synchronously with the rising edge of the transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data can not be guaranteed.

Serial Interrupt Request Flag (IFS: \$003 Bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: \$003 Bit 1): The serial interrupt masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by a write signal to the serial mode register when the operation mode is changed.

Table 7. Serial Mode Register

SMR3	R4 ₀ /SCK
0	Used as R4 ₀ port input/output pin
1	Used as SCK input/output pin

Transfer Clock						
SMR 2	SMR 1	SMR 0	R4 ₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	SCK Output	Prescaler	÷ 2048	÷ 4096
0	0	1	SCK Output	Prescaler	÷ 512	÷ 1024
0	1	0	SCK Output	Prescaler	÷ 128	÷ 256
0	1	1	SCK Output	Prescaler	÷ 32	÷ 64
1	0	0	SCK Output	Prescaler	÷ 8	÷ 16
1	0	1	SCK Output	Prescaler	÷ 2	÷ 4
1	1	0	SCK Output	System Clock	—	÷ 1
1	1	1	SCK Input	External Clock	—	—

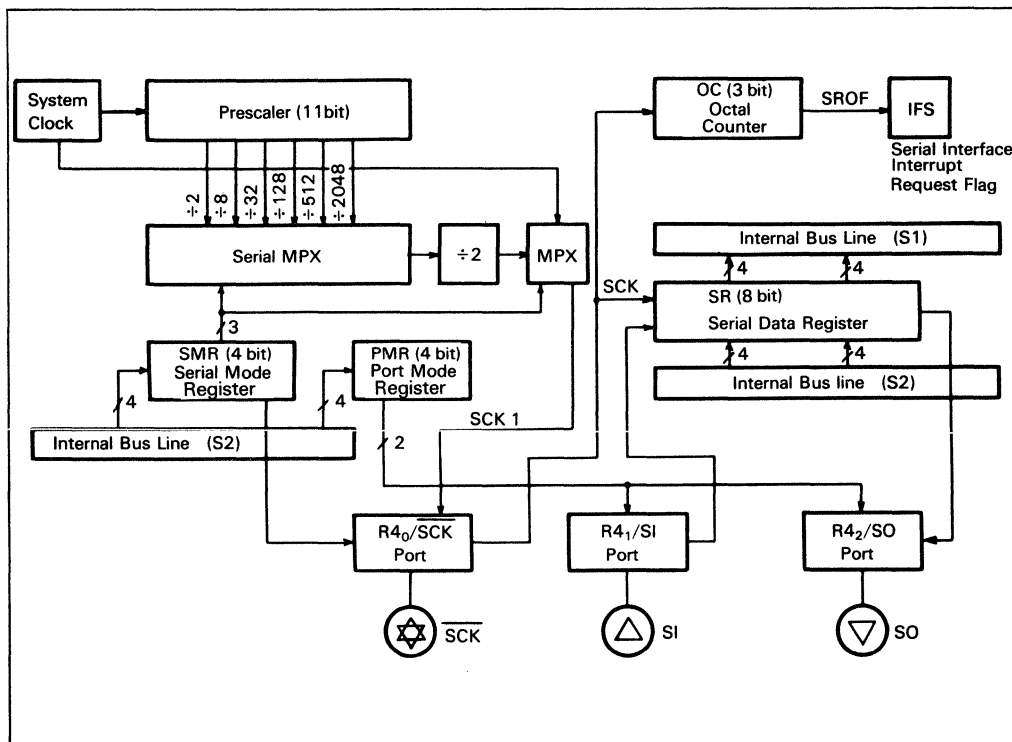


Figure 9. Serial Interface Block Diagram

Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by the operation mode changing through a change in the data in the port mode register, or by data being written into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK waiting state.

In this state the falling edge of the first trans-

fer clock causes the serial interface shift to transfer state. While the octal counter counts up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.

The octal counter becomes 000 again after 8 transfer clocks or execution of an STS instruction, so the serial interface returns to SCK waiting state and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output triggered by the execution of an STS instruction, and it stops after 8 clocks.

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

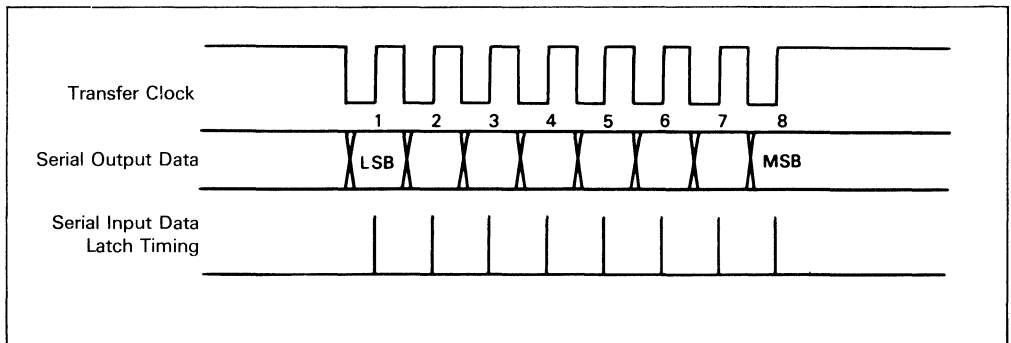


Figure 10. Serial Interface I/O Timing Chart

Transfer Clock Errors Detection Example: The serial interface functions abnormally when the transfer clock is disturbed by external noises. Transfer clock errors can be detected by the procedure shown in figure 12.

SCK waiting state, the state of the serial interface shifts as follows: first, transfer state, second, SCK waiting state and third, transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure sets the serial IRF again.

If more than 8 transfer clocks occur in the

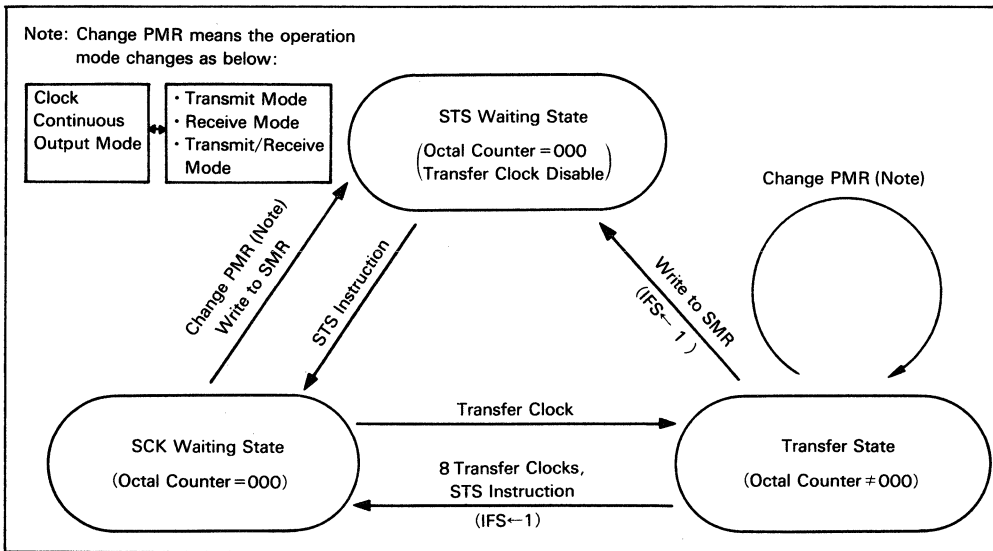


Figure 11. Serial Interface Operation State

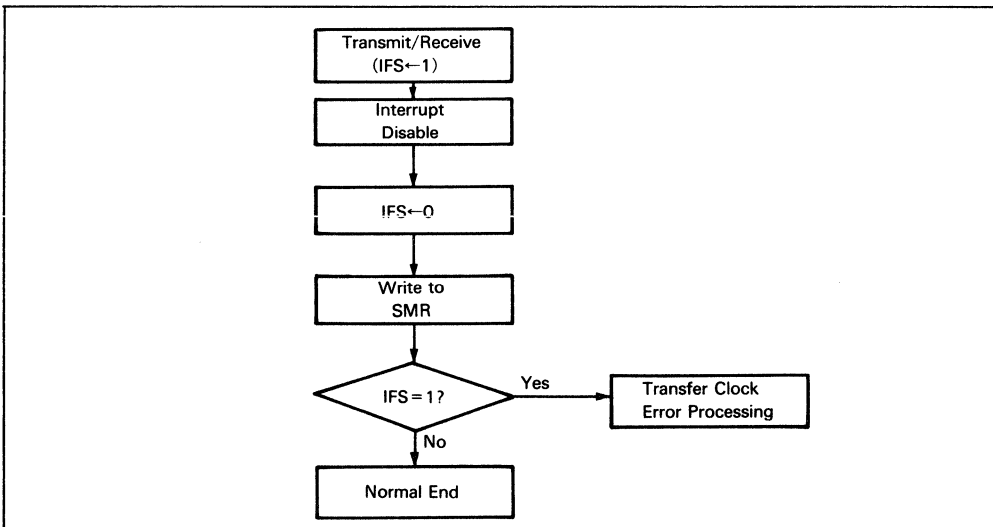


Figure 12. Transfer Clock Error Detection Example

Timer

The MCU contains a prescaler and two timer/counters (timer A, timer B). See figure 13. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter, and timer B an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to \$0000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), or the serial mode register (SMR).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A becomes \$FF, it generates an overflow and becomes \$00. This overflow causes the timer A interrupt request

flag (IFTA: \$001 bit 2) to go to 1. This timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by timer mode register A (TMA: \$008).

Timer B Operation: Timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio of timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB:

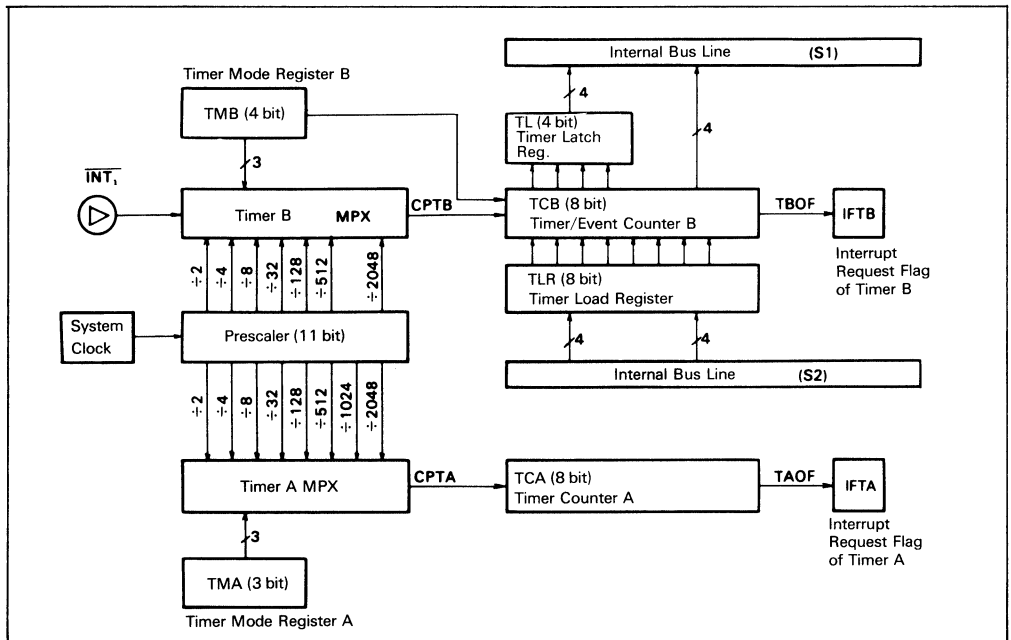


Figure 13. Timer/Counter Block Diagram



\$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: \$008):

Timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input, as shown in table 11. The timer mode register A is initialized to \$0 by MCU reset.

Timer Mode Register B (TMB: \$009):

Timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B):

Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. Write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

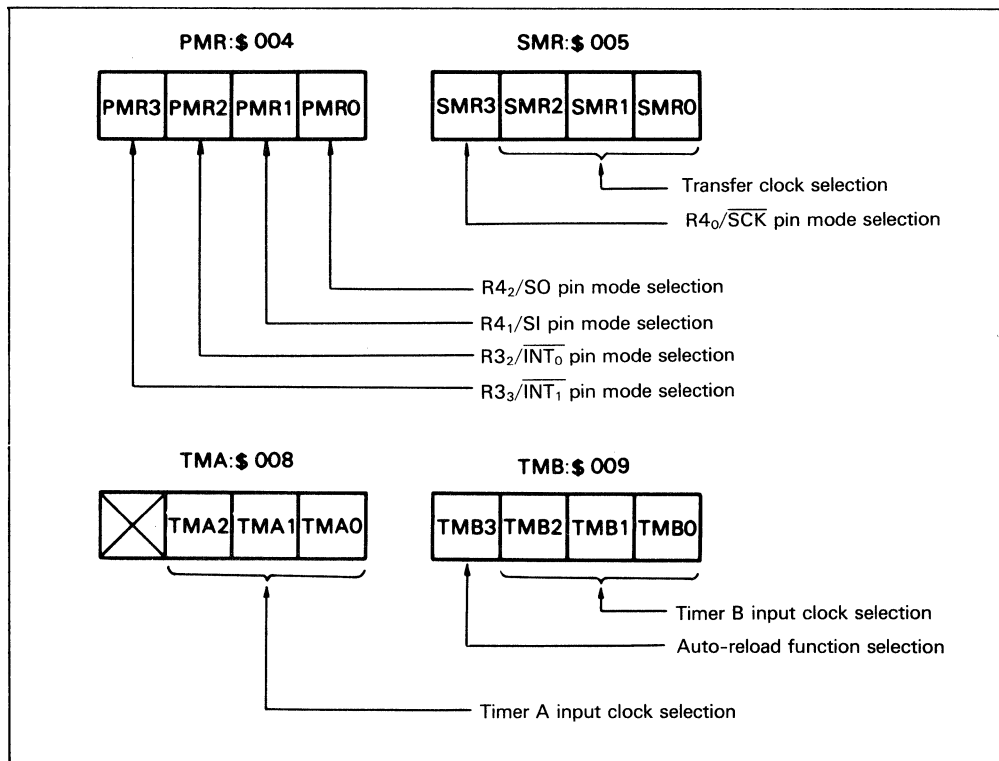


Figure 14. Mode Register Configuration and Function



Timer A Interrupt Request Flag (IFTA: \$001 Bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 13).

Timer A Interrupt Mask (IMTA: \$001 Bit 3): The timer A interrupt mask prevents an interrupt request from being generated by the timer A interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: \$002 Bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Timer B Interrupt Mask (IMTB: \$002 Bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 16).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{\text{INT}}_1$ (External Event Input)

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Input/Output

The MCU has 58 I/O pins, 32 standard and 26 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain); and one of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the R_{A1}/V_{disp} pin via mask option when with pull-down MOS option is selected for at least one high-voltage pin. See table 17 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

Output Circuit Operation of Standard Pins With Pull-Up MOS: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps the PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the \overline{HLT} signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: I/O port D has 16 discrete I/O pins,

each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See tables 17 and 18 for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The eleven R ports in the HD404019/HD4074019 are composed of 36 I/O pins, and 6 input-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read when the output-only and/or non-existing ports are read.

The R_{32} , R_{33} , R_{40} , R_{41} , and R_{42} pins are multiplexed with the $\overline{INT_0}$, $\overline{INT_1}$, \overline{SCK} , \overline{SI} , and \overline{SO} pins respectively. See tables 17 and 18 for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-down MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

R_{40}/\overline{SCK} and R_{42}/\overline{SO} should be used as R_{40} and R_{42} by serial mode register and port mode register respectively.

Table 17. I/O Pin Circuit Types

		Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
Standard Pins	I/O Common Pins				D ₀ –D ₃ R ₃₀ –R ₃₃ R ₄₀ –R ₄₃ R ₅₀ –R ₅₃ R ₆₀ –R ₆₃ R ₇₀ –R ₇₃ R ₈₀ –R ₈₃
	Input Pins				R ₉₀ –R ₉₃

Table 17. I/O Pin Circuit Types (cont)

		Without Pull-Down MOS (PMOS Open Drain) (D)	With Pull-Down MOS (E)	Applicable Pins
High Voltage Pins	I/O Common Pins			D ₄ –D ₁₅ R ₀₀ –R ₀₃ R ₁₀ –R ₁₃ R ₂₀ –R ₂₃
	Input Pins			RA ₀
	Input Pins			RA ₁

Table 17. I/O Pin Circuit Types (cont)

		Without Pull-Up MOS (NMOS Open Drain) or CMOS (A or C)	With Pull-Up MOS (B)	Applicable Pins
Standard Pins	I/O Common Pins			$\overline{\text{SCK}}$ (Note 2) (Output mode)
	Output Pins			SO
	Input Pins			$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$ SI $\overline{\text{SCK}}$ (Input mode)

- Notes:
1. In the stop mode, $\overline{\text{HLT}}$ signal is 0, HLT signal is 1 and I/O pins are in high impedance state.
 2. If the MCU is interrupted by serial interface in the external clock input mode, the SCK terminal becomes input only.

Table 18. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0

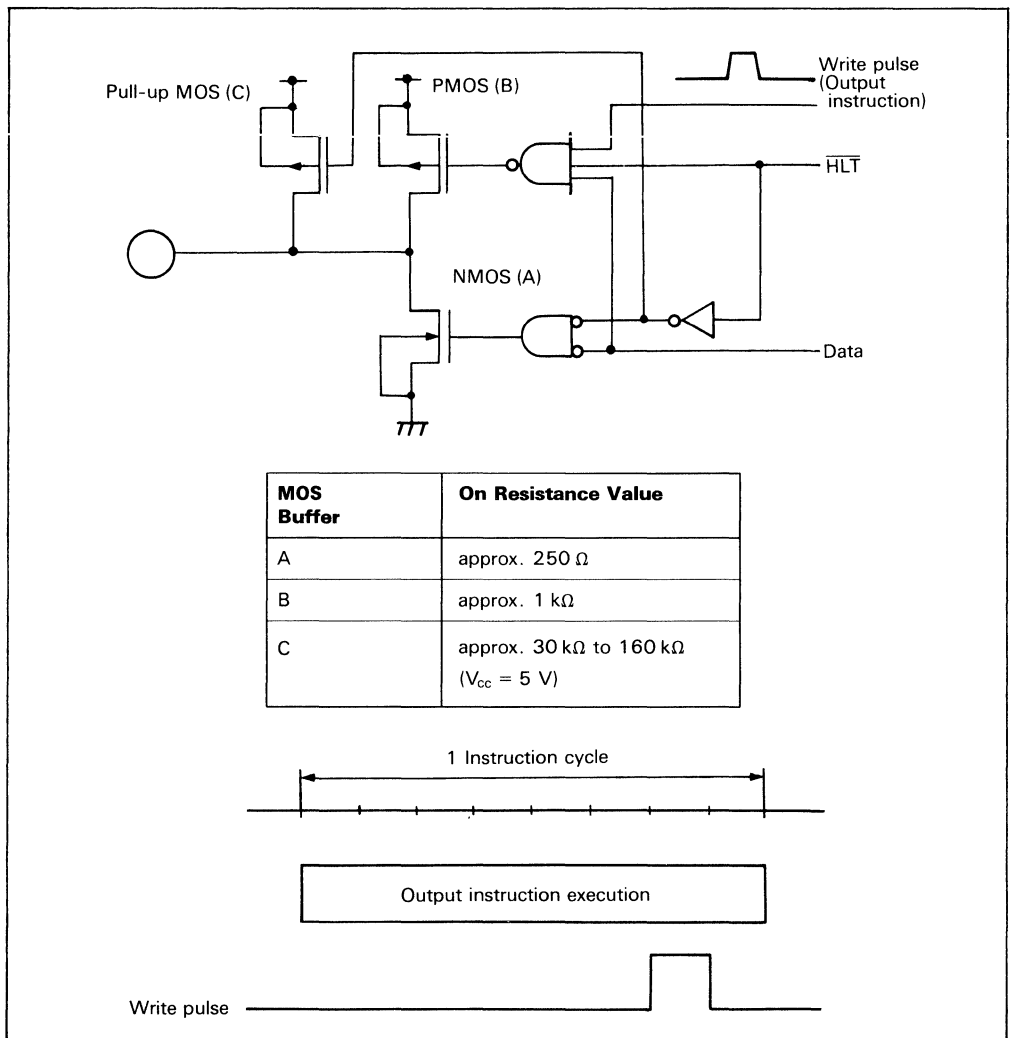


Figure 15. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two

instructions cycles are required for the MCU to be reset.

Table 19 shows the parts initialized by MCU reset, and the status of each.

Table 19. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin (A) Without Pull-Up MOS	1	Enable to input
	(B) With Pull-Up MOS	1	Enable to input
	(C) CMOS	1	—
	High-Voltage Pin (D) Without Pull-Down MOS	0	Enable to input
	(E) With Pull-Down MOS	0	Enable to input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Serial Mode Register (SMR)	0000	See serial mode register
	Timer Mode Register A (TMA)	000	See timer mode register A
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Counter A (TCA)	\$00	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—
	Octal Counter	000	—

Table 19. Initial Value After MCU Reset (cont)

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Crystal oscillator or ceramic filter oscil-

lator can be selected as the oscillator type. Refer to table 20 to select the type. In addition, see figure 17 for layout of the crystal or ceramic filter.

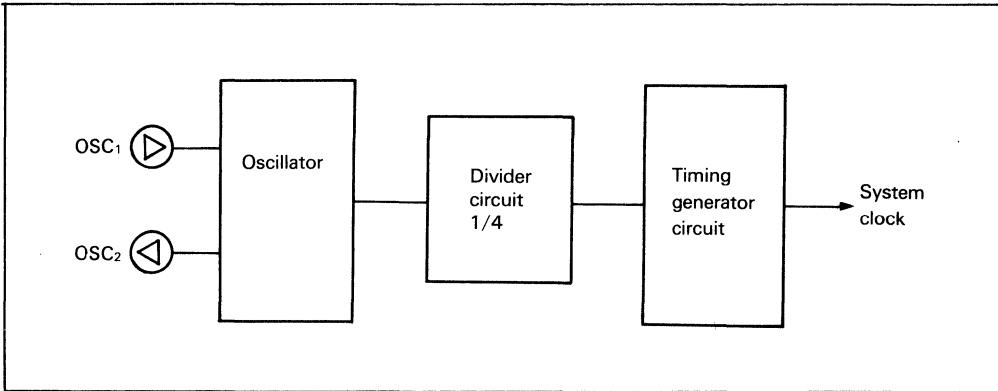


Figure 16. Internal Oscillator Circuit

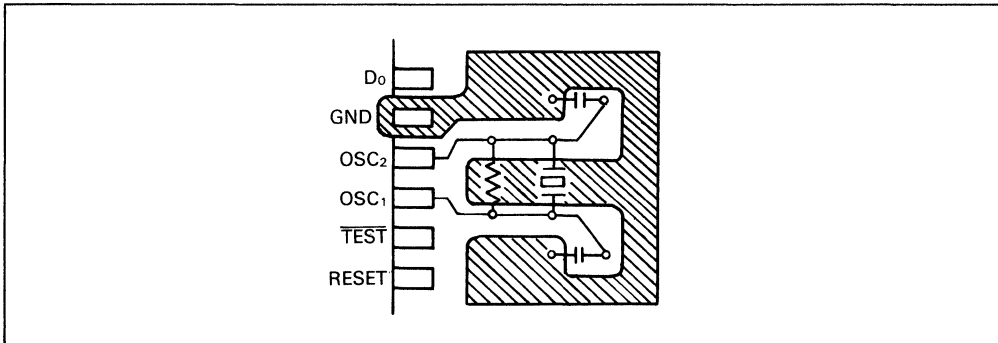
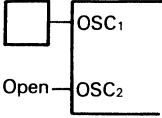
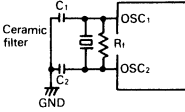
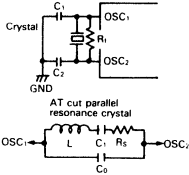


Figure 17. Layout of Crystal and Ceramic Filter

Table 20. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation	<p>Oscillator</p> 	
Ceramic Filter Oscillator		<p>Ceramic filter CSA4.00MG (Murata) R_f: 1 MΩ ± 20% C₁: 30 pF ± 20% C₂: 30 pF ± 20%</p>
Crystal Oscillator		<p>R_f: 1 MΩ ± 20% C₁: 10-22 pF ± 20% C₂: 10-22 pF ± 20% Crystal: equivalent to circuit shown C₀: 7 pF max. R₀: 100 Ω max. f: 1.0-4.5 MHz</p>

- Notes :
1. Since the circuit constants change according to the crystal and ceramic filter resonator and stray capacitance of the board, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
 2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross other wiring. Refer to figure 17.

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 21). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter and serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, flag	Retained	Reset (note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (note 2)	High impedance
Timer/counter, serial interface	Active	Stopped
Recovery method	RESET input, interrupt request	RESET input

- Notes:
1. The MCU recovers from stop mode by RESET input. Refer to table 19 for the contents of flags and registers.
 2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 19 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction

brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, reset input must be applied for at least t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry, and serial data register may not retain their contents.

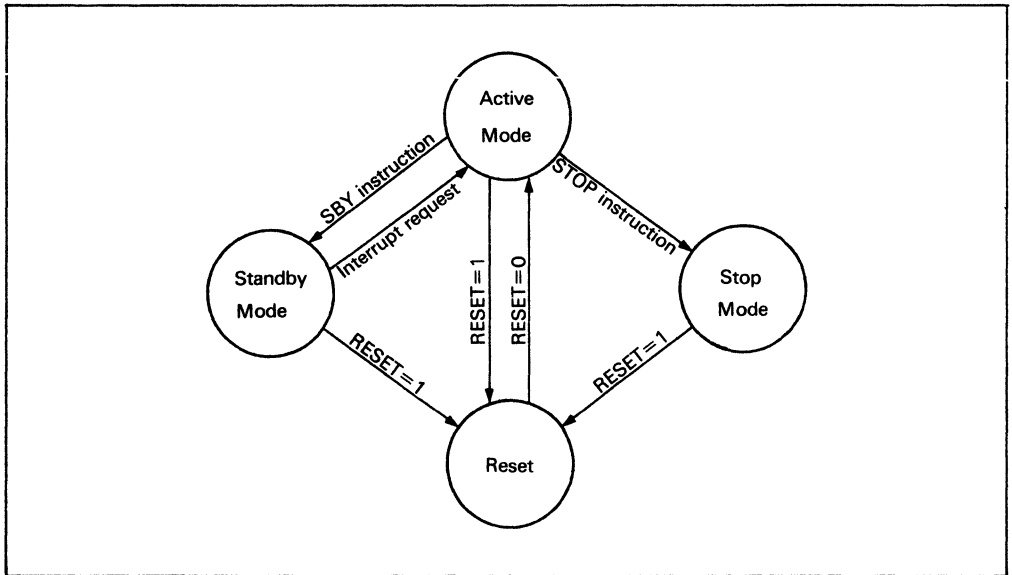


Figure 18. MCU Operation Mode Transition

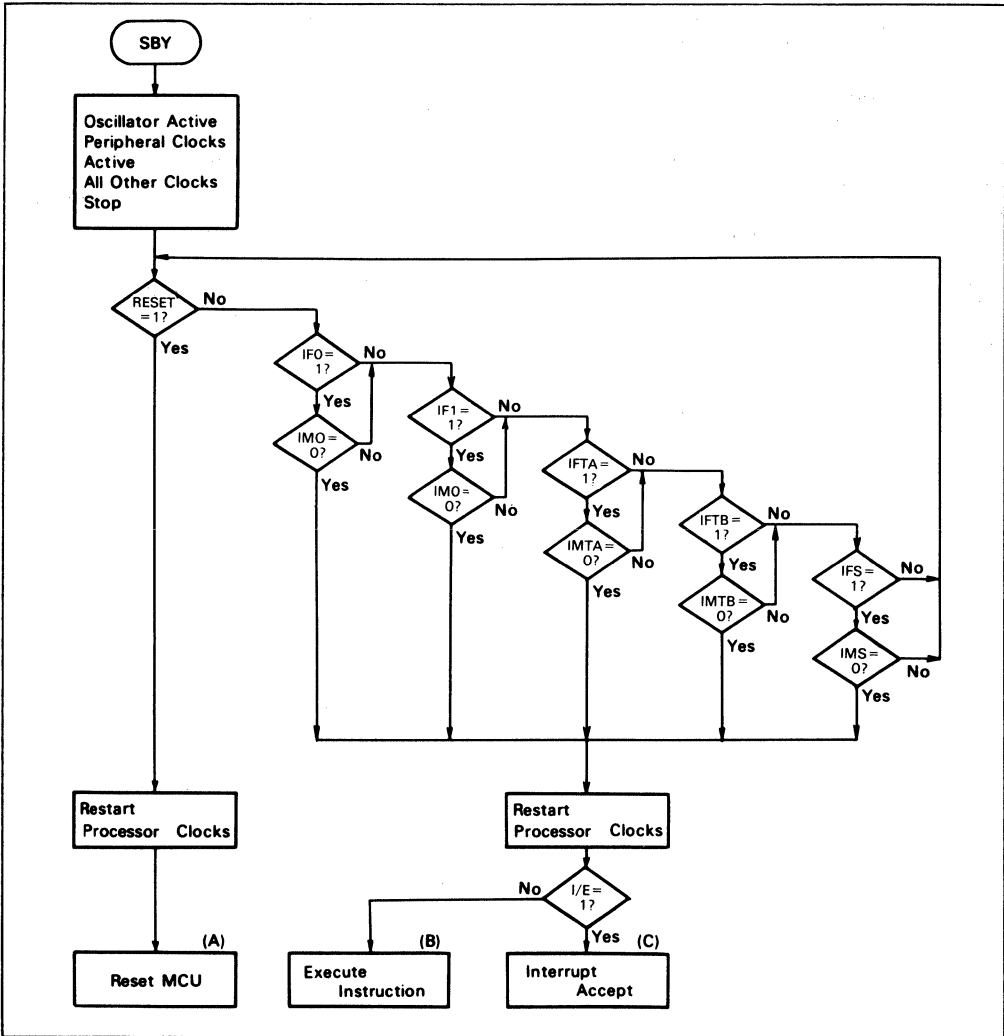


Figure 19. MCU Operating Flowchart in Standby Mode

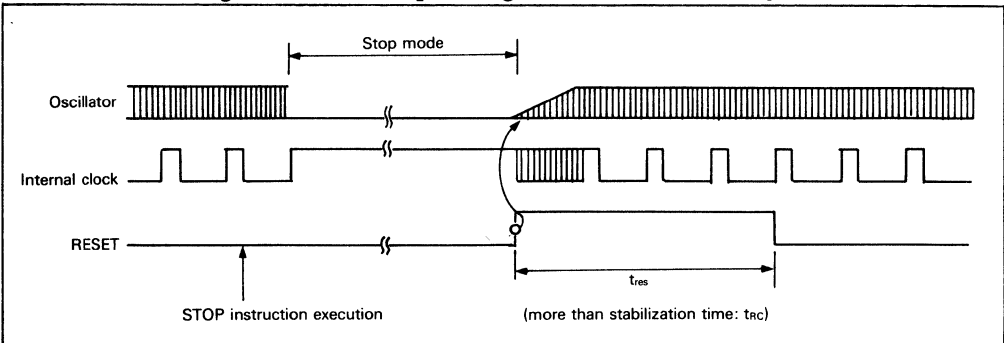


Figure 20. Timing Chart of Recovering from Stop Mode



PROM Mode Pin Description

Table 22 and figure 21 describe the pin functions in PROM mode

Table 22. PROM Mode Signals

Pin No.	MCU Mode		PROM Mode	
	DC-64S, DP-64S	FP-64B Symbol I/O	Symbol	I/O
1	59	D ₁₁ I/O	V _{CC}	
2	60	D ₁₂ I/O		
3	61	D ₁₃ I/O		
4	62	D ₁₄ I/O		
5	63	D ₁₅ I/O		
6	64	R0 ₀ I/O	A ₁	I
7	1	R0 ₁ I/O	A ₂	I
8	2	R0 ₂ I/O	A ₃	I
9	3	R0 ₃ I/O	A ₄	I
10	4	R1 ₀ I/O	A ₅	I
11	5	R1 ₁ I/O	A ₆	I
12	6	R1 ₂ I/O	A ₇	I
13	7	R1 ₃ I/O	A ₈	I
14	8	R2 ₀ I/O	A ₀	I
15	9	R2 ₁ I/O	A ₁₀	I
16	10	R2 ₂ I/O	A ₁₁	I
17	11	R2 ₃ I/O	A ₁₂	I
18	12	RA ₀ I	V _{CC}	
19	13	RA ₁ I		
20	14	R3 ₀ I/O	A ₁₃	I
21	15	R3 ₁ I/O	A ₁₄	I
22	16	R3 ₂ /INT ₀ I/O		
23	17	R3 ₃ /INT ₁ I/O		
24	18	R5 ₀ I/O		
25	19	R5 ₁ I/O		
26	20	R5 ₂ I/O		
27	21	R5 ₃ I/O		
28	22	R6 ₀ I/O		
29	23	R6 ₁ I/O		
30	24	R6 ₂ I/O		
31	25	R6 ₃ I/O		
32	26	V _{CC}	V _{CC}	

Pin No.	MCU Mode		PROM Mode	
	DC-64S, DP-64S	FP-64B Symbol I/O	Symbol	I/O
33	27	R4 ₀ /SCK I/O	O ₄	I/O
34	28	R4 ₁ /SI I/O	O ₅	I/O
35	29	R4 ₂ /SO I/O	O ₆	I/O
36	30	R4 ₃ I/O	O ₇	I/O
37	31	R7 ₀ I/O	\overline{CE}	I
38	32	R7 ₁ I/O	\overline{OE}	I
39	33	R7 ₂ I/O		
40	34	R7 ₃ I/O		
41	35	R8 ₀ I/O		
42	36	R8 ₁ I/O		
43	37	R8 ₂ I/O		
44	38	R8 ₃ I/O		
45	39	R9 ₀ I	V _{PP}	
46	40	R9 ₁ I	A ₉	I
47	41	R9 ₂ I	$\overline{M_0}$	I
48	42	R9 ₃ I	$\overline{M_1}$	I
49	43	RESET I	RESET	I
50	44	TEST I	TEST	I
51	45	OSC ₁ I		
52	46	OSC ₂ O		
53	47	GND	GND	
54	48	D ₀ I/O	O ₀	I/O
55	49	D ₁ I/O	O ₁	I/O
56	50	D ₂ I/O	O ₂	I/O
57	51	D ₃ I/O	O ₃	I/O
58	52	D ₄ I/O		
59	53	D ₅ I/O		
60	54	D ₆ I/O		
61	55	D ₇ I/O		
62	56	D ₈ I/O		
63	57	D ₉ I/O		
64	58	D ₁₀ I/O	V _{CC}	

Note: I/O: Input/Output Pins
 I: Input Pins
 O: Output Pins

HD404019/HD4074019

V_{PP} (Program Voltage): V_{PP} is the input for the program voltage (12.5 V ± 0.3 V) for programming the PROM.

CE (Chip Enable): CE input programs and verifies internal PROM.

OE (Output Enable): OE is the data output control signal for verify input.

A₀–A₁₄ (Address Bus): A₀–A₁₄ are address input pins for internal PROM.

O₀–O₇ (PROM Data Bus): O₀–O₇ are the data bus for internal PROM.

M₀, M₁ (Mode): M₀ and M₁ set PROM mode. PROM mode is set when M₀, M₁, and TEST pins are low level and RESET pin is high level.

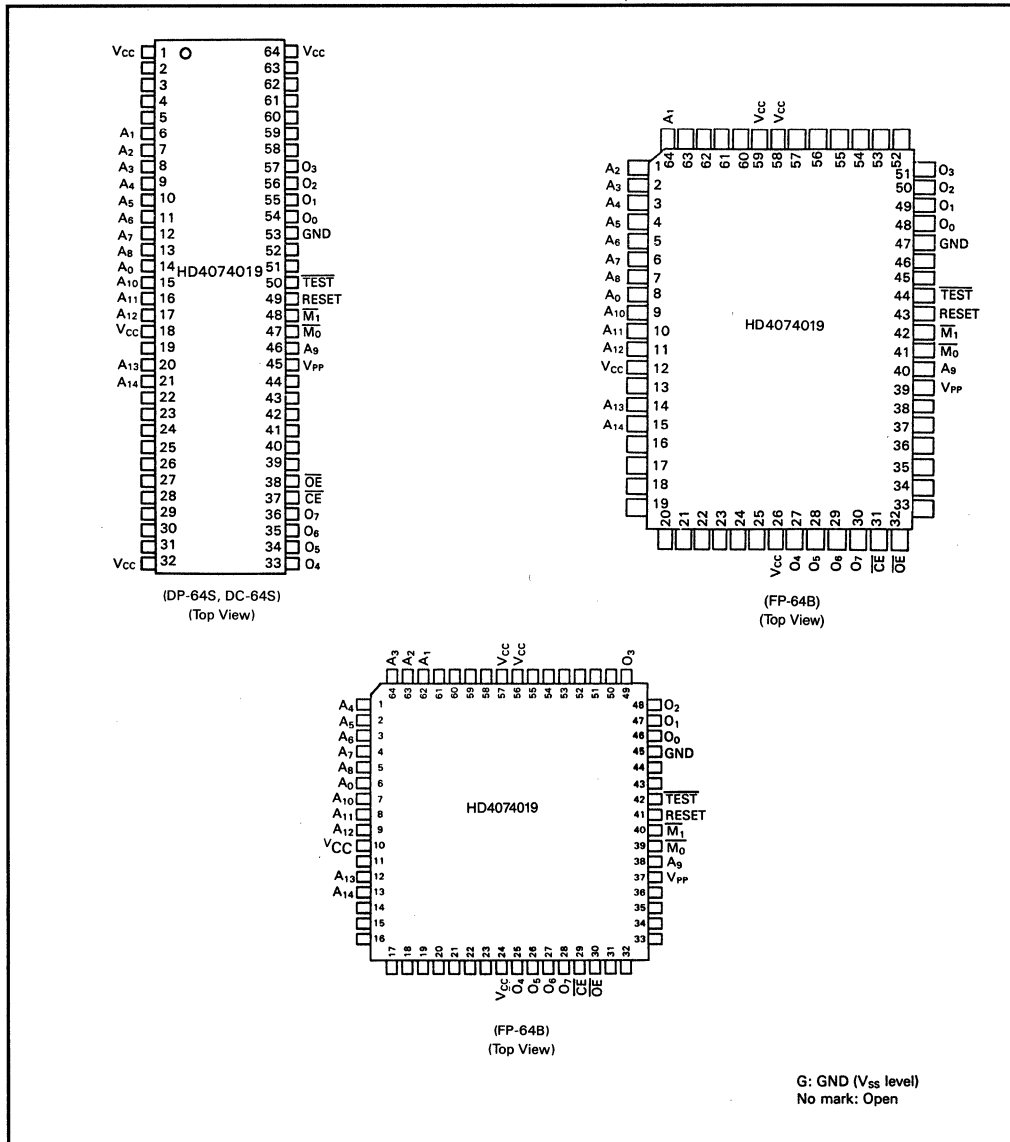


Figure 21. PROM Mode Pin Arrangement



Programmable ROM Operation

The HD4074019's on-chip PROM is programmed in PROM mode (figures 22–24). PROM mode is set by bringing TEST, M_0 , and M_1 low, and RESET high as shown in figure 22. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 24 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporate conversion circuit to use a general purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 23. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses (\$0000–\$3FFF) should be specified.

Programming And Verification

The HD4074019 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 23 shows how programming and verification modes are selected.

Figure 24 is a programming flowchart, and figure 42 is a timing chart. For precautions on PROM programming, refer to Precautions and On-Chip EPROM reliability after programming.

Erasing

PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are: ultraviolet (UV) light

with wavelength 2537\AA with a minimum irradiation of $15\text{W}\cdot\text{s}/\text{cm}^2$. These conditions are satisfied by exposing the LSI to a $12,000\ \mu\text{W}/\text{cm}^2$ UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. Addresses \$0000 to \$7FFF should be specified if the PROM is programmable by a PROM programmer. Note that the plastic package type cannot be erased and reprogrammed. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.) Data in address space beyond \$8000 must be set to \$FF.
2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with $V_{PP}=12.5\text{ V}$. Other PROMs use 21 V. If 21 V is applied to the HD4074019, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP} .

On-Chip EPROM Reliability after Programming

Generally, semiconductors are reliable except for initial failures. Parts can be screened to avoid failures. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold characteristics are high. Exposing the LSI to 150°C after user programming can effectively upgrade these characteristics. Figure 25 shows the recommended screening flow.

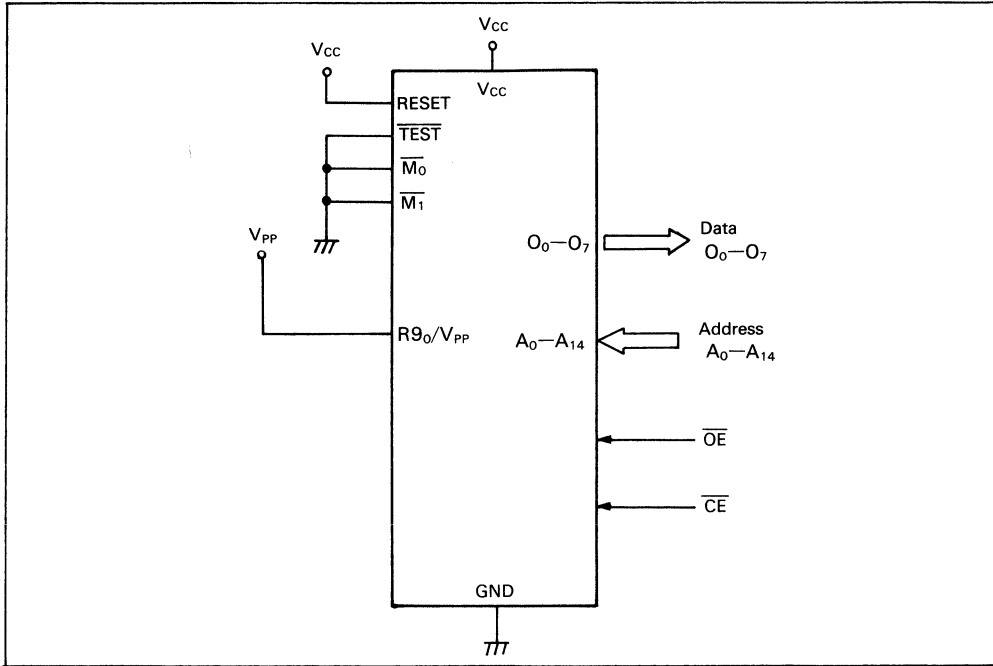


Figure 22. PROM Mode Function Diagram

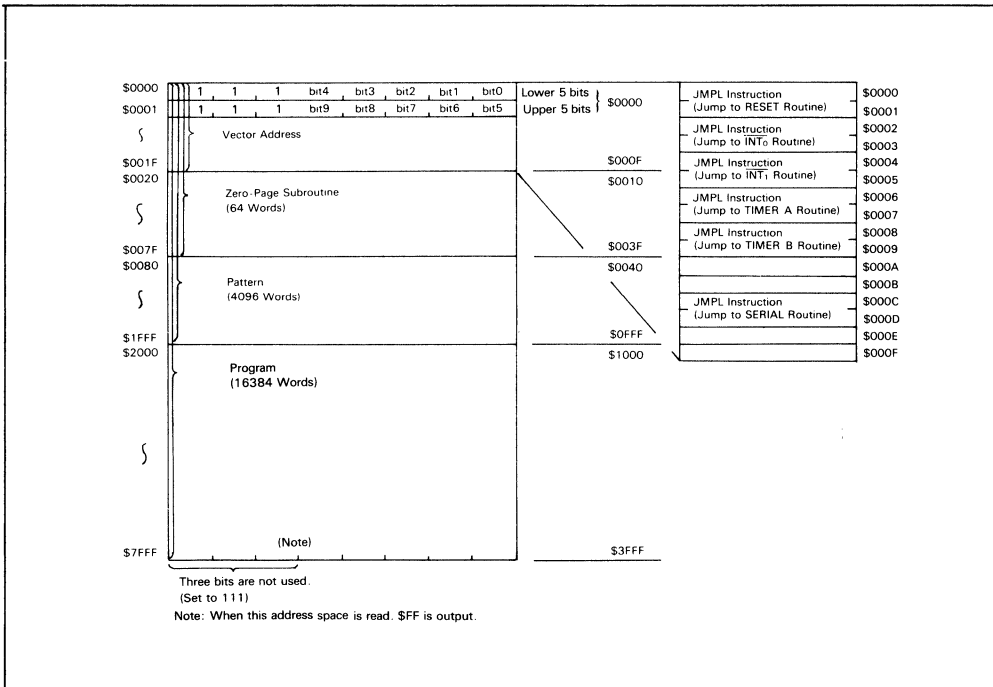


Figure 23. PROM Mode Memory Map



Table 23. PROM Mode Selection

Mode	Pin			O ₀ -O ₇
	CE	OE	V _{PP}	
Programming	Low	High	V _{PP}	Data input
Verify	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance

Table 24. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter	
Maker	Type name	Maker	Type name
DATA I/O	22B 29B	Hitachi	TBD
AVAL Corp	PKW-1000 PKW-7000	Hitachi	TBD

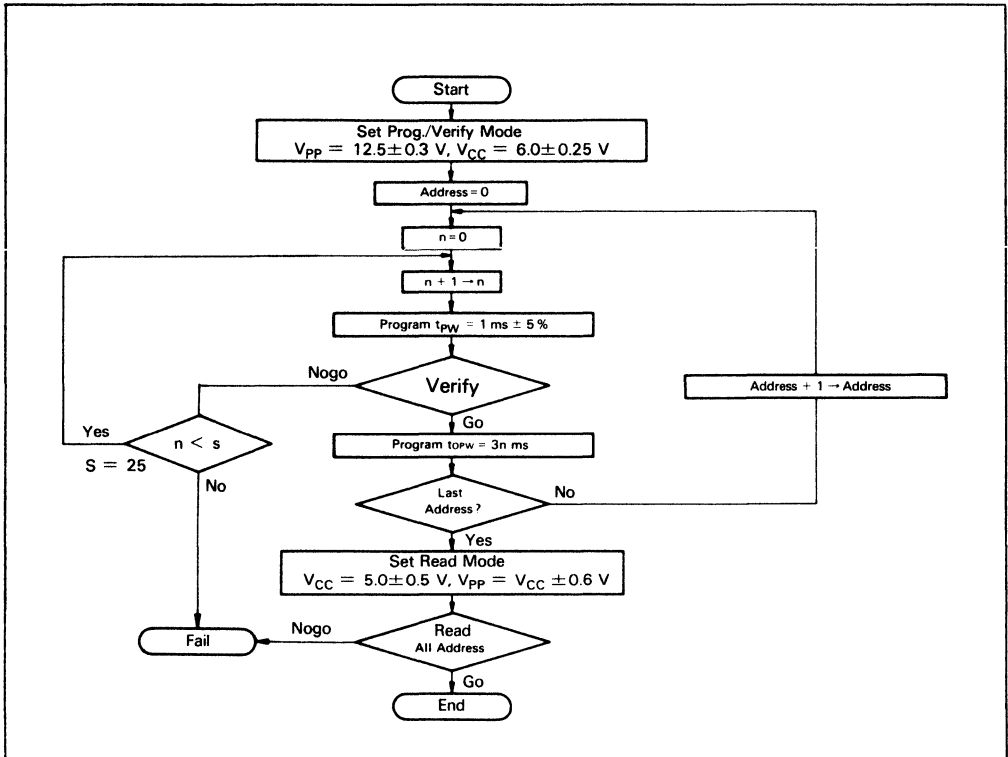


Figure 24. PROM Programming

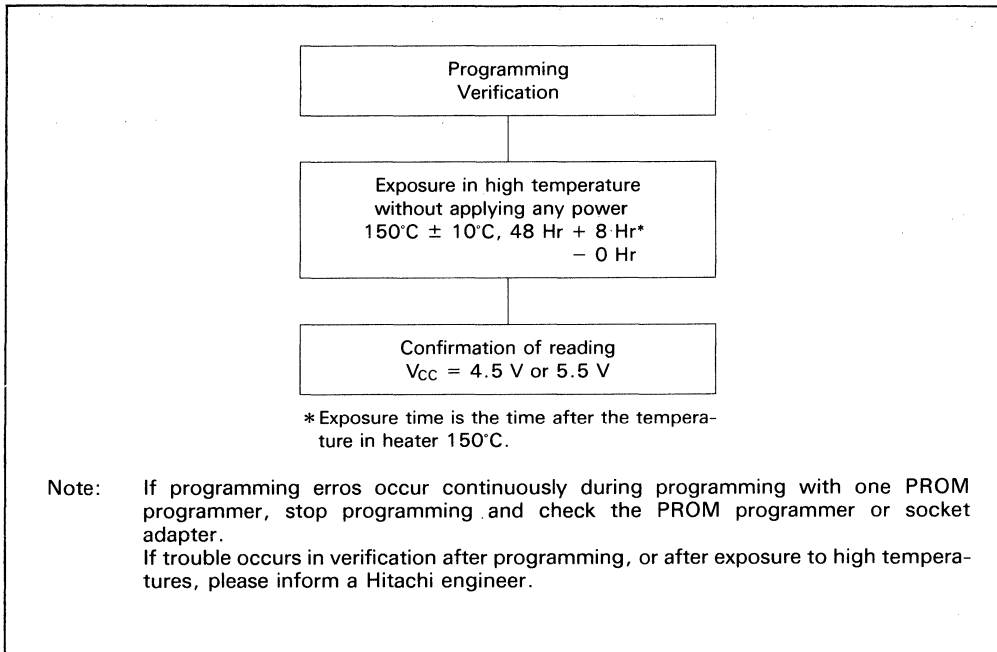


Figure 25. Recommended Screening Flow

Addressing Mode

RAM Addressing Mode

As shown in figure 26, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 27.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on a page boundary ($256n + 255$) (figure 28), executing a BR instruction transfers the PC contents to the next page, due to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 29). When bit 8 in the referenced ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

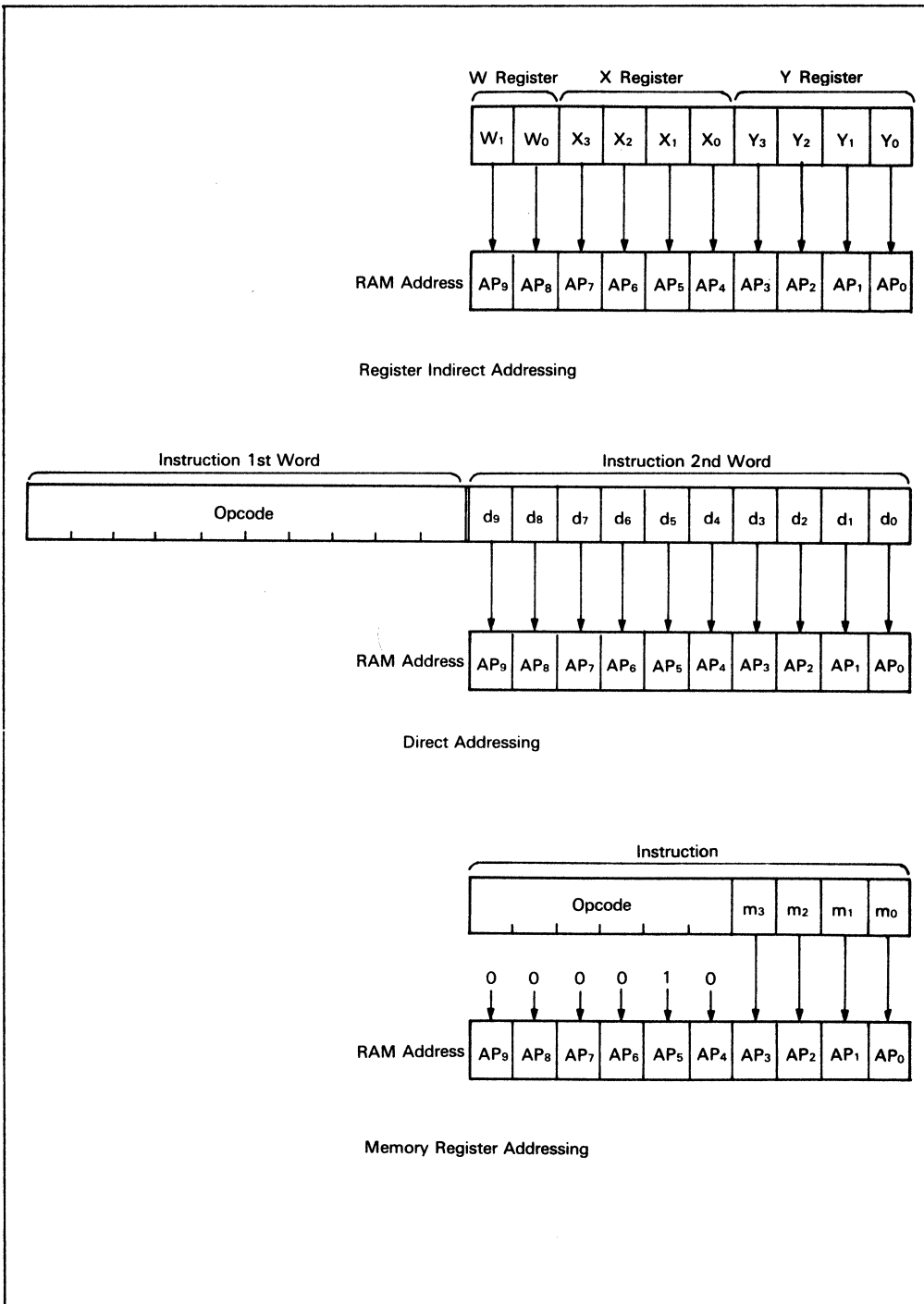


Figure 26. RAM Addressing Modes



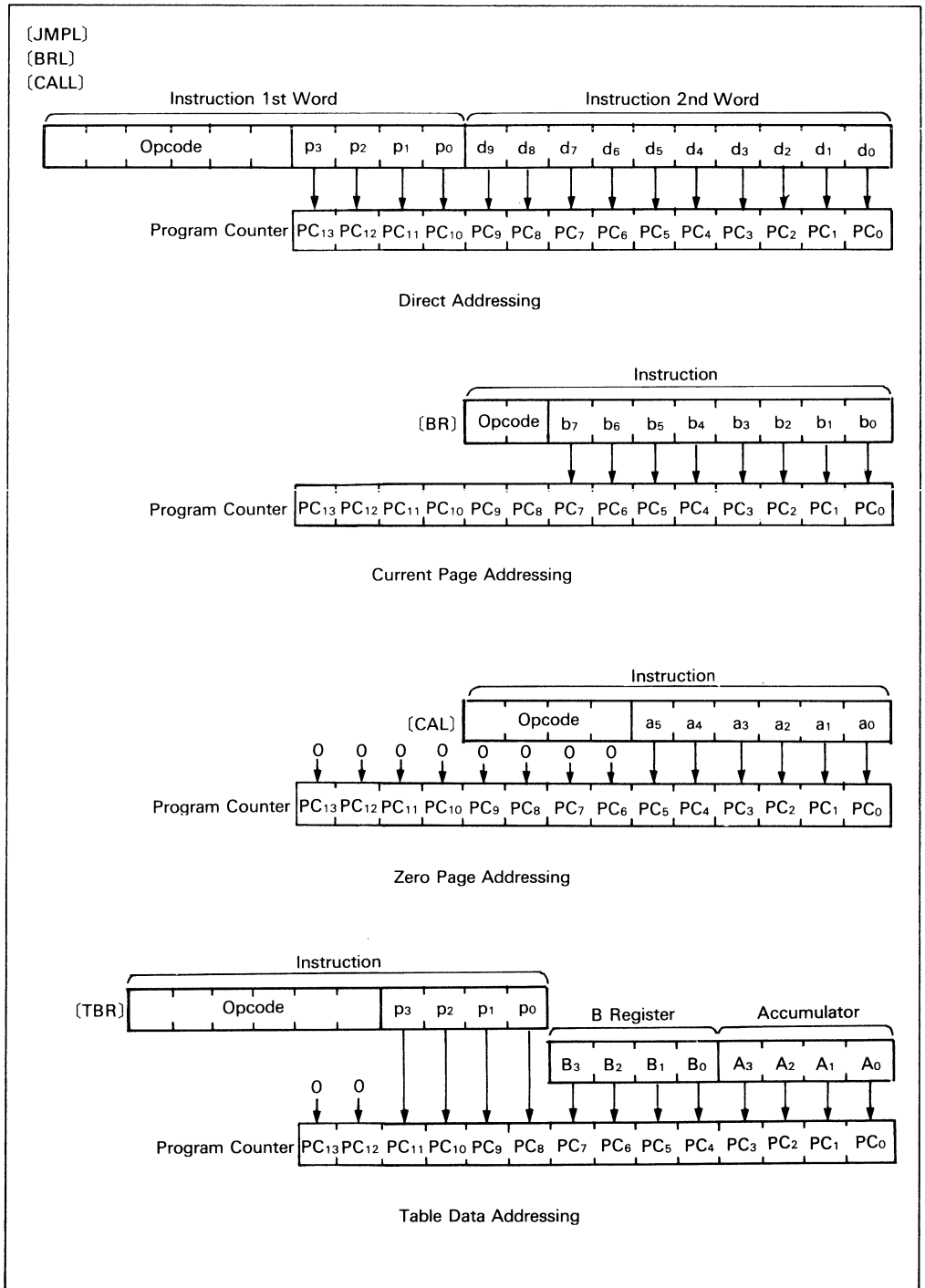


Figure 27. ROM Addressing Modes

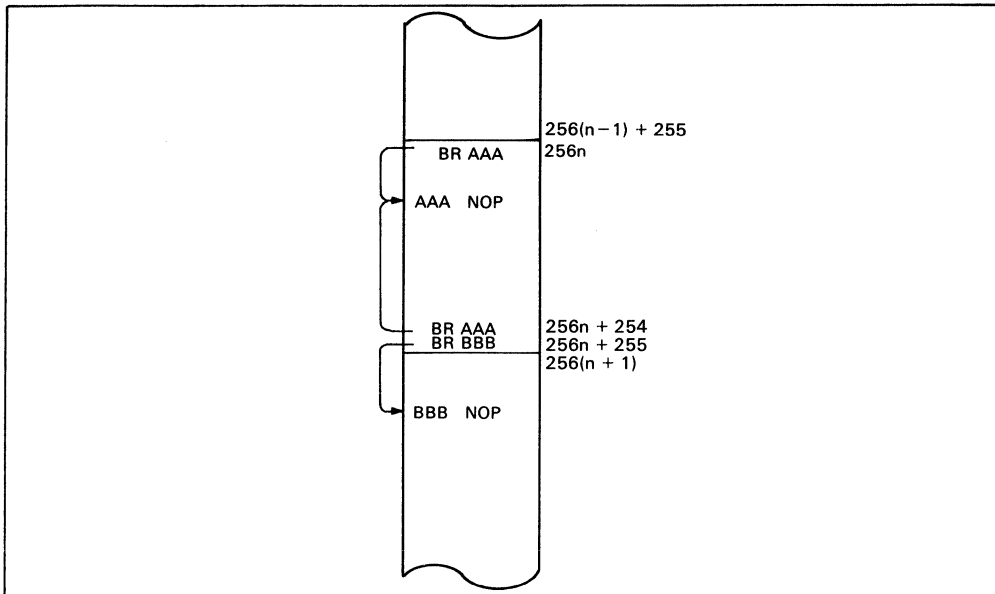


Figure 28. BR Instruction Branch Destination on Pages Boundary

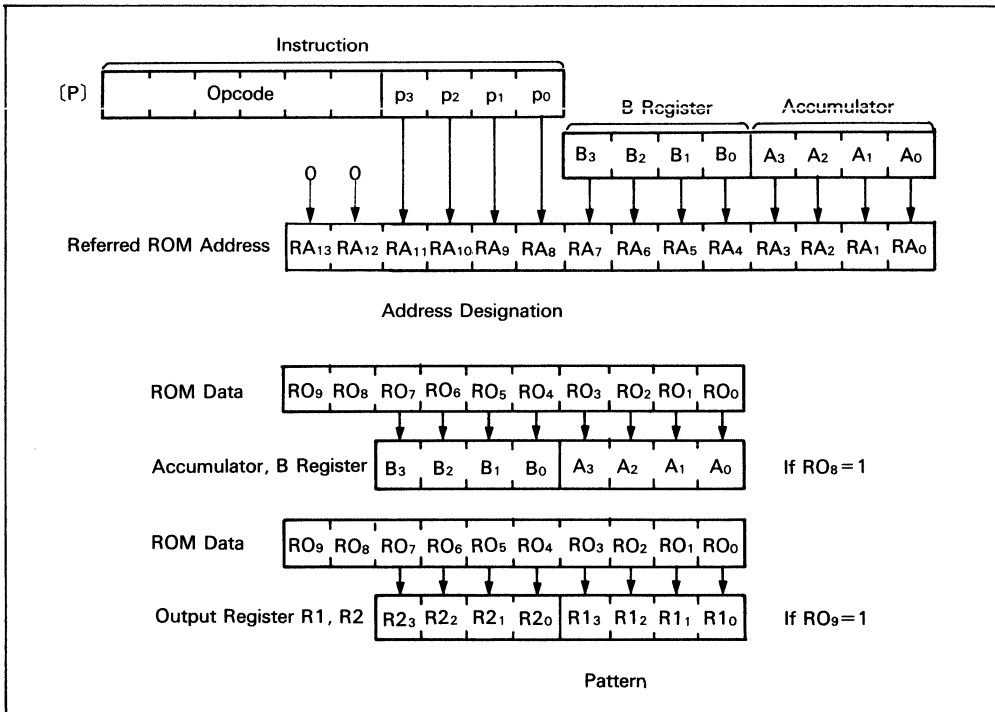


Figure 29. P Instruction



Instruction Set

The HD404019, HD4074019 provides 101 instructions which are classified into 10 groups as follows:

1. Immediate instructions
2. Register-to-register instructions
3. RAM address instructions
4. RAM register instructions
5. Arithmetic instructions

6. Compare instructions
7. RAM bit manipulation instructions
8. ROM address instructions
9. Input/output instructions
10. Control instructions

Tables 25-34 list their functions, and table 35 is an opcode map.

Table 25. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y + 1 → Y	NZ	1/1

Table 26. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.



Table 27. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 28. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M ← A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ← A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M ← B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).

The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 29. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR



Table 30. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 31. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 32. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 33. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 34. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1



Table 35. Opcode Map

R8		0																1																							
R9	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F								
	0	NOP	XSP	XSP	XSP	AN XY	EM	/	/	AM	/	/	/	ORM	/	/	LAW	/	/	/	ANEMD	/	/	AMD	/	/	/	ORND	/	/											
	1	RTN	RTN	/	/	ALEM	/	/	AMC	/	/	/	EORM	/	/	LVA	/	/	/	ALEMCD	/	/	AMCD	/	/	/	EORMD	/	/												
	2	INEM								i(4)								INEMD								i(4)															
	3	ILEM								i(4)								ILEMD								i(4)															
	4	LBM(XY)	/	ENEM	/	/	/	LAB	/	/	/	IB	/	/	COMB	/	/	OR	/	/	STS	/	/	/	SBYSTOP	/	/	/	/												
	5	LMAY(X)	/	/	AYY	/	/	LASPY	/	/	/	IY	/	/	JMPL p(4)																										
	6	NEGA	/	/	RED	/	/	LASPY	/	/	/	/	TC	CALL p(4)																											
0	7	YNEI								i(4)								BRL								p(4)															
	8	XMA(XY)	/	/	SEM n(2)	/	/	REM n(2)	/	/	/	TM n(2)	/	/	XMAD	/	/	SEMD n(2)	/	/	REMD n(2)	/	/	TMD n(2)	/	/	/	/	/												
	9	LAM(XY)	/	/	LMA(XY)	/	/	SMC	/	/	/	ANM	/	/	LAMD	/	/	LMAD	/	/	SMCD	/	/	ANMD	/	/	/	/	/												
	A	ROTR	ROTL	/	/	DAA	/	/	DAS	/	/	LAY	LMID i(4)																												
	B	TBR								p(4)								P								p(4)															
	C	XMB(XY)	/	BLEM	/	/	/	LBA	/	/	/	/	DB	CAL a(6)																											
	D	LMADY(X)	/	/	SY	/	/	LYA	/	/	/	DY																													
	E	TD	/	/	SED	/	/	LXA	/	/	REC	SEC																													
	F	LWI i(2)																																							
1	0	LBI								i(4)																															
	1	LYI								i(4)																															
	2	LXI								i(4)																															
	3	LAI								i(4)																															
	4	LBR								m(4)																															
	5	LAR								m(4)																															
	6	REDD								m(4)																															
	7	LAMR								m(4)																								BR				b(8)			
	8	AI								i(4)																															
	9	LMIIY								i(4)																															
	A	TDD								m(4)																															
	B	ALEI								i(4)																															
	C	LRB								m(4)																															
	D	LRA								m(4)																															
	E	SEDD								m(4)																															
F	XMRA								m(4)																																

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction (2-word/2-cycle)
 2-word/2-cycle Instruction



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V	
Programming Voltage	V_{PP}	- 0.3 to + 14	V	13
Terminal Voltage	V_T	- 0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 42$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	- I_O	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Total Allowance of Output Current	- ΣI_O	150	mA	6
Operating Temperature	T_{opr}	- 20 to + 75	°C	
Storage Temperature	T_{stg}	- 55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_3$ and $R3 - R8$.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $D_0 - D_3$ and $R3 - R8$.
 11. $R0 - R2$.
 12. $D_4 - D_{15}$.
 13. Applied to HD4074019.



HD4074019 Electrical Characteristics

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, \overline{SCK} , INT ₀ , INT ₁	0.8 V_{CC}	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, \overline{SCK} , INT ₀ , INT ₁	-0.3	0.2 V_{CC}	V		
		OSC ₁	-0.3	0.5	V		
		SI	-0.3	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	\overline{SCK} , SO	$V_{CC} - 1.0$		V	$-I_{OH} = 1.0\text{ mA}$	
			$V_{CC} - 0.5$		V	$-I_{OH} = 0.5\text{ mA}$	
Output Low Voltage	V_{OL}	\overline{SCK} , SO		0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , INT ₀ , INT ₁ , OSC ₁ , SI, SO		1	μA	$V_{in} = 0\text{ V to } V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		TBD	mA	$V_{CC} = 5\text{ V}$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		TBD	mA	Maximum logic operation $V_{CC} = 5\text{ V}$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		TBD	μA	$V_{in}(\overline{TEST}) = V_{CC} - 0.3\text{ V to } V_{CC}$. $V_{in}(\text{RESET}) = 0\text{ V to } 0.3\text{ V}$	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

- Notes:
1. Excluding pull-up MOS current and output buffer current.
 2. The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: V_{disp}
 3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: V_{disp}



- 4. Excluding pull-down MOS current.
- 5. When $f_{osc} = x$ MHz, estimate the current dissipation as follows:
 Max value @ x MHz = $x/4 \times$ (max value @ 4 MHz)

Input/Output Characteristics for Standard Pin

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R ₃ -R ₅ R ₉	0.7 V_{CC}	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R ₃ -R ₅ R ₉	-0.3	0.3 V_{CC}	V		
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R ₃ -R ₈		0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₃ , R ₃ -R ₈ , R ₉ ₁ -R ₉ ₃		1	μA	$V_{in} = 0\text{ V to } V_{CC}$	1
		R ₉ ₀		20	μA		

Note: 1. Pull-up MOS current and output buffer current are excluded.

Input/Output Characteristics for High Voltage Pin

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₄ -D ₁₅ , R ₀ , R ₁ , R ₂ , R _{A0} , R _{A1}	0.7 V_{CC}	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₄ -D ₁₅ , R ₀ , R ₁ , R ₂ , R _{A0} , R _{A1}	$V_{CC} - 40$	0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₄ -D ₁₅	$V_{CC} - 3.0$		V	$-I_{OH} = 15\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 2.0$		V	$-I_{OH} = 10\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 1.0$		V	$-I_{OH} = 4\text{ mA}$, $V_{CC} = 5\text{ V}$	
		R ₀ -R ₂	$V_{CC} - 3.0$		V	$-I_{OH} = 3\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 2.0$		V	$-I_{OH} = 2\text{ mA}$, $V_{CC} = 5\text{ V}$	
			$V_{CC} - 1.0$		V	$-I_{OH} = 0.8\text{ mA}$, $V_{CC} = 5\text{ V}$	
Output Low Voltage	V_{OL}	D ₄ -D ₁₅ , R ₀ -R ₂		$V_{CC} - 34$	V	150 $k\Omega$ to $V_{CC} - 40$	
Input/Output Leakage Current	$ I_{IL} $	D ₄ -D ₁₅ , R ₀ -R ₂ , R _{A0} , R _{A1}		20	μA	$V_{in} = V_{CC} - 40\text{ V}$, V_{CC}	1

Note: 1. Pull-down MOS current and output buffer current are excluded.



AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{dissp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.2	4	4.5	MHz	divide by 4	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs	divide by 4	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	divide by 4	2
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			20	ns		2
\overline{INT}_0 High Level Width	t_{i0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{i0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins except R9 ₀			30	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$	
		R9 ₀			180	pF		
RESET Fall Time	t_{RSTf}				20	ms		4

- Notes:
- Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 30)
 - See figure 31.
 - See figure 32.
 - See figure 33.



Serial Interface Timing Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{diss} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{cyc}	SCK (Output)	1		t_{cyc}		1, 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK (Output)	0.4		t_{cyc}		1, 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK (Output)		40	ns		1, 2
Transfer Clock Cycle Time	t_{cyc}	SCK (Input)	1		t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK (Input)	0.4		t_{cyc}		1
Transfer Clock END Detect High Level Width	t_{SCKHD}	SCK (Input)	1		t_{cyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK (Input)		40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO		300	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	100		ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200		ns		1

Note: 1. See figure 34
2. See figure 35



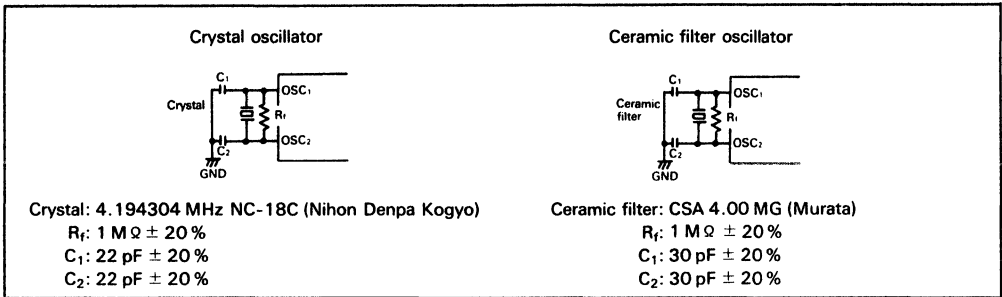


Figure 30. Oscillator Circuit

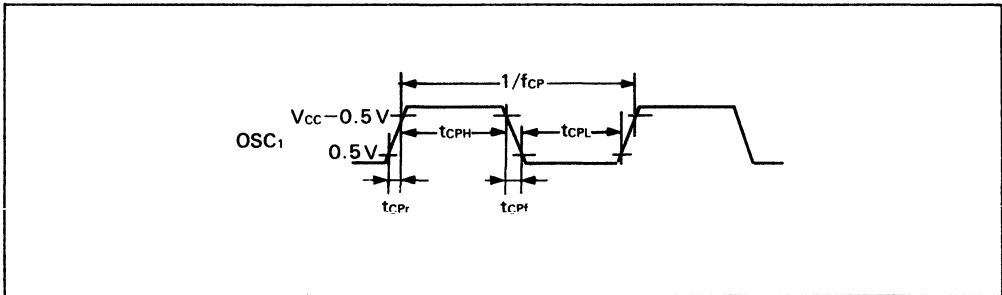


Figure 31. Oscillator Timing

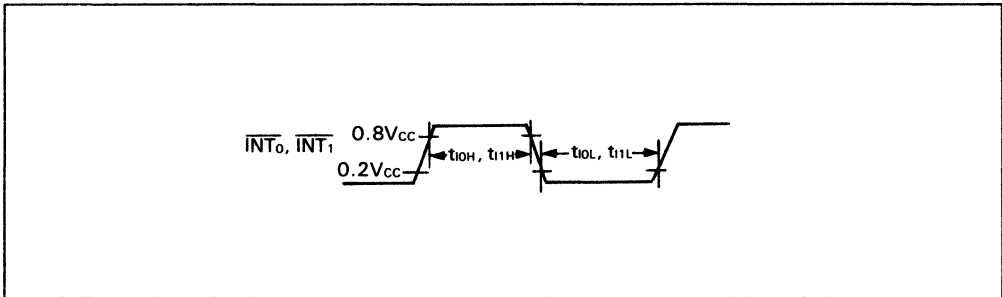


Figure 32. Interrupt Timing

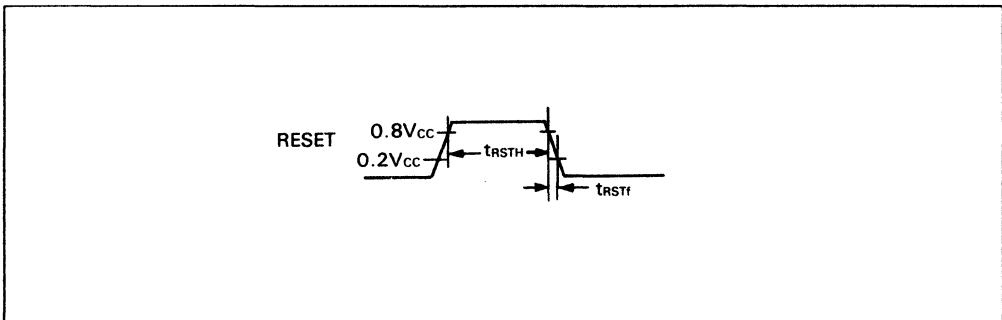


Figure 33. Reset Timing

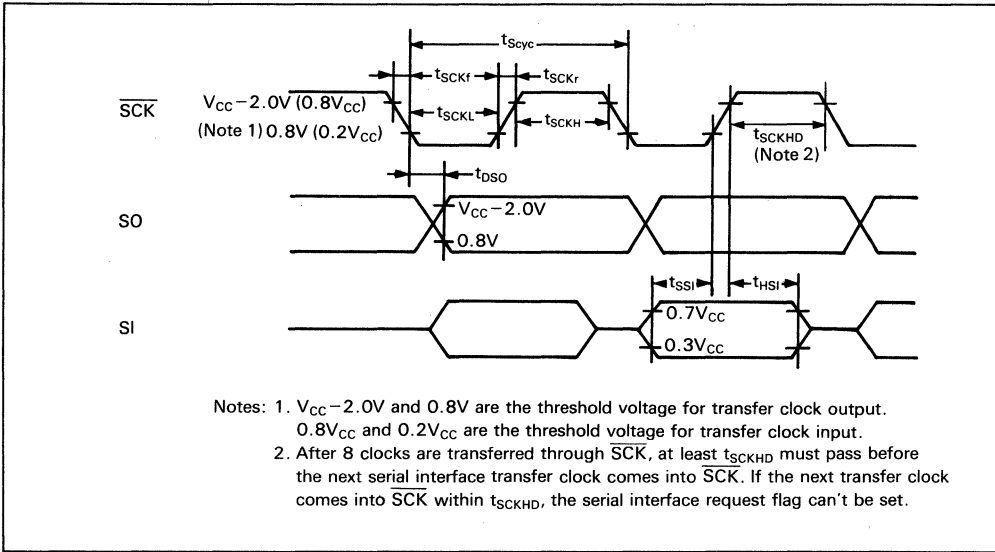


Figure 34. Timing Diagram of Serial Interface

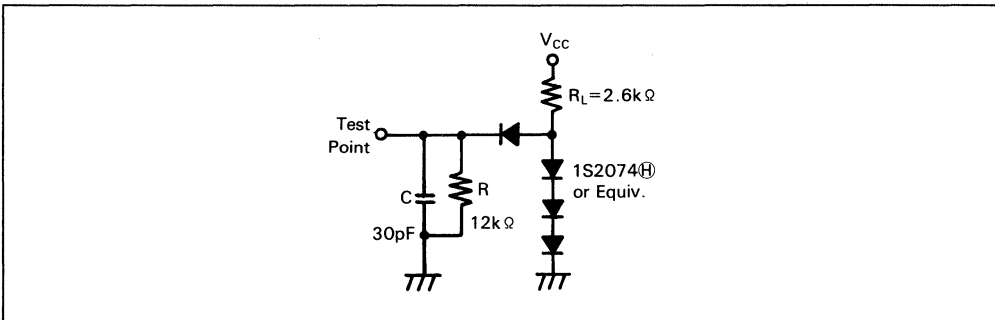


Figure 35. Timing Load Circuit

HD404019 Electrical Characteristics

DC Characteristics

($V_{CC} = 3.5\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, \overline{SCK} INT ₀ , INT ₁	$0.8V_{CC}$	$V_{CC} + 0.3$	V		
		SI	$0.7V_{CC}$	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, \overline{SCK} INT ₀ , INT ₁	-0.3	$0.2V_{CC}$	V		
		SI	-0.3	$0.3V_{CC}$	V		
		OSC ₁	-0.3	0.5	V		
Output High Voltage	V_{OH}	\overline{SCK} , SO	$V_{CC} - 1.0$		V	$- I_{OH} = 1.0\text{ mA}$	
			$V_{CC} - 0.5$		V	$- I_{OH} = 0.5\text{ mA}$	
Output Low Voltage	V_{OL}	\overline{SCK} , SO		0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} INT ₀ , INT ₁ , SI, SO, OSC ₁		1	μA	$V_{in} = 0\text{ V to }V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		TBD	mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}, \div 4$	2, 5

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Current Dissipation in Standby Mode	I _{SBY}	V _{CC}		TBD	mA	V _{CC} = 5 V; f _{osc} = 4 MHz, ÷ 4	3, 5
Current Dissipation in Stop Mode	I _{stop}	V _{CC}		TBD	μA	V _{in} (TEST) = V _{CC} - 0.3 V to V _{CC} ; V _{in} (RESET) = 0 V to 0.3 V	4
Stop Mode Retain Voltage	V _{stop}	V _{CC}	2			V	

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R₃-R₉: V_{CC}
 - D₄-D₁₅, R₀-R₂, RA₀, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When f_{osc} = x MHz, estimate the current dissipation as follows:
Max value @ x MHz = x/4 × (max value @ 4 MHz)

Input/Output Characteristics for Standard Pins

($V_{CC} = 3.5\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R3-R5, R9	$0.7V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R3-R5, R9	-0.3		$0.3V_{CC}$	V		
Output High Voltage	V_{OH}	D ₀ -D ₃ , R3-R8	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{ mA}$	1
		D ₀ -D ₃ , R3-R8	$V_{CC} - 0.5$			V	$-I_{OH} = 0.5\text{ mA}$	1
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R3-R8			0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₃ , R3-R9			1	μA	$V_{in} = 0\text{ V to }V_{CC}$	2
Pull-Up MOS Current	$-I_p$	D ₀ -D ₃ , R3-R9	TBD	TBD	TBD	μA	$V_{CC} = 5\text{ V}$, $V_{in} = 0\text{ V}$	3

- Notes:
1. Applied to I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins with pull-up MOS selected by mask option.

Input/Output Characteristics for High Voltage Pins

($V_{CC} = 3.5 \text{ V to } 6 \text{ V}$, $GND = 0 \text{ V}$, $V_{disp} = V_{CC} - 40 \text{ V to } V_{CC}$, $T_a = -20^\circ\text{C to } +75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D4-D15, R0, R1, R2, RA0, RA1	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D4-D15, R0, R1, R2, RA0, RA1	$V_{CC} - 40$		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D4-D15	$V_{CC} - 3.0$			V	$-I_{OH} = 15 \text{ mA}, V_{CC} = 5 \text{ V} \pm 20\%$	
			$V_{CC} - 2.0$			V	$-I_{OH} = 10 \text{ mA}, V_{CC} = 5 \text{ V} \pm 20\%$	
			$V_{CC} - 1.0$			V	$-I_{OH} = 4 \text{ mA}$	
		R0-R2	$V_{CC} - 3.0$			V	$-I_{OH} = 3 \text{ mA}, V_{CC} = 5 \text{ V} \pm 20\%$	
			$V_{CC} - 2.0$			V	$-I_{OH} = 2 \text{ mA}, V_{CC} = 5 \text{ V} \pm 20\%$	
			$V_{CC} - 1.0$			V	$-I_{OH} = 0.8 \text{ mA}$	
Output Low Voltage	V_{OL}	D4-D15, R0-R2			$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40 \text{ V}$	1
		D4-D15, R0-R2			$V_{CC} - 37$	V	$150 \text{ k}\Omega \text{ to } V_{CC} - 40 \text{ V}$	2
Input/Output Leakage Current	$ I_{IL} $	D4-D15, R0-R2, RA0, RA1			20	μA	$V_{in} = V_{CC} - 40 \text{ V to } V_{CC}$	3
Pull-Down MOS Current	I_d	D4-D15, R0-R2, RA0, RA1	TBD	TBD	TBD	μA	$V_{disp} = V_{CC} - 35 \text{ V},$ $V_{in} = V_{CC}$	4

- Notes:
1. Applied to I/O pins with pull-down MOS selected by mask option.
 2. Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. Applied to I/O pins with pull-down MOS selected by mask option.

AC Characteristics

($V_{CC} = 3.5\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.2	4	4.5	MHz	divide by 4	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs		
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	divide by 4	2
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CPl}	OSC ₁			20	ns		2
\overline{INT}_0 High Level Width	t_{i0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{i0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			30	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms		4

- Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (3.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 36)
 2. See figure 37.
 3. See figure 38.
 4. See figure 39.



Serial Interface Timing Characteristics

($V_{CC} = 3.5\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK} (Output)	1		t_{cyc}		1, 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	\overline{SCK} (Output)	0.4		t_{cyc}		1, 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	\overline{SCK} (Output)		40	ns		1, 2
Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK} (Input)	1		t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	\overline{SCK} (Input)	0.4		t_{cyc}		1
Transfer Clock END Detect High Level Width	t_{SCKHD}	\overline{SCK} (Input)	1		t_{cyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	\overline{SCK} (Input)		40	ns		1
Serial Output Data Delay Time	t_{DSO}	SO		300	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	100		ns		1
Serial Input Data Hold Time	t_{HSI}	SI	200		ns		1

Notes: 1. See figure 40.
2. See figure 41.



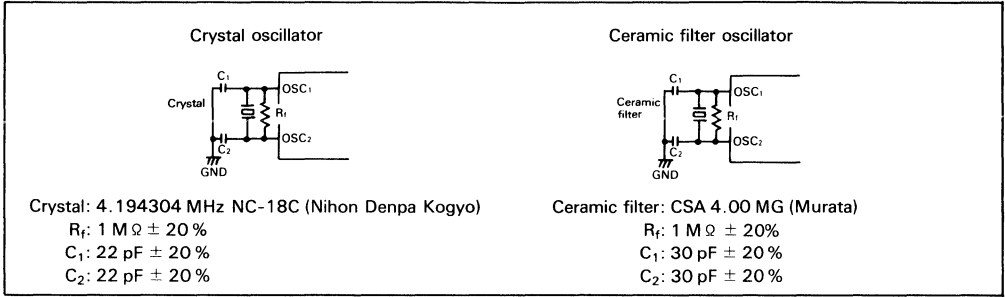


Figure 36. Oscillator Circuit

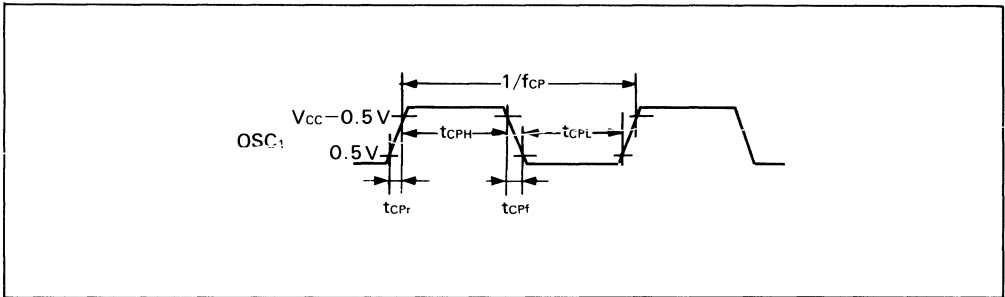


Figure 37. Oscillator Timing

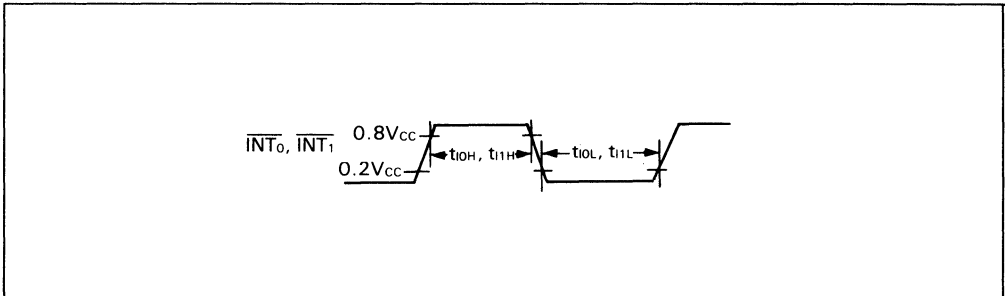


Figure 38. Interrupt Timing

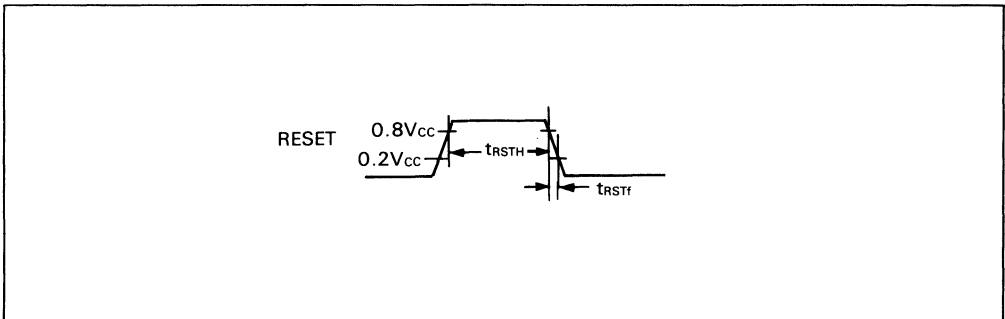


Figure 39. Reset Timing

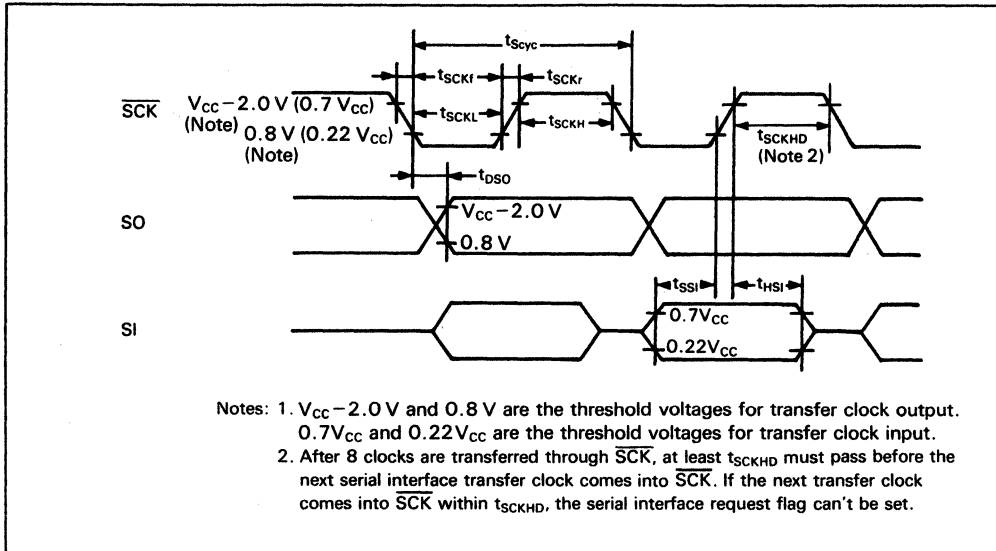


Figure 40. Timing Diagram of Serial Interface

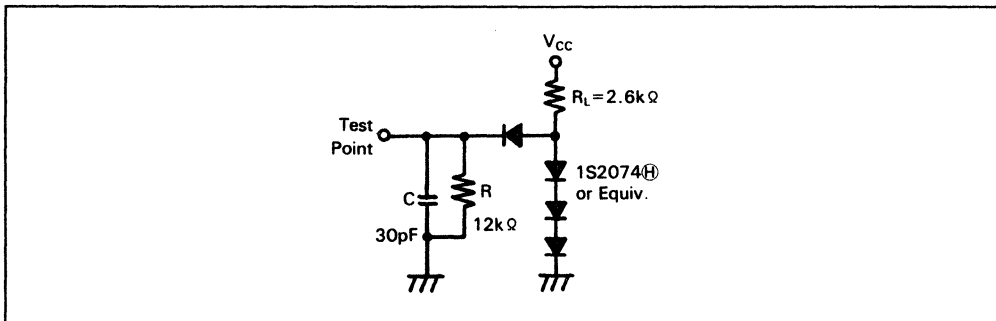


Figure 41. Timing Load Circuit

**Programming Electrical Characteristics for HD4074019
Write and Verify Mode**

DC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		$V_{CC} + 0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\ \mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{ V}/0.5\text{ V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time		t_{AS}	2			μs	Fig. 42
\overline{OE} set-up time		t_{OES}	2			μs	Input Pulse level: 0.8–2.2 V
Data set-up time		t_{DS}	2			μs	Input rise/fall time $\leq 20\text{ ns}$
Address hold time		t_{AH}	0			μs	Timing reference level
Data hold time		t_{DH}	2			μs	{ input: 1.0 V, 2.0 V output: 0.8 V, 2.0 V
Output disable delay time		t_{DF}			130	ns	
V_{PP} set-up time		t_{VPS}	2			μs	
Program pulse width		t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming		t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time		t_{VCS}	2			μs	
Data output delay time		t_{OE}	0		500	ns	

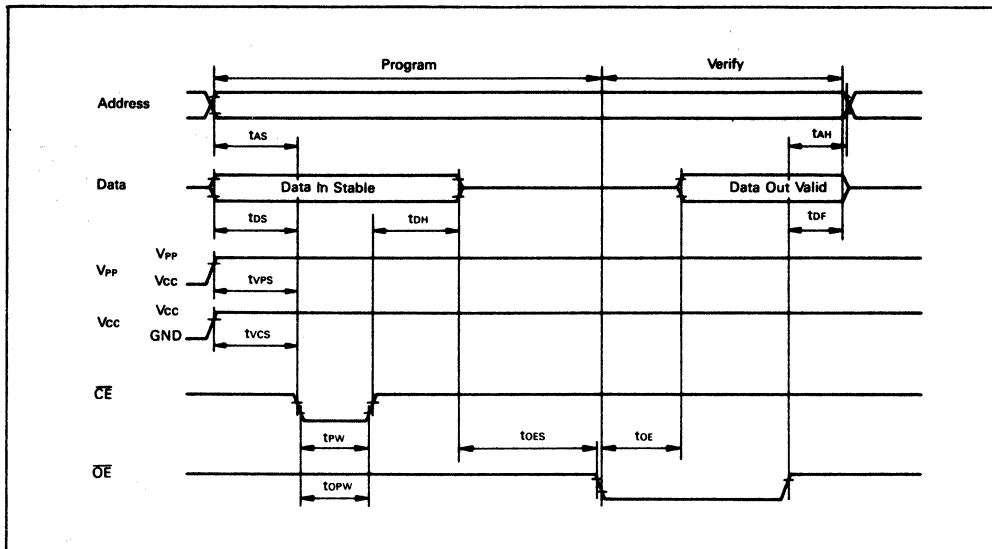


Figure 42. PROM Programming/Verify Timing

Read Mode

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Leakage Current	I_{LI}			1	μA	$V_{CC} = 5.5\text{ V}$, $V_{in} = \text{GND to } V_{CC}$
Output Leakage Current	I_{LO}			1	μA	$V_{CC} = 5.5\text{ V}$, $V_{out} = \text{GND to } V_{CC}$
Program Current	I_{PP}		1	100	μA	$V_{PP} = V_{CC} + 0.6\text{ V}$
Current Dissipation Active Mode	I_{CC}			30	mA	
Input Voltage	V_{IL}	-0.3		0.8	V	
	V_{IH}	2.2		$V_{CC} + 0.3$	V	
Output Voltage	V_{OL}			0.40	V	$I_{OL} = 1.6\text{ mA}$
	V_{OH}	2.4			V	$I_{OH} = -200\ \mu\text{A}$

AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $V_{PP} = V_{CC} \pm 0.6\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Min	Max	Unit	Test Condition	Note
Access Time	t_{ACC}		500	ns	$\overline{CE} = \overline{OE} = V_{IL}$	
\overline{CE} Output Delay Time	t_{CE}		500	ns	$\overline{OE} = V_{IL}$	
\overline{OE} Output Delay Time	t_{OE}	10	150	ns	$\overline{CE} = V_{IL}$	
Output Disable Delay Time	t_{DF}	0	105	ns	$\overline{CE} = V_{IL}$	1
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$	

Note: 1. t_{DF} is defined when output becomes open because output level cannot be defined.

Switching characteristics

Input Pulse Level 0.8 to 2.2 V

Input Rise/Fall Time ≤ 20 ns

Output Load 1TTL Gate + 100 pF

Input/Output Timing Reference Level Output: 1 V, 2 V

Input: 0.8 V, 2 V

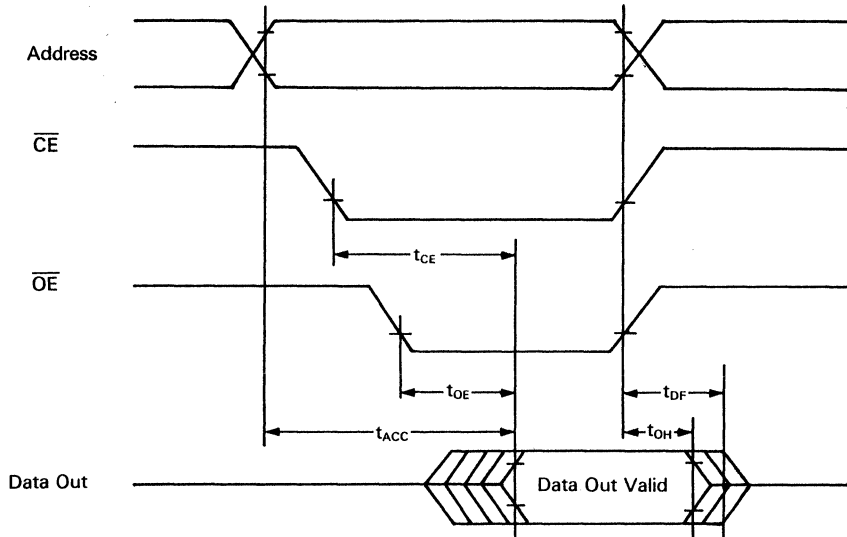


Figure 44. PROM Read Timing

HD404019
MASK OPTION LIST

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

* Please enter check marks in
(■, x, ✓).

(1) I/O Option

Note (I/O options masked by are not available.)

PIN	INPUT/OUTPUT	I/O OPTION					PIN	INPUT/OUTPUT	I/O OPTION					
		A	B	C	D	E			A	B	C	D	E	
D ₀	Standard Pins Input/Output				■	■	R3 ₀	Input/Output				■	■	
D ₁		Input/Output				■	R3 ₁	Input/Output				■	■	
D ₂		Input/Output				■	R3 ₂	Input/Output				■	■	
D ₃		Input/Output				■	R3 ₃	Input/Output				■	■	
D ₄	High Voltage Pins Input/Output	■	■	■			R4 ₀	Input/Output				■	■	
D ₅		Input/Output	■	■	■			R4 ₁	Input/Output				■	■
D ₆		Input/Output	■	■	■			R4 ₂	Input/Output				■	■
D ₇		Input/Output	■	■	■			R4 ₃	Input/Output				■	■
D ₈		Input/Output	■	■	■			R5 ₀	Input/Output				■	■
D ₉		Input/Output	■	■	■			R5 ₁	Input/Output				■	■
D ₁₀		Input/Output	■	■	■			R5 ₂	Input/Output				■	■
D ₁₁		Input/Output	■	■	■			R5 ₃	Input/Output				■	■
D ₁₂		Input/Output	■	■	■			R6 ₀	Input/Output				■	■
D ₁₃		Input/Output	■	■	■			R6 ₁	Input/Output				■	■
D ₁₄		Input/Output	■	■	■			R6 ₂	Input/Output				■	■
D ₁₅		Input/output	■	■	■			R6 ₃	Input/Output				■	■
							R7 ₀	Input/Output				■	■	
							R7 ₁	Input/Output				■	■	
							R7 ₂	Input/Output				■	■	
							R7 ₃	Input/Output				■	■	
R0	RO ₀	Input/Output	■	■	■		R8 ₀	Input/Output				■	■	
	RO ₁	Input/Output	■	■	■		R8 ₁	Input/Output				■	■	
	RO ₂	Input/Output	■	■	■		R8 ₂	Input/Output				■	■	
	RO ₃	Input/Output	■	■	■		R8 ₃	Input/Output				■	■	
R1	R1 ₀	Input/Output	■	■	■		R9 ₀	Input				■	■	
	R1 ₁	Input/Output	■	■	■		R9 ₁	Input				■	■	
	R1 ₂	Input/Output	■	■	■		R9 ₂	Input				■	■	
	R1 ₃	Input/Output	■	■	■		R9 ₃	Input				■	■	
R2	R2 ₀	Input/Output	■	■	■		RA ₀	Input	■	■	■			
	R2 ₁	Input/Output	■	■	■		RA ₁	Input	■	■	■			
	R2 ₂	Input/Output	■	■	■		Please Mark on RA ₁ /V _{disp}							
	R2 ₃	Input/Output	■	■	■									

* Please enter "0" in applicable item for I/O option selection.
 A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
 C: CMOS (not be used as Input) D: Without Pull-down MOS (PMOS Open Drain)
 E: With Pull-down MOS



HD404019/HD4074019

(2) RA₁/V_{disp}

RA ₁ /V _{disp}	
<input type="checkbox"/>	RA ₁ : Without Pull-down MOS (D)
<input type="checkbox"/>	V _{disp}

* Please enter check marks (■, X, ✓) in applicable item.

(3) Package

Package	
<input type="checkbox"/>	DP-64S (shrink package)
<input type="checkbox"/>	FP-64B

* Please enter check marks (■, X, ✓) in applicable item.

Note) RA₁/V_{disp} has to be selected as V_{disp} pin even if one high voltage pin is specified as "E".

(4) Divider (DIV)

Clock divide ratio	
<input checked="" type="checkbox"/>	Divided-by-4

Check List of Application	
---------------------------	--

(5) ROM Code Media

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

(A) Oscillator (CPG option)

CPG option	
<input type="checkbox"/>	Ceramic Filter
<input type="checkbox"/>	Crystal
<input type="checkbox"/>	External Clock

* Please enter check marks (■, X, ✓) in applicable item.



HD614P080S/HD614P0160S

DESCRIPTION

The HD614P080S and HD614P0160S are 4-bit single chip microcomputers which have mounted a standard EPROM 2764/27128/27256 for program memory.

The HD614P080S and HD614P0160S are pin-compatible with the mask ROM type HMCS402/404/408, but have some differences with them as shown in Table 33. By modifying the program in the EPROM, they can be used for the evaluation of the HMCS402/404/408, or for small-scale production.

HARDWARE FEATURES

- 4-bit Architecture
- Application to 4k, 8k or 16k words x 10 bits of EPROM
 - 4096 words x 10 bits HN482764, HN27C64
 - 8192 words x 10 bits HN4827128
 - 16384 words x 10 bits HN27C256
- Data Memory (RAM) Capacity 576 digits x 4 bits
- 58 I/O Pins — 26 I/O pins are high voltage up to 40V (max).
- 2 Timer/Counters
 - 11-bit Prescaler
 - 8-bit Free Running Counter
 - 8-bit Auto-reload Timer/Event Counter
- Clocked Synchronous 8-bit Serial Interface
- 5 Interrupts
 - External 2
 - Timer/Counter 2
 - Serial Interface 1
- Subroutine Stack
 - Up to 16 levels including interrupts
- Minimum Instruction Execution Time; 1.33 μ s
- 2 Low Power Modes
 - Standby — Stops instruction execution while keeping clock generator and interrupt functions included Timer/Counter and Serial Interface in operation
 - Stop — Stops instruction execution and clock generation while retaining RAM data
- Clock Generator
 - External Connection of Crystal Resonator or Ceramic Filter Resonator (externally drivable)
- Power Voltage Range; 5V \pm 10%
- I/O Pin Circuit Form
 - All standard pins are "without pull-up MOS".
 - All high voltage pins are "without pull-down MOS".
- Shrink Type 64 Pin EPROM On-package

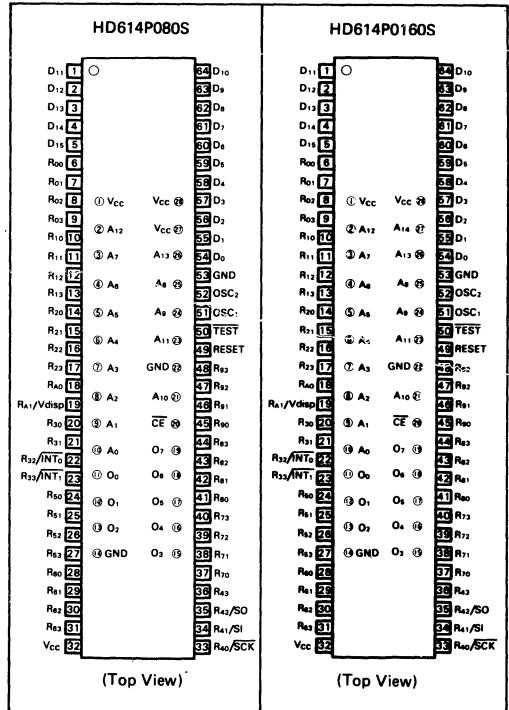
SOFTWARE FEATURES

- Software Compatible with HMCS402/404/408
- Instruction Set Similar to and More Powerful than HMCS40 Series; 99 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 79 instructions are single word instructions.
 - Direct Branch to All ROM Area
 - Direct or Indirect Addressing to All RAM Area
 - Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logic Arithmetic Operation
- Pattern Generation — Table Look Up Capability —
- Bit Manipulation for Both RAM and I/O

PROGRAM DEVELOPMENT SUPPORT TOOLS

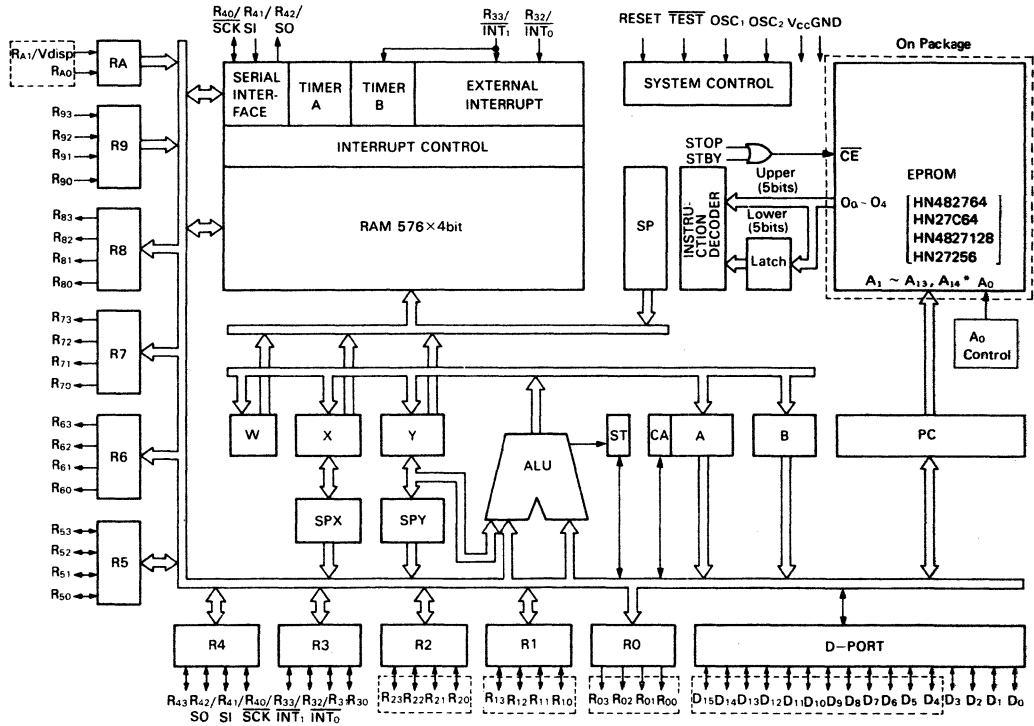
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

PIN ARRANGEMENT



RECOMMENDED APPLICABLE EPROM

Type No.	Program Memory Capacity	f _{osc} (MHz)	EPROM Type No.
HD614P080S	4096 words	4	HN27C64-30 HN482764-3
		6	HN27C64-25 HN482764
HD614P0160S	8192 words	4	HN4827128-45
		6	HN4827128-25
HD614P0160S	16384 words	4	HN27C256-30
		6	HN27C256-25



High Voltage Pins

*A₁₄ is available only to the HD614P0160S.



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" of the LSI or the EPROM are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.

(Note 2) All voltages are with respect to GND.

(Note 3) Applied to standard pins.

(Note 4) Applied to high voltage I/O pins.

(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.

(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.

(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.

(Note 8) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.

(Note 10) Applied to $D_0 \sim D_3$ and $R3 \sim R8$.

(Note 11) Applied to $R0 \sim R2$.

(Note 12) Applied to $D_4 \sim D_{15}$.

HD614P080S/HD614P0160S

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{CC} = 4.5V$ to $5.5V$, $GND = 0V$, $T_a = -20$ to $+75^{\circ}C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Input "High" Voltage	V_{IH}	RESET, SCK, INT ₀ , INT ₁		$0.7V_{CC}$	—	$V_{CC}+0.3$	V		
		SI		$0.7V_{CC}$	—	$V_{CC}+0.3$	V		
		OSC ₁		$V_{CC}-0.5$	—	$V_{CC}+0.3$	V		
Input "Low" Voltage	V_{IL}	RESET, SCK, INT ₀ , INT ₁		-0.3	—	$0.22V_{CC}$	V		
		SI		-0.3	—	$0.22V_{CC}$	V		
		OSC ₁		-0.3	—	0.5	V		
Output "High" Voltage	V_{OH}	SCK, SO	$-I_{OH} = 1.0$ mA	$V_{CC}-1.0$	—	—	V		
			$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	—	—	V		
Output "Low" Voltage	V_{OL}	SCK, SO	$I_{OL} = 1.6$ mA	—	—	0.4	V		
Input/Output Leakage Current	$ I_{IL} $	RESET, SCK, INT ₀ , INT ₁ , SI, SO, OSC ₁	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	1	
Current Dissipation in Operation Mode	I_{CC}	V_{CC}	$V_{CC} = 5V$	Crystal or Ceramic Filter Resonator $f_{osc} = 4MHz$	—	—	2.0	mA	2, 5
Current Dissipation in Standby Mode	I_{SBY1}	V_{CC}	Maximum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Resonator $f_{osc} = 4MHz$	—	—	1.2	mA	3, 5
	I_{SBY2}	V_{CC}	Minimum Logic Operation $V_{CC} = 5V$	Crystal or Ceramic Filter Resonator $f_{osc} = 4MHz$	—	—	0.9	mA	4, 5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}	$V_{in} (TEST) = V_{CC}$ $\sim V_{CC}-0.3V$ $V_{in} (RESET) = 0 \sim 0.3V$		—	—	10	μA	
Stop Mode Retain Voltage	V_{stop}	V_{CC}			2.0	—	—	V	

(Note 1) Output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

Test Conditions: MCU state; ● Reset state in Operation Mode
Pin state; ● RESET, TEST – V_{CC} voltage
 ● D₀ ~ D₃, R3 ~ R9 – V_{CC} voltage
 ● D₄ ~ D₁₅, R0 ~ R2, R_{AD}, RA₁ – $V_{CC} \sim V_{CC}-40V$

(Note 3) The timer/counter with the fastest clock and input/output current does not flow.

Test Conditions: MCU state; ● Standby Mode
 ● Input/Output; Reset state
 ● TIMER-A; ± 2 prescaler divide ratio
 ● TIMER-B; ± 2 prescaler divide ratio
 ● SERIAL; Stop
Pin state; ● RESET – GND voltage
 ● TEST – V_{CC} voltage
 ● D₀ ~ D₃, R3 ~ R9 – V_{CC} voltage
 ● D₄ ~ D₁₅, R0 ~ R2, R_{AD}, RA₁ – $V_{CC} \sim V_{CC}-40V$

(Note 4) The timer/counter with the slowest clock and input/output current does not flow.

Test Conditions: MCU state; ● Standby Mode
 ● Input/Output; Reset state
 ● TIMER-A; ± 2048 prescaler divide ratio
 ● TIMER-B; ± 2048 prescaler divide ratio
 ● SERIAL; Stop



- Pin state:
- RESET – GND voltage
 - TEST – V_{CC} voltage
 - D₀~D₃, R₃~R₉ – V_{CC} voltage
 - D₄~D₁₅, R₀~R₂, R_{A0}, R_{A1} – V_{CC} ~ V_{CC}-40V

(Note 5) The consumption of current in operation and standby mode is proportional to f_{osc}. When f_{osc} = x [MHz], the value of each current is calculated as follows.

$$\text{max. value (f}_{\text{osc}} = x) = \frac{x}{4} \times \text{max. value (f}_{\text{osc}} = 4 \text{ [MHz]}.)$$

● **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
(V_{CC} = 4.5V to 5.5V, GND = 0V, T_a = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₀ ~ D ₃ , R ₃ ~ R ₅ , R ₉		0.7V _{CC}	–	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₀ ~ D ₃ , R ₃ ~ R ₅ , R ₉		–0.3	–	0.22V _{CC}	V	
Output "Low" Voltage	V _{OL}	D ₀ ~ D ₃ , R ₃ ~ R ₈	I _{OL} = 1.6 mA	–	–	0.4	V	
Input/Output Leakage Current	I _{IL}	D ₀ ~ D ₃ , R ₃ ~ R ₉	V _{in} = 0V–V _{CC}	–	–	1	μA	1

(Note 1) Output buffer current are excluded.

● **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
(V_{CC} = 4.5V to 5.5V, GND = 0V, T_a = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₄ ~ D ₁₅ , R ₁ R ₂ , R _{A0} , R _{A1}		0.7V _{CC}	–	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₄ ~ D ₁₅ , R ₁ R ₂ , R _{A0} , R _{A1}		V _{CC} -40	–	0.22V _{CC}	V	
Output "High" Voltage	V _{OH}	D ₄ ~ D ₁₅	–I _{OH} = 15mA	V _{CC} -3.0	–	–	V	
			–I _{OH} = 9mA	V _{CC} -2.0	–	–	V	
		R ₀ ~ R ₂	–I _{OH} = 3mA	V _{CC} -3.0	–	–	V	
			–I _{OH} = 1.8 mA	V _{CC} -2.0	–	–	V	
Output "Low" Voltage	V _{OL}	D ₄ ~ D ₁₅ R ₀ ~ R ₂	150kΩ to V _{CC} -40V	–	–	V _{CC} -37	V	
Input/Output Leakage Current	I _{IL}	D ₄ ~ D ₁₅ R ₀ ~ R ₂ R _{A0} , R _{A1}	V _{in} = V _{CC} -40V to V _{CC}	–	–	20	μA	1

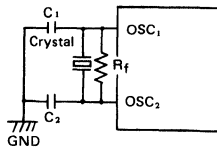
(Note 1) Output buffer current are excluded.

HD614P080S/HD614P0160S

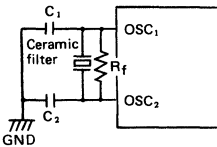
● AC CHARACTERISTICS ($V_{CC} = 4.5V$ to $5.5V$, $GND = 0V$, $T_a = -20$ to $+75^\circ C$, if not specified.)

	Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
					min	typ	max		
Crystal Resonator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂		0.4	—	6.2	MHz	
	Instruction Cycle Time	t_{cyc}			1.29	—	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂		—	—	20	ms	1
Ceramic Filter Resonator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂		0.4	—	6.2	MHz	
	Instruction Cycle Time	t_{cyc}			1.29	—	20	μs	
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂		—	—	20	ms	1
External Clock	External Clock Frequency	f_{CP}	OSC ₁		0.4	—	6.2	MHz	2
	External Clock "High" Level Width	t_{CPH}	OSC ₁		70	—	—	ns	2
	External Clock "Low" Level Width	t_{CPL}	OSC ₁		70	—	—	ns	2
	External Clock Rise Time	t_{CPr}	OSC ₁		—	—	20	ns	2
	External Clock Fall Time	t_{CPl}	OSC ₁		—	—	20	ns	2
	Instruction Cycle Time	t_{cyc}			1.29	—	20	μs	2
	INT ₀ "High" Level Width	t_{10H}	INT ₀		2	—	—	t_{cyc}	3
	INT ₀ "Low" Level Width	t_{10L}	INT ₀		2	—	—	t_{cyc}	3
	INT ₁ "High" Level Width	t_{11H}	INT ₁		2	—	—	t_{cyc}	3
	INT ₁ "Low" Level Width	t_{11L}	INT ₁		2	—	—	t_{cyc}	3
	RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4
	Input Capacitance	C_{in}	all pins	$f = 1MHz$ $V_{in} = 0V$	—	—	15	pF	
	Reset Fall Time	t_{RSTf}			—	—	20	ms	4

(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage $V_{CC} = 4.5V$ after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.

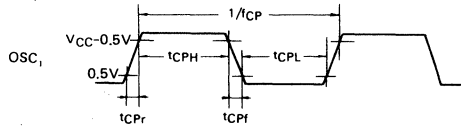


Crystal: 6.0 [MHz]
NC-18C (Nihon Denpa Kogyo)
 $R_f = 1 [M\Omega] \pm 2\%$, $C_1 = C_2 = 20 [pF] \pm 20\%$

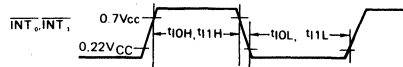


Ceramic filter: CSA6.00 MG (Murata)
 $R_f = 1 [M\Omega] \pm 2\%$, $C_1 = C_2 = 30 [pF] \pm 20\%$

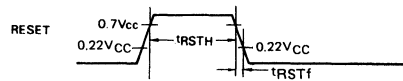
(Note 2)



(Note 3)



(Note 4)



● SERIAL INTERFACE TIMING CHARACTERISTICS
($V_{CC} = 4.5V$ to $5.5V$, $GND = 0V$, $T_a = -20$ to $+75^{\circ}C$, if not specified.)

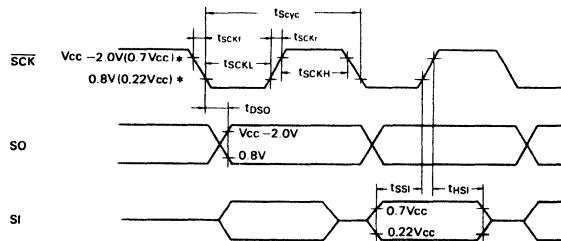
- At Transfer Clock Output

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	\overline{SCK}	(Note 2)	1	—	—	t_{CYC}	1, 2
Transfer Clock "High" Level Width	t_{SCKH}	\overline{SCK}	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock "Low" Level Width	t_{SCKL}	\overline{SCK}	(Note 2)	0.5	—	—	t_{SCYC}	1, 2
Transfer Clock Rise Time	t_{SCKr}	\overline{SCK}	(Note 2)	—	—	100	ns	1, 2
Transfer Clock Fall Time	t_{SCKf}	\overline{SCK}	(Note 2)	—	—	100	ns	1, 2
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

- At Transfer Clock Input

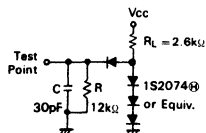
Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Transfer Clock Cycle Time	t_{SCYC}	\overline{SCK}		1	—	—	t_{CYC}	1
Transfer Clock "High" Level Width	t_{SCKH}	\overline{SCK}		0.5	—	—	t_{SCYC}	1
Transfer Clock "Low" Level Width	t_{SCKL}	\overline{SCK}		0.5	—	—	t_{SCYC}	1
Transfer Clock Rise Time	t_{SCKr}	\overline{SCK}		—	—	100	ns	1
Transfer Clock Fall Time	t_{SCKf}	\overline{SCK}		—	—	100	ns	1
Serial Output Data Delay Time	t_{DSO}	SO	(Note 2)	—	—	250	ns	1, 2
Serial Input Data Set-up Time	t_{SSI}	SI		300	—	—	ns	1
Serial Input Data Hold Time	t_{HSI}	SI		150	—	—	ns	1

(Note 1) Timing Diagram of Serial Interface



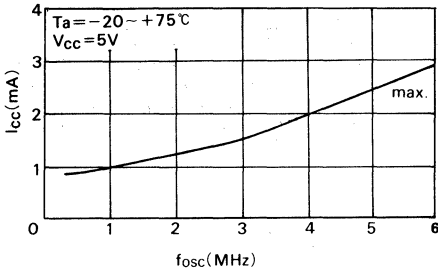
* $V_{CC} - 2.0V$ and $0.8V$ are the threshold voltage for transfer clock output.
 $0.7V_{CC}$ and $0.22V_{CC}$ are the threshold voltage for transfer clock input.

(Note 2) Timing Load Circuit

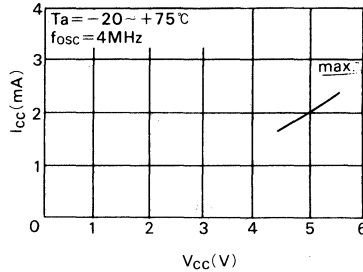


HD614P080S/HD614P0160S

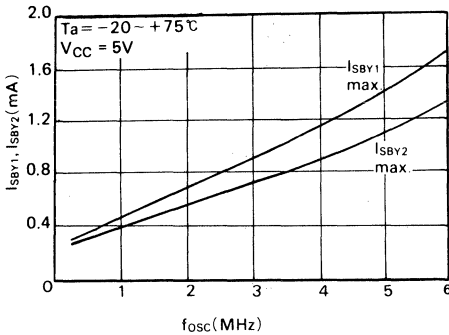
CHARACTERISTICS CURVE (REFERENCE DATA)



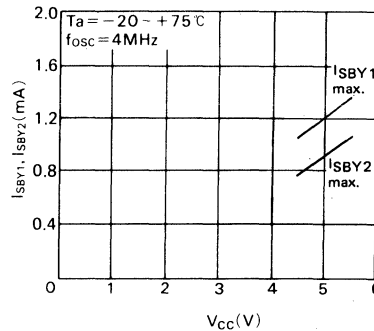
I_{CC} vs. f_{osc} characteristic
(crystal, ceramic resonator)



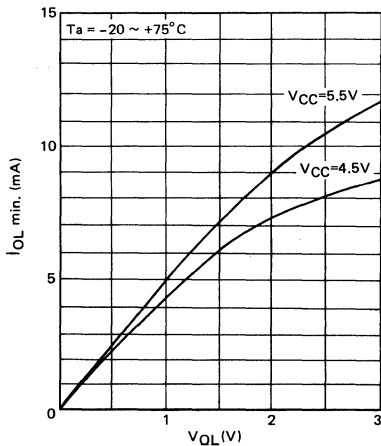
I_{CC} vs. V_{CC} characteristic
(crystal, ceramic resonator)



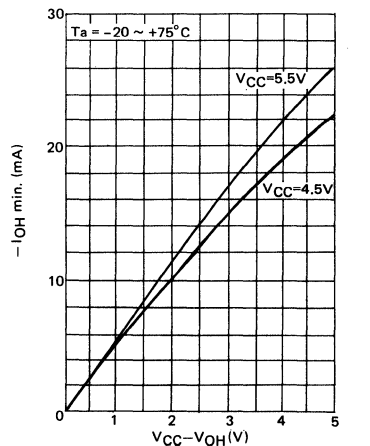
I_{SBY1} vs. f_{osc} characteristics
(crystal, ceramic resonator)



I_{SBY1} vs. V_{CC} characteristics
(crystal, ceramic resonator)

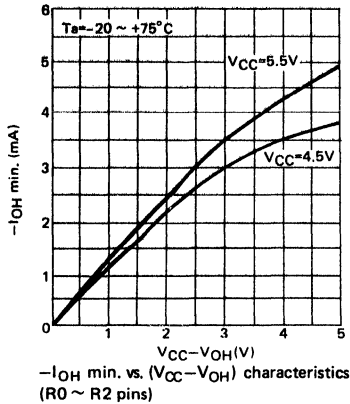


$I_{OL \text{ min.}}$ vs. V_{OL} characteristics
(Standard Pin)



$-I_{OH \text{ min.}}$ vs. $(V_{CC} - V_{OH})$ characteristics
(D4 ~ D15 pins)





■ DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

● GND, V_{CC}, V_{disp}

These are power supply pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. R_{A1}/V_{disp} pin is used for R_{A1} as all high voltage pins are "without pull-down MOS" (PMOS open drain).

● TEST

TEST pin is not for users application. Connect it to V_{CC}.

● RESET

RESET pin is used to reset MCU. For details, see "RESET"

● OSC₁, OSC₂

These are input pins to the internal clock generator circuit. They can be connected to crystal resonator, ceramic filter resonator, or external oscillator circuit. For details, see "INTERNAL OSCILLATOR CIRCUIT."

● D-port (D₀ to D₁₅)

D-port is a 1-bit Input/Output common port. D₀ to D₃ are

standard type, D₄ to D₁₅ are for high voltage. For details, see "INPUT/OUTPUT".

● R-port (R₀ to R_A)

R-port is a 4-bit Input/Output port. (only R_A is 2-bit construction.) R₀ and R₆ to R₈ are output ports, R₉ to R_A are input ports, and R₁ to R₅ are Input/Output common ports. R₀ to R₂ and R_A are the high voltage ports, R₃ to R₉ are the standard ports. R₃₂, R₃₃, R₄₀, R₄₁, and R₄₂ are also available as INT₀, INT₁, SCK, SI and SO respectively. For details, see "INPUT/OUTPUT".

● INT₀, INT₁

These are the input pins to interrupt MCU operation externally. INT₁ can be used as an external event input pin for TIMER-B. INT₀ and INT₁ are also available as R₃₂, and R₃₃ respectively. For details, see "INTERRUPT".

● SCK, SI, SO

These are transfer clock I/O pin (SCK), serial data input pin (SI) and serial data output pin (SO) used for serial interface. SCK, SI and SO are also available as R₄₀, R₄₁, and R₄₂ respectively. For details, see "SERIAL INTERFACE".

■ ROM MEMORY MAP

ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

● Vector Address Area \$0000 to \$000F

When MCU reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

● Zero-Page Subroutine Area \$0000 to \$003F

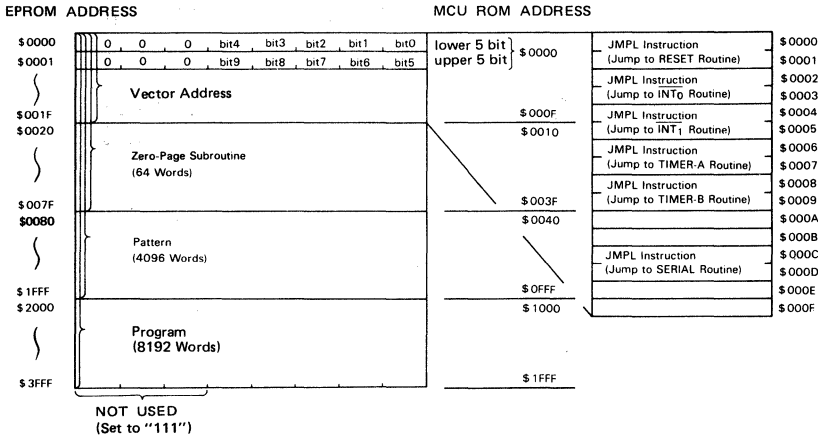
CAL instruction allows to branch to the subroutines in \$0000 to \$003F.

● Pattern Area \$0000 to \$0FFF

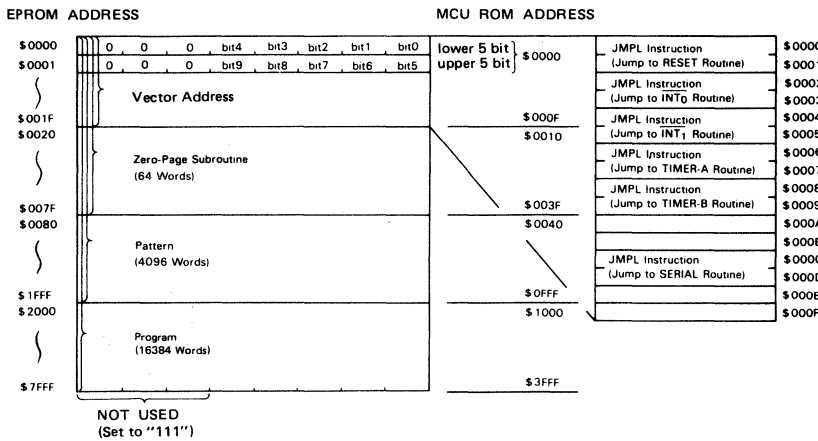
P instruction allows referring to the ROM data in \$0000 to \$0FFF as a pattern.

● Program Area \$0000 to \$1FFF; HD614P080S
\$0000 to \$3FFF; HD614P0160S

HD614P080S/HD614P0160S



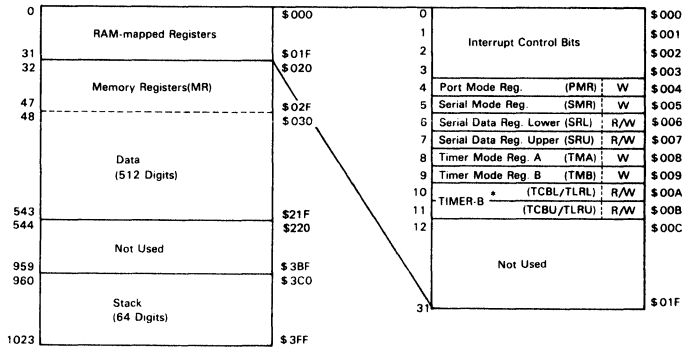
HD614P080S



HD614P0160S

Fig. 1 ROM Memory Map





* Two registers are mapped on same address.

R : Read Only
W : Write Only
R/W : Read/Write

Timer/Event Counter B Lower (TCBL)	R	Timer Load Reg. Lower (TLRL)	W	\$00A
Timer/Event Counter B Upper (TCBU)	R	Timer Load Reg. Upper (TLRU)	W	\$00B

Fig. 2 RAM Memory Map

RAM MEMORY MAP

The MCU includes 576 digits x 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits

and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of $\overline{INT_0}$)	IFO (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	IMTA (IM of $\overline{INT_A}$)	IFTA (IF of $\overline{INT_A}$)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	\$001
2	Not Used	Not Used	IMTB (IM of $\overline{INT_B}$)	IFTB (IF of $\overline{INT_B}$)	\$002
3	Not Used	Not Used	IMS (IM of $\overline{INT_S}$)	IFS (IF of $\overline{INT_S}$)	\$003

IF : Interrupt Request Flag
IM : Interrupt Mask
I/E : Interrupt Enable Flag
SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invalid when "RSP" bit and "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

HD614P080S/HD614P0160S

- **Interrupt Control Bit Area \$000 to \$003**

This area is used for interrupt controls, and is illustrated in Fig. 3. It is accessible only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is only used to reset the SP.

- **Special Register Area \$004 to \$00B**

Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

- **Data Area \$020 to \$21F**

16 digits of \$020 to \$02F are called memory register (MR) and accessible by LAMR and XMRA instructions.

- **Stack Area \$3C0 to \$3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction, and not affected by RTN instruction. The area, not used for stacking, is available as a data area.

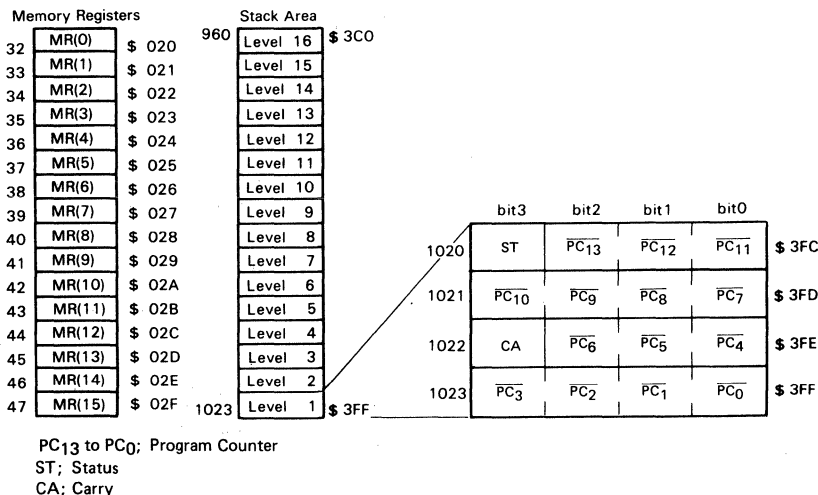


Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

- **REGISTER AND FLAG**

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

- **Accumulator (A), B Register (B)**

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

- **W Register (W), X Register (X), Y Register (Y)**

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y Register is also used for D-port addressing. W Register is write-only and cannot be read.

- **SPX Register (SPX), SPY Register (SPY)**

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

- **Carry (CA)**

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

- **Status (ST)**

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)



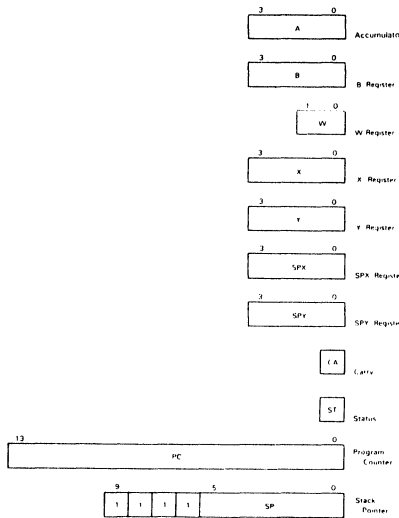


Fig. 5 Register and Flags

● **Program Counter (PC)**

Program Counter is a 14-bit binary counter for ROM addressing.

● **Stack Pointer (SP)**

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate \$3FF on the RAM address, and is decremented by 4 as data pushed into the stack,

and incremented by 4 as data restored back from the stack.

■ **INTERRUPT**

The MCU can be interrupted by five different sources: the external signals (INT₀, INT₁), timer/counter (TIMER-A, TIMER-B), and serial interface (SERIAL). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

● **Interrupt Control Bit and Interrupt Service**

The interrupt control bit is mapped on \$000 to \$003 of the RAM address and accessible by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the five interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the five interrupt sources.

Fig. 7 shows the interrupt services sequence, and Fig. 8 shows the interrupt flowchart. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

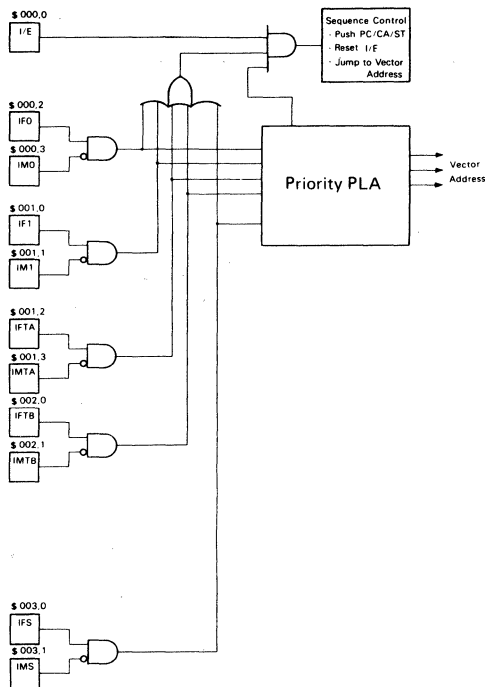


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset / Interrupt	Priority	Vector addresses
RESET	-	\$0000
INT ₀	1	\$0002
INT ₁	2	\$0004
TIMER-A	3	\$0006
TIMER-B	4	\$0008
SERIAL	5	\$000C

Table 2. Conditions of Interrupt Service

Interrupt source Interrupt control bits	INT ₀	INT ₁	TIMER-A	TIMER-B	SERIAL
I/E	1	1	1	1	1
IFO · IMO	1	0	0	0	0
IF1 · IM1	*	1	0	0	0
IFTA · IMTA	*	*	1	0	0
IFTB · IMTB	*	*	*	1	0
IFS · IMS	*	*	*	*	1

* Don't care

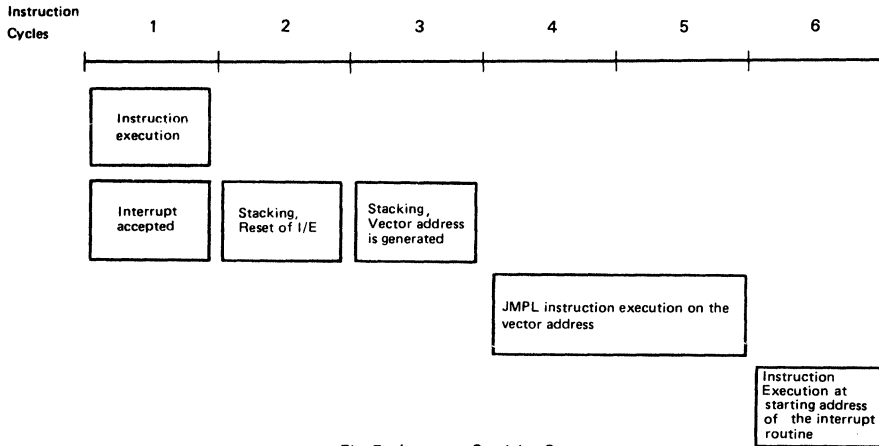


Fig. 7 Interrupt Servicing Sequence

● **Interrupt Enable Flag (I/E: \$000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

● **External Interrupt (\overline{INT}_0 , \overline{INT}_1)**

To use external interrupt, select R_{32}/\overline{INT}_0 , R_{33}/\overline{INT}_1 port for \overline{INT}_0 , \overline{INT}_1 mode by setting the Port Mode Register (PMR: \$004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 , \overline{INT}_1 inputs.

\overline{INT}_1 input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using \overline{INT}_1 as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted.

● **External Interrupt Request Flag (IF0: \$000,2, IF1: \$001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of \overline{INT}_0 , \overline{INT}_1 inputs respectively.

● **External Interrupt Mask (IM0: \$000,3, IM1: \$001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

● **Port Mode Register (PMR: \$004)**

The Port Mode Register is a 4-bit write-only register which controls the R_{32}/\overline{INT}_0 pin, R_{33}/\overline{INT}_1 pin, R_{41}/SI pin and R_{42}/SO pin as shown in Table 6. The Port Mode Register will be initialized to \$0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	R_{33}/\overline{INT}_1 pin
0	Used as R_{33} port input/output pin
1	Used as \overline{INT}_1 input pin

PMR bit 2	R_{32}/\overline{INT}_0 pin
0	Used as R_{32} port input/output pin
1	Used as \overline{INT}_0 input pin

PMR bit 1	R_{41}/SI pin
0	Used as R_{41} port input/output pin
1	Used as SI input pin

PMR bit 0	R_{42}/SO pin
0	Used as R_{42} port input/output pin
1	Used as SO output pin

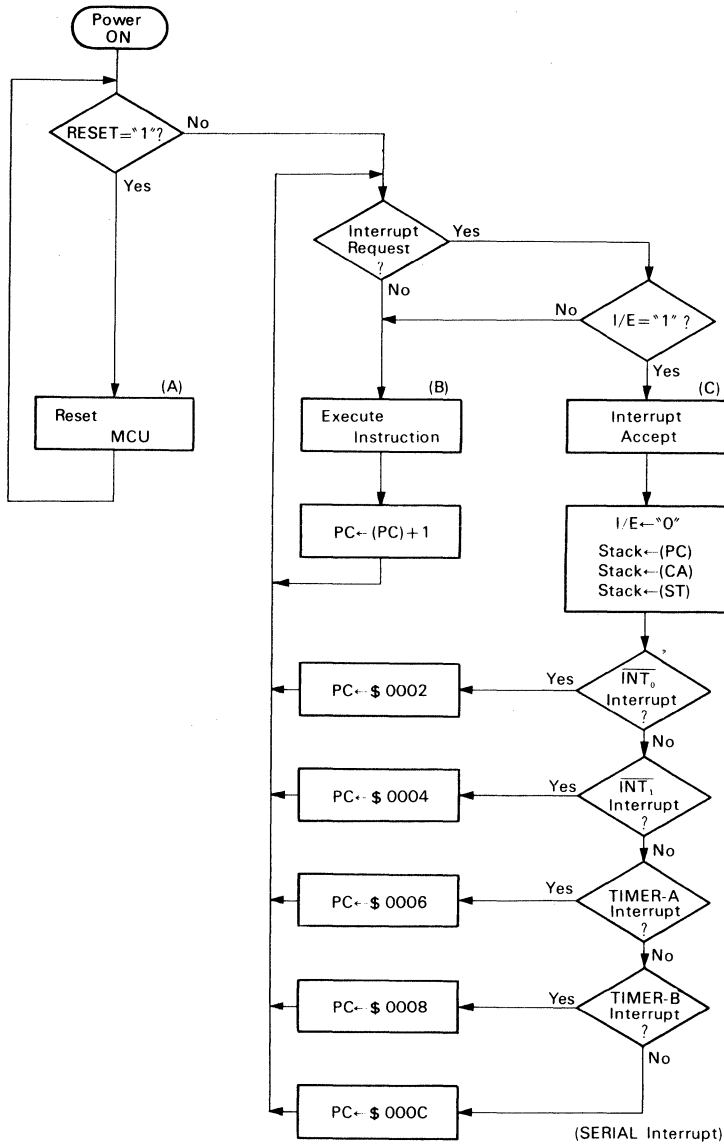


Fig. 8 Interrupt Servicing Flowchart

■ SERIAL INTERFACE

The serial interface is used to transmit/receive 8-bit data serially. This consists of the Serial Data Register, the Serial Mode Register, the Octal Counter and the multiplexer, as illustrated in Fig. 9. Pin R_{A0}/SCK and the transfer clock signal are controlled by the Serial Mode Register. Contents of the Serial Data Register can be written into or read out by the software. The data in the Serial Data Register can be shifted synchronous-

ly with the transfer clock signal.

The serial interface operation is initiated with STS instruction. The Octal Counter is reset to \$0 by STS instruction. It starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of the SCK. When the Octal Counter is reset to \$0 after eight transfer clock signals, or discontinued transmit/receive operation by resetting the Octal Counter, the SERIAL Interrupt Request Flag will be set.

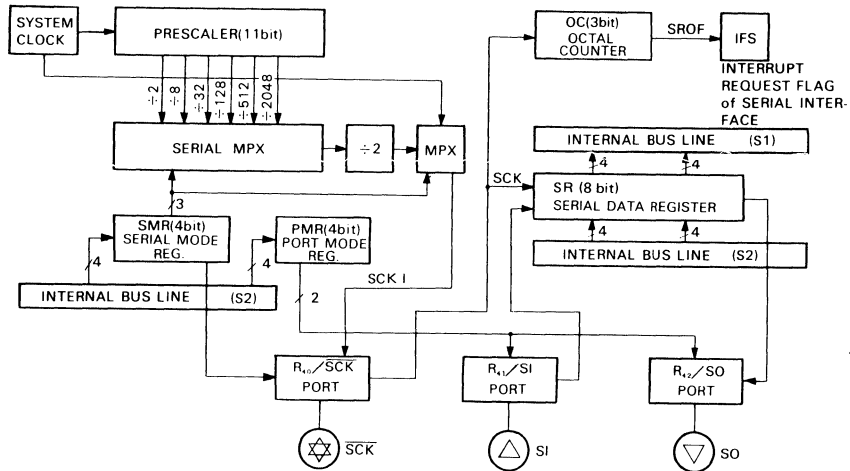


Fig. 9 Serial Interface Block Diagram

● Serial Mode Register (SMR: \$005)

The Serial Mode Register is a 4-bit write-only register. This register controls the R_{A0}/SCK and the prescaler divide ratio as the transfer clock source as shown in Table 7.

The Write Signal to the Serial Mode Register controls the operating state of serial interface.

The Write Signal to the Serial Mode Register stops the transfer clock applied to the Serial Data Register and the Octal Counter. And it also reset the Octal Counter to \$0 simultaneously.

When the Serial Interface is in the "Transfer State", the Write Signal to the Serial Mode Register causes to quit the data transfer and to set the SERIAL Interrupt Request Flag.

Contents of the Serial Mode Register will be changed on the second instruction cycle after writing into the Serial Mode Register. Therefore, it will be necessary to execute the STS instruction after the data in the Serial Mode Register has been changed completely. The Serial Mode Register will be reset to

\$0 by MCU reset.

● Serial Data Register (SRL: \$006, SRU: \$007)

The Serial Data Register is an 8-bit read/write register. It consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the Serial Data Register will be output from the LSB side at SO pin synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the LSB side at SI pin to the Serial Data Register synchronously with the rising edge of the transfer clock. Fig. 10 shows the I/O timing chart for the transfer clock signal and the data.

The writing into/reading from the Serial Data Register during its shifting causes the validity of the data.

Therefore complete data transmit/receive before writing into/reading from the serial data register.

Table 7. Serial Mode Register

SMR Bit 3	R_{40}/\overline{SCK}
0	Used as R_{40} port input/output pin
1	Used as \overline{SCK} input/output pin

SMR			Transfer Clock			
Bit 2	Bit 1	Bit 0	R_{40}/\overline{SCK} Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	\overline{SCK} Output	Prescaler	÷ 2048	÷ 4096
0	0	1	\overline{SCK} Output	Prescaler	÷ 512	÷ 1024
0	1	0	\overline{SCK} Output	Prescaler	÷ 128	÷ 256
0	1	1	\overline{SCK} Output	Prescaler	÷ 32	÷ 64
1	0	0	\overline{SCK} Output	Prescaler	÷ 8	÷ 16
1	0	1	\overline{SCK} Output	Prescaler	÷ 2	÷ 4
1	1	0	\overline{SCK} Output	System Clock	—	÷ 1
1	1	1	\overline{SCK} Input	External Clock	—	—

(In the case of SMR Bit 3 = 1)

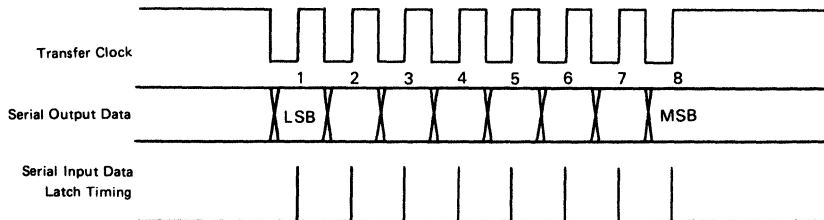


Fig. 10 Serial Interface I/O Timing Chart

- SERIAL Interrupt Request Flag (IFS: \$003, 0)**
 The SERIAL Interrupt Request Flag will be set after the eight transfer clock signals or transmit/receive discontinued operation by resetting the Octal Counter.
- SERIAL Interrupt Mask (IMS: \$003, 1)**
 The SERIAL Interrupt Mask masks the interrupt request.

Table 8. SERIAL Interrupt Request Flag

SERIAL Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. SERIAL Interrupt Mask

SERIAL Interrupt Mask	Interrupt Request
0	Enable
1	Disable (masks)

- Selection of the Operation Mode**
 Table 10 shows the operation mode of the serial interface. Select a combination of the value in the Port Mode Register and the Serial Mode Register according to Table 10. Initialize the serial interface by the Write Signal to the Serial Mode Register, when the Operation Mode is changed.
- Operating State of Serial Interface**
 The serial interface has 3 operating states as shown in Fig. 11. The serial interface gets into "STS waiting state" by 2 ways: one way is to change the operation mode by changing the data

in the Port Mode Register, the other is to write data into the Serial Mode Register. In this state, the serial interface does not operate although the transfer clock is applied. If STS instruction is executed, the serial interface changes its state to "SCK waiting state".

In the "SCK waiting state", the falling edge of first transfer clock affects the serial interface to get into "transfer state", while the Octal Counter counts-up and the Serial Data Register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in "SCK waiting state" while the transfer clock outputs continuously.

The Octal Counter becomes "000" again by 8 transfer clocks or execution of STS instruction, so that the serial interface gets back into the "SCK waiting state", and SERIAL Interrupt Request Flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output are triggered by the execution of STS instruction, and it stops after 8 clocks.

● **Example of Transfer Clock Error Detection**

The serial interface functions abnormally when the transfer clock was disturbed by external noises. In this case, the transfer

clock error can be detected in the procedure shown in Fig. 12.

If more than 9 transfer clocks are applied by the external noises in the "SCK waiting state", the state of the serial interface shifts as the following sequence: first "transfer state" (while 1 to 7 transfer clocks), second "SCK waiting state" (at 8th transfer clock) and third "transfer state" again. Then reset the SERIAL Interrupt Request Flag, and make "STS waiting state" by writing to the Serial Mode Register. SERIAL Interrupt Request Flag is set again in this procedure, and it shows that the transfer clock was invalid and that the transmit/receive data were also invalid.

Table 10. Serial Interface Operation Mode

SMR Bit 3	PMR		Serial Interface Operating Mode
	Bit 1	Bit 0	
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

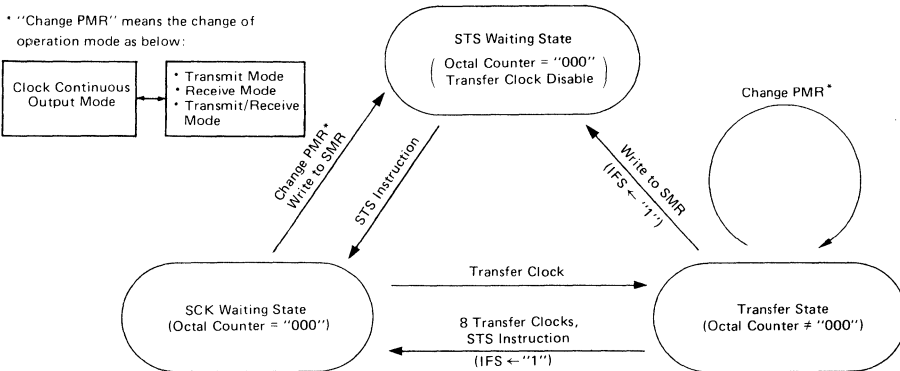


Fig. 11 Serial Interface Operation State

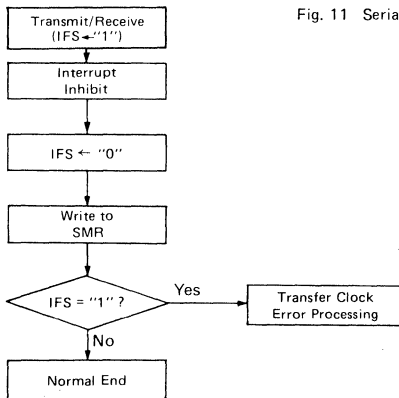


Fig. 12 Example of Transfer Clock Error Detection

■ **TIMER**

The MCU contains a prescaler and two timer/counters (TIMER-A, TIMER-B). Fig. 13 shows the block diagram. The prescaler is an 11-bit binary counter. TIMER-A is an 8-bit free-run timer. TIMER-B is an 8-bit auto-reload timer/event counter.

● **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-A, TIMER-B and serial interface. The prescaler divide ratio of the clock signals are selected according to the content of the mode registers such as - Timer Mode Register A (TMA), Timer Mode Register B (TMB), Serial Mode Register (SMR).

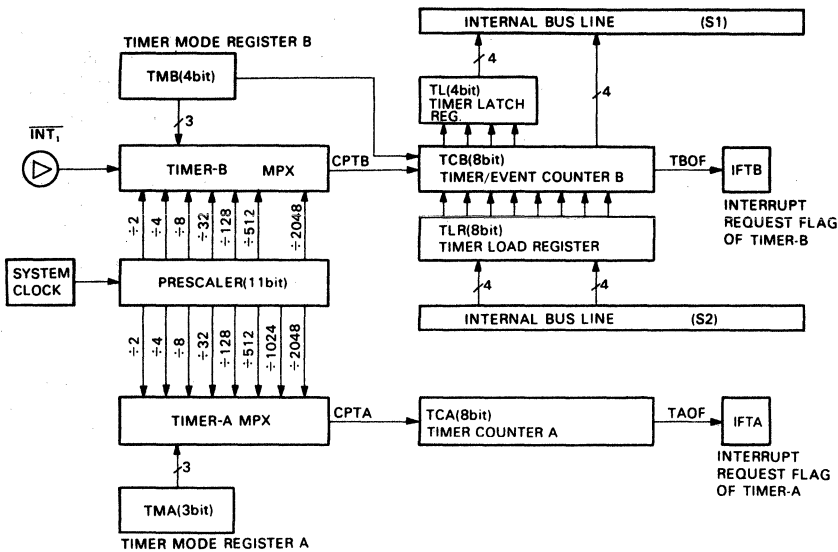


Fig. 13 Timer/Counter Block Diagram

● **TIMER-A Operation**

After **TIMER-A** is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after **TIMER-A** is counted up to \$FF, **TIMER-A** is set to \$00 again, and generating overflow output. This leads to setting **TIMER-A** Interrupt Request Flag (IFTA: \$001, 2) to "1". Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to **TIMER-A** are selected by the **Timer Mode Register A (TMA: \$008)**.

● **TIMER-B Operation**

Timer Mode Register B (TMB: \$009) is used to select the auto-reload function and the prescaler divide ratio of **TIMER-B** as the input clock source. When the external event input is used as an input clock signal to **TIMER-B**, select the R_{33}/\overline{INT}_1 as \overline{INT}_1 and set the External Interrupt Mask (IM1) to "1" to prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the **Timer Load Register** by software. **TIMER-B** counts up at every clock input signal. When the next clock signal is applied to **TIMER-B** after **TIMER-B** is set to \$FF, **TIMER-B** will be initialized again and generate overflow output. In this case if the auto-reload function is selected, **TIMER-B** is initialized according to the value of the **Timer Load Register**. Else if the auto-reload function is not selected, **TIMER-B** goes to \$00. **TIMER-B** Interrupt Request Flag (IFTB: \$002.0) will be set at this overflow output.

● **Timer Mode Register A (TMA: \$008)**

The **Timer Mode Register A** is a 3-bit write-only register. The **TMA** controls the prescaler divide ratio of **TIMER-A** clock input, as shown in Table 11.

The **Timer Mode Register A** is initialized to \$0 by MCU reset.

● **Timer Mode Register B (TMB: \$009)**

The **Timer Mode Register B** is a 4-bit write-only register. The **Timer Mode Register B** controls the selection for the auto-reload function of **TIMER-B** and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 12.

The **Timer Mode Register B** is initialized to \$00 by MCU reset.

The operation mode of **TIMER-B** is changed at the second instruction cycle after writing into the **Timer Mode Register B**.

Therefore, it is necessary to program the write instruction to **TLRU** after the content of **TMB** is changed.

Table 11. **Timer Mode Register A**

TMA			Prescaler Divide Ratio
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB			Auto-reload Function
Bit 3			
0			No
1			Yes

TMB			Prescaler Divide Ratio, Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

• **TIMER-B (TCBL: \$00A, TCBU: \$00B)
(TLRL: \$00A, TLRU: \$00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to \$00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading

the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

• **TIMER-A Interrupt Request Flag (IFTA: \$001, 2)**

The TIMER-A Interrupt Request Flag is set by the overflow output of TIMER-A.

• **TIMER-A Interrupt Mask (IMTA: \$001, 3)**

TIMER-A Interrupt Mask prevents an interrupt request generated by TIMER-A Interrupt Request Flag.

Table 13. TIMER-A Interrupt Request Flag

TIMER-A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. TIMER-A Interrupt Mask

TIMER-A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

• **TIMER-B Interrupt Request Flag (IFTB: \$002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

• **TIMER-B Interrupt Mask (IMTB: \$002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

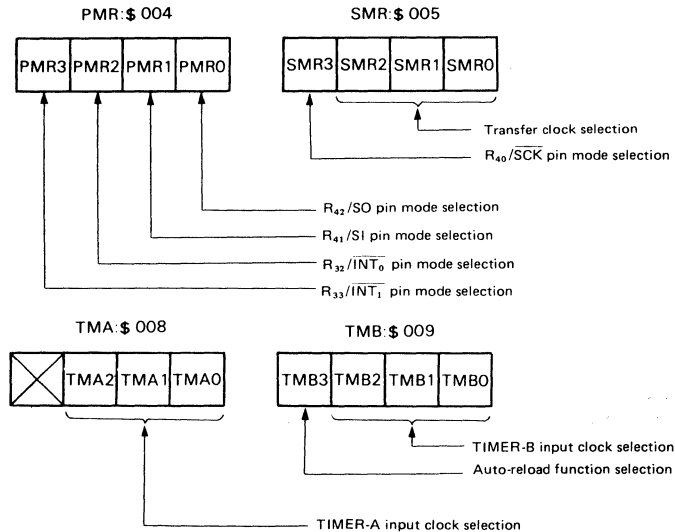


Fig. 14 Mode Register Configuration and Function



HD614P080S/HD614P0160S

Table 15. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

INPUT/OUTPUT

The MCU provides 58 Input/Output pins, and they are consist of 32 standard pins of "Without pull-up MOS (NMOS open drain)" and 26 high voltage pins of "Without pull-down MOS (PMOS open drain)".

When any input/output common pin is used as input pin, it is necessary to set the output data as shown in Table 18.

Table 17 I/O Pin Circuit Forms

	Without pull-up MOS (NMOS open drain)	Applied pins
Standard pins		D ₀ ~ D ₃ , R ₃₀ ~ R ₃₃ , R ₄₀ ~ R ₄₃ , R ₅₀ ~ R ₅₃
		R ₆₀ ~ R ₆₃ , R ₇₀ ~ R ₇₃ , R ₈₀ ~ R ₈₃
		R ₉₀ ~ R ₉₃

(Continued)

	Without pull-down MOS (PMOS open drain)	Applied pins
High voltage pins		D ₄ ~ D ₁₅ , R ₁₀ ~ R ₁₃ , R ₂₀ ~ R ₂₃
		R ₀₀ ~ R ₀₃
		R _{A0} , R _{A1} /V _{disp}

	Without pull-up MOS (NMOS open drain)	Applied pins
Standard pins		SCK (Note 2) (Output Mode)
		SO
		INT ₀ , INT ₁ , SI, SCK (Note 2) (Input Mode)

(Note 1) In the stop mode, HLT signal is "0", HLT signal is "1" and I/O pins are in high impedance state.

(Note 2) If the MCU is interrupted by serial interface in the external clock input mode, the SCK terminal becomes input only.



Table 18 Data Input from Input/Output Common Pins

I/O circuit type	Available pin condition for input
For Standard pins "Without pull-up MOS (NMOS open drain)"	"1"
For High voltage pins "Without pull-down MOS (PMOS open drain)"	"0"

● **D-port**

D-port is 1-bit I/O port, and it has 16 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD and TDD instructions. Table 17 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

● **R-port**

R-port is 4-bit I/O port. It provides 20 input/output common pins, 16 output-only pins, and 6 input-only pins. Data input is processed using the LAR and LBR instructions and data

output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R₃₂, R₃₃, R₄₀, R₄₁ and R₄₂ pins are also used as the INT₀, INT₁, SCK, SI and SO pins respectively. Table 17 shows the classification of standard pins, high voltage pins and Input/Output pins circuit types.

■ **RESET**

The MCU is reset by setting RESET pin to "1". At power

Table 19 MCU Initial Value by Reset

Items		Initial value by MCU reset	Contents	
Program counter (PC)		\$0000	Execute program from the top of ROM address.	
Status (ST)		"1"	Enable to branch with conditional branch instructions.	
Stack pointer (SP)		\$3FF	Stack level is 0.	
I/O output register	Standard pin	Without pull-up MOS	"1"	Enable to input.
	High voltage pin	Without pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)	"0"	Inhibit all interrupts.	
	Interrupt Request Flag (IF)	"0"	No interrupt request.	
	Interrupt Mask (IM)	"1"	Mask interrupt request.	
Mode register	Port Mode Register (PMR)	"0000"	See Item "Port Mode Register".	
	Serial Mode Register (SMR)	"0000"	See Item "Serial Mode Register".	
	Timer Mode Register A (TMA)	"000"	See Item "Timer Mode Register A".	
	Timer Mode Register B (TMB)	"0000"	See Item "Timer Mode Register B".	
Timer/Counter, Serial Interface	Prescaler	\$000	—	
	Timer/Counter A (TCA)	\$00	—	
	Timer/Event Counter B (TCB)	\$00	—	
	Timer Load Register (TLR)	\$00	—	
	Octal Counter	"000"	—	

(Note) The values of registers and flags which are not described on above table will become as follows.

Item	After releasing stop mode by MCU Reset	After MCU Reset except the left
Carry (CA)	The value immediately before MCU reset is not guaranteed. Initialization by the program should be required.	The value immediately before MCU Reset is not guaranteed. Initialization by the program should be required.
Accumulator (A)		
B register (B)		
W register (W)		
X/SPX register (X/SPX) Y/SPY register (Y/SPY)		
Serial data register (SR)	— ditto —	— ditto —
RAM	The value immediately before MCU reset (the value immediately before executing stop instruction) is retained.	— ditto —



ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 19 shows initialized items by MCU reset and each status after reset.

INTERNAL OSCILLATOR CIRCUIT

Fig. 15 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal resonator, or ceramic filter resonator as shown in Table 20. In any cases, external clock operation is available.

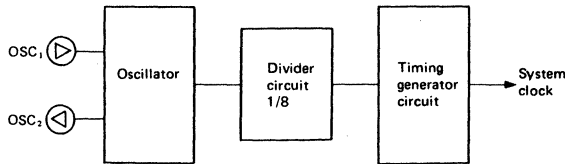


Fig. 15 Internal Oscillator Circuit

Table 20 Oscillator Circuit Example

	Circuit configuration	Remarks
External clock operation		
Ceramic filter resonator		Ceramic filter: CSA 4.00MG (Murata) R_f : $1M\Omega \pm 2\%$ C_1 : $33pF \pm 20\%$ C_2 : $33pF \pm 20\%$ Ceramic filter: CSA 6.00MG (Murata) R_f : $1M\Omega \pm 2\%$ C_1 : $30pF \pm 20\%$ C_2 : $30pF \pm 20\%$
Crystal resonator	 	Crystal: 4.194304 (MHz) NC-18C (Nihon Denpa Kogyo) R_f : $1M\Omega \pm 2\%$ C_1 : $22pF \pm 20\%$ C_2 : $22pF \pm 20\%$ Crystal: 6.0 (MHz) NC-18C (Nihon Denpa Kogyo) R_f : $1M\Omega \pm 2\%$ C_1 : $20pF \pm 20\%$ C_2 : $20pF \pm 20\%$ Crystal: ATcut parallel resonance crystal C_0 : 7 pF max. R_s : 100Ω max. f : 2.0 ~ 6.2MHz

(Note 1) On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.

(Note 2) Wiring among OSC₁, OSC₂ and elements should be as short as possible, and never cross the other wirings. Refer to the layout of crystal and ceramic filter.

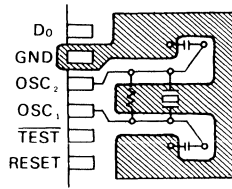


Fig. 16 Layout of Crystal and Ceramic Filter

■ **LOW POWER DISSIPATION MODE**

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 21 shows the function of the low power dissipation mode, and Fig. 17 shows the diagram of the mode transition.

Table 21 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/Output pin	Timer/Counter, Serial Interface	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ^{*2)}	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ^{*1)}	Stop	Retained	High impedance	Stop	RESET Input

*1) STOP mode is released only by MCU Reset. Refer to Table 19 as for the values of the registers and flags after releasing stop mode.

*2) Current flows in I/O Circuit by I/O pin state at stand-by mode, because I/O circuit is active. This current is an addition to stand-by mode power dissipation.

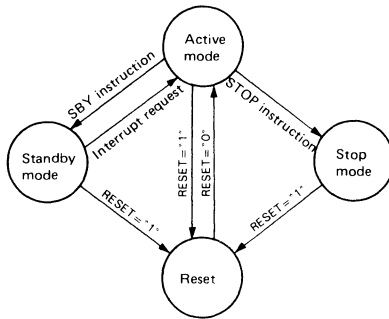


Fig. 17 MCU Operation Mode Transition

● **Standby Mode**

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/

counter and serial interface continue working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 18 shows the flowchart of the Standby Mode.

● **Stop Mode**

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 19, apply the RESET input for more than t_{rc} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode after releasing stop mode by MCU reset, the values of the B register, W register, X/SPX register, Y/SPY register, carry and serial data register are not guaranteed.

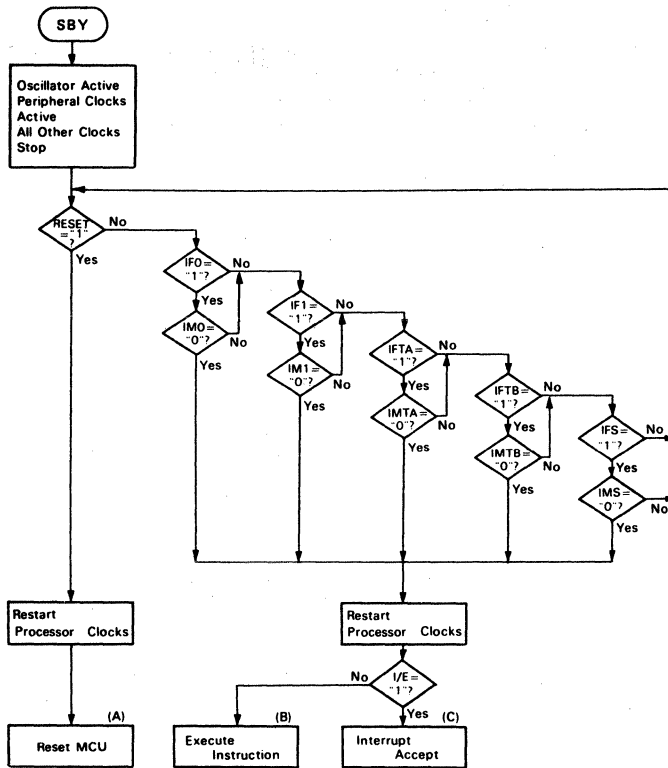


Fig. 18 MCU Operating Flowchart

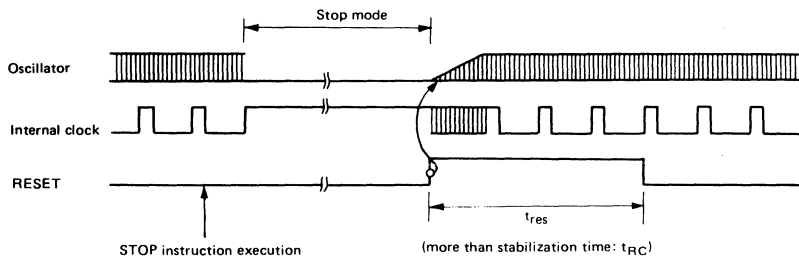


Fig. 19 Stop Mode Cancel Timing Chart

■ RAM ADDRESSING MODE

As shown in Fig. 20, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

● Register Indirect Addressing

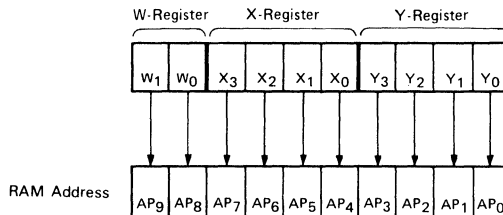
The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

● Direct Addressing

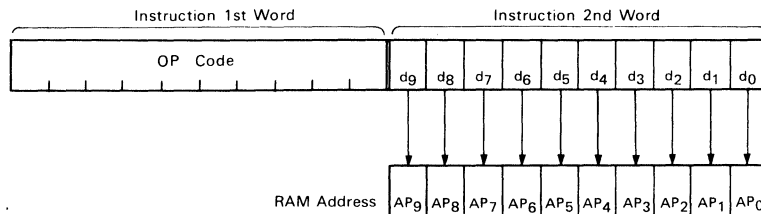
The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

● Memory Register Addressing

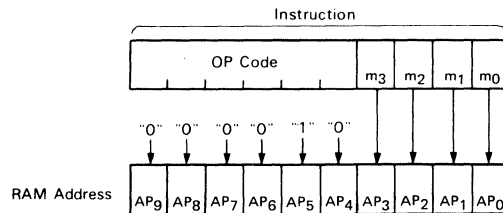
The Memory Register Addressing can access 16 digits (Memory Register: MR) from \$020 to \$02F by using the LAMR and XMRA instruction.



(a) Register Indirect Addressing



(b) Direct Addressing



(c) Memory Register Addressing

Fig. 20 RAM Addressing Mode



ROM ADDRESSING MODE AND P INSTRUCTION

The MCU has four kinds of ROM addressing modes as shown in Fig. 21.

Direct Addressing Mode

The program can branch to any addresses in the ROM memory space by using JMWL, BRL or CALL instruction. These instructions replace 14-bit program counter (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode

ROM memory space is divided into 256 words in each page starting from \$0000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC₇ to PC₀) with 8-bit immediate data.

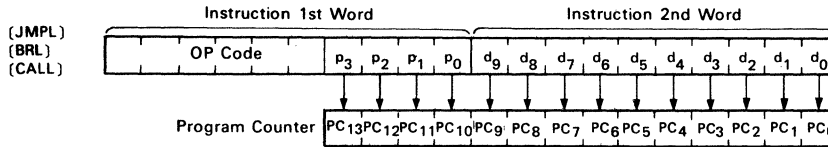
The branch destination by BR instruction on the boundary between pages is in the next page. Refer to Fig. 23.

Zero Page Addressing Mode

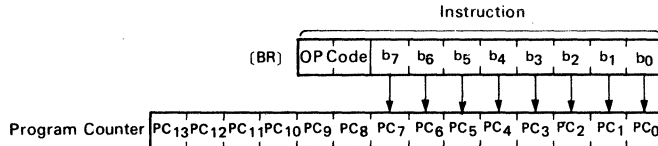
The program branches to the zero page subroutine area, which is located on the address from \$0000 to \$003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC₅ to PC₀) and "0's" are placed in high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing

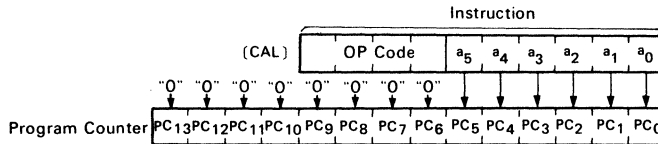
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



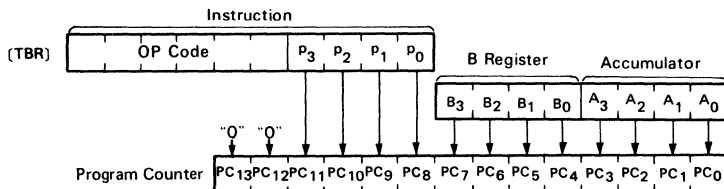
(a) Direct Addressing



(b) Current Page Addressing



(c) Zero Page Addressing



(d) Table Data Addressing

Fig. 21 ROM Addressing Mode

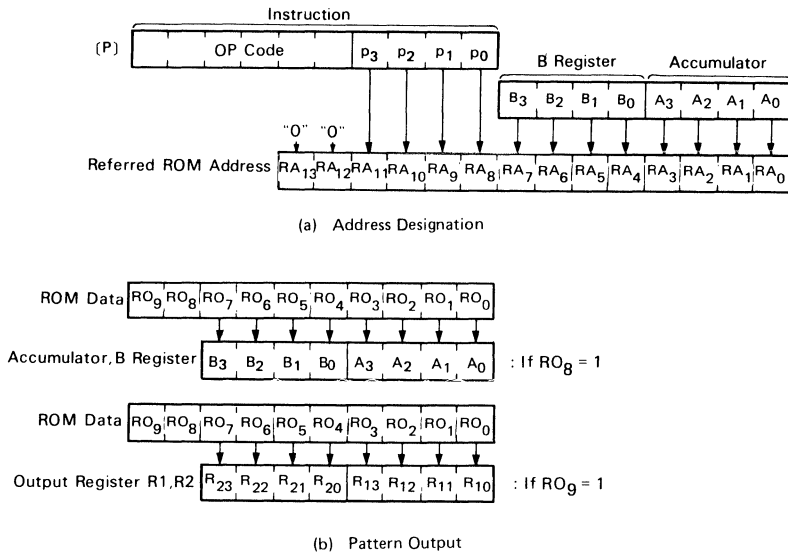


Fig. 22 P Instruction

● **P Instruction (Pattern Instruction)**

By P instruction, the ROM data determined by Table Data addressing is referred. When bit 8 in referred ROM data is "1", 8 bits of referred ROM data are written into the accumu-

lator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

● **Description of the branch destination on page boundary**

When BR is on page boundary (256n + 255), BR instruction transfers the contents of PC to the next page with hardware architecture. Therefore, the program branches to the next page when using BR on page boundary.

The HMCS400 series cross macro assembler has automatic paging facility for ROM page.

■ **INSTRUCTION SET**

The HD614P080S and HD614P0160S provide 99 instructions. These instructions are classified into 10 groups as follows;

- (1) Immediate Instruction
- (2) Register-to-Register Instruction
- (3) RAM Address Instruction
- (4) RAM Register Instruction
- (5) Arithmetic Instruction
- (6) Compare Instruction
- (7) RAM Bit Manipulation Instruction
- (8) ROM Address Instruction
- (9) Input/Output Instruction
- (10) Control Instruction

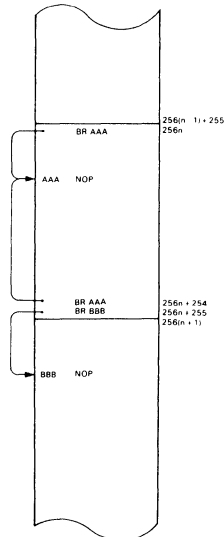


Fig. 23 The Branch Destination by BR Instruction on the Boundary between Pages

Table 22. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1 / 1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1 / 1
Load Memory from Immediate	LMID i, d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2 / 2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y + 1 → Y	NZ	1 / 1

Table 23. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0 0	B → A		1 / 1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0 0	A → B		1 / 1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1 1	Y → A		1 / 1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0 0	SPX → A		1 / 1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0 0	SPY → A		1 / 1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1 / 1
Exchange MR and A	XMRM m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1 / 1

Table 24. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1 / 1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1 / 1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1 / 1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0 0	A → X		1 / 1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0 0	A → Y		1 / 1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0 0	Y + 1 → Y	NZ	1 / 1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1 1	Y - 1 → Y	NB	1 / 1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0 0	Y + A → Y	OVF	1 / 1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0 0	Y - A → Y	NB	1 / 1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1 0	X ↔ SPX		1 / 1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0 0	Y ↔ SPY		1 / 1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1 0	X ↔ SPX, Y ↔ SPY		1 / 1

Table 25. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X ↔ SPX, Y ↔ SPY)		1 / 1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2 / 2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X ↔ SPX, Y ↔ SPY)		1 / 1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X ↔ SPX, Y ↔ SPY)		1 / 1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2 / 2
Load Memory from A, Increment Y	LMAI(Y)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X ↔ SPX)	NZ	1 / 1
Load Memory from A, Decrement Y	LMAD(Y)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X ↔ SPX)	NB	1 / 1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X ↔ SPX, Y ↔ SPY)		1 / 1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2 / 2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X ↔ SPX, Y ↔ SPY)		1 / 1



Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔SPX
LAMY	1	0	Y ↔SPY
LAMXY	1	1	X ↔SPX, Y ↔SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY (X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔SPX

Table 26. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A + i →A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 →B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B - 1 →B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 →CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 →CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A →A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M + A →A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A →A OVF →CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M + A →A OVF →CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M - A →A NB →CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M - A →A NB →CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A B →A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A M →A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A M →A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 1 1 0 0 0	A M →A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A M →A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A + M →A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A + M →A	NZ	2/2



Table 27. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 28. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 29. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA RESTORE		1/3

Table 30. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2



HD614P080S/HD614P0160S

■ PRECAUTION TO USE THE EPROM ON-PACKAGE 4 BIT SINGLE CHIP MICROCOMPUTER

Please pay attention to the followings, since this MCU has special structure with pin socket on the package.

- (1) Don't apply high static voltage or surge voltage over MAXIMUM RATINGS to the socket pins as well as the LSI pins.
If not, that may cause permanent damage to the device.
- (2) When using this in production like mask ROM type single chip microcomputer, pay attention to the followings to keep the good contact between the EPROM pins and socket pins.
 - (a) When soldering the LSI on a print circuit board, the recommended condition is

Temperature: lower than 250°C

Time : within 10 sec.

Over time/temperature may cause the bonding solder of socket pin to melt and the socket pin may drop.

- (b) Note that the detergent or coating will not get in the socket during flux washing or board coating after soldering, because that may cause bad effect on socket contact.
- (c) Avoid permanent application of this under the condition of vibratory place and system.
- (d) The socket, inserted and pulled repeatedly loses its contactability. It is recommended to use new one when applied in production.

Table 33 Differences among HD614P080S/HD614P0160S and HMCS402/404/408

Type name		HD614P080S	HD614P0160S	HMCS404AC	HMCS404C	HMCS404CL	HMCS402AC	HMCS402C	HMCS402CL	HMCS408C
Item										
Minimum instruction execution time		1.33 μs	1.33 μs	1.33 μs	2 μs	4 μs	1.33 μs	2 μs	4 μs	2 μs
Power supply voltage		4.5 ~ 5.5V	4.5 ~ 5.5V	4.5 ~ 6V	4 ~ 6V	2.7 ~ 6V	4.5 ~ 6V	4 ~ 6V	2.7 ~ 6V	4 ~ 6V
ROM		<ul style="list-style-type: none"> ○ 4096 words x 10 bits (using standard EPROM 2764) ○ 8192 words x 10 bits (using standard EPROM 27128) 	16384 words x 10 bits (using standard EPROM 27256)	4,096 words x 10 bits Mask ROM			2,048 words x 10 bits Mask ROM			8192 words x 10 bits Mask ROM
RAM		576 digits x 4 bits		256 digits x 4 bits			160 digits x 4 bits			512 digits x 4 bits
I/O pin circuit	Standard pins	All pins are "without pull-up MOS (NMOS open drain)".		Each pin selects "without pull-up MOS (NMOS open drain)", "with pull-up MOS", or "CMOS".						
	High Voltage pins	All pins are "without pull-down MOS (PMOS open drain)".		Each pin selects "without pull-down MOS (PMOS open drain)" or "with pull-down MOS".						
Clock generator	Crystal resonator	Available		Available	Available	Available	Available	Available	Available	Available
	Ceramic filter resonator	Available		Available	Available	Available	Available	Available	Available	Available
	Resistance oscillator	-		-	Available	-	-	Available	-	-
Package		Shrink type 64-pin EPROM on package (DC-64SP). The base chip pins are compatible with those of the HMCS404 AC/C/CL, HMCS402AC/C/CL and HMCS408C		Shrink type 64-pin dual-in-line plastic package (DP-64S) or 64-pin flat plastic package (FP-64).						
		Type	DC-64SP	DP-64S			FP-64			
		Occupied area (mm ²)	23 x 57.3	17 x 57.6			19.6 x 25.6			
		High from stand-off (mm)	7.5 (max.) EPROM on package	5.1 (max.)			2.9 (max.)			



HMCS412C/HMCS412CL/— HMCS412AC (HD614120/HD614125/HD614128)

Description

The HMCS412C/CL/AC are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins to drive a fluorescent display directly.

Features

- 4-bit architecture
 - 2048 words of 10-bit ROM
 - 160 digits of 4-bit RAM
 - 36 I/O pins, including 24 high-voltage I/O pins (40 V max)
 - Timer/counter
 - 11-bit prescaler
 - 8-bit auto-reload timer/event counter (timer B)
 - Three interrupt sources
 - External: 2
 - Timer/counter: 1
 - Subroutine stack
 - Up to 16 levels including interrupts
 - Minimum instruction execution time
 - 0.89 μ s: HMCS412AC
 - 1.78 μ s: HMCS412C
 - 3.55 μ s: HMCS412CL
 - Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
 - On-chip oscillator
 - Crystal or ceramic filter
 - External clock input
 - Package
 - Standard 42-pin dual in-line plastic package
 - 42-pin shrink dual in-line plastic package
 - 44-pin flat plastic package
- Instruction set compatible with HMCS404; 98 instructions
 - High programming efficiency with 10-bit/word ROM: 78 single-word instructions
 - Direct branch to all RAM areas
 - Direct or indirect addressing of all RAM areas
 - Subroutine nesting up to 16 levels including interrupts
 - Binary and BCD arithmetic operations
 - Powerful logical arithmetic operations
 - Pattern generation-table lookup capability
 - Bit manipulation for both RAM and I/O

Program Development Support Tools

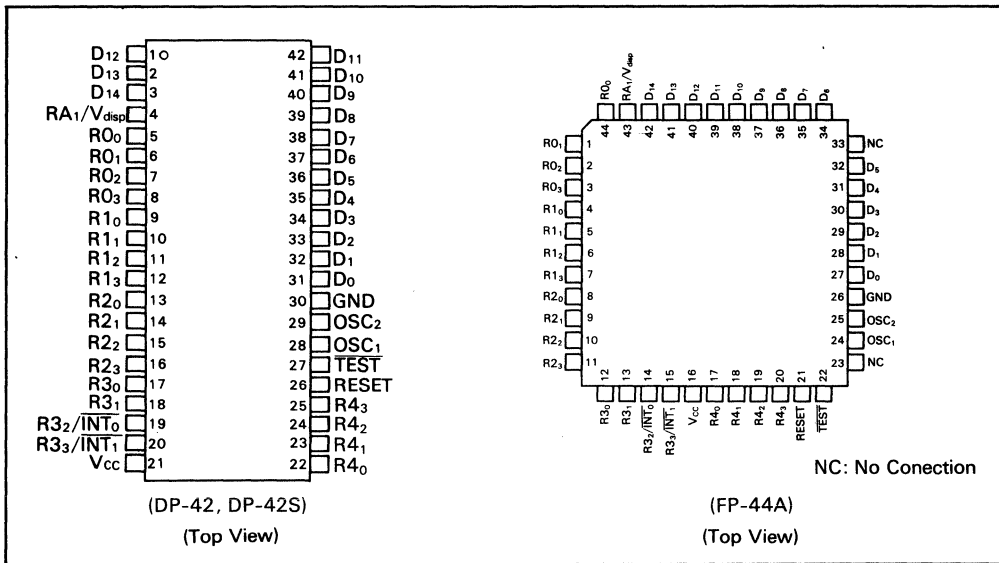
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD614P180 with the following fixed options:
 - I/O pin: open drain
 - Oscillator: crystal or ceramic filter oscillator (externally drivable)
 - Divider: Divide by 8
 - Package: standard 42-pin dual in-line ceramic package

Ordering Information

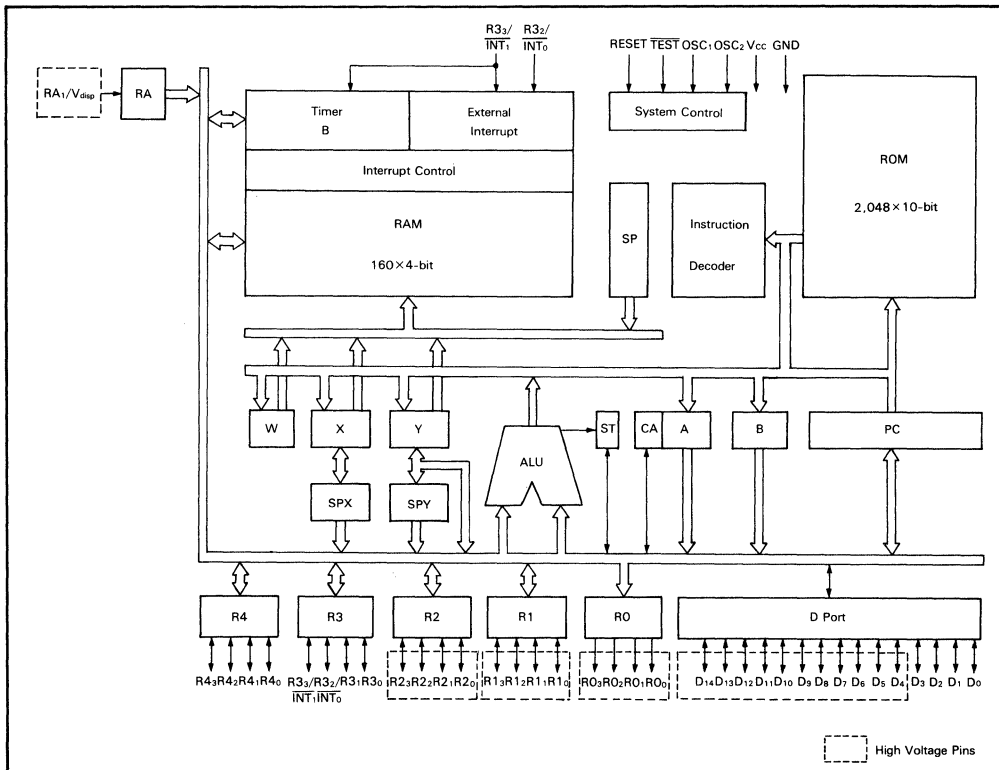
Item	HMCS412C	HMCS412CL	HMCS412AC
Product Name	HD614120	HD614125	HD614128
Power Supply (V)	3.5 to 6	2.5 to 6	4.5 to 6
Typical instruction Cycle Time (μ s)	2	4	1



Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC} - 40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₄ are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁₀–R₁₃, R₂₀–R₂₃, R₃₀–R₃₃, R₄₀–R₄₃, RA₁ (R Ports)

R₀ to R₄ are 4-bit ports. RA is a 1-bit port. R₀ is an output port, RA is an input port, and R₁ to R₄ are I/O ports. R₀, R₁, R₂, and RA are high-voltage ports, and R₃ and R₄ are standard ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, and R₃₃ are multiplexed with INT₀ and INT₁ respectively. For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 2,048 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F can be used for JPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F can be used for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$07FF): Locations \$0000 through \$07FF can be used for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$07FF): Locations from \$0000 to \$07FF can be used for program

code.

RAM Memory Map

The MCU includes 160 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers

HMCS412C/HMCS412CL/HMCS412AC

cannot be accessed by RAM bit manipulation instructions.

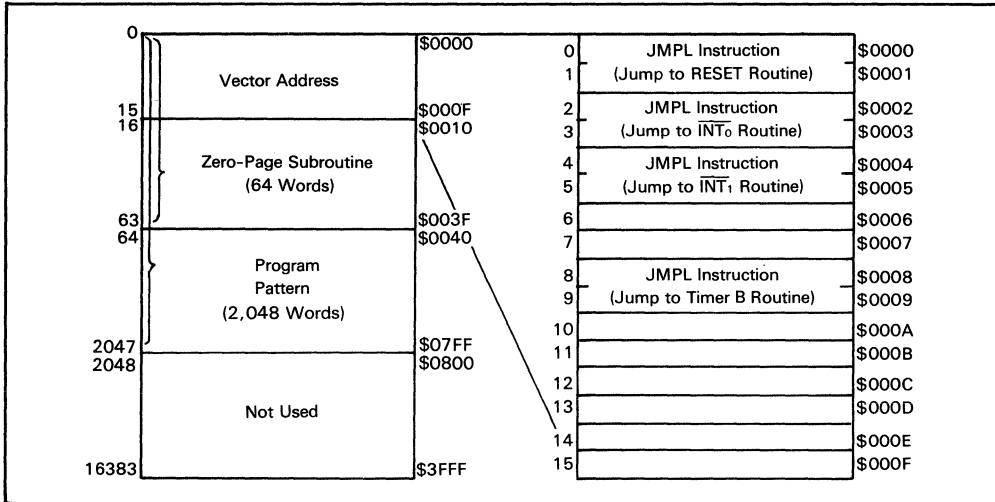


Figure 1. ROM Memory Map

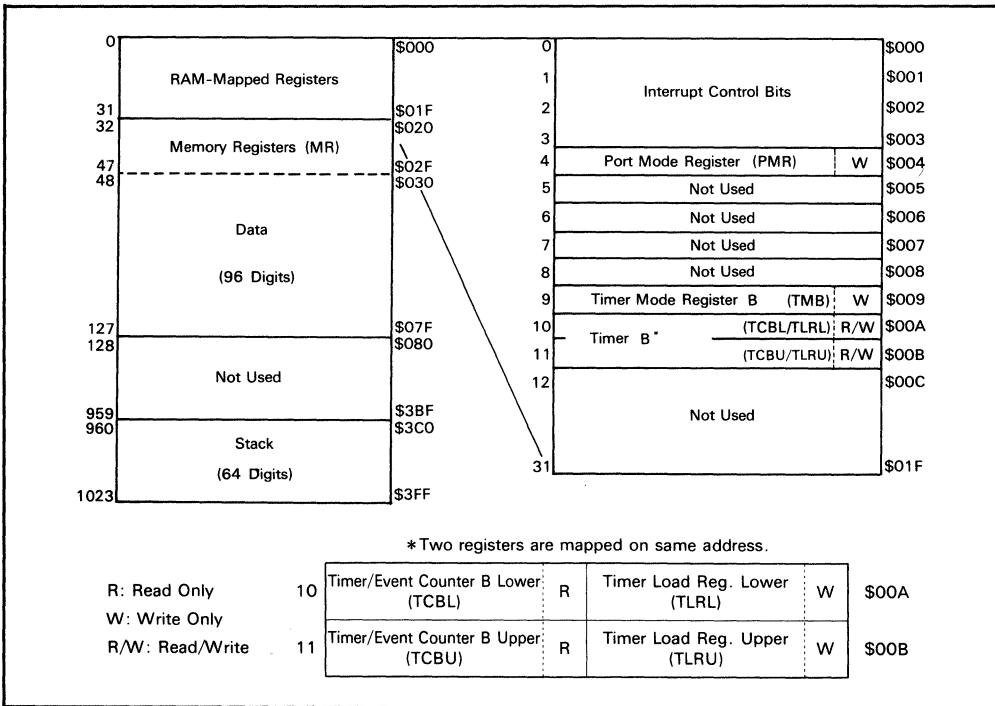


Figure 2. RAM Memory Map



Data Area (\$020 to \$07F): 16 digits of \$020 through \$07F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of \overline{INT}_0)	IFO (IF of \overline{INT}_0)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	Not Used	Not Used	IM1 (IM of \overline{INT}_1)	IF1 (IF of \overline{INT}_1)	\$001
2	Not Used	Not Used	IMTB (IM of Timer B)	IFTB (IF of Timer B)	\$002
3	Not Used	Not Used	Not Used	Not Used	\$003

IF: Interrupt Request Flag
 IM: Interrupt Mask
 I/E: Interrupt Enable Flag
 SP: Stack Pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, is reset by the REM/REMD instruction, and is tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore the interrupt request flag is not affected by the SEM/SEMD instruction.
 The content of status becomes invalid when "Not Used" bit and RSP bit are tested by a TM or TMD instruction.

Figure 3. Configuration of Interrupt Control Bit Area

Memory Registers		Stack Area		
32	MR(0) \$020	960	Level 16	\$3C0
33	MR(1) \$021		Level 15	
34	MR(2) \$022		Level 14	
35	MR(3) \$023		Level 13	
36	MR(4) \$024		Level 12	
37	MR(5) \$025		Level 11	
38	MR(6) \$026		Level 10	
39	MR(7) \$027		Level 9	
40	MR(8) \$028		Level 8	
41	MR(9) \$029		Level 7	
42	MR(10) \$02A		Level 6	
43	MR(11) \$02B		Level 5	
44	MR(12) \$02C		Level 4	
45	MR(13) \$02D		Level 3	
46	MR(14) \$02E		Level 2	
47	MR(15) \$02F	1023	Level 1	\$3FF

PC₁₃ to PC₀: Program Counter
 ST: Status
 CA: Carry

Note: As the HMCS412C/CL/AC have 2k ROM, PC₁₁, PC₁₂ and PC₁₃ are not used.

	bit 3	bit 2	bit 1	bit 0	
1020	ST	PC ₁₃	PC ₁₂	PC ₁₁	\$3FC
1021	PC ₁₀	PC ₉	PC ₈	PC ₇	\$3FD
1022	CA	PC ₆	PC ₅	PC ₄	\$3FE
1023	PC ₃	PC ₂	PC ₁	PC ₀	\$3FF

Figure 4. Configuration of Memory Register, Stack Area, and Stack Position



Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W register is write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

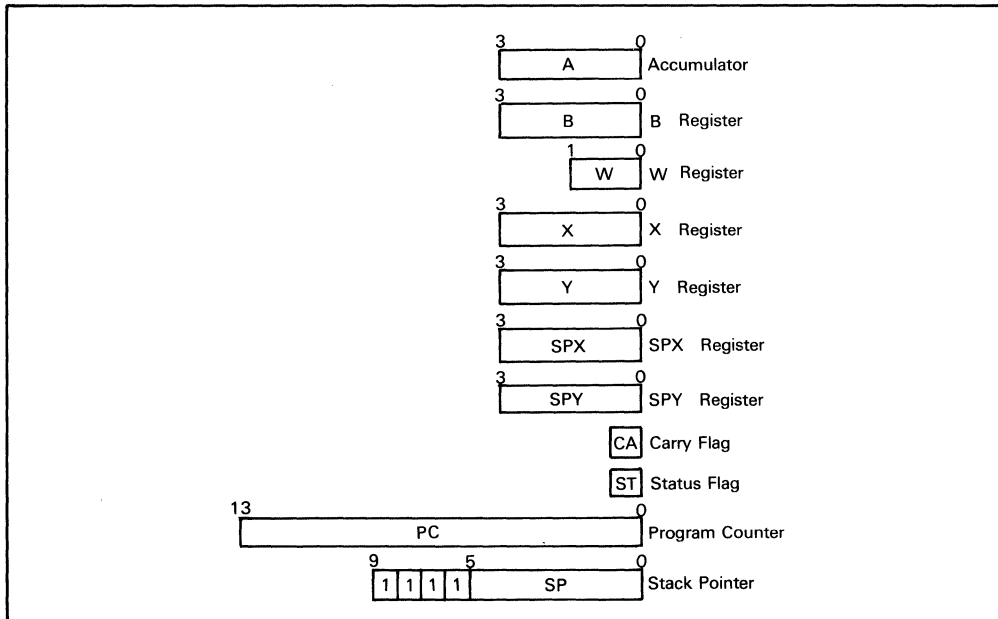


Figure 5. Registers and Flags



The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Three interrupt sources are available on the MCU: external requests (\overline{INT}_0 , \overline{INT}_1), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	-	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer B	3	\$0008

Table 2. Interrupt Service Conditions

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer B
I/E	1	1	1
IFO·IM0	1	0	0
IF1·IM1	*	1	0
IFTB·IMTB	*	*	1

* Don't care

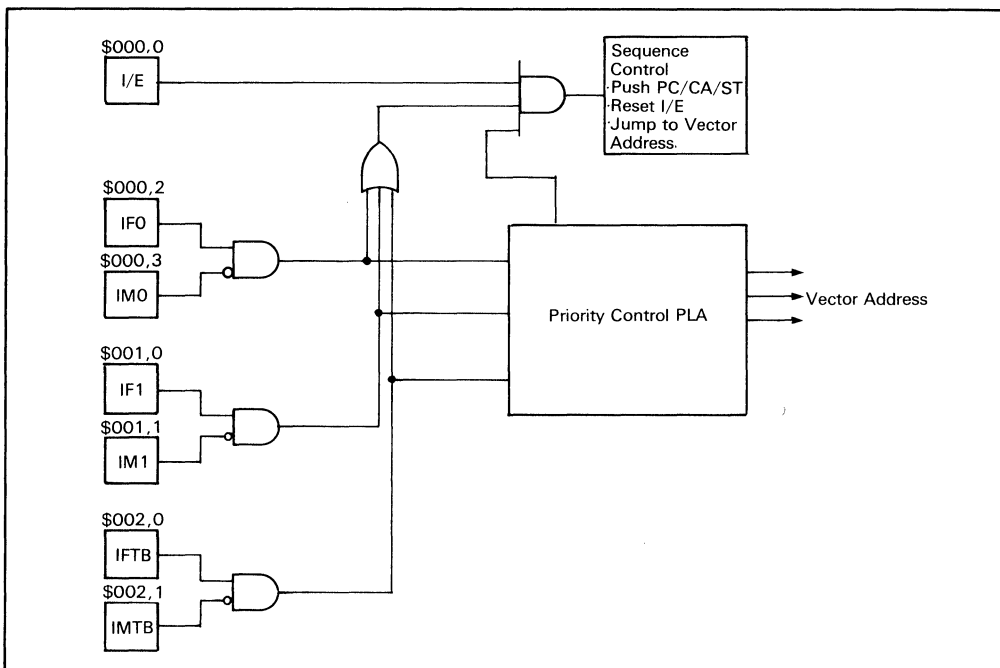


Figure 6. Interrupt Control Circuit Block Diagram



The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): The external interrupt request inputs ($\overline{INT_0}$, $\overline{INT_1}$)

can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT_1}$ pin and $R3_2/\overline{INT_0}$ pin to be used as $\overline{INT_1}$ pin and $\overline{INT_0}$ pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{INT_0}$ and $\overline{INT_1}$ inputs (table 4).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as timer B external event input, the external interrupt mask (IM1) has to be set so that the $\overline{INT_1}$ interrupt request will not be accepted (table 5).

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{INT_0}$, and $\overline{INT_1}$ inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The 4-bit write-only port mode register controls the $R3_2/\overline{INT_0}$ pin, and $R3_3/\overline{INT_1}$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT_1}$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as $\overline{INT_1}$ input pin

PMR2	$R3_2/\overline{INT_0}$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as $\overline{INT_0}$ input pin



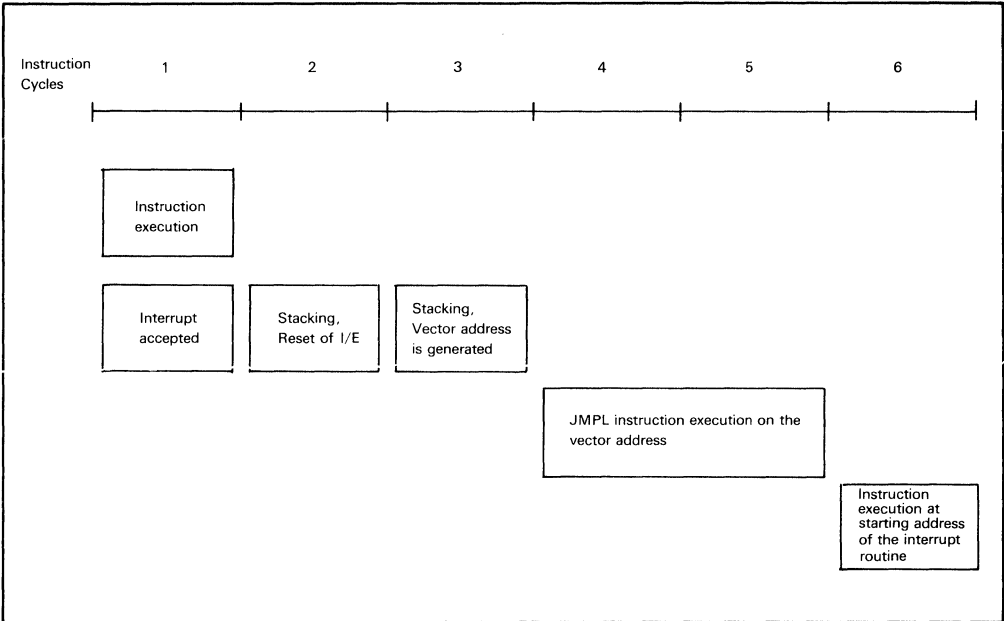


Figure 7. Interrupt Servicing Sequence

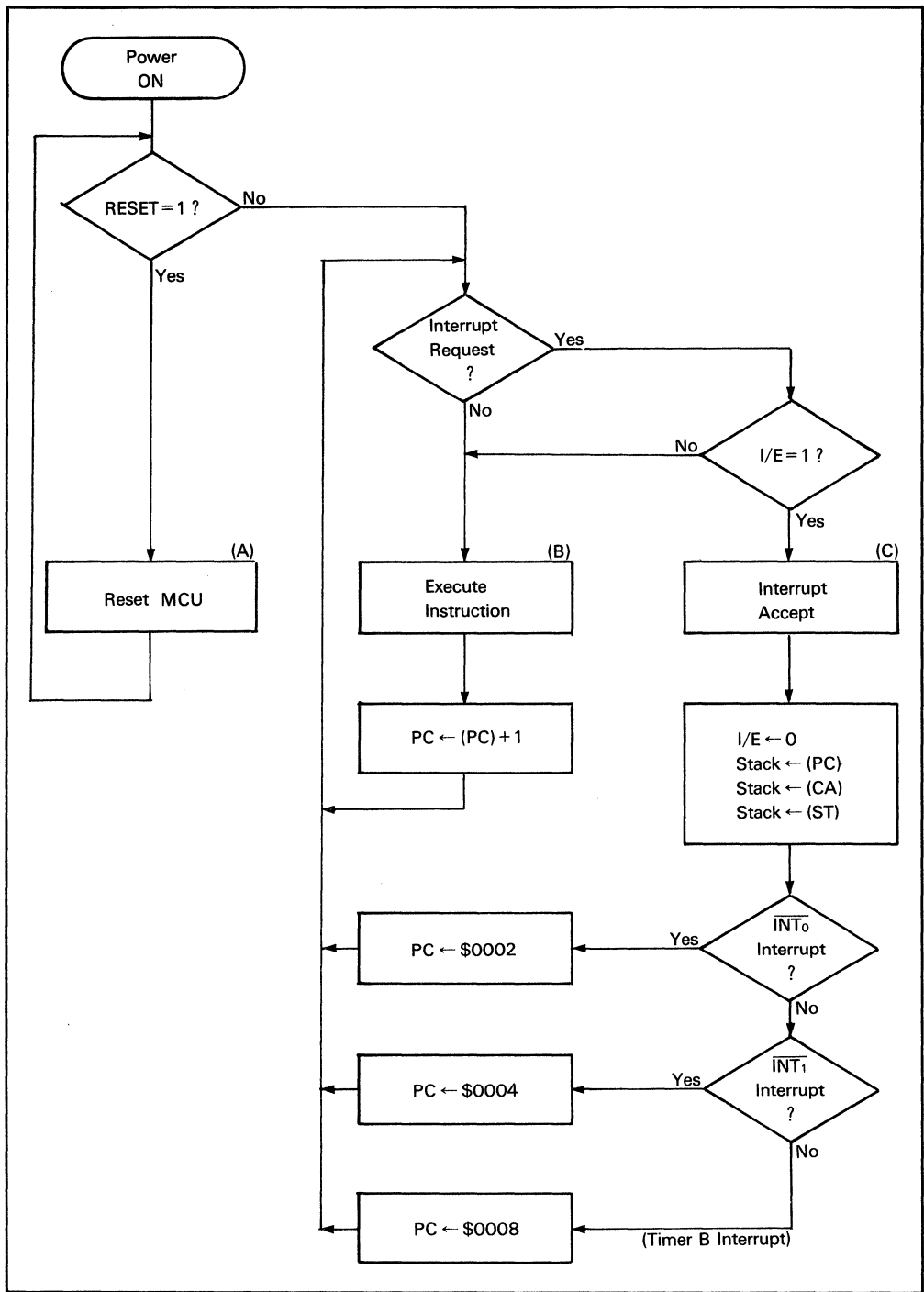


Figure 8. Interrupt Servicing Flowchart



Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as the RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. Then case, if the auto-reload function is selected, timer B is initialized to the value of the timer load register. If it is not selected, timer B goes to \$00. The

timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: \$009): The 4-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: \$00A, TCBU: \$00B, TLR: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: \$00A, TLR: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B) (figure 2).

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then

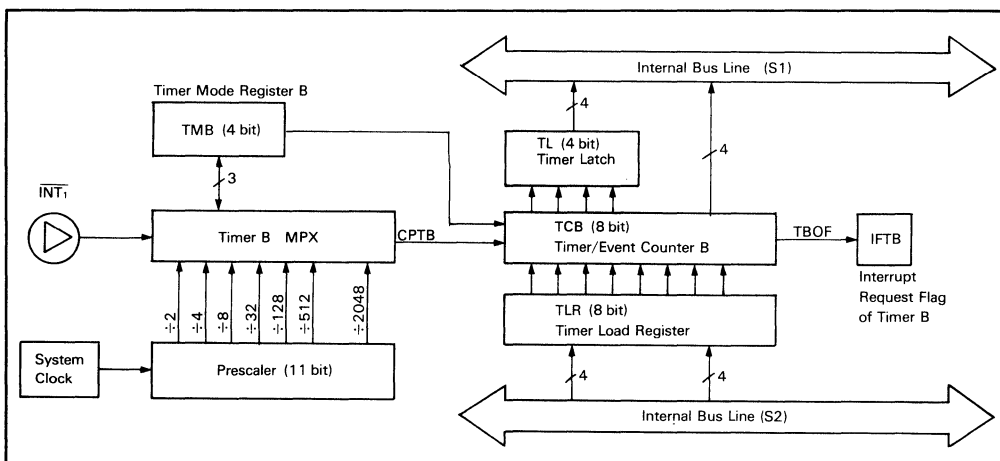


Figure 9. Timer Block Diagram

HMCS412C/HMCS412CL/HMCS412AC

the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B

(table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B Interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3		Auto-reload Function	
0		No	
1		Yes	

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	\overline{INT}_1 (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

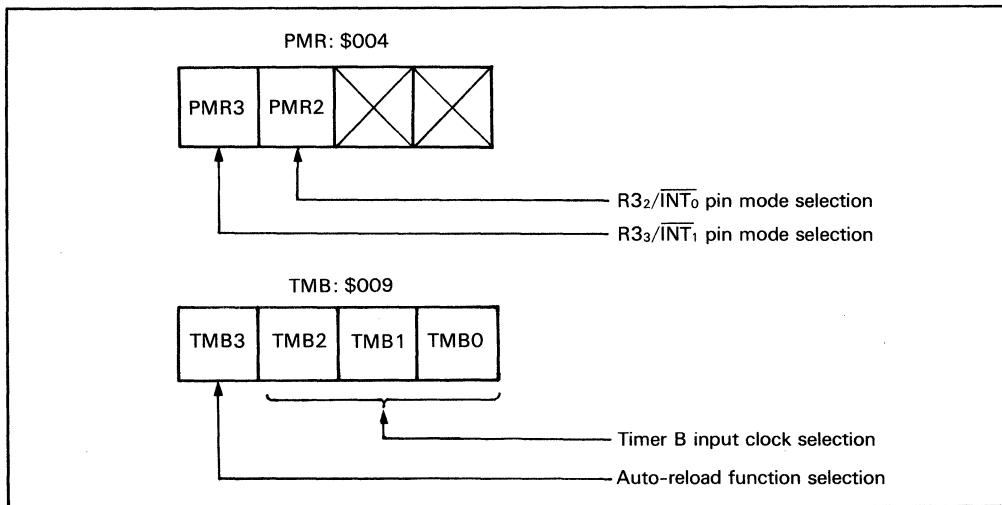


Figure 10. Mode Register Configuration and Function



Input/Output

The MCU has 36 I/O pins, 12 standard and 24 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain). One of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_1/V_{disp} pin via mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 10 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 11.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in Figure 11 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the \overline{HLT} signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D port I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 as for the classification of

standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The six R ports in the HMCS414 are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read from the output-only and/or non-existing ports.

The R_{32} and R_{33} pins are multiplexed with the \overline{INT}_0 and \overline{INT}_1 pins respectively. See table 10 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-up MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 12 shows the parts initialized by MCU reset, and the status of each. Table 13 shows how registers recover from stop mode.

Table 10. I/O Pin Circuit Types

		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable pins
Standard Pins	I/O				D ₀ - D ₃ R ₃₀ - R ₃₃ R ₄₀ - R ₄₃
	Common Pins				

Table 10. I/O Pin Circuit Types (Cont)

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applicable pins
High Voltage Pins	I/O			D ₄ - D ₁₄ R ₁₀ - R ₁₃ R ₂₀ - R ₂₃ R ₀₀ - R ₀₃ R _{A1}
	Output Pins			
	Input Pins			

Table 10. I/O Pin Circuit Types (Cont)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applicable pins
Standard Pins	Input Pins			\overline{INT}_0 \overline{INT}_1

Note: In the stop mode, \overline{HLT} signal is 0, HLT signal is 1 and I/O pins are in high impedance state.



Table 11. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0

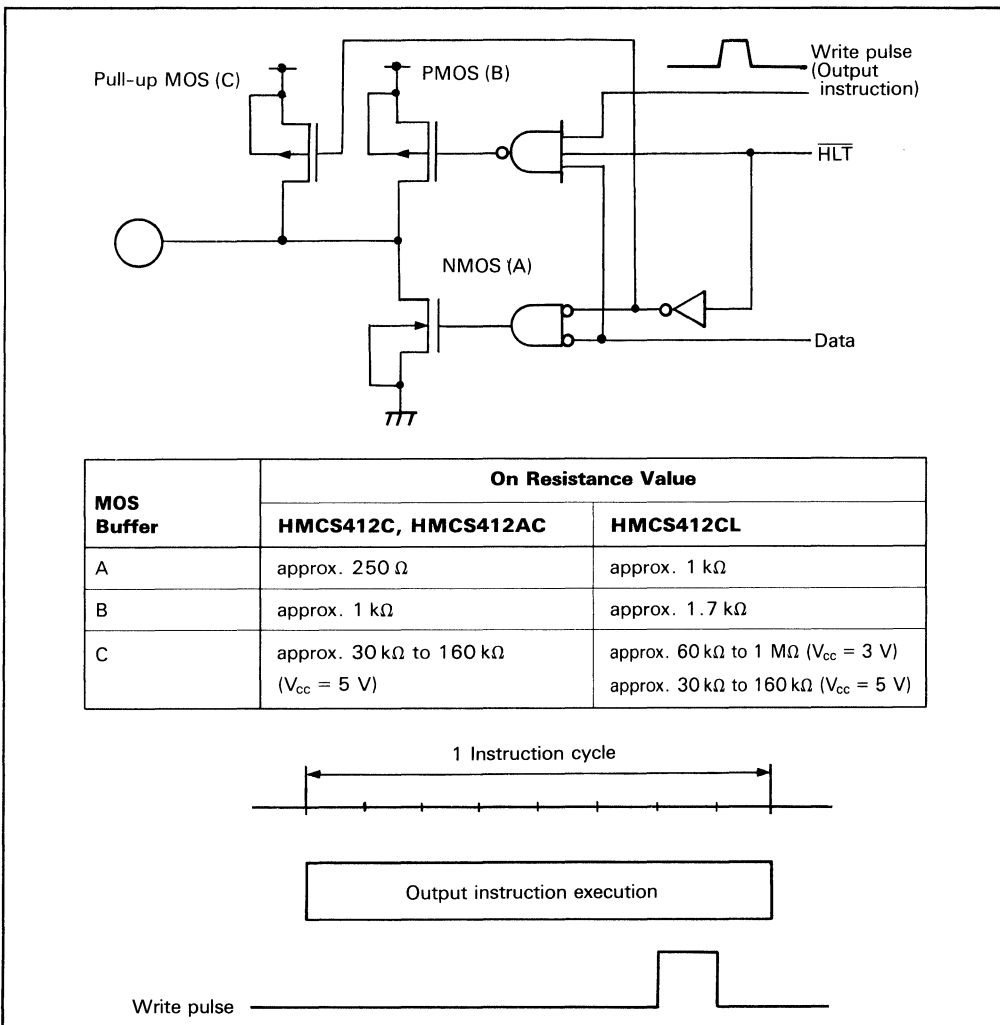


Figure 11. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Table 12. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin (A) Without Pull-Up MOS	1	Enable input
	(B) With Pull-Up MOS	1	Enable input
	(C) CMOS	1	—
	High Voltage Pin (D) Without Pull-Down MOS	0	Enable input
	(E) With Pull-Down MOS	0	Enable input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—

Table 13. Initial Value after Stop Reset

Item		After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop Mode)
Carry	(CA)	The contents of the items before MCU reset are not retained.	
Accumulator	(A)	It is necessary to initialize them by software.	
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. Through mask option, either crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table

15 for selection of the type. In addition, see figure 13 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available. Three divide ratios, 1/16, 1/8, and 1/4, are selectable via mask option (table 14).

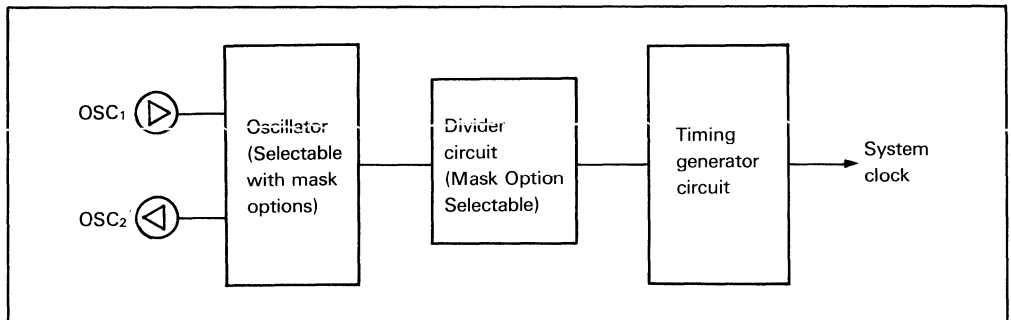


Figure 12. Internal Oscillator Circuit

Table 14. Internal Oscillation Circuit Mask Option

		HMCS 412C	HMCS 412CL	HMCS 412AC
Divider	1/16	—	○	—
	1/8	○	○	—
	1/4	○	—	○
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○

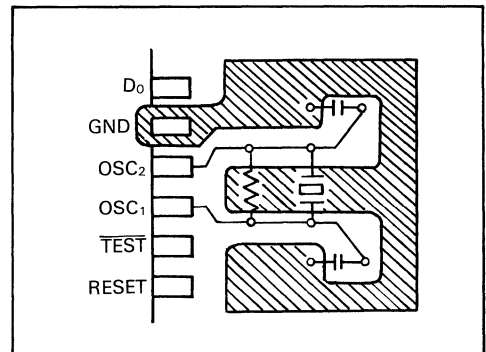


Figure 13. Layout of Crystal and Ceramic Filter

Table 15. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants		
		HMCS412C	HMCS412CL	HMCS412AC
External Clock Operation				
Ceramic Filter Oscillator		Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA4.00MG (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$
Crystal Oscillator	<p>AT cut parallel resonance crystal</p>	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$
	<p>GT cut parallel resonance crystal</p>		$R_f: 2\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}2.25\text{ MHz}$	

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 13).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 16). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 16. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Input/Output Pin	Timer/Counter	Recovery Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained (Note 3)	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET (Note 1)	Stop	Retained	High impedance (Note 2)	Stop	RESET input

- Notes:
1. The MCU recovers from STOP mode by RESET input. Refer to table 13 for the contents of the flags and registers.
 2. A high-voltage pin with a pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is in addition to the current dissipation in stop mode (I_{stop}).
 3. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is in addition to the current dissipation in standby mode.

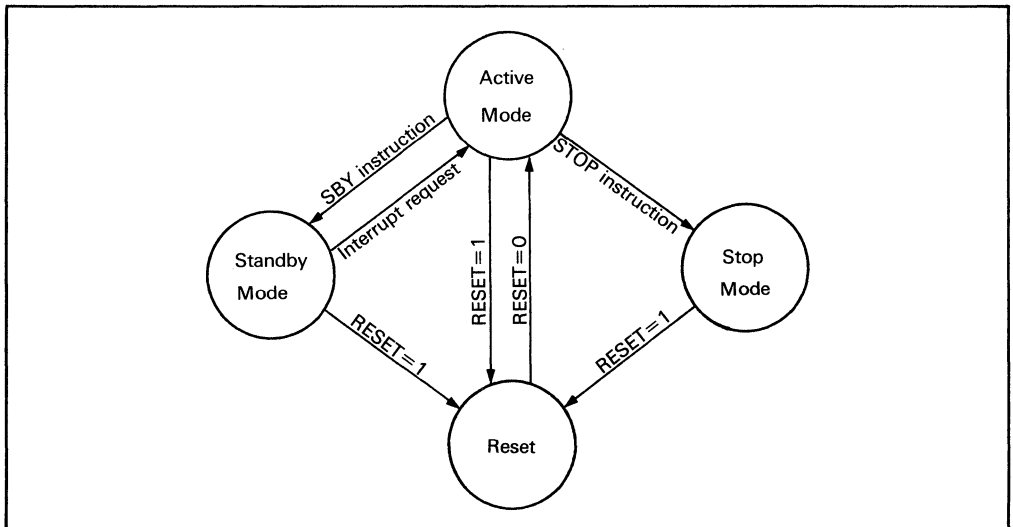


Figure 14. MCU Operation Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 15 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

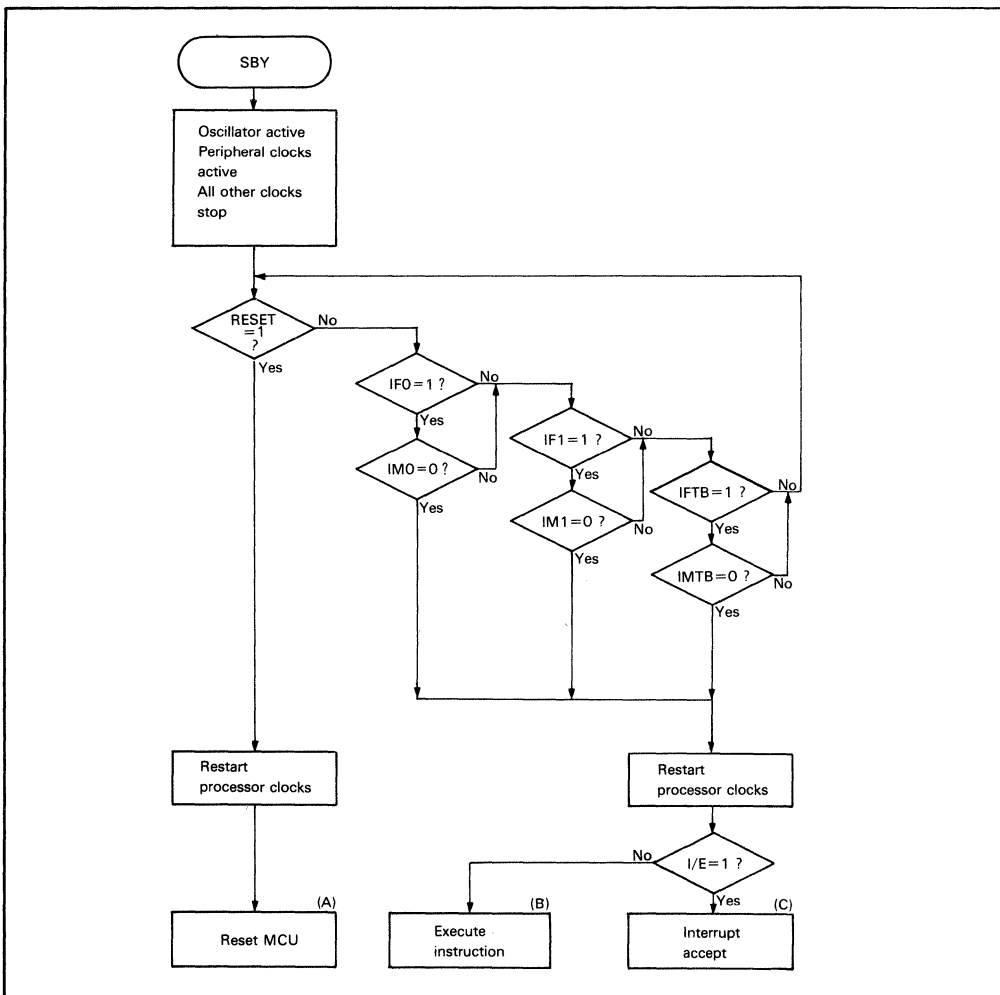


Figure 15. MCU Operating Flowchart in Standby Mode



RAM Addressing Mode

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 18.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 19), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 20). When bit 8 in the ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

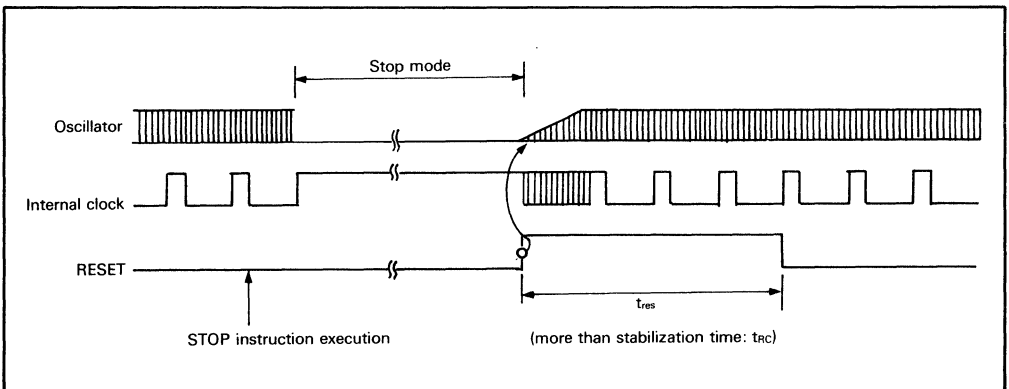


Figure 16. Timing Chart of Recovering from Stop Mode



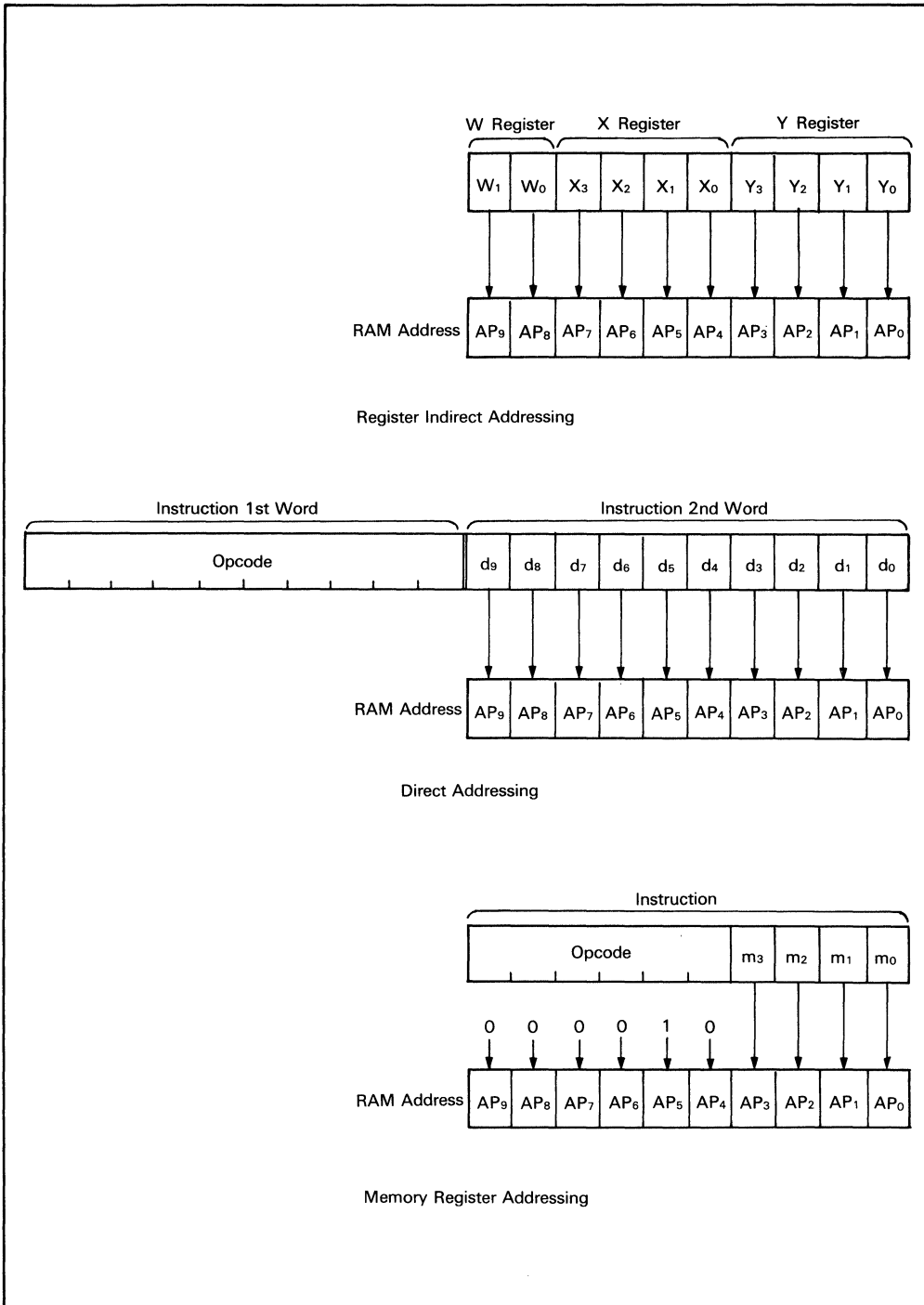


Figure 17. RAM Addressing Mode

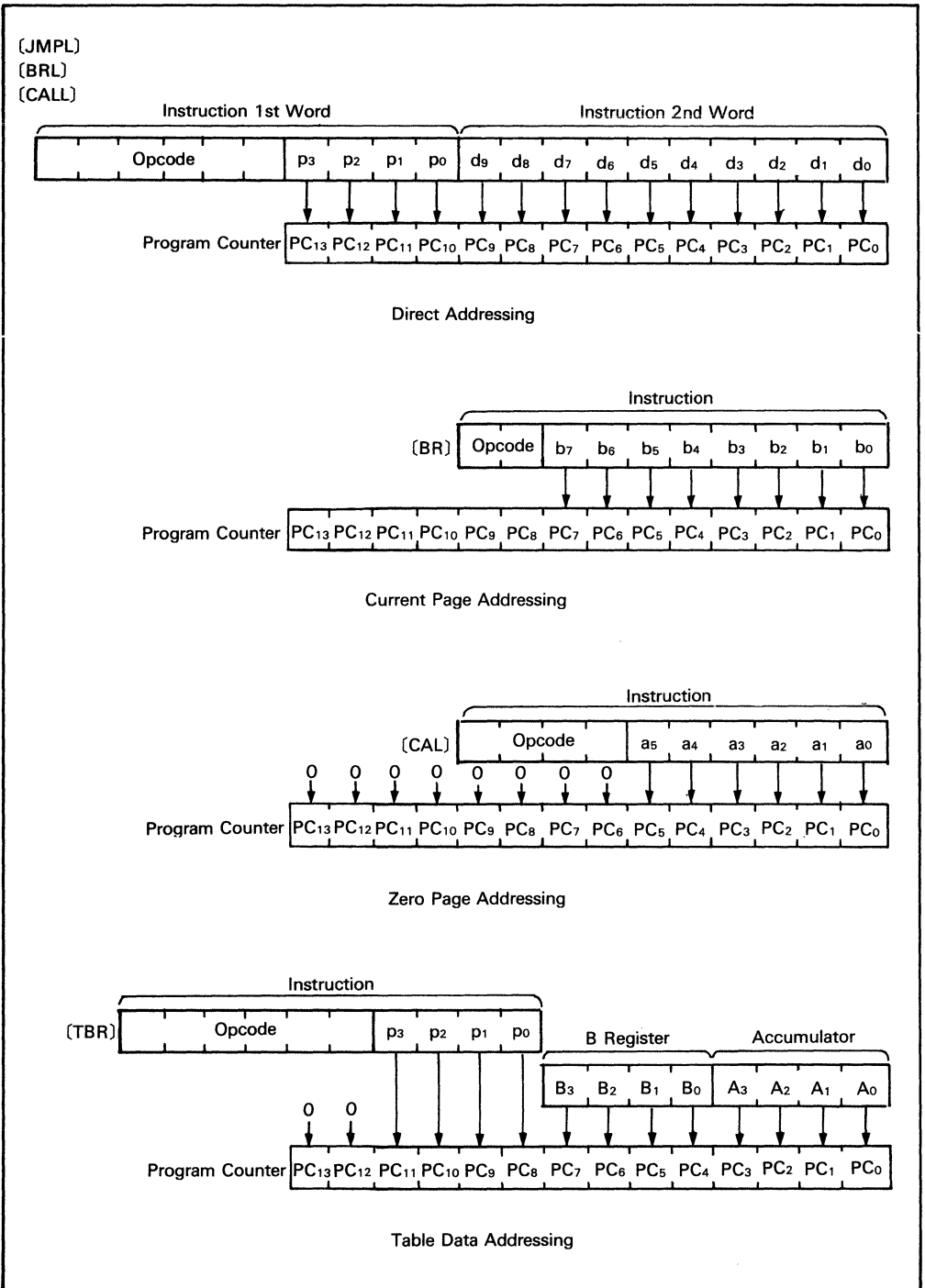


Figure 18. ROM Addressing Mode



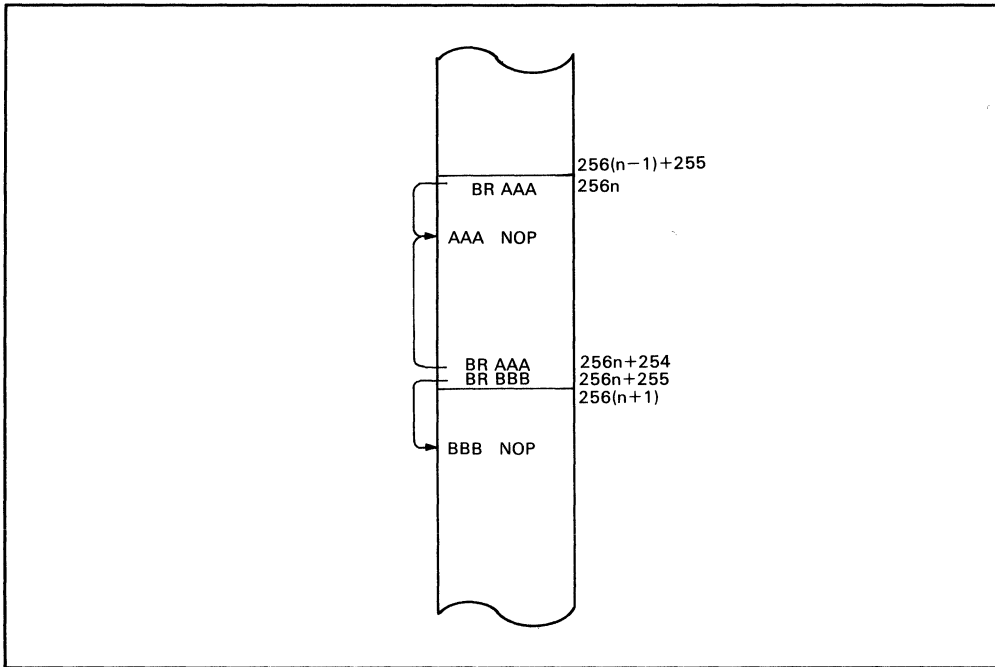


Figure 19. BR Instruction Branch Destination on Pages Boundary

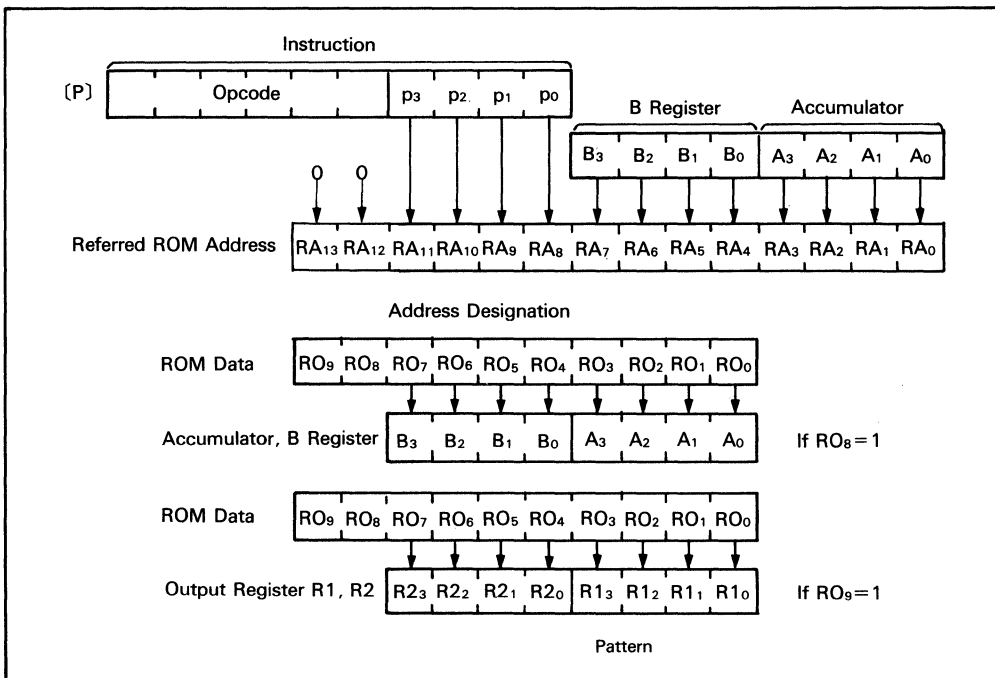


Figure 20. P Instruction



Instruction Set

The HMCS412C/CL/AC provide 98 instructions which are classified into 10 groups as follows:

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 17-26 list their functions, and table 27 is an opcode map.

Table 17. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 18. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B · A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A · B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y · A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX · A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY · A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) · A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1



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Table 19. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 0 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SYX	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Table 20. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X → SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

(2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

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Table 21. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M-A- \bar{CA} →A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M-A- \bar{CA} →A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR



Table 22. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 23. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

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Table 24. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 25. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 26. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: HMCS412 has no serial interface, so STS (start serial) operates the same as NOP.



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Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V	
Terminal Voltage	V_T	- 0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	25	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$- I_O$	4 (2)	mA	9, 10, 13
		6 (3)	mA	9, 11, 13
		30 (15)	mA	9, 12, 13
Total Allowance of Output Current	$-\Sigma I_O$	85 (100)	mA	6, 13
Operating Temperature	T_{opr}	- 20 to + 75	°C	
Storage Temperature	T_{stg}	- 55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. D_0-D_3 , R3 and R4.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. D_0-D_3 , R3 and R4.
 11. R0-R2.
 12. D_4-D_{15} .
 13. $-\Sigma I_O = 100$ mA if $-I_O$ s equal to or less than 2 mA, 3 mA, or 15 mA.

Electrical Characteristics

DC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
HMCS412C: $V_{CC} = 3.5$ V to 6 V,
HMCS412CL: $V_{CC} = 2.5$ V to 6 V,
HMCS412AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, R3 ₂ /INT ₀ , R3 ₃ /INT ₁	0.8 V_{CC}	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	HMCS412C/AC	
			$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	HMCS412CL	
Input Low Voltage	V_{IL}	RESET, R3 ₂ /INT ₀ , R3 ₃ /INT ₁	-0.3	0.2 V_{CC}	V		
		OSC ₁	-0.3	0.5	V	HMCS412C/AC	
			-0.3	0.3	V	HMCS412CL	
Input/Output Leakage Current	$ I_{II} $	RESET, R3 ₂ /INT ₀ , R3 ₃ /INT ₁ , OSC ₁		1	μA	$V_{in} = 0$ V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		1.8	mA	HMCS412C; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	2.5
				0.8	mA	HMCS412CL; $V_{CC} = 3$ V; $f_{osc} = 4$ MHz, $\div 16$, or $f_{osc} = 2$ MHz, $\div 8$	2.5
				3.0	mA	HMCS412AC; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 4$	2.5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		1.0	mA	HMCS412C; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	3.5
				0.5	mA	HMCS412CL; $V_{CC} = 3$ V; $f_{osc} = 4$ MHz, $\div 16$, or $f_{osc} = 2$ MHz, $\div 8$	3.5
				1.4	mA	HMCS412AC; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 4$	3.5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		10	μA	$V_{in}(\text{TEST}) = V_{CC} - 0.3$ V to V_{CC} ; V_{CC} , $V_{in}(\text{RESET}) = 0$ V to 3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

Notes: 1. Excluding pull-up MOS current and output buffer current.

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- Notes:
- The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When $f_{osc} = x$ MHz, estimate the current dissipation as follows:
 HMCS412C/AC; Max value @ x MHz = $x/4 \times$ (max value @ 4 MHz)
 HMCS412CL; Max value @ x MHz = $x/2 \times$ (max value @ 2 MHz)

Input/Output Characteristics for Standard Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$,
 HMCS412C: $V_{CC} = 3.5$ V to 6 V,
 HMCS412CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS412AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	-0.3		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	$V_{CC} - 1.0$			V	HMCS412C/AC; - $I_{OH} = 1.0$ mA	1
		D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	$V_{CC} - 0.5$			V	HMCS412C/AC; - $I_{OH} = 0.5$ mA HMCS412CL; - $I_{OH} = 0.3$ mA	1
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄			0.4	V	HMCS412C/AC; $I_{OL} = 1.6$ mA HMCS412CL; $I_{OH} = 0.4$ mA	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄			1	μA	$V_{in} = 0$ V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	30	60	150	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	3
		D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	3	15	50	μA	HMCS412CL only; $V_{CC} = 3$ V, $V_{in} = 0$ V	3

- Notes:
- I/O pins with CMOS output selected by mask option.
 - Pull-up MOS current and output buffer current are excluded.
 - I/O pins with pull-up MOS selected by mask option.



Input/Output Characteristics for High-Voltage Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
HMCS412C: $V_{CC} = 3.5$ V to 6 V,
HMCS412CL: $V_{CC} = 2.5$ V to 6 V,
HMCS412AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D4-D14, R1, R2, RA1	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D4-D14, R1, R2, RA1	$V_{CC} - 40$		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D4-D14	$V_{CC} - 3.0$			V	$- I_{OH} = 15$ mA, HMCS412C/CL; $V_{CC} = 5$ V \pm 20% HMCS412AC; $V_{CC} = 4.5$ V to 6 V	
			$V_{CC} - 2.0$			V	$- I_{OH} = 10$ mA, HMCS412C/CL; $V_{CC} = 5$ V \pm 20% HMCS412AC; $V_{CC} = 4.5$ V to 6 V	
			$V_{CC} - 1.0$			V	HMCS412C/AC; $- I_{OH} = 4$ mA HMCS412CL; $- I_{OH} = 2.5$ mA	
		R0-R2	$V_{CC} - 3.0$			V	$- I_{OH} = 3$ mA, HMCS412C/CL; $V_{CC} = 5$ V \pm 20% HMCS412AC; $V_{CC} = 4.5$ V to 6 V	
			$V_{CC} - 2.0$			V	$- I_{OH} = 2$ mA, HMCS412C/CL; $V_{CC} = 5$ V \pm 20% HMCS412AC; $V_{CC} = 4.5$ V to 6 V	
			$V_{CC} - 1.0$			V	HMCS412C/AC; $- I_{OH} = 0.8$ mA HMCS412CL; $- I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	D4-D14, R0-R2			$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40$ V	1
					$V_{CC} - 37$	V	150k Ω to $V_{CC} - 40$ V	2
Input/Output Leakage Current	$ I_{II} $	D4-D14, R0-R2, RA1		20		μA	$V_{in} = V_{CC} - 40$ V to V_{CC}	3
Pull-Down MOS Current	I_d	D4-D14, R0-R2, RA1	125	250	600	μA	$V_{disp} = V_{CC} - 35$ V, $V_{in} = V_{CC}$	4

- Notes:
1. I/O pins with pull-down MOS selected by mask option.
 2. I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. I/O pins with pull-down MOS selected by mask option.

HMCS412C/HMCS412CL/HMCS412AC

AC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
HMCS412C: $V_{CC} = 3.5$ V to 6 V,
HMCS412CL: $V_{CC} = 2.5$ V to 6 V,
HMCS412AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	HMCS412C; divide by 8	
			0.2	2	2.25	MHz	HMCS412C; divide by 4	
			0.8	4	4.5	MHz	HMCS412CL; divide by 16	
			0.4	2	2.25	MHz	HMCS412CL; divide by 8	
			0.2	4	4.5	MHz	HMCS412AC; divide by 4	
Instruction Cycle Time	t_{cyc}		1.78	2	20	μs	HMCS412C	
			3.55	4	20	μs	HMCS412CL	
			0.89	1	20	μs	HMCS412AC	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms	HMCS412C/AC	1
					60	ms	HMCS412CL	1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	HMCS412C; divide by 8 HMCS412CL; divide by 16 HMCS412AC; divide by 4	2
			203			ns	HMCS412C; divide by 4 HMCS412CL; divide by 8	2

(continued)



AC Characteristics (Cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CpF}	OSC ₁			20	ns		2
\overline{INT}_0 High Level Width	t_{i0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{i0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$	
RESET Fall Time	t_{RSTF}				20	ms	HMCS412C/AC	4
					15	ms	HMCS412CL	4

- Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (HMCS412C; 3.5 V, HMCS412CL; 2.5 V, HMCS412AC; 4.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 21.)
 2. See figure 22.
 3. See figure 23.
 4. See figure 24.

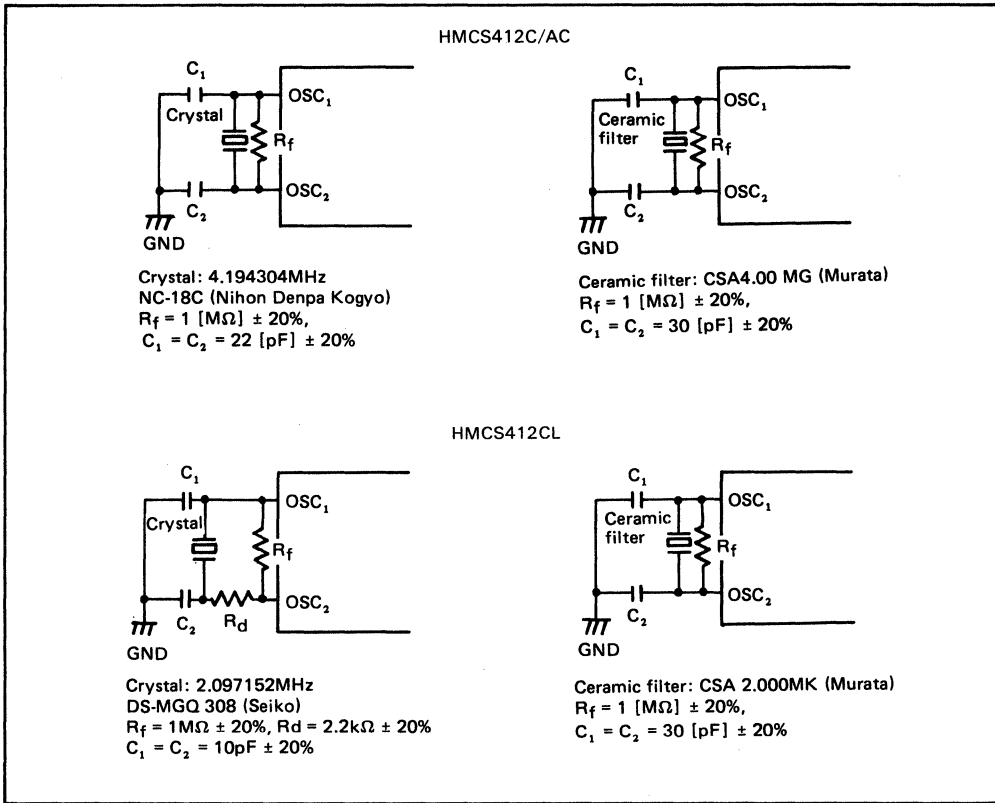


Figure 21. Oscillation Circuit

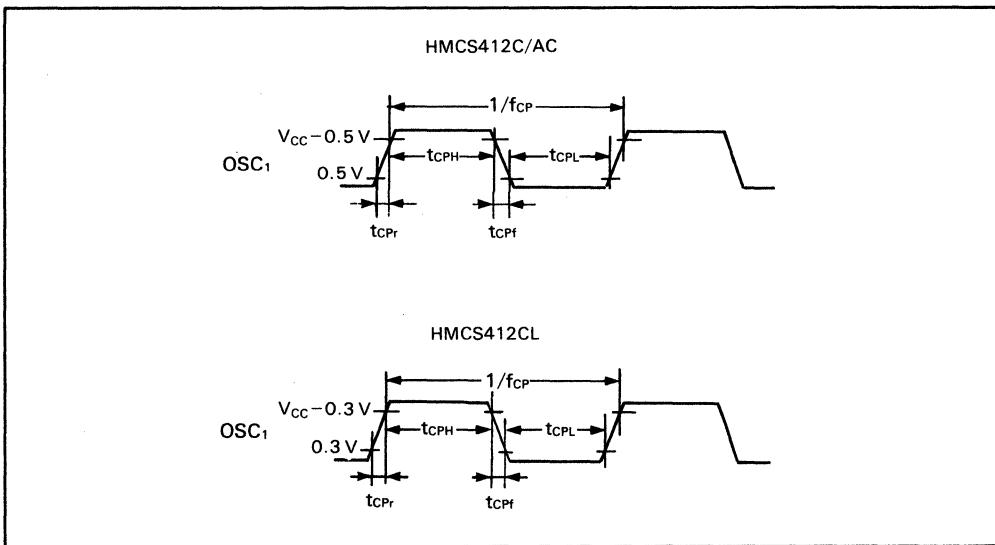


Figure 22. Oscillator Timing

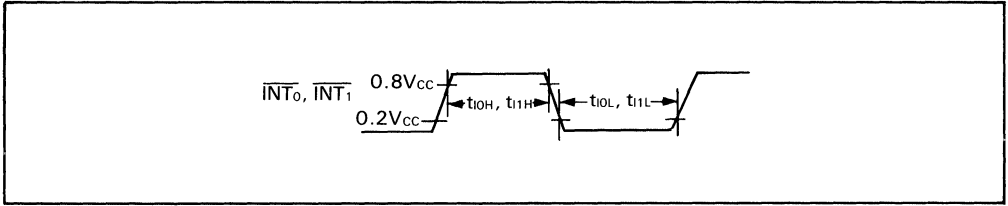


Figure 23. Interrupt Timing

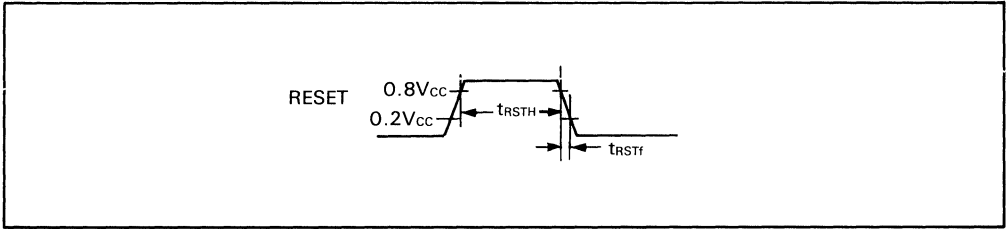


Figure 24. Reset Timing

HMCS412C/HMCS412CL/HMCS412AC

HMCS412C/CL/AC Mask Option List

* Please enter check marks in
(■, x, √).

5V Operation:	<input type="checkbox"/> HMCS412C
3V Operation:	<input type="checkbox"/> HMCS412CL
High Speed Operation:	<input type="checkbox"/> HMCS412AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

(1) I/O Option

Please enter 0 in applicable item to select I/O option.

- A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
C: CMOS (cannot be used as input) D: Without Pull-down MOS (PMOS Open Drain) E: With Pull-down MOS

Note: I/O options masked by ■ are not available.

Pin	Input/Output	I/O Option					Pin	Input/Output	I/O Option						
		A	B	C	D	E			A	B	C	D	E		
D ₀	Standard Pins Input/Output				■	■	R0	RO ₀	Output	■	■	■			
D ₁					■	■		RO ₁	Output	■	■	■			
D ₂					■	■		RO ₂	Output	■	■	■			
D ₃					■	■		RO ₃	Output	■	■	■			
D ₄	High Voltage Pins Input/Output	■	■	■			R1	R1 ₀	Input/Output	■	■	■			
D ₅		■	■	■				R1 ₁	Input/Output	■	■	■			
D ₆		■	■	■				R1 ₂	Input/Output	■	■	■			
D ₇		■	■	■				R1 ₃	Input/Output	■	■	■			
D ₈		High Voltage Pins Input/Output	■	■	■			R2	R2 ₀	Input/Output	■	■	■		
D ₉			■	■	■				R2 ₁	Input/Output	■	■	■		
D ₁₀			■	■	■				R2 ₂	Input/Output	■	■	■		
D ₁₁			■	■	■			R3	R2 ₃	Input/Output	■	■	■		
D ₁₂			■	■	■				R3 ₀	Input/Output				■	■
D ₁₃			■	■	■				R3 ₁	Input/Output				■	■
D ₁₄	■	■	■			Standard Pins Input/Output	R3 ₂	Input/Output				■	■		
							R3 ₃	Input/Output				■	■		
							R4	R4 ₀	Input/Output				■	■	
								R4 ₁	Input/Output				■	■	
								R4 ₂	Input/Output				■	■	
						R4 ₃	Input/Output				■	■			
RA	RA ₁						High Voltage Input	Input	Please Mark as RA ₁ /V _{disp}						



(2) RA₁/V_{disp}

Please check (■, X, ✓) applicable item.

RA ₁ /V _{disp}	
<input type="checkbox"/>	RA ₁ : Without Pull-down MOS (D)
<input type="checkbox"/>	V _{disp}

Note: RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high pins are option D.

(3) Divider (Div)

Please check (■, X, ✓) applicable item.

Divider	HMCS412C	HMCS412CL	HMCS412AC
16	■	<input type="checkbox"/>	■
8	<input type="checkbox"/>	<input type="checkbox"/>	■
4	<input type="checkbox"/>	■	<input type="checkbox"/>

(4) ROM Code Media

Please check (■, X, ✓) applicable item.

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

(5) Oscillator (CPG option)

Please check (■, X, ✓) applicable item.

CPG option	<input type="checkbox"/> HMCS 412C (5V Operation)	<input type="checkbox"/> HMCS412CL (3V Operation)	<input type="checkbox"/> HMCS412AC (High Speed Operation)
	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock



HMCS414C/HMCS414CL/ — HMCS414AC (HD614140/HD614145/HD614148)

Description

The HMCS414C/CL/AC are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins to drive a fluorescent display directly.

Features

- 4-bit architecture
- 4096 words of 10-bit ROM
- 160 digits of 4-bit RAM
- 36 I/O pins, including 24 high-voltage I/O pins (40 V max)
- Timer/counter
 - 11-bit prescaler
 - 8-bit auto-reload timer/event counter (timer B)
- Three interrupt sources
 - External: 2
 - Timer/counter: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time
 - 0.89 μ s: HMCS414AC
 - 1.78 μ s: HMCS414C
 - 3.55 μ s: HMCS414CL
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Crystal or ceramic filter
 - External clock input
- Package
 - Standard 42-pin dual in-line plastic package
 - 42-pin shrink dual in-line plastic package
 - 44-pin flat plastic package

- Instruction set compatible with HMCS412; 98 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

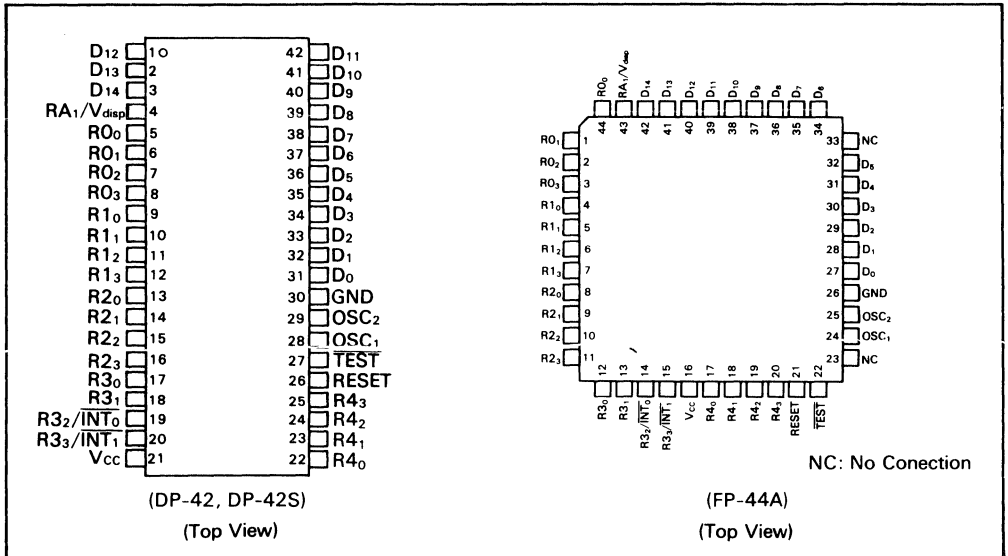
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD614P180 with the following fixed options:
 - I/O pin: open drain
 - Oscillator: crystal or ceramic filter oscillator (externally drivable)
 - Divider: Divide by 8
 - Package: standard 42-pin dual in-line ceramic package

Ordering Information

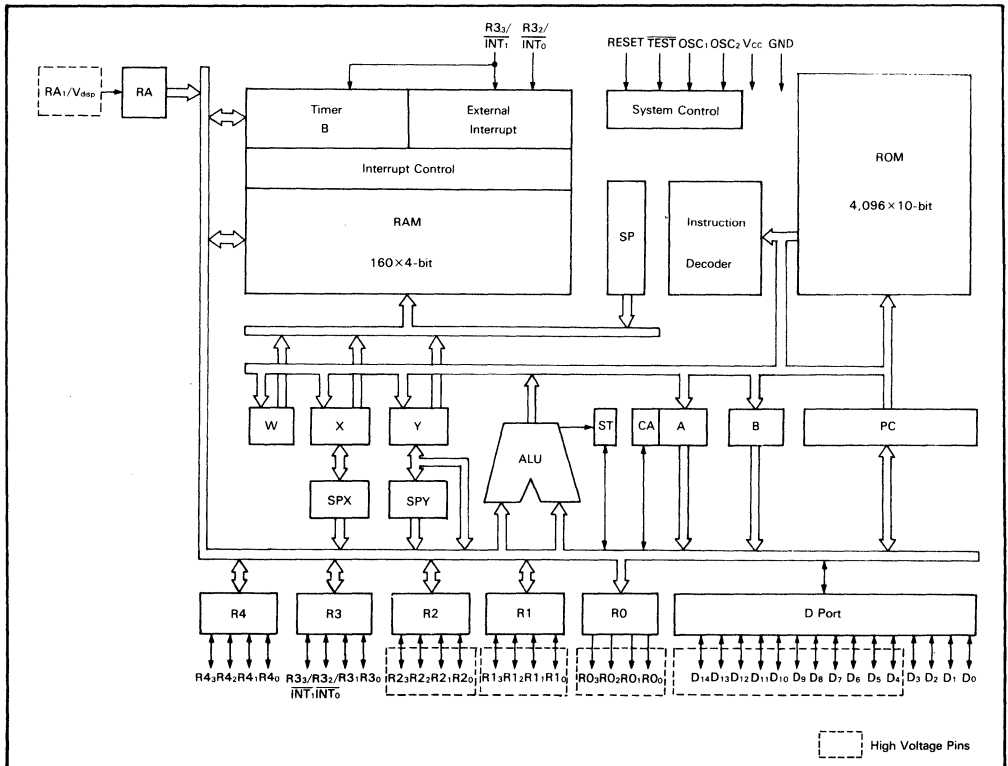
Item	HMCS414C	HMCS414CL	HMCS414AC
Product Name	HD614140	HD614145	HD614148
Power Supply (V)	3.5 to 6	2.5 to 6	4.5 to 6
Typical instruction Cycle Time (μ s)	2	4	1



Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC}–40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₄ are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁–R₁₃, R₂–R₂₃, R₃–R₃₃, R₄–R₄₃, RA₁ (R Ports)

R₀ to R₄ are 4-bit ports. RA is a 1-bit port. R₀ is an output port, RA is an input port, and R₁ to R₄ are I/O ports. R₀, R₁, R₂, and RA are high-voltage ports, and R₃ and R₄ are standard ports. Each pin has a mask option which selects its circuit type. The pins R₃₂ and R₃₃ are multiplexed with INT₀ and INT₁ respectively. For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 4,096 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F can be used for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F can be used for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF can be used for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$0FFF): Locations from \$0000 to \$0FFF can be used for

program code.

RAM Memory Map

The MCU includes 160 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers



cannot be accessed by RAM bit manipulation instructions.

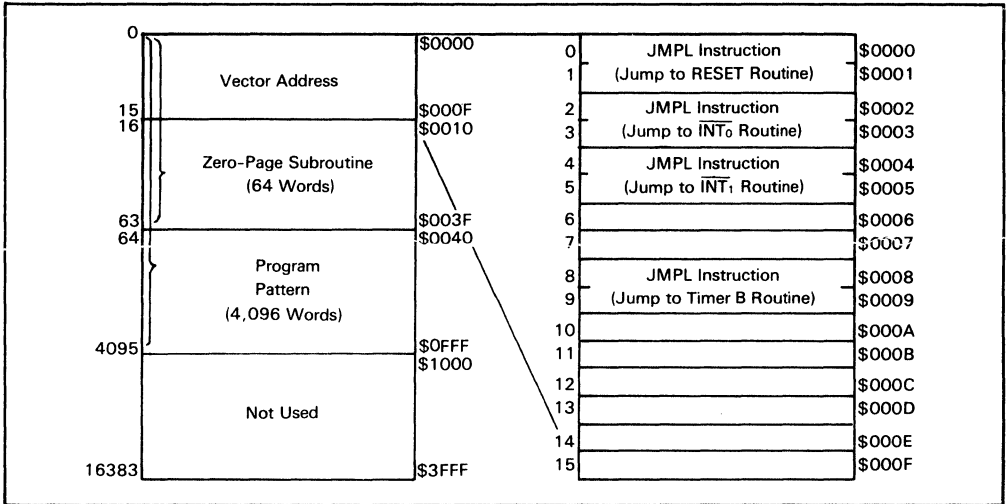


Figure 1. ROM Memory Map

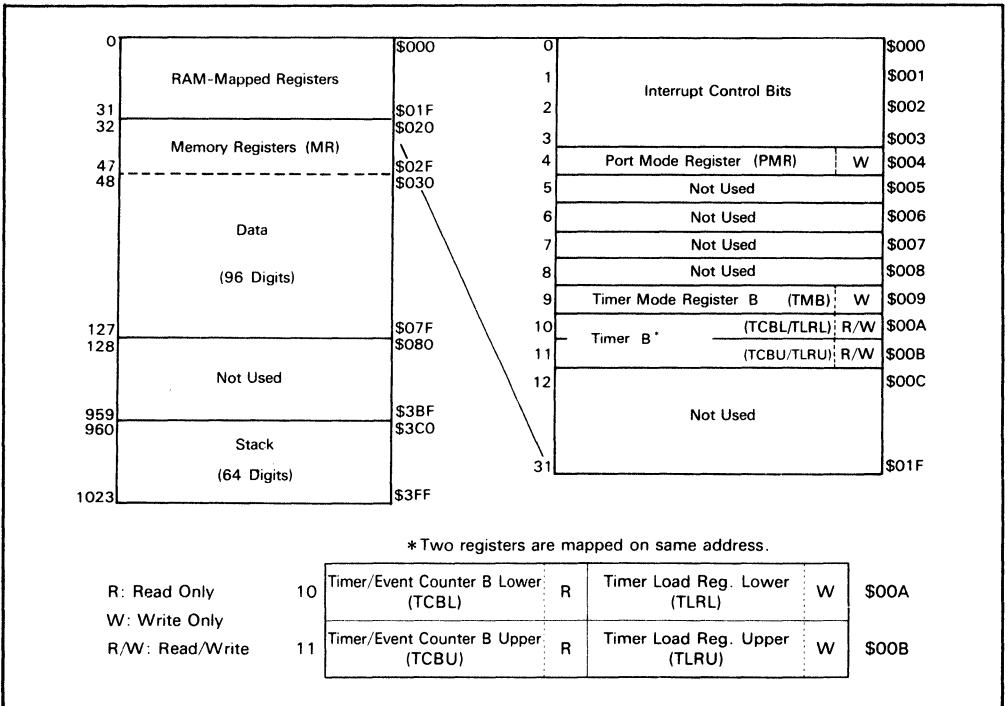


Figure 2. RAM Memory Map



HMCS414C/HMCS414CL/HMCS414AC

Data Area (\$020 to \$07F): 16 digits of \$020 through \$02F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

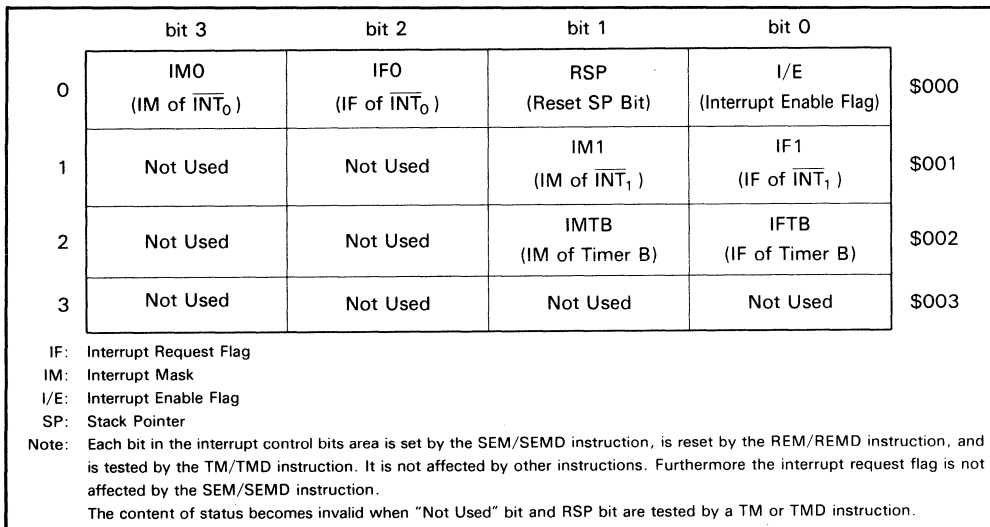


Figure 3. Configuration of Interrupt Control Bit Area

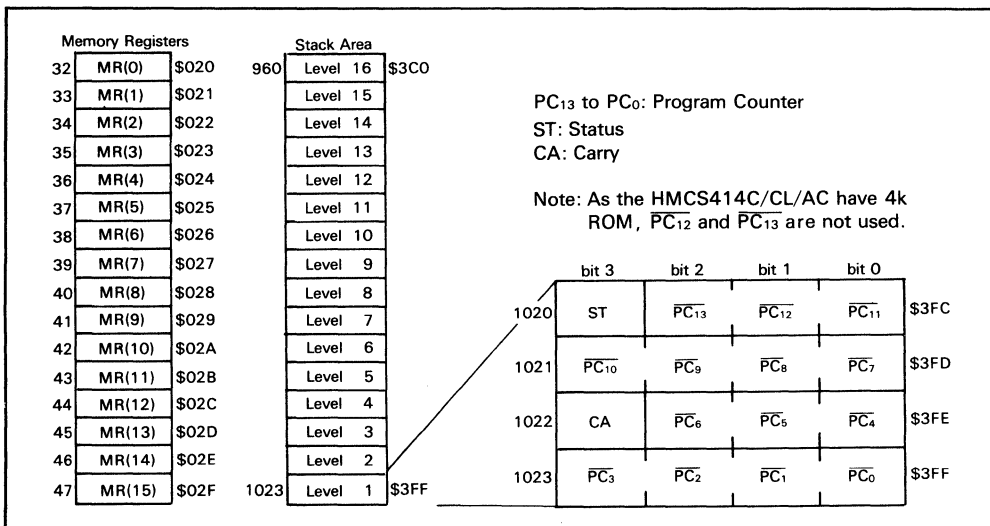


Figure 4. Configuration of Memory Register, Stack Area, and Stack Position



Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W register is write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

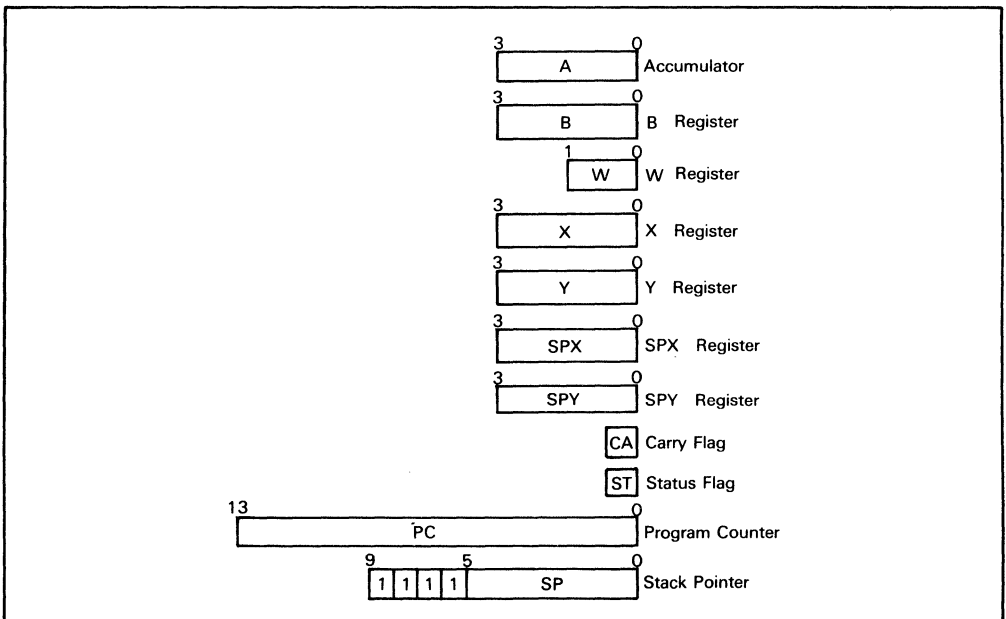


Figure 5. Registers and Flags



The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Three interrupt sources are available on the MCU: external requests (\overline{INT}_0 , \overline{INT}_1), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service:

The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	-	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer B	3	\$0008

Table 2. Interrupt Service Conditions

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer B
I/E	1	1	1
IFO·IMO	1	0	0
IF1·IM1	*	1	0
IFTB·IMTB	*	*	1

* Don't care

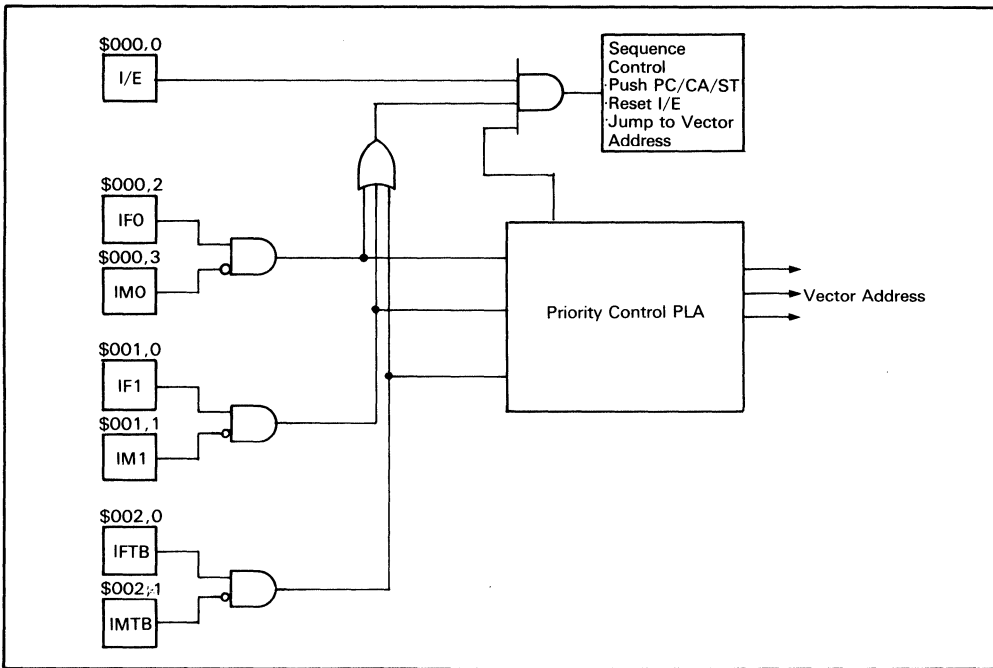


Figure 6. Interrupt Control Circuit Block Diagram



The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1)

can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs (table 4).

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, the external interrupt mask (IM1) has to be set so that the \overline{INT}_1 interrupt request will not be accepted (table 5).

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The 4-bit write-only port mode register controls the $R3_2/\overline{INT}_0$ pin, and $R3_3/\overline{INT}_1$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin

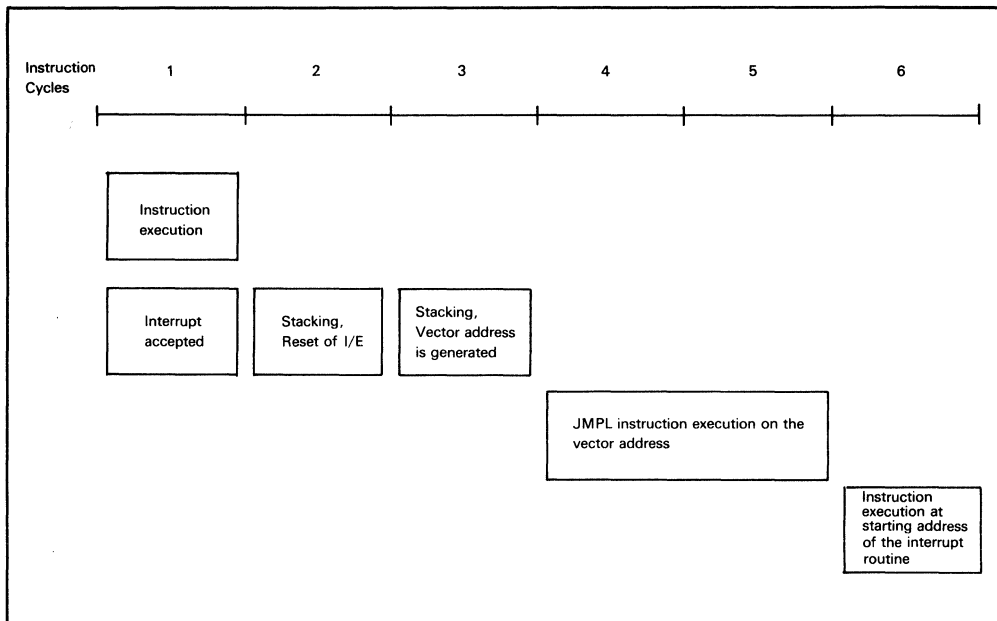


Figure 7. Interrupt Servicing Sequence

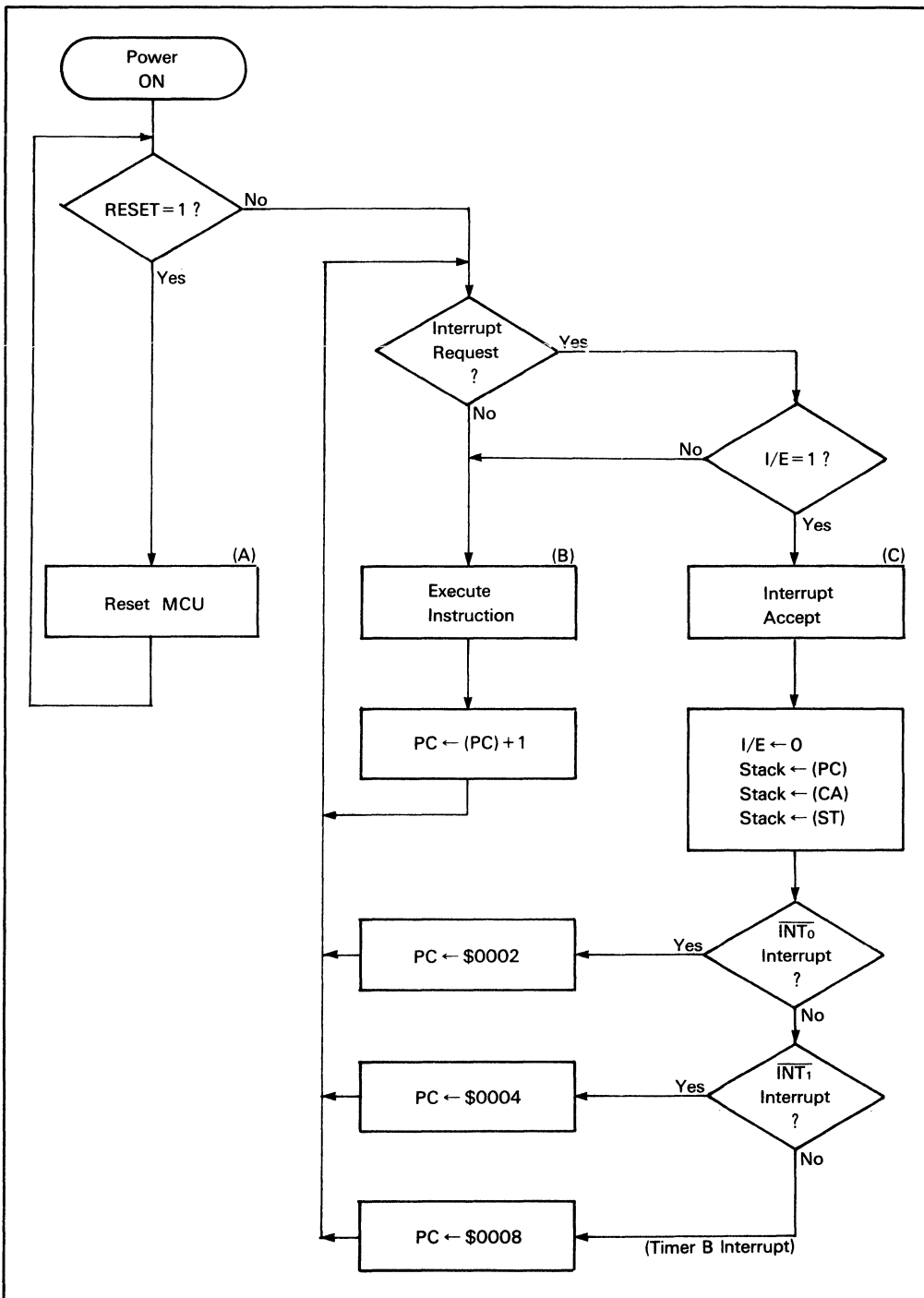


Figure 8. Interrupt Servicing Flowchart



Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as the RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. Then case, if the auto-reload function is selected, timer B is initialized to the value of the timer load register. If it is not selected, timer B goes to \$00. The

timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: \$009): The 4-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B) (figure 2).

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then

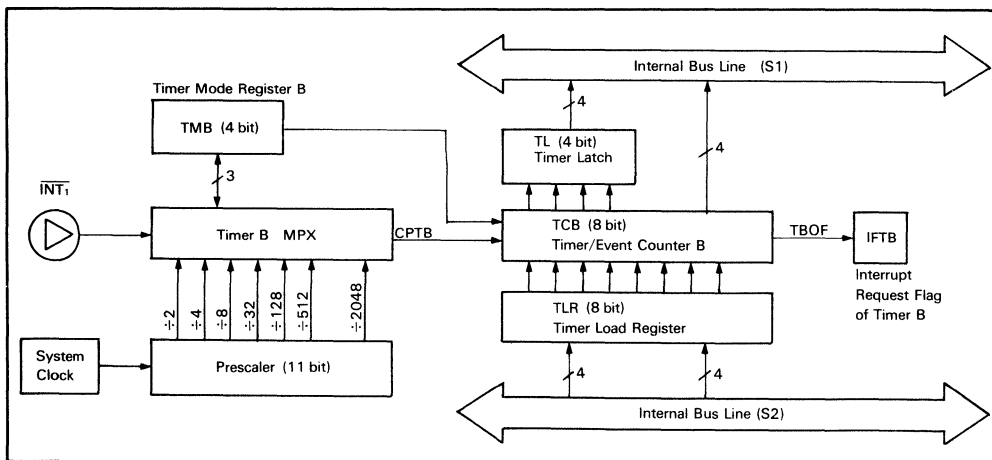


Figure 9. Timer Block Diagram



the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B

(table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B Interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	\overline{INT}_1 (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

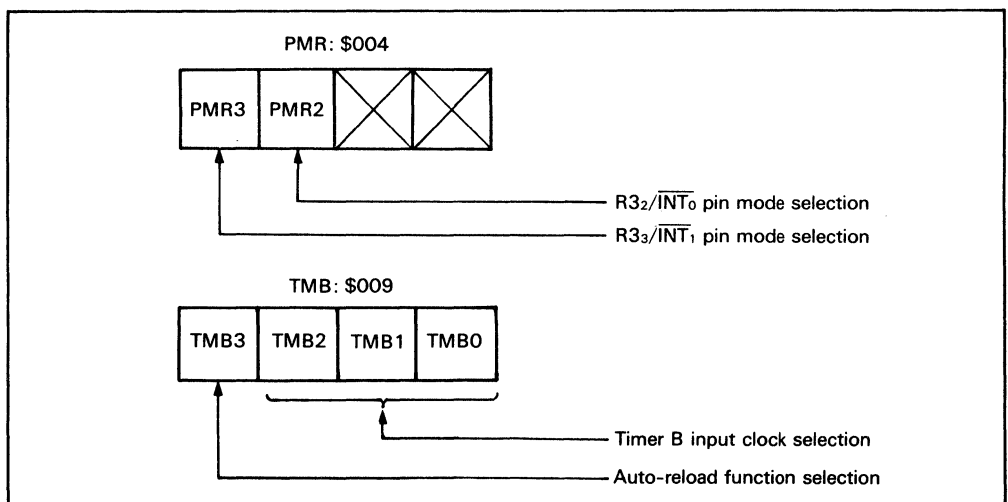


Figure 10. Mode Register Configuration and Function

Input/Output

The MCU has 36 I/O pins, 12 standard and 24 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain). One of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_i/V_{disp} pin via mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 10 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 11.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in Figure 11 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the \overline{HLT} signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D port I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 as for the classification of

standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The six R ports in the HMCS414 are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read from the output-only and/or non-existing ports.

The $R3_2$ and $R3_3$ pins are multiplexed with the INT_0 and INT_1 pins respectively. See table 10 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-up MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 12 shows the parts initialized by MCU reset, and the status of each. Table 13 shows how registers recover from stop mode.

Table 10. I/O Pin Circuit Types

		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable pins
Standard Pins	I/O Common Pins				D ₀ - D ₃ R ₃₀ - R ₃₃ R ₄₀ - R ₄₃

Table 10. I/O Pin Circuit Types (Cont)

		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applicable pins
High Voltage Pins	I/O Common Pins			D ₄ - D ₁₄ R ₁₀ - R ₁₃ R ₂₀ - R ₂₃
	Output Pins			R ₀₀ - R ₀₃
	Input Pins			RA ₁

Table 10. I/O Pin Circuit Types (Cont)

		Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applicable pins
Standard Pins	Input Pins			$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$

Note: In the stop mode, $\overline{\text{HLT}}$ signal is 0, HLT signal is 1 and I/O pins are in high impedance state.

Table 11. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0

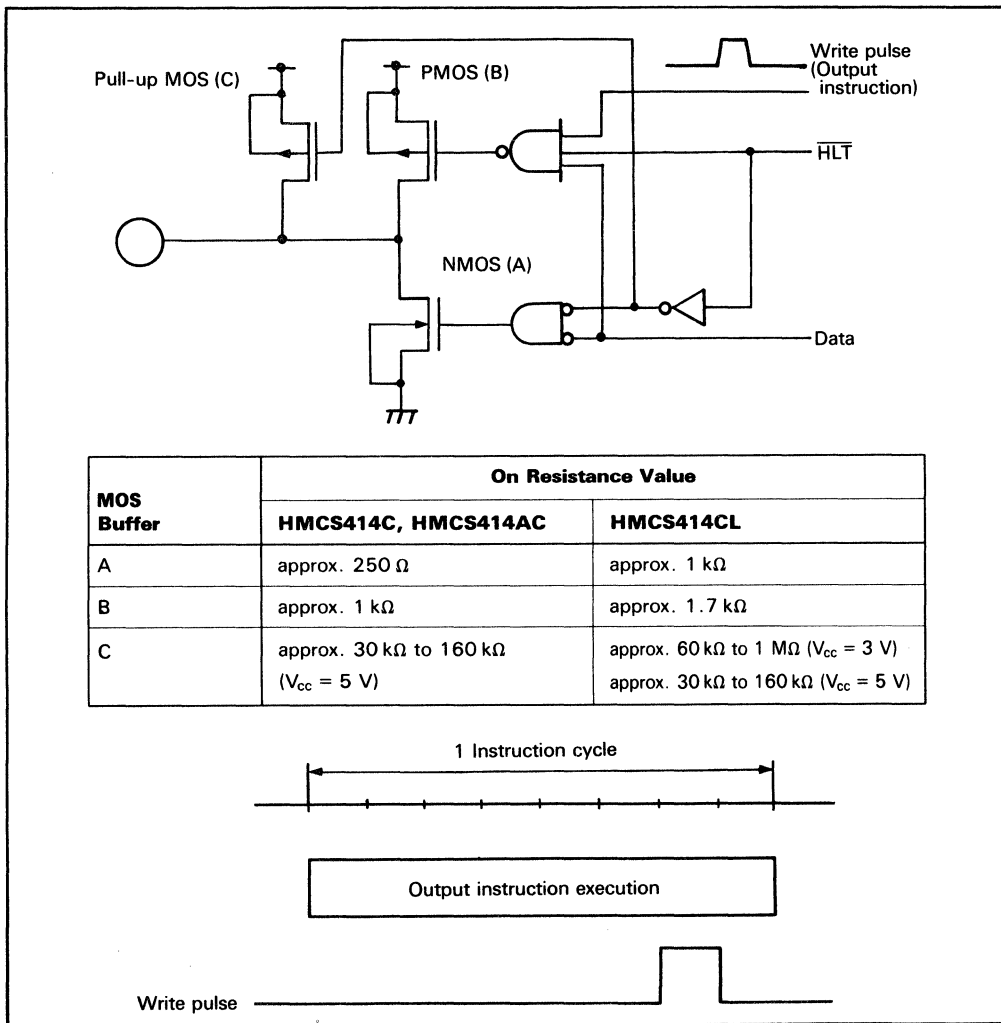


Figure 11. Output Circuit Operation of Standard Pins With Pull-Up MOS Option

Table 12. Initial Value After MCU Reset

Items	Initial Value by MCU Reset	Contents	
Program Counter (PC)	\$0000	Execute program from the top of ROM address	
Status (ST)	1	Enable to branch with conditional branch instructions	
Stack Pointer (SP)	\$3FF	Stack level is 0	
I/O Pin Output Register	Standard Pin (A) Without Pull-Up MOS	1	Enable input
	(B) With Pull-Up MOS	1	Enable input
	(C) CMOS	1	—
	High Voltage Pin (D) Without Pull-Down MOS	0	Enable input
	(E) With Pull-Down MOS	0	Enable input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—

Table 13. Initial Value after Stop Reset

Item	After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop Mode)
Carry (CA)	The contents of the items before MCU reset are not retained.	
Accumulator (A)	It is necessary to initialize them by software.	
B Register (B)		
W Register (W)		
X/SPX Registers (X/SPX)		
Y/SPY Registers (Y/SPY)		
RAM	The contents of RAM before MCU reset (just before STOP instruction) are retained.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. Through mask option, either crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table

15 for selection of the type. In addition, see figure 13 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available. Three divide ratios, 1/16, 1/8, and 1/4, are selectable via mask option (table 14).

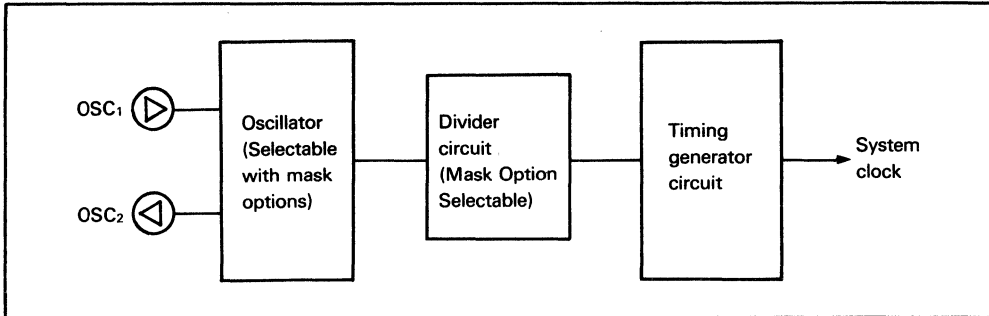


Figure 12. Internal Oscillator Circuit

Table 14. Internal Oscillation Circuit Mask Option

		HMCS 414C	HMCS 414CL	HMCS 414AC
Divider	1/16	—	○	—
	1/8	○	○	—
	1/4	○	—	○
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○

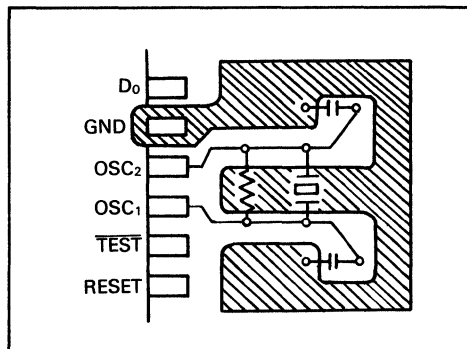


Figure 13. Layout of Crystal and Ceramic Filter

Table 15. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants		
		HMCS414C	HMCS414CL	HMCS414AC
External Clock Operation				
Ceramic Filter Oscillator		Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA4.00MG (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$
Crystal Oscillator	<p>AT cut parallel resonance crystal</p>	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$
	<p>GT cut parallel resonance crystal</p>		$R_f: 2\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}2.25\text{ MHz}$	

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 13).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 16). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 16. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Input/Output Pin	Timer/Counter	Recovery Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained (Note 3)	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET (Note 1)	Stop	Retained	High impedance (Note 2)	Stop	RESET input

- Notes:
1. The MCU recovers from STOP mode by RESET input. Refer to table 13 for the contents of the flags and registers.
 2. A high-voltage pin with a pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is in addition to the current dissipation in stop mode (I_{stop}).
 3. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is in addition to the current dissipation in standby mode.

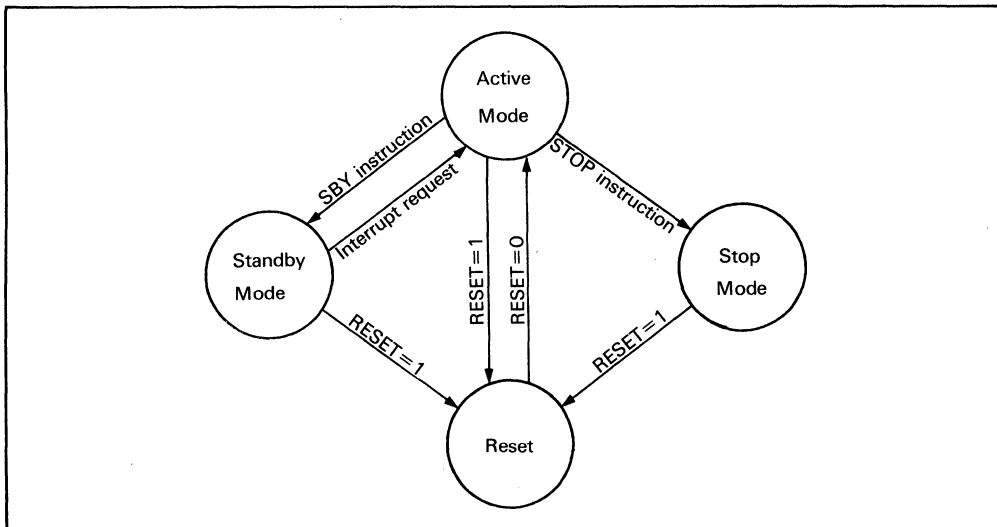


Figure 14. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 15 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

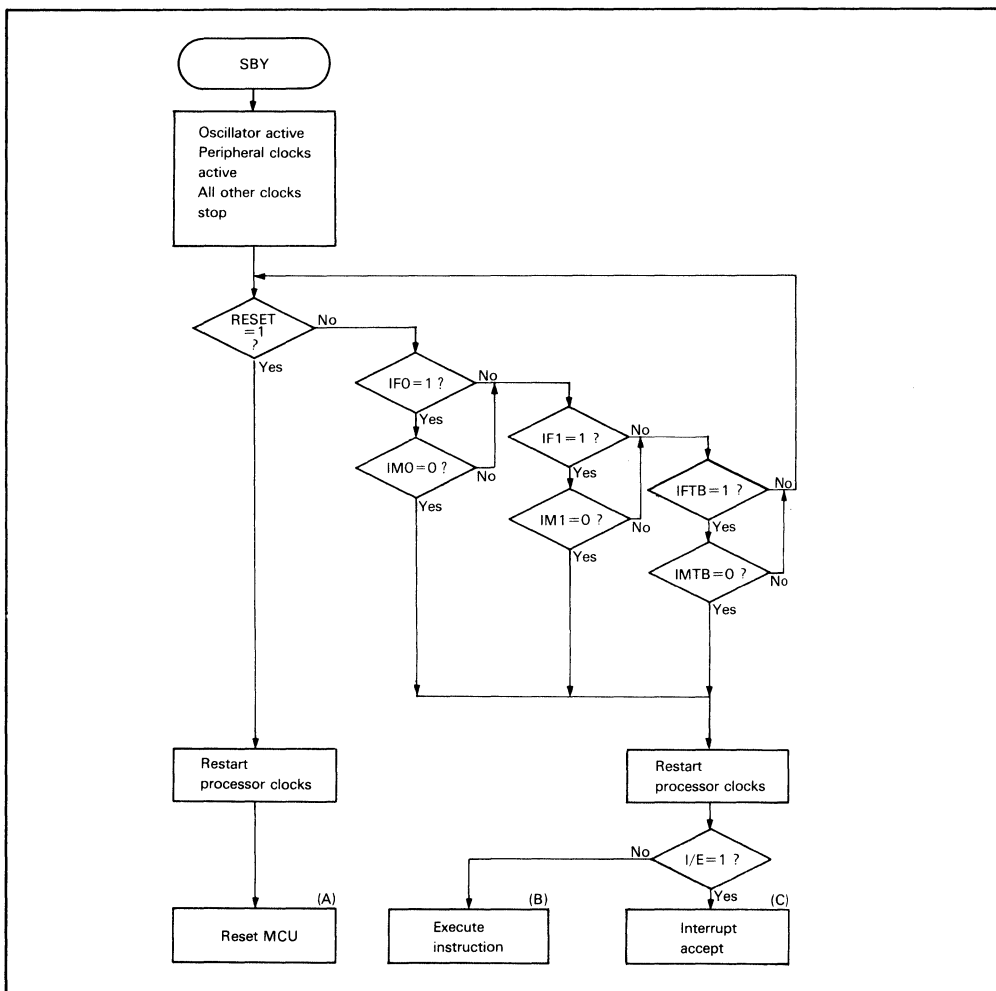


Figure 15. MCU Operating Flowchart in Standby Mode

RAM Addressing Mode

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 18.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 19), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 20). When bit 8 in the ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

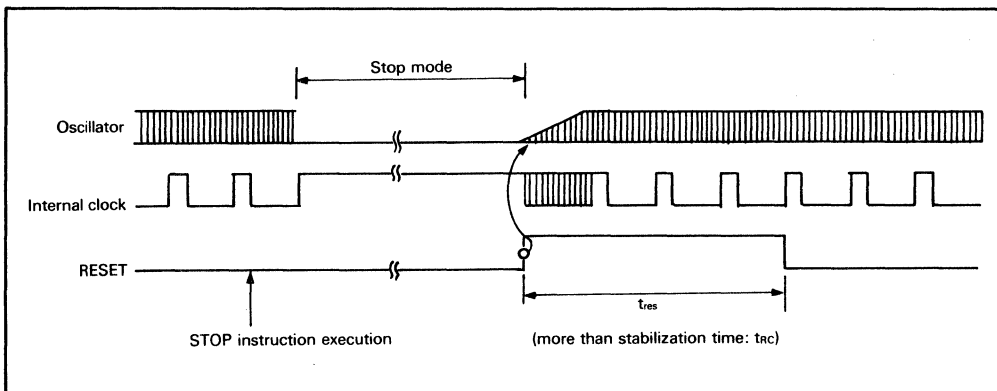


Figure 16. Timing Chart of Recovering from Stop Mode



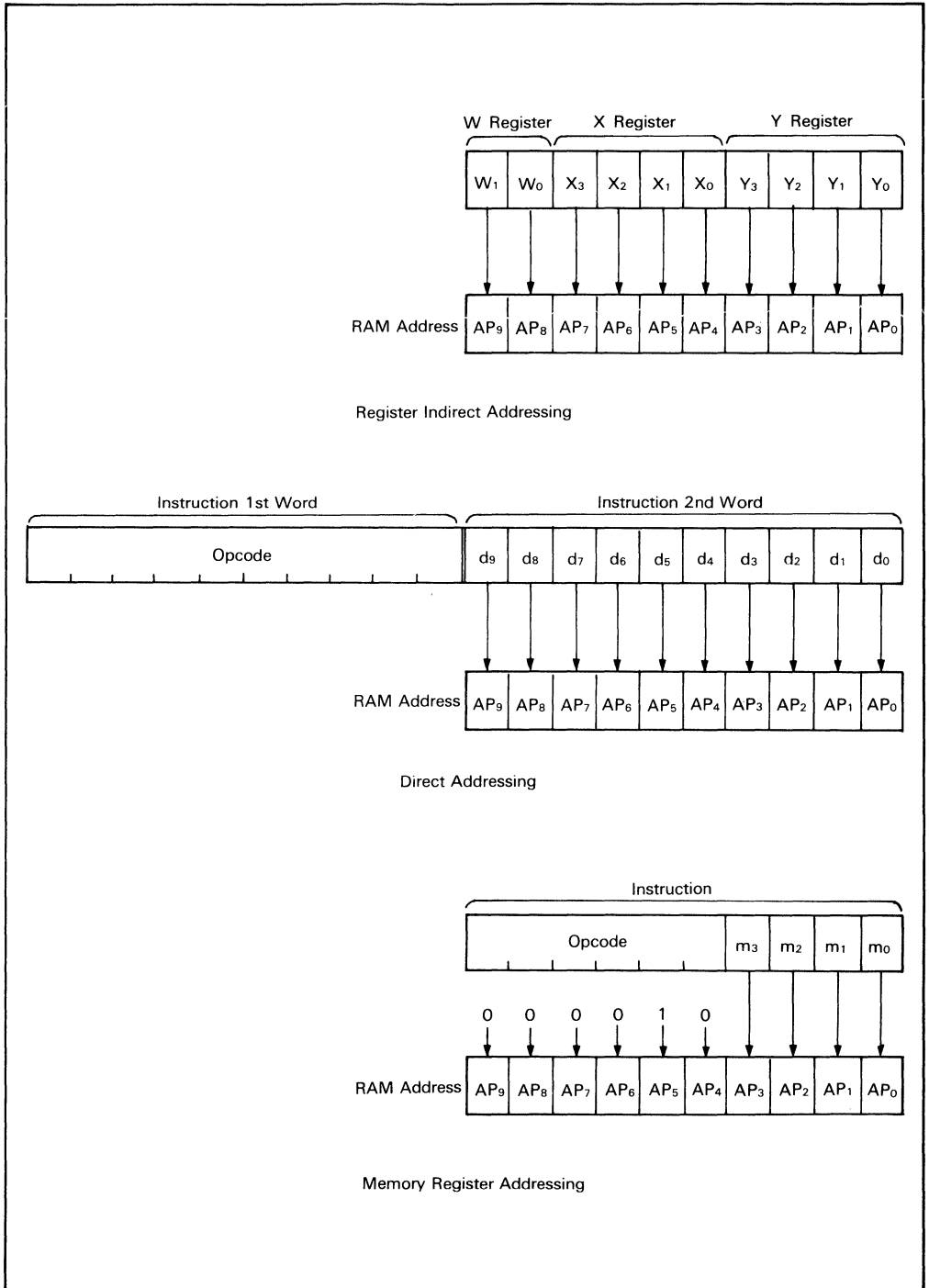


Figure 17. RAM Addressing Mode

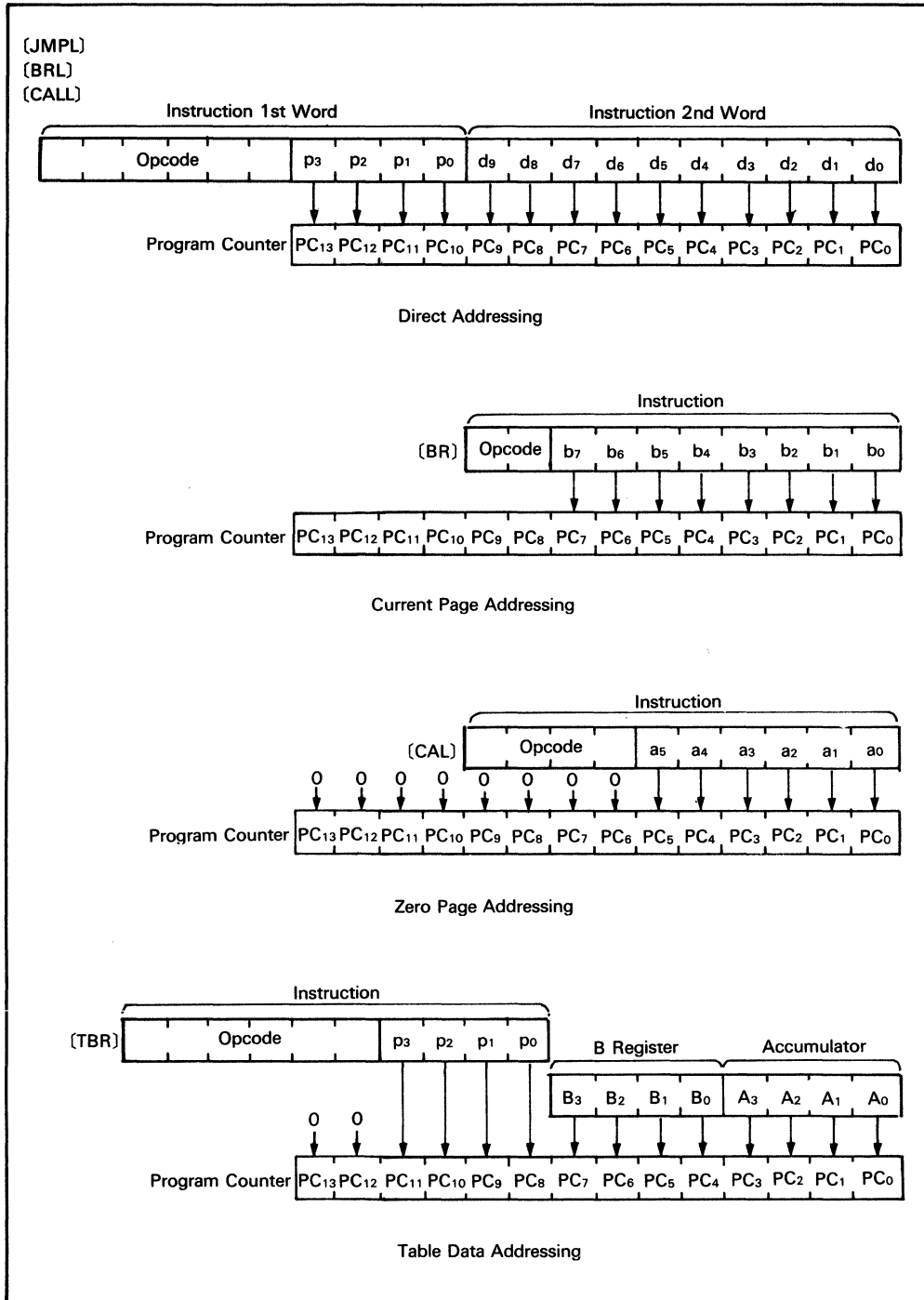


Figure 18. ROM Addressing Mode



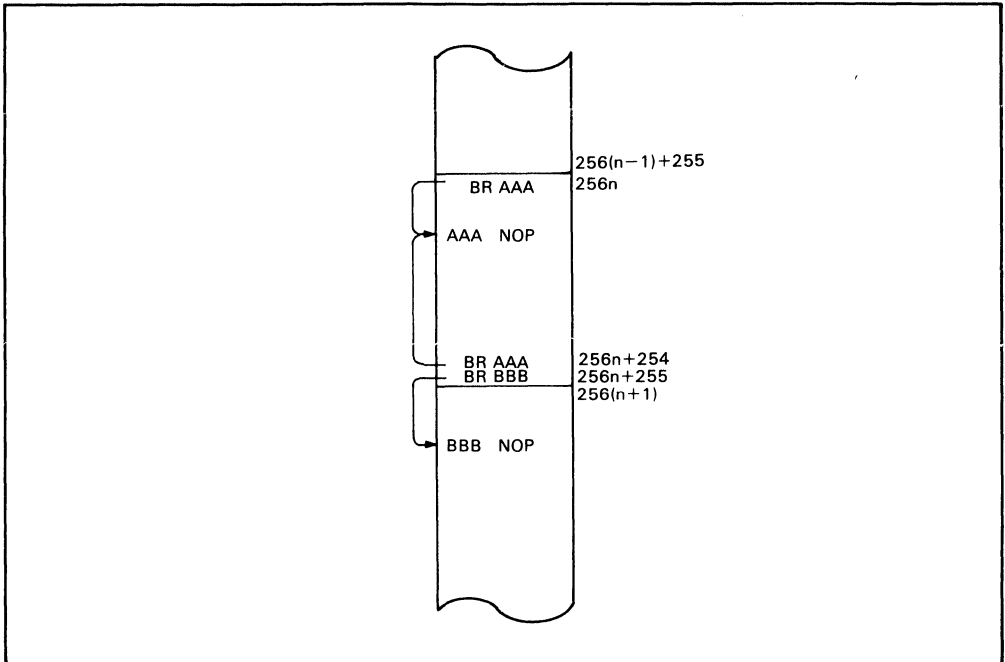


Figure 19. BR Instruction Branch Destination on Pages Boundary

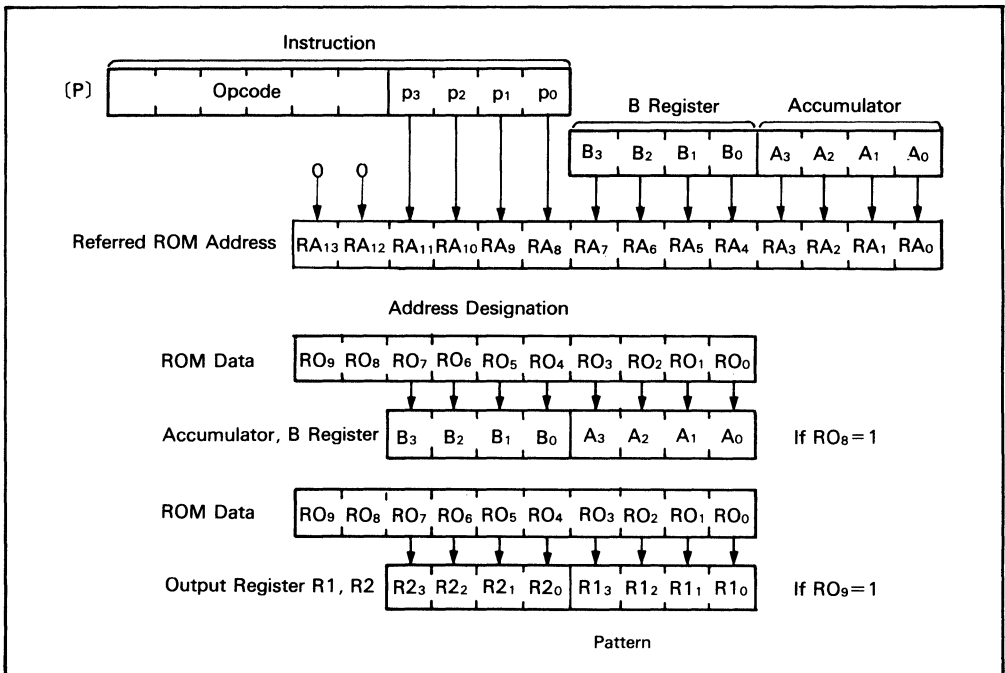


Figure 20. P Instruction

Instruction Set

The HMCS414C/CL/AC provide 98 instructions which are classified into 10 groups as follows:

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 17-26 list their functions, and table 27 is an opcode map.

Table 17. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 18. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Table 19. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

HMCS414C/HMCS414CL/HMCS414AC

Table 20. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 21. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A + i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B + 1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B - 1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M + A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M - A - \overline{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M - A - \overline{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

HMCS414C/HMCS414CL/HMCS414AC

Table 22. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 23. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2



Table 24. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 25. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 26. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: HMCS414 has no serial interface, so STS (start serial) operates the same as NOP.



HMCS414C/HMCS414CL/HMCS414AC

Table 27. Opcode Map

R8		0																1															
		H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
0	0	NOP	XSPX	XSPY	XSPXY	ANEM				AM					ORM								ANEMC					AMDC					ORMC
	1	RTN	RTNI			ALEM				AMC					EORM								ALEMCD					AMCD				EORMC	
	2	INEM								i(4)								INEMD								i(4)							
	3	ILEM								i(4)								ILEMD								i(4)							
	4	LBM(XY)			BNEM				LAB						IB				COMB				OR								SBYSTOP		
	5	LMAY(X)			AYY				LASPY						IY																	JMPL	
	6	NEGA			RED				LASPY																							CALL	
	7	YNEI								i(4)								BRL								p(4)							
	8	XMA(XY)				SEM n(2)			REM n(2)						TM n(2)				XMAD				SEMD n(2)				REMD n(2)				TMD n(2)		
	9	LAM(XY)				LMA(XY)			SMC						ANM				LAMD				LMAD				SMCD				ANMD		
	A	ROT	ROTL					DAA						DAS				LAY													LMID		
	B	TBR								p(4)								P								p(4)							
	C	XMB(XY)			BLEM				LBA																							DB	
	D	LMADY(X)			SY				LYA																							DY	
	E	TD			SED				LXA					REC				SEC													CAL		
	F	LWI								i(2)																							
1	0	LBI								i(4)																							
	1	LYI								i(4)																							
	2	LXI								i(4)																							
	3	LAI								i(4)																							
	4	LBR								m(4)																							
	5	LAR								m(4)																							
	6	REDD								m(4)																							
	7	LAMR								m(4)								BR								b(8)							
	8	AI								i(4)																							
	9	LMIIY								i(4)																							
	A	TDD								m(4)																							
	B	ALEI								i(4)																							
	C	LRB								m(4)																							
	D	LRA								m(4)																							
	E	SEDD								m(4)																							
	F	XMRA								m(4)																							

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction (2-word/2-cycle)
 2-word/2-cycle Instruction



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V	
Terminal Voltage	V_T	- 0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	25	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$- I_O$	4 (2)	mA	9, 10, 13
		6 (3)	mA	9, 11, 13
		30 (15)	mA	9, 12, 13
Total Allowance of Output Current	$-\Sigma I_O$	85 (100)	mA	6, 13
Operating Temperature	T_{opr}	- 20 to + 75	°C	
Storage Temperature	T_{stg}	- 55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_3$, R3 and R4.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $D_0 - D_3$, R3 and R4.
 11. R0 - R2.
 12. $D_4 - D_{15}$.
 13. $-\Sigma I_O = 100$ mA if $-I_O$ s equal to or less than 2 mA, 3 mA, or 15 mA.

HMCS414C/HMCS414CL/HMCS414AC

Electrical Characteristics

DC Characteristics

(GND = 0 V, $V_{diap} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,

HMCS414C: $V_{CC} = 3.5$ V to 6 V,

HMCS414CL: $V_{CC} = 2.5$ V to 6 V,

HMCS414AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, R32/INT ₀ , R33/INT ₁	0.8 V_{CC}	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	HMCS414C/AC	
			$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	HMCS414CL	
Input Low Voltage	V_{IL}	RESET, R32/INT ₀ , R33/INT ₁	-0.3	0.2 V_{CC}	V		
		OSC ₁	-0.3	0.5	V	HMCS414C/AC	
			-0.3	0.3	V	HMCS414CL	
Input/Output Leakage Current	$ I_{IL} $	RESET, R32/INT ₀ , R33/INT ₁ , OSC ₁		1	μA	$V_{in} = 0$ V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		1.8	mA	HMCS414C; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	2,5
				0.8	mA	HMCS414CL; $V_{CC} = 3$ V; $f_{osc} = 4$ MHz, $\div 16$, or $f_{osc} = 2$ MHz, $\div 8$	2,5
				3.0	mA	HMCS414AC; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 4$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		1.0	mA	HMCS414C; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	3,5
				0.5	mA	HMCS414CL; $V_{CC} = 3$ V; $f_{osc} = 4$ MHz, $\div 16$, or $f_{osc} = 2$ MHz, $\div 8$	3,5
				1.4	mA	HMCS414AC; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 4$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		10	μA	$V_{in}(\overline{\text{TEST}}) = V_{CC} - 0.3$ V to V_{CC} ; V_{CC} , $V_{in}(\text{RESET}) =$ 0 V to 3 V	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2		V		

Notes: 1. Excluding pull-up MOS current and output buffer current.



- Notes:
2. The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, R_{A1}: V_{disp}
 3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, R_{A1}: V_{disp}
 4. Excluding pull-down MOS current.
 5. When $f_{osc} = x$ MHz, estimate the current dissipation as follows:
 HMCS414C/AC; Max value @ x MHz = $x/4 \times$ (max value @ 4 MHz)
 HMCS414CL; Max value @ x MHz = $x/2 \times$ (max value @ 2 MHz)

Input/Output Characteristics for Standard Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$,
HMCS414C: $V_{CC} = 3.5$ V to 6 V,
HMCS414CL: $V_{CC} = 2.5$ V to 6 V,
HMCS414AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	-0.3		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	$V_{CC} - 1.0$			V	HMCS414C/AC; - $I_{OH} = 1.0$ mA	1
		D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	$V_{CC} - 0.5$			V	HMCS414C/AC; - $I_{OH} = 0.5$ mA HMCS414CL; - $I_{OH} = 0.3$ mA	1
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄			0.4	V	HMCS414C/AC; $I_{OL} = 1.6$ mA HMCS414CL; $I_{OH} = 0.4$ mA	
Input/Output Leakage Current	$ I_{II} $	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄			1	μA	$V_{in} = 0$ V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	30	60	150	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	3
		D ₀ -D ₃ , R ₃₀ , R ₃₁ , R ₄	3	15	50	μA	HMCS414CL only; $V_{CC} = 3$ V, $V_{in} = 0$ V	3

- Notes:
1. I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. I/O pins with pull-up MOS selected by mask option.



HMCS414C/HMCS414CL/HMCS414AC

Input/Output Characteristics for High-Voltage Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,

HMCS414C: $V_{CC} = 3.5$ V to 6 V,

HMCS414CL: $V_{CC} = 2.5$ V to 6 V,

HMCS414AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₄ -D ₁₄ , R ₁ , R ₂ , RA ₁	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₄ -D ₁₄ , R ₁ , R ₂ , RA ₁	$V_{CC} - 40$		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₄ -D ₁₄	$V_{CC} - 3.0$			V	- $I_{OH} = 15$ mA, HMCS414C/CL; $V_{CC} = 5$ V \pm 20% HMCS414AC; $V_{CC} = 4.5$ to 6 V	
			$V_{CC} - 2.0$			V	- $I_{OH} = 10$ mA, HMCS414C/CL; $V_{CC} = 5$ V \pm 20% HMCS414AC; $V_{CC} = 4.5$ to 6 V	
			$V_{CC} - 1.0$			V	HMCS414C/AC; - $I_{OH} = 4$ mA HMCS414CL; - $I_{OH} = 2.5$ mA	
		RO-R2	$V_{CC} - 3.0$			V	- $I_{OH} = 3$ mA, HMCS414C/CL; $V_{CC} = 5$ V \pm 20% HMCS414AC; $V_{CC} = 4.5$ to 6 V	
			$V_{CC} - 2.0$			V	- $I_{OH} = 2$ mA, HMCS414C/CL; $V_{CC} = 5$ V \pm 20% HMCS414AC; $V_{CC} = 4.5$ to 6 V	
			$V_{CC} - 1.0$			V	HMCS414C/AC; - $I_{OH} = 0.8$ mA HMCS414CL; - $I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	D ₄ -D ₁₄ , RO-R2	$V_{CC} - 37$			V	$V_{disp} = V_{CC} - 40$ V	1
			$V_{CC} - 37$			V	150k Ω to $V_{CC} - 40$ V	2
Input/Output Leakage Current	$ I_{II} $	D ₄ -D ₁₄ , RO-R2, RA ₁		20		μA	$V_{in} = V_{CC} - 40$ V to V_{CC}	3
Pull-Down MOS Current	I_d	D ₄ -D ₁₄ , RO-R2, RA ₁	125	250	600	μA	$V_{disp} = V_{CC} - 35$ V, $V_{in} = V_{CC}$	4

- Notes:
1. I/O pins with pull-down MOS selected by mask option.
 2. I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. I/O pins with pull-down MOS selected by mask option.



AC Characteristics

**(GND = 0 V, $V_{diss} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
HMCS414C: $V_{CC} = 3.5$ V to 6 V,
HMCS414CL: $V_{CC} = 2.5$ V to 6 V,
HMCS414AC: $V_{CC} = 4.5$ V to 6 V)**

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	HMCS414C; divide by 8	
			0.2	2	2.25	MHz	HMCS414C; divide by 4	
			0.8	4	4.5	MHz	HMCS414CL; divide by 16	
			0.4	2	2.25	MHz	HMCS414CL; divide by 8	
			0.2	4	4.5	MHz	HMCS414AC; divide by 4	
Instruction Cycle Time	t_{cyc}		1.78	2	20	μs	HMCS414C	
			3.55	4	20	μs	HMCS414CL	
			0.89	1	20	μs	HMCS414AC	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms	HMCS414C/AC	1
					60	ms	HMCS414CL	1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	HMCS414C; divide by 8 HMCS414CL; divide by 16 HMCS414AC; divide by 4	2
			203			ns	HMCS414C; divide by 4 HMCS414CL; divide by 8	2

(continued)

HMCS414C/HMCS414CL/HMCS414AC

AC Characteristics (Cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			20	ns		2
\overline{INT}_n High Level Width	t_{10H}	\overline{INT}_n	2			t_{cvc}		3
\overline{INT}_0 Low Level Width	t_{10L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{11H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{11L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms	HMCS414C/AC	4
					15	ms	HMCS414CL	4

- Notes:
- Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (HMCS414C; 3.5 V, HMCS414CL; 2.5 V, HMCS414AC; 4.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 21.)
 - See figure 22.
 - See figure 23.
 - See figure 24.

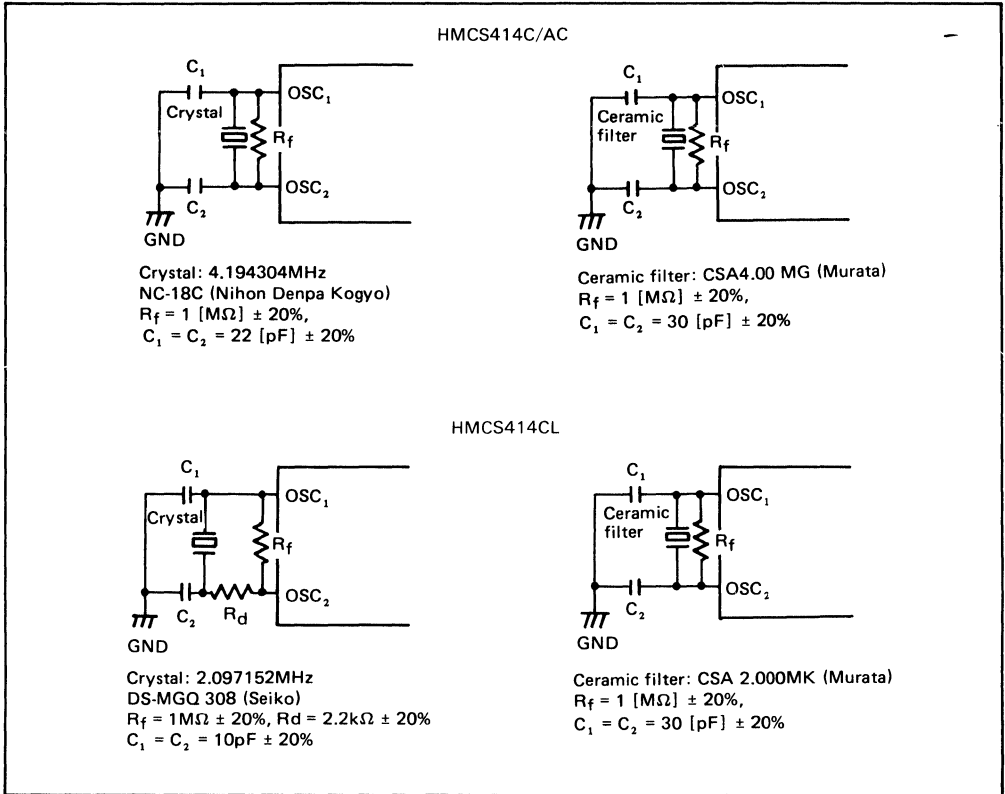


Figure 21. Oscillation Circuit

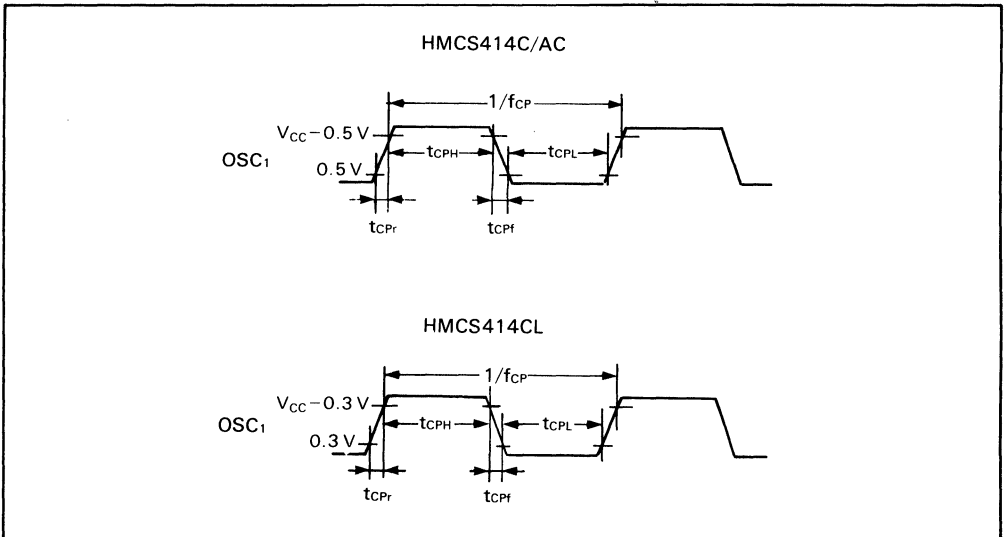


Figure 22. Oscillator Timing

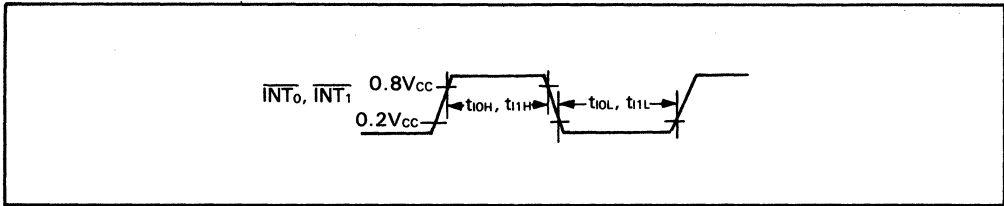


Figure 23. Interrupt Timing

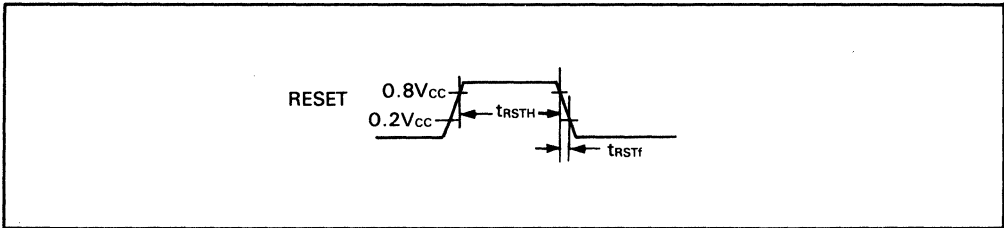


Figure 24. Reset Timing

HMCS414C/CL/AC Mask Option List

• Please enter check marks in
(■, x, ✓).

5V Operation:	<input type="checkbox"/> HMCS414C
3V Operation:	<input type="checkbox"/> HMCS414CL
High Speed Operation:	<input type="checkbox"/> HMCS414AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

(1) I/O Option

Please enter 0 in applicable item to select I/O option.

- A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
 C: CMOS (cannot be used as input) E: With Pull-down MOS
 D: Without Pull-down MOS (PMOS Open Drain)

Note: I/O options masked by are not available.

Pin	Input/Output	I/O Option					Pin	Input/Output	I/O Option						
		A	B	C	D	E			A	B	C	D	E		
D ₀	Standard Pins	Input/Output				<input checked="" type="checkbox"/>		RO	Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₁		Input/Output				<input checked="" type="checkbox"/>			RO ₁	Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₂		Input/Output				<input checked="" type="checkbox"/>			RO ₂	Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₃		Input/Output				<input checked="" type="checkbox"/>			RO ₃	Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₄	High Voltage Pins	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>				R1	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>				
D ₅		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R1 ₁	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₆		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R1 ₂	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₇		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R1 ₃	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₈		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R2	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₉		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>						R2 ₀	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₁₀		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>						R2 ₁	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₁₁		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>						R2 ₂	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
D ₁₂		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R2 ₃	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
D ₁₃		Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>					R3	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₄	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>				R3 ₀	Input/Output				<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>				R3 ₁	Input/Output				<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>				R3 ₂	Input/Output				<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
							R4	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
								R4 ₀	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
								R4 ₁	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
								R4 ₂	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
							R4 ₃	Input/Output			<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
RA	RA ₁	High Speed Pin	Input	Please Mark as RA ₁ /V _{disp}											



HMCS414C/HMCS414CL/HMCS414AC

(2) RA₁/V_{disp}

Please check (■, X, ✓) applicable item.

RA ₁ /V _{disp}	
<input type="checkbox"/>	RA ₁ : Without Pull-down MOS (D)
<input type="checkbox"/>	V _{disp}

Note. RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high pins are option D.

(3) Divider (Div)

Please check (■, X, ✓) applicable item.

Divider	HMCS414C	HMCS414CL	HMCS414AC
16		<input type="checkbox"/>	
8	<input type="checkbox"/>	<input type="checkbox"/>	
4	<input type="checkbox"/>		<input type="checkbox"/>

(4) ROM Code Media

Please check (■, X, ✓) applicable item.

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

(5) Oscillator (CPG option)

Please check (■, X, ✓) applicable item.

CPG option	<input type="checkbox"/> HMCS 414C (5V Operation)	<input type="checkbox"/> HMCS414CL (3V Operation)	<input type="checkbox"/> HMCS414AC (High Speed Operation)
	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock



HMCS424C/HMCS424CL/ — HMCS424AC (HD404240/HD40L4240/HD40A4240)

Description

The HMCS424C/CL/AC are CMOS 4-bit single-chip microcomputers in the HMCS400 series. Each device incorporates ROM, RAM, I/O, serial interface, and 2 timer/counters, and contain high-voltage I/O pins including high-current output pins to drive a fluorescent display directly.

Features

- 4-bit architecture
- 4096 words of 10-bit ROM
- 256 digits of 4-bit RAM
- 36 I/O pins, including 24 high-voltage I/O pins (40 V max)
- 2 timer/counters
 - 11-bit prescaler
 - 8-bit free running timer/counter
 - 8-bit auto-reload timer/event counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
 - External: 2
 - Timer/counter: 2
 - Serial interface: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time
 - 0.89 μ s: HMCS424AC
 - 1.78 μ s: HMCS424C
 - 3.55 μ s: HMCS424CL
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Crystal or ceramic filter
 - External clock input
- Package
 - Standard 42-pin dual in-line plastic package
 - 42-pin shrink dual in-line plastic package
 - 44-pin flat plastic package
- Instruction set compatible with HMCS408; 99 instructions
- High programming efficiency with 10-bit/word ROM: 79 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas

- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD40P4281 with the following fixed options:
 - I/O pin: open drain
 - Oscillator: crystal or ceramic filter oscillator (externally drivable)
 - Divider: Divided by 8
 - Package: Standard 42-pin dual in-line ceramic package

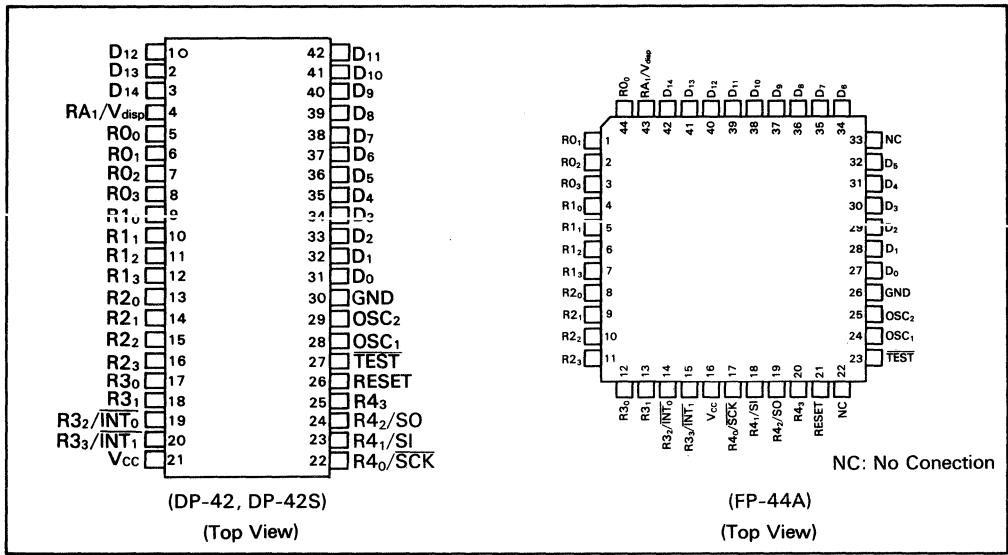
Type of Products

Item	HMCS424C	HMCS424CL	HMCS424AC
Product Name	HD404240	HD40L4240	HD40A4240
Power Supply (V)	3.5 to 6	2.5 to 6	4.5 to 6
Typical Instruction Cycle Time (μ s)	2	4	1

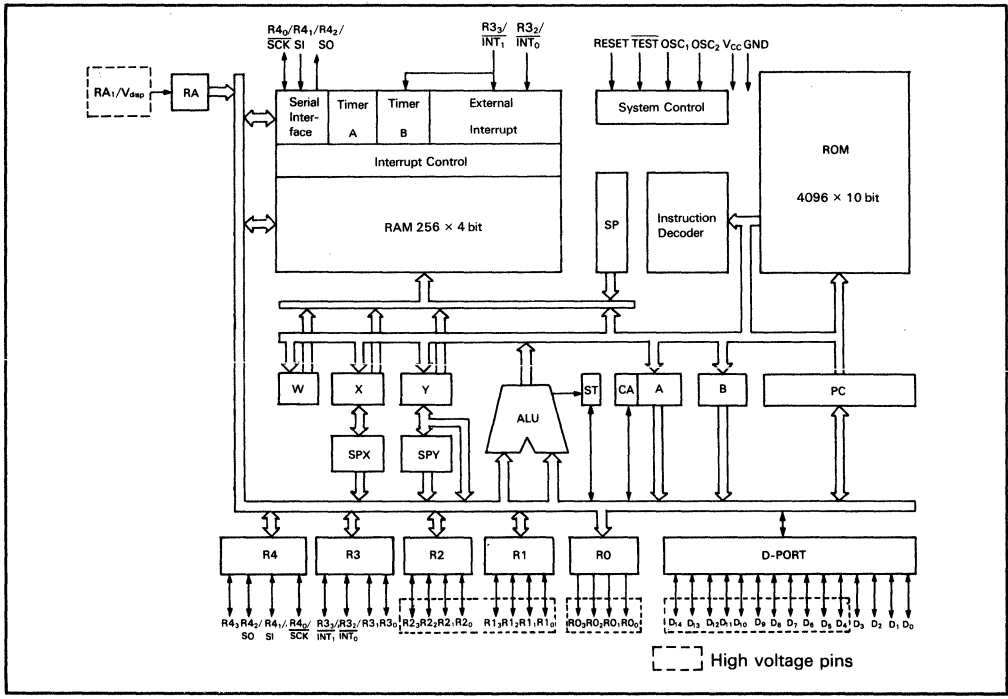


HMCS424C/HMCS424CL/HMCS424AC

Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC} and V_{disp} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC} - 40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀-D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 16 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₄ are

high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀-R₃, R₁₀-R₁₃, R₂₀-R₂₃, R₃₀-R₃₃, R₄₀-R₄₃, RA₁ (R Ports)

R₀ to R₄ are 4-bit ports. RA is a 1-bit port. R₀ is an output port, RA is an input port, and R₁ to R₄ are I/O ports. R₀, R₁, R₂, and RA are high-voltage ports, and R₃ and R₄ are standard ports. Each pin has a mask option which selects its circuit type. The pins R_{3₂}, R_{3₃}, R_{4₀}, R_{4₁}, and R_{4₂} are multiplexed with INT₀, INT₁, SCK, SI, and SO respectively. For details, see Input/ Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R_{3₂} and R_{3₃} respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R_{4₀}, R_{4₁}, and R_{4₂} respectively. For details, see Serial Interface.

Functional Description

ROM Memory Map

The MCU includes 4,096 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F can be used for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F can be used for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF can be used for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$0FFF): Locations from \$0000 to \$0FFF can be used for program code.

RAM Memory Map

The MCU includes 256 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area (\$020 to \$0DF): 16 digits of \$020 through \$02F are called memory registers

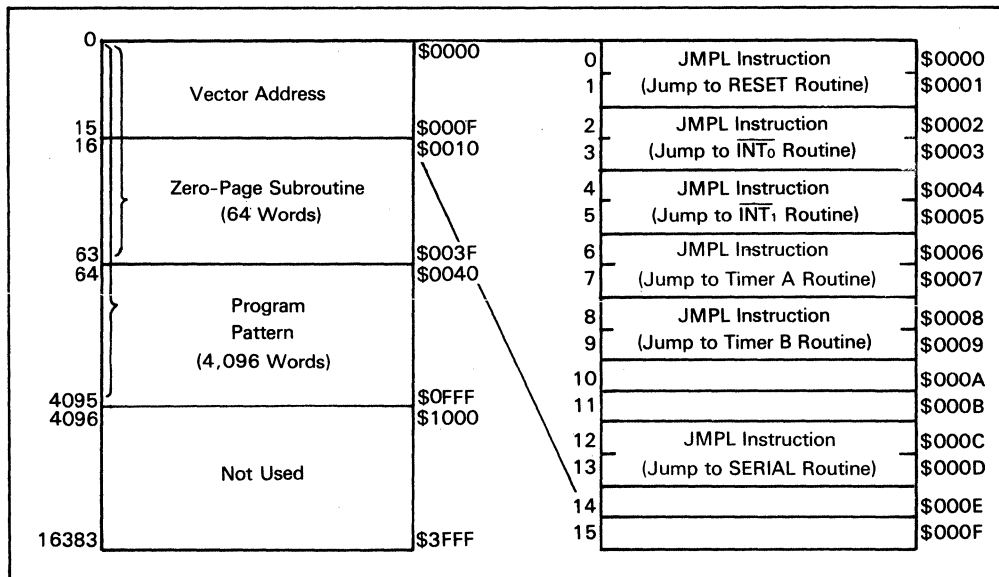


Figure 1. ROM Memory Map



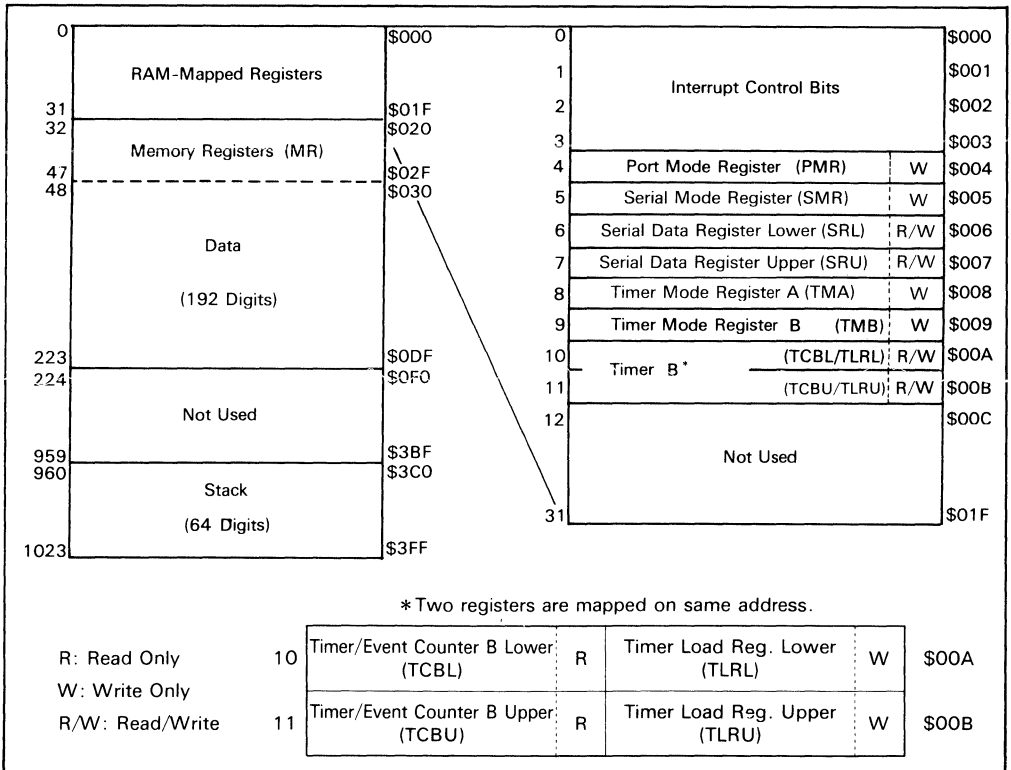


Figure 2. RAM Memory Map

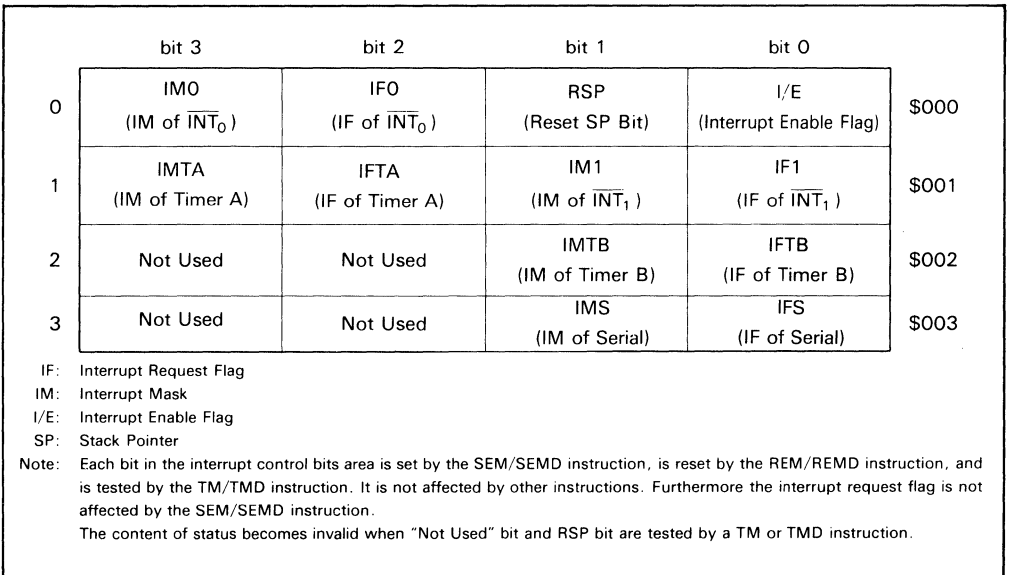


Figure 3. Configuration of Interrupt Control Bit Area



(MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W regis-

ter is write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions

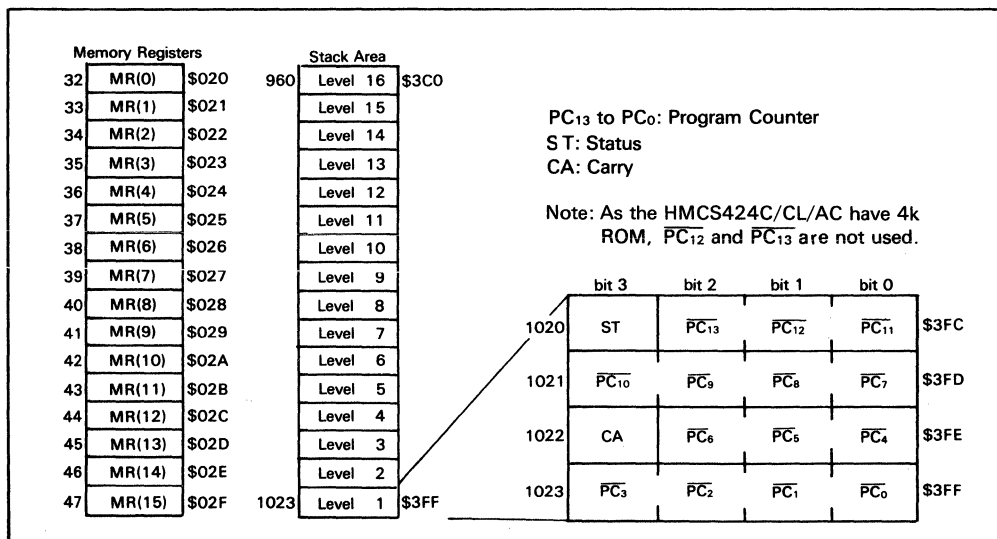


Figure 4. Configuration of Memory Register, Stack Area, and Stack Position



stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timer A, timer B), and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt

vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the

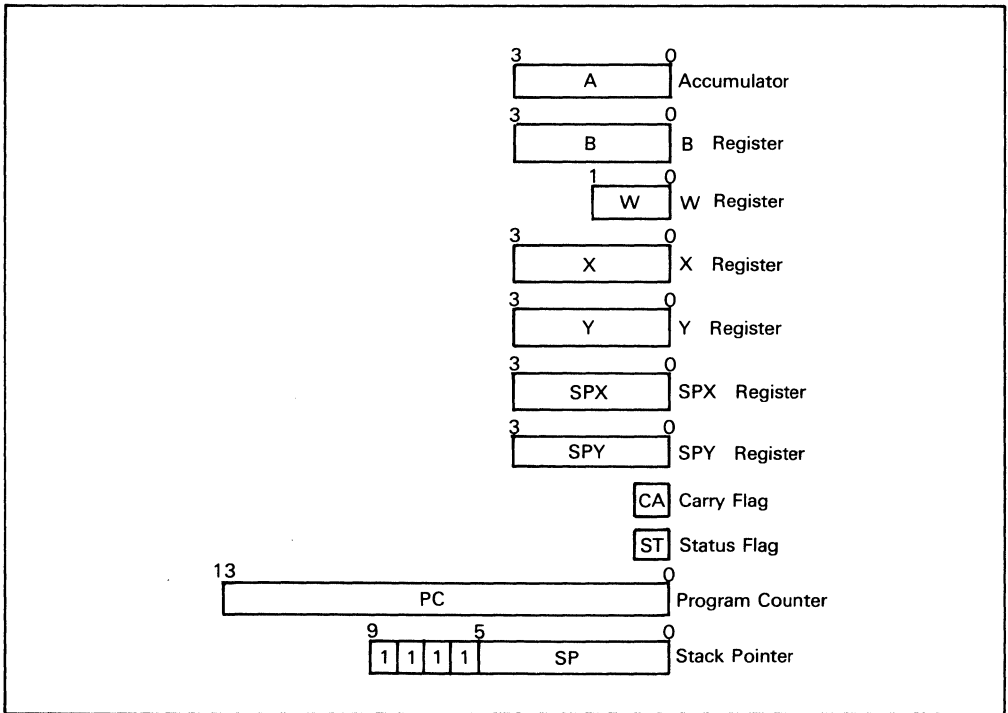


Figure 5. Registers and Flags



priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0):

The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1):

The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_2/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs (table 4).

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, the external interrupt mask (IM1) has to be set so that the \overline{INT}_1 interrupt request will not

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
SERIAL	5	\$000C

Table 2. Interrupt Service Conditions

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer A	Timer B	Serial
I/E	1	1	1	1	1
IFO · \overline{IM}_0	1	0	0	0	0
IF1 · \overline{IM}_1	*	1	0	0	0
IFTA · \overline{IMTA}	*	*	1	0	0
IFTB · \overline{IMTB}	*	*	*	1	0
IFS · \overline{IMS}	*	*	*	*	1

* Don't care



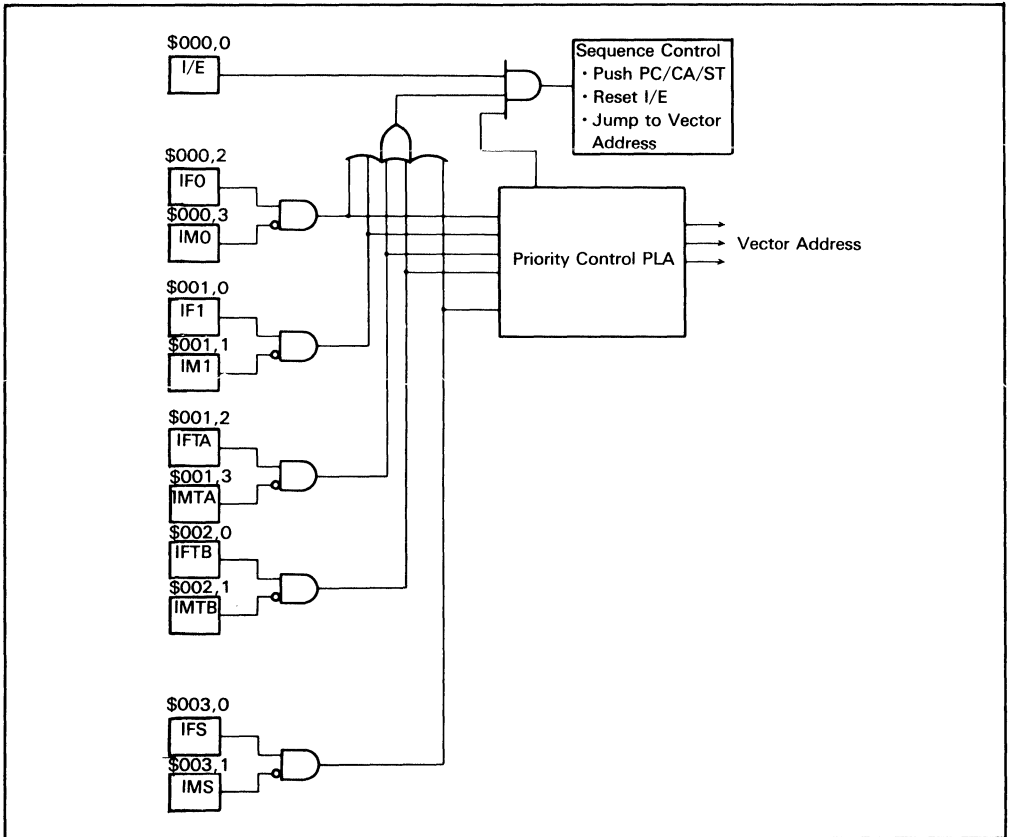


Figure 6. Interrupt Control Circuit Block Diagram

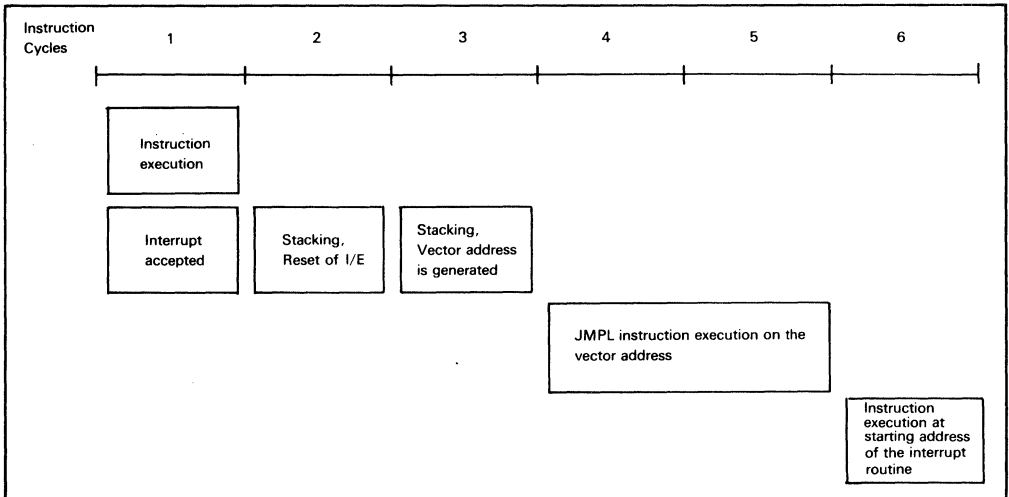


Figure 7. Interrupt Servicing Sequence



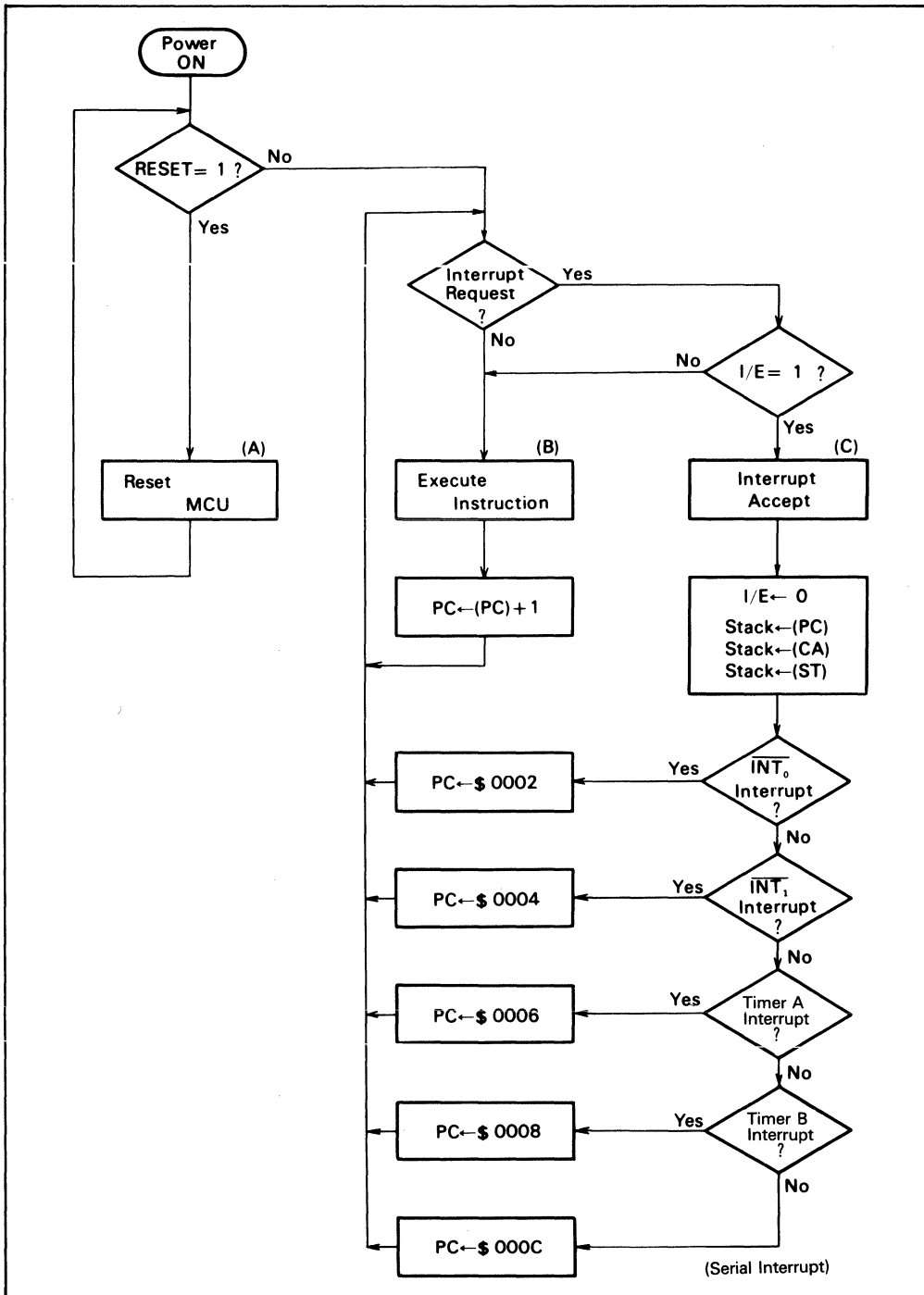


Figure 8. Interrupt Servicing Flowchart



be accepted (table 5).

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the INT₀, and INT₁ inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The 4-bit write-only port mode register controls the R₃/ $\overline{\text{INT}}_0$ pin, R₃/ $\overline{\text{INT}}_1$ pin, R₄/SI pin, and R₄/SO pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, the serial mode register,

the octal counter and the multiplexer as illustrated in figure 9. Pin R₄/SCK and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to \$0. The counter starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of the SCK. When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the R₄/SCK, prescaler divide ratio, and transfer clock source as shown in table 7. The write signal to the serial mode register controls the operating state of the serial

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

Ex Int Req Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	R ₃ / $\overline{\text{INT}}_1$ Pin
0	Used as R ₃ port input/output pin
1	Used as $\overline{\text{INT}}_1$ input pin

PMR2	R ₃ / $\overline{\text{INT}}_0$ Pin
0	Used as R ₃ port input/output pin
1	Used as $\overline{\text{INT}}_0$ input pin

PMR1	R ₄ /SI Pin
0	Used as R ₄ port input/output pin
1	Used as SI input pin

PMR0	R ₄ /SO Pin
0	Used as R ₄ port input/output pin
1	Used as SO output pin



interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it is necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SDR: \$006, SRU: \$007): The 8-bit read/write serial data register consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register will be output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time,

external data will be input from the SI pin to the serial data register, to MSB first, synchronously with the rising edge of the transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Serial Interrupt Request Flag (IFS: \$003 bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: \$003 bit 1): The serial interrupt mask masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

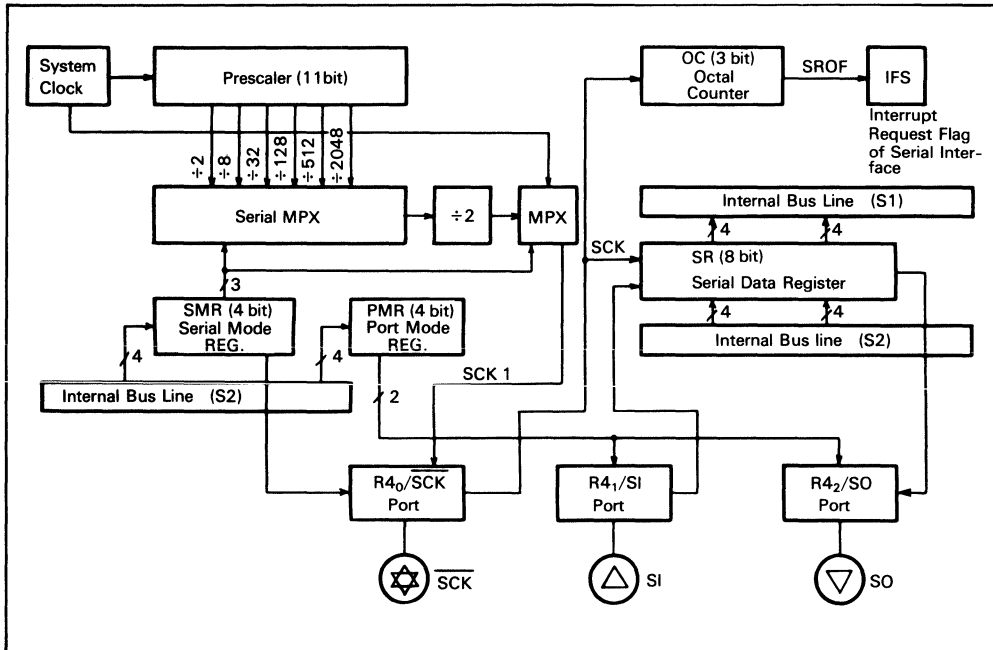


Figure 9. Serial Interface Block Diagram



Initialize the serial interface by the write signal to the serial mode register when the operation mode is changed.

Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface is put into this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK

waiting state.

In this state the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the octal counter counts up and the serial data register shifts simultaneously. If the clock continuous output mode is selected, however, the serial interface stays in SCK waiting state while the transfer clock outputs continuously.

The octal counter becomes 000 again after 8 transfer clocks or execution of the STS instruction, so that the serial interface returns to SCK waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops after 8 clocks.

Table 7. Serial Mode Register

SMR3	R4 ₀ /SCK
0	Used as R4 ₀ port input/output pin
1	Used as SCK input/output pin

SMR2	SMR1	SMR0	R4 ₀ /SCK Port	Transfer Clock		
				Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	SCK Output	Prescaler	÷ 2048	÷ 4096
0	0	1	SCK Output	Prescaler	÷ 512	÷ 1024
0	1	0	SCK Output	Prescaler	÷ 128	÷ 256
0	1	1	SCK Output	Prescaler	÷ 32	÷ 64
1	0	0	SCK Output	Prescaler	÷ 8	÷ 16
1	0	1	SCK Output	Prescaler	÷ 2	÷ 4
1	1	0	SCK Output	System Clock	—	÷ 1
1	1	1	SCK Input	External Clock	—	—

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

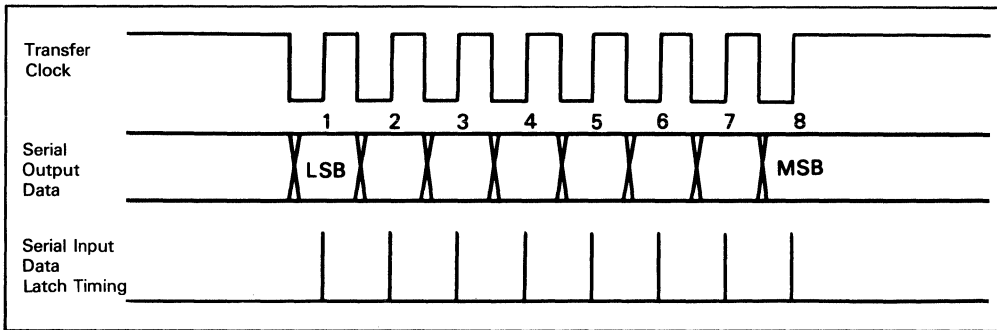


Figure 10. Serial Interface I/O Timing Chart

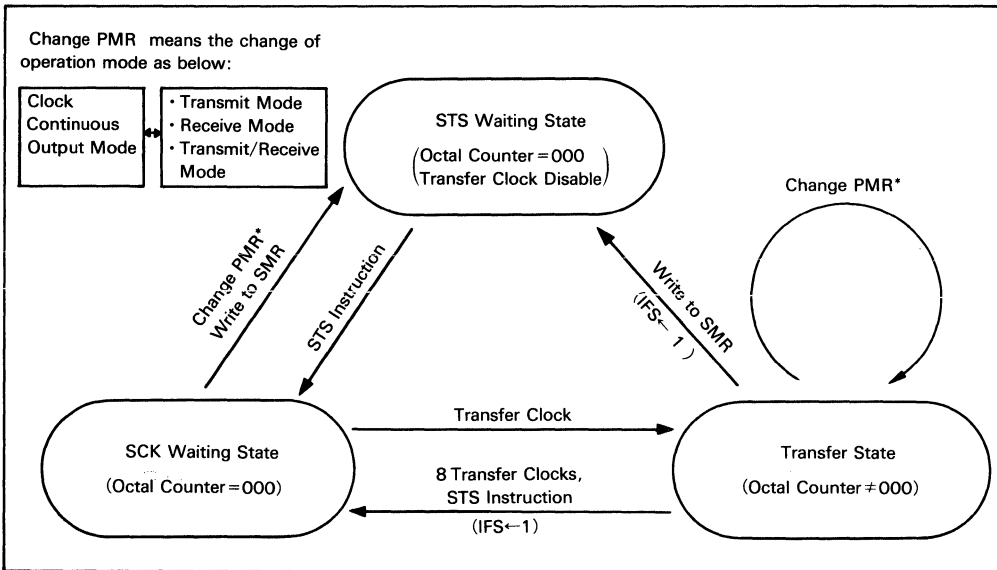


Figure 11. Serial Interface Operation State



Example of Transfer Clock Error Detection:

The serial interface functions abnormally when the transfer clock is disturbed by external noise. In this case, transfer clock error can be detected by the procedure shown in figure 12.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts as the following sequence: first, transfer state, second, SCK waiting state and third, transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

Timer

The MCU contains a prescaler and a timer/counter (timer A, timer B, figure 13) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter, and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to

count up the system clock signal as soon as the RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by the timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A counts up to \$FF, timer A is set to \$00 again, and generates an overflow output. This sets to timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input. The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock

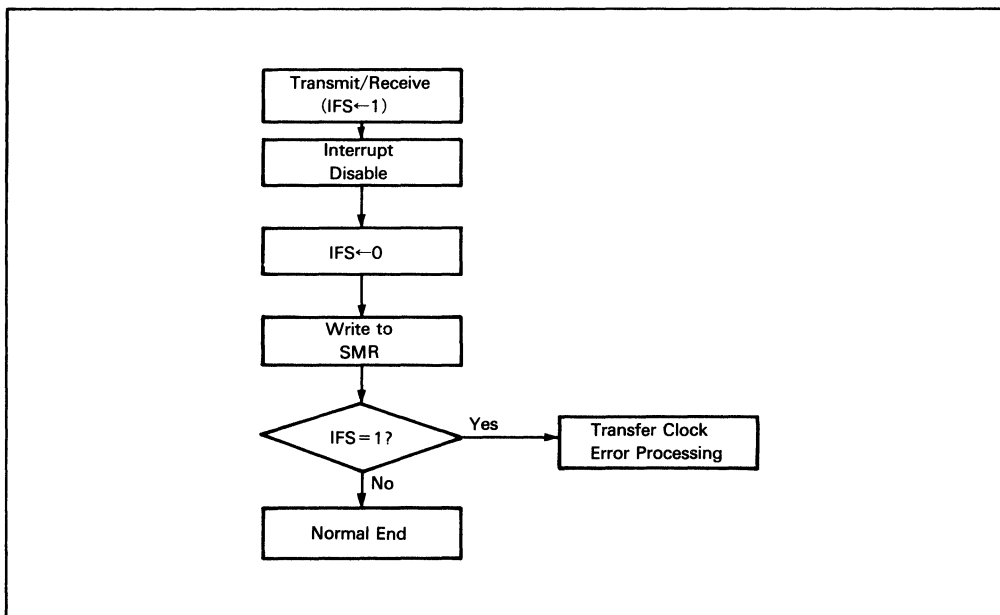


Figure 12. Example of Transfer Clock Error Detection

signal to timer B, select $R3_3/\overline{INT}_1$ as \overline{INT}_1 and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. Then, if the auto-reload function is selected, timer B is initialized to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: \$008): The 3-bit write-only timer mode register A controls the prescaler divide ratio of timer A clock input, as shown in table 11. The timer mode register A is initialized to \$0 by MCU reset.

Timer Mode Register B (TMB: \$009): The 4-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Timer B should be initialized by writing data into the timer load register after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: \$00A, TCBU: \$00B, TLR: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: \$00A, TLR: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B) (figure 2).

The timer/event counter can be initialized by

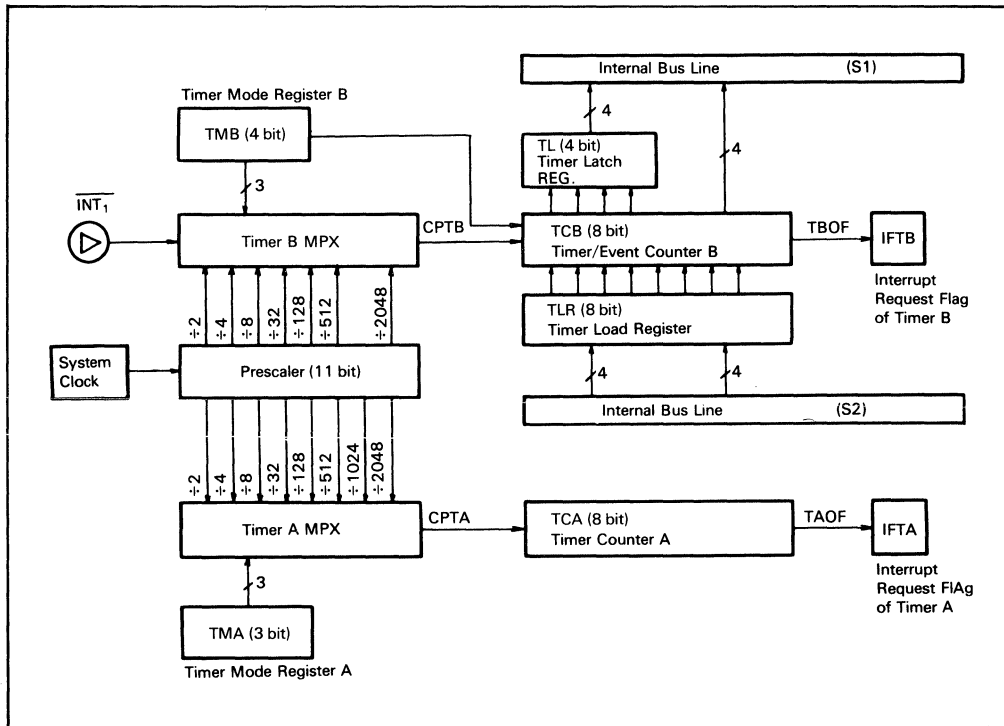


Figure 13. Timer Block Diagram



writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set by the timer A overflow output

(table 13).

Timer A Interrupt Mask (IMTA: \$001 bit 3): Timer A interrupt mask prevents an interrupt request generated by the timer A interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 15).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag (table 16).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler	Divide Ratio
0	0	0	÷	2048
0	0	1	÷	1024
0	1	0	÷	512
0	1	1	÷	128
1	0	0	÷	32
1	0	1	÷	8
1	1	0	÷	4
1	1	1	÷	2

Table 12. Timer Mode Register B

TMB3			Auto-reload Function
0			No
1			Yes

			Prescaler Divide Ratio, Clock Input Source
TMB2	TMB1	TMB0	
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

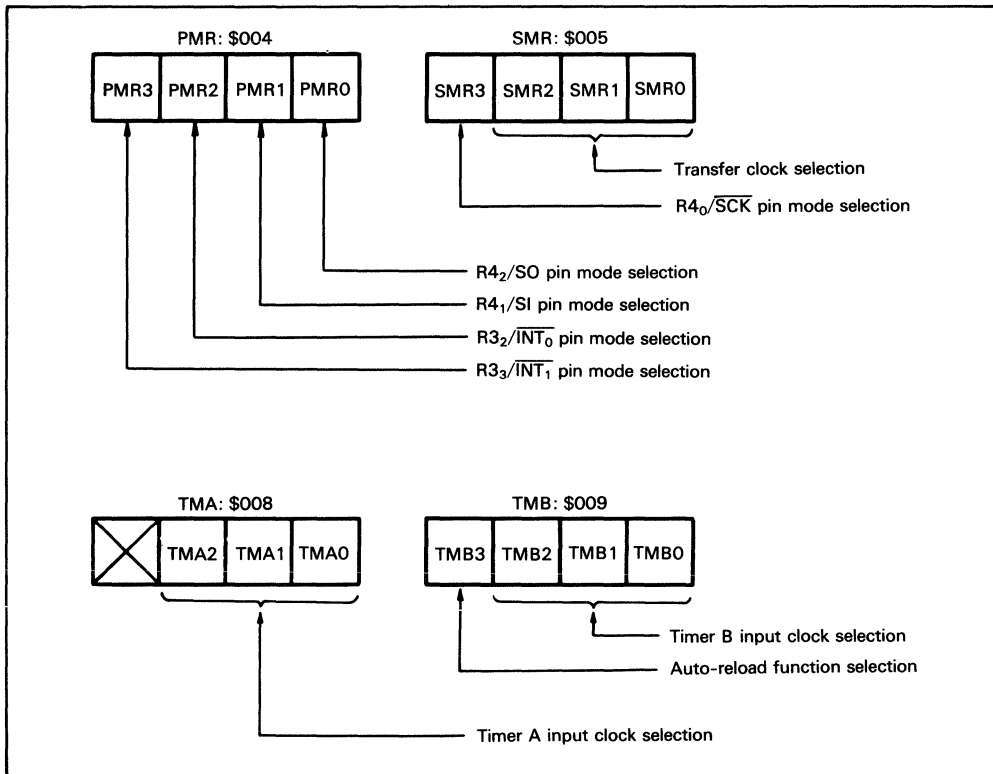


Figure 14. Mode Register Configuration and Function

Input/Output

The MCU has 36 I/O pins, 12 standard and 24 high voltage. One of three circuit types can be selected by mask option for each standard pin: CMOS, with pull-up MOS, and without pull-up MOS (NMOS open drain). One of two circuit types can be selected for each high-voltage pin: with pull-down MOS and without pull-down MOS (PMOS open drain). Since the pull-down MOS is connected to the internal V_{disp} line, V_{disp} must be selected for the RA_1/V_{disp} pin via mask option when at least one high-voltage pin is selected as with pull-down MOS. See table 17 for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 18.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 15 is used to shorten rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the \overline{HLT} signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D port I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 17 as for the classification of standard pin, high-voltage pin, and the I/O

pin circuit types.

R Ports: The six R ports in the HMCS424 are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read from the output-only and/or non-existing ports.

The $R3_2$, $R3_3$, $R4_0$, $R4_1$, and $R4_2$ pins are multiplexed with the \overline{INT}_0 , \overline{INT}_1 , SCK, SI, and SO pins respectively. See table 17 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage pins: select without pull-down MOS (PMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard pins: Select without pull-up MOS (NMOS open drain) via mask option and connect to GND on the printed circuit board.

$R4_0/\overline{SCK}$ and $R4_2/SO$ should be set to $R4_0$ and $R4_2$ by serial mode register and port mode register respectively.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 19 shows the parts initialized by MCU reset, and the status of each. Table 20 shows how registers recover from stop mode.

Table 17. I/O Pin Circuit Types

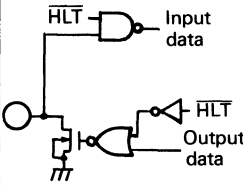
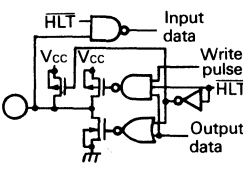
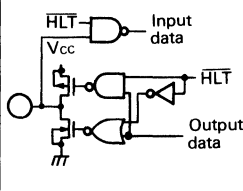
		Without pull-up MOS (NMOS open drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable pins
Standard Pins	I/O Common Pins				D ₀ -D ₃ R ₃₀ -R ₃₃ R ₄₀ -R ₄₃

Table 17. I/O Pin Circuit Types (Cont)

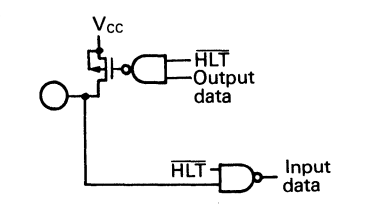
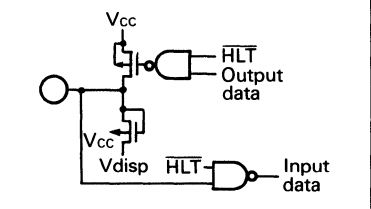
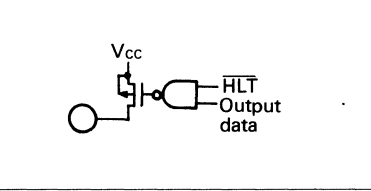
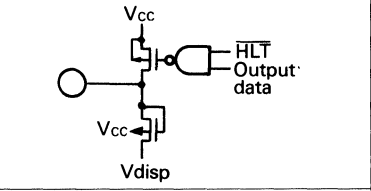
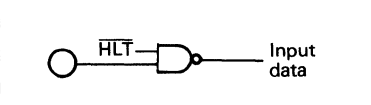
		Without pull-down MOS (PMOS open drain) (D)	With pull-down MOS (E)	Applicable pins
High Voltage Pins	I/O Common Pins			D ₄ -D ₁₅ R ₁₀ -R ₁₃ R ₂₀ -R ₂₃
	Output Pins			R ₀₀ -R ₀₃
	Input Pins			RA ₁

Table 17. I/O Pin Circuit Types (Cont)

	Without pull-up MOS (NMOS open drain) or CMOS (A or C)	With pull-up MOS (B)	Applicable pins
Standard Pins	<p>I/O Common Pins</p>		<p>SCK (Note 2) (Output mode)</p>
	<p>Output pins</p>		<p>SO</p>
	<p>Input Pins</p>		<p>$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$ SI $\overline{\text{SCK}}$ (Input mode)</p>

Note: 1. In the stop mode, HLT signal is 0, HLT signal is 1 and I/O pins are in high impedance state.
 2. If the MCU is interrupted by serial interface in the external clock input mode, the SCK terminal becomes input only.

HMCS424C/HMCS424CL/HMCS424AC

Table 18. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	CMOS	No	—
	Without pull-up MOS (NMOS open drain)	Yes	1
	With pull-up MOS	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0
	With pull-down MOS	Yes	0

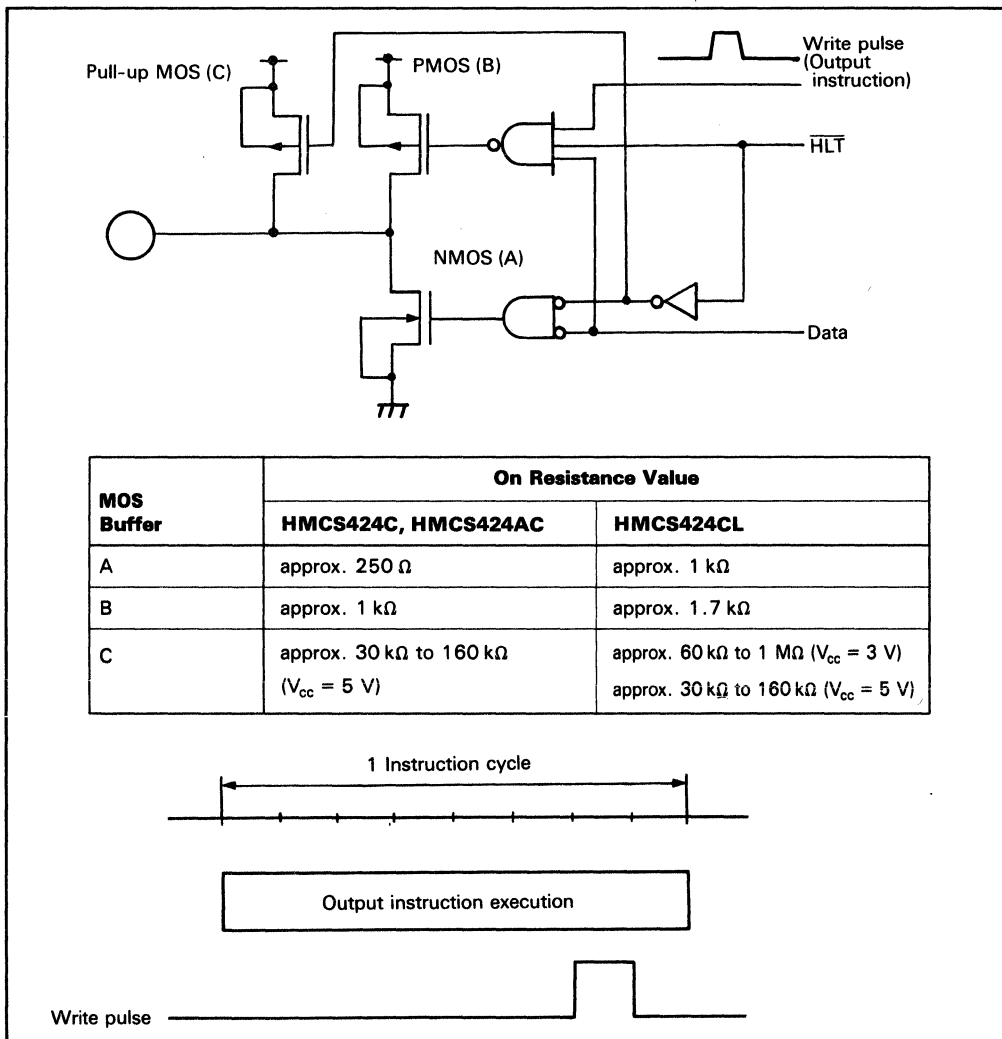


Figure 15. Output Circuit Operation of Standard Pins With Pull-Up MOS Option



Table 19. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top ROM address
Status (ST)		1	Enable to branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin Without Pull-Up MOS	1	Enable input
	With Pull-Up MOS	1	Enable input
	CMOS	1	—
	High Voltage Pin Without Pull-Down MOS	0	Enable input
	With Pull-Down MOS	0	Enable input
	Interrupt Flag	Interrupt Enable Flag (I/E)	0
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Serial Mode Register (SMR)	0000	See serial mode register
	Timer Mode Register A (TMA)	000	See timer mode register A
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Counter A (TCA)	\$00	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—
	Octal Counter	000	—

Table 20. Initial Value after Stop Reset

Item		After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop Mode)
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.

Internal Oscillator Circuit

Figure 16 outlines the internal oscillator circuit. Through mask option, either crystal oscillator or ceramic filter oscillator can be selected as the oscillator type. Refer to table 22 for selection of the type. In addition, see

figure 17 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available. Two divide ratios, 1/8, and 1/4, are selectable via mask option (table 21).

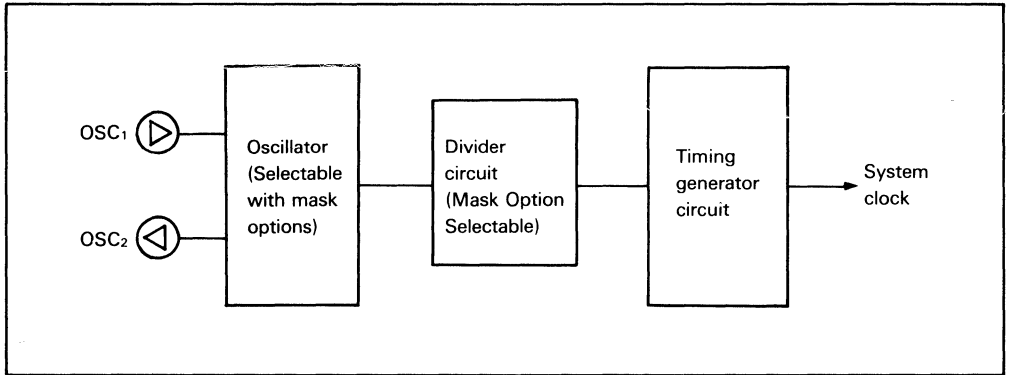


Figure 16. Internal Oscillator Circuit

Table 21. Internal Oscillation Circuit Mask Option

		HMCS 424C	HMCS 424CL	HMCS 424AC
Divider	1/8	○	○	—
	1/4	○	—	○
Oscillator	Crystal	○	○	○
	Ceramic	○	○	○

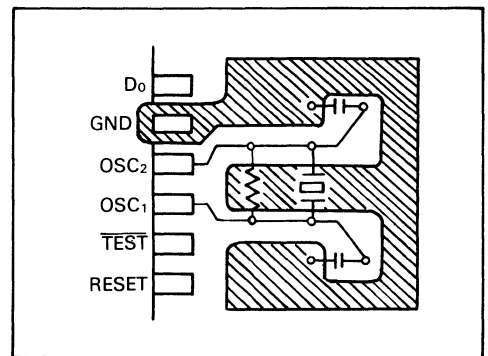


Figure 17. Layout of Crystal and Ceramic Filter

HMCS424C/HMCS424CL/HMCS424AC

Table 22. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants		
		HMCS424C	HMCS424CL	HMCS424AC
External Clock Operation	<p>Oscillator</p> <p>OSC₁</p> <p>Open — OSC₂</p>			
Ceramic Filter Oscillator		Ceramic filter CSA 4.00MG CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA 2.000MK (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$	Ceramic filter CSA4.00MG (Murata) $R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$
Crystal Oscillator	<p>Crystal</p> <p>AT cut parallel resonance crystal</p> <p>OSC₁</p> <p>OSC₂</p> <p>Crystal</p> <p>GT cut parallel resonance crystal</p> <p>OSC₁</p> <p>OSC₂</p>	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$	/	$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$
	<p>Crystal</p> <p>GT cut parallel resonance crystal</p> <p>OSC₁</p> <p>OSC₂</p>		$R_f: 2\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown $C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}2.25\text{ MHz}$	/

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 17).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 23). Figure 18 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 23. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Input/Output Pin	Timer/Counter, Serial Interface	Recovery Method
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained (Note 3)	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET (Note 1)	Stop	Retained	High impedance (Note 2)	Stop	RESET input

- Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to table 19 for the contents of the flags and registers.
 2. A high-voltage pin with a pull-down MOS is tied to the V_{disp} power supply through the pull-down MOS. As the pull-down MOS stays on, a pull-down current flows when a difference between the pin voltage and the V_{disp} voltage exists. This is in addition to the current dissipation in stop mode (I_{stop}).
 3. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is in addition to the current dissipation in standby mode.

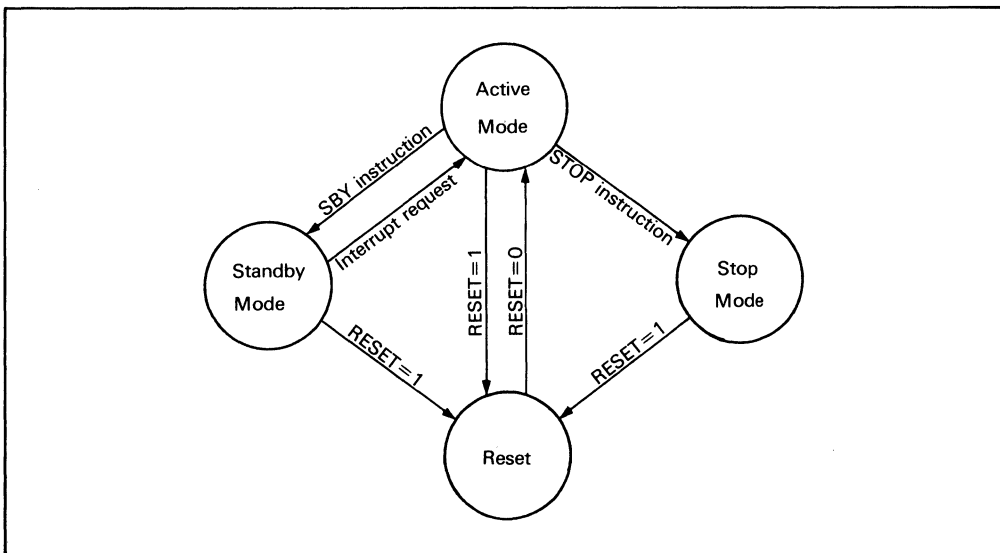


Figure 18. MCU Operation Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 19 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 20, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

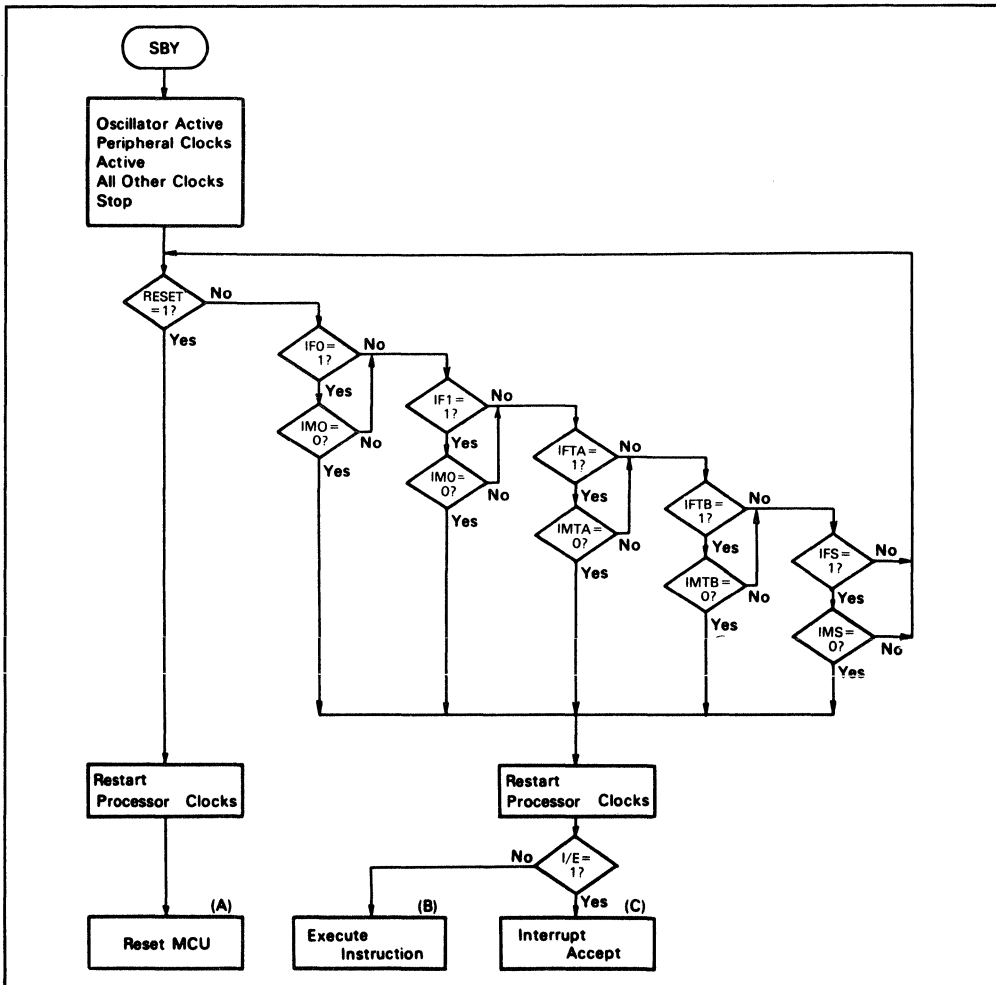


Figure 19. MCU Operating Flowchart in Standby Mode



RAM Addressing Mode

As shown in figure 21, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 22.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on a page boundary ($256n + 255$) (figure 23), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 24). When bit 8 in the ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

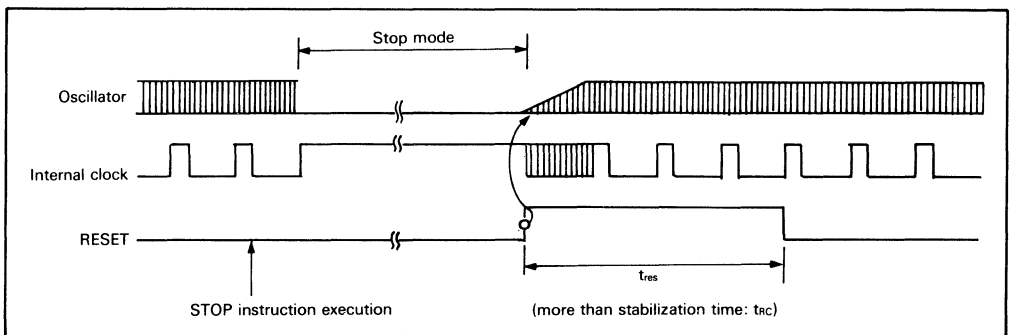


Figure 20. Timing Chart of Recovering from Stop Mode



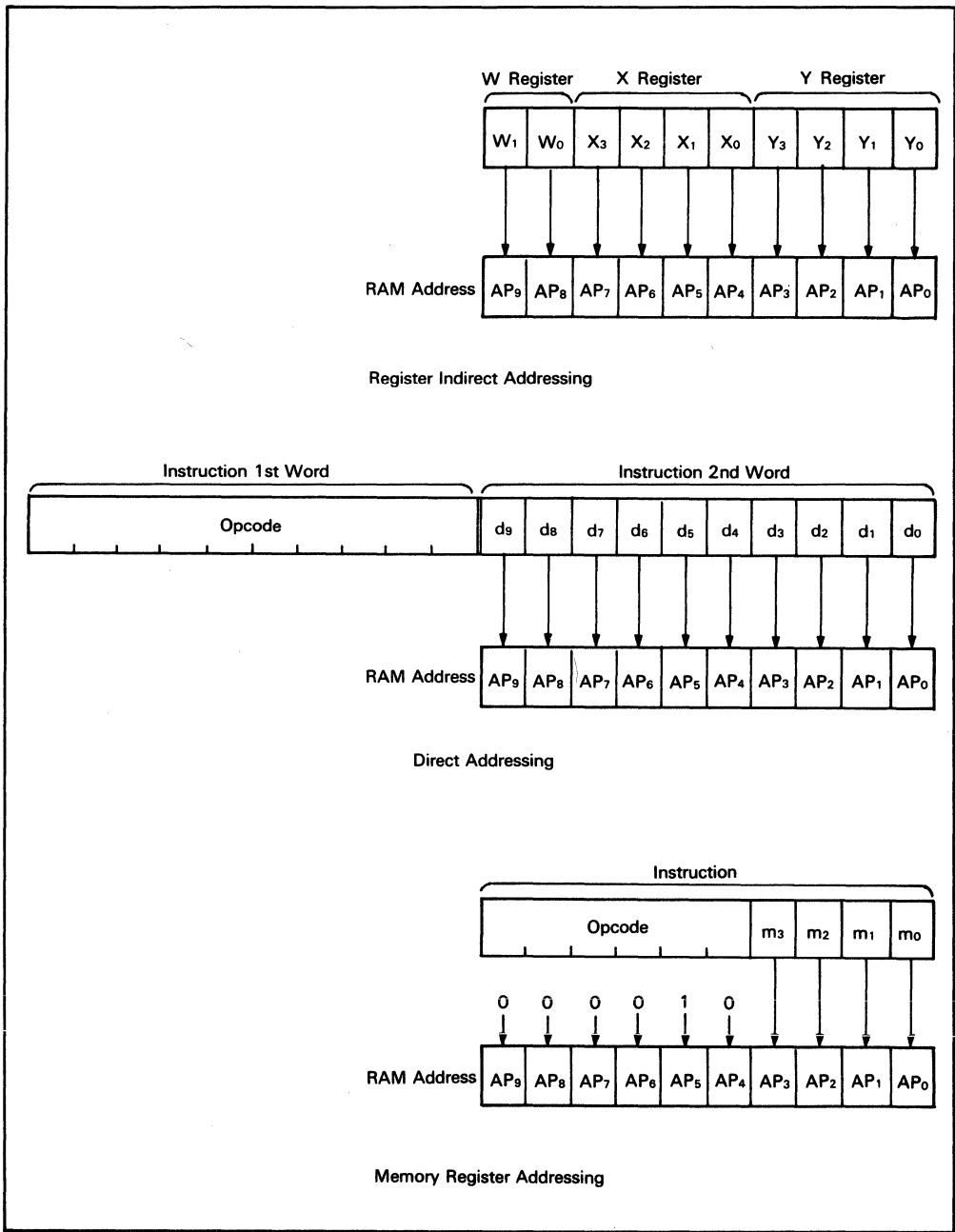


Figure 21. RAM Addressing Mode



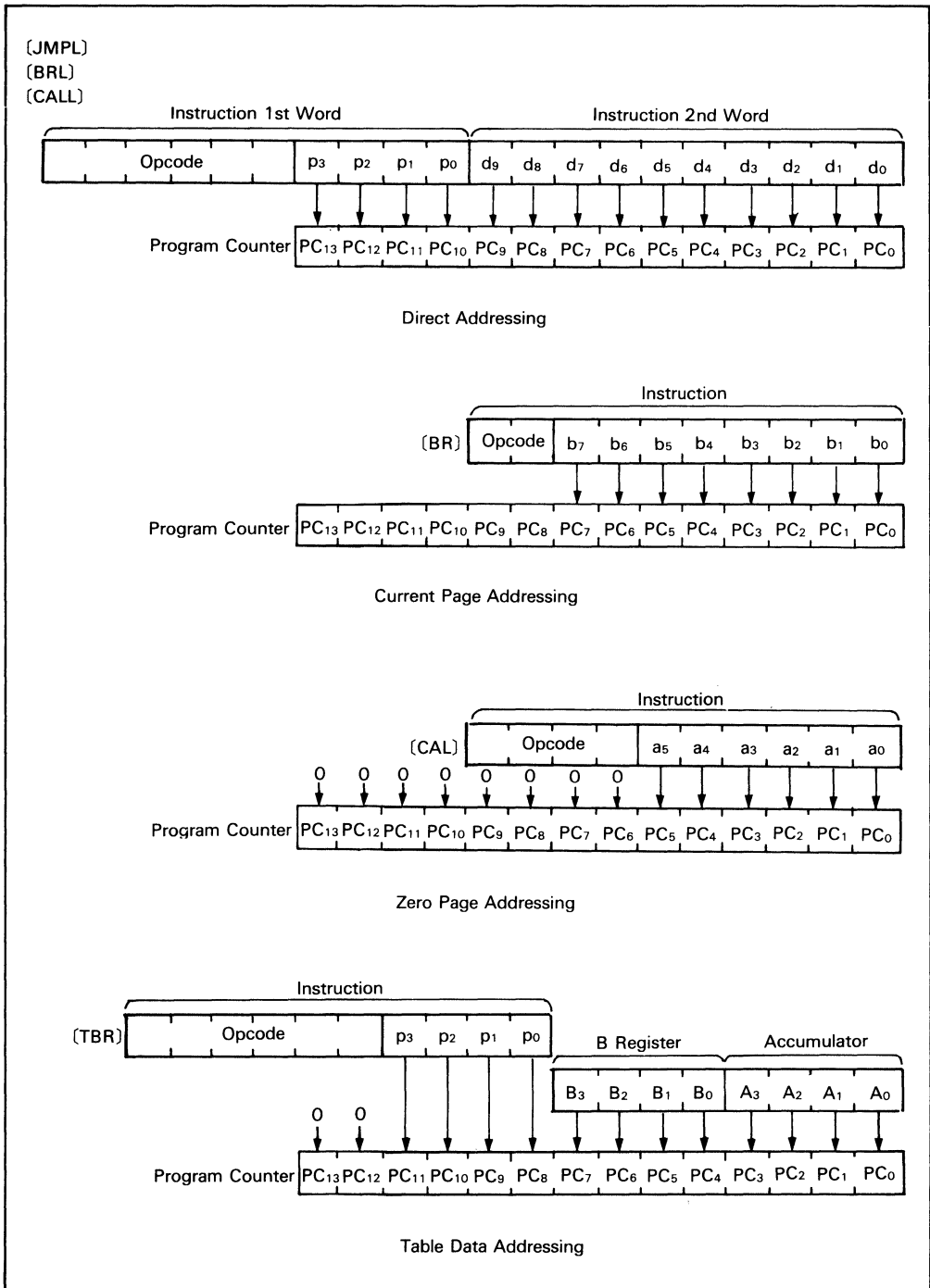


Figure 22. ROM Addressing Mode



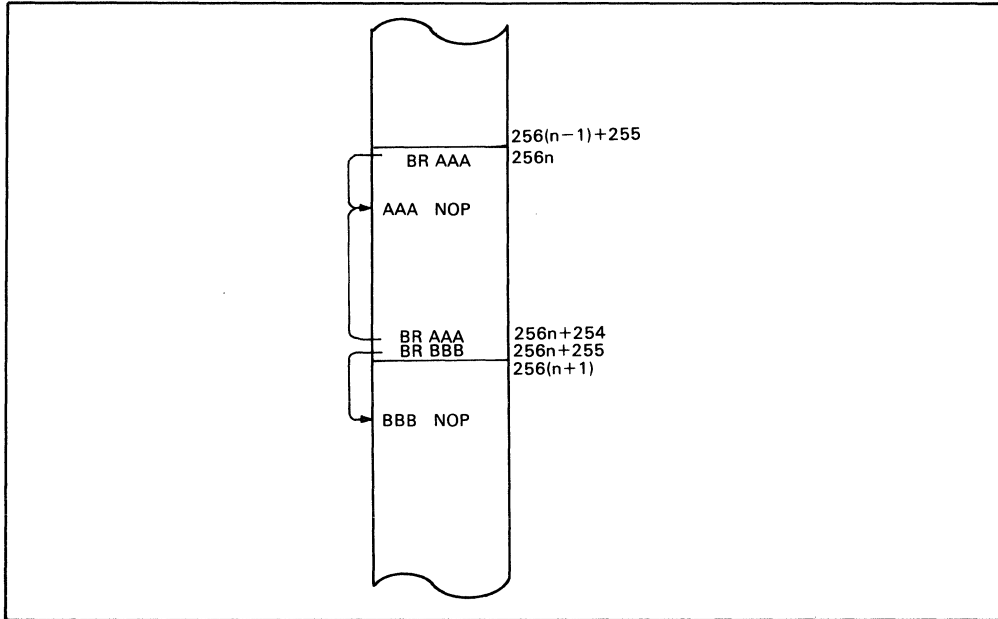


Figure 23. BR Instruction Branch Destination on Page Boundary

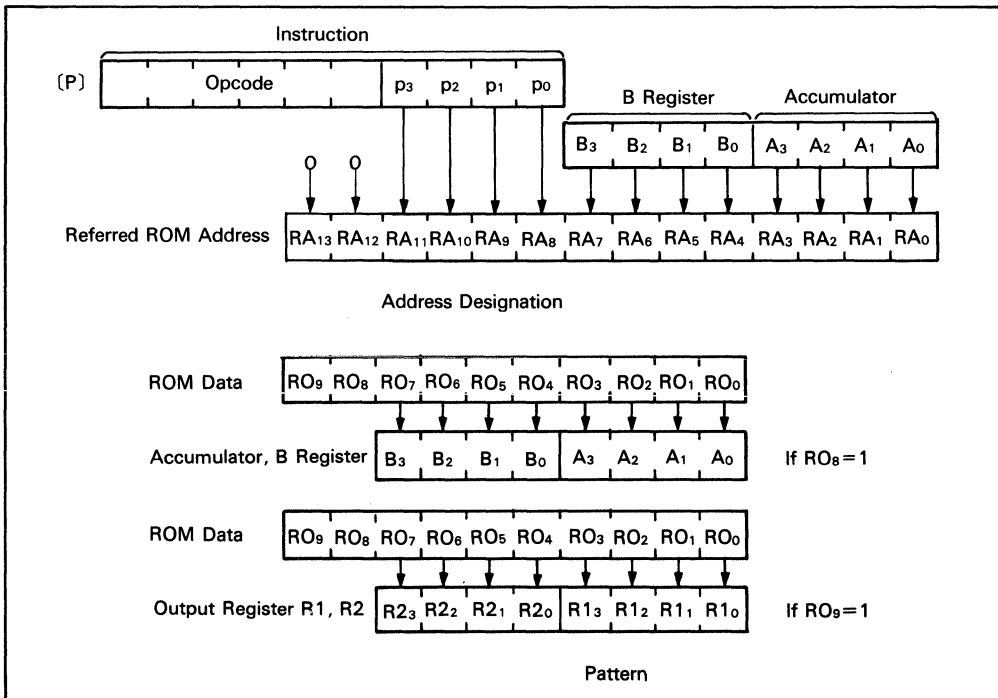


Figure 24. P Instruction



Instruction Set

The HMCS424C/CL/AC provide 99 instructions which are classified into 10 groups as follows:

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. Immediate instruction 2. Register-to-register instruction 3. RAM address instruction 4. RAM register instruction 5. Arithmetic instruction | <ol style="list-style-type: none"> 6. Compare instruction 7. RAM bit manipulation instruction 8. ROM address instruction 9. Input/output instruction 10. Control instruction |
|---|---|

Tables 24-33 list their functions, and table 34 is an opcode map.

Table 24. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 25. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

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Table 26. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Table 27. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y+1 → Y (X → SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y-1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

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Table 28. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 0 $i_3 i_2 i_1 i_0$	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 $d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR



Table 29. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \neq M$	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \neq M$	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	$A \neq M$	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \neq M$	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	$B \neq M$	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	$Y \neq i$	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \leq M$	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \leq M$	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	$A \leq M$	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \leq M$	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	$B \leq M$	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	$A \leq i$	NB	1/1

Table 30. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	$1 \rightarrow M(n)$		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$1 \rightarrow M(n)$		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	$0 \rightarrow M(n)$		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$0 \rightarrow M(n)$		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		$M(n)$	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		$M(n)$	2/2

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Table 31. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 32. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

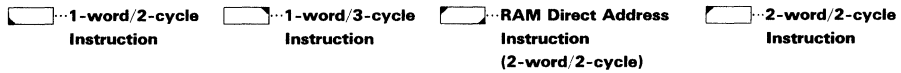
Table 33. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1



Table 34. Opcode Map

R8		O																1																	
R9	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
			0	NOP	XSPX	XSPY	XSPAN	EM			AM				ORM								ANEMC			AMC					ORMC				
			1	RTN	RTNI		ALEM				AMC				EORM								ALEM			AMC					EORMC				
			2	INEM								i(4)				INEMD								i(4)											
			3	ILEM								i(4)				ILEMD								i(4)											
			4	LBM(XY)		BNEM		LAB		IB		COMB		OR		STS		SBY		STOP															
			5	LMAY(X)		AYY		LASPY		IY		JMPL								p(4)															
			6	NEGA		RED		LASPX		TC		CALL								p(4)															
0			7	YNEI								i(4)				BRL								p(4)											
			8	XMA(XY)		SEM n(2)		REM n(2)		TM n(2)		XAMD		SEMD n(2)		REMD n(2)		TMD n(2)																	
			9	LAM(XY)		LMA(XY)		SMC		ANM		LAMD		LMAD		SMCD		ANMD																	
			A	ROTR		ROTL		DAA		DAS		LAY		LMID								i(4)													
			B	TBR								p(4)				P								p(4)											
			C	XMB(XY)		BLEM		LBA		DB																									
			D	LMADY(X)		SY		LYA		DY																									
			E	TD		SED		LXA		REC		SEC		CAL								a(6)													
			F	LWI								i(2)																							
			0	LBI								i(4)																							
			1	LYI								i(4)																							
			2	LXI								i(4)																							
			3	LAI								i(4)																							
			4	LBR								m(4)																							
			5	LAR								m(4)																							
			6	REDD								m(4)																							
1			7	LAMR								m(4)												BR		b(8)									
			8	AI								i(4)																							
			9	LMIIY								i(4)																							
			A	TDD								m(4)																							
			B	ALEI								i(4)																							
			C	LRB								m(4)																							
			D	LRA								m(4)																							
			E	SEDD								m(4)																							
			F	XMRA								m(4)																							



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	25	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$- I_O$	4 (2)	mA	9, 10, 13
		6 (3)	mA	9, 11, 13
		30 (15)	mA	9, 12, 13
Total Allowance of Output Current	$-\Sigma I_O$	85 (100)	mA	6, 13
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input currents which flow in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output currents which flow out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. D_0-D_3 , R3 and R4.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. D_0-D_3 , R3 and R4.
 11. R0-R2.
 12. D_4-D_{14} .
 13. $-\Sigma I_O = 100$ mA if $- I_O$ is equal to or less than 2 mA, 3 mA, or 15 mA.

Electrical Characteristics

DC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
 HMCS424C: $V_{CC} = 3.5$ V to 6 V,
 HMCS424CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS424AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, $\overline{\text{SCK}}$, R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / $\overline{\text{INT}}_1$	0.8 V_{CC}	$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	$V_{CC} + 0.3$	V	HMCS424C/AC	
			$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	HMCS424CL	
Input Low Voltage	V_{IL}	RESET, $\overline{\text{SCK}}$, R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / $\overline{\text{INT}}_1$	-0.3	0.2 V_{CC}	V		
		SI	-0.3	0.3 V_{CC}	V		
		OSC ₁	-0.3	0.5	V	HMCS424C/AC	
			-0.3	0.3	V	HMCS424CL	
Output High Voltage	V_{OH}	$\overline{\text{SCK}}$, SO	$V_{CC} - 1.0$		V	HMCS424C/AC; - $I_{OH} = 1.0$ mA	
			$V_{CC} - 0.5$		V	HMCS424C/AC; - $I_{OH} = 0.5$ mA HMCS424CL; - $I_{OH} = 0.3$ mA	
Output Low Voltage	V_{OL}	$\overline{\text{SCK}}$, SO		0.4	V	HMCS424C/AC; $I_{OL} = 1.6$ mA HMCS424CL; $I_{OL} = 0.4$ mA	
Input/Output Leakage Current	$ I_{IL} $	RESET, $\overline{\text{SCK}}$, R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / $\overline{\text{INT}}_1$, SI, SO, OSC ₁		1	μA	$V_{in} = 0$ V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		2	mA	HMCS424C; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 8$, or $f_{osc} = 2$ MHz, $\div 4$	2,5
				0.7	mA	HMCS424CL; $V_{CC} = 3$ V; $f_{osc} = 2$ MHz, $\div 8$	2,5
				3.2	mA	HMCS424AC; $V_{CC} = 5$ V; $f_{osc} = 4$ MHz, $\div 4$	2,5

HMCS424C/HMCS424CL/HMCS424AC

Item	Symbol	Pin	Min	Max	Unit	Test Condition	Note
Current Dissipation in Standby Mode	I _{SBY}	V _{CC}		1.2	mA	HMCS424C; V _{CC} = 5 V; f _{osc} = 4 MHz, ÷ 8, or f _{osc} = 2 MHz, ÷ 4	3,5
				0.5	mA	HMCS424CL; V _{CC} = 3 V; f _{osc} = 2 MHz, ÷ 8	3,5
				1.7	mA	HMCS424AC; V _{CC} = 5 V; f _{osc} = 4 MHz, ÷ 4	3,5
Current Dissipation in Stop Mode	I _{stop}	V _{CC}		10	μA	HMCS424C/AC; V _{in} (TEST) = V _{CC} - 0.3 V to V _{CC} ; V _{in} (RESET) = 0 V to 0.3 V HMCS424CL; V _{in} (TEST) = V _{CC} - 0.3 V to V _{CC} ; V _{in} (RESET) = 0 V to 0.2 V	4
Stop Mode Retain Voltage	V _{stop}	V _{CC}	2		V		

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When f_{osc} = x MHz, estimate the current dissipation as follows:
 HMCS424C/AC; Max value @ x MHz = x/4 × (max value @ 4 MHz)
 HMCS424CL; Max value @ x MHz = x/2 × (max value @ 2 MHz)

HMCS424C/HMCS424CL/HMCS424AC

Input/Output Characteristics for Standard Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
 HMCS424C: $V_{CC} = 3.5$ V to 6 V,
 HMCS424CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS424AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R3, R4	0.7 V_{CC}		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R3, R4,	-0.3		0.3 V_{CC}	V		
Output High Voltage	V_{OH}	D ₀ -D ₃ , R3, R4	$V_{CC} - 1.0$			V	HMCS424C/AC; - $I_{OH} = 1.0$ mA	1
		D ₀ -D ₃ , R3, R4	$V_{CC} - 0.5$			V	HMCS424C/AC; - $I_{OH} = 0.5$ mA HMCS424CL; - $I_{OH} = 0.3$ mA	1
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R3, R4			0.4	V	HMCS424C/AC; $I_{OL} = 1.6$ mA HMCS424CL; $I_{OL} = 0.4$ mA	
Input/Output Leakage Current	$ I_{IJ} $	D ₀ -D ₃ , R3, R4			1	μA	$V_{in} = 0$ V to V_{CC}	2
Pull-Up MOS Current	$-I_p$	D ₀ -D ₃ , R3, R4	30	60	150	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	3
		D ₀ -D ₃ , R3, R4	3	15	50	μA	HMCS424CL only; $V_{CC} = 3$ V, $V_{in} = 0$ V	3

- Notes: 1. I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. I/O pins with pull-up MOS selected by mask option.

HMCS424C/HMCS424CL/HMCS424AC

Input/Output Characteristics for High-Voltage Pins

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,

HMCS424C: $V_{CC} = 3.5$ V to 6 V,

HMCS424CL: $V_{CC} = 2.5$ V to 6 V,

HMCS424AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note	
Input High Voltage	V_{IH}	D ₄ -D ₁₄ , R ₁ , R ₂ , RA ₁	0.7 V_{CC}		$V_{CC} + 0.3$	V			
Input Low Voltage	V_{IL}	D ₄ -D ₁₄ , R ₁ , R ₂ , RA ₁	$V_{CC} - 40$		0.3 V_{CC}	V			
Output High Voltage	V_{OH}	D ₄ -D ₁₄	$V_{CC} - 3.0$			V	- $I_{OH} = 15$ mA, HMCS 424 C/CL; $V_{CC} = 5$ V \pm 20% HMCS 424 AC; $V_{CC} = 4.5$ V to 6.0V		
			$V_{CC} - 2.0$			V	- $I_{OH} = 10$ mA, HMCS 424 C/CL; $V_{CC} = 5$ V \pm 20% HMCS 424 AC; $V_{CC} = 4.5$ V to 6.0V		
			$V_{CC} - 1.0$			V	HMCS424C/AC; - $I_{OH} = 4$ mA HMCS424CL; - $I_{OH} = 2.5$ mA		
		R0-R2	$V_{CC} - 3.0$				V	- $I_{OH} = 3$ mA, HMCS 424 C/CL; $V_{CC} = 5$ V \pm 20% HMCS 424 AC; $V_{CC} = 4.5$ V to 6.0V	
			$V_{CC} - 2.0$				V	- $I_{OH} = 2$ mA, HMCS 424 C/CL; $V_{CC} = 5$ V \pm 20% HMCS 424 AC; $V_{CC} = 4.5$ V to 6.0V	
			$V_{CC} - 1.0$				V	HMCS424C/AC; - $I_{OH} = 0.8$ mA HMCS424CL; - $I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	D ₄ -D ₁₄ , R0-R2	$V_{CC} - 37$			V	$V_{disp} = V_{CC} - 40$ V	1	
			$V_{CC} - 37$			V	150k Ω to $V_{CC} - 40$ V	2	
Input/Output Leakage Current	$ I_{II} $	D ₄ -D ₁₄ , R0-R2, RA ₁		20		μA	$V_{in} = V_{CC} - 40$ V to V_{CC}	3	
Pull-Down MOS Current	I_d	D ₄ -D ₁₄ , R0-R2, RA ₁	125	250	600	μA	$V_{disp} = V_{CC} - 35$ V, $V_{in} = V_{CC}$	4	

- Notes: 1. I/O pins with pull-down MOS selected by mask option.
 2. I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. I/O pins with pull-down MOS selected by mask option.



HMCS424C/HMCS424CL/HMCS424AC

AC Characteristics

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$,
 HMCS424C: $V_{CC} = 3.5$ V to 6 V,
 HMCS424CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS424AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	HMCS424C; divide by 8	
			0.2	2	2.25	MHz	HMCS424C; divide by 4	
			0.4	2	2.25	MHz	HMCS424CL; divide by 8	
			0.2	4	4.5	MHz	HMCS424AC; divide by 4	
Instruction Cycle Time	t_{cyc}		1.78	2	20	μs	HMCS424C	
			3.55	4	20	μs	HMCS424CL	
			0.89	1	20	μs	HMCS424AC	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms	HMCS424C/AC	1
					60	ms	HMCS424CL	1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92			ns	HMCS424C; divide by 8 HMCS424AC; divide by 4	2
			203			ns	HMCS424C; divide by 4 HMCS424CL; divide by 8	2

(continued)

HMCS424C/HMCS424CL/HMCS424AC

AC Characteristics (Cont)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t_{CpF}	OSC ₁			20	ns		2
\overline{INT}_0 High Level Width	t_{10H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{10L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{11H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{11L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms	HMCS424C/AC	4
					15	ms	HMCS424CL	4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage (HMCS424C:3.5 V, HMCS424CL; 2.5 V, HMCS424AC; 4.5 V) after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.

2. See figure 25.
3. See figure 26.
4. See figure 27.



Serial Interface Timing Characteristics

AT Transfer Clock Output

(GND = 0 V, $V_{disp} = V_{CC} - 40$ V to V_{CC} , $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$,
 HMCS424C: $V_{CC} = 3.5$ V to 6 V,
 HMCS424CL: $V_{CC} = 2.5$ V to 6 V,
 HMCS424AC: $V_{CC} = 4.5$ V to 6 V)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{scyc}	$\overline{\text{SCK}}$	1			t_{cyc}		1,2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{\text{SCK}}$	0.5			t_{scyc}		1,2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{\text{SCK}}$			100	ns	HMCS424C/AC	1,2
					300	ns	HMCS424CL	1,2
Serial Output Data Delay time	t_{DSO}	SO			300	ns	HMCS424C	1,2
					600	ns	HMCS424CL	1,2
					250	ns	HMCS424AC	1,2
Serial Input Data Set-up Time	t_{SSI}	SI	500			ns	HMCS424C	1
			1000			ns	HMCS424CL	1
			300			ns	HMCS424AC	1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns	HMCS424C/AC	1
			500			ns	HMCS424CL	1

HMCS424C/HMCS424CL/HMCS424AC

AT Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	$\overline{\text{SCK}}$	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	$\overline{\text{SCK}}$	0.5			t_{scyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	$\overline{\text{SCK}}$			100	ns	HMCS424C/AC	1
					300	ns	HMCS424CL	1
Serial Output Data Delay Time	t_{DSO}	SO			300	ns	HMCS424C	1,2
					600	ns	HMCS424CL	1,2
					250	ns	HMCS424AC	1,2
Serial Input Data Set-up Time	t_{SSI}	SI	500			ns	HMCS424C	1
			1000			ns	HMCS424CL	1
			300			ns	HMCS424AC	1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns	HMCS424C/AC	1
			500			ns	HMCS424CL	1

- Notes: 1. See figure 28.
2. See figure 30.

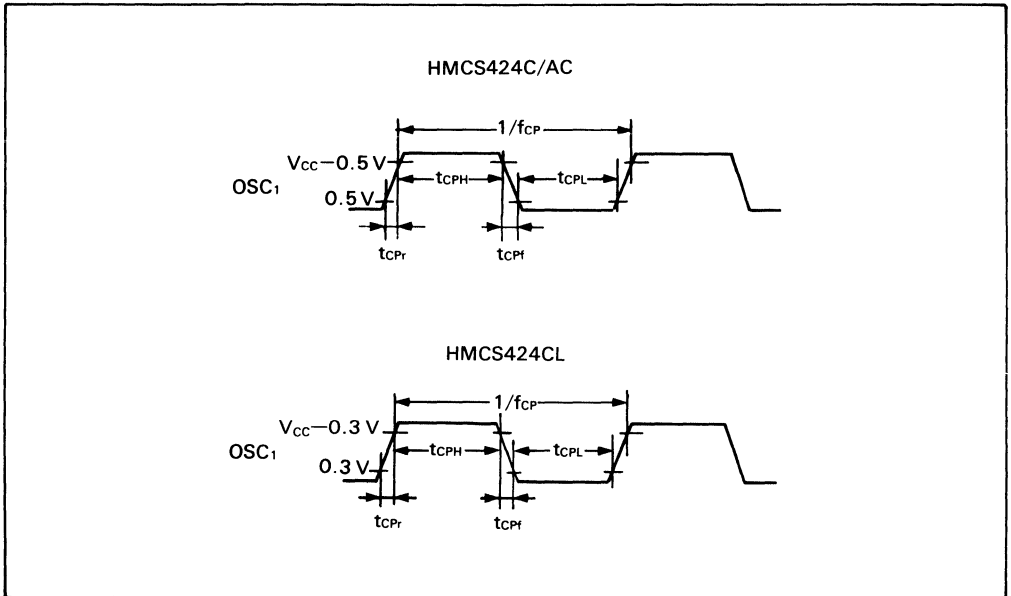


Figure 25. Oscillator Timing

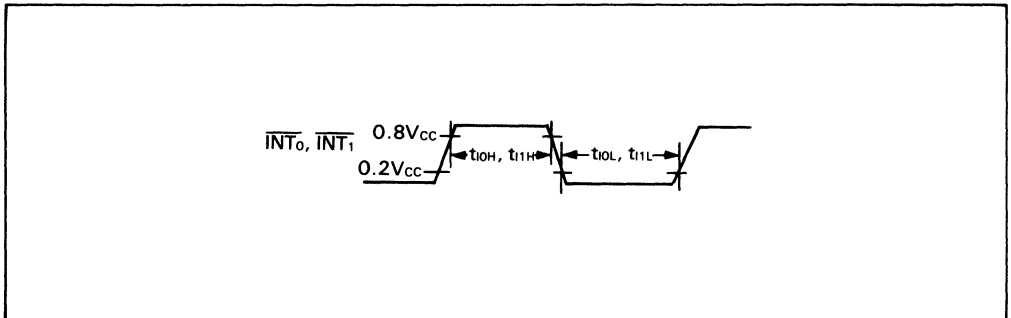


Figure 26. Interrupt Timing

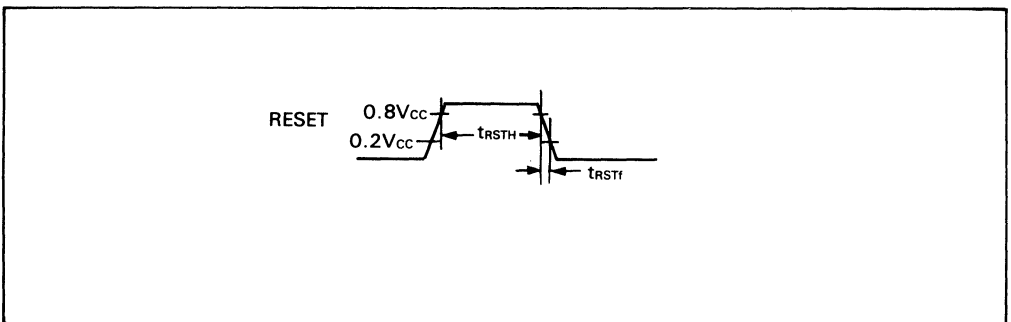


Figure 27. Reset Timing

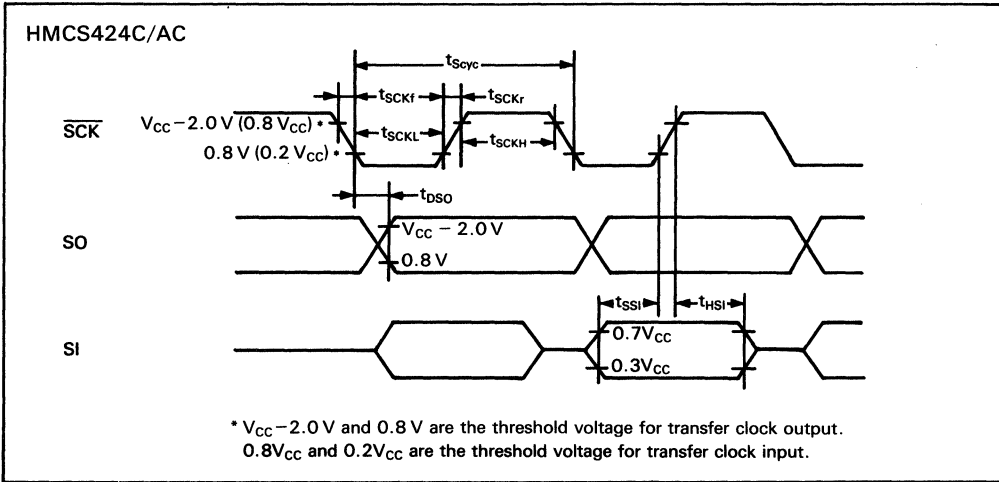


Figure 28. Timing Diagram of Serial Interface

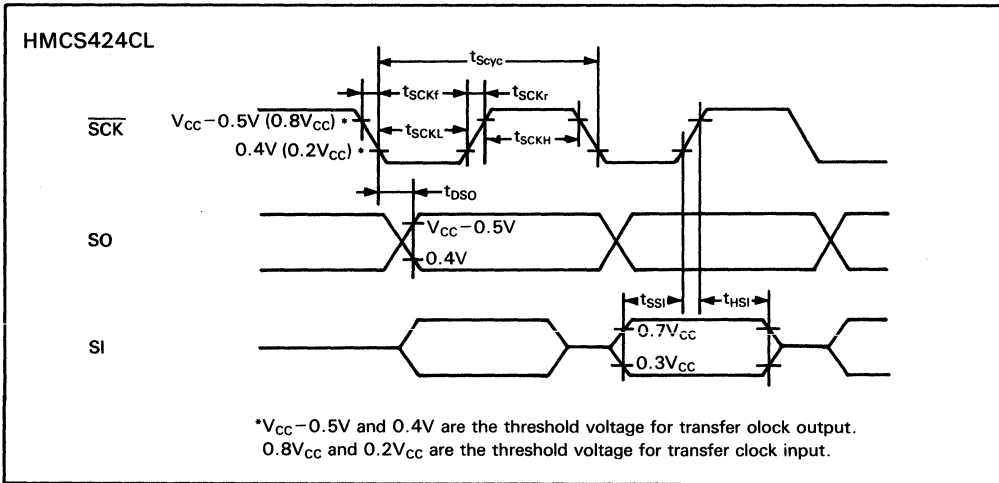


Figure 29. Timing Diagram of Serial Interface

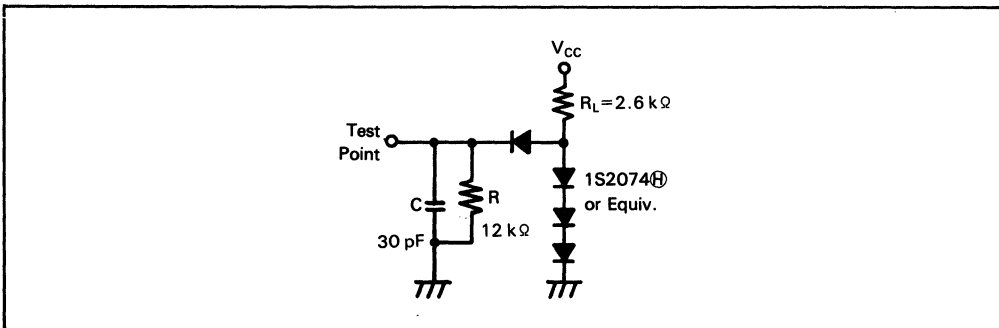


Figure 30. Timing Load Circuit

**HMCS424C/CL/AC
Mask Option List**

• Please enter check marks in
(■, x, ✓).

5V Operation:	<input type="checkbox"/> HMCS424C
3V Operation:	<input type="checkbox"/> HMCS424CL
High Speed Operation:	<input type="checkbox"/> HMCS424AC

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

(1) I/O Option

Please enter 0 in applicable item to select I/O option.

- A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
 C: CMOS (cannot be used as input) D: Without Pull-down MOS (PMOS Open Drain) E: With Pull-down MOS

Note: I/O options masked by ■ are not available.

Pin	Input/Output	I/O Option					Pin	Input/Output	I/O Option					
		A	B	C	D	E			A	B	C	D	E	
D ₀	Standard Pins Input/Output				■	■	R0	R0 ₀	Output	■	■			
D ₁					■	■		R0 ₁	Output	■	■			
D ₂					■	■		R0 ₂	Output	■	■			
D ₃					■	■		R0 ₃	Output	■	■			
D ₄	High Voltage Pins Input/Output	■	■				R1	R1 ₀	Input/Output	■	■			
D ₅		■	■					R1 ₁	Input/Output	■	■			
D ₆		■	■					R1 ₂	Input/Output	■	■			
D ₇		■	■					R1 ₃	Input/Output	■	■			
D ₈		■	■				R2	R2 ₀	Input/Output	■	■			
D ₉		■	■					R2 ₁	Input/Output	■	■			
D ₁₀		■	■					R2 ₂	Input/Output	■	■			
D ₁₁		■	■					R2 ₃	Input/Output	■	■			
D ₁₂		■	■				R3	R3 ₀	Input/Output				■	■
D ₁₃		■	■					R3 ₁	Input/Output				■	■
D ₁₄	■	■				R3 ₂		Input/Output				■	■	
	■	■				R3 ₃		Input/Output				■	■	
						R4	R4 ₀	Input/Output					■	■
							R4 ₁	Input/Output					■	■
							R4 ₂	Input/Output					■	■
							R4 ₃	Input/Output					■	■
RA	RA ₁						High Voltage Pin	Input	Please Mark as RA ₁ /V _{disp}					



HMCS424C/HMCS424CL/HMCS424AC

(2) RA₁/V_{disp}

Please check (■, X, ✓) applicable item.

RA ₁ /V _{disp}	
<input type="checkbox"/>	RA ₁ : Without Pull-down MOS (D)
<input type="checkbox"/>	V _{disp}

Note: RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high pins are option D.

(3) Divider (Div)

Please check (■, X, ✓) applicable item.

Divider	HMCS424C	HMCS424CL	HMCS424AC
8	<input type="checkbox"/>	<input type="checkbox"/>	
4	<input type="checkbox"/>		<input type="checkbox"/>

(4) ROM Code Media

Please check (■, X, ✓) applicable item.

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

(5) Oscillator (CPG option)

Please check (■, X, ✓) applicable item.

CPG option	<input type="checkbox"/> HMCS 424C (5V Operation)	<input type="checkbox"/> HMCS424CL (3V Operation)	<input type="checkbox"/> HMCS424AC (High Speed Operation)
	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock	<input type="checkbox"/> External Clock



HD614P180

Description

The HD614P180 is a 4-bit single chip microcomputer which has mounted a standard EPROM 2764/27128 for program memory.

The HD614P180 is pin-compatible with the mask ROM type HMCS412C, but has some differences with it as shown in Table 26. By modifying the program in the EPROM, it can be used for the evaluation of the HMCS412C or for small-scale production.

HARDWARE FEATURES

- 4-bit Architecture
- Applicable to 4k or 8k words x 10 bits of EPROM
 - 2048 words x 10 bits] HN482764, HN27C64
 - 4096 words x 10 bits] HN4827128
 - 8192 words x 10 bits] HN4827128
- Data Memory (RAM) Capacity 576 digits x 4 bits.
- 36 I/O Pins – 24 I/O pins are high voltage up to 40V (max.).
- 1 Timer/Counter
 - 11-bit Prescaler
 - 8-bit Auto-reload Timer/Event Counter (Timer B)
- 3 Interrupts
 - External 2
 - Timer/Counter 1
- Subroutine Stack
 - Up to 16 levels including interrupts
- Minimum Instruction Execution Time; 1,33 μ s
- 2 Low Power Modes
 - Standby – Stops instruction execution while keeping clock generator and interrupt functions included Timer/Counter in operation
 - Stop – Stops instruction execution and clock generation while retaining RAM data
- Clock Generator
 - External Connection of Crystal Resonator or Ceramic Filter Resonator (externally drivable)
- Power Voltage Range; 5V \pm 10%
- I/O Pin Circuit Form
 - All standard pins are "without pull-up MOS"
 - All high voltage pins are "without pull-down MOS".
- 42 Pin EPROM On-package

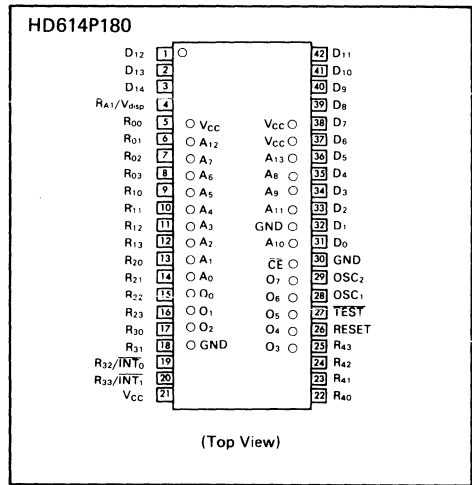
SOFTWARE FEATURES

- Software Compatible with HMCS412/414
- Instruction Set Similar to and More Powerful than HMCS40 Series; 98 Instructions
- High Programming Efficiency with 10-bit ROM/Word; 78 instructions are single word instructions.
- Direct Branch to All ROM Area
- Direct or Indirect Addressing to All RAM Area
- Subroutine Nesting Up to 16 Levels Including Interrupts
- Binary and BCD Arithmetic Operation
- Powerful Logic Arithmetic Operation
- Pattern Generation – Table Look Up Capability –
- Bit Manipulation for Both RAM and I/O

PROGRAM DEVELOPMENT SUPPORT TOOLS

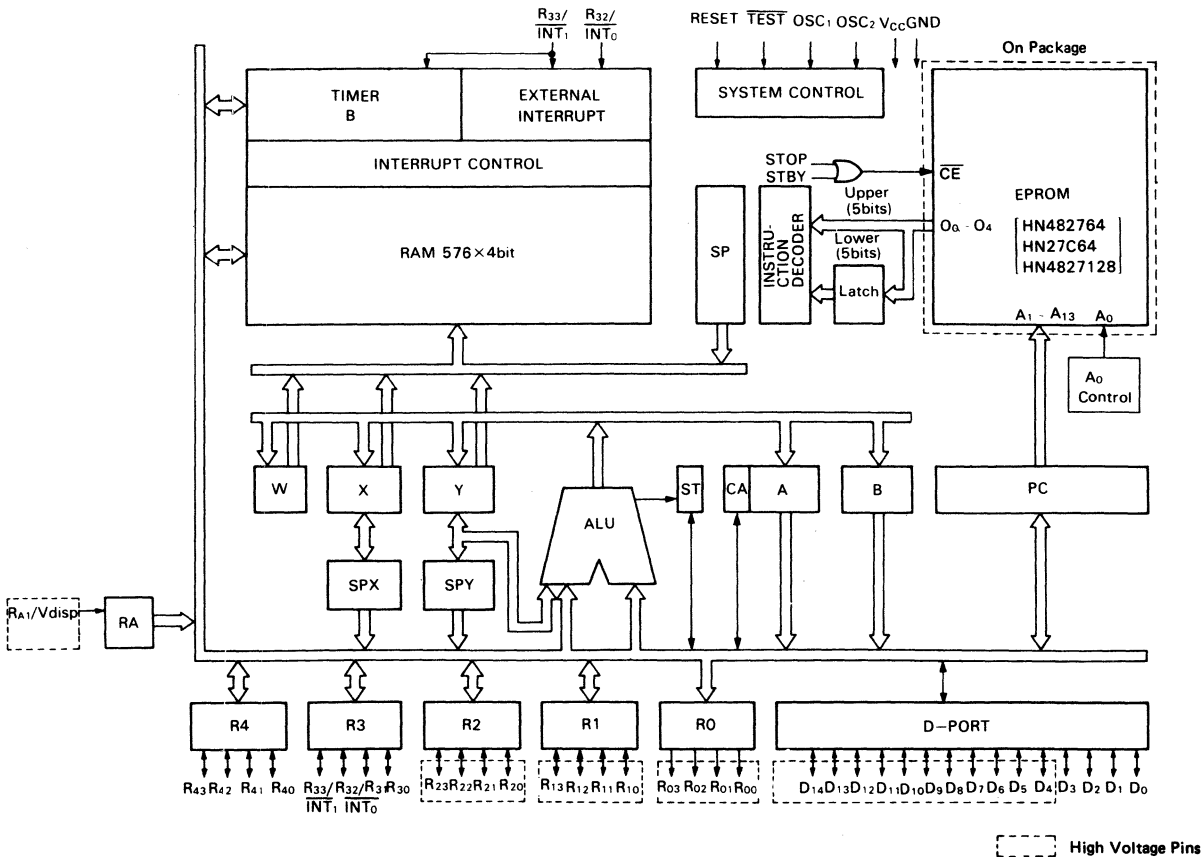
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

PIN ARRANGEMENT



RECOMMENDED APPLICABLE EPROM

Type No.	Program Memory Capacity	f _{osc} (MHz)	EPROM Type No.
HD614P180	2048 words 4096 words	4	HN27C64-30 HN482764-3
		6	HN27C64G-25 HN482764
	8192 words	4	HN4827128-45
		6	HN4827128-25



High Voltage Pins

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Currents	ΣI_O	50	mA	5
Total Allowance of Output Currents	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

(Note 1) Permanent damage may occur if "Absolute Maximum Ratings" of the LSI or the EPROM are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the malfunction and affect the reliability of LSI.

(Note 2) All voltages are with respect to GND.

(Note 3) Applied to standard pins.

(Note 4) Applied to high voltage I/O pins.

(Note 5) Total allowance of input current is the total sum of input current which flow in from all I/O pins to GND simultaneously.

(Note 6) Total allowance of output current is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.

(Note 7) Maximum input current is the maximum amount of input current from each I/O pin to GND.

(Note 8) Applied to $D_0 \sim D_3$ and $R3 \sim R4$.

(Note 9) Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.

(Note 10) Applied to $D_0 \sim D_3$ and $R3 \sim R4$.

(Note 11) Applied to $R0 \sim R2$.

(Note 12) Applied to $D_4 \sim D_{14}$.



HD614P180

■ ELECTRICAL CHARACTERISTICS

- DC CHARACTERISTICS ($V_{CC} = 4.5V$ to $5.5V$, $GND = 0V$, $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Input "High" Voltage	V_{IH}	RESET, INT ₀ , INT ₁		0.7V _{CC}	—	V _{CC} +0.3	V		
		OSC ₁		V _{CC} -0.5	—	V _{CC} +0.3	V		
Input "Low" Voltage	V_{IL}	RESET, INT ₀ , INT ₁		-0.3	—	0.22V _{CC}	V		
		OSC ₁		-0.3	—	0.5	V		
Input/Output Leakage Current	$ I_{IL} $	RESET, INT ₀ , INT ₁ , OSC ₁	$V_{in} = 0V$ to V_{CC}	—	—	1	μA	1	
Current Dissipation in Active Mode	I_{CC}	V _{CC}	V _{CC} =5V	Crystal or Ceramic Filter Oscillator $f_{osc} = 4MHz$	—	—	2.0	mA	2,5
Current Dissipation in Standby Mode	I_{SBY1}	V _{CC}	Maximum Logic Operation V _{CC} = 5V	Crystal or Ceramic Filter Oscillator $f_{osc} = 4MHz$	—	—	1.2	mA	3,5
	I_{SBY2}	V _{CC}	Minimum Logic Operation V _{CC} = 5V	Crystal or Ceramic Filter Oscillator $f_{osc} = 4MHz$	—	—	0.9	mA	4,5
Current Dissipation in Stop Mode	I_{stop}	V _{CC}	$V_{in} (\overline{TEST}) = V_{CC}-0.3V$ to V_{CC} $V_{in} (RESET) = 0V$ to $0.3V$		—	—	10	μA	
Stop Mode Retain Voltage	V_{stop}	V _{CC}			2	—	—	V	

(Note 1) Output buffer current are excluded.

(Note 2) The MCU is in the reset state. The input/output current does not flow.

- Test Conditions: MCU state; ● Reset state in Operation Mode
Pin state; ● RESET, TEST ... V_{CC} voltage
 ● D₀ ~ D₃, R3 ~ R4 ... V_{CC} voltage
 ● D₄ ~ D₄, R0 ~ R2, RA1, RA1 ... V_{CC} ~ V_{CC}-40V

(Note 3) The timer/counter with the fastest clock and input/output current does not flow.

- Test Conditions: MCU state; ● Standby Mode
 ● Input/Output; Reset state
 ● TIMER-B; +2 prescaler divide ratio
Pin state; ● RESET ... GND voltage
 ● TEST ... V_{CC} voltage
 ● D₀ ~ D₃, R3 ~ R4 ... V_{CC} voltage
 ● D₄ ~ D₄, R0 ~ R2, RA1 ... V_{CC} ~ V_{CC}-40V

(Note 4) The timer/counter with the slowest clock and input/output current does not flow.

- Test Conditions: MCU state; ● Standby Mode
 ● Input/Output; Reset state
 ● TIMER-B; +2048 prescaler divide ratio



- Pin state;
- RESET ... GND voltage
 - TEST ... V_{CC} voltage
 - D₀ ~ D₃, R₃ ~ R₄ ... V_{CC} voltage
 - D₄ ~ D₁₄, R₀ ~ R₂, R_{A1} ... V_{CC} ~ V_{CC}-40V

(Note 5) When f_{osc}=x [MHz], the Current Dissipation in Operation mode and Standby mode are estimated as follows:

$$\text{max. value (f}_{\text{osc}}=x[\text{MHz}]) = \frac{x}{4} \times \text{max. value (f}_{\text{osc}}=4[\text{MHz}])$$

● **INPUT/OUTPUT CHARACTERISTICS FOR STANDARD PIN**
(V_{CC} = 4.5V to 5.5V, GND = 0V, T_a = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₀ ~ D ₃ , R ₃ ~ R ₄		0.7V _{CC}	-	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₀ ~ D ₃ , R ₃ ~ R ₄		-0.3	-	0.22V _{CC}	V	
Output "Low" Voltage	V _{OL}	D ₀ ~ D ₃ , R ₃ ~ R ₄	I _{OL} = 1.6 mA	-	-	0.4	V	
Input/Output Leakage Current	I _{IL}	D ₀ ~ D ₃ , R ₃ ~ R ₄	V _{in} = 0V to V _{CC}	-	-	1	μA	1

(Note 1) Output buffer current are excluded.

● **INPUT/OUTPUT CHARACTERISTICS FOR HIGH VOLTAGE PIN**
(V_{CC} = 4.5V to 5.5V, GND = 0V, T_a = -20 to +75°C, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note
				min	typ	max		
Input "High" Voltage	V _{IH}	D ₄ ~ D ₁₄ , R ₁ , R ₂ , R _{A1}		0.7V _{CC}	-	V _{CC} +0.3	V	
Input "Low" Voltage	V _{IL}	D ₄ ~ D ₁₄ , R ₁ , R ₂ , R _{A1}		V _{CC} -40	-	0.22V _{CC}	V	
Output "High" Voltage	V _{OH}	D ₄ ~ D ₁₄	-I _{OH} = 15mA	V _{CC} -3.0	-	-	V	
			-I _{OH} = 9 mA	V _{CC} -2.0	-	-	V	
			-I _{OH} = 3 mA	V _{CC} -3.0	-	-	V	
			-I _{OH} = 1.8 mA	V _{CC} -2.0	-	-	V	
Output "Low" Voltage	V _{OL}	D ₄ ~ D ₁₄ , R ₀ ~ R ₂	150kΩ to V _{CC} -40V	-	-	V _{CC} -37	V	
Input/Output Leakage Current	I _{IL}	D ₄ ~ D ₁₄ , R ₀ ~ R ₂ , R _{A1}	V _{in} = V _{CC} -40V to V _{CC}	-	-	20	μA	1

(Note 1) Output buffer current are excluded.



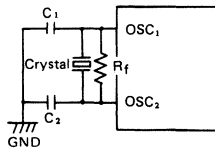
HD614P180

• AC CHARACTERISTICS ($V_{CC} = 4.5V$ to $5.5V$, $GND = 0V$, $T_a = -20$ to $+75^\circ C$, if not specified.)

Item	Symbol	Pin Name	Test Conditions	Value			Unit	Note	
				min	typ	max			
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	4	6.2	MHz		
	Instruction Cycle Time	t_{cyc}		1.29	2	20	μs		
	Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂	—	—	20	ms	1	
External Clock	External Clock Frequency	f_{CP}	OSC ₁	0.4	—	6.2	MHz	2	
	External Clock "High" Level Width	t_{CPH}	OSC ₁	70	—	—	ns	2	
	External Clock "Low" Level Width	t_{CPL}	OSC ₁	70	—	—	ns	2	
	External Clock Rise Time	t_{CPr}	OSC ₁	—	—	20	ns	2	
	External Clock Fall Time	t_{CPf}	OSC ₁	—	—	20	ns	2	
	Instruction Cycle Time	t_{cyc}			1.29	—	20	μs	2
	INT ₀ "High" Level Width	t_{I0H}	INT ₀		2	—	—	t_{cyc}	3
INT ₀ "Low" Level Width	t_{I0L}	INT ₀		2	—	—	t_{cyc}	3	
INT ₁ "High" Level Width	t_{I1H}	INT ₁		2	—	—	t_{cyc}	3	
INT ₁ "Low" Level Width	t_{I1L}	INT ₁		2	—	—	t_{cyc}	3	
RESET "High" Level Width	t_{RSTH}	RESET		2	—	—	t_{cyc}	4	
Input Capacitance	C_{in}	all pins	$f = 1MHz$ $V_{in} = 0V$	—	—	15	pF		
RESET Fall Time	t_{RSTf}			—	—	20	ms	4	

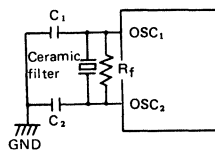
(Note 1) Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage $V_{CC} = 4.5V$ after power-on, or after RESET goes high. At power-on or STOP mode release, RESET Must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.

Crystal oscillator



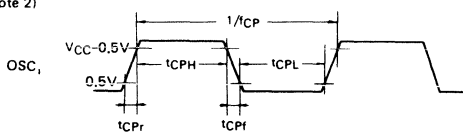
Crystal: 4.194304MHz NC-18C (Nihon Denpa Kogyo)
 R_f : $1M\Omega \pm 2\%$
 C_1 : $22pF \pm 20\%$
 C_2 : $22pF \pm 20\%$

Ceramic filter oscillator

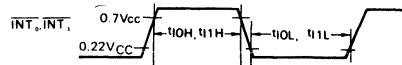


Ceramic filter: CSA4.00MG (Murata)
 R_f : $1M\Omega \pm 2\%$
 C_1 : $30pF \pm 20\%$
 C_2 : $30pF \pm 20\%$

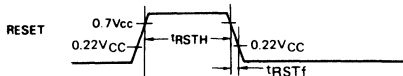
(Note 2)



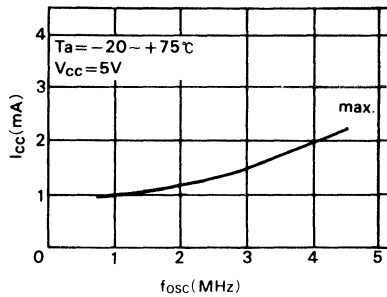
(Note 3)



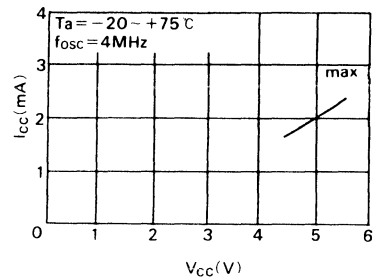
(Note 4)



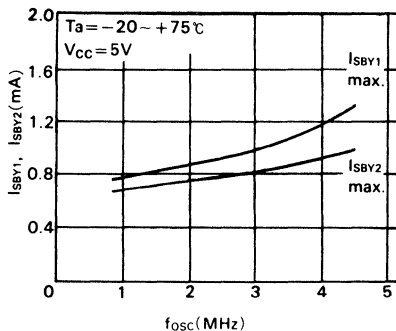
■ CHARACTERISTICS CURVE (REFERENCE DATA)



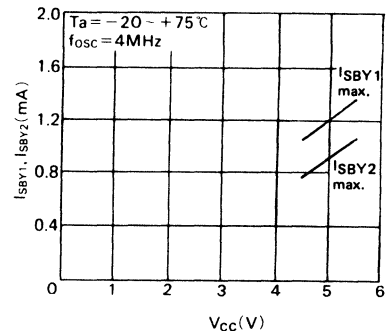
I_{CC} vs. f_{osc} characteristic
(crystal, ceramic resonator)



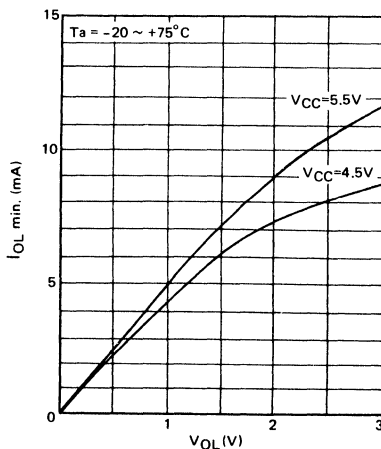
I_{CC} vs. V_{CC} characteristic
(crystal, ceramic resonator)



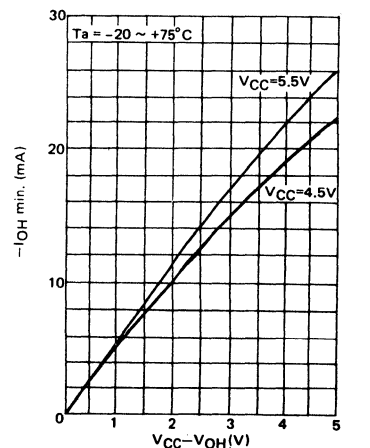
I_{SB1} vs. f_{osc} characteristics
(crystal, ceramic resonator)



I_{SB1} vs. V_{CC} characteristics
(crystal, ceramic resonator)

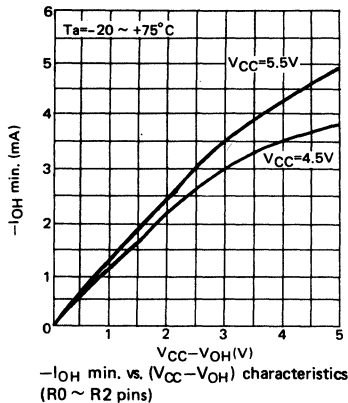


$I_{OL} \text{ min.}$ vs. V_{OL} characteristics
(Standard Pin)



$-I_{OH} \text{ min.}$ vs. $(V_{CC} - V_{OH})$ characteristics
($D_4 \sim D_{14}$ pins)





DESCRIPTION OF PIN FUNCTIONS

Input and output signals of MCU are described below.

GND, V_{CC}, V_{disp}

These are power supply pins. Connect GND pin to Earth (0V) and apply V_{CC} power supply voltage to V_{CC} pin. R_{A1}/V_{disp} pin is used for R_{A1} as all high voltage pins are "without pull-down MOS" (PMOS open drain).

TEST

TEST pin is not for users application. Connect it to V_{CC}.

RESET

RESET pin is used to reset MCU. For details, see "RESET".

OSC₁, OSC₂

These are input pins to the internal clock generator circuit. They can be connected to crystal resonator, ceramic filter resonator, or external oscillator circuit. For details, see "INTERNAL OSCILLATOR CIRCUIT."

D-port (D₀ to D₁₄)

D-port is a 1-bit Input/Output common port. D₀ to D₃ are standard type, D₄ to D₁₄ are for high voltage. For details, see "INPUT/OUTPUT".

R-port (R₀ to R₄, R_A)

R-port is a 4-bit Input/Output port. (only R_A is 1-bit construction.) R₀ is output port, R_A is input port, and R₁ to R₄ are Input/Output common ports. R₀ to R₂ and R_A are the high voltage ports, R₃ to R₄ are the standard ports. R₃₂ and R₃₃ are also available as INT₀ and INT₁, respectively. For details, see "INPUT/OUTPUT".

INT₀, INT₁

These are the input pins to interrupt MCU operation externally. INT₁ can be used as an external event input pin for TIMER-B. INT₀ and INT₁ are also available as R₃₂ and R₃₃ respectively. For details, see "INTERRUPT".

ROM MEMORY MAP

ROM memory map is illustrated in Fig. 1 and described in the following paragraph.

Vector Address Area \$0000 to \$000F

When MCU reset or an interrupt is serviced, the program is executed from the vector address. Program the JMPL instructions branching to the starting addresses of reset routine or of interrupt routines.

Zero-Page Subroutine Area \$0000 to \$003F

CAL instruction allows to branch to the subroutines in \$0000 to \$003F.

Pattern Area \$0000 to \$0FFF

P instruction allows referring to the ROM data in \$0000 to \$0FFF as a pattern.

Program Area \$0000 to \$1FFF

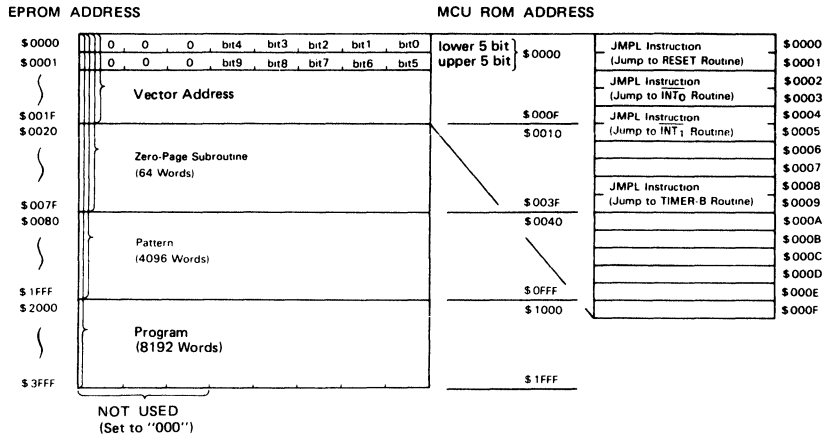
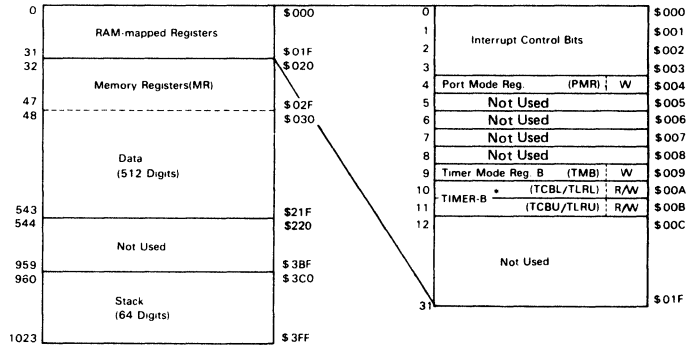


Fig. 1 ROM Memory Map



* Two registers are mapped on same address.

R : Read Only
W : Write Only
R/W : Read/Write

Timer/Event Counter B Lower (TCBL)	R	Timer Load Reg Lower (TLRL)	W	\$00A
Timer/Event Counter B Upper (TCBU)	R	Timer Load Reg Upper (TLRU)	W	\$00B

Fig. 2 RAM Memory Map

RAM MEMORY MAP

The MCU includes 576 digits x 4 bits RAM as the data area and stack area. In addition to these areas, interrupt control bits

and special registers are also mapped on the RAM memory space. RAM memory map is illustrated in Fig. 2 and described in the following paragraph.



	bit 3	bit 2	bit 1	bit 0	
0	IMO (IM of $\overline{INT_0}$)	IFO (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	Not Used	Not Used	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	\$001
2	Not Used	Not Used	IMTB (IM of TIMER-B)	IFTB (IF of TIMER-B)	\$002
3	Not Used	Not Used	Not Used	Not Used	\$003

IF : Interrupt Request Flag
 IM : Interrupt Mask
 I/E : Interrupt Enable Flag
 SP : Stack Pointer

(Note) Each bit in Interrupt Control Bits Area is set by SEM/SEMD instruction, is reset by REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, Interrupt Request Flag is not affected by SEM/SEMD instruction. The content of Status becomes invalid when "RSP" bit and "Not Used" bit is tested.

Fig. 3 Configuration of Interrupt Control Bit Area

● **Interrupt Control Bit Area \$000 to \$003**

This area is used for interrupt controls, and is illustrated in Fig. 3. It is accessible only by RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is only used to reset the SP.

● **Special Register Area \$004 to \$00B**

Special Register is a mode or a data register for the external interrupt, the serial interface, and the timer/counter. These registers are classified into 3 types: Write-only, Read-only, and Read/Write as shown in Fig. 2. These registers cannot be accessed by RAM bit manipulation instruction.

● **Data Area \$020 to \$21F**

16 digits of \$020 to \$02F are called memory register (MR) and accessible by LAMR and XMRA instructions.

● **Stack Area \$3C0 to \$3FF**

Stack Area is used for LIFO stacks with the contents of the program counter (PC), status (ST) and carry (CA) when processing subroutine call and interrupt. As 1 level requires 4 digits, this stack area is nested to 16 level-stack max. The data pushed in the stack and LIFO stack state are provided in Fig. 4. The program counter is restored by RTN and RTNI instructions. Status and Carry are restored only by RTNI instruction, and not affected by RTN instruction. The area, not used for stacking, is available as a data area.

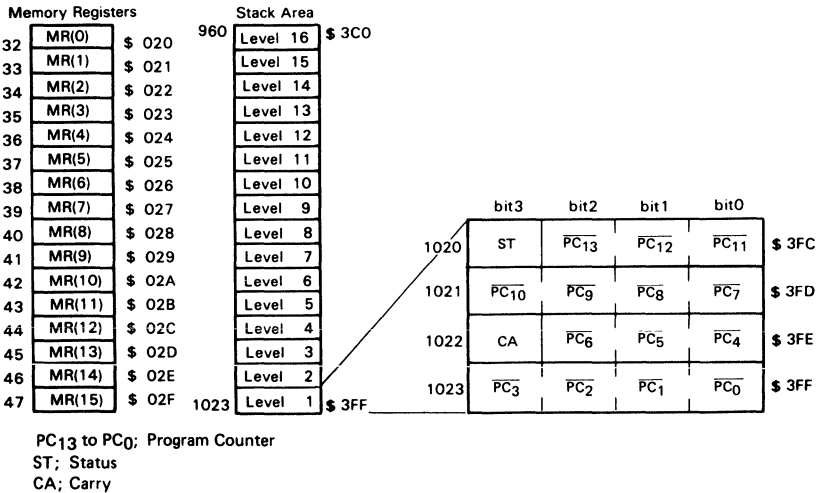


Fig. 4 Configuration of Memory Register, Stack Area and Stack Position

■ REGISTER AND FLAG

The MCU has nine registers and two flags for the CPU operations. They are illustrated in Fig. 5 and described in the following paragraphs.

● Accumulator (A), B Register (B)

Accumulator and B Register are 4-bit registers used to hold the results of Arithmetic Logic Unit (ALU), and to transfer data to/from memories, I/O and other registers.

● W Register (W), X Register (X), Y Register (Y)

W Register is 2-bit, and X and Y Register are 4-bit registers used for indirect addressing of RAM. Y Register is also used for D-port addressing. W Register is write-only and cannot be read.

● SPX Register (SPX), SPY Register (SPY)

SPX and SPY Register are 4-bit registers used to assist X and Y Register respectively.

● Carry (CA)

Carry (CA) stores the overflow of ALU generated by the arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, Carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

● Status (ST)

Status (ST) holds the ALU overflow, ALU non-zero and the results of bit test instruction for the arithmetic or compare instruction. It is used for a branch condition of BR, BRL, CAL or CALL instructions. The value of the Status remains unchanged until the next arithmetic, compare or bit test instruction is executed. Status becomes "1" after the BR, BRL, CAL or CALL instruction has been executed (irrespective of its execution/skip). During the interrupt servicing, Status is pushed onto the

stack and restored back from the stack by RTNI instruction. (It's not affected by RTN instruction.)

● Program Counter (PC)

Program Counter is a 14-bit binary counter for ROM addressing.

● Stack Pointer (SP)

Stack Pointer is used to point the address of the next stacking area up to 16 levels.

The Stack Pointer is initialized to locate \$3FF on the RAM address, and is decremented by 4 as data pushed into the stack, and incremented by 4 as data restored back from the stack.

■ INTERRUPT

The MCU can be interrupted by three different sources: the external signals (INT₀, INT₁) and timer/counter (TIMER-B). In each sources, the Interrupt Request Flag, Interrupt Mask and interrupt vector address will be used to control and maintain the interrupt request. The Interrupt Enable Flag is also used to control the total interrupt operations.

● Interrupt Control Bit and Interrupt Service

The interrupt control bit is mapped on \$000 to \$003 of the RAM address and accessible by RAM bit manipulation instruction. (The Interrupt Request Flag (IF) cannot be set by software.) The Interrupt Enable Flag (I/E) and Interrupt Request Flag (IF) are set to "0", and the Interrupt Mask (IM) is set to "1" at the initialization by MCU reset.

Fig. 6 shows the interrupt block diagram. Table 1 shows the interrupt priority and vector addresses, and Table 2 shows the conditions that the interrupt service is executed by any one of the three interrupt sources.

The interrupt request is generated when the Interrupt Request Flag is set to "1" and the Interrupt Mask is "0". If the Interrupt Enable Flag is "1", then the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the three interrupt sources.

Fig. 7 shows the interrupt services flowchart, and Fig. 8 shows the interrupt sequence. If the interrupt is requested, the instruction finishes its execution in the first cycle. The Interrupt Enable Flag is reset in the second cycle. In the second and third cycles, the Carry, Status and Program Counter are pushed onto the stack. In the third cycle, the instruction is executed again after jumping to the vector address.

In each vector address, program JMPL instruction to branch to a starting address of the interrupt routine. The Interrupt Request Flag which caused the interrupt service has to be reset by software in the interrupt routine.

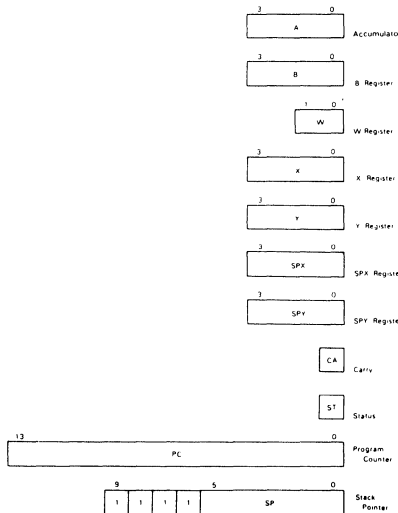


Fig. 5 Register and Flags

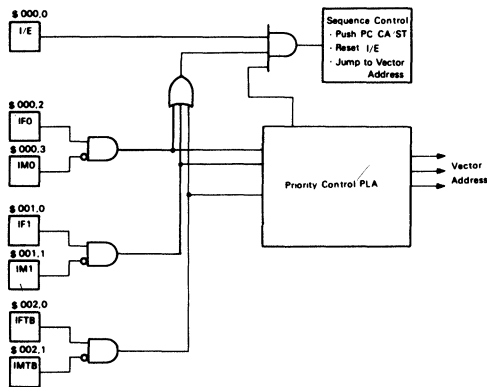


Fig. 6 Interrupt Circuit Block Diagram

Table 1. Vector Addresses and Interrupt Priority

Reset · Interrupt	Priority	Vector addresses
RESET	—	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
TIMER-B	3	\$0008

Table 2. Conditions of Interrupt Service

Interrupt control bits	Interrupt source		
	\overline{INT}_0	\overline{INT}_1	TIMER-B
I/E	1	1	1
IFO · IMO	1	0	0
IF1 · IM1	*	1	0
IFTB · IMTB	*	*	1

* Don't care

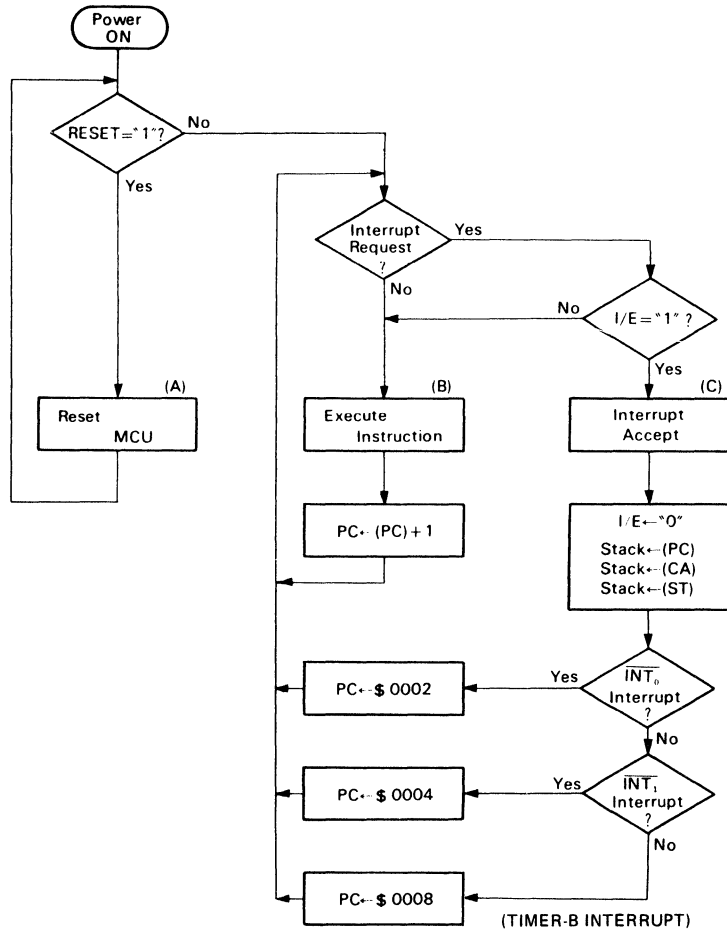


Fig. 7 Interrupt Servicing Flowchart

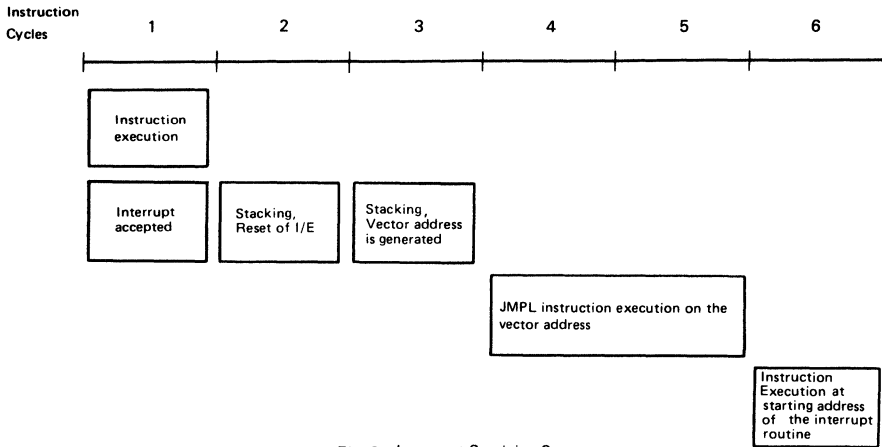


Fig. 8 Interrupt Servicing Sequence

• **Interrupt Enable Flag (I/E: \$000,0)**

The Interrupt Enable Flag controls enable/disable of all interrupt requests as shown in Table 3. The Interrupt Enable Flag is reset by the interrupt servicing and set by RTNI instruction.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

• **External Interrupt (\overline{INT}_0 , \overline{INT}_1)**

To use external interrupt, select R_{32}/\overline{INT}_0 , R_{33}/\overline{INT}_1 port for \overline{INT}_0 , \overline{INT}_1 mode by setting the Port Mode Register (PMR: \$004).

The External Interrupt Request Flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 , \overline{INT}_1 inputs.

\overline{INT}_1 input can be used as a clock signal input of TIMER-B. Then, TIMER-B counts up at each falling edge of input. When using \overline{INT}_1 as TIMER-B external event, an External Interrupt Mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted.

• **External Interrupt Request Flag (IF0: \$000,2, IF1: \$001,0)**

The External Interrupt Request Flags (IF0, IF1) are set at the falling edges of \overline{INT}_0 , \overline{INT}_1 inputs respectively.

• **External Interrupt Mask (IM0: \$000,3, IM1: \$001,1)**

The External Interrupt Mask is used to mask the external interrupt requests.

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

• **Port Mode Register (PMR: \$004)**

The Port Mode Register is a 2-bit write-only register which controls the R_{32}/\overline{INT}_0 pin and R_{33}/\overline{INT}_1 pin as shown in Table 6. The Port Mode Register will be initialized to \$0 by MCU reset, so that all these pins are set to a port mode.

Table 6. Port Mode Register

PMR bit 3	R_{33}/\overline{INT}_1 pin
0	Used as R_{33} port input/output pin
1	Used as \overline{INT}_1 input pin

PMR bit 2	R_{32}/\overline{INT}_0 pin
0	Used as R_{32} port input/output pin
1	Used as \overline{INT}_0 input pin

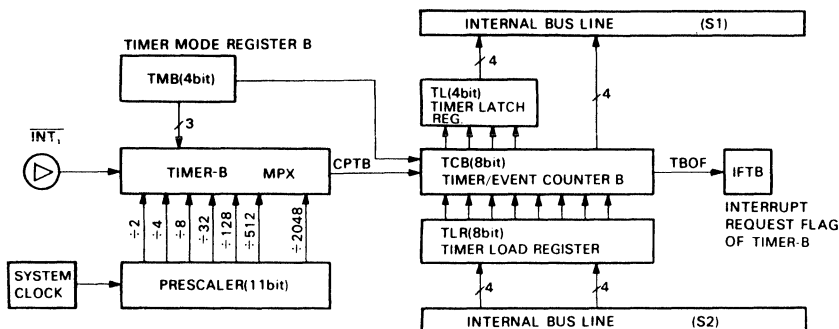


Fig. 9 Timer/Counter Block Diagram

■ **TIMER**

The MCU contains a prescaler and timer/counter (TIMER-B). Fig. 9 shows the block diagram. The prescaler is an 11-bit binary counter which has same function with the HMCS412C. TIMER-B is an 8-bit auto-reload timer/counter which has same function with the HMCS412C.

● **Prescaler**

The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and the prescaler starts to count up the system clock signal as soon as RESET input goes to logic "0". The prescaler keeps counting up except MCU reset and stop mode. The prescaler provides clock signals to TIMER-B. The prescaler divide ratio of the clock signals are selected according to the content of the mode registers such as - Timer Mode Register B (TMB).

● **TIMER-B Operation**

Timer Mode Register B (TMB: \$009) is used to select the auto-reload function and the prescaler divide ratio of TIMER-B as the input clock source. When the external event input is used as an input clock signal to TIMER-B, select the R_{33}/\overline{INT}_1 as \overline{INT}_1 and set the External Interrupt Mask (IM1) to "1" to

prevent the external interrupt request from occurring.

TIMER-B is initialized according to the value written into the Timer Load Register by software. TIMER-B counts up at every clock input signal. When the next clock signal is applied to TIMER-B after TIMER-B is set to \$FF, TIMER-B will be initialized again and generate overflow output. In this case if the auto-reload function is selected, TIMER-B is initialized according to the value of the Timer Load Register. Else if the auto-reload function is not selected, TIMER-B goes to \$00. TIMER-B Interrupt Request Flag (IFTB: \$002.0) will be set at this overflow output.

● **Timer Mode Register B (TMB: \$009)**

The Timer Mode Register B is a 4-bit write-only register. The Timer Mode Register B controls the selection for the auto-reload function of TIMER-B and the prescaler divide ratio, and the source of the clock input signal, as shown in Table 7.

The Timer Mode Register B is initialized to \$00 by MCU reset.

The operation mode of TIMER-B is changed at the second instruction cycle after writing into the Timer Mode Register B.

Therefore, it is necessary to program the write instruction to TLRU after the content of TMB is changed.

Table 7 Timer Mode Register B

TMB		Auto-reload Function
Bit 3		
0		No
1		Yes

TMB			Prescaler Divide Ratio, Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

- **TIMER-B (TCBL: \$00A, TCBU: \$00B)
(TLRL: \$00A, TLRU: \$00B)**

TIMER-B consists of an 8-bit write-only Timer Load Register, and an 8-bit read-only Timer/Event Counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

The Timer/Event Counter can be initialized by writing data into the Timer Load Register. In this case, write the low-order digit first, and then the high-order digit. The Timer/Event Counter is initialized at the time when the high-order digit is written. The Timer Load Register will be initialized to \$00 by the MCU reset.

The counter value of TIMER-B can be obtained by reading the Timer/Event Counter. In this case, read the high-order digit first, and then the low-order digit. The count value of low-order digit is latched at the time when the high-order digit is read.

- **TIMER-B Interrupt Request Flag (IFTB: \$002, 0)**

The TIMER-B Interrupt Request Flag is set by the overflow output of TIMER-B.

- **TIMER-B Interrupt Mask (IMTB: \$002, 1)**

TIMER-B Interrupt Mask prevents an interrupt request generated by TIMER-B Interrupt Request Flag.

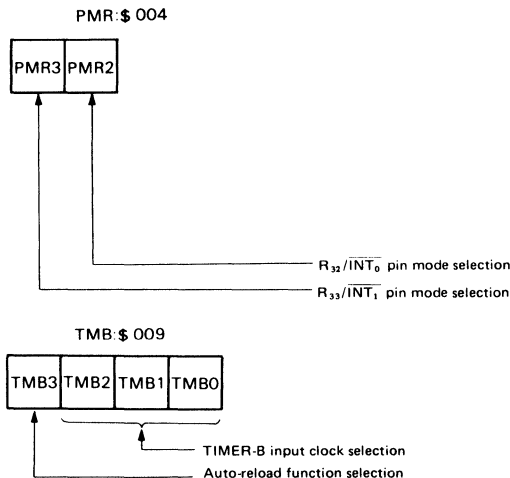


Fig. 10 Mode Register Configuration and Function

Table 8. TIMER-B Interrupt Request Flag

TIMER-B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. TIMER-B Interrupt Mask

TIMER-B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Data Input from Input/Output Common Pins

I/O circuit type	Available pin condition for input
For Standard pins "Without pull-up MOS (NMOS open drain)"	"1"
For High voltage pins "Without pull-down MOS (PMOS open drain)"	"0"

Table 11. I/O Pin Circuit Forms

	Without pull-up MOS (NMOS open drain)	Applied pins
Standard pins		D ₀ ~ D ₃ , R ₃₀ ~ R ₃₃ , R ₄₀ ~ R ₄₃
I/O common pins		D ₄ ~ D ₁₄ , R ₁₀ ~ R ₁₃ , R ₂₀ ~ R ₂₃
High voltage pins		R ₀₀ ~ R ₀₃
Input pins		$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$

(Continued)

■ INPUT/OUTPUT

The MCU provides 36 Input/Output pins, and they are consist of 12 standard pins of "Without pull-up MOS (NMOS open drain)" and 24 high voltage pins of "Without pull-down MOS (PMOS open drain)".

When any input/output common pin is used as input pin, it is necessary to set the output data as shown in Table 10.

	Without pull-down MOS (PMOS open drain)	Applied pins
I/O common pins		D ₄ ~ D ₁₄ , R ₁₀ ~ R ₁₃ , R ₂₀ ~ R ₂₃
High voltage pins		R ₀₀ ~ R ₀₃
	Input pins	
Input pins		R _{A1}

(Note) In the stop mode, HLT signal is "0", HLT signal is "1" and I/O pins are in high impedance.

● D-port

D-port is 1-bit I/O port, and it has 15 Input/Output common pins. It can be set/reset by the SED/RED and SEDD/REDD

instructions, and can be tested by the TD and TDD instructions. Table 11 shows the classification of standard pins, high voltage pins and the Input/Output pins circuit types.

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● **R-port**

R-port is 4-bit I/O port. It provides 16 input/output common pins, 4 output-only pins, and 1 input-only pin. Data input is processed using the LAR and LBR instructions and data output is processed using the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, invalid data will be read by reading from the output-only and/or non-existing ports.

The R₃₂ and R₃₃ pins are also used as the \overline{INT}_0 and \overline{INT}_1 pins respectively. Table 11 shows the classification of standard

pins, high voltage pins and Input/Output pins circuit types.

■ **RESET**

The MCU is reset by setting RESET pin to "1". At power ON or recovering from stop mode, apply RESET input more than t_{RC} to obtain the necessary time for oscillator stabilization. In other cases, the MCU reset requires at least two instructions cycle time of RESET input.

Table 12 shows initialized items by MCU reset and each status after reset.

Table 12 MCU Initial Value by Reset

Items		Initial value by MCU reset	Contents
Program counter (PC)		\$0000	Execute program from the top of ROM address.
Status (ST)		"1"	Enable to branch with conditional branch instructions.
Stack pointer (SP)		\$3FF	Stack level is 0.
I/O output register	Standard pin Without pull-up MOS	"1"	Enable to input.
	High voltage pin Without pull-down MOS	"0"	Enable to input.
Interrupt flag	Interrupt Enable Flag (I/E)	"0"	Inhibit all interrupts.
	Interrupt Request Flag (IF)	"0"	No interrupt request.
	Interrupt Mask (IM)	"1"	Mask interrupt request.
Mode register	Port Mode Register (PMR)	"0000"	See Item "Port Mode Register".
	Timer Mode Register B (TMB)	"0000"	See Item "Timer Mode Register B".
Timer/Counter	Prescaler	\$000	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—

(Note) The values of registers and flags which are not described on above table will become as follows.

Item	After releasing stop mode by MCU Reset	After MCU Reset except the left
Carry (CA)	The value immediately before MCU reset is not guaranteed. Initialization by the program should be required.	The value immediately before MCU Reset is not guaranteed. Initialization by the program should be required.
Accumulator (A)		
B register (B)		
W register (W)		
X/SPX register (X/SPX) Y/SPY register (Y/SPY)		
RAM	The value immediately before MCU reset (the value immediately before executing stop instruction) is retained.	— ditto —



■ INTERNAL OSCILLATOR CIRCUIT

Fig. 11 gives internal oscillator circuit. The oscillator type can be selected from the followings; crystal resonator, or ceramic

filter resonator as shown in Table 13, In any cases, external clock operation is available.

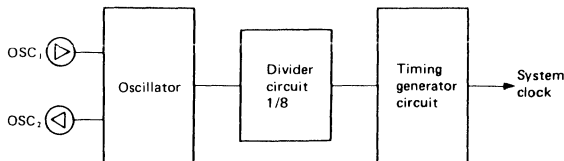


Fig. 11 Internal Oscillator Circuit

Table 13 Oscillator Circuit Example

	Circuit configuration	Remarks
External clock operation		
Ceramic filter resonator		<p>Ceramic filter: CSA 4.00MG (Murata) R_f: $1M\Omega \pm 2\%$ C_1: $30pF \pm 20\%$ C_2: $30pF \pm 20\%$</p> <p>Ceramic filter: CSA 6.00MG (Murata) R_f: $1M\Omega \pm 2\%$ C_1: $30pF \pm 20\%$ C_2: $30pF \pm 20\%$</p>
Crystal resonator	<p>ATcut parallel resonance crystal</p>	<p>Crystal: 4.194304 (MHz) NC-18C (Nihon Denpa Kogyo) R_f: $1M\Omega \pm 2\%$ C_1: $22pF \pm 20\%$ C_2: $22pF \pm 20\%$</p> <p>Crystal: 6.0 (MHz) R_f: $1M\Omega \pm 2\%$ C_1: $20pF \pm 20\%$ C_2: $20pF \pm 20\%$</p> <p>Crystal: A T cut parallel resonance crystal C_0: 7 pF max. R_s: 100Ω max. f: 2.0 ~ 4.5MHz</p>

(Note 1) On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.

(Note 2) Wiring among OSC₁, OSC₂ and elements should be as short as possible, and never cross the other wirings. Refer to the layout of crystal and ceramic filter.

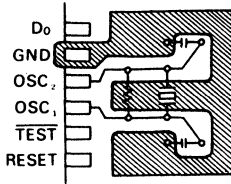


Fig. 12 Layout of Crystal and Ceramic Filter

■ **LOW POWER DISSIPATION MODE**

The MCU provides two low power dissipation modes, that is, a Standby mode and a Stop mode. Table 14 shows the function of the low power dissipation mode, and Fig. 13 shows the diagram of the mode transition.

Table 14 Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							Recovering method
		Oscillator circuit	Instruction execution	Register, Flag	Interrupt function	RAM	Input/Output pin	Timer/Counter	
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ^{*2)}	Active	RESET Input, Interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ^{*1)}	Stop	Retained	High impedance	Stop	RESET Input

*1) As the MCU recovers from STOP mode by RESET input, the contents of the flags and registers are initialized according to Table 12.

*2) As a I/O circuit is active, a I/O current possibly flows according the state of I/O pin. This is the additional current to the current dissipation in Standby Mode (ISBY1, ISBY2).

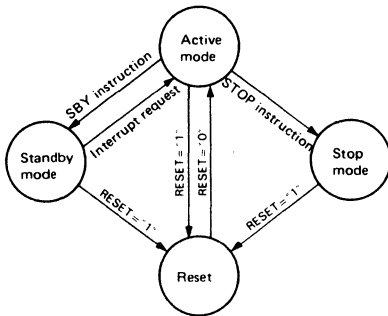


Fig. 13 MCU Operation Mode Transition

● **Standby Mode**

The SBY instruction puts the MCU into the Standby mode. In the Standby mode, the oscillator circuit is active and timer/

counter continues working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and Input/Output pins retain the state they had just before going into the Standby mode.

The Standby mode is canceled by the MCU reset or interrupt request. When canceled by the interrupt request, the MCU becomes an active mode and executes the instruction next to the SBY instruction. At this time, if the Interrupt Enable Flag is "1", the interrupt is executed. If the Interrupt Enable Flag is "0", the interrupt request is held on and the normal instruction execution continues.

Fig. 14 shows the flowchart of the Standby Mode.

● **Stop Mode**

The STOP instruction brings the MCU into the Stop mode. In this mode the oscillator circuit and every function of the MCU stop.

The Stop mode is canceled by the MCU reset. At this time, as shown in Fig. 15, apply the RESET input for more than t_{RC} to get enough oscillator stabilization time. (Refer to the "AC CHARACTERISTICS".) After the Stop mode is canceled, RAM retains the state it had just before going into the Stop mode after releasing stop mode by MCU reset, the values of the B register, W register, X/SPX register, Y/SPY register, carry and serial data register are not guaranteed.

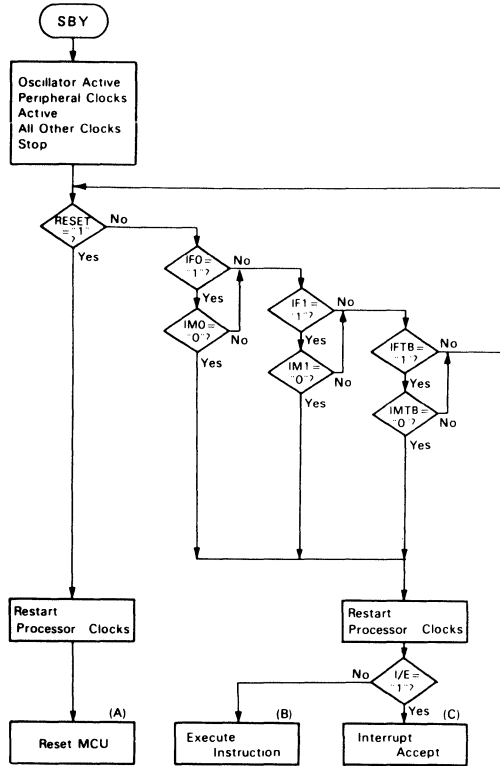


Fig. 14 MCU Operating Flowchart

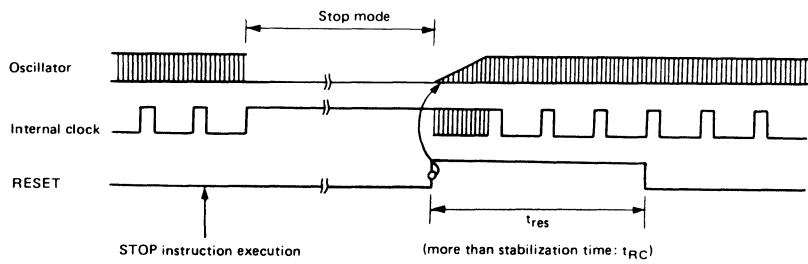


Fig. 15 Stop Mode Cancel Timing Chart

RAM ADDRESSING MODE

As shown in Fig. 16, the MCU provides three RAM addressing modes; Register Indirect Addressing, Direct Addressing and Memory Register Addressing.

Register Indirect Addressing

The combined 10-bit contents of W Register, X Register and Y Register is used as the RAM address in this mode.

Direct Addressing

The direct addressing instruction consists of two words and the second word (10 bits) following Op-code (the first word) is used as the RAM address.

Memory Register Addressing

The Memory Register Addressing can access 16 digits (Memory Register: MR) from \$020 to \$02F by using the LAMR and XMRA instruction.

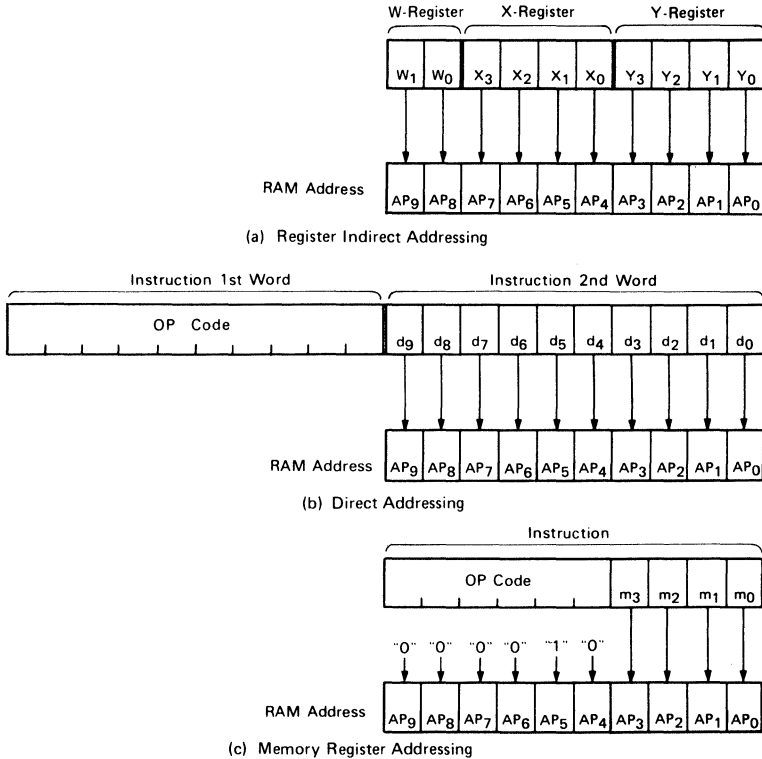


Fig. 16 RAM Addressing Mode

■ **ROM ADDRESSING MODE AND P INSTRUCTION**

The MCU has four kinds of ROM addressing modes as shown in Fig. 17.

● **Direct Addressing Mode**

The program can branch to any addresses in the ROM memory space by using JMPL, BRL or CALL instruction. These instructions replace 14-bit program counter (PC13 to PC0) with 14-bit immediate data.

● **Current Page Addressing Mode**

ROM memory space is divided into 256 words in each page starting from \$0000. The program branches to the address in the same page using BR instruction. This instruction replace the low-order eight bits of program counter (PC7 to PC0) with

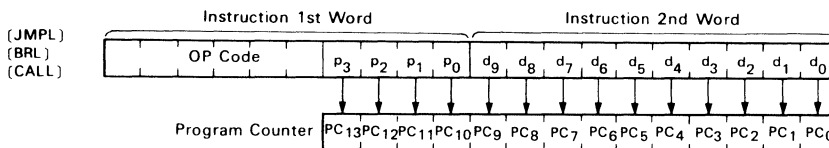
8-bit immediate data. The branch destination by BR instruction on the boundary between pages is given in Fig. 19.

● **Zero Page Addressing Mode**

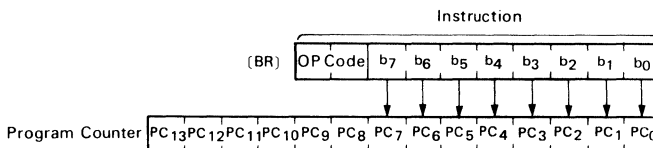
The program branches to the zero page subroutine area, which is located on the address from \$0000 to \$003F, using CAL instruction. When CAL instruction is executed, 6-bit immediate data is placed in low-order six bits of program counter (PC5 to PC0) and "0's" are placed in high-order eight bits (PC13 to PC6).

● **Table Data Addressing**

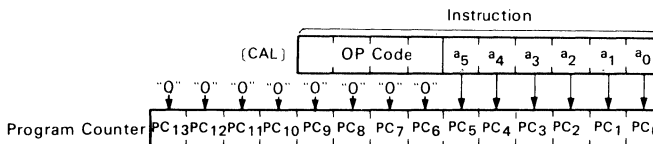
The program branches to the address determined by the contents of the 4-bit immediate data, accumulator and B register, using TBR instruction.



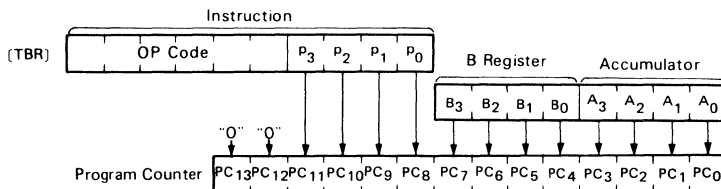
(a) Direct Addressing



(b) Current Page Addressing



(c) Zero Page Addressing



(d) Table Data Addressing

Fig. 17 ROM Addressing Mode



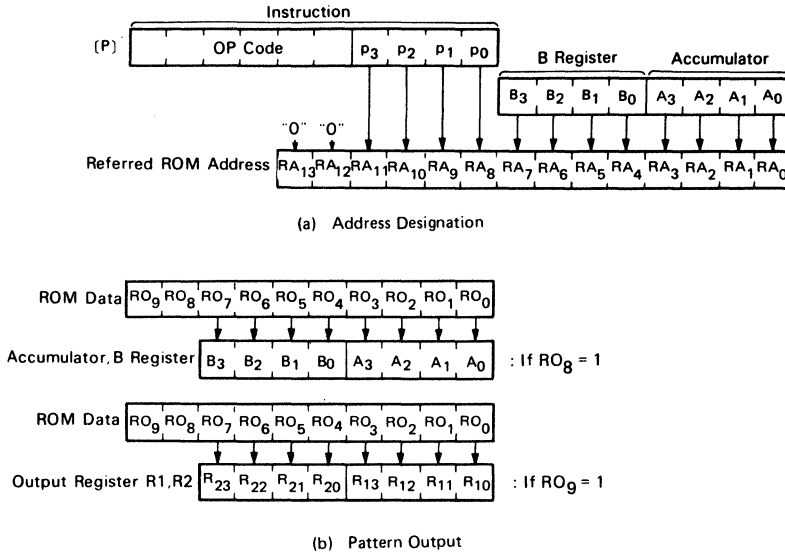


Fig. 18 P Instruction

● **P Instruction**

The P instruction refers ROM data addressed by Table Data Addressing. ROM data addressed also determine its destination. When bit 8 in referred ROM data is "1", 8 bits of referred ROM

data are written into the accumulator and B Register. When bit 9 is "1", 8 bits of referred ROM data are written into the R1 and R2 port output register. When both bit 8 and 9 are "1", ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at a same time.

The P instruction has no effect on the program counter.

● **Description of the Branch Destination on Page Boundary.**

When BR is on page boundary (256n+255), BR instruction transfers the contents of PC to the next page with hardware architecture. Therefore, the program branches to the next page when using BR on page boundary. The HMCS400 series cross macro assembler has automatic paging facility for ROM page.

■ **INSTRUCTION SET**

The HD614P180 provides 98 instructions. These instructions are classified into 10 groups as follows;

- (1) Immediate Instruction
- (2) Register-to-Register Instruction
- (3) RAM Address Instruction
- (4) RAM Register Instruction
- (5) Arithmetic Instruction
- (6) Compare Instruction
- (7) RAM Bit Manipulation Instruction
- (8) ROM Address Instruction
- (9) Input/Output Instruction
- (10) Control Instruction

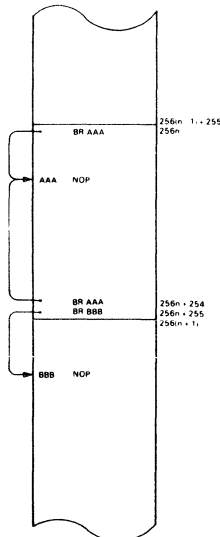


Fig. 19 The Branch Destination by BR Instruction on the Boundary between Pages

Table 15. Immediate Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1 / 1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1 / 1
Load Memory from Immediate	LMID i, d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i → M		2 / 2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y + 1 → Y	NZ	1 / 1

Table 16. Register-to-Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1 / 1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1 / 1
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1 / 1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1 / 1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1 / 1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1 / 1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1 / 1

Table 17. RAM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1 / 1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1 / 1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1 / 1
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1 / 1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1 / 1
Increment Y	IY	0 0 0 1 0 1 1 1 1 0	Y + 1 → Y	NZ	1 / 1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y - 1 → Y	NB	1 / 1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y + A → Y	OVF	1 / 1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y - A → Y	NB	1 / 1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1 / 1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1 / 1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1 / 1

Table 18. RAM Register Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX) (Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M→A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX) (Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX) (Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A→M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y(X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y(X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX) (Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M↔A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX) (Y→SPY)		1/1

Note) (XY) and (x) have the meaning as follows:

(1) The instructions with (XY) have 4 mnemonics and 4 object codes for each. (example of LAM (XY) is given below.)

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

(2) The instructions with (x) have 2 mnemonics and 2 object codes for each. (example of LMAIY (X) is given below.)

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 19. Arithmetic Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A + i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B - 1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	\bar{A} + 1 → A		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	B → B		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A OVF + CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A + CA → A OVF + CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M - A - CA → A NB + CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M - A - CA → A NB + CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 1 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2



Table 20. Compare Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 21. RAM Bit Manipulation Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1→M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	1→M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0→M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	0→M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 22. ROM Address Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Branch on Status 1	BR - b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1→I/E CA RESTORE	ST	1/3

Table 23. Input/Output Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1→D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1→D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0→D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0→D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m)→A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m)→B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A→R(m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B→R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2



Table 24. Control Instruction

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1 / 1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1 / 1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1 / 1

(Note) HD614P180 has not serial Interface, so STS (start serial) cannot be used. If used STS, its operation equals to NOP.

Table 25. OP-Code Map

R9	0										1																				
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E
0	NOP	XSPX	XSPY	XSPXY	AN	EM		AM																							
1	RTN	RTN			ALEM			AMC																							
2																															
3																															
4		LBM(XY)		BNEM				LAB			IB																		SBY	STOP	
5		LMAY(X)			AYY			LSPY			IY																				
6		NEGA			RED			LSPX																							
7																															
8		XMA(XY)			SEM	n(2)		REM	n(2)		TM	n(2)																			
9		LAM(XY)						SMC			ANM																				
A		ROT	ROT					DAA			DAS																				
B																															
C		XMB(XY)			BEM			LBA																							
D		LMADY(X)																													
E		TD						SED			LXA																				
F																															
1																															
0																															
1																															
2																															
3																															
4																															
5																															
6																															
7																															
8																															
9																															
A																															
B																															
C																															
D																															
E																															
F																															

... 1 word/2 cycle Instruction
 ... 1 word/3 cycle Instruction
 ... RAM Direct Address Instruction (2 word/2 cycle)
 ... 2 word/2 cycle Instruction

HD614P180

■ PRECAUTION TO USE THE EPROM ON-PACKAGE 4 BIT SINGLE CHIP MICROCOMPUTER

Please pay attention to the followings, since this MCU has special structure with pin socket on the package.

- (1) Don't apply high static voltage or surge voltage over MAXIMUM RATINGS to the socket pins as well as the LSI pins.
If not, that may cause permanent damage to the device.
- (2) When using this in production like mask ROM type single chip microcomputer, pay attention to the followings to keep the good contact between the EPROM pins and socket pins.
 - (a) When soldering the LSI on a print circuit board, the recommended condition is

Temperature: lower than 250°C

Time : within 10 sec.

Over time/temperature may cause the bonding solder of socket pin to melt and the socket pin may drop.

- (b) Note that the detergent or coating will not get in the socket during flux washing or board coating after soldering, because that may cause bad effect on socket contact.
- (c) Avoid permanent application of this under the condition of vibratory place and system.
- (d) The socket, inserted and pulled repeatedly loses its contactability. It is recommended to use new one when applied in production.

Table 26. Difference between the HD614P180 and HMCS412C

Type name		HD614P180	HMCS412AC	HMCS412C	HMCS412CL	HMCS414AC	HMCS414C	HMCS414CL
Item								
Minimum instruction execution time		1.33 μs	1.33 μs	2 μs	4 μs	1.33 μs	2 μs	4 μs
Power supply voltage		4.5 ~ 5.5 V	4.5 ~ 6 V	3.5 ~ 6 V	2.5 ~ 6 V	4.5 ~ 6 V	3.5 ~ 6 V	2.5 ~ 6 V
ROM		<ul style="list-style-type: none"> ○ 4,096 words x 10 bits (using standard EPROM 2764) ○ 8,192 words x 10 bits (using standard EPROM 27128) 	2,048 words x 10 bits Mask ROM			4,096 words x 10 bits Mask ROM		
RAM		576 digits x 4 bits	160 digits x 4 bits			256 digits x 4 bits		
I/O pin circuit	Standard pins	All pins are "without pull-up MOS (NMOS open drain)".	Each pin selects "without pull-up MOS (NMOS open drain)", "with pull-up MOS", or "CMOS".					
	High voltage pins	All pins are "without pull-down MOS (PMOS open drain)".	Each pin selects "without pull-down MOS (PMOS open drain)" or "with pull-down MOS".					
Clock generator		Crystal resonator or ceramic filter resonator	Crystal resonator, ceramic filter resonator, or resistance oscillator					
Package		42-pin EPROM on package. The base chip pins are compatible with those of the HMCS412C	42-pin dual in line package (DP-42) Shrink type 42-pin dual in line package (DP-42S) 44-pin flat plastic package (FP-44A)					
Type		DC-42P	DP-42		DP-42S		FP-44A	
Occupied area (mm)		19 x 52.8	13.4 x 52.8		14 x 37.4		17.2 x 17.2	
High from stand-off		7.5 (max.) EPROM on package	5.08 (max.)		5.08 (max.)		2.9 (max.)	

HD40P4281/HD40P42161

—Under Development—

Description

The HD40P4281/HD40P42161 are 4-bit single chip microcomputers which can mount a standard EPROM 2764/27128 for program memory.

The HD40P4281 is pin-compatible with the mask ROM type HMCS424, but has some differences with it as shown in Table 33. By modifying the program in the EPROM, it can be used for the evaluation of the HMCS424 or for small-scale production.

Features

- 4-bit architecture
- Application to 4096, 8192 words of 10 bits EPROM
 - 4096 words.....HN482764, HN27C64
 - 8192 words.....HN4827128
- 992 digits of 4-bit RAM
- 36 I/O pins, including 24 high-voltage I/O pins (40 V max)
- 2 Timer/counter
 - 11-bit prescaler
 - 8-bit free running timer/counter
 - 8-bit auto-reload timer/event counter
- Clock synchronous 8-bit serial interface
- Five interrupt sources
 - External: 2
 - Timer/counter: 2
 - Serial interface: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time
 - 0.89 μ s
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate.
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data.
- On-chip oscillator
 - Crystal or ceramic filter (externally drivable)
- Package
 - 42-pin dual in-line ceramic, EPROM on-package
- Instruction set compatible with HMCS424; 101 instructions
- High programming efficiency with 10-bit/word ROM: 79 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels includ-

ing interrupts

- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

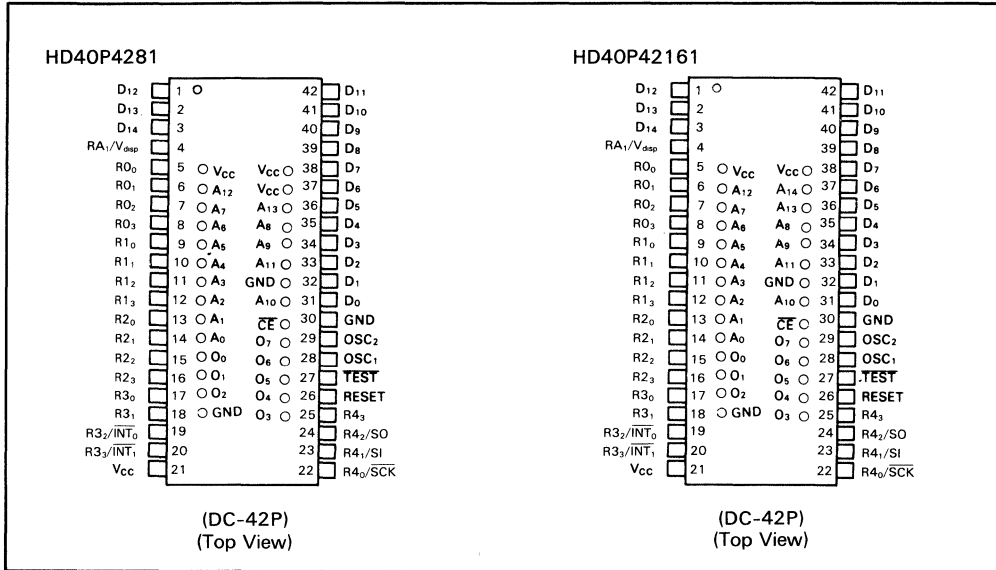
Recommended Applicable EPROM

Type No.	Program Memory		EPROM Type No.
	Capacity	f _{osc} (MHz)	
HD40P4281	4096 words	4	HN27C64-30 HN482764-3
		8	HN27C64G-15
	8192 words	4	HN4827128-45
		8	HN4827128A-17
HD40P42161	16384 words	4	HN27256-30
		8	HN27256-25

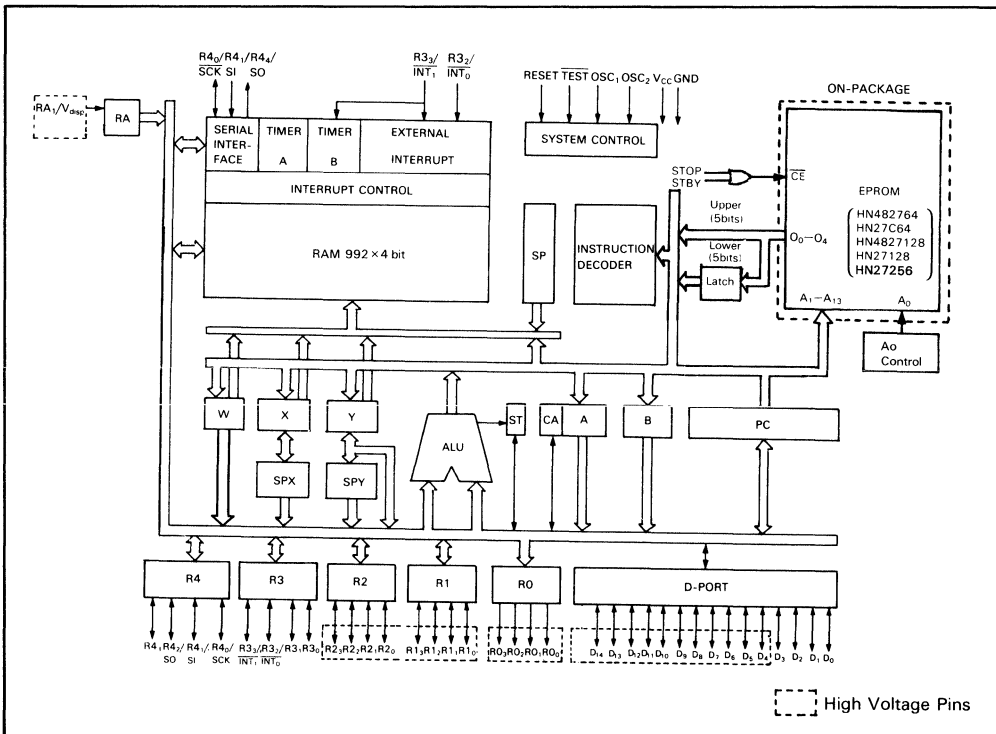


HD40P4281/HD40P42161

Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high-voltage I/O pins with maximum voltage of 40 V (V_{CC}–40 V). For details, see Input/Output section.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀-D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 16 pins are all input/output pins. D₀ to D₃ are standard and D₄ to D₁₄ are

high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀-R₀₃, R₁₀-R₁₃, R₂₀-R₂₃, R₃₀-R₃₃, R₄₀-R₄₃, RA₁ (R Ports)

R₀ to R₄ are 4-bit I/O ports. RA is a 1-bit port. R₀ is an output port, RA an input port, and R₁ to R₄ I/O ports. R₀, R₁, R₂, and RA are high-voltage ports, and R₃ and R₄ are standard ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, R₃₃, R₄₀, R₄₁ and R₄₂ are multiplexed with INT₀, INT₁, SCK, SI and SO respectively. For details, see Input/ Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI) and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R₄₀, R₄₁ and R₄₂ respectively. For details, see Serial interface.

Functional Description

ROM Memory Map

ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area

\$0000 to \$1FFF : HD40P4281
\$0000 to \$3FFF : HD40P42161

RAM Memory Map

The MCU includes 992 digits of 4-bits RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

HD40P4281/HD40P42161

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into

three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

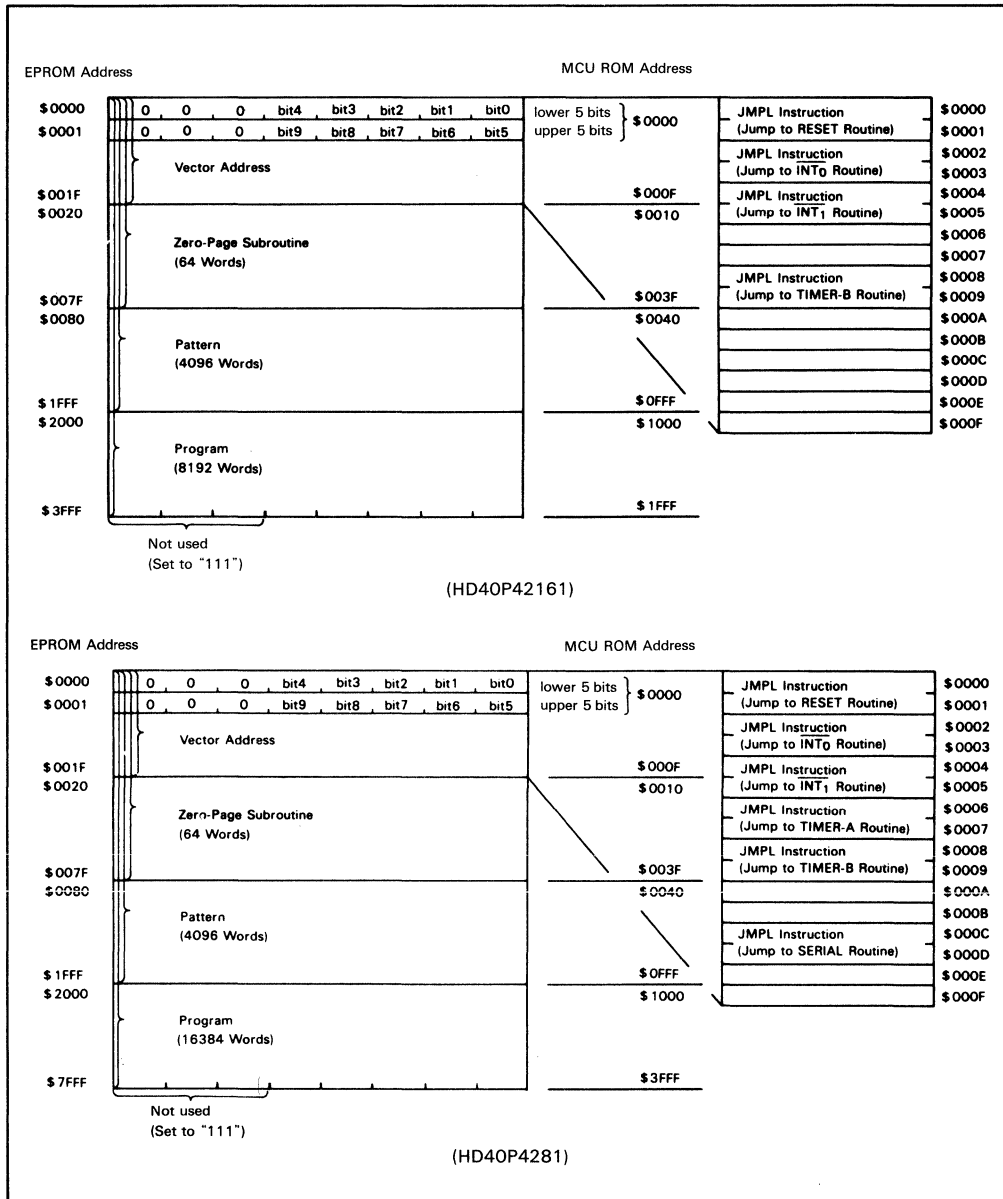


Figure 1. ROM Memory Map



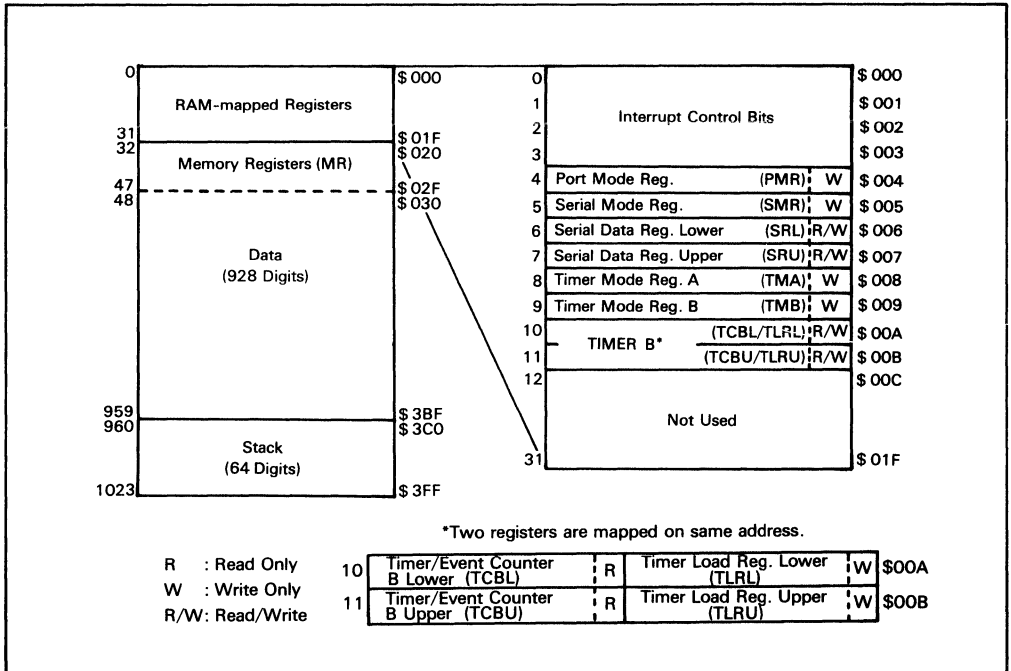


Figure 2. RAM Memory Map

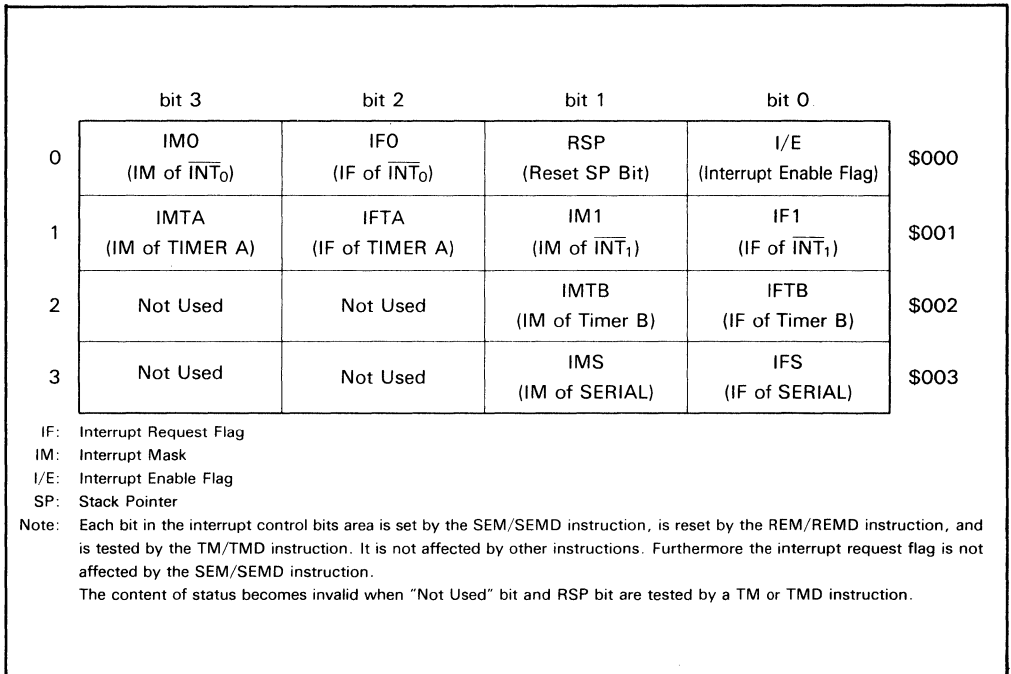


Figure 3. Configuration of Interrupt Control Bit Area



Data Area (\$020 to \$3BF): 16 digits of \$020 through \$02F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X

and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing. The W register is a write-only register.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

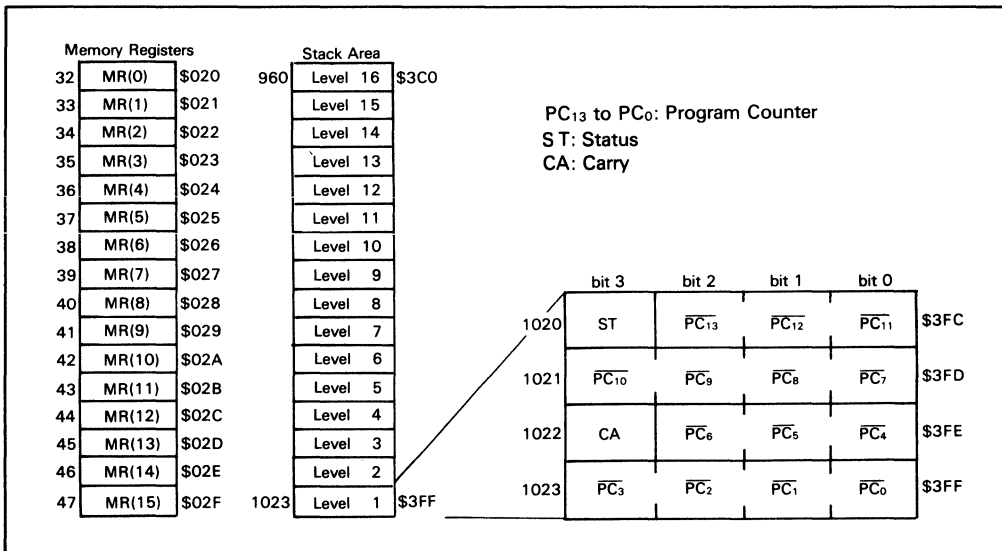


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

Interrupt

Five interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timer A, timer B), and serial interface

(serial). For each source, an interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and

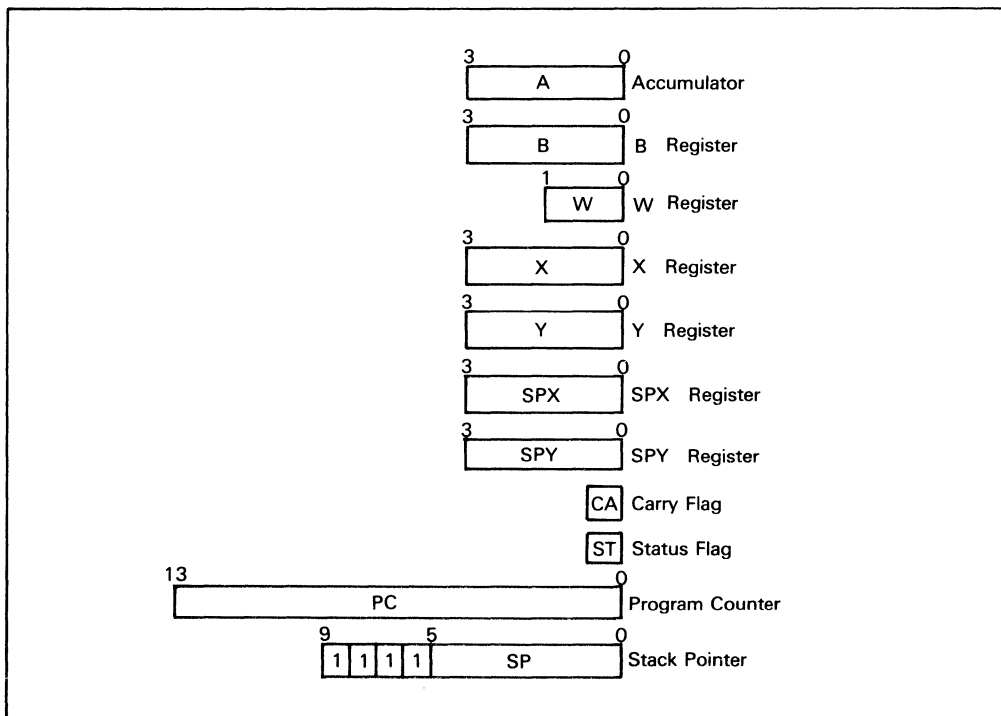


Figure 5. Registers and Flags



Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	—	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
SERIAL	5	\$000C

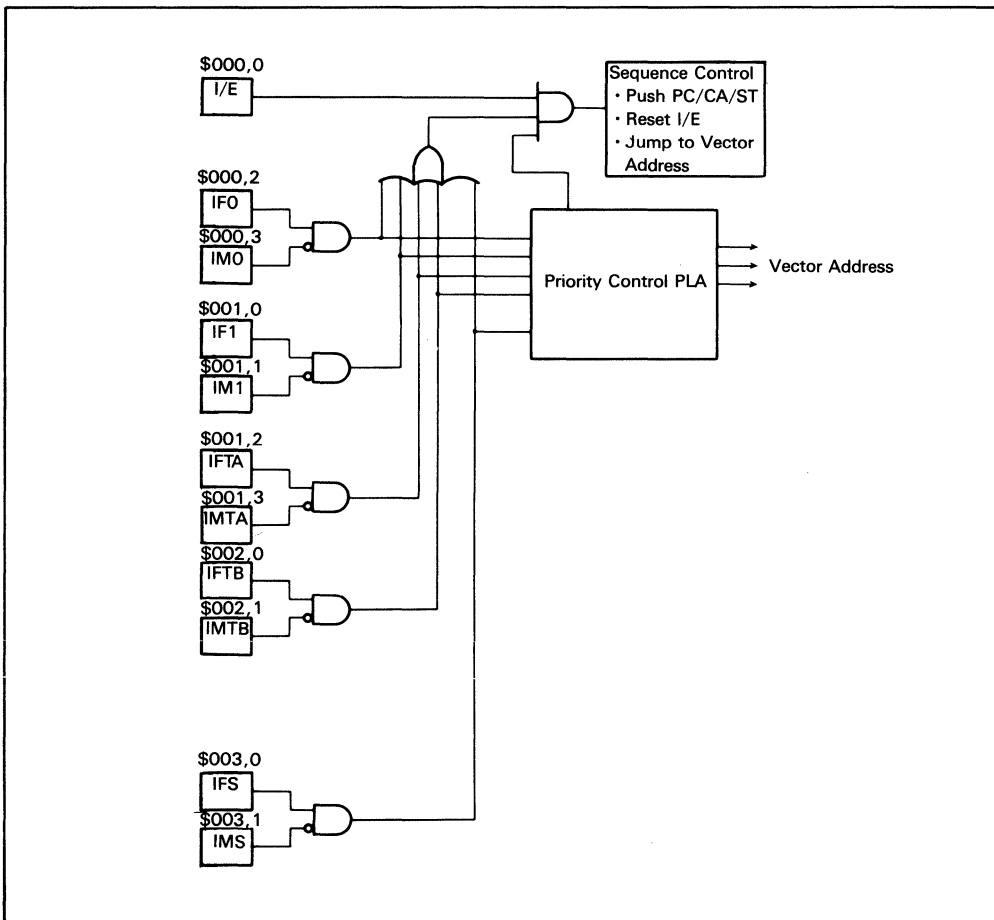


Figure 6. Interrupt Control Circuit Block Diagram

vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1)

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer A	Timer B	Serial
I/E	1	1	1	1	1
I/O · \overline{IMO}	1	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0
I/TA · \overline{IMTA}	*	*	1	0	0
I/TB · \overline{IMTB}	*	*	*	1	0
I/S · \overline{IMS}	*	*	*	*	1

* Don't care

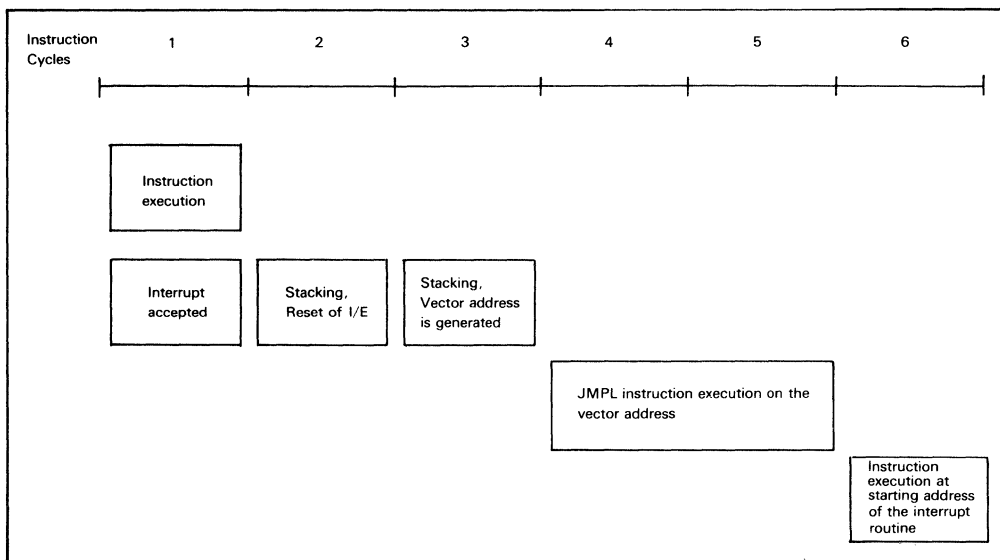


Figure 7. Interrupt Servicing Sequence

can be selected by the port mode register (PMR: \$004). Setting bit 3 and bit 2 of PMR causes R3₃/ $\overline{\text{INT}}_1$ pin and R3₂/ $\overline{\text{INT}}_0$ pin to be used as $\overline{\text{INT}}_1$ pin and $\overline{\text{INT}}_0$ pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ inputs. (Refer to table 4.)

The $\overline{\text{INT}}_1$ input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the $\overline{\text{INT}}_1$ input. When using $\overline{\text{INT}}_1$ as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by $\overline{\text{INT}}_1$ will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the $\overline{\text{INT}}_0$, and $\overline{\text{INT}}_1$ inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the R3₂/ $\overline{\text{INT}}_0$ pin, R3₃/ $\overline{\text{INT}}_1$ pin, R4₁/SI pin, and R4₂/SO pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	R3 ₃ / $\overline{\text{INT}}_1$ Pin
0	Used as R3 ₃ port input/output pin
1	Used as $\overline{\text{INT}}_1$ input pin

PMR2	R3 ₂ / $\overline{\text{INT}}_0$ Pin
0	Used as R3 ₂ port input/output pin
1	Used as $\overline{\text{INT}}_0$ input pin

PMR1	R4 ₁ /SI Pin
0	Used as R4 ₁ port input/output pin
1	Used as SI input pin

PMR0	R4 ₂ /SO Pin
0	Used as R4 ₂ port input/output pin
1	Used as SO output pin

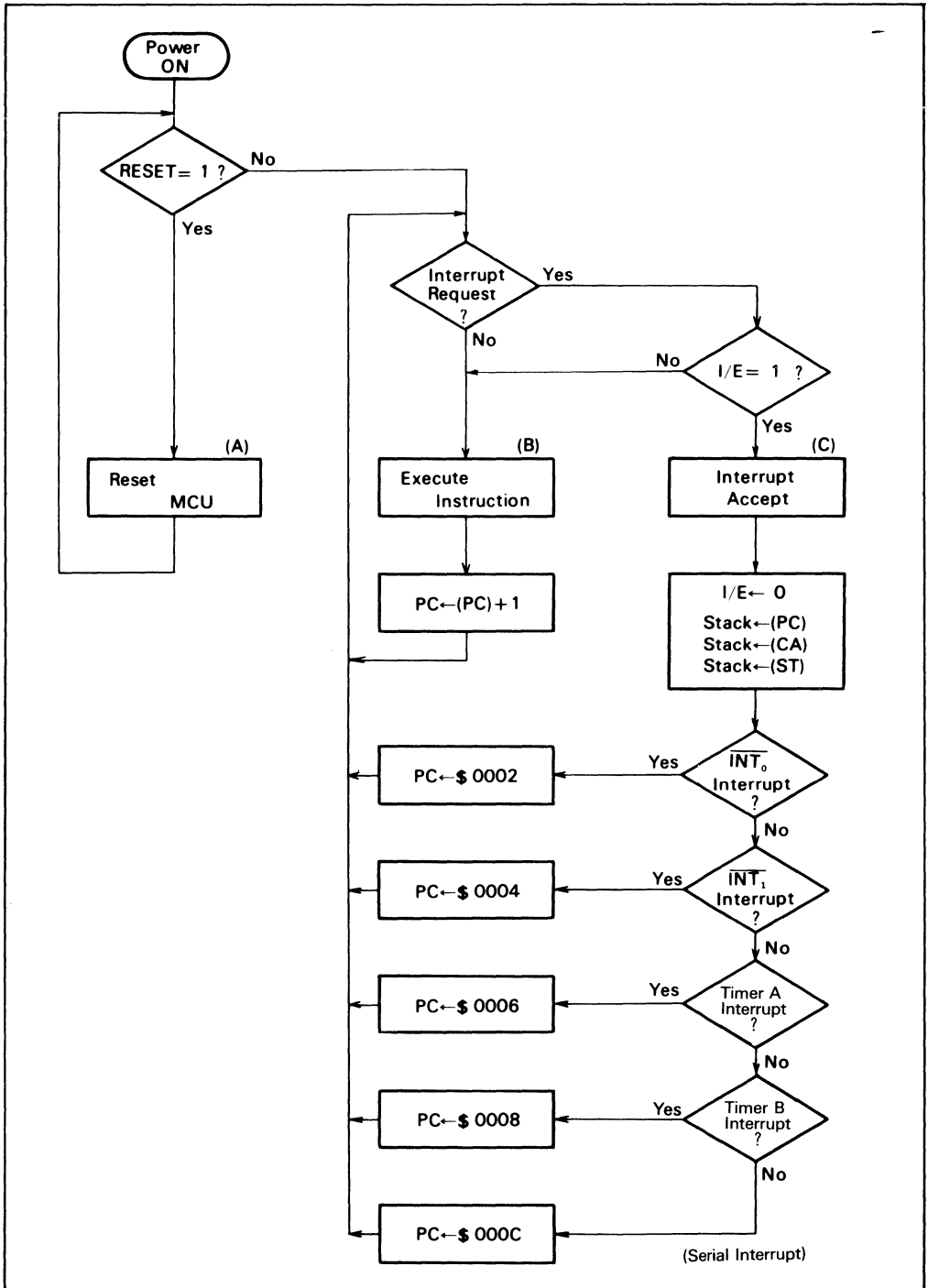


Figure 8. Interrupt Servicing Flowchart



Serial Interface

The serial interface is used to transmit/receive 8-bit data serially. This consists of the serial data register, the serial mode register, the octal counter and the multiplexer as illustrated in figure 9. Pin R4₀/SCK and the transfer clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

STS instruction is used to initiate serial interface operations and to reset the octal counter to \$0. The counter starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of the SCK. When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the R4₀/SCK, prescaler divide ratio, and

transfer clock source as shown in table 7.

The write signal to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it will be necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SDR: \$006, SRU: \$007): The 8-bit read/write serial data register consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register will be

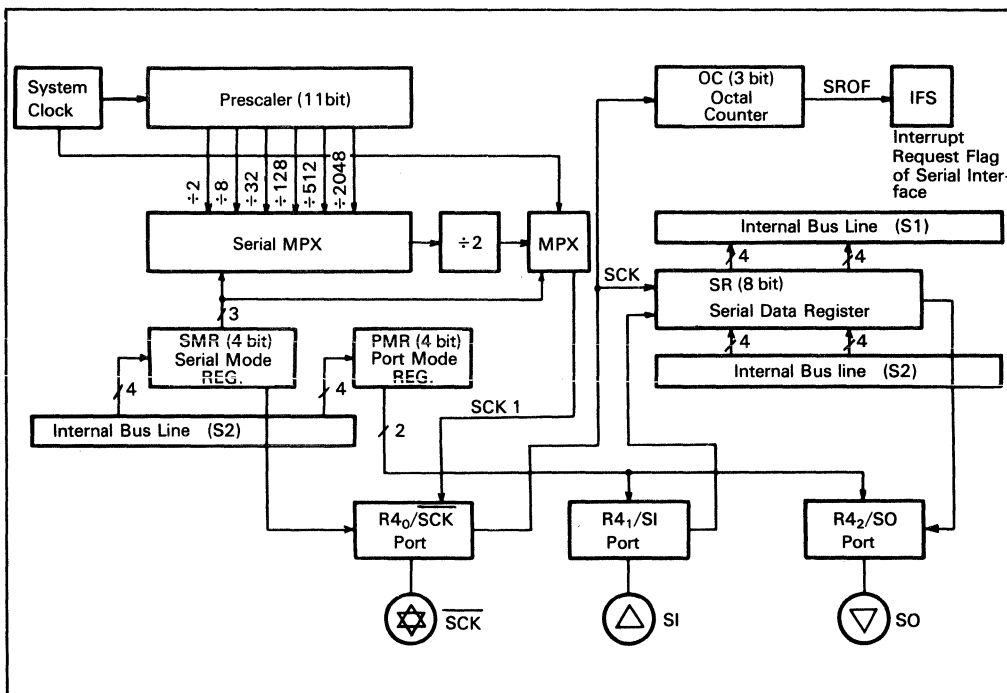


Figure 9. Serial Interface Block Diagram



output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the SI pin to the serial data register, to MSB first, synchronously with the rising edge of the transfer clock. Figure 10 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Serial Interrupt Request Flag (IFS: \$003 bit 0): The serial Interrupt request flag will be set when the octal counter counts eight

transfer clock signals, or when data transfer is discontinued by resetting the octal counter. Refer to table 8.

Serial Interrupt Mask (IMS: \$003 bit 1): The serial Interrupt mask masks the interrupt request. Refer to table 9.

Selection and Change of the Operation Mode: Table 10 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register. Initialize the serial interface by the write signal to the serial mode register, when the operation mode is changed.

Table 7. Serial Mode Register

SMR3	R4 ₀ /SCK
0	Used as R4 ₀ port input/output pin
1	Used as SCK input/output pin

Transfer Clock							
SMR2	SMR1	SMR0	R4 ₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio	
0	0	0	SCK Output	Prescaler	÷ 2048	÷	4096
0	0	1	SCK Output	Prescaler	÷ 512	÷	1024
0	1	0	SCK Output	Prescaler	÷ 128	÷	256
0	1	1	SCK Output	Prescaler	÷ 32	÷	64
1	0	0	SCK Output	Prescaler	÷ 8	÷	16
1	0	1	SCK Output	Prescaler	÷ 2	÷	4
1	1	0	SCK Output	System Clock	—	÷	1
1	1	1	SCK Input	External Clock	—	—	—

Operating State of Serial Interface: The serial interface has three operating states, the STS waiting state, SCK waiting state, and transfer state, as shown in figure 11.

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed, the serial interface shifts to SCK waiting state.

In this state the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the Octal Counter counts-up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the

transfer clock outputs continuously.

The octal counter becomes 000 again by 8 transfer clocks or by execution of STS instruction, so that the serial interface returns to SCK waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops after 8 clocks.

Example of Transfer Clock Error Detection: The serial interface functions abnormally when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 12.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts as the following sequence: first, transfer state, second, SCK waiting state and third, transfer state again. The serial

Table 8. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Serial Interface Operation Mode

SMR3	PMR1	PMR0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

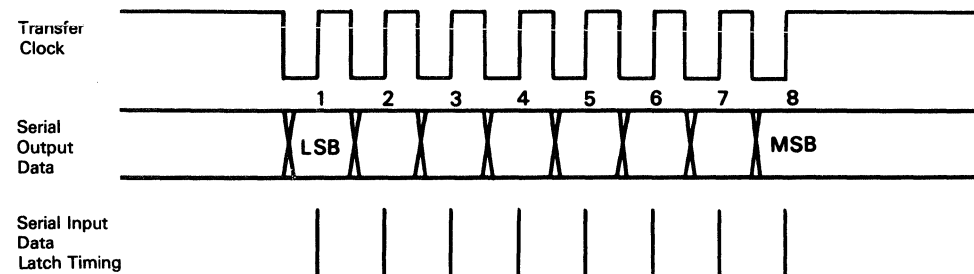


Figure 10. Serial Interface I/O Timing Chart



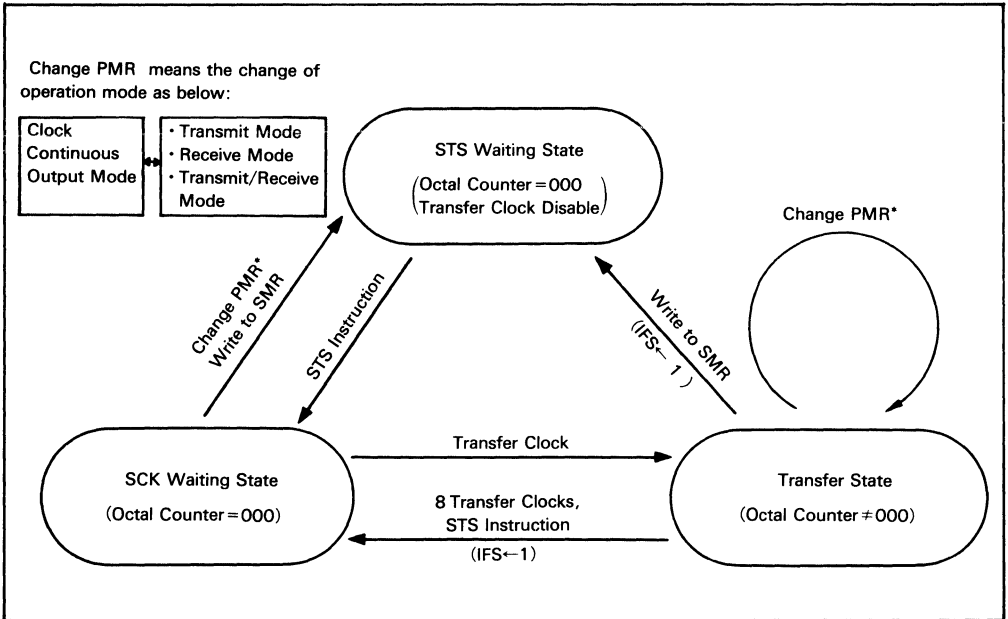


Figure 11. Serial Interface Operation State

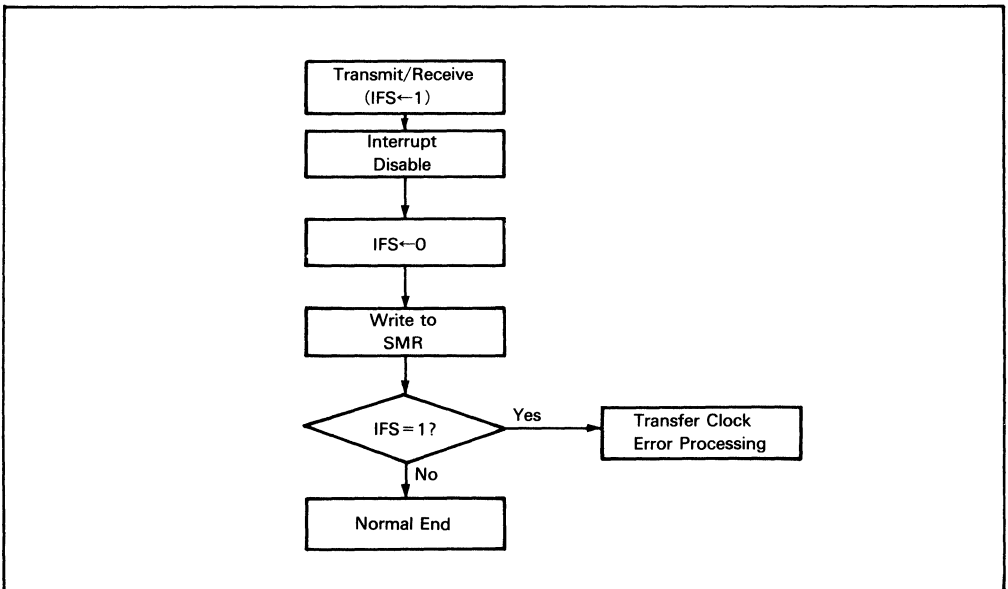


Figure 12. Example of Transfer Clock Error Detection

Interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial Interface Request Flag to be set again.

Timer

The MCU contains a prescaler and a timer/counter (timer A, timer B, figure 13) whose functions are the same as HMCS424C's. The prescaler is an 11-bit binary counter, timer A an 8-bit free-running timer/counter and timer B is an 8-bit auto-reload timer/event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface. The prescaler divide ratio is selected by the timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up to \$FF, timer A is set to \$00 again, and generating overflow output. This leads to setting timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal input.

The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by soft-

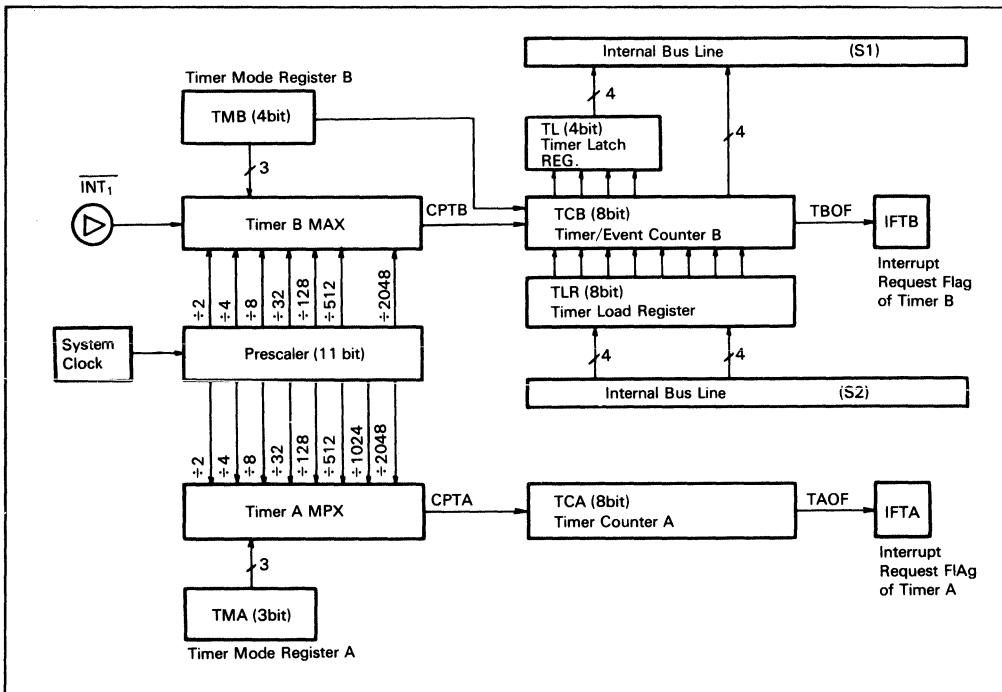


Figure 13. Timer Block Diagram



ware. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register A (TMA: \$008): The timer mode register A is a 3-bit write-only register. The TMA controls the prescaler divide ratio of timer A clock input, as shown in Table 11. The timer mode register A is initialized to \$0 by MCU reset.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 12. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of

TMB are changed. Configuration and function of timer mode register B is shown in figure 14.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set by the overflow output to time A (table 13).

Table 11. Timer Mode Register A

TMA2	TMA1	TMA0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Table 12. Timer Mode Register B

TMB3			Auto-reload Function
0			No
1			Yes

TMB2 TMB1 TMB0			Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	INT ₁ (External Event Input)

Timer A Interrupt Mask (IMTA: \$001 bit 3): Timer A interrupt mask prevents an interrupt request generated by timer A interrupt request flag (table 14).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request

flag is set by the overflow output of timer B (table 15).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B interrupt request flag (table 16).

Table 13. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 14. Timer A Interrupt Mask

Timer A Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

Table 15. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 16. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

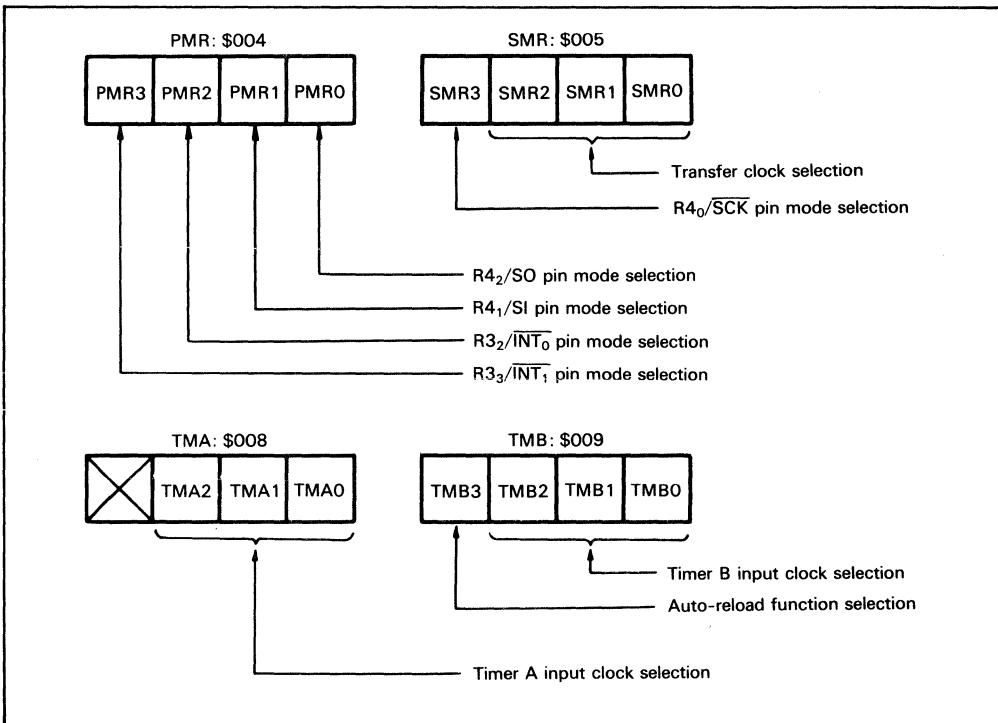


Figure 14. Mode Register Configuration and Function

Input/Output

The MCU has 50 I/O pins, 12 standard without pull-up MOS (NMOS open drain) and 24 high voltage without pull-down MOS (PMOS open drain). See table 17 as for I/O pin circuit types.

When every input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 18.

D Port: The D port is an I/O port which has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 17 as for the classification of standard pin, high-voltage pin, and the I/O pin circuit types.

R Ports: The six R ports in the MCU are composed of 16 I/O pins, 4 output-only pins, and 1 input-only pin. Data is input through

LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and/or non-existing ports, while invalid data will be read by reading from the output-only and/or non-existing ports.

The R₃₂, R₃₃, R₄₀, R₄₁, and R₄₂ pins are multiplexed with the INT₀, INT₁, SCK, SI, and SO pins respectively. See table 17 as for the classification of standard pins, high-voltage pins and selectable circuit types of these I/O pins.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 19 shows the parts initialized by MCU reset, and the status of each.

Table 17. I/O Pin Circuit Types

		Without pull-up MOS (NMOS open drain)	Applicable pins
Standard Pins	I/O Common Pins		D ₀ - D ₃ R ₃₀ - R ₃₃ R ₄₀ - R ₄₃
	Input pins		INT ₀ INT ₁

		Without pull-down MOS (PMOS open drain)	Applicable pins
High Voltage Pins	I/O Common Pins		$D_4 - D_{14}$ $R1_0 - R1_3$ $R2_0 - R2_3$
	Output Pins		$R0_0 - R0_3$
	Input Pins		RA_1

Note: 1. In the stop mode, \overline{HLT} signal is 0, HLT signal is 1 and I/O pins are in high impedance.

Table 18. Data Input from Input/Output Common Pins

I/O Pin Circuit Type		Input Possible	Input Pin State
Standard Pins	Without pull-up MOS (NMOS open drain)	Yes	1
High Voltage Pins	Without pull-down MOS (PMOS open drain)	Yes	0

Table 19. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	Standard Pin Without Pull-Up MOS	0	Enable to input
	High Voltage Without Pull-Down MOS	0	Enable to input
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Serial Mode Register (SMR)	0000	See serial mode register
	Timer Mode Register A (TMA)	000	See timer mode register A
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Counter A (TCA)	\$00	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—
	Octal Counter	000	—

Note: MCU reset affects the rest of registers as follows:

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above



Internal Oscillator Circuit

Figure 15 outlines the internal oscillator circuit. Without mask option, either crystal oscillator or ceramic filter oscillator can be

selected as the oscillator type. Refer to table 20 for selection of the type. In addition, see figure 16 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available.

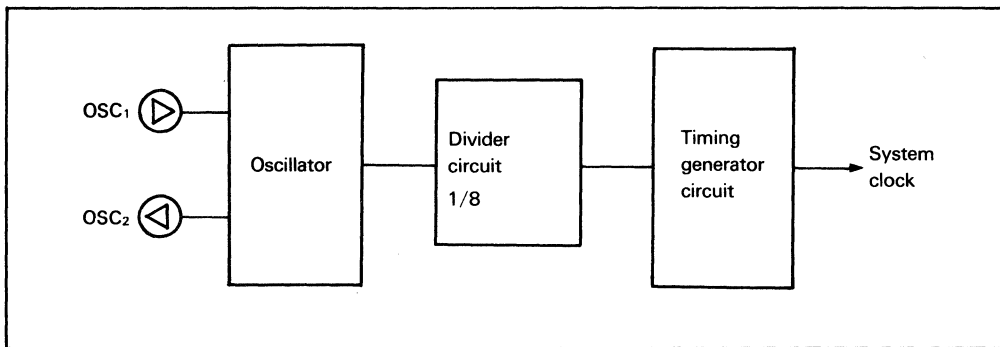


Figure 15. Internal Oscillator Circuit

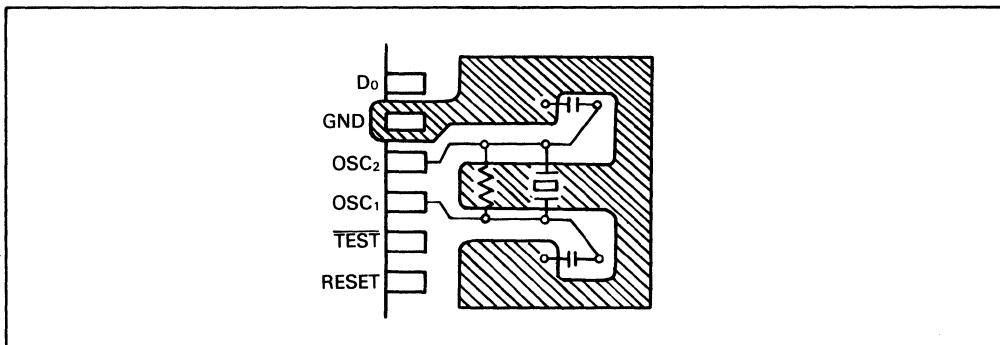
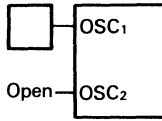
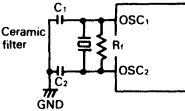
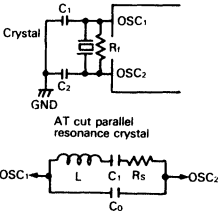


Figure 16. Layout of Crystal and Ceramic Filter

Table 20. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation	<p>Oscillator</p> 	
Ceramic Filter Oscillator		<p>Ceramic filter: CSA 8.00MT (Murata)</p> <p>R_f: $1M\Omega \pm 20\%$</p> <p>C_1: $30pF \pm 20\%$</p> <p>C_2: $30pF \pm 20\%$</p>
Crystal Oscillator	 <p>AT cut parallel resonance crystal</p>	<p>Crystal: 8.388608 (MHz)</p> <p>NC-18 (Nihon Denpa Kogyo)</p> <p>R_f: $1M\Omega \pm 2\%$</p> <p>C_1: $10pF \pm 20\%$</p> <p>C_2: $10pF \pm 20\%$</p> <p>Crystal: AT cut parallel resonance crystal</p> <p>C_0: 7pF max.</p> <p>R_S: 100Ω max.</p> <p>f: 1.0~9.0 MHz</p>

- Notes:
1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
 2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 17).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 21). Figure 17 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 21. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition					Input/Output Pin	Timer/Counter, Serial Interface	Recovery Method
		Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM			
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ²	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ¹	Stop	Retained	High impedance	Stop	RESET input

- Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to table 18 for the contents of the flags and registers.
 2. As an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

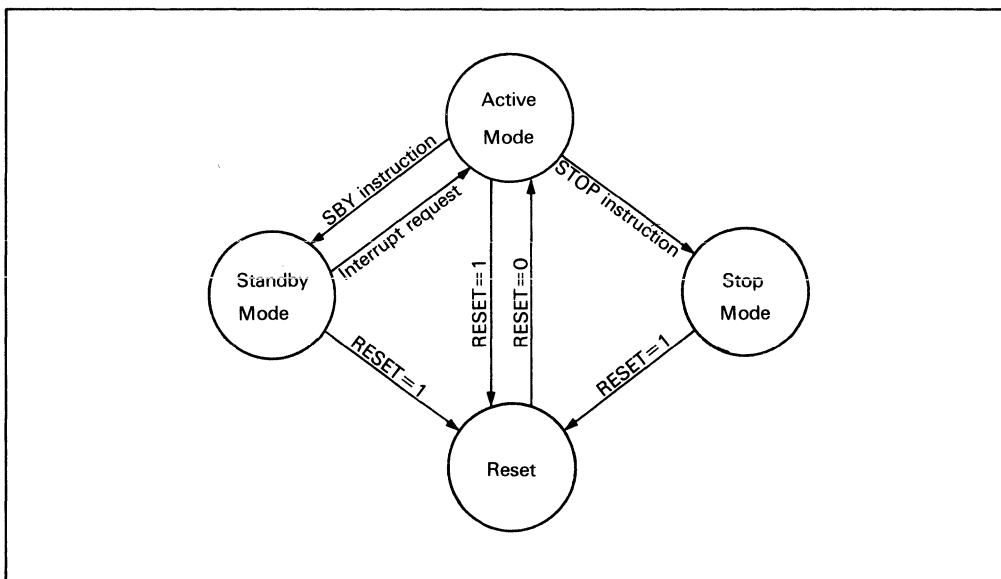


Figure 17. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 18 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

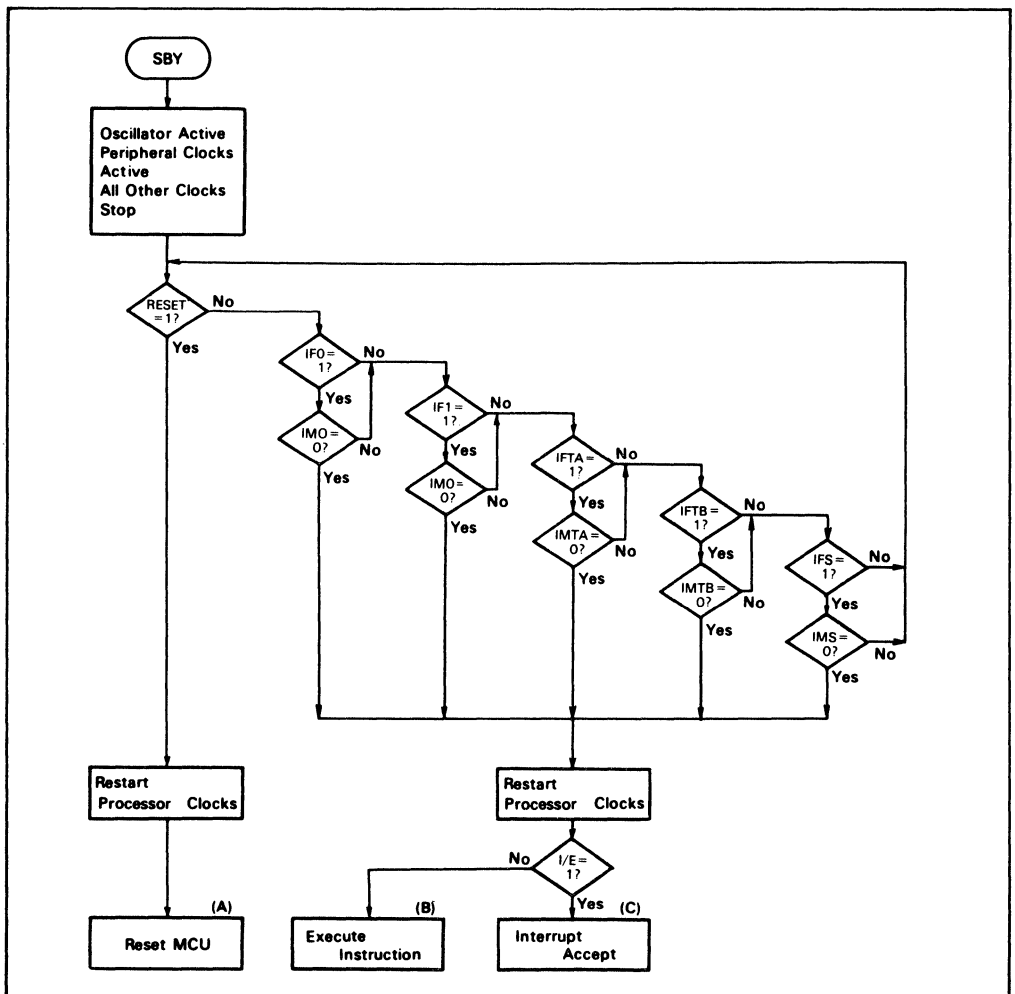


Figure 18. MCU Operating Flowchart in Standby Mode

RAM Addressing Mode

As shown in Figure 20, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 21.

Direct addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on page boundary (256n + 255) (figure 22), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 23). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

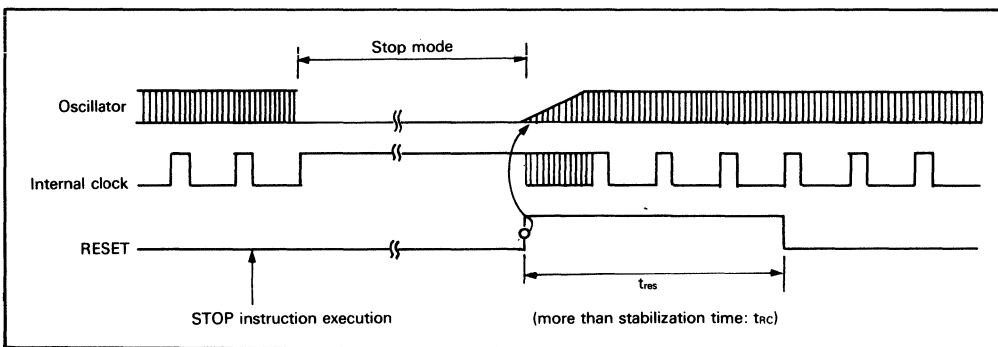


Figure 19. Timing Chart of Recovering from Stop Mode



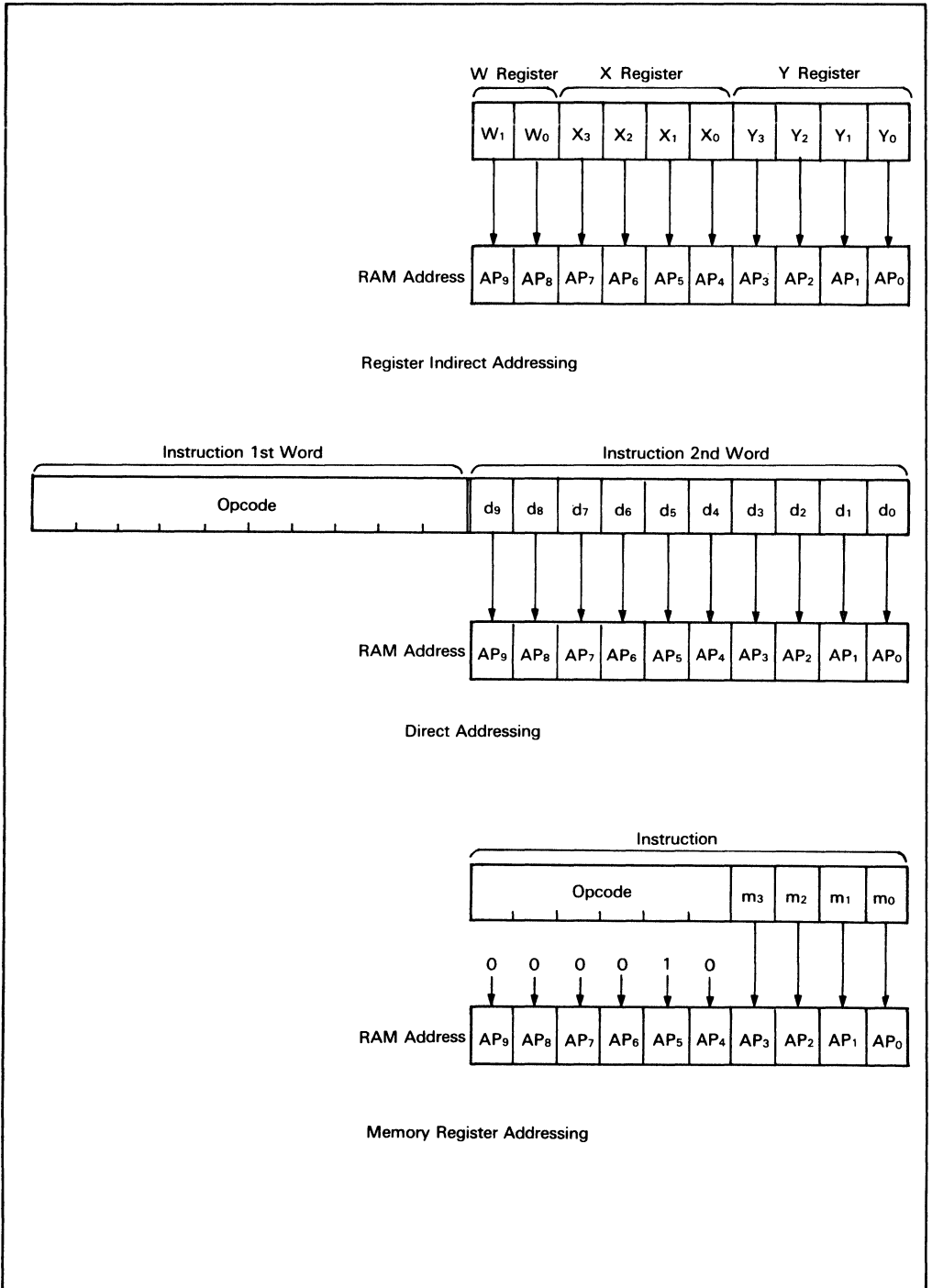


Figure 20. RAM Addressing Mode



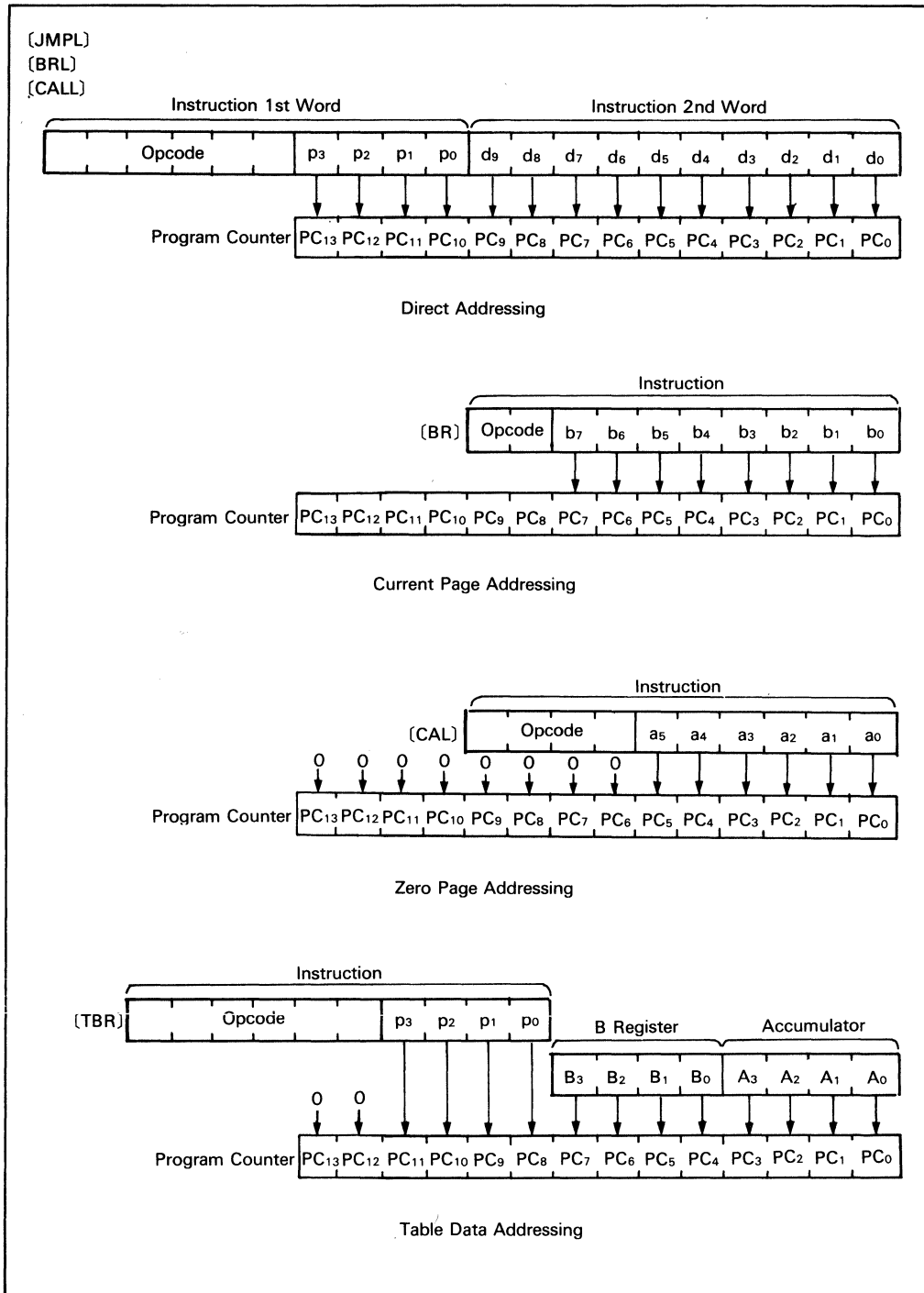


Figure 21. ROM Addressing Mode



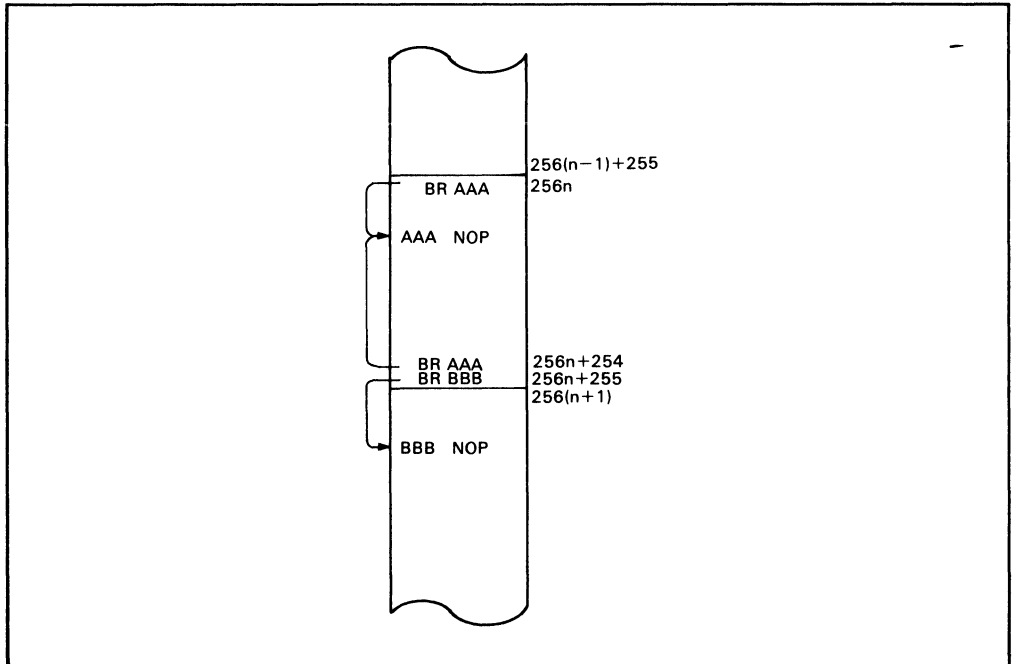


Figure 22. The Branch Destination by BR Instruction on the Boundary between Pages

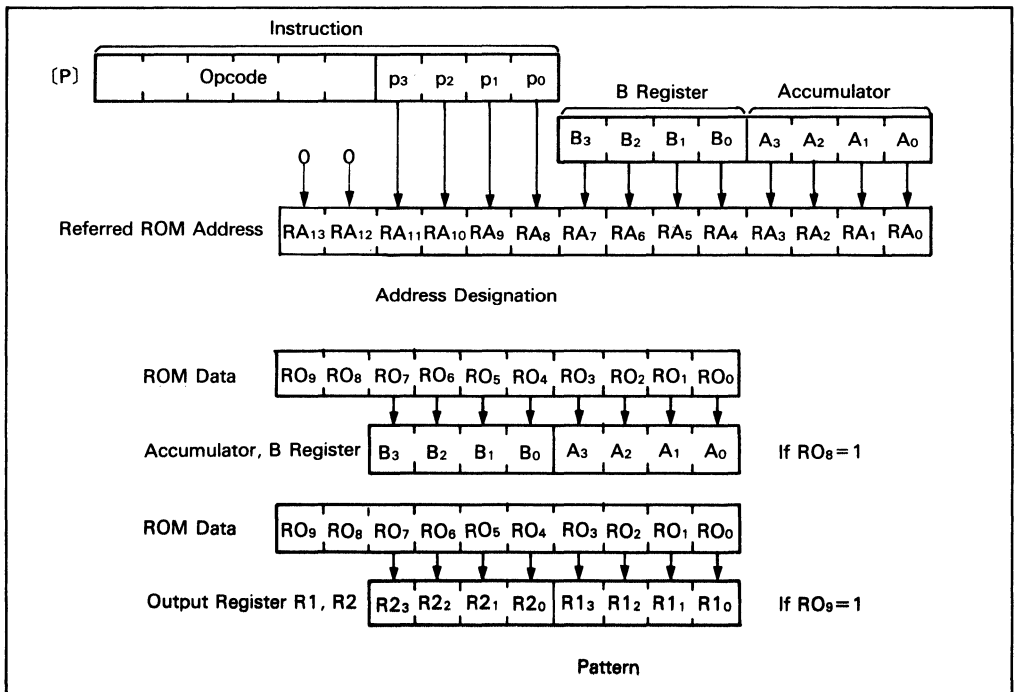


Figure 23. P Instruction

Instruction Set

The HD40P4281/HD40P42161 provide 101 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction

5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 22-31 list their functions, and table 32 is an opcode map.

Table 22. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 23. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 Note
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 24. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 Note
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 25. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 26. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A+CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M-A- $\bar{CA} \rightarrow A$ NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M-A- $\bar{CA} \rightarrow A$ NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR

Table 27. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 28. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 · M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 29. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 30. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 31. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	- 0.3 to + 7.0	V	
Terminal Voltage	V_T	- 0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	- I_O	4	mA	9, 10
		6	mA	9, 11
		30	mA	9, 12
Total Allowance of Output Current	- ΣI_O	150	mA	6
Operating Temperature	T_{opr}	- 20 to + 75	°C	
Storage Temperature	T_{stg}	- 55 to + 125	°C	

- Notes:
1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_3$ and R3, R4.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $D_0 - D_3$ and R3, R4.
 11. R0 - R2.
 12. $D_4 - D_{14}$.

Electrical Characteristics

DC Characteristics

($V_{CC} = 4.5 - 5.5$ V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, $\overline{\text{SCK}}$ R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / INT_1	0.8 V_{CC}		$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, $\overline{\text{SCK}}$ R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / INT_1	- 0.3		0.2 V_{CC}	V		
		SI	- 0.3		0.3 V_{CC}	V		
		OSC ₁	- 0.3		0.5	V		
Output High Voltage	V_{OH}	$\overline{\text{SCK}}$, SO	$V_{CC} - 1.0$			V	$- I_{OH} = 1.0$ mA	
			$V_{CC} - 0.5$			V	$- I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	$\overline{\text{SCK}}$, SO			0.4	V	$I_{OL} = 1.6$ mA	
Input/Output Leakage Current	$ I_{II} $	RESET, $\overline{\text{SCK}}$ R3 ₂ / $\overline{\text{INT}}_0$, R3 ₃ / INT_1 , SI, SO, OSC ₁			1	μA	$V_{in} = 0$ V to V_{CC}	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			TBD	mA	$V_{CC} = 5$ V; $f_{osc} = 8$ MHz, $\div 8$	2,4
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}			TBD	mA	$V_{CC} = 5$ V; $f_{osc} = 8$ MHz, $\div 8$	3,4
Current Dissipation in Stop Mode	I_{stop}	V_{CC}			10	μA	$V_{in}(\overline{\text{TEST}}) = V_{CC} - 0.3$ V to V_{CC} ; $V_{in}(\text{RESET}) = 0$ V to 0.3 V	
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes: 1. Excluding pull-up MOS current and output buffer current.
 2. The MCU is in the reset state. Input/output current does not flow.
- MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - D₀-D₃, R₃, R₄: V_{CC}
 - D₄-D₁₄, R₀-R₂, RA₁: V_{CC} to $V_{CC} - 40$ V

3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₃, R3, R4: V_{CC}
 - D₄-D₁₄, R0-R2, RA₁: V_{CC} to $V_{CC} - 40$ V
4. When $f_{osc} = x$ MHz, estimate the current dissipation as follows:
 Max value @ x MHz = $x/8 \times$ (max value @ 8 MHz)

Input/Output Characteristics for Standard Pin

($V_{CC} = 4.5 - 5.5$ V, GND = 0 V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₃ , R3, R4	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₃ , R3, R4	- 0.3		$0.3V_{CC}$	V		
Output Low Voltage	V_{OL}	D ₀ -D ₃ , R3, R4			0.4	V	$I_{OL} = 1.6$ mA	
Input/Output Leakage Current	I_{IL}	D ₀ -D ₃ , R3, R4			1	μA	$V_{in} = 0$ V to V_{CC}	1

Note: 1. Output buffer current are excluded.

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Input/Output Characteristics for High Voltage Pin

($V_{CC} = 4.5 - 5.5$ V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₄ -D ₁₅ , R ₁ , R ₂ , R _{A1}	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₄ -D ₁₅ , R ₁ , R ₂ , R _{A1}	$V_{CC} - 40$		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D ₄ -D ₁₅	$V_{CC} - 3.0$			V	$- I_{OH} = 15$ mA	
			$V_{CC} - 2.0$			V	$- I_{OH} = 10$ mA	
			$V_{CC} - 1.0$			V	$- I_{OH} = 4$ mA	
		R ₀ -R ₂	$V_{CC} - 3.0$			V	$- I_{OH} = 3$ mA	
			$V_{CC} - 2.0$			V	$- I_{OH} = 2$ mA	
			$V_{CC} - 1.0$			V	$- I_{OH} = 0.8$ mA	
Output Low Voltage	V_{OL}	D ₄ -D ₁₄ , R ₀ -R ₂			$V_{CC} - 37$	V	$150\text{k}\Omega$ to $V_{CC} - 40\text{V}$	
Input/Output Leakage Current	$ I_{II} $	D ₄ -D ₁₄ , R ₀ -R ₂ , R _{A1}			20	μA	$V_{in} = V_{CC} - 40$ V to V_{CC}	1

Note: 1. Output buffer current are excluded.



AC Characteristics

($V_{CC} = 4.5 - 5.5$ V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	8	9	MHz	divide by 8	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs	divide by 8	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	41			ns	divide by 8	2
			41			ns	divide by 8	2
External Clock Rise Time	t_{CPr}	OSC ₁			15	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			15	ns		2
$\overline{\text{INT}}_0$ High Level Width	t_{i0H}	$\overline{\text{INT}}_0$	2			t_{cyc}		3
$\overline{\text{INT}}_0$ Low Level Width	t_{i0L}	$\overline{\text{INT}}_0$	2			t_{cyc}		3
$\overline{\text{INT}}_1$ High Level Width	t_{i1H}	$\overline{\text{INT}}_1$	2			t_{cyc}		3
$\overline{\text{INT}}_1$ Low Level Width	t_{i1L}	$\overline{\text{INT}}_1$	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1$ MHz, $V_{in} = 0$ V	
RESET Fall Time	t_{RSTf}				20	ms		4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage $V_{CC} = 4.5$ V after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.

- 2. See figure 24.
- 3. See figure 25.
- 4. See figure 26.

Serial Interface Timing Characteristics

AT Transfer Clock Output

($V_{CC} = 4.5 - 5.5$ V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{scyc}	$\overline{\text{SCK}}$	1			t_{cyc}		1.2
Transfer Clock High, Low Level Width	t_{sckh} t_{sckl}	$\overline{\text{SCK}}$	0.5			t_{scyc}		1.2
Transfer Clock Rise, Fall Time	t_{sckr} t_{sckf}	$\overline{\text{SCK}}$			100	ns		1.2
Serial Output Data Delay time	t_{dso}	SO			250	ns		1.2
Serial Input Data Set-up Time	t_{ssi}	SI	300			ns		1
Serial Input Data Hold Time	t_{hsi}	SI	150			ns		1

Notes: 1. See figure 27.
2. See figure 28.

AT Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{scyc}	$\overline{\text{SCK}}$	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{sckh} t_{sckl}	$\overline{\text{SCK}}$	0.5			t_{scyc}		1
Transfer Clock Rise, Fall Time	t_{sckr} t_{sckf}	$\overline{\text{SCK}}$			100	ns		1
Serial Output Data Delay Time	t_{dso}	SO			250	ns		1.2
Serial Input Data Set-up Time	t_{ssi}	SI	300			ns		1
Serial Input Data Hold Time	t_{hsi}	SI	150			ns		1

Notes: 1. See figure 27.
2. See figure 28.

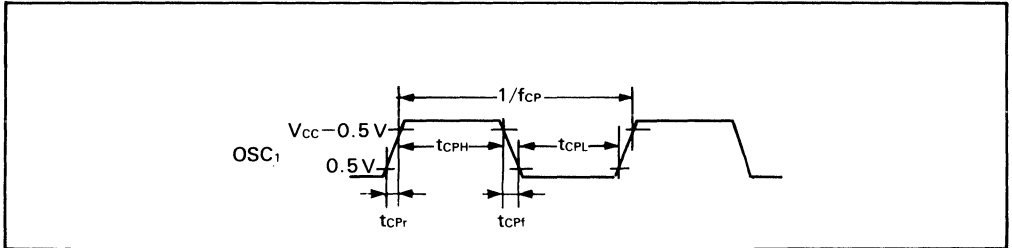


Figure 24. Oscillator Timing

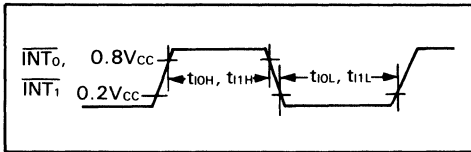


Figure 25. Interrupt Timing

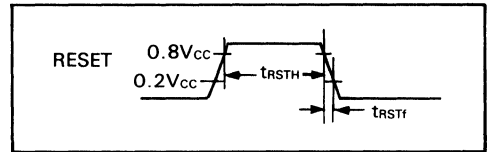


Figure 26. Reset Timing

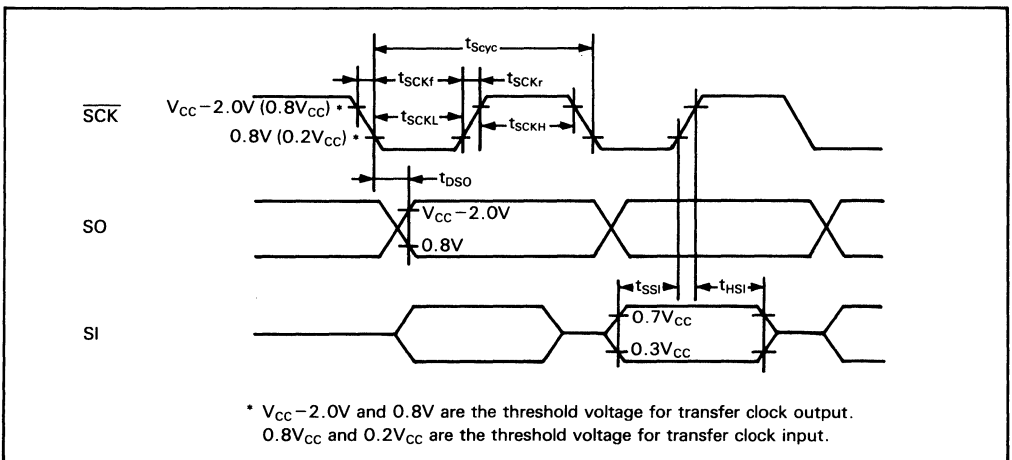


Figure 27. Timing Diagram of Serial Interface

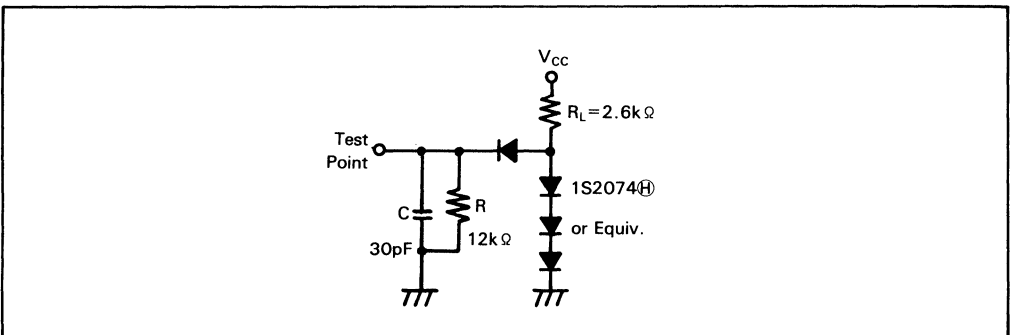


Figure 28. Timing Load Circuit

HD40P4281/HD40P42161

Precautions on Using EPROM on chip type 4-bit Single-Chip Microcomputer

Since the HD40P4281/HD40P42161 has a special structure with pin sockets installed on the surface of the package, the following should be noted when using it.

- (1) Do not apply an electric voltage or surge voltage more than the maximum ratings to the pin socket pins. This may destroy the LSI permanently.
- (2) When installing this LSI in system products in the same way as the mask ROM 4-bit single chip microcomputer, observe the following in order to maintain good ohmic contact between EPROM pins and pin sockets.
 - (a) When soldering the LSI on a printed

circuit board, keep pin conditions under 250 °C within 10 seconds. If these conditions are exceeded, the solder fixing the pin sockets may melt and the pins may fall out.

- (b) Keep out detergent on coater from the pin sockets during flux removal or board coating. Flux or coater may decrease pin socket contactivity.
- (c) Avoid permanent use of this LSI in places with excessive vibration.
- (d) Since repeated insertion/removal of EPROMs may decrease pin sockets contactivity, it is recommended to use new ones for your system products. Please ask Hitachi's sales office if you have any question.

Difference Between The HD40P4281/HD40P42161 and HMCS424C/428C

Table 33. The Difference between HD40P4281/HD40P42161 and HMCS424C/428C

Item	HD40P4281/HD40P42161	HMCS424AC	HMCS424C	HMCS424CL
Power Supply Voltage	4.5 to 5.5 V	4.5 to 6 V	3.5 to 6 V	2.5 to 6 V
ROM	<ul style="list-style-type: none"> ○4,096 words × 10 bits (using standard EPROM 2764) ○8,192 words × 10 bits (using standard EPROM 27128) 		4,096 words × 10 bits Mask ROM	
RAM	992 digits × 4 bits		256 digits × 4 bits	
I/O pin circuit type	Standard pins	All pins are "without pull-up MOS (NMOS open drain)".	One of three circuit types, without pull-up MOS (NMOS open drain), with pull-up MOS, CMOS, can be selected for each standard pin.	
	High voltage pin	All pins are "without pull-down MOS (PMOS open drain)".	One of two circuit types, without pull-down MOS (PMOS open drain), with pull-down MOS, can be selected for each high voltage pin.	
Oscillator	Crystal oscillator, Ceramic filter oscillator	Crystal oscillator, Ceramic filter oscillator		
Package	42-pin EPROM on package. The base chip pins are compatible with those of the HMCS424C/428C.	42-pin dual in line package (DP-42) 42-pin shrink dual in line package (DP-42S) 44-pin flat plastic package (FP-44A)		
Type/ Occupied area (mm)/ Height from Stand-off	DC-42P/ 19 × 52.8/ 7.5mm (max)	DP-42/13.4 × 52.8/5.08 (max) DP-42S/14 × 37.4/5.08 (max) FP-44A/17.2 × 17.2/2.9 (max)		



HMCS400 Series Application Specific Microcomputer



HD404302/HD4074308

—Preliminary—

Description

The HD404302 and HD4074308 are CMOS 4-bit single-chip microcomputers basically equivalent to the HMCS400 series providing high programming productivity, high speed operation, and low power dissipation. They incorporate ROM, RAM, I/O, A/D converter, and timer/counter, and contain high voltage I/O pins to drive fluorescent display tube directly.

- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation-table lookup capability
- Bit manipulation for both RAM and I/O

Features

- 4-bit architecture
- 2048 words of 10-bit ROM (mask ROM version)
- 8192 words of 10-bit ROM (ZTAT version)
- 160 digits of 4-bit RAM
- 33 I/O pins, including 25 High voltage I/O pins (40 V max)
- Two Timers/Counters
 - 11-bit prescaler
 - 8-bit timer (free-run timer/watchdog timer)
 - 8-bit timer (reload timer/event counter)
- Five interrupt sources
 - External 2
 - Timer 2
 - A/D 1
- A/D converter: 8 bits × 4 channels
- Two Tone generator outputs: 2
- Subroutine Stack
 - Up to 16 levels including interrupts
- Two low power dissipation modes
 - Standby mode
 - Stop mode
- On-chip oscillator
 - Crystal or ceramic filter (externally drivable)
- Package
 - 42-pin plastic DIP (DP-42)
 - 42-pin ceramic DIP with window (DC-42)
- Instruction set compatible with HMCS412C; 100 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all ROM areas
- Direct or indirect addressing of all RAM areas

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device
- Emulator unit can be used for both HMCS400 series and AS microcomputer

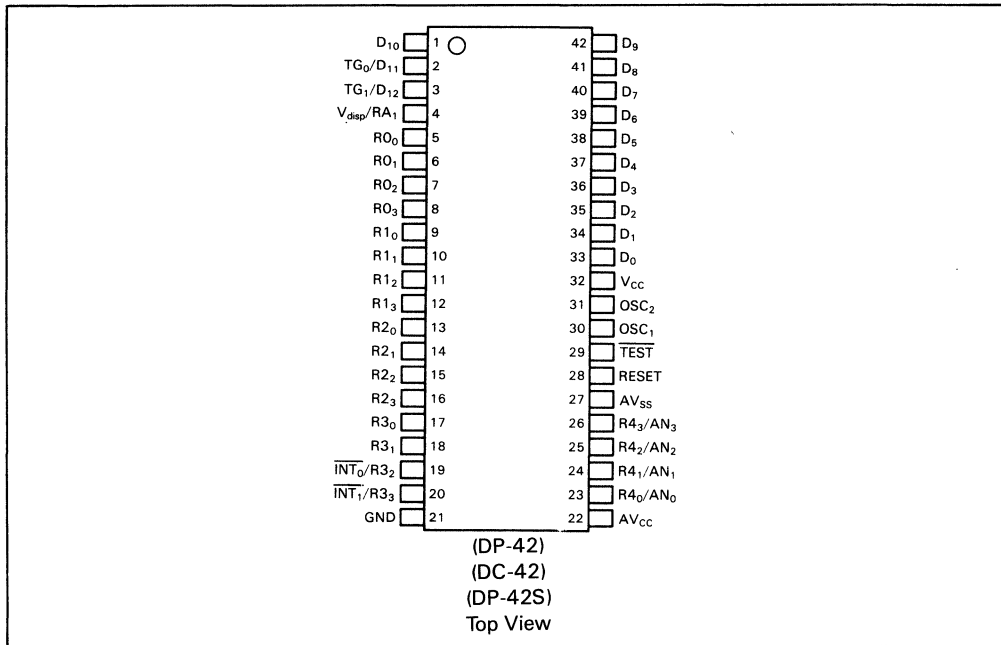
Ordering Information

	Part No.	ROM(Words)	Package
Mask ROM type	HD404302P	2,048	DP-42 DP-42S
ZTAT type	HD4074308P	8,192	DP-42
	HD4074308C		DC-42 (Note)

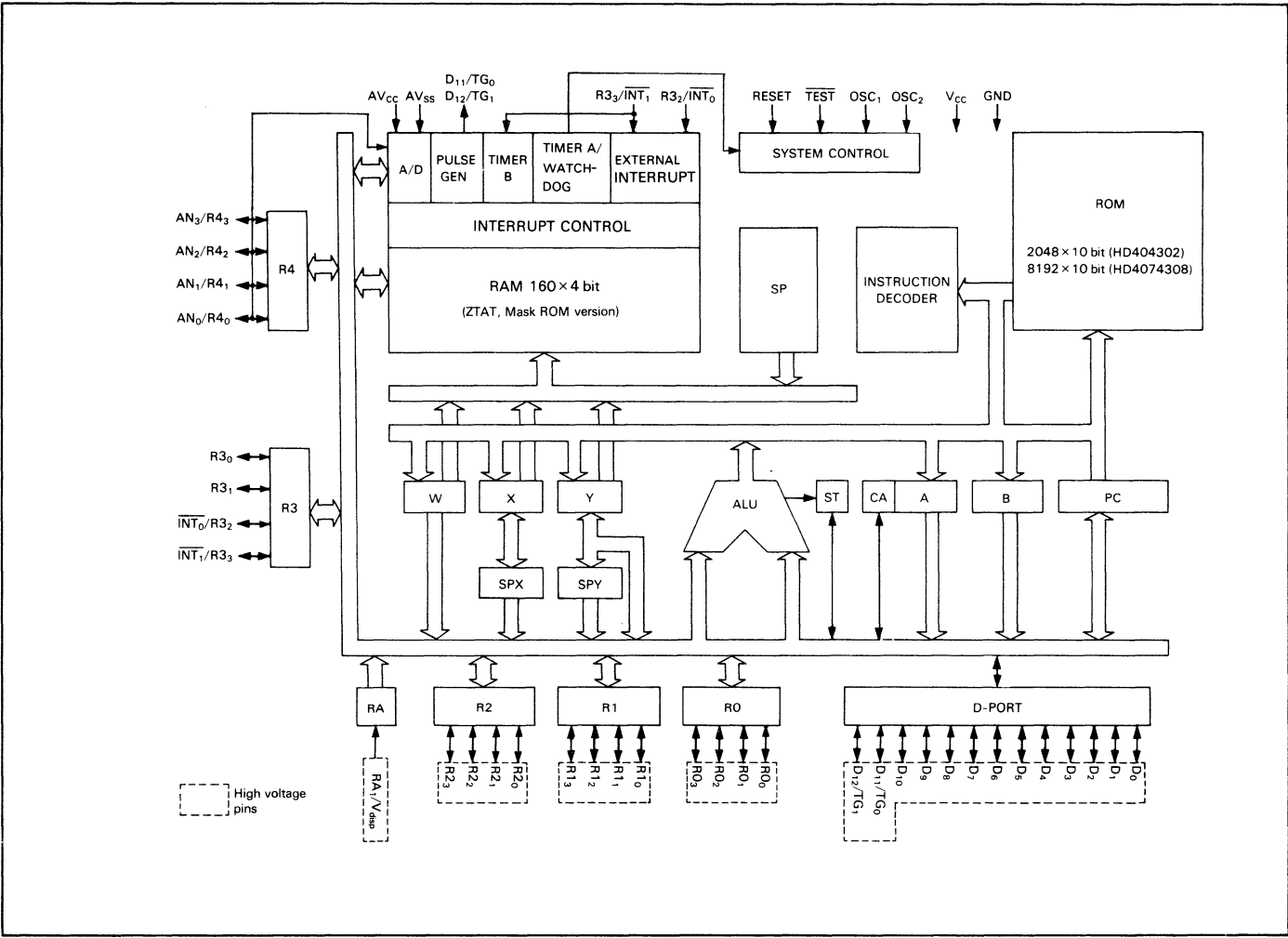
Note: Under Development



Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC}, V_{disp} (Power)

GND, V_{CC}, and V_{disp} are the Power supply pins for the MCU. Connect the GND to the ground and apply the V_{CC} power supply voltage to the V_{CC} pin. The V_{disp} pin (multiplexed with RA₁) is a power supply for high voltage output pin with maximum voltage of V_{CC}-40V. For details, see Input/Output section.

AV_{CC}, AV_{SS}

AV_{CC} and AV_{SS} are the power supply pins for the A/D converter.

TEST (Test)

Input for a factory test mode. The user should tie this pin to V_{CC} for normal operation.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are pins for the internal oscillator circuit. They can be connected to the crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see internal Oscillator Circuit section.

D₀-D₁₂ (D Port)

The D port is an input/output port addressed

by the bit. These 13 pins are all high-voltage input/output pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀-R₀₃, R₁₀-R₁₃, R₂₀-R₂₃, R₃₀-R₃₃, R₄₀-R₄₃, RA(R Ports)

R₀ to R₄ are 4-bit I/O ports. RA is a 1-bit port. RA is an input port, and R₀ to R₄ I/O ports. The pins of R₀-R₂ and RA₁ are high-voltage pins, and the pins of R₃-R₄ are standard pins. R₃₂ and R₃₃ are multiplexed with $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ respectively. For details, see Input/Output section.

$\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$ (Interrupt)

$\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ are external interrupts for the MCU. $\overline{\text{INT}}_1$ can be used as an external event input pin for timer B. $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

TG₀, TG₁

TG₀ and TG₁ are tone generator output pins. These pins are high-voltage pins multiplexed with D₁₁ and D₁₂, respectively.

AD Port (AN₀-AN₃)

The AD port is an A/D converter input port. AN₀-AN₃ are multiplexed with R₄₀-R₄₃, respectively. For details, see A/D converter section.

Memory Map

ROM Memory Map

ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$07FF): Locations \$0000 through \$07FF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.
 \$0000-\$07FF: HD404302
 \$0000-\$1FFF: HD4074308

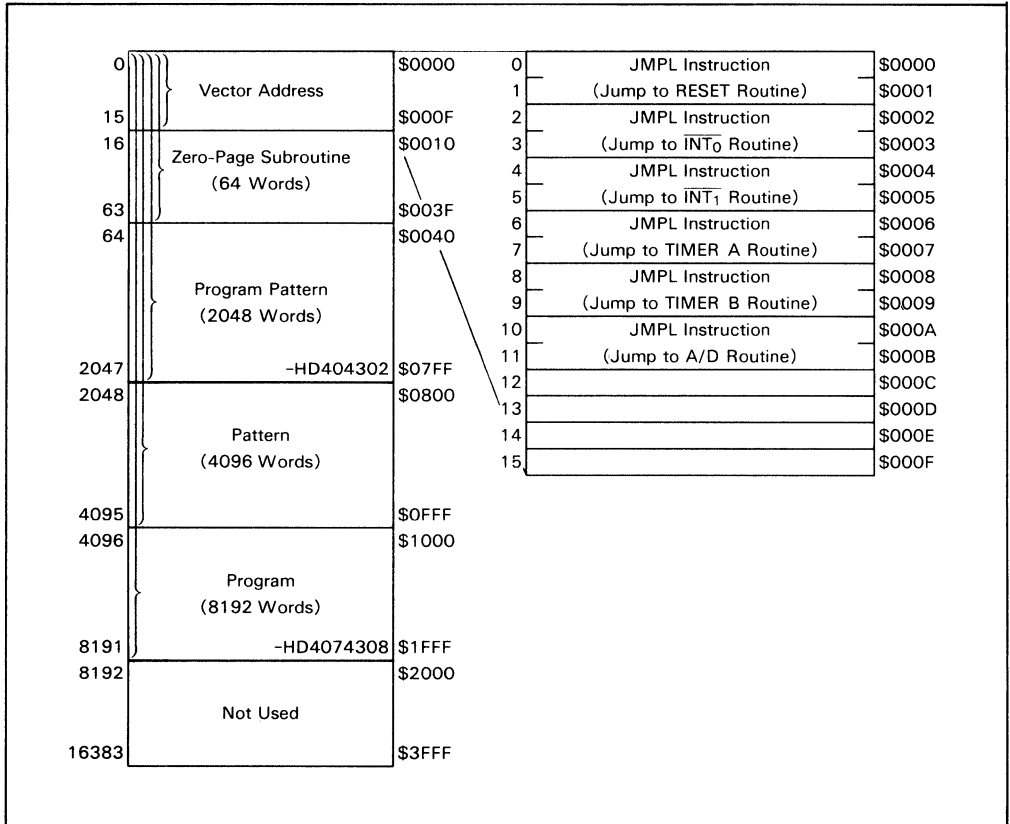


Figure 1. ROM Memory Map

RAM Memory Map

The MCU includes 160 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003):

The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$034):

The special function registers are the mode or data registers for the external interrupt, the A/D, and the timer/counter and are the I/O port data control registers. These registers are classified into three types: write-only, read-only, and read/write as shown in

figure 2. These registers cannot be accessed by RAM bit manipulation instructions. However, WDON (\$020) can be accessed by only that instructions.

Data Area (\$040 to \$09F): 16 digits of \$040 through \$09F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for stack area to save the contents of the program counter (PC), status (ST) and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

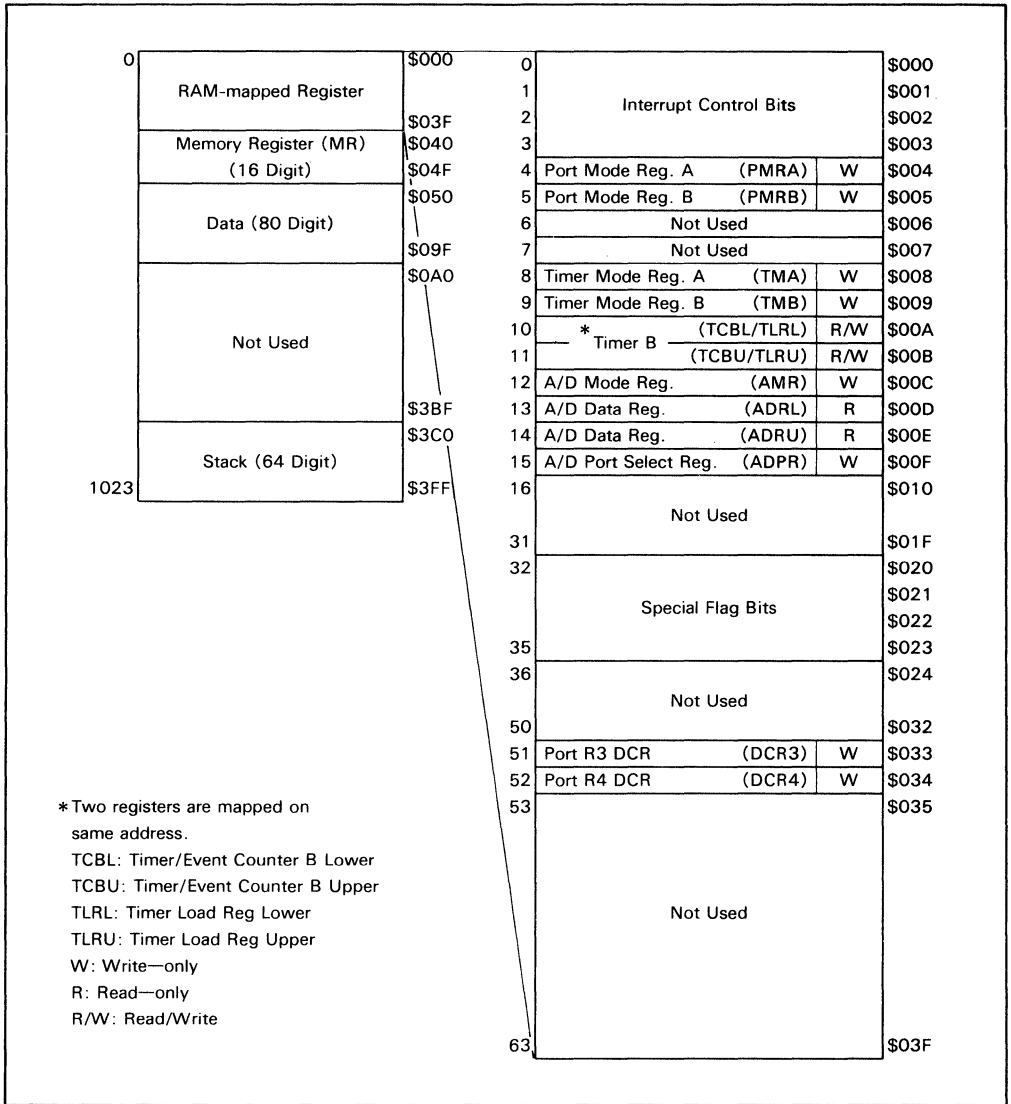


Figure 2. RAM Memory Map

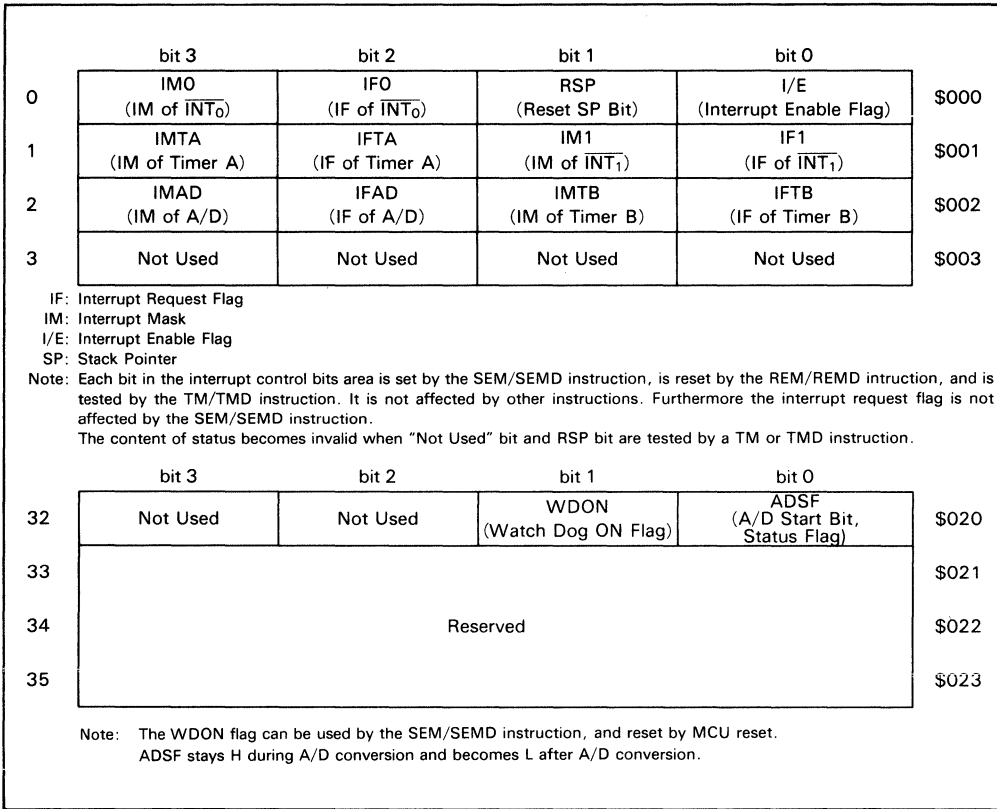


Figure 3. Configuration of Interrupt Control Bit Area

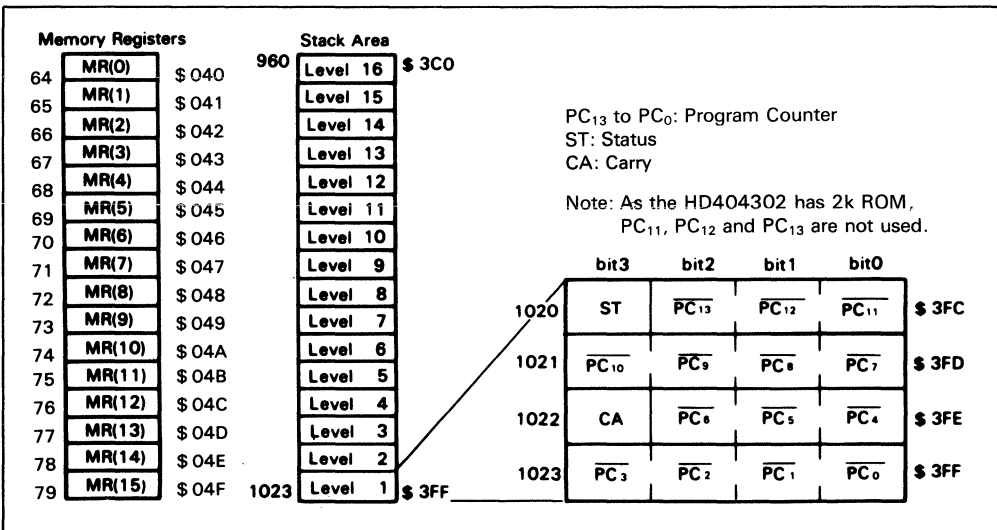


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Functional Description

Register and Flags

The MCU has nine registers and two flags for CPU operation. The following paragraphs describe the registers and flags in detail. Figure 5 shows these registers and flags.

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the Arithmetic Logic Unit (ALU) as well as transfer data between memories, I/O and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry (CA): The carry flag (CA) indicates an overflow resulting from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL and ROTR instructions. The content of the carry flag is pushed onto the stack during interrupt servicing, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions and the result of the bit test instruction. Moreover, the status flag controls branches caused by the BR, BRL, CAL or CALL instructions. Whether these instructions are executed or skipped, the status flag is set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, and branch instruction is executed. During interrupt servicing, the content of the status is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which holds the ROM address.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to \$3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit (\$000-bit1) is reset by the REM or REMD instructions.

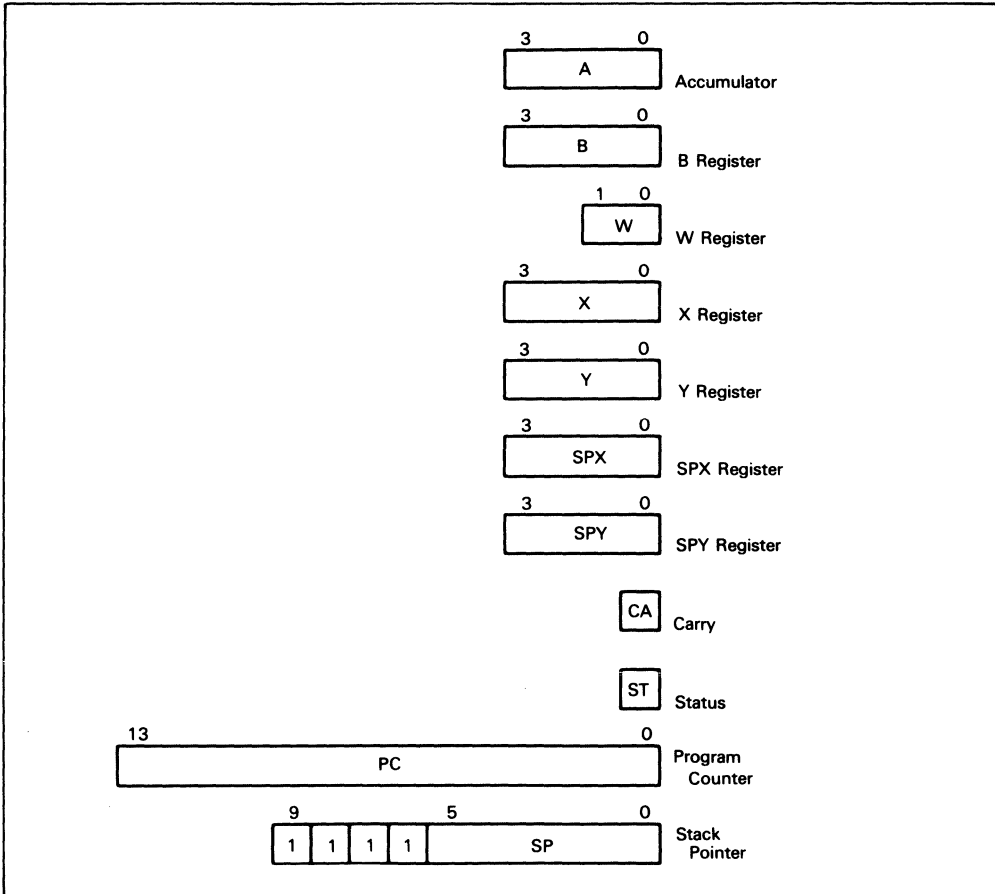


Figure 5. Registers and Flags

Interrupt

Five interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), timer/counter (timer A, timer B), and A/D. For each source, the interrupt request flag (IF), interrupt mask (IM) and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (I/E) is also used to control the total interrupt operations.

Interrupt Control Bits and Interrupt Service:

The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (I/E) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and Table 2

shows the interrupt conditions corresponding to each interrupt source. The interrupt request is generated when the IF is set to 1 and IM is 0. If the I/E is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and Figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The I/E is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after jumping to the vector address.

In each vector address, program JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	—	\$0000
$\overline{INT_0}$	1	\$0002
$\overline{INT_1}$	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
A/D	5	\$000A

Table 2. Conditions of interrupt Service

Interrupt control bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer A	Timer B	A/D
I/E	1	1	1	1	1
IFO · $\overline{IM_0}$	1	0	0	0	0
IF1 · $\overline{IM_1}$	*	1	0	0	0
IFTA · \overline{IMTA}	*	*	1	0	0
IFTB · \overline{IMTB}	*	*	*	1	0
IFAD · \overline{IMAD}	*	*	*	*	1

*: Don't care

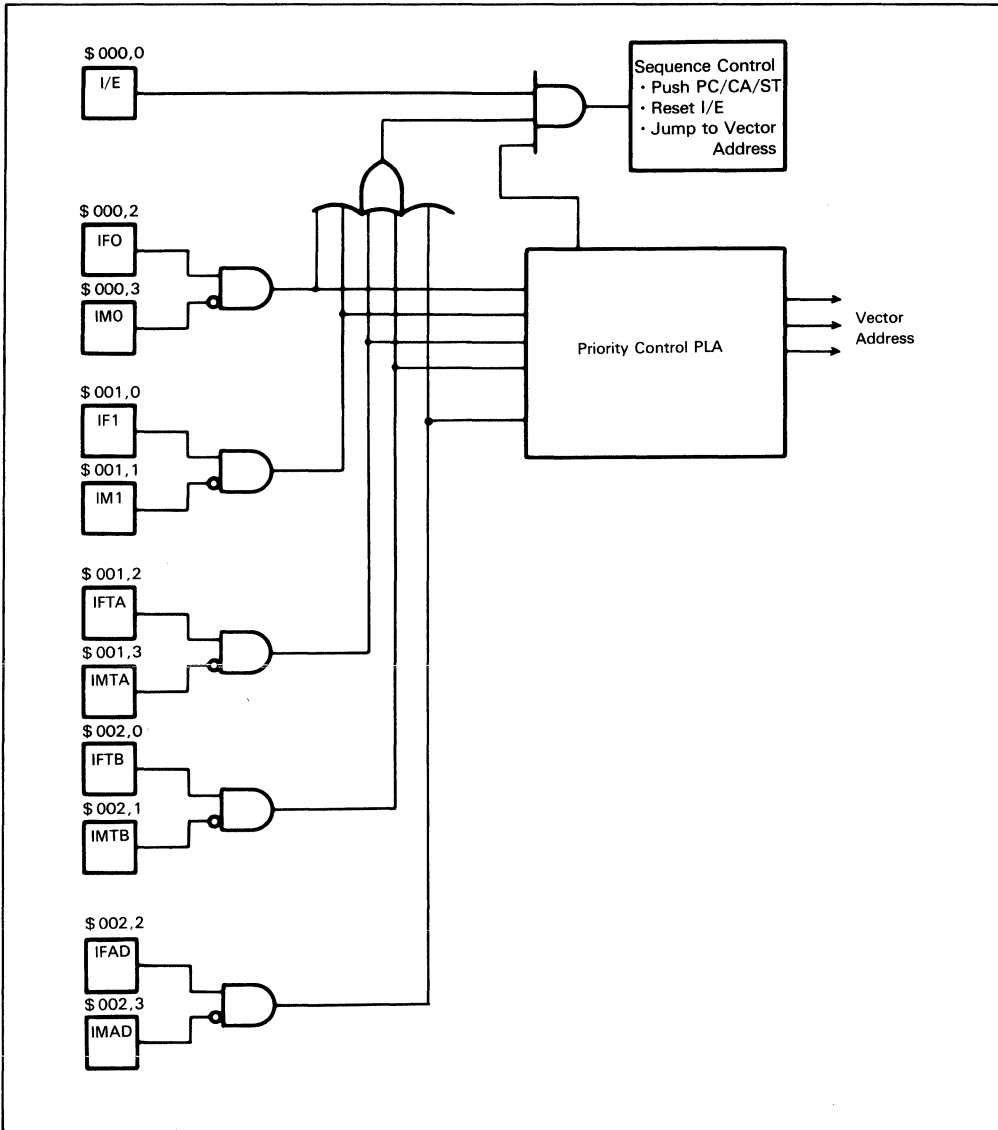


Figure 6. Interrupt Circuit Block Diagram

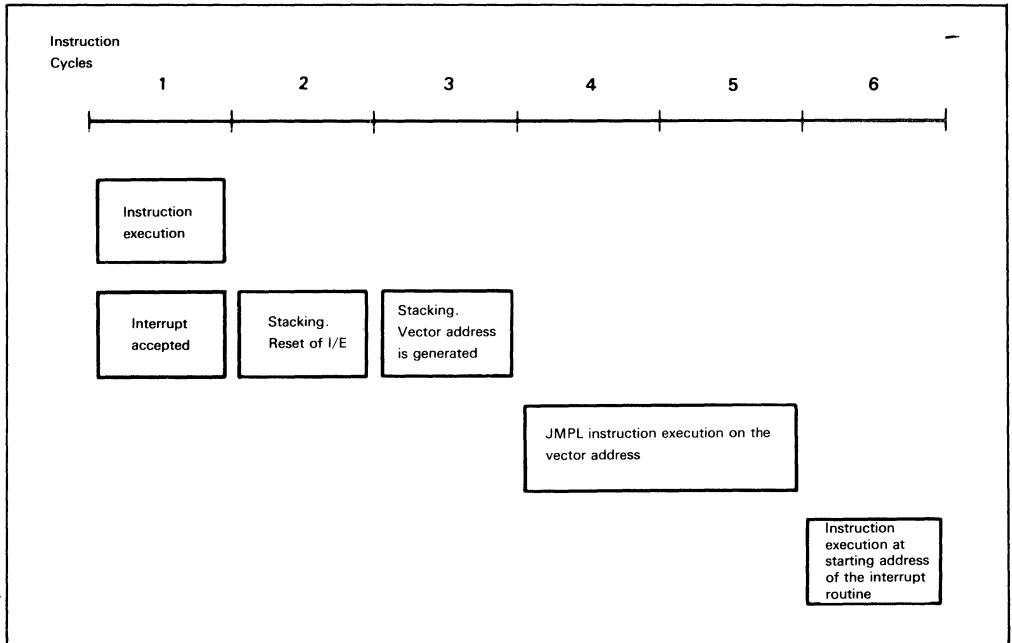


Figure 7. Interrupt Servicing Sequence

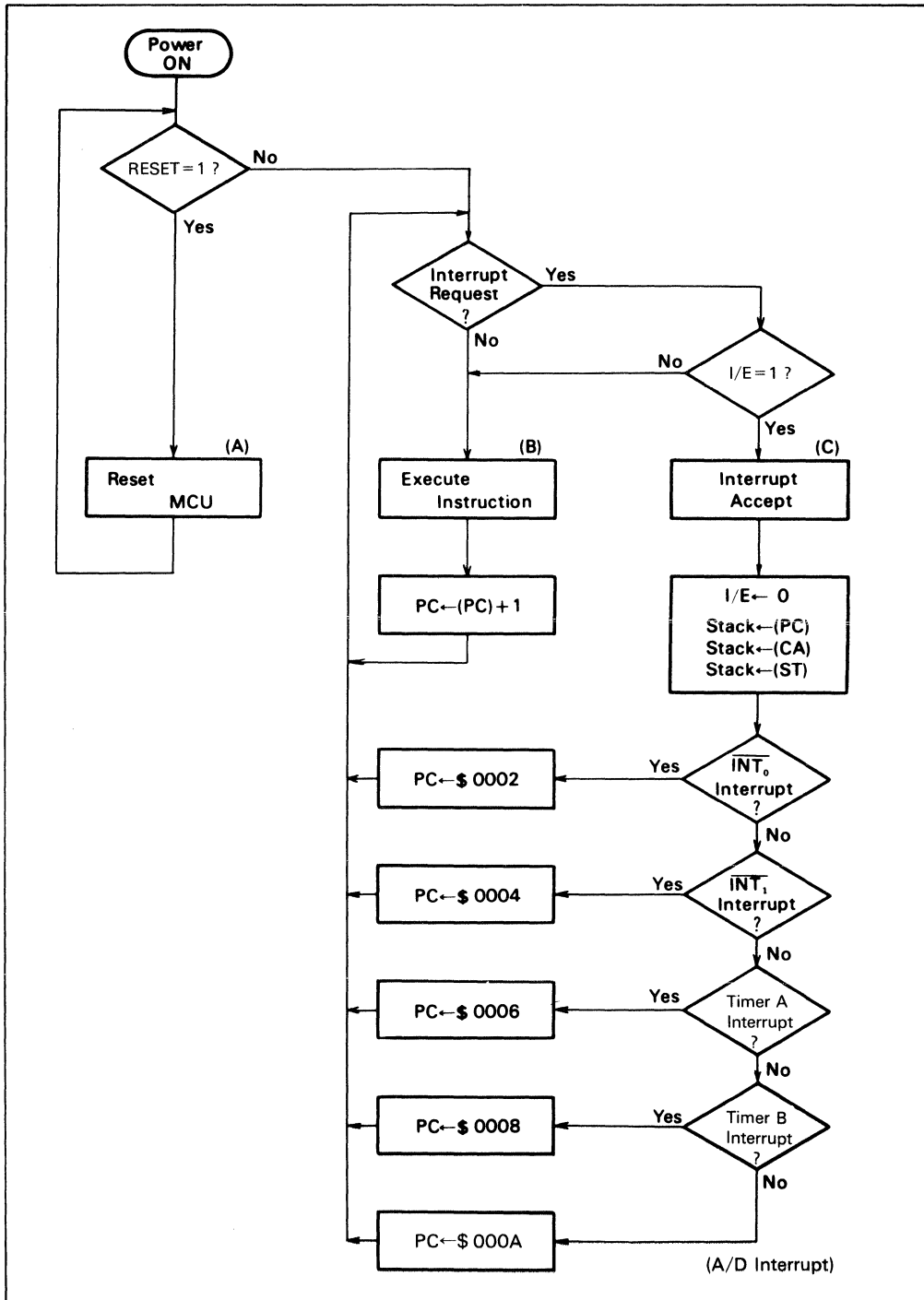


Figure 8. Interrupt Servicing Flowchart



Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMRA: \$004). (Figure 10)

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs.

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 . When using \overline{INT}_1 as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. Figure 9 shows the interrupt mode register.

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 and \overline{INT}_1 inputs respectively. (Figure 9)

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt mask bits mask an interrupt request caused

by the external interrupt request flags. (Figure 9)

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set when an overflow occurs in timer A. (Figure 9)

Timer A Interrupt Mask (IMTA: 001 bit 3): The timer A interrupt mask bit masks an interrupt request caused by the timer A interrupt request flag. (Figure 9)

Timer B interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set when an overflow occurs in timer B. (Figure 9)

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask bit masks an interrupt request caused by the timer B interrupt request flag. (Figure 9)

A/D Interrupt request Flag (IFAD: \$002 bit 2): The A/D interrupt request flag is set when an A/D conversion is completed. (Figure 9)

A/D Interrupt Mask (IMAD: \$002 bit 3): The A/D interrupt mask bit masks an interrupt request caused by the A/D interrupt request flag. (Figure 9)

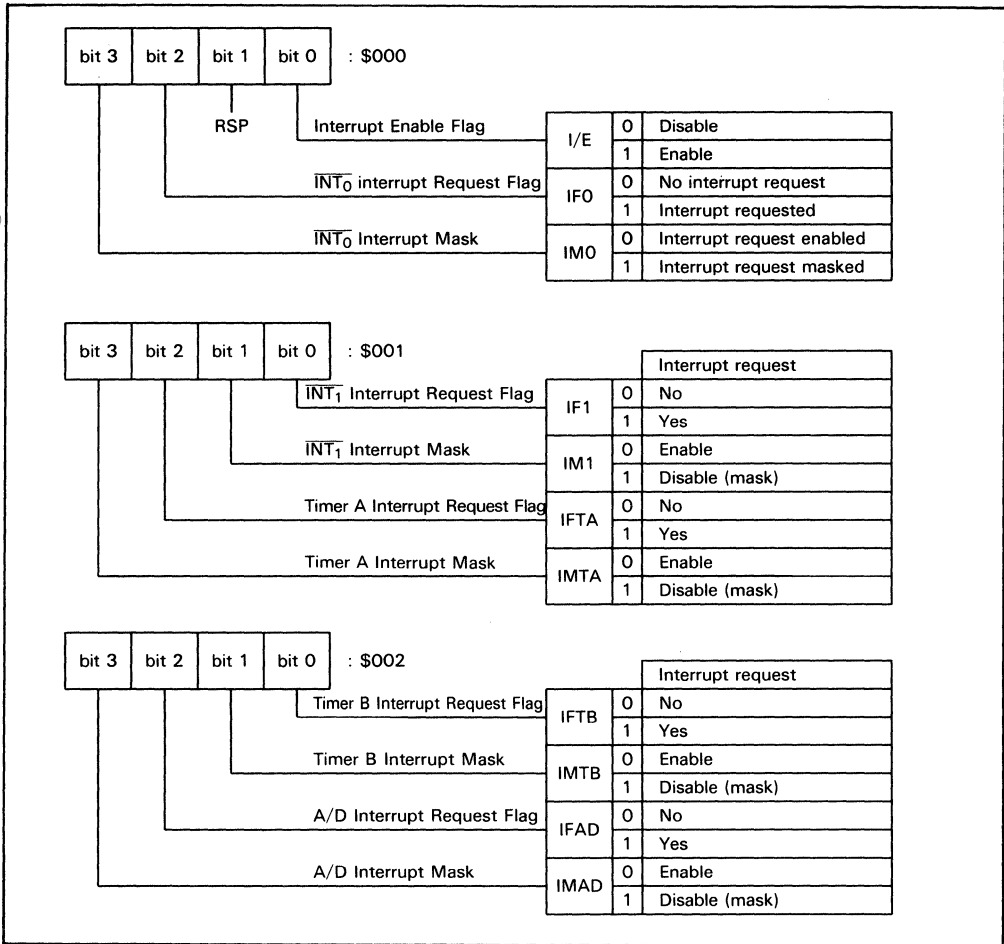


Figure 9. Interrupt Control Bits

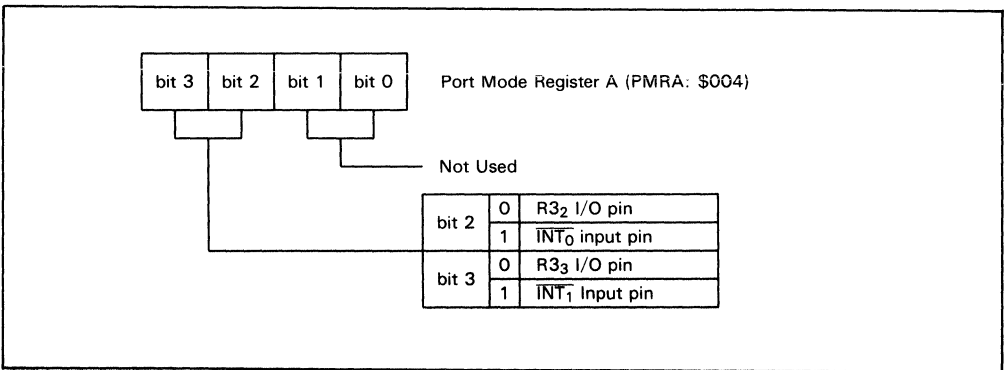


Figure 10. Port Mode Register A

Timer

The MCU contains a prescaler and two timer/counters (timer A, timer B) as shown by the block diagram in figure 11.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset and setting bit 3 of timer mode register A (TMA: \$008) during the watchdog timer ON flag (WDON: \$20, bit 1) is 0, after which the prescaler starts to divide the system clock. It continues operation until MCU reset or stop mode.

Pulse frequency of timer A input clock, timer B input clock, and tone generator outputs (TG₀, TG₁) is selected among prescaler outputs by timer mode register A (TMA: \$008), timer mode register B (TMB: \$009), and port mode register B (PMRB: \$005), respectively.

After MCU reset, WDON is 0. Thus, when timer A is reset by setting bit 3 of timer mode register A (TMA) during the watchdog timer OFF, the prescaler is also reset, which affects the operation of timer B and tone generator outputs (TG₀, TG₁). Consequently, program should be prepared considering the above.

Timer A operation: Timer A is an 8-bit interval timer which can be used also as a watchdog timer. The prescaler divide ratio of timer A is selected by timer mode register A (TMA: \$008).

After timer A is initialized to \$00 by MCU reset and setting bit 3 of timer mode register A (TMA: \$008), it counts up at every clock

input signal. 8 different clock signals divided by the prescaler can be used as an input clock. The clock input signals to timer A are selected by timer mode register A. When the next clock signal is applied after timer A becomes \$FF, it will generate an overflow and reset timer A to \$00. This overflow causes the timer A interrupt request flag (IFTA \$001 bit 2) to go to 1.

This timer can function as a watchdog timer to detect a programming error. The MCU is reset when an overflow output generated from a timer counter cannot be controlled due to a programming error while the watchdog timer ON flag (WDON) is 1.

Timer B operation: Timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When an external event input is used as an input clock signal to timer B, select R₃ /INT₁ as INT₁ by setting the port mode register (PMRA: \$004), and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of the timer load register. If it is not selected, timer B is reset to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

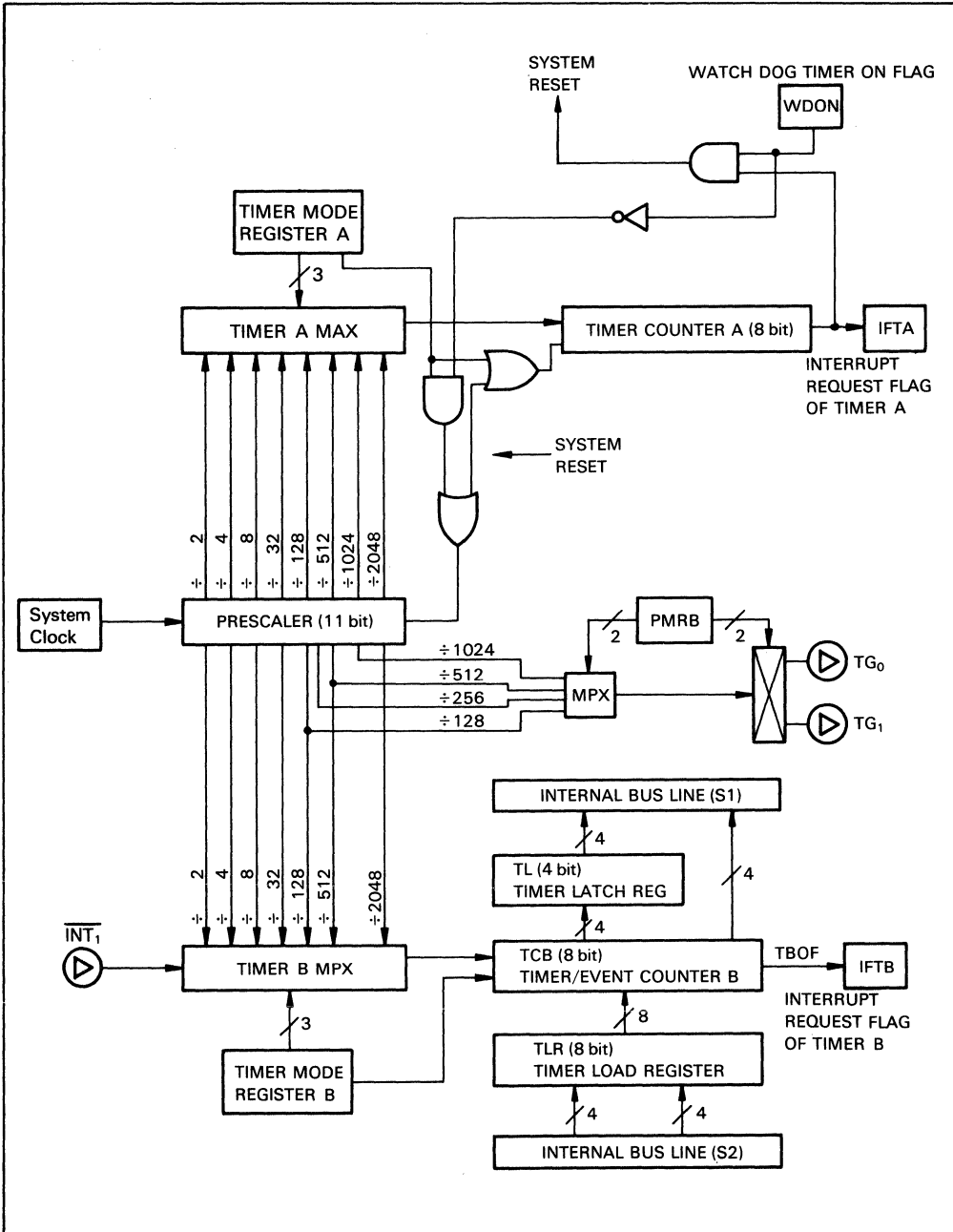


Figure 11. Timer A/Timer B Block Diagram

Timer mode register A (TMA: \$008): Timer mode register A is a 4-bit write-only register. Bits 0 to 2 of TMA control the prescaler divide ratio of timer counter A clock input, as shown in Figure 12. Bit 3 resets timer A when set to 1; while WDON = 0, the pres-

caler is also reset. Bit 3 stays 1 only for one instruction cycle.

Timer mode register A can be modified from the second instruction cycle of the write instruction for timer mode register A.

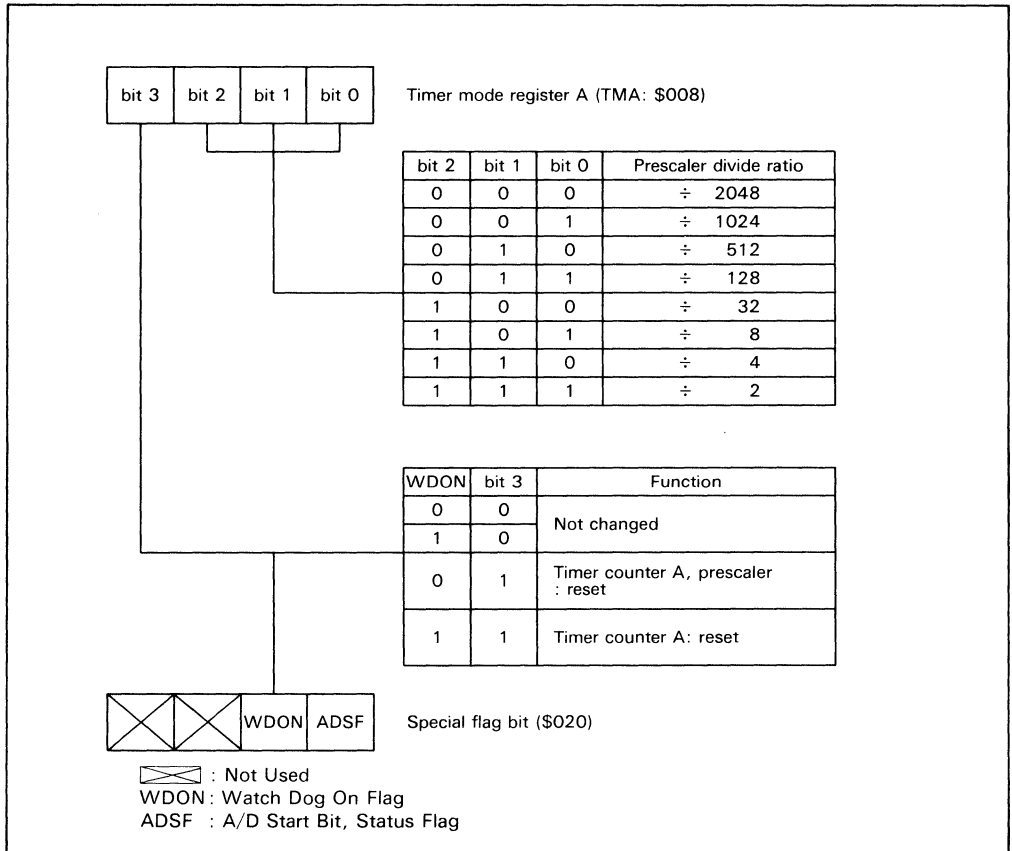


Figure 12. Timer Mode Register A Configuration

Timer mode register B (TMB: \$009): Timer mode register B is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in Figure 13. Timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B can be modified from the second instruction cycle after timer mode register B is written to. Initialization of timer B by a write to the timer load register should be performed after the contents of timer mode register B have been appropriately changed.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit

read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

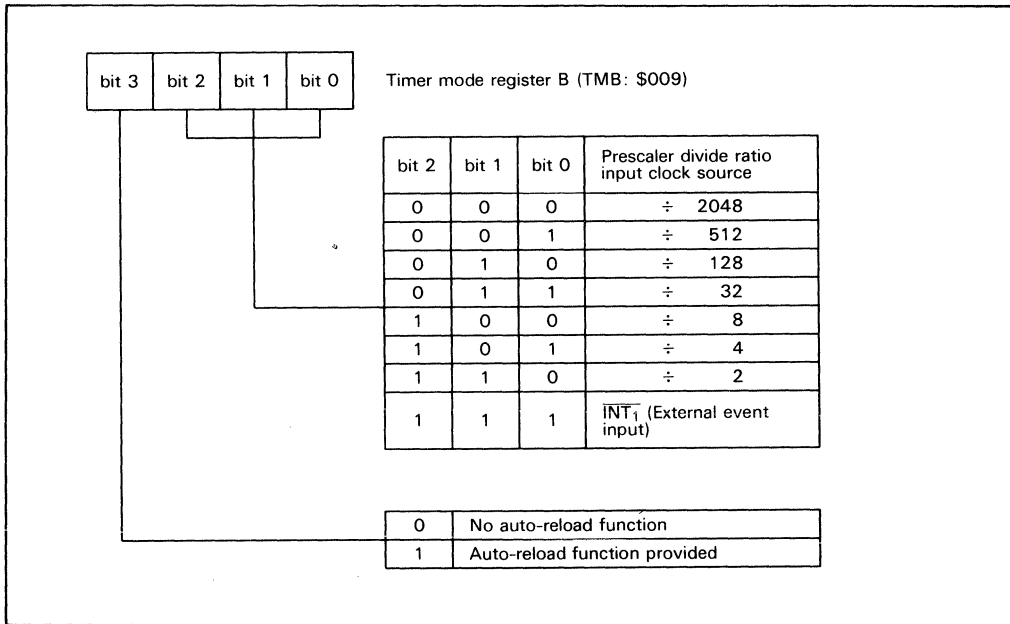


Figure 13. Timer Mode Register B Configuration

Timer A Interrupt Request Flag (IFTA: \$001, bit 2): The timer A interrupt request flag is set by the overflow output of timer A. When watchdog timer function is selected, the timer interrupt request flag is not set since the MCU is reset by an overflow output. (Figure 14)

Timer A Interrupt Mask (IMTA: \$001, bit 3): The timer A interrupt mask prevents an interrupt request from being generated by

timer A interrupt request flag. (Figure 14)

Timer B Interrupt Request Flag (IFTB: \$002, bit 0): The timer B interrupt request flag is set by the overflow output of timer B. (Figure 14)

Timer B Interrupt Mask (IMTB: \$002, bit 1): The timer B interrupt mask prevents an interrupt request from being generated by the timer B interrupt request flag. (Figure 14)

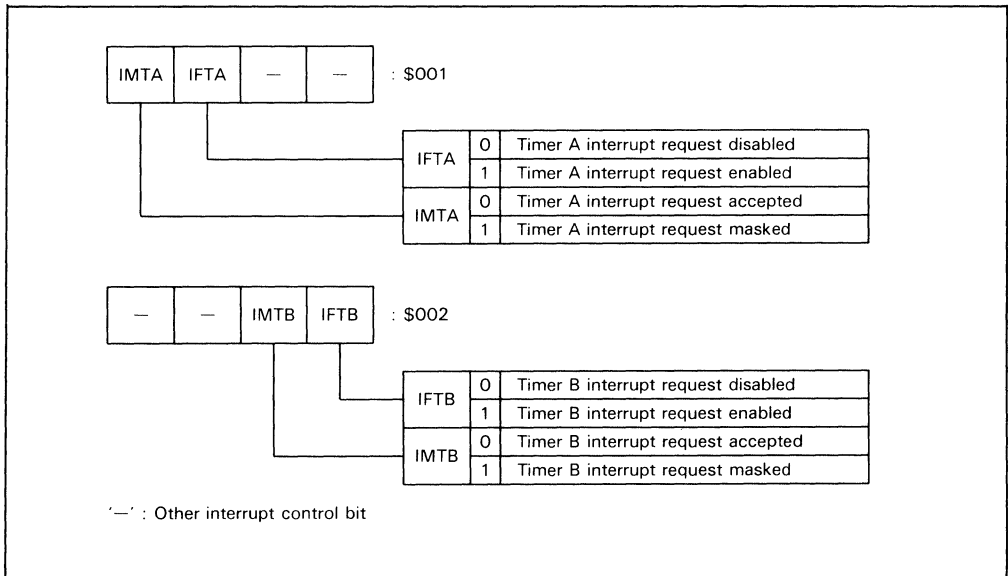


Figure 14. Timer Interrupt Control Bits

A/D Converter

The HD404302 and HD4074308 incorporate a sequential comparison system A/D converter having a resistor ladder. It can measure four analog inputs with 8-bit resolution. Figure 15 shows the A/D converter block diagram. The A/D converter consists of the following registers:

- A/D mode register (4 bits)
- A/D start bit, status flag (1 bit)
- A/D port select register (4 bits)
- A/D data register (4 bits + 4 bits)

A/D Mode Register (AMR): The A/D mode register is a 4-bit write-only register which selects A/D conversion speed (Bit 0, Bit 1) and analog input channel (Bit 2, Bit 3). (Figure 16)

A/D Start Bit, Status Flag (ADSF): A/D conversion is started when 1 is written to the A/D start bit. After a conversion is completed, conversion data is set in the A/D data register, and the A/D start bit is cleared at the same time. (Figure 16)

(Note that the bit manipulation instruction SEM or SEMD should be used to write data to ADSF. During A/D conversion, ADSF must not be written to.)

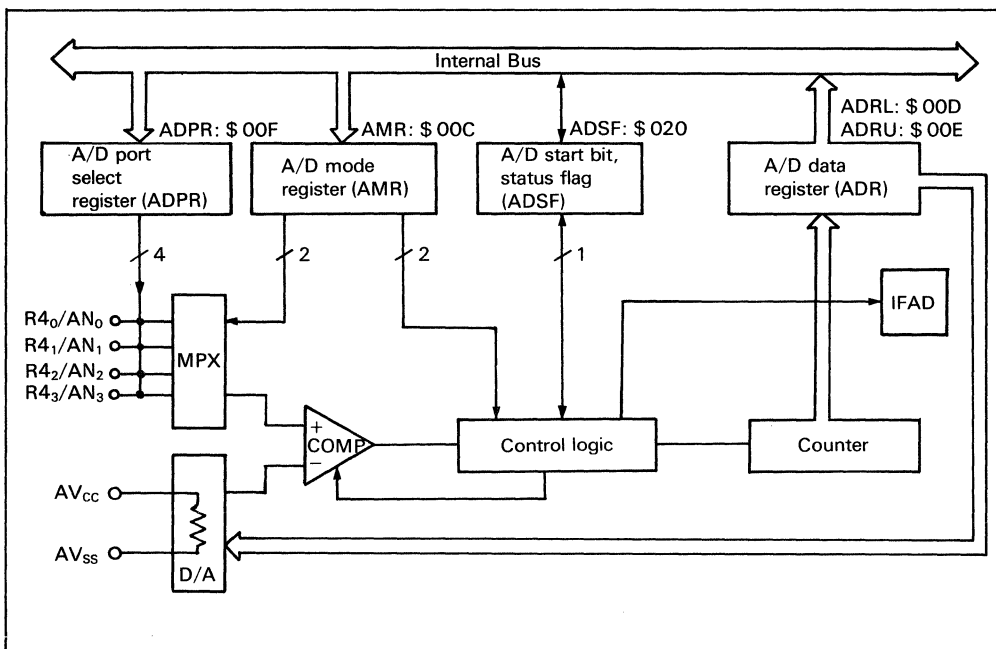


Figure 15. A/D Converter Block Diagram

A/D Port Select Register (ADPR): The A/D port select register is a write-only register

which selects the digital port and analog port. (Figure 16)

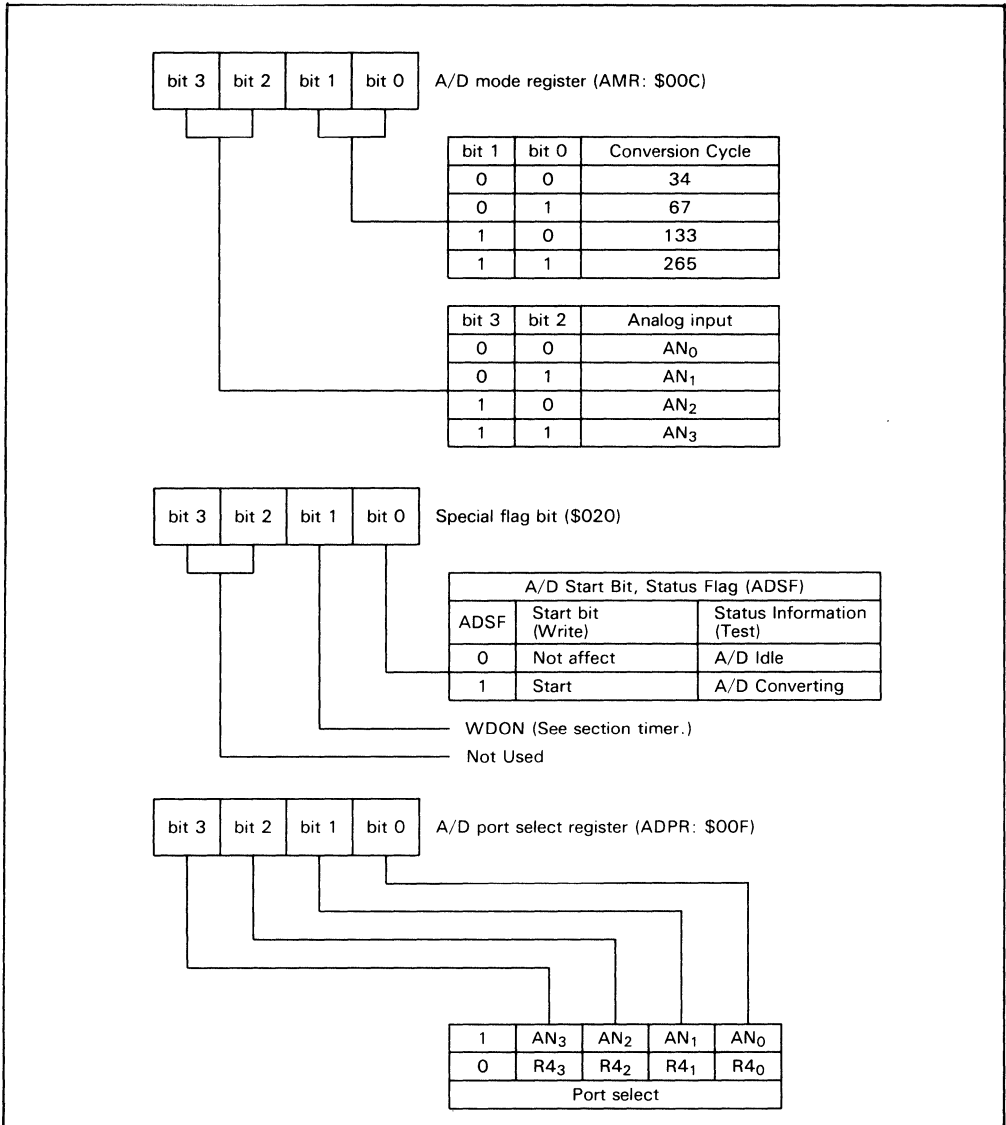


Figure 16. A/D Register Configuration

A/D Data Register (ADRL: \$00D, ADRU: \$00E): The A/D data register is a 4-bit/4-bit read-only register in which the 8-bit conversion result is set after completing A/D conversion. The data is preserved until the next conversion begins. Data read is not guaranteed during A/D conversion. The A/D data register is initialized to \$80 by the MCU reset. (Figure 17)

Precautions on using the A/D converter:

- If a digital signal is input to the R4₀-R4₃ or adjacent pins during A/D conversion, conversion accuracy may be affected.
- Data in the A/D data register is not guaranteed during A/D conversion.
- Port output instructions should not be executed during A/D conversion to allow the A/D converter to operate stably.

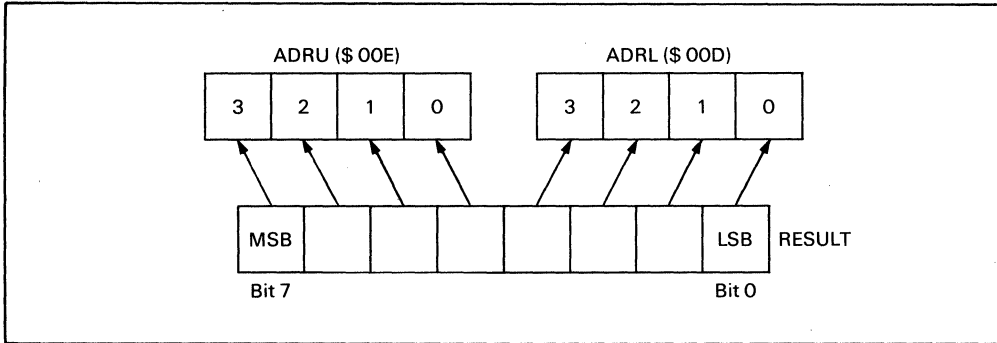


Figure 17. A/D Data Register Configuration

Input/output

The MCU has 33 I/O pins. 25 pins of them are high-voltage pins. On and off of output buffer of the standard pins are controlled by combination of the value of the port register (PDR) and data control register (DCR). (Figure 19)

D Port: The D port is an I/O port which has 13 discrete I/O pins, each of which can be addressed independently. It can be tested through SED/TDD and SEDD/REDD instructions. D₁₁ and D₁₂ ports are multiplexed with the tone generator pins TG₀, TG₁, respectively. The circuit type of the D port is shown in Table 3.

R Ports: The R ports are composed of 20 I/O pins and one 4-bit input-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU will not be affected by writing into the input-only and non-existing ports. On and off of output buffer of the R3 and R4 ports are controlled by the R port data control register (DCR3, DCR4). R₃₂ and R₃₃ are multiplexed with $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$, respectively. R₄₀, R₄₁, R₄₂, and R₄₃ pins are multiplexed with AN₀,

AN₁, AN₂, and AN₃, respectively. The circuit type of the R port is shown in table 3.

Port Mode Register (PMRA: \$004, PMRB: \$005): The port mode register is a 4-bit write-only register which controls the R₃₂/ $\overline{\text{INT}}_0$ pin, R₃₃/ $\overline{\text{INT}}_1$ pin, D₁₁/TG₀ pin, and D₁₂/TG₁ pin as shown in Figure 18. The port mode register is initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent malfunction.

If without pull-down MOS (PMOS open drain) is selected for high-voltage pins, connect to V_{CC} on the printed circuit board.

If without pull-up MOS is selected for standard pins, connect to GND on the printed circuit board.

The contents of PDR and DCR of the corresponding pin should be remained as the same as in reset state by program. The corresponding pin should not be used as peripheral function I/O pin.

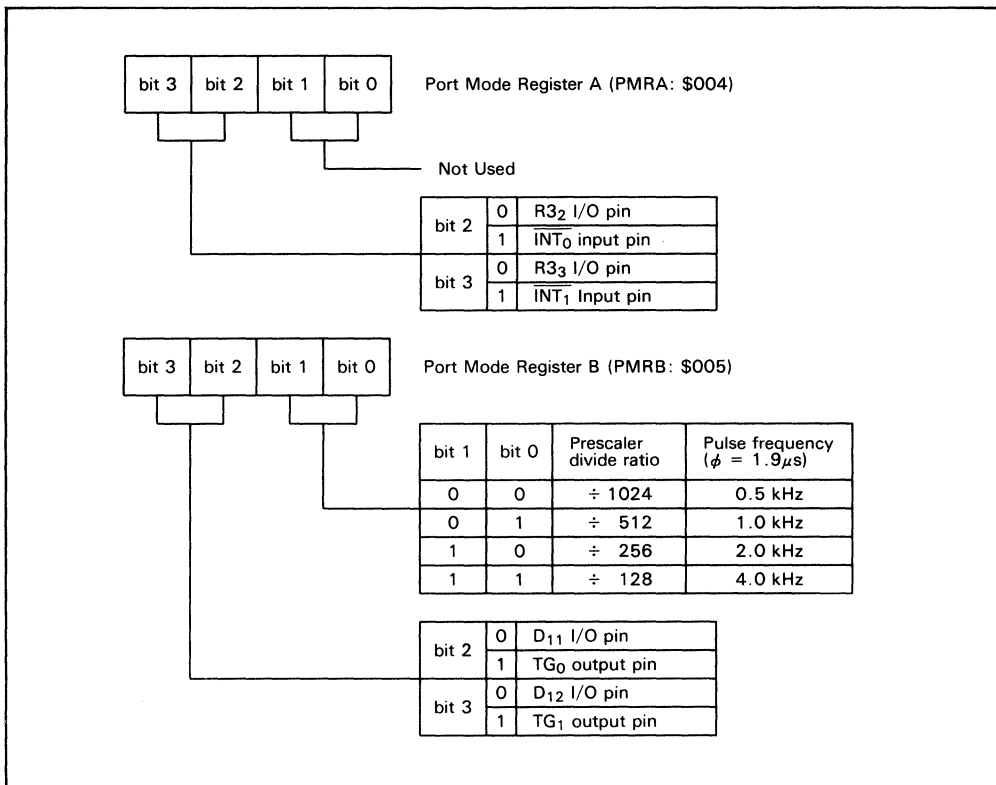


Figure 18. Port Mode Register Functions

Table 3. I/O Pin Circuit Types

		With pull-up MOS (B)	Without pull-up MOS (C)	Applicable pins
Standard pins	I/O common pins			R3 ₀ ~R3 ₃
		<p>Note: Cannot be used (AN₀-AN₃) as an analog input pin.</p>		R4 ₀ ~R4 ₃
	Input pins			$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$

Table 3. I/O Pin Circuit Types (cont.)

		Without pull-down MOS (D)	With pull-down MOS (E)	Applicable pins
High-voltage pins	I/O common pins			D ₀ ~D ₁₂ R ₀₀ ~R ₀₃ R ₁₀ ~R ₁₃ R ₂₀ ~R ₂₃
	Input pins			RA ₁

Note: In the stop mode, MCU becomes reset state and peripheral function cannot be selected, and HLT signal is 1 and I/O pins are in high impedance state.

Circuit type / Product type	B	C	D	E
	Mask ROM type HD404302	option		
ZTAT type HD4074308	X	fixed		X

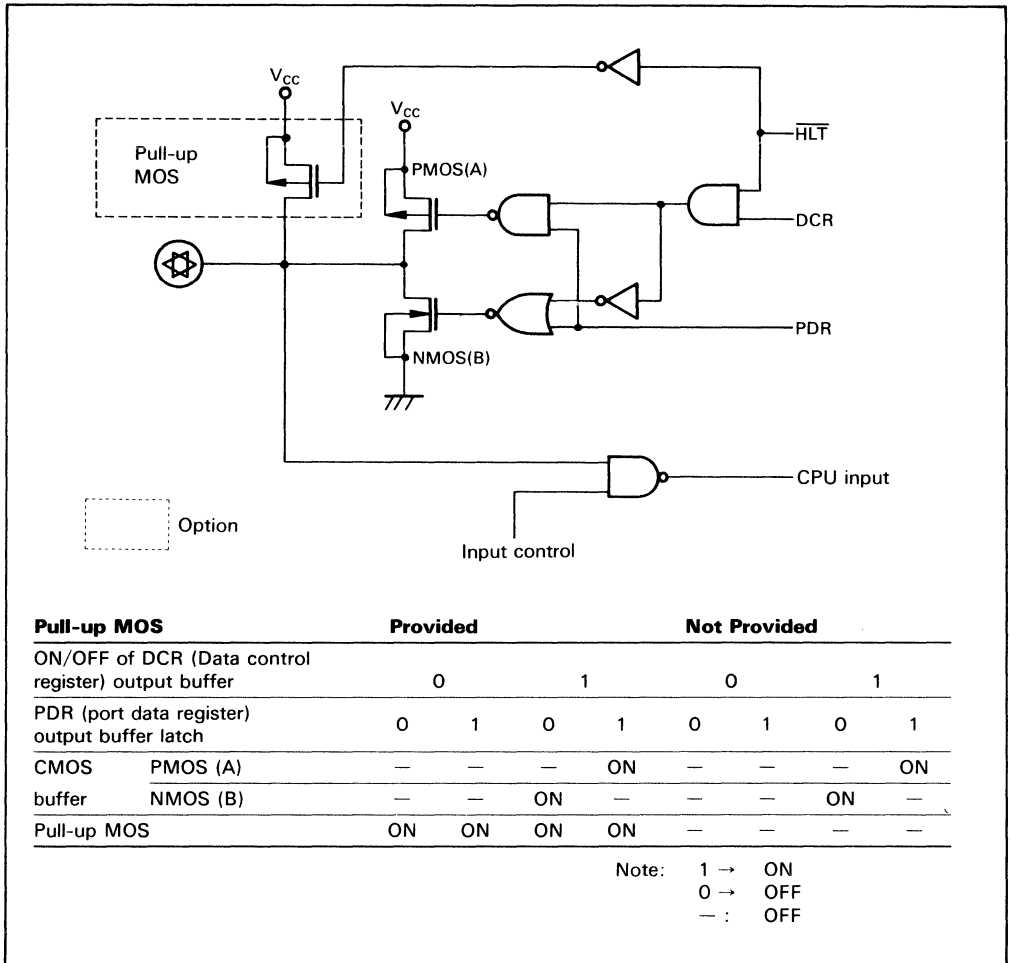


Figure 19. I/O Buffer Configuration (Standard pins)

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two

instructions cycles are required for the MCU to be reset.

Table 4 shows the parts initialized by MCU reset and the status of each after the reset has been carried out.

Table 4. Initial Value after MCU Reset

Item		Initial value after MCU reset	Contents
Program counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable branch with conditional instructions
Stack pointer (SP)		\$3FF	Stack level is 0
I/O	High-voltage pin port data register (PDR)	All bits are 0	Enable to output 0
	Standard pin port data register (PDR)	All bits are 1	Enable to output 1
	Data control register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port mode register A (PMRA)	0000	See section port mode register A.
	Port mode register B (PMRB)	0000	See section port mode register B.
Interrupt flag/mask	Interrupt enable flag (I/E)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode register	Timer mode register A (TMA)	0000	See section timer mode register A.
	Timer mode register B (TMB)	0000	See section timer mode register B.
Timer/counter	Timer counter	\$00	—
	Timer/event counter B (TCB)	\$00	—
	Timer load register (TLR)	\$00	—
	Prescaler	\$000	—
A/D	A/D port select register (ADPR)	0000	See section A/D port select register
	A/D mode register (AMR)	0000	See section A/D mode register
	A/D data register (ADR)	\$80	See section A/D data register
	A/D start bit, status flag (ADSF)	0	See section A/D start bit, status flag
Bit register	Watch dog timer on flag (WDON)	0	See section Timer A

Note: Registers and flags except above become as follows after MCU reset.

Internal Oscillator Circuit

In addition, see Figure 21 for the layout of the crystal or ceramic filter. In all cases, external clock operation is available.

Figure 20 outlines the internal oscillator circuit. Refer to Table 5 for selection of the type.

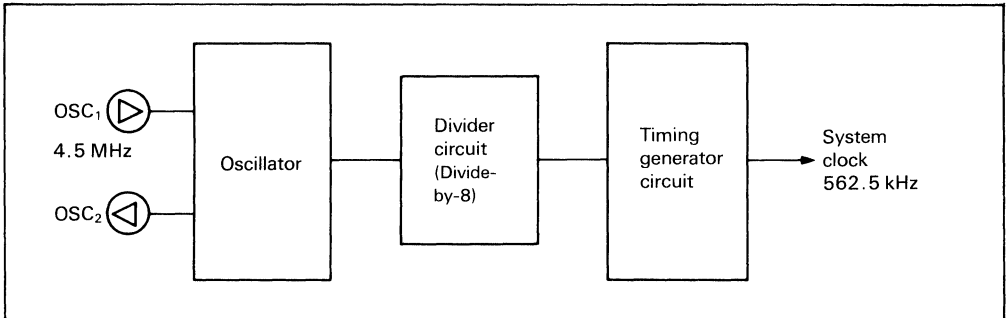


Figure 20. Internal Oscillator Circuit

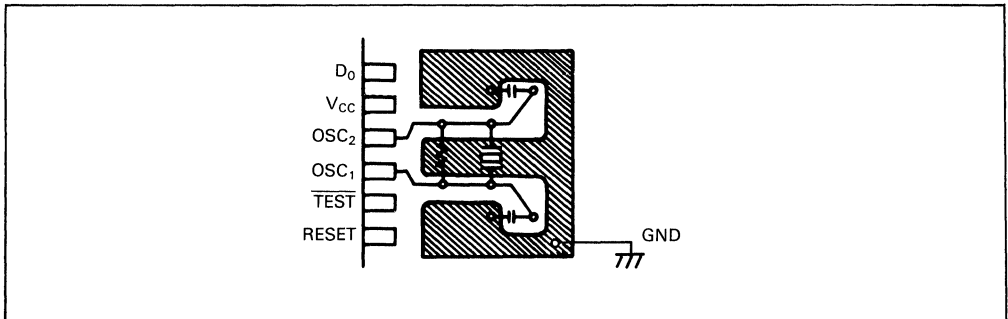
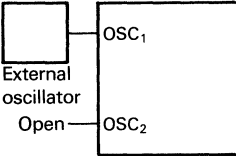
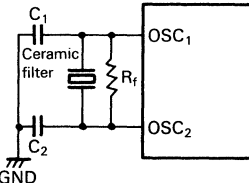
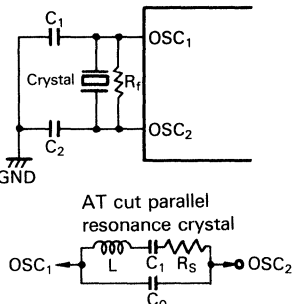


Figure 21. Layout of Crystal and Ceramic Filter

Table 4. Initial Value after MCU Reset (cont.)

Items	After recovering from STOP mode by MCU reset	After all other MCU reset
Carry (CA)	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.
Accumulator (A)		
B register (B)		
W register (W)		
X/SPX register (X/SPX)		
Y/SPY register (Y/SPY)		
A/D data register (ADRL, ADRU)		
RAM	The contents of RAM just before MCU reset (just before STOP instruction) are retained.	

Table 5. Example of Oscillator Circuits

	Circuit configuration	Circuit constant
<p>External clock operation</p>	 <p>External oscillator Open</p>	<p>TBD</p>
<p>Ceramic filter oscillator</p>	 <p>C₁ Ceramic filter C₂ GND R_f OSC₁ OSC₂</p>	<p>Ceramic filter: TBD</p> <p>R_f : } C₁ : } TBD C₂ : }</p>
<p>Crystal oscillator</p>	 <p>C₁ Crystal C₂ GND R_f OSC₁ OSC₂</p> <p>AT cut parallel resonance crystal</p> <p>OSC₁ → L → C₁ → R_S → OSC₂ C₀</p>	<p>R_f : } C₁ : } TBD C₂ : }</p> <p>Crystal: equivalent to circuit shown</p> <p>C₀ : } R_S : } TBD f : }</p>

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator, and the floating capacitance in designing the board. In employing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring between OSC₁, OSC₂ and elements should be as short as possible, and never cross the other wires. Refer to the layout of crystal and ceramic filter (figure 21).

Low Power Dissipation Mode

The MCU has two low power dissipation

modes, standby mode and stop mode (table 6). Figure 22 is a mode transition diagram for these modes.

Table 6. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, Flag	Retained	Reset (Note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/Output pins	Retained (Note 2)	High impedance
Timer/Counter	Active	Stopped
A/D	Active	Stopped
Recovery method	RESET input, Interrupt request	RESET input

- Notes:
1. The MCU recovers from stop mode by RESET input. Refer to table 4 for the contents of flags and registers.
 2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

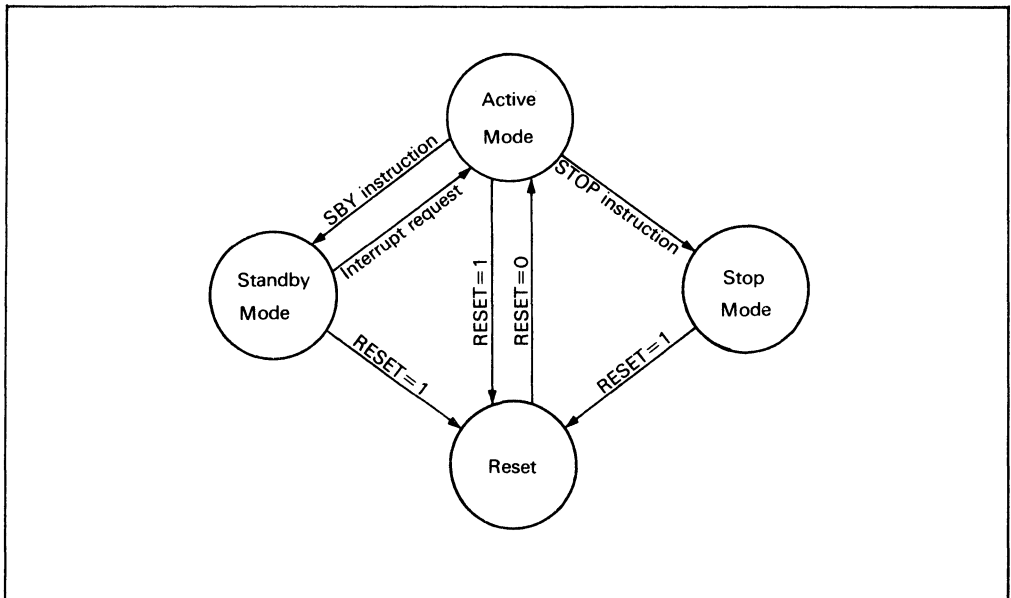


Figure 22. MCU Operation Mode Transition

Standby Mode: Executing an SBY instruction puts the MCU into standby mode. In standby mode, the oscillator circuit continue working and the timer/counter, A/D, and interrupts are active. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM and I/O pins retain the state they were in just before the MCU went into standby mode.

In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Standby Mode may be cancelled by inputting RESET or by asserting an interrupt request.

Figure 23 shows the flowchart of the standby mode.

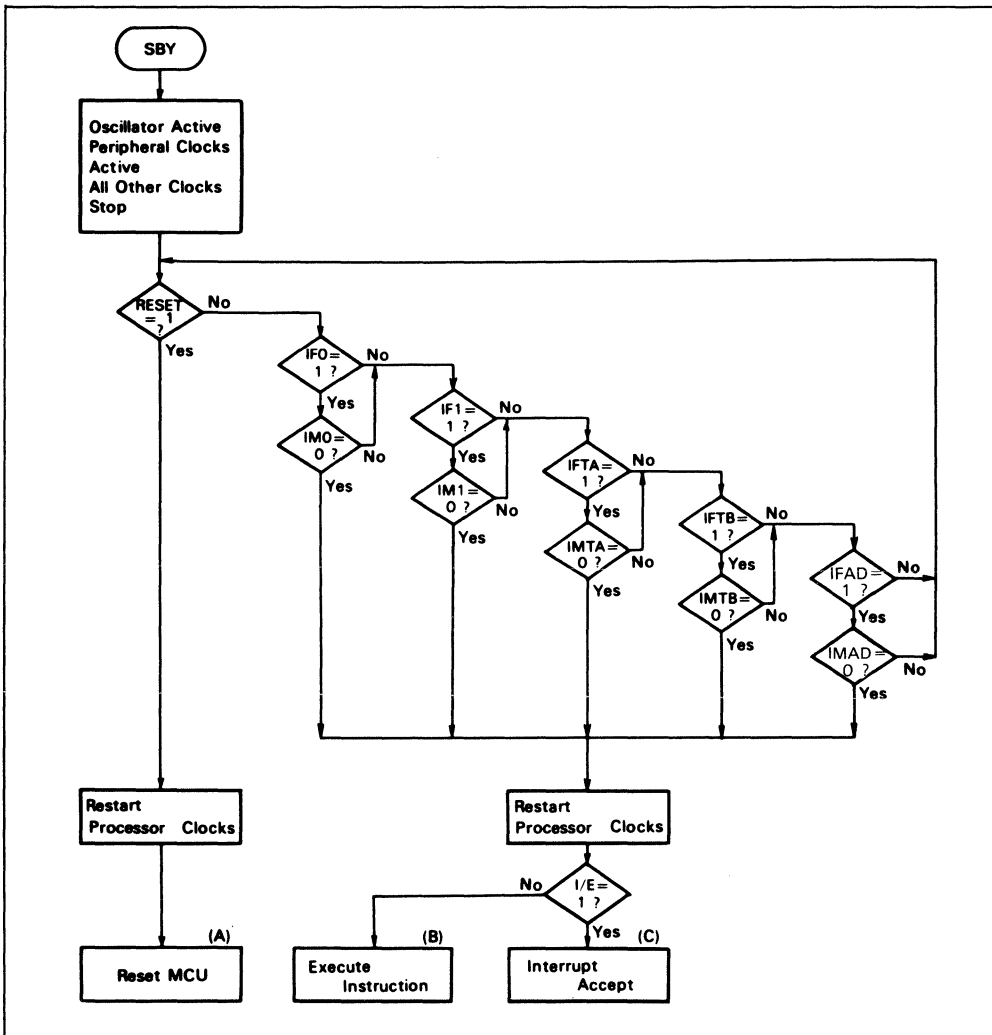


Figure 23. MCU Operating Flowchart



Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop Mode may be cancelled by resetting the MCU. At this time, as shown in Figure 24, reset input must be applied at least to t_{RC} for

oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry, and A/D data register may not retain their contents.

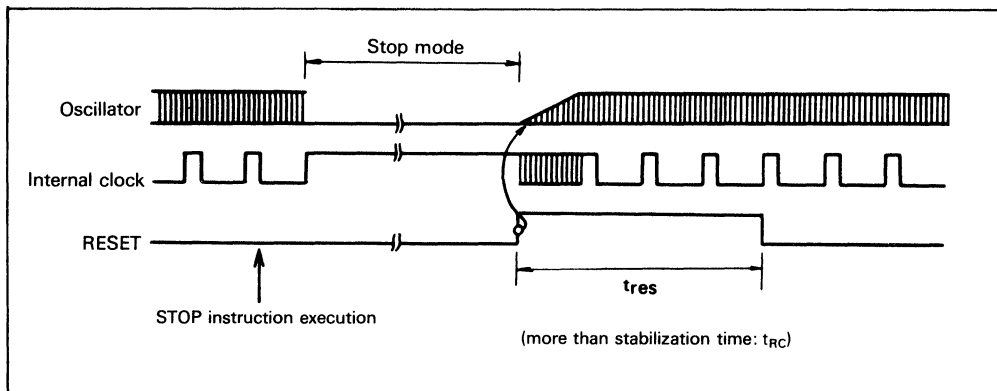


Figure 24. Timing Chart of Recovering from Stop Mode

PROM Mode Pin Description

Pin No.	MCU mode		PROM mode		Pin No.	MCU mode		PROM mode	
	Pin name	I/O	Pin name	I/O		Pin name	I/O	Pin name	I/O
1	D ₁₀	I/O	M ₂	I	22	AV _{CC}		V _{CC}	
2	D ₁₁ /TG ₀	I/O	V _{CC}		23	R ₄₀ /AN ₀	I/O	O ₄	I/O
3	D ₁₂ /TG ₁	I/O	V _{CC}		24	R ₄₁ /AN ₁	I/O	O ₅	I/O
4	RA ₁ /V _{disp}	I			25	R ₄₂ /AN ₂	I/O	O ₆	I/O
5	RO ₀	I/O	A ₁	I	26	R ₄₃ /AN ₃	I/O	O ₇	I/O
6	RO ₁	I/O	A ₂	I	27	AV _{SS}		GND	
7	RO ₂	I/O	A ₃	I	28	RESET	I	V _{PP}	
8	RO ₃	I/O	A ₄	I	29	TEST	I	TEST	I
9	R ₁₀	I/O	A ₅	I	30	OSC1	I		
10	R ₁₁	I/O	A ₆	I	31	OSC2	O	V _{CC}	
11	R ₁₂	I/O	A ₇	I	32	V _{CC}		V _{CC}	
12	R ₁₃	I/O	A ₈	I	33	D ₀	I/O	M ₀	I
13	R ₂₀	I/O	A ₀	I	34	D ₁	I/O	M ₁	I
14	R ₂₁	I/O	A ₁₀	I	35	D ₂	I/O	A ₉	I
15	R ₂₂	I/O	A ₁₁	I	36	D ₃	I/O		
16	R ₂₃	I/O	A ₁₂	I	37	D ₄	I/O	A ₁₃	I
17	R ₃₀	I/O	O ₀	I/O	38	D ₅	I/O	A ₁₄	I
18	R ₃₁	I/O	O ₁	I/O	39	D ₆	I/O	CE	I
19	R ₃₂ /INT ₀	I/O	O ₂	I/O	40	D ₇	I/O	OE	I
20	R ₃₃ /INT ₁	I/O	O ₃	I/O	41	D ₈	I/O		
21	GND		GND		42	D ₉	I/O		

Note: I/O: Input/Output pin I: Input pin O: Output pin
 The V_{CC} and GND pins in PROM mode must supply V_{CC} and GND levels to all V_{CC} and GND pins.

Pins for PROM Mode (HD4074308)

Figure 25 shows pin arrangement is PROM mode.

V_{PP}

Apply the programming voltage (12.5 V ± 0.3 V) to V_{PP}.

CE

$\overline{\text{CE}}$ inputs the control signal to enable PROM programming and verify.

OE

$\overline{\text{OE}}$ inputs the data output control signal for verify.

A₀-A₁₄

These pins are address input pins of the internal PROM.

O₀-O₇

Data bus input pins of the internal PROM.

M₀, M₁, M₂

These pins are used to set PROM mode. The MCU is set to the PROM mode by pulling AV_{SS} and $\overline{\text{TEST}}$ low, and RESET, M₀, M₁, M₂, and AV_{CC} high.

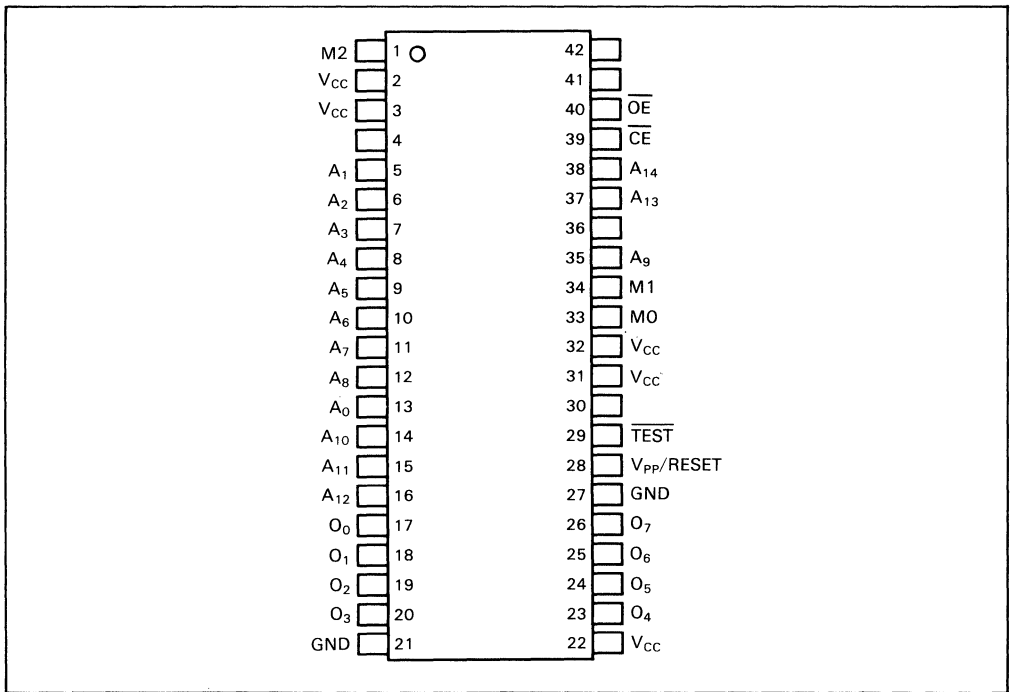


Figure 25. Pin Arrangement is PROM Mode

Programmable ROM (HD4074308)

The MCU on-chip PROM is programmed in PROM mode (figures 26, 27). PROM mode is set by bringing TEST low, and RESET, M₀, M₁, M₂ high as shown in figure 26. In PROM mode, the MCU does not operate. Table 7 shows the PROM mode selection. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 42-to-28-pin socket adapter. Table 8 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series MCU incorporates a conversion circuit to enable use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits, as shown in figure 27. For example, if 8 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 7 shows how programming and verification modes are selected.

Figure 28 is a programming flowchart.

Erasing

PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are: ultraviolet (UV) light with wavelength 2537Å with a minimum irradiation of 15W·sec/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Table 7. PROM Mode Selection

Mode	Pin			
	CE	OE	V _{PP}	O ₀ -O ₇
Programming	Low	High	V _{PP}	Data input
Verify	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance

Table 8. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter	
Maker	Type Name	Maker	Type Name
DATA I/O	22B 29B	Hitachi	TBD
AVAL Corp	PKW-7000 PKW-1000	Hitachi	TBD



Precautions

1. Addresses \$0000 to \$3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.) Data in unused addresses must be set to \$FF.
2. Be sure that the PROM programmer,

socket adapter and LSI lineup (pin 1 positions match). Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI (table 8). Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.

3. The PROM should be programmed with $V_{PP} = 12.5$ V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP} .

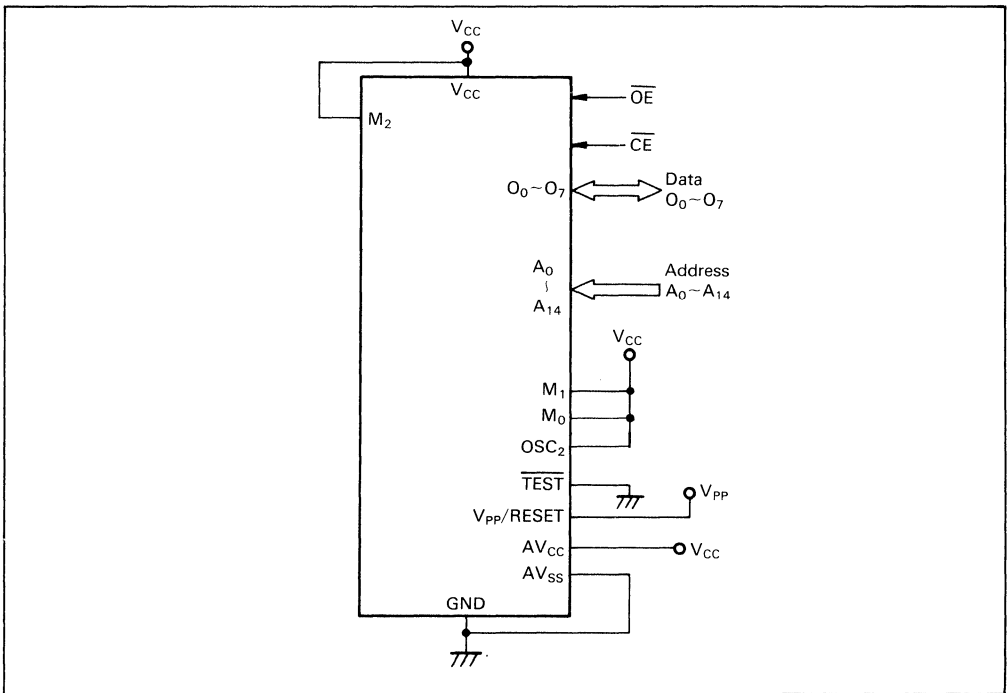


Figure 26. PROM Mode

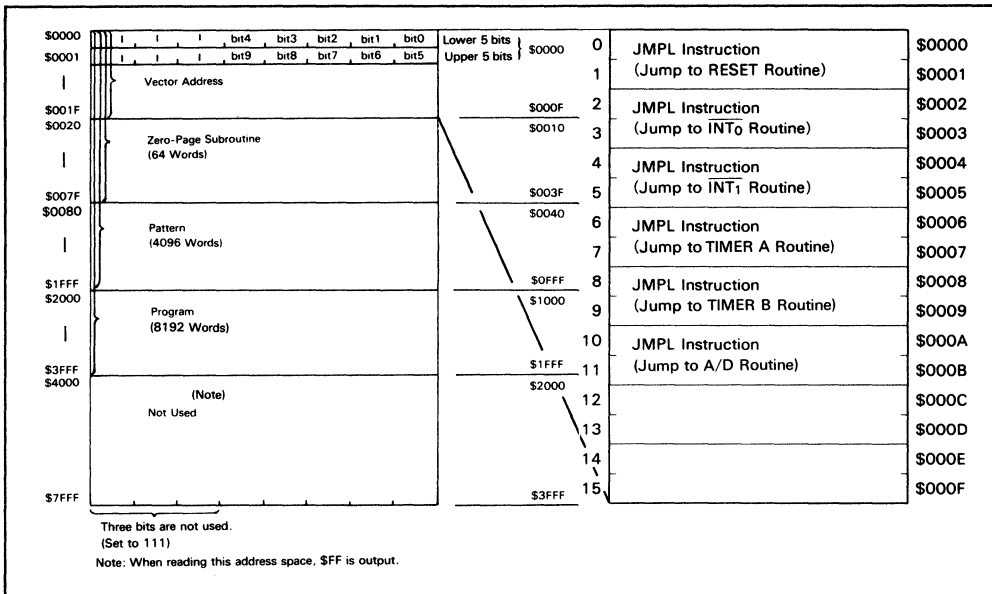


Figure 27. PROM Mode Memory Map

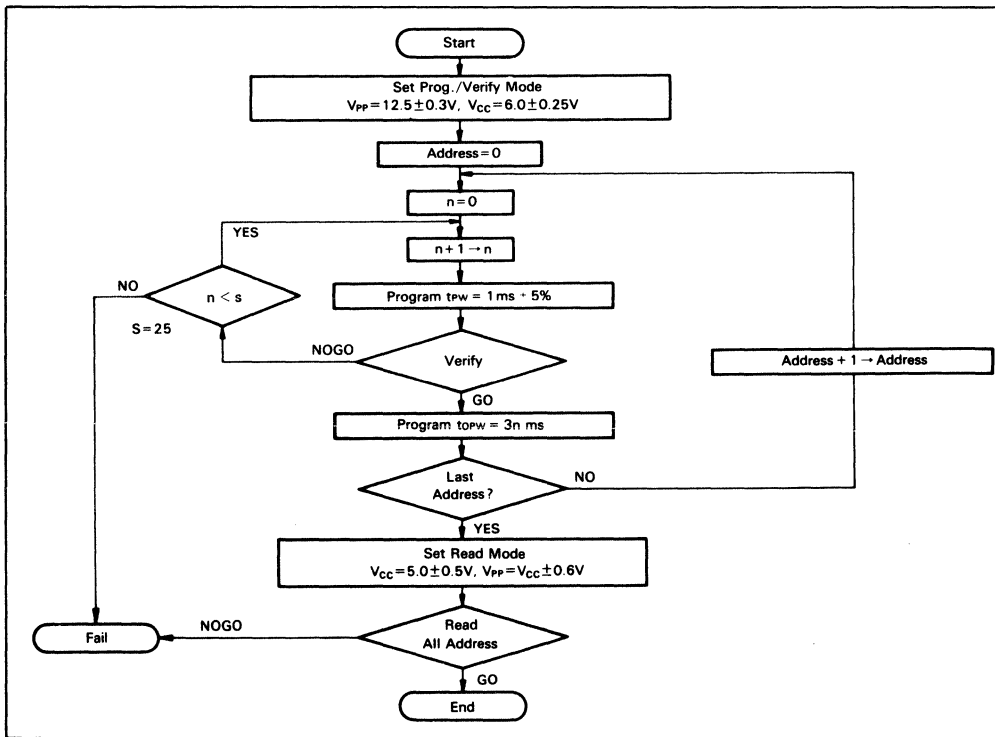


Figure 28. A Sequence of High-Speed Programming Flowchart



ZTAT MCU On-Chip PROM Characteristics and Precautions

Principles of Programming/Erasing: The ZTAT micros' memory cells are the same as an EPROM's. Therefore they are programmed by applying high voltage to control gates and drains, which injects hot electrons into the floating gate. They are stable, surrounded by an energy barrier of SiO₂ film. Such a cell becomes a 0 bit due to the memory threshold voltage change. A cell with no condensed electrons at its floating gate appears as a 1 bit (figure 29).

The electron charge in memory cells may

decrease as time goes by. This can be caused by:

- Ultraviolet light: discharged by photo-emitted electrons (erasure principle)
- Heat: discharged by thermal emitted electrons
- High voltage: discharged by a high electric field at the control gate or drain

If the oxide film covering a floating gate is defective, the erasure rate is great. Normally, electron erasure does not occur, because such defective devices are found and removed during testing.

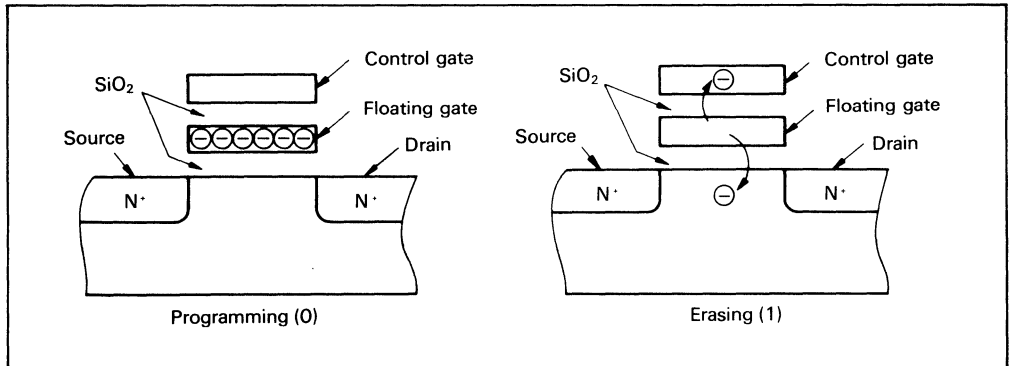


Figure 29. Cross-section of EPROM Memory Cell

Programming Precautions: The EPROM memory cells should be programmed under specific voltage and timing conditions. The higher the program voltage and the longer the program pulse is applied, the more electrons will be injected into the floating gate. However, if an overvoltage is applied to V_{PP} , the p-n junction may be permanently damaged. Pay particular attention to PROM programmer overshoot. Negative voltage noise will cause a parasitic transistor effect, which may reduce break-down voltage.

The ZTAT micros are connected electrically to the PROM programmer through a socket adapter. Therefore, pay attention to the following:

- Confirm that the socket adapter is firmly

fixed on the PROM programmer.

- Do not touch the socket adapter or the LSI during programming.
- Misprogramming can be caused by poor contacts.

On-Chip EPROM Reliability after Programming: Generally, semiconductors are reliable except for initial failures. Parts can be screened to avoid failures. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold characteristics are high. Exposing the LSI to 150°C after user programming can effectively upgrade these characteristics. Figure 30 shows the recommended screening flow.

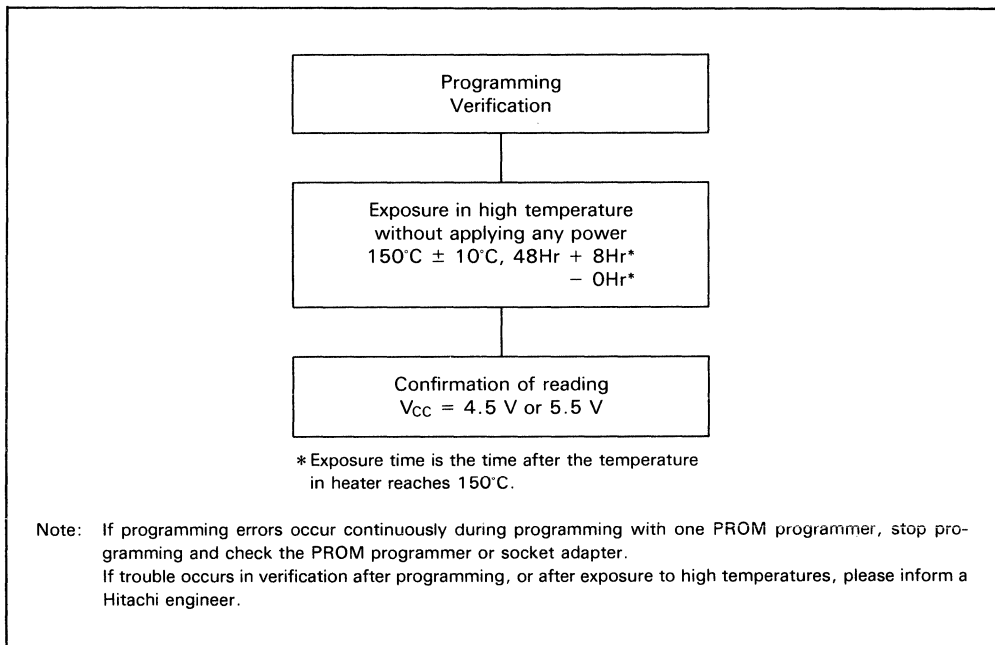


Figure 30. Recommended Screening Flow

Window-Type Package Precautions

Glass Erasure Window: If the glass window comes in contact with plastic or anything with a static charge, the LSI may malfunction due to the electrostatic charge on the surface of the window. If this occurs, exposing the LSI to ultraviolet light for a few minutes neutralizes the charge, and restores the LSI to normal operation. However, charge stored in the floating gate decreases at the same time, so reprogramming is recommended.

Electrostatic charge buildup on the window is a fundamental cause of malfunctions. Measures for its prevention are the same as those for preventing electrostatic breakdown:

1. Operators should be grounded when handling equipment.
2. Do not rub the glass window with plastics.
3. Be careful of coolant sprays, which may contain a few ions.
4. The ultraviolet shading label (which includes conductive material) effectively neutralizes charge.

Ultraviolet Shading Label: If the LSI is exposed to fluorescent light or sunlight, its memory contents may be erased by the small quantity of ultraviolet light in these sources.

In strong light, the MCU may fail under the influence of photocurrent. To prevent these problems, it is recommended that the device be used with an ultraviolet shading label covering the erasure window after programming.

Special labels are sold for this purpose. They contain metal to absorb ultraviolet light. When choosing a label, note the following:

1. Adhesion (mechanical intensity)—Re-use and dust reduce adhesion. Peeling off a label may cause static electricity. Therefore, erasing and rewriting is recommended after peeling. Sticking a new label over the old one is better than replacing a label.
2. Allowable temperature range—The allowable environmental temperature range of the label should be noted. If it is used under conditions outside this range, the paste may stiffen or adhere to the label, causing paste to remain on the window when the label is removed.
3. Moisture resistance—The allowable moisture range and environmental conditions of the label should be noted. It is difficult to find a shade label applicable to all conditions. The proper label should be selected depending on the intended use of the MCU.

Addressing Mode

RAM Addressing Mode

As shown in figure 31, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 32.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on page boundary (256n + 255) (figure 33), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (Figure 34). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

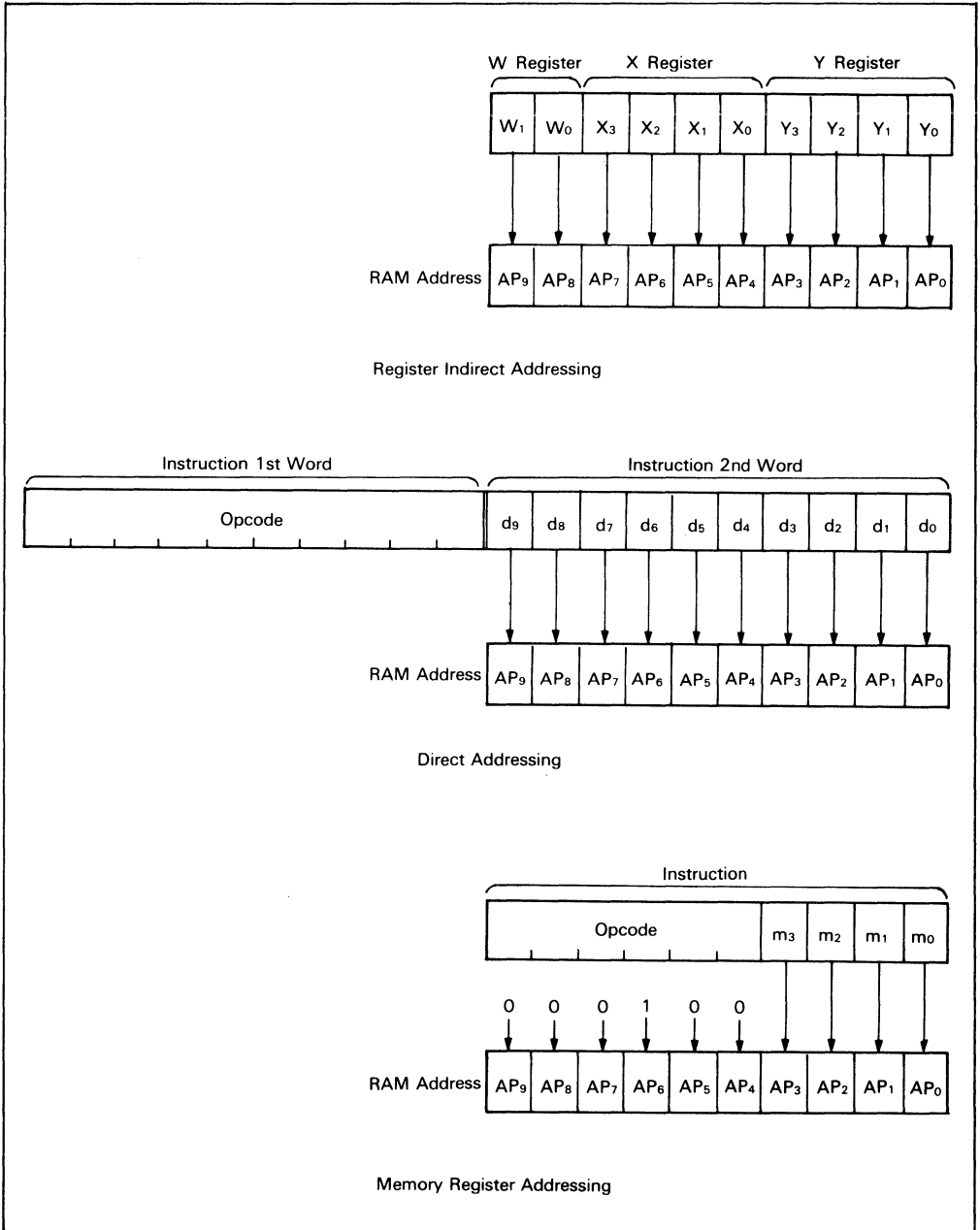


Figure 31. RAM Addressing Mode

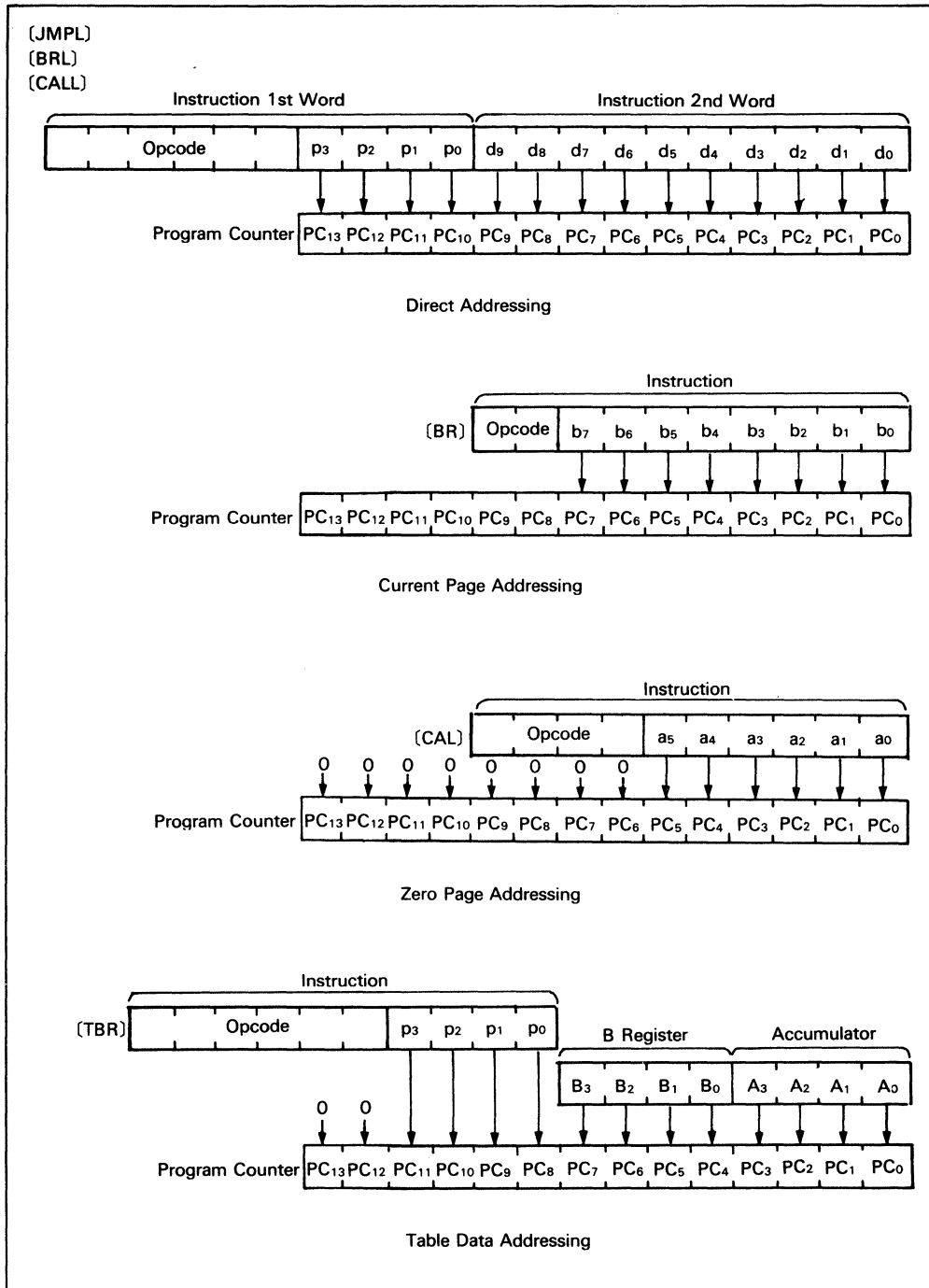


Figure 32. ROM Addressing Mode



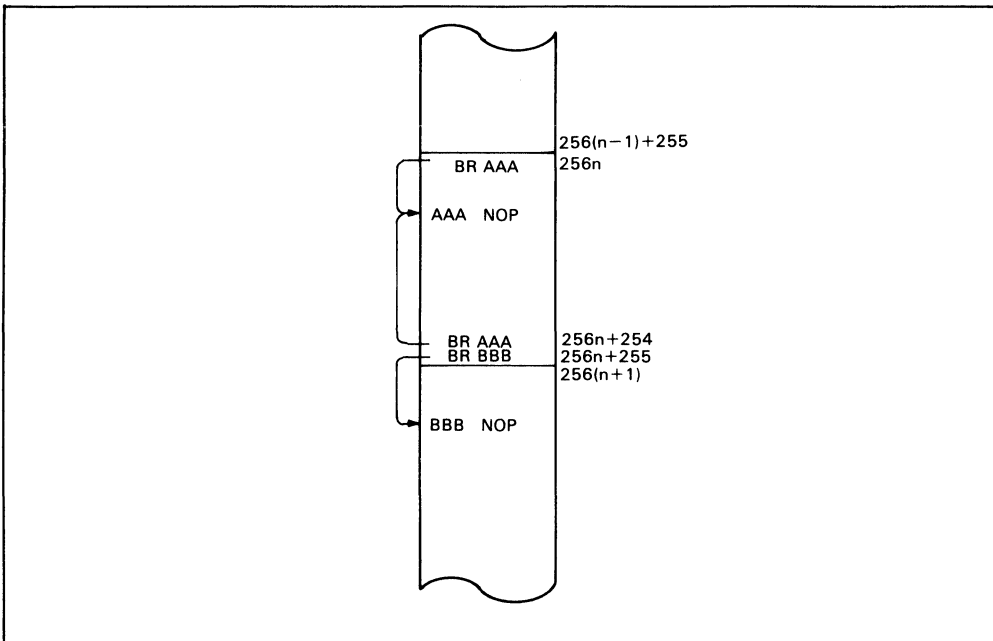


Figure 33. BR Instruction Branch Destination on Page Boundary

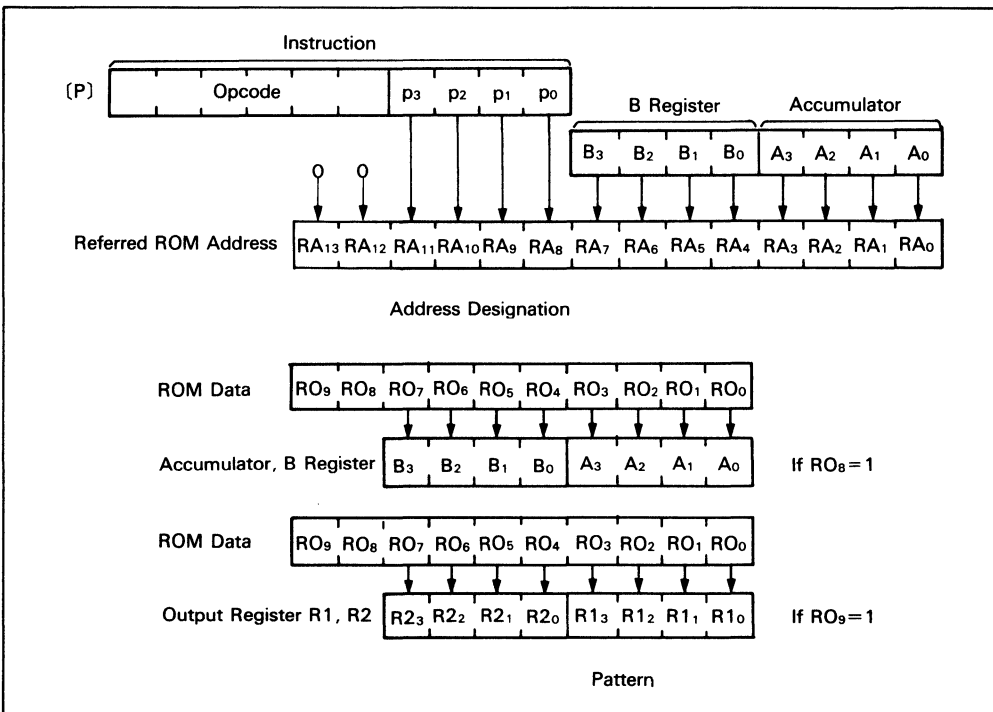


Figure 34. P Instruction



Instruction Set

The HD404302, HD4074308 provide 100 instructions which are classified into 10 groups as follows:

1. Immediate instruction (Table 9)
2. Register-to-register instruction (Table 10)
3. RAM address instruction (Table 11)
4. RAM register instruction (Table 12)
5. Arithmetic instruction (Table 13)
6. Compare instruction (Table 14)
7. RAM bit manipulation instruction (Table 15)
8. ROM address instruction (Table 16)
9. Input/output instruction (Table 17)
10. Control instruction (Table 18)

Tables 9-18 list their functions, and table 19 is an opcode map.

Table 9. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 10. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 11. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX,Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 12. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given, below).
Opcode X and Y are assembler as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X↔SPX, Y↔SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).
Opcode X is assembler as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 13. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/ Cycles	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A+CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M-A- \bar{CA} → A NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M-A- \bar{CA} → A NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR

Table 14. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 15. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 16. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 17. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 18. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: The STS (Start serial) instruction is not provided for the HD404302/HD4074308 since it does not have a serial interface.



Table 19. Opcode Map

R9 \ R8		0																1																						
		L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F						
0	0	NOP	XSP	XSP	XSP	XSP	AN	EM			AM				ORM			LAW				ANEMD				AMCD				ORMD										
	1	RTN	RTNI			ALEM				AMC					EOFM			LWA				ALEMCD				AMCD				EOFMCD										
	2	INEM								i(4)								INEMD								i(4)														
	3	ILEM								i(4)								ILEMD								i(4)														
	4	LBM(XY)				BNEM				LAB					IB			COMB				OR								SBYSTOP										
	5	LMAY(X)				AYY				LASPY					IY																	JMPL	p(4)							
	6	NEGA				RED				LASPX								TC														CALL	p(4)							
	7	YNEI								i(4)								BRL								p(4)														
	8	XMA(XY)				SEM	n(2)				REM	n(2)				TM	n(2)				XVMD				SEMD	n(2)				REMD	n(2)				TMD	n(2)				
	9	LAM(XY)				LMA(XY)				SMC					ANM			LAMD				LMAD				SMCD				ANMD										
	A	ROTR	ROTL						DAA					DAS			LAY															LMID	i(4)							
	B	TBR								p(4)								P								p(4)														
	C	XMB(XY)				BLEM				LBA							DB																							
	D	LMADY(X)				SY				LYA							DY																							
	E	TD				SED				LXA					REC		SEC															CAL	a(6)							
	F	LWI								i(2)																														
1	0	LBI								i(4)																														
	1	LYI								i(4)																														
	2	LXI								i(4)																														
	3	LAI								i(4)																														
	4	LBR								m(4)																														
	5	LAR								m(4)																														
	6	REDD								m(4)																														
	7	LAMR								m(4)								BR								b(8)														
	8	AI								i(4)																														
	9	LMIIY								i(4)																														
	A	TDD								m(4)																														
	B	ALEI								i(4)																														
	C	LRB								m(4)																														
	D	LRA								m(4)																														
	E	SEDD								m(4)																														
	F	XMRA								m(4)																														

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction
 2-word/2-cycle Instruction (2-word/2-cycle)



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Program Voltage	V_{PP}	-0.3 to +14.0	V	2, 13
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 42$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Maximum Input Current	I_O	15	mA	7, 8
Maximum Output Current	- I_O	4	mA	8, 9
		6	mA	9, 10
		30	mA	9, 11
Total Allowance of Output Current	- ΣI_O	150	mA	6
Operation Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{str}	-55 to +125	°C	
Storage Temperature (bias)	T_{bias}	-25 to +80	°C	13

- Notes:
1. Permanent LSI damage may occur if absolute maximum ratings are exceeded. Normal operation should be performed under the conditions specified by electrical characteristics. Exceeding these conditions can result in LSI malfunction or degraded performance.
 2. Applies to the RESET pin (V_{PP}). (HD4074308)
 3. Applies to pins except for high-voltage pins.
 4. Applies to high-voltage pins.
 5. Total allowance of input currents is the total sum of input current which flow in from all I/O pins to GND simultaneously.
 6. Total allowance of output currents is the total sum of the output current which flow output from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. Applies to R3 and R4.
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. Applies to R0 to R2.
 11. Applies to D0 to D12.
 12. Voltage is based on GND.
 13. Applies to the HD4074308.



Electrical Characteristics

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20\text{ to } +75\text{ }^\circ\text{C}$ unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, R32/ $\overline{INT_0}$, R33/ $\overline{INT_1}$	0.8 V_{CC}		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, R32/ $\overline{INT_0}$, R33/ $\overline{INT_1}$	- 0.3		0.2 V_{CC}	V		
		OSC ₁	- 0.3		0.5	V		
Input/Output Leakage Current	$ I_{II} $	RESET, R32/ $\overline{INT_0}$, R33/ $\overline{INT_1}$, OSC ₁			TBD	μA	$V_{in} = 0\text{ V to } V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			TBD	mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}			TBD	mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}			TBD	μA	$V_{in}(\overline{TEST}) = V_{CC}$ $V_{in}(\overline{RESET}) = GND$	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, TEST: V_{CC}
 - R3, R4: V_{CC}
 - D₀-D₁₂, R0-R2, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - RESET: GND
 - TEST: V_{CC}
 - R3, R4: V_{CC}
 - D₀-D₁₂, R0-R2, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When $f_{osc} = x$ (MHz) estimate the current dissipation as follows:
 Max value $f_{osc} = x\text{ MHz} = x/8 \times (\text{max value } f_{osc} = 4\text{ (MHz)})$



Input/Output Characteristics for Standard Pin ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20$ to $+75\text{ }^\circ\text{C}$ unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	R3 R4	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	R3 R4	-0.3		$0.2V_{CC}$	V		
Output High Voltage	V_{OH}	R3 R4	$V_{CC} - 1.0$			V	$- I_{OH} = 1.0\text{ mA}$	1
		R3 R4	$V_{CC} - 0.5$			V	$- I_{OH} = 0.5\text{ mA}$	1
Output Low Voltage	V_{OL}	R3 R4			0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IJ} $	R3 R4			1	μA	$V_{in} = 0\text{ V}$ to V_{CC}	2
Pull-Up MOS Current	$-I_p$	R3 R4	TBD	TBD	TBD	μA	$V_{CC} = 5\text{ V}$, $V_{in} = 0\text{ V}$	3

- Notes:
1. Applied to I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins with pull-up MOS selected by mask option.

HD404302/HD4074308

Input/Output Characteristics for High Voltage Pin ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20$ to $+75\text{ }^\circ\text{C}$ unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₁₂ , R ₁ , R ₂ , RA ₁ , R ₀	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₁₂ , R ₁ , R ₂ , RA ₁ , R ₀	$V_{CC} - 40$		$0.2 V_{CC}$	V		
Output High Voltage	V_{OH}	D ₀ -D ₁₂ , TG ₀ , TG ₁	$V_{CC} - 3.0$			V	$- I_{OH} = 15\text{ mA}$	
			$V_{CC} - 2.0$			V	$- I_{OH} = 10\text{ mA}$	
			$V_{CC} - 1.0$			V	$- I_{OH} = 4\text{ mA}$	
		R ₀ -R ₂	$V_{CC} - 3.0$			V	$- I_{OH} = 3\text{ mA}$,	
			$V_{CC} - 2.0$			V	$- I_{OH} = 2\text{ mA}$	
			$V_{CC} - 1.0$			V	$- I_{OH} = 0.8\text{ mA}$	
Output Low Voltage	V_{OL}	D ₀ -D ₁₂ , R ₀ -R ₂			$V_{CC} - 34$	V	$V_{disp} = V_{CC} - 40\text{ V}$	1
		D ₀ -D ₁₂ , R ₀ -R ₂			$V_{CC} - 37$	V	$150\text{k}\Omega$ to $V_{CC} - 40\text{V}$	2
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₁₂ , R ₀ -R ₂ , RA ₁		20		μA	$V_{in} = V_{CC} - 40\text{ V}$ to V_{CC}	3
Pull-Down MOS Current	I_d	D ₀ -D ₁₂ , R ₀ -R ₂ ,	TBD	TBD	TBD	μA	$V_{disp} = V_{CC} - 35\text{ V}$, $V_{in} = V_{CC}$	4

- Notes:
1. Applied to I/O pins with pull-down MOS selected by mask option.
 2. Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
 3. Pull-down MOS current and output buffer current are excluded.
 4. Applied to I/O pins with pull-down MOS selected by mask option.

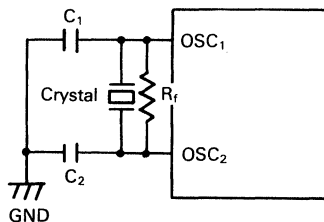


AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20\text{ to } +75^\circ\text{C}$, unless otherwise noted)

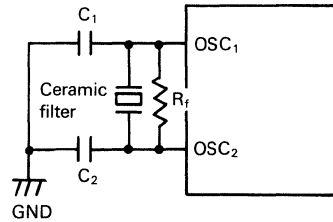
Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Oscillation Frequency (Divide-by-8)	f_{OSC}	OSC ₁ , OSC ₂	TBD	4	4.5	MHz		
Instruction Cycle Time	T_{cyc}		1.78	2	TBD	μs		
Oscillation Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External Clock Frequency	$f_{CP,}$	OSC ₁	TBD	—	4.5	MHz		
External Clock High, Low Level Width	$t_{CPH,}$ t_{CPL}	OSC ₁	203			ns	Divide-by-8	2
External Clock Rising, Falling Time	$t_{CPr,}$ t_{Cpf}	OSC ₁			20	ns		2
INT ₀ High, Low Level Width	$t_{IOH,}$ t_{IOL}	INT ₀	2			T_{cyc}		3
INT ₁ High, Low Level Width	$t_{IIH,}$ t_{IIL}	INT ₁	2			T_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			T_{cyc}		4
Input Capacitance	C_{in}	Except RESET			20	pF	$f = 1\text{ MHz}, V_{in} = 0\text{V}$	
		RESET			TBD	pF	$f = 1\text{ MHz}, V_{in} = 0\text{V}$	
RESET Falling Time	t_{RSTf}				20	ms		4

Notes: 1. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5 V at power-on, or after RESET goes to high in canceling system oscillator stop state. At power-on, or canceling system oscillator stop state, RESET must remain high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, it is recommended that the user should get the maker's advice when designing the RESET circuit.



Crystal: 4.194304 MHz
 $R_f =$ } TBD
 $C_1 =$ }

2. See figure 35.
3. See figure 36.
4. See figure 37.
5. See figure 38.



Ceramic filter: CSA 4.00 MG (Murata)
 $R_f =$ } TBD
 $C_1 = C_2 =$ }



HD404302/HD4074308

A/D Converter Characteristics ($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = \text{GND}$, $T_a = 0\text{ to } +70\text{ }^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition
Analog power supply voltage	AV_{CC}	AV_{CC}	$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V	
Analog input voltage	AV_{in}	ANO-AN3	AV_{SS}		AV_{CC}	V	
Current between AV_{CC} - AV_{SS}	I_{ad}		—	TBD	—	mA	
Analog input capacity	C_{ain}	ANO-AN3	—	TBD	—	pF	
Resolution			8	8	8	Bit	
Conversion Time			61	—	—	μs	
Number of inputs			0	—	4	Channel	
Absolute accuracy			—	—	TBD	LSB	$T_a = 25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$

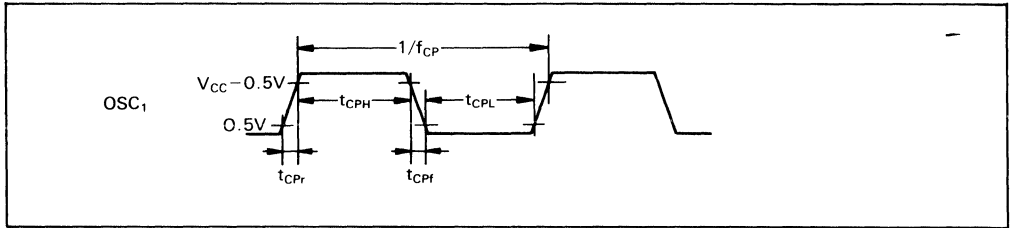


Figure 35. Oscillator Timing

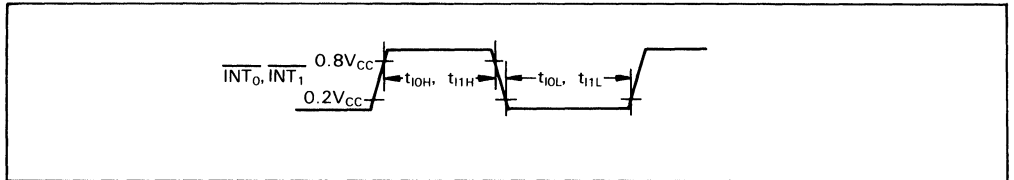


Figure 36. Interrupt Timing

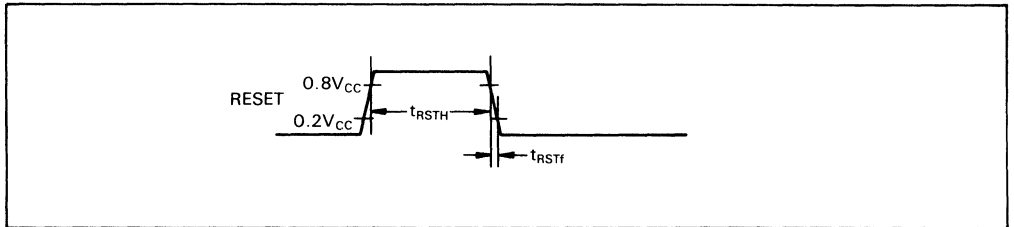


Figure 37. Reset Timing

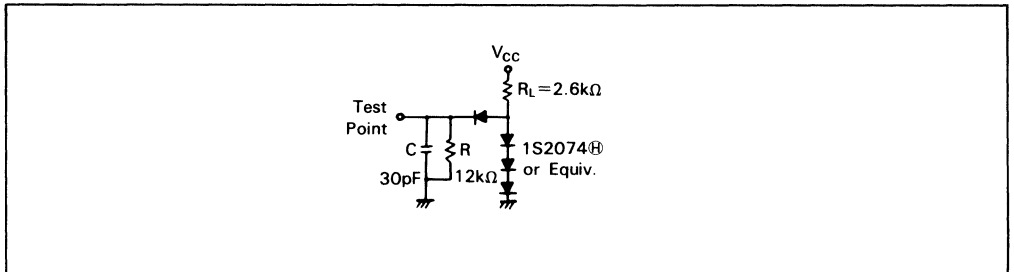


Figure 38. Timing Load Circuit

HD404302/HD4074308

Programming Electrical Characteristics for HD4074308

Write and Verify Mode

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{V}/0.5\text{V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time	t_{AS}	2			μs	Figure 39
\overline{OE} set-up time	t_{OES}	2			μs	
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

Note : 1. Input pulse level—0.8 to 2.2V
 Input rising/falling time $\leq 20\text{ns}$
 Timing reference level { input : 1.0V, 2.0V
 output : 0.8V, 2.0V



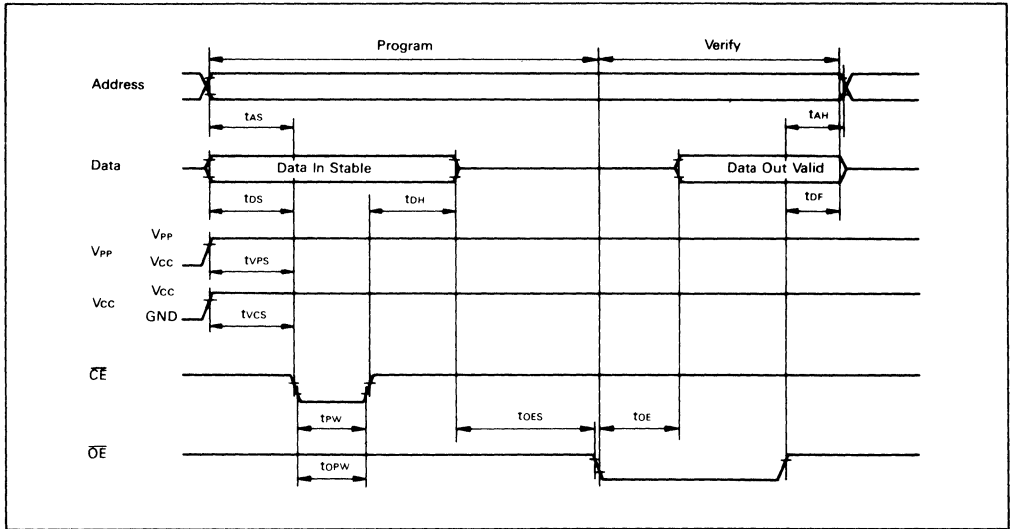


Figure 39. PROM Programming/Verifying Timing Diagram

Switching characteristics

- Input pulse level0.8V to 2.2V
- Input rising/falling time ≤ 20 ns
- Output loading1TTL Gate + 100pF
- Input/output timing reference levelOutput: 1V, 2V
Input: 0.8V, 2V

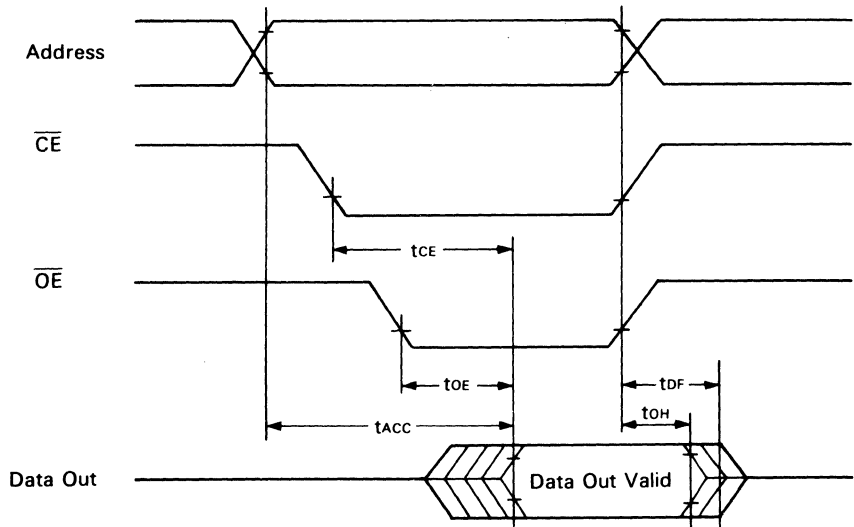


Figure 40. PROM Read Timing Diagram

Read Mode

DC Characteristics

($V_{CC}=5\text{ V} \pm 10\%$, $V_{PP}=V_{CC} \pm 0.6\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Condition
Input Leak Current	I_{LI}			1	μA	$V_{CC}=5.5\text{ V}$, $V_{in}=\text{GND to } V_{CC}$
Output Leak Current	I_{LO}			1	μA	$V_{CC}=5.5\text{ V}$, $V_{out}=\text{GND to } V_{CC}$
Programming V_{PP} Current	I_{PP}		1	100	μA	$V_{PP}=V_{CC}+0.6\text{ V}$
Operating V_{CC} Current	I_{CC}^*			30	mA	$f=1\text{ MHz}$, $I_{out}=0\text{ mA}$
Input Voltage	V_{IL}	-0.3		0.8	V	
	V_{IH}	2.2		$V_{CC}+0.3$	V	
Output Voltage	V_{OL}			0.4	V	$I_{OL}=1.6\text{ mA}$
	V_{OH}	2.4			V	$I_{OH}=-200\mu\text{A}$

* Input through current is excluded.

AC Characteristics

($V_{CC}=5\text{ V} \pm 10\%$, $V_{PP}=V_{CC} \pm 0.6\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Max	Unit	Condition
Access Time	t_{ACC}		500	ns	$\overline{CE}=\overline{OE}=V_{IL}$
\overline{CE} Output Delay Time	t_{CE}		500	ns	$\overline{OE}=V_{IL}$
\overline{OE} Output Delay Time	t_{OE}	10	150	ns	$\overline{CE}=V_{IL}$
Output Disable Delay Time	t_{DF}^*	0	105	ns	$\overline{CE}=V_{IL}$
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

* t_{DF} is determined when the output reaches open state and output level cannot be referred.

HD404302
Option List

* Please enter check marks in , for example , x or .

(1) Package type

<input type="checkbox"/> DP-42

(2) ZTAT compatibility

<input type="checkbox"/> I/O circuit compatibility with the HD4074308
<input type="checkbox"/> No I/O circuit compatibility with the HD4074308

(Note) ZTAT compatibility is enabled only when all pins use C or D type circuit. In this case do not check the list item (3) and (5).

(3) I/O option (I/O options masked by are not available)

Pin name	I/O	I/O option				
		A	B	C	D	E
D ₀	I/O	/	/	/	/	/
D ₁	I/O	/	/	/	/	/
D ₂	I/O	/	/	/	/	/
D ₃	I/O	/	/	/	/	/
D ₄	I/O	/	/	/	/	/
D ₅	I/O	/	/	/	/	/
D ₆	I/O	/	/	/	/	/
D ₇	I/O	/	/	/	/	/
D ₈	I/O	/	/	/	/	/
D ₉	I/O	/	/	/	/	/
D ₁₀	I/O	/	/	/	/	/
D ₁₁	I/O	/	/	/	/	/
D ₁₂	I/O	/	/	/	/	/
RA RA ₁	I	Check (5)				
R0	High-voltage pins					
	RO ₀	I/O	/	/	/	/
	RO ₁	I/O	/	/	/	/
	RO ₂	I/O	/	/	/	/
RO ₃	I/O	/	/	/	/	
R1	R1 ₀	I/O	/	/	/	/
	R1 ₁	I/O	/	/	/	/
	R1 ₂	I/O	/	/	/	/
	R1 ₃	I/O	/	/	/	/
R2	R2 ₀	I/O	/	/	/	/
	R2 ₁	I/O	/	/	/	/
	R2 ₂	I/O	/	/	/	/
	R2 ₃	I/O	/	/	/	/

Please check the option you select.

- A: Without pull-up MOS
- B: CMOS output with pull-up MOS
- C: CMOS output without pull-up MOS
- D: Without pull-down MOS (PMOS open-drain)
- E: With pull-down MOS

Note that when all pins are selected as C or D, items (3) and (5) should not be checked.

Order data	
Company name	
Department	
Name	
ROM code	
LSI type	HD40

(4) ROM media

<input type="checkbox"/> EPROM: emulator type
<input type="checkbox"/> HD4074308

(5) RA₁/V_{disp}

<input type="checkbox"/> RA ₁ : without pull-down MOS (D)
<input type="checkbox"/> V _{disp}

Note: RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high voltage pins are option E.

Condition

(6) OSC₁ and OSC₂ oscillator

<input type="checkbox"/> Ceramic filter	f =	MHz
<input type="checkbox"/> Crystal	f =	MHz
<input type="checkbox"/> External clock	f =	MHz

Pin name	I/O	I/O option				
		A	B	C	D	E
R3	Standard pins					
	R3 ₀	I/O	/	/	/	/
	R3 ₁	I/O	/	/	/	/
	R3 ₂	I/O	/	/	/	/
R3 ₃	I/O	/	/	/	/	
R4	Standard pins					
	R4 ₀	I/O	/	/	/	/
	R4 ₁	I/O	/	/	/	/
	R4 ₂	I/O	/	/	/	/
R4 ₃	I/O	/	/	/	/	



HD404418/HD4074418/ HD4074408

Description

The HD404418, HD4074418, and HD4074408 are 4-bit single chip microcomputers basically equivalent to the HMCS400 series providing high programming productivity and high-speed operation. The devices have on-chip resources such as ROM, RAM, I/O, four timer/counters, and two serial interfaces. All pins are CMOS standard for the HD404418, HD4074418, and the HD4074408 includes 8 high-voltage pins.

Features

- 8,192 words × 10 bits ROM
- 512 digits × 4 bits RAM
- 58 I/O pins
 - Including 4 input pins, 16 high current pins (total current: 100 mA), 2 NMOS open-drain pins, and 8 high-voltage NMOS open-drain pins (HD4074408 only)
 - HD404418, HD4074418: all CMOS standard pins
 - HD4074408: includes 8 high voltage pins
- 4 timer/counters
- 4 analog inputs
- 2 clock-synchronous 8-bit serial interfaces
- 12 interrupt sources
 - External: 6
 - Internal: 6

- Subroutine stack: Up to 16 levels including interrupts
- Two low power dissipation modes
 - Standby mode
 - Stop mode
- On-chip oscillator: Crystal or ceramic filter (Externally drivable)
- Instruction cycle time: $1.0 \mu\text{s}$ ($f_{\text{osc}} = 8 \text{ MHz}$)
- Package
 - 64-pin shrink type ceramic DIP with window
 - 64-pin shrink type plastic DIP
 - 64-pin flat plastic package

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Ordering Information

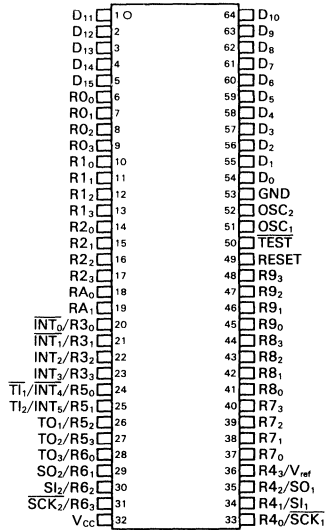
	Part No.	Package
Mask ROM type	HD404418S	DP-64S
	HD404418F	FP-64
	HD404418H	FP-64A
ZTAT type	HD4074418S	DP-64S
	HD4074418C	DC-64S
	HD4074418F	FP-64
	HD4074418H	FP-64A
	HD4074408S	DP-64S
	HD4074408C	DC-64S
	HD4074408F	FP-64
	HD4074408H	FP-64A



Pin Arrangement

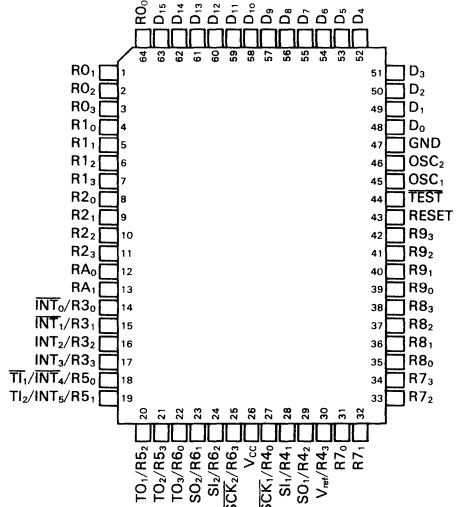
HD404418S, HD4074418C, HD4074418S,
HD4074408C, HD4074408S

HD404418F, HD4074418F, HD4074408F



DC-64S, DP-64S

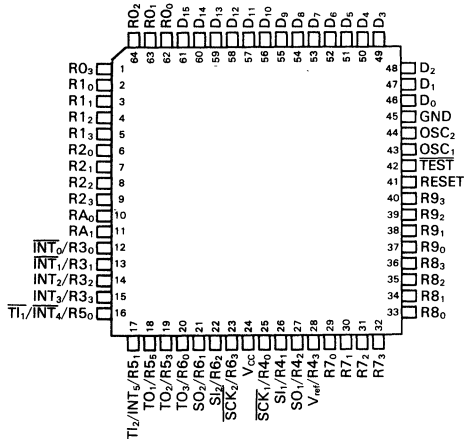
(Top View)



FP-64

(Top View)

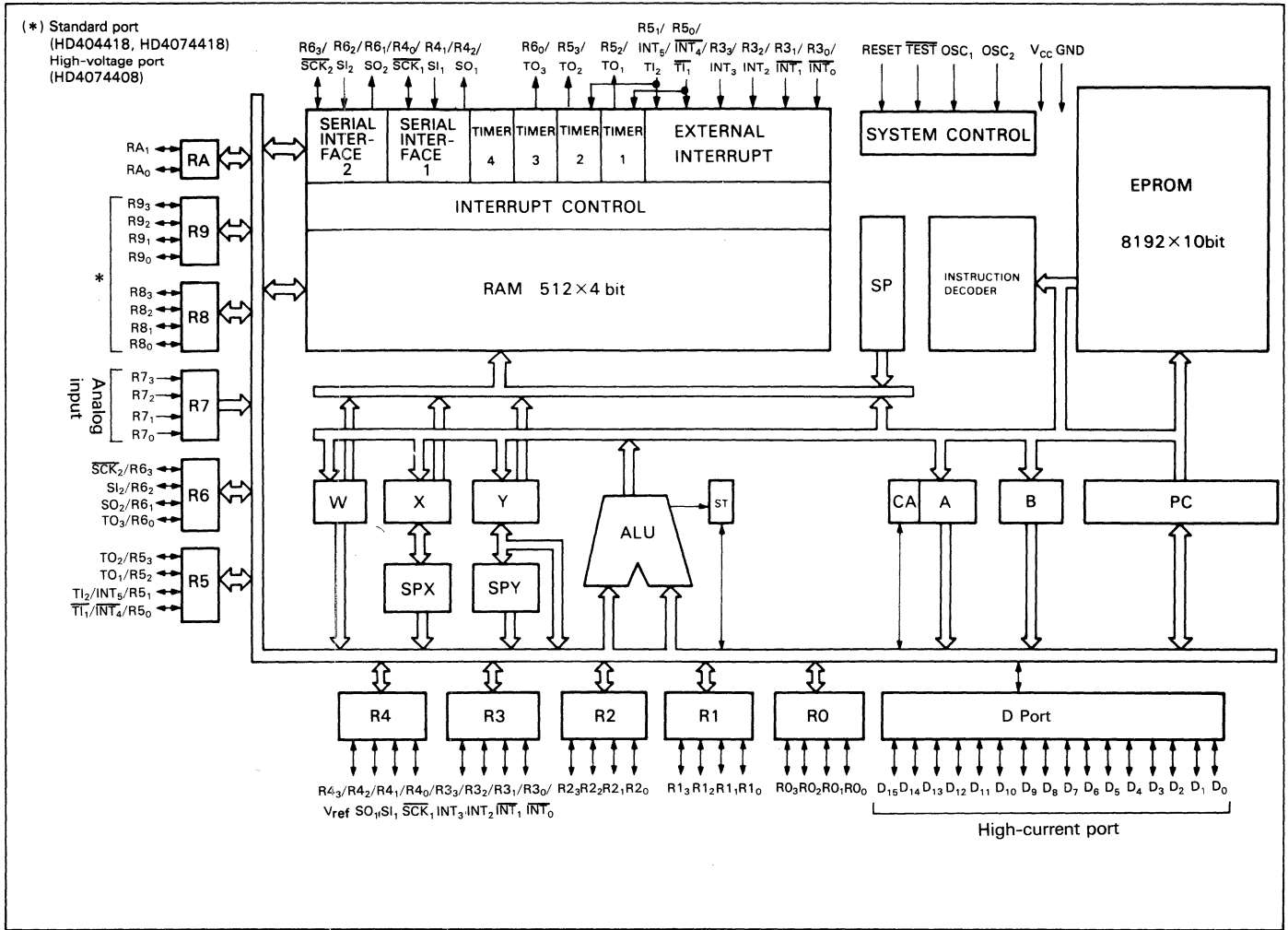
HD404418H, HD4074418H, HD4074408H



FP-64A

(Top View)

Block Diagram



Pin Function

GND, V_{CC} (Power)

GND and V_{CC} are the power supply pins for the MCU. Connect GND to the ground (0 V) and apply 5 V ± 10% to the V_{CC} pin.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are the connection pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits.

D₀–D₁₅ (Port D)

Port D consists of 16 1-bit input/output ports. Pins D₀-D₁₅ are all high-current pins. For details, see Input/Output section.

R0–RA (Port R)

Ports R0-R9 are 4-bit I/O ports. (RA consists of two bits.) Refer to Input/Output section for details.

Ports R0-R2, RA: R0-R2, RA are I/O ports.

Port R3: Port R3 I/O port is available as an input of the external interrupts (INT₀-INT₃).

Port R4: Port R4 is an I/O port. Pins R4₀-R4₂ can be used as I/O pins of the serial interface. Pin R4₃ functions as a reference voltage input pin (V_{ref}) of the analog input pin.

Port R5: Port R5 is an I/O port. Pins R5₀ and R5₁ function as the inputs of external interrupt pins (INT₄, INT₅) or timer 1, timer 2. Pins R5₂

and R5₃ function as outputs of timer 1 and timer 2.

Port R6: Port R6 is an I/O port. Pins R6₁-R6₃ are the I/O pins of the serial interface 2. R6₀ is available as output pin of timer 3.

Port R7: Port R7 input port is available as an analog input port.

Ports R8, R9: Ports R8 and R9 I/O ports are used as standard ports for the HD404418, HD4074418, and as high-voltage ports for the HD4074408.

INT₀, INT₁, INT₂, INT₃, INT₄, INT₅ (Interrupts)

INT₀, INT₁, INT₂, INT₃, INT₄, INT₅ are external interrupts for the MCU. INT₀, INT₁, INT₂, INT₃, INT₄, INT₅ are multiplexed with R3₀, R3₁, R3₂, R3₃, R5₀/TI₁, R5₁/TI₂ respectively. For details, see Interrupt section.

SCK₁, SCK₂, SI₁, SI₂, SO₁, SO₂ (Serial Interface)

The transfer clock I/O pin (SCK₁, SCK₂), serial data input pin (SI₁, SI₂), and serial data output pin (SO₁, SO₂) are used for serial interface. SCK₁, SCK₂, SI₁, SI₂, SO₁, SO₂ are multiplexed with R4₀, R6₃, R4₁, R6₂, R4₂, R6₁ respectively. For details, see Serial Interface section.

TI₁, TI₂, TO₁, TO₂, TO₃ (Timer)

TI₁ and TI₂ are external clock input pins for the timers, and TO₁-TO₃ are timer output pins. TI₁, TI₂, TO₁, TO₂, and TO₃ are multiplexed with R5₀/INT₄, R5₁/INT₅, R5₂, R5₃, and R6₀, respectively.

V_{ref}, R7 (Analog Reference Inputs)

V_{ref} reference voltage input pin inputs threshold voltage of analog input pins. V_{ref} is multiplexed with R4₃. Analog input pins are multiplexed with port R7.

Functional Description

ROM Memory Map

The MCU includes 8,192 words \times 10 bits of PROM. It is described in the following paragraphs and the PROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After the reset or interrupt is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions can refer to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

RAM Memory Map

The MCU includes 512 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$005): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$006 to \$027): The special function registers are the mode or data registers for the external interrupt, the serial interface, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. SEM/SEMD instruction or REM/REMD instruction are available for the mode register (SMR) and clock register (SCR) of the serial interface, the mode register (TMR) and output register (TOR) of the timer, the analog mode register (AMR) and the port mode register (PMR), and each data direction register (DDR). TM/TMD instruction is available for read register. RAM

bit manipulation instructions are unavailable to other registers.

Data Area (\$040 to \$1FF): 16 digits of \$040 through \$04F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when subroutine calls (CAL instruction, CALL instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

Registers and Flags

The MCU has nine registers and two flags for the CPU operations (figure 5).

Accumulator (A), Register B (B): The 4-bit accumulator and register B hold the results from the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

Register W (W), Register X (X), Register Y (Y): The 2-bit register W, and the 4-bit registers X and Y address RAM indirectly. Register Y is also used for port D addressing.

Register SPX (SPX), Register SPY (SPY): The 4-bit registers SPX and SPY assist registers X and Y, respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value for the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after a BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack. It is



restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter to hold the ROM address.

Stack Pointer (SP): The stack pointer (SP) points to the address of the next stack area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the high four bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF either by MCU reset or by the RSP bit reset through REM/REMD instruction.

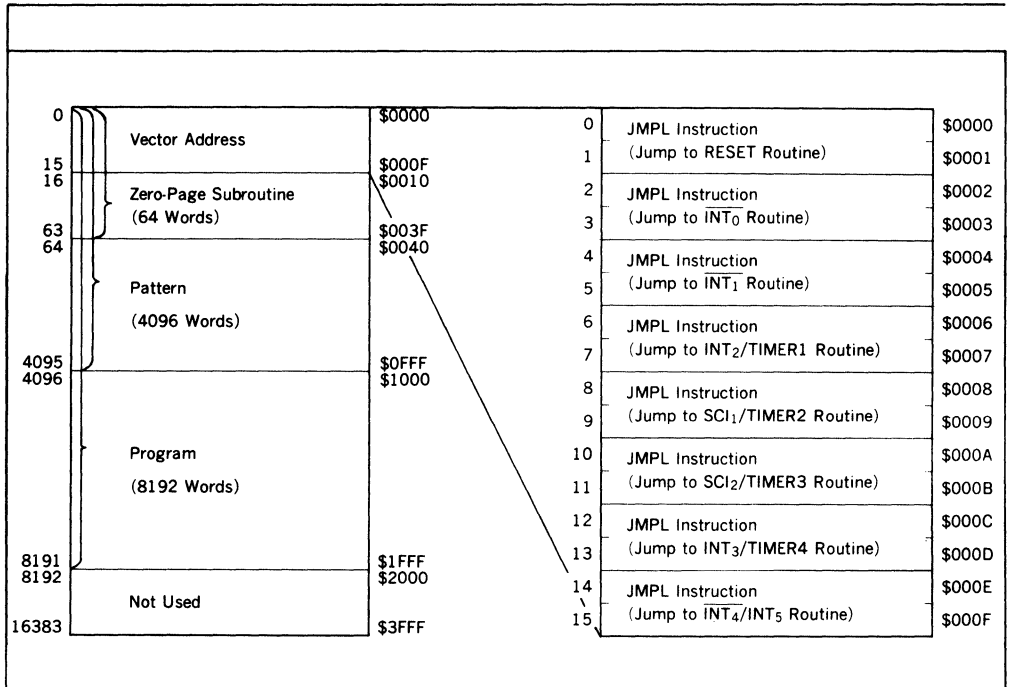


Figure 1. ROM Memory Map



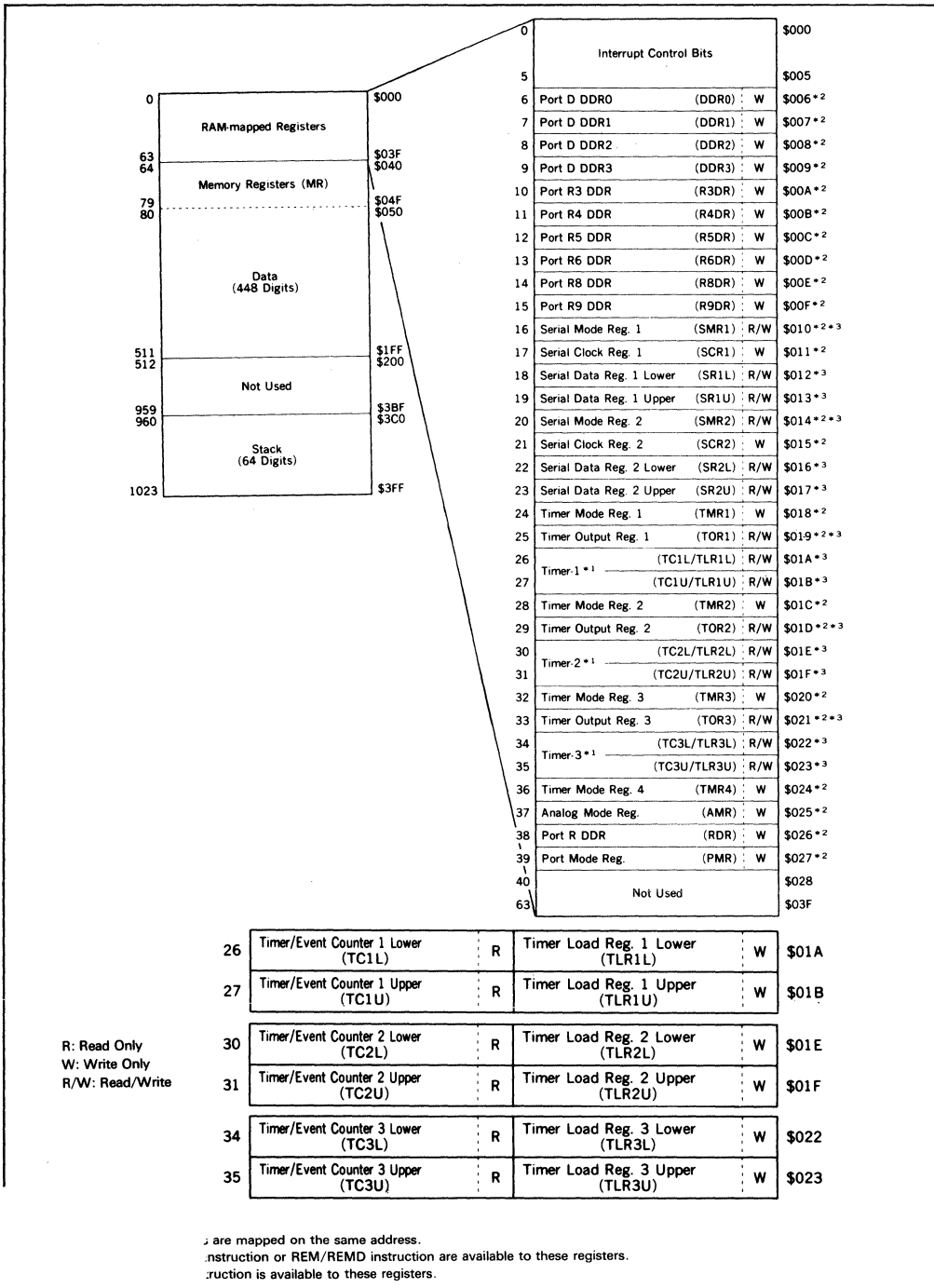


Figure 2. RAM Memory Map



	bit 3	bit 2	bit 1	bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP Bit)	I/E (Interrupt Enable Flag)	\$000
1	IM2 (IM of INT_2)	IF2 (IF of INT_2)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	\$001
2	IMS1 (IM of Serial 1)	IFS1 (IF of Serial 1)	IMT1 (IM of Timer 1)	IFT1 (IF of Timer 1)	\$002
3	IMS2 (IM of Serial 2)	IFS2 (IF of Serial 2)	IMT2 (IM of Timer 2)	IFT2 (IF of Timer 2)	\$003
4	IM3 (IM of INT_3)	IF3 (IF of INT_3)	IMT3 (IM of Timer 3)	IFT3 (IF of Timer 3)	\$004
5	IM4 (IM of $\overline{INT_4}/INT_5$)	IF4 (IF of $\overline{INT_4}/INT_5$)	IMT4 (IM of Timer 4)	IFT4 (IF of Timer 4)	\$005

IF: Interrupt Request Flag
 IM: Interrupt Mask
 I/E: Interrupt Enable Flag
 SP: Stack Pointer

Note: Each bit in interrupt control bits area is set and reset by SEM/SEMD and REM/REMD instruction and is tested by TM/TMD instruction. It is not affected by other instructions. Furthermore, interrupt request flag is not affected by SEM/SEMD instruction. The contents of status becomes invalid when RSP bit is tested.

Figure 3. Configuration of Interrupt Control Bit Area

Memory Registers			Stack Area		
64	MR(0)	\$ 040	960	Level 16	\$ 3C0
65	MR(1)	\$ 041		Level 15	
66	MR(2)	\$ 042		Level 14	
67	MR(3)	\$ 043		Level 13	
68	MR(4)	\$ 044		Level 12	
69	MR(5)	\$ 045		Level 11	
70	MR(6)	\$ 046		Level 10	
71	MR(7)	\$ 047		Level 9	
72	MR(8)	\$ 048		Level 8	
73	MR(9)	\$ 049		Level 7	
74	MR(10)	\$ 04A		Level 6	
75	MR(11)	\$ 04B		Level 5	
76	MR(12)	\$ 04C		Level 4	
77	MR(13)	\$ 04D		Level 3	
78	MR(14)	\$ 04E		Level 2	
79	MR(15)	\$ 04F	1023	Level 1	\$ 3FF

	bit 3	bit 2	bit 1	bit 0	
1020	ST	\overline{PC}_{13}	\overline{PC}_{12}	\overline{PC}_{11}	\$ 3FC
1021	\overline{PC}_{10}	\overline{PC}_9	\overline{PC}_8	\overline{PC}_7	\$ 3FD
1022	CA	\overline{PC}_6	\overline{PC}_5	\overline{PC}_4	\$ 3FE
1023	\overline{PC}_3	\overline{PC}_2	\overline{PC}_1	\overline{PC}_0	\$ 3FF

\overline{PC}_{13} — \overline{PC}_0 : Program Counter
 ST: Status
 CA: Carry

Figure 4. Configuration of Memory Register, Stack Area, and Stack Position



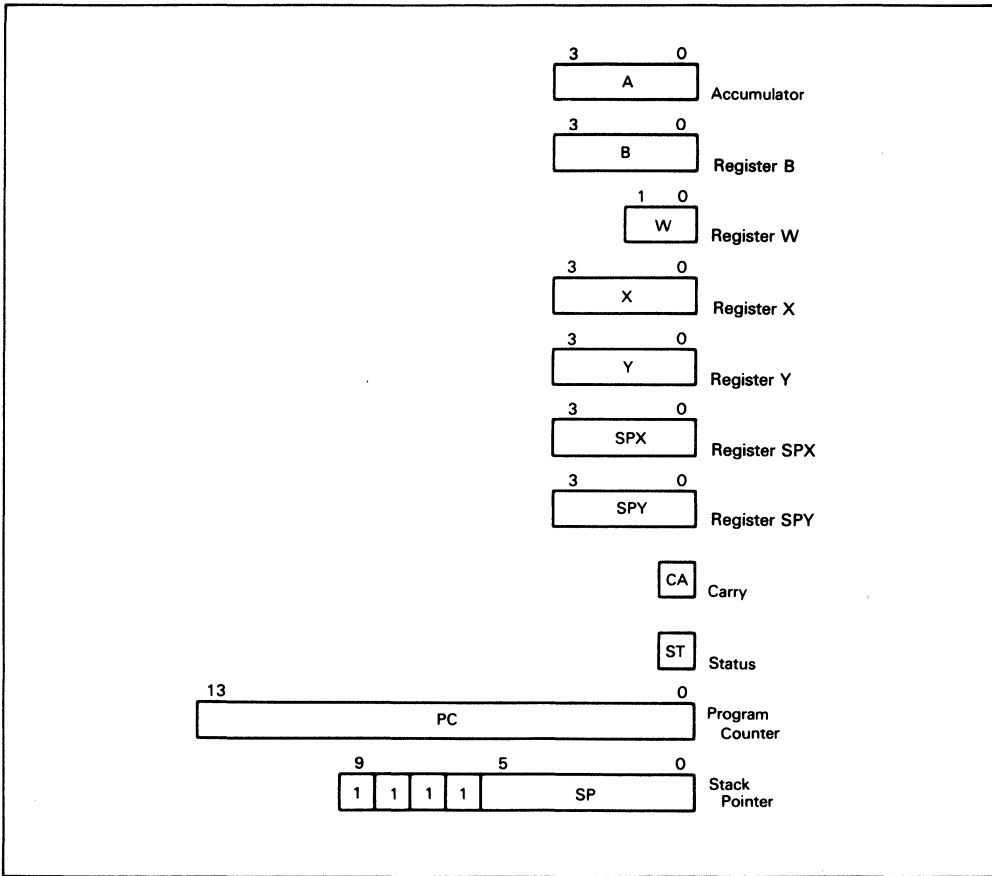


Figure 5. Registers and Flags

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode, the reset must satisfy t_{RC} to stabilize the oscillator. In all other cases, at least three

instruction cycles are required to reset the MCU.

Tables 1 and 2 show the parts and the status of each initialized by MCU reset.

Table 1. Initial Value after MCU Reset

Items		Initial value after MCU reset	Contents	
Program counter (PC)		\$0000	Execute program from the top of ROM address	
Status (ST)		1	Enable branch with conditional branch instructions	
Stack pointer (SP)		\$3FF	Stack level is 0	
I/O pin output register	Standard pin	CMOS	1	Enable input
		NMOS Open Drain	1	Enable input
	High-voltage pin	NMOS Open Drain	1	Enable input
Interrupt flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupt	
	Interrupt Request Flag (IF)	0	No interrupt request	
	Interrupt Mask (IM)	1	Mask interrupt request	
Mode Register	Serial Mode Register (SMR1 to 2)	0000	Refer to Serial Mode Register	
	Serial Clock Register (SCR1 to 2)	000	Refer to Serial Clock Register	
	Timer Mode Registers 1-3 (TMR1-3)	0000	Refer to Timer Mode Registers 1-3	
	Timer Output Registers 1-3 (TOR1-3)	0000	Refer to Timer Output Register	
	Timer Mode Register 4 (TMR4)	0000	Refer to Timer Mode Register 4	
	Analog Mode Register (AMR)	0000	Refer to Analog Mode Register	
	Port Mode Register (PMR)	0000	Refer to Port Mode Register	
	Data Direction Register (DDR0-3, R3DR-R9DR, RDR)	0000	Refer to Data Direction Register	
Timer/Counter, Serial Interface	Prescaler	\$000		
	Timer/Counter (TC4)	\$00		
	Timer/Event Counter (TC1-3)	\$00		
	Timer Load Register (TLR1-3)	\$00		
	Octal Counter	000		

Table 2. MCU Reset after Stop

Item		After Recovering from STOP Mode by MCU Reset	After All Other MCU Resets
Carry	(CA)	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.
Accumulator	(A)		
Register B	(B)		
Register W	(W)		
Register X/SPX	(X/SPX)		
Register Y/SPY	(Y/SPY)		
Serial Data Register 1-2 (SR1-SR2)			
RAM		The contents of RAM before MCU reset (just STOP instruction) are retained.	

Interrupt

The MCU can be interrupted by 12 different sources: the external signals (\overline{INT}_0 , \overline{INT}_1 , \overline{INT}_2 , \overline{INT}_3 , \overline{INT}_4 , \overline{INT}_5), timers (timer 1, timer 2, timer 3, timer 4), and serial interfaces (serial 1, serial 2).

Each interrupt source provides an interrupt request flag, and interrupt mask (\overline{INT}_4 and \overline{INT}_5 provide a common interrupt request flag and interrupt mask) to hold or control interrupt requests. Interrupt enable flags are available for controlling the total interrupt operations. Note that \overline{INT}_2 and timer 1, serial 1 and timer 2, serial 2 and timer 3, \overline{INT}_3 and timer 4 use common vector addresses, respectively. Therefore, the interrupt requests must be checked by software initially in the interrupt processing routine.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$005 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status and program counter are pushed onto the stack. In the third cycle, the execution of instruction starts after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF, which caused the interrupt service, must be reset by software in the interrupt service program.

Table 3. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector Addresses
RESET	—	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
\overline{INT}_2 /Timer 1	3	\$0006
Serial 1/Timer 2	4	\$0008
Serial 2/Timer 3	5	\$000A
\overline{INT}_3 /Timer 4	6	\$000C
\overline{INT}_4 / \overline{INT}_5	7	\$000E

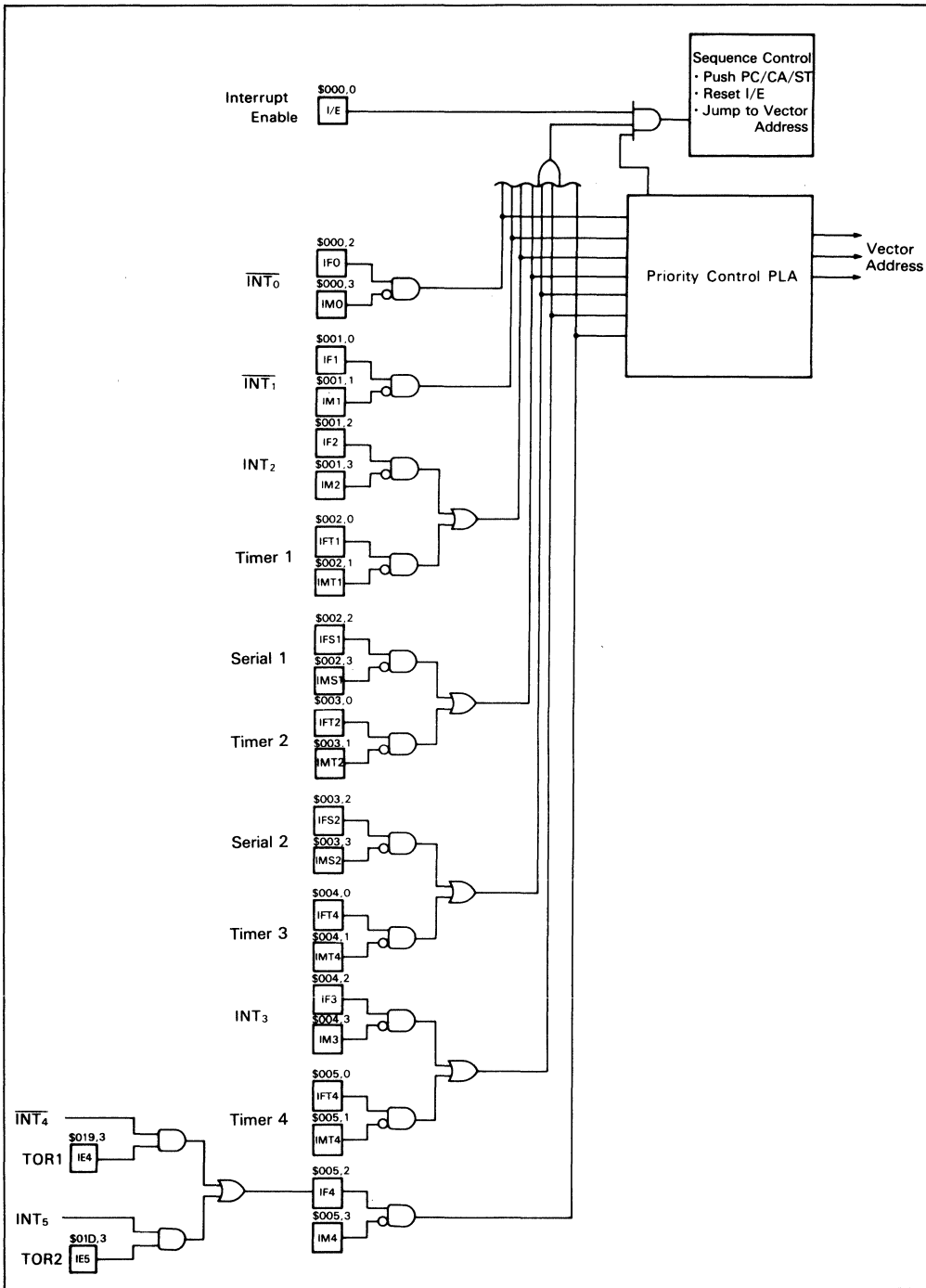


Figure 6. Interrupt Control Circuit Block Diagram



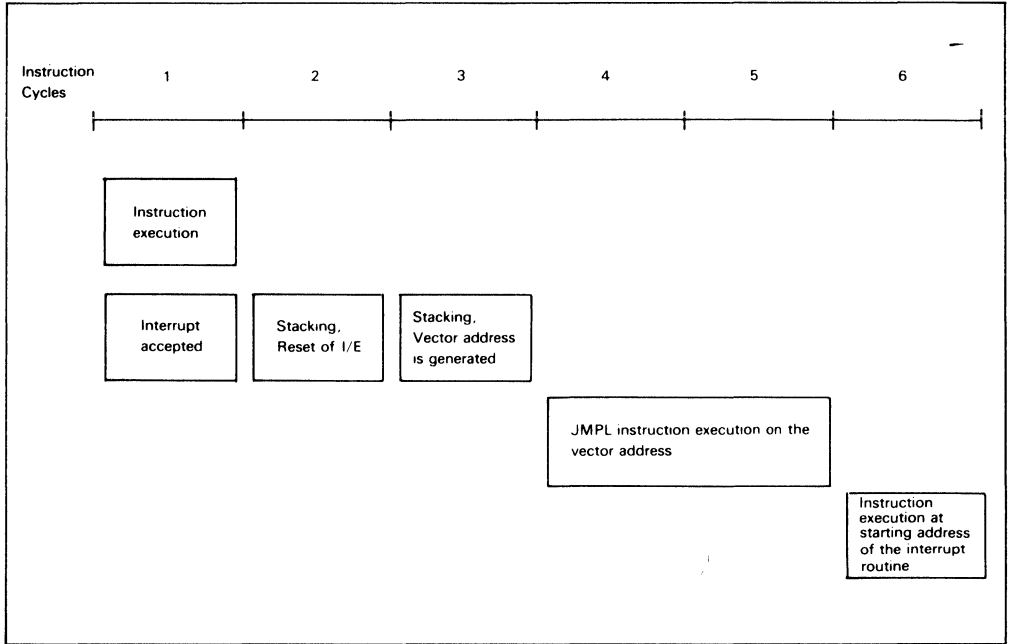


Figure 7. Interrupt Servicing Sequence

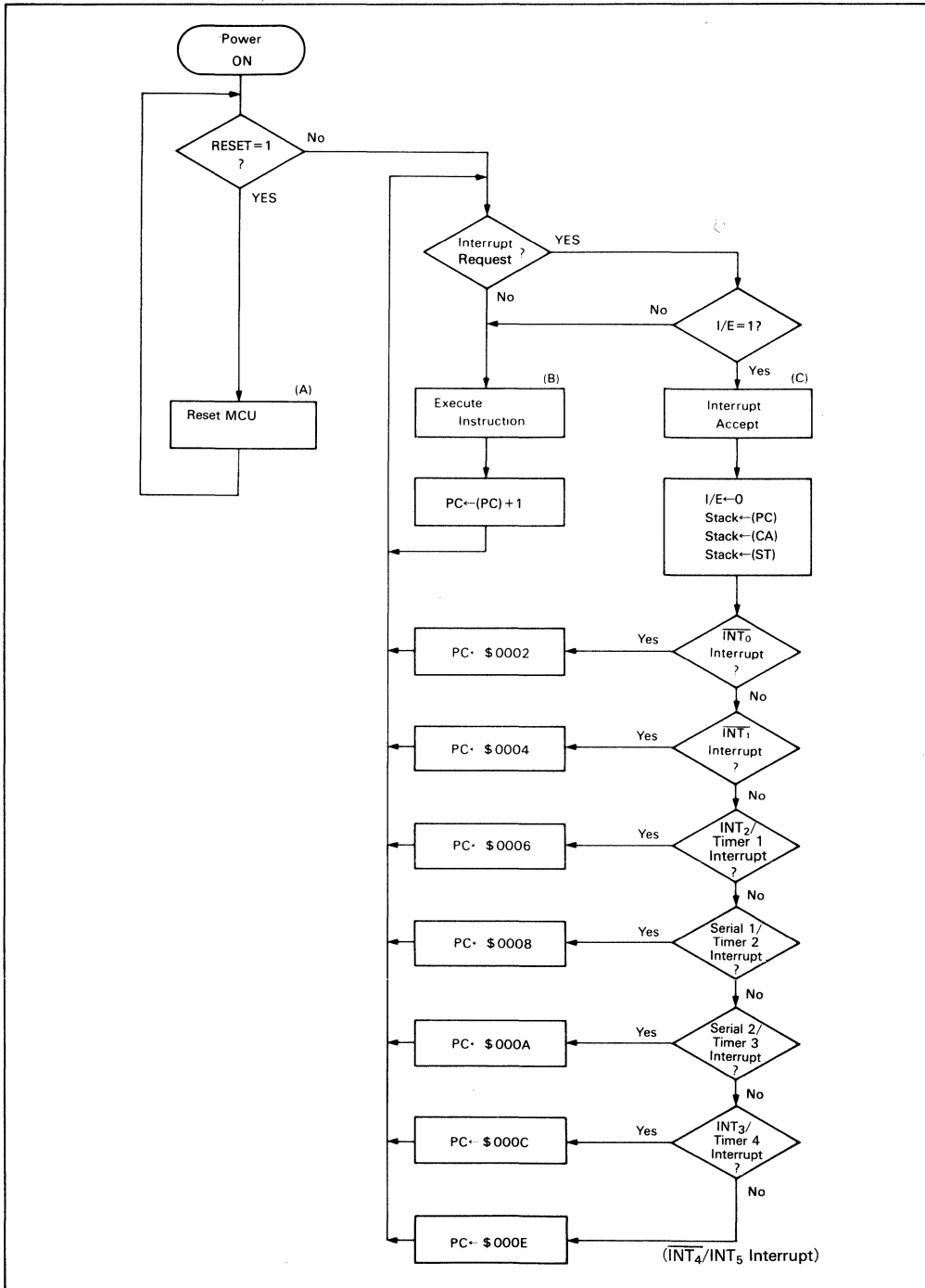


Figure 8. Interrupt Servicing Flowchart



Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 5. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1 , INT_2 , INT_3 , INT_4 , INT_5): External interrupt request flags are set at the falling edge of \overline{INT}_0 , \overline{INT}_1 , \overline{INT}_4 inputs or the rising edge of INT_2 , INT_3 , INT_5 inputs.

When using \overline{INT}_0 - INT_3 , select the external interrupt input by setting the appropriate bit of the port mode register (PMR: \$027). When the port mode register has been reset, external interrupt input signals are masked to ignore external interrupt requests.

When using \overline{INT}_4 and INT_5 , set the external interrupt enable bit of the timer output register (TOR1: \$019, TOR2: \$01D). Then the data direction registers of the corresponding pins are automatically reset to receive the external interrupt input signals. When the interrupt enable bit has been reset, external interrupt input signal and external interrupt request will be ignored.

Note that \overline{INT}_4 and INT_5 use a common

external interrupt request flag. Therefore, when using these pins, use one external interrupt input pin, or check the interrupt by software before starting the processing.

External Interrupt Request Flags (IF0: \$000,2, IF1: \$001,0, IF2: \$001,2, IF3: \$004,2, IF4: \$005,2): IF₀, IF₁ are set at the falling edge of INT_0 and \overline{INT}_1 inputs, respectively (table 6).

IF₂, IF₃ are set at the rising edge of INT_2 and INT_3 , respectively.

IF₄ is set at the falling edge of \overline{INT}_4 or at the rising edge of INT_5 .

External Interrupt Masks (IM0: \$000,3, IM1: \$001,1, IM2: \$001,3, IM3: \$004,3, IM4: \$005,3): These bits mask interrupt request to be generated by external interrupt request flags (table 7).

Timer Interrupt Request Flags (IFT1: \$002,0, IFT2: \$003,0, IFT3: \$004,0, IFT4: \$005,0): The timer interrupt request flags are set by the overflow output of timers 1-4. When timers 1-3 select PWM operation, overflow output does not set the interrupt request flag. When timer 4 is selected as the watchdog timer, overflow output resets the

Table 4. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	INT_2 / Timer 1	Serial 1/ Timer 2	Serial 2/ Timer 3	INT_3 / Timer 4	\overline{INT}_4 / INT_5
I/E	1	1	1	1	1	1	1
IF0· $\overline{IM0}$	1	0	0	0	0	0	0
IF1· $\overline{IM1}$	*	1	0	0	0	0	0
IF2· $\overline{IM2}$	*	*	1	*	0	0	0
IFT1· $\overline{IMT1}$	*	*	*	1	0	0	0
IFS1· $\overline{IMS1}$	*	*	*	1	*	0	0
IFT2· $\overline{IMT2}$	*	*	*	*	1	0	0
IFS2· $\overline{IMS2}$	*	*	*	*	1	*	0
IFT3· $\overline{IMT3}$	*	*	*	*	*	1	0
IF3· $\overline{IM3}$	*	*	*	*	*	1	*
IFT4· $\overline{IMT4}$	*	*	*	*	*	*	1
IF4· $\overline{IM4}$	*	*	*	*	*	*	1

* Don't care

MCU. Therefore, timer interrupt request flag is not set by overflow output (table 8).

Timer Interrupt Masks (IMT1: \$002,1, IMT2: \$003,1, IMT3: \$004,1, IMT4: \$005,1): The timer interrupt masks mask the occurrence of interrupt request to be generated by timers 1-4 interrupt request flags (table 9).

Serial Interrupt Request Flags (IFS1: \$002,2, IFS2: \$003,2): The serial interrupt request flags are set when the octal counter counts 8 transfer clocks, or when the data transfer is suspended, then the octal counter is reset (table 10).

Serial Interrupt Masks (IMS1: \$002,3, IMS2: \$003,3): The serial interrupt masks mask the interrupt request which the serial interrupt request flag generates. (table 11).

Table 5. Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt Enable/Disable
0	Disable
1	Enable

Table 6. External Interrupt Request Flag

External Interrupt Request Flags (IF0, IF1, IF2, IF3, IF4)	Interrupt Requests
0	No
1	Yes

Table 7. External Interrupt Mask

External Interrupt Masks (IM0, IM1, IM2, IM3, IM4)	Interrupt Requests
0	Enable
1	Disable (masks)

Table 8. Timer Interrupt Request Flags

Timer Interrupt Request Flags (IFT1, IFT2, IFT3, IFT4)	Interrupt Requests
0	No
1	Yes

Table 9. Timer Interrupt Masks

Timer Interrupt Mask (IMT1, IMT2, IMT3, IMT4)	Interrupt Requests
0	Enable
1	Disable (mask)

Table 10. Serial Interrupt Request Flag

Serial Interrupt Request Flag (IFS1, IFS2)	Interrupt Requests
0	No
1	Yes

Table 11. Serial Interrupt Mask

Serial Interrupt Mask (IMS1, IMS2)	Interrupt Requests
0	Enable
1	Disable (mask)

Low Power Dissipation Mode

The MCU has two low power dissipation modes: standby mode and stop mode (table 12). Figure 9 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter, and serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 12. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition					Input/Output Pin	Timer/Counter, Serial Interface	Recovery Method
		Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM			
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ²	Active	RESET input, interrupt request
Stop mode	STOP instruction	Stop	Stop	RESET ¹	Stop	Retained	High impedance	Stop	RESET input

- Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to tables 1 and 2 for the contents of the flags and registers.
 2. If an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

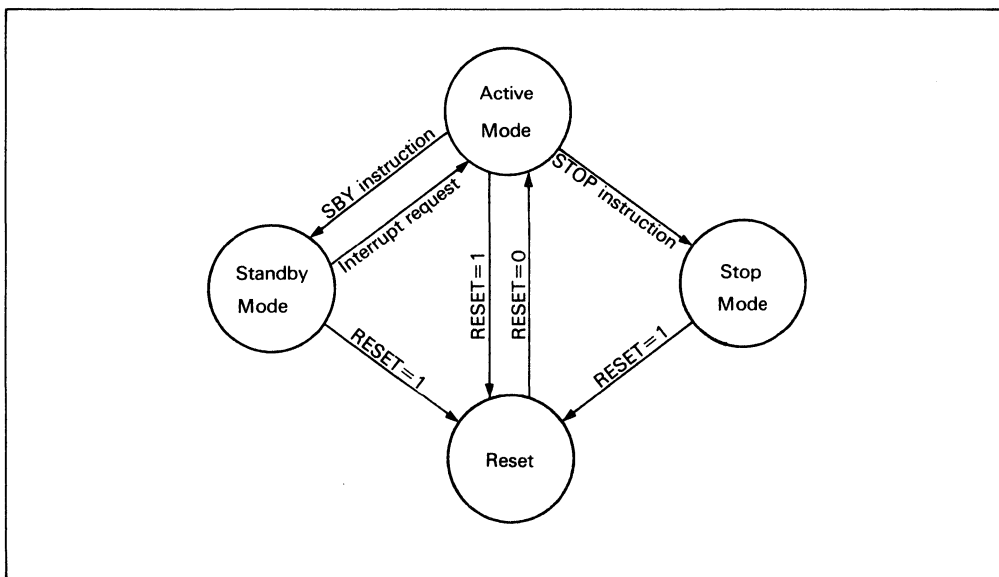


Figure 9. MCU Operation Mode Transition

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. If the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 10 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stops.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 11, reset input must be applied for at least t_{RC} to stabilize oscillation. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, registers B, W, X/SPX, and Y/SPY, carry, and serial data register do not retain their contents.

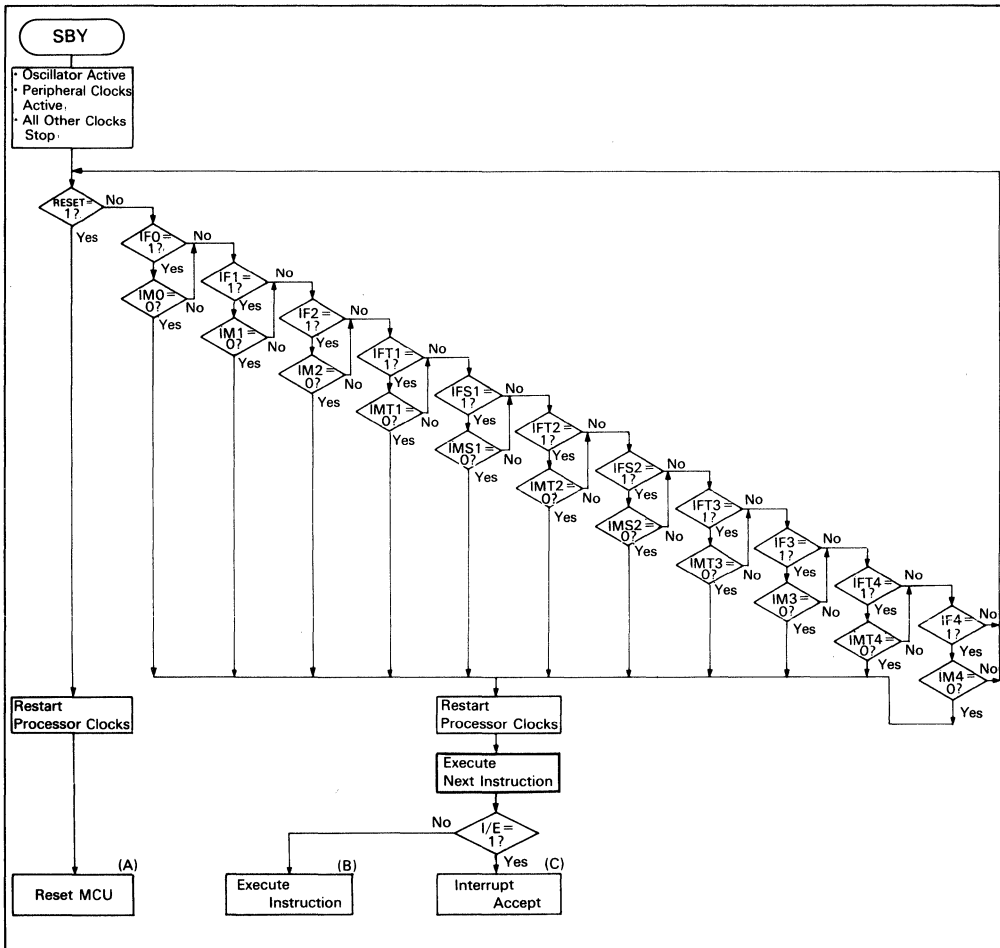


Figure 10. MCU Operating Flowchart in Standby Mode



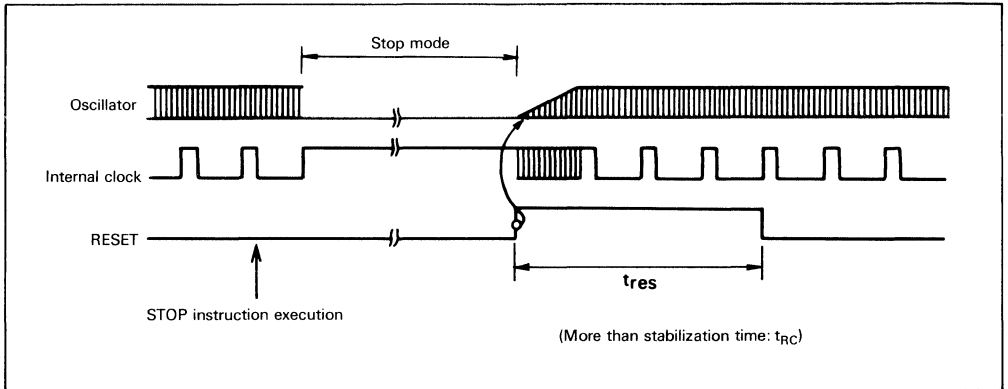


Figure 11. Timing Chart of Recovering from Stop Mode

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. Crystal oscillator or ceramic filter oscill-

ator can be selected as the oscillator type. Refer to table 13 to select the type. In addition, see figure 13 for layout of the crystal or ceramic filter.

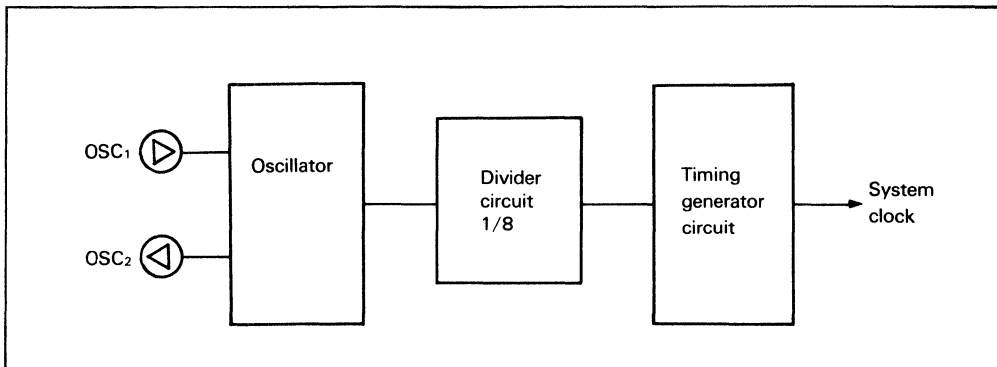


Figure 12. Internal Oscillator Circuit

Table 13. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation	<p>Oscillator</p>	
Ceramic Filter Oscillator		<p>Ceramic filter CSA8.00MT (Murata) R_f: 1 MΩ ± 20% C₁: 30 pF ± 20% C₂: 30 pF ± 20%</p>
Crystal Oscillator		<p>R_f: 1 MΩ ± 20% C₁: 10-22 pF ± 20% C₂: 10-22 pF ± 20% Crystal: equivalent to circuit shown C₀: 7 pF max. R_S: 100 Ω max. f: 1.0–9.0 MHz</p>

- Notes: 1. Since the circuit constant changes according to the crystal and ceramic filter resonator and stray capacitance of the board, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameters.
2. Wiring among OSC₁, OSC₂, and elements should be as short as possible, and never cross other wiring. Refer to figure 13.

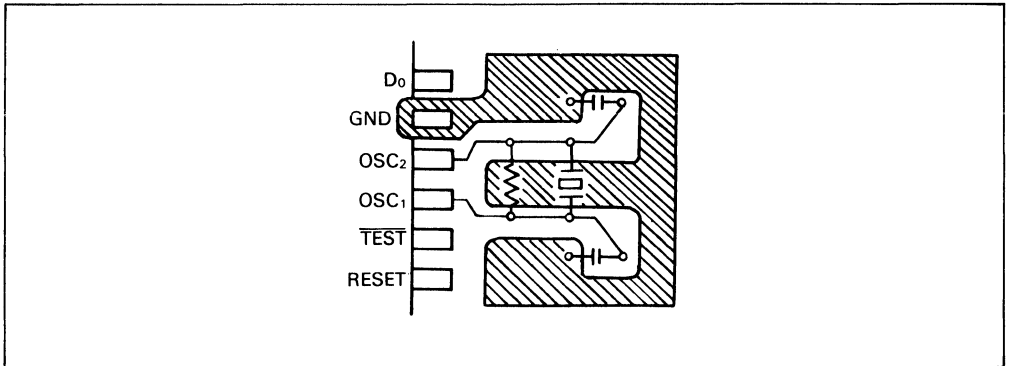


Figure 13. Layout of Crystal and Ceramic Filter

Input/Output

The MCU provides 58 I/O pins. Each port provides a data direction register (DDR). Each bit of ports D, R3, R4, R5, R6, R8, R9 can be individually programmed as an input or as an output. Ports R0, R1, R2, RA can be individually programmed as input or as an output. Port R7 is a 4-bit input only port.

Port D: Port D consists of 16 high-current I/O pins. Each bit of port D can be individually programmed as an input or as an output by port D data direction register (DDR0-DDR3) (0 = input, 1 = output). Port D becomes an input port at MCU reset. Port D can be set/reset by SED/RED and SEDD/REDD instruction, and tested by TD/TDD instruction. The data direction register can be set or reset either by SEM/REM instruction or SEMD/REMD instruction.

Port R: Ports R0-R9 are 4-bit I/O ports. Port RA is a 2-bit I/O port.

Ports R0, R1, R2: Ports R0, R1, and R2 are 4-bit I/O ports. Each port can be individually programmed as an input or as an output by the port R data direction register (RDR) (0 = input, 1 = output). Ports R0, R1, R2 become input ports at the MCU reset. These ports receive data by LAR/LBR instruction and transmit data by LRA/LRB instruction. The data direction register can be set/reset either by SEM/REM instruction or SEMD/REMD instruction.

Port R3: Port R3 is a 4-bit I/O port. Each bit of port R3 can be individually programmed as an input or as an output by the port R3 data direction register (R3DR) (0 = input, 1 = output). Port R3 becomes an input port at MCU reset.

Note that port R3 is multiplexed with external interrupt input pins (\overline{INT}_0 , \overline{INT}_1 , \overline{INT}_2 , \overline{INT}_3). These pins can be used as interrupt input pins when the data direction register of the appropriate bit is automatically reset with an interrupt enable bit of the port mode register (PMR) been set.

Port R3 receive data by LAR/LBR instruction, and transmits data by LRA/LRB instruction. The data direction register can be reset either by SEM/REM instruction or SEMD/REMD instruction.

Port R4: Port R4 is a 4-bit I/O port. Each bit of port R4 can be individually programmed as an input or as an output by port R data direction register (R4DR) (0 = input, 1 =

output). Port R4 becomes an input port at MCU reset.

Note that pins R4₀, R4₁, R4₂ of port R4 are multiplexed with SCK₁, SI₁, SO₁ of the serial interface 1, respectively. R4₃ is multiplexed with the reference voltage input (V_{ref}) for comparator input.

Port R4 receive data by LAR/LBR instruction, and transmits data by LRA/LRB instruction. The data direction register can be set/reset either by SEM/REM instruction or SEMD/REMD instruction.

Port R5: Port R5 is a 4-bit I/O port. Each bit of port R5 can be individually programmed as an input or as an output by port R5 data direction register (R5DR) (0 = input, 1 = output). Port R5 becomes an input port at MCU reset.

Note that port R5 is multiplexed with external interrupts (\overline{INT}_4 , \overline{INT}_5), timer inputs (\overline{TI}_1 , \overline{TI}_2), and timer outputs (TO₁, TO₂). (R5₀/ \overline{INT}_4 / \overline{TI}_1 , R5₁/ \overline{INT}_5 / \overline{TI}_2 , R5₂/TO₁, R5₃/TO₂). \overline{TI}_1 and \overline{TI}_2 become clock input pins when timer is used as an event counter. TO₁ and TO₂ becomes clock output pins of timers 1 and 2, respectively. These pins transmit clocks (with appropriate cycles) and PWM output signals through the use of the reload function.

Port R5 receives data by LAR/LBR instruction, and transmits data by LRA/LRB instruction. The data direction register can be set/cleared by SEM/REM instruction, or SEMD/REMD instruction.

Port R6: Port R6 is a 4-bit I/O port. Each bit of port R6 can be individually programmed as an input or as an output by programming the port R6 data direction register (R6DR) (0 = input, 1 = output). Port R6 becomes an input port at MCU reset.

R6₀ is multiplexed with TO₃. R6₁, R6₂, R6₃ are multiplexed with SCK₂, SI₂, SO₂ of the serial interface, respectively.

Port R6 receives data by LAR/LBR instruction, and transmits data by LRA/LRB instruction. The data direction register can be set/cleared by SEM/REM instruction or SEMD/REMD instruction.

Port R7 (analog input port): Port R7 is a 4-bit port which provides the digital input and analog input operation modes. These modes are available to each bit by programming the analog mode register (AMR).

In the digital input mode, port R7 is available as an input-only port with characteristics equivalent to other I/O ports. In the analog input mode, port R7 reads the comparison result between the reference voltage which is input by $R4_3/V_{ref}$ and the input voltage of port, as an input data.

In the analog input mode, direct current constantly flows in the analog comparator to assure its characteristics. Thus the MCU consumes power in the analog input mode. The power consumption cannot be reduced even with the reduction of the operation cycle. Therefore, you should not put port R7 into the analog input mode, except when analog comparison is required. In this case, 2 instruction cycles are required after R7 goes into the analog input mode until the analog comparator is stabilized to read the precise data. Therefore, read the data after at least 2 instruction cycles after you put R7 into the analog input mode. The analog comparator holds its state in the standby mode, but stops operating in the stop mode.

Ports R8, R9: Ports R8 and R9 are 4-bit I/O ports. These ports are standard I/O ports for the HD404418 and HD4074418, and high-voltage ports which can apply 12.8 V max voltage for the HD4074408.

I/O direction is specified by the port 8 data direction register (R8DR) and port 9 data direction register (R9DR) on a bit basis (0 = input, 1 = output). Ports 8 and 9 become inputs at reset since the registers are cleared by reset input.

Ports R8 and R9 receive data by LAR/LBR instruction, and transmit data by LRA/LRB instruction. The data direction register can be set/reset by SEM/REM instruction or SEMD/REMD instruction.

Port RA: Port RA is a 2-bit I/O port. Port RA can be programmed as an input or as an output by port R data direction register (RDR) (0 = input, 1 = output). The RDR is cleared at MCU reset, then becomes an input port.

Port RA receives data by LAR/LBR instruction, and transmits data by LRA/LRB instruction. The data direction register can be set/reset by SEM/REM instruction, or SEMD/REMD instruction.

Data Direction Register (\$006-\$00F, \$026): The 4-bit write-only data direction registers (DDR0-DDR3, RDR, R3DR-R9DR) (table 14) control input/output selection of

the I/O port. Each bit of ports D, R3-R6, R8, R9 can be individually programmed as an input or as an output by the DDR for each bit.

Ports R0-R2, RA can be individually programmed as input or as output by the DDR for each port.

When functioning as an input port, each port reads data from pins. When functioning as an output port, each port reads data from the data register. Thus, the MCU reads the transmitted data precisely even when the output is changing.

Each DDR is reset to 0 at MCU reset. Then each port becomes an input port immediately after the MCU reset. To use as an output port, set the DDR to 1 in the initialize routine of the program.

Port D Data Direction Register (DDR0: \$006, DDR1: \$007, DDR2: \$008, DDR3: \$009): Each bit of port D can be individually programmed as an input or as an output port. Port D becomes an input port at MCU reset (figure 14).

Port R Data Direction Register (RDR: \$026): Ports R0, R1, R2, RA can be individually programmed as an input or as an output. When reset, each port becomes an input port (figure 15).

Ports R3-R9 Data Direction Register (R3DR: \$00A, R4DR: \$00B, R5DR: \$00C, R6DR: \$00D, R8DR: \$00E, R9DR: \$00F): Each bit of ports R3-R9 can be individually programmed as an input port. Each port becomes an input at MCU reset (figure 16).

I/O Circuit Configuration: The basic port I/O circuit type is CMOS. (R7 is an input circuit, RA an NMOS open-drain I/O circuit.) See table 15.

Ports 8 and 9 are CMOS I/O circuits for the HD404418 and HD4074418, NMOS open-drain I/O circuits for the HD4074408.

The direction of any type of I/O pin can be controlled by the data direction register.

To prevent floating input pins on the HD404418, a pull-up MOS can be attached to I/O circuits (D₀-D₁₅, R0-R6) via mask option. It can be selected for any pin. For the HD4074418 and HD4074408, all circuits are specified as without pull-up MOS. See figures 17-19 for circuit configurations.

Table 14. Data Direction Register (DDR)

DDR	Port Condition
0	Input Port (Output Buffer Off)
1	Output Port (Output Buffer On)

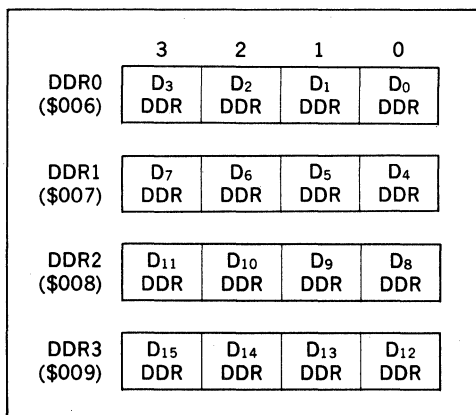


Figure 14. Port D Data Direction Register

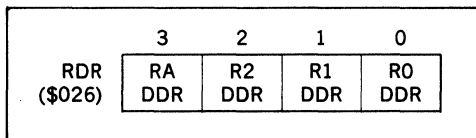


Figure 15. Port R Data Direction Register

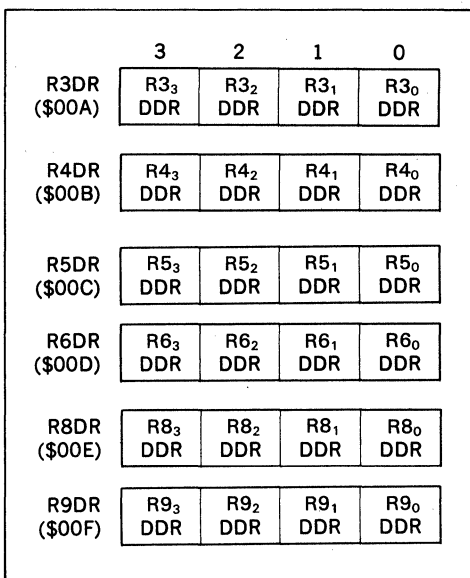


Figure 16. Ports R3-R9 Data Direction Register

Table 15. I/O Pin Circuit Type (Cont)

I/O Pins	Circuit	Applied Pins		
		HD404418	HD4074418	HD4074408
Standard Pins		R7 ₀ - R7 ₃	R7 ₀ - R7 ₃	R7 ₀ - R7 ₃
		$\overline{\text{INT}}_0, \overline{\text{INT}}_1, \overline{\text{INT}}_2,$ $\overline{\text{INT}}_3, \overline{\text{INT}}_4, \overline{\text{INT}}_5$ $\overline{\text{T}}_1, \overline{\text{T}}_2, \text{S}1, \text{S}2$	$\overline{\text{INT}}_0, \overline{\text{INT}}_1$ $\overline{\text{INT}}_2, \overline{\text{INT}}_3$ $\overline{\text{INT}}_4, \overline{\text{INT}}_5$ $\overline{\text{T}}_1, \overline{\text{T}}_2$ $\text{S}1, \text{S}2$	$\overline{\text{INT}}_0, \overline{\text{INT}}_1$ $\overline{\text{INT}}_2, \overline{\text{INT}}_3$ $\overline{\text{INT}}_4, \overline{\text{INT}}_5$ $\overline{\text{T}}_1, \overline{\text{T}}_2$ $\text{S}1, \text{S}2$
	<p>(With Pull-up MOS)</p>	$\overline{\text{INT}}_0, \overline{\text{INT}}_1, \overline{\text{INT}}_2,$ $\overline{\text{INT}}_3, \overline{\text{INT}}_4, \overline{\text{INT}}_5$ $\overline{\text{T}}_1, \overline{\text{T}}_2, \text{S}1, \text{S}2$	$\overline{\text{INT}}_0, \overline{\text{INT}}_1$ $\overline{\text{INT}}_2, \overline{\text{INT}}_3$ $\overline{\text{INT}}_4, \overline{\text{INT}}_5$ $\overline{\text{T}}_1, \overline{\text{T}}_2$ $\text{S}1, \text{S}2$	
Output Pins		$\text{S}0_1, \text{S}0_2$ $\text{TO}_1, \text{TO}_2, \text{TO}_3$	$\text{S}0_1, \text{S}0_2$ $\text{TO}_1, \text{TO}_2, \text{TO}_3$	$\text{S}0_1, \text{S}0_2$ $\text{TO}_1, \text{TO}_2, \text{TO}_3$
High-Voltage Pins				$\text{R}8_0 - \text{R}8_3$ $\text{R}9_0 - \text{R}9_3$

- Notes: 1. Either without pull-up MOS or with pull-up MOS can be specified for each pin via mask option. (Circuit with pull-up MOS is provided only for the HD404418.)
2. HLT signal becomes 0 in stop mode. Then I/O pins and output pins are in high-impedance state, and all pull-up MOSs turn off.
3. When serial clock registers bits 2 are 1, pins R4₀/SCK₁ and R6₃/SCK₂ become SCK₁ and SCK₂ outputs respectively when SCK₁ and SCK₂ internal clock enable signals are set to 0 by putting the serial clock registers in transfer clock output mode. The pins become SCK₁ and SCK₂ outputs when SCK₁ and SCK₂ internal clock signals are set to 1 by putting the serial clock registers in transfer clock input mode.
4. When SCI₁ and SCI₂ are set to transmit or transmit/receive mode, SCI₁, SCI₂ transmit enable signal becomes 1, then SO₁ and SO₂ pins become outputs. Pins TO₁-TO₃ become output if the timer output registers 1-3 are set to timer output state or PWM active state.

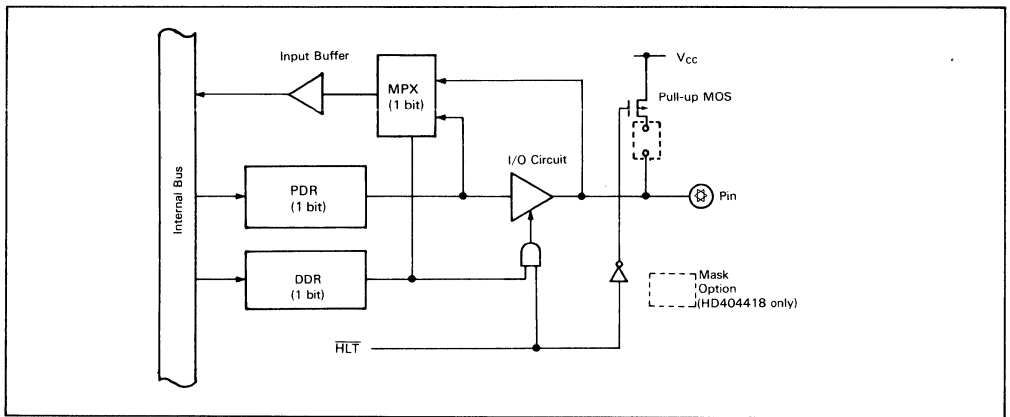


Figure 17. Ports D, R3-R6, R8, R9 Configuration

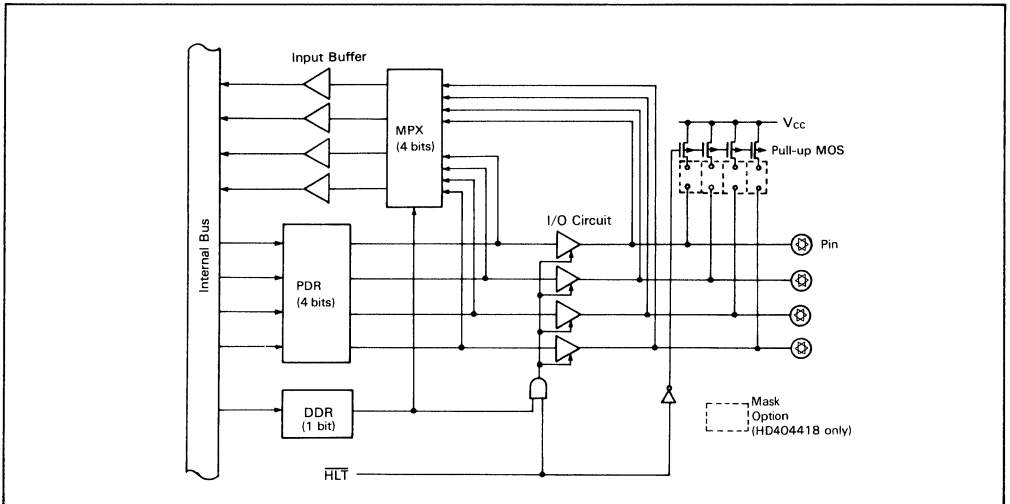


Figure 18. Ports R0-R2, RA Configuration

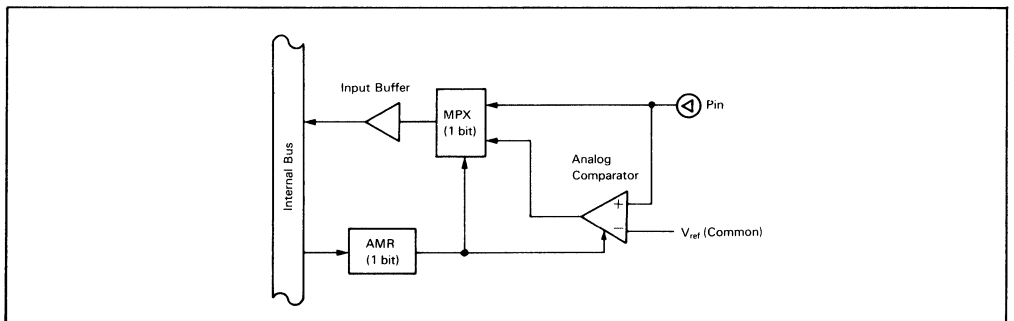


Figure 19. Port R7 Configuration

Pin Function Control: Several pins are multiplexed with the timer or serial interface I/O pins. The functions of these pins are controlled by the corresponding mode registers.

Port Mode Register (PMR: \$027): The port mode register is a 4-bit write-only register which controls pins R3₀/ $\overline{\text{INT}}_0$, R3₁/ $\overline{\text{INT}}_1$, R3₂/ $\overline{\text{INT}}_2$ and R3₃/ $\overline{\text{INT}}_3$ as shown in table 16. The port mode register is initialized to \$0 by MCU reset. These pins are therefore used as ports.

IF₀ or IF₁ is set if R3₀/ $\overline{\text{INT}}_0$ or R3₁/ $\overline{\text{INT}}_1$ is low when you set bit 0 or bit 1 of the port mode register. IF₂ or IF₃ is set if R3₂/ $\overline{\text{INT}}_2$, or R3₃/ $\overline{\text{INT}}_3$ are high when you set bit 2 or bit 3 of

the port mode register. Keep this in mind when you use external interrupts.

Analog Mode Register (AMR: \$025): The analog mode register is a 4-bit write-only register. Each bit controls the operation modes of R7₀-R7₃ inputs (table 16). The data direction register of R4₃ is automatically reset when analog input mode is selected by setting a bit of the analog mode register. Then the analog comparator receives the reference voltage (V_{ref}) of the analog input.

Note that all bits of the analog mode register are initialized to 0 at MCU reset. Thus, pins R7₀-R7₃ go into the digital input mode at the MCU reset.

Table 16. Pin Function Control

PMR (Port Mode Register: \$027)

	Bit 3	Bit 2	Bit 1	Bit 0
Pin	R3 ₃ / $\overline{\text{INT}}_3$	R3 ₂ / $\overline{\text{INT}}_2$	R3 ₁ / $\overline{\text{INT}}_1$	R3 ₀ / $\overline{\text{INT}}_0$
Bit=0	R3 ₃	R3 ₂	R3 ₁	R3 ₀
Bit=1	$\overline{\text{INT}}_3$	$\overline{\text{INT}}_2$	$\overline{\text{INT}}_1$	$\overline{\text{INT}}_0$

AMR (Analog Mode Register: \$025)

	Bit 3	Bit 2	Bit 1	Bit 0
Pin	R7 ₃	R7 ₂	R7 ₁	R7 ₀
Bit=0	Digital	Digital	Digital	Digital
Bit=1	Analog	Analog	Analog	Analog

AMR (Analog Mode Register : \$025)

Bit 3-0	R4 ₃ /V _{ref}
0 0 0 0	R4 ₃
not 0 0 0 0	V _{ref}

SMR 1 (Serial Mode Register 1: \$010)

	Bit 2	Bit 1	Bit 0
Pin	R4 ₀ / $\overline{\text{SCK}}_1$	R4 ₁ /SI ₁	R4 ₂ /SO ₁
Bit=0	R4 ₀	R4 ₁	R4 ₂
Bit=1	$\overline{\text{SCK}}_1$	SI ₁	SO ₁

SMR 2 (Serial Mode Register 2: \$014)

	Bit 2	Bit 1	Bit 0
Pin	R6 ₃ / $\overline{\text{SCK}}_2$	R6 ₂ /SI ₂	R6 ₁ /SO ₂
Bit=0	R6 ₃	R6 ₂	R6 ₁
Bit=1	$\overline{\text{SCK}}_2$	SI ₂	SO ₂

Serial Mode Registers (SMR1: \$010, SMR2: \$014): The serial mode registers are 4-bit read/write registers which control pins R40/SCK₁, R63/SCK₂, R41/SI₁, R62/SI₂, R42/SO₁, and R61/SO₂ as shown in table 16. For details, refer to the serial interface section.

Timer Mode Registers (TMR1: \$018, TMR2: \$01C): The timer mode registers are 4-bit write-only registers which control pins R50/INT₄/TI₁ and R51/INT₅/TI₂ as shown in Table 16. For details, refer to the timer section.

Timer Output Registers (TOR1: \$019, TOR2: \$01D, TOR3: \$021): The timer output registers are 4-bit read/write registers which control pins R50/INT₄/TI₁, R51/INT₅/TI₂, R52/TO₁, R53/TO₂, and R60/TO₃ as shown in Table 16. For details, refer to the timer section.

Unused I/O Pins: If unused I/O pins left floating, the LSI may malfunction because of noise. To prevent this, unused pins should be dealt with as follows:

Standard I/O pins: Pull up to V_{CC} through about 100 kΩ resistor.

Standard input pins: Connect to V_{CC}.

High-voltage pins: Connect to GND.

Table 16. Pin Function Control (Cont)

TMR1 (Timer Mode Register 1: \$018)

Bit 2-0	R50/INT ₄ /TI ₁
not 1 1 1	R50/INT ₄
1 1 1	TI ₁

TMR2 (Timer Mode Register 2: \$01C)

Bit 2-0	R51/INT ₅ /TI ₂
not 1 1 1	R50/INT ₅
1 1 1	TI ₂

TOR1 (Timer Output Register 1: \$019)

Bit 3	R50/INT ₄ /TI ₁
0	R50/TI ₁
1	INT ₄

Bit			R52/TO ₁
2	1	0	
0	0	0	R5 ₂
0	0	1	TO ₁
0	1	0	
0	1	1	
1	x	x	

TOR2 (Timer Output Register 2: \$01D)

Bit 3	R51/INT ₅ /TI ₂
0	R51/TI ₂
1	INT ₅

Bit			R53/TO ₂
2	1	0	
0	0	0	R5 ₃
0	0	1	TO ₂
0	1	0	
0	1	1	
1	x	x	

TOR3 (Timer Output Register 3: \$021)

Bit			R60/TO ₃
2	1	0	
0	0	0	R6 ₀
0	0	1	TO ₃
0	1	0	
0	1	1	
1	x	x	

Note: x = Don't care

Unused pins must retain the state of reset in the program. The program should not change DDR and register values.

Timer

The MCU contains a prescaler and 4 timers/counters (timers 1-4). Figures 20 and 21 show their block diagrams.

Timers 1-3 are versatile timers/counters providing the following functions: free-running timers/counters, reload timers/counters, and pulse width modulation (PWM) circuit, etc. The functions are controllable by software. Each timer provides a timer output pin which permits the MCU to transmit the clock signal with an appropriate cycle in combination with the reload function and the PWM output. Timer 4 is a free-running counter which is also available as a watchdog timer (WDT) provided with a hardware reset function selectable by mask option.

Prescaler: The input clock to the prescaler is a system clock signal. The prescaler is initialized to \$000 at MCU reset, then it starts to count up the system clock signals. The prescaler keeps counting up except at MCU reset and the stop mode. Prescaler outputs provide timer input clocks and serial interface transfer clocks. Their divide ratios can be selected by the timer mode registers (TMR1-TMR4), and the serial clock registers (SCR1, SCR2), respectively.

Timers 1-3 Operation: Timers 1-3 are versatile timers provided with following functions: free-running timers, event counters, reload timers, and PWM circuit. The functions are controllable by software and selectable by the timer mode registers (TMR1, TMR2, TMR3) and the timer output registers (TOR1, TOR2, TOR3) for each timer.

The timers/counters (TC1-TC3) count up with every input clock after they have been initialized at MCU reset. When used as timers/counters, the clock divided by the prescaler is available as an input clock. When used as an event counter, external clock is available. When selecting external clock input, an interrupt enable bit in the timer output register must be reset in order to disable the external interrupt (timer 3 does not have an external clock input).

The timer interrupt request flags (IFT1, IFT2, IFT3) are set with the input clock supply after timer counter has become \$FF. When auto-reload function is not selected, timers 1-3 become free-run timers/event counters, and

restart counting up after they have been reinitialized to \$00. When you select auto-reload function, timers 1-3 become reload timers, and the data in the timer load registers (TL1R, TL2R, TL3R) are reloaded into the timer/counter with the input clock supply after the timer/counter reaches \$FF. Then timers 1-3 starts counting up.

Timers 1-3 also provide a timer output circuit, which affects the output level when the input clock supply after timer counter has become \$FF. This circuit can transmit a clock signal (with an appropriate cycle) in combination with the reload timer. When you select PWM function by the timer output register, PWM output is available. PWM output transmits high during the clock cycle specified in the timer load register (1 cycle = 1 timer input clock \times 256), and transmits low otherwise. To obtain a voltage level in proportion to the timer load register value, combine PWM output with a lowpass filter.

Timer 4 Operation: Timer 4 is an 8-bit free-running/watchdog timer. When timer 4 is used as a free-running timer, 8 clocks divided by the prescaler can be selected as input clocks. Timer 4 is initialized to \$00 at MCU reset, then counts up every input clock signal. If a clock signal is applied after the timer becomes \$FF, the timer returns to \$00, then continue counting. At the same time the timer interrupt request flag is set.

When timer 4 is used as a watchdog timer, input clock is specified as the 1/2048 output divided by the prescaler. The watchdog timer is initialized to \$00 at MCU reset, then counts up every input clock signal. If a clock signal is applied after the timer becomes \$FF, an overflow is generated and hardware reset function is enabled for the MCU.

After reset, the MCU re-executes the program from the beginning. Therefore, to operate the system normally, the program should set the watchdog timer reset bit in a cycle shorter than 2^{19} . The program resets the MCU at overflow generation if the MCU malfunctions because of noise. This function is effective for improving system reliability.

Timer 4 function of the HD404418 is selected via mask option. For the HD4074418 and HD4074408, watchdog timer versions are provided in addition to free-running timer versions.

Note that the type names of the watchdog timer versions differ from that of the free-running timer versions.



Timer Mode Registers 1-3 (TMR1: \$018, TMR2: \$01C, TMR3: \$020): The 4-bit write-only timer mode registers 1-3 select the auto-reload function, the prescaler divide ratio, and the source of the input clock signal (table 17). The timer mode registers 1-3 are initialized to \$0 at MCU reset.

Users can change the data in the timer mode register after the second instruction cycle of writing into the timer mode registers 1-3. Initialize timers 1-3 by programming the timer load register after the data of the TMR are changed.

Note that timer 3 does not provide an event input pin. Therefore, timer 3 is unavailable as an event counter.

Timer Mode Register 4 (TMR: \$024): The timer mode register 4 is a write only register. The function differs depending on the timer 4 function. When timer 4 functions as a free-running counter, bits 0-2 affects the operation of timer 4 (table 18). When users select watchdog timer by mask option, bit 3 affects the timer 4 (watchdog timer) operation.

Timer Output Registers (TOR1: \$019, TOR2: \$01D, TOR3: \$021) The timer output registers are 4-bit read/write registers which control timer 1-3 output mode, PWM output selection, and external interrupts multiplexed with timer input pin (table 19).

When bits 0 and 1 of the timer output registers go into any mode other than timer output inhibit mode, the pins become timer output pins automatically. These modes are

Table 17. Timer Mode Register 1-3

TMR1, TMR2, TMR3	
Bit 3	Auto-Reload Function
0	No
1	Yes

TMR1, TMR2, TMR3			
Prescaler Divide Ratio			Clock Input Source
Bit 2	Bit 1	Bit 0	
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\bar{T}1_1, T1_2$ (External event inputs)

Note: External event input is unavailable, as timer 3 does not provide an event input pin. If you select external event input at timers 1, 2, ports R5₀, R5₁ data direction registers are automatically reset, then become inputs.

Table 18. Timer Mode Register 4

TMR4	
Bit 3	Function
0	Does not affect the watchdog timer operation
1	Watchdog timer is reset, then restarts counting up from \$00

Note: Bit 3 is available when timer 4 is functioning as a watchdog timer. When timer 4 is functioning as a free-running counter, bit 3 is unavailable.

TMR4			
Bit 2	Bit 1	Bit 0	Prescaler Divide Ratio
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Note: Bits 0-2 are available when timer 4 is functioning as a free-running timer. When timer 4 is functioning as a watchdog timer, they are independent of timer 4 operation.



available for transmitting clock signals (with appropriate cycles and duties) in combination with each mode of timers 1-3. When you select the PWM output, timer output pin becomes PWM output independent of timer output mode.

The data of the timer output register changes after the second instruction cycle of writing into the timer output register. The timer output register 3 becomes a 3-bit register without bit 3, because timer 3 does not provide an event input pin.

Timers 1-3 (TC1L: \$01A, TC1U: \$01B, TL1L: \$01A, TL1U: \$01B, TC2L: \$01E, TC2U: \$01F, TL2L: \$01E, TL2U: \$01F, TC3L: \$022, TC3U: \$023, TL3L: \$022, TL3U: \$023): Timers 1-3 consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each of them

provides low order digits (TC1L: \$01A, TC2L: \$01E, TC3L: \$022), and high-order digits (TC1U: \$01B, TC2U: \$01F, TC3U: \$023). Refer to figure 20.

The timer/event counter can be initialized by programming the timer load register. In this case, write the low-order digits first, then the high-order digits. The timer/event counter is initialized according to the timer load register value when the high-order digit is written. The timer load register is initialized to \$00 at MCU reset.

The counter value of timers 1-3 can be obtained by reading the timer/event counter. In this case, read the high-order digit first, then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

Table 19. Timer Output Register

TOR1, TOR2

Bit 3	\overline{INT}_4 , INT ₅ External Interrupts
0	Inhibits the \overline{INT}_4 , INT ₅ external interrupts
1	Enables the \overline{INT}_4 , INT ₅ external interrupts

Note: Port R5₀, R5₁ data direction registers are automatically reset when bits 3 of the TOR1 and TOR2 are set, then become inputs.

TOR1, TOR2, TOR3

Bit 2	PWM Function
0	Normal timer operation
1	PWM operation, transmits data from TO ₁ , TO ₂ , TO ₃

Note: The data direction register for ports R5₂, R5₃, R6₀ are automatically set when bits 2 of TOR1, TOR2, and TOR3 are set, then become outputs.

TOR1, TOR2, TOR3

Bit 1	Bit 0	Timer Output Mode
0	0	Inhibits timer output
0	1	Transmits 1 synchronously with timer overflow output (Toggle output mode)
1	0	Transmits reverse level synchronously with timer output (1 output mode)
1	1	Transmits 0 synchronously with timer overflow output (0 output mode)

Note: The data direction registers for ports R5₂, R5₃, R6₀ are automatically set when bits 0 and 1 for TOR1, TOR2, TOR3 are other than 00.



Operation Mode of Timers 1-3: Timers 1-3 provide the following 3 timer functions: free-running, reload, and PWM. Internal/external clock input and the absence/presence of the timer output are also selectable. The combination of these functions are available for selecting a variety of operation modes.

Table 20 describes the combinations of timers 1-3 operation mode selection. Select the operation mode according to this table in order to set the appropriate data to the timer mode register and the timer output register. Figure 22 illustrates an example of timer output waveform. Note that output

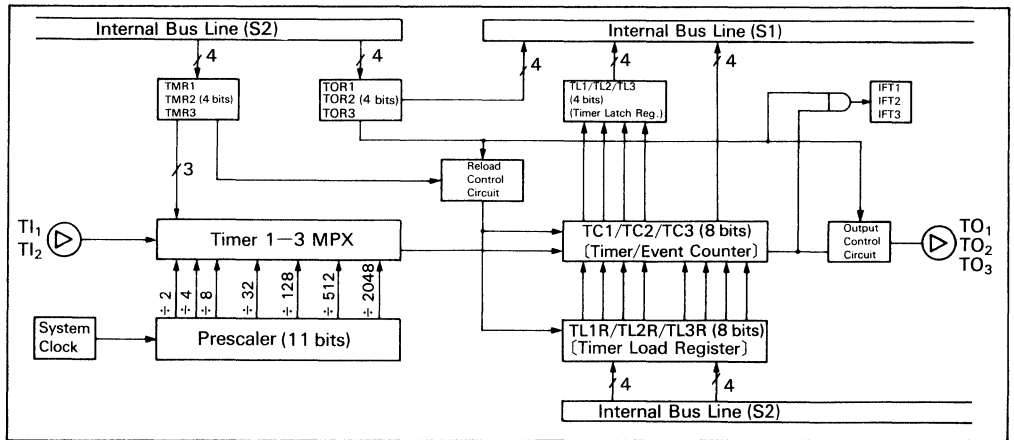


Figure 20. Timer 1-3 Block Diagram

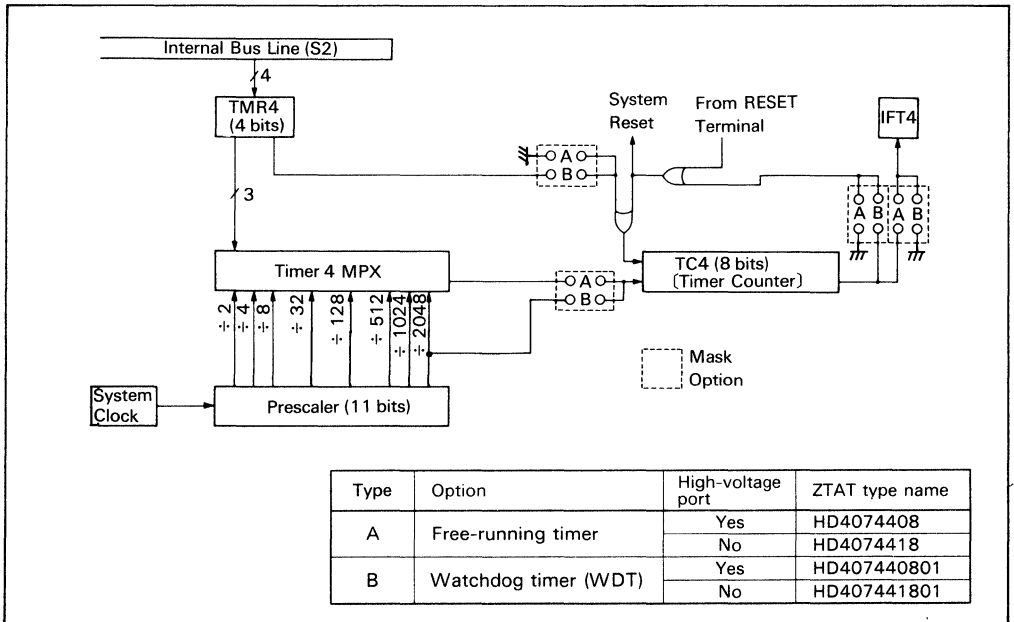


Figure 21. Timer 4 Block Diagram



waveform differs depending on operation modes.

Table 20. Combinations of Timer 1-3 Operation Modes

TMR1, TMR2, TMR3				TOR1, TOR2, TOR3				Timer Input Pin	Timer Output Pin	Timer 1-3 Function
Bit 3	Bit 2	Bit 1	Bit 0	Bit 3	Bit 2	Bit 1	Bit 0			
0	Note 3	Note 3	Note 3	0	0	0	0	R5 ₀ ,R5 ₁	R5 ₂ ,R5 ₃ ,R6 ₀	Free-Running
0	Note 3	Note 3	Note 3	0	0	Note 2	Note 2	R5 ₀ ,R5 ₁	TO ₁ ,TO ₂ ,TO ₃	Timer
0	Note 3	Note 3	Note 3	1	0	0	0	$\overline{\text{INT}}_4$,INT ₅	R5 ₂ ,R5 ₃ ,R6 ₀	
0	Note 3	Note 3	Note 3	1	0	Note 2	Note 2	$\overline{\text{INT}}_4$,INT ₅	TO ₁ ,TO ₂ ,TO ₃	
0	1	1	1	0	0	0	0	$\overline{\text{T}}_1$,T _{l2}	R5 ₂ ,R5 ₃ ,R6 ₀	Event Counter
0	1	1	1	0	0	Note 2	Note 2	$\overline{\text{T}}_1$,T _{l2}	TO ₁ ,TO ₂ ,TO ₃	
1	Note 3	Note 3	Note 3	0	0	0	0	R5 ₀ ,R5 ₁	R5 ₂ ,R5 ₃ ,R6 ₀	Reload Timer
1	Note 3	Note 3	Note 3	0	0	Note 2	Note 2	R5 ₀ ,R5 ₁	TO ₁ ,TO ₂ ,TO ₃	
1	Note 3	Note 3	Note 3	1	0	0	0	$\overline{\text{INT}}_4$,INT ₅	R5 ₂ ,R5 ₃ ,R6 ₀	
1	Note 3	Note 3	Note 3	1	0	Note 2	Note 2	$\overline{\text{INT}}_4$,INT ₅	TO ₁ ,TO ₂ ,TO ₃	
1	1	1	1	0	0	0	0	$\overline{\text{T}}_1$,T _{l2}	R5 ₂ ,R5 ₃ ,R6 ₀	Event Counter (With
1	1	1	1	0	0	Note 2	Note 2	$\overline{\text{T}}_1$,T _{l2}	TO ₁ ,TO ₂ ,TO ₃	Reload Function)
Note 1	Note 3	Note 3	Note 3	0	1	Note 1	Note 1	R5 ₀ ,R5 ₁	TO ₁ ,TO ₂ ,TO ₃	PWM (Note 4)
Note 1	Note 3	Note 3	Note 3	1	1	Note 1	Note 1	$\overline{\text{INT}}_4$,INT ₅	TO ₁ ,TO ₂ ,TO ₃	
Note 1	1	1	1	0	1	Note 1	Note 1	$\overline{\text{T}}_1$,T _{l2}	TO ₁ ,TO ₂ ,TO ₃	PWM (External Clock) (Note 4)

- Notes: 1. Don't care
 2. One of or both of bits 0 and 1 of TOR is 1
 3. Bit 0, 1, and 2 of TMR are not 111
 4. When PWM output is selected, timer functions in the same way as the free-running timer by initializing the timer load register to \$00.

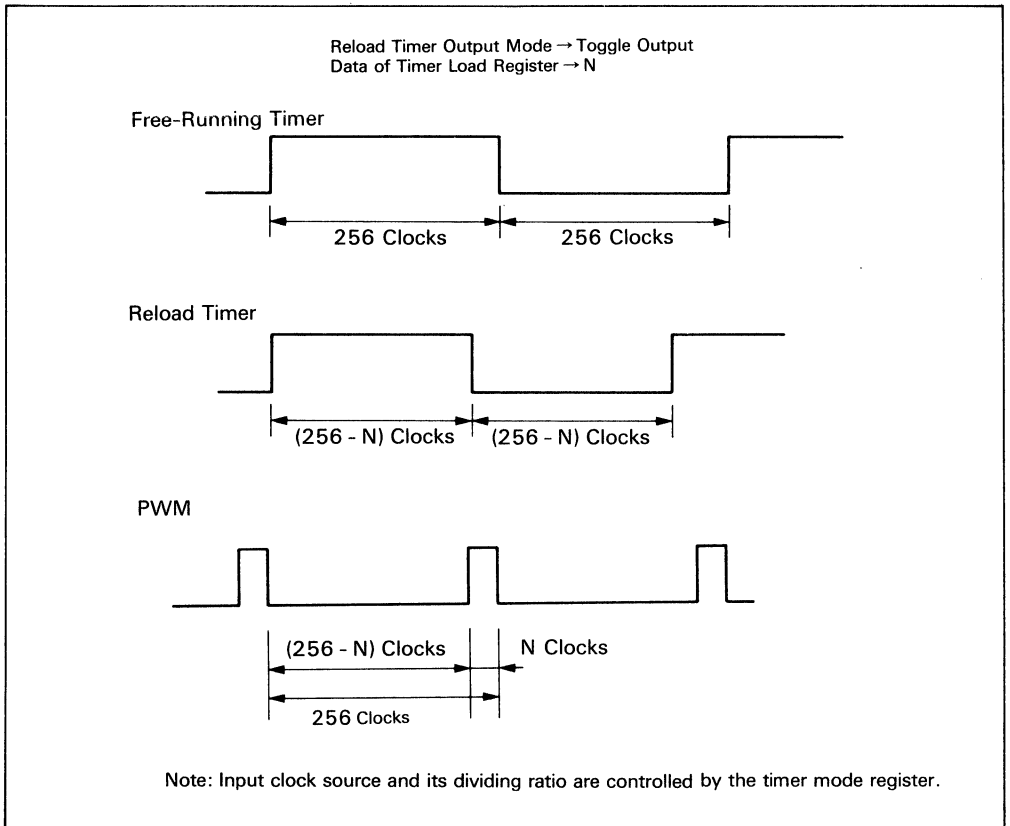


Figure 22. Timer Output Waveform Examples

Serial Mode Register (SMR1: \$010, SMR2: \$014): The serial mode register is a 4-bit read/write register, which controls the serial interface operation, \overline{SCK}_1 , \overline{SCK}_2 , SI₁, SI₂, SO₁, SO₂ (table 21).

The write signal to the serial mode register initializes the internal state of the serial interface. The write signal stops the transfer clock supply to the serial data register and the octal counter, resetting the octal counter to \$0 simultaneously. Thus, the write signal to the serial mode register causes the data transfer to quit and the serial interrupt request flag to be set while the serial interface is operating.

Data in the serial mode register can be changed in the second instruction cycle after writing into the serial mode register. Therefore, program the serial interface to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register is initialized to \$0 at MCU reset.

Bit 3 of the serial mode register is an enable bit of the serial interface. Set the enable bit before executing the STS instruction. To activate both serial interfaces, set the enable bits of both serial interfaces, then execute the single STS instruction. An enable bit is automatically reset by STS instruction execution.

Table 21. Serial Mode Register

SMR1, SMR2

Bit 3	STS instruction
0	Disable
1	Enable

Note: Bit 3 of the SMR1 and SMR2 are automatically reset by STS instruction.

SMR1, SMR2

Bit 2	R4 ₀ / \overline{SCK}_1 , R6 ₃ / \overline{SCK}_2
0	Used as ports R4 ₀ , R6 ₃ I/O pin
1	Used as \overline{SCK}_1 , \overline{SCK}_2 input or output

Note: When the internal clocks are selected, ports R4₀ and R6₃ data direction registers are automatically set by bit 2 of the SMR1 and SMR2 set, then become outputs. When the external clocks are selected, ports R4₀ and R6₃ data direction registers are automatically reset by bit 2 of the SMR1 and SMR2 set, then become inputs.

SMR1, SMR2

Bit 1	R4 ₁ /SI ₁ , R6 ₂ /SI ₂
0	Used as ports R4 ₁ , R6 ₂ I/O pin
1	Used as SI ₁ , SI ₂ input pin

Note: Ports R4₁, R6₂ data direction registers are automatically reset by bit 1 of SMR1 and SMR2 set, then become inputs.

SMR1, SMR2

Bit 0	R4 ₂ /SO ₁ , R6 ₁ /SO ₂
0	Used as ports R4 ₂ , R6 ₁ I/O pin
1	Used as SO ₁ , SO ₂ output pin

Note: Ports R4₂, R6₁ data direction registers automatically set by bit 0 of the SMR1 and SMR2 set, then become outputs.

Serial Clock Register (SCR1: \$011, SCR2: \$015): The serial clock register is a 3-bit write only register which controls the transmit clock source and the prescaler divide ratio (table 22).

The write signal to the serial clock register initializes the internal state of the serial interface. Transfer clock supply to the serial data register and the octal counter is stopped by programming the serial clock register, then the octal counter is reset. Thus, data transfer is stopped and interrupt request flag is set by programming the serial clock register during serial interface operation.

Serial Data Register (SR1L: \$012, SR2L: \$016, SR1U: \$013, SR2U: \$017): The serial data register is an 8-bit read/write register

consisting of low-order digits (SR1L, SR2L) and the high-order digits (SR1U, SR2U).

The data in the serial data register is transmitted LSB first at SO₁, SO₂ synchronously with the falling edge of the transfer clock signal. At the same time, the serial data register receives external data LSB first at SI₁, SI₂ synchronously with the rising edge of the transfer clock. Figure 24 shows the I/O timing chart for the transfer clock signal and the data.

The validity of the data contents cannot be assured when writing/reading the serial data register during data transfer. Therefore, write/read the serial data register after completing data transfer.

Table 22. Serial Clock Register

SCR1, SCR2

Bit 2	Bit 1	Bit 0	R4 ₀ /SCK ₁ R6 ₃ /SCK ₂	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio
0	0	0	SCK ₁ , SCK ₂ output	Prescaler	2048	4096
0	0	1	SCK ₁ , SCK ₂ output	Prescaler	512	1024
0	1	0	SCK ₁ , SCK ₂ output	Prescaler	128	256
0	1	1	SCK ₁ , SCK ₂ output	Prescaler	32	64
1	0	0	SCK ₁ , SCK ₂ output	Prescaler	8	16
1	0	1	SCK ₁ , SCK ₂ output	Prescaler	2	4
1	1	0	SCK ₁ , SCK ₂ output	System clock		1
1	1	1	SCK ₁ , SCK ₂ input	External clock		

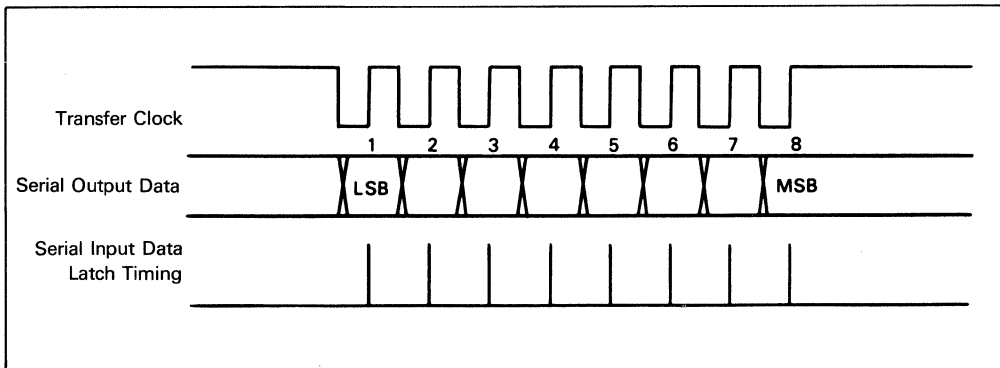


Figure 24. Serial Interface I/O Timing Chart



Selection of the Operation Modes: Table 23 shows the operation modes of the serial interface. Set the serial mode register according to this table.

Operating State of the Serial Interface: The serial interfaces provide 4 operation states (figure 25).

When the serial interface has been initialized, the MCU is in transfer inhibit state in which STS instruction and the transfer clocks are both ignored.

Set the enable bit of the serial interface to put the serial interface into the STS waiting state in which serial data transfer is available by executing STS instruction. Two serial interfaces operate simultaneously with a single STS instruction when the enable bits of serial interfaces 1 and 2 are both set.

In the SCK waiting state, the falling edge of the first transfer clock puts the serial interface into the transfer state, while the octal counter counts up and the serial data register shifts simultaneously. If the clock continuous output mode is selected, the serial interface stays in the SCK waiting state while continuously transmitting transfer clocks.

The octal counter is initialized to 000 by 8 transfer clocks in the transfer state, and the serial interrupt request flag is set. When the internal transfer clock is selected, the MCU goes into the transfer inhibit state. When the external clock is selected, the MCU goes into the transfer clock waiting state. The octal counter is initialized to \$000, transfer is suspended, and the interrupt request flag is set simultaneously by programming the serial mode register or serial clock register in the transfer state or the transfer inhibit state.

An Example of Transfer Clock Error Detection: The serial interface malfunctions when the transfer clock is disturbed by external noise. In this case, the transfer clock error can be detected by the procedure shown in figure 26.

If more than eight transfer clocks are applied by external noise in the SCK waiting state, the state of the serial interface shifts in the following sequence: first, transfer state (for 1 to 7 transfer clocks), second, SCK waiting state (at 8th transfer clock), and third, back to transfer state. To set the serial interrupt flag again after resetting it, program the serial mode register to put the MCU into the STS waiting state.

Table 23. Serial Interface Operation Mode

SMR1, SMR2

Bit 2	Bit 1	Bit 0	Serial Interface Operation Mode
1	0	0	Clock continuous output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

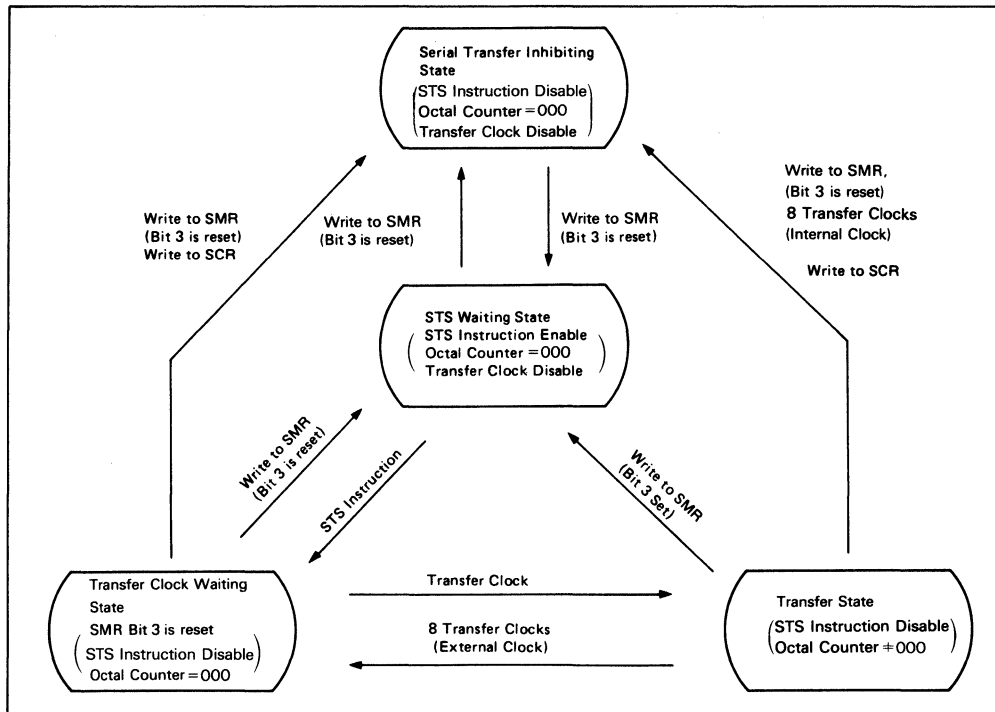


Figure 25. Serial Interface Operation State

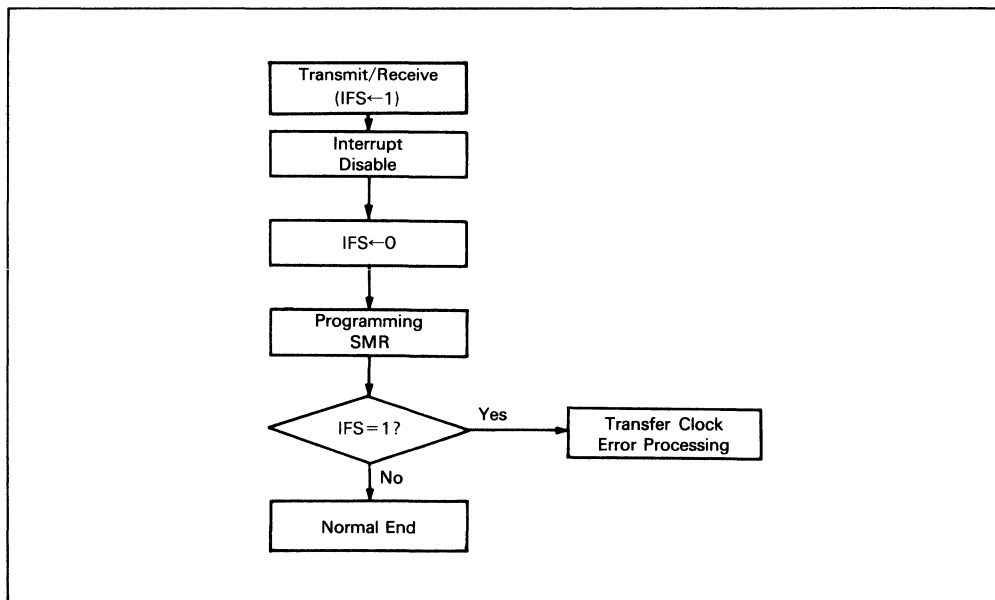


Figure 26. Example of Transfer Clock Error Detection

PROM Mode Pin Description

Table 24 and figure 27 describe the pin functions in PROM mode.

Table 24. PROM Mode Signals

Pin No.			MCU mode		PROM mode		Pin No.			MCU mode		PROM mode	
DC-64S DP-64S	FP-64	FP-64A	Symbol	I/O	Symbol	I/O	DC-64S DP-64S	FP-64	FP-64A	Symbol	I/O	Symbol	I/O
1	59	57	D ₁₁	I/O	V _{CC}		33	27	25	R4 ₀ /SCK ₁	I/O		
2	60	58	D ₁₂	I/O			34	28	26	R4 ₁ /SI ₁	I/O		
3	61	59	D ₁₃	I/O			35	29	27	R4 ₂ /SO ₁	I/O		
4	62	60	D ₁₄	I/O	A ₁₃	I	36	30	28	R4 ₃ /V _{ref}	I/O		
5	63	61	D ₁₅	I/O	A ₁₄	I	37	31	29	R7 ₀	I	\overline{CE}	I
6	64	62	RO ₀	I/O	A ₁	I	38	32	30	R7 ₁	I	\overline{OE}	I
7	1	63	RO ₁	I/O	A ₂	I	39	33	31	R7 ₂	I	\overline{MO}	I
8	2	64	RO ₂	I/O	A ₃	I	40	34	32	R7 ₃	I	\overline{MI}	I
9	3	1	RO ₃	I/O	A ₄	I	41	35	33	R8 ₀	I/O		
10	4	2	R1 ₀	I/O	A ₅	I	42	36	34	R8 ₁	I/O		
11	5	3	R1 ₁	I/O	A ₆	I	43	37	35	R8 ₂	I/O		
12	6	4	R1 ₂	I/O	A ₇	I	44	38	36	R8 ₃	I/O		
13	7	5	R1 ₃	I/O	A ₈	I	45	39	37	R9 ₀	I/O		
14	8	6	R2 ₀	I/O	A ₀	I	46	40	38	R9 ₁	I/O		
15	9	7	R2 ₁	I/O	A ₁₀	I	47	41	39	R9 ₂	I/O		
16	10	8	R2 ₂	I/O	A ₁₁	I	48	42	40	R9 ₃	I/O		
17	11	9	R2 ₃	I/O	A ₁₂	I	49	43	41	RESET	I	RESET	I
18	12	10	RA ₀	I/O	V _{PP}		50	44	42	\overline{TEST}	I	\overline{TEST}	I
19	13	11	RA ₁	I/O	A ₉	I	51	45	43	OSC ₁	I		
20	14	12	R3 ₀ / \overline{INT} ₀	I/O			52	46	44	OSC ₂	O		
21	15	13	R3 ₁ / \overline{INT} ₁	I/O			53	47	45	GND	I/O	GND	
22	16	14	R3 ₂ /INT ₂	I/O			54	48	46	D ₀	I/O	O ₀	I/O
23	17	15	R3 ₃ /INT ₃	I/O			55	49	47	D ₁	I/O	O ₁	I/O
24	18	16	R5 ₀ / \overline{INT} ₄ / \overline{TI} ₁	I/O			56	50	48	D ₂	I/O	O ₂	I/O
25	19	17	R5 ₁ /INT ₅ /TI ₂	I/O			57	51	49	D ₃	I/O	O ₃	I/O
26	20	18	R5 ₂ /TO ₁	I/O			58	52	50	D ₄	I/O	O ₄	I/O
27	21	19	R5 ₃ /TO ₂	I/O			59	53	51	D ₅	I/O	O ₅	I/O
28	22	20	R6 ₀ /TO ₃	I/O			60	54	52	D ₆	I/O	O ₆	I/O
29	23	21	R6 ₁ /SO ₂	I/O			61	55	53	D ₇	I/O	O ₇	I/O
30	24	22	R6 ₂ /SI ₂	I/O			62	56	54	D ₈	I/O		
31	25	23	R6 ₃ /SCK ₂	I/O			63	57	55	D ₉	I/O		
32	26	24	V _{CC}		V _{CC}		64	58	56	D ₁₀	I/O	V _{CC}	

(Note) I/O : Input/Output Pins
 I : Input Pins
 O : Output Pins

HD404418/HD4074418/HD4074408

V_{PP} (Program Voltage)

V_{PP} is the input for the program voltage (12.5 V ± 0.3 V) for programming the PROM.

\overline{CE} (Chip Enable)

\overline{CE} is the input for programming and verifying internal PROM.

\overline{OE} (Output Enable)

\overline{OE} is the input for the data output control signal for PROM verify.

A₀–A₁₄ (Address Bus)

A₀–A₁₄ are address input pins for internal PROM.

O₀–O₇ (PROM Data Bus)

O₀–O₇ are the data bus for internal PROM.

\overline{M}_0 , \overline{M}_1 (Mode)

\overline{M}_0 and \overline{M}_1 set PROM mode. PROM mode is set when \overline{M}_0 , \overline{M}_1 , and TEST pins are low level and RESET pin is high level.

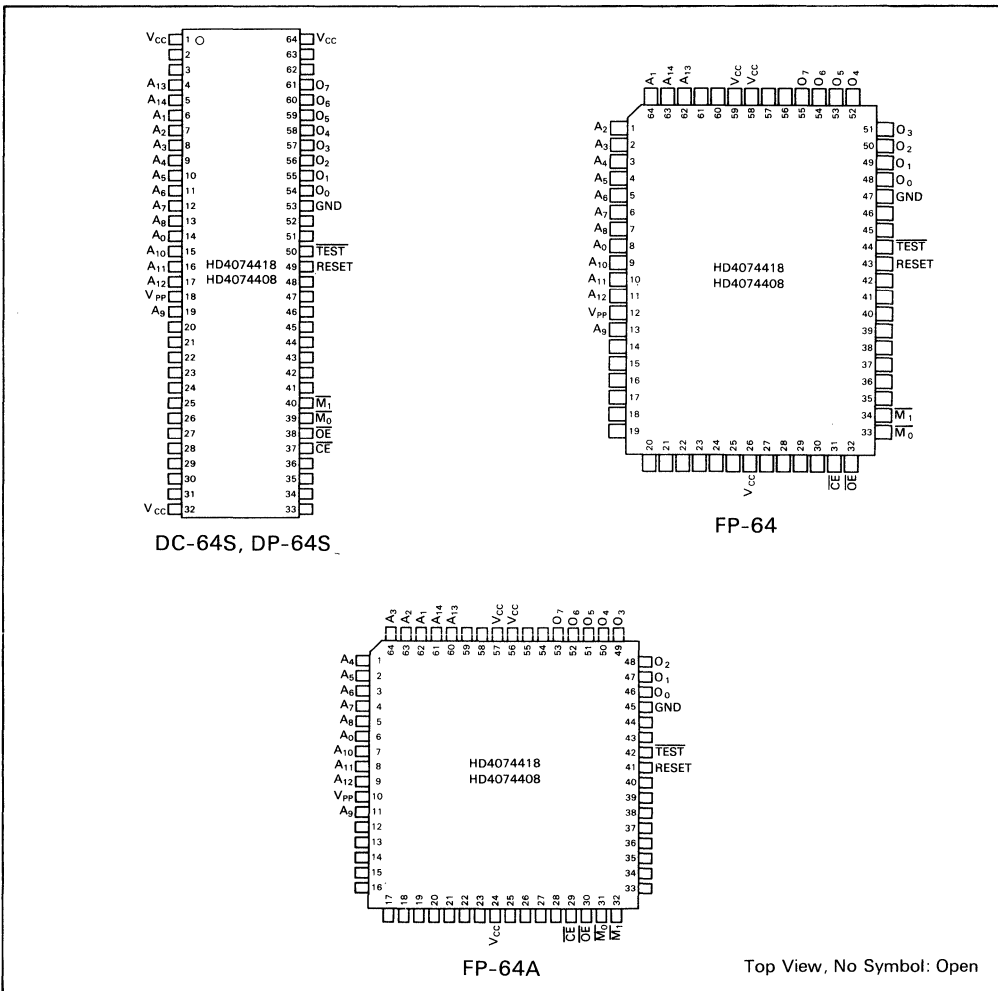


Figure 27. PROM Mode Pin Arrangement



Programmable ROM Operation

The MCU on-chip PROM is programmed in PROM mode (figures 27-29). PROM mode is set by bringing TEST, M₀, and M₁ low, and RESET high as shown in figure 28. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 64-to-28-pin socket adapter. Table 26 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series MCU incorporates a conversion circuit to enable use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits, as shown in figure 29. For example, if 8 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 25 shows how programming and verification modes are selected.

Figure 30 is a programming flowchart, and figure 42 is a timing chart.

Ehasing

The PROMs in ceramic window packages can

be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are : ultraviolet (UV) light with wavelength 2537Å with a minimum irradiation of 15 W·s/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. Addresses \$0000 to \$3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.) Data in unused addresses must be set to \$FF.
2. Be sure that the PROM programmer, socket adapter and LSI lineup (pin 1 positions match). Using the wrong programmer or socket adapter may cause an over-voltage and damage the LSI (table 26). Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Table 25. PROM Mode Selection

Mode	Pin		V _{PP}	O ₀ -O ₇
	CE	OE		
Programming	Low	High	V _{PP}	Data input
Verify	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance

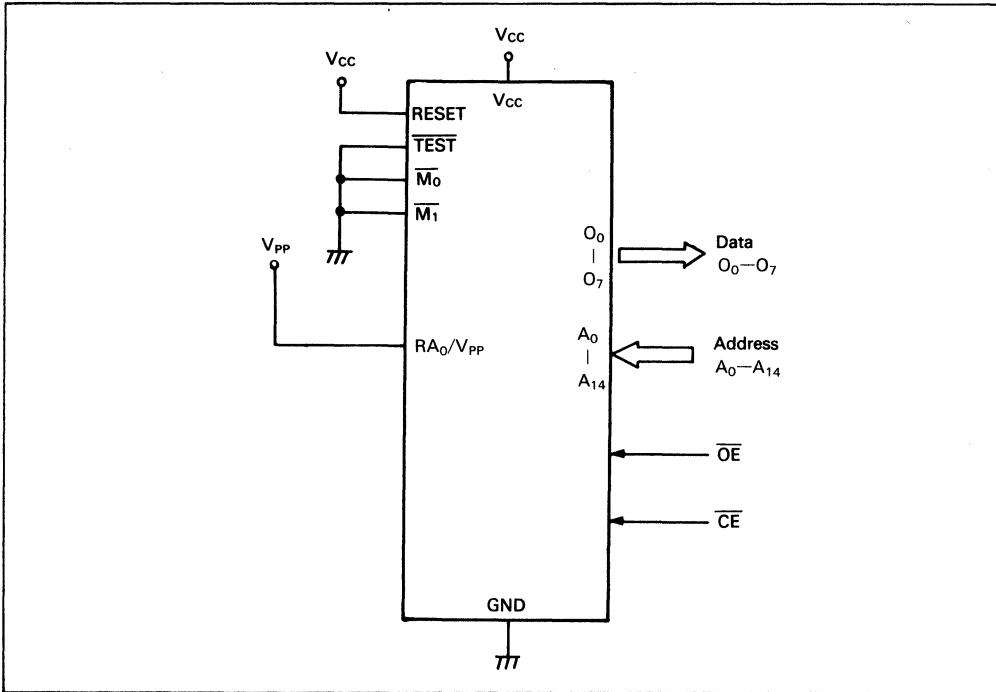


Figure 28. PROM Mode Function Diagram

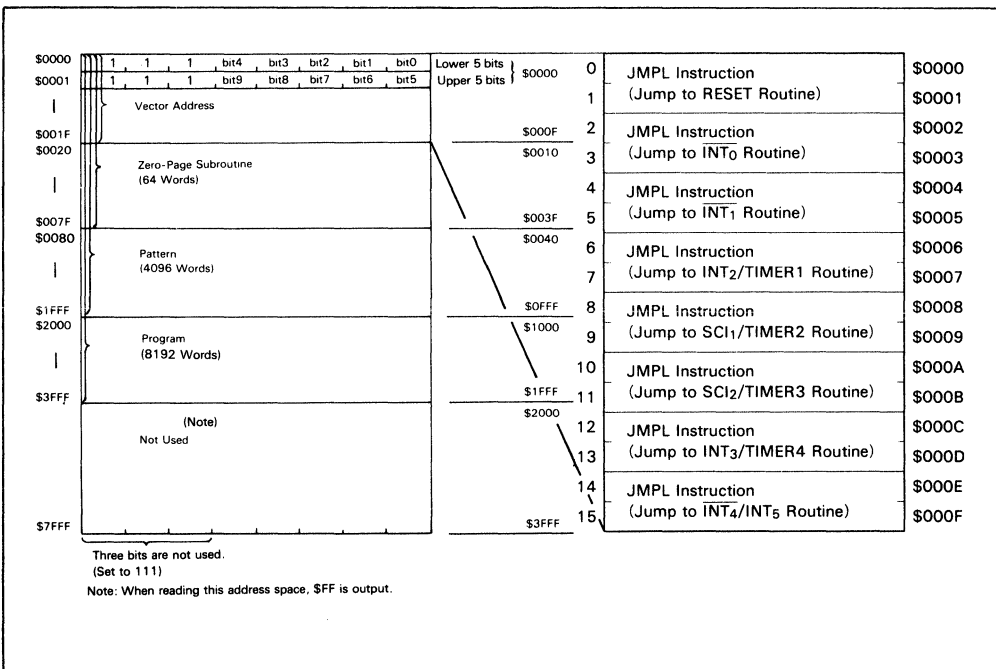


Figure 29. PROM Mode Memory Map



Table 26. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type Name	Maker	Type Name	Package
DATA I/O	22B	Hitachi	HS448ESS11H	DP-64S
	29B		HS440ESF01H	FP-64
			HS440ESF03H	FP-64A
AVAL Corp	PKW-1000	Hitachi	HS448ESS21H	DP-64S
			HS440ESF01H	FP-64
			HS440ESF03H	FP-64A

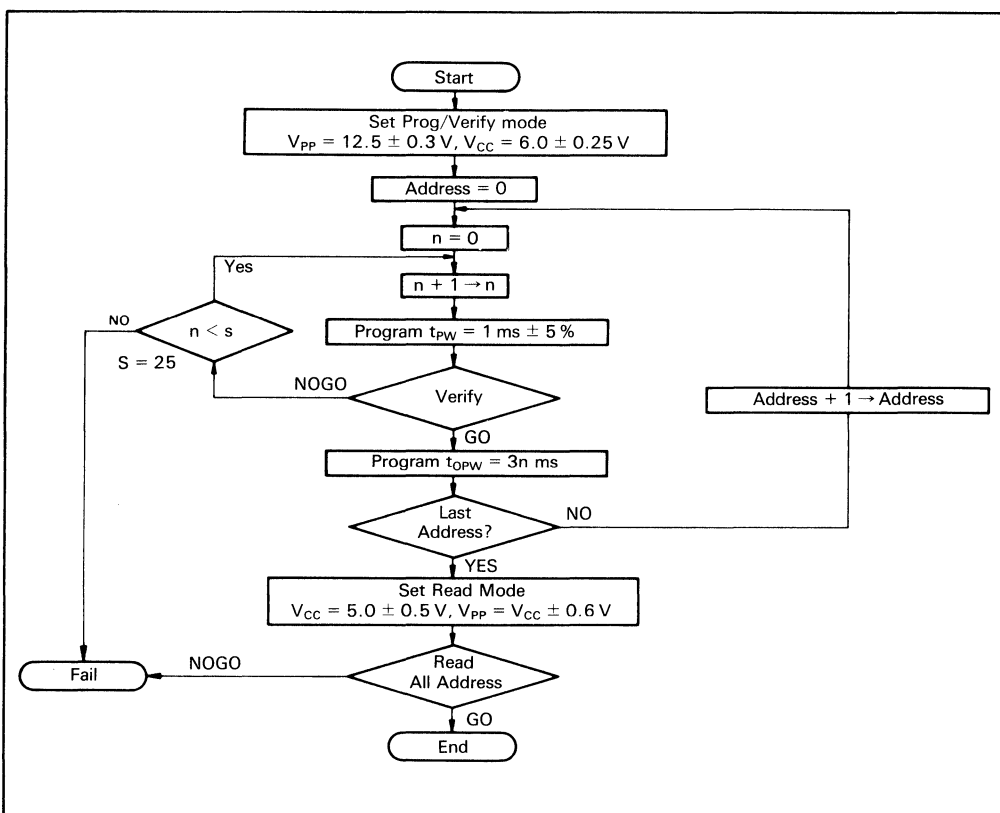


Figure 30. High-Speed Programming Flowchart

ZTAT MCU On-Chip PROM Characteristics and Precautions

Principles of Programming/Erasing: The ZTAT micros' memory cells are the same as an EPROM's. Therefore they are programmed by applying high voltage to control gates and drains, which injects hot electrons into the floating gate. They are stable, surrounded by an energy barrier of SiO₂ film. Such a cell becomes a 0 bit due to the memory threshold voltage change. A cell with no condensed electrons at its floating gate appears as a 1 bit (figure 31).

The electron charge in memory cells may

decrease as time goes by. This can be caused by:

- Ultraviolet light: discharged by photo-emitted electrons (erasure principle)
- Heat: discharged by thermal emitted electrons
- High voltage: discharged by a high electric field at the control gate or drain

If the oxide film covering a floating gate is defective, the erasure rate is great. Normally, electron erasure does not occur, because such defective devices are found and removed during testing.

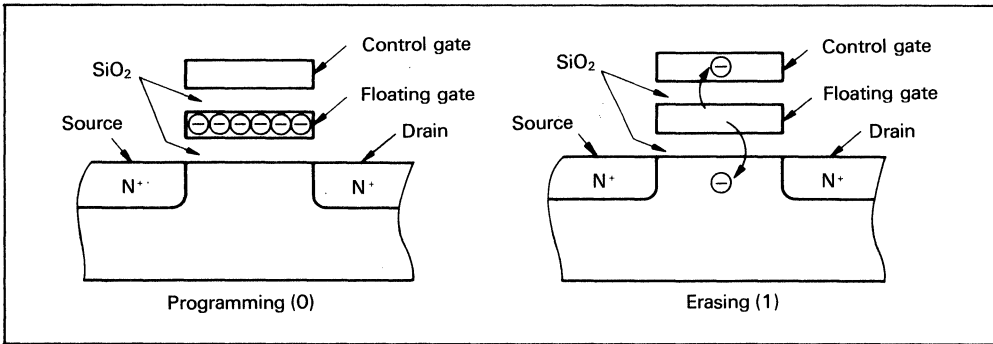


Figure 31. Cross-section of EPROM Memory Cell

Programming Precautions: The EPROM memory cells should be programmed under specific voltage and timing conditions. The higher the program voltage and the longer the program pulse is applied, the more electrons will be injected into the floating gate. However, if an overvoltage is applied to V_{PP} , the p-n junction may be permanently damaged. Pay particular attention to PROM programmer overshoot. Negative voltage noise will cause a parasitic transistor effect, which may reduce break-down voltage.

The ZTAT micros are connected electrically to the PROM programmer through a socket adapter. Therefore, pay attention to the following:

- Confirm that the socket adapter is firmly fixed on the PROM programmer.

- Do not touch the socket adapter or the LSI during programming.

- Misprogramming can be caused by poor contacts.

On-Chip EPROM Reliability after Programming: Generally, semiconductors are reliable except for initial failures. Parts can be screened to avoid failures. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold characteristics are high. Exposing the LSI to 150°C after user programming can effectively upgrade these characteristics. Figure 32 shows the recommended screening flow.

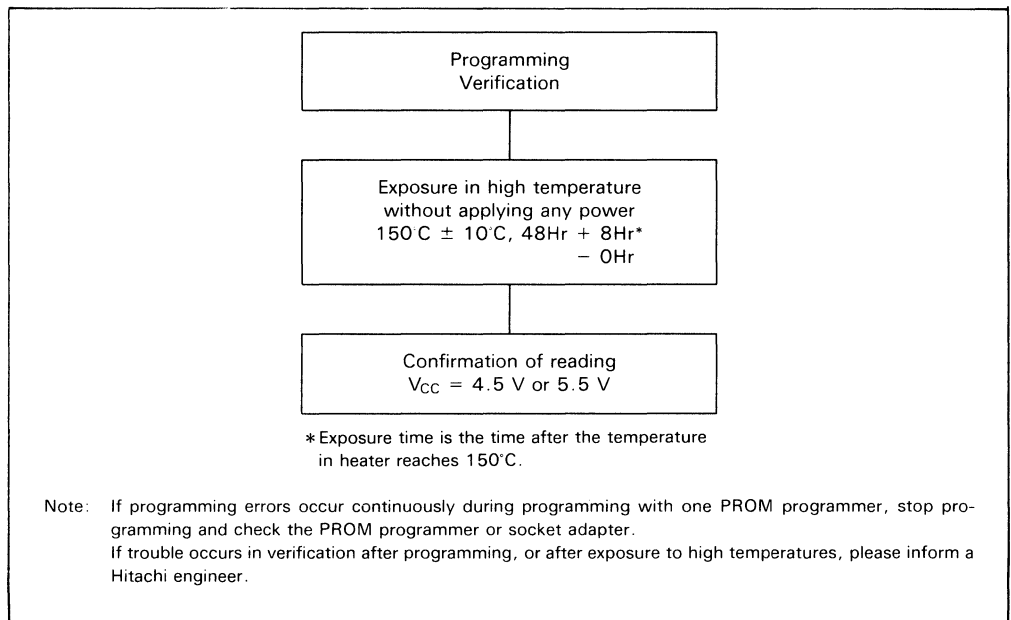


Figure 32. Recommended Screening Flow

RAM Addressing Mode

As shown in figure 33, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: Contents of registers W, X, and Y (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 addresses; from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 34.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR instruction is on a page boundary (256n + 255) (figure 35), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when BR is used on a page boundary. The HMCS400-series cross macro assembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero-page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6 bits of immediate data are placed in the low-order 6 bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order 8 bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and register B.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 36). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and register B. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port data registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and register B and also to the R1 and R2 port data registers at the same time.

The P instruction has no effect on the program counter.

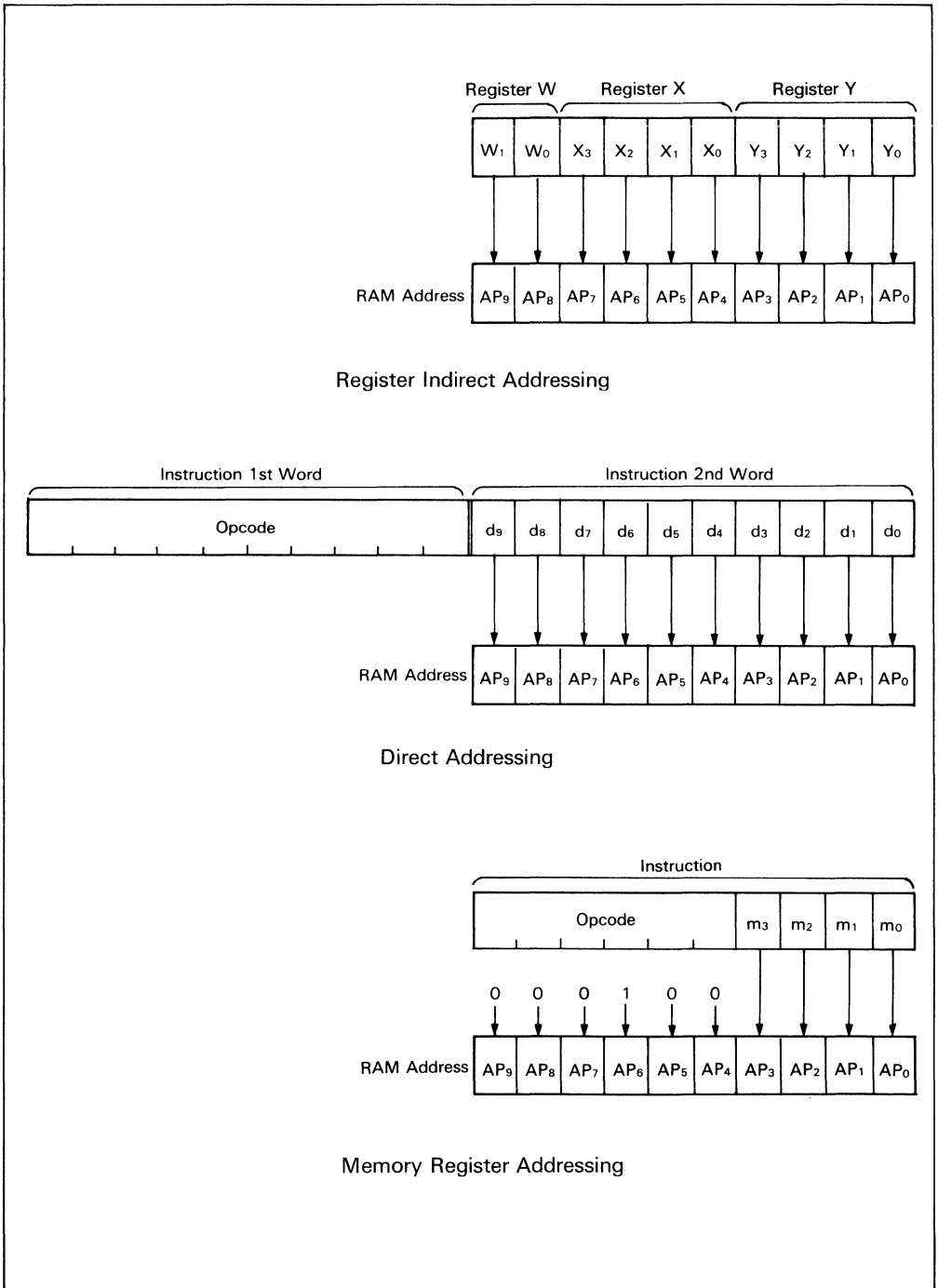


Figure 33. RAM Addressing Modes

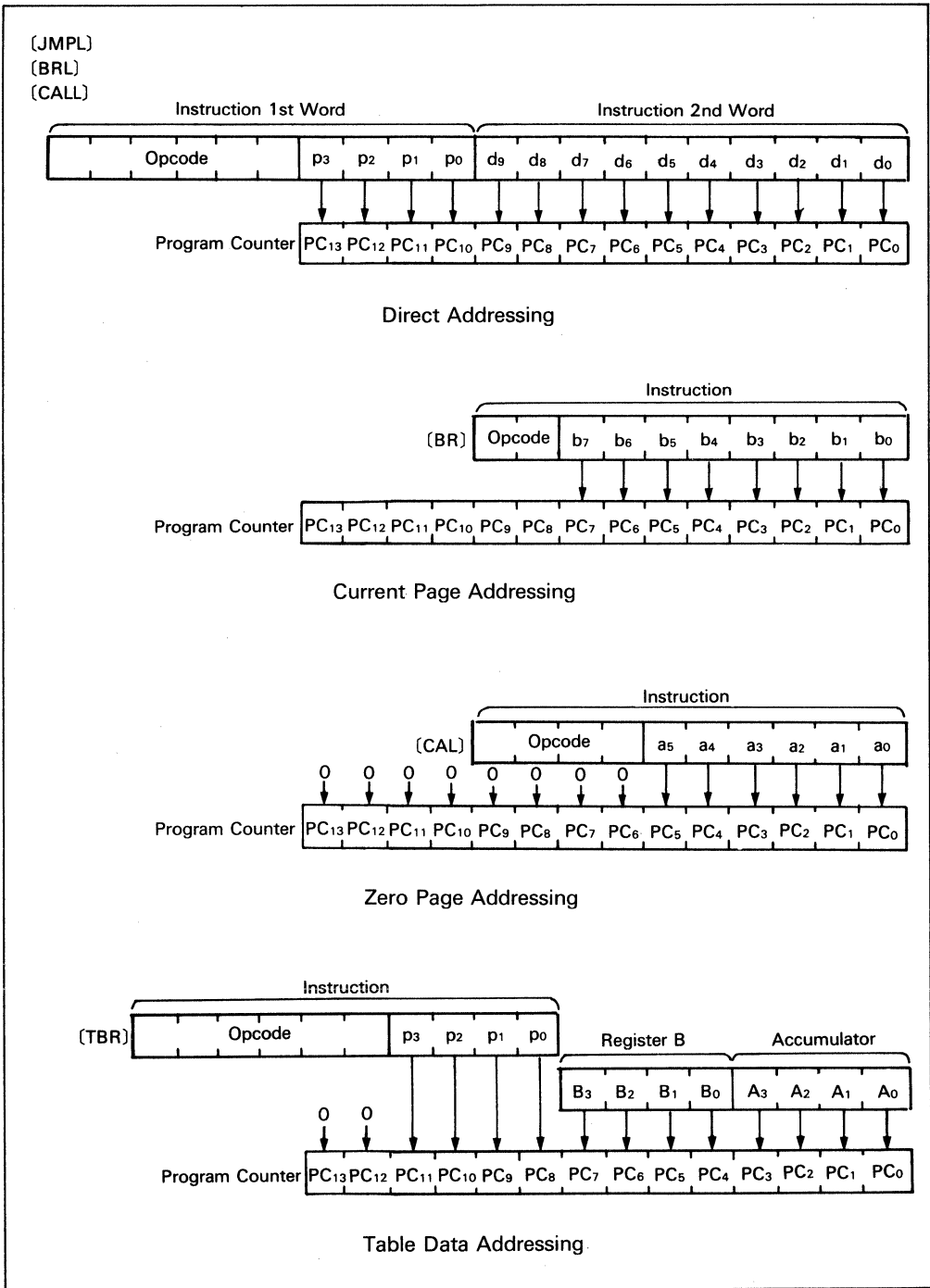


Figure 34. ROM Addressing Mode



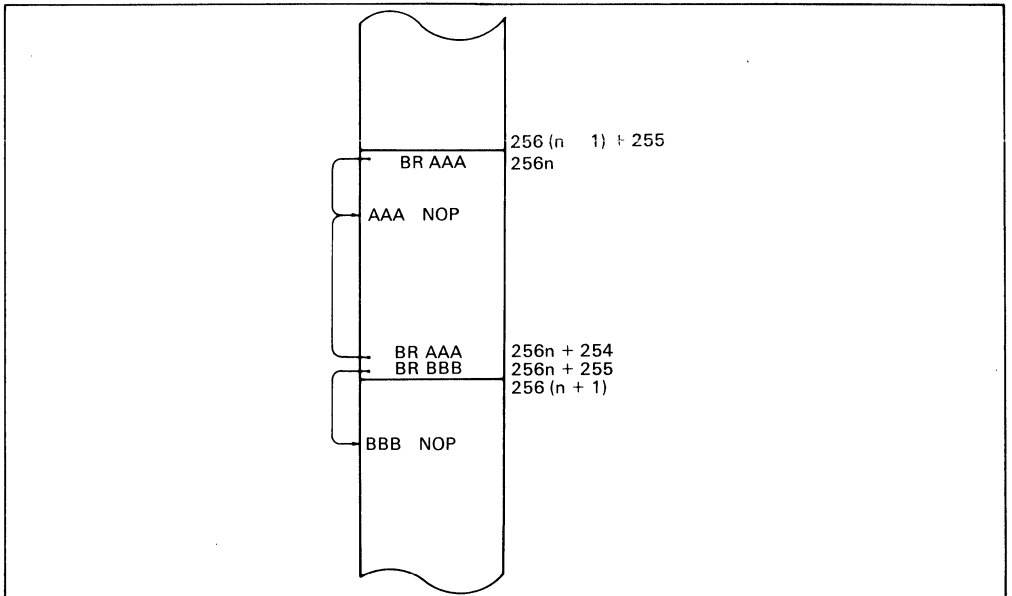


Figure 35. Branch Destination of BR Instruction on the Boundary between Pages

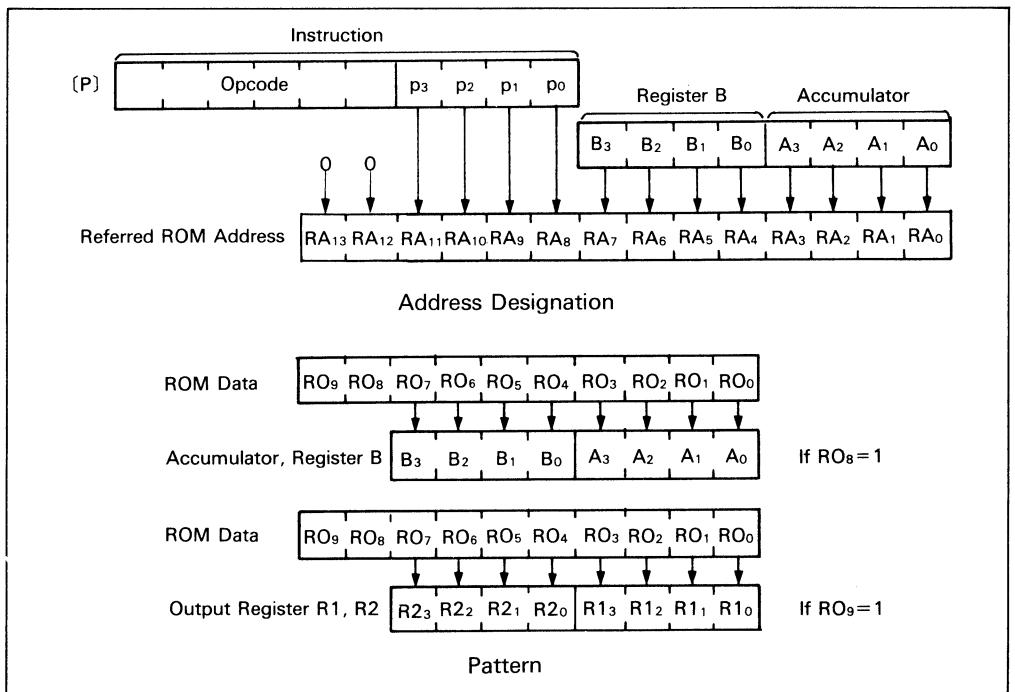


Figure 36. P Instruction



Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows:

1. Immediate instructions
2. Register-to-register instructions
3. RAM address instructions
4. RAM-register instructions
5. Arithmetic instructions

6. Compare instructions
7. RAM bit manipulation instructions
8. ROM address instructions
9. Input/output instructions
10. Control instructions

Tables 27-36 list their functions, and table 37 is an opcode map.

Table 27. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 28. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by assembler.

Table 29. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 $i_1 i_0$	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 $i_3 i_2 i_1 i_0$	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 $i_3 i_2 i_1 i_0$	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by the assembler.

Table 30. RAM-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).

The op-code X or Y is assembled as follows:

Mnemonic	Y	X	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).

The op-code X is assembled as follows:

Mnemonic	X	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 31. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A + i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B + 1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B - 1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M + A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

Table 32. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 33. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2



Table 34. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 35. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 36. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 37. Opcode Map

R8		0																1																		
R9	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
0		NO	SP	SP	SP	XSP	XY	AN	EM	/	/	/	/	AM	/	/	/	ORM	/	/	LAW	/	/	/	ANE	MD	/	/	AMD	/	/	OR	MD			
1		RTN	RTN	/	/	/	ALEM	/	/	/	AMC	/	/	/	EORM	/	/	/	LWA	/	/	/	ALE	MD	/	/	AM	CD	/	/	EOR	MD				
2		INEM i(4)																INEMD i(4)																		
3		ILEM i(4)																ILEMD i(4)																		
4		LBM(XY)	/	/	BNE	/	/	LAB	/	/	/	IB	/	/	/	CO	MB	/	/	OR	/	/	STS	/	/	SBY	STOP	/	/	/	/					
5		LMAY(X)	/	/	AYY	/	/	LSPY	/	/	/	IY	/	/	/	/	/	/	/	/	JMPL p(4)															
6		NEGA	/	/	RED	/	/	LSPX	/	/	/	/	/	/	/	/	/	/	/	TC	CALL p(4)															
0	7	YNEI i(4)																BRL p(4)																		
8		XMA(XY)	SEM n(2)				REM n(2)				TM n(2)				XMD	/	/	/	SEMD n(2)	REMD n(2)				TMD n(2)												
9		LAM(XY)	LMA(XY)				SMC	/	/	ANM	/	/	/	/	LAMD	/	/	/	LMAD	/	/	/	SMCD	/	/	/	AN	MD	/	/	/	/				
A		ROTR	ROTL	/	/	DAA	/	/	DAS	/	/	/	/	LAY	LMID i(4)																					
B		TBR p(4)																P p(4)																		
C		XMB(XY)	/	/	BLE	/	/	LBA	/	/	/	/	/	DB																						
D		LMADY(X)	/	/	SY	/	/	LYA	/	/	/	/	/	DY	CAL a(6)																					
E		TD	/	/	SED	/	/	LXA	/	/	/	REC	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/				
F		LWI i(2)																																		
1	0	LBI i(4)																																		
1	1	LYI i(4)																																		
1	2	LXI i(4)																																		
1	3	LAI i(4)																																		
1	4	LBR m(4)																																		
1	5	LAR m(4)																																		
1	6	REDD m(4)																																		
1	7	LAMR m(4)																BR	b(8)																	
1	8	AI i(4)																																		
1	9	LMIIY i(4)																																		
1	A	TDD m(4)																																		
1	B	ALEI i(4)																																		
1	C	LRB m(4)																																		
1	D	LRA m(4)																																		
1	E	SEDD m(4)																																		
1	F	XMRA m(4)																																		

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction
 2-word/2-cycle Instruction (2-word/2-cycle)



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	
Programming voltage	V_{PP}	-0.3 to +14.0	V	2
Pin voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
		-0.3 to +15.0	V	3
Total allowance of input currents	ΣI_o	100	mA	4
Total allowance of output currents	$-\Sigma I_o$	50	mA	5
Maximum input current	I_o	4	mA	6, 7
		6	mA	6, 8
		30	mA	6, 9
Maximum output current	$-I_o$	4	mA	10, 11
Operating temperature	T_{opr}	-20 to +75	°C	
Storage temperature	T_{stg}	-55 to +125	°C	
Storage temperature (when bias)	T_{bias}	-25 to +80	°C	12

- Notes:
1. Permanent damage may occur if "Absolute Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics". If these conditions are exceeded, it may cause the LSI to malfunction or affect the reliability of LSI.
 2. Applies to RA_0 (V_{PP}) of HD4074418 and HD4074408.
 3. Applies to the high-voltage pins (R8, R9) of HD4074408.
 4. Total allowance of input currents is the total sum of input current which flow in from all I/O pins to GND simultaneously.
 5. Total allowance of output currents is the total sum of the output current which flow out from V_{CC} to all I/O pins simultaneously.
 6. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 7. Applies to R0 to R6.
 8. Applies to R8 to RA.
 9. Applies to D0 to D15.
 10. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 11. Applies to D0-D15, R0-R6, R8, and R9 of HD404418 and HD4074418, or D0-D15, R0-R6 of the HD4074408.
 12. Applies to HD4074418 and HD4074408.

Electrical Characteristics

DC Characteristics ($V_{CC} = 4.5$ to 5.5 V, $GND = 0$ V, $T_a = -20$ °C to $+75$ °C, unless otherwise specified)

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Input high voltage	V_{IH}	RESET,	$0.85V_{CC}$		$V_{CC}+0.3$	V		
		$\overline{INT}_0, \overline{INT}_1,$ $INT_2, INT_3,$ $INT_4, INT_5,$ $SCK_1, SCK_2,$	$0.8V_{CC}$		$V_{CC}+0.3$	V		
		\overline{TI}_1, TI_2	$0.8V_{CC}$		$V_{CC}+0.3$	V		
		SI1, SI2	$0.8V_{CC}$		$V_{CC}+0.3$	V		
		OSC1	$V_{CC}-0.5$		$V_{CC}+0.3$	V	External Clock Operation	
Input low voltage	V_{IL}	RESET,	-0.3		$0.15V_{CC}$	V		
		$\overline{INT}_0, \overline{INT}_1,$ $INT_2, INT_3,$ $INT_4, INT_5,$ $SCK_1, SCK_2,$	-0.3		$0.2V_{CC}$	V		
		\overline{TI}_1, TI_2	-0.3		$0.2V_{CC}$	V		
		SI1, SI2	-0.3		$0.2V_{CC}$	V		
		OSC1	-0.3		0.5	V	External Clock Operation	
Output high voltage	V_{OH}	$\overline{SCK}_1, SO_1,$ $SCK_2, SO_2,$	$V_{CC}-1.0$			V	$-I_{OH} = 1.0$ mA	
		TO1, TO2, TO3	$V_{CC}-0.3$			V	$-I_{OH} = 0.01$ mA	
Output low voltage	V_{OL}	$\overline{SCK}_1, SO_1,$ $SCK_2, SO_2,$ TO1, TO2, TO3		0.4		V	$I_{OL} = 1.6$ mA	
Input/output leakage current	$ I_{IL} $	RESET, OSC1, $\overline{INT}_0, \overline{INT}_1,$ $INT_2, INT_3,$ $INT_4, INT_5,$ $\overline{TI}_1, TI_2,$ $\overline{SCK}_1, SI_1,$ SCK_2, SI_2		1		μA	$V_{in} = 0$ V to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}		4	8	mA	$V_{CC} = 5$ V R7 digital input mode $f_{osc} = 8$ MHz	2, 5
	I_{CMP}			7	12	mA	$V_{CC} = 5$ V R7 analog input mode $f_{osc} = 8$ MHz	3
Current dissipation in standby mode	I_{SBY}	V_{CC}		2	4	mA	$V_{CC} = 5$ V, $f_{osc} = 8$ MHz	4, 5
Current dissipation in stop mode	I_{stop}	V_{CC}			10	μA	$V_{in}(TEST) = V_{CC}$ to $V_{CC} - 0.3$ V $V_{in}(RESET) = 0$ to 0.3 V	
Stop mode retain voltage	V_{stop}	V_{CC}	2			V		



- Notes: 1. Pull-up MOS and output buffer current are excluded.
 2. The MCU is in the reset state. The input/output current does not flow.
 Test Conditions: MCU state: ● Reset state
 Pin state: ● RESET, TEST...V_{CC}
 3. The source power when I/O current does not flow with all pins of R7 in the analog input mode.
 Test condition: ● V_{ref}, R7₀-R7₃...GND
 4. The timer operates with the fastest clock and input/output current does not flow.
 Test Conditions: MCU state: ● Standby Mode
 ● Input/Output: Reset state
 ● Timer: ÷ 2 prescaler divide ratio
 ● Serial Interface: Stop
 Pin state: ● RESET...GND
 ● TEST...V_{CC}
 ● D₀-D₁₅, R₀-R_A...V_{CC}
 5. When f_{osc}=x [MHz], the current dissipation in operation mode and standby mode are estimated as follows:

$$\text{max. value (f}_{\text{osc}} = x \text{ [MHz])} = \frac{x}{8} \times \text{max. value (f}_{\text{osc}} = 8)$$

When f_{osc} is less than 1 [MHz], current dissipation is sometimes more than estimated.

Input/Output Characteristics for Standard Pin

(V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = -20°C to +75°C, unless otherwise specified.)

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Input high voltage	V _{IH}	R0-RA	0.7V _{CC}		V _{CC} +0.3	V		1
Input low voltage	V _{IL}	R0-RA	-0.3		0.3V _{CC}	V		1
Output high voltage	V _{OH}	R0-R6, R8, R9	V _{CC} -1.0			V	-I _{OH} = 1.0 mA	1
		R0-R6, R8, R9	V _{CC} -0.3			V	-I _{OH} = 0.01 mA	1
Output low voltage	V _{OL}	R0-R6, R8-RA			0.4	V	I _{OL} = 1.6 mA	1
Input/output leakage current	I _{IL}			1		μA	V _{in} = 0 V to V _{CC}	2,3
				10		μA	V _{in} = 0 V to V _{CC}	2,4
Pull-up MOS current	-I _p	R0-R6	15		120	μA	V _{CC} =5 V, V _{in} =0 V	5
Input high voltage	V _{IHA}	R7(Analog compare mode)	V _{ref} +0.1		V _{CC} -1.2	V		
Input low voltage	V _{ILA}	R7(Analog compare mode)	0		V _{ref} -0.1	V		
Analog input reference voltage scope	V _{ref}	V _{ref}	0		V _{CC} -1.2	V		

- Notes: 1. Does not apply to R8, R9 of the HD4074408.
 2. Pull-up MOS and output buffer current is excluded.
 3. Applies to R0-RA of the HD404418, R0-R9 and RA₁ of the HD4074418, R0-R7 and RA₁ of the HD4074408.
 4. Applies to RA₀ of the HD4074418, HD4074408.
 5. Applies to HD404418 pins which were specified as with pull-up MOS via mask option.

Input/Output Characteristics for High-Current Pins

($V_{CC} = 4.5$ to 5.5 V, $GND = 0$ V, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise specified)

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Input high voltage	V_{IH}	D ₀ -D ₁₅	$0.7V_{CC}$		$V_{CC}+0.3$	V		
Input low voltage	V_{IL}	D ₀ -D ₁₅	-0.3		$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D ₀ -D ₁₅	$V_{CC}-1.0$			V	$-I_{OH} = 1.0$ mA	
		D ₀ -D ₁₅	$V_{CC}-0.3$			V	$-I_{OH} = 0.01$ mA	
Output low voltage	V_{OL}	D ₀ -D ₁₅			1.5	V	$I_{OL} = 10$ mA	
Input/output leakage current	$ I_{IL} $	D ₀ -D ₁₅			1	μA	$V_{in} = 0$ V - V_{CC}	1
Pull up MOS current	$-I_P$	D ₀ -D ₁₅	15		120	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	2

- Notes: 1. Pull-up MOS and output buffer current are excluded.
 2. Applies to HD404418 pins which are specified as with pull-up MOS via mask option.

Input/Output Characteristics for High-Voltage Pins

($V_{CC} = 4.5$ to 5.5 V, $GND = 0$ V, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted)

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Input high voltage	V_{IH}	R8, R9	$0.7V_{CC}$		12.8	V		1
Input low voltage	V_{IL}	R8, R9	-0.3		$0.3V_{CC}$	V		1
Output high voltage	V_{OH}	R8, R9	11			V	7.5 k Ω to 12 V	1
Output low voltage	V_{OL}	R8, R9			0.4	V	$I_{OL} = 1.6$ mA	1
Input/output leakage current	$ I_{IL} $	R8, R9			10	μA	$V_{in} = 0$ V - 12.8 V	1

- Note: 1. Applies to the HD4074408.



AC Characteristics

(V_{CC} = 4.5 to 5.5 V, GND = 0 V, T_a = -20°C to +75°C, unless otherwise specified)

Items	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Crystal of ceramic filter oscillator	Oscillation frequency	f _{osc}	OSC ₁ , OSC ₂	0.4	8	9.0	MHz	
	Instruction cycle time	t _{cyc}		0.89	1	20	μs	
	Oscillator stabilization time	t _{RC}	OSC ₁ , OSC ₂			20	ms	1
External clock operation	External clock frequency	f _{CP}	OSC ₁	0.4		9.0	MHz	2
	External clock high level width	t _{CPH}	OSC ₁	41			ns	2
	External clock low level width	t _{CPL}	OSC ₁	41			ns	2
	External clock rise time	t _{CPr}	OSC ₁			20	ns	2
	External clock fall time	t _{CPf}	OSC ₁			20	ns	2
	Instruction cycle time	t _{cyc}		0.89		20	μs	2
External interrupt signal high level width	t _{IH}	$\overline{\text{INT}}_0, \overline{\text{INT}}_1, \overline{\text{INT}}_2, \overline{\text{INT}}_3, \overline{\text{INT}}_4, \overline{\text{INT}}_5$	2			t _{cyc}	3	
External interrupt signal low level width	t _{IL}	$\overline{\text{INT}}_0, \overline{\text{INT}}_1, \overline{\text{INT}}_2, \overline{\text{INT}}_3, \overline{\text{INT}}_4, \overline{\text{INT}}_5$	2			t _{cyc}	3	
Timer input high level width	t _{TH}	$\overline{\text{T}}_1, \text{T}_2$	2			t _{cyc}	3	
Timer input low level width	t _{TL}	$\overline{\text{T}}_1, \text{T}_2$	2			t _{cyc}	3	
RESET high level width	t _{RSTH}	RESET	3			t _{cyc}	4	
Input capacitance	C _{in}					70	pF	f = 1 MHz, V _{in} = 0V 5
						15	pF	f = 1 MHz, V _{in} = 0V 6
RESET fall time	t _{RSTf}					20	ms	4
Analog comparator stabilization time	t _{CSTB}	R7 (In analog input mode)				2	t _{cyc}	7

- Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 4.5 V at power-on, or after RESET input level goes high after resetting to leave the stop mode. When using crystal or ceramic filter oscillator, please check the crystal oscillator stabilization time, since it depends on the circuit constant and stray capacitance.
2. See figure 37.
3. See figure 38.
4. See figure 39.
5. Applies to RA₀ of HD4074418, HD4074408.
6. Applies to all input pins of HD404418 and input pins except for RA₀ of HD4074418, HD4074408.
7. Analog comparator stabilization time is the time until the analog comparator stabilizes to read precise data after R7 goes into the analog input mode.



Serial Interface Timing Characteristics

(V_{CC} = 5 V ± 10 %, GND = 0 V, T_a = -20°C to +75°C, unless otherwise specified)
At Transfer Clock Output

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Transfer clock cycle time	t _{Syc}	SCK ₁ , SCK ₂	1			t _{cyc}	1, 2	
Transfer clock high level width	t _{SCKH}	SCK ₁ , SCK ₂	0.5			t _{Syc}	1, 2	
Transfer clock low level width	t _{SCKL}	SCK ₁ , SCK ₂	0.5			t _{Syc}	1, 2	
Transfer clock rise time	t _{SCKr}	SCK ₁ , SCK ₂			100	ns	1, 2	
Transfer clock fall time	t _{SCKf}	SCK ₁ , SCK ₂			100	ns	1, 2	
Serial output data delay time	t _{DSO}	SO ₁ , SO ₂			250	ns	1, 2	
Serial input data set-up time	t _{SSI}	SI ₁ , SI ₂	300			ns	1	
Serial input data hold time	t _{HSI}	SI ₁ , SI ₂	150			ns	1	

At Transfer Clock Input

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min	Typ	Max			
Transfer clock cycle time	t _{Syc}	SCK ₁ , SCK ₂	1			t _{cyc}	1	
Transfer clock high level width	t _{SCKH}	SCK ₁ , SCK ₂	0.5			t _{Syc}	1	
Transfer clock low level width	t _{SCKL}	SCK ₁ , SCK ₂	0.5			t _{Syc}	1	
Transfer clock rise time	t _{SCKr}	SCK ₁ , SCK ₂			100	ns	1	
Transfer clock fall time	t _{SCKf}	SCK ₁ , SCK ₂			100	ns	1	
Serial output data delay time	t _{DSO}	SO ₁ , SO ₂			250	ns	1, 2	
Serial input data set-up time	t _{SSI}	SI ₁ , SI ₂	300			ns	1	
Serial input data hold time	t _{HSI}	SI ₁ , SI ₂	150			ns	1	

- Notes: 1. See figure 40.
 2. See figure 41.



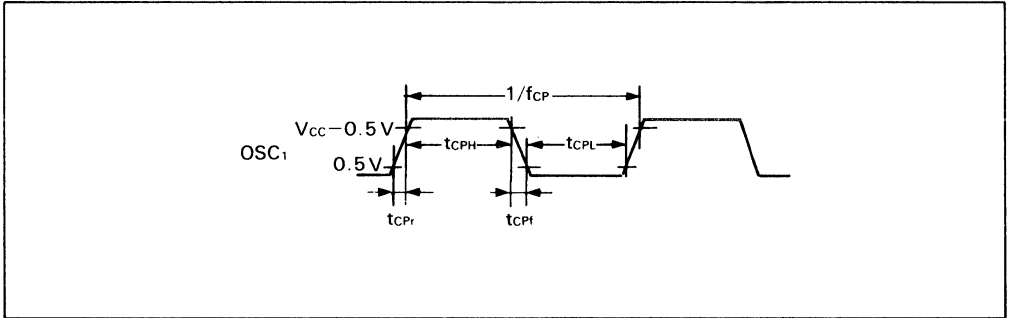


Figure 37. External Clock Timing

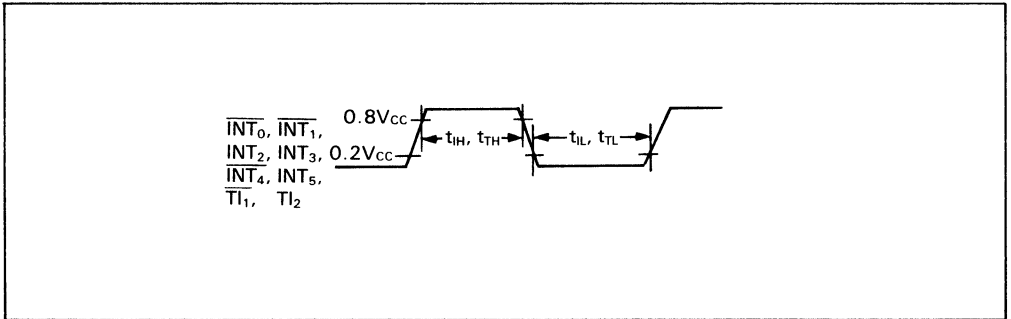


Figure 38. Interrupt and Timer Input Timing

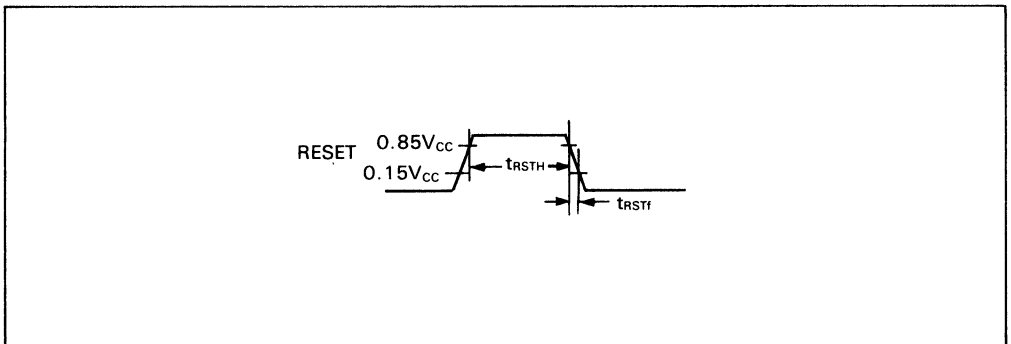


Figure 39. Reset Timing

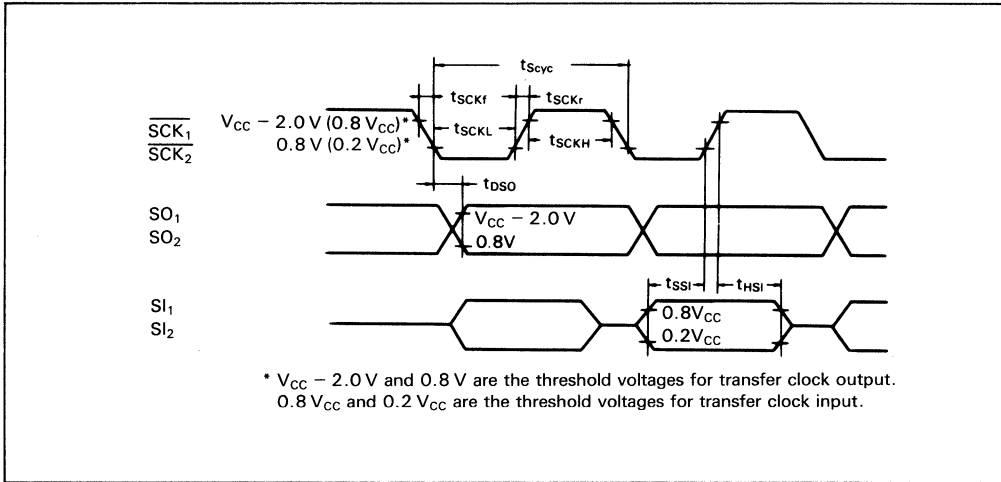


Figure 40. Timing Diagram of Serial Interface

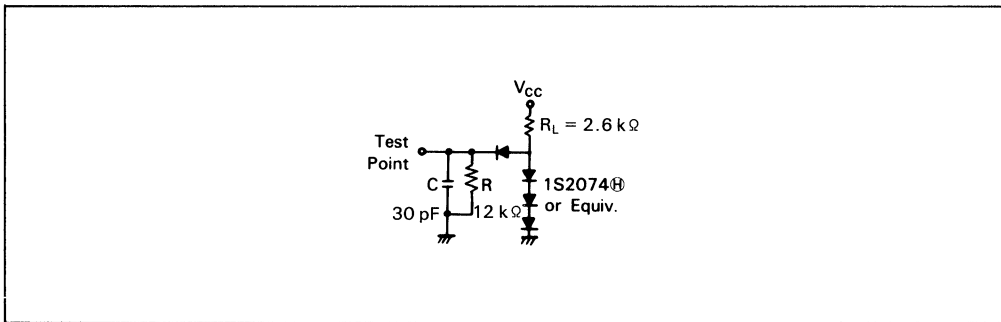


Figure 41. Timing Load Circuit

Programming Electrical Characteristics

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2	$V_{CC}+0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3	0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4		V	$I_{OH} = -200\ \mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}		0.4	V	$I_{OL} = 1.6\ \text{mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $		2	μA	$V_{in} = 5.25\text{ V}/0.5\text{ V}$
V_{CC} current		I_{CC}		30	mA	
V_{PP} current		I_{PP}		40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Address set-up time	t_{AS}	2			μs	Figure 42
\overline{OE} set-up time	t_{OES}	2			μs	(Note)
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

Note : Input pulse level: 0.8 to 2.2 V
 Input rising/falling time $\leq 20\text{ ns}$
 Timing reference level { input : 1.0 V, 2.0 V
 output : 0.8 V, 2.0 V

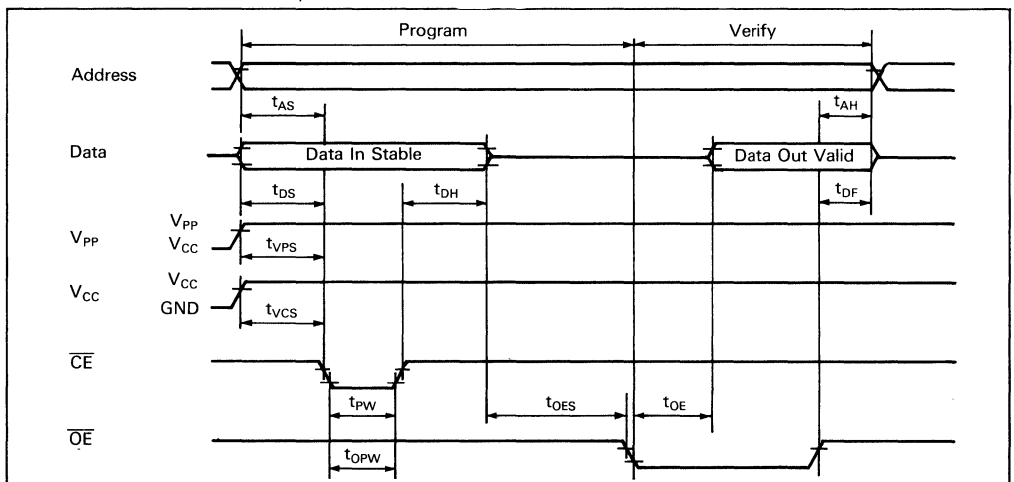


Figure 42. PROM Program/Verify Timing



HD404418/HD4074418/HD4074408

Differences between HD404418 and HD4074418 (HD4074408)

Item	HD4074418 (ZTAT) HD4074408 (ZTAT)		HD404418 (Mask ROM)	
Input/Output Leakage Current	RA ₀ /V _{PP} Other standard pins	10 μ A max 1 μ A max	All standard pins	1 μ A max
Input Pin Capacitance	RA ₀ /V _{PP} Other pins	70 pF max 15 pF max	All pins	15 pF max
I/O Option	No All pins are without pull-up MOS		Yes With pull-up MOS can be specified (D ₀ -D ₁₅ , R ₀ -R ₆ , except R ₄₃)	
Timer Option	No One of two options provided for each product can be selected		Yes Free-running timer, watchdog timer	
High-voltage Port Version (R ₈ , R ₉)	Yes (HD4074408)		No	
Precaution	The HD404418 differs from HD4074418 (HD4074408) in chip design and manufacturing process. Be careful when using the HD4074418 (HD4074408) system for the HD404418 since characteristic values are not exactly the same though guaranteed values are identical.			

HD404418 Mask Option List

5 V Operation : HD404418


Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

(1) I/O Option

Please enter in applicable item for I/O option selection.

A: Without Pull-Up MOS B: With Pull-Up MOS

C: NMOS Open Drain

Note (I/O options masked by  are not available.)

Pin	Input/Output		I/O Option			Pin	Input/Output		I/O Option			
			A	B	C				A	B	C	
D ₀	High Current Pins	Input/Output				R3	R3 ₀	Input/Output				
D ₁		Input/Output					R3 ₁	Input/Output				
D ₂		Input/Output					R3 ₂	Input/Output				
D ₃		Input/Output					R3 ₃	Input/Output				
D ₄		R4	Input/Output				R4 ₀	Input/Output				
D ₅			Input/Output				R4 ₁	Input/Output				
D ₆			Input/Output				R4 ₂	Input/Output				
D ₇		R5	Input/Output				R4 ₃	Input/Output	<input type="checkbox"/>			
D ₈			Input/Output				R5 ₀	Input/Output				
D ₉			Input/Output				R5 ₁	Input/Output				
D ₁₀			Input/Output				R5 ₂	Input/Output				
D ₁₁		R6	Input/Output				R5 ₃	Input/Output				
D ₁₂			Input/Output				R6 ₀	Input/Output				
D ₁₃			Input/Output				R6 ₁	Input/Output				
D ₁₄			Input/Output				R6 ₂	Input/Output				
D ₁₅		Input/Output				R6 ₃	Input/Output					
Standard Pins												
Standard Pins												
R0	Standard Pins	R0 ₀	Input/Output				R7	R7 ₀	Input	<input type="checkbox"/>		
		R0 ₁	Input/Output					R7 ₁	Input	<input type="checkbox"/>		
		R0 ₂	Input/Output					R7 ₂	Input	<input type="checkbox"/>		
		R0 ₃	Input/Output					R7 ₃	Input	<input type="checkbox"/>		
R1	Standard Pins	R1 ₀	Input/Output				R8	R8 ₀	Input/Output	<input type="checkbox"/>		
		R1 ₁	Input/Output					R8 ₁	Input/Output	<input type="checkbox"/>		
		R1 ₂	Input/Output					R8 ₂	Input/Output	<input type="checkbox"/>		
		R1 ₃	Input/Output					R8 ₃	Input/Output	<input type="checkbox"/>		
R2	Standard Pins	R2 ₀	Input/Output				R9	R9 ₀	Input/Output	<input type="checkbox"/>		
		R2 ₁	Input/Output					R9 ₁	Input/Output	<input type="checkbox"/>		
		R2 ₂	Input/Output					R9 ₂	Input/Output	<input type="checkbox"/>		
		R2 ₃	Input/Output				R9 ₃	Input/Output	<input type="checkbox"/>			
								RA	RA ₀	Input/Output		
							RA ₁	Input/Output			<input type="checkbox"/>	



HD404418/HD4074418/HD4074408

(2) Package

Package
<input type="checkbox"/> DP-64S (shrink package)
<input type="checkbox"/> FP-64
<input type="checkbox"/> FP-64A

* Please enter check marks (■, ×, √) in applicable item.

(3) Timer 4

Divider Circuit
<input type="checkbox"/> Free-running Timer
<input type="checkbox"/> Watchdog Timer

Application Check List

(4) ROM Code Media

ROM Code Media
<input checked="" type="checkbox"/> EPROM: EPROM On-Package Microcomputer Type

(A) Oscillator (CPG option)

	<input checked="" type="checkbox"/> HD404418 (5 V Operation)
CPG option	<input type="checkbox"/> Ceramic Filter
	<input type="checkbox"/> Crystal
	<input type="checkbox"/> External Clock

* Please enter check marks (■, ×, √) in applicable item.



HD404418/HD4074418/HD4074408

HD4074418/HD4074408 Type Name and Mark

Package		Timer Option	
		Free-running Timer	Watchdog Timer
DC-64S	Type Name	HD4074418C HD4074408C	HD4074418C01 HD4074408C01
	Mark	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> JAPAN 7G1 HD4074418C </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> JAPAN 7G1 HD4074408C </div>	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> JAPAN 7G1 HD4074418C01 </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> JAPAN 7G1 HD4074408C01 </div>
DP-64S	Type Name	HD4074418S HD4074408S	HD4074418S01 HD4074408S01
	Mark	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> 7G1 HD4074418S JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD4074408S JAPAN </div>	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> 7G1 HD4074418S 01 JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD4074408S 01 JAPAN </div>
FP-64	Type Name	HD4074418F HD4074408F	HD4074418F01 HD4074408F01
	Mark	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> 7G1 HD4074418F JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD4074408F JAPAN </div>	<div style="border: 1px solid black; padding: 5px; text-align: center; margin-bottom: 5px;"> 7G1 HD4074418F 01 JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD4074408F 01 JAPAN </div>
FP-64A	Type Name	HD4074418H HD4074408H	HD4074418H01 HD4074408H01
	Mark	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 5px; text-align: center; margin-right: 10px;"> 7G1 HD 4074418H JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD 4074408H JAPAN </div> </div>	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 5px; text-align: center; margin-right: 10px;"> 7G1 HD 4074418H 01 JAPAN </div> <div style="border: 1px solid black; padding: 5px; text-align: center;"> 7G1 HD 4074408H 01 JAPAN </div> </div>

Note: Marks presented here are standard specification.



HD404608/HD4074608

Description

The MCU is a microcomputer unit which has powerful and efficient architecture of the HMCS400 family. The MCU incorporates a high-precision dual tone multi-frequency (DTMF) circuit, LCD driver/controller, voltage comparator, and 32kHz watch oscillator circuit.

The HD4074608, incorporating PROM, is a ZTAT microcomputer which can dramatically shorten system development period and smoothly proceed from debugging to mass production.

Features

- 8192 words of 10-bit ROM
- 1184 digits of 4-bit RAM
- 30 I/O pins:
Including 10 high current output pins.
I/O pin circuit configuration is CMOS
Input/Output pull-up MOS can be selected by software
- On-chip DTMF generator
- 16-digit LCD driver
- Three timers/counters
- Clock synchronous 8-bit serial interface
- Six interrupt sources
 - External: 2
 - Internal: 4
- Subroutine stack
 - Up to 16 levels including interrupts
- Instruction cycle time
 - 10 μ s (fosc = 400kHz)
 - 5 μ s (fosc = 800kHz)
- Four low power dissipation modes
 - Stop mode
 - Standby mode
 - Watch mode
 - Subactive mode (Option)
- Internal oscillator:
Crystal or ceramic filter
(external clock is available)
- Voltage comparator (2 channels)
- Operation modes:
MCU mode
PROM mode (HD4074608)
- Package
 - 80-pin plastic flat package (FP-80B)
(FP-80A)

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Type of Products

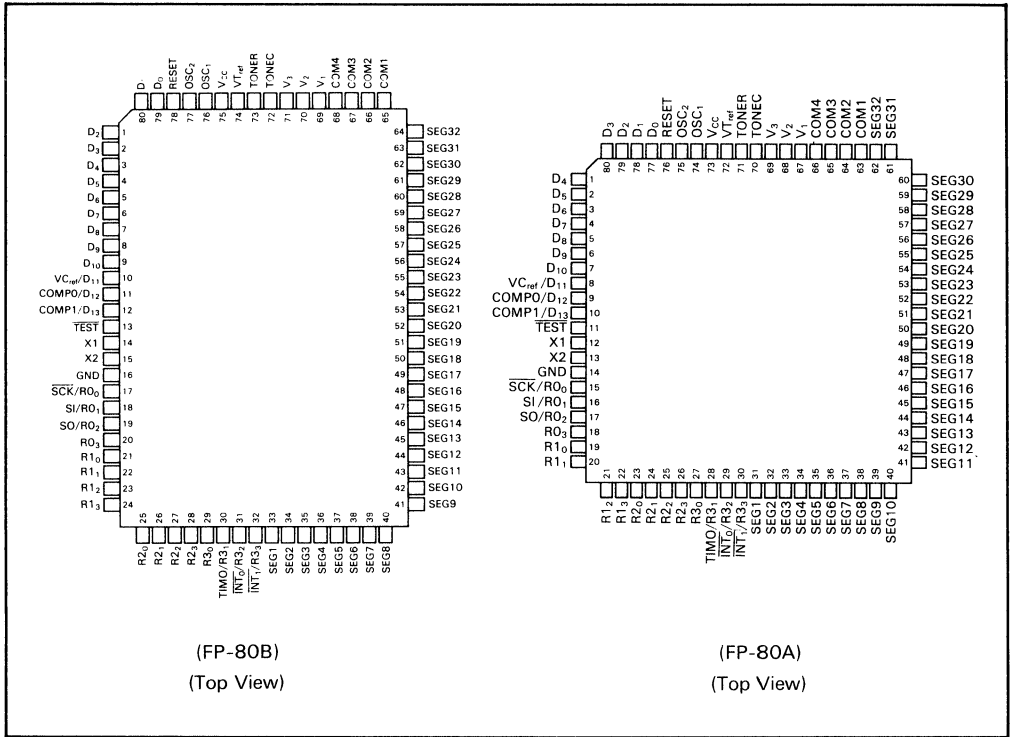
Mask ROM type

Part No.	Clock Freq. (kHz)	Package
HD404608FS	400/800	FP-80B
HD404608H		FP-80A

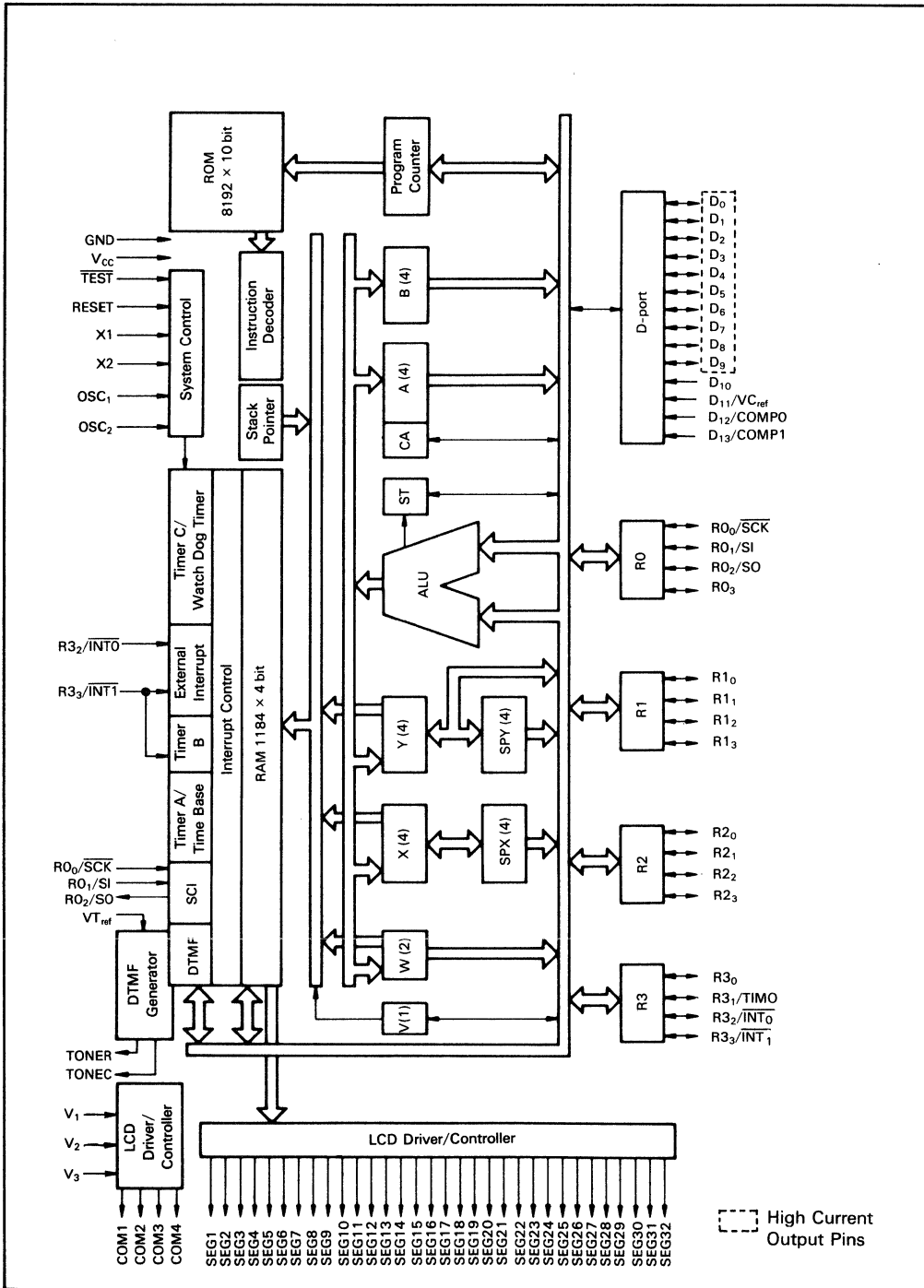
ZTAT type

Part No.	Clock Freq. (kHz)	Package
HD4074608FS	400/800	FP-80B
HD4074608H		FP-80A

Pin Arrangement



Block Diagram



Pin Function

Pin No. FP-80B	FP-80A	Pin Name	I/O	Pin No. FP-80B	FP-80A	Pin Name	I/O
1	79	D ₂	I/O	41	39	SEG9	O
2	80	D ₃	I/O	42	40	SEG10	O
3	1	D ₄	I/O	43	41	SEG11	O
4	2	D ₅	I/O	44	42	SEG12	O
5	3	D ₆	I/O	45	43	SEG13	O
6	4	D ₇	I/O	46	44	SEG14	O
7	5	D ₈	I/O	47	45	SEG15	O
8	6	D ₉	I/O	48	46	SEG16	O
9	7	D ₁₀	I	49	47	SEG17	O
10	8	D ₁₁ /V _{Cref}	I	50	48	SEG18	O
11	9	D ₁₂ /COMPO	I	51	49	SEG19	O
12	10	D ₁₃ /COMP1	I	52	50	SEG20	O
13	11	TEST	I	53	51	SEG21	O
14	12	X1	I	54	52	SEG22	O
15	13	X2	O	55	53	SEG23	O
16	14	GND		56	54	SEG24	O
17	15	R0 ₀ /SCK	I/O	57	55	SEG25	O
18	16	R0 ₁ /SI	I/O	58	56	SEG26	O
19	17	R0 ₂ /SO	I/O	59	57	SEG27	O
20	18	R0 ₃	I/O	60	58	SEG28	O
21	19	R1 ₀	I/O	61	59	SEG29	O
22	20	R1 ₁	I/O	62	60	SEG30	O
23	21	R1 ₂	I/O	63	61	SEG31	O
24	22	R1 ₃	I/O	64	62	SEG32	O
25	23	R2 ₀	I/O	65	63	COM1	O
26	24	R2 ₁	I/O	66	64	COM2	O
27	25	R2 ₂	I/O	67	65	COM3	O
28	26	R2 ₃	I/O	68	66	COM4	O
29	27	R3 ₀	I/O	69	67	V ₁	
30	28	R3 ₁ /TIMO	I/O	70	68	V ₂	
31	29	R3 ₂ /INT ₀	I/O	71	69	V ₃	
32	30	R3 ₃ /INT ₁	I/O	72	70	TONEC	O
33	31	SEG1	O	73	71	TONER	O
34	32	SEG2	O	74	72	V _{Tref}	
35	33	SEG3	O	75	73	V _{CC}	
36	34	SEG4	O	76	74	OSC ₁	I
37	35	SEG5	O	77	75	OSC ₂	O
38	36	SEG6	O	78	76	RESET	I
39	37	SEG7	O	79	77	D ₀	I/O
40	38	SEG8	O	80	78	D ₁	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin



Pin Description

GND, V_{CC} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to V_{CC}.

TEST

TEST is for test purposes only. Connect it to V_{CC}.

RESET

RESET resets the MCU. Refer to Reset section for details.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are the oscillator terminals of the system. They can be connected to a ceramic filter resonator or external oscillator circuits.

X1, X2

These are watch oscillator on which 32.768 kHz crystal is used.

Port D (D₀–D₁₃)

Port D is a 1-bit I/O port. D₀–D₉ are I/O ports and D₁₀–D₁₃ are input ports. D₀–D₉ are high current output ports (15 mA max). D₁₁–D₁₃ are also available as voltage comparators. Refer to Input/Output for details.

Port R (R0–R3)

Port R is a 4-bit I/O port. R0–R3 are I/O ports. And R₀, R₀, R₀, R₃₁, R₃₂, and R₃₃ are multiplexed with SCK, SI, SO, TIMO, INT₀, INT₁, respectively.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R₀, R₀, and R₀, respectively. For details, see Serial Interface section.

TIMO

TIMO is a duty variable square waveform output pin. See Timer C section for details.

V₁, V₂, V₃

These are power supply pins for LCD driver. Internal resistors provide voltage level for each pin. The voltage condition is; V_{CC} ≥ V₁ ≥ V₂ ≥ V₃ ≥ GND. See section Liquid Crystal Display for details.

COM1 to COM4

These are common signal output pins for LCD display. See Liquid Crystal Display section for details.

SEG1 to SEG32

These are segment signals output pins for LCD display. See Liquid Crystal Display section for details.

TONER, TONEC, VT_{ref}

These are DTMF signal output pins. TONER and TONEC transmits signals for ROW and COLUMN, respectively. VT_{ref} is a reference voltage of DTMF signals and apply V_{CC} = VT_{ref} ≥ GND to this. For details, see DTMF Output section.

COMP0, COMP1, VC_{ref}

COMP0, COMP1 are analog inputs for the voltage comparator. VC_{ref} is used as a reference voltage pin to input the threshold voltage of the analog input pin.

Functional Description

ROM Memory Map

The MCU includes 8,192 words \times 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. Program sequence branches to subroutine by CAL instruction.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow the MCU to refer to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

RAM Memory Map

The MCU includes 1184 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$01F, \$024 to \$03F): The special function registers are the mode or data registers for the serial interface, timer/counter, LCD, and DTMF, and the data control registers for the

I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

SEM/REM, SEMD/REMD instructions are available to the LCD control register (LCR).

Other registers cannot be accessed by RAM bit manipulation instructions.

Register Flag Area (\$020-\$023): Locations \$020 through \$023 are consisted of LSON, WDON, TGSP flags which are bit registers accessible by RAM bit manipulation instruction. Note that WDON flag can only be set and SEM/SEMD instruction is available to this.

TGSP flag can be set/reset, and SEM/REM and SEMD/REMD instructions are available to this.

LCD Data Area (\$050-\$06F): Locations \$050 to \$06F store the LCD data which is automatically transmitted to segment as a display data. LCD is illuminated with 1 and faden with 0. This area can be used as a data area.

Data Area (\$040 to \$2CF, \$100 to \$2CF; Bank1): 16 digits of \$040 through \$04F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4). 464 digits of \$100 through \$2CF is select the bank of location depending on the value of V register.

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

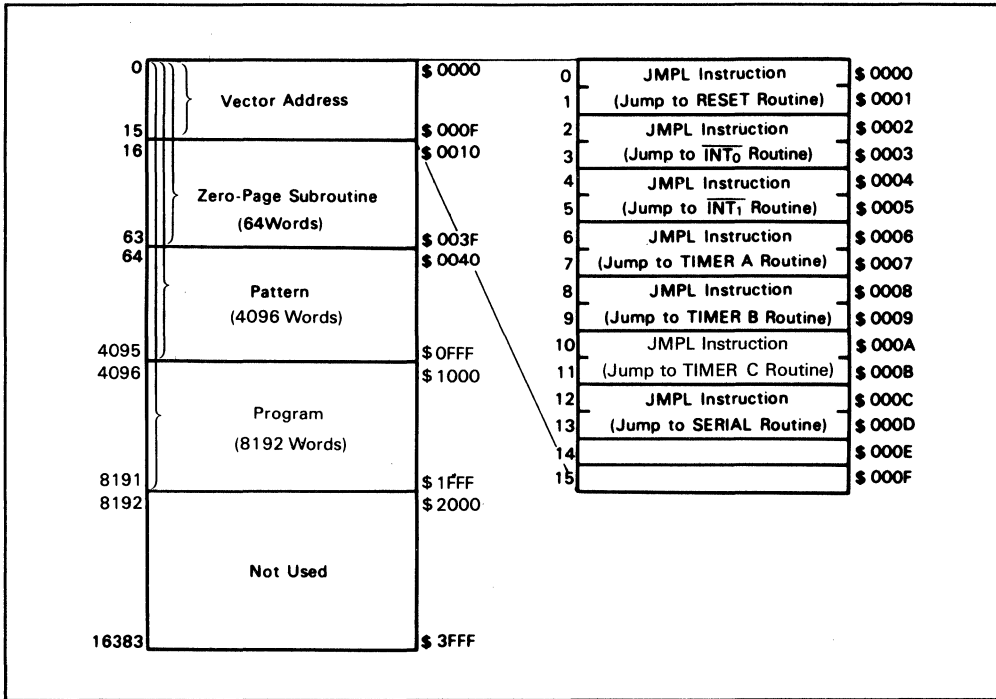


Figure 1. ROM Memory Map

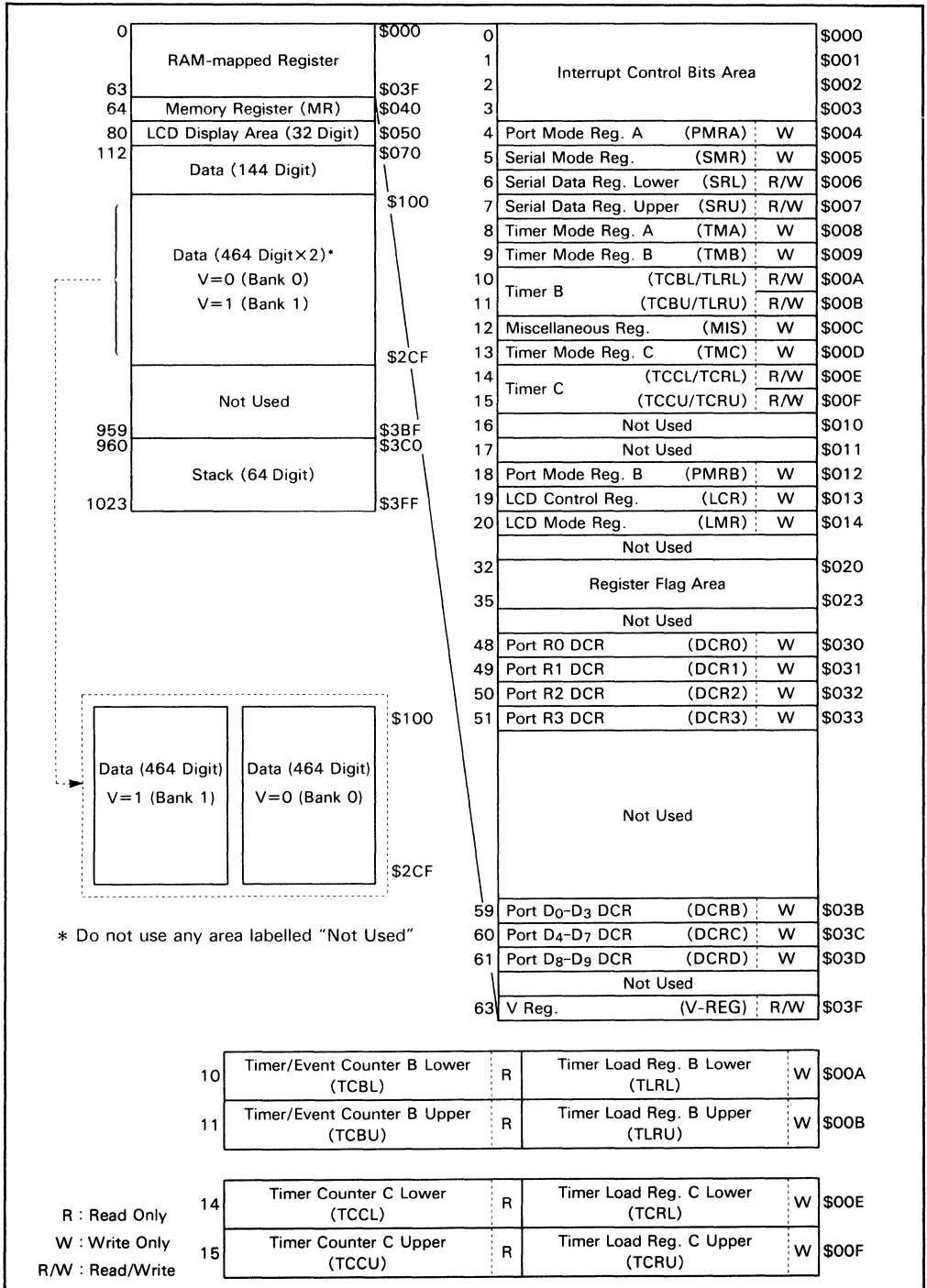


Figure 2. RAM Memory Map



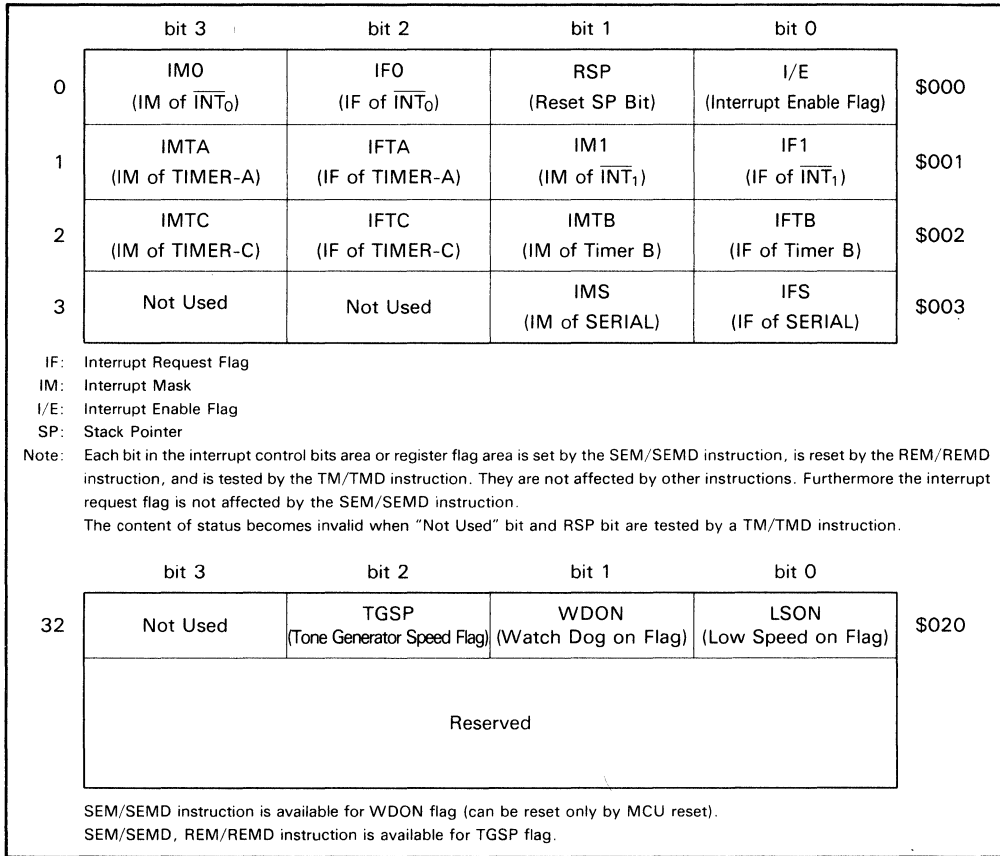


Figure 3. Configuration of Interrupt Control Bit Area and Register Flag Area

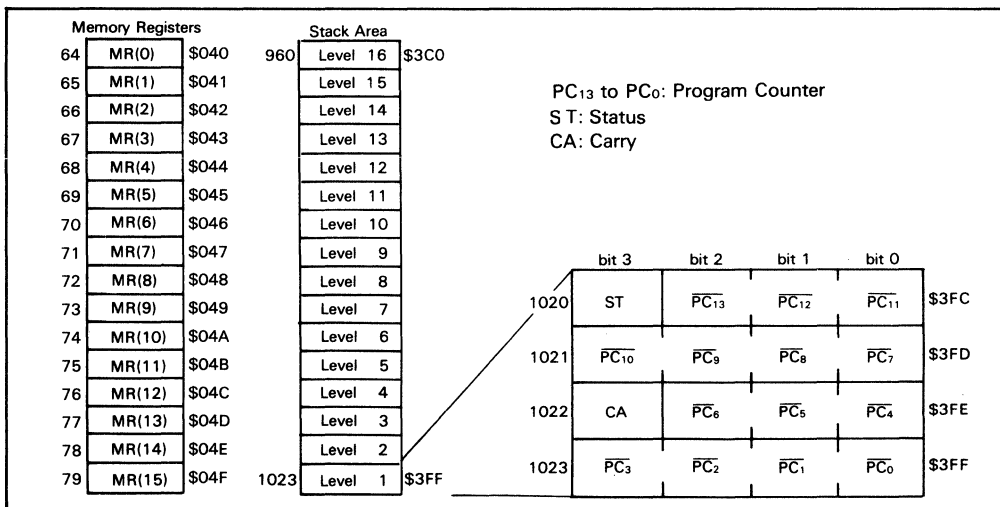


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU provides ten registers and two flags for the CPU operations. They are illustrated in figure 5 and described in the following paragraphs.

Accumulator (A), Register B (B): The accumulator and register B are 4-bit registers which hold the results of the arithmetic logic unit (ALU), and exchange data between memories, I/O pins, and other registers.

Register V (V): Register V, available for RAM address expansion, selects the bank of location \$100-\$2CF on the RAM address (464 digits) depending on its value. Therefore, when you access location \$100-\$2CF on the RAM address, specify the value of register V (V=\$0; Bank 0, V=\$1; Bank 1). You can access location \$000-\$0FF and \$300-\$3FF independently of register V's value. Register V locates on \$03F of the RAM address area.

Register W (W), Register X (X), Register Y (Y): Register W is a 2-bit, and registers X and Y are 4-bit registers which address RAM indirectly. Register Y is also available for addressing port D.

Register SPX (SPX), Register SPY (SPY): Registers SPX and SPY are 4-bit registers available for assisting registers X and Y, respectively.

Carry (CA): The carry holds the ALU overflow which arithmetic operation generates. It is also affected by SEC, REC, ROTL, and ROTR instructions. During interrupt servicing, the carry is pushed onto the stack and restored back from the stack by RTNI instruction (It is unaffected by RTN instructions).

Status (ST): The status holds the ALU overflow, ALU non-zero, and the results of bit test instruction for the arithmetic or compare instructions. The status is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until an instruction which affects the next status is executed. The status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, the status is pushed onto the stack and restored back from the stack by RTNI instruction, not by RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter for holding ROM address.

Stack Pointer (SP): The stack pointer is a 10-bit register to indicate the next stacking area up to 16 levels. The stack pointer is initialized to \$3FF on the RAM address at the MCU reset. It is decremented by 4 as data pushed onto the stack, and incremented by 4 as data restored back from the stack. The stack pointer is initialized to \$3FF either by MCU reset or the RSP bit reset by REM/REMD instruction.

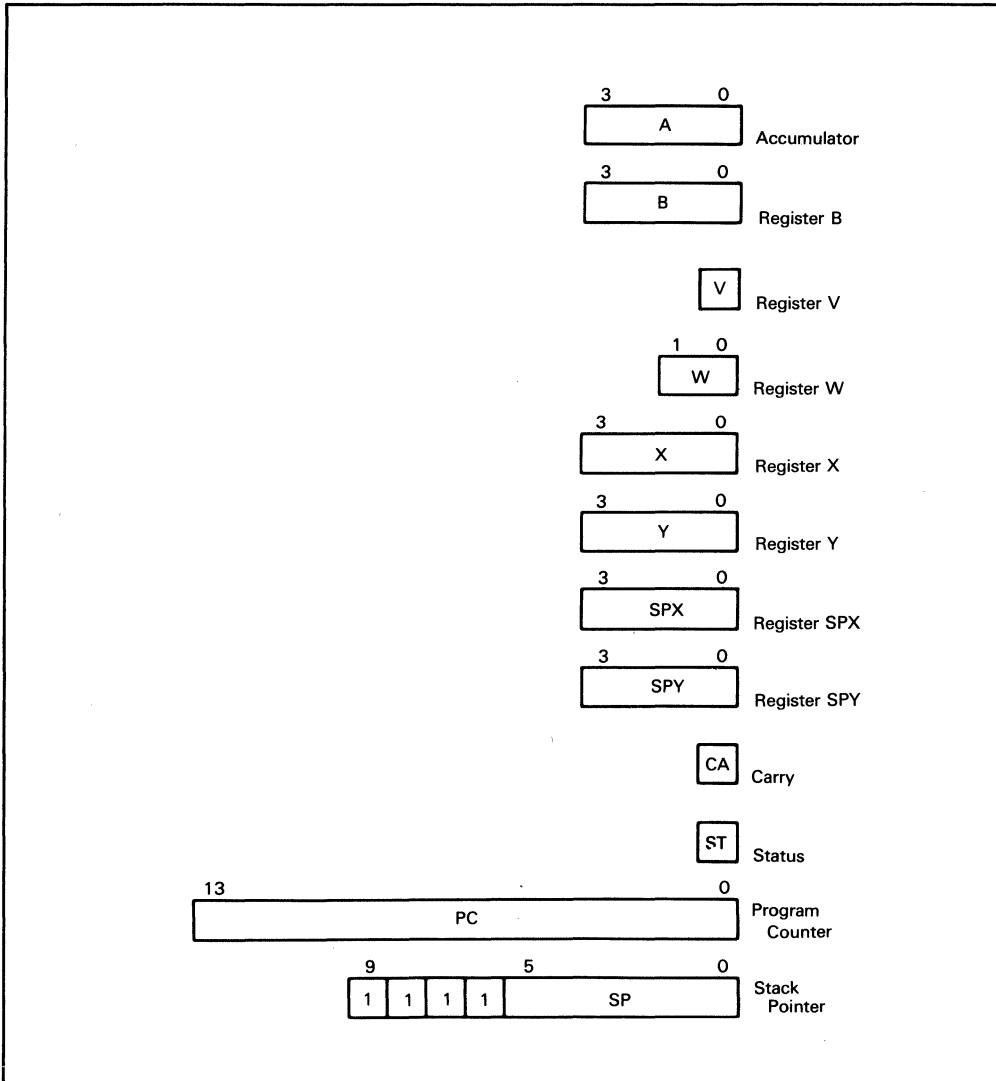


Figure 5. Registers and Flags

Interrupt

Six interrupt sources are available on the MCU: external requests (\overline{INT}_0 , \overline{INT}_1), timer/counter (timers A, B, C), and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control an interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions (The interrupt

request flag (IF) cannot be set by software). The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

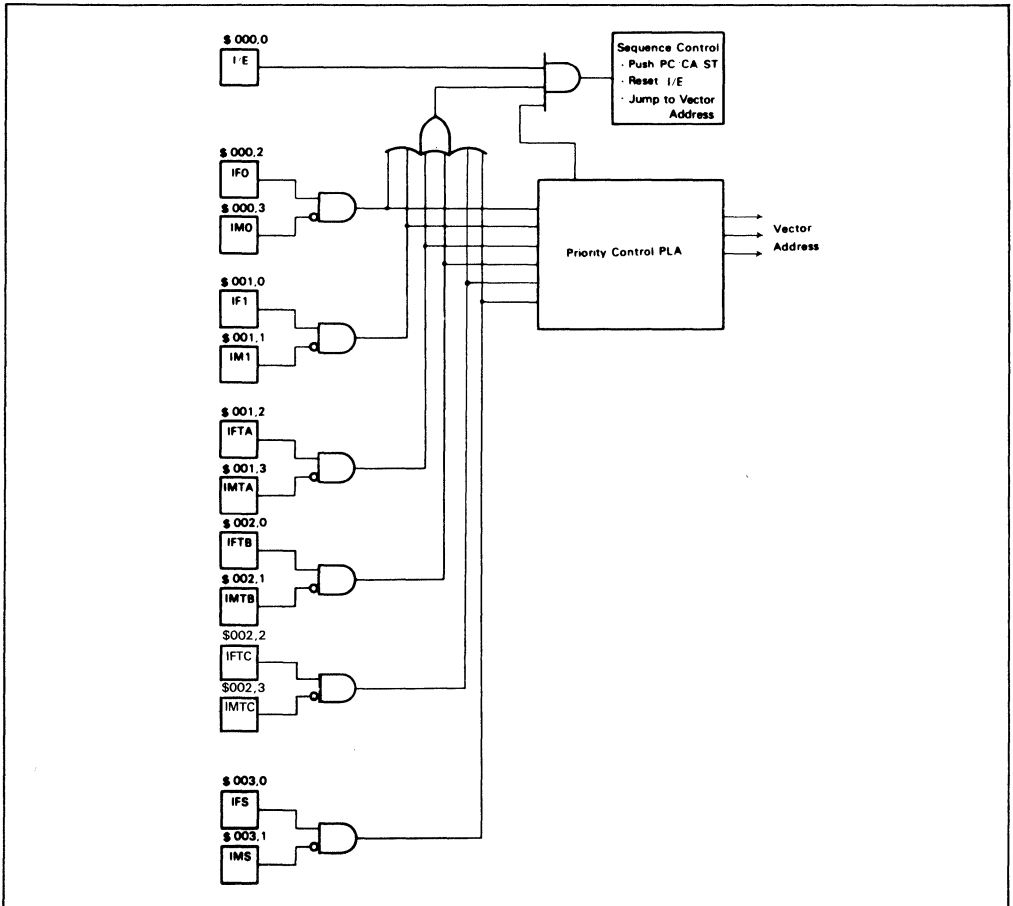


Figure 6. Interrupt Control Circuit Block Diagram



Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF, which caused the interrupt service, must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests (table 3). It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMRA: \$004).

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs (table 4).

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	–	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
Timer C	5	\$000A
SERIAL	6	\$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	Interrupt Source					
	\overline{INT}_0	\overline{INT}_1	Timer A	Timer B	Timer C	SERIAL
I/E	1	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0
IFTA · \overline{IMTA}	*	*	1	0	0	0
IFTB · \overline{IMTB}	*	*	*	1	0	0
IFTC · \overline{IMTC}	*	*	*	*	1	0
IFS · \overline{IMS}	*	*	*	*	*	1

* Don't care

each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted (table 5).

To detect the edge of \overline{INT}_0 or \overline{INT}_1 , it must need more than two instruction cycle times level ($2t_{cyc}/2t_{SUBcyc}$).

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs, respectively (table 4).

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests (table 5).

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 6).

Timer A Interrupt Mask (IMTA: \$001 bit 3): Timer A interrupt mask prevents an interrupt request from being generated by timer A interrupt request flag (table 7).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B interrupt request flag (table 9).

Timer C Interrupt Request Flag (IFTC: \$002 bit 2): The timer C interrupt request flag is set by the overflow output of timer C (table 10).

Timer C Interrupt Mask (IMTC: \$002 bit 3): The timer C interrupt mask prevents the interrupt from being generated by timer C interrupt request flag (table 11).

Serial Interrupt Request Flag (IFS: \$003 bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter (table 12).

Serial Interrupt Mask (IMS: \$003 bit 1): The serial interrupt mask masks the interrupt request (table 13).

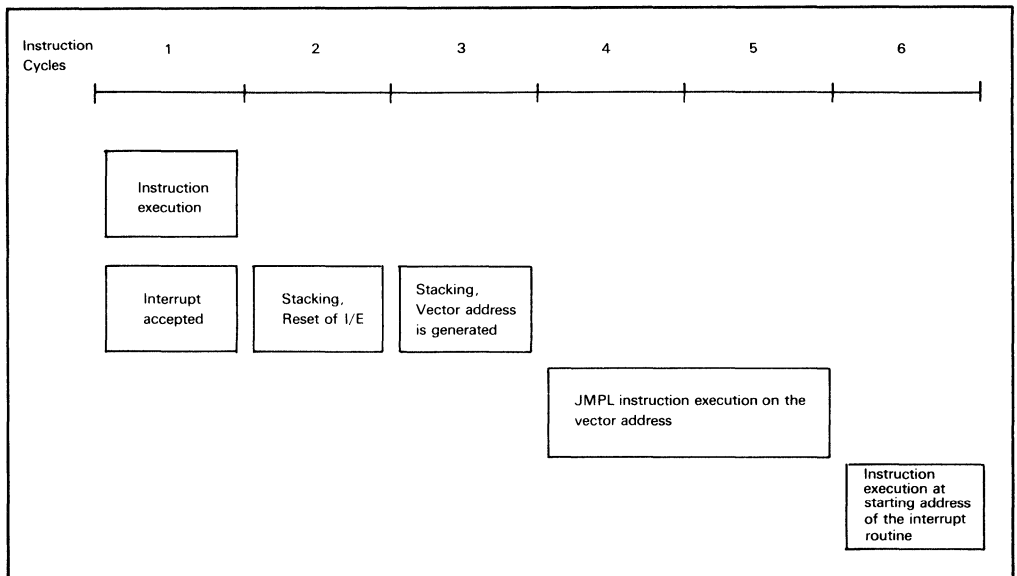


Figure 7. Interrupt Servicing Sequence

Table 3. Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags (IFO, IF1)	Interrupt Request
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks (IMO, IM1)	Interrupt Request
0	Enable
1	Disable (masks)

Table 6. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag (IFTA)	Interrupt Request
0	No
1	Yes

Table 7. Timer A Interrupt Mask

Timer A Interrupt Mask (IMTA)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag (IFTB)	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask (IMTB)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Timer C Interrupt Request Flag

Timer C Interrupt Request Flag (IFTC)	Interrupt Request
0	No
1	Yes

Table 11. Timer C Interrupt Mask

Timer C Interrupt Mask (IMTC)	Interrupt Request
0	Enable
1	Disable (mask)

Table 12. Serial Interrupt Request Flag

Serial Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 13. Serial Interrupt Mask

Serial Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

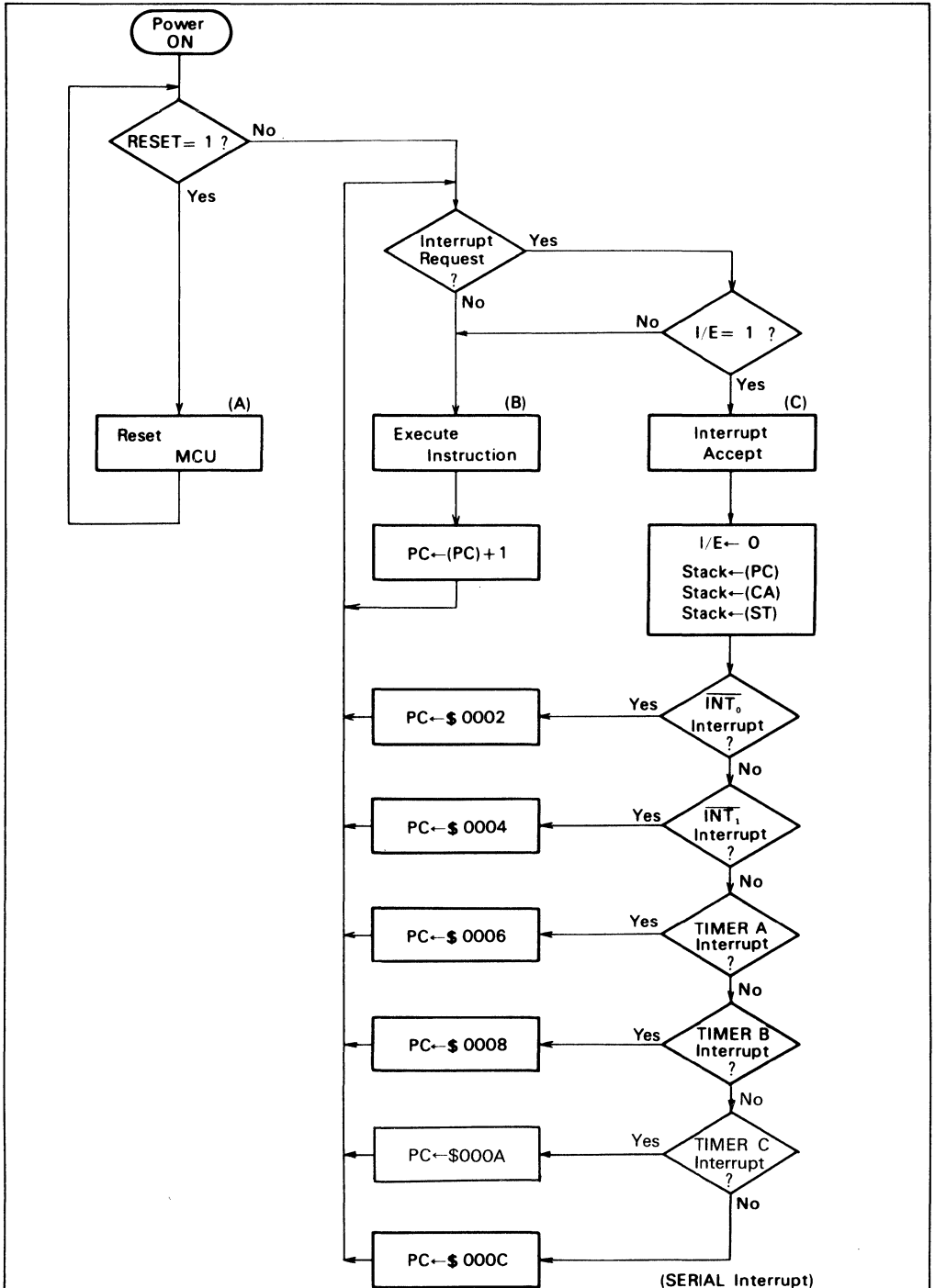


Figure 8. Interrupt Servicing Flowchart



Serial Interface

The serial interface transmits/receive 8-bit data in serial. This consists of the serial data register, the serial mode register, the port mode register A, the octal counter, and the multiplexer (figure 9). Pin $R0_0/\overline{SCK}$ and the transfer clock signal are controlled by the serial mode register. The data of the serial data register can be written in or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

The STS instruction starts serial interface operations and resets the octal counter to \$0. The octal counter starts to count at the falling edge of the transfer clock (\overline{SCK}) signal and increments by one at the rising edge of the \overline{SCK} . When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls

the $R0_0/\overline{SCK}$, prescaler divide ratio, and transfer clock source (table 14).

The write signal to the serial mode register controls the internal state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Data of the serial mode register will be changed from the second instruction of writing into the serial mode register. Therefore, it is required to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SRL: \$006, SRU: \$007): The 8-bit read/write serial data regis-

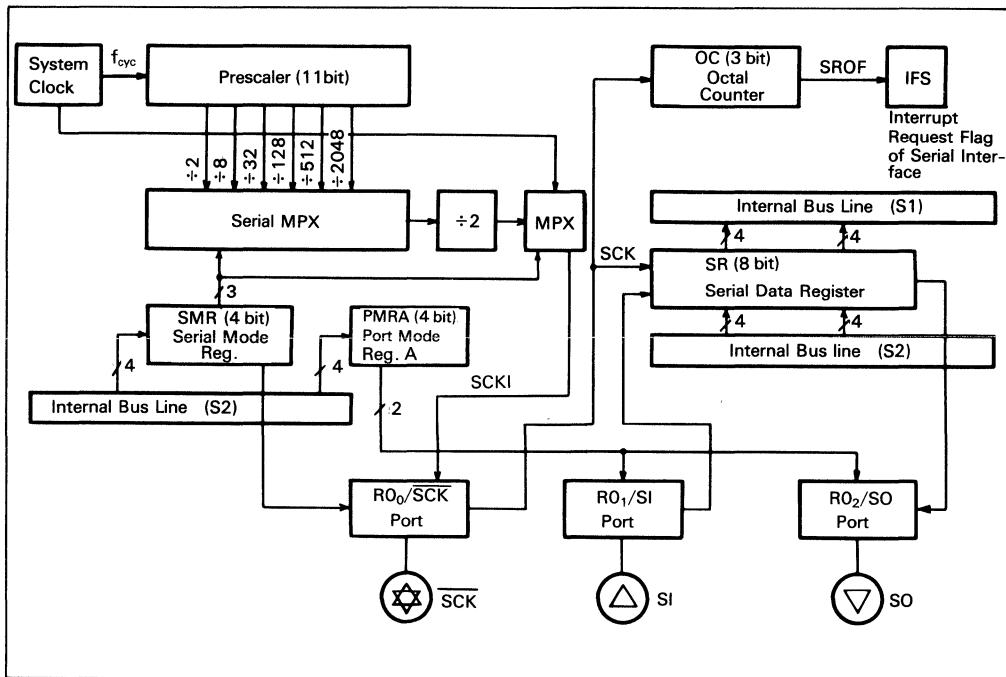


Figure 9. Serial Interface Block Diagram

ter consists of a low-order digit (SRL: \$006) and a high-order digit (SRU: \$007).

The data in the serial data register will be output from the SO pin of LSB synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the SI pin to the serial data register synchronously with the rising edge of the transfer clock. Figure 11 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Selection and Change of the Operation Mode: Table 15 shows the serial interface operation modes which are determined by a

combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by the write signal to the serial mode register in order to change the operation mode of the serial interface.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, SCK waiting state, and transfer state (figure 12).

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer

Table 14. Serial Mode Register

SMR3	RO ₀ /SCK
0	Used as RO ₀ port input/output pin
1	Used as SCK input/output pin

SMR2	SMR1	SMR0	RO ₀ /SCK Port	Transfer Clock			
				Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio	
0	0	0	SCK Output	Prescaler	÷ 2048	÷	4096
0	0	1	SCK Output	Prescaler	÷ 512	÷	1024
0	1	0	SCK Output	Prescaler	÷ 128	÷	256
0	1	1	SCK Output	Prescaler	÷ 32	÷	64
1	0	0	SCK Output	Prescaler	÷ 8	÷	16
1	0	1	SCK Output	Prescaler	÷ 2	÷	4
1	1	0	SCK Output	System Clock		÷	1
1	1	1	SCK Input	External Clock			



clock is applied. If an STS instruction is executed then, the serial interface shifts to SCK waiting state.

In this state, the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the octal counter counts-up and the serial data register shifts

simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously. The octal counter becomes 000 again by 8 external transfer clocks or by execution of STS instruction, so that the serial interface returns to SCK waiting state, and the serial

Table 15. Serial Interface Operating Mode

SMR3	PMRA1	PMRA0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

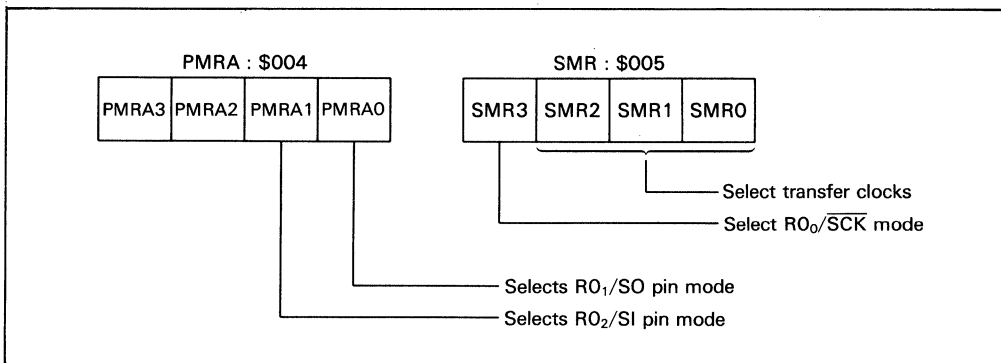


Figure 10. Configurations and the Functions of the Mode Registers

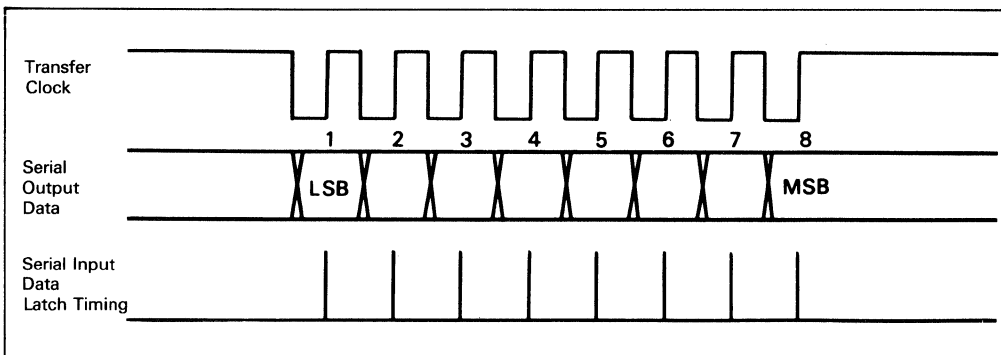


Figure 11. Serial Interface I/O Timing Chart

interrupt request flag is set simultaneously. In transfer state the octal counter becomes 000 by 8 internal transfer clocks, so that the serial interface enters to STS instruction waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops after 8 clocks.

Program the SMR again to initialize the

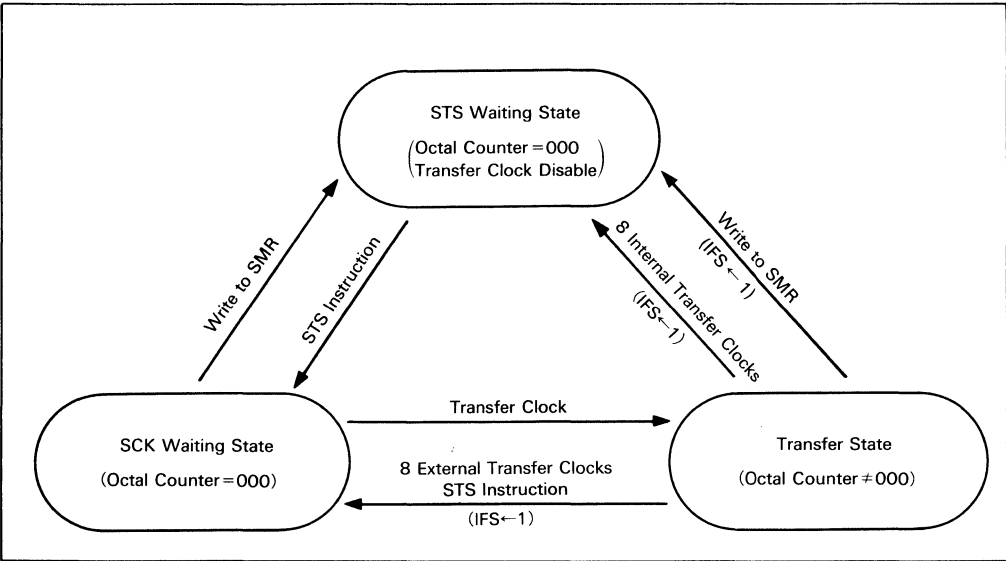


Figure 12. Serial Interface Operation State

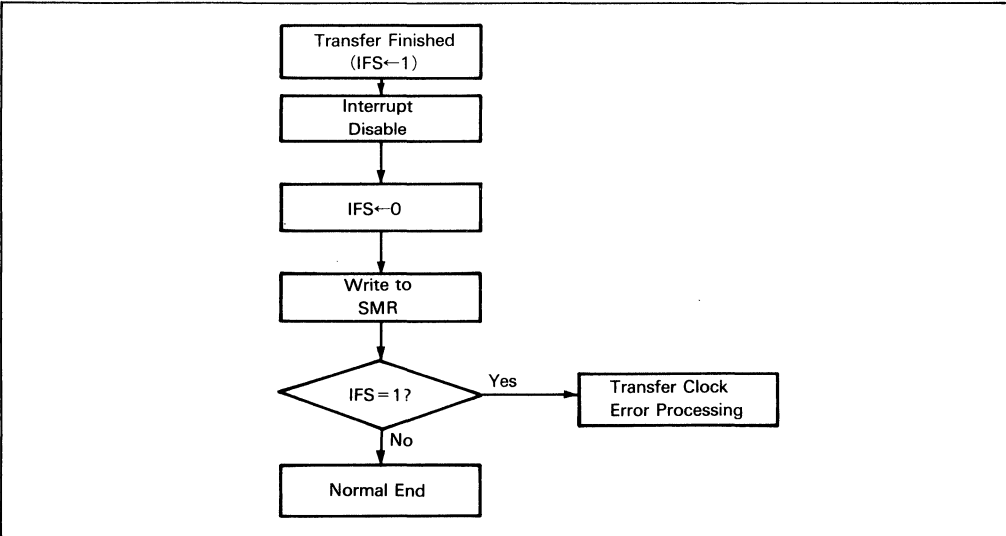


Figure 13. Example of Transfer Clock Error Detection



internal state of the serial interface when the PMRA is programmed in the transfer state or in the SCK waiting state. Then the serial interface goes into the STS waiting state.

Example of Transfer Clock Error Detection: The serial interface malfunctions when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 13.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts in the following sequence: first, transfer state, second, SCK waiting state, and third, transfer state again. The serial interrupt request flag should be reset before entering into the STS waiting state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

Timer

The MCU provides prescalers S and B (Each prescaler has the different input clock source individually), and 3 timers/counters (timers A, B, and C). Figures 14, 15 shows their diagrams.

Prescaler S: The input to the prescaler S is a

system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except by MCU reset and in the stop and watch modes. The prescaler provides input clock signals of timer A-C and the transfer clock of the serial interface. They can be selected by the timer mode registers A (TMA), B (TMB), C (TMC), and the serial mode register (SMR), respectively.

Prescaler W: The input to the prescaler W is a clock which divides X1 input clock into 8. The output of the prescaler W is available as an input clock for timer A by controlling the timer mode register (TMA).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up to \$FF, timer A is set to \$00 again, and generating overflow output. This leads to setting timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, timer A can function as an interval timer periodically generating overflow output at every 256th clock signal input.

To use timer A as a watch time base, set TMA3 to 1. The timer counter receives pres-

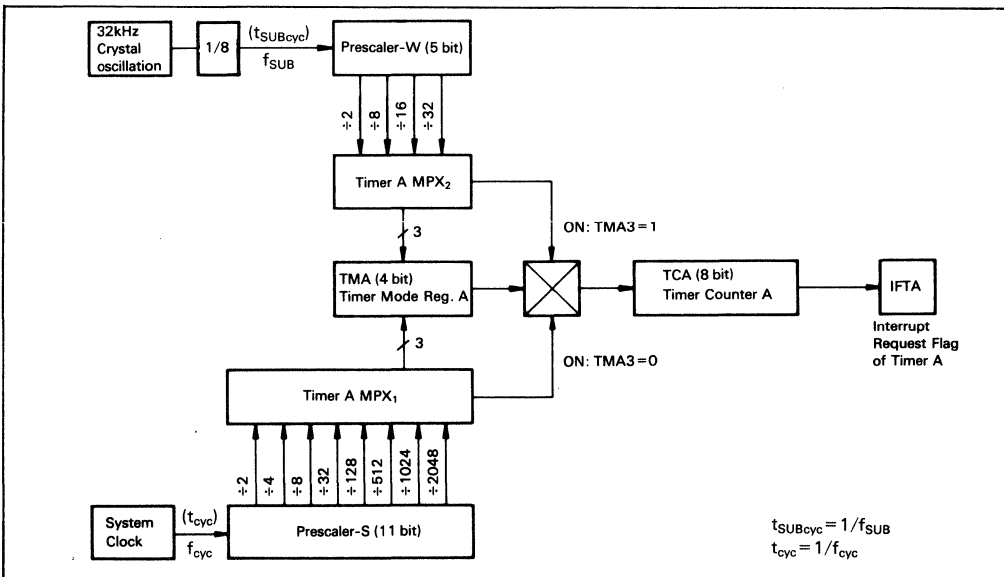


Figure 14. Timer A Block Diagram



caler W output, and timer A generates interrupts with an accurate timing (reference clock = 32kHz crystal oscillation). When you use timer A as a watch time base, prescaler W and timer counter can be initialized to \$0 by

setting timer mode register A.

The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

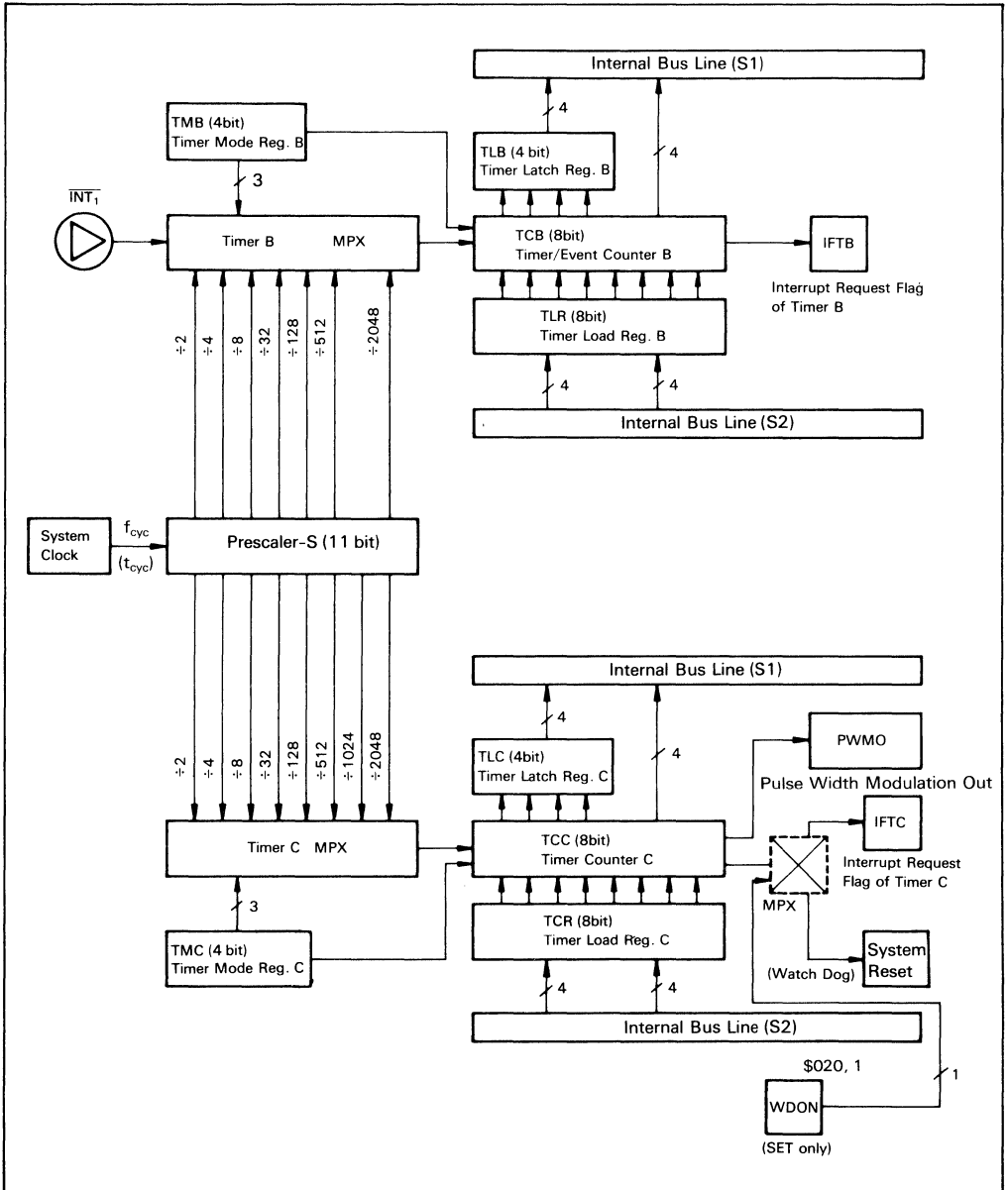


Figure 15. Timer B/Timer C Block Diagram



Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3/ \overline{INT}_1 as \overline{INT}_1 by the port mode register (PMR: \$004) control to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer C Operation: The timer mode register C (TMC: \$00D) selects the auto-reload function, and the prescaler divide ratio for timer C.

Timer C is initialized according to the data written into the timer load register by software. Timer C counts up at every clock input signal. When the next clock signal is applied to timer C after it is set to \$FF, it will generate an overflow output. In this case, if the auto-

reload function is selected, timer C is initialized according to the value of the timer load register. If it is not selected, timer C goes to \$00. The timer C interrupt request flag (IFTC: \$002 bit 2) will be set at this overflow output.

Timer C is also available as a watch dog timer for detecting a program out of sequence. An MCU reset occurs when the watch dog on flag (WDON) is 1 and the counter overflow output is generated by the program out of sequence. During timer C is stopped, the watchdog timer function is also stopped. In the standby mode, the function is enabled.

Timer C provides the duty variable pulse output function (PWMO). The output waveform differs depending on the contents of the timer mode register and the timer load register C (figure 16). When you select pulse output function, set R31/TIMO to TIMO by controlling the port mode register B. During timer C is stopped, this function is also stopped.

Timer Mode Register A (TMA: \$008): The timer mode register A is a 4-bit write only register which controls the timer A operation as table 16 shows. The timer mode register A is initialized to \$0 at MCU reset.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-

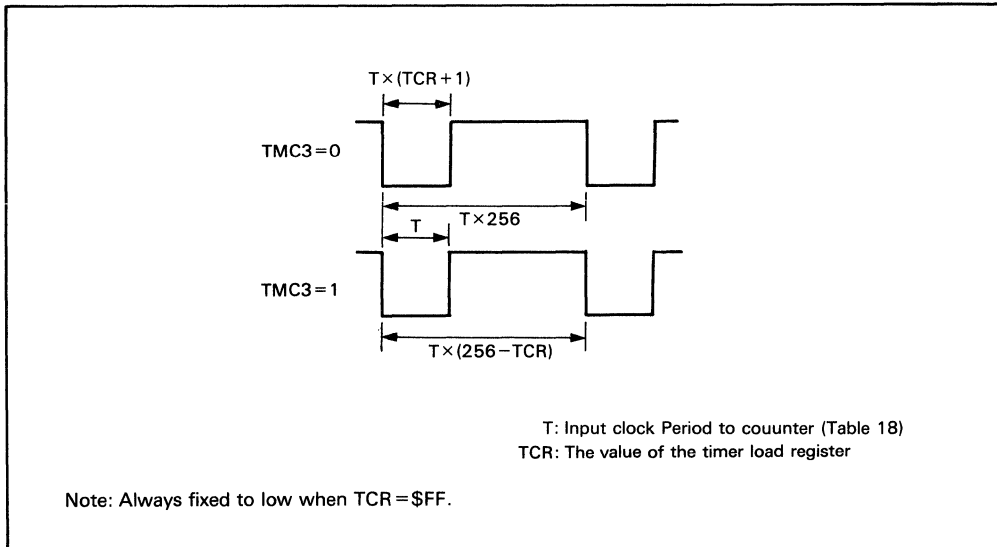


Figure 16. Variable Duty-Cycle Pulse Output Waveform



only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 17. The timer mode register B is initialized to \$0 by MCU reset.

The data of timer B changes from the second instruction cycle of the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed.

Timer Mode Register C (TMC: \$00D): The timer mode register C is a 4-bit write only register which selects the auto-reload function and prescaler divide ratio as table 18 shows. The timer mode register C is initialized to \$0 at MCU reset.

The contents of the timer mode register C can be changed from the second instruction cycle of writing into this. Therefore, it is required to initialize the timer C after the contents of the timer mode register C has been changed completely.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has low-order digits (TCBL: \$00A, TLRL: \$00A) and high-order digits (TCBU: \$00B, TLRU: \$00B). (Refer to figure 15.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digits first, and then the high-order digits. The timer/event

Table 16. Timer Mode Register A

TMA3	TMA2	TMA1	TMA0	Source prescaler, input clock period, operation mode
0	0	0	0	PSS, 2048 t_{cyc} Timer A mode
			1	PSS, 1024 t_{cyc}
		1	0	PSS, 512 t_{cyc}
			1	PSS, 128 t_{cyc}
	1	0	0	PSS, 32 t_{cyc}
			1	PSS, 8 t_{cyc}
		1	0	PSS, 4 t_{cyc}
			1	PSS, 2 t_{cyc}
1	0	0	0	PSW, 32 t_{SUBcyc} Time base mode
			1	PSW, 16 t_{SUBcyc}
		1	0	PSW, 8 t_{SUBcyc}
			1	PSW, 2 t_{SUBcyc}
	1	0	0	PSW, TCA reset
			1	
		1	0	
			1	

- Notes: 1. $t_{SUBcyc} = 244.14 \mu s$ (when 32.768 kHz crystal oscillation is used.)
 2. Timer counter overflow output cycle (s) = Input clock cycle(s) \times 256
 3. LCD enters into halt mode when PSW/TCA reset is selected during LCD display (Power switch OFF). To display LCD continuously, PSW/TCA reset time must be minimized by programming.



counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digits first, and then the low-order digits. The count value of the low-order digit is obtained when the high-order digit is read.

Timer C (TCCL: \$00E, TCCU: \$00F, TCRL: \$00E, TCRU: \$00F): Timer C is consisted of the 8-bit write-only timer load register and the 8-bit read-only timer/counter. These are individually consisted of low-order digits (TCCL: \$00E, TCRL: \$00E) and high-order digits (TCCU: \$00F, TCRU: \$00F). The operation mode of timer C is the same as that of timer B.

Table 17. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

Table 18. Timer Mode Register C

TMC3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{\text{INT}}_1$ (External Event Input)

TMC2	TMC1	TMC0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Input/Output

The MCU provides 26 I/O pins and 4 input only pins including 10 high current pins (15 mA max). 26 I/O pins contain pull-up MOS controllable by program.

When every I/O is used as an input, the data control register (DCR) controls ON/OFF of the output buffer. Table 19 shows the I/O pin circuit type.

The configuration of I/O buffers are shown in figure 19.

Table 19. I/O Pin Circuit Type

I/O pins	Circuit	Applicable pins
I/O common pins (with pull-up MOS)		<p>D₀-D₉ R₀-R₃ R₁₀-R₁₃ R₂₀-R₂₃ R₃₀-R₃₃</p>
		<p>$\overline{\text{SCK}}$</p>
Output pins (with pull-up MOS)		<p>SO TIMO</p>
Input pins		<p>$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$ SI</p>
		<p>D₁₀ D₁₁/VCreff</p>
		<p>D₁₂/COMPO D₁₃/COMP1 (Multiplexed with analog inputs)</p>

Note: Refer to table 20, Note 3 about R₀₂/SO.



Port D: Port D is consisted of 10 1-bit I/O ports and 4 input ports. Ports D₀-D₉ are high current I/O ports (15 mA max). The sum of the current for all ports is up to 100mA. Port D can be set/reset by SED/RED and SEDD/REDD instructions, and can be tested by TD/TDD instructions. An output data is stored in the port data register.

ON/OFF of the output buffer for port D can be controlled by the data control registers for port D (DCRB, DCRC, DCRD). The DCR is located on the memory address area. Pins D₁₀-D₁₃ are input only pins.

Two operation modes are available to pins D₁₂ and D₁₃: digital input mode and analog input mode. The operation modes can be selected by the port mode register (PMRB; bits 1, 0). In the digital input mode, these pins can be used as input with the same characteristics as other I/O pins. In the analog input mode, users can read the result of the comparison between the reference voltage as an input data. The reference voltage is input by D₁₁/VCref.

Port R: Port R, consisted of 16 4-bit I/O ports, can receive/transmit data by LAR/LRA and LBR/LRB instructions. An output data is stored in data register (PDR) of each pin.

ON/OFF of the output buffer for port R can be controlled by the data control registers for port R (DCR0-DCR3).

The DCR is located on the memory address area.

Pins R₀, R₁, R₂ are multiplexed with \overline{SCK} , SI, SO, respectively.

Pins R₃, R₃, R₃ are multiplexed with TIMO, INT₀, INT₁, respectively. Refer to figure 18.

Controlling the pull-up MOS: All I/O ports, except for pins D₁₀-D₁₃, contain pull-up MOS controllable by program.

Bit 3 of the port mode register B (PMRB3) controls ON/OFF of all pull-up MOS simultaneously. Pull-up MOS is controlled by the port data register (PDR) of each pin. Therefore, each bit of pull-up MOS can be individually ON and OFF. Refer to table 20.

Unused I/O Pins: If unused pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent this; pull-up with V_{CC} through internal pull-up MOS, or pull-up with V_{CC} through a resistor 100kΩ approx.

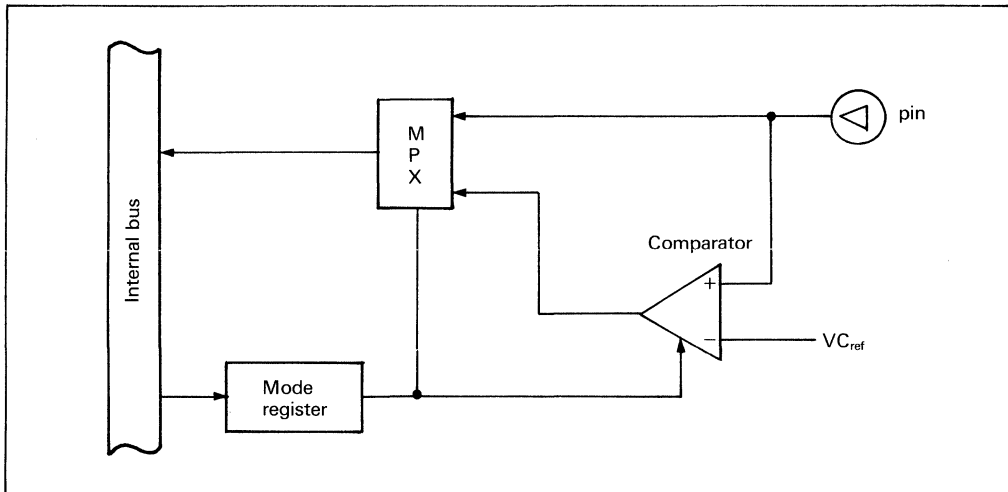


Figure 17. Configuration of D₁₂, D₁₃

Table 20. Input/Output by Program Control

PRMB; bit 3	0		1					
DCR	0	1	0	1				
PDR	0	1	0	1	0	1	0	1
PMOS (A)	-	-	-	ON	-	-	-	ON
NMOS (B)	-	-	ON	-	-	-	ON	-
Pull-up MOS	-	-	-	-	-	ON	-	ON

Notes: 1. - : OFF

- Combine the values of the mode registers above (PMRB3, DCR, PDR) to select input/output for PMOS (A), NMOS (B), and the pull-up MOS individually.
The DCR and the PDR control each pin. And the PMRB3 controls ON/OFF of all pull-ups.
- The second bit of the miscellaneous register (MIS2) controls RO₂/SO. When MIS2 is 1, PMOS (A) is OFF.

MIS2	RO ₂ /SO
0	PMOS (A)
0	ON
1	OFF

- Correspondence between DCR's and pins are shown below:

DCR	bit 3	bit 2	bit 1	bit 0
DCR0	RO ₃	RO ₂	RO ₁	RO ₀
DCR1	R1 ₃	R1 ₂	R1 ₁	R1 ₀
DCR2	R2 ₃	R2 ₂	R2 ₁	R2 ₀
DCR3	R3 ₃	R3 ₂	R3 ₁	R3 ₀
DCRB	D3	D2	D1	D0
DCRC	D7	D6	D5	D4
DCRD	-	-	D9	D8

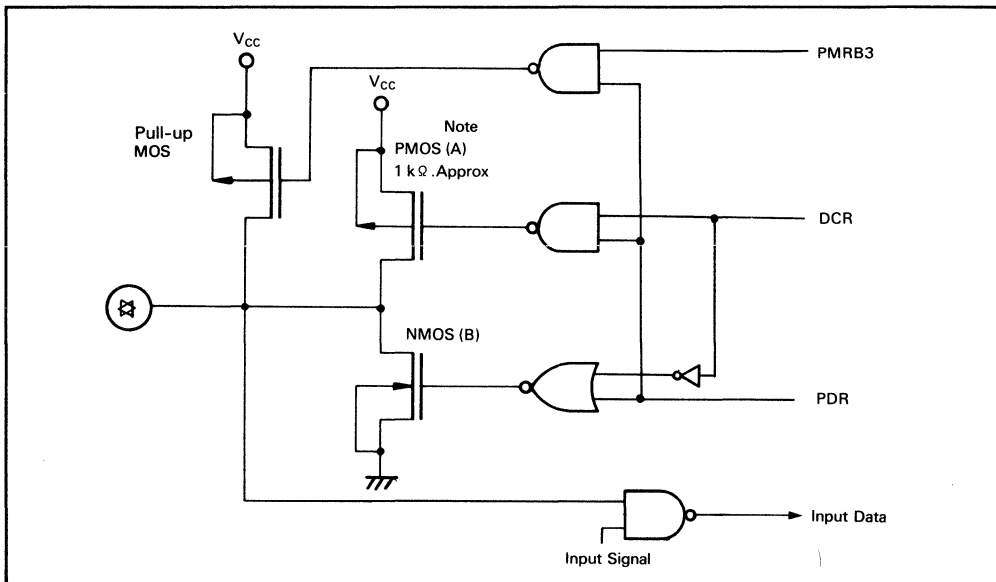


Figure 19. Configuration of the Input/Output Buffer

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when obtaining the stabilization time for oscillator, apply the RESET input for at least t_{RC} . In all other cases, at least

two instruction cycles of RESET input are required for the MCU reset.

Table 21 shows the parts initialized by MCU reset, and the status of each.

Table 21. Initial Value After MCU Reset

Items		Initial value by MCU reset	Contents
Program Counter	(PC)	\$0000	Execute program from the top of the ROM address.
Status	(ST)	1	Enable to branch with conditional branch instructions
Stack Pointer	(SP)	\$3FF	Stack level is 0
Register V (Bank Register) (V)		0	Bank 0 (Memory)
Interrupt	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
Flag/Mask	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Masks interrupt request
I/O	Port Data Register (PDR)	All bits are 1	Enable to transmit high
	Data Control Register (DCR)	All bits are 0	Output buffer is OFF (high impedance)
	Port Mode Register A (PMRA)	0000	See port mode register A
	Port Mode Register B (PMRB)	0000	See port mode register B
Timer/Counter	Timer Mode Register A (TMA)	0000	See timer mode register A
Serial Interface	Timer Mode Register B (TMB)	0000	See timer mode register B
	Timer Mode Register C (TMC)	0000	See timer mode register C
	Serial Mode Register (SMR)	0000	See serial mode register
	Prescaler S	\$000	—
	Prescaler W	\$00	—
	Timer Counter A (TCA)	\$00	—
	Timer Counter B (TCB)	\$00	—
	Timer Counter C (TCC)	\$00	—
	Timer Load Register B (TLR)	\$00	—
	Timer Load Register C (TCR)	\$00	—
	Octal Counter	000	—

Table 21. Initial Value After MCU Reset (Cont)

Items		Initial value by MCU reset	Contents
LCD	LCD Control Register (LCR)	000	See LCD control register
	LCD Mode Register (LMR)	0000	See LCD duty/clock control
DTMF Generator	Tone Generator Control Register (TGC)	000	See tone generator control register
	Tone Generator Mode Register (TGM)	0000	See generator mode register
Bit Register	Low Speed On Flag (LSON)	0	See low power dissipation mode
	Watch Dog Timer ON Flag (WDON)	0	See timer C
	Tone Generator Speed Flag (TGSP)	0	See DTMF generation circuit
Miscellaneous Register	(MIS)	000	—

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
Register B	(B)		
Register W	(W)		
Registers X/SPX	(X/SPX)		
Registers Y/SPY	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

Internal Oscillator Circuit

Figure 20 gives an internal oscillator circuit. Ceramic filter can be connected to OSC₁-

OSC₂. 32.768 kHz crystal oscillator can be connected to X1, X2. External clock operation is available to the system oscillator.

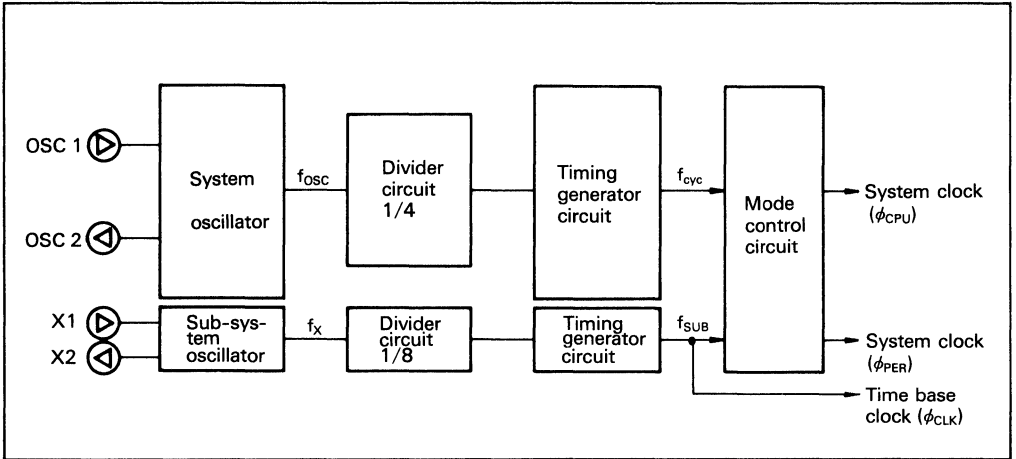


Figure 20. Internal Oscillator Circuit

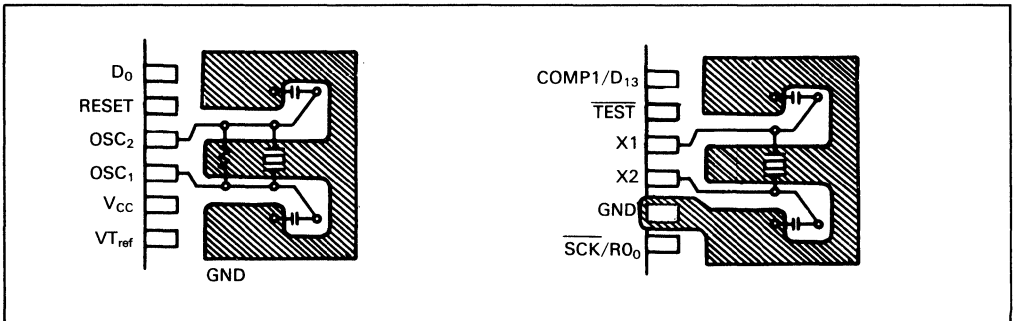
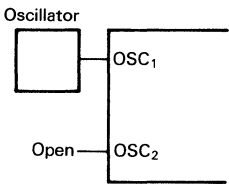
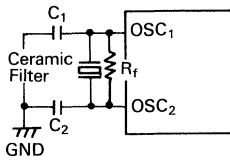
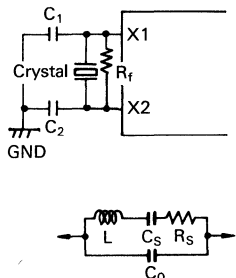


Figure 21. Layout of Crystal and Ceramic Filter

Table 22. Examples of Oscillator Circuit

	Circuit Configuration	Circuit Constants
External clock Operation		
Ceramic filter oscillator		<p>Ceramic filter: CSB400P (Murata) $R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 220\text{ pF} \pm 5\%$ Ceramic filter: CSB800J (Murata) $R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 220\text{ pF} \pm 5\%$</p>
Crystal oscillator		<p>Crystal: 32.768kHz: MX38T (Nippon Denpa Kogyo) $R_s = 14\text{ k}$ $C_0 = 1.5\text{ pF}$ $C_1 = 6\text{ pF} \pm 20\%$ $C_2 = 20\text{ pF} \pm 20\%$</p>

- Notes: 1. On the crystal and ceramic filter resonator, the upper circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring among OSC₁, OSC₂ (X1, X2) and elements should be as short as possible, and never cross the other wirings. Refer to figure 21.
3. When the crystal (32.768 kHz) is not used, the X1 pin must be fixed to V_{CC} and the X2 pin must be opened.

Liquid Crystal Display (LCD)

The MCU contains 4 common signal pins, the controller, and the driver. The controller and the driver drive 32 segment signal pins. The controller is consisted of display data RAM, the LCD control register (LCR), and the duty/clock control register (LMR) (figure 22). 4 kinds of duties and the LCD clocks are

available by program control. And the MCU contains the dual port RAM. Thus displayed data can be transferred to segment signal pins automatically without program control. When you select 32kHz oscillation clock as a LCD clock source, the system allows the LCD display even in the watch mode in which the system clock halts.

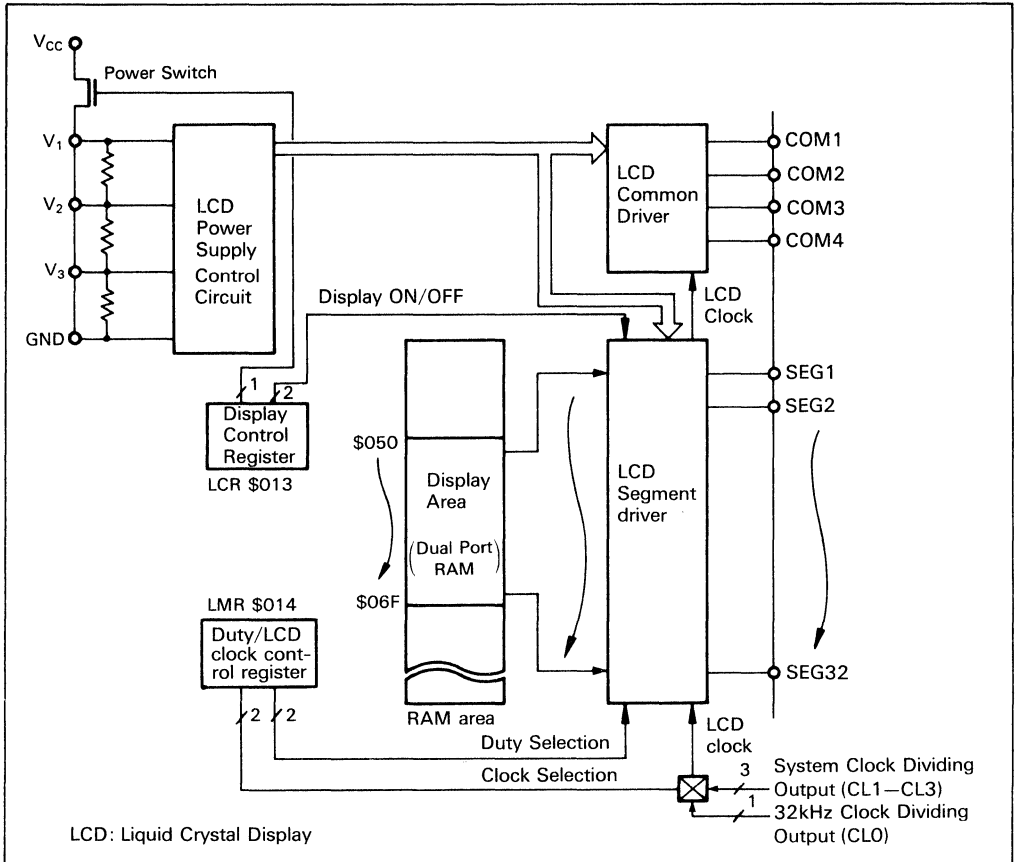


Figure 22. LCD Driver Configuration

LCD Data Area and Segment Data (\$050-\$06F): Figure 23 shows a configuration of LCD RAM area. Each bit of this area, corresponds to 4 types of duties, can be transmitted to segment as a display data by programming the area corresponding to the duty.

LCD Control Register (LCR: \$013): The LCD control register is a 3-bit write only register which controls the blanking of the LCD, ON/OFF of the power switch and the display in the watch mode/subactive mode (table 23).

- Blank/Display
Blank: Segment signal is faden irrespective of the LCD RAM data.
Display: LCD RAM data is transmitted as a

segment signal.

- Power Switch ON/OFF
OFF: Power switch is off.
ON: Power switch is on, and V_1 is V_{CC} .
- Watch Mode/Subactive mode Display
OFF: In the watch mode/subactive mode, all common/segment pins are fixed to GND. And power switch is off.
ON: In the watch mode/subactive mode, LCD RAM data is transmitted as a segment signal.

LCD Duty/Clock Control Register (LMR: \$014): The LCD duty/clock control register is a write only register which specifies 4 kinds of display duties and reference clock for LCD (table 24).

	bit 3	bit 2	bit 1	bit 0		bit 3	bit 2	bit 1	bit 0	
80	SEG 1	SEG 1	SEG 1	SEG 1	\$050	96	SEG 17	SEG 17	SEG 17	\$060
81	SEG 2	SEG 2	SEG 2	SEG 2	\$051	97	SEG 18	SEG 18	SEG 18	\$061
82	SEG 3	SEG 3	SEG 3	SEG 3	\$052	98	SEG 19	SEG 19	SEG 19	\$062
83	SEG 4	SEG 4	SEG 4	SEG 4	\$053	99	SEG 20	SEG 20	SEG 20	\$063
84	SEG 5	SEG 5	SEG 5	SEG 5	\$054	100	SEG 21	SEG 21	SEG 21	\$064
85	SEG 6	SEG 6	SEG 6	SEG 6	\$055	101	SEG 22	SEG 22	SEG 22	\$065
86	SEG 7	SEG 7	SEG 7	SEG 7	\$056	102	SEG 23	SEG 23	SEG 23	\$066
87	SEG 8	SEG 8	SEG 8	SEG 8	\$057	103	SEG 24	SEG 24	SEG 24	\$067
88	SEG 9	SEG 9	SEG 9	SEG 9	\$058	104	SEG 25	SEG 25	SEG 25	\$068
89	SEG 10	SEG 10	SEG 10	SEG 10	\$059	105	SEG 26	SEG 26	SEG 26	\$069
90	SEG 11	SEG 11	SEG 11	SEG 11	\$05A	106	SEG 27	SEG 27	SEG 27	\$06A
91	SEG 12	SEG 12	SEG 12	SEG 12	\$05B	107	SEG 28	SEG 28	SEG 28	\$06B
92	SEG 13	SEG 13	SEG 13	SEG 13	\$05C	108	SEG 29	SEG 29	SEG 29	\$06C
93	SEG 14	SEG 14	SEG 14	SEG 14	\$05D	109	SEG 30	SEG 30	SEG 30	\$06D
94	SEG 15	SEG 15	SEG 15	SEG 15	\$05E	110	SEG 31	SEG 31	SEG 31	\$06E
95	SEG 16	SEG 16	SEG 16	SEG 16	\$05F	111	SEG 32	SEG 32	SEG 32	\$06F
	COM 4	COM 3	COM 2	COM 1		COM 4	COM 3	COM 2	COM 1	

Figure 23. Configuration of LCD RAM Area

Table 23. LCD Control Register

LCR bit 2	Watch Mode/Sub-Active Mode Display	LCR bit 1	Power Switch ON/OFF	LCR bit 0	Blank /Display
0	OFF	0	OFF	0	Blank
1	ON	1	ON	1	Display

Note: In case of LCD in the watch mode, use divider output of 32kHz oscillator as an LCD clock and set LCR bit2 to 1. When system oscillator divider output is used as an LCD clock, set LCD bit2 to 0.

Table 24. LCD Duty/Clock Control Register

LMR				
bit 3	bit 2	bit 1	bit 0	Duty Select/Input Clock Select
		0	0	1/4 Duty
		0	1	1/3 Duty
		1	0	1/2 Duty
		1	1	Static
0	0			CL0 (32.768kHz/64; when 32.768kHz oscillator is used)
0	1			CL1 ($f_{cyc}/256$)
1	0			CL2 ($f_{cyc}/2048$)
1	1			CL3 (Refer to table 25.)

Note: f_{cyc} is a system oscillator divider output.

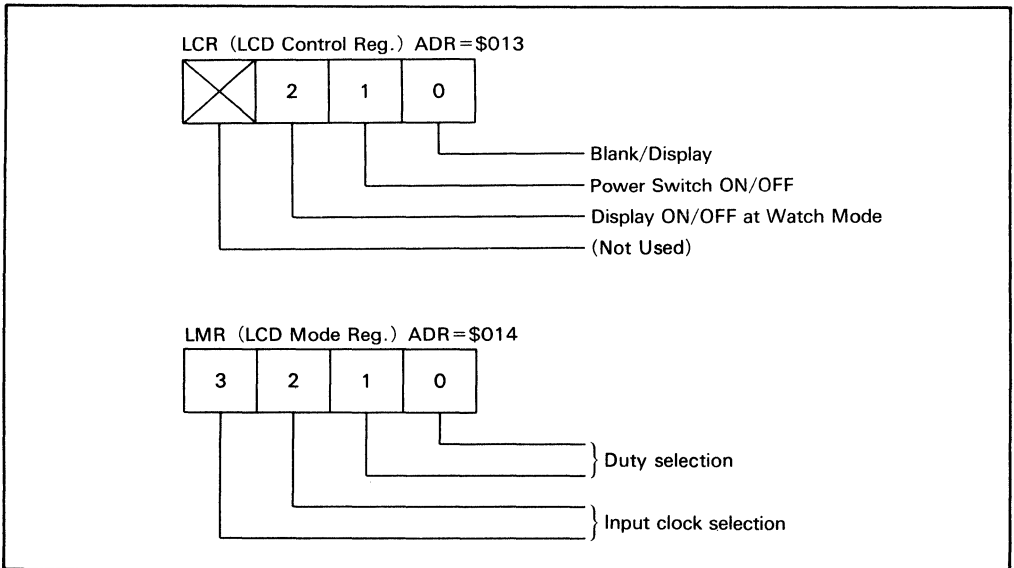


Figure 24. LCD Control Register

Table 25. LCD Frame Frequency

Duty		Static							
Instruction Cycle Time	LMR	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2
		0	0	0	1	1	0	1	1
		CL0		CL1		CL2		CL3	*
10μs		512Hz		390.6Hz		48.8Hz		24.4Hz/64Hz	
5μs		512Hz		781.2Hz		97.6Hz		48.8Hz/64Hz	

Duty		1/2 Duty							
Instruction Cycle Time	LMR	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2
		0	0	0	1	1	0	1	1
		CL0		CL1		CL2		CL3	*
10μs		256Hz		196.3Hz		24.4Hz		12.2Hz/32Hz	
5μs		256Hz		390.6Hz		48.8Hz		24.4Hz/32Hz	

Duty		1/3 Duty							
Instruction Cycle Time	LMR	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2
		0	0	0	1	1	0	1	1
		CL0		CL1		CL2		CL3	*
10μs		170.6Hz		130.2Hz		16.3Hz		8.1Hz/21.3Hz	
5μs		170.6Hz		260.4Hz		32.6Hz		16.2Hz/21.3Hz	

Duty		1/4 Duty							
Instruction Cycle Time	LMR	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2	bit 3	bit 2
		0	0	0	1	1	0	1	1
		CL0		CL1		CL2		CL3	*
10μs		128Hz		97.7Hz		12.2Hz		6.1Hz/16Hz	
5μs		128Hz		195.4Hz		24.4Hz		12.2Hz/16Hz	

* Division ratio differs depending on the value of bit 3 of the timer mode register (TMA3).
(TMA3 = 0/TMA3 = 1)

TMA3=0	CL3 = $f_{cyc}/4096$
TMA3=1	CL3 = 32.768 kHz/512



Large LCD Panel Driving and Driving Voltage (V_{LCD}): When using the large LCD panel, lower the dividing resistance by implementing the external resistors parallel to the internal dividing resistors (See the following figure).

Since the liquid crystal display board is of matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, as it

varies depending on display condition, a value of resistance cannot be simply determined by referring to the load capacitance of liquid crystal display. A value of resistance must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented.

Capacitor C (0.1 to 0.3 μF) is recommended to be attached. In general, R is 1 k Ω to 10 k Ω .

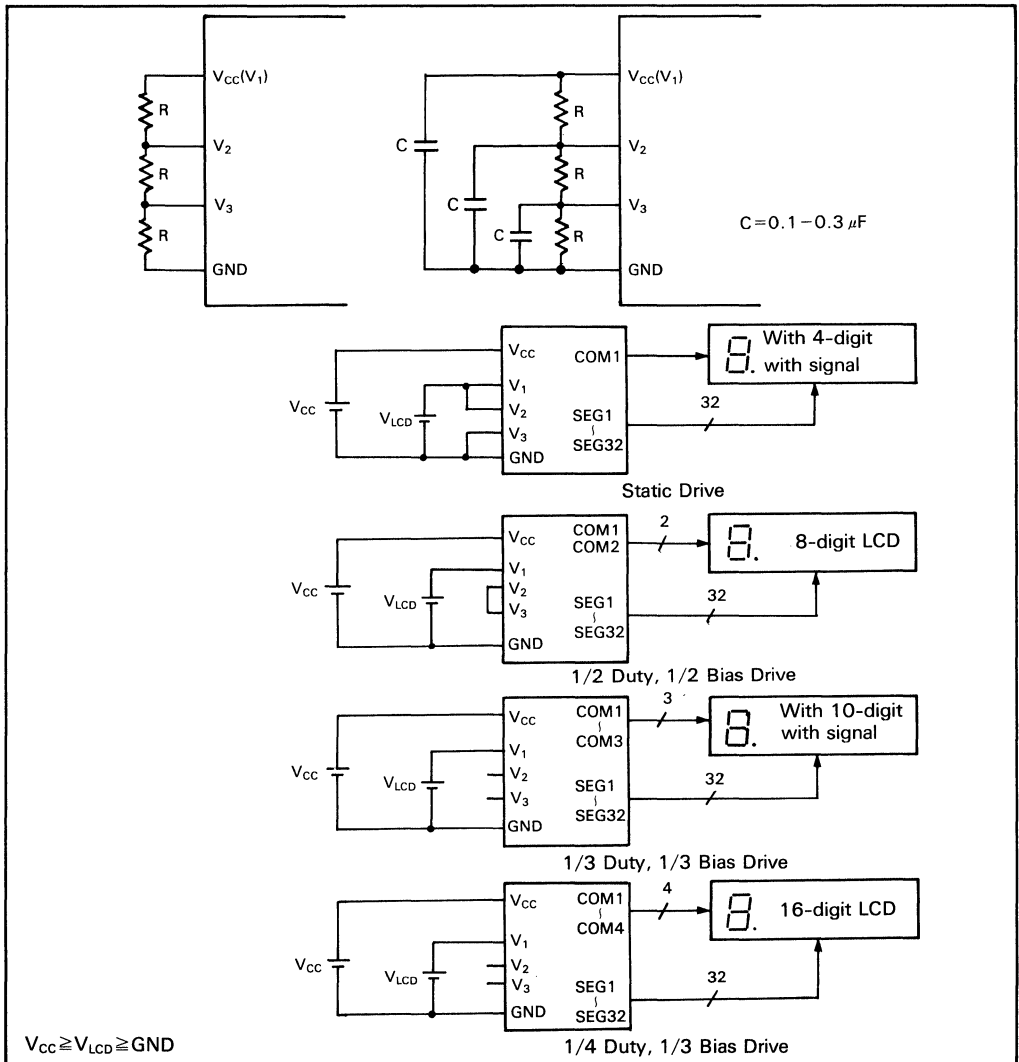


Figure 25. An Example of LCD Connection



The following figure shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, power supply switch for dividing resistor (power switch) should be turned OFF (Bit 1 of the LCR register is 0).

DTMF Generation Circuit

The MCU provides a dual tone multi-frequency (DTMF) generation circuit.

The DTMF signal consists of two sine waves to access the switching system.

Figure 26 shows DTMF keypad and frequencies. Press one of the keys to generate tones which corresponds to each frequencies. Figure 27 shows a block diagram of DTMF circuit.

The MCU uses oscillation frequency reduced to 400kHz, a eighth of conventional one, to realize a low power consumption. In this case, the problem is a frequency deviation. The MCU provides transformed programmable dividers in addition to sine wave counters

and a control register to reduce a frequency deviation.

The DTMF generation circuit is controlled by the following three registers.

Tone Generator Mode Register (TGM: \$010): The TGM register is a 4-bit write-only register which controls output frequencies (table 26), and is cleared to \$0 at MCU reset.

Tone Generator Control Register (TGC: \$011): The TGC register is a 3-bit write-only register which controls start/stop of DTMF signal output (table 27), and is cleared to \$0 at MCU reset.

Tone Generator Speed Flag (TGSP: \$020, 2): The TGSP flag is a 1-bit register which can be set/reset by SEM/REM and SEMD/REMD instruction. The DTMF generation circuit generates output frequencies as table 26 shows when 400kHz clock is selected. When 800kHz clock is selected, the DTMF generation circuit generates equivalent frequencies by pulling TGSP flag high.

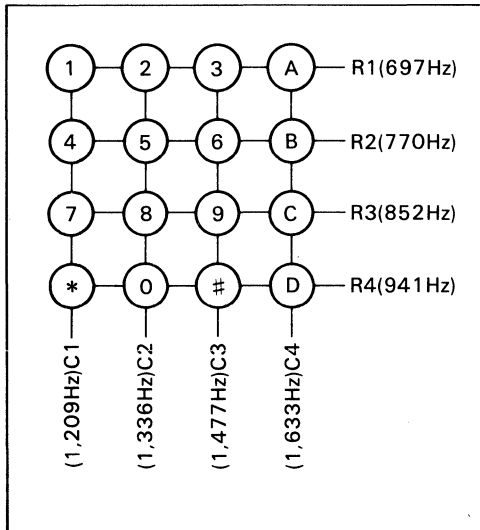


Figure 26. DTMF Keypad and Frequencies

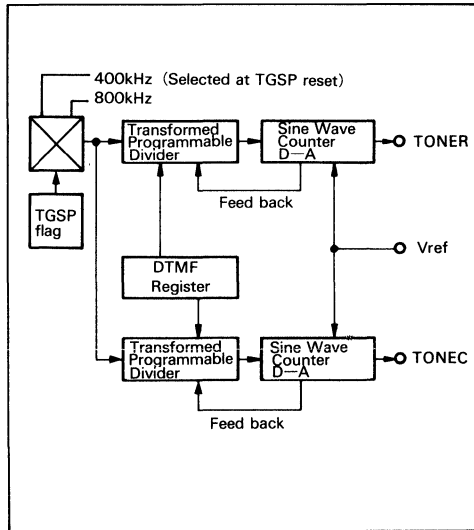


Figure 27. Block Diagram of DTMF Circuit

Table 26. Tone Generator Mode Register

TGM				
bit 3	bit 2	bit 1	bit 0	Output Frequencies
Option		0	0	f _{R1} (: 697Hz) Output through
(TONER output		0	1	f _{R2} (: 770Hz) TONER pin
is not affected)		1	0	f _{R3} (: 852Hz)
		1	1	f _{R4} (: 941Hz)
0	0	Option		f _{C1} (: 1,209Hz) Output through
0	1	(TONEC output		f _{C2} (: 1,336Hz) TONEC pin
1	0	is not affected)		f _{C3} (: 1,477Hz)
1	1			f _{C4} (: 1,633Hz)

Table 27. Tone Generator Control Register

TGC1	DTMF Enable Bit
0	DTMF Disable
1	DTMF Enable

TGC2	TONER Output Control (Row)
0	Stop
1	TONER Output (Active)

TGC3	TONEC Output Control (Column)
0	Stop
1	TONEC Output (Active)

DTMF Output: The sine waves of row-group and high-group are individually converted from digital to analog in the D/A conversion circuit which provides high precision ladder resistance. The DTMF output pins (TONER, TONEC) transmits the sine waves of row-group and high-group, respectively. Figure 28

shows the TONE output equivalent circuit. Figure 29 shows the output waveform. One cycle of this wave consists of 32 slots. Therefore, the output waveform is stable with little distortion. And table 28 details the frequency deviation of the MCU from standard DTMF signals.

Table 28. Frequency Deviation of the MCU from Standard

Standard DTMF (Hz)	MCU (Hz)	Deviation from Standard (%)
R1 697	694.44	-0.37
R2 770	769.23	-0.10
R3 852	851.06	-0.11
R4 941	938.97	-0.22
C1 1,209	1,212.12	0.26
C2 1,336	1,333.33	-0.20
C3 1,477	1,481.48	0.30
C4 1,633	1,639.34	0.39

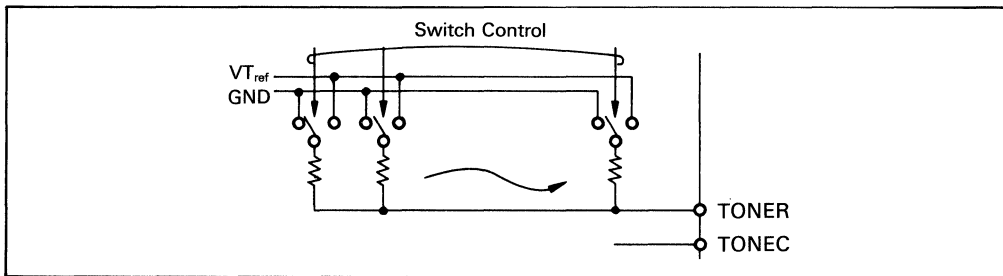


Figure 28. Tone Output Equivalent Circuit

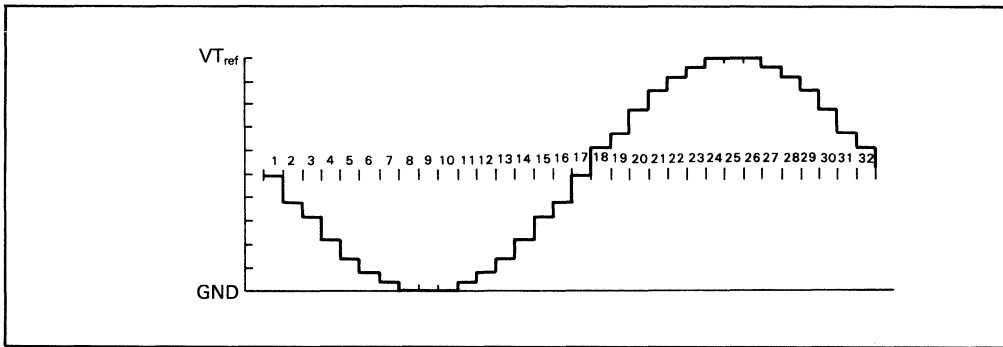


Figure 29. Waveform of Tone Output

Operating Modes

Low Power Dissipation Mode

The MCU has five low power dissipation modes.

Active Mode: In the active mode, the MCU operates through clocks generated in the oscillator circuits: OSC₁ and OSC₂.

Standby mode: Execute SBY instruction to put the MCU into the standby mode from the active mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter, and the serial interface working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they

were in just before the MCU went into standby mode.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 after instruction execution, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction. (figure 31)

Figurer 31 shows the flowchart of the standby mode.

Table 29. Low Power Dissipation Mode Function

Operating Mode	Activated by	Condition									
		System oscillator	Sub-system oscillator	Instruction execution (ϕ_{CPU})	Peripheral interrupt (ϕ_{PER})	Clock interrupt (ϕ_{CLK})	RAM	Register/Flag	I/O	Released by	
Active mode	RESET release Interrupt request	Active	Active	Active	Active	Active	Active	Active	Active	Active ³	RESET input STOP/SBY instruction
Standby mode	SBY instruction	Active	Active	Stop	Active	Active	Hold	Hold	Hold	Hold	RESET input Interrupt request
Stop mode	TMA3=0, Stop instruction	Stop	Active ¹	Stop	Stop	Stop	Hold	Reset	High impedance ³	High	RESET input
Watch mode	TMA3=1, Stop instruction	Stop	Active	Stop	Stop	Active ²	Hold	Hold	Hold ³	Hold	Reset input INT ₀ or Time A interrupt request
Sub-active ⁴ mode	INT ₀ from watch mode or Timer A interrupt request	Stop	Active	Active	Stop	Active ²	Active	Hold/Active	Active ³	Active	RESET input STOP/SBY instruction


- Notes: 1. When you minimize the I_{CC}, stop the oscillation by external circuit.
 2. Refer to interrupt frame section for details.
 3. Refer to table 30.
 4. Sub-active mode is a functional option specified via function option list.
 5. On using watch mode or Sub-active mode, 32.768 kHz Crystal oscillator is essential for MCU.

Table 30. I/O State in the Low Power Dissipation Mode

	Output		Input
	Standby mode, Watch mode	Stop mode	Active mode, Sub-active
D ₀ -D ₉	Retained	High impedance	Input enable
D ₁₀ -D ₁₃			Input enable
RO-R3	Retained	High impedance	Input enable

Table 31. Operations in the low power dissipation mode

Functions	Stop mode	Watch mode	Standby mode	Sub-active mode³
CPU	Reset	Hold	Hold	Active
RAM	Hold	Hold	Hold	Active
Timer A	Reset	Active	Active	Active
Timer B	Reset	Stop	Active	Stop
Timer C	Reset	Stop	Active ²	Stop
Serial	Reset	Stop ⁴	Active	Stop ⁴
LCD	Reset	Active/ Stop	Active	Active/ Stop
DTMF	Reset	Reset	Active	Reset
I/O	Reset ¹	Hold ¹	Hold	Active

- Notes: 1. Output pins are in the high impedance state.
 2. : in operation
 3. Sub-active mode is a functional option specified via functional option list.
 4. When a clock is input in the external clock mode, transmit-receive operation is performed (Interrupt processing stops).

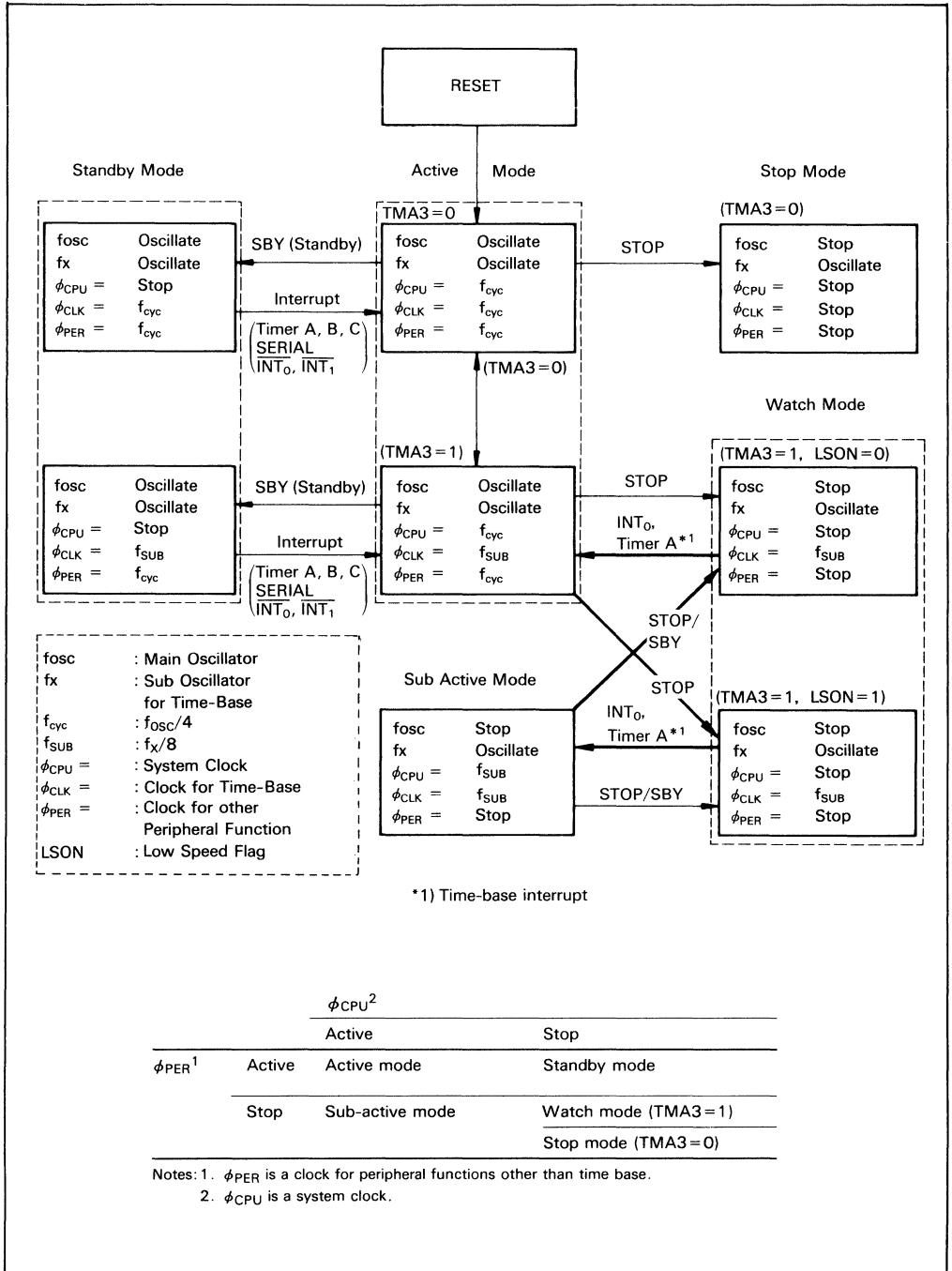


Figure 30. MCU Operation Mode Transfer

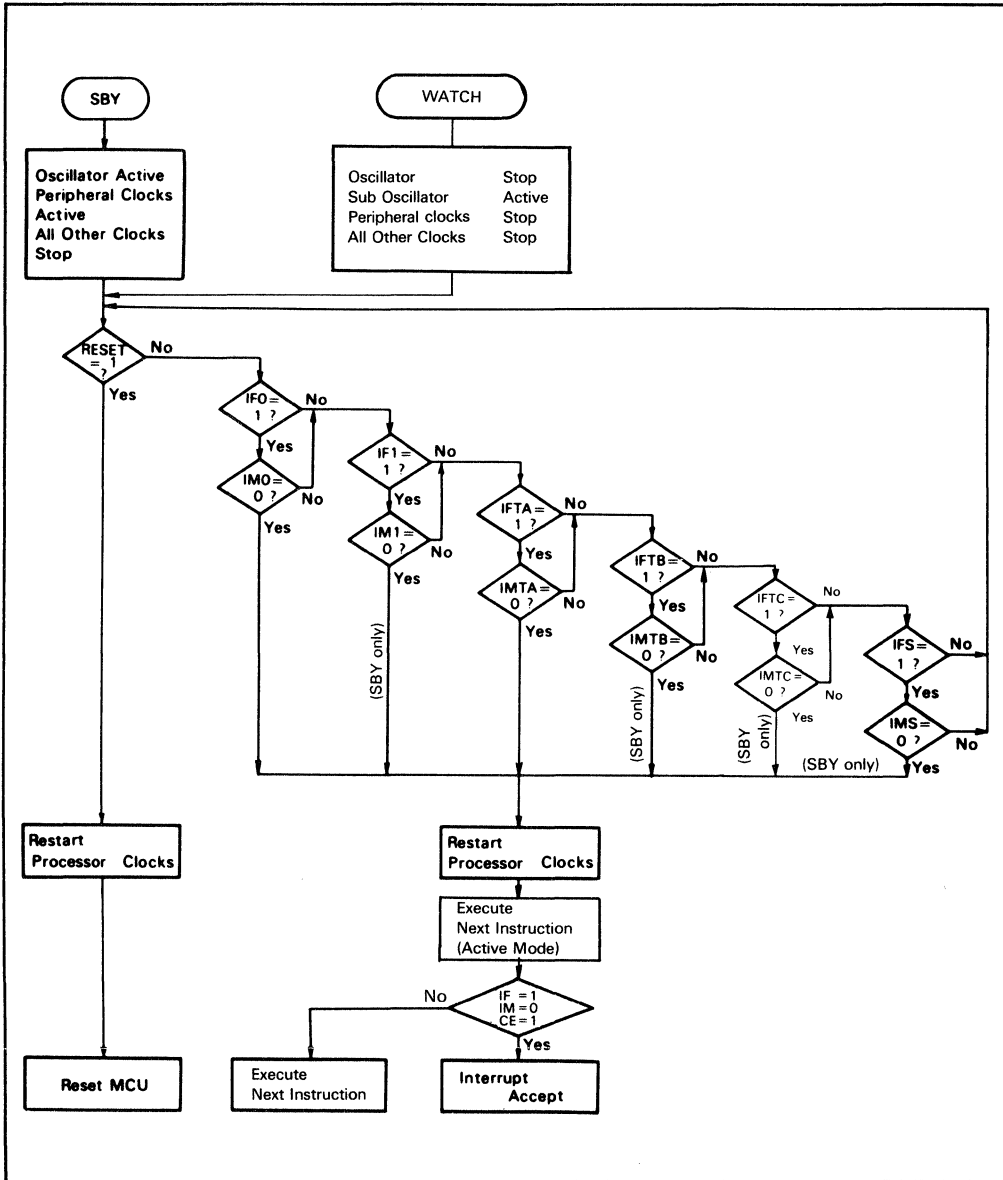


Figure 31. MCU Operating Flowchart

Stop Mode: Execute STOP instruction to put the MCU into the stop mode when the MCU is in the active mode and TMA3 is 0. In the stop mode, oscillator circuit and every function of the MCU stops.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 32, reset input must be applied at least to t_{RC} to stabilize oscillation (Refer to AC Characteristics table). After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, register B, register W, registers X/SPX and Y/SPY, and carry may not retain contents.

Watch Mode: The MCU enters Watch mode by the STOP instruction during Active mode

and TMA3=1 or by the STOP or SBY instruction during Sub Active mode. Watch mode can be canceled by the RESET input or timer A/ \overline{INT}_0 interrupt request. For a detailed description of the RESET input in canceling mode, see Stop mode section. If Watch mode is canceled by the timer A/ \overline{INT}_0 interrupt request, the MCU enters either Active mode or Sub Active mode depending on the state of the LSON bit. When the MCU enters Active mode, the interrupt request is delayed for a half of the interrupt frame period (t_{RC}) in order to wait stabilization of the system oscillation (figure 33). In this case, MCU operation is the same as that when canceling Standby mode (figure 31).

Sub-active Mode: In the sub-active mode,

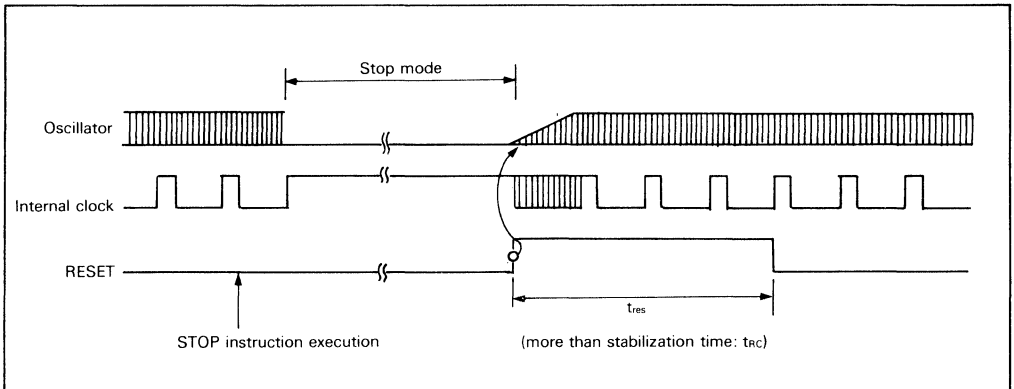


Figure 32. Timing Chart of Recovering from Stop Mode

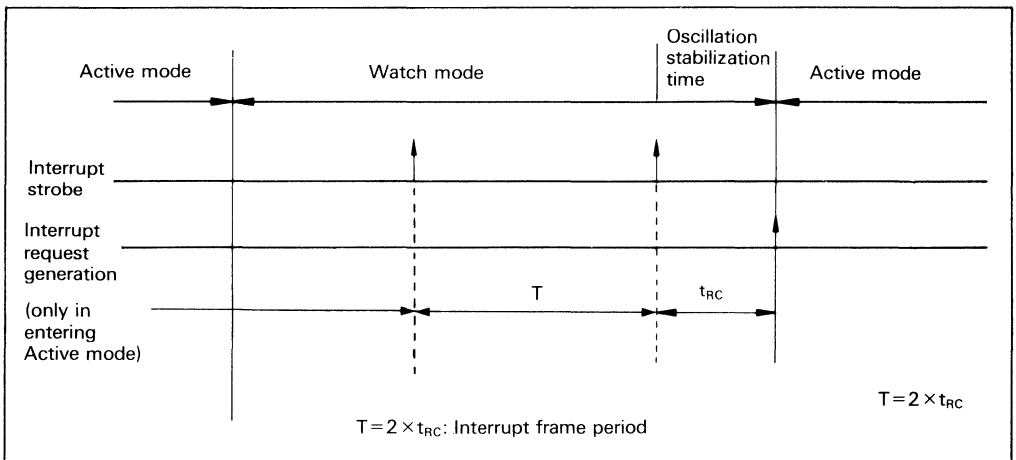


Figure 33. Interrupt Frame

the MCU operates with the clock generated in the oscillator circuit; X1-X2. Timer A/ \overline{INT}_0 interrupt is generated in this mode with the timing synchronous with the interrupt frame timing.

Note that sub-active mode is a functional option. Therefore, sub-active is available for the devices provided with this option.

Interrupt Frame: In Watch mode and Sub-Active mode, the time-base clock (ϕ_{CLK}) is applied to timer A and the \overline{INT}_0 circuit. Prescaler W and timer A operates as the time-base and generate the timing clock for the interrupt frame. The interrupt frame period (T) depends on the state of the miscellaneous register as shown in figure 34.

In Watch mode and Sub Active mode, the

timer A/ \overline{INT}_0 interrupt occurs synchronously with the interrupt strobe timing clock. When the MCU wakes up to Active mode from Watch mode, the interrupt request is delayed for a half of interrupt frame period (t_{RC}). The falling edge of \overline{INT}_0 , which is input regardless of the interrupt frame clock cycle, is equivalent to that synchronous with the interrupt strobe clock just after the falling edge. During oscillation stabilization (t_{RC}) the falling edge of \overline{INT}_0 is not recognized. An overflow and interrupt request in timer A occurs synchronously with the interrupt strobe clock.

Limitation on Use

Please pay attention to the following items.

When MCU goes from watch mode to active

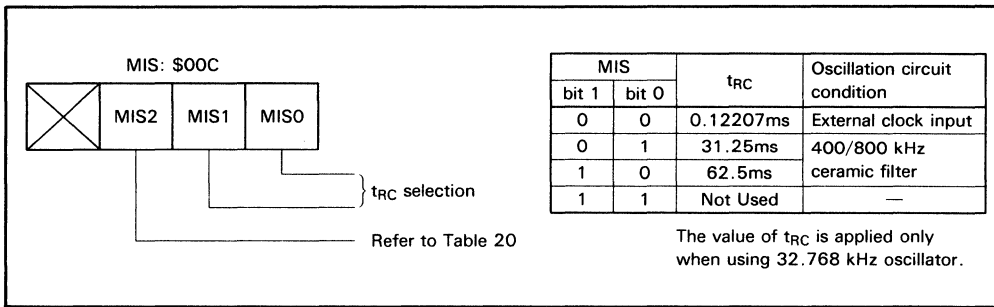


Figure 34. Miscellaneous Register

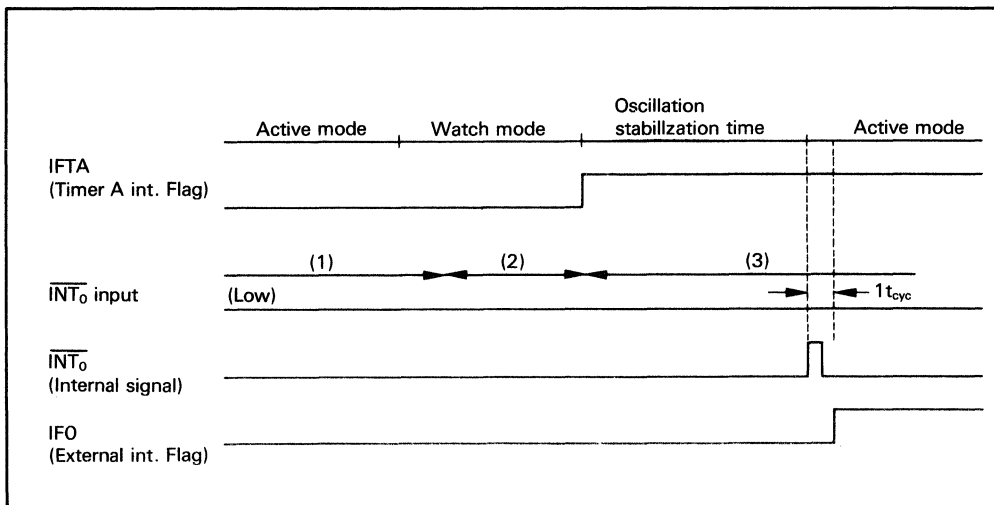


Figure 35. \overline{INT}_0 Detect Timing



mode by timer A interrupt request under the following conditions, the timer A interrupt request flag (IFTA) and also the external interrupt request flag (IF0) will be set.

- (1) MCU goes from active mode to watch mode in \overline{INT}_0 low state.
- (2) \overline{INT}_0 is low state during watch mode.
- (3) MCU goes from watch mode to active mode by timer A interrupt in \overline{INT}_0 low state.

Interrupt flag will be set by falling edge of \overline{INT}_0 input signal and will not be set without this edge in regular case. However the internal \overline{INT}_0 signal is initialized during 1st t_{cyc} after the MCU transition from watch mode to

active mode by timer A interrupt, therefore the falling edge will be generated internally with \overline{INT}_0 low state during this 1st t_{cyc} . This edge will cause to set IF0. (figure 35)

The \overline{INT}_0 input must be high if MCU goes from watch mode to active mode by the timer A interrupt.

MCU Operating Sequence

The MCU operates according to the flow-chart shown in figures 36 to 38.

Note that RESET input is asynchronous. Therefore, the MCU is reset immediately after the RESET input supply.

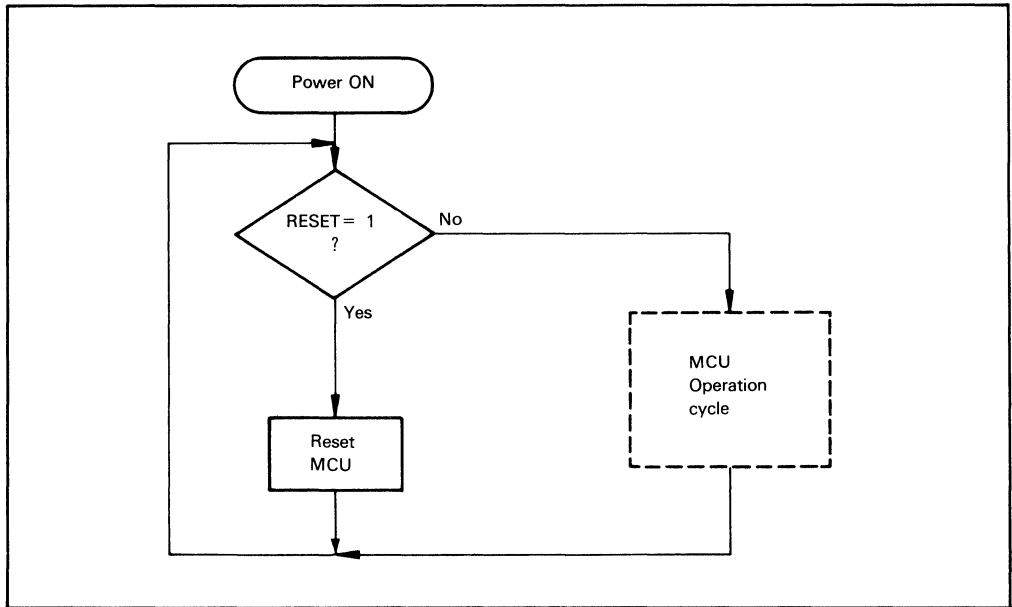


Figure 36. MCU Operating Sequence (Power ON)

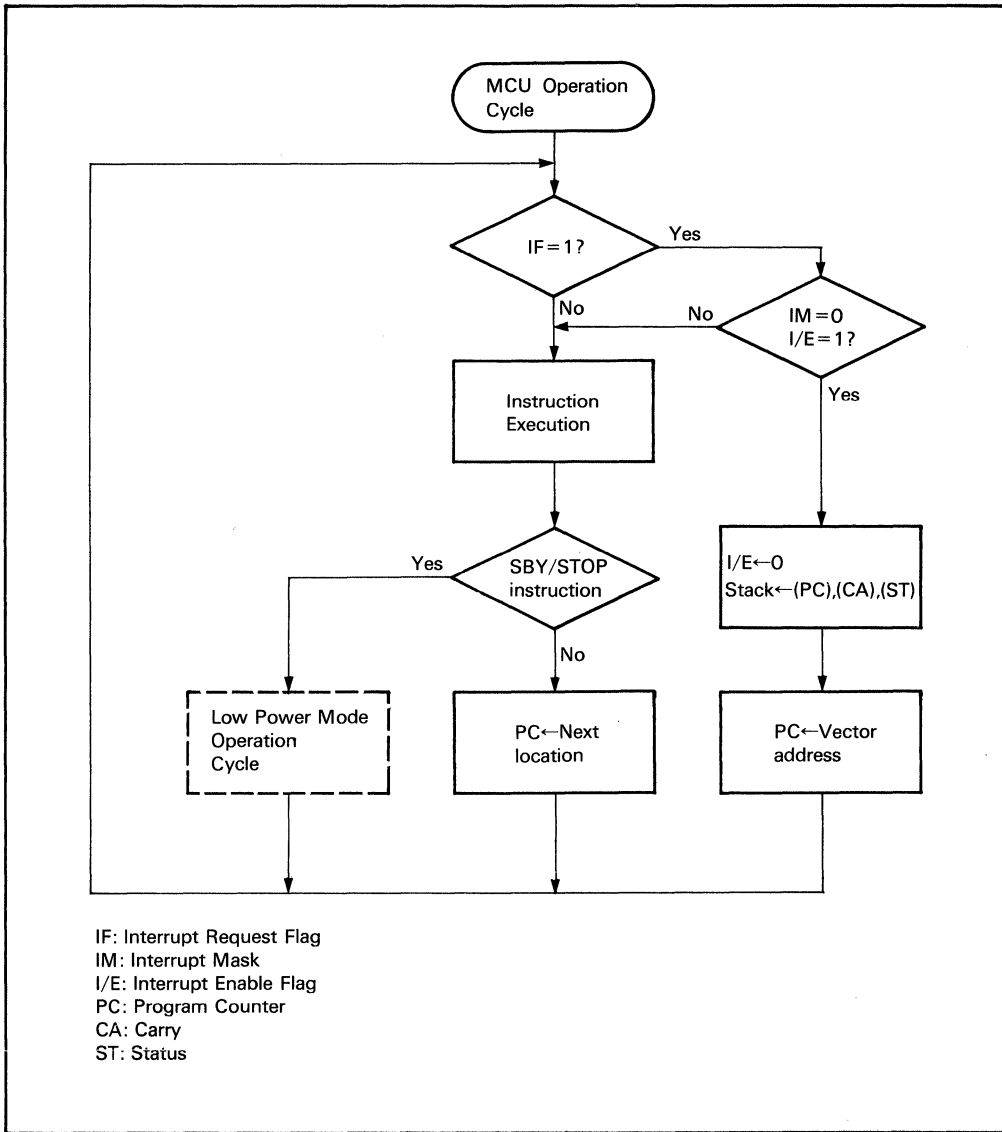


Figure 37. MCU Operating Sequence (MCU Operation Cycle)

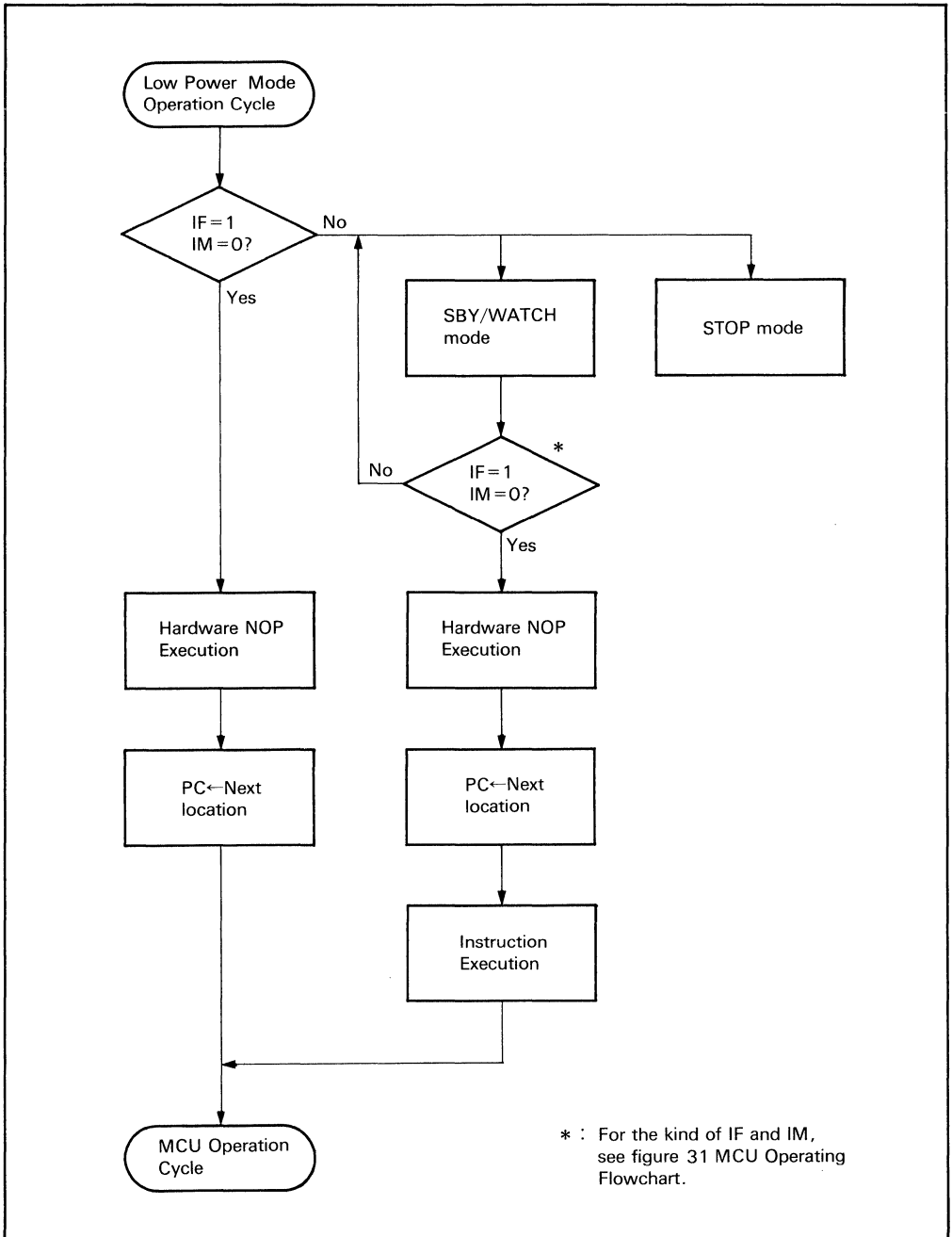


Figure 38. MCU Operating Sequence (Low Power Mode Operation)

HD404608/HD4074608

Pin Description in PROM Mode

The HD4074608 is a ZTAT microcomputer

incorporating PROM. In the PROM mode, the MCU does not operate and the HD4074608 can program the on-chip PROM.

Pin No.		MCU Mode		PROM Mode		Pin No.		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	D ₂	I/O	O ₂	I/O	41	39	SEG9	O		
2	80	D ₃	I/O	O ₃	I/O	42	40	SEG10	O		
3	1	D ₄	I/O	O ₄	I/O	43	41	SEG11	O		
4	2	D ₅	I/O	O ₅	I/O	44	42	SEG12	O		
5	3	D ₆	I/O	O ₆	I/O	45	43	SEG13	O		
6	4	D ₇	I/O	O ₇	I/O	46	44	SEG14	O		
7	5	D ₈	I/O			47	45	SEG15	O		
8	6	D ₉	I/O			48	46	SEG16	O		
9	7	D ₁₀	I	V _{PP}		49	47	SEG17	O		
10	8	D ₁₁ /V _{Cref}	I	A ₉	I	50	48	SEG18	O		
11	9	D ₁₂ /COMPO	I	$\overline{M0}$	I	51	49	SEG19	O		
12	10	D ₁₃ /COMP1	I	$\overline{M1}$	I	52	50	SEG20	O		
13	11	TEST	I	TEST	I	53	51	SEG21	O		
14	12	X1	I	GND		54	52	SEG22	O		
15	13	X2	O			55	53	SEG23	O		
16	14	GND		GND		56	54	SEG24	O		
17	15	R ₀ /SCK	I/O	A ₁	I	57	55	SEG25	O		
18	16	R ₀ /SI	I/O	A ₂	I	58	56	SEG26	O		
19	17	R ₀ /SO	I/O	A ₃	I	59	57	SEG27	O		
20	18	R ₀	I/O	A ₄	I	60	58	SEG28	O		
21	19	R ₁	I/O	A ₅	I	61	59	SEG29	O		
22	20	R ₁	I/O	A ₆	I	62	60	SEG30	O		
23	21	R ₁	I/O	A ₇	I	63	61	SEG31	O		
24	22	R ₁	I/O	A ₈	I	64	62	SEG32	O		
25	23	R ₂	I/O	A ₀	I	65	63	COM1	O		
26	24	R ₂	I/O	A ₁₀	I	66	64	COM2	O		
27	25	R ₂	I/O	A ₁₁	I	67	65	COM3	O		
28	26	R ₂	I/O	A ₁₂	I	68	66	COM4	O		
29	27	R ₃	I/O	A ₁₃	I	69	67	V ₁			
30	28	R ₃ /TIMO	I/O	A ₁₄	I	70	68	V ₂			
31	29	R ₃ /INT ₀	I/O	\overline{CE}	I	71	69	V ₃		V _{CC}	
32	30	R ₃ /INT ₁	I/O	\overline{OE}	I	72	70	TONEC	O		
33	31	SEG1	O			73	71	TONER	O		
34	32	SEG2	O			74	72	V _{Tref}		V _{CC}	
35	33	SEG3	O			75	73	V _{CC}		V _{CC}	
36	34	SEG4	O			76	74	OSC ₁	I	V _{CC}	
37	35	SEG5	O			77	75	OSC ₂	O		
38	36	SEG6	O			78	76	RESET	I	RESET	I
39	37	SEG7	O			79	77	D ₀	I/O	O ₀	I/O
40	38	SEG8	O			80	78	D ₁	I/O	O ₁	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin



V_{PP}
Apply the programming voltage (12.5V ± 0.3V) to V_{PP}.

CE
Program the internal PROM and input the control signal to enable verify.

OE
Input the data output control signal when verify.

A₀-A₁₄
A₀-A₁₄ are address input pins of the internal PROM.

O₀-O₇
O₀-O₇ are data bus I/O pins of the internal PROM.

M₀, M₁
These are for PROM mode specification. To put the MCU into the PROM mode, pull M₀, M₁, and TEST low, and RESET high.

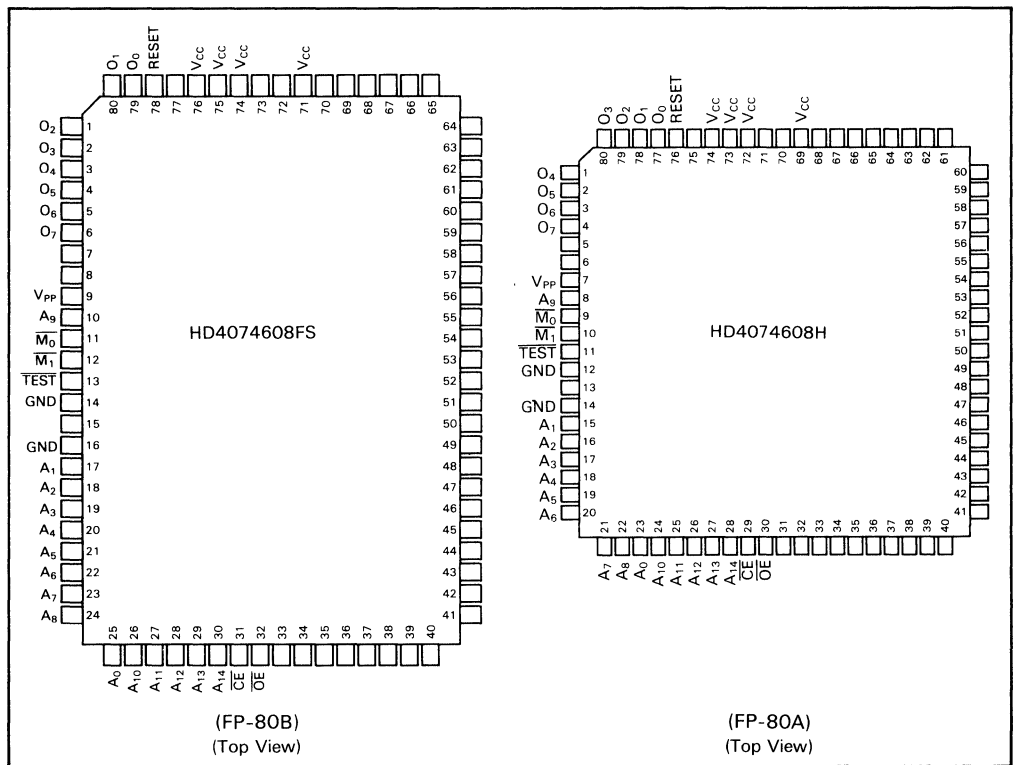


Figure 39. PROM Mode Pin Arrangement

Programmable ROM Operation

The MCU on-chip PROM is programmed in PROM mode (figures 40, 41). PROM mode is set by bringing $\overline{\text{TEST}}$, $\overline{\text{M}_0}$, and $\overline{\text{M}_1}$ low, and RESET high as shown in figure 40. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 80-to-28-pin socket adapter. Table 33 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporate conversion circuit to use a general perpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 41. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 32 shows how programming and verification modes are selected.

Figure 42 is a programming flowchart, and figure 43 is a timing chart. For precautions on PROM programming, refer to ZTAT MCU On-Chip PROM Characteristics and Precautions for Applications.

Precautions

1. Addresses \$0000 to \$3FFF should be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. Data in unused addresses should be set to \$FF.
2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with $V_{PP}=12.5\text{ V}$. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP} .

Table 32. PROM Mode Selection

Mode	Pin			
	CE	OE	V_{PP}	O_0-O_7
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 33. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type name	Maker	Type name	Package Type
DATA I/O	121B	Hitachi	HS460ESF01H	FP-80B
	29B		HS460ESF03H Under Development	FP-80A
AVAL Corp	PKW-1000	Hitachi	HS460ESF01H	FP-80B
			HS460ESF03H Under Development	FP-80A

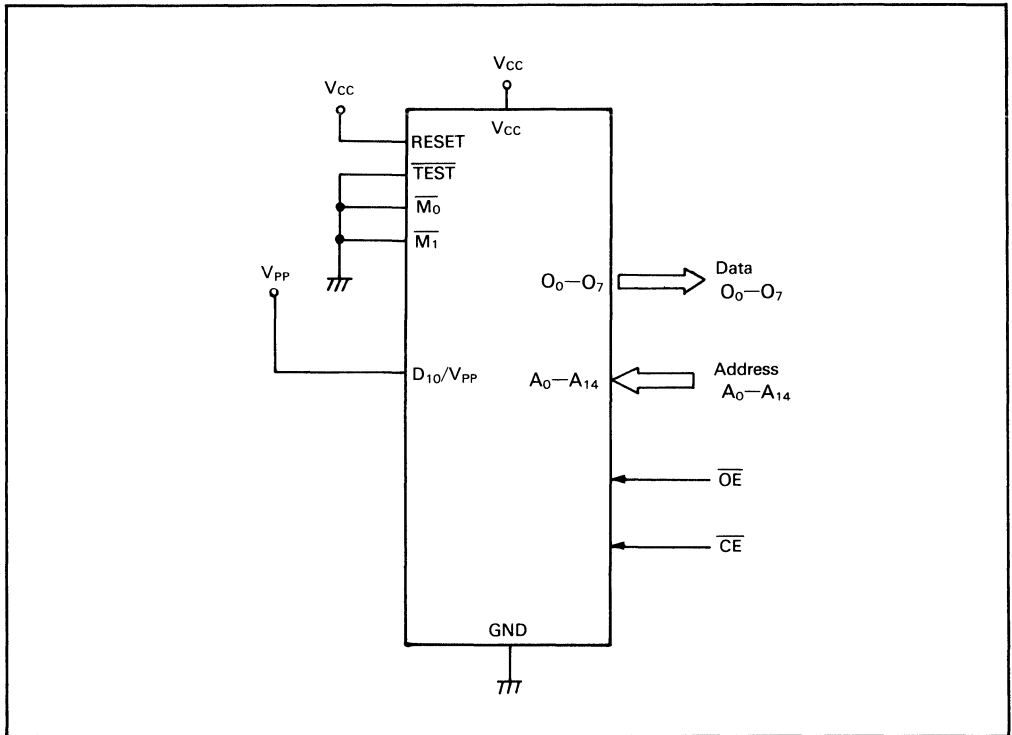


Figure 40. PROM Mode Function Diagram

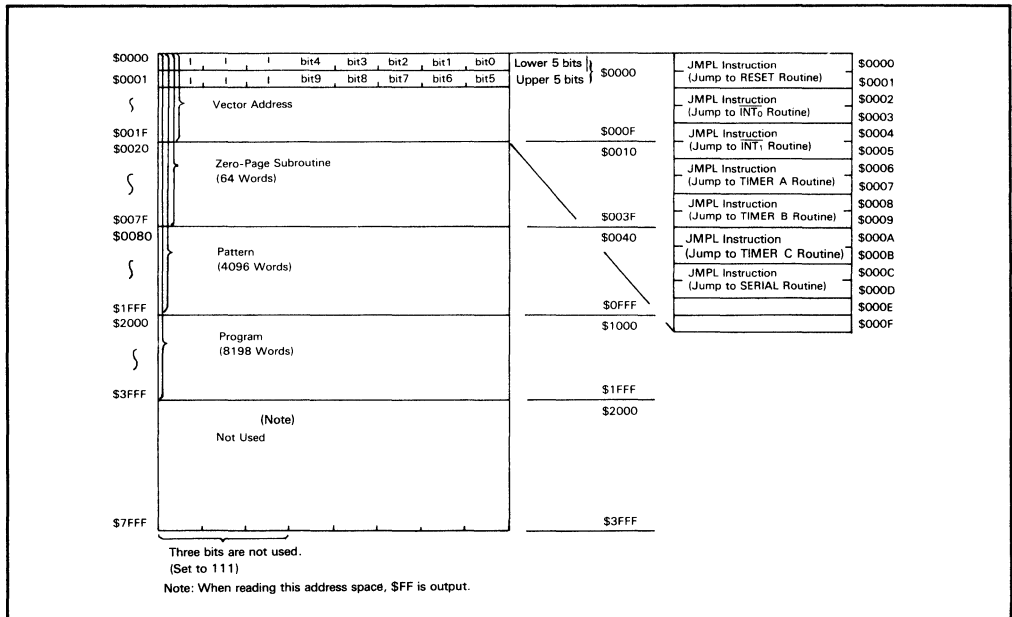


Figure 41. PROM Mode Memory Map



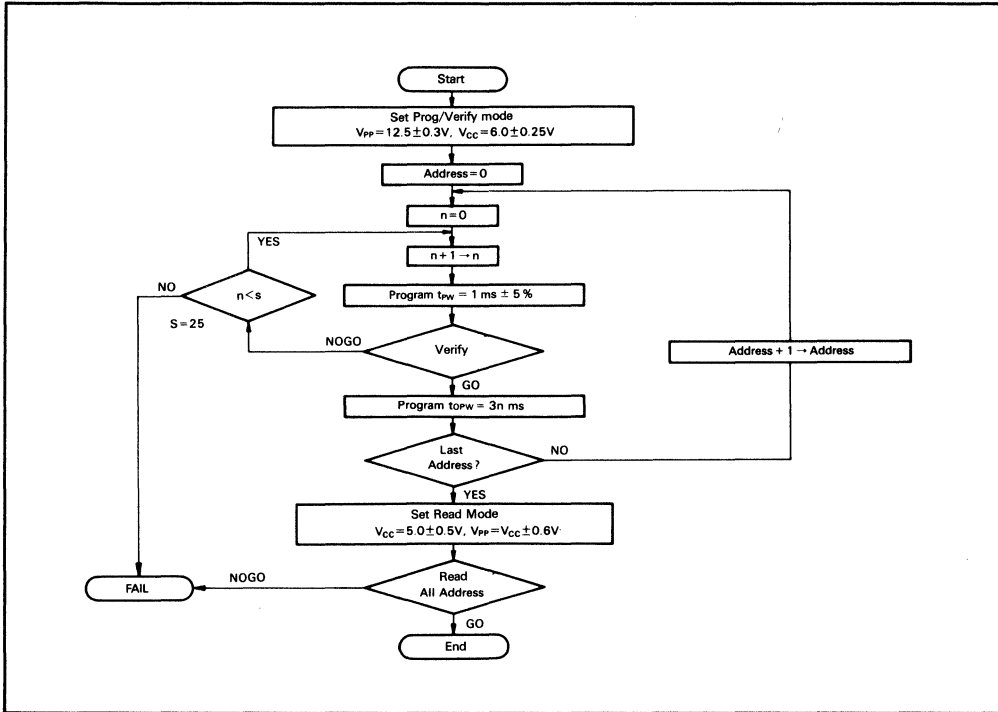


Figure 42. High Speed Programming Flowchart

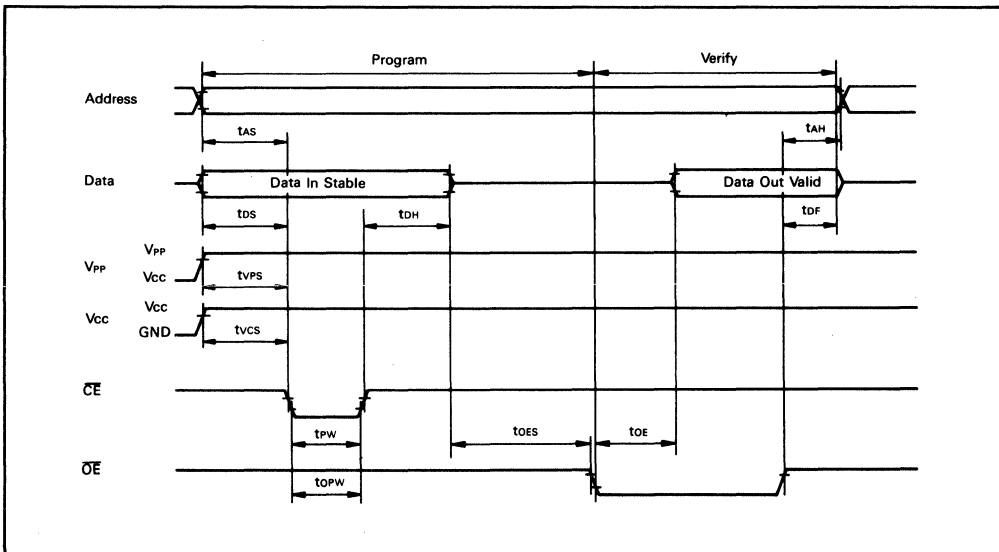


Figure 43. PROM Program/Verify Timing

Programming Electrical Characteristics

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{V}/0.5\text{V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time		t_{AS}	2			μs	Figure 42*
\overline{OE} set-up time		t_{OES}	2			μs	
Data set-up time		t_{DS}	2			μs	
Address hold time		t_{AH}	0			μs	
Data hold time		t_{DH}	2			μs	
Output disable delay time		t_{DF}			130	ns	
V_{PP} set-up time		t_{VPS}	2			μs	
Program pulse width		t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming		t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time		t_{VCS}	2			μs	
Data output delay time		t_{OE}	0		500	ns	

* Input Pulse level 0.8 to 2.2V
 Input rising/falling time $\leq 20\text{ns}$

Timing reference level { input : 1.0V, 2.0V
 output : 0.8V, 2.0V

Precautions on PROM Programming

Principles of PROM Programming/Erasing

The ZTAT microcomputer has the same type of the memory cell as the EPROM. The PROM is programmed by applying high voltage to the control gate and drain and injecting hot electrons into the floating gate, in the same way in the EPROM programming. The electrons in the floating gate remains stabilized, surrounded by the energy barrier of SiO₂ film. By this electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced as over time. This reduction is caused by:

1. Ultraviolet lightThe electrons are discharged by the ultraviolet light (erasure principle)
2. HeatThe electrons, which are excited by heat, are discharged
3. Application of high voltage...The number of electrons is reduced due to the high voltage which is applied to the control gate and drain

If there is any failure in the oxide film, the charge is markedly reduced; however, in general, such reduction does not occur, since devices which failed are usually excluded

during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PP}) and the longer the program pulse width (t_{pw}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a P-N junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise causes a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

1. Confirm that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
2. Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

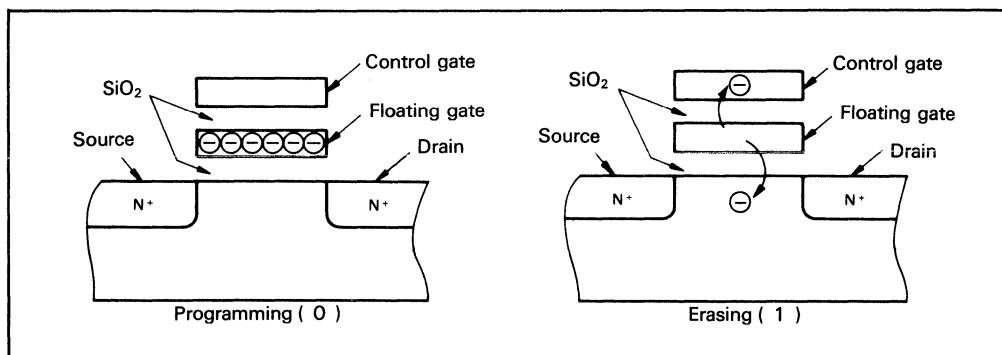


Figure 44. Cross Section of PROM Memory Cell

PROM Reliability after Programming

In general, semiconductor devices retain their reliability, if some initial failures can be rejected. Initial failures can be rejected by adequate screening. "Baking" the device under high-temperature conditions is a screening method which eliminates initial short-time data hold failures in the memory cell (See "Principles of PROM Programming/Eras-

ing"). ZTAT microcomputer devices realize good reliability because they have been subjected to such screening during the water fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 45 shows the recommended screening procedure.

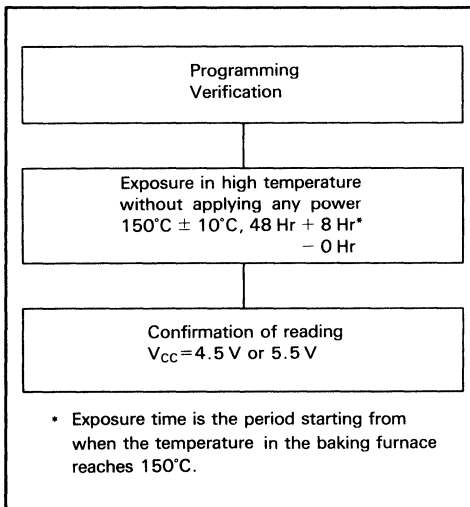


Figure 45. Recommended Screening Procedure

(note) If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

RAM Addressing Mode

As shown in figure 46, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 47.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on page boundary ($256n + 255$) (figure 48), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bit immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 49). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

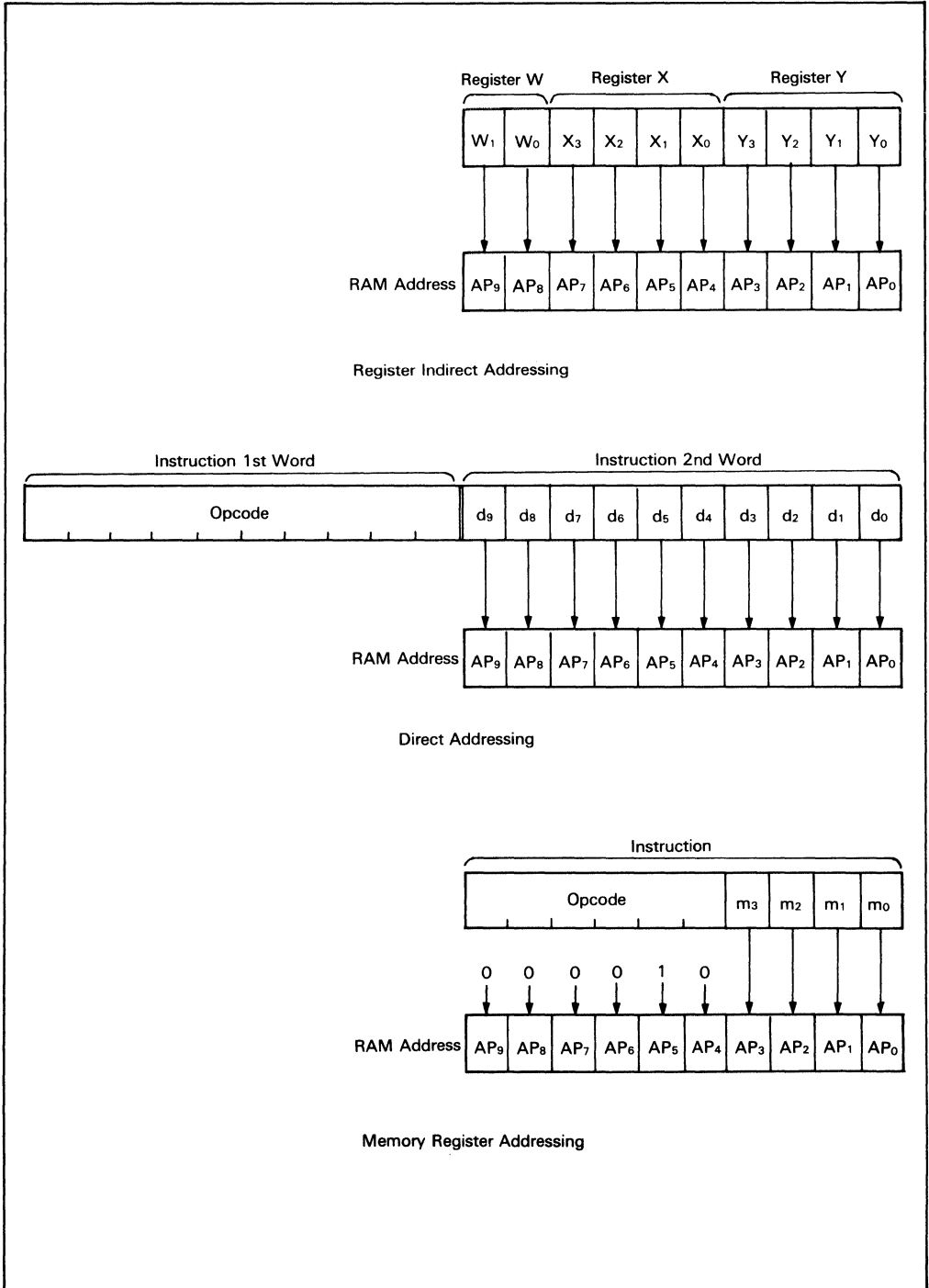


Figure 46. RAM addressing Mode



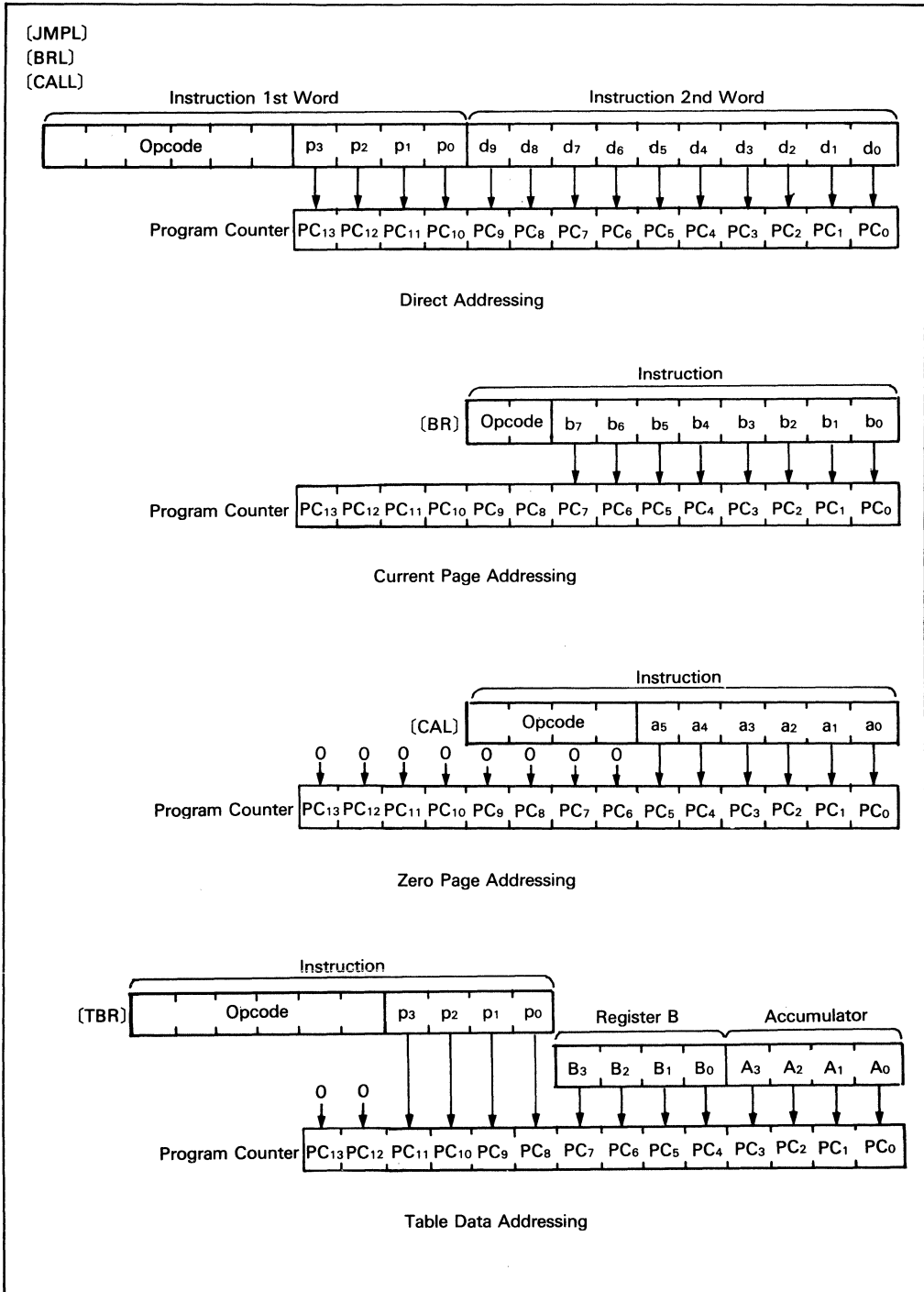


Figure 47. ROM Addressing Mode



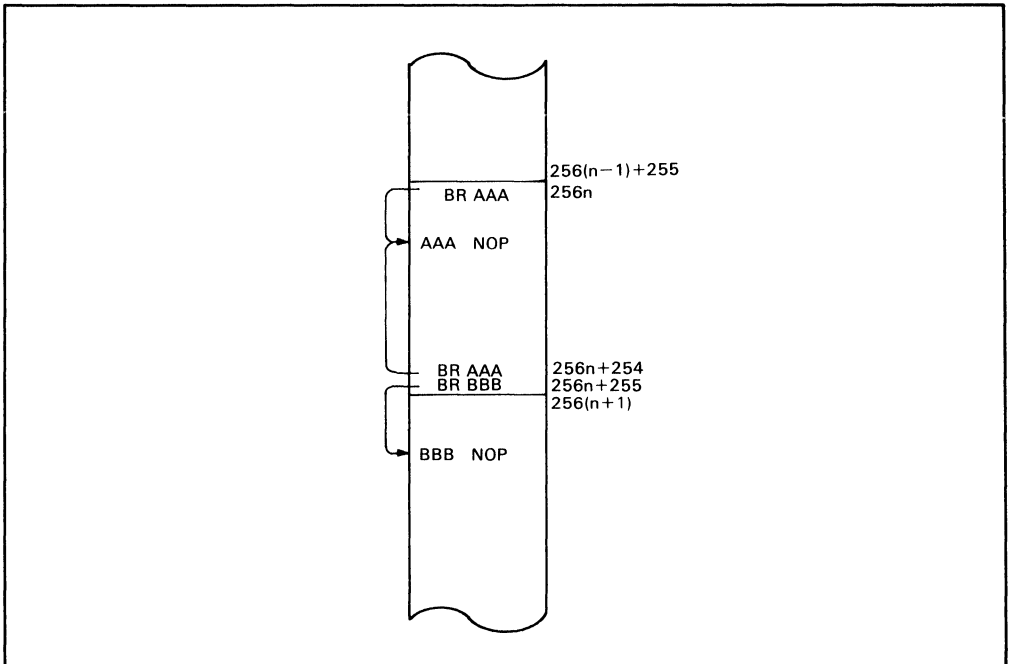


Figure 48. The Branch Destination by BR Instruction on the Boundary between Pages

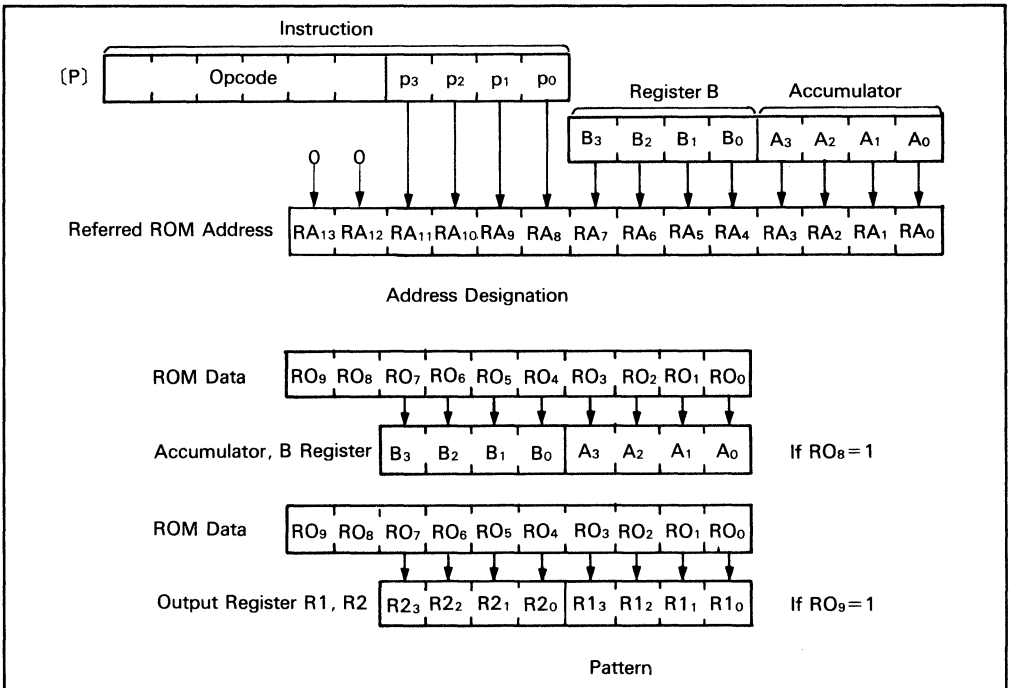


Figure 49. P Instruction

Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 34-43 list their functions, and table 44 is an opcode map.

Table 34. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 35. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 36. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 37. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY (X) is given below).
The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 38. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\overline{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\overline{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A+CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M-A- \overline{CA} → A NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M-A- \overline{CA} → A NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR

Table 39. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 40. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 41. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 42. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 43. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode/Watch Mode*	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/Watch Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

* : Only when shifted from sub-active mode.



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14.0	V	2
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Total Allowance of Input Current	ΣI_O	100	mA	3
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	4
Maximum Input Current	I_O	4	mA	5, 6
		30	mA	5, 7
Maximum Output Current	$-I_O$	4	mA	8, 9
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	-25 to + 80	°C	

- Notes: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. D_{10} (V_{PP}) of the HD4074608.
 3. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 4. Total allowance of output current is the sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 6. R0-R3
 7. D_0 - D_9
 8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 9. D_0 - D_9 , R0-R3.

Electrical Characteristics

DC Characteristics

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, GND = 0 V, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, INT ₀ , INT ₁	$0.9 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.3$		$V_{CC} + 0.3$	V	External clock operation	
		SI	$0.9 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, SCK, INT ₀ , INT ₁	- 0.3		$0.1 V_{CC}$	V		
		OSC ₁	- 0.3	0.3		V	External clock operation	
		SI	- 0.3		$0.1 V_{CC}$	V		
Output High Voltage	V_{OH}	SCK, TIMO SO	$V_{CC} - 1.0$			V	$-I_{OH} = 0.5\text{mA}$	
Output Low Voltage	V_{OL}	SCK, TIMO SO			0.4	V	$I_{OL} = 0.4\text{mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, SCK, INT ₀ , INT ₁ , SI, SO, TIMO, OSC ₁		1		μA	$V_{in} = 0\text{ V to }V_{CC}$	1
Stop Mode Hold Voltage	V_{stop}	V_{CC}	2			V	Without 32kHz oscillator	7
Current Dissipation in Active Mode	I_{CC1}	V_{CC}		400	1000	μA	$V_{CC} = 3\text{ V}$ $f_{osc} = 400\text{kHz}$	2
	I_{CC2}	V_{CC}		500	1500	μA	$V_{CC} = 3\text{ V}$ DTMF: active $f_{osc} = 400\text{kHz}$	3
	I_{CC3}	V_{CC}		1	2	mA	$V_{CC} = 3\text{ V}$ $f_{osc} = 400\text{kHz}$ D ₁₂ , D ₁₃ analog input mode	4
Current Dissipation in Standby Mode	I_{stby}	V_{CC}		200	500	μA	$V_{CC} = 3\text{ V}$ LCD: ON $f_{osc} = 400\text{kHz}$	5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		1	10	μA	$V_{CC} = 3\text{ V}$ Without 32kHz oscillator	
Current Dissipation in Sub-active Mode	I_{sub}	V_{CC}		50	100	μA	$V_{CC} = 3\text{ V}$	
				35	70	μA	LCD: ON	6
Current Dissipation in Watch Mode (1)	I_{wtc1}	V_{CC}		5	15	μA	$V_{CC} = 3\text{ V}$ LCD: OFF	
Current Dissipation in Watch Mode (2)	I_{wtc2}	V_{CC}		15	35	μA	$V_{CC} = 3\text{ V}$ LCD: ON	

- Notes:
1. Excluding output buffer current.
 2. The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state
 - RESET, $\overline{\text{TEST}}$: V_{CC}
 3. The MCU operates and I/O current does not flow.
 - D₁₂, D₁₃ digital input mode
 - DTMF operates (Current flowing from $V_{T_{ref}}$ to the GND is excluded.)
 4. The D₁₂ and D₁₃ pins are analog input mode and I/O current does not flow.
 - $V_{C_{ref}}$ /D₁₁, COMPO/D₁₂, COMP1/D₁₃: GND
 - DTMF does not operate
 5. The timer operates and I/O current does not flow.
 - MCU is in standby mode
 - Input/output is in reset state
 - Serial interface: Stop
 - D₁₂, D₁₃: digital input mode
 - DTMF: stop
 - RESET: GND
 - $\overline{\text{TEST}}$: V_{CC}
 6. Applies to the HD404608.
 7. RAM data retention

HD404608/HD4074608

Input/Output Characteristics for Standard Pin

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₁₀ -D ₁₃ R0-R3	0.7 V_{CC}		$V_{CC}+0.3$		V	
Input Low Voltage	V_{IL}	D ₁₀ -D ₁₃ R0-R3	-0.3		0.3 V_{CC}		V	
Output High Voltage	V_{OH}	R0-R3	$V_{CC}-1.0$			- $I_{OH} = 0.5\text{ mA}$	V	
Pull-up MOS Current	$-I_P$	R0-R3	5	40	90	$V_{CC} = 3\text{ V}$, $V_{in} = 0\text{ V}$	μA	
Output Low Voltage	V_{OL}	R0-R3			0.4	$I_{OL} = 0.4\text{ mA}$	V	
Input/Output Leakage Current	$ I_{IL} $	D ₁₀ R0-R3 D ₁₁ -D ₁₃			20 1	$V_{in} = 0\text{V to }V_{CC}$	μA	2 1
Input High Voltage	V_{IHA}	D ₁₂ , D ₁₃ (Analog Compare mode)	$V_{Cref} + 0.1$				V	
Input Low Voltage	V_{ILA}	D ₁₂ , D ₁₃ (Analog Compare mode)			$V_{Cref} - 0.1$		V	
Analog Input Reference Voltage Scope	V_{Cref}	V_{Cref}	0		$V_{CC}-1.2$		V	

- Notes: 1. Output buffer current is excluded.
2. The maximum value of the HD404608 is 1 μA .

Input/Output Characteristics for High Voltage Pin

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₀ -D ₉	0.7 V_{CC}		$V_{CC}+0.3$		V	
Input Low Voltage	V_{IL}	D ₀ -D ₉	-0.3		0.3 V_{CC}		V	
Output High Voltage	V_{OH}	D ₀ -D ₉	$V_{CC}-1.0$			- $I_{OH} = 0.5\text{ mA}$	V	
Pull-up MOS Current	$-I_P$	D ₀ -D ₉	5	40	90	$V_{CC}=3\text{V}$, $V_{in}=0\text{V}$	μA	
Output Low Voltage	V_{OL}	D ₀ -D ₉			2.0	$I_{OL} = 15\text{ mA}$ $V_{CC}=4.5\text{V to }6\text{V}$	V	
					0.4	$I_{OL} = 0.4\text{ mA}$		
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₉			1	$V_{in} = 0\text{V to }V_{CC}$	μA	1

Note: Output buffer current are excluded.



Liquid Crystal Circuit Characteristics

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment Driver Descending Voltage	V_{ds}	SEG1 – SEG32			0.6	V	$I_d = 3\ \mu\text{A}$	1
Common Driver Descending Voltage	V_{dc}	COM1 – COM4			0.3	V	$I_d = 3\ \mu\text{A}$	1
LCD Power Supply Divide Resistor	R_{well}		100	300	900	$k\Omega$	Between V1 and GND	
LCD Voltage	V_{LCD}	V1			V_{CC}	V		2, 3

- Notes:
1. Descending voltage from the power supply pins V1, V2, V3, and GND to the segment and common pins.
 2. Keep the relation $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$ when V_{LCD} is supplied by external power supply.
 3. $V_{LCD\ min} = 2.7\text{ V}$ (HD404608)
 $V_{LCD\ min} = 3.0\text{ V}$ (HD4074608)

DTMF Characteristics

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
TONE Output Voltage (1)	V_{OR}	TONER	500	660		mVrms	$V_{Tref} - GND = 2.0\text{ V}$, $R_L = 100\text{ k}\Omega$	1
TONE Output Voltage (2)	V_{OC}	TONEC	520	690		mVrms	$V_{Tref} - GND = 2.0\text{ V}$, $R_L = 100\text{ k}\Omega$	1
TONE Output Distortion	$\%_{DIS}$			3	7	%	Short circuit between TONER and TONEC, $R_L = 100\text{ k}\Omega$	2
TONE Output Ratio	d_{BCR}			2.5		dB	Short circuit between TONER and TONEC, $R_L = 100\text{ k}\Omega$	2

- Notes:
1. See figure 50.
 2. See figure 51.

HD404608/HD4074608

AC Characteristics

(HD404608: $V_{CC} = 2.7\text{ V to }6.0\text{ V}$, HD4074608: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	400			kHz	Divided into 4	
			800			kHz		
		X1, X2	32.768			kHz		
Instruction Cycle Time	t_{cyc}		10			μs	$f_{osc} = 400\text{kHz}$	
			5			μs	$f_{osc} = 800\text{kHz}$	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			30	ms	$f_{osc} = 400\text{kHz}$	1
					30	ms	$f_{osc} = 800\text{kHz}$	1
		X1, X2			3	S	$T_a = -10\text{ to }+60^\circ\text{C}$	2
External Clock Frequency	f_{CP}	OSC ₁	400			kHz		
			800			kHz		
External Clock High	t_{CPH}	OSC ₁	1100			ns	$f_{CP} = 400\text{kHz}$	3
			550			ns	$f_{CP} = 800\text{kHz}$	3
External Clock Low	t_{CPL}	OSC ₁	1100			ns	$f_{CP} = 400\text{kHz}$	3
			550			ns	$f_{CP} = 800\text{kHz}$	3
External Clock Rise Time	t_{CPr}	OSC ₁			150	ns	$f_{CP} = 400\text{kHz}$	3
					75	ns	$f_{CP} = 800\text{kHz}$	3
External Clock Fall Time	t_{CPf}	OSC ₁			150	ns	$f_{CP} = 400\text{kHz}$	3
					75	ns	$f_{CP} = 800\text{kHz}$	3
$\overline{\text{INT}}_0$ High Level Width	t_{iOH}	$\overline{\text{INT}}_0$	2			t_{cyc}/t_{SUBcyc}	4, 6	
$\overline{\text{INT}}_0$ Low Level Width	t_{iOL}	$\overline{\text{INT}}_0$	2			t_{cyc}/t_{SUBcyc}	4, 6	
$\overline{\text{INT}}_1$ High Level Width	t_{i1H}	$\overline{\text{INT}}_1$	2			t_{cyc}	4	
$\overline{\text{INT}}_1$ Low Level Width	t_{i1L}	$\overline{\text{INT}}_1$	2			t_{cyc}	4	
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}	5	
Input Capacitance	C_{in}	D ₁₀			90	pF	$f = 1\text{ MHz}, V_{in} = 0\text{V}$	8
		All pins except D ₁₀			15	pF	$f = 1\text{ MHz}, V_{in} = 0\text{V}$	
RESET Fall Time	t_{RSTf}				20	ms		5
Analog Comparator stabilization time	t_{CSTB}	D ₁₂ , D ₁₃ (Analog input mode)			2	t_{cyc}		7



- Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD4074608: V_{CC} is 3.0 V) after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.
 2. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD4074608: V_{CC} is 3.0 V) after power-on. Time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the crystal circuit constant and stray capacitance, please get the manufacturer's advice.
 3. See figure 52.
 4. See figure 53. The unit t_{cyc} is applied when the MCU is in the standby mode or active mode.
 5. See figure 54.
 6. See figure 53. The unit t_{SUBcyc} is applied when the MCU is in the watch mode or sub-active mode. $t_{SUBcyc} = 244.14 \mu s$ (when 32.768 kHz crystal oscillation is used.)
 7. Analog comparator stabilization time is the time until the analog comparator stabilizes and correct data can be read after entering D₁₂/D₁₃ into analog input mode.
 8. The maximum value of the HD404608 is 15 pF.

Serial Interface Timing Characteristics

(HD404608: V_{CC} = 2.7 V to 6.0 V, HD4074608: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise noted)

AT Transfer Clock Output

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t _{cytc}	$\overline{\text{SCK}}$	1			t _{cytc}		1.2
Transfer Clock High, Low Level Width	t _{SCKH} t _{SCKL}	$\overline{\text{SCK}}$	0.5			t _{SCK}		1.2
Transfer Clock Rise, Fall Time	t _{SCKr} t _{SCKf}	$\overline{\text{SCK}}$			200	ns		1.2
Serial Output Data Delay Time	t _{D_{SO}}	SO			500	ns		1.2
Serial Input Data Set-up Time	t _{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t _{HSI}	SI	300			ns		1

AT Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t _{cytc}	$\overline{\text{SCK}}$	1			t _{cytc}		1
Transfer Clock High, Low Level Width	t _{SCKH} t _{SCKL}	$\overline{\text{SCK}}$	0.5			t _{SCK}		1
Transfer Clock Rise, Fall Time	t _{SCKr} t _{SCKf}	$\overline{\text{SCK}}$			200	ns		1
Serial Output Data Delay Time	t _{D_{SO}}	SO			500	ns		1.2
Serial Input Data Set-up Time	t _{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t _{HSI}	SI	300			ns		1
Transfer Clock Completion Detect Time	t _{SCKHD}	$\overline{\text{SCK}}$	1			t _{cytc}		3

- Notes:
1. See figure 55.
 2. See figure 56.
 3. Transfer Clock Completion Detect Timer is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before Transfer Clock Completion Detect Time has passed.

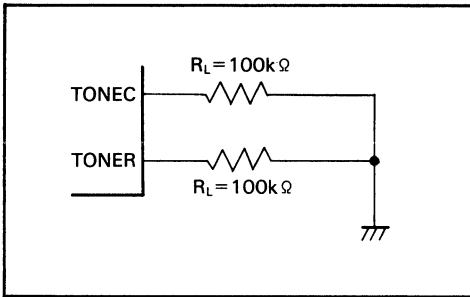


Figure 50. TONE Output Load Circuit

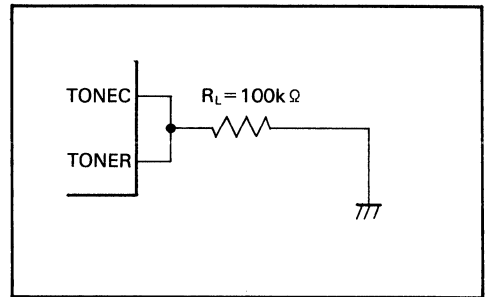


Figure 51. Distortion dB_{CR} Load Circuit

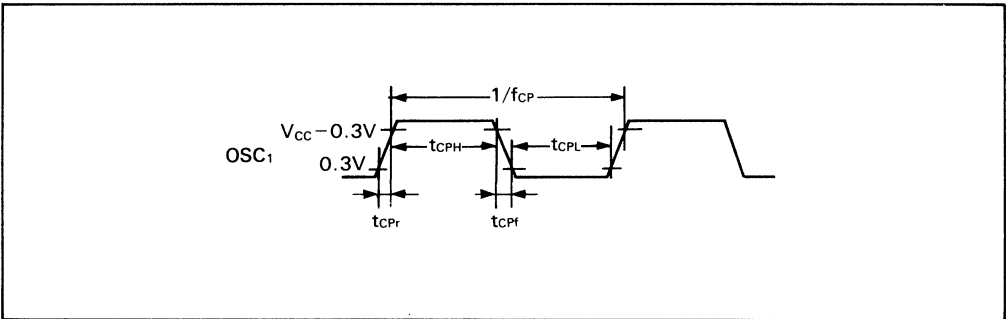


Figure 52. External Clock Timing

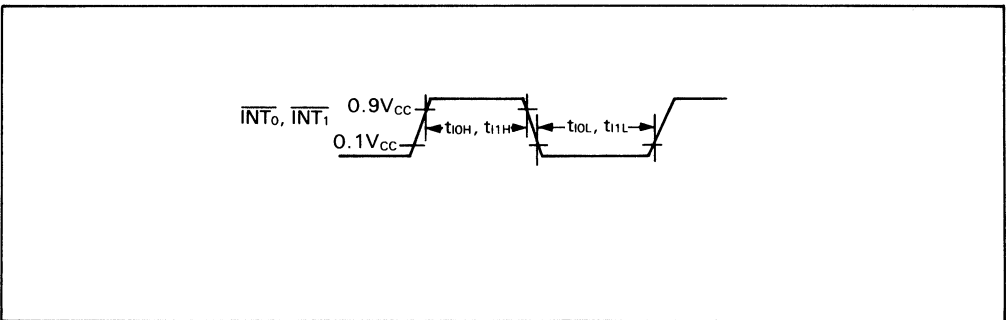


Figure 53. Interrupt Timing

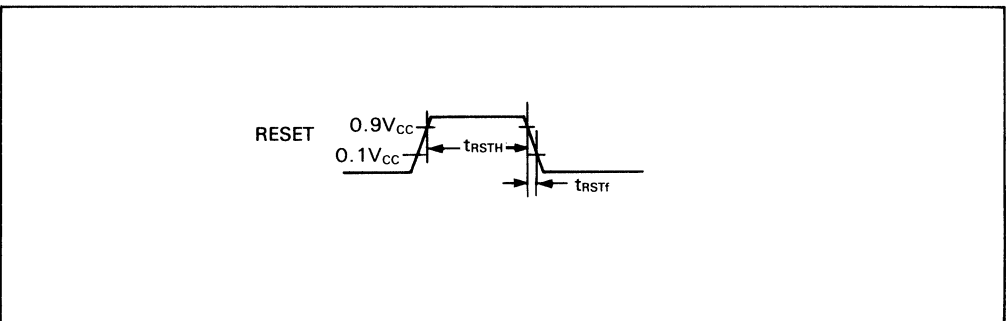


Figure 54. Reset Timing



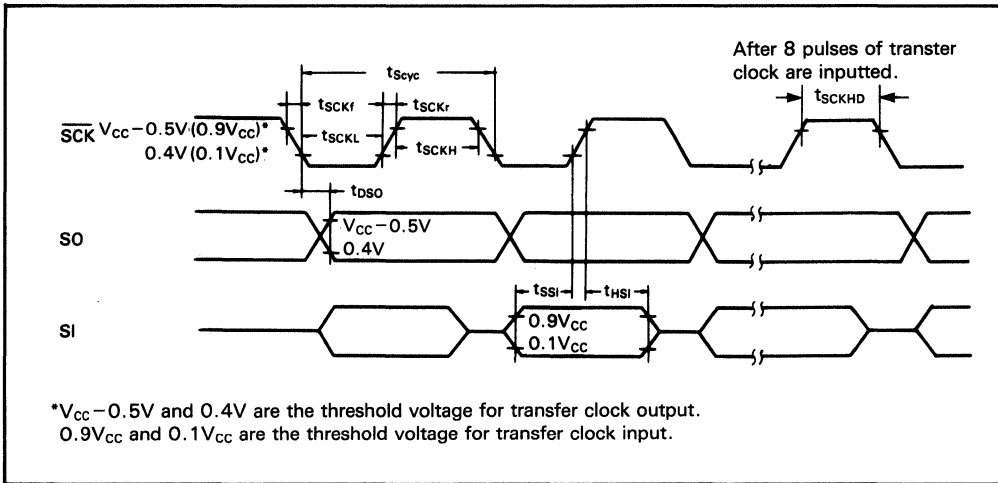


Figure 55. Timing Diagram of Serial Interface

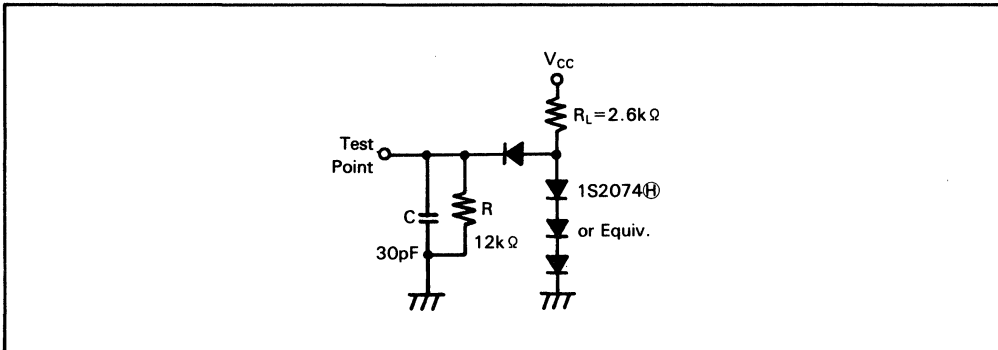


Figure 56. Timing Load Circuit

HD404608 Option List

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number	
Hitachi's Entry	HD404608

Note: Please enter check marks in (■, ×, √).

(1) Functional Option

<input type="checkbox"/> With 32 kHz CPU Operation and With a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and With a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and Without a Watch Time Base

(2) Package

<input type="checkbox"/> FP-80A
<input type="checkbox"/> FP-80B

(3) ROM Code Media

ROM Code Media
<input checked="" type="checkbox"/> EPROM On-Package Microcomputer Type

(4) Oscillator

Main	<input type="checkbox"/> Ceramic Filter Oscillator (f = kHz)
	<input type="checkbox"/> External Clock (f = kHz)
Sub	<input type="checkbox"/> 32.768kHz Crystal Oscillator
	<input type="checkbox"/> Not Used



HD404678

—Under Development—

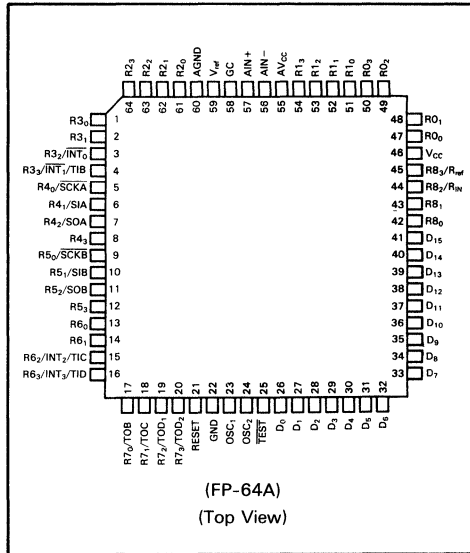
Description

The HD404678 is a 4-bit single-chip HMCS400-series microcomputer for telephone applications which is designed to increase program productivity and incorporates a high-precision dual tone multi-frequency (DTMF) receiver that is especially suitable for answering machines.

Features

- 8192 word \times 10 bit ROM
- 512 digit \times 4 bit RAM
- 48 I/O pins and 4 dedicated input pins
 - 16 large current output pins: Ten 15 mA Sinks (Maximum of 7 pins can be used at the same time) and six 10 mA Sources
- Four timer/counters
 - One 8-bit free-running timer
 - Three 8-bit reload-timer/event-counter/timer-output circuits
- Built-in 2-channel clock synchronous 8-bit serial interface
- Built-in DTMF receiver
- Built-in reset voltage variable function
- 11 interrupt sources
 - External sources: 4
 - Timer/counter: 4
 - Serial interface: 2
 - DTMF receiver: 1
- Subroutine stack: up to 16 levels including interrupts
- Instruction cycle time: 2 μ s
- Two low-power dissipation modes
 - Standby mode
 - Stop mode
- Package
 - 64-pin flat plastic package (FP-64A)

Pin Arrangement



Type of Products

Mask ROM type

Part No.	Clock Frequency (MHz)	Package
HD404678H	4	FP-64A

ZTAT type

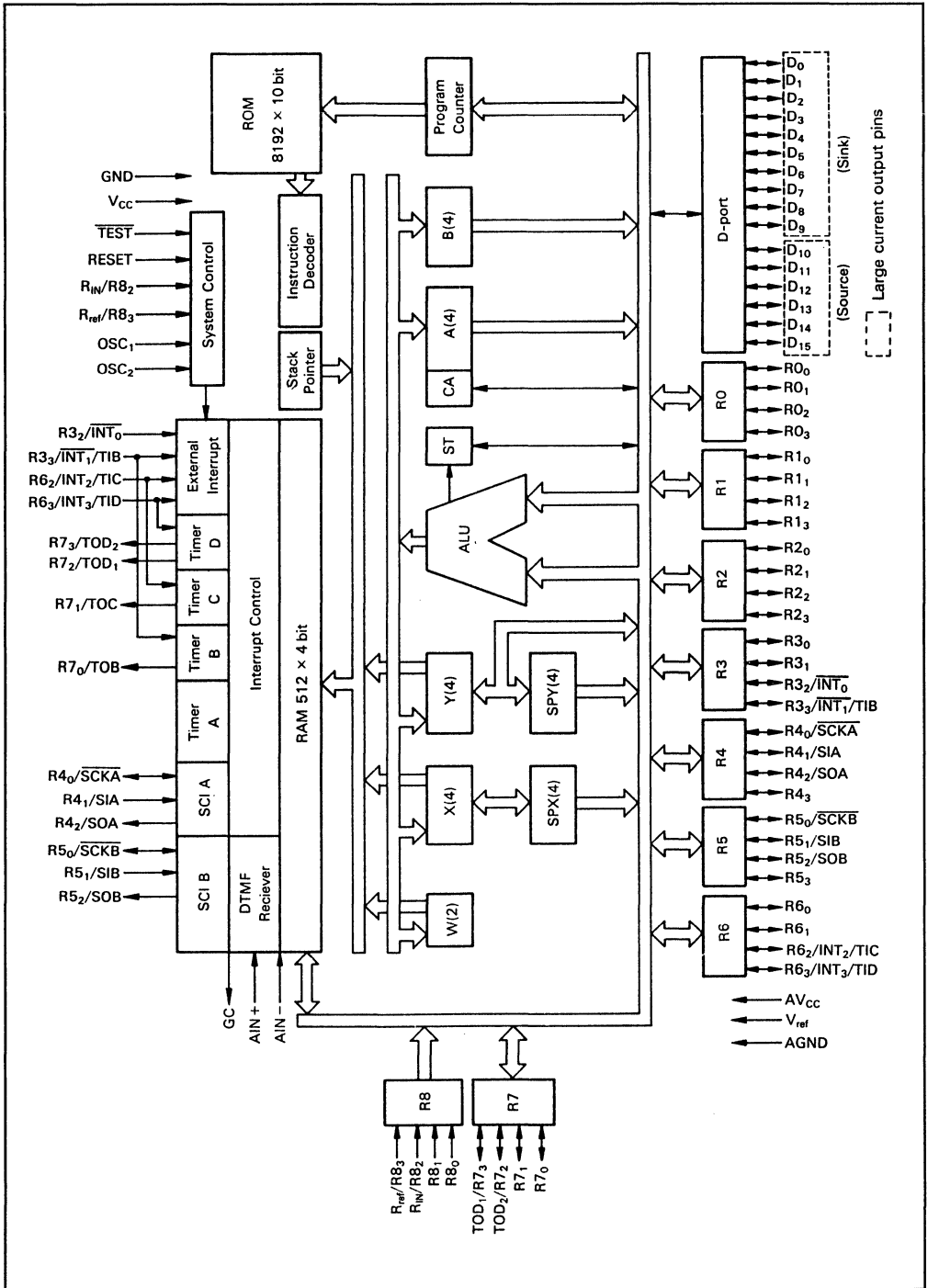
Part No.	Clock Frequency (MHz)	Package
HD4074678H	4	FP-64A

Program Development Support Tools

- Cross assembler and stimulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device



Block Diagram



Pin Description

Function	Symbol	Pin No.	I/O	
Power	V _{cc}	46		Power supply voltage (5 V ± 10%)
	GND	22		Connected to the ground
Test	TEST	25		Used for factory tests Connected to the V _{cc}
Reset	RESET	21	I	Resets the MCU
Oscillator	OSC1, OSC2	23, 24	I	Input pins for the internal oscillator circuit. Connected to the crystal oscillator or external oscillation circuit. External oscillation circuit can be connected to OSC1.
Port	D0–D9	26–35	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current sink pins with pull-up MOS.
	D10–D15	36–41	I/O	Input/output ports. All bits can be accessed separately. Port pins are large current source pins with pull-down MOS.
	R00–R73	1–20, 47–54, 61–64	I/O	Input/output ports accessed with 4-bit-wide nibbles. Pins R00–R53 are standard pins with pull-up MOS while R60–R80 each has a pull-down MOS.
	R80–R83	42–45	I	An input port accessed with 4-bit-wide nibbles. Port pins are standard pins with pull-down MOS.
Interrupt	INT0–INT3	3, 4, 15, 16	I	External interrupts. These pins are multiplexed with R32, R33/TIB, R62/TIC, and R63/TID, respectively.
Serial Communication Interface	SCKA, SCKB	5, 9	I/O	Transfer clock input/output pins for SCIA, SCIB.
	SIA, SIB	6, 10	I	Receive data input pins for SCIA, SCIB.
	SOA, SOB	7, 11	O	Transmit data output pins for SCIA, SCIB.
Timer	TIB, TIC, TID	4, 15, 16	I	External clock input pins for Timers B, C, and D. These pins are multiplexed with R33/INT1, R62/INT2, and R63/INT3, respectively.
	TOB, TOC, TOD1, TOD2	17–20	O	Timer output pins for Timers B, C, and D. These pins are multiplexed with R70, R71, R72, and R73, respectively.
DTMF	AV _{cc}	55		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to set AV _{cc} at the same potential as V _{cc} . Stabilized power supply must be applied.
	AGND	60		Power supply pin for the DTMF receiver analog block. Connect it as close as possible to the power supply to put AGND to the same potential as GND.
	V _{ref}	59		DTMF receiver analog block reference voltage. A stabilized voltage AV _{cc} /2 must be applied.
	AIN+, AIN–	57, 56	I	DTMF signal input pins for the DTMF receiver.
	GC	58	O	DTMF receiver gain control pin.
Reset Voltage Variable Circuit	R _{ref}	45	I	A reference voltage input pin for threshold voltage of the reset voltage variable circuitry. R _{ref} is multiplexed with R83.
	R _{IN}	44	I	An analog input pin of the reset voltage variable circuit. R _{IN} is multiplexed with R82.

Functional Description

ROM Memory Map

The MCU contains an 8192 word × 10 bit ROM area. The ROM memory map is shown in Figure 1 and is explained below.

Vector address area (\$0000-\$000F): Reserved for JMPL instructions that branch to the starting addresses of the reset and interrupt service routines. After the reset or interrupt routine is serviced, the program continues from the vector address.

Zero page subroutine area (\$0000-\$003F): Reserved for subroutines. The program branches to the subrou-

tine in the \$0000-\$003F area, in response to the CAL instruction.

Pattern area (\$0000-\$0FFF): ROM data in locations \$0000 through \$0FFF can be referenced with the P instruction.

Program area (\$0000-\$1FFF): Used for program code.

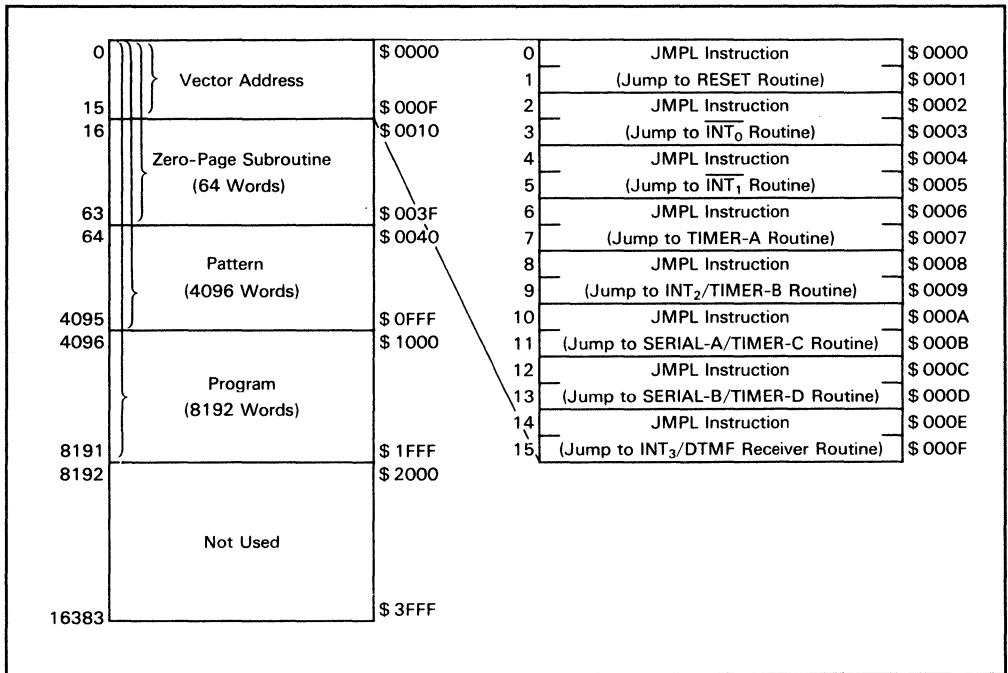


Figure 1. ROM Memory Map

RAM Memory Map

The MCU contains a 512×4 bit RAM area comprised of a data and stack area. In addition, interrupt control bits, special registers, and display data RAM are mapped in the same RAM memory space. The RAM memory map (Figure 2) is described in the following paragraphs.

Interrupt control bit area (\$000-\$003, \$022-\$023): Used for interrupt control (Figure 3). It can be accessed only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special registers are (\$004-\$01B, \$024-\$02C, \$030-\$037, \$03B-\$03E): Mode registers for external interrupt, serial interface, and timer, and data direction and data registers for I/O ports. As shown in Figure 2, these registers can be classified into three types: write-only, read-only, and read/write registers. The registers in special registers area are shown in Table 1. DTMF receiver related registers (\$024-\$02C) are shown in Table 29.

Register flag area (\$020-\$021): Used for the WDON flag which is one bit registers accessed by RAM bit manipulation instructions. This flag can be set by the SEM and SEMD instructions. This flag is shown in Figure 4.

Data area (\$040-\$04F, \$070-\$21F): The memory register (MR), 16 addresses deep (\$040-\$04F), can be accessed by the LAMR and XMRA instructions (Figure 5).

Stack area (\$3C0-\$3FF): Used for saving the contents of the program counter (PC), status (ST), and carry (CA). This area can be used as a 16-nesting-level subroutine stack in which one level requires 4 nibbles. The data to be saved and save conditions are shown in Figure 5. The program counter is restored by the RTN and RTNI instructions. Status and carry are restored by the RTNI instruction only. Any space not used is available data storage.

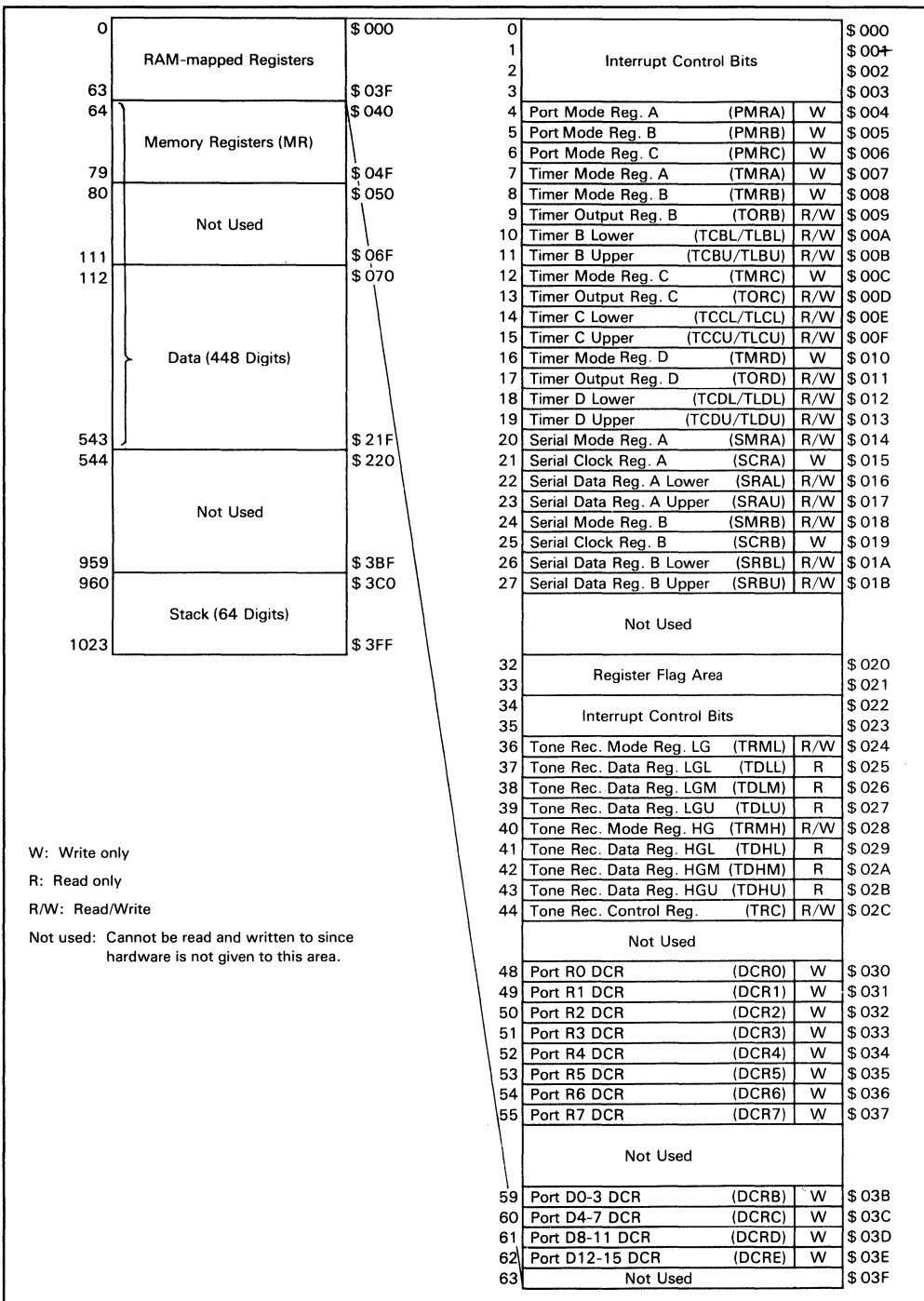


Figure 2. RAM Memory Map



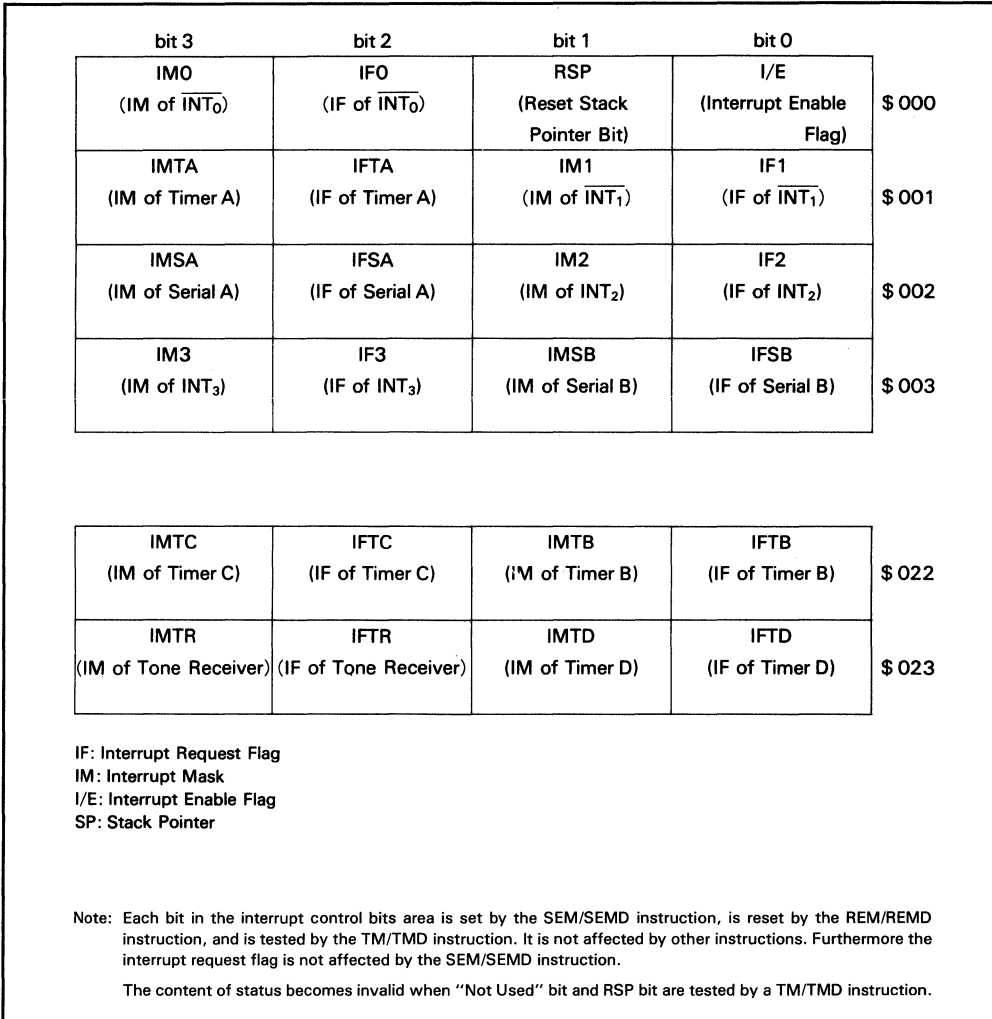


Figure 3. Configuration of Interrupt Control Bits Area

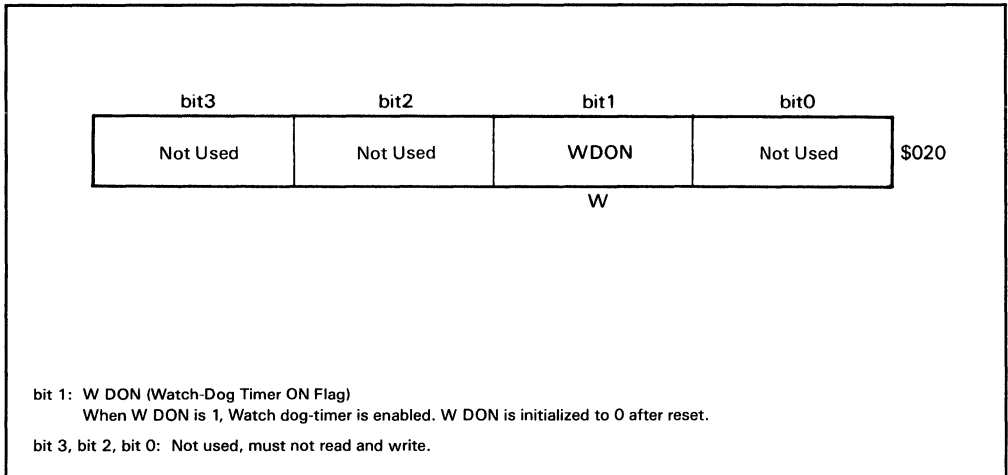


Figure 4. Configuration of Register Flag Area

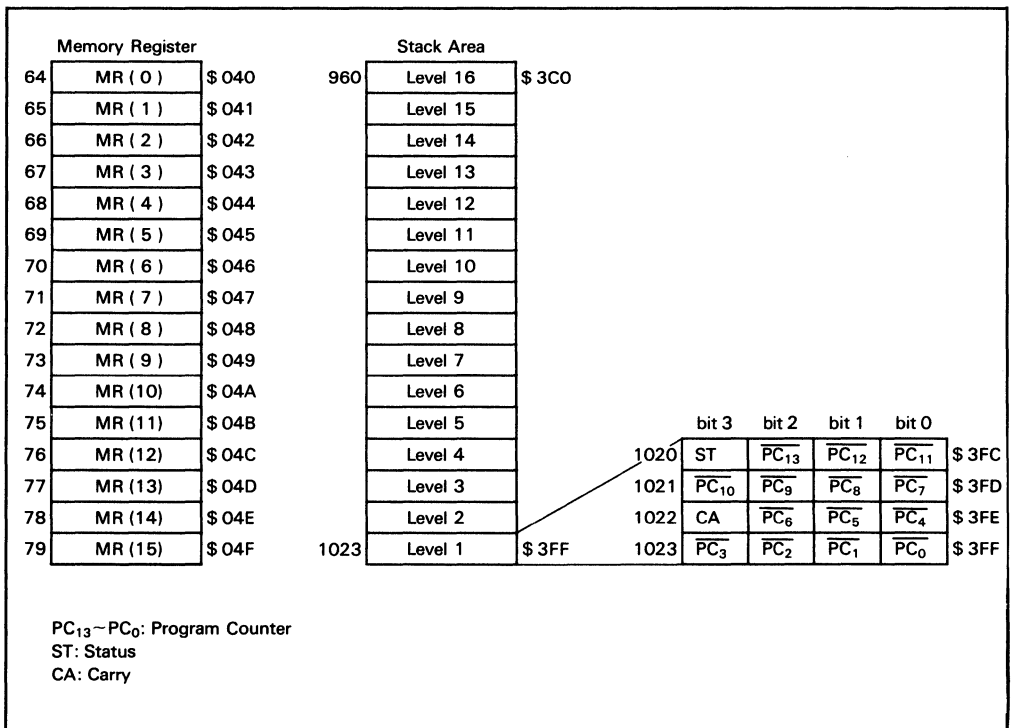


Figure 5. Configuration of Memory Register, Stack Area, and Stack Position

Table 1. Special Registers

Name	Address	Bit	Function
PMRA	\$004	0	Selects R32/INT0 pin mode
		1	Selects R33/INT1 pin mode
		2	Selects R62/INT2 pin mode
		3	Selects R63/INT3 pin mode
PMRB	\$005	0	Selects R42 pin circuit type (CMOS/NMOS open drain)
		1	Selects R52 pin circuit type (CMOS/NMOS open drain)
		2	Selects R82/R _{IN} , R83/R _{ref} pin mode
		3	Disables input fix resistor MOS
PMRC	\$006	0	Selects R70/TOB pin mode
		1	Selects R71/TOC pin mode
		2	Selects R72/TOD 1 pin mode
		3	Selects R73/TOD 2 pin mode
TMRA	\$007	0	Selects Timer A input clock
		1	
		2	
		3	Resets Timer A
TMRB	\$008	0	Selects Timer B input clock
		1	
		2	
		3	Enables auto-reload function
TORB	\$009	0	Selects Timer B output mode
		1	
		2	Selects PWM operation (Pulse Width Modulation)
		3	Not used
TCBL/TLBL	\$00A	0	Low nibble of timer counter/timer load register (Timer B)
		1	
		2	
		3	
TCBU/TLBU	\$00B	0	High nibble of timer counter/timer load register (Timer B)
		1	
		2	
		3	
TMRC	\$00C	0	Selects Timer C input clock
		1	
		2	
		3	Enables auto-reload function
TORC	\$00D	0	Selects Timer C output mode
		1	
		2	Selects PWM operation
		3	Not used
TCCL/TLCL	\$00E	0	Low nibble of timer counter/timer load register (Timer C)
		1	
		2	
		3	
TCCU/TLCU	\$00F	0	High nibble of timer counter/timer load register (Timer C)
		1	
		2	
		3	
TMRD	\$010	0	Selects Timer D input clock
		1	
		2	
		3	Enables auto-reload function



Table 1. Special Registers (Cont'd.)

Name	Address	Bit	Function
TORD	\$011	0	Selects Timer D output mode
		1	
		2	Selects PWM operation
		3	Not used
TCDL/TLDL	\$012	0	Low nibble of timer counter/timer load register (Timer D)
		1	
		2	
		3	
TCDU/TLDU	\$013	0	High nibble of timer counter/timer load register (Timer D)
		1	
		2	
		3	
SMRA	\$014	0	Selects R42/SOA pin mode
		1	Selects R41/SIA pin mode
		2	Selects R40/SCKA pin mode
		3	Enables STS for SCIA
SCRA	\$015	0	Selects transfer clock source (SCIA)
		1	
		2	
		3	
SRAL	\$016	0	SCIA data register low nibble
		1	
		2	
		3	
SRAU	\$017	0	SCIA data register high nibble
		1	
		2	
		3	
SMRB	\$018	0	Selects R52/SOB pin mode
		1	Selects R51/SIB pin mode
		2	Selects R50/SCKB pin mode
		3	Enables STS for SCIB
SCRB	\$019	0	Selects transfer clock source (SCIB)
		1	
		2	
		3	
SRBL	\$01A	0	SCIB data register low nibble
		1	
		2	
		3	
SRBU	\$01B	0	SCIB data register high nibble
		1	
		2	
		3	
DCRO	\$030	0	R0 port data control register
		1	
		2	
		3	
DCR1	\$031	0	R1 port data control register
		1	
		2	
		3	

Table 1. Special Registers (Cont'd.)

Name	Address	Bit	Function
DCR2	§032	0	R2 port data control register
		1	
		2	
		3	
DCR3	§033	0	R3 port data control register
		1	
		2	
		3	
DCR4	§034	0	R4 port data control register
		1	
		2	
		3	
DCR5	§035	0	R5 port data control register
		1	
		2	
		3	
DCR6	§036	0	R6 port data control register
		1	
		2	
		3	
DCR7	§037	0	R7 port data control register
		1	
		2	
		3	
DCRB	§03B	0	D0–D3 port data control register
		1	
		2	
		3	
DCRC	§03C	0	D4–D7 port data control register
		1	
		2	
		3	
DCRD	§03D	0	D8–D11 port data control register
		1	
		2	
		3	
DCRE	§03E	0	D12–D15 port data control register
		1	
		2	
		3	

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are illustrated in Figure 6 and described in the following paragraphs.

Accumulator (A), B register (B): The 4-bit register accumulator and B register are used to hold the results from the arithmetic logic unit (ALU) and to transfer data to/from memories, I/O, and other registers.

W register (W), X register (X), Y register (Y): W register is a 2-bit, and X and Y registers are 4-bit registers used for indirect RAM addressing. Y register is also used for D-port addressing.

SPX register (SPX), SPY register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry (CA): Stores ALU overflow generated by the arithmetic operation. It is affected by the SEC, REC, ROTL, and ROTR instructions. Carry is pushed onto the stack during interrupt servicing, and popped from the stack by the RTNI instruction, but not by the RTN instruction.

Status (ST): Latches ALU overflow generated by the arithmetic and compare instructions, Not Zero from

the ALU, and results of bit tests. It is a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of the status remain unchanged until the next arithmetic, compare, or bit test instruction is executed. ST becomes 1 after the BR, BRL, CAL, or CALL instruction is executed regardless if it is executed or skipped. The contents of the status are pushed onto the stack during interrupt servicing, and popped from the stack by the RTNI instruction, but not only by the RTN instruction.

Program counter (PC): The 14-bit program counter points to the address of the instruction being executed.

Stack pointer (SP): The 10-bit stack pointer contains the address of the stack area. SP is initialized to \$3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the high nibble of SP are set to "1111", the stack can be used for up to 16 levels. SP is initialized to \$3FF in two ways: MCU reset and RSP bit reset with the REM or REMD instruction.

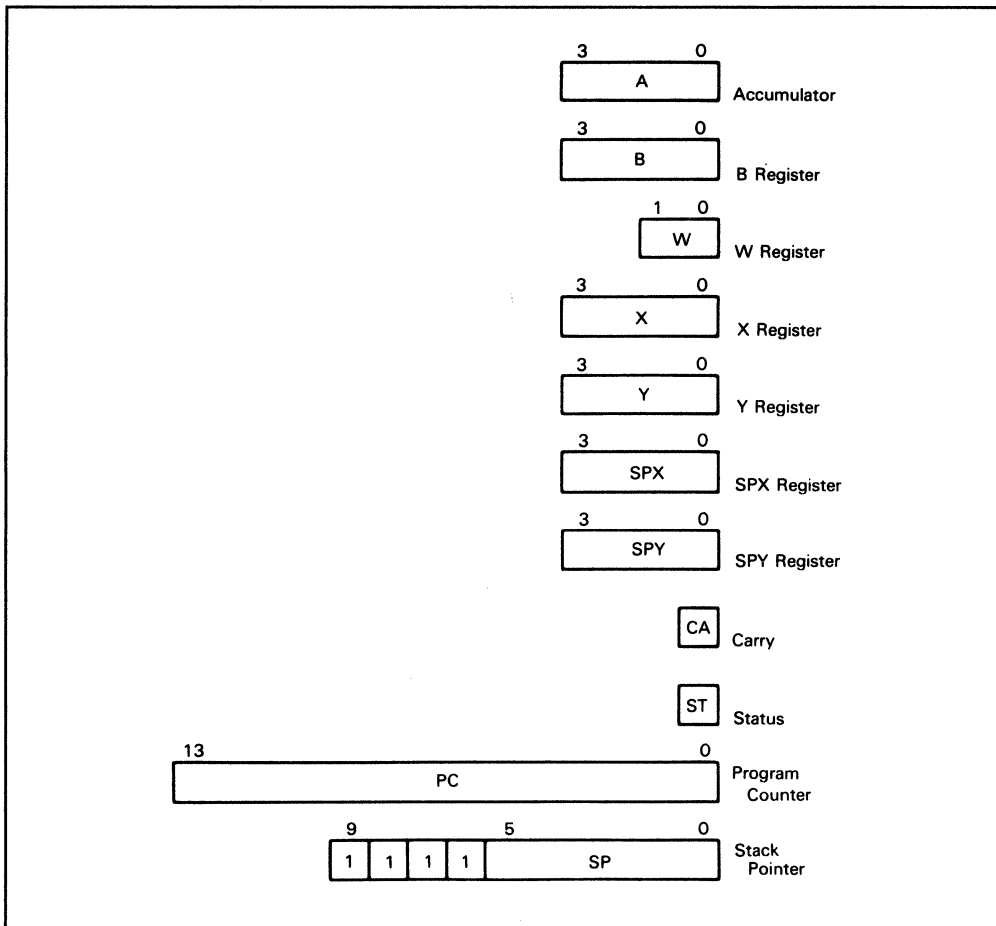


Figure 6. Registers and Flags

Reset

The MCU is reset at the rising edge of the reset signal. This signal should be asserted high for at least t_{RC} to stabilize oscillation at power-on and when cancelling stop mode. In all other cases, reset input signal must be asserted high for at least three instruction cycles to reset the MCU.

From power-on to the beginning of normal oscillation, the MCU and I/O are undefined since reset input is not latched.

Values initialized by MCU reset are shown in Table 2.

Table 2. Initial Values after MCU Reset

Registers		Initial Value	Description	
Program Counter (PC)		\$0000	The program is executed from ROM start address.	
Status (ST)		"1"	The program performs conditional branch	
Stack Pointer (SP)		\$3FF	The stack level becomes 0	
I/O Pin Output Registers	With pull-up MOS ports R00–R53, DO–D9 (PDR)	"1"	Pulled up with input state	
	With pull-down MOS ports R60–R83, D10–D15 (PDR)	"0"	Pulled down with input state. (R8 port is a dedicated input port.)	
	Port Mode Registers A, C (PMRA, PMRC)	"0000"	See port mode registers A, C section	
	Port Mode Register B (PMRB)	"0000"	See port mode register B section	
	Data Control Registers (DCRO–7, DCRB–D)	"0000"	See data control register section	
Interrupt Flag	Interrupt Enable Flag (I/E)	"0"	All interrupts are disabled	
	Interrupt Request Flag (IF)	"0"	No interrupt request occurs	
	Interrupt Mask (IM)	"1"	Interrupt request is masked	
Mode Registers	Serial Mode Registers A, B, (SMRA, SMRB)	"0000"	See serial mode register section	
	Serial Clock Registers A, B (SCRA, SCRB)	"000"	See serial clock register section	
	Timer Mode Registers B–D (TMRB–TMRD)	"0000"	See timer mode registers B–D section	
	Timer Output Registers B–D (TORB–TORD)	"0000"	See timer output registers B–D section	
	Timer Mode Register A (TMRA)	"0000"	See timer mode register A section	
Timer/Counter Serial Interface	Prescaler	\$000	Reset	
	Timer/Event Counters B–D (TCB–TCD)	\$00	Reset	
	Timer Counter A (TCA)	\$00	Reset	
	Timer Load Registers B–D (TLRB–TLRD)	\$00	Reset	
	Octal Counter	"000"	Reset	
DTMF Receiver	Tone Receiver Control Register (TRC)	"000"	Reset	
	Low-group	Tone Receiver Mode Register (TRML)	\$0	Reset
		Tone Receiver Data Registers (TDLL, TDLM, TDLU)	\$000	Reset
	High-group	Tone Receiver Mode Register (TRMH)	\$0	Reset
		Tone Receiver Data Registers (TDHL, TDHM, TDHU)	\$000	Reset

Registers and flags except above become as follows after MCU reset.



Interrupt

Eleven interrupt sources are available on the MCU: four external requests (INT0, INT1, INT2, INT3) and seven internal requests (Timer A, Timer B, Timer C, Timer D, Serial A, Serial B, DTMFR). For each source, an interrupt request flag (IF) and an interrupt mask (IM) are provided to control and maintain the interrupt requests. To control total interrupt operations, the interrupt enable flag (I/E) is provided.

Since the vector addresses are shared between Timer B and INT2, between Serial A and Timer C, between Serial B and Timer D, and between INT3 and DTMFR, determining which request occurs must be done by software. Interrupt function table is shown in Table 3.

Interrupt control bits and interrupt processing: The interrupt control bits are mapped to addresses \$000 through \$003, and \$022 through \$023 of RAM space and are accessed by the RAM bit manipulation instruction. However, interrupt request flag (IF) cannot be set by software. The interrupt enable flag (I/E) and interrupt request flag (IF) are set to "0" and the interrupt mask (IM) is set to "1" by MCU reset.

An interrupt control circuit block diagram is shown in Figure 7. Interrupt priority and vector addresses are shown in Table 4, and conditions of interrupt processing is shown in Table 5. When interrupt request flag is "1" and interrupt mask is "0", an interrupt request is generated. If the interrupt enable flag is "1" at that time, interrupt processing activates. Then a vector address corresponding to the interrupt request is generated from priority PLA.

An interrupt processing sequence and flowchart are shown in Figure 8 and Figure 9, respectively. When an interrupt is received, the current instruction execution finishes at the first cycle, then the contents of the carry, status, and program counter are pushed onto the stack in the second and third cycles, and the program jumps to the vector address area to restart instruction execution in the third cycle. For each vector address area, the JMPL instruction must be programmed to branch the starting address of interrupt routine. The interrupt request flag which causes processing must be reset by software.

Table 2A.

Item	After recovering from STOP mode by MCU reset	After all other MCU reset
Carry (CA)	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.
Accumulator (A)		
B Register (B)		
W Register (W)		
X/SPX Register (X/SPX)		
Y/SPY Register (Y/SPY)		
Serial Data Registers A, B (SRA, SRB)		
RAM	The contents of RAM just before MCU reset (just before STOP instruction) are retained.	

Table 3. Interrupt Function Table

Interrupt Source	Interrupt Generation	Priority	Interrupt Vector Address	Interrupt Control Bit Address					
				Interrupt Request Flag			Interrupt Mask		
				Symbol	Address	Bit	Symbol	Address	Bit
RESET	RESET pin = "H" Variable voltage reset mode ($R_{IN} > R_{ref}$) Timer A (WDT) overflow	Note	\$0000						
INT0	INT0 pin falling edge detection	1	\$0002	IF0	\$000	2	IM0	\$000	3
INT1	INT1 pin falling edge detection	2	\$0004	IF1	\$001	0	IM1	\$001	1
Timer A	Timer A overflow	3	\$0006	IFTA	\$001	2	IMTA	\$001	3
INT2/Timer B	INT2 pin rising edge detection	4	\$0008	IF2	\$002	0	IM2	\$002	1
	Timer B overflow			IFTB	\$022	0	IMTB	\$022	1
Serial A/Timer C	Serial A transmit end Serial A transmit suspended	5	\$000A	IFSA	\$002	2	IMSA	\$002	3
	Timer D overflow			IFTC	\$022	2	IMTC	\$022	3
Serial B/Timer D	Serial B transmit end Serial B transmit suspended	6	\$000C	IFSB	\$003	0	IMSB	\$003	1
	Timer D overflow			IFTD	\$023	0	IMTD	\$023	1
INT3/DTMFR	INT3 pin rising edge detection	7	\$000E	IF3	\$003	2	IM3	\$003	3
	DTMF signal cycle measurement end			IFTR	\$023	2	IMTR	\$023	3

Note: Highest priority

- High input to the RESET pin
- Reset by watchdog timer mode
- Reset by variable voltage reset mode

Table 4. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector Addresses
RESET		\$0000
INT0	1	\$0002
INT1	2	\$0004
Timer A	3	\$0006
INT2/Timer B	4	\$0008
Serial A/Timer C	5	\$000A
Serial B/Timer D	6	\$000C
INT3/DTMFR	7	\$000E

Table 5. Conditions of Interrupt Processing

Interrupt Source Interrupt Control Bit	INT ₀		INT ₁	TimerA	INT ₂ / TimerB		SerialA/ TimerC		SerialB/ TimerD		INT ₃ / DTMFR	
	INT ₀	INT ₀	INT ₁	TimerA	INT ₂ / TimerB	INT ₂ / TimerB	SerialA/ TimerC	SerialA/ TimerC	SerialB/ TimerD	SerialB/ TimerD	INT ₃ / DTMFR	INT ₃ / DTMFR
I/E	1	1	1	1	1	1	1	1	1	1	1	1
IF0 · IM0	1	0	0	0	0	0	0	0	0	0	0	0
IF1 · IM1	*	1	0	0	0	0	0	0	0	0	0	0
IFTA · IMTA	*	*	1	0	0	0	0	0	0	0	0	0
IF2 · IM2	*	*	*	*	1	*	0	0	0	0	0	0
IFTB · IMTB	*	*	*	*	*	1	0	0	0	0	0	0
IFSA · IMSA	*	*	*	*	*	*	1	*	0	0	0	0
IFTC · IMTC	*	*	*	*	*	*	*	1	0	0	0	0
IFSB · IMSB	*	*	*	*	*	*	*	*	1	*	0	0
IFTD · IMTD	*	*	*	*	*	*	*	*	*	1	0	0
IF3 · IM3	*	*	*	*	*	*	*	*	*	*	1	*
IFTR · IMTR	*	*	*	*	*	*	*	*	*	*	*	1

*Don't Care.

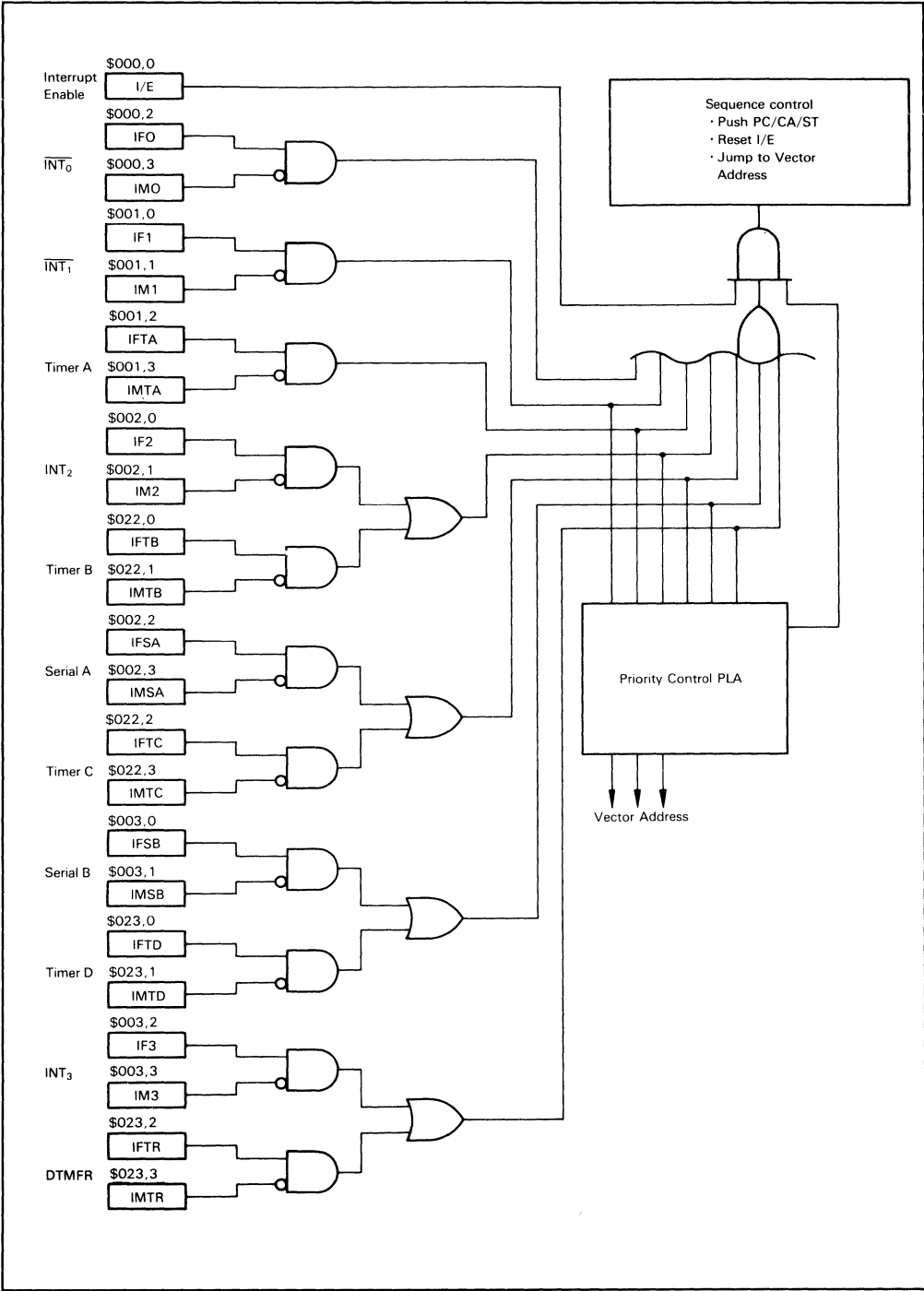


Figure 7. Interrupt Control Circuit Block Diagram



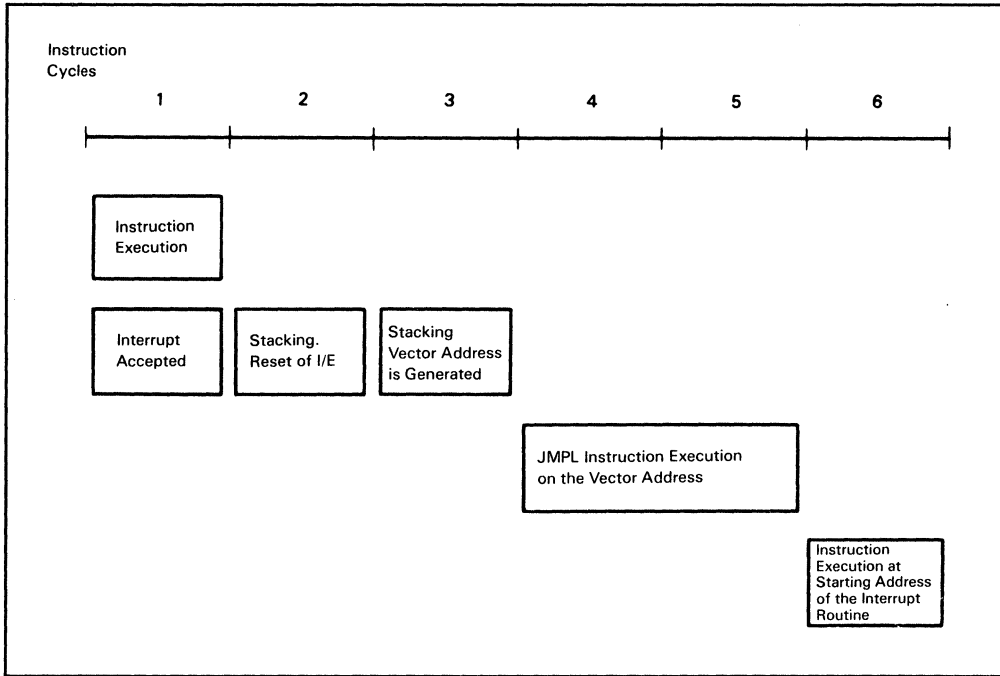


Figure 8. Interrupt Servicing Sequence

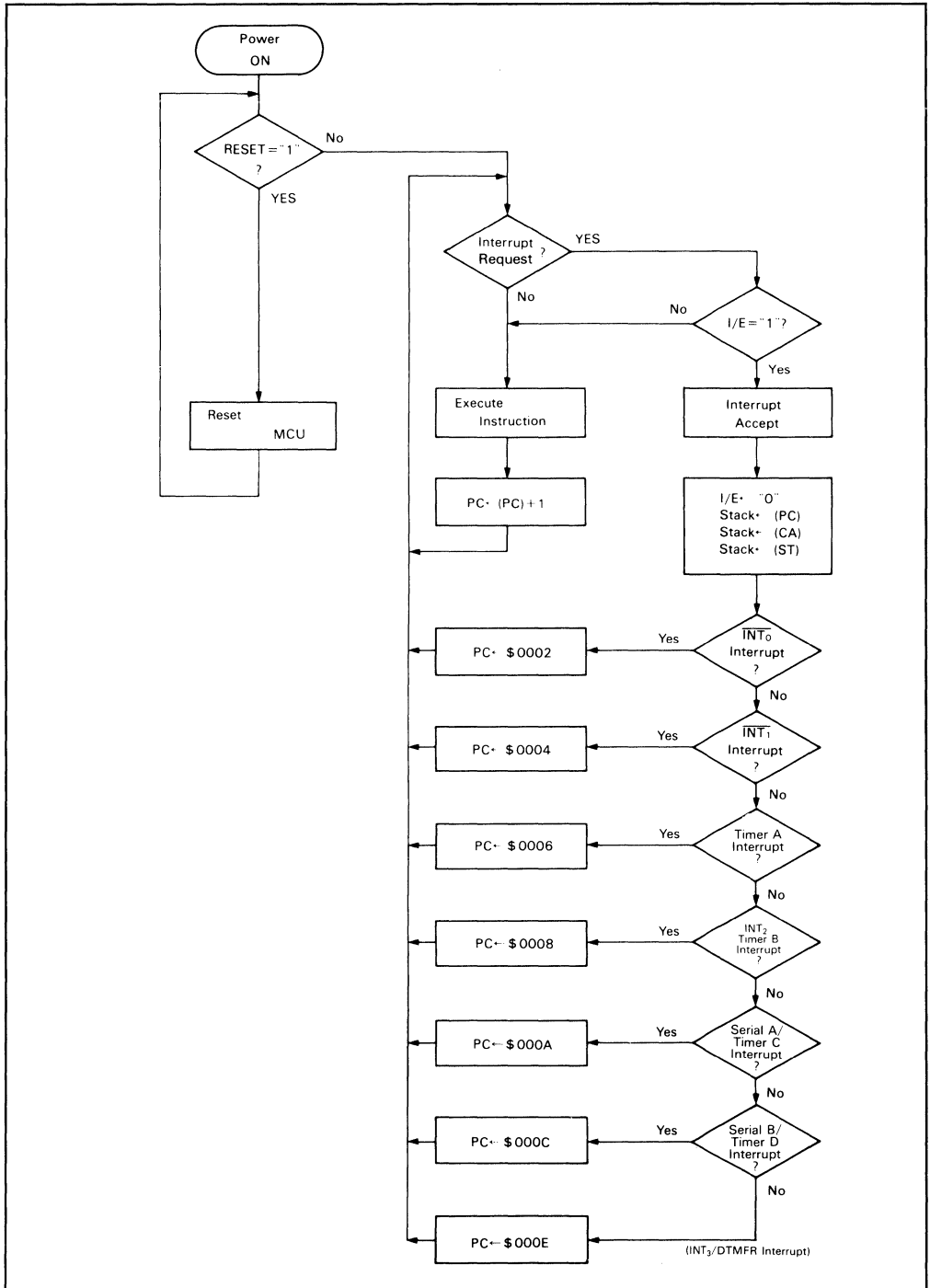


Figure 9. Interrupt Processing Flowchart



Interrupt Enable Flag (I/E: \$000, 0): The interrupt enable flag controls enable/disable of all interrupt requests. It is reset by interrupt processing and set by the RTNI instruction. (Table 6)

Table 6. Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt
0	Disable
1	Enable

External Interrupts ($\overline{\text{INT0}}$, $\overline{\text{INT1}}$, INT2, INT3): Four external interrupt pins are provided for the MCU. The external interrupt request flag is set at the falling edge of the INT0 and INT1 inputs. It is set at the rising edge of the INT2, and INT3 inputs.

When using $\overline{\text{INT0}}$ –INT3, the corresponding bit of port mode register A (PMRA: \$004) selects external interrupt input. If port mode register A is set, the data control register of the corresponding pin is reset automatically, and external interrupt input is enabled. If port mode register A is reset, external interrupt request flag is not set in spite of external interrupt signal input and interrupt processing is not performed since the external interrupt input signal is masked.

External Interrupt Request Flag (IF0: \$000, 2 IF1: \$001, 0 IF2: \$002, 0 IF3: 003, 2): External interrupt request flags IF0 and IF1 are set at the falling edge of the INT0 and INT1 inputs. IF2 and IF3 are set at the rising edge of the INT2 and INT3 inputs. (Table 7)

Table 7. External Interrupt Request Flag

External Interrupt Request Flag (IF0, IF1, IF2, IF3)	Interrupt Request
0	Disable
1	Enable

External Interrupt Mask (IM0: \$000, 3 IM1: \$001, 1 IM2: \$002, 1 IM3: \$003, 3): The external interrupt request masks disable the interrupt request from the external interrupt request flags. (Table 8)

Table 8. External Interrupt Mask Flag

External Mask Flag (IM0, IM1, IM2, IM3)	Interrupt Request
0	Enable
1	Disable (mask)

Low Power Dissipation Mode

The MCU has two low-power dissipation modes, standby mode, and stop mode. The low-power dissipation mode functions are shown in Table 9, and MCU operation mode relationships are shown in Figure 10.

Standby Mode: The MCU enters standby mode when a SBY instruction is executed. In this mode, an oscillator, interrupt, timer/counter, and serial interface (one of each) continue to operate, but all instruction-related clocks stop. This in turn stops the CPU, retains all RAM and register contents, and maintains current I/O pin status. The counter of the DTMF receiver continues to operate and the receiver retains the measurement value.

The standby mode is terminated by a RESET or interrupt request. After an interrupt request, the MCU resumes by executing the next instruction following the SBY instruction. Then, if the interrupt enable flag is "1", the interrupt is processed. If the interrupt enable

flag is "0", the interrupt request is left pending and normal instruction execution continues.

MCU operating flowchart in standby mode is shown in Figure 11.

Stop Mode: The MCU enters stop mode when a stop instruction is executed. In this mode, the oscillator stops, causing all MCU functions to also stop.

The stop mode is terminated by a RESET as shown in Figure 12. Reset must be High for at least one t_{RC} to stabilize oscillation. (See the 'AC Characteristics' section). During stop mode, all RAM contents are retained. When the MCU resumes after stop mode, the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry, and serial data register cannot be guaranteed.

Table 9. Low Power Dissipation Mode Function

Low Power Dissipation Mode	Instruction	Condition							DTMFR	Recovery Method
		Oscillator Circuit	Instruction Execution	Register, Flag	Interrupt Function	RAM	Input/Output Pin	Timer/Counter, Serial Interface		
Standby mode	SBY instruction	Active	Stop	Retained	Active	Retained	Retained ²	Active	Active	RESET input, interrupt request WDT
Stop mode	STOP instruction	Stop	Stop	RESET ¹	Stop	Retained	High impedance	Stop	Stop	RESET input

- Notes: 1. The MCU recovers from STOP mode by RESET input. Refer to tables 1 and 2 for the contents of the flags and registers.
 2. If an I/O circuit is active, an I/O current may flow, depending on the state of I/O pin in standby mode. This is the additional current to the current dissipation in standby mode.

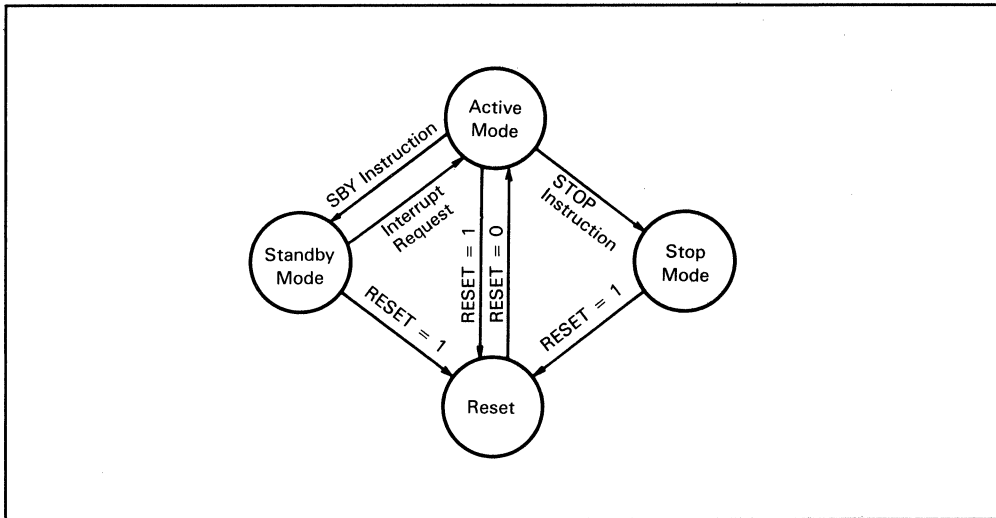


Figure 10. MCU Operation Mode Transition

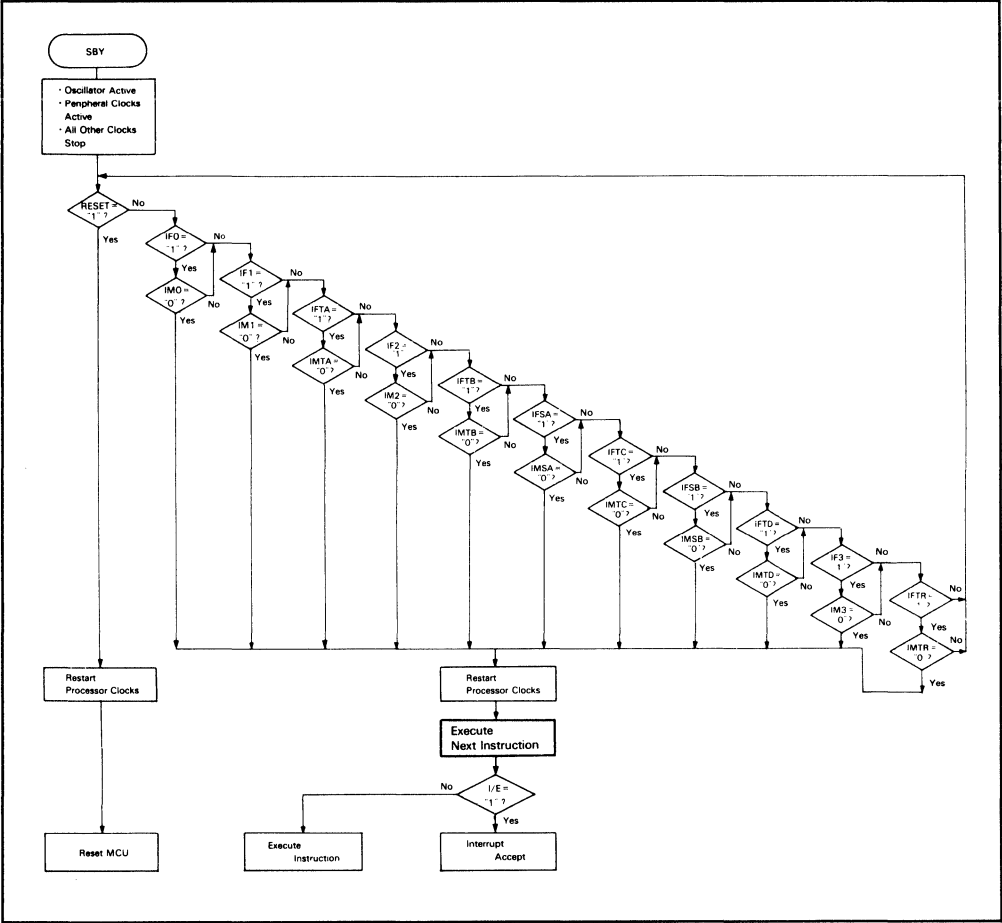


Figure 11. MCU Operating Flowchart in Standby Mode

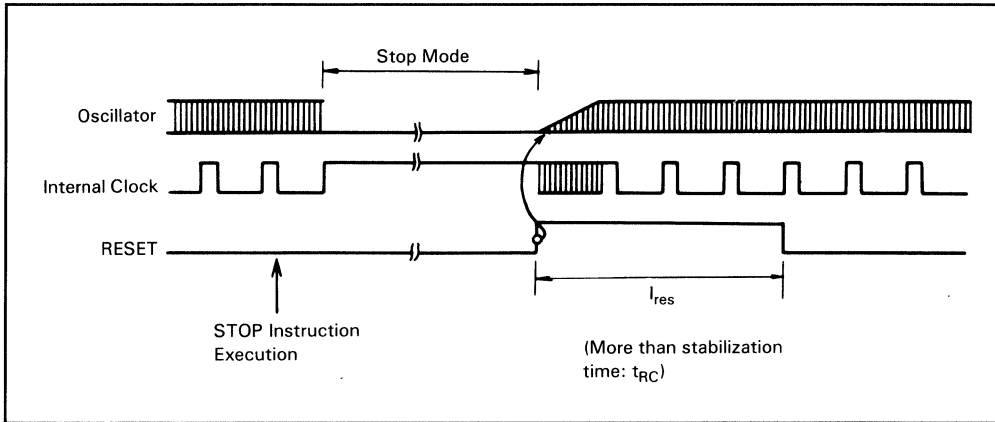


Figure 12. Timing Chart of Recovering from Stop Mode

Internal Oscillator Circuit

A block diagram of the internal oscillator circuit is illustrated in Figure 13. Crystal can be used as shown in Table 10. External clock operation is also available.

Table 10. Example of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation		
Crystal Oscillator	<p>AT cut parallel resonance crystal</p>	R_f : 1 M Ω \pm 20% C_1 : 10–22 pF \pm 20% C_2 : 10–22 pF \pm 20% Crystal: equivalent to circuit shown C_0 : 7 pF max. R_s : 100 Ω max. f : 4.0 MHz (\pm 0.01%)

- Notes: 1. The above circuit constants are recommended values provided by the oscillator manufacturer. They may change according to stray capacitance from the resonator or board, so please consult with the crystal manufacturer to determine the actual circuit parameters required.
 2. Wiring between the OSC 1/OSC 2 pin and an element must be as short as possible, and never cross other wiring. See the recommended layout of the crystal in Figure 14.

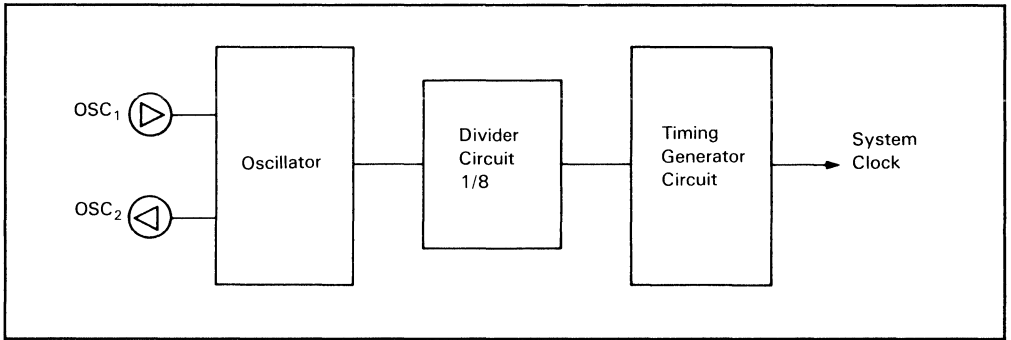


Figure 13. Internal Oscillator Circuit

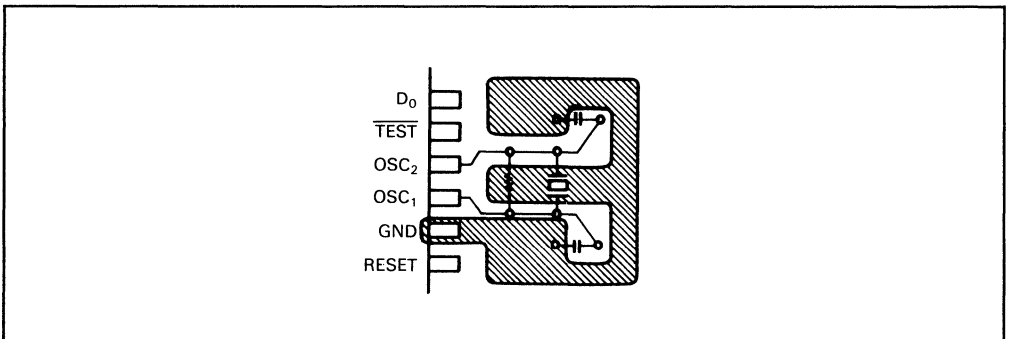


Figure 14. Layout of Crystal Oscillator

Input/Output

The MCU has 48 input/output pins and 4 dedicated input pins. All the input/output pins except the dedicated input port R8 have data control registers (DCR) that control the data direction. All ports, however, feature either a programmable pull-up MOS or pull-down MOS.

Several of the above pins are multiplexed with the input/output pins of peripheral circuits such as for the timer and serial interface. The peripheral circuit has priority on these pins. When set as a peripheral circuit's input or output, pin function and data direction for these pins are automatically selected accordingly.

I/O buffer configuration with pull-up and pull-down MOS is shown in Figures 15 and 16. The software directed I/O circuit control is shown in Tables 11 and 12. Several I/O types are available due to the combinations of the mode registers (PMRB, DCR, PDR) shown in these tables.

PMRB bit 3 controls on and off of all pull-up and pull-down MOS's. DCR and PDR control that of individual pins.

D Port: The D port is an I/O port having 16 I/O pins accessible on a bit basis. A maximum current of 15 mA can flow into each of the pins D0 to D9, with a total maximum current of less than 105 mA. In addition, D10–D15 can each act as a 10 mA maximum current source.

Pins D0–D9 and D10–D15 incorporate program controllable pull-up MOS and pull-down MOS, respectively. Data direction is controlled by the D port data control registers (DCRB–DCRE). DCR registers are mapped to RAM.

The D port can be set/reset with the SED/RED, SEDD/REDD instructions and tested with the TD/TDD instructions.

R Port: The R port consists of 32 I/O pins and 4 dedicated input pins, and is accessible on a 4-bit basis. R0–R7 are I/O ports and R8 is an input port. R0–R5 and R6–R8 have program controllable pull-up MOS and pull-down MOS, respectively. Pull-down MOS is controlled by PDR (Port Data Register) on a bit basis. The data direction of the I/O ports is controlled by the R port data control registers (DCR0–DCR7), which are also mapped to RAM. For the R port, the LRA/LRB instructions output the contents of the accumulator and B register through the port, and the LAR/LBR input instructions load port data into the accumulator and B register. Several of these pins are multiplexed with the I/O pins of peripheral circuits (Table 13).

Port R8 is a 4-bit dedicated input port accessed in 4-bit units. The R82 pin operates in two modes, digital input mode and analog input mode (variable voltage reset mode). In digital input mode, R82 functions as a dedicated input pin with input characteristics the same as other I/O pins. In analog input mode, comparison between a reference voltage input through R83/R_{ref} and R82/R_{IN} input is performed. If the input is higher than the R_{ref} voltage, the system is reset. After a reset pulse is automatically generated synchronously with the system cycle for one cycle, the MCU preceeds to execute from a reset vector. These operation modes are set by port mode register B (PMRB).

In analog mode, an analog voltage comparator is activated. To maintain required characteristics, analog current continues to flow into the analog comparator while it is on. Consequently, current dissipation increases in analog mode. Accordingly, to reduce current dissipation, a program should be prepared which sets R82 to analog mode only during analog comparison. Note that the analog comparator retains its previous state in standby mode, although in stop mode, it is automatically turned off.

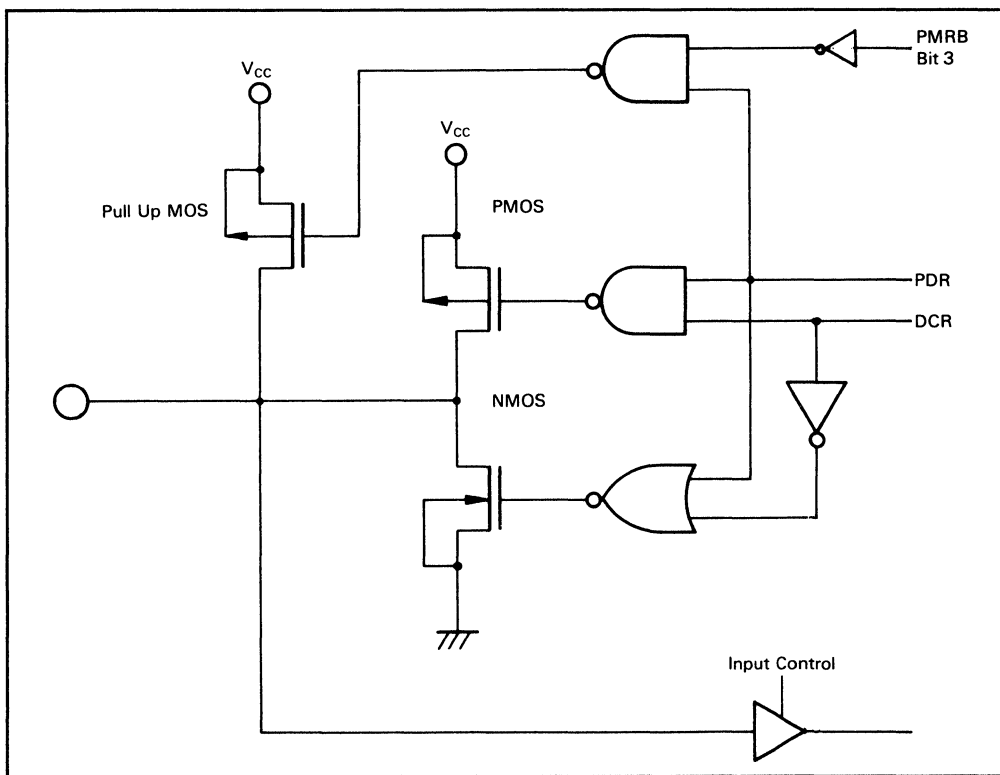


Figure 15. Configuration of I/O Buffer with Pull-up MOS

Table 11. Programmable I/O Combination (-: OFF)

Control Bit	PMRB Bit 3	1				0			
	DCR	0	1	0	1	0	1	0	1
I/O Circuit Condition	PMOS	-	-	-	ON	-	-	-	ON
	NMOS	-	-	ON	-	-	-	ON	-
	Pull-up MOS	-	-	-	-	-	ON	-	ON

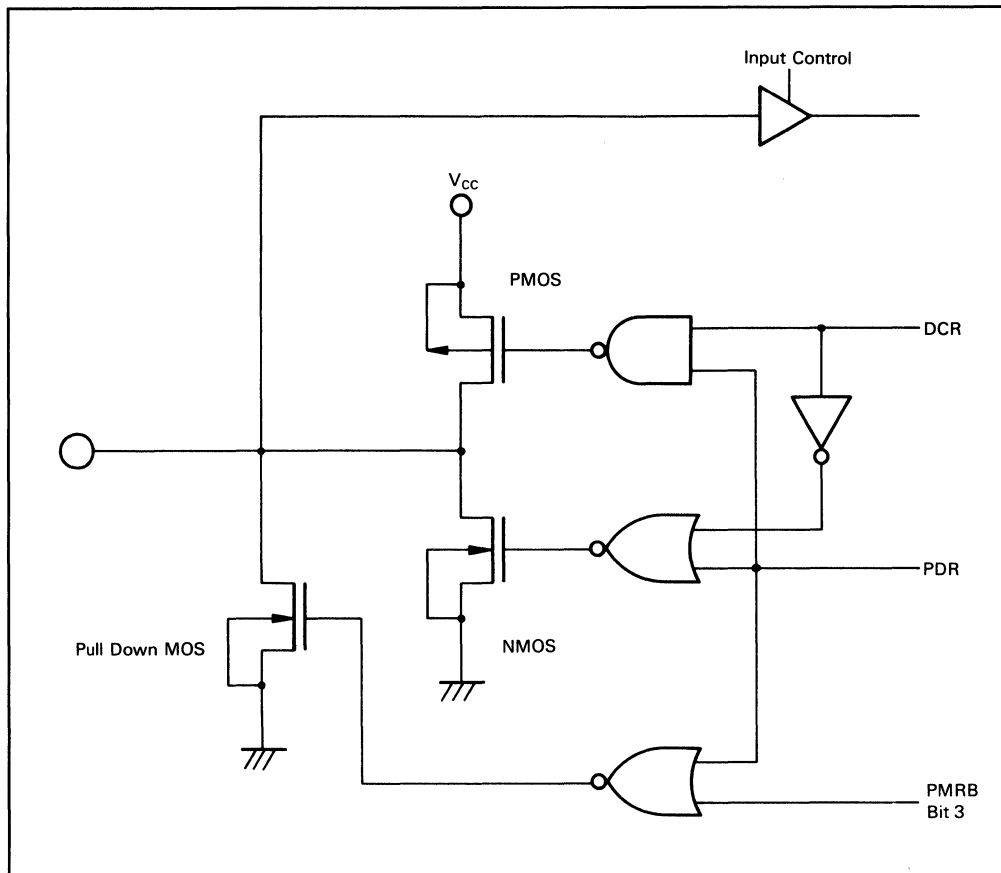


Figure 16. Configuration of I/O Buffer with Pull-down MOS

Table 12. Programmable I/O Combination (-: OFF)

Control Bit	PMRB Bit 3	1				0			
	DCR	0	1	0	1	0	1	0	1
PDR		0	1	0	1	0	1	0	1
I/O Circuit Condition	PMOS	-	-	-	ON	-	-	-	ON
	NMOS	-	-	ON	-	-	-	ON	-
	Pull-down MOS	-	-	-	-	ON	-	ON	-

For the R8 ports, the LAR/LBR instructions load port data into the accumulator and B register. This input-only port cannot be written to.

Data Control Registers (\$030-\$037, \$03B-\$03E): The data control registers (DCR) are 4-bit dedicated write registers which control the data direction of the I/O ports. DCRs are provided for the pins of the D port and R0-R7 ports as 4-bit registers to switch data direction on a bit basis (Table 14).

Each port loads data from a pin or pins when functioning as an input port, and loads data from a data register when functioning as an output port. Consequently, even if output potential varies by load when a port functions as an output, output data can be read correctly.

Since DCR is reset to "0" by reset input, all ports are inputs immediately after reset. To use a port as an output, the corresponding DCR must be set to "1" by a program initialization routine.

Port Mode Registers A, B, C (\$004-\$006): The port mode registers are 4-bit dedicated write registers. PMRA, PMRB, and PMRC have the functions shown in Tables 15, 16, 17.

PMRA controls the function of R32/ $\overline{INT_0}$, R33/ $\overline{INT_1}$, R62/ INT_2 , and R63/ INT_3 . These pins can be used as R-port pins when all bits of PMRA are initialized to "0".

If R32/ $\overline{INT_0}$ or R33/ $\overline{INT_1}$ is "Low" when bit 0 or 1 of PMRA is set, external interrupt request flag IF0 or IF1 is set. If R62/ INT_2 or R63/ INT_3 is "High" when bit 2 or 3 is set, external interrupt request flag IF2 or IF3 is set.

PMRB controls R42, R52, R82/ R_{IN} , R83/ R_{ref} , and pull-up MOS/pull-down MOS enable/disable of all ports. When bit 2 of PMRB is set to use the reset voltage variable function, and if a voltage higher than R_{ref} is applied to R_{IN} , the MCU will be reset.

0 to $V_{cc}-1.2 V$ must be applied to R_{ref} to enable the analog comparator function.

When bit 3 of PMRB is reset, pull-up/pull-down MOS attached to all ports are enabled and when it is set, they are disabled. While they are enabled, on/off of each pull-up/pull-down MOS can be controlled by bit settings in the PDR provided for each port. When PMRB bit 3 is initialized to "0" by MCU reset, pull-up/pull-down MOS of all ports are enabled.

PMRC controls R70/ TOB , R71/ TOC , R72/ TOD_1 , and R73/ TOD_2 . These pins function as R-port pins when PMR is initialized to "0" by MCU reset.

TOD_1 and TOD_2 are Timer D outputs which are actually identical signals. By controlling bit 2 and 3 of PMRC, Timer D output signals can be output to either or both TOD_1 and TOD_2 .

Table 13. Multiplexed Pins of R Ports

Pin	Multiplexed Pin	Control Register
R3 ₂	$\overline{INT_0}$	PMRA
R3 ₃	$\overline{INT_1}$ (Timer B input)	PMRA
R4 ₀	\overline{SCKA}	SMRA
R4 ₁	SIA	SMRA
R4 ₂	SOA	SMRA, PMRB
R5 ₀	\overline{SCKB}	SMRB
R5 ₁	SIB	SMRB
R5 ₂	SOB	SMRB, PMRB
R6 ₂	INT_2 (Timer C input)	PMRA
R6 ₃	INT_3 (Timer D input)	PMRA
R7 ₀	TOB	PMRC
R7 ₁	TOC	PMRC
R7 ₂	TOD_1	PMRC
R7 ₃	TOD_2	PMRC
R8 ₂	R_{IN}	PMRB
R8 ₃	R_{ref}	PMRB

Table 14. Data Control Registers and Control Pins

DCR	bit3	bit2	bit1	bit0
DCR0	R0 ₃	R0 ₂	R0 ₁	R0 ₀
DCR1	R1 ₃	R1 ₂	R1 ₁	R1 ₀
DCR2	R2 ₃	R2 ₂	R2 ₁	R2 ₀
DCR3	R3 ₃	R3 ₂	R3 ₁	R3 ₀
DCR4	R4 ₃	R4 ₂	R4 ₁	R4 ₀
DCR5	R5 ₃	R5 ₂	R5 ₁	R5 ₀
DCR6	R6 ₃	R6 ₂	R6 ₁	R6 ₀
DCR7	R7 ₃	R7 ₂	R7 ₁	R7 ₀
DCRB	D ₃	D ₂	D ₁	D ₀
DCRC	D ₇	D ₆	D ₅	D ₄
DCRD	D ₁₁	D ₁₀	D ₉	D ₈
DCRE	D ₁₅	D ₁₄	D ₁₃	D ₁₂

Table 15. Port Mode Register A Function

PMRA (Port Mode Reg. A)

Bit		3	2	1	0
Pin		R6 ₃ /INT ₃	R6 ₂ /INT ₂	R3 ₃ /INT ₁	R3 ₂ /INT ₀
Pin Function	0	R6 ₃	R6 ₂	R3 ₃	R3 ₂
	1	INT ₃	INT ₂	INT ₁	INT ₀

Table 16. Port Mode Register B Function

PMRB (Port Mode Reg. B)

Bit		3	2	1	0
Pin		Pull Up MOS, Pull Down MOS Disabled	R8 ₂ /R _{IN} R8 ₃ /R _{ref}	R5 ₂ (CMOS/NMOS)	R4 ₂ (CMOS/NMOS)
Pin Function	0	Resistor MOS Enabled	R8 ₂ , R8 ₃	CMOS	CMOS
	1	Resistor MOS Disabled	R _{IN} , R _{ref}	NMOS	NMOS

Table 17. Port Mode Register C Function

PMRC (Port Mode Reg. C)

Bit		3	2	1	0
Pin		R7 ₃ /TOD ₂	R7 ₂ /TOD ₁	R7 ₁ /TOC	R7 ₀ /TOB
Pin Function	0	R7 ₃	R7 ₂	R7 ₁	R7 ₀
	1	TOD ₂	TOD ₁	TOC	TOB

I/O Pins Unused on the User System: If unused I/O pins are left floating, the LSI may malfunction due to noise. To prevent this, unused pins should be dealt with as follows:

Ports with pull-up MOS—Pull up to V_{cc} through an incorporated pull-up MOS or a resistor of approximately 100 kΩ.

Ports with pull-down MOS—Pull down to GND through an incorporated pull-down MOS or a resistor of approximately 100 kΩ.

Unused pins other than ports—Pull up to V_{cc} through a resistor of approximately 100 kΩ.

During a programmed reset, the condition of unused pins must be retained. Accordingly, the data control register and any other registers related to these unused pins must not be changed.

Timer

The MCU incorporates a prescaler and four timers.

Timer A is an 8-bit free-running timer. Timer A is allowed to function as a watchdog timer with hardware reset.

The prescaler is an 11-bit counter to which a system clock signal is input. The prescaler divides this system clock signal into several different clock signals and outputs these signals to different timers. A prescaler output signal is also used as a transmit clock for the serial interface.

Timers B, C, and D are 8-bit versatile timers which can be respectively programmed as a free-running timer, reload timer, and PWM (duty variable pulse output). Timers B to D have I/O pins by which functions such as event counter or frequency variable clock output can be specified.

Table 18. Timer Function

	Input		Timer Function				Output				
	Pin Name	Edge	Free-running	Reload	PWM	Watch-dog	Pin Name	Function			
								Toggle	"0" Output	"1" Output	PWM
Timer A	No input pins		Yes	—	—	Yes	No output pins				
Timer B	TIB (R33)	↓	Yes	Yes	Yes	—	TOB (R70)	Yes	Yes	Yes	Yes
Timer C	TIC (R62)	↑	Yes	Yes	Yes	—	TOC (R71)	Yes	Yes	Yes	Yes
Timer D	TID (R63)	↑	Yes	Yes	Yes	—	TOD1 (R72)	Yes	Yes	Yes	Yes
							TOD2 (R73)	Yes	Yes	Yes	Yes

Prescaler: The prescaler is an 11-bit counter whose input is the system clock. After being initialized to \$000 by MCU reset, the prescaler counts up by clock cycles. The prescaler outputs are fed to Timers A-D and serial interfaces A-B. The prescaler continues counting except during MCU reset and stop mode. It cannot be read from or written to, and its divide ratio can be independently programmed.

Operation of Timer A: Functions as a free-running timer and a watchdog timer.

Free-running timer operation—Timer A is an 8-bit count-up timer that increments with every input clock.

When specified as a free-running timer, Timer A's input clock is selected among the 8 clocks output by the prescaler using TCS2-TCS0 of timer mode register A.

When Timer A reaches \$FF, it generates an overflow, and the Timer A interrupt request flag is set. Timer A then restarts counting from \$00. The timer interrupt request flag is not reset even when an interrupt is accepted; it must be reset by an instruction in an interrupt processing routine.

Timer A (free-running timer) is used to generate an interrupt at regular intervals.

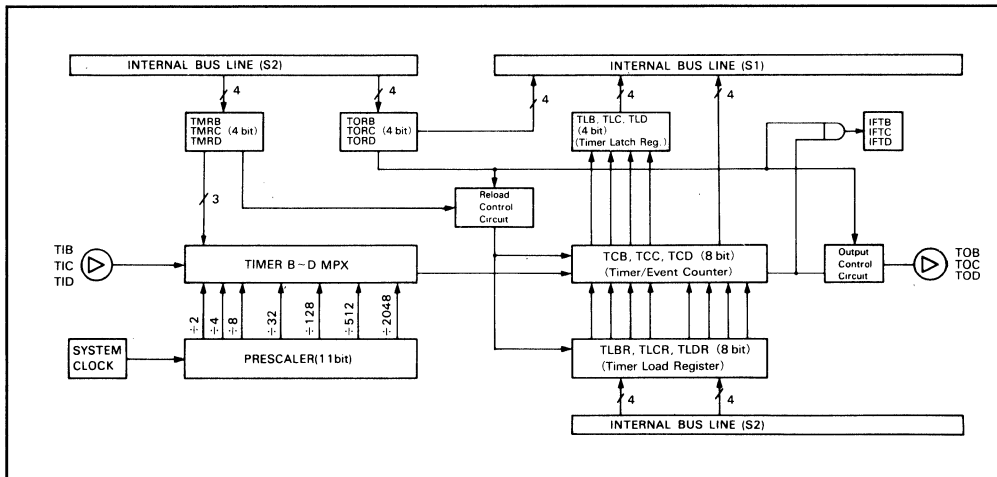


Figure 17. Timers B-D Block Diagram

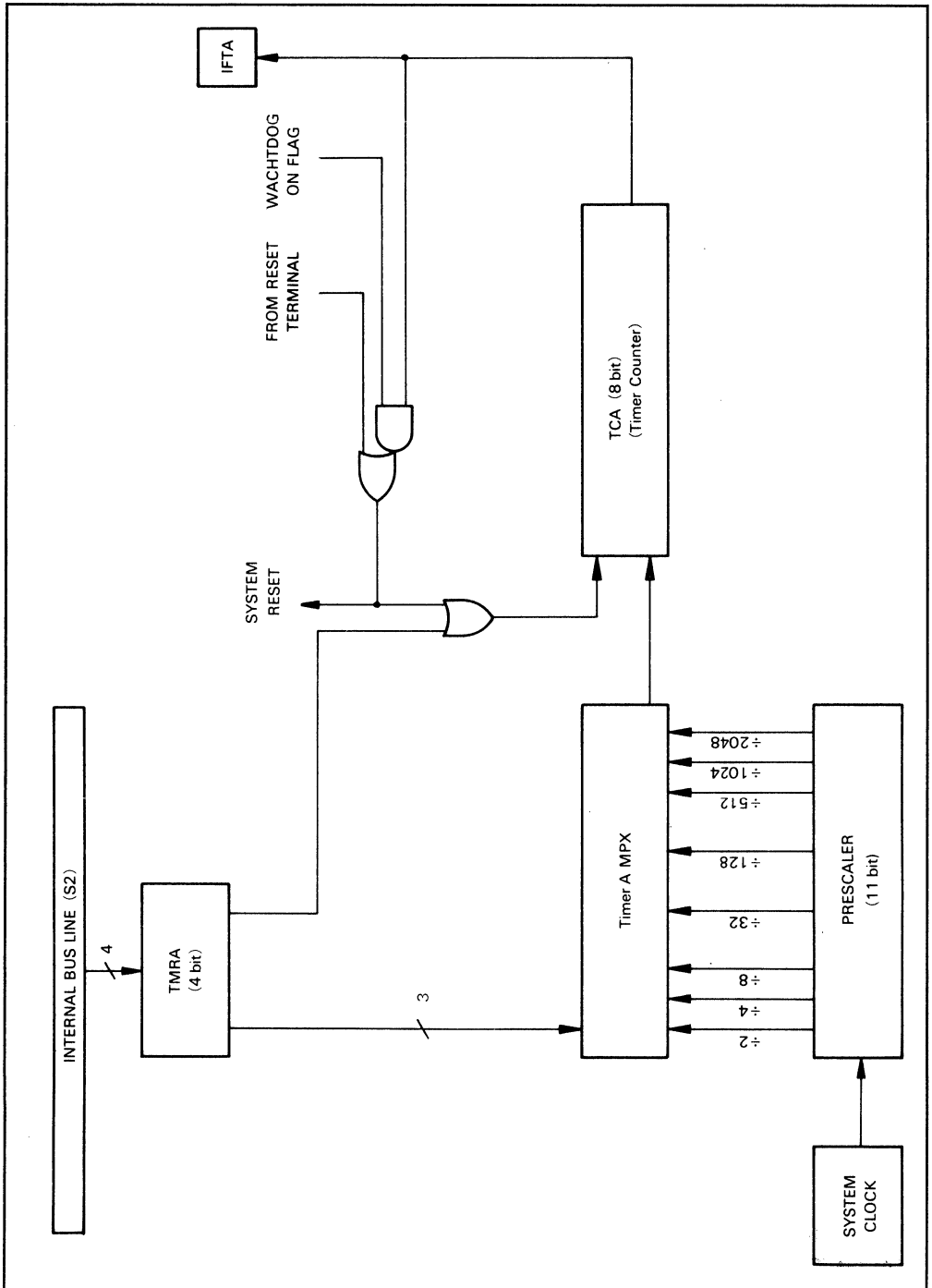


Figure 18. Timer A Block Diagram

Watchdog timer operation—Timer A can function as a watchdog timer that increments with every input clock. When Timer A overflows, an internal reset signal is generated. If WDTR of timer mode register A is set, Timer A is reset and begins counting from \$00.

A watchdog timer can reset and recover the MCU when control has been lost. To enable the function, program must be prepared so that Timer A is reset within the cycle shorter than the prescaler output and the cycle counted by timer A. In such a program, an overflow is not generated during normal MCU operation, because the timer has been reset by the program. However, when the MCU is out of control, Timer A generates an overflow, and the MCU is reset.

In watchdog timer mode, Timer A is initialized to \$00 with a reset signal via the RESET pin. When an overflow is generated, an interrupt does not occur since the MCU has already been reset. The timer can be reset but cannot be written to or read.

Operation of Timers B, C, D: Timers B to D are 8-bit multifunctional timers. Three operation modes—free-running, event counter, reload, and PWM—are provided by programming the timer mode registers (TMRB, TMRC, TMRD) and timer output registers (TORB, TORC, TORC).

The timer/counters (TCB, TCC, TCD) count up with every input clock after being initialized to "00" by MCU reset. An input clock can be selected among the clock divided by the prescaler, and an external clock

is available for the event counter. When selecting an external clock input, the interrupt mask bit of each external interrupt must be set to inhibit external interrupt since an external clock input pin is multiplexed with an external interrupt pin.

The timer interrupt request flags (IFTB, IFTC, IFTD) are set if an input clock is supplied after the timer/counters reach \$FF. When auto-reload function is not specified, Timers B–D function as free-running timers/event counters, and restart to count up from \$00. When auto-reload function is specified, Timer B–D function as reload timers. In the reload mode, an overflow signal causes the timer load register value to be loaded into the timer/counter, and the timer counts up from that value.

Timers B–D also function as timer input/output circuits. The timer output circuits varies output level when the clock after reaching \$FF is input. By combining this circuit and the reload timer, several different cycle clock signals can be output.

Timers B–D are set in PWM mode when the timer output register is programmed. The cycle of the pulse is 256 clocks, and the length of the "High" portion is the same value as that of the timer load register. A voltage level proportional to the value set in the timer load register can be obtained by combining PWM and a lowpass filter.

Table 19. Timer A Function

Item	Free-running Timer	Watchdog Timer
Prescaler Divide Ratio		Variable (8: + 2 to + 2048)
Timer Reset		Possible (Write 1 to WDTR)
Interrupt Function	Provided	None
Internal System Reset Function	None	Provided

Timer Mode Register A (TMRA: \$007): 4-bit write-only register. Timer mode register A function is shown in Figure 19 and Table 20.

Timer Mode Registers B, C, D (TMRB: \$008, TMRC: \$00C, TMRD: \$010): 4-bit write-only registers which control the auto-reload function, input source, and prescaler divide ratio of timers B, C, D as shown in Figure 20 and Table 21. These registers are initialized to \$0 by MCU reset.

The timer mode register value can be changed from the third instruction after executing the timer mode register write instruction. Timer initialization by the timer load register write instruction must be executed after the varied mode becomes valid.

Timer Output Registers B, C, D, (TORB: \$009, TORC: \$00D, TORC: \$011): 4-bit read/write registers which control the output mode, PWM output mode, the external interrupt multiplexed with timer input pins of

Timers B–D as shown in Figure 21 and Table 22. By combining these modes and various mode of Timers B–D, several different frequencies and duty clock signals can be obtained. When setting PWM output, the timer output pin functions as a PWM output regardless of timer output mode. Timer output register value becomes valid from the third instruction after the timer output register write instruction.

Timer Counters BL, BU, CL, CU, DL, DU (TCBL: \$00A, TCBU: \$00B, TCCL: \$00E, TCCU: \$00F, TC DL: \$012, TCDU: \$013), Timer Load Registers BL, BU, CL, CU, DL, CU (TLBL: \$00A, TLBU: \$00B, TLCL: \$00E, TLCU: \$00F, TLDL: \$012, TLDU: \$013): Timers B–D are 8-bit timers comprised of read-only timer counters and write-only timer load registers at the same address. Each register is divided into low and high nibbles which are located at sequential addresses.

The high data nibble is read from the timer/counter first. At the same time, the low nibble is latched into

the 4-bit timer latch register. When a low nibble is read, it is read from the latched register. Therefore, it is possible to read a high and low nibble at the same time.

After data is written in the timer load register, it is loaded into the timer/counter and the timer begins counting from the loaded value. The low nibble must be written in the timer load register first. The timer mode register value is loaded into the timer/counter at the same time the high nibble is written to. The timer/counter and timer load register are initialized to '\$00' during reset.

Timers B, C, D, Operation Modes: Various modes can be provided by Timers B–D by programming each timer mode register and timer output register. Programmable operation modes are listed in Table 25. Timer output waveform examples are shown in Figure 21.

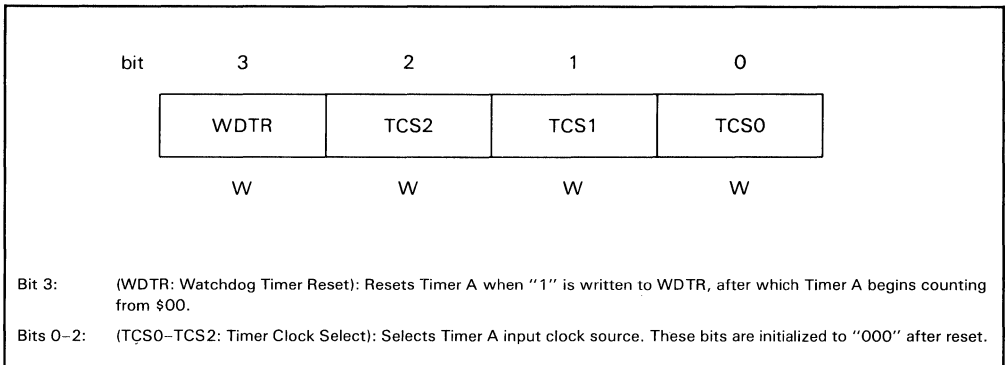
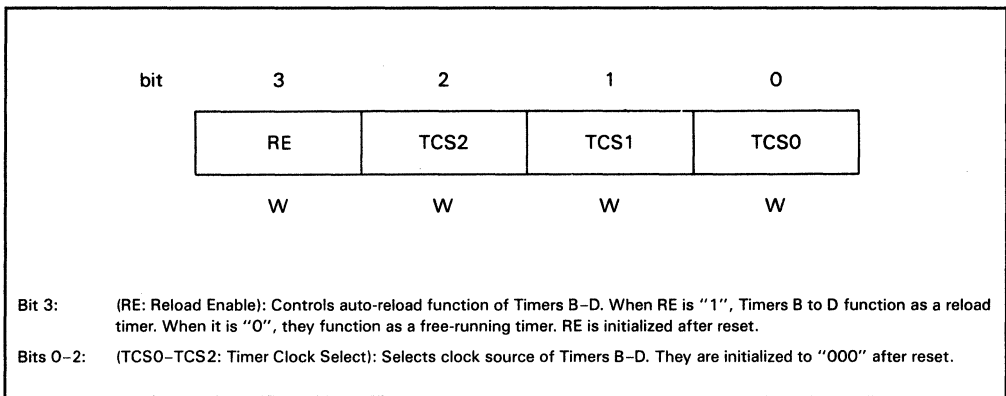


Figure 19. Timer Mode Register A

Table 20. Input Clock Source Selection for Timer A

Timer Mode Register Bit			Input Clock Source
TCS2	TCS1	TCS0	
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2



Bit 3: (RE: Reload Enable): Controls auto-reload function of Timers B–D. When RE is “1”, Timers B to D function as a reload timer. When it is “0”, they function as a free-running timer. RE is initialized after reset.

Bits 0–2: (TCS0–TCS2: Timer Clock Select): Selects clock source of Timers B–D. They are initialized to “000” after reset.

Figure 20. Timer Mode Registers B, C, D

Table 21. Input Clock Source Selection for Timers B, C, D

Timer Mode Register Bit			Input Clock Source
TCS2	TCS1	TCS0	
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	(External event input)*

*When external event input is selected, pins R33, R62, and R63 should have been set to INT input by PMRA.

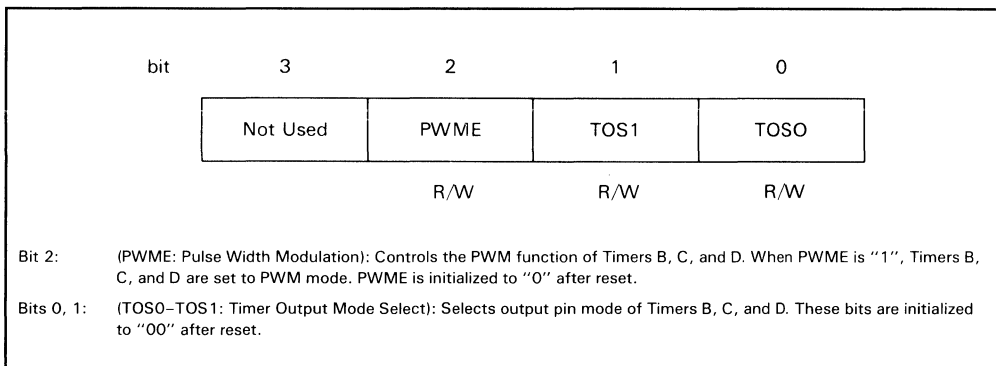


Figure 21. Timer Output Register

Table 22. Output Mode Selection of Timers B, C, D

Timer TOS1	Output TOSO	Register Bit Output Mode	Function
0	0	–	Output disabled
0	1	Toggle output	Output is reversed synchronously with timer overflow
1	0	"0" output	Low is output synchronously with timer overflow
1	1	"1" output	High is output synchronously with timer overflow

Note: For timer output, pins R70, R71, R72, and R73 must be set to timer output mode by PMRC.

Table 23. Operation Modes of Timers B, C, D

PMRA	PMRC	TMRB, TMRC, TMRD				TORB, TORC, TORC			Timer Input Pin	Timer Output Pin	Timers B-D Function
		Bit 3	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0			
1	0	0	1	1	1	0	0	0	TIB, TIC, TID	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	Event Counter
1	1	0	1	1	1	0	* 2	* 2	TIB, TIC, TID	TOB, TOC, TOD ₁ , TOD ₂	
0	0	0	* 3	* 3	* 3	0	0	0	R3 ₃ , R6 ₂ , R6 ₃	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	Free-running Timer
0	1	0	* 3	* 3	* 3	0	* 2	* 2	R3 ₃ , R6 ₂ , R6 ₃	TOB, TOC, TOD ₁ , TOD ₂	
1	0	0	* 3	* 3	* 3	0	0	0	$\overline{\text{INT}}_1$, INT ₂ , INT ₃	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	
1	1	0	* 3	* 3	* 3	0	* 2	* 2	$\overline{\text{INT}}_1$, INT ₂ , INT ₃	TOB, TOC, TOD ₁ , TOD ₂	
0	0	1	* 3	* 3	* 3	0	0	0	R3 ₃ , R6 ₂ , R6 ₃	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	Reload Timer
0	1	1	* 3	* 3	* 3	0	* 2	* 2	R3 ₃ , R6 ₂ , R6 ₃	TOB, TOC, TOD ₁ , TOD ₂	
1	0	1	* 3	* 3	* 3	0	0	0	$\overline{\text{INT}}_1$, INT ₂ , INT ₃	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	
1	1	1	* 3	* 3	* 3	0	* 2	* 2	$\overline{\text{INT}}_1$, INT ₂ , INT ₃	TOB, TOC, TOD ₁ , TOD ₂	
1	0	1	1	1	1	0	0	0	TIB, TIC, TID	R7 ₀ , R7 ₁ , R7 ₂ , R7 ₃	Event Counter (with reload function)
1	1	1	1	1	1	0	* 2	* 2	TIB, TIC, TID	TOB, TOC, TOD ₁ , TOD ₂	
0	1	* 1	* 3	* 3	* 3	1	* 1	* 1	R3 ₃ , R6 ₂ , R6 ₃	TOB, TOC, TOD ₁ , TOD ₂	PWM * 4
1	1	* 1	* 3	* 3	* 3	1	* 1	* 1	$\overline{\text{INT}}_1$, INT ₂ , INT ₃	TOB, TOC, TOD ₁ , TOD ₂	
1	1	* 1	1	1	1	1	* 1	* 1	TIB, TIC, TID	TOB, TOC, TOD ₁ , TOD ₂	* 4 PWM (external clock)

*1: Neither "0" nor "1" affect operation.

*2: Either or both TOR bits 0 and 1 are "1".

*3: One, two, or all TMR bits 0-2 are "0".

*4: If the timer load register value is \$00 when PWM output is selected, the timer functions as a free-running timer.

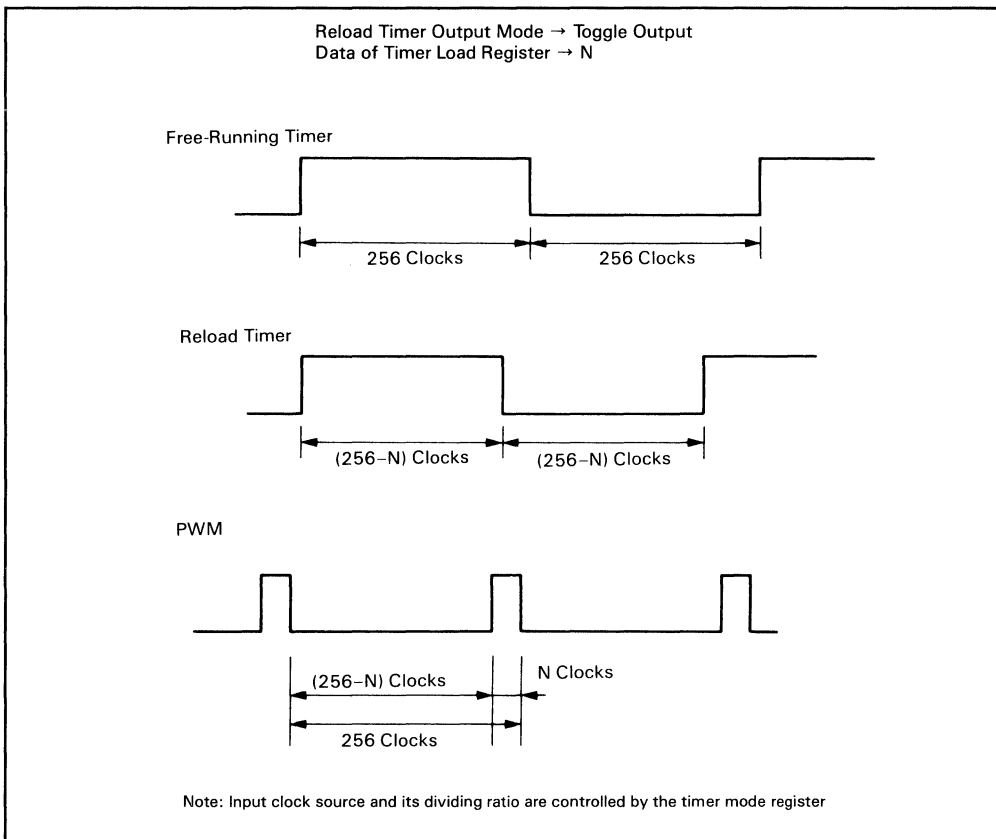


Figure 22. Timer Output Waveform Examples

Serial Interface

The MCU incorporates two clock-synchronous 8-bit serial interfaces that are composed of serial data registers, serial mode registers, serial clock registers, octal counters, and multiplexers as shown in Figure 22.

Two serial interfaces have identical function, however, the transfer clock and transmit speed can be set independently. Each serial interface also functions as a clock output.

Table 24. Serial Interface Function

Item	Function	
Transmit Format	Clock synchronous serial interface (LSB transmitted first)	
Number of Transmit Bits	8 bits	
Transmit Rate ($t_{cyc} = \text{Baud Rate at } 2 \mu\text{s: BPS}$)	$1/t_{cyc}$ (500000 to $1/4096 \times t_{cyc}$ (122))	
Operation Mode	Transmit mode: transmit mode receive mode transmit/receive mode Special mode: clock output mode	
Transmit Clock	Internal Clock (transmit clock output) External Clock (transmit clock input)	
Pin	Serial Interface A	Clock SCKA R40 I/O Data Input SIA R41 I Data Output SOA R42 O
	Serial Interface B	Clock SCKB R50 I/O Data Input SIB R51 I Data Output SOB R52 O

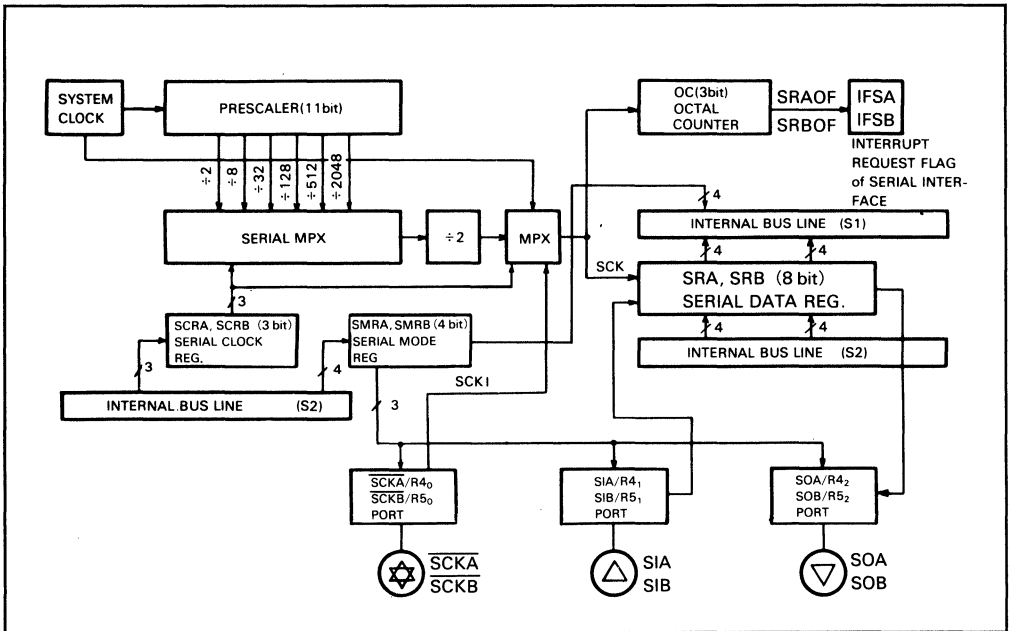


Figure 23. Serial Interface Block Diagram

Serial Mode Registers A, B, (SMRA: \$014, SMRB: \$018: 4-bit read/write registers which control serial interface operation and the SCKA, SCKB, SIA, SIB, SOA, and SOB pins as explained in Figure 23. When the serial mode register is written to, transmit clock stops to be supplied to the serial data register and octal counter, then the octal counter is initialized to \$0. Therefore, if the serial mode register is written to

during serial interface operation, data transmission stops and the serial interrupt request flag is set.

Serial mode register change becomes valid from the second instruction after the serial mode register write instruction, so that the STS instruction must be executed two cycles after the serial mode register write instruction. The serial mode register is initialized to \$0 by MCU reset.

Table 25. Related Serial Interface Registers

Serial Interface	Register Name	Abbr.	Address	Read/Write
Serial Interface A	Serial Mode Register A	SMRA	\$014	R/W
	Serial Clock Register A	SCRA	\$015	W
	Serial Data Register A (L)	SRAL	\$016	R/W
	Serial Data Register A (U)	SRAU	\$017	R/W
Serial Interface B	Serial Mode Register B	SMRB	\$018	R/W
	Serial Clock Register B	SCRB	\$019	W
	Serial Data Register B (L)	SRBL	\$01A	R/W
	Serial Data Register B (U)	SRBU	\$01B	R/W

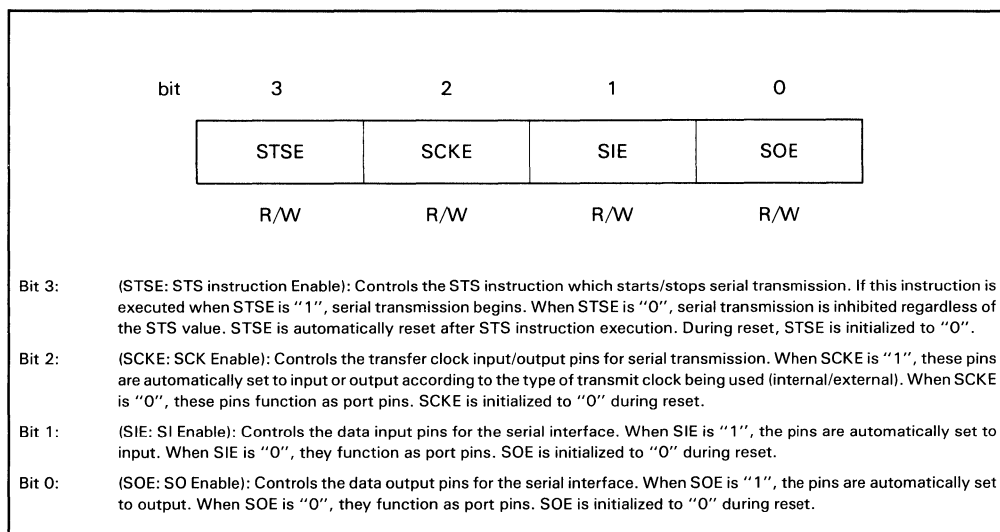


Figure 24. Serial Mode Registers A, B

Serial Clock Registers A, B, (SCRA: \$015, SCRB: \$019): 3-bit dedicated write registers. These registers can be written to on a bit basis with the bit set/bit reset instruction other than on a nibble basis.

Writing in the serial clock register becomes valid two cycles after instruction execution. Writing in the reg-

ister initializes the octal counter to "000". If the serial clock register is written to during transmission, the octal counter becomes "000" to stop transmission, and the serial interrupt request flag is set at the same time.

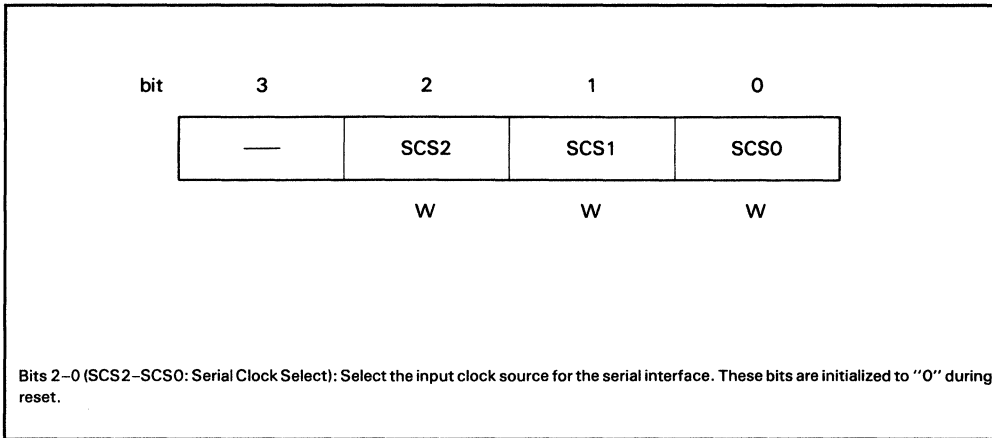


Figure 25. Serial Clock Register

Table 26. Input Clock Sources

Bit			SCK I/O	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio	Baud Rate at $t_{cyc} = 2\mu s$ (BSP)
SCS2	SCS1	SCS0					
0	0	0	0	Prescaler	-2048	-4096	122
0	0	1	0	Prescaler	-512	-1024	488
0	1	0	0	Prescaler	-128	-256	1953
0	1	1	0	Prescaler	-32	-64	7812
1	0	0	0	Prescaler	-8	-16	31250
1	0	1	0	Prescaler	-2	-4	125000
1	1	0	0	System Clock	—	-1	500000
1	1	1	1	External Clock	—	—	—

Note: If an internal clock is selected (transmit clock output: SCK I/O = 0) when the SCKE bit of the serial clock mode register is "1", the clock input/output pin is automatically set to output. When an external clock (transmit clock input: SCK I/O = 1) is selected, the pin is automatically set to input.

Serial Data Registers AL, AU, BL, BU (SRAL: \$016, SRAU: \$017, SRBL: \$01A, SRBU: \$01B): The serial data registers are 8-bit registers which shift to the right (towards the LSB) with every transfer clock input. During serial transmission, the LSB is output through a data pin and "0" is written to the MSB. In transmit/receive mode, the LSB output and MSB input are performed at the same time.

The serial data register is separated into low and high nibbles which are located at sequential addresses. Therefore, data read/write must be performed twice. Since data shift and data read/write are performed asynchronously, data read/write cannot be performed during serial data transmission. If read/write is executed during serial transmission, the accuracy of the data cannot be guaranteed.

The serial data register cannot be reset. The value of the serial data register is undefined after reset.

Serial Interface Operation: The serial interface is used to transmit data between the HD404678 and other devices. As shown in Figure 26, the clock pin, data input pin, and data output pin one device are connected to the respective clock pin data output pin, and data input pin of another device. If one-directional transfer is required, a data input pin and a data output pin are connected. For example, during serial transmission from the HD404678, the serial output pin of the HD404678 and the data input pin of the other device are connected. (The HD404678 can also

operate in receive mode.) Data transfer timing is shown in Figure 27.

Proper transfer timing and AC timing must be implemented for serial transmissions to different devices.

Note that the HD404678 transmits the LSB first, however, some other devices transmit the MSB first. Accordingly, the order of data conversion should be checked.

STS Instruction and STSE Bit: The STS instruction (Start Serial) initiates two serial interface operation. Each serial interface has a STS instruction enable bit (STSE). When this bit is set, the STS instruction is executed. When both STSE bits are set, two serial interfaces operate with one STS instruction. Conversely, when two STSE bits are reset, the serial interface does not operate even if the STS instruction is executed. To prevent conflict between two serial interfaces, after the STS instruction is executed, the STSE bit is automatically reset at the following cycle.

Serial Interface Operation Mode: The serial interface operation mode is set with the serial mode register, and the serial transmit clock is set with the serial clock register. The serial interface has four operation modes: three transmit modes and a special mode. When the serial interface is set in any of these modes, the pins multiplexed with ports function as serial input/output pins.

Table 27. Serial Interface Operation Modes

Serial Mode Register Bit			Serial Interface Operation Modes	
SCKE	SIE	SOE		
1	0	1	Transmit Mode	Transmit Mode
1	1	0	Receive Mode	Transmit Mode
1	1	1	Transmit/Receive Mode	Transmit Mode
1	0	0	Clock Output Mode	Special Mode

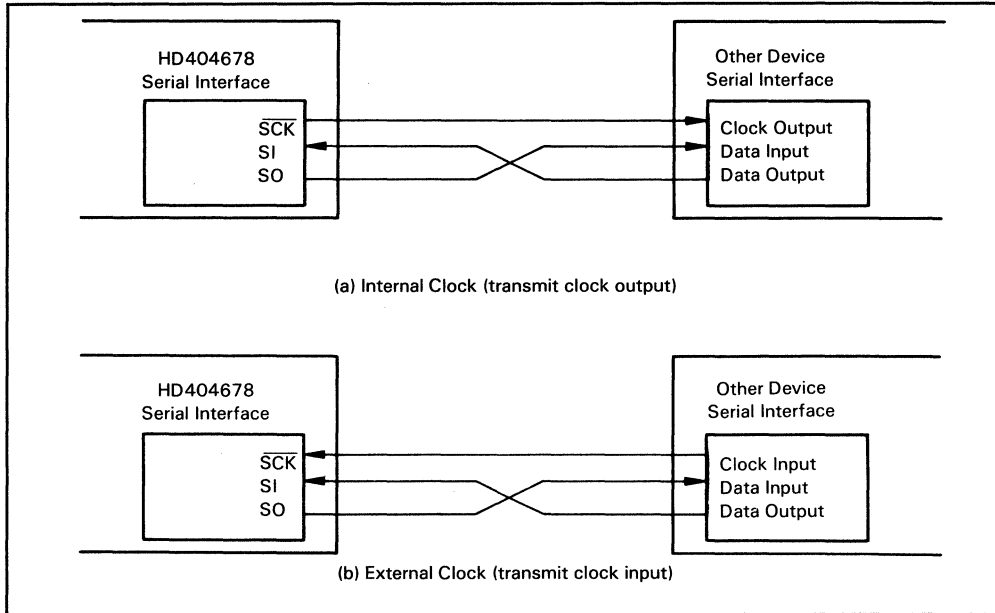


Figure 26. Serial Interface Connection

Transmit mode: Data is transmitted synchronously with a transmit clock. At the same time, "0" is received by the MSB.

Receive mode: Data is received via an input synchronously with the transmit clock.

Transmit/receive mode: Data is transmitted and received simultaneously and synchronously with a transmit clock.

Clock output mode: A transmit clock is output when transmit clock output mode (internal clock) is selected. The serial data register does not shift.

Data Transmit Procedure: Four operating states are provided for the serial interface. Their interaction is shown in Figure 28.

The serial interface is initialized in the transfer inhibit state in which the STS instruction and transmit clock are ignored.

The serial interface is in a STS wait state if the STSE bit of the serial mode register of the desired serial interface is set. When the STS instruction is executed while the STSE bits of the serial interfaces 1 and 2 are both set, two serial interfaces can be controlled by one STS instruction.

During a transfer clock wait state, an input to the transmit clock increments the octal counter, shifts the

serial data register, and starts serial transmission. If a clock output mode is selected by the serial mode register, the transmit clock continues to output without data transmission.

During transmission, 8 clock inputs set the octal counter "000" and also set the serial interrupt request flag. In this state, if the internal clock is selected, serial transmission is inhibited, and if an external clock is selected, the system enters a transmit clock wait state. If the serial mode register and the serial clock register are written to during transmission, the octal counter is set to "000", which stops transmission, and, at the same time, the interrupt request flag is set.

Transmit Clock Error Detection: The serial interface malfunctions when a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error can be detected as shown in Figure 29.

During a transmit clock wait state, more than 8 transfer clock inputs set the serial interface transmit state, and transmit clock wait state, and then transmit state. If the serial interrupt request flag (IFS) is reset after SMR has been programmed to enter a STS wait state, the serial interrupt request flag is again set.

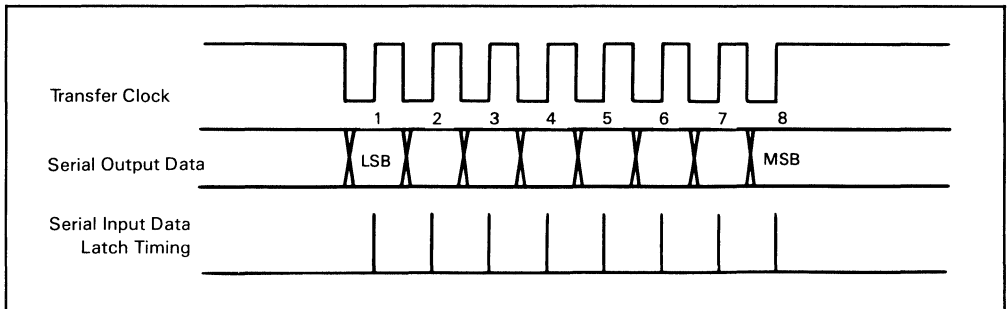


Figure 27. Serial Interface I/O Timing Chart

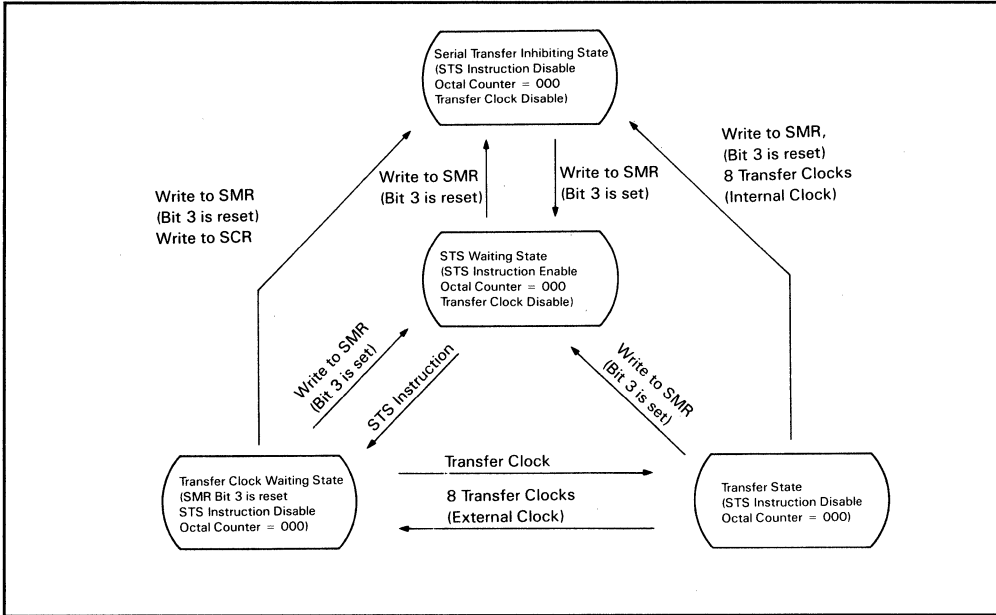


Figure 28. Serial Interface Operation State

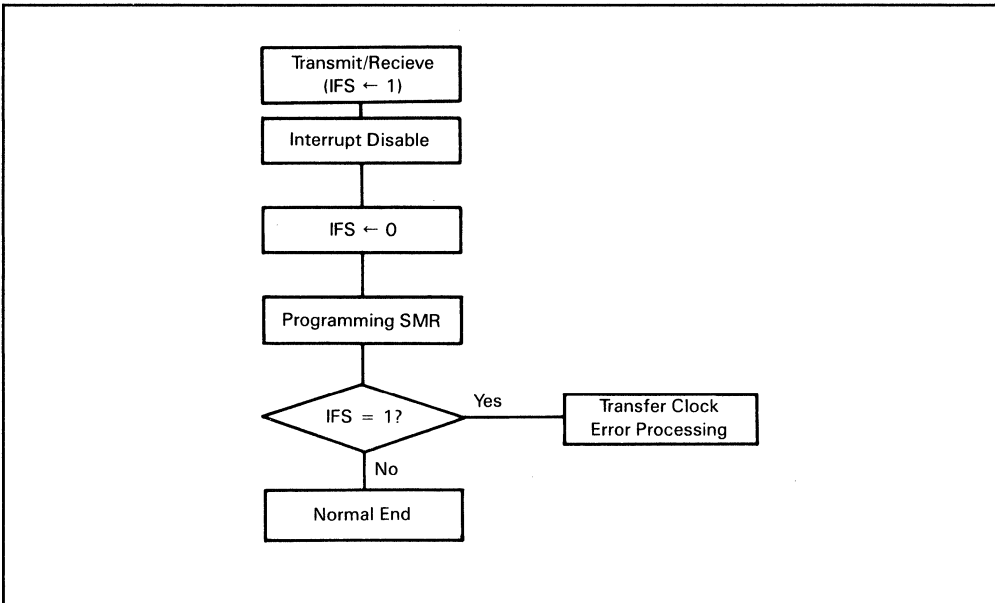


Figure 29. Example of Transfer Clock Error Detection

DTMF Receiver

The HD404678 incorporates a high-/low-group isolation circuit and a frequency measurement circuit for DTMF signal reception. A DTMF signal can be examined by these circuits. A block diagram of the DTMF receiver is shown in Figure 30.

The DTMF signal is generated by mixing two sine waves, one of four low-group frequencies (697, 770, 852, 941 Hz) and one of four high-group frequencies (1209, 1336, 1477, 1633 Hz). The signal is used for communication using telephone lines. Figure 31 shows a matrix of telephone push buttons and the DTMF frequencies.

The DTMF signal is a mixed wave passed through a nonlinear telephone line, so that the receiver recognizes that the signal includes harmonic and inter-modulation components other than the two main frequencies mentioned above.

DTMF Receiver Configuration

High-/Low-group Isolation Circuit: A high-/low-group isolation circuit consists of a gain control pre-amplifier, an anti-aliasing filter, high-group/low-group band pass filters, and high precision comparators.

The gain control pre-amplifier compensates for line loss and loss generated within a telephone set.

The anti-aliasing filter is an analog filter to reduce sampling noise in a following SCF (Switched Capacitor Filter). It employs a second-order Sallen-Key circuit having a cutoff around 8 kHz (typ).

The high-/low-group band pass circuit is a sixth-order band pass filter comprising SCF. The rejection ratio of the low-/high-group is designed to be 32 dB. (Figure 34)

The high-precision comparator incorporates an offset compensation circuit to detect the zero-crossing point of a signal isolated in high- and low-group.

Frequency Measurement Circuit: The frequency measurement circuit is comprised of the following control sections, edge generation circuits, edge counters, period counters, data registers, and flags.

The edge counter is a 4-bit counter whose value can be set from a half cycle up to 7.5 cycles. Several cycles are required to be examined to prevent malfunction due to voice characteristics.

The period counter is a 10-bit counter. One bit is equivalent to 10 μ s for high-group and to 20 μ s for low-group.

The measurement value hold register is a 10-bit register holding three sequential addresses in RAM.

To recognize a frequency, the period between zero-crossings must be measured by the edge and period counters. The period counter counts the time until the edge counter reaches the desired value. When the edge counter reaches the desired value, the value of the period counter at this time is fetched into the measurement value hold register. The edge and period counters are then initialized to start measurement of the next cycle. At the same time, an load flag is set, by which the CPU acknowledges that a measurement value has been loaded into the measurement value hold register. The CPU can then recognize DTMF signal transmission and code by examining whether the value corresponds to a DTMF signal.

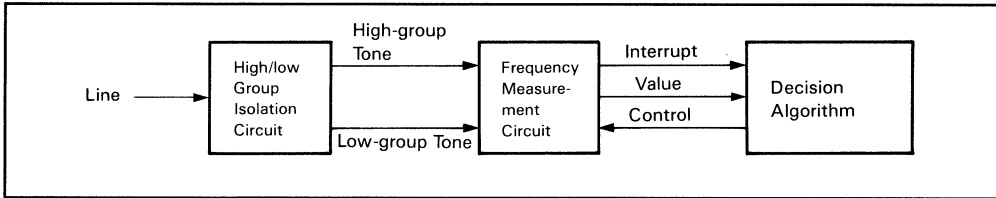


Figure 30. DTMF Receiver Block Diagram

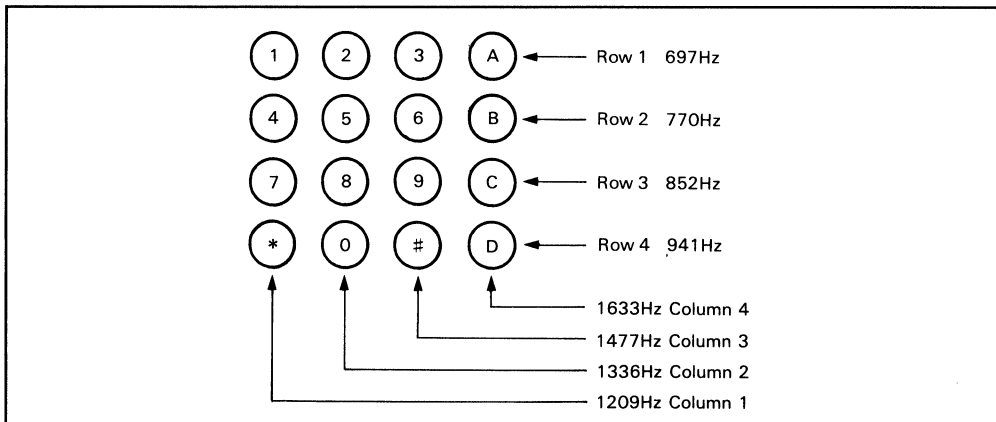


Figure 31. DTMF Keypad and Frequencies

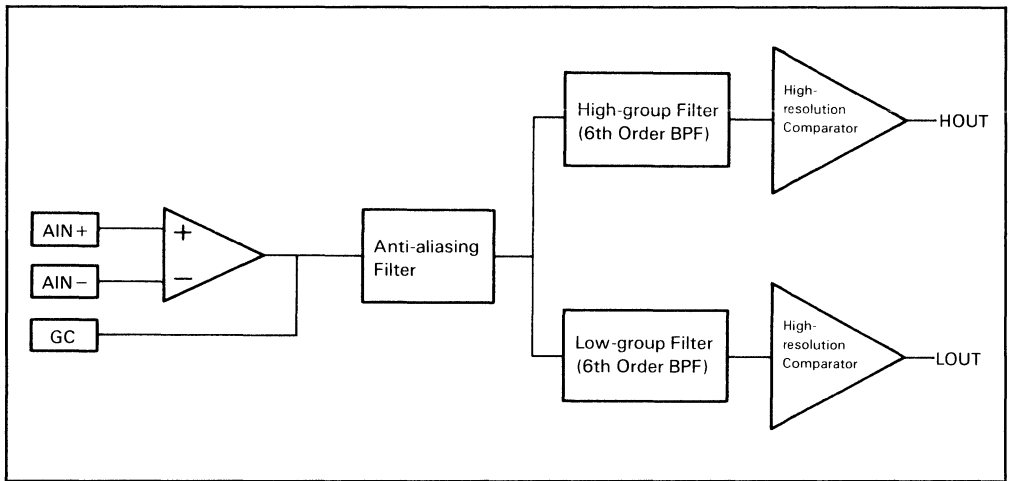


Figure 32. High-/Low- Group Isolation Circuit (Analog Block)

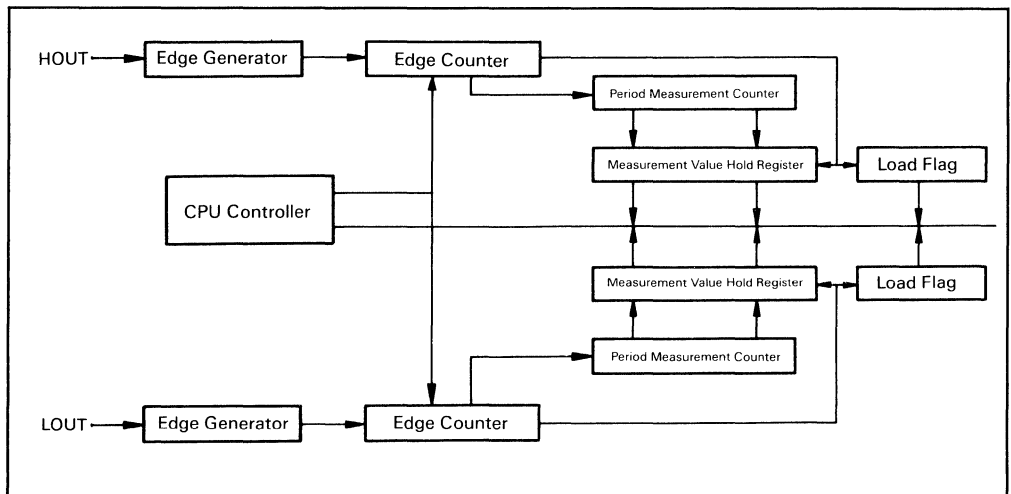


Figure 33. Frequency Measurement Circuit (Digital Block)

Tone Receiver Mode Register (Low-group (TRML): \$024, High-group (TRMH): \$028): TRM retains the number of cycles to be measured by the frequency measurement circuit, and the value to be counted is set in the edge counter.

The unit of the TRM value is a half cycle. In three-cycle measurement, \$6 is set in TRM. The frequency measurement circuit is initialized to measure the period of a signal by updating the value of TRM.

When TRM is \$0, the frequency measurement circuit stops. This mode is required when waiting for filter stabilization and when a signal is not being examined.

Tone Receiver control Register (TRC: \$02C): TRC consists of 4 bits as shown in Table 28.

TRON (bit 3)—Tone receiver enable bit. When this bit is set, an analog circuit and the period measure-

ment circuit become active. Signal examination must be performed after at least 100 ms from the time this bit is set, since several tens of milliseconds is required to stabilize the analog circuit.

HGLF (bit 2)—HGLF indicates that data has been loaded into the data register of the high-group frequency measurement unit. This bit can be reset but cannot be set by software.

LGLF (bit 1)—LGLF indicates that data has been loaded into the data register of the low-group frequency measurement unit. This bit can be reset but cannot be set by software.

When the load flag has been set, the value of the data register is not updated even if the edge counter becomes equal to TRM again. The load flag should be reset after the CPU performs the process described above.

Table 28. Tone Receiver Control Register

Bit	3	2	1	0
Function	TRON	HGLF	LGLF	Not Used

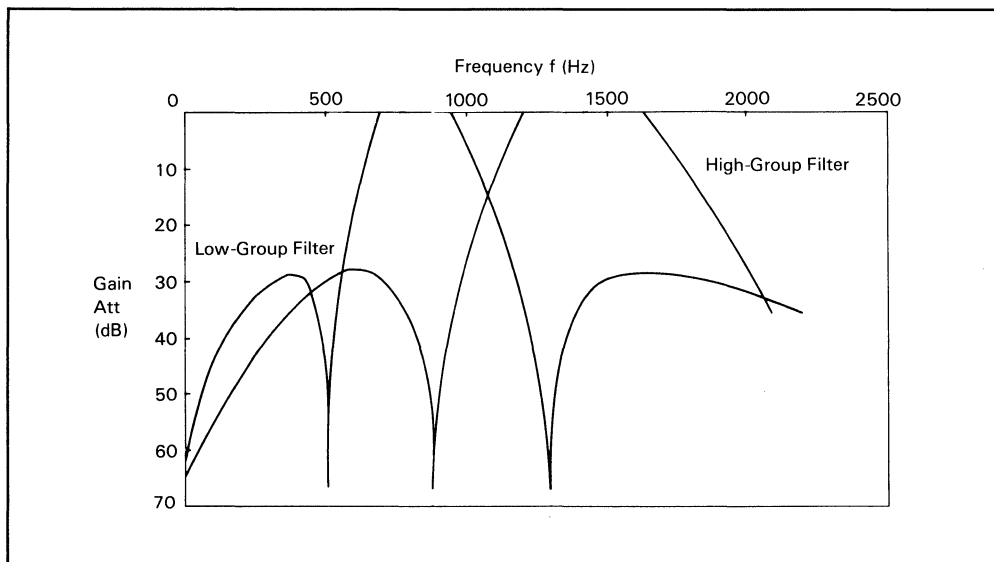


Figure 34. Frequency Characteristics of High-/Low- Group Isolation Circuit

Table 29. DTMF Receiver Registers

Register Name	Address	Bit	Function
TRML	\$024	0	Setting the number of measurement cycles of low-group frequency
		1	
		2	
		3	
TDLL	\$025	0	Low-group frequency period measurement data (Bits 0–3)
		1	
		2	
		3	
TDLM	\$026	0	Low-group frequency period measurement data (Bits 4–7)
		1	
		2	
		3	
TDLU	\$027	0	Low-group frequency period measurement data (Bits 8, 9)
		1	
		2	Not used
		3	
TRMH	\$028	0	Setting the number of measurement cycles of high-group frequency
		1	
		2	
		3	
TDHL	\$029	0	High-group frequency period measurement data (Bits 0–3)
		1	
		2	
		3	
TDHM	\$02A	0	High-group frequency period measurement data (Bits 4–7)
		1	
		2	
		3	
TDHU	\$02B	0	High-group frequency period measurement data (Bits 8, 9)
		1	
		2	Not used
		3	
TRC	\$02C	0	Not used
		1	Low-group measurement data load flag (1: Load end)
		2	High-group measurement data load flag (1: Load end)
		3	DTMF receiver enable (0: Disable, 1: Enable)

Addressing Modes

RAM Addressing Mode

The MCU has three RAM addressing modes as shown in Figure 35: register indirect addressing, direct addressing, and memory register addressing.

Register indirect addressing: The contents of registers W, X, and Y (10 bits) are used as RAM addresses.

Direct addressing: The direct addressing instruction consists of two words. The contents of the second

word (10 bits) following the opcode are used as a RAM address.

Memory register addressing: The memory register, 16 addresses from \$040 to \$04F, is accessed with the LAMR and XMRA instructions.

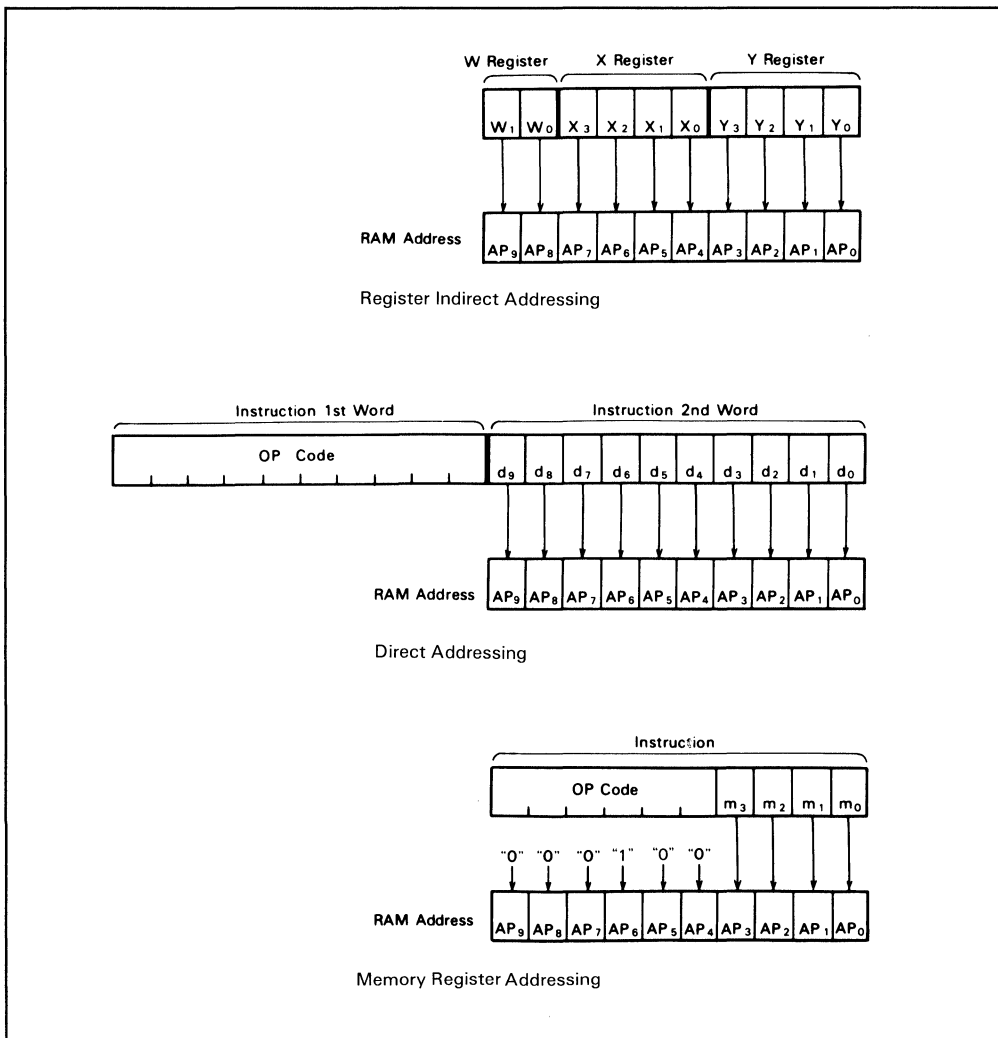


Figure 35. RAM Addressing Mode

ROM Addressing Mode and the P Instruction

The MCU has four ROM addressing modes, as shown in Figure 36.

Direct addressing mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14-bit program counter (PC13-PC0) with 14-bit immediate data.

Current page addressing mode: The MCU has 32 pages of ROM (256 words per page). By executing the BR instruction, the program can branch to any address in the current page. This instruction replaces the low eight bits of the program counter (PC7 to PC0) with 8-bit immediate data. When BR is on a page boundary ($256n + 255$) (Figure 38), executing the BR instruction transfers the PC contents to the next physical page. Consequently, the program branches to the next physical page when BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero page addressing mode: By executing the CAL instruction, the program can branch to the zero page

subroutine area located at \$0000-\$003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low six bits of the program counter (PC5-PC0), and 0s are placed in the high eight bits (PC13-PC6).

Table data addressing: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P instruction: ROM data addressed by table data addressing can be referenced with the P instruction (Figure 37). When bit 8 of the ROM data is 1, 8 bits of ROM data are written to the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written to the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data is written simultaneously into the accumulator and B register and also to the R1 and R2 port output registers. The P instruction has no effect on the program counter.

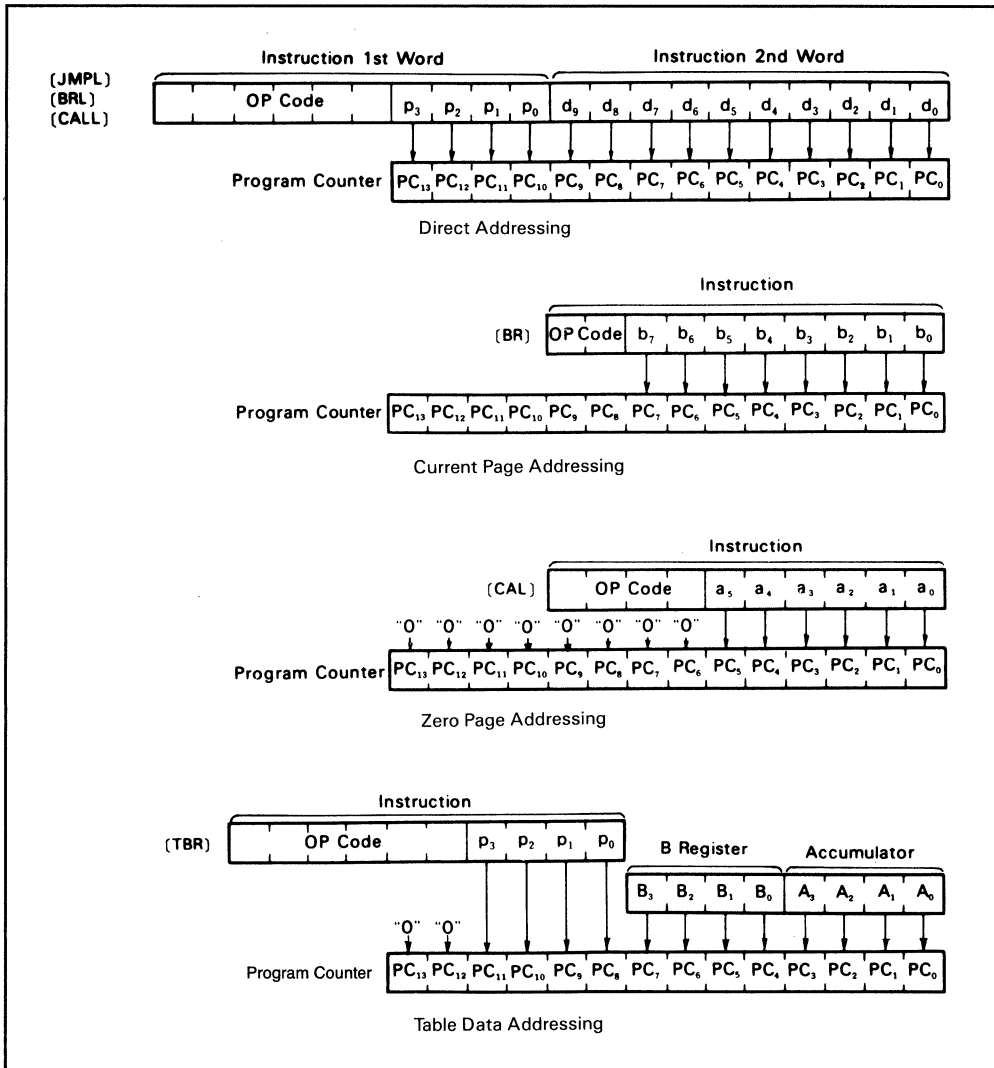


Figure 36. ROM Addressing Mode

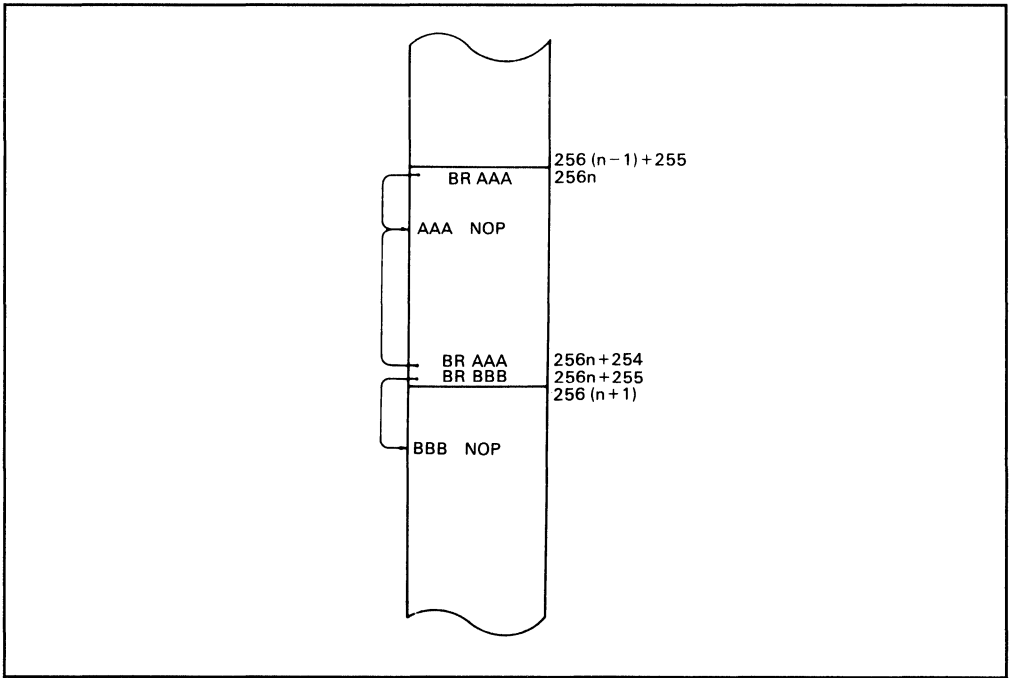


Figure 37. Branch Destination of BR Instruction on the Boundary between Pages

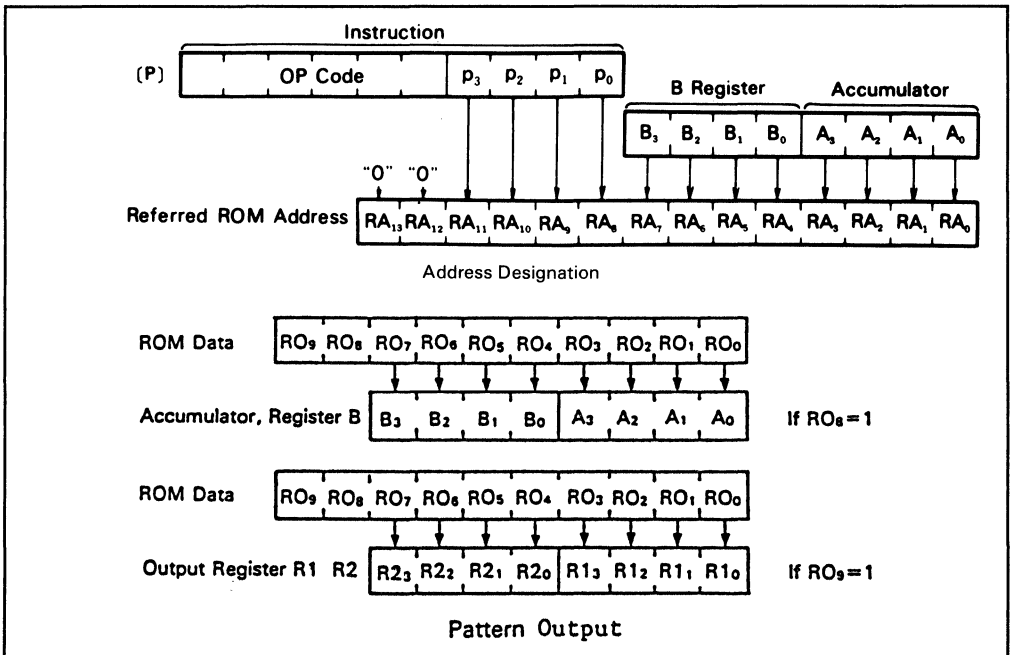


Figure 38. P Instruction



Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows:

1. Immediate instructions
2. Register-to-register instructions
3. RAM address instructions
4. RAM-register instructions
5. Arithmetic instructions
6. Compare instructions
7. RAM bit manipulation instructions
8. ROM address instructions
9. Input/output instructions
10. Control instructions

Tables 30–39 list their functions, and Table 40 is an opcode map.

Table 30. Immediate Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from Immediate	LAI i	1 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \rightarrow A$		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i_3 i_2 i_1 i_0	$i \rightarrow B$		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \rightarrow M$		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow M, Y+1 \rightarrow Y$	NZ	1/1

Table 31. Register-to-Register Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	$B \rightarrow A$		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	$A \rightarrow B$		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$W \rightarrow A$		2/2 See Note
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	$Y \rightarrow A$		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	$SPX \rightarrow A$		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	$SPY \rightarrow A$		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m_3 m_2 m_1 m_0	$MR(m) \rightarrow A$		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m_3 m_2 m_1 m_0	$MR(m) \leftrightarrow A$		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by assembler.

Table 32. RAM Address Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_1 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 See Note
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX,$ $Y \leftrightarrow SPY$		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by assembler.

Table 33. RAM-Register Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	$M \rightarrow A, \begin{pmatrix} X \leftrightarrow SPX \\ Y \leftrightarrow SPY \end{pmatrix}$		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₈ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 0 y x	$M \rightarrow B, \begin{pmatrix} X \leftrightarrow SPX \\ Y \leftrightarrow SPY \end{pmatrix}$		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	$A \rightarrow M, \begin{pmatrix} X \leftrightarrow SPX \\ Y \leftrightarrow SPY \end{pmatrix}$		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₈ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	$A \rightarrow M, Y+1 \rightarrow Y$ (X ↔ SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	$A \rightarrow M, Y-1 \rightarrow Y$ (X ↔ SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	$M \leftrightarrow A, \begin{pmatrix} X \leftrightarrow SPX \\ Y \leftrightarrow SPY \end{pmatrix}$		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₈ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	$M \leftrightarrow B, \begin{pmatrix} X \leftrightarrow SPX \\ Y \leftrightarrow SPY \end{pmatrix}$		1/1

Note: (XY) and (X) have the following meaning:

- The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below). The op-code X or Y is assembled as follows:

MNEMONIC	y	x	FUNCTION
LAM	0	0	
LAMX	0	1	X ↔ SPX
LAMY	1	0	Y ↔ SPY
LAMXY	1	1	X ↔ SPX, Y ↔ SPY

- The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY (X) is given below). The op-code X is assembled as follows:

MNEMONIC	x	FUNCTION
LMAIY	0	
LMAIYX	1	X ↔ SPX

Table 34. Arithmetic Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-CA \rightarrow A$ NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	$M-A-CA \rightarrow A$ NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₃ d ₂ d ₁ d ₀ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩: Logic AND
 ∪: Logical OR
 ⊕: Exclusive OR

Table 35. Compare Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \neq M$	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \neq M$	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	$A \neq M$	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \neq M$	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	$B \neq M$	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	$Y \neq i$	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \leq M$	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \leq M$	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	$A \leq M$	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \leq M$	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	$B \leq M$	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	$A \leq i$	NB	1/1

Table 36. RAM Bit Manipulation Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD / CYCLE
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	$1 \rightarrow M(n)$		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$1 \rightarrow M(n)$		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 0 1 0 n_1 n_0	$0 \rightarrow M(n)$		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 0 1 0 n_1 n_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$0 \rightarrow M(n)$		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 0 1 1 n_1 n_0		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 0 1 1 n_1 n_0 d_6 d_5 d_4 d_3 d_2 d_1 d_0		M(n)	2/2

Table 37. ROM Address Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₃ d ₂ d ₁ d ₀ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	¹ CA · I/E	ST	1/3

Table 38. Input/Output Instructions




OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D (Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D (m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D (Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D (m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D (Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D (m)	1/1
Load A from R-Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R (m) → A		1/1
Load B from R-Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R (m) → B		1/1
Load R-Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R (m)		1/1
Load R-Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R (m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 39. Control Instructions

OPERATION	MNEMONIC	OPERATION CODE	FUNCTION	STATUS	WORD CYCLE
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Stand-by Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Table 40. Opcode Map

R8		O																1																		
R9	H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F			
		0	NOP	XSPX	XSPY	XSPXY	ANEM	/	/	/	/	AM	/	/	/	/	/	/	LAW	/	/	/	/	ANE TMD	/	/	/	/	AMD	/	/	/	OFMD			
1	RTN	RTNI	/	/	ALEM	/	/	/	/	AMC	/	/	/	/	/	/	LWA	/	/	/	/	ALE TMD	/	/	/	/	AMCD	/	/	/	EOFM TMD					
2	/	/	/	/	INEM i(4)								/	/	/	/	/	/	/	INEMD i(4)																
3	/	/	/	/	ILEM i(4)								/	/	/	/	/	/	/	/	ILEMD i(4)															
4	LBM(XY)	/	/	BNEM	/	/	/	/	LAB	/	/	/	/	IB	/	/	COMB	/	/	/	/	OR	/	/	/	STS	/	/	/	SBY STOP						
5	LMAI(X)	/	/	AYY	/	/	/	/	LASPY	/	/	/	/	IY	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	JMPL p(4)					
6	NEGA	/	/	RED	/	/	/	/	LASPK	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	CALL p(4)					
7	/	/	/	/	YNEI i(4)								/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	BRL p(4)			
8	XMA(XY)	/	/	SEM n(2)				/	/	/	REM n(2)				/	/	/	/	XMAD	/	/	/	/	SEMD n(2)				/	/	/	/	REMD n(2)				TMD n(2)
9	LAM(XY)	/	/	LMA(XY)				/	/	/	SMC	/	/	/	ANM	/	/	LAMD	/	/	/	/	LMAD	/	/	/	SMCD	/	/	/	/	ANMD				
A	ROTR	ROTL	/	/	DAA				/	/	/	DAS				/	/	/	LAY	/	/	/	/	LMID i(4)				/	/	/	/	/	/			
B	/	/	/	/	TBR p(4)								/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	P p(4)		
C	XMB(XY)	/	/	BLEM	/	/	/	/	LBA	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	DB					
D	LMADY(X)	/	/	SYI	/	/	/	/	LYA	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	DY					
E	TD	/	/	SED	/	/	/	/	LXA	/	/	/	/	REC	/	/	SEC	/	/	/	/	CAL				/	/	/	/	/	/	a(6)				
F	LWI	i(2)																/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/		
0	/	/	/	/	LBI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
1	/	/	/	/	LYI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
2	/	/	/	/	LXI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
3	/	/	/	/	LAI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
4	/	/	/	/	LBR m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
5	/	/	/	/	LAR m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
6	/	/	/	/	REDD m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
7	/	/	/	/	LAMR m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
8	/	/	/	/	AI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	BR				/	/	/	/	/	b(8)				
9	/	/	/	/	LMIIY i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
A	/	/	/	/	TDD m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
B	/	/	/	/	ALEI i(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
C	/	/	/	/	LRB m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
D	/	/	/	/	LRA m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
E	/	/	/	/	SEDD m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					
F	/	/	/	/	XMRA m(4)				/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/					

 ... 1-word/2-cycle Instruction
  ... 1-word/3-cycle Instruction
  ... RAM Direct Address Instruction
  ... 2-word/2-cycle Instruction (2-word/2-cycle)



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Total Allowance of Input Current	ΣI_O	105	mA	2
Total Allowance of Output Current	$-\Sigma I_O$	60	mA	3
Maximum Input Current	I_O	4	mA	4, 5
		30	mA	4, 6
Maximum Output Current	$-I_O$	4	mA	7, 8
		20	mA	7, 9
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	

- Notes:
1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 3. Total allowance of output current is the sum of output current which flows out from V_{CC} to all I/O pins simultaneously.
 4. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 5. D₁₀-D₁₅, R₀-R₇.
 6. D₀-D₉
 7. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 8. D₀-D₉, R₀-R₇.
 9. D₁₀-D₁₅

Electrical Characteristics

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20\text{ to }+75\text{ }^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	RESET	$0.85 V_{CC}$		$V_{CC} + 0.3$	V		
		INT0, INT1 INT2, INT3 SCKA, SCKB	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		SIA, SIB	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC1	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V	External Clock Operation	
Input Low Voltage	V_{IL}	RESET	-0.3		$0.15 V_{CC}$	V		
		INT0, INT1 INT2, INT3 SCKA, SCKB	-0.3		$0.2 V_{CC}$	V		
		SIA, SIB	-0.3		$0.2 V_{CC}$	V		
		OSC1	-0.3		0.5	V	External Clock Operation	
Output High Voltage	V_{OH}	SCKA, SOA SCKB, SOB TOB, TOC TOD1, TOD2	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{ mA}$	
Output Low Voltage	V_{OL}	SCKA, SOA SCKB, SOB TOB, TOC TOD1, TOD2			0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, OSC1 INT0, INT1 INT2, INT3 SCKA, SIA SCKB, SIB			1	μA	$V_{in} = 0\text{V to }V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			5	mA	$V_{CC} = 5\text{V}$, $f_{osc} = 4\text{ MHz}$ DTMF receiver and analog comparator stop	2
	I_{CCA}	V_{CC}			20	mA	$V_{CC} = 5\text{V}$, $f_{osc} = 4\text{ MHz}$ DTMF receiver operates	3
	I_{CCB}	V_{CC}			7	mA	$V_{CC} = 5\text{V}$, $f_{osc} = 4\text{ MHz}$ Analog comparator operates	4
Current dissipation in standby mode	I_{SBY1}	V_{CC}			3.5	mA	$V_{CC} = 5\text{V}$, $f_{osc} = 4\text{ MHz}$ maximum logic operation	5
	I_{SBY2}	V_{CC}			3	mA	$V_{CC} = 5\text{V}$, $f_{osc} = 4\text{ MHz}$ minimum logic operation	
Current dissipation in stop mode	I_{STOP}	V_{CC}			10	μA	$V_{CC} = 5\text{V}$	6
Stop mode retain voltage	V_{STOP}		2.0			V		7

- Notes:
- Output buffer current is excluded.
 - The MCU is in the reset state. Input/output current does not flow.
Test conditions: MCU: Reset
Pin: RESET, TEST – V_{CC}
 - DTMF signal receive mode. Input/output current does not flow.
 - Analog comparator operates and input/output current does not flow.
 - The timer operates with the fastest clock and input/output current does not flow.
Test conditions: MCU: Standby mode
Input/output – Reset state
Serial interface – Stop
Timer – Prescaler divide ratio is –2
Pin: RESET – GND
TEST – V_{CC}
 - Input/output current does not flow.
Test conditions: MCU: Stop Mode
Pin: RESET – GND
TEST – V_{CC}
 - RAM data is retained.

Input/Output Characteristics for Standard Pin
(V_{CC} = 5 V ± 10%, GND = 0 V, T_a = –20 to +75 °C, unless otherwise noted)

Item	Symbol	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input High Voltage	V _{IH}	R0–R8	0.7 V _{CC}		V _{CC} + 0.3	V		
Input Low Voltage	V _{IL}	R0–R8	–0.3		0.3 V _{CC}	V		
Output High Voltage	V _{OH}	R0–R7	V _{CC} – 1.0			V	–I _{OH} = 1.0 mA	
Output Low Voltage	V _{OL}	R0–R7			0.4	V	–I _{OL} = 1.6 mA	
Input/Output Leakage Current	I _{IL}	R0–R8			1	μA	V _{in} = 0V to V _{CC}	1
Input High/Low Voltage	$\frac{VR_{INH}}{VR_{INL}}$	R82 (variable voltage reset mode)	VR _{ref} + 0.1		VR _{ref} – 0.1	V		
Analog Input Reference Voltage Range	VR _{ref}	R83	0		V _{CC} – 1.2	V		
Pull-Up MOS Current	–I _{pu}	R0–R5	20	100	200	μA	V _{CC} = 5.0V, V _{in} = 0V	
Pull-Down MOS Current	I _{pd}	R6–R8	20	100	200	μA	V _{CC} = 5.0V, V _{in} = 5.0V	

Note 1: Output buffer current is excluded.

Input/Output Characteristics for Large-Current Pins
($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20\text{ to } +75\text{ }^\circ\text{C}$)

Item	Symbol	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D0-D15	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D0-D15	-0.3		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D10-D15	2.0			V	$-I_{OH} = 10\text{ mA}$	
		D0-D15	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{ mA}$	
Output Low Voltage	V_{OL}	D0-D9		2.0		V	$I_{OL} = 15\text{ mA}$	
		D0-D15		0.4		V	$I_{OL} = 1.6\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	D0-D15			1	μA	$V_{in} = 0\text{V to } V_{CC}$	1
Full-Up MOS Current	$-I_{pu}$	D0-D9	20	100	200	μA	$V_{CC} = 5.0\text{V}$, $V_{in} = 0\text{V}$	
Full-Down MOS Current	I_{pd}	D10-D15	20	100	200	μA	$V_{CC} = 5.0\text{V}$, $V_{in} = 5.0\text{V}$	

Note 1: Output buffer current is excluded.

AC Characteristics**(V_{CC} = 5 V ± 10%, GND = 0 V, T_a = -20°C to +75°C, unless otherwise noted)**

Items	Symbol	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions	Note
Crystal or Ceramic Filter Oscillator	Oscillation Frequency	f _{OSC}	OSC ₁ , OSC ₂	1	4	4.5	MHz	
	Instruction Cycle Time	t _{CYC}		1.78	2	8	μs	
	Oscillator Stabilization Time	t _{RC}	OSC ₁ , OSC ₂			20	ms	1
External Clock Operation	External Clock Frequency	f _{CP}	OSC ₁	1	4	4.5	MHz	2
	External Clock High Level Width	t _{CPH}	OSC ₁	82			ns	2
	External Clock Low Level Width	t _{CPL}	OSC ₁	82			ns	2
	External Clock Rise Time	t _{CPr}	OSC ₁			20	ns	2
	External Clock Fall Time	t _{CPf}	OSC ₁			20	ns	2
	Instruction Cycle Time	t _{CYC}		1.78	2	8	μs	2
External Interrupt Signal High Level Width	t _{IH}	INT ₀ , INT ₁ INT ₂ , INT ₃	2				t _{cyc}	3
External Interrupt Signal Low Level Width	t _{IH}	INT ₀ , INT ₁ INT ₂ , INT ₃	2				t _{cyc}	3
RESET High Level Width	t _{RSTH}	RESET	3				t _{cyc}	4
Input Capacitance	C _{in}				15	pF	f = 1 MHz, V _{in} = 0V	
RESET Fall Time	t _{RSTf}				20	ms		4
Analog Comparator Stabilization Time	t _{CSTB}	R82 (variable voltage reset mode)			2		t _{cyc}	5
DTMF Received Filter Stabilization Time	t _{DTMFR}	DTMF receive mode	—	—	120	ms		6

Notes: 1. Oscillator stabilization time is the time until oscillator stabilizes after V_{CC} reaches 4.5 V at power-on, or after RESET input goes high after cancelling stop mode. At power-on and during stop mode, RESET input must be applied for at least t_{RC} to ensure oscillation stabilization time. When using crystal oscillator, please contact oscillator marker since oscillation stabilization time depends on the circuit constant and stray capacitance.

2. See Figure 40.

3. See Figure 41.

4. See Figure 42.

5. t_{CSTB} is the time until the analog comparator stabilizes after R8₂ enters variable voltage reset mode.

6. t_{DTMFR} is the time until the filter and comparator stabilize to read correct data after the DTMFR enable bit is set to "1".

Serial Interface Timing Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise noted)

At Transfer Clock Output

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min.	Typ.	Max.			
Transfer Clock Cycle Time	t_{Scyc}	SCKA, SCKB	1			t_{cyc}	Fig. 44	1, 2
Transfer Clock High Level Width	t_{SCKH}	SCKA, SCKB	0.5			t_{Scyc}	Fig. 44	1, 2
Transfer Clock Low Level Width	t_{SCKL}	SCKA, SCKB	0.5			t_{Scyc}	Fig. 44	1, 2
Transfer Clock Rise Time	t_{SCKr}	SCKA, SCKB			100	ns	Fig. 44	1, 2
Transfer Clock Fall Time	t_{SCKf}	SCKA, SCKB			100	ns	Fig. 44	1, 2
Serial Output Data Delay Time	t_{DSO}	SOA, SOB			250	ns	Fig. 44	1, 2
Serial Input Data Set-up Time	t_{SSI}	SIA, SIB	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SIA, SIB	150			ns		1

At Transfer Clock Input

Item	Symbol	Pin Name	Value			Unit	Test Conditions	Note
			Min.	Typ.	Max.			
Transfer Clock Cycle Time	t_{Scyc}	SCKA, SCKB	1			t_{cyc}		1
Transfer Clock High Level Width	t_{SCKH}	SCKA, SCKB	0.5			t_{Scyc}		1
Transfer Clock Low Level Width	t_{SCKL}	SCKA, SCKB	0.5			t_{Scyc}		1
Transfer Clock Rise Time	t_{SCKr}	SCKA, SCKB			100	ns		1
Transfer Clock Fall Time	t_{SCKf}	SCKA, SCKB			100	ns		1
Serial Output Data Delay Time	t_{DSO}	SOA, SOB			250	ns	Fig. 44	1, 2
Serial Input Data Set-up Time	t_{SSI}	SIA, SIB	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SIA, SIB	150			ns		1
Transfer Clock End Detection Time	t_{SCKHD}	SCKA, SCKB	1			t_{cyc}		1, 2, 3

- Notes: 1. See Figure 43.
 2. See Figure 44.
 3. Transfer Clock Completion Detect Time is the period of high level after 8 pulses of transfer clock are input. SCI interrupt request flag is not set when the next transfer clock is input before completion detect time has passed.

DTMF Receiver Characteristics

($V_{CC} = 5\text{ V}$, $GND = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $f_{osc} = 4.00\text{ MHz}$)

Item		Min.	Typ.	Max.	Unit	Test Condition	Unit	Note
Dynamic Range	Valid Input Signal Levels (each composite signal tone)	-29.0	-	+1.0	dBm			1, 2, 5
	Noise Tolerance	-	-16	-	dB			1, 3, 5
	Hum Tolerance	-	+20	-	dB			1, 5
	Dial Tone Tolerance	-	0	-	dB			1, 5
Twist	Positive/Negative Twist Accept	-	± 10	-	dB			1, 5
Accuracy	Frequency Deviation Accept	-	± 1.8	-	%			1, 5
	Frequency Deviation Reject	-	± 3.5	-	%			1, 5
Speech Immunity		-	2	-	No. of Times			1, 4, 5

- Notes: 1. Receiver characteristics are tested at the factory using a special program.
 2. Reference power of 1 mW into a 600 Ω load.
 3. Total distortion is 300 Hz to 3.4 KHz.
 4. MITEL standard tape is used.
 5. Use Figure 45.



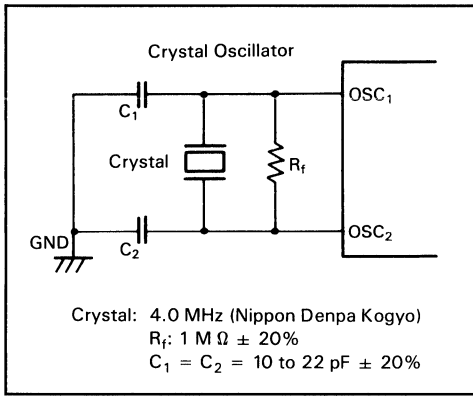


Figure 39. Oscillation Circuit

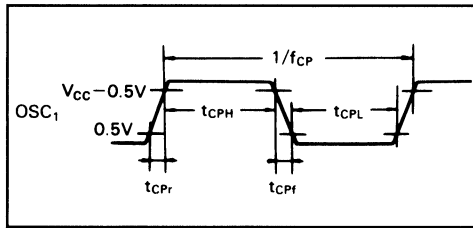


Figure 40. External Clock Timing

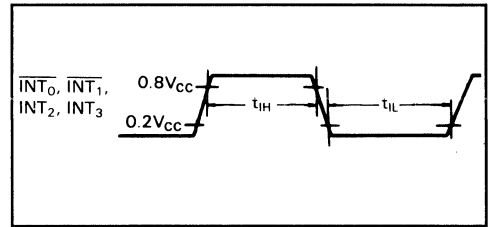


Figure 41. Interrupt and Timer Input Timing

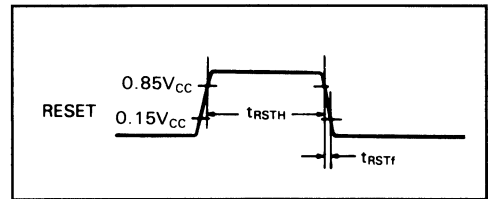


Figure 42. Reset Timing

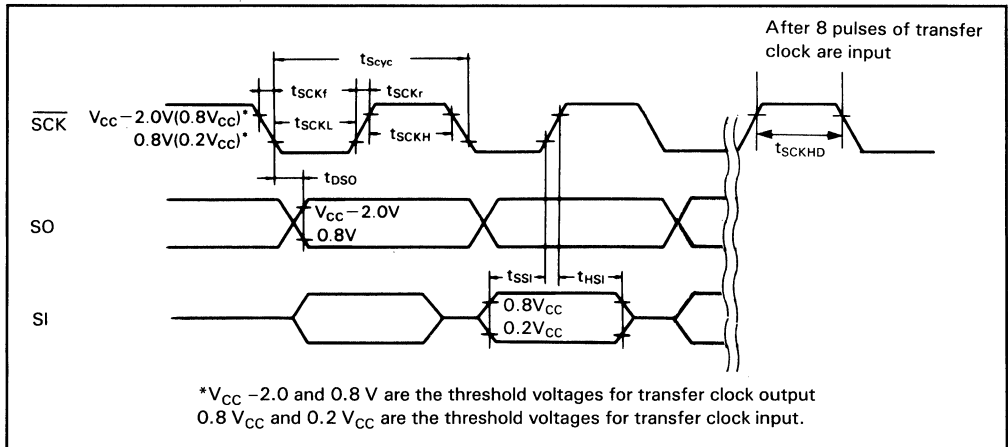


Figure 43. Timing Diagram of Serial Interface

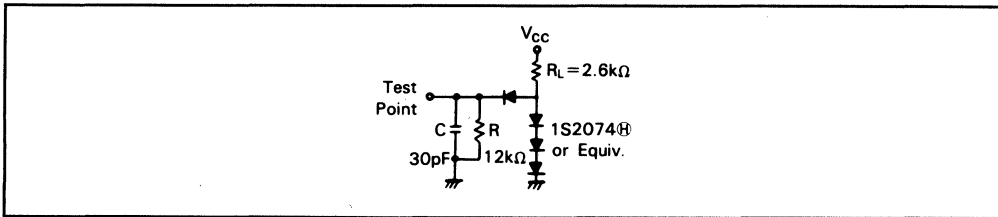


Figure 44. Timing Load Circuit

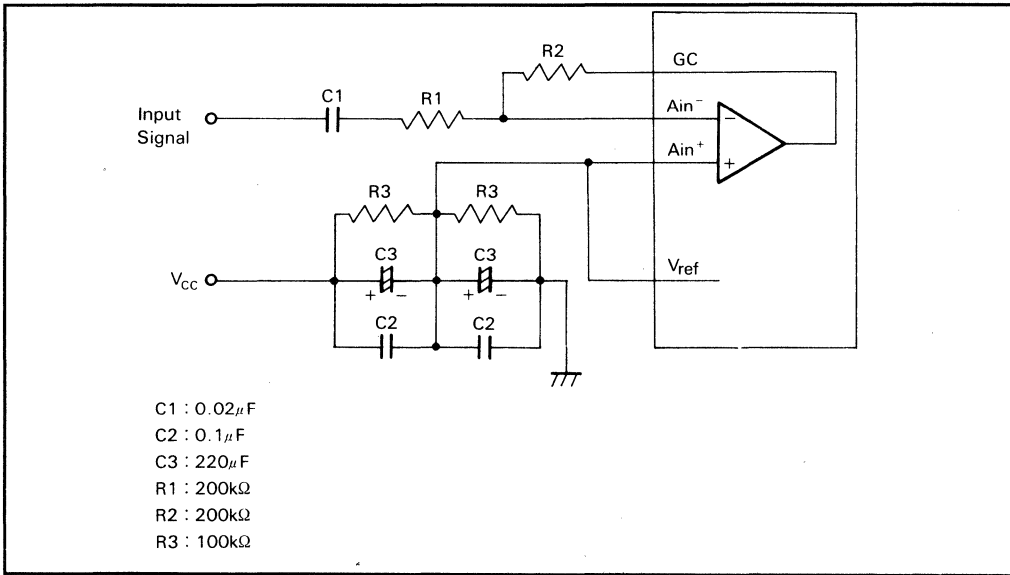
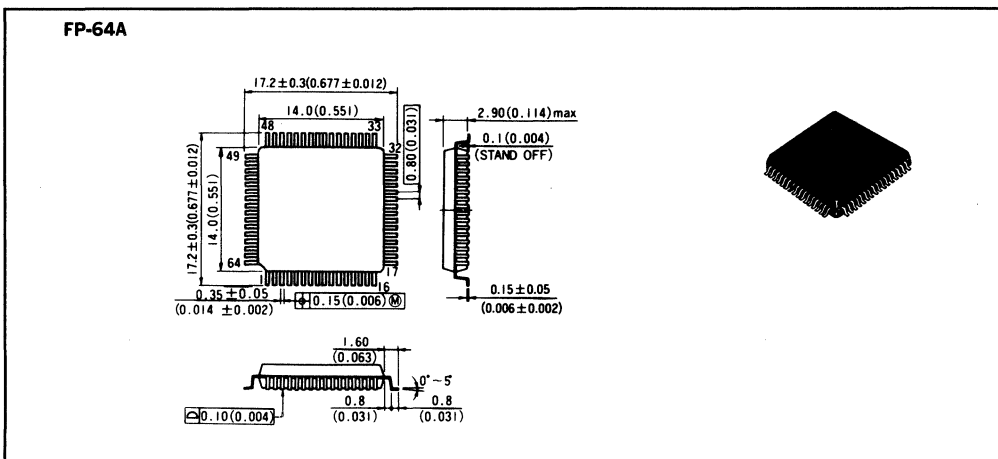


Figure 45. DTMF Receiver Measurement Circuit

Package Dimensions

Unit: mm (inch)



HD404678 OPTION LIST

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number	

(1) Package

Package
<input checked="" type="checkbox"/> FP-64A

(2) ROM Code Media

ROM Code Media
<input checked="" type="checkbox"/> EPROM On-Package Microcomputer Type

Application Check List

(3) Oscillator

<input type="checkbox"/> 4MHz Crystal
<input type="checkbox"/> 4MHz External Clock

*Please enter check marks (■, X, ✓) in applicable item



HD404708/HD404709/ HD4074709

Description

The MCU are 4-bit single-chip HMCS400 series microcomputers providing high programming productivity. They incorporate high-voltage I/O pins, a Vacuum Fluorescent Display (VFD) controller/driver, a pulse width modulation output circuit, and a 32.768 kHz oscillator used for the precise watch.

Features

- 8192 words × 10 bits ROM (HD404708)
16384 words × 10 bits ROM (HD404709)
16384 words × 10 bits PROM (HD4074709)
(The PROM is compatible with the 27256 type.)
- 576 digits × 4 bits RAM
- 56 I/O pins including 32 high-voltage (max. 40V), high current (max. 15mA) pins.
- Three on-chip timer/counters
- Clock synchronous 8-bit serial interface
- 14 bit PWM D/A converter
- Four external (including two double-edged) and five internal interrupt sources
- Subroutine stack which allows up to 16 levels including interrupts
- Three low power dissipation modes: Standby mode, Watch mode, Stop mode
- Two builtin oscillators: System/subsystem oscillator
- Instruction cycle time: $0.89\mu\text{s}$ ($V_{CC} = 3.5-6\text{V}$)
- Modes: MCU mode
PROM mode (HD4074709)

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Type of Products

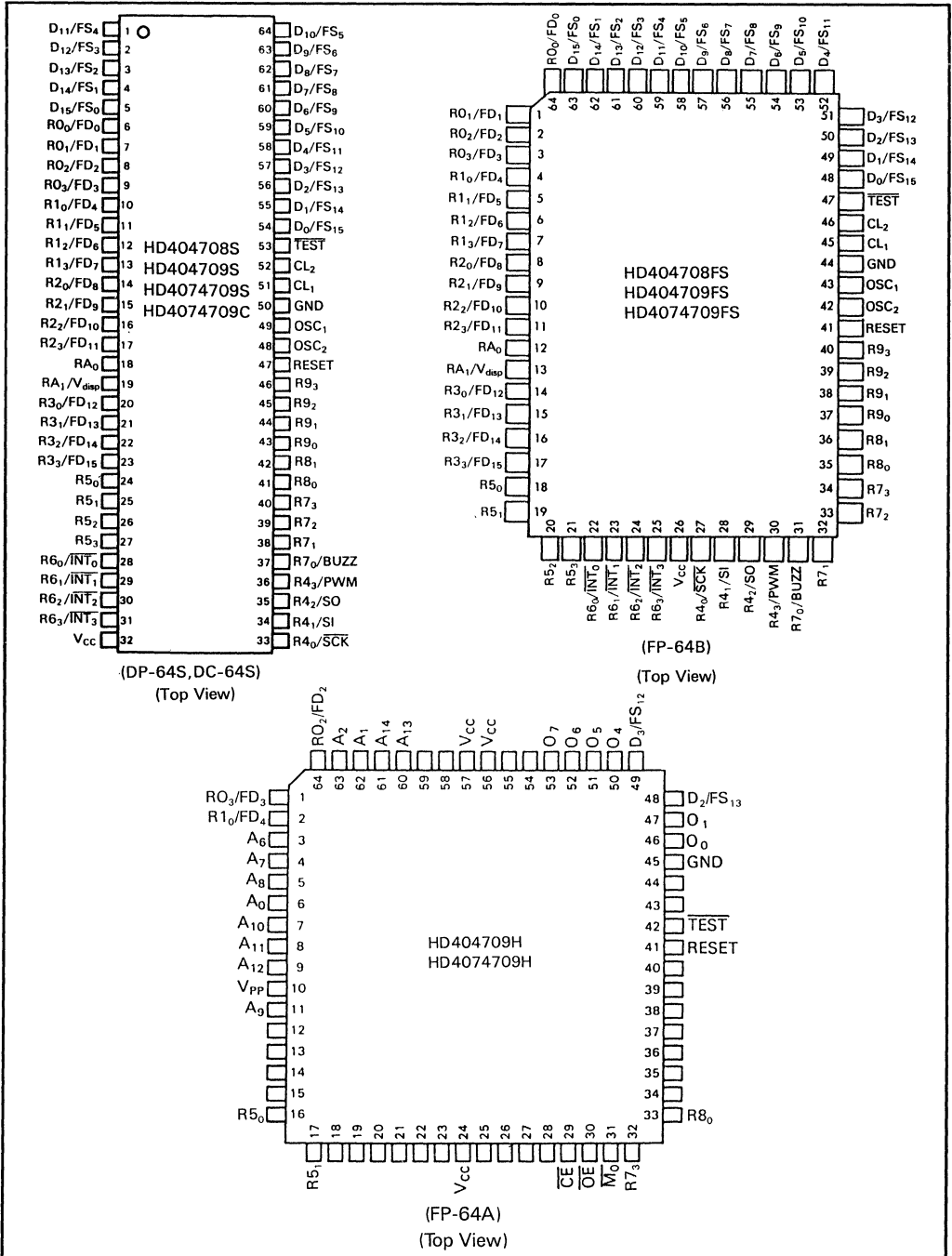
Mask ROM type (* * * : ROM code)

Part No.	ROM (Words)	Package
HD404708***S	8192	DP-64S
HD404708***FS		FP-64B
HD404709***S	16384	DP-64S
HD404709***FS		FP-64B
HD404709***H		FP-64A

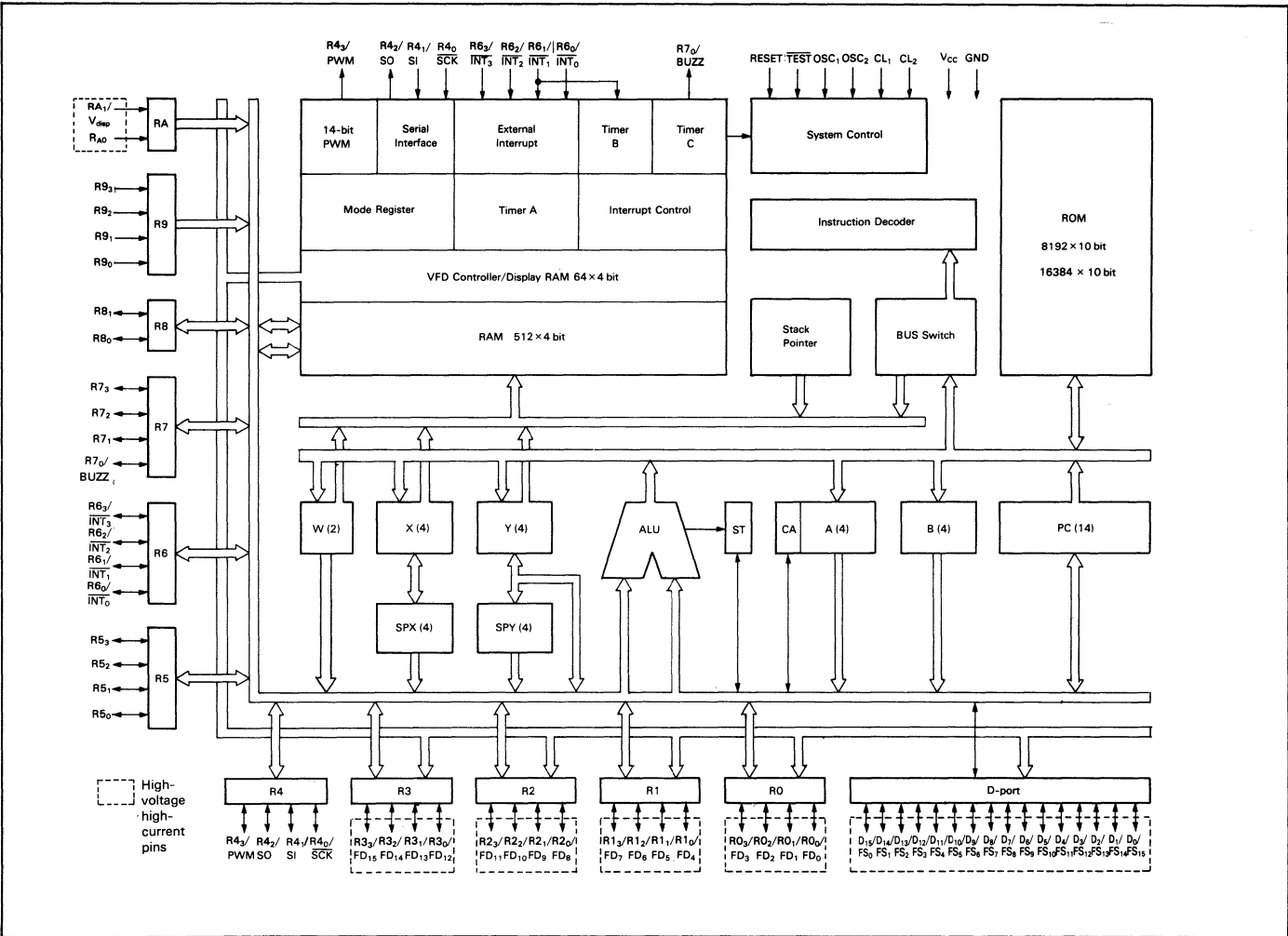
ZTAT type

Part No.	ROM (Words)	Package
HD4074709S	16384	DP-64S
HD4074709FS		FP-64B
HD4074709C		DC-64S
HD4074709H		FP-64A

Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC} (Power)

These are the power supply pins for the MCU. Connect the GND to the ground (0V) and apply the V_{CC} power supply voltage to V_{CC}.

TEST

TEST is used for test purposes only. TEST must be connected to V_{CC}.

RESET

RESET resets the MCU.

OSC₁, OSC₂

OSC₁ and OSC₂ are input and output pin for the internal oscillator circuit. They can be connected to a crystal resonator, a ceramic filter resonator. In the case of an external oscillator circuit, an external clock signal is connected to OSC₁ and OSC₂ is open.

CL₁, CL₂

These pins are input pins for the 32.768 kHz crystal oscillator used for the precise watch.

D₀ – D₁₅ (D Ports)

The D ports are input/output ports addressed by bit. Each port output consists of an open-drain PMOS, which realizes high-voltage and high drive current capability on these port pins. These pins are multiplexed with the segment pins used for the VFD controller.

R₀ – R_A (R Ports)

The R ports are 4-bit ports, except for R₈ and R_A which are addressed by 2 bits. R₉ and R_A are input ports and R₀ to R₈ are input/output

ports. While R₄ to R₉ port pins are standard pins, R₀ to R₃ and R_A pins are high-voltage pins. Each R₀ to R₃ output consists of an open-drain PMOS which realizes high-voltage and high drive current capability on these port pins. These pins are multiplexed with the digit pins for the VFD controller. Port pins R₄ to R₃, R₆ to R₆ and R₇ are multiplexed with peripheral pins.

INT₀, INT₁, INT₂, INT₃ (Interrupts)

These signals externally interrupt the MCU. INT₁ can be also used as an external event input for timer B. INT₀ to INT₃ are multiplexed with R₆ to R₆, respectively.

SCK, SI, SO (Serial Communications Interface)

The MCU is provided with a clock input/output (SCK), receive data input (SI), and transmit data output (SO) for a serial communications interface. SCK, SI and SO are multiplexed with R₄ to R₄, respectively.

BUZZ (Timer Output)

This pin outputs a variable-duty square wave. It is multiplexed with R₇.

FD₀ – FD₁₅, FS₀ – FS₁₅ (VFD Controller)

FD₀ to FD₁₅ are the digit pins for the VFD (Vacuum Fluorescent Display) controller. They are multiplexed with port pins R₀ to R₃. FS₀ to FS₁₅ are the segment pins for the VFD controller. They are multiplexed with the D port pins.

PWM (PWM D/A Converter)

This pin output a square wave from the PWM D/A converter. It is multiplexed with pin R₄.

Functional Description

ROM Memory Map

The following paragraphs describe the ROM in detail. Figure 1 shows the ROM memory map.

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for the JMWL instruction which results in a branch to the starting address of the reset routine and the starting address of the interrupt service routine. After reset or interrupt execution, the program starts from the vector address.

Zero-page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines to which the CAL instruction branches the program.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data which can be referred to as a pattern by the P instruction.

Program Area (\$0000 to \$1FFF : HD404708, \$0000 to \$3FFF : HD404709/HD4074709): Locations \$0000 through \$1FFF, \$3FFF can be used for the program code.

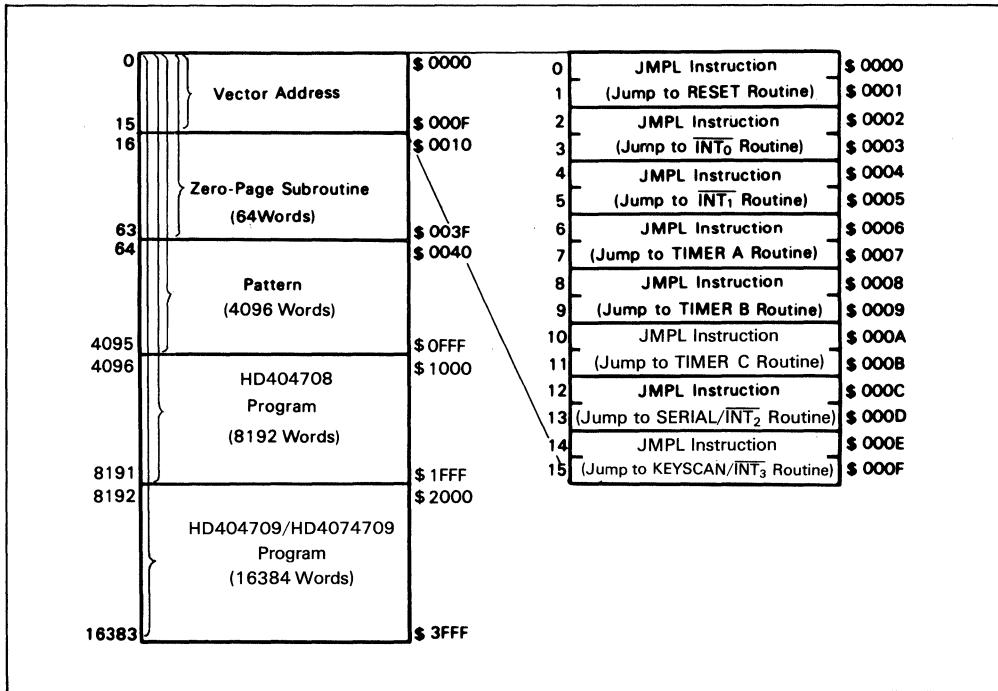


Figure 1. ROM Memory Map

RAM Memory Map

The MCU contains 512 digits of 4-bit RAM for the data and stack areas. In addition to these areas, interrupt control bits, special function registers and a VFD data area are also mapped on the RAM. The following paragraphs describe the RAM in detail. Figure 2 shows the RAM memory map.

Interrupt Control Bit Area (\$000 to \$003, \$020 to \$023): This area is used for interrupt control. Figure 3 shows this area. It can be accessed only by the RAM bit manipulation instructions.

The interrupt request flag cannot be set by software. The RSP bit resets only the stack pointer. The state of the LSON flag depends on the low power mode. The WDON flag is affected by the SEM and SEMD instructions only.

Special Function Registers Area (\$004 to \$01F, \$024 to \$03F): This area consists of mode or data registers for external interrupts, the serial interface, the timer/counter, and data control registers for all I/O ports. There are three types of the registers: read-only, write-only and read/write. These registers cannot be affected by the RAM bit manipu-

lation instructions.

VFD Data Area (\$060 to \$09F): This area stores the data to be displayed on the VFD. This data automatically appears in the VFD segment. Data "1" indicates the segment is ON and "0" indicates OFF. Also, this area is available as a data area.

Data Area (\$040 to \$04F, \$0A0 to \$24F): Location \$040 through \$04F, the memory registers (MR), can be also accessed by the LAMR and XMRA instructions. Figure 4 shows memory register area.

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for the stack area to save the contents of the program counter (PC), the status flag (ST) and the carry flag (CA) during subroutine calls (the CAL and CALL instructions) or during interrupt servicing. One level of subroutine requires four digits, which allows the programmer to use up to 16 levels of subroutines. Figure 4 shows the stack area and saved data. The program counter is popped off the stack by the RTN and RTNI instructions, while the status and carry flags are popped off the stack only by the RTNI instruction. The unused area is available as a data area.

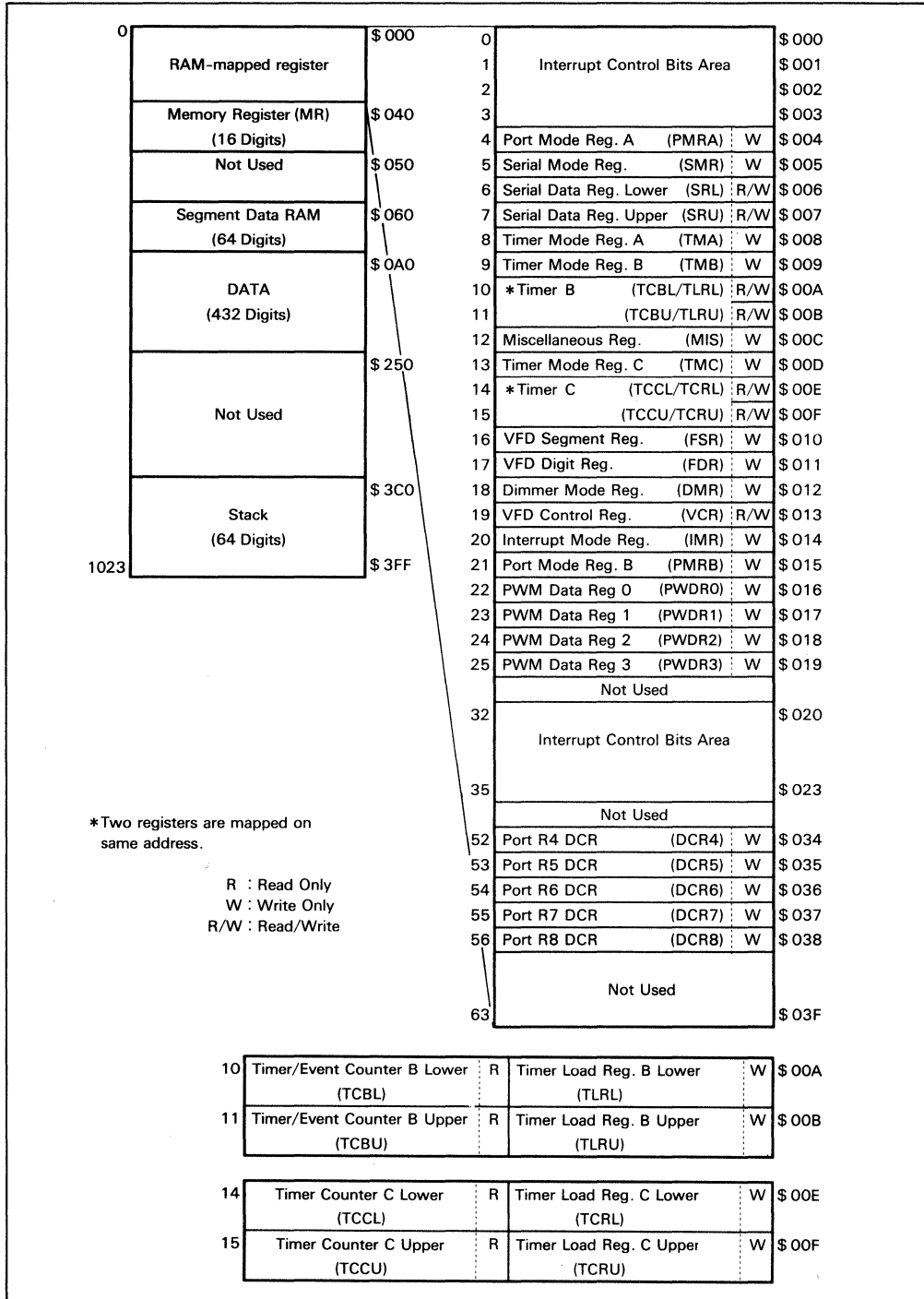


Figure 2. RAM Memory Map



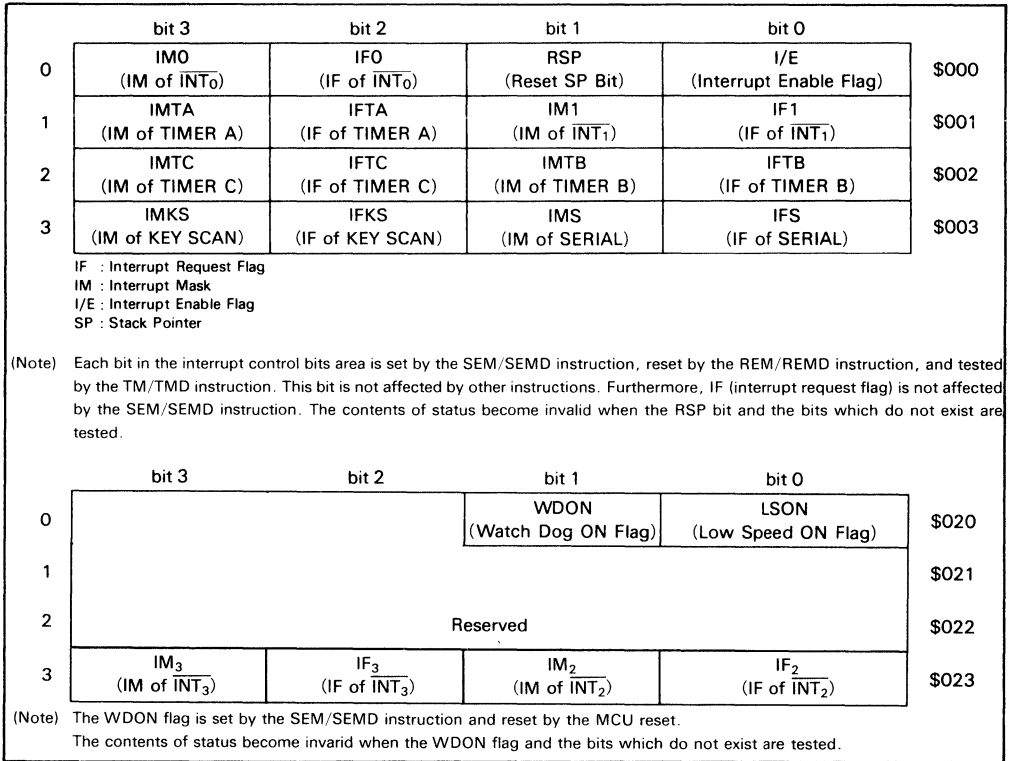


Figure 3. Interrupt Control Bits Area and Register Flag Area

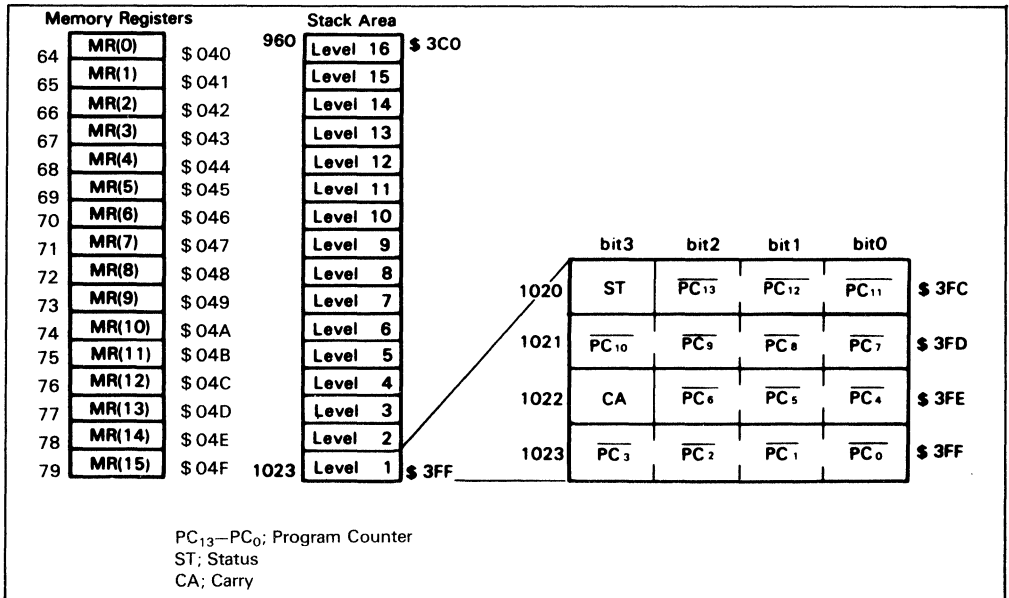


Figure 4. Memory Register, Stack Area and Stack Position

Register and Flags

The MCU has nine registers and two flags for CPU operation. The following paragraphs describe the registers and flags in detail. Figure 5 shows these registers and flags.

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the Arithmetic Logic Unit (ALU) as well as transfer data between memories, I/O and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry (CA): The carry flag (CA) indicates an overflow resulting from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL and ROTR instructions. The content of the carry flag is pushed onto the stack during interrupt servicing, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions and the result of the bit test instruction. Moreover, the status flag controls branches caused by the BR, BRL, CAL or CALL instructions. Whether these instructions are executed or skipped, the status flag is set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, and branch instruction is executed. During interrupt servicing, the content of the status is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which holds the ROM address.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to \$3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit is reset by the REM or REMD instructions.

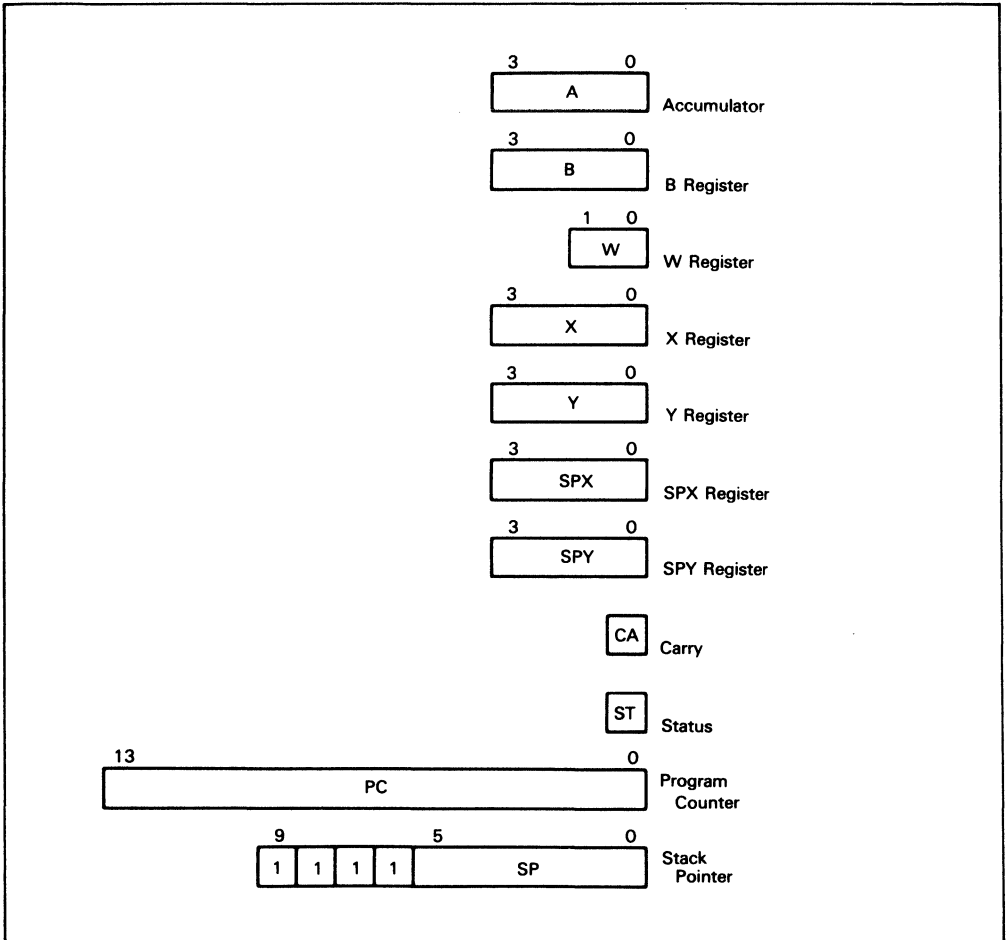


Figure 5. Registers and Flags

Reset

The MCU is reset by setting the RESET pin to high level. At power-on or releasing the system oscillator from stop state, the RESET input must be applied for t_{RC} or for a longer period in order to stabilize the oscillator. In other cases, the RESET input for two instruction cycles resets the MCU. Table 1 lists the initialization values for the registers and counters at the MCU reset.

Interrupt

The MCU has nine interrupt sources; external signals ($\overline{INT_0} - \overline{INT_3}$), timer counter (timer A, timer B, timer C), serial interface, and key scanning. For each interrupt source, an interrupt request flag (IF), an interrupt mask bit (IM) and vector address are provided in order to control the interrupt request. The interrupt enable flag (I/E) allows interrupt service.

Interrupt Control Bits and Interrupt Service: Locations \$000 through \$003 and \$020 through \$023 in RAM are reserved for the interrupt control bits. These bits can be accessed by the RAM bit manipulation instructions. The interrupt request flags are set only by signals from interrupt sources. The MCU reset initializes the interrupt enable

flag and the interrupt request flags to 0 and the interrupt mask bits to 1. Figure 6 shows the interrupt control circuit block diagram. Table 2 lists interrupt priority and vector addresses for each interrupt source. Table 3 lists the state of the interrupt control bits for interrupt service caused by each interrupt source. An interrupt request occurs when the interrupt request flag is set to 1 and the interrupt mask flag is set to 0. In this case the interrupt enable flag is then set to 1, an interrupt occurs and a vector address corresponding to the interrupt source is then obtained from the PLA.

The sequence and flowchart for interrupt service are shown in figures 7 and 8 respectively. If an interrupt is requested, the current instruction is completed in the first cycle. The interrupt enable flag is then reset in the second cycle. The contents of the carry flag, status flag and program counter are pushed onto the stack in the second and third cycles. In the third cycle the program routine jumps to the appropriate vector address and the interrupt routine is executed. The user must assign each vector address to the JMPL instruction which branches to the starting address of the interrupt routine. In the interrupt routine, the interrupt request flag must be reset by software.

Table 1. Initial Values at the MCU Reset

Registers		Initial value	Description
Program Counter (PC)		\$0000	The program is executed from address \$0000
Status (ST)		1	The program branches by branch instruction
Stack Pointer (SP)		\$3FF	The stack level is set to 0
Interrupt flag/mask	Interrupt enable flag (I/E)	0	Any interrupts are masked
	Interrupt request flag (IF)	0	No interrupt request occurs
	Interrupt mask (IM)	1	Interrupt request is masked
I/O	Port data reg. (PDR) (high voltage pin)	0	Output 0 is enabled
	Port data reg. (PDR) (standard pin)	1	Output 1 is enabled
	Data control reg. (DCR)	0	Output buffer is OFF (in high impedance)
	Port mode reg. A (PMRA)	0000	See port mode register A section
	Port mode reg. B (PMRB)	0000	See port mode register B section
	Interrupt mode reg. (IMR)	0000	See interrupt mode register section
	Timer/serial	Timer mode reg. A (TMA)	0000
Timer mode reg. B (TMB)		0000	See timer mode register B section
Timer mode reg. C (TMC)		0000	See timer mode register C section
Serial mode reg. (SMR)		0000	See serial mode register section
Prescaler S		\$000	—
Prescaler W		\$00	—
Timer counter A (TCA)		\$00	—
Timer counter B (TCB)		\$00	—
Timer counter C (TCC)		\$00	—
Timer load reg. B (TLR)		\$00	—
Timer load reg. C (TCR)		\$00	—
VFD	Octal counter	000	—
	VFD segment reg. (FSR)	0000	See VFD segment register section
	VFD digit reg. (FDR)	0000	See VFD digit register section
	VFD dimmer mode reg. (DMR)	0000	See VFD dimmer mode register section
VFD control reg. (VCR)	0000	See VFD control register	
PWM	PWM data reg. (PWDR3-0)	0000	See PWM data register
Bit register	Low speed ON flag (LSON)	0	See low power dissipation mode section
	Watchdog timer ON flag (WDON)	0	See timer C section
Miscellaneous reg. (MIS)		0000	See miscellaneous register section

The following is the state of other registers and flags at the MCU reset:

Registers	In canceling Stop mode by the MCU reset	
	In canceling Stop mode by the MCU reset	In other cases at the MCU reset
Carry (CA)	The value before the MCU reset may be changed.	The value before the MCU reset may be changed.
Accumulator (A)	In this case the MCU must be initialized by software.	In this case the MCU must be initialized by software.
B register (B)		
W register (W)		
X/SPX register (X/SPX)		
Y/SPY register (Y/SPY)		
Serial data register (SR)	Same as above	Same as above
RAM	The value before the MCU reset (the value before the STOP instruction execution)	Same as above

Table 2. Vector Addresses and Interrupt Priority

Reset and interrupt	Priority	Vector address
Reset		\$0000
INT ₀	1	\$0002
INT ₁	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
Timer C	5	\$000A
Serial, INT ₂	6	\$000C
KEY SCAN, INT ₃	7	\$000E

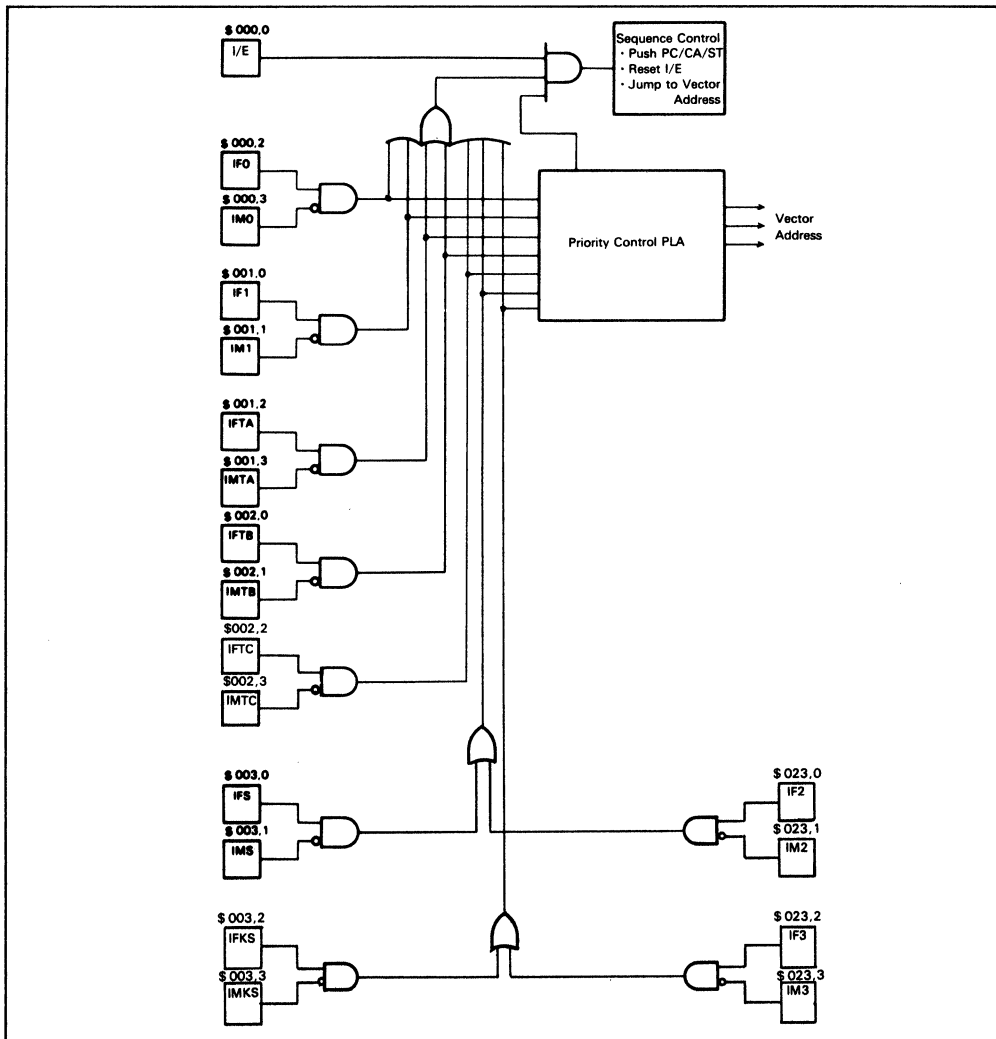


Figure 6. Interrupt Control Circuit Block Diagram

Table 3. Interrupt Service Conditions

Interrupt Control Bit	Interrupt Source					Serial, INT ₂	Key Scan, INT ₃
	INT ₀	INT ₁	Timer A	Timer B	Timer C		
I/E	1	1	1	1	1	1	1
IFO · IM0	1	0	0	0	0	0	0
IF1 · IM1	*	1	0	0	0	0	0
IFTA · IMTA	*	*	1	0	0	0	0
IFTB · IMTB	*	*	*	1	0	0	0
IFTC · IMTC	*	*	*	*	1	0	0
IFS · IMS + IF2 · IM2	*	*	*	*	*	1	0
IFKS · IMKS + IF3 · IM3	*	*	*	*	*	*	1

* : Don't care

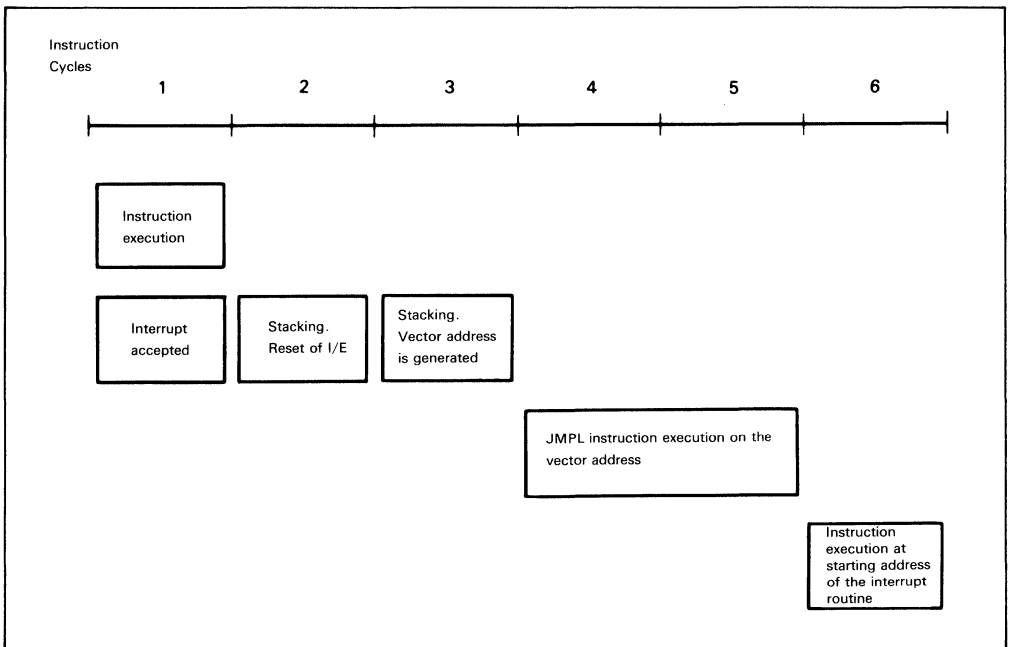


Figure 7. Interrupt Servicing Sequence

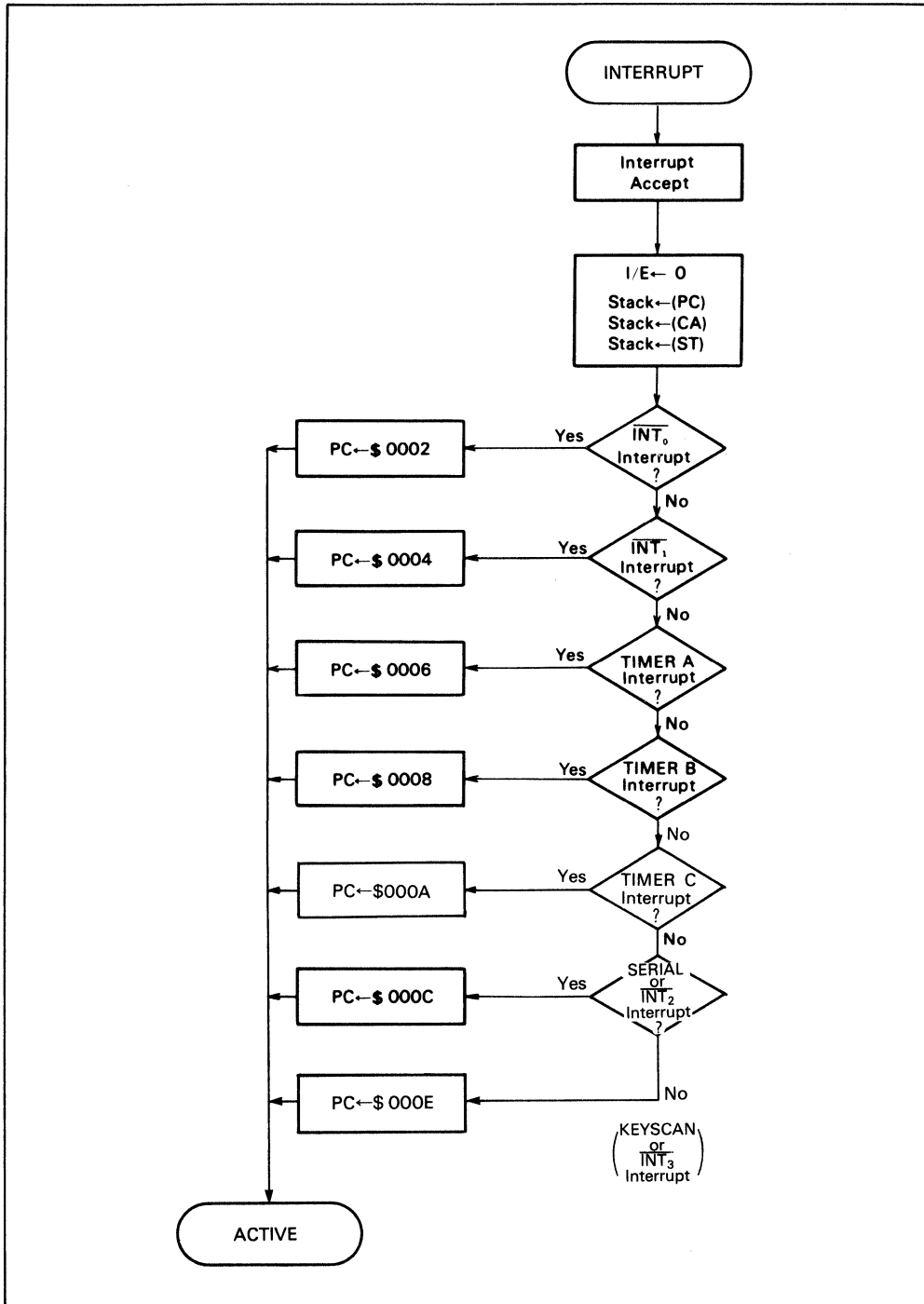


Figure 8. A Flowchart of Interrupt Servicing



Interrupt Enable Flag (I/E: \$000, 0): The interrupt enable flag controls all interrupts. This flag is reset by interrupt service and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 – \overline{INT}_3): The external interrupt input is activated by the port mode register (PMRA:\$004, PMRB:\$005). The external interrupt request flags IF0 and IF1 are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 . IF2 and IF3 are set at the rising and/or falling edge of \overline{INT}_2 and \overline{INT}_3 respectively. The contents of the interrupt mode register (IMR : \$014) specify the active edges. Figure 9 shows the interrupt mode register.

The \overline{INT}_1 can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 . In this case, the external interrupt mask flag (IM1) must be set so that \overline{INT}_1 should not request an interrupt.

External Interrupt Request Flags (IF0: \$000, 2, IF1:\$001, 0, IF2:\$023, 0, IF3:\$023, 2): The external interrupt request flags, IF0 through IF3, are set depending on the edge of \overline{INT}_0 through \overline{INT}_3 respectively.

External Interrupt Mask (IM0:\$000, 3, IM1:\$001, 1, IM2:\$023, 1, IM3:\$023, 3): The external interrupt mask bits mask an interrupt request caused by the external interrupt request flags.

Timer A Interrupt Request Flag (IFTA: \$001, 2): The timer A interrupt request flag is set when an overflow occurs in timer A.

Timer A Interrupt Mask (IMTA:\$001, 3): The timer A interrupt mask bit masks an interrupt request caused by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: \$002, 0): The timer B interrupt request flag is set when an overflow occurs in timer B.

Table 4. Interrupt Enable Flag

Interrupt enable flag (I/E)	Interrupt
0	Disable
1	Enable

Table 5. External Interrupt Request Flag

External interrupt request flag (IF0, IF1, IF2, IF3)	Interrupt request
0	Disable
1	Enable

Table 6. External Interrupt Mask Flag

External mask flag (IM0, IM1, IM2, IM3)	Interrupt request
0	Enable
1	Disable (mask)

Table 7. Timer A Interrupt Request Flag

Timer A interrupt request flag (IFTA)	Interrupt requests
0	Disable
1	Enable

Table 8. Timer A Interrupt Mask Flag

Timer A interrupt mask flag (IMTA)	Interrupt request
0	Enable
1	Disable (mask)

Table 9. Timer B Interrupt Request Flag (IFTB)

Timer B interrupt request flag (IFTB)	Interrupt request
0	Disable
1	Enable

Timer B Interrupt Mask (IMTB:\$002, 1): The timer B interrupt mask bit masks an interrupt request caused by the timer B interrupt request flag.

Timer C Interrupt Request Flag (IFTC:\$002, 2): The timer C interrupt request flag is set when an overflow occurs in timer C.

Timer C Interrupt Mask (IMTC:\$002, 3): The timer C interrupt mask bit masks an interrupt request caused by the timer C interrupt request flag.

Serial Interrupt Request Flag (IFS:\$003, 0): The serial interrupt request flag is set when the octal counter counts eight transfer

clock cycles or when data transfer is halted intermediately and the counter is reset.

Serial Interrupt Mask (IMS:\$003, 1): The serial interrupt mask bit masks an interrupt request caused by the serial interrupt request flag.

Key Scan Interrupt Request Flag (IFKS:\$003, 2): The key scan interrupt request flag is set when the VFD controller is put in the key scan mode.

Key Scan Interrupt Mask (IMKS:\$003, 3): The key scan mask bit masks an interrupt request caused by the key scan interrupt flag.

Table 10. Timer B Interrupt Mask Flag

Timer B interrupt mask flag (IMTB)	Interrupt request
0	Enable
1	Disable (Mask)

Table 11. Timer C Interrupt Request Flag

Timer C interrupt request flag (IFTC)	Interrupt request
0	Disable
1	Enable

Table 12. Timer C Interrupt Mask Flag

Timer C interrupt mask flag (IMTC)	Interrupt request
0	Enable
1	Disable (Mask)

Table 13. Serial Interrupt Request Flag

Serial interrupt request flag (IFS)	Interrupt request
0	Disable
1	Enable

Table 14. Serial Interrupt Mask Flag

Serial interrupt mask flag (IMS)	Interrupt request
0	Enable
1	Disable (Mask)

Table 15. Key Scan Interrupt Request Flag

Key scan interrupt request flag (IFKS)	Interrupt request
0	Disable
1	Enable

Table 16. Key Scan Interrupt Mask Flag

Key scan interrupt mask flag (IMKS)	Interrupt request
0	Enable
1	Disable (Mask)

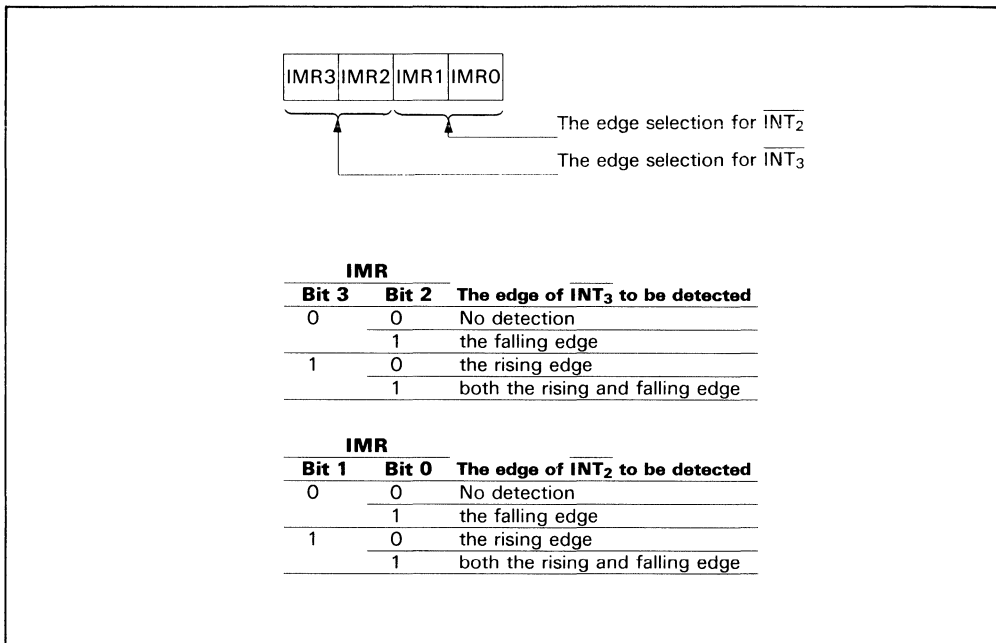


Figure 9. Interrupt Mode Register

Operating Modes

The MCU has two internal oscillation circuits. The oscillation clocks are used in the state shown in figure 10. Five operating modes are available according to how the clock is used.

Tables 17, 18, 19, show low power dissipation modes, the operations of low power dissipation modes, and I/O state in low power dissipation modes, respectively. Figure 10 shows the transition of the MCU operation modes.

Table 17. Low Power Dissipation Modes

		$\phi_{CPU}^{Note\ 2}$	
		Active	Stop
$\phi_{PER}^{Note\ 1}$	Active	Active mode (LSON = 0)	Standby mode
	Stop	Sub Active mode ^{Note 3} (LSON = 1)	Watch mode (TMA3 = 1) Stop mode (TMA3 = 0)

- Notes: 1. ϕ_{PER} : Clock signal for peripheral function except for time base.
 2. ϕ_{CPU} : System clock
 3. Sub Active mode is an optional mode.

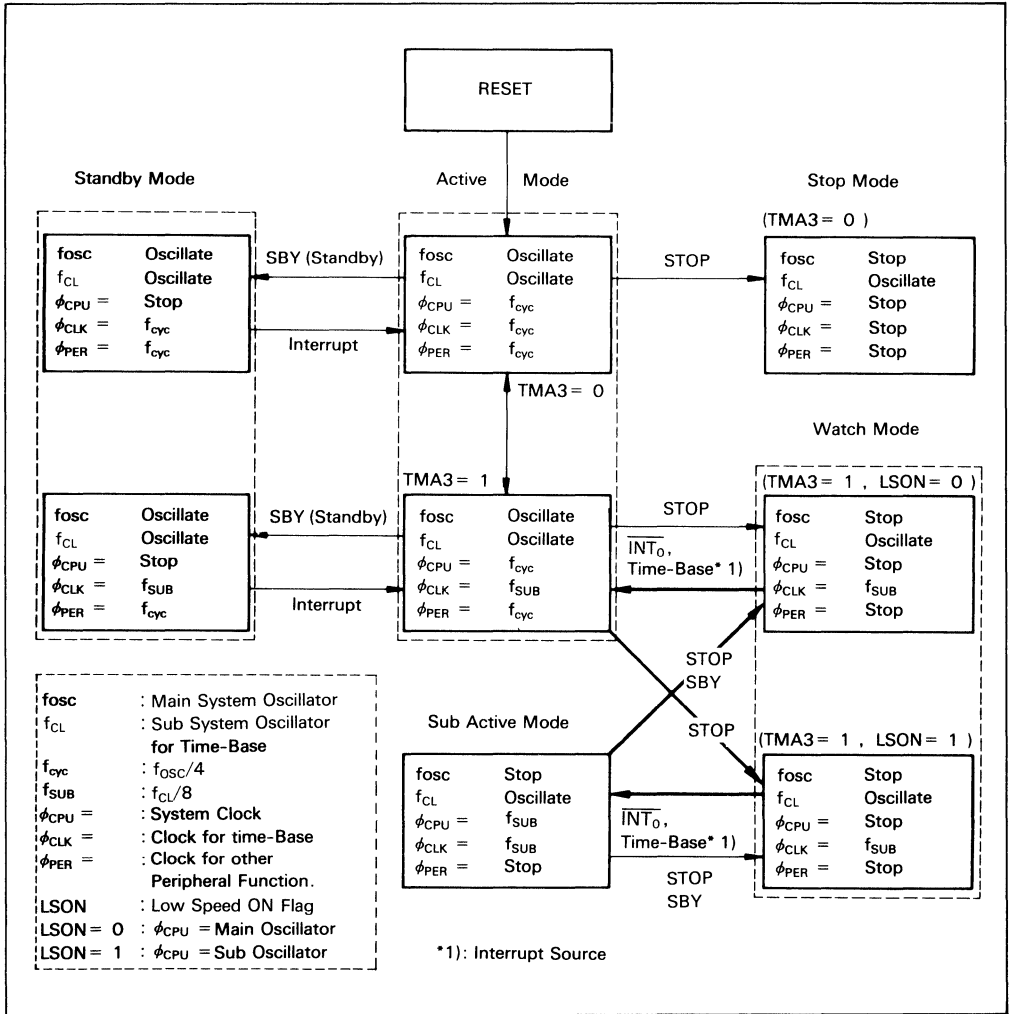



Figure 10. The Transition of the MCU Operation Modes

Table 18. The Operations of Low Power Dissipation Modes

Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Sub Active Mode ^{Note 7}
System Oscillator		Stop	Stop			Stop
Subsystem Oscillator		Note 2				
CPU Operation (ϕ_{CLK})	Instruction Execution	Stop	Stop	Stop		
	RAM	Hold	Hold	Hold		
	Registers, Flags	Reset	Hold	Hold		
	I/O ^{Note 3}	Reset	Hold	Hold		
Peripheral Function, Interrupt (ϕ_{PER})	\overline{INT}_0	Reset	Hold			Hold
	$\overline{INT}_1 - \overline{INT}_3$	Reset	Hold			Hold
	Timer A	Reset	Hold			Hold
	Timer B	Reset	Hold			Hold
	Timer C	Reset	Hold			Hold
	Serial	Reset	Hold			Hold
	VFD	Reset	Hold/ Reset ^{Note 4}	Note 8		Hold/ Reset ^{Note 4}
	PWM	Reset	Hold/ Reset ^{Note 4}			Hold/ Reset ^{Note 4}
Time-Base Function, Interrupt (ϕ_{PER})	\overline{INT}_0	Reset	Note 5	Note 6	Note 6	Note 5
	Time-Base	Reset	Note 5	Note 6	Note 6	Note 5

- Notes: 1.  indicates active.
2. When decreasing I_{CC} , stop oscillation by an external circuit.
 3. Refer to Table 19.
 4. Only timing generator is reset. The contents of the mode registers are retained.
 5. Refer to section interrupt frame.
 6. If TMA3 is set to 1, Timer A and \overline{INT}_0 are switched to time-base function and interrupt, respectively.
 7. Sub Active mode is an optional mode.
 8. VFD is active, but it displays nothing because the display data RAM stops working.



Active Mode: In Active mode, the MCU operates based on the clock generated by the system oscillator.

Standby Mode: The SBY instruction causes the MCU to enter Standby mode. In this mode, the oscillator remains active and an interrupt, the timer/counter and serial interface are enabled. The CPU is halted, since the clock which executes instructions has stopped. The state of the registers, RAM and I/O pins remains unchanged even after the MCU recover from Standby mode.

A RESET input or an interrupt request cancels Standby mode. In the case of the RESET input, the MCU is also reset. When an interrupt is requested, the MCU enters Active mode and an instruction next to the SBY instruction is executed. After this instruction is completed, if the interrupt enable flag is set, an interrupt is serviced; if the flag is reset, the interrupt request is suspended and the program routine is resumed. Figure 11 shows a flowchart of Standby mode.

Stop Mode: When the STOP instruction is executed while TMA3 = 0, the MCU enters Stop mode. In this mode, the system oscillator is halted, and the MCU enters stopped state.

Stop mode is canceled by the RESET input, as shown in figure 12. In this case, the RESET input must be applied for a t_{RC} (stabilization

time) (See AC characteristics section.). During Stop mode, the RAM holds its contents before the MCU entered this mode. After canceling Stop mode, the contents of the accumulator, B register, W register, X and SPX registers, Y and SPY registers, carry flag and serial data register can be changed.

Watch Mode: The MCU enters Watch mode by the STOP instruction during Active mode and TMA3 = 1 or by the STOP or SBY instruction during Sub Active mode. Watch mode can be canceled by the RESET input or timer A/INT₀ interrupt request. For a detailed description of the RESET input in canceling mode, see Stop mode section. If Watch mode is canceled by the timer A/INT₀ interrupt request, the MCU enters either Active mode or Sub Active mode depending on the state of the LSON bit. When the MCU enters Active mode, the interrupt request is delayed for a half of the interrupt frame period (t_{RC}) in order to wait stabilization of the system oscillation (figure 13). In this case, MCU operation is the same as that when canceling Standby mode (figure 11).

Sub Active mode: When entering Sub Active mode, the MCU operates based on the clock generated by the 32.768 kHz oscillator through CL₁ and CL₂. Table 19 shows MCU operation in Sub Active mode. As Sub Active mode is optional mode, the selection must be made in mask version orders.

Table 19. The State of Input/Output in Low Power Dissipation Modes

	Output	Input
	Standby Mode	Stop/Watch/ Sub Active Mode
D ₀ – D ₁₅	Hold/Peripheral function output	High impedance
RO – RA	Hold/Peripheral function output	High impedance
		All Modes (input state)
		Input enable
		Input enable

Note: Applying $V_{CC} - 0.3$ to GND + 0.3V to the input state pins generates current between V_{CC} and GND.

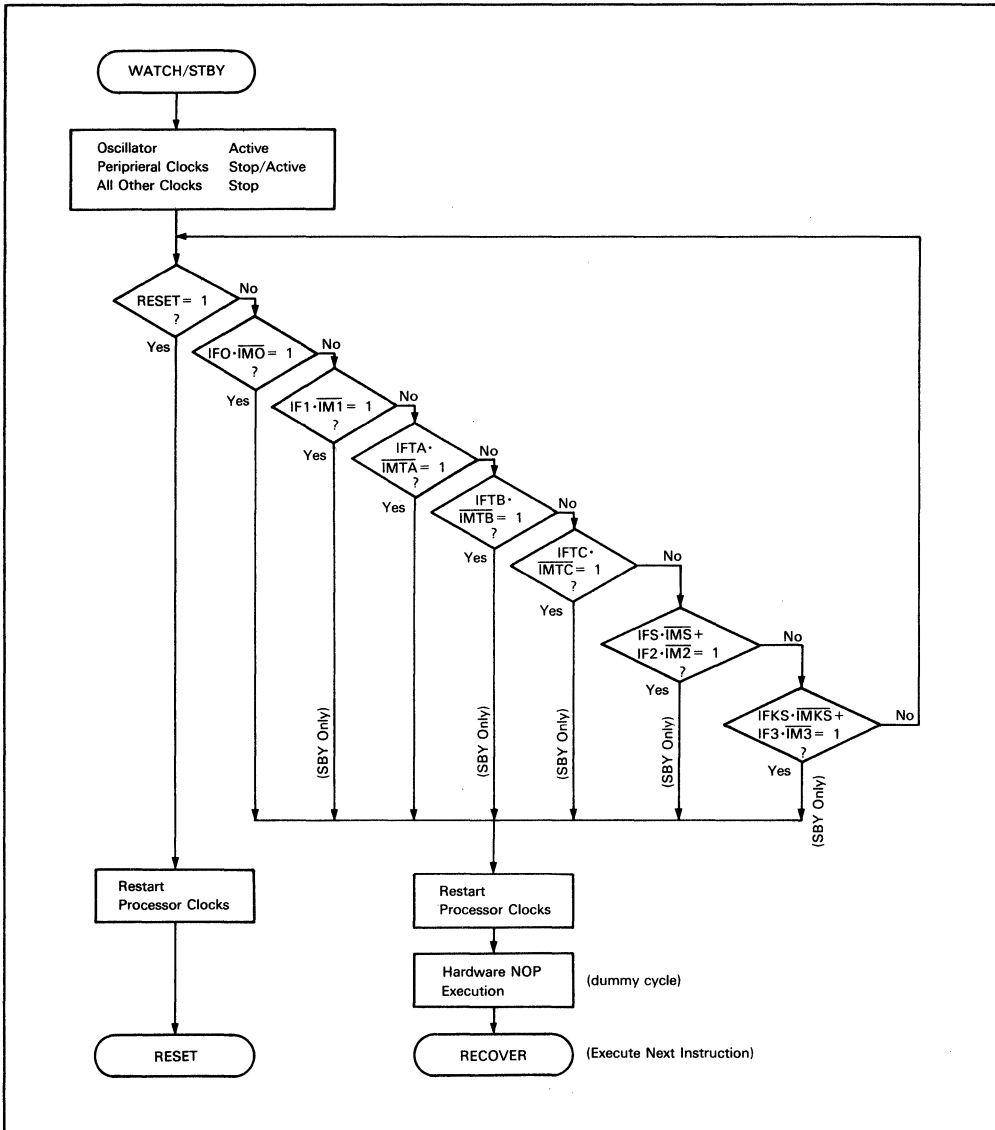


Figure 11. A Flowchart of Watch and Standby Mode

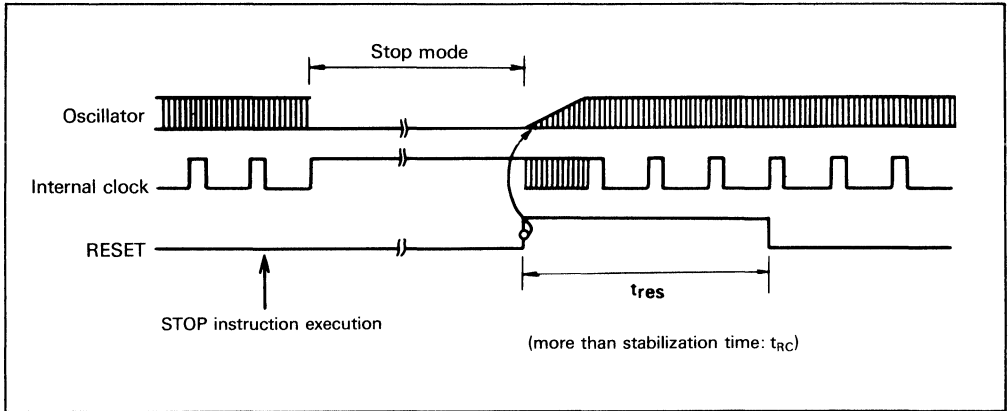


Figure 12. Timing Diagram When Canceling Stop Mode

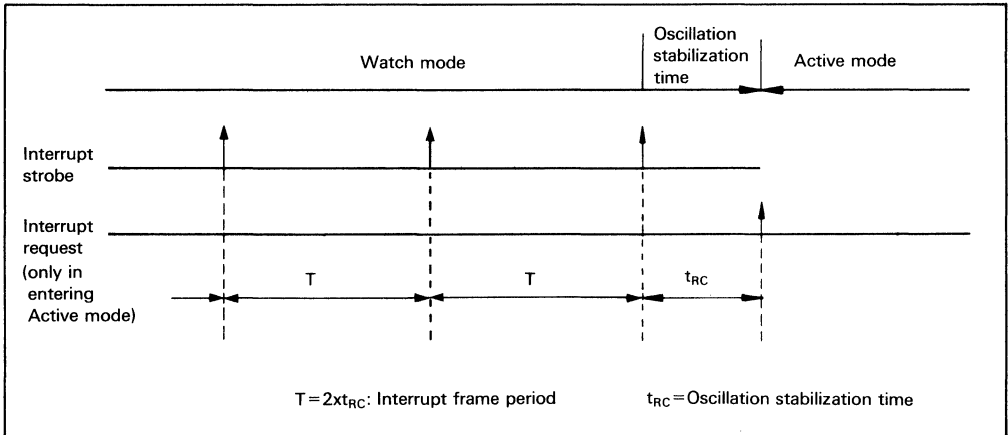


Figure 13. Interrupt Frame

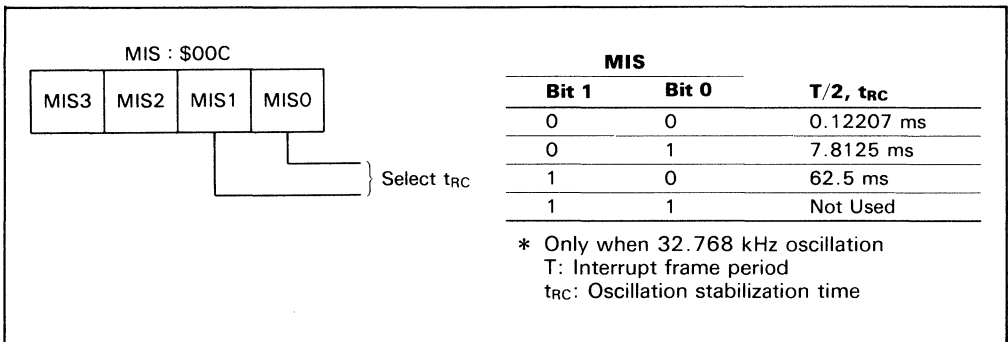


Figure 14. Miscellaneous Register

Interrupt Frame: In Watch mode and Sub Active mode, the time-base clock (ϕ_{CLK}) is applied to timer A and the \overline{INT}_0 circuit. Prescaler W and timer A operates as the time-base and generate the timing clock for the interrupt frame. The interrupt frame period (T) depends on the state of the miscellaneous register as shown in figure 14.

In Watch mode and Sub Active mode, the timer A/ \overline{INT}_0 interrupt occurs synchronously with the interrupt strobe timing clock. When the MCU wakes up to Active mode from Watch mode, the interrupt request is delayed for a half of interrupt frame period (t_{rc}). The falling edge of \overline{INT}_0 , which is input regardless of the interrupt frame clock cycle, is equiva-

lent to that synchronous with the interrupt strobe clock just after the falling edge. An overflow and interrupt request in timer A occurs synchronously with the interrupt strobe clock. But, when MCU transfers the watch mode to the active mode through the timer A interrupt, \overline{INT}_0 pin has to be high level.

MCU Operation Sequence

Figures 15, 16 and 17 show the MCU operation sequence. The RESET is an asynchronous input, which resets the MCU regardless of the MCU state.

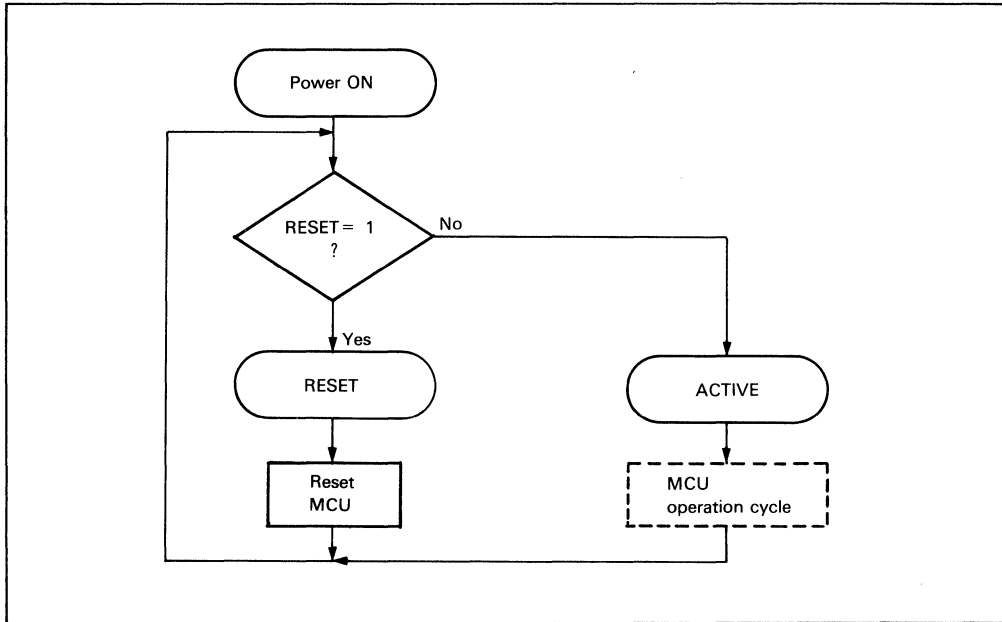


Figure 15. A Flowchart of MCU Operation (1)

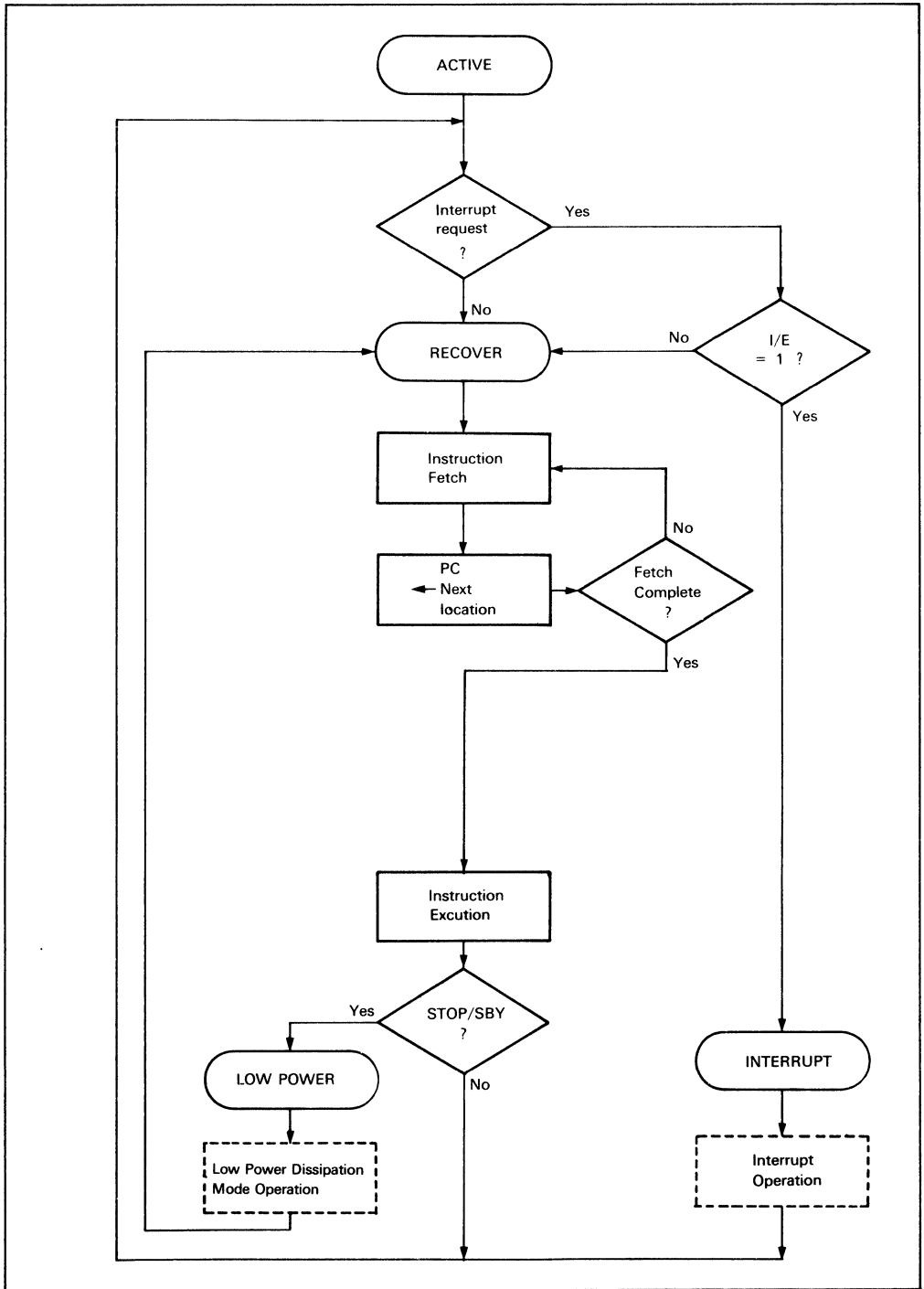


Figure 16. A Flowchart of MCU Operation (2) (MCU operation cycle)

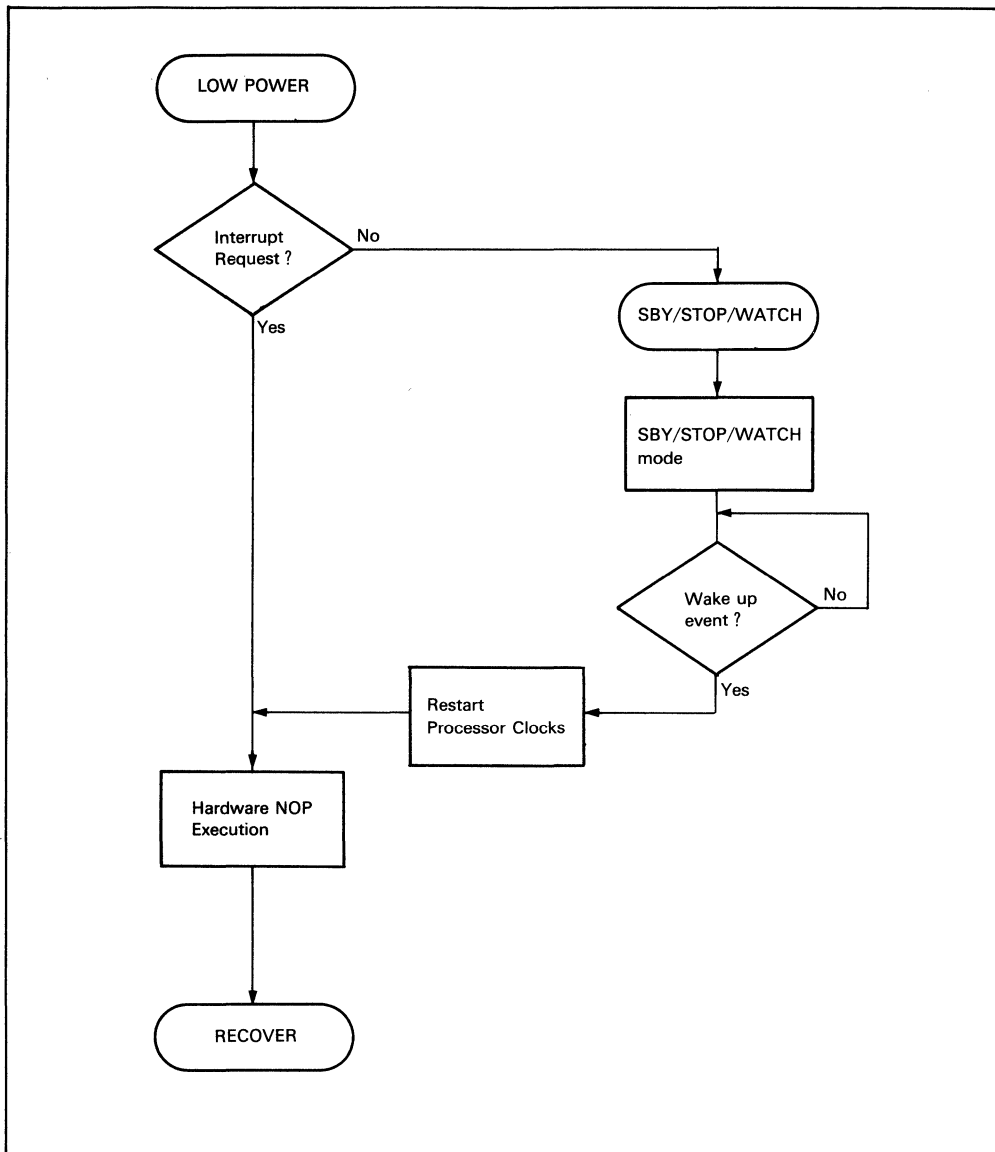


Figure 17. A Flowchart of MCU Operation (Low power dissipation mode operation)

Internal Oscillation Circuit

Figure 18 shows the internal oscillation circuit. The MCU can be connected with the

oscillator through OSC₁ and OSC₂, and with the 32.768 kHz crystal oscillator through CL₁ and CL₂.

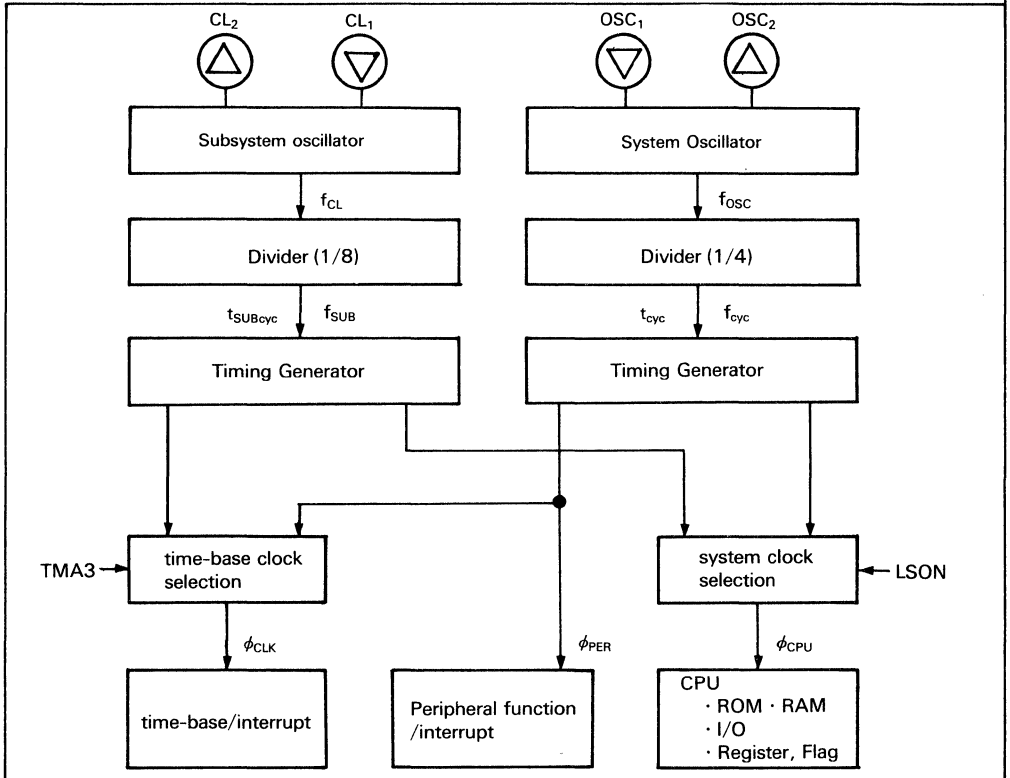


Figure 18. Internal Oscillation Circuit

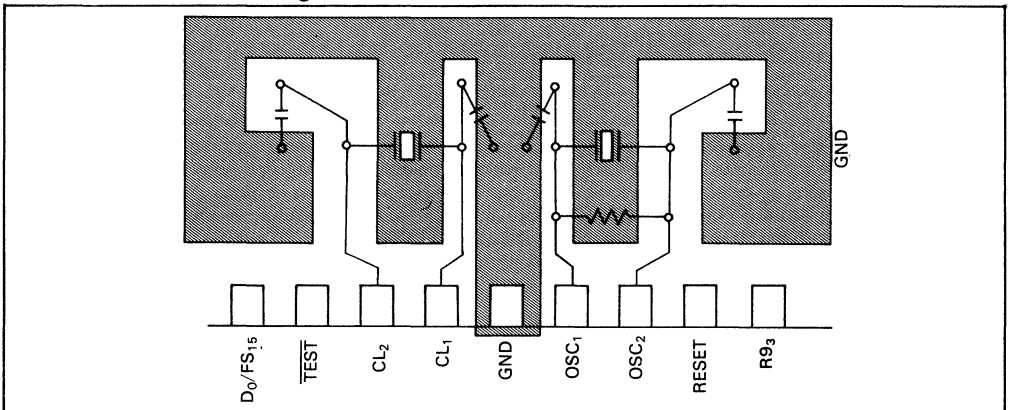


Figure 19. Layout of Crystal and Ceramic Filter

Table 20. Examples of Oscillation Circuit

	Oscillation circuit	Constant
External clock (OSC ₁ , OSC ₂)		
Ceramic filter oscillator (OSC ₁ , OSC ₂)		Ceramic filter: CSA4.00MG (Murata) Rf = 1MΩ ±20%, C ₁ = C ₂ = 30pF ±20%
Crystal oscillator (OSC ₁ , OSC ₂)		Rf = 1MΩ ±20%, C ₁ = C ₂ = 10–22pF ±20% Crystal: equivalent to circuit shown below Co = 7pF max. Rs = 100Ω max. f = 1.0 – 4.5 MHz
Crystal oscillator (CL ₁ , CL ₂)		C ₁ = C ₂ = 15pF ±5% Crystal: MX38T(Nippon Denpa) Co = 1.5pF typ. Rs = 14kΩ typ. f = 32.768 kHz

- Notes:
1. Since the circuit constant changes depending on the crystal and ceramic filter resonator and stray capacitance of the board, it is recommended that the user should consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
 2. Wiring among OSC₁, OSC₂, CL₁, CL₂ and elements should be as short as possible, and never cross other wiring (see figure 19).
 3. If the 32.768 kHz crystal oscillator is not used, CL₁ pin must be fixed to GND and CL₂ must be open.

Input/Output

The MCU has 50 input/output pins and six input pins including 32 high-voltage, high-current pins which are multiplexed with the

VFD controller pins. The state of the output buffer of the standard pins depends on a combination of the port data register (PDR) and the data control register (DCR).

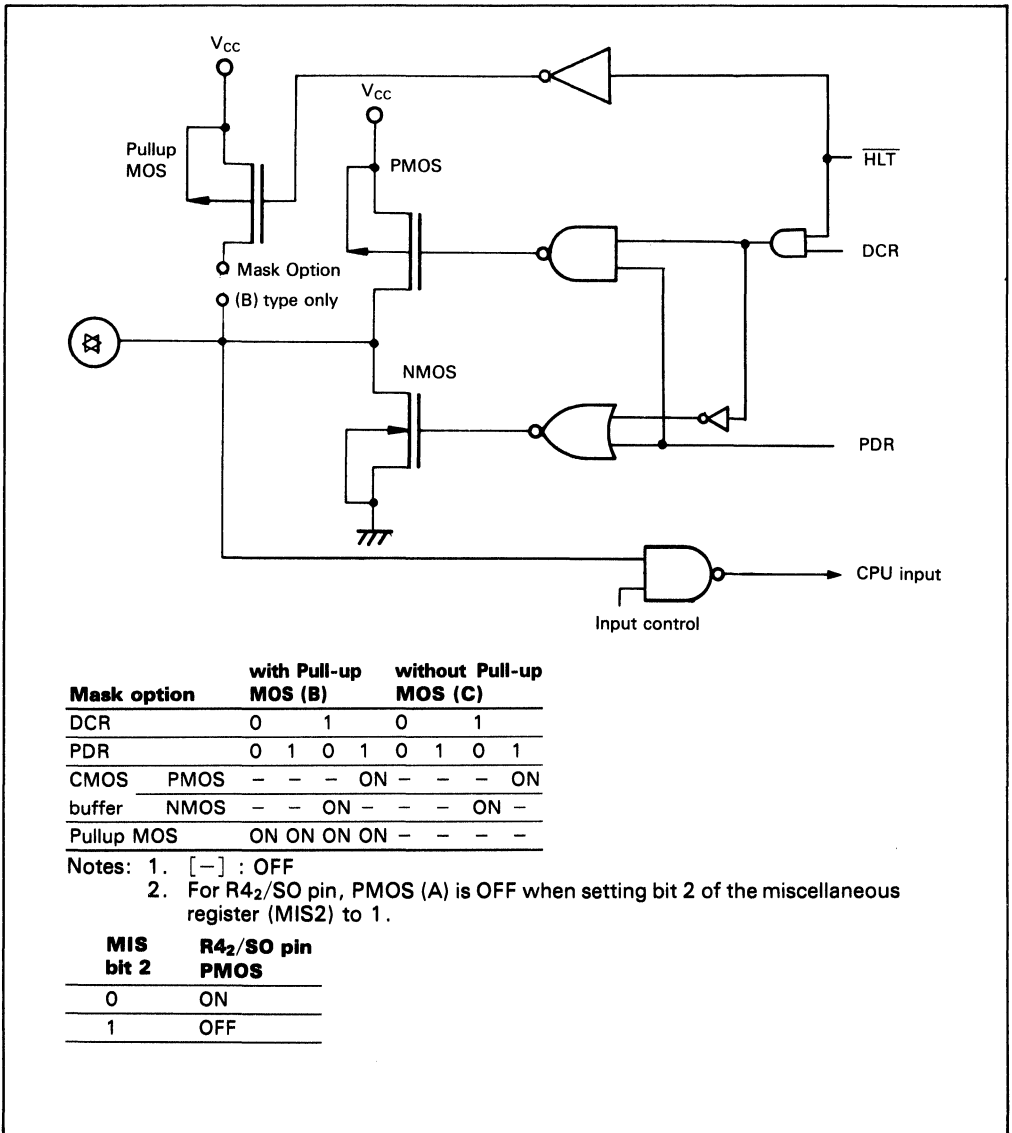


Figure 20. Input/Output Buffer

D Ports: The D ports are input/output ports addressed by bit. The SED and SEDD instructions set the ports, and the RED and REDD instructions reset them. The TD and TDD instructions test these pins. Port pins D_0 through D_{15} are multiplexed with the VFD controller pins FS_{15} through FS_0 , respectively.

R Ports: The R ports are ports addressed by 4 bits. The LAR and LBR instructions input data through these ports, and the LRA and LRB instructions output data through the ports. The state of the output buffer of R4 through R8 depends on the data control register (DCR4 to DCR8). R_{4_0} , R_{4_1} , R_{4_2} , R_{4_3} , R_{6_0} to R_{6_3} , R_{7_0} are multiplexed with SCK , SI , SO , PWM , $\overline{INT}_0 - \overline{INT}_3$ and $BUZZ$, respectively. Table 21 shows the R port circuit types.

Mask Options: The HD4074709 selects a C type circuit (without pullup MOS) or a D type circuit (without pulldown MOS), as shown in

table 21. The HD404709/HD404708 can also select the B type circuit (with pullup MOS) or the E type circuit (with pulldown MOS). In this case, however, these MCUs are not compatible with the HD4074709. If the HD404709/HD404708 selects the E type (with pulldown MOS), the source of the pulldown MOS are connected to the V_{disp} power supply through the RA_1/V_{disp} pin by the mask option.

How to Deal with Unused I/O Pins: The state of unused pins must be fixed to V_{CC} in order to prevent the LSI from malfunctioning due to noise. Note the following cautions before connection. Without pulldown MOS and without pullup MOS are selected for high voltage pins and standard pins, respectively. The contents of PDR and DCR of target pins must be retained as in reset state. The target pins must not be selected as a peripheral function I/O pins.

Table 21. Input/Output Pin Circuit Type

	With pullup MOS (B)	Without pullup MOS (C)	Pin name
Standard pins	I/O pins		R4 ₀ - R4 ₃ R5 ₀ - R5 ₃ R6 ₀ - R6 ₃ R7 ₀ - R7 ₃ R8 ₀ - R8 ₁
	Input pins		R9 ₀ - R9 ₃
	Peripheral I/O Pins		SCK (output) Note 1
	Peripheral output Pins		SO PWM BUZZ
	Peripheral input Pins		SCK (input) Note 1 SI INT ₀ INT ₁ INT ₂ INT ₃

Table 21. Input/Output Pin Circuit Type (Continued)

		Without pulldown MOS (D)	With pulldown MOS (E)	Pin name
High-voltage pin	I/O pins			D ₀ - D ₁₅ R ₀ - R ₃ R ₁₀ - R ₁₃ R ₂₀ - R ₂₃ R ₃₀ - R ₃₃
	Input Pins			RA ₀ - RA ₁
	Peripheral output pins			FS ₀ - FS ₁₅ FD ₀ - FD ₁₅

- Notes: 1. If the external clock is selected to the MCU as the clock source for the serial interface, \overline{SCK} is used as an input pin.
2. In Stop mode the MCU is internally reset and the selected peripheral function is canceled. The HLT signal goes to 1 and the I/O pins are put in high impedance.
3. In Watch/Sub Active mode the HLT signal is 1 and the output pins are put in high impedance. During these modes the pins selected to peripheral input or input/output must be fixed to input level, otherwise the current through V_{CC} and GND is generated.
4. The mask option of the circuit type is shown in the following. The mask ROM type MCU is compatible with the ZTAT type only when the mask ROM type selects the C and D circuit type.

Circuit type	Product type			
	B	C	D	E
Mask ROM type (HD404709 HD404708)	option			
ZTAT type (HD4074709)		fixed		

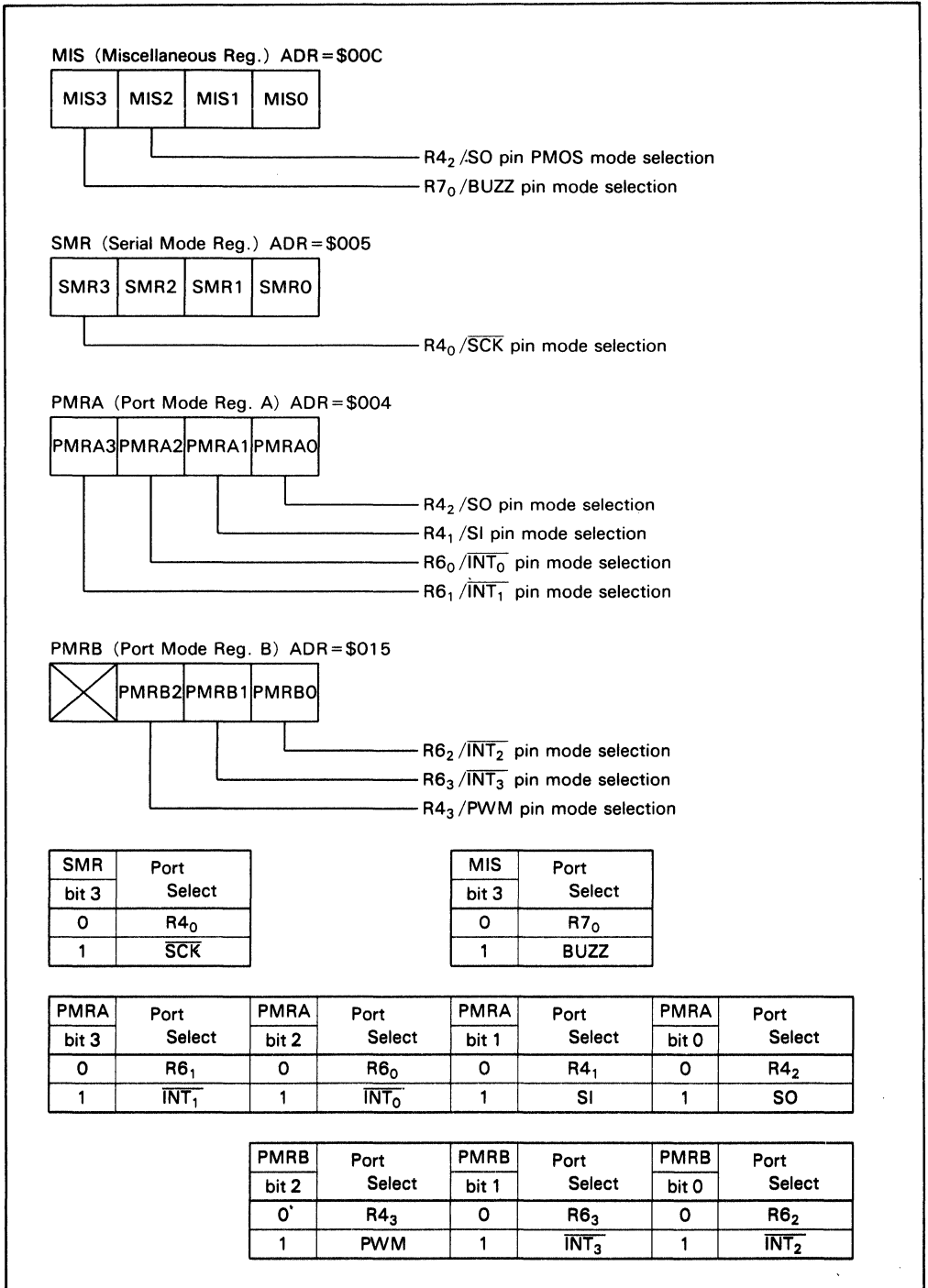


Figure 21. Pin Mode Selection Registers

Timer

The MCU contains two prescalers (prescaler W and prescaler S) and three timer/counters (timer A, timer B, timer C). Figures 22 and 23 show the block diagrams of the timers. The function of the timers depend on the state of the bits as shown in table 22.

Prescaler S: Prescaler S is driven by the system clock. This prescaler, after being initialized to \$000 by the MCU reset, divides the system clock frequency. During Watch mode and Sub Active mode, dividing operation stops and count value is retained. When the mode is canceled, dividing operation re-

starts. From among the prescaler outputs the input clock of the timer and the transfer clock of serial interface are specified by timer mode registers (TMA, TMB, TMC) and serial mode register (SMR) respectively.

Prescaler W: Prescaler W is driven by the CL1 input clock divided by 8. This prescaler, after being initialized to \$00 by the MCU reset, divides the input clock frequency. The input clock of the timer A may be specified from among prescaler W outputs, depending on the state of timer mode register A. In this case, prescaler W and timer A can be reset by software.

Table 22. Selecting Functions of Timers A/B/C

Timer A Condition	Function	Timer C Condition	Function
TMA3 = 0	system clock base interval timer	WDON = 0 (MIS3 = 1)	automatic reloading timer (square wave output circuit using R7 ₀ /BUZZ)
TMA3 = 1	time-base for watch	WDON = 1	watchdog timer

Timer B Condition	Function
TMB2 - 0 ≠ 111	automatic reloading timer
TMB2 - 0 = 111 PMRA3 = 1	event counter (using R6 ₁ /INT ₁)

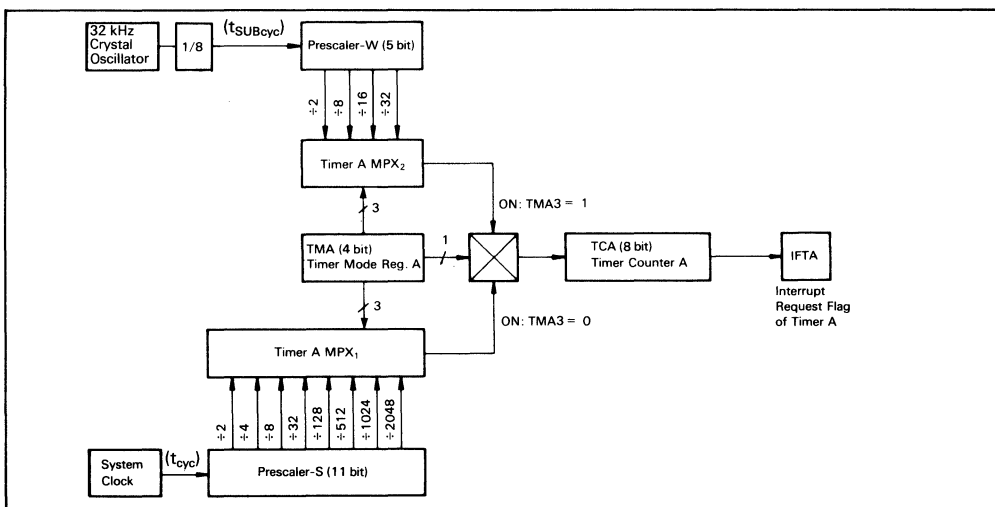


Figure 22. Timer A Block Diagram



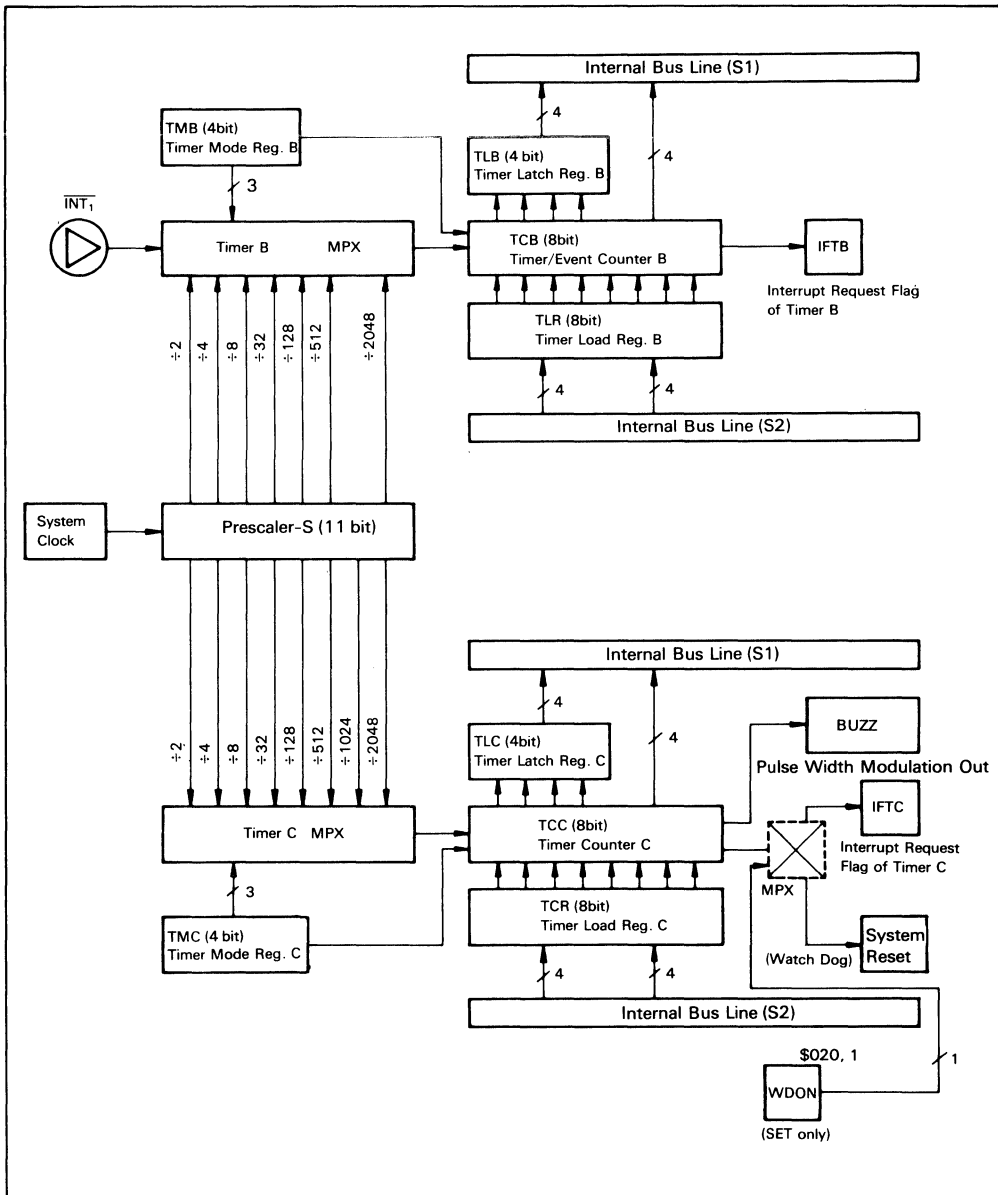


Figure 23. Timer B/Timer C Block Diagram

Timer A Operation: Timer A is initialized to \$00, and then counts up at every input clock. If an input clock is applied to timer A after the timer is \$FF, an overflow occurs and timer A is set to \$00. The overflow causes timer A interrupt request flag (IFTA: \$001, 2) to go to 1, and the timer continues to count up from \$00. Timer A is an interval timer in which an overflow occurs every 256 clock inputs.

Timer A can also be used as the watch time base when the TMA3 bit of timer mode register A is set to 1. The timer is driven by the 32.768 kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by timer mode register A.

Timer B Operation: Automatic reloading, input clock source and prescaler dividing ratio of timer B depend on the state of timer mode register B. When using the external event input as the input clock source of timer B, the R6₁/INT₁ pin must be defined as INT₁, by the port mode register (PMRA: \$004) and an interrupt must be masked by the external interrupt mask bit (IM1).

Timer B is initialized to the value set in timer load register by software, and is then incremented by one every clock input. If an

input clock is applied to timer B after the timer is \$FF, an overflow occurs. In this case, if automatic reloading is enabled, timer B is initialized to the initial value; if reloading is disabled, the timer is initialized to \$00. The overflow sets the timer B interrupt request flag (IFTB: \$002, 0).

Timer C Operation: The automatic reloading, and the prescaler dividing ratio of timer C depend on the state of timer mode register C. Timer C is initialized to the value set in the timer load register by software, and is then incremented by one every clock input. If an input clock is applied to timer C after the timer is \$FF, an overflow occurs. In this case, if automatic reloading is enabled, timer C is initialized to the initial value; if reloading is disabled, the timer is initialized to \$00. The overflow sets the timer C interrupt request flag (IFTC: \$002, 2).

Timer C also functions as a watchdog timer. When the program routine goes out of control and an overflow occurs while the WDON flag is set, the MCU is reset. Moreover, timer C provides a variable-duty pulse output (BUZZ). The output waveform depends on the state of timer mode register C and timer load register, as shown in figure 24. During the pulse output, the R7₀/BUZZ pin must be defined as BUZZ by the miscellaneous register.

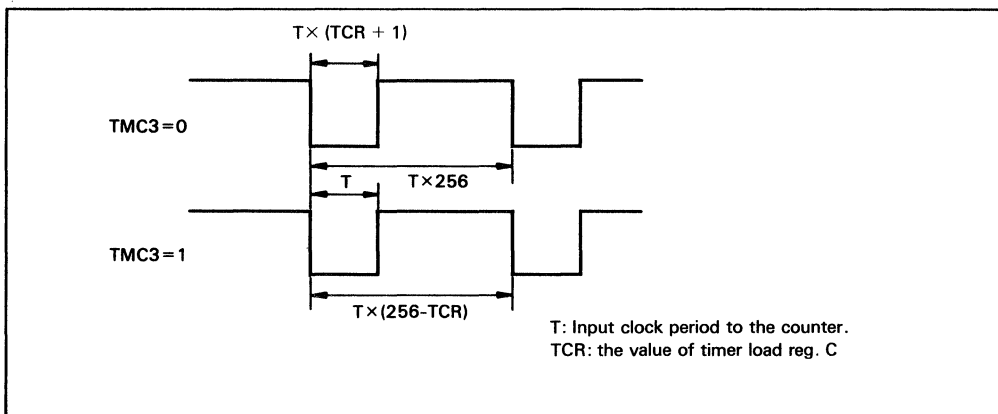


Figure 24. Variable-duty Pulse Output Waveform

Timer Mode Register A (TMA: \$008):
 Timer mode register A is a 4-bit write-only register which controls timer A as shown in figure 25. This register is initialized to \$0 by the MCU reset.

Timer Mode Register B (TMB: \$009):
 Timer mode register B is a 4-bit write-only register which determines whether or not the MCU provides automatic reloading and selects the input clock and the prescaler dividing ratio. This register is initialized to \$0 by the MCU reset. The contents of the register can be changed at the second instruction cycle following write instruction execution. Timer B must be programmed not to be

initialized by the write instruction to timer load register until the timer mode is enabled.

Timer Mode Register C (TMC: \$00D):
 Timer mode register C is a 4-bit write-only register which determines whether or not the MCU provides the automatic reloading and selects the prescaler dividing ratio. This register is initialized to \$0 by the MCU reset. The contents of the register can be changed at the second instruction cycle after write instruction execution. Timer C must be programmed so as not to be initialized by the write instruction to timer load register until the timer mode is enabled.

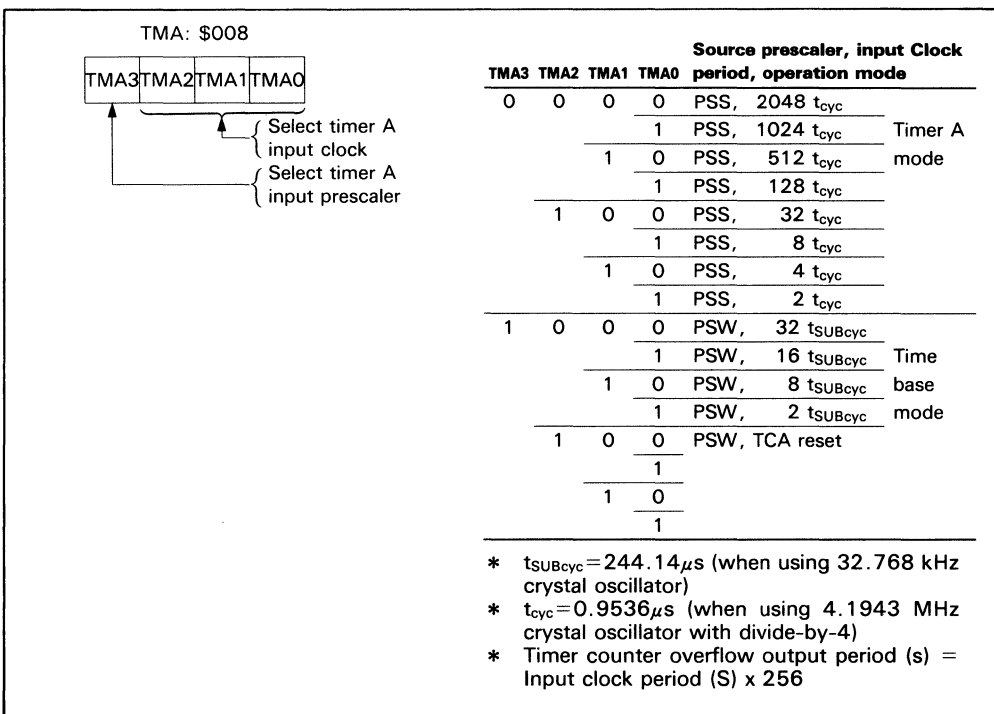


Figure 25. Timer Mode Register A

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low digit (TCBL: \$00A, TLRL: \$00A) and a high digit (TCBU: \$00B, TLRU: \$00B).

The timer/event counter is initialized by writing data to the timer load register. In this case, the user must write data to the lower digit first. The timer/event counter is initialized to the value set in the timer load register with a write cycle of the higher digit. The timer load register is initialized to \$00 by the MCU reset.

Timer B count value is obtained by reading the timer/event counter. In this case, the user must read the higher digit first. The count value is latched at the time when the higher digit is read.

Timer C (TCCL: \$00E, TCCU: \$00F, TCRL: \$00E, TCRU: \$00F): Timer C consists of an 8-bit write-only timer load register and an 8-bit read-only timer/counter. Each of them has a lower digit (TCCL: \$00E, TCRL: \$00E) and a higher digit (TCCU: \$00F, TCRU: \$00F). Timer C operation is the same as that for timer B.

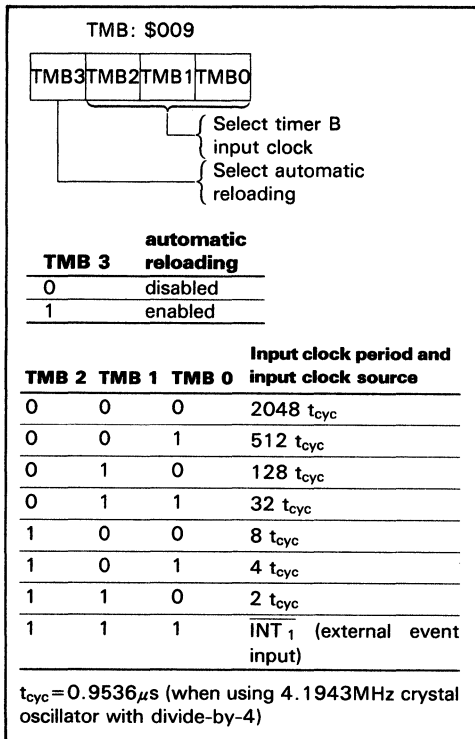


Figure 26. Timer Mode Register B

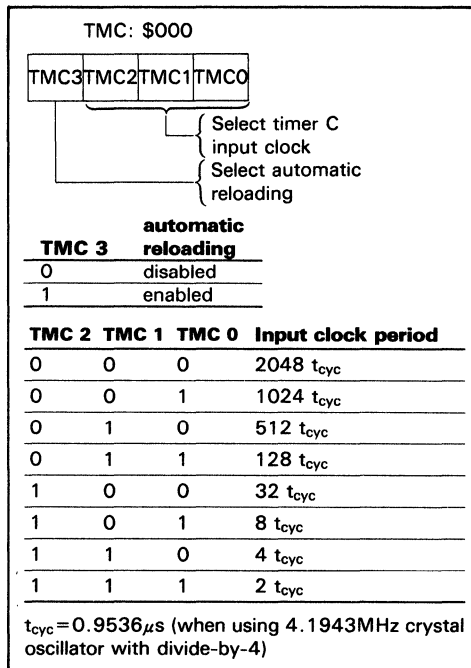


Figure 27. Timer Mode Register C

Serial Interface

The serial interface transmits/receives 8-bit serial data. It consists of the serial data register, the serial mode register, the port mode register A, the octal counter and the multiplexer (figure 28). The R4₀/SCK pin and the transfer clock signal are controlled by writing data to the serial mode register. The serial data register can be read and written by software. The contents of this register can be shifted synchronously with the transfer clock

signal.

The serial interface is activated by the STS instruction. The octal counter, which is initialized to \$0 by the STS instruction, starts to count at the falling edge of the transfer clock signal (SCK) and is incremented by one at the rising edge of the clock signal. When the counter is reset after eight clock signals are input or when data transmission is discontinued, the serial interrupt request flag is set.

Table 23. Serial Interface Operation Modes

SMR 3	PMR 1	PMR 0	Serial interface operation modes
1	0	0	Clock Continuous Output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/Receive mode

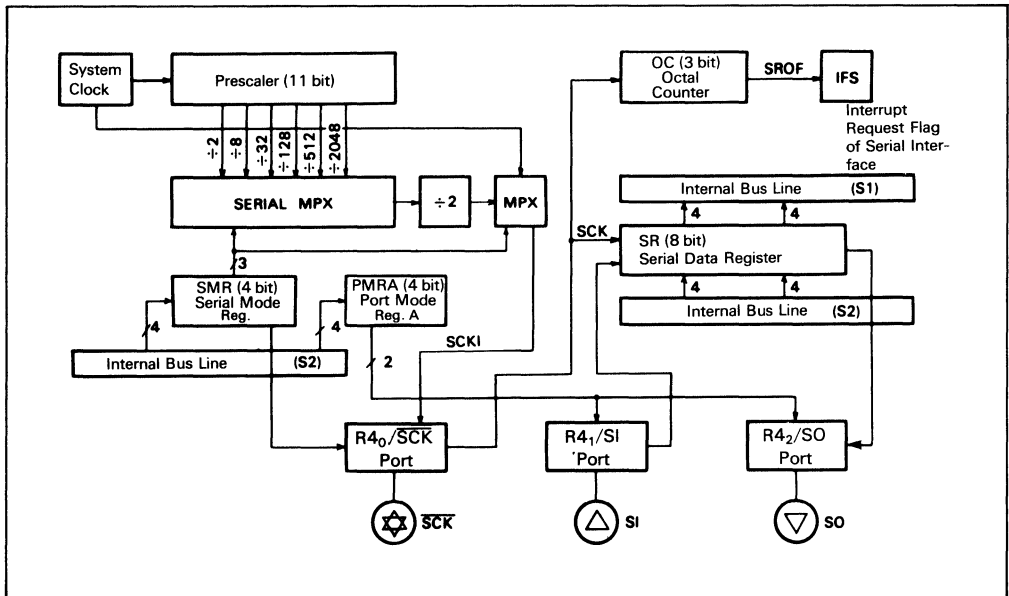


Figure 28. Serial Interface Block Diagram

Serial Mode Register (SMR: \$005): The serial mode register is a 4-bit write-only register which controls the R4₀/SCK pin and the transfer clock signal. When data is written to this register, the serial interface is internally initialized. Write signal to the serial mode register discontinues the transfer clock to the serial data register and octal counter, resets the counter to \$0, and sets the serial interrupt request flag if previous value of octal counter

was not \$0 (figure 29).

The contents of the serial mode register is not valid until the second instruction cycle after the write instruction execution. The user must program the STS instruction to be executed after this instruction cycle. The serial mode register is initialized to \$0 by the MCU reset.

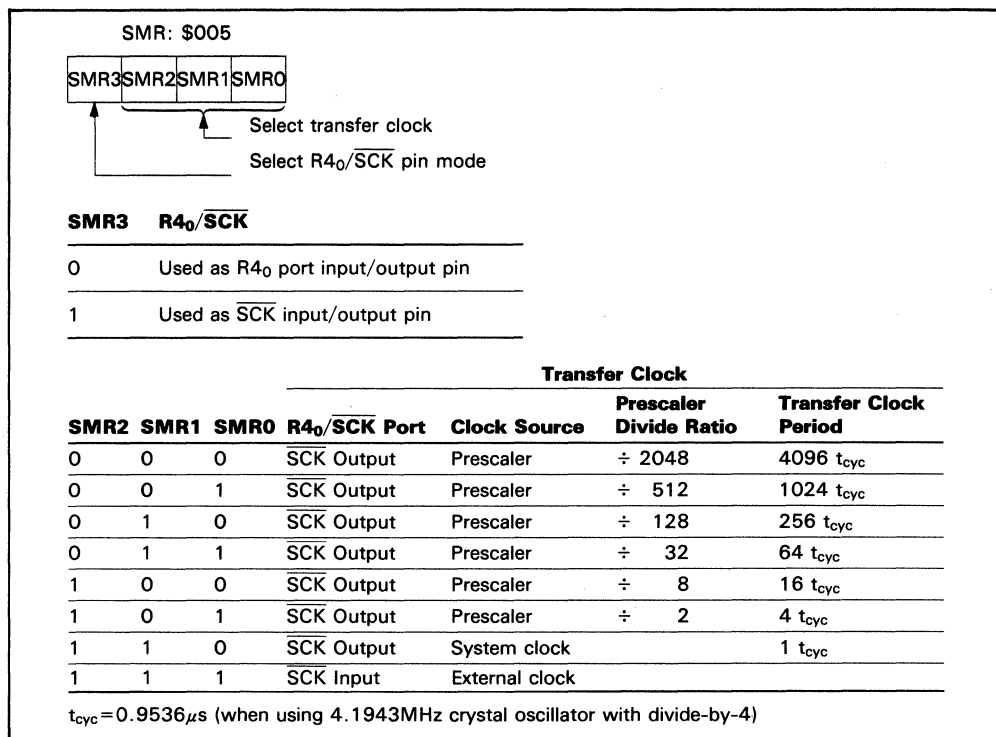


Figure 29. Serial Mode Register

Serial Data Register (SRL: \$006, SRU: \$007): The serial data register is an 8-bit read/write register which consists of a lower digit (SRL: \$006) and a higher digit (SRU: \$007). The data in this register is output from the least significant bit (LSB) through the SO pin synchronously with the falling edge of the transfer clock. External data is then written to the register from the LSB through the SI pin synchronously with the rising edge of the transfer clock. Figure 30 shows the timing chart for the transfer clock and data input/output clock.

The serial data register must not be read or written until the data transmission is completed. If the register is read or written during the data transmission, the data may be changed.

Serial Interface Operation Modes: Table 23 lists the serial interface operation modes. The user must specify the state of the port mode register and serial mode register as listed in the table. In changing the operation modes, the serial interface must be internally initialized by writing data to the serial mode register.

The State of Serial Interface: The serial interface is provided with three different states as shown in figure 31. In STS waiting state, the serial interface is internally initialized. In this case, even the transfer clock

input does not enable the serial interface. When the STS instruction is executed during this state, the serial interface system enters SCK waiting state. If the transfer clock is applied to the MCU during this state, the interface system enters transfer state, which enables the octal counter and the serial data register. In this case, if the system is in the clock continuous output mode, the system remains in SCK waiting state and the transfer clock is continuously output.

If eighth transfer clock cycles are applied to the MCU or the STS instruction is executed during the clock transfer state, the octal counter is reset to 000 and the interface system enters the SCK waiting state. When the system is changed from the transfer state to another state, the counter is reset to 000, which sets the serial interrupt request flag.

When the internal transfer clock is used, the STS instruction triggers the transfer clock output. The clock output is stopped after eight clock cycles. When data is written to the port mode register during the SCK waiting state or transfer state, the serial interface must be internally initialized by writing data to the serial mode register. After performing a write to the serial mode register, the serial interface system is put in the STS waiting state.

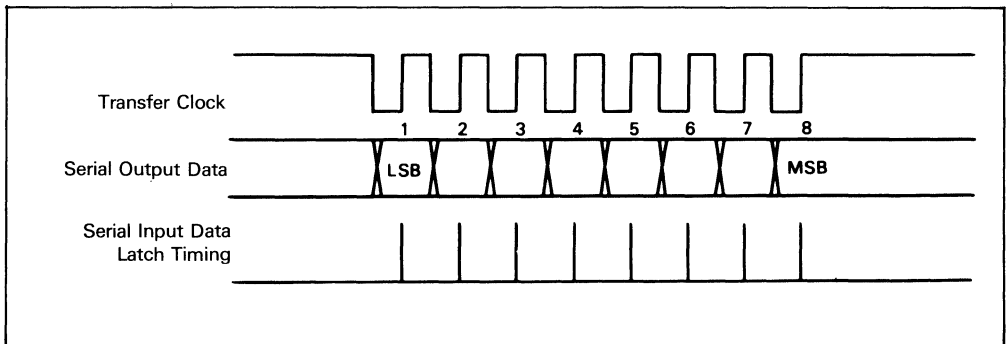


Figure 30. Serial Interface Timing Diagram

Example of Transfer Clock Error Detection: The serial interface system malfunctions when an external noise pulse is superimposed over the transfer clock pulse. Such errors can be detected through the procedure shown figure 32.

For example, if, after eight clock cycles, the transfer clock continues to be applied to the MCU during transfer clock wait state, the

state of the serial interface system is changed to transfer state. This state remains unchanged for next eight clock cycles, and the system is then changed to SCK waiting state again. The serial interrupt request flag must be reset before entering the serial interface system into the STS waiting state by writing data to the serial mode register. This procedure sets the interrupt request flag again.

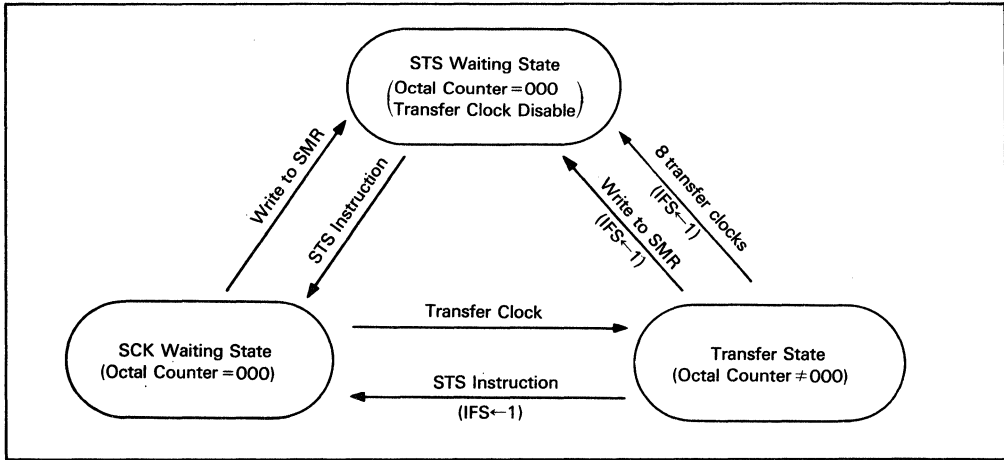


Figure 31. Serial Interface Operation State

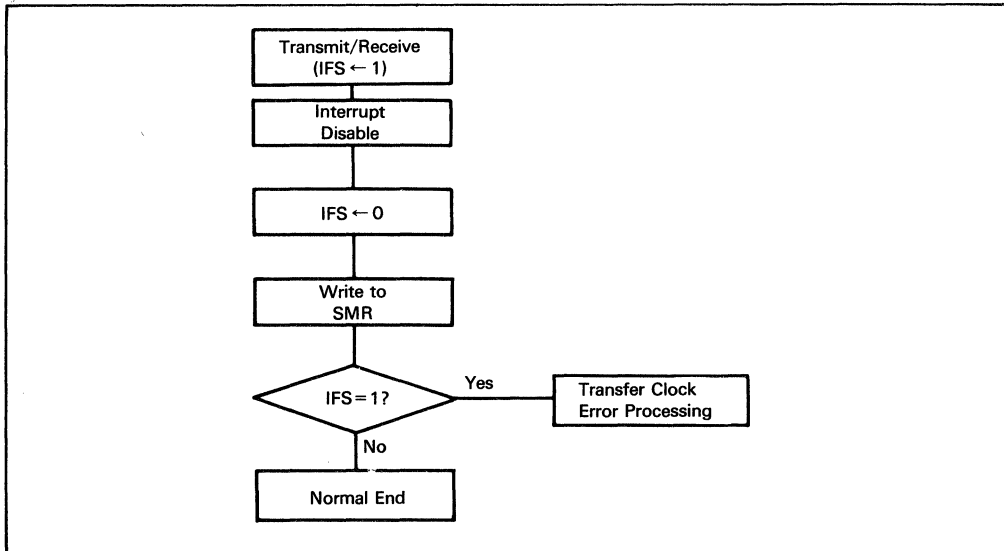


Figure 32. Example of Transfer Clock Error Detection

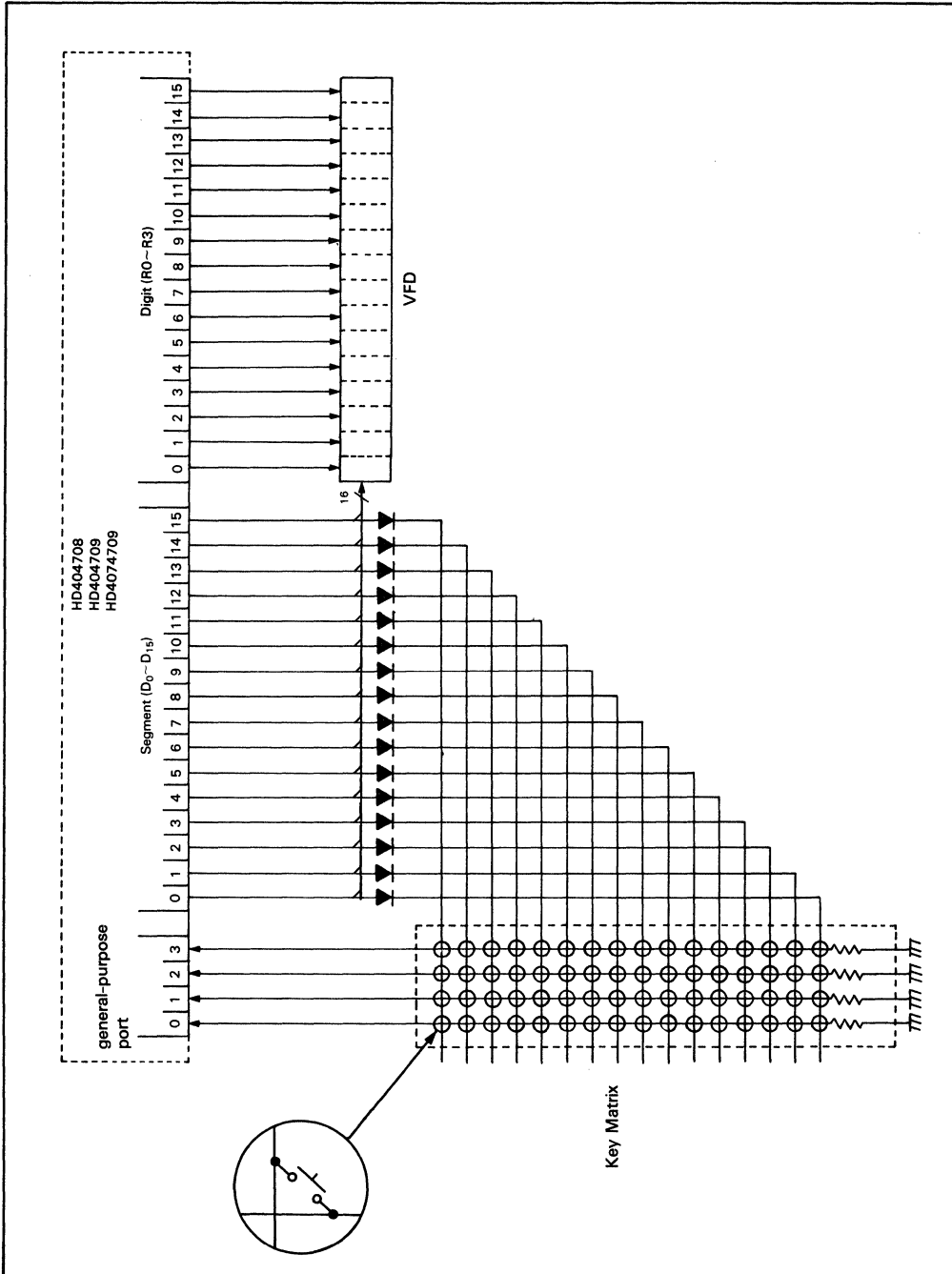


Figure 34. Example of Connection with the VFD

VFD Data RAM: Table 24 lists the addresses of the VFD data RAM. The RAM area unused

in the display mode can be assigned for general purpose.

Table 24. The VFD Data RAM Addresses

Pin	Segment Digit	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RO ₀	0	\$090			\$080			\$070			\$060						
RO ₁	1	\$091			\$081			\$071			\$061						
RO ₂	2	\$092			\$082			\$072			\$062						
RO ₃	3	\$093			\$083			\$073			\$063						
R1 ₀	4	\$094			\$084			\$074			\$064						
R1 ₁	5	\$095			\$085			\$075			\$065						
R1 ₂	6	\$096			\$086			\$076			\$066						
R1 ₃	7	\$097			\$087			\$077			\$067						
R2 ₀	8	\$098			\$088			\$078			\$068						
R2 ₁	9	\$099			\$089			\$079			\$069						
R2 ₂	10	\$09A			\$08A			\$07A			\$06A						
R2 ₃	11	\$09B			\$08B			\$07B			\$06B						
R3 ₀	12	\$09C			\$08C			\$07C			\$06C						
R3 ₁	13	\$09D			\$08D			\$07D			\$06D						
R3 ₂	14	\$09E			\$08E			\$07E			\$06E						
R3 ₃	15	\$09F			\$08F			\$07F			\$06F						

- Notes:
1. In each segment, the right end corresponds to the LSB and the left end to the MSB.
 2. The halftone indicates the VFD data RAM location used in displaying 8-segment x 12-digit data. In this example, other locations can be used for general purpose.
 3. The contents of RAM addresses \$07C – \$07F and \$06C – \$06F (not display data) are output from segment pins at the timing of digit 12 – 15.

HD404708/HD404709/HD4074709

VFD Control Register (VCR: \$013): The VFD control register consists of a write-only bit and a read/test-only bit.

The VFD mode bit (FLMO: \$013, 0) is a write-only bit which selects a frame period of either 3264 or 6528 instruction cycles. This bit is initialized to 0 by the MCU reset.

The key scan flag (KSF: \$013, 3) is a read/test-

only flag. This flag indicates either the display period or the key scan period. The key scan period is one-seventeenth of the frame period. During the key scan period, the D port and R0 through R3 port pins are controlled by the CPU for general purpose. When using these pins, key scanning can be enabled by software. At the rising edge of the key scan interrupt request flag is set to 1.

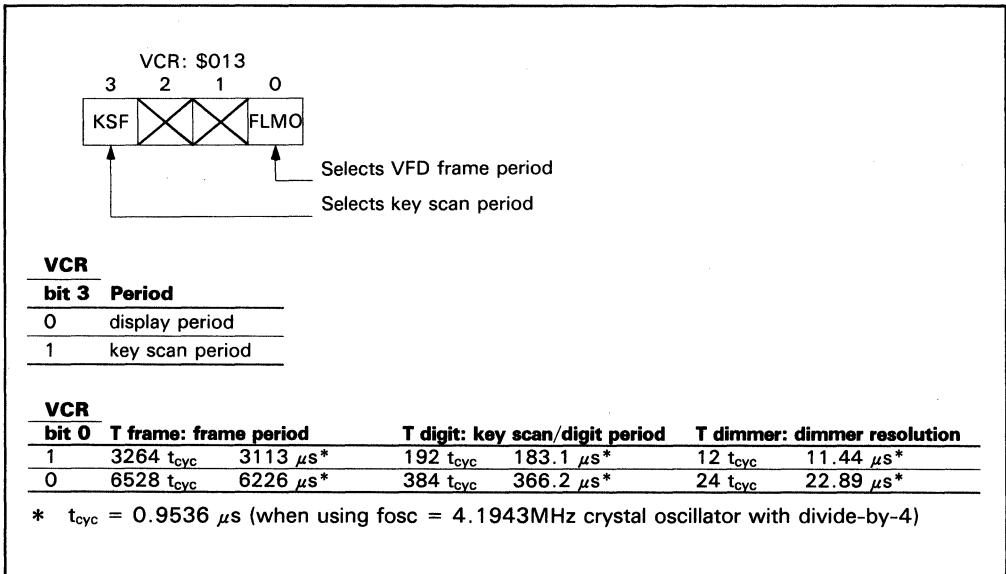


Figure 35. VFD Control Register

Dimmer Mode Register (DMR: \$012): The dimmer mode register is a 4-bit write-only register which controls the VFD driver pin mode and the digit signal output waveform. The register can specify the waveform from among eight types as shown in figure 36. The dimmer mode register is initialized to \$0 by the MCU reset. When specifying the

waveform, the user must take into consideration the waveform resolution. For detailed description of the resolution, see the VFD control register section. DMR3 is used as a master bit for the VFD controller. During DMR3 is 0, D₀ - D₁₅ and R₀ - R₃ function as general purpose ports, and the display timing generator is in reset state.

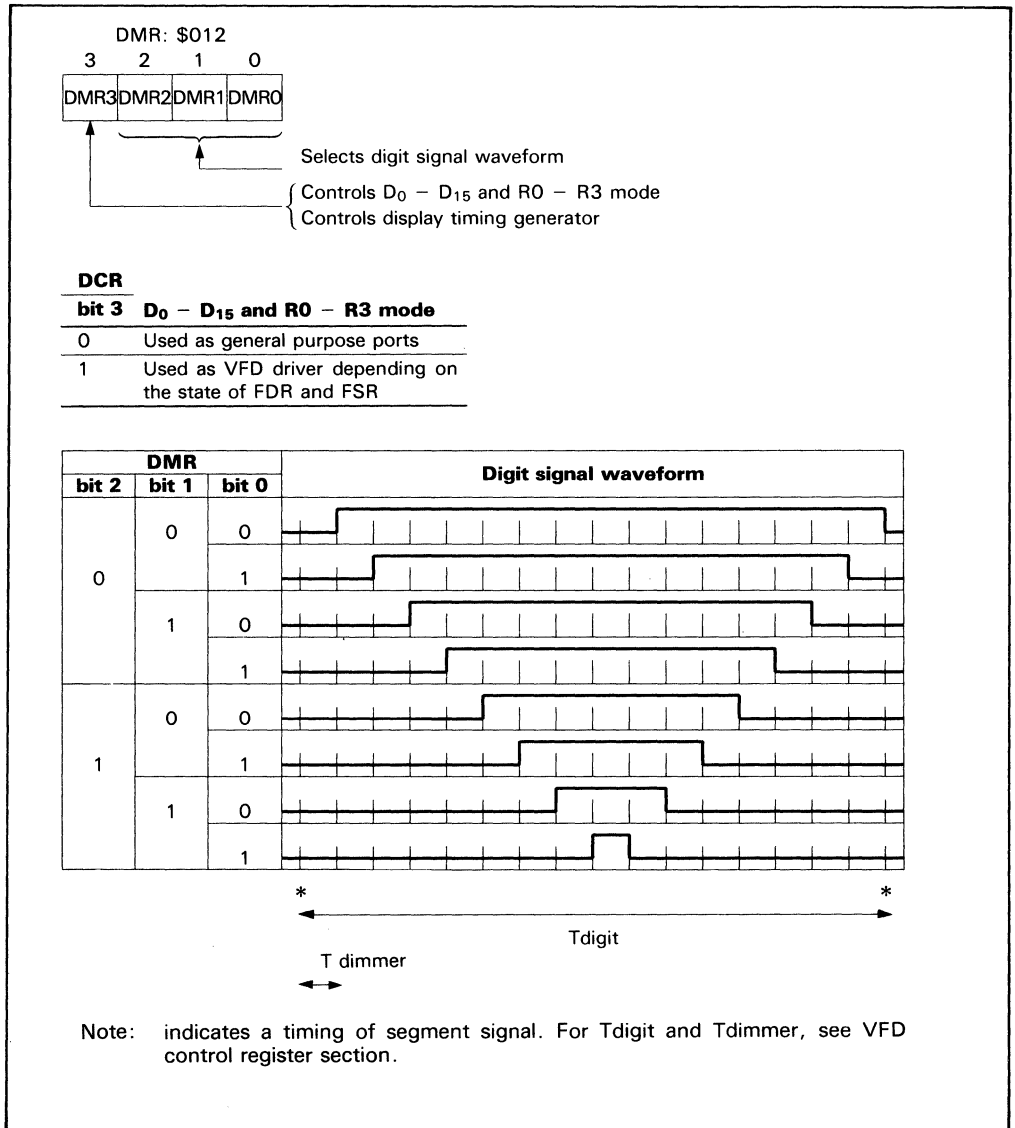


Figure 36. Dimmer Mode Register

VFD Digit Register (FDR: \$011), VFD Segment Register (FSR: \$010): The VFD digit register and the VFD segment register are 4-bit write-only registers which control the VFD driver pins. The pins selected by the these registers are used for the VFD driver or

general purpose, depending on the state of bit 3 of the dimmer mode register and the key scan flag. All other pins are used for general purpose. These registers are initialized to \$0 by the MCU reset.

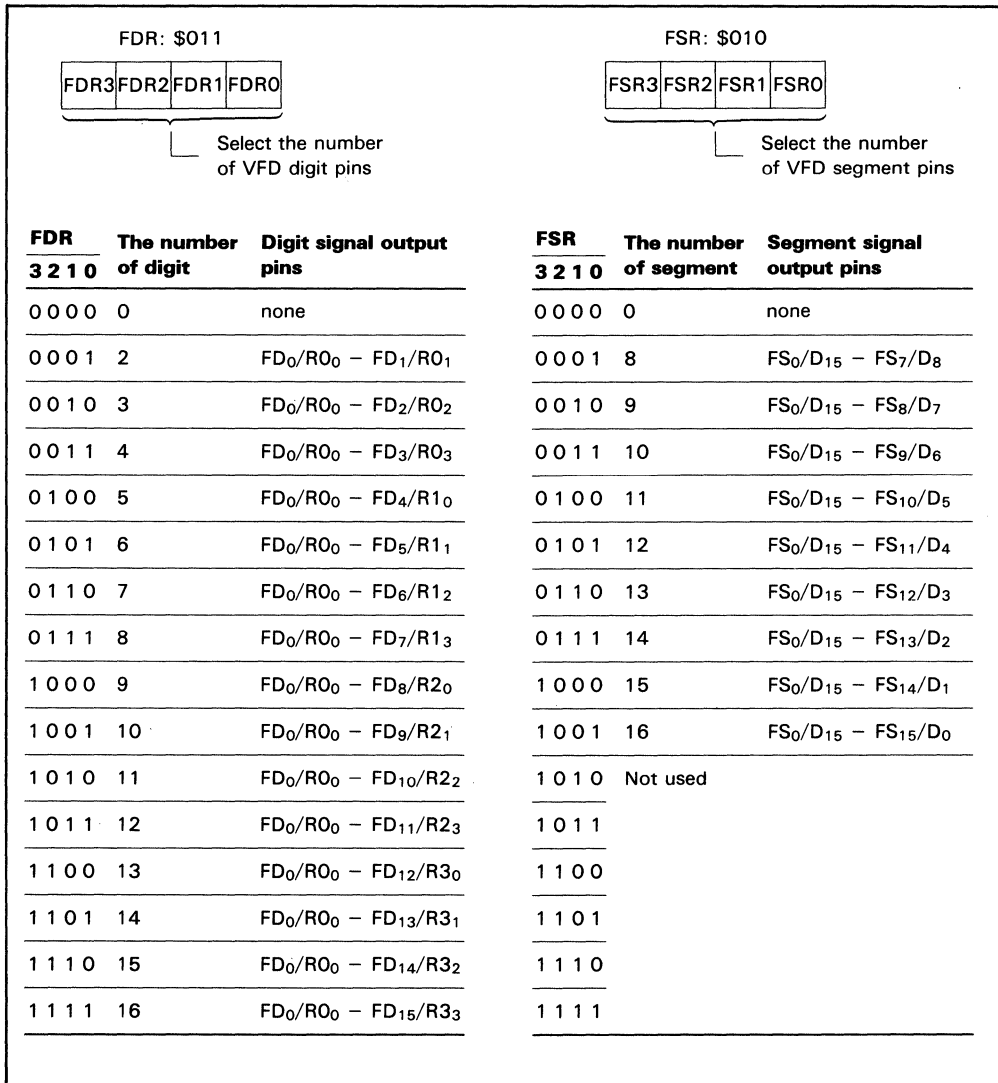


Figure 37. VFD Digit Register and Segment Register

PWM (Pulse Width Modulation) D/A Converter

The PWM D/A converter is used to generate DC voltage which controls the VTR tuner using the voltage synthesizer method. This converter provides 14-bit pulse-divided PWM (Pulse Width Modulation) which realizes high resolution and high speed response.

The D/A converter consists of four registers and a pulse width modulator. When data is written to the PWM data register 3, the data is latched into the modulator and the PWM data is then output synchronously with the internal clock signal. It should be noted that bits 2 and 3 of PWM data register 3 are invalid. Figure 39 shows the flowchart of PWM D/A converter operation.

Data Register Name and Address	Bit Number	READ/WRITE
PWM data register PWDR 3 (\$019)	2	W
PWM data register PWDR 2 (\$018)	4	W
PWM data register PWDR 1 (\$017)	4	W
PWM data register PWDR 0 (\$016)	4	W

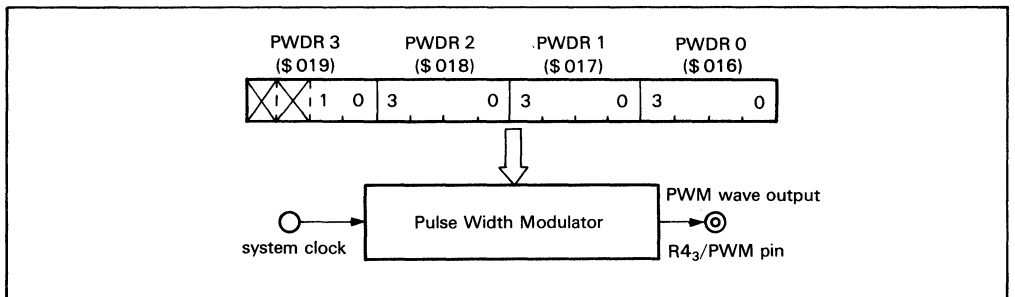


Figure 38. PWM D/A Converter Block Diagram

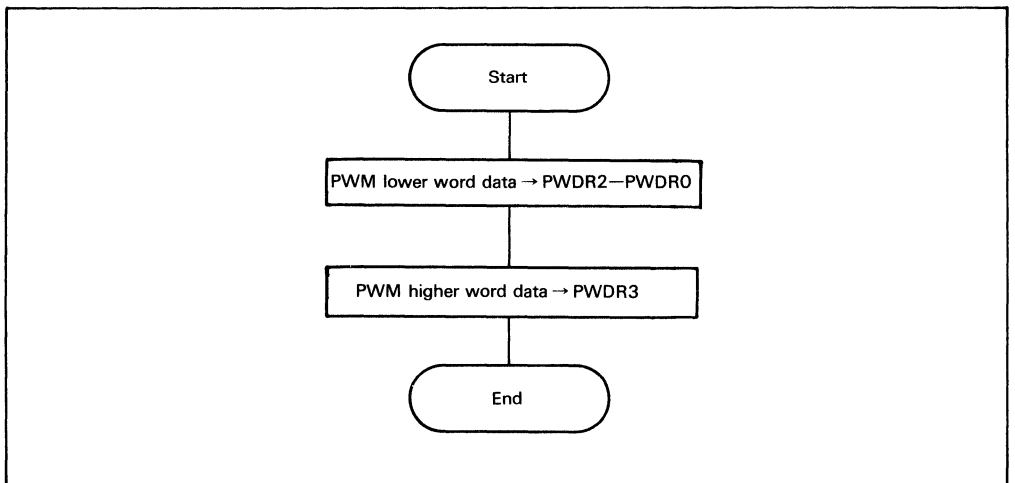
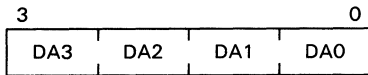


Figure 39. A Sequence of PWM D/A Converter Operation

PWM Registers

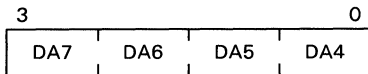
PWM data register 0 (PWDR0: \$016)

a 4-bit write-only data register



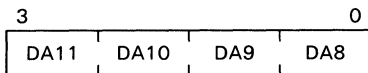
PWM data register 1 (PWDR1: \$017)

a 4-bit write-only data register



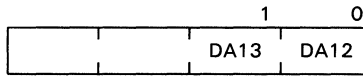
PWM data register 2 (PWDR2: \$018)

a 4-bit write-only data register



PWM data register 3 (PWDR3: \$019)

a 2-bit write-only data register



PWM Operation

Figure 40 shows the PWM waveform. One frame period has 64 clock pulses. The relationship between total pulse width at low level in one frame and the data value is represented by the following equation; in the equation, t_{cyc} indicates the instruction cycle time.

$$T_L = (\text{PWDR value} + 64) \times \frac{t_{cyc}}{2}$$

$$1 \text{ frame period} = 8192 t_{cyc}$$

$$t_{fm} = 128 t_{cyc}$$

$$\text{resolution} = \frac{t_{cyc}}{2}$$

$$t_{cyc} = 0.9536 \mu\text{s} \text{ (when using 4.1943 MHz crystal oscillator with divide-by-4)}$$

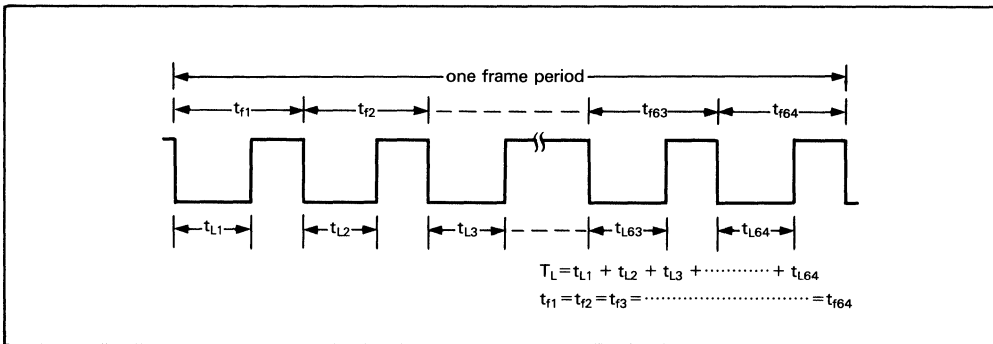


Figure 40 PWM Waveform

PROM Mode Pin Description

Table 25 and figure 41 describe the pin function in PROM mode.

Table 25. PROM Mode Signals

Pin No.	MCU mode		PROM mode		Pin No.	MCU mode		PROM mode			
DC-64S DP-64S	FP-64B	Pin name	I/O	Pin name	I/O	DC-64S DP-64S	FP-64B	Pin name	I/O	Pin name	I/O
1	59	D ₁₁ /FS ₄	I/O			33	27	R ₄₀ /SCK	I/O		
2	60	D ₁₂ /FS ₃	I/O			34	28	R ₄₁ /SI	I/O	O ₄	I/O
3	61	D ₁₃ /FS ₂	I/O			35	29	R ₄₂ /SO	I/O	O ₃	I/O
4	62	D ₁₄ /FS ₁	I/O			36	30	R ₄₃ /PWM	I/O	O ₂	I/O
5	63	D ₁₅ /FS ₀	I/O			37	31	R ₇₀ /BUZZ	I/O	O ₄	I/O
6	64	RO ₀ /FD ₀	I/O	A ₁	I	38	32	R ₇₁	I/O	O ₅	I/O
7	1	RO ₁ /FD ₁	I/O	A ₂	I	39	33	R ₇₂	I/O	O ₆	I/O
8	2	RO ₂ /FD ₂	I/O	A ₃	I	40	34	R ₇₃	I/O	O ₇	I/O
9	3	RO ₃ /FD ₃	I/O	A ₄	I	41	35	R ₈₀	I/O	O ₁	I/O
10	4	R ₁₀ /FD ₄	I/O	A ₅	I	42	36	R ₈₁	I/O	O ₀	I/O
11	5	R ₁₁ /FD ₅	I/O	A ₆	I	43	37	R ₉₀	I	V _{PP}	
12	6	R ₁₂ /FD ₆	I/O	A ₇	I	44	38	R ₉₁	I	A ₉	I
13	7	R ₁₃ /FD ₇	I/O	A ₈	I	45	39	R ₉₂	I	M ₀	I
14	8	R ₂₀ /FD ₈	I/O	A ₀	I	46	40	R ₉₃	I	M ₁	I
15	9	R ₂₁ /FD ₉	I/O	A ₁₀	I	47	41	RESET	I	RESET	I
16	10	R ₂₂ /FD ₁₀	I/O	A ₁₁	I	48	42	OSC ₂	O		
17	11	R ₂₃ /FD ₁₁	I/O	A ₁₂	I	49	43	OSC ₁	I		
18	12	RA ₀	I	V _{CC}		50	44	GND		GND	
19	13	RA ₁ /Vdisp	I			51	45	CL ₁	I	GND	
20	14	R ₃₀ /FD ₁₂	I/O	A ₁₃	I	52	46	CL ₂	O		
21	15	R ₃₁ /FD ₁₃	I/O	A ₁₄	I	53	47	TEST	I	TEST	I
22	16	R ₃₂ /FD ₁₄	I/O			54	48	D ₀ /FS ₁₅	I/O		
23	17	R ₃₃ /FD ₁₅	I/O			55	49	D ₁ /FS ₁₄	I/O		
24	18	R ₅₀	I/O	CE	I	56	50	D ₂ /FS ₁₃	I/O		
25	19	R ₅₁	I/O	OE	I	57	51	D ₃ /FS ₁₂	I/O		
26	20	R ₅₂	I/O	V _{CC}		58	52	D ₄ /FS ₁₁	I/O		
27	21	R ₅₃	I/O	V _{CC}		59	53	D ₅ /FS ₁₀	I/O		
28	22	R ₆₀ /INT ₀	I/O	O ₀	I/O	60	54	D ₆ /FS ₉	I/O		
29	23	R ₆₁ /INT ₁	I/O	O ₁	I/O	61	55	D ₇ /FS ₈	I/O		
30	24	R ₆₂ /INT ₂	I/O	O ₂	I/O	62	56	D ₈ /FS ₇	I/O		
31	25	R ₆₃ /INT ₃	I/O	O ₃	I/O	63	57	D ₉ /FS ₆	I/O		
32	26	V _{CC}				64	58	D ₁₀ /FS ₅	I/O		

- Notes: 1. I/O: Input/Output Pins, I: Input Pins, O: Output Pins
 2. Connect each pair of O₄, O₃, O₂, O₁ and O₀. Hitachi supplies the socket adapter on which these pairs are internally connected.



HD404708/HD404709/HD4074709

Pins for PROM Mode (HD4074709)

V_{PP}

Apply the programming voltage (12.5V ± 0.3 V) to V_{PP}.

CE

Program the internal PROM and input the control signal to enable verify.

OE

Input the data output control signal when verify.

A₀ – A₁₄

A₀ – A₁₄ are address input pins of the internal PROM.

O₀ – O₇

O₀ – O₇ are data bus I/O pins of the internal PROM.

M₀, M₁

These are for PROM mode specification. To put the MCU into the PROM mode, pull M₀, M₁, and TEST to low level, and RESET to high level.

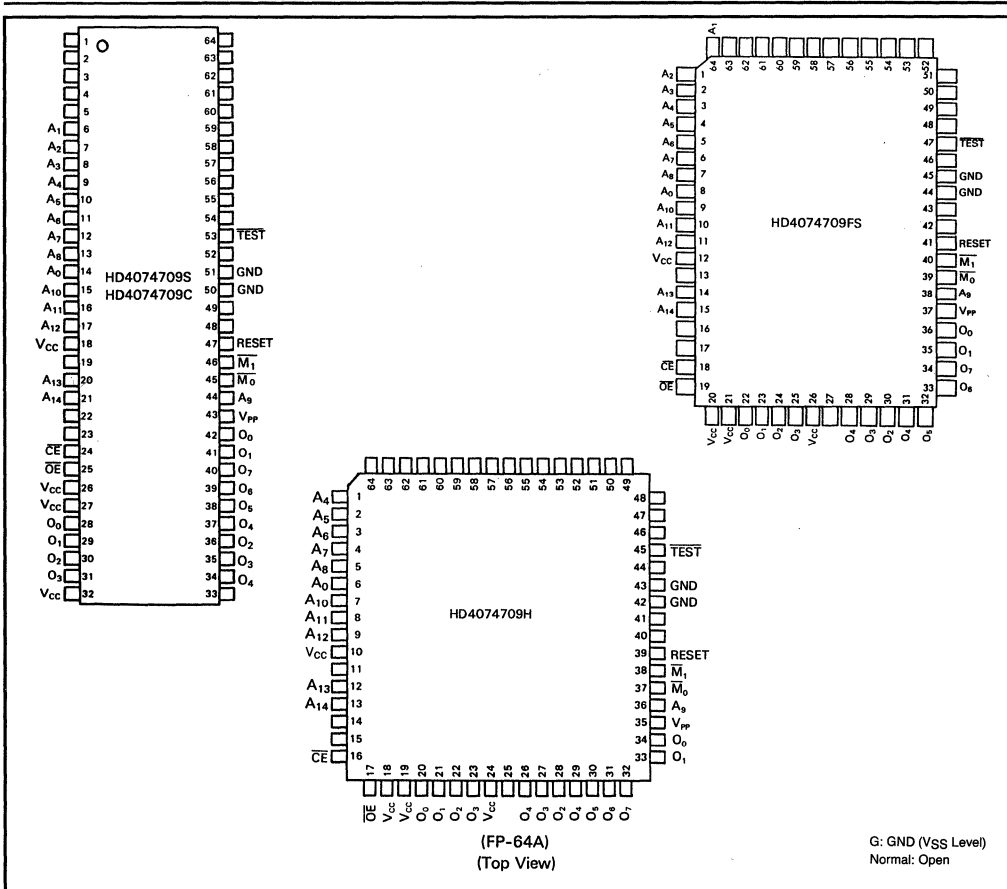


Figure 41. Pin Assignment in PROM Mode

Programmable ROM (HD4074709)

The PROM mode of the HD4074709 internally halts the MCU operation and allows the PROM to be programmed. The MCU enters the PROM mode when the TEST, M₀ and M₁ pins go to low and the RESET pin goes to high. The specifications for the PROM are the same as for the EPROM 27256; therefore, the PROM is programmed with a general-purpose ROM writer using a 64-to-28 pin socket adapter.

In order to program the PROM with using a general-purpose PROM writer, the HD4074709 incorporates the conversion circuit which divides a 10-bit HMCS series instruction into 5 higher bits and 5 lower bits. One MCU address is assigned to two PROM addresses. For example, in programming an 8k-word PROM with a general-purpose PROM writer, the user must assign 16 kbyte address locations.

Programming and Verification

The HD4074709 can perform high-speed programming without causing voltage stress or degrading data reliability. Figures 44 and 45 show the procedure for high-speed programming and timing chart, respectively. For details of PROM programming, see Precautions on PROM Programming.

Erasing

PROMs in ceramic window packages can be erased by ultraviolet light. All erased bits become 1s.

Erasing conditions are: ultraviolet (UV) light

with wavelength 2537Å with a minimum irradiation of 15W · sec/cm². These conditions are satisfied by exposing the LSI to a 12,000 μW/cm² UV source for 15-20 minutes, at a distance of 1 inch.

Precautions

1. The user must specify address locations \$0000 through \$7FFF when programming the PROM with a general-purpose PROM writer. If \$8000 or higher locations are addressed, the PROM cannot be programmed or verified. It should be noted that the plastic package type of the PROM cannot be erased and reprogrammed due to this error. The data written in unused address locations must be \$FF.
*The ceramic package type of the PROM can be erased and reprogrammed by ultraviolet light in the event of programming errors.
2. If any index of the PROM socket, socket adapter and LSI does not match, an overcurrent can occur, resulting in LSI destruction. Verify that the LSI is properly connected to the PROM writer before programming.
3. In general, the PROM is provided with a programming voltage (V_{PP}) either 12.5V or 21V. The V_{PP} of the HD4074709 PROM is 12.5V. If the user applies 21V to the PROM, this may permanently damage the LSI. The PROM writer in Intel's 27256 specifications selects 12.5V as V_{PP}.

Table 26. Mode selection

Mode	Pin			O ₀ - O ₇
	CE	OE	V _{PP}	
Programming	low	High	V _{PP}	Data input
Verify	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance



Table 27. PROM Programmiers and Socket Adapters

PROM Programmer		Socket Adapters		
Maker	Type name	Package	Maker	Type name
DATA I/O	22B 29B	DP-64S	Hitachi	HS470ESS11H
		DC-64S		
		FP-64B		
		FP-64A	Hitachi	HS470ESH01H
AVAL CORP	PKW-1000 PKW-7000	DP-64S	Hitachi	HS470ESS21H
		DC-64S		
		FP-64B		

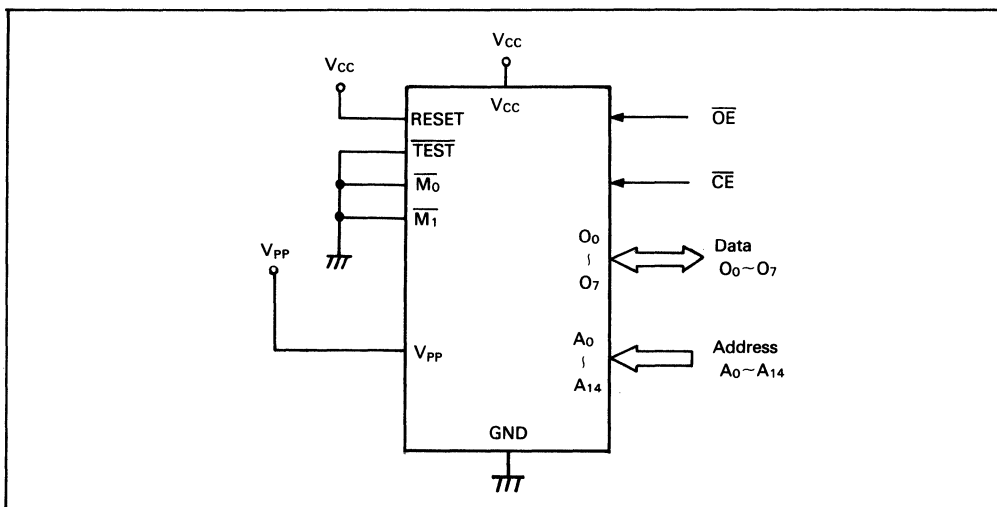


Figure 42. PROM Mode

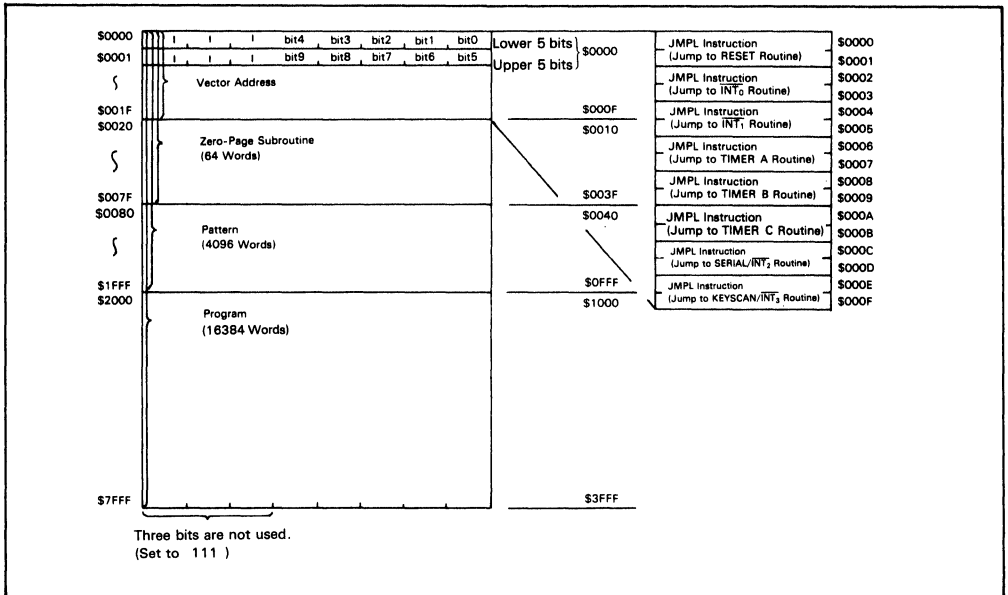


Figure 43. PROM Memory Map

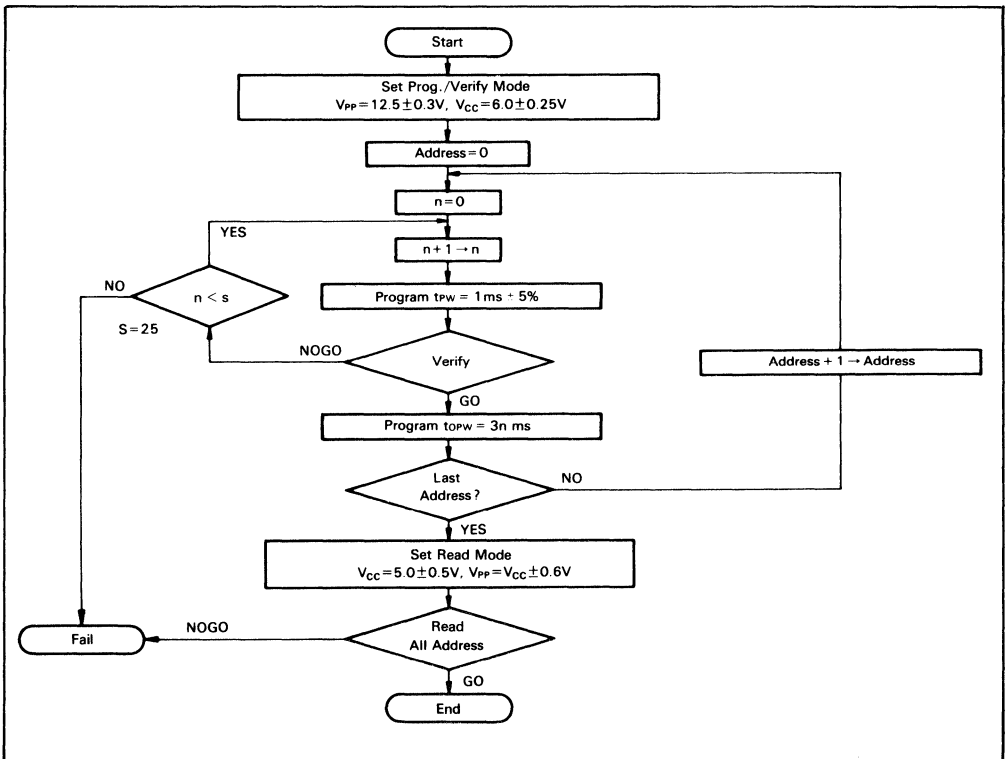


Figure 44. A Sequence of High Speed Programming

Programming Electrical Characteristics

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}	V_{IH}	2.2		$V_{CC}+0.3$	V	
Input low voltage	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{mA}$
Input leakage current	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{V}/0.5\text{V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time		t_{AS}	2			μs	Figure 45 ¹
\overline{OE} set-up time		t_{OES}	2			μs	
Data set-up time		t_{DS}	2			μs	
Address hold time		t_{AH}	0			μs	
Data hold time		t_{DH}	2			μs	
Output disable delay time		t_{DF}			130	ns	
V_{PP} set-up time		t_{VPS}	2			μs	
Program pulse width		t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming		t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time		t_{VCS}	2			μs	
Data output delay time		t_{OE}	0		500	ns	

Note : 1. Input Pulse level—0.8 to 2.2V
 Input rising/falling time $\leq 20\text{ns}$
 Timing reference level { input : 1.0V, 2.0V
 output : 0.8V, 2.0V

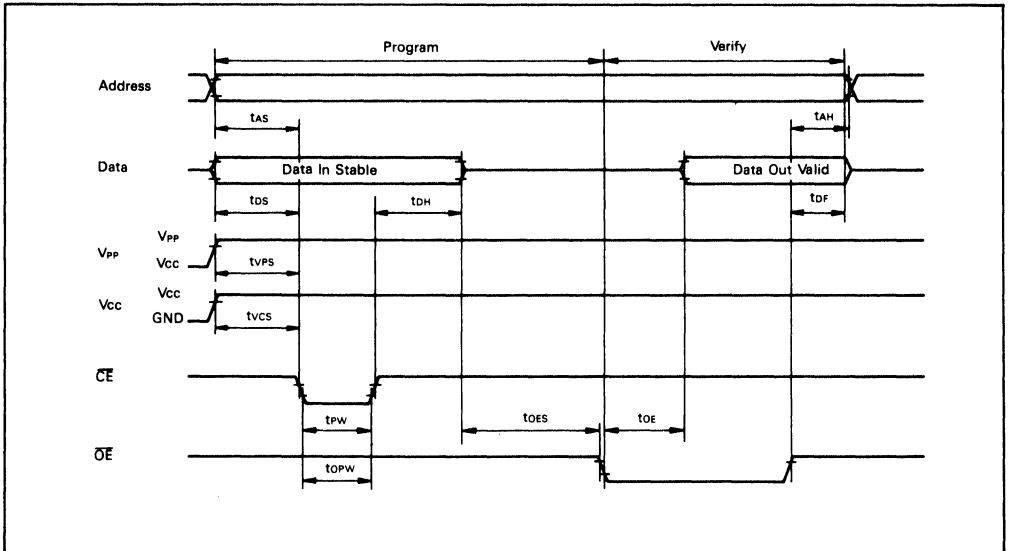


Figure 45. PROM Programming/Verifying Timing Diagram

Switching characteristics

- Input pulse level0.8V to 2.2V
- Input rising/falling time ≤ 20 ns
- Output loading1TTL Gate + 100pF
- Input/output timing reference levelOutput: 1V, 2V
Input: 0.8V, 2V

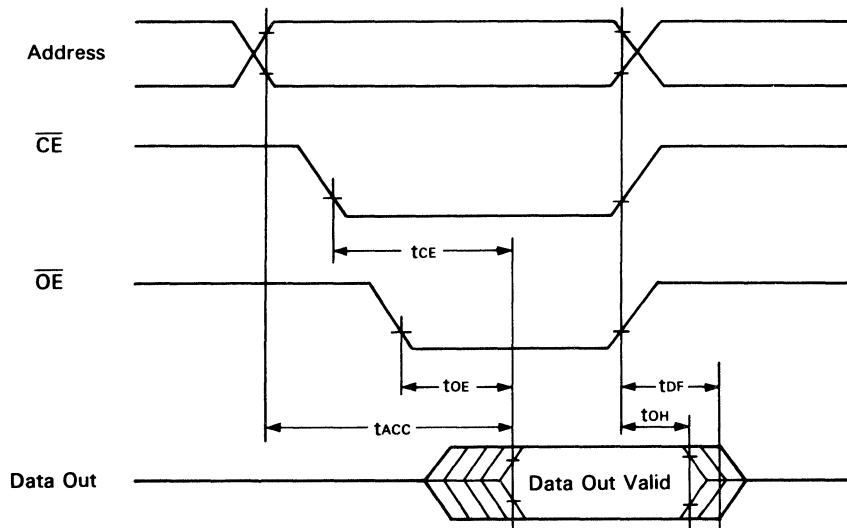


Figure 46. PROM Read Timing Diagram

Read Operation Electrical Characteristics

DC Characteristics

($V_{CC}=5\text{ V} \pm 10\%$, $V_{PP}=V_{CC} \pm 0.6\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Typ	Max	Unit	Condition
Input Leak Current	I_{LI}			1	μA	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND to } V_{CC}$
Output Leak Current	I_{LO}			1	μA	$V_{CC}=5.5\text{V}$, $V_{out}=\text{GND to } V_{CC}$
Programming V_{PP} Current	I_{PP}		1	100	μA	$V_{PP}=V_{CC}+0.6\text{V}$
Operating V_{CC} Current	I_{CC}^*			30	mA	$f=1\text{MHz}$, $I_{out}=0\text{mA}$
Input Voltage	V_{IL}	-0.3		0.8	V	
	V_{IH}	2.2		$V_{CC}+0.3$	V	
Output Voltage	V_{OL}			0.4	V	$I_{OL}=1.6\text{mA}$
	V_{OH}	2.4			V	$I_{OH}=-200\mu\text{A}$

* Input through current is excluded.

AC Characteristics

($V_{CC}=5\text{ V} \pm 10\%$, $V_{PP}=V_{CC} \pm 0.6\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise notes.)

Item	Symbol	Min	Max	Unit	Condition
Access Time	t_{ACC}		500	ns	$\overline{CE}=\overline{OE}=V_{IL}$
\overline{CE} Output Delay Time	t_{CE}		500	ns	$\overline{OE}=V_{IL}$
\overline{OE} Output Delay Time	t_{OE}	10	150	ns	$\overline{CE}=V_{IL}$
Output Disable Delay Time	t_{DF}^*	0	105	ns	$\overline{CE}=V_{IL}$
Data Output Hold Time	t_{OH}	0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

* t_{DF} is determined when the output reaches open state and output level cannot be referred.

Precautions on PROM Programming

Principles of PROM Programming/Erasing

The ZTAT microcomputer has the same type of the memory cell as the EPROM. The PROM is programmed by applying high voltage to the control gate and drain and injecting hot electrons into the floating gate, in the same way in the EPROM programming. The electrons in the floating gate remains stabilized, surrounded by the energy barrier of SiO₂ film. By this electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced as over time. This reduction is caused by:

1. Ultraviolet lightThe electrons are discharged by the ultraviolet light (erasure principle)
2. HeatThe electrons, which are excited by heat, are discharged
3. Application of high voltage...The number of electrons is reduced due to the high voltage which is applied to the control gate and drain

If there is any failure in the oxide film, the charge is markedly reduced; however, in general, such reduction does not occur, since devices which failed are usually excluded

during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PF}) and the longer the program pulse width (t_{FW}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a P-N junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise causes a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

1. Confirm that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
2. Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

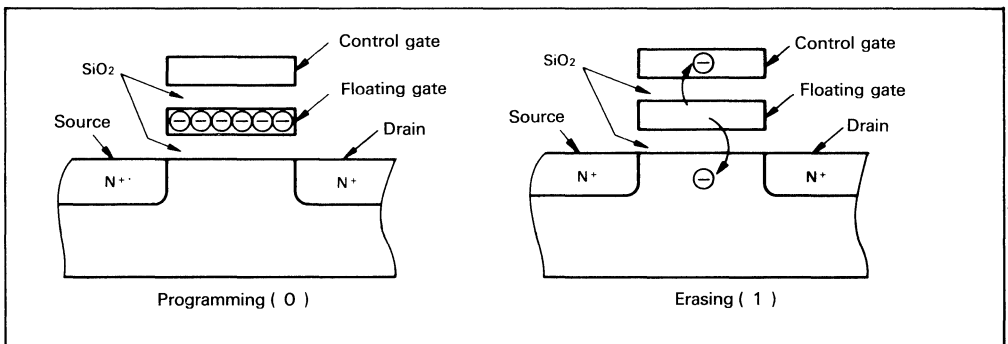


Figure 47. Cross Section of PROM Memory Cell

PROM Reliability after Programming

In general, semiconductor devices retain their reliability, if some initial failures can be rejected. Initial failures can be rejected by adequate screening. Baking the device under high-temperature conditions is a screening method which eliminates initial short-time data hold failures in the memory cell. (See Principles of PROM Programming/Erasing). ZTAT microcomputer devices realize good reliability because they have been subjected to such screening during the water fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 48. shows the recommended screening procedure.

Window-Type Package Precautions

Glass Erasure Window: If the glass window comes in contact with plastic or anything with a static charge, the LSI may malfunction due to the electrostatic charge on the surface of the window. If this occurs, exposing the LSI to ultraviolet light for a few minutes neutralizes the charge, and restores the LSI to normal operation. However, charge stored in the floating gate decreases at the same time, so reprogramming is recommended.

Electrostatic charge buildup on the window is a fundamental cause of malfunctions. Measures for its prevention are the same as those for preventing electrostatic breakdown:

1. Operators should be grounded when handling equipment.
2. Do not rub the glass window with plastics.
3. Be careful of coolant sprays, which may contain a few ions.
4. The ultraviolet shading label (which includes conductive material) effectively neutralizes charge.

Ultraviolet Shading Label: If the LSI is exposed to fluorescent light or sunlight, its memory contents may be erased by the small quantity of ultraviolet light in these sources. In strong light, the MCU may fail under the influence of photocurrent. To prevent these problems, it is recommended that the device be used with an ultraviolet shading label covering the erasure window after programming.

Special labels are sold for this purpose. They contain metal to absorb ultraviolet light. When choosing a label, note the following:

1. Adhesion (mechanical intensity)—Re-use and dust reduce adhesion. Peeling off a label may cause static electricity. Therefore, erasing and rewriting is recom-

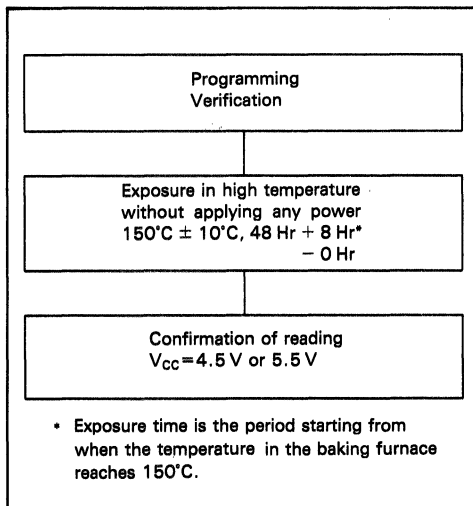


Figure 48. Recommended Screening Procedure

(note) If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter when using the window-package-type of the EPROM. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

- mended after peeling. Sticking a new label over the old one is better than replacing a label.
2. Allowable temperature range—The allowable environmental temperature range of the label should be noted. If it is used under conditions outside this range, the paste may stiffen or adhere to the label, causing paste to remain on the

- window when the label is removed.
3. Moisture resistance—The allowable moisture range and environmental conditions of the label should be noted. It is difficult to find a shade label applicable to all conditions. The proper label should be selected depending on the intended use of the MCU.

Addressing Mode

RAM Addressing Mode

As shown in figure 49, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register

register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

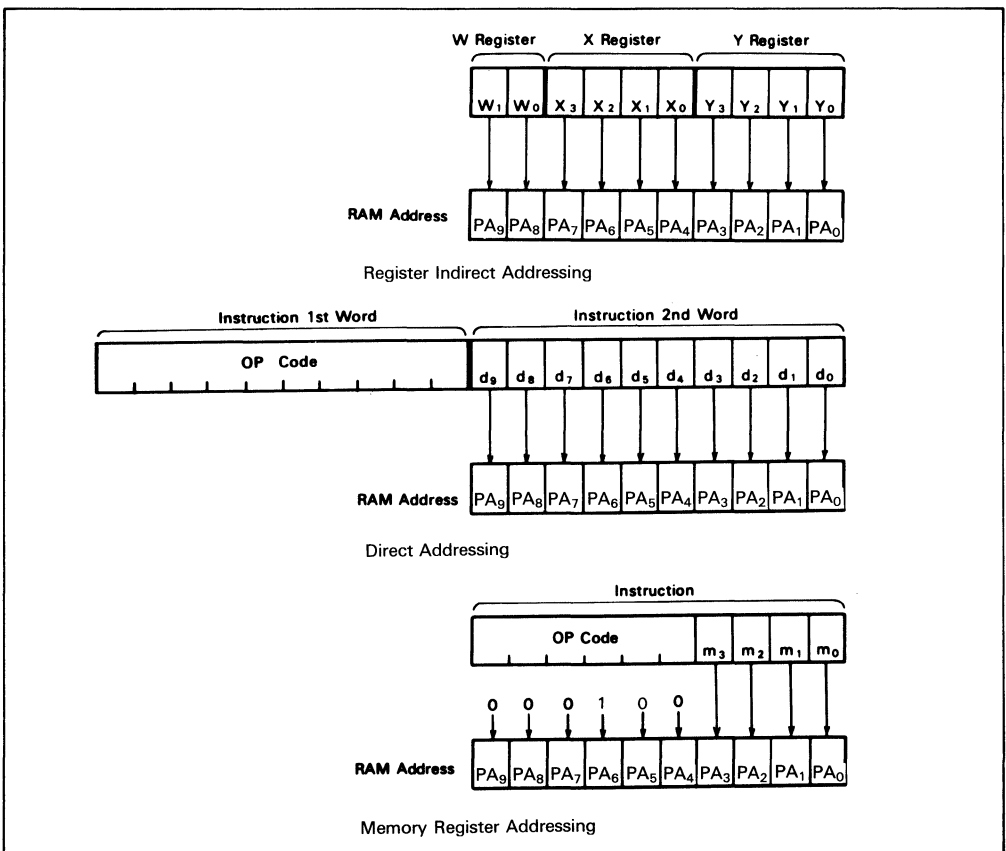


Figure 49. RAM Addressing Modes



Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 50.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on page boundary ($256n + 255$) (figure 52), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Conse-

quently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 51). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B Register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

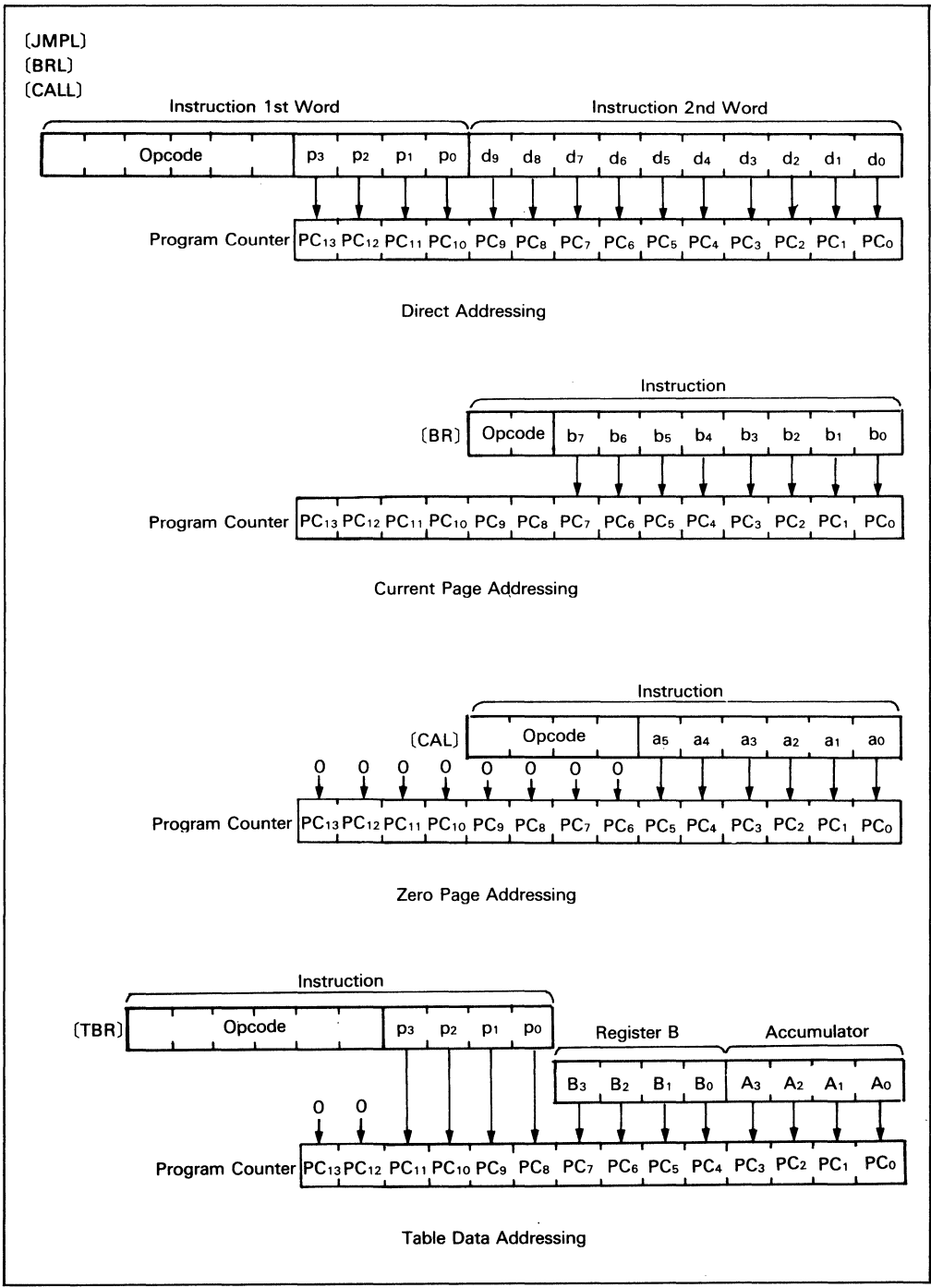


Figure 50. ROM Addressing Modes

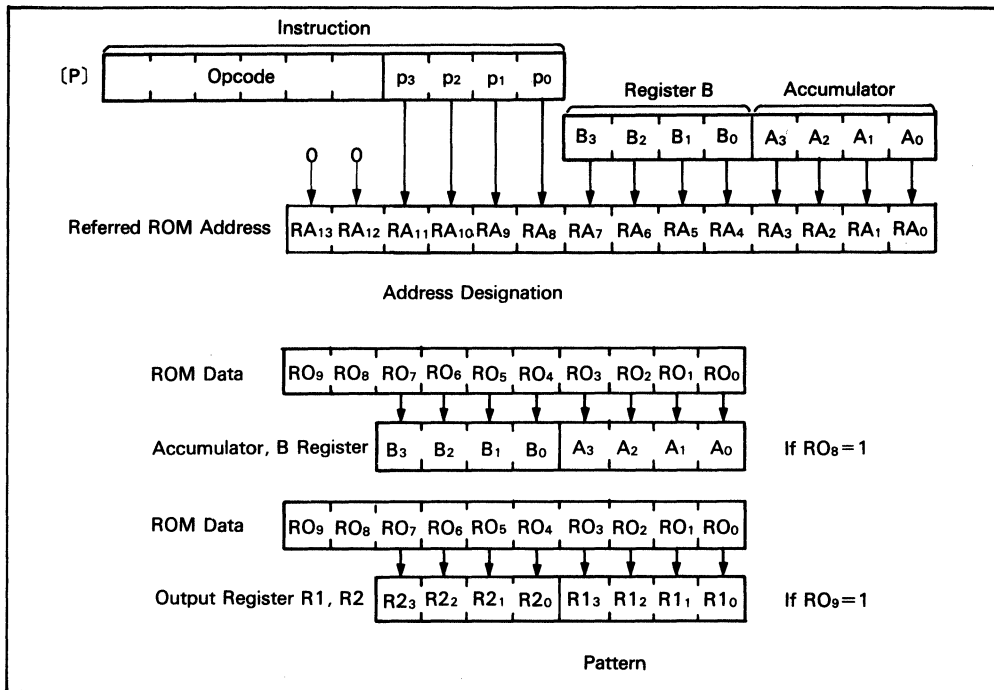


Figure 51. P Instruction

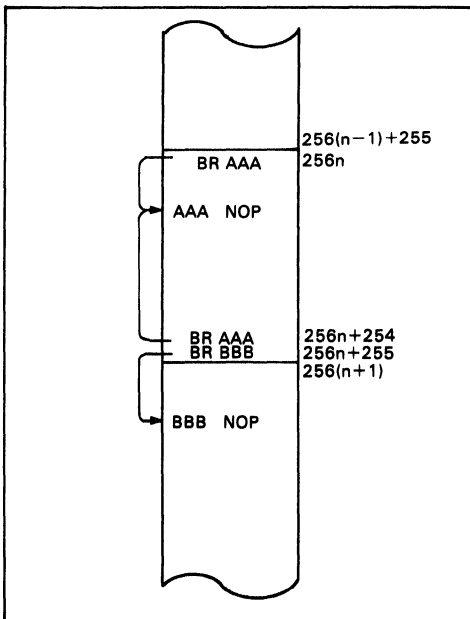


Figure 52. The Branch Destination by BR Instruction on the Boundary Between Pages

Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows:

- | | |
|---------------------------------------|---------------------------------------|
| (1) Immediate instructions | (6) Compare instructions |
| (2) Register-to-register instructions | (7) RAM bit manipulation instructions |
| (3) RAM address instructions | (8) ROM address instructions |
| (4) RAM register instructions | (9) Input/output instructions |
| (5) Arithmetic instructions | (10) Control instructions |
- Tables 28-37 list their functions, and table 38 is an opcode map.

Table 28. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 29. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 30. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 31. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X → SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have four mnemonics and four object codes for each (example of LAM (XY) is given below).

The op-code X or Y is assembled as follows:

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

- (2) The instructions with (X) have two mnemonics and two object codes for each (example of LMAIY(X) is given below).

The op-code X is assembled as follows:

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 32. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A+i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B+1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B-1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M+A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M+A+CA → A OVF→CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M+A+CA→A OVF→CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M-A- \bar{CA} →A NB→CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M-A- \bar{CA} →A NB→CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR



Table 33. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \neq M$	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \neq M$	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	$A \neq M$	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \neq M$	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	$B \neq M$	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	$Y \neq i$	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \leq M$	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \leq M$	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	$A \leq M$	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \leq M$	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	$B \leq M$	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	$A \leq i$	NB	1/1

Table 34. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	$1 \rightarrow M(n)$		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$1 \rightarrow M(n)$		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	$0 \rightarrow M(n)$		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$0 \rightarrow M(n)$		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		$M(n)$	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		$M(n)$	2/2

Table 35. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA recovery	ST	1/3

Table 36. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 37. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode/ Watch mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/Watch mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1



Table 38. Opcode Map

R8		0																1																
R9	H	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	NOP	XSP	XSP	XSP	XSP	ANXY	EM				AM				ORM			LAW								ANEMD			AMD			ORMD
1	RTN	RTN				ALEM					AMC				EORM			LWA							ALEMCD			AMCD			EORMD			
2																																		
3																																		
4	LBM(XY)					BNEM					LAB				IB			COMB							OR		STS			SBY	STOP			
5	LMAY(X)					AYY					LASPY				IY																			
6	NEGA					RED					LASPY																							
7																																		
8	XMA(XY)																																	
9	LAM(XY)																																	
A	ROT	ROT									DAA				DAS																			
B																																		
C	XMB(XY)																																	
D	LMADY(X)																																	
E	TD																																	
F	LWI																																	
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 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction (2-word/2-cycle)
 2-word/2-cycle Instruction

 is not available, the undefined instruction.



Absolute Maximum Ratings

Item	Symbol	Constant	Unit	Notes
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14.0	V	12
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 42$ to $V_{CC} + 0.3$	V	4
Total Allowance of Input Current	ΣI_O	50	mA	5
Total Allowance of Output Current	$-\Sigma I_O$	150	mA	6
Maximum Input Current	I_O	.15	mA	7, 8
Maximum Output Current	$-I_O$	4	mA	9, 10
		30	mA	9, 11
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	-25 to + 80	°C	12

- Notes:
1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. All voltages are with respect to GND.
 3. Standard pins
 4. High voltage pins
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. R4-R8
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. R4-R8
 11. D₀-D₁₅, R₀-R₃
 12. HD4074709



Electrical Characteristics

HD404708, HD404709 Electrical Characteristics

DC Characteristics

($V_{CC} = 3\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK,INT ₀ - INT ₃	0.8 V_{CC}	-	$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}	-	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	-	$V_{CC} + 0.3$	V	$V_{CC}=3.5\text{V to }6.0\text{V}$	
			$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, SCK,INT ₀ - INT ₃	- 0.3	-	0.2 V_{CC}	V		
		SI	- 0.3	-	0.3 V_{CC}	V		
		OSC ₁	- 0.3	-	0.5	V	$V_{CC}=3.5\text{V to }6.0\text{V}$	
			- 0.3	-	0.3	V		
Output High Voltage	V_{OH}	SCK,SO, PWM,BUZZ	$V_{CC} - 1.0$	-	-	V	$-I_{OH}=1.0\text{mA}$, $V_{CC}=3.5\text{V to }6.0\text{V}$	
			$V_{CC} - 0.5$	-	-	V	$-I_{OH}=0.5\text{mA}$, $V_{CC}=3.5\text{V to }6.0\text{V}$	
							$-I_{OH}=0.3\text{mA}$	
Output Low Voltage	V_{OL}	SCK,SO, PWM,BUZZ	-	-	0.4	V	$I_{OL}=1.6\text{mA}$, $V_{CC}=3.5\text{V to }6.0\text{V}$	
							$I_{OL}=0.4\text{mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, SCK,INT ₀ - INT ₃ SI,SO, PWM,BUZZ OSC ₁	-	-	1	μA	$V_{in}=0\text{V to }V_{CC}$	1
Power Dissipation in Active Mode	I_{CC}	V_{CC}	-	-	5.0	mA	$V_{CC}=5\text{V}$, $f_{osc}=4\text{MHz}$, Divide-by-4	2,5,8
					8.0	mA		9
			-	-	3.0	mA	$V_{CC}=3\text{V}$, $f_{osc}=2\text{MHz}$, Divide-by-4	2,5,8
					4.5	mA		9
Power Dissipation in Standby Mode	I_{SBY}	V_{CC}	-	-	2.0	mA	$V_{CC}=5\text{V}$, $f_{osc}=4\text{MHz}$, Divide-by-4	3,5
							1.0	mA



Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Power Dissipation in Subactive Mode	I_{sub}	V_{CC}	–	–	30	μA	$V_{CC}=3V$, when using 32.768kHz crystal $V_{in}(\overline{TEST})=V_{CC}-0.3V$ to V_{CC} , $V_{in}(\overline{RESET})=0V$ to 0.3V	4, 6, 8
			–	–	80	μA		9
Power Dissipation in Watch Mode	I_{watch}	V_{CC}	–	–	15	μA	$V_{CC}=3V$, when using 32.768kHz crystal, $V_{in}(\overline{TEST})=V_{CC}-0.3V$ to V_{CC} , $V_{in}(\overline{RESET})=0V$ to 0.3V	4, 6, 7
Power Dissipation in Stop Mode	I_{stop}	V_{CC}	–	–	10	μA	$V_{in}(\overline{TEST})=V_{CC}-0.3V$ to V_{CC} , $V_{in}(\overline{RESET})=0V$ to 0.3V not using 32.768kHz crystal	4
Watch Mode Retain Voltage	V_{watch}	V_{CC}	3.5	–	6.0	V	$V_{CC}=3.5V$ to 6V	6, 7
			3.0	–	6.0	V		
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2	–	–	V	not using 32.768kHz crystal	

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is reset and input/output current does not flow.
Pin conditions:
 - RESET, \overline{TEST} V_{CC}
 - R4-R9..... V_{CC}
 - D₀-D₁₅, R0-R3, RA..... V_{disp}
 - The timer/counter is enabled and input/output current does not flow.
MCU conditions:
 - I/O.....same as at reset
 - Serial interface.....halt
 - Standby mode
 Pin conditions:
 - RESET.....GND
 - \overline{TEST} V_{CC}
 - R4-R9..... V_{CC}
 - D₀-D₁₅, R0-R3, RA..... V_{disp}
 - Excluding pull-down MOS current to V_{disp} .
 - Power dissipation in MCU operation or in Standby mode is in proportion to f_{osc} ; each current value when $f_{osc}=x$ [MHz] is given by the following equation:
Maximum value ($f_{osc}=x$ [MHz])= $x/4 \times$ Max. value ($f_{osc}=4$ [MHz])
 - Applied to the product with 32 kHz CPU operation selected by optional function.
 - Applied to the product with no 32 kHz CPU operation, TIME-BASE operation selected by optional function.
 - HD404708
 - HD404709

Input/Output Characteristics for Standard Pins

($V_{CC} = 3\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	R4-R9	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	R4-R9	- 0.3	-	$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	R4-R8	$V_{CC} - 1.0$	-	-	V	$-I_{OH} = 1.0\text{mA}$, $V_{CC} = 3.5\text{V to }6.0\text{V}$	
			$V_{CC} - 0.5$	-	-	V	$-I_{OH} = 0.5\text{mA}$, $V_{CC} = 3.5\text{V to }6.0\text{V}$	
							$-I_{OH} = 0.3\text{mA}$	
Output Low Voltage	V_{OL}	R4-R8	-	-	0.4	V	$I_{OL} = 1.6\text{mA}$, $V_{CC} = 3.5\text{V to }6.0\text{V}$ $I_{OL} = 0.4\text{mA}$	
Input/Output Leakage Current	$ I_{IL} $	R4-R9	-	-	1	μA	$V_{in} = 0\text{V to }V_{CC}$	1
Pull-Up MOS Current	- I_P	R4-R9	30	70	150	μA	$V_{CC} = 5\text{V}, V_{in} = 0\text{V}$	2
			10	20	50	μA	$V_{CC} = 3\text{V}, V_{in} = 0\text{V}$	

- Notes: 1. Pull-up MOS current and output buffer current are excluded.
 2. Applied to I/O pins with pull-up MOS selected by mask option.

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Input/Output Characteristics for High Voltage Pins

($V_{CC} = 3\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	D ₀ -D ₁₅ , RA, R ₀ -R ₃	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₁₅ , RA, R ₀ -R ₃	$V_{CC} - 40\text{V}$	-	$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D ₀ -D ₁₅ , R ₀ -R ₃	$V_{CC} - 3.0$	-	-	V	$-I_{OH} = 15\text{mA}$, $V_{CC} = 5\text{V} \pm 20\%$	
			$V_{CC} - 2.0$	-	-	V	$-I_{OH} = 10\text{mA}$, $V_{CC} = 5\text{V} \pm 20\%$	
			$V_{CC} - 1.0$	-	-	V	$-I_{OH} = 4\text{mA}$	
Output Low Voltage	V_{OL}	D ₀ -D ₁₅ , R ₀ -R ₃	-	-	$V_{CC} - 34$	V	$V_{disp} = V_{CC} - 40\text{V}$	1
		D ₀ -D ₁₅ , R ₀ -R ₃	-	-	$V_{CC} - 37$	V	$150\text{k}\Omega$ to $V_{CC} - 40\text{V}$	2
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₁₅ , RA, R ₀ -R ₃	-	-	20	μA	$V_{in} = V_{CC} - 40\text{V}$ to V_{CC}	3
Pull-Down MOS Current	I_d	D ₀ -D ₁₅ , RA, R ₀ -R ₃	200	400	800	μA	$V_{disp} = V_{CC} - 35\text{V}$ $V_{in} = V_{CC}$	4

- Notes: 1. Applied to I/O pins with pull-down MOS selected by mask option.
Applied to I/O pins without pull-down MOS (PMOS open drain) selected by mask option.
2. Pull-down MOS current and output buffer current are excluded.
Applied to I/O pins with pull-down MOS selected by mask option.

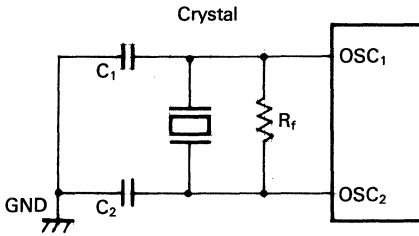


AC Characteristics

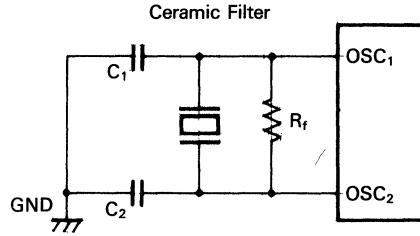
($V_{CC} = 3\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note	
Oscillation Frequency (Divide-by-4)	f_{OSC}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	$V_{CC} = 3.5\text{ V to }6\text{ V}$	7	
			1.6	4	4.5	MHz			
			0.4	2	2.25	MHz			7
			1.6	2	2.25	MHz			
Oscillation Frequency (Divide-by-8)	f_{CL}	CL ₁ , CL ₂	–	32.768	–	kHz			
Instruction Cycle Time	t_{cyc}		0.89	1	10	μs	$V_{CC} = 3.5\text{ V to }6\text{ V}$	7	
			0.89	1	2.5	μs			
			1.78	2	10	μs			7
			1.78	2	2.5	μs			
Instruction Cycle Time	t_{SUBcyc}		–	244.14	–	μs		8	
Oscillation Stabilization (Crystal)	t_{RC}	OSC ₁ , OSC ₂	–	–	40	ms	$V_{CC} = 3.5\text{ V to }6\text{ V}$	1	
			–	–	60	ms			
Oscillation Stabilization (Ceramic Filter)	t_{RC}	OSC ₁ , OSC ₂	–	–	20	ms	$V_{CC} = 3.5\text{ V to }6\text{ V}$	1	
			–	–	60	ms			
Oscillation Stabilization	t_{RC}	CL ₁ , CL ₂	–	–	2	s		2, 8, 9	
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92	–	–	ns	$V_{CC} = 3.5\text{ V to }6\text{ V}$	3	
			203	–	–	ns			
External Clock Rising, Falling Time	t_{CPr} , t_{CPf}	OSC ₁	–	–	20	ns	$V_{CC} = 3.5\text{ V to }6\text{ V}$	3	
			–	–	20	ns			
INT ₀ High, Low Level Width	t_{IOH} , t_{IOL}	$\overline{\text{INT}}_0$	2	–	–	$t_{cyc}/$ t_{SUBcyc}		4, 6, 8, 9	
INT ₁ High, Low Level Width	t_{11H} , t_{11L}	$\overline{\text{INT}}_1$ – $\overline{\text{INT}}_3$	2	–	–	t_{cyc}		4	
RESET High Level Width	t_{RSTH}	RESET	2	–	–	t_{cyc}		5	
Input Capacitance	C_{in}	All pins	–	–	30	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$		
RESET Falling Time	t_{RSTf}	RESET	–	–	20	ms		5	

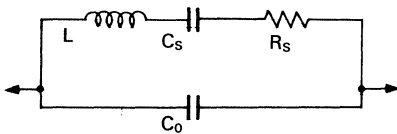
Notes: 1. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V (3.5V, in case of $V_{CC} = 3.5\text{ V} - 6.0\text{ V}$) after Power on, or after RESET goes high. RESET must be kept high for at least t_{RC} to obtain oscillation time. Oscillation stabilization time depends on the crystal or ceramic filter's circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal or ceramic filter marker to determine the circuit parameter.



Crystal
 Xtal: Under the equivalent circuit
 $R_f: 1\text{M}\Omega \pm 20\%$
 $C_1: 10\text{pF} \pm 20\%$
 $C_2: 10\text{pF} \pm 20\%$

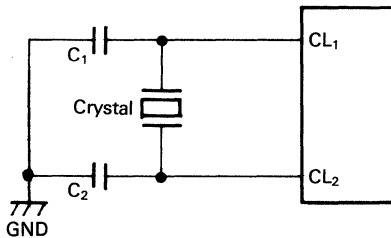


Ceramic Filter
 Ceramic Filter: CSA4.00MG (MURATA)
 $R_f: 1\text{M}\Omega \pm 20\%$
 $C_1: 30\text{pF} \pm 20\%$
 $C_2: 30\text{pF} \pm 20\%$

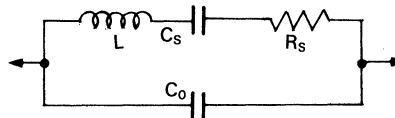


$C_0 = 7\text{pF max}$
 $R_s = 100\Omega \text{ max}$
 $f = 1.0 - 4.5\text{MHz}$

- Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V after power on. Oscillation stabilization time depends on the crystal circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal maker to determine the circuit parameter.



Crystal
 Xtal: MX38T (Nihon denpa kogyo)
 Right the equivalent circuit
 $C_1: 15\text{pF} \pm 5\%$
 $C_2: 15\text{pF} \pm 5\%$



$C_0 = 1.5\text{pF typ}$
 $R_s = 14\text{k}\Omega \text{ typ}$
 $f = 32.768\text{kHz}$

- See figure 53.
- See figure 54. Unit t_{cyc} is applied when MCU is Standby or Active mode.
- See figure 55.
- See figure 54. Unit t_{SUBcyc} is applied when MCU is in Watch or Sub-Active mode. $t_{SUBcyc} = 244.14\mu\text{s}$ (when using 32.768kHz crystal oscillator)
- Apply the data in parenthesis when subsystem oscillator is not used.
- Applied to the product with 32kHz CPU operation selected by optional function.
- Applied to the product with no 32kHz CPU operation, TIME-BASE operation selected by optional function.

Serial Interface Timing Characteristics

($V_{CC} = 3V$ to $6V$, $GND = 0V$, $V_{disp} = V_{CC} - 40V$ to V_{CC} , $T_a = -20$ to $+75^\circ C$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK}	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH} , t_{SCKL}	\overline{SCK}	0.4	–	–	t_{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr} , t_{SCKf}	\overline{SCK}	–	–	80	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	\overline{SCK}	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH} , t_{SCKL}	\overline{SCK}	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr} , t_{SCKf}	\overline{SCK}	–	–	80	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	600	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	200	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	400	–	–	ns		1

- Notes: 1. See figure 56.
 2. See figure 57.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

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(V_{CC} = 3.5 V to 6 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t _{S_{cyc}}	$\overline{\text{SCK}}$	1	–	–	t _{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t _{S_{CKH}} , t _{S_{CKL}}	$\overline{\text{SCK}}$	0.4	–	–	t _{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t _{S_{CKr}} , t _{S_{CKf}}	$\overline{\text{SCK}}$	–	–	40	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t _{S_{CKHD}}	$\overline{\text{SCK}}$	1	–	–	t _{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t _{S_{CKH}} , t _{S_{CKL}}	$\overline{\text{SCK}}$	0.4	–	–	t _{cyc}		1
Input Transfer Clock Rising, Falling Time	t _{S_{CKr}} , t _{S_{CKf}}	$\overline{\text{SCK}}$	–	–	40	ns		1
Serial Output Data Delay Time	t _{D_{SO}}	SO	–	–	300	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t _{S_{SI}}	SI	100	–	–	ns		1
Serial Input Data Hold Time	t _{H_{SI}}	SI	200	–	–	ns		1

- Notes: 1. See figure 56.
 2. See figure 57.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.



Electrical Characteristics

HD4074709 Electrical Characteristics

DC Characteristics

($V_{CC} = 3\text{ V to } 5.5\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to } V_{CC}$, $T_a = -20\text{ to } +75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK,INT ₀ - INT ₃	0.8 V_{CC}	-	$V_{CC} + 0.3$	V		
		SI	0.7 V_{CC}	-	$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$	-	$V_{CC} + 0.3$	V	$V_{CC}=3.5\text{V to } 5.5\text{V}$	
			$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, SCK,INT ₀ - INT ₃	- 0.3	-	0.2 V_{CC}	V		
		SI	- 0.3	-	0.3 V_{CC}	V		
		OSC ₁	- 0.3	-	0.5	V	$V_{CC}=3.5\text{V to } 5.5\text{V}$	
			- 0.3	-	0.3	V		
Output High Voltage	V_{OH}	SCK,SO, PWM,BUZZ	$V_{CC}-1.0$	-	-	V	$-I_{OH}=1.0\text{mA}$ $V_{CC}=3.5\text{V to } 5.5\text{V}$	
			$V_{CC}-0.5$	-	-	V	$-I_{OH}=0.5\text{mA}$ $V_{CC}=3.5\text{V to } 5.5\text{V}$	
							$-I_{OH}=0.3\text{mA}$	
Output Low Voltage	V_{OL}	SCK,SO, PWM,BUZZ	-	-	0.4	V	$I_{OL}=1.6\text{mA}$ $V_{CC}=3.5\text{V to } 5.5\text{V}$	
							$I_{OL}=0.4\text{mA}$	
Input/Output Leakage Current	$ I_{IL} $	RESET, SCK,INT ₀ - INT ₃ SI,SO, PWM,BUZZ OSC ₁	-	-	1	μA	$V_{in}=0\text{V to } V_{CC}$	1
Power Dissipation in Active Mode	I_{CC}	V_{CC}	-	-	8.0	mA	$V_{CC}=5\text{V}$, $f_{osc}=4\text{MHz}$ Divide-by-4	2,4
			-	-	4.5	mA	$V_{CC}=3\text{V}$, $f_{osc}=2\text{MHz}$ Divide-by-4	2,4
Power Dissipation in Standby Mode	I_{SBY}	V_{CC}	-	-	2.0	mA	$V_{CC}=5\text{V}$, $f_{osc}=4\text{MHz}$ Divide-by-4	3,4
			-	-	1.0	mA	$V_{CC}=3\text{V}$, $f_{osc}=2\text{MHz}$ Divide-by-4	3,4

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Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Power Dissipation in Subactive Mode	I_{sub}	V_{CC}	–	–	150	μA	$V_{CC}=3V$, when using 32.768kHz crystal, $V_{in}(TEST)=V_{CC}-0.3V$ to V_{CC} , $V_{in}(RESET)=0V$ to 0.3V	
Power Dissipation in Watch Mode	I_{watch}	V_{CC}	–	–	15	μA	$V_{CC}=3V$, when using 32.768kHz crystal, $V_{in}(TEST)=V_{CC}-0.3V$ to V_{CC} , $V_{in}(RESET)=0V$ to 0.3V	
Power Dissipation in Stop Mode	I_{stop}	V_{CC}	–	–	10	μA	$V_{in}(TEST, R90)=V_{CC}-0.3V$ to V_{CC} , $V_{in}(RESET)=0V$ to 0.3V not using 32.768kHz crystal	
Watch Mode Retain Voltage	V_{watch}	V_{CC}	3.5	–	5.5	V	$V_{CC}=3.5V$ to 5.5V	
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2	–	–	V	not using 32.768kHz crystal	

- Notes:
- Excluding Pull-up MOS current and output buffer current
 - The MCU is reset and input/output current does not flow.
Pin conditions:
 - RESET, TEST..... V_{CC}
 - R4-R9..... V_{CC}
 - D₀-D₁₅, R0-R3, RA..... V_{disp}
 - The timer/counter is enabled and input/output current does not flow.
MCU Conditions:
 - I/O.....same as at reset
 - Serial interface.....halt
 - Standby mode
 Pin conditions:
 - RESET.....GND
 - TEST..... V_{CC}
 - R4-R9..... V_{CC}
 - D₀-D₁₅, R0-R3, RA..... V_{disp}
 - Power dissipation in MCU operation or in Standby mode is in proportion to f_{osc} ; each current value when $f_{osc}=x$ [MHz] is given by the following equation:
Maximum value ($f_{osc}=x$ [MHz])= $x/4 \times$ Max. value ($f_{osc}=4$ [MHz])



Input/Output Characteristics for Standard Pins

($V_{CC} = 3\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	R4-R9	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	R4-R9	- 0.3	-	$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	R4-R8	$V_{CC} - 1.0$	-	-	V	$-I_{OH} = 1.0\text{mA}$ $V_{CC} = 3.5\text{V to }5.5\text{V}$	
			$V_{CC} - 0.5$	-	-	V	$-I_{OH} = 0.5\text{mA}$ $V_{CC} = 3.5\text{V to }5.5\text{V}$	
						V	$-I_{OH} = 0.3\text{mA}$	
Output Low Voltage	V_{OL}	R4-R8	-	-	0.4	V	$I_{OL} = 1.6\text{mA}$ $V_{CC} = 3.5\text{V to }5.5\text{V}$	
Input/Output Leakage Current	$ I_{IL} $	R4-R8, R9 ₁ -R9 ₃	-	-	1	μA	$V_{in} = 0\text{V to }V_{CC}$	1
		R9 ₀	-	-	20	μA	$V_{in} = 0\text{V to }V_{CC}$	

Note: 1. Output buffer current are excluded.

Input/Output Characteristics for High Voltage Pins

($V_{CC} = 3\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	D ₀ -D ₁₅ , RA, R0-R3	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	D ₀ -D ₁₅ , RA, R0-R3	$V_{CC} - 40$	-	$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D ₀ -D ₁₅ , R0-R3	$V_{CC} - 3.0$	-	-	V	$-I_{OH} = 15\text{mA}$ $V_{CC} = 4\text{V to }5.5\text{V}$	
			$V_{CC} - 2.0$	-	-	V	$-I_{OH} = 10\text{mA}$ $V_{CC} = 4\text{V to }5.5\text{V}$	
			$V_{CC} - 1.0$	-	-	V	$-I_{OH} = 4\text{mA}$	
Output Low Voltage	V_{OL}	D ₀ -D ₁₅ , R0-R3	-	-	$V_{CC} - 37$	V	$150\text{k}\Omega\text{ to }V_{CC} - 40\text{V}$	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₁₅ , RA, R0-R3	-	-	20	μA	$V_{in} = V_{CC} - 40\text{V to }V_{CC}$	1

Note: 1. Output buffer current are excluded.



HD404708/HD404709/HD4074709

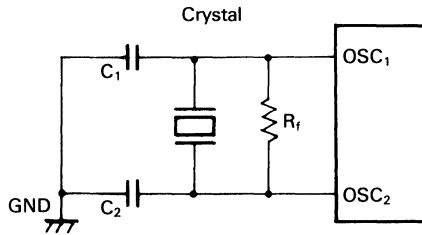
AC Characteristics

($V_{CC} = 3\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Oscillation Frequency Divide-by-4	f_{OSC}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	7
			1.6	4	4.5	MHz		
			0.4	2	2.25	MHz		
			1.6	2	2.25	MHz		
Oscillation Frequency (Divide-by-8)	f_{CL}	CL ₁ , CL ₂	–	32.768	–	kHz		
Instruction Cycle Time	t_{cyc}		0.89	1	10	μs	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	7
			0.89	1	2.5	μs		
			1.78	2	10	μs		
			1.78	2	2.5	μs		
Instruction Cycle Time	t_{SUBcyc}		–	244.14	–	μs		
Oscillation Stabilization (Crystal)	t_{RC}	OSC ₁ , OSC ₂	–	–	40	ms	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	1
			–	–	60	ms		1
Oscillation Stabilization (Ceramic Filter)	t_{RC}	OSC ₁ , OSC ₂	–	–	20	ms	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	1
			–	–	60	ms		1
Oscillation Stabilization	t_{RC}	CL ₁ , CL ₂	–	–	2	s		2
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	92	–	–	ns	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	3
			203	–	–	ns		3
External Clock Rising, Falling Time	t_{CPr} , t_{CPf}	OSC ₁	–	–	20	ns	$V_{CC} = 3.5\text{ to }5.5\text{ V}$	3
			–	–	20	ns		3
INT ₀ High, Low Level Width	t_{i0H} , t_{i0L}	$\overline{\text{INT}}_0$	2	–	–	$t_{cyc}/$ t_{SUBcyc}		4,6
INT ₁ High, Low Level Width	t_{i1H} , t_{i1L}	$\overline{\text{INT}}_1\text{--}\overline{\text{INT}}_3$	2	–	–	t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2	–	–	t_{cyc}		5
Input Capacitance	C_{in}	Except R9 ₀	–	–	30	pF	$f = 1\text{ MHz}, V_{in} = 0\text{ V}$	
		R9 ₀	–	–	180	pF		
RESET Falling Time	t_{RSTf}	RESET	–	–	20	ms		5

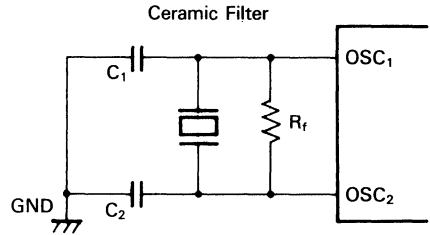
Notes: 1. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V (3.5V, in case of $V_{CC} = 3.5\text{ V--}5.5\text{ V}$) after Power on, or after RESET goes high. RESET must be kept high for at least t_{RC} to obtain oscillation time. Oscillation stabilization time depends on the crystal or ceramic filter's circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal or ceramic filter marker to determine the circuit parameter.





Crystal

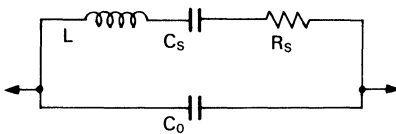
Xtal: Under the equivalent circuit
 $R_f: 1M\Omega \pm 20\%$
 $C_1: 10pF \pm 20\%$
 $C_2: 10pF \pm 20\%$



Ceramic Filter

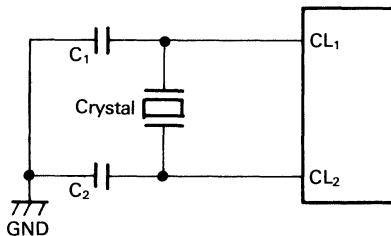
Ceramic Filter: CSA4.00MG (MURATA)

$R_f: 1M\Omega \pm 20\%$
 $C_1: 30pF \pm 20\%$
 $C_2: 30pF \pm 20\%$



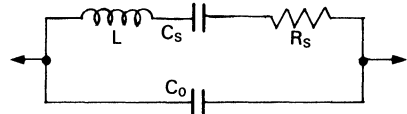
$C_0 = 7pF \text{ max}$
 $R_s = 100\Omega \text{ max}$
 $f = 1.0 - 4.5MHz$

- Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 3.0V after power on.
 Oscillation stabilization time depends on the crystal circuit constant and stray capacitance. In employing the resonator, please consult with the engineers of the crystal maker to determine the circuit parameter.



Xtal: MX38T (Nihon denpa kogyo)
 Right the equivalent circuit

$C_1: 15pF \pm 5\%$
 $C_2: 15pF \pm 5\%$



$C_0 = 1.5pF \text{ typ}$
 $R_s = 14k\Omega \text{ typ}$
 $f = 32.768kHz$

- See figure 53.
- See figure 54. Unit t_{cyc} is applied when MCU is Standby or Active mode.
- See figure 55.
- See figure 54. Unit t_{SUBcyc} is applied when MCU is in Watch or Sub-Active mode.
 $t_{SUBcyc} = 244.14\mu s$ (When using 32.768kHz crystal oscillator)
- Apply the data in parenthesis when subsystem oscillator is not used.

HD404708/HD404709/HD4074709

Serial Interface Timing Characteristics

($V_{CC} = 3\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V to }V_{CC}$, $T_a = -20\text{ to }+75^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t_{cyc}	\overline{SCK}	1	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t_{SCKH} , t_{SCKL}	\overline{SCK}	0.4	–	–	t_{cyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t_{SCKr} , t_{SCKf}	\overline{SCK}	–	–	80	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t_{SCKHD}	\overline{SCK}	1	–	–	t_{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t_{SCKH} , t_{SCKL}	\overline{SCK}	0.4	–	–	t_{cyc}		1
Input Transfer Clock Rising, Falling Time	t_{SCKr} , t_{SCKf}	\overline{SCK}	–	–	80	ns		1
Serial Output Data Delay Time	t_{DSO}	SO	–	–	600	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t_{SSI}	SI	200	–	–	ns		1
Serial Input Data Hold Time	t_{HSI}	SI	400	–	–	ns		1

- Notes: 1. See figure 56.
 2. See figure 57.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.



(V_{CC} = 3.5 V to 5.5 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Output Transfer Clock Cycle Time	t _{Scyc}	$\overline{\text{SCK}}$	1	–	–	t _{cyc}	Loading (note 2)	1,2
Output Transfer Clock High, Low Level Width	t _{SCKH} , t _{SCKL}	$\overline{\text{SCK}}$	0.4	–	–	t _{scyc}	Loading (note 2)	1,2
Output Transfer Clock Rising, Falling Time	t _{SCKr} , t _{SCKf}	$\overline{\text{SCK}}$	–	–	40	ns	Loading (note 2)	1,2
Input Transfer Clock Completion Detect Time	t _{SCKHD}	$\overline{\text{SCK}}$	1	–	–	t _{cyc}		1,2,3
Input Transfer Clock High, Low Level Width	t _{SCKH} , t _{SCKL}	$\overline{\text{SCK}}$	0.4	–	–	t _{cyc}		1
Input Transfer Clock Rising, Falling Time	t _{SCKr} , t _{SCKf}	$\overline{\text{SCK}}$	–	–	40	ns		1
Serial Output Data Delay Time	t _{DSO}	SO	–	–	300	ns	Loading (note 2)	1,2
Serial Input Data Setup Time	t _{SSI}	SI	100	–	–	ns		1
Serial Input Data Hold Time	t _{HSI}	SI	200	–	–	ns		1

- Notes: 1. See figure 55.
 2. See figure 56.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

**HD404708/HD404709
Option List**

* Please enter check marks in , for example , x or .

(1) ROM size (2) Package type (3) Optional Function

<input type="checkbox"/> HD404708	<input type="checkbox"/> DP-64S	<input type="checkbox"/> 32kHz CPU operation
<input type="checkbox"/> HD404709	<input type="checkbox"/> FP-64B	<input type="checkbox"/> no 32kHz CPU operation

Order date	
Company name	
Department	
Name	
ROM code	
LSI type	HD40470

(4) ZTAT compatibility

<input type="checkbox"/> I/O circuit compatibility with the HD4074709
<input type="checkbox"/> No I/O circuit compatibility with the HD4074709

(5) ROM media

<input type="checkbox"/> EPROM: emulator type
<input type="checkbox"/> HD4074709

(Note) ZTAT compatibility is enabled only when all pins use C or D type circuit. In this case do not check the list item (6) and (7).

(6) I/O option (I/O options masked by are not available)

Pin name	I/O	I/O option					Pin name	I/O	I/O option				
		B	C	D	E	B			C	D	E		
D ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R3	R3 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R3	R3 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R3	R3 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R3	R3 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₄	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R4	R4 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₅	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R4	R4 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₆	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R4	R4 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₇	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R4	R4 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₈	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R5	R5 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₉	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R5	R5 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R5	R5 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R5	R5 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R6	R6 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R6	R6 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₄	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R6	R6 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
D ₁₅	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R6	R6 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R0	R0 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R7	R7 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R0 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R7 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R0 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R7 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R0 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R7 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R1	R1 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R8	R8 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R1 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R8 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R1 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R9	R9 ₀	I	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R1 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			R9 ₁	I	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R2	R2 ₀	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	R9	R9 ₂	I	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	R2 ₁	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		R9 ₃	I	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		
	R2 ₂	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		RA	RA ₀	I	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
	R2 ₃	I/O	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			RA ₁	I	Check (7)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

(7) RA₁/V_{disp}

<input type="checkbox"/> RA ₁ : without pull-down MOS (D)
<input type="checkbox"/> V _{disp}

Note: RA₁/V_{disp} has to be selected as V_{disp} pin except the case that all high voltage pins are option D.

Condition

(1) OSC₁ and OSC₂ oscillator

<input type="checkbox"/> Ceramic filter	f =	MHz
<input type="checkbox"/> Crystal	f =	MHz
<input type="checkbox"/> External clock	f =	MHz

(2) CL₁ and CL₂ oscillator

<input type="checkbox"/> Not used	—
<input type="checkbox"/> Crystal	f = 32.768 kHz

Check I/O option you select.

B: with pull-up MOS C: without pull-up MOS
D: without pull-down MOS E: with pull-down MOS



HD404808/HD4074808/ HD40L4808/HD407L4808

Description

The MCU is a 4-bit single chip HMCS400 series microcomputer providing high program productivity. It incorporates large size memory, LCD driver/controller, voltage comparator, and 32 kHz watch oscillator circuit.

The HD4074808/HD407L4808, incorporating PROM, is a ZTAT microcomputer which can dramatically shorten system development period and smoothly proceed from debug-ging to mass production.

- Four low power dissipation modes
 - Standby mode
 - Stop mode
 - Watch mode
 - Subactive mode (Functional Option)
- Internal oscillator:
 - Crystal or ceramic filter
 - External clock is available
- Voltage comparator (2 channels)
- Operation modes:
 - MCU mode
 - PROM mode (HD4074808/HD407L4808)
- Package
 - 80-pin flat plastic package (FP-80B)
(FP-80A)

Features

- 8192 words of 10-bit ROM
- 1184 digits of 4-bit RAM
- 30 I/O pins:
 - Including 10 high-current output pins.
 - CMOS I/O pin circuit configuration
 - Input/output pull-up MOS can be selected by software
- 16-digit LCD driver
- Three timers/counters
- Clock synchronous 8-bit serial interface
- Six interrupt sources
 - External: 2
 - Internal: 4
- Subroutine stack
 - Up to 16 levels including interrupts
- Instruction cycle time:
 - 1 μ s ($f_{osc} = 4$ MHz for HD404808/
HD4074808)
 - 5 μ s ($f_{osc} = 800$ kHz for HD40L4808/
HD407L4808)

Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

Type of Products

Mask ROM type

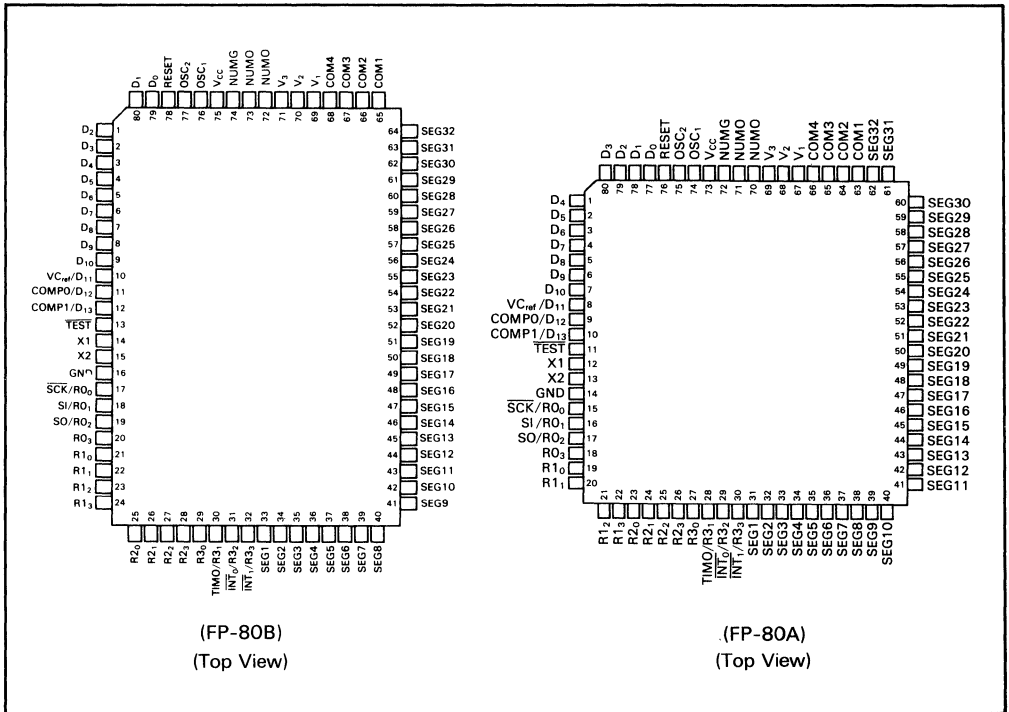
Part No.	Clock Freq. (MHz)	Package
HD404808FS	4	FP-80B
HD404808H		FP-80A
HD40L4808FS	0.8	FP-80B
HD40L4808H		FP-80A

ZTAT type

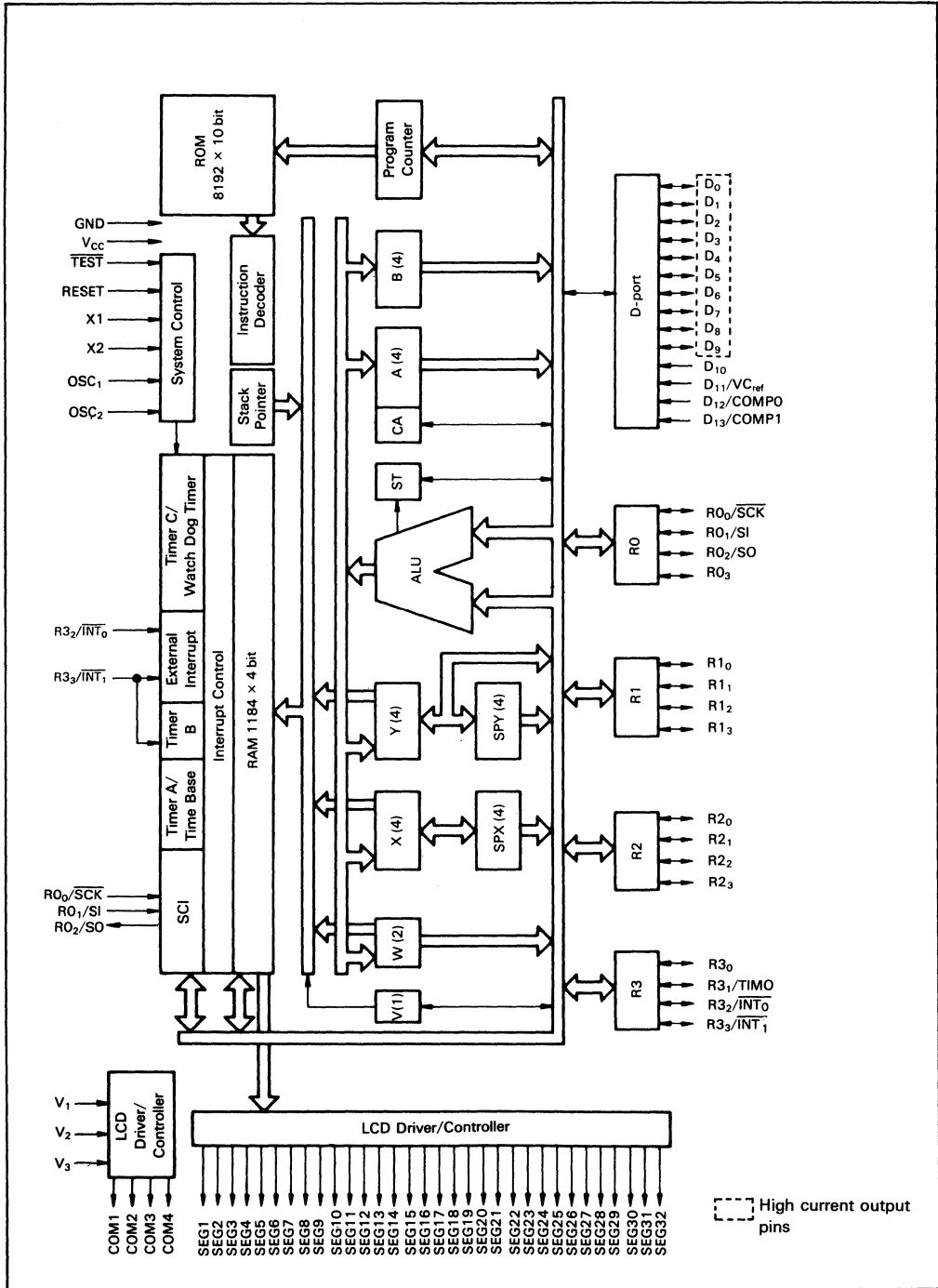
Part No.	Clock Freq. (MHz)	Package
HD4074808FS	4	FP-80B
HD4074808H		FP-80A
HD407L4808FS	0.8	FP-80B
HD407L4808H		FP-80A



Pin Arrangement



Block Diagram



Pin Function

Pin No. FP-80B	FP-80A	Pin Name	I/O	Pin No. FP-80B	FP-80A	Pin Name	I/O
1	79	D ₂	I/O	41	39	SEG9	O
2	80	D ₃	I/O	42	40	SEG10	O
3	1	D ₄	I/O	43	41	SEG11	O
4	2	D ₅	I/O	44	42	SEG12	O
5	3	D ₆	I/O	45	43	SEG13	O
6	4	D ₇	I/O	46	44	SEG14	O
7	5	D ₈	I/O	47	45	SEG15	O
8	6	D ₉	I/O	48	46	SEG16	O
9	7	D ₁₀	I	49	47	SEG17	O
10	8	D ₁₁ /V _{Cref}	I	50	48	SEG18	O
11	9	D ₁₂ /COMPO	I	51	49	SEG19	O
12	10	D ₁₃ /COMP1	I	52	50	SEG20	O
13	11	TEST	I	53	51	SEG21	O
14	12	X1	I	54	52	SEG22	O
15	13	X2	O	55	53	SEG23	O
16	14	GND		56	54	SEG24	O
17	15	RO ₀ /SCK	I/O	57	55	SEG25	O
18	16	RO ₁ /SI	I/O	58	56	SEG26	O
19	17	RO ₂ /SO	I/O	59	57	SEG27	O
20	18	RO ₃	I/O	60	58	SEG28	O
21	19	R1 ₀	I/O	61	59	SEG29	O
22	20	R1 ₁	I/O	62	60	SEG30	O
23	21	R1 ₂	I/O	63	61	SEG31	O
24	22	R1 ₃	I/O	64	62	SEG32	O
25	23	R2 ₀	I/O	65	63	COM1	O
26	24	R2 ₁	I/O	66	64	COM2	O
27	25	R2 ₂	I/O	67	65	COM3	O
28	26	R2 ₃	I/O	68	66	COM4	O
29	27	R3 ₀	I/O	69	67	V ₁	
30	28	R3 ₁ /TIMO	I/O	70	68	V ₂	
31	29	R3 ₂ /INT ₀	I/O	71	69	V ₃	
32	30	R3 ₃ /INT ₁	I/O	72	70	NUMO	
33	31	SEG1	O	73	71	NUMO	
34	32	SEG2	O	74	72	NUMG	
35	33	SEG3	O	75	73	V _{CC}	
36	34	SEG4	O	76	74	OSC ₁	I
37	35	SEG5	O	77	75	OSC ₂	O
38	36	SEG6	O	78	76	RESET	I
39	37	SEG7	O	79	77	D ₀	I/O
40	38	SEG8	O	80	78	D ₁	I/O

Note: I/O: Input pin Output pin, I: Input pin, O: Output pin, NUMO: Open, NUMG: GND



Pin Description

GND, V_{CC} (Power)

GND and V_{CC} are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to V_{CC}.

TEST

TEST is for test purposes only. Connect it to V_{CC}.

RESET

RESET resets the MCU. Refer to Reset section for details.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. Refer to Internal Oscillator for details.

X1, X2

X1 and X2 are the watch oscillator 32 kHz crystal terminals.

Port D (D₀-D₁₃)

Port D consists of 14 1-bit I/O ports. D₀-D₉ are I/O ports and D₁₀-D₁₃ are input ports. D₀-D₉ are high current output ports (15 mA max). D₁₁-D₁₃ are also available as voltage comparators. Refer to Input/Output for details.

Port R (R₀-R₃)

Ports R₀-R₃ are 4-bit I/O ports. R₀, R₀₁, R₀₂, R₃₁, R₃₂, and R₃₃ are multiplexed with SCK, SI, SO, TIMO, INT₀, INT₁, respectively.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

SCK, SI, SO

The transfer clock I/O pin (SCK), serial data input pin (SI), and serial data output pin (SO) are used for serial interface. SCK, SI, and SO are multiplexed with R₀₀, R₀₁, and R₀₂, respectively. For details, see Serial Interface section.

TIMO

TIMO is a variable duty-cycle pulse waveform output pin. See Timer C section for details.

V₁, V₂, V₃

V₁-V₃ are power supply pins for the LCD driver. As LCD driving resistors are provided internally, no line should be connected to these pins. The voltage on each pin is V_{CC} ≥ V₁ ≥ V₂ ≥ V₃ ≥ GND. See Liquid Crystal Display section for details.

COM1 to COM4

These are common signal output pins for LCD display. See Liquid Crystal Display section for details.

SEG1 to SEG32

These are segment signals output pins for LCD display. See Liquid Crystal Display section for details.

NUMG

NUMG is not a user pin. Connect to GND.

NUMO

NUMO is not a user pin. Do not connect to any lines.

COMP0, COMP1, VC_{ref}

COMP0, COMP1 are analog inputs for the voltage comparator. VC_{ref} is used as a reference voltage pin to input the threshold voltage of the analog input pin.

Functional Description

ROM Memory Map

The MCU includes 8,192 words \times 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. Program sequence branches to subroutine by CAL instruction.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow the MCU to refer to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

RAM Memory Map

The MCU includes 1184 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$01F, \$024 to \$03F): The special function registers are the mode or data registers for

the serial interface, timer/counter, LCD, and the data control registers for the I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

SEM/REM, SEMD/REMD instructions are available to the LCD control register (LCR).

Other registers cannot be accessed by RAM bit manipulation instructions.

Register Flag Area (\$020-\$023): Locations \$020 through \$023 consist of the LSON and WDON flags which are bit registers accessible by RAM bit manipulation instruction. Note that WDON flag can only be set and SEM/SEMD instruction is available for this.

LCD Data Area (\$050-\$06F): Locations \$050 to \$06F store the LCD data which is automatically transmitted to segment as a display data. LCD is illuminated with 1 and faded with 0. This area can be used as a data area.

Data Area (\$040 to \$2CF, \$100 to \$2CF; Bank 1): 16 digits of \$040 through \$04F are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4). 464 digits of \$100 through \$2CF is select the bank of location depending on the value of V register.

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST), and carry (CA) when subroutine call (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by RTNI instruction. This area, when not used for a stack, is available as a data area.

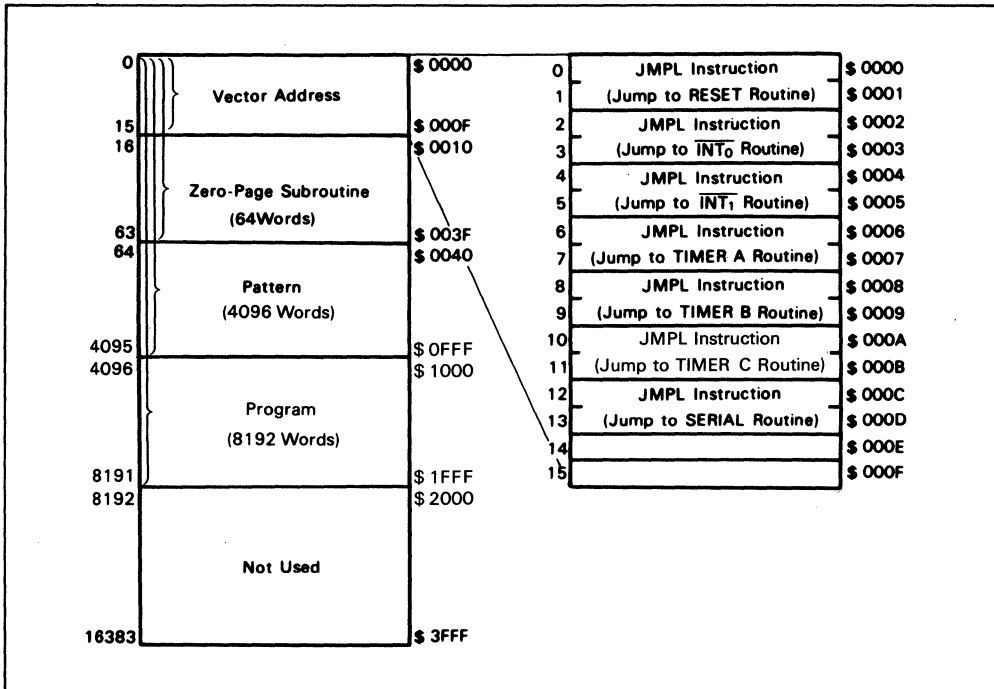


Figure 1. ROM Memory Map

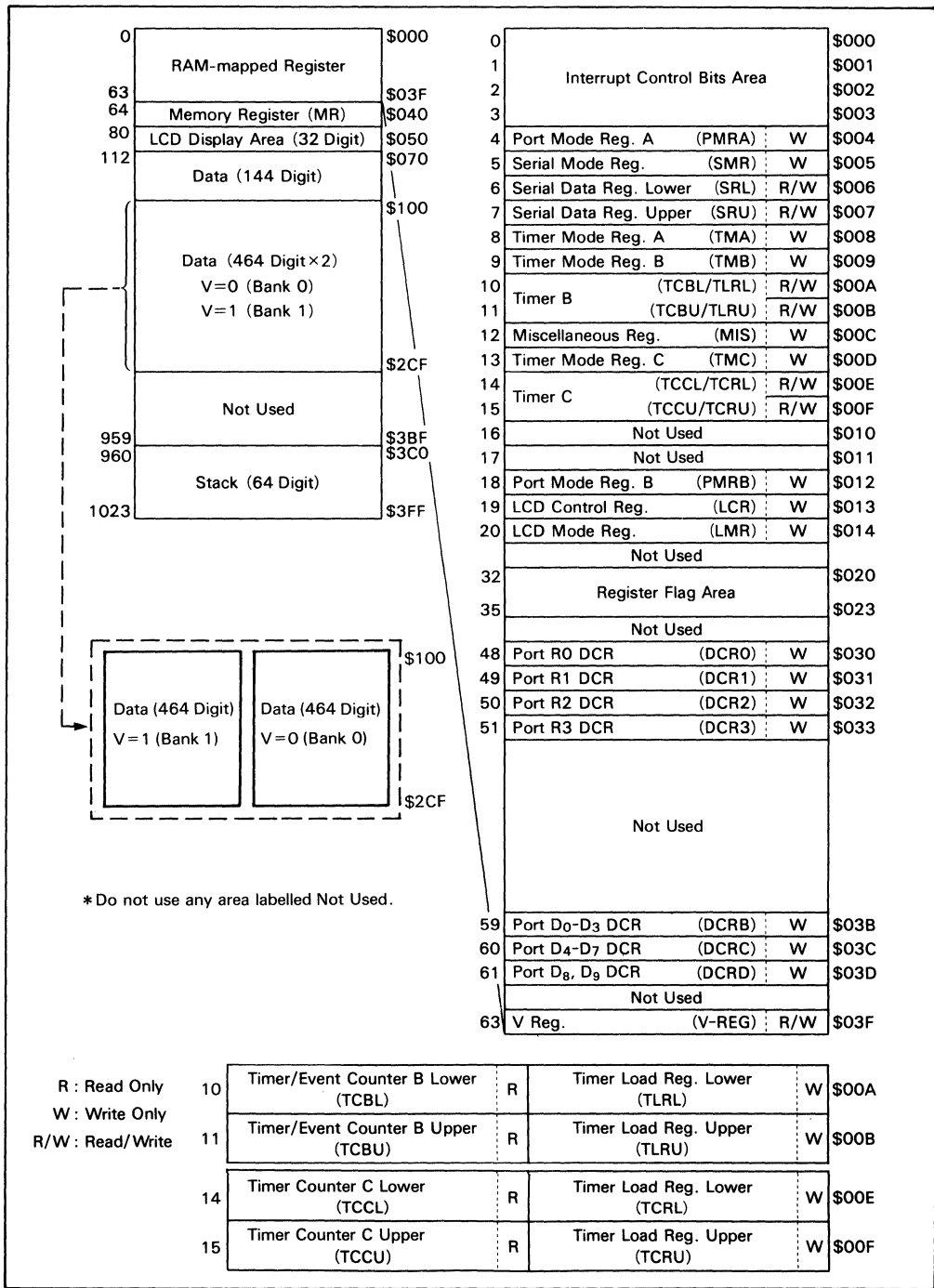


Figure 2. RAM Memory Map

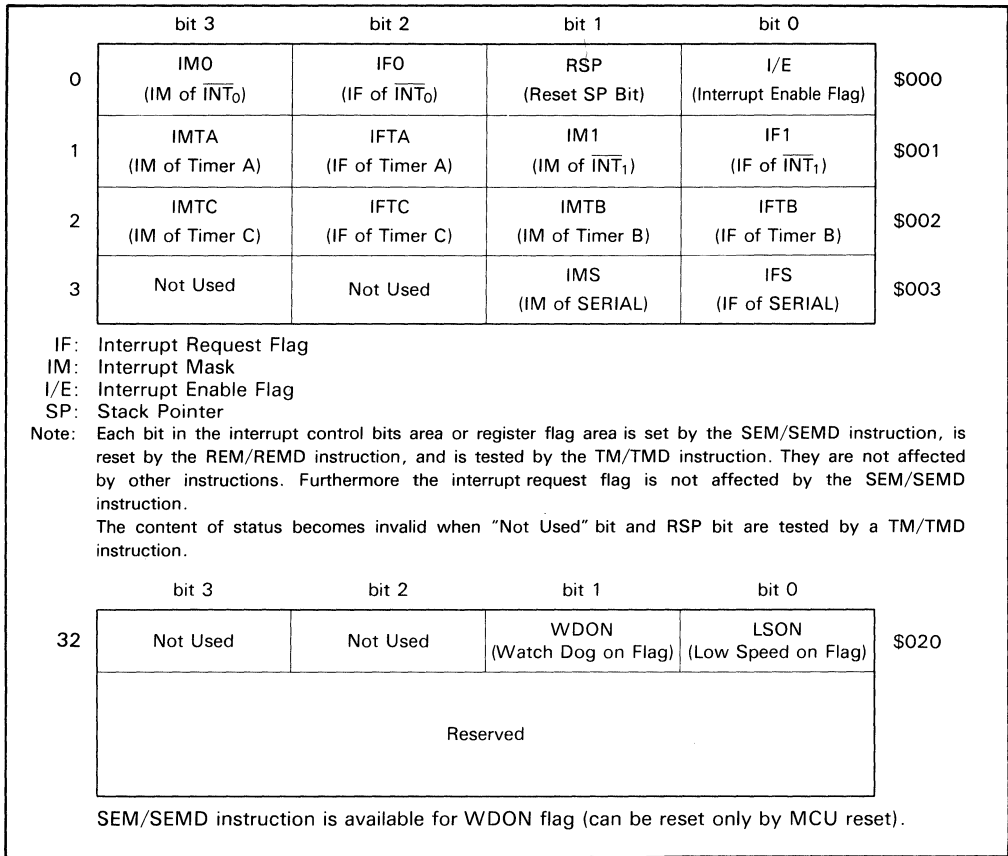


Figure 3. Configuration of Interrupt Control Bit Area and Register Flag Area

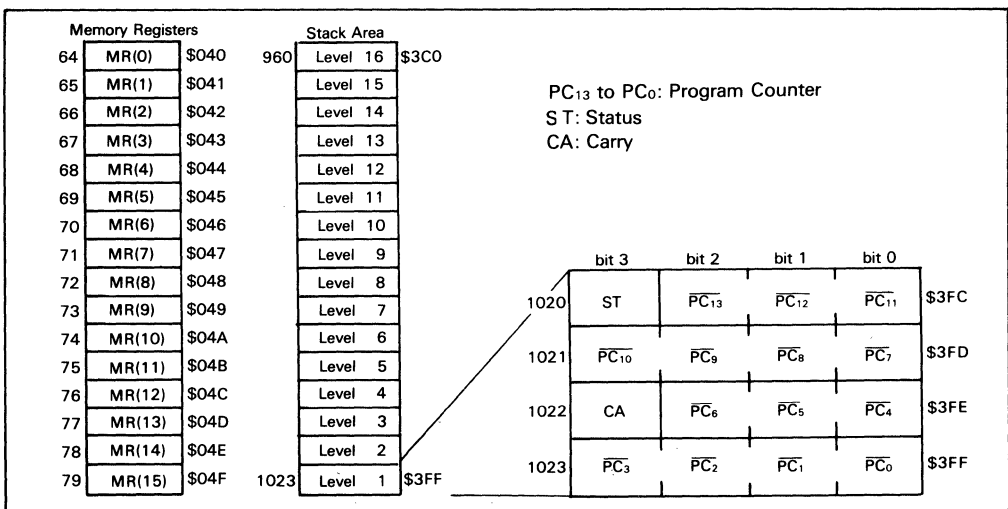


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU provides ten registers and two flags for the CPU operations. They are illustrated in figure 5 and described in the following paragraphs.

Accumulator (A), Register B (B): The accumulator and register B are 4-bit registers which hold the results of the arithmetic logic unit (ALU), and exchange data between memories, I/O pins, and other registers.

Register V (V): Register V, available for RAM address expansion, selects the bank of location \$100-\$2CF on the RAM address (464 digits) depending on its value. Therefore, when you access location \$100-\$2CF on the RAM address, specify the value of register V ($V = \$0$; Bank 0, $V = \$1$; Bank 1). You can access location \$000-\$0FF and \$300-\$3FF independently of register V's value. Register V is located in \$03F of the RAM address area.

Register W (W), Register X (X), Register Y (Y): Register W is a 2-bit, and registers X and Y are 4-bit registers which address RAM indirectly. Register Y is also available for addressing port D.

Register SPX (SPX), Register SPY (SPY): Registers SPX and SPY are 4-bit registers available for assisting registers X and Y, respectively.

Carry (CA): The carry holds the ALU overflow generated by an arithmetic operation. It is also affected by SEC, REC, ROTL, and ROTR instructions. During interrupt servicing, the carry is pushed onto the stack and restored back from the stack by RTNI instruction. (It is unaffected by RTN instructions.)

Status (ST): The status holds the ALU overflow, ALU non-zero, and the results of bit test instructions for the arithmetic or compare instructions. The status is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until an instruction which affects the next status is executed. The status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, the status is pushed onto the stack and restored back from the stack by RTNI instruction, not by RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter for holding the ROM address.

Stack Pointer (SP): The stack pointer is a 10-bit register to indicate the next stacking area up to 16 levels. The stack pointer is initialized to \$3FF on the RAM address at the MCU reset. It is decremented by 4 as data is pushed onto the stack, and incremented by 4 as data is restored back from the stack. The stack pointer is initialized to \$3FF either by MCU reset or the RSP bit reset by REM/REMD instruction.

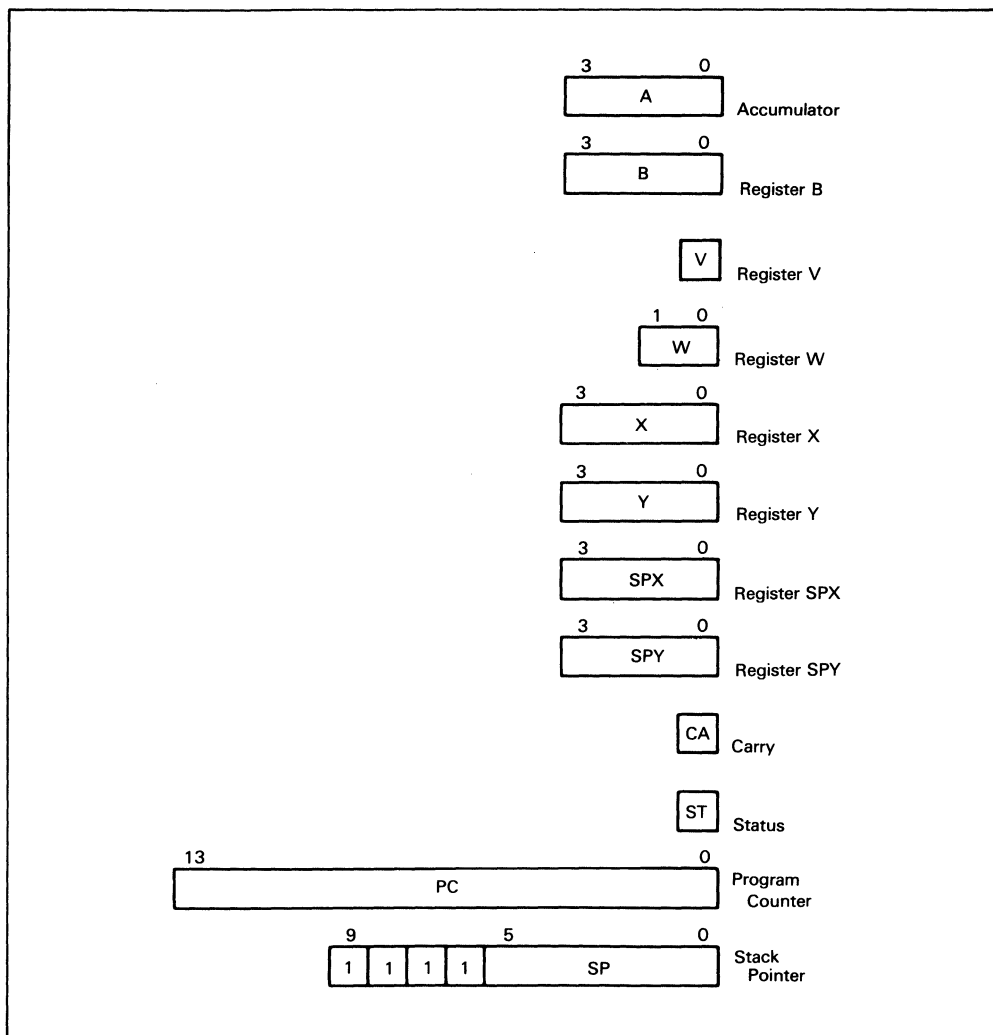


Figure 5. Registers and Flags

Interrupt

Six interrupt sources are available on the MCU: external requests (INT₀, INT₁), timer/counter (timers A, B, C), and serial interface (serial). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt

request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

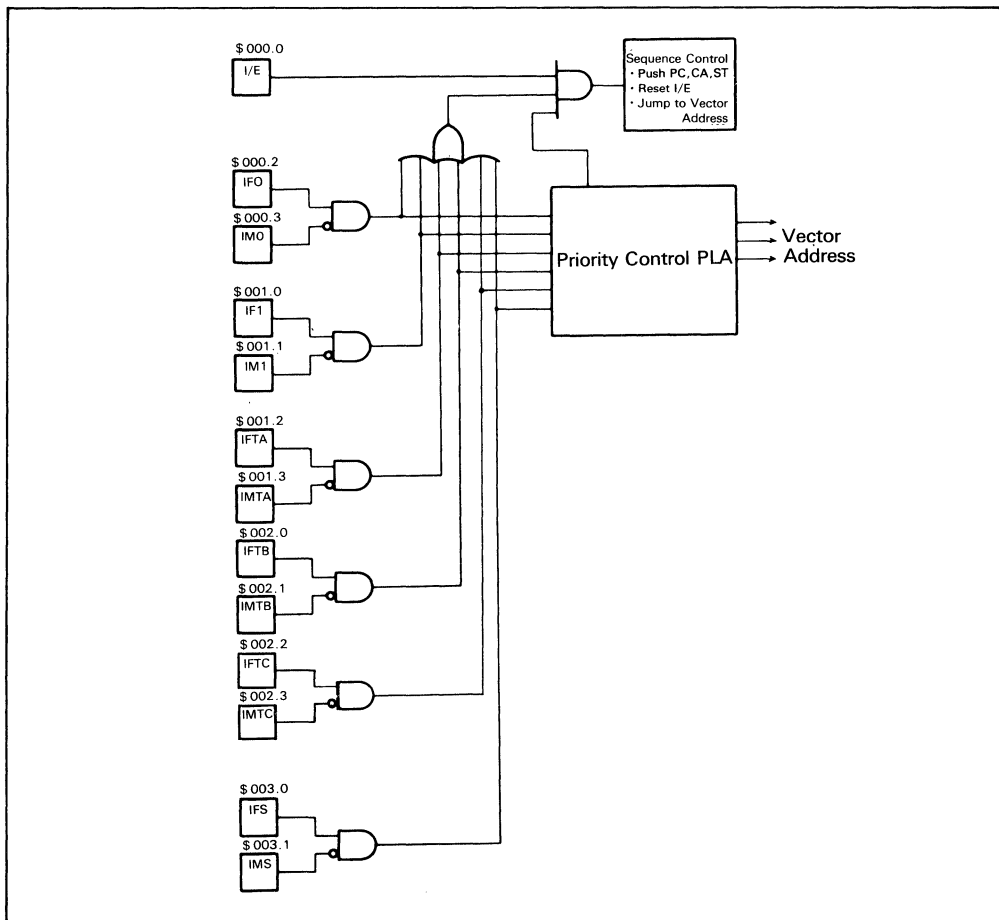


Figure 6. Interrupt Control Circuit Block Diagram



Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is executed after jumping to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF, which caused the interrupt service, must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests (table 3). It is reset by

interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register (PMRA: \$004).

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs (table 4).

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When using \overline{INT}_1 as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted (table 5).

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	—	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
Timer C	5	\$000A
SERIAL	6	\$000C

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	Interrupt Source					
	\overline{INT}_0	\overline{INT}_1	Timer A	Timer B	Timer C	SERIAL
I/E	1	1	1	1	1	1
IF0 · \overline{IMO}	1	0	0	0	0	0
IF1 · $\overline{IM1}$	*	1	0	0	0	0
IFTA · \overline{IMTA}	*	*	1	0	0	0
IFTB · \overline{IMTB}	*	*	*	1	0	0
IFTC · \overline{IMTC}	*	*	*	*	1	0
IFS · \overline{IMS}	*	*	*	*	*	1

* Don't care



To detect the edge of \overline{INT}_0 or \overline{INT}_1 , it must need more than two instruction cycle times level ($2t_{cyc}/2t_{SUBcyc}$).

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs, respectively (table 4).

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests (table 5).

Timer A Interrupt Request Flag (IFTA: \$001 bit 2): The timer A interrupt request flag is set by the overflow output of timer A (table 6).

Timer A Interrupt Mask (IMTA: \$001 bit 3): Timer A interrupt mask prevents an interrupt request from being generated by timer A interrupt request flag (table 7).

Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B

(table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B interrupt request flag (table 9).

Timer C Interrupt Request Flag (IFTC: \$002 bit 2): The timer C interrupt request flag is set by the overflow output of timer C (table 10).

Timer C Interrupt Mask (IMTC: \$002 bit 3): The timer C interrupt mask prevents the interrupt from being generated by timer C interrupt request flag (table 11).

Serial Interrupt Request Flag (IFS: \$003 bit 0): The serial interrupt request flag will be set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter (table 12).

Serial Interrupt Mask (IMS: \$003 bit 1): The serial interrupt mask masks the interrupt request (table 13).

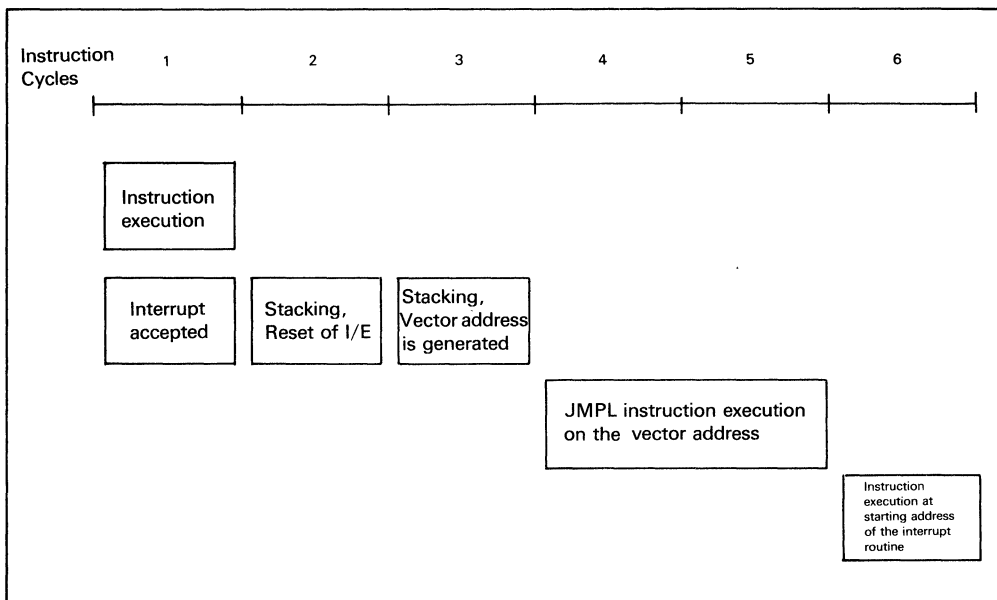


Figure 7. Interrupt Servicing Sequence

Table 3. Interrupt Enable Flag

Interrupt Enable Flag (I/E)	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

External Interrupt Request Flags (IFO, IF1)	Interrupt Request
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks (IM0, IM1)	Interrupt Request
0	Enable
1	Disable (masks)

Table 6. Timer A Interrupt Request Flag

Timer A Interrupt Request Flag (IFTA)	Interrupt Request
0	No
1	Yes

Table 7. Timer A Interrupt Mask

Timer A Interrupt Mask (IMTA)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag (IFTB)	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask (IMTB)	Interrupt Request
0	Enable
1	Disable (Mask)

Table 10. Timer C Interrupt Request Flag

Timer C Interrupt Request Flag (IFTC)	Interrupt Request
0	No
1	Yes

Table 11. Timer C Interrupt Mask

Timer C Interrupt Mask (IMTC)	Interrupt Request
0	Enable
1	Disable (mask)

Table 12. Serial Interrupt Request Flag

Serial Interrupt Request Flag (IFS)	Interrupt Request
0	No
1	Yes

Table 13. Serial Interrupt Mask

Serial Interrupt Mask (IMS)	Interrupt Request
0	Enable
1	Disable (Mask)

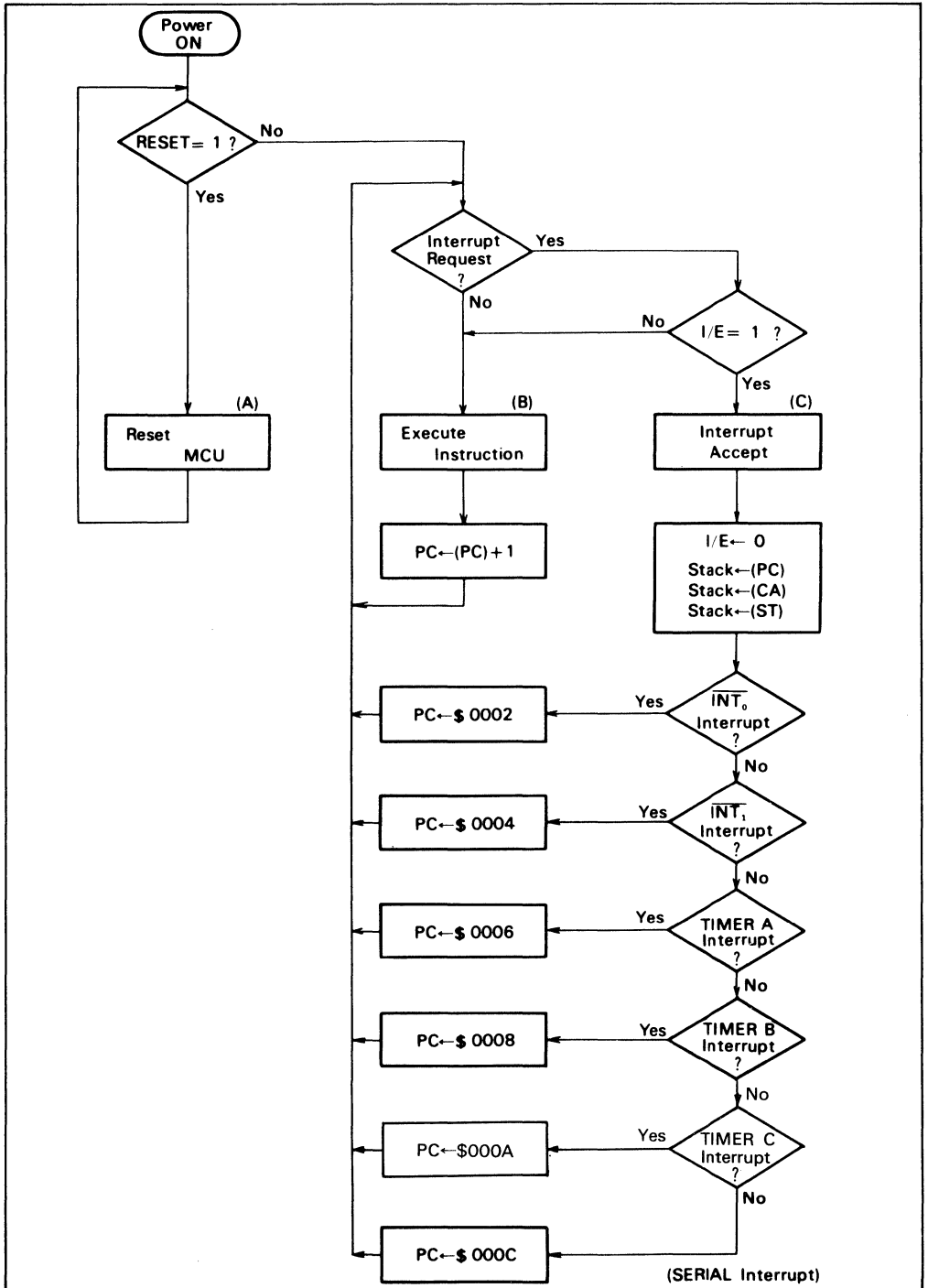


Figure 8. Interrupt Servicing Flowchart



Serial Interface

The serial interface transmits/receives 8-bit data in serial. It consists of the serial data register, the serial mode register, the port mode register A, the octal counter, and the multiplexer (figure 9). Pin RO_0/SCK and the transfer clock signal are controlled by the serial mode register. The data of the serial data register can be written in or read out by software. The data in the serial data register can be shifted synchronously with the transfer clock signal.

The STS instruction starts serial interface operations and resets the octal counter to \$0. The octal counter starts to count at the falling edge of the transfer clock (SCK) signal and increments by one at the rising edge of the SCK. When the octal counter is reset to \$0 after eight transfer clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

Serial Mode Register (SMR: \$005): The 4-bit write-only serial mode register controls the RO_0/SCK , prescaler divide ratio, and transfer clock source (table 14).

The write signal to the serial mode register controls the internal state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying the transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

Data of the serial mode register will be changed at the second instruction after write instruction to the serial mode register. Therefore, it is required to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Serial Data Register (SRL: \$006, SRU: \$007): The 8-bit read/write serial data register consists of low-order digits (SRL: \$006) and high-order digits (SRU: \$007).

The data in the serial data register will be

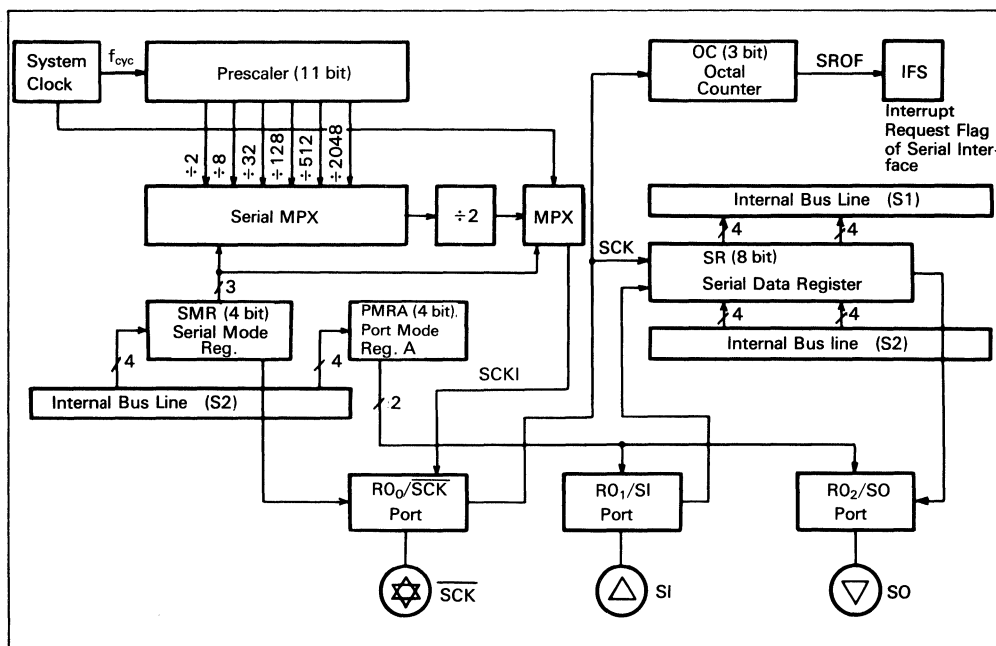


Figure 9. Serial Interface Block Diagram



output from the SO pin LSB first synchronously with the falling edge of the transfer clock signal. At the same time, external data will be input from the SI pin to the serial data register synchronously with the rising edge of the transfer clock. Figure 11 shows the I/O timing chart for the transfer clock signal and the data.

The read/write operations of the serial data register should be performed after the completion of data transmit/receive. Otherwise the data may not be guaranteed.

Selection and Change of the Operation Mode: Table 15 shows the serial interface operation modes which are determined by a combination of the value in the port mode register and that in the serial mode register.

Initialize the serial interface by the write signal to the serial mode register in order to change the operation mode of the serial interface.

Operating State of Serial Interface: The serial interface has three operating states: the STS waiting state, SCK waiting state, and transfer state (figure 12).

The STS waiting state is the initialization state of the serial interface internal state. The serial interface enters this state in one of two ways: either by changing the operation mode through a change in the data in the port mode register, or by writing data into the serial mode register. In this state, the serial interface does not operate even if the transfer clock is applied. If an STS instruction is executed then, the serial interface shifts to

Table 14. Serial Mode Register

SMR3	R0 ₀ /SCK
0	Used as R0 ₀ port input/output pin
1	Used as SCK input/output pin

Transfer Clock							
SMR2	SMR1	SMR0	R0 ₀ /SCK Port	Clock Source	Prescaler Divide Ratio	System Clock Divide Ratio	
0	0	0	SCK Output	Prescaler	÷ 2048	÷	4096
0	0	1	SCK Output	Prescaler	÷ 512	÷	1024
0	1	0	SCK Output	Prescaler	÷ 128	÷	256
0	1	1	SCK Output	Prescaler	÷ 32	÷	64
1	0	0	SCK Output	Prescaler	÷ 8	÷	16
1	0	1	SCK Output	Prescaler	÷ 2	÷	4
1	1	0	SCK Output	System Clock		÷	1
1	1	1	SCK Input	External Clock			

SCK waiting state.

In this state, the falling edge of the first transfer clock causes the serial interface shift to transfer state, while the octal counter counts-up and the serial data register shifts simultaneously. As an exception, if the clock continuous output mode is selected, the serial interface stays in SCK waiting state while the transfer clock outputs continuously. The octal counter becomes 000 again by 8 external transfer clocks or by execution of STS

instruction, so that the serial interface returns to SCK waiting state, and the serial interrupt request flag is set simultaneously. In transfer state the octal counter becomes 000 by 8 internal transfer clock, so that the serial interface enters STS instruction waiting state, and the serial interrupt request flag is set simultaneously.

When the internal transfer clock is selected, the transfer clock output is triggered by the execution of an STS instruction, and stops

Table 15. Serial Interface Operation Mode

SMR3	PMRA1	PMRA0	Serial Interface Operating Mode
1	0	0	Clock Continuous Output Mode
1	0	1	Transmit Mode
1	1	0	Receive Mode
1	1	1	Transmit/Receive Mode

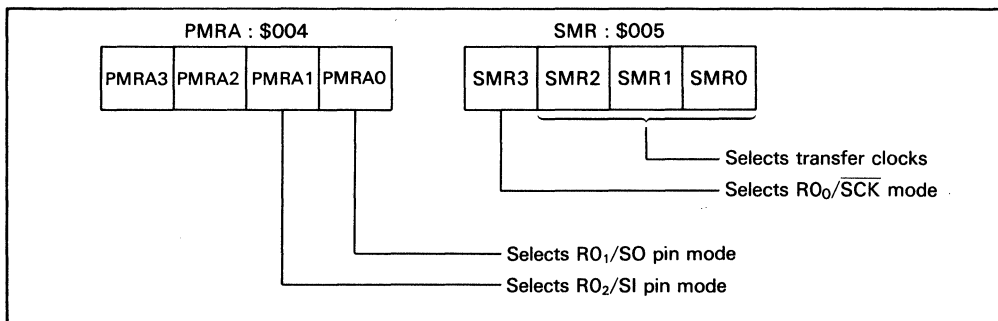


Figure 10. Configurations and the Functions of the Mode Registers

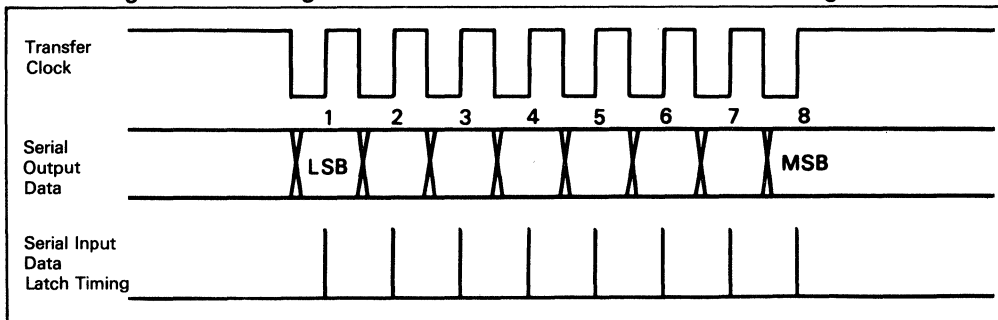


Figure 11. Serial Interface I/O Timing Chart

after 8 clocks.

Program the SMR again to initialize the internal state of the serial interface when the PMRA is programmed in the transfer state or in the SCK waiting state. Then the serial interface goes into the STS waiting state.

Example of Transfer Clock Error Detection: The serial interface malfunctions when the transfer clock is disturbed by external

noises. In this case, transfer clock error can be detected by the procedure shown in figure 13.

If more than 8 transfer clocks are applied in the SCK waiting state, the state of the serial interface shifts in the following sequence: first, transfer state, second, SCK waiting state, and third, transfer state again. The serial interrupt request flag should be reset before entering into the STS waiting state by

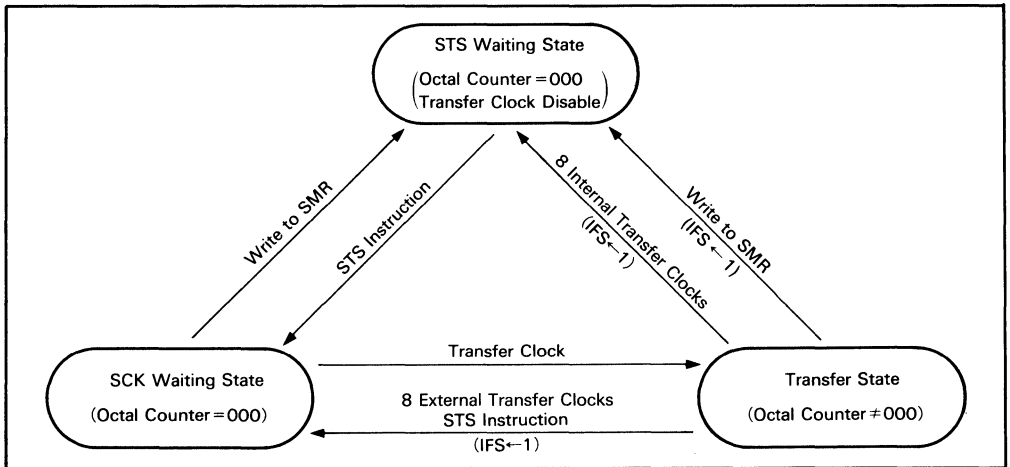


Figure 12. Serial Interface Operation State

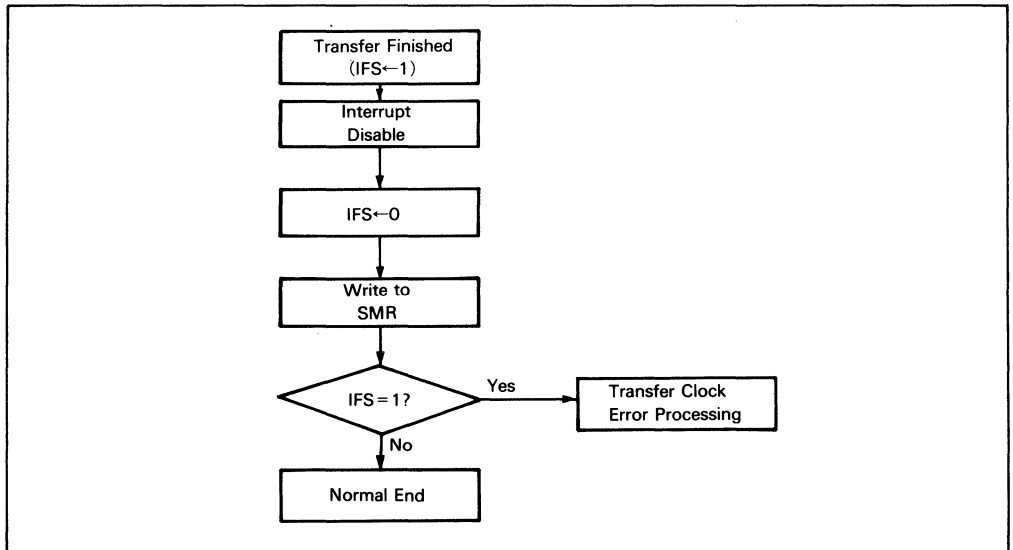


Figure 13. Example of Transfer Clock Error Detection

writing data to SMR. This procedure causes the serial interface request flag to be set again.

Timer

The MCU provides prescalers S and B (Each prescaler has the different input clock source individually), and 3 timers/counters (timers A, B, and C). Figures 14, 15 show their diagrams.

Prescaler S: The input to the prescaler S is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except by MCU reset and in the stop and watch mode. The prescaler provides input clock signals of timers A-C and the transfer clock of the serial interface. They can be selected by the timer mode registers A (TMA), B (TMB), C (TMC), and the serial mode register (SMR), respectively.

Prescaler W: The input to the prescaler W is a clock which divides X1 input clock into 8. The output of the prescaler W is available as an input clock for timer A by controlling the timer mode register (TMA).

Timer A Operation: After timer A is initialized to \$00 by MCU reset, it counts up at every clock input signal. When the next clock signal is applied after timer A is counted up

to \$FF, timer A is set to \$00 again, and generating overflow output. This leads to setting timer A interrupt request flag (IFTA: \$001, bit 2) to 1. Therefore, timer A can function as an interval timer periodically generating overflow output at every 256th clock signal input.

To use timer A as a watch time base, set TMA3 to 1. The timer counter receives prescaler W output, and timer A generates interrupts with an accurate timing (reference clock = 32 kHz crystal oscillator). When you use timer A as a watch time base, prescaler W and timer counter can be initialized to \$0 by setting timer mode register A.

The clock input signals to timer A are selected by the timer mode register A (TMA: \$008).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ by the port mode register (PMR: \$004) control to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied

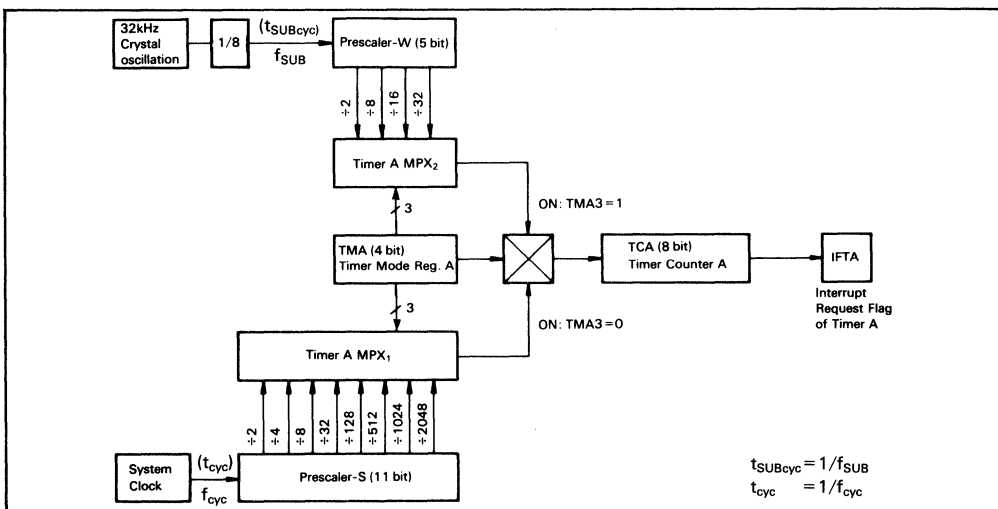


Figure 14. Timer A Block Diagram



to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load

register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002, bit 0) will be set at this overflow output.

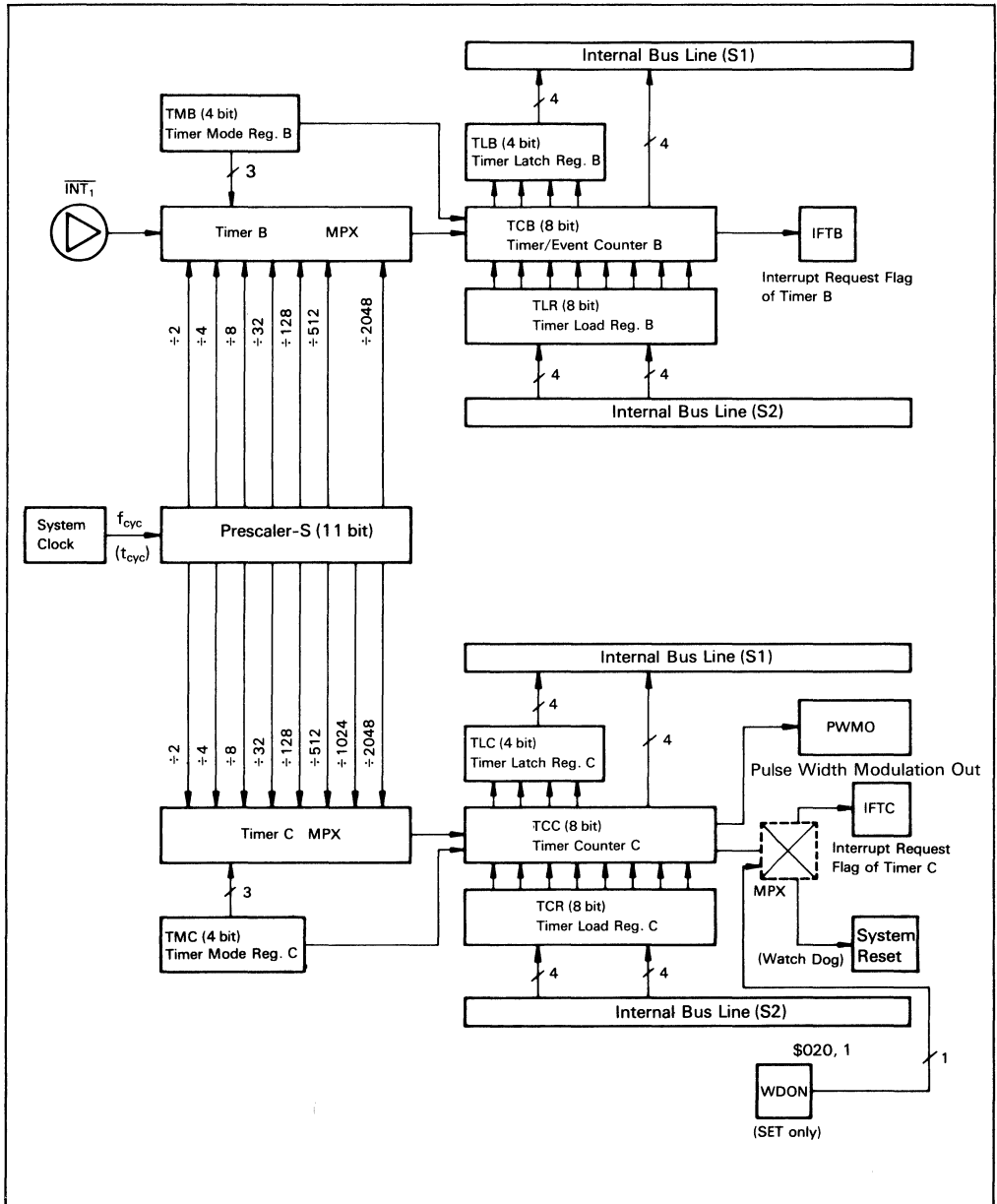


Figure 15. Timer B/Timer C Block Diagram

Timer C Operation: The timer mode register C (TMC: \$00D) selects the auto-reload function, and the prescaler divide ratio for timer C.

Timer C is initialized according to the data written into the timer load register by software. Timer C counts up at every clock input signal. When the next clock signal is applied to timer C after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer C is initialized according to the value of the timer load register. If it is not selected, timer C goes to \$00. The timer C interrupt request flag (IFTC: \$002, bit 2) will be set at this overflow output.

Timer C is also available as a watch dog timer for detecting a program out of sequence. An MCU reset occurs when the watch dog on flag (WDON) is 1 and the counter overflow output is generated by the program going out of sequence. During timer C is stopped, the watchdog timer function is also stopped. In the standby mode, the function is enabled.

Timer C provides a variable duty-cycle pulse output function (PWMO). The output waveform differs depending on the contents of the timer mode register and the timer load register C (figure 16). When you select pulse output function, set R31/TIMO to TIMO by controlling the port mode register B.

During timer C is stopped, this function is also stopped.

Timer Mode Register A (TMA: \$008): The timer mode register A is a 4-bit write only register which controls the timer A operation as table 16 shows. The timer mode register A is initialized to \$0 at MCU reset.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 17. The timer mode register B is initialized to \$0 by MCU reset.

The data of timer B changes at the second instruction cycle of write instruction. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed.

Timer Mode Register C (TMC: \$00D): The timer mode register C is a 4-bit write only register which selects the auto-reload function, input clock source, and prescaler divide ratio as table 18 shows. The timer mode register C is initialized to \$0 at MCU reset.

The contents of the timer mode register C can be changed at the second instruction cycle of write instruction. Therefore, it is required to initialize the timer C after the contents of the

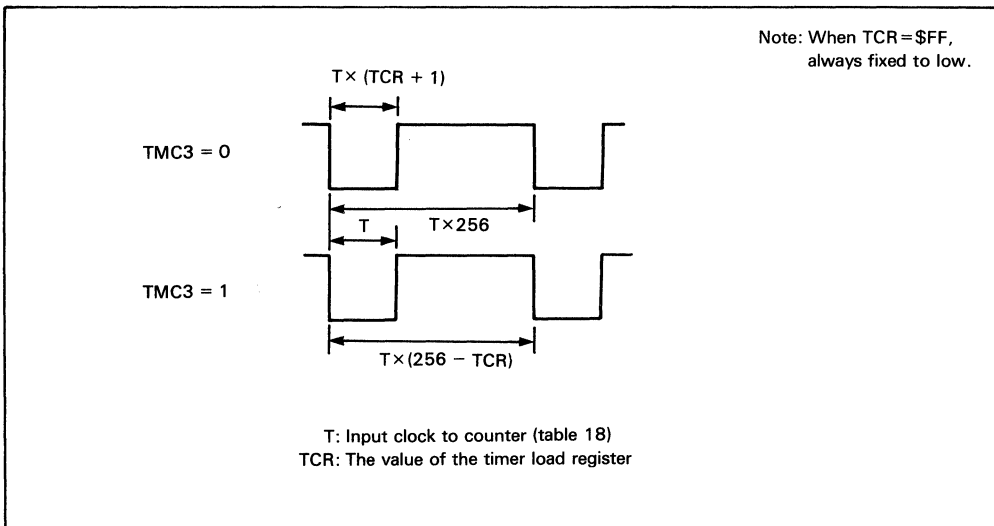


Figure 16. Variable Duty-Cycle Pulse Output Waveform



Table 16. Timer Mode Register A

TMA3	TMA2	TMA1	TMA0	Source prescaler, input clock cycle, operation mode	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

- Notes: 1. $t_{SUBcyc} = 244.14 \mu s$ (when 32.768 kHz crystal oscillation is used)
 2. Timer counter overflow output cycle(s) = Input clock cycle(s) \times 256
 3. LCD enters into halt mode when PSW/TCA reset is selected during LCD display (Power switch off). To display LCD continuously, PSW/TCA reset time must be minimized by programming.

timer mode register C has been changed completely.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit read-only timer/event counter. Each of them has low-order digits (TCBL: \$00A, TLRL: \$00A) and high-order digits (TCBU: \$00B, TLRU: \$00B). (Refer to figure 15.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digits first, and then the high-order digits. The timer/event counter is initialized when the high-order digit is written. The timer load register is

initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digits first, and then the low-order digits. The count value of the low-order digit is obtained when the high-order digit is read.

Timer C (TCCL: \$00E, TCCU: \$00F, TCRL: \$00E, TCRU: \$00F): Timer C consists of the 8-bit write-only timer load register and the 8-bit read-only timer/counter. These individually consist of low-order digits (TCCL: \$00E, TCRL: \$00E) and high-order digits (TCCU: \$00F, TCRU: \$00F). The operation mode of timer C is the same as that of timer B.

Table 17. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{\text{INT}}_1$ (External Event Input)

Table 18. Timer Mode Register C

TMC3	Auto-reload Function
0	No
1	Yes

TMC2	TMC1	TMC0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Input/Output

The MCU provides 26 I/O pins and 4 input only pins including 10 high current pins (15 mA max). 26 I/O pins contain pull-up MOS controllable by program. When each I/O is

used as an input, the data control register (DCR) controls the output buffer. Table 19 shows I/O pin circuit types.

The configuration of I/O buffers are shown in figure 19.

Table 19. I/O Pin Circuit Type

I/O pins	Circuit	Applicable pins
I/O common pins (with pull-up MOS)		D ₀ -D ₉ R ₀ -R ₀ ₃ R ₁ ₀ -R ₁ ₃ R ₂ ₀ -R ₂ ₃ R ₃ ₀ -R ₃ ₃
		$\overline{\text{SCK}}$
Output pins (with pull-up MOS)		SO TIMO
Input pins		$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$ SI
		D ₁₀ D ₁₁ /V _{Cref}
		D ₁₂ /COMPO D ₁₃ /COMP1 (Multiplexed with analog inputs)

Note: Refer to table 20, Note 3 for R₀₂/SO.

Port D: Port D is consisted of 10 1-bit I/O ports and 4 input ports. Ports D₀-D₉ are high current I/O ports (15 mA max). The sum of the current for all ports is up to 100mA. Port D can be set/reset by SED/RED and SEDD/REDD instructions, and can be tested by TD/TDD instructions. An output data is stored in the port data register. ON/OFF of the output buffer for port D can be controlled by the data control register for port D (DCRB, DCRC, DCRD). The DCR is located on the memory address area. Pins D₁₀-D₁₃ are input only pins.

Two operation modes are available for pins D₁₂ and D₁₃: digital input mode and analog input mode. The operation modes can be selected by the port mode register B (PMRB; bits 1, 0). In the digital input mode, these pins can be used as input with the same characteristics as other I/O pins. In the analog input mode, users can read the result of the comparison between the reference voltage as an input data. The reference voltage is input through D₁₁/V_{ref}.

Port R: Port R, consisting of 4 4-bit I/O ports, can receive/transmit data by LAR/LRA and LBR/LRB instructions. An output data is stored in data register (PDR) of each pin.

ON/OFF of the output buffer for port R can be controlled by the data control registers for port R (DCR0-DCR3).

The DCR is located on memory address area.

Pins R₀, R₁, R₂ are multiplexed with \overline{SCK} , SI, SO, respectively.

Pins R₃, R₃, R₃ are multiplexed with TIMO, INT₀, INT₁, respectively. Refer to figure 18.

Controlling the Pull-Up MOS: All I/O ports, except for pins D₁₀-D₁₃, contain pull-up MOS which can be controlled by program.

Bit 3 of the port mode register B (PMRB3) controls activation of all pull-up MOS simultaneously. Pull-up MOS is controlled by the port data register (PDR) of each pin. Therefore, each bit of pull-up MOS can be individually on and off. Refer to table 20.

Unused I/O Pins: If unused pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent this; pull-up with V_{CC} through internal pull-up MOS, or pull-up with V_{CC} through a 100 kΩ approx resistor.

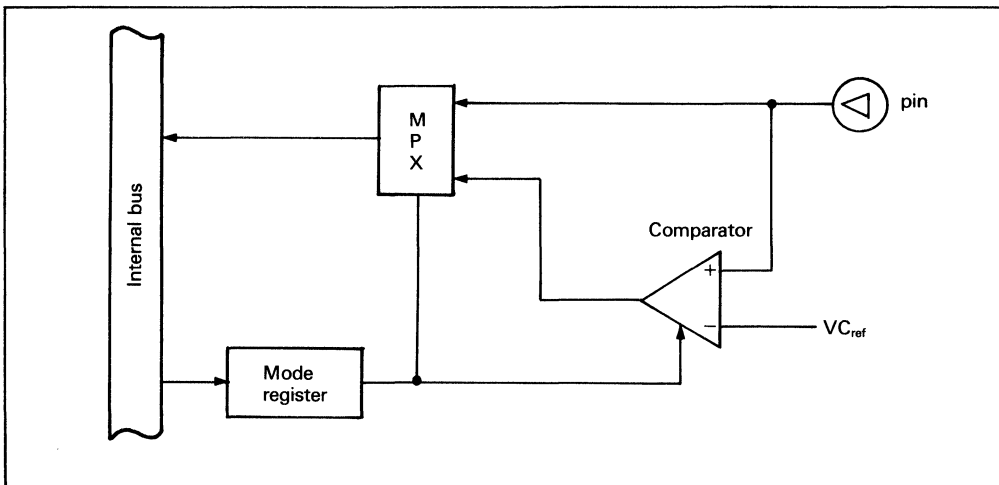


Figure 17. Configuration of D₁₂, D₁₃

Table 20. Input/Output by Program Control

PRMB; bit 3	0				1			
DCR	0	1	0	1	0	1	0	1
PDR	0	1	0	1	0	1	0	1
PMOS (A)	Off	Off	Off	On	Off	Off	Off	On
NMOS (B)	Off	Off	On	Off	Off	Off	On	Off
Pull-up MOS	Off	Off	Off	Off	Off	On	Off	On

Notes: 1. Combine the values of the above mode registers (PMRB3, DCR, PDR) to select input/output for PMOS (A), NMOS (B), and the pull-up MOS individually.
 The DCR and the PDR control each pin. And the PMRB3 controls ON/OFF of all pull-ups.
 2. The second bit of the miscellaneous register (MIS2) controls RO₂/SO. When MIS2 is 1, PMOS (A) is off.

	RO ₂ /SO
MIS2	PMOS (A)
0	On
1	Off

3. Each bit of DCR corresponds to each port as follows:

DCR	bit 3	bit 2	bit 1	bit 0
DCR 0	R0 ₃	R0 ₂	R0 ₁	R0 ₀
DCR 1	R1 ₃	R1 ₂	R1 ₁	R1 ₀
DCR 2	R2 ₃	R2 ₂	R2 ₁	R2 ₂
DCR 3	R3 ₃	R3 ₂	R3 ₁	R3 ₀
DCR B	D ₃	D ₂	D ₁	D ₀
DCR C	D ₇	D ₆	D ₅	D ₄
DCR D	—	—	D ₉	D ₈

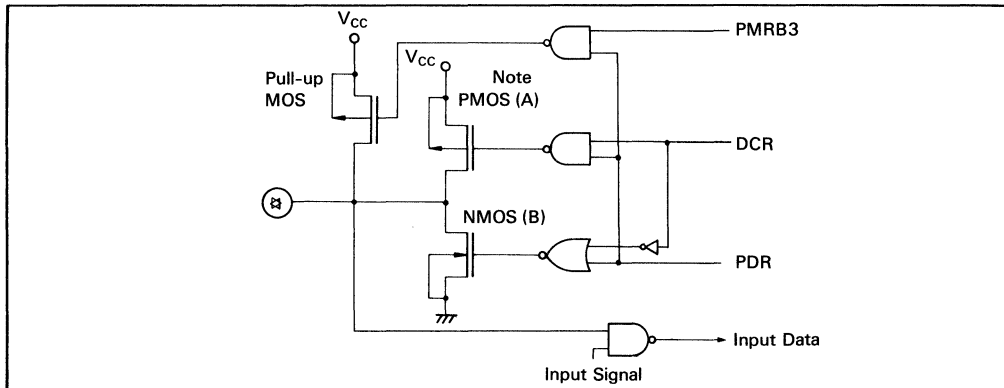


Figure 19. Configuration of the Input/Output Buffer

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when cancelling stop mode for oscillator, apply the RESET input for at least t_{RC} for the oscillator to stabilize. In all

other cases, at least two instruction cycles of RESET input are required for the MCU reset.

Table 21 shows the parts initialized by MCU reset, and each status.

Table 21. Initial Value After MCU Reset

Items		Initial value by MCU reset	Contents
Program Counter	(PC)	\$0000	Execute program from the top of the ROM address
Status	(ST)	1	Enable to branch with conditional branch instructions
Stack Pointer	(SP)	\$3FF	Stack level is 0
Register V (Bank Register) (V)		0	Bank 0 (Memory)
Interrupt	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
Flag/Mask	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Masks interrupt request
I/O	Port Data Register (PDR)	All bits are 1	Enable to transmit high
	Data Control Register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port Mode Register A (PMRA)	0000	See port mode register A
	Port Mode Register B (PMRB)	0000	See port mode register B
Timer/Counter	Timer Mode Register A (TMA)	0000	See timer mode register A
Serial Interface	Timer Mode Register B (TMB)	0000	See timer mode register B
	Timer Mode Register C (TMC)	0000	See timer mode register C
	Serial Mode Register (SMR)	0000	See serial mode register
	Prescaler S	\$000	
	Prescaler W	\$00	
	Timer Counter A (TCA)	\$00	
	Timer Counter B (TCB)	\$00	
	Timer Counter C (TCC)	\$00	
	Timer Load Register B (TLR)	\$00	
	Timer Load Register C (TCR)	\$00	
	Octal Counter	000	



Table 21. Initial Value After MCU Reset (Cont)

Items		Initial value by MCU reset	Contents
LCD	LCD Control Register (LCR)	000	See LCD control register
	LCD Mode Register (LMR)	0000	See LCD duty/clock control
Bit Register	Low Speed On Flag (LSON)	0	See low power dissipation mode
	Watch Dog Timer ON Flag (WDON)	0	See timer C
Miscellaneous Register	(MIS)	000	See miscellaneous register

Item		After recovering from STOP mode by MCU reset	After MCU reset except for the left condition
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
Register B	(B)		
Register W	(W)		
Registers X/SPX	(X/SPX)		
Registers Y/SPY	(Y/SPY)		
Serial Data Register	(SR)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	Same as above

Internal Oscillator Circuit

OSC₁-OSC₂. 32.768 kHz crystal oscillator can be connected to X1, X2. External clock operation is available for the system oscillator.

Figure 20 gives an internal oscillator circuit diagram. Ceramic filter can be connected to

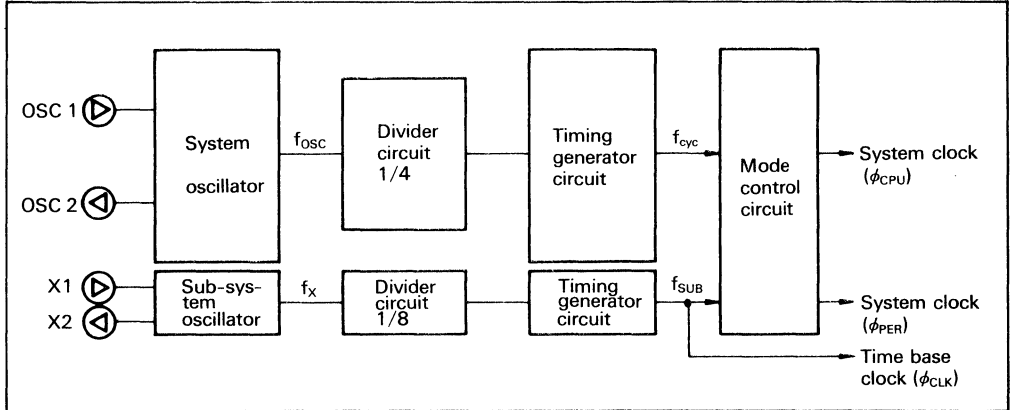


Figure 20. Internal Oscillator Circuit

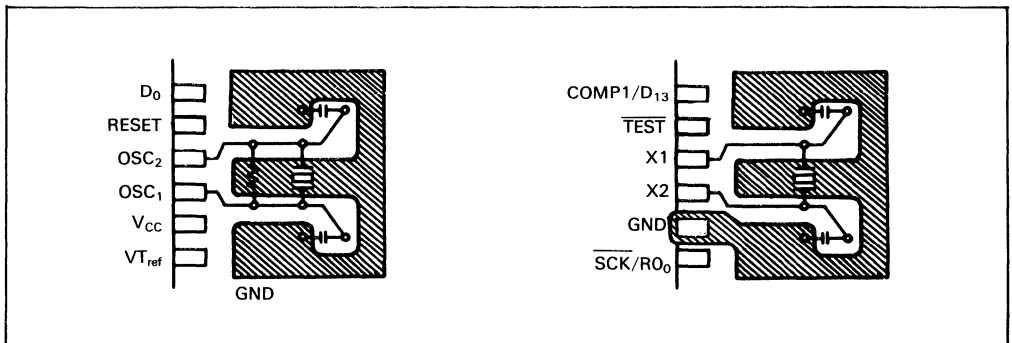
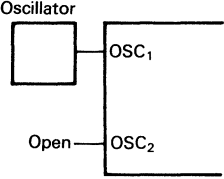
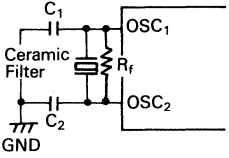
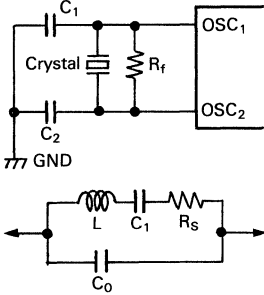
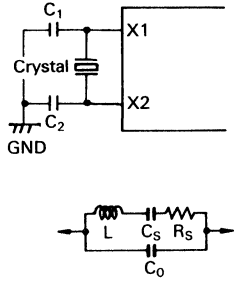


Figure 21. Layout of Crystal and Ceramic Filter

Table 22. Examples of Oscillator Circuit

	Circuit Configuration	Circuit Constants
External clock operation	 <p>Oscillator</p> <p>OSC₁</p> <p>Open</p> <p>OSC₂</p>	
Ceramic filter oscillator	 <p>C₁</p> <p>Ceramic Filter</p> <p>OSC₁</p> <p>R_f</p> <p>OSC₂</p> <p>C₂</p> <p>GND</p>	<p>HD404808, HD4074808</p> <p>Ceramic filter: CSA4.00MG (Murata)</p> <p>R_f = 1 MΩ ± 20%</p> <p>C₁ = C₂ = 30 pF ± 20%</p>
		<p>HD40L4808, HD407L4808</p> <p>Ceramic filter: CSB400P (Murata)</p> <p>R_f = 1 MΩ ± 20%</p> <p>C₁ = C₂ = 220 pF ± 5%</p> <p>Ceramic filter: CSB800J (Murata)</p> <p>R_f = 1 MΩ ± 20%</p> <p>C₁ = C₂ = 220 pF ± 5%</p>
Crystal oscillator	 <p>C₁</p> <p>Crystal</p> <p>OSC₁</p> <p>R_f</p> <p>OSC₂</p> <p>C₂</p> <p>GND</p> <p>L</p> <p>C₁</p> <p>R_s</p> <p>C₀</p>	<p>HD404808, HD4074808</p> <p>C₁: 10~22 pF ± 20%</p> <p>C₂: 10~22 pF ± 20%</p> <p>R_f: 1 MΩ ± 20%</p> <p>C₀: 7 pF max</p> <p>R_s: 100Ω max</p> <p>f = 1.0 - 4.2 MHz</p>

	Circuit Configuration	Circuit Constants
Crystal oscillator		Crystal: 32.768 kHz: MX38T (Nippon Denpa Kogyo) $C_1 = 6 \text{ pF} \pm 20\%$ $C_2 = 20 \text{ pF} \pm 20\%$ $R_s = 14 \text{ k}\Omega$ $C_0 = 1.5 \text{ pF}$

- Notes: 1. On the crystal and ceramic filter resonator, the above circuit parameters are the one recommended by crystal or ceramic filter maker. The circuit parameters are changed by crystal, ceramic filter resonator and the floated capacitance in designing the board. In employing the resonator, please consult with the engineers of crystal or ceramic filter maker to determine the circuit parameter.
2. Wiring among OSC₁, OSC₂ (X1, X2) and elements should be as short as possible, and never cross other wiring. Refer to figure 21.
3. When 32.768 kHz crystal oscillator is not used, pin X1 must be fixed to V_{CC} and pin X2 must be open.

LCD Data Area and Segment Data (\$050-\$06F): Figure 23 shows the configuration of LCD RAM area. Each bit of this area, corresponding to 4 types of duty cycles can be transmitted to segment as a display data by programming the area corresponding to the duty cycle.

LCD Control Register (LCR: \$013): The LCD control register is a 3-bit write only register which controls the blanking of the LCD, activation of the power switch and the display in the watch mode/subactive mode (table 23).

- Blank/Display
Blank: Segment signal is faded irrespective of the LCD RAM data.
Display: LCD RAM data is transmitted as a

segment signal.

- Power Switch ON/OFF
OFF: Power switch is off.
ON: Power switch is on, and V_1 is V_{CC} .
- Watch Mode/Subactive Mode Display
OFF: In the watch mode/subactive mode, all common/segment pins are fixed to GND. And power switch is off.
ON: In the watch mode/subactive mode, LCD RAM data is transmitted as a segment signal.

LCD Duty Cycle/Clock Control Register (LMR: \$014): The LCD duty cycle/clock control register is a write only register which specifies 4 display duty cycles and reference clock for LCD (table 24).

	bit 3	bit 2	bit 1	bit 0		bit 3	bit 2	bit 1	bit 0	
80	SEG 1	SEG 1	SEG 1	SEG 1	\$050	SEG 17	SEG 17	SEG 17	SEG 17	\$060
81	SEG 2	SEG 2	SEG 2	SEG 2	\$051	SEG 18	SEG 18	SEG 18	SEG 18	\$061
82	SEG 3	SEG 3	SEG 3	SEG 3	\$052	SEG 19	SEG 19	SEG 19	SEG 19	\$062
83	SEG 4	SEG 4	SEG 4	SEG 4	\$053	SEG 20	SEG 20	SEG 20	SEG 20	\$063
84	SEG 5	SEG 5	SEG 5	SEG 5	\$054	SEG 21	SEG 21	SEG 21	SEG 21	\$064
85	SEG 6	SEG 6	SEG 6	SEG 6	\$055	SEG 22	SEG 22	SEG 22	SEG 22	\$065
86	SEG 7	SEG 7	SEG 7	SEG 7	\$056	SEG 23	SEG 23	SEG 23	SEG 23	\$066
87	SEG 8	SEG 8	SEG 8	SEG 8	\$057	SEG 24	SEG 24	SEG 24	SEG 24	\$067
88	SEG 9	SEG 9	SEG 9	SEG 9	\$058	SEG 25	SEG 25	SEG 25	SEG 25	\$068
89	SEG 10	SEG 10	SEG 10	SEG 10	\$059	SEG 26	SEG 26	SEG 26	SEG 26	\$069
90	SEG 11	SEG 11	SEG 11	SEG 11	\$05A	SEG 27	SEG 27	SEG 27	SEG 27	\$06A
91	SEG 12	SEG 12	SEG 12	SEG 12	\$05B	SEG 28	SEG 28	SEG 28	SEG 28	\$06B
92	SEG 13	SEG 13	SEG 13	SEG 13	\$05C	SEG 29	SEG 29	SEG 29	SEG 29	\$06C
93	SEG 14	SEG 14	SEG 14	SEG 14	\$05D	SEG 30	SEG 30	SEG 30	SEG 30	\$06D
94	SEG 15	SEG 15	SEG 15	SEG 15	\$05E	SEG 31	SEG 31	SEG 31	SEG 31	\$06E
95	SEG 16	SEG 16	SEG 16	SEG 16	\$05F	SEG 32	SEG 32	SEG 32	SEG 32	\$06F
	COM 4	COM 3	COM 2	COM 1		COM 4	COM 3	COM 2	COM 1	

Figure 23. Configuration of LCD RAM Area (Dual Port RAM)

Table 23. LCD Control Register

LCR bit 2	Watch Mode/ Subactive Mode Display	LCR bit 1	Power Switch ON/OFF	LCR bit 0	Blank /Display
0	OFF	0	OFF	0	Blank
1	ON	1	ON	1	Display

Note: In case of LCD in the watch mode, use divider output of 32 kHz oscillator as an LCD clock and set LCR bit 2 to 1. When system oscillator divider output is used as an LCD clock, set LCD bit 2 to 0.

Table 24. LCD Duty Cycle/Clock Control Register

LMR

bit 3	bit 2	bit 1	bit 0	Duty Cycle Select/Input Clock Select
		0	0	1/4 Duty Cycle
		0	1	1/3 Duty Cycle
		1	0	1/2 Duty Cycle
		1	1	Static
0	0			CL0 (32.768 kHz/64; when 32.768 kHz oscillator is used)
0	1			CL1 ($f_{cyc}/256$)
1	0			CL2 ($f_{cyc}/2048$)
1	1			CL3 (Refer to table 25)

Note: f_{cyc} is a system oscillator divider output.

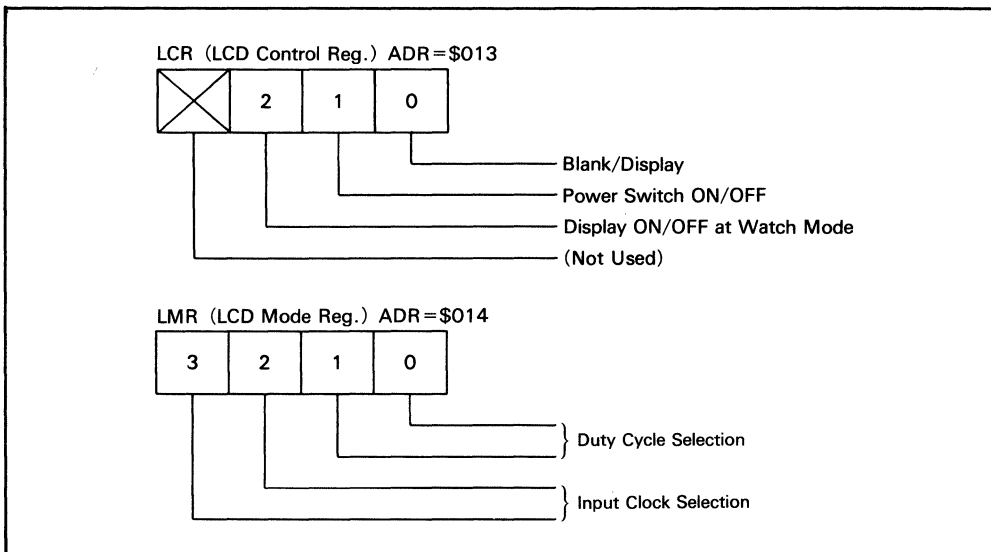


Figure 24. LCD Control Register



Table 25. LCD Frame Frequency

Duty Cycle: Static

Instruction Cycle Time	LMR	bit 3 0 CLO	bit 2 0	bit 3 0 CL1	bit 2 1	bit 3 1 CL2	bit 2 0	bit 3 1 CL3	bit 2 1 *
	10 μ s			512Hz		390.6Hz		48.8Hz	
1 μ s			512Hz		3906Hz		488Hz		244Hz/64Hz

Duty Cycle: 1/2

Instruction Cycle Time	LMR	bit 3 0 CLO	bit 2 0	bit 3 0 CL1	bit 2 1	bit 3 1 CL2	bit 2 0	bit 3 1 CL3	bit 2 1 *
	10 μ s			256Hz		195.3Hz		24.4Hz	
1 μ s			256Hz		1953Hz		244Hz		122Hz/32Hz

Duty Cycle: 1/3

Instruction Cycle Time	LMR	bit 3 0 CLO	bit 2 0	bit 3 0 CL1	bit 2 1	bit 3 1 CL2	bit 2 0	bit 3 1 CL3	bit 2 1 *
	10 μ s			170.6Hz		130.2Hz		16.3Hz	
1 μ s			170.6Hz		1302Hz		162.6Hz		81.3Hz/21.3Hz

Duty Cycle: 1/4

Instruction Cycle Time	LMR	bit 3 0 CLO	bit 2 0	bit 3 0 CL1	bit 2 1	bit 3 1 CL2	bit 2 0	bit 3 1 CL3	bit 2 1 *
	10 μ s			128Hz		97.7Hz		12.2Hz	
1 μ s			128Hz		977Hz		122Hz		61Hz/16Hz

* Division ratio differs depending on the value of bit 3 of the timer mode register (TMA3) (TMA3 = 0/
TMA3 = 1).

$$\begin{array}{l} \text{TMA3=0} \quad \text{CL3} = f_{\text{cyc}} / 4096 \\ \text{TMA3=1} \quad \text{CL3} = 32.768 \text{ kHz} / 512 \end{array}$$

Large LCD Panel Driving and Driving Voltage (V_{LCD}): When using a large LCD panel, lower the dividing resistance by attaching external resistors parallelly to the internal dividing resistors. (See figure 25.)

Since the liquid crystal display board is matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, since it varies depending on display condition, a value of resistance cannot be simply determined by referring to the load

capacitance of liquid crystal display. A value of resistance must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented. Capacitor C (0.1 to 0.3 μF) is recommended to be attached. In general, R is 1 k Ω to 10 k Ω .

Figure 25 shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, power supply switch for dividing resistor (power switch) must be turned OFF. (Bit 1 of the LCR register is 0).

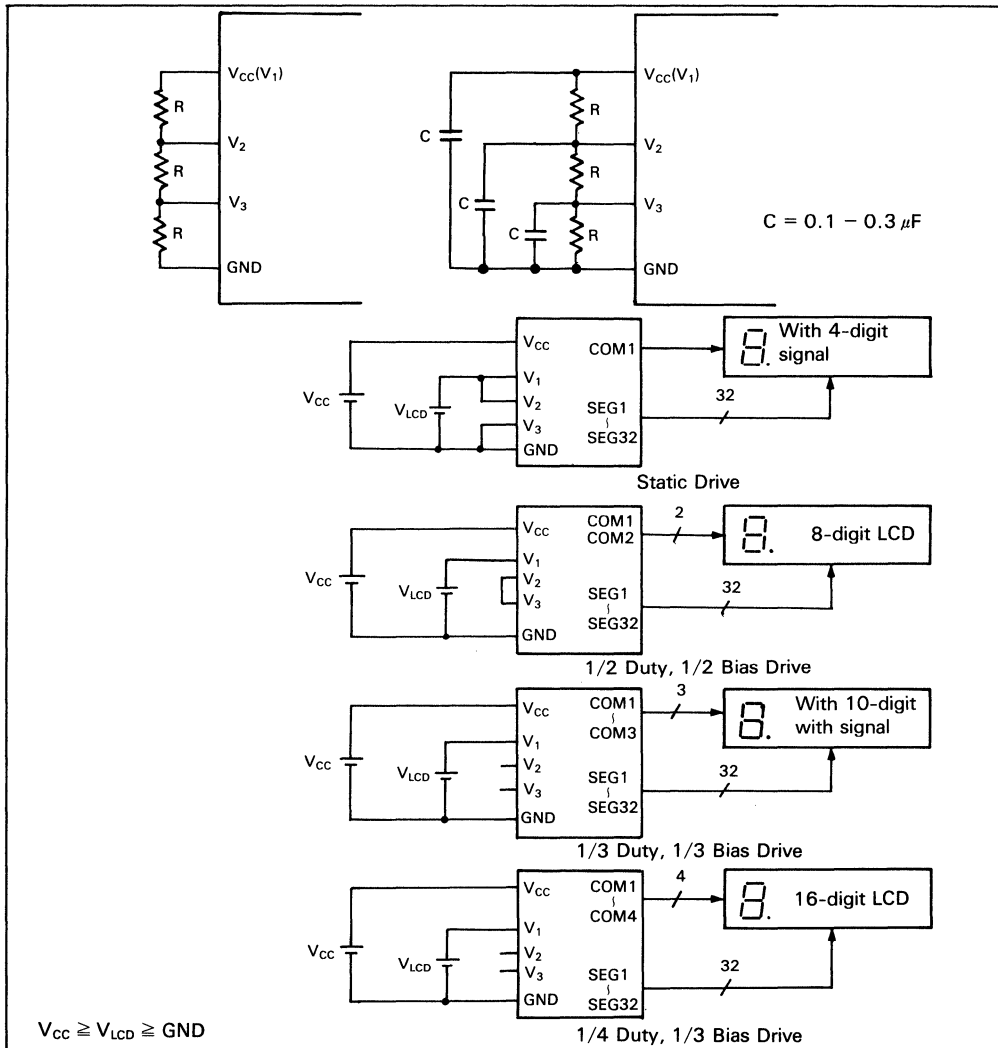


Figure 25. An Example of LCD Connection



Operating Modes

Low Power Dissipation Mode

The MCU has five operation modes.

Active Mode: In the active mode, the MCU operates through clocks generated in the oscillator circuits: OSC₁ and OSC₂.

Standby mode: Execute SBY instruction to put the MCU into the standby mode from the active mode. In standby mode, the oscillator circuit is active and interrupts, timer/counter, and the serial interface continue working. On the other hand, the CPU stops since the clock

related to the instruction execution stops. Registers, RAM, and I/O pins retain their previous states.

Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 after instruction execution, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction. (figure 27)

Table 26. Low Power Dissipation Mode Function

Operating Mode	Activated by	System oscillator	Sub-system oscillator	Instruction execution (ϕ CPU)	Peripheral interrupt (ϕ PER)	Condition				Released by
						Clock interrupt (ϕ CLK)	RAM	Register/Flag	I/O	
Active mode	RESET release Interrupt request	Active	Active	Active	Active	Active	Active	Active	Active ³	RESET input STOP/SBY instruction
Standby mode	STBY instruction	Active	Active	Stop	Active	Active	Hold	Hold	Hold	RESET input Interrupt request
Stop mode	TMA3 = 0, Stop Stop instruction		Active ¹	Stop	Stop	Stop	Hold	Reset	High impedance ³	RESET input
Watch mode	TMA3 = 1, Stop Stop instruction		Active	Stop	Stop	Active ²	Hold	Hold	Hold ³	Reset input INT ₀ or Timer A interrupt request
Sub-active ⁴ mode	INT ₀ from watch mode or Timer A interrupt request	Stop	Active	Active	Stop	Active ²	Active	Hold/ Active	Active	RESET input STOP/SBY instruction


- Notes:
1. To minimize I_{CC}, stop the oscillation by external circuit.
 2. Refer to interrupt frame section for details.
 3. Refer to table 27.
 4. Sub-active mode is a functional option specified via function option list.
 5. On using watch mode or Sub-active mode, 32.768 kHz crystal oscillator is essential for MCU.

Table 27. I/O State in the Low Power Dissipation Mode

	Output		Input
	Standby mode, Watch mode	Stop mode	Active mode, Sub-active mode
D ₀ -D ₉	Retained	High impedance	Input enable
D ₁₀ -D ₁₃			Input enable
RO-R3	Retained	High impedance	Input enable

Table 28. Operations in the Low Power Dissipation Mode

Functions	Stop mode	Watch mode	Standby mode	Sub-active mode ³
CPU	Reset	Hold	Hold	Active
RAM	Hold	Hold	Hold	Active
Timer A	Reset	Active	Active	Active
Timer B	Reset	Stop	Active	Stop
Timer C	Reset	Stop	Active ²	Stop
Serial	Reset	Stop ⁴	Active	Stop ⁴
LCD	Reset	Active/ Stop	Active	Active/ Stop
I/O	Reset ¹	Hold ¹	Hold	Active

- Notes: 1. Output pins are in the high impedance state.
 2. : in operation
 3. Sub-active mode is a functional option specified via functional option list.
 4. When a clock is input in the external clock mode, transmit-receive operation is performed. (Interrupt processing stops.)

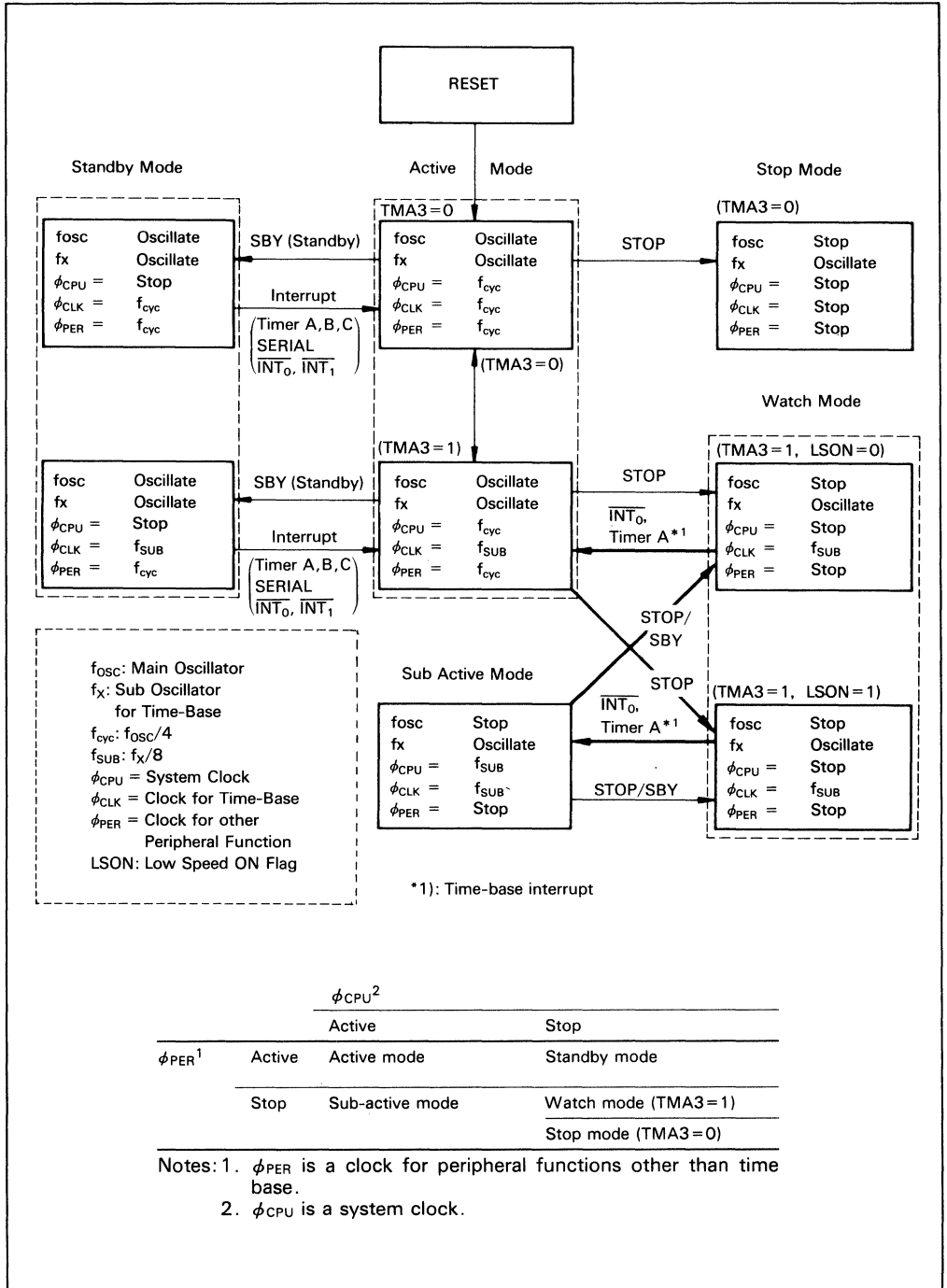


Figure 26. MCU Operation Mode Transfer



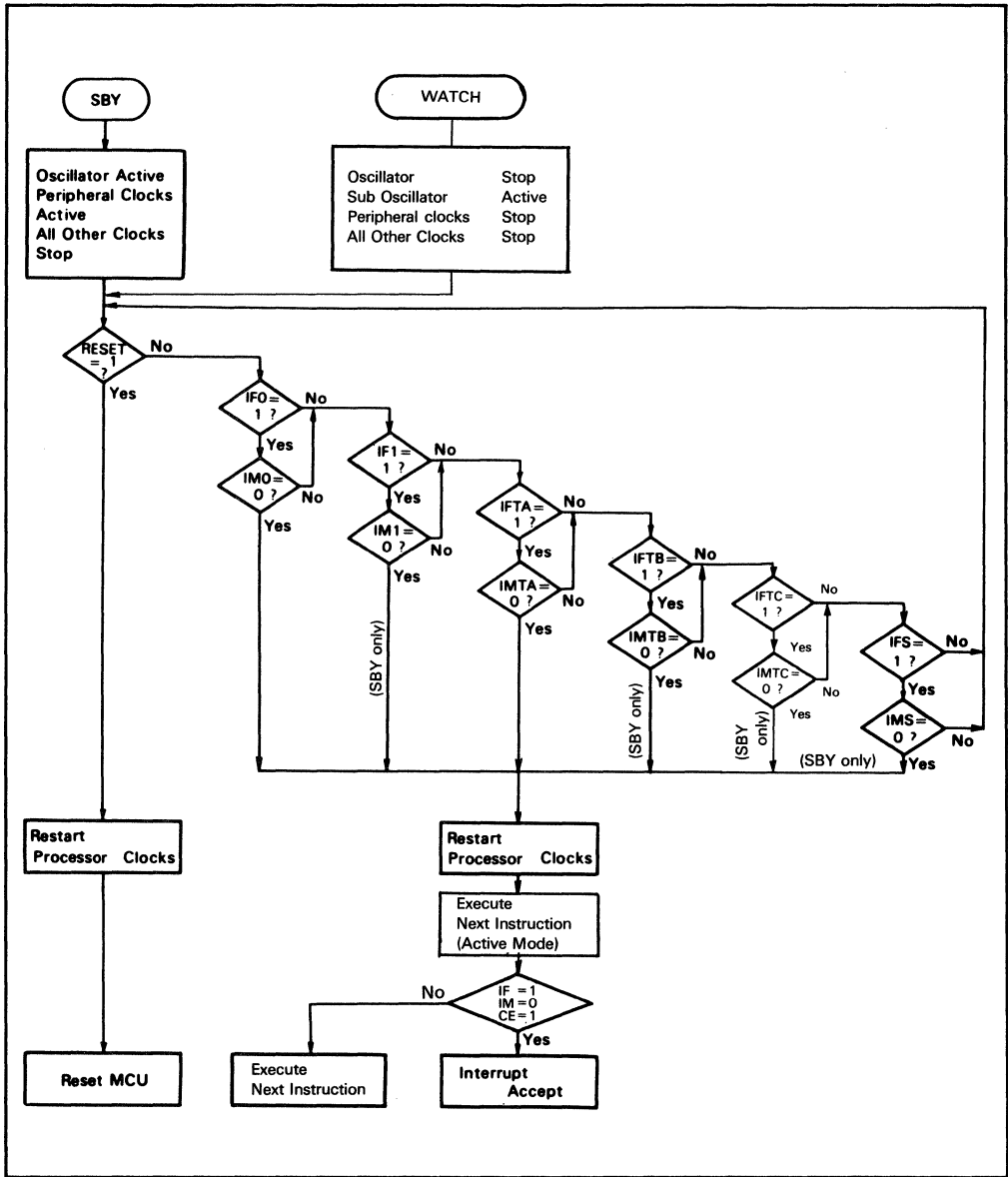


Figure 27. MCU Operating Flowchart

Stop Mode: Execute STOP instruction to put the MCU into the stop mode when the MCU is in the active mode and TMA3 is 0. In the stop mode, oscillator circuit and every function of the MCU stops.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 28, reset input must be applied at least t_{RC} to stabilize oscillation. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the previous state, but the accumulator, register B, register W, registers X/SPX and Y/SPY, and carry may not retain their contents.

Watch Mode: The MCU enters Watch mode by the STOP instruction during Active mode and TMA3 = 1 or by the STOP or SBY instruction during Sub Active mode. Watch mode can be canceled by the RESET input or timer A/INT₀ interrupt request. For a detailed description of the RESET input in canceling mode, see Stop mode section. If Watch mode is canceled by the timer A/INT₀ interrupt request, the MCU enters either Active mode or Sub Active mode depending on the state of the LSON bit. When the MCU enters Active mode, the interrupt request is delayed for a half of the interrupt frame period (t_{RC}) in order to wait stabilization of the system oscillation (figure 29). In this case, MCU

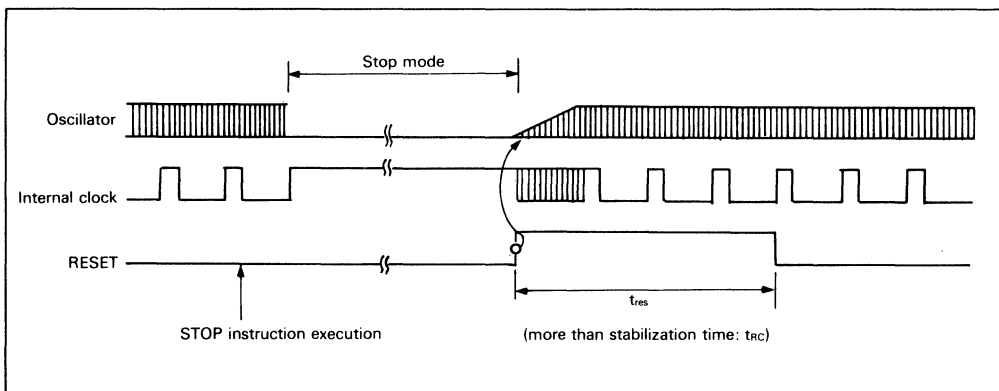


Figure 28. Timing Chart of Recovering from Stop Mode

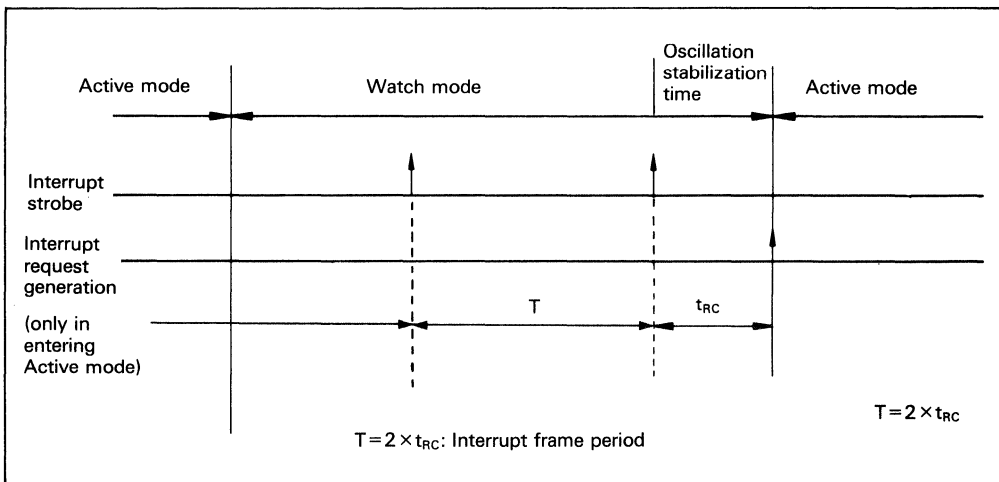


Figure 29. Interrupt Frame

operation is the same as that when canceling Standby mode (figure 27).

Sub-Active Mode: In the sub-active mode, the MCU operates with the clock generated in the oscillator circuit; X1-X2. Timer A/ \overline{INT}_0 interrupt is generated in this mode with the timing synchronously with the interrupt frame timing.

Note that sub-active mode is a functional option. Therefore sub-active is available for the devices provided with this option.

Interrupt Frame: In Watch mode and Sub Active mode, the time-base clock (ϕ_{CLK}) is applied to timer A and the \overline{INT}_0 circuit. Prescaler W and timer A operates as the time-base and generate the timing clock for the interrupt frame. The interrupt frame period

(T) depends on the state of the miscellaneous register as shown in figure 30.

In Watch mode and Sub Active mode, the timer A/ \overline{INT}_0 interrupt occurs synchronously with the interrupt strobe timing clock. When the MCU wakes up to Active mode from Watch mode, the interrupt request is delayed for a half of interrupt frame period (t_{RC}). The falling edge of \overline{INT}_0 , which is input regardless of the interrupt frame clock cycle, is equivalent to that synchronous with the interrupt strobe clock just after the falling edge. During oscillation stabilization (t_{RC}) the falling edge of \overline{INT}_0 is not recognized. An overflow and interrupt request in timer A occurs synchronously with the interrupt strobe clock.

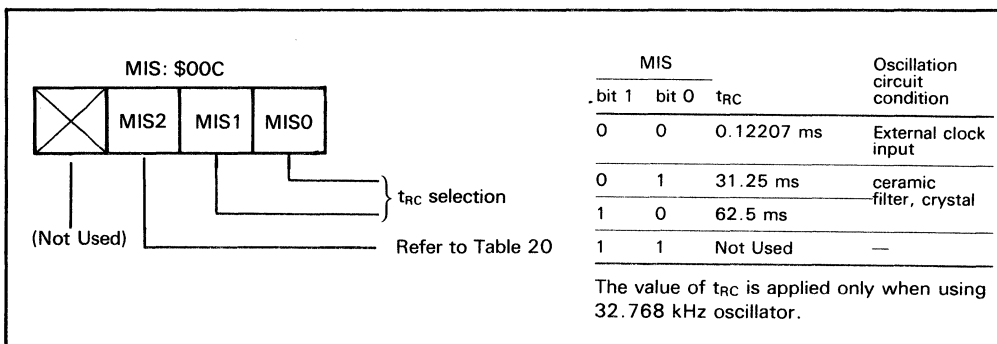


Figure 30. Miscellaneous Register

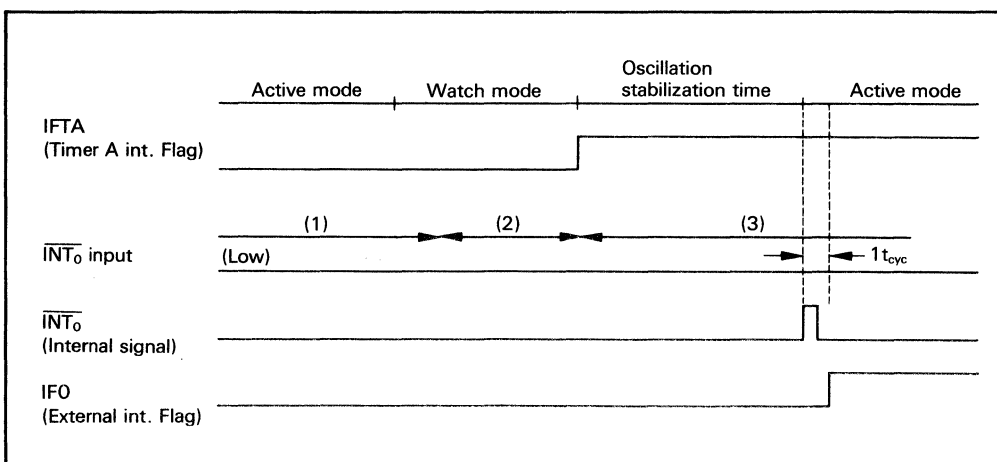


Figure 31. \overline{INT}_0 Detect Timing

Limitation on Use

Please pay attention to the following items.

When MCU goes from watch mode to active mode by timer A interrupt request under the following conditions, the timer A interrupt request flag (IFTA) and also the external interrupt request flag (IF0) will be set.

- (1) MCU goes from active mode to watch mode in \overline{INT}_0 low state.
- (2) \overline{INT}_0 is low state during watch mode.
- (3) MCU goes from watch mode to active mode by timer A interrupt in \overline{INT}_0 low state.

Interrupt flag will be set by falling edge of \overline{INT}_0 input signal and will not be set without

this edge in regular case. However the internal \overline{INT}_0 signal is initialized during 1st t_{cyc} after the MCU transition from watch mode to active mode by timer A interrupt, therefore the falling edge will be generated internally with \overline{INT}_0 low state during this 1st t_{cyc} . This edge will cause to set IF0. (figure 31)

The \overline{INT}_0 input must be high if MCU goes from watch mode to active mode by the timer A interrupt.

MCU Operating Sequence

The MCU operates according to the flowcharts shown in figures 32 to 34.

Note that RESET input is asynchronous. Therefore, the MCU is reset immediately after the RESET input supply.

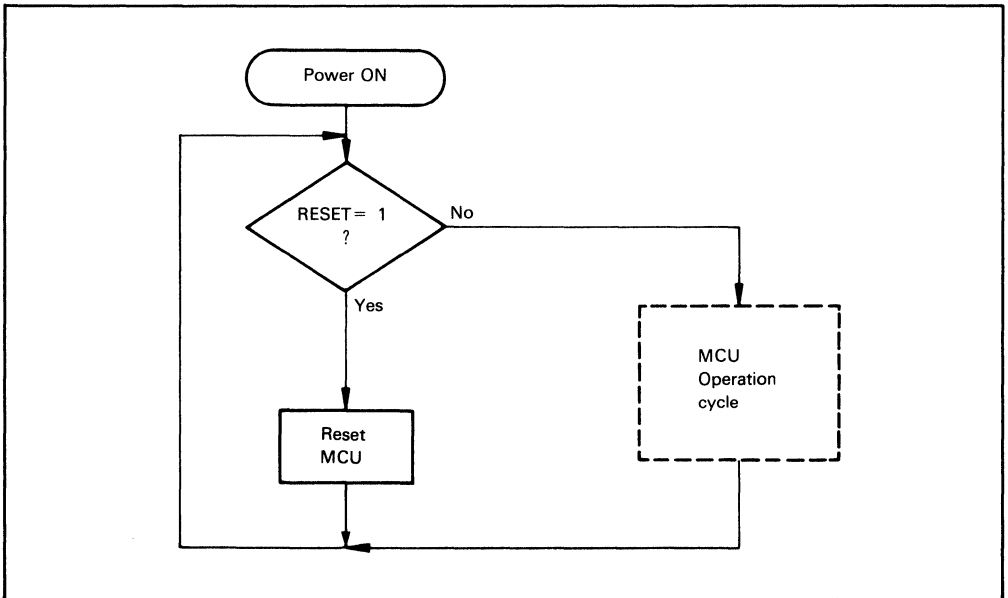


Figure 32. MCU Operating Sequence (Power On)

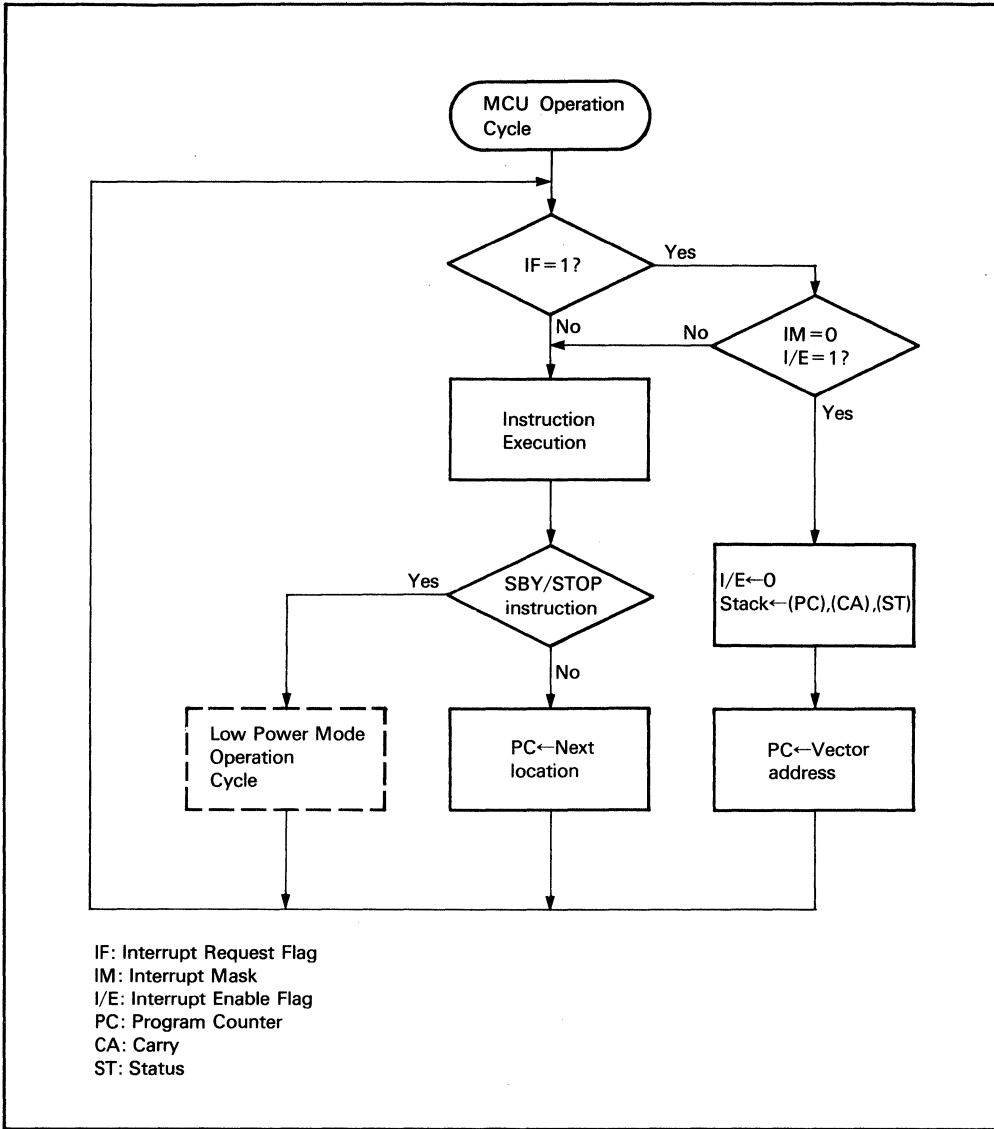


Figure 33. MCU Operating Sequence (MCU Operation Cycle)

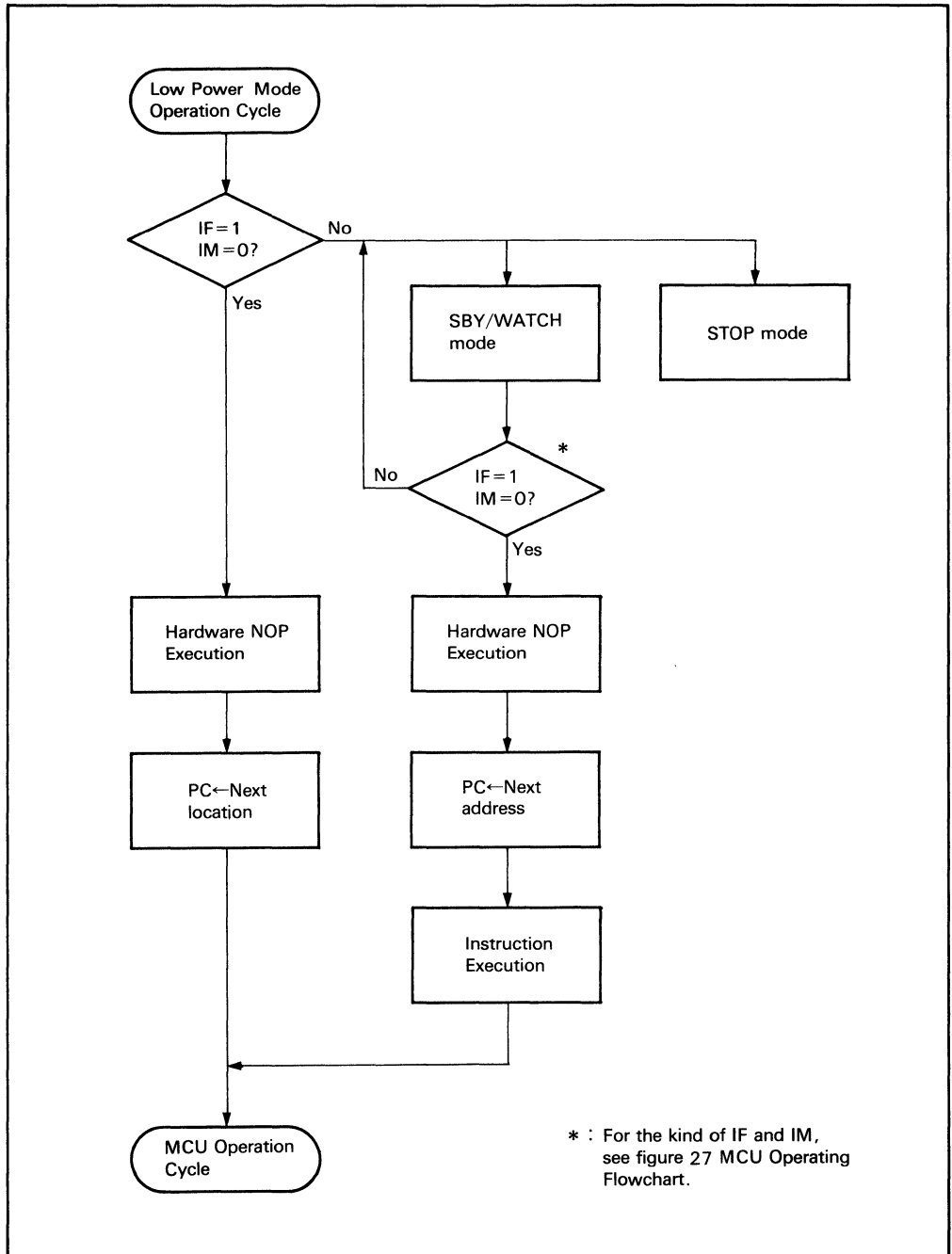


Figure 34. MCU Operating Sequence (Low Power Mode Operation)

HD404808/HD4074808/HD40L4808/HD407L4808

Pin Description in PROM Mode

The HD4074808/HD407L4808 is a ZTAT microcomputer incorporating PROM. In the

PROM mode, the MCU does not operate and the HD4074808/HD407L4808 can program the on-chip PROM.

Pin No.		MCU Mode		PROM Mode		Pin No.		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	D ₂	I/O	O ₂	I/O	41	39	SEG9	O		
2	80	D ₃	I/O	O ₃	I/O	42	40	SEG10	O		
3	1	D ₄	I/O	O ₄	I/O	43	41	SEG11	O		
4	2	D ₅	I/O	O ₅	I/O	44	42	SEG12	O		
5	3	D ₆	I/O	O ₆	I/O	45	43	SEG13	O		
6	4	D ₇	I/O	O ₇	I/O	46	44	SEG14	O		
7	5	D ₈	I/O			47	45	SEG15	O		
8	6	D ₉	I/O			48	46	SEG16	O		
9	7	D ₁₀	I	V _{PP}		49	47	SEG17	O		
10	8	D ₁₁ /V _{Cref}	I	A ₉	I	50	48	SEG18	O		
11	9	D ₁₂ /COMPO	I	M ₀	I	51	49	SEG19	O		
12	10	D ₁₃ /COMP1	I	M ₁	I	52	50	SEG20	O		
13	11	TEST	I	TEST	I	53	51	SEG21	O		
14	12	X1	I	GND		54	52	SEG22	O		
15	13	X2	O			55	53	SEG23	O		
16	14	GND		GND		56	54	SEG24	O		
17	15	R0 ₀ /SCK	I/O	A ₁	I	57	55	SEG25	O		
18	16	R0 ₁ /SI	I/O	A ₂	I	58	56	SEG26	O		
19	17	R0 ₂ /SO	I/O	A ₃	I	59	57	SEG27	O		
20	18	R0 ₃	I/O	A ₄	I	60	58	SEG28	O		
21	19	R1 ₀	I/O	A ₅	I	61	59	SEG29	O		
22	20	R1 ₁	I/O	A ₆	I	62	60	SEG30	O		
23	21	R1 ₂	I/O	A ₇	I	63	61	SEG31	O		
24	22	R1 ₃	I/O	A ₈	I	64	62	SEG32	O		
25	23	R2 ₀	I/O	A ₀	I	65	63	COM1	O		
26	24	R2 ₁	I/O	A ₁₀	I	66	64	COM2	O		
27	25	R2 ₂	I/O	A ₁₁	I	67	65	COM3	O		
28	26	R2 ₃	I/O	A ₁₂	I	68	66	COM4	O		
29	27	R3 ₀	I/O	A ₁₃	I	69	67	V ₁			
30	28	R3 ₁ /TIMO	I/O	A ₁₄	I	70	68	V ₂			
31	29	R3 ₂ /INT ₀	I/O	CE	I	71	69	V ₃		V _{CC}	
32	30	R3 ₃ /INT ₁	I/O	OE	I	72	70	NUMO	O		
33	31	SEG1	O			73	71	NUMO	O		
34	32	SEG2	O			74	72	NUMG		V _{CC}	
35	33	SEG3	O			75	73	V _{CC}		V _{CC}	
36	34	SEG4	O			76	74	OSC ₁	I	V _{CC}	
37	35	SEG5	O			77	75	OSC ₂	O		
38	36	SEG6	O			78	76	RESET	I	RESET	I
39	37	SEG7	O			79	77	D ₀	I/O	O ₀	I/O
40	38	SEG8	O			80	78	D ₁	I/O	O ₁	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin



Pins for PROM Mode (HD4074808)

V_{PP}: Apply the programming voltage (12.5 V ± 0.3 V) to V_{PP}.

CE: Program the internal PROM and input the control signal to enable verify.

OE: Input the data output control signal when verifying.

A₀-A₁₄: A₀-A₁₄ are address input pins of the internal PROM.

O₀-O₇: O₀-O₇ are data bus I/O pins of the internal PROM.

M₀, M₁: M₀, M₁ are for PROM mode specification. To put the MCU into the PROM mode, pull M₀, M₁, and TEST low, and RESET high.

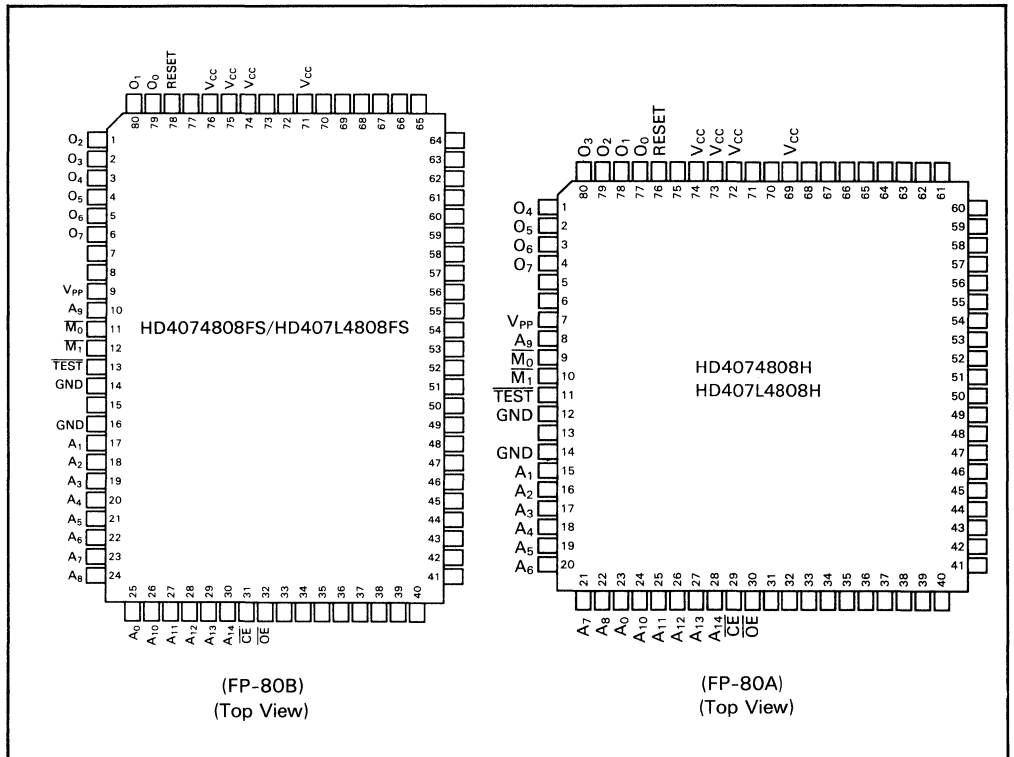


Figure 35. PROM Mode Pin Arrangement

Programmable ROM Operation

The MCU on-chip PROM is programmed in PROM mode (figures 36, 37). PROM mode is set by bringing TEST, M₀, and M₁ low, and RESET high as shown in figure 36. In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Table 30 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporates a conversion circuit to use a general purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits as shown in figure 37. For example, if 8 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 16 kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming And Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 29 shows how programming and veri-

fication modes are selected.

Figure 38 is a programming flowchart, and figure 39 is a timing chart. For precautions on PROM programming, refer to ZTAT MCU On-Chip PROM Characteristics and Precautions for Applications.

Precautions

1. Addresses \$0000 to \$3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. Data in unused addresses must be set to \$FF.
2. Be careful that the PROM programmer, socket adapter and LSI match. Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with V_{PP}=12.5 V. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Table 29. PROM Mode Selection

Mode	Pin			O ₀ -O ₇
	CE	OE	V _{PP}	
Programming	Low	High	V _{PP}	Data input
Verify	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance

Table 30. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type name	Maker	Type name	Package Type
DATA I/O	121B	Hitachi	HS460ESF01H	FP-80B
	29B		HS460ESF03H	FP-80A
AVAL Corp	PKW-1000	Hitachi	Under Development	
			HS460ESF01H	FP-80B
			HS460ESF03H	FP-80A
			Under Development	

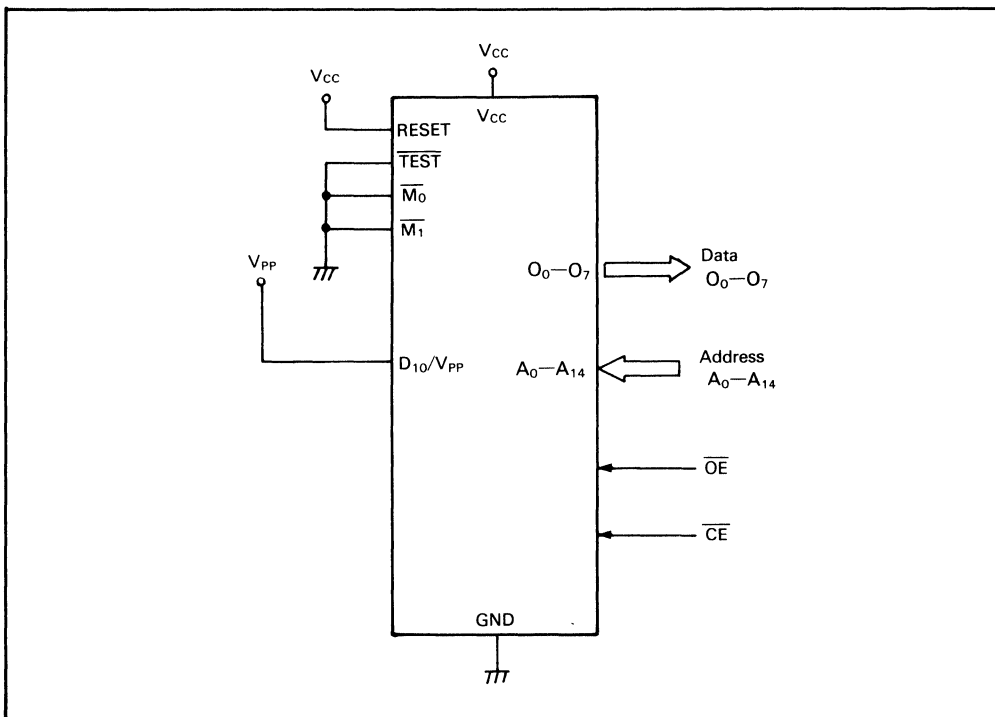


Figure 36. PROM Mode Function Diagram

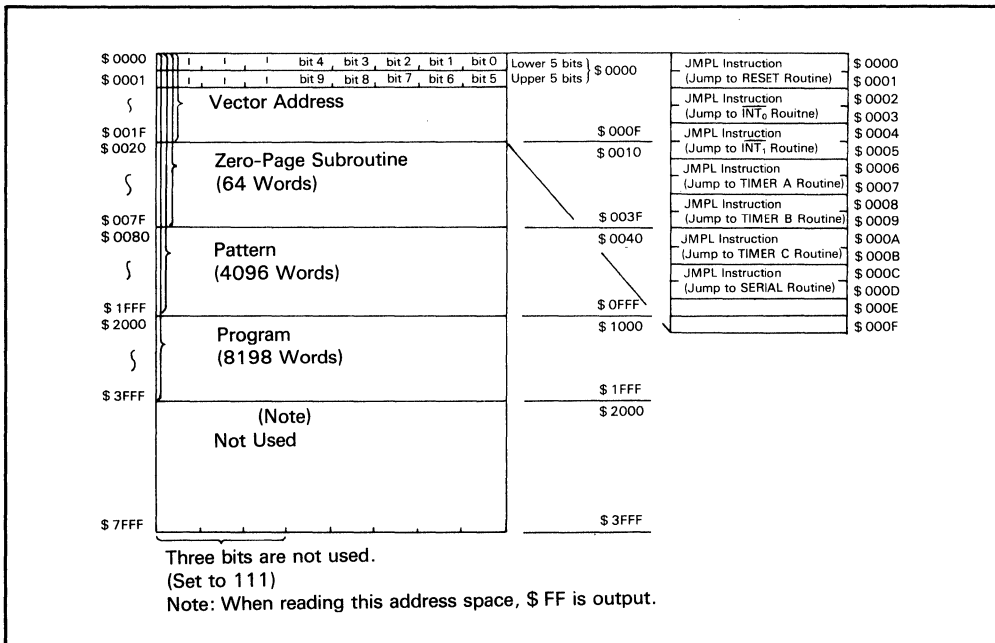


Figure 37. PROM Mode Memory Map



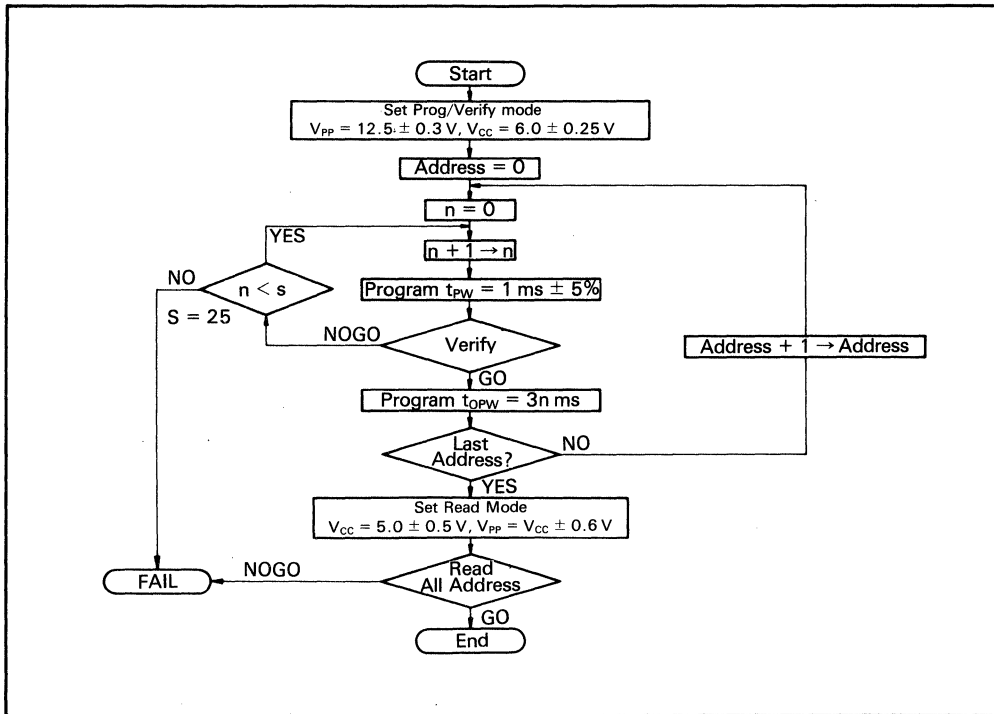


Figure 38. High Speed Programming Flowchart

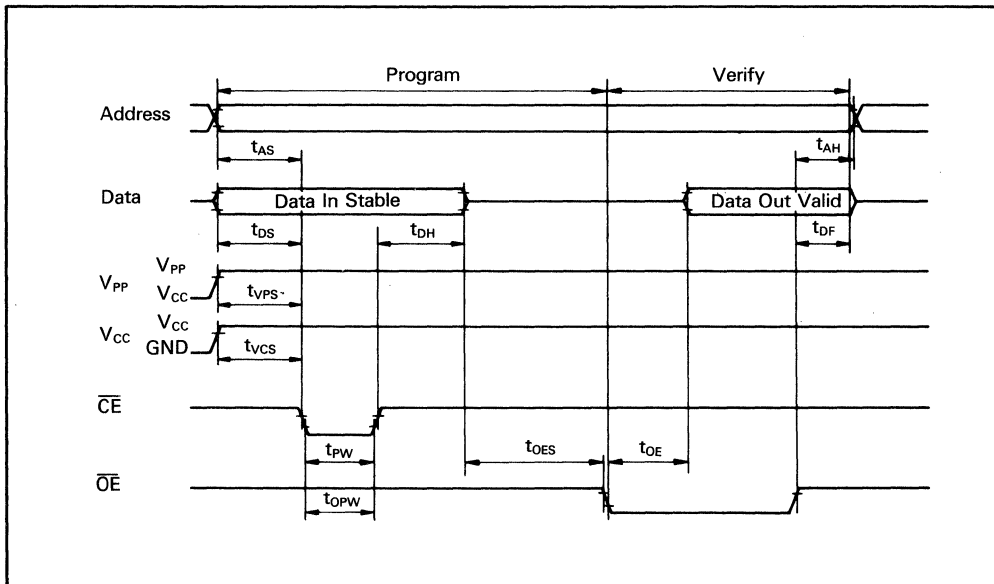


Figure 39. PROM Program/Verify Timing

Programming Electrical Characteristics

DC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS}=0\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise noted.)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		5.5	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\text{ }\mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{LI} $			2	μA	$V_{in} = 5.25\text{ V}/0.5\text{ V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC}=6\text{ V} \pm 0.25\text{ V}$, $V_{PP}=12.5\text{ V} \pm 0.3\text{ V}$, $T_a=25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time	t_{AS}	2			μs	Figure 38*
\overline{OE} set-up time	t_{OES}	2			μs	
Data set-up time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} set-up time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

* Input pulse level 0.8 to 2.2 V
Input rising/falling time $\leq 20\text{ ns}$

Timing reference level { input: 1.0 V, 2.0 V
output: 0.8 V, 2.0 V

Precautions on PROM Programming

Principles of PROM Programming/Erasing

The ZTAT microcomputer has the same type of the memory cell as the EPROM. The PROM is programmed by applying high voltage to the control gate and drain and injecting hot electrons into the floating gate, in the same way in the EPROM programming. The electrons in the floating gate remains stabilized, surrounded by the energy barrier of SiO₂ film. By this electrons, the threshold voltage in the memory cell changes and the corresponding bit goes to 0.

The hot electrons are reduced as over time. This reduction is caused by:

1. Ultraviolet light.....The electrons are discharged by the ultraviolet light (erasure principle)
2. HeatThe electrons, which are excited by heat, are discharged
3. Application of high voltage...The number of electrons is reduced due to the high voltage which is applied to the control gate and drain

If there is any failure in the oxide film, the charge is markedly reduced; however, in general, such reduction does not occur, since devices which failed are usually excluded

during screening tests.

When the memory cell does not have any hot electrons in the floating gate, the corresponding bit goes to 1.

PROM Programming

PROM programming should be performed under specified voltage and timing conditions. The higher the program voltage (V_{PP}) and the longer the program pulse width (t_{pw}), the more electrons will be injected into the memory cell. If an overvoltage is applied, a P-N junction may be permanently damaged. It is especially important to note that an overshoot occurs in the PROM writer. Moreover, negative voltage noise caused a parasitic transistor effect, which can reduce the apparent breakdown voltage.

During PROM programming, the ZTAT microcomputer is electrically connected with the PROM writer via the socket adapter. The user should ensure the following:

1. Confirm that the socket adapter is firmly connected to the PROM writer before beginning PROM programming.
2. Do not touch the socket adapter and the LSI during programming; this can cause faulty contacts, resulting in programming errors.

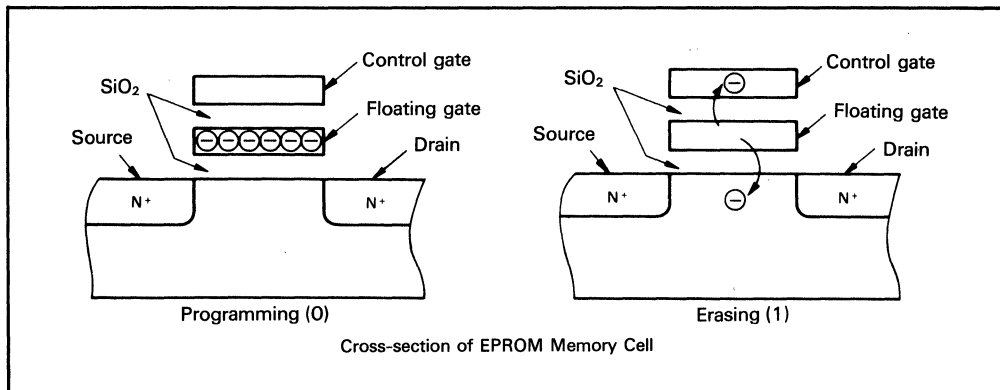


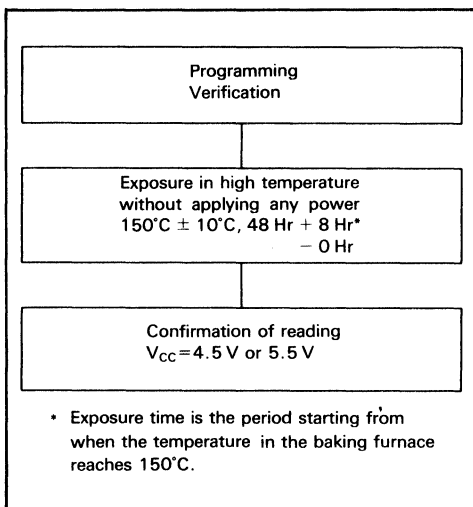
Figure 40. Cross Section of PROM Memory Cell

PROM Reliability after Programming

In general, semiconductor devices retain their reliability, if some initial failures can be rejected. Initial failures can be rejected by adequate screening. Baking the device under high-temperature conditions is a screening method which eliminates initial shorttime data hold failures in the memory cell. (See Principles of PROM Programming/Erasing).

ZTAT microcomputer devices realize good reliability because they have been subjected to such screenign during the water fabrication process. It is recommended that the user expose the device to 150°C at one atmosphere after programming in order to verify device performance.

Figure 41 shows the recommended screening procedure.



(note) If programming errors occur sequentially during PROM programming, the user should suspend programming and determine whether there is any trouble with the PROM writer or the socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi of the trouble.

Figure 41. Recommended Screening Procedure

RAM Addressing Mode

As shown in figure 42, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four kinds of ROM addressing modes, as shown in figure 43.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with the 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC_7 to PC_0) with the 8-bit immediate data.

When BR is on a page boundary ($256n + 255$) (figure 44), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bit immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 45). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

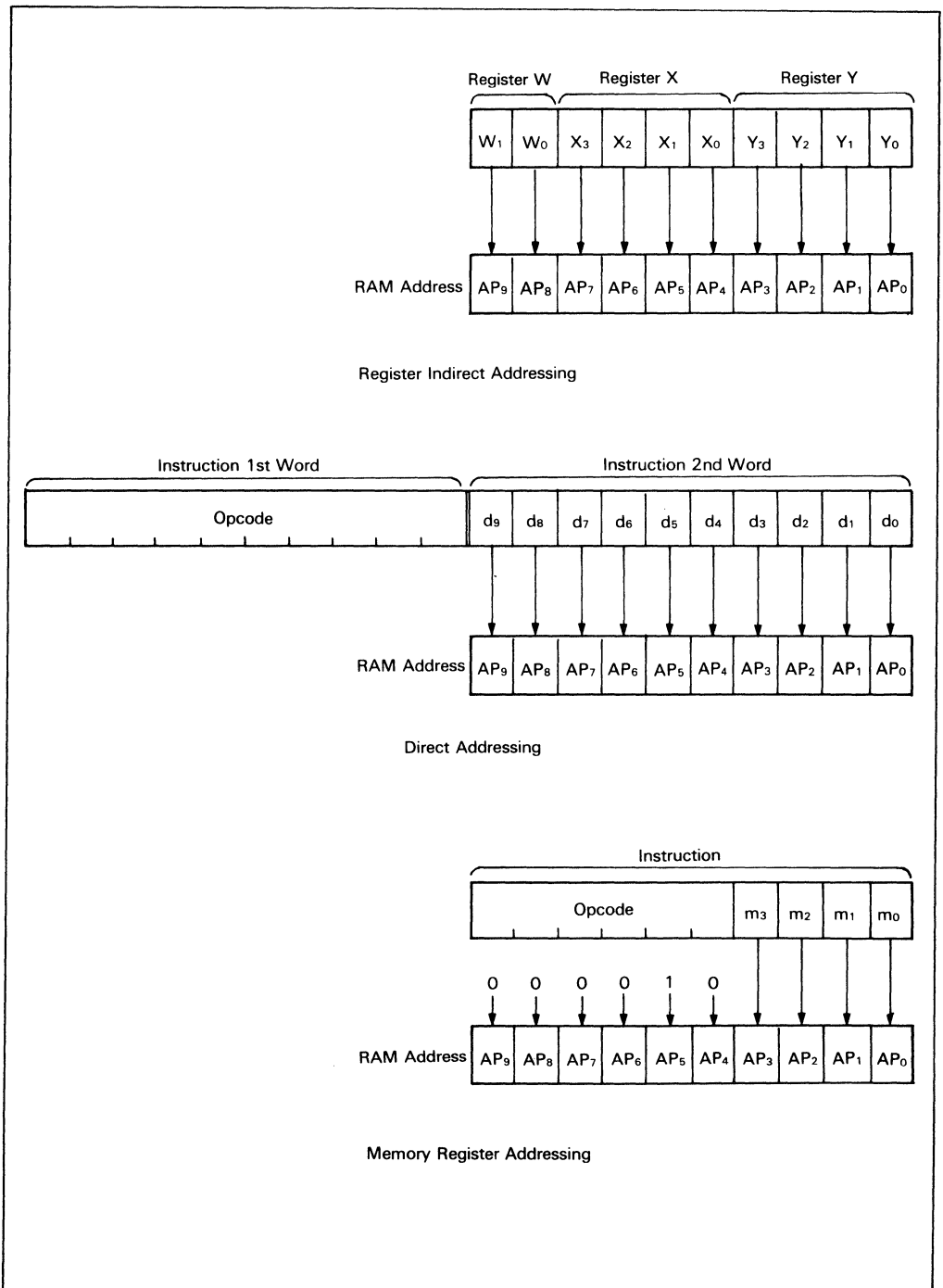


Figure 42. RAM Addressing Mode

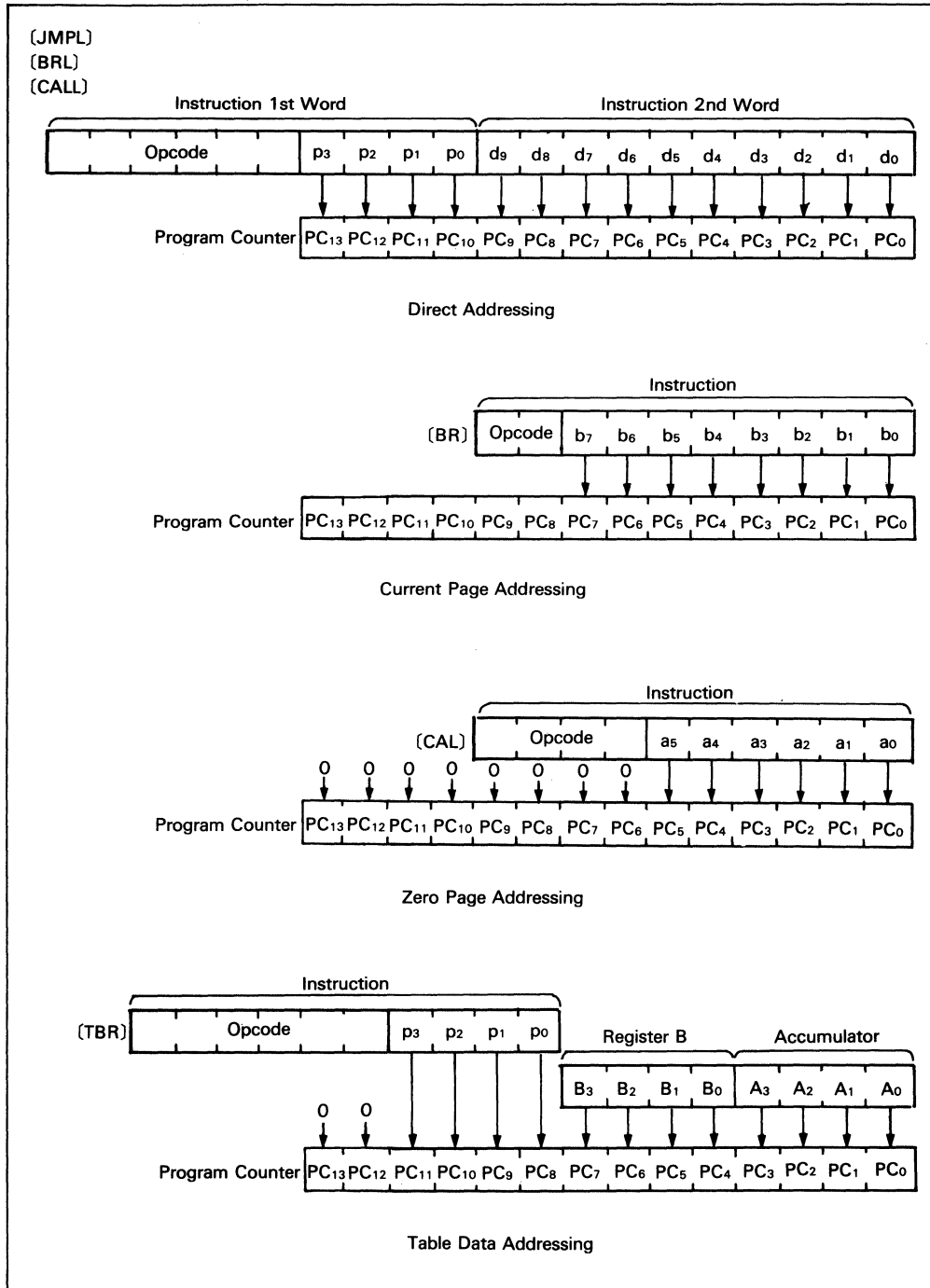


Figure 43. ROM Addressing Mode



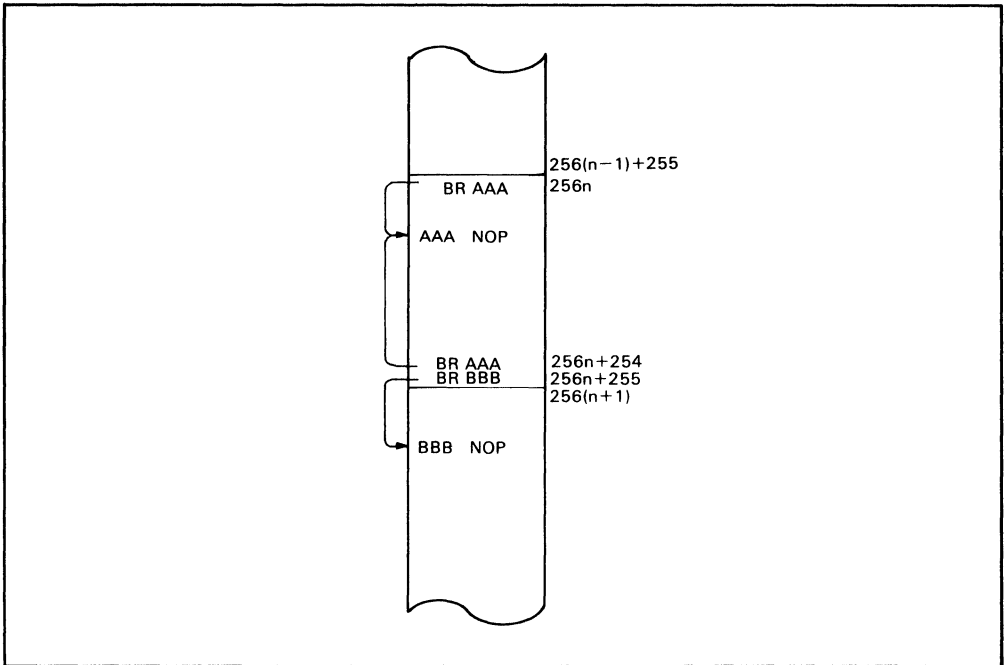
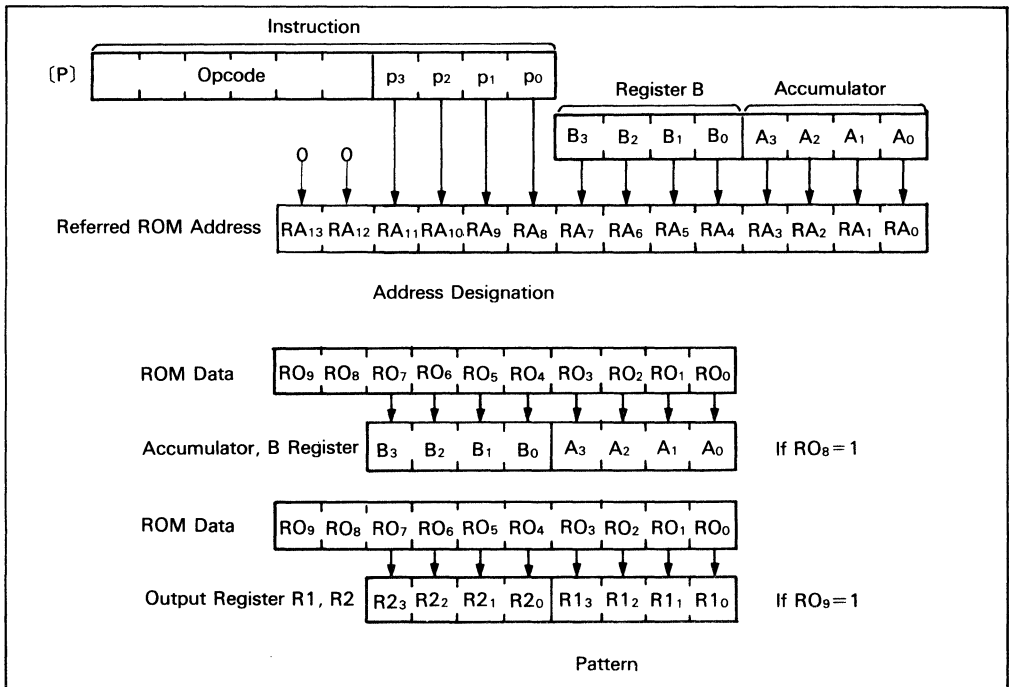


Figure 44. The Branch Destination by BR Instruction on the Boundary between Pages



Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 31-40 list their functions, and table 41 is an opcode map.

Table 31. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 32. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 33. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i_7 i_0	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i_3 i_2 i_1 i_0	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 34. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A → M, Y + 1 → Y (X → SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A → M, Y - 1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows.

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).
The op-code X is assembled as follows.

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 35. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	A + i → A	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	B + 1 → B	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	B - 1 → B	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	1 → CA		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	0 → CA		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	M + A → A	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A → A	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	M + A + CA → A OVF → CA	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M + A + CA → A OVF → CA	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	M - A - \bar{CA} → A NB → CA	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M - A - \bar{CA} → A NB → CA	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	A ∪ B → A		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	A ∩ M → A	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∩ M → A	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	A ∪ M → A	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ∪ M → A	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	A ⊕ M → A	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ⊕ M → A	NZ	2/2

Note: ∩ : Logical AND
 ∪ : Logical OR
 ⊕ : Exclusive OR



Table 36. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 37. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 38. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 39. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 40. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode/Watch Mode*	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode/Watch Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

* : Only when shifted from sub-active mode.



Table 41. Opcode Map

R8		0																1																								
		L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F								
0	H	0	NOP	XSP	XSP	XSP	AN	EM	/	/	AM	/	/	ORM	/	/	LAW	/	/	ANEM	/	/	AMD	/	/	ORMD	/	/	/	/	/	/										
	L	1	RTN	RTN	/	/	ALEM	/	/	AMC	/	/	EORM	/	/	LWA	/	/	ALEM	/	/	AMC	/	/	EORMD	/	/	/	/	/	/											
		2	INEM								i(4)				INEMD								i(4)																			
		3	ILEM								i(4)				ILEMD								i(4)																			
		4	LBM(XY)	/	BEM	/	/	/	LAB	/	/	IB	/	/	COMB	/	/	OR	/	/	STS	/	/	SBYSTOP	/	/	/	/	/	/	/											
		5	LMAY(X)	/	/	AYY	/	/	LSPY	/	/	IY	/	/	JMPL								p(4)																			
		6	NEGA	/	/	RED	/	/	LSPX	/	/	/	/	TC	CALL								p(4)																			
		7	YNEI								i(4)				BRL								p(4)																			
		8	XMA(XY)	/	/	SEM n(2)	/	/	REM n(2)	/	/	TM n(2)	/	/	XVAD	/	/	SEMD n(2)	/	/	REMD n(2)	/	/	TMD n(2)	/	/	/	/	/	/	/											
		9	LAM(XY)	/	/	LMA(XY)	/	/	SMC	/	/	ANM	/	/	LAMD	/	/	LMAD	/	/	SMCD	/	/	ANMD	/	/	/	/	/	/	/											
		A	ROTR	ROTL	/	/	DAA	/	/	DAS	/	/	LAY	LMID								i(4)																				
		B	TBR								p(4)				P								p(4)																			
		C	XMB(XY)	/	BLEM	/	/	/	LBA	/	/	/	/	DB	CAL								a(6)																			
		D	LMADY(X)	/	/	SY	/	/	LYA	/	/	/	DY																													
		E	TD	/	/	SED	/	/	LXA	/	/	REC	SEC																													
		F	LWI								i(2)																															
1		0	LBI								i(4)																															
		1	LYI								i(4)																															
		2	LXI								i(4)																															
		3	LAI								i(4)																															
		4	LBR								m(4)																															
		5	LAR								m(4)																															
		6	REDD								m(4)																															
		7	LAMR								m(4)																				BR								b(8)			
		8	AI								i(4)																															
		9	LMIIY								i(4)																															
		A	TDD								m(4)																															
		B	ALEI								i(4)																															
		C	LRB								m(4)																															
		D	LRA								m(4)																															
		E	SEDD								m(4)																															
		F	XMRA								m(4)																															

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction (2-word/2-cycle)
 2-word/2-cycle Instruction



Absolute Maximum Ratings

HD404808, HD4074808 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14.0	V	2
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Total Allowance of Input Current	ΣI_o	100	mA	3
Total Allowance of Output Current	$-\Sigma I_o$	50	mA	4
Maximum Input Current	I_o	4	mA	5, 6
		30	mA	5, 7
Maximum Output Current	$-I_o$	4	mA	8, 9
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	-25 to + 80	°C	

- Notes: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. D_{10} (V_{PP}) of the HD4074808.
3. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
4. Total allowance of output current is the sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. R0-R3
7. D0-D9
8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
9. D0-D9, R0-R3.

HD40L4808, HD407L4808 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14.0	V	2
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Total Allowance of Input Current	ΣI_O	100	mA	3
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	4
Maximum Input Current	I_O	4	mA	5, 6
		30	mA	5, 7
Maximum Output Current	$-I_O$	4	mA	8, 9
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	-25 to + 80	°C	

- Notes: 1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. D_{10} (V_{PP}) of the HD407L4808.
3. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
4. Total allowance of output current is the sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
6. RO-R3
7. D_0 - D_9
8. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
9. D_0 - D_9 , RO-R3.

Electrical Characteristics

HD404808, HD4074808 Electrical Characteristics

DC Characteristics

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, GND = $0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, SCK, INT ₀ , SI, INT ₁	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, SCK, INT ₀ , SI, INT ₁	-0.3		$0.2 V_{CC}$	V		
		OSC ₁	-0.3		0.5	V		
Output High Voltage	V_{OH}	SCK, TIMO, SO	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0mA$	
Output Low Voltage	V_{OL}	SCK, TIMO, SO			0.4	V	$I_{OL} = 1.6mA$	
Input/Output Leakage Current	$ I_{IL} $	RESET, SCK, INT ₀ , INT ₁ , SI, SO, TIMO, OSC ₁			1	μA	$V_{in} = 0V$ to V_{CC}	1
Stop Mode Hold Voltage	V_{stop}	V_{CC}	2			V	Without 32 kHz oscillator	5
Current Dissipation in Active Mode	I_{CC1}	V_{CC}		3.5	7	mA	$V_{CC} = 5V$, $f_{osc} = 4MHz$	2, 4
	I_{CC2}	V_{CC}		6	12	mA	$V_{CC} = 5V$, $f_{osc} = 4MHz$, analog input mode (D ₁₂ /D ₁₃)	4, 6
Current Dissipation in Standby Mode	I_{stby}	V_{CC}		1	2	mA	$V_{CC} = 5V$, $f_{osc} = 4MHz$	3, 4
Current Dissipation in Sub-Active Mode	I_{sub}	V_{CC}		150	300	μA	$V_{CC} = 5V$	
				75	150		LCD: ON	7
Current Dissipation in Watch Mode (1)	I_{wtc1}	V_{CC}		10	20	μA	$V_{CC} = 5V$, LCD: OFF	
Current Dissipation in Watch Mode (2)	I_{wtc2}	V_{CC}		25	50	μA	$V_{CC} = 5V$, LCD: ON	
Current Dissipation in Stop mode	I_{stop}	V_{CC}		1	10	μA	$V_{CC} = 5V$, Without 32 kHz osc	

- Notes:
- Excluding output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state
 - RESET, TEST: V_{CC}
 - D₀-D₁₃, RO—R3: V_{CC}
 - The timer operates and input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₁₃, RO—R3: V_{CC}
 - When $f_{osc} = X$ MHz, estimate the current dissipation as follows:
 Max value $f_{osc} = X$ [MHz] = $X/4 \times$ max value ($f_{osc} = 4$ [MHz])
 - RAM data retention.
 - D₁₂/D₁₃ is in the analog input mode. Input/output current does not flow. V_{Cref} , D₁₂, D₁₃: GND
 - Applies to the HD404808.



Input/Output Characteristics for Standard Pin

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, $GND = 0V$, $T_a = -20^\circ C$ to $+75^\circ C$, unless otherwise noted.)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₀ –D ₁₃ R ₀ –R ₃	$0.7 V_{CC}$		$V_{CC}+0.3$		V	
Input Low Voltage	V_{IL}	D ₀ –D ₁₃ R ₀ –R ₃	-0.3		$0.3 V_{CC}$		V	
Output High Voltage	V_{OH}	R ₀ –R ₃	$V_{CC}-1.0$			$-I_{OH} = 1.0$ mA	V	
Pull-up MOS Current	$-I_P$	R ₀ –R ₃	30	100	180	$V_{CC} = 5V$, $V_{in} = 0V$	μA	
Output Low Voltage	V_{OL}	R ₀ –R ₃			0.4	$I_{OL} = 1.6$ mA	V	
Input/Output Leakage Current	$ I_{IL} $	D ₁₁ –D ₁₃ , R ₀ –R ₃			1	$V_{in} = 0V$ to V_{CC}	μA	1
		D ₁₀			20			
Input High Voltage	V_{IHA}	D ₁₂ , D ₁₃ (Analog Compare mode)	$V_{Cref}+0.1$				V	
Input Low Voltage	V_{ILA}	D ₁₂ , D ₁₃ (Analog Compare mode)			$V_{Cref}-0.1$		V	
Analog Input Reference Voltage	V_{Cref}	V_{Cref}	0		$V_{CC}-1.2$		V	

Note: Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pin

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, $GND = 0V$, $T_a = -20^\circ C$ to $+75^\circ C$, unless otherwise noted.)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₀ –D ₉	$0.7 V_{CC}$		$V_{CC}+0.3$		V	
Input Low Voltage	V_{IL}	D ₀ –D ₉	-0.3		$0.3 V_{CC}$		V	
Output High Voltage	V_{OH}	D ₀ –D ₉	$V_{CC}-1.0$			$-I_{OH} = 1.0$ mA	V	
Pull-up MOS Current	$-I_P$	D ₀ –D ₉	30	100	180	$V_{CC} = 5V$, $V_{in} = 0V$	μA	
Output Low Voltage	V_{OL}	D ₀ –D ₉			2.0	$I_{OL} = 15$ mA $V_{CC} = 4.5$ to $6V$	V	
					0.4	$I_{OL} = 1.6$ mA	V	
Input/Output Leakage Current	$ I_{IL} $	D ₀ –D ₉			1	$V_{in} = 0V - V_{CC}$	μA	1

Note: Output buffer current is excluded.



Liquid Crystal Circuit Characteristics

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, GND = $0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment Driver Voltage Drop	V_{ds}	SEG1 to SEG32			0.6	V	$I_d = 3 \mu A$	1
Common Driver Voltage Drop	V_{dc}	COM1 to COM4			0.3	V	$I_d = 3 \mu A$	1
LCD Power Supply Dividing Resistance	R_{well}		100	300	900	$k\Omega$		
LCD Voltage	V_{LCD}	V1	4		V_{CC}	V		2

Note 1: Voltage drops from pins V_1 , V_2 , V_3 , and GND to each segment and common pin.

2. Keep the relation $V_{CC} > V_1 > V_2 > V_3 > GND$ when V_{LCD} is supplied by external power supply.

AC Characteristics

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	1.6	4.0	4.2	MHz		
		X1, X2		32.768		kHz		
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂ (without 32 kHz)	0.25	4.0	4.2	MHz		
Instruction Cycle Time	t_{cyc}		0.95	1	2.5	μs		
			0.95	1	16		without 32 kHz	
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			40	ms	Crystal	1
					20	ms	Ceramic Filter fosc=4 MHz	1
		X1, X2		3	s	$T_a = -10$ to $60^{\circ}C$	2	
External Clock Frequency	t_{CP}	OSC ₁	1.6		4.2	MHz		3
			0.25		4.2	MHz	without 32 kHz	3
External Clock High	t_{CPH}	OSC ₁	110			ns		3
External Clock Low	t_{CPL}	OSC ₁	110			ns		3
External Clock Rise Time	t_{CPr}	OSC ₁			20	ns		3
External Clock Fall Time	t_{CPf}	OSC ₁			20	ns		3
\overline{INT}_0 High Level Width	t_{0H}	\overline{INT}_0	2			t_{cyc}/t_{SUBcyc}		4, 6
\overline{INT}_0 Low Level Width	t_{0L}	\overline{INT}_0	2			t_{cyc}/t_{SUBcyc}		4, 6
\overline{INT}_1 High Level Width	t_{1H}	\overline{INT}_1	2			t_{cyc}		4
\overline{INT}_1 Low Level Width	t_{1L}	\overline{INT}_1	2			t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		5
Input Capacitance	C_{in}	D ₁₀			90	pF	f = 1 MHz, $V_{in} = 0V$	8
		All pins except D ₁₀			15	pF	f = 1 MHz, $V_{in} = 0V$	
RESET Fall Time	t_{RSTf}				20	ms		5
Analog Comparator Stabilization Time	t_{CSTB}	D ₁₂ , D ₁₃			2	t_{cyc}		7



- Notes:
1. Oscillator stabilization time is the time until the oscillator (see Figure 46) stabilizes after V_{CC} reaches 4.0V after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.
 2. Oscillator stabilization time is the time until the oscillator (see Figure 47) stabilizes after V_{CC} reaches 4.0V after power-on. Time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the crystal circuit constant and stray capacitance, please get the manufacturer's advice.
 3. See figure 48.
 4. See figure 49. The unit t_{cyc} is applied when the MCU is in the standby mode or active mode.
 5. See figure 50.
 6. See figure 49. The unit t_{SUBcyc} is applied when the MCU is in the watch mode or sub-active mode. $t_{SUBcyc} = 244.14 \mu s$ (when 32.768 kHz crystal oscillation is used.)
 7. Analog comparator stabilization time is the time until the analog comparator stabilizes and correct data can be read after entering D₁₂/D₁₃ into analog input mode.
 8. The maximum value of the HD404808 is 15pF.

Serial Interface Timing Characteristics

Transfer Clock Output

(HD404808: $V_{CC} = 4$ to $6V$, HD4074808: $V_{CC} = 4$ to $5.5V$, GND = $0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	SCK	1			t_{cyc}		1, 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK	0.5			t_{Scyc}		1, 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK			100	ns		1, 2
Serial Output Data Delay Time	t_{DSO}	SO			300	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	200			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns		1

Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t_{Scyc}	SCK	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	SCK	0.5			t_{Scyc}		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	SCK			100	ns		1
Serial Output Data Delay Time	t_{DSO}	SO			300	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	200			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	150			ns		1
Transfer Clock Completion Detect Time	t_{SCKHD}	SCK	1			t_{cyc}		1, 2, 3

- Notes: 1. See figure 51.
 2. See figure 52.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

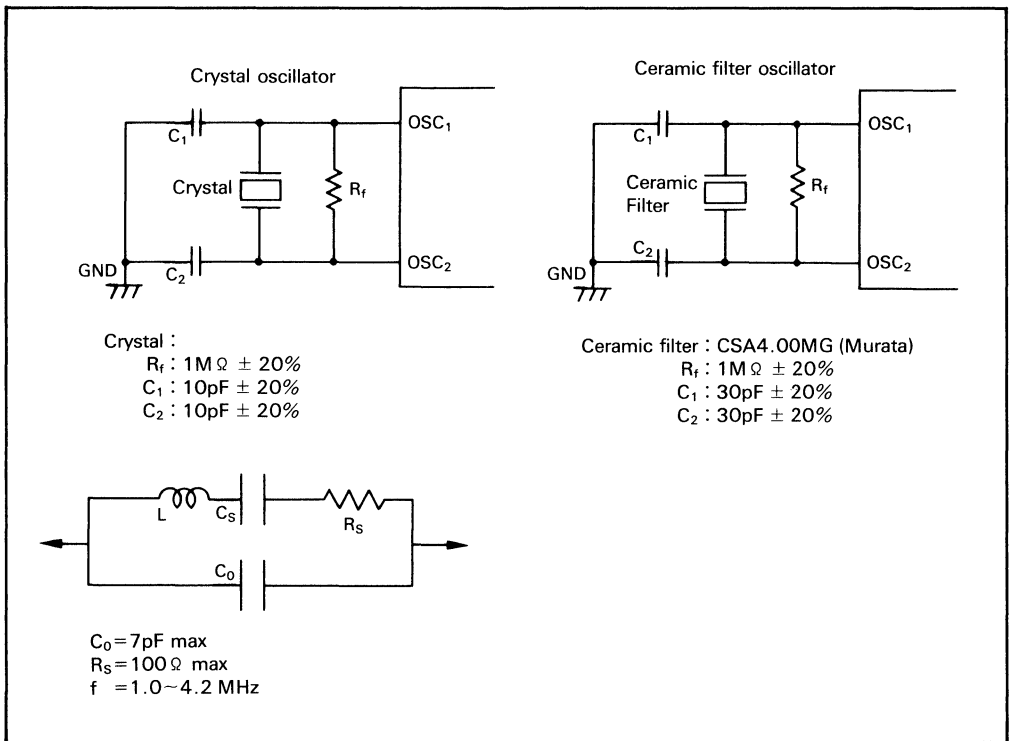


Figure 46. Oscillator Circuit

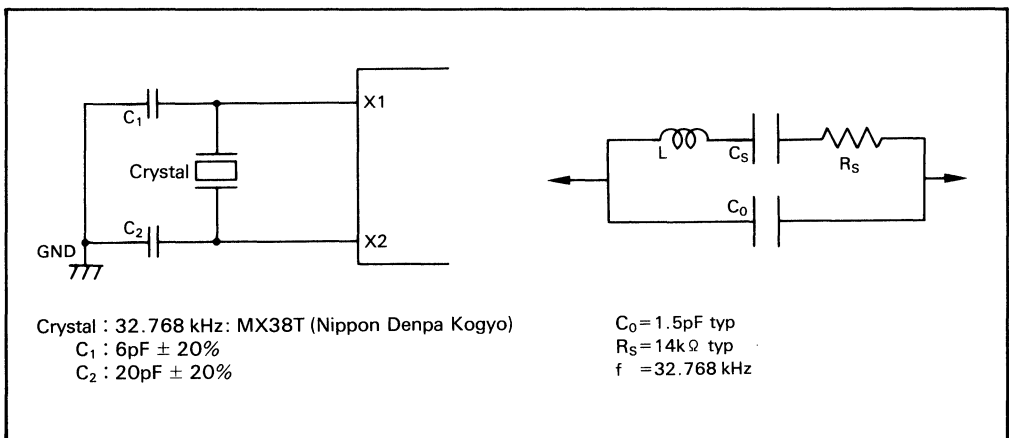


Figure 47. Oscillator Circuit

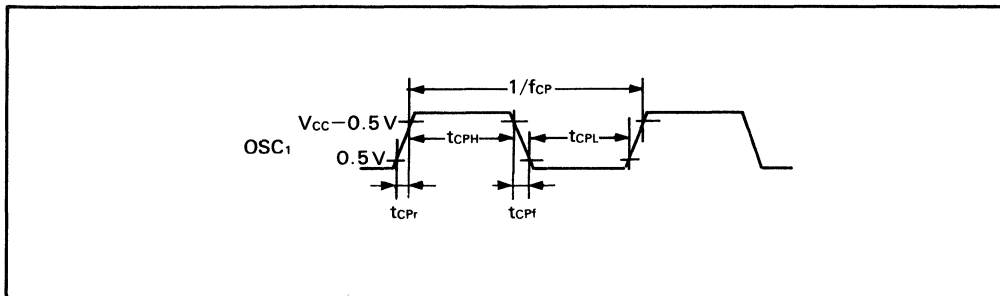


Figure 48. Oscillator Timing

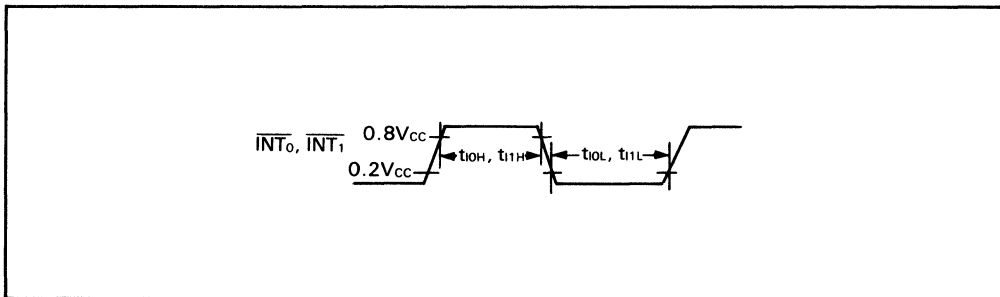


Figure 49. Interrupt Timing

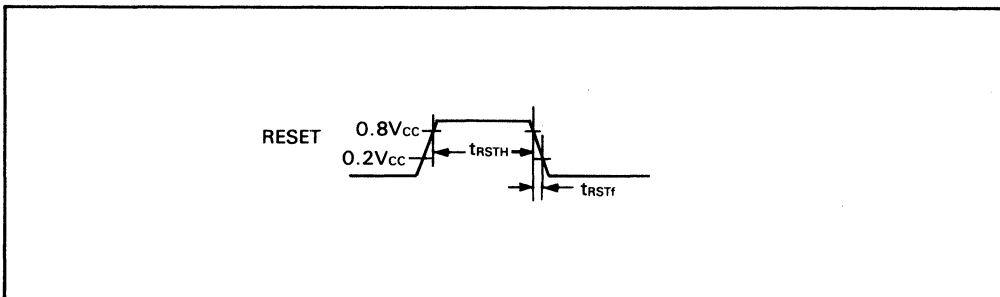


Figure 50. Reset Timing

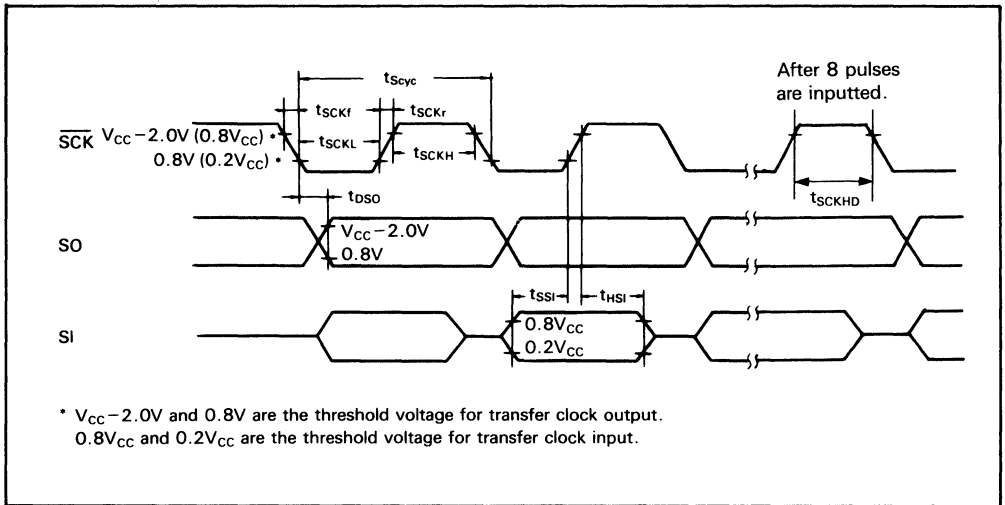


Figure 51. Timing Diagram of Serial Interface

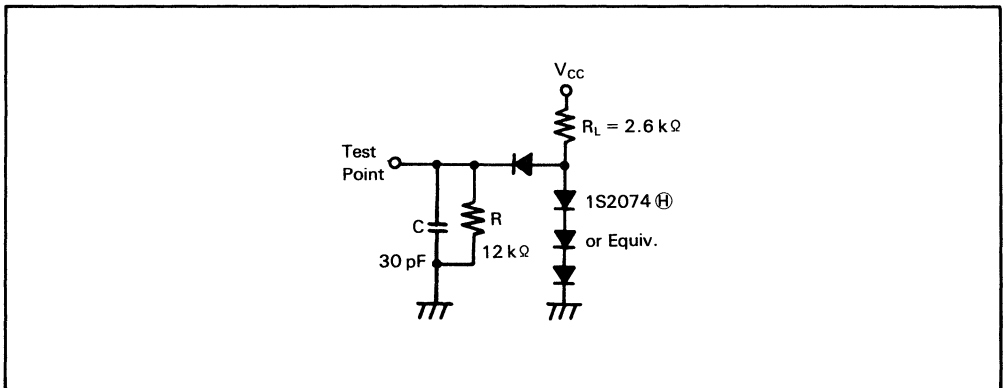


Figure 52. Timing Load Circuit

Electrical Characteristics

HD40L4808, HD407L4808 Electrical Characteristics

DC Characteristics

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, \overline{SCK} , INT ₀ , SI, INT ₁	$0.9 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.3$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, \overline{SCK} , INT ₀ , SI, INT ₁	-0.3		$0.2 V_{CC}$	V		
		OSC ₁	-0.3		0.3	V		
Output High Voltage	V_{OH}	\overline{SCK} , TIMO SO	$V_{CC} - 1.0$			V	$-I_{OH} = 0.5mA$	
Output Low Voltage	V_{OL}	\overline{SCK} , TIMO SO			0.4	V	$I_{OL} = 0.4mA$	
Input/Output Leakage Current	$ I_{IL} $	RESET, \overline{SCK} , INT ₀ , INT ₁ , SI, SO, TIMO, OSC ₁			1	μA	$V_{in} = 0V$ to V_{CC}	1
Stop Mode Hold Voltage	V_{stop}	V_{CC}	2			V	Without 32 kHz oscillator	5
Current	I_{CC1}	V_{CC}		400	1000	μA	$V_{CC} = 3V$	2, 4
Dissipation in Active Mode	I_{CC2}	V_{CC}		1	2	mA	$V_{CC} = 3V$ analog input mode (D ₁₂ /D ₁₃)	4, 6
Current Dissipation in Standby Mode	I_{stby}	V_{CC}		200	500	μA	$V_{CC} = 3V$	3, 4
Current Dissipation in Sub-Active Mode	I_{sub}	V_{CC}		50	100	μA	$V_{CC} = 3V$	
				35	70		LCD: ON	7
Current Dissipation in Watch Mode (1)	I_{wtc1}	V_{CC}		5	15	μA	$V_{CC} = 3V$ LCD: OFF	
Current Dissipation in Watch Mode (2)	I_{wtc2}	V_{CC}		15	35	μA	$V_{CC} = 3V$ LCD: ON	
Current Dissipation in Stop mode	I_{stop}	V_{CC}		1	10	μA	$V_{CC} = 3V$ Without 32 kHz osc	

- Notes:
- Excluding output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state
 - RESET, TEST: V_{CC}
 - D₀-D₁₃, R₀-R₃: V_{CC}
 - The timer operates and input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - Serial interface: Stop
 - RESET: GND
 - TEST: V_{CC}
 - D₀-D₁₃, R₀-R₃: V_{CC}
 - $f_{osc} = 400$ kHz
 - RAM data retention.
 - D₁₂/D₁₃ is in the analog input mode. Input/output current does not flow. V_{Cref} , D₁₂, D₁₃: GND
 - Applies to the HD404808.



Input/Output Characteristics for Standard Pin

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^\circ C$ to $+75^\circ C$, unless otherwise noted.)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₀ –D ₁₃ R ₀ –R ₃	$0.7 V_{CC}$		$V_{CC} + 0.3$		V	
Input Low Voltage	V_{IL}	D ₀ –D ₁₃ R ₀ –R ₃	-0.3		$0.3 V_{CC}$		V	
Output High Voltage	V_{OH}	R ₀ –R ₃	$V_{CC} - 1.0$			$-I_{OH} = 0.5\text{ mA}$	V	
Pull-up MOS Current	$-I_P$	R ₀ –R ₃	5	40	90	$V_{CC} = 3V$, $V_{in} = 0V$	μA	
Output Low Voltage	V_{OL}	R ₀ –R ₃			0.4	$I_{OL} = 0.4\text{ mA}$	V	
Input/Output Leakage Current	$ I_{IL} $	D ₁₁ –D ₁₃ , R ₀ –R ₃			1	$V_{in} = 0V$ to V_{CC}	μA	1
		D ₁₀			20			
Input High Voltage	V_{IHA}	D ₁₂ , D ₁₃ (Analog Compare mode)	$V_{Cref} + 0.1$				V	
Input Low Voltage	V_{ILA}	D ₁₂ , D ₁₃ (Analog Compare mode)			$V_{Cref} - 0.1$		V	
Analog Input Reference Voltage	V_{Cref}	V_{Cref}	0		$V_{CC} - 1.2$		V	

Note: Output buffer current is excluded.

Input/Output Characteristics for High Voltage Pin

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^\circ C$ to $+75^\circ C$, unless otherwise noted.)

Item	Symbol	Pin	min	typ	max	Test Conditions	Unit	Note
Input High Voltage	V_{IH}	D ₀ –D ₉	$0.7 V_{CC}$		$V_{CC} + 0.3$		V	
Input Low Voltage	V_{IL}	D ₀ –D ₉	-0.3		$0.3 V_{CC}$		V	
Output High Voltage	V_{OH}	D ₀ –D ₉	$V_{CC} - 1.0$			$-I_{OH} = 0.5\text{ mA}$	V	
Pull-up MOS Current	$-I_P$	D ₀ –D ₉	5	40	90	$V_{CC} = 3V$, $V_{in} = 0V$	μA	
Output Low Voltage	V_{OL}	D ₀ –D ₉			2.0	$I_{OL} = 15\text{ mA}$ $V_{CC} = 4.5$ to $6V$	V	
					0.4	$I_{OL} = 0.4\text{ mA}$	V	
Input/Output Leakage Current	$ I_{IL} $	D ₀ –D ₉			1	$V_{in} = 0V - V_{CC}$	μA	1

Note: Output buffer current is excluded.



Liquid Crystal Circuit Characteristics

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Segment Driver Voltage Drop	V_{ds}	SEG1 to SEG32			0.6	V	$I_d = 3 \mu A$	1
Common Driver Voltage Drop	V_{dc}	COM1 to COM4			0.3	V	$I_d = 3 \mu A$	1
LCD Power Supply Dividing Resistance	R_{well}		100	300	900	$k\Omega$		
LCD Voltage	V_{LCD}	V1			V_{CC}	V		2, 3

- Note 1: Voltage drops from pins V_1 , V_2 , V_3 , and GND to each segment and common pin.
 2. Keep the relation $V_{CC} > V_1 > V_2 > V_3 > GND$ when V_{LCD} is supplied by external power supply.
 3. $V_{LCD} \text{ min} = 2.7V$ (HD40L4808)
 $V_{LCD} \text{ min} = 3V$ (HD407L4808)

AC Characteristics

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.25	0.8	0.9	MHz		
		X1, X2		32.768		kHz		
Instruction Cycle Time	t_{cyc}		4.45	5	16	μs		
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			30	ms	$f_{osc} = 400$ kHz	1
					30	ms	$f_{osc} = 800$ kHz	1
		X1, X2			3	s	$T_a = -10$ to $60^{\circ}C$	2
External clock Frequency	f_{CP}	OSC ₁	0.25		0.9	MHz		
External Clock High	t_{CPH}	OSC ₁	525			ns		3
External Clock Low	t_{CPL}	OSC ₁	525			ns		3
External Clock Rise Time	t_{CPr}	OSC ₁			30	ns		3
External Clock Fall Time	t_{CPf}	OSC ₁			30	ns		3
\overline{INT}_0 High Level Width	t_{iOH}	\overline{INT}_0	2			t_{cyc}/t_{SUBcyc}		4, 6
\overline{INT}_0 Low Level Width	t_{iOL}	\overline{INT}_0	2			t_{cyc}/t_{SUBcyc}		4, 6
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		4
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		4
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		5
Input Capacitance	C_{in}	D ₁₀			90	pF	$f = 1$ MHz, $V_{in} = 0V$	8
		All pins except D ₁₀			15	pF	$f = 1$ MHz, $V_{in} = 0V$	
RESET Fall Time	t_{RSTf}				20	ms		5
Analog Comparator Stabilization Time	t_{CSTB}	D ₁₂ , D ₁₃			2	t_{cyc}		7

- Notes:
1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD407L4808: V_{CC} is 3.0 V) after power-on, or after RESET goes high. At power-on or STOP mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit.
 2. Oscillation stabilization time is the time until the oscillator stabilizes after V_{CC} reaches 2.7 V (HD407L4808: V_{CC} is 3.0 V) after power-on. Time required to stabilize the oscillator (t_{RC}) must be obtained. Since t_{RC} depends on the crystal circuit constant and stray capacitance, please get the manufacturer's advice.
 3. See figure 53.
 4. See figure 54. The unit t_{cyc} is applied when the MCU is in the standby mode or active mode.
 5. See figure 55.
 6. See figure 54. The unit t_{SUBcyc} is applied when the MCU is in the watch mode or sub-active mode. $t_{SUBcyc} = 244.14 \mu s$ (when 32.768 kHz crystal oscillation is used.)
 7. Analog comparator stabilization time is the time until the analog comparator stabilizes and correct data can be read after entering D_{12}/D_{13} into analog input mode.
 8. The maximum value of the HD40L4808 is 15pF.

Serial Interface Timing Characteristics

Transfer Clock Output

(HD40L4808: $V_{CC} = 2.7$ to $6V$, HD407L4808: $V_{CC} = 3$ to $5.5V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$, unless otherwise noted.)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK}	1			t_{cyc}		1, 2
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	\overline{SCK}	0.5			$t_{S_{cyc}}$		1, 2
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	\overline{SCK}			200	ns		1, 2
Serial Output Data Delay Time	t_{DSO}	SO			500	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	300			ns		1

Transfer Clock Input

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	$t_{S_{cyc}}$	\overline{SCK}	1			t_{cyc}		1
Transfer Clock High, Low Level Width	t_{SCKH} t_{SCKL}	\overline{SCK}	0.5			$t_{S_{cyc}}$		1
Transfer Clock Rise, Fall Time	t_{SCKr} t_{SCKf}	\overline{SCK}			200	ns		1
Serial Output Data Delay Time	t_{DSO}	SO			500	ns		1, 2
Serial Input Data Set-up Time	t_{SSI}	SI	300			ns		1
Serial Input Data Hold Time	t_{HSI}	SI	300			ns		1
Transfer Clock Completion Detect Time	t_{SCKHD}	SCK	1			t_{cyc}		1, 2, 3

- Notes: 1. See figure 56.
 2. See figure 57.
 3. Transfer clock completion detect time is the period of high level after 8 pulses of transfer clock are inputted. SCI interrupt request flag is not set when the next transfer clock is input before transfer clock completion detect time has passed.

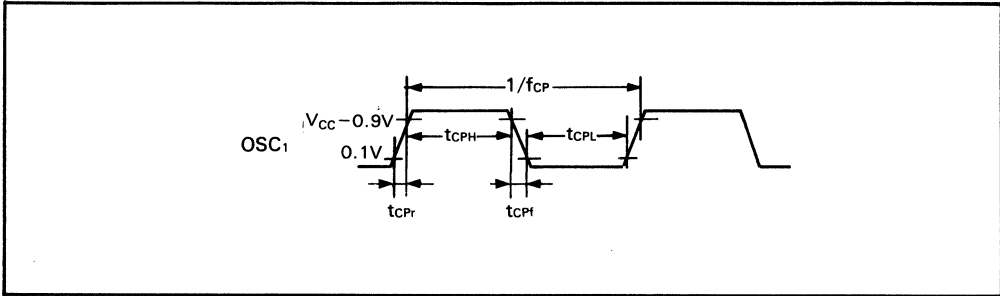


Figure 53. Oscillator Timing

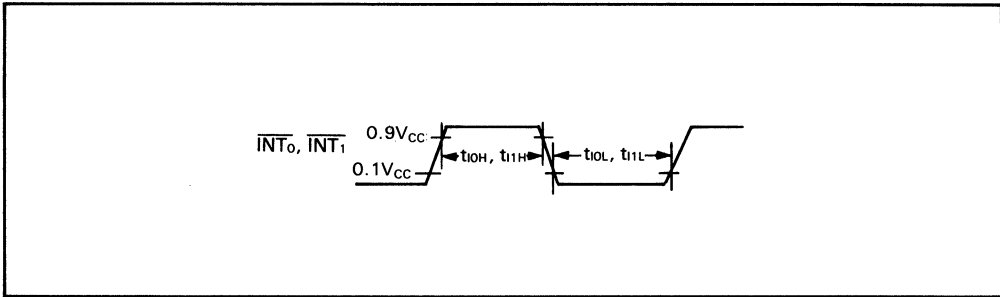


Figure 54. Interrupt Timing

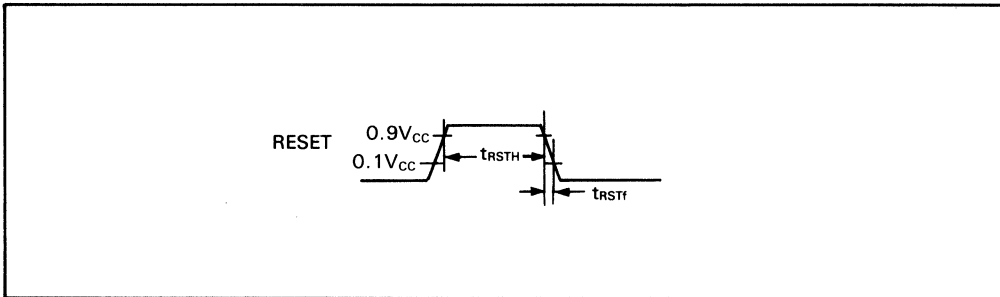


Figure 55. Reset Timing

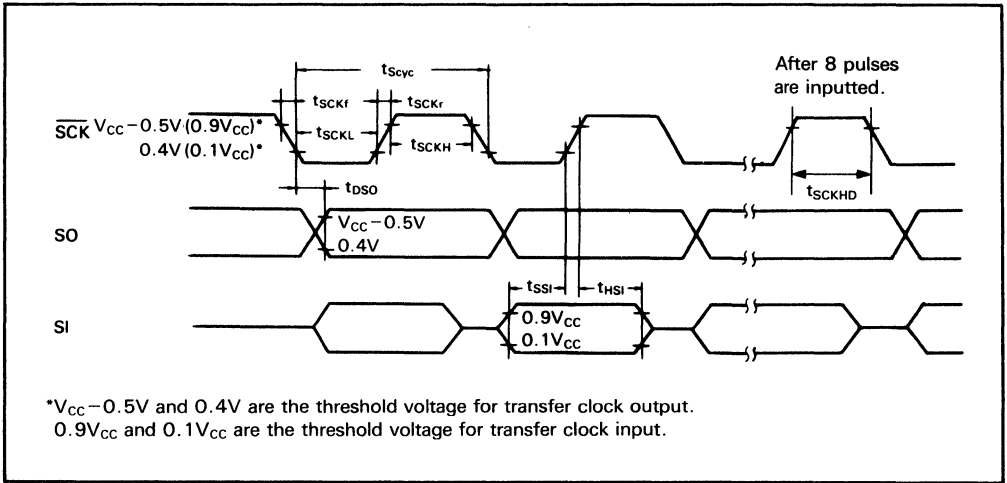


Figure 56. Timing Diagram of Serial Interface

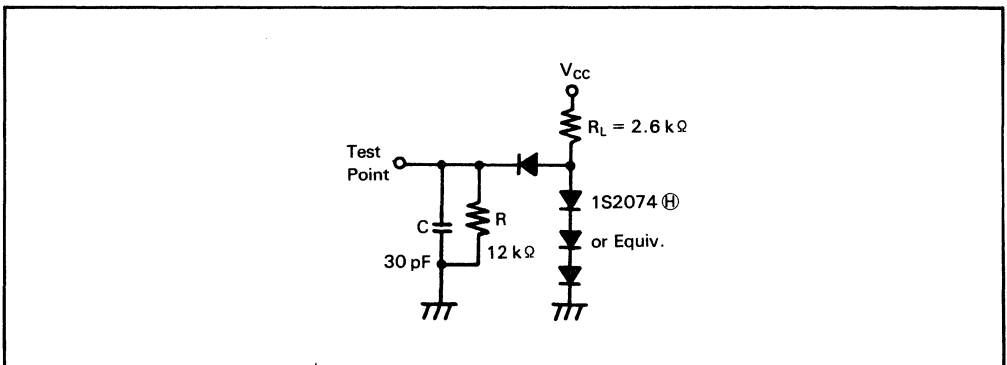


Figure 57. Timing Load Circuit

HD404808/HD4074808/HD40L4808/HD407L4808

HD404808
Option List

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number	
Hitachi's Entry	HD404808

NOTE: Please enter check marks in (■, ×, √).

(1) Functional Option

<input type="checkbox"/> With 32 kHz CPU Operation and with a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and with a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and without a Watch Time Base

(2) Package

<input type="checkbox"/> FP-80A
<input type="checkbox"/> FP-80B

(3) ROM Code Media

ROM Code Media
<input checked="" type="checkbox"/> EPROM On-Package Microcomputer Type

(4) Oscillator

HD404808			
Main	<input type="checkbox"/>	Crystal Oscillator	(f = MHz)
	<input type="checkbox"/>	Ceramic Filter Oscillator	(f = MHz)
	<input type="checkbox"/>	External Clock	(f = MHz)
Sub	<input type="checkbox"/>	32.768 kHz Crystal Oscillator	
	<input type="checkbox"/>	Not Used	



HD40L4808 Option List

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number	
Hitachi's Entry	HD40L4808

NOTE: Please enter check marks in (■, ×, √).

(1) Functional Option

<input type="checkbox"/> With 32 kHz CPU Operation and with a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and with a Watch Time Base
<input type="checkbox"/> Without 32 kHz CPU Operation and without a Watch Time Base

(2) Package

<input type="checkbox"/> FP-80A
<input type="checkbox"/> FP-80B

(3) ROM Code Media

ROM Code Media
<input checked="" type="checkbox"/> EPROM On-Package Microcomputer Type

(4) Oscillator

HD40L4808	
Main	<input type="checkbox"/> Ceramic Filter Oscillator (f= kHz) <input type="checkbox"/> External Clock (f= kHz)
Sub	<input type="checkbox"/> 32.768 kHz Crystal Oscillator <input type="checkbox"/> Not Used



HD404918

Description

The HD404918 CMOS 4-bit single-chip microcomputer in the HMCS400 series incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins.

Features

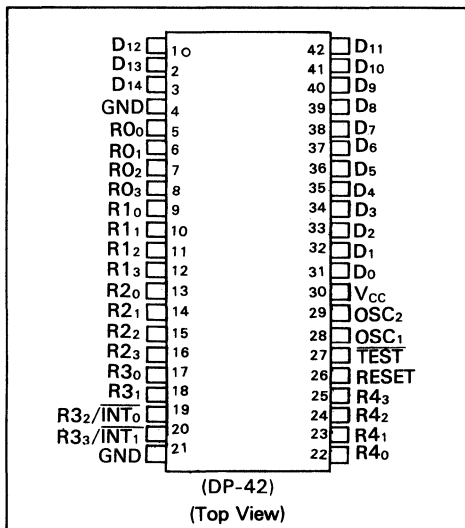
- 4-bit architecture
- 8192 words of 10-bit ROM
- 512 digits of 4-bit RAM
- 35 I/O pins, including 27 high-voltage I/O pins (12 V max)
- Timer/counter
 - 11-bit prescaler
 - 8-bit auto-reload timer/event counter (timer B)
- Three interrupt sources
 - External: 2
 - Timer/counter: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time: 1.78 μ s
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Crystal or ceramic filter
 - External Clock input
- Standard 42-pin dual in-line plastic package
- Instruction set compatible with HMCS412; 100 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation/table lookup capability
- Bit manipulation for both RAM and I/O

Program Development Support Tools

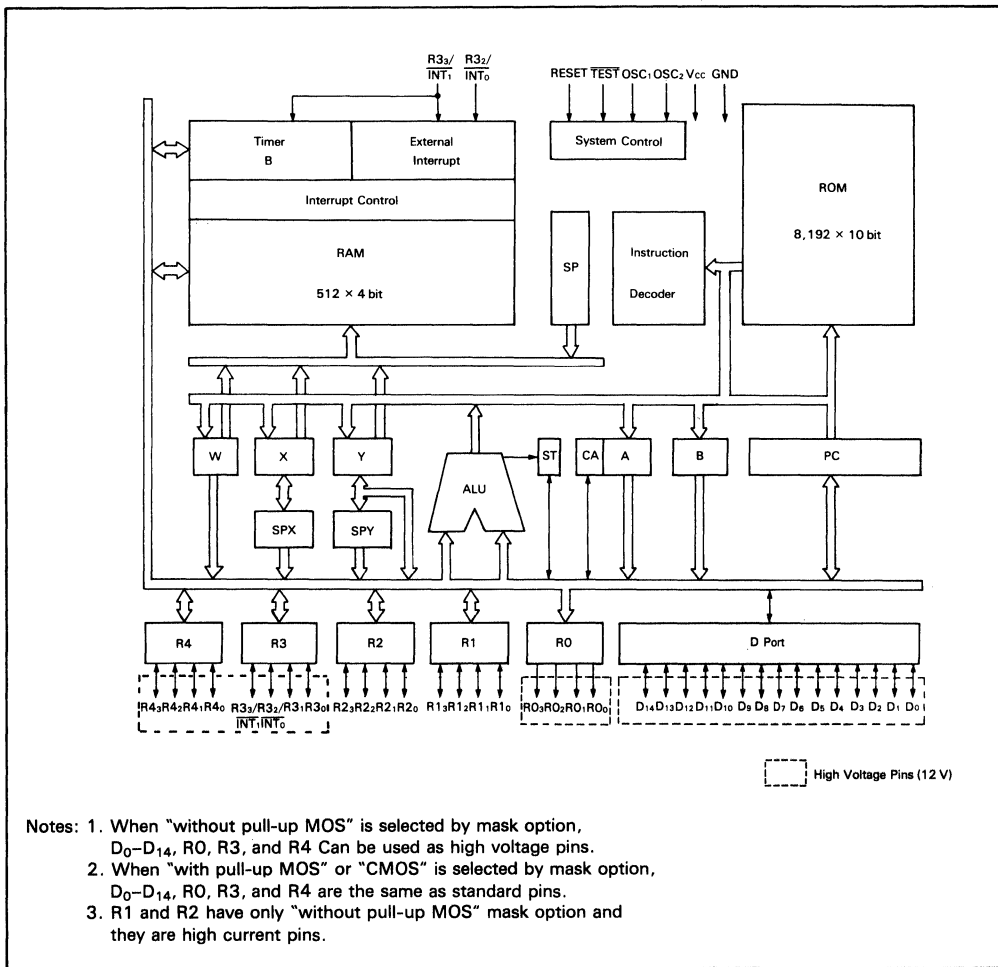
- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD40P4919 with the following fixed options:
 - I/O pin: NMOS open drain
 - Oscillator: ceramic filter oscillator (externally drivable)
 - Timing generator divider: Divide by 8
 - Package: standard 42-pin dual in-line ceramic package

Note: Support tools are under development.

Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC} (Power Supply)

GND and V_{CC} are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin.

$\overline{\text{TEST}}$ (Test)

$\overline{\text{TEST}}$ is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D₀ to D₁₄ are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁–R₁₃, R₂–R₂₃, R₃–R₃₃, R₄–R₄₃ (R Ports)

R₀ to R₄ are 4-bit I/O ports. R₀ is an output port, and R₁ to R₄ are I/O ports. R₀, R₃, and R₄ are high-voltage ports, and R₁ and R₂ are high current ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, R₃₃ of port R₃ are multiplexed with $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ respectively. For details, see Input/Output section.

$\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$ (Interrupts)

$\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ are external interrupts for the MCU. $\overline{\text{INT}}_1$ can be used as an external event input pin for timer B. $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 8192 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After a reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$1FFF): Locations from \$0000 to \$1FFF can be used for program code.

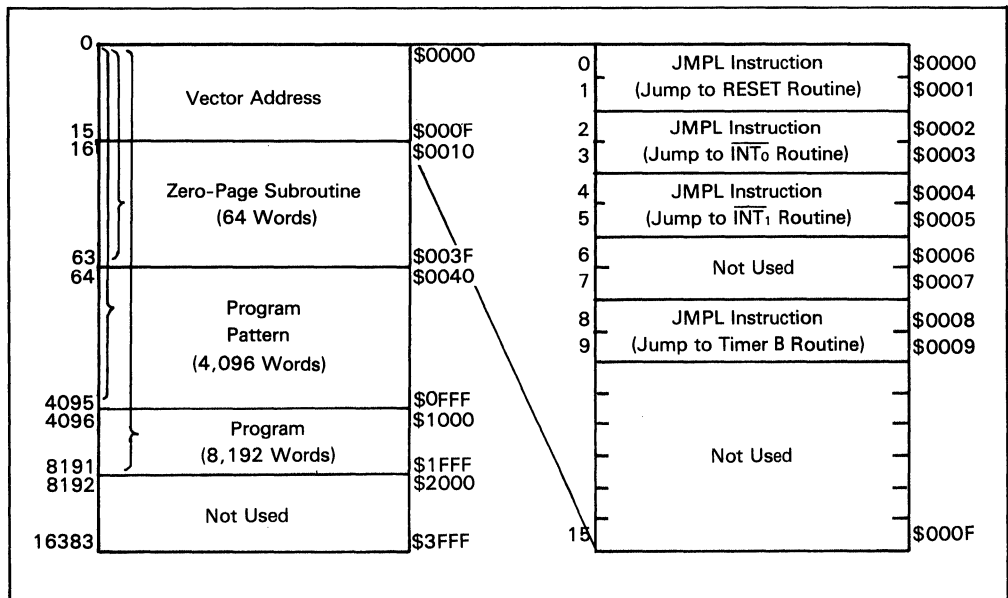


Figure 1. ROM Memory Map

RAM Memory Map

The MCU includes 512 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003):

The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction.

However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B):

The special function registers are the mode or data registers for the external interrupt, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

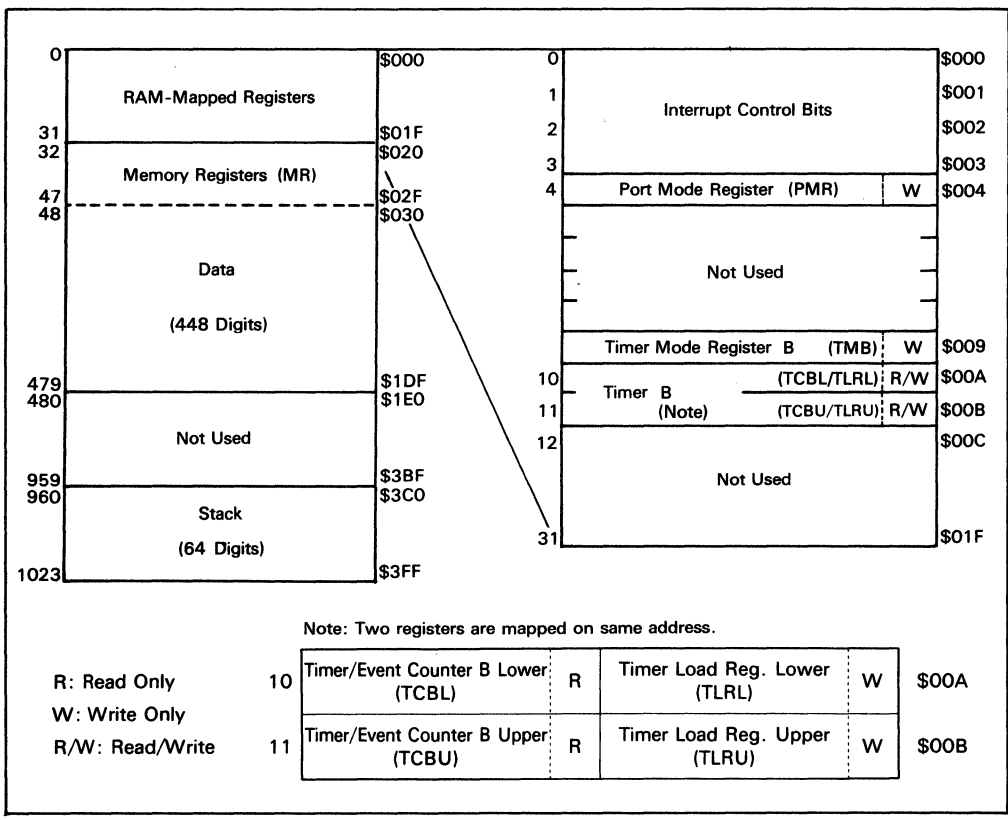


Figure 2. RAM Memory Map

Data Area (\$020 to \$1DF): 16 digits, \$020 through \$02F, in the data area are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine calls (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

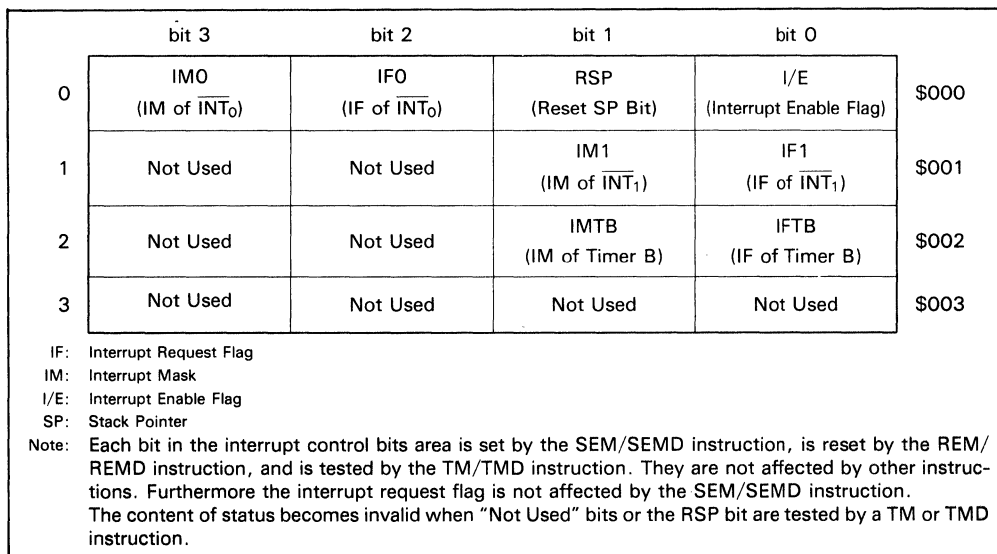


Figure 3. Interrupt Control Bit Area Configuration

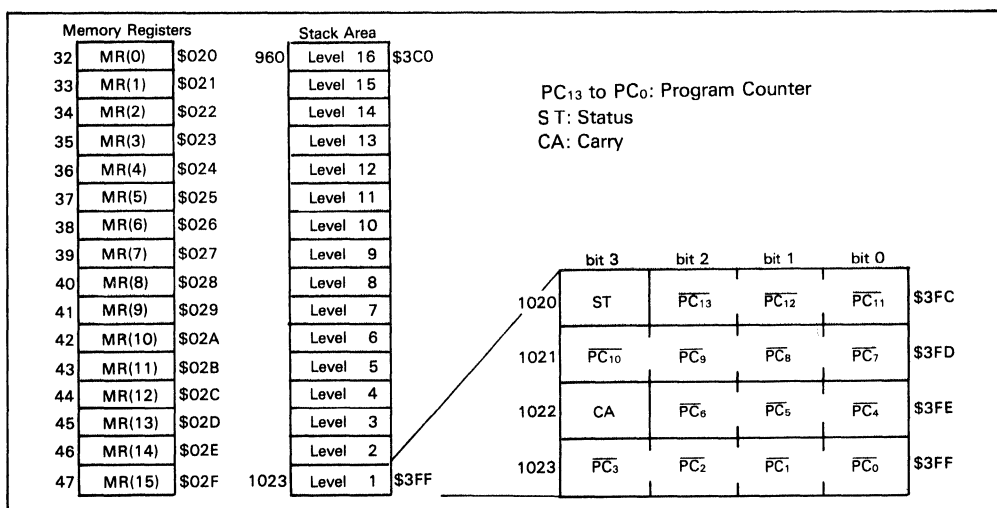


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU has nine registers and two flags for CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit

test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

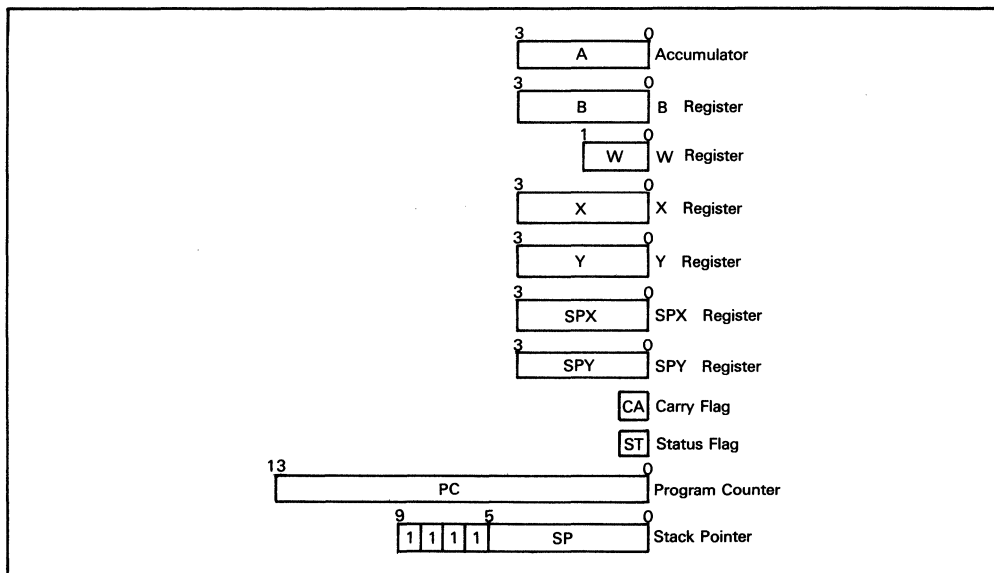


Figure 5. Registers and Flags



Interrupt

Three interrupt sources are available on the MCU: external requests ($\overline{INT_0}$, $\overline{INT_1}$), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are

mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	—	\$0000
$\overline{INT_0}$	1	\$0002
$\overline{INT_1}$	2	\$0004
Timer B	3	\$0008

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	Timer B
I/E	1	1	1
$IF_0 \cdot \overline{IM_0}$	1	0	0
$IF_1 \cdot \overline{IM_1}$	*	1	0
$IFTB \cdot \overline{IMTB}$	*	*	1

Notes: Don't care

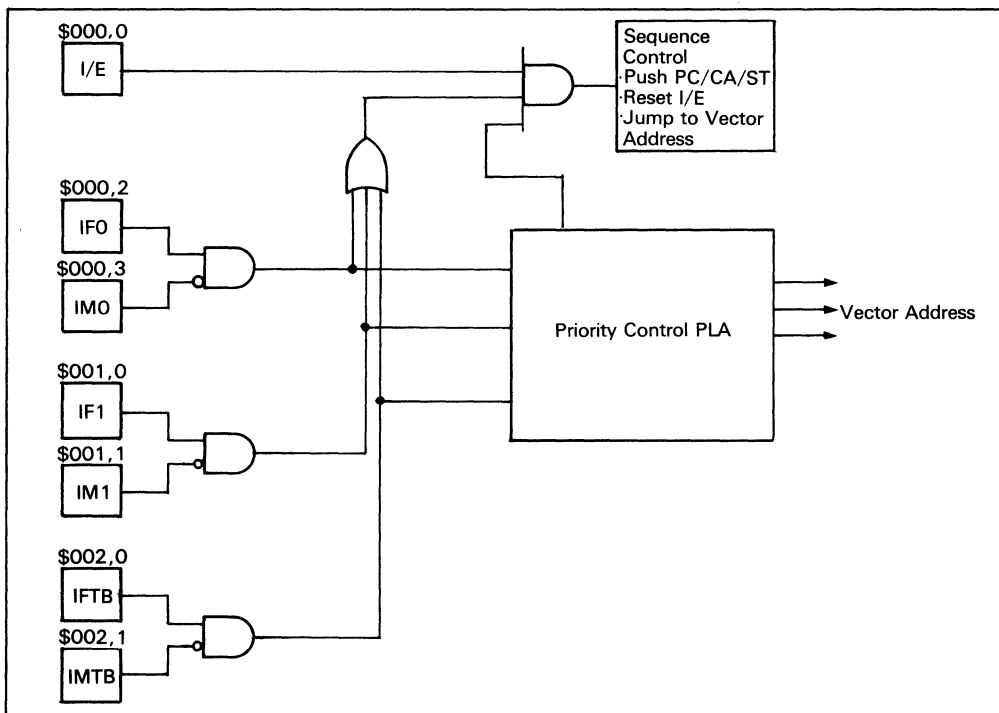


Figure 6. Interrupt Control Circuit Block Diagram

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after the MCU jumps to the vector address.

In each vector address, program a JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register

(PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When \overline{INT}_1 is used as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (\overline{IF}_0 , \overline{IF}_1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, and $R3_3/\overline{INT}_1$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

Ex Int Req Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin

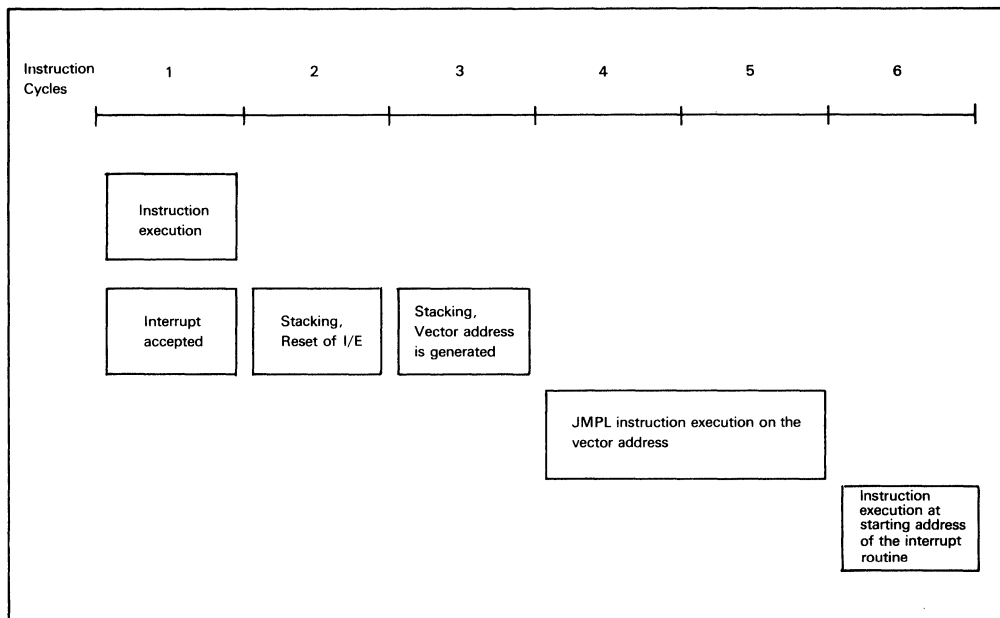


Figure 7. Interrupt Servicing Sequence

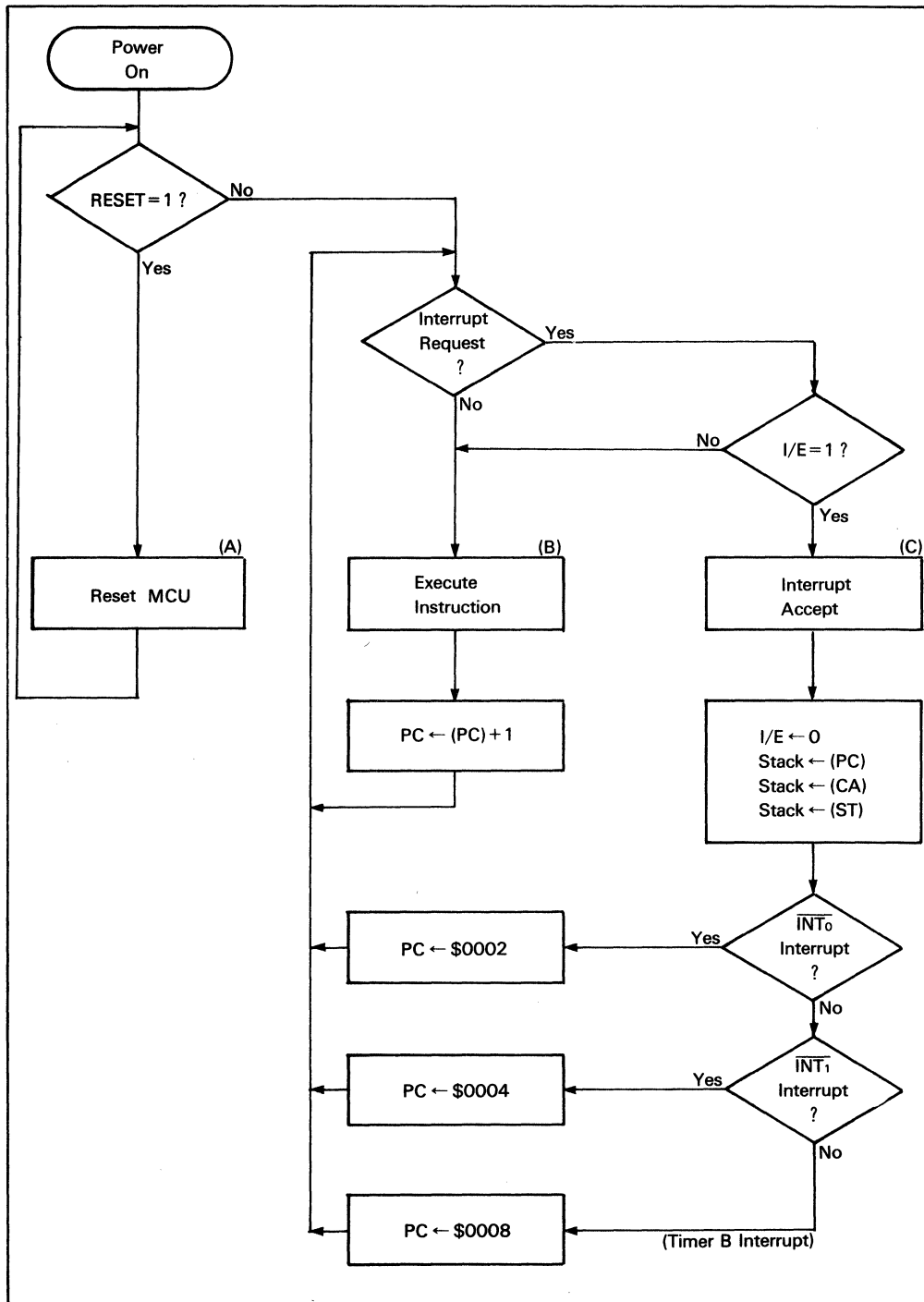


Figure 8. Interrupt Servicing Flowchart



Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/ event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

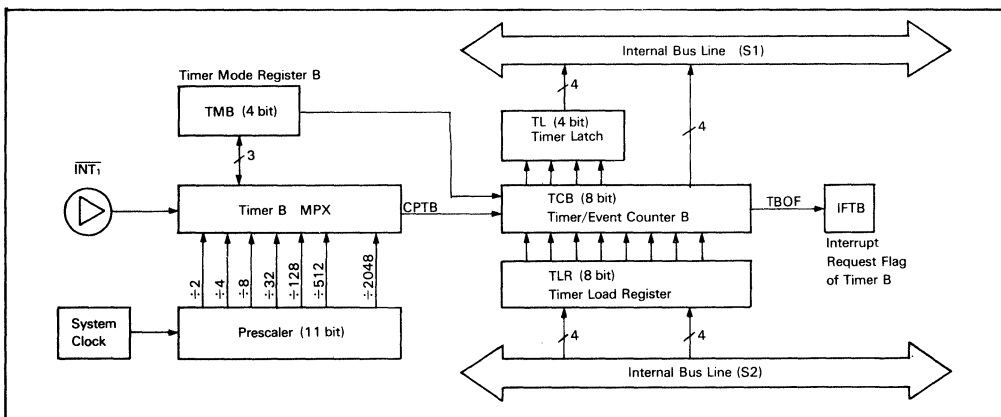


Figure 9. Timer Block Diagram



Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3	Auto-reload Function		
0	No		
1	Yes		

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	\overline{INT}_1 (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

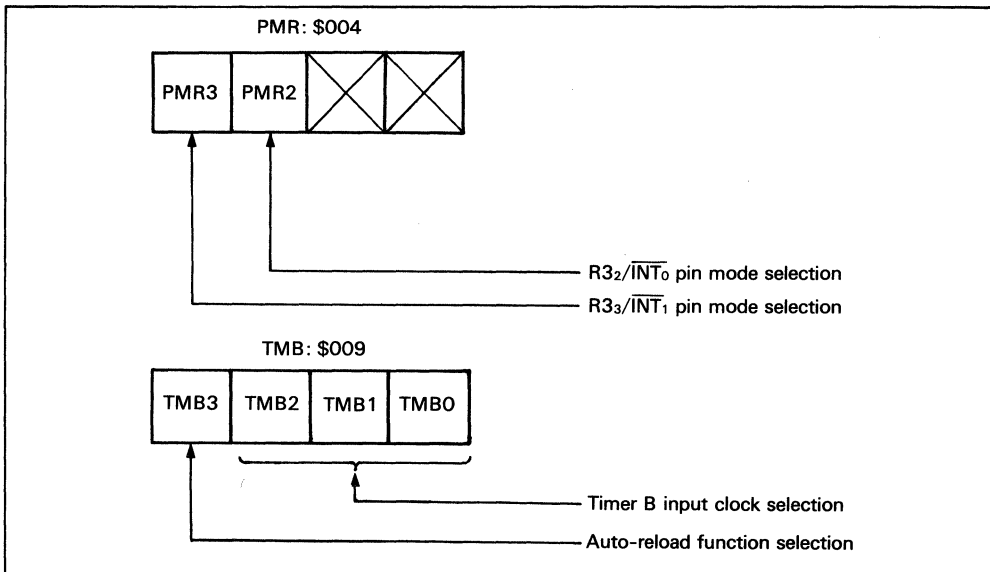


Figure 10. Mode Register Configuration and Function

Input/Output

The MCU has 35 I/O pins, 8 standard and 27 high voltage. One of three circuit types can be selected by mask option for each high-voltage pin: (A) "without pull-up MOS (NMOS open drain)", (B) "with pull-up MOS", or (C) "CMOS". High-voltage pins can be used as high-voltage I/O pins only when (A) is selected, but except R1 and R2. R1 and R2 are fixed to (A) mask option.

When any input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 11.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 11 shortens the rise time of the output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{\text{HLT}}$ signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 for the I/O pin circuit types.

R Ports: The six R ports are composed of 16 I/O pins, 4 output-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU is not be affected when the input-only and/or non-existing ports are written into, while invalid data will be read from the output-only and/or non-existing ports.

The R3₂ and R3₃ pins are multiplexed with the $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ pins respectively. See table 10 for the selectable circuit types for these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage: select "without pull-up MOS" (NMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard: select "without pull-up MOS" (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when stop mode, is called the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 12 shows the parts initialized by MCU reset, and the status of each.

Table 10. I/O Pin Circuit Types

	Without Pull-Up MOS (NMOS Open Drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable Pins
I/O Common Pins				D ₀ –D ₁₄ R ₃₀ –R ₃₃ R ₄₀ –R ₄₃
High Current	Not available	Not available	Not available	
High Voltage	Available	Not available	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	Applicable pins
I/O Common Pins		R ₁₀ –R ₁₃ R ₂₀ –R ₂₃
High Current	Available	
High Voltage	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
Output Pins				R ₀₀ –R ₀₃
High Current	Not available	Not available	Not available	
High Voltage	Available	Not available	Not available	

- Notes: 1. When "without pull-up MOS" is selected by mask option, D₀–D₁₄, R₀, R₃, and R₄ can be used as high voltage pins.
 2. When "with pull-up MOS" or "CMOS" is selected by mask option, D₀–D₁₄, R₀, R₃, and R₄ are the same as standard pins.
 3. R₁ and R₂ have only "without pull-up MOS" mask option and they are high current pins.



Table 11. Data Input from Input/Output Common Pins

I/O Pin Circuit Type	Input Possible	Input Pin State
CMOS	No	—
Without pull-up MOS (NMOS open drain)	Yes	1
With pull-up MOS	Yes	1

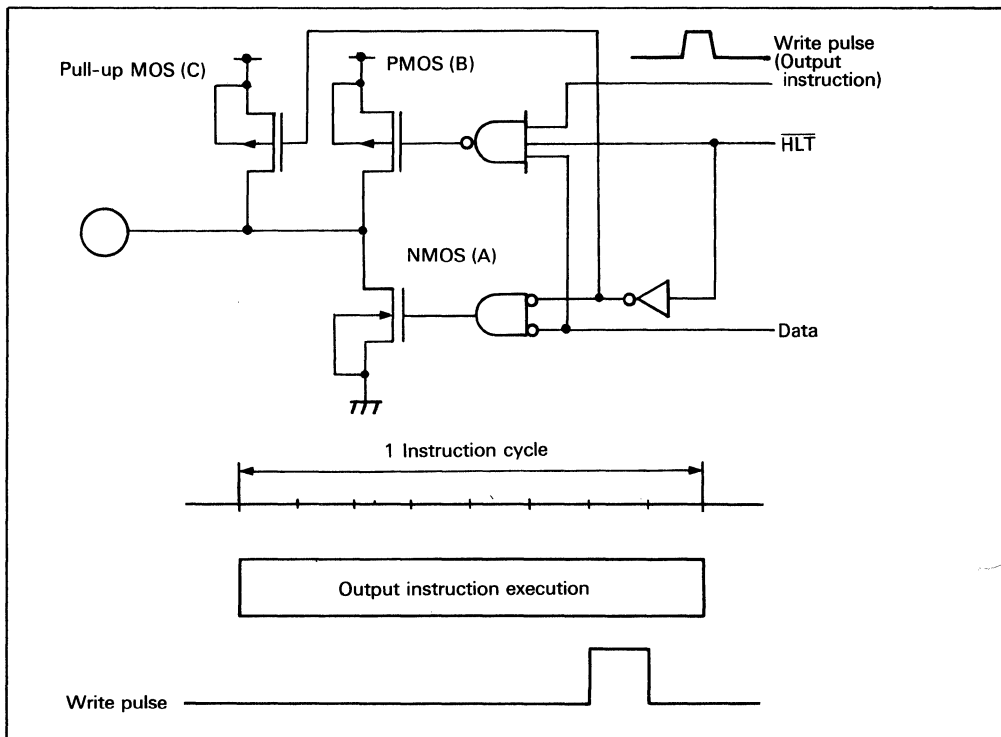


Figure 11. Output Circuit Operation of Pins With Pull-Up MOS Option

Table 12. Initial Value After MCU Reset

Items	Initial Value by MCU Reset	Contents
Program Counter (PC)	\$0000	Execute program from the top of ROM address
Status (ST)	1	Enable branch with conditional branch instructions
Stack Pointer (SP)	\$3FF	Stack level is 0
I/O Pin Output Register	(A) Without Pull-Up MOS	1 Enable input
	(B) With Pull-Up MOS	1 Enable input
	(C) CMOS	1 —
Interrupt Flag	Interrupt Enable Flag (I/E)	0 Inhibit all interrupts
	Interrupt Request Flag (IF)	0 No interrupt request
	Interrupt Mask (IM)	1 Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000 See port mode register
	Timer Mode Register B (TMB)	0000 See timer mode register B
Timer/Counter	Prescaler	\$000 —
	Timer/Event Counter B (TCB)	\$00 —
	Timer Load Register (TLR)	\$00 —

Note: MCU reset affects the rest of registers as follows:

Item	After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop-Mode)
Carry (CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator (A)		
B Register (B)		
W Register (W)		
X/SPX Registers (X/SPX)		
Y/SPY Registers (Y/SPY)	The contents of RAM before MCU reset (just before STOP instruction) are retained.	
RAM		

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. In addition, see figure 13 for the layout of

the crystal or ceramic filter. In all cases, external clock operation is available.

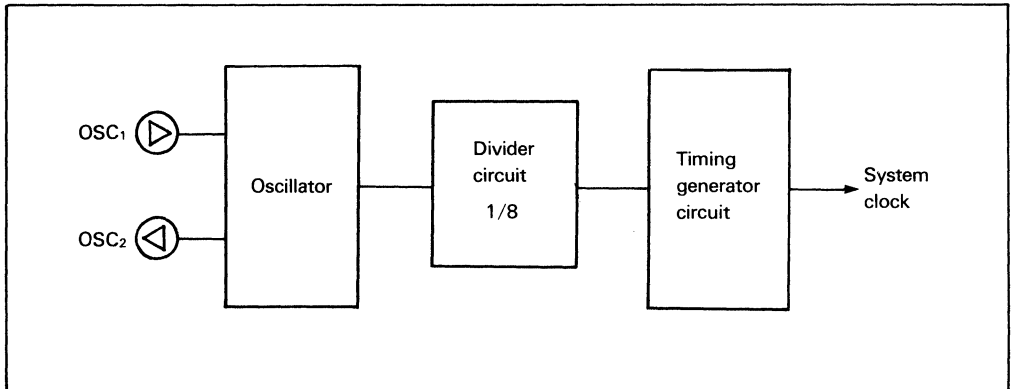


Figure 12. Internal Oscillator Circuit

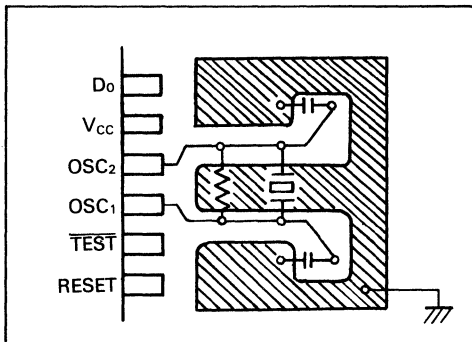
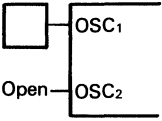
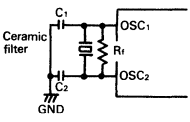
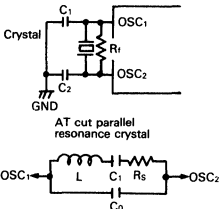


Figure 13. Layout of Crystal and Ceramic Filter

Table 13. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
<p>External Clock Operation</p>	<p>Oscillator</p> 	
<p>Ceramic Filter Oscillator</p>		<p>Ceramic filter CSA 4.00MG (Murata)</p> <p>$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$</p>
<p>Crystal Oscillator</p>	 <p>AT cut parallel resonance crystal</p>	<p>$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 10\text{-}22\text{ pF} \pm 20\%$ $C_2: 10\text{-}22\text{ pF} \pm 20\%$ Crystal: equivalent to circuit shown</p> <p>$C_0: 7\text{ pF max.}$ $R_s: 100\ \Omega\text{ max.}$ $f: 1.0\text{-}4.5\text{ MHz}$</p>

Notes: 1. For the crystal and ceramic filter resonator, the upper circuit parameters are recommended by the crystal or ceramic filter maker. Crystal, ceramic filter resonator, and the floating capacitance change circuit parameters in designing the board. In designing the resonator, please consult with the engineers of the crystal or ceramic filter maker to determine the circuit parameters.

2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross other wires. Refer to the layout of crystal and ceramic filter (figure 13).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 14). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 14. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, flag	Retained	Reset (note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (note 2)	High impedance
Timer/counter	Active	Stopped
Recovery method	RESET input, interrupt request	RESET input

- Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 12 for the contents of flags and registers.
 2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

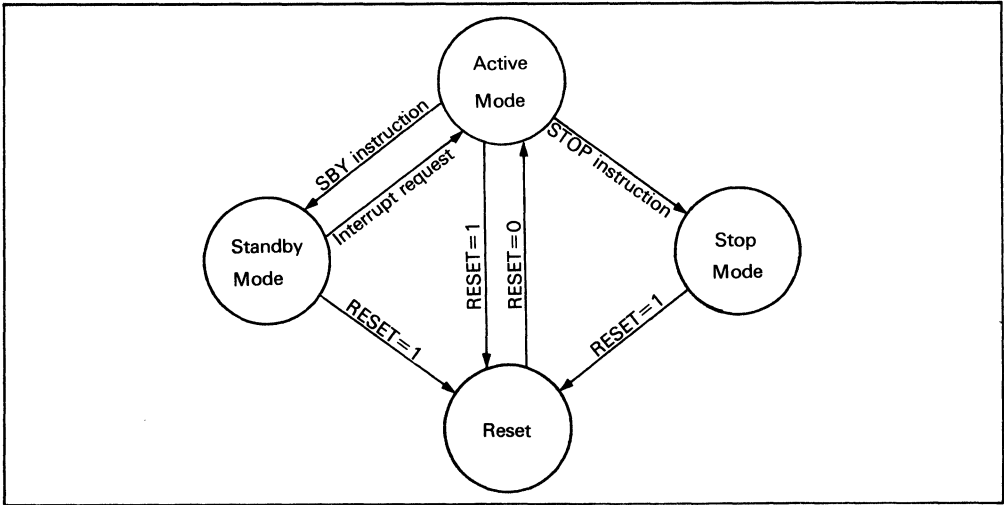


Figure 14. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 15 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

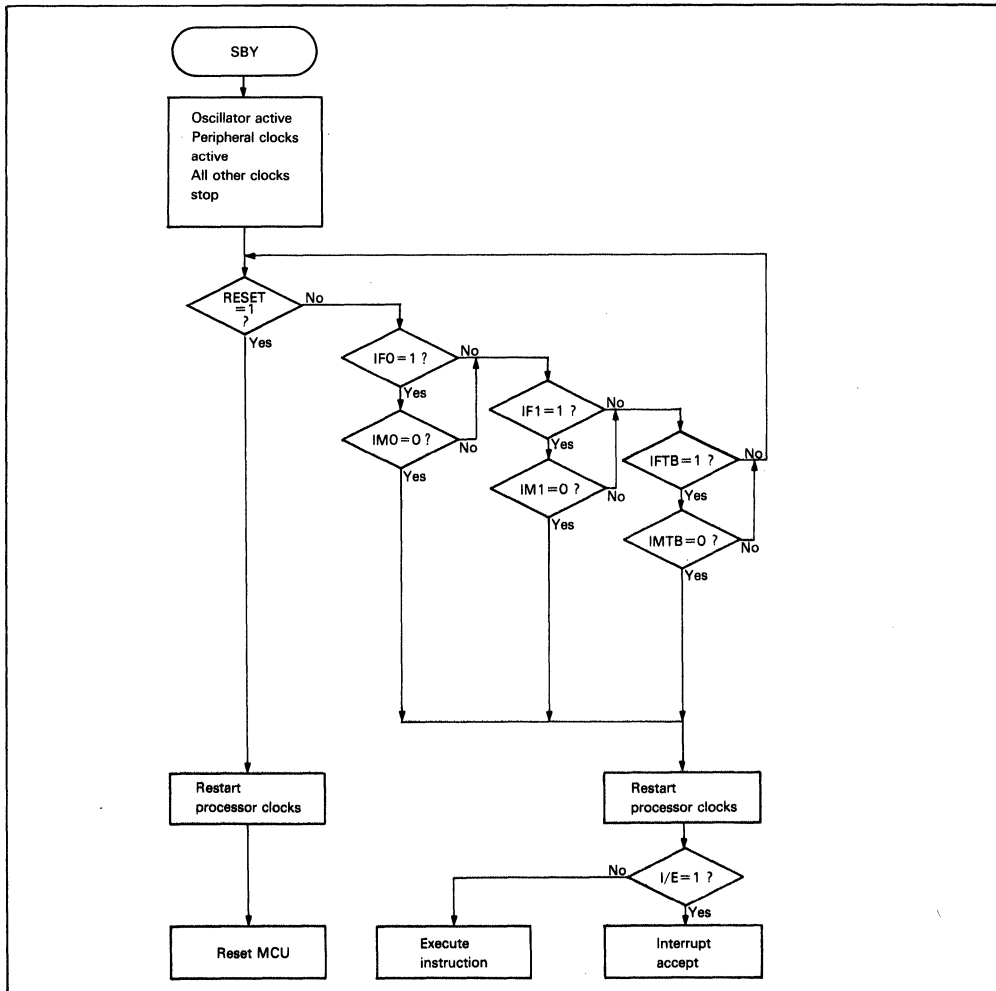


Figure 15. MCU Standby Mode Operation Flowchart

RAM Addressing Mode

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 18.

Direct addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 19), executing a BR instruction transfers the PC contents to the next page because of the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 20). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

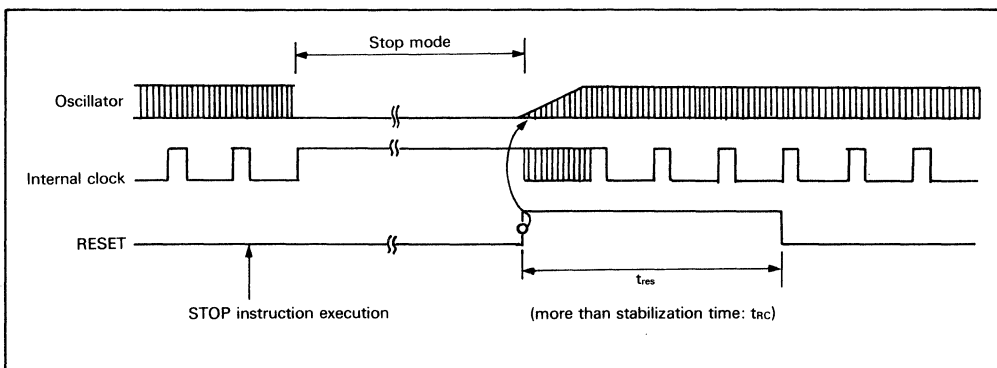


Figure 16. Timing Chart of Recovering from Stop Mode

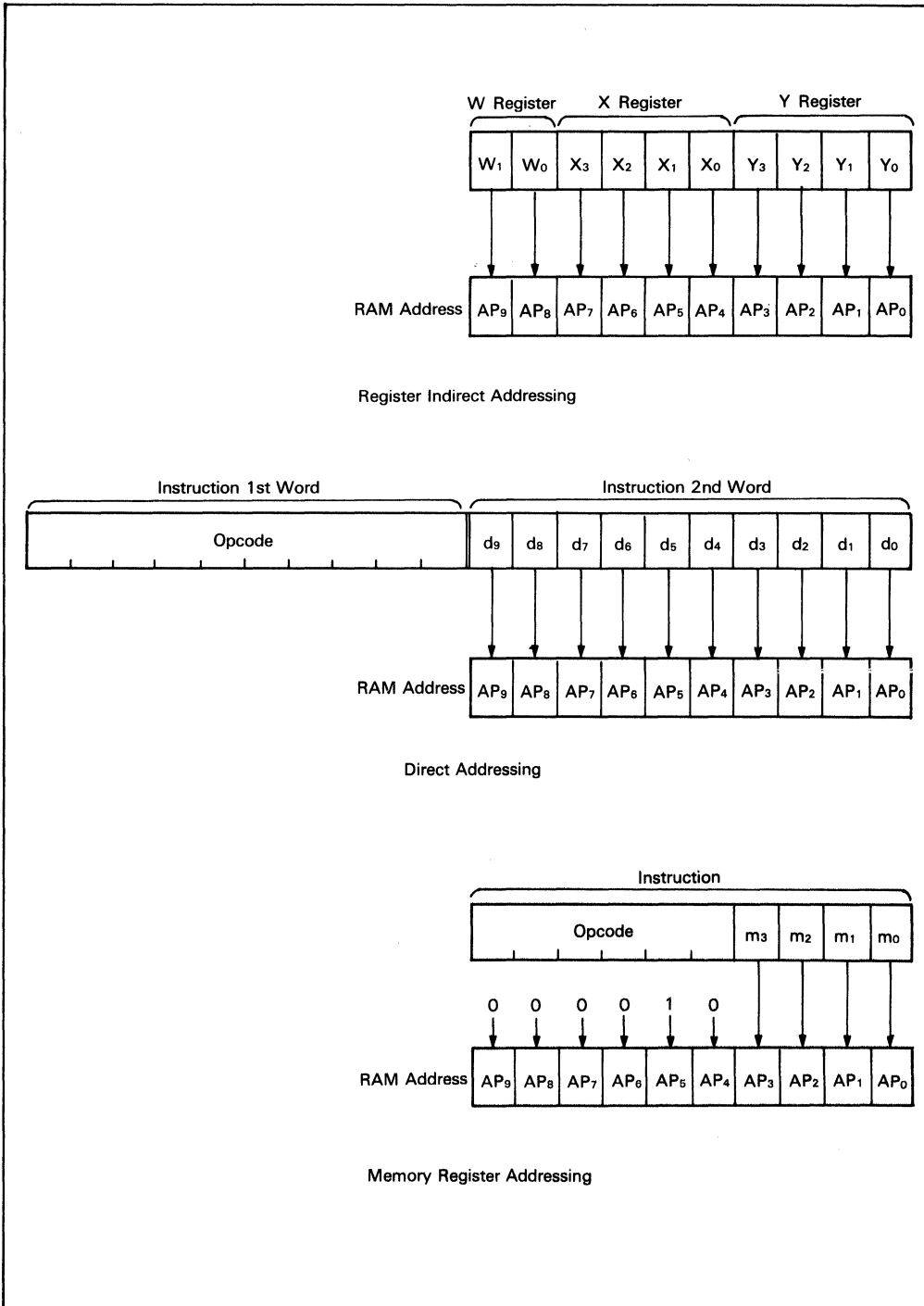


Figure 17. RAM Addressing Mode



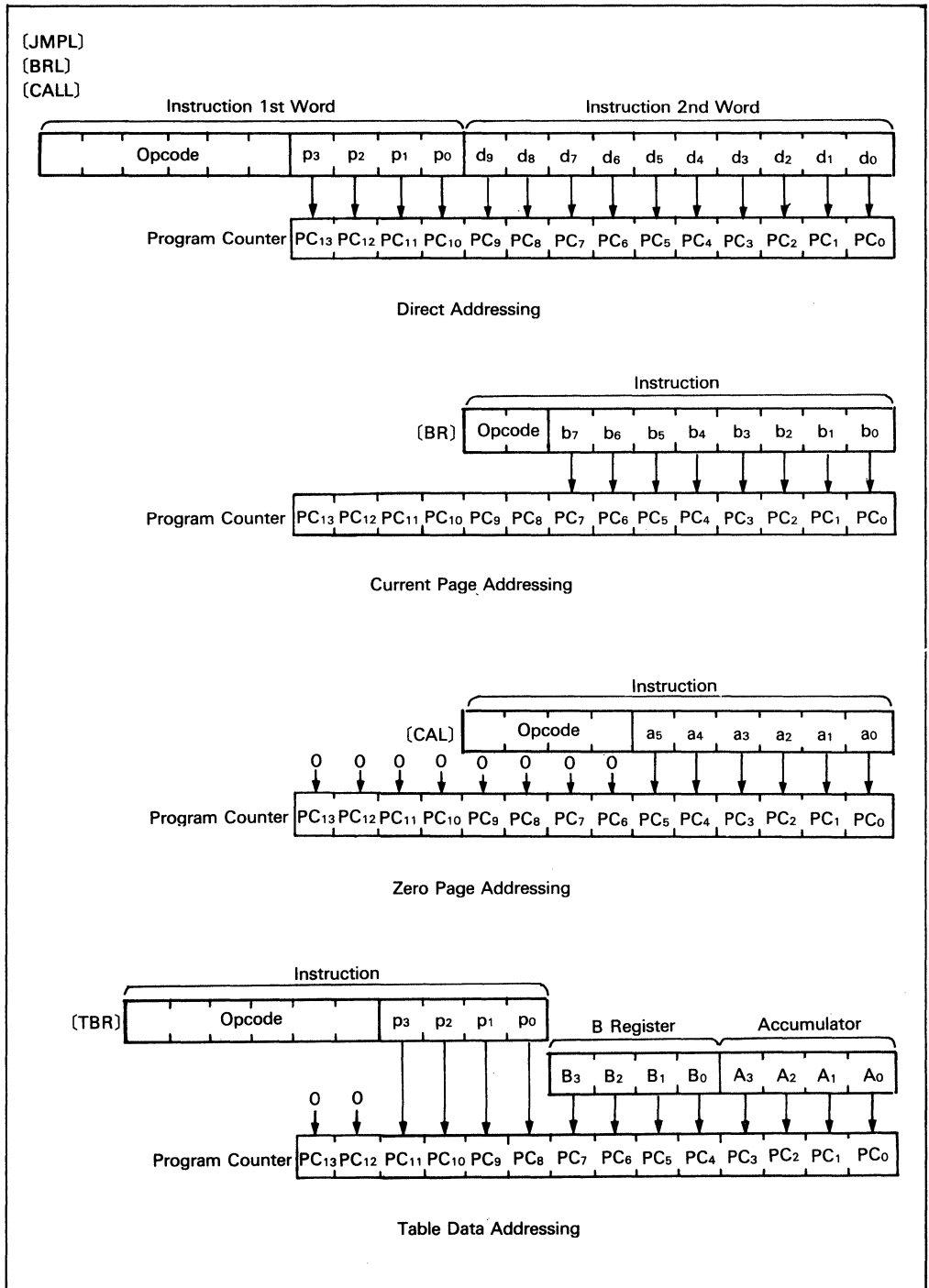


Figure 18. ROM Addressing Mode



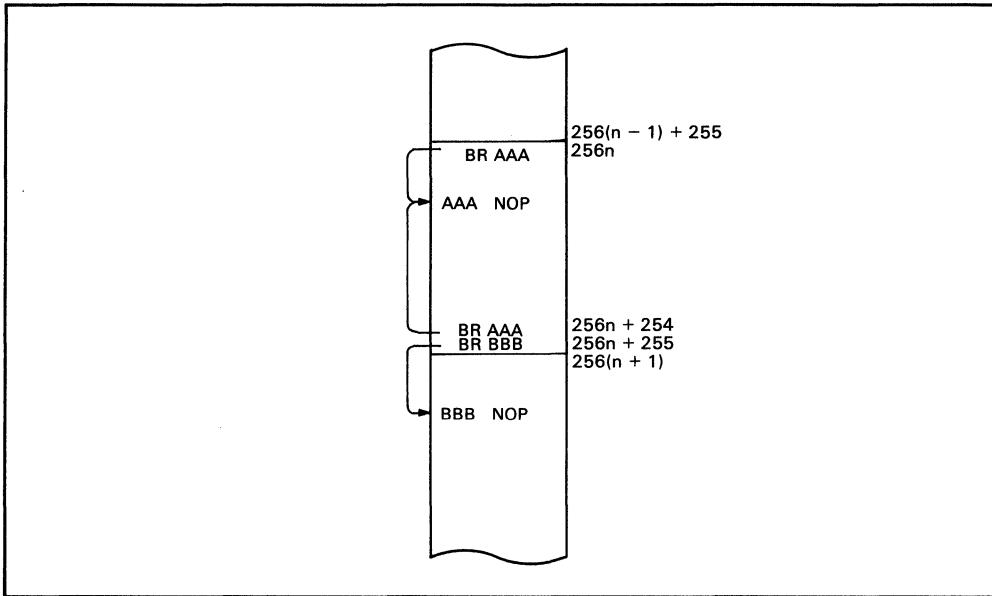


Figure 19. BR Instruction Branch Destination on Page Boundary

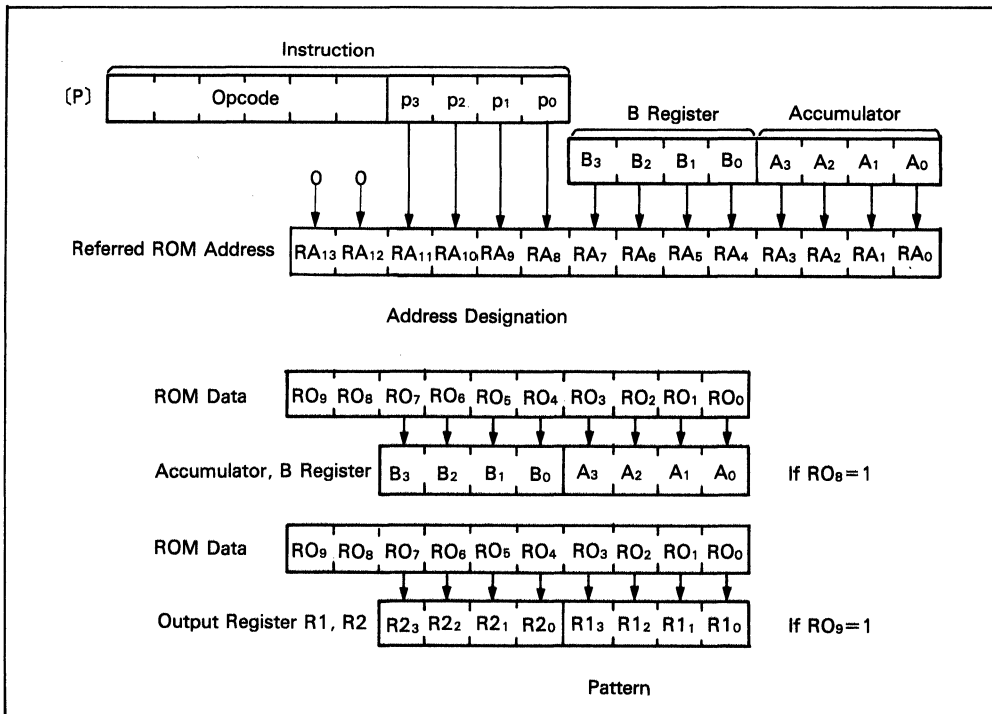


Figure 20. P Instruction

Instruction Set

The HD404918 provides 100 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 15-24 list their functions, and table 25 is an opcode map.

Table 15. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 16. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note :An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 17. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYY	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 18. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M↔A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M↔B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes each (example of LMAIY (X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 19. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

Table 20. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 21. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2



HD404918

Table 22. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 23. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 24. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: HD404918 has no serial interface, so STS (start serial) operates the same as NOP.



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		-0.3 to + 15	V	4
Total Allowance of Input Current	ΣI_O	200	mA	5
Maximum Input Current	I_O	15	mA	7, 8
		35	mA	7, 10
Maximum Output Current	$-I_O$	4	mA	8, 9
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	6
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	

- Notes: 1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_{14}$, $R_3 - R_4$, R_0
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $R_1 - R_2$.

Electrical Characteristics

DC Characteristics

($V_{CC} = 4\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, INT ₀ , INT ₁	0.8 V_{CC}		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET, INT ₀ , INT ₁	- 0.3		0.2 V_{CC}	V		
		OSC ₁	- 0.3		0.5	V		
Input/Output Leakage Current	$ I_{IL} $	RESET, INT ₀ , INT ₁ , OSC ₁			1	μA	$V_{in} = 0\text{ V to }V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			2.5	mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}, \div 8$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}			1.0	mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}, \div 8$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}			10	μA	$V_{in}(\overline{\text{TEST}}) = V_{CC} - 0.3\text{ V to }0\text{ V};$ $V_{CC}; V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes: 1. Excluding pull-up MOS current and output buffer current.
 2. The MCU is in the reset state. Input/output current does not flow.
 • MCU in reset state, operation mode
 • RESET, TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 • MCU in standby mode
 • Input/output in reset state
 • RESET: GND
 • TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 4. Excluding pull-up MOS current.
 5. When $f_{osc} = x\text{ MHz}$, estimate the current dissipation as follows:
 Max value @ $x\text{ MHz} = x/4 \times (\text{max value @ }4\text{ MHz})$

Input/Output Characteristics for Standard Use

($V_{CC}=4V$ to $6V$, $GND=0V$, $T_a=-20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	R1-R2	$0.7V_{CC}$		$V_{CC} + 0.3$	V		3
		D0-D14 R3-R4						4
Input Low Voltage	V_{IL}	R1-R2	-0.3		$0.3V_{CC}$	V		3
		D0-D14 R3-R4						4
Output High voltage	V_{OH}	D0-D14 R3-R4, R0	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0$ mA	1
		D0-D14, R3-R4, R0	$V_{CC} - 0.5$			V	$-I_{OH} = 0.5$ mA	1
Output Low Voltage	V_{OL}	D0-D14, R3-R4, R0			0.4	V	$I_{OL} = 1.6$ mA	
		R1-R2			1.0	V	$V_{CC} = 5$ V, $I_{OL} = 25$ mA	3
Input/Output Leakage Current	$ I_{II} $	D0-D14, R3-R4, R0			1	μA	$V_{in} = 0$ V to V_{CC}	2
		R1-R2			20			
Pull-Up MOS Current	$-I_p$	D0-D14, R3-R4, R0	30	60	150	μA	$V_{CC} = 5$ V, $V_{in} = 0$ V	4

- Notes: 1. Applied to I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins without pull-up MOS mask option.
 4. With pull up MOS is selected by mask option.

Input/Output Characteristics for High Voltage Use

($V_{CC} = 4$ V to 6 V, $GND = 0$ V, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D0-D14, R3-R4	$0.7V_{CC}$		12	V		1
Input Low Voltage	V_{IL}	D0-D14, R3-R4	-0.3		$0.3V_{CC}$	V		1
Output High Voltage	V_{OH}	D0-D14, R3-R4, R0	11.5			V	500 k Ω to 12V	1
Output Low Voltage	V_{OL}	D0-D14, R3-R4, R0			0.4	V	$I_{OL} = 1.6$ mA	1
Input/Output Leakage Current	$ I_{II} $	D0-D14, R3-R4, R0			1	μA	$V_{in} = 0$ V to V_{CC}	1

- Notes: 1. Applied to I/O pins without pull-up MOS by mask option.



AC Characteristics(V_{CC} = 4 V to 6 V, GND = 0 V, T_a = -20°C to + 75°C)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f _{osc}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz	Divide by 8	
Instruction Cycle Time	t _{cyc}		1.78	2	20	μs		
Oscillator Stabilization Time	t _{RC}	OSC ₁ , OSC ₂			20	ms		1
External clock Frequency	f _{cp}	OSC ₁	0.4		4.5	MHz		2
External Clock High, Low Level Width	t _{CPH} , t _{CPL}	OSC ₁	92			ns	Divide by 8	2
External Clock Rise Time	t _{CPr}	OSC ₁			20	ns		2
External Clock Fall Time	t _{CPf}	OSC ₁			20	ns		2
Instruction cycle Time	t _{cyc}		1.78		20	μs		2
$\overline{\text{INT}}_0$ High Level Width	t _{t0H}	$\overline{\text{INT}}_0$	2			t _{cyc}		3
$\overline{\text{INT}}_0$ Low Level Width	t _{t0L}	$\overline{\text{INT}}_0$	2			t _{cyc}		3
$\overline{\text{INT}}_1$ High Level Width	t _{t1H}	$\overline{\text{INT}}_1$	2			t _{cyc}		3
$\overline{\text{INT}}_1$ Low Level Width	t _{t1L}	$\overline{\text{INT}}_1$	2			t _{cyc}		3
RESET High Level Width	t _{RSTH}	RESET	2			t _{cyc}		4
Input Capacitance	C _{in}	All pins			15	pF	f = 1 MHz, V _{in} = 0 V	
RESET Fall Time	t _{RSTf}				20	ms		4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage 4 V after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC}. Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 21.)

2. See figure 22.
3. See figure 23.
4. See figure 24.

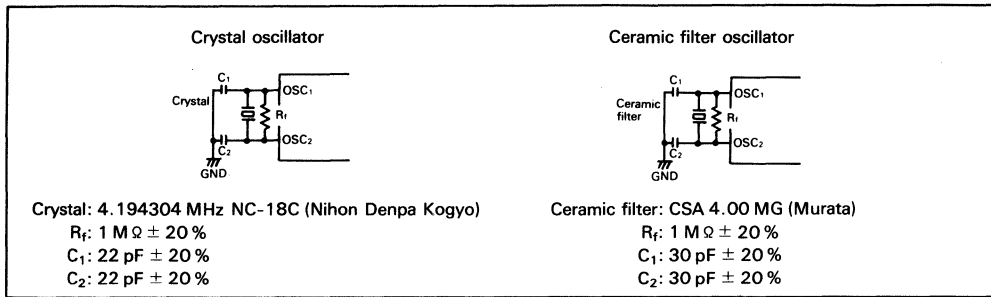


Figure 21. Oscillator Circuit

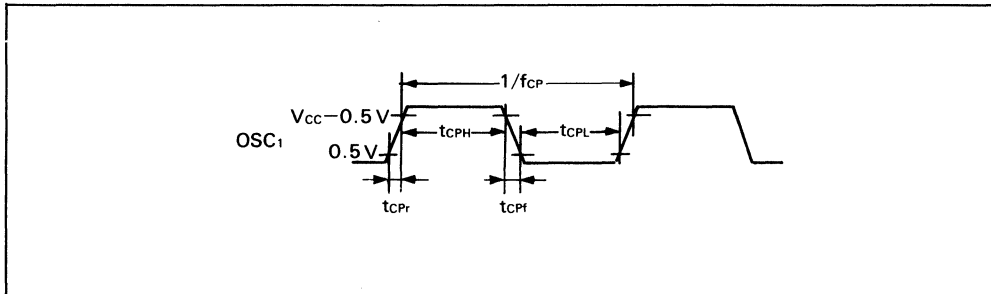


Figure 22. Oscillator Timing

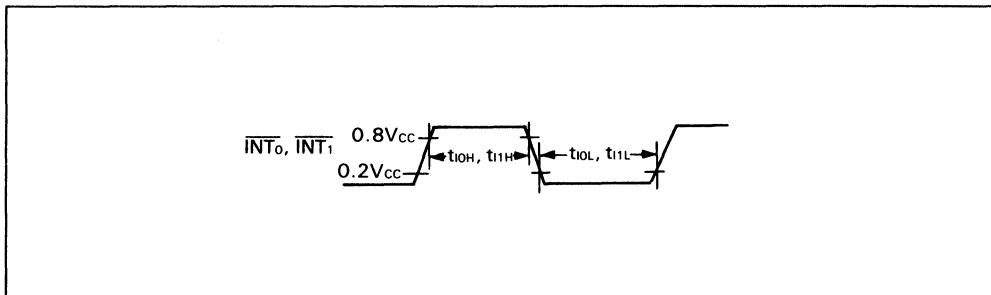


Figure 23. Interrupt Timing

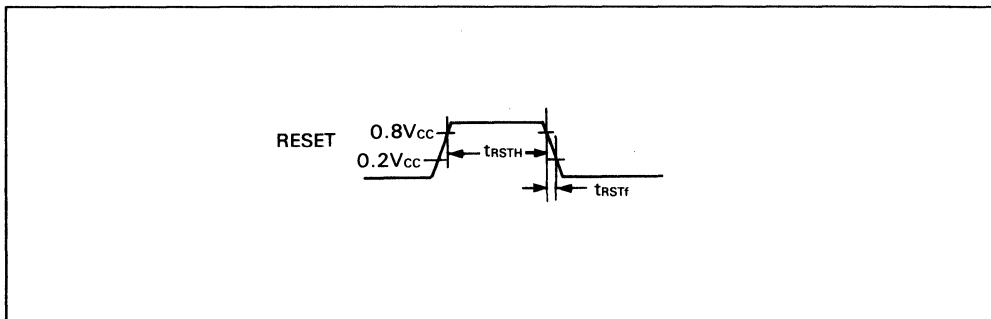


Figure 24. Reset Timing

HD404918
MASK OPTION LIST

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

I/O Option

Please enter check marks in applicable items for I/O option selection.

A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS
C: CMOS (not be used as Input)

Note: I/O options masked by are not available.

Pin	Input/Output	I/O Option			Pin	Input/Output	I/O Option			
		A	B	C			A	B	C	
D ₀	Input/Output				R0	RO ₀	Output			
D ₁	Input/Output					RO ₁	Output			
D ₂	Input/Output					RO ₂	Output			
D ₃	Input/Output					RO ₃	Output			
D ₄	Input/Output				R1	R1 ₀	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₅	Input/Output					R1 ₁	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₆	Input/Output					R1 ₂	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₇	Input/Output					R1 ₃	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₈	Input/Output				R2	R2 ₀	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₉	Input/Output					R2 ₁	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₀	Input/Output					R2 ₂	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₁	Input/Output					R2 ₃	Input/Output	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₂	Input/Output				R3	R3 ₀	Input/Output			
D ₁₃	Input/Output					R3 ₁	Input/Output			
D ₁₄	Input/Output					R3 ₂	Input/Output			
	Input/Output					R3 ₃	Input/Output			
					R4	R4 ₀	Input/Output			
						R4 ₁	Input/Output			
						R4 ₂	Input/Output			
						R4 ₃	Input/Output			

Notes * 1. Means high current pins.

* 2. Means high voltage pins only when "A" mask option is selected.



HD404918

ROM Code Media

Please enter check mark (■, X, ✓) in applicable item.

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

APPLICATION CHECK LIST

Oscillator (CPG option)

Please enter check mark (■, X, ✓) in applicable item.

CPG	<input type="checkbox"/>	Ceramic Filter
Option	<input type="checkbox"/>	Crystal
	<input type="checkbox"/>	External Clock



HD404919

—Preliminary—

Description

The HD404919 CMOS 4-bit single-chip microcomputer in the HMCS400 series incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins.

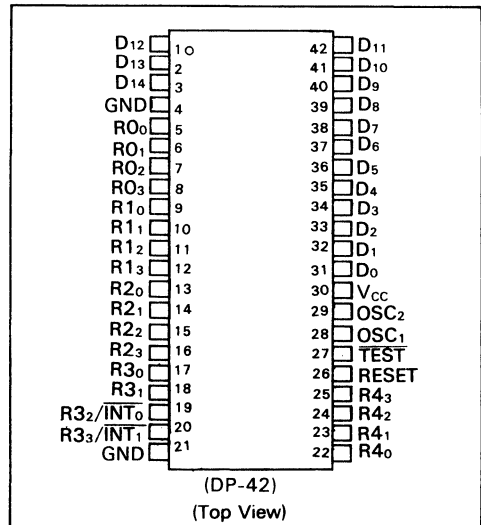
Features

- 4-bit architecture
- 16384 words of 10-bit ROM
- 992 digits of 4-bit RAM
- 35 I/O pins, including 27 high-voltage I/O pins (12 V max)
- Timer/counter
 - 11-bit prescaler
 - 8-bit auto-reload timer/event counter (timer B)
- Three interrupt sources
 - External: 2
 - Timer/counter: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time: 0.89 μ s
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Ceramic filter
 - External Clock input
- Standard 42-pin dual in-line plastic package
- Instruction set compatible with HD404918/HD40P4919; 100 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation/table lookup capability
- Bit manipulation for both RAM and I/O

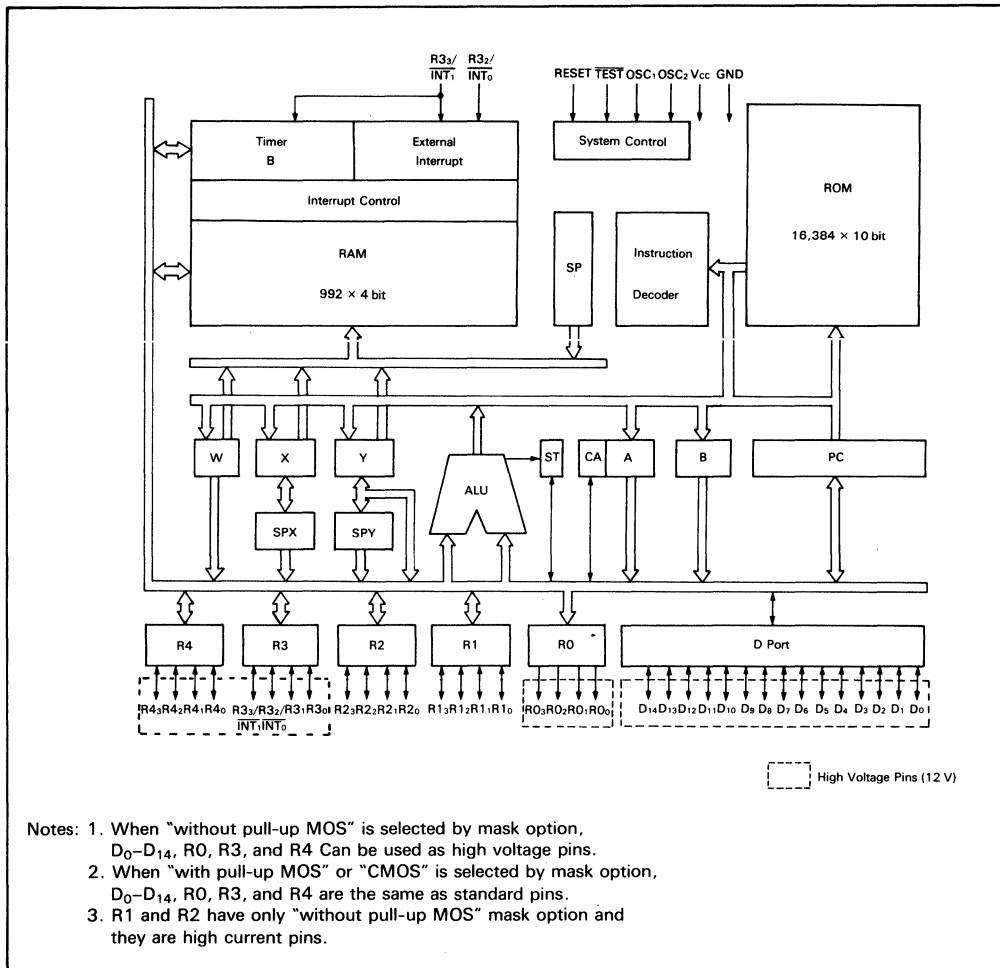
Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC HD40P4919 with the following fixed options:
 - I/O pin: NMOS open drain
 - Oscillator: ceramic filter oscillator (externally drivable)
 - Timing generator divider: Divide by 8
 - Package: standard 42-pin dual in-line ceramic package

Pin Arrangement



Block Diagram



Pin Description

GND, V_{CC} (Power Supply)

GND and V_{CC} are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D₀ to D₁₄ are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁–R₁₃, R₂–R₂₃, R₃–R₃₃, R₄–R₄₃ (R Ports)

R₀ to R₄ are 4-bit I/O ports. R₀ is an output port, and R₁ to R₄ are I/O ports. R₀, R₃, and R₄ are high-voltage ports, and R₁ and R₂ are high current ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, R₃₃ of port R₃ are multiplexed with INT₀ and INT₁ respectively. For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 16384 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After a reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$3FFF): Locations from \$0000 to \$3FFF can be used for program code.

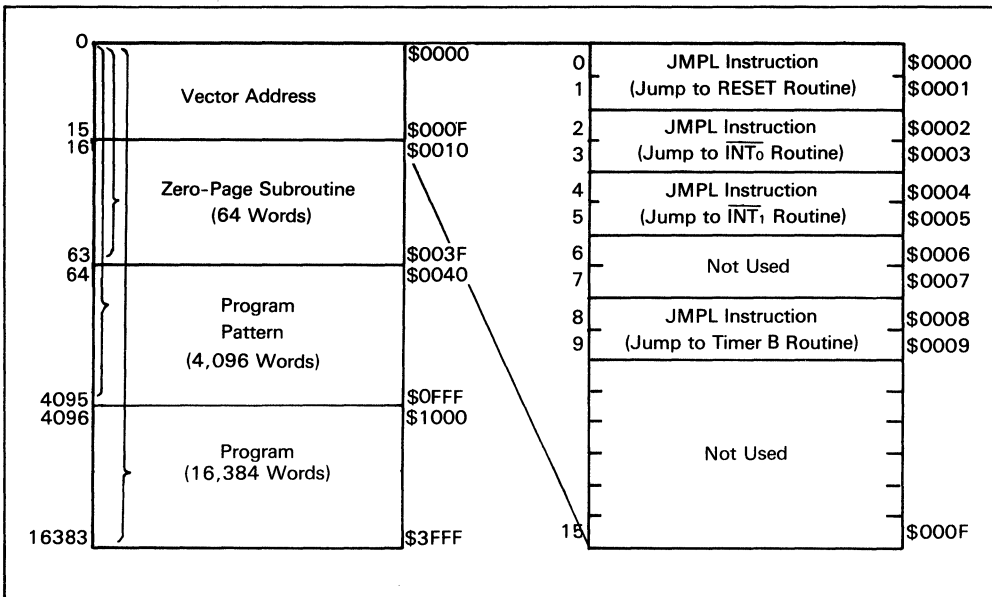


Figure 1. ROM Memory Map

Data Area (\$020 to \$3BF): 16 digits, \$020 through \$02F, in the data area are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine calls (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

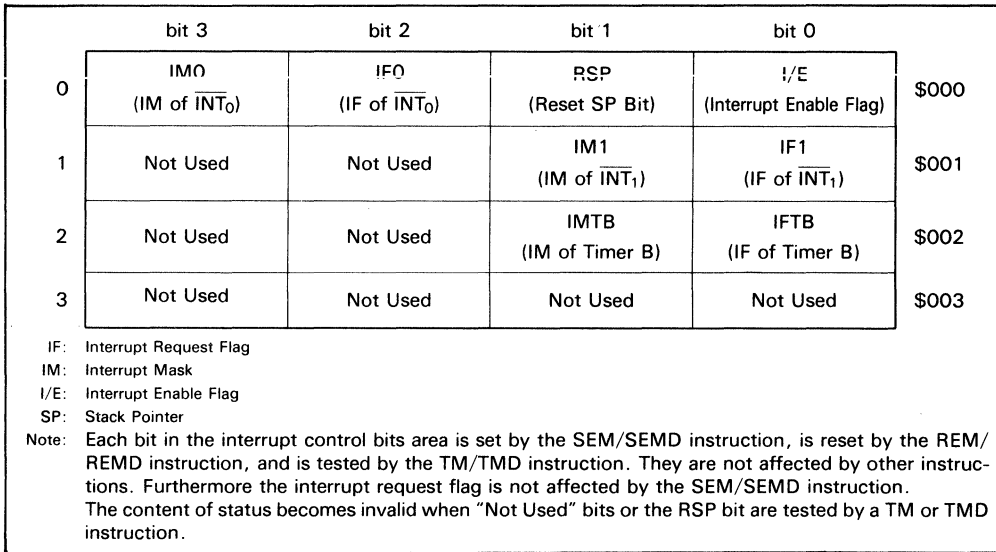


Figure 3. Interrupt Control Bit Area Configuration

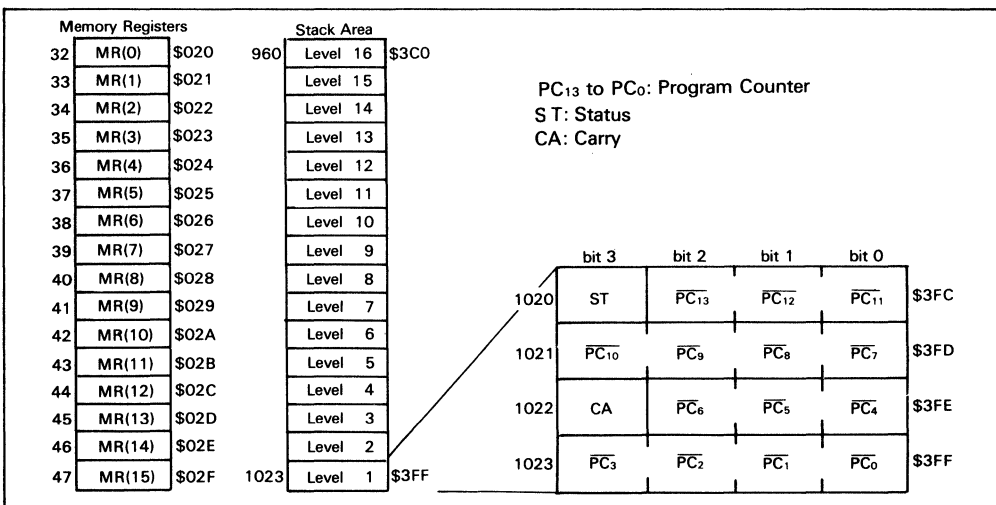


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU has nine registers and two flags for CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit

test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

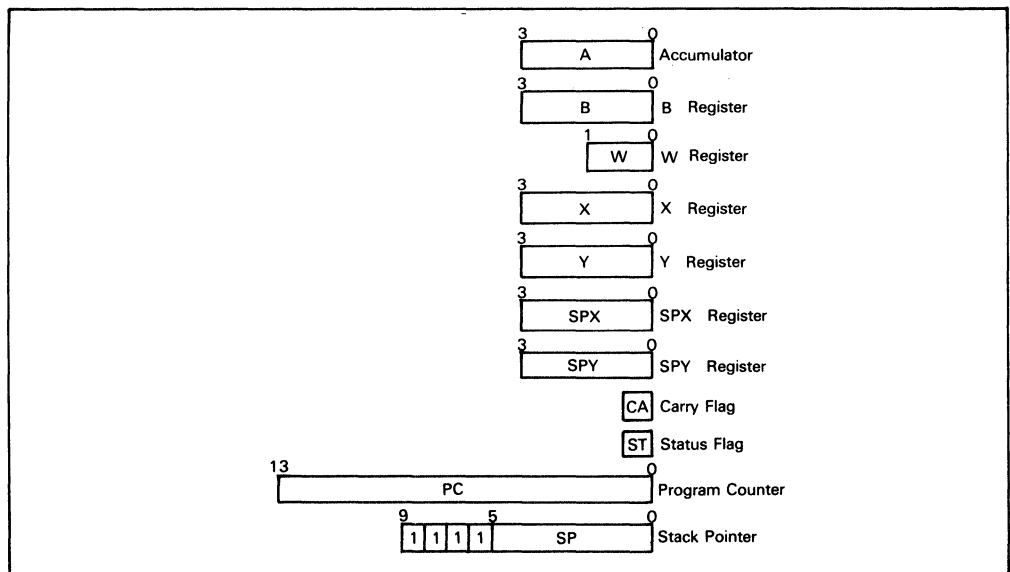


Figure 5. Registers and Flags

Interrupt

Three interrupt sources are available on the MCU: external requests (\overline{INT}_0 , \overline{INT}_1), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are

mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	-	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer B	3	\$0008

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer B
I/E	1	1	1
IFO·IM $\overline{0}$	1	0	0
IF1·IM1	*	1	0
IFTB·IMTB	*	*	1

Notes: Don't care

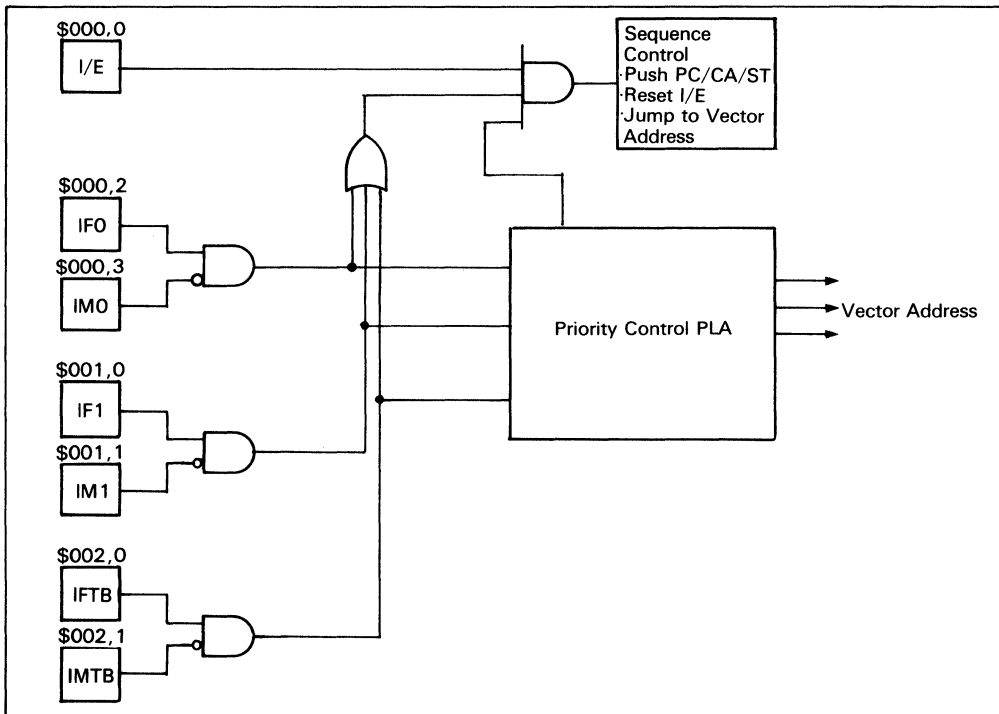


Figure 6. Interrupt Control Circuit Block Diagram

The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after the MCU jumps to the vector address.

In each vector address, program a JMPL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register

(PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When \overline{INT}_1 is used as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (\overline{INT}_0 , \overline{INT}_1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, and $R3_3/\overline{INT}_1$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

Ex Int Req Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin

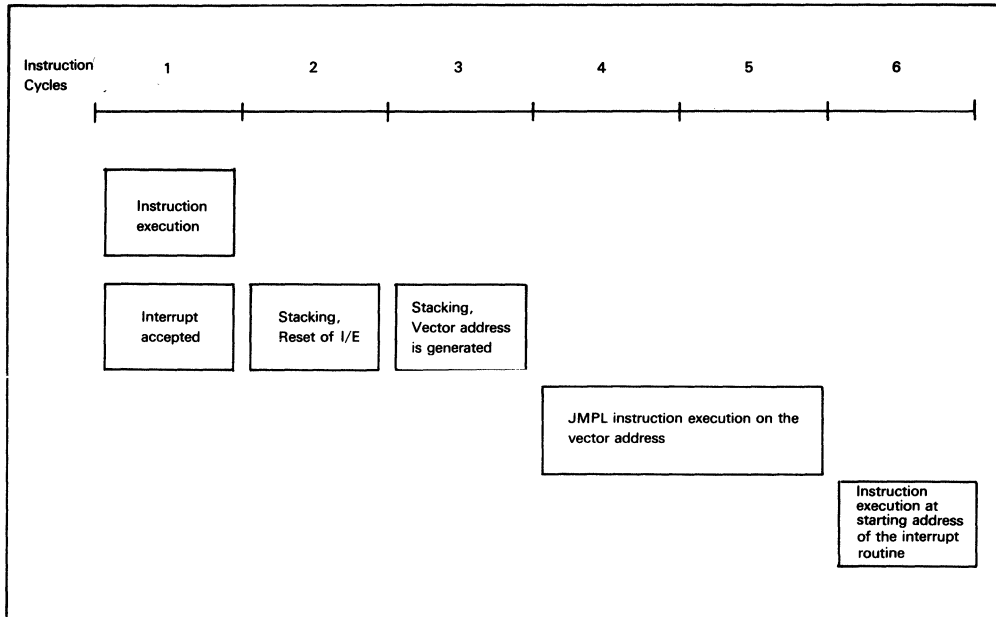


Figure 7. Interrupt Servicing Sequence

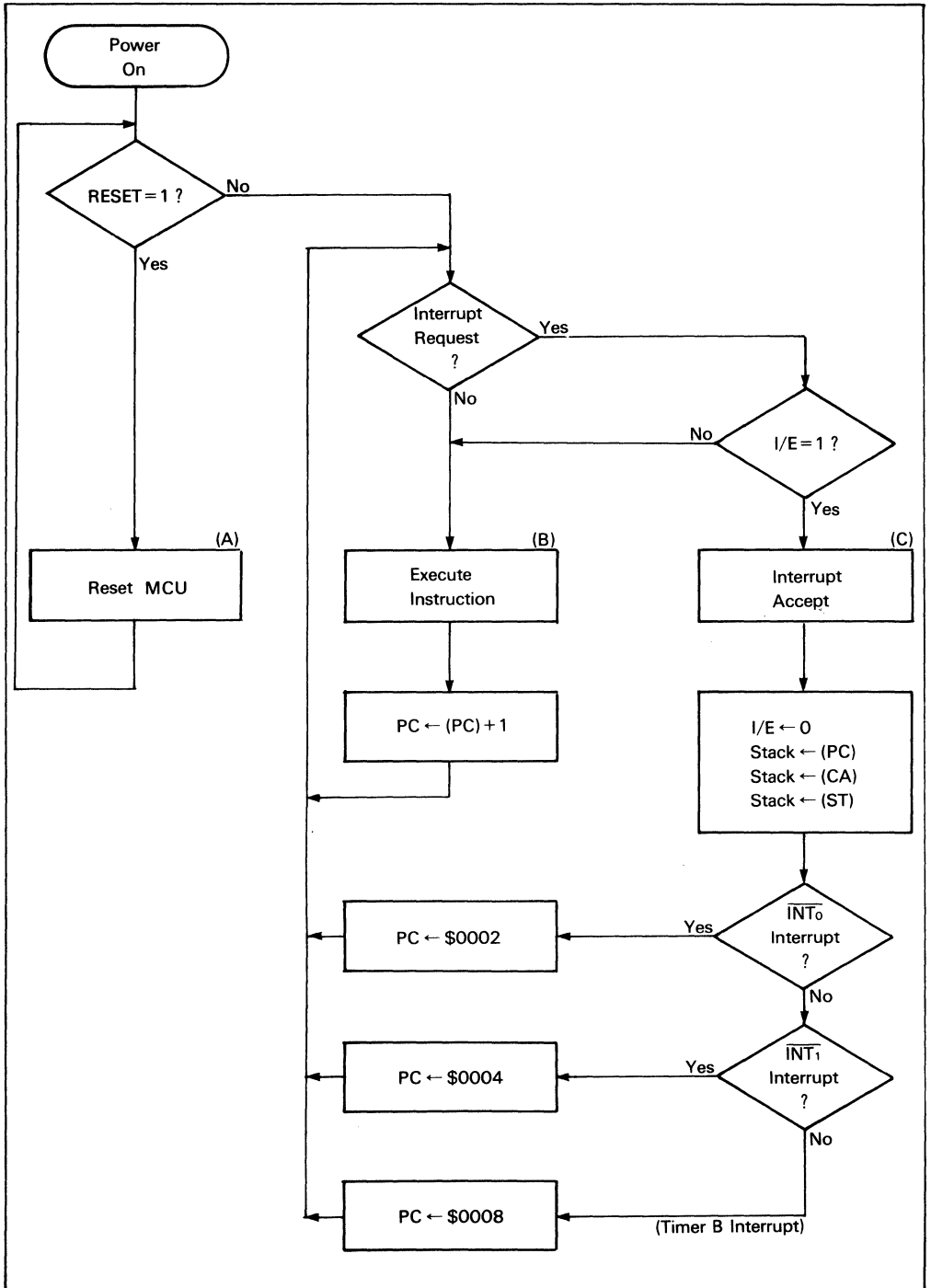


Figure 8. Interrupt Servicing Flowchart



Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/ event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

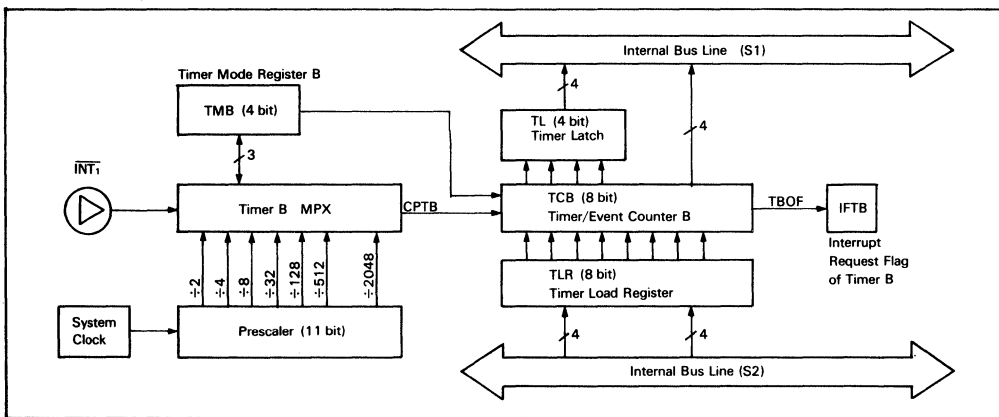


Figure 9. Timer Block Diagram



Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	\overline{INT}_1 (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

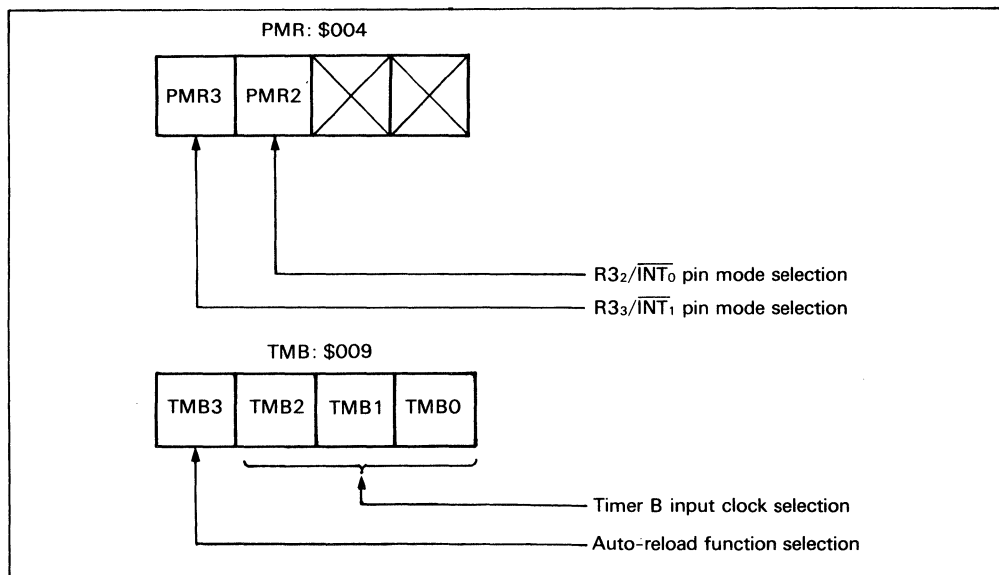


Figure 10. Mode Register Configuration and Function

Input/Output

The MCU has 35 I/O pins, 8 standard and 27 high voltage. One of three circuit types can be selected by mask option for each high-voltage pin: (A) "without pull-up MOS (NMOS open drain)", (B) "with pull-up MOS", or (C) "CMOS". High-voltage pins can be used as high-voltage I/O pins only when (A) is selected, but except R1 and R2. R1 and R2 are fixed to (A) mask option.

When any input/output pin is used as an input pin, the mask option and output data must be selected in the manner specified in table 11.

Output Circuit Operation With Pull-Up MOS Standard Pins: In the standard pin option with pull-up MOS, the circuit shown in figure 11 shortens the rise time of the output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on and shorten the rise time. The write pulse keeps PMOS in the on state for one-eighth of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{\text{HLT}}$ signal becomes 0 in stop mode, MOS (A) (B) (C) turn off.

D Port: The D I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 for the I/O pin circuit types.

R Ports: The six R ports are composed of 16 I/O pins, 4 output-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU is not be affected when the input-only and/or non-existing ports are written into, while invalid data will be read from the output-only and/or non-existing ports.

The R3₂ and R3₃ pins are multiplexed with the INT₀ and INT₁ pins respectively. See table 10 for the selectable circuit types for these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage: select "without pull-up MOS" (NMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard: select "without pull-up MOS" (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when stop mode, is can called the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 12 shows the parts initialized by MCU reset, and the status of each.

Table 10. I/O Pin Circuit Types

	Without Pull-Up MOS (NMOS Open Drain) (A)	With pull-up MOS (B)	CMOS (C)	Applicable Pins
I/O Common Pins				D ₀ –D ₁₄ R ₃₀ –R ₃₃ R ₄₀ –R ₄₃
High Current	Not available	Not available	Not available	
High Voltage	Available	Not available	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	Applicable pins
I/O Common Pins		R ₁₀ –R ₁₃ R ₂₀ –R ₂₃
High Current	Available	
High Voltage	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	With Pull-Up MOS (B)	CMOS (C)	Applicable Pins
Output Pins				R ₀₀ –R ₀₃
High Current	Not available	Not available	Not available	
High Voltage	Available	Not available	Not available	

- Notes: 1. When "without pull-up MOS" is selected by mask option, D₀–D₁₄, R₀, R₃, and R₄ can be used as high voltage pins.
 2. When "with pull-up MOS" or "CMOS" is selected by mask option, D₀–D₁₄, R₀, R₃, and R₄ are the same as standard pins.
 3. R₁ and R₂ have only "without pull-up MOS" mask option and they are high current pins.



Table 11. Data Input from Input/Output Common Pins

I/O Pin Circuit Type	Input Possible	Input Pin State
CMOS	No	—
Without pull-up MOS (NMOS open drain)	Yes	1
With pull-up MOS	Yes	1

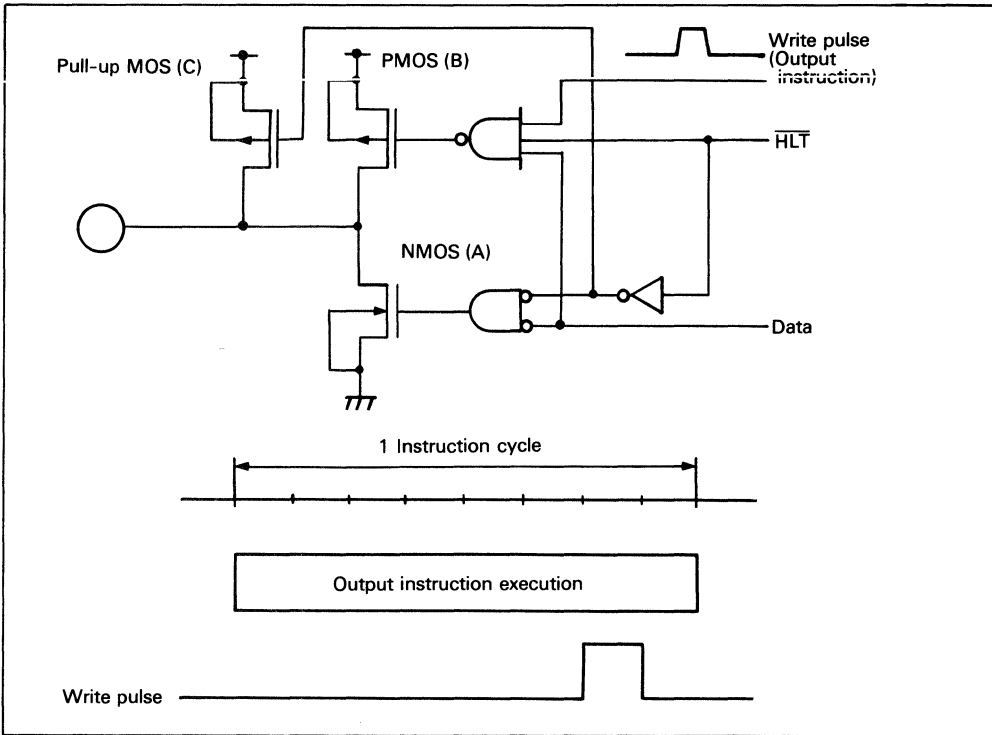


Figure 11. Output Circuit Operation of Pins With Pull-Up MOS Option

Table 12. Initial Value After MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable branch with conditional branch instructions
Stack Pointer (SP)		\$3FF	Stack level is 0
I/O Pin Output Register	(A) Without Pull-Up MOS	1	Enable input
	(B) With Pull-Up MOS	1	Enable input
	(C) CMOS	1	—
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—

Note: MCU reset affects the rest of registers as follows:

Item		After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop-Mode)
Carry	(CA)	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.	The contents of the items before MCU reset are not retained. It is necessary to initialize them by software.
Accumulator	(A)		
B Register	(B)		
W Register	(W)		
X/SPX Registers	(X/SPX)		
Y/SPY Registers	(Y/SPY)		
RAM		The contents of RAM before MCU reset (just before STOP instruction) are retained.	

Internal Oscillator Circuit

Figure 12 outlines the internal oscillator circuit. In addition, see figure 13 for the layout of

the ceramic filter. In this cases, external clock operation is available.

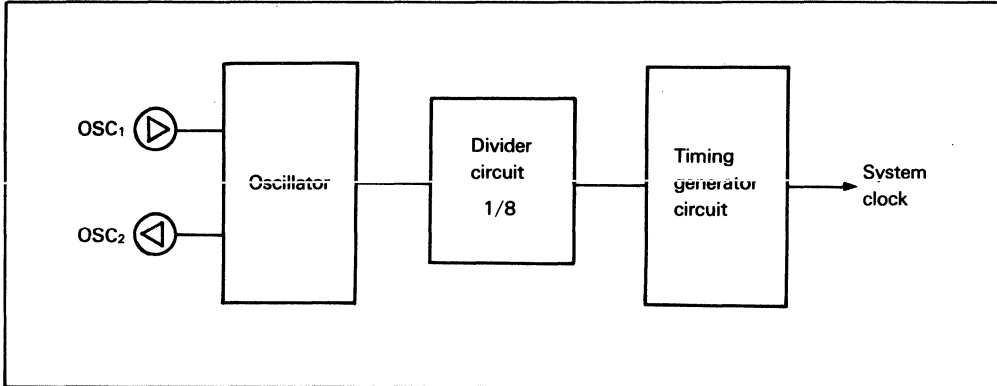


Figure 12. Internal Oscillator Circuit

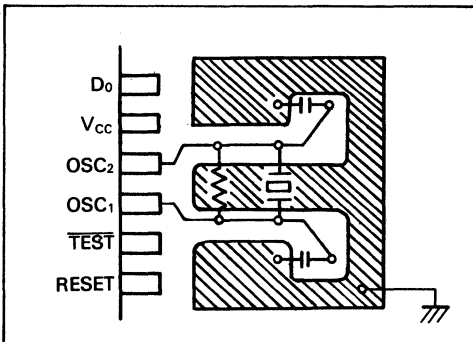
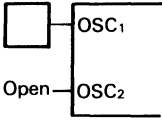
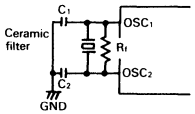


Figure 13. Layout of Ceramic Filter

Table 13. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
External Clock Operation	<p>Oscillator</p> 	
Ceramic Filter Oscillator		<p>Ceramic filter CSA 8.00MT (Murata)</p> <p>$R_f: 1\text{ M}\Omega \pm 20\%$ $C_1: 30\text{ pF} \pm 20\%$ $C_2: 30\text{ pF} \pm 20\%$</p>

- Notes: 1. For the ceramic filter resonator, the upper circuit parameters are recommended by the ceramic filter maker. Ceramic filter resonator, and the floating capacitance change circuit parameters in designing the board. In designig the resonator, please consult with the engineers of the ceramic filter maker to determine the circuit parameters.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross other wires. Refer to the layout of ceramic filter (figure 13).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 14). Figure 14 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 14. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, flag	Retained	Reset (note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (note 2)	High impedance
Timer/counter	Active	Stopped
Recovery method	RESET input, interrupt request	RESET input

Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 12 for the contents of flags and registers.

2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

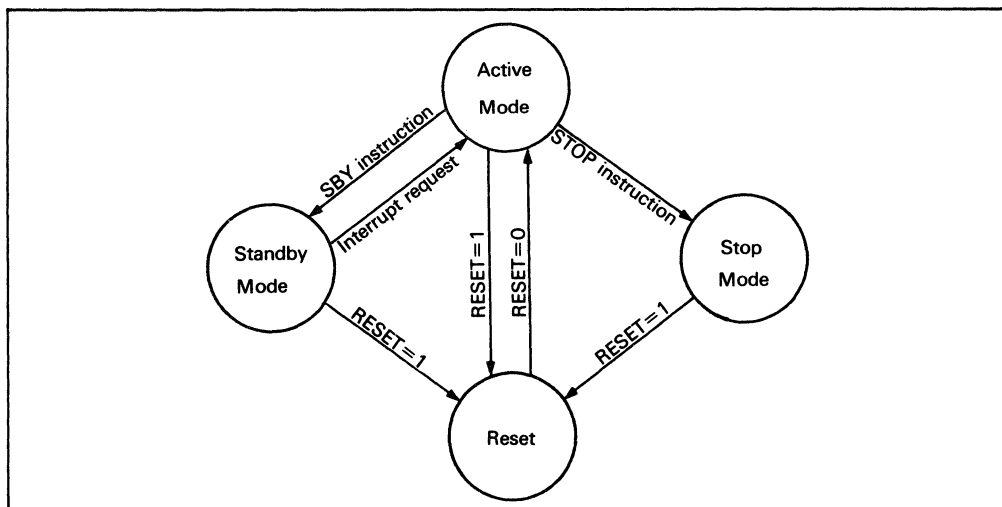


Figure 14. MCU Operation Mode Transition



Standby mode may be cancelled by inputting **RESET** or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the **SBY** instruction.

Figure 15 shows the flowchart of the standby mode.

Stop Mode: Executing a **STOP** instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 16, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

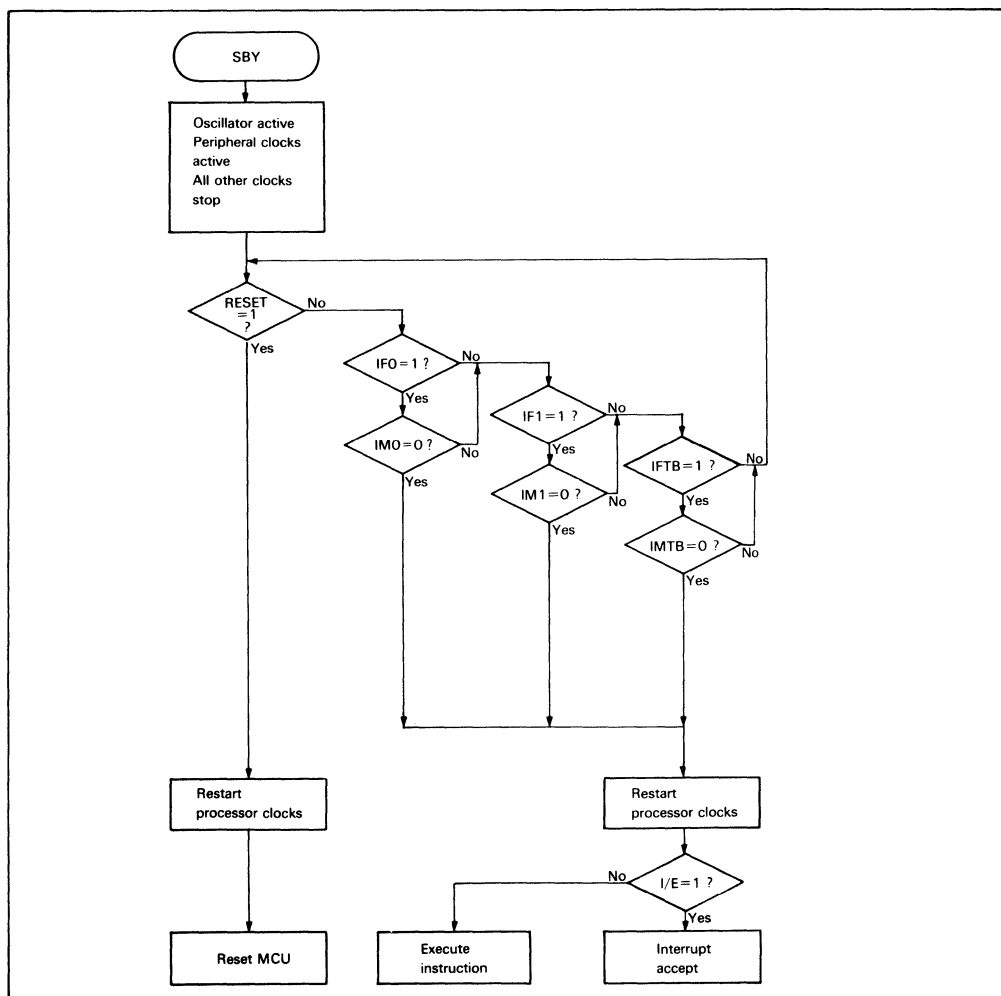


Figure 15. MCU Standby Mode Operation Flowchart



RAM Addressing Mode

As shown in figure 17, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 18.

Direct addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 19), executing a BR instruction transfers the PC contents to the next page because of the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 20). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

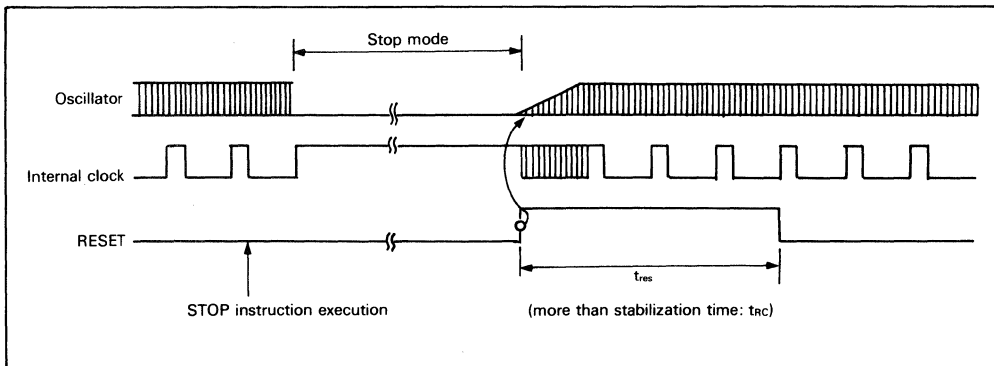


Figure 16. Timing Chart of Recovering from Stop Mode



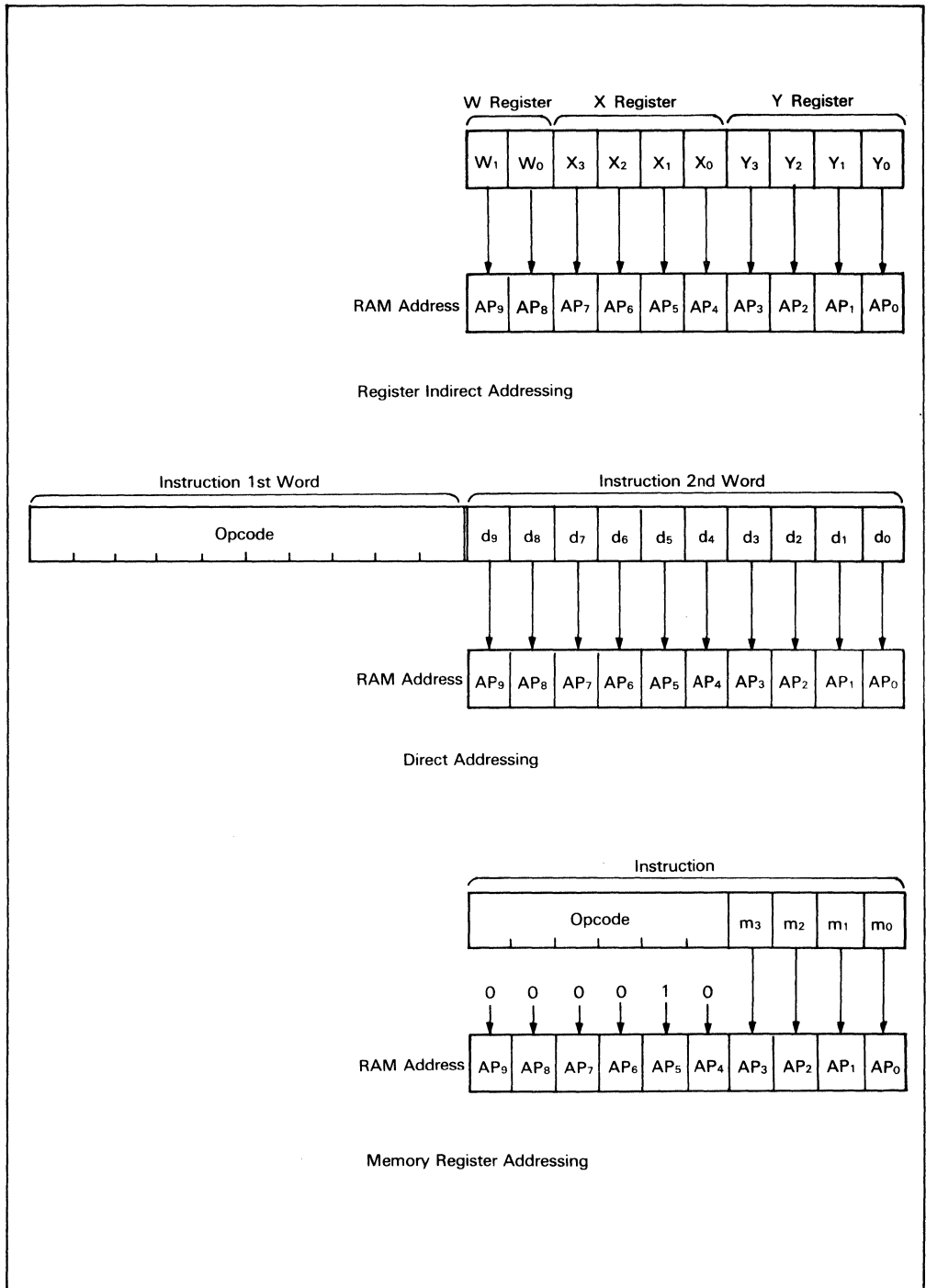


Figure 17. RAM Addressing Mode

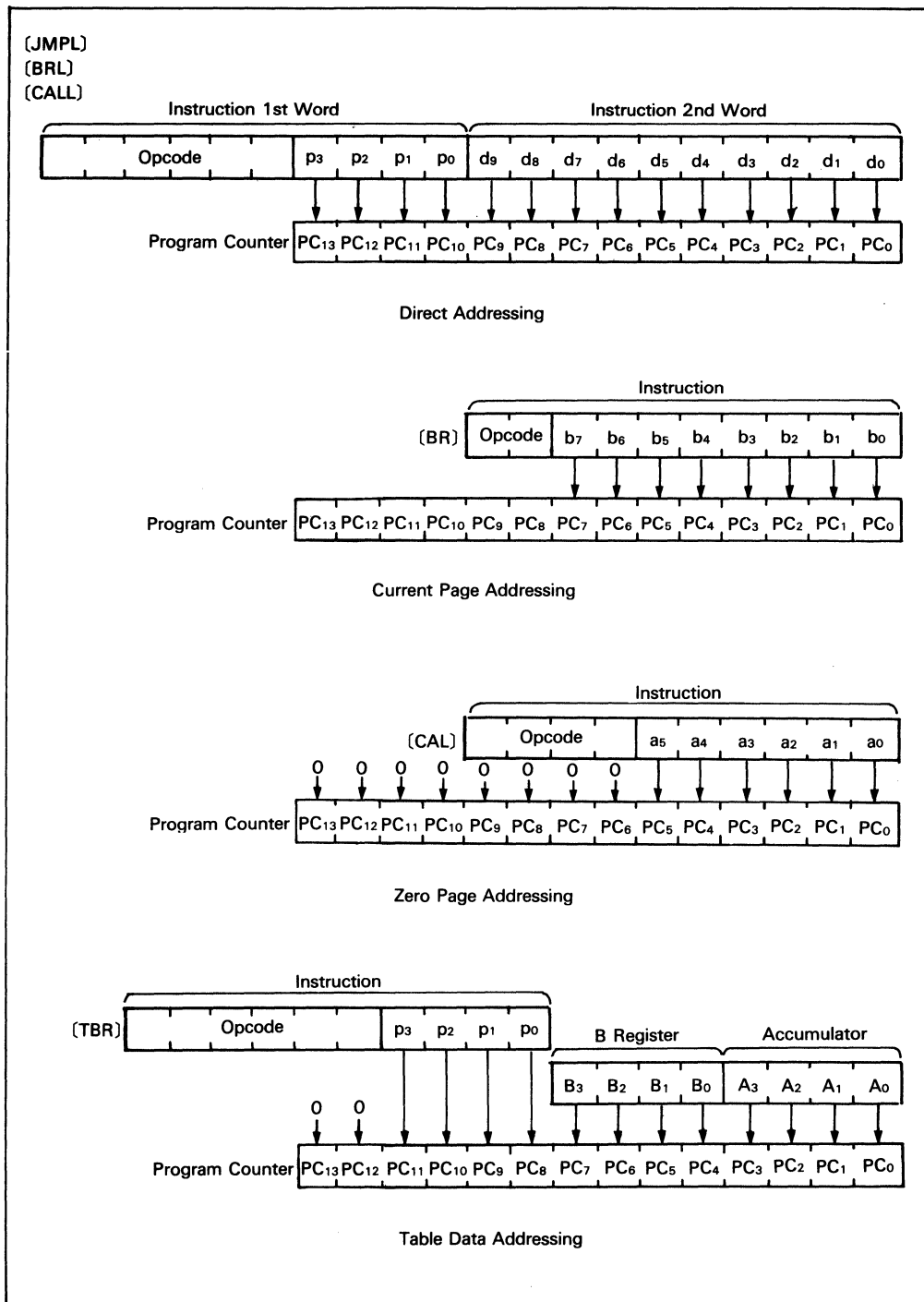


Figure 18. ROM Addressing Mode



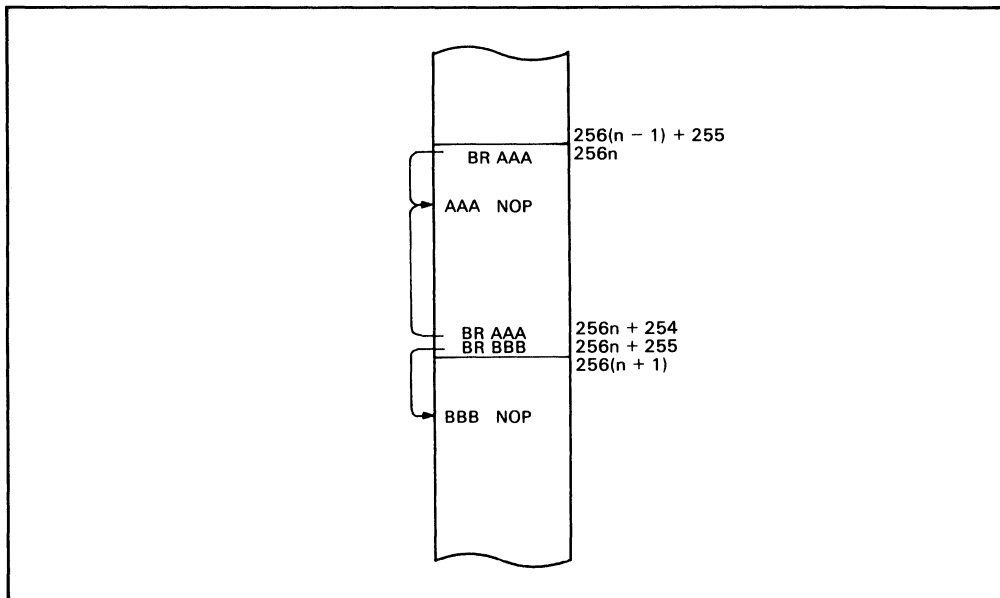


Figure 19. BR Instruction Branch Destination on Page Boundary

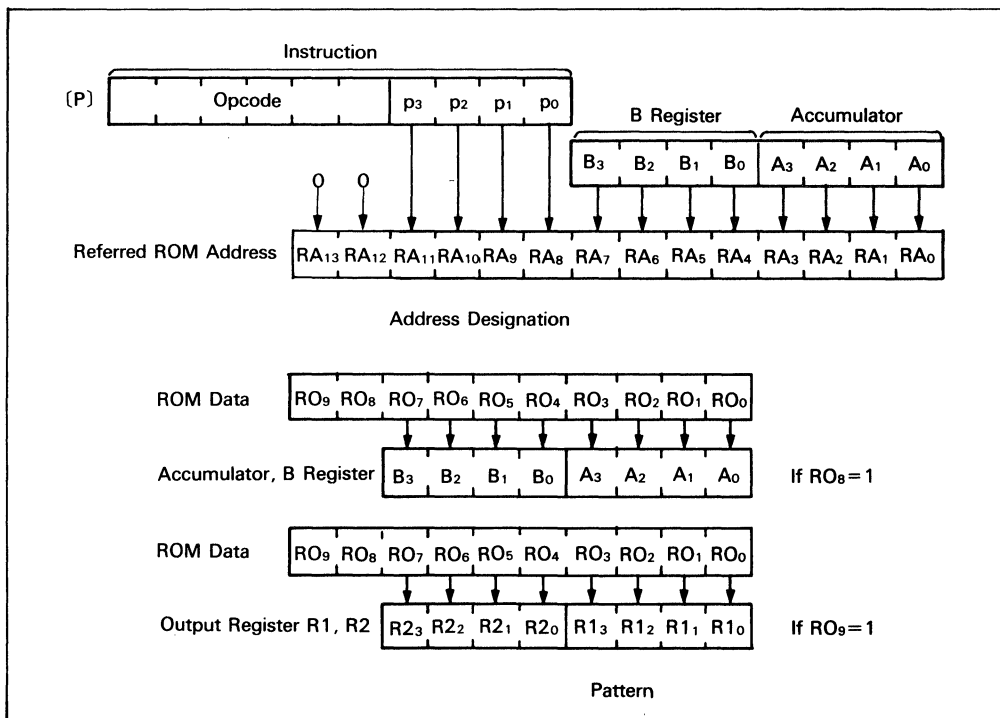


Figure 20. P Instruction

Instruction Set

The HD404919 provides 100 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction

6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 15-24 list their functions, and table 25 is an opcode map.

Table 15. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 16. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note :An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.

Table 17. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 18. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A→M, (X→SPX, Y→SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A→M, Y+1→Y (X→SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A→M, Y-1→Y (X→SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M→A, (X→SPX, Y→SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M→B, (X→SPX, Y→SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X→SPX, Y→SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes each (example of LMAIY (X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 19. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR



Table 20. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 21. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 22. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 →I/E CA Restore	ST	1/3

Table 23. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 24. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

Note: HD404919 has no serial interface, so STS (start serial) operates the same as NOP.



Table 25. Opcode Map

R8	0															1																
	L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E
0	NO	SP	SP	SP	AN	EM			AM					OR	M		LAW				ANEM				AMD				ORM			
1	RTN	RTN			ALE				AMC					EOR	M		LWA				ALEM				AMCD				EORM			
2	INEM										i(4)				INEMD										i(4)							
3	ILEM										i(4)				ILEMD										i(4)							
4	LBM(XY)			BNE		LAB		IB		COMB		OR		SB		STOP																
5	LMAI(YX)		AYY		LASPY		IY		JMPL										p(4)													
6	NEGA		RED		LASPX		TC		CALL										p(4)													
0	YNEI										i(4)				BRL										p(4)							
8	XMA(XY)			SEM n(2)			REM n(2)			TM n(2)			XMD		SEMD n(2)			REMD n(2)			TMD n(2)											
9	LAM(XY)			LMA(XY)			SMC		ANM		LMD		LMAD		SMCD		ANMD															
A	ROTR		ROTL		DAA		DAS		LAY		LMID										i(4)											
B	TBR										p(4)				P										p(4)							
C	XMB(XY)			BLEM		LBA		DB																								
D	LMADY(X)		SY		LYA		DY		CAL										a(6)													
E	TD		SED		LXA		REC		SEC																							
F	LWI i(2)																															
1	0	LBI				i(4)																										
1	1	LYI				i(4)																										
2	2	LXI				i(4)																										
3	3	LAI				i(4)																										
4	4	LBR				m(4)																										
5	5	LAR				m(4)																										
6	6	REDD				m(4)																										
7	7	LAMR				m(4)				BR		b(8)																				
8	8	AI				i(4)																										
9	9	LMIY				i(4)																										
A	A	TDD				m(4)																										
B	B	ALEI				i(4)																										
C	C	LRB				m(4)																										
D	D	LRA				m(4)																										
E	E	SEDD				m(4)																										
F	F	XMRA				m(4)																										

 1-word/2-cycle Instruction
 1-word/3-cycle Instruction
 RAM Direct Address Instruction (2-word/2-cycle)
 2-word/2-cycle Instruction



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		-0.3 to + 15	V	4
Total Allowance of Input Current	ΣI_O	200	mA	5
Maximum Input Current	I_O	15	mA	7, 8
		35	mA	7, 10
Maximum Output Current	$-I_O$	4	mA	8, 9
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	6
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	

- Notes: 1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_{14}$, $R_3 - R_4$, R_0
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $R_1 - R_2$.

Electrical Characteristics

DC Characteristics

($V_{CC} = 4\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET,	$0.85 V_{CC}$		$V_{CC} + 0.3$	V		
		\overline{INT}_0 , INT ₁	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET,	- 0.3		$0.15 V_{CC}$	V		
		\overline{INT}_0 , INT ₁	- 0.3		$0.2 V_{CC}$	V		
		OSC ₁	- 0.3		0.5	V		
Input/Output Leakage Current	$ I_{IL} $	RESET, INT ₀ , INT ₁ , OSC ₁		1		μA	$V_{in} = 0\text{ V to }V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}		6.5		mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}, \div 8$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}		1.8		mA	$V_{CC} = 5\text{ V};$ $f_{osc} = 4\text{ MHz}, \div 8$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}		10		μA	$V_{in}(\overline{TEST}) = V_{CC} - 0.3\text{ V to }V_{CC};$ $V_{CC}; V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes: 1. Excluding pull-up MOS current and output buffer current.
 2. The MCU is in the reset state. Input/output current does not flow.
 • MCU in reset state, operation mode
 • RESET, TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 • MCU in standby mode
 • Input/output in reset state
 • RESET: GND
 • TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 4. Excluding pull-up MOS current.
 5. When $f_{osc} = x\text{ MHz}$, estimate the current dissipation as follows:
 Max value @ $x\text{ MHz} = x/4 \times (\text{max value @ }4\text{ MHz})$

Input/Output Characteristics for Standard Use

($V_{CC}=4V$ to $6V$, $GND=0V$, $T_a=-20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	R1-R2	$0.7V_{CC}$		$V_{CC} + 0.3$	V		3
		D ₀ -D ₁₄ R3-R4						4
Input Low Voltage	V_{IL}	R1-R2	-0.3		$0.3V_{CC}$	V		3
		D ₀ -D ₁₄ R3-R4						4
Output High Voltage	V_{OH}	D ₀ -D ₁₄ R3-R4, R0	$V_{CC} - 1.0$			V	- $I_{OH} = 1.0$ mA	1
		D ₀ -D ₁₄ , R3-R4, R0	$V_{CC} - 0.5$			V	- $I_{OH} = 0.5$ mA	1
Output Low Voltage	V_{OL}	D ₀ -D ₁₄ , R3-R4, R0			0.4	V	$I_{OL} = 1.6$ mA	
		R1-R2			1.2	V	$V_{CC} = 5V$, $I_{OL} = 25$ mA	3
Input/Output Leakage Current	$ I_{IJ} $	D ₀ -D ₁₄ , R3-R4, R0			1	μA	$V_{in} = 0V$ to V_{CC}	2
		R1-R2			20			
Pull-Up MOS Current	$-I_p$	D ₀ -D ₁₄ , R3-R4, R0	30	60	150	μA	$V_{CC} = 5V$, $V_{in} = 0V$	4

- Notes: 1. Applied to I/O pins with CMOS output selected by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins without pull-up MOS mask option.
 4. With pull up MOS is selected by mask option.

Input/Output Characteristics for High Voltage Use

($V_{CC} = 4V$ to $6V$, $GND = 0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₁₄ , R3-R4	$0.7V_{CC}$		12	V		1
Input Low Voltage	V_{IL}	D ₀ -D ₁₄ , R3-R4	-0.3		$0.3V_{CC}$	V		1
Output High Voltage	V_{OH}	D ₀ -D ₁₄ , R3-R4, R0	11.5			V	500 k Ω to 12V	1
Output Low Voltage	V_{OL}	D ₀ -D ₁₄ , R3-R4, R0			0.4	V	$I_{OL} = 1.6$ mA	1
Input/Output Leakage Current	$ I_{IJ} $	D ₀ -D ₁₄ , R3-R4, R0			1	μA	$V_{in} = 0V$ to V_{CC}	1

- Notes: 1. Applied to I/O pins without pull-up MOS by mask option.



HD404919

AC Characteristics

($V_{CC} = 4\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC ₁ , OSC ₂	0.4	8	9	MHz	Divide by 8	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs		
Oscillator Stabilization Time	t_{RC}	OSC ₁ , OSC ₂			20	ms		1
External clock Frequency	f_{cp}	OSC ₁	0.4	8	9	MHz		2
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC ₁	41			ns	Divide by 8	2
External Clock Rise Time	t_{CPr}	OSC ₁			15	ns		2
External Clock Fall Time	t_{CPf}	OSC ₁			15	ns		2
Instruction cycle Time	t_{cyc}		0.89	1	20	μs		2
\overline{INT}_0 High Level Width	t_{i0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{i0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms		4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage 4 V after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 21.)

2. See figure 22.
3. See figure 23.
4. See figure 24.

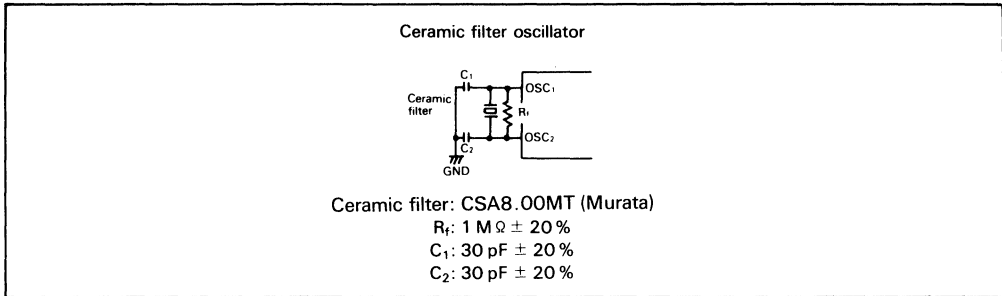


Figure 21. Oscillator Circuit

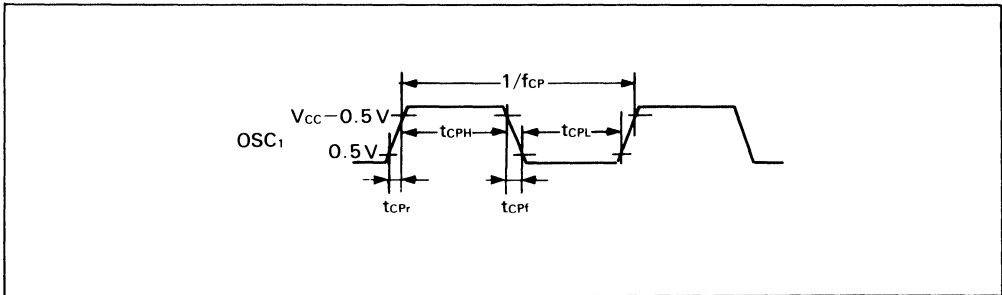


Figure 22. Oscillator Timing

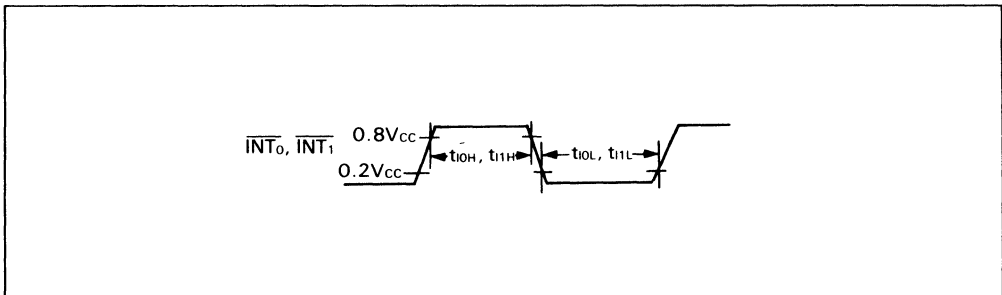


Figure 23. Interrupt Timing

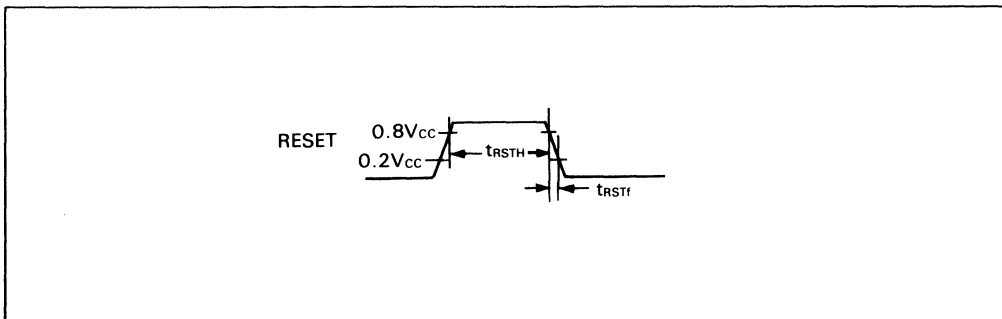


Figure 24. Reset Timing

HD404919

HD404919
MASK OPTION LIST

Date of Order	
Customer	
Dept.	
Name	
ROM Code Name	
LSI Type Number (Hitachi's entry)	

I/O Option

Please enter check marks in applicable items for I/O option selection.

A: Without Pull-up MOS (NMOS Open Drain) B: With Pull-up MOS

C: CMOS (not be used as Input)

Note: I/O options masked by are not available.

Pin	Input/Output	I/O Option			Pin	Input/Output	I/O Option			
		A	B	C			A	B	C	
D ₀	Input/Output				R0	R0 ₀	Output			
D ₁	Input/Output					R0 ₁	Output			
D ₂	Input/Output					R0 ₂	Output			
D ₃	Input/Output					R0 ₃	Output			
D ₄	Input/Output				R1	R1 ₀	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₅	Input/Output					R1 ₁	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₆	Input/Output					R1 ₂	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₇	Input/Output					R1 ₃	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₈	Input/Output				R2	R2 ₀	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₉	Input/Output					R2 ₁	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₀	Input/Output					R2 ₂	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₁	Input/Output					R2 ₃	Input/Output		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
D ₁₂	Input/Output				R3	R3 ₀	Input/Output			
D ₁₃	Input/Output					R3 ₁	Input/Output			
D ₁₄	Input/Output					R3 ₂	Input/Output			
	Input/Output					R3 ₃	Input/Output			
					R4	R4 ₀	Input/Output			
						R4 ₁	Input/Output			
						R4 ₂	Input/Output			
						R4 ₃	Input/Output			

Notes * 1. Means high current pins.

* 2. Means high voltage pins only when "A" mask option is selected.



ROM Code Media

Please enter check mark (■, X, ✓) in applicable item.

ROM Code Media	
<input type="checkbox"/>	EPROM: Emulator Type
<input type="checkbox"/>	EPROM: EPROM On-Package Microcomputer Type

APPLICATION CHECK LIST

Oscillator (CPG option)

Please enter check mark (■, X, ✓) in applicable item.

CPG	<input type="checkbox"/>	Ceramic Filter
Option	<input type="checkbox"/>	External Clock

HD40P4919

—Preliminary—

Description

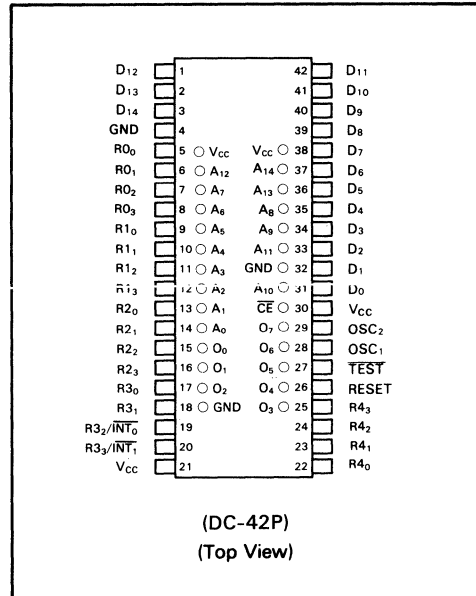
The HD40P4919 CMOS 4-bit single-chip microcomputer in the HMCS400 series incorporates ROM, RAM, I/O, and timer/counter and contain high-voltage I/O pins including high-current output pins.

By modifying the program in the EPROM, the HD40P4919 can be used for the evaluation of the HD40P4919 and HD404919 on for small-scale production.

Features

- 4-bit architecture
- Application to 8k, 16k words × 10 bits of EPROM
 - 8192 words × 10 bits } ...HN27C256
 - 16384 words × 10 bits }
- 992 digits of 4-bit RAM
- 35 I/O pins, including 27 high-voltage I/O pins (12 V max)
- Timer/counter
 - 11-bit prescaler
 - 8-bit auto-reload timer/event counter (timer B)
- Three interrupt sources
 - External: 2
 - Timer/counter: 1
- Subroutine stack
 - Up to 16 levels including interrupts
- Minimum instruction execution time: 0.89μs
- Low power dissipation modes
 - Standby: Stops instruction execution while allowing clock oscillation and interrupt functions to operate
 - Stop: Stops instruction execution and clock oscillation while retaining RAM data
- On-chip oscillator
 - Ceramic filter
 - External Clock input
- Standard 42-pin dual in-line ceramic package
- Instruction set compatible with HD404918/HD404919; 100 instructions
- High programming efficiency with 10-bit/word ROM: 78 single-word instructions
- Direct branch to all RAM areas
- Direct or indirect addressing of all RAM areas
- Subroutine nesting up to 16 levels including interrupts
- Binary and BCD arithmetic operations
- Powerful logical arithmetic operations
- Pattern generation/table lookup capability
- Bit manipulation for both RAM and I/O

Pin Arrangement



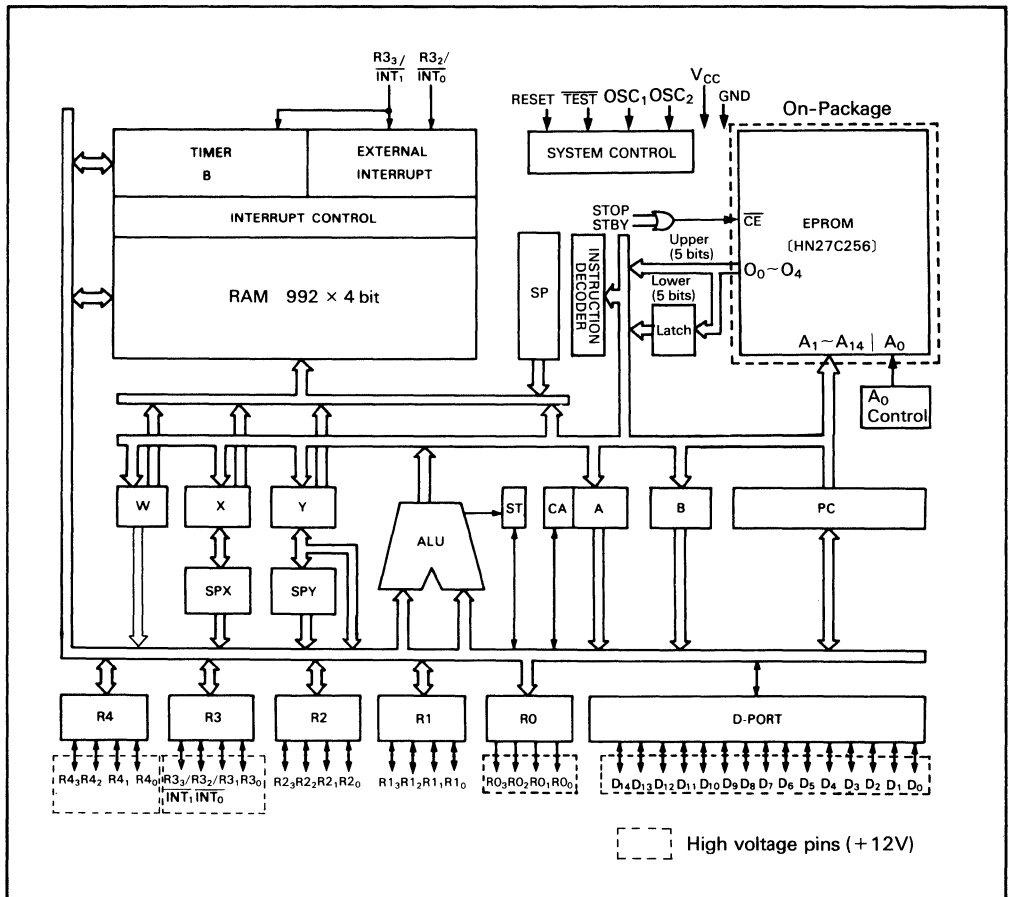
Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

Recommended Application EPROM

Type No.	Program Memory Capacity	fosc (MHz)	EPROM Type No.
HD40P4919	8192 words	4	HN27C256G20
		8	HN27C256H85
	16384 words	4	HN27C256G20
		8	HN27C256H85

Block Diagram



Pin Description

GND, V_{CC} (Power Supply)

GND and V_{CC} are the power supply pins for the MCU. Connect the GND to the ground (0 V) and apply the V_{CC} power supply voltage to the V_{CC} pin.

TEST (Test)

TEST is for test purposes only. Connect it to V_{CC}.

RESET (Reset)

RESET resets the MCU. For details, see Reset section.

OSC₁, OSC₂ (Oscillator Connections)

OSC₁ and OSC₂ are input pins for the internal oscillator circuit. They can be connected to a ceramic filter resonator, or external oscillator circuits. For details, see Internal Oscillator Circuit section.

D₀–D₁₄ (D Port)

The D port is an input/output port addressed by the bit. These 15 pins are all input/output pins. D₀ to D₁₄ are high-voltage pins. The circuit type for each pin can be selected using a mask option. For details, see Input/Output section.

R₀–R₀₃, R₁–R₁₃, R₂–R₂₃, R₃–R₃₃, R₄–R₄₃ (R Ports)

R₀ to R₄ are 4-bit I/O ports. R₀ is an output port, and R₁ to R₄ are I/O ports. R₀, R₃, and R₄ are high-voltage ports, and R₁ and R₂ are high current ports. Each pin has a mask option which selects its circuit type. The pins R₃₂, R₃₃ of port R₃ are multiplexed with INT₀ and INT₁ respectively. For details, see Input/Output section.

INT₀, INT₁ (Interrupts)

INT₀ and INT₁ are external interrupts for the MCU. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃ respectively. For details, see Interrupt section.

Functional Description

ROM Memory Map

The MCU includes 16384 words × 10 bits of ROM. ROM is described in the following paragraphs and the ROM memory map (figure 1).

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMWL instructions to branch to the starting address of the initialization program and of the interrupt service programs. After a reset or interrupt routine is serviced, the program is executed from the vector address.

Zero-Page Subroutine Area (\$0000 to \$003F): Locations \$0000 through \$003F are reserved for subroutines. CAL instructions branch to subroutines.

Pattern Area (\$0000 to \$0FFF): Locations \$0000 through \$0FFF are reserved for ROM data. P instructions allow referring to the ROM data as a pattern.

Program Area (\$0000 to \$3FFF): Locations from \$0000 to \$3FFF can be used for program code.

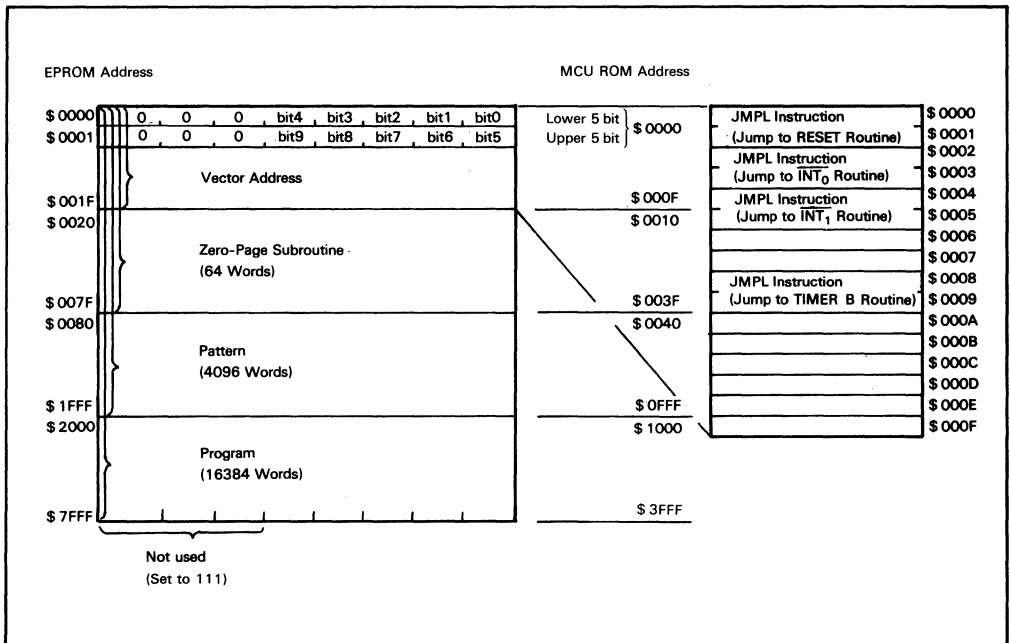


Figure 1. EPROM Memory Map

RAM Memory Map

The MCU includes 992 digits of 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bit Area (\$000 to \$003): The interrupt control bit area (figure 3) is used for interrupt controls. It is accessible only by a RAM bit manipulation instruction.

However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$00B): The special function registers are the mode or data registers for the external interrupt, and the timer/counter. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions.

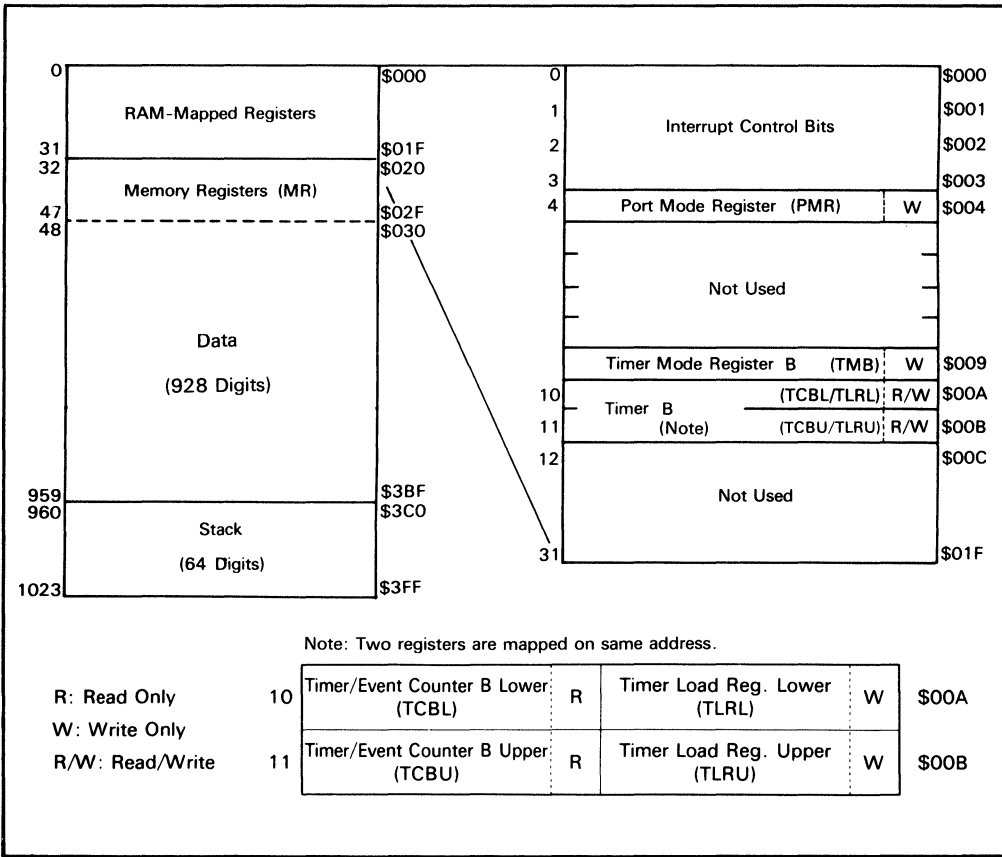


Figure 2. RAM Memory Map

Data Area (\$020 to \$3BF): 16 digits, \$020 through \$02F, in the data area are called memory registers (MR) and are accessible by LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for LIFO stacks to save the contents of the program counter (PC), status (ST) and carry (CA) when su-

broutine calls (CAL-instruction, CALL-instruction) and interrupts are serviced. This area can be used as a 16 nesting level stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by RTN and RTNI instructions. Status and carry are restored only by the RTNI instruction. This area, when not used for a stack, is available as a data area.

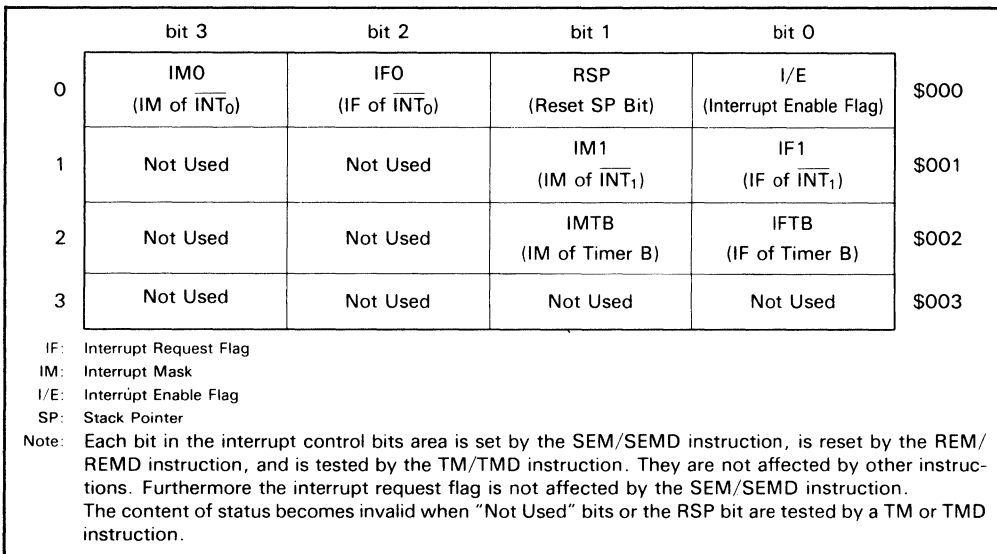


Figure 3. Interrupt Control Bit Area Configuration

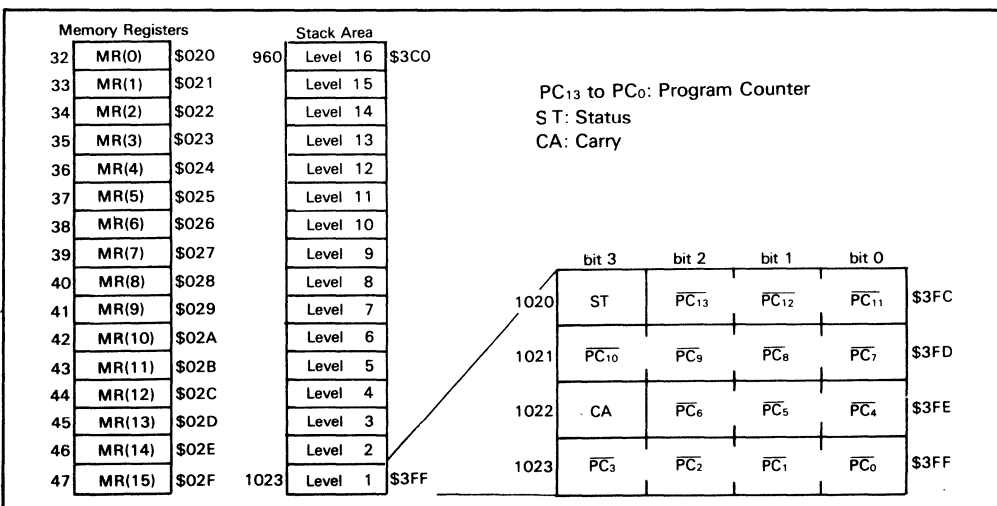


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Registers and Flags

The MCU has nine registers and two flags for CPU operations (figure 5).

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memories, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit, and the X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit registers SPX and SPY assist the X and Y registers respectively.

Carry (CA): The carry (CA) stores the overflow from ALU generated by an arithmetic operation. It is also affected by SEC, REC, ROTL and ROTR instructions.

During interrupt servicing, carry is pushed onto the stack. It is restored by a RTNI instruction, but not by a RTN instruction.

Status (ST): The status (ST) holds the ALU overflow, ALU non-zero, and the results of bit

test instruction for the arithmetic or compare instructions. It is a branch condition of the BR, BRL, CAL, or CALL instructions. The value of the status remains unchanged until the next arithmetic, compare, or bit test instruction is executed. Status becomes 1 after the BR, BRL, CAL, or CALL instruction whether it is executed or skipped. During interrupt servicing, status is pushed onto the stack and restored back from the stack by a RTNI instruction, but not by a RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

Stack Pointer (SP): The stack pointer (SP) is used to point to the address of the next stacking area (up to 16 levels).

The stack pointer is initialized to RAM address \$3FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is restored from it. The stack can only be used up to 16 levels deep because the upper 4 bits of the stack pointer are fixed at 1111.

The stack pointer is initialized to \$3FF by either MCU reset or the RSP bit reset by a REM/REMD instruction.

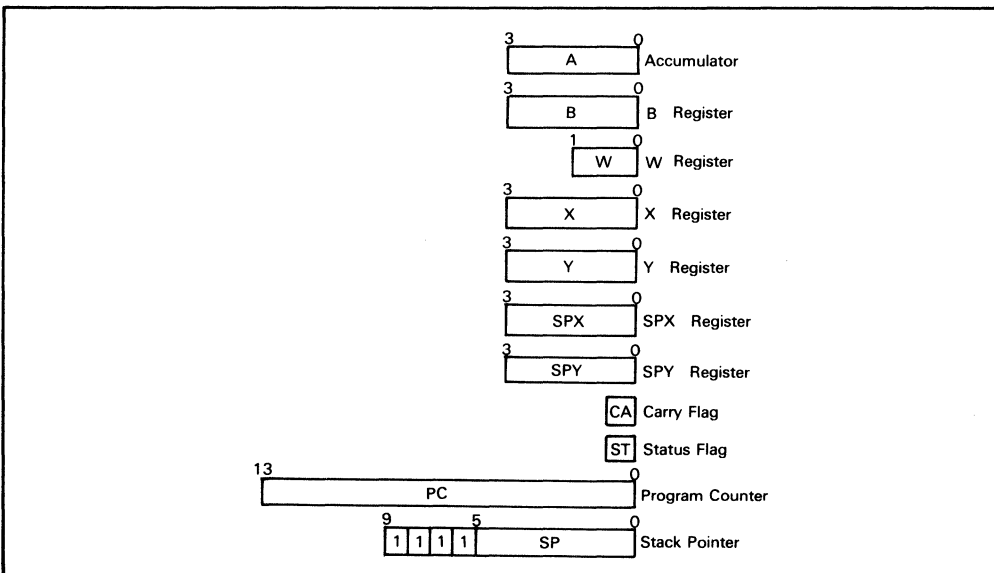


Figure 5. Registers and Flags



Interrupt

Three interrupt sources are available on the MCU: external requests (\overline{INT}_0 , \overline{INT}_1), and timer/counter (timer B). For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service: The interrupt control bits are

mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. (The interrupt request flag (IF) cannot be set by software.) The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 at initialization by MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2 shows the interrupt conditions corresponding to each interrupt source.

Table 1. Vector Addresses and Interrupt Priority

Reset, Interrupt	Priority	Vector addresses
RESET	-	\$0000
\overline{INT}_0	1	\$0002
\overline{INT}_1	2	\$0004
Timer B	3	\$0008

Table 2. Conditions of Interrupt Service

Interrupt Control Bit	\overline{INT}_0	\overline{INT}_1	Timer B
I/E	1	1	1
IF0· $\overline{IM0}$	1	0	0
IF1· $\overline{IM1}$	*	1	0
IFTB· \overline{IMTB}	*	*	1

Notes: Don't care

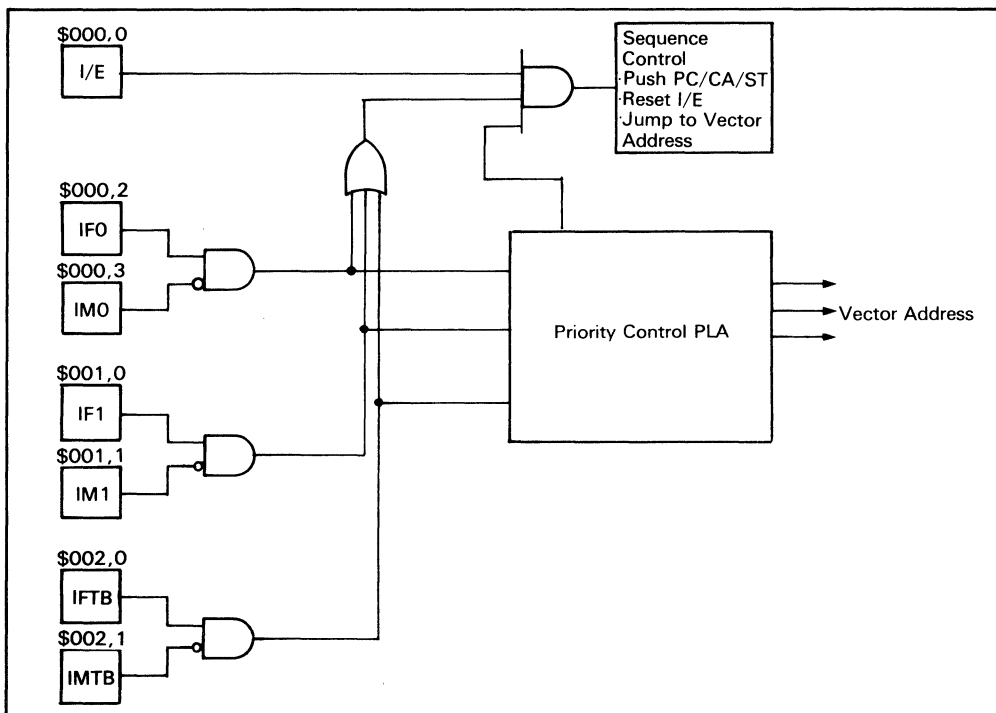


Figure 6. Interrupt Control Circuit Block Diagram



The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt service sequence, and figure 8 shows the interrupt service flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry, status, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed after the MCU jumps to the vector address.

In each vector address, program a JMWL instruction to branch to the starting address of the interrupt service program. The IF which caused the interrupt service must be reset by software in the interrupt service program.

Interrupt Enable Flag (I/E: \$000 bit 0): The interrupt enable flag enables/disables interrupt requests as shown in table 3. It is reset by interrupt servicing and set by the RTNI instruction.

External Interrupts (\overline{INT}_0 , \overline{INT}_1): The external interrupt request inputs (\overline{INT}_0 , \overline{INT}_1) can be selected by the port mode register

(PMR: \$004). Setting bit 3 and bit 2 of PMR causes $R3_3/\overline{INT}_1$ pin and $R3_2/\overline{INT}_0$ pin to be used as \overline{INT}_1 pin and \overline{INT}_0 pin respectively.

The external interrupt request flags (IF0, IF1) are set at the falling edge of \overline{INT}_0 and \overline{INT}_1 inputs. (Refer to table 4.)

The \overline{INT}_1 input can be used as a clock signal input to timer B. Then, timer B counts up at each falling edge of the \overline{INT}_1 input. When \overline{INT}_1 is used as timer B external event input, external interrupt mask (IM1) has to be set so that the interrupt request by \overline{INT}_1 will not be accepted. (Refer to table 5.)

External Interrupt Request Flags (IF0: \$000 bit 2, IF1: \$001 bit 0): The external interrupt request flags (IF0, IF1) are set at the falling edge of the \overline{INT}_0 , and \overline{INT}_1 inputs respectively.

External Interrupt Masks (IM0: \$000 bit 3, IM1: \$001 bit 1): The external interrupt masks mask the external interrupt requests.

Port Mode Register (PMR: \$004): The port mode register is a 4-bit write-only register which controls the $R3_2/\overline{INT}_0$ pin, and $R3_3/\overline{INT}_1$ pin as shown in table 6. The port mode register will be initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Table 3. Interrupt Enable Flag

Interrupt Enable Flag	Interrupt Enable/Disable
0	Disable
1	Enable

Table 4. External Interrupt Request Flag

Ex Int Req Flags	Interrupt Requests
0	No
1	Yes

Table 5. External Interrupt Mask

External Interrupt Masks	Interrupt Requests
0	Enable
1	Disable (masks)

Table 6. Port Mode Register

PMR3	$R3_3/\overline{INT}_1$ Pin
0	Used as $R3_3$ port input/output pin
1	Used as \overline{INT}_1 input pin

PMR2	$R3_2/\overline{INT}_0$ Pin
0	Used as $R3_2$ port input/output pin
1	Used as \overline{INT}_0 input pin



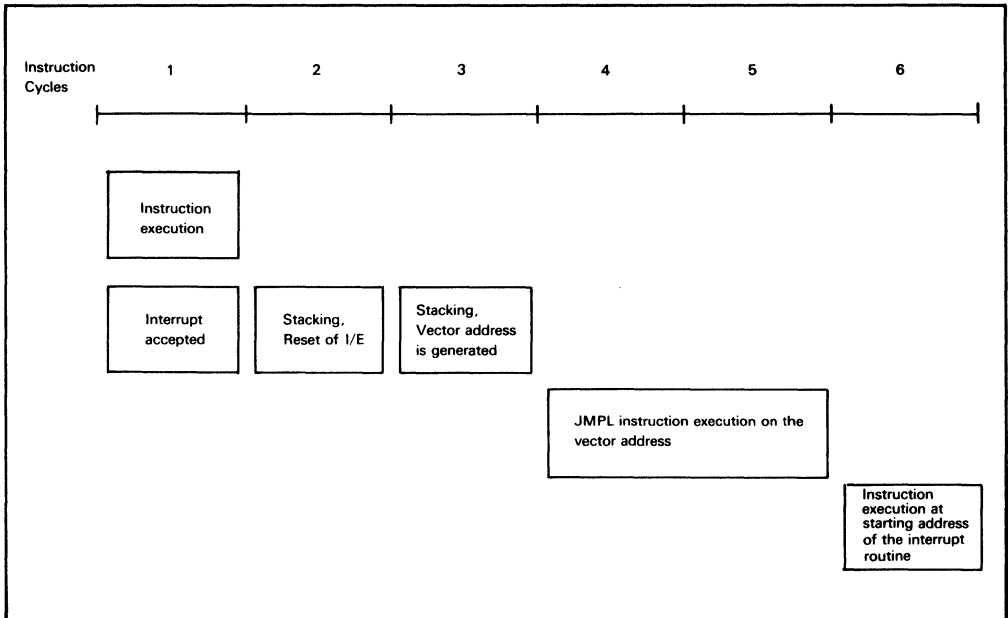


Figure 7. Interrupt Servicing Sequence

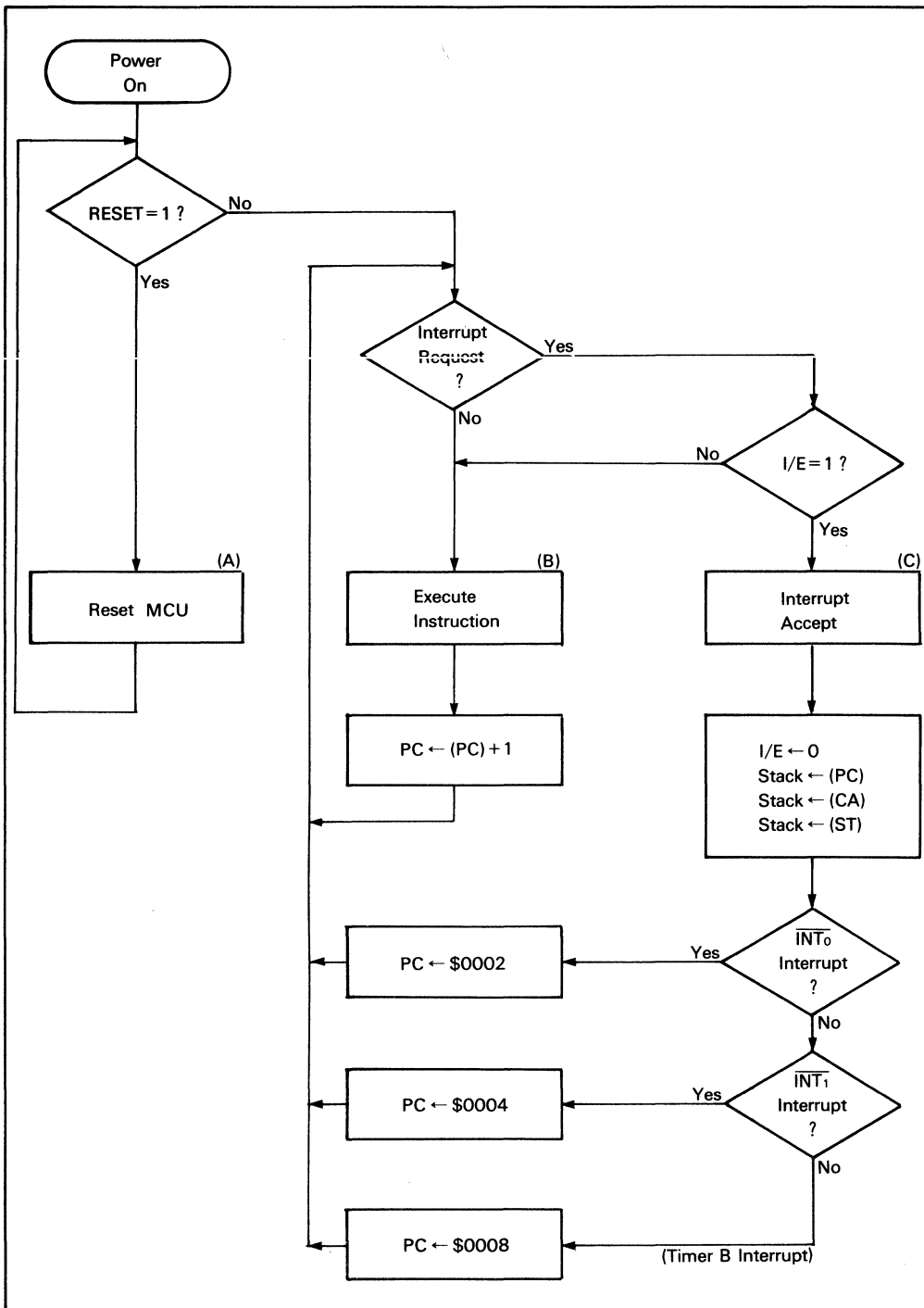


Figure 8. Interrupt Servicing Flowchart



Timer

The MCU contains a prescaler and a timer/counter (timer B, figure 9) whose functions are the same as HMCS404C's. The prescaler is an 11-bit binary counter, and timer B is an 8-bit auto-reload timer/ event counter.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset, and it starts to count up the system clock signal as soon as RESET input goes to logic 0. The prescaler keeps counting up except in MCU reset and stop mode. The prescaler provides clock signals to timer B. The prescaler divide ratio is selected by the timer mode register B (TMB).

Timer B Operation: The timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select R3₃/INT₁ as INT₁ and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to the data written into the timer load register by software. Timer B counts up at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected timer B is initialized according to the value of the timer load register. If it is not selected, timer B goes to \$00. The timer B interrupt request flag (IFTB: \$002 bit 0) will be set at this overflow output.

Timer Mode Register B (TMB: \$009): The timer mode register B (TMB) is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in table 7. The timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after the timer mode register B is written to. Initialization of timer B by writing data into the timer load register should be performed after the contents of TMB are changed. Configuration and function of timer mode register B is shown in figure 10.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B). (Refer to figure 2.)

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by the MCU reset.

The counter value of timer B can be obtained by reading the timer/event counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

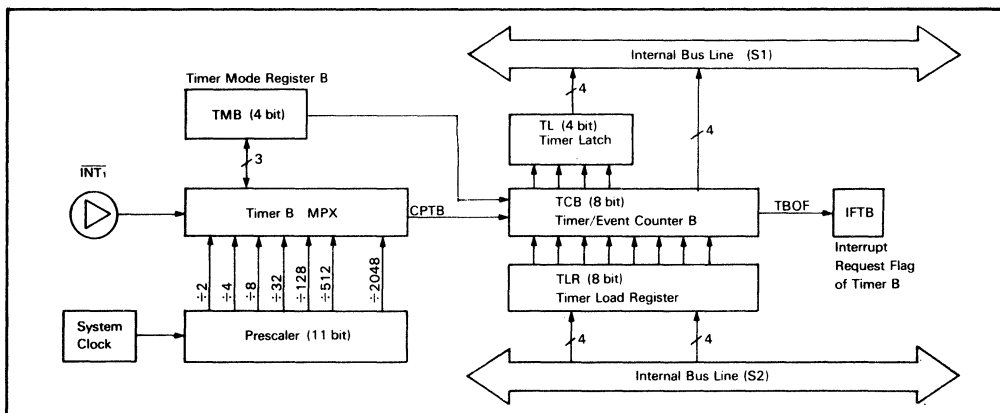


Figure 9. Timer Block Diagram



Timer B Interrupt Request Flag (IFTB: \$002 bit 0): The timer B interrupt request flag is set by the overflow output of timer B (table 8).

Timer B Interrupt Mask (IMTB: \$002 bit 1): The timer B interrupt mask prevents an interrupt request from being generated by timer B Interrupt request flag (table 9).

Table 7. Timer Mode Register B

TMB3	Auto-reload Function
0	No
1	Yes

TMB2	TMB1	TMB0	Prescaler Divide Ratio, Clock Input Source
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	\overline{INT}_1 (External Event Input)

Table 8. Timer B Interrupt Request Flag

Timer B Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Table 9. Timer B Interrupt Mask

Timer B Interrupt Mask	Interrupt Request
0	Enable
1	Disable (Mask)

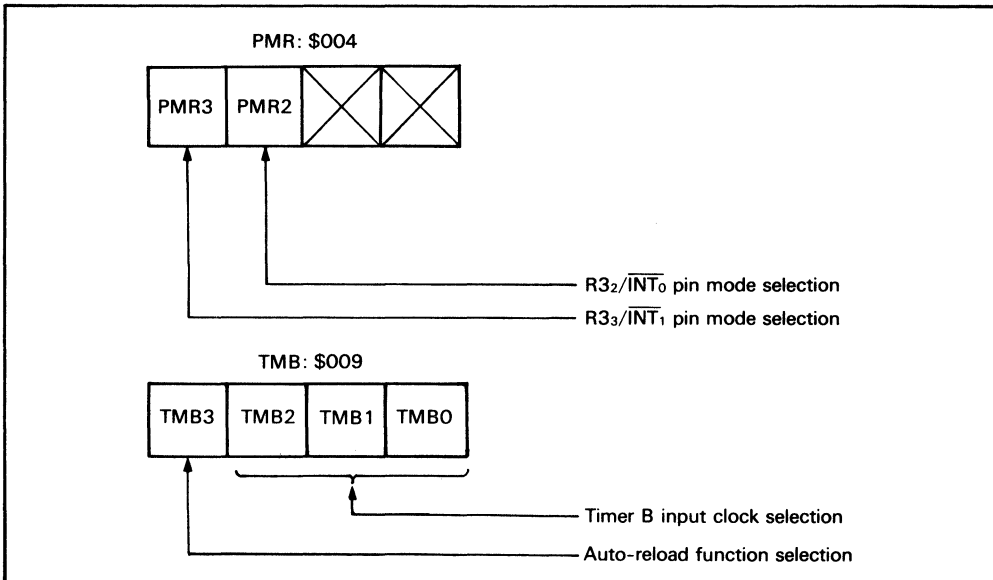


Figure 10. Mode Register Configuration and Function

Input/Output

The MCU has 35 I/O pins, 8 standard and 27 high voltage. The R1 and R2 port are high voltage pin.

When any input/output pin is used as an input pin, the mask option and output data must be selected as follows : when inputting, the Input Pin State should be high.

D Port: The D I/O port has 15 discrete I/O pins, each of which can be addressed independently. It can be set/reset through SED/RED and SEDD/REDD instructions, and can be tested through TD and TDD instructions. See table 10 for the I/O pin circuit types.

R Ports: The six R ports are composed of 16 I/O pins, 4 output-only pins. Data is input through LAR and LBR instructions and output through LRA and LRB instructions. The MCU is not be affected when the input-only and/or non-existing ports are written into, while invalid data will be read from the output-only and/or non-existing ports.

The R₃₂ and R₃₃ pins are multiplexed with

the $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ pins respectively. See table 10 for the selectable circuit types for these I/O pins.

Unused I/O Pins: If unused I/O pins are left floating, the LSI may malfunction because of noise. The I/O pins should be fixed as follows to prevent the malfunction.

High-voltage: select "without pull-up MOS" (NMOS open drain) via mask option and connect to V_{CC} on the printed circuit board.

Standard: select "without pull-up MOS" (NMOS open drain) via mask option and connect to GND on the printed circuit board.

Reset

Bringing the RESET pin high resets the MCU. At power-on, or when stop mode, is can called the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instructions cycles are required for the MCU to be reset.

Table 11 shows the parts initialized by MCU reset, and the status of each.

Table 10. I/O Pin Circuit Types

	Without Pull-Up MOS (NMOS Open Drain) (A)	Applicable Pins
I/O Common Pins		D ₀ –D ₁₄ R ₃₀ –R ₃₃ R ₄₀ –R ₄₃
High Current	Not available	
High Voltage	Available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	Applicable Pins
I/O Common Pins		R ₁₀ –R ₁₃ R ₂₀ –R ₂₃
High Current	Available	
High Voltage	Not available	

	Without Pull-Up MOS (NMOS Open Drain) (A)	Applicable Pins
Output Pins		R ₀₀ –R ₀₃
High Current	Not available	
High Voltage	Available	

Table 11. Initial Value After MCU Reset

Items	Initial Value by MCU Reset	Contents	
Program Counter (PC)	\$0000	Execute program from the top of ROM address	
Status (ST)	1	Enable branch with conditional branch instructions	
Stack Pointer (SP)	\$3FF	Stack level is 0	
I/O Pin Output Register	(A) Without Pull-Up MOS	1	Enable input
	(B) With Pull-Up MOS	1	Enable input
	(C) CMOS	1	—
Interrupt Flag	Interrupt Enable Flag (I/E)	0	Inhibit all interrupts
	Interrupt Request Flag (IF)	0	No interrupt request
	Interrupt Mask (IM)	1	Mask interrupt request
Mode Register	Port Mode Register (PMR)	0000	See port mode register
	Timer Mode Register B (TMB)	0000	See timer mode register B
Timer/Counter	Prescaler	\$000	—
	Timer/Event Counter B (TCB)	\$00	—
	Timer Load Register (TLR)	\$00	—

Note: MCU reset affects the rest of registers as follows:

Item	After Recovering from Stop Mode by MCU Reset	After MCU Reset (Non-Stop-Mode)
Carry (CA)	The contents of the items before MCU reset are not retained.	The contents of the items before MCU reset are not retained.
Accumulator (A)	It is necessary to initialize them by software.	It is necessary to initialize them by software.
B Register (B)		
W Register (W)		
X/SPX Registers (X/SPX)		
Y/SPY Registers (Y/SPY)		
RAM	The contents of RAM before MCU reset (just before STOP instruction) are retained.	

Internal Oscillator Circuit

Figure 11 outlines the internal oscillator circuit. In addition, see figure 12 for the layout of

the ceramic filter. In this cases, external clock operation is available.

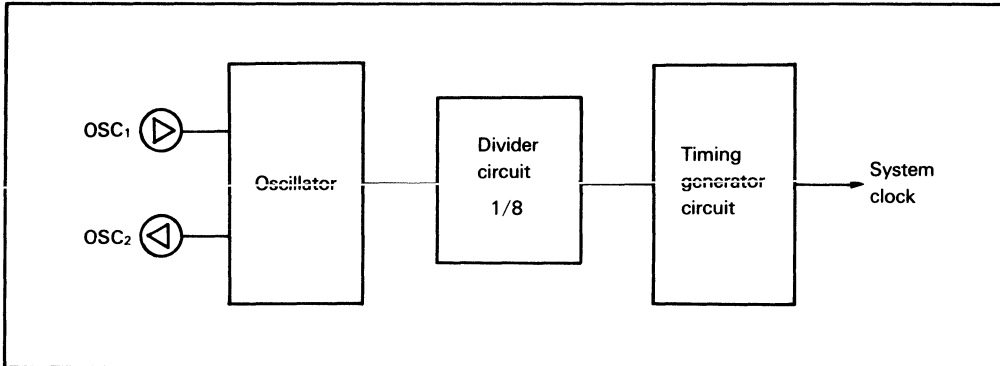


Figure 11. Internal Oscillator Circuit

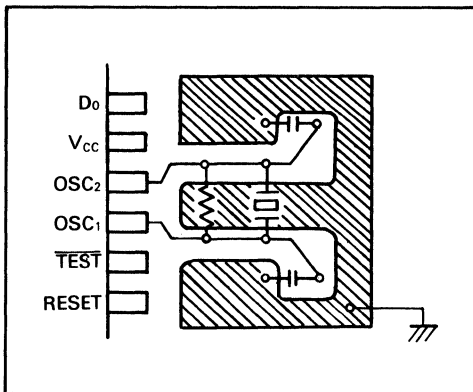
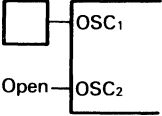
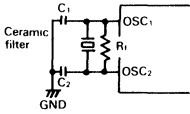


Figure 12. Layout of Ceramic Filter

Table 12. Examples of Oscillator Circuits

	Circuit Configuration	Circuit Constants
<p>External Clock Operation</p>	<p>Oscillator</p> 	
<p>Ceramic Filter Oscillator</p>		<p>Ceramic filter CSA 8.00MT (Murata)</p> <p>R_f: 1 MΩ \pm 20% C_1: 30 pF \pm 20% C_2: 30 pF \pm 20%</p>

- Notes: 1. For the ceramic filter resonator, the upper circuit parameters are recommended by the ceramic filter maker. Ceramic filter resonator, and the floating capacitance change circuit parameters in designing the board. In designing the resonator, please consult with the engineers of the ceramic filter maker to determine the circuit parameters.
2. Wiring between OSC₁, OSC₂, and elements should be as short as possible, and never cross other wires. Refer to the layout of ceramic filter (figure 12).

Operating Modes

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode and stop mode (table 13). Figure 13 is a mode transition diagram for these modes.

Standby Mode: Executing an SBY instruc-

tion puts the MCU into standby mode. In standby mode, the oscillator circuit is active and interrupts and timer/counter working. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

Table 13. Low Power Dissipation Mode

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Register, flag	Retained	Reset (note 1)
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained (note 2)	High impedance
Timer/counter	Active	Stopped
Recovery method	RESET input, interrupt request	RESET input

- Notes: 1. The MCU recovers from stop mode by RESET input. Refer to table 11 for the contents of flags and registers.
 2. As I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

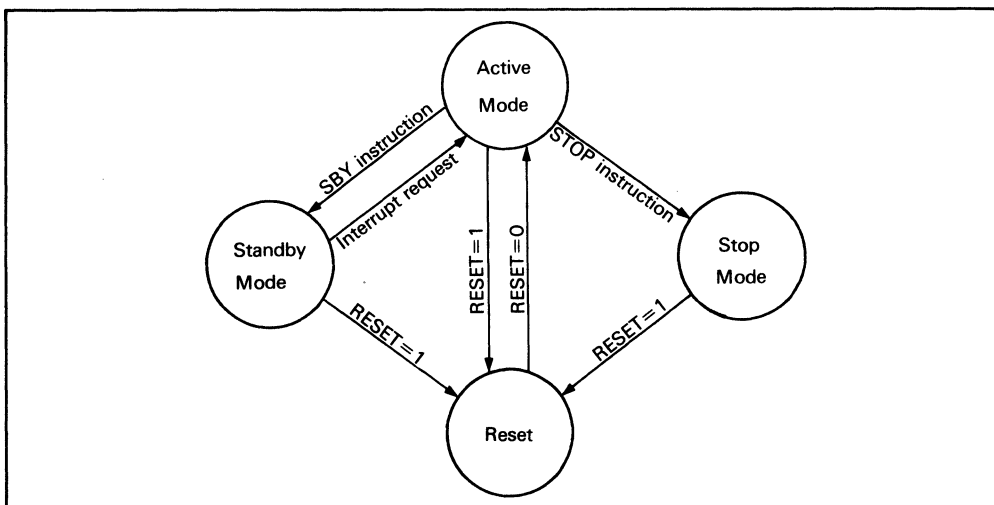


Figure 13. MCU Operation Mode Transition



Standby mode may be cancelled by inputting RESET or by asserting an interrupt request. In the former case the MCU is reset. If the interrupt enable flag is 1 at this time, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues. In the later case, the MCU becomes active and executes the next instruction following the SBY instruction.

Figure 14 shows the flowchart of the standby mode.

Stop Mode: Executing a STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

Stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 15, reset input must be applied at least to t_{RC} for oscillation to stabilize. (Refer to AC Characteristics table.) After stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, Y/SPY registers, and carry may not retain their contents.

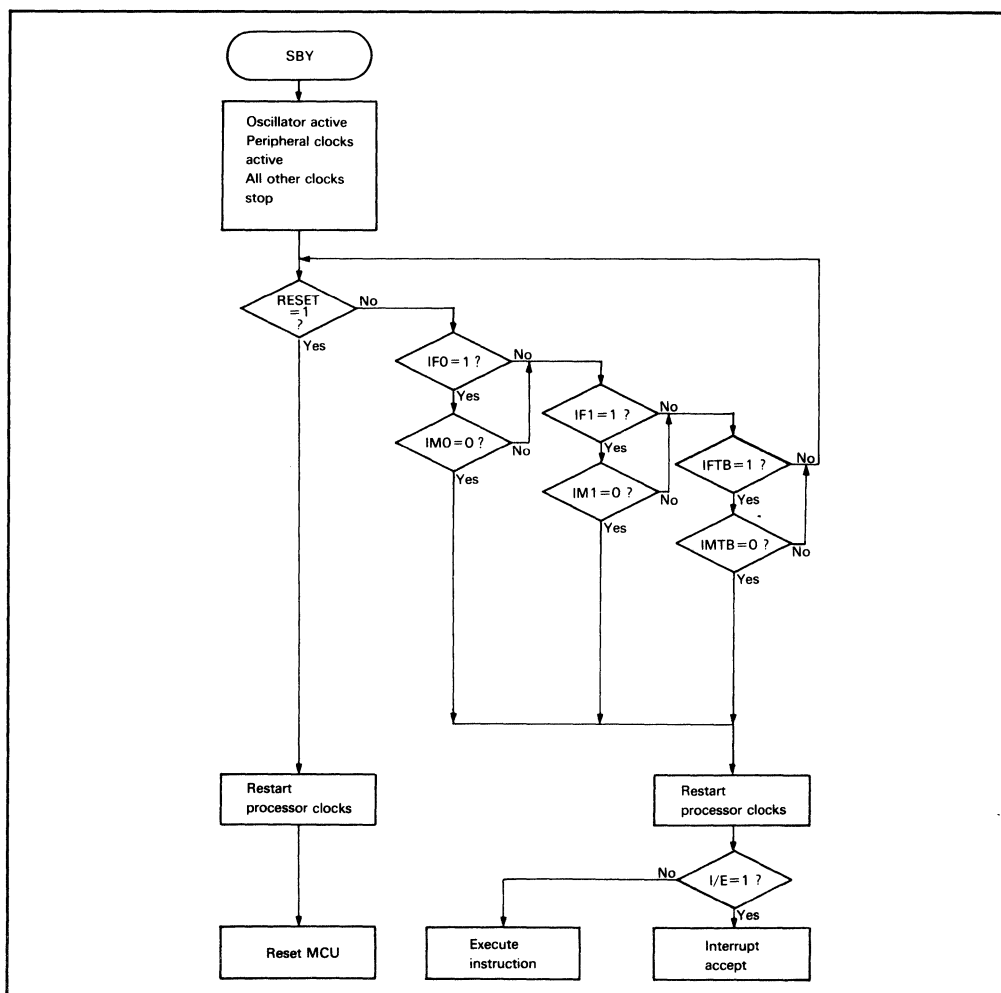


Figure 14. MCU Standby Mode Operation Flowchart



RAM Addressing Mode

As shown in figure 16, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 digits from \$020 to \$02F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 17.

Direct addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with 14-bit immediate data.

Current Page Addressing Mode: The ROM memory space is divided into pages, with 256 words in each page. Page zero begins at address \$0000. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR is on a page boundary (256n + 255) (figure 18), executing a BR instruction transfers the PC contents to the next page because of the hardware architecture. Consequently, the program branches to the next page when the BR is used on a page boundary. The HMCS400 series cross macro assembler has an automatic paging facility for ROM pages.

Zero Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order eight bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referred to by a P instruction (figure 19). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output register. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register and also to the R1 and R2 port output register at the same time.

The P instruction has no effect on the program counter.

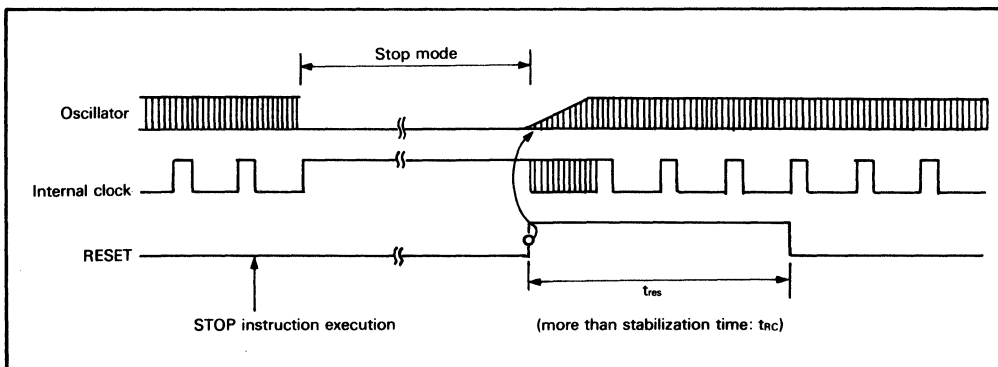


Figure 15. Timing Chart of Recovering from Stop Mode



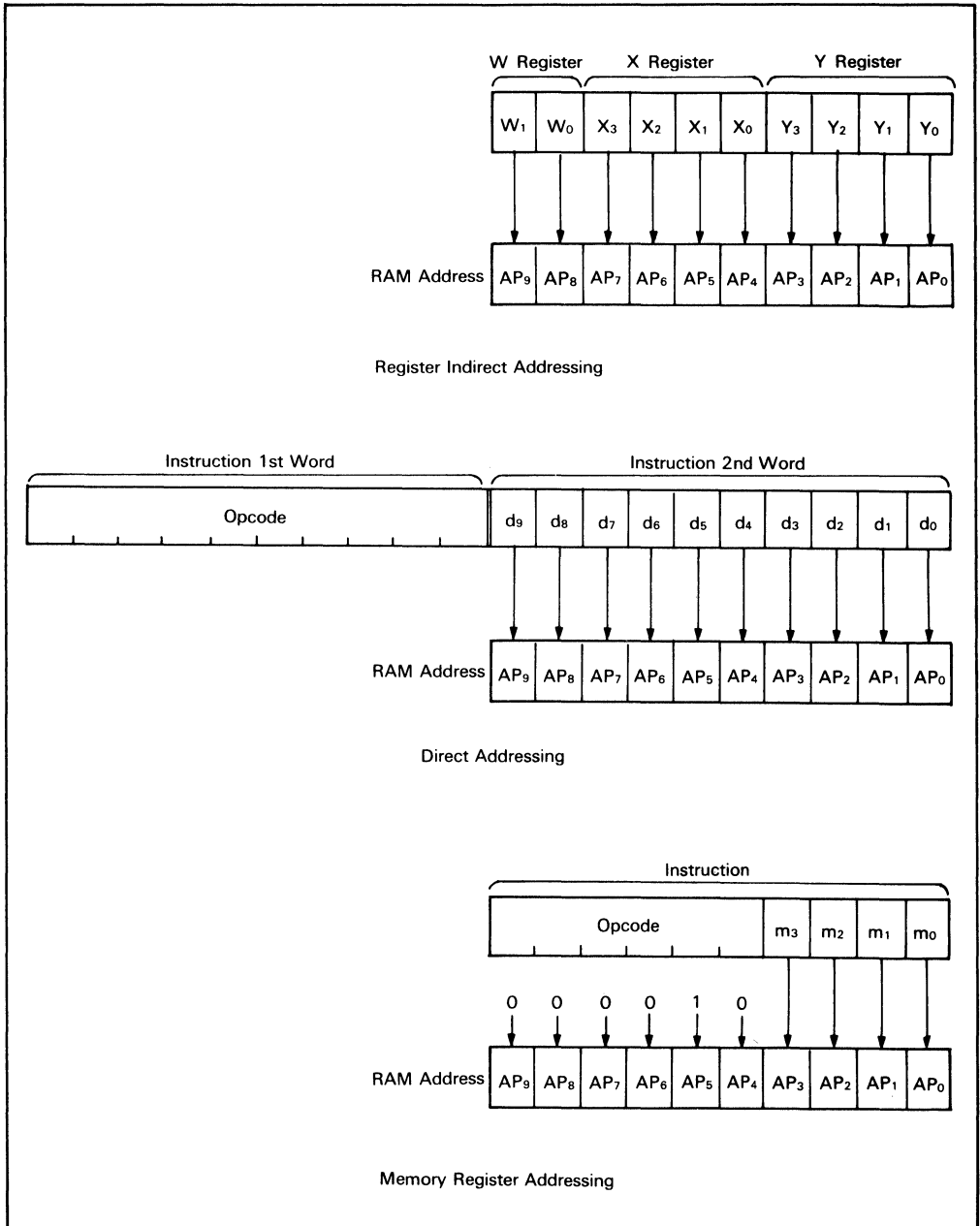


Figure 16. RAM Addressing Mode

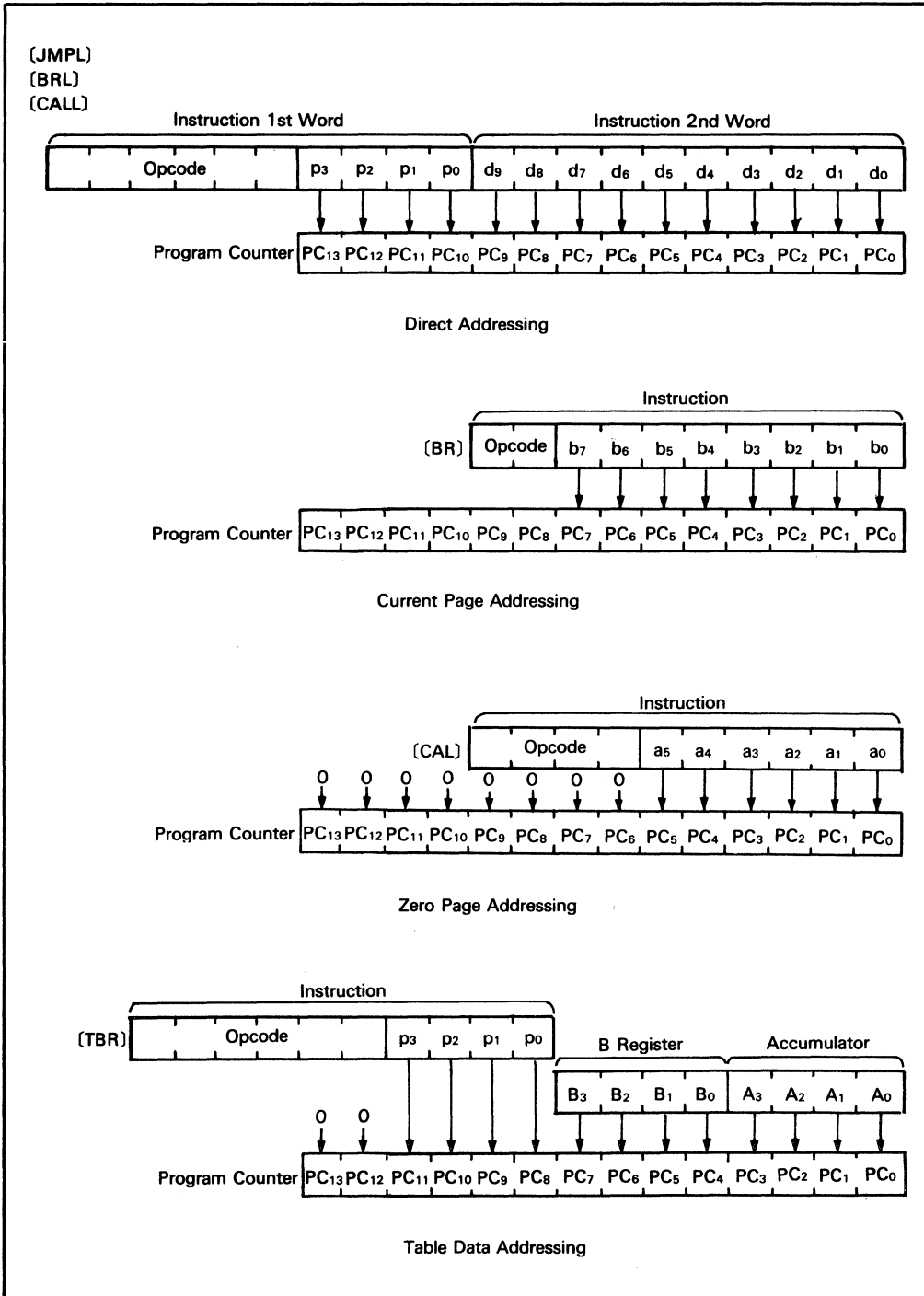


Figure 17. ROM Addressing Mode



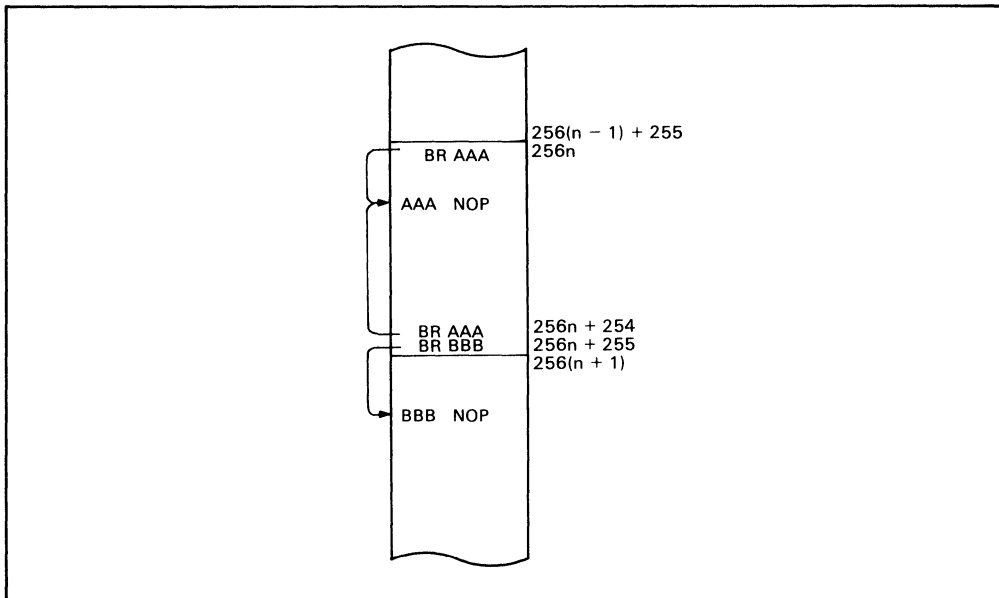


Figure 18. BR Instruction Branch Destination on Page Boundary

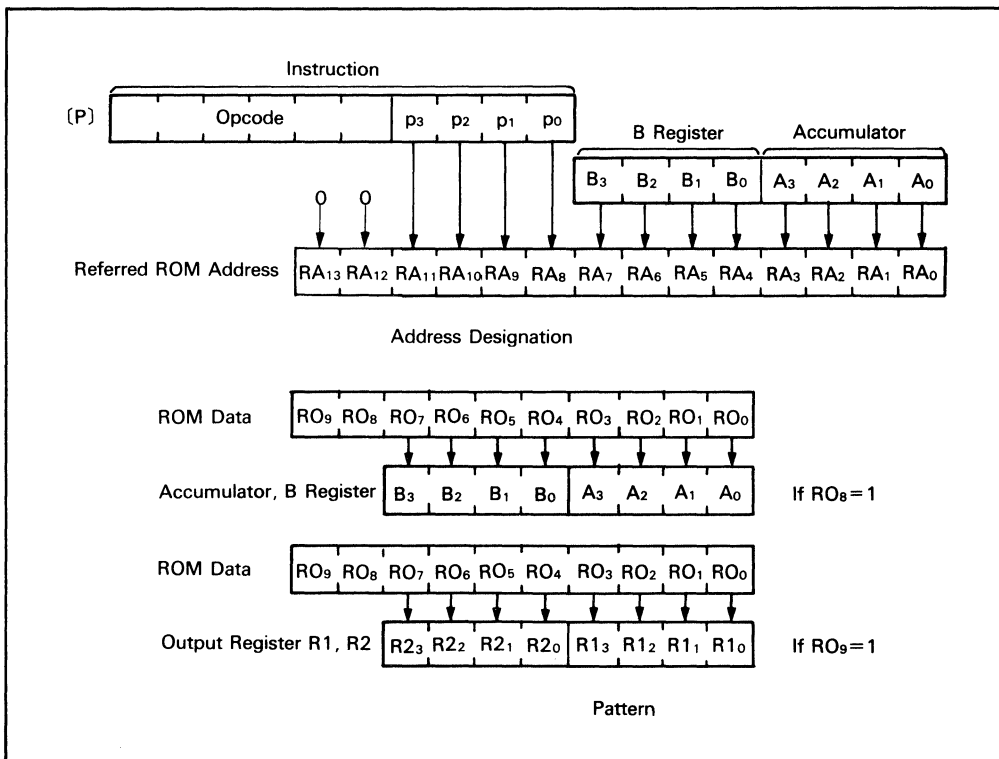


Figure 19. P Instruction

HD40P4919

Instruction Set

The HD404919 provides 100 instructions which are classified into 10 groups as follows;

1. Immediate instruction
2. Register-to-register instruction
3. RAM address instruction
4. RAM register instruction
5. Arithmetic instruction
6. Compare instruction
7. RAM bit manipulation instruction
8. ROM address instruction
9. Input/output instruction
10. Control instruction

Tables 14-23 list their functions, and table 24 is an opcode map.

Table 14. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i → A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i → B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i → M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i → M, Y+1 → Y	NZ	1/1

Table 15. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B → A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A → B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W → A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y → A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX → A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY → A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) → A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ↔ A		1/1

Note :An operand is provided for the second word of LAW and LWA instruction by the assembler automatically.



Table 16. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 i ₁ i ₀	i → W		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i → X		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀	i → Y		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A → W		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	A → X		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	A → Y		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	Y+1 → Y	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	Y-1 → Y	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	Y+A → Y	OVF	1/1
Subtract A from Y	SYX	0 0 1 1 0 1 0 1 0 0	Y-A → Y	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	X ↔ SPX		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	Y ↔ SPY		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	X ↔ SPX, Y ↔ SPY		1/1

Note: An operand is provided for the second word of LAW and LWA instruction by assembler automatically.

Table 17. RAM Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A → M, (X → SPX, Y → SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A → M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 x	A → M, Y + 1 → Y (X → SPX)	NZ	i/i
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 x	A → M, Y - 1 → Y (X → SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M → A, (X → SPX, Y → SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M → A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M → B, (X → SPX, Y → SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes each (example of LAM (XY) is given, below).

Mnemonic	y	x	Function
LAM	0	0	
LAMX	0	1	X → SPX
LAMY	1	0	Y → SPY
LAMXY	1	1	X → SPX, Y → SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes each (example of LMAIY (X) is given below).

Mnemonic	x	Function
LMAIY	0	
LMAIYX	1	X → SPX

Table 18. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A+i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B+1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B-1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A}+1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M+A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M+A+CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M-A-\bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR

Table 19. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀	i ≠ M	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≠ M	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	A ≠ M	NZ	1/1
A Not Equal to Memory	AMEMD d	0 1 0 0 0 0 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≠ M	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	B ≠ M	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i ₃ i ₂ i ₁ i ₀	Y ≠ i	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i ≤ M	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i ≤ M	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	A ≤ M	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ≤ M	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	B ≤ M	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i ₃ i ₂ i ₁ i ₀	A ≤ i	NB	1/1

Table 20. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n ₁ n ₀	1 → M(n)		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	1 → M(n)		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n ₁ n ₀	0 → M(n)		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	0 → M(n)		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n ₁ n ₀		M(n)	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n ₁ n ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		M(n)	2/2

Table 21. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 -I/E CA Restore	ST	1/3

Table 22. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direc	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 · D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 · D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 · D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) · A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) · B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A · R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B · R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 23. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1

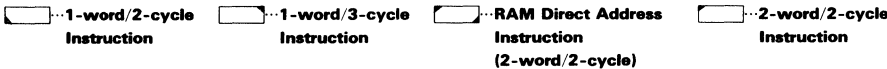
Note: HD404919 has no serial interface, so STS (start serial) operates the same as NOP.



HD40P4919

Table 24. Opcode Map

		0																1																																							
R8																																																									
R9	LH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																								
	0	NOP	XSP	XSPY	XSPAN	XY	EM			AM				ORM			LAW				ANEMD			AMD				ORMD																													
	1	RTN	RTNI			ALEM				AMC				EDRM			LWA				ALEM			AMCD				EDRMD																													
	2	INEM								i(4)								INEMD								i(4)																															
	3	ILEM								i(4)								ILEMD								i(4)																															
	4	LBM(XY)			ENEM				LAB					IB			COMB				OR							SBYSTOP																													
	5	LMAY(X)				AYY				LASY				IY			JMPL																p(4)																								
	6	NEGA				RED				LSPX						TC	CALL																p(4)																								
0	7	VNE!								i(4)								BRL								p(4)																															
	8	XMA(XY)				SEM	n(2)				REM	n(2)				TM	n(2)				XMAD				SEMD	n(2)				REMD	n(2)				TMD	n(2)																					
	9	LAM(XY)				LMA(XY)			SMC					ANM			LAMC				LMAD				SMCD				ANMD																												
	A	ROTR	ROTL					DAA					DAS			LAY	LMID																i(4)																								
	B	TBR																p(4)																P																p(4)							
	C	XMB(XY)				BLEM				LBA						DB	CAL																a(6)																								
	D	LMADY(X)				SY				LYA					DY																																										
	E	TD				SED				LXA				REC	SEC																																										
	F	LWI								i(2)																																															
1	0	LBI								i(4)																																															
	1	LYI								i(4)																																															
	2	LXI								i(4)																																															
	3	LAI								i(4)																																															
	4	LBR								m(4)																																															
	5	LAR								m(4)																																															
	6	REDD								m(4)																																															
	7	LAMR								m(4)								BR								b(8)																															
	8	AI								i(4)																																															
	9	LMIIY								i(4)																																															
	A	TDD								m(4)																																															
B	ALEI								i(4)																																																
C	LRB								m(4)																																																
D	LRA								m(4)																																																
E	SEDD								m(4)																																																
F	XMRA								m(4)																																																



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		-0.3 to + 15	V	4
Total Allowance of Input Current	ΣI_o	200	mA	5
Maximum Input Current	I_o	15	mA	7, 8
		35	mA	7, 10
Maximum Output Current	$-I_o$	4	mA	8, 9
Total Allowance of Output Current	$-\Sigma I_o$	50	mA	6
Operating Temperature	T_{opr}	-20 to + 75	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	

- Notes: 1. Permanent damage may occur if Absolute Maximum Ratings are exceeded. Normal operation should be under the conditions of Electrical Characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
2. All voltages are with respect to GND.
 3. Standard pins.
 4. High-voltage pins.
 5. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 6. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 8. $D_0 - D_{14}$, $R_3 - R_4$, R_0
 9. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 10. $R_1 - R_2$.

HD40P4919

Electrical Characteristics

DC Characteristics

($V_{CC} = 4\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET,	$0.85 V_{CC}$		$V_{CC} + 0.3$	V		
		$\overline{INT_0}$, INT ₁	$0.8 V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}	RESET,	- 0.3		$0.15 V_{CC}$	V		
		$\overline{INT_0}$, INT ₁	- 0.3		$0.2 V_{CC}$	V		
		OSC ₁	- 0.3		0.5	V		
Input/Output Leakage Current	$ I_{IL} $	RESET, $\overline{INT_0}$, INT ₁ , OSC ₁			1	μA	$V_{in} = 0\text{ V to }V_{CC}$	1
Current Dissipation in Active Mode	I_{CC}	V_{CC}			5	mA	$V_{CC} = 5\text{ V}$; $f_{osc} = 8\text{ MHz, } \div 8$	2,5
Current Dissipation in Standby Mode	I_{SBY}	V_{CC}			2.6	mA	$V_{CC} = 5\text{ V}$; $f_{osc} = 8\text{ MHz, } \div 8$	3,5
Current Dissipation in Stop Mode	I_{stop}	V_{CC}			10	μA	$V_{in}(\overline{TEST}) = V_{CC} - 0.3\text{ V to }V_{CC}$; V_{CC} ; $V_{in}(\text{RESET}) = 0\text{ V to }0.3\text{ V}$	4
Stop Mode Retain Voltage	V_{stop}	V_{CC}	2			V		

- Notes: 1. Output buffer current are excluded.
 2. The MCU is in the reset state. Input/output current does not flow.
 • MCU in reset state, operation mode
 • RESET, TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 3. The timer/counter operates with the fastest clock. Input/output current does not flow.
 • MCU in standby mode
 • Input/output in reset state
 • RESET: GND
 • TEST: V_{CC}
 • D₀-D₁₄, R₀-R₄: V_{CC} voltage
 4. Excluding pull-up MOS current.
 5. When $f_{osc} = x\text{ MHz}$, estimate the current dissipation as follows:
 Max value @ $x\text{ MHz} = x/4 \times (\text{max value @ }4\text{ MHz})$



Input/Output Characteristics for Standard Use

($V_{CC}=4V$ to $6V$, $GND=0V$, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	R1-R2	$0.7V_{CC}$		$V_{CC} + 0.3$	V		
		D ₀ -D ₁₄ R3-R4						
Input Low Voltage	V_{IL}	R1-R2	-0.3		$0.3V_{CC}$	V		
		D ₀ -D ₁₄ R3-R4						
Output High Voltage	V_{OH}	D ₀ -D ₁₄ R3-R4, RO	$V_{CC} - 1.0$			V	$- I_{OH} = 1.0$ mA	
		D ₀ -D ₁₄ , R3-R4, RO	$V_{CC} - 0.5$			V	$- I_{OH} = 0.5$ mA	
Output Low Voltage	V_{OL}	D ₀ -D ₁₄ , R3-R4, RO			0.4	V	$I_{OL} = 1.6$ mA	
		R1-R2			1.2	V	$V_{CC} = 5$ V, $I_{OL} = 25$ mA	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₁₄ , R3-R4, RO			1	μA	$V_{in} = 0$ V to V_{CC}	1
		R1-R2			20			

Note: 1. Output buffer current are excluded.

Input/Output Characteristics for High Voltage Use

($V_{CC} = 4$ V to 6 V, $GND = 0$ V, $T_a = -20^{\circ}C$ to $+75^{\circ}C$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Input High Voltage	V_{IH}	D ₀ -D ₁₄ , R3-R4	$0.7V_{CC}$		12	V		
Input Low Voltage	V_{IL}	D ₀ -D ₁₄ , R3-R4	-0.3		$0.3 V_{CC}$	V		
Output High Voltage	V_{OH}	D ₀ -D ₁₄ , R3-R4, RO	11.5			V	500 k Ω to 12V	
Output Low Voltage	V_{OL}	D ₀ -D ₁₄ , R3-R4, RO			0.4	V	$I_{OL} = 1.6$ mA	
Input/Output Leakage Current	$ I_{IL} $	D ₀ -D ₁₄ , R3-R4, RO			1	μA	$V_{in} = 0$ V to V_{CC}	1

Note: 1. Output buffer current are excluded.



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AC Characteristics

($V_{CC} = 4\text{ V to }6\text{ V}$, $GND = 0\text{ V}$, $T_a = -20^\circ\text{C to }+75^\circ\text{C}$)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Conditions	Note
Oscillation Frequency	f_{osc}	OSC1, OSC2	0.4	8	9	MHz	Divide by 8	
Instruction Cycle Time	t_{cyc}		0.89	1	20	μs		
Oscillator Stabilization Time	t_{RC}	OSC1, OSC2			20	ms		1
External clock Frequency	f_{cp}	OSC1	0.4	8	9	MHz		2
External Clock High, Low Level Width	t_{CPH} , t_{CPL}	OSC1	41			ns	Divide by 8	2
External Clock Rise Time	t_{CPr}	OSC1			15	ns		2
External Clock Fall Time	t_{CPf}	OSC1			15	ns		2
Instruction cycle Time	t_{cyc}		0.89	1	20	μs		2
\overline{INT}_0 High Level Width	t_{i0H}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_0 Low Level Width	t_{i0L}	\overline{INT}_0	2			t_{cyc}		3
\overline{INT}_1 High Level Width	t_{i1H}	\overline{INT}_1	2			t_{cyc}		3
\overline{INT}_1 Low Level Width	t_{i1L}	\overline{INT}_1	2			t_{cyc}		3
RESET High Level Width	t_{RSTH}	RESET	2			t_{cyc}		4
Input Capacitance	C_{in}	All pins			15	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$	
RESET Fall Time	t_{RSTf}				20	ms		4

Notes: 1. Oscillator stabilization time is the time until the oscillator stabilizes after V_{CC} reaches its minimum allowable voltage 4 V after power-on, or after RESET goes high. At power-on or stop mode release, RESET must be kept high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, please get the manufacturer's advice when designing the RESET circuit. (See figure 20.)

2. See figure 21.
3. See figure 22.
4. See figure 23.



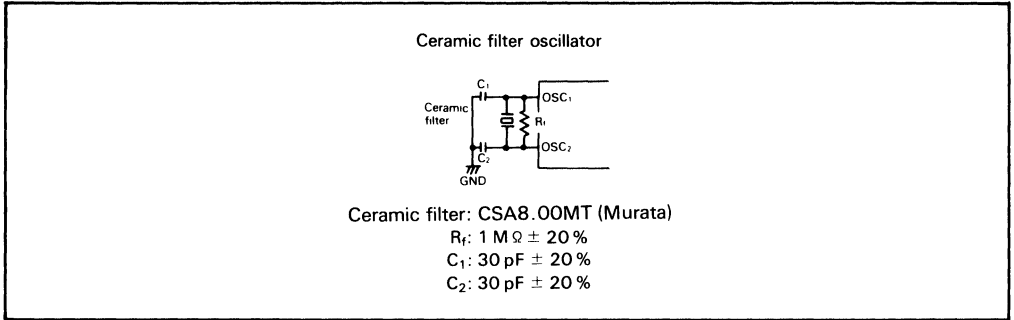


Figure 20. Oscillator Circuit

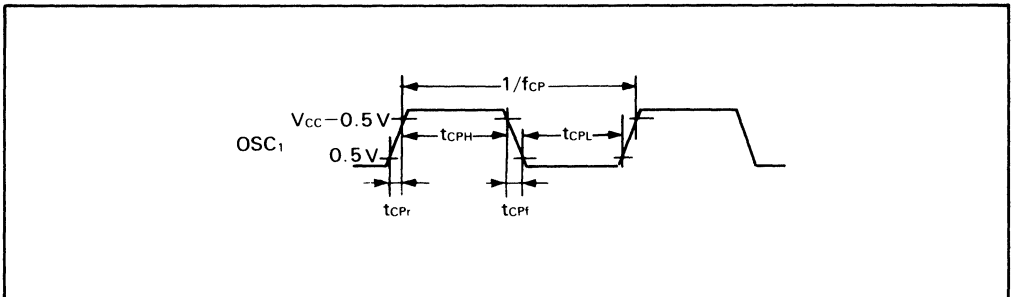


Figure 21. Oscillator Timing

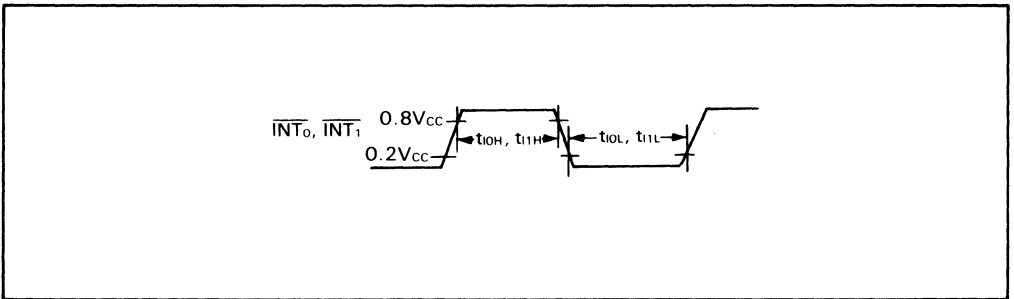


Figure 22. Interrupt Timing

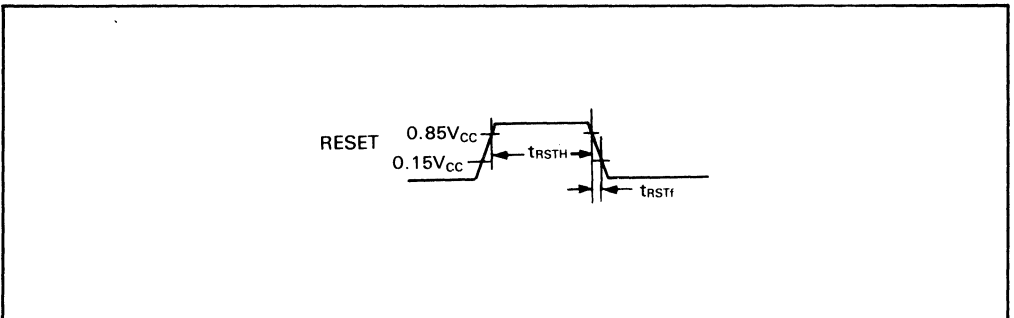


Figure 23. Reset Timing

Precautions on using EPROM on Package Type Microcomputer

Since the HD40P4919 has a special structure with pin sockets installed on the surface of the package, the following should be noted when using it.

- (1) Do not apply an electrostatic voltage or surge voltage more than the maximum ratings to the pin socket pins. This may destroy the LSI permanently.
- (2) When installing this LSI in system products in the same way as the mask ROM 4-bit single chip microcomputer, observe the following in order to maintain good ohmic contact between EPROM pins and pin sockets.
 - (a) When soldering the LSI on a printed circuit board, keep pin conditions under 250°C within 10 seconds. If these conditions are exceeded, the solder fixing the pin sockets may melt and the pins may fall out.
 - (b) Keep out detergent or coater from the pin sockets during flux removal or board coating. Flux or coater may decrease pin socket contactivity.
 - (c) Avoid permanent use of this LSI in places with excessive vibration.
 - (d) Since repeated insertion/removal of EPROMs may decrease pin sockets' contactivity, it is recommended to use new ones for your system products.

LCD-III
(HD44790,HD44795)



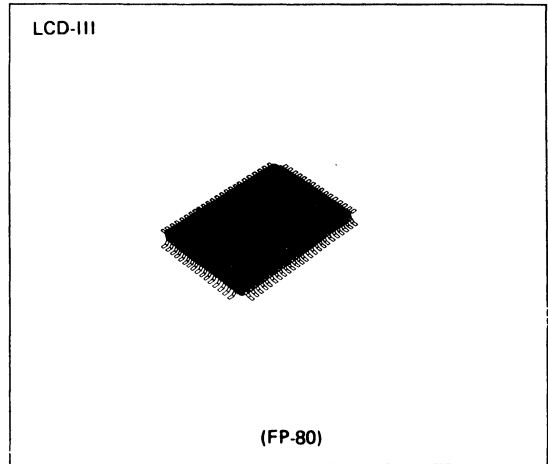
LCD— III (HD44790, HD44795)

DESCRIPTION

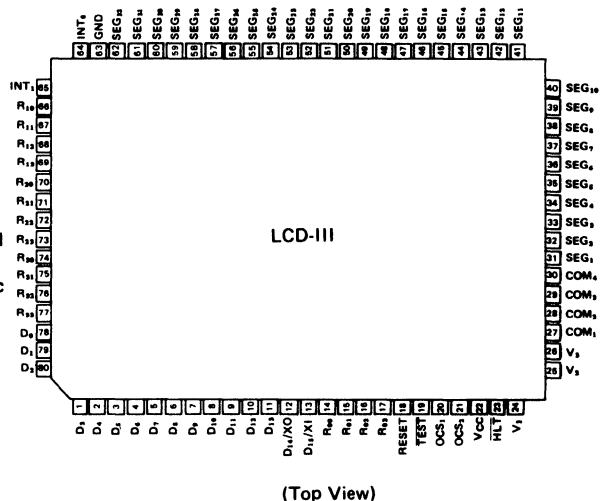
The LCD-III is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-III is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-III provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.

FEATURES

- 4-bit Architecture
- 2,048 Words of Program ROM (10 bits/Word)
128 Words of Pattern ROM (10 bits/Word)
- 160 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
4 Commons (Duty Radio; Static, 1/2, 1/3, 1/4)
32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100s)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
— Table Look Up Capability —
- Powerful Interrupt Function
3 Interrupt Sources
├ 2 External Interrupt Lines
└ Timer/Event Counter
Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Built-in Power-on Reset Circuit
- Low Operating Power Dissipation; 2mW typ.
- Stand-by Mode (Halt Mode); 50μW max.
- 2 Versions; HD44790 VCC = 5V ± 10%, 10 μs Instruction Cycle Time
HD44795 VCC = 2.7V to 5.5V, 20 μs Instruction Cycle Time

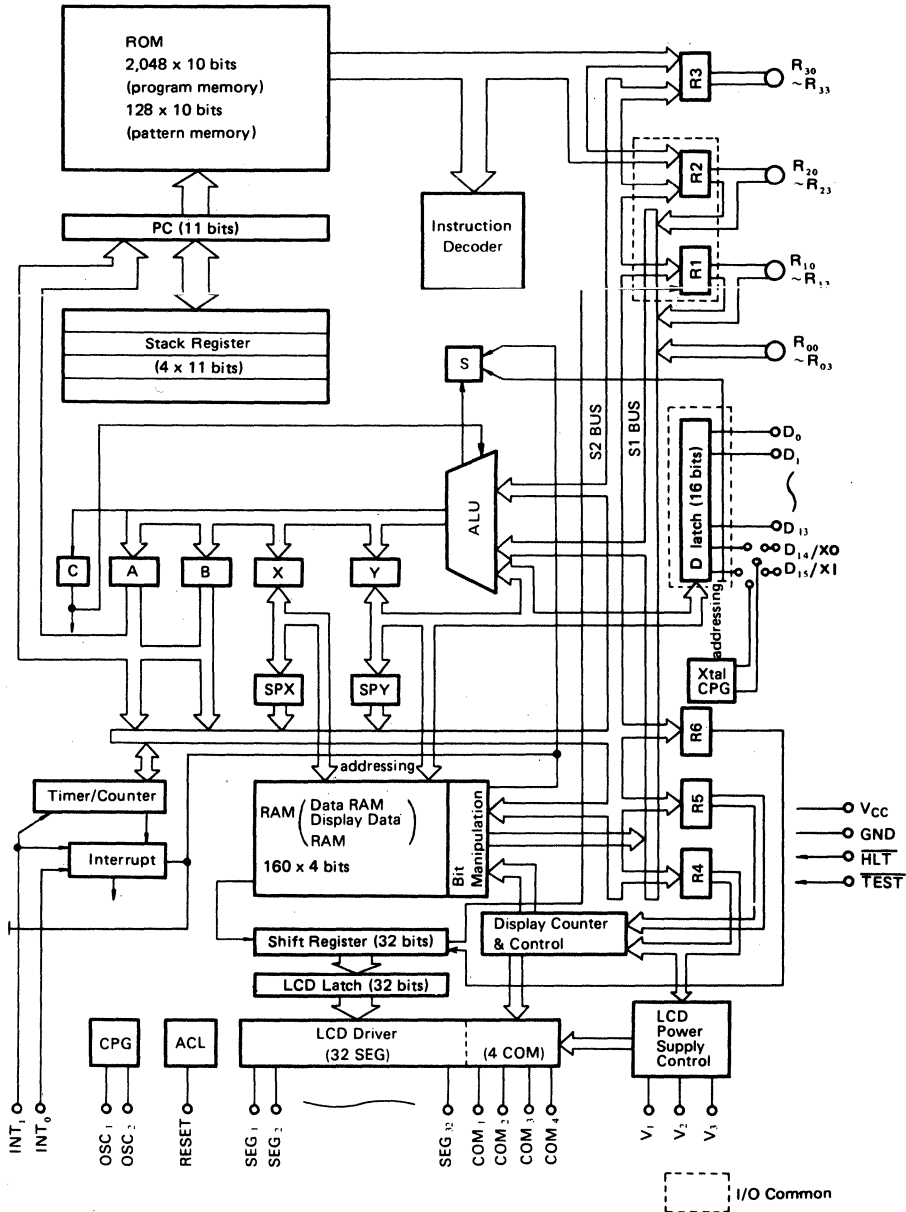


PIN ARRANGEMENT



LCD—III (HD44790, HD44795)

■ BLOCK DIAGRAM



■ HD44790 ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$)

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage (1)	V_{T1}	-0.3 to $V_{CC}+0.3$	V	Applied to all pins except those specified in V_{T2} .
Pin Voltage (2)	V_{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	45	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

- (NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geq V1 \geq V2 \geq V3 \geq GND$ should be maintained.

LCD—III (HD44790, HD44795)

LCD-III

• ELECTRICAL CHARACTERISTICS – 1 ($V_{CC} = 5V \pm 10\%$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test Conditions	Value			Unit	Note	
			min	typ	max			
Input "Low" Voltage	V_{IL}		—	—	1.0	V		
Input "High" Voltage (1)	V_{IH1}		$V_{CC} - 1.0$	—	V_{CC}	V	(9)	
Input "High" Voltage (2)	V_{IH2}		$V_{CC} - 1.0$	—	10	V	(10)	
Output "Low" Voltage	V_{OL}	$I_{OL} = 1.6$ mA	—	—	0.8	V		
Output "High" Voltage (1)	V_{OH1}	$-I_{OH} = 1.0$ mA	2.4	—	—	V	(1)	
Output "High" Voltage (2)	V_{OH2}	$-I_{OH} = 0.01$ mA	$V_{CC} - 0.3$	—	—	V	(2)	
Driver Voltage Descending (COM)	V_{d1}	$I_d = 0.05$ mA	—	—	0.4	V	(13)	
Driver Voltage Descending (SEG)	V_{d2}	$I_d = 0.01$ mA	—	—	0.4	V	(13)	
Dividing Resistor of LCD Power Supply	R_{well}		25	—	300	k Ω		
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	—	—	μs	(15)	
Interrupt Input Fall Time	t_{fINT}		—	—	50	μs	(15)	
Interrupt Input Rise Time	t_{rINT}		—	—	50	μs	(15)	
Output "High" Current	I_{OH}	$V_{OH} = 10V$	—	—	3	μA	(3)	
Input Leakage Current	I_{IL}	$V_{in} = 0$ to V_{CC}	—	—	1.0	μA	(3), (9)	
		$V_{in} = 0$ to 10V	—	—	3	μA	(3), (10)	
Pull up MOS Current	$-I_p$	$V_{CC} = 5V$	45	—	250	μA		
Supply Current (1)	I_{CC1}	$V_{in} = V_{CC}$, $V_{CC} = 5V$, Ceramic Filter Oscillation ($f_{osc} = 400$ kHz)	—	—	1.3	mA	(5)	
Supply Current (2)	I_{CC2}	$V_{in} = V_{CC}$, $V_{CC} = 5V$ R_f Oscillation ($f_{osc} = 400$ kHz) External Clock Operation ($f_{cp} = 400$ kHz)	—	—	0.6	mA	(5), (12)	
Standby I/O Leakage Current	I_{LS}	$HLT = 1.0V$	$V_{in} = 0$ to V_{CC}	—	—	1.0	μA	(6), (9)
			$V_{in} = 0$ to 10V	—	—	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	$V_{in} = V_{CC}$, $HLT = 0.2V$	—	—	10	μA	(11)	
Standby Supply Current (2)	I_{CCS2}	$V_{in} = V_{CC}$, $HLT = 0.2V$	—	—	40	μA	(7)	
Frame Frequency of LCD Drive	f_F	$n = 1$ (static) $n = 2$ (1/2 Duty) $n = 3$ (1/3 Duty) $n = 4$ (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$			Hz		
LCD Display Voltage	V_{LCD}	$V_{CC} - V_3$	2.5	—	V_{CC}	V	(8)	
External Clock Operation; System Clock								
External Clock Frequency	f_{cp}		40	400	440	kHz		
External Clock Duty	Duty		45	50	55	%		
External Clock Rise Time	t_{rcp}		0	—	0.2	μs		
External Clock Fall Time	t_{fcp}		0	—	0.2	μs		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	9.1	10	100	μs		
Internal Clock Operation (R_f Oscillation); System Clock								
Clock Oscillation Frequency	f_{osc}	$R_f = 110k\Omega \pm 2\%$	300	—	500	kHz		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	8.0	—	13.3	μs		
Internal Clock Operation (Ceramic Filter Oscillation); System Clock								
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	392	—	408	kHz		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	9.8	—	10.2	μs		
Internal Clock Operation (Crystal Oscillation); Clock for Timer								
Clock Oscillation Frequency	f_{oscx}	Crystal	32.768			kHz		



● ELECTRICAL CHARACTERISTICS – 2 (T_a = -20 to +75°C)

Item	Symbol	Test Conditions	Value		Unit	Note
			min	max		
Halt Duration Voltage	V _{DH}	$\overline{HLT} = 0.2V$	2.3	—	V	
Halt Current	I _{DH}	V _{in} = V _{CC} , $\overline{HLT} = 0.2V$, V _{DH} = 2.3V	—	4.0	μA	(14)
Halt Delay Time	t _{HD}		100	—	μs	
Operation Recovery Time	t _{RC}		100	—	μs	
HLT Fall Time	t _{fHLT}		—	1000	μs	
HLT Rise Time	t _{rHLT}		—	1000	μs	
HLT "Low" Hold Time	t _{HLT}		400	—	μs	
HLT "High" Hold Time	t _{OPR}	R _f Oscillation, External Clock Operation	100	—	μs	
		Ceramic Filter Oscillation	4000	—		
Power Supply Rise Time	t _{rCC}	Built-in Reset, $\overline{HLT} = V_{CC}$	0.1	10	ms	
Power Supply OFF Time	t _{OFF}	Built-in Reset, $\overline{HLT} = V_{CC}$	1	—	ms	
RESET Pulse Width (1)	t _{RST1}	External Reset, V _{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (R _f Oscillation, External Clock Operation)	1	—	ms	
		External Reset, V _{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$ (Ceramic Filter Oscillation)	4	—		
RESET Pulse Width (2)	t _{RST2}	External Reset, V _{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = System Clock)	2 · T _{inst}	—	μs	
		External Reset, V _{CC} = 4.5 to 5.5V, $\overline{HLT} = V_{CC}$, (Prescaler Clock = Crystal Clock)	32 × 10 ⁶ / f _{oscx}	—		
RESET Rise Time	t _{rRST}	External Reset, $\overline{HLT} = V_{CC}$, V _{CC} = 4.5 to 5.5V	—	100	μs	
RESET Fall Time	t _{fRST}	External Reset, $\overline{HLT} = V_{CC}$, V _{CC} = 4.5 to 5.5V	—	100	μs	

- (NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
 2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
 3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
 4. Pull up MOS current is excluded.
 5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).

Test Conditions: RESET, \overline{HLT} , TEST = V_{CC} (Reset State)
 INT₀, INT₁, R₀ to R₃₃, D₀ to D₁₃ = V_{CC}
 D₁₄/XO, D₁₅/XI — D₁₄/XO, D₁₅/XI = V_{CC} (Crystal oscillation for timer is not selected).
 V₁, V₂, V₃ = V_{CC} — D₁₄/XO = Open, D₁₅/XI = V_{CC} (Crystal oscillation for timer is selected).
 COM₁ to COM₄, SEG₁ to SEG₃₂ = Open

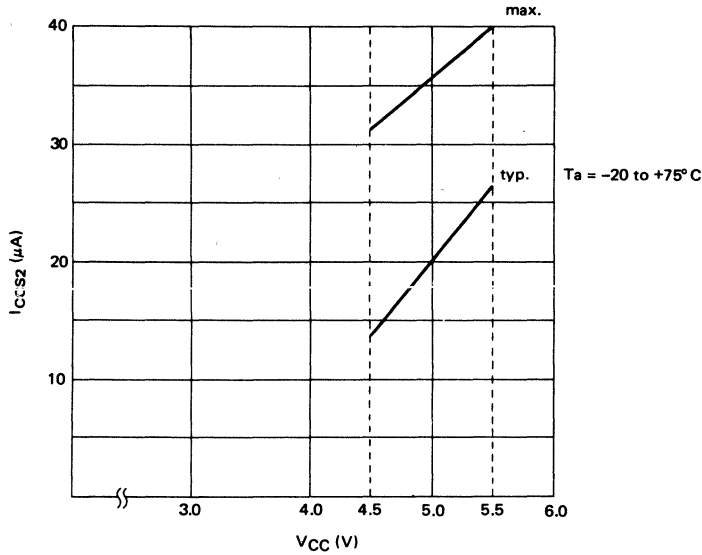
When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC1} or I_{CC2}. When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).

6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

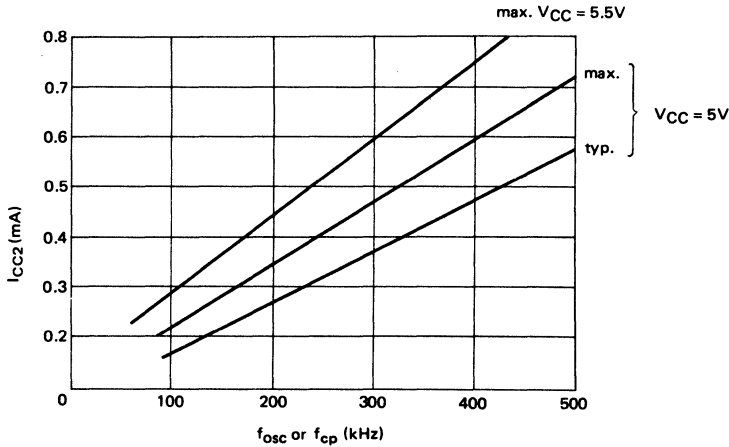


LCD—III (HD44790, HD44795)

7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at $V_{CC} = 5V \pm 10\%$ in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).



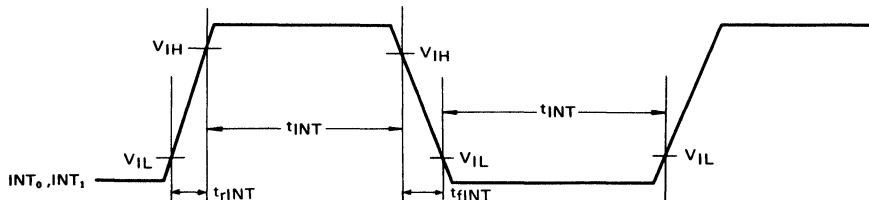
8. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
9. Applied to the following pins.
 - (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R pins.
 - (2) RESET, HLT, OSC₁, INT₀ and INT₁.
10. Applied to open-drain I/O common pins among D and R pins.
11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at $V_{CC} = 5V \pm 10\%$ in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply pins (V_{CC} , V_1 , V_2 , V_3) and each common or segment output pin.
14. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.



15. Interrupt inputs must be retained for two or more cycles at both "High" and "Low" levels.



■ HD44795 ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V)

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V _{CC}	-0.3 to +7.0	V	
Pin Voltage (1)	V _{T1}	-0.3 to V _{CC} +0.3	V	Applied to all pins except those specified in V _{T2} .
Pin Voltage (2)	V _{T2}	0.3 to +10.0	V	Applied to open-drain output pins and open-drain I/O common pins.
Maximum Total Output Current (1)	-ΣI _{o1}	45	mA	(Note 3)
Maximum Total Output Current (2)	ΣI _{o2}	45	mA	(Note 3)
Operating Temperature	T _{opr}	-20 to +75	°C	
Storage Temperature	T _{stg}	-55 to +125	°C	

- (NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition V_{CC} ≥ V1 ≥ V2 ≥ V3 ≥ GND should be maintained.

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● ELECTRICAL CHARACTERISTICS – 1 ($V_{CC} = 2.7$ to $5.5V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test Conditions	Value			Unit	Note	
			min	typ	max			
Input "Low" Voltage	V_{IL}		–	–	0.4	V		
Input "High" Voltage (1)	V_{IH1}		$V_{CC}-0.4$	–	V_{CC}	V	(9)	
Input "High" Voltage (2)	V_{IH2}		$V_{CC}-0.4$	–	10	V	(10)	
Output "Low" Voltage	V_{OL}	$I_{OL} = 0.4$ mA	–	–	0.4	V		
Output "High" Voltage (1)	V_{OH1}	$-I_{OH} = 0.08$ mA	$V_{CC}-0.4$	–	–	V	(1)	
Output "High" Voltage (2)	V_{OH2}	$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	–	–	V	(2)	
Driver Voltage Descending (COM)	V_{d1}	$I_d = 0.05$ mA	–	–	0.4	V	(13)	
Driver Voltage Descending (SEG)	V_{d2}	$I_d = 0.01$ mA	–	–	0.4	V	(13)	
Dividing Resistor of LCD Power Supply	Rwell		25	–	300	k Ω		
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	–	–	μs	(15)	
Interrupt Input Fall Time	t_{fINT}		–	–	50	μs	(15)	
Interrupt Input Rise Time	t_{rINT}		–	–	50	μs	(15)	
Output "High" Current	I_{OH}	$V_{OH} = 10V$	–	–	3	μA	(3)	
Input Leakage Current	I_{IL}	$V_{in} = 0$ to V_{CC}	–	–	1.0	μA	(3), (9)	
		$V_{in} = 0$ to $10V$	–	–	3			(3), (10)
Pull up MOS Current	$-I_P$	$V_{CC} = 3V$	15	–	80	μA		
Supply Current	I_{CC}	$V_{in} = V_{CC}$, $V_{CC} = 3V$ R _f Oscillation ($f_{osc} = 200$ kHz) External Clock Operation ($f_{cp} = 200$ kHz)	–	–	0.15	mA	(5), (12)	
Standby I/O Leakage Current	I_{LS}	$HLT = 0.5V$	$V_{in} = 0$ to V_{CC}	–	–	1.0	μA	(6), (9)
			$V_{in} = 0$ to $10V$	–	–	3	μA	(6), (10)
Standby Supply Current (1)	I_{CCS1}	$V_{in} = V_{CC}$, $HLT = 0.1V$ $V_{CC} = 2.7$ to $3.3V$	–	–	6	μA	(11)	
Standby Supply Current (2)	I_{CCS2}	$V_{in} = V_{CC}$, $HLT = 0.1V$ $V_{CC} = 2.7$ to $3.3V$	–	–	21	μA	(7)	
Frame Frequency of LCD Drive	f_F	$n = 1$ (static) $n = 2$ (1/2 Duty) $n = 3$ (1/3 Duty) $n = 4$ (1/4 Duty)	$\frac{1}{128 \times n \times T_{inst}}$			Hz		
LCD Display Voltage	V_{LCD}	$V_{CC}-V_3$	2.5	–	V_{CC}	V	(8)	
External Clock Operation; System Clock								
External Clock Frequency	f_{cp}		40	200	240	kHz		
External Clock Duty	Duty		45	50	55	%		
External Clock Rise Time	t_{rep}		0	–	0.2	μs		
External Clock Fall Time	t_{fcp}		0	–	0.2	μs		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	16.6	20	100	μs		
Internal Clock Operation (R_f Oscillation); System Clock								
Clock Oscillation Frequency	f_{osc}	R _f = 200k Ω ±2%	$V_{CC} = 2.7$ to $3.3V$	150	–	250	kHz	
			$V_{CC} = 2.7$ to $5.5V$	150	–	350		
Instruction Cycle Time	T_{inst}	$T_{inst} =$ $4/f_{osc}$	$V_{CC} = 2.7$ to $3.3V$	16	–	26.6	μs	
			$V_{CC} = 2.7$ to $5.5V$	11.4	–	26.6		
Internal Clock Operation (Crystal Oscillation); Clock for Timer								
Clock Oscillation Frequency	f_{oscx}	Crystal	32.768			kHz		



● ELECTRICAL CHARACTERISTICS – 2 (T_a = -20 to +75°C)

Item	Symbol	Test Conditions	Value		Unit	Note
			min	max		
Halt Duration Voltage	V _{DH}	HLT = 0.2V	2.3	–	V	
Halt Current	I _{DH}	V _{in} = V _{CC} , HLT = 0.1V, V _{DH} = 2.3V	–	4.0	μA	(14)
Halt Delay Time	t _{HD}		100	–	μs	
Operation Recovery Time	t _{RC}		100	–	μs	
HLT Fall Time	t _{fHLT}		–	1000	μs	
HLT Rise Time	t _{rHLT}		–	1000	μs	
HLT "Low" Hold Time	t _{HLT}		400	–	μs	
HLT "High" Hold Time	t _{OPR}	R _f Oscillation, External Clock Operation	100	–	μs	
Power Supply Rise Time	t _{rCC}	Built-in Reset, HLT = V _{CC}	0.1	10	ms	
Power Supply OFF Time	t _{OFF}	Built-in Reset, HLT = V _{CC}	1	–	ms	
RESET Pulse Width (1)	t _{RST1}	External Reset, HLT = V _{CC}	1	–	ms	
RESET Pulse Width (2)	t _{RST2}	External Reset, V _{CC} = 2.7 to 5.5V, HLT = V _{CC} , (Prescaler Clock = System Clock)	2 · T _{inst}	–	μs	
		External Reset, V _{CC} = 2.7 to 5.5V, HLT = V _{CC} , (Prescaler Clock = Crystal Clock)	32 × 10 ⁶ / f _{oscx}	–		
RESET Rise Time	t _{rRST}	External Reset, HLT = V _{CC} , V _{CC} = 2.7 to 5.5V	–	100	μs	
RESET Fall Time	t _{fRST}	External Reset, HLT = V _{CC} , V _{CC} = 2.7 to 5.5V	–	100	μs	

- (NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
 2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
 3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
 4. Pull up MOS current is excluded.
 5. Applied to the supply current when the LCD-III is in the reset state and the crystal oscillation for timer doesn't operate (Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded).

Test Conditions: RESET, HLT, TEST = V_{CC} (Reset State)
 INT₀, INT₁, R₀₀ to R₃₃, D₀ to D₁₃ = V_{CC}
 D₁₄/XO, D₁₅/XI $\begin{cases} \text{D}_{14}/\text{XO}, \text{D}_{15}/\text{XI} = \text{V}_{\text{CC}} & \text{(Crystal oscillation for timer is not selected)} \\ \text{D}_{14}/\text{XO} = \text{Open}, \text{D}_{15}/\text{XI} = \text{V}_{\text{CC}} & \text{(Crystal oscillation for timer is selected)} \end{cases}$
 V₁, V₂, V₃ = V_{CC}
 COM₁ to COM₄, SEG₁ to SEG₃₂ = Open

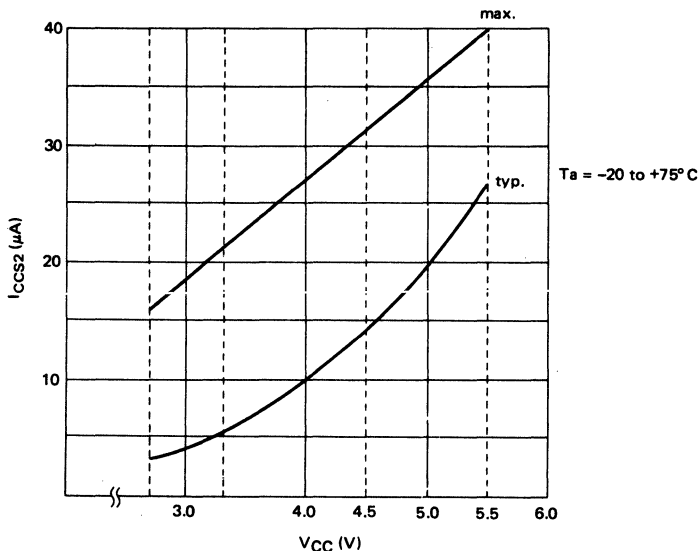
When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}. When the LCD-III is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-III. User should design the power supply in consideration of this point (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).

6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.

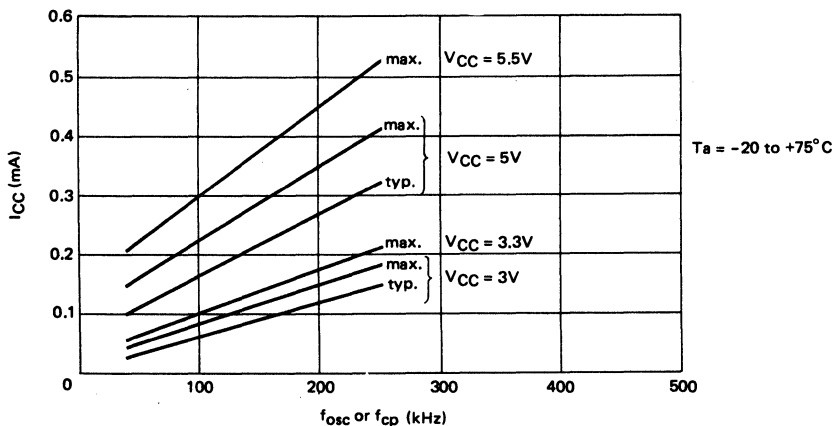


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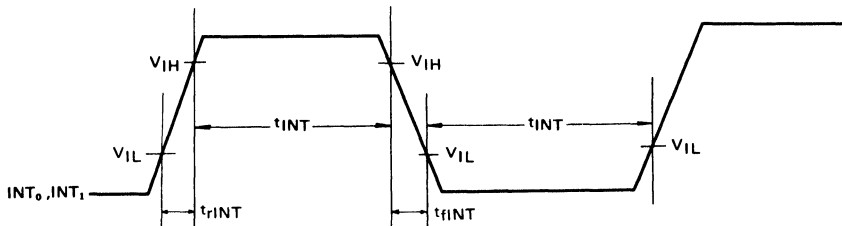
7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at $V_{CC} = 3V \pm 10\%$ in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).



8. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
 9. Applied to the following pins.
 (1) Input pins, I/O common pins with pull up MOS, and CMOS I/O common pins among D and R pins.
 (2) RESET, HLT, OSC₁, INT₀ and INT₁
 10. Applied to open-drain I/O common pins among D and R pins.
 11. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current is the supply current at $V_{CC} = 3V \pm 10\%$ in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}).
 12. The supply current changes as follows according to operating frequency.



13. The voltage that drops between the power supply pins (V_{CC} , V_1 , V_2 , V_3) and each common or segment output pin.
14. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.
15. Interrupt inputs must be retained for two or more cycles at both "High" and "Low" levels.



■ **SIGNAL DESCRIPTION**

The input and output signals for the LCD-III shown in PIN ARRANGEMENT are described in the following paragraphs.

● **VCC and GND**

Power is supplied to the LCD-III using these two pins. VCC is power and GND is the ground connection.

● **RESET**

This pin resets the LCD-III independently of the automatic resetting capability (ACL; Built-in Reset Circuit) already in the LCD-III. The LCD-III can be reset by pulling RESET High.

Refer to RESET FUNCTION for additional information.

● **OSC₁ and OSC₂**

These pins provide control input for the on-chip clock oscillator circuit. A resistor, a ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized.

Refer to OSCILLATOR for recommendations about these pins.

● **HLT**

This pin is used to enter the LCD-III into the HALT state (Stand-by Mode). The LCD-III can be moved into the halt state by pulling HLT Low.

In the halt state the internal clock stops and all the internal statuses (RAM, Registers, Carry, Status, Program Counter, etc.) are maintained. Consequently power consumption is greatly reduced. By pulling HLT high, the LCD-III starts operation from the status just before the halt state.

Refer to HALT FUNCTION for details of halt mode.

● **TEST**

This pin is not for user application and must be connected to VCC.

● **INT₀ and INT₁**

These pins generate interrupt request to the LCD-III. Refer to INTERRUPT for additional information.

● **V₁, V₂ and V₃**

Power for liquid crystal display are supplied to the LCD-III using these pins ($V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$).

● **R₀₀ to R₀₃**

These four lines are a 4-bit input channel.

Refer to INPUT/OUTPUT for additional information.

● **R₁₀ to R₁₃, R₂₀ to R₂₃**

These 8 lines are arranged into two 4-bit Input/Output common channels. 4-bit registers (data I/O register) are attached to these channels. Each channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain, With Pull Up MOS, and CMOS using a mask option.

Refer to INPUT/OUTPUT for additional information.

● **R₃₀ to R₃₃**

These four lines are a 4-bit output channel. 4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option.

Refer to INPUT/OUTPUT for additional information.

● **D₀ to D₁₃**

These are 14 discrete signals which can be configured as Input/Output lines.

Refer to INPUT/OUTPUT for additional information.

● **D₁₄/XO, D₁₅/XI**

D₁₄/XO and D₁₅/XI select in the following 3 types with a mask option.

- Discrete I/O (common pin)
- Crystal circuit connecting pins (with internal halt)
- Crystal circuit connecting pins (no internal halt)

Refer to INPUT/OUTPUT for additional information.

● **COM₁ to COM₄**

These pins are common pins for liquid crystal display.

Refer to LIQUID CRYSTAL DISPLAY for additional information.

● **SEG₁ to SEG₃₂**

These are segment pins for liquid crystal display.



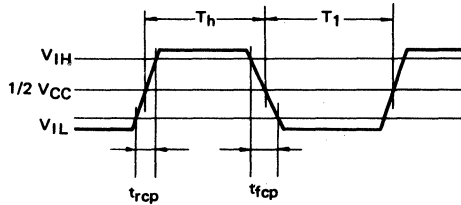
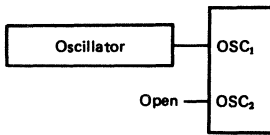
LCD—III (HD44790, HD44795)

Refer to LIQUID CRYSTAL DISPLAY for additional information.

■ OSCILLATOR

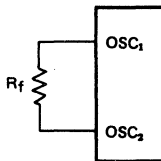
A resistor, a ceramic filter circuit or an external oscillator can be connected to OSC₁ and OSC₂. However, a ceramic filter circuit cannot be used on the HD44795. The connection methods are shown in Figure 1.

(1) External Clock



$$\text{Duty} = \frac{T_1}{T_h + T_1} \times 100\%$$

(2) Resistor



Length of the wirings for OSC₁ and OSC₂ pins should be minimized because the oscillation frequency varies depending on the capacitance of these pins.

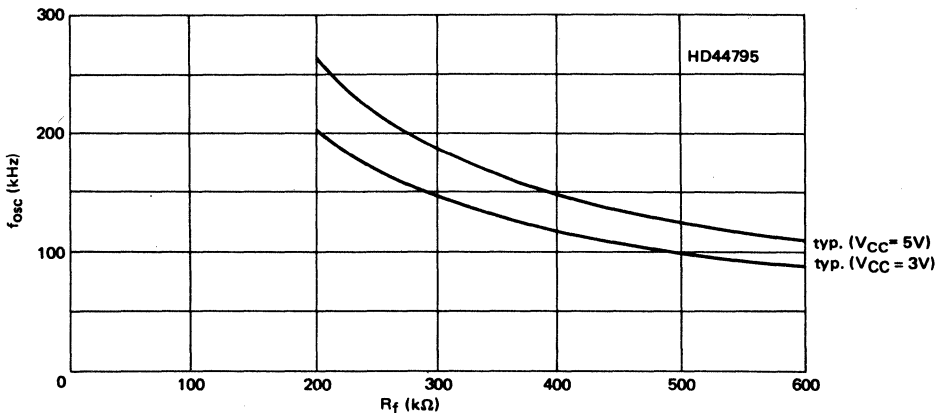
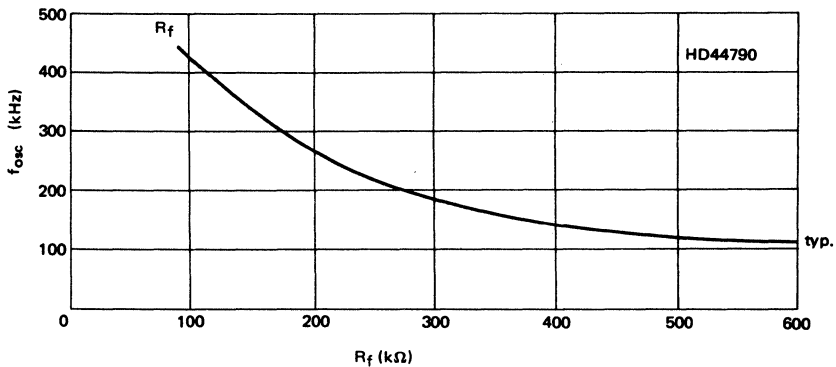
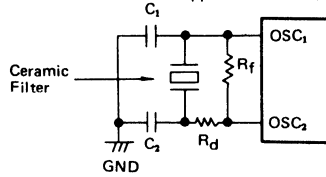


Figure 1 Connection Methods for Oscillator (to be continued)



(3) Ceramic Filter (This is not applied to HD44795.)



Ceramic Filter: CSB400P (MURATA)
 R_f : $1M\Omega \pm 10\%$
 C_1 : $330pF \pm 10\%$ (ceramic capacitor)
 C_2 : $330pF \pm 10\%$ (ceramic capacitor)
 R_d : $2.2k\Omega \pm 10\%$

Reset at the time of Halt releasing.
 This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constant carefully on your application.

Figure 1 Connection Methods for Oscillator

■ ROM

ROM is used as program and pattern (constants) memory. The instruction used in the LCD-III consists of 10 bits.

The pattern area is in pages 61 and 62. No program can be

stored in this area. The area is only used to store patterns (constants) that are referred in programs by user.

The program area (instructions can be programmed) consists of 2,048 words (64×32) of pages 0 to 31. In this area, either of programs or patterns can be stored.

Table 1 ROM Capacity

Program Area	32 pages
Pattern Area	2 pages
Total Number of the words	2,176 words

(NOTE) 1 page = 64 words

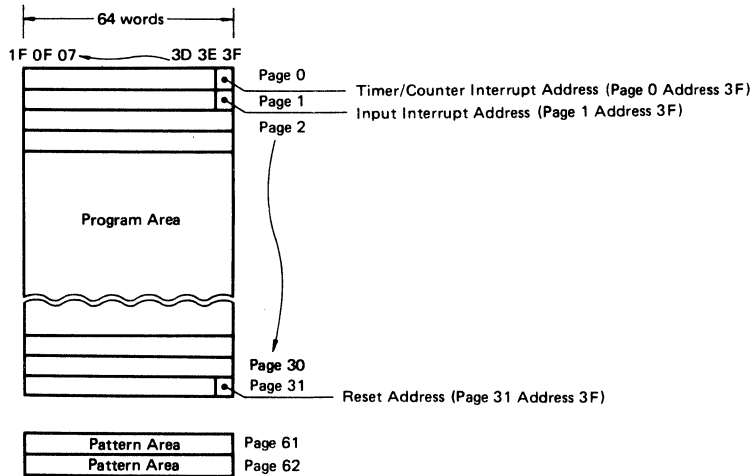


Figure 2 ROM Address Space

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PROGRAM COUNTER (PC)

PC is the counter for addressing the program area of ROM. It consists of the page part and the address part as shown in Figure 3.

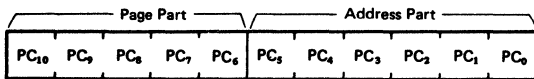


Figure 3 PC Structure

Page Part (5-bit register)

Once a certain value is loaded into a page part, it is unchanged until other value is loaded by the program. Any number among 0 to 31 can be set in the page part.

Address Part (6-bit counter)

The address part consists of a random sequential counter and this counter counts up for each word, that is, one instruc-

tion cycle. All instructions except the pattern instruction are executed in one cycle. (While the pattern instruction is executed in two cycles.)

The sequence indicated in decimal and hexadecimal is shown in Table 2. This sequence forms a loop and has neither the starting nor ending points. It generates no overflow carry. Therefore, instructions on a same page are executed in order unless the contents of the page part is unchanged.

PATTERN GENERATION

The pattern (constants) can be assigned into ROM for user's reference in program. It can be written both in the program area and the pattern area.

Pattern reference is performed by the instruction of pattern (P) in the program.

ROM Addressing for the pattern reference is performed by modifying PC with A, B, C (F/F), and the operand p. The modifying scheme is shown in Figure 4. The address part is replaced by the contents of A (Accumulator) and the lower 2 bits of B. The page part is logically ORed with the PC, the upper 2 bits of the operand is for referring to the pattern area. When the upper bit is preset to 1, the pattern area is referred, and it is preset to 0, the program area is referred. Non-existing ROM area can not be referred.

Table 2 Sequence of the PC Address Part

Decimal	Hexa-decimal	Decimal	Hexa-decimal	Decimal	Hexa-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		

The value of PC is only modified apparently and is not changed. Then the address is counted up after the execution of P instruction and the next instruction is executed. The execution time of this instruction is 2-cycle time. Moreover, an instruction just after this instruction is masked.

The bit pattern of referred ROM address is generated as the following two ways.

(i) The pattern is loaded into A and B.

(ii) The pattern is loaded into the output ports R2 and R3.

The command bits (O_9 , O_{10}) in the pattern determine which way is taken. Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1". Mode (i) and (ii) are simultaneously performed when both O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

In the program run, the pattern can not be distinguished from the instruction. When the program is running at the address written as a pattern by user, the instruction corresponding to the pattern bit is executed.

Therefore, when the pattern is written in the pattern area, the instruction must not be executed.

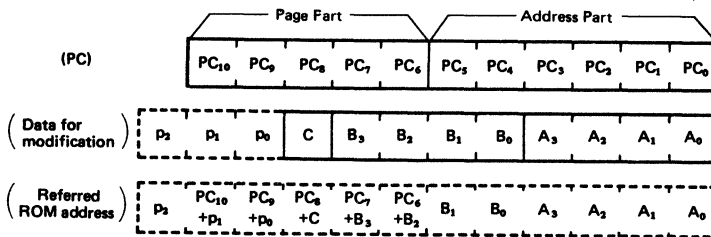


Figure 4 ROM Addressing for Pattern Reference



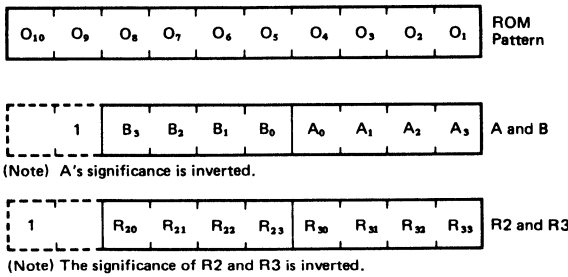


Figure 5 Correspondence of Each Bit of the Pattern

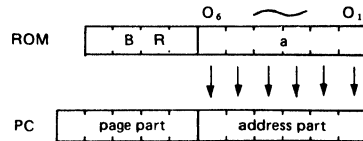
■ **BRANCH**

ROM is accessed according to the PC sequence and the program is executed. In order to jump to an optional address out of the sequence, there are four ways.

- (i) Branch to an address in the same page
- (ii) Page jump
- (iii) Branch to an address in any page (combination of (i) and (ii))
- (iv) Branch referring to the data (Table Branch)

● **Branch to an address in the same page (BR)**

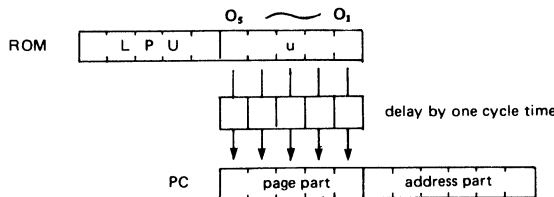
The lower 6 bits of ROM output (operand a, O_6 to O_1) are transferred to the lower 6 bits of PC (address part). This instruction is a conditional statement and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1"



● **Page Jump (LPU)**

The lower bits of ROM output (operand u, O_1 to O_5) are transferred to the upper 5 bits (page part) of PC with delay by one cycle time. Therefore, at the cycle just after this instruction, the page remains unchanged and the page jump is performed at the next cycle.

This instruction is a conditional statement and executed only when the Status is "1". But the Status is unchanged (remains "0") even if it is skipped.



(NOTE) Operand u can be 0 to 31

Interrupt is disabled for one instruction cycle time immediately after LPU instruction in spite of interrupt enable condition. Interrupt request is latched into the interrupt request F/F. LPU instruction is normally used as a macro instruction of BRL and CALL.

If it is used singly, page is changed after the execution of the instruction just after LPU. Address part of PC follows the usual sequence.

● **Branch to an Address in Any Page (BRL)**

This is a macro instruction composed of LPU + BR divided into two steps as follows.

BRL $a - b \rightarrow$ LPU a

(Jump to address b on page a) BR b

This is also conditional statement like LPU and BR, and executed only when the Status is "1". If it is "0", the instruction is skipped and it becomes "1".

● **Branch Referring to the Data (TBR : Table Branch)**

PC is modified by accumulator, B register, C(F/F), and the operand p. The address part is replaced by accumulator and the lower 2 bits of B register. The page part is logically ORed with the upper 2 bits of B register, C(F/F), and the operand p_1, p_0 . This instruction is executed irrespectively of the Status.

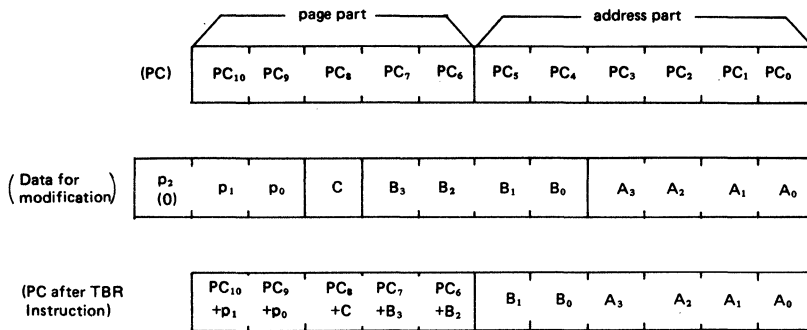


Figure 6 Modification of PC by TBR instruction

The method of the modification of PC by TBR is the same as that of pattern instruction. But the content of PC is changed because TBR is a jump instruction. Interrupt is disabled for one instruction cycle time immediately after TBR instruction inspite of interrupt enable condition. Interrupt request is latched into interrupt request F/F.

(NOTE) The upper bit (p_2) of the operand p should be "0" because it indicates the pattern area. The value of operand p should be 0 to 3.

- **SUBROUTINE**
There are two kinds of subroutine jump.
 - (i) Subroutine jump to an address in a subroutine space (CAL)
 - (ii) Subroutine jump to an address on any page (CALL)
 Here, the subroutine space means page 0.

- **Subroutine Jump to an Address in a Subroutine Space (CAL)**
PC is pushed on the stack in the following order.

PC+1 → ST1 → ST2 → ST3 → ST4

The page part of PC is 0. The lower 6 bits of ROM output (Operand a , O_6 to O_1) are transferred to the lower 6 bits of PC (Address Part).

(NOTE) "PC+1" does not mean the added address by 1, but the next address to the CAL instruction address in the sequence of PC address part. Refer to the sequence (Table 2) in PC address part.

CAL instruction is a conditional statement. It is executed only when the Status is "1". If the Status is "0", this instruction is skipped and the status becomes "1". Interrupt is disabled for one instruction cycle time immediately after CAL instruction in spite of interrupt enable condition. Interrupt request is latched into the interrupt request F/F.

The condition of PC when pushed on the stack during the execution of CAL instruction is shown in Fig. 7.

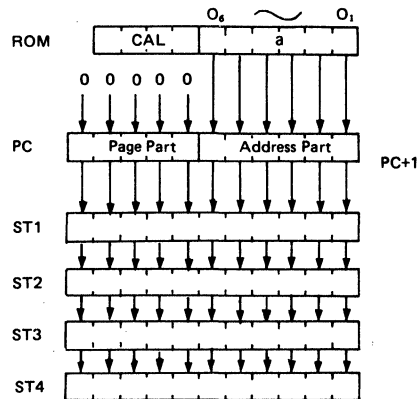


Figure 7 The condition of PC when pushed on the stack during the execution of CAL instruction

- **Subroutine Jump to an Address on Any Page (CALL)**
This is a macro instruction of LPU+CAL. The subroutine jump to any address on the page specified by LPU is possible.

CALL $a - b$ → LPU a

(Subroutine jump to address b on page a)

CAL b

This is a conditional instruction like LPU and CAL, and executed when the Status is "1". If the status is "0", this instruction is skipped and the Status becomes "1".

- **Return (RTN)**
Return from subroutine is performed by RTN instruction in the following sequence:

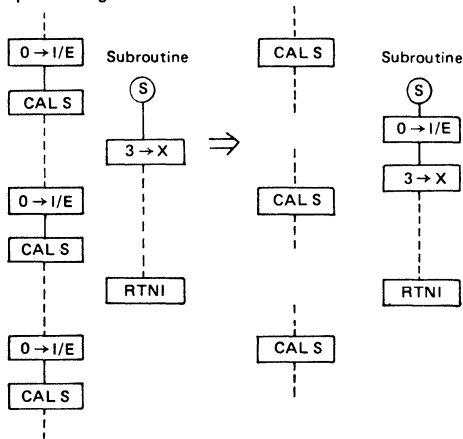
ST4 → ST3 → ST2 → ST1 → PC

Since the next address to PC is pushed on the stack register (ST1) during the execution of subroutine jump, the address next to the subroutine jump instruction (CAL instruction) is pulled into the PC at execution of RTN.

(NOTE) Up to 4 levels are available for subroutine levels (nesting) including interrupt level. Note that when counting level numbers, interrupt servicing is a kind of subroutine jump and should be included in the numbers. (When subroutines are used up to the maximum level, interrupt must be disabled condition during executing the last level subroutine. An interrupt, if

occurred, destroys the contents of the stack register. Execution of REIE and CAL to make interrupt disabled during the execution of the last level subroutine, is not recommended, because the same number of REIE instruction as subroutines is required. To solve this problem number of steps can be reduced by executing REIE instruction at the start of the subroutine, as shown in the following instruction, utilizing the fact that any interrupt is disabled for one instruction cycle time immediately after CAL instruction. This method is also effective to inhibit an interrupt during subroutine execution.

Example of Program



RAM

RAM is the memory used for data storage and register save (data RAM) and storage of segment data for liquid crystal display (display data RAM). One unit (digit) consists of 4 bits and there is a total of 160 digits (640 bits).

(NOTE) Capacity of display data RAM varies corresponding to the duty ratio of LCD.

Addressing of RAM is performed by the matrix of the file number and the digit number. There are 10 files and 16 digits in the matrix. Normally the file No. is set in the X register and the digit No. is in the Y register, then the matrix of X and Y addresses RAM and performs the Read/Write operation.

Special digits in RAM can be addressed without using X and Y. These digits, 16 digits (MR0 to MR15), are called Memory Register (MR). Memory register can be exchanged for A register By XAMR instruction. RAM address space is shown in Figure 8.

	Y	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	d																	← digit No.
0	0																	
1	1																	
2	2																	
3	3																	
4	4																	
5	5																	
6	6																	
7	7																	
8	8																	
12~15	9	MR15	MR14	MR13	MR12	MR11	VR10	MR 9	MR 8	MR 7	MR 6	MR 5	MR 4	MR 3	MR 2	MR 1	MR 0	
		↑ file No.																

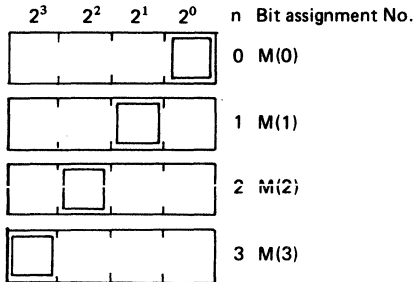
- * The area marked as is usable only for data.
- * The area marked as is usable for both data and display.
- * The file 8 is selected when X register has any value among 8 to 11, and the file 9 is selected when 12 to 15.

Figure 8 RAM Address Space



If an instruction consists of a simultaneous Read/Write operations of RAM (exchange of RAM and a register), the writing data doesn't affect the reading data because the read operation precedes the write operation.

RAM bit manipulation is usable, which performs any bit set, reset or test of the addressed RAM. Bit assignment is made by the program as shown below.



The bit test makes the status "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

REGISTERS

The LCD-III has six 4-bit registers and two 1-bit registers available to the programmer. 1-bit registers are Carry F/F and Status F/F. They are explained in the following paragraphs.

Accumulator (A; A Register) and Carry F/F (C)

The result of ALU operation (4 bits) and the overflow of the ALU are put into the accumulator and Carry F/F respectively. Carry F/F can be set, reset or tested. Combination of the accumulator and Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

B Register (B)

The result of ALU operation (4 bits) is put into this register. B register is used as a sub-accumulator to stack the data temporarily and also used as a counter.

X Register (X)

The result of ALU operation (4 bits) is put into this register. X register is exchangeable with SPX register and addresses the RAM file.

SPX Register (SPX)

SPX register is exchangeable with X register. SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with X register.

Y Register (Y)

The result of ALU operation (4 bits) is put into this register. Y register is exchangeable with SPY register. Y register can calculate itself simultaneously with transferring the data by bus lines, which is usable for the calculation of two or more digits (4 bits/digit). Y register addresses the RAM digits and 1-bit discrete input/output common pins.

SPY Register (SPY)

SPY register is exchangeable with Y register. SPY register is used to stack the contents of the Y register and expand the addressing system of RAM and 1-bit discrete input/output common pins in combination with Y register.

Status F/F (S)

Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. Status F/F affects conditional instructions (LPU, BR and CAL). These instructions are executed only when Status F/F is "1". If it is "0", these instructions are skipped and Status F/F becomes "1".

INPUT/OUTPUT

Discrete I/O (D Pin)

The discrete I/O is composed of 1-bit latch and I/O pin. Figure 9 shows the basic block diagram.

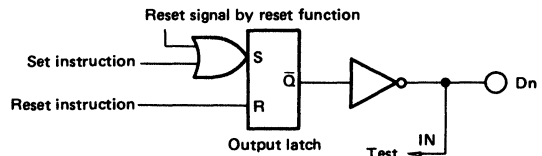


Figure 9 Discrete I/O Block Diagram

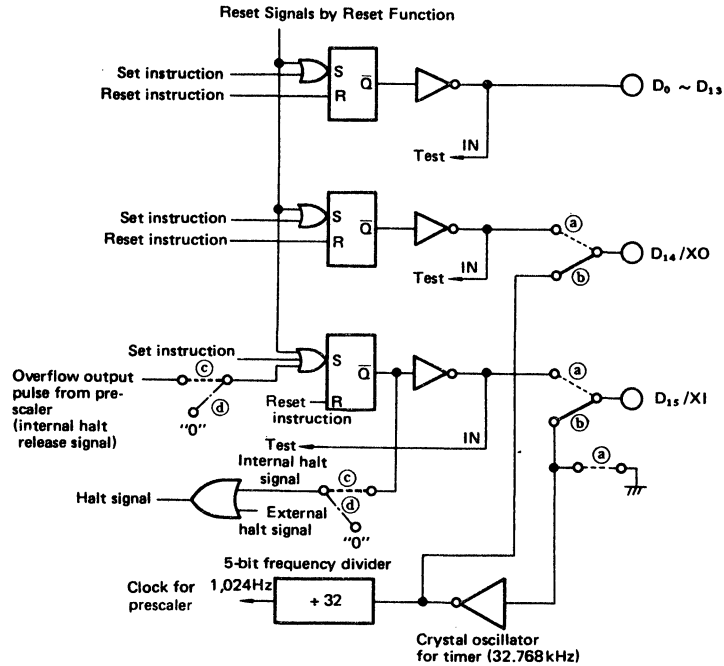


Figure 10 Mask Option of D₁₄ and D₁₅

D₀ to D₁₃ are discrete I/Os of common for input and output, D₁₄ and D₁₅ require 3 types of mask option.

If there is internal halt mode, latch of D₁₅ is used as a register for internal halt mode specially.

In such case, since D₁₅ means internal halt state and D₁₅ = "1" means operating state, LSI can be in internal halt state by

resetting D₁₅ using an instruction. The prescaler keeps its operation in internal halt state. Therefore, D₁₅ may be set by overflow output pulse from the prescaler to return to operating state. Refer to HALT FUNCTION for details of internal halt mode.

Table 3 Mask Option of D₁₄/XO and D₁₅/XI Pins

Mask Option		a	b	c	d	Function of D ₁₄ /XO and D ₁₅ /XI	Function of D ₁₄ /XO and D ₁₅ /XI latch
1	Unselectable crystal oscillation for timer (no internal halt)	short	open			discrete I/O (common Pin)	Output Latch
2	Selectable crystal oscillation for timer	with internal halt		open	short	Crystal Circuit Connecting Pin	
3		no internal halt	open	short			D ₁₅ ; register for internal halt

(NOTE) Users can specify this mask option in "The format of I/O channels" at ROM order.

Discrete I/O is addressed by Y register, and the set/reset instruction is executed for the addressed latch. Level ("0" or "1") of the addressed pin and 1 bit register can be tested. The test is executed by performing wired OR between the output of the latch and the pin input. Therefore, in the case of the

I/O common pins, the output latch should be in the high impedance state when the test instruction is executed. In order to test the pin input, it is necessary the state that the output latch should not affect the pin input.

LCD—III (HD44790, HD44795)

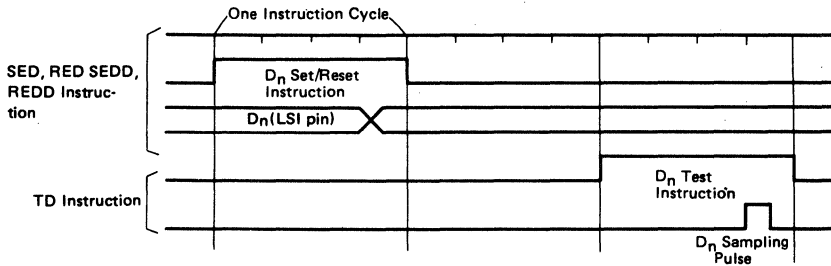


Figure 11 Timing Chart of Discrete I/O

● Data I/O (R Pin)

Table 4 Data I/O for the LCD-III

I/O common channel	R1, R2 (2 channels)
Input channel	R0 (1 channel)
Output channel	R3 (1 channel)
Total	4 channels

4-bit register (data I/O register) is attached to each I/O common channel and output channel. No register is attached to input channel. Addressing to all channels is performed by programs (addressed by operands in instructions).

Figure 12 shows the block diagram of each channel.

(NOTE) In addition to the above, R4, R5 and R6 are provided as register setting liquid crystal display mode. In these registers, there is no pin and exists only data I/O register each, which controls liquid crystal display mode. Data is transferred to R4, R5 and R6 by LRA or LRB instruction, same as data transfer to data I/O registers of R1, R2 and R3. For details of R4, R5 and R6, refer to LIQUID CRYSTAL DISPLAY.

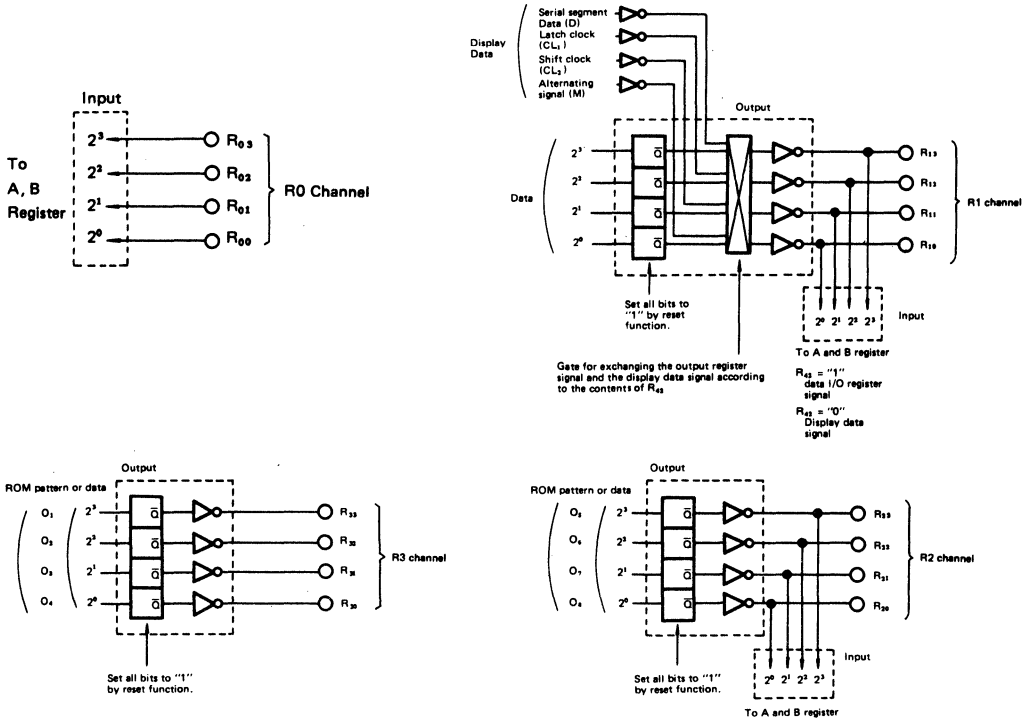


Figure 12 Data I/O Block Diagram



When expansion of segment signal for liquid crystal display is designated by a program (Register $R_{42} = "0"$), R1 is used as a display data output pin. This prohibits R1 to be used as an I/O common channel by users (Refer to Figure 12, R1 channel).

If LRA or LRB instruction is executed at the time, data is transferred to data I/O register, but the contents of data I/O register is not output from R1. If LAR or LBR instruction is executed, display data is input to accumulator (A register) or B register.

Data is transferred from the accumulator (A register) and B register to data I/O registers R1, R2, and R3 through the bus

line. In addition, ROM bit patterns can be transferred to R2 and R3 by pattern generation instruction.

Input instructions input 4-bit data to the accumulator (A register) and B register through the channels R0, R1 and R2. However, in the case of I/O common channels R2 and R3, since data I/O register outputs are connected to pins, input is executed by performing wired OR between the register output and the pin input. For this reason, to input pin input signal, registers must be set to a state that would not affect the pin input.

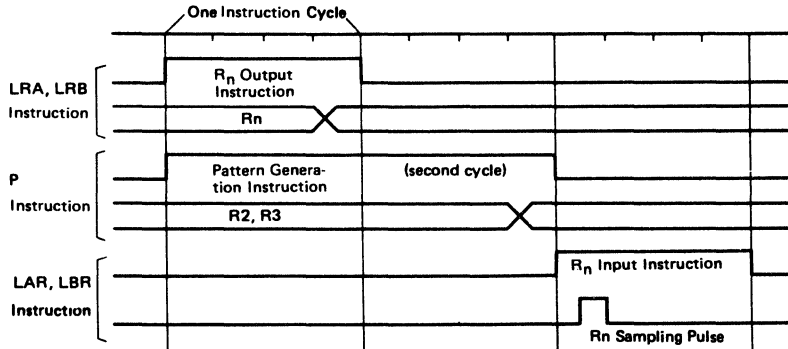
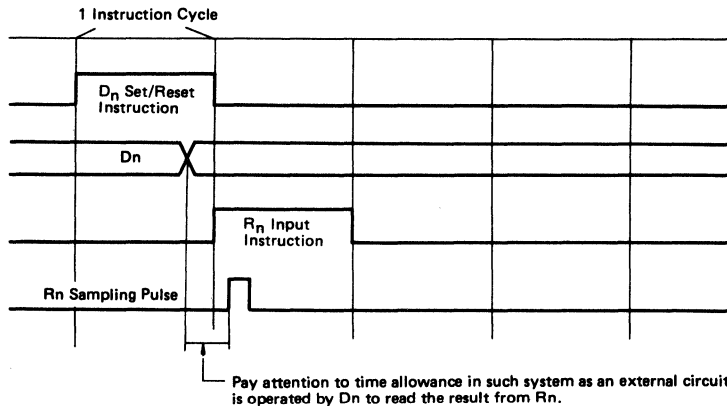


Figure 13 Data I/O Timing Chart

Pay attention: When executing an input instruction to output channel, the microcomputer reads unstabilized value causing malfunction of the program.

When executing an input instruction (LAR and LBR) from the data I/O, pay attention to time allowance after executing an output instruction. At the time, the input sampling pulse is generated during the first half of the instruction cycle.



Applied Pins: INT₀, INT₁, R₀₀ to R₀₃

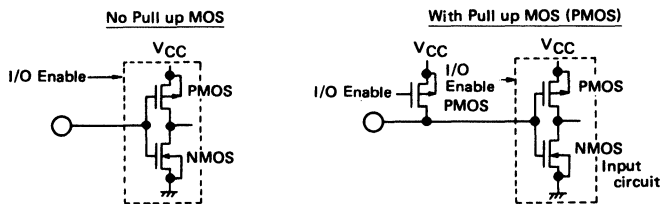


Figure 14 Configuration of Input Pins

Applied Pins: R₃₀ to R₃₃

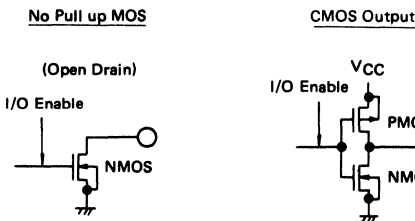


Figure 15 Configuration of Output Pins

Applied Pins: D₀ to D₁₃, D₁₄/XO, D₁₅/XI, R₁₀ to R₁₃, R₂₀ to R₂₃

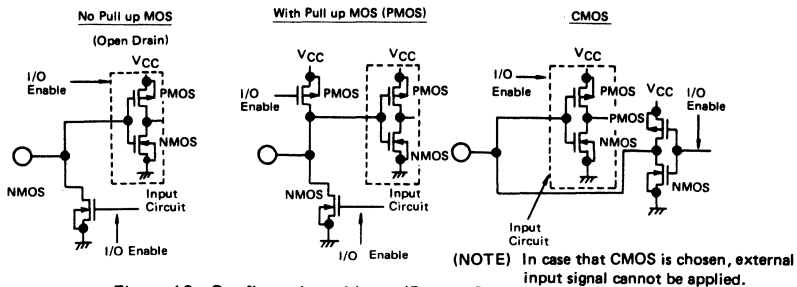


Figure 16 Configuration of Input/Output Pins



■ TIMER/COUNTER

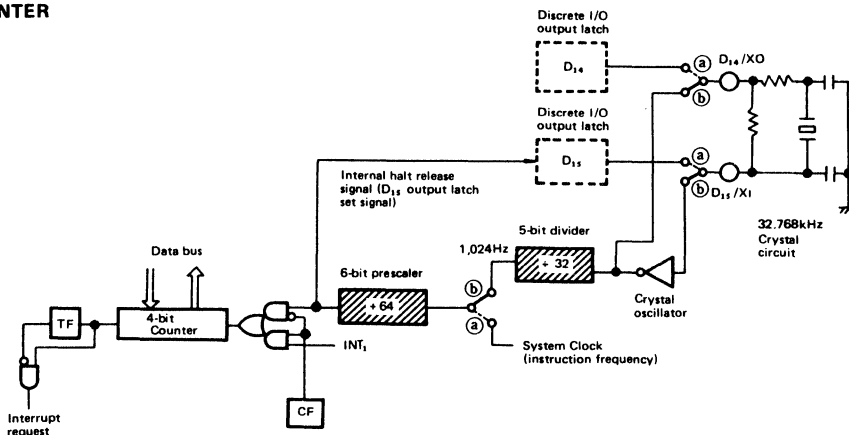


Figure 17 Timer/Counter Block Diagram

Timer/Counter Block Diagram is shown in Figure 17. 5-bit divider divides the crystal oscillation (32.768kHz) by 32 and generates clocks of 1,024Hz in the crystal oscillation mode. It does not stop in the halt state. Prescaler divides the system clock (instruction frequency) or 1,024Hz clock by 64 and generates overflow output pulse of "Instruction frequency/64Hz" or 16Hz. In the crystal oscillation mode, it does not stop during halt state. The input of the 4-bit counter is overflow output pulse of the prescaler or a pulse of INT₁ pin. Input selection is determined by CF state. Data can be exchanged between the counter and bus by LTI, LTA or LAT instruction. TF is a flip-flop which masks the interrupt of timer/counter.

The timer is operable in 2 modes (timer mode and counter mode) depending on what to count, and the mode is selected by programs.

● Timer Mode

The 4-bit counter counts prescaler overflow output pulses. One of the following two can be selected as the prescaler count clock by the mask option.

1. System clock (Instruction frequency)
2. 1,024Hz clock (Crystal oscillation for timer is selected.) . . .

Clock obtained by dividing the crystal oscillation (32.768kHz) for timer by 32. Crystal oscillator is constructed between D pins of D₁₄ and D₁₅ :

Note 1) In this case, the overflow output pulses from the prescaler are 16Hz. These pulses are counted by the 4-bit counter to generate an interrupt (16Hz to 1Hz).

Note 2) In this case, the part marked with in Figure 17 Timer/Counter does not stop even in halt state. When using "internal halt mode", internal halt state is generated by resetting the register for internal halt mode (D latch: D₁₅) by an instruction (D₁₅ = "0": internal halt state, D₁₅ = "1": operating state), and all the operation stop. In this case, overflow output pulse from the prescaler work as the internal halt releasing signal and set the D₁₅ output latch.

By utilizing this function, intermittent operation is possible, that is, program execution for necessary processing (for example, counting for clock function) starts after every 62.5 msec (16Hz) and the LSI stops after execution of the program by an instruction which makes the LSI into internal halt state. This reduces the time in which the LSI operates, resulting in power consumption in substance.

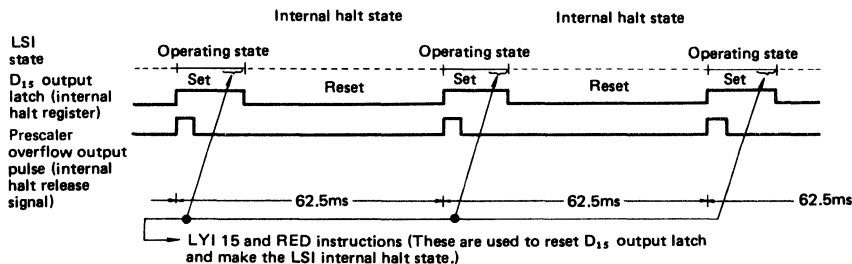


Figure 18 Set/Reset Operation Using Crystal Oscillator for Timer



● **Counter Mode**

Counts pulses of INT₁ pin.

(Note) The width of INT₁ pulse in the counter mode must be at least 2-cycle time for both the “High” and “Low” levels.

■ **INTERRUPT**

There are interrupt caused by the timer/counter or the

inputs. Each interrupt factor has the interrupt request F/F and the request is latched into this flip-flop when it is generated. If an interrupt request can be accepted, the interrupt is generated.

It is controlled by Interrupt Enable F/F (I/E F/F) whether an interrupt can be accepted or not.

Figure 19 shows the interrupt block diagram and Figure 20 shows the interrupt timing chart.

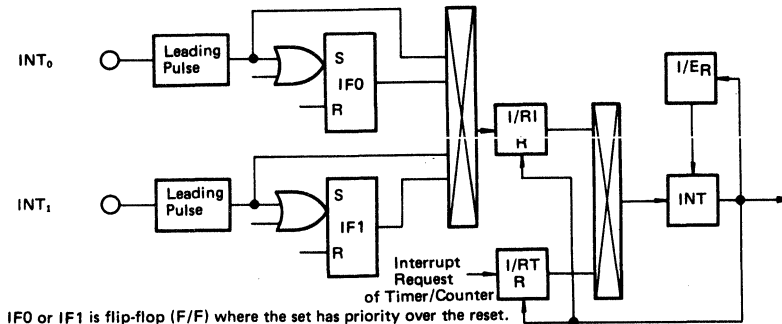


Figure 19 Interrupt Block Diagram

The status is unchanged. (The interrupt is different from general CAL in regard to this matter.)

Stacking of registers is performed by the program. Returning from the interrupt routine is performed in the same way as that from normal subroutine. But it is convenient to use RTNI (Return Interrupt) which sets the I/E simultaneously with RTN.

An interrupt is generated irrespectively of the condition of stack registers, so enough stack registers are needed.

TF, IF0, or IF1 is flip-flop where the set has priority over the reset. It is not reset when the reset instruction is issued simultaneously with OVF of the timer/counter or the leading edge of the input, though the interrupt request is generated and latched into I/RI or I/RT.

The interrupt servicing caused by the interrupt generation is basically the subroutine jump and the jumping location in memory is fixed as:

Interrupt of the timer/counter Page 0 Address 3F (00–3F)
 Interrupt of the inputs Page 1 Address 3F (01–3F)

In addition,

The saving operation of PC → ST1 → ST2 → ST3 → ST4.

I/E reset

● **Interrupt of the Inputs**

Two pins INT₀ and INT₁ have the interrupt request functions. They have the leading pulse generation circuit and the

interrupt mask F/F (IF0, IF1). When IF0 or IF1 is reset, the interrupt request is able to generate interrupt mask release. When INT₀ or INT₁ changes from “0” to “1” (“Low” level → “High” level), the leading pulse is generated and generates the interrupt request. When IF0 or IF1 is set, the interrupt is masked.

The interrupt request generated by the leading pulse is latched in the interrupt request F/F on the input side (I/RI). If interrupt Enable F/F (I/E) is “1”, the interrupt is generated immediately and I/RI is reset. But if Interrupt Enable F/F (I/E) is “0”, I/RI is held at “1” level until it gets into the Interrupt Enable state.

IF0, IF1, INT₀ and INT₁ can be tested by the program. Therefore, they can also be used as normal input pins or latch pins of momentary pulse input.

The interrupt pulse width (at both “High” and “Low” levels) should be more than two-cycle.

● **Interrupt of the Timer/Counter**

The interrupt request of the timer/counter is latched into the interrupt request F/F of the timer (I/RT). Then I/RT operates in the same way as I/RI, but the interrupt of the input has priority over that of the timer. Therefore, the input interrupt is serviced when both I/RI and I/RT are at “1” level (interrupt requests are simultaneously generated). During the input interrupt, I/RT remains set. Thus, after the input interrupt, the timer/counter interrupt can be serviced.

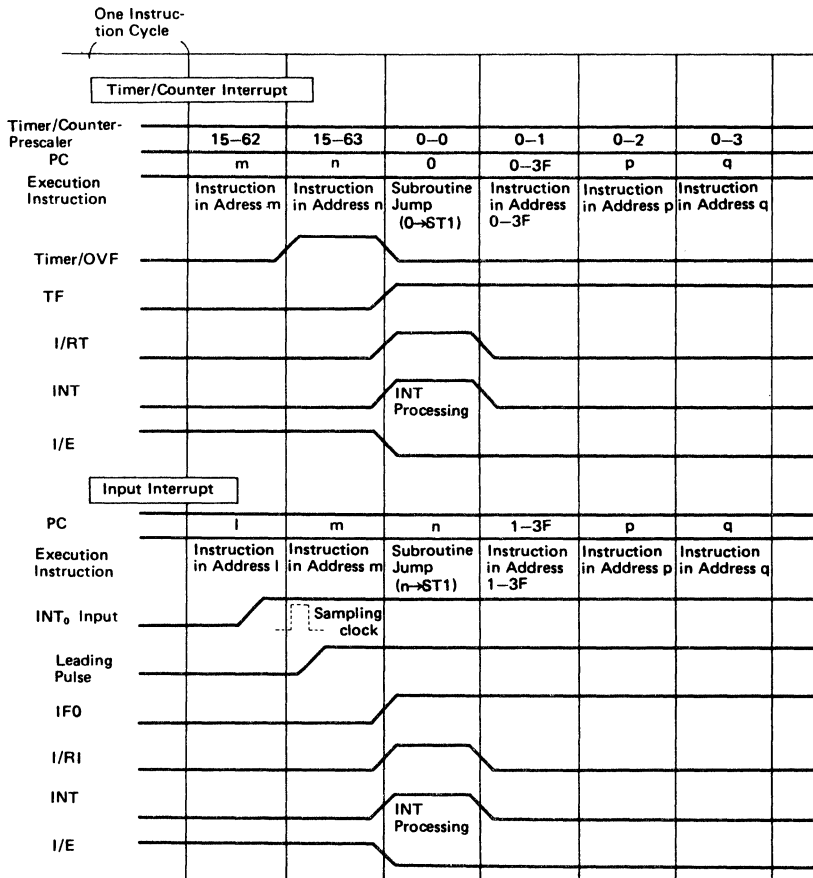


Figure 20 Interrupt Timing Chart

■ LIQUID CRYSTAL DISPLAY

● Liquid Crystal Display Circuit

The LCD-III can directly drive the liquid crystal display panel of static, 1/2 duty factor, 1/3 duty factor and 1/4 duty factor.

The LCD-III has 4 common signal pins and 32 segment signal pins. Further, if liquid crystal driver LSI (HD44100H) is connected to the LCD-III, up to 96 segment signal pins can be extended externally. Thus, in addition to the internal 32 pins, total 128 segment signal pins can be driven.



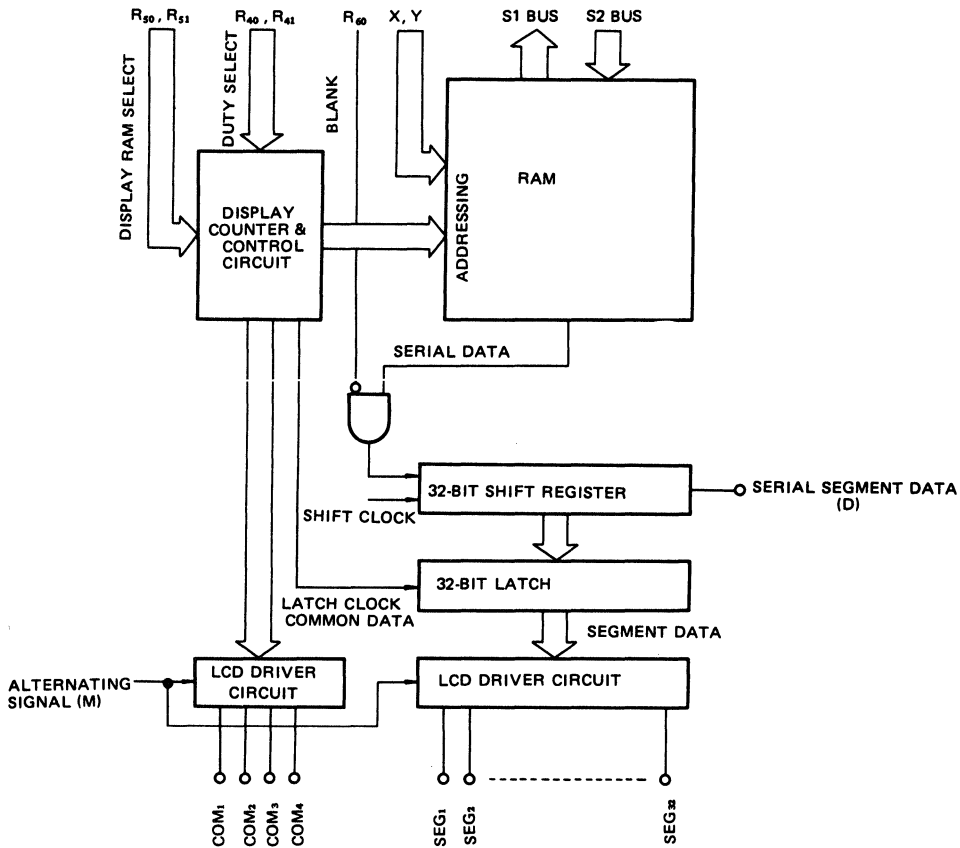


Figure 21 Liquid Crystal Display Circuit Block Diagram

Display is automatically executed by writing segment data into RAM. The RAM reads segment data bit by bit sequentially every one instruction cycle upon receiving address signal from the display counter and the control circuit. Every time common signal is scanned, the RAM reads 128-segment data (SEG₁ to SEG₁₂₈), which corresponds to common signal selected at the next time. In the HD44790, scan of common signal is executed every 256-instruction cycle. Therefore, the data which corresponds to 128-segment is read twice at the same time. And in the HD44795, scan of common signal is executed every 128-instruction cycle. Therefore, 128-segment data is read. The serial data read is converted to parallel data by the shift register

and latch, converted to LCD drive signal by the liquid crystal driver and the output from a segment pin. 32-segment (SEG₁ to SEG₃₂) out of 128-segment serial data is used within the LCD-III, and the rest (96-segment) is output to the liquid crystal driver LSI HD44100H which is connected to the LCD-III and is converted to the LCD drive signal in the HD44100H at the time of designation of with liquid crystal segment output extension. Cycle of the latch clock is 256-instruction cycle in the HD44790 and 128-instruction cycle in the HD44795. In the case of dynamic drive, data at the common side changes synchronously with the latch clock. These display operations are all executed regardless of program.

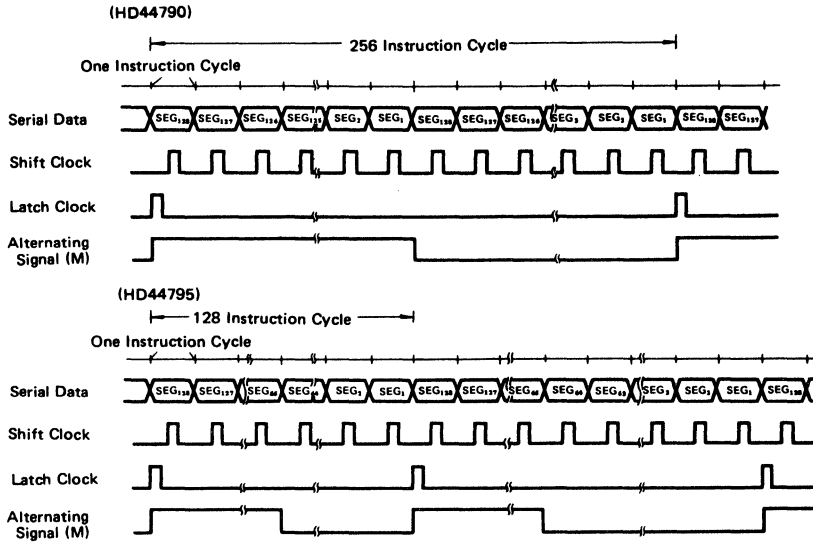


Figure 22 Liquid Crystal Display Circuit Time Chart (To be continued)

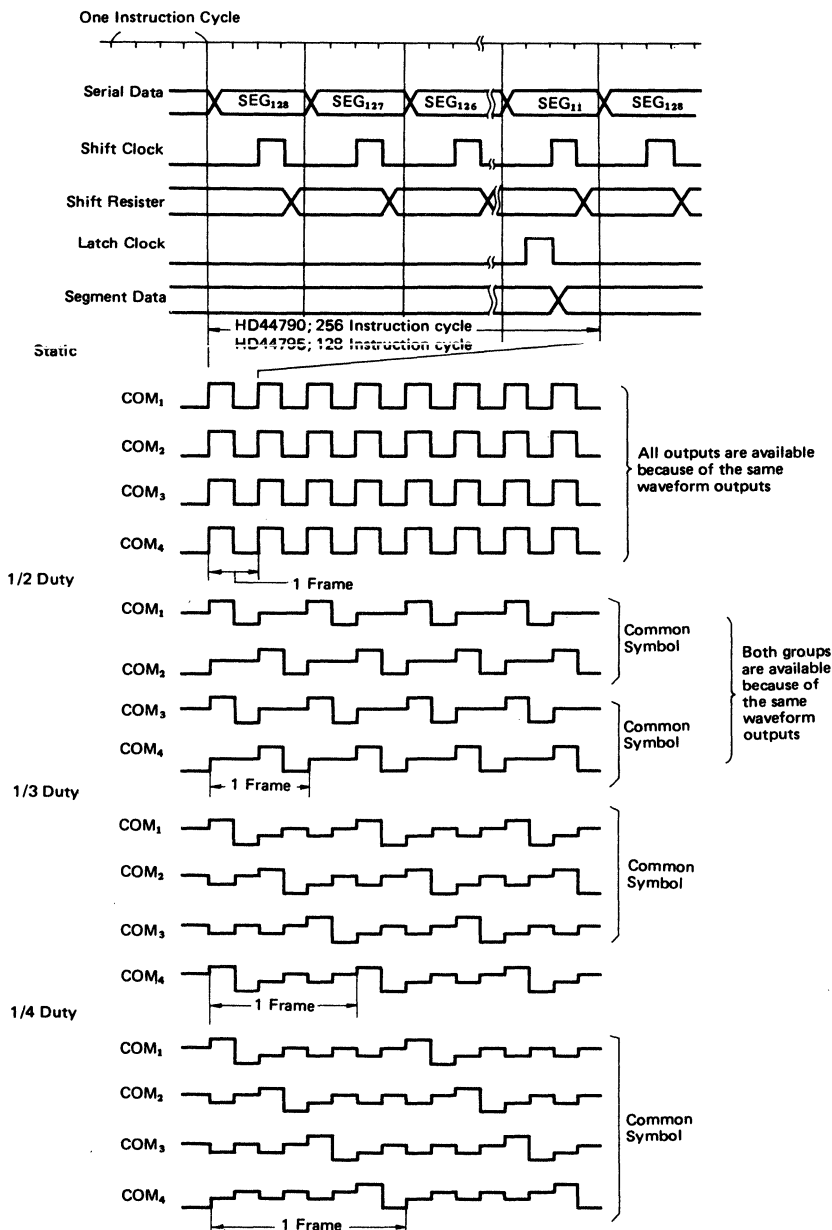


Figure 22 Liquid Crystal Display Circuit Time Chart

• **Liquid Crystal Display Mode Setting Registers**

For selection of the liquid crystal display mode, data I/O registers of R4, R5 and R6 are used.

Table 5 Function of Liquid Crystal Display Mode Setting Registers

Selection of liquid crystal display duty factor (R ₄₀ , R ₄₁)	R ₄₁	R ₄₀	Function
	0	0	Static
	0	1	1/2 duty
	1	0	1/3 duty
	1	1	1/4 duty
Designation of with or without liquid crystal segment output extension (R ₄₂)	R ₄₂	Function	
	0	To be extended (Outputs display data from Channel R1)	
	1	Not to be extended (Channel R1 becomes an ordinary 4-bit data I/O.)	
Liquid crystal display blanking signal (R ₆₀)	R ₆₀	Function	
	0	Outputs RAM data for liquid crystal display as segment signals.	
	1	Segment signals become non-selection status (blanking) regardless of RAM data for liquid crystal display.	
RAM designation for liquid crystal display (R ₅₀ , R ₅₁)	R ₅₁	R ₅₀	Function
	Function varies with liquid crystal display duty factor.		

(NOTE) Liquid crystal display mode at resetting

Since all bits of registers R4, R5 and R6 are set to "1" by the reset function, display mode after resetting becomes as shown below:

Liquid crystal display duty factor: 1/4 duty (R₄₀ = "1", R₄₁ = "1")

Liquid crystal segment output extension: Not extended (R₄₂ = "1")

Designation of liquid crystal display blanking: Display blanking (R₆₀ = "1")

• **Relation between Display RAM and Segment Data**

In the LCD-III, 4 types of display duty factor (static, 1/2 duty, 1/3 duty, and 1/4 duty) can be selected by programs, and correspondence between RAM bits and segment data changes according to these duty factors.

RAM Address				RAM						
X				Y	2 ²	2 ¹	2 ⁰			
6	4	2	0	0	SEG ₆	SEG ₇	SEG ₂	SEG ₁		
				1	SEG ₈	SEG ₉	SEG ₆	SEG ₅		
		3	2	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉			
			3	SEG ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃			
	4	4	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇				
		5	SEG ₂₄	SEG ₂₃	SEG ₂₂	SEG ₂₁				
	6	6	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅				
		7	SEG ₃₂	SEG ₃₁	SEG ₃₀	SEG ₂₉				
	7	5	3	1	8	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	
					9	SEG ₄₀	SEG ₃₉	SEG ₃₈	SEG ₃₇	
					10	SEG ₄₄	SEG ₄₃	SEG ₄₂	SEG ₄₁	
		6	4	2	0	11	SEG ₄₈	SEG ₄₇	SEG ₄₆	SEG ₄₅
						12	SEG ₅₂	SEG ₅₁	SEG ₅₀	SEG ₄₉
						13	SEG ₅₆	SEG ₅₅	SEG ₅₄	SEG ₅₃
		5	4	3	1	14	SEG ₆₀	SEG ₅₉	SEG ₅₈	SEG ₅₇
						15	SEG ₆₄	SEG ₆₃	SEG ₆₂	SEG ₆₁
0						SEG ₆₈	SEG ₆₇	SEG ₆₆	SEG ₆₅	
4		3	2	0	1	SEG ₇₂	SEG ₇₁	SEG ₇₀	SEG ₆₉	
					2	SEG ₇₆	SEG ₇₅	SEG ₇₄	SEG ₇₃	
					3	SEG ₈₀	SEG ₇₉	SEG ₇₈	SEG ₇₇	
3		2	1	0	4	SEG ₈₄	SEG ₈₃	SEG ₈₂	SEG ₈₁	
					5	SEG ₈₈	SEG ₈₇	SEG ₈₆	SEG ₈₅	
					6	SEG ₉₂	SEG ₉₁	SEG ₉₀	SEG ₈₉	
2	1	0	0	7	SEG ₉₆	SEG ₉₅	SEG ₉₄	SEG ₉₃		
				8	SEG ₁₀₀	SEG ₉₉	SEG ₉₈	SEG ₉₇		
				9	SEG ₁₀₄	SEG ₁₀₃	SEG ₁₀₂	SEG ₁₀₁		
1	0	0	0	10	SEG ₁₀₈	SEG ₁₀₇	SEG ₁₀₆	SEG ₁₀₅		
				11	SEG ₁₁₂	SEG ₁₁₁	SEG ₁₁₀	SEG ₁₀₉		
				12	SEG ₁₁₆	SEG ₁₁₅	SEG ₁₁₄	SEG ₁₁₃		
0	0	0	0	13	SEG ₁₂₀	SEG ₁₁₉	SEG ₁₁₈	SEG ₁₁₇		
				14	SEG ₁₂₄	SEG ₁₂₃	SEG ₁₂₂	SEG ₁₂₁		
				15	SEG ₁₂₈	SEG ₁₂₇	SEG ₁₂₆	SEG ₁₂₅		

R ₅₁	0	0	1	1
R ₅₀	0	1	0	1

(NOTE) The SEG₃₃ to SEG₁₂₅ are extended segments.

Figure 23 Relation between RAM for LCD & Segment Data (Static)



RAM Address				RAM					
X				Y	2 ³	2 ²	2 ¹	2 ⁰	
6	4	2	0	0	SEG ₄	SEG ₃	SEG ₂	SEG ₁	COM ₁
				1	SEG ₄	SEG ₃	SEG ₂	SEG ₁	COM ₂
				2	SEG ₆	SEG ₇	SEG ₈	SEG ₉	COM ₁
				3	SEG ₆	SEG ₇	SEG ₈	SEG ₉	COM ₂
				4	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	COM ₁
				5	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉	COM ₂
				6	SEG ₁₈	SEG ₁₅	SEG ₁₄	SEG ₁₃	COM ₁
				7	SEG ₁₈	SEG ₁₈	SEG ₁₄	SEG ₁₃	COM ₂
				8	SEG ₂₀	SEG ₁₈	SEG ₁₈	SEG ₁₇	COM ₁
				9	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇	COM ₂
				10	SEG ₂₄	SEG ₂₃	SEG ₂₂	SEG ₂₁	COM ₁
				11	SEG ₂₄	SEG ₂₃	SEG ₂₂	SEG ₂₁	COM ₂
				12	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	COM ₁
				13	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅	COM ₂
				14	SEG ₃₂	SEG ₃₁	SEG ₃₀	SEG ₂₉	COM ₁
				15	SEG ₃₂	SEG ₃₁	SEG ₃₀	SEG ₂₉	COM ₂
7	5	3	1	0	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	COM ₁
				1	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃	COM ₂
				2	SEG ₄₀	SEG ₃₉	SEG ₃₈	SEG ₃₇	COM ₁
				3	SEG ₄₀	SEG ₃₉	SEG ₃₈	SEG ₃₇	COM ₂
				4	SEG ₄₄	SEG ₄₃	SEG ₄₂	SEG ₄₁	COM ₁
				5	SEG ₄₄	SEG ₄₃	SEG ₄₂	SEG ₄₁	COM ₂
				6	SEG ₄₈	SEG ₄₇	SEG ₄₆	SEG ₄₅	COM ₁
				7	SEG ₄₈	SEG ₄₇	SEG ₄₆	SEG ₄₅	COM ₂
				8	SEG ₅₂	SEG ₅₁	SEG ₅₀	SEG ₄₉	COM ₁
				9	SEG ₅₂	SEG ₅₁	SEG ₅₀	SEG ₄₉	COM ₂
				10	SEG ₅₆	SEG ₅₅	SEG ₅₄	SEG ₅₃	COM ₁
				11	SEG ₅₆	SEG ₅₅	SEG ₅₄	SEG ₅₃	COM ₂
				12	SEG ₆₀	SEG ₅₉	SEG ₅₈	SEG ₅₇	COM ₁
				13	SEG ₆₀	SEG ₅₉	SEG ₅₈	SEG ₅₇	COM ₂
				14	SEG ₆₄	SEG ₆₃	SEG ₆₂	SEG ₆₁	COM ₁
				15	SEG ₆₄	SEG ₆₃	SEG ₆₂	SEG ₆₁	COM ₂
4	6	0	2	0	SEG ₆₈	SEG ₆₇	SEG ₆₆	SEG ₆₅	COM ₁
				1	SEG ₆₈	SEG ₆₇	SEG ₆₆	SEG ₆₅	COM ₂
				2	SEG ₇₂	SEG ₇₁	SEG ₇₀	SEG ₆₉	COM ₁
				3	SEG ₇₂	SEG ₇₁	SEG ₇₀	SEG ₆₉	COM ₂
				4	SEG ₇₆	SEG ₇₅	SEG ₇₄	SEG ₇₃	COM ₁
				5	SEG ₇₆	SEG ₇₅	SEG ₇₄	SEG ₇₃	COM ₂
				6	SEG ₈₀	SEG ₇₉	SEG ₇₈	SEG ₇₇	COM ₁
				7	SEG ₈₀	SEG ₇₉	SEG ₇₈	SEG ₇₇	COM ₂
				8	SEG ₈₄	SEG ₈₃	SEG ₈₂	SEG ₈₁	COM ₁
				9	SEG ₈₄	SEG ₈₃	SEG ₈₂	SEG ₈₁	COM ₂
				10	SEG ₈₈	SEG ₈₇	SEG ₈₆	SEG ₈₅	COM ₁
				11	SEG ₈₈	SEG ₈₇	SEG ₈₆	SEG ₈₅	COM ₂
				12	SEG ₉₂	SEG ₉₁	SEG ₉₀	SEG ₈₉	COM ₁
				13	SEG ₉₂	SEG ₉₁	SEG ₉₀	SEG ₈₉	COM ₂
				14	SEG ₉₆	SEG ₉₅	SEG ₉₄	SEG ₉₃	COM ₁
				15	SEG ₉₆	SEG ₉₅	SEG ₉₄	SEG ₉₃	COM ₂
5	7	1	3	0	SEG ₁₀₀	SEG ₉₉	SEG ₉₈	SEG ₉₇	COM ₁
				1	SEG ₁₀₀	SEG ₉₉	SEG ₉₈	SEG ₉₇	COM ₂
				2	SEG ₁₀₄	SEG ₁₀₃	SEG ₁₀₂	SEG ₁₀₁	COM ₁
				3	SEG ₁₀₄	SEG ₁₀₃	SEG ₁₀₂	SEG ₁₀₁	COM ₂
				4	SEG ₁₀₈	SEG ₁₀₇	SEG ₁₀₆	SEG ₁₀₅	COM ₁
				5	SEG ₁₀₈	SEG ₁₀₇	SEG ₁₀₆	SEG ₁₀₅	COM ₂
				6	SEG ₁₁₂	SEG ₁₁₁	SEG ₁₁₀	SEG ₁₀₉	COM ₁
				7	SEG ₁₁₂	SEG ₁₁₁	SEG ₁₁₀	SEG ₁₀₉	COM ₂
				8	SEG ₁₁₆	SEG ₁₁₅	SEG ₁₁₄	SEG ₁₁₃	COM ₁
				9	SEG ₁₁₆	SEG ₁₁₅	SEG ₁₁₄	SEG ₁₁₃	COM ₂
				10	SEG ₁₂₀	SEG ₁₁₉	SEG ₁₁₈	SEG ₁₁₇	COM ₁
				11	SEG ₁₂₀	SEG ₁₁₉	SEG ₁₁₈	SEG ₁₁₇	COM ₂
				12	SEG ₁₂₄	SEG ₁₂₃	SEG ₁₂₂	SEG ₁₂₁	COM ₁
				13	SEG ₁₂₄	SEG ₁₂₃	SEG ₁₂₂	SEG ₁₂₁	COM ₂
				14	SEG ₁₂₈	SEG ₁₂₇	SEG ₁₂₆	SEG ₁₂₅	COM ₁
				15	SEG ₁₂₈	SEG ₁₂₇	SEG ₁₂₆	SEG ₁₂₅	COM ₂

R ₅₁	0	0	1	1
R ₅₀	0	1	0	1

(NOTE) The SEG₃₃ to SEG₁₂₆ are extended segments.

Figure 24 Relation between RAM for LCD & Segment Data (1/2 Duty, 1/2 Bias)



RAM Address				RAM			
X	Y	2 ³	2 ²	2 ¹	2 ⁰		
6	4	2	0	0	SEG ₁	SEG ₁	SEG ₁
				1	SEG ₂	SEG ₂	SEG ₂
				2	SEG ₃	SEG ₃	SEG ₃
				3	SEG ₄	SEG ₄	SEG ₄
				4	SEG ₅	SEG ₅	SEG ₅
				5	SEG ₆	SEG ₆	SEG ₆
				6	SEG ₇	SEG ₇	SEG ₇
				7	SEG ₈	SEG ₈	SEG ₈
				8	SEG ₉	SEG ₉	SEG ₉
				9	SEG ₁₀	SEG ₁₀	SEG ₁₀
				10	SEG ₁₁	SEG ₁₁	SEG ₁₁
				11	SEG ₁₂	SEG ₁₂	SEG ₁₂
				12	SEG ₁₃	SEG ₁₃	SEG ₁₃
				13	SEG ₁₄	SEG ₁₄	SEG ₁₄
				14	SEG ₁₅	SEG ₁₅	SEG ₁₅
				15	SEG ₁₆	SEG ₁₆	SEG ₁₆
7	5	3	1	0	SEG ₁₇	SEG ₁₇	SEG ₁₇
				1	SEG ₁₈	SEG ₁₈	SEG ₁₈
				2	SEG ₁₉	SEG ₁₉	SEG ₁₉
				3	SEG ₂₀	SEG ₂₀	SEG ₂₀
				4	SEG ₂₁	SEG ₂₁	SEG ₂₁
				5	SEG ₂₂	SEG ₂₂	SEG ₂₂
				6	SEG ₂₃	SEG ₂₃	SEG ₂₃
				7	SEG ₂₄	SEG ₂₄	SEG ₂₄
				8	SEG ₂₅	SEG ₂₅	SEG ₂₅
				9	SEG ₂₆	SEG ₂₆	SEG ₂₆
				10	SEG ₂₇	SEG ₂₇	SEG ₂₇
				11	SEG ₂₈	SEG ₂₈	SEG ₂₈
				12	SEG ₂₉	SEG ₂₉	SEG ₂₉
				13	SEG ₃₀	SEG ₃₀	SEG ₃₀
				14	SEG ₃₁	SEG ₃₁	SEG ₃₁
				15	SEG ₃₂	SEG ₃₂	SEG ₃₂
4	6	0	2	0	SEG ₃₃	SEG ₃₃	SEG ₃₃
				1	SEG ₃₄	SEG ₃₄	SEG ₃₄
				2	SEG ₃₅	SEG ₃₅	SEG ₃₅
				3	SEG ₃₆	SEG ₃₆	SEG ₃₆
				4	SEG ₃₇	SEG ₃₇	SEG ₃₇
				5	SEG ₃₈	SEG ₃₈	SEG ₃₈
				6	SEG ₃₉	SEG ₃₉	SEG ₃₉
				7	SEG ₄₀	SEG ₄₀	SEG ₄₀
				8	SEG ₄₁	SEG ₄₁	SEG ₄₁
				9	SEG ₄₂	SEG ₄₂	SEG ₄₂
				10	SEG ₄₃	SEG ₄₃	SEG ₄₃
				11	SEG ₄₄	SEG ₄₄	SEG ₄₄
				12	SEG ₄₅	SEG ₄₅	SEG ₄₅
				13	SEG ₄₆	SEG ₄₆	SEG ₄₆
				14	SEG ₄₇	SEG ₄₇	SEG ₄₇
				15	SEG ₄₈	SEG ₄₈	SEG ₄₈
5	7	1	3	0	SEG ₄₉	SEG ₄₉	SEG ₄₉
				1	SEG ₅₀	SEG ₅₀	SEG ₅₀
				2	SEG ₅₁	SEG ₅₁	SEG ₅₁
				3	SEG ₅₂	SEG ₅₂	SEG ₅₂
				4	SEG ₅₃	SEG ₅₃	SEG ₅₃
				5	SEG ₅₄	SEG ₅₄	SEG ₅₄
				6	SEG ₅₅	SEG ₅₅	SEG ₅₅
				7	SEG ₅₆	SEG ₅₆	SEG ₅₆
				8	SEG ₅₇	SEG ₅₇	SEG ₅₇
				9	SEG ₅₈	SEG ₅₈	SEG ₅₈
				10	SEG ₅₉	SEG ₅₉	SEG ₅₉
				11	SEG ₆₀	SEG ₆₀	SEG ₆₀
				12	SEG ₆₁	SEG ₆₁	SEG ₆₁
				13	SEG ₆₂	SEG ₆₂	SEG ₆₂
				14	SEG ₆₃	SEG ₆₃	SEG ₆₃
				15	SEG ₆₄	SEG ₆₄	SEG ₆₄

RAM Address				RAM			
X	Y	2 ³	2 ²	2 ¹	2 ⁰		
2	0	6	4	0	SEG ₆₅	SEG ₆₅	SEG ₆₅
				1	SEG ₆₆	SEG ₆₆	SEG ₆₆
				2	SEG ₆₇	SEG ₆₇	SEG ₆₇
				3	SEG ₆₈	SEG ₆₈	SEG ₆₈
				4	SEG ₆₉	SEG ₆₉	SEG ₆₉
				5	SEG ₇₀	SEG ₇₀	SEG ₇₀
				6	SEG ₇₁	SEG ₇₁	SEG ₇₁
				7	SEG ₇₂	SEG ₇₂	SEG ₇₂
				8	SEG ₇₃	SEG ₇₃	SEG ₇₃
				9	SEG ₇₄	SEG ₇₄	SEG ₇₄
				10	SEG ₇₅	SEG ₇₅	SEG ₇₅
				11	SEG ₇₆	SEG ₇₆	SEG ₇₆
				12	SEG ₇₇	SEG ₇₇	SEG ₇₇
				13	SEG ₇₈	SEG ₇₈	SEG ₇₈
				14	SEG ₇₉	SEG ₇₉	SEG ₇₉
				15	SEG ₈₀	SEG ₈₀	SEG ₈₀
3	1	7	5	0	SEG ₈₁	SEG ₈₁	SEG ₈₁
				1	SEG ₈₂	SEG ₈₂	SEG ₈₂
				2	SEG ₈₃	SEG ₈₃	SEG ₈₃
				3	SEG ₈₄	SEG ₈₄	SEG ₈₄
				4	SEG ₈₅	SEG ₈₅	SEG ₈₅
				5	SEG ₈₆	SEG ₈₆	SEG ₈₆
				6	SEG ₈₇	SEG ₈₇	SEG ₈₇
				7	SEG ₈₈	SEG ₈₈	SEG ₈₈
				8	SEG ₈₉	SEG ₈₉	SEG ₈₉
				9	SEG ₉₀	SEG ₉₀	SEG ₉₀
				10	SEG ₉₁	SEG ₉₁	SEG ₉₁
				11	SEG ₉₂	SEG ₉₂	SEG ₉₂
				12	SEG ₉₃	SEG ₉₃	SEG ₉₃
				13	SEG ₉₄	SEG ₉₄	SEG ₉₄
				14	SEG ₉₅	SEG ₉₅	SEG ₉₅
				15	SEG ₉₆	SEG ₉₆	SEG ₉₆
0	2	4	6	0	SEG ₉₇	SEG ₉₇	SEG ₉₇
				1	SEG ₉₈	SEG ₉₈	SEG ₉₈
				2	SEG ₉₉	SEG ₉₉	SEG ₉₉
				3	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀
				4	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁
				5	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂
				6	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃
				7	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄
				8	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅
				9	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆
				10	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇
				11	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈
				12	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉
				13	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀
				14	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁
				15	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂
1	3	5	7	0	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃
				1	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄
				2	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅
				3	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆
				4	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇
				5	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈
				6	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉
				7	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀
				8	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁
				9	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂
				10	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃
				11	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄
				12	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅
				13	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆
				14	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇
				15	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈

R ₅₁	0	0	1	1	COM ₃	COM ₂	COM ₁
R ₅₀	0	1	0	1			

R ₅₀	0	0	1	1	COM ₃	COM ₂	COM ₁
R ₅₁	0	1	0	1			

(NOTE) The SEG₃₃ to SEG₁₂₈ are extended segments.

Figure 25 Relation between RAM for Liquid Crystal Display and Segment Data (1/3 Duty, 1/3 Bias Drive)



LCD—III (HD44790, HD44795)

RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
6	4	2	0	0	SEG ₁	SEG ₁	SEG ₁	SEG ₁
				1	SEG ₂	SEG ₂	SEG ₂	SEG ₂
				2	SEG ₃	SEG ₃	SEG ₃	SEG ₃
				3	SEG ₄	SEG ₄	SEG ₄	SEG ₄
				4	SEG ₅	SEG ₅	SEG ₅	SEG ₅
				5	SEG ₆	SEG ₆	SEG ₆	SEG ₆
				6	SEG ₇	SEG ₇	SEG ₇	SEG ₇
				7	SEG ₈	SEG ₈	SEG ₈	SEG ₈
				8	SEG ₉	SEG ₉	SEG ₉	SEG ₉
				9	SEG ₁₀	SEG ₁₀	SEG ₁₀	SEG ₁₀
				10	SEG ₁₁	SEG ₁₁	SEG ₁₁	SEG ₁₁
				11	SEG ₁₂	SEG ₁₂	SEG ₁₂	SEG ₁₂
				12	SEG ₁₃	SEG ₁₃	SEG ₁₃	SEG ₁₃
				13	SEG ₁₄	SEG ₁₄	SEG ₁₄	SEG ₁₄
				14	SEG ₁₅	SEG ₁₅	SEG ₁₅	SEG ₁₅
				15	SEG ₁₆	SEG ₁₆	SEG ₁₆	SEG ₁₆
7	5	3	1	0	SEG ₁₇	SEG ₁₇	SEG ₁₇	SEG ₁₇
				1	SEG ₁₈	SEG ₁₈	SEG ₁₈	SEG ₁₈
				2	SEG ₁₉	SEG ₁₉	SEG ₁₉	SEG ₁₉
				3	SEG ₂₀	SEG ₂₀	SEG ₂₀	SEG ₂₀
				4	SEG ₂₁	SEG ₂₁	SEG ₂₁	SEG ₂₁
				5	SEG ₂₂	SEG ₂₂	SEG ₂₂	SEG ₂₂
				6	SEG ₂₃	SEG ₂₃	SEG ₂₃	SEG ₂₃
				7	SEG ₂₄	SEG ₂₄	SEG ₂₄	SEG ₂₄
				8	SEG ₂₅	SEG ₂₅	SEG ₂₅	SEG ₂₅
				9	SEG ₂₆	SEG ₂₆	SEG ₂₆	SEG ₂₆
				10	SEG ₂₇	SEG ₂₇	SEG ₂₇	SEG ₂₇
				11	SEG ₂₈	SEG ₂₈	SEG ₂₈	SEG ₂₈
				12	SEG ₂₉	SEG ₂₉	SEG ₂₉	SEG ₂₉
				13	SEG ₃₀	SEG ₃₀	SEG ₃₀	SEG ₃₀
				14	SEG ₃₁	SEG ₃₁	SEG ₃₁	SEG ₃₁
				15	SEG ₃₂	SEG ₃₂	SEG ₃₂	SEG ₃₂
4	6	0	2	0	SEG ₃₃	SEG ₃₃	SEG ₃₃	SEG ₃₃
				1	SEG ₃₄	SEG ₃₄	SEG ₃₄	SEG ₃₄
				2	SEG ₃₅	SEG ₃₅	SEG ₃₅	SEG ₃₅
				3	SEG ₃₆	SEG ₃₆	SEG ₃₆	SEG ₃₆
				4	SEG ₃₇	SEG ₃₇	SEG ₃₇	SEG ₃₇
				5	SEG ₃₈	SEG ₃₈	SEG ₃₈	SEG ₃₈
				6	SEG ₃₉	SEG ₃₉	SEG ₃₉	SEG ₃₉
				7	SEG ₄₀	SEG ₄₀	SEG ₄₀	SEG ₄₀
				8	SEG ₄₁	SEG ₄₁	SEG ₄₁	SEG ₄₁
				9	SEG ₄₂	SEG ₄₂	SEG ₄₂	SEG ₄₂
				10	SEG ₄₃	SEG ₄₃	SEG ₄₃	SEG ₄₃
				11	SEG ₄₄	SEG ₄₄	SEG ₄₄	SEG ₄₄
				12	SEG ₄₅	SEG ₄₅	SEG ₄₅	SEG ₄₅
				13	SEG ₄₆	SEG ₄₆	SEG ₄₆	SEG ₄₆
				14	SEG ₄₇	SEG ₄₇	SEG ₄₇	SEG ₄₇
				15	SEG ₄₈	SEG ₄₈	SEG ₄₈	SEG ₄₈
5	7	1	3	0	SEG ₄₉	SEG ₄₉	SEG ₄₉	SEG ₄₉
				1	SEG ₅₀	SEG ₅₀	SEG ₅₀	SEG ₅₀
				2	SEG ₅₁	SEG ₅₁	SEG ₅₁	SEG ₅₁
				3	SEG ₅₂	SEG ₅₂	SEG ₅₂	SEG ₅₂
				4	SEG ₅₃	SEG ₅₃	SEG ₅₃	SEG ₅₃
				5	SEG ₅₄	SEG ₅₄	SEG ₅₄	SEG ₅₄
				6	SEG ₅₅	SEG ₅₅	SEG ₅₅	SEG ₅₅
				7	SEG ₅₆	SEG ₅₆	SEG ₅₆	SEG ₅₆
				8	SEG ₅₇	SEG ₅₇	SEG ₅₇	SEG ₅₇
				9	SEG ₅₈	SEG ₅₈	SEG ₅₈	SEG ₅₈
				10	SEG ₅₉	SEG ₅₉	SEG ₅₉	SEG ₅₉
				11	SEG ₆₀	SEG ₆₀	SEG ₆₀	SEG ₆₀
				12	SEG ₆₁	SEG ₆₁	SEG ₆₁	SEG ₆₁
				13	SEG ₆₂	SEG ₆₂	SEG ₆₂	SEG ₆₂
				14	SEG ₆₃	SEG ₆₃	SEG ₆₃	SEG ₆₃
				15	SEG ₆₄	SEG ₆₄	SEG ₆₄	SEG ₆₄

RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
2	0	6	4	0	SEG ₆₅	SEG ₆₅	SEG ₆₅	SEG ₆₅
				1	SEG ₆₆	SEG ₆₆	SEG ₆₆	SEG ₆₆
				2	SEG ₆₇	SEG ₆₇	SEG ₆₇	SEG ₆₇
				3	SEG ₆₈	SEG ₆₈	SEG ₆₈	SEG ₆₈
				4	SEG ₆₉	SEG ₆₉	SEG ₆₉	SEG ₆₉
				5	SEG ₇₀	SEG ₇₀	SEG ₇₀	SEG ₇₀
				6	SEG ₇₁	SEG ₇₁	SEG ₇₁	SEG ₇₁
				7	SEG ₇₂	SEG ₇₂	SEG ₇₂	SEG ₇₂
				8	SEG ₇₃	SEG ₇₃	SEG ₇₃	SEG ₇₃
				9	SEG ₇₄	SEG ₇₄	SEG ₇₄	SEG ₇₄
				10	SEG ₇₅	SEG ₇₅	SEG ₇₅	SEG ₇₅
				11	SEG ₇₆	SEG ₇₆	SEG ₇₆	SEG ₇₆
				12	SEG ₇₇	SEG ₇₇	SEG ₇₇	SEG ₇₇
				13	SEG ₇₈	SEG ₇₈	SEG ₇₈	SEG ₇₈
				14	SEG ₇₉	SEG ₇₉	SEG ₇₉	SEG ₇₉
				15	SEG ₈₀	SEG ₈₀	SEG ₈₀	SEG ₈₀
3	1	7	5	0	SEG ₈₁	SEG ₈₁	SEG ₈₁	SEG ₈₁
				1	SEG ₈₂	SEG ₈₂	SEG ₈₂	SEG ₈₂
				2	SEG ₈₃	SEG ₈₃	SEG ₈₃	SEG ₈₃
				3	SEG ₈₄	SEG ₈₄	SEG ₈₄	SEG ₈₄
				4	SEG ₈₅	SEG ₈₅	SEG ₈₅	SEG ₈₅
				5	SEG ₈₆	SEG ₈₆	SEG ₈₆	SEG ₈₆
				6	SEG ₈₇	SEG ₈₇	SEG ₈₇	SEG ₈₇
				7	SEG ₈₈	SEG ₈₈	SEG ₈₈	SEG ₈₈
				8	SEG ₈₉	SEG ₈₉	SEG ₈₉	SEG ₈₉
				9	SEG ₉₀	SEG ₉₀	SEG ₉₀	SEG ₉₀
				10	SEG ₉₁	SEG ₉₁	SEG ₉₁	SEG ₉₁
				11	SEG ₉₂	SEG ₉₂	SEG ₉₂	SEG ₉₂
				12	SEG ₉₃	SEG ₉₃	SEG ₉₃	SEG ₉₃
				13	SEG ₉₄	SEG ₉₄	SEG ₉₄	SEG ₉₄
				14	SEG ₉₅	SEG ₉₅	SEG ₉₅	SEG ₉₅
				15	SEG ₉₆	SEG ₉₆	SEG ₉₆	SEG ₉₆
0	2	4	6	0	SEG ₉₇	SEG ₉₇	SEG ₉₇	SEG ₉₇
				1	SEG ₉₈	SEG ₉₈	SEG ₉₈	SEG ₉₈
				2	SEG ₉₉	SEG ₉₉	SEG ₉₉	SEG ₉₉
				3	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀
				4	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁
				5	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂
				6	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃
				7	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄
				8	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅
				9	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆
				10	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇
				11	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈
				12	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉
				13	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀
				14	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁
				15	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂
1	3	5	7	0	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃
				1	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄
				2	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅
				3	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆
				4	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇
				5	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈
				6	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉
				7	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀
				8	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁
				9	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂
				10	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃
				11	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄
				12	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅
				13	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆
				14	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇
				15	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈

R ₅₁	0	0	1	1	COM ₄	COM ₃	COM ₂	COM ₁
R ₆₀	0	1	0	1				

R ₅₀	0	0	1	1	COM ₄	COM ₃	COM ₂	COM ₁
R ₅₁	0	1	0	1				

(NOTE) The SEG₃₃ to SEG₁₂₈ are extended segments.

Figure 26 Relation between RAM for Liquid Crystal Display and Segment Data (1/4 Duty, 1/3 Bias Drive)



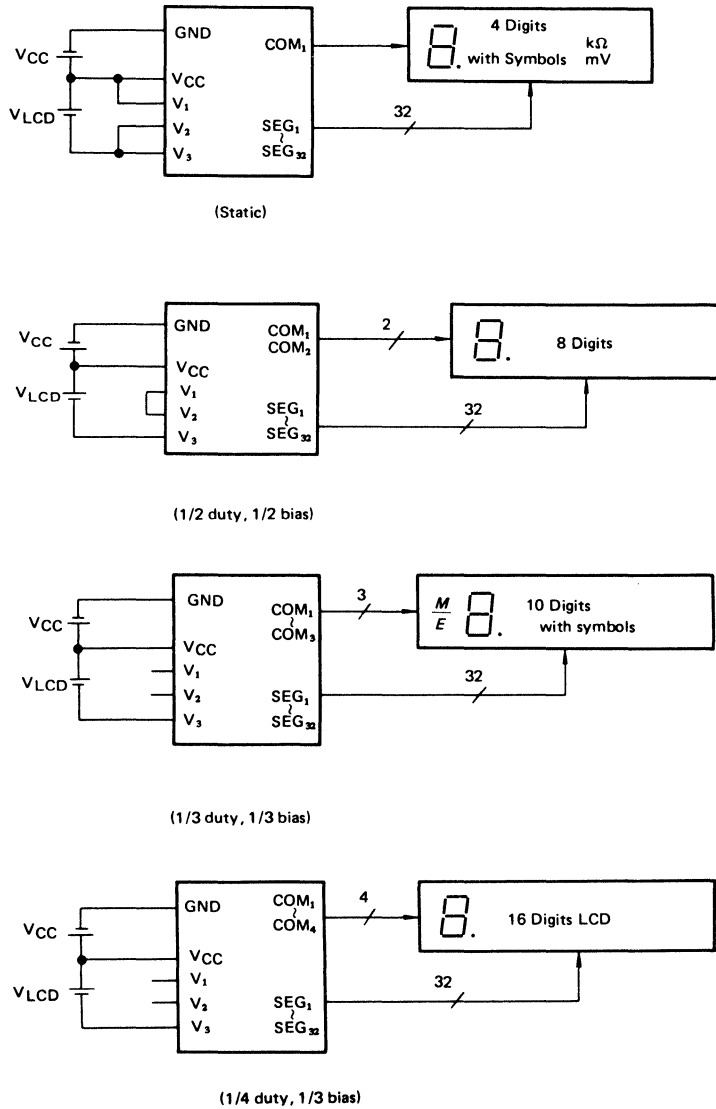


Figure 27 LCD Wiring Samples

● Extension of Display Function

Number of display digits can be increased by externally connecting an LCD driver LSI HD44100H to the LCD-III.

The HD44100H consists of shift registers and latch and liquid crystal drive circuit. When connected with the LCD-III, the HD44100H is used as a circuit for segment. In the LCD-III, 128 segments display data is sent to the 32-bit shift register from RAM constantly. When R₄₂ is set to "0", the R₁ channel outputs the 32nd stage output D of the shift register, shift clock CL₂, latch clock CL₁ and AC signal M. Therefore, up to 96 segment pins of SEG₃₃ to SEG₁₂₈ can be added by directly connecting the HD44100H.

■ RESET FUNCTION

The LCD-III can be reset by setting the reset pin to "1"

(High) and its operation starts when the pin is set to "0" (Low). Also an automatic reset function (internal reset circuit) that operates when power is turned on is provided.

However, note that in the case of internal reset circuit the rise time of a power supply has a restriction. The LCD-III internal state is set as follows by the reset function:

The program counter is set to Address 3F of Page 31.

IR/I, IR/T, I/E and CF are reset to "0".

IFO, IF1 and TF are set to "1".

All bits of data I/O register, discrete I/O output latches

(R₁, R₂, R₃ and D₀ to D₁₅) are set to "1".

Liquid crystal display . . . All bits of display mode setting registers (data I/O registers) R₄, R₅ and R₆ are set to "1".

When internal halt mode, RAM data is not retained after reset.

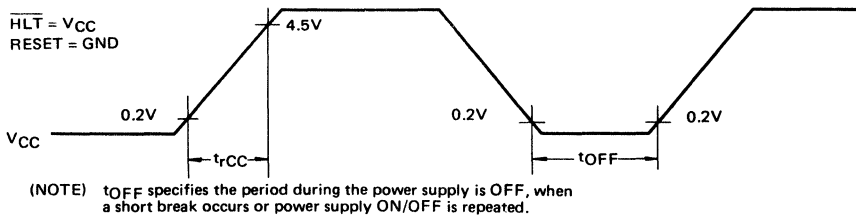


Figure 28 Power Supply Condition Using the Built-in Reset Circuit

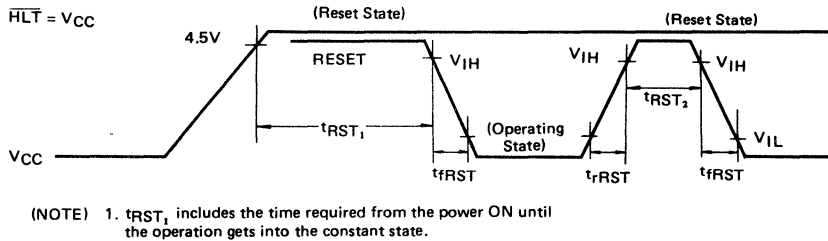


Figure 29 Reset Input Condition Using an External Reset Circuit

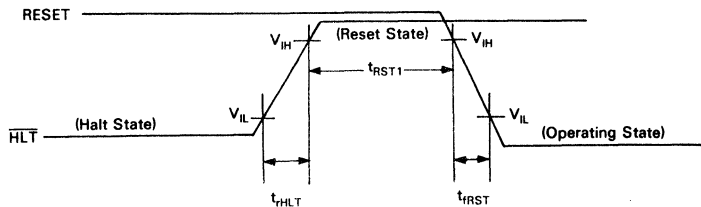


Figure 30 RESET Timing when Releasing Halt (Ceramic Filter Oscillation)



■ HALT FUNCTION

The LCD-III is provided with halt function. The halt function reduces power consumption in the halt state by temporarily stopping all statuses including RAM. When halt is released, operation restarts from the state immediately before the halt.

(Caution at the halt)

When the LCD-III goes into halt state, segment pins (SEG₁ to SEG₃₂) and common pins (COM₁ to COM₄) become the same potential and display goes out. However, in order to reduce power consumption during halt, disconnect the voltage applied to liquid crystal power supply V₃. Since there are dividing resistors among V₁, V₂, and V₃, current of up to 50μA flows if voltage is applied between V_{CC} and V₃ in the same way as normal operation.

The user can select one of the following I/O status at the time of halt based on the "MASK OPTION LIST" when ordering ROM:

- i) All I/O statuses are kept as the state immediately before the halt.
- ii) All I/O statuses are held in the high impedance state (both PMOS and NMOS are off, and pull-up MOS is off).

There are the following two types of halt:

- 1) External Halt (Halt state is generated by using $\overline{\text{HLT}}$ pin) All operations stop when the $\overline{\text{HLT}}$ pin is set to the "0" level (Low). When the $\overline{\text{HLT}}$ pin is set to the "1" level (High), operation restarts from the state immediately before the halt.

- 2) Internal Halt (Halt state is generated by programs)

The user can select availability of internal halt at ROM ordering based on the "MASK OPTION LIST". When internal halt is selected, timer crystal should be attached externally. Therefore, the D₁₄/XO and D₁₅/XI pins should not be used as general I/Os, but as XO and XI pins for connecting crystal oscillator.

Resetting of the D₁₅ latch by RED instruction generates internal halt state. Overflow signals of the prescaler return the LCD-III from internal halt. 16Hz overflow signals are output from the prescaler if a crystal oscillator of 32.768 kHz is connected to the D₁₄/XO and D₁₅/XI pins. When an overflow signal is issued, the D₁₅ latch is set to "1" from "0", the LCD-III returns from halt state, adds 1 to the timer register, and execution restarts from the instruction next to the RED instruction.

Note that external halt caused by the $\overline{\text{HLT}}$ pin cannot be released by prescaler overflow signals.

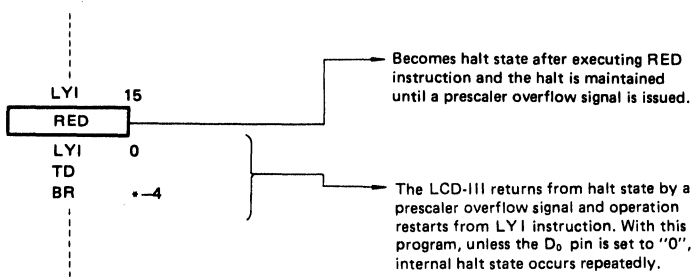


Figure 31 Program example in the Internal Halt Mode

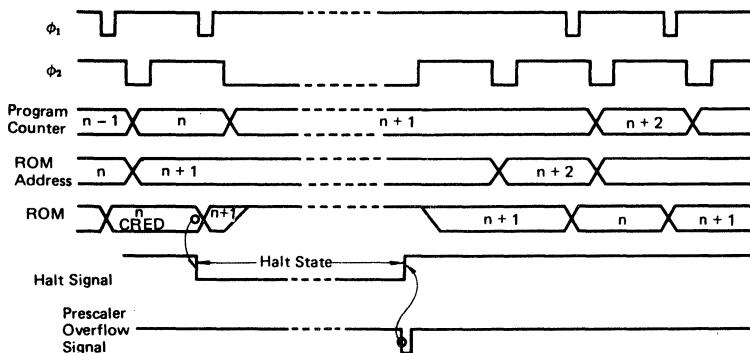


Figure 32 Internal Halt Timing Chart



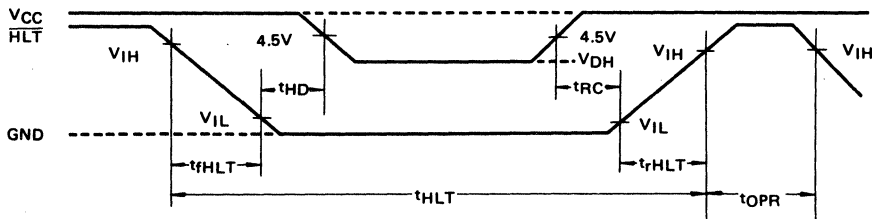


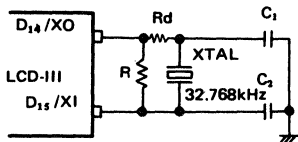
Figure 33 External Halt Timing Chart

■ CRYSTAL OSCILLATION CIRCUIT FOR TIMER

The user can specify whether or not the timer crystal should be externally attached by the "MASK OPTION LIST". By

externally attaching a crystal oscillator of 32.768 kHz to the D₁₄/XO and D₁₅/XI pins, use₁ can set the prescaler clock to 1,024Hz and timer interrupt cycle to max. of 1 sec.

This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.



$C_1 = C_2 = 20\text{pF} \pm 10\%$

$R = 10\text{M}\Omega \pm 10\%$

$R_d = 200\text{k}\Omega \pm 10\%$

(NOTE)

The crystal oscillator, resistor R, Rd and load capacitor C₁ and C₂ should be placed as close as possible to the LCD-III. Induction of external noise to D₁₄/XO and D₁₅/XI may disturb normal oscillation.

Figure 34 Crystal Oscillator Circuit

No.	Halt state	With or without timer crystal	D ₁₄ , D ₁₅ (XO, XI)	Function
1	External halt	Externally attached crystal (32.768 kHz)	Pins for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. Up to 1 second can be set as the timer interruption cycle.
2	External halt	(Without crystal) Internal clock of LSI	Used as general I/O	The prescaler clock becomes a typ. of 100 kHz, and the timer interruption cycle can be set to max. of 97.66 Hz.
3	Internal and external halt	Externally attached crystal (32.768 kHz)	Pins for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. This signal performs the LCD-III return from internal halt. (Return from external halt is not possible by the prescaler overflow signal.)

■ **MASK OPTION**

The following type mask option is available.

● **I/O Pin Format Select one of A, B or C**

A: Without pull-up MOS

B: With pull-up MOS

C: CMOS output

(Note) External input is not permitted if CMOS output is selected in the case of I/O common pins.

● **I/O Status in the Halt State Select Enable or Disable**

Enable — Output Maintained in the status before halt.

— Pull-up MOS . . . ON

— Input . . . Unrelated to halt state

(Since Pull-up MOS is ON, if halt occurs when output is "0" (Low) level (NMOS; ON), pull-up MOS current always flows. If input changes, transient current flows through the input circuit. Also, current flows through the input pull-up MOS. These currents are added to standby power supply current (or halt current).)

Disable — Output . . . NMOS output; OFF

— CMOS output; High impedance
(NMOS, PMOS; OFF)

— Pull-up MOS . . . OFF

— Input . . . Input circuit; OFF

(Both input and output become high impedance

state. Since the input circuit is turned off, input change does not lead to flow other than the standby power supply current or halt current.)

● **With or without Externally Attached Timer Crystal**

Without timer crystal . . .

The D₁₄ and D₁₅ can be used as general I/O pins. Select one of A, B or C in the D₁₄/D₁₅ column of the I/O format specifications.

With timer crystal . . .

The D₁₄ and D₁₅ cannot be used as general I/O terminals.

Therefore, leave the D₁₄/D₁₅ column in blank.

● **With or without Internal Halt**

With internal halt . . .

When internal halt is specified, the timer crystal must also be specified.

Without internal halt . . .

Without internal halt can be specified regardless of existing the crystal for timer.

Group	Mnemonic code	Function	Status
Compare	MNEI i	M ≠ i	NZ
	YNEI i	Y ≠ i	NZ
	ANEM	A ≠ M	NZ
	BNEM	B ≠ M	NZ
	ALEI i	A ≤ i	NB
	ALEM	A ≤ M	NB
	BLEM	B ≤ M	NB
RAM bit Manipulation	SEM n	1 → M (n)	
	REM n	0 → M (n)	
	TM n	Test M (n)	M (n)
ROM Address	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt	SEIE	1 → I/E	
	SEIF0	1 → IF0	
	SEIF1	1 → IF1	
	SETF	1 → TF	
	SECF	1 → CF	
	REIE	0 → I/E	
	REIF0	0 → IF0	
	REIF1	0 → IF1	
	RETF	0 → TF	
	RECF	0 → CF	
	TIO	Test INT ₀	INT ₀
	TI1	Test INT ₁	INT ₁
	TIF0	Test IF0	IF ₀
	TIF1	Test IF1	IF ₁
	TTF	Test TF	TF
	LTI i	i → Timer/Counter	
LTA	A → Timer/Counter		
LAT	Timer/Counter → A		
RTNI	Return Interrupt		
Input/Output (Display Control)	SED	1 → D (Y)	
	RED	0 → D (Y)	
	TD	Test D (Y)	D (Y)
	SEDD n	1 → D (n)	
	REDD n	0 → D (n)	
	LAR p	R (p) → A	
	LBR p	R (p) → B	
	LRA p	A → R (p)	
	LRB p	B → R (p)	
	Pp	Pattern Generation	
NOP	No Operation		

LCD—III (HD44790, HD44795)

(NOTE) 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	Instruction execution, X ↔ SPX
Mnemonic with Y	Instruction execution, Y ↔ SPY
Mnemonic with XY	Instruction execution, X ↔ SPX, Y ↔ SPY
[Example] LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY

2. Status column shows the factor which affects status by the instruction of status change.

NZ	ALU	Not Zero
C	ALU	Overflow in Addition/Carry
NB	ALU	Overflow in Subtraction/No Borrow
except above		Content of status column affects status directly.

3. Carry flip-flop is not always affected by executing the instruction which affects the Status.

Instructions which affect Carry flip-flop are eight as follows.

AMC	SEC
SMC	REC
DAA	ROTL
DAS	ROTR

4. All instructions except for P are executed in single cycle.

P is executed in 2 cycle.

LCD-III Mask Option List

- 5V Operation
 3V Operation

☆ Mark "✓" in "□" for the selected spec.

Date	
Customer	
Dept.	
Name	
ROM CODE ID	
LSI Type Name (entered by Hitachi)	

(1) I/O Option

Pin Name	I/O	I/O Option			Remarks	Pin Name	I/O	I/O Option			Remarks
		A	B	C				A	B	C	
D ₀	I/O					R ₀₀	I				
D ₁	I/O					R ₀₁	I				
D ₂	I/O					R ₀₂	I				
D ₃	I/O					R ₀₃	I				
D ₄	I/O					R ₁₀	I/O				
D ₅	I/O					R ₁₁	I/O				
D ₆	I/O					R ₁₂	I/O				
D ₇	I/O					R ₁₃	I/O				
D ₈	I/O					R ₂₀	I/O				
D ₉	I/O					R ₂₁	I/O				
D ₁₀	I/O					R ₂₂	I/O				
D ₁₁	I/O					R ₂₃	I/O				
D ₁₂	I/O					R ₃₀	O				
D ₁₃	I/O					R ₃₁	O				
D ₁₄	I/O					R ₃₂	O				
D ₁₅	I/O					R ₃₃	O				
INT ₀	I										
INT ₁	I										

* Specify the I/O composition with a mark of "O" in the applicable composition column.

A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) Other Options

I/O State at Halt Mode	<input type="checkbox"/> Enable	<input type="checkbox"/> Disable
External Crystal for Timer <input type="checkbox"/> NDK : MX-38T <input type="checkbox"/> Kyocera : KF-38G	<input type="checkbox"/> Yes [D ₁₄ and D ₁₅ become XO and XI. Do not enter anything in I/O option column of D ₁₄ and D ₁₅ .]	<input type="checkbox"/> No
Internal Halt	<input type="checkbox"/> Yes [When selecting Crystal for Timer and Oscillator except ceramic filter.]	<input type="checkbox"/> No

☆ Mark "V" in "□" for the selected spec.

Check List of Application

[A] Oscillation (for System Clock)

CPG	5V Operation	3V Operation
Resistor	<input type="checkbox"/> R _f = 110kΩ ± 2%	<input type="checkbox"/> R _f = 200kΩ ± 2%
Ceramic Filter	<input type="checkbox"/> MURATA : CSB400P	
External Clock	<input type="checkbox"/> f _{cp} = 40k to 400kHz	<input type="checkbox"/> f _{cp} = 40k to 220 kHz

☆Mark "V" in "□" for the selected oscillation.

[B] Halt Function (Only when Ceramic Filter is selected in [A].)

	Using Ceramic Filter
External Halt Mode	<input type="checkbox"/> Not used <input type="checkbox"/> Used (Recovery with Reset)

☆ Mark "V" in "□" for the selected spec.



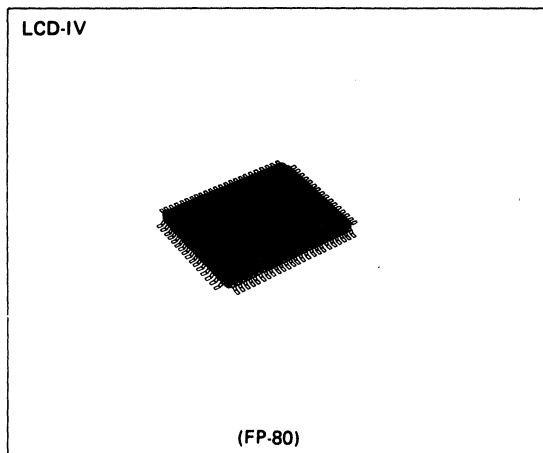
LCD— IV (HD613901)

Description

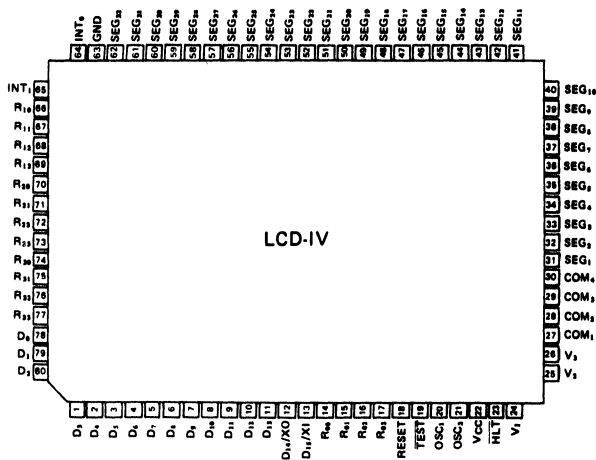
The LCD-IV is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O, Timer/Event Counter and Control Circuit, Direct Drive Circuit for LCD on single chip. The LCD-IV is designed to drive LCD directly and perform efficient controller function as well as arithmetic function for both binary and BCD data. With the on-chip crystal oscillator for timer, the clock function is easily realized. The CMOS technology of the LCD-IV provides the flexibility of microcomputers for battery powered and battery back-up applications in combination with low power consuming LCD.

FEATURES

- 4-bit Architecture
- 4,096 Words of Program ROM (10 bits/Word)
- 256 Digits of Data RAM and Display Data RAM (4 bits/Digit)
- Control Circuit and Direct Drive Circuit for LCD
 - 4 Commons (Duty Ratio; Static, 1/2, 1/3, 1/4)
 - 32 Segments (Externally expandable up to 96 Segments using external Drivers HD44100Hs)
- 32 I/O Lines and 2 External Interrupt Lines
- Timer/Event Counter
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
 - Table Look Up Capability —
- Powerful Interrupt Function
 - 3 Interrupt Sources
 - 2 External Interrupt Lines
 - Timer/Event Counter
 - Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; Pull Up MOS or CMOS or Open Drain
- Built-in Oscillator for System Clock (Resistor or Ceramic Filter)
- Built-in Crystal Oscillator for Timer
- Low Operating Power Dissipation
- Stand-by Mode (Halt Mode)
- 2 Versions;
 - $V_{CC} = 5V \pm 10\%$, 5 μ s Instruction Cycle Time
 - $V_{CC} = 2.5V$ to 5.5V, 20 μ s Instruction Cycle Time



PIN ARRANGEMENT

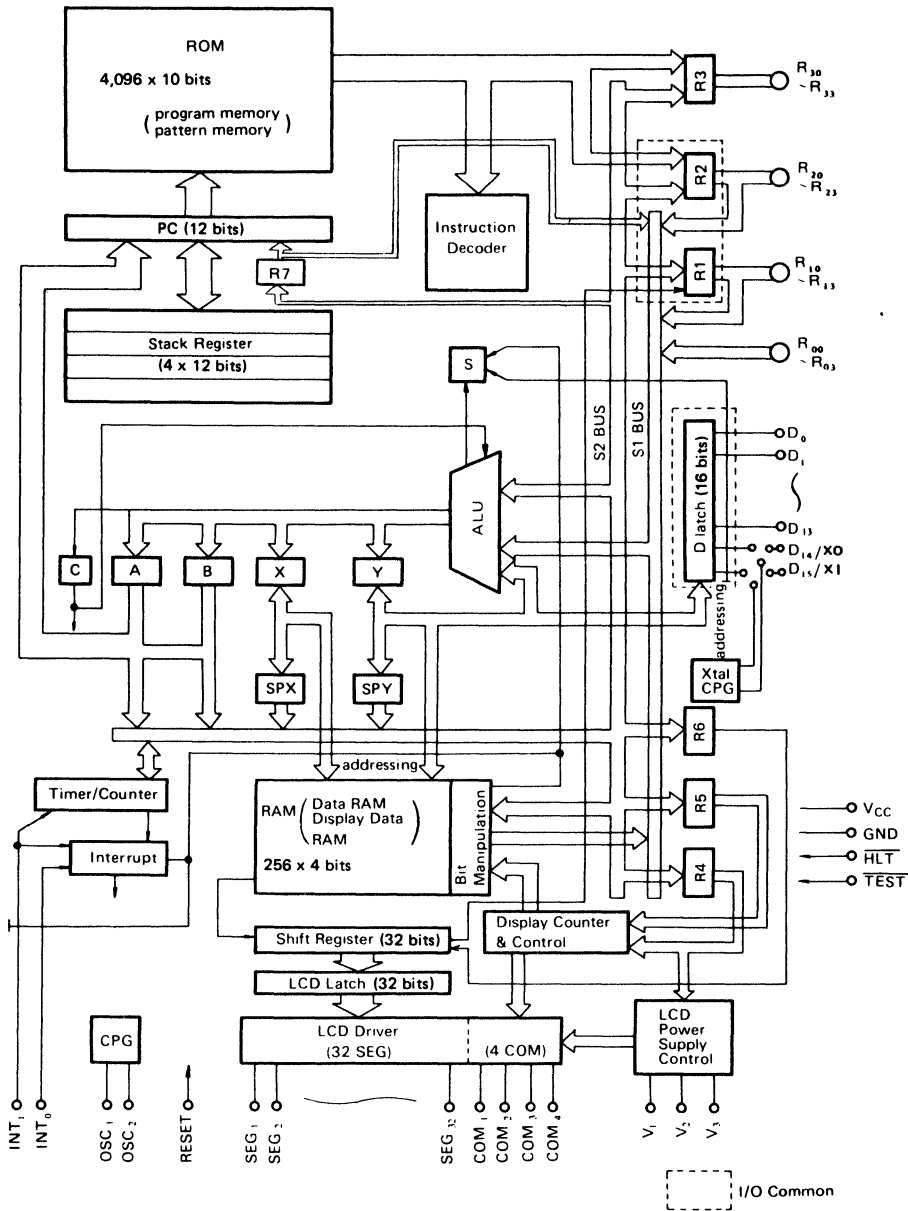


(Top View)

PROGRAM DEVELOPMENT SUPPORT TOOLS

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC

■ BLOCK DIAGRAM



LCD—IV (HD613901)

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

- (NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2". If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
2. All voltages are with respect to GND.
3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
4. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.

● ELECTRICAL CHARACTERISTICS - 1 ($V_{CC} = 5V \pm 10\%$, $T_a = -20$ to $+75^\circ C$)

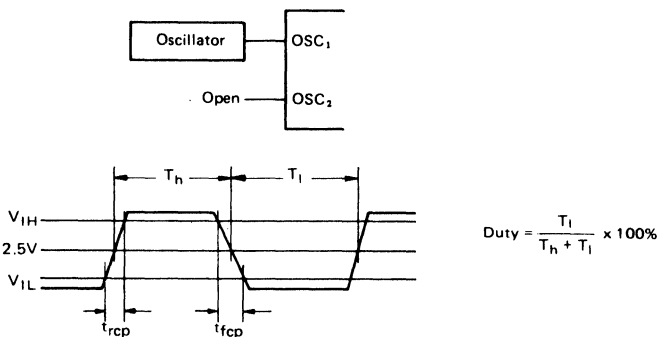
Item	Symbol	Test Conditions	Value			Unit	Note
			min	typ	max		
Input "Low" Voltage	V_{IL}		-0.3	-	1.0	V	
Input "High" Voltage	V_{IH}		$V_{CC}-1.0$	-	$V_{CC}+0.3$	V	(12)
Output "Low" Voltage	V_{OL}	$I_{OL} = 1.6$ mA	-	-	0.8	V	
Output "High" Voltage (1)	V_{OH1}	$-I_{OH} = 1.0$ mA	2.4	-	-	V	(1)
Output "High" Voltage (2)	V_{OH2}	$-I_{OH} = 0.01$ mA	$V_{CC}-0.3$	-	-	V	(2)
Driver Voltage Descending (COM)	V_{d1}	$I_d = 0.05$ mA, $V_{LCD} = 5V$	-	-	0.4	V	(16)
Driver Voltage Descending (SEG)	V_{d2}	$I_d = 0.01$ mA, $V_{LCD} = 5V$	-	-	0.4	V	(16)
Dividing Resistor of LCD Power Supply	R_{well}		25	-	300	k Ω	
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	-	-	μs	(14)
Output "High" Current	I_{OH}	$V_{OH} = V_{CC}$	-	-	4	μA	(3)
Input Leakage Current	I_{IL}	$V_{in} = 0$ to V_{CC}	-	-	2	μA	(4), (12)
Pull up MOS Current	$-I_p$	$V_{CC} = 5V$	45	-	250	μA	
Supply Current (1)	I_{CC1}	$V_{in} = V_{CC}$, $V_{CC} = 5V$ Ceramic Filter Oscillation ($f_{osc} = 800$ kHz)	-	-	3	mA	(5)
		$V_{in} = V_{CC}$, $V_{CC} = 5V$ Ceramic Filter Oscillation ($f_{osc} = 400$ kHz)	-	-	1.5	mA	(5)
Supply Current (2)	I_{CC2}	$V_{in} = V_{CC}$, $V_{CC} = 5V$ R_f Oscillation ($f_{osc} = 800$ kHz) External Clock Operation ($f_{cp} = 800$ kHz)	-	-	2	mA	(5)
		$V_{in} = V_{CC}$, $V_{CC} = 5V$ R_f Oscillation ($f_{osc} = 400$ kHz) External Clock Oscillation ($f_{cp} = 400$ kHz)	-	-	1	mA	(5)
Standby I/O Leakage Current	I_{LS}	$HLT = 1.0V$, $V_{in} = 0$ to V_{CC}	-	-	1.0	μA	(6), (12)
Standby Supply Current (1)	I_{CCS1}	$V_{in} = V_{CC}$, $HLT = 0.2V$	-	-	10	μA	(15)
Standby Supply Current (2)	I_{CCS2}	$V_{in} = V_{CC}$, $HLT = 0.2V$	-	50*	120	μA	(7)
LCD Display Voltage	V_{LCD}	$V_{CC}-V_3$	2.5	-	V_{CC}	V	(11)
Frame Frequency of LCD Drive	f_F	$n = 1$ (static) $n = 2$ (1/2 Duty) $n = 3$ (1/3 Duty) $n = 4$ (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$			Hz	(13)
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		130	-	1,000	kHz	(8), (13)
External Clock Duty	Duty		45	-	55	%	(8)
External Clock Rise Time	t_{rcp}		0	-	0.2	μs	(8)
External Clock Fall Time	t_{fcp}		0	-	0.2	μs	(8)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	4.0	-	30.7	μs	(8)
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	$R_f = 62k\Omega \pm 2\%$	600	-	1,000	kHz	(9)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.0	-	6.7	μs	(9)
Internal Clock Operation (Ceramic Filter Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	Ceramic Filter	784	-	816	kHz	(10)
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	4.9	-	5.1	μs	(10)

(NOTE) All voltages are with respect to GND.

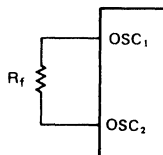
* A typical value of I_{CCS2} is a reference value when T_a is at $25^\circ C$.



8. Applied to external clock operation (system clock).



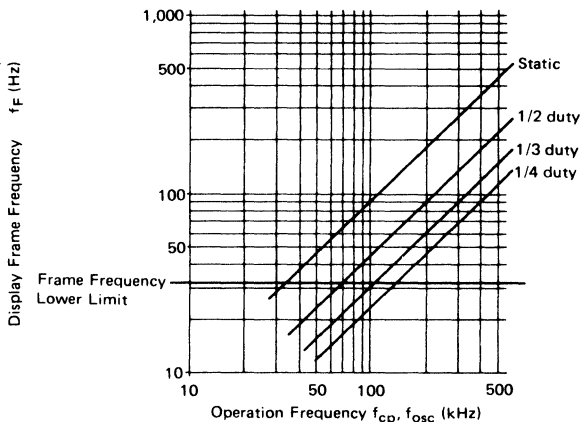
9. Applied to internal clock operation using resistor R_f. (system clock)



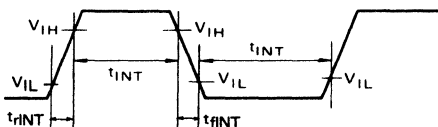
Wiring of OSC₁ and OSC₂ pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.

10. Applied to internal clock operation using ceramic filter. (system clock)
11. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
12. Applied to input pins, I/O common pins among D and R pins, and RESET, HLT, OSC₁, INT₀, INT₁ pins.
13. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.

The following shows the relation between liquid crystal display frame frequency and operation frequency.



14. INT₀ and INT₁ inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.

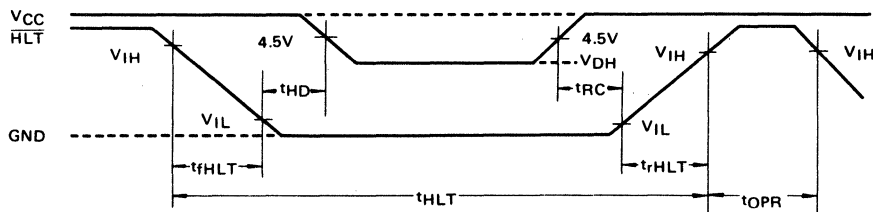


15. Power supply circuit for LCD is excluded. The standby supply current (1) is the supply at $V_{CC} = 5V \pm 10\%$ in "Halt" state in the case that the crystal oscillation for timer is not selected. The supply current when supply voltage falls to the Halt Duration Voltage is called "Halt Current" (I_{DH}). (shown in ELECTRICAL CHARACTERISTICS—2)

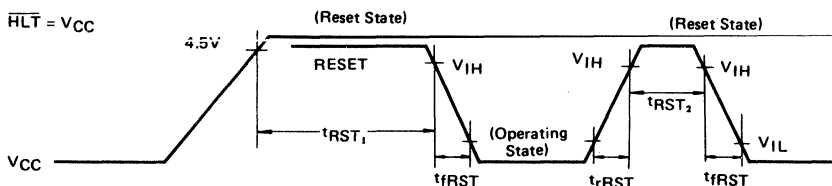


LCD—IV (HD613901)

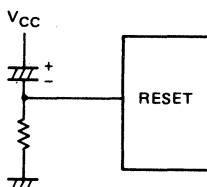
16. The voltage that drops between the power supply pins (V_{CC} , V_1 , V_2 , V_3) and each common or segment output pin.
 17. External Halt Timing Chart



18. RESET Input Condition



- t_{RST1} includes the time that required from the power ON until the operation gets into the constant state.
 - t_{RST2} is applied when the operation is in the constant state.
- Reset circuit at power on is not installed. Simple reset circuit at power on is the following.



19. The supply current at $V_{CC} = V_{DH} = 2.3V$ in "Halt" state, in the case that the crystal oscillation for timer is not selected. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded.

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.5$ to $5.5V$)

● ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 to +7.0	V	
Pin Voltage	V_{T1}	-0.3 to $V_{CC} + 0.3$	V	
Maximum Total Output Current (1)	$-\Sigma I_{O1}$	25	mA	(Note 3)
Maximum Total Output Current (2)	ΣI_{O2}	25	mA	(Note 3)
Operating Temperature	T_{opr}	-20 to +75	°C	
Storage Temperature	T_{stg}	-55 to +125	°C	

- (NOTE) 1. Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under the conditions of "ELECTRICAL CHARACTERISTICS-1, -2." If these conditions are exceeded, it could be cause of malfunction of LSI and affects reliability of LSI.
 2. All voltages are with respect to GND.
 3. Maximum Total Output Current is the total sum of output currents which can flow out or in simultaneously.
 4. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.



● ELECTRICAL CHARACTERISTICS – 1 ($V_{CC} = 2.5$ to $5.5V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test Conditions	Value		Unit	Note	
			min	max			
Input "Low" Voltage	V_{IL}		-0.3	$0.15 \cdot V_{CC}$	V		
Input "High" Voltage	V_{IH}		$0.85 \cdot V_{CC}$	$V_{CC} + 0.3$	V	(11)	
Output "Low" Voltage	V_{OL}	$I_{OL} = 0.4$ mA	-	0.4	V		
Output "High" Voltage (1)	V_{OH1}	$-I_{OH} = 0.08$ mA	$V_{CC} - 0.5$	-	V	(1)	
Output "High" Voltage (2)	V_{OH2}	$-I_{OH} = 0.01$ mA	$V_{CC} - 0.4$	-	V	(2)	
Driver Voltage Descending (COM)	V_{d1}	$I_d = 0.05$ mA	-	0.5	V	(15)	
Driver Voltage Descending (SEG)	V_{d2}	$I_d = 0.01$ mA	-	0.5	V	(15)	
Dividing Resistor of LCD Power Supply	R_{well}		25	300	k Ω		
Interrupt Input Hold Time	t_{INT}		$2 \cdot T_{inst}$	-	μs	(13)	
Output "High" Current	I_{OH}	$V_{OH} = V_{CC}$	-	4	μA	(3)	
Input Leakage Current	I_{IL}	$V_{in} = 0$ to V_{CC}	-	2	μA	(4), (11)	
Pull up MOS Current	$-I_P$	$V_{CC} = 3V$	10	100	μA		
Supply Current	I_{CC}	$V_{in} = V_{CC}$, $V_{CC} = 3V$ R_f Oscillation ($f_{osc} = 200$ kHz) External Clock Operation ($f_{cp} = 200$ kHz)	-	0.3	mA	(5)	
Standby I/O Leakage Current	I_{LS}	$HLT = 0.5V$, $V_{in} = 0$ to V_{CC}	-	1	μA	(6), (11)	
Standby Supply Current (1)	I_{CCS1}	$V_{in} = V_{CC}$, $HLT = 0.1V$, $V_{CC} = 2.5$ to $3.5V$	-	6	μA	(14)	
Standby Supply Current (2)	I_{CCS2}	$V_{in} = V_{CC}$, $HLT = 0.1V$, $V_{CC} = 3.0V$	-	21	μA	(7)	
LCD Display Voltage	V_{LCD}	$V_{CC} - V_3$	2.5	V_{CC}	V	(10)	
Frame Frequency of LCD Drive	f_F	$n = 1$ (static) $n = 2$ (1/2 Duty) $n = 3$ (1/3 Duty) $n = 4$ (1/4 Duty)	$\frac{1}{256 \times n \times T_{inst}}$		Hz	(12)	
External Clock Operation; System Clock							
External Clock Frequency	f_{cp}		130	300	kHz	(8), (12)	
External Clock Duty	Duty		45	55	%	(8)	
External Clock Rise Time	t_{rcp}		0	0.2	μs	(8)	
External Clock Fall Time	t_{fcp}		0	0.2	μs	(8)	
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{cp}$	13.3	30.7	μs	(8)	
Internal Clock Operation (R_f Oscillation); System Clock							
Clock Oscillation Frequency	f_{osc}	$R_f = 270k\Omega \pm 2\%$	$V_{CC} = 2.5$ to $3.5V$	130	270	kHz	(9)
			$V_{CC} = 2.5$ to $5.5V$	130	300		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	$V_{CC} = 2.5$ to $3.5V$	14.8	30.7	μs	(9)
			$V_{CC} = 2.5$ to $5.5V$	13.3	30.7		
Clock Oscillation Frequency	f_{osc}	$R_f = 62k\Omega \pm 2\%$	$V_{CC} = 4.5$ to $5.5V$	600	1000	kHz	(9)
			$V_{CC} = 2.5$ to $5.5V$	420	1000		
Instruction Cycle Time	T_{inst}	$T_{inst} = 4/f_{osc}$	$V_{CC} = 4.5$ to $5.5V$	4.0	6.7	μs	(9)
			$V_{CC} = 2.5$ to $5.5V$	4.0	9.5		

(NOTE) All voltages are with respect to GND.



LCD—IV (HD613901)

● ELECTRICAL CHARACTERISTICS-2 (T_a = -20 to +75°C)

Item	Symbol	Test Conditions	Value		Unit	Note
			min	max		
Halt Duration Voltage	V _{DH}	HLT = 0.2V	2.3	—	V	(16)
Halt Current	I _{DH}	V _{in} = V _{CC} , HLT = 0.2V, V _{DH} = 2.3V	—	4.0	μA	(16), (18)
Halt Delay Time	t _{HD}		100	—	μs	(16)
Operation Recovery Time	t _{RC}		100	—	μs	(16)
HLT Fall Time	t _{fHLT}		—	1000	μs	(16)
HLT Rise Time	t _{rHLT}		—	1000	μs	(16)
HLT "Low" Hold Time	t _{HLT}		400	—	μs	(16)
HLT "High" Hold Time	t _{OPR}		100	—	μs	(16)
RESET Pulse Width (1)	t _{RST1}	External Reset, HLT = V _{CC}	1	—	ms	(17)
RESET Pulse Width (2)	t _{RST2}	External Reset, HLT = V _{CC} , V _{CC} = 2.5V to 5.5V	2·T _{inst}	—	μs	(17)
RESET Rise Time	t _{rRST}	External Reset, HLT = V _{CC} , V _{CC} = 2.5 to 5.5V	—	100	μs	(17)
RESET Fall Time	t _{fRST}	External Reset, HLT = V _{CC} , V _{CC} = 2.5 to 5.5V	—	100	μs	(17)
INT ₀ , INT ₁ Rise Time	t _{rINT}		—	50	μs	(13)
INT ₀ , INT ₁ Fall Time	t _{fINT}		—	50	μs	(13)

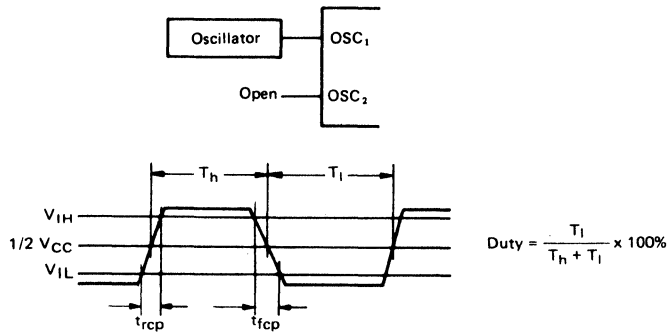
- (NOTE) 1. Applied to PMOS load of CMOS output pins and CMOS I/O common pins among D and R pins.
 2. Applied to CMOS output pins, CMOS I/O common pins, input pins with pull up MOS, and I/O common pins with pull up MOS among D and R pins.
 3. Applied to open-drain output pins and open-drain I/O common pins among D and R pins.
 4. Pull up MOS current is excluded.
 5. Applied to the supply current when the LCD-IV is in the reset state and the crystal oscillation for timer doesn't operate. (Current that flows in input/output circuit and in the power supply circuit for LCD is excluded).
 Test Conditions: RESET, HLT = V_{CC} (Reset State), TEST = V_{CC}
 $D_{14}/XO, D_{15}/XI \begin{cases} D_{14}/XO, D_{15}/XI = V_{CC} & \text{(Crystal oscillation for timer is not selected.)} \\ D_{14}/XO = \text{Open}, D_{15}/XI = V_{CC} & \text{(Crystal oscillation for timer is selected.)} \end{cases}$
 $V_1, V_2, V_3 = V_{CC}$
 COM₁ to COM₄, SEG₁ to SEG₃₂ = Open

When the crystal oscillation for timer operates, the standby supply current (2) I_{CCS2} flows in addition to I_{CC}. When the LCD-IV is installed in the user's system, and in operation current increases according to the external circuitry and devices. Those are connected to the LCD-IV. User should design the power supply in consideration of this point. (The difference between the measured current in the above reset state and that measured in the operational state in the user's system is the increased part of the supply current).

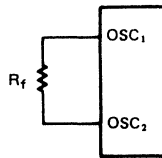
6. Standby I/O leakage current is the leakage current of I/O pins in the "Halt" and "Disable" state.
 7. Current that flows in the input/output circuit and in the power supply circuit for LCD is excluded. The standby supply current (2) is the supply current at V_{CC} = 3.0V in "Halt" state in the case that the crystal oscillation for timer is selected (only the crystal oscillator for timer, 5-bit divider and 6-bit prescaler are in operation).



8. Applied to external clock operation. (system clock)



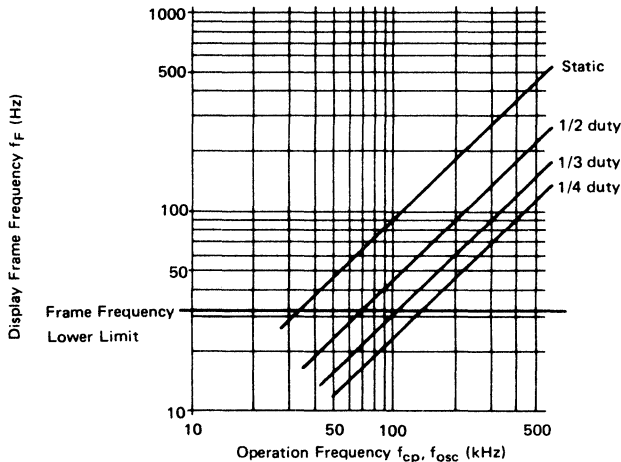
9. Applied to internal clock operation using resistor R_f. (System Clock)



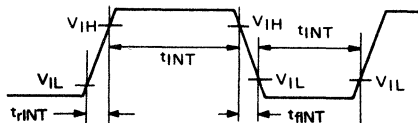
Wiring OSC₁ and OSC₂ pins should be as short as possible because the oscillation frequency is modified by capacitance of these pins.

- 10. Power supply condition $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$ should be maintained.
- 11. Applied to input pins, I/O common pins among D and R pins, and RESET, HLT, OSC₁, INT₀, INT₁ pins.
- 12. Lower limit of operation frequency is determined by liquid crystal display duty. Flutter occurs on liquid crystal display if frame frequency is under 32 Hz. Therefore operation frequency should be determined to prevent that frame frequency becomes under 32 Hz.

The following shows the relation between liquid crystal display frame frequency and operation frequency.



- 13. INT₀ and INT₁ inputs must be retained for two or more instruction cycle time at both "High" and "Low" levels.



● **V₁, V₂ and V₃**

Power for liquid crystal display are supplied to the LCD-IV using these pins ($V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$).

● **R₀₀ to R₀₃**

These 4 lines are a 4-bit input channel. Refer to INPUT/OUTPUT for additional information.

● **R₁₀ to R₁₃, R₂₀ to R₂₃**

These 8 lines are arranged into two 4-bit Input/Output common channels. The 4-bit register is attached to these channels. These channels are directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option. Refer to INPUT/OUTPUT for additional information.

● **R₃₀ to R₃₃**

These 4 lines are a 4-bit output channel. 4-bit register is attached to this channel. This channel is directly addressed by the operand of an instruction. I/O configuration of each pin can be specified among Open Drain and CMOS using a mask option. Refer to INPUT/OUTPUT for additional information.

● **D₀ to D₁₃**

These are 14 discrete signals which can be configured as Input/Output lines. Refer to INPUT/OUTPUT for additional information.

● **D₁₄/XO, D₁₅/XI**

D₁₄/XO and D₁₅/XI are selected in the following 3 types with a mask option.

- Discrete I/O (common pin)
- Crystal circuit connecting pins (with internal halt)
- Crystal circuit connecting pins (no internal halt)

Refer to INPUT/OUTPUT for additional information.

● **COM₁ to COM₄**

These pins are common pins for liquid crystal display. Refer to LIQUID CRYSTAL DISPLAY for additional information.

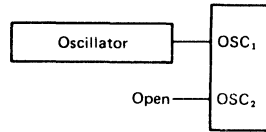
● **SEG₁ to SEG₃₂**

These are segment pins for liquid crystal display.

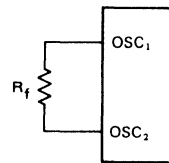
■ **OSCILLATOR**

The user can specify a resistor, or a ceramic filter circuit or an external oscillator by "MASK OPTION LIST".

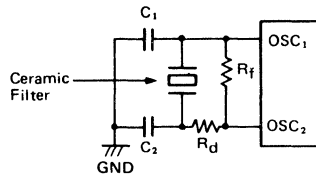
(1) External Clock



(2) Resistor



(3) Ceramic Filter (This is not applied to Low Voltage Operation Version.)



(NOTE) Configuration and constant of external parts are depend upon each applied ceramic filter.

Reset at the time of halt releasing.

This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

■ **ROM**

● **ROM Address Space**

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the LCD-IV consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

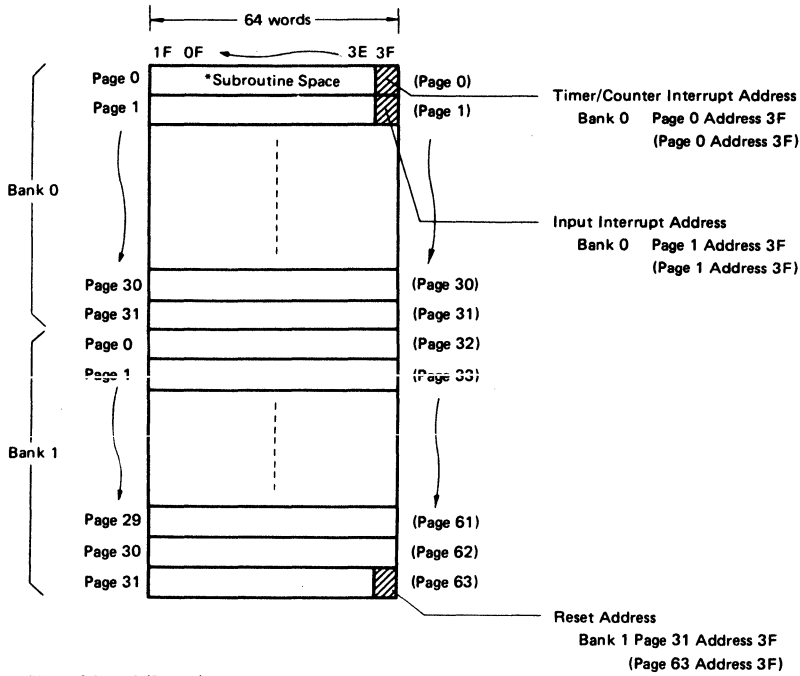
The ROM address is split into two banks.

Each bank is composed of 32 pages (64 words/page).

The ROM capacity is 4,096 words (1 word = 10 bits) in all.

All addresses can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 1.



*Bank 0 Page 0 (Page 0) is the Subroutine Space.

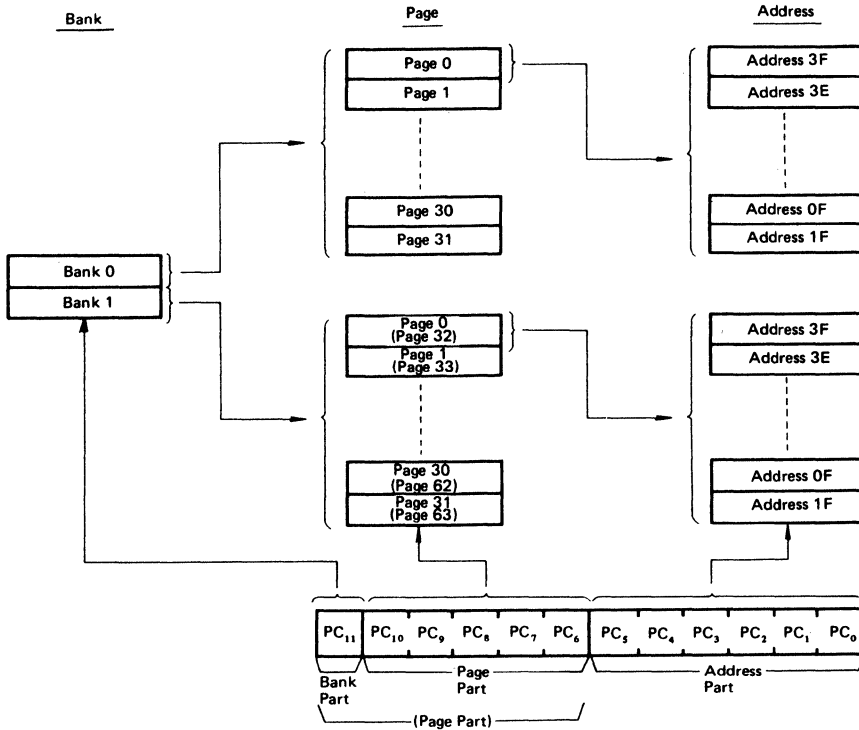
Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 1 ROM Address Space

● Program Counter (PC)

The program counter is used for addressing of ROM. The

program counter consists of the bank part, the page part, and the address part as shown in Figure 2.



Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 2 Configuration of Program Counter

The bank part is a 1-bit register and the page part is a 5-bit register.

Once a certain value is loaded into the bank part or the page part, it is unchanged until other value is loaded by a program. "0" (the Bank 0) or "1" (the Bank 1) can be set in the bank part, and any number among 0 to 31 in the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexadecimal system is shown in Table 1. This sequence forms a loop and has neither the starting nor ending point. It doesn't generate an overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part or the page part is changed.

Table 1 Program Counter Address Part Sequence

Decimal	Hexa-decimal	Decimal	Hexa-decimal	Decimal	Hexa-decimal
63	3F	5	05	9	09
62	3E	11	0B	19	13
61	3D	23	17	38	26
59	3B	46	2E	12	0C
55	37	28	1C	25	19
47	2F	56	38	50	32
30	1E	49	31	37	25
60	3C	35	23	10	0A
57	39	6	06	21	15
51	33	13	0D	42	2A
39	27	27	1B	20	14
14	0E	54	36	40	28
29	1D	45	2D	16	10
58	3A	26	1A	32	20
53	35	52	34	0	00
43	2B	41	29	1	01
22	16	18	12	3	03
44	2C	36	24	7	07
24	18	8	08	15	0F
48	30	17	11	31	1F
33	21	34	22		
2	02	4	04		



● **Designation of ROM Address and ROM Code**

The bank part of the ROM address is shown in the binary system and the page part in the decimal system. The address part is divided into 2 bits and 4 bits, and shown in the hexadecimal system.

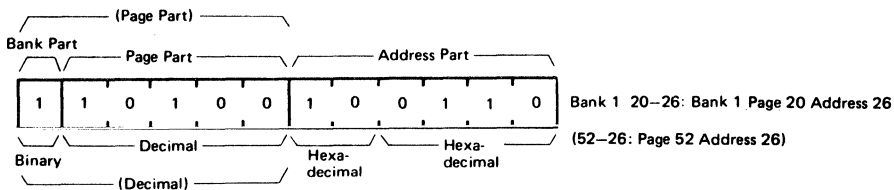
It is possible to combine the bank part and the page part and show the combined part as the Page (in the decimal system).

In this case, the Page 0 to the Page 31 in the Bank 1 are shown as the Page 32 to the Page 63. The examples are shown in Figure 3.

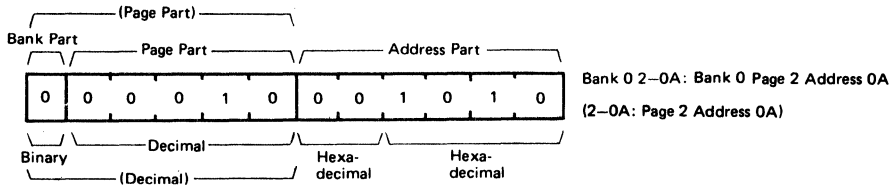
One word (10 bits) of ROM is divided into three parts (2 bits, 4 bits and 4 bits from the most significant bit O_{10} in order) shown in the hexadecimal system. The examples are shown in Figure 3.

(a) ROM Address

(Example 1)

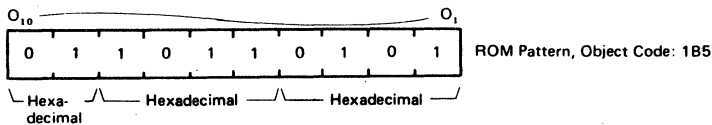


(Example 2)



(b) ROM Code

(Example 1)



(Example 2)

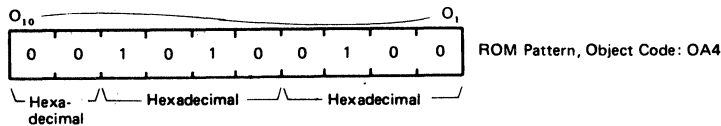


Figure 3 Designation of ROM Address and ROM Code

■ **PATTERN GENERATION**

The pattern (constant) can be accessed by the pattern instruction (P). The pattern can be written in any address of the ROM address space.

● **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 4 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part and the bank part are ORed with the upper 2 bits of B register, the Carry F/F and the operand p.

The bank part of the ROM address is determined by the logical equation: $PC_{11} + p_2$ (p_2 = the MSB of the operand p).

If the address where the pattern instruction exists is in the Bank 1, only the pattern of the Bank 1 can be referenced.

If the address where the pattern instruction exists is in the Bank 0, the pattern of the either Bank 1 or Bank 0 can be referenced depending on the value of p_2 . The truth table of the bank part of the ROM address is shown in Table 2.

The value of the program counter is apparently modified and not changed actually. After execution of the pattern instruction, the program counter counts up and the next instruction is executed.

The pattern instruction is executed in 2 cycles.

● **Generation**

The pattern of referred ROM address is generated as the following two ways:

- (i) The pattern is loaded into the accumulator and B register.
- (ii) The pattern is loaded into the Data I/O Registers R2 and R3.

The command bits (O_9, O_{10}) in the pattern determine which way is taken.

Mode (i) is performed when O_9 is "1" and mode (ii) is performed when O_{10} is "1".

Mode (i) and (ii) are simultaneously performed when both O_9 and O_{10} are "1". The correspondence of each bit of the pattern is shown in Figure 5.

Examples of how to use the pattern instruction is shown in Table 3.

CAUTION

In the program execution, the pattern can not be distinguished from the instruction. When the program is running at the address written as a pattern, the instruction corresponding to the pattern bit is executed. Take care not to execute a pattern as an instruction.

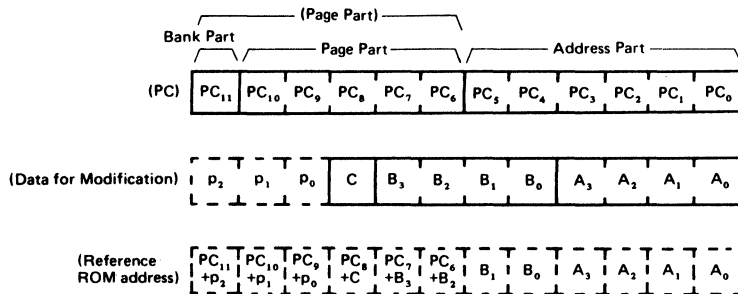


Figure 4 ROM Addressing for Pattern Generation

Table 2 Bank Part Truth Table of Pattern Generation

PC_{11}	p_2	Bank part of ROM address to be referenced to
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

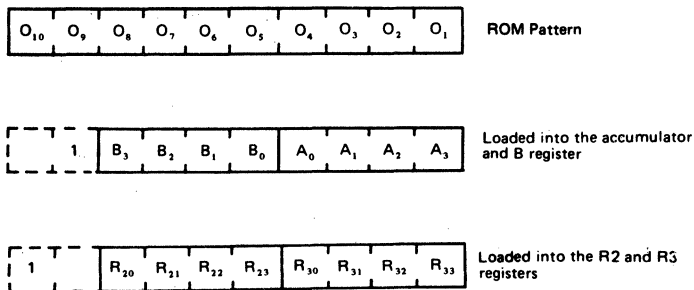


Figure 5 Correspondence of Each Bit of Pattern

Table 3 Example of how to use Pattern Instructions

Before Execution					Referred ROM Address	ROM Pattern	After Execution			
PC	p	C	B	A			B	A	R2	R3
Bank 0 0-3F (0-3F)	1	0	A	0	Bank 0 10-20 (10-20)	12D	2	B	—	—*
Bank 0 0-3F (0-3F)	7	1	4	0	Bank 1 29-00 (61-00)	22D	—	—	4	B
Bank 1 30-00 (62-00)	4	0/1**	0	9	Bank 1 30-09 (62-09)	32D	2	B	4	B
Bank 1 30-00 (62-00)	1	0/1**	F	9	Bank 1 31-39 (63-39)	223	—	—	4	C

* “—” means that the value does not change after execution of the instruction.
 ** “0/1” means that either “0” or “1” may be selected.

■ **BRANCH**

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways. They are explained in the following paragraphs.

● **BR**

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, O₆ to O₁) are transferred to the address part of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is “1”. If it is “0”, the instruction is skipped and the Status F/F becomes “1”. The operation is shown in Figure 6.

● **LPU**

By LPU instruction, a jump between the bank and page is performed.

The lower 5 bits of the ROM Object Code (operand u, O₅ to O₁) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. At the same time, the signal $\overline{R_{70}}$ (the reversed-phase signal of the Data I/O Register R₇₀) is transferred to the bank part of the program counter with a delay of 1 instruction cycle time. The operation is shown in Figure 7.

Consequently, the bank and page will remain unchanged in the cycle immediately following this instruction. In the next cycle, a jump between the bank and page is achieved.

This instruction (LPU) is conditional, and is executed only when the Status F/F is “1”. Even after a skip, the Status F/F

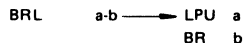
will remain unchanged (“0”).

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

● **BRL**

By BRL instruction, the program branches to an address in any bank and page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.



< Jump to Bank “ $\overline{R_{70}}$ ” Page a — Address b >

BRL instruction is a conditional instruction because of its characteristics of LPU and BR instructions, and is executed only when the Status F/F is “1”. If the Status F/F is “0”, the instruction is skipped and the Status F/F becomes “1”. The examples of BRL instruction are shown in Figure 8.

● **TBR (Table Branch)**

By TBR instruction, the program branches referring to the table.

The program counter is modified with the accumulator, the B register, the Carry F/F and the operand p.

The method for modification is shown in Figure 9.

The bank part is determined by the logical equation: PC₁₁ + P₂, as shown in Table 4.

If the address where TBR instruction exists is in the Bank 1,



it is possible to jump to an address only in the Bank 1, not to an address in the Bank 0.

If the address where TBR instruction exists is in the Bank 0, it is possible to jump to an address in either the Bank 1 or the

Bank 0 depending on the value of the operand p_2 .

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.

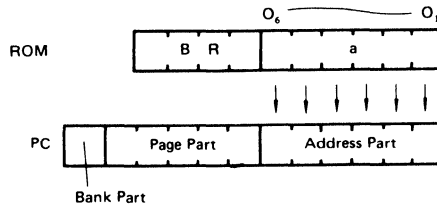


Figure 6 BR Operation

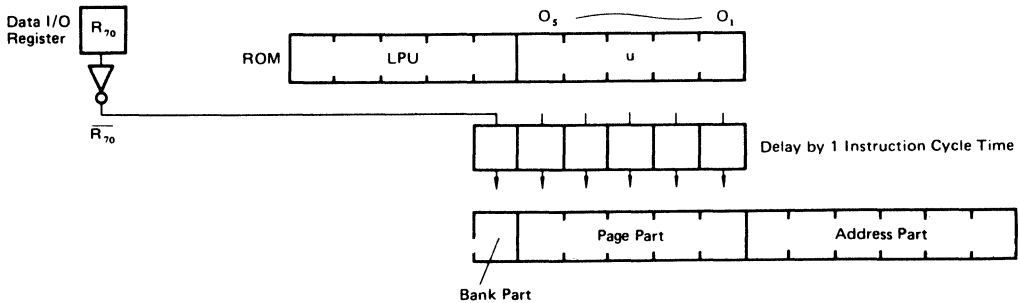


Figure 7 LPU Operation

Branch to Bank 0		
• LAI	15	} $R_{70} = "1"$ ($\overline{R_{70}} = "0"$)
• LRA	7	
• LPU	5	
BR	3F	
		(Branch to Bank 0 5-3F (5-3F))
Branch to Bank 1		
• LAI	15	} $R_{70} = "1"$ ($\overline{R_{70}} = "0"$)
• LBA	7	
• COMB	31	
• LPU	3F	
		(Branch to Bank 0 31-3F (31-3F))
Branch to Bank 1		
• LAI	0	} $R_{70} = "0"$ ($\overline{R_{70}} = "1"$)
• LRA	7	
• LPU	15	
BR	3F	
		(Branch to Bank 1 15-3F (47-3F))
• LAI	0	} $R_{70} = "0"$ ($\overline{R_{70}} = "1"$)
• LTA	7	
• LYI	2	
• XMA	10	
• LPU	2E	
BR	2E	(Branch to Bank 1 10-2E (42-2E))

Figure 8 BRL Example

Table 4 Bank Part Truth Table of TBR Instruction

PC ₁₁	P ₂	Bank Part of PC after TBR
1 (Bank 1)	1	1 (Bank 1)
	0	1 (Bank 1)
0 (Bank 0)	1	1 (Bank 1)
	0	0 (Bank 0)

■ SUBROUTINE JUMP

There are two types of subroutine jumps. They are explained in the following paragraphs.

● CAL

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The Subroutine Space is the Bank 0 Page 0 (Page 0).

The address next to CAL instruction address is pushed onto the Stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 10.

The bank part of the program counter becomes the Bank 0 and the page part becomes the Page 0. The lower 6 bits (operand a, O₆ to O₁) of the ROM Object Code are transferred to the address part of the program counter.

The LCD-IV has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine



LCD—IV (HD613901)

jumps (including interrupts).

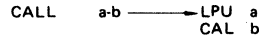
CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

● **CALL**

By CALL instruction, subroutine jump to an address in any bank and page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction in the bank designated by the reversed-phase signal $\overline{R_{70}}$.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two steps as follows.



< Subroutine Jump to Bank " $\overline{R_{70}}$ ", Page a — Address b >

CALL instruction is conditional because of characteristics of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F changes to "1". The examples of CALL instruction are shown in Figure 11.

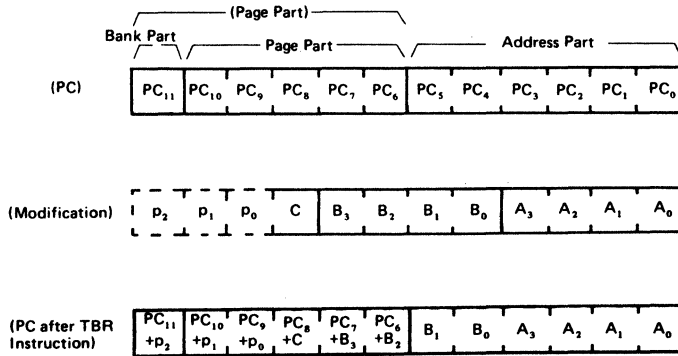


Figure 9 Modification of Program Counter by TBR Instruction

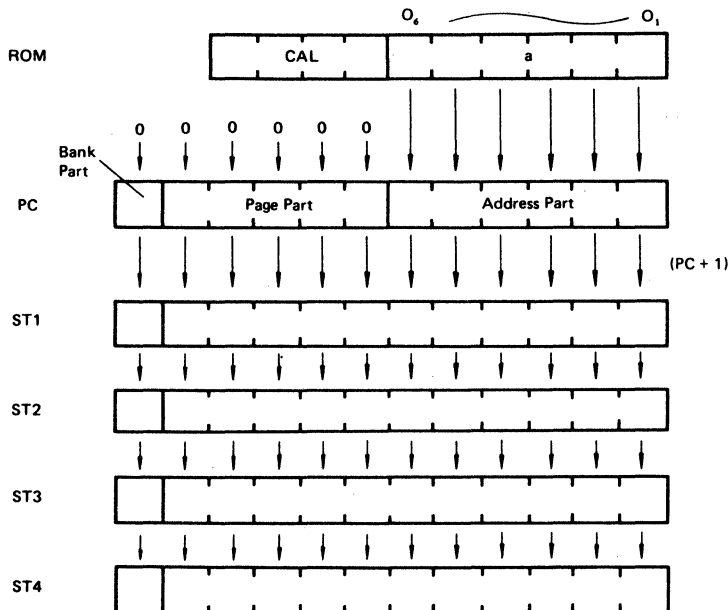


Figure 10 Subroutine Jump Stacking Order



```

Subroutine Jump to Bank 0
LAI 15
LRA 7      R70 = "1" (R̄70 = "0")
LPU 5      CALL 5-3F
CAL 3F     (Subroutine Jump to Bank 0 5-3F (5-3F))

LAI 15
LBA 7
LRA 7      R70 = "1" (R̄70 = "0")
COMB
LPU 31     CALL 31-3F
CAL 3F     (Subroutine Jump to Bank 0 31-3F (31-3F))

Subroutine Jump to Bank 1
LAI 0
LRA 7      R70 = "0" (R̄70 = "1")
LPU 15     CALL 15-3F
CAL 3F     (Subroutine Jump to Bank 1 15-3F (47-3F))

LAI 0
LTA 7
LYI 3      R70 = "0" (R̄70 = "1")
XMA
LPU 10     CALL 10-2E
CAL 2E     (Subroutine Jump to Bank 1 10-2E (42-2E))
    
```

Figure 11 CALL Example

■ RAM

RAM is the memory used for data storage and register save (data RAM) and storage of segment data for liquid crystal display (display data RAM). Its capacity is 256 digits (1,024 bits) where one digit consists of 4 bits.

(Note 1) Capacity of display data RAM varies corresponding to the duty ratio of LCD.

(Note 2) On the LCD-IV, RAM contents is not broken at system reset.

Addressing of RAM is performed by a matrix of the file No. and the digit No. Normally the file No. is set in the X register and the digit No. is set in the Y register, then the matrix of X and Y addresses RAM and performs the Read/Write operation. Special digits in RAM can be addressed without using X and Y. These digits, 16 digits (MR0 to MR15), are called Memory Register (MR). Memory Register can be exchanged for A register by XAMR instruction. RAM address space is shown in Figure 12.

	X	Y	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	[Shaded Area]															
	1	1																
	2	2																
	3	3																
	4	4																
	5	5																
	6	6																
	7	7	[White Area]															
	8	8																
	9	9																
	10	10																
	11	11																
	12	12																
	13	13																
	14	14	[White Area]															
	15	15																
		MR15	MR14	MR13	MR12	MR11	MR10	MR9	MR8	MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0	
X register File No.																		

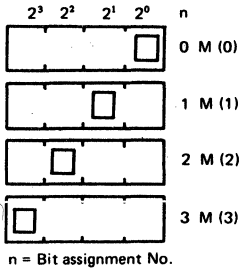
(NOTE) The area marked as [White Area] is usable only for data.
The area marked as [Shaded Area] is usable for both liquid crystal display and data.

Figure 12 RAM Address Space



If an instruction consists of a simultaneous Read/Write operations of RAM (exchange of RAM and a register), the writing data doesn't affect the reading data because the read operation precedes the write operation.

RAM bit manipulation is usable, which performs any bit set (SEM), reset (REM) or test (TM) of the addressed RAM. Bit assignment is made by the program as shown below.



The bit test makes the status "1" when the assigned bit is "1" and makes it "0" when the assigned bit is "0".

REGISTERS

The LCD-IV has six 4-bit registers and two 1-bit registers available to the programmer. 1-bit registers are Carry F/F and Status F/F. They are explained in the following paragraphs.

Accumulator (A; A Register) and Carry F/F (C)

The result of ALU operation (4 bits) and the overflow of the ALU are put into the accumulator and Carry F/F respectively. Carry F/F can be set, reset or tested. Combination of the accumulator and Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

B Register (B)

The result of ALU operation (4 bits) is put into this register. B register is used as a sub-accumulator to stack the data temporarily and also used as a counter.

X Register (X)

The result of ALU operation (4 bits) is put into this register. X register is exchangeable with SPX register and addresses the RAM file.

SPX Register (SPX)

SPX register is exchangeable with X register. SPX register is used to stack the contents of the X register and expand the addressing system of RAM in combination with X register.

Y Register (Y)

The result of ALU operation (4 bits) is put into this register. Y register is exchangeable with SPY register. Y register can calculate itself simultaneously with transferring the data by bus lines, which is usable for the calculation of two or more digits (4 bits/digit). Y register addresses the RAM digits and 1-bit discrete input/output common pins.

SPY Register (SPY)

SPY register is exchangeable with Y register. SPY register is used to stack the contents of the Y register and expand the addressing system of RAM and 1-bit discrete input/output common pins in combination with Y register.

Status F/F (S)

Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. Status F/F affects conditional instructions (LPU, BR and CAL). These instructions are executed only when Status F/F is "1". If it is "0", these instructions are skipped and Status F/F becomes "1".

INPUT/OUTPUT

Discrete I/O (D Pin)

The discrete I/O is composed of 1-bit latch and I/O pin. Figure 13 shows the basic block diagram.

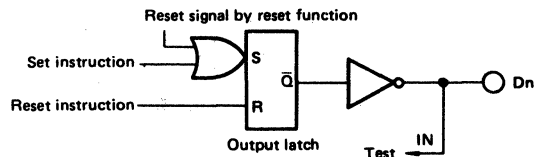


Figure 13 Discrete I/O Block Diagram

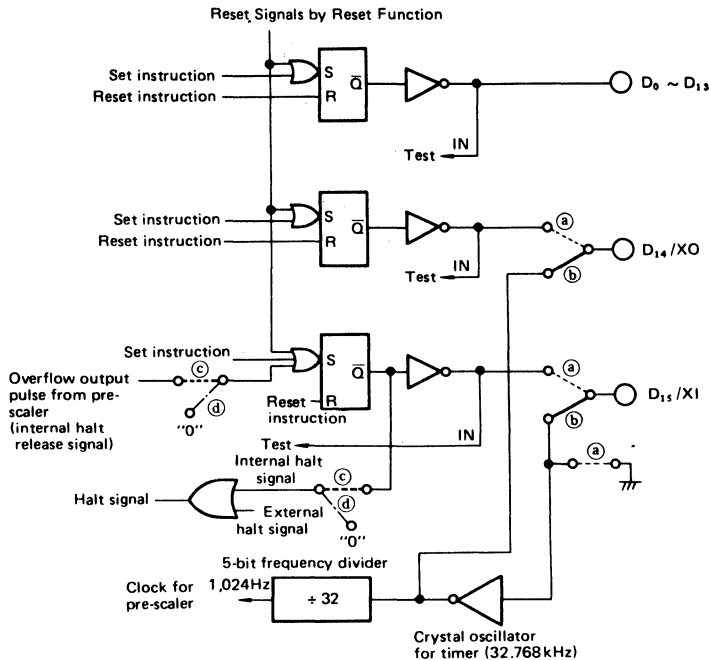


Figure 14 Mask Option of D₁₄ and D₁₅

D₀ to D₁₃ are discrete I/Os of common for input and output, D₁₄ and D₁₅ require 3 types of mask option. If there is internal halt mode, latch of D₁₅ is used as a register for internal halt mode specially.

In such case, since D₁₅ means internal halt state and D₁₅ = "1" means operating state, LSI can be in internal halt state by

resetting D₁₅ using an instruction. The pre-scaler keeps its operation in internal halt state. Therefore, D₁₅ may be set by overflow output pulse from the pre-scaler to return to operating state. For details of internal halt mode, refer to HALT FUNCTION.

Table 5 Mask Option of D₁₄/XO and D₁₅/XI Pins

Mask Option		a	b	c	d	Function of D ₁₄ /XO and D ₁₅ /XI	Function of D ₁₄ /XO and D ₁₅ /XI latch
1	Unselectable crystal oscillation for timer (no internal halt)	short	open	open	short	discrete I/O (common pin)	Output Latch
2	Selectable crystal oscillation for timer	open	short				short
3				with internal halt			
	no internal halt			short	open	Crystal Circuit Connecting Pin	

(NOTE) Users can specify this mask option in "The format of I/O channels" at ROM order.

Discrete I/O is addressed by Y register, and the set/reset instruction is executed for the addressed latch. Level ("0" or "1") of the addressed pin and 1 bit register can be tested. The test is executed by performing wired OR between the output of the latch and the pin input. Therefore, in the case

of the I/O common pins, the output latch should be in the high impedance state when the test instruction is executed. In order to test the pin input, it is necessary the state that the output latch should not affect the pin input.

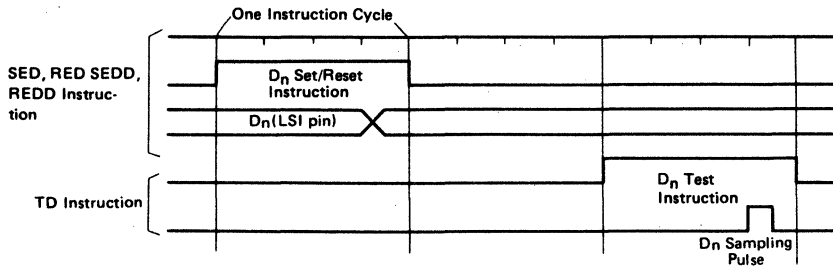


Figure 15 Timing Chart of Discrete I/O

• Data I/O (R Pin)

Table 6 Data I/O for the LCD-IV

I/O common channel	R1, R2 (2 channels)
Input channel	R0 (1 channel)
Output channel	R3 (1 channel)
Total	4 channels

(NOTE) In addition to the above, R4, R5 and R6 are provided as register setting liquid crystal display mode. In these registers, there is no pin and exists only data I/O register each, which controls liquid crystal display mode. Data is transferred to R4, R5 and R6 by LRA or LRB instruction, the same as data transfer to data I/O registers of R1, R2 and R3. For details of R4, R5 and R6, refer to LIQUID CRYSTAL DISPLAY.

4-bit register (data I/O register) is attached to each I/O common channel and output channel. No register is attached to input channel. Addressing to all channels is performed by programs (addressed by operands in instructions).

Figure 16 shows the block diagram of each channel.

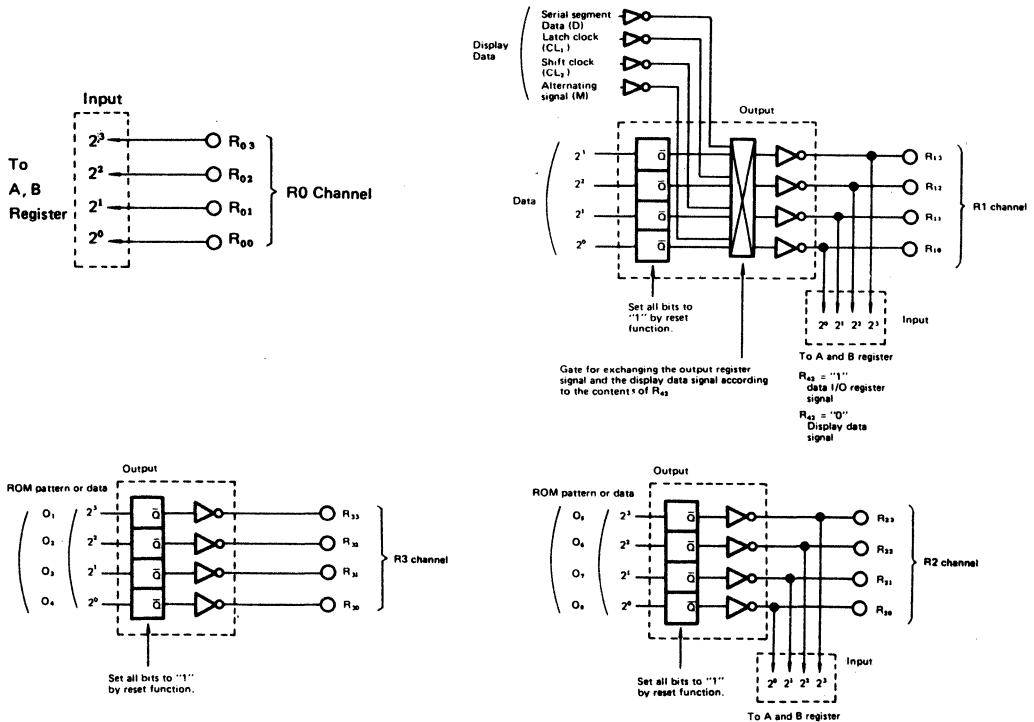


Figure 16 Data I/O Block Diagram

When expansion of segment signal for liquid crystal display is designated by a program (Register $R_{42} = "0"$), R_1 is used as a display data output pin. This prohibits R_1 to be used as an I/O common channel by users (Refer to Figure 16, R_1 channel).

If LRA or LRB instruction is executed at the time, data is transferred to data I/O register, but the content of data I/O register is not output from R_1 . If LAR or LBR instruction is executed, display data is input to accumulator (A register) or B register.

Data is transferred from the accumulator (A register) and B register to data I/O registers R_1 , R_2 , and R_3 through the bus

line. In addition, ROM bit patterns can be transferred to R_2 and R_3 by pattern generation instructions.

Input instructions input 4-bit data to the accumulator (A register) and B register through the channels R_0 , R_1 and R_2 . However, in the case of I/O common channels R_2 and R_3 , since data I/O register outputs are connected to pins, input is executed by performing wired OR between the register output and the pin input. For this reason, to input pin input signals, registers must be set to a state that would not affect the pin input.

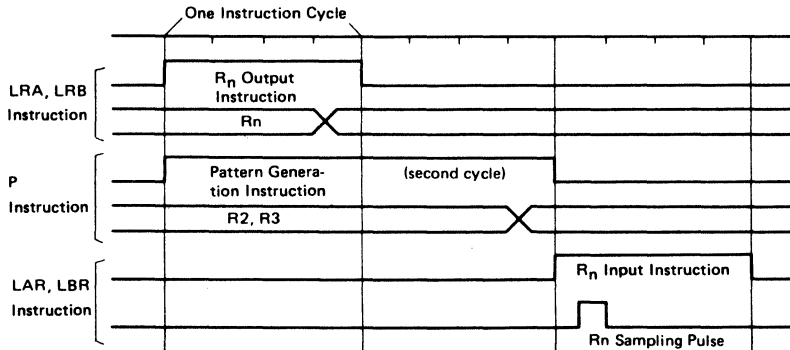
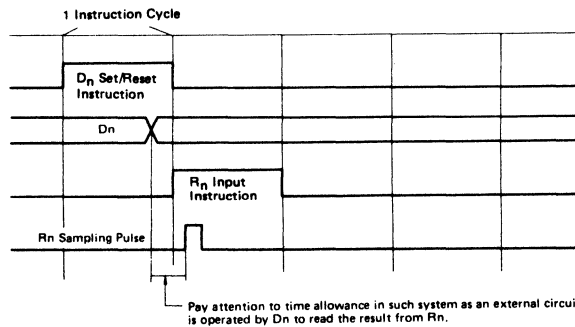


Figure 17 Data I/O Timing Chart

Pay attention: When executing an input instruction to output channel, the microcomputer reads unstabilized value causing malfunction of the program.

When executing an input instruction (LAR and LBR) from the data I/O, pay attention to time allowance after executing an output instruction. At the time, the input sampling pulse is generated during the first half of the instruction cycle.



Applied Pins: INT_0 , INT_1 , R_{00} to R_{03}

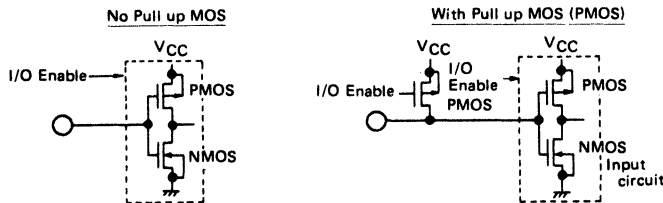


Figure 18 Configuration of Input Pins



Applied Pins: R₃₀ to R₃₃

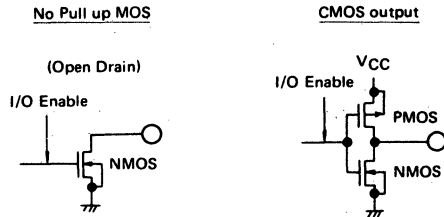


Figure 19 Configuration of Output Pins

Applied Pins: D₀ to D₁₃, D₁₄/XO, D₁₅/XI, R₁₀ to R₁₃, R₂₀ to R₂₃

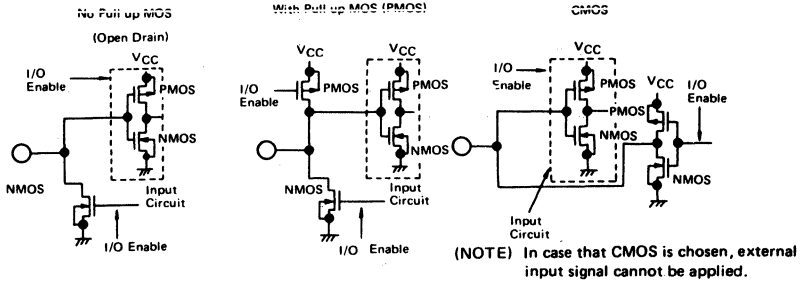


Figure 20 Configuration of Input/Output Pins

■ TIMER/COUNTER

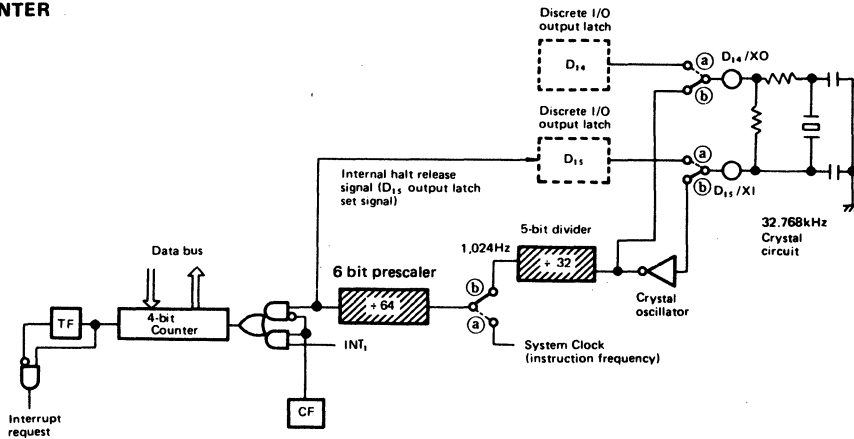


Figure 21 Timer/Counter Block Diagram



Timer/Counter Block Diagram is shown in Figure 21. 5-bit divider divides the crystal oscillation (32.768kHz) by 32 and generates clocks of 1,024Hz in the crystal oscillation mode. It does not stop in the halt state. Prescaler divides the system clock (instruction frequency) or 1,024Hz clock by 64 and generates overflow output pulse of "Instruction frequency/64Hz" or 16Hz. In the crystal oscillation mode, it does not stop during halt state. The input of the 4-bit counter is overflow output pulse of the prescaler or a pulse of INT₁ pin. Input selection is determined by CF state. Data can be exchanged between the counter and bus by LTI, LTA or LAT instruction. TF is a flip-flop which masks the interrupt of timer/counter.

The timer is operable in 2 modes (timer mode and counter mode) depending on what to count, and the mode is selected by programs.


● **Timer Mode**

The 4-bit counter counts prescaler overflow output pulses. One of the following two can be selected as the prescaler count clock by the mask option.

1. System clock (Instruction frequency)
2. 1,024Hz clock (Crystal oscillation for timer is selected.) . . .

Clock obtained by dividing the crystal oscillation (32.768kHz) for timer by 32. Crystal oscillator is constructed between D pins of D₁₄ and D₁₅:

Note 1) In this case, the overflow output pulses from the prescaler are 16Hz. These pulses are counted by the 4-bit counter to generate an interrupt of 16Hz - 1Hz.

Note 2) In this case, the part marked with  in Figure 21 Timer/Counter does not stop even in halt state. When using "internal halt mode", internal halt state is generated by resetting the register for internal halt mode (D latch: D₁₅) by an instruction (D₁₅ = "0": internal halt state, D₁₅ = "1": operating state), and all the operation stop. In this case, overflow output pulses from the prescaler work as the internal halt releasing signal and set the D₁₅ output latch.

By utilizing this function, intermittent operation is possible, that is, program execution for necessary processing (for example, counting for clock function) starts after every 62.5 msec (16Hz) and the LSI stops after execution of this program by an instruction which makes the LSI into internal halt state. This reduces the time in which the LSI operates, resulting in power consumption in substance.

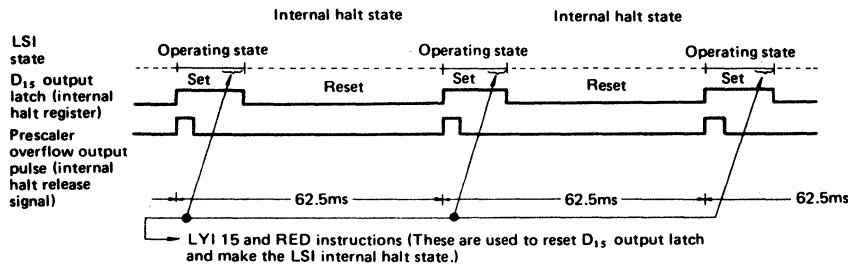


Figure 22 Set/Reset Operation Using Crystal Oscillator for Timer

● **Counter Mode**

Counts pulse of INT₁ pin.

(Note) The width of INT₁ pulse in the counter mode must be at least 2-cycle time for both the "High" and "Low"

levels.

The relation between the specified value of the counter and specified time in the Timer Mode are shown in Table 7 and 8.

Table 7 Timer Range (Prescaler clock: system clock)

Specified Value	Cycles	*Time (ms)	Specified Value	Cycles	*Time (ms)
0	1,024	5.12	8	512	2.56
1	960	4.80	9	448	2.24
2	896	4.48	10	384	1.92
3	832	4.16	11	320	1.60
4	768	3.84	12	256	1.28
5	704	3.52	13	192	0.96
6	640	3.20	14	128	0.64
7	576	2.88	15	64	0.32

* Time is based on instruction frequency 200kHz. (One Instruction Cycle Time (T_{inst}) = 5μs)



Table 8 Timer Range (Prescaler clock: 1,024 Hz)

Specified Value	* Time (ms)	Frequency (Hz)	Specified Value	* Time (ms)	Frequency
0	1,000	1	8	500	2
1	937.5	1.07	9	437.5	2.29
2	875	1.04	10	375	2.67
3	812.5	1.23	11	312.5	3.20
4	750	1.33	12	250	4
5	687.5	1.45	13	187.5	5.33
6	625	1.60	14	125	8
7	562.5	1.78	15	62.5	16

* Time is based on crystal oscillation for timer 32.768 kHz.

■ INTERRUPT

There are interrupt caused by the timer/counter or the inputs. Each interrupt factor has the interrupt request F/F and the request is latched into this flip-flop when it is generated. If an interrupt can be accepted, the interrupt is generated.

It is controlled by Interrupt Enable F/F (I/E F/F) whether an interrupt can be accepted or not.

Figure 23 shows the interrupt block diagram and Figure 24 shows the interrupt timing chart.

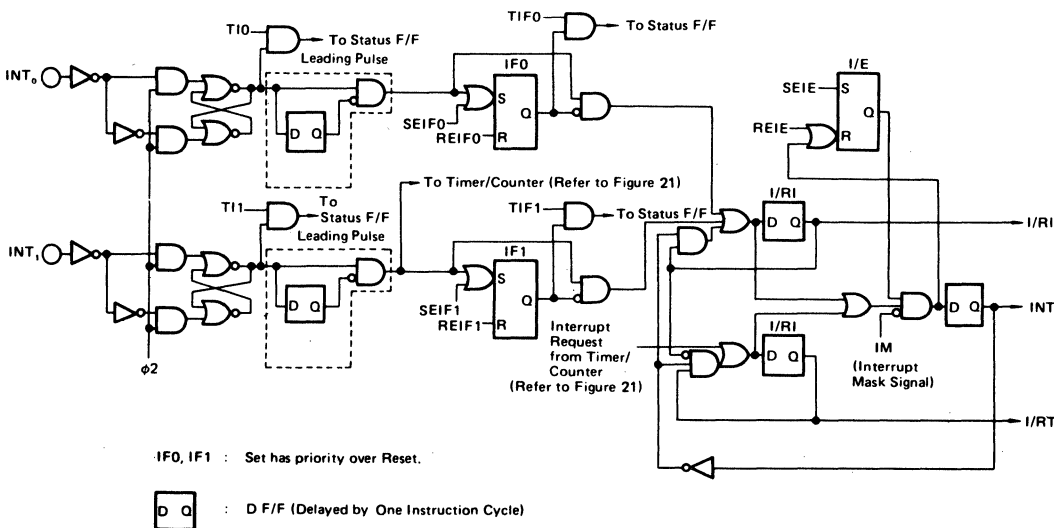


Figure 23 Interrupt Circuit Block Diagram

The status is unchanged. (The interrupt is different from general CAL in regard to this matter.)

Stacking of registers is performed by the program. Returning from the interrupt routine is performed in the same way as that from normal subroutine. But it is convenient to use RTNI (Return Interrupt) which sets the I/E simultaneously with RTN.

An interrupt is generated irrespectively of the condition of stack registers, so enough stack registers are needed.

TF, IF0, or IF1 is flip-flop where the set has priority over the reset. It is not reset when the reset instruction is issued simultaneously with OVF of the timer/counter or the leading

edge of the input, though the interrupt request is generated and latched into I/R or I/RT.

The interrupt processing caused by the interrupt generation is basically the subroutine jump and the jumping location in memory is fixed as:

- Interrupt of the timer/counter Bank 0 page 0 address 3F (00–3F)
- Interrupt of the inputs Bank 0 page 1 address 3F (01–3F)

In addition,

The saving operation of PC → ST1 → ST2 → ST3 → ST4.



I/E reset

● **Interrupt of the Inputs**

Two pins INT_0 and INT_1 have the interrupt request functions. They have the leading pulse generation circuit and the interrupt mask F/F (IF_0 , IF_1). When IF_0 or IF_1 is reset, the interrupt request is able to generate interrupt mask release. When INT_0 or INT_1 changes from "0" to "1" ("Low" level → "High" level), the leading pulse is generated and generates the interrupt request. When IF_0 or IF_1 is set, the interrupt is masked.

The interrupt request generated by the leading pulse is latched in the interrupt request F/F on the input side (I/RI). If interrupt Enable F/F (I/E) is "1", the interrupt is generated immediately and I/RI is reset. But if Interrupt Enable F/F (I/E) is "0", I/RI is held at "1" level until it gets into the

Interrupt Enable state.

IF_0 , IF_1 , INT_0 and INT_1 can be tested by the program. Therefore, they can also be used as normal input pins or latch pins of momentary pulse input.

The interrupt pulse width (at both "High" and "Low" levels) should be more than two-cycle.

● **Interrupt of the Timer/Counter**

The interrupt request of the timer/counter is latched into the interrupt request F/F of the timer (I/RT). Then I/RT operates in the same way as I/RI , but the interrupt of the input has priority over that of the timer. Therefore, the input interrupt is serviced when both I/RI and I/RT are at "1" level (interrupt requests are simultaneously generated). During the input interrupt, I/RT remains set. Thus, after the input interrupt, the timer/counter interrupt can be serviced.

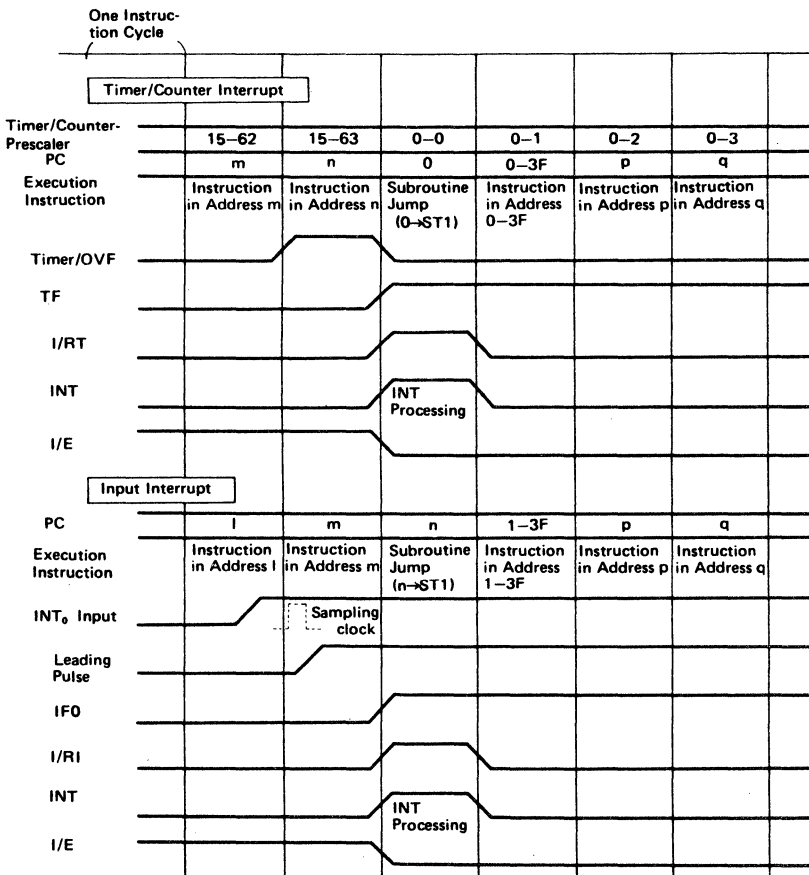


Figure 24 Interrupt Timing Chart



LCD—IV (HD613901)

■ LIQUID CRYSTAL DISPLAY

● Liquid Crystal Display Circuit

The LCD-IV can directly drive the liquid crystal display panel of static, 1/2 duty factor, 1/3 duty factor and 1/4 duty factor.

The LCD-IV has 4 common signal pins and 32 segment signal pins. Further, if liquid crystal driver LSI (HD44100H) is connected to the LCD-IV, up to 96 segment signal pins can be extended externally. Thus, in addition to the internal 32 pins, total 128 segment signal pins can be driven.

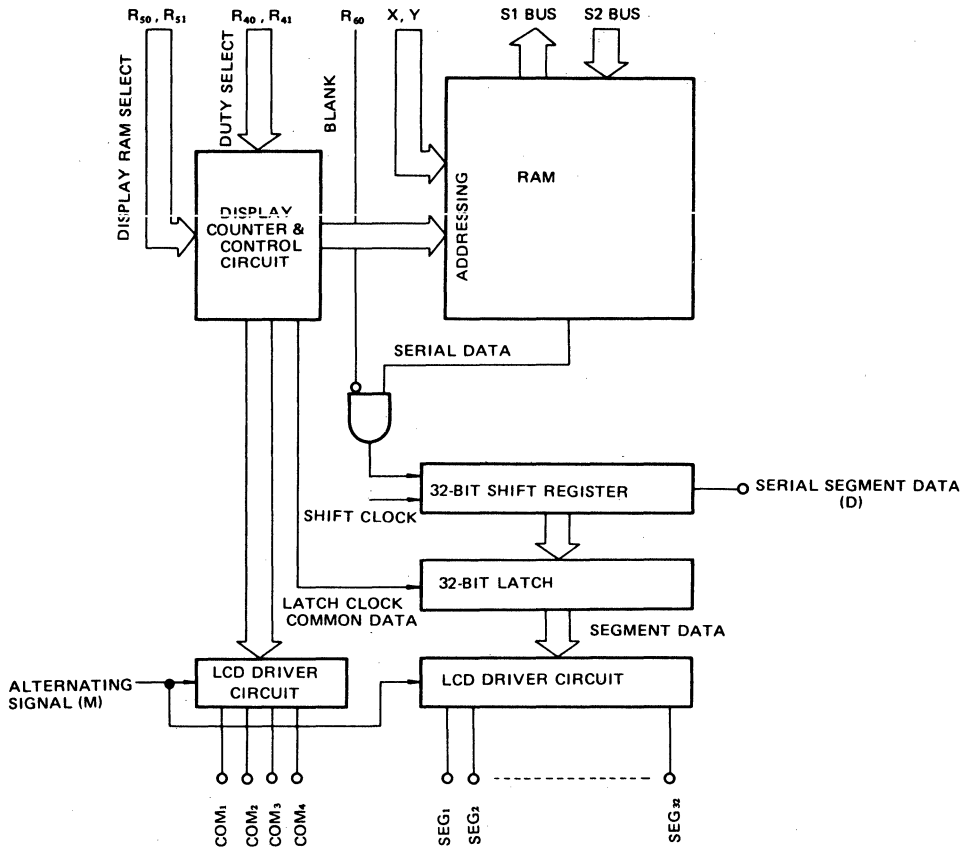


Figure 25 Liquid Crystal Display Circuit Block Diagram

Display is automatically executed by writing segment data into RAM. The RAM reads segment data bit by bit sequentially every one instruction cycle upon receiving address signal from the display counter and the control circuit. Every time common signal is scanned, the RAM reads 128-segment data (SEG₁ to SEG₁₂₈), which is correspond to common signal selected at the next time. Scan of common signal is executed every 256-instruction cycle. Therefore, the data which corresponds to 128-segment is read twice at the same time. The serial data read is converted to parallel data by the shift register and latch, converted to LCD drive signal by the liquid crystal driver and the

output from a segment pin. 32-segment (SEG₁ to SEG₃₂) out of 128-segment serial data is used within the LCD-IV, and the rest (96-segment) is output to liquid crystal driver LSI HD-44100H which is connected to the LCD-IV and is converted to LCD drive signal in the HD44100H at the time of designation of with liquid crystal segment output extension. Cycle of the latch clock is 256-instruction cycle in the LCD-IV. In the case of dynamic drive, data at the common side changes synchronously with the latch clock. These display operations are all executed regardless of program.



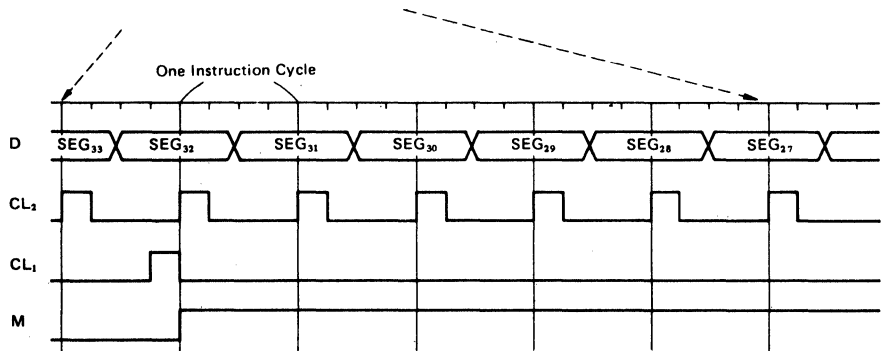
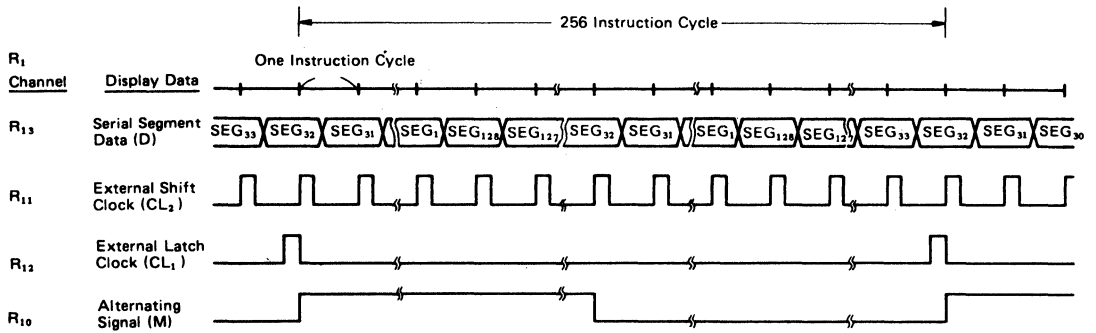


Figure 26 Display Data Timing Chart

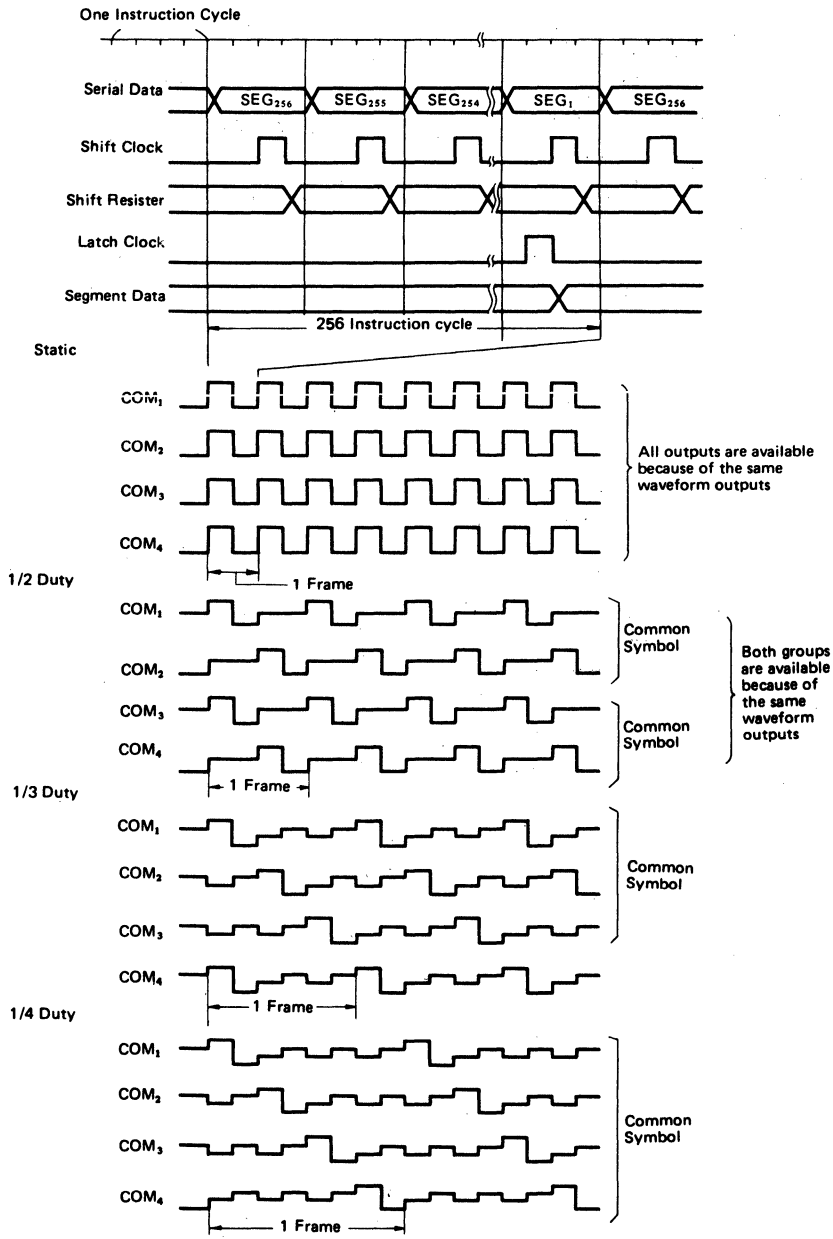


Figure 27 Liquid Crystal Display Circuit Timing Chart



● **Liquid Crystal Display Mode Setting Registers**

For selection of the liquid crystal display mode, data I/O registers of R4, R5 and R6 are used.

Table 9 Function of Liquid Crystal Display Mode Setting Registers

Selection of liquid crystal display duty factor (R ₄₀ , R ₄₁)	R ₄₁	R ₄₀	Function		
	0	0	Static		
	0	1	1/2 duty		
	1	0	1/3 duty		
	1	1	1/4 duty		
Designation of with or without liquid crystal segment output extension (R ₄₂)	R ₄₂	Function			
	0	To be extended (Outputs display data from Channel R1)			
	1	Not to be extended (Channel R1 becomes an ordinary 4-bit data I/O.)			
Liquid crystal display blanking signal (R ₆₀)	R ₆₀	Function			
	0	Outputs RAM data for liquid crystal display as segment signals.			
	1	Segment signals become non-selection status (blanking) regardless of RAM data for liquid crystal display.			
RAM designation for liquid crystal display (R ₅₀ , R ₅₁)	R ₅₁	R ₅₀	Function		
	Function varies with liquid crystal display duty factor.				
Selection of halt function and oscillation circuit for timer	R ₆₃	R ₆₂	R ₆₁	R ₆₀	Function
	/	0	0	/	Do not set in this state.
	/	0	1	/	With crystal for timer, with internal halt, XI, XO
	/	1	0	/	Without crystal for timer, D ₁₄ and D ₁₅ are general I/O.
	/	1	1	/	With crystal for timer, without internal halt, XI, XO.
I/O state at halt	0	/	/	/	Enable:
	1	/	/	/	Disable:

(NOTE) Liquid crystal display mode at resetting.

Since all bits of registers R4, R5 and R6 are set to "1" by the reset function, display mode after resetting becomes as shown below:

Liquid crystal display duty factor: 1/4 duty (R₄₀ = "1", R₄₁ = "1")

Liquid crystal segment output extension: Not extended (R₄₂ = "1")

Designation of liquid crystal display blanking: Display blanking (R₆₀ = "1")

Designation of RAM for liquid crystal display: Varies correspond to each liquid crystal display duty factor. (R₅₀ = "1", R₅₁ = "1")

Designation of crystal for timer and internal halt: With crystal for timer, without internal halt (R₆₁ = "1", R₆₂ = "1").

I/O state at halt: I/O state at halt becomes disable (R₆₃ = "1").

LCD—IV (HD613901)

● Relation between Display RAM and Segment Data

In the LCD-IV, 4 types of display duty factor (static, 1/2 duty, 1/3 duty, and 1/4 duty) can be selected by programs, and correspondence between RAM bits and segment data changes according to these duty factors.

Figure 28 shows segment signal output from the LCD-IV.

RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
6	4	2	0	0	SEG ₄	SEG ₃	SEG ₂	SEG ₁
				1	SEG ₆	SEG ₅	SEG ₄	SEG ₃
				2	SEG ₁₂	SEG ₁₁	SEG ₁₀	SEG ₉
				3	SEG ₁₈	SEG ₁₇	SEG ₁₆	SEG ₁₅
				4	SEG ₂₄	SEG ₂₃	SEG ₂₂	SEG ₂₁
				5	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇
				6	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃
				7	SEG ₄₂	SEG ₄₁	SEG ₄₀	SEG ₃₉
				8	SEG ₄₈	SEG ₄₇	SEG ₄₆	SEG ₄₅
				9	SEG ₅₄	SEG ₅₃	SEG ₅₂	SEG ₅₁
				10	SEG ₆₀	SEG ₅₉	SEG ₅₈	SEG ₅₇
				11	SEG ₆₆	SEG ₆₅	SEG ₆₄	SEG ₆₃
				12	SEG ₇₂	SEG ₇₁	SEG ₇₀	SEG ₆₉
				13	SEG ₇₈	SEG ₇₇	SEG ₇₆	SEG ₇₅
				14	SEG ₈₄	SEG ₈₃	SEG ₈₂	SEG ₈₁
				15	SEG ₉₀	SEG ₈₉	SEG ₈₈	SEG ₈₇
7	5	3	1	0	SEG ₈	SEG ₇	SEG ₆	SEG ₅
				1	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁
				2	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇
				3	SEG ₂₆	SEG ₂₅	SEG ₂₄	SEG ₂₃
				4	SEG ₃₂	SEG ₃₁	SEG ₃₀	SEG ₂₉
				5	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅
				6	SEG ₄₄	SEG ₄₃	SEG ₄₂	SEG ₄₁
				7	SEG ₅₀	SEG ₄₉	SEG ₄₈	SEG ₄₇
				8	SEG ₅₆	SEG ₅₅	SEG ₅₄	SEG ₅₃
				9	SEG ₆₂	SEG ₆₁	SEG ₆₀	SEG ₅₉
				10	SEG ₆₈	SEG ₆₇	SEG ₆₆	SEG ₆₅
				11	SEG ₇₄	SEG ₇₃	SEG ₇₂	SEG ₇₁
				12	SEG ₈₀	SEG ₇₉	SEG ₇₈	SEG ₇₇
				13	SEG ₈₆	SEG ₈₅	SEG ₈₄	SEG ₈₃
				14	SEG ₉₂	SEG ₉₁	SEG ₉₀	SEG ₈₉
				15	SEG ₉₈	SEG ₉₇	SEG ₉₆	SEG ₉₅

(NOTE) The SEG₃₃ to SEG₁₂₈ are extended segments.

R ₅₀	0	1	0	1
R ₅₁	0	0	1	1

Figure 28 Relation between RAM for LCD & Segment Data (Static)

RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
6	4	2	0	0	SEG ₈	SEG ₇	SEG ₆	SEG ₅
				1	SEG ₁₄	SEG ₁₃	SEG ₁₂	SEG ₁₁
				2	SEG ₂₀	SEG ₁₉	SEG ₁₈	SEG ₁₇
				3	SEG ₂₆	SEG ₂₅	SEG ₂₄	SEG ₂₃
				4	SEG ₃₂	SEG ₃₁	SEG ₃₀	SEG ₂₉
				5	SEG ₃₈	SEG ₃₇	SEG ₃₆	SEG ₃₅
				6	SEG ₄₄	SEG ₄₃	SEG ₄₂	SEG ₄₁
				7	SEG ₅₀	SEG ₄₉	SEG ₄₈	SEG ₄₇
				8	SEG ₅₆	SEG ₅₅	SEG ₅₄	SEG ₅₃
				9	SEG ₆₂	SEG ₆₁	SEG ₆₀	SEG ₅₉
				10	SEG ₆₈	SEG ₆₇	SEG ₆₆	SEG ₆₅
				11	SEG ₇₄	SEG ₇₃	SEG ₇₂	SEG ₇₁
				12	SEG ₈₀	SEG ₇₉	SEG ₇₈	SEG ₇₇
				13	SEG ₈₆	SEG ₈₅	SEG ₈₄	SEG ₈₃
				14	SEG ₉₂	SEG ₉₁	SEG ₉₀	SEG ₈₉
				15	SEG ₉₈	SEG ₉₇	SEG ₉₆	SEG ₉₅
7	5	3	1	0	SEG ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃
				1	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉
				2	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅
				3	SEG ₃₄	SEG ₃₃	SEG ₃₂	SEG ₃₁
				4	SEG ₄₀	SEG ₃₉	SEG ₃₈	SEG ₃₇
				5	SEG ₄₆	SEG ₄₅	SEG ₄₄	SEG ₄₃
				6	SEG ₅₂	SEG ₅₁	SEG ₅₀	SEG ₄₉
				7	SEG ₅₈	SEG ₅₇	SEG ₅₆	SEG ₅₅
				8	SEG ₆₄	SEG ₆₃	SEG ₆₂	SEG ₆₁
				9	SEG ₇₀	SEG ₆₉	SEG ₆₈	SEG ₆₇
				10	SEG ₇₆	SEG ₇₅	SEG ₇₄	SEG ₇₃
				11	SEG ₈₂	SEG ₈₁	SEG ₈₀	SEG ₇₉
				12	SEG ₈₈	SEG ₈₇	SEG ₈₆	SEG ₈₅
				13	SEG ₉₄	SEG ₉₃	SEG ₉₂	SEG ₉₁
				14	SEG ₁₀₀	SEG ₉₉	SEG ₉₈	SEG ₉₇
				15	SEG ₁₀₆	SEG ₁₀₅	SEG ₁₀₄	SEG ₁₀₃
4	6	0	2	0	SEG ₁₆	SEG ₁₅	SEG ₁₄	SEG ₁₃
				1	SEG ₂₂	SEG ₂₁	SEG ₂₀	SEG ₁₉
				2	SEG ₂₈	SEG ₂₇	SEG ₂₆	SEG ₂₅
				3	SEG ₃₄	SEG ₃₃	SEG ₃₂	SEG ₃₁
				4	SEG ₄₀	SEG ₃₉	SEG ₃₈	SEG ₃₇
				5	SEG ₄₆	SEG ₄₅	SEG ₄₄	SEG ₄₃
				6	SEG ₅₂	SEG ₅₁	SEG ₅₀	SEG ₄₉
				7	SEG ₅₈	SEG ₅₇	SEG ₅₆	SEG ₅₅
				8	SEG ₆₄	SEG ₆₃	SEG ₆₂	SEG ₆₁
				9	SEG ₇₀	SEG ₆₉	SEG ₆₈	SEG ₆₇
				10	SEG ₇₆	SEG ₇₅	SEG ₇₄	SEG ₇₃
				11	SEG ₈₂	SEG ₈₁	SEG ₈₀	SEG ₇₉
				12	SEG ₈₈	SEG ₈₇	SEG ₈₆	SEG ₈₅
				13	SEG ₉₄	SEG ₉₃	SEG ₉₂	SEG ₉₁
				14	SEG ₁₀₀	SEG ₉₉	SEG ₉₈	SEG ₉₇
				15	SEG ₁₀₆	SEG ₁₀₅	SEG ₁₀₄	SEG ₁₀₃
5	7	1	3	0	SEG ₂₄	SEG ₂₃	SEG ₂₂	SEG ₂₁
				1	SEG ₃₀	SEG ₂₉	SEG ₂₈	SEG ₂₇
				2	SEG ₃₆	SEG ₃₅	SEG ₃₄	SEG ₃₃
				3	SEG ₄₂	SEG ₄₁	SEG ₄₀	SEG ₃₉
				4	SEG ₄₈	SEG ₄₇	SEG ₄₆	SEG ₄₅
				5	SEG ₅₄	SEG ₅₃	SEG ₅₂	SEG ₅₁
				6	SEG ₆₀	SEG ₅₉	SEG ₅₈	SEG ₅₇
				7	SEG ₆₆	SEG ₆₅	SEG ₆₄	SEG ₆₃
				8	SEG ₇₂	SEG ₇₁	SEG ₇₀	SEG ₆₉
				9	SEG ₇₈	SEG ₇₇	SEG ₇₆	SEG ₇₅
				10	SEG ₈₄	SEG ₈₃	SEG ₈₂	SEG ₈₁
				11	SEG ₉₀	SEG ₈₉	SEG ₈₈	SEG ₈₇
				12	SEG ₉₆	SEG ₉₅	SEG ₉₄	SEG ₉₃
				13	SEG ₁₀₂	SEG ₁₀₁	SEG ₁₀₀	SEG ₉₉
				14	SEG ₁₀₈	SEG ₁₀₇	SEG ₁₀₆	SEG ₁₀₅
				15	SEG ₁₁₄	SEG ₁₁₃	SEG ₁₁₂	SEG ₁₁₁

R ₅₀	0	1	0	1
R ₅₁	0	0	1	1

Figure 29 Relation between RAM for LCD & Segment Data (1/2 Duty, 1/2 Bias)



RAM Address					RAM			
X					Y	2 ³	2 ¹	2 ⁰
6	4	2	0	0	SEG ₁	SEG ₁	SEG ₁	
				1	SEG ₂	SEG ₂	SEG ₂	
				2	SEG ₃	SEG ₃	SEG ₃	
				3	SEG ₄	SEG ₄	SEG ₄	
				4	SEG ₅	SEG ₅	SEG ₅	
				5	SEG ₆	SEG ₆	SEG ₆	
				6	SEG ₇	SEG ₇	SEG ₇	
				7	SEG ₈	SEG ₈	SEG ₈	
				8	SEG ₉	SEG ₉	SEG ₉	
				9	SEG ₁₀	SEG ₁₀	SEG ₁₀	
				10	SEG ₁₁	SEG ₁₁	SEG ₁₁	
				11	SEG ₁₂	SEG ₁₂	SEG ₁₂	
				12	SEG ₁₃	SEG ₁₃	SEG ₁₃	
				13	SEG ₁₄	SEG ₁₄	SEG ₁₄	
				14	SEG ₁₅	SEG ₁₅	SEG ₁₅	
				15	SEG ₁₆	SEG ₁₆	SEG ₁₆	
7	5	3	1	0	SEG ₁₇	SEG ₁₇	SEG ₁₇	
				1	SEG ₁₈	SEG ₁₈	SEG ₁₈	
				2	SEG ₁₉	SEG ₁₉	SEG ₁₉	
				3	SEG ₂₀	SEG ₂₀	SEG ₂₀	
				4	SEG ₂₁	SEG ₂₁	SEG ₂₁	
				5	SEG ₂₂	SEG ₂₂	SEG ₂₂	
				6	SEG ₂₃	SEG ₂₃	SEG ₂₃	
				7	SEG ₂₄	SEG ₂₄	SEG ₂₄	
				8	SEG ₂₅	SEG ₂₅	SEG ₂₅	
				9	SEG ₂₆	SEG ₂₆	SEG ₂₆	
				10	SEG ₂₇	SEG ₂₇	SEG ₂₇	
				11	SEG ₂₈	SEG ₂₈	SEG ₂₈	
				12	SEG ₂₉	SEG ₂₉	SEG ₂₉	
				13	SEG ₃₀	SEG ₃₀	SEG ₃₀	
				14	SEG ₃₁	SEG ₃₁	SEG ₃₁	
				15	SEG ₃₂	SEG ₃₂	SEG ₃₂	
4	6	0	2	0	SEG ₃₃	SEG ₃₃	SEG ₃₃	
				1	SEG ₃₄	SEG ₃₄	SEG ₃₄	
				2	SEG ₃₅	SEG ₃₅	SEG ₃₅	
				3	SEG ₃₆	SEG ₃₆	SEG ₃₆	
				4	SEG ₃₇	SEG ₃₇	SEG ₃₇	
				5	SEG ₃₈	SEG ₃₈	SEG ₃₈	
				6	SEG ₃₉	SEG ₃₉	SEG ₃₉	
				7	SEG ₄₀	SEG ₄₀	SEG ₄₀	
				8	SEG ₄₁	SEG ₄₁	SEG ₄₁	
				9	SEG ₄₂	SEG ₄₂	SEG ₄₂	
				10	SEG ₄₃	SEG ₄₃	SEG ₄₃	
				11	SEG ₄₄	SEG ₄₄	SEG ₄₄	
				12	SEG ₄₅	SEG ₄₅	SEG ₄₅	
				13	SEG ₄₆	SEG ₄₆	SEG ₄₆	
				14	SEG ₄₇	SEG ₄₇	SEG ₄₇	
				15	SEG ₄₈	SEG ₄₈	SEG ₄₈	
5	7	1	3	0	SEG ₄₉	SEG ₄₉	SEG ₄₉	
				1	SEG ₅₀	SEG ₅₀	SEG ₅₀	
				2	SEG ₅₁	SEG ₅₁	SEG ₅₁	
				3	SEG ₅₂	SEG ₅₂	SEG ₅₂	
				4	SEG ₅₃	SEG ₅₃	SEG ₅₃	
				5	SEG ₅₄	SEG ₅₄	SEG ₅₄	
				6	SEG ₅₅	SEG ₅₅	SEG ₅₅	
				7	SEG ₅₆	SEG ₅₆	SEG ₅₆	
				8	SEG ₅₇	SEG ₅₇	SEG ₅₇	
				9	SEG ₅₈	SEG ₅₈	SEG ₅₈	
				10	SEG ₅₉	SEG ₅₉	SEG ₅₉	
				11	SEG ₆₀	SEG ₆₀	SEG ₆₀	
				12	SEG ₆₁	SEG ₆₁	SEG ₆₁	
				13	SEG ₆₂	SEG ₆₂	SEG ₆₂	
				14	SEG ₆₃	SEG ₆₃	SEG ₆₃	
				15	SEG ₆₄	SEG ₆₄	SEG ₆₄	

RAM Address					RAM			
X					Y	2 ³	2 ¹	2 ⁰
2	0	6	4	0	SEG ₆₅	SEG ₆₅	SEG ₆₅	
				1	SEG ₆₆	SEG ₆₆	SEG ₆₆	
				2	SEG ₆₇	SEG ₆₇	SEG ₆₇	
				3	SEG ₆₈	SEG ₆₈	SEG ₆₈	
				4	SEG ₆₉	SEG ₆₉	SEG ₆₉	
				5	SEG ₇₀	SEG ₇₀	SEG ₇₀	
				6	SEG ₇₁	SEG ₇₁	SEG ₇₁	
				7	SEG ₇₂	SEG ₇₂	SEG ₇₂	
				8	SEG ₇₃	SEG ₇₃	SEG ₇₃	
				9	SEG ₇₄	SEG ₇₄	SEG ₇₄	
				10	SEG ₇₅	SEG ₇₅	SEG ₇₅	
				11	SEG ₇₆	SEG ₇₆	SEG ₇₆	
				12	SEG ₇₇	SEG ₇₇	SEG ₇₇	
				13	SEG ₇₈	SEG ₇₈	SEG ₇₈	
				14	SEG ₇₉	SEG ₇₉	SEG ₇₉	
				15	SEG ₈₀	SEG ₈₀	SEG ₈₀	
3	1	7	5	0	SEG ₈₁	SEG ₈₁	SEG ₈₁	
				1	SEG ₈₂	SEG ₈₂	SEG ₈₂	
				2	SEG ₈₃	SEG ₈₃	SEG ₈₃	
				3	SEG ₈₄	SEG ₈₄	SEG ₈₄	
				4	SEG ₈₅	SEG ₈₅	SEG ₈₅	
				5	SEG ₈₆	SEG ₈₆	SEG ₈₆	
				6	SEG ₈₇	SEG ₈₇	SEG ₈₇	
				7	SEG ₈₈	SEG ₈₈	SEG ₈₈	
				8	SEG ₈₉	SEG ₈₉	SEG ₈₉	
				9	SEG ₉₀	SEG ₉₀	SEG ₉₀	
				10	SEG ₉₁	SEG ₉₁	SEG ₉₁	
				11	SEG ₉₂	SEG ₉₂	SEG ₉₂	
				12	SEG ₉₃	SEG ₉₃	SEG ₉₃	
				13	SEG ₉₄	SEG ₉₄	SEG ₉₄	
				14	SEG ₉₅	SEG ₉₅	SEG ₉₅	
				15	SEG ₉₆	SEG ₉₆	SEG ₉₆	
0	2	4	6	0	SEG ₉₇	SEG ₉₇	SEG ₉₇	
				1	SEG ₉₈	SEG ₉₈	SEG ₉₈	
				2	SEG ₉₉	SEG ₉₉	SEG ₉₉	
				3	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀	
				4	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁	
				5	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂	
				6	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃	
				7	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄	
				8	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅	
				9	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆	
				10	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇	
				11	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈	
				12	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉	
				13	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀	
				14	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁	
				15	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂	
1	3	5	7	0	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃	
				1	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄	
				2	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅	
				3	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆	
				4	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇	
				5	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈	
				6	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉	
				7	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀	
				8	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁	
				9	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂	
				10	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃	
				11	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄	
				12	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅	
				13	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆	
				14	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇	
				15	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈	

R ₅₀	0	1	0	1	COM ₃	COM ₂	COM ₁
R ₅₁	0	0	1	1			

R ₆₀	0	1	0	1	COM ₃	COM ₂	COM ₁
R ₆₁	0	0	1	1			

Figure 30 Relation between RAM for LCD & Segment Data (1/3 Duty, 1/3 Bias)



RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
6	4	2	0	0	SEG ₁	SEG ₁	SEG ₁	SEG ₁
				1	SEG ₂	SEG ₂	SEG ₂	SEG ₂
				2	SEG ₃	SEG ₃	SEG ₃	SEG ₃
				3	SEG ₄	SEG ₄	SEG ₄	SEG ₄
				4	SEG ₅	SEG ₅	SEG ₅	SEG ₅
				5	SEG ₆	SEG ₆	SEG ₆	SEG ₆
				6	SEG ₇	SEG ₇	SEG ₇	SEG ₇
				7	SEG ₈	SEG ₈	SEG ₈	SEG ₈
				8	SEG ₉	SEG ₉	SEG ₉	SEG ₉
				9	SEG ₁₀	SEG ₁₀	SEG ₁₀	SEG ₁₀
				10	SEG ₁₁	SEG ₁₁	SEG ₁₁	SEG ₁₁
				11	SEG ₁₂	SEG ₁₂	SEG ₁₂	SEG ₁₂
				12	SEG ₁₃	SEG ₁₃	SEG ₁₃	SEG ₁₃
				13	SEG ₁₄	SEG ₁₄	SEG ₁₄	SEG ₁₄
				14	SEG ₁₅	SEG ₁₅	SEG ₁₅	SEG ₁₅
15	SEG ₁₆	SEG ₁₆	SEG ₁₆	SEG ₁₆				
7	5	3	1	0	SEG ₁₇	SEG ₁₇	SEG ₁₇	SEG ₁₇
				1	SEG ₁₈	SEG ₁₈	SEG ₁₈	SEG ₁₈
				2	SEG ₁₉	SEG ₁₉	SEG ₁₉	SEG ₁₉
				3	SEG ₂₀	SEG ₂₀	SEG ₂₀	SEG ₂₀
				4	SEG ₂₁	SEG ₂₁	SEG ₂₁	SEG ₂₁
				5	SEG ₂₂	SEG ₂₂	SEG ₂₂	SEG ₂₂
				6	SEG ₂₃	SEG ₂₃	SEG ₂₃	SEG ₂₃
				7	SEG ₂₄	SEG ₂₄	SEG ₂₄	SEG ₂₄
				8	SEG ₂₅	SEG ₂₅	SEG ₂₅	SEG ₂₅
				9	SEG ₂₆	SEG ₂₆	SEG ₂₆	SEG ₂₆
				10	SEG ₂₇	SEG ₂₇	SEG ₂₇	SEG ₂₇
				11	SEG ₂₈	SEG ₂₈	SEG ₂₈	SEG ₂₈
				12	SEG ₂₉	SEG ₂₉	SEG ₂₉	SEG ₂₉
				13	SEG ₃₀	SEG ₃₀	SEG ₃₀	SEG ₃₀
				14	SEG ₃₁	SEG ₃₁	SEG ₃₁	SEG ₃₁
15	SEG ₃₂	SEG ₃₂	SEG ₃₂	SEG ₃₂				
4	6	0	2	0	SEG ₃₃	SEG ₃₃	SEG ₃₃	SEG ₃₃
				1	SEG ₃₄	SEG ₃₄	SEG ₃₄	SEG ₃₄
				2	SEG ₃₅	SEG ₃₅	SEG ₃₅	SEG ₃₅
				3	SEG ₃₆	SEG ₃₆	SEG ₃₆	SEG ₃₆
				4	SEG ₃₇	SEG ₃₇	SEG ₃₇	SEG ₃₇
				5	SEG ₃₈	SEG ₃₈	SEG ₃₈	SEG ₃₈
				6	SEG ₃₉	SEG ₃₉	SEG ₃₉	SEG ₃₉
				7	SEG ₄₀	SEG ₄₀	SEG ₄₀	SEG ₄₀
				8	SEG ₄₁	SEG ₄₁	SEG ₄₁	SEG ₄₁
				9	SEG ₄₂	SEG ₄₂	SEG ₄₂	SEG ₄₂
				10	SEG ₄₃	SEG ₄₃	SEG ₄₃	SEG ₄₃
				11	SEG ₄₄	SEG ₄₄	SEG ₄₄	SEG ₄₄
				12	SEG ₄₅	SEG ₄₅	SEG ₄₅	SEG ₄₅
				13	SEG ₄₆	SEG ₄₆	SEG ₄₆	SEG ₄₆
				14	SEG ₄₇	SEG ₄₇	SEG ₄₇	SEG ₄₇
15	SEG ₄₈	SEG ₄₈	SEG ₄₈	SEG ₄₈				
5	7	1	3	0	SEG ₄₉	SEG ₄₉	SEG ₄₉	SEG ₄₉
				1	SEG ₅₀	SEG ₅₀	SEG ₅₀	SEG ₅₀
				2	SEG ₅₁	SEG ₅₁	SEG ₅₁	SEG ₅₁
				3	SEG ₅₂	SEG ₅₂	SEG ₅₂	SEG ₅₂
				4	SEG ₅₃	SEG ₅₃	SEG ₅₃	SEG ₅₃
				5	SEG ₅₄	SEG ₅₄	SEG ₅₄	SEG ₅₄
				6	SEG ₅₅	SEG ₅₅	SEG ₅₅	SEG ₅₅
				7	SEG ₅₆	SEG ₅₆	SEG ₅₆	SEG ₅₆
				8	SEG ₅₇	SEG ₅₇	SEG ₅₇	SEG ₅₇
				9	SEG ₅₈	SEG ₅₈	SEG ₅₈	SEG ₅₈
				10	SEG ₅₉	SEG ₅₉	SEG ₅₉	SEG ₅₉
				11	SEG ₆₀	SEG ₆₀	SEG ₆₀	SEG ₆₀
				12	SEG ₆₁	SEG ₆₁	SEG ₆₁	SEG ₆₁
				13	SEG ₆₂	SEG ₆₂	SEG ₆₂	SEG ₆₂
				14	SEG ₆₃	SEG ₆₃	SEG ₆₃	SEG ₆₃
15	SEG ₆₄	SEG ₆₄	SEG ₆₄	SEG ₆₄				

RAM Address				RAM				
X				Y	2 ³	2 ²	2 ¹	2 ⁰
2	0	6	4	0	SEG ₆₅	SEG ₆₅	SEG ₆₅	SEG ₆₅
				1	SEG ₆₆	SEG ₆₆	SEG ₆₆	SEG ₆₆
				2	SEG ₆₇	SEG ₆₇	SEG ₆₇	SEG ₆₇
				3	SEG ₆₈	SEG ₆₈	SEG ₆₈	SEG ₆₈
				4	SEG ₆₉	SEG ₆₉	SEG ₆₉	SEG ₆₉
				5	SEG ₇₀	SEG ₇₀	SEG ₇₀	SEG ₇₀
				6	SEG ₇₁	SEG ₇₁	SEG ₇₁	SEG ₇₁
				7	SEG ₇₂	SEG ₇₂	SEG ₇₂	SEG ₇₂
				8	SEG ₇₃	SEG ₇₃	SEG ₇₃	SEG ₇₃
				9	SEG ₇₄	SEG ₇₄	SEG ₇₄	SEG ₇₄
				10	SEG ₇₅	SEG ₇₅	SEG ₇₅	SEG ₇₅
				11	SEG ₇₆	SEG ₇₆	SEG ₇₆	SEG ₇₆
				12	SEG ₇₇	SEG ₇₇	SEG ₇₇	SEG ₇₇
				13	SEG ₇₈	SEG ₇₈	SEG ₇₈	SEG ₇₈
				14	SEG ₇₉	SEG ₇₉	SEG ₇₉	SEG ₇₉
15	SEG ₈₀	SEG ₈₀	SEG ₈₀	SEG ₈₀				
3	1	7	5	0	SEG ₈₁	SEG ₈₁	SEG ₈₁	SEG ₈₁
				1	SEG ₈₂	SEG ₈₂	SEG ₈₂	SEG ₈₂
				2	SEG ₈₃	SEG ₈₃	SEG ₈₃	SEG ₈₃
				3	SEG ₈₄	SEG ₈₄	SEG ₈₄	SEG ₈₄
				4	SEG ₈₅	SEG ₈₅	SEG ₈₅	SEG ₈₅
				5	SEG ₈₆	SEG ₈₆	SEG ₈₆	SEG ₈₆
				6	SEG ₈₇	SEG ₈₇	SEG ₈₇	SEG ₈₇
				7	SEG ₈₈	SEG ₈₈	SEG ₈₈	SEG ₈₈
				8	SEG ₈₉	SEG ₈₉	SEG ₈₉	SEG ₈₉
				9	SEG ₉₀	SEG ₉₀	SEG ₉₀	SEG ₉₀
				10	SEG ₉₁	SEG ₉₁	SEG ₉₁	SEG ₉₁
				11	SEG ₉₂	SEG ₉₂	SEG ₉₂	SEG ₉₂
				12	SEG ₉₃	SEG ₉₃	SEG ₉₃	SEG ₉₃
				13	SEG ₉₄	SEG ₉₄	SEG ₉₄	SEG ₉₄
				14	SEG ₉₅	SEG ₉₅	SEG ₉₅	SEG ₉₅
15	SEG ₉₆	SEG ₉₆	SEG ₉₆	SEG ₉₆				
0	2	4	6	0	SEG ₉₇	SEG ₉₇	SEG ₉₇	SEG ₉₇
				1	SEG ₉₈	SEG ₉₈	SEG ₉₈	SEG ₉₈
				2	SEG ₉₉	SEG ₉₉	SEG ₉₉	SEG ₉₉
				3	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀	SEG ₁₀₀
				4	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁	SEG ₁₀₁
				5	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂	SEG ₁₀₂
				6	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃	SEG ₁₀₃
				7	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄	SEG ₁₀₄
				8	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅	SEG ₁₀₅
				9	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆	SEG ₁₀₆
				10	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇	SEG ₁₀₇
				11	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈	SEG ₁₀₈
				12	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉	SEG ₁₀₉
				13	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀	SEG ₁₁₀
				14	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁	SEG ₁₁₁
15	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂	SEG ₁₁₂				
1	3	5	7	0	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃	SEG ₁₁₃
				1	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄	SEG ₁₁₄
				2	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅	SEG ₁₁₅
				3	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆	SEG ₁₁₆
				4	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇	SEG ₁₁₇
				5	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈	SEG ₁₁₈
				6	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉	SEG ₁₁₉
				7	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀	SEG ₁₂₀
				8	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁	SEG ₁₂₁
				9	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂	SEG ₁₂₂
				10	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃	SEG ₁₂₃
				11	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄	SEG ₁₂₄
				12	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅	SEG ₁₂₅
				13	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆	SEG ₁₂₆
				14	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇	SEG ₁₂₇
15	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈	SEG ₁₂₈				

R ₅₀	0	1	0	1				
R ₅₁	0	0	1	1	COM ₄	COM ₃	COM ₂	COM ₁

R ₅₀	0	1	0	1				
R ₅₁	0	0	1	1	COM ₄	COM ₃	COM ₂	COM ₁

Figure 31 Relation between RAM for LCD & Segment Data (1/4 Duty, 1/3 Bias)



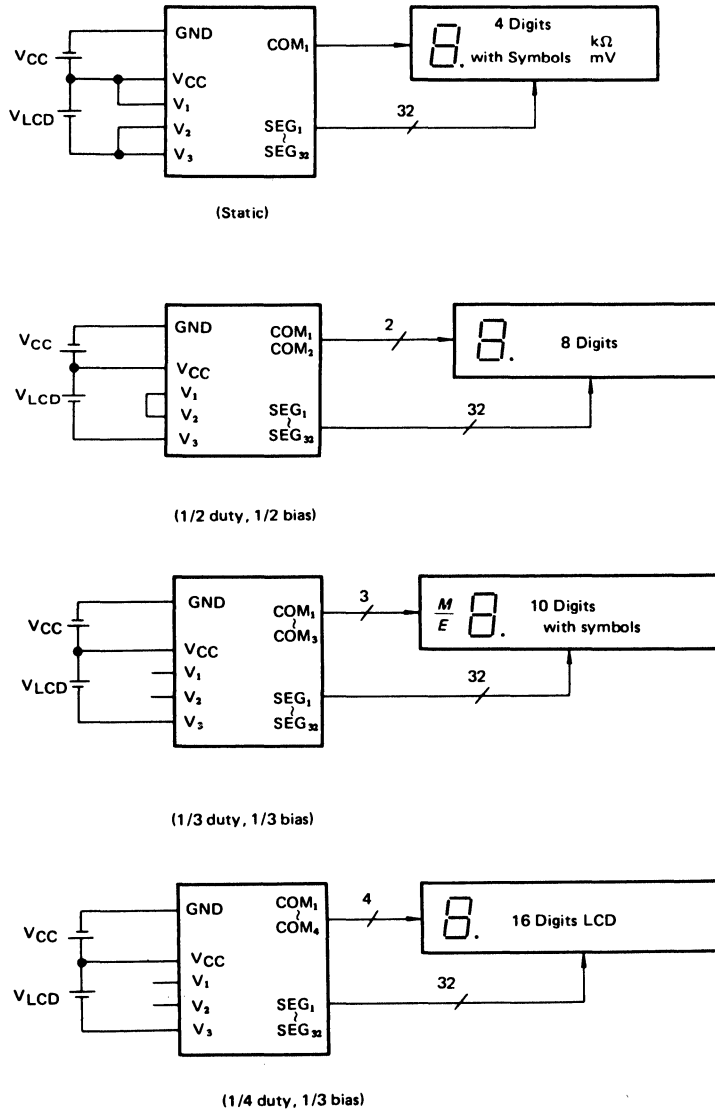


Figure 32 LCD Wiring Samples

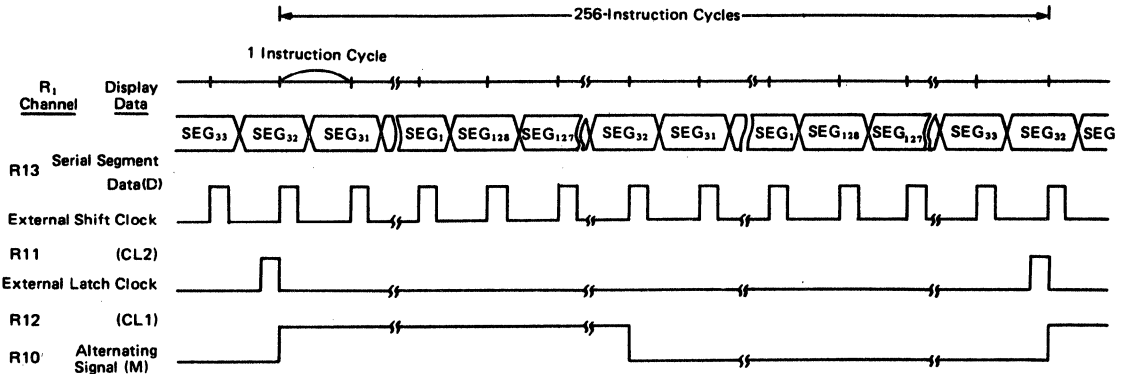
LCD—IV (HD613901)

● Extension of Display Function

Number of display digits can be increased by externally connecting an LCD driver LSI HD44100H to the LCD-IV.

The HD44100H consists of shift registers and latch and liquid crystal drive circuit. When connected with the LCD-IV, the HD44100H is used as a circuit for segment. In the LCD-

IV, 128 segments display data is sent to the 32-bit shift register from RAM constantly. When R_{42} is set to "0", the R1 channel outputs the 32nd stage output D of the shift register, shift clock CL_2 , latch clock CL_1 and AC signal M. Therefore, up to 96 segment pins of SEG_{33} to SEG_{128} can be added by directly connecting the HD44100H.



■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the LCD-IV gets into operation by setting it to "0" ("Low" level).

Internal state of the LCD-IV are specified as follows by the reset function.

- Program Counter (PC) is set to Bank 1 Page 63 Address 3F.
- IR/I, IR/T, I/E and CF are reset to "0".
- IF0, IF1 and TF are set to "1".
- Data I/O Registers and Discrete I/O Latches (R1, R2, R3, D₀ to D₁₅) are all set to "1".
- Bank Register R₇₀ is set to "1" (Jumps to Bank 0 by execution of LPU instruction after the reset).
- Liquid Crystal Display all bits of display mode setting register (Data I/O Register) R4, R5, R6 are set to "1".

(Note) All the other logic blocks (the Stack Registers, the Status F/F, the accumulator, the Carry F/F, the registers, the Timer/Counter, RAM) are not cleared by the reset function.

■ HALT FUNCTION

The LCD-IV is provided with halt function. The halt function reduces power consumption in the halt state by temporarily stopping all statuses including RAM. When halt is released, operation restarts from the state before the halt.

HALT state is kept 16-instruction after receiving halt releasing signal. (Internal, External)

The user can select one of the following I/O status at the time of halt based on the "MASK OPTION LIST" when ordering ROM:

- All I/O statuses are kept as the state immediately before the halt.
 - All I/O statuses are held in the high impedance state (both PMOS and NMOS are off, and pull-up MOS is off).
- There are the following two types of halt :

- 1) External Halt (Halt state is generated by using \overline{HLT} pin)

All operations stop when the \overline{HLT} pin is set to the "0" level (Low). When the \overline{HLT} pin is set to the "1" level (High), operation restarts from the state immediately before the halt.

2) Internal Halt (Halt state is generated by programs)

The user can select availability of internal halt at ROM ordering based on the "MASK OPTION LIST". When internal halt is selected, timer crystal should be attached externally. Therefore, the D₁₄/XO and D₁₅/XI pins should not be used as general I/Os, but as XO and XI pins for connecting crystal oscillator.

Resetting of the D₁₅ latch by RED instruction generates internal halt state. 16Hz overflow signals are output from the prescaler if a crystal oscillator of 32.768kHz is connected to the D₁₄/XO and D₁₅/XI pins. When an overflow signal is issued, the D₁₅ latch is set to "1" from "0", the LCD-IV returns from halt state, adds 1 to the timer register, and execution restarts from the instruction next to the RED instruction.

Note that external halt caused by the \overline{HLT} pin cannot be released by prescaler overflow signals.

(Caution at the halt)

When the LCD-IV goes into halt state, segment pins (SEG₁ to SEG₃₂) and common pins (COM₁ to COM₄) become the same potential and display goes out. However, in order to reduce power consumption during halt, disconnect the voltage applied to liquid crystal power supply V₃. Since there are dividing resistors among V₁, V₂, and V₃, current of up to 50μA flows if voltage is applied between V_{CC} and V₃ in the same way as normal operation.

Overflow signals of the prescaler return the LCD-IV from internal halt.

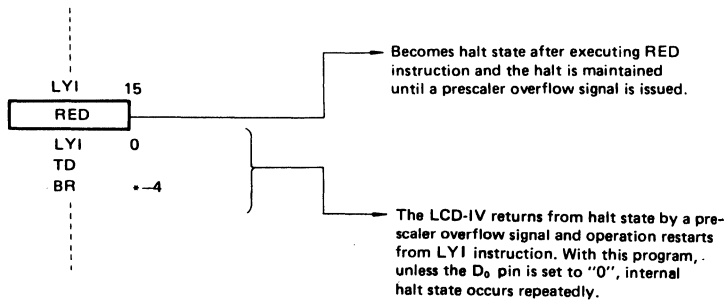


Figure 33 Program example in the Internal Halt Mode

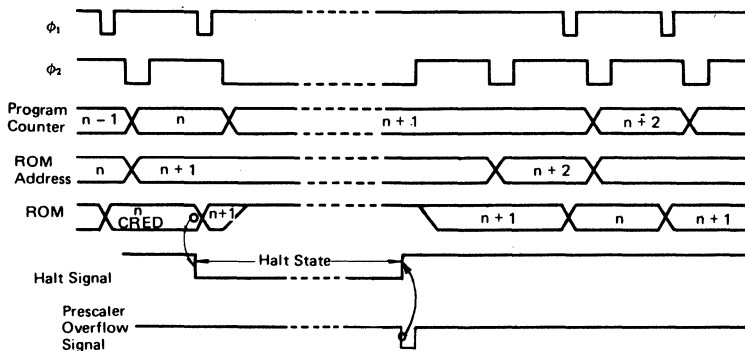
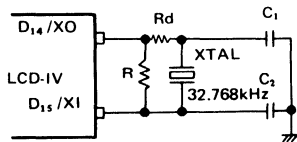


Figure 34 Internal Halt Timing Chart

■ CRYSTAL OSCILLATION CIRCUIT FOR TIMER

The user can specify whether or not the timer crystal should be externally attached by the "MASK OPTION LIST". By externally attaching a crystal oscillator of 32.768kHz to the

D₁₄/XO and D₁₅/XI pins, user can set the prescaler clock to 1,024Hz and timer interrupt cycle to max. of 1 sec.



(NOTE)
The crystal oscillator, resistor R, Rd and load capacitor C₁ and C₂ should be placed as close as possible to the LCD-IV. Induction of external noise to D₁₄/XO and D₁₅/XI may disturb normal oscillation.
This circuit is the example of the typical use. As the oscillation characteristics is not guaranteed, please consider and examine the circuit constants carefully on your application.

Figure 35 Crystal Oscillator Circuit

No.	Halt state	With or without timer crystal	D ₁₄ , D ₁₅ (XO, XI)	Function
1	External halt	Externally attached crystal (32.768 kHz)	Pins for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. Up to 1 second can be set as the timer interruption cycle.
2	External halt	(Without crystal) Internal clock of LSI	Used as general I/O	The prescaler clock becomes a typ. of 100kHz, and the timer interruption cycle can be set to maximum of 97.66Hz.
3	Internal and external halt	Externally attached crystal (32.768 kHz)	Pins for attaching crystal. Cannot be used as general I/O.	Prescaler clock is set to 1,024 Hz and the overflow signal to 16 Hz. This signal performs the LCD-IV return from internal halt. (Return from external halt is not possible by the prescaler overflow signal.)

LCD—IV (HD613901)

■ MASK OPTION

The following type mask option is available.

● I/O Pin Format Select one of A, B or C.

- A: Without pull-up MOS
- B: With pull-up MOS
- C: CMOS output

(Note) External input is not permitted if CMOS output is selected in the case of I/O common pins.

● I/O Status in the Halt State Select Enable or Disable.

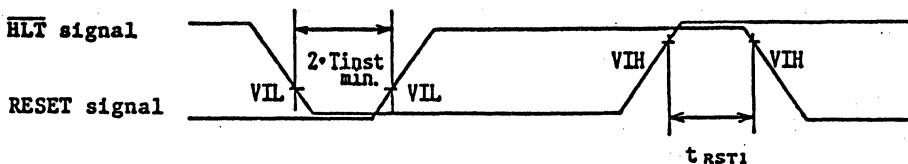
- Enable
 - Output Maintained in the status before halt.
 - Pull-up MOS . . . ON
 - Input . . . Unrelated to halt state

(Since Pull-up MOS is ON, if halt occurs when output is "0" (Low) level (NMOS; ON), pull-up MOS current always flows. If input changes, transient current flows through the input circuit. Also, current flows through the input pull-up MOS. These currents are added to standby power supply current (or halt current).)
- Disable
 - Output . . . NMOS output; OFF
CMOS output; High impedance
(NMOS, PMOS; OFF)
 - Pull-up MOS . . . OFF
 - Input . . . Input circuit; OFF

(Both input and output become high impedance state. Since the input circuit is turned off, input change does not lead to flow other than the standby power supply current or halt current.)

■ PRECAUTION WHEN USING HALT FUNCTION

- Please set the LCD-IV halt state before resetting it in timing shown below, when resetting the LCD-IV under condition below:
Liquid crystal display duty: Static or 1/2 duty,
Display RAM file (Register R₅₁, R₅₀): (0,0) or (0,1) or (1,0).



(Note) • t_{RST1}: RESET pulse width (1)
• T_{inst}: Instruction cycle time

2. REASON

RAM data is destroyed at resetting according to the setting way of liquid crystal display duty or display RAM file (refer to the table below).

Liquid crystal display mode	RAM data destroyed	RAM data retained
Liquid crystal display duty	Static or 1/2 duty (Registers R41, R40 =0, 0 or 0, 1)	1/3 or 1/4 duty (Registers R41, R40 =1, 0 or 1, 1)
Display RAM file	Registers R51, R50 =0, 0 or 0, 1 or 1, 0)	Registers R51, R50 =1, 1



■ INSTRUCTION

Instructions are listed according to their functions.
Each mnemonic code and function is shown in this table.

Group	Mnemonic code	Function	Status
Register to Register	LAB	$B \rightarrow A$	
	LBA	$A \rightarrow B$	
	LAY	$Y \rightarrow A$	
	LASPX	$SPX \rightarrow A$	
	LASPY	$SPY \rightarrow A$	
	XAMR m	$A \leftrightarrow MR(m)$	
RAM Address	LXA	$A \rightarrow X$	
	LYA	$A \rightarrow Y$	
	LXI i	$i \rightarrow X$	
	LYI i	$i \rightarrow Y$	
	IY	$Y+1 \rightarrow Y$	NZ
	DY	$Y-1 \rightarrow Y$	NB
	AYY	$Y+A \rightarrow Y$	C
	SYY	$Y-A \rightarrow Y$	NB
	XSPX	$X \leftrightarrow SPX$	
	XSPY	$Y \leftrightarrow SPY$	
	XSPXY	$X \leftrightarrow SPX, Y \leftrightarrow SPY$	
	Register RAM	LAM(XY)	$M \rightarrow A (XY \leftrightarrow SPXY)$
LBM(XY)		$M \rightarrow B (XY \leftrightarrow SPXY)$	
XMA(XY)		$M \leftrightarrow A (XY \leftrightarrow SPXY)$	
XMB(XY)		$M \leftrightarrow B (XY \leftrightarrow SPXY)$	
LMAIY(X)		$A \rightarrow M, Y+1 \rightarrow Y (X \leftrightarrow SPX)$	NZ
LMADY(X)	$A \rightarrow M, Y-1 \rightarrow Y (X \leftrightarrow SPX)$	NB	
Immediate	LMIIY i	$i \rightarrow M, Y+1 \rightarrow Y$	NZ
	LAI i	$i \rightarrow A$	
	LBI i	$i \rightarrow B$	
Arithmetic	AI i	$A+i \rightarrow A$	C
	IB	$B+1 \rightarrow B$	NZ
	DB	$B-1 \rightarrow B$	NB
	AMC	$M+A+C(F/F) \rightarrow A$	C
	SMC	$M-A-\bar{C}(F/F) \rightarrow A$	NB
	AM	$M+A \rightarrow A$	C
	DAA	Decimal Adjustment (Addition)	
	DAS	Decimal Adjustment (Subtraction)	
	NEGA	$\bar{A}+1 \rightarrow A$	
	COMB	$\bar{B} \rightarrow B$	
	SEC	$1 \rightarrow C (F/F)$	
	REC	$0 \rightarrow C (F/F)$	
	TC	Test C (F/F)	C (F/F)
	ROTL	Rotation Left	
	ROTR	Rotation Right	
OR	$A \cup B \rightarrow A$		

(to be continued)

LCD—IV (HD613901)

Group	Mnemonic code	Function	Status
Compare	MNEI i	$M \neq i$	NZ
	YNEI i	$Y \neq i$	NZ
	ANEM	$A \neq M$	NZ
	BNEM	$B \neq M$	NZ
	ALEI i	$A \leq i$	NB
	ALEM	$A \leq M$	NB
	BLEM	$B \leq M$	NB
RAM bit Manipulation	SEM n	$1 \rightarrow M(n)$	
	REM n	$0 \rightarrow M(n)$	
	TM n	Test M(n)	M(n)
ROM Address	BR a	Branch on Status 1	1
	CAL a	Subroutine Jump on Status 1	1
	LPU u	Load Program Counter Upper on Status 1	
	TBR p	Table Branch	
	RTN	Return from Subroutine	
Interrupt	SEIE	$1 \rightarrow I/E$	
	SEIF0	$1 \rightarrow IF0$	
	SEIF1	$1 \rightarrow IF1$	
	SETF	$1 \rightarrow TF$	
	SECF	$1 \rightarrow CF$	
	REIE	$0 \rightarrow I/E$	
	REIF0	$0 \rightarrow IF0$	
	REIF1	$0 \rightarrow IF1$	
	RETF	$0 \rightarrow TF$	
	RECF	$0 \rightarrow CF$	
	TIO	Test INT ₀	INT ₀
	TI1	Test INT ₁	INT ₁
	TIF0	Test IF0	IF ₀
	TIF1	Test IF1	IF ₁
	TTF	Test TF	TF
	LTI	i → Timer/Counter	
	LTA	A → Timer/Counter	
LAT	Timer/Counter → A		
RTNI	Return Interrupt		
Input/Output (Display Control)	SED	$1 \rightarrow D(Y)$	
	RED	$0 \rightarrow D(Y)$	
	TD	Test D(Y)	D(Y)
	SEDD n	$1 \rightarrow D(n)$	
	REDD n	$0 \rightarrow D(n)$	
	LAR p	R(p) → A	
	LBR p	R(p) → B	
	LRA p	A → R(p)	
	LRB p	B → R(p)	
	Pp	Pattern Generation	
	NOP	No Operation	

(NOTE) 1. (XY) after a mnemonic code has four meanings as follows.

Mnemonic only	Instruction execution only
Mnemonic with X	Instruction execution, X ↔ SPX
Mnemonic with Y	Instruction execution, Y ↔ SPY
Mnemonic with XY	Instruction execution, X ↔ SPX, Y ↔ SPY
[Example] LAM	M → A
LAMX	M → A, X ↔ SPX
LAMY	M → A, Y ↔ SPY
LAMXY	M → A, X ↔ SPX, Y ↔ SPY



HITACHI

2. Status column shows the factor which affects status by the instruction of status change.
 - NZ ALU Not Zero
 - C ALU Overflow in Addition/Carry
 - NB ALU Overflow in Subtraction/No Borrow
 except above Content of status column affects status directly.
3. Carry flip-flop is not always affected by executing the instruction which affects the Status. Instructions which affect Carry flip-flop are eight as follows.
 - AMC SEC
 - SMC REC
 - DAA ROTL
 - DAS ROTR
4. All instructions except for P are executed in single cycle. P is executed in 2 cycles.

The Difference between LCD-III and LCD-IV

No.	Item	LCD-III	LCD-IV
1	ROM	(Program Memory) 2,048 words (Pattern Memory) 128 words	(Program Memory) 4,096 words (Includes Pattern Memory)
2	RAM	160 digits	256 digits
3	Cycle Time (V _{CC} = 5V±10%)	10μs/cycle (f _{CP} = 400 kHz)	5μs/cycle (f _{CP} = 800 kHz)
4	Stored Reset Circuit (Power-on Reset)	Yes	No
5	Select Option	Selected by Mask Option List (Note) But when program evaluation with HD44797E, set up the option with the register as LCD-IV.	When ordering ROM, selected by Mask Option List or by program using internal register R6. (Mask Option List + Program)
	Crystal for Timer		R ₆₁ = 0 (No crystal for timer) R ₆₁ = 1 (With crystal for timer)
	Internal Halt		R ₆₂ = 0 (With internal halt) R ₆₂ = 1 (No internal halt)
	I/O Condition at "Halt" state		R ₆₃ = 0 (Enable) R ₆₃ = 1 (Disable)
6	Oscillator	Refer to the manual as for circuit constant of resistor oscillation and ceramic oscillation.	Circuit constants of resistor oscillation and ceramic oscillation are undecided. (As for low voltage operation board (V _{CC} = 2.5 to 5.5V), undecided that ceramic filter can be used or not.)
7	Reset Address	31—3F	63—3F (Bank 1)
8	Bank Register (ROM Addressing)	No Bank Register	ROM is divided in 2 Banks.
9	Absolute Maximum Rating V _{T2} for Pin Voltage of Open Drain Configuration Output Pins and I/O Common Pins	-0.3 to +10.0V	-0.3 to V _{CC} + 0.3V (same as V _T)

(to be continued)



LCD—IV (HD613901)

No.	Item	LCD-III	LCD-IV												
10	Input "High" level Voltage V_{IH} of Open Drain Configuration Output Pins and I/O Common Pins.	<table border="1"> <thead> <tr> <th>min</th> <th>typ</th> <th>max</th> </tr> </thead> <tbody> <tr> <td>$V_{CC}-1.0$</td> <td>—</td> <td>10</td> </tr> </tbody> </table>	min	typ	max	$V_{CC}-1.0$	—	10	<table border="1"> <thead> <tr> <th>min</th> <th>typ</th> <th>max</th> </tr> </thead> <tbody> <tr> <td>$V_{CC}-1.0$</td> <td>—</td> <td>$V_{CC}+0.3$</td> </tr> </tbody> </table>	min	typ	max	$V_{CC}-1.0$	—	$V_{CC}+0.3$
min	typ	max													
$V_{CC}-1.0$	—	10													
min	typ	max													
$V_{CC}-1.0$	—	$V_{CC}+0.3$													
11	RAM Contents Destruction at Reset	With RAM destruction	No RAM destruction												
12	Maximum Total Output Current (1) $-\Sigma I_{O1}$	45 mA	25 mA												
13	Maximum Total Output Current(2) ΣI_{O2}	45 mA	25 mA												
14	Supply Current(1) I_{CC1} ($V_{CC} = 5V$)	1.3 mA max ($f_{OSC} = 400kHz$)	<table border="1"> <tbody> <tr> <td>3 mA max ($f_{OSC} = 800kHz$)</td> </tr> <tr> <td>1.5 mA max ($f_{OSC} = 400kHz$)</td> </tr> </tbody> </table>	3 mA max ($f_{OSC} = 800kHz$)	1.5 mA max ($f_{OSC} = 400kHz$)										
3 mA max ($f_{OSC} = 800kHz$)															
1.5 mA max ($f_{OSC} = 400kHz$)															
15	Supply Current(2) I_{CC2} ($V_{CC} = 5V$)	0.6 mA max ($f_{OSC} = 400kHz$)	<table border="1"> <tbody> <tr> <td>2 mA max ($f_{OSC} = 800kHz$)</td> </tr> <tr> <td>1 mA max ($f_{OSC} = 400kHz$)</td> </tr> </tbody> </table>	2 mA max ($f_{OSC} = 800kHz$)	1 mA max ($f_{OSC} = 400kHz$)										
2 mA max ($f_{OSC} = 800kHz$)															
1 mA max ($f_{OSC} = 400kHz$)															
16	Supply Current(2) Current(2) I_{CCS2}	40 μA max	120 μA max												
17	Pull up MOS Current $-I_P$	$V_{CC} = 3V, 15 \leq -I_P \leq 80 \mu A$	$V_{CC} = 3V, 10 \leq -I_P \leq 100 \mu A$												
18	Supply Current I_{CC} $V_{CC} = 3V, f_{OSC} = 200kHz, R_f$ Oscillation, External clock	0.15 mA	0.3 mA max												
19	Standby Supply Current(2) I_{CCS2}	$V_{CC} = 2.7$ to $3.3V; 21 \mu A$ max	$V_{CC} = 3.0V; 21 \mu A$												

LCD-IV Mask Option List

- 5V Operation
 3V Operation

☆ Mark "√" in "□" for the selected spec.

Date	
Customer	
Dept.	
Name	
ROM CODE ID	
LSI Type Name (entered by Hitachi)	

(1) I/O Option

Pin Name	I/O	I/O Option			Remarks	Pin Name	I/O	I/O Option			Remarks
		A	B	C				A	B	C	
D0	I/O					R00	I				
D1	I/O					R01	I				
D2	I/O					R02	I				
D3	I/O					R03	I				
D4	I/O					R10	I/O				
D5	I/O					R11	I/O				
D6	I/O					R12	I/O				
D7	I/O					R13	I/O				
D8	I/O					R20	I/O				
D9	I/O					R21	I/O				
D10	I/O					R22	I/O				
D11	I/O					R23	I/O				
D12	I/O					R30	O				
D13	I/O					R31	O				
D14	I/O					R32	O				
D15	I/O					R33	O				
INT0	I										
INT1	I										

* Specify the I/O composition with a mark of "O" in the applicable composition column.

A: No pull up MOS B: With pull up MOS C: CMOS Output

(2) Other Options

I/O State at Halt Mode	<input type="checkbox"/> Enable	<input type="checkbox"/> Disable
External Crystal for Timer (NDK : MX-3BT)	<input type="checkbox"/> Yes [D ₁₄ and D ₁₅ become XO and X1. Do not enter anything in I/O option column of D ₁₄ and D ₁₅ .]	<input type="checkbox"/> No
Internal Halt	<input type="checkbox"/> Yes [When selecting Crystal for Timer and Oscillator except ceramic filter.]	<input type="checkbox"/> No

☆ Mark "√" in "□" for the selected spec.

Check list of Application

[A] Oscillation (for System Clock)

CPG	5V Operation	3V Operation
Resistor	<input type="checkbox"/> R _f = 62kΩ ± 2%	<input type="checkbox"/> R _f = 270kΩ ± 2%
Ceramic Filter	<input type="checkbox"/> 800 kHz : <input type="checkbox"/> 400 kHz	
External Clock	<input type="checkbox"/> t _{cp} = 130K to 1000 kHz	<input type="checkbox"/> t _{cp} = 130K to 300 kHz

☆Mark "√" in "□" for the selected oscillation.

[B] External Halt

External Halt Mode	<input type="checkbox"/> Not used
	<input type="checkbox"/> Used (Recovery with Reset)
	<input type="checkbox"/> Used (Cannot be recovered)

☆ Mark "√" in "□" for the selected spec.

HD404508, HD4074509

Description

The HD404508, HD4074509 is a CMOS 4-bit single-chip HMCS400 series microcomputer providing high program productivity. It is suitable for a digital tuning system by virtue of its PLL frequency synthesizer with 160 MHz prescaler, IF counter, A/D converter, and LCD driver incorporated in addition to ROM, RAM, I/O, timer, and serial interface. The HD4074509 is a ZTAT microcomputer incorporating PROM. It can dramatically shorten system development period and provide a smooth transition debugging to mass production.

Features

- 4-bit CPU (HMCS400)
- 8192 words × 10 bits ROM (HD404508)
- 16384 words × 10 bits programmable ROM (HD4074509) (Program specification is compatible with 27256 type.)
- 512 digits × 4 bits RAM
- I/O ports
 - I/O ports: 29
 - Input ports: 2
 - Output ports: 16 (multiplexed with the LCD segment pins)
- PLL with prescaler (max. 160 MHz)
 - 12 programmable reference frequency
 - 2-modulus prescaler (1/32, 1/33)
 - Phase comparator
 - PLL lock detection circuit
- LCD driver
 - Display duty: static, 1/2, 1/3
 - Segment signal output pins: 28 (including 16 multiplexed pins with R ports)
 - Common signal output pins: 3
- IF counter
 - Gate time: 1 ms, 4 ms, 8 ms, ∞ ms
 - Maximum input frequency: 15 MHz
- Two clock synchronous SCIs
- A/D converter (8 bits × 2 channels)
- Three timer/counters
 - 8-bit timer (multiplexed with reload, event, PWM)
 - 8-bit timer (multiplexed with reload, event)
 - 20-bit timer (free-running, 125 ms interrupt)
- Instruction cycle time: 1.8 μs

- Subroutine stack: 16 levels including interrupts
- Five external and six internal interrupts
- Package: 80-pin flat plastic package (FP-80B)

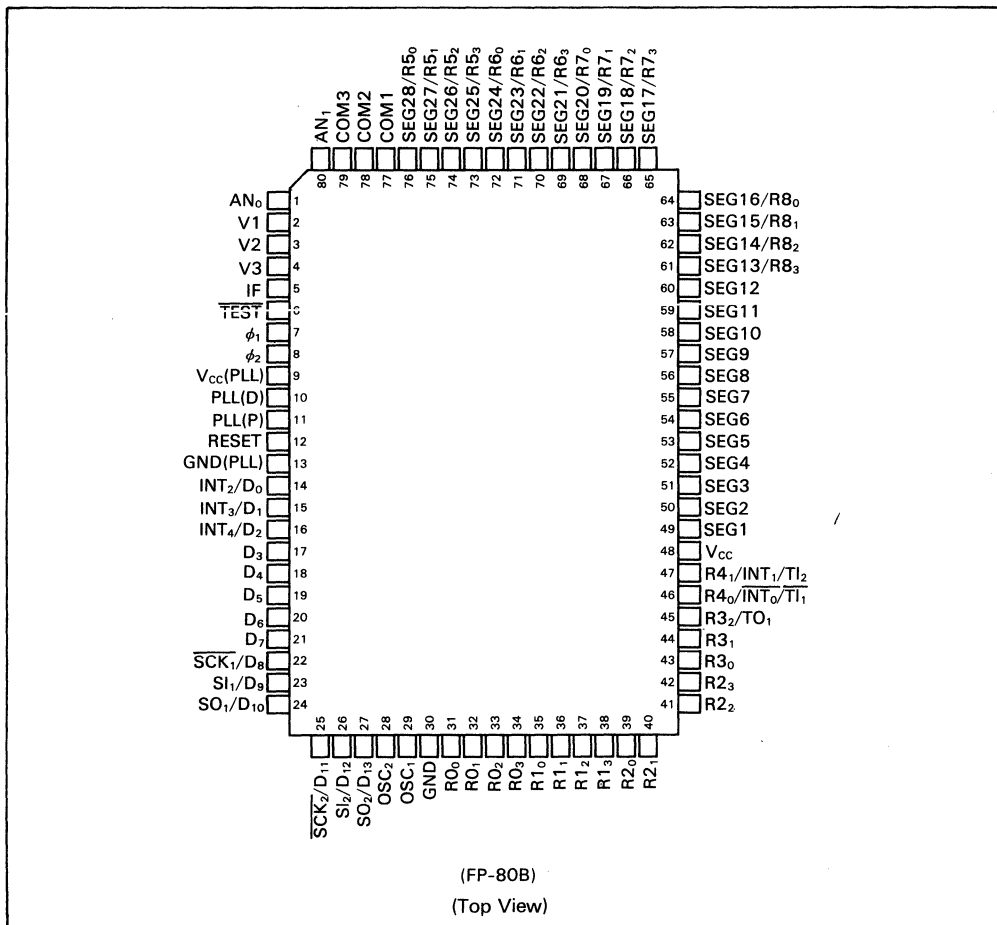
Program Development Support Tools

- Cross assembler and simulator software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PC
- Programming socket adapter for programming the EPROM-on-chip device

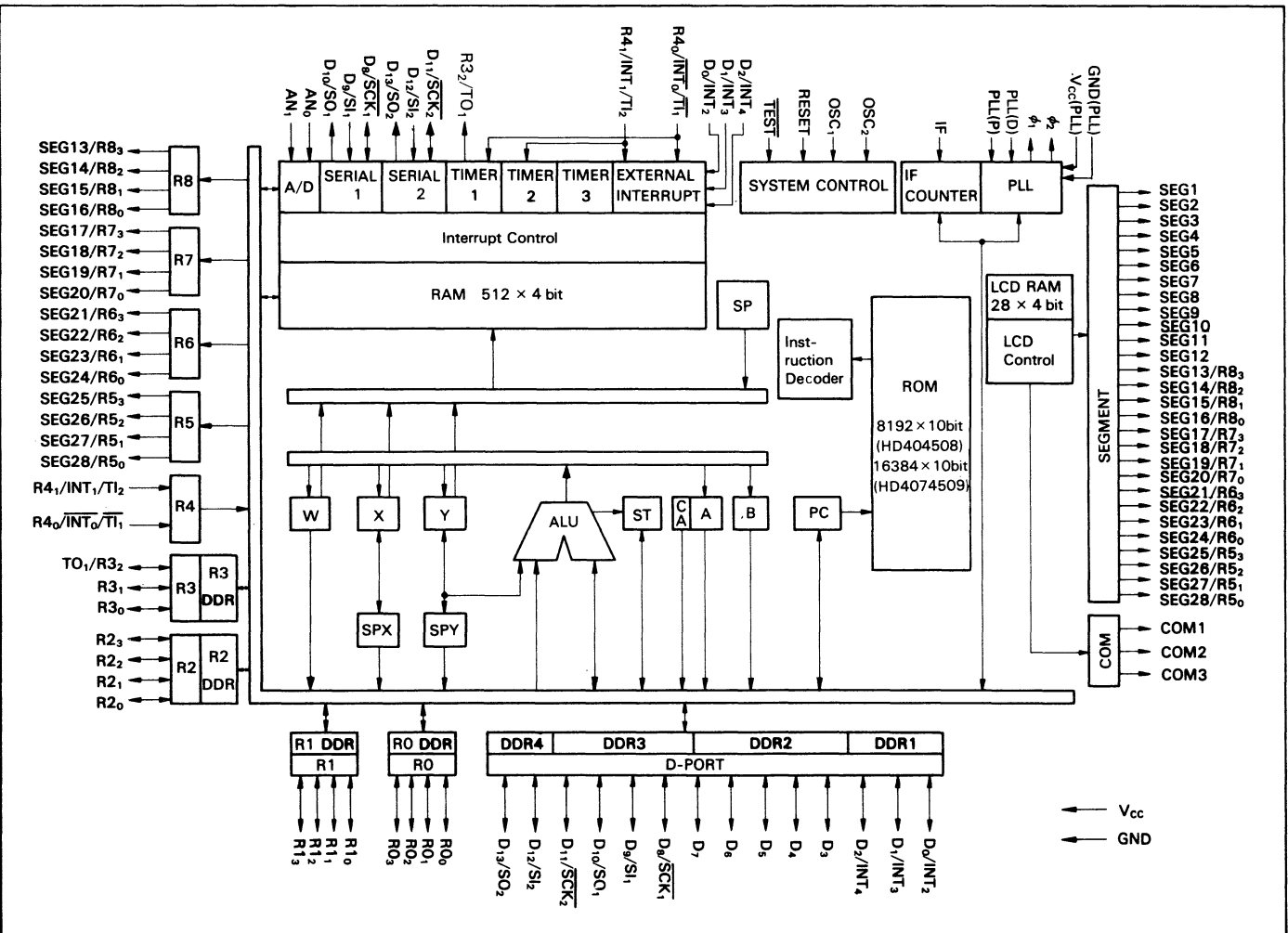
Ordering Information

Part No.	ROM (Words)	Package
HD404508FS	8192 (Mask ROM)	FP-80B
HD4074509FS	16384 (PROM)	

Pin Arrangement



Block Diagram



HD404508, HD4074509



Pin Function

Power supply

V_{CC}: Power supply voltage (+5 V) is applied to V_{CC}.

GND: Connected to the ground (0 V).

V_{CC}(PLL): Connected to power supply for PLL (+5 V).

GND(PLL): Connected to the ground for PLL (0V).

Test

TEST: Input for a factory test mode. Connected to the V_{CC} for normal operation.

Reset

RESET: RESET resets the MCU.

Oscillation

OSC1, OSC2: Input pins for the crystal oscillator circuits. Connected to the 4.5 MHz crystal resonator.

Ports

D port (D₀-D₁₃): The D port is an input/output port accessed on a bit basis. All D₀-D₁₃ are input/output pins. D₀, D₁ and D₂ are multiplexed with INT₂, INT₃ and INT₄, respectively. D₈ to D₁₃ are multiplexed with SCK₁, SI₁, SO₁, SCK₂, SI₂, and SO₂, respectively.

R ports (R0-R8): The R ports are input/output ports accessed in 4-bit units. However, R3 is a 3-bit port and R4 a 2-bit port. R0 to R3 are I/O ports; R5 to R8 output ports; and R4 an input port. The pins R3₂, R5₀-R8₃, R4₀, and R4₁ are multiplexed with TO₁, SEG28-SEG13, INT₀/TI₁, and INT₁/TI₂, respectively.

Interrupt

INT₀, INT₁, INT₂, INT₃, INT₄: External interrupts for the MCU. These five pins are multiplexed with R4₀/TI₁, R4₁/TI₂, D₀, D₁ and D₂, respectively.

Serial communication interface

SCK₁, SI₁, SO₁, SCK₂, SI₂, SO₂: These are transmit clock input/output pins (SCK₁, SCK₂), serial data input pins (SI₁, SI₂), and serial data output pins (SO₁, SO₂) used for serial interface. SCK₁, SCK₂, SI₁, SI₂, SO₁, and SO₂ are

multiplexed with D₈, D₁₁, D₉, D₁₂, D₁₀, and D₁₃, respectively.

Timer

TI₁, TI₂, TO₁: These are external clock input pins (TI₁, TI₂) and timer output pin (TO₁) used for the timer. TI₁, TI₂, and TO₁ are multiplexed with R4₀/INT₀, R4₁/INT₁, and R3₂, respectively.

Liquid crystal display

COM1, COM2, COM3, SEG1-SEG28: These are the common signal output pins (COM1-COM3) and segment signal output pins (SEG1-SEG28) used for the LCD driver. The sixteen pins from SEG13 to SEG28 are multiplexed with R8₃-R8₀, R7₃-R7₀, R6₃-R6₀, and R5₃-R5₀, respectively.

V1, V2, V3: Power supply pins for the LCD.

PLL

PLL (P): An input pin for 160 MHz max. of local oscillation output (VCO output). This pin becomes active when pulse swallow mode is selected during PLL enable. Since an alternating current amplifier is incorporated, local oscillation output should be latched after being filtered through a capacitor.

PLL (D): An input pin for 20 MHz max. of local oscillation output (VCO output). This pin becomes active when direct dividing mode is selected during PLL enable. Since an alternating current amplifier is incorporated, local oscillation output should be latched after being filtered through a capacitor.

φ1, φ2: These pins are outputs of a phase comparator used by the PLL function. The same signal is output from φ1 and φ2.

IF counter

IF: An input pin for intermediate frequency measurement. Since an alternating current amplifier is incorporated, local oscillation output must be latched after being filtered through a capacitor.

AD converter

AN₀, AN₁: These pins are the AD converter input pins.

Memory Map

ROM Memory MAP

ROM memory map is shown in figure 1 and is explained below.

Vector address area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instruction to branch to the start addresses of the reset routine and the interrupt service routine. After reset or interrupt routine is serviced, the program is executed from the vector address.

Zero page subroutine area (\$0000 to \$003F): Locations \$0000 through \$003F are

reserved for subroutines. The program branches to the subroutine in \$0000-\$003F by the CAL instruction.

Pattern area (\$0000 to \$0FFF): The ROM data in locations \$0000 through \$0FFF can be referred to by the P instruction.

Program area

**(\$0000 to \$1FFF: HD404508,)
(\$0000 to \$3FFF: HD4074509):**

Locations \$0000 through \$1FFF, \$3FFF can be used for program code.

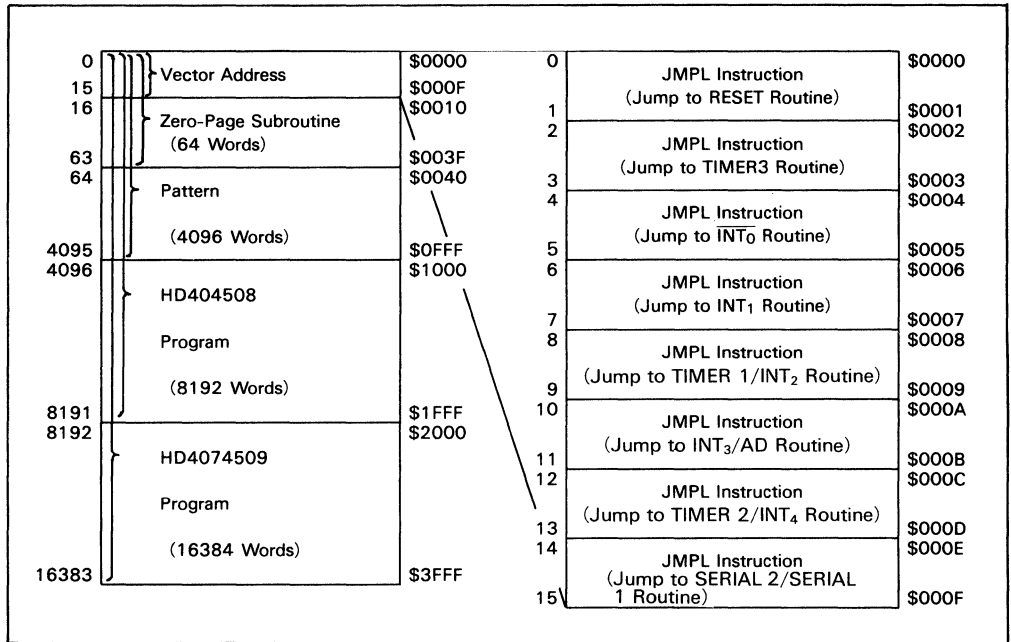


Figure 1. ROM Memory Map

RAM Memory MAP

The MCU contains 512 digits \times 4 bits RAM comprising data area and stack area. In addition to these areas, interrupt control bits, special registers, and display data RAM are mapped to the same RAM memory space. RAM memory map (figure 2) is described in the following paragraphs.

Interrupt control bit area (\$000 to \$003, \$020 to \$023): The interrupt control bit area (figure 3) is used to control interrupt. It can be accessed only by the RAM bit manipulation instruction. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special registers area (\$004 to \$01F, \$024 to \$03F): The special registers are the mode registers for external interrupt, serial interface, and timer, data direction and data registers for I/O ports. As shown in figure 2, these registers can be classified into three

types: write-only, read-only, and read/write registers.

Note that some of these registers cannot be accessed by the RAM bit manipulation instruction.

Data area (\$040 to \$01FF): The memory register (MR), 16 addresses deep (\$040-\$04F), can be accessed by the LAMR and XMRA instructions (figure 4).

Stack area (\$03C0 to \$03FF): The stack area is used for saving the contents of the program counter (PC), status (ST), and carry (CA). This area can be used as a 16-nesting-level subroutine stack in which one level requires 4 digits. The data to be saved and save conditions are shown in figure 4. The program counter is restored by the RTN and RTNI instructions. Status and carry are restored by the RTNI instruction only. Any space not used is available data storage.

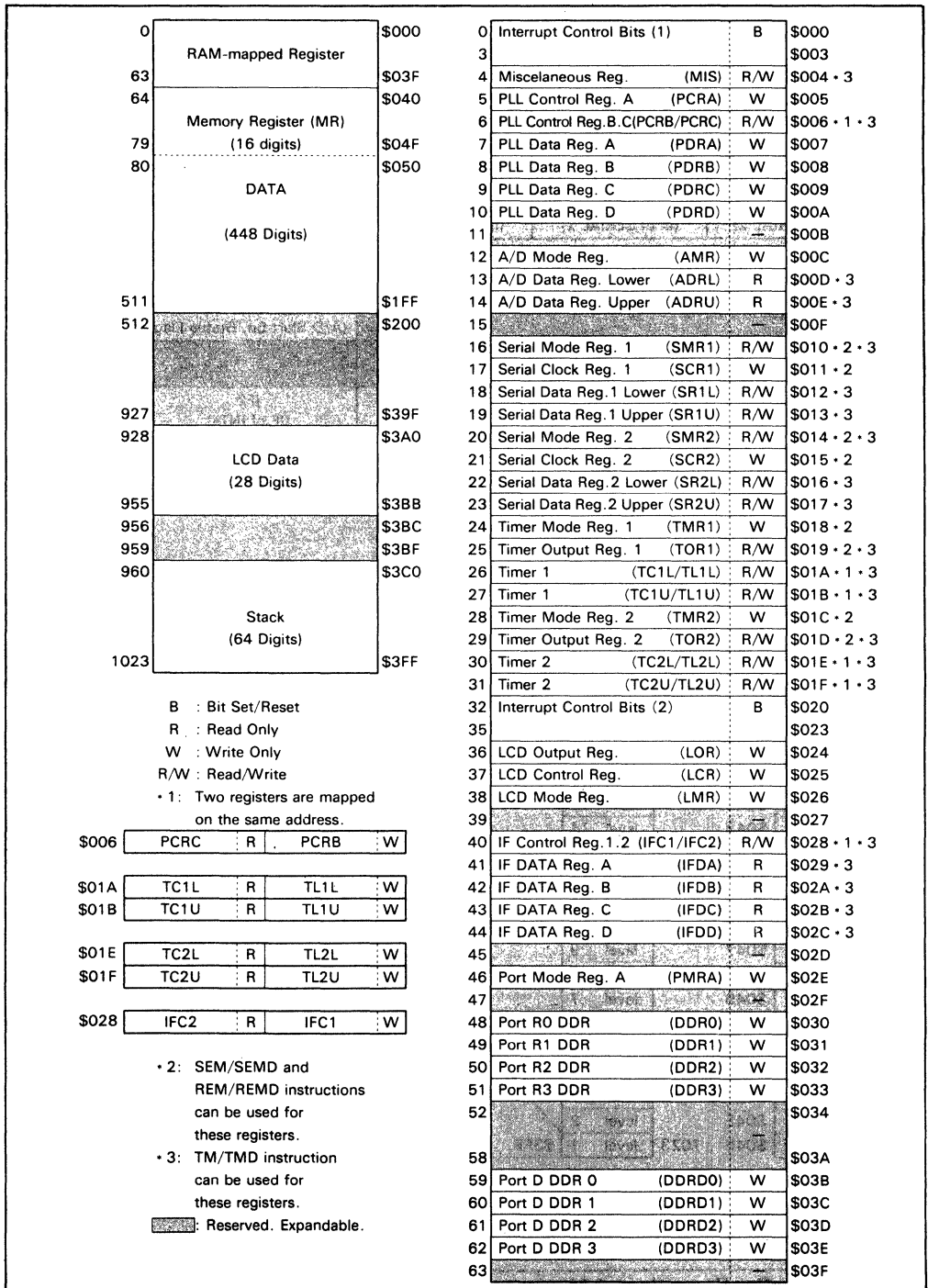


Figure 2. RAM Memory Map



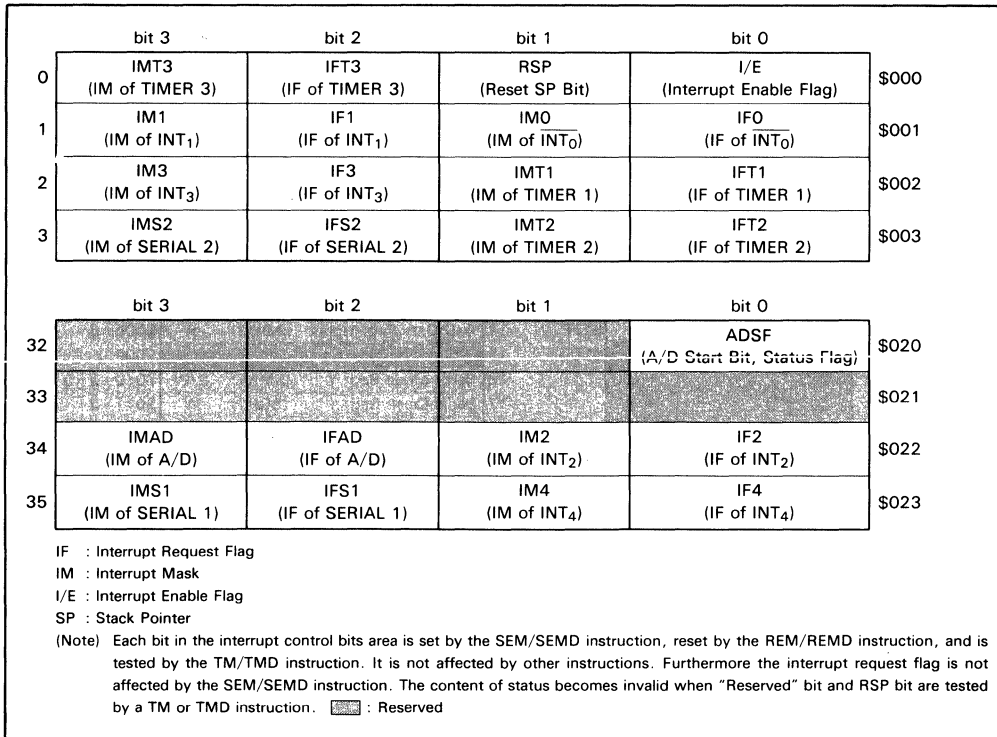


Figure 3. Configuration of Interrupt Control Bit Area (RAM Space)

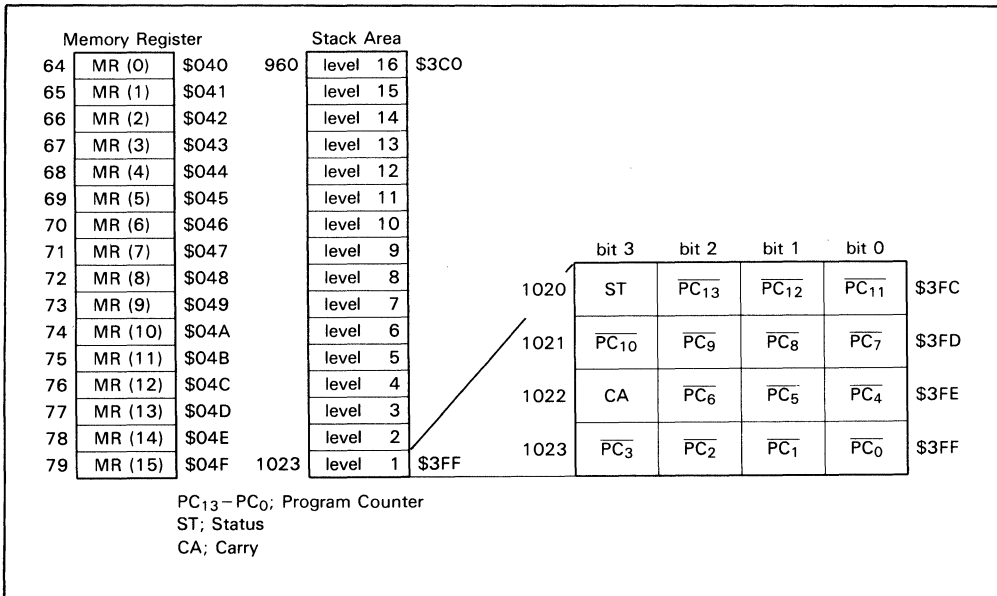


Figure 4. Configuration of Memory Register, Stack Area and Stack Position



Functional Description

Registers and Flags

The MCU has nine registers and two flags for the CPU operations. They are illustrated in figure 5 and described in the following paragraphs.

Accumulator (A), B register (B): The 4-bit register accumulator and B register are used to hold the results from the arithmetic logic unit (ALU), and to transfer data to/from memories, I/O, and other registers.

W register (W), X register (X), Y register (Y): W register is a 2-bit, and X and Y registers are 4-bit registers used for register indirect RAM addressing. Y register is also used for D-port addressing.

SPX register (SPX), SPY register (SPY): The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

Carry (CA): Carry (CA) stores ALU overflow generated by the arithmetic operation. It is affected by the SEC, REC, ROTL, and ROTR instructions. Carry is pushed onto the stack during interrupt servicing, and popped from the stack by the RTNI instruction, but not by the RTN instruction.

Status (ST): Status (ST) latches ALU overflow generated by the arithmetic and compare instructions, Not Zero from ALU, and results of bit tests. It is a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of the status remain unchanged until the next arithmetic, compare, or bit test instruction is executed. ST becomes 1 after the BR, BRL, CAL, or CALL instruction is executed irrespective of whether it is executed or skipped. The contents of the status are pushed onto the stack during interrupt servicing, and popped from the stack by the RTNI instruction, but not by the RTN instruction.

Program counter (PC): The 14-bit program counter is a binary counter which holds a ROM address.

Stack pointer (SP): The 10-bit stack pointer contains the address of the next stack area. SP is initialized to \$3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the upper 4 bits of SP are fixed to 1111, the stack can be used for up to 16 levels. SP is initialized to \$3FF in two ways; MCU reset and RSP bit reset with the REM or REMD instruction.

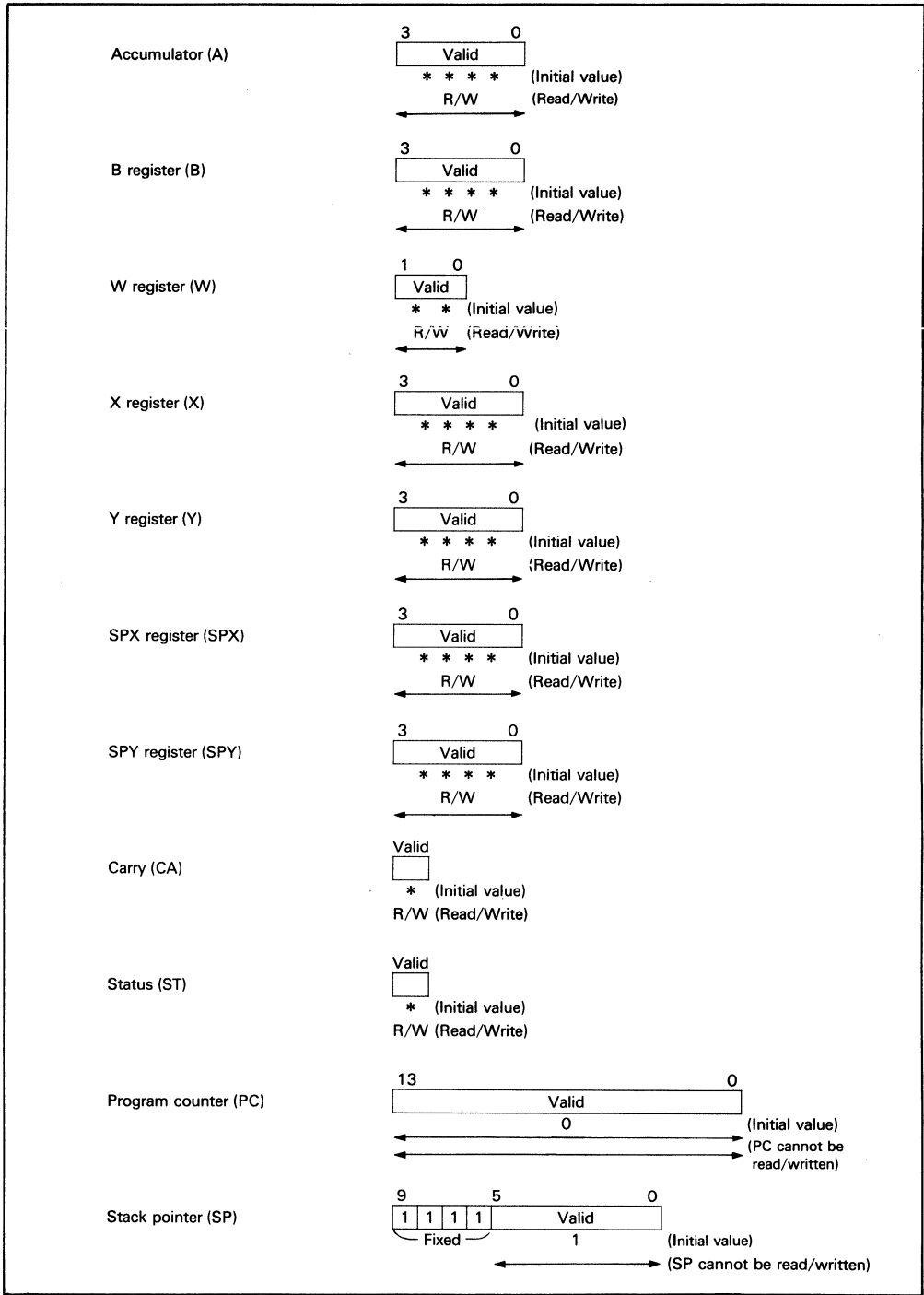


Figure 5. Registers and Flags



Reset**Power-on reset:**

At power-on, the MCU automatically enters reset state for approximately 60 to 65 ms to assure oscillation stabilization time, and then the MCU recovers from that state.

Reset by RESET pin (reset from active mode, standby mode):

The MCU is reset at the rising edge of the reset signal. This signal should be asserted high for at least 3.6 μ s. The MCU is then reset for one instruction cycle time, after which reset is cancelled.

Reset by RESET pin (reset from stop mode):

The MCU is reset at the rising edge of the reset signal. This signal should be asserted high for at least 20 ms. At the beginning of oscillation, the MCU automatically enters reset state for 60 to 65 ms to assure oscillation stabilization time, and then reset is cancelled.

Read function:

The accessible RESET pin is mapped to the bit 0 (\$004, 0) of the miscellaneous register (MLS).

Note that from power-on to the beginning of normal oscillation, the I/O pins are undefined since the I/O data direction registers are not initialized. Values initialized by MCU reset are shown in table 1 and table 2.

HD404508, HD4074509

Table 1. Initial Value by MCU Reset

Items		Initial Value by MCU Reset	Contents
Program Counter (PC)		\$0000	Execute program from the top of ROM address
Status (ST)		1	Enable to branch with conditional branch instruction
Stack Pointer (SP)		\$3FF	Stack level is 0
Interrupt Flag/Mask	Interrupt Enable Flag (I/E)	0	
	Interrupt Request Flag (IF)	0	
	Interrupt Mask (IM)	1	
PLL	PLL Control Register A, B, C (PCRA, PCRB, PCRC)	0000	
A/D	A/D Mode Register (AMR)	0000	
Serial Interface	Serial Mode Register 1, 2 (SMR1, SMR2)	0000	
	Serial Clock Register 1, 2 (SCR1, SCR2)	0000	
Timer/ Counter	Timer Mode Register 1, 2 (TMR1, TMR2)	0000	
	Timer Output Register 1, 2 (TOR1, TOR2)	0000	
	Timer/Event Counter 1, 2 Lower, Upper (TC1L, TC1U, TC2L, TC2U)	0000	
	Timer 3	Note 1	
LCD	LCD Output Register (LOR)	Note 2	
	LCD Control Register (LCR)	0000	
	LCD Mode Register (LMR)	0000	After reset is cancelled, duty must be set by program
IF	IF Control Register 1, 2 (IFC1, IFC2)	0000	
	IF Counter Data Register A, B, C, D (IFDA, IFDB, IFDC, IFDD)	0000	
I/O	Port D Data Register	1	
	Port R0-R3 Data Register	Note 3	
	Port R0-R3 DDR (DDR0, DDR1, DDR2, DDR3)	Note 4	
	Port D DDR (DDR0, DDR1, DDR2, DDR3)	0000	
	Port Mode Register A (PMRA)	0000	

Note 1: Initial value of timer 3 by MCU reset

The initial value of depends on the value of the data retention bit (MIS₃: \$004, 3).



Item	Reset when power-on reset or data retention bit is 0	Reset when data retention bit is 1
Timer 3	All bits become 0 and are initialized	Not initialized

Note 2: Initial value of the LCD output register by MCU reset
 The initial value of the LCD output register depends on the value of the data retention bit (MIS₃: \$004, 3).

Item	Reset when power-on reset or data retention bit is 0	Reset when data retention bit is 1
LCD output register	LCD output register becomes 0000 and SEG/R-port pins become R port	Retained (SEG/R port is not changed)

Note 3: Initial value of the port R0-R3 data register by MCU reset
 The initial value of the port R0-R3 data register depends on the value of the data retention bit (MIS₃: \$004, 3).

Item	Reset when power-on reset or data retention bit is 0	Reset when data retention bit is 1
Port R0-R3 data register	1	Retained

Note 4: Initial value of the R port data direction register by MCU reset
 Initial value of the R port data direction register depends on the value of the data retention bit (MIS₃: \$004, 3).

Item	Reset when power-on reset or data retention bit is 0	Reset when data retention bit is 1
R port data direction register	The R port data direction register becomes 0000 and R port becomes input port	Retained (I/O of the R port is not changed)

Table 2. Values of the Registers except for Table 1 after the Reset

Items	Initial Value by MCU Reset from Active Mode	Initial Value by MCU Reset from Standby Mode	Initial Value by MCU Reset from Oscillation Stop Mode	Initial Value by MCU Reset from Power-on
Carry (CA)	The contents of the items just before MCU reset are not assured. It is necessary to initialize them by software again.			
Accumulator (A)				
B Register (B)				
W Register (W)				
X/SPX Register (X/SPX)				
Y/SPY Register (Y/SPY)				
PLL Data Register (PDRA, PDRB, PDRC, PDRD)				
A/D Data Register Lower, Upper (ADRL, ADRU)				
Serial Data Register 1, 2 Lower, Upper (SR1L, SR1U, SR2L, SR2U)				
RAM	The contents of RAM just before MCU reset are retained		Same as above	
Miscellaneous Register (MIS)	MIS ₃	The contents of MIS ₃ just before MCU reset are retained		0
	MIS ₀	MIS ₀ reads RESET pin level at read operation		

Interrupt

Eleven interrupt sources are available on the MCU: external requests (\overline{INT}_0 , INT_1 , INT_2 , INT_3 , INT_4), timers (TIMER 1, TIMER 2, TIMER 3), A/D converter, and serial interfaces (SERIAL 1, SERIAL 2). For each source, an interrupt request flag (IF) and interrupt mask (IM) are provided to control and maintain the interrupt requests. To control the entire interrupt process, the interrupt enable flag (I/E) is provided.

Since the vector addresses are shared between timer 1 and INT_2 , between A/D and INT_3 , between timer 2 and INT_4 , and between serial 1 and serial 2, determining which request occurs must be done by software.

Interrupt control bits and interrupt processing: The interrupt control bits are mapped to addresses \$000 through \$003, and \$020 through \$023 of RAM space and are accessed by the RAM bit manipulation instruction.

However, interrupt request flag IF cannot be set by software.

The interrupt enable flag (I/E) and interrupt request flag (IF) are set to 0, and the interrupt mask (IM) is initialized to 1 by MCU reset.

An interrupt control circuit block diagram is shown in figure 6. Interrupt priority and vector addresses are shown in table 3, and the interrupt processing conditions for 11 different interrupt types in table 4.

When interrupt request flag is 1 and interrupt mask is 0, an interrupt request is generated. If the interrupt enable flag is 1 at that time, interrupt processing activates. Then a vector address corresponding to the interrupt request is generated from priority PLA.

An interrupt processing sequence and flow-chart are shown in figures 7 and 8 respectively. When an interrupt is received, the current instruction execution finishes at the first cycle, I/E is reset at the second cycle, then the contents of the carry, status, and program counter are pushed onto the stack in the second and third cycles, and the program jumps to the vector address to restart instruction execution in the third cycle. For each vector address area, the JMWL instruction must be programmed to branch the starting address of interrupt routine. The interrupt request flag which causes interrupt

processing must be reset by software in an interrupt routine.

Interrupt enable flag (I/E: \$000, 0): The interrupt enable flag controls enable/disable of all interrupt requests. It is reset by interrupt processing and set by the RTNI instruction. (See table 5.)

External interrupts (\overline{INT}_0 , INT_1 , INT_2 , INT_3 , INT_4): Five external interrupt pins are provided for the MCU. The external interrupt request flag is set at the falling edge of the \overline{INT}_0 input. It is set at the rising edge of the INT_1 , INT_2 , INT_3 , and INT_4 inputs. When using \overline{INT}_0 and INT_1 , interrupt input should be enabled by setting the external interrupt enable bit of the timer output register (TOR1: \$019, TOR2: \$01D). If the interrupt enable bit is reset, the external interrupt request flag is not set and interrupt processing is not performed since input signal itself is masked. (See section "Timer".)

When using INT_2 , INT_3 , and INT_4 , the corresponding bits of port mode register A (PMRA: \$02E) select external interrupt input. If port mode register A is set, the corresponding data direction register bit is reset automatically to input. If port mode register A is reset, external interrupt request flag is not set in spite of external interrupt signal input and interrupt processing is not performed since the external interrupt input signal is masked.

External interrupt request flags (IF0: \$001, 0 IF1: \$001, 2 IF2: \$022, 0 IF3: 002, 2 IF4: \$023, 0): External interrupt request flag IF0 is set at the falling edge of the \overline{INT}_0 input. IF1-IF4 are set at the rising edge of INT_1 - INT_4 . (See table 6.)

External interrupt masks (IM0: \$001, 1 IM1: \$001, 3 IM2: \$022, 1 IM3: \$022, 3 IM4: \$023, 1): The external interrupt request masks mask the interrupt request from the external interrupt request flag. (See table 7.)

Port mode register A (PMRA: \$02E): Port mode register A is a 3-bit write-only register which controls the D_0 / INT_2 , D_1 / INT_3 , and D_2 / INT_4 pins as shown in figure 9.

Port mode register A is initialized to \$0 by MCU reset, so that these pins are all set to D port I/O pins after reset.

Table 3. Vector Addresses and Interrupt Priority

Reset, interrupt	Priority	Vector address
RESET	–	\$0000
TIMER3	1	\$0002
$\overline{\text{INT}}_0$	2	\$0004
INT_1	3	\$0006
TIMER1/ INT_2	4	\$0008
$\text{INT}_3/\text{A/D}$	5	\$000A
TIMER2/ INT_4	6	\$000C
SERIAL2/SERIAL1	7	\$000E

Table 4. Interrupt Servicing Conditions

Interrupt Control Bit	Interrupt Source						
	TIMER3	$\overline{\text{INT}}_0$	INT_1	TIMER1 / INT_2	INT_3 / A/D	TIMER2 / INT_4	SERIAL1 /SERIAL2
I/E	1	1	1	1	1	1	1
$\text{IFT}_3 \cdot \text{IMT}_3$	1	0	0	0	0	0	0
$\text{IFO} \cdot \text{IMO}$	*	1	0	0	0	0	0
$\text{IF}_1 \cdot \text{IM}_1$	*	*	1	0	0	0	0
$\text{IFT}_1 \cdot \text{IMT}_1 + \text{IF}_2 \cdot \text{IM}_2$	*	*	*	1	0	0	0
$\text{IF}_3 \cdot \text{IM}_3 + \text{IFAD} \cdot \text{IMAD}$	*	*	*	*	1	0	0
$\text{IFT}_2 \cdot \text{IMT}_2 + \text{IF}_4 \cdot \text{IM}_4$	*	*	*	*	*	1	0
$\text{IFS}_2 \cdot \text{IMS}_2 + \text{IFS}_1 \cdot \text{IMS}_1$	*	*	*	*	*	*	1

* : Both 0 and 1 do not affect operation

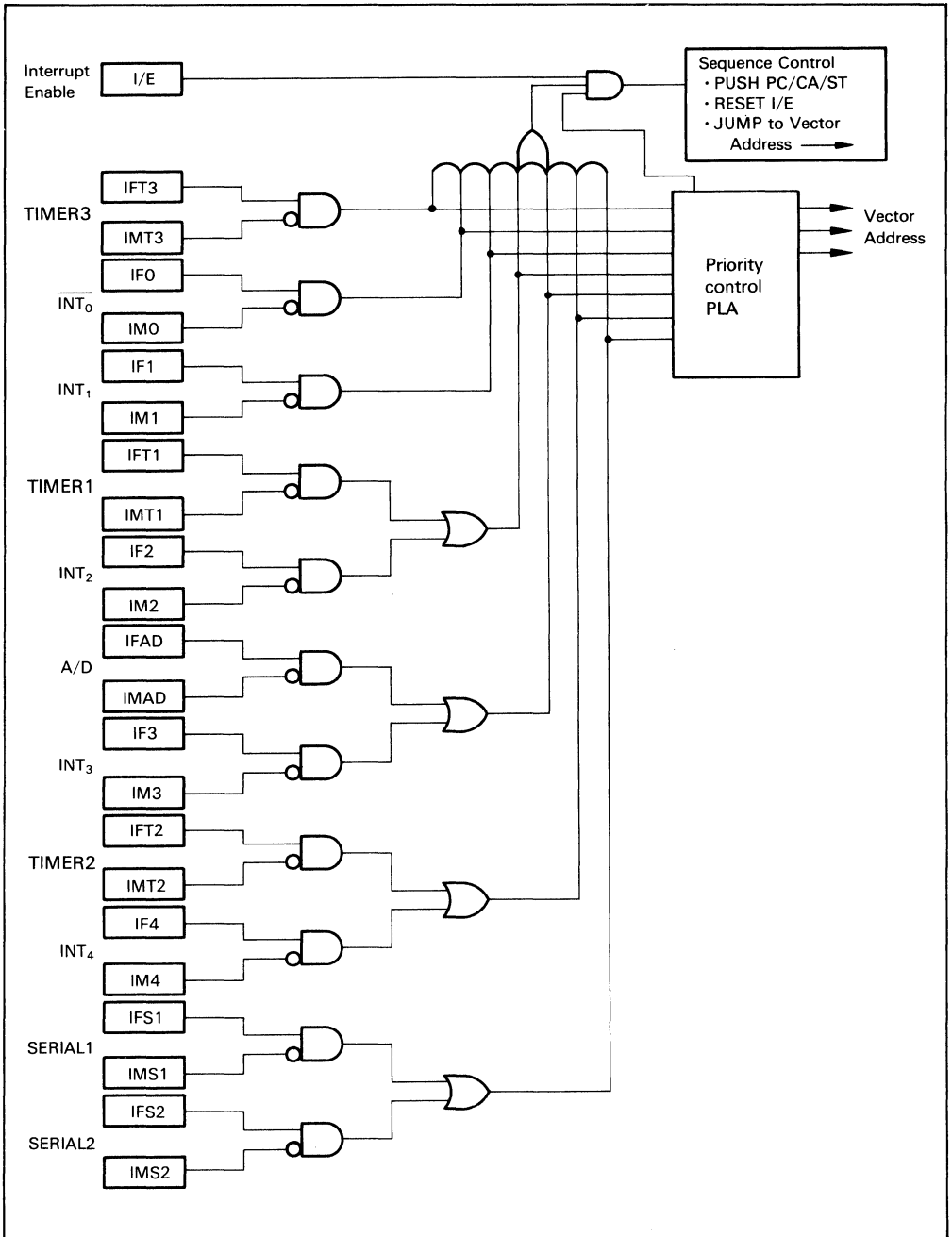


Figure 6. Interrupt Control Circuit Block Diagram

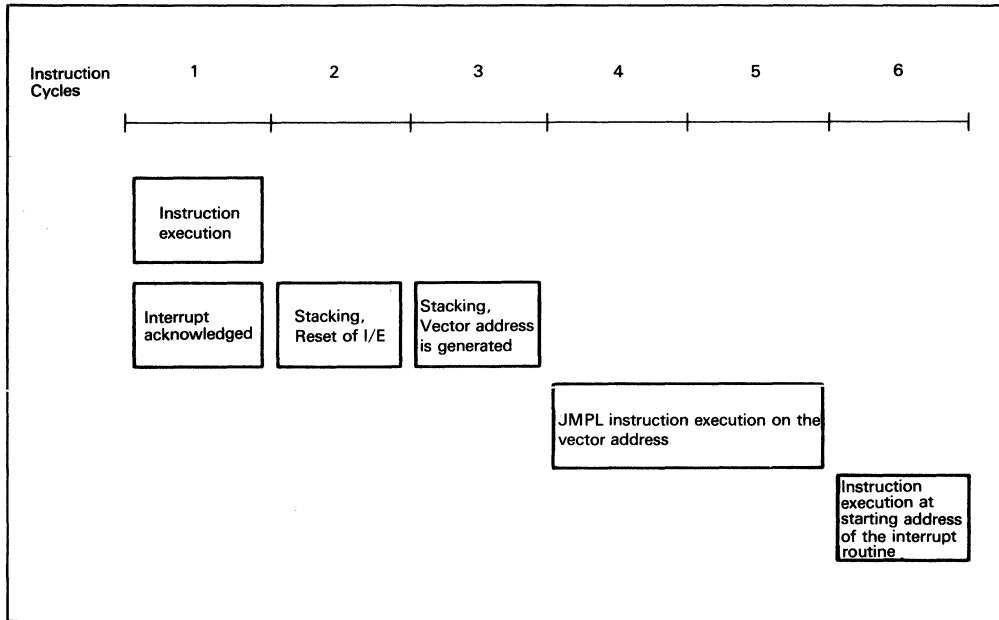


Figure 7. Interrupt Servicing Sequence

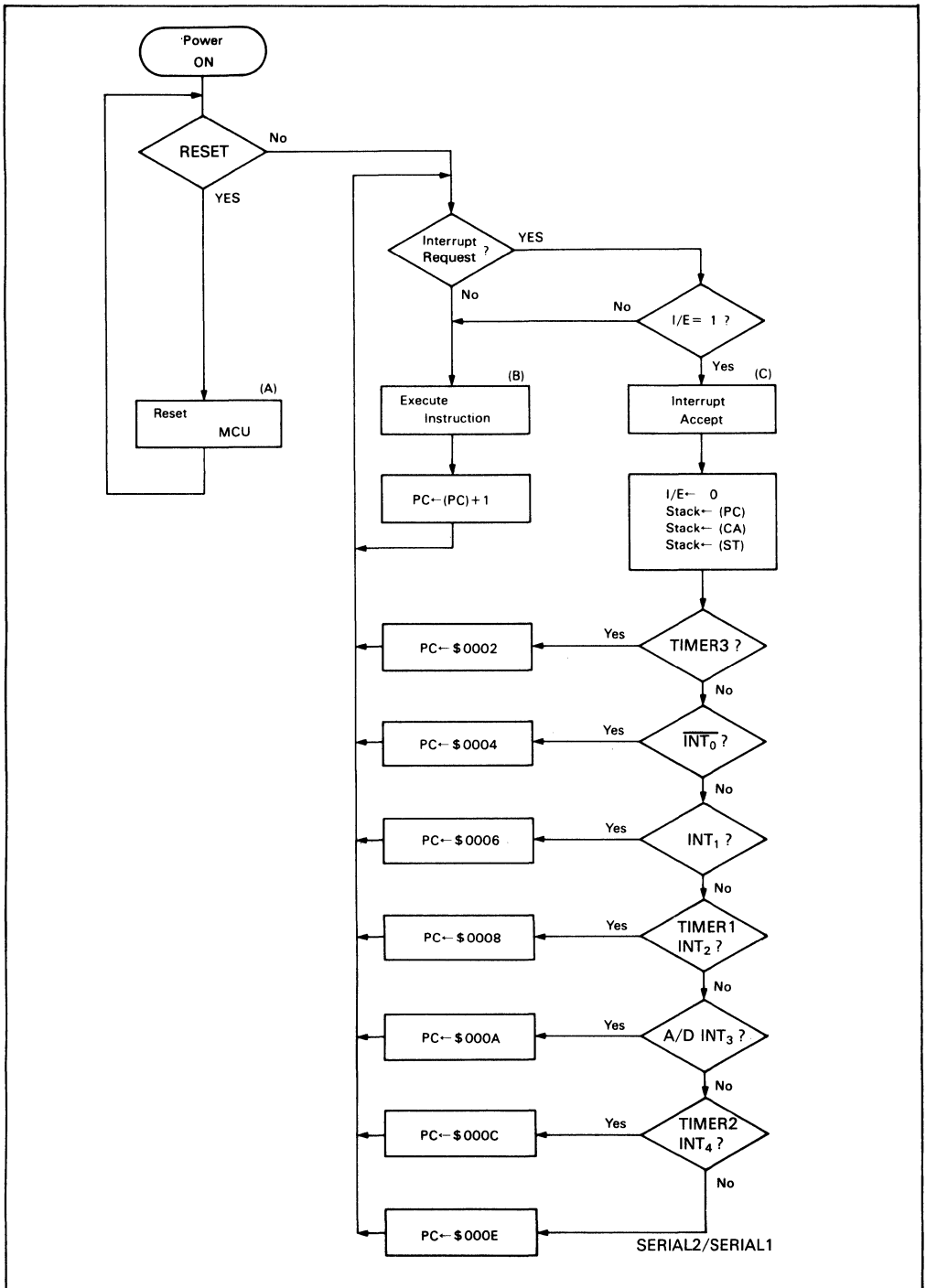


Figure 8. Interrupt Servicing Flowchart



Table 5. Interrupt Enable Flag (\$000,0)

Interrupt Enable Flag (I/E)	Interrupt Enable /Disable
0	Disable
1	Enable

Initial value 0, R/W

Table 6. External Interrupt Request Flag (\$001,0, \$001,2, \$002,2, \$022,0, \$023,0)

External Interrupt Request Flag (IF0, IF1, IF2, IF3, IF4)	Interrupt Requests
0	No
1	Yes

Initial value 0, R/W (cannot be set to 1)

Table 7. External Interrupt Mask (\$001,1, \$001,3, \$002,3, \$022,1, \$023,1)

External Interrupt Mask (IM0, IM1, IM2, IM3, IM4) Interrupt Requests	
0	Enable
1	Disable (masks)

Initial value 1, R/W

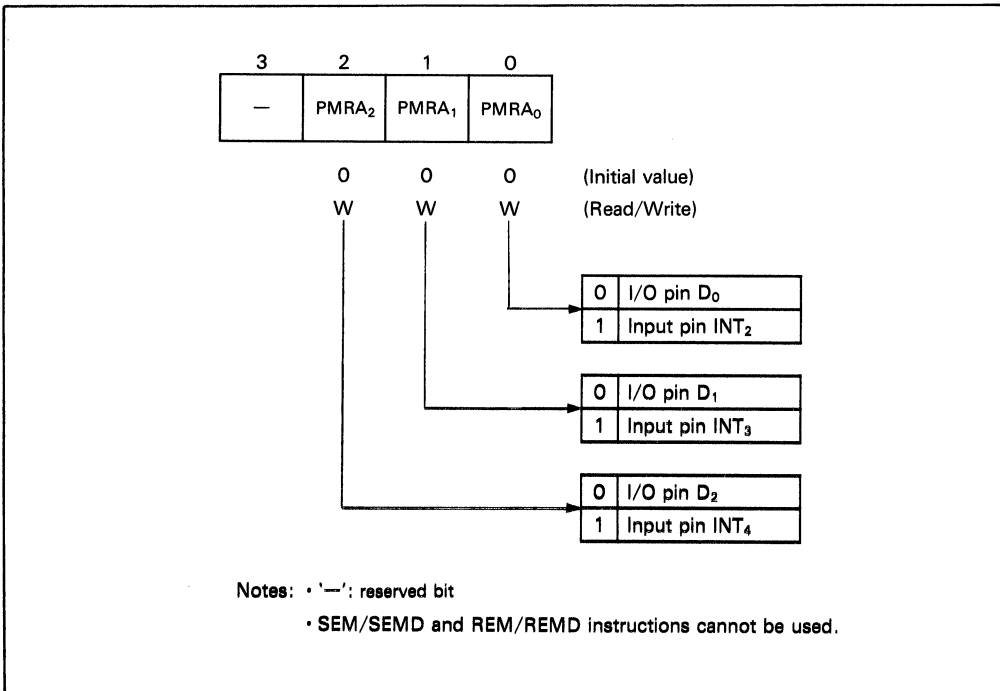


Figure 9. Port Mode Register A (PMRA: \$02E)

Low Power Dissipation Mode

The MCU has two low power dissipation modes, standby mode, stop mode. The function of the low power dissipation mode is

shown in table 8. CPU state transition between low power dissipation modes is shown in figure 10.

Table 8. Low Power Dissipation Mode

Low Power Dissipation Mode	Instruction	Oscillator circuit	Conditions					Input/Output Pin	Timer 1,2,3 Serial Interface 1, 2, A/D, IF counter, LCD, PLL (ϕ PER *3)
			Instruction Execution (ϕ CPU *2)	Interrupt Function (ϕ PER *3)	RAM	Register, Flag	RAM		
Standby Mode	SBY instruction	Active	Stop	Active	Retained	Retained	Retained	Active	
Stop Mode	Stop instruction	Stop	Stop	Stop	Retained	Reset *1	R port: retained D port: high impedance	Stop	

* 1) The MCU recovers from STOP mode by Reset input. Refer to table 1 of section "Reset" for the contents of the flags and registers.

* 2) ϕ CPU: System clock

* 3) ϕ PER: Interrupt, peripheral function clock

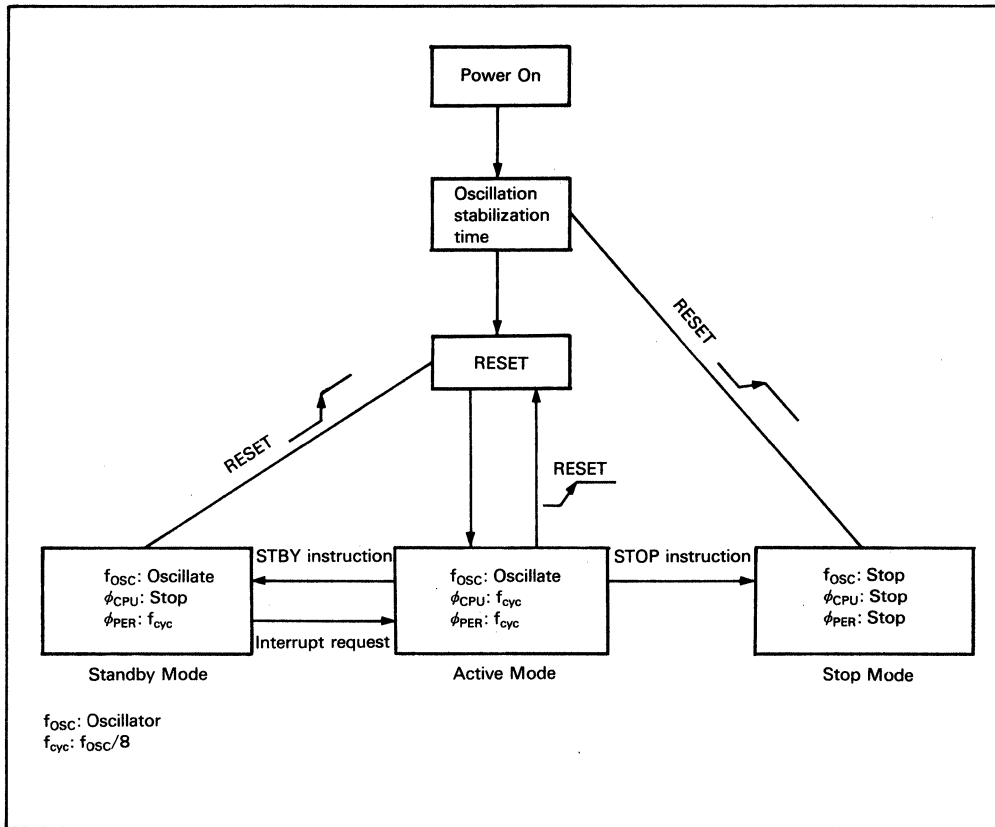


Figure 10. CPU State Transition

Active Mode: In active mode, the MCU operates depending on the clock generated from the OSC1 and OSC2 oscillator circuits.

Standby Mode: The MCU enters standby mode when a SBY instruction is executed. In this mode, an oscillator, interrupt, timer, serial interface, A/D, LCD, PLL, and IF counter continue to operate, but all instruction-related clocks stop.

This in turn stops the CPU, retains all RAM and register contents, and maintains current I/O pin status.

The standby mode is terminated by a RESET or interrupt request. After an interrupt request, the MCU resumes by executing the next instruction following the SBY instruction. Then, if the interrupt enable flag is 1, the interrupt is processed. If the interrupt enable flag is 0, the interrupt request is left pending and normal instruction execution continues.

MCU operating flowchart in standby mode is

shown in figure 11.

Stop Mode: The MCU enters stop mode when a stop instruction is executed. In this mode, the oscillator stops, causing all MCU functions to also stop.

The stop mode is terminated by a RESET input as shown in figure 12. Reset must be High for at least 20 ms to stabilize oscillation. During stop mode, all RAM contents are retained.

When the MCU resumes after stop mode, the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry, and serial data register cannot be guaranteed.

MCU Operation Sequence: The MCU operates according to the flowcharts shown in figures 13 and 14. The RESET is an asynchronous input, which resets the MCU regardless of the MCU state.

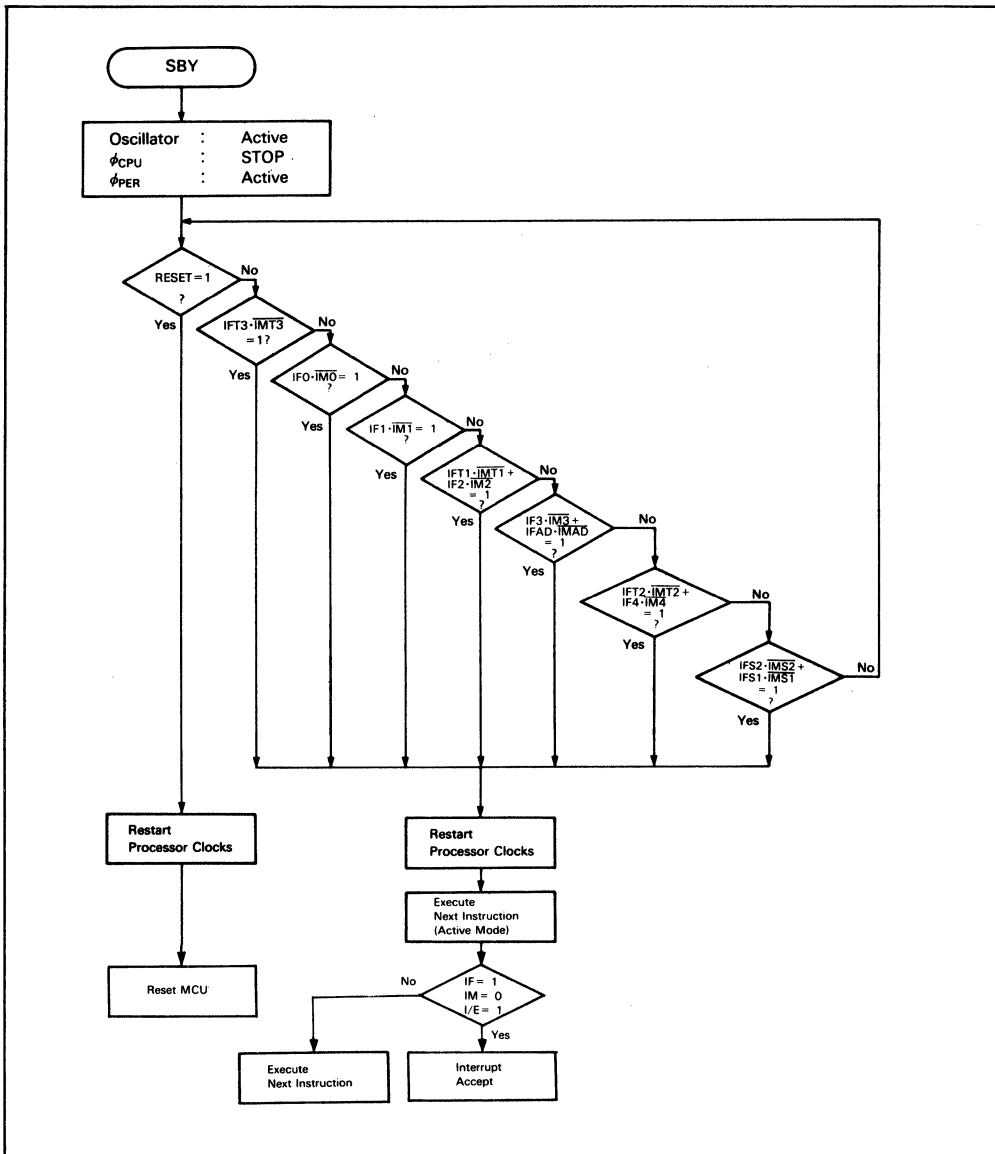


Figure 11. A Standby Mode Flowchart

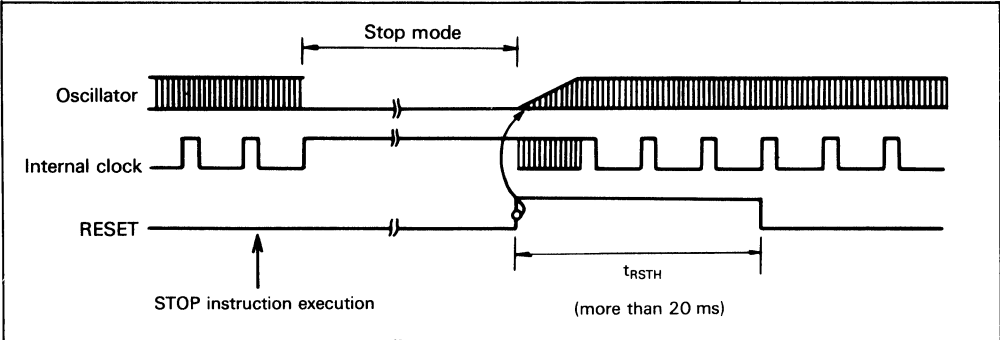


Figure 12. Timing Diagram When Canceling Stop Mode

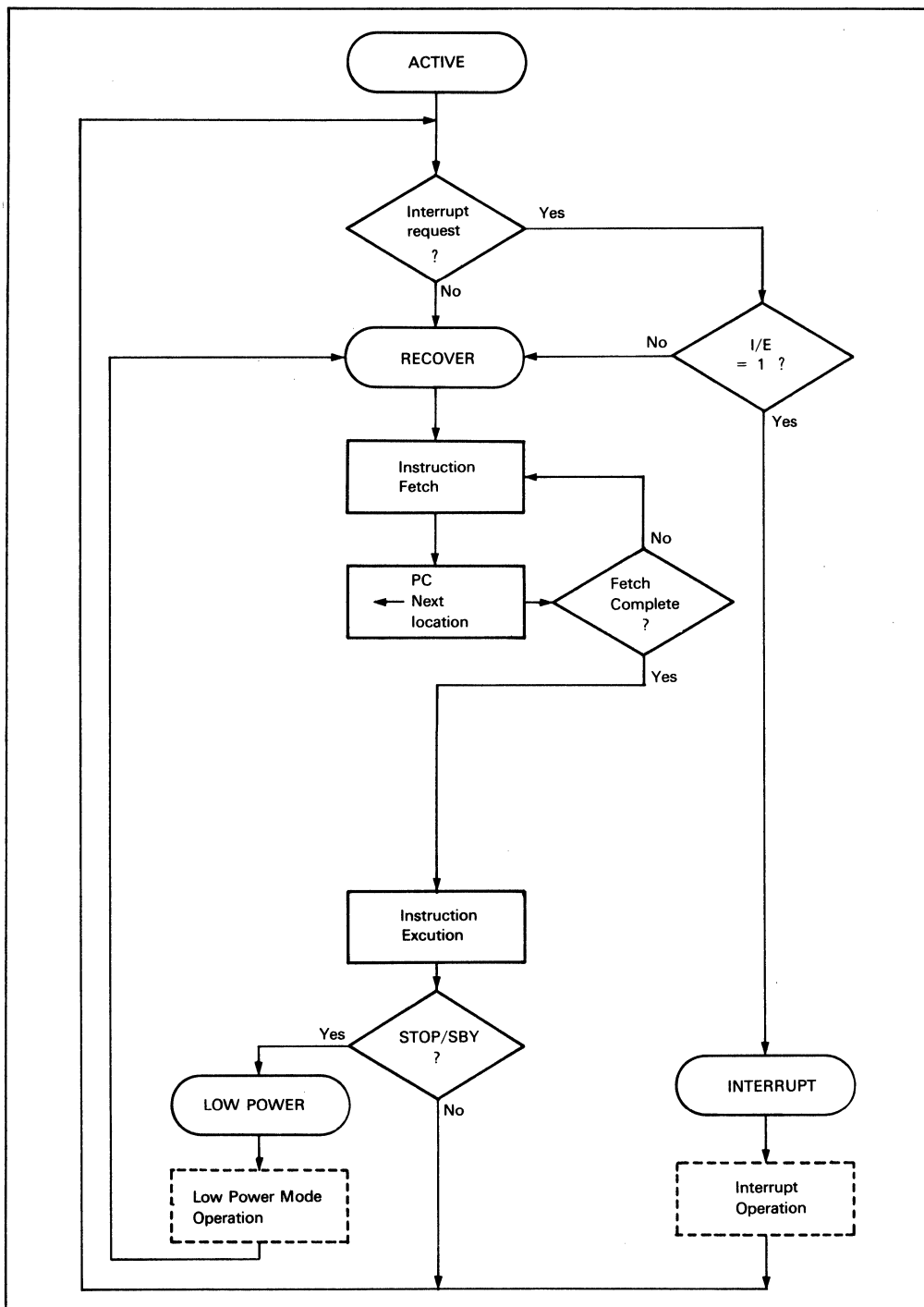


Figure 13. MCU Operation Sequence (MCU Operation Cycle)



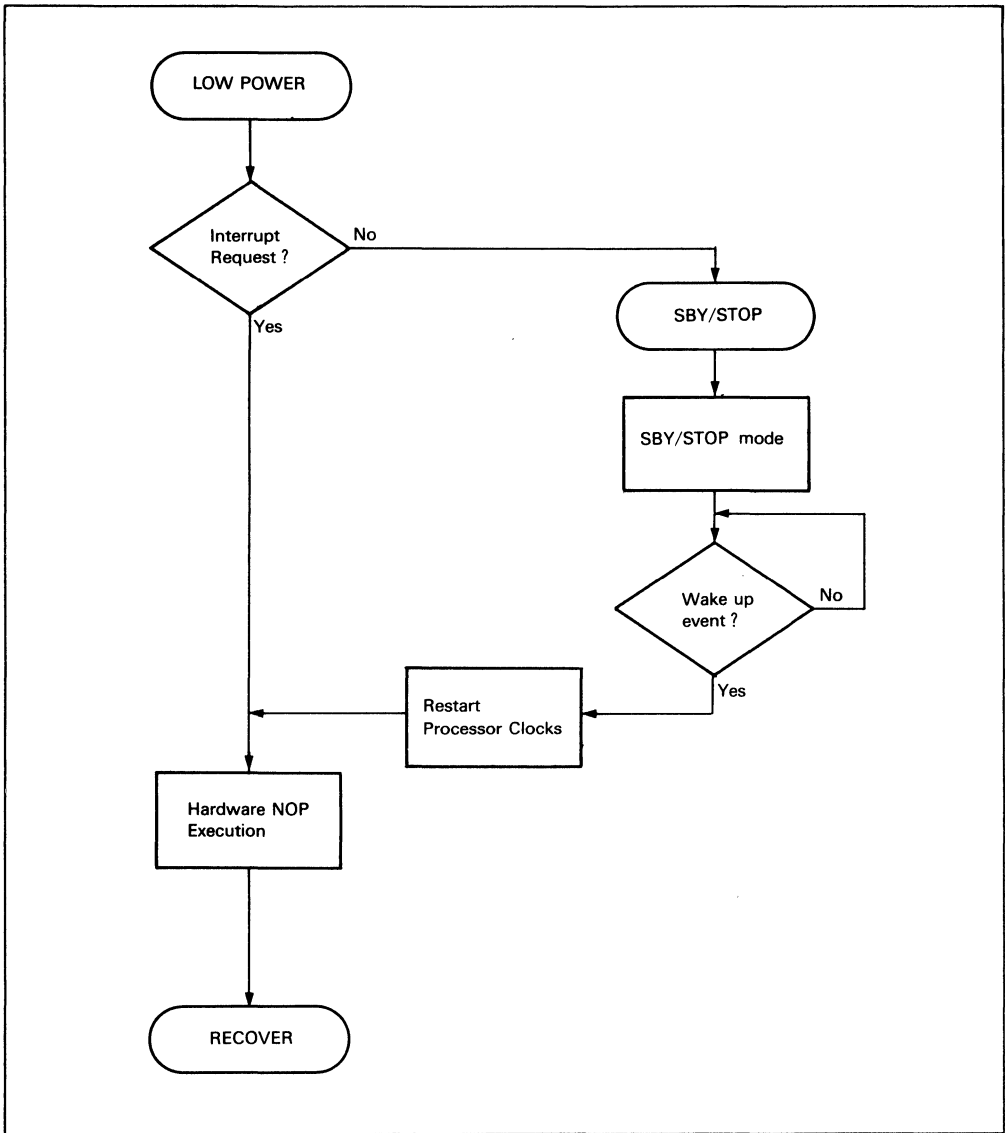


Figure 14. MCU Operation Sequence (Low Power Mode Operation)

PLL Function

The PLL function performs phase comparison between an external input signal and an internal reference signal, and outputs a comparison result signal. Block diagram is shown in figure 15.

PLL Features:

- 12 programmable reference frequencies (1, 2, 5, 6.25, 9, 10, 12.5, 18, 20, 25, 50, 100 kHz)
- Two dividing modes
 - Pulse swallow mode
divide ratio: 1024 to $(2^{15} - 1)$
 - Direct mode
divide ratio: 4 to $(2^{15} - 1)$
- Two independent comparison output signal pins
- PLL lock detection function

Reference frequency generator: The reference frequency generator divides source oscillation (4.5 MHz) to generate twelve different reference frequencies f_r : 1, 2, 5, 6.25, 9, 10, 12.5, 18, 20, 25, 50, and 100 kHz. Any of them can be selected by programming bit 0 to bit 3 of PLL control register A (PCRA₀-PCRA₃).

Variable divider: The variable divider is a down-counter composed of a 5-bit M counter and a 10-bit A counter. In direct dividing

mode, the variable divider functions as a 15-bit down-counter with connected M and A counters to perform the auto-reload function. In pulse swallow dividing mode, both M and A counters function as down-counters which input 2-modulus prescaler (mode 1/33) output. When the M counter reaches 0, 2-modulus prescaler mode changes from 1/33 to 1/32, and the A counter continues to count. When the A counter reaches 0, the M and A counters are auto-reloaded and start counting again. The dividing mode (direct or pulse swallow) can be selected by programming bit 2 of PLL control register B (PCRB₂). Divide value should be set in the PLL data register. The value is set in the PLL reload register via the PLL data register. The contents of the PLL data register (15 bits) are loaded in the PLL reload register automatically by the write instruction to the lower four bits of the PLL data register (PDRA register). Therefore, data must be written in the registers in the following order: PDRD, PDRC, PDRB, and PDRA.

Phase comparator: The phase comparator detects phase difference between the reference frequency (f_r) and the output signal (f_v) from the variable divider. The result is output from the $\phi 1$ and $\phi 2$ pins, as shown in figure 16, figure 17.

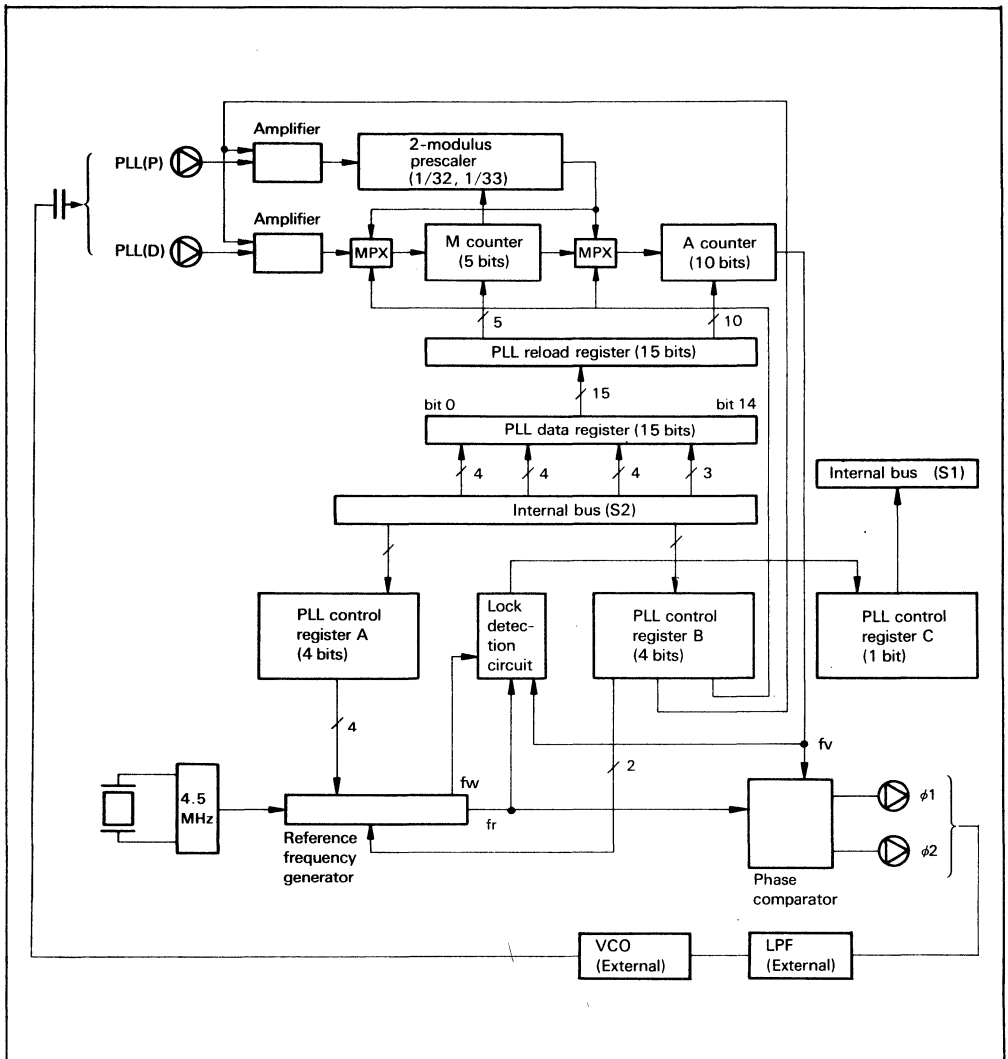


Figure 15. PLL Function Block Diagram

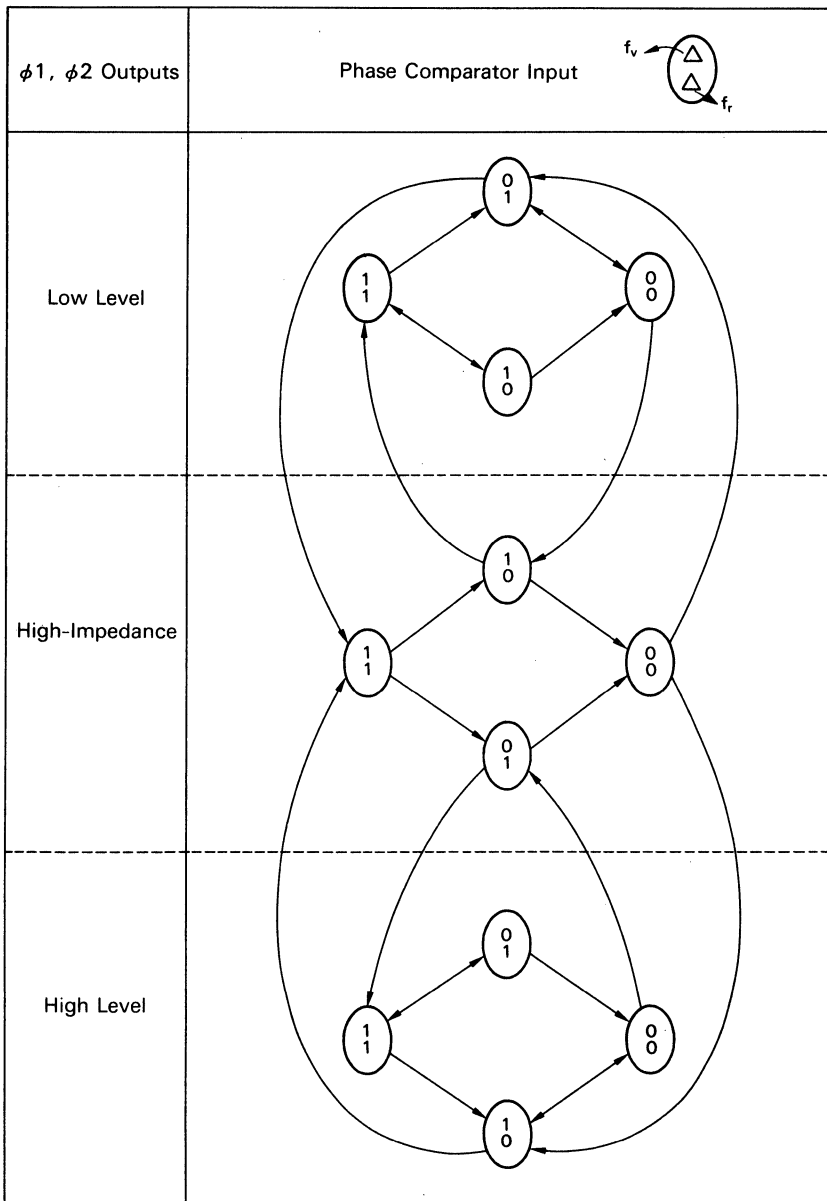


Figure 16. State Diagram (Phase Comparator)

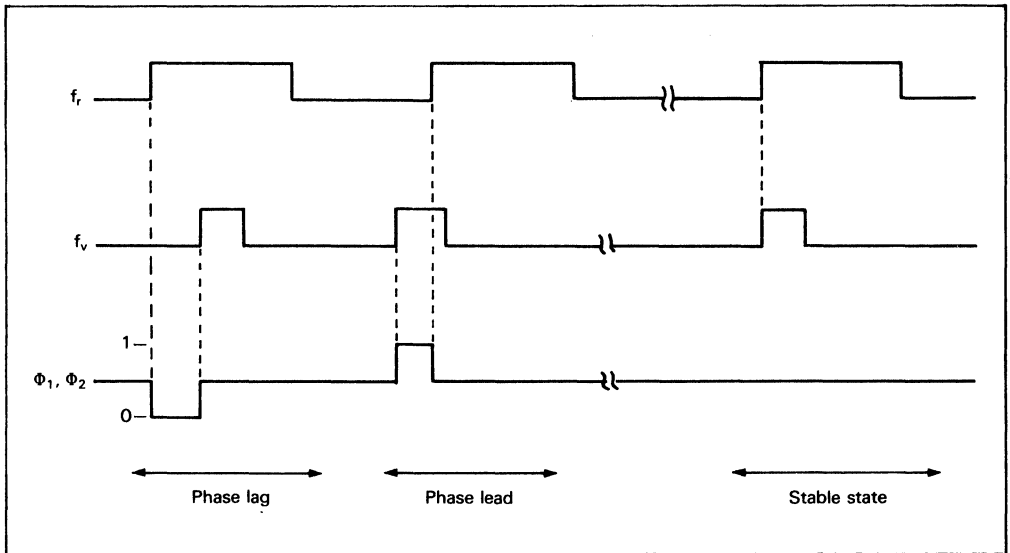


Figure 17. Input/Output Waveform (Phase Comparator)

Lock detection circuit: If the phase difference between the reference frequency (f_r) and a signal (f_v) generated by dividing an external input signal through the variable divider is less than a specified value $\pm \alpha$, PLL is assumed to be locked and bit 3 of the PLL control register C (PCRC₃) is set. The set condition of PCRC₃ is shown in figure 18. PCRC₃ is reset automatically after being read. Note: Value α varies with programming bit 0 and bit 1 of PLL control register B (PCRB₀, PCRB₁).

When entering the stop mode, set PCRB₃ to 0 and PLL is disabled. PLL (P) and PLL (D) are pulled down to the GND so that current is not consumed by the alternate amplifier.

PLL control register A (PCRA: \$005): PLL control register A is a 4-bit write-only register (figure 19).

PLL control registers B, C (PCRB: \$006, PCRC: \$006): PLL control register B is a 4-bit write-only register. PLL control register C is a 1-bit read-only register (figure 20).

PLL data register A (PDRA: \$007)

PLL data register B (PDRB: \$008)

PLL data register C (PDRC: \$009)

PLL data register D (PDRD: \$00A): PLL data registers A, B and C are 4-bit write-only registers, and PLL data register D is a 3-bit write-only register (figure 21).

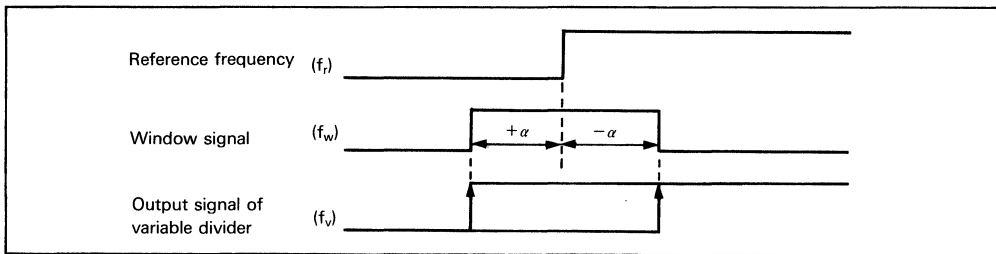


Figure 18. PCRC₃ SET Condition

3	2	1	0	
PCRA ₃	PCRA ₂	PCRA ₁	PCRA ₀	
← 0 → (Initial value)				
← W → (Read/Write)				
↑ Reference frequency selection				

PCRA ₃	PCRA ₂	PCRA ₁	PCRA ₀	Reference frequency (kHz)
0	0	0	0	1
0	0	0	1	5
0	0	1	0	6.25
0	0	1	1	9
0	1	0	0	10
0	1	0	1	12.5
0	1	1	0	25
0	1	1	1	50
1	0	0	0	2
1	0	0	1	10
1	0	1	0	12.5
1	0	1	1	18
1	1	0	0	20
1	1	0	1	25
1	1	1	0	50
1	1	1	1	100

SEM/SEMD and REM/REMD instructions cannot be used.

Figure 19. PLL Control Register A (PCRA: \$005)



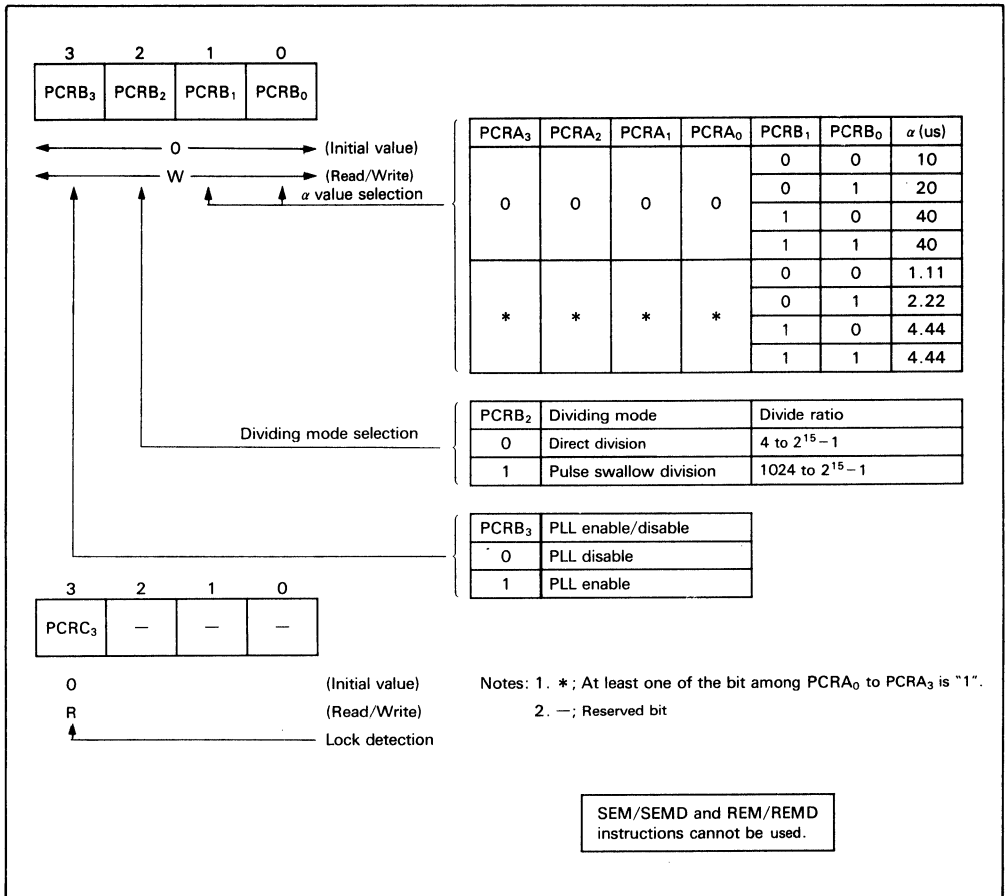


Figure 20. PLL Control Register B, C (PCRB: \$006, PCRC: \$006)

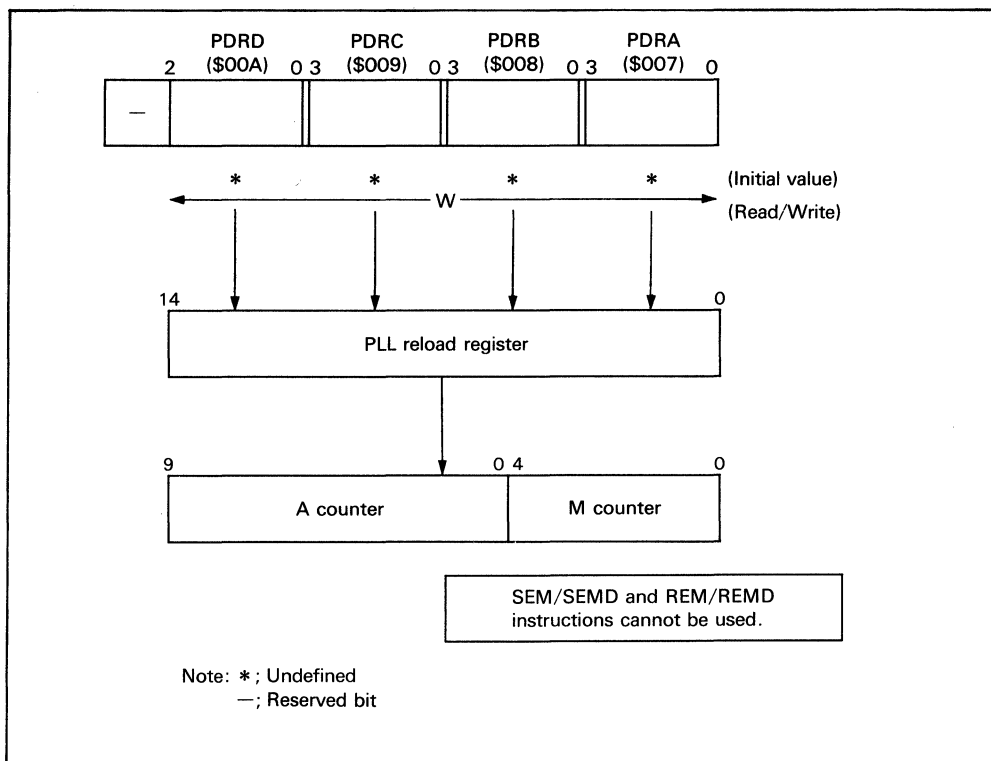


Figure 21. PLL Data Register and PLL Reload Register

IF Counter

IF Counter Features:

- Resolution: 16 bits
- Gate time: 1, 4, 8, ∞ ms
- Input signal: 15 MHz max.

IF Counter Function: The IF counter is a 16-bit binary counter whose data can be read. It is used to detect a stop signal during auto-search tuning; if a desired IF frequency range is found by counting the input frequency of the IF pin during auto-search tuning, it can be assumed that a radio station exists on the received frequency. The block diagram of the IF counter is shown in figure 22.

Count time (gate signal) of the IF counter can be selected from among 1, 4, 8 and ∞ ms by the IF counter control register. After all, the frequency input to the IF pin can be measured by counting the number of pulses input to the IF counter within the selected count time.

The IF counter is reset by clearing the IF clear start bit of the IF counter control register, and initiates counting by setting the IF clear start

bit. When the IF clear start bit is set, the busy bit is set, and when counting is terminated, it is cleared. Accordingly, whether or not counting is being performed can be acknowledged by software. Note that when entering into the stop mode, IFC1₃ must be set to 0 and the IF counter must be disabled. The IF pin is pulled down to the GND, so that current is not consumed by the alternate amplifier.

IF counter control register 1 (IFC1: \$028): IF counter control register 1 is a 4-bit write-only register (figure 23).

IF counter data register A (IFDA: \$029)
IF counter data register B (IFDB: \$02A)
IF counter data register C (IFDC: \$02B)
IF counter data register D (IFDD: \$02C): IF counter data registers A to D are 4-bit read-only registers. The most significant digit is IFDD, the other bits are, in order: IFDC, IFDB, and IFDA (figure 24).

IF counter control register 2 (IFC2: \$028): IF counter control register 2 is a 1-bit read-only register (figure 25).

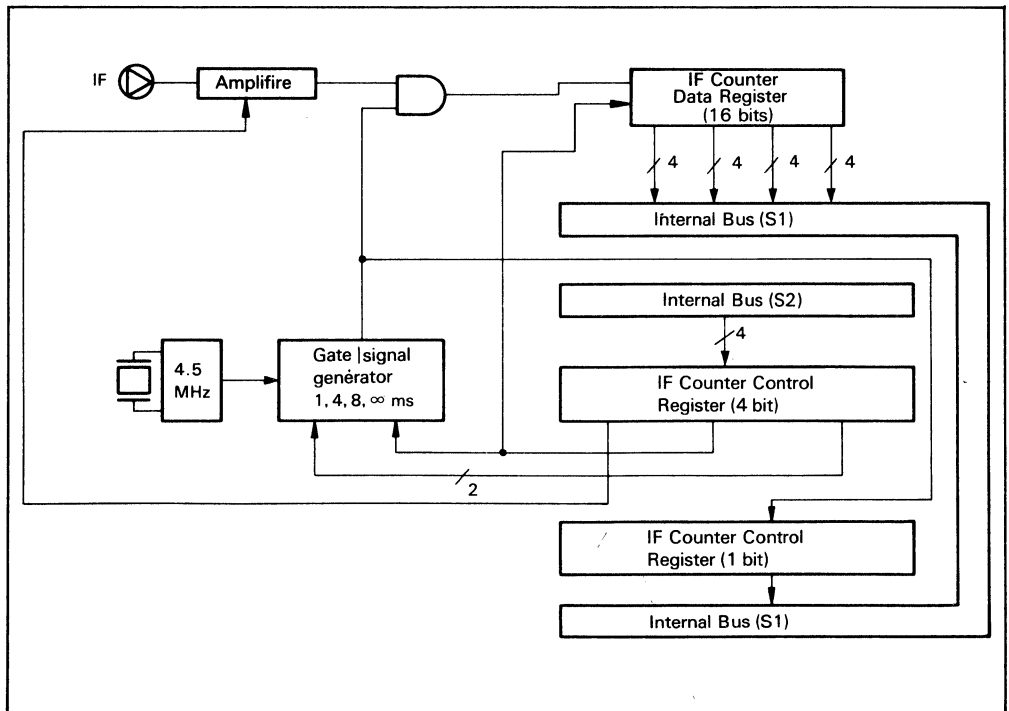


Figure 22. IF Counter Block Diagram



Gate Signal: The IF counter's gate signal time is specified by the IF counter control register 1. The basic clock timing is a 1 ms pulse generated asynchronously with an instruction. Dividing this clock produces a 1, 4, or 8 ms gate signal. (Gate signal is selected among 1, 4, 8, ∞ ms.) Accordingly, even if the IF clear start bit of the IF counter control register 1 is set to initiate counting, the IF counter does not start counting until the first basic clock is generated after executing the current instruction. Time difference between the busy bit and the actual gate signal is max. 1 ms, independent of the specified gate time, since basic clock timing is 1 ms.

Note: Precautions when gate signal ∞ is selected.

When gate signal ∞ is selected, the counter always operates by the IF input signal. Consequently, if data is read at counter update wrong data may be read. Thus, a gate must

be closed once before data is read. To close a gate in the ∞ mode, a value other than ∞ should be set in the gate signal selection bits (bit 1, 0) during setting of the IF enable bit (bit 3) and IF clear start bit (bit 2) of the IF counter control register 1 to 1.

To continue counting after data read, the ∞ mode should be set again. Make certain that the counter does not operate while the gate is being closed.

Accordingly, gate closure time should be considered when counting continues after data read.

When gate signal ∞ is selected, the IF counter does not start counting until the first basic clock is generated after executing the current instruction (max. 1 ms) even if the IF clear start bit of the IF counter control register is set to initiate counting.

Busy signal is invalid for the gate signal ∞ mode.

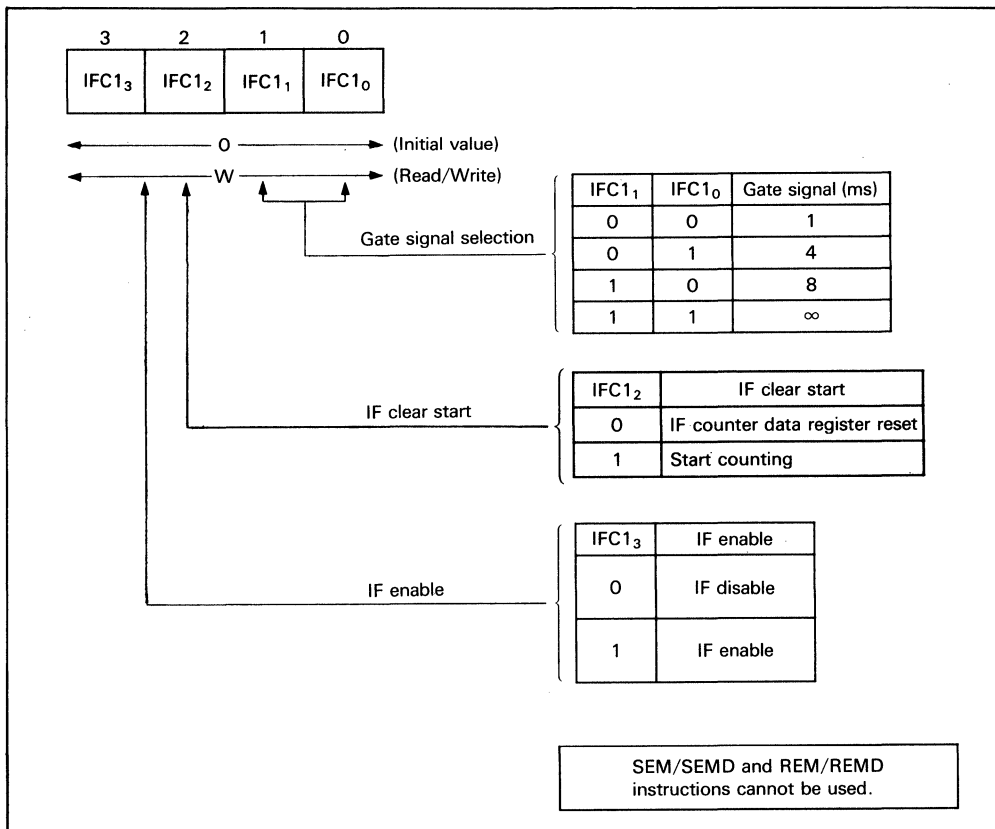


Figure 23. IF Counter Control Register 1 (IFC1: \$028)

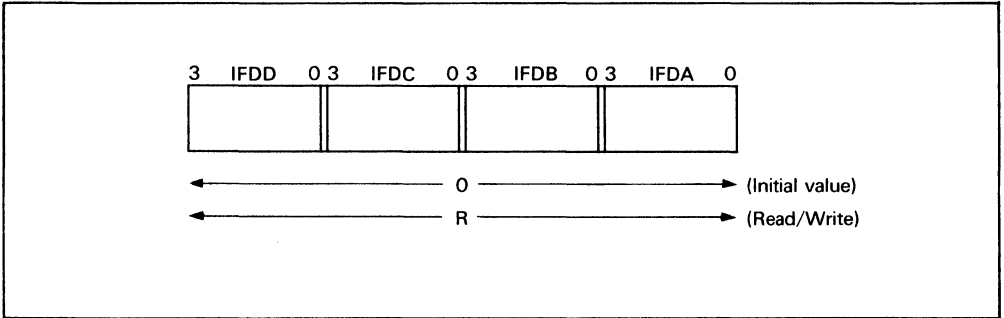


Figure 24. IF Counter Data Register (IFDA: \$029, IFDB: \$02A, IFDC: \$02B, IFDD: \$02C)

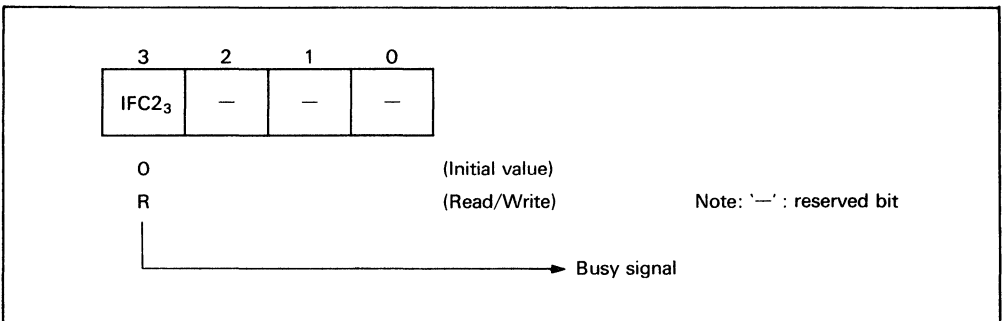


Figure 25. IF Counter Control Register 2 (IFC2: \$028)

Serial Mode Registers (SMR1: \$010, SMR2: \$014): The 4-bit write-only serial mode registers control the serial interface operation and the pins SCK₁, SCK₂, SI₁, SI₂, SO₁, and SO₂ as shown in figure 27.

The write signal to the serial mode register initializes the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from applying transfer clock, and it also resets the octal counter to \$0 simultaneously. Therefore, when the serial interface is in the "Transfer State", the write signal causes the serial mode register to cease the data transfer and to set the serial interrupt request flag.

The contents of the serial mode register is invalid until the second instruction is executed after a write instruction. Therefore, it will be necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to \$0 by MCU reset.

Bit 3 of the serial mode register is an enable bit for the serial interface. To operate the serial interface, this bit should be set before executing the STS instruction.

If the STS instruction is executed while the enable bit is set, the serial interface starts to operate. If the STS instruction is executed while the enable bits of both serial interfaces are set, two serial interfaces start to operate. The internal clocks of SERIAL 1 and SERIAL 2 are asynchronous each other.

The enable bit is automatically reset after the STS instruction execution.

Serial Clock Registers (SCR1: \$011, SCR2: \$015): The serial clock register is a 3-bit write-only register which controls the transfer clock source and prescaler divide ratio as shown in figure 28. A write signal to the serial clock register initializes internal state of the serial interface. A write signal to the serial clock register stops the serial data register and octal counter from applying transfer clock, and it resets the octal counter. Therefore, when the serial interface is in the transfer state, the write signal to the serial clock register stops the data transfer and sets the serial interrupt request flag.

Serial Data Registers (SR1L: \$012, SR1U: \$013, SR2L: \$016, SR2U: \$017): The 8-bit read/write serial data register consists of a lower digit (SR1L: \$012, SR2L: \$016) and a higher digit (SR1U: \$013, SR2U: \$017).

The data in the serial data register will be output from the SO₁ and SO₂ pins, from LSB to MSB, synchronously with the falling edge of the transfer clock. At the same time, external data will be input from the SI₁ and SI₂ pins to the serial data register, to LSB first, synchronously with the rising edge of the transfer clock. Figure 29 shows the I/O timing chart for the transfer clock signal and the data. The read/write operations of the serial data register should be performed after the completion of data transmit/receive.

Otherwise the data may not be guaranteed.

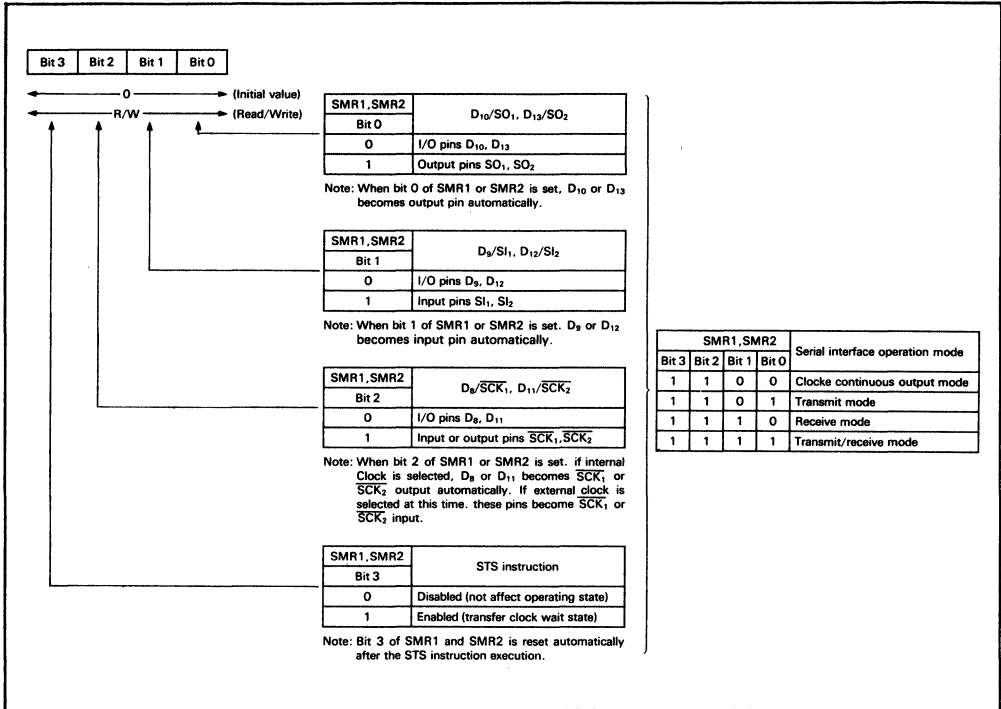


Figure 27. Serial Mode Register (SMR1: \$010, SMR2: \$014) and Operation Mode Selection

Table 9. Serial Interrupt Request Flag (IFS2: \$003,2, IFS1: \$023,2)

Serial Interrupt Request Flag	Interrupt Requests
0	No
1	Yes

Initial value: 0, R/W
 Note: Reset by the REM and REMD instructions. 1 cannot be set by software. Tested by the TM and TMD instructions.

Table 10. Serial Interrupt Mask (IMS2: \$003, 3, IMS1: \$023, 3)

Serial interrupt mask	Interrupt Requests
0	Enabled
1	Masked (held)

Initial value: 1, R/W
 Note: REM, REMD, SEM, SEMD, TM, and TMD instructions can be used.

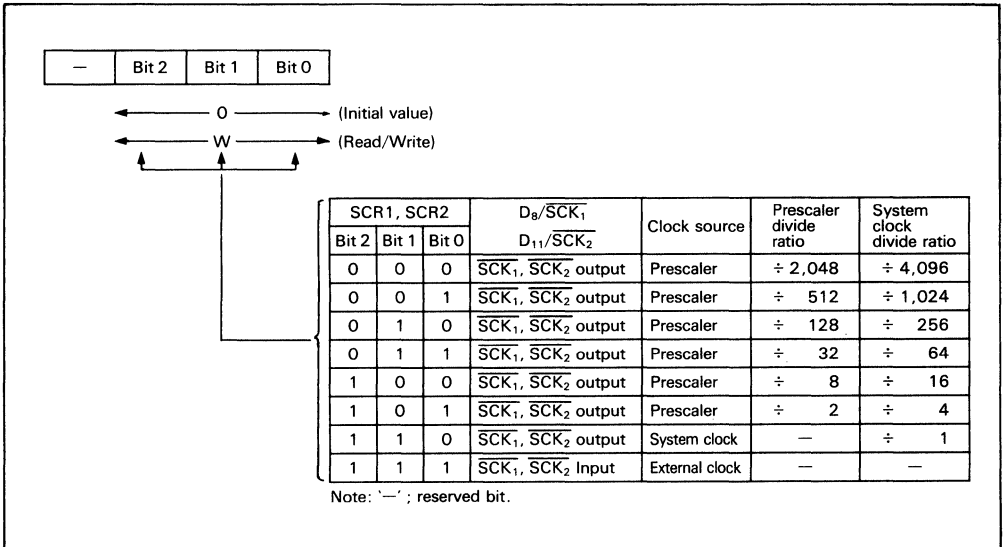


Figure 28. Serial Clock Register (SCR1: \$011, SCR2: \$015)

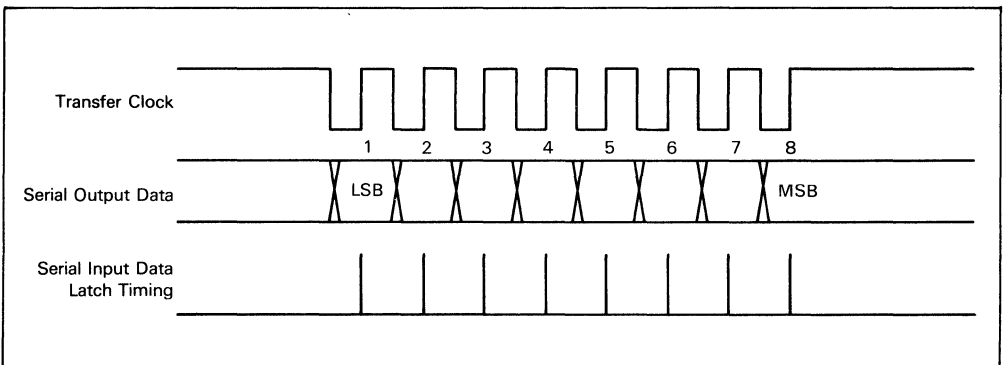


Figure 29. Serial Interface I/O Timing Chart

Serial Interrupt Request Flag (IFS1: \$023 bit 2, IFS2: \$003 bit 2): The serial interrupt request flag is set when the octal counter counts eight transfer clock signals, or when data transfer is discontinued by resetting the octal counter. See table 9.

Serial Interrupt Mask (IMS1: \$023 bit 3, IMS2: \$003 bit 3): The serial interrupt mask masks the interrupt request. See table 10.

Selection and Change of the Operation Mode: The serial interface operation modes which are determined by a combination of the value in the serial mode register are shown in figure 27.

Operating State of Serial Interface: The serial interface has four operating states, transfer disable state, STS waiting state, transfer clock waiting state, and transfer state, as shown in figure 30.

The transfer disable state is the initialization state of the serial interface. In this state, the serial interface does not operate even if the STS instruction is executed or the transfer clock is applied. Setting the enable bit of the desired serial interface enters it into STS waiting state.

When the STS instruction is executed in this state, the serial interface becomes transfer clock waiting state and serial transfer is enabled. When both enable bits of the serial interface 1 and 2 are set before executing the STS instruction, two serial interfaces start to

operate. If the transfer clock is applied during the transfer clock waiting state, the serial interface changes to transfer state, while the octal counter counts up and the serial data register changes simultaneously. However, if the consecutive clock output mode is selected, only transfer clock is output consecutively without transfer.

In the transfer state, the octal counter becomes 000 by 8 transfer clocks and the serial interrupt flag is set. At this time, if internal clock is selected, the serial interface changes to the transfer disable state, and if external clock is selected, it changes to the transfer clock waiting state. A write signal to the serial mode register during the transfer state resets the octal counter to 000 to stop transfer and sets the interrupt request flag simultaneously.

Example of Transfer Clock Error Detection: The serial interface malfunctions when the transfer clock is disturbed by external noises. In this case, transfer clock error can be detected by the procedure shown in figure 31. If more than 8 transfer clocks are applied in the transfer clock waiting state, the state of the serial interface changes as the following sequence: first, transfer state, second, transfer clock waiting state, and third, transfer state again. The serial interrupt flag should be reset before entering into the STS waiting state by writing data to the serial mode register. This procedure causes the serial interrupt request flag to be set again.

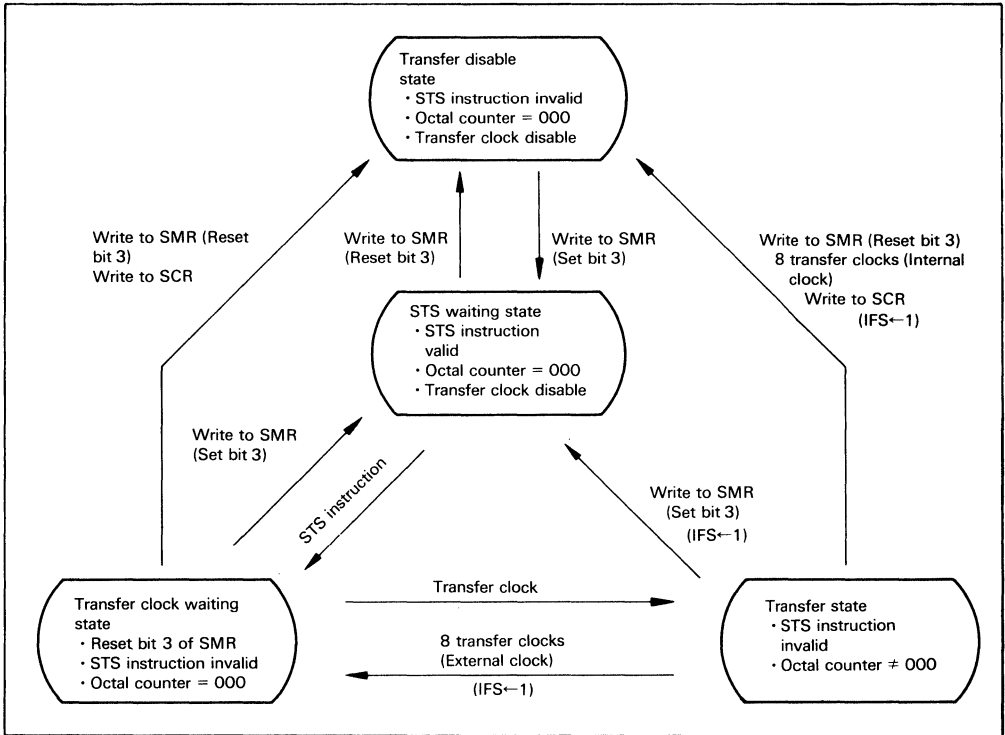


Figure 30. Operating State of Serial Interface

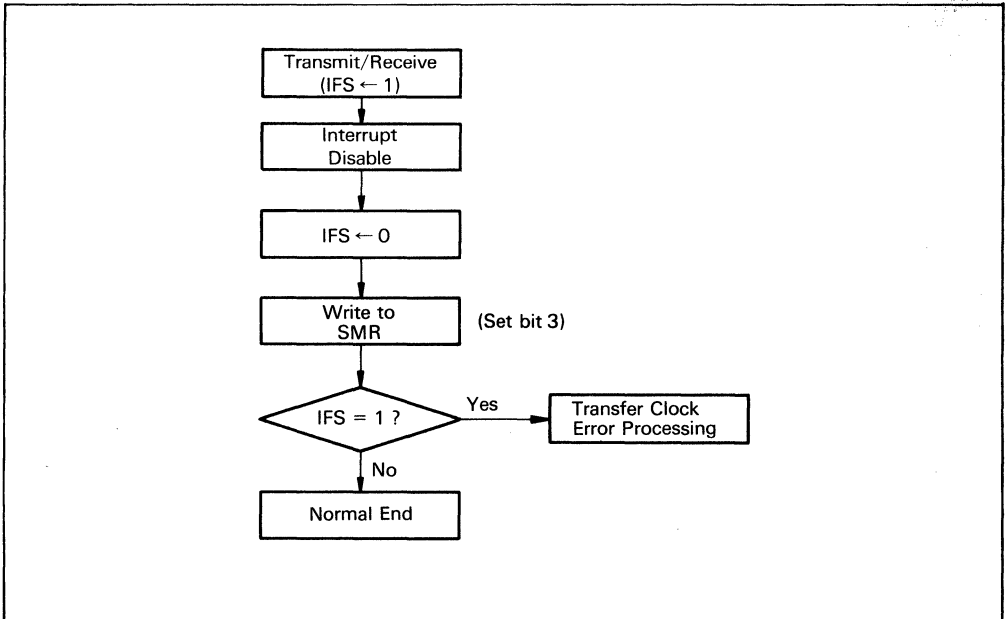


Figure 31. Example of Transfer Clock Error Detection

Timer

The MCU contains a prescaler, two timer/counters (timer-1, 2) and time-base prescaler (timer 3). Figures 32, 33 and 34 show the block diagrams of the timers.

Prescaler: The input to the prescaler is a system clock signal. The prescaler is initialized to \$000 by MCU reset before dividing the system clock. The prescaler keeps counting up except in MCU reset and stop mode. Timer input clock and serial transfer clock are selected by the timer mode registers (TMR1, TMR2) and serial clock registers (SCR1, SCR2) among prescaler outputs.

Operation of Timer 1, Timer 2: Timer 1 and 2 are multifunctional timers. They can be used as a free-running timer, event counter, reload timer, or PWM circuit (Timer 2 does not have a PWM function). Each function is selected by the timer mode register (TMR1, TMR2) and timer output register (TOR1, TOR2).

The timer/counter (TC1, TC2) is initialized to \$00 by MCU reset, and it starts to count up every input signal. As an input clock, the clock divided by the prescaler and an external clock can be used. When an external clock input is selected, external interrupt must be inhibited by setting the external interrupt mask bit (IM0 or IM1) since the external clock input pin is multiplexed with the external interrupt pin. (External interrupt cannot be inhibited by setting the interrupt enable bit of the timer output register.) If an input clock is applied after the timer counter reaches \$FF, the timer interrupt request flag (IFT1, IFT2) is set. If an auto-reload function is not selected, timer 1 and 2 function as free-run-

ning timer/event counter and continue to count up after returning to \$00. If the auto-reload function is selected, they are reload timers.

The timers initiate counting up from the timer load register (TLR1, TLR2) value loaded in the timer counter for each clock input after the timer counter reaches \$FF.

Timer 1 has a timer output circuit. This circuit changes output level when a clock is input after the timer counter reaches \$FF. An optional cycle clock signal can be output by combining this circuit and the reload timer. Also this output circuit becomes PWM output circuit if PWM function is specified by the timer output register. One cycle of the PWM output is 256 input clocks. The output becomes 1 during the time for the number of clocks set in the timer load register, and becomes 0 during the other time.

To obtain the voltage level in proportion to the value set in the timer load register, PWM output should be combined with low-pass filter.

Timer 3 Operation: Timer 3 is a prescaler which sets interrupt request flag (IFT3) every 125 ms.

- Timer interrupt request flag (IFT3: \$000 bit 2)
- Timer interrupt mask (IMT3: \$000 bit 3)

The timer interrupt mask masks the timer 3 interrupt request.

Timer 3 is initialized in the following condition.

- Power-on Reset
- MCU Reset when the data retention bit (MIS₃: \$004,3) is 0.

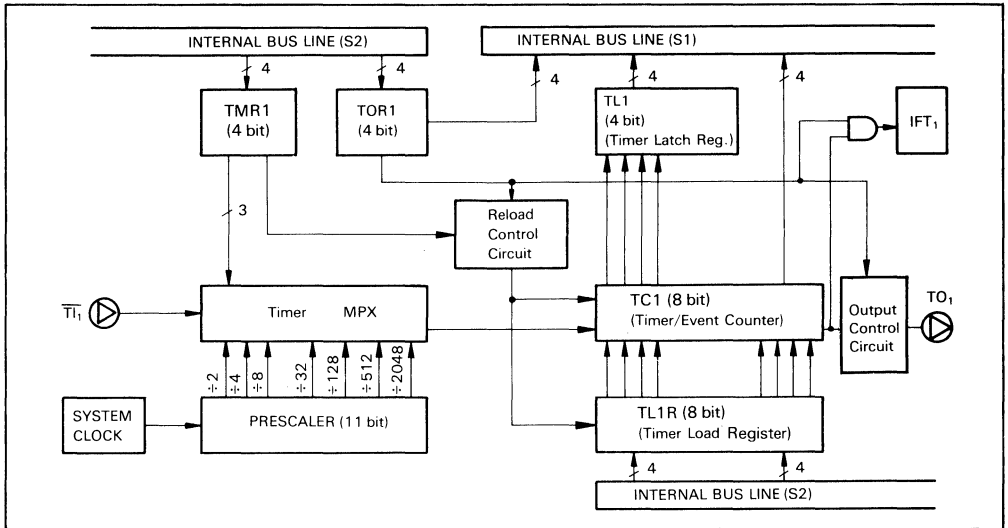


Figure 32. Timer 1 Block Diagram

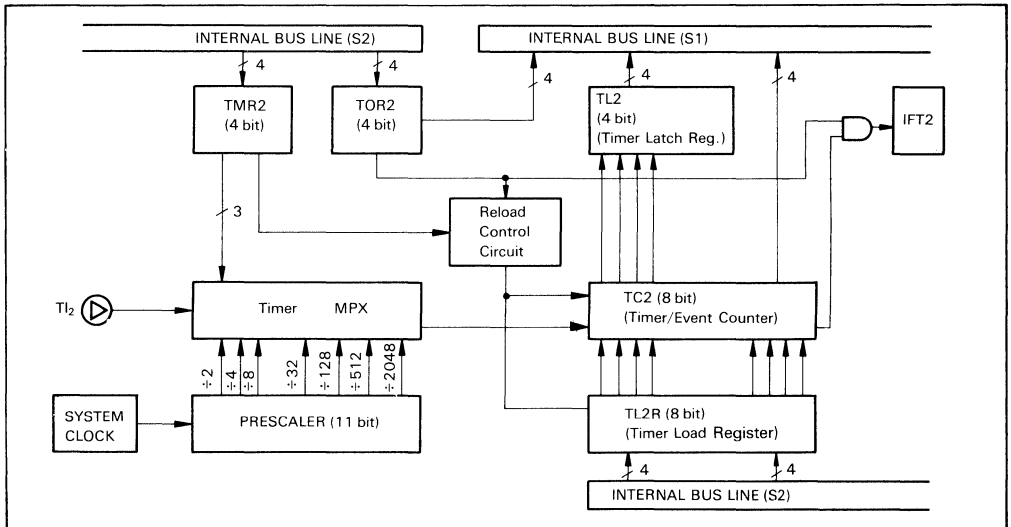


Figure 33. Timer 2 Block Diagram

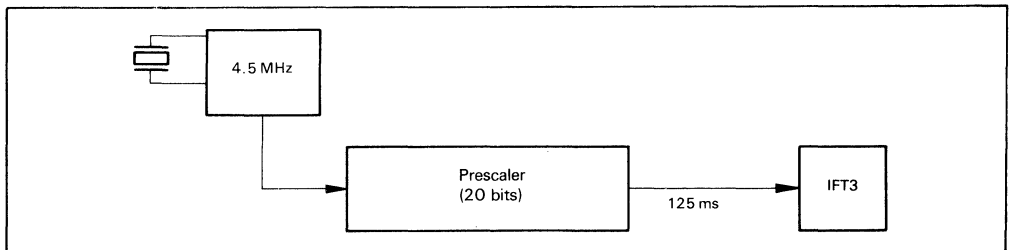


Figure 34. Timer 3 Block Diagram

Timer Mode Register 1, 2 (TMR1: \$018, TMR2: \$01C): The timer mode register is a 4-bit write-only register which selects the autoreload function, input clock, and prescaler divide ratio as shown in figure 35.

The timer mode register is initialized to \$0 by MCU reset.

The operation mode of the timer mode register is changed at the second instruction cycle after the timer mode register is written to. Initialization of the timer by a write to the timer mode register should be performed after the operation mode is completely changed.

Timer Output Register (TOR1: \$019, TOR2: \$01D): The timer output register is a 4-bit read/write register which controls the

timer output mode, PWM output, and external interrupts as shown in figure 36.

If bit 0 and 1 of the timer output register are set in the mode except for timer output disable mode, the pin becomes timer output pin automatically.

Combination of these modes and each mode of the timer 1 to 3 can produce optional frequency and optional duty clock signal. When PWM output is set, the timer output pin becomes PWM output pin independently of the timer output mode.

The timer output register is initialized to \$0 by MCU reset.

The operation mode of the timer output register is changed at the second instruction cycle after the timer output register is written to.

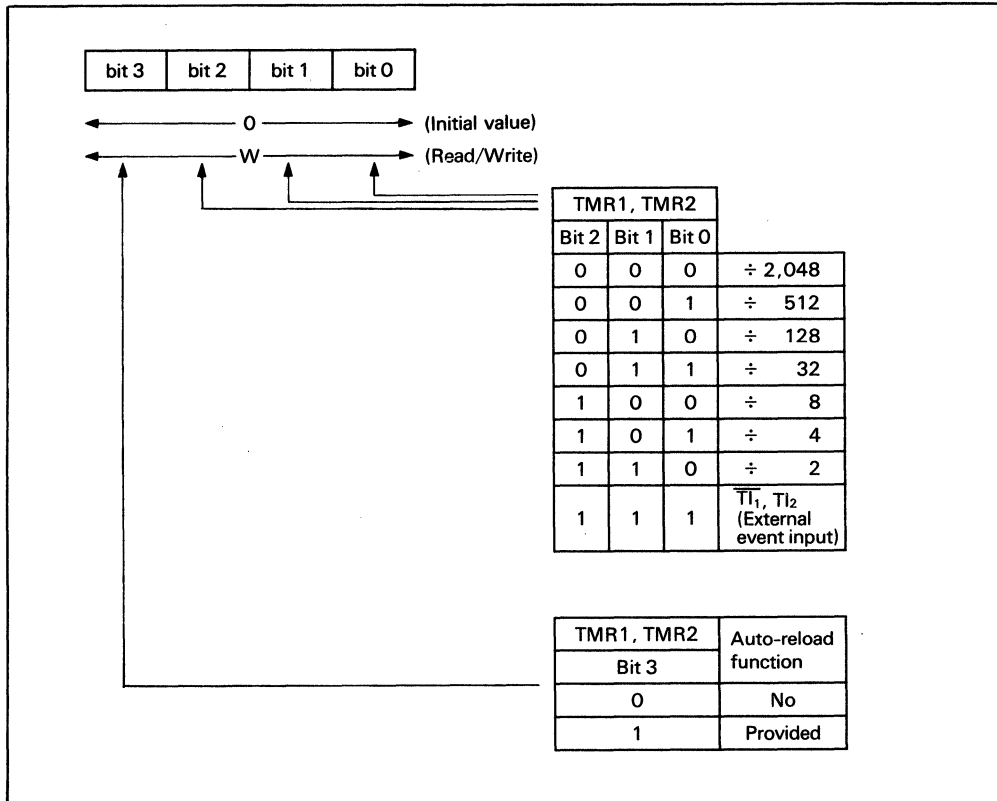


Figure 35. Timer Mode Register 1, 2 (TMR1: \$018, TMR2: \$019)

Timer 1, 2 (TC1L: \$01A, TC1U: \$01B, TL1L: \$01A, TL1U: \$01B, TC2L: \$01E, TC2U: \$01F, TL2L: \$01E, TL2U: \$01F): Timer 1 and 2 consist of write-only timer load register (8 bits) and read-only timer/event counter (8 bits) respectively. Each of them has a lower digit (TC1L: \$01A, TC2L: \$01E) and a higher digit (TC1U: \$01B, TC2U: \$01F).

The timer/event counter can be initialized by writing data into the timer load register. In this case, write the lower digit first, and then the higher digit. The timer load register is initialized to \$00 by the MCU reset.

The counter value of the timer can be obtained by reading the timer/event counter. In this case, read the higher digit first, and then the lower digit. The count value of the

lower digit is latched at the time when the higher digit is read.

Timer Interrupt Request Flag (IFT1: \$002 bit 0, IFT2: \$003 bit 0): The timer interrupt request flag is set by the overflow output of timer 1 or timer 2. If the PWM function is selected, the timer interrupt request flag is not set even if the overflow output generates.

See table 11.

Timer Interrupt Mask (IMT1: \$002 bit1, IMT2: \$003 bit 1): The timer interrupt mask masks an interrupt request from timer 1 or timer 2.

See table 12.

Table 11. Timer Interrupt Request Flag

Timer Interrupt Request Flag	Interrupt Request
0	No
1	Yes

Initial value: 0, R/W

Table 12. Timer Interrupt Mask

Timer Interrupt Mask	Interrupt Request
0	Enabled
1	Disabled (masks)

Initial value: 1, R/W

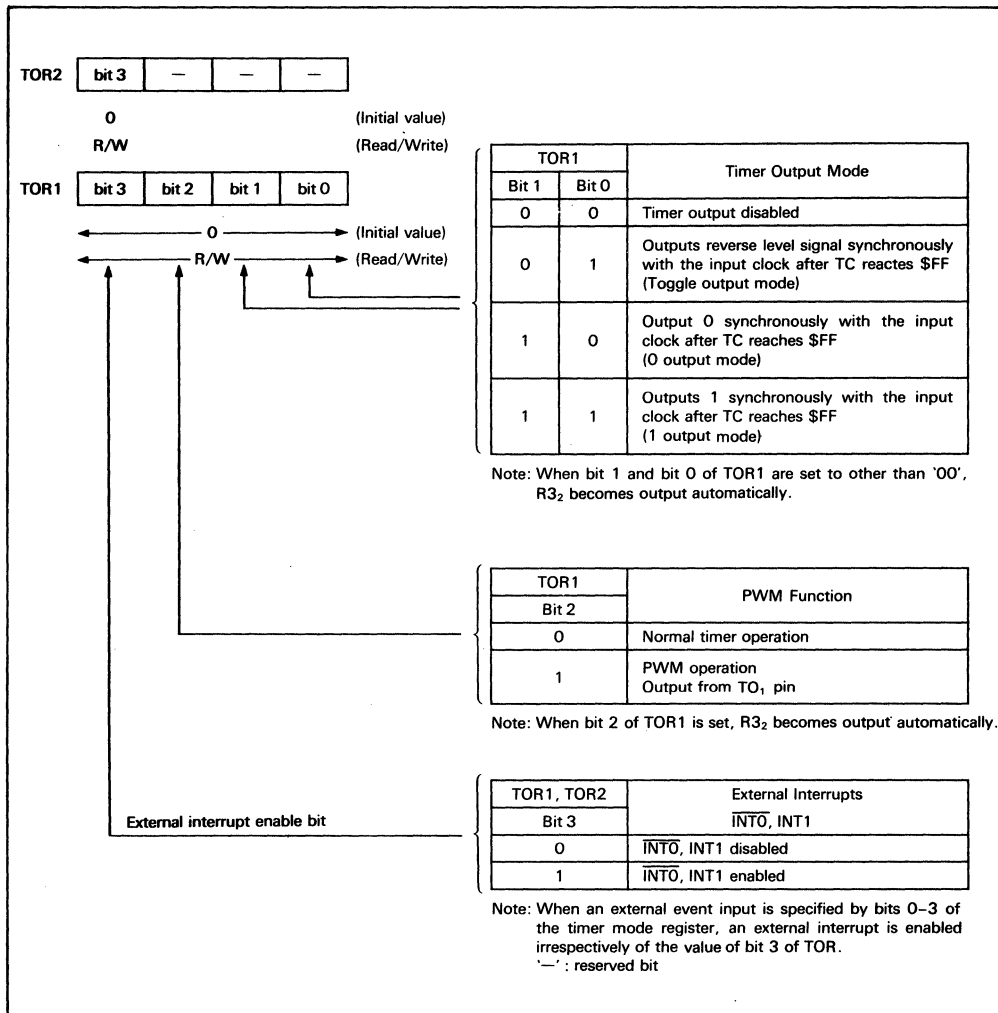


Figure 36. Timer Output Register

Operating Mode of Timer 1, Timer 2:
 Since timer 1 and timer 2 can select several functions as free-running, reload, PWM (timer 1 only), and can control clock input and timer output, various operating states can be specified by combination of these functions as shown in figure 37, 38. Required data should

be set in the timer mode register and timer output register for the selected operating state.
 Example of the timer output waveform is shown in figure 39. The waveform depends on the operation mode.

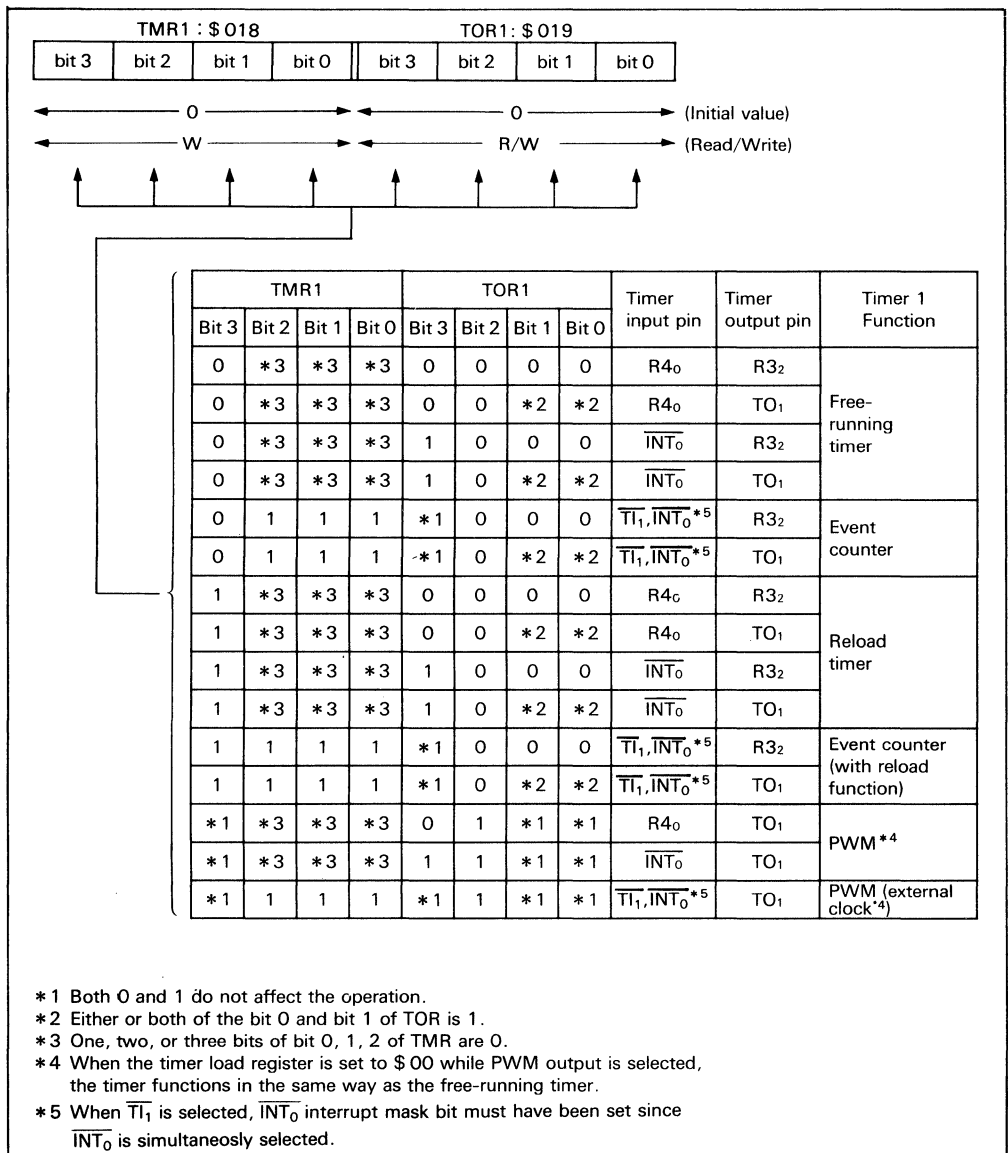


Figure 37. Combination of Timer 1 Operation Modes

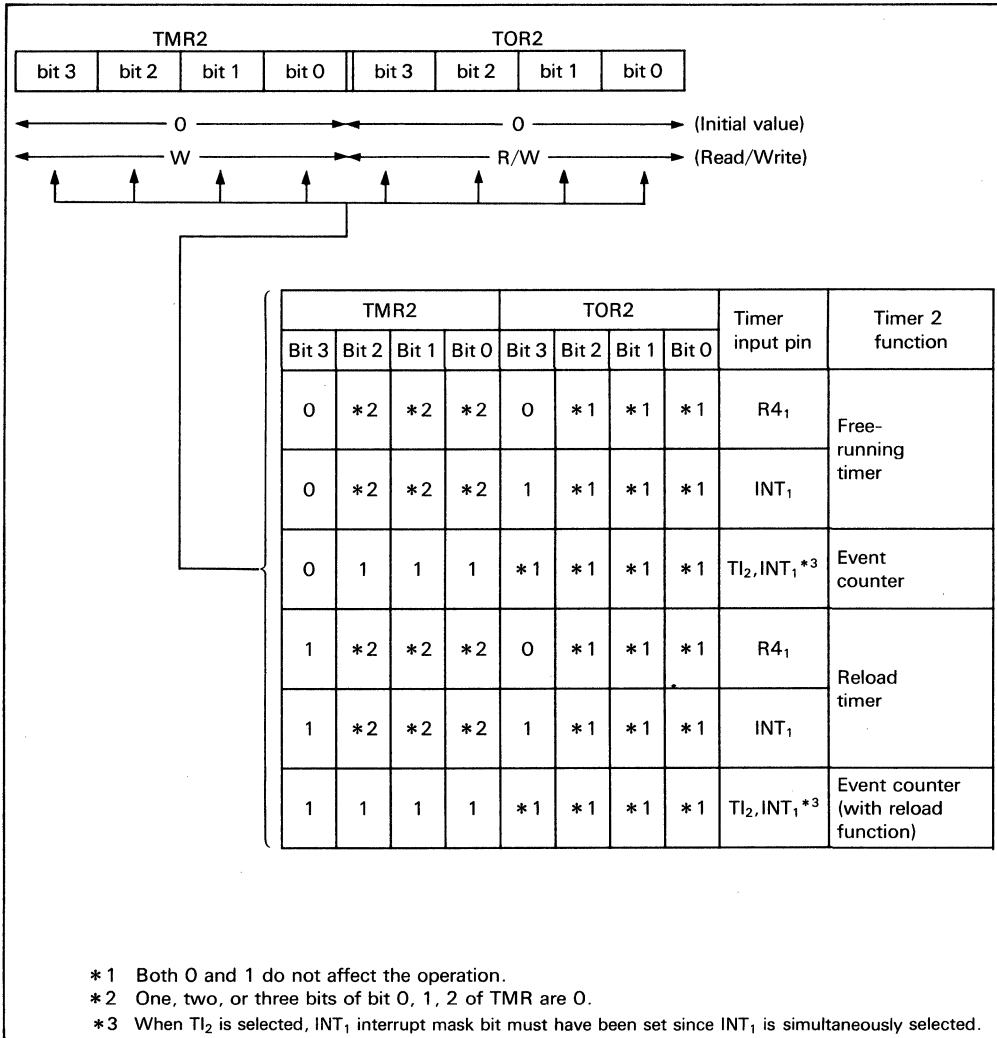


Figure 38. Combination of Timer 2 Operation Modes

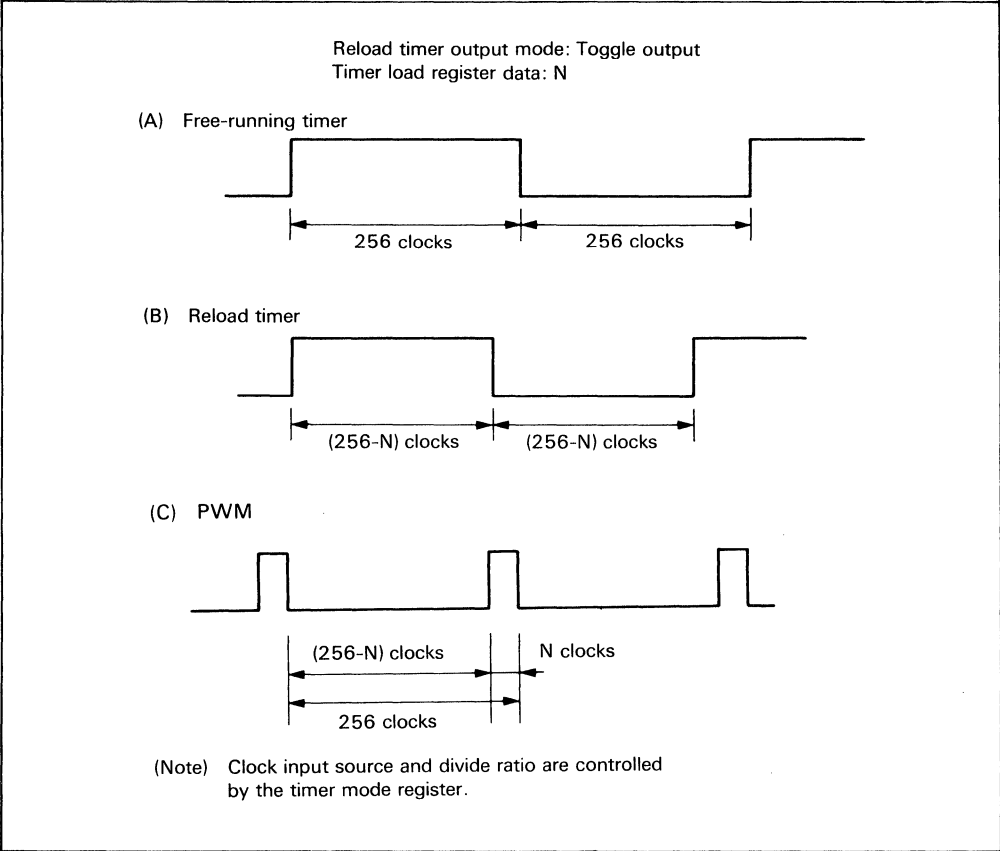


Figure 39. Examples of Timer Output Waveform

A/D Converter

The MCU incorporates an A/D converter operating in the sequential comparison method with a resistor ladder. It can measure two analog inputs with 8-bit resolution. A block diagram of the A/D converter is shown in figure 40.

The A/D converter is composed of the following registers and bit.

A/D mode register (AMR: \$00C): The A/D mode register is a write-only register. Bits 0 and 1 select an A/D conversion period, and bits 2 and 3 select a channel (figure 41).

A/D data register (ADRU: \$00E, ADRL: \$00D): The A/D data register is a read-only register. Data read during A/D conversion is not guaranteed. After completion of a conversion,

resulting data is maintained until the following conversion starts (figure 42).

A/D start bit, status flag (ADSF: \$020, 0): Writing 1 into the A/D start bit initiates A/D conversion. On completion of A/D conversion, the converted data is stored in the A/D data register simultaneously with setting the A/D interrupt flag, and the A/D start flag is cleared.

Note that writing into ADSF should be performed by bit manipulation instruction SEM or SEMD. It is invalid with the REM/REMD instructions. ADSF must not be written to during A/D conversion. The configuration of ADSF is shown in figure 43.

Precautions on A/D converter use: Port output instructions should not be executed during A/D conversion to allow the A/D converter to operate stably.

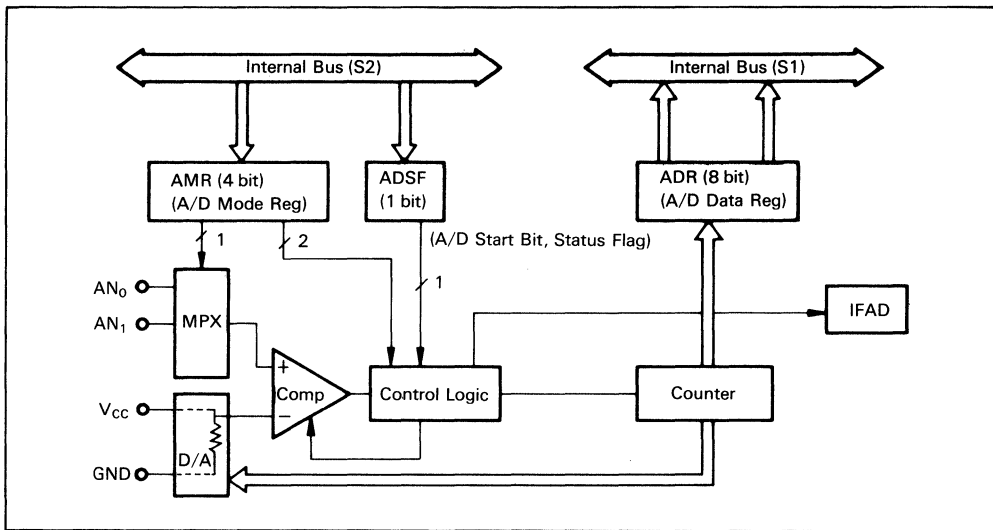


Figure 40. A/D Converter Block Diagram

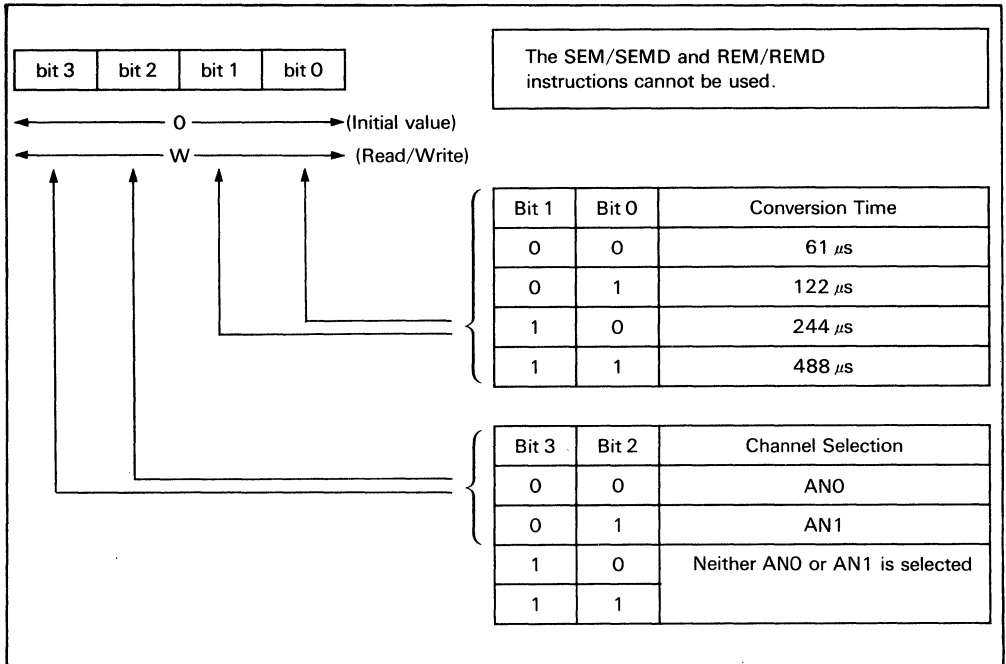


Figure 41. A/D Mode Register (AMR: \$00C)

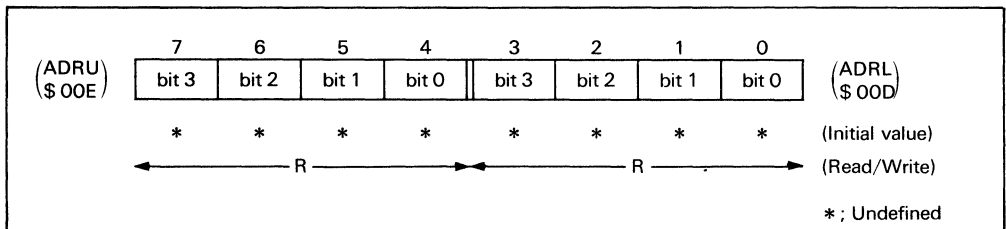


Figure 42. A/D Data Register (ADRU: \$00E, ADRL: \$00D)

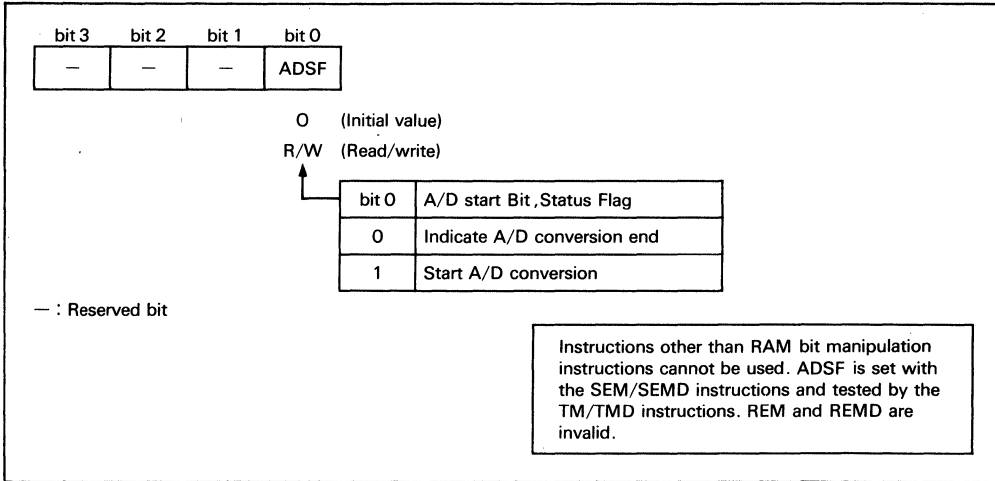


Figure 43 A/D Start Bit, Status Flag (ADSF: \$020,0)

Liquid Crystal Display Circuit

A LCD circuit can directly drive a liquid crystal in three drive systems, static, 1/2 duty, and 1/3 duty with its three common signal pins and 28 segment signal pins. The LCD circuit is comprised of RAM, controller, and driver as shown in figure 44.

RAM (\$3A0-\$3BB): RAM in the LCD circuit is dual-port RAM which sends display data to the segment signal pin without software. Relation between display RAM area and segment signal is shown in figure 45. By writing data in RAM area, the corresponding

segment pin automatically outputs it as display data. 1 means light on, and 0 means light off.

Control Section: The control section consists of the following three registers:

- LCD output register (LOR: \$024) (figure 46)
- LCD control register (LCR: \$025) (figure 47)
- LCD mode register (LMR: \$026) (figure 48)

LCD Driver: The LCD driver has three common signal pins and 28 segment signal pins. 16 segment pins SEG13 to SEG28 are multiplexed with output ports R8, R7, R6, and R5.

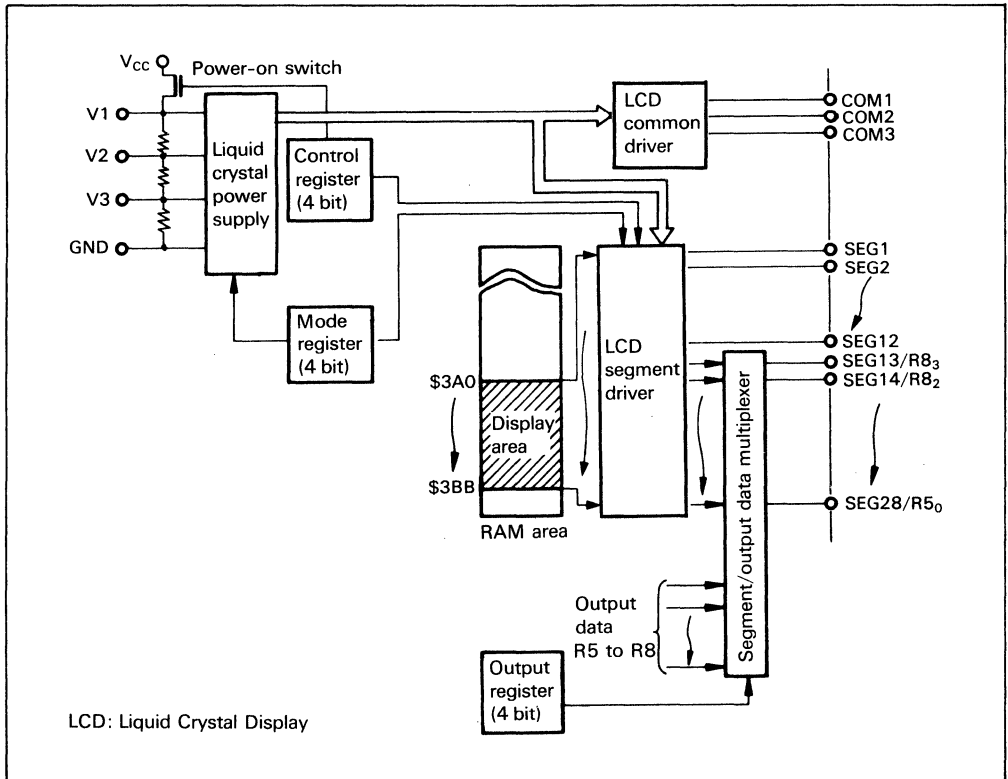
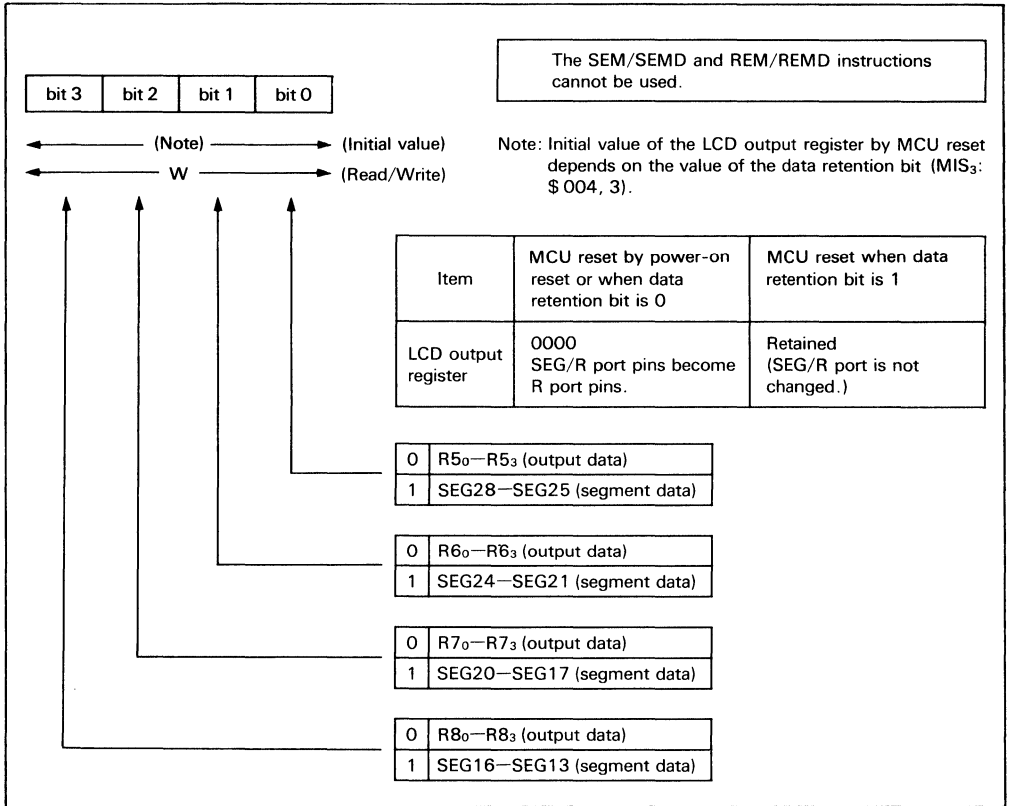


Figure 44. LCD Circuit Block Diagram

BIT 3	BIT 2	BIT 1	BIT 0	Address (Hexadecimal)
—	SEG 1	SEG 1	SEG 1	\$3A0
—	SEG 2	SEG 2	SEG 2	\$3A1
—	SEG 3	SEG 3	SEG 3	\$3A2
—	SEG 4	SEG 4	SEG 4	\$3A3
—	SEG 5	SEG 5	SEG 5	\$3A4
—	SEG 6	SEG 6	SEG 6	\$3A5
—	SEG 7	SEG 7	SEG 7	\$3A6
—	SEG 8	SEG 8	SEG 8	\$3A7
—	SEG 9	SEG 9	SEG 9	\$3A8
—	SEG 10	SEG 10	SEG 10	\$3A9
—	SEG 11	SEG 11	SEG 11	\$3AA
—	SEG 12	SEG 12	SEG 12	\$3AB
—	SEG 13	SEG 13	SEG 13	\$3AC
—	SEG 14	SEG 14	SEG 14	\$3AD
—	SEG 15	SEG 15	SEG 15	\$3AE
—	SEG 16	SEG 16	SEG 16	\$3AF
—	SEG 17	SEG 17	SEG 17	\$3B0
—	SEG 18	SEG 18	SEG 18	\$3B1
—	SEG 19	SEG 19	SEG 19	\$3B2
—	SEG 20	SEG 20	SEG 20	\$3B3
—	SEG 21	SEG 21	SEG 21	\$3B4
—	SEG 22	SEG 22	SEG 22	\$3B5
—	SEG 23	SEG 23	SEG 23	\$3B6
—	SEG 24	SEG 24	SEG 24	\$3B7
—	SEG 25	SEG 25	SEG 25	\$3B8
—	SEG 26	SEG 26	SEG 26	\$3B9
—	SEG 27	SEG 27	SEG 27	\$3BA
—	SEG 28	SEG 28	SEG 28	\$3BB
	COM3	COM2	COM1	

Note: Some areas do not correspond to a segment signal.
They can be read/written to.

Figure 45. LCD RAM Area and Segment Signals



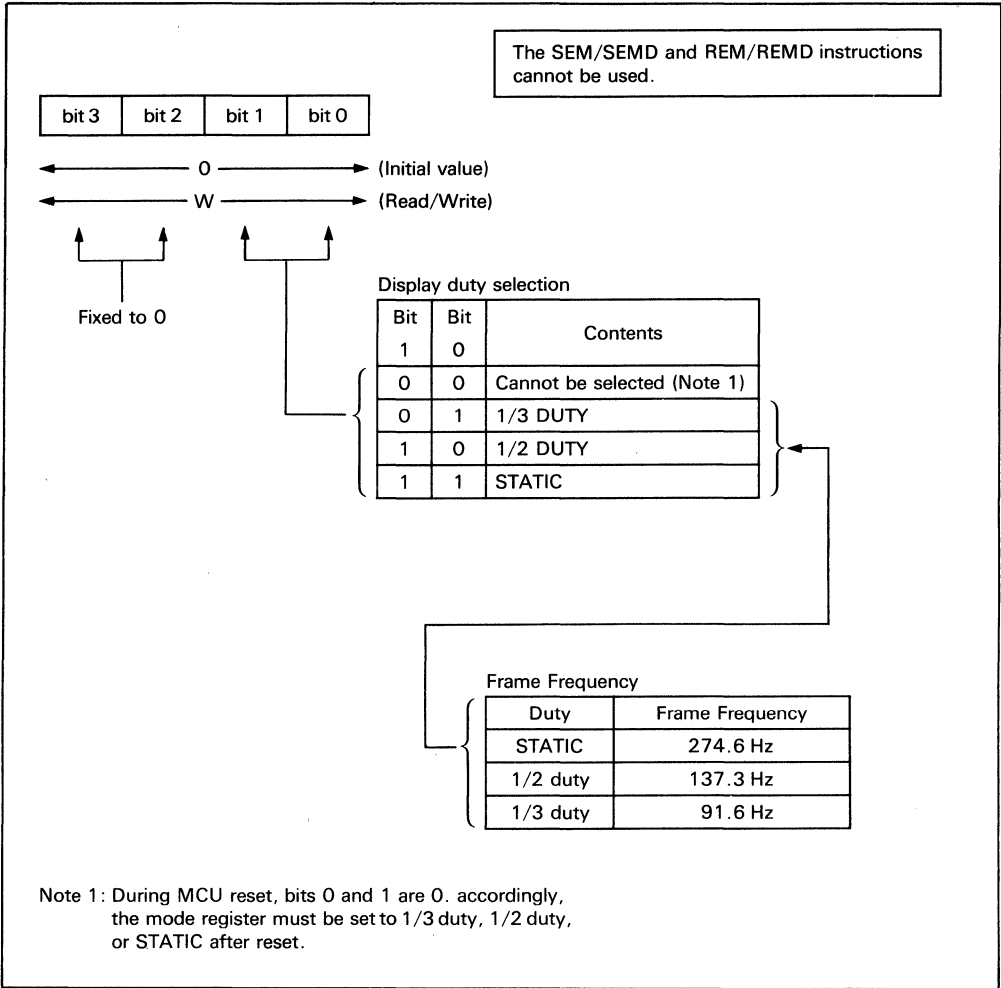


Figure 48. LCD Mode Register (LMR: \$026)

Large LCD Panel Driving and Driving Voltage (V_{LCD}): When using the large LCD panel, lower the dividing resistance by implementing the external resistors parallel to the internal dividing resistors as shown in figure 49.

Since the liquid crystal display board is of matrix configuration, the path of the charge/discharge current through the load capacitors is very complicated. Moreover, as it varies depending on display condition, a value of resistance cannot be simply determined by referring to the load capacitance of liquid

crystal display. A value of resistance must be experimentally determined according to the demand for power consumption of the equipment in which the liquid crystal display is implemented. (A capacitor, $C=0.1$ to $0.3 \mu F$ can be used if necessary.) In general, R is $1 k\Omega$ to $10 k\Omega$.

The following figure shows a connection when changing the liquid crystal driving voltage (V_{LCD}). In this case, power supply switch for dividing resistor (power switch) should be turned OFF. (Bit 1 of the LCR register is 0).

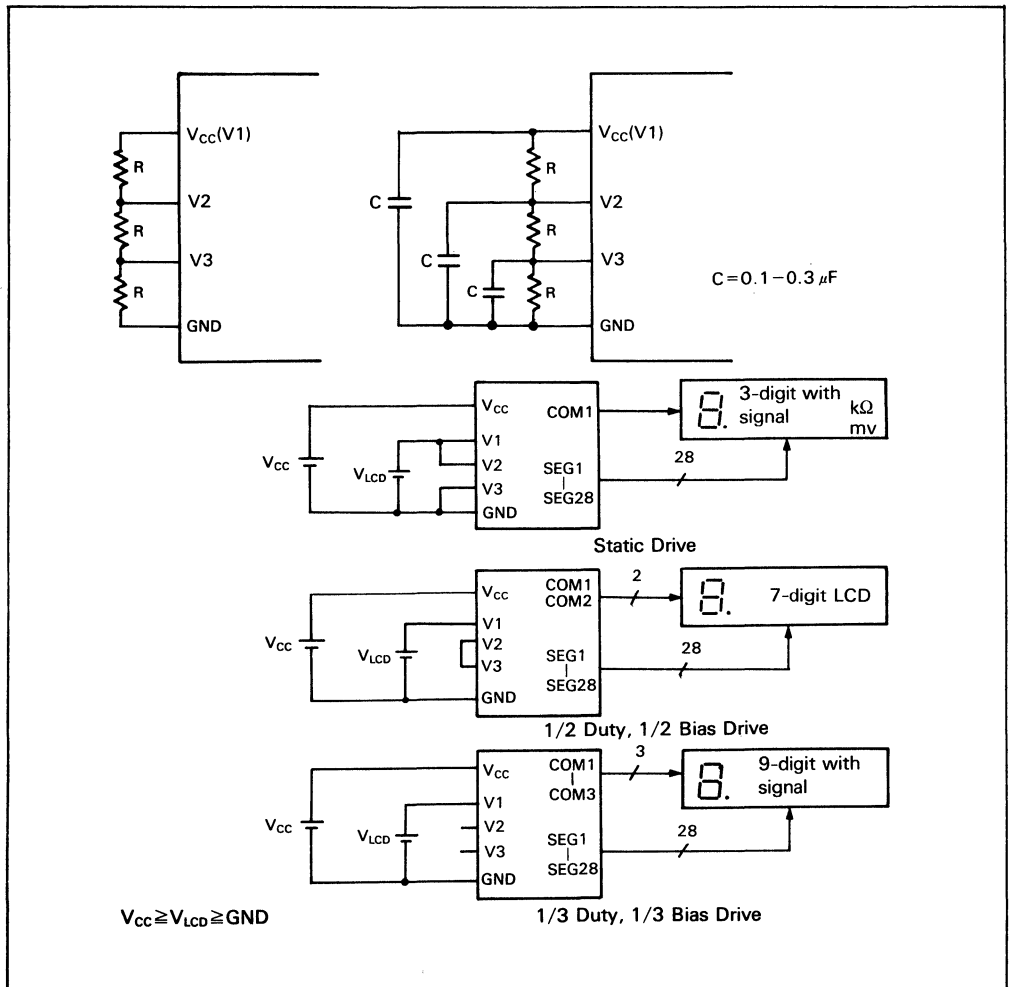


Figure 49. An Example of LCD Connection



Input/Output Port

The MCU has 47 I/O pins comprising 29 I/O pins, 2 input pins, and 16 output pins (multiplexed with SEG pins). The I/O ports (D, R0-R3) have individual data direction registers so that data direction (I/O) can be selected for each bit. Port R4 is an input port. All ports are standard ports. The registers which control the I/O ports of each module are shown in figure 52.

Port D (D₀-D₁₃): The D port is an I/O port composed of 14 I/O pins accessed on a bit basis. All bits of the port D data register are set to 1 by MCU reset. Data direction (input/output) of each pin can be selected by the data direction register provided for each bit (0: input, 1: output). The data direction register is cleared by reset, so that the D port becomes an input port by reset. (See figure 50.) The D port can be set and reset by the SED/RED and SEDD/REDD instructions, and can be tested by the TD/TDD instructions. Pins D₀-D₂ and D₈-D₁₃ are multiplexed with INT₂, INT₃, INT₄, SCK₁, SI₁, SO₁, SCK₂, SI₂, and SO₂, respectively.

Ports R0-R3: These are the I/O ports accessed in 4-bit units. The initial value of the port R data register by MCU reset depends on the value of the data retention bit. When it is 0, register value is 1, when it is 1, the register value before reset is retained. Data direction (input/output) of each bit of port R can be controlled by the port R data direction register (DDR0-DDR3) (0: input, 1: output). Since the data direction register is cleared by reset, the R port becomes an input port by reset. However, when the data retention bit is 1, I/O direction of the R port remains unchanged since the previous data is maintained without being cleared. (See figure 51.)

Data is input as well as output through ports R0-R3 by the LAR and LBR instruction.

Pin R3₂ of port R3 is multiplexed with timer output pin TO₁. TO₁ is an output pin of timer 1, which can output optional frequency clock and PWM output signal utilizing reload function. For details, see section "Timer".

Circuit types of I/O pins are shown in table 13.

Port R4: Port R4 is an input port accessed in 2-bit units. Pin R4₀ is multiplexed with external interrupt input INT₀ and timer input TI₁, and R4₁ is multiplexed with external interrupt input INT₁ and timer input TI₂. Operation mode of each pin is selected by the timer mode register and timer output regis-

ter. (for details, see section "Timer".)

Data is input through port R4 by the LAR and LBR instructions.

Circuit types of the R4 port pins are shown in table 13.

Ports R5-R8: These ports are output ports accessed in 4-bit units. Pins R5₀-R5₃ are multiplexed with SEG28-SEG25; R6₀-R6₃, with SEG24-SEG21; R7₀-R7₃ with SEG20-SEG17; and R8₀-R8₃, with SEG16-SEG13, respectively. Operation mode of each pin is selected by the LCD output register (for details, see section "LCD Circuit").

During reset, these ports are used as R ports and 1 is output. However, when the data retention bit is 1, these pins are not switched to R ports and 1 is not set in the data register, so that the previous data is maintained.

Circuit types of the R5-R8 pins are shown in table 13.

Data Direction Register (\$030-\$033, \$03B-\$03E): The data direction register (DDR) is a 4-bit write-only register which controls input and output of the I/O ports. Each I/O port bit has a DDR and data direction can be selected on a bit basis. Data is input from each pin when a port is an input port. For an output port, data is accessed from the data register.

The I/O ports become input ports when DDR is cleared by reset. However, the R port data direction register is not cleared by reset when the data retention bit is 1, so that the previous data is retained.

D port data direction register (DDR0: \$03B, DDR1: \$03C, DDR2: \$03D, DDR3: \$03E): This register can select D port data direction on a bit basis. RAM bit manipulation instruction cannot be used. The D port becomes an input port by reset (figure 50).

R port data direction register (DDR0: \$030, DDR1: \$031, DDR2: \$032, DDR3: \$033): This register can select data direction for ports R0-R3 on a bit basis. RAM bit manipulation instruction cannot be used. When the R port data direction register is cleared by MCU reset, the R ports become input ports. However, if the data retention bit is 1, this register is not cleared by reset and the previous data is retained (figure 51).

Note: I/O pins unused on the user system.

If unused I/O pins are left floating, the LSI may malfunction because of noise. To prevent this, unused pins should be pulled up to V_{CC} through a resistor of approximately 100 kΩ.

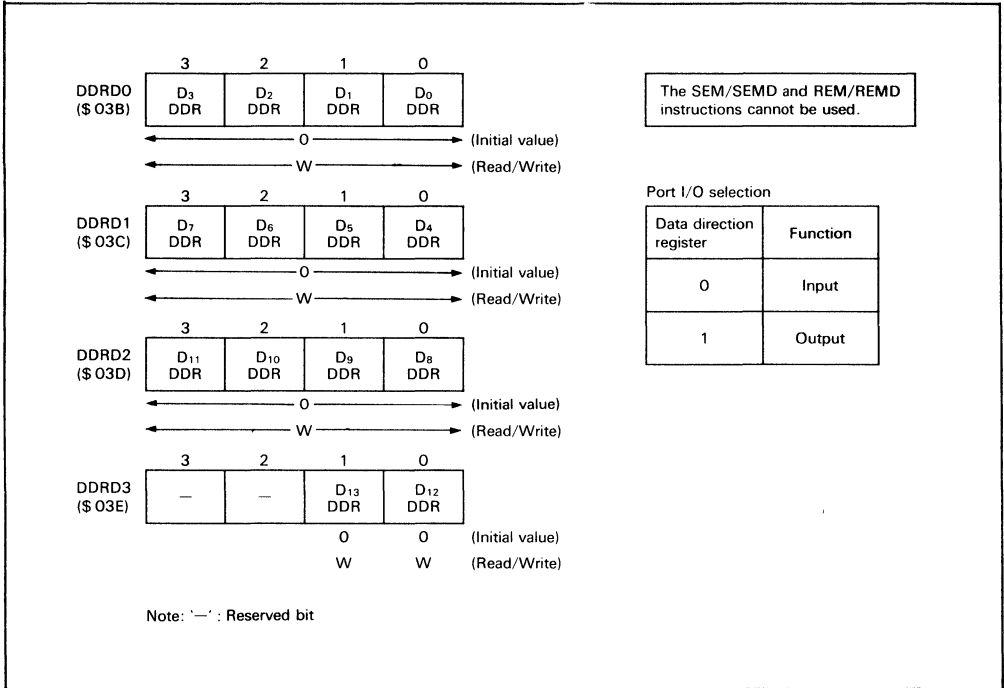


Figure 50. D Port Data Direction Register

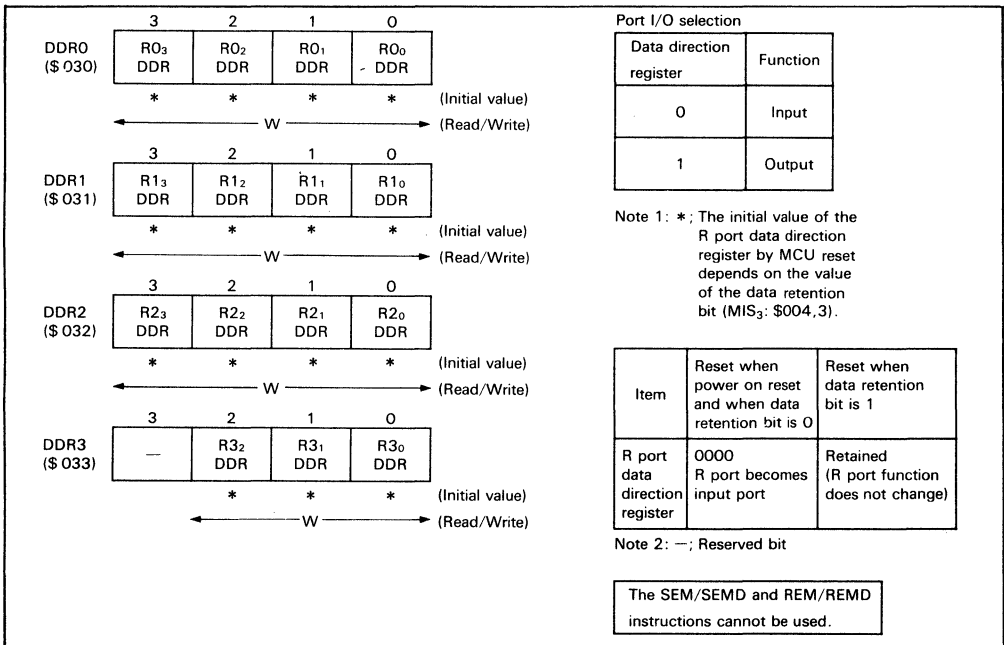


Figure 51. R Port Data Direction Register



Table 13. Circuit Type of I/O Pins

I/O Pins	Circuit Type	Applied Pins
<p>I/O common pin</p>		<p>D₀-D₁₃</p>
		<p>R₀-R₃</p>
		<p>$\overline{SCK}_1, \overline{SCK}_2$</p>
<p>Output pin</p>		<p>R₅-R₈</p>
		<p>SO₁, SO₂, TO₁ (STOP="1")</p>
<p>Input pin</p>		<p>R₄</p>
		<p>$\overline{INT}_0, \overline{INT}_1, \overline{INT}_2$ $\overline{INT}_3, \overline{INT}_4, SI_1$ SI₂, TI₁, TI₂</p>

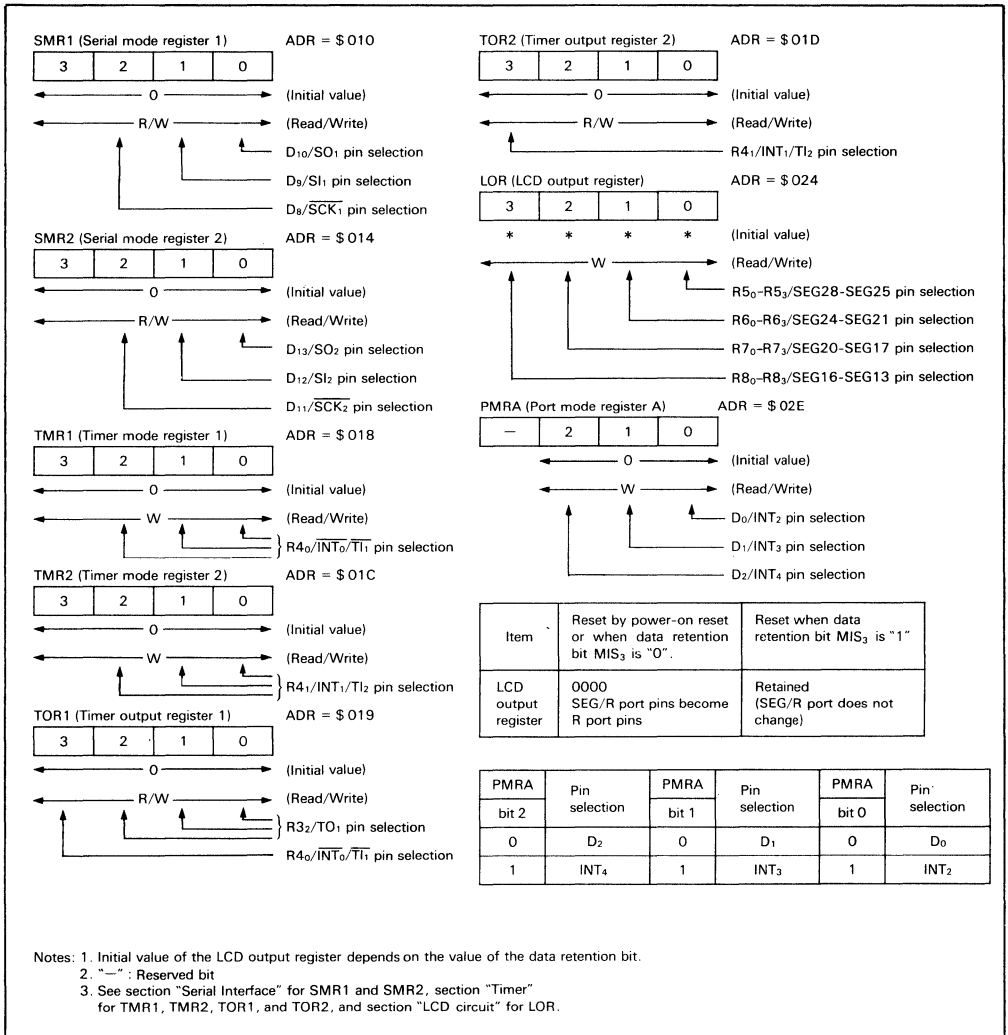


Figure 52. I/O Mode Selection Registers

Oscillation Circuit

The oscillation circuit configuration is shown in figure 53.

Figure 54 shows an internal oscillation circuit block diagram. 4.5 MHz crystal should be attached.

Figure 55 is an example of a crystal oscillation circuit, and its layout example is shown in figure 56.

- Notes: 1. The circuit parameters are changed by crystal resonator and the floating capacitance in the board. In employing a resonator, please consult with the engineers of the crystal maker to determine the actual circuit parameter.
2. Wiring between OSC1, OSC2, and elements should be as short as possible, and never cross other wires. (See figure 56.)

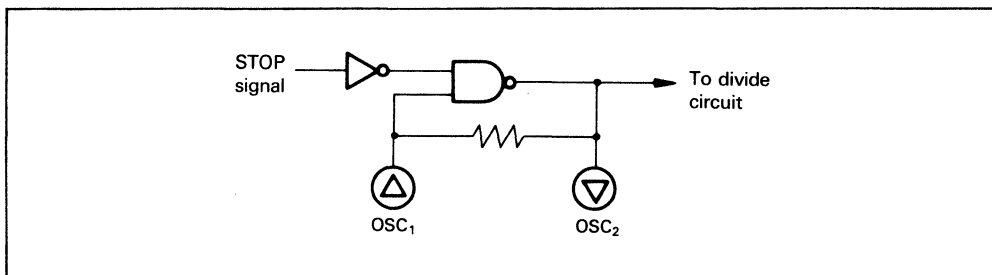


Figure 53. Oscillator

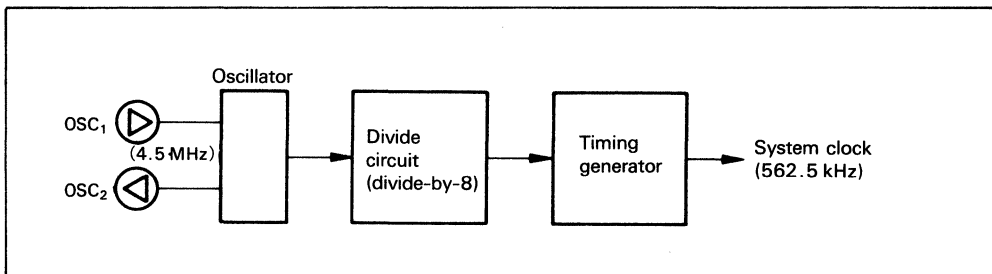


Figure 54. Internal Oscillation Circuit

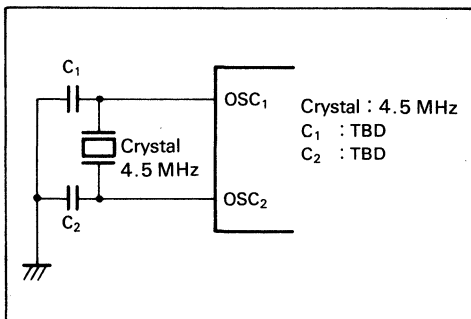


Figure 55. Crystal Oscillation Circuit

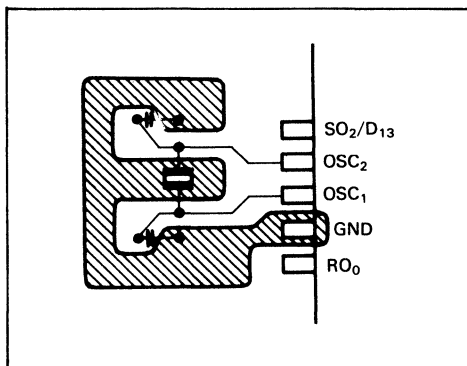


Figure 56. Crystal Oscillation Circuit Layout

Miscellaneous Register

The function of the miscellaneous register, shown in figure 57, is described below.

RESET: The RESET pin level can be read by reading the MIS₀ bit.

Data retention bit: This bit is cleared if V_{CC} voltage supply stops. This bit is set before the MCU enters into stop mode. Then, if this bit is set when the MCU recovers from stop mode by MCU reset, V_{CC} voltage is applied during stop mode and RAM data is retained.

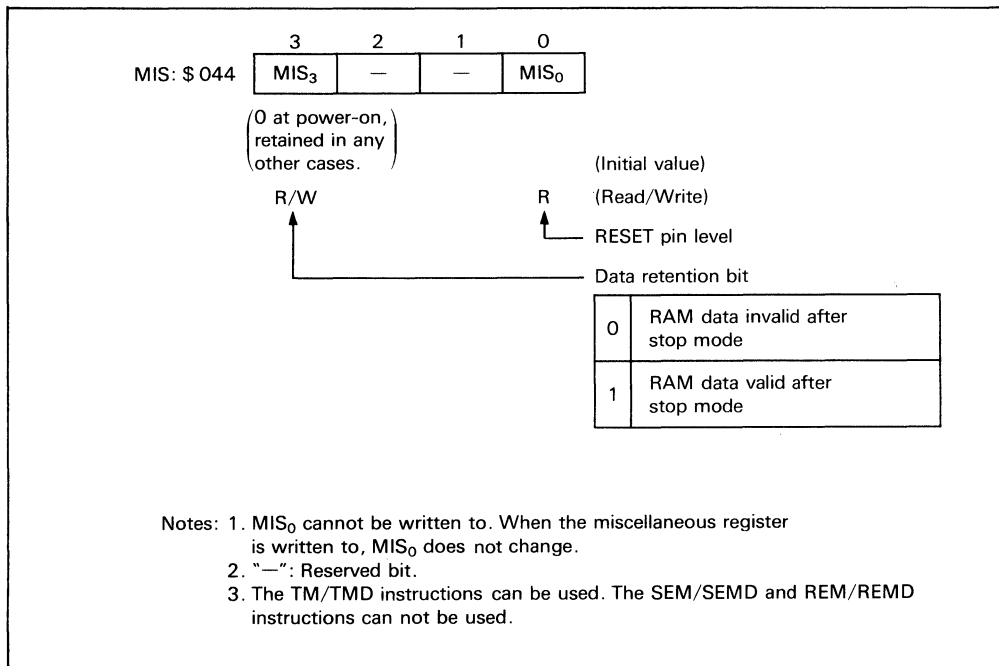


Figure 57. Miscellaneous Register

PROM Mode Pin Description

The HD4074509 is a ZTAT microcomputer incorporating PROM. When the MCU enters PROM mode, the MCU stops to program the

PROM. PROM mode signals are listed in table 14, and PROM mode pin assignment is in figure 58.

Table 14. PROM Mode Signals

MCU mode			PROM mode		MCU mode			PROM mode	
Pin No.	Pin name	I/O	Pin name	I/O	Pin No.	Pin name	I/O	Pin name	I/O
1	AN ₀	I	M ₀	I	41	R2 ₂	I/O	A ₁₁	I
2	V1				42	R2 ₃	I/O	A ₁₂	I
3	V2				43	R3 ₀	I/O	A ₁₃	I
4	V3				44	R3 ₁	I/O	A ₁₄	I
5	IF	I			45	R3 ₂ /TO ₁	I/O		
6	TEST	I	TEST	I	46	R4 ₀ /INT ₀ /TI ₁	I	V _{PP}	
7	φ ₁	O			47	R4 ₁ /INT ₁ /TI ₂	I	A ₉	I
8	φ ₂	O			48	V _{CC}		V _{CC}	
9	V _{CC} (PLL)		V _{CC}		49	SEG1	O	O ₀	I/O
10	PLL(D)	I			50	SEG2	O	O ₁	I/O
11	PLL(P)	I			51	SEG3	O	O ₂	I/O
12	RESET	I	RESET	I	52	SEG4	O	O ₃	I/O
13	GND (PLL)		GND		53	SEG5	O	O ₄	I/O
14	INT ₂ /D ₀	I/O	O ₀	I/O	54	SEG6	O	V _{CC}	
15	INT ₃ /D ₁	I/O	O ₁	I/O	55	SEG7	O		
16	INT ₄ /D ₂	I/O	O ₂	I/O	56	SEG8	O		
17	D ₃	I/O	O ₃	I/O	57	SEG9	O		
18	D ₄	I/O	O ₄	I/O	58	SEG10	O		
19	D ₅	I/O	O ₅	I/O	59	SEG11	O		
20	D ₆	I/O	O ₆	I/O	60	SEG12	O		
21	D ₇	I/O	O ₇	I/O	61	SEG13/R8 ₃	O		
22	SCK ₁ /D ₈	I/O	OE	I	62	SEG14/R8 ₂	O		
23	SI ₁ /D ₉	I/O	CE	I	63	SEG15/R8 ₁	O		
24	SO ₁ /D ₁₀	I/O	V _{CC}		64	SEG16/R8 ₀	O		
25	SCK ₂ /D ₁₁	I/O	V _{CC}		65	SEG17/R7 ₃	O		
26	SI ₂ /D ₁₂	I/O			66	SEG18/R7 ₂	O		
27	SO ₂ /D ₁₃	I/O			67	SEG19/R7 ₁	O		
28	OSC ₂	O			68	SEG20/R7 ₀	O		
29	OSC ₁	I			69	SEG21/R6 ₃	O		
30	GND		GND		70	SEG22/R6 ₂	O		
31	RO ₀	I/O	A ₁	I	71	SEG23/R6 ₁	O		
32	RO ₁	I/O	A ₂	I	72	SEG24/R6 ₀	O		
33	RO ₂	I/O	A ₃	I	73	SEG25/R5 ₃	O		
34	RO ₃	I/O	A ₄	I	74	SEG26/R5 ₂	O		
35	R1 ₀	I/O	A ₅	I	75	SEG27/R5 ₁	O		
36	R1 ₁	I/O	A ₆	I	76	SEG28/R5 ₀	O		
37	R1 ₂	I/O	A ₇	I	77	COM1	O		
38	R1 ₃	I/O	A ₈	I	78	COM2	O		
39	R2 ₀	I/O	A ₀	I	79	COM3	O		
40	R2 ₁	I/O	A ₁₀	I	80	AN ₁	I	M ₁	I

- Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin
 2. Pins O₀ to O₄ each have two pins. Each pair must be closed when using.



Pins for PROM mode

V_{PP} : V_{PP} applies program voltage ($12.5\text{ V} \pm 0.3\text{ V}$).

\overline{CE} : \overline{CE} inputs the control signal which enables PROM programming and verifying.

\overline{OE} : \overline{OE} inputs the data output control signal for verify.

A_0 - A_{14} : These are the address input pins of on-chip PROM.

O_0 - O_7 : These are the data I/O pins of on-chip PROM.

$\overline{M_0}$, $\overline{M_1}$: These are used for setting PROM mode. PROM mode is set by bringing $\overline{M_0}$, $\overline{M_1}$, and TEST pins to low and RESET pin to high.

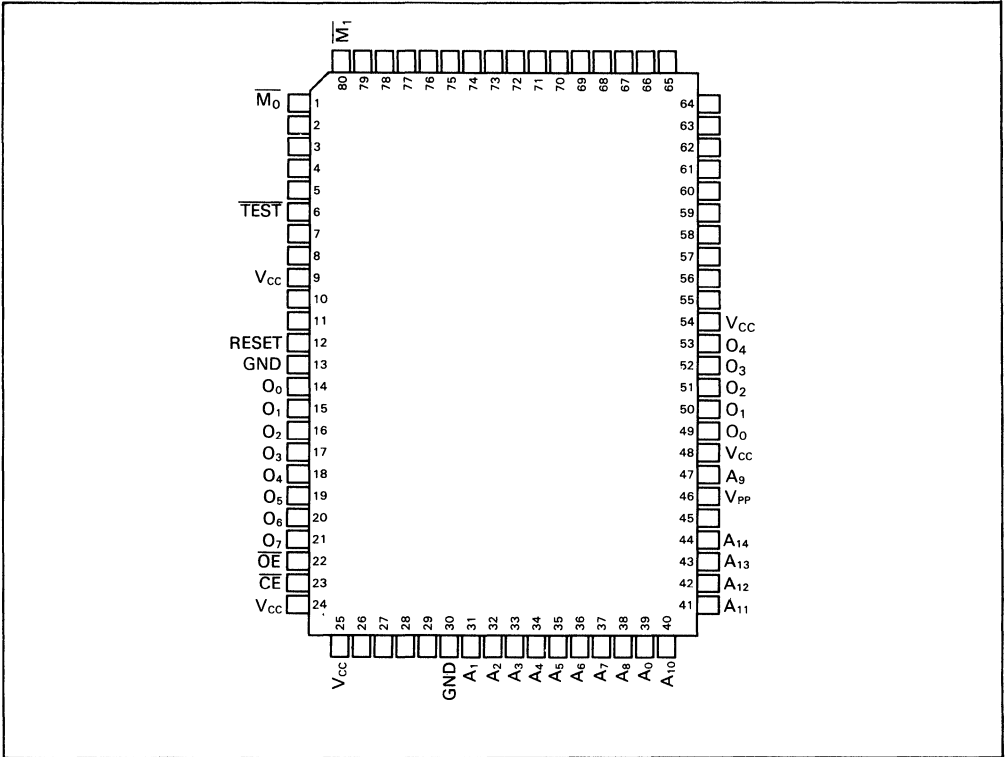


Figure 58. Pin Arrangement in PROM Mode

Programmable ROM Programming

The MCU enters into PROM mode by setting TEST, \overline{M}_0 , \overline{M}_1 , to low, and RESET pin to high (figure 59).

The specification of the on-chip PROM is the same as that of EPROM 27256. It can be programmed by the standard PROM programmer using a 80-to-28 pin socket adapter. In order to program the PROM using a general-purpose PROM programmer, the HD4074509 incorporates the conversion circuit which divides a 10-bit HMCS400 series instruction into 5 higher bits and 5 lower bits as shown in figure 60. One MCU address is assigned to two PROM addresses. For example, in programming an 16 k word PROM with a general-purpose PROM programmer, the user should assign 32 kbyte address locations (\$0000-\$7FFF).

Precautions

1. Addresses \$0000 to \$7FFF should be specified if the PROM is programmed by the PROM programmer. If addresses of \$8000 or higher is accessed, the PROM

may not be programmed or verified. Note that the plastic package type cannot be erased and reprogrammed. Unused address data must be set to \$FF.

2. Be careful that an index of the PROM programmer socket, socket adapter, and LSI match. Using the wrong programmer of socket adapter may cause an over-voltage and damage the LSI. Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed in the programmer.
3. The PROM should be programmed with $V_{PP} = 12.5$ V. Other PROMs also use 21 V. If 21 V is applied to the HD4074509, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP} .

Programming and verification

The HD4074509 can accomplish high-speed programming without causing voltage stress or degrading data reliability. The flowchart is shown in figure 61. For details, see "Characteristics and Applications of PROM".

Table 15. Mode Selection

Mode	Pin			
	\overline{CE}	\overline{OE}	V_{PP}	O_0-O_7
Programming	Low	High	V_{PP}	Data input
Verify	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 16. PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapters	
Maker	Type name	Maker	Type name
DATA I/O	22 B 29 B	Hitachi	HS450ESF01H
AVAL Corp	PKW-1000 PKW-7000	Hitachi	HS450ESF01H

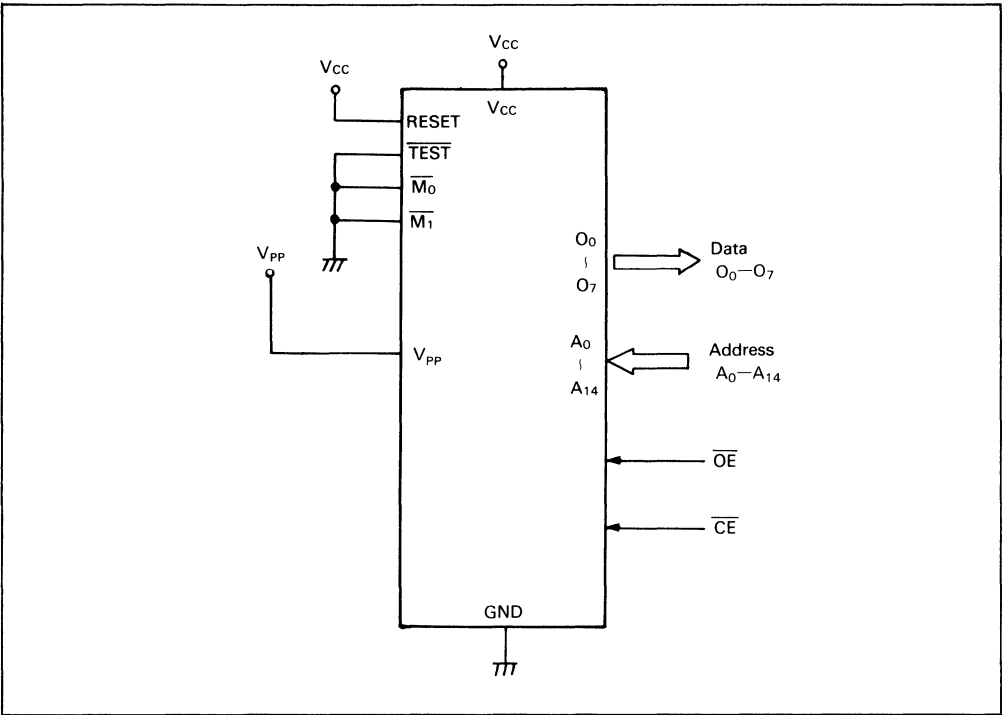


Figure 59. PROM Mode

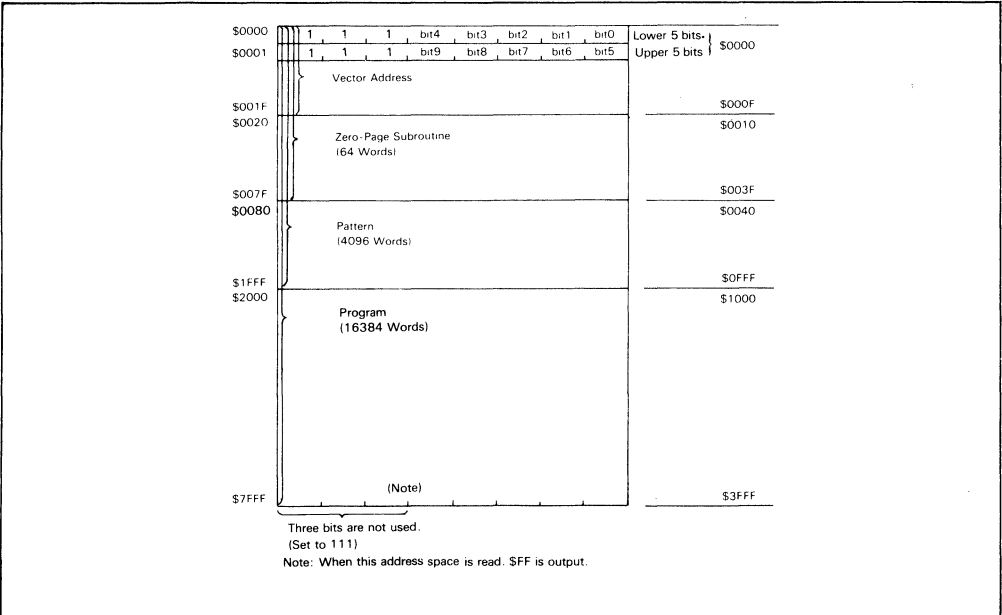


Figure 60. PROM Mode Memory Map



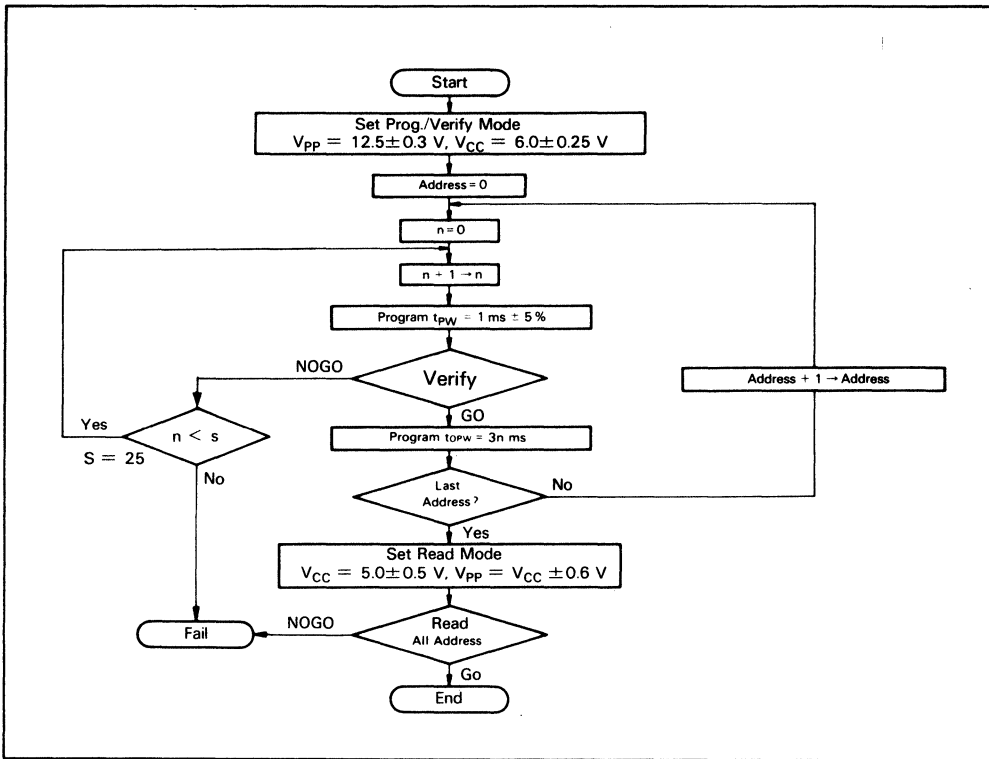


Figure 61. A Sequence of High Speed Programming

Characteristics and Applications of PROM

Principles of Programming/Erasing

The configuration of the ZTAT micros' memory cells are the same as that of an EPROM's (figure 62). Therefore they are programmed by applying high voltage to control gates and drains, which injects hot electrons into the floating gate. The stored electrons become stable since they are surrounded by an energy barrier of SiO₂ film. Such a cell becomes a 0 bit due to the memory threshold voltage change. A cell with so condensed electrons at its floating gate appears as a 1 bit.

The electron charge in memory cells may decrease as time goes by. This can be caused by:

- ① Ultraviolet light, discharged by photo-emitting electrons (erasure principle)
- ② Heat, discharged by thermal emitting electrons
- ③ High voltage, discharged by a high electric field at the control gate or drain

If the oxide film covering a floating gate is defective, the erasure rate is great. Normally, electron erasure does not occur, because such defective devices are found and removed during testing.

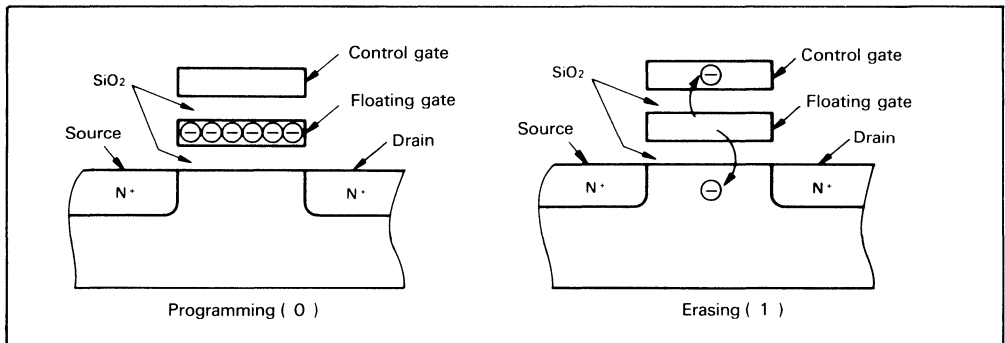


Figure 62. Cross-section of PROM Memory Cell

Programming precautions

The PROM memory cells should be programmed under specific voltage and timing conditions. The higher the program voltage and the longer the program pulse is applied, the more electrons will be injected into the floating gate. However, if an overvoltage is applied to V_{PP} , the p-n junction may be permanently damaged. Pay particular attention to PROM programmer overshoot. Negative voltage noise will cause a parasitic transistor effect, which may reduce break-down voltage.

The ZTAT micros are connected electrically to the PROM programmer through a socket adapter. Therefore, pay attention to the followings:

- ① Confirm that the socket adapter is firmly fixed on the PROM programmer.

- ② Do not touch the socket adapter or the LSI during programming. Misprogramming can be caused by poor contacts.

On-chip PROM reliability after programming

Generally, semiconductors are reliable except for initial failures. To avoid failures, screening can be performed. Exposure to high temperature is a kind of screening which removes PROM memory cells with data hold failures in a short time. This is done to the ZTATs in the wafer stage, so ZTAT data hold characteristics are high. Exposing the LSI to 150 °C after user programming can effectively upgrade these characteristics. Figure 63 shows the recommended screening flow.

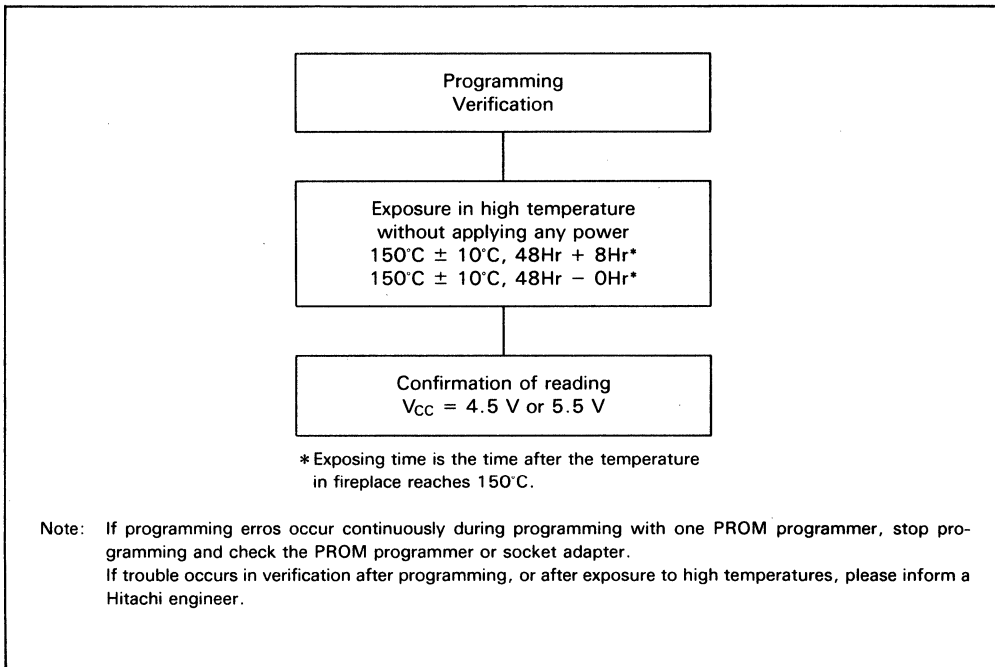


Figure 63. Recommended Screening Flow

RAM Addressing Mode

As shown in figure 64, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing: Contents of registers W, X, and Y (10 bits) are used as the RAM address.

Direct Addressing: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing: The memory register (16 addresses; from \$040 to \$04F) is accessed by executing the LAMR and XMRA instructions.

ROM Addressing Mode and P Instructions

The MCU has four ROM addressing modes, as shown in figure 65.

Direct Addressing Mode: The program can branch to any address in the ROM memory space by executing a JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC₁₃ to PC₀) with the 14-bit immediate data.

Current Page Addressing Mode: A page is 256 words. By executing a BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order eight bits of the program counter (PC₇ to PC₀) with the 8-bit immediate data.

When BR instruction is on a page boundary (256n + 255) (figure 67), executing a BR instruction transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when BR is used on a page boundary. The HMCS400-series cross macro assembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing a CAL instruction, the program can branch to the zero-page subroutine area, which is located at \$0000-\$003F. When a CAL instruction is executed, 6 bits of immediate data are placed in the low-order 6 bits of the program counter (PC₅ to PC₀) and 0s are placed in the high-order 8 bits (PC₁₃ to PC₆).

Table Data Addressing: By executing a TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and register B.

P Instruction: ROM data accessed by table data addressing can be referred to by a P instruction (figure 66). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and register B. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port data registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and register B and also to the R1 and R2 port data registers at the same time.

The P instruction has no effect on the program counter.

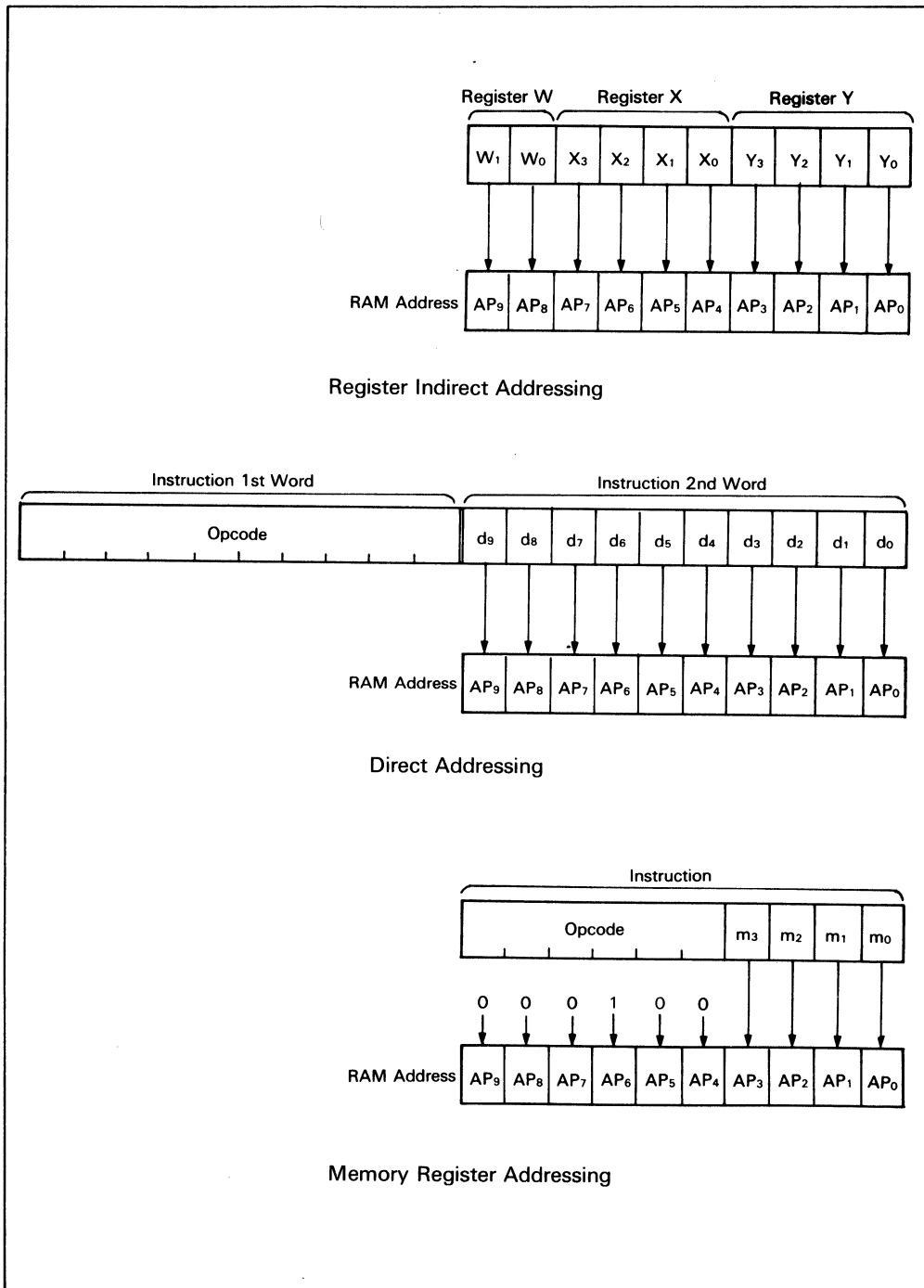


Figure 64. RAM Addressing Modes



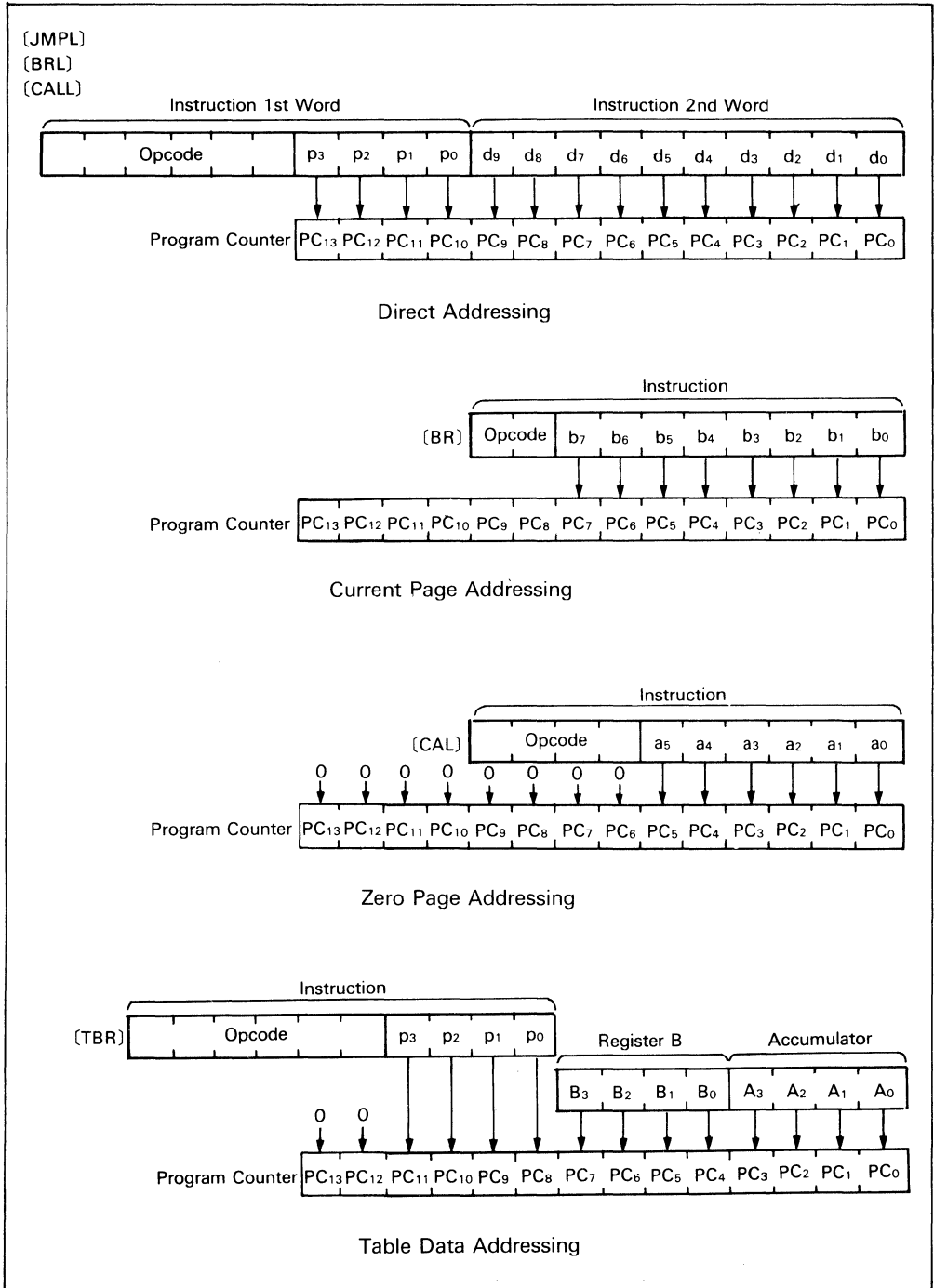
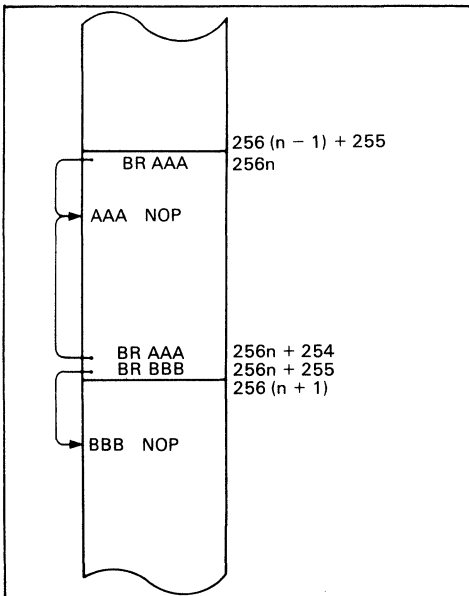
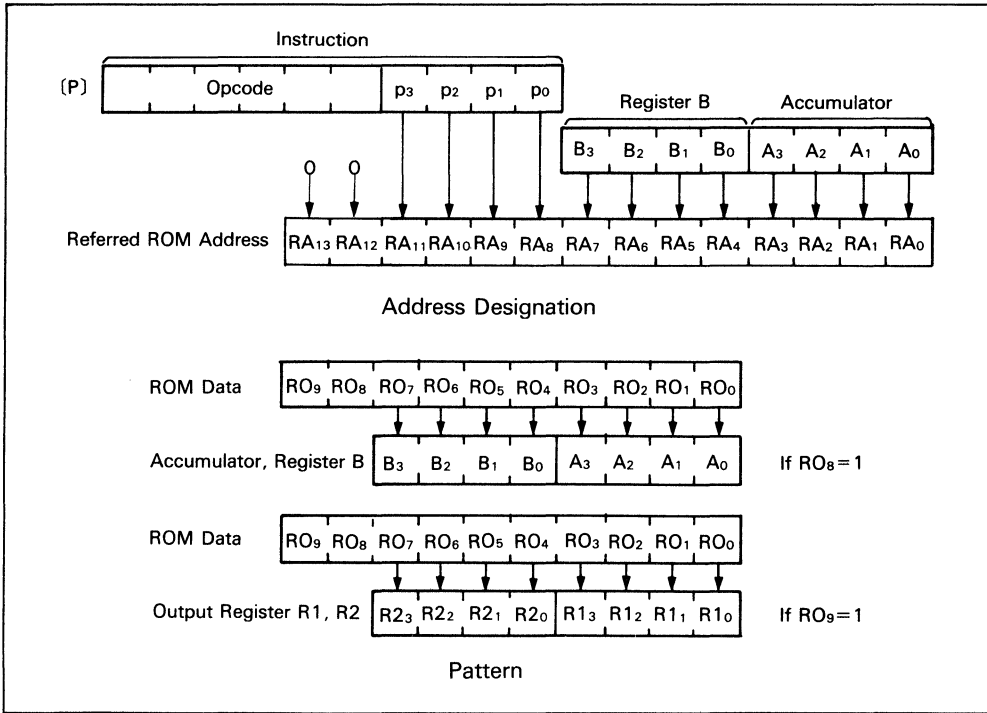


Figure 65. ROM Addressing Mode



Instruction Set

The MCU provides 101 instructions which are classified into 10 groups as follows:

1. Immediate instructions
2. Register-to-register instructions
3. RAM address instructions
4. RAM-register instructions
5. Arithmetic instructions
6. Compare instructions
7. RAM bit manipulation instructions
8. ROM address instructions
9. Input/output instructions
10. Control instructions

Tables 17-26 list their functions, and table 27 is an opcode map.

Table 17. Immediate Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Immediate	LAI i	1 0 0 0 1 1 i ₃ i ₂ i ₁ i ₀	i · A		1/1
Load B from Immediate	LBI i	1 0 0 0 0 0 i ₃ i ₂ i ₁ i ₀	i · B		1/1
Load Memory from Immediate	LMID i,d	0 1 1 0 1 0 i ₃ i ₂ i ₁ i ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	i · M		2/2
Load Memory from Immediate, Increment Y	LMIIY i	1 0 1 0 0 1 i ₃ i ₂ i ₁ i ₀	i · M, Y+1 · Y	NZ	1/1

Table 18. Register-to-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from B	LAB	0 0 0 1 0 0 1 0 0 0	B · A		1/1
Load B from A	LBA	0 0 1 1 0 0 1 0 0 0	A · B		1/1
Load A from W	LAW	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	W · A		2/2 (Note)
Load A from Y	LAY	0 0 1 0 1 0 1 1 1 1	Y · A		1/1
Load A from SPX	LASPX	0 0 0 1 1 0 1 0 0 0	SPX · A		1/1
Load A from SPY	LASPY	0 0 0 1 0 1 1 0 0 0	SPY · A		1/1
Load A from MR	LAMR m	1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) · A		1/1
Exchange MR and A	XMRA m	1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀	MR(m) ·· A		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by assembler.



Table 19. RAM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load W from Immediate	LWI i	0 0 1 1 1 1 0 0 $i_1 i_0$	$i \rightarrow W$		1/1
Load X from Immediate	LXI i	1 0 0 0 1 0 $i_3 i_2 i_1 i_0$	$i \rightarrow X$		1/1
Load Y from Immediate	LYI i	1 0 0 0 0 1 $i_3 i_2 i_1 i_0$	$i \rightarrow Y$		1/1
Load W from A	LWA	0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$A \rightarrow W$		2/2 (Note)
Load X from A	LXA	0 0 1 1 1 0 1 0 0 0	$A \rightarrow X$		1/1
Load Y from A	LYA	0 0 1 1 0 1 1 0 0 0	$A \rightarrow Y$		1/1
Increment Y	IY	0 0 0 1 0 1 1 1 0 0	$Y+1 \rightarrow Y$	NZ	1/1
Decrement Y	DY	0 0 1 1 0 1 1 1 1 1	$Y-1 \rightarrow Y$	NB	1/1
Add A to Y	AYY	0 0 0 1 0 1 0 1 0 0	$Y+A \rightarrow Y$	OVF	1/1
Subtract A from Y	SY Y	0 0 1 1 0 1 0 1 0 0	$Y-A \rightarrow Y$	NB	1/1
Exchange X and SPX	XSPX	0 0 0 0 0 0 0 0 0 1	$X \leftrightarrow SPX$		1/1
Exchange Y and SPY	XSPY	0 0 0 0 0 0 0 0 1 0	$Y \leftrightarrow SPY$		1/1
Exchange X and SPX, Y and SPY	XSPXY	0 0 0 0 0 0 0 0 1 1	$X \leftrightarrow SPX, Y \leftrightarrow SPY$		1/1

Note: An operand is automatically provided for the second word of LAW and LWA instruction by the assembler.

Table 20. RAM-Register Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Load A from Memory	LAM(XY)	0 0 1 0 0 1 0 0 y x	M ← A, (X←SPX, Y←SPY)		1/1
Load A from Memory	LAMD d	0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ← A		2/2
Load B from Memory	LBM(XY)	0 0 0 1 0 0 0 0 y x	M ← B, (X←SPX, Y←SPY)		1/1
Load Memory from A	LMA(XY)	0 0 1 0 0 1 0 1 y x	A ← M, (X←SPX, Y←SPY)		1/1
Load Memory from A	LMAD d	0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	A ← M		2/2
Load Memory from A, Increment Y	LMAIY(X)	0 0 0 1 0 1 0 0 0 x	A ← M, Y+1 ·Y (X←SPX)	NZ	1/1
Load Memory from A, Decrement Y	LMADY(X)	0 0 1 1 0 1 0 0 0 x	A ← M, Y-1 ·Y (X←SPX)	NB	1/1
Exchange Memory and A	XMA(XY)	0 0 1 0 0 0 0 0 y x	M ↔ A, (X←SPX, Y←SPY)		1/1
Exchange Memory and A	XMAD d	0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	M ↔ A		2/2
Exchange Memory and B	XMB(XY)	0 0 1 1 0 0 0 0 y x	M ↔ B, (X←SPX, Y←SPY)		1/1

Note: (XY) and (X) have the following meaning:

- (1) The instructions with (XY) have 4 mnemonics and 4 object codes for each (example of LAM (XY) is given below).
The op-code X or Y is assembled as follows:

Mnemonic	Y	X	Function
LAM	0	0	
LAMX	0	1	X ← SPX
LAMY	1	0	Y ← SPY
LAMXY	1	1	X←SPX, Y←SPY

- (2) The instructions with (X) have 2 mnemonics and 2 object codes for each (example of LMAIY(X) is given below).
The op-code X is assembled as follows:

Mnemonic	X	Function
LMAIY	0	
LMAIYX	1	X ← SPX

Table 21. Arithmetic Instructions

Operation	Mnemonic	Operation Code	Function	Words/	
				Status	Cycles
Add Immediate to A	AI i	1 0 1 0 0 0 i ₃ i ₂ i ₁ i ₀	$A + i \rightarrow A$	OVF	1/1
Increment B	IB	0 0 0 1 0 0 1 1 0 0	$B + 1 \rightarrow B$	NZ	1/1
Decrement B	DB	0 0 1 1 0 0 1 1 1 1	$B - 1 \rightarrow B$	NB	1/1
Decimal Adjust for Addition	DAA	0 0 1 0 1 0 0 1 1 0			1/1
Decimal Adjust for Subtraction	DAS	0 0 1 0 1 0 1 0 1 0			1/1
Negate A	NEGA	0 0 0 1 1 0 0 0 0 0	$\bar{A} + 1 \rightarrow A$		1/1
Complement B	COMB	0 1 0 1 0 0 0 0 0 0	$\bar{B} \rightarrow B$		1/1
Rotate Right A with Carry	ROTR	0 0 1 0 1 0 0 0 0 0			1/1
Rotate Left A with Carry	ROTL	0 0 1 0 1 0 0 0 0 1			1/1
Set Carry	SEC	0 0 1 1 1 0 1 1 1 1	$1 \rightarrow CA$		1/1
Reset Carry	REC	0 0 1 1 1 0 1 1 0 0	$0 \rightarrow CA$		1/1
Test Carry	TC	0 0 0 1 1 0 1 1 1 1		CA	1/1
Add A to Memory	AM	0 0 0 0 0 0 1 0 0 0	$M + A \rightarrow A$	OVF	1/1
Add A to Memory	AMD d	0 1 0 0 0 0 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A \rightarrow A$	OVF	2/2
Add A to Memory with Carry	AMC	0 0 0 0 0 1 1 0 0 0	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	1/1
Add A to Memory with Carry	AMCD d	0 1 0 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M + A + CA \rightarrow A$ $OVF \rightarrow CA$	OVF	2/2
Subtract A from Memory with Carry	SMC	0 0 1 0 0 1 1 0 0 0	$M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	1/1
Subtract A from Memory with Carry	SMCD d	0 1 1 0 0 1 1 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$	NB	2/2
OR A and B	OR	0 1 0 1 0 0 0 1 0 0	$A \cup B \rightarrow A$		1/1
AND Memory with A	ANM	0 0 1 0 0 1 1 1 0 0	$A \cap M \rightarrow A$	NZ	1/1
AND Memory with A	ANMD d	0 1 1 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cap M \rightarrow A$	NZ	2/2
OR Memory with A	ORM	0 0 0 0 0 0 1 1 0 0	$A \cup M \rightarrow A$	NZ	1/1
OR Memory with A	ORMD d	0 1 0 0 0 0 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \cup M \rightarrow A$	NZ	2/2
EOR Memory with A	EORM	0 0 0 0 0 1 1 1 0 0	$A \oplus M \rightarrow A$	NZ	1/1
EOR Memory with A	EORMD d	0 1 0 0 0 1 1 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	$A \oplus M \rightarrow A$	NZ	2/2

Note: \cap : Logical AND
 \cup : Logical OR
 \oplus : Exclusive OR



Table 22. Compare Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Immediate Not Equal to Memory	INEM i	0 0 0 0 1 0 i_3 i_2 i_1 i_0	$i \neq M$	NZ	1/1
Immediate Not Equal to Memory	INEMD i,d	0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \neq M$	NZ	2/2
A Not Equal to Memory	ANEM	0 0 0 0 0 0 0 1 0 0	$A \neq M$	NZ	1/1
A Not Equal to Memory	ANEMD d	0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \neq M$	NZ	2/2
B Not Equal to Memory	BNEM	0 0 0 1 0 0 0 1 0 0	$B \neq M$	NZ	1/1
Y Not Equal to Immediate	YNEI i	0 0 0 1 1 1 i_3 i_2 i_1 i_0	$Y \neq i$	NZ	1/1
Immediate Less or Equal to Memory	ILEM i	0 0 0 0 1 1 i_3 i_2 i_1 i_0	$i \leq M$	NB	1/1
Immediate Less or Equal to Memory	ILEMD i,d	0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$i \leq M$	NB	2/2
A Less or Equal to Memory	ALEM	0 0 0 0 0 1 0 1 0 0	$A \leq M$	NB	1/1
A Less or Equal to Memory	ALEMD d	0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$A \leq M$	NB	2/2
B Less or Equal to Memory	BLEM	0 0 1 1 0 0 0 1 0 0	$B \leq M$	NB	1/1
A Less or Equal to Immediate	ALEI i	1 0 1 0 1 1 i_3 i_2 i_1 i_0	$A \leq i$	NB	1/1

Table 23. RAM Bit Manipulation Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Memory Bit	SEM n	0 0 1 0 0 0 0 1 n_1 n_0	$1 \cdot M(n)$		1/1
Set Memory Bit	SEMD n,d	0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$1 \cdot M(n)$		2/2
Reset Memory Bit	REM n	0 0 1 0 0 0 1 0 n_1 n_0	$0 \cdot M(n)$		1/1
Reset Memory Bit	REMD n,d	0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0	$0 \cdot M(n)$		2/2
Test Memory Bit	TM n	0 0 1 0 0 0 1 1 n_1 n_0		$M(n)$	1/1
Test Memory Bit	TMD n,d	0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0		$M(n)$	2/2



Table 24. ROM Address Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Branch on Status 1	BR b	1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀		1	1/1
Long Branch on Status 1	BRL u	0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Long Jump Unconditionally	JMPL u	0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀			2/2
Subroutine Jump on Status 1	CAL a	0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀		1	1/2
Long Subroutine Jump on Status 1	CALL u	0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀		1	2/2
Table Branch	TBR p	0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/1
Return from Subroutine	RTN	0 0 0 0 0 1 0 0 0 0			1/3
Return from Interrupt	RTNI	0 0 0 0 0 1 0 0 0 1	1 → I/E CA Restore	ST	1/3

Table 25. Input/Output Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
Set Discrete I/O Latch	SED	0 0 1 1 1 0 0 1 0 0	1 → D(Y)		1/1
Set Discrete I/O Latch Direct	SEDD m	1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀	1 → D(m)		1/1
Reset Discrete I/O Latch	RED	0 0 0 1 1 0 0 1 0 0	0 → D(Y)		1/1
Reset Discrete I/O Latch Direct	REDD m	1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀	0 → D(m)		1/1
Test Discrete I/O Latch	TD	0 0 1 1 1 0 0 0 0 0		D(Y)	1/1
Test Discrete I/O Latch Direct	TDD m	1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀		D(m)	1/1
Load A from R Port Register	LAR m	1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀	R(m) → A		1/1
Load B from R Port Register	LBR m	1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀	R(m) → B		1/1
Load R Port Register from A	LRA m	1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀	A → R(m)		1/1
Load R Port Register from B	LRB m	1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀	B → R(m)		1/1
Pattern Generation	P p	0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀			1/2

Table 26. Control Instructions

Operation	Mnemonic	Operation Code	Function	Status	Words/ Cycles
No Operation	NOP	0 0 0 0 0 0 0 0 0 0			1/1
Start Serial	STS	0 1 0 1 0 0 1 0 0 0			1/1
Standby Mode	SBY	0 1 0 1 0 0 1 1 0 0			1/1
Stop Mode	STOP	0 1 0 1 0 0 1 1 0 1			1/1



Absolute Maximum Ratings

Item	Symbol	Constant	Unit	Notes
Supply Voltage	V_{CC}	-0.3 to + 7.0	V	
Programming Voltage	V_{PP}	-0.3 to + 14.0	V	2, 8
Terminal Voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	
Total Allowance of Input Current	ΣI_O	50	mA	3
Total Allowance of Output Current	$-\Sigma I_O$	50	mA	4
Maximum Input Current	I_O	4	mA	5, 7
Maximum Output Current	$-I_O$	4	mA	6, 7
Operating Temperature	T_{opr}	-40 to + 85	°C	
Storage Temperature	T_{stg}	-55 to + 125	°C	
Storage Temperature (bias)	T_{bias}	-45 to +90	°C	8

- Notes:
1. Permanent damage may occur if absolute maximum ratings are exceeded. Normal operation should be under the conditions of electrical characteristics. If these conditions are exceeded, it may cause a malfunction or affect the reliability of LSI.
 2. $R4_O/INT_O/TI_1$ (V_{PP})
 3. Total allowance of input current is the total sum of input current which flows in from all I/O pins to GND simultaneously.
 4. Total allowance of output current is the total sum of the output current which flows out from V_{CC} to all I/O pins simultaneously.
 5. Maximum input current is the maximum amount of input current from each I/O pin to GND.
 6. Maximum output current is the maximum amount of output current from V_{CC} to each I/O pin.
 7. R0-R3, R5-R8, D0-D13, $\phi 1$, $\phi 2$.
 8. Applied for the HD4074509.

Electrical Characteristics

DC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -40\text{ to } +85^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	RESET, INT ₀ , INT ₁ , INT ₂ , INT ₃ , INT ₄ , $\overline{TI_1}$, $\overline{TI_2}$, $\overline{SCK_1}$, SCK ₂ , SI ₁ , SI ₂	0.8 V_{CC}		$V_{CC} + 0.3$	V		
Input low Voltage	V_{IL}		- 0.3		0.2 V_{CC}	V		
Output High Voltage	V_{OH}	SCK ₁ , SCK ₂ , SO ₁ , SO ₂ , TO ₁	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{mA}$	
		$\phi 1$, $\phi 2$	0.5 V_{CC}			V	$-I_{OH} = 2\text{mA}$	
Output Low Voltage	V_{OL}	SCK ₁ , SCK ₂ , SO ₁ , SO ₂ , TO ₁			0.4	V	$I_{OL} = 1.6\text{mA}$	
		$\phi 1$, $\phi 2$			0.4	V	$I_{OL} = 2\text{mA}$	
Input Leakage Current	$ I_{IL} $	RESET, INT ₀ , INT ₁ , INT ₂ , INT ₃ , INT ₄ , $\overline{TI_1}$, $\overline{TI_2}$, SCK ₁ , SCK ₂			1	μA	$V_{in} = 0\text{V to } V_{CC}$	
Three-state Current	$ I_{TS} $	$\phi 1$, $\phi 2$			1	μA	$V_{in} = 0\text{V to } V_{CC}$	
Power Dissipation in CPU Operation	I_{CC}	V_{CC}		TBD	TBD	mA	$V_{CC} = 5\text{V}$, $f_{OSC} = 4.5\text{MHz}$ PLL halts	1
Power Dissipation in PLL Operation	I_{CC}	V_{CC}		TBD	TBD	mA	$V_{CC} = 5\text{V}$, CPU, PLL operating ($f_P = 160\text{MHz}$) $f_{OSC} = 4.5\text{MHz}$	1
Power Dissipation in Standby Mode	I_{SBY}	V_{CC}		TBD	TBD	mA	$V_{CC} = 5\text{V}$, $f_{OSC} = 4.5\text{MHz}$	1
Power Dissipation in Stop Mode	I_{STOP}	V_{CC}			10	μA	$V_{CC} = 5\text{V}$	1
Stop Mode Retain Voltage	V_{STOP}	V_{CC}	2			V		

Notes: 1. Output buffer current is excluded.

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Input/Output Characteristics for Standard Pins

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -40\text{ to } +85\text{ }^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input High Voltage	V_{IH}	D0-D13 R0-R4	$0.7 V_{CC}$		$V_{CC} + 0.3$	V		
Input Low Voltage	V_{IL}		-0.3		$0.22 V_{CC}$	V		
Output High Voltage (1)	V_{OH1}	D0-D13 R0-R3	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{ mA}$	
Output Low Voltage (1)	V_{OL1}				0.4	V	$I_{OL} = 1.6\text{ mA}$	
Output High Voltage (2)	V_{OH2}	R5-R8	$V_{CC} - 1.0$			V	$-I_{OH} = 0.2\text{ mA}$	
Output Low Voltage (2)	V_{OL2}				0.4	V	$I_{OL} = 0.3\text{ mA}$	
Input/Output Leakage Current	$ I_{IL} $	D0-D13 R0-R3, R4 ₁ R4 ₀ (V_{PP})			1	μA	$V_{in} = 0\text{V to } V_{CC}$	1
					TBD	μA	$V_{in} = 0\text{V to } V_{CC}$	

Notes: 1. Output buffer current is excluded.

A/D Converter Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -40\text{ to } +85\text{ }^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Resolution				8		bit		
Absolute Accuracy					± 6	LSB		

Liquid Crystal Circuit Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -40\text{ to } +85\text{ }^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Segment Driver Descending Voltage	V_{ds}	SEG1-SEG28			0.6	V	$I_d = 3\mu\text{A}$	1
Common Driver Descending Voltage	V_{dc}	COM1-COM3			0.3	V	$-I_d = 3\mu\text{A}$	1
LCD Power Supply Dividing Resistor	R_{WELL}		TBD	TBD	TBD	k Ω	$V_{CC} = 5\text{V}$	
LCD Frame Frequency	f_F	SEG1-SEG28		274.6		Hz	STATIC	
		COM1-COM3		137.3		Hz	1/2 duty	
				91.6		Hz	1/3 duty	

Note 1: Descending voltage from power supply pins V1, V2, V3, and GND to the segment and common pins.



PLL and IF Circuit Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = GND (PLL) = 0\text{ V}$, $T_a = -40\text{ to } +70^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
PLL Power Supply Voltage	V_{CC} (PLL)	V_{CC} (PLL)	$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V		
Input Frequency	f_{in1}	PLL(P)	20	–	160	MHz	$V_{in} = 0.3 V_{P-P}$	
Input Frequency	f_{in2}	PLL(D)	0.4	–	20	MHz	$V_{in} = 0.3 V_{P-P}$	
Input Frequency	f_{in3}	IF	0.4	–	15	MHz	$V_{in} = 0.3 V_{P-P}$	

AC Characteristics

($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $T_a = -40\text{ to } +85^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Crystal Oscillation	Clock Oscillation Frequency	f_{OSC}	OSC ₁ , OSC ₂	4.5		MHz		
	Instruction Cycle Time	t_{cyc}		1.78		μs	Divide-by-8	
External Interrupt Signal High, Low Width	t_{IH} , t_{IL}	INT ₀ , INT ₁ , INT ₂ , INT ₃ , INT ₄	2			t_{cyc}		1
RESET High Width	t_{RSTH}	RESET	2			t_{cyc}	Other than stop mode	2
			20			ms	Stop mode	
RESET Rise Time	t_{RSTr}	RESET			TBD	ms		2
Input Capacity	C_{in}	All pins other than R40(V_{PP})			15	pF	$f = 1\text{ MHz}$, $V_{in} = 0\text{ V}$, $T_a = 25\text{ C}$	
		R40(V_{PP})			TBD			
Power Supply Voltage Rise Time	t_{rcc}		TBD		TBD	ms		3

- Notes: 1. See figure 68
 2. See figure 69
 3. See figure 70

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Serial Interface Timing Characteristics

(V_{CC} = 5 V ± 10 %, GND = 0 V, T_a = -40 to + 85°C, unless otherwise noted.)

• At Transfer Clock Output

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock Cycle Time	t _{SCYC}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	1	—	—	t _{cyc}	Load circuit	1, 2
Transfer Clock "High" Level Width	t _{SCKH}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	t _{SCYC}	in Fig. 72	1, 2
Transfer Clock "Low" Level Width	t _{SCKL}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	t _{SCYC}		1, 2
Transfer Clock Rise Time	t _{SCKr}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	100	ns		1, 2
Transfer Clock Fall Time	t _{SCKf}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	100	ns		1, 2
Serial Output Data Delay Time	t _{DSO}	SO ₁ , SO ₂	—	—	300	ns		1, 2
Serial Input Data Set-up Time	t _{SSI}	SI ₁ , SI ₂	300	—	—	ns		1
Serial Input Data Hold Time	t _{HSI}	SI ₁ , SI ₂	150	—	—	ns		1

• At Transfer Clock input

Item	Symbol	Pin Name	Min	Typ	Max	Unit	Test Condition	Note
Transfer Clock End Detection Time	t _{SCKHD}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	1	—	—	t _{cyc}		1, 3
Transfer Clock "High" Level Width	t _{SCKH}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	t _{cyc}		1
Transfer Clock "Low" Level Width	t _{SCKL}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	0.4	—	—	t _{cyc}		1
Transfer Clock Rise Time	t _{SCKr}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	100	ns		1
Transfer Clock Fall Time	t _{SCKf}	$\overline{\text{SCK}}_1, \overline{\text{SCK}}_2$	—	—	100	ns		1
Serial Output Data Delay Time	t _{DSO}	SO ₁ , SO ₂	—	—	250	ns	Load circuit in Fig. 72	1, 2
Serial Input Data Set-up Time	t _{SSI}	SI ₁ , SI ₂	300	—	—	ns		1
Serial Input Data Hold Time	t _{HSI}	SI ₁ , SI ₂	150	—	—	ns		1

- Notes: 1. See figure 71
 2. See figure 72
 3. Transfer clock end detection time is an input transfer clock high level width after 8 transfer clock inputs. If the following clock is input before this, the serial interrupt request flag may not be set.



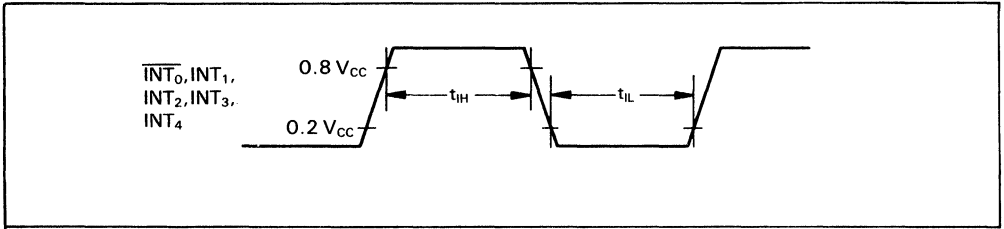


Figure 68. Interrupt Timing

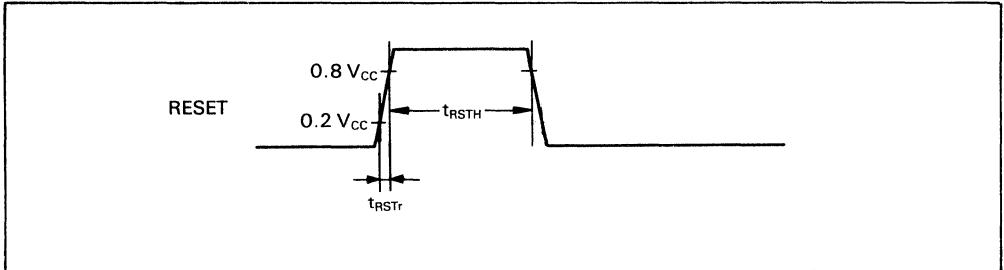


Figure 69. Reset Timing

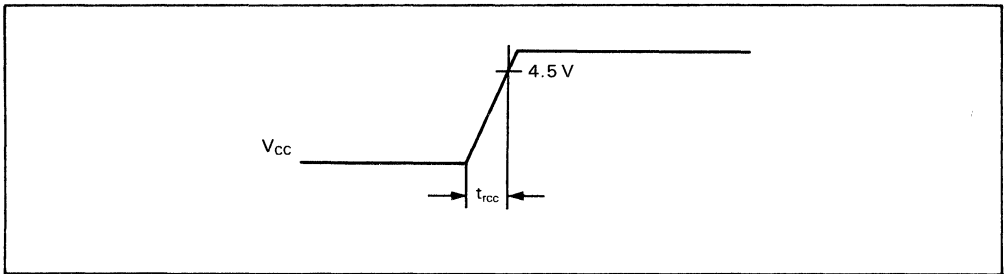


Figure 70. Supply Voltage Rise Time

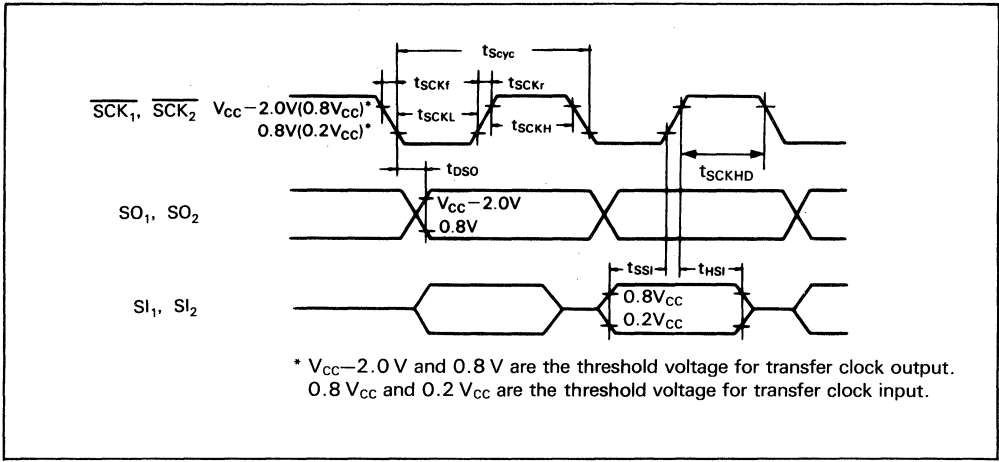


Figure 71. Serial Interface Timing

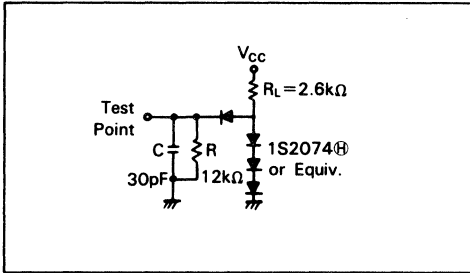


Figure 72. Timing Load Circuit

Programming Electrical Characteristics for HD4074509

DC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Input high voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IH}	2.2		$V_{CC} + 0.3$	V	
Input low voltage	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	V_{IL}	-0.3		0.8	V	
Output high voltage	O_0-O_7	V_{OH}	2.4			V	$I_{OH} = -200\ \mu\text{A}$
Output low voltage	O_0-O_7	V_{OL}			0.4	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	$O_0-O_7, A_0-A_{14}, \overline{OE}, \overline{CE}$	$ I_{Li} $			2	μA	$V_{in} = 5.25\text{ V}/0.5\text{ V}$
V_{CC} current		I_{CC}			30	mA	
V_{PP} current		I_{PP}			40	mA	

AC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise noted)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Address set-up time		t_{AS}	2			μs	Fig. 73
\overline{OE} set-up time		t_{OES}	2			μs	Input Pulse level: 0.8–2.2 V
Data set-up time		t_{DS}	2			μs	Input rise/fall time $\leq 20\text{ ns}$
Address hold time		t_{AH}	0			μs	Timing reference level
Data hold time		t_{DH}	2			μs	input: 1.0 V, 2.0 V output: 0.8 V, 2.0 V
Data output disable time		t_{DF}			130	ns	
V_{PP} set-up time		t_{VPS}	2			μs	
Program pulse width		t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming		t_{OPW}	2.85		78.75	ms	
V_{CC} set-up time		t_{VCS}	2			μs	
Data output delay time		t_{OE}	0		500	ns	

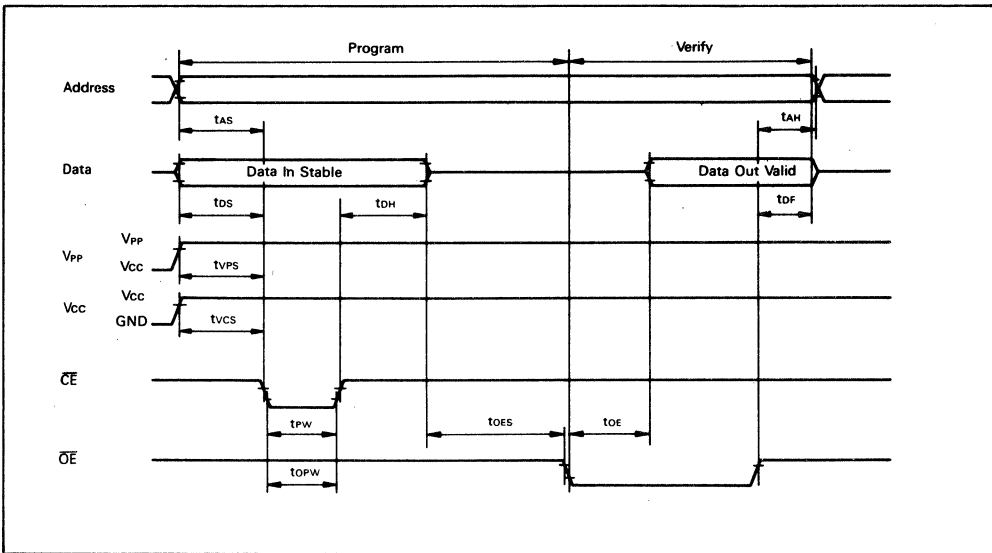
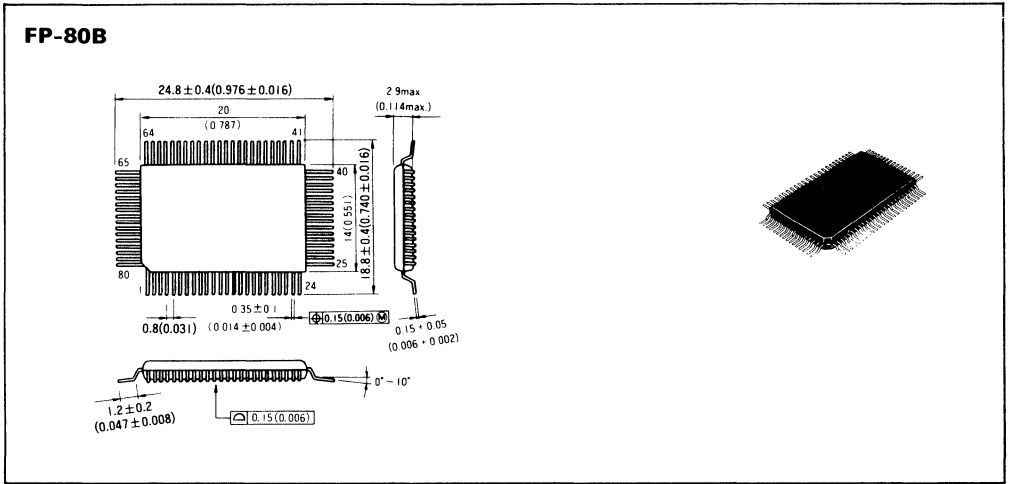


Figure 73. PROM Programming/Verify Timing

Package Dimensions

Unit: mm (inch)



Hitachi America, Ltd.

SEMICONDUCTOR and IC DIVISION

Hitachi America, Ltd.
Semiconductor & IC Division
Hitachi Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819
Telephone: 415-589-8300
Telex: 17-1581
Twx: 910-338-2103
FAX: 415-583-4207

REGIONAL OFFICES

MID-ATLANTIC REGION

Hitachi America, Ltd.
1700 Galloping Hill Rd.
Kenilworth, NJ 07033
201/245-6400

NORTHEAST REGION

Hitachi America, Ltd.
5 Burlington Woods Drive
Burlington, MA 01803
617/229-2150

NORTH CENTRAL REGION

Hitachi America, Ltd.
500 Park Blvd., Suite 415
Itasca, IL 60143
312/773-4864

NORTHWEST REGION

Hitachi America, Ltd.
2000 Sierra Point Parkway
Brisbane, CA 94005-1819
415/589-8300

SOUTH CENTRAL REGION

Hitachi America, Ltd.
Two Lincoln Centre, Suite 865
5420 LBJ Freeway
Dallas, TX 75240
214/991-4510

SOUTHWEST REGION

Hitachi America, Ltd.
18300 Von Karman Avenue,
Suite 730
Irvine, CA 92715
714/553-8500

SOUTHEAST REGION

Hitachi America, Ltd.
4901 N.W. 17th Way, Suite 302
Fort Lauderdale, FL 33309
305/491-6154

AUTOMOTIVE

Hitachi America, Ltd.
6 Parklane Blvd., #558
Dearborn, MI 48126
313/271-4410

DISTRICT OFFICES

Hitachi America, Ltd.
3800 W. 80th Street
Suite 1050
Bloomington, MN 55431
612/896-3444

Hitachi America, Ltd.
21 Old Main Street, Suite 104
Fishkill, NY 12524
914/897-3000

Hitachi America, Ltd.
6161 Savoy Dr., Suite 850
Houston, TX 77036
713/974-0534

Hitachi (Canadian) Ltd.
2625 Queensview Dr.
Ottawa, Ontario, Canada K2A 3Y4
613/596-2777

Hitachi America, Ltd.
401 Harrison Oaks Blvd.
Suite #317
Cary, NC 27513
919/481-3908





Our Standards Set Standards

Hitachi America, Ltd.
Semiconductor and IC Division
Hitachi Plaza
2000 Sierra Point Parkway, Brisbane, CA 94005-1819
1-415-589-8300
