

HT — 6560A	JAN.04.1994
VL_BUS IDE CONTROLLER	PAGE: 1

A. General Description —

HT-6560A is a VL_Bus IDE controller which provides a control logic and data path between 486, 386 VL_Bus and IDE drives. The HT-6560A is fully compatible with the ANSI ATA revision 3.0 specification for IDE hard disk operation and VESA VL_Bus revision 1.0 specification for local bus PC drives.

The HT-6560A is a high performance and fully design for IDE application. At the host CPU interface, HT-6560A provides a posted write and pre-fetched read fully 32 bits data path. It can operate up to 50 MHz and zero wait-state cycle. Double word read and write operations are provided. It also allows concurrent IDE and CPU memory operations to maximize system performance. Flexible IDE drive interface timing selection. Power on reset latch the adequate IDE active and recovery time into config register. HT-6560A also allows you detect IDE performance and change the config register by software program or BIOS.

B. Features —

- VESA VL_Bus rev 1.0 compatible.
- Connects directly to VL_Bus and IDE interface no extra TTL needed.
- Supports 16 bits and 32 bits data transfer.
- Zero wait_state 50MHz operation.
- Support read pre-fetch, posted write and I/O channel ready function.
- Support various type of ANSI ATA compatible IDE drives.
- Programmable command active and recovery time.
- Support primary and secondary I/O port selection.
- 100-pin PQFP package.
- BIOS and software driver supported.

C. Block Diagram —

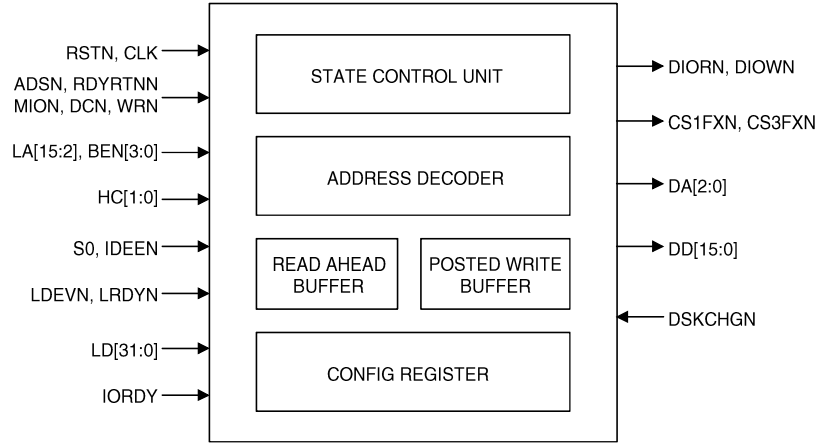
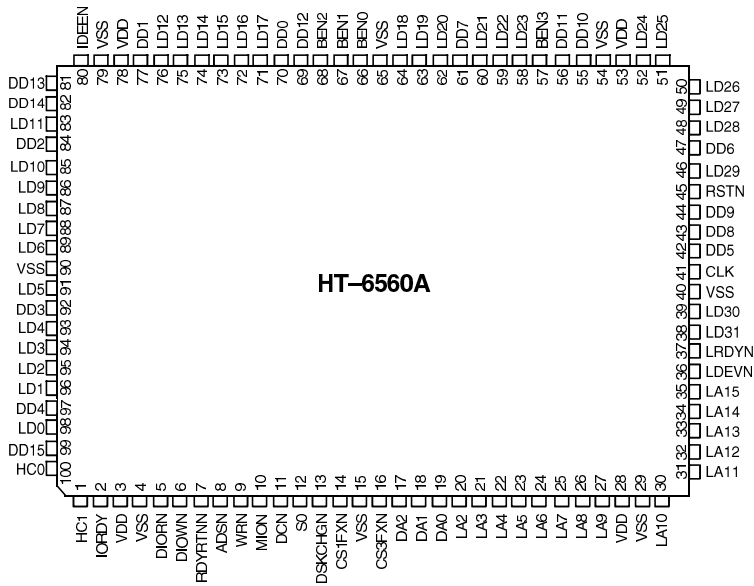


Fig.1.

D. Pin Assignment —



E. Pin Description —

Pin No.	Pin Name	I/O	Description
1	HCI	I	Command recovery time counter bit 1.
2	IORDY	I	This signal is negated to extend the host transfer cycle of any host command or data register access when the drive is not ready to respond to a data transfer request. When IORDY is not negated, IOCHRDY is in a high impedance state.
3,28,53,78	VDD	—	+5V POWER.
4,15,29,40,54, 65,79,90	VSS	—	GROUND.
5	DIORN	O	Drive I/O read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIORN cycles is determined by the type of IDE drive and programmed by HT-6560A.
6	DIOWN	O	Drive I/O write is an active low output which enables data to be written to the drive. The duration and repetition rate of DIOWN cycles is determined by the type of IDE drive and programmed by HT-6560A.
7	RDYRTNN	I	Ready return is an active low signal which indicates the end of the current host CUP transfer.
8	ADSN	I	Address strobe is an active low input signal which indicates that there is a valid address and command on the bus.
9	WRN	I	Write (active high) or read (active low) is an input which distinguishes between write and read cycles.
10	MION	I	Memory (active high) or I/O (active low) is an input which distinguished between momory and I/O cycles.
11	DCN	I	Data (active high) or control (active low) is an input which is used to distinguish between I/O and interrupt or halt cycles.

Pin No.	Pin Name	I/O	Description
12	S0	I	Primary or secondary I/O port selection input. Level high for primary, level low for secondary I/O port.
13	DSKCHGN	I	Disk change is an input which comes from floppy diskette drive connector pin 34.
14	CS1FXN	I/O	Drive chip select 1 is normal an active low output which used to select the command block registers in the drive. This pin is an input which is command active time counter bit 3 during power on reset and sampled on the rising edge of RSTN.
16	CS3FXN	I/O	Drive chip select 3 is normal an active low output which used to select the control block registers in the drive. This pin is an input which is command recovery time counter bit 2 during power on reset and sampled on the rising edge of RSTN.
17	DA2	I/O	Drive address, bit 2, is normally output to the IDE connector for register selection in the drive. This pin is an input which is command active time counter bit 2 during power on reset and sampled on the rising edge of RSTN.
18	DA1	I/O	Drive address, bit 1, is normally output to the IDE connector for register selection in the drive. This pin is an input which is command active time counter bit 1 during power on reset and sampled on the rising edge of RSTN.
19	DA0	I/O	Drive address, bit 0, is normally output to the IDE connector for register selection in the drive. This pin is an input which is command active time counter bit 0 during power on reset and sampled on the rising edge of RSTN.
20~27,30~35	LA2~LA15	I	These are the host address bits 2 through bits 15 from the host address bus.

Pin No.	Pin Name	I/O	Description
36	LDEVN	O	Local device is an active low output which indicates that the current host CPU command cycle is a valid HT-6560A address.
37	LRDYN	Tri-O	Local ready is an active low output which indicates that the current host CPU transfer has completed. As the current cycle is completed, the LRDYN will immediately pull low and remain active for one T-state.
38,39,46,48~52, 58~60,62~64, 71~76,83,85~89 ,91,93~96,98	LD31~LD0	I/O	Host data is the 32 bits bi-directional data bus which connects to the host CPU LD[7:0] define the lowest data byte while LD[31:24] define the most significant data byte. The active bytes on a CPU transfer are specified by the BEN[3:0] signals. The LD bus is normally in high impedance state and is driven only after T2 state of HT-6560A read cycles.
41	CLK	I	VL_Bus clock.
42~44,47,55,56, 61,69,70,77,81, 82,84,92,97,99	DD15~DD0	I/O	Drive data bus, bits 15 through 0, are the 16 bits bi-directional data bus which connects to the IDE drive. DD[7:0] define the lowest data byte while DD[15:8] define the most significant data byte.
45	RSTN	I	System reset is an active low input.
57,66~68	BEN3~0	I	Byte enable bits 0 through 3 from the host CPU address bus. These inputs are active low and specify which bytes will be valid for host read/write data transfers.
80	IDEEN	I	IDE enable is an active high input which enable the HT-6560A for drive operation. Low input which disables HT-6560A.
100	HC0	I	Command recovery time counter bit 0.

F. Absolute Maximum Ratings —

Parameter		Symbol	Minimum	Maximum	Unit
Supply Voltage		V _{DD}	-0.5	6	V
Input/Output Voltage		V _I ,V _O	V _{SS} -0.5	V _{DD} +0.5	V
Storage Temperature	Plastic	T _{STG}	-40	125	°C
Temperature Under Bias	Plastic	T _{BIAS}	-40	85	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

V_{SS}=0V.

G. Recommended Operating Conditions —

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{DD}	4.75	5	5.25	V
Input High Voltage for Normal Input	V _{IH}	2.2	—	—	V
Input Low Voltage for Normal Input	V _{IL}	—	—	0.8	V
Operating Temperature	T _A	0°C	25°C	70°C	°C

H. DC Characteristics —

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{DD5}	Power Supply Current	Steady state.	—	—	0.2	mA
V _{OH1}	Output High Voltage for Normal Output (LD[3:0], LRDYN, LDEVN)	I _{OH} =-2mA	4	—	V _{DD}	V
V _{OH2}	Output High Voltage for Driver Output (DD[15:8], DA[0:2], CS1FXN, CS3FXN, DIORN, DIOWN)	I _{OH} =-4mA	4	—	V _{DD}	V
V _{OH3}	Output High Voltage for Driver Output (DD[0:7])	I _{OH} =-0.8mA	4	—	V _{DD}	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{OL1}	Output Low Voltage for Normal Output (LD[31:0], LRDYN, LDEVN)	I _{OL} =3.2mA or 8mA	V _{SS}	—	0.4	V
V _{OL2}	Output Low Voltage for Driver Output (DD[15:8], DA[0:2], CS1FXN, CS3FXN, DIORN, DDOWN)	I _{OL} =12mA	V _{SS}	—	0.4	V
V _{OL3}	Output Low Voltage for Driver Output (DD[0:7])	I _{OL} =24mA	V _{SS}	—	0.5	V
V _{IH}	Input High Voltage	Normal	2.2	—	V _{DD}	V
		Schmitt Trigger	2.4	—	V _{DD}	V
V _{IL}	Input Low Voltage	Normal	V _{SS}	—	0.8	V
		Schmitt Trigger	V _{SS}	—	0.6	V
I _{LI}	Input Leakage Current	V _I =0–V _{DD}	–10	—	10	μA
I _{LZ}	Input Leakage Current	Tri-state V _I =0–V _{DD}	–10	—	10	μA
R _P	Input Pull-Up Resistor	V _{IH} =V _{DD}	25	50	100	KΩ
R _N	Input Pull-Down Resistor	V _{IL} =V _{SS}	5			

I. Capacitance — (T_a=25°C, V_{DD}=V_I=0V, f=1MHz)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V _{DD}	Condition				
C _{IN}	Input Pin Capacitance					16	pF
C _{OUT}	Output Pin Capacitance (I _{OL} =3.2/8/12mA)					16	pF
C _{OUT}	Output Pin Capacitance (I _{OL} =24mA)					18	pF
C _{I/O}	I/O Pin Capacitance (I _{OL} =3.2/8/12mA)					16	pF
C _{I/O}	I/O Pin Capacitance (I _{OL} =24mA)					18	pF

J. Functional Description —

The HT-6560A contains five major blocks as shown in fig.1. They are state control unit, address decoder, read ahead buffer, posted write buffer, config register.

The state control unit contains a state machine which controls all of the read/write timing and data swapping to IDE drives. The address decoder connects to VL_Bus directly, decodes valid address of the HT-6560A config register and IDE drive registers. Read ahead buffer and posted write buffer which can accelerate the data read/write speed. The config register let user can set the command active and recovery time to optimize the IDE performance. In addition to, you can detect or set primary or secondary IDE port through the config register.

1. Restet Initialization

Signal Name	Signal State During Reset
CS1FXN	High-Impedance
CS3FXN	High-Impedance
LDEVN	High-Impedance
DIOWN	1
DIORN	1
LRDYN	High-Impedance
DA[2:0]	High-Impedance
LD[31:0]	High-Impedance
DD[15:0]	High-Impedance

2. Host Interface

a. CPU Cycle Definition:

MION	DCN	WRN	Address Space	IDE Cycle
0	1	0	1F0h-1F7h and 3F6h for primary drive. 170h-177h and 376h for secondary drive.	DIORN CYCLE
0	1	1	1F0h-1F7h and 3F6h for primary drive. 170h-177h and 376h for secondary drive.	DIOWN CYCLE
0	0	0	Don't care.	NOP
0	0	1	Don't care.	NOP
1	0	0	Don't care.	NOP
1	0	1	Don't care.	NOP
1	1	0	Don't care.	NOP
1	1	1	Don't care.	NOP

b. HT-6560A Write Data Operation:

CPU Write Byte Enable				HT-6560A Input Data			
BEN3	BEN2	BEN1	BEN0	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]
0	0	0	0	valid	valid	valid	valid
0	1	1	1	valid	X	X	X
1	0	1	1	X	valid	X	X
1	1	0	0	X	X	valid	valid
1	1	0	1	X	X	valid	X
1	1	1	0	X	X	X	vaild

c. HT-6560A Read Data Operation

CPU Write Byte Enable				HT-6560A Output Data			
BEN3	BEN2	BEN1	BEN0	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]
0	0	0	0	valid	valid	valid	valid
0	1	1	1	valid	same as LD[31:24]	same as LD[31:24]	same as LD[31:24]
1	0	1	1	same as LD[23:16]	valid	same as LD[23:16]	same as LD[23:16]
1	1	0	0	same as LD[15:0]		valid	
1	1	0	1	same as LD[15:8]	same as LD[15:8]	valid	same as LD[15:8]
1	1	1	0	same as LD[7:0]	same as LD[7:0]	same as LD[7:0]	valid

3. IDE Interface

a. DA[2:0] Generation:

LA2	BEN[3:0]	DA[2:0]
0	XX00	000
0	XX01	001
0	X011	010
0	0111	011
1	XXX0	100
1	XX01	101
1	X011	110
1	0111	111

b. Drive Select Signal Operation:

Signal Name	Address Range
CS1FXN	1F0h-1F7h for primary drive. 170h-177h for secondary drive.
CS3FXN	3F6h-3F7h for primary drive. 376h-377h for secondary drive.

K. HT-6560A Register Setting —

1. Active Time and Recovery Time Setting

Suggest active time is 2~15 cycles which depend on IDE drive type and system speed.

You can set this register by hardware or software setting.

a. Hardware Setting:

During power on reset, this register can be latched from following pins.

Active Time:

CS1FXN	DA2	DA1	DA0	Cycles
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
		↓		
1	1	1	1	15

Recovery Time:

CS3FXN	HC1	HC0	Cycles
0	0	0	8
0	0	1	9
		↓	
1	1	1	15

b. Software Setting:

After power on reset, you still can program the config register by following procedures:

- Read I/O port 3E6 four times to turn on config mode.
- Write 8 bits data to I/O port 1F6 (or 176)

Recovery Time:

Data	bit7	bit6	bit5	bit4	Cycles
	0	1	0	0	4
	0	1	0	1	5
	↓				
	1	1	1	1	15
	0	0	0	0	16
	0	0	0	1	17

Active Time:

Data	bit3	bit2	bit1	bit0	Cycles
	0	0	1	0	2
	0	0	1	1	3
	↓				
	1	1	1	1	15

- Read I/O port 1F7 (or 177) one time to clear config mode.

2. Primary and Secondary I/O Port Setting

a. Hardware Setting:

During power on reset, this register can be latched from the S0 pin.

S0	I/O Port
1	1F0~7, 3F6~7, (primary)
0	170~7, 376~7, (secondary)

b. Software Setting:

After power on reset, you still can program the I/O port register by writing data to port 3E6.

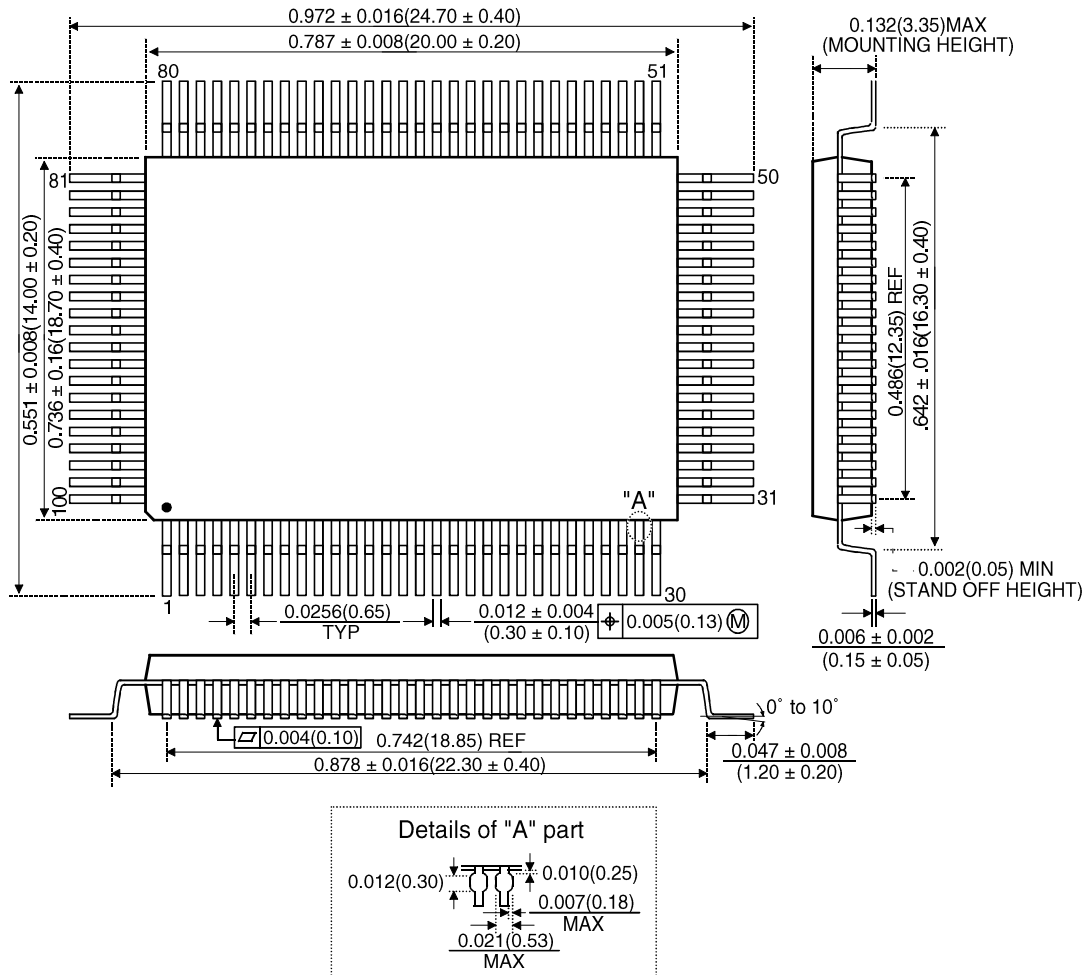
bit 0	I/O Port
1	1F0~7, 3F6~7, 3E6 (primary)
0	170~7, 376~7, 3E6 (secondary)

This bit also can be read in data bit 0 by reading port 3E6.

3. Register 3E6:

- bit 0: Primary and secondary I/O port setting.
 - 1: Primary.
 - 0: Secondary.
- bit 1: Define pre-fetched data read function, normally no pre-fetched data read function.
 - 1: No pre-fetch function.
 - 0: Pre-fetch.
- bit 2: If system is multi-master, then set it 0, normally 1 (not multi-master system).
- bit 3: Define address setup time, normally 1.
 - 1:3 cycle time
 - 0:2 cycle time

L. Package Information —



Dimensions in inches (millimeters)

M. Application Circuit —

