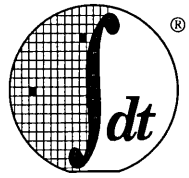

1995
RISC
MICROPROCESSOR
PROCESSORS,
SUPPORT
COMPONENTS,
SOFTWARE, &
BOARD-LEVEL
PRODUCTS
DATA BOOK
Integrated
Device
Technology,
Inc.
idt
CERTIFIED POWER
ORION
Complexity



Integrated Device Technology, Inc.

1995
RISC MICROPROCESSORS DATA BOOK

2975 Stender Way, Santa Clara, California 95054
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 492-8674
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GENERAL INFORMATION

CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books — Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1995 RISC Data Book is comprised of new and revised data sheets for the RISC and RISC Subsystems product groups. Also included is a current packaging section for the products included in this book. This section will be updated in each subsequent data book to reflect packages offered for products included in that book.

The 1995 RISC Data Book's Table of Contents contains a listing of the products contained in that data book only. In the past we have included products that appeared in other IDT data books. The numbering scheme for the book is as follows: the number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speed, lower power, and package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, and Cross Reference Guides. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

PRODUCT BRIEF — contains initial descriptions, subject to change, for products that are in development, also includes a features listiing.

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1995 RISC DATA BOOK
TABLE OF CONTENTS

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1995 RISC DATA BOOK (Continued)

RISC DEVELOPMENT SUPPORT PRODUCTS

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

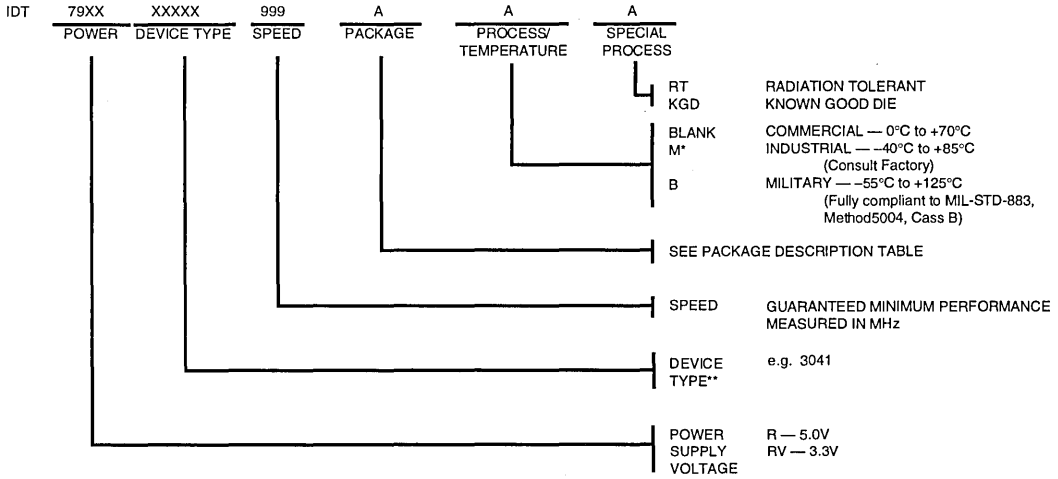
ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772
Dun & Bradstreet Number — 03-814-2600
Federal Tax I.D. — 94-2669985
TLX# — 887766
FAX# — 408-727-3468

PART NUMBER DESCRIPTION



PACKAGE DESCRIPTION TABLE

J	84-lead PLCC
PF	100-lead TQFP
	160-Lead PQFP
	208-Lead PQFP
MJ	84-lead MQUAD
FD	84-lead Cavity-down Flatpak
G	179-pin PGA
	447-pin PGA
GL	Extended lead 447-pin PGA
MS	208-lead MQUAD

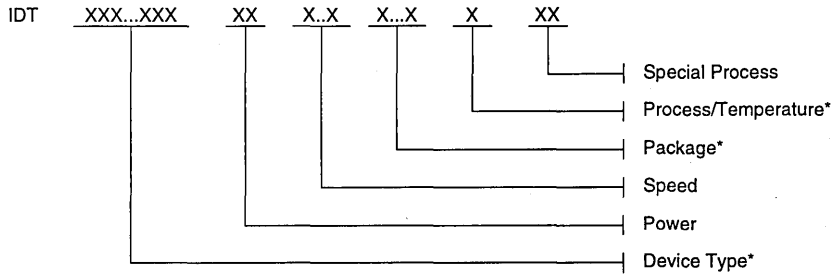
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "R" is used for 5.0V compliant products.
   "RV" is used for 3.3V compliant products.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

V = Penang, hermetic
I = Anam, Korea
T = Hong Kong
A = USA
G = USA, hermetic
M = USA, plastic
P = Api, Phillipines
H = Penang, plastic

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships certain military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

Integrated Device Technology, Inc.

HIGH-SPEED CMOS MICROPROCESSOR FAMILY PRODUCT SELECTOR GUIDE

High-Speed CMOS Microprocessor Family

- Broadest range of high-performance to low-cost, code-compatible RISC processors: R3000A, R4000 CPUs, R3041/51/52/81 RISControllers, R4600, R4650, and R4700
- R4400—third-generation high-performance 64-bit CPU and FPA with on-chip cache
- R3051/52/81/41 RISController Family—designed for lower-cost embedded systems, all code-compatible with original R3000
- Support chips designed for RISC systems: R3715 System Controller, R3740 Laser Printer Controller, R4761 Orion Family System Controller, and R4762 Orion Family PCI Bridge Chip
- Applications range from real-time control to multiprocessing systems
- Optimizing compilers
- Low-cost Evaluation Boards available

Number	Description	Pkgs.	Avail.	Data Book Page
RISC CMOS MICROPROCESSORS				
IDT79R4400	Very high-performance, highly integrated 64-bit CPU, fully binary compatible with the R3000A. Combines CPU, floating-point and 16/32KB of cache, capable of over 50 VAX mips sustained performance	447PGA 179PGA	NOW	5.6
IDT79R3041	RISController, 2.5KB cache, R3000A core, 4-deep read/write buffers, low-cost packaging, pin-compatible with R3051/52/81	84PLCC 100PF	NOW	5.2
IDT79R3051/52	RISControllers, 6KB or 10KB on-chip cache, R3000A CPU core, and 4-deep read/write buffers, low-cost 84-pin packaging	84PLCC 84MJ	NOW	5.2
IDT79R3081	RISController, 20KB on-chip, R300 CPU core, R3010A Floating Point Accelerator, 4-deep read/write buffers, pin-compatible with R3041/51/52	84MJ 84FD 100PQFP	NOW	5.3
IDT79R4600	Very high-performance, highly integrated 64-bit CPU, fully binary compatible with the R3000A . Combines CPU, floating-point and 32KB of cache, capable of over 175 mips sustained performance	179PGA 208 MQUAD	NOW	5.4
IDT79R4650	R4600 derivative capable of 66.7 Million Integer Multiply-Accumulate Operations/sec @ 133MHz and 175 mips sustained performance. Combines CPU, floating-point and 16KB of cache.	208MQUAD	NOW	5.5
IDT79R4700	Pin-compatible with the R4600, the R4700 is an enhanced version of the R4600. Combines CPU, floating-point and 32KB of cache, capable of over 225 mips sustained performance	179PGA 208MQUAD	NOW	5.6

Part Number	Description	Avail.	Data Book Page
R3000 FAMILY EVALUATION KITS			
IDT79S341	R3041 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3041 CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	7.5
IDT79S385A	R305X Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3052E CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports. Supplied with all schematics, PAL equations and user's manual. Also includes DOS version of the IDT/c compiler (see 7RS903) and a sample of the R3081.	NOW	7.4
IDT79S381	R3081 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R3081 CPU, 2MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	7.6
IDT79S460	R4600 Family Evaluation Board. Complete, self-contained system requiring only a power supply and simple terminal to be operational. Kit contains R4600 CPU, 1MB of DRAM, IDT/sim monitor in EPROM, serial I/O ports.	NOW	7.7
R3000 FAMILY SOFTWARE DEVELOPMENT TOOLS			
IDT79S901	IDT/sim System Integration Manager (see RISC SubSystems for description)	NOW	7.8
IDT79S903	IDT/c C-Compiler (see RISC SubSystems for description)	NOW	7.9
IDT79S909	IDT/kit Kernel Integration Toolkit (see RISC SubSystems for description)	NOW	7.10

Integrated RISC Design Solutions

IDT is committed to providing complete integrated RISC solutions by combining expertise in silicon process technology with leadership products in development systems and software. Long an industry leader in producing the fastest static RAMs for cache memory and high-speed logic for memory interface, IDT offers:

- Dedicated RISC support chips
- Development tools such as multi-hosted Cross Compilers
- CPU and cache modules
- RISC evaluation and prototyping vehicles
- Monitors and debuggers

RISC SubSystems—RISC Without Risk ..... IDT Provides Total RISC System Solutions!

FASTER SYSTEMS: FASTER DESIGN CYCLES

Using RISC technology, you can build systems that will run rings around an old x86 or 680x0 design. IDT's RISC SubSystems Division can help you get your design completed in record time. IDT has proven RISC design and manufacturing experience that you can rely on. Exploit our expertise by having IDT design *AND* manufacture your board. Or integrate one of our pre-built, fully-tested modules into your design.

Architectural Expertise

IDT brings together a unique combination of component knowledge, software skills, and board design experience as the foundation for developing a board-level product that meets your needs. As experienced system architects, we understand that component knowledge alone is not enough—that the interface between hardware and software is critical to a successful design. We have spent years honing our architectural expertise to include an in-depth understanding of both the hardware and software issues so our designs produce the performance you expect.

Fast Development Cycle

IDT uses the most advanced engineering tools in our hardware development lab. We have qualified quick-turn PCB fab houses and our own fully-equipped advanced manufacturing area, so new fabs can be assembled and sent into debug in a matter of days. In addition, IDT has developed the best software diagnostic tools available for MIPS RISC debug. Spotting behavioral patterns in malfunctioning systems and quickly identifying and fixing the hardware or software problem is key to maintaining a time-critical development cycle—and we want you to be first to market!

Optimized Designs

IDT is a premier supplier of RISC assemblies. Our expertise in handling layout, termination, and component selection issues is unmatched, and we use the latest tools for PCB layout, routing and design simulation. Our design team is fast and experienced, coordinating component selection with availability of the latest technology, and using ASICs where appropriate to improve performance and reduce space and cost. To date, we have designed and produced more different MIPS RISC assemblies than anyone else, optimizing every design for the highest possible performance per dollar.

Total Support

On-going support means on-time deliveries. IDT has on-going vendor TQM programs with suppliers of critical components to ensure on-time delivery of in-spec material. Our manufacturing organization is experienced in building very high-speed boards with tight tolerances and high-pin-count surface-mount components. And our design team is on-call to solve problems quickly if difficulties arise during production. We provide total support—from board design and software porting through production and test—because our success depends on your success!

Modules

Our modules contain the RISC CPU, Floating Point Accelerator, and all the cache memory. Most include clock control, interrupt and initialization logic, and read and write buffers, as well. All the components are surface-mounted on small, plug-in PC boards, burned-in and tested at the rated speed. All the tricky timing, and high-speed design is done and tested for you. The modules can be plugged into motherboards containing main memory, I/O, and the rest of the system, all of which is relatively low-speed and is easy to lay out using conventional design techniques.

Custom Subsystems

For custom boards that meet your unique requirements, we can develop a complete product specification, design the boards, deliver prototypes, and provide production units in any quantities. Many customers have found this to be a cost-effective way to augment their own engineering resources, and to procure material that exactly meets their needs without all the headaches of purchasing, material control, and on-going product and manufacturing engineering.

Printer Controllers

IDT has designed and produced a number of printer controllers, using both custom and standard hardware solutions. IDT's board-level products have been used to run Adobe PostScript™, PCL5 emulation, and Pipeline Associates' color PostScript emulation. IDT is a licensee for Adobe's CPSI interpreter, and can develop a flexible true Adobe solution in a variety of hardware and software environments.

Model	Description
Custom Designs	
	• Plotter Controllers
	• Add-In Cards to EISA/ISA Bus
	• Add-in Cards for Macintosh
	• Laser Printer Controllers
Software	
	• Adobe CPSI PostScript Application Development
	• UNIX™ Porting, and Driver Development
	• C-EXECUTIVE™ Real Time OS
	• Interprocessor Communication between RISC Subsystem and Mac or PC

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 Static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CMOS technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L

SMD	
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L
CLP	**IDT**
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A

SMD	
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92205	29FCT520AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92232	54FCT241T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT
RISC	**IDT**
5962-94550	79R3081E

SMD

SRAM	IDT
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682

SMP	IDT
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S

FIFO	IDT
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L

CLP	IDT
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A

LOGIC	IDT
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92205	29FCT520AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92232	54FCT241T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT

RISC	IDT
5962-94550	79R3081E

RADIATION HARDENED TECHNOLOGY

On an order by order basis IDT can manufacture and supply radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply most of its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

KNOWN GOOD DIE

Emerging high performance electronic systems require smaller and smaller form-factors. IDT is meeting these design challenges by offering Known Good Die (KGD) in addition to its broad array of small form-factor packages. The IDT KGD manufacturing process enables IDT to offer die that have received the same electrical tests, burn-in, and speed sorting at elevated temperatures as shipped packaged products. Via IDT KGD, users are able to manufacture cost-efficient and reliable multi-chip modules (MCMs), hybrids, and other high-density interconnect products. All IDT KGD, at the completion of their test flow, receive 100% die visual inspection and are packed within Gel-Pak™ containers. The Gel-Pak™ containers are then placed in vacuum sealed ESD wrappers prior to shipping. Delivered KGD products have superior yield, quality, and reliability over standard raw die offerings. Most IDT products can be offered as "KGD", and commercial, industrial or military temperatures can be considered.

THE PRODUCTIVITY REVOLUTION

New microprocessor-based systems enhance productivity by improving the accessibility and usability of information. By connecting systems through a network, data can be transmitted instantly, anywhere in the world. Using affordable computing systems, information can be located, retrieved, analyzed, and displayed as needed.

The systems that provide these capabilities are built around the microprocessor, and IDT's products maximize the potential of these microprocessor-based systems. As sales of these productivity-enhancing systems grow, so do the markets for IDT products.

INNOVATIVE PRODUCTS FOR MORE PRODUCTIVE SYSTEMS

IDT markets products from four product groups: SRAMs, Specialty Memory Products, Logic products, and RISC Microprocessors.

Our strategy is to define, develop, and manufacture products that help our customers deliver greater value to their customers. We develop products in partnership with customers who are leaders in markets that fuel the productivity revolution, such as high-performance desktop and server computing, data communications and networking, and office automation. These customers use our products to build systems that are faster, less costly, and more productive.

Our customers are also building systems that are energy-efficient. Designers are developing 3.3V systems to comply with the governmental Energy Star requirements. We have a competitive advantage because our CMOS VII technology was specifically designed to maintain higher speeds at this lower voltage.

Customers using high-performance microprocessors to build desktop computers and file servers can improve the performance of their products by incorporating cache memory systems. Cache memory systems are constructed with high-speed SRAMs, cache tag memories, and control logic. We are a recognized technology leader in SRAMs and the world's leading supplier of cache tag memories. Today, we supply these products both as discrete components and in the form of complete high-density cache memory modules used with PowerPC™, Intel 486™, Pentium™ processor, and our own RISC microprocessors. We are working with manufacturers of both the microprocessors and their associated chipsets to develop new cache memory products that will maximize the performance of future microprocessor-based systems.

Customers building digital data communications and networking equipment use FIFO and dual-port memory products that are designed for these applications. FIFOs and dual-ports are uniquely suited to exchanging data between systems that operate at different speeds or use different protocols, a common requirement in communications systems. We are the market leader in these SMP product areas, and we have introduced the industry's largest number of product and technology innovations over the years. Development work is now under way to design a family of products for the emerging ATM (Asynchronous Transfer Mode) market, which is expected to grow dramatically over the next several years.

Every high-performance system needs high-speed logic parts to connect memories, microprocessors, communications circuits, and other system components. We have been the performance leader in high-speed FCT logic devices since we pioneered these products in 1985, and we currently offer more than 150 different logic products. We have also introduced two new ultra-small packaging choices for our logic products, ideal for use in compact desktop and portable systems, as well as in PCMCIA cards, which are credit-card sized modules that add functionality to personal computers.

Customers who build high-performance office automation and communications systems are taking advantage of our family of 32-bit and 64-bit software-compatible RISC microprocessors, based on the extendable architecture developed by MIPS Technologies. The 20+ different microprocessors in our RISC family offer customers a wider range of price/performance choices than competing microprocessor families. Software compatibility allows designers to choose one microprocessor for a particular product and then easily upgrade to a higher-performing version, in many cases simply by removing one device and plugging in another. Our 32-bit RISC microprocessor products are winning acceptance in a variety of embedded applications, including laser printers, network routers, and graphics display terminals.

In fiscal 1994, we introduced our 64-bit R4600™ Orion™ processor. This microprocessor provides leading-edge performance for embedded applications, such as laser printers and networking systems, and is also used in file servers and workstations that run UNIX® and Microsoft's new Windows NT™ operating systems.

ADVANCING OUR OWN PRODUCTIVITY

We participate in the productivity revolution both as a technology enabler and as a beneficiary. While our products enhance the productivity of our customers' microprocessor-based systems, we improve our own internal productivity by developing new manufacturing technologies, re-engineering workflows, and by adopting new electronic systems.

One of the primary ways we increase internal productivity is by developing and implementing advanced technologies. New process technologies result in smaller die, and new production equipment allows the use of larger wafers. The combination of smaller die and larger wafers allows us to generate significantly more devices per wafer. Migrating to an advanced 0.6-micron CMOS fabrication process in fiscal 1994 not only resulted in smaller die, it also improved product performance, increased yields, and lowered unit costs. Our new CMOS VIII 0.5-micron process is expected to extend our

process technology momentum.

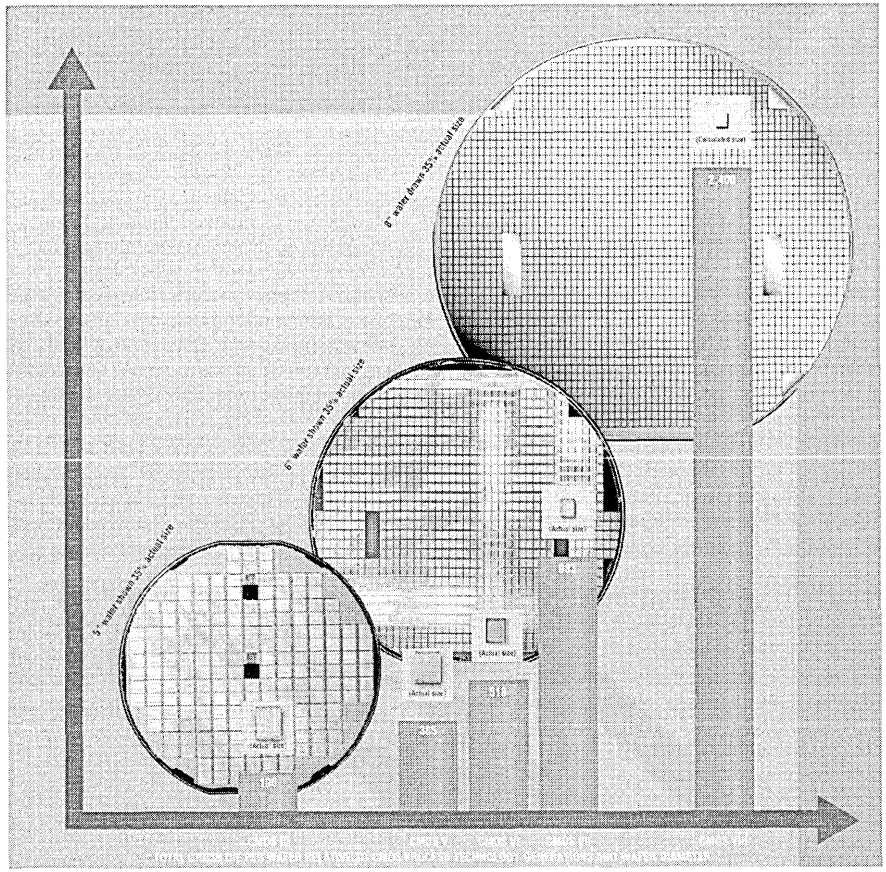
Because we have our own fabrication facilities, we control critical manufacturing operations, giving us a competitive advantage as we continue to improve our productivity. IDT has two sub-micron 6" wafer fabrication facilities, located in San José and Salinas, California, and a high-volume assembly and test facility in Penang, Malaysia. To support future growth, we have built a new sub-micron 8" wafer fabrication facility in Hillsboro, Oregon that will be fully operational in fiscal 1997, and an additional 40,000-square-foot building for test and assembly in Penang.

Manufacturing productivity is also improved by adjusting work schedules to increase the output from equipment already in place and improving product development cycles. Updated computer-aided design tools shorten product design times and improve the functionality of new product prototypes. For example, the R4600 Orion processor was designed by Quantum Effect Design, Inc., an IDT affiliate operating on-site, in just 21 months, which is a remarkably short development cycle for such a complex product.

Improvements in quality are the direct result of improvements in productivity. Our manufacturing quality levels have been improving for several years. In fiscal 1993, IDT was one of the first semiconductor companies to achieve ISO 9000 registration for wafer fabrication activities. ISO 9000 is a worldwide quality systems standard, and certification provides an important competitive advantage in both domestic and international markets. All of our manufacturing facilities are now ISO 9000 certified.

Customer service and support have been directly enhanced by many of our productivity improvements. New planning and scheduling systems allow us to improve our efficiency and predictability for meeting delivery commitments to customers. Expanded computer systems allow the migration of order services to field sales offices, bringing support closer to the customer. Increased use of EDI (Electronic Data Interchange) allows customers to directly enter orders and check order status, resulting in more timely information with less paperwork.

Improving productivity continues to be a key issue for technology companies. By continuing to improve internal productivity and manufacture quality products that support the productivity revolution, we expect to enhance the value of our company to our shareholders, our employees, and our customers.



SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-I-38535, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform Class S processing per MIL-STD-883 and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Total Quality Commitment (TQC) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR TQC

Measurable standards are essential to the success of TQC. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

PRODUCT FLOW

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on TQC by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the TQC process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing

To accomplish continuous improvement during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the TQC process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to continuous improvement is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade. With the implementation of the TQC strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C[1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min. or equivalent	100%	Per applicable device specification	100%
PORT BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, –55 and 125°C	100%	Per applicable device specification +25, –55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC, Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D	Sample	5005 Group B, C, D	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on Total Dose Accumulation. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan can qualify wafers to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are

assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified (if desired) to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of most product types (some speed grades may not be available).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (TJ), it becomes increasingly important to maintain a low (TJ).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp\left[\frac{Ea}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

- t_A = lifetime at elevated junction (TJ) temperature
- t_O = normal lifetime at normal junction (TO) temperature
- Ea = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5} ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (TJ), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

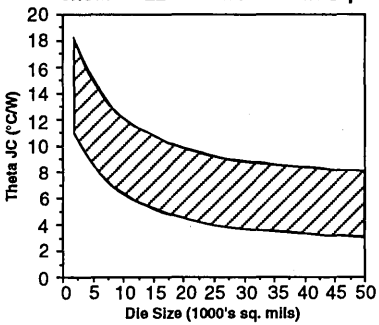
where

$$\frac{\theta_{JC} = T_J - T_C}{P} \qquad \frac{\theta_{CA} = T_C - T_A}{P}$$

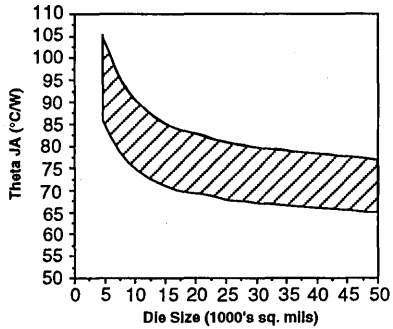
- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

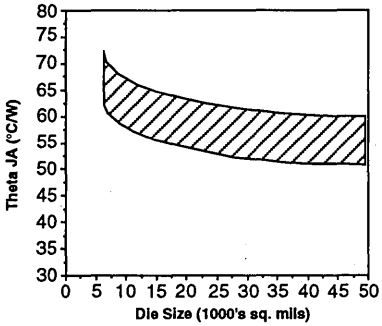
Theta JC 22-40 Lead Ceramic Dips



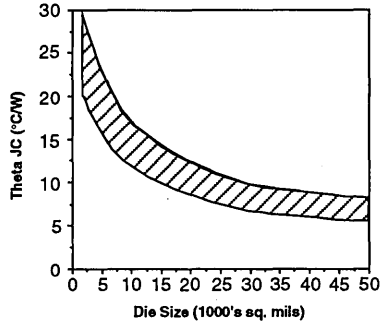
Theta JA - Still Air 16-20 Lead Ceramic Dips



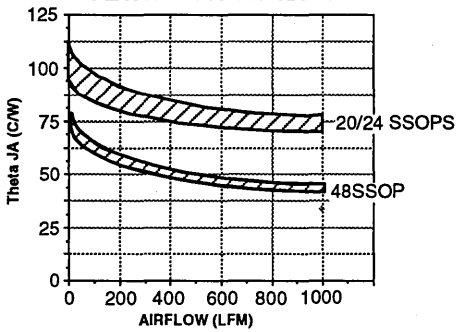
Theta JA - Still Air 22-40 Ceramic Dips



Theta JC 16-20 Lead Ceramic Dip

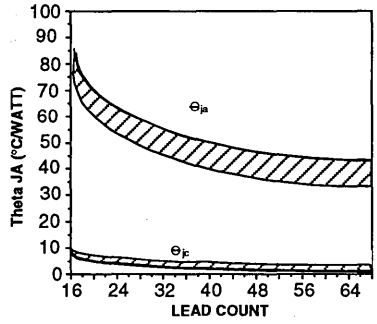


Theta JA vs. Airflow
PLASTIC SSOP PACKAGES

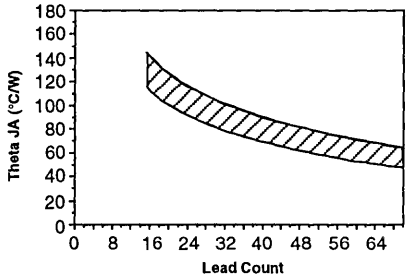


THETA JC : 20/24 PIN = 35-40 °C/W
48 PIN = 16-20 °C/W

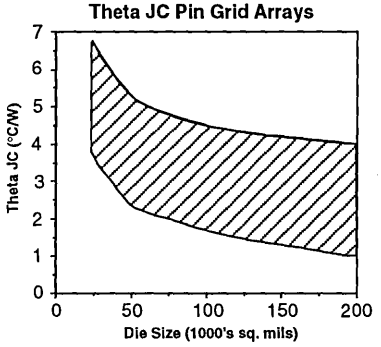
Thermal Resistance of Ceramic LCC's



Theta JA Ceramic Flatpacks/Cerpacks

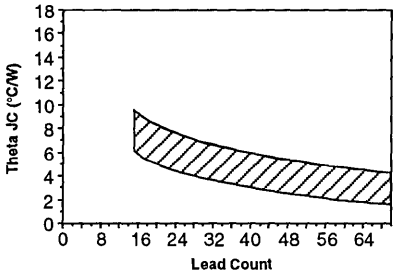


Theta JC Pin Grid Arrays

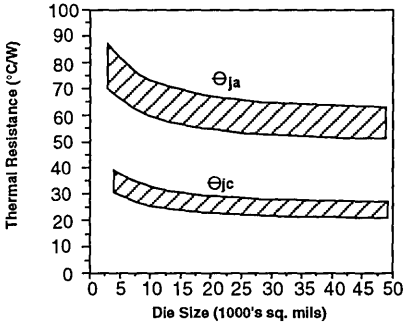


4

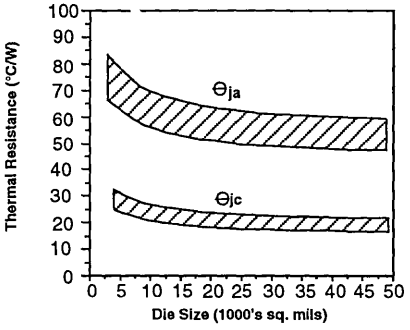
Theta JC Ceramic Flatpacks/Cerpacks



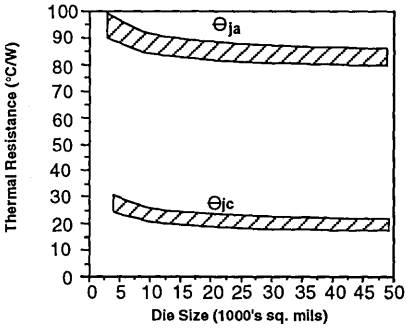
PLASTIC DIPS: 16,18 & 20 PINS



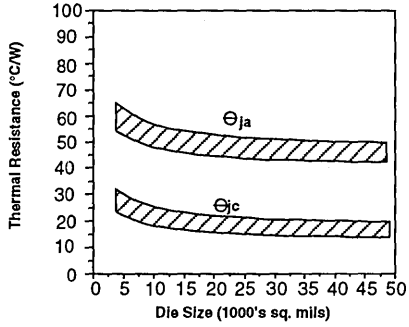
PLASTIC SOICS: 24,28 & 32 PINS



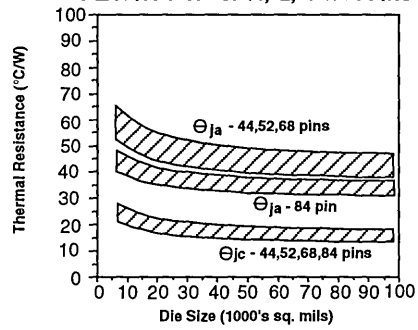
PLASTIC SOICS: 16 & 20 PINS



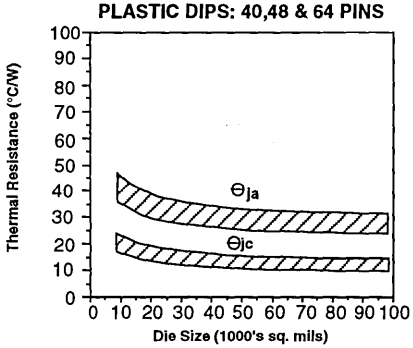
PLASTIC DIPS: 22,24 & 28 PINS



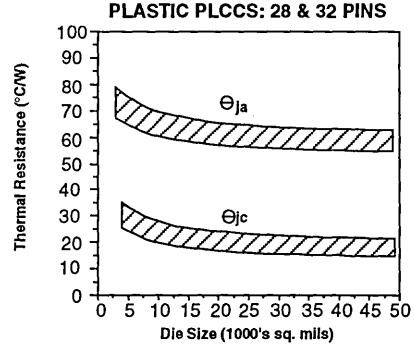
PLASTIC PLCCS: 44,52,68 & 84 PINS



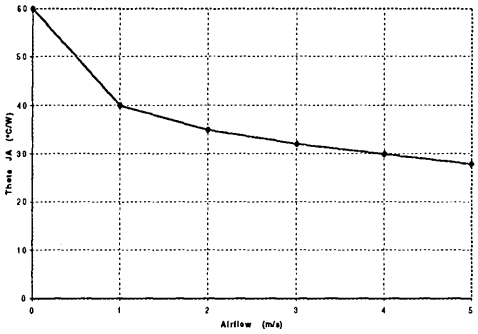
PLASTIC DIPS: 40,48 & 64 PINS



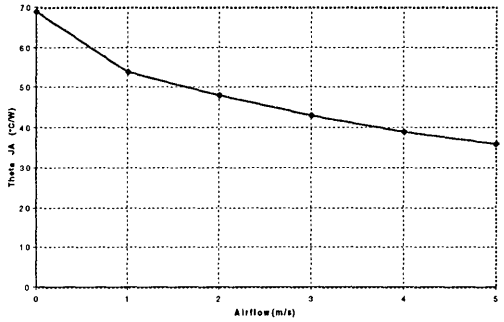
PLASTIC PLCCS: 28 & 32 PINS



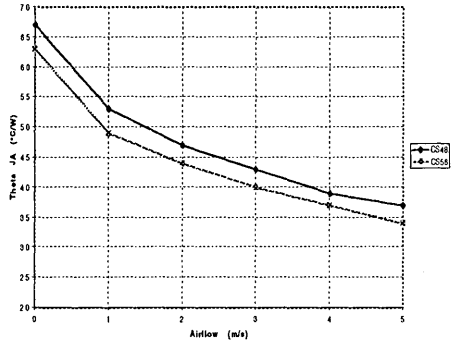
28 Pin Flatpack vs. Airflow



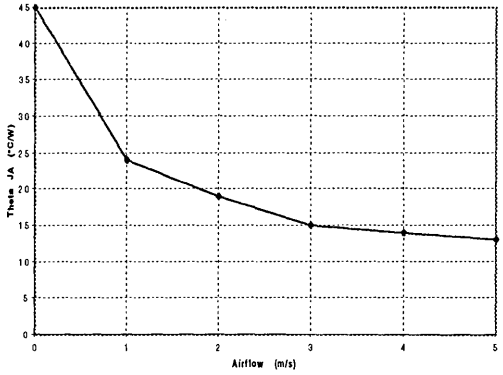
28 Pin Cerpack vs. Airflow



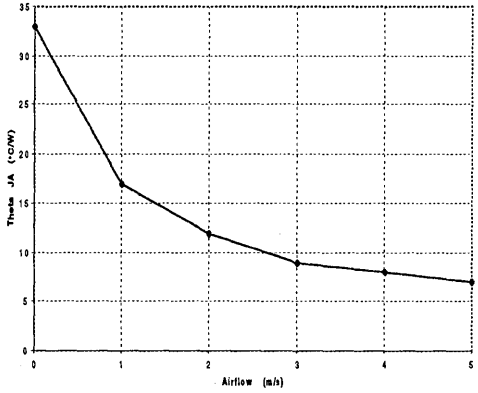
48/56 Pin Cerpack Theta JA vs. Airflow



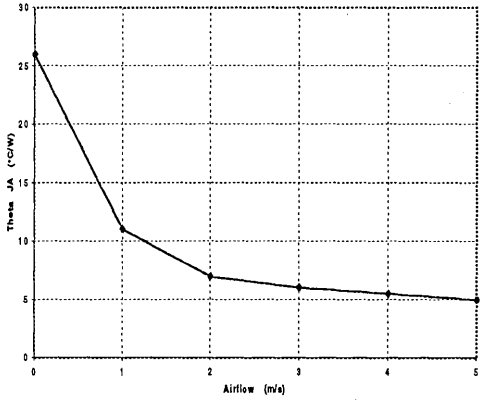
68 Pin PGA Theta JA vs. Airflow
Cavity Up without internal heatsink



84 Pin PGA Theta JA vs. Airflow
Cavity Down with CuW internal heatsink

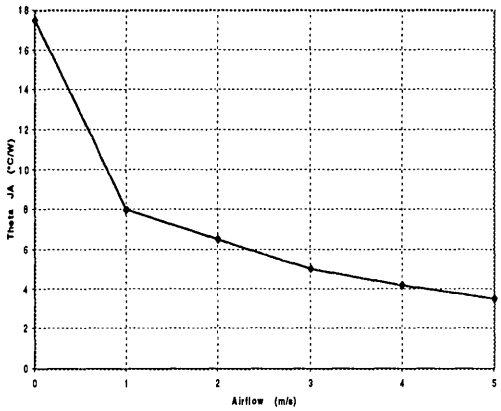


144 Pin PGA Theta JA vs. Airflow
Cavity Down with CuW internal heatsink

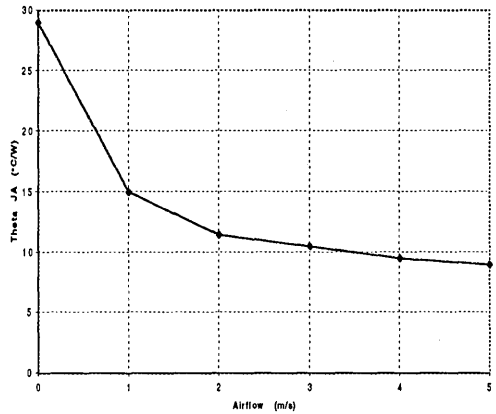


4

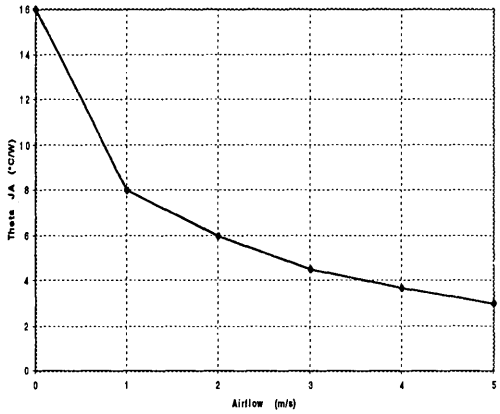
179 Pin PGA Theta JA vs. Airflow
Cavity Down with CuW internal heatsink



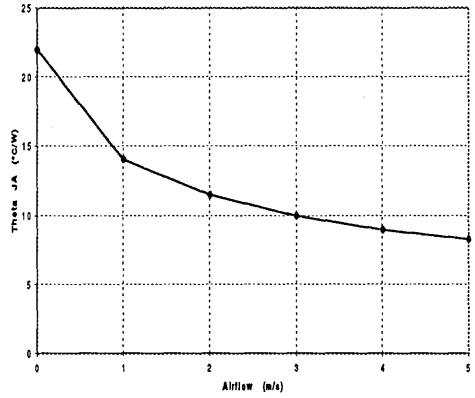
208 Pin PGA Theta JA vs. Airflow
Cavity Down without internal heatsink



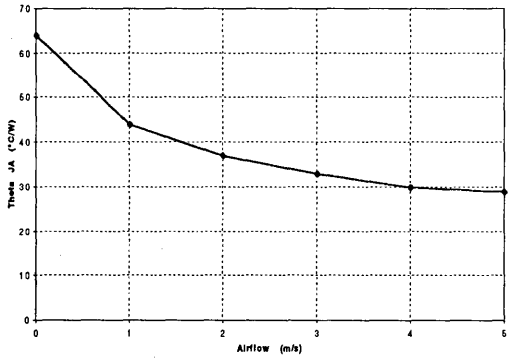
447 Pin PGA Theta JA vs. Airflow
Cavity Down with internal heatsink



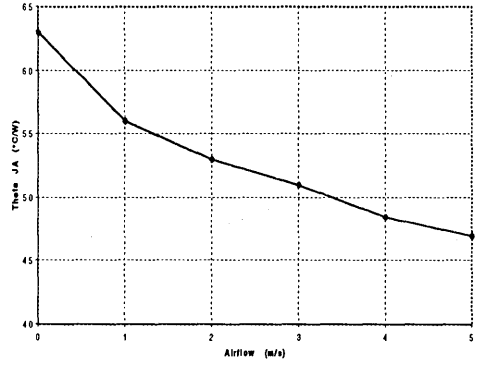
Theta JA vs. Airflow
84/160/208 lead MQIAD flatpack
28mm body



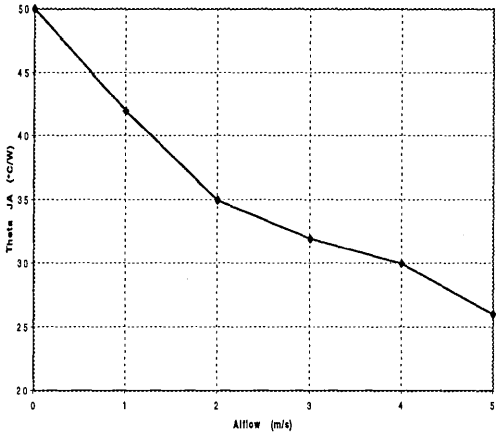
28 Pin Plastic Dip Theta JA vs. Airflow



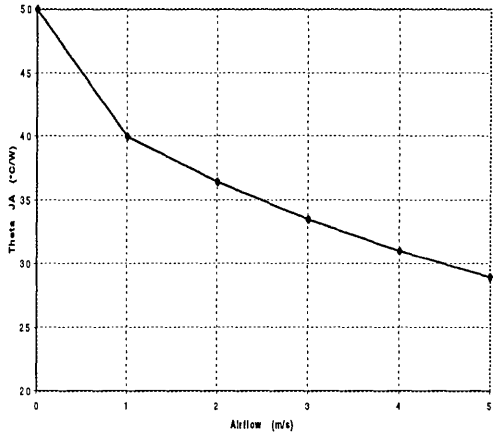
28 Pin SOJ Theta JA vs. Airflow



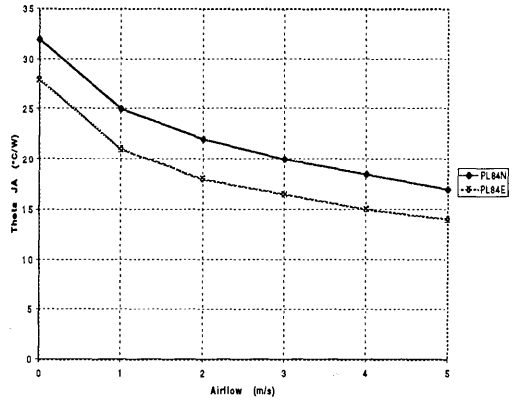
32 Pin SOJ Theta JA vs. Airflow



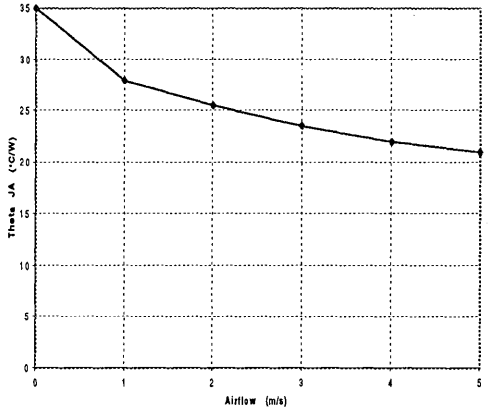
32 Pin PLCC vs. Airflow



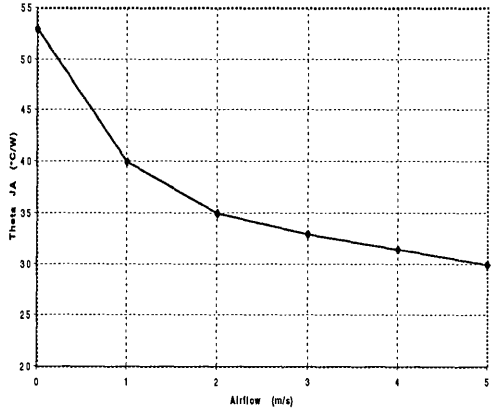
84 Pin PLCCs vs. Airflow
Normal & Enhanced



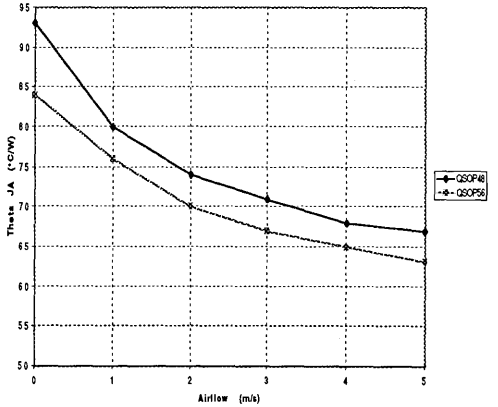
208 Pin PQFP vs. Airflow



Theta JA vs. Airflow
64/80/100 lead Thin Quad Flatpack
14mm body

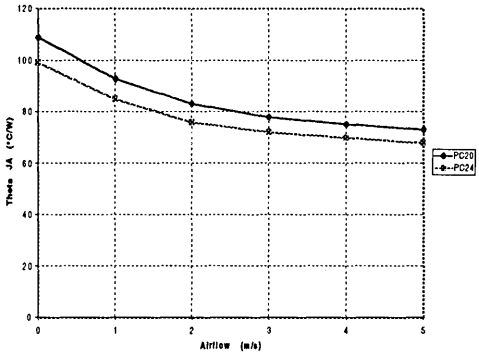


48/56 Pin QSOPs vs. Airflow
(.150" body)

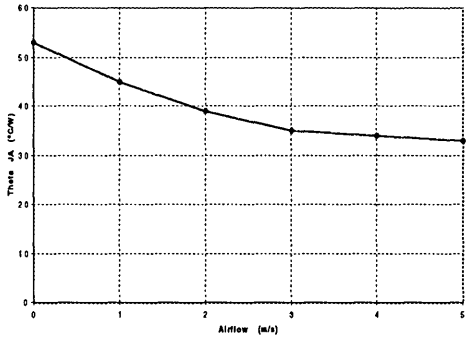


4

Theta JA vs. Airflow for 20/24 pin SSOPs



128 Pin Thin Quad Flatpack



PACKAGE DIAGRAM OUTLINE INDEX

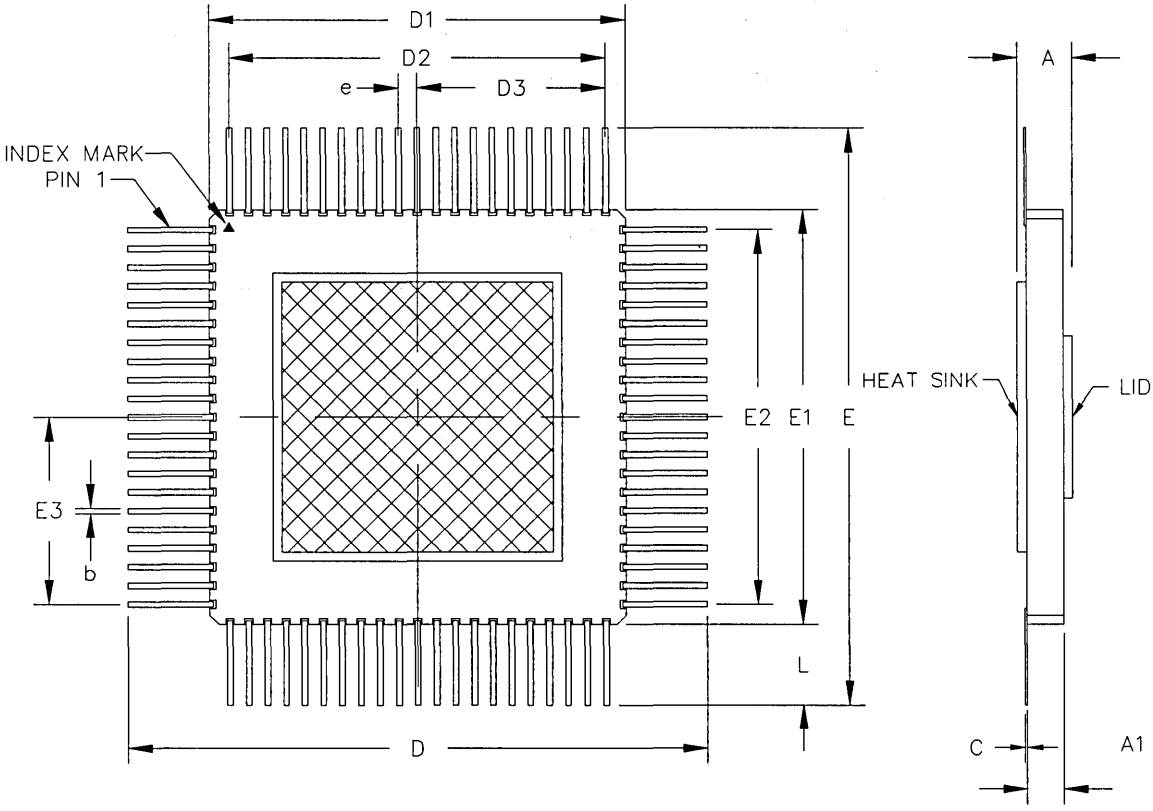
4

MODULE PACKAGE DIAGRAM OUTLINES

Module package diagrams are located at the back of each Subsystems data sheet.

FLATPACKS

84 LEAD QUAD FLATPACK (CAVITY DOWN)

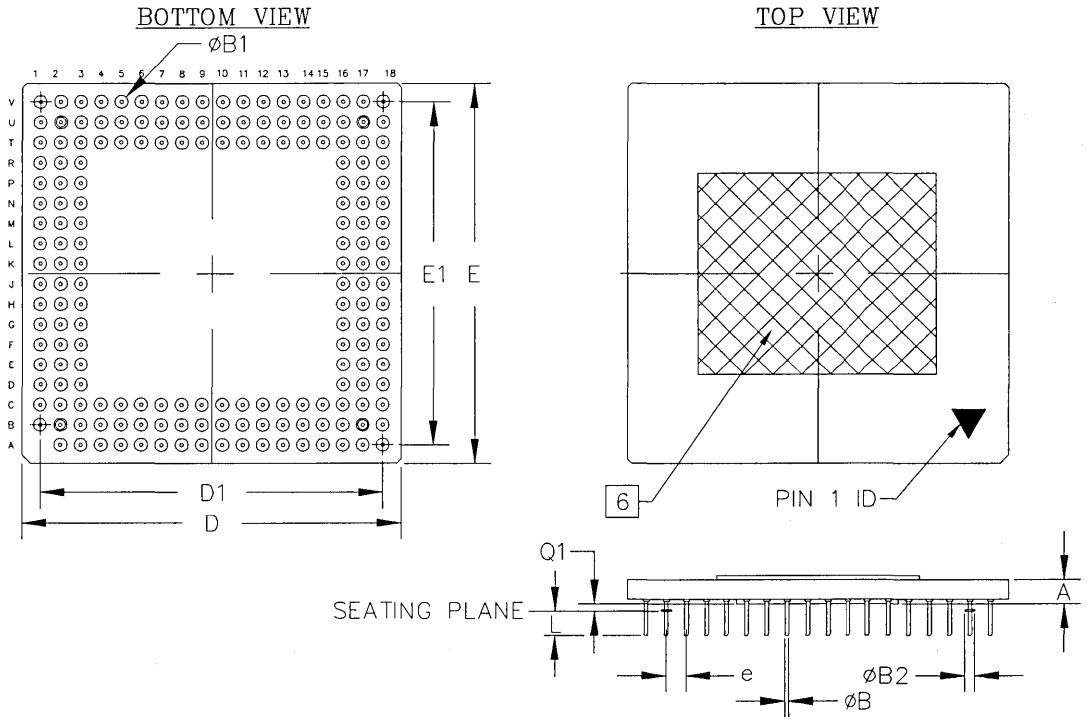


DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.135
A1	–	.105
b	.014	.020
C	.007	.011
D/E	1.940	1.960
D1/E1	1.140	1.160
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.390	.410
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS

179 PIN PGA (CAVITY DOWN)



DWG #	G179-1	
# OF PINS (N)	179	
SYMBOL	MIN	MAX
A	.082	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.840	1.880
D1/E1	1.700 BSC	
e	.100 BSC	
L	.120	.140
M	18	
Q1	.025	.060

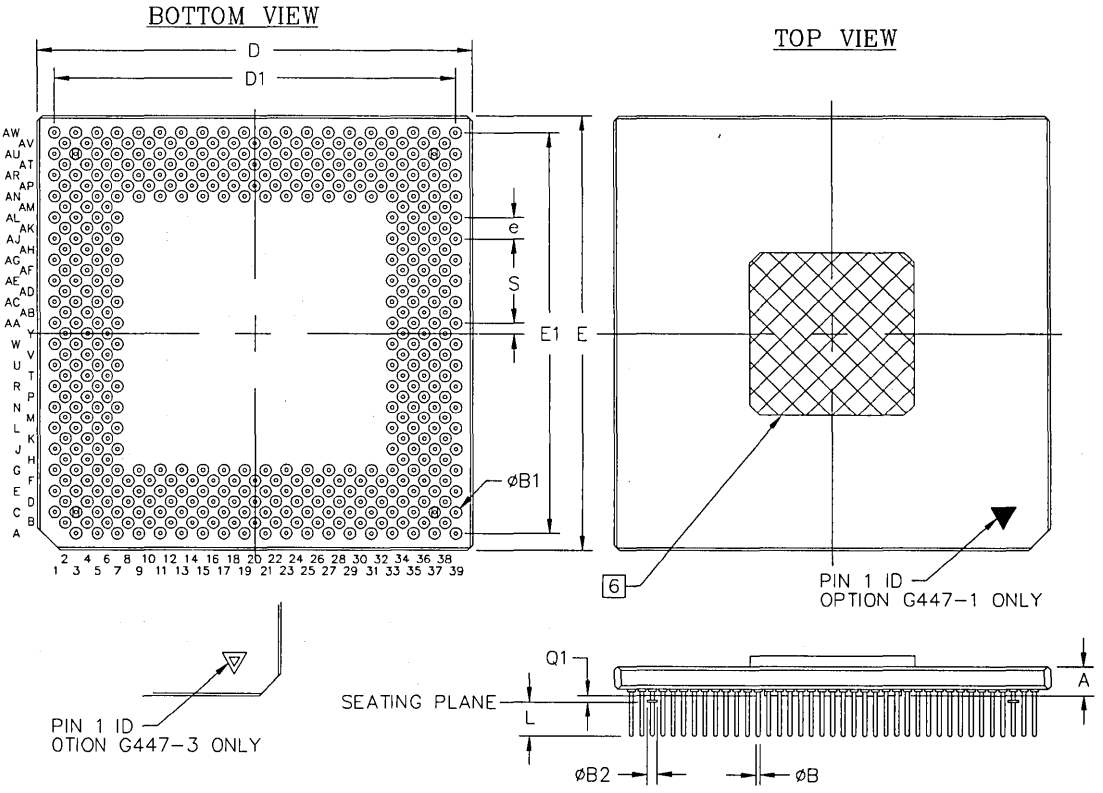
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.

[6] CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

PIN GRID ARRAYS (Continued)

447 PIN PGA (CAVITY DOWN)



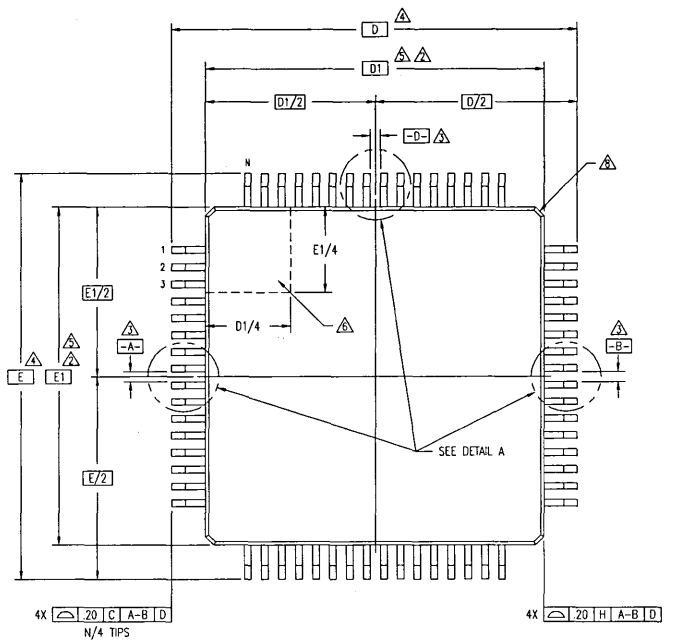
DWG #	G447-1		G447-3	
# OF PINS (N)	447		447	
SYMBOL	MIN	MAX	MIN	MAX
A	.070	.145	.070	.145
øB	.016	.020	.016	.020
øB1	.050	.060	.050	.060
øB2	.045	.055	.045	.055
D/E	2.040	2.080	2.040	2.080
D1/E1	1.900 BSC		1.900 BSC	
e	.100 BSC		.100 BSC	
L	.120	.140	.120	.140
M	39		39	
Q1	.030	.045	.045	.060
S	.050 BSC		.050 BSC	

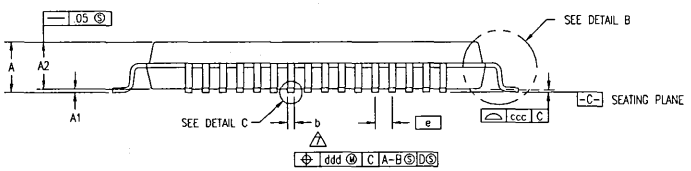
NOTES:
1. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK..

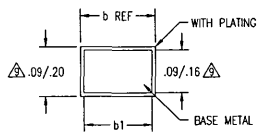
PACKAGE DIAGRAM OUTLINES

TQFP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	



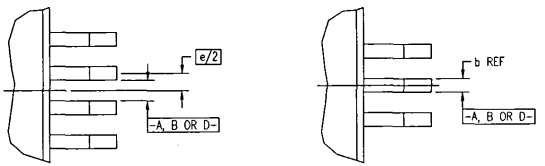




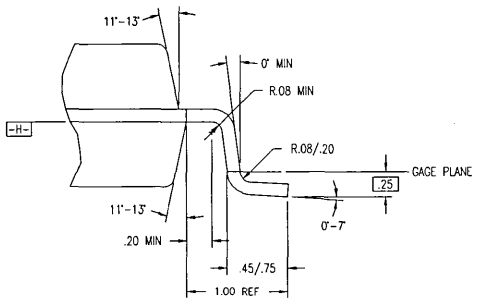
DETAIL C

EVEN LEAD SIDES

ODD LEAD SIDES



DETAIL A



DETAIL B

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL ANGULAR XX± ± XXX± XXXX±				
APPROVALS	DATE	TITLE PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM		
DRAWN dd	03/12/92			
CHECKED				
		SIZE C	DRAWING No. PSC-4036	REV 03
		DO NOT SCALE DRAWING		SHEET 1 OF 2

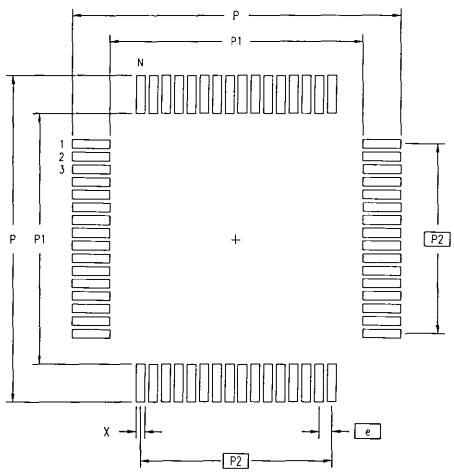
PACKAGE DIAGRAM OUTLINES

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN dd	03/12/92
CHECKED	

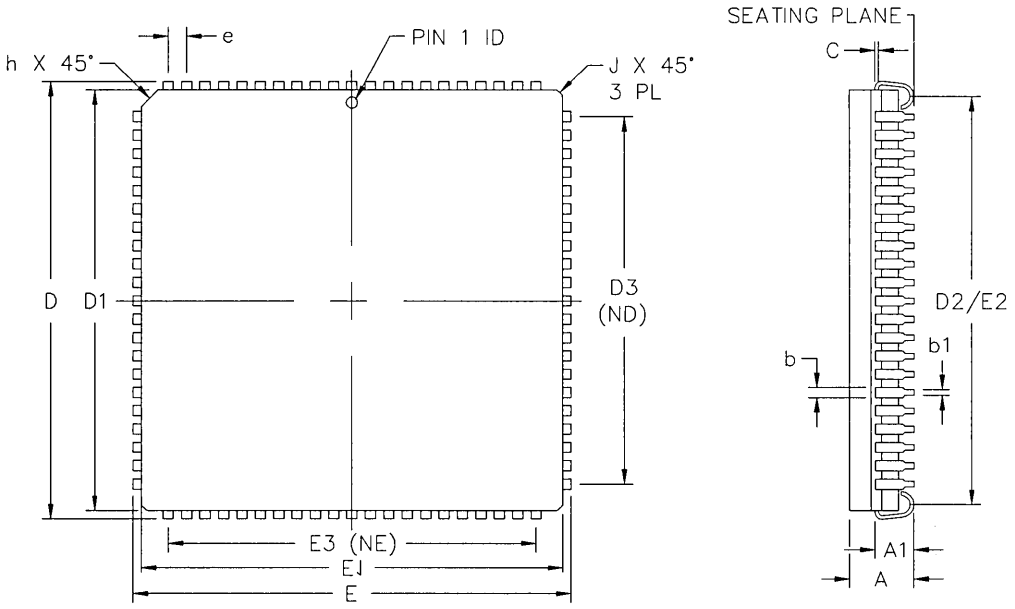
TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C | DRAWING No. PSC-4036 | REV 03

DO NOT SCALE DRAWING | SHEET 2 OF 2

MQUADS ®

84 LEAD MQUAD (J-BEND, CAVITY DOWN)



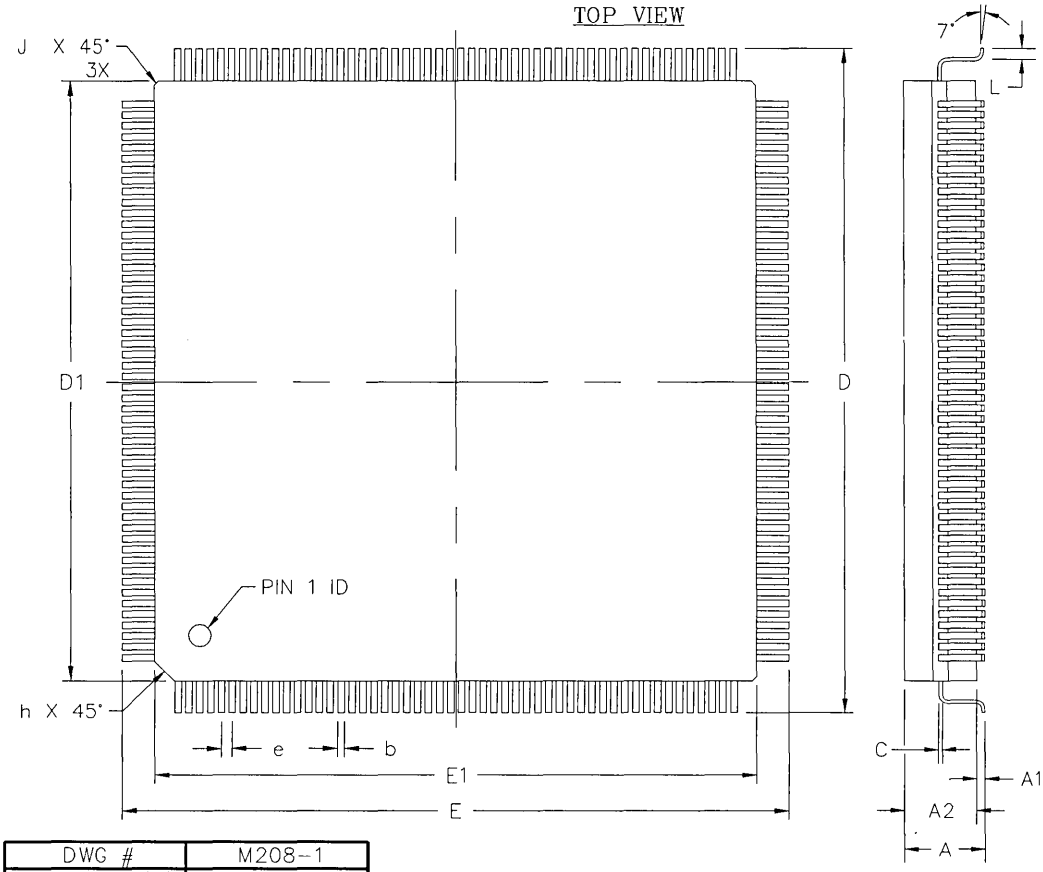
DWG #	M84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.165	.180
A1	.094	.114
b	.026	.032
b1	.013	.021
C	.008	.012
D/E	1.185	1.195
D1/E1	1.140	1.150
D2/E2	1.090	1.130
D3/.E3	1.000 BSC	
e	.050 BSC	
h	.045 REF	
J	.015 REF	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
4. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

MQUADS ® (Continued)

208 LEAD MQUAD (CAVITY DOWN)



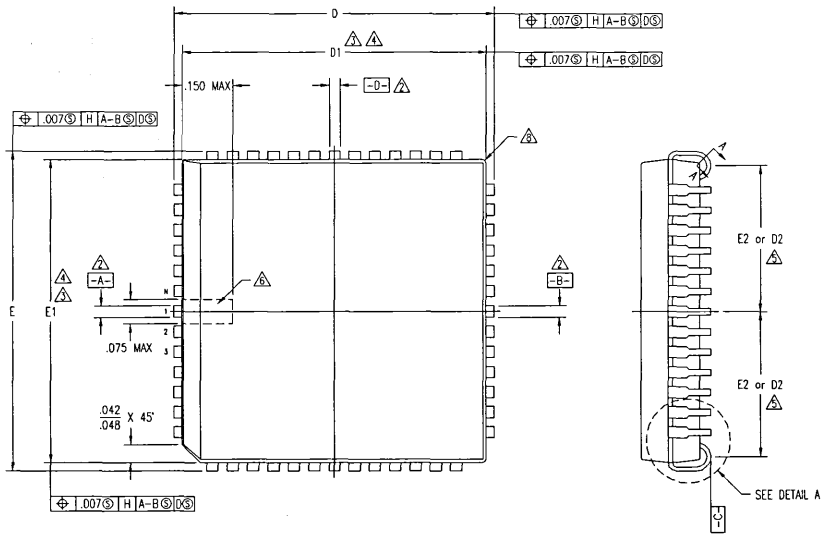
DWG #	M208-1	
# OF LDS (N)	208	
SYMBOL	MIN	MAX
A	3.50	3.86
A1	.25	.51
A2	3.17	3.43
b	.22	.35
C	.13	.20
D/E	30.50	30.70
D1/E1	27.59	27.79
e	.50 BSC	
h	.89 REF	
J	.20 REF	
L	.40	.60
ND/NE	52	

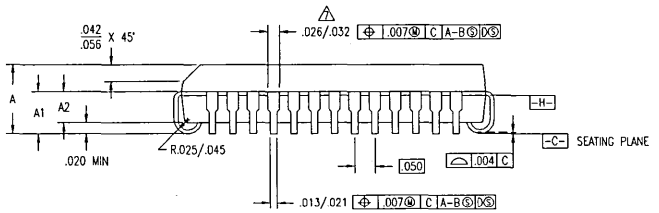
NOTES:

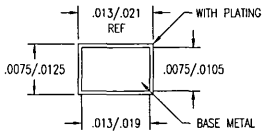
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 SHOULD BE MEASURED FORM THE BOTTOM OF THE PACKAGE.
4. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

PLCC

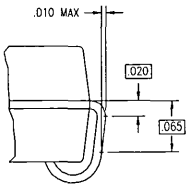
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

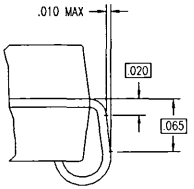






SECTION A–A





DETAIL A

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN AA	08/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	SHEET 1 OF 3

PACKAGE DIAGRAM OUTLINES

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	05	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1				DWG #	J44-1				DWG #	J52-1				DWG #	J68-1				DWG #	J84-1			
SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.165	.172	.180		.165	.172	.180		.165	.172	.180		.165	.172	.180		.165	.172	.180		.165	.172	.180	
A1	.095	.105	.115		.095	.105	.115		.095	.105	.115		.095	.105	.115		.095	.105	.115		.095	.105	.115	
A2	.062	–	.083		.062	–	.083		.062	–	.083		.062	–	.083		.062	–	.083		.059	–	.080	
D	.485	.490	.495		.685	.690	.695		.785	.790	.795		.985	.990	.995		.985	.990	.995		1.185	1.190	1.195	
D1	.450	.453	.456	3,4	.650	.653	.656	3,4	.750	.753	.756	3,4	.950	.953	.956	3,4	.950	.953	.956	3,4	1.150	1.154	1.156	3,4
D2	.195	.205	.215	5	.295	.305	.315	5	.345	.355	.365	5	.445	.455	.465	5	.445	.455	.465	5	.545	.555	.565	5
E	.485	.490	.495		.685	.690	.695		.785	.790	.795		.985	.990	.995		.985	.990	.995		1.185	1.190	1.195	
E1	.450	.453	.456	3,4	.650	.653	.656	3,4	.750	.753	.756	3,4	.950	.953	.956	3,4	.950	.953	.956	3,4	1.150	1.154	1.156	3,4
E2	.191	.205	.219	5	.291	.305	.319	5	.341	.355	.369	5	.441	.455	.469	5	.441	.455	.469	5	.541	.555	.569	5
N	28				44				52				68				68				84			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN AA	08/15/89
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

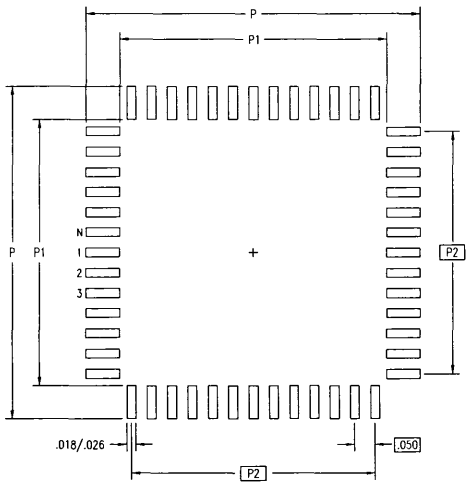
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING SHEET 2 OF 3

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL ANGULAR		2975 Stender Way, Santa Clara, CA 95054
XX± ±		PHONE: (408) 727-6116
XXX±		FAX: (408) 492-8674 TWX: 910-338-2070
XXXX±		
APPROVALS	DATE	TITLE: PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN AA	08/15/89	
CHECKED		
		SIZE C / DRAWING No. PSC-4008 / REV 06
		DO NOT SCALE DRAWING / SHEET 3 OF 3

IDT RISC PROCESSING COMPONENTS

THE COMPLETE RISC SOLUTION

Integrated Device Technology, Inc. is dedicated to providing complete RISC design solutions by combining expertise in silicon processes with leadership products in development systems and software. Long an industry leader in the fastest static RAMs and high-speed logic, IDT now offers RISC system building blocks comprised of components and board-level subsystems.

As a semiconductor partner with MIPS Computer Systems, IDT has established a leadership position in the RISC marketplace by supplying the fastest CPUs at 40MHz, pioneering RISC CPU Subsystem™ modules, and offering cost-effective development tools and software.

The MIPS architecture has become an industry standard and has been adopted by over 100 leading OEM manufacturers including DEC, Sony, Tandem, NEC, CDC, Adobe, Siemens, Nixdorf, Honeywell Bull and Silicon Graphics. The MIPS ISA (Instruction Set Architecture) has been selected by JIAWG as the 32-bit microprocessor standard for military avionics.

RISComponent™ FAMILY OVERVIEW

The R3000 Family consists of the R3000 RISC CPU, the R3041, R3051/52, R3071, R3081 and R36100 RISControllers™. The R3000 processor is a derivative of the R2000A, the first commercially-available RISC processor introduced in 1985. The R3001 RISController and the R3051 family, including the R3041 and R3081, are versions of the processor tailored for embedded control and low-cost workstations. The R3500 integrates floating-point capability onto the R3000 pinout. The R4000 is the third generation of the MIPS RISC architecture that sets a new performance standard for the 1990s.

THE IDT79R3000 CPU

The R3000 processor consists of two tightly-coupled processors implemented on a single chip.

The first processor is a full 32-bit Harvard Architecture CPU consisting of 32 registers, an integer ALU, a single-cycle shifter, and a multiplier/divider. The second processor is a system control coprocessor containing a Translation Lookaside Buffer (TLB) and control registers to support a virtual memory space of 4GB and separate instruction and Data caches.

The R3000 CPU features:

- Full 32-bit operation
- Three instruction formats
- Efficient 5-stage pipeline
- On-chip cache control
- On-chip Memory Management Unit
- Multiprocessor capability

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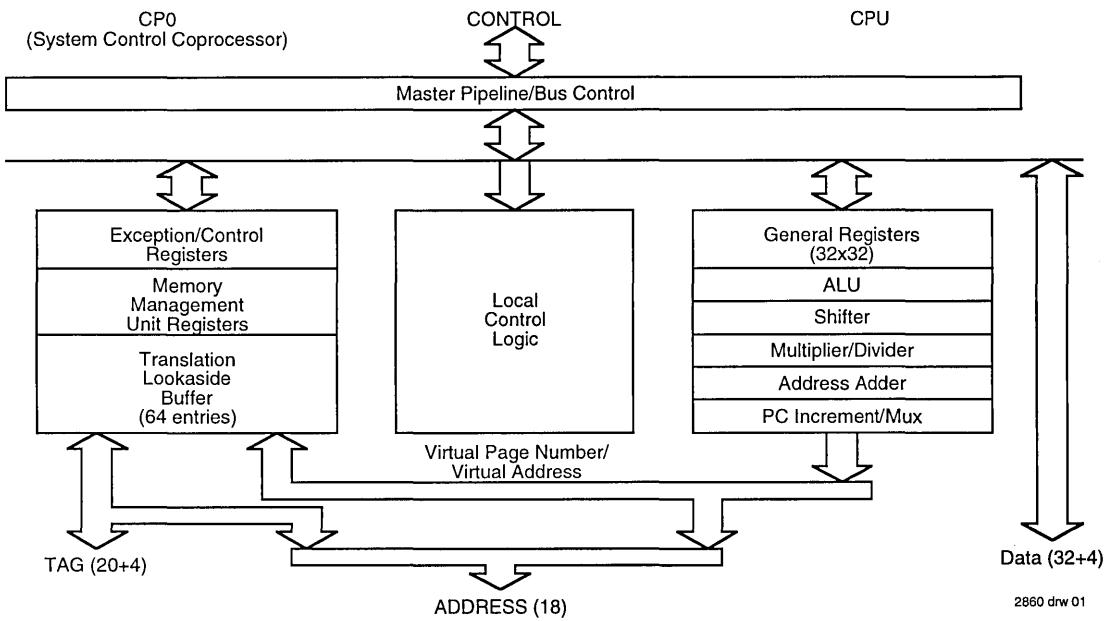

Figure 1. IDT79R3000 Processor

THE R3051 FAMILY OF RISControllers™

The IDT79R3051 Family is a derivative of the R3000, featuring a high level of integration and targeted to high-performance but cost-sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost rather than to increase the inherent performance of the integer engine. Thus, the R3051 family is able to offer 35 MIPS of integer performance at 40MHz without requiring external SRAM or caches.

The R3041 extends the range of price/performance achievable with the R3051 family, by dramatically lowering the cost of using the MIPS architecture. The R3041 has been designed to achieve minimal system and components cost, yet maintain the high performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the R3051 and R3081.

The R3081 extends the capabilities of the R3051 family by integrating the additional resources into the same pinout. The R3081 thus extends the range of applications addressed by the R3051 family and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs according to the price/performance goals of the end system.

THE IDT79R4000 CPU

The R4000 is the third generation of MIPS RISC technology and establishes a new performance standard for RISC processors for the 1990s. The R4000 extends the performance range served by the MIPS architecture and, thereby, provides a migration path to applications served by the R3051 RISController family.

This third generation processor maintains full binary compatibility with applications executing on the R2000/R3000 and IDT's RISController family, while achieving substantially higher performance. The key to this performance is both the architecture/implementation of the processor and the high level of integration achieved in a single chip. The R4000 contains the RISC integer unit, floating-point unit, MMU, 8K of I- and D-cache, along with multiprocessing support such as direct control of optional secondary caches. To achieve performance levels capable of over 50 VAX MIPS sustained performance, the R4000 utilizes technology such as super-pipelining to exploit 2-level instruction parallelism with no issue restrictions. The R4000 presents a balanced architectural approach to achieve a wide range of price/performance goals.

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Integrated Device Technology, Inc.

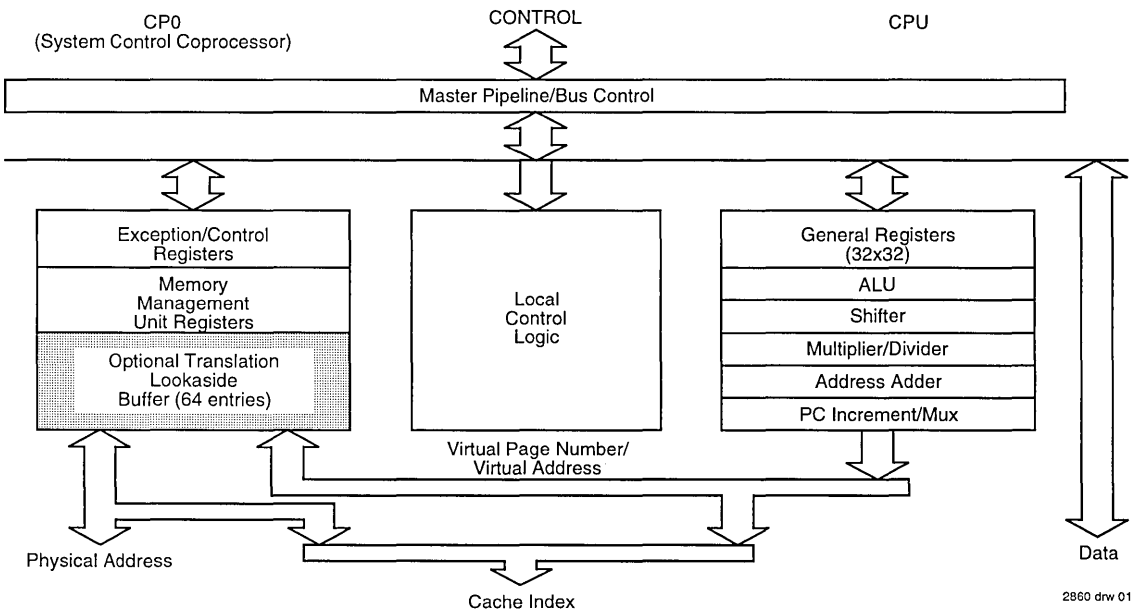
RISC CPU CORE

R3000A Core for RISController Devices

FEATURES:

- Enhanced instruction set compatible R3000A Core for integrated RISControllers
- Integrates well with R3010A Core Hardware Floating Point Accelerator
- Full 32-bit Operation—Thirty-two 32-bit registers and all instructions and addresses are 32-bit.
- Efficient Pipelining—The CPU's 5-stage pipeline design assists in obtaining an execution rate approaching one instruction per cycle. Pipeline stalls and exceptions are handled precisely and efficiently.
- Integrated Cache Control for On-Chip Caches—The CPU core contains a high-bandwidth memory interface that handles separate Instruction and Data Caches. Both caches are accessed during a single CPU cycle. All cache control is integrated into the core, allowing high-speed execution.
- "E" versions feature Memory Management Unit, including a fully-associative, 64-entry Translation Look-aside Buffer (TLB). This provides fast address translation for virtual-to-physical memory mapping of the 4GB virtual address space.
- Dynamically able to switch between Big- and Little-Endian byte ordering conventions.
- Software compatible with all R3000 devices. This insures a wide range of development support, including compilers, operating systems, libraries, and applications software.
- High-speed 0.6μ CMOS technology.
- 50MHz clock rates yield up to 40VUPS sustained throughput.
- Supports independent multi-word block refill of both the instruction and data caches.
- Supports concurrent refill and execution of instructions.
- Partial word stores executed as read-modify-write operations.
- 6 external interrupt inputs, 2 software interrupts, with single cycle latency to exception handler routine.

R3000A CORE BLOCK DIAGRAM



DESCRIPTION

The R3000A RISC Microprocessor Core consists of two tightly-coupled processors. The first processor is a full 32-bit CPU based on RISC (Reduced Instruction Set Computer) principles to achieve a new standard of microprocessor price/performance. The second processor is a system control coprocessor, called CP0, containing an optional fully-associative 64-entry TLB (Translation Look-aside Buffer), MMU (Memory Management Unit) and control registers, supporting a 4GB virtual memory subsystem, and a Harvard Architecture Cache Controller achieving a bandwidth of 400MB/second using integrated cache memory.

This data sheet provides an overview of the features and architecture of the R3000A core. This core is integrated into various members of the IDT RISController family, such as the R3041, R3051, and R3081. Detail on those specific devices is found in separate data sheets and user's manuals.

R3000A CPU Registers

The R3000A CPU provides 32 general-purpose 32-bit registers, a 32-bit Program Counter, and two 32-bit registers which hold the results of integer multiply and divide operations. Only two of the 32 general registers have a special purpose: register r0 is hard-wired to the value "0", which is a useful constant, and register r31 is used as the link register in jump-and-link instructions (return address for subroutine calls).

The CPU registers are shown in Figure 2. Note that there is no Program Status Word (PSW) register shown in this figure: the functions traditionally provided by a PSW register are instead provided in the Status and Cause registers incorporated within the System Control Coprocessor (CP0).

Instruction Set Overview

All R3000A instructions are 32 bits long, and there are only three instruction formats. This approach simplifies instruction decoding, thus minimizing instruction execution time. The R3000A core initiates a new instruction on every run cycle, and is able to complete an instruction on almost every clock cycle. The only exceptions are the Load instructions and Branch instructions, which each have a single cycle of latency associated with their execution. Note, however, that in the majority of cases the compilers are able to fill these latency cycles with useful instructions which do not require the result of the previous instruction. This effectively eliminates these latency effects.

The actual instruction set of the CPU was determined after extensive simulations to determine which instructions should be implemented in hardware, and which operations are best synthesized in software from other basic instructions.

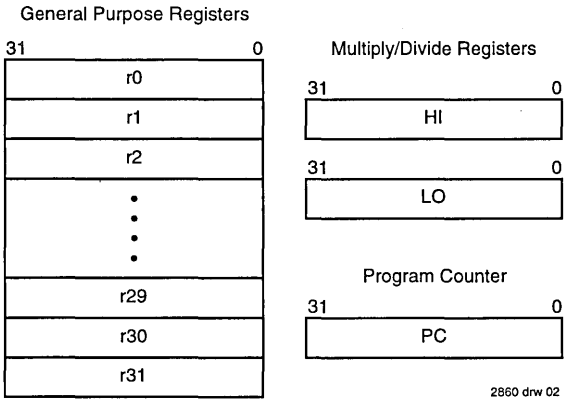


Figure 2. R3000A CPU Registers

The R3000A instruction set can be divided into the following groups:

- **Load/Store** instructions move data between memory and general registers. They are all I-type instructions, since the only addressing mode supported is base register plus 16-bit, signed immediate offset.

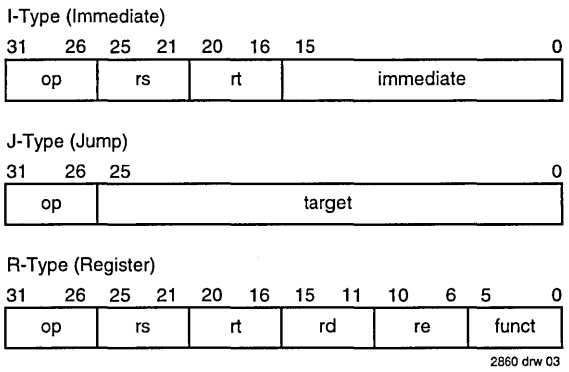


Figure 3. R3000A Instruction Formats

The Load instruction has a single cycle of latency, which means that the data being loaded is not available to the instruction immediately after the load instruction. The compiler will fill this delay slot with either an instruction which is not dependent on the loaded data, or with a NOP instruction. There is no latency associated with the store instruction.

Loads and Stores can be performed on byte, half-word, word, or non-aligned word data (32-bit data not aligned on a modulo-4 address). The CPU cache is constructed as a write-through cache.

- **Computational** instructions perform arithmetic, logical and shift operations on values in registers. They occur in both R-type (both operands and the result are registers) and I-type (one operand is a 16-bit immediate) formats. Note that computational instructions are three operand instructions; that is, the result of the operation can be stored into a different register than either of the two

operands. This means that operands need not be overwritten by arithmetic operations. This results in a more efficient use of the large register set.

- **Jump and Branch** instructions change the control flow of a program. Jumps are always to a paged absolute address formed by combining a 26-bit target with four bits of the Program counter (J-type format, for subroutine calls), or 32-bit register byte addresses (R-type, for returns and dispatches). Branches have 16-bit offsets relative to the program counter (I-type). Jump and Link instructions save a return address in Register 31. The R3000A instruction set features a number of branch conditions. Included is the ability to compare a register to zero and branch, and also the ability to branch based on a comparison between two registers. Thus, net performance is increased since software does not have to perform arithmetic instructions prior to the branch to set up the branch conditions.
- **Coprocessor** instructions perform operations in the coprocessors. Coprocessor Loads and Stores are I-type. Coprocessor computational instructions have coprocessor-dependent formats (see coprocessor manuals).
- **Coprocessor 0** instructions perform operations on the System Control Coprocessor (CP0) registers to manipulate the memory management and exception handling facilities of the processor.
- **Special** instructions perform a variety of tasks, including movement of data between special and general registers, system calls, and breakpoint. They are always R-type.

R3000A INSTRUCTION SUMMARY

OP	Description	OP	Description
	Load/Store Instructions		**Multiply/Divide Instructions**
LB	Load Byte	MULT	Multiply
LBU	Load Byte Unsigned	MULTU	Multiply Unsigned
LH	Load Halfword	DIV	Divide
LHU	Load Halfword Unsigned	DIVU	Divide Unsigned
LW	Load Word	MFHI	Move From HIGH
LWL	Load Word Left	MTHI	Move To HIGH
LWR	Load Word Right	MFLO	Move From LOW
SB	Store Byte	MTLO	Move To LOW
SH	Store Halfword		
SW	Store Word		**Jump and Branch Instructions**
SWL	Store Word Left	J	Jump
SWR	Store Word Right	JAL	Jump and Link
		JR	Jump to Register
	Arithmetic Instructions	JALR	Jump and Link Register
	(ALU Immediate)	BEQ	Branch on Equal
ADDI	Add Immediate	BNE	Branch on Not Equal
ADDIU	Add Immediate Unsigned	BLEZ	Branch on Less than or Equal to Zero
SLTI	Set on Less Than Immediate	BGTZ	Branch on Greater Than Zero
SLTIU	Set on Less Than Immediate	BLTZ	Branch on Less Than Zero
	Unsigned	BGEZ	Branch on Greater than or
ANDI	AND Immediate		Equal to Zero
ORI	OR Immediate	BLTZAL	Branch on Less Than Zero and Link
XORI	Exclusive OR Immediate	BGEZAL	Branch on Greater than or Equal to
LUI	Load Upper Immediate		Zero and Link
			Special Instructions
	Arithmetic Instructions	SYSCALL	System Call
	(3-operand, register-type)	BREAK	Break
ADD	Add		
ADDU	Add Unsigned		**Coprocessor Instructions**
SUB	Subtract	LWCz	Load Word from Coprocessor
SUBU	Subtract Unsigned	SWCz	Store Word to Coprocessor
SLT	Set on Less Than	MTCz	Move To Coprocessor
MFCz	Move From Coprocessor		
SLTU	Set on Less Than Unsigned	CTCz	Move Control to Coprocessor
AND	AND	CFCz	Move Control From Coprocessor
OR	OR	COPz	Coprocessor Operation
XOR	Exclusive OR	BCzT	Branch on Coprocessor z True
NOR	NOR	BCzF	Branch on Coprocessor z False
	Shift Instructions		**System Control Coprocessor**
SLL	Shift Left Logical		**(CP0) Instructions**
SRL	Shift Right Logical	MTC0	Move To CP0
SRA	Shift Right Arithmetic	MFC0	Move From CP0
SLLV	Shift Left Logical Variable	TLBR	Read indexed TLB entry
SRLV	Shift Right Logical Variable	TLBWI	Write Indexed TLB entry
SRAV	Shift Right Arithmetic Variable	TLBWR	Write Random TLB entry
		TLBP	Probe TLB for matching entry
		RFE	Restore From Exception

2860 tbl 01

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Table 1 lists the instruction set of the R3000A processor core.

R3000A System Control Coprocessor (CP0)

The R3000A core can operate with up to four tightly-coupled coprocessors (designated CP0 through CP3). The System Control Coprocessor (or CP0), is incorporated on the R3000A core and supports the virtual memory system and exception handling functions of the processor. The virtual memory system is implemented using a Translation Look-aside Buffer and a group of programmable registers as shown in Figure 3.

SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS

The CP0 registers shown in Figure 3 are used to control the memory management and exception handling capabilities of the R3000A. Table 2 provides a brief description of the registers common to most devices using the core. Note, however, that certain devices (e.g. non-E versions, the R3081, and R3041) implement slightly different sets of these registers, as described in their user's manuals.

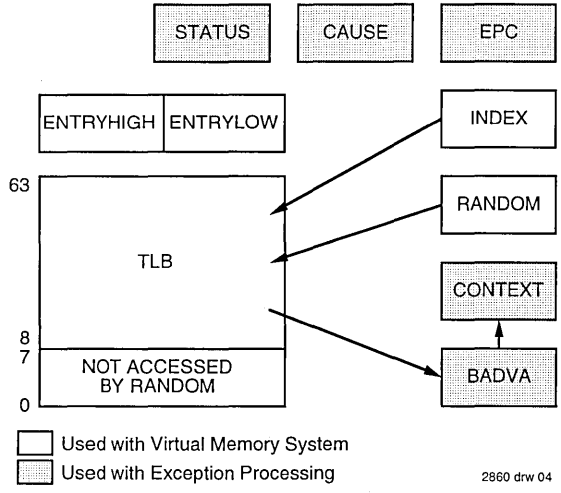

Figure 4. The System Coprocessor Registers

SYSTEM CONTROL COPROCESSOR (CP0) REGISTERS

Register	Description
EntryHIGH	HIGH half of a TLB entry
EntryLOW	LOW half of a TLB entry
Index	Programmable pointer into TLB array
Random	Pseudo-random pointer into TLB array
Status	Mode, interrupt enables, and diagnostic status info
Cause	Indicates nature of last exception
EPC	Exception Program Counter
Context	Pointer into kernel's virtual Page Table Entry array
BadVA	Most recent bad virtual address
PRId	Processor revision identification (Read only)

2860 tbl 02

Memory Management System

The R3000A has an addressing range of 4gB. However, since most R3000A systems implement a physical memory smaller than 4gB, theR3000A provides for the logical expansion of memory space by translating addresses composed in a large virtual address space into available physical memory address. The 4gB address space is divided into 2gB which can be accessed by both the users and the kernel, and 2gB for the kernel only.

The actual virtual to physical translation mechanism is either through an on-chip translation lookaside buffer (TLB), or through a fixed translation mechanism, depending on the device ("E" vs. non-"E" devices). These mechanisms are explained in the data sheets and user's manuals for those devices.

R3000A Operating Modes

TheR3000A has two operating modes: User mode and Kernel/mode. The R3000A normally operates in the User mode until an exception is detected forcing it into the Kernel mode. It remains in the Kernel mode until a Restore From Exception (RFE) instruction is executed. The manner in which memory addresses are translated or mapped depends on the operating mode of the R3000A, and whether the device implements an on-chip TLB.

User Mode—in this mode, a single, uniform virtual address space (kuseg) of 2gB is available. Each virtual address is extended with a 6-bit process identifier field to form unique virtual addresses. The actual virtual to physical address mapping is either done via a fixed translation, or through the TLB, depending on the device.

Kernel Mode—four separate segments are defined in this mode:

- *kuseg*—when in the kernel mode, references to this segment are treated just like user mode references, thus streamlining kernel access to user data.
- *kseg0*—references to this 512mB segment use cache memory but are not mapped through the optional TLB. Instead, they always map to the first 0.5gB of physical address space, whether or not the device contains an on-chip TLB.
- *kseg1*—references to this 512mB segment are not mapped through the TLB and do not use the cache. Instead, they are hard-mapped into the same 0.5gB segment of physical address space as kseg0.
- *kseg2*—references to this 1gB segment are either mapped through the TLB (with use of the cache determined by bit settings within the TLB entries) or through a predetermined mapping (non-E versions; all references go through the cache).

R3000A Pipeline Architecture

The execution of a single R3000A instruction consists of five primary steps:

1) **IF** — Fetch the instruction (I-Cache).
2) **RD** — Read any required operands from CPU registers while decoding the instruction.
3) **ALU** — Perform the required operation on instruction operands.
4) **MEM**— Access memory (D-Cache).
5) **WB** — Write back results to register file.

Each of these steps requires approximately one CPU cycle, as shown in Figure 4 (parts of some operations overlap into another cycle while other operations require only 1/2 cycle).

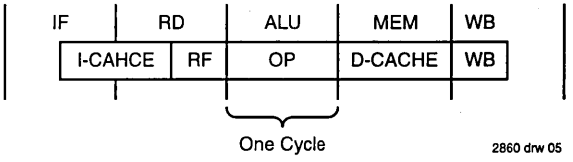

Figure 5. R3000A Instruction Pipeline

INSTRUCTION EXECUTION

The R3000A uses a 5-stage pipeline to achieve an instruction execution rate approaching one instruction per CPU cycle. Thus, execution of five instructions at a time are overlapped as shown in Figure 5.

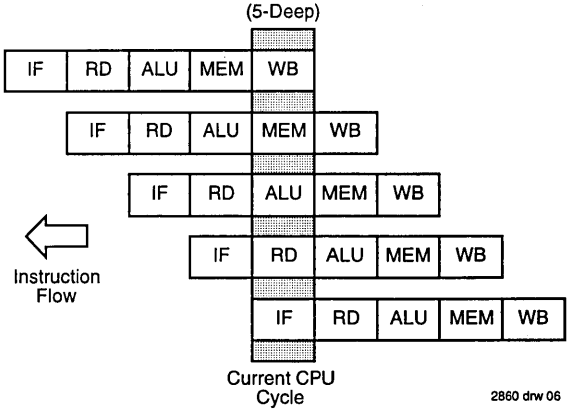

Figure 6. R3000A Execution Sequence

This pipeline operates efficiently because different CPU resources (address and data bus accesses, ALU operations, register accesses, and so on) are utilized on a non-interfering basis.

Memory System Hierarchy

A primary goal of systems employing RISC techniques is to minimize the average number of cycles each instruction requires for execution. In order to achieve this goal, RISC processors incorporate a number of RISC techniques, including a compact and uniform instruction set, a deep instruction pipeline (as described above), and utilization of optimizing compilers.

Figure 6 illustrates a memory system that supports the significantly greater memory bandwidth required to take full advantage of the R3000A's performance capabilities. The key features of this system are:

- **On-chip Cache Memory**—Local, high-speed memory (called cache memory) is used to hold instructions and data that is repetitively accessed by the CPU (for example, within a program loop) and thus reduces the number of references that must be made to the slower-speed main memory.
- **Separate Caches for data and Instructions**—Even with high-speed caches, memory speed can still be a limiting factor because of the fast cycle time of a high-performance microprocessor. The R3000A supports separate caches for instructions and data and alternates accesses of the two caches during each CPU cycle. Thus, the processor can obtain data and instructions at the cycle rate of the CPU.
- **Write Buffer**—in order to ensure data consistency, all data that is written to the data cache must also be written out to main memory. The cache write model used by the R3000A is that of a write-through cache; that is, all data written by the CPU is immediately written into the main memory. To relieve the CPU of this responsibility (and the inherent performance burden) the R3000A supports an interface to an on-chip write buffer. Thus, the R3000A core continues execution at high-speed, while the store data is retired at the slower memory rate.
- **Read Buffer**—The IDT RISController family typically incorporates an on-chip read buffer. This enables the system interface to match the speed of the high-speed execution core with the slower speed of a low-cost memory system, while still optimizing performance. This small on-chip FIFO enables the CPU to refill the cache and execute instructions even while additional instructions are being read from memory. This process is called instruction streaming.

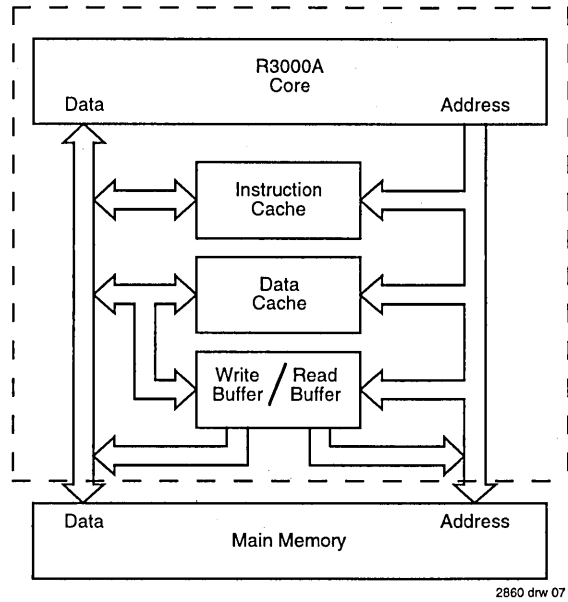

Figure 7. An R3000A System with a High-Performance Memory System

ADVANCED FEATURES

The R3000A offers a number of additional features such as the ability to swap the instruction and data caches, facilitating diagnostics and cache flushing. Another feature isolates the caches, which forces cache hits to occur regardless of the contents of the tag fields. The R3000A allows the processor to execute user tasks of the opposite byte ordering (endianness) of the operating system, and further allows parity checking to be disabled. More details on these features can be found in the various devices' Hardware User's Manuals.

Further features of the R3000A are configured by the user, in a device dependent fashion. These functions include whether byte ordering follows "Big-Endian" or "Little-Endian" protocols, particulars of the memory interface, etc.

Integrated Device Technology, Inc.

IDT79R3041™ INTEGRATED RISController™ FOR LOW-COST SYSTEMS

IDT79R3041
IDT79RV3041

FEATURES:

- Instruction set compatible with IDT79R3000A and R3051™ Family MIPS RISC CPUs
- High level of integration minimizes system cost
  - — RISC CPU
  - — Multiply/divide unit
  - — Instruction Cache
  - — Data Cache
  - — Programmable bus interface
  - — Programmable port width support
- On-chip instruction and data caches
  - — 2KB of Instruction Cache
  - — 512B of Data Cache
- Flexible bus interface allows simple, low-cost designs
  - — Superset pin-compatible with R3051
  - — Adds programmable port width interface (8-, 16-, and 32-bit memory sub-regions)
  - — Adds programmable bus interface timing support (Extended address hold, Bus turn around time, Read/write masks)
- Single, double-frequency clock input
- 16.67MHz, 20MHz, 25MHz and 33MHz operation
- 20MIPS at 25MHz
- Low cost 84-pin PLCC packaging
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-word read buffer supports burst or simple block reads
- On-chip DMA arbiter
- On-chip 24-bit timer
- Boot from 8-bit, 16-bit, or 32-bit wide PROMs
- Pin- and software-compatible family includes R3041, R3051, R3052™, and R3081™
- Complete software support
  - — Optimizing compilers
  - — Real-time operating systems
  - — Monitors/debuggers
  - — Floating Point emulation software
  - — Page Description Languages

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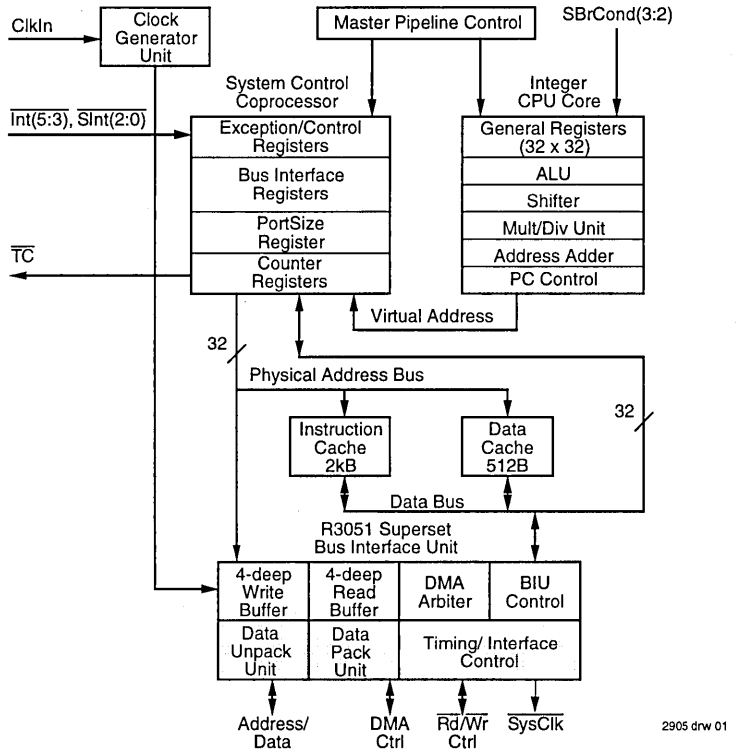

Figure 1. R3041 Block Diagram

INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Further, the R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging. Thus, the R3051 family allows customer applications to bring maximum performance at minimum cost.

The R3041 extends the range of price/performance achievable with the R3051 family, by dramatically lowering the cost of using the MIPS architecture. The R3041 is designed to achieve minimal system and components cost, yet maintain the high-performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the R3051 and R3081.

The R3051 family offers a variety of price/performance features in a pin-compatible, software compatible family. Table 1 provides an overview of the current members of the R3051 family. Note that the R3051, R3052, and R3081 are also available in pin-compatible versions that include a full-function memory management unit, including 64-entry TLB. The R3051/2 and R3081 are described in separate manuals and data sheets.

Figure 1 shows a block level representation of the functional units within the R3041. The R3041 can be viewed as the embodiment of a discrete solution built around the R3000A. By integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

An overview of these blocks is presented here, followed with detailed information on each block.

Device Name	Instruction Cache	Data Cache	Floating Point	Bus Options
R3051	4kB	2kB	Software Emulation	Mux'ed A/D
R3052	8kB	2kB	Software Emulation	Mux'ed A/D
R3071 R3081	16kB or 8kB	4kB or 8kB	On-chip Hardware	1/2 frequency bus option
R3041	2kB	512B	Software Emulation Programmable timing support	8-, 16-, and 32-bit port width support

2905 tbl 01

Table 1. Pin compatible R3051 Family

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to a single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3051 family implements the MIPS-I Instruction Set Architecture (ISA). In fact, the execution engine of the R3041 is the same as the execution engine of the R3000A. Thus, the R3041 is binary compatible with those CPU engines, as well as compatible with other members of the R3051 family.

The execution engine of the R3051 family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). The five parts of the pipeline are the Instruction Fetch, Read register, ALU execution, Memory, and Write Back stages. Figure 2 shows the concurrency achieved by the R3051 family pipeline.

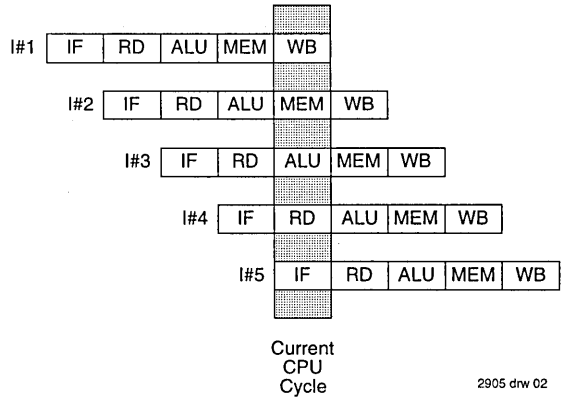

Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3041 also integrates on-chip a System Control Co-processor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the R3051 family, but instead performs the same virtual to physical address mapping of the base version of the R3051 family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

The memory mapping used by these devices is illustrated in Figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other system specific forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- **Cache Configuration Register:** This register controls the data cache block size and miss refill algorithm.
- **Bus Control Register:** This register controls the behavior of the various bus interface signals.
- **Count and Compare Registers:** Together, these two registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **Port Size Control Register:** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring additional external logic.

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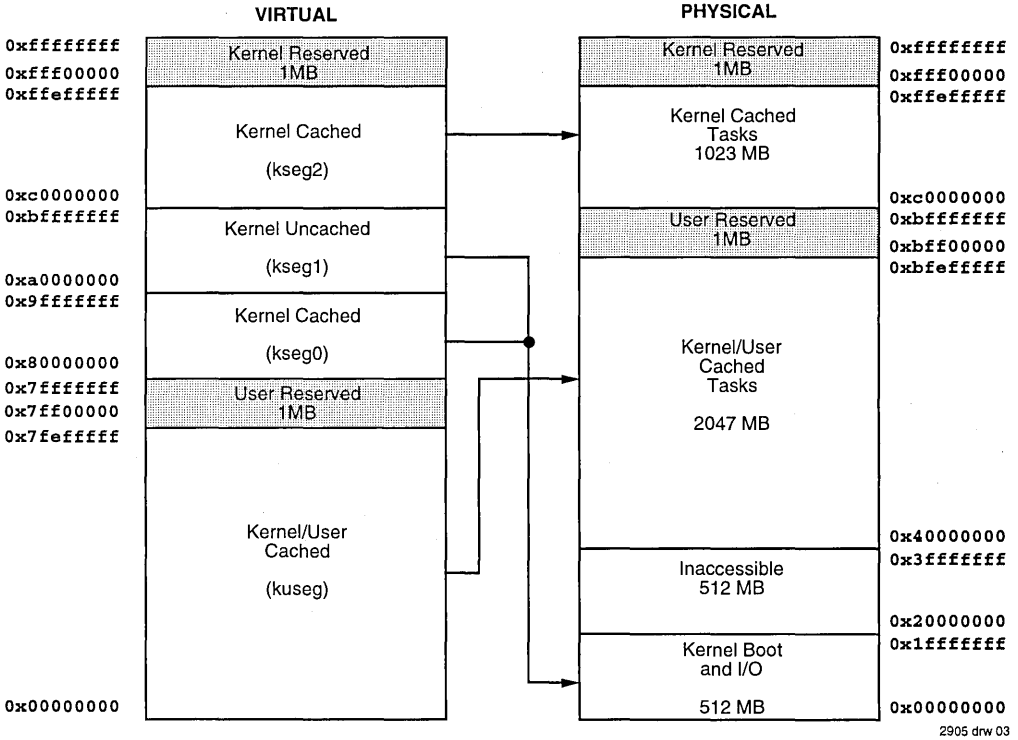

Figure 3. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The R3041 is driven from a single 2x frequency input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3041 integrates 2kB of on-chip Instruction Cache, organized with a line size of 16 bytes (four 32-bit entries) a nd is direct mapped. This relatively large cache substantially contributes to the performance inherent in the R3041, and allows systems based on the R3041 to achieve high-performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switch.

Data Cache

The R3041 incorporates an on-chip data cache of 512B, organized as a line size of 4 bytes (one word) and is direct mapped. This relatively large data cache contributes substantially to the performance inherent in the R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3041 incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3041 augments the basic R3051 bus interface capability by adding the ability to directly interface with varying memory port widths, for instructions or data. For example, the R3041 can be used in a system with an 8-bit boot PROM, 16-bit font/program cartridges, and 32-bit main memory, transparently to software, and without requiring external data packing, rotation, and unpacking.

In addition, the R3041 incorporates the ability to change some of the interface timing of the bus. These features can be used to eliminate external data buffers and take advantage of lower speed and lower cost interface components.

One of the bus interface options is the Extended Address Hold mode which adds 1/2 clock of extra address hold time from ALE falling. This allows easier interfacing to FPGAs and ASICs.

The R3041 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate. During main memory writes, the R3041 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software which initiated the store, insuring that the same software can run in true 32-bit memory systems.

The R3051 family read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to use page or static column mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or even to use simpler SRAM techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R3041 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, using 8-, 16-, or 32-bit boot PROMs is easily supported by the R3041.

SYSTEM USAGE

The IDT R3051 family is specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems use inexpensive EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. An embedded system can optionally use an 8-bit boot PROM instead. A 16-bit font/program cartridge interface is provided for add-in cards. A 16-bit DRAM interface is used for a low-cost page frame buffer. In this system example, a field or manufacturing upgrade to a 32-bit page frame buffer is supported by the boot software and DRAM controller. Embedded systems may optionally substitute SRAMs for the DRAMs. Finally various 8/16/32-bit I/O ports such as RS-232/422, SCSI, and LAN as well as the laser printer engine interface are supported. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the R3051 family.

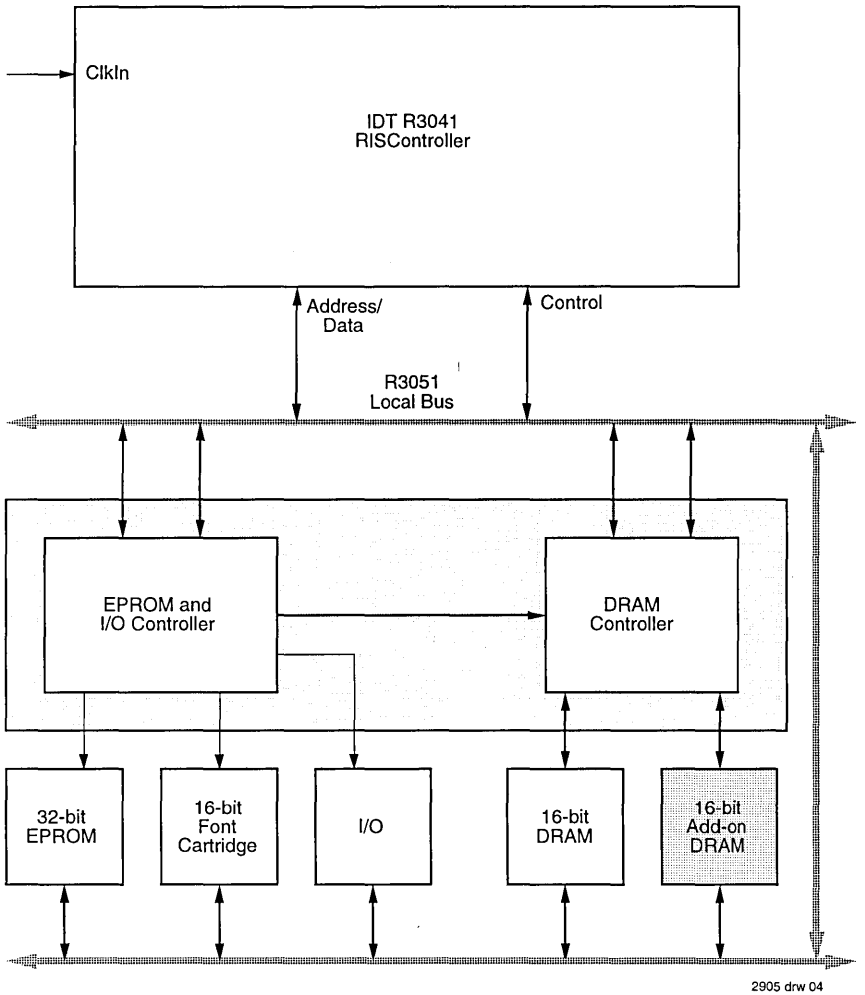

Figure 4. Typical R3041-Based Application

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family based applications, and include tools such as:

- Optimizing compilers from MIPS Technology, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point emulation library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT Laser Printer System boards, which directly drive a low-cost print engine, and runs Adobe PostScript™ Page Description Language
- Adobe PostScript Page Description Language running on the IDT R3051 family.
- The IDT/sim™ PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™ (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

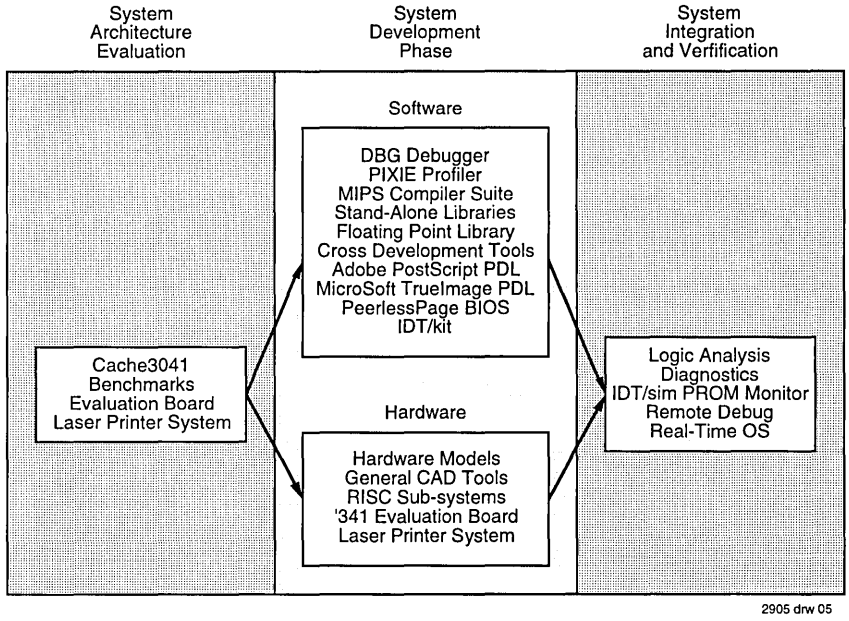

Figure 5. R3041 Development Environment

PERFORMANCE OVERVIEW

The R3051 family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine:** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves over 16 MIPS performance when operating out of cache.
- **Large on-chip caches:** The R3051 family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- **Autonomous multiply and divide operations:** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- **Integrated write buffer:** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support:** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various R3051 family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these devices in their application.

SELECTABLE FEATURES

The R3051 family uses two methods to allow the system designer to configure bus interface operation options.

The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communication between various types of processors and databases.
- **Data Cache Refill of one or four words:** The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed:** The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time:** The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals:** The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.
- **Programmable memory Port Widths:** The R3041 allows the kernel to partition the physical memory space into various sub-regions, and to individually indicate the port width of these sub-regions. Thus, the bus interface unit can perform data packing and unpacking when communicating with narrow memory sub-regions. For example, these features, can be used to allow the R3041 to interface with narrow 8-bit boot PROMs, or to implement 16-bit only memory systems.

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THERMAL CONSIDERATIONS

The R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the R3051 family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package is used for all speeds of the R3041 family.

Higher speed and higher performance members of the R3051 family utilize more advanced packaging techniques to dissipate power while remaining both low-cost and pin- and socket- compatible with the PLCC package. Thus, these members of the R3051 family are available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

The members of the R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 2 for the PLCC package.

	Airflow (ft/min)					
ØCA	**0**	**200**	**400**	**600**	**800**	**1000**
"J" Package	29	26	21	18	16	15
TQFP	55	40	35	33	31	30

2905 tbl 02

Table 2. Thermal Resistance ($Ø_{CA}$) at Various Airflows

NOTES ON SYSTEM DESIGN

The R3041 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

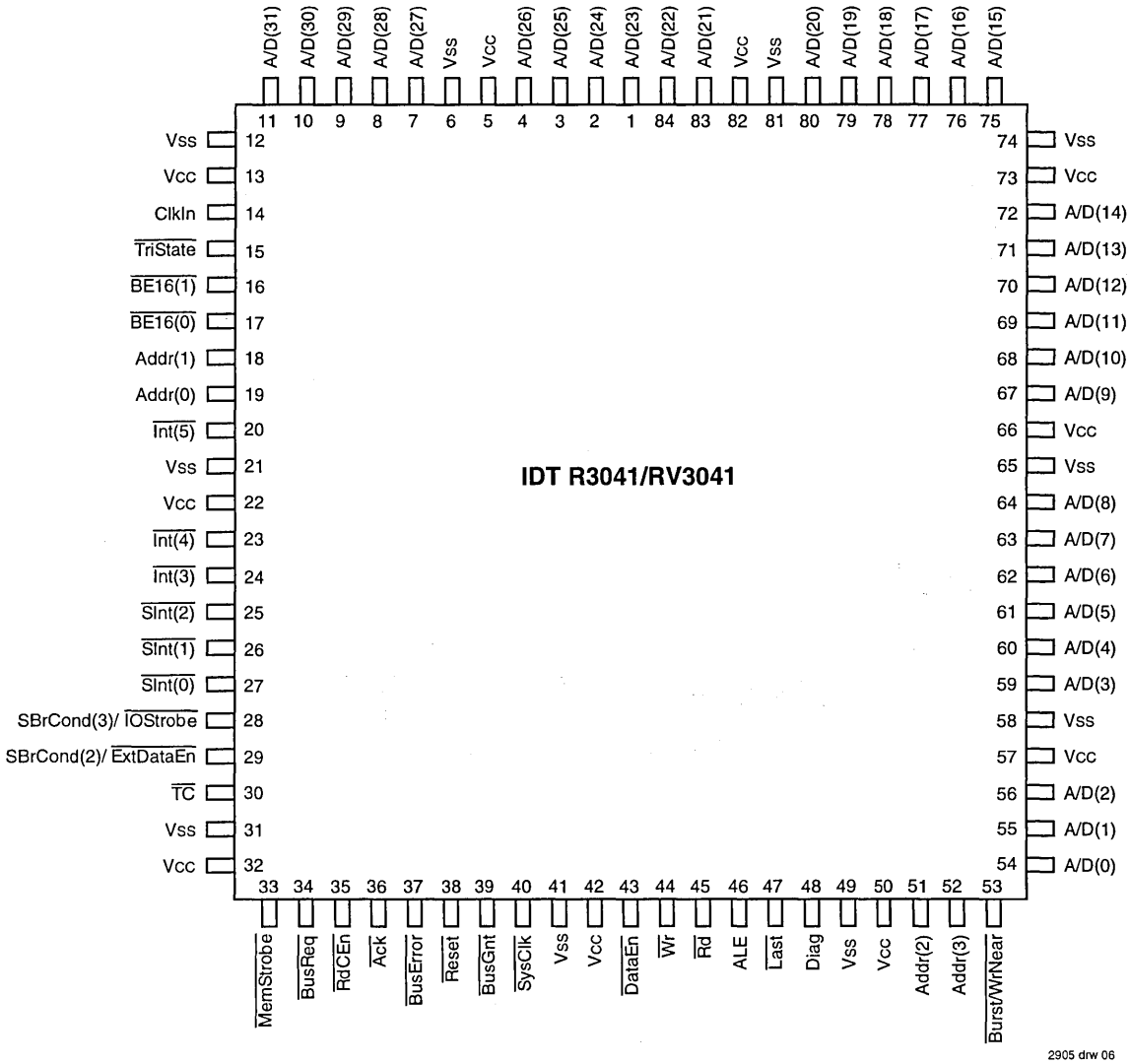
To minimize these AC parameters, the R3041 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3041 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3041 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

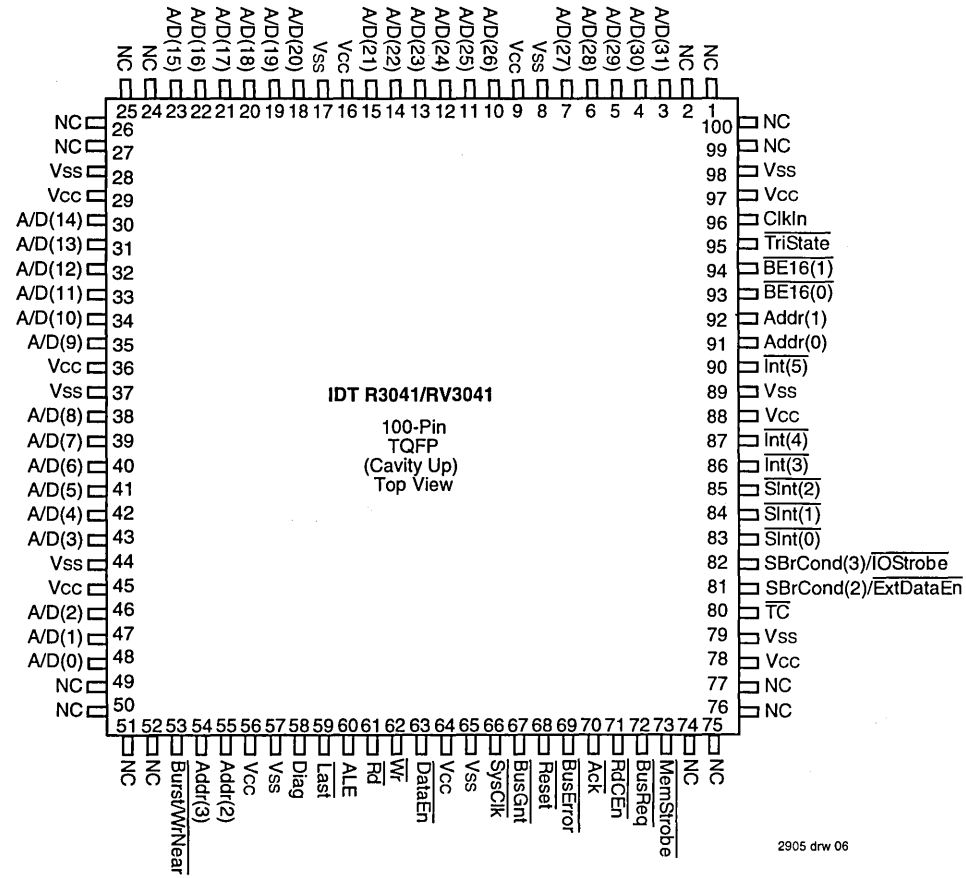
PIN CONFIGURATIONS



2905 drw 06

84-Pin PLCC/
Top View
(Cavity Down)

PIN CONFIGURATIONS



2905 drw 06

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). $\overline{BE(3:0)}$: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). $\overline{BE(3)}$ indicates that A/D(31:24) will be used, and $\overline{BE(0)}$ corresponds to A/D(7:0). These strobes are only valid for accesses to 32-bit wide memory ports. Note that $\overline{BE(3:0)}$ can be held in-active during reads by setting the appropriate bit of CP0; thus when latched, these signals can be directly used as Write Enable strobes. During the second phase, these signals are the data bus for the transaction. **Data(31:0):** During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. The byte lanes used during the transfer are a function of the datum size, the memory port width, and the system byte-ordering.
Addr(3:0)	O	**Low Address (3:0)** A 4-bit bus which indicates which word/halfword/byte is currently expected by the processor. For 32-bit port widths, only Addr(3:2) is valid during the transfer; for 16-bit port widths, only Addr(3:1) are valid; for 8-bit port widths, all of Addr(3:0) are valid. These address lines always contain the address of the current datum to be transferred. In writes and single datum reads, the addresses initially output the specific target address, and will increment if the size of the datum is wider than the target memory port. For quad word reads, these outputs function as a counter starting at '0000', and incrementing according to the width of the memory port.
	I[1]	During $\overline{Reset}$, the Addr(3:0) pins act as Reset Configuration Mode bit inputs for the $\overline{BootProm16}$, $\overline{BootProm8}$, ReservedHigh, and $\overline{ExtAddrHold}$ options. The R3041 Addr(1:0) output pins are designated as the unconnected Rsvd(1:0) pins in the R3051 and R3081.
Diag	O	**Diagnostic Pin.** This output indicates whether the current bus read transaction is due to an on-chip cache miss and whether the read is an instruction or data. It is time multiplexed as described below: **Cached/$\overline{Uncached}$:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether or not the current read is a result of a cache miss. The value of this pin at this time other than in read cycles is undefined. I/$\overline{D}$: A high at this time indicates an instruction reference, and a low indicates a data reference. The value of this pin at this time other than in read cycles is undefined. The R3041 Diag output pin is designated as the Diag(1) output pin in the R3051 and R3081.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically by using transparent latches.
$\overline{DataEn}$	O	**Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.

NOTE:
1. Reset Configuration Mode bit input when $\overline{Reset}$ is asserted, normal signal function when $\overline{Reset}$ is de-asserted.

2905 tbl 03

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PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if the 4-word data block refill option is selected in the CP0 Cache Config Register. On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "System" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master. The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the BusGnt output early, and waiting for the BusReq input to be negated.
SBrCond(3)/ IOStrobe	I/O	**Branch Condition Port/IO Strobe:** The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as IOStrobe, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals on the bus interface.
SBrCond(2)/ ExtDataEn	I/O	**Branch Condition Port/Extended Data Enable:** The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of Rd or Wr. This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.
MemStrobe	O	**Memory Strobe:** This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices. The R3041 MemStrobe output pin is designated as the BrCond(0) input pin in the R3051 and R3081.

2905 tbl 04

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{BE16(1:0)}$	O	**Byte Enable Strobes for 16-bit Memory Port:** These active low outputs are the byte lane strobes for accesses to 16-bit wide memory ports; they are not necessarily valid for 8- or 32-bit wide ports. If $\overline{BE16(1)}$ is asserted, then the most significant byte (either D(31:24) or D(15:8), depending on system endianness) is going to be used in this transfer. If $\overline{BE16(0)}$ is asserted, the least significant byte (D(23:16) or D(7:0)) will be used. $\overline{BE16(1:0)}$ can be held inactive (masked) during read transfers, according to the programming of the CP0 Bus Control register.
	I[1]	During $\overline{Reset}$, the $\overline{BE16(1:0)}$ act as Reset Configuration Mode bit inputs for two ReservedHigh options. The $\overline{BE16(1:0)}$ output pins are designated as the unconnected Rsvd(3:2) pins in the R3051 and R3081.
$\overline{Last}$	O	**Last Datum in Mini-Burst:** This active low output indicates that this is the last datum transfer in a given transaction. It is asserted after the next to last $\overline{RdCEn}$ (reads) or $\overline{Ack}$ (writes), and is negated when $\overline{Rd}$ or $\overline{Wr}$ is negated. The $\overline{Last}$ output pin is designated in the R3051 and R3081 as the Diag(0) output pin.
$\overline{TC}$	O	**Terminal Count:** This is an active low output from the processor which indicates that the on-chip timer has reached its terminal count. It will remain low for either 1.5 clock cycles, or until software resets the timer, depending on the mode selected in the CP0 Bus Control register. Thus, the on-chip timer can function either as a free running timer for system functions such as DRAM refresh, or can operate as a software controlled time-slice timer, or real-time clock. The $\overline{TC}$ output pin is designated in the R3051 as the BrCond(1) input pin, and in the R3081 as the Run pin output.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{Int(5:3)}$ $\overline{SInt(2:0)}$	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int(5:0)}$ signals of the R3000A. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals on the original R3000A.
	I[1]	During $\overline{Reset}$, $\overline{Int(3)}$ and $\overline{SInt(0)}$ act as Reset Configuration Mode bit inputs for the AddrDisplayAndForceCacheMiss and BigEndian options. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
ClkIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Reset initialization mode selection is performed during the last cycle of $\overline{Reset}$.
$\overline{TriState}$	I	**Tri-State:** This input to the R3041 requests that the R3041 tri-state all of its outputs. In addition to those outputs tri-stated during DMA, tri-state will cause $\overline{SysClk}$, $\overline{TC}$, and $\overline{BusGnt}$ to tri-state. This signal is intended for use during board testing and emulation during debug and board manufacture. The $\overline{TriState}$ input pin is designated as the unconnected Rsvd(4)pin in the R3051 and R3081.
Vcc	I	**Power:** These inputs must be supplied with the rated supply voltage (VCC). All Vcc inputs must be connected to insure proper operation.
Vss	I	**Ground:** These inputs must be connected to ground (GND). All Vss inputs must be connected to insure proper operation.

NOTE:
1. Reset Configuration Mode bit input when $\overline{Reset}$ is asserted, normal signal function when $\overline{Reset}$ is de-asserted.

2905 tbl 05

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ABSOLUTE MAXIMUM RATINGS[1, 3] R3041

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
VIN	Input Voltage	–0.5 to +7.0	V

2905 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS R3041

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0	V

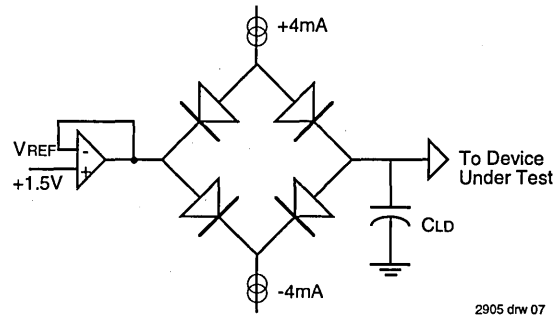
2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2905 tbl 07

OUTPUT LOADING FOR AC TESTING



2905 drw 07

Signal	Cld
All Signals	25 pF

2905 tbl 09

DC ELECTRICAL CHARACTERISTICS R3041 — (TC = 0°C to +85°C, VCC = +5.0V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	VCC = Min., IOH = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage[3]	—	2.0	—	2.0	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage[1]	—	—	0.8	—	0.8	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage[2,3]	—	3.0	—	3.0	—	3.0	—	3.0	—	V
VILS	Input LOW Voltage[1,2]	—	—	0.4	—	0.4	—	0.4	—	0.4	V
CIN	Input Capacitance[4]	—	—	10	—	10	—	10	—	10	pF
COUT	Output Capacitance[4]	—	—	10	—	10	—	10	—	10	pF
ICC	Operating Current	VCC = 5V, TC = 25°C	—	225	—	250	—	300	—	370	mA
IIH	Input HIGH Leakage	VIH = VCC	—	100	—	100	—	100	—	100	µA
IIL	Input LOW Leakage	VIL = GND	–100	—	–100	—	–100	—	–100	—	µA
IOZ	Output Tri-state Leakage	VOH = 2.4V, VOL = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

2905 tbl 10

NOTES:
1. VIL Min. = –3.0V for pulse width less than 15ns. VIL should not fall below –0.5 volts for larger periods.
2. VIHS and VILS apply to ClkIn and $\overline{\text{Reset}}$.
3. VIH should not be held above VCC + 0.5 volts.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS R3041 (1, 2, 3) — (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	8	—	6	—	5	—	4	—	ns
t1a	A/D	Set-up to SysClk falling	9	—	7	—	6	—	5	—	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	4	—	3	—	2.5	—	2.5		ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1.5	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	10	—	8	—	7	—	6	ns
t6	BusGnt	Negated from SysClk falling	—	10	—	8	—	7	—	6	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	—	8	—	6	—	5	—	4	ns
t7a	A/D	Valid from SysClk rising	—	15	—	12	—	10	—	9	ns
t7b	Last	Valid from SysClk rising	—	8	—	5	—	5	—	4	ns
t8	ALE	Asserted from SysClk rising	—	5	—	4	—	4	—	3	ns
t9	ALE	Negated from SysClk falling	—	5	—	4	—	4	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5		ns
t11	DataEn	Asserted from SysClk	—	19	—	15	—	15	—	13	ns
t12	DataEn	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising(4)	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	—	9	—	7	—	6	—	5	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	—	8	—	6	—	6	—	5	ns
t17	Diag	Valid from SysClk	—	15	—	12	—	11	—	10	ns
t18	A/D	Tri-state from SysClk	—	13	—	10	—	10	—	10	ns
t19	A/D	SysClk to data out	—	16	—	13	—	12	—	10	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	Reset	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t26	Int	Mode set-up to Reset rising	8	—	6	—	5	—	5	—	ns
t27	Int	Mode hold from Reset rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

2905 tbl 11

5

AC ELECTRICAL CHARACTERISTICS R3041 (CONT.)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t45	ExtDataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	ExtDataEn	Driven from SysClk falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	IOStrobe	Valid from SysClk falling	—	10	—	8	—	7	—	7	ns
t48	ExtDataEn, DataEn	Asserted from SysClk rising	—	15	—	12	—	9	—	9	ns
t49	ExtDataEn	Negated from SysClk rising	—	9	—	7	—	6	—	6	ns
t50	MemStrobe	Asserted from SysClk rising	—	19	—	15	—	13	—	11	ns
t51	MemStrobe	Negated from SysClk falling	—	19	—	15	—	13	—	11	ns
t52	MemStrobe	Asserted from Addr(3:0) valid[4]	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF[4, 5]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

2905 tbl 12

NOTES:
1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other R3051 family members.

ABSOLUTE MAXIMUM RATINGS[1, 3] RV3041

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
VIN	Input Voltage	–0.5 to +7.0	V

2905 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS RV3041

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.0	—	V
VILS	Input LOW Voltage	—	0	V

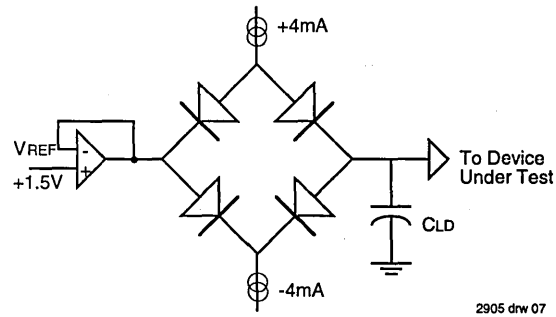
2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial RV3041	0°C to +85°C (Case)	0V	3.3 ±5%

2905 tbl 07

OUTPUT LOADING FOR AC TESTING



2905 drw 07

Signal	Cld
All Signals	25 pF

2905 tbl 09

DC ELECTRICAL CHARACTERISTICS RV3041 — (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	2.5	—	2.5	—	2.5	—	2.5	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 3.3V, T_C = 25°C	—	130	—	150	—	180	—	225	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	mA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	mA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	mA

NOTES:

2905 tbl 10

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 volts for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

5

AC ELECTRICAL CHARACTERISTICS RV3041 (1, 2, 3) — (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$	Set-up to $\overline{SysClk}$ rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to $\overline{SysClk}$ falling	12	—	9	—	7	—	7	—	ns
t2	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$	Hold from $\overline{SysClk}$ rising	4	—	3	—	2.5	—	2.5	—	ns
t2a	A/D	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Tri-state from $\overline{SysClk}$ rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Driven from $\overline{SysClk}$ falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	$\overline{BusGnt}$	Asserted from $\overline{SysClk}$ rising	—	10	—	8	—	7	—	7	ns
t6	$\overline{BusGnt}$	Negated from $\overline{SysClk}$ falling	—	10	—	8	—	7	—	7	ns
t7	$\overline{Wr}$, $\overline{Rd}$, $\overline{Burst/WrNear}$, TC	Valid from $\overline{SysClk}$ rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from $\overline{SysClk}$ rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from $\overline{SysClk}$ rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from $\overline{SysClk}$ rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from $\overline{SysClk}$ falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5		ns
t11	$\overline{DataEn}$	Asserted from $\overline{SysClk}$	—	19	—	15	—	15	—	15	ns
t12	$\overline{DataEn}$	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{SysClk}$ rising(4)	0	—	0	—	0	—	0	—	ns
t15	$\overline{Wr}$, $\overline{Rd}$, $\overline{DataEn}$, $\overline{Burst/WrNear}$, Last, TC	Negated from $\overline{SysClk}$ falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from $\overline{SysClk}$	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from $\overline{SysClk}$	—	15	—	12	—	11	—	11	ns

2905 tbl 11

AC ELECTRICAL CHARACTERISTICS RV3041 (CONT.)

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t18	A/D	Tri-state from $\overline{SysClk}$	—	13	—	10	—	10	—	10	ns
t19	A/D	$\overline{SysClk}$ to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	8	—	6	—	5	—	5	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	4	—	3	—	3	—	3	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	4	—	3	—	3	—	3	—	ns
tsys	$\overline{SysClk}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{SysClk}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	$\overline{SysClk}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t45	$\overline{ExtDataEn}$	Tri-state from $\overline{SysClk}$ rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	$\overline{ExtDataEn}$	Driven from $\overline{SysClk}$ falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	$\overline{IOStrobe}$	Valid from $\overline{SysClk}$ falling	—	10	—	8	—	7	—	7	ns
t48	$\overline{ExtDataEn}$,	Asserted from $\overline{SysClk}$ rising	—	15	—	12	—	9	—	9	ns
t49	$\overline{ExtDataEn}$ $\overline{DataEn}$	Negated from $\overline{SysClk}$ rising	—	9	—	7	—	6	—	6	ns
t50	$\overline{MemStrobe}$	Asserted from $\overline{SysClk}$ rising	—	19	—	15	—	15	—	15	ns
t51	$\overline{MemStrobe}$	Negated from $\overline{SysClk}$ falling	—	19	—	15	—	15	—	15	ns
t52	$\overline{MemStrobe}$	Asserted from Addr(3:0) valid[4]	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF[4, 5]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

2905 tbl 12

NOTES:

1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other R3051 family members.

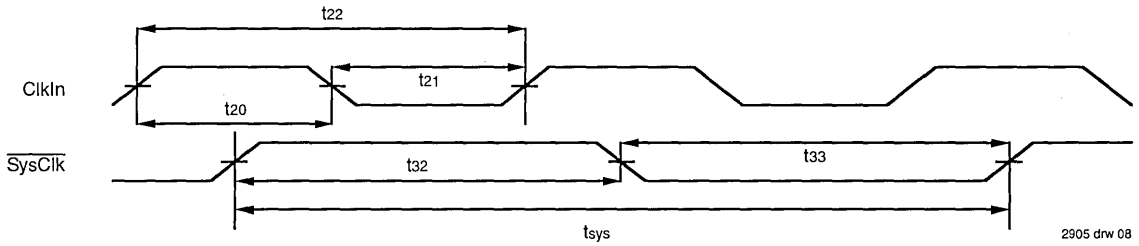


Figure 8. R3051 Family Clocking

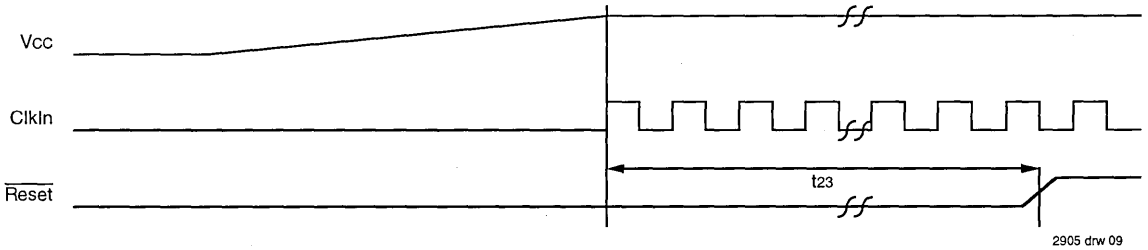


Figure 9. Power-On Reset Sequence

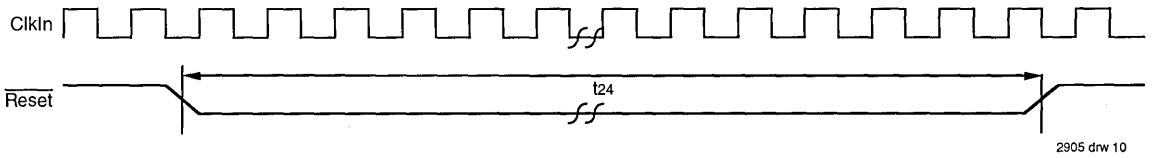


Figure 10(a). Warm Reset Sequence

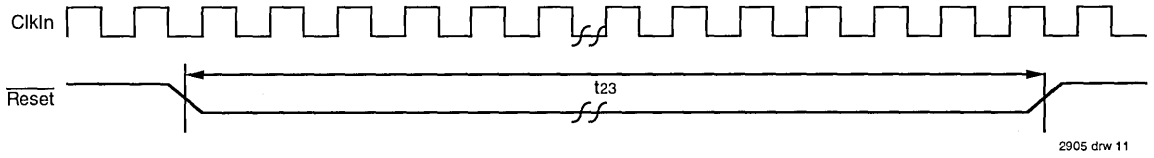


Figure 10(b). Warm Reset Sequence (Internal Pull-Ups Used)

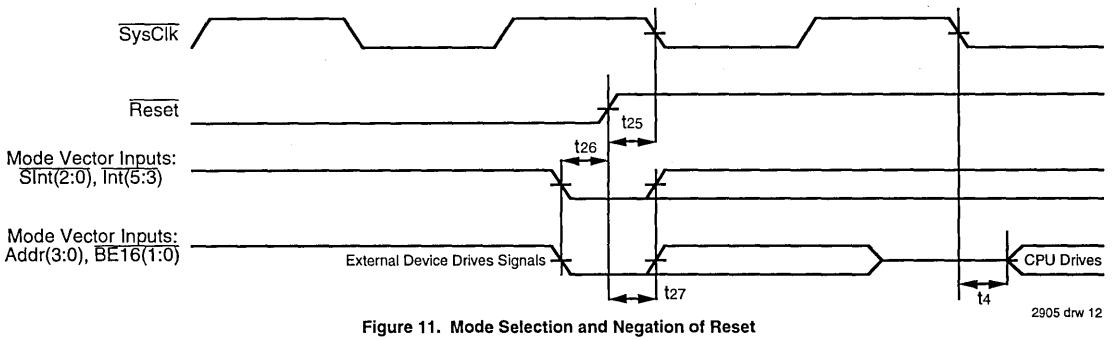


Figure 11. Mode Selection and Negation of Reset

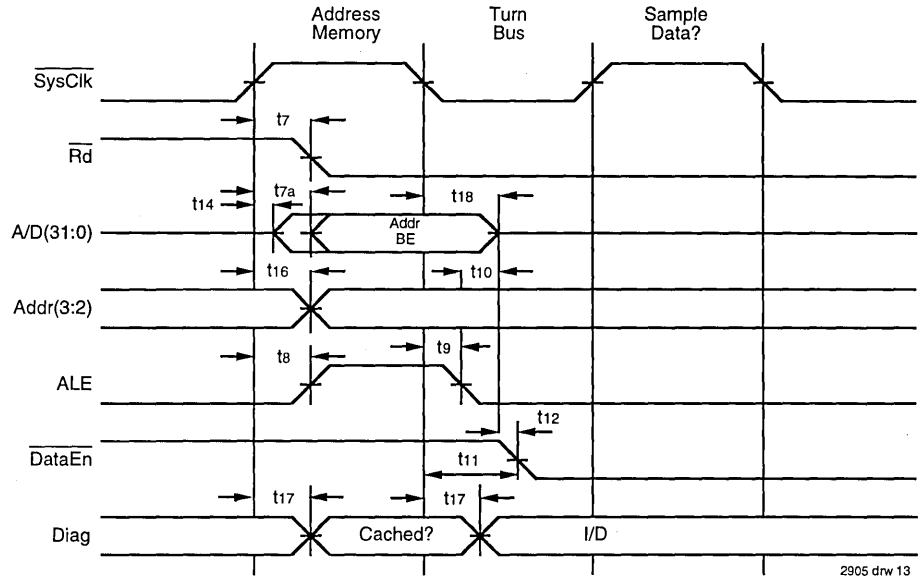


Figure 12(a). Start of Read Timing with Non-Extended Address Hold Option

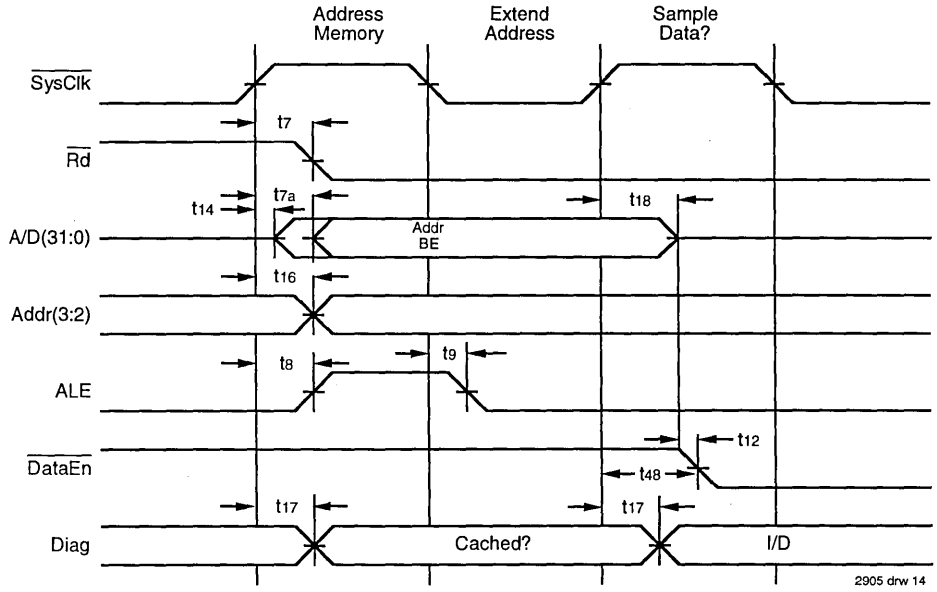


Figure 12(b). Start of Read Timing with Extended Address Hold Option

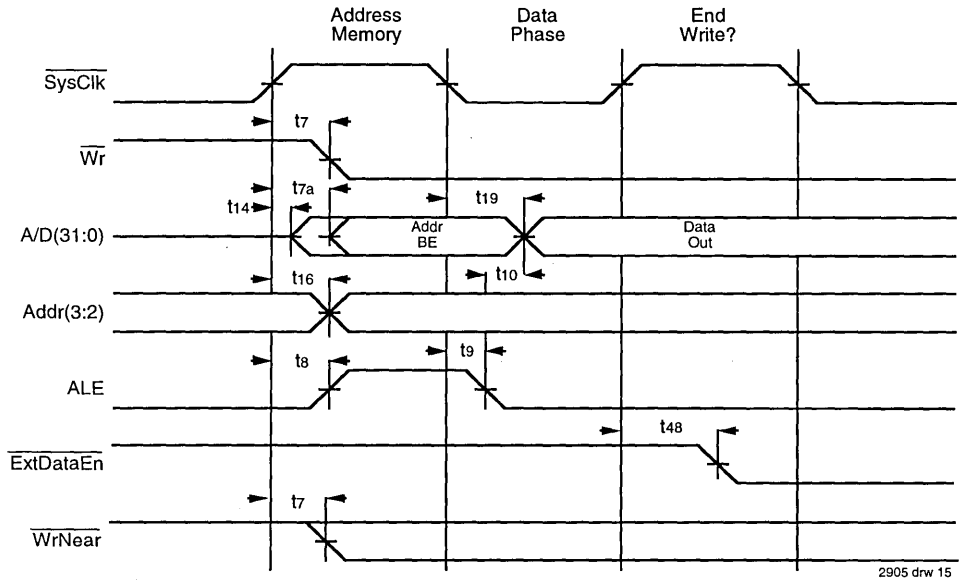


Figure 12(c). Start of Write Timing with Non-Extended Address Hold Option

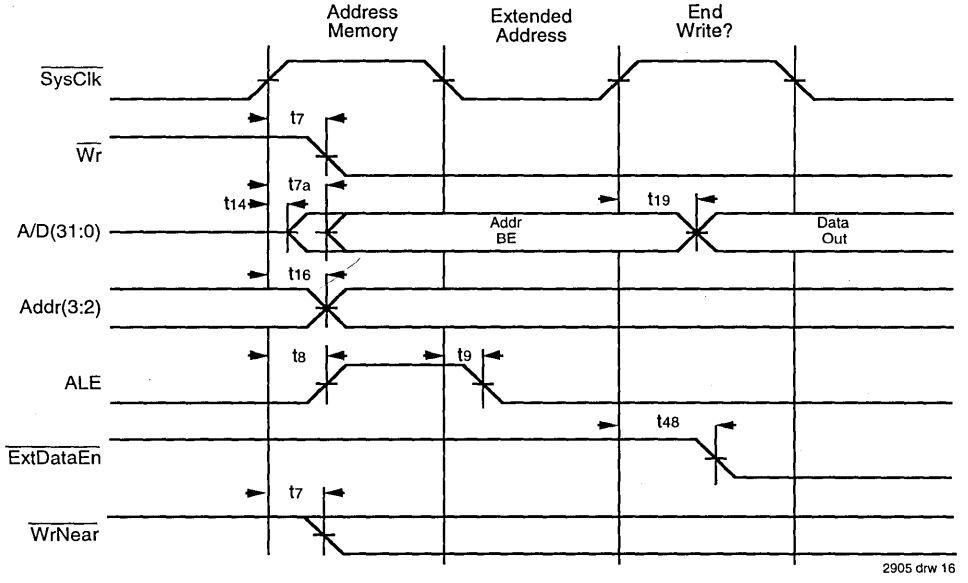


Figure 12(d). Start of Write Timing with Extended Address Hold Option

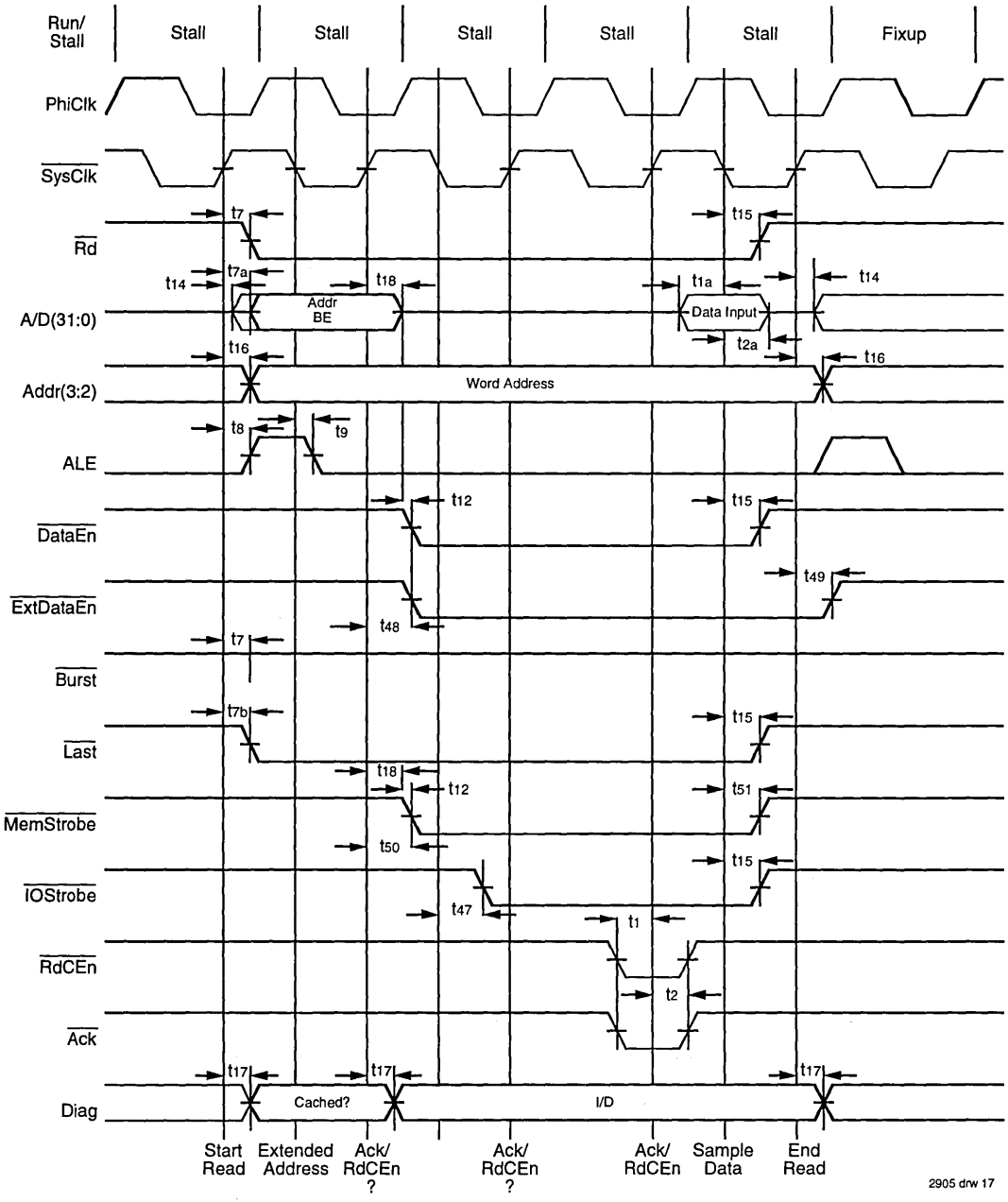


Figure 13. Single Datum Read

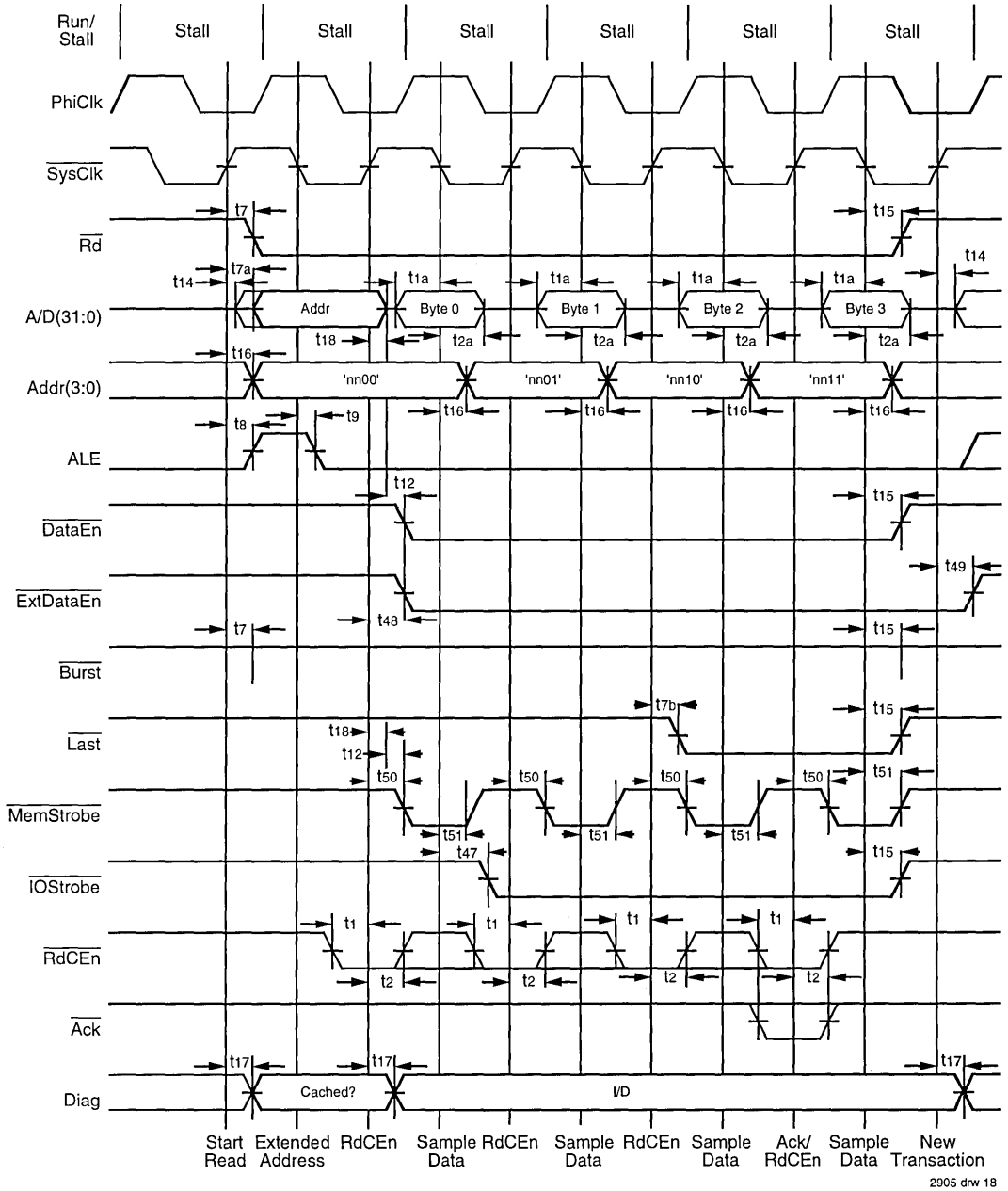


Figure 14. Mini-burst read of 32-bit datum from 8-bit wide memory port

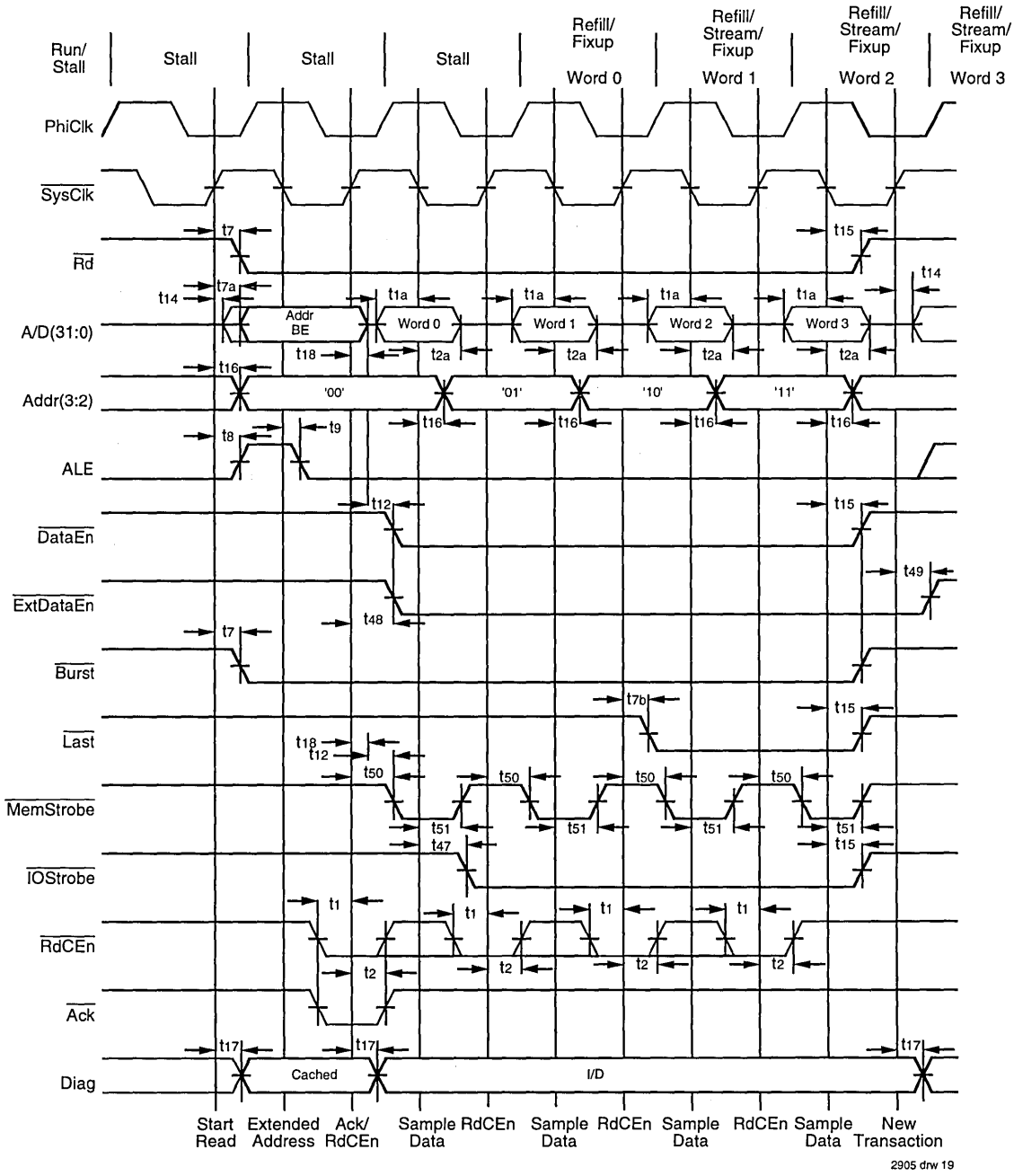


Figure 15. R3041 Quad Word Read

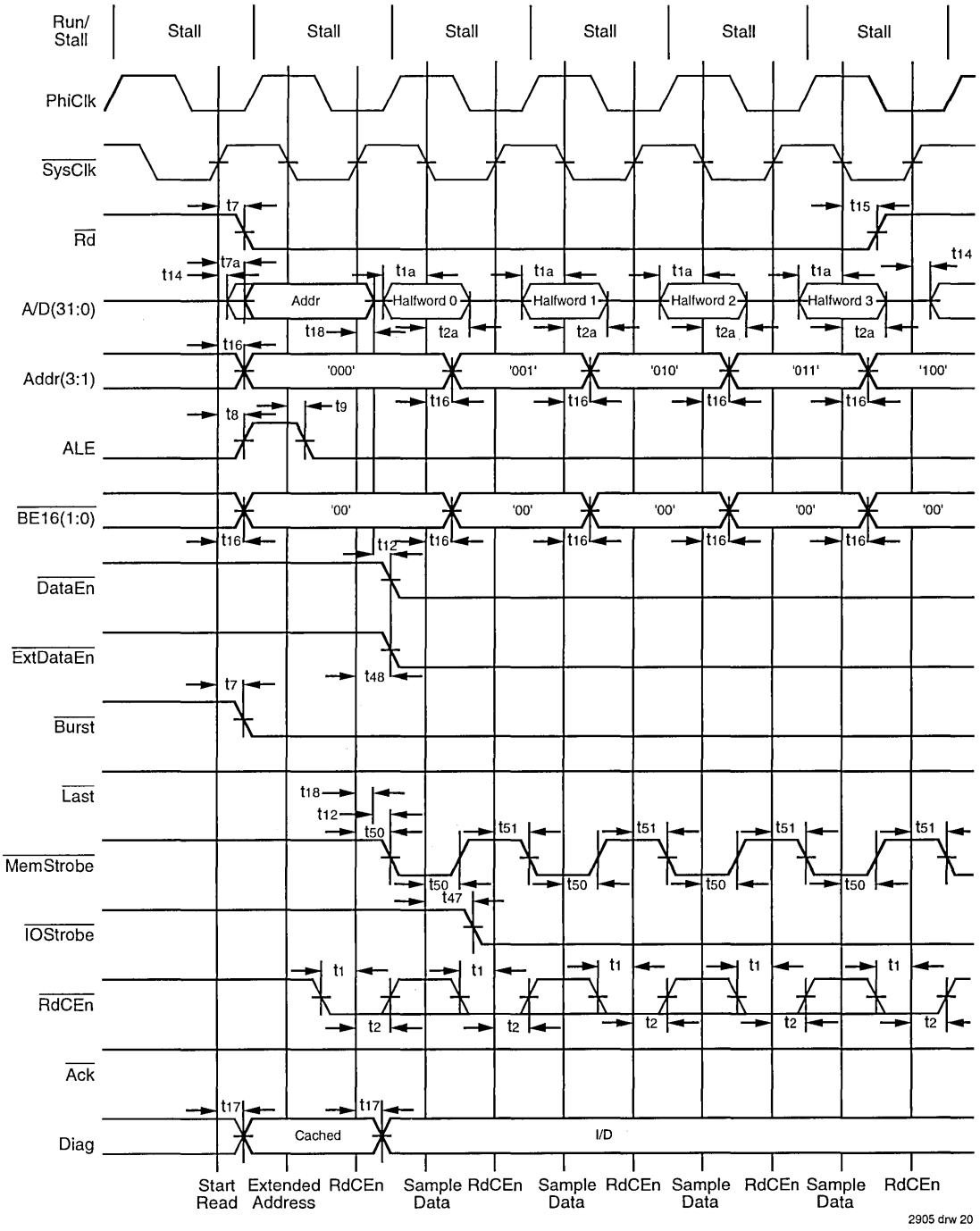


Figure 16(a). Quad Word Read to 16-bit wide Memory Port

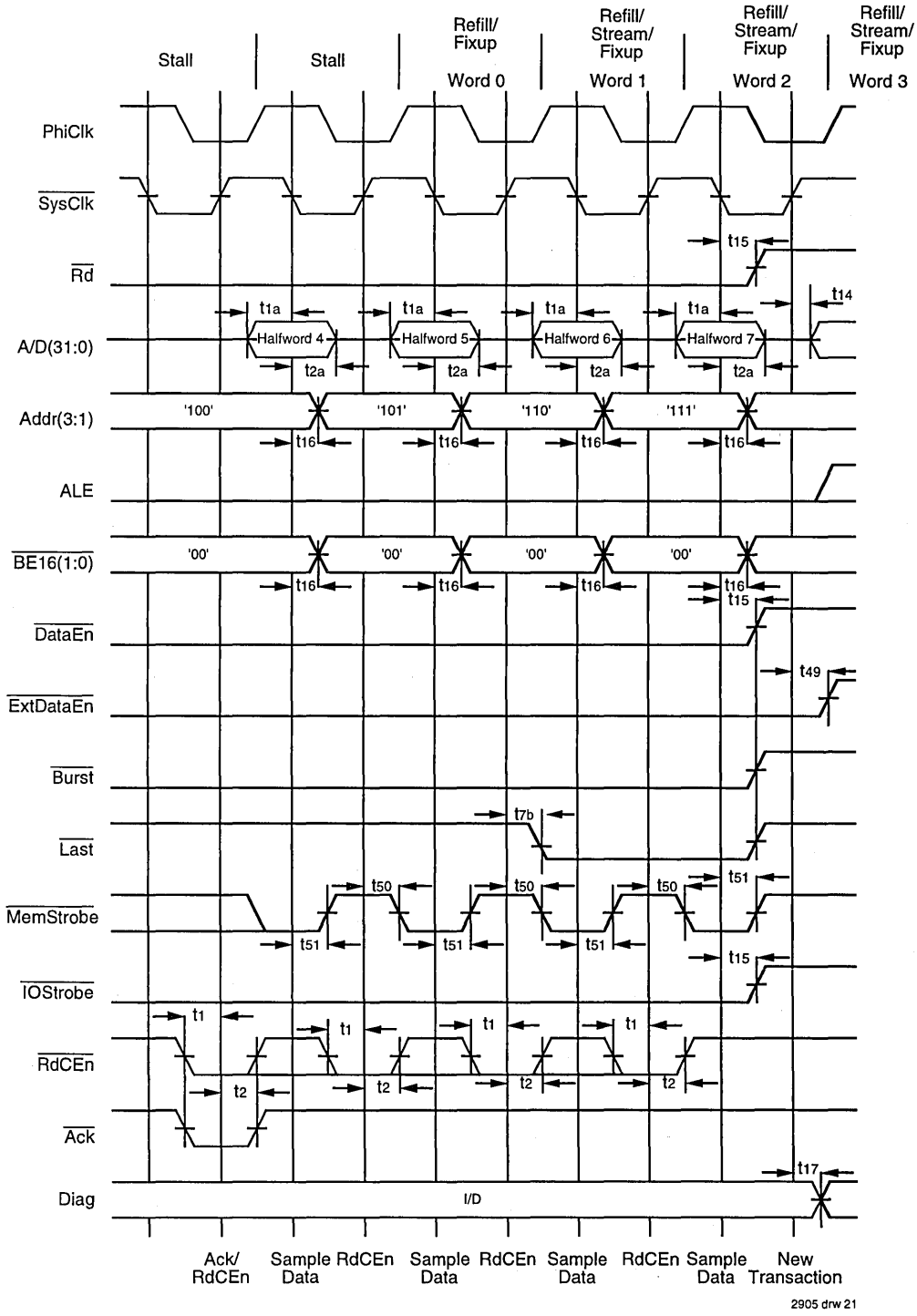


Figure 16(b). End of Quad Word read from 16-bit Wide Memory Port

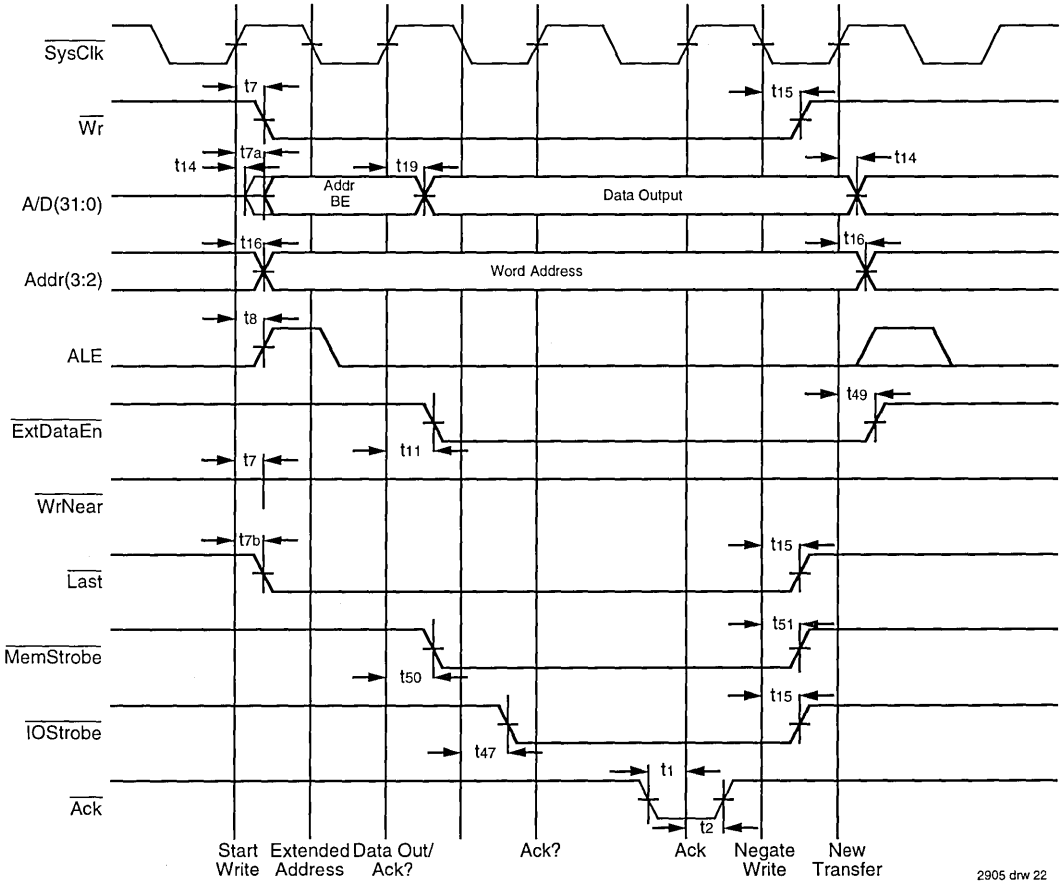


Figure 17. Basic Write to 32-bit Memory Port

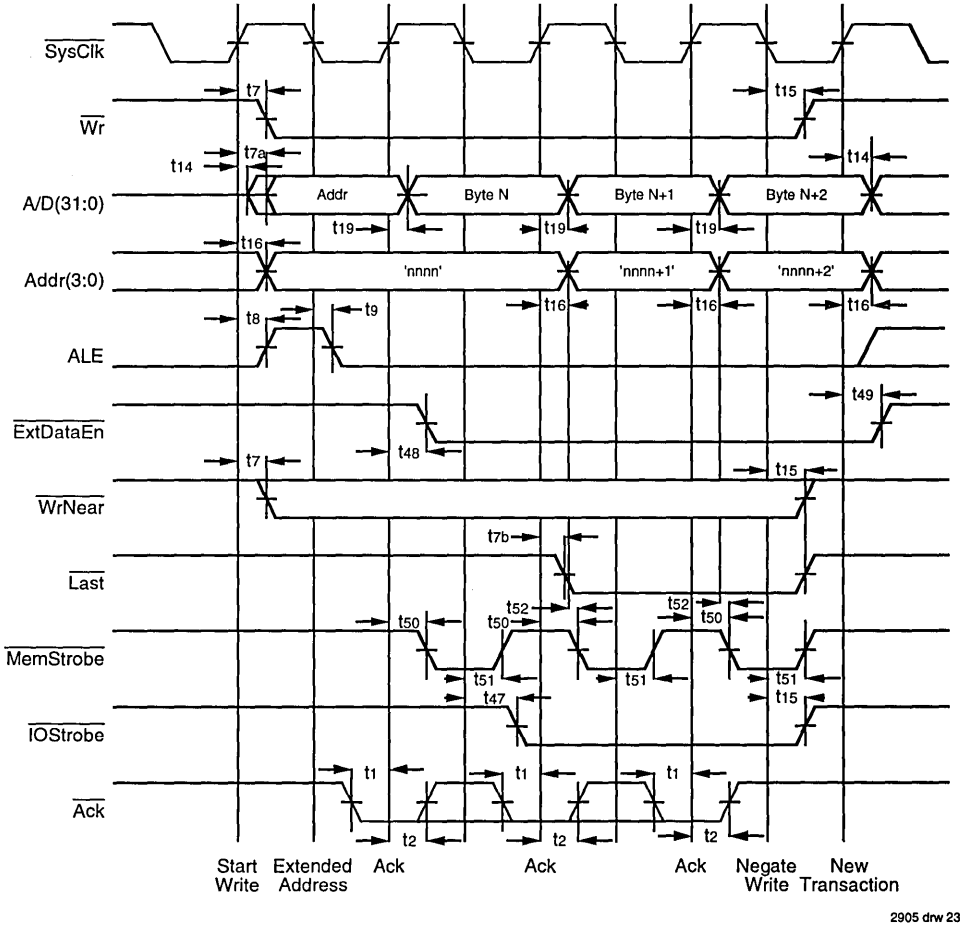


Figure 18. Tri-Byte Mini-burst Write to 8-bit Port

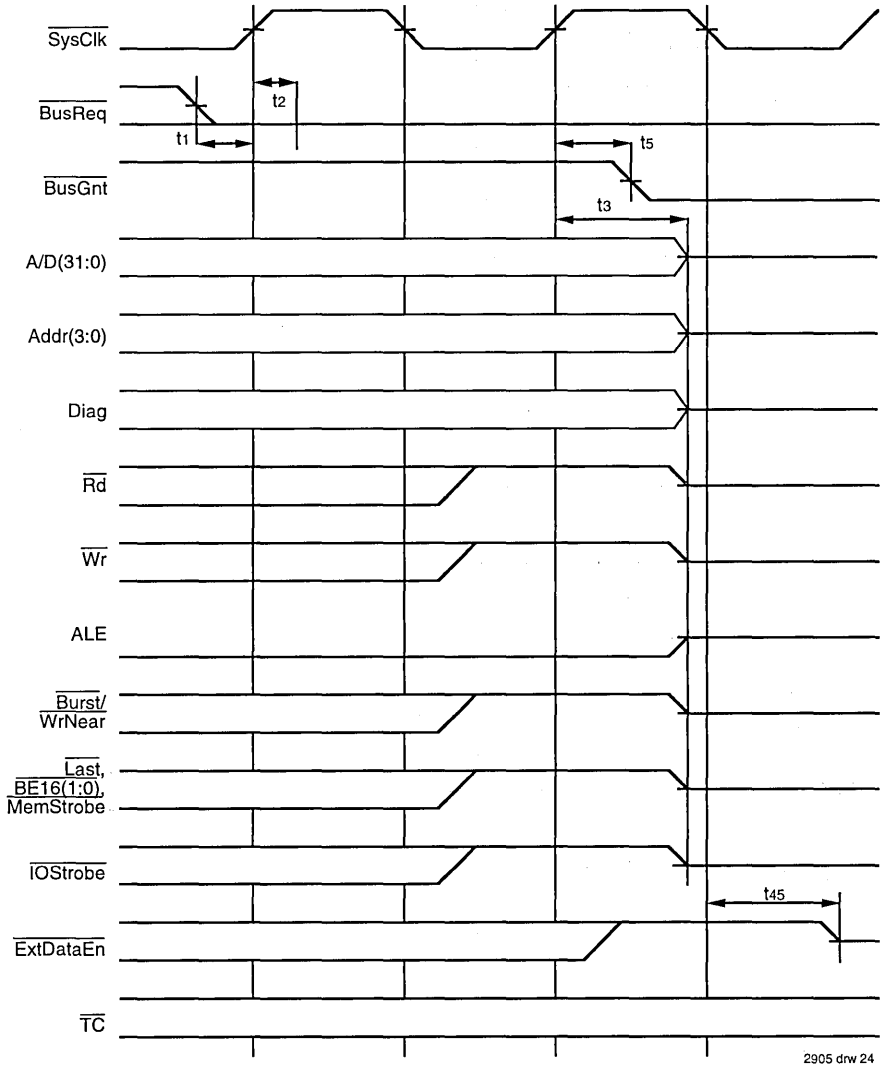


Figure 19. Request and Relinquish of R3041 Bus to External Master

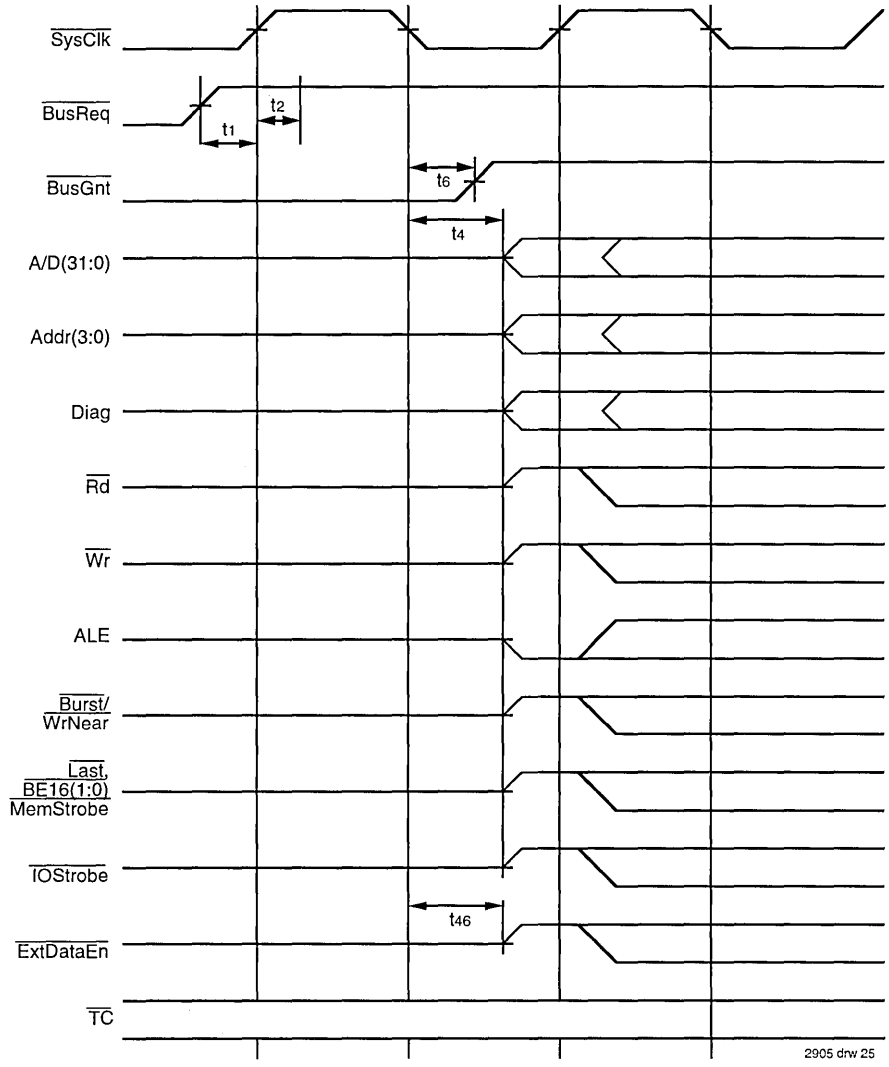


Figure 20. R3041 Regaining Bus Mastership

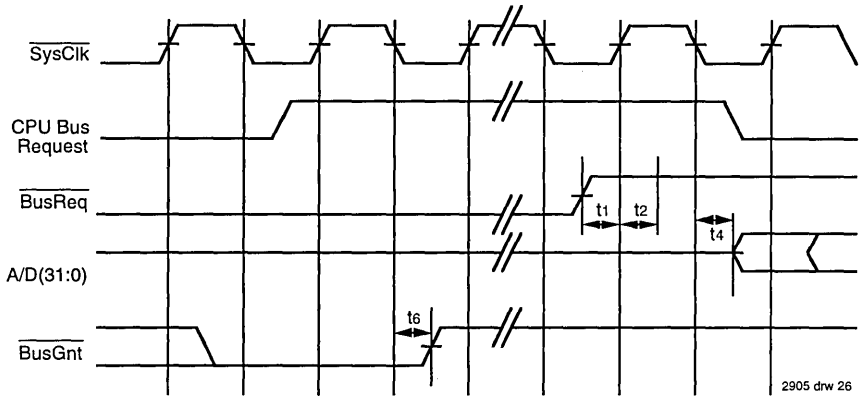


Figure 21. R3041 DMA Pulse Protocol

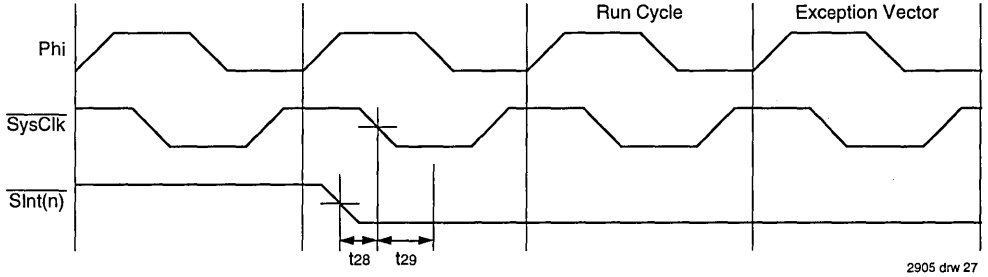


Figure 22. Synchronized Interrupt Input Timing

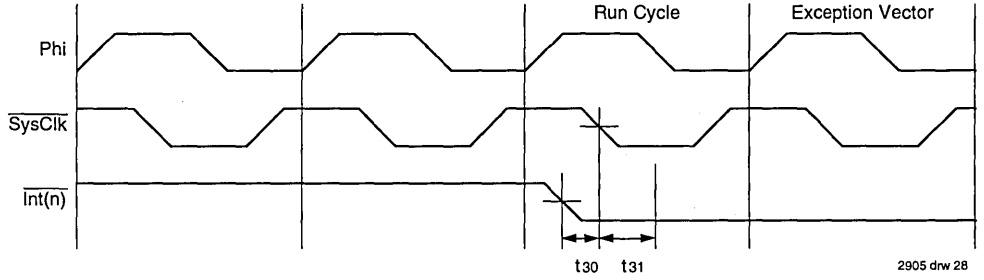


Figure 23. Direct Interrupt Input Timing

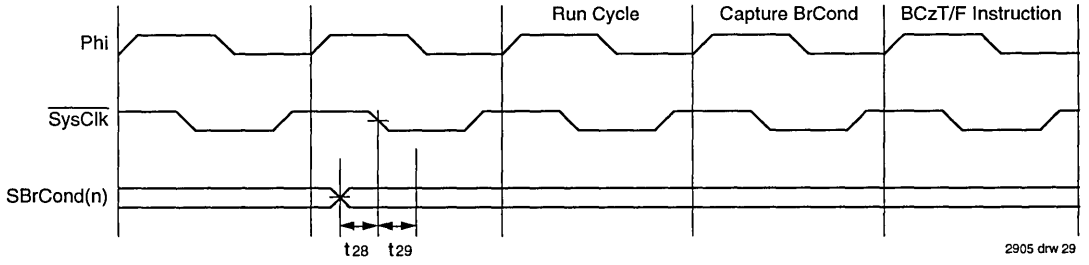


Figure 24. Synchronized Branch Condition Input Timing

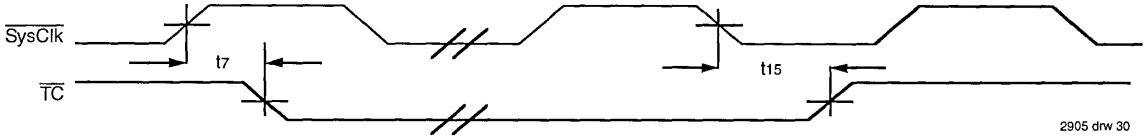
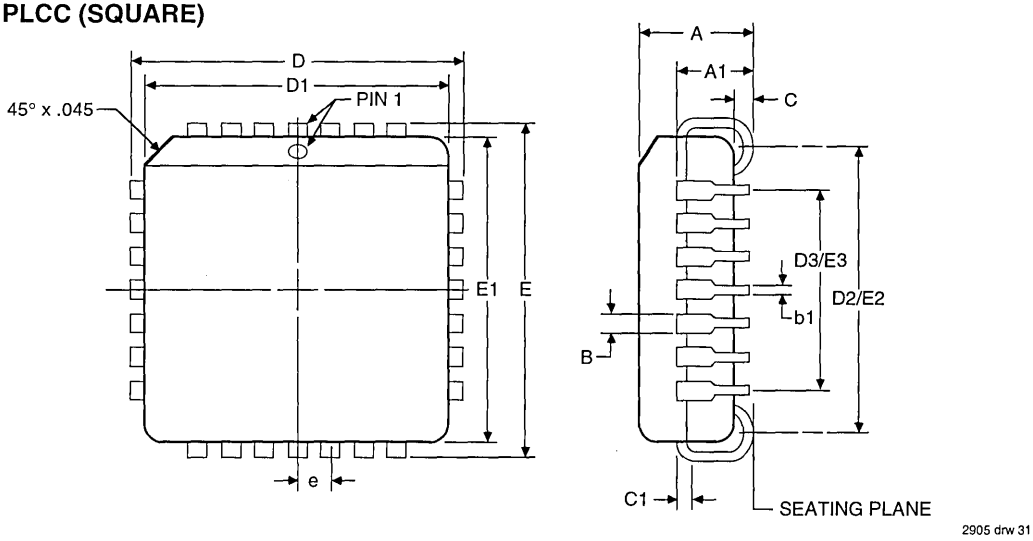


Figure 25. $\overline{TC}$ Output

84 LEAD PLCC (SQUARE)

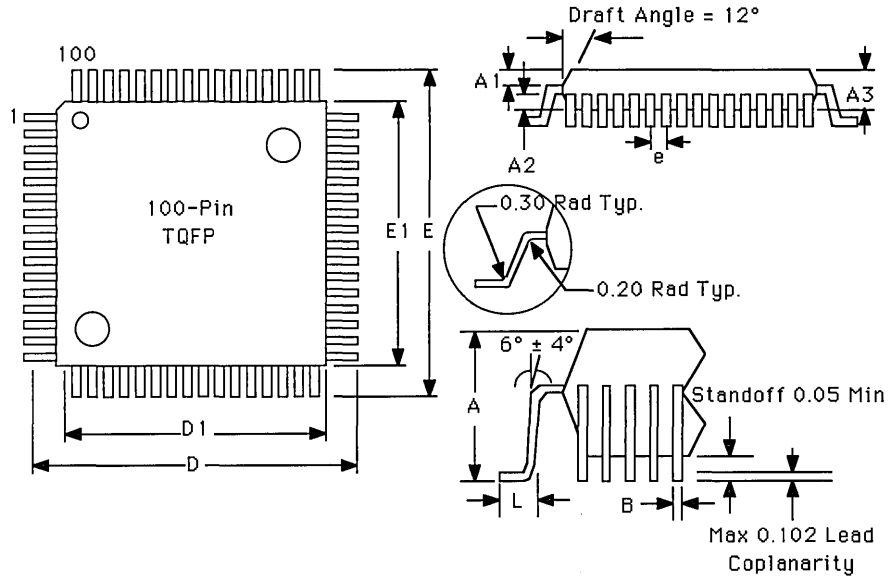


DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

2905 tbl 13

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. PLCC is pin & form compatible with MQUAD; the MQUAD package is used in other R3051 family members.

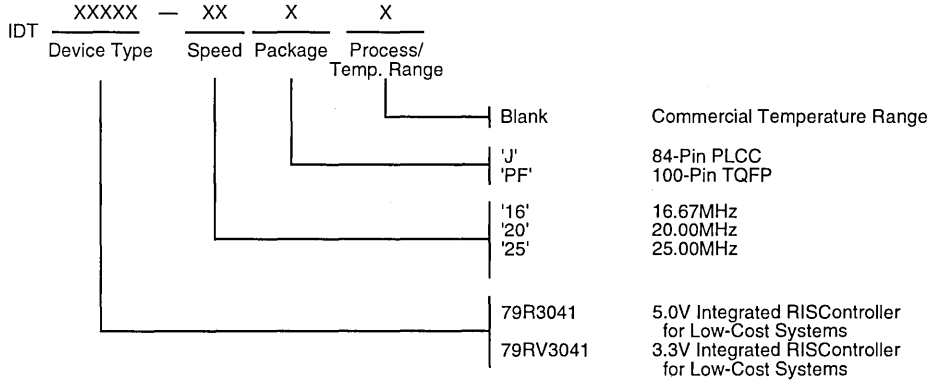
100-PIN TQFP



DWG #	TQFP	
# of Leads	100	
Symbol	Min.	Max.
A	—	1.60
A1	0.5	0.15
A2	1.35	1.45
D	15.75	16.25
D1	13.95	14.05
E	15.75	16.25
E1	13.95	14.05
L	0.45	0.70
N	100	
e	0.50BSC	
b	0.17	0.27
ccc	—	0.08
ddd	—	0.08
R	0.08	0.20
R1	0.08	—
θ	0	7.0
θ1	11.0	13.0
θ2	11.0	13.0
c	0.09	0.16

2905 tbl 14

ORDERING INFORMATION



2905 drw 32

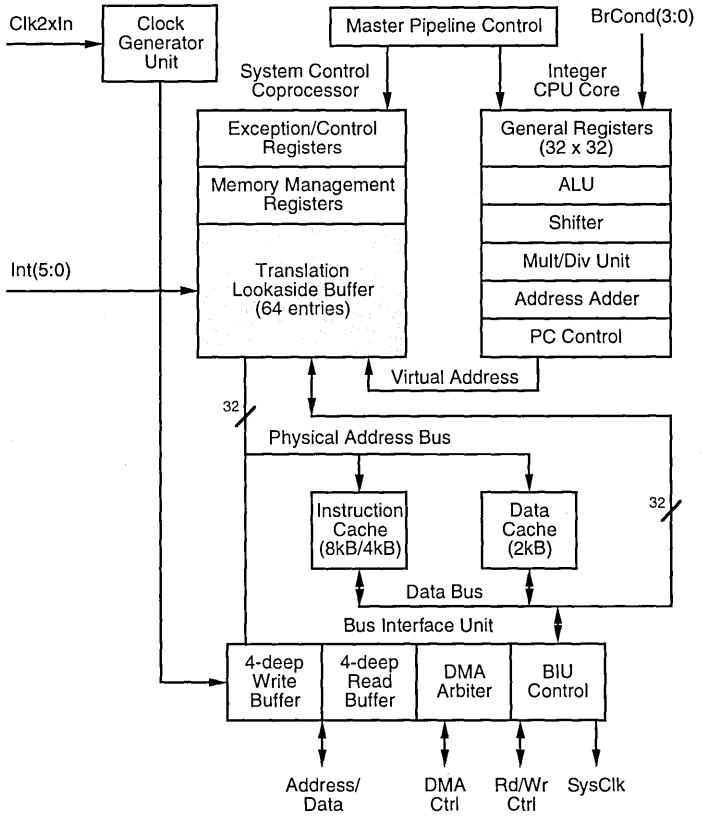
VALID COMBINATIONS

IDT	79R3041 - 16	TQFP, PLCC Package
	79R3041 - 20	TQFP, PLCC Package
	79R3041 - 25	TQFP, PLCC Package
	79RV3041 - 16	TQFP, PLCC Package
	79RV3041 - 20	TQFP, PLCC Package
	79RV3041 - 25	TQFP, PLCC Package

FEATURES:

- Instruction set compatible with IDT79R3000A and IDT79R3001 MIPS RISC CPUs
- High level of integration minimizes system cost, power consumption
  - IDT79R3000A /IDT79R3001 RISC Integer CPU
  - R3051 features 4KB of Instruction Cache
  - R3052 features 8KB of Instruction Cache
  - All devices feature 2kB of Data Cache
  - "E" Versions (Extended Architecture) feature full function Memory Management Unit, including 64-entry Translation Lookaside Buffer (TLB)
  - 4-deep write buffer eliminates memory write stalls
  - 4-deep read buffer supports burst refill from slow memory devices
  - On-chip DMA arbiter
  - Bus Interface minimizes design complexity
- Single clock input with 40%-60% duty cycle
- 35 MIPS, over 64,000 Dhrystones at 40MHz
- Low-cost 84-pin PLCC packaging that's pin-/package-compatible with thermally enhanced 84-pin MQUAD.
- Flexible bus interface allows simple, low-cost designs
- 20, 25, 33, and 40MHz operation
- Complete software support
  - Optimizing compilers
  - Real-time operating systems
  - Monitors/debuggers
  - Floating Point Software
  - Page Description Languages

5



2874 drw 01

Figure 1. R3051 Family Block Diagram

INTRODUCTION

The IDT IDT79R3051 family is a series of high-performance 32-bit microprocessors featuring a high level of integration which are targeted to high-performance, but cost-sensitive embedded processing applications. The IDT79R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Functional units were integrated onto the CPU core in order to reduce the total system cost, without significantly degrading system performance. Thus, the IDT79R3051 family is able to offer 35MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Furthermore, the IDT79R3051 family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging for devices up to 25 MHz. The IDT79R3051 family allows customer applications to bring maximum performance at minimum cost.

Figure 1 shows a block-level representation of the functional units within the IDT79R3051 family. The IDT79R3051 family could be viewed as the embodiment of a discrete solution built around the IDT79R3000A or IDT79R3001. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Currently, there are four members of the IDT79R3051 family. All devices are pin- and software-compatible: the differences lie in the amount of instruction cache, and in the memory management capabilities of the processor:

- The IDT79R3052"E" incorporates 8kB of Instruction Cache, and features a full-function Memory Management Unit (MMU), including a 64-entry fully-associative Translation Lookaside Buffer (TLB). This is the same MMU incorporated into the IDT79R3000A and IDT79R3001.
- The IDT79R3052 also incorporates 8kB of Instruction Cache. However, the MMU is a much simpler subset of the capabilities of the enhanced versions of the architecture, and in fact does not use a TLB.
- The IDT79R3051"E" incorporates 4KB of Instruction Cache. Additionally, this device features the same full-function MMU (including TLB file) as the IDT79R3052"E", and IDT79R3000A.
- The IDT79R3051 incorporates 4KB of Instruction Cache, and uses the simpler memory management model of the IDT79R3052.

An overview of the functional blocks incorporated in these devices follows.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close-to single cycle execution rate. The CPU core contains a five stage pipeline and 32 orthogonal 32-bit registers. The IDT79R3051 family implements the MIPS ISA. In fact, the execution engine of the IDT79R3051 family is the same as the execution engine of the IDT79R3000A (and IDT79R3001). Thus the IDT79R3051 family is binary-compatible with those CPU engines.

The execution engine of the IDT79R3051 family uses a five-stage pipeline to achieve close-to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved by the IDT79R3051 family pipeline.

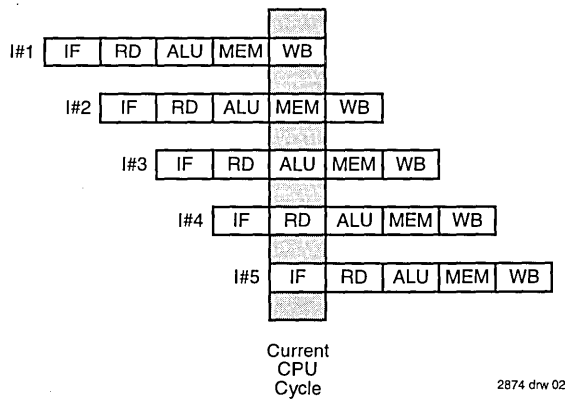


Figure 2. R3051 Family 5-Stage Pipeline

System Control Co-Processor

The R3051 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the IDT79R3051 family, as well as the virtual to physical mapping of the IDT79R3051 family.

There are two versions of the IDT79R3051 family architecture: the Extended Architecture Versions (the IDT79R3051E and IDT79R3052E) contain a fully associative 64-entry TLB which maps 4KB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard mapped to physical addresses, and kernel and user segments which are mapped on a page basis by the TLB into anywhere within the 4GB physical address space. In this TLB, 8-page translations can be "locked" by the kernel to insure deterministic response in real-time applications. These versions thus use the same MMU structure as that found in the IDT79R3000A and IDT79R3001. Figure 3 shows the virtual-to-physical address mapping found in the Extended Architecture versions of the processor family.

The Extended Architecture devices allow the system designer to implement kernel software to dynamically manage User task utilization of memory resources, and also allow the Kernel to effectively "protect" certain resources from user tasks. These capabilities are important in a number of embedded applications, from process control (where resource protection may be extremely important) to X-Window display systems (where virtual memory management is extremely important), and can also be used to simplify system debugging.

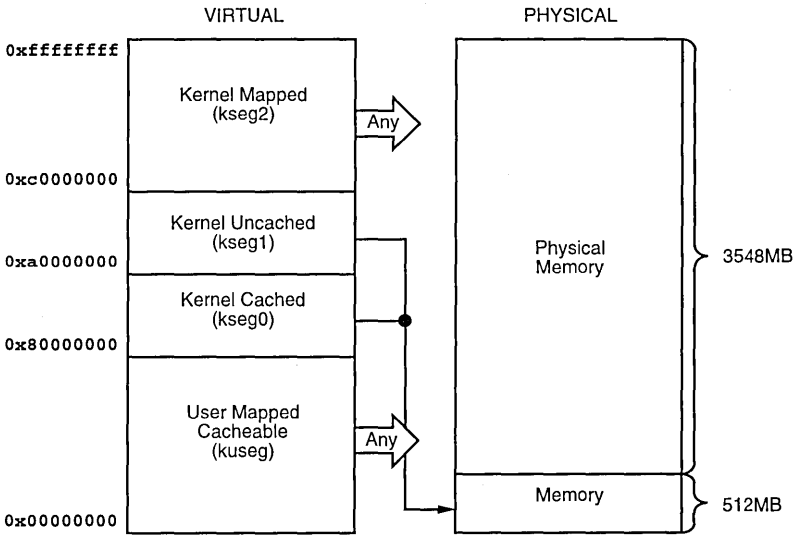


Figure 3. Virtual-to-Physical Mapping of Extended Architecture Versions

5

The base versions of the architecture (the IDT79R3051 and IDT79R3052) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. The base processors support distinct kernel and user mode operation without requiring page management software, leading to a simpler software model. The memory mapping used by these devices is illustrated in Figure 4. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

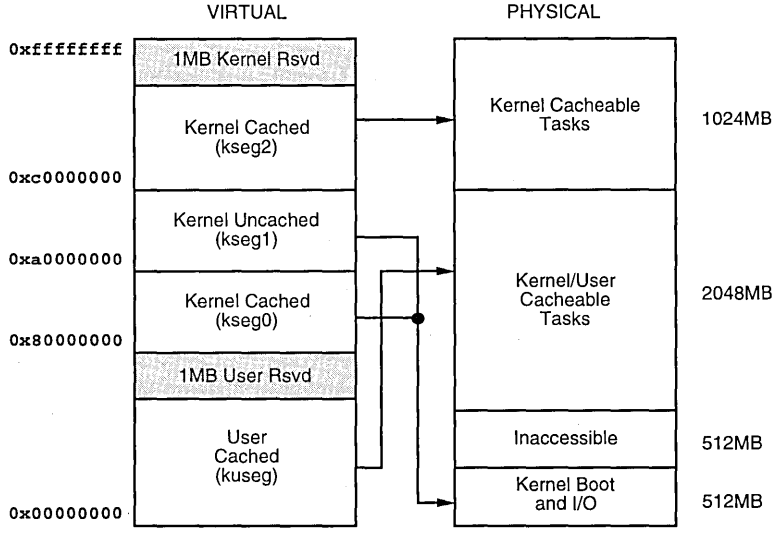


Figure 4. Virtual-to-Physical Mapping of Base Architecture Versions

Clock Generation Unit

The IDT79R3051 family is driven from a single input clock, capable of operating in a range of 40%-60% duty cycle. On chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in IDT79R3000A and IDT79R3001 based applications.

Instruction Cache

The current family includes two different instruction cache sizes: the IDT79R3051 family (the IDT79R3051 and IDT79R3051E) feature 4KB of instruction cache, and the IDT79R3052 and IDT79R3052E each incorporate 8KB of Instruction Cache. For all four devices, the instruction cache is organized as a line size of 16 bytes (four words). This relatively large cache achieves a hit rate well in excess of 95% in most applications, and substantially contributes to the performance inherent in the IDT79R3051 family. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

Data Cache

All four devices incorporate an on-chip data cache of 2KB, organized as a line size of 4 bytes (one word). This relatively large data cache achieves hit rates well in excess of 90% in most applications, and contributes substantially to the performance inherent in the IDT79R3051 family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The IDT79R3051 family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The IDT79R3051 family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE signal to demultiplex the A/D bus, and simple handshake signals to process processor read and write requests. In addition to the read and write interface, the IDT79R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The IDT79R3051 family incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and presents it to the bus interface as write transactions at the rate the memory system can accommodate.

The IDT79R3051/52 read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving), if desired, in high-performance systems, or use simpler techniques to reduce complexity.

In order to accommodate slower quad-word reads, the IDT79R3051 family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches. Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize the read buffer to process quad word reads from slower memory systems.

SYSTEM USAGE

The IDT79R3051 family has been specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems utilize slow EPROMs, DRAMs, and application-specific peripherals. These systems may also typically contain large, slow Static RAMs, although the IDT79R3051 family has been designed to not specifically require the use of external SRAMs.

Figure 5 shows a typical system block diagram. Transparent latches are used to de-multiplex the IDT79R3051/52 address and data busses from the A/D bus. The data paths between the memory system elements and the R3051 family A/D bus is managed by simple octal devices. A small set of simple PALs can be used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

DEVELOPMENT SUPPORT

The IDT79R3051 family is supported by a rich set of development tools, ranging from system simulation tools through prom monitor support, logic analysis tools, and subsystem modules.

Figure 7 is an overview of the system development process typically used when developing IDT79R3051 family-based applications. The IDT79R3051 family is supported by powerful tools through all phases of project development. These tools allow timely, parallel development of hardware and software for IDT79R3051/52 based applications, and include tools such as:

- A program, Cache-3051, which allows the performance of an IDT79R3051 family based system to be modeled and understood without requiring actual hardware.

- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- IDT Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, which has been integrated into the compiler toolchain to allow software floating point to replace hardware floating point without modifying the original source code.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT Prom Monitor.
- The IDT Laser Printer System board, which directly drives a low-cost print engine, and runs Microsoft TrueImage™ Page Description Language on top of PeerlessPage™ Advanced Printer Controller BIOS.
- Adobe PostScript™ Page Description Language, ported to the R3000 instruction set, runs on the IDT79R3051 family.
- The IDT Prom Monitor, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- An In-Circuit Emulator, developed and sold by Embedded Performance, Inc.

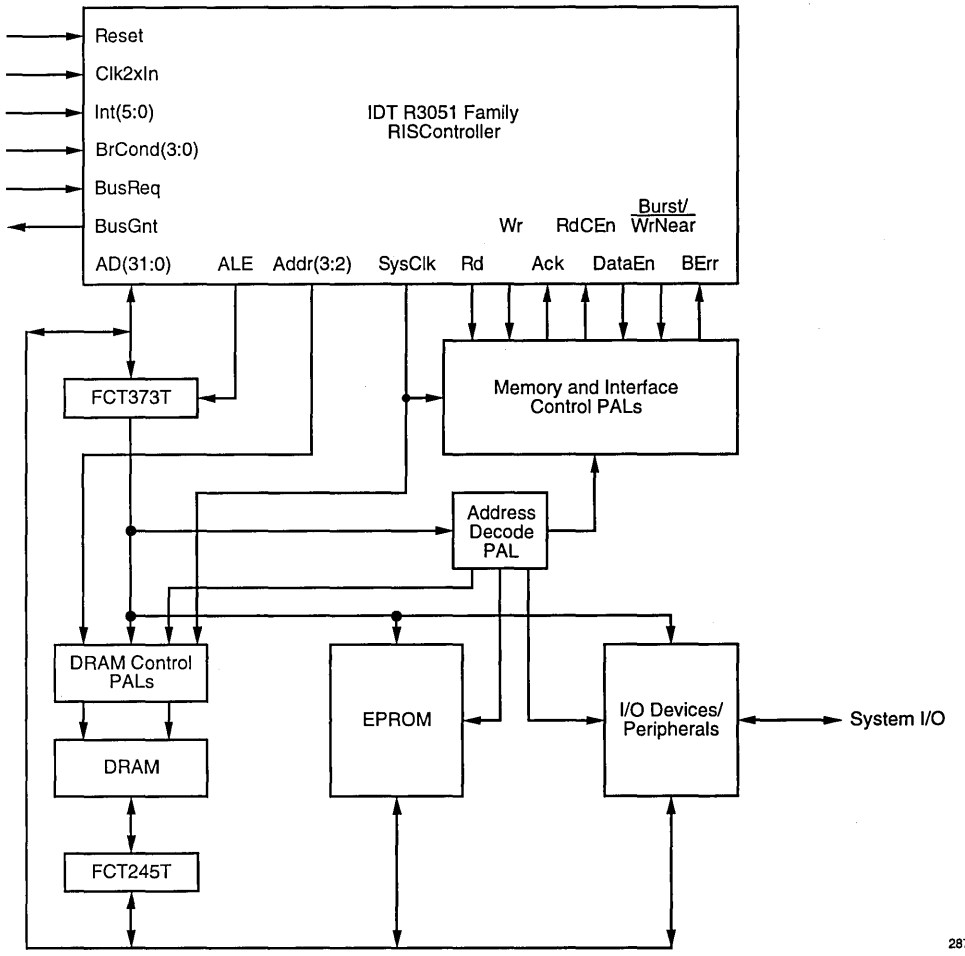


Figure 5. Typical R3051 Family Based System

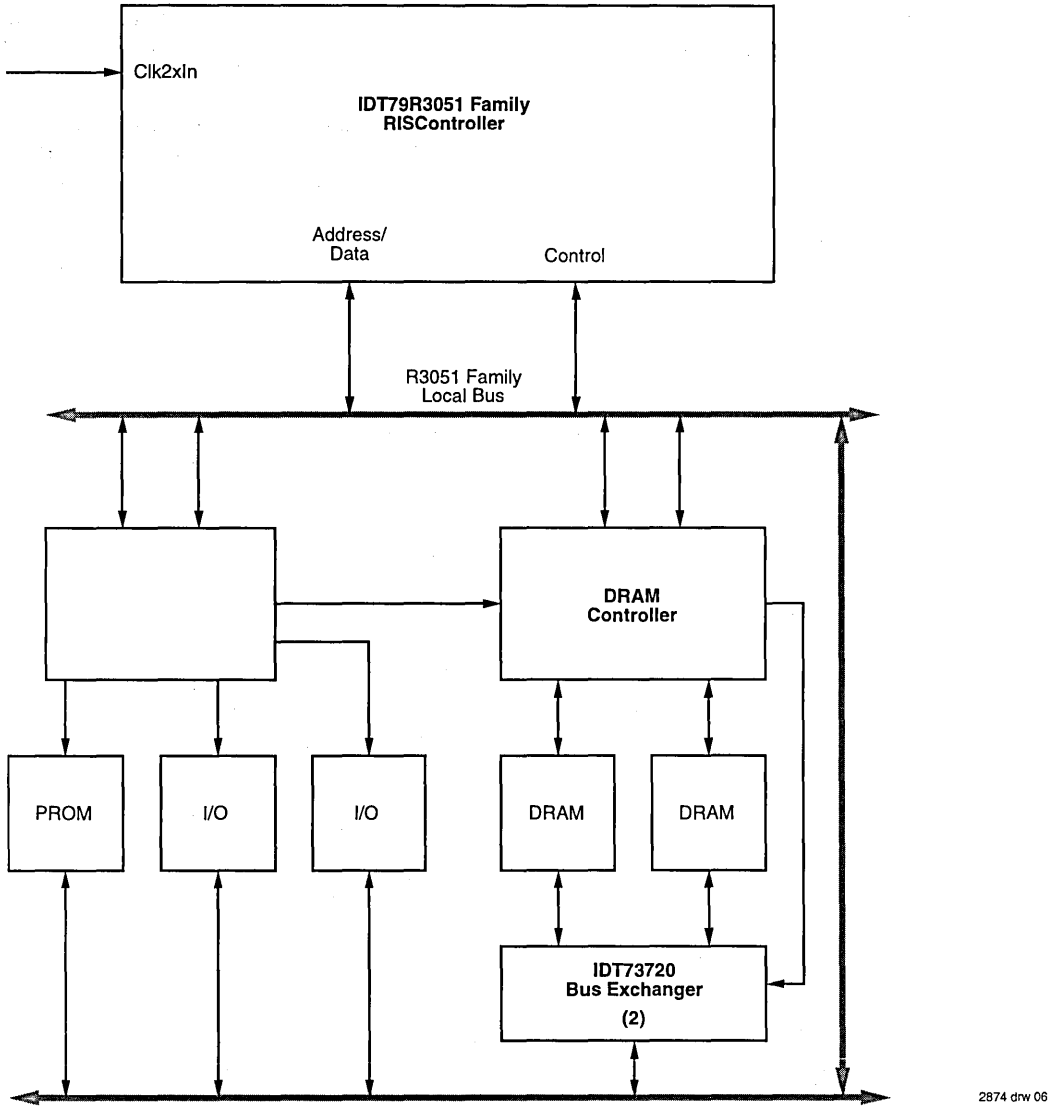


Figure 6. R3051 Family Chip Set Based System

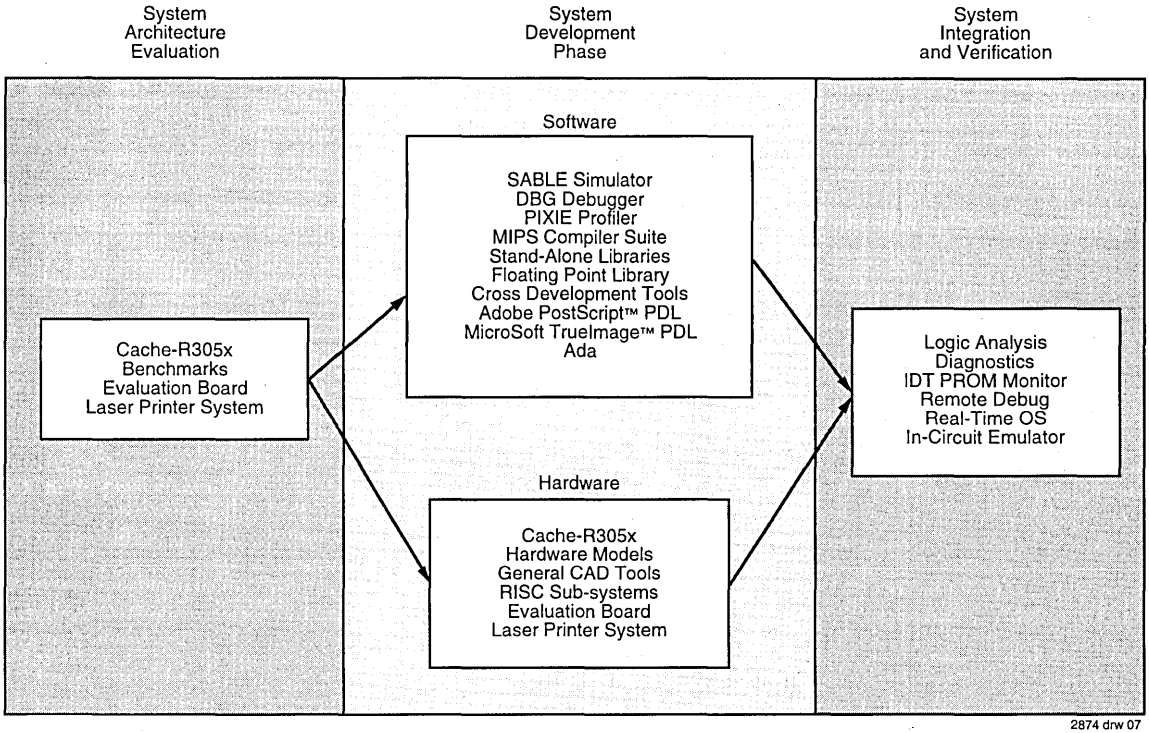


Figure 7. R3051 Family Development Toolchain

5

PERFORMANCE OVERVIEW

The IDT79R3051 family achieves a very high level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations at a single cycle rate, and has an effective load time of 1.3 cycles, and a branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35MIPS performance when operating out of cache.
- **Large on-chip caches.** The IDT79R3051 family contains caches which are substantially larger than those on the majority of today's embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance, very close to its peak execution rate.
- **Autonomous multiply and divide operations.** The IDT79R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the IDT79R3051 family to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The IDT79R3051 family features a four-deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The IDT79R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve 35MIPS integer performance, and over 64,000 dhrystones at 40MHz without the use of external caches or zero wait-state memory devices.

SELECTABLE FEATURES

The IDT79R3051 family allows the system designer to configure some aspects of operation. These aspects are established when the device is reset and include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits intercommunications between various types of processors and databases.
- **Data cache refill of one or four words:** The memory system must be capable of performing 4-word transfers to satisfy cache misses. This option allows the system designer to choose between one- and four-word refill on data cache misses, depending on the performance each option brings to his application.

THERMAL CONSIDERATIONS

The IDT79R3051 family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the IDT79R3051 family are packaged in cavity-down packaging.

The lowest cost members of the family use a standard cavity-down, injection molded PLCC package (the "J" package). This package, coupled with the power reduction techniques employed in the design of the IDT79R3051 family, allows operation at speeds to 25MHz. However, at higher speeds, additional thermal care must be taken.

For this reason, the IDT79R3051 family is also available in the MQUAD package (the "MJ" package), which is an all-aluminum package with the die attached to a normal copper lead-frame, mounted to the aluminum casing. The MQUAD allows for more efficient thermal transfer between the die and the case of the part due to the heat-spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, which reduces the temperature gradient across the package, and, therefore, presents a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin- and form-compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

The members of the IDT79R3051 family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 1 for the various packages.

	Airflow (ft/min)					
ØCA	**0**	**200**	**400**	**600**	**800**	**1000**
"J" Package	29	26	21	18	16	15
"MJ" Package*	22	14	12	11	9	8

2874 tbl 01

Table 1. Thermal Resistance ($Ø_{CA}$) at Various Airflows
(*estimated: final values tbd)

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are represented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss. The value of this pin at this time in other than read cycles is undefined. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.

2874 tbl 02

5

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Burst}}$/ $\overline{\text{WrNear}}$	O	**Burst Transfer/Write Near:** On read transactions, the $\overline{\text{Burst}}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if selected at device reset time. On write transactions, the $\overline{\text{WrNear}}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{\text{Rd}}$	O	**Read:** An output which indicates that the current bus transaction is a read.
$\overline{\text{Wr}}$	O	**Write:** An output which indicates that the current bus transaction is a write.
$\overline{\text{Ack}}$	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer.
$\overline{\text{RdCEn}}$	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{\text{SysClk}}$	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
$\overline{\text{BusReq}}$	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{\text{BusGnt}}$	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a $\overline{\text{BusReq}}$ has been detected, and that the bus is relinquished to the external master.
SBrCond(3:2) BrCond(1:0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously.
$\overline{\text{BErr}}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{\text{Int}}$(5:3) $\overline{\text{SInt}}$(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{\text{Int}}$(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{\text{SInt}}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
Clk2xIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{\text{Reset}}$	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{\text{Reset}}$.
Rsvd(4:0)	I/O	**Reserved:** These five signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins.

2874 tbl 03

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
VIN	Input Voltage	–0.5 to +7.0	V

2874 tbl 04

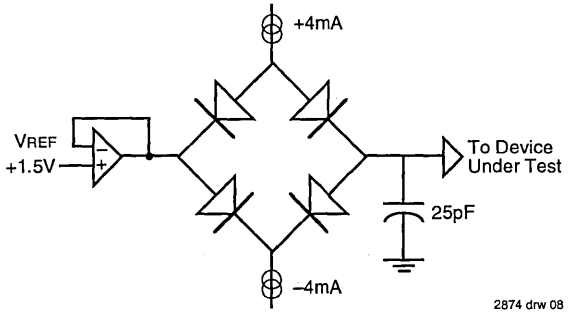
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2874 tbl 06

OUTPUT LOADING FOR AC TESTING



2874 drw 08

AC TEST CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0	V

2874 tbl 05

DC ELECTRICAL CHARACTERISTICS (TC = 0°C to +85°C, VCC = +5.0V ±5%)

			20MHz		25MHz		33.33MHz		40MHz		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = Min., IOH = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
VILS	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
CIN	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
COUT	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
ICC	Operating Current	VCC = 5V, TC = 25°C	—	350	—	400	—	450	—	500	mA
IIH	Input HIGH Leakage	VIH = VCC	—	100	—	100	—	100	—	100	µA
IIL	Input LOW Leakage	VIL = GND	–100	—	–100	—	–100	—	–100	—	µA
IOZ	Output Tri-state Leakage	VOH = 2.4V, VOL = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

2874 tbl 07

NOTES:
1. VIL Min. = –3.0V for pulse width less than 15ns. VIL should not fall below –0.5V for larger periods.
2. VIHS and VILS apply to Clk2xIn and $\overline{\text{Reset}}$.
3. VIH should not be held above VCC + 0.5V.
4. Guaranteed by design.

5

AC ELECTRICAL CHARACTERISTICS [1, 2, 3] (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

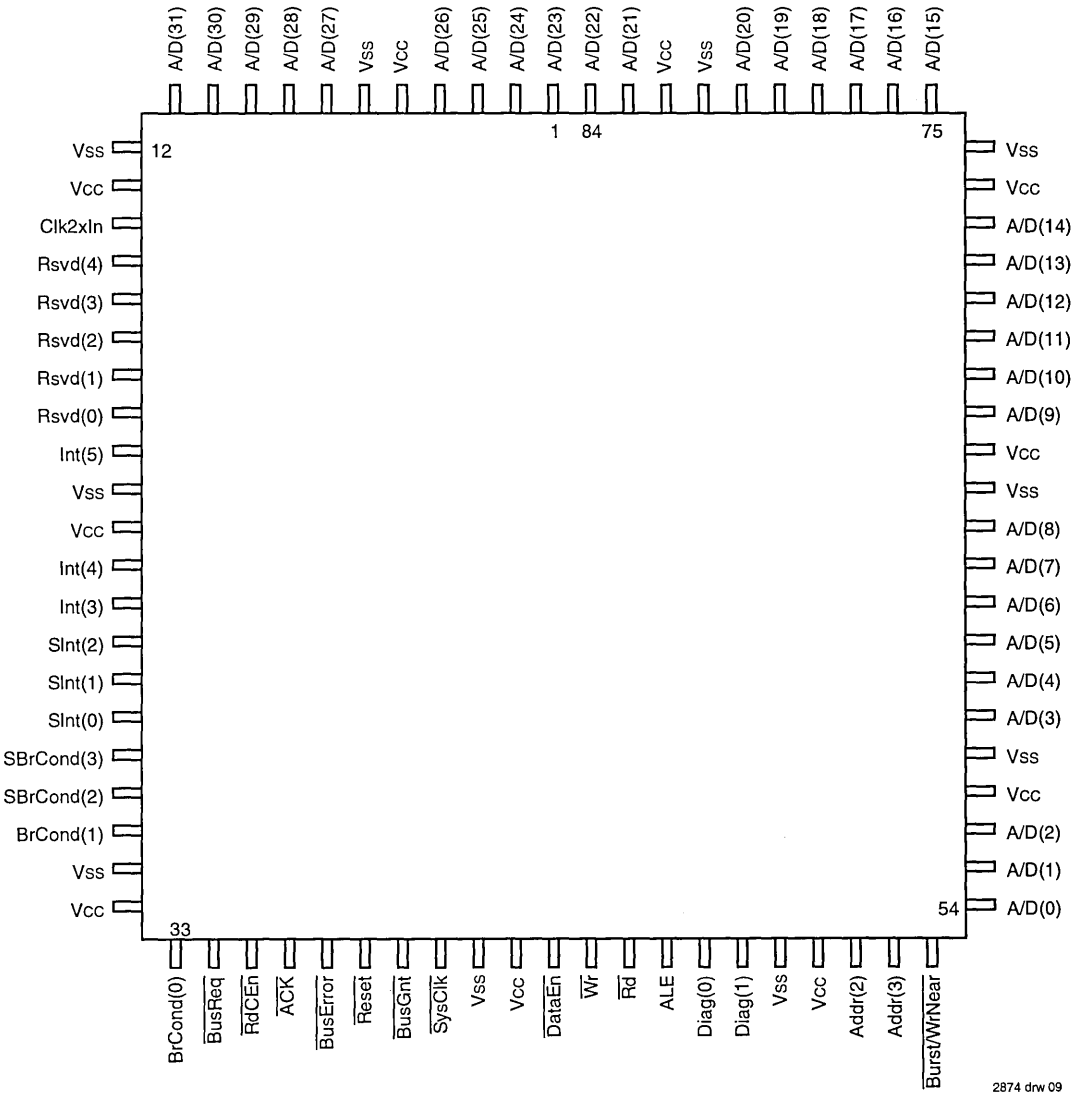
Symbol	Signals	Description	20MHz		25MHz		33.33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn,	Set-up to SysClk rising	6	—	5	—	4	—	3	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	5	—	4.5	—	ns
t2	BusReq, Ack, BusError, RdCEn,	Hold from SysClk rising	4	—	4	—	3	—	3	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	—	6	—	5	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	—	6	—	5	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	—	4	—	3.5	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	—	3	—	3	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	—	3	—	3	ns
t10	A/D	Hold from ALE negated	2	—	2	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state[4]	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising[4]	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	—	5	—	4	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	—	5	—	4.5	ns
t17	Diag	Valid from SysClk	—	12	—	11	—	10	—	9	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	—	9	—	8	ns
t19	A/D	SysClk falling to data out	—	12	—	11	—	10	—	9	ns
t20	Clk2xIn	Pulse Width HIGH	10	—	8	—	6.5	—	5.6	—	ns
t21	Clk2xIn	Pulse Width LOW	10	—	8	—	6.5	—	5.6	—	ns
t22	Clk2xIn	Clock Period	25	250	20	250	15	250	12.5	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t26	Int	Mode set-up to Reset rising	6	—	5	—	4	—	3	—	ns
t27	Int	Mode hold from Reset rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	Sint, SBrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t29	Sint, SBrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	4	—	3	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	3	—	2	—	2	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	
t32	SysClk	Clock HIGH Time	t22 – 2	t22 + 2	t22 – 2	t22 + 2	t22 – 1	t22 + 1	t22 – 1	t22 + 1	ns
t33	SysClk	Clock LOW Time	t22 – 2	t22 + 2	t22 – 2	t22 + 2	t22 – 1	t22 + 1	t22 – 1	t22 + 1	ns
tderate	All outputs	Timing deration for loading over 25pf[4, 5]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

NOTES:

2874 tbl 08

1. All timings referenced to 1.5V, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3051 Family Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.

PIN CONFIGURATIONS



84-Pin PLCC/MQUAD
Top View

NOTE:
Reserved Pins must not be connected.

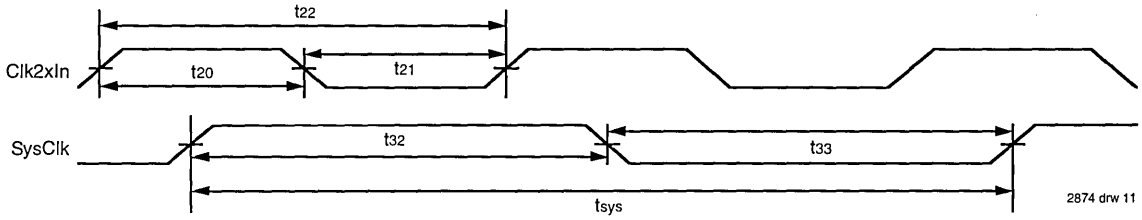


Figure 8. R3051 Family Clocking

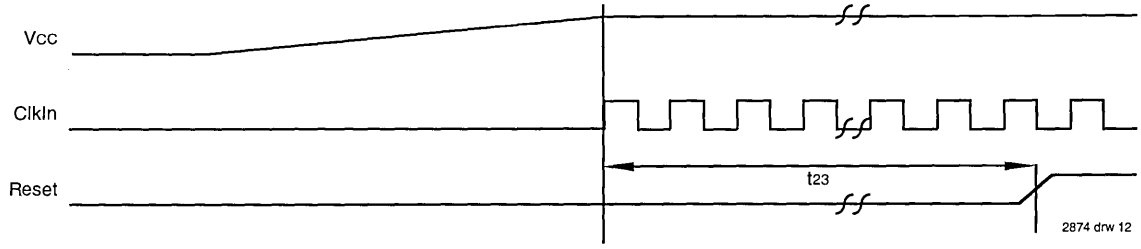


Figure 9. Power-On Reset Sequence

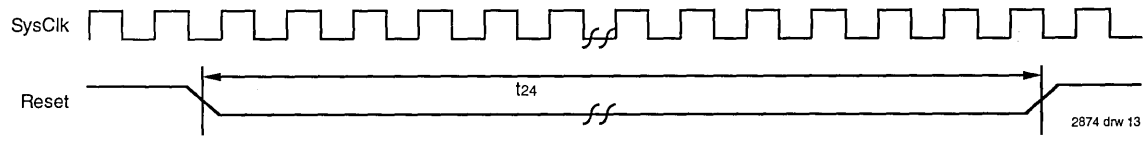


Figure 10. Warm Reset Sequence

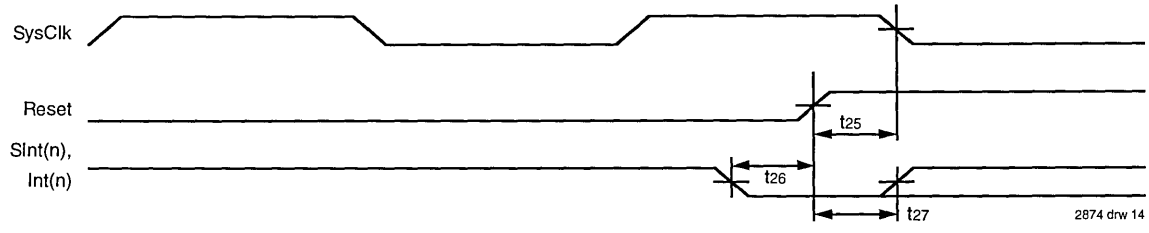


Figure 11. Mode Selection and Negation of Reset

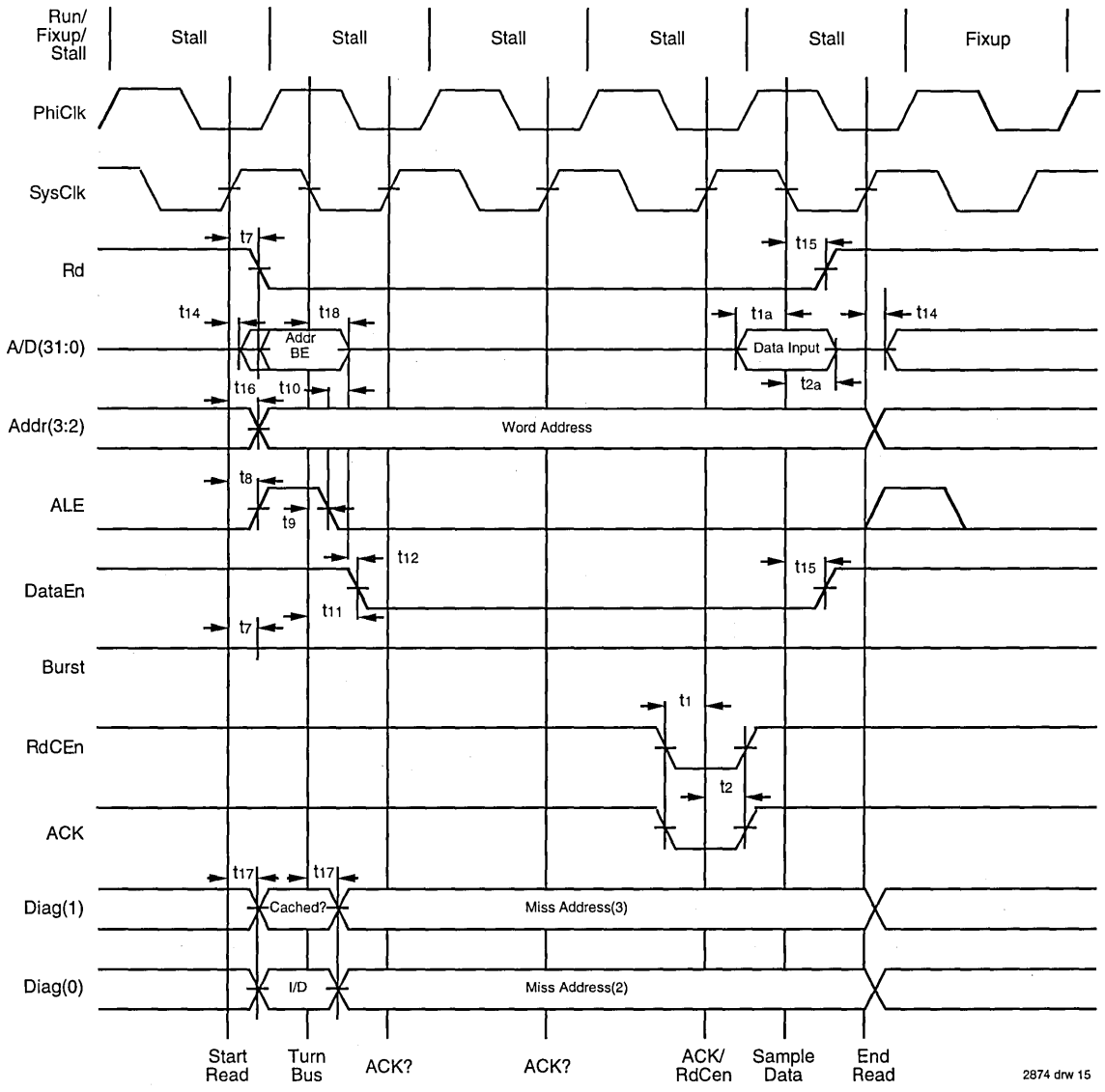


Figure 12. Single Datum Read in R3051 Family

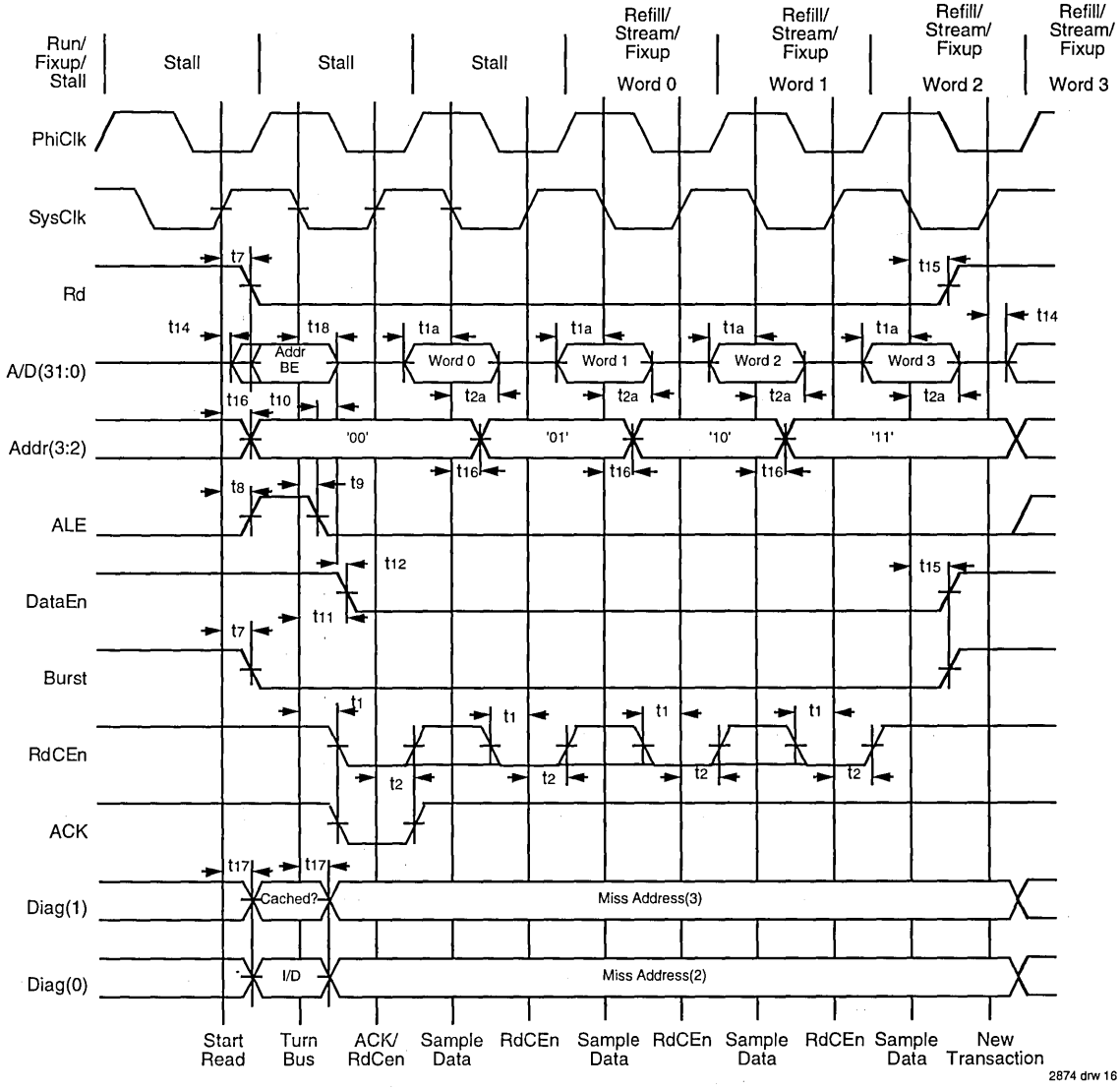


Figure 13. R3051 Family Burst Read

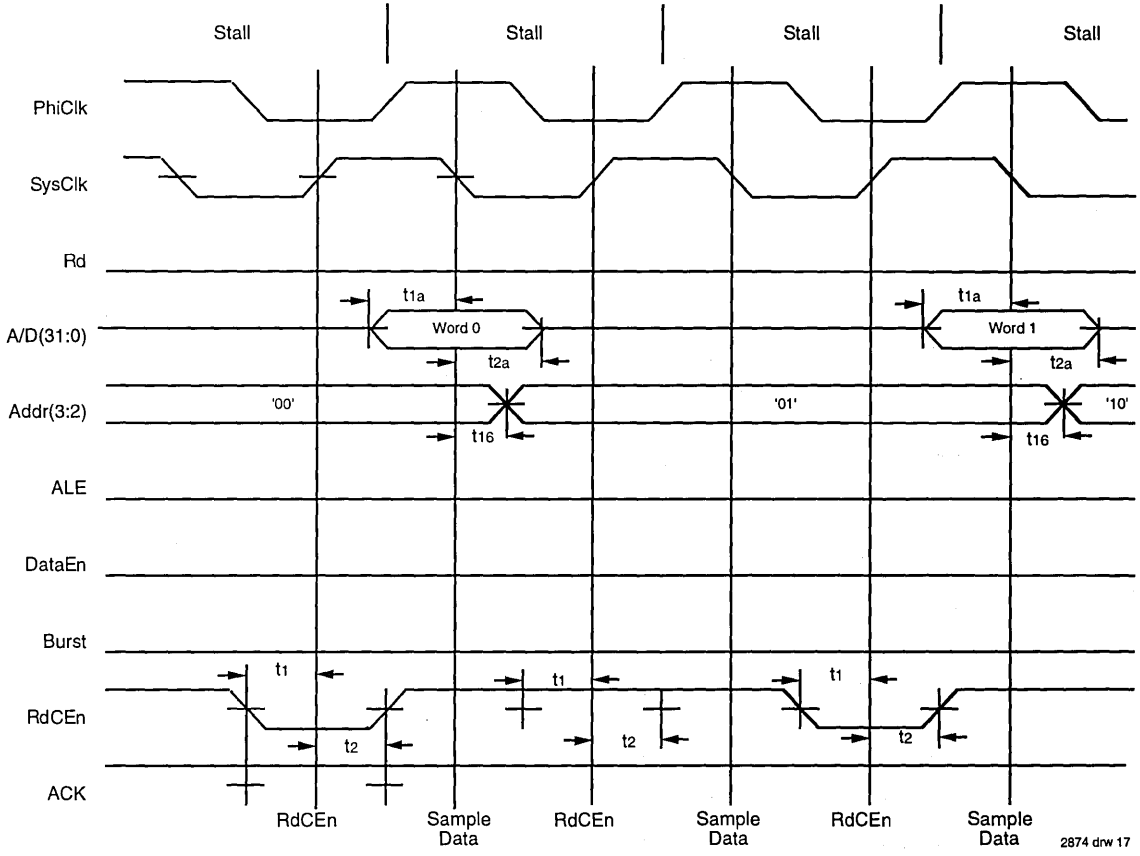


Figure 14 (a). Start of Throttled Quad Read

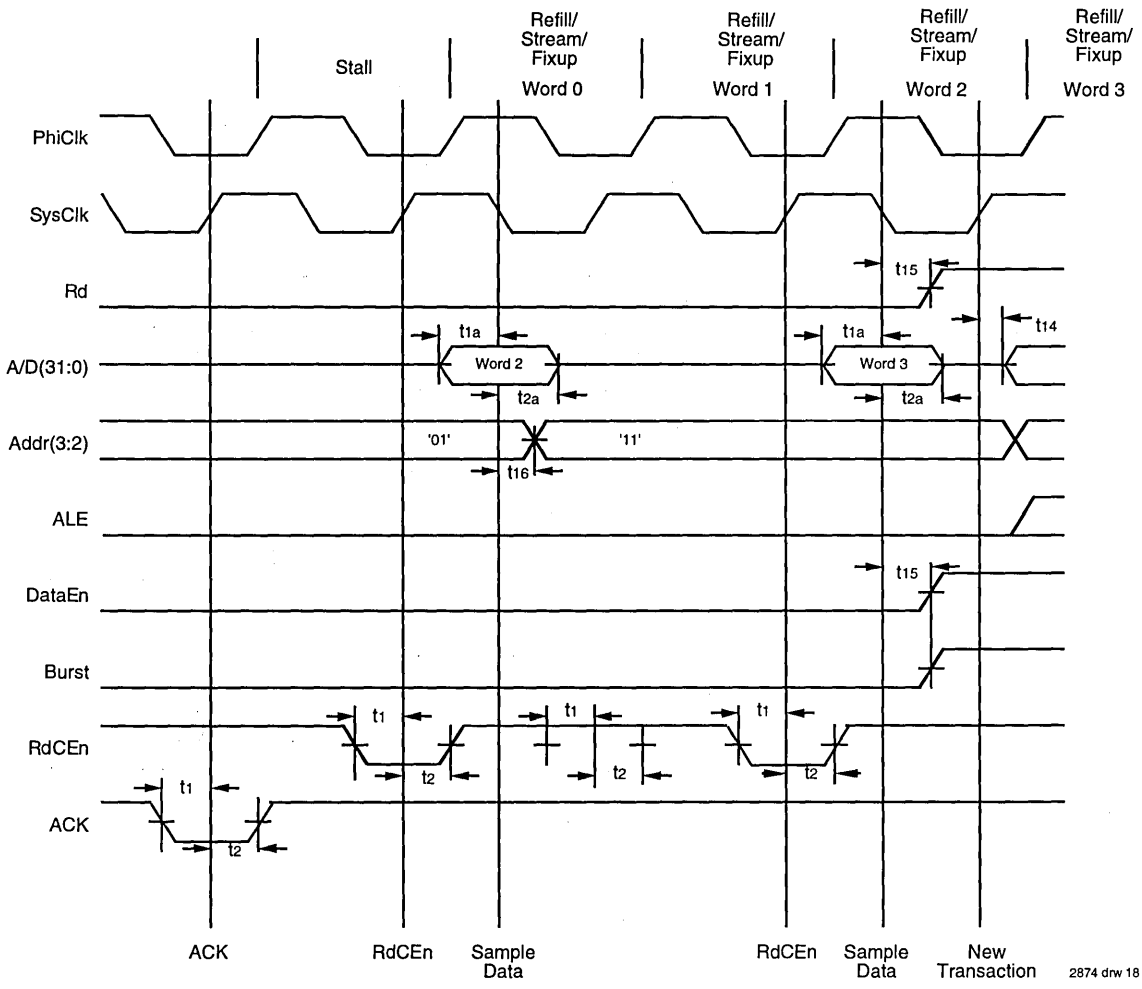


Figure 14 (b). End of Throttled Quad Read

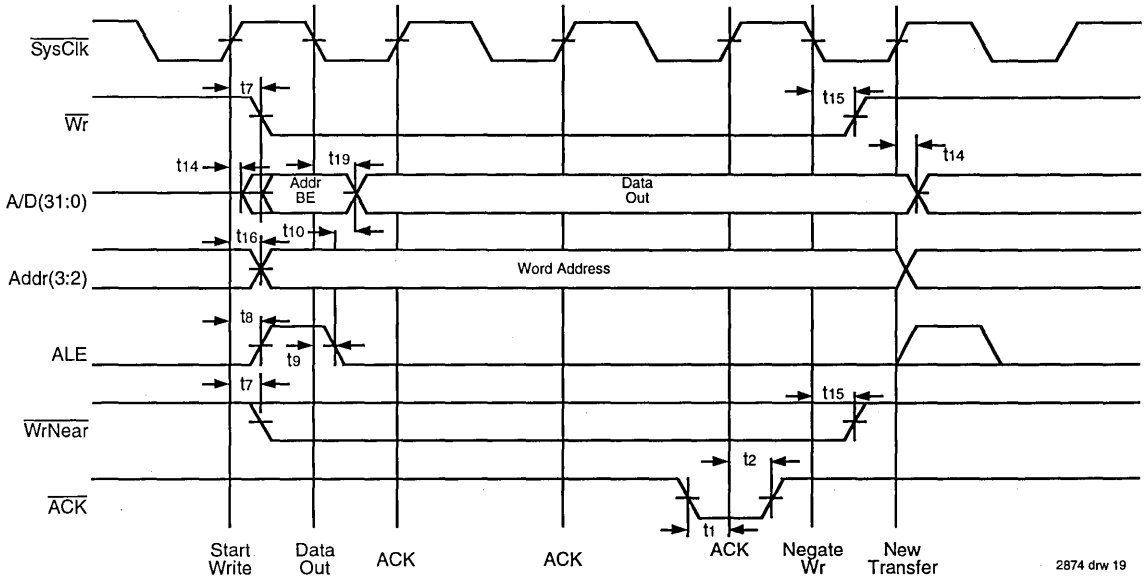


Figure 15. R3051 Family Write Cycle

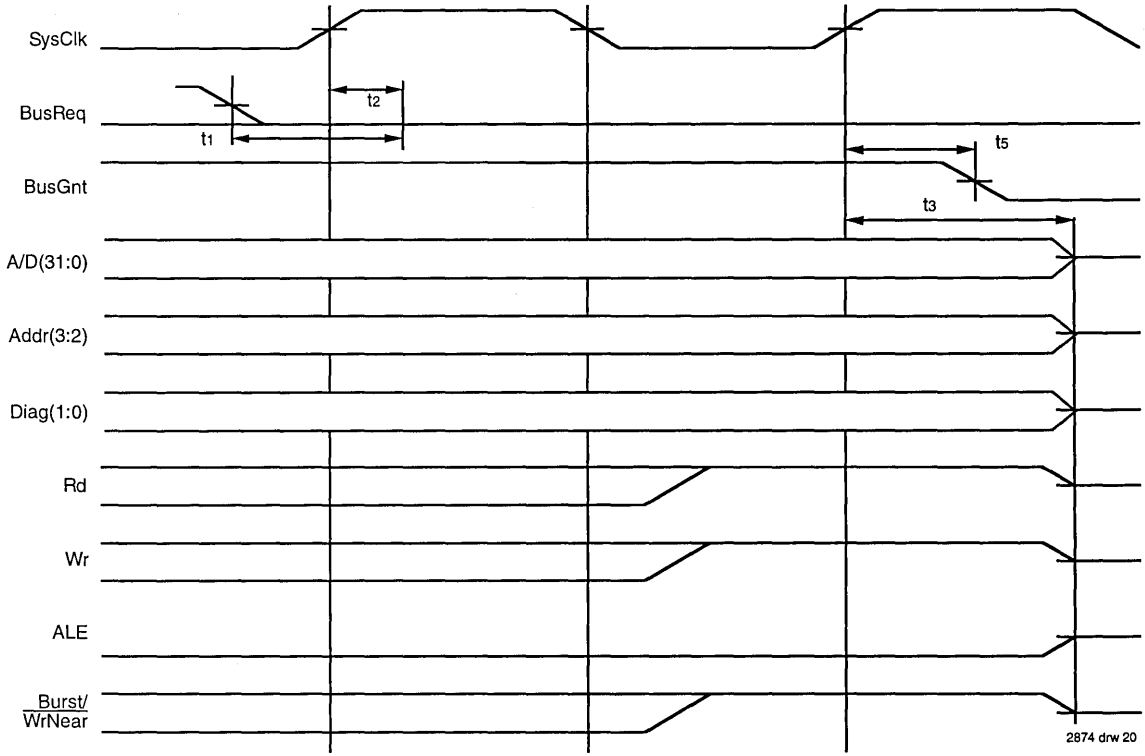


Figure 16. Request and Relinquish of R3051 Family Bus to External Master

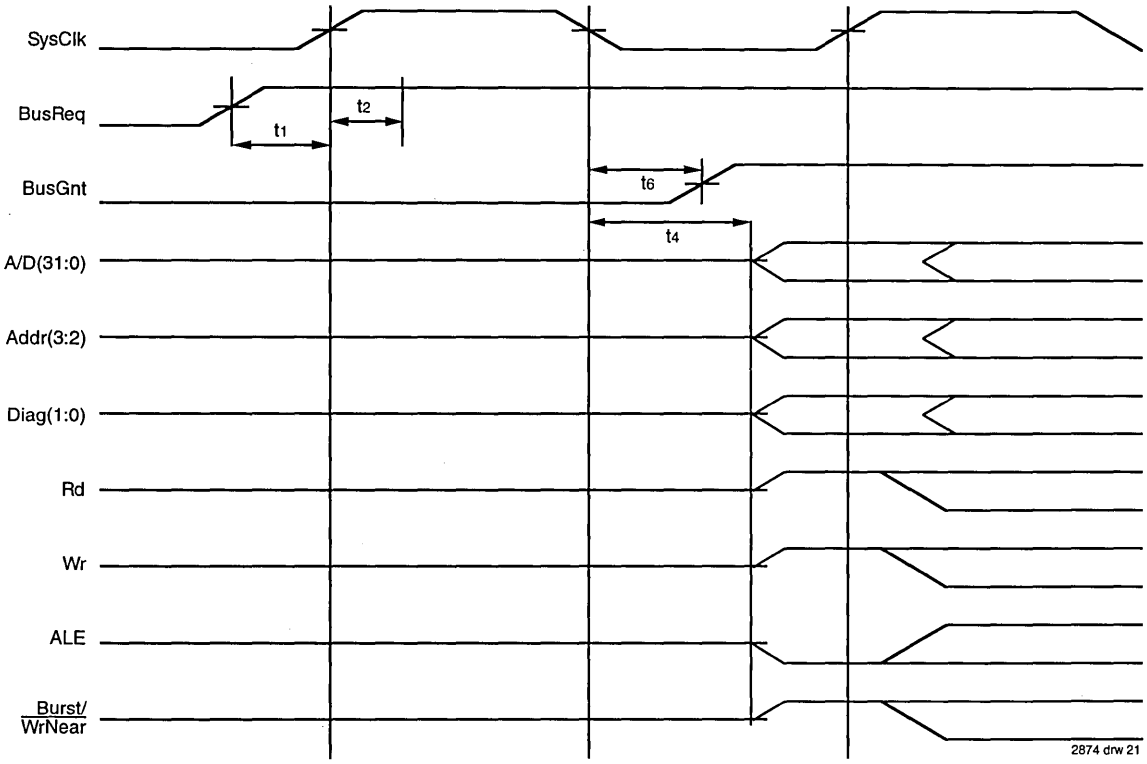


Figure 17. R3051 Family Regaining Bus Mastership

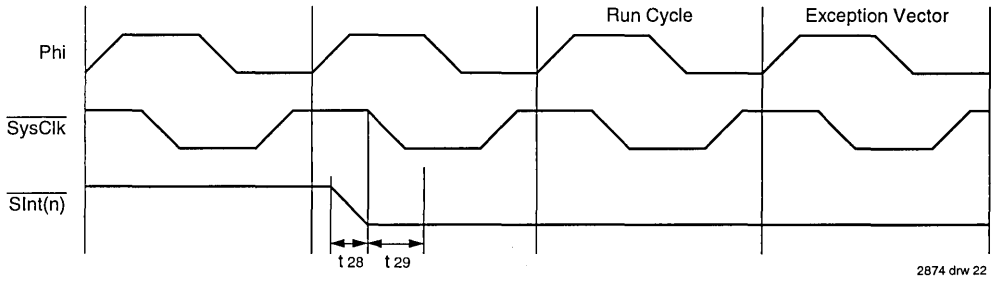


Figure 18. Synchronized Interrupt Input Timing

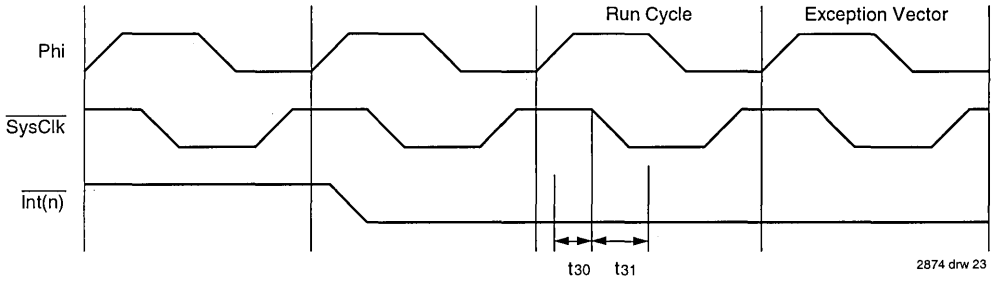


Figure 19. Direct Interrupt Input Timing

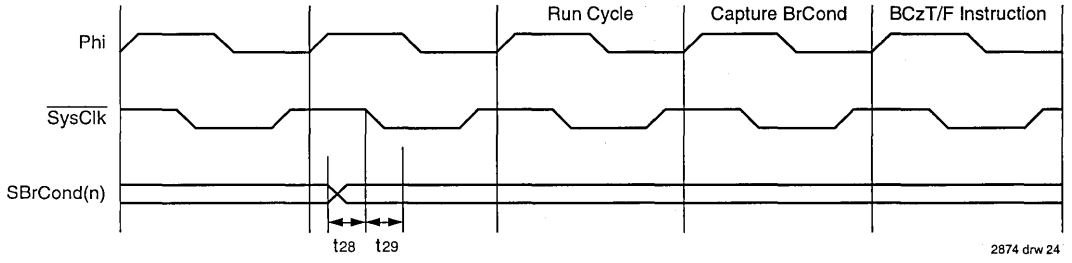


Figure 20. Synchronized Branch Condition Input Timing

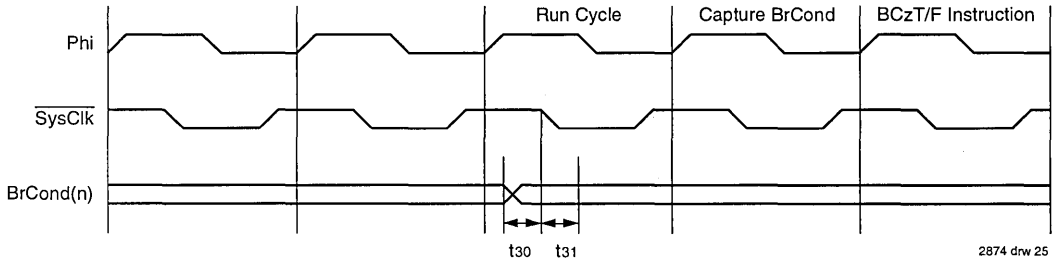
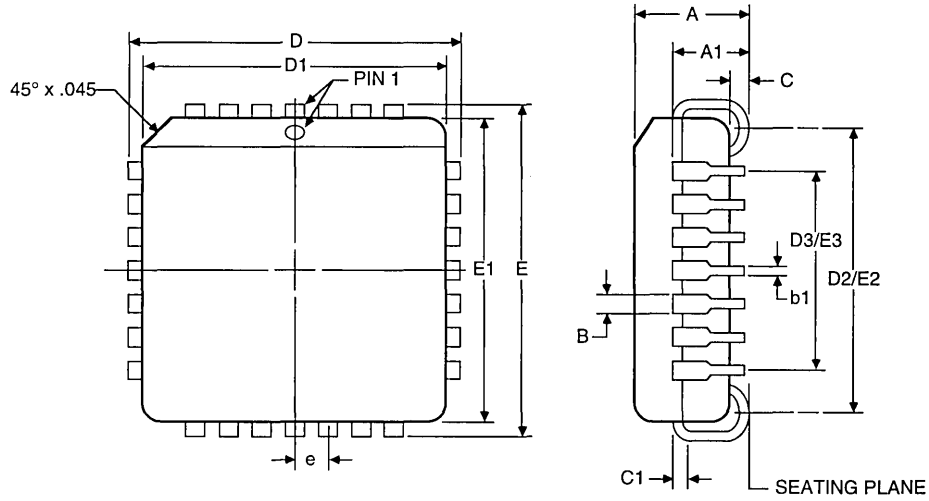


Figure 21. Direct Branch Condition Input Timing

84 LEAD PLCC/MQUAD[7] (SQUARE)



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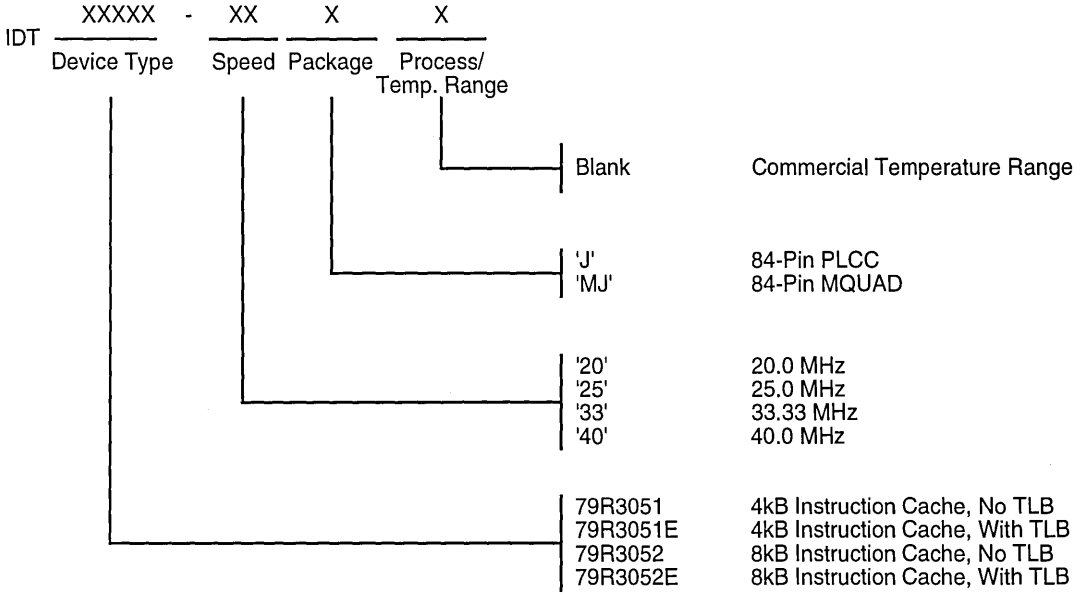
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. MQUAD is pin & form compatible with PLCC.

DWG #	J84-1		MJ84-1	
# of Leads	84		84	
Symbol	Min.	Max.	Min.	Max.
A	165	.180	165	.180
A1	.095	.115	.094	.114
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	1.185	1.195	1.185	1.195
D1	1.150	1.156	1.140	1.150
D2/E2	1.090	1.130	1.090	1.130
D3/E3	1.000 REF		1.000 REF	
E	1.185	1.195	1.185	1.195
E1	1.150	1.156	1.140	1.150
e	.050 BSC		.050 BSC	
ND/NE	21		21	

ORDERING INFORMATION



2874 drw 28

VALID COMBINATIONS

IDT	79R3051 - 20, 25	J Packages Only
	79R3051E - 20, 25	J Packages Only
	79R3052 - 20, 25	J Packages Only
	79R3052E - 20, 25	J Packages Only
	79R3051 - 33, 40	MJ Packages Only
	79R3051E - 33, 40	MJ Packages Only
	79R3052 - 33, 40	MJ Packages Only
	79R3052E - 33, 40	MJ Packages Only

Integrated Device Technology, Inc.

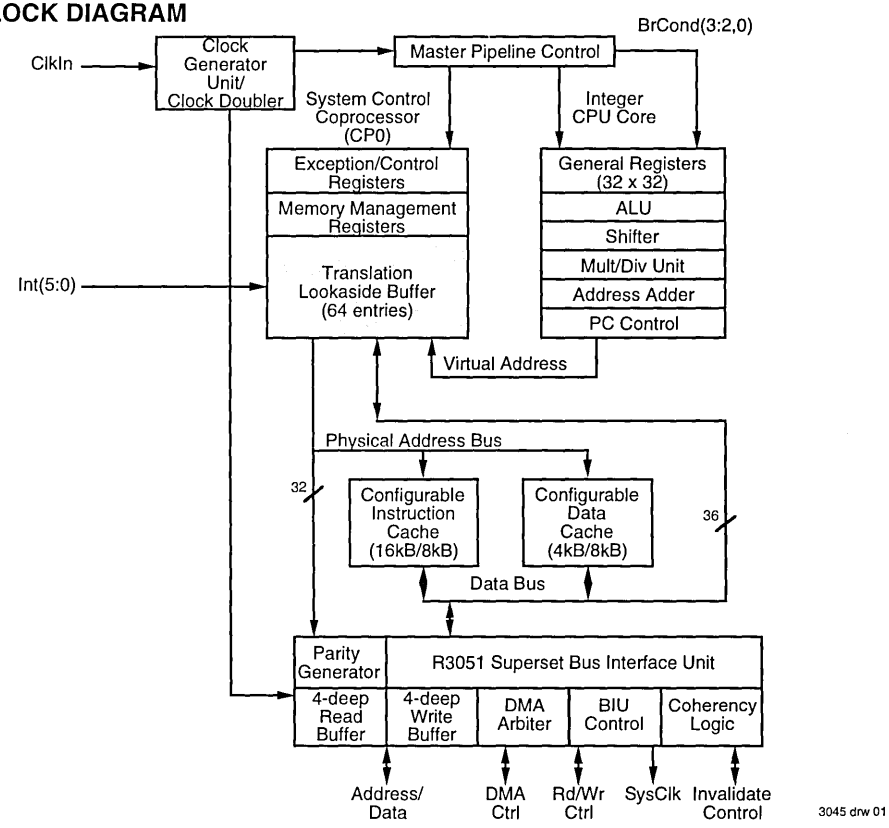
IDT79R3071™ RISController™

IDT79R3071
IDT79R3071E

FEATURES

- Instruction set compatible with IDT79R3000A, R3051™, and R3500 RISC CPUs
- High level of integration minimizes system cost
  - — R3000A Compatible CPU
  - — Optional R3000A compatible MMU
  - — Large Instruction Cache
  - — Large Data Cache
  - — Read/Write Buffers
- 35VUPS at 40MHz
  - — 320MB/sec on-chip bandwidth
  - — 160MB/sec bus bandwidth
- Flexible bus interface allows simple, low-cost designs
- 1x clock input
- 33- through 50MHz operation
- 50MHz at 1x clock input and 1/2 bus frequency
- Superset pin- and software-compatible with R3041™, R3051, R3052™, and R3081™
- Large on-chip caches with user configurability
  - — 16kB Instruction Cache, 4kB Data Cache
  - — Dynamically configurable to 8kB Instruction Cache, 8kB Data Cache
  - — Parity protection over data and tag fields
- Low cost 84-pin packaging
- Multiplexed bus interface with support for low-cost, low-speed memory systems with a high-speed CPU
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-deep read buffer supports burst or simple block reads
- On-chip DMA arbiter
- Hardware-based Cache Coherency Support
- Programmable power reduction mode
- Bus Interface operates only at half-processor frequency

R3071 BLOCK DIAGRAM



INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, which is targeted to high-performance but cost-sensitive processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power-sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 35VUPS performance at 40MHz without requiring external SRAM or caches.

The R3071 extends the capabilities of the R3051 family, by integrating additional resources into the same pin-out. The R3071 thus extends the range of applications addressed by the R3051 family, and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs, according to the price/performance goals of the end system.

An overview of this device, and quantitative electrical parameters and mechanical data, is found in this data sheet; consult the *R3071 Family Hardware User's Guide* for a complete description of this processor.

DEVICE OVERVIEW

As part of the R3051 family, the R3071 extends the offering of a wide range of functionality in a compatible interface. The R3051 family allows the system designer to implement a single base system, and utilize interface-compatible processors of various complexity to achieve the price-performance goals of the particular end system.

Differences among the various family members pertain to the on-chip resources of the processor. Current family members are shown in Table 1, below.

Figure 1 shows a block-level representation of the functional units within the R3071E. The R3071E could be viewed as the embodiment of a discrete solution built around the R3000A and R3010A. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

Device Name	Instruction Cache	Data Cache	MMU Option	FPA	Bus Options
R3041	2kB	512B	No	Software	Programmable Options Variable Port width interface
R3051	4kB	2kB	"E" version	Software	32-bit mux'ed
R3052	8kB	2kB	"E" version	Software	32-bit mux'ed
R3071	16kB	4kB or 8kB	"E" version or 8kB	Software	1/2 frequency bus only
R3081	16kB or 8kB	4kB or 8kB	"E" version	On-chip hardware	1/2 frequency bus

3045 tbl 01

Table 1. R3051 Family Members

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3071 uses the same basic integer execution core as the entire R3051 family, which is the R3000A implementation of the MIPS instruction set. Thus, the R3071 family is binary compatible with the R3051, R3052, R3000A, R3001, and R3500 CPUs. In addition, the R4000 and Orion represent an upwardly software compatible migration path to still higher levels of performance.

The execution engine in the R3071 uses a five-stage pipeline to achieve near single-cycle instruction execution rates. A new instruction can be initiated in each clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved in the R3071 execution pipeline.

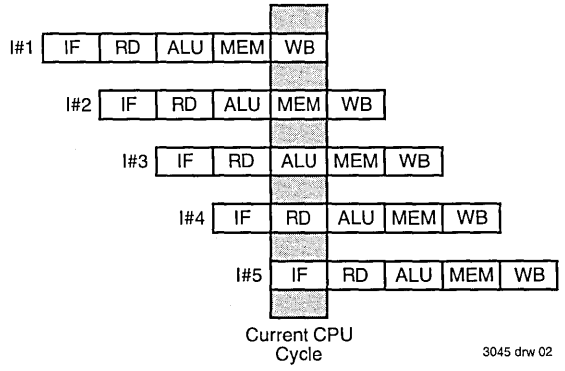


Figure 2. R3071 5-Stage Pipeline

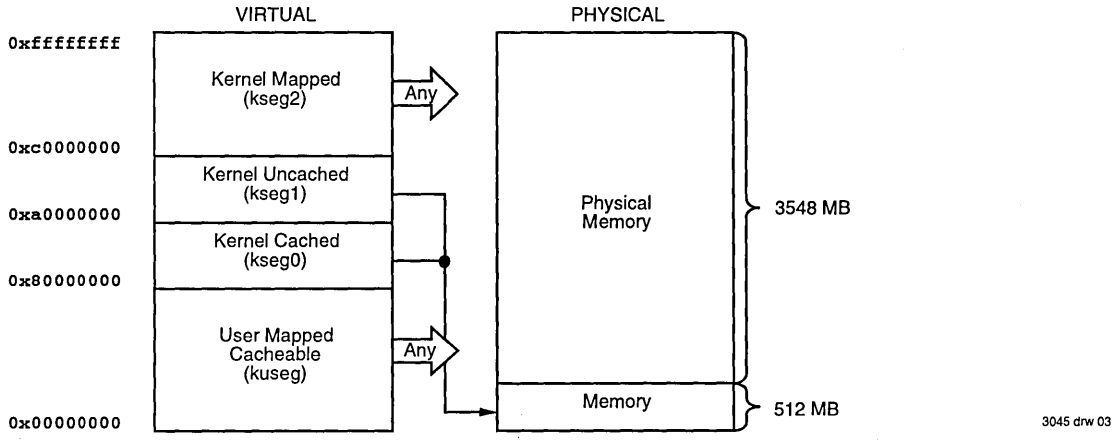


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

System Control Co-Processor

The R3071 family also integrates the System Control Co-processor, CP0, on-chip. CP0 manages both the exception handling capability of the R3071, as well as the virtual-to-physical address mapping.

As with the R3051 and R3052, the R3071 offers two versions of memory management and virtual-to-physical address mapping: the extended architecture versions, the R3051E, R3052E, and R3071E, incorporate the same MMU as the R3000A. These versions contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard-mapped to physical addresses, and kernel and user segments which are mapped page by page by the TLB into anywhere in the 4GB physical address space. In this TLB, 8 pages can be "locked" by the kernel to insure deterministic response in real-time applications. Figure 3 illustrates the virtual to physical mapping found in the R3071E.

The Extended architecture versions of the R3051 family (the R3051E, R3052E, and R3071E) allow the system designer to implement kernel software which dynamically manages User task utilization of system resources, and also allows the Kernel to protect certain resources from User tasks. These capabilities are important in general computing applications such as ARC computers, and are also important in a variety of embedded applications, from process control (where protection may be important) to X-Window display systems (where virtual memory management can be used). The MMU can also be used to simplify system debug.

R3051 family base versions (the R3051, R3052, and R3071) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. These devices still support distinct kernel and user mode operation, but do not require page management software, leading to a simpler software model. The memory mapping used by these devices is shown in Figure 4. Note that the reserved spaces are for compatiblity with future family members, which may map on-

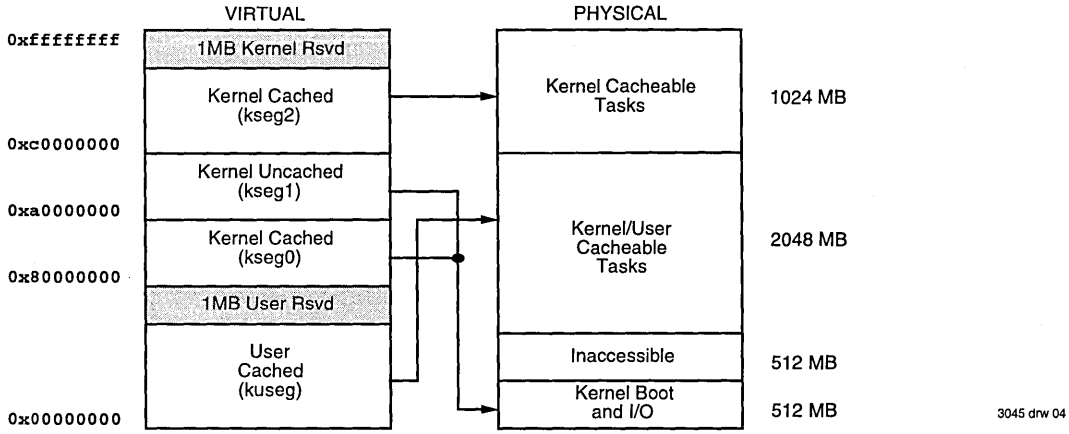


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

chip resources to these addresses. References to these addresses in the R3071 will be translated in the same fashion as the rest of their respective segments, with no traps or exceptions signalled.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to implement page management software. This distinction can be implemented by decoding the output physical address. In systems which do not need memory protection, and wish to have the kernel and user tasks operate out of the same memory space, high-order address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

Clock Generator Unit

The R3071 is driven from a single input clock at the processor rated speed. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The R3071 includes an on-chip clock doubler to provide higher frequency signals to the internal execution core. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3071 implements a 16kB Instruction Cache. The system may choose to repartition the on-chip caches, so that the instruction cache is reduced to 8kB but the data cache is increased to 8kB. The instruction cache is organized with a line size of 16 bytes (four entries). This large cache achieves hit rates in excess of 98% in most applications, and substantially contributes to the performance inherent in the R3071. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

The instruction cache is parity protected over the instruction word and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

Data Cache

The R3071 incorporates an on-chip data cache of 4kB, organized as a line size of 4 bytes (one word). The R3071 allows the system to reconfigure the on-chip cache from the default 16kB I-Cache/4kB D-Cache to 8kB of Instruction and 8kB of Data caches.

The relatively large data cache achieves hit rates in excess of 95% in most applications, and contributes substantially to the performance inherent in the R3071. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write-through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance. Further, support has been provided to allow hardware based data cache coherency in a multi-master environment, such as one utilizing DMA from I/O to memory.

The data cache is parity protected over the data and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

Bus Interface Unit

The R3071 uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slower memory devices. Alternately, a high-performance, low-cost secondary cache can be implemented, allowing the processor to increase performance in systems where bus bandwidth is a performance limitation.

As part of the R3051 family, the R3071 bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3071 also supports hardware based cache coherency during DMA writes. The R3071 can invalidate a specified line of data cache, or in fact can perform burst invalidations during burst DMA writes.

The R3071 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3071 read interface performs both single datum reads and quad word reads. Single reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3071 incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

The R3071 is R3051 superset compatible in its bus interface. Specifically, the R3071 has additional support to simplify the design of very high frequency systems. This support includes the ability to run the bus interface at one-half the processor execution rate, as well as the ability to slow the transitions

between reads and writes to provide extra buffer disable time for the memory interface. However, it is still possible to design a system which, with no modification to the PC Board or software, can accept either an R3051, R3052, or R3071.

SYSTEM USAGE

The IDT R3051 family has been specifically designed to allow a wide variety of memory systems. Low-cost systems can use slow speed memories and simple controllers, while other designers may choose to incorporate higher frequencies, faster memories, and techniques such as DMA to achieve maximum performance. The R3071 includes specific support for high performance systems, including signals necessary to implement external secondary caches, and the ability to perform hardware based cache coherency in multi-master systems.

Figure 5 shows a typical system implementation. Transparent latches are used to de-multiplex the R3071 address and data busses from the A/D bus. The data paths between the memory system elements and the A/D bus is managed by simple octal devices. A small set of simple PALs is used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize a simpler, lower performance memory system to reduce cost and simplify the design. Similarly, the system designer could choose to implement techniques, such as external secondary cache, or DMA, to further improve system performance.

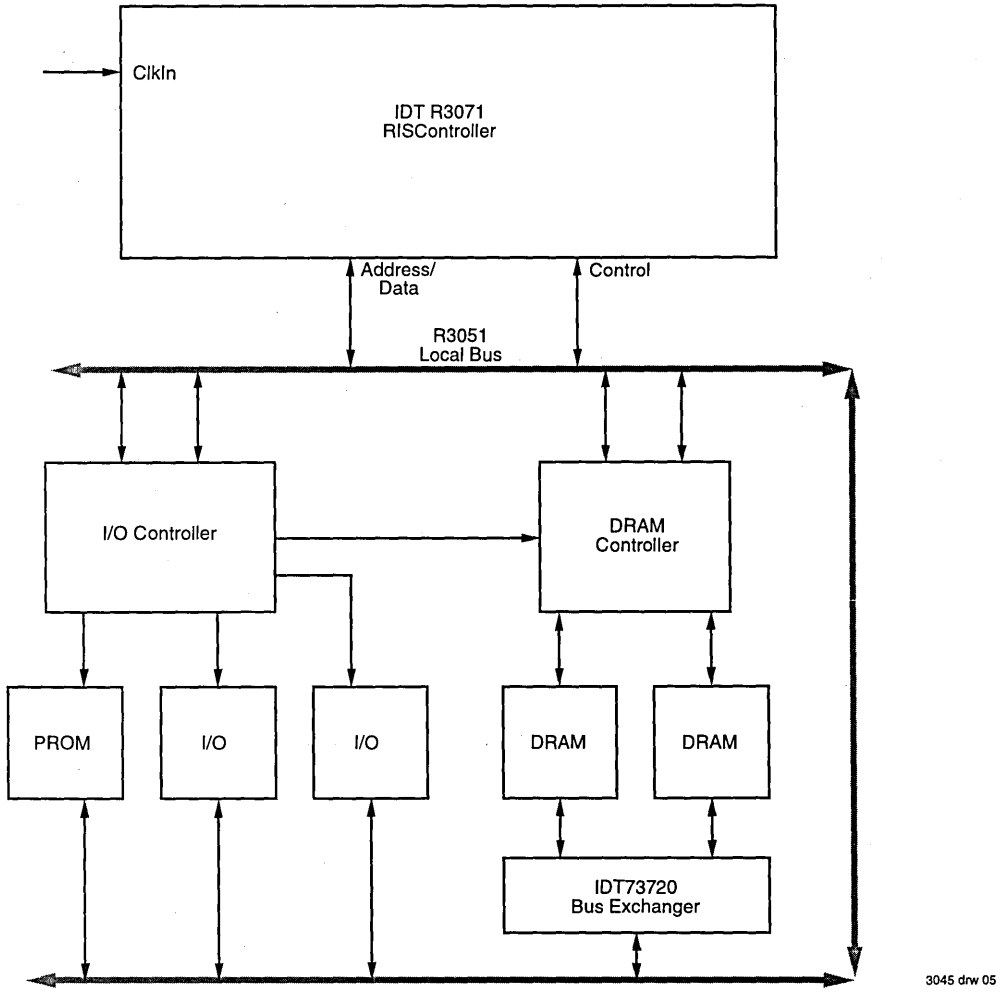


Figure 5. R3071-Based System

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, sub-system modules, and shrink wrap operating systems. The R3071, which is pin and software compatible with the R3051, can directly utilize these existing tools to reduce time to market.

Figure 6 is an overview of the system development process typically used when developing R3051 family applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family applications, and include tools such as:

- A program, Cache-R3051, which allows the performance of an R3051 family system to be modeled and understood without requiring actual hardware.
- Sable, an instruction set simulator.
- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point library software, including transcendental functions and IEEE compliant exception handlers.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- Adobe PostScript™ Page Description Language, ported to the IDT 79S389 Centaurus reference board.
- IDT/sim™, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™, which implements a run-time support package for R3051 family systems.

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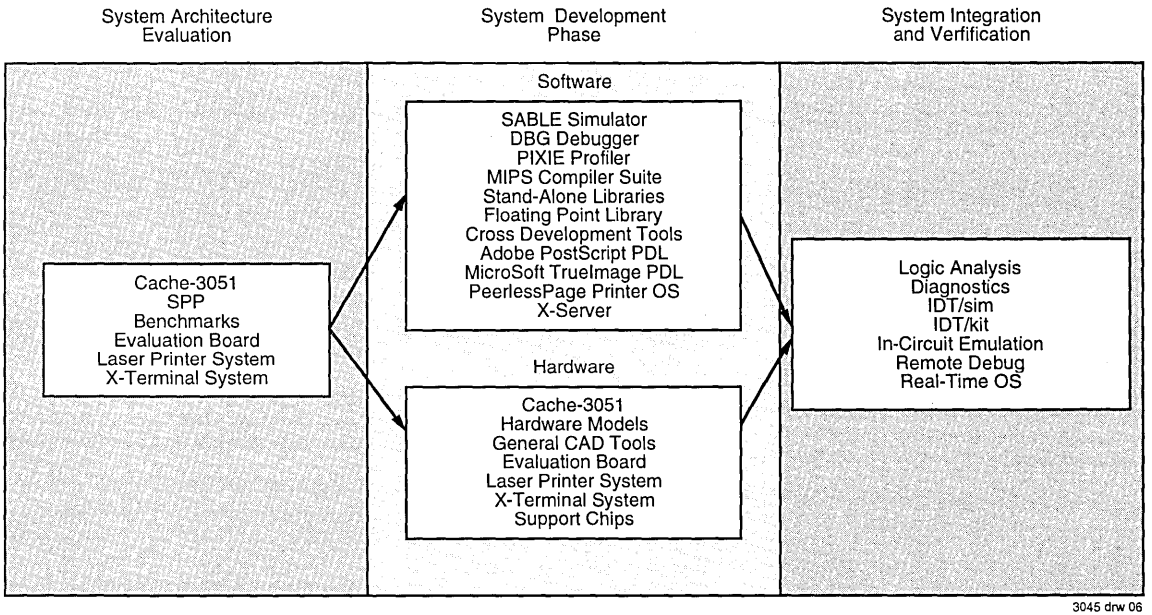

Figure 6. R3051 Family Development Toolchain

PERFORMANCE OVERVIEW

The R3071 achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35VUPS performance when operating out of cache.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of today's microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate. The R3071 doubles the cache available on the R3052.
- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the CPU to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The R3071 features a four-deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve over 35VUPS integer performance and 64,000 dhrystones without the use of external caches or zero wait-state memory devices.

The performance differences between the various family members depends on the application software and the design of the memory system. The impact of the various cache sizes, and the hardware floating point, can be accurately modeled using Cache-3051. Since the R3051, R3052, and R3071 are all pin and software compatible, the system designer has maximum freedom in trading between performance and cost. A system can be designed, and later the appropriate CPU inserted into the board, depending on the desired system performance.

SELECTABLE FEATURES

The R3071 allows the system designer to configure certain aspects of operation. Some of these options are established when the device is reset, while others are enabled via the Config registers:

- **BigEndian vs. LittleEndian Byte Ordering.** The part can be configured to operate with either byte ordering. ACE/ ARC systems typically use Little Endian byte ordering. However, various embedded applications, written originally for a Big Endian processor such as the MC680x0, are easier to port to a Big Endian system.
- **Data Cache Refill of one or four words.** The memory system must be capable of performing four word refills of instruction cache misses. The R3071 allows the system designer to enable D-Cache refill of one or four words dynamically. Thus, specialized algorithms can choose one refill size, while the rest of the system can operate with the other.
- **Half-frequency bus mode.** The processor can be configured such that the external bus interface is at one-half the frequency of the processor core. This simplifies system design; however, the large on-chip caches mitigate the performance impact of using a slower system bus clock.
- **Slow bus turn-around.** The R3071 allows the system designer to space processor operations, so that more time is allowed for transitions between memory and the processor on the multiplexed address/data bus.
- **Configurable cache.** The R3071 allows the system designer to use software to select either a 16kB Instruction Cache/4kB Data Cache organization, or an 8kB Instruction/ 8kB Data Cache organization.
- **Cache Coherent Interface.** The R3071 has an optional hardware based cache coherency interface intended to support multi-master systems such as those utilizing DMA between memory and I/O.

THERMAL CONSIDERATIONS

The R3071 utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, the R3071 is packaged using cavity-down packaging, utilizing techniques to improve thermal transfer to the suurrounding air.

The R3071 utilizes the 84-pin MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package allows for an efficient thermal transfer between the die and the case due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin and form compatible with the PLCC used for the R3051. Thus, designers can inter-change R3071s and R3051s in a particular design, without changing their PC Board.

	ØCA					
Airflow (ft/min)	0	200	400	600	800	1000
"MJ" Package*	22	14	12	11	9	8

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Table 2. Thermal Resistance (ØCA) at Various Airflows (*estimated: final values tbd)

NOTES ON SYSTEM DESIGN

The R3071 has been designed to simplify the task of high-speed system design. Thus,set-up and hold-time requirements have been kept to a minimum,allowing a wide variety of system interface strategies.

To minimize these AC parameters,the R3071 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3071 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3071 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

The R3071 is guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient temperature conditions which will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 2.

Note that the R3071 allows the operational frequency to be turned down during idle periods to reduce power consumption. This operation is described in the *R3071 Hardware User's Guide*. Reducing the operation frequency dramatically reduces power consumption.

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PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). $\overline{BE}$**(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. During cache coherency operations, the R3071 monitors the A/D bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Addr(3:2)	I/O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations. During cache coherency operations, the R3071 monitors the Addr bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether the current read is a result of a cache miss. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. On write cycles, this output signals whether the data being written as retained in the on-chip data cache. The value of this pin is time multiplexed during writes: **Cached:** During the address phase of write transactions, this signal is an active high output which indicates that the store data was retained in the on-chip data cache. **Reserved:** The value of this pin during the data phase of writes is reserved.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/**$\overline{\textbf{D}}$**:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. During write cycles, the value of this pin during both the address and data phases is reserved.

3045 tbl 03

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
ALE	I/O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches. During cache coherency operations, the R3071 monitors ALE at the start of a DMA write, to capture the write target address for potential data cache invalidates.
$\overline{Rd}$	O	**Read:** An output which indicates that the current bus transaction is a read.
$\overline{Wr}$	I/O	**Write:** An output which indicates that the current bus transaction is a write. During coherent DMA, this input indicates that the current transfer is a write.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers
$\overline{Burst}$/ $\overline{WrNear}$	O	**Burst Transfer/Write Near:** On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if quad word refill is currently selected. On write transactions, the $\overline{WrNear}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 512 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{Ack}$	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer. During Coherent DMA, this input indicates that the current write transfer is completed, and that the internal invalidation address counter should be incremented.
$\overline{RdCEn}$	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{SysClk}$	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit. This clock will either be at the same frequency as the CPU execution rate clock, or at one-half that frequency, as selected during reset.
$\overline{BusReq}$	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{IvdReq}$	I	**Invalidate Request.** An input provided by an external DMA controller to request that the CPU invalidate the Data Cache line corresponding to the current DMA write target address. This signal is the same pin as Diag(0)
$\overline{CohReq}$	I	**Coherent DMA Request.** An input used by the external DMA controller to indicate that the requested DMA operations could involve hardware cache coherency. This signal is the Rsvd(0) of the R3051.
SBrCond(3:2) BrCond(0) BrCond(1)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously. Note that BrCond(1) is reserved for use by the R3081 internal FPA, and must be pulled-up externally.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.

3045 tbl 04

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PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{Int}$(5:3) $\overline{SInt}$(2:0)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int}$(5:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts. Note that one interrupt, reserved for use by the R3081 on-chip FPA, will not be monitored externally.
ClkIn	I	**Master Clock Input:** This input clock is provided at the execution frequency of the CPU.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{Reset}$.
Rsvd(4:1)	I/O	**Reserved:** These four signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins. Note that Rsvd(0) of the R3051 is now used for the $\overline{CohReq}$ input pin.

3045 tbl 05

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
VIN	Input Voltage	–0.5 to +7.0	V

3045 tbl 06

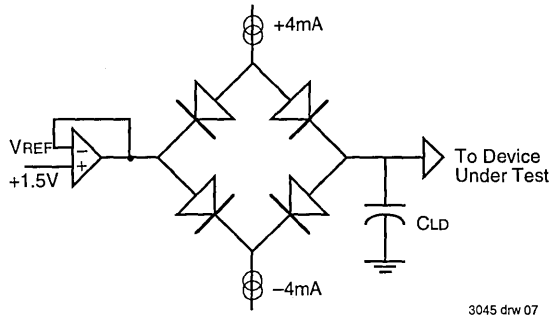
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Commercial	0°C to +85°C	0V (Case)	5.0 ±5%
Commercial	0°C to +85°C	0V (Case)	3.3 ±5%

3045 tbl 07

OUTPUT LOADING FOR AC TESTING



3045 drw 07

Signal	CLD
SysClk	50 pf
All Others	25 pf

3045 tbl 09

AC TEST CONDITIONS—R3071

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0	V

3045 tbl 08

DC ELECTRICAL CHARACTERISTICS R3071— (TC = 0°C to +85°C, VCC = +5.0V ±5%)

			33.33MHz		40MHz		50MHz		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = Min., IOH = –4mA	3.5	—	3.5	—	3.5	—	V
VOL	Output LOW Voltage	VCC = Min., IOL = 4mA	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	V
VILS	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	V
CIN	Input Capacitance(4)	—	—	10	—	10	—	10	pF
COUT	Output Capacitance(4)	—	—	10	—	10	—	10	pF
ICC	Operating Current	VCC = 5V, TC = 25°C	—	625	—	700	—	825	mA
IIH	Input HIGH Leakage	VIH = VCC	—	100	—	100	—	100	µA
IIL	Input LOW Leakage	VIL = GND	–100	—	–100	—	–100	—	µA
IOZ	Output Tri-state Leakage	VOH = 2.4V, VOL = 0.5V	–100	100	–100	100	–100	–100	µA

3045 tbl 10

NOTES:
1. VIL Min. = –3.0V for pulse width less than 15ns. VIL should not fall below –0.5V for larger periods.
2. VIHS and VILS apply to ClkIn and $\overline{\text{Reset}}$.
3. VIH should not be held above VCC + 0.5V.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS R3071 (1, 2)— (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	33.33MHz		40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	4	—	3	—	5	—	ns
t1a	A/D	Set-up to SysClk falling	5	—	4.5	—	6	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	3	—	3	—	4	—	ns
t2a	A/D	Hold from SysClk falling	1	—	1	—	2	—	
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	6	—	5	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	6	—	5	—	7	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	4	—	3.5	—	5	ns
t8	ALE	Asserted from SysClk rising	—	3	—	3	—	4	ns
t9	ALE	Negated from SysClk falling	—	3	—	3	—	4	ns
t10	A/D	Hold from ALE negated	1.5	—	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	13	—	12	—	15	ns
t12	DataEn	Asserted from A/D tri-state(3)	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising(3)	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	5	—	4	—	6	ns
t16	Addr(3:2)	Valid from SysClk	—	5	—	4.5	—	6	ns
t17	Diag	Valid from SysClk	—	10	—	9	—	11	ns
t18	A/D	Tri-state from SysClk falling	—	9	—	8	—	10	ns
t19	A/D	SysClk falling to data out	—	11	—	10	—	12	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	6.5	—	5.6	—	N/A(6)	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	6.5	—	5.6	—	N/A(6)	—	ns
t22	ClkIn (2x clock mode)	Clock Period	15	250	12.5	250	N/A(6, 7)	—	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	4	—	3	—	5	—	ns
t26	Int	Mode set-up to Reset rising	8	—	7	—	9	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	4	—	3	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	2	—	2	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	4	—	3	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	2	—	2	—	3	—	ns

3045 tbl 11

NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. The design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
6. For the 50MHz version, 1x clock mode and half frequncy bus mode only.
7. when using the reduced frequency feature, the minimum allowed internal CPU speed is 0.5MHz.

AC ELECTRICAL CHARACTERISTICS R3071 (continued)[1, 2] — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	33.33MHz		40MHz		50MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
tsys	$\overline{SysClk}$ (full frequency mode)	Pulse Width	2*t22	2*t22	2*t22	2*t22	N/A[7]	N/A[7]	ns
t32	$\overline{SysClk}$ (full frequency mode)	Clock HIGH time[6]	t22-1	t22+1	t22-1	t22+1	N/A[7]	N/A[7]	ns
t33	$\overline{SysClk}$ (full frequency mode)	Clock LOW time[6]	t22-1	t22+1	t22-1	t22+1	N/A[7]	N/A[7]	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[6]	2*t22	2*t22	2*t22	2*t22	2*t44	2*t44	ns
t34	$\overline{SysClk}$ (half frequency mode)	Clock HIGH Time[6]	t22-1	t22+1	t22-1	t22+1	t44-1	t44+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock LOW Time[6]	t22-1	t22+1	t22-1	t22+1	t44-1	t44+1	ns
t36	ALE	Set-up to $\overline{SysClk}$ falling	7	—	6	—	8	—	ns
t37	ALE	Hold from $\overline{SysClk}$ falling	1	—	1	—	2	—	ns
t38	A/D	Set-up to ALE falling	8	—	8	—	9	—	ns
t39	A/D	Hold from ALE falling	1	—	1	—	2	—	ns
t40	$\overline{Wr}$	Set-up to $\overline{SysClk}$ rising	8	—	7	—	6	—	ns
t41	$\overline{Wr}$	Hold from $\overline{SysClk}$ rising	3	—	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[5]	13	—	11[5]	—	16[5]	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[5]	13	—	11[5]	—	16[5]	—	ns
t44	ClkIn (1x clock mode)	Clock Period[5]	30	50	25	50	20	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	—	1	ns/ 25pF

3045 tbl 12

NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. The design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
6. In 1x clock mode, t22 is replaced by t44/2.
7. For the 50MHz version, 1x clock mode and half frequency bus mode only.
8. When using the reduced frequency feature, the minimum allowed internal CPU speed is 0.5MHz.

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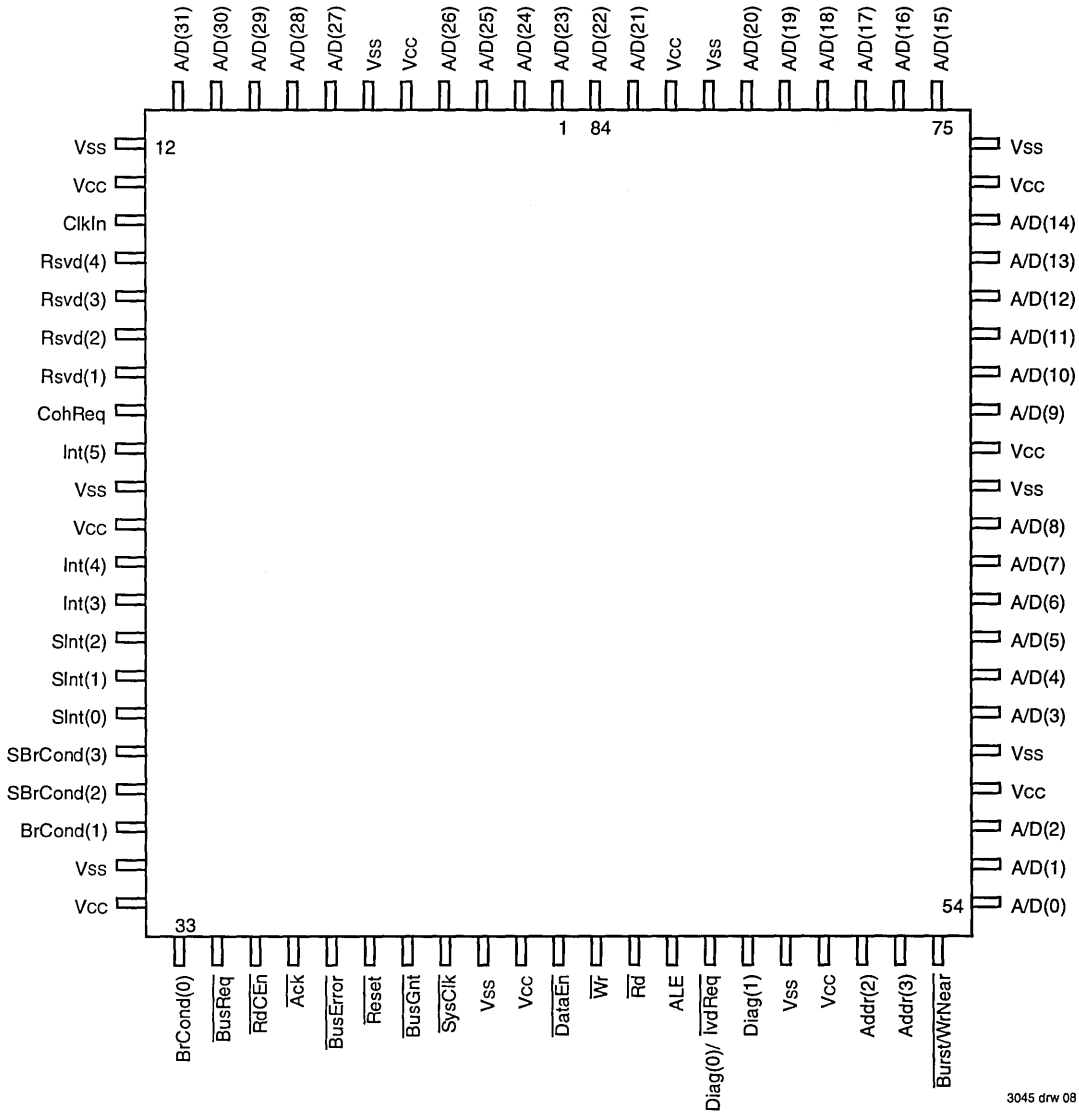
PIN CONFIGURATIONS



84-Pin MQUAD
Top View

NOTE:
1. Reserved Pins must not be connected.
2. BrCond(1) is reserved in the R3071, and must be pulled-up externally.

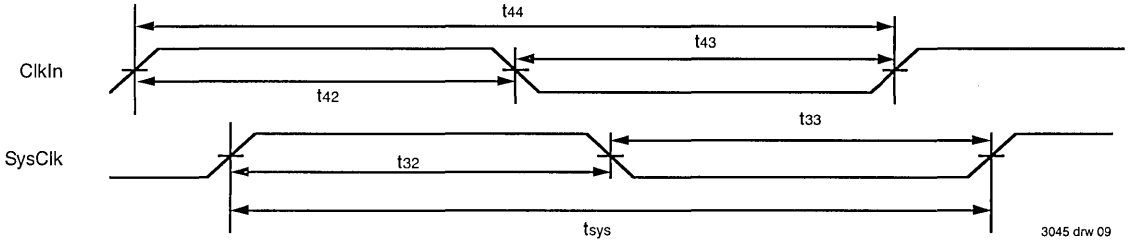


Figure 7 (a). R3071 Clocking (1x clock input mode, full frequency bus)

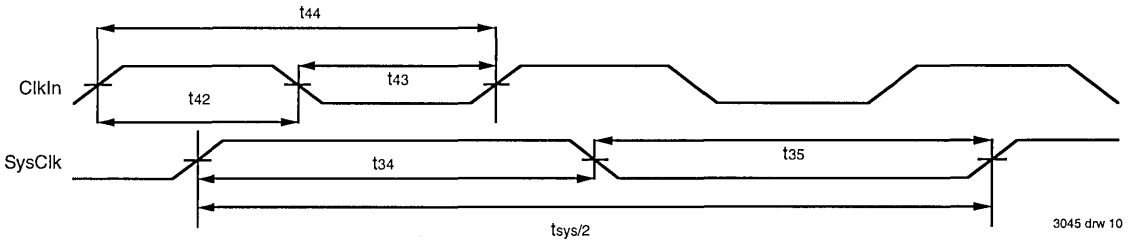


Figure 7 (b). R3071Clocking (1x clock input mode, half-frequency bus)

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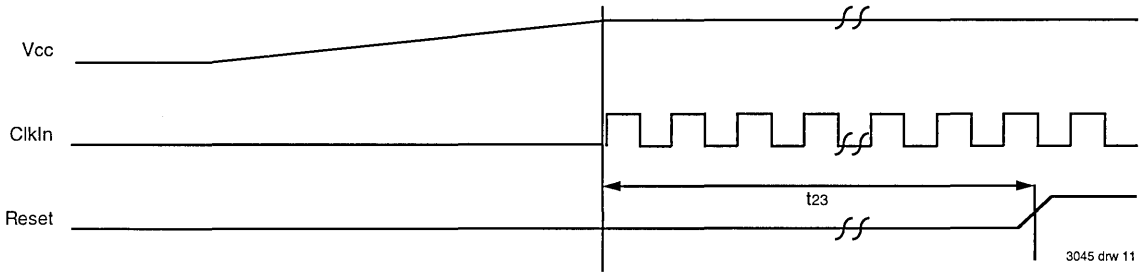


Figure 8. Power-On Reset Sequence

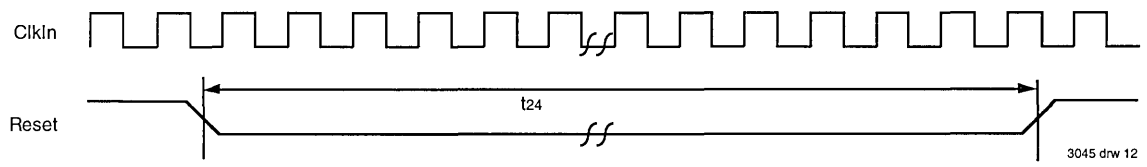


Figure 9. Warm Reset Sequence

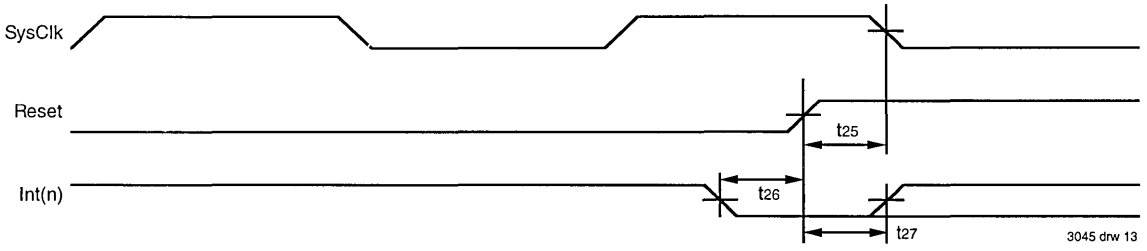


Figure 10. Mode Selection and Negation of Reset

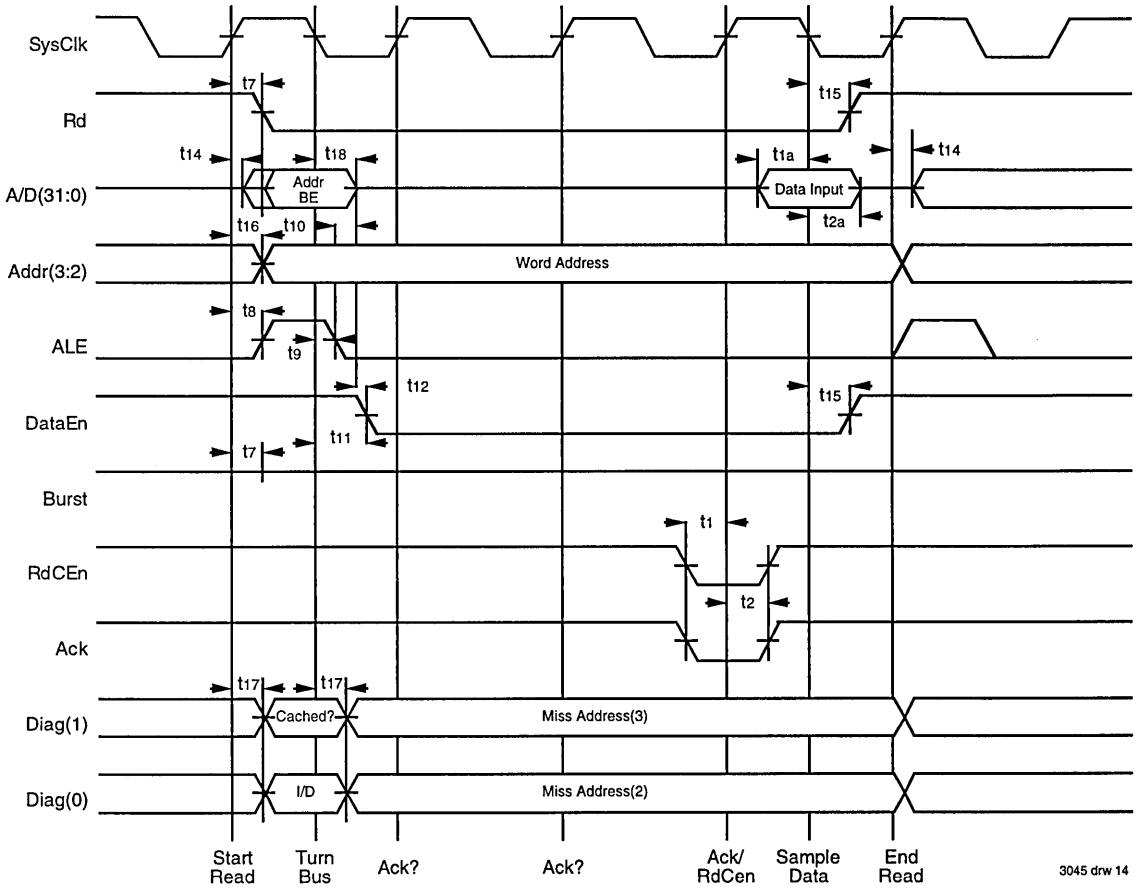


Figure 11. Single Datum Read in R3071

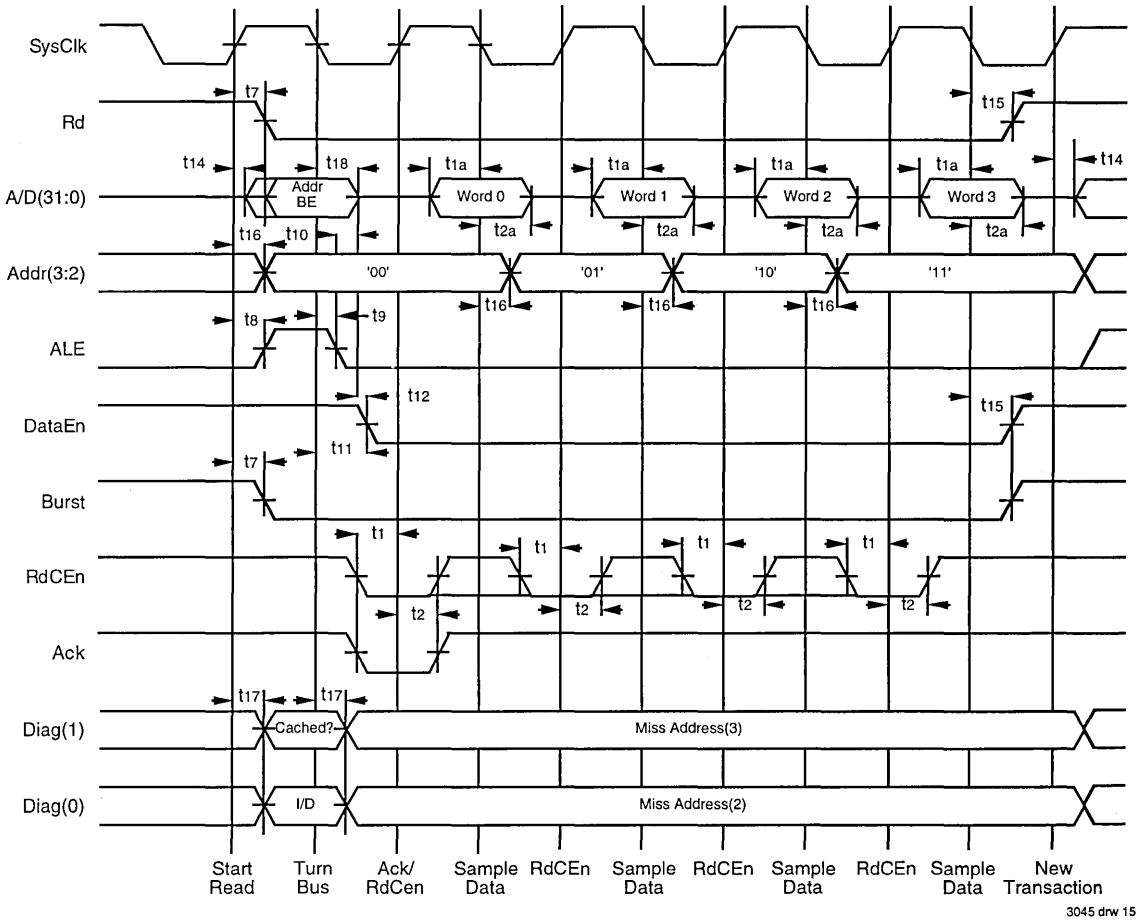


Figure 12. R3071 Burst Read

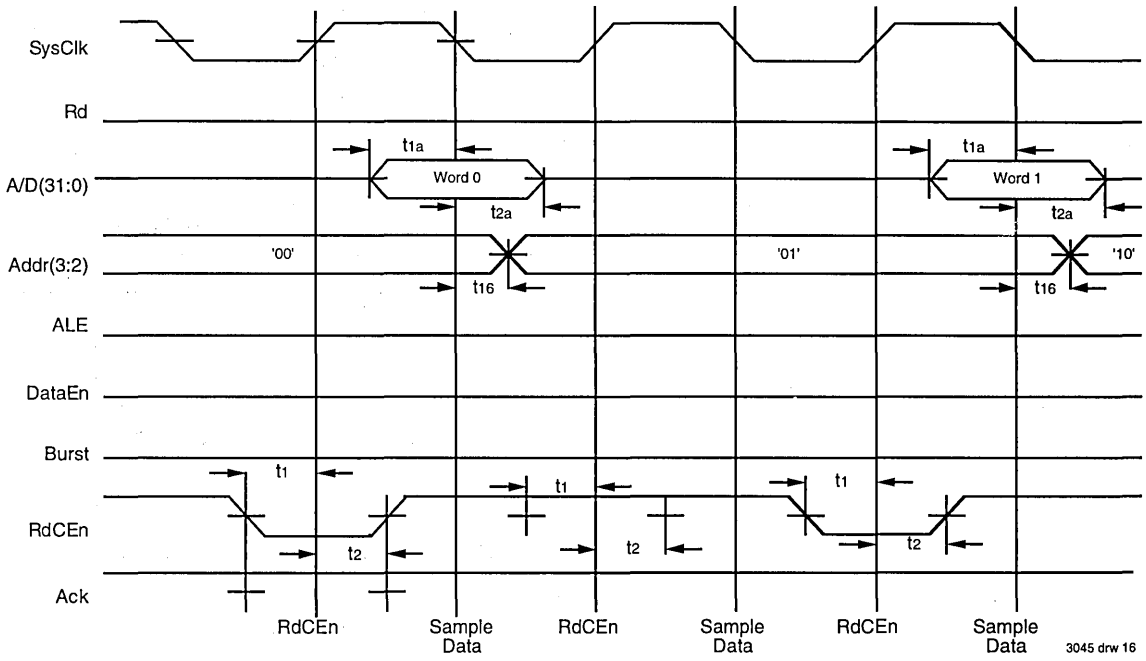


Figure 13 (a). Start of Throttled Quad Read

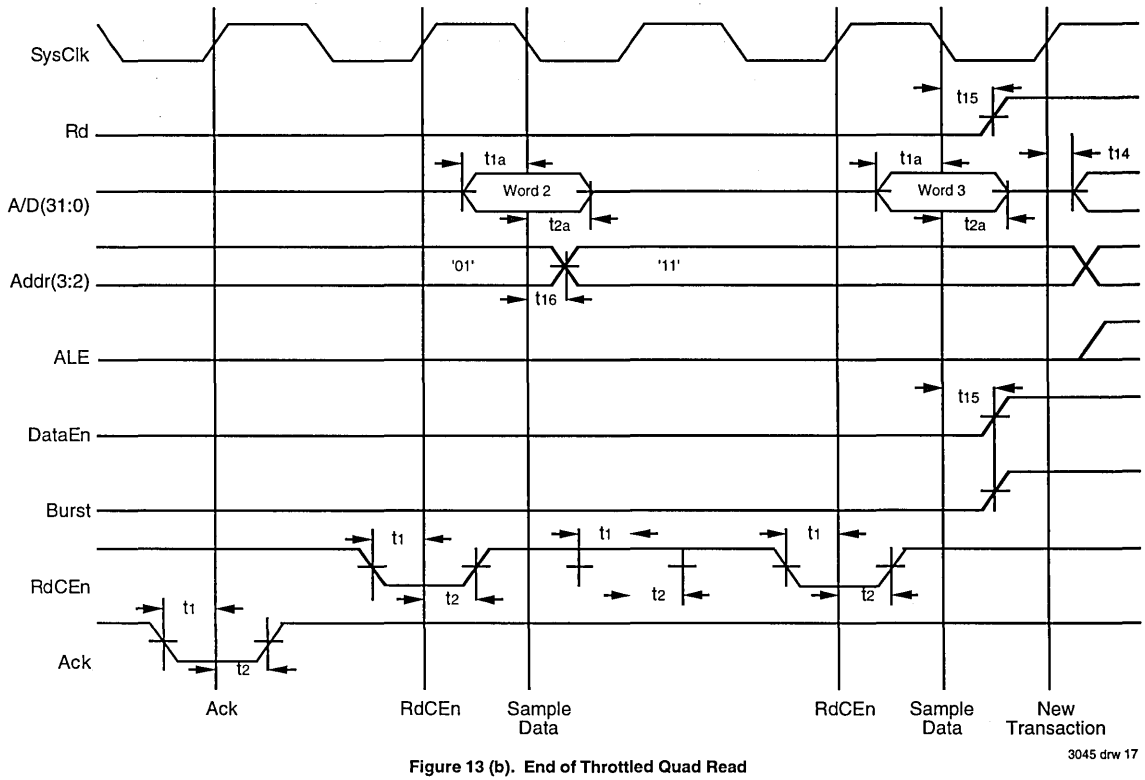


Figure 13 (b). End of Throttled Quad Read

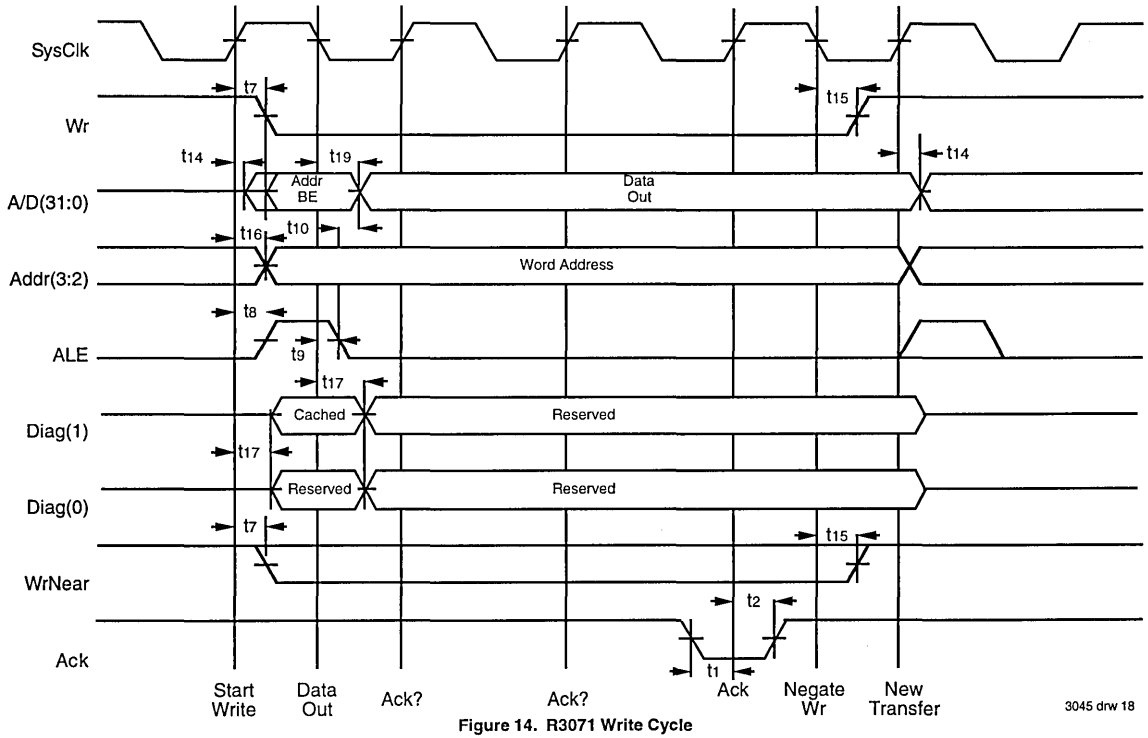


Figure 14. R3071 Write Cycle

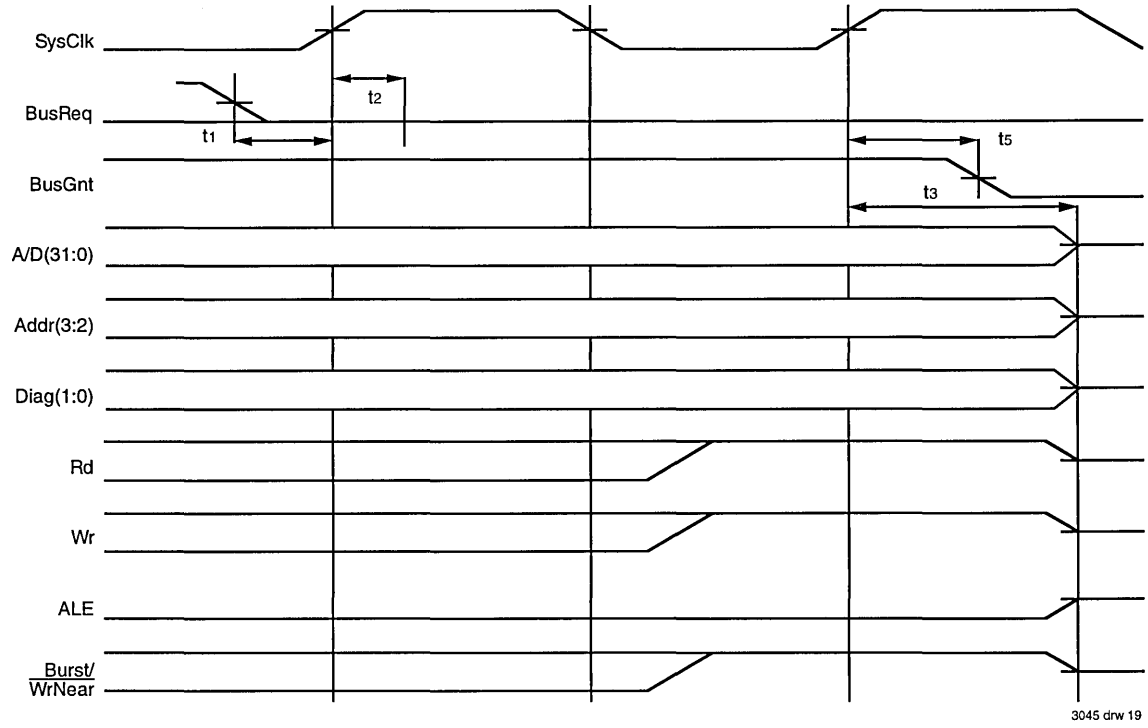


Figure 15. Request and Relinquish of R3071 Bus to External Master

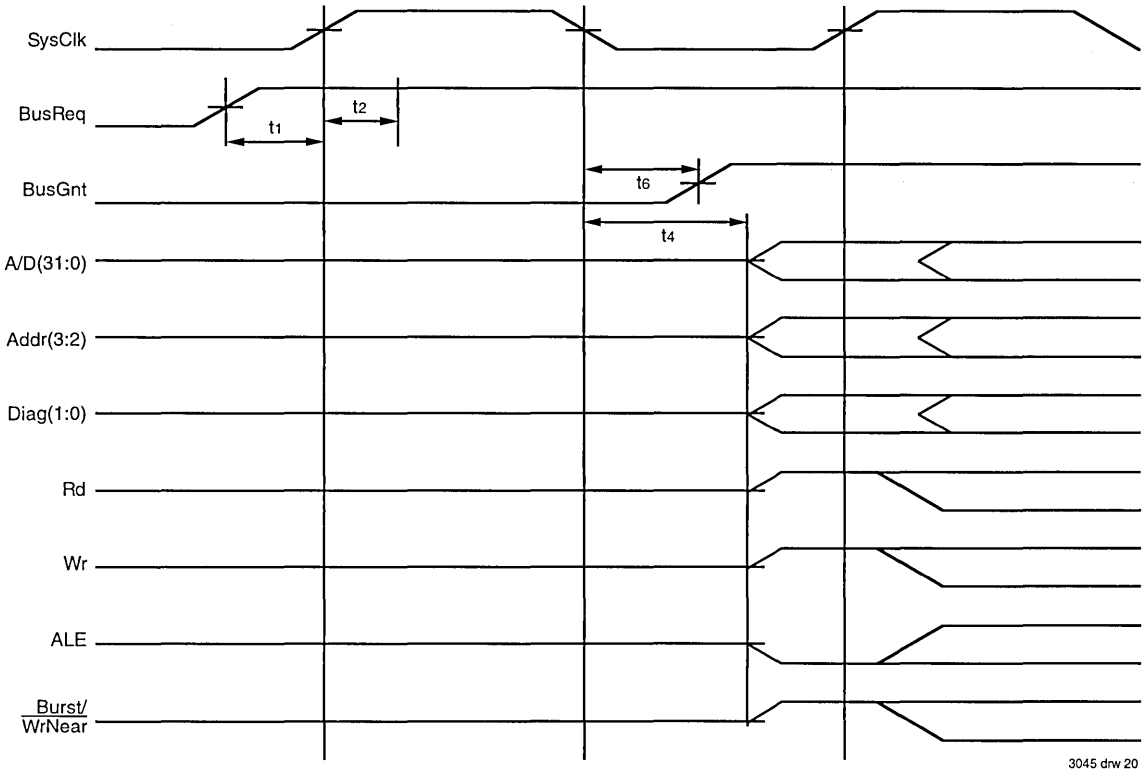


Figure 16. R3071 Regaining Bus Mastership

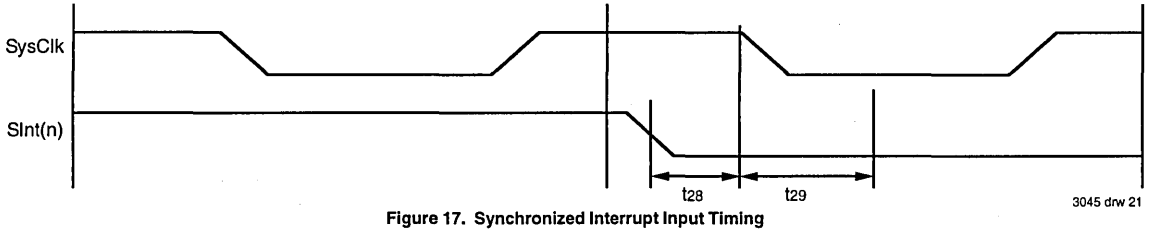


Figure 17. Synchronized Interrupt Input Timing

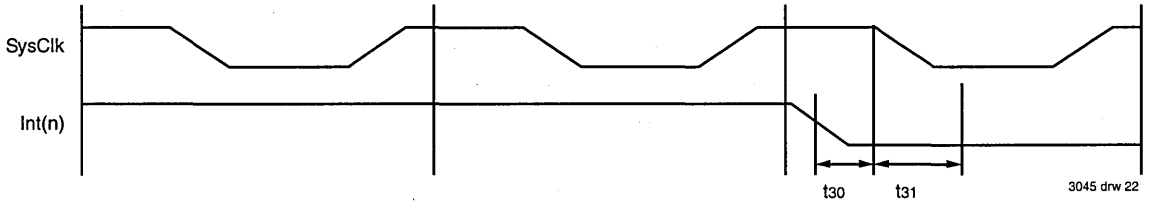


Figure 18. Direct Interrupt Input Timing

5

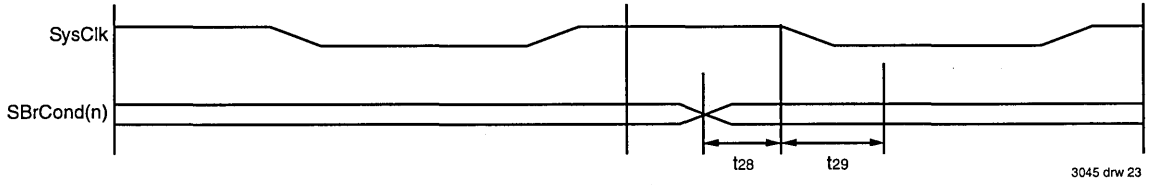


Figure 19. Synchronized Branch Condition Input Timing

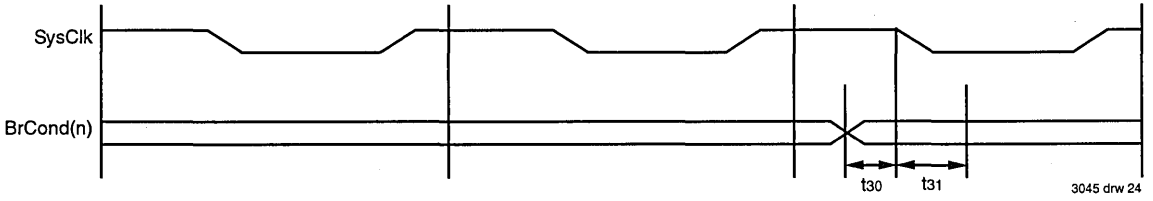


Figure 20. Direct Branch Condition Input Timing

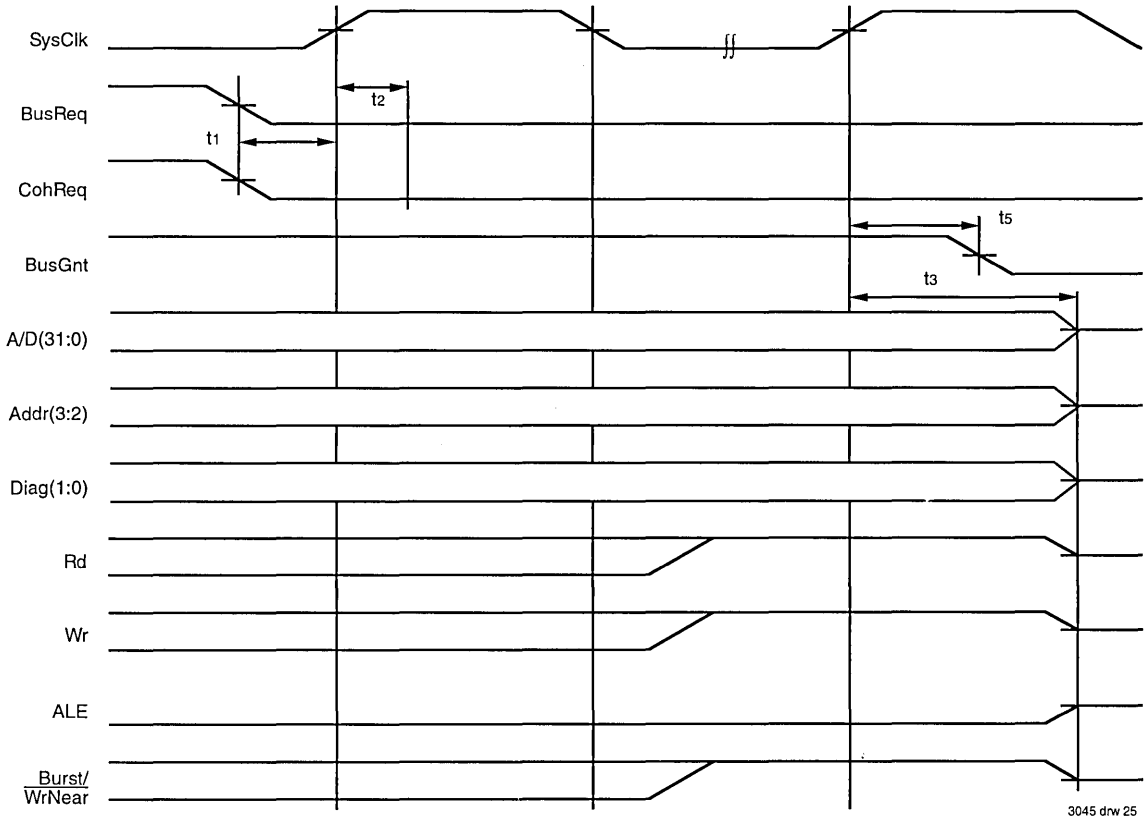


Figure 21. Coherent DMA Request

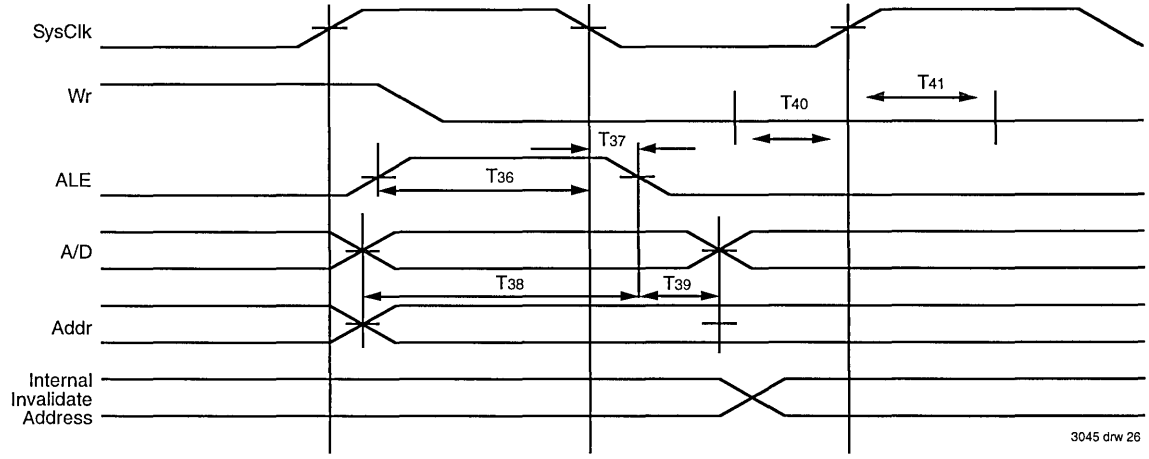


Figure 22. Beginning of Coherent DMA Write

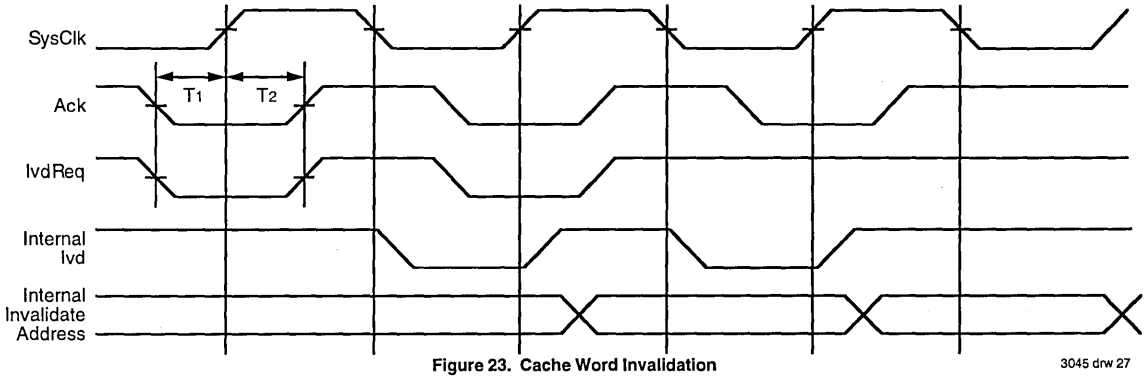


Figure 23. Cache Word Invalidation

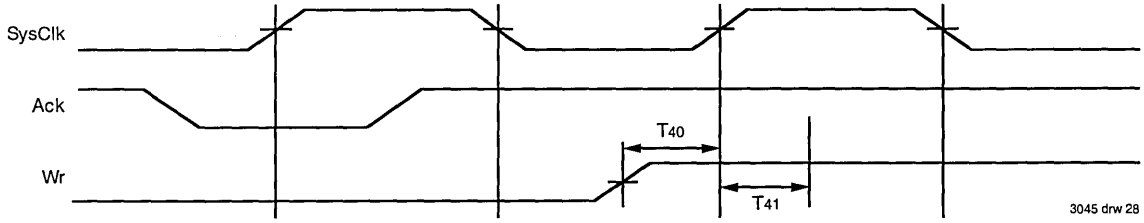


Figure 24. End of Coherent Write

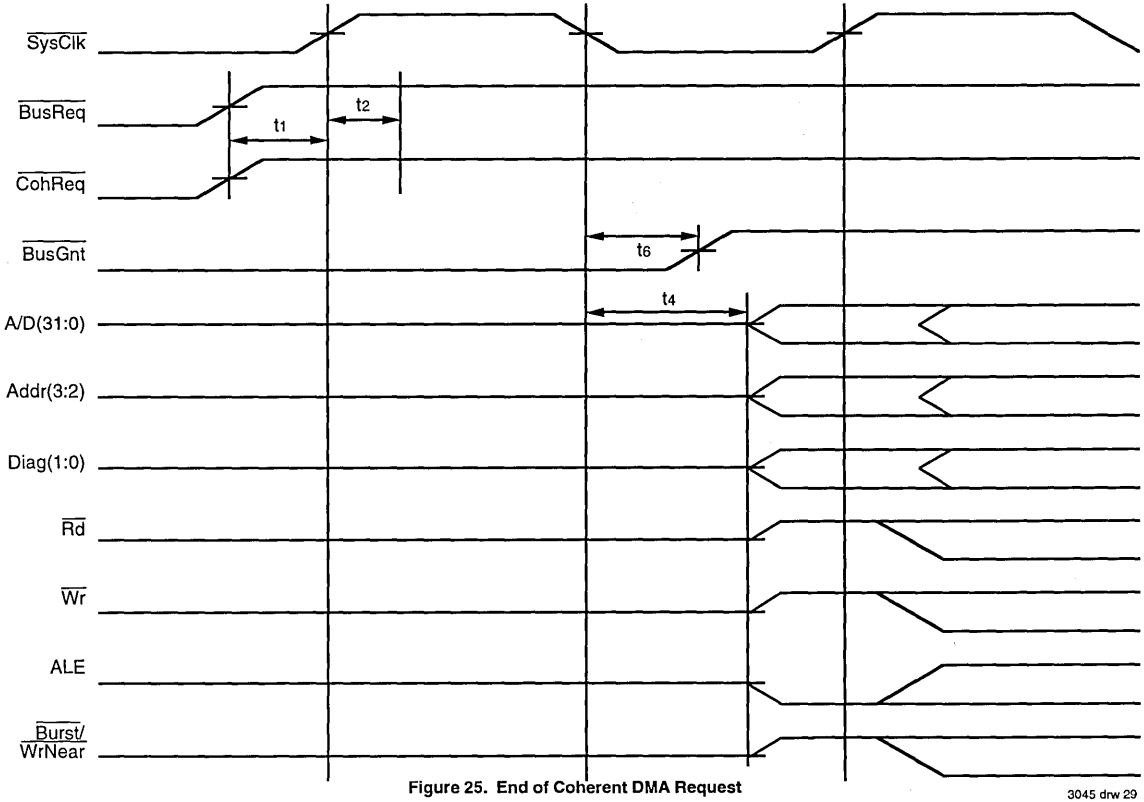
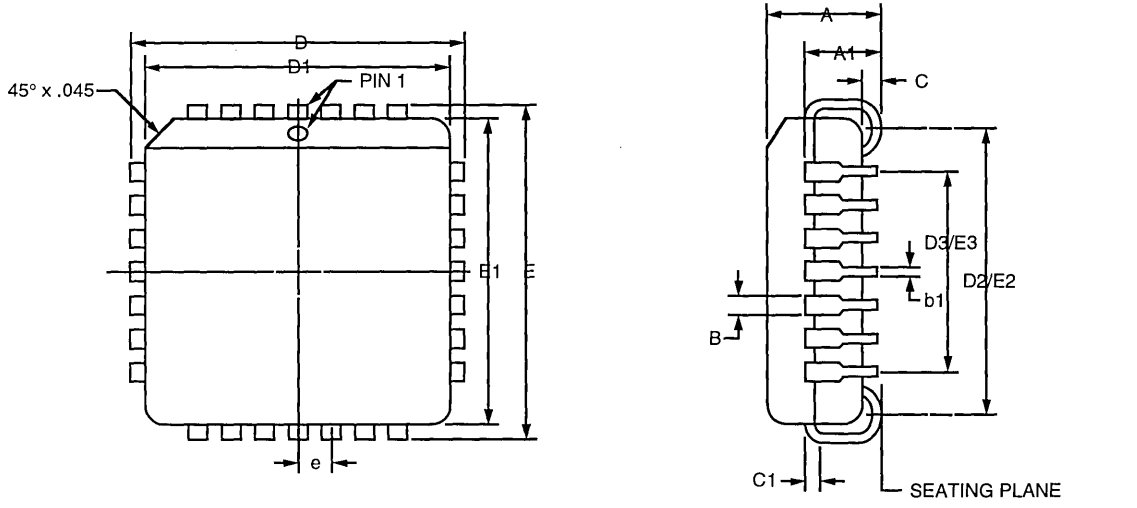


Figure 25. End of Coherent DMA Request

84 LEAD MQUAD[7]



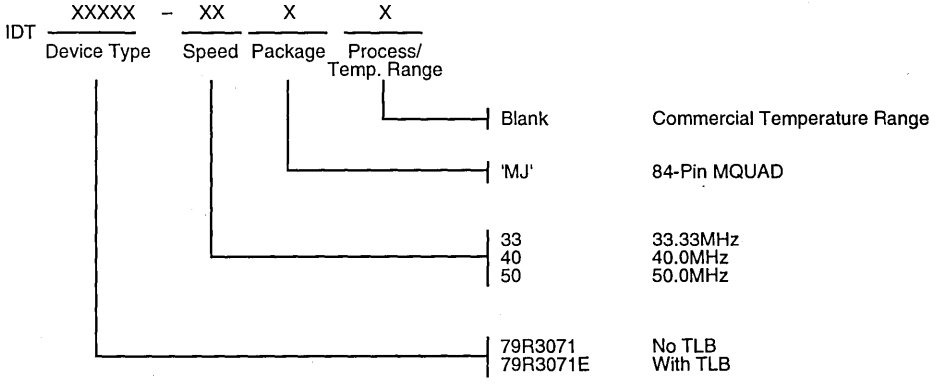
3045 drw 30

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. 84-pin MQUAD is pin & form compatible with 84-pin PLCC of R3051/2

DWG #	MJ84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.094	.114
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.140	1.150
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.140	1.150
e	.050 BSC	
ND/NE	21	

3045 tbl 13

ORDERING INFORMATION



3045 drw 31

VALID COMBINATIONS

IDT	79R3071 – 33, 40, 50 MJ	MQUAD Package
	79R3071E – 33, 40, 50 MJ	MQUAD Package

5

Integrated Device Technology, Inc.

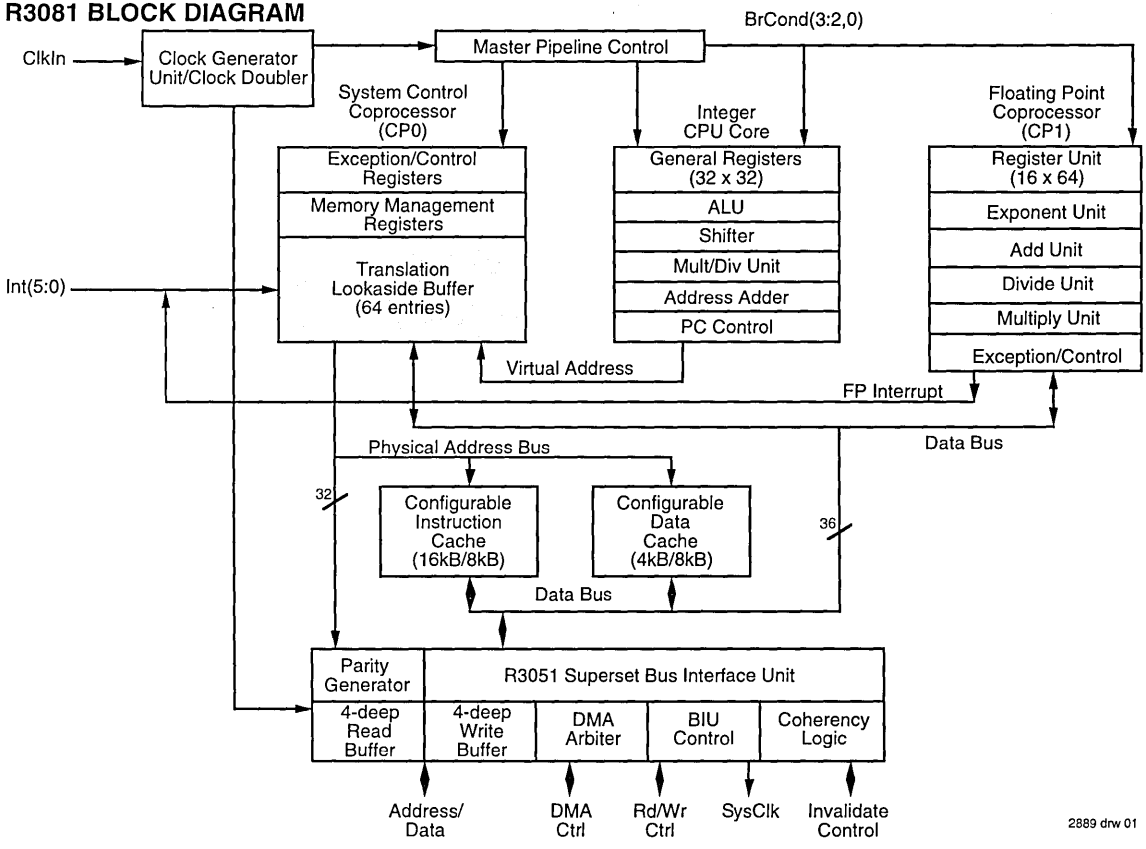
IDT79R3081 RISController™ with FPA

IDT 79R3081™, 79R3081E
IDT 79RV3081, 79RV3081E

FEATURES

- Instruction set compatible with IDT79R3000A, R3041, R3051, and R3071 RISC CPUs
- High level of integration minimizes system cost
  - — R3000A Compatible CPU
  - — R3010A Compatible Floating Point Accelerator
  - — Optional R3000A compatible MMU
  - — Large Instruction Cache
  - — Large Data Cache
  - — Read/Write Buffers
- 43VUPS at 50MHz
  - — 13MFlops
- Flexible bus interface allows simple, low cost designs
- Optional 1x or 2x clock input
- 20 through 50MHz operation
- "V" version operates at 3.3V
- 50MHz at 1x clock input and 1/2 bus frequency only
- Large on-chip caches with user configurability
  - — 16kB Instruction Cache, 4kB Data Cache
  - — Dynamically configurable to 8kB Instruction Cache, 8kB Data Cache
  - — Parity protection over data and tag fields
- Low cost 84-pin packaging
- Superset pin- and software-compatible with R3051, R3071
- Multiplexed bus interface with support for low-cost, low-speed memory systems with a high-speed CPU
- On-chip 4-deep write buffer eliminates memory write stalls
- On-chip 4-deep read buffer supports burst or simple block reads
- On-chip DMA arbiter
- Hardware-based Cache Coherency Support
- Programmable power reduction mode
- Bus Interface can operate at half-processor frequency

R3081 BLOCK DIAGRAM



2889 drw 01

INTRODUCTION

The IDT R3051 family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive processing applications. The R3051 family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the R3051 family is able to offer 43VUPS performance at 50MHz without requiring external SRAM or caches.

The R3081 extends the capabilities of the R3051 family, by integrating additional resources into the same pin-out. The R3081 thus extends the range of applications addressed by the R3051 family, and allows designers to implement a single, base system and software set capable of accepting a wide variety of CPUs, according to the price/performance goals of the end system.

In addition to the embedded applications served by the R3051 family, the R3081 allows low-cost, entry level computer systems to be constructed. These systems will offer many times the performance of traditional PC systems, yet cost approximately the same. The R3081 is able to run any standard R3000A operation system, including ACE UNIX. Thus, the R3081 can be used to build a low-cost ARC compliant system, further widening the range of performance solutions of the ACE Initiative.

An overview of this device, and quantitative electrical parameters and mechanical data, is found in this data sheet; consult the *"R3081 Family Hardware User's Guide"* for a complete description of this processor.

DEVICE OVERVIEW

As part of the R3051 family, the R3081 extends the offering of a wide range of functionality in a compatible interface. The R3051 family allows the system designer to implement a single base system, and utilize interface-compatible processors of various complexity to achieve the price-performance goals of the particular end system.

Differences among the various family members pertain to the on-chip resources of the processor. Current family members include:

- The R3052E, which incorporates an 8kB instruction cache, a 2kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB).
- The R3052, which also incorporates an 8kB instruction cache and 2kB data cache, but does not include the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3051E, which incorporates 4kB of instruction cache and 2kB of data cache, along with the full function MMU/TLB of the R3000A.
- The R3051, which incorporates 4kB of instruction cache and 2kB of data cache, but omits the TLB, and instead uses a simpler virtual to physical address mapping.
- The R3081E, which incorporates a 16kB instruction cache, a 4kB data cache, and full function memory management unit (MMU) including 64-entry fully associative Translation Lookaside Buffer (TLB). The cache on the R3081E is user configurable to an 8kB Instruction Cache and 8kB Data Cache.
- The R3081, which incorporates a 16kB instruction cache, a 4kB data cache, but uses the simpler memory mapping of the R3051/52, and thus omits the TLB. The cache on the R3081 is user configurable to an 8kB Instruction Cache and 8kB Data Cache.

Figure 1 shows a block level representation of the functional units within the R3081E. The R3081E could be viewed as the embodiment of a discrete solution built around the R3000A and R3010A. However, by integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to single cycle execution. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The R3081 uses the same basic integer execution core as the entire R3051 family, which is the R3000A implementation of the MIPS instruction set. Thus, the R3081 family is binary compatible with the R3051, R3052, R3000A, R3001, and R3500 CPUs. In addition, the R4000 represents an upwardly software compatible migration path to still higher levels of performance.

The execution engine in the R3081 uses a five-stage pipeline to achieve near single-cycle instruction execution rates. A new instruction can be initiated in each clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). Figure 2 shows the concurrency achieved in the R3081 execution pipeline.

System Control Co-Processor

The R3081 family also integrates on-chip the System Control Co-processor, CP0. CP0 manages both the exception handling capability of the R3081, as well as the virtual to physical address mapping.

As with the R3051 and R3052, the R3081 offers two versions of memory management and virtual to physical address mapping: the extended architecture versions, the R3051E, R3052E, and R3081E, incorporate the same MMU as the R3000A. These versions contain a fully associative 64-entry TLB which maps 4kB virtual pages into the physical address space. The virtual to physical mapping thus includes kernel segments which are hard-mapped to physical addresses, and kernel and user segments which are mapped page by page by the TLB into anywhere in the 4GB physical address space. In this TLB, 8 pages can be "locked" by the kernel to insure deterministic response in real-time applications. Figure 3 illustrates the virtual to physical mapping found in the R3081E.

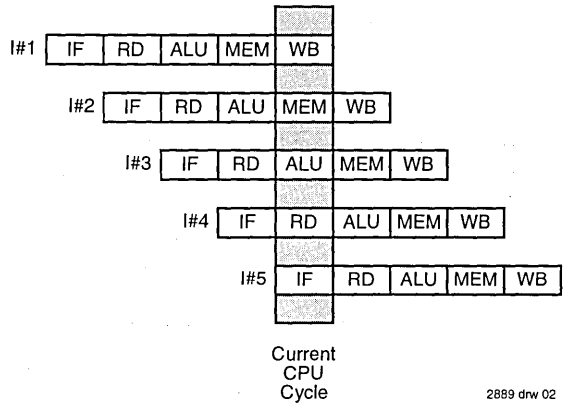


Figure 2. R3081 5-Stage Pipeline

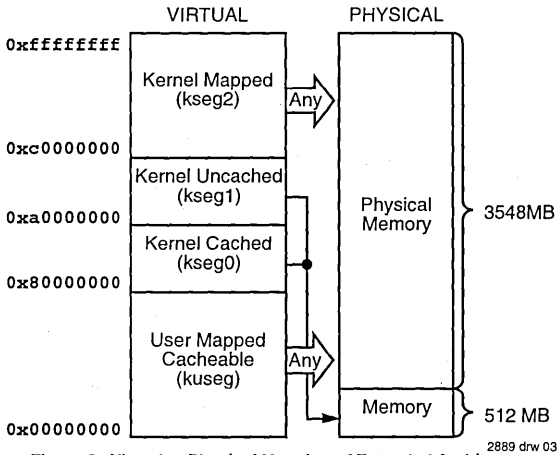


Figure 3. Virtual to Physical Mapping of Extended Architecture Versions

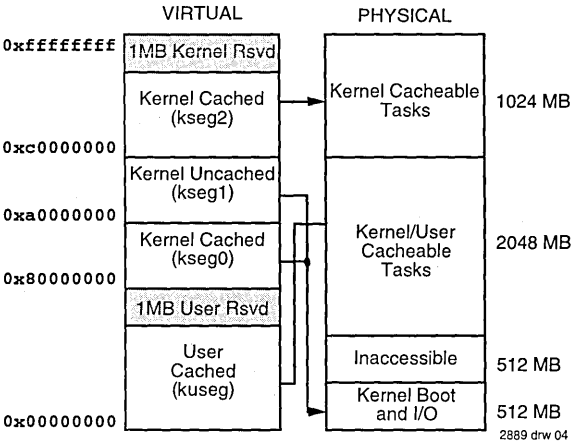


Figure 4. Virtual to Physical Mapping of Base Architecture Versions

The extended architecture versions of the R3051 family (the R3051E, R3052E, and R3081E) allow the system designer to implement kernel software which dynamically manages user task utilization of system resources, and also allows the Kernel to protect certain resources from user tasks. These capabilities are important in general computing applications such as ARC computers, and are also important in a variety of embedded applications, from process control (where protection may be important) to X-Window display systems (where virtual memory management can be used). The MMU can also be used to simplify system debug.

R3051 family base versions (the R3051, R3052, and R3081) remove the TLB and institute a fixed address mapping for the various segments of the virtual address space. These devices still support distinct kernel and user mode operation, but do not require page management software, leading to a simpler software model. The memory mapping used by these devices is shown in Figure 4. Note that the reserved spaces are for compatiblity with future family members, which may map on-chip resources to these addresses. References to these addresses in the R3081 will be translated in the same fashion as the rest of their respective segments, with no traps or exceptions signalled.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to implement page management software. This distinction can be implemented by decoding the output physical address. In systems which do not need memory protection, and wish to have the kernel and user tasks operate out of the same memory space, high-order address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

Floating Point Co-Processor

The R3081 also integrates an R3010A compatible floating point accelerator on-chip. The FPA is a high-performance co-processor (co-processor 1 to the CPU) providing separate add, multiply, and divide functional units for single and double precision floating point arithmetic. The floating point accelerator features low latency operations, and autonomous functional units which allow differing types of floating point operations to function concurrently with integer operations. The R3010A appears to the software programmer as a simple extension of the integer execution unit, with 16 dedicated 64-bit floating point registers (software references these as 32 32-bit registers when performing loads or stores). Figure 5 illustrates the functional block diagram of the on-chip FPA.

Clock Generator Unit

The R3081 is driven from a single input clock which can be either at the processor rated speed, or at twice that speed. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The R3081 includes an on-chip clock doubler to provide higher frequency signals to the internal execution core; if 1x clock mode is selected, the clock doubler will internally convert it to

a double frequency clock. The 2x clock mode is provided for compatiblity with the R3051. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3081 implements a 16kB Instruction Cache. The system may choose to repartition the on-chip caches, so that the instruction cache is reduced to 8kB but the data cache is increased to 8kB. The instruction cache is organized with a line size of 16bytes (four entries). This large cache achieves hit rates in excess of 98% in most applications, and substantially contributes to the performance inherent in the R3081. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses (rather than virtual addresses), and thus does not require flushing on context switch.

The instruction cache is parity protected over the instruction word and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

Data Cache

The R3081 incorporates an on-chip data cache of 4kB, organized as a line size of 4 bytes (one word). The R3081 allows the system to reconfigure the on-chip cache from the default 16kB I-Cache/4kB D-Cache to 8kB of Instruction and 8kB of Data caches.

The relatively large data cache achieves hit rates in excess of 95% in most applications, and contributes substantially to the performance inherent in the R3081. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write-through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance. Further, support has been provided to allow hardware based data cache coherency in a multi-master environment, such as one utilizing DMA from I/O to memory.

The data cache is parity protected over the data and tag fields. Parity is generated by the read buffer during cache refill; during cache references, the parity is checked, and in the case of a parity error, a cache miss is processed.

Bus Interface Unit

The R3081 uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slower memory devices. Alternately, a high-performance, low-cost secondary cache can be implemented, allowing the processor to increase performance in systems where bus bandwidth is a performance limitation.

As part of the R3051 family, the R3081 bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and

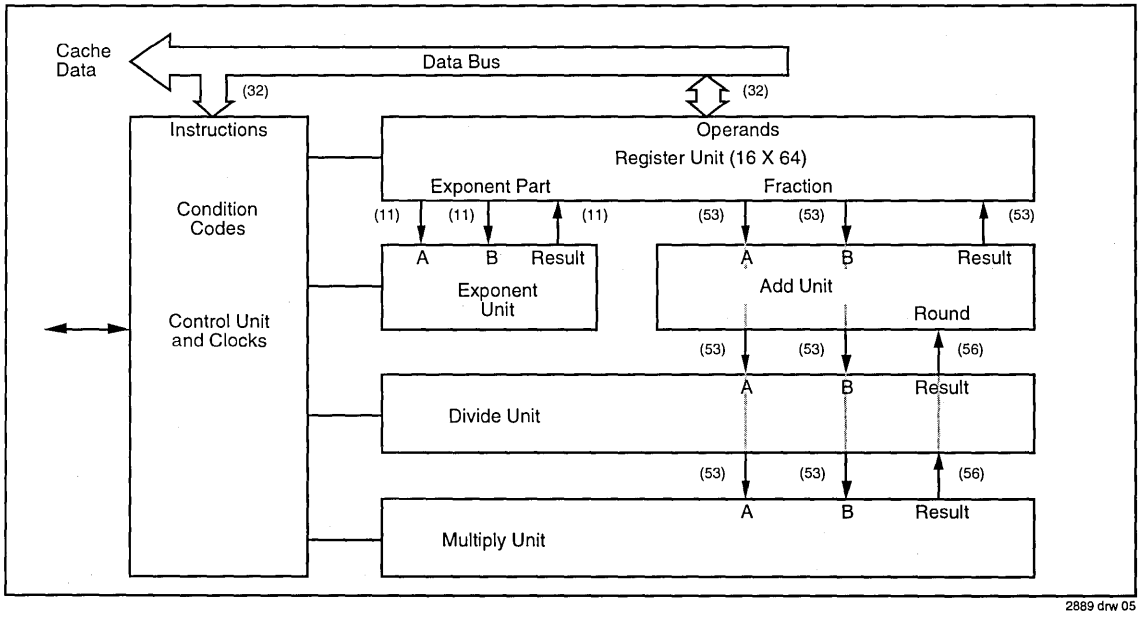


Figure 5. FPA Functional Block Diagram

simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3051 family incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3081 also supports hardware based cache coherency during DMA writes. The R3081 can invalidate a specified line of data cache, or in fact can perform burst invalidations during burst DMA writes.

The R3081 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate.

The R3081 read interface performs both single datum reads and quad word reads. Single reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to utilize page or nibble mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or use simpler techniques to reduce complexity.

In order to accommodate slower quad word reads, the R3081 incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

The R3081 is R3051 superset compatible in its bus interface. Specifically, the R3081 has additional support to simplify the design of very high frequency systems. This support includes the ability to run the bus interface at one-half the processor execution rate, as well as the ability to slow the transitions between reads and writes to provide extra buffer disable time for the memory interface. However, it is still possible to design a system which, with no modification to the PC Board or software, can accept either an R3041, R3051, R3052, R3071, or R3081.

SYSTEM USAGE

The IDT R3051 family has been specifically designed to allow a wide variety of memory systems. Low-cost systems can use slow speed memories and simple controllers, while other designers may choose to incorporate higher frequencies, faster memories, and techniques such as DMA to achieve maximum performance. The R3081 includes specific support for high perfromance systems, including signals necessary to implement external secondary caches, and the ability to perform hardware based cache coherency in multi-master systems.

Figure 6 shows a typical system implementation. Transparent latches are used to de-multiplex the R3081 address and data busses from the A/D bus. The data paths between the memory system elements and the A/D bus is managed by simple octal devices. A small set of simple PALs is used to control the various data path elements, and to control the handshake between the memory devices and the CPU.

Depending on the cost vs. performance tradeoffs appropriate to a given application, the system design engineer could include true burst support from the DRAM to provide for high-performance cache miss processing, or utilize a simpler, lower performance memory system to reduce cost and simplify the design. Similarly, the system designer could choose to implement techniques such as external secondary cache, or DMA, to further improve system performance.

DEVELOPMENT SUPPORT

The IDT R3051 family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, sub-system modules, and shrink wrap operating systems. The R3081, which is pin and software compatible with the R3051, can directly utilize these existing tools to reduce time to market.

Figure 7 is an overview of the system development process typically used when developing R3051 family applications. The R3051 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R3051 family applications, and include tools such as:

- Optimizing compilers from MIPS, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT/sim™, which implements a full prom monitor (diagnostics, remote debug support, peek/poke, etc.).
- IDT/kit™, which implements a run-time support package for R3051 family systems.

PERFORMANCE OVERVIEW

The R3081 achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine.** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the execution engine achieves over 35 VUPS performance when operating out of cache.
- **A full featured floating point accelerator/co-processor.** The R3081 incorporates an R3010A compatible floating point accelerator on-chip, with independent ALUs for floating point add, multiply, and divide. The floating point unit is fully hardware interlocked, and features overlapped operation and precise exceptions. The FPA allows floating point adds, multiplies, and divides to occur concurrently with each other, as well as concurrently with integer operations.
- **Large on-chip caches.** The R3051 family contains caches which are substantially larger than those on the majority of today's microprocessors. These large caches minimize the number of bus transactions required, and allow the R3051 family to achieve actual sustained performance very close to its peak execution rate. The R3081 doubles the cache available on the R3052, making it a suitable engine for

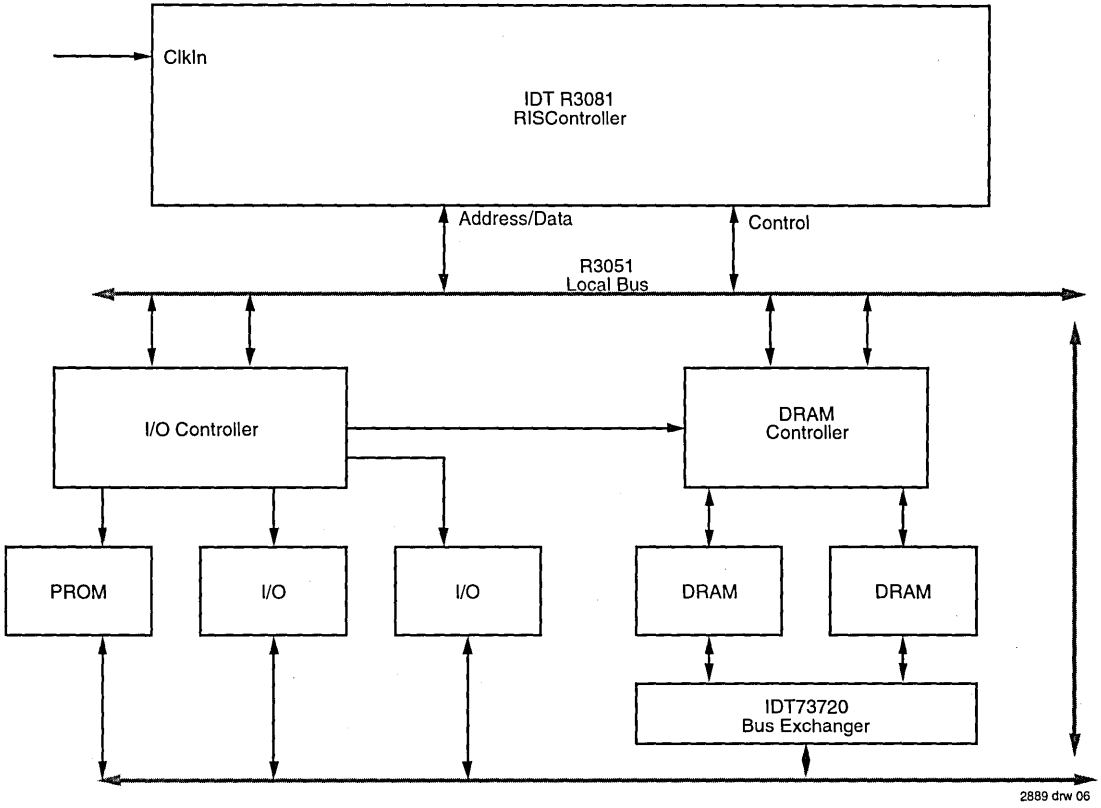


Figure 6. R3081 RISChipset Based System

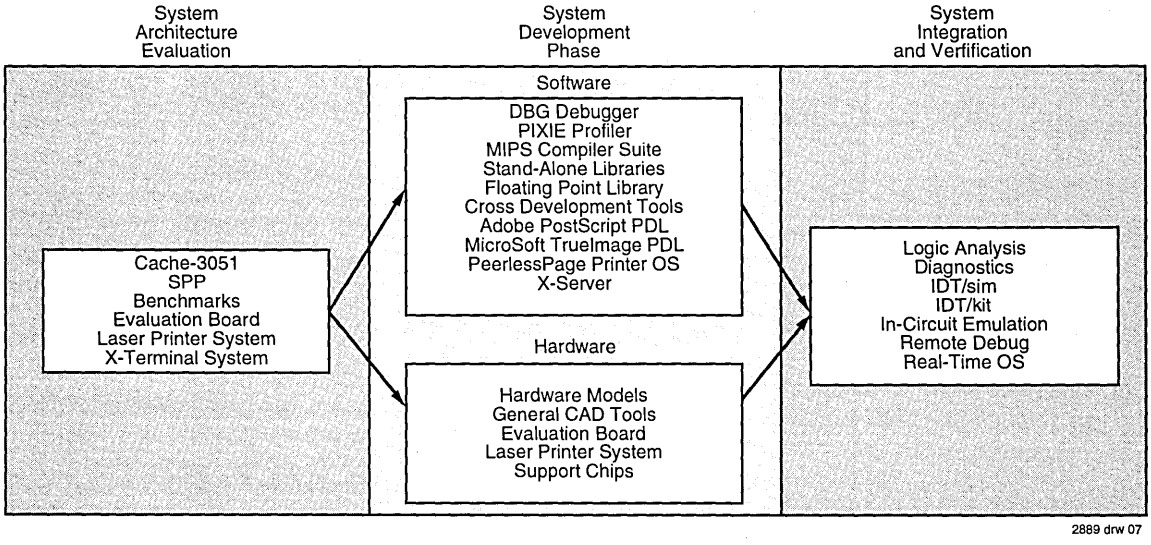


Figure 7. R3051 Family Development Toolchain

many general purpose computing applications, such as ARC compliant systems.

- **Autonomous multiply and divide operations.** The R3051 family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the CPU to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.** The R3081 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.** The R3051 family enables the system designer to utilize page mode or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

These techniques combine to allow the processor to achieve over 43 VUPS integer performance, 13MFlops of Linpack performance, and 70,000 dhrystones without the use of external caches or zero wait-state memory devices.

The performance differences between the various family members depends on the application software and the design of the memory system. The impact of the various cache sizes, and the hardware floating point, can be accurately modeled using Cache-3051. Since the R3041, R3051, R3052, R3071, and R3081 are all pin and software compatible, the system designer has maximum freedom in trading between performance and cost. A system can be designed, and later the appropriate CPU inserted into the board, depending on the desired system performance.

SELECTABLE FEATURES

The R3081 allows the system designer to configure certain aspects of operation. Some of these options are established when the device is reset, while others are enabled via the Config registers:

- **BigEndian vs. LittleEndian Byte Ordering.** The part can be configured to operate with either byte ordering. ACE/ARC systems typically use Little Endian byte ordering. However, various embedded applications, written originally for a Big Endian processor such as the MC680x0, are easier to port to a Big Endian system.
- **Data Cache Refill of one or four words.** The memory system must be capable of performing four word refills of instruction cache misses. The R3081 allows the system designer to enable D-Cache refill of one or four words dynamically. Thus, specialized algorithms can choose one refill size, while the rest of the system can operate with the other.
- **Half-frequency bus mode.** The processor can be configured such that the external bus interface is at one-half the frequency of the processor core. This simplifies system design; however, the large on-chip caches mitigate the performance impact of using a slower system bus clock.
- **Slow bus turn-around.** The R3081 allows the system designer to space processor operations, so that more time is allowed for transitions between memory and the processor on the multiplexed address/data bus.
- **Configurable cache.** The R3081 allows the system designer to use software to select either a 16kB Instruction Cache/4kB Data Cache organization, or an 8kB Instruction/8kB Data Cache organization.
- **Cache Coherent Interface.** The R3081 has an optional hardware based cache coherency interface intended to support multi-master systems such as those utilizing DMA between memory and I/O.
- **Optional 1x or 2x clock input.** The R3081 can be driven with an R3051 compatible 2x clock input, or a lower frequency 1x clock input.

THERMAL CONSIDERATIONS

The R3081 utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, the R3081 is packaged using cavity down packaging, with an embedded thermal slug to improve thermal transfer to the suurrounding air.

The R3081 utilizes the 84-pin MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package allows for an efficient thermal transfer between the die and the case due to the heat spreading effect of the aluminum. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation. The MQUAD package is available at all frequencies, and is pin and form compatible with the PLCC used for the R3051. Thus, designers can inter-change R3081s and R3051s in a particular design, without changing their PC Board.

The R3081 is guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient temperature conditions which will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($Ø_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * Ø_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $Ø_{CA}$ at various airflows are shown in Table 1.

Note that the R3081 allows the operational frequency to be turned down during idle periods to reduce power consumption. This operation is described in the *R3081 Hardware User's Guide*. Reducing the operation frequency dramatically reduces power consumption.

	ØCA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
"MJ" Package*	22	14	12	11	9	8
PLCC Package	29	26	21	18	16	15

2889 tbl 01

Table 1. Thermal Resistance (ØCA) at Various Airflows (*estimated: final values tbd)

NOTES ON SYSTEM DESIGN

The R3081 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

To minimize these AC parameters, the R3081 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3081 to reference input signals to the reference clock seen by the external system. The $\overline{\text{SysClk}}$ output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3081 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

5

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). **$\overline{BE}$(3:0):** These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. During cache coherency operations, the R3081 monitors the A/D bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Addr(3:2)	O	**Low Address (3:2)** A 2-bit bus which indicates which word is currently expected by the processor. Specifically, this two bit bus presents either the address bits for the single word to be transferred (writes or single datum reads) or functions as a two bit counter starting at '00' for burst read operations. During cache coherency operations, the R3081 monitors the Addr bus at the start of a DMA write to capture the write target address for potential data cache invalidates.
Diag(1)	O	**Diagnostic Pin 1.** This output indicates whether the current bus read transaction is due to an on-chip cache miss, and also presents part of the miss address. The value output on this pin is time multiplexed: **Cached:** During the phase in which the A/D bus presents address information, this pin is an active HIGH output which indicates whether the current read is a result of a cache miss. **Miss Address (3):** During the remainder of the read operation, this output presents address bit (3) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. On write cycles, this output signals whether the data being written as retained in the on-chip data cache. The value of this pin is time multiplexed during writes: **Cached:** During the address phase of write transactions, this signal is an active high output which indicates that the store data was retained in the on-chip data cache. **Reserved:** The value of this pin during the data phase of writes is reserved.
Diag(0)	O	**Diagnostic Pin 0.** This output distinguishes cache misses due to instruction references from those due to data references, and presents the remaining bit of the miss address. The value output on this pin is also time multiplexed: **I/$\overline{D}$:** If the "Cached" Pin indicates a cache miss, then a high on this pin at this time indicates an instruction reference, and a low indicates a data reference. If the read is not due to a cache miss but rather an uncached reference, then this pin is undefined during this phase. **Miss Address (2):** During the remainder of the read operation, this output presents address bit (2) of the address the processor was attempting to reference when the cache miss occurred. Regardless of whether a cache miss is being processed, this pin reports the transfer address during this time. During write cycles, the value of this pin during both the address and data phases is reserved.

2889 tbl 02

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
ALE	I/O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically using transparent latches. During cache coherency operations, the R3081 monitors ALE at the start of a DMA write, to capture the write target address for potential data cache invalidates.
$\overline{Rd}$	O	**Read:** An output which indicates that the current bus transaction is a read.
$\overline{Wr}$	I/O	**Write:** An output which indicates that the current bus transaction is a write. During coherent DMA, this input indicates that the current transfer is a write.
$\overline{DataEn}$	O	**External Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers
$\overline{Burst}$/ $\overline{WrNear}$	O	**Burst Transfer/Write Near:** On read transactions, the $\overline{Burst}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if quad word refill is currently selected. On write transactions, the $\overline{WrNear}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 512 word page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows near writes to be retired quickly.
$\overline{Ack}$	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction, and that the CPU may either terminate the write cycle or process the read data from this read transfer. During Coherent DMA, this input indicates that the current write transfer is completed, and that the internal invalidation address counter should be incremented.
$\overline{RdCEn}$	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{SysClk}$	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "Sys" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit. This clock will either be at the same frequency as the CPU execution rate clock, or at one-half that frequency, as selected during reset.
$\overline{BusReq}$	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master.
$\overline{BusGnt}$	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a $\overline{BusReq}$ has been detected, and that the bus is relinquished to the external master.
$\overline{IvdReq}$	I	**Invalidate Request.** An input provided by an external DMA controller to request that the CPU invalidate the Data Cache line corresponding to the current DMA write target address. This signal is the same pin as Diag(0)
$\overline{CohReq}$	I	**Coherent DMA Request.** An input used by the external DMA controller to indicate that the requested DMA operations could involve hardware cache coherency. This signal is the Rsvd(0) of the R3051.
SBrCond(3:2) BrCond(0)	I	**Branch Condition Port:** These external signals are internally connected to the CPU signals CpCond(3:0). These signals can be used by the branch on co-processor condition instructions as input ports. There are two types of Branch Condition inputs: the SBrCond inputs have special internal logic to synchronize the inputs, and thus may be driven by asynchronous agents. The direct Branch Condition inputs must be driven synchronously. Note that BrCond(1) is used by the internal FPA, and thus is not available on an external pin.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.

2889 tbl 03

5

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{Int}$(5:3)	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int}$(5:0) $\overline{SInt}$(2:0) signals of the R3000. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals of the R3000. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts. Note that the interrupt used by the on-chip FPA will not be monitored externally.
ClkIn	I	**Master Clock Input:** This input clock can be provided at the execution frequency of the CPU (1x clock mode) or at twice that frequency (2x clock mode), as selected at reset.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Mode selection is performed during the last cycle of $\overline{Reset}$.
Rsvd(4:1)	I/O	**Reserved:** These four signal pins are reserved for testing and for future revisions of this device. Users must not connect these pins. Note that Rsvd(0) of the R3051 is now used for the $\overline{CohReq}$ input pin.

2889 tbl 04

ABSOLUTE MAXIMUM RATINGS(1, 3)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TC	Operating Case Temperature	0 to +85	–55 to +125	°C
TBIAS	Case Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
VIN	Input Voltage	–0.5 to +7.0	–0.5 to +7.0	V

2889 tbl 05

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = –3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5V.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature(Case)	GND	Vcc
Military	–55°C to +125°C	0V	5.0 ±10%
Commercial	0°C to +85°C	0V	5.0 ±5%
Commercial	0°C to +85°C	0V	3.3 ±5%

2889 tbl 07

AC TEST CONDITIONS—R3081

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	—	0	V

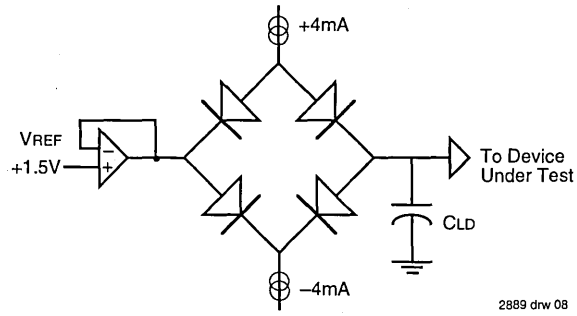
2889 tbl 06

AC TEST CONDITIONS—RV3081

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.0	—	V
VILS	Input LOW Voltage	—	0	V

2889 tbl 06

OUTPUT LOADING FOR AC TESTING



2889 drw 08

Signal	CLD
$\overline{SysClk}$	50 pf
All Others	25 pf

2889 tbl 08

DC ELECTRICAL CHARACTERISTICS RV3081

COMMERCIAL TEMPERATURE RANGE[1, 2]— (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage[3]	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage[1]	—	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage[2,3]	—	2.8	—	2.8	—	V
V_{ILS}	Input LOW Voltage[1,2]	—	—	0.4	—	0.4	V
C_{IN}	Input Capacitance[4,5]	—	—	10	—	10	pF
C_{OUT}	Output Capacitance[4,5]	—	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 3.3V, T_A = 25°C	—	375	—	425	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

NOTES:

2889 tbl 09

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.
5. ALE is 12pF for SysClk values C_{IN} and C_{OUT} for all speeds.

AC ELECTRICAL CHARACTERISTICS RV3081

COMMERCIAL TEMPERATURE RANGE [1, 2]— (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Signals	Description	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t1	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$, $\overline{CohReq}$	Set-up to $\overline{SysClk}$ rising	6	—	5	—	ns
t1a	A/D	Set-up to $\overline{SysClk}$ falling	7	—	6	—	ns
t2	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$, $\overline{CohReq}$	Hold from $\overline{SysClk}$ rising	4	—	4	—	ns
t2a	A/D	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Tri-state from $\overline{SysClk}$ rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Driven from $\overline{SysClk}$ falling	—	10	—	10	ns
t5	$\overline{BusGnt}$	Asserted from $\overline{SysClk}$ rising	—	8	—	7	ns
t6	$\overline{BusGnt}$	Negated from $\overline{SysClk}$ falling	—	8	—	7	ns
t7	$\overline{Wr}$, $\overline{Rd}$, $\overline{Burst/WrNear}$, A/D	Valid from $\overline{SysClk}$ rising	—	5	—	5	ns
t8	ALE	Asserted from $\overline{SysClk}$ rising	—	4	—	4	ns
t9	ALE	Negated from $\overline{SysClk}$ falling	—	4	—	4	ns
t10	A/D	Hold from ALE negated[3]	2	—	2	—	ns
t11	$\overline{DataEn}$	Asserted from $\overline{SysClk}$ falling	—	15	—	15	ns
t12	$\overline{DataEn}$	Asserted from A/D tri-state[3]	0	—	0	—	ns
t14	A/D	Driven from $\overline{SysClk}$ rising[3]	0	—	0	—	ns
t15	$\overline{Wr}$, $\overline{Rd}$, $\overline{DataEn}$, $\overline{Burst/WrNear}$	Negated from $\overline{SysClk}$ falling	—	7	—	6	ns
t16	Addr(3:2)	Valid from $\overline{SysClk}$	—	6	—	6	ns
t17	Diag	Valid from $\overline{SysClk}$	—	12	—	11	ns

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AC ELECTRICAL CHARACTERISTICS RV3081 (cont.)

COMMERCIAL TEMPERATURE RANGE[1, 2] — (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Signals	Description	20MHz Min.	20MHz Max.	25MHz Min.	25MHz Max.	Unit
t18	A/D	Tri-state from $\overline{SysClk}$ falling	—	10	—	10	ns
t19	A/D	$\overline{SysClk}$ falling to data valid	—	13	—	12	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	10	—	8	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	10	—	8	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	tsys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	6	—	5	—	ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	10	—	9	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	0	—	0	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	6	—	5	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	3	—	3	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	6	—	5	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	3	—	3	—	ns
tsys	$\overline{SysClk}$ (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{SysClk}$ (full frequency mode)	Clock High Time[5]	t22-2	t22+2	t22-2	t22+2	ns
t33	$\overline{SysClk}$ (full frequency mode)	Clock LOW Time[5]	t22-2	t22+2	t22-2	t22+2	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]4*t22	4*t22	4*t22	4*t22	4*t22	ns
t34	$\overline{SysClk}$ (half frequency mode)	Clock HIGH Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock LOW Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t36	ALESet-up to $\overline{SysClk}$ falling		9	—	8	—	ns
t37	ALEHold from $\overline{SysClk}$ falling		2	—	2	—	ns
t38	A/DSet-up to ALE falling		10	—	9	—	ns
t39	A/DHold from ALE falling		2	—	2	—	ns
t40	$\overline{Wr}$Set-up to $\overline{SysClk}$ rising		10	—	9	—	ns
t41	$\overline{Wr}$Hold from $\overline{SysClk}$ rising		3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	20	—	16	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	20	—	16	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	50	50	40	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	ns/ 25pF

NOTES:

2889 tbl 11

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.

DC ELECTRICAL CHARACTERISTICS RV3081

COMMERCIAL TEMPERATURE RANGE[1, 2]— (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Parameter	Test Conditions	33MHz		40MHz		Units
			Min.	Max.	Min.	Max.	
VOH	Output HIGH Voltage	Vcc = Min., IOH = –4mA	2.4	—	2.4	—	V
VOL	Output LOW Voltage	Vcc = Min., IOL = 4mA	—	0.4	—	0.4	V
VIH	Input HIGH Voltage[3]	—	2.0	—	2.0	—	V
VIL	Input LOW Voltage[1]	—	—	0.8	—	0.8	V
VIHS	Input HIGH Voltage[2,3]	—	2.8	—	2.8	—	V
VILS	Input LOW Voltage[1,2]	—	—	0.4	—	0.4	V
CIN	Input Capacitance[4,5]	—	—	10	—	10	pF
COUT	Output Capacitance[4,5]	—	—	10	—	10	pF
ICC	Operating Current	Vcc = 3.3V, TA = 25°C	—	525	—	600	mA
IIH	Input HIGH Leakage	VIH = VCC	—	100	—	100	µA
IIL	Input LOW Leakage	VIL = GND	–100	—	–100	—	µA
IOZ	Output Tri-state Leakage	VOH = 2.4V, VOL = 0.5V	–100	100	–100	100	µA

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NOTES:

1. VIL Min. = –3.0V for pulse width less than 15ns. VIL should not fall below -0.5V for larger periods.
2. VIHS and VILS apply to ClkIn and $\overline{\text{Reset}}$.
3. VIH should not be held above Vcc + 0.5V.
4. Guaranteed by design.
5. ALE is 12pF for SysClk values C_{IN} and C_{OUT} for all speeds.

AC ELECTRICAL CHARACTERISTICS RV3081

COMMERCIAL TEMPERATURE RANGE [1, 2]— (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Signals	Description	33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	
t1	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$, $\overline{\text{CohReq3}}$	Set-up to $\overline{\text{SysClk}}$ rising	4	—	3	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	5	—	4.5	—	ns
t2	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$, $\overline{\text{CohReq}}$	Hold from $\overline{\text{SysClk}}$ rising	3	—	3	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Driven from $\overline{\text{SysClk}}$ falling	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	6	—	5	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	6	—	5	ns
t7	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{Burst/WrNear}}$, A/D	Valid from $\overline{\text{SysClk}}$ rising	—	4	—	3.5	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	3	—	3	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	3	—	3	ns
t10	A/D	Hold from ALE negated[3]	1.5	—	1.5	—	ns
t11	$\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$ falling	—	13	—	12	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state[3]	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising[3]	0	—	0	—	ns
t15	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$, $\overline{\text{Burst/WrNear}}$	Negated from $\overline{\text{SysClk}}$ falling	—	5	—	4	ns
t16	Addr(3:2)	Valid from $\overline{\text{SysClk}}$	—	5	—	4.5	ns
t17	Diag	Valid from $\overline{\text{SysClk}}$	—	10	—	9	ns

AC ELECTRICAL CHARACTERISTICS RV3081 (cont.)

COMMERCIAL TEMPERATURE RANGE[1, 2]— (Tc = 0°C to +85°C, Vcc = +3.3V ±5%)

Symbol	Signals	Description	33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	
t18	A/D	Tri-state from $\overline{SysClk}$ falling	—	9	—	8	ns
t19	A/D	$\overline{SysClk}$ falling to data valid	—	11	—	10	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	6.5	—	5.6	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	6.5	—	5.6	—	ns
t22	ClkIn (2x clock mode)	Clock Period	15	250	12.5	250	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	tsys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	4	—	3	—	ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	8	—	7	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	0	—	0	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	4	—	3	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	4	—	3	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
tsys	$\overline{SysClk}$ (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{SysClk}$ (full frequency mode)	Clock High Time[5]	t22-1	t22+1	t22-1	t22+1	ns
t33	$\overline{SysClk}$ (full frequency mode)	Clock LOW Time[5]	t22-1	t22+1	t22-1	t22+1	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]4*t22	4*t22	4*t22	4*t22	4*t22	ns
t34	$\overline{SysClk}$ (half frequency mode)	Clock HIGH Time[5]	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock LOW Time[5]	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t36	ALESet-up to $\overline{SysClk}$ falling		7	—	6	—	ns
t37	ALEHold from $\overline{SysClk}$ falling		1	—	1	—	ns
t38	A/DSet-up to ALE falling		8	—	8	—	ns
t39	A/DHold from ALE falling		1	—	1	—	ns
t40	$\overline{Wr}$Set-up to $\overline{SysClk}$ rising		8	—	7	—	ns
t41	$\overline{Wr}$Hold from $\overline{SysClk}$ rising		3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	13	—	11[6]	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	13	—	11[6]	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	30	50	25	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	ns/ 25pF

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1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns

DC ELECTRICAL CHARACTERISTICS R3081
COMMERCIAL TEMPERATURE RANGE — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		33.33MHz		40MHz		50MHZ		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_A = 25°C	—	475	—	525	—	625	—	700	—	825	mA
I_{IH}	Input HIGH Leakage	V_{IH} = V_{CC}	—	100	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	–100	100	µA

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NOTES:

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.

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AC ELECTRICAL CHARACTERISTICS R3081

COMMERCIAL TEMPERATURE RANGE [1, 2] (20, 25MHz)—(Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

Symbol	Signals	Description	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError,	Set-up to SysClk rising RdCEn, CohReq	6	—	5	—	ns
t1a	A/D	Set-up to SysClk falling	7	—	6	—	ns
t2	BusReq, Ack, BusError,	Hold from SysClk rising RdCEn, CohReq	4	—	4	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	ns
t3	A/D, Addr, Diag, ALE, Wr	Tri-state from SysClk rising Burst/WrNear, Rd, DataEn	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr	Driven from SysClk falling Burst/WrNear, Rd, DataEn	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	8	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	8	—	7	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	—	5	ns
t8	ALE	Asserted from SysClk rising	—	4	—	4	ns
t9	ALE	Negated from SysClk falling	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state[3]	0	—	0	—	ns
t14	A/D	Driven from SysClk rising[3]	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	7	—	6	ns
t16	Addr(3:2)	Valid from SysClk	—	6	—	6	ns
t17	Diag	Valid from SysClk	—	12	—	11	ns
t18	A/D	Tri-state from SysClk falling	—	10	—	10	ns
t19	A/D	SysClk falling to data valid	—	13	—	12	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	10	—	8	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	10	—	8	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	3	—	ns
tsys	SysClk (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk (full frequency mode)	Clock HIGH Time[5]	t22-2	t22+2	t22-2	t22+2	ns

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NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
7. When using the Reduced Frequency feature, the minimum allowed internal CPU speed is 0.5 MHz.

AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

COMMERCIAL TEMPERATURE RANGE[1, 2] (20, 25MHz)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	20MHz Min.	20MHz Max.	25MHz Min.	25MHz Max.	Unit
t33	SysClk (full frequency mode)	Clock LOW Time[5]	t22-2	t22+2	t22-2	t22+2	ns
tsys/2	SysClk (half frequency mode)	Pulse Width [5]	4*t22	4*t22	4*t22	4*t22	ns
t34	SysClk (half frequency mode)	Clock HIGH Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t35	SysClk (half frequency mode)	Clock LOW Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t36	ALE	Set-up to SysClk falling	9	—	8	—	ns
t37	ALE	Hold from SysClk falling	2	—	2	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	ns
t40	Wr	Set-up to SysClk rising	10	—	9	—	ns
t41	Wr	Hold from SysClk rising	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	20	—	16	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	20	—	16	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	50	50	40	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	ns/ 25pF

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NOTES:
1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
7. When using the Reduced Frequency feature, the minimum allowed internal CPU speed is 0.5 MHz.

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AC ELECTRICAL CHARACTERISTICS R3081

COMMERCIAL TEMPERATURE RANGE [1, 2] (33, 40MHz)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	33MHz Min.	33MHz Max.	40MHz Min.	40MHz Max.	Unit
t1	BusReq, Ack, BusError, RdCEn, CohReq	Set-up to SysClk rising	4	—	3	—	ns
t1a	A/D	Set-up to SysClk falling	5	—	4.5	—	ns
t2	BusReq, Ack, BusError, RdCEn, CohReq	Hold from SysClk rising	3	—	3	—	ns
t2a	A/D	Hold from SysClk falling	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	6	—	5	ns
t6	BusGnt	Negated from SysClk falling	—	6	—	5	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	4	—	3.5	ns
t8	ALE	Asserted from SysClk rising	—	3	—	3	ns
t9	ALE	Negated from SysClk falling	—	3	—	3	ns
t10	A/D	Hold from ALE negated	1.5	—	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	13	—	12	ns
t12	DataEn	Asserted from A/D tri-state[3]	0	—	0	—	ns
t14	A/D	Driven from SysClk rising[3]	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	5	—	4	ns

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AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

COMERCIAL TEMPERATURE RANGE [1, 2] (33, 40MHz)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	33MHz		40MHz		Unit
			Min.	Max.	Min.	Max.	
t16	Addr(3:2)	Valid from $\overline{SysClk}$	—	5	—	4.5	ns
t17	Diag	Valid from $\overline{SysClk}$	—	10	—	9	ns
t18	A/D	Tri-state from $\overline{SysClk}$ falling	—	9	—	8	ns
t19	A/D	$\overline{SysClk}$ falling to data valid	—	11	—	10	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	6.5	—	5.6	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	6.5	—	5.6	—	ns
t22	ClkIn (2x clock mode)	Clock Period	15	250	12.5	250	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	tsys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	4	—	3		ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	8	—	7	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	0	—	0	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	4	—	3	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	4	—	3	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
tsys	$\overline{SysClk}$ (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{SysClk}$ (full frequency mode)	Clock HIGH Time[5]	t22-1	t22+1	t22-1	t22+1	ns
t33	$\overline{SysClk}$ (full frequency mode)	Clock LOW Time[5]	t22-1	t22+1	t22-1	t22+1	ns
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]	4*t22	4*t22	4*t22	4*t22	ns
t34	$\overline{SysClk}$ (half frequency mode)	Clock HIGH Time[5]	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock LOW Time[5]	2*t22-1	2*t22+1	2*t22-1	2*t22+1	ns
t36	ALE	Set-up to $\overline{SysClk}$ falling	7	—	6	—	ns
t37	ALE	Hold from $\overline{SysClk}$ falling	1	—	1	—	ns
t38	A/D	Set-up to ALE falling	8	—	8	—	ns
t39	A/D	Hold from ALE falling	1	—	1	—	ns
t40	$\overline{Wr}$	Set-up to $\overline{SysClk}$ rising	8	—	7	—	ns
t41	$\overline{Wr}$	Hold from $\overline{SysClk}$ rising	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	13	—	11[6]	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	13	—	11[6]	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	30	50	25	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	ns/ 25pF

NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40 and 50MHz.
7. When using the Reduced Frequency feature, the minimum allowed internal CPU speed is 0.5 MHz.

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AC ELECTRICAL CHARACTERISTICS R3081

COMMERCIAL TEMPERATURE RANGE [1, 2] (50MHz)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	50MHz Min.	50MHz Max.	Unit
t1	BusReq, Ack, BusError,	Set-up to SysClk rising RdCEn, CohReq	5	—	ns
t1a	A/D	Set-up to SysClk falling	6	—	ns
t2	BusReq, Ack, BusError,	Hold from SysClk rising RdCEn, CohReq	4	—	ns
t2a	A/D	Hold from SysClk falling	2	—	ns
t3	A/D, Addr, Diag, ALE, Wr	Tri-state from SysClk rising Burst/WrNear, Rd, DataEn	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr	Driven from SysClk falling Burst/WrNear, Rd, DataEn	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	7	ns
t7	Wr, Rd, Burst/WrNear, A/D	Valid from SysClk rising	—	5	ns
t8	ALE	Asserted from SysClk rising	—	4	ns
t9	ALE	Negated from SysClk falling	—	4	ns
t10	A/D	Hold from ALE negated	1.5	—	ns
t11	DataEn	Asserted from SysClk falling	—	15	ns
t12	DataEn	Asserted from A/D tri-state[3]	0	—	ns
t14	A/D	Driven from SysClk rising[3]	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear	Negated from SysClk falling	—	6	ns
t16	Addr(3:2)	Valid from SysClk	—	6	ns
t17	Diag	Valid from SysClk	—	11	ns
t18	A/D	Tri-state from SysClk falling	—	10	ns
t19	A/D	SysClk falling to data valid	—	12	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	N/A [8]		ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	N/A [8]		ns
t22	ClkIn (2x clock mode)	Clock Period	N/A [7, 8]		ns
t23	Reset	Pulse Width from Vcc valid	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	tsys
t25	Reset	Set-up to SysClk falling	5		ns
t26	Int	Mode set-up to Reset rising	9	—	ns
t27	Int	Mode hold from Reset rising	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	3	—	ns
tsys	SysClk (full frequency mode)	Pulse Width[5]	N/A [8]	N/A [8]	ns
t32	SysClk (full frequency mode)	Clock HIGH Time[5]	N/A [8]	N/A [8]	ns
t33	SysClk (full frequency mode)	Clock LOW Time[5]	N/A [8]	N/A [8]	ns

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NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
7. When using the Reduced Frequency feature, the minimum allowed internal CPU speed is 0.5 MHz.
8. For the 50MHz version, 1x Clock Mode and half-frequency bus mode only.

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AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

COMERCIAL TEMPERATURE RANGE [1, 2] (50MHz)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	50MHz Min.	50MHz Max.	Unit
tsys/2	$\overline{SysClk}$ (half frequency mode)	Pulse Width[5]	2*t44	2*t44	ns
t34	$\overline{SysClk}$ (half frequency mode)	Clock HIGH Time[5]	t44-1	t44+1	ns
t35	$\overline{SysClk}$ (half frequency mode)	Clock LOW Time[5]	t44-1	t44+1	ns
t36	ALE	Set-up to $\overline{SysClk}$ falling	8	—	ns
t37	ALE	Hold from $\overline{SysClk}$ falling	2	—	ns
t38	A/D	Set-up to ALE falling	9	—	ns
t39	A/D	Hold from ALE falling	2	—	ns
t40	$\overline{Wr}$	Set-up to $\overline{SysClk}$ rising	9	—	ns
t41	$\overline{Wr}$	Hold from $\overline{SysClk}$ rising	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	16[6]	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	16[6]	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	40	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	ns/ 25pF

NOTES:

1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns, 3ns for 40MHz and 50MHz.
7. When using the Reduced Frequency feature, the minimum allowed internal CPU speed is 0.5 MHz.
8. For the 50MHz version, 1x Clock Mode and half-frequencybus mode only.

DC ELECTRICAL CHARACTERISTICS R3081

MILITARY TEMPERATURE RANGE— (T_C[5] = -55°C to +125°C, V_{CC} = +5.0V ±10%)

Symbol	Parameter	Test Conditions	20MHz		25MHz		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage[3]	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage[1]	—	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage[2,3]	—	2.8	—	2.8	—	V
V_{ILS}	Input LOW Voltage[1,2]	—	—	0.4	—	0.4	V
C_{IN}	Input Capacitance[4]	—	—	12	—	12	pF
C_{OUT}	Output Capacitance[4]	—	—	12	—	12	pF
I_{CC}	Operating Current	V_{CC} = 5.0V, T_A = 25°C	—	550	—	650	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	µA

NOTES:

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1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5V for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{Reset}$.
3. V_{IH} should not be held above V_{CC} + 0.5V.
4. Guaranteed by design.
5. Case Temperatures are "instant on."

AC ELECTRICAL CHARACTERISTICS R3081

MILITARY TEMPERATURE RANGE [1, 2]— (T_C[7] = -55°C to +125°C, V_{CC} = +5.0V ±10%)

Symbol	Signals	Description	20MHz		25MHz		Unit
			Min.	Max.	Min.	Max.	
t1	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$, $\overline{CohReq}$	Set-up to $\overline{SysClk}$ rising	6	—	5	—	ns
t1a	A/D	Set-up to $\overline{SysClk}$ falling	7	—	6	—	ns
t2	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$, $\overline{CohReq}$	Hold from $\overline{SysClk}$ rising	4	—	4	—	ns
t2a	A/D	Hold from $\overline{SysClk}$ falling	2	—	2	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Tri-state from $\overline{SysClk}$ rising	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Driven from $\overline{SysClk}$ falling	—	10	—	10	ns
t5	$\overline{BusGnt}$	Asserted from $\overline{SysClk}$ rising	—	8	—	7	ns
t6	$\overline{BusGnt}$	Negated from $\overline{SysClk}$ falling	—	8	—	7	ns
t7	$\overline{Wr}$, $\overline{Rd}$, $\overline{Burst/WrNear}$, A/D	Valid from $\overline{SysClk}$ rising	—	5	—	5	ns
t8	ALE	Asserted from $\overline{SysClk}$ rising	—	4.5	—	4.5	ns
t9	ALE	Negated from $\overline{SysClk}$ falling	—	4	—	4	ns
t10	A/D	Hold from ALE negated[3]	1.5	—	1.5	—	ns
t11	$\overline{DataEn}$	Asserted from $\overline{SysClk}$ falling	—	15	—	15	ns
t12	$\overline{DataEn}$	Asserted from A/D tri-state[3]	0	—	0	—	ns
t14	A/D	Driven from $\overline{SysClk}$ rising[3]	0	—	0	—	ns
t15	$\overline{Wr}$, $\overline{Rd}$, $\overline{DataEn}$, $\overline{Burst/WrNear}$	Negated from $\overline{SysClk}$ falling	—	7	—	6	ns
t16	Addr(3:2)	Valid from $\overline{SysClk}$	—	6	—	6	ns
t17	Diag	Valid from $\overline{SysClk}$	—	12	—	11	ns

AC ELECTRICAL CHARACTERISTICS R3081 (cont.)

MILITARY TEMPERATURE RANGE[1, 2] — (T_C[7] = -55°C to +125°C, V_{CC} = +5.0V ±10%)

Symbol	Signals	Description	20MHz Min.	20MHz Max.	25MHz Min.	25MHz Max.	Unit
t18	A/D	Tri-state from SysClk falling	—	10	—	10	ns
t19	A/D	SysClk falling to data valid	—	13	—	12	ns
t20	ClkIn (2x clock mode)	Pulse Width HIGH	10	—	8	—	ns
t21	ClkIn (2x clock mode)	Pulse Width LOW	10	—	8	—	ns
t22	ClkIn (2x clock mode)	Clock Period	25	250	20	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	µs
t24	Reset	Minimum Pulse Width	32	—	32	—	tsys
t25	Reset	Set-up to SysClk falling	6	—	5	—	ns
t26	Int	Mode set-up to Reset rising	10	—	9	—	ns
t27	Int	Mode hold from Reset rising	0	—	0	—	ns
t28	SInt, SBrCond	Set-up to SysClk falling	6	—	5	—	ns
t29	SInt, SBrCond	Hold from SysClk falling	3.5	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	6	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	3.5	—	3	—	ns
tsys	SysClk (full frequency mode)	Pulse Width[5]	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk (full frequency mode)	Clock High Time[5]	t22-2	t22+2	t22-2	t22+2	ns
t33	SysClk (full frequency mode)	Clock LOW Time[5]	t22-2	t22+2	t22-2	t22+2	ns
tsys/2	SysClk (half frequency mode)	Pulse Width[5]	4*t22	4*t22	4*t22	4*t22	ns
t34	SysClk (half frequency mode)	Clock HIGH Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t35	SysClk (half frequency mode)	Clock LOW Time[5]	2*t22-2	2*t22+2	2*t22-2	2*t22+2	ns
t36	ALE	Set-up to SysClk falling	9	—	8	—	ns
t37	ALE	Hold from SysClk falling	2	—	2	—	ns
t38	A/D	Set-up to ALE falling	10	—	9	—	ns
t39	A/D	Hold from ALE falling	2	—	2	—	ns
t40	Wr	Set-up to SysClk rising	10	—	9	—	ns
t41	Wr	Hold from SysClk rising	3	—	3	—	ns
t42	ClkIn (1x clock mode)	Pulse Width HIGH[6]	20	—	16	—	ns
t43	ClkIn (1x clock mode)	Pulse Width LOW[6]	20	—	16	—	ns
t44	ClkIn (1x clock mode)	Clock Period[6]	50	50	40	50	ns
tderate	All outputs	Timing deration for loading over C_{LD}[3, 4]	—	1	—	1	ns/ 25pF

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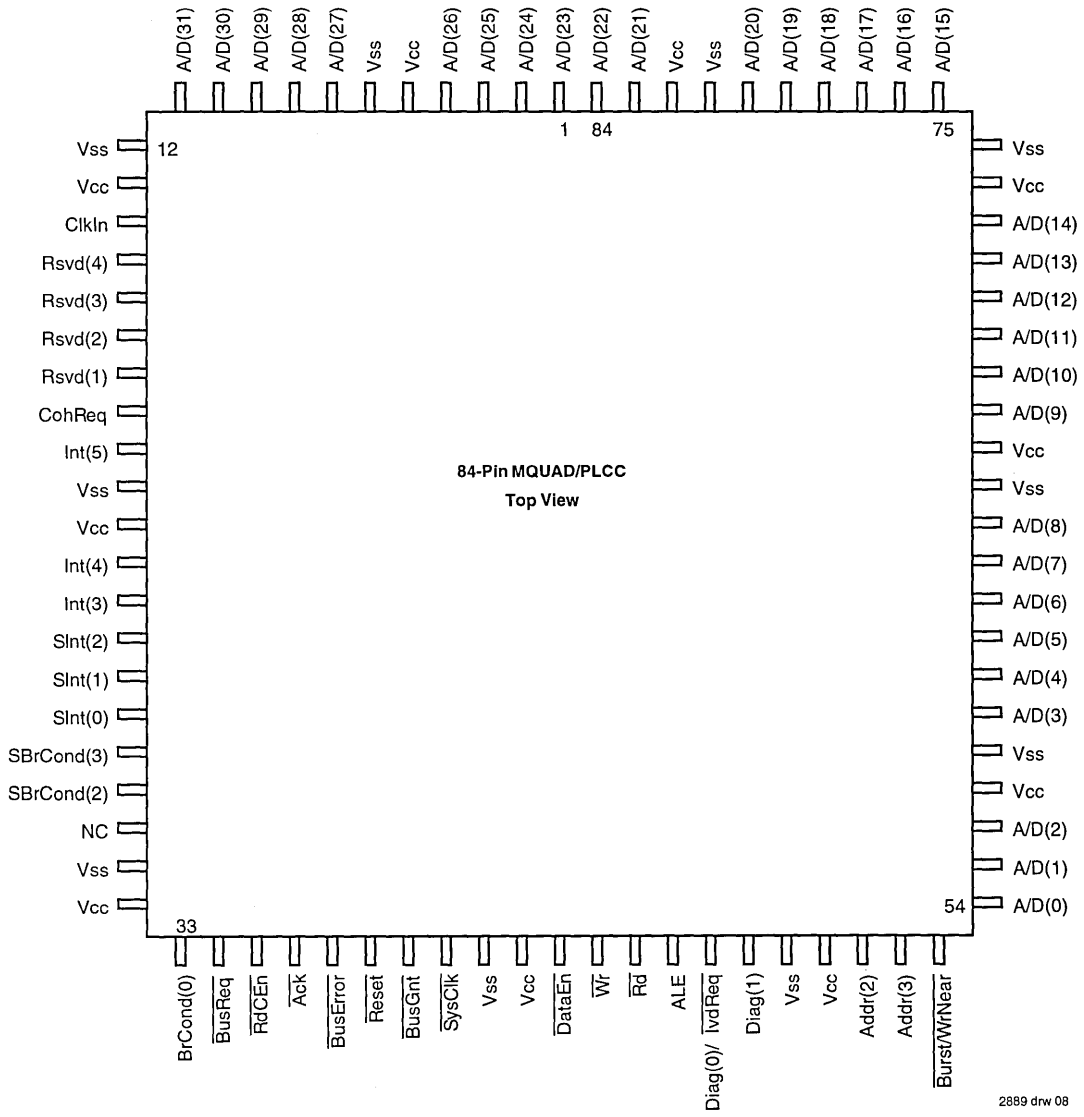
NOTES:

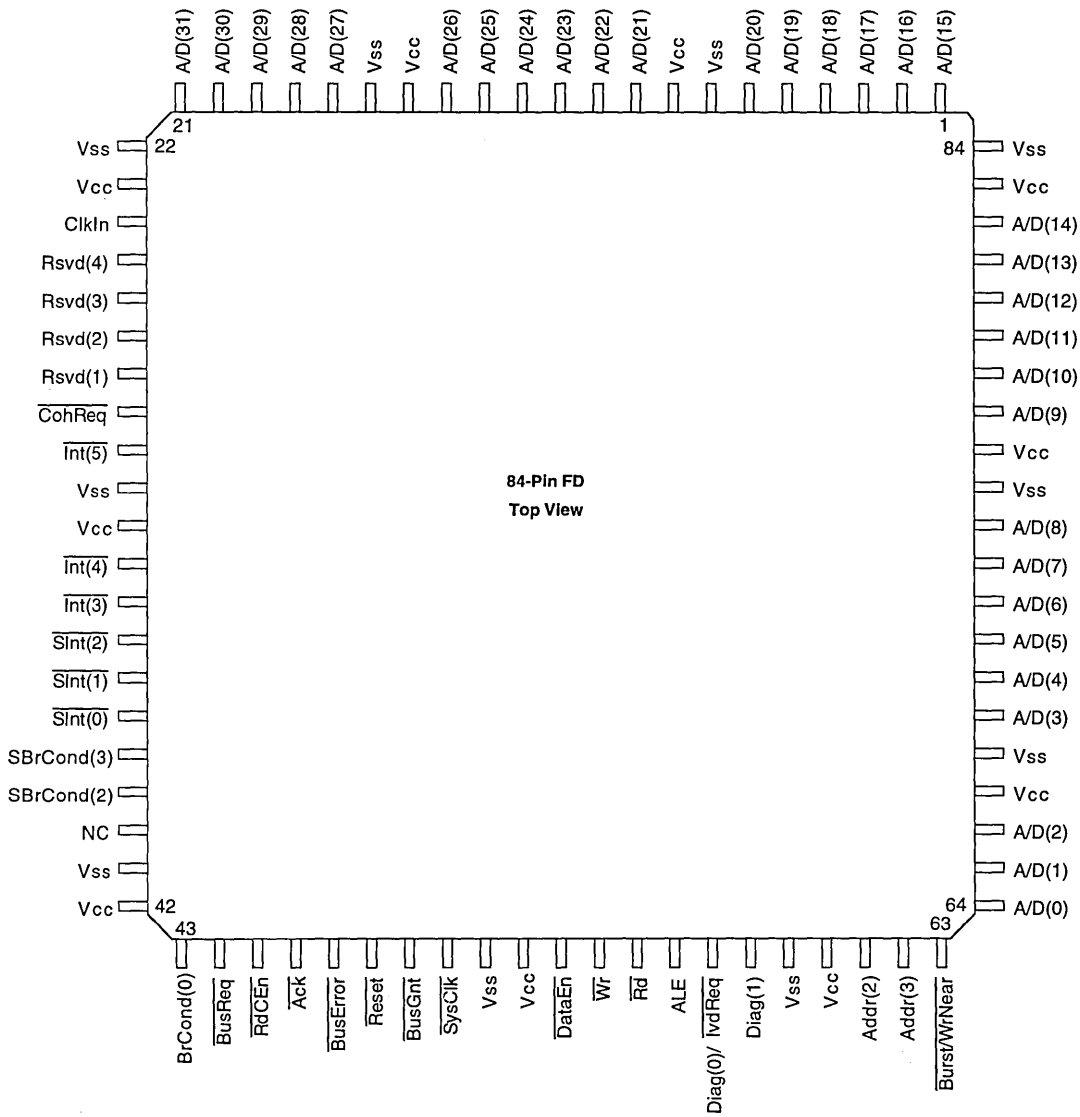
1. All timings referenced to 1.5V. All timings measured with respect to a 2.5ns rise and fall time.
2. The AC values listed here reference timing diagrams contained in the *R3081 Family Hardware User's Manual.*
3. Guaranteed by design.
4. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
5. In 1x clock mode, t22 is replaced by t44/2.
6. In 1x clock mode, the design guarantees that the input clock rise and fall times can be as long as 5ns.
7. Case Temperatures are "instant on."

PIN CONFIGURATIONS

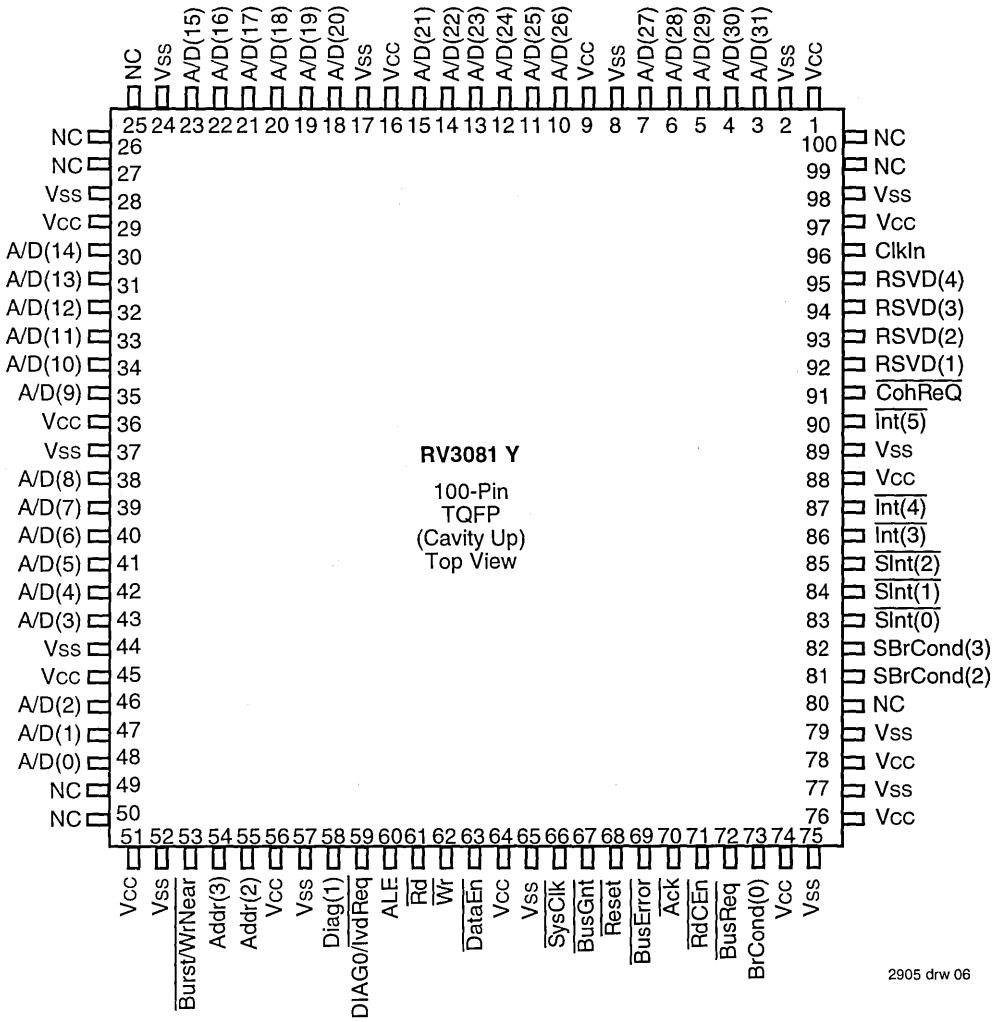


NOTE:
Reserved Pins must not be connected.

PIN CONFIGURATIONS



NOTE:
Reserved Pins must not be connected.


RV3081 Y
100-Pin
TQFP
(Cavity Up)
Top View
1 NC
2 Vss
3 A/D(31)
4 A/D(30)
5 A/D(29)
6 A/D(28)
7 A/D(27)
8 Vss
9 Vcc
10 A/D(26)
11 A/D(25)
12 A/D(24)
13 A/D(23)
14 A/D(22)
15 A/D(21)
16 Vcc
17 Vss
18 A/D(20)
19 A/D(19)
20 A/D(18)
21 A/D(17)
22 A/D(16)
23 A/D(15)
24 Vss
25 NC
26 NC
27 NC
28 Vss
29 Vcc
30 A/D(14)
31 A/D(13)
32 A/D(12)
33 A/D(11)
34 A/D(10)
35 A/D(9)
36 Vcc
37 Vss
38 A/D(8)
39 A/D(7)
40 A/D(6)
41 A/D(5)
42 A/D(4)
43 A/D(3)
44 Vss
45 Vcc
46 A/D(2)
47 A/D(1)
48 A/D(0)
49 NC
50 NC
51 Vcc
52 Vss
53 Burst/WrNear
54 Addr(3)
55 Addr(2)
56 Vcc
57 Vss
58 Diag(1)
59 DIAG0/IvdReq
60 ALE
61 Rd
62 Wr
63 DataEn
64 Vcc
65 Vss
66 SysClk
67 BusGnt
68 Reset
69 BusError
70 Ack
71 RdCEn
72 BusReq
73 BrCond(0)
74 Vcc
75 Vss
76 Vcc
77 Vss
78 Vcc
79 Vss
80 NC
81 SBrCond(2)
82 SBrCond(3)
83 SInt(0)
84 SInt(1)
85 SInt(2)
86 Int(3)
87 Int(4)
88 Vcc
89 Vss
90 Int(5)
91 CohReQ
92 RSVD(1)
93 RSVD(2)
94 RSVD(3)
95 RSVD(4)
96 ClkIn
97 Vcc
98 Vss
99 NC
100 NC

2905 drw 06

5

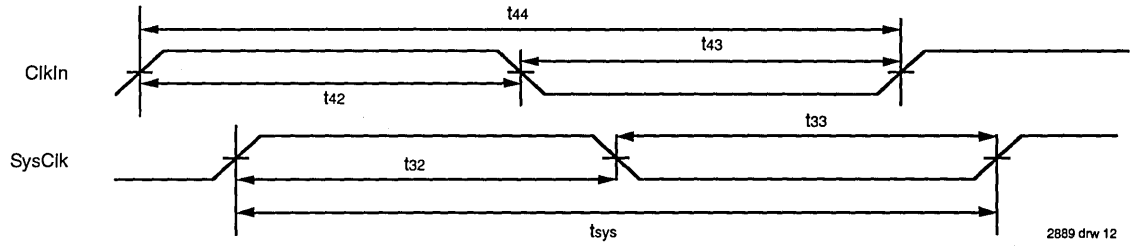


Figure 8 (a). R3081 Clocking (1x clock input mode, full frequency bus)

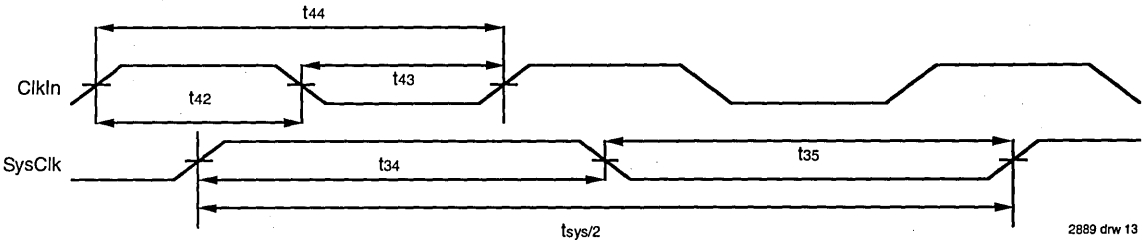


Figure 8 (b). R3081Clocking (1x clock input mode, half-frequency bus)

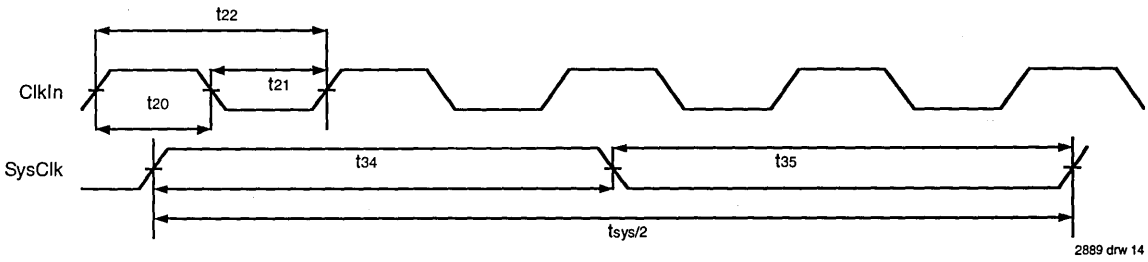


Figure 8 (c). R3081 Clocking (2x clock input mode, half-frequency bus)

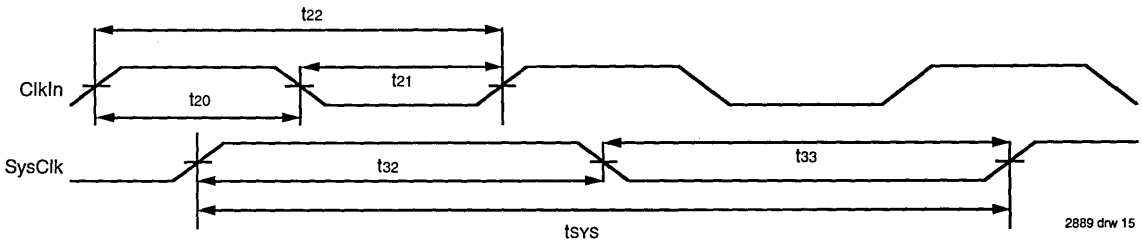


Figure 8 (d). R3081 Clocking (2x clock input mode, full-frequency bus)

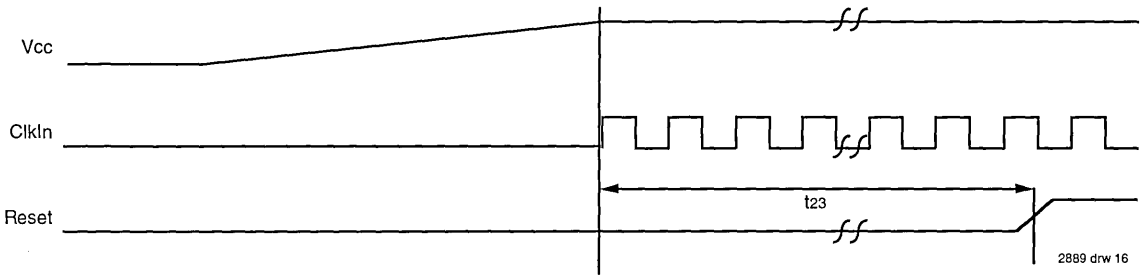


Figure 9. Power-On Reset Sequence

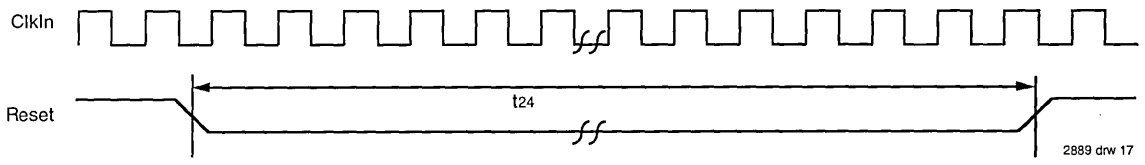


Figure 10. Warm Reset Sequence

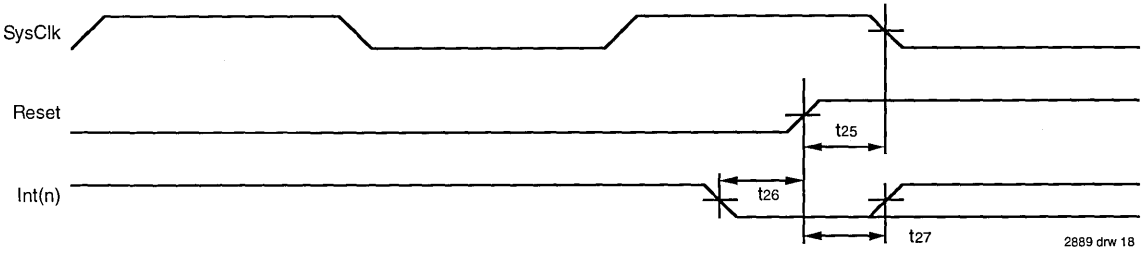


Figure 11. Mode Selection and Negation of Reset

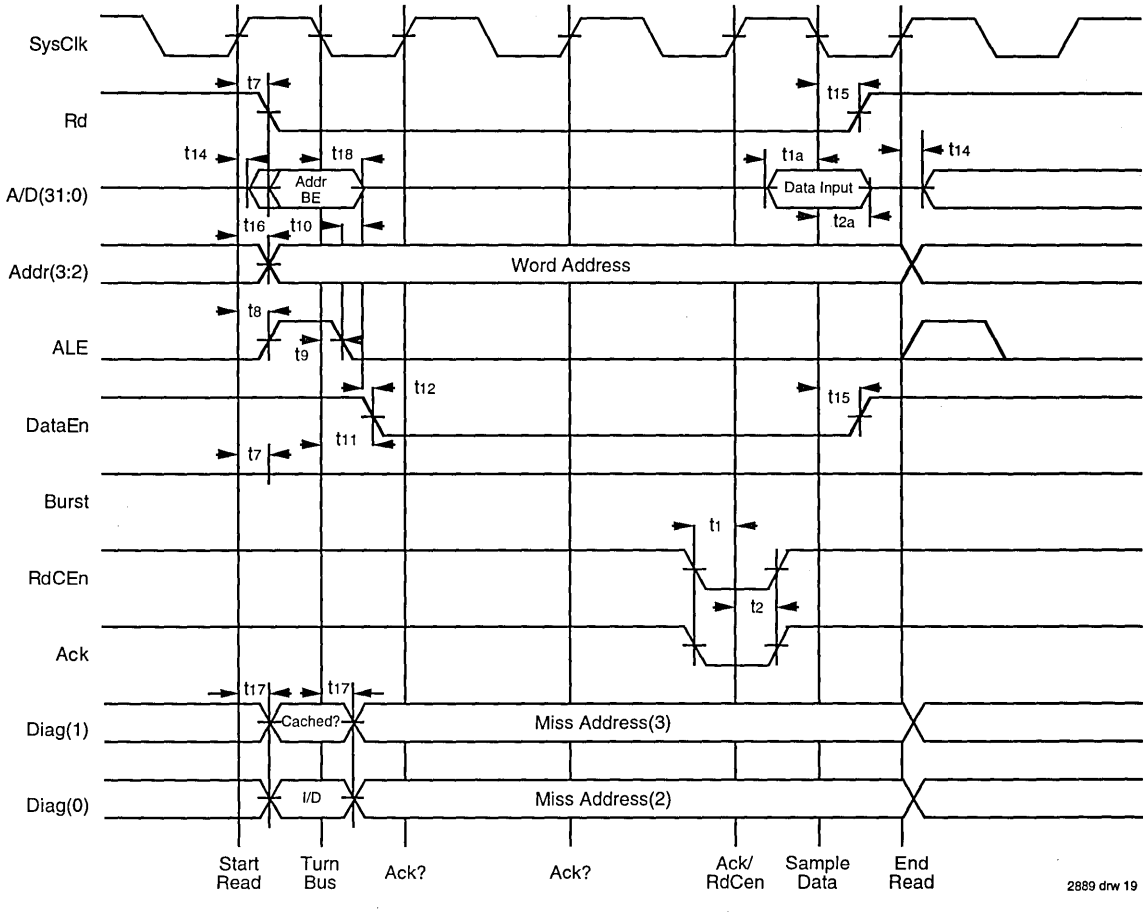


Figure 12. Single Datum Read in R3081

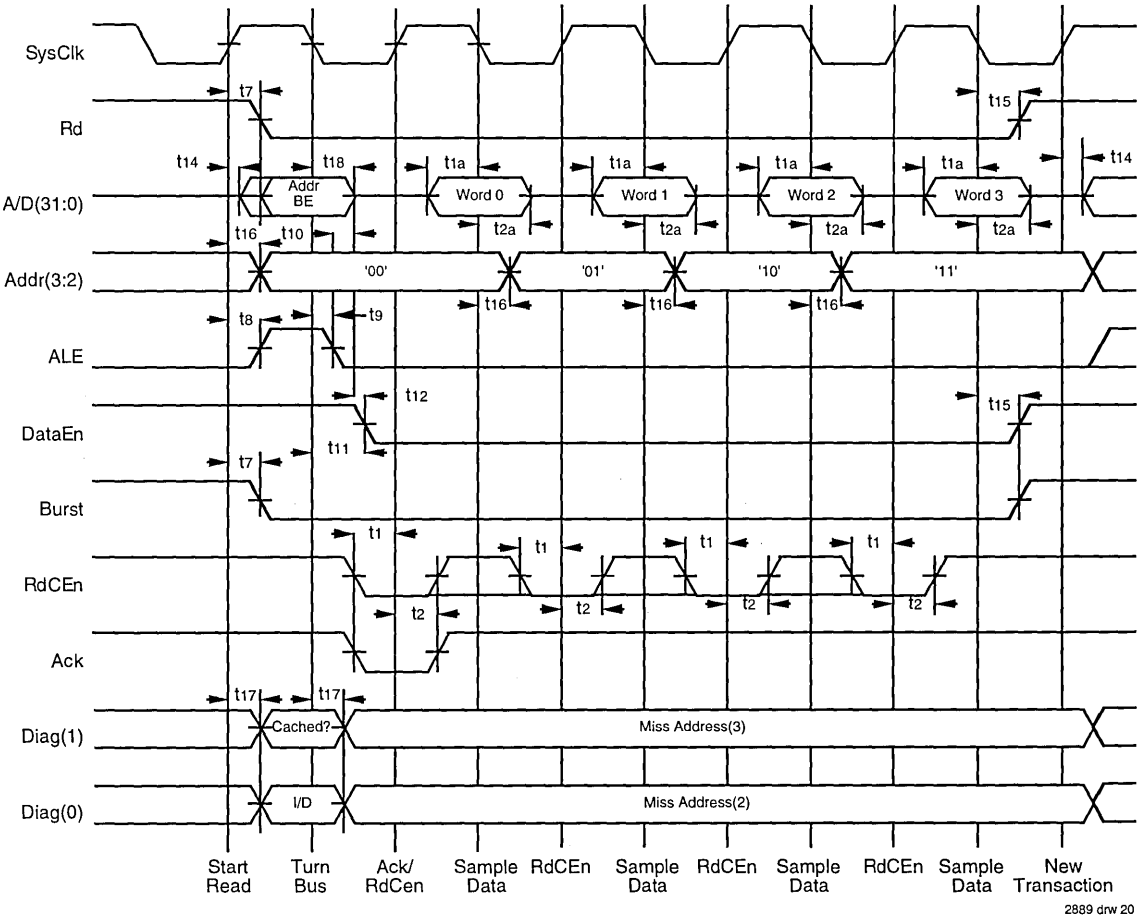


Figure 13. R3081 Burst Read

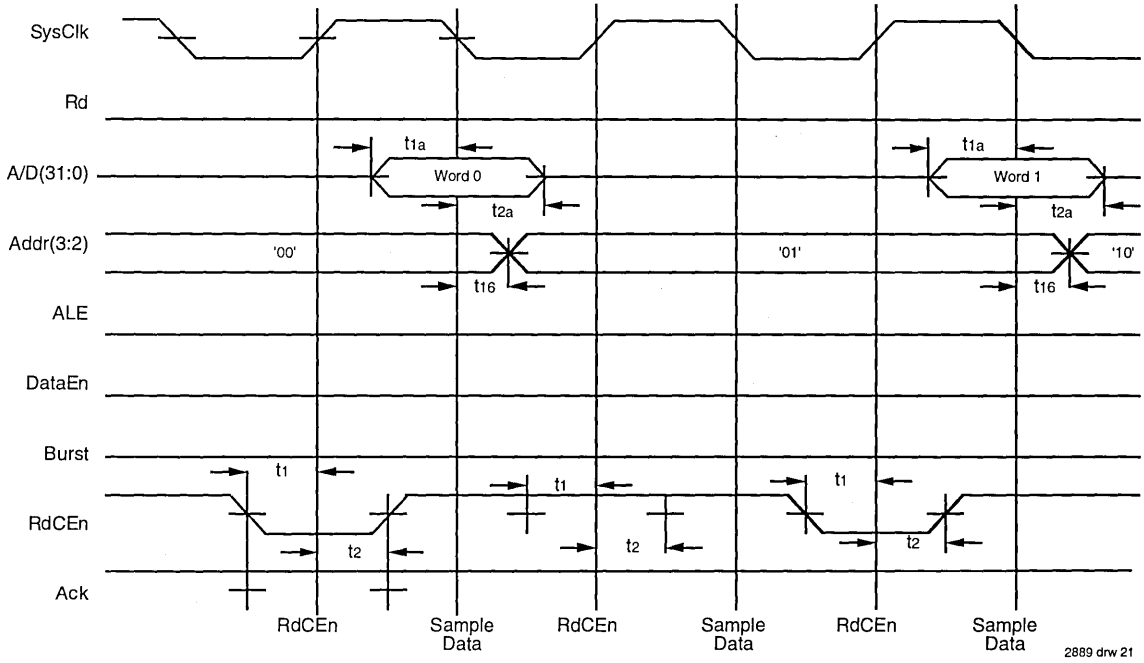


Figure 14 (a). Start of Throttled Quad Read

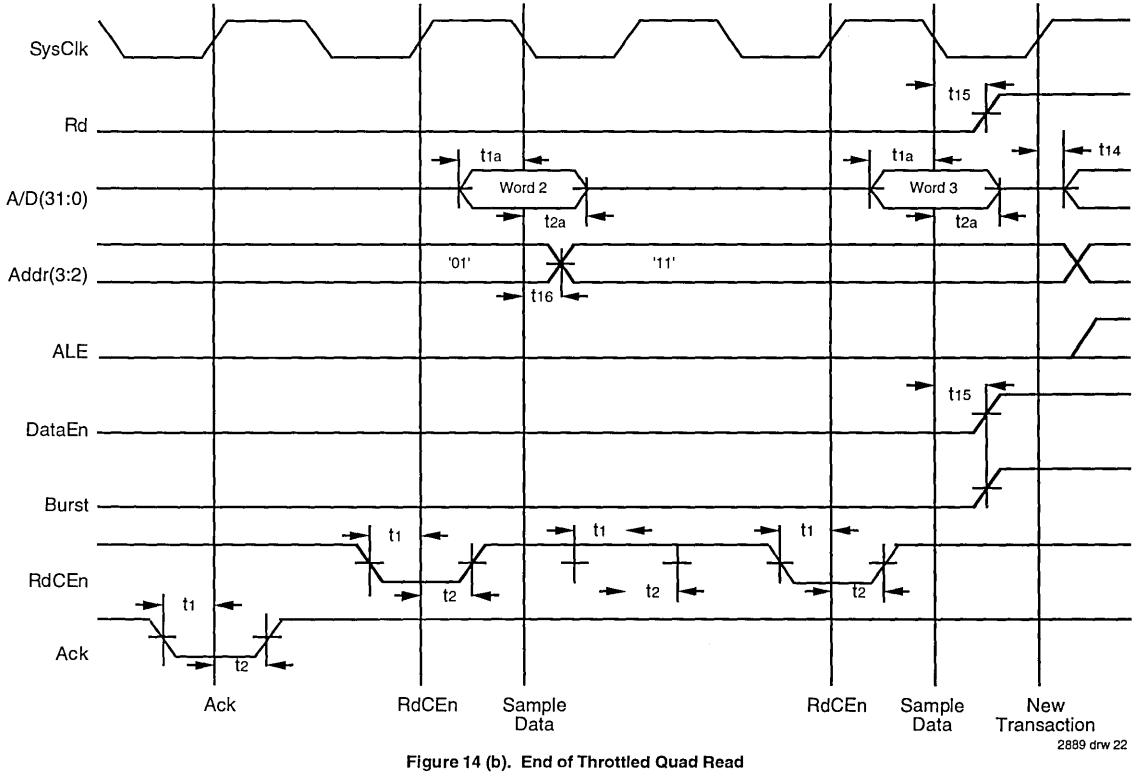


Figure 14 (b). End of Throttled Quad Read

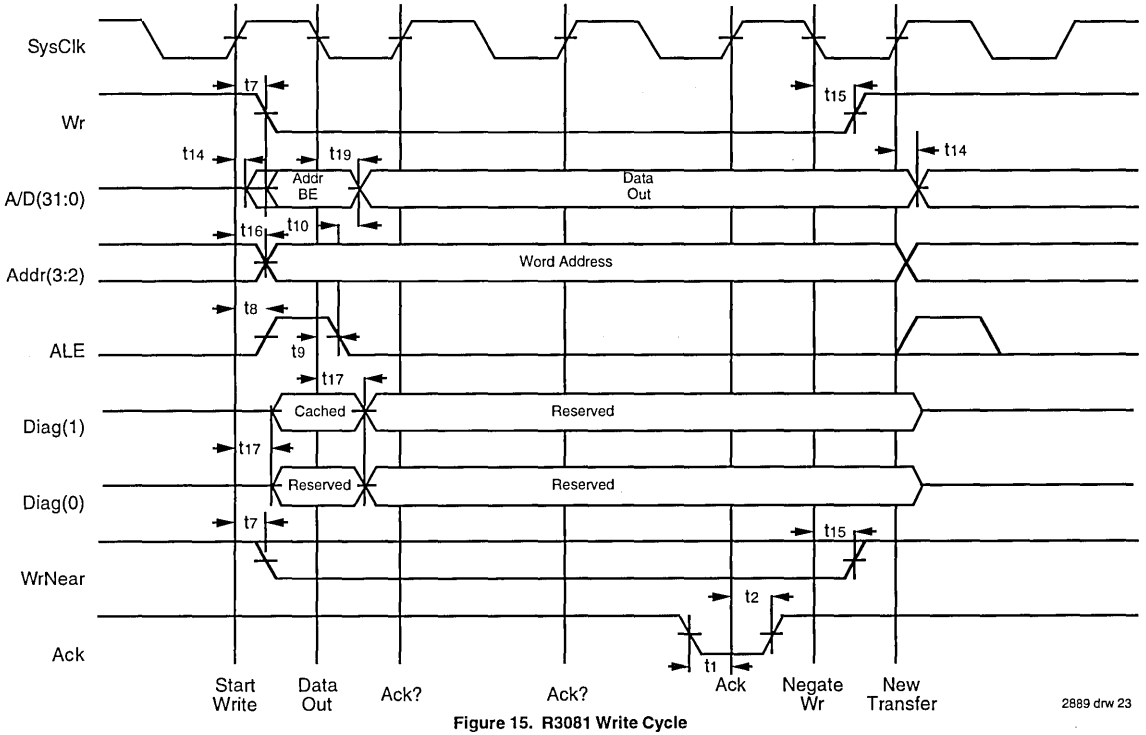


Figure 15. R3081 Write Cycle

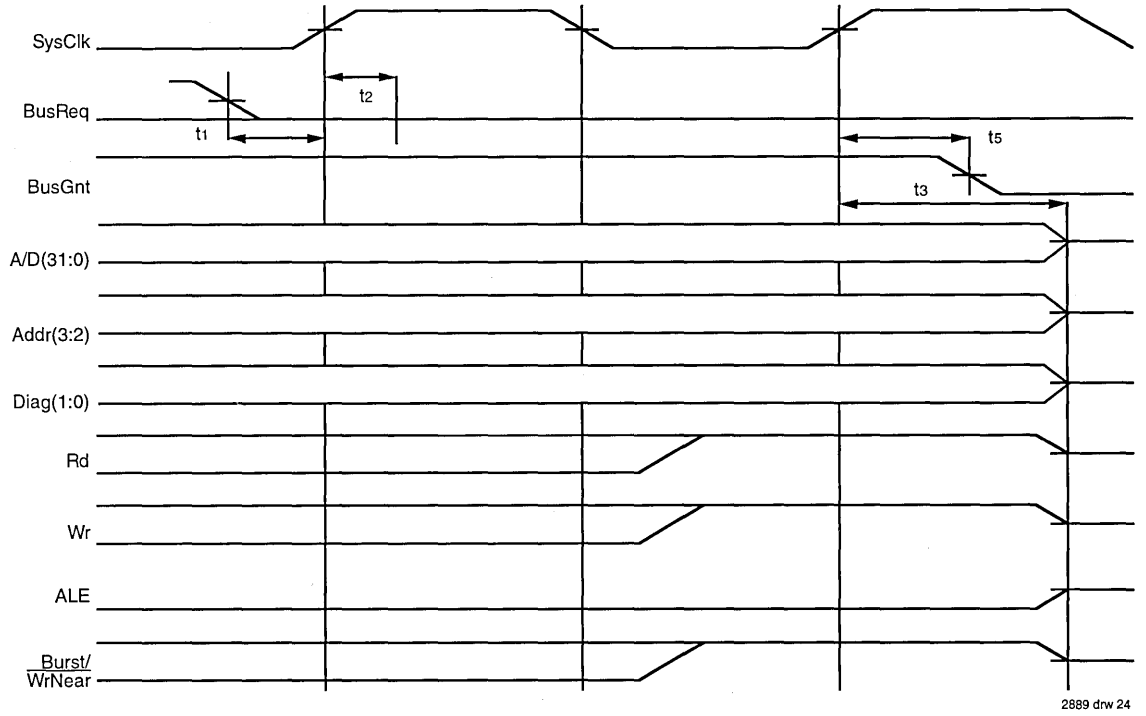


Figure 16. Request and Relinquish of R3081 Bus to External Master

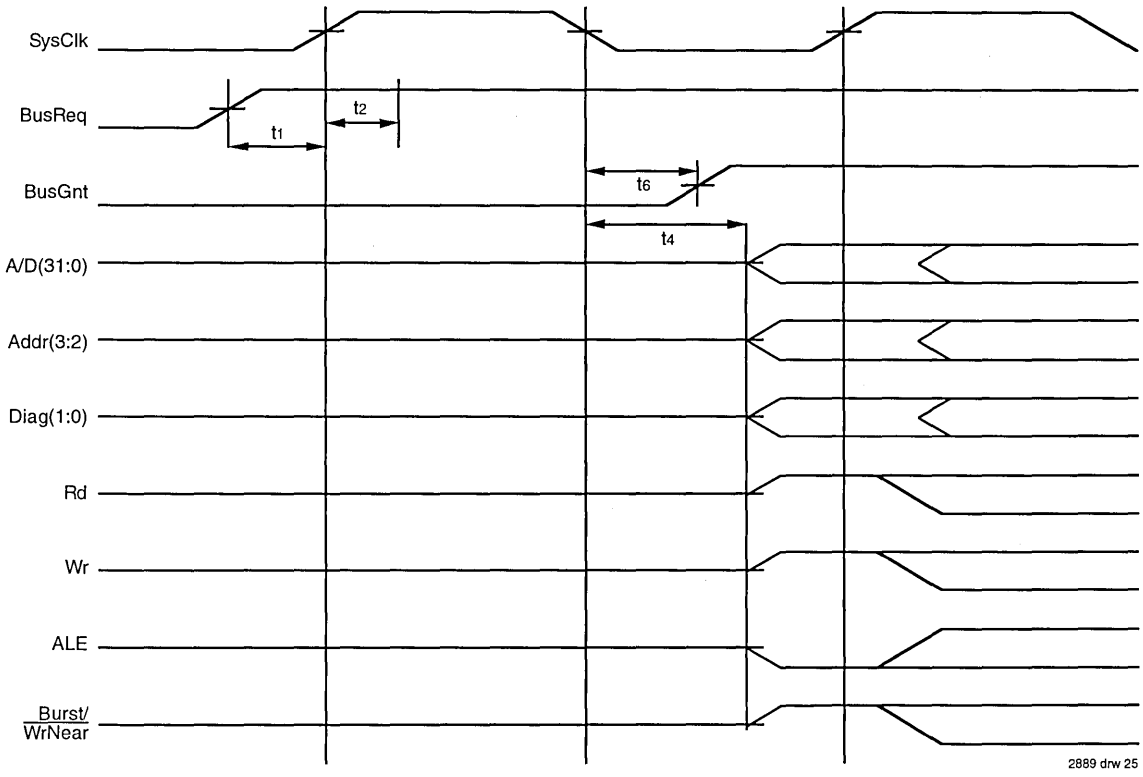


Figure 17. R3081 Regaining Bus Mastership

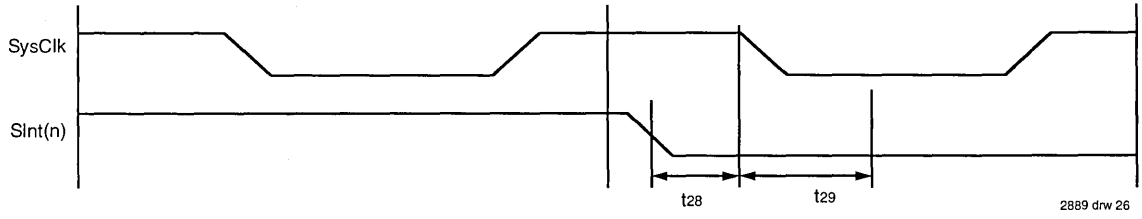


Figure 18. Synchronized Interrupt Input Timing

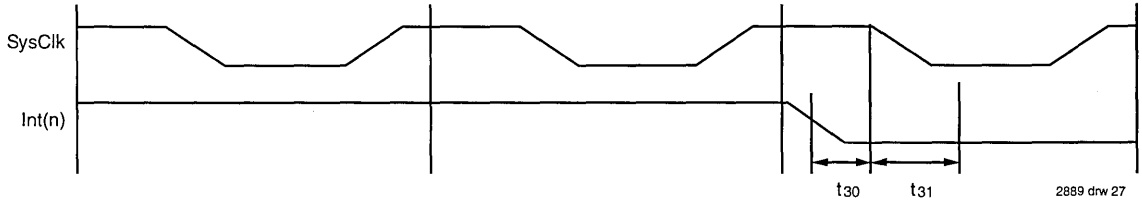


Figure 19. Direct Interrupt Input Timing

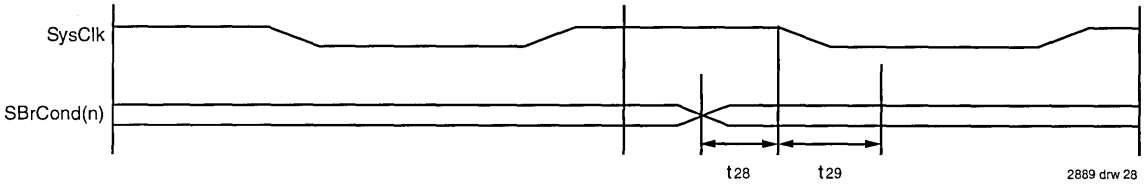


Figure 20. Synchronized Branch Condition Input Timing

Figure 21. Direct Branch Condition Input Timing

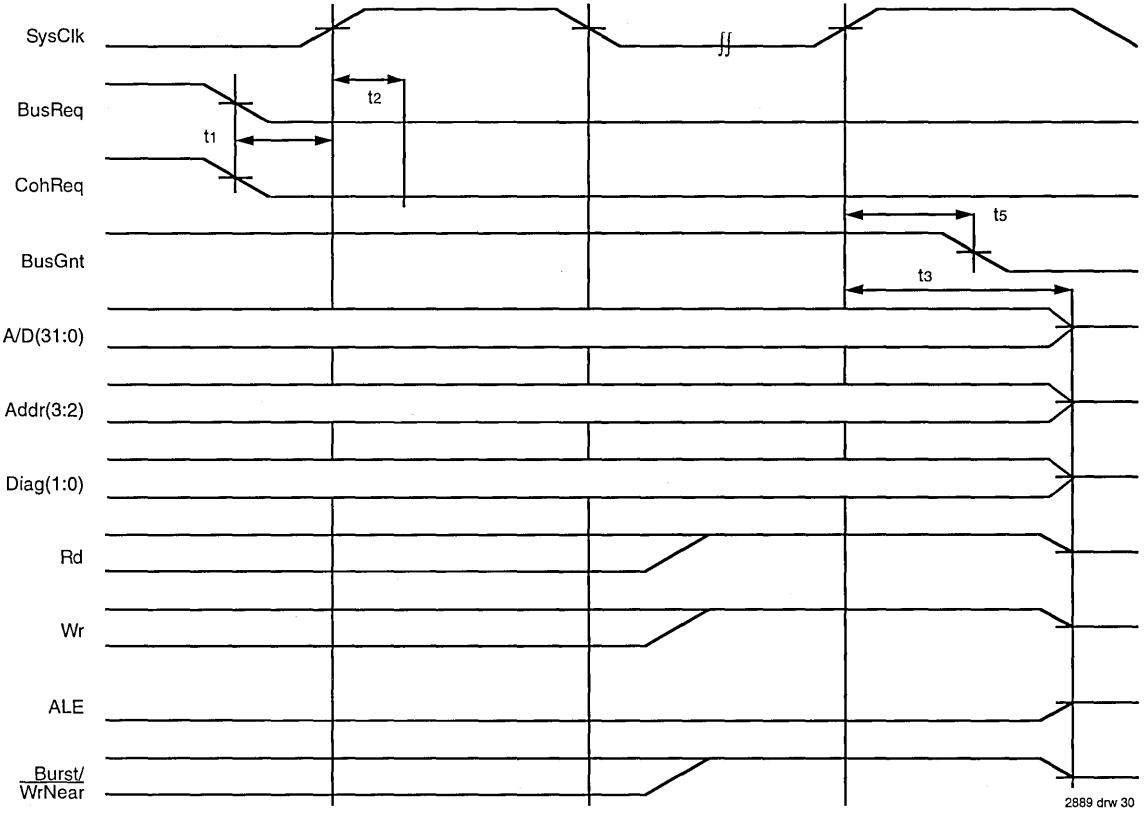


Figure 22. Coherent DMA Request

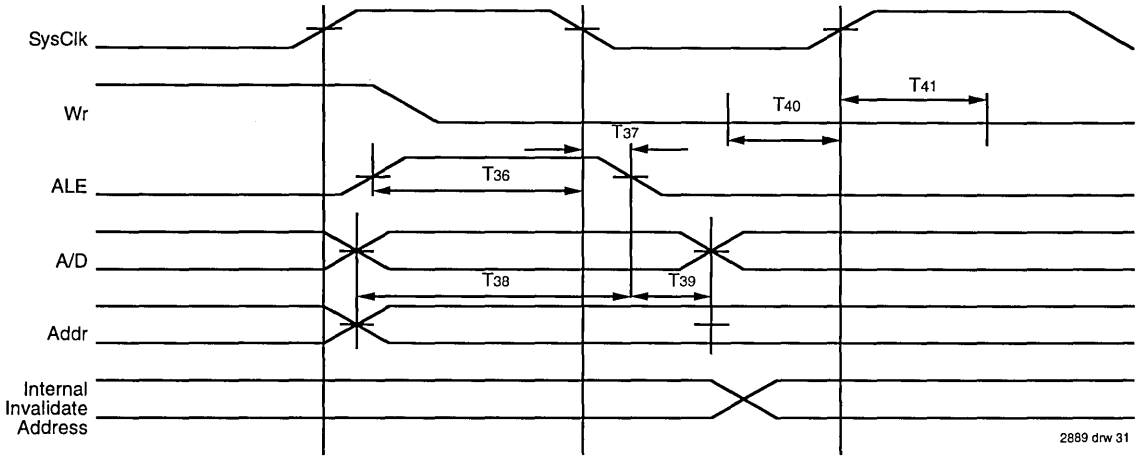


Figure 23. Beginning of Coherent DMA Write

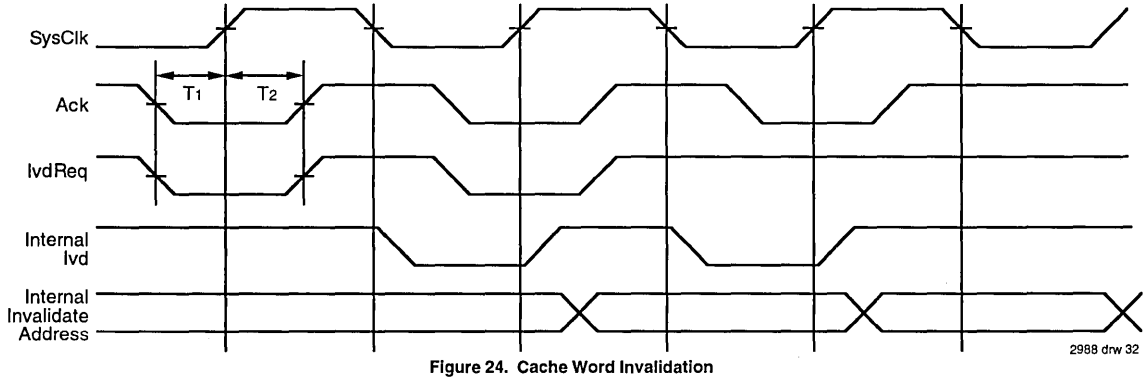


Figure 24. Cache Word Invalidation

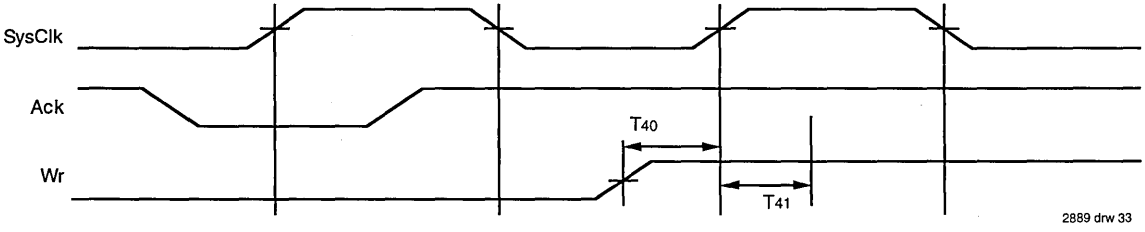


Figure 25. End of Coherent Write

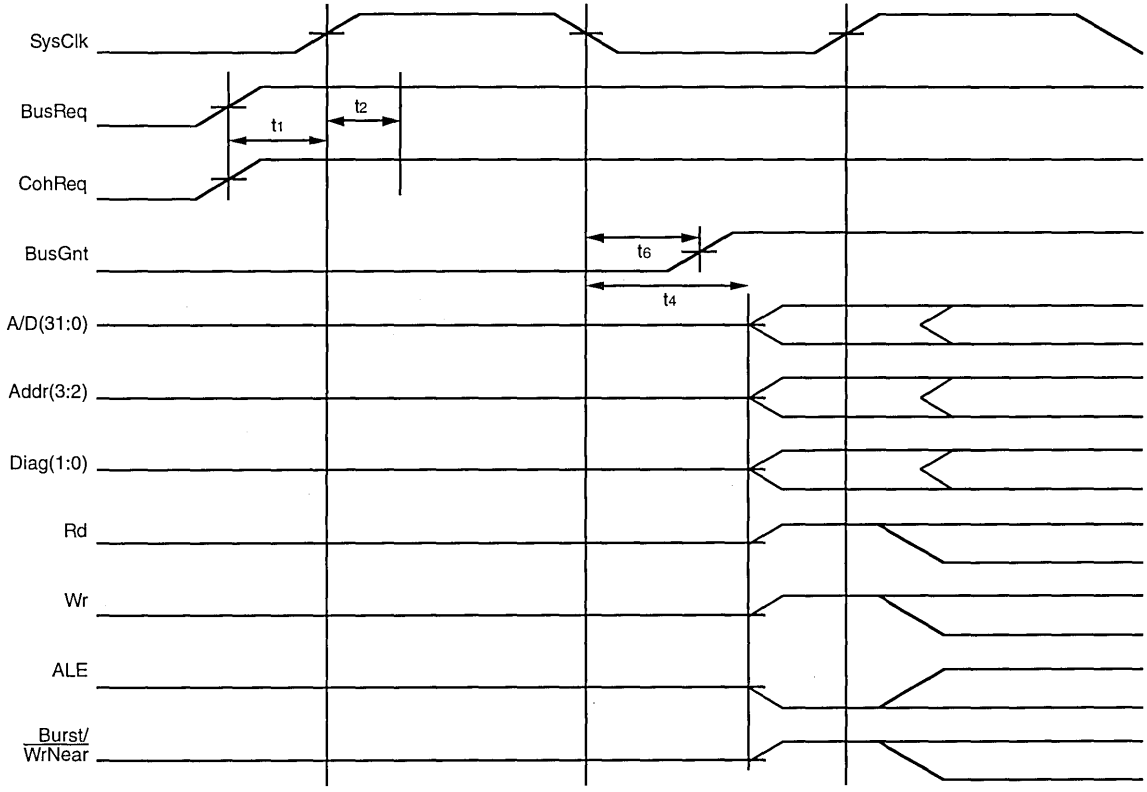
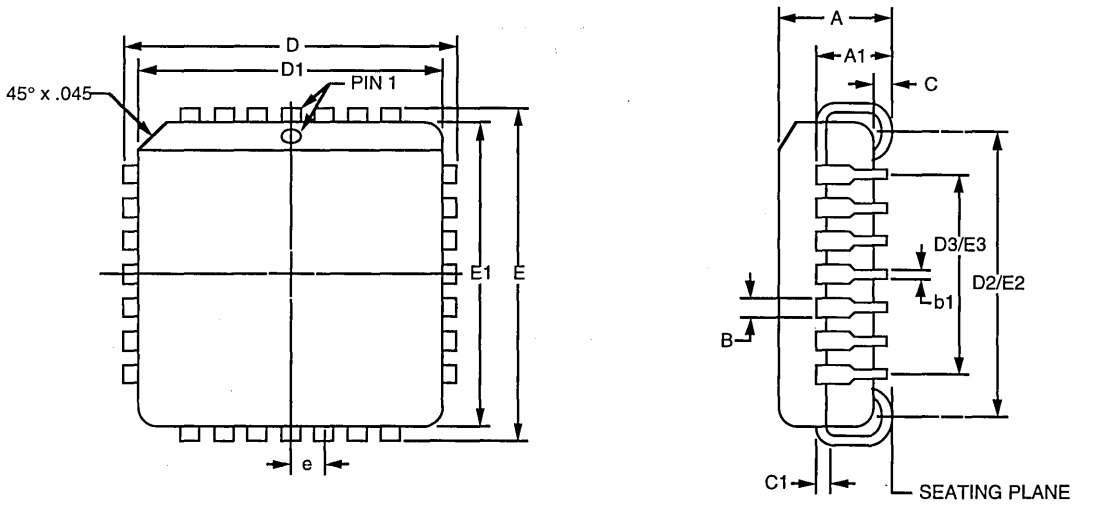


Figure 26. End of Coherent DMA Request

84 LEAD PLCC/MQUAD[7] (SQUARE)



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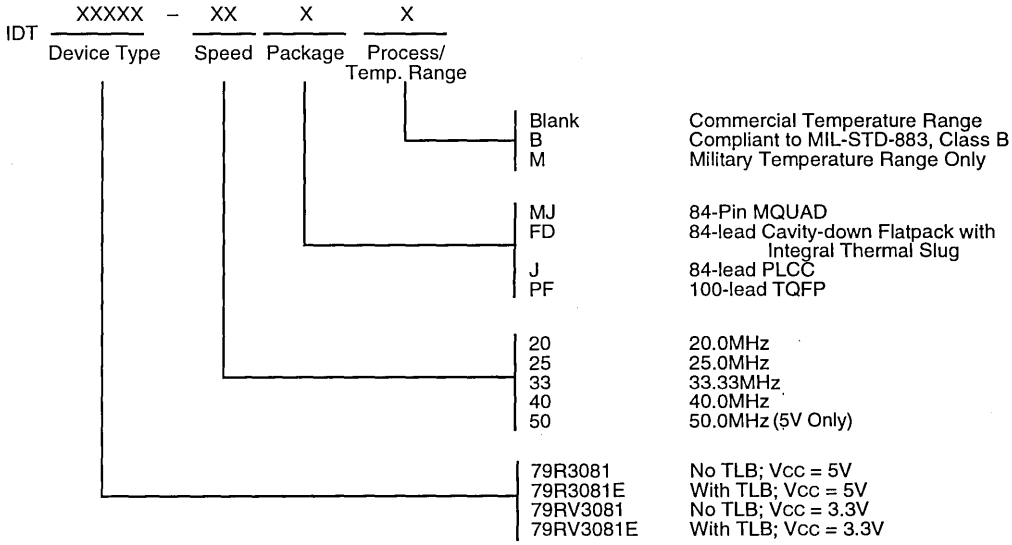
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004 inches at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. MQUAD is pin & form compatible with PLCC.

DWG #	J84-1		MJ84-1	
# of Leads	84		84	
Symbol	Min.	Max.	Min.	Max.
A	165	.180	165	.180
A1	.095	.115	.094	.114
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.020	.040	.020	.040
C1	.008	.012	.008	.012
D	1.185	1.195	1.185	1.195
D1	1.150	1.156	1.140	1.150
D2/E2	1.090	1.130	1.090	1.130
D3/E3	1.000 REF		1.000 REF	
E	1.185	1.195	1.185	1.195
E1	1.150	1.156	1.140	1.150
e	.050 BSC		.050 BSC	
ND/NE	21		21	

ORDERING INFORMATION



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VALID COMBINATIONS

IDT	79R3081 (E) – 20, 25, 33, 40, 50	MJ Package
	79RV3081 (E) – 20, 25, 33	PF Package
	79RV3081(E) – 20, 25, 33, 40	MJ Package
	79R3081E – 20, 25 (FDB/FDM)	FD Package Only

Integrated Device Technology, Inc.

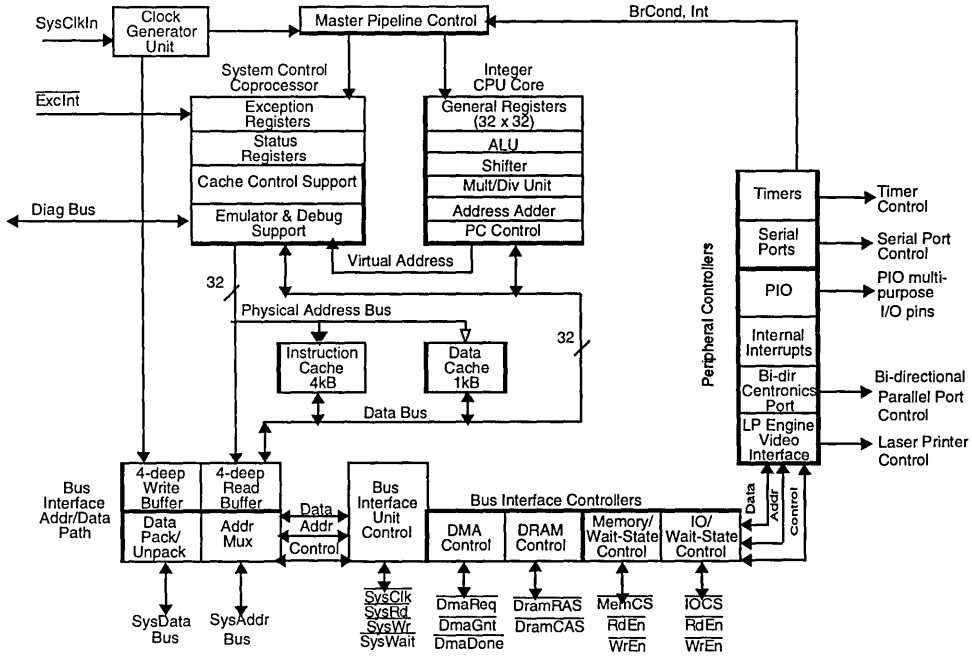
IDT79R36100™ HIGHLY INTEGRATED RISController™

IDT79R36100™ Advanced Information

FEATURES

- Instruction set compatible with the IDT RISController Family MIPS RISC CPUs
- System-level integration minimizes system cost
  - 32-bit RISC CPU
  - 4KB instruction cache on-chip
  - 1KB data cache on-chip
  - Memory, DMA and I/O controllers
  - System peripherals
- 24 MIPS/ 42K Dhrystone-2.1 at 25 MHz
- Improved cache control and cache locking
- Flexible bus interface allows simple, low cost designs
  - De-multiplexed address bus and data bus
  - On-chip 4-deep Read/Write buffer
  - Programmable bus width (8-,16-, and 32-bit)
- On-chip DRAM controller with Address Multiplexer
  - Supports optional interleaved DRAMs
- On-chip memory and I/O controller
  - Chip selects, wait-state generator
  - Supports optional interleaved ROMs
  - Supports PCMCIA Master protocol
- On-chip DMA controller
  - 4 internal channels, 2 external channels
- On-chip bi-directional IEEE 1284 Centronics™ Parallel Port interface
- On-chip laser printer video raster engine interface
- Built-in debug/emulator support
- 3.3V and 5V versions, MQUAD-208 packaging
- Supports interrupt steering to internal DMA
- On-chip dual-channel serial communications controller
- On-chip timers and interrupt controller

BLOCK DIAGRAM



DESCRIPTION

The IDT79R36100 is a highly integrated member of the IDT RISController family. The R36100 implements a "system on a chip" including the CPU core, cache memory, system logic functions and application specific peripherals. The 36100 is well-suited to a wide variety of very cost sensitive and board space constrained embedded applications. The high level of integration also greatly reduces the system design challenge, substantially reducing design risk and time to market.

The R36100 RISController is based upon the general purpose R3000A MIPS RISC CPU core and integrates substantial amounts of on-chip instruction cache and data cache memory. In addition to the CPU core and cache memory, the R36100 integrates all necessary system logic functions on-chip, including DRAM, ROM, I/O and DMA controllers; counter/timers; interrupt controllers; general purpose parallel I/O and debug support circuitry. The R36100 also integrates printer and data communication peripherals including an IEEE 1284 parallel port, laser printer video rasterizer, and two serial communications ports.

The R36100 RISController is software compatible with all members of the IDT RISController family, including the family of low-cost 32-bit R30xx RISControllers and the Orion family of high-performance 64-bit embedded controllers. The common instruction set architecture (ISA) enables the same applications software to be used across a wide variety of price/performance points.

The R36100 RISController has four on-chip bus controllers allowing seamless interfaces with a wide variety of standard memories and peripherals, including:

- Standard page mode DRAMs
- EPROMs, FLASH, SRAM, Dual-Port SRAM
- FIFOs, SCSI, A/D, and other I/O peripherals
- Ethernet, data compression, and other coprocessors

The R36100 RISController integrates an IEEE 1284 parallel port, RS-232C and Local Talk serial ports, and a laser printer video rasterizer to serve printer system applications, including:

- monochrome laser and ink-jet printers
- host-based printer cards
- multi-function laser/fax printer systems

In addition, the R36100 RISController integrates asynchronous and synchronous serial controller channels and multiple timers to serve data communications applications, such as:

- Local Area Network (LAN) interface cards
- CSU/DSU SDLC/HDLC line driver cards
- Router, switcher, and data compression cards

Device Overview

The R36100 RISController shown in the figure on page 1 is a block level representation of the functional units. The R36100 can be viewed as a "system on a chip"—the embodiment of a discrete system built around the R3000A CPU. By integrating the system functionality onto a single chip, dramatic cost, size, and power reductions are achieved. Thus the overall system complexity is reduced and system development time is minimized.

CPU Core

The R36100 RISController is based on the R3000A CPU core. The R3000A is a full 32-bit RISC integer execution engine, capable of sustaining a peak single cycle execution rate by using its five-stage pipeline. The CPU core contains an integer ALU unit and bit shifter with a separate integer multiplier/divider unit, address adder and program counter generator, and 32 orthogonal 32-bit registers. The R36100 execution core implements the MIPS-I instruction set architecture (ISA). Thus, the R36100 is binary compatible with all other MIPS CPU engines, including the low-cost R30xx family and the high-speed R4600 Orion family.

System Control Co-Processor

The R36100 RISController also integrates a System Control Co-processor (CPO) on chip. CP0 manages the exception handling capability of the R36100, the virtual to physical address memory mapping of the R36100, and the various programmable bus-to-cache interface capabilities of the R36100. These topics are discussed in the *Hardware User's Manual.*

The R36100 does not include the optional TLB found in other members of the IDT RISController family, but instead performs the same virtual to physical address mapping of the Base Versions of the R30xx family. These Base Version devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler operating system software model and a lower cost processor.

Clock Generator Unit

The R36100 RISController is driven from a single, double frequency input clock. An on-chip clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line that was required in discrete R3000A based systems.

Instruction Cache

The R36100 RISController integrates 4kB of on-chip instruction cache, which is organized with a line size of 16 bytes (four 32-bit entries). This relatively large cache substantially contributes to the high performance inherent in the R36100, and allows systems based on the R36100 to achieve high performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The

cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switches.

The R36100 instruction cache supports a cache locking mechanism to improve real-time performance. Each cache can be split into two halves or four quarters, each half or quarter servicing a different area of the large address space. This enables the system software to "lock" time-critical code (e.g., router address hash-table lookup algorithms and interrupt service routines), into one of the halves or quarters, and allow other tasks to utilize the other half or quarters without disrupting the locked-time critical code. This technique allows software to perform instruction cache locking, which ensures deterministic response.

Data Cache

The R36100 RISController incorporates an on-chip data cache of 1kB, which is organized as a line size of 4 bytes (one word). This relatively large data cache contributes substantially to the high performance inherent in the R36100. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache to insure that main memory is always consistent and coherent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer that captures address and data at the processor execution rate. This allows the data to be retired to main memory at a much slower rate without impacting the performance of the internal CPU pipeline.

The R36100 supports data cache locking with the same mechanism as the instruction cache. The 36100 allows the data cache to be split into two halves or quarters, each half or quarter servicing a different area of the large address space. This enables the system software to "lock" time-critical data (e.g., routing address information tables and the interrupt stack) into one of the halves or quarters, and allows other tasks to utilize the other half or quarter without disrupting the critical data. This technique allows software to perform data cache locking without requiring memory management support.

Bus Interface Unit

The R36100 RISController uses its large internal caches to provide the majority of its memory bandwidth requirements to/from the execution engine. The execution engine pipeline can access both one instruction and one data load/store per clock cycle. Only on the relatively rare cache miss or on writes does the R36100 require access to main memory. Thus, the R36100 can utilize a simple bus interface that connects to slow memory devices without sacrificing performance.

The R36100 bus interface utilizes a de-multiplexed address and data bus. This interface readily connects to memory subsystems that are 8-, 16-, or 32-bits wide, and/or interleaved.

The R36100 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture the processor's address and data information during internal store operations and process as FIFO at a rate of up to one per clock. The write buffer then presents the bus interface write transactions at the rate the memory system can accommodate.

During main memory writes, the R36100 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software that initiated the store. This insures that the same software can run across multiple platfoms having differing memory system configurations.

The R36100 read interface performs both single datum reads and quad word reads. In order to accommodate slower reads, the R36100 incorporates a 4-deep read buffer FIFO, so that the external interface can queue data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R36100 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, which simplifies migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, the R36100 easily supports the use of 8-, 16-, 32-bit, or interleaved boot PROMs.

Memory Controller

The R36100 RISController uses the on-chip memory controller to gluelessly attach external ROM (including FLASH) and/or SRAM, in a number of system configurations. For example, the memory controller supports interleaved ROM and/or SRAM, 8-bit boot ROM, 32-bit burst ROMs, as well as a simple 32-bit wide EPROM array. The memory controller integrates all of the control signals as well as managing the access timing and wait-state generation for multiple banks, all under the control of boot software.

DRAM Controller

The R36100 RISController integrates an on-chip DRAM controller. The DRAM controller directly controls up to four banks of standard page mode DRAMs in a number of configurations, including systems with varying densities of DRAM, 32-bit wide, interleaved DRAM, and 16-bit wide DRAM subsystems.

I/O Controller

The R36100 RISController has an on-chip I/O controller that performs all necessary address decoding and wait-state generation for external I/O devices. In addition, the on-chip I/O controller readily interfaces as a master to PCMCIA, including support of the large address space required and the PCMCIA chip-select protocol and timing.

DMA Control

The R36100 RISController provides on-chip DMA control for internal peripherals, external peripherals, and external memory. Multiple internal channels allow block moves of data between any combination of memory and I/O. Each channel can also be interrupt controlled, which allows an I/O peripheral like the serial port to regulate the individual transactions of a block move.

The R36100 RISController also supports external DMA masters, which take over the external system bus via a bus request and grant handshake. Once in control of the system bus, the external DMA master can read and write to memory, I/O, and internal peripherals via the R36100's bus controllers.

Counter/Timers

The R36100 RISController contains 3 general purpose timers. Each timer consists of a 16-bit count register as well as a 16-bit compare register. The count register resets to 0 and then counts upward until it equals the compare register. When the count register equals the compare register, the TCN output is asserted and the count is reset back to 0. In order to support intervals longer than 2^{16} ticks, the timers use a common 16-bit prescaler counter. Each timer is programmable to select a power-of-2 divisor of the prescaler. Using these features, each timer can be used as a general purpose real-time clock, bus timeout timer, watch dog timer, PWM/square wave/baud rate generator or gated clock external event counter.

PIO Interface

The R36100 RISController has a Parallel Input/Output (PIO) interface for controlling multi-purpose utility pins. The PIO pins can be programmed to act as general purpose inputs or outputs. Each PIO pin is also multiplexed with other controllers' inputs or outputs. This flexible arrangement allows system designers to customize the R36100 resources according to their needs. Thus, designs needing a special purpose controller--such as the laser printer video controller--can allocate the laser printer video pins for that purpose. Other applications, such as Datacom, which do not need the laser printer video, can use those pins for general purpose inputs or outputs.

Serial Communications Controller

The R36100 RISController integrates a dual channel serial port. This peripheral controller can perform a variety of synchronous and asynchronous protocols, including RS-232C, LocalTalk, SDLC, and HDLC. To maximize throughput, the on-chip serial port is optionally serviced by the auto-initiated on-chip DMA controller which can automatically block move data to and from the port.

Interrupt Controller

The R36100 RISController integrates an on-chip interrupt controller to manage both external interrupts and interrupts signaled from the on-chip peripherals. The interrupt controller improves internal interrupt servicing speed and assists in interrupt prioritization and nesting, as well as interfacing with the auto-initiated DMA.

IEEE 1284 Bi-directional Parallel Port

The R36100 RISController includes an internal IEEE1284 parallel port peripheral, which implements a true bi-directional port. Features include:

- 8-bit input Target Compatible protocol (for backward compatibility with legacy PCs)
- nibble and byte mode output protocol (for backward compatibility with most PCs)
- ECP protocol (for the emerging Laser Printer PC standard)
- EPP protocol (for datacom applications)
- External transceiver interface control pins
- Auto-initiated DMA via internal interrupts

Laser Printer Video Interface

The R36100 RISController integrates an on-chip laser printer video/control interface. This peripheral provides support for the following:

- 1-bit serial stream laser printer or raster engine interface
- On-chip FIFO
- Programmable margin widths and page lengths
- Auto-initiated DMA via internal interrupts

5

Performance Overview

The R36100 RISController achieves a very high-level of performance. This performance is due to the following features:

- An efficient execution engine. The CPU performs ALU operations and store operations in a single cycle, has an effective load time of 1.3 cycles and branch execution rate of 1.5 cycles based on the ability of the compilers to avoid software interlocks. Thus, the R36100 achieves over 24 dhrystone MIPS performance at 25MHz.
- Large on-chip caches. The R36100 contains caches that are substantially larger than most embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the R36100 to achieve actual sustained performance that is very close to its peak execution rate, even with low cost memory systems.
- Autonomous multiply and divide operations. The R36100 features an on-chip integer multiplier/divide unit that is separate from the other ALU. This allows the R36100 to perform multiply or divide operations in parallel with other integer operations by using a single multiply or divide instruction rather than "step" operations.
- Integrated write buffer. The R36100 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires them to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support. The R36100 enables the system designer to utilize page, static, or nibble mode RAMs when performing read operations. This minimizes the main memory read penalty and increase the effective cache hit rates.
- Tightly coupled memory system. System resources can be accessed and managed efficiently for the needs of the execution core when memory controllers are integrated on-chip.

Selectable Features

Boot-time selectable features are:8/16 or 32-bit PROM support and Big/Little Endian selection. Other selectable, register-configurable features are:

- Number of wait states for different memory and I/O controllers
- Memory and I/O map configuration
- 16 or 32-bit DRAM and 8/16 or 32-bit memory and I/O
- Interleaved or non interleaved memory/DRAM
- Programmable control signals timing for all controllers
- Selectable PIO
- Selectable transceivers type for all controllers (FCT 260/FCT245/FCT543)
- Selectable I/O style (Motorola/Intel/PCMCIA)

Development Support

The R36100 is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis and emulator tools, and sub-system modules.

Figure 1 is an overview of the system development process typically used when developing R36100 applications. The R36100 family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for R36100 based applications, and include tools such as the following:

- IDT/c compiler, based on the GCC/GNU tool chain.
- Cross development tools, available for a variety of development environments.
- High-performance IDT floating point emulation library software.
- IDT Evaluation Boards, which include RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT laser printer system boards, which directly drive a low-cost print engine.
- Adobe PostScript Page Description Language running on the IDT R3051 family.
- IDT/sim PROM Monitor, which implements a full PROM monitor, including diagnostics, remote debug support, and peek/poke.
- IDT/kit™ (Kernel Integration Toolkit), which provides library support and a framework for the system runtime environment.
- Logic analyzer and in-circuit emulator support for fast debugging and hardware/software integration.

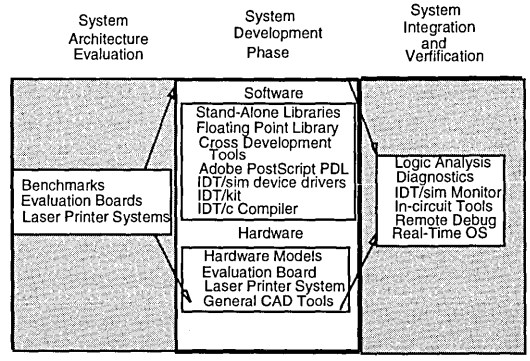


Figure 1. Development Support

System Usage

The IDT R36100 RISController is specifically designed to easily implement low-cost memory systems. Typical low-cost memory systems use EPROMs, DRAMs, as well as application specific peripherals. Some embedded systems also optionally contain or substitute DRAM with static RAMs.

Figure 2 demonstrates the low-system cost inherent in the R36100. In this example system, which is typical of a low-cost laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. Other embedded systems could optionally use an 8-bit or a 16-bit PROM, or even an interleaved 64-bit interface. A 16-bit font cartridge interface is provided through PCMCIA for add-in cards and a 32-bit page buffer DRAM is used for high-resolution.

In this example, a field or manufacturing upgrade to a larger page buffer is supported by the boot software and DRAM controller. Such a system features a very low entry price, with a range of field upgrade options. Note that the performance of the R36100 allows software frame buffer compression to be effective in reducing system DRAM while maintaining expected performance.

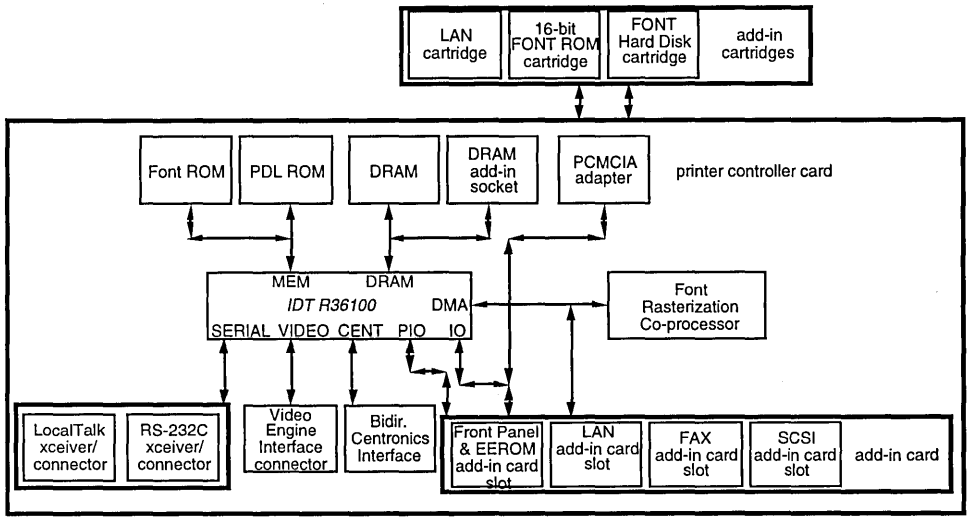


Figure 2. R36100-based Printer System

Pin Description

The following is a list of interface, interrupt, and miscellaneous pins available on the R36100. Pins marked with one asterisk are active when low.

Pin Name	Type	Description
System Bus Interface:		
SysAddr(25:0)	Output	System Address Bus. Also serves as the DramAddr(13:2) Bus.
SysData(31:0)	Input/Output	System Data Bus.
SysClkInInput	Input	System Clock Input. Twice (2x) the internal CPU frequency.
SysClk	Output	System Clock Output. All other outputs are referenced to this system clock.
SysReset	Input	System Reset. Initializes entire chip, except for JTAG circuitry.
SysWait	Input	System Way. Extends current bus transaction.
SysBusError	Input	System Bus Error. Terminates current bus transaction.
SysALEn	Out-put/Input(DMA)	System Address Latch Enable. Indicates valid address at the beginning of a bus transaction.
SysBurstFrame	Out-put/Input(DMA)	System Burst Frame. First indicates the beginning of a bus transaction. Then indicates if the bus transaction is a burst and if the next datum is the last datum.
SysData Rdy	Output	System Data Ready. Indicates valid data during each datum of a bus transaction (except when SysWait is asserted).
SysRd	Out-put/Input(DMA)	System Read. Indicates current bus transaction is a read.
SysWr	Out-put/Input(DMA)	System Write. Indicates current bus transaction is a write.
DRAM Controller Pins		
DramRAS(3:0)	Output	DRAM Row Address Strobe.
DramCAS(3:0)	Output	DRAM Column Address Strobe.
DramRDEnEven	Output	DRAM Read Enable for Even FCT245/543 Type Banks. On FCT260 type banks, it is the read enable for both.
DramRdEnOdd	Output	DRAM Read Enable for Odd FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
DramWrEnEven	Output	DRAM Write Enable for Even Banks.
DramWrEnOdd	Output	DRAM Write Enable for Odd Banks.

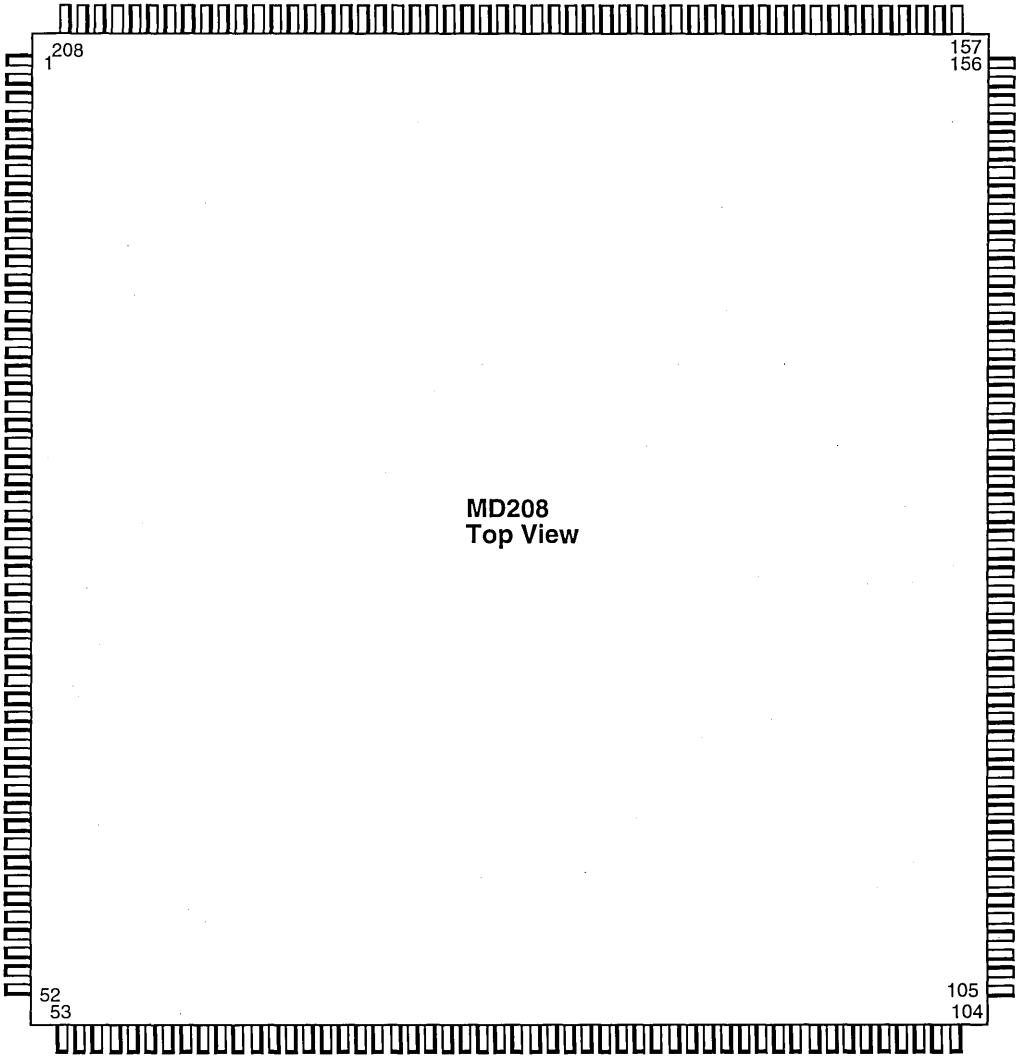
Pin Name	Type	Description
Memory Controller:		
MemCS/IoCS(7:0)	Output	Memory or I/O Chip Selects. MemCS(0) and optionally MemCS(1) are reserved for the Boot PROM. IoCS(6) and/or IoCS(7) are optionally reserved for the Centronics Port if used.
MemRdEnEven	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type banks, it is the read enable for both even and odd banks.
MemRdEnOdd	Output	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
MemWrEn(3:0)	Output	Memory Write Enable for each byte lane.
IoRdEn/DStrobe	Output	I/O Read Enable or I/O Data Strobe.
IoWrEn/RdWr	Output	I/O Write Enable or I/O Read/Write.
DMA Controller:		
DmaBusGnt(1:0)	Output	DMA Bus Grant Indicates that the CPU has tri-stated the bus and other DMA related signals.
DmaBusReq(1:0)	Input	DMA Bus Request. Indicates that external DMA agent would like control of the bus and other DMA related signals.
DmaDone	Input/Output	DMA transaction done
Serial Port Pins:		
SerialPClkIn(1:0)	Input	Optional Prim ary Serial Clock Input.
SerialSClk(1:0)	Input/Output	Optional Secondary Serial Clock Input or Output.
SerialRxData(1:0)	Input	Serial Receiver Data Stream.
SerialTxData(1:0)	Output	Serial Transmitter Data Stream.
SerialCTS(1:0)	Input	Serial Clear To Send.
SerialRTS(1:0)	Output	Serial Request To Send.
Serial Sync(1:0)	Input/Output	Serial Frame Sync.
Serial DCD(1:0)	Input	Serial Data Carrier Detect.
SerialDTR(1:0)	Output	Serial Data Terminal Ready.
Timer:		
TimerTC(2:0) /TimerGate(2:0)	Input/Output	Timer Terminal count output or Timer Count Gate Enable input. Terminal count asserts when Timer Count equals 0. Timer Gate enables counter to count upward or to stop.
PIO:		
PIO(31:0)	Input/Output	Parallel inputs or Parallel Outputs. Parallel inputs and parallel outputs are multiplexed with various peripheral inputs and peripheral outputs. If the peripheral is unused, the input or output pin can be reconfigured to be a general purpose input or output, respectively.

Pin Name	Type	Description
Bi-Directional Centronics Interface:		
CentStrobe	Input	Centronics Strobe. In compatible mode, strobes data into the printer. Has other uses for other modes.
CentAck	Output	Centronics Acknowledge. In compatible mode, acknowledges a strobe. Has other uses for other modes.
CentBusy	Output	Centronics Busy. In compatible mode, delays the host from sending more data. Has other uses for other modes.
CentPaperError	Output	Centronics Paper Out/Jam Error. In Compatible mode, indicates that the printer has a paper error when asserted with CentFault. Has other uses for other modes.
CentSelect	Output	Centronics Select. In Compatible mode, used to indicate that this printer is on-line. Has other uses for other modes.
CentAutoFeed	Input	Centronics Auto Page Feed. In compatible mode, sends a paper feed to the printer. Has other uses for other modes.
CentInit	Input	Centronics Initialization/Reset. In Compatible mode, resets the printer. Has other uses for other modes.
CentFault	Output	Centronics Fault. In Compatible mode, indicates that the printer has a problem. Has other uses for other modes.
CentSelectIn	Input	Centronics Select In. In Compatible mode, indicates that the Host wants to select this printer on a shared cable. Has other uses for other modes
CentHostStrobe	Output	Centronics Host Strobe. Used to latch Host data on the external FCT952/374 data transceiver during a Host write.
CentHostOEn	Output	Centronics Host Output Enable. Used to enable the external FCT952/374 data transceiver during a Host read.
Laser Engine Interface:		
LaserVideoData	Output	Laser Video Data Stream.
LaserVideoClkIn	Input	Laser Video Clock Input. Accepts either the (1x) Video Data Stream frequency or 8 times (8x) the PLL frequency.
LaserLineSync	Input	Laser Line Sync. Indicates that the laser drum is ready to start accepting data for a new line.
LaserPageSync	Input	Laser Page Sync. Indicates that the laser drum is ready to start a new page.
Debug/Emulator Interface:		
JtagClkIn	Input	JTAG Clock Input (TCK). Test mode serial boundary scan input clock.

Pin Name	Type	Description
Debug/Emulator Interface:		
JtagModeSelect	Input	JTAG Mode Select (TSEL). Test mode serial boundary scan command data. In normal operating mode, JtagModeSelect should be left unasserted high.
JtagDataIn	Input	JTAG Data In (TDI). Test mode serial boundary scan register data input.
JtagDataOut	Output	JTAG Data Out (TDO). Test mode serial boundary scan register data output.
JtagReset	Input	TAG Reset (TRES*). Resets the JTAG test circuitry. Does not reset any other chip functions.In normal operating mode, JtagReset should be left asserted low.
Diagnostic Pins		
DiagC/UnC	Output	Diagnostic Cached versus Uncached. On read bus transactions indicates whether the read is cached or uncached.
DiagInst/Data	Output	Diagnostic Instruction versus Data. On read bus transactions indicates whether the read is for instructions or data.
DiagRun	Output	Diagnostic Run. Indicates an internal pipeline run cycle. This pin has iso-synchronous timing.
DiagBranchTaken	Output	DiagBranchTaken Indicates that a branch, jump, or exception has been taken. This pin has asynchronous timing.
DiagJRorExe	Output	Diagnostic Jump Register or Exception occurring. Indicates that a jump register or exception is executing. This pin has asynchronous timing.
DiagInternalWr	Output	Diagnostic Internal Write. Indicates that a MTCO to CP0 register $3 is occurring.
DiagInstCacheWr-Dis	Output	Diagnostic Cache Write Disable. Disables writes to the instruction and data cache. This pin has iso-synchronous timing and is not recommended for functional use.
DiagTriState	Input	Diagnostic Tri-State all outputs. All outputs are tri-stated including SysClk. This pin is asynchronous such that tri-stating asserts or de-asserts output enables immediately.
DiagFCM	Input	Diagnostic Force Cache Miss. This pin has iso-synchronous timing. If used for functional board tests, it is recommended that it be (de-)asserted statically at reset time and left (de-)asserted.
DiagIntDis	Input	Diagnostic Interrupt Disable.
DiagNoCS	Output	Diagnostic No Chip Select. No internal or external chip select has occurred for the current bus transaction, therefore an external state machine should handle the bus transaction.
DiagInternalDMA	Output	Diagnostic Internal DMA. Asserts whenever any of the Internal DMA channels is generating the current bus transaction.

Pin Name	Type	Description
Exception Handling:		
ExcSInt(2:0)	Input	Exception Synchronized Interrupts. Also used as the reset initialization vector for 2:Boot16, 1:Boot8, and 0:BigEndian modes.
ExcInt(4:3)	Input	Exception Interrupts.
ExcSBrCond(3:2)	Input	Exception Synchronized Branch Condition inputs.
Power/Ground:		
Vcc	Input	Power pin. All power pins must be connected. 5V or 3.3V depending on part type.
Gnd	Input	Ground pin (VSS). All ground pins must be connected. 0V.

Physical Specifications



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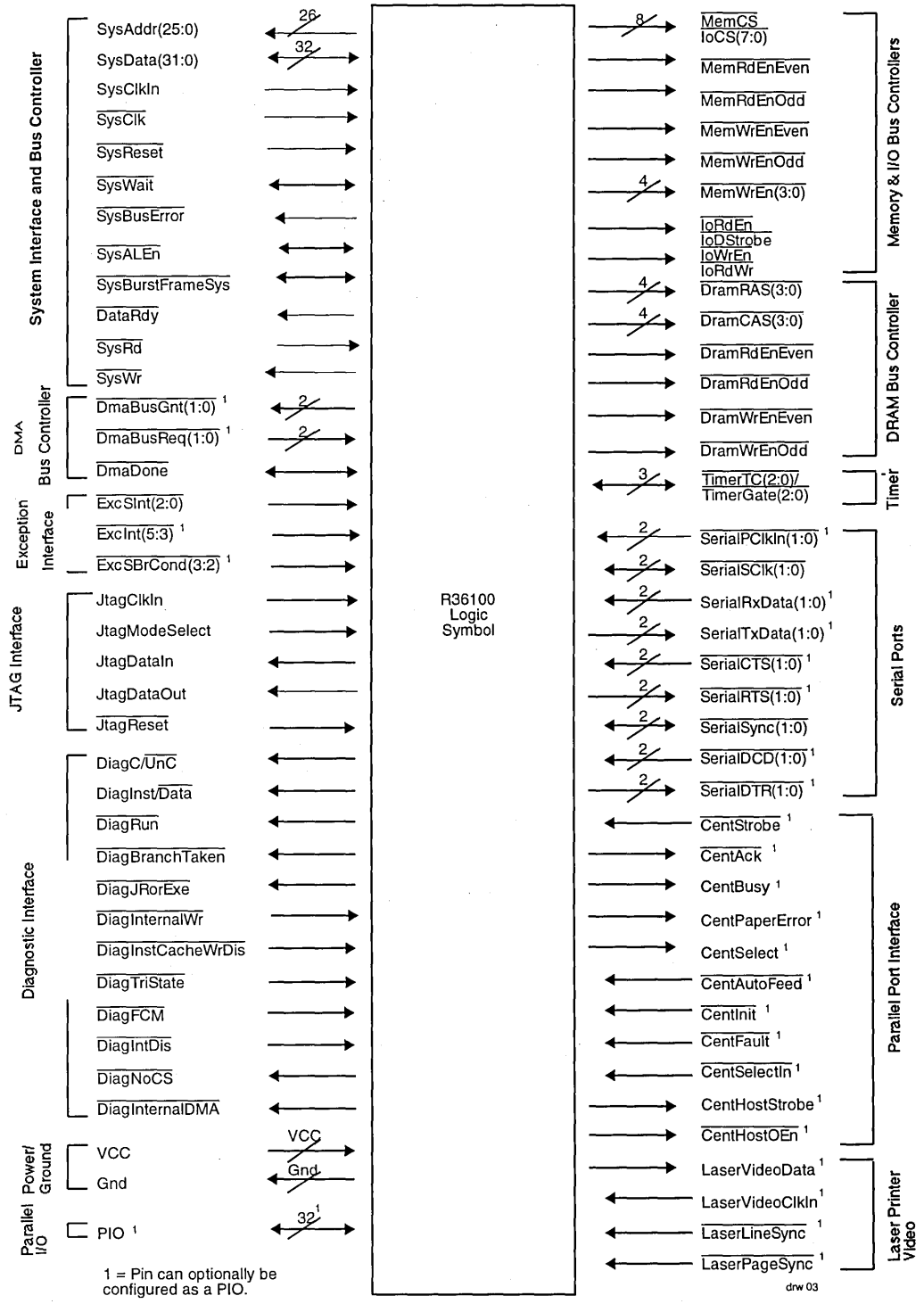
36100 Advance Pin-Out

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Test1N	53	JtagDataOut	105	N/C	157	SerialTxData(0)
2	SysAddr(0)	54	SysData(0)	106	DramRASN(2)	158	SerialCTSN(0)
3	SysAddr(1)	55	SysData(1)	107	DramRASN(3)	159	SerialRTSN(0)
4	DiagC_UnCN	56	SysData(2)	108	DramCASN(0)	160	SerialTxClkN(0)
5	SysAddr(2)	57	SysData(3)	109	DramCASN(1)	161	SerialSycnN(0)
6	vcc	58	vcc	110	vcc	162	vcc
7	vss	59	vss	111	vss	163	vss
8	SysAddr(3)	60	SysData(4)	112	DramCASN(2)	164	SerialDTRN(0)
9	SysAddr(4)	61	SysData(5)	113	DramCASN(3)	165	SerialDCDN(0)
10	DiagRunN	62	SysData(6)	114	DramRdEnEvenN	166	SerialClkInN(1)
11	DiagBranchTakenN	63	SysData(7)	115	DramRdEnOddN_TrN	167	SerialTxClkN(1)
12	DiagJRorExeN	64	SysData(8)	116	MemCSN_IoCSN(0)	168	SerialSyncN(1)
13	DiagInternalWrN	65	SysData(9)	117	MemCSN_IoCSN(1)	169	SerialRxData(1)
14	SysAddr(5)	66	SysData(10)	118	MemCSN_IoCSN(2)	170	SerialTxData(1)
15	SysAddr(6)	67	SysData(11)	119	MemCSN_IoCSN(3)	171	SerialCTSN(1)
16	vcc	68	vcc	120	vcc	172	vcc
17	vss	69	vss	121	vss	173	vss
18	SysAddr(7)	70	SysData(12)	122	MemCSN_IoCSN(4)	174	SerialRTSN(1)
19	SysAddr(8)	71	SysData(13)	123	MemCSN_IoCSN(5)	175	SerialDCDN(1)
20	DiagInst-CacheWrDisN	72	SysData(14)	124	MemCSN_IoCSN(6)	176	SerialDTRN(1)
21	DiagTriStateN	73	SysData(15)	125	MemCSN_IoCSN(7)	177	TimerTCN(0)
22	DiagFCMN	74	SysData(16)	126	MemRdEnEvenN	178	TimerTCN(1)
23	DiagIntDisN	75	SysData(17)	127	MemRdEnOddN	179	TimerTCN(2)
24	SysAddr(9)	76	SysData(18)	128	MemWrEnN(0)	180	CentStrobeN
25	SysAddr(10)	77	SysData(19)	129	MemWrEnN(1)	181	CentAckN
26	vcc	78	vcc	130	vcc	182	vcc
27	vss	79	vss	131	vss	183	vss
28	SysAddr(11)	80	SysData(20)	132	MemWrEnN(2)	184	CentBusy
29	SysAddr(12)	81	SysData(21)	133	MemWrEnN(3)	185	CentPaperError
30	DiagNoCSN	82	SysData(22)	134	IoRdEnN_DStrobeN	186	CentSelect
31	Diaginst_DataN	83	SysData(23)	135	IoWrEnN_RdWrN	187	CentAutoFeedN
32	SysAddr(13)	84	SysData(24)	136	N/C	188	CentInitN
33	SysAddr(14)	85	SysData(25)	137	N/C	189	CentFaultN
34	SysAddr(15)	86	SysData(26)	138	LaserVideoData	190	CentSelectInN
35	SysAddr(16)	87	SysData(27)	139	LaserVideoClk	191	CentHostStrobeN
36	vcc	88	vcc	140	vcc	192	vcc
37	vss	89	vss	141	vss	193	vss
38	SysAddr(17)	90	SysData(28)	142	LaserLineSyncN	194	CentHostOEnN
39	SysAddr(18)	91	SysData(29)	143	LaserPageSyncN	195	DmaBusGntN(0)
40	SysAddr(19)	92	SysData(30)	144	ExcSintN(0)	196	DmaBusGntN(1)
41	SysAddr(20)	93	SysData(31)	145	ExcSintN(1)	197	DmaBusReqN(0)
42	SysAddr(21)	94	SysClkIn	146	ExcSintN(2)	198	DmaBusReqN(1)
43	SysAddr(22)	95	SysResetN	147	ExcIntN(3)	199	DmaDoneN
44	SysAddr(23)	96	DramWrEvenN	148	ExcIntN(4)	200	SysAleN
45	SysAddr(24)	97	N/C	149	DiagIntDmaN	201	SysDataRdyN
46	vcc	98	vcc	150	vcc	202	vcc
47	vss	99	vss	151	vss	203	vss
48	SysAddr(25)	100	DramWrOddN	152	SysWaitN	204	SysRdN
49	JtagModeSelect	101	N/C	153	SysBusErrorN	205	SysWrN
50	JtagResetN	102	DramRASN(0)	154	SysClkN	206	SysBurstFrameN
51	JtagClkIn	103	DramRASN(1)	155	SerialClkInN(0)	207	ExcSBrCond(2)
52	JtagDataIn	104	Test0N	156	SerialRxData(0)	208	ExcSBrCond(3)


System Interface and Bus Controller
SysAddr(25:0)
SysData(31:0)
SysClkIn
SysClk
SysReset
SysWait
SysBusError
SysALEn
SysBurstFrameSys
DataRdy
SysRd
SysWr
DMA Bus Controller
DmaBusGnt(1:0) 1
DmaBusReq(1:0) 1
DmaDone
Exception Interface
ExcSInt(2:0)
ExcInt(5:3) 1
ExcSBrCond(3:2) 1
JTAG Interface
JtagClkIn
JtagModeSelect
JtagDataIn
JtagDataOut
JtagReset
Diagnostic Interface
DiagC/UnC
DiagInst/Data
DiagRun
DiagBranchTaken
DiagJRorExe
DiagInternalWr
DiagInstCacheWrDis
DiagTriState
DiagFCM
DiagIntDis
DiagNoCS
DiagInternalDMA
Parallel I/O Power/Ground
VCC
Gnd
PIO 1
1 = Pin can optionally be configured as a PIO.
R36100 Logic Symbol
Memory & I/O Bus Controllers
MemCS
IoCS(7:0)
MemRdEnEven
MemRdEnOdd
MemWrEnEven
MemWrEnOdd
MemWrEn(3:0)
IoRdEn
IoDStrobe
IoWrEn
IoRdWr
DRAM Bus Controller
DramRAS(3:0)
DramCAS(3:0)
DramRdEnEven
DramRdEnOdd
DramWrEnEven
DramWrEnOdd
Timer
TimerTC(2:0)/
TimerGate(2:0)
Serial Ports
SerialPClkIn(1:0) 1
SerialSClk(1:0)
SerialRxData(1:0) 1
SerialTxData(1:0) 1
SerialCTS(1:0) 1
SerialRTS(1:0) 1
SerialSync(1:0)
SerialDCD(1:0) 1
SerialDTR(1:0) 1
Parallel Port Interface
CentStrobe 1
CentAck 1
CentBusy 1
CentPaperError 1
CentSelect 1
CentAutoFeed 1
CentInit 1
CentFault 1
CentSelectIn 1
CentHostStrobe 1
CentHostOEn 1
Laser Printer Video
LaserVideoData 1
LaserVideoClkIn 1
LaserLineSync 1
LaserPageSync 1
drw 03

Integrated Device Technology, Inc.

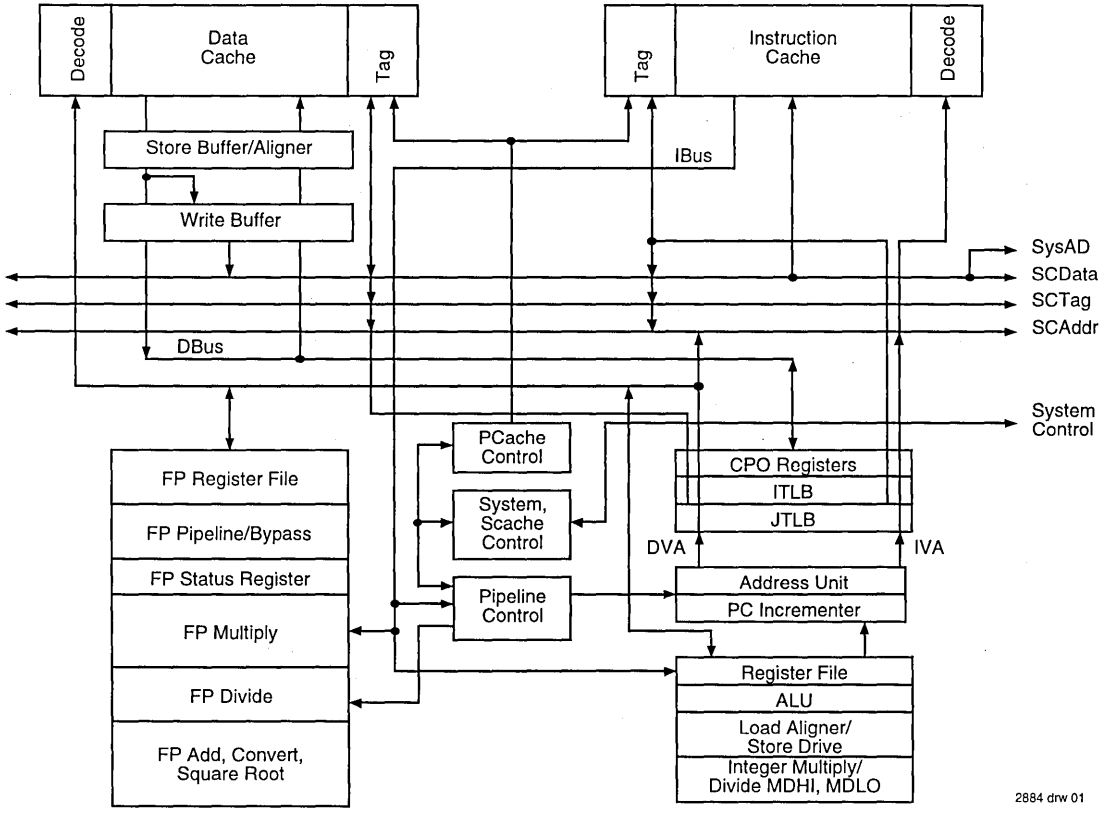
THIRD GENERATION 64-BIT SUPER-PIPELINED RISC MICROPROCESSOR

IDT79R4400™
IDT79RV4400

FEATURES:

- True 64-bit microprocessor
  - — 64-bit integer operations
  - — 64-bit floating-point operations
  - — 64-bit registers
  - — 64-bit virtual address space
- High-performance microprocessor
  - — Super-pipelined architecture supports 200MIPS at 100MHz
  - — No issue restrictions for dual instruction issue
- High level of integration
  - — 64-bit integer CPU
  - — 64-bit floating-point accelerator
  - — 16KB instruction; 16KB data cache
  - — Flexible MMU with large TLB
- Standard operating system support includes:
  - — Microsoft Windows™ NT
  - — UNISOFT UNIX™ System V.4
- Fully software compatible with R3000A 32-bit RISC Processor Family
- 50, 67, 75, 88 and 100MHz clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - — Desktop workstations
  - — Deskside or departmental servers
  - — High-performance embedded applications
  - — Tightly coupled multi-processing systems
  - — Fault tolerant systems
- R4400 for 5V operation and RV4400 for 3.3V operation

BLOCK DIAGRAM



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DESCRIPTION:

The IDT79R4400 family supports a wide variety of processor-based applications, from 32-bit ARC compliant desktop systems through high-performance, 64-bit OLTP systems manipulating large data bases in a multi-processor-based system. The IDT79R4400 products offer a broad range of price-performance options for high-performance systems, allowing the system architect unprecedented degrees of freedom in making price-performance tradeoffs.

The IDT R4400 products provide complete upward application-software compatibility with the IDT79R3000 family of microprocessors, including the IDT79R3000A and the IDT RISController™ family (IDT79R3051™ family). Microsoft Windows NT and UNISOFT UNIX V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4400-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The R4400 family achieves a unique balance between high-integer and high-floating-point performance. The key to this balance is the super-pipelined architecture of the processor, which brings performance gains to both integer and floating-point intensive programs without requiring recompilation to take advantage of the architectural advancement. The execution engine is assured of a rapid and continual supply of instructions and data through the use of large on-chip caches, and a high-performance on-chip TLB.

The R4400 family also provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4400 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit operating systems and applications.

The 64-bit computing and addressing capability of the R4400 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the IDT79R4400 CPU family. A more detailed description of the processor is available in the *"R4400 Hardware User's Manual"*. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

IDT79R4400 FAMILY MEMBERS

The IDT79R4400 processor is available in three different configurations: the IDT79R4400MC and IDT79R4400SC, which include a 128-bit wide secondary cache bus; and the IDT79R4400PC, with no secondary cache interface. All references to R4400 apply to R4400 (5V) and RV4400 (3.3V) operation.

PC CONFIGURATION

The IDT79R4400PC is available in a 179-pin Pin Grid Array (PGA). This configuration does not support secondary cache or cache coherency, and is ideal for applications such as high-performance embedded control and low-cost desktop systems, where the on-chip caches provide enough performance and where cost, power, and board space must be kept to a minimum. By eliminating a secondary cache, a system can be designed with fewer parts and lower power consumption.

SC CONFIGURATION

The 79R4400SC is available in a 447-pin Pin Grid Array (PGA). This processor supports a secondary cache interface and is ideal in systems where high performance is desired. This component supports a 128kB to 4mB secondary cache made from standard SRAMs. This flexibility allows system designers to make price/performance tradeoffs in cache subsystem designs.

MC CONFIGURATION

The IDT79R4400MC is also available in the 447-pin Pin Grid Array (PGA). This processor supports a secondary cache and configurable multiprocessor cache coherency protocols. Like the "SC" configuration, this processor also supports a 128kB to 4mB secondary cache made from standard SRAMs. The IDT79R4400MC is well suited for a range of designs from high performance desktop systems to fault tolerant multiprocessor servers.

5

HARDWARE OVERVIEW

The IDT R4400 processor brings a high-level of integration designed for high-performance computing. The key elements of the IDT R4400 are briefly described below. A more detailed description of each of these subsystems is available in other literature.

Superpipelined Implementation

In order to achieve the high-performance desired for today's applications and user's interfaces, the R4400 exploits instruction level parallelism using a superpipelined microarchitecture.

The R4400 uses an 8-stage superpipeline which places no issue restrictions on instruction issue. Thus, any two instructions can be issued each master clock cycle under normal circumstances, leading to 200MIPS performance at 100MHz. One key advantage of this architecture is that all existing applications can gain from the architectural advancement represented by the R4400, without requiring recompilation to reorder the software.

In order to support dual instruction issue, the internal pipeline of the R4400 operates at twice the external clock frequency. Instruction execution stages such as cache accesses are pipelined (thus the chip itself is super-pipelined) to eliminate bottlenecks associated with long-latency functional units. Other stages, such as the ALU stage, completely process one operation per pipeline clock cycle, allowing the results of one operation to be immediately used by the instruction which follows, with no pipeline interlocks.

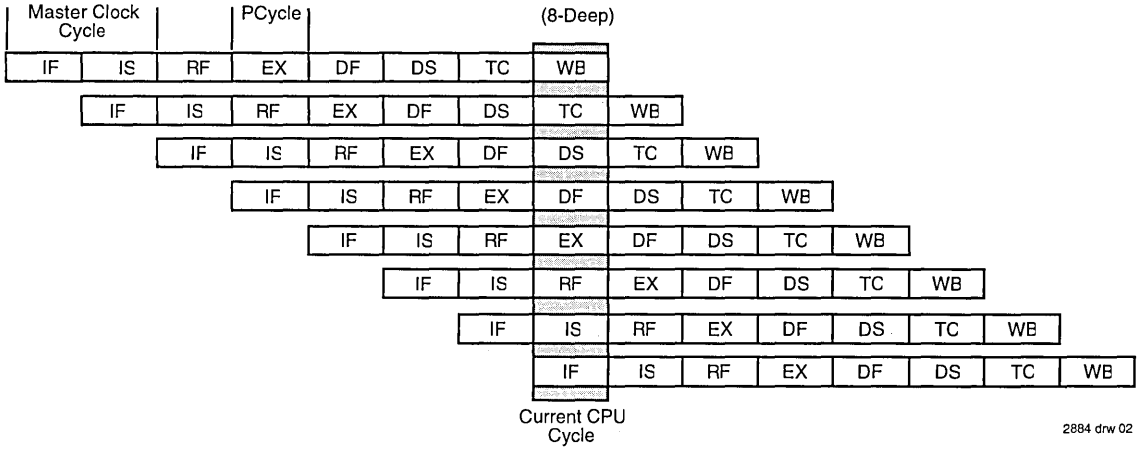
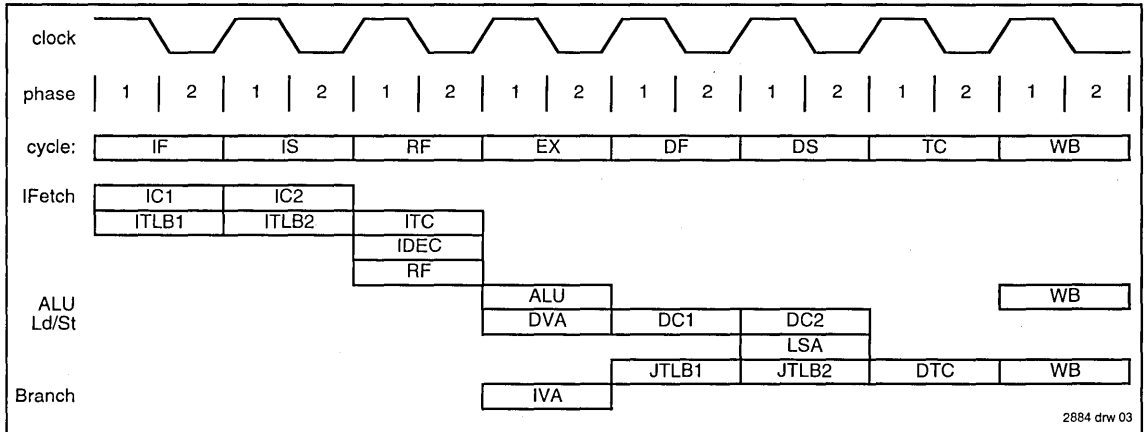


Figure 1. R4400 8-Stage Super-Pipeline



IC1	Instruction cache access stage 1
IC2	Instruction cache access stage 2
ITLB1	Instruction address translation stage 1
ITLB2	Instruction address translation stage 2
ITC	Instruction tag check
IDEC	Instruction decode
RF	Register operand fetch
ALU	Operation
DVA	Data virtual address calculation
DC1	Data cache access stage 1
DC2	Data cache access stage 2
LSA	Data load or store align
JTLB1	Data/Instruction address translation stage 1
JTLB2	Data/Instruction address translation stage 2
DTC	Data tag check
IVA	Instruction virtual address calculation
WB	Write-back to register file

Figure 2. Pipeline Activities

High clock frequency results from careful construction of the various resources of the processor: pipelining cache accesses, shortening register access times, implementing virtually indexed primary caches, and allowing the latency of functional units to span multiple pipeline stages.

After extensive simulation of many methods of exploiting instruction level parallelism, superpipelining was chosen because it improves integer performance commensurate with floating-point performance. Thus, the R4400 provides performance benefits both to technical computing applications, and also to a wide variety of commercial applications as well. In today's technology, superpipelining results in less complex logic, faster cycle times, quicker design cycles, and lower cost. The pipeline of the IDT79R4400 is illustrated in Figure 1.

THE R4400 PIPELINE

The R4400 processor has an eight-stage execution pipeline. That is, each instruction takes eight Pclock (Pipeline clocks, at twice the frequency of the input clock) cycles to execute, but a new instruction is started on each Pclock cycle. Another way of viewing the process is that, at any point in time, eight separate instructions are being executed at once. Figure 1 shows the R4400 pipeline in both views: a horizontal slice shows the execution process of individual instructions, and a vertical slice shows the processing of eight instructions at once.

Each box shown in Figure 1 corresponds to a part of the execution process.

Figure 2 illustrates the activities occuring within each pipestage as a function of the instruction type. First, in the IF stage, an instruction address is selected by the program counter logic and the first half of both the instruction cache fetch (IC1) and the instruction virtual to physical address translation (ITLB1) is performed. The instruction address translation is done through a two entry subset of the main or *joint* translation lookaside buffer (JTLB) called the ITLB. In the IS stage, the second half of both the instruction cache fetch (IC2) and instruction translation (ITLB2) are done.

During the RF stage, three activities occur in parallel. The instruction decoder (IDEC) decodes the instruction and checks for interlock conditions. Meanwhile, the instruction tag check (ITC) is performed between the instruction cache tag and the page frame number (PFN) from the ITLB's translation. In parallel with both of the above, the operands are fetched from the register file (RF).

In the EX stage, if the instruction is a register-to-register operation, the arithmetic or logical operation is performed (ALU). If the instruction is a load/store, a data virtual address is calculated (DVA). If the instruction is a branch, a virtual branch target address is calculated (IVA).

For load/stores, the DF stage is used to do the first half of both the data cache fetch (DC1) and the data virtual to physical address translation (JTLB1). Similarly, the DS stage does the second half of both the data fetch (DC2) and the data translation (JTLB2) as well as the load align or store align (LSA), as appropriate. If the instruction is a branch, the JTLB is used during DF and DS to translate the branch address and refill the ITLB if necessary.

The TC stage is used to perform the tag check for load/stores. During the WB stage the instruction result is written to the register file.

Smooth pipeline flow is interrupted when cache accesses miss, data dependencies are detected, or when exceptions occur. Interruptions that are handled by hardware, such as cache misses, are referred to as *interlocks,* while those that are handled using software are *exceptions.* Collectively, the cases of all interlock and exception conditions are referred to as *faults.*

Interlocks come in two varieties. Those interlocks which are resolved by simply stopping the pipeline are referred to as *stalls,* while those which require part of the pipeline to advance while holding up another part are *slips.*

At each cycle, exception and interlock conditions are checked for all active instructions. The conditions can be referred back to particular instructions, as each exception or interlock condition corresponds to a particular pipeline stage.

When an exception condition occurs, the relevant instruction and all that follow it in the pipeline are cancelled. Accordingly, any stall conditions and any later exception conditions that are referenced to the same instruction are inhibited; there is no value in servicing stalls for a cancelled instruction. A new

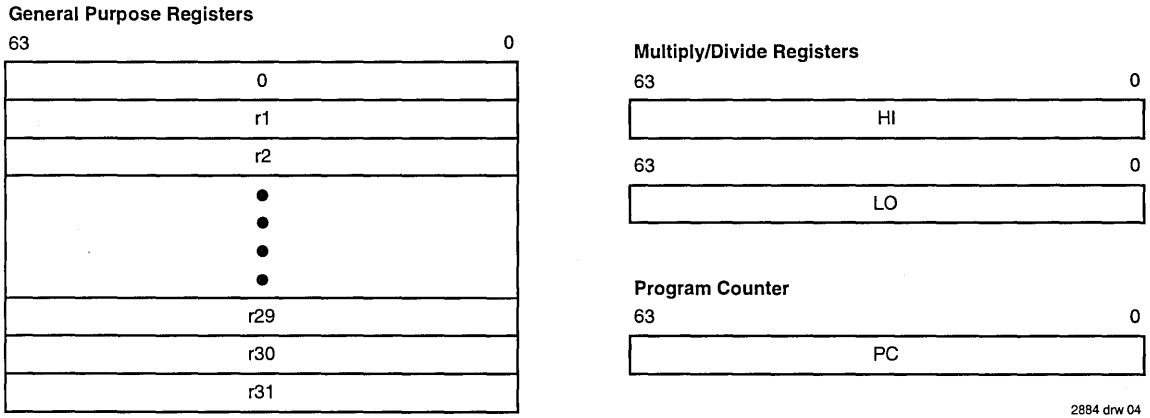


Figure 3. CPU Registers

instruction stream is begun, starting execution at a predefined exception vector. System control coprocessor registers are loaded with information that will identify the type of exception and any necessary auxiliary information, such as the virtual address at which translation exceptions occur.

When a stall condition is detected, all eight instructions, each in a different stage of the pipeline, are frozen at once. Often, the stall condition is only detected after parts of the pipeline have advanced using incorrect data; this occurrence is referred to as *pipeline overrun.* When in the stalled state, parts of the pipeline that are immune to overrun are frozen and the remainder is permitted to continue clocking. Just before resuming execution, the pipeline overrun is reversed by inserting corrected information into the pipeline.

When a slip condition is detected, the pipeline stages which must advance in order to resolve the dependency continue to be retired while the dependent stages are held until the necessary data is available.

Another class of interlocks exists which, since they originate external to the processor, are not referenced to a particular pipeline stage. These interlocks are referred to as *external* stalls and are unaffected by the occurrence of exceptions.

Integer Execution Engine

The R4400 implements the extended MIPS Instruction Set architecture, and thus is fully upwards compatible with applications running on the earlier generation parts. The R4400 includes additions to the instruction set, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, as well as faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability amongst implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4400 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The programmer model for the R4400 includes the register set illustrated in Figure 3. The register resources include: 32 general purpose orthogonal integer registers, the HI/LO result registers for the intger multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

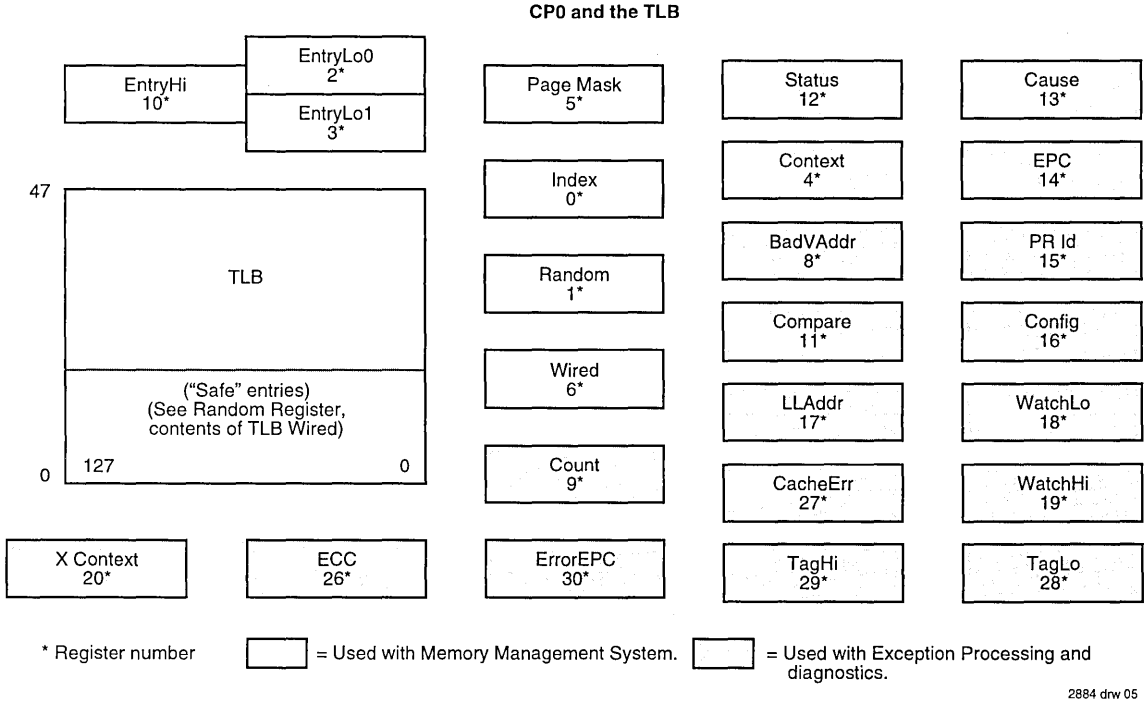


Figure 4. The R4400 CP0 Registers

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory subsystem, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4400 CP0 is a superset extension of the MMU found in the R3000A.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction translation buffer (the ITLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

System Control Co-Processor Registers

The R4400 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined, changed (the operating modes, kernel vs. user mode, interrupts enabled or disabled, cache features) and controlled. Also, these registers control exception handling. In addition, the R4400 includes registers to implement a real-time cycle counting facility, to address reference traps for debugging, to aid in cache diagnostic testing, and to assist in data error detection and correction.

Figure 4 illustrates the System Control Co-Processor registers.

Virtual to Physical Address Mapping

The R4400 provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4400 provides a single, uniform virtual address space of 2GB.

When operating in the kernel mode, four distinct virtual address spaces, totalling 4GB, are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4400 processor also support a supervisor mode in which the virtual address space is 2.5GB, divided into two regions based on the high-order bits of the virtual address. The three different modes of virtual addressing are shown in Figure 5. When the R4400 is configured as a 64-bit microprocessor, the virtual address space layout is a compatible extension of the 32-bit virtual address space layout.

Joint TLB

For fast virtual-to-physical address decoding, the R4400 uses a large, fully associative TLB which maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64gB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can treat various regions of memory distinctly from applications programs and data files. For example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4400 uses a Random Replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, noncoherent, sharable, exclusive, or update. The use of these attributes, coupled with state information in the processor caches, enables a wide variety of multiprocessing strategies to be easily implemented.

Figure 6 shows the format of the TLB entry and registers used to control the TLB.

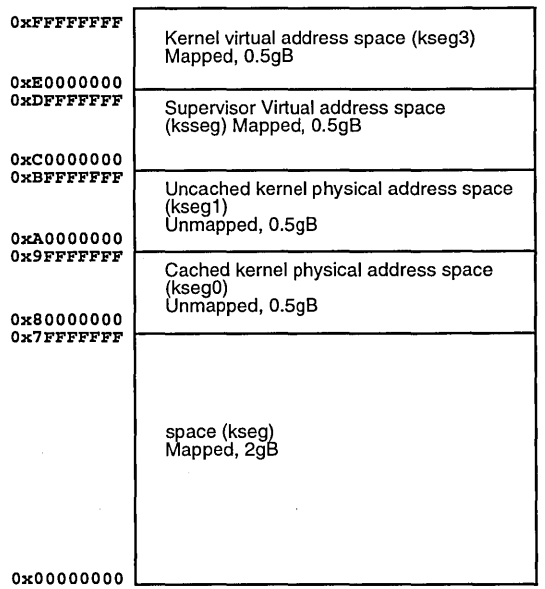


Figure 5. Kernel Mode Virtual Addressing (32-bit mode)

Instruction TLB

The R4400 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the ITLB is filled from the JTLB. The operation of the ITLB is invisible to the user.

Register File

The R4400 has thirty-two general purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and uses bypassing to enable the reading and writing of the same register twice per cycle as well as to minimize the operation latency in the pipeline.

ALU

The R4400 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all shift operations. Each of these units is highly optimized and can perform an operation in a single superpipeline cycle.

Integer Multiplier/Divider

The R4400 integer multplier and divider units perform signed and unsigned multiply and divide operations and execute instructions in parallel with the ALU. The results of the operation are placed in the *MDHI* and *MDLO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. The following table shows the number of processor internal cycles required between a 32-bit integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall

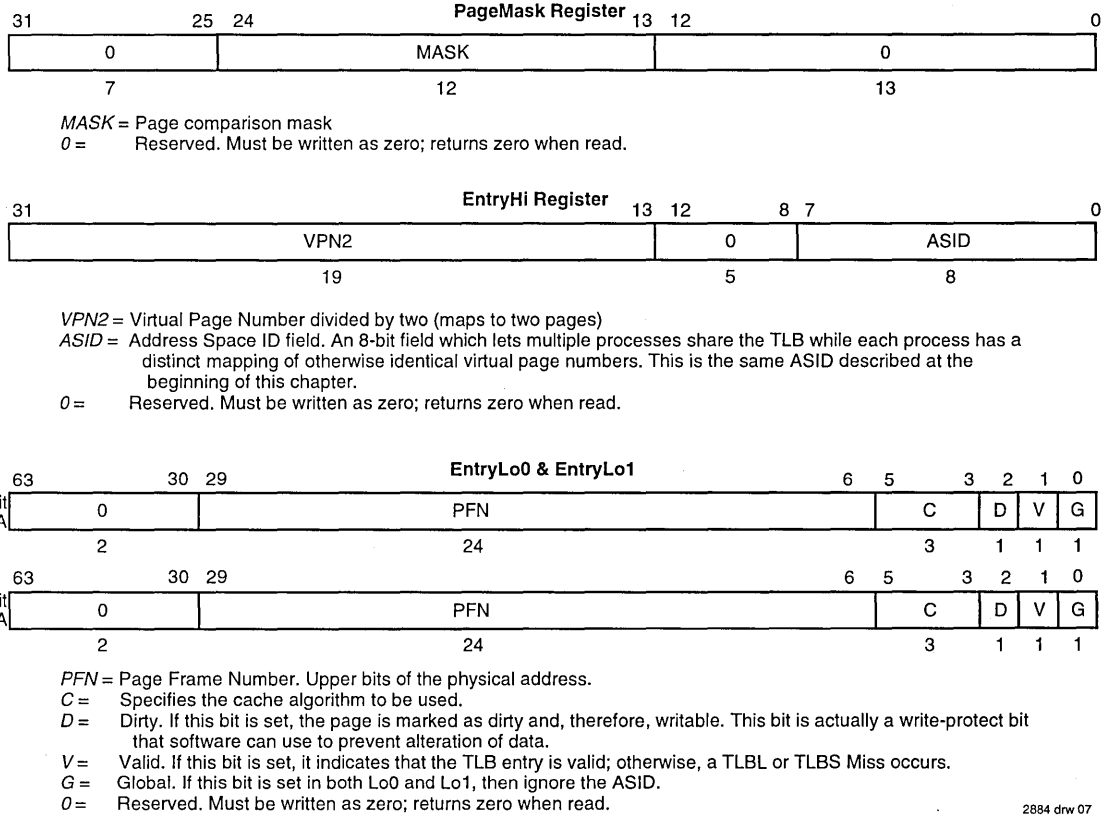


Figure 6. Fields of an R4400 TLB Entry

occurs.

Operation	Single Word	Double Word
MULT	10	20
DIV	69	133

FLOATING-POINT UNIT

The R4400 incorporates an entire floating-point unit on chip, including a floating-point register file and execution unit. The floating-point unit forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

Floating-point Co-Processor

The R4400 floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into separate multiply, divide, and add/convert/square root units, which allow for overlapped operations. The multiplier is pipelined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R3010, the R4400 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. Thes operations comply with the IEEE Standard 754.

The following table gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	7	8
DIV	23	36
SQRT	54	112
CMP	3	3
FIX	4	4
ROUND	4	4
TRUNC	4	4
FLOAT	5	5
ABS	2	2
MOV	1	1
NEG	2	2
LWC1,LDC1	3	3
SWC1,SDC1	1	1

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Floating-Point General Register File

The floating-point register file is made up of sixteen 64-bit registers which can also be viewed as thirty-two 32-bit floating-point registers. The MIPS architecture supports a coprocessor load and store double so, when configured as 64-bit registers, the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store a doubleword instruction in every cycle.

Floating-Point Control Register File

The floating-point control registers contain a register for determining configuration and revision information for the coprocessor and control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

CACHE MEMORY

In order to keep the high-performance superpipeline full and operating efficiently, the R4400 incorporates on-chip instruction and data caches. Each cache has its own 64-bit data path that can be accessed twice a cycle, so the instruction and data caches can be accessed in parallel with full pipelining. Combining this feature with a pipelined, single master clock cycle access of each cache, the cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2GB per second at a system clock frequency of 75MHz.

5

Instruction Cache

The IDT79R4400 incorporates a direct-mapped on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with byte parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed twice per master clock cycle, although the current IDT79R4400 CPU fetches on 32-bit unit/master cycle for a peak instruction bandwidth of 400MB/sec. The line size can be configured as four or eight words to allow different applications to have a line size that delivers optimum performance.

Data Cache

For fast, single cycle data access, the IDT79R4400 includes an 16KB on-chip data cache.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

The Data Cache is direct mapped, and its line size can be configured as four or eight words. The write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck

of waiting for each store operation to finish before issuing a subsequent memory operation.

Associated with the Data Cache is the store buffer. When the R4400 executes a store instruction, this 2-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data gets written into the Data Cache in the next cycle that the Data Cache is not accessed. The store buffer allows the R4400 to execute two stores per master cycle and to perform back-to-back stores without penalty. Likewise, the R4400 can perform two loads or a load and store per master cycle without penalty, yielding 1.2GB/sec bandwidth without restrictions on instruction combinations.

When the Data Cache line does need to be written back to slower memory (either secondary cache or main memory), the processor writes the data to an internal write buffer which can hold a line (4 or 8 words) of data. By writing the data to the fast write buffer, the processor can continue executing instructions without having to wait until the write completes to the slower memory.

The IDT79R4400 caches are designed for easy and flexible integration in many types of multiprocessor systems. The Data Cache contains all the necessary state bits to allow the R4400 to maintain cache coherency across all R4400 processors in a system.

SECONDARY CACHE INTERFACE

The R4400SC and R4400MC support a secondary cache that can range in size from 128KBs to 4MBs. The cache can be configured as a unified cache or split into an instruction cache and a data cache, and it can be designed using industry standard SRAMs. The IDT R4400 provides all of the secondary cache control circuitry on chip, including ECC.

The secondary cache interface consists of a 128-bit data bus, a 25-bit tag bus, and 18-bit address bus, and SRAM control signals. The wide data bus improves performance by providing a high bandwidth data path to fill the primary caches. ECC check bits are added to both the data and tag buses to improve data integrity. All double-bit errors can be detected and all single bit-errors can be detected and all single bit-errors can be corrected on both buses.

The secondary cache access time is configurable, providing system designers with the flexibility to tailor the cache design to specific applications. The line size of the secondary cache is also configurable and can be 4-, 8-, 16-, or 32-words. The line size of the primary cache must always be less than or equal to the line size of the secondary cache.

The secondary cache is physically tagged and physically indexed. The physical cache prevents problems that could arise due to virtual address aliasing. Also, a physical cache makes multiprocessing cache coherency protocols easier to implement. The R4400MC provides a set of cache states and a mechanism for manipulating the contents and state of the cache, which are sufficient to implement a variety of cache coherency protocols, using either bus snooping or directory based schemes.

SYSTEM INTERFACE

The R4400 supports a 64-bit system interface that can be used to construct systems as simple as a uniprocessor with a direct DRAM interface and no secondary cache or as sopisticated as a fully cache coherent multiprocessor. The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 75MHz.

Figure 7 shows a typical desktop system using the R4400PC. Similarly, a high-performance desktop workstation/server system can be built using the IDT79R4400SC and adding a secondary cache.

The system interface allows the processor to access external resources in order to satisfy cache misses and uncached operations. The IDT79R4400MC, in addition to handling simple memory and I/O transactions, supports a number of cache coherency transactions of sufficient generality to support a variety of cache coherent multiprocessing models. In particular, the interface is designed to support both bus snooping and directory based multiprocessor models and supports both write-update and write-invalidate coherency protocols.

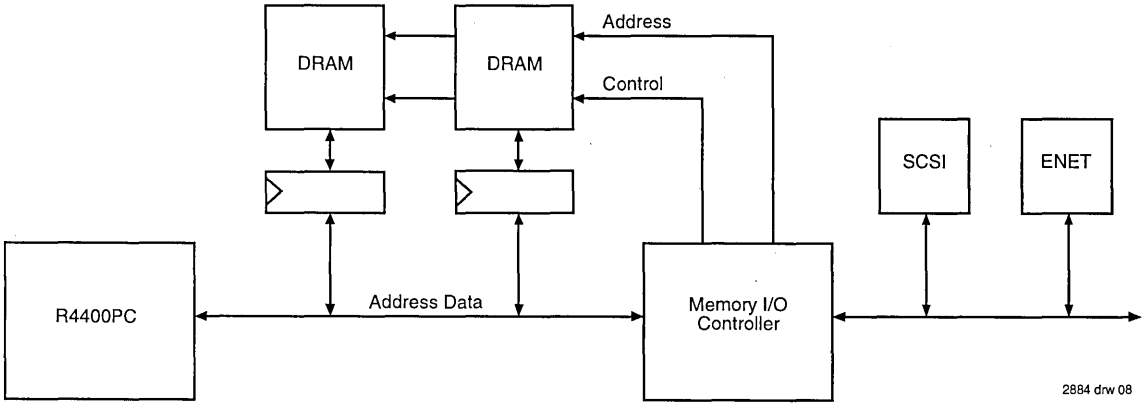

Figure 7. Typical Desktop System Block Diagram

Figure 8 shows a typical multiprocessor system using the IDT79R4400MC, an interface agent, and a secondary cache.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4400 and the rest of the system. It is protected with an 8-bit check bus, SysADC. The check bits can be configured as either parity or ECC, for flexibility in interfacing to either parity or ECC memory systems.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4400 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no write buffering or a fast, high performance interface can be designed to communicate with the R4400. Again, the system designer has the flexibility to make these price/perfomance tradeoffs.

System Command Bus

The R4400 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this line of data is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4400. Processor requests are initiated by the R4400 and responded to by an external device. External requests are issued by an external device and require the R4400 to respond.

The R4400 supports byte, halfword, tribyte, word, doubleword, and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

Handshake Signals

There are eight handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the IDT79R4400 whether it can accept a new read or write transaction. The IDT79R4400 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$ and $\overline{\text{Release}}$ are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{\text{ExtRqst}}$. The IDT79R4400 responds by asserting $\overline{\text{Release}}$ to release the system interface to slave state.

$\overline{\text{ValidOut}}$ and $\overline{\text{ValidIn}}$ are used by the IDT79R4400 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4400 asserts $\overline{\text{ValidOut}}$ when it is driving these buses with a valid command or data, and the external device drives $\overline{\text{ValidIn}}$ when it has control of the buses and is driving a valid command or data.

Finally, there are two signals that are available on the MC version only and are used in multiprocessing systems. They are $\overline{\text{IvdAck}}$ and $\overline{\text{IvdErr}}$, and they are driven by an external device to indicate the completion status of the current processor invalidate or update request.

R4400 Requests

The R4400 is capable of issuing requests to a memory and I/O subsystem. The system interface supports two modes of operation:

- Secondary Cache mode
- No Secondary Cache mode

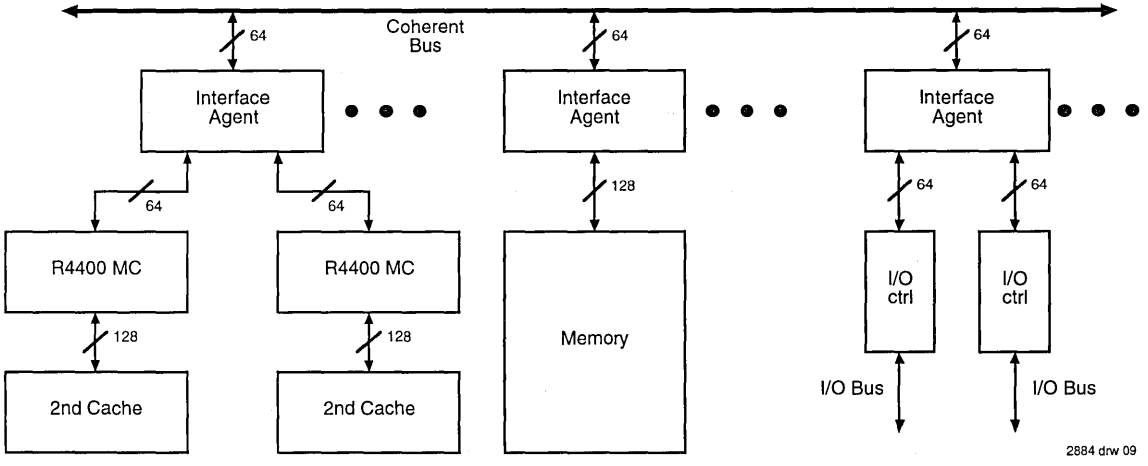

Figure 8. Multiprocessor System Using the R4400 MC

No Secondary Cache Mode

The R4400 without a secondary cache requires a non-overlapping system interface. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4400 issues another request. The R4400PC can issue read and write requests to an external device, and an external device can issue read and write requests to the R4400.

Figure 9 shows a processor read request. The R4400 asserts $\overline{\text{ValidOut}}$ and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has $\overline{\text{RdRdy}}$ asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting $\overline{\text{Release}}$. The external device can then begin sending the data to the IDT79R4400.

Secondary Cache Mode

The R4400 with a secondary cache operates in an overlapping bus transfer mode in which multiple system interface transactions may be issued in parallel. The processor may issue a combination of read request, an update or invalidate request, and a write request. For instance, when a dirty cache line needs to be replaced, the processor issues a read request immediately followed by a write request, without waiting for the read data to return. This has the advantage of "hiding" the write transaction between the read request and read response, thus increasing overall system performance. This mode of operation is not necessary or useful in R4400 systems without secondary cache since the processor contains a write buffer capable of accepting an entire primary cache line of data. Overlapping is a superset of non-overlapping system operation.

Figure 10 illustrates a processor request in overlap mode. This request is made up of a read, invalidate, and write request. Note that the protocol for the read, the invalidate, and the write are all similar to each other, with the exception that the processor also sends out valid data during the write request. In Figure 10 the processor write transaction not only occurs before the read response from the external device, but it also illustrates how an external device can hold off a write request through the deassertion of WrRdy.

External Requests

The R4400 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4400 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue cache coherency requests to the processor, such as a request for the R4400 to update, invalidate, or snoop upon its caches, or to supply a cache line of data. Additionally, an external device may need to write to the R4400 interrupt register.

The following is a list of the supported external requests:

- Read
- Write
- Invalidate

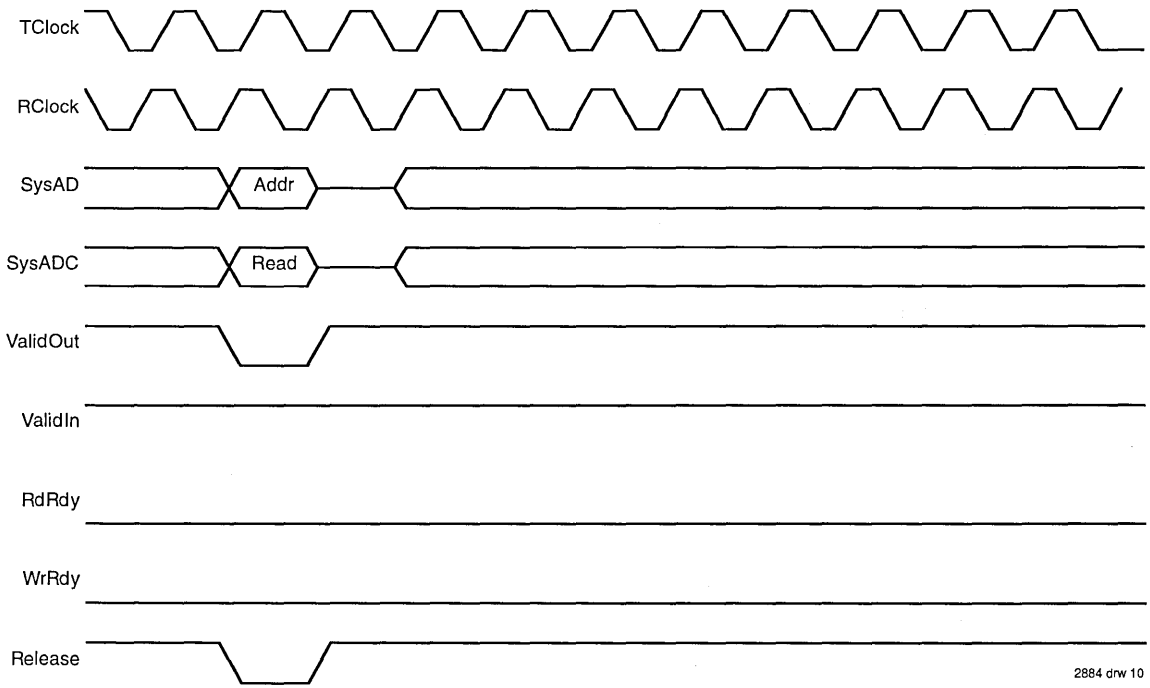

Figure 9. Processor Read Request

- Update
- Snoop
- Intervention
- Null

Figure 11 shows an example of an external snoop request. The process by which the external device issues the request is very similar to the way the R4400 issues a request. The external device first gains ownership of the system interface by asserting $\overline{\text{ExtRqst}}$ and waiting for the R4400 to assert $\overline{\text{Release}}$. The external device then sends in a valid command by asserting $\overline{\text{ValidIn}}$ and driving the SysCmd and SysAD buses with the snoop command and address. The R4400 responds to the request by asserting $\overline{\text{ValidOut}}$ and driving the SysCmd bus with the cache state of the snooped upon line.

CACHE COHERENCY CAPABILITY

With the IDT79R4400MC, cache coherence is maintained in hardware. The system control coprocessor permits the specification of different caching protocols on a per-page basis. A page may be:

- uncached
- cached but non-coherent
- cached and coherent exclusive (only one processor cache contains the data on loads and stores).
- cached and coherent exclusive on writes (write invalidate scheme-only one processor cache contains the data when that datum is written to).
- cached and coherent with updates on writes (write-update scheme).

Depending upon the amount and type of data sharing in an application, the operating system can choose the most appropriate caching strategy.

Support for processor synchronization is provided by the Load Linked and Store Conditional instructions. The Load Linked and Store Conditional instructions:

1. Provide a simple mechanism for generating all of the common synchronization primitives including test-and-set, bit-level locks, semaphores, counters, sequencers, etc. with no additional hardware overhead.
2. Operate in such a fashion that bus traffic is only generated when the state of the cache line changes.
3. Need not lock a system bus—a very important feature for larger systems.

ADVANCED FEATURES

The R4400 supports a number of other capabilities in addition to the standard processor model described above. Many of these capabilities are selected by the system designer during the processor reset sequence, via the boot time mode control interface. Features are included to support fault tolerance, system test, or other system environments.

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (Master clock divided by 256). The low

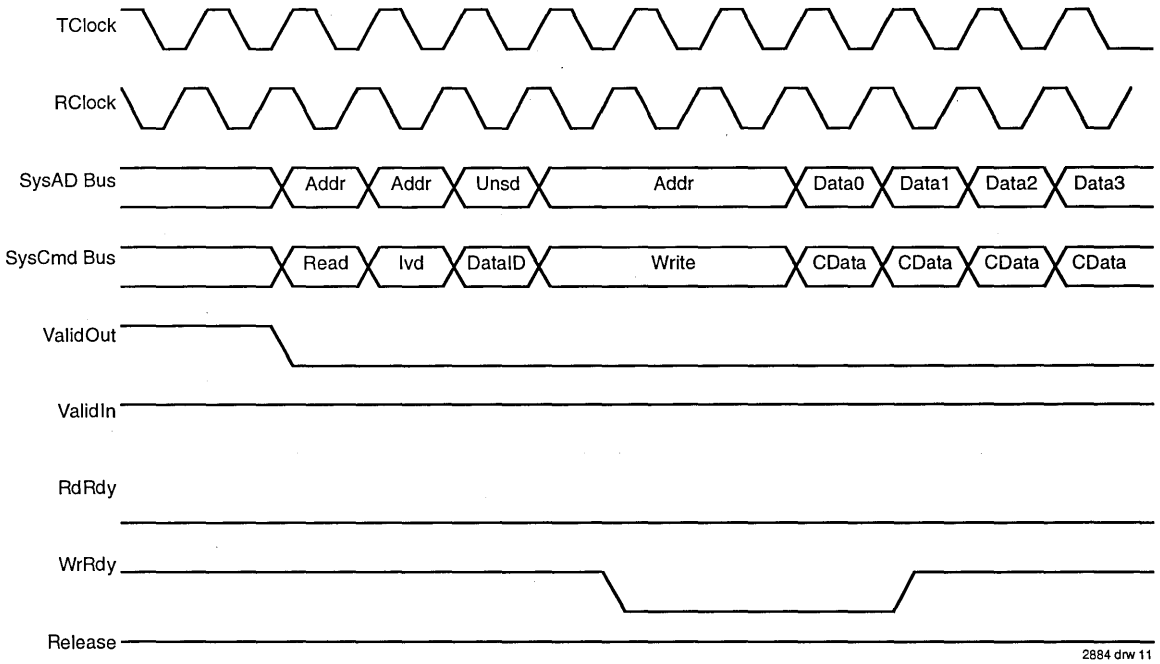

Figure 10. Processor Read, Invalidate, Write Request

frequency operation allows the initialization information to be kept in a low cost EPROM.

Immediately after the VCCOk Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG INTERFACE

The JTAG boundary scan mechanism provides a capability for testing the interconnect between the IDT79R4400 processor, the printed circuit board to which it is attached, and the other components on the board. In addition the JTAG boundary scan mechanism provides a rudimentary capability for low-speed logical testing of the secondary cache RAMs. The JTAG boundary scan mechanism does not provide any capability for testing the R4400 processor itself.

In accordance with the JTAG specification the R4400 processor contains a TAP controller, JTAG instruction register, JTAG boundary scan register, JTAG identification register, and JTAG bypass register. However, the R4400 JTAG implementation provides only the *external test* functionality of the boundary scan register.

FAULT TOLERANT SUPPORT

The R4400 has been designed to support varying models of fault tolerance. These modes include: master/checker operation and triple-modular redundancy. In addition to explicit fault-tolerant modes of operation, the design of internal processor operation is such to support processor synchronization; for example, both the TLB random replacement algorithm, and the on-chip timer, can be forced to known states via software. Thus, the IDT R4400 family can be used to build "non-stop" machines across a number of different system models.

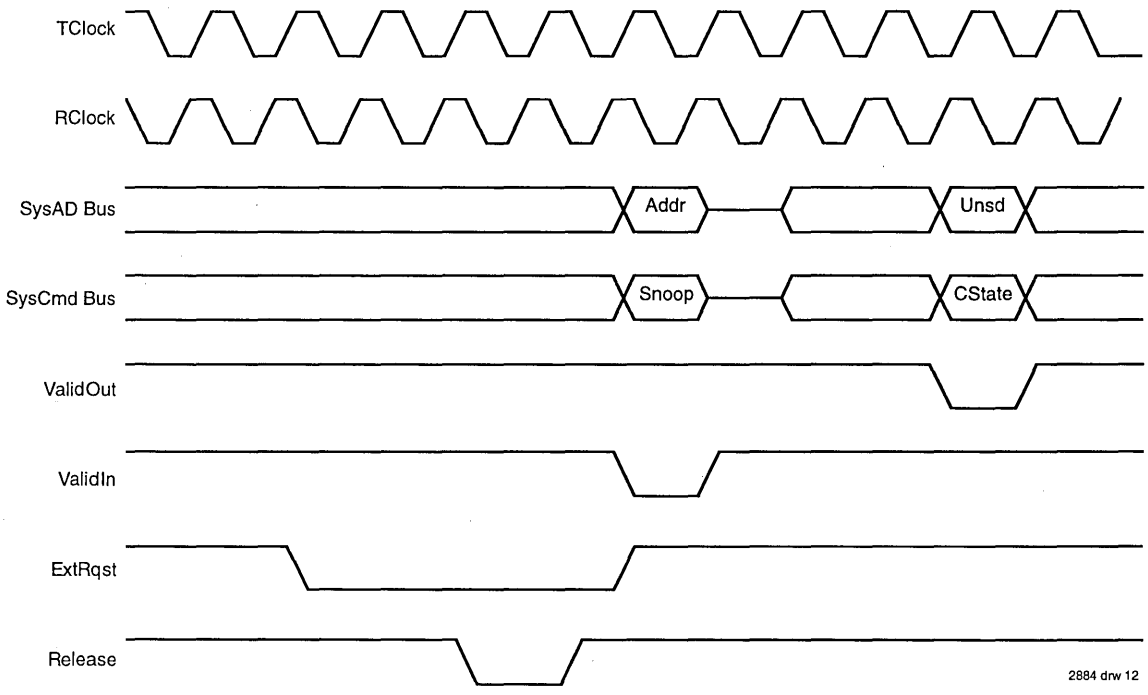

Figure 11. External Snoop Request

BOOT-TIME MODES

Serial Bit	Value	Mode Setting
0		**BlkOrder**: Block read response ordering.
	0	Sequential ordering.
	1	Sub-block ordering.
1		**EIBParMode:** System interface check bus checking.
	0	SECDED error checking and correcting mode.
	1	Byte parity.
2		**EndBit:** Byte ordering.
	0	Little Endian.
	1	Big Endian.
3		**DShMdDis:** Dirty shared mode, enables transition to dirty shared state on processor update successful.
	0	Dirty Shared Enabled.
	1	Dirty Shared Disabled.
4		**NoSCMode:** Specifies presence of secondary cache.
	0	Present.
	1	Not Present.
5:6		**SysPort:** System Interface port width (Bit 6 Most Significant).
	0	64 bits.
	1-3	Reserved(1)
7		**SC64BitMd:** Secondary cache interface port width.
	0	128 bits.
	1	Reserved(1).
8		**ElSpltMd:** Secondary cache organization
	0	Unified
	1	Reserved(1)
9:10		**SCBlkSz:** Secondary cache line size (Bit 10 Most Significant).
	0	4 words.
	1	8 words.
	2	16 words.
	3	32 words.
11:14		**XmitDatPat:** System Interface Data Rate (Bit 14 Most Significant).
	0	D
	1	DDx
	2	DDxx
	3	DxDx
	4	DDxxx
	5	DDxxxx
	6	DxxDxx
	7	DDxxxxxx
	8	DxxxDxxx
	9-15	Reserved(1)
15:17		**SysCkRatio:** PClock to SClock divisor: frequency relationship between SClock, RClock, and TClock and PClock (Bit 17 MostSignificant).
	0	Divide by 2
	1	Divide by 3
	2	Divide by 4
	3	Divide by 6
	4	Divide by 8
	5-7	Reserved(1)
18	0	Reserved (Required value)
19		**TimIntDis:** Timer Interrupt enable allows timer interrupts, otherwise the interrupt used by the timer becomes a general-purpose interrupt.
	0	Enabled
	1	Disabled
20		**PotUpdDis:** Potential invalidate enable (allows potential invalidates to be issued. Otherwise only normal invalidates are issued).

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Serial Bit	Value	Mode Setting
	0	Enabled
	1	Disabled
21:24		**TWrSUp:** Secondary cache write deassertion delay, T_{WrSup} in PCycles (Bit 24 Most Signifi cant).
	0-2	Undefined
	3-15	Number of PCLK cycles (Min 3; Max 15)
25:26		**TWr2Dly:** Secondary cache write assertion delay 2, T_{Wr2Dly} in PCycles (Bit 26 Most Signifi cant).
	0	Undefined
	1-3	Number of PCLK cycles (Min 1; Max 3)
27:28		**TWr1Dly:** Secondary cache write assertion delay 1, T_{Wr1Dly} in PCycles (Bit 28 Most Signifi cant).
	0	Undefined
	1-3	Number of PCLK cycles (Min 1; Max 3)
29		**TWrRc:** Secondary cache write recovery time, T_{WrRc} in PCycles either 0 or 1 cycles.
	0	0 cycle
	1	1 cycle
30:32		**TDis:** Secondary cache disable time, T_{Dis} in PCycles (Bit 32 Most Significant).
	0	Undefined
	1	Number of PCLK cycles (Min 2; Max 7)
33:36		**TRd2Cyc:** Secondary cache read cycle time 2, T_{RdCyc2} in PCycles (Bit 36 Most Significant).
	0-2	Undefined
	3-15	Number of PCLK cycles (Min 3; Max 15)
37:40		**TRd2Cyc:** Secondary cache read cycle time 1, T_{RdCyc1} in PCycles, (Bit 40 Most Significant).
	0-3	Undefined
	4-15	Number of PCLK cycles (Min 4; Max 15)
41		**NoMPmode:** Secondary cache line is not invalidated
	0	NoMPmode off: after a secondary cache miss, the existing valid caceline is invalidated (following writeback if necessary)
	1	NoMPmode on: after a secondary cache miss, the existing valid cache line is not invali dated. Available on the R4400SC to improve performance.
42		**SCMaster Md:** selects the type of Master/Checker mode (also see description of mode bit 18).
	SCMasterMd	SIMasterMd (Bit 18)
	0	0 Complete Master (required for single-chip operation)
	1	1 Complete Listener (paired with Complete Master)
	1	0 System Interface Master (SIMaster)
	0	1 Secondary Cache Master (SCMaster, paired with SIMaster)
43:45[2]	0	Reserved.
46		**Pkg179:** R4400 type.
	0	Large (447 pin). SC/MC
	1	Small (179). PC
47:49		**CycDivisor:** This mode determines the clock divisior for the reduced power mode. When the RP bit in the Status Register is set to one, the pipeline clock is divided by one of the following values (Bit 49 is Most Significant).
	0	Divide by 2
	1	Divide by 4
	2	Divide by 8
	3	Divide by 16
	4-7	Reserved[1]
50:52		**Drv0_50, Drv0_75, Drv1_00:** Drive the outputs in N x MasterClock period (Bit 52 Most Significant) .
	0-1	Drive at 0.5 x MasterClockperiod.
	2-3	Drive at 0.75 x MasterClock period.
	4-7	Drive at 1.0 x MasterClock period.

2884 tbl 04

53:56		**InitP:** Initial values for the state bits that determine the pull-down di/dt and switching speed of the output buffers (Bit 53 Most Significant).
	0	Fastest pull-down rate.
	1-14	Intermediate pull-down rate.
	15	Slowest pull-down rate.
57:60		**InitN:** Initial values for the state bits that determine the pull-up di/dt and switching speed of the output buffers (Bit 57 Most Significant).
	0	Slowest pull-up rate.
	1-14	Intermediate pull-up rates.
	15	Fastest pull-up rate.
61		**EnbIDPLLR:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers only during ColdReset.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.
Serial Bit	**Value**	**Mode Setting**
62		**EnbIDPLL:** Enables the negative feedback loop that determines the di/dt and switching speed of the output buffers during ColdReset and during normal operation.
	0	Disable di/dt control mechanism.
	1	Enable di/dt control mechanism.
63		**DsbIDPLL:** Enables PLLs that match MasterIn and produce RClock, TClock, SClock and the internal clocks.
	0	Enable PLLs.
	1	Disable PLLs.
64		**SRTristate:** Controls when output-only pins are trestated
	0	Only whe $\overline{\text{ColdReset}}$ is asserted.
	1	When $\overline{\text{Reset}}$ or $\overline{\text{ColdReset}}$ are asserted
65-255	0[2]	Reserved (must be scanned in as zeros).

2884 tbl 05

NOTES:
1. Selecting a Reserved value results in undefined processor behavior.
2. 0's must be presented for these reserved values.

PIN DESCRIPTION

The following is a list of interface, interrupt and maintenance pins available on the different package configurations.

Pin Name	Type	Description
Secondary cache interface pins available *only* on the SC and MC configuration:		
SCAddr(17:1)	Output	Secondary cache address bus A 17-bit address bus for the secondary cache.
SCAddr0(W:Z)	Output	Secondary cache address lsb To minimize loading effect, there are 4 identical copies of this signal.
SCAPar(2:0)	Output	Secondary cache address parity bus A 3-bit bus that carries the parity of the SCAddr bus and the cache control lines $\overline{\text{SCOE}}$, $\overline{\text{SCWR}}$, $\overline{\text{SCDCS}}$ and $\overline{\text{SCTCS}}$.
SCData(127:0)	Input/Output	Secondary cache data bus A 128-bit bus used to read or write cache data from/to the secondary cache.
SCDChk(15:0)	Input/Output	Secondary cache data ECC bus A 16-bit bus that carries two 8-bit ECC fields that covers the 128 bits of the SCData from/to the secondary cache. SCDChk(15:8) corresponds to SCData(127:64) and SCDChk(7:0) corresponds to SCData(63:0).
$\overline{\text{SCDCS}}$	Output	Secondary cache data chip select Chip select enable signal for the secondary cache Ram associated with SCData and SCDChk.
$\overline{\text{SCOE}}$	Output	Secondary cache output enable Output enable for the secondary cache RAM.
SCTag(24:0)	Input/Output	Secondary cache tag bus A 25-bit bus used to read or write cache tags from/to the secondary cache.
SCTChk(6:0)	Input/Output	Secondary cache tag ECC bus A 7-bit bus that carries an ECC field covering the SCTag from/to the secondary cache.

PIN DESCRIPTION (Cont.)

Pin Name	Type	Description
$\overline{SCTCS}$	Output	Secondary cache tag chip select Chip select enable signal for the secondary cache tag RAM associated with SCTag and SCTChk.
$\overline{SCWr}$(W:Z)	Output	Secondary Cache write enable Write enable for the secondary cache RAM.
System interface pins available on all parts:		
$\overline{ExtRqst}$	Input	External request Signals that the system interface needs to submit an external request.
$\overline{Release}$	Output	Release interface Signals that the processor is releasing the system interface to slave state
$\overline{RdRdy}$	Input	Read Ready Signals that an external agent can now accept a processor read, invalidate, or update request in both secondary cache and no secondary cache mode or can accept a read followed by a write request in secondary cache mode.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing check bits for the SysAD bus.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	System command/data identifier bus parity A single, even-parity bit for the SysCmd bus.
$\overline{ValidIn}$	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{ValidOut}$	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
$\overline{WrRdy}$	Input	Write Ready Signals that an external agent can now accept a processor write request in both non-overlap and overlap mode.
System interface pins available only on the MC configuration.		
$\overline{IvdAck}$	Input	Invalidate acknowledge Signals successful completion of a processor invalidate or update request.
$\overline{IvdErr}$	Input	Invalidate error Signals unsuccessful completion of a processor invalidate or update request.
Interrupt pins available only on the PC configuration:		
$\overline{Int}$(5:1)	Input	Interrupt Five of six general processor interrupts, bit-wise ORed with bits 5:1 of the interrupt register.
Interrupt pin available on all devices:		
$\overline{Int}$(0)	Input	Interrupt One of six general processor interrupts, bit-wise ORed with bit 0 of the interrupt register.
Non-maskable interrupt pin available on all devices:		
$\overline{NMI}$	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

2884 tbl 06

PIN DESCRIPTION (Cont.)

Pin Name	Type	Description
Boot-time mode control interface pins available on all devices:		
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.
JTAG interface pins available on all devices:		
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.
Maintenance pins available on all devices:		
IOOut	Output	I/O output Output slew rate control feedback loop output. Must be connected to IOIn through a delay loop that models the IO path from the R4000 to an external agent.
IOIn	Input	I/O input Output slew rate control feedback loop input (see IOOut).
MasterClock	Input	Master clock Master clock input at the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
VCCOk	Input	VCC is OK When asserted, this signal indicates to the R4000 that the +5 volt power supply has been above 4.75 volts for more than 100 milliseconds and will remain stable. The assertion of VCCOk initiates the reading of the boot-time mode control serial stream.
$\overline{\text{ColdReset}}$	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of $\overline{\text{ColdReset}}$. $\overline{\text{ColdReset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Reset}}$	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. $\overline{\text{Reset}}$ must be de-asserted synchronously with MasterOut.
$\overline{\text{Fault}}$	Output	Fault Mismatch output of boundary comparators.
VccP	Input	Quiet VCC for PLL Quiet Vcc for the internal phase locked loop.

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PIN DESCRIPTION (Cont.)

VssP	Input	Quiet VSS for PLL Quiet Vss for the internal phase locked loop.
Maintenance pins available only on the SC and MC configurations:		
Status(7:0)	Status	Output An 8-bit bus that indicates the current operation status of the processor.

2884 tbl 07

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TC	Operating Temperature	0 to +85 (Case)	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

2884 tbl 09

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed Vcc +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
R4400 Com.	0°C to +85°C (Case)	0V	5.0 ±5%
RV4400 Com.	0°C to +85°C (Case)	0V	3.3 ±5%

2884 tbl 10

DC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE

(Vcc = 5.0V ± 5%; Tcase = 0°C to +85°C)

			50MHz		67MHz		75MHz		
Symbol	Parameter	Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Units
VOH	Output HIGH Voltage	IOH = –4mA	3.5	—	3.5	—	3.5	—	V
VOHC	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	IOH = –4mA	4.0	—	4.0	—	4.0	—	V
VOL	Output LOW Voltage	IOL = 4mA	—	0.4	—	0.4	—	0.4	V
VIH	Input HIGH Voltage		2.0	Vcc + .5	2.0	Vcc + .5	2.0	Vcc + .5	V
VIL	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	–0.5(1)	0.8	V
VIHC	Input HIGH Voltage (MasterClock, SyncIn)		0.8 Vcc	Vcc + .5	0.8 Vcc	Vcc + .5	0.8 Vcc	Vcc + .5	V
VILC	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 Vcc	–0.5(1)	0.2 Vcc	–0.5(1)	0.2 Vcc	V
CIn	Input Capacitance		—	10	—	10	—	10	pF
COut	Output Capacitance		—	10	—	10	—	10	pF
ILeak	Input Leakage		—	10	—	10	—	10	µA
IOLeak	Input/Output Leakage		—	20	—	20	—	20	µA
ICC	Operating Current	Vcc = 5V, Tc=25°C	—	2.8	—	3.2	—	3.6	A

2884 tbl 11

NOTES:
1. VIL (min.) = –3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

AC ELECTRICAL CHARACTERISTICS—R4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=5.0V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	(3)	4	—	3	—	3	—	ns
TMCkLow	MasterClock Low	(3)	4	—	3	—	3	—	ns
	MasterClock Freq[1]		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

2884 tbl 12

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SYSTEM INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TDO[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
TDS	Data Setup		5	—	5	—	3.5	—	ns
TDH	Data Hold		1.5	—	1.5	—	1	—	ns

NOTES:
1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

2884 tbl 13a

BOOT MODE INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMDS	Mode Data Setup		3	—	3	—	3	—	MCLK cycles
TMDH	Mode Data Hold		0	—	0	—	0	—	MCLK cycles

2884 tbl 13b

SECONDARY CACHE INTERFACE PARAMETERS—R4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{SCDS}	Data Setup		5	—	5	—	3.5	—	ns
T_{SCDH}	Data Hold		2	—	1.5	—	1	—	ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	3	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

NOTES:
1. When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the Pclock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Number of cycles is configured through the boot time mode control.

CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

DC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	I_{OH} = –4mA	2.7	—	2.7	—	2.7	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + .5	2.0	V_{CC} + .5	2.0	V_{CC} + .5	V
V_{IL}	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IHC}	Input HIGH Voltage (MasterClock, SyncIn)		0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	V
V_{ILC}	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	V
C_{In}	Input Capacitance		—	10	—	10	—	10	pF
C_{Out}	Output Capacitance		—	10	—	10	—	10	pF
I_{Leak}	Input Leakage		—	10	—	10	—	10	µA
I_{OLeak}	Input/Output Leakage		—	20	—	20	—	20	µA
I_{CC}	Operating Current	V_{CC} = 3.3V, Tc=25°C	—	2.0	—	2.4	—	2.8	A

2884 tbl 11

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

DC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(V_{CC} = 3.3V ± 5%; Tcase = 0°C to +85°C)

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V
V_{OHC}	Output HIGH Voltage (MasterOut, TClock, RClock, SyncOut)(3)	I_{OH} = –4mA	2.7	—	2.7	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + .5	2.0	V_{CC} + .5	V
V_{IL}	Input LOW Voltage(1,2)		–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IHC}	Input HIGH Voltage (MasterClock, SyncIn)		0.8 V_{CC}	V_{CC} + .5	0.8 V_{CC}	V_{CC} + .5	V
V_{ILC}	Input LOW Voltage (MasterClock, SyncIn)		–0.5(1)	0.2 V_{CC}	–0.5(1)	0.2 V_{CC}	V
C_{In}	Input Capacitance		—	10	—	10	pF
C_{Out}	Output Capacitance		—	10	—	10	pF
I_{Leak}	Input Leakage		—	10	—	10	µA
I_{OLeak}	Input/Output Leakage		—	20	—	20	µA
I_{CC}	Operating Current	V_{CC} = 3.3V, Tc=25°C	—	TBD	—	TBD	A

2884 tbl 11

NOTES:
1. V_{IL} (min.) = –3.0V for pulse width less than 15ns.
2. Except for MasterClock input.
3. Applies to TClock, RClock, MasterOut, and ModeClock outputs.

AC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=3.3V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	4	—	3	—	3	—	ns
TMCkLow	MasterClock Low	[3]	4	—	3	—	3	—	ns
	MasterClock Freq[1]		25	50	25	67	25	75	MHz
TMCP	MasterClock Period		20	40	15	40	13.3	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)		—	±500	—	±500	—	±500	ps
TMCRise	MasterClock Rise Time		—	5	—	4	—	3.5	ns
TMCFall	MasterClock Fall Time		—	5	—	4	—	3.5	ns
TModeCKP	ModeClock Period		—	256*TMCP	—	256*TMCP	—	256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	4*TMCP	—	ns

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 5ns for 50, 67MHz; transition ≤ 3.5ns for 75MHz.

2884 tbl 12

AC ELECTRICAL CHARACTERISTICS—RV4400 COMMERCIAL TEMPERATURE RANGE

(Vcc=3.3V ± 5%; Tcase = 0°C to +85°C) MasterClock and Clock Parameters[2]

Symbol	Parameter	Conds.	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
TMCkHigh	MasterClock High	[3]	2.5	—	2.5	—	ns
TMCkLow	MasterClock Low	[3]	2.5	—	2.5	—	ns
	MasterClock Freq[1]		25	88	25	100	MHz
TMCP	MasterClock Period		11.3	40	10	40	ns
TMCJitter	Clock Jitter (on RClock, TClock, MasterOut, SyncOut)			±500		±500	ps
TMCRise	MasterClock Rise Time			2.5	—	2.5	ns
TMCFall	MasterClock Fall Time			2.5		2.5	ns
TModeCKP	ModeClock Period			256*TMCP		256*TMCP	ns
TJTAGCKP	JTAG Clock Period		4*TMCP	—	4*TMCP	—	ns

NOTES:
1. Operation of the R4400 is only guaranteed with the phase lock loop enabled.
2. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
3. Transition ≤ 2.5ns5.

2884 tbl 12

SYSTEM INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{DO}[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	3.5	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{DS}	Data Setup		5	—	5	—	3.5	—	ns
T_{DH}	Data Hold		1.5	—	1.5	—	1	—	ns

NOTES: 2884 tbl 13a

1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

SYSTEM INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max.	Min.	Max.	
T_{DO}[1,2,3]	Data Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	1	5	1	5	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	5	10	5	10	ns
T_{DS}	Data Setup		3.5	—	3.5	—	ns
T_{DH}	Data Hold		1	1	1	1	ns

NOTES: 2884 tbl 13a

1. When the dynamic output slew rate control Modebits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56] = 15, Modebits [57:60] = 0.
2. Timings are measured from 1.5V of the clock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per C_{LD} specification.
4. Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the R4000 on the system interface. Secondary cache signals are specified separately.

BOOT MODE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{MDS}	Mode Data Setup		3	—	3	—	3	—	M_{CLK} cycles
T_{MDH}	Mode Data Hold		0	—	0	—	0	—	M_{CLK} cycles

2884 tbl 13b

BOOT MODE INTERFACE PARAMETERS—R4400

Symbol	Paramete	88MHz		100MHz		Units
		Min.	Max.	Min.	Max.	
T_{MDS}	Mode Data Setup	3		3		M_{CLK} cycles
T_{MDH}	Mode Data Hold	0		0		M_{CLK} cycles

2884 tbl 13b

SECONDARY CACHE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	50MHz		67MHz		75MHz		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	2	10	2	7	2	7	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	6	16	6	12	6	12	ns
T_{SCDS}	Data Setup		5	—	5	—	3.5	—	ns
T_{SCDH}	Data Hold		2	—	1.5	—	1	—	ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	3	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	1	3	Pcycles

2884 tbl 14

SECONDARY CACHE INTERFACE PARAMETERS—RV4400

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max	Min	Max.	
T_{SCO}[1,2,3]	PClock to Output	Max Slew Rate Modebits[53:56] = 0 Modebits[57:60] = 15	1	5	1	5	ns
		Min Slew Rate Modebits[53:56] = 15 Modebits[57:60] = 0	5	10	5	10	ns
T_{SCDS}	Data Setup		3.5		3.5		ns
T_{SCDH}	Data Hold		1		1		ns
T_{Rd1Cyc}[4]	Cycle length of 4 word Rd		4	15	4	15	Pcycles
T_{Dis}[4]	Cycles between Rd & Wr		2	7	2	7	Pcycles
T_{Rd2Cyc}[4]	Cycle length of 8 word Rd		3	15	3	15	Pcycles
T_{Wr1Dly}[4]	Cycles bet. Addr & $\overline{SCWr}$		1	3	1	3	Pcycles
T_{WrRc}[4]	Cycles bet. deassertion of $\overline{SCWr}$ to start of next cycle		0	1	0	1	Pcycles
T_{WrSUp}[4]	Cycles from second doubleword to $\overline{SCWr}$		2	15	2	15	Pcycles
T_{Wr2Dly}[4]	Cycles between1st & 2nd word in 8-word write		1	3	1	3	Pcycles

2884 tbl 14

NOTES:

1. When the dynamic output slew rate control Mode bits [61] or [62] are enabled, the initial values for the pull-up and pull-down rates should be set to the slowest value, Modebits [53:56]=15, Modebits[57:60]=0.
2. Timings are measured from 1.5V of the Pclock to 1.5V of signal.
3. Capacitive load for all output timings is 50pF. Deration is per CLD specification.
4. Number of cycles is configured through the boot time mode control.

CAPACITIVE LOAD DERATION

Symbol	Parameter	50MHz		67MHz		75MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
CLD	Load Derate	—	2	—	2	—	2	ns/25pF

2884 tbl 15

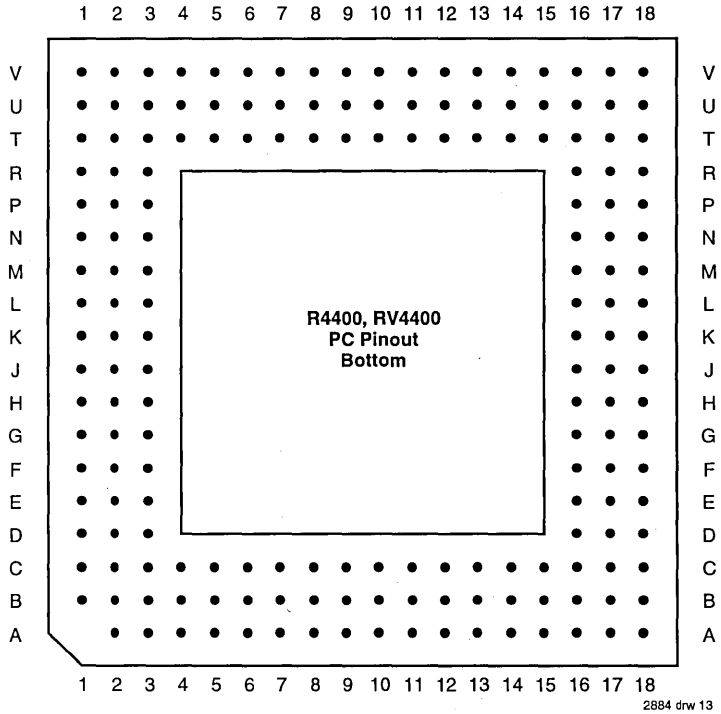
CAPACITIVE LOAD DERATION

Symbol	Parameter	Conditions	88MHz		100MHz		Units
			Min.	Max	Min	Max.	
CLD	Load Derate			2		2	ns/25pF

PRELIMINARY

2884 tbl 15

PHYSICAL SPECIFICATIONS



2884 drw 13

IDT79R4400/RV4400 PC PACKAGE PINOUT

R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin	R4400 Function	PC Pkg Pin
ColdReset	T14	SysAD29	T16	VssP	K16
ExtRqst	U2	SysAD30	R17	Vcc	A2
Fault	B16	SysAD31	M16	Vcc	A4
Reserved (NC)	U10	SysAD32	H2	Vcc	A7
Vcc	T9	SysAD33	G3	Vcc	A9
IOIn	T13	SysAD34	F3	Vcc	A11
IOOut	U12	SysAD35	D2	Vcc	A13
Int0	N2	SysAD36	C3	Vcc	A16
Int1	L3	SysAD37	B3	Vcc	B18
Int2	K3	SysAD38	C6	Vcc	C1
Int3	J3	SysAD39	C7	Vcc	D18
Int4	H3	SysAD40	C10	Vcc	F1
Int5	F2	SysAD41	C11	Vcc	G18
JTCK	H17	SysAD42	B13	Vcc	H1
JTDI	G16	SysAD43	A15	Vcc	J18
JTDO	F16	SysAD44	C15	Vcc	K1
JTMS	E16	SysAD45	B17	Vcc	L18
MasterClock	J17	SysAD46	E17	Vcc	M1
MasterOut	P17	SysAD47	F17	Vcc	N18
ModeClock	B4	SysAD48	L2	Vcc	R1
ModeIn	U4	SysAD49	M3	Vcc	T18
NMI	U7	SysAD50	N3	Vcc	U1
PLLCap0	****	SysAD51	R2	Vcc	V3
PLLCap1	****	SysAD52	T3	Vcc	V6
RClock0	T17	SysAD53	U3	Vcc	V8
RClock1	R16	SysAD54	T6	Vcc	V10
RdRdy	T5	SysAD55	T7	Vcc	V12
Release	V5	SysAD56	T10	Vcc	V14
Reset	U16	SysAD57	T11	Vcc	V17
SyncIn	J16	SysAD58	U13	Vss	A3
SyncOut	P16	SysAD59	V15	Vss	A6
SysAD0	J2	SysAD60	T15	Vss	A8
SysAD1	G2	SysAD61	U17	Vss	A10
SysAD2	E1	SysAD62	N16	Vss	A12
SysAD3	E3	SysAD63	N17	Vss	A14
SysAD4	C2	SysADC0	C8	Vss	A17
SysAD5	C4	SysADC1	G17	Vss	A18
SysAD6	B5	SysADC2	T8	Vss	B1
SysAD7	B6	SysADC3	L16	Vss	C18
SysAD8	B9	SysADC4	B8	Vss	D1
SysAD9	B11	SysADC5	H16	Vss	F18
SysAD10	C12	SysADC6	U8	Vss	G1
SysAD11	B14	SysADC7	L17	Vss	H18
SysAD12	B15	SysCmd0	E2	Vss	J1
SysAD13	C16	SysCmd1	D3	Vss	K18
SysAD14	D17	SysCmd2	B2	Vss	L1
SysAD15	E18	SysCmd3	A5	Vss	M18
SysAD16	K2	SysCmd4	B7	Vss	N1
SysAD17	M2	SysCmd5	C9	Vss	P18
SysAD18	P1	SysCmd6	B10	Vss	R18
SysAD19	P3	SysCmd7	B12	Vss	T1
SysAD20	T2	SysCmd8	C13	Vss	U18
SysAD21	T4	SysCmdP	C14	Vss	V1
SysAD22	U5	TClock0	C17	Vss	V2
SysAD23	U6	TClock1	D16	Vss	V4
SysAD24	U9	VCCOk	M17	Vss	V7
SysAD25	U11	ValidIn	P2	Vss	V9
SysAD26	T12	ValidOut	R3	Vss	V11
SysAD27	U14	WrRdy	C5	Vss	V13
SysAD28	U15	VccP	K17	Vss	V16
				Vss	V18

2884 tbl 16

PHYSICAL SPECIFICATIONS

2884 drw 14

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IDT79R4400/RV4400 MC/SC PACKAGE PINOUT

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
ColdReset	AW37	SCDChk9	N37	SCData53	AR13
ExtRqst	AV2	SCDChk10	AU17	SCData54	AR15
Fault	C39	SCDChk11	AG37	SCData55	AT18
Reserved (NC)	AV24	SCDChk12	E19	SCData56	AU23
IOIn	AV32	SCDChk13	R35	SCData57	AT26
IOOut	AV28	SCDChk14	AR19	SCData58	AR27
Int0	AL1	SCDChk15	AE35	SCData59	AN29
IvdAck(1)	AA35	SCData0	R3	SCData60	AP32
IvdErr(1)	AA39	SCData1	R7	SCData61	AN35
JTCK	U39	SCData2	L5	SCData62	AJ35
JTDI	N39	SCData3	F8	SCData63	AE33
JTDO	J39	SCData4	C9	SCData64	V4
JTMS	G37	SCData5	F12	SCData65	R5
MasterClock	AA37	SCData6	G15	SCData66	N5
MasterOut	AJ39	SCData7	E17	SCData67	E5
ModeClock	B8	SCData8	G21	SCData68	G9
ModeIn	AV8	SCData9	C25	SCData69	E11
NMI	AV16	SCData10	G25	SCData70	G13
PLLCap0	****	SCData11	E29	SCData71	D14
PLLCap1	****	SCData12	G31	SCData72	C21
RClock0	AM34	SCData13	C35	SCData73	D22
RClock1	AL33	SCData14	K36	SCData74	E25
RdRdy	AW7	SCData15	N35	SCData75	G27
Release	AV12	SCData16	AE3	SCData76	C31
Reset	AU39	SCData17	AG5	SCData77	F32
Reserved (NC)	Y2	SCData18	AK4	SCData78	J35
SCAPar0	U5	SCData19	AN9	SCData79	M34
SCAPar1	U1	SCData20	AU9	SCData80	AC7
SCAPar2	P4	SCData21	AN13	SCData81	AE5
SCAddr1	AL5	SCData22	AT14	SCData82	AG7
SCAddr2	AG1	SCData23	AR17	SCData83	AR5
SCAddr3	AE7	SCData24	AT22	SCData84	AR9
SCAddr4	AC1	SCData25	AU25	SCData85	AR11
SCAddr5	AC5	SCData26	AN27	SCData86	AN15
SCAddr6	AC3	SCData27	AR29	SCData87	AP16
SCAddr7	AA1	SCData28	AN31	SCData88	AU21
SCAddr8	AB4	SCData29	AR35	SCData89	AN23
SCAddr9	AA5	SCData30	AK36	SCData90	AR25
SCAddr10	AA7	SCData31	AG35	SCData91	AP28
SCAddr11	AA3	SCData32	T6	SCData92	AU31
SCAddr12	W3	SCData33	L3	SCData93	AR33
SCAddr13	Y6	SCData34	L7	SCData94	AL35
SCAddr14	W5	SCData35	E7	SCData95	AH34
SCAddr15	W7	SCData36	G11	SCData96	U7
SCAddr16	W1	SCData37	E13	SCData97	N3
SCAddr17	U3	SCData38	E15	SCData98	N7
SCAddr0W	AN7	SCData39	G17	SCData99	C5
SCAddr0X	AN5	SCData40	C23	SCData100	E9
SCAddr0Y	AM6	SCData41	F24	SCData101	C11
SCAddr0Z	AL7	SCData42	E27	SCData102	C13
SCDCS	M6	SCData43	D30	SCData103	F16
SCDChk0	G19	SCData44	C33	SCData104	E21
SCDChk1	T34	SCData45	E35	SCData105	G23
SCDChk2	AP20	SCData46	L35	SCData106	C27
SCDChk3	AD34	SCData47	R33	SCData107	F28
SCDChk4	C19	SCData48	AF4	SCData108	E31
SCDChk5	R37	SCData49	AJ3	SCData109	G33
SCDChk6	AU19	SCData50	AJ7	SCData110	J37
SCDChk7	AE37	SCData51	AP8	SCData111	N33
SCDChk8	C17	SCData52	AT10	SCData112	AD6

2884 tbl 17

IDT79R4400/RV4400 MC/SC PACKAGE PINOUT (continued)

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
SCData113	AG3	Status7	AC33	SysAD57	AW27
SCData114	AJ5	SyncIn	W39	SysAD58	AW31
SCData115	AU5	SyncOut	AN39	SysAd59	AW35
SCData116	AN11	SysAD0	T2	SysAD60	AU37
SCData117	AU11	SysAD1	M2	SysAD61	AR39
SCData118	AU13	SysAD2	J3	SysAD62	AL39
SCData119	AN17	SysAD3	G3	SysAD63	AG39
SCData120	AR21	SysAD4	C1	SysADC0	A17
SCData121	AP24	SysAD5	A3	SysADC1	R39
SCData122	AU27	SysAD6	A9	SysADC2	AW17
SCData123	AT30	SysAD7	A13	SysADC3	AD38
SCData124	AU33	SysAD8	A21	SysADC4	A19
SCData125	AN33	SysAD9	A25	SysADC5	T38
SCData126	AL37	SysAD10	A29	SysADC6	AW19
SCData127	AG33	SysAD11	A33	SysADC7	AC39
$\overline{\text{SCOE}}$	N1	SysAd12	B38	SysCmd0	G1
$\overline{\text{SCTCS}}$	J1	SysAD13	E37	SysCmd1	E3
SCTChk0	AN21	SysAD14	G39	SysCmd2	B2
SCTChk1	AN19	SysAD15	L39	SysCmd3	B12
SCTChk2	AU15	SysAD16	AD2	SysCmd4	B16
SCTChk3	AP12	SysAD17	AH2	SysCmd5	B20
SCTChk4	AU7	SysAD18	AL3	SysCmd6	B24
SCTChk5	AR7	SysAD19	AN3	SysCmd7	B28
SCTChk6	AH6	SysAD20	AU1	SysCmd8	B32
SCTag0	K4	SysAD21	AW3	SysCmdP	A37
SCTag1	G7	SysAD22	AW9	TClock0	H34
SCTag2	C7	SysAD23	AW13	TClock1	J33
SCTag3	D10	SysAD24	AW21	VCCOk	AE39
SCTag4	C15	SysAD25	AW25	$\overline{\text{ValidIn}}$	AN1
SCTag5	D18	SysAD26	AW29	$\overline{\text{ValidOut}}$	AR3
SCTag6	F20	SysAD27	AW33	$\overline{\text{WrRdy}}$	A7
SCTag7	E23	SysAD28	AV38	VccSense	W33
SCTag8	D26	SysAD29	AR37	VssSense	U37
SCTag9	C29	SysAD30	AM38	VccP	AA33
SCTag10	G29	SysAD31	AH38	VssP	Y34
SCTag11	E33	SysAD32	R1	Vcc	A39
SCTag12	G35	SysAD33	L1	Vcc	B6
SCTag13	L33	SysAD34	H2	Vcc	B10
SCTag14	L37	SysAD35	E1	Vcc	B18
SCTag15	P36	SysAD36	C3	Vcc	B26
SCTag16	AF36	SysAD37	A5	Vcc	B34
SCTag17	AJ37	SysAD38	A11	Vcc	D4
SCTag18	AJ33	SysAd39	A15	Vcc	D8
SCTag19	AN37	SysAD40	A23	Vcc	D16
SCTag20	AU35	SysAD41	A27	Vcc	D24
SCTag21	AR31	SysAd42	A31	Vcc	D32
SCTag22	AU29	SysAD43	A35	Vcc	D36
SCTag23	AN25	SysAd44	C37	Vcc	F2
SCTag24	AR23	SysAD45	E39	Vcc	F14
$\overline{\text{SCWrW}}$	J5	SysAD46	H38	Vcc	F22
$\overline{\text{SCWrX}}$	J7	SysAD47	M38	Vcc	F30
$\overline{\text{SCWrY}}$	H6	SysAD48	AE1	Vcc	F38
$\overline{\text{SCWrZ}}$	G5	SysAD49	AJ1	Vcc	H4
Status0	U33	SysAD50	AM2	Vcc	H36
Status1	U35	SysAD51	AR1	Vcc	K6
Status2	V36	SysAD52	AU3	Vcc	K38
Status3	W35	SysAD53	AW5	Vcc	P2
Status4	W37	SysAD54	AW11	Vcc	P34
Status5	AC37	SysAD55	AW15	Vcc	T4
Status6	AC35	SysAD56	AW23		

2884 tbl 18

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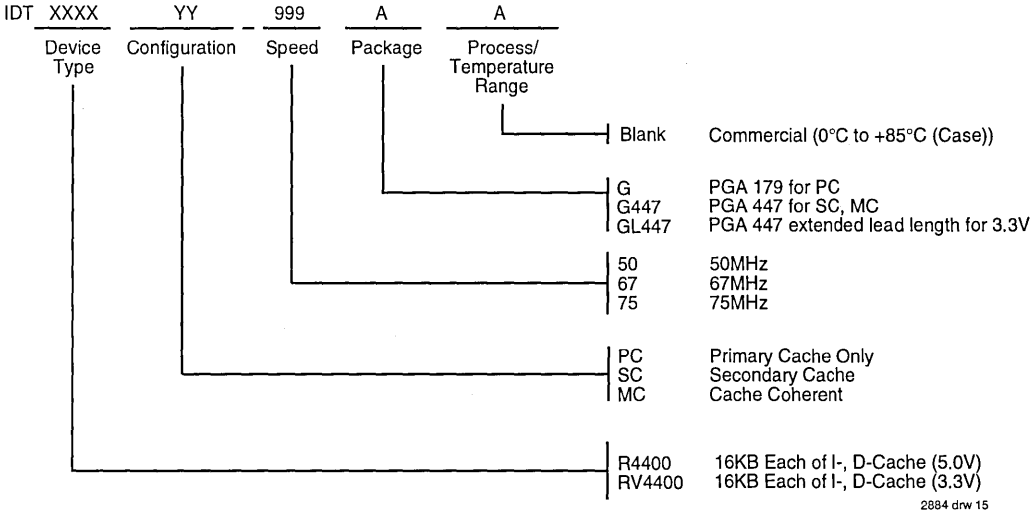
IDT79R4400 MC/SC PACKAGE PINOUT (continued)

R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin	R4400 Function	SC/MC Pkg Pin
Vcc	T36	Vcc	AV34	Vss	Y4
Vcc	V6	Vcc	AW1	Vss	Y36
Vcc	V38	Vcc	AW39	Vss	AB6
Vcc	Y38	Vss	B4	Vss	AB36
Vcc	AB2	Vss	B14	Vss	AB38
Vcc	AB34	Vss	B22	Vss	AF2
Vcc	AD4	Vss	B30	Vss	AF34
Vcc	AD36	Vss	B36	Vss	AH4
Vcc	AF6	Vss	D2	Vss	AH36
Vcc	AF38	Vss	D6	Vss	AK6
Vcc	AK2	Vss	D12	Vss	AK38
Vcc	AK34	Vss	D20	Vss	AP4
Vcc	AM4	Vss	D28	Vss	AP6
Vcc	AM36	Vss	D34	Vss	AP14
Vcc	AP2	Vss	D38	Vss	AP22
Vcc	AP10	Vss	F4	Vss	AP30
Vcc	AP18	Vss	F6	Vss	AP34
Vcc	AP26	Vss	F10	Vss	AP36
Vcc	AP38	Vss	F18	Vss	AT2
Vcc	AT4	Vss	F26	Vss	AT6
Vcc	AT8	Vss	F34	Vss	AT12
Vcc	AT16	Vss	F36	Vss	AT20
Vcc	AT24	Vss	K2	Vss	AT28
Vcc	AT32	Vss	K34	Vss	AT34
Vcc	AT36	Vss	M4	Vss	AT38
Vcc	AV6	Vss	M36	Vss	AV4
Vcc	AV14	Vss	P6	Vss	AV10
Vcc	AV20	Vss	P38	Vss	AV18
Vcc	AV22	Vss	V2	Vss	AV26
Vcc	AV30	Vss	V34	Vss	AV36

2884 tbl 19

NOTE:
1. Available in IDT79R4400MC only. For IDT79R4400SC, these inputs must be pulled to Vcc.

ORDERING INFORMATION



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VALID COMBINATIONS

R4400 PC — 50, 67, 75	G
R4400 SC — 50, 67, 75	G447
R4400 MC — 50, 67, 75	G447
RV4400 SC — 50, 67, 75, 100	GL447
RV4400 MC — 50, 67, 75, 100	GL447

Integrated Device Technology, Inc.

FOURTH GENERATION 64-BIT RISC MICROPROCESSOR

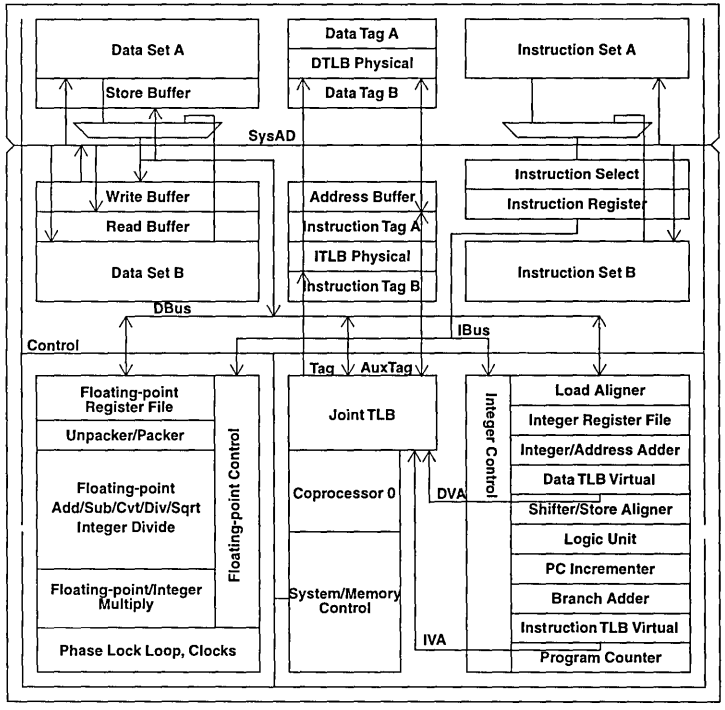
ORION™

IDT79R4600™

FEATURES:

- True 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit floating-point operations
  - 64-bit registers
  - 64-bit virtual address space
- High-performance microprocessor
  - 150 peak MIPS at 150MHz
  - 50peak MFLOP/s at 150MHz
  - 96 SPECint92 at 150Mz
  - Two-way set associative caches
- High level of integration
  - 64-bit integer CPU
  - 64-bit floating-point unit
  - 16KB instruction cache; 16KB data cache
  - Flexible MMU with large TLB
- Low-power operation
  - 3.3V or 5V power supply options
  - 20mW/MHZ typical internal power dissipation (2.0W @ 100MHz, 3.3V)
  - Standby mode reduces internal power to 90mA @ 5V and 60mA @ 3.3V (450mW @ 5V and 400mW @ 3.3V).
- Standard operating system support includes:
  - Microsoft Windows™ NT
  - UNISOFT Unix™ System V.4
- Fully software compatible with R4400 RISC Processor Family
- Available in R4000PC/R4400PC pin-compatible 179-pin PGA or 208-pin MQUAD
- 50MHz and 67MHz input frequencies with mode bit dependent output clock frequencies
  - On-chip clock doubler for 133MHz pipeline
- 64GB physical address space
- Processor family for a wide variety of applications
  - Desktop workstations and PCs
  - Deskside or departmental servers
  - High-performance embedded applications (e.g. color printers, multi-media and internetworking.)
  - Notebooks

BLOCK DIAGRAM:



3038 drw 01

DESCRIPTION:

The IDT79R4600 supports a wide variety of processor-based applications, from 32-bit Windows NT desktop or notebook systems through high-performance, 64-bit OLTP systems. Compatible with the IDT79R4000PC family for both hardware and software, the R4600 will serve in many of the same applications, but, in addition supports low-power operation for applications such as "green" desktops and notebook computers. It does not provide integrated secondary cache and multiprocessor support as found in the R4000SC and R4000MC, but an external secondary cache can lastly be designed around it. The large on-chip two-way set associative caches make this unnecessary in most embedded control applications.

The R4600 brings R4000SC performance levels to the R4000PC package, while at the same time providing lower cost and lower power. It does this by providing larger on-chip caches that are two-way set associative, fewer pipeline stalls, and early restart for data cache misses. The result is 102 SPECint92 and >90SPECfp92 (exact figures are system-dependent).

The R4600 provides complete upward application-software compatibility with the IDT79R3000™ family of microprocessors, including the IDT RISController™ 79R3051™/R3052™/R3041™/R3071™/R3081™ as well as the IDT79R4000 family of microprocessors. Microsoft Windows NT and UNISOFT Unix V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4600-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

Together with the R4000 family, the R4600 provides a compatible, timely, and necessary evolution path from 32-bit to true, 64-bit computing. The original design objectives of the R4000 clearly mandated this evolution path; the result is a true 64-bit processor fully compatible with 32-bit operating systems and applications.

The 64-bit computing and addressing capability of the R4600 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the R4600 CPU. A more detailed description of the processor is available in the *"IDT79R4600 Processor Hardware User's Manual"*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

HARDWARE OVERVIEW

The R4600 family brings a high-level of integration designed for high-performance computing. The key elements of the R4600 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

5

Pipeline

The R4600 uses a 5-stage pipeline similar to the IDT79R3000. The simplicity of this pipeline allows the R4600 to be lower cost and lower power than super-scalar or super-pipelined processors. Unlike the R3000, the R4600 does virtual-to-physical translation in parallel with cache access. This allows the R4600 to operate at twice the frequency of the R3000 and to support a larger TLB for address translation.

Compared to the 8-stage R4000 pipeline, the R4600 is more efficient (requires fewer stalls).

Figure 2 shows the R4600 pipeline.

Figure 1. CPU Registers

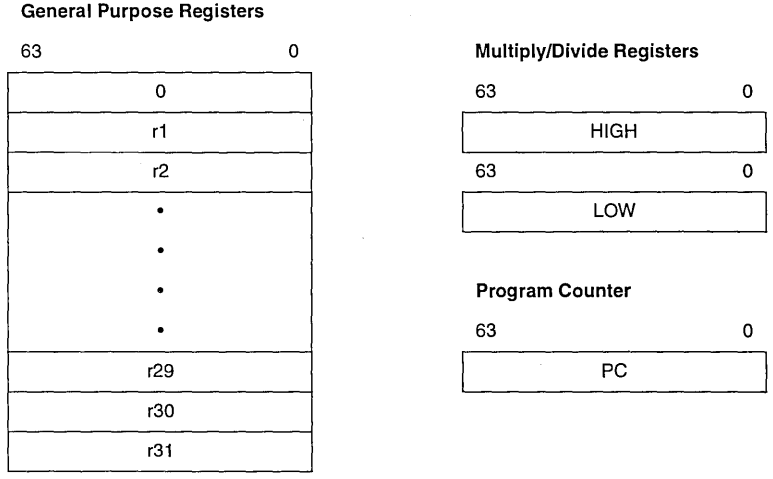
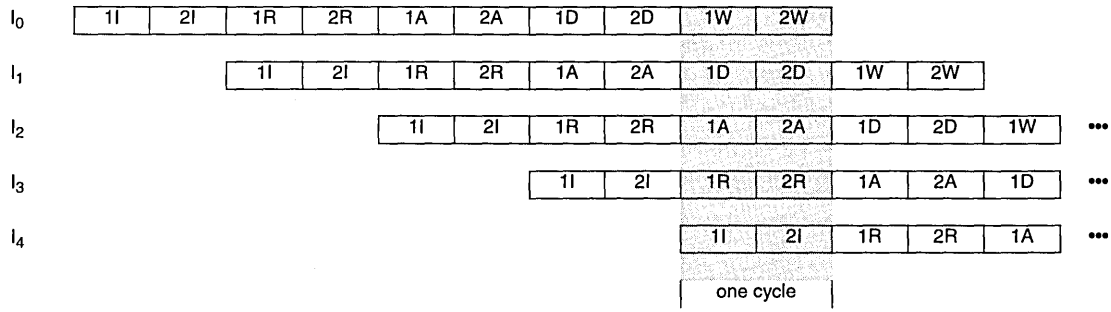


Figure 2. R4600 Pipeline



1I-1R	Instruction cache access
2I	Instruction virtual to physical address translation in ITLB
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation in DTLB
1D-2D	Virtual to physical address translation in JTLB
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Integer Execution Engine

The R4600 implements the MIPS Instruction Set architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4600 includes the same additions to the instruction set as found in the R4000 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions have been defined to take advantage of the 64-bit architecture of the processor. When operating as a 32-bit processor, the R4600 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The register resources include: 32 general-purpose orthogonal integer registers, the HIGH/LOW result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

Register File

The R4600 has thirty-two general-purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

ALU

The R4600 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

Integer Multiply/Divide

The R4600 uses the floating-point unit to perform integer multiply and divide. The results of the operation are placed in the *HIGH* and *LOW* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. Table 1 below shows the number of processor internal cycles required between an integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs.

Table 1: Integer multiply/divide cycles

	32-bit	64-bit
MULT	8 or 11	10 or 13
DIV	42	74

Floating-Point Co-Processor

The R4600 incorporates an entire floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

Floating-Point Units

The R4600 floating-point execution units supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 6 cycles.

As in the IDT79R3010A and IDT79R4000, the R4600 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with the IEEE Standard 754.

Table 2 below gives the latencies of some of the floating-point instructions in internal processor cycles.

Table 2: Floating-Point Cycles

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	8	8
DIV	32	61
SQRT	31	60
CMP	3	3
FIX	4	4
FLOAT	6	6
ABS	1	1

Table 2: Floating-Point Cycles

Operation	Single Precision	Double Precision
MOV	1	1
NEG	1	1
LWC1, LDC1	2	2
SWC1, SDC1	1	1

Floating-Point General Register File

The floating-point register file is made up of thirty-two 64-bit registers. With the LDC1 and SDC1 instructions the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store double-word instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

5

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4600 CP0 is essentially identical to that of the R4000PC, except that the WatchLo and WatchHi registers are no longer present and the Index CACHE ops use an extra address bit to select one of the two sets (the R4000 caches are direct mapped, instead of two-way set associative).

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer (the ITLB), a data address translation buffer (the DTLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

System Control Co-Processor Registers

The R4600 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4600 includes registers to implement a real-time cycle counting facility, to aid in cache diagnostic testing, and to assist in data error detection.

Figure 3 shows the CP0 registers.

Virtual to Physical Address Mapping

The R4600 provides three modes of virtual addressing:

- user mode
- supervisor mode
- kernel mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4600 provides a single, uniform virtual address space of 256GB (2GB for 32-bit mode).

When operating in the kernel mode, four distinct virtual address spaces, totalling 1024GB (4GB in 32-bit mode), are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4600 processors also support a supervisor mode in which the virtual address space is 256.5GB (2.5GB in 32-bit mode), divided into three regions based on the high-order bits of the virtual address.

Figure 4 shows the address space layout for 32-bit operation.

When the R4600 is configured as a 64-bit microprocessor, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout.

Joint TLB

For fast virtual-to-physical address decoding, the R4600 uses a large, fully associative TLB which maps 96 Virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory mapped using only one TLB entry.

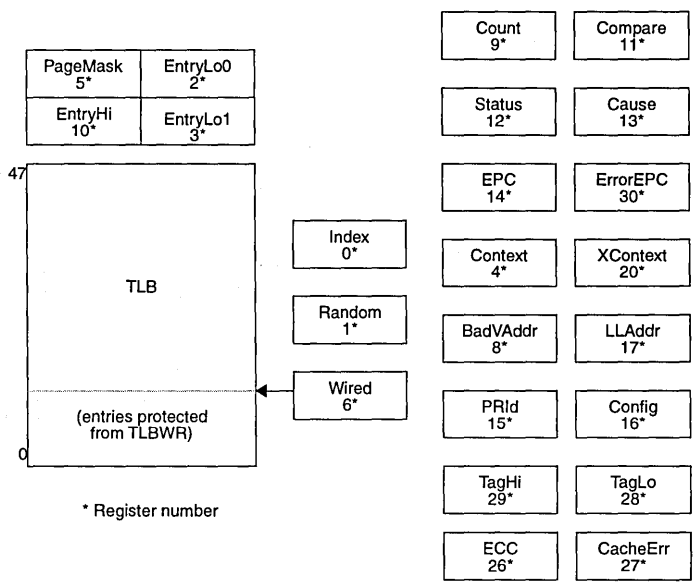
The second mechanism controls the replacement algorithm when a TLB miss occurs. The R4600 provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, non-coherent write-back, non-coherent write-through write-allocate, non-coherent write-through no write-allocate. Non-coherent write-back is typically used for both code and data on the R4600; the write-through modes support more efficient frame buffer accesses than the R4000 family, cache coherency is not supported, however.

Instruction TLB

The R4600 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address

Figure 3. The R4600 CP0 Registers



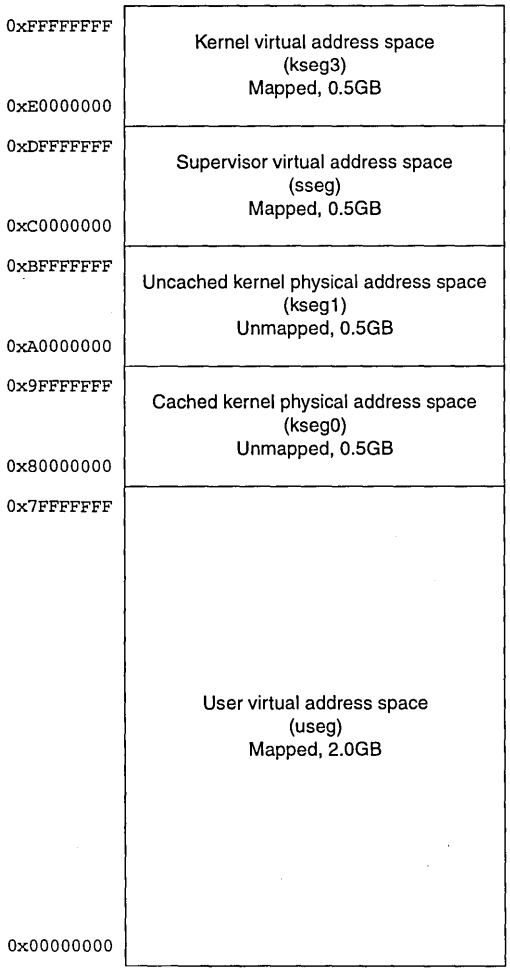
translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is invisible to the user.

Data TLB

The R4600 also incorporates a 4-entry data TLB. Each entry maps a 4KB page. The data TLB improves performance by allowing data address translation to occur in parallel with data address translation. When a miss occurs on an data address translation, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used half is filled. The operation of the DTLB is invisible to the user.

Furthermore, the large 2-way set-associative caches increase emulation performance of DOS and Windows 3.1 applications when running under Windows NT.

Figure 4. Kernel Mode Virtual Addressing (32-bit mode)



Cache Memory

In order to keep the R4600's high-performance pipeline full and operating efficiently, the R4600 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2.4GB per second at a pipeline-clock frequency of 150MHz.

Instruction Cache

The R4600 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 600MB/sec at 150MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill writes 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

Data Cache

For fast, single cycle data access, the R4600 includes a 16KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through on a per-page basis when it is appropriate, such as for frame buffers.

Associated with the Data Cache is the store buffer. When the R4600 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4600 to execute a store every processor cycle and to perform back-to-back stores without penalty.

Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses,

use the on-chip write buffer. The write buffer holds up to four 64-bit address and data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

System Interface

The R4600 supports a 64-bit system interface that is compatible with the R4000PC system interface. This interface operates from two clocks provided by the R4600, TClock[1:0] and RClock[1:0], at some division of the internal clock.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 600MB/sec at 150MHz.

Figure 5 on page 7 shows a typical system using the R4600. In this example two banks of DRAMs are used to supply and accept data with a DDxxDD data pattern.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4600 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4600 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4600. Again, the system designer has the flexibility to make these price/performance trade-offs.

System Command Bus

The R4600 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4600. Processor requests are initiated by the R4600 and responded to by an external device. External requests are issued by an external device and require the R4600 to respond.

The R4600 supports one to eight byte and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

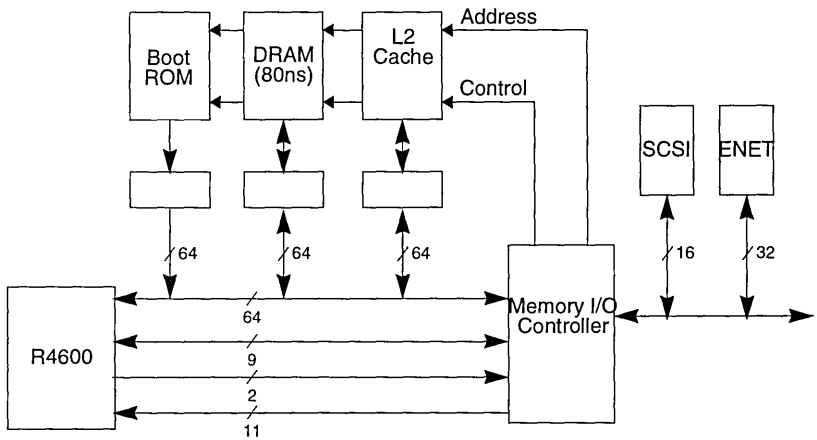
Handshake Signals

There are six handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the R4600 whether it can accept a new read or write transaction. The R4600 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$ and $\overline{\text{Release}}$ are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{\text{ExtRqst}}$. The R4600 responds by asserting $\overline{\text{Release}}$ to release the system interface to slave state.

$\overline{\text{ValidOut}}$ and $\overline{\text{ValidIn}}$ are used by the R4600 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4600 asserts $\overline{\text{ValidOut}}$ when it is driving these buses with a valid command or data, and the external device drives

Figure 5. Typical Desktop System Block Diagram



ValidIn when it has control of the buses and is driving a valid command or data.

Non-overlapping System Interface

The R4600 requires a non-overlapping system interface, compatible with the R4000PC. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4600 issues another request. The R4600 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4600.

The R4600 asserts ValidOut and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release. The external device can then begin sending the data to the R4600.

Figure 6 on page 8 shows a processor block read request and the external agent read response. The read latency is 4 cycles (ValidOut to ValidIn), and the response data pattern is DDxxDD. Figure 6 on page 8 shows a processor block write.

External Requests

The R4600 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4600 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue requests to the processor, such as a request for the R4600 to write to the R4600 interrupt register.

The following is a list of the supported external requests:

- Write
- Null

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the VccOK Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG Interface

For compatibility with the R4000PC, the R4600 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

Boot-Time Modes

The boot-time serial mode stream is defined in Table 3 below. Bit 0 is the bit presented to the processor when VccOK is asserted; bit 255 is the last.

Power Management

CP0 is also used to control the power management for the R4600. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU. The standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by any interrupt.

Figure 6. Processor Block Read

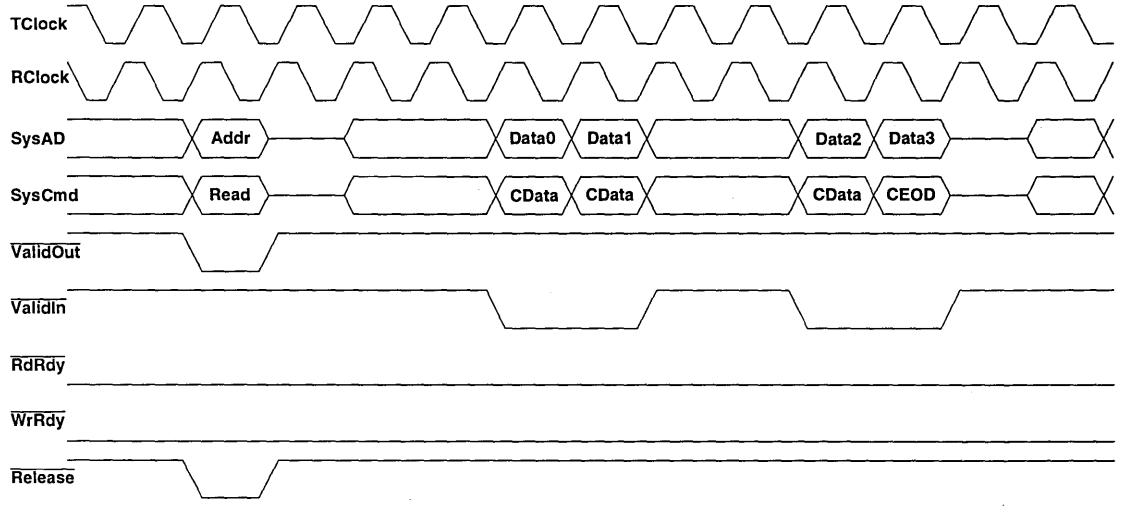


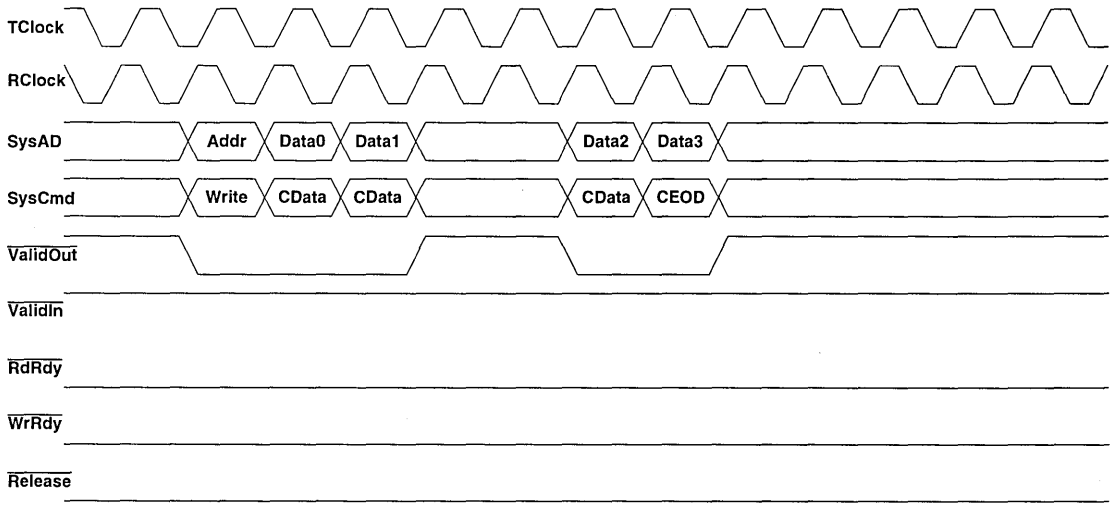
Table 3: Boot time mode stream

Mode bit	Description
0	reserved (must be zero)
4..1	Writeback data rate 0 → D, 1 → DDx, 2 → DDxx, 3 → DxDx, 4 → DDxxx, 5 → DDxxxx, 6 → DxxDxx, 7 → DDxxxxxx, 8 → DxxxDxxx, 9-15 reserved
7..5	Clock divisor 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved
8	0 → Little endian, 1 → Big endian
10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue

Table 3: Boot time mode stream

Mode bit	Description
11	Disable the timer interrupt on Int[5]. 0 → Enabled 1 → Disabled
12	reserved (must be zero)
14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)
	Reserved
bit 15*	0 -> TClock[0] enabled
	1 -> TClock[0] disabled
bit 16*	0 -> TClock[1] enabled
	1 -> TClock[1] disabled
bit 17*	0 -> RClock[0] enabled
	1 -> RClock[0] disabled
bit 18*	0 -> RClock[1] enabled
	1 -> RClock[1] disabled
255..19	must be zero
*	valid for rev 2.0 only, otherwise must be zero

Figure 7. Processor Block Write



Comparison of R4600/R4700 and R4400

This section compares features of the R4600/R4700 to the earlier R4400 PC. Table 1.20 to Table 1.26 highlight some of the differences between the R4600/R4700 and the R4400 PC. This list is not exhaustive.

Table 4: System interface comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
I/O	R4400: TTL compatible RV4400: LV CMOS	R4600/R4700: TTL-compatible (5V ±0.5%) RV4600/RV4700: LVCMOS (3.3V±0.3V)
Package	179-pin ceramic PGA	179-pin PGA and 208-pin MQUAD
JTAG	yes	no (serial out connected directly to serial in)
Block transfer sizes	16B or 32B	32B
Sclock divisor	2, 3, 4, 6, 8	2, 3, 4, 5, 6, 7, 8
Non-block writes	max throughput of 4 sclock cycles	two new system interface protocol options that support 2 sclock cycle throughput (remains 4 in compatibility mode)
Serial configuration	as described in *R4000 User's Guide*	different, as described in Table 9.2 on page 9-7
Address bits 63..56 on reads and writes	zero	bits 19..12 of virtual address
Uncached and write-through stores	uncached stores are buffered in 1-entry uncached store buffer (write through not possible)	uncached and write-though stores buffered in 4-entry write buffer
SysADC	parity only	same
SysADC for non-data cycles	parity	zero
SysCmdP	parity	zero
Parity error during writeback	use Cache Error exception	output bad parity
Error bit in data identifier of read responses	Bus Error if error bit set for any double-word	only check error bit of first doubleword; all other error bits ignored
Parity error on read data	Bus Error if parity error in any doubleword	bad parity written to cache; take Cache Error exception if bad parity occurs on doublewords that the processor is waiting for
Block writes	1-2 null cycles between address and data	0 cycles between address and data
Release after Read Request	variable latency	0 latency
SysAD value for x cycles of write-back data pattern	data bus undefined	data bus maintains last D cycle value
SysAD bus use after last D cycle of writeback	data bus undefined	trailing x cycles (e.g. DDxxDDxx, not DDxxDD) follow rule in entry immediately preceding
Output slew rate	dynamic feedback control	simple CMOS output buffers with 2-bit static strength control
IOOut output	output slew rate control feedback loop output	driven HIGH, do not connect (reserved for future output)
IOIn input	output slew rate control input	should be driven high (reserved for future input)
GrpRunB output	do not connect	same (reserved for future output)
GrpStallB input	should be connected to VCC	same (reserved for future input)
FaultB output pin	indicates compare mismatch	driven HIGH, do not connect (reserved for future output)

Table 5: Cache comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
Cache Sizes	16KB Instruction cache, 16KB Data cache	16KB Instruction cache, 16KB Data cache
Cache Line Sizes	software selectable between 16B and 32B	fixed at 32B
Cache Index	$vAddr_{13..0}$	$vAddr_{12..0}$
Cache Tag	$pAddr_{35..12}$	same
Cache Organization	direct mapped	2-way set associative
Data cache write policy	write-allocate and write-back	write-allocate or not based on TLB entry, write-through or not based on TLB entry
Data cache miss	stall, output address, copy dirty data to writeback buffer, refill cache, output write-back data	same, with FIFO to select the set to refill
Data order for block reads	sub-block ordering	same
Data order for block writes	sequential	same
Instruction cache miss restart	restart after all data received and written to cache	same
Data cache miss restart	restart after all data received and written to cache	restart on first doubleword, send subsequent doublewords to response buffer
Instruction Tag	2-bit cache state	1-bit cache state
Cache miss overhead	5-8 cycles	3 cycles
Instruction cache parity	1 parity bit per 8 data bits	1 parity bit per 32 data bits
Data cache parity	1 parity bit per 8 data bits	same

Table 6: TLB comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
Instruction virtual address translation	2-entry ITLB	same
ITLB miss	1 cycle penalty, refilled from JTLB, LRU replacement	1 cycle on branch, jump, and ERET, 2 cycles otherwise, refilled from JTLB, LRU replacement
Data virtual address translation	done directly in JTLB	4-entry DTLB
DTLB miss	n.a.	1 cycle penalty, refilled from JTLB, pseudo-LRU replacement
JTLB	48 entries of even/odd page pairs, fully associative	same
Page size	4KB, 16KB, ..., 16MB	same
Multiple entry match in JTLB	sets TS in Status and disables TLB until Reset to prevent damage	no damage for multiple match; no detection or shutdown implemented
Virtual address size	VSIZE = 40	same
Physical address size	PSIZE = 36	same

Table 7: Pipeline comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
ALU latency	1 cycle	1 cycle
Load latency	3 cycles	2 cycles
Branch latency	4 cycles (2 cycle penalty for taken branches)	2 cycles (no penalty for taken branches)
Store buffer (not write buffer)	2 doublewords	1 doubleword
Integer multiply	integer multiply hardware, 1 cycle to issue	done in floating-point multiplier, 4 cycles to issue
Integer divide	done in integer datapath adder, slips until done	done in floating-point adder, 4 cycles to issue
Integer multiply	HIGH and LOW available at the same time	LOW available one cycle before HIGH
Integer divide	HIGH and LOW available at the same time	HIGH available one cycle before LOW
HIGH and LOW hazards	yes, HIGH and LOW written early in pipeline	no, HIGH and LOW written after W
MFHI/MFLO latency	1 cycle	2 cycles
SLLV, SRLV, SRAV	2 cycles to issue	1 cycle to issue
DSLL, DSRL, DSRA, DSLL32, DSRL32, DSRA32, DSLLV, DSRLV, DSRAV	2 cycles to issue	1 cycle to issue

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Table 8: Coprocessor 0 comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
WatchLo, WatchHi	implemented	unimplemented (no watch registers)
Config	as described in *R4000 User's Guide*	subset
Status	as described in *R4000 User's Guide*, but RP not functional	no TS or RP
Low-power standby mode	no	WAIT instruction disables internal clock, freezing pipeline and other state; resume on interrupt
MFC0/MTC0 hazard	only hazardous for certain cp0 register combinations	always hazardous -- detected and 1-cycle slip inserted
EntryLo0, EntryLo1	as described in *R4000 User's Guide*	two new cache algorithms added to C field for non-coherent write-through
TagLo, TagHi, ECC, CacheErr	R4400SC bits implemented but meaningless	Only bits meaningful on R4400 PC implemented
TagLo	as described in *R4000 User's Guide*	bits 5..3 read/writeable but otherwise unused, bit 2 used for F bit
Exceptions	as described in *R4000 User's Guide* (VCEI and VCED not possible)	VCEI, VCED, and WATCH exceptions not implemented
Index CACHE ops I Fill CACHE op	use $vAddr_{13..4}$ to select line	use $vAddr_{13}$ to select set, $vAddr_{12..5}$ to select line of set
Index Store Tag CACHE op	Status.CE ignored	TagLo.P stored if Status.CE set
PRId	Imp = 0x04	R4600: Imp = 0x20 R4700: Imp = 0x21

Table 9: Coprocessor 1 comparison between R4400PC and R4600

Item	R4400 PC	R4600/R4700
Possible exception stall	only for operands that can cause exceptions	some simplifications in detection hardware
Floating-point divide	separate divide unit	done in floating-point adder
Floating-point square root	done in floating-point adder	same
Converts to/from 64-bit integer	uses unimplemented for integer operands/ results with more than 53 bits of precision	handles full 64-bit operands and results
Floating-point registers	Status.FR enables all 32 floating point registers	same
FCR0	Imp = 0x05	R4600: Imp = 0x20 R4700: Imp = 0x21

PIN DESCRIPTION

The following is a list of interface, interrupt, and miscellaneous pins available on the R4600.

Pin Name	Type	Description
System interface:		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity for the R4600 unused on input and zero on output.
Clock/control interface:		
MasterClock	Input	Master clock Master clock input at one half the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
IOOut	Output	Reserved for future output Always HIGH.
IOIn	Input	Reserved for future input Should be driven HIGH.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.

Pin Name	Type	Description
Fault*	Output	Fault Always HIGH.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.
Interrupt interface:		
Int*(5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Initialization interface:		
Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4600 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset. ColdReset must be de-asserted synchronously with MasterOut.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterOut.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

Standby Mode Operations

The R4600 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as "Standby Mode" .

Entering Standby Mode

Executing the WAIT iunstruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, some of the input pin clocks (Int[5:0]*, NMI*, ExtRqst*, Reset*, and ColdReset*) and the output clocks (TClock[1:0], RClock[1:0], SyncOut, Modeclock and MasterOut) will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (i.e. the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt or ExtRqst*, will cause the CPU to exit Standby Mode.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	RV4600 3.3V±5%	R4600 5.0V±5%	
		Commercial	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	−0.5(2) to +4.6	−0.5(2) to +7.0	V
T_C	Operating Temperature (case)	0 to +85	0 to +85	°C
T_{BIAS}	Case Temperature Under Bias	−55 to +125	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	−55 to +125	°C
I_{IN}	DC Input Current	20(3)	20(3)	mA
I_{OUT}	DC Output Current	50	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = −2.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. When V_{IN} < 0V or V_{IN} > V_{CC}
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V_{CC}	
			RV4600	R4600
Commercial	0°C to +85°C (Case)	0V	3.3V±5%	5.0V±5%

DC ELECTRICAL CHARACTERISTICS — COMMERICAL TEMPERATURE RANGE RV4600

(V_{cc} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RV4600 100MHz		RV4600 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
V_{OHC}	—	—	—	—	—
V_{ILC}	—	—	—	—	—
V_{IHC}	—	—	—	—	—
C_{IN}	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	Input/Output Leakage

Parameter		RV4600 100MHz		RV4600 133MHz		Conditions
		Typical[12]	Maximum	Typical[12]	Maximum	
System Condition:		100/50MHz		133/44MHz		—
I_{CC}	standby	—	125mA	—	175mA	C_L = 0pF[11]
		—	175mA	—	225mA	C_L = 50pF
	active	575mA	875mA	775mA	1150mA	C_L = 0pF, No SysAd activity[11]
		650mA	1100mA	850mA	1375mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		650mA	1275mA	850mA	1525mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C

AC ELECTRICAL CHARACTERISTICS — COMMERICAL TEMPERATURE RANGE RV4600

(V_{CC}=3.3V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters

Parameter	Symbol	Test Conditions	RV4600 100MHz		RV4600 133MHz		Units
			Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock Frequency(5)	—	—	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(11)	—	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$(11)	—	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}(11)	—	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(11)	—	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTES:

5. Operation of the R4600 is only guaranteed with the Phase Lock Loop enabled.

System Interface Parameters(6)

Parameter	Symbol	Test Conditions	RV4600 100MHz (V_{CC}= 3.3±5%)		RV4600 133MHz (V_{CC}= 3.3±5%)		Units
			Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	3.5	—	3.5	—	ns
Data Hold	t_{DH}		1.5	—	1.5	—	ns

Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	RV4600 100MHz		RV4600 133MHz		Units
			Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	Master Clock Cycle

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Capacitive Load Deration

Parameter	Symbol	RV4600 100MHz		RV4600 133MHz		Units
		Min	Max	Min	Max	
Load Derate	C_{LD}	—	2	—	2	ns/25pF

DC ELECTRICAL CHARACTERISTICS — COMMERICAL TEMPERATURE RANGE R4600

(V_{CC}= 5.0±5%, T_{CASE} = 0°C to +85°C)

Parameter	R4600 100MHz		R4600 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	3.5V	—	3.5V	—	
V_{IL}	–0.5V	0.8V	–0.5V	0.8V	—
V_{IH}	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—
I/O_{LEAK}	—	±20uA	—	±20uA	Input/Output Leakage

Parameter		R4600 100MHz		R4600 133MHz		Conditions
		Typical[12]	Maximum	Typical[12]	Maximum	
System Condition:		100/50MHz		133/44MHz		—
I_{CC}	standby	—	175mA	—	225mA	C_L = 0pF[11]
		—	250mA	—	325mA	C_L = 50pF
	active	875mA	1000mA	1175mA	1300mA	C_L = 0pF, No SysAd activity[11]
		975mA	1200mA	1275mA	1510mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		1100mA	1400mA	1300mA	1675mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C

AC ELECTRICAL CHARACTERISTICS — COMMERICAL TEMPERATURE RANGE R4600

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters

Parameter	Symbol	Test Conditions	100MHz		133MHz		Units
			Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock Frequency(5)	—	—	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(11)	—	—	±250	—,	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$(11)	—	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}(11)	—	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(11)	—	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	ns
JTAG Clock Period	$t_{JTAGCKP}$	—	—	4* t_{MCP}	—	4* t_{MCP}	ns

NOTES:

6. Operation of the R4600 is only guaranteed with the Phase Lock Loop enabled.

AC ELECTRICAL CHARACTERISTICS — COMMERICAL TEMPERATURE RANGE R4600

(V_{CC} = 5.0V ± 5%; T_{CASE} = 0°C to +85°C)

System Interface Parameters(6)

Parameter	Symbol	Test Conditions	R4600 100MHz		R4600 133MHz		Units
			Min	Max	Min	Max	
Data Output(7)	t_{DO}	$mode_{14..13}$ = 10 (fastest)	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 11	1.3	11	1.3	10	ns
		$mode_{14..13}$ = 00	1.6	13	1.6	11	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	3.5	—	3.5	—	ns
Data Hold	t_{DH}		1.5	—	1.5	—	ns

NOTES:

7. Timings are measured from 1.5V of the clock to 1.5V of the signal.
8. Capacitive load for all output timings is 50pF.
9. Timings are measured from 1.5V of the clock to 1.5V of the signal.
10. Capacitive load for all output timings is 50pF.
11. Guaranteed by Design.
12. Typical integer instruction mix and cache miss rates.

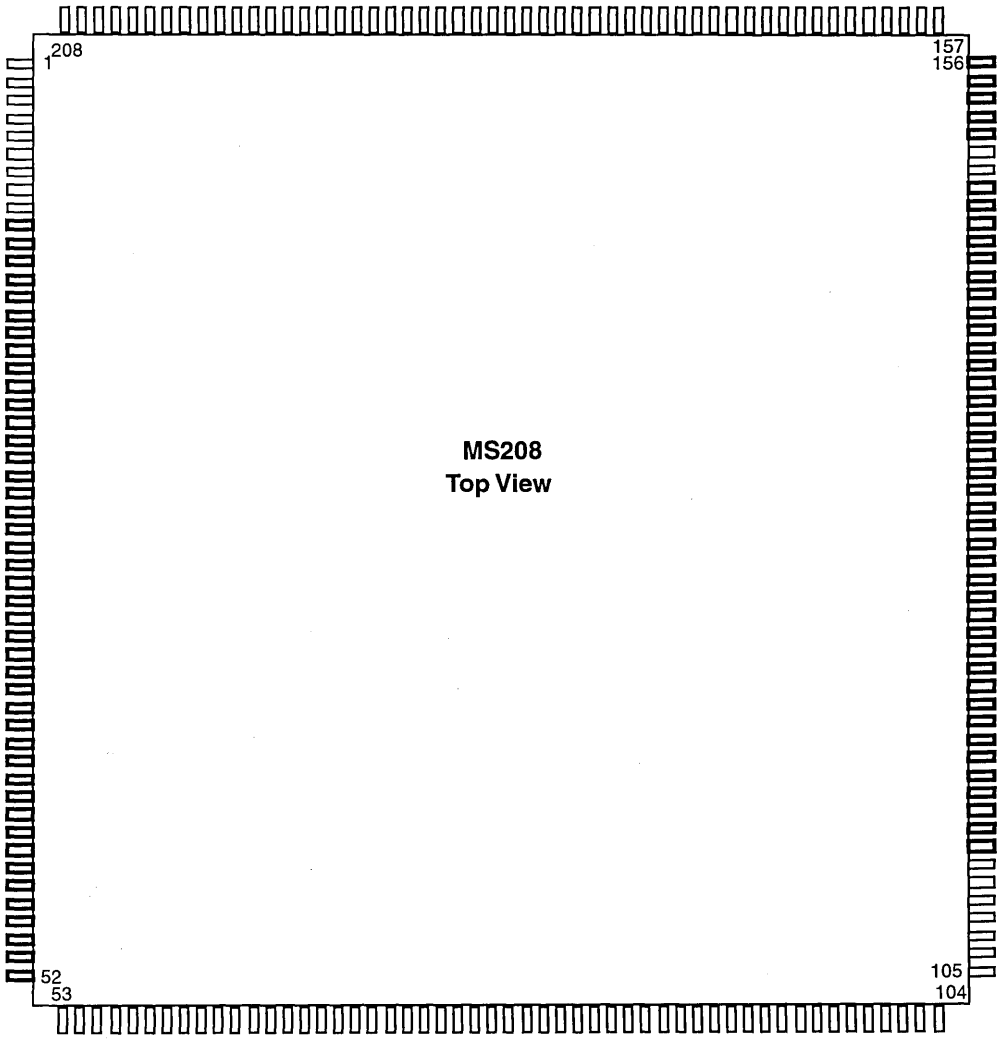
Boot Time Interface Parameters

Parameter	Symbol	Test Conditions	R4600 100MHz		R4600 133MHz		Units
			Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	MasterClock cycles
Mode Data Hold	t_{DH}	—	0	—	0	—	MasterClock cycles

CAPACITIVE LOAD DERATION

Parameter	Symbol	R4600 100MHz		R4600 133MHz		Units
		Min	Max	Min	Max	
Load Derate	C_{LD}	—	2	—	2	ns/25pF

PHYSICAL SPECIFICATIONS — MQUAD



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RV4600 MQUAD package pin-out

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	Vss	55	SysCmd2	107	N.C.	159	RClock0
4	Vcc	56	SysAD36	108	N.C.	160	RClock1
5	SysAD45	57	SysAD4	109	Vcc	161	SyncOut
6	SysAD13	58	SysCmd1	110	Vss	162	SysAD30
7	FaultB	59	Vss	111	SysAD21	163	Vcc
8	SysAD44	60	Vcc	112	SysAD53	164	Vss
9	Vss	61	SysAD35	113	RdRdyB	165	SysAD62
10	Vcc	62	SysAD3	114	ModeIn	166	MasterOut
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	Vss	117	Vcc	169	Vcc
14	SysAD11	66	Vcc	118	Vss	170	Vss
15	Vss	67	N.C.	119	ReleaseB	171	VccOK
16	Vcc	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	IntB5	122	NMIB	174	Vcc
19	SysAD10	71	SysAD33	123	Vcc	175	Vss
20	SysCmd7	72	SysAD1	124	Vss	176	N.C.
21	Vss	73	Vss	125	SysADC2	177	N.C.
22	Vcc	74	Vcc	126	SysADC6	178	N.C.
23	SysAD41	75	IntB4	127	Vcc	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	Vcc	181	VccP
26	SysAD40	78	IntB3	130	Vss	182	VssP
27	N.C.	79	Vss	131	SysAD56	183	N.C.
28	N.C.	80	Vcc	132	N.C.	184	N.C.
29	Vss	81	IntB2	133	SysAD25	185	MasterClock
30	Vcc	82	SysAD16	134	SysAD57	186	Vcc
31	SysAD8	83	SysAD48	135	Vcc	187	Vss
32	SysCmd5	84	IntB1	136	Vss	188	SyncIn
33	SysADC4	85	Vss	137	IOOut	189	Vcc
34	SysADC0	86	Vcc	138	SysAD26	190	Vss
35	Vss	87	SysAD17	139	SysAD58	191	N.C.
36	Vcc	88	SysAD49	140	IOIn	192	SysADC5
37	SysCmd4	89	IntB0	141	Vcc	193	SysADC1
38	SysAD39	90	SysAD18	142	Vss	194	N.C.
39	SysAD7	91	Vss	143	SysAD27	195	Vcc
40	SysCMD3	92	Vcc	144	SysAD59	196	Vss
41	Vss	93	SysAD50	145	ColdResetB	197	SysAD47
42	Vcc	94	ValidInB	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	Vcc	199	N.C.
44	SysAD6	96	SysAD51	148	Vss	200	SysAD46
45	ModeClock	97	Vss	149	SysAD60	201	Vcc
46	WrRdyB	98	Vcc	150	ResetB	202	Vss
47	SysAD37	99	ValidOutB	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	N.C.
49	Vss	101	SysAD52	153	Vcc	205	TClock1
50	Vcc	102	ExtRqstB	154	Vss	206	TClock0
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.C.

N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

R4600/RV4600 PGA Pin-out

Function	Pin
$\overline{\text{ColdReset}}$	T14
$\overline{\text{ExtRqst}}$	U2
$\overline{\text{Fault}}$	B16
Reserved O (NC)	U10
Reserved I (Vcc)	T9
IOIn	T13
IOOut	U12
Int0	N2
Int1	L3
Int2	K3
Int3	J3
Int4	H3
Int5	F2
JTCK	H17
JTDI	G16
JTDO	F16
JTMS	E16
MasterClock	J17
MasterOut	P17
ModeClock	B4
ModeIn	U4
NMI	U7
RClock0	T17
RClock1	R16
$\overline{\text{RdRdy}}$	T5
Release	V5
$\overline{\text{Reset}}$	U16
SyncIn	J16
SyncOut	P16
SysAD0	J2
SysAD1	G2
SysAD2	E1
SysAD3	E3
SysAD4	C2

Function	Pin
SysAD5	C4
SysAD6	B5
SysAD7	B6
SysAD8	B9
SysAD9	B11
SysAD10	C12
SysAD11	B14
SysAD12	B15
SysAD13	C16
SysAD14	D17
SysAD15	E18
SysAD16	K2
SysAD17	M2
SysAD18	P1
SysAD19	P3
SysAD20	T2
SysAD21	T4
SysAD22	U5
SysAD23	U6
SysAD24	U9
SysAD25	U11
SysAD26	T12
SysAD27	U14
SysAD28	U15
SysAD29	T16
SysAD30	R17
SysAD31	M16
SysAD32	H2
SysAD33	G3
SysAD34	F3
SysAD35	D2
SysAD36	C3
SysAD37	B3
SysAD38	C6
SysAD39	C7

Function	Pin
SysAD40	C10
SysAD41	C11
SysAD42	B13
SysAD43	A15
SysAD44	C15
SysAD45	B17
SysAD46	E17
SysAD47	F17
SysAD48	L2
SysAD49	M3
SysAD50	N3
SysAD51	R2
SysAD52	T3
SysAD53	U3
SysAD54	T6
SysAD55	T7
SysAD56	T10
SysAD57	T11
SysAD58	U13
SysAD59	V15
SysAD60	T15
SysAD61	U17
SysAD62	N16
SysAD63	N17
SysADC0	C8
SysADC1	G17
SysADC2	T8
SysADC3	L16
SysADC4	B8
SysADC5	H16
SysADC6	U8
SysADC7	L17
SysCmd0	E2
SysCmd1	D3
SysCmd2	B2

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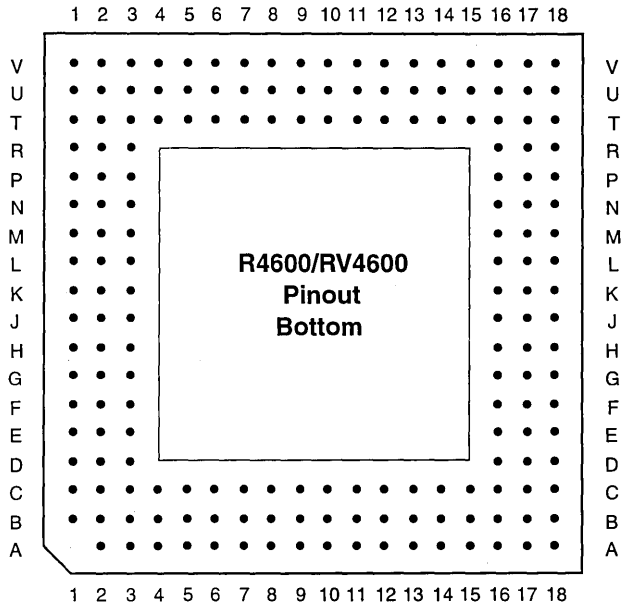
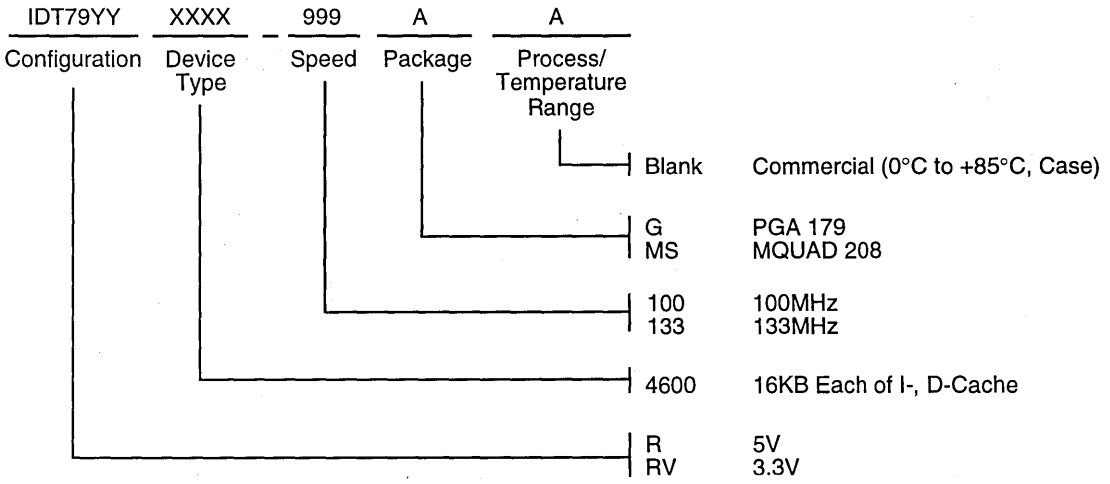
Function	Pin
SysCmd3	A5
SysCmd4	B7
SysCmd5	C9
SysCmd6	B10
SysCmd7	B12
SysCmd8	C13
SysCmdP	C14
TClock0	C17
TClock1	D16
VCCOk	M17
$\overline{\text{ValidIn}}$	P2
$\overline{\text{ValidOut}}$	R3
$\overline{\text{WrRdy}}$	C5
VccP	K17
VssP	K16
Vcc	A2
Vcc	A4
Reserved I (NC)	A7
Vcc	A9
Vcc	A11
Vcc	A13
Vcc	A16
Vcc	B18
Vcc	C1
Vcc	D18
Vcc	F1
Vcc	G18
Vcc	H1
Vcc	J18
Vcc	K1
Vcc	L18
Vcc	M1
Vcc	N18
Vcc	R1
Vcc	T18

Function	Pin
Vcc	U1
Vcc	V3
Vcc	V6
Vcc	V8
Vcc	V10
Vcc	V12
Vcc	V14
Vcc	V17
Vss	A3
Vss	A6
Vss	A8
Vss	A10
Vss	A12
Vss	A14
Vss	A17
Vss	A18
Vss	B1
Vss	C18
Vss	D1
Vss	F18
Vss	G1
Vss	H18
Vss	J1
Vss	K18
Vss	L1
Vss	M18
Vss	N1
Vss	P18
Vss	R18
Vss	T1
Vss	U18
Vss	V1
Vss	V2
Vss	V4
Vss	V7

Function	Pin
Vss	V9
Vss	V11
Vss	V13
Vss	V16
Vss	V18
JTCK	H17
JTDI	G16
JTDO	F16
JTMS	E16





VALID COMBINATIONS

IDT	79R4600 - 100, 133	G, MS Packages
	79RV4600 - 100, 133	G, MS Packages

Integrated Device Technology, Inc.

EMBEDDED 64-BIT RISC ORION MICROPROCESSOR

ORION

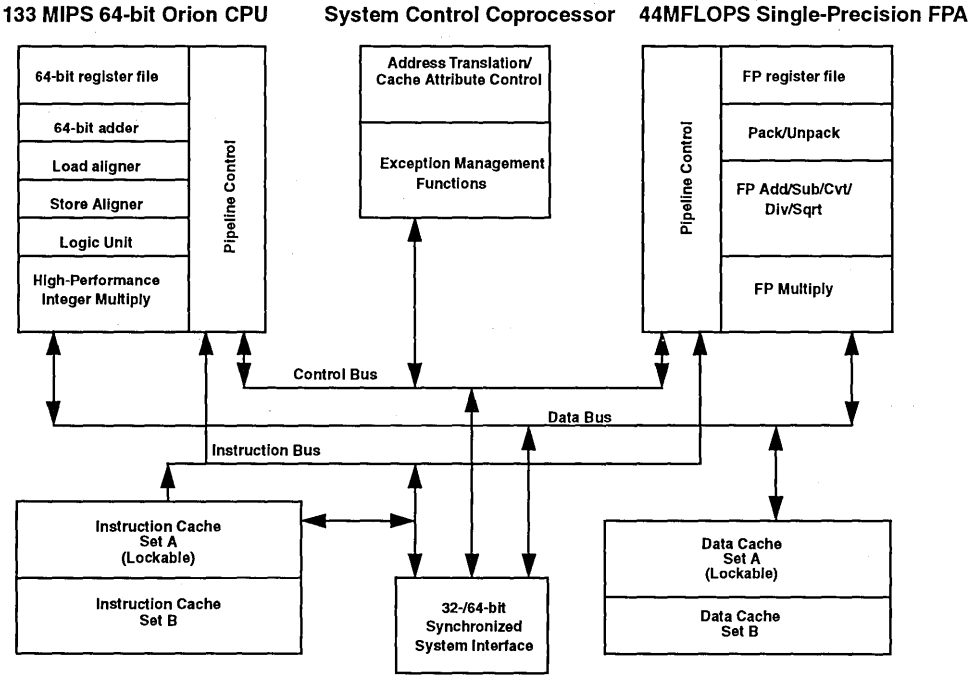
IDT79R4650™

Preliminary

FEATURES:

- High-performance embedded 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit registers
  - 80MHz, 100MHz, 133MHz operation frequency
- High-performance DSP capability
  - 66.7 Million Integer Multiply-Accumulate Operations/ sec @ 133 MHz
  - 44 MFlops floating point operations @133MHz
- High-performance microprocessor
  - 133 MIPS at 133MHz
  - 66.7 M Mul-Add/second at 133MHz
  - 44 MFLOP/s at 133MHz
  - >300,000 dhrystone (2.1)/sec capability at 133MHz (175 dhrystone MIPS)
- High level of integration
  - 64-bit, 133 MIPS integer CPU
  - 44MFlops Single precision floating-point unit
  - 8KB instruction cache; 8KB data cache
  - Integer multiply unit with 66.7M Mul-Add/sec
- Low-power operation
  - Less than 3W peak internal power at 100MHz
  - Active power management powers-down inactive units
  - Standby mode power consumption <200mW
- Upward software compatible with IDT RISController Family
- Large, efficient on-chip caches
  - Separate 8kB Instruction and 8kB Data caches
  - Over 1500MB/sec bandwidth from internal caches
  - 2-set associative
  - Write-back and write-through support
  - Cache locking to facilitate deterministic response
- Bus compatible with R4600/Orion family
  - System interfaces to 67 MHz, provides bandwidth up to 533 MB/S
  - Direct interface to 32-bit wide or 64-bit wide systems
  - Synchronized to external reference clock for multi-master operation
- Improved real-time support
  - Fast interrupt decode
  - Optional cache locking

BLOCK DIAGRAM:



DESCRIPTION:

The IDT79R4650 is a low-cost member of the IDT Orion family, targeted to a variety of performance hungry embedded applications. The R4650 continues the Orion tradition of high-performance through high-speed pipelines, high-bandwidth caches and bus interface, 64-bit architecture, and careful attention to efficient control. The R4650 reduces the cost of this performance relative to the R4600, by removing functional units that are frequently unneeded for many embedded applications, such as double-precision floating point arithmetic and a TLB.

The R4650 adds features relative to the R4600, reflective of its target applications. These features enable system cost reduction (e.g. optional 32-bit system interface) as well as higher performance for certain types of systems (e.g. cache locking, improved real-time support, integer DSP capability).

The R4650 supports a wide variety of embedded processor-based applications, such as consumer game systems, multi-media functions, internetworking equipment, switching equipment, and printing systems. Upwardly software-compatible with the RISController family, and bus- and upwardly software-compatible with the IDT Orion family, the R4650 will serve in many of the same applications, but, in addition supports other applications such as those requiring integer DSP functions.

The R4650 brings Orion performance levels to lower cost systems. Orion performance is preserved by retaining large on-chip caches that are two-way set associative, a streamlined high-speed pipeline, high-bandwidth, 64-bit execution, and facilities such as early restart for data cache misses. These techniques combine to allow the system designer over 2GB/sec aggregate internal bandwidth, 533 MB/sec bus bandwidth, 175 VAX MIPS, 44MFlops, and 66.7 M Multiply-add/second.

The R4650 provides complete upward application-software compatibility with the IDT79R3000™ family of microprocessors, including the IDT RISController™ 79R3051™/R3052™/R3041™/R3071™/R3081™ as well as the IDT79R4600 family of microprocessors. An array of development tools facilitates the rapid development of R4650-based systems, enabling a wide variety of customers to take advantage of the high-performance capabilities of the processor while maintaining short time to market goals.

The 64-bit computing capability of the R4650 enables a wide variety of capabilities previously limited by the lower bandwidth and bit-manipulation rates inherent in 32-bit architectures. For example, the R4650 can perform loads and stores from cached memory at the rates of 8-bytes every clock cycle, doubling the bandwidth of an equivalent 32-bit processor. This capability, coupled with the high clock rate for the R4650 pipeline, enables new levels of performance to be obtained from embedded systems.

This data sheet provides an overview of the features and architecture of the R4650 CPU. A more detailed description of the processor is available in the *IDT79R4650 Processor Hardware User's Manual*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

HARDWARE OVERVIEW

The R4650 family brings a high-level of integration designed for high-performance computing. The key elements of the R4650 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

Pipeline

The R4650 uses a 5-stage pipeline similar to the IDT79R3000 and the IDT79R4600. The simplicity of this pipeline allows the R4650 to be lower cost and lower power than super-scalar or super-pipelined processors. Unlike superscalar processors, applications that have large data dependencies or that require a great deal of load/stores

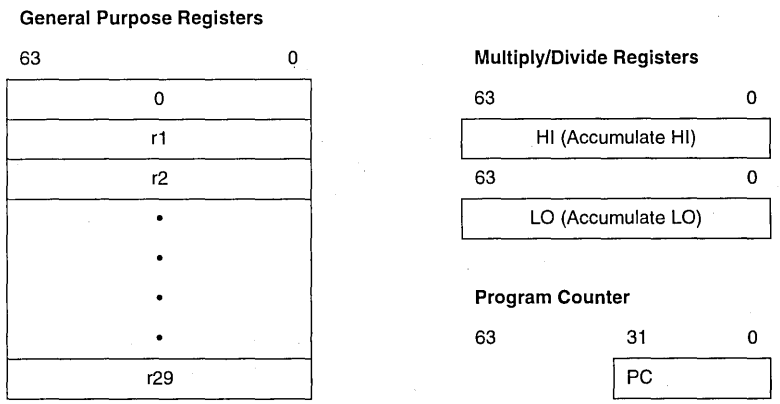
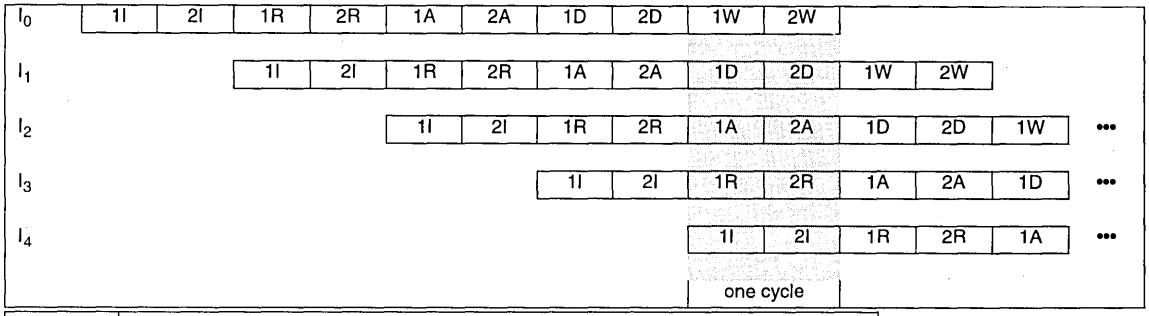


Figure 1: CPU Registers



1I-1R	Instruction cache access
2I	Instruction virtual to physical address translation
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation
1D-2D	Virtual to physical address translation
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Figure 2: R4650 Pipeline

can still achieve performance close to the peak performance of the processor. Figure 2 shows the R4650 pipeline.

Integer Execution Engine

The R4650 implements the MIPS-III Instruction Set Architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4650 includes the same additions to the instruction set found in the R4600 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier R30xx processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture. In addition, MIPS-III specifies new instructions defined to take advantage of the 64-bit architecture of the processor.

Finally, the R4650 also implements additional instructions, which are considered extensions to the MIPS-III architecture. These instructions improve the multiply and multiply-add throughput of the CPU, making it well suited to a wide variety of imaging and DSP applications. These extensions, which use opcodes allocated by MIPS Technologies for this purpose, are supported by a wide variety of development tools.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The 64-bit register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

Register File

The R4650 has thirty-two general-purpose 64-bit registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline. Figure 1 illustrates the R4650 Register File.

ALU

The R4650 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

Integer Multiply/Divide

The R4650 uses a dedicated integer multiply/divide unit, optimized for high-speed multiply and multiply-accumulate operation. Table 1 shows the performance, expressed in terms of pipeline clocks, achieved by the R4650 integer multiply unit.

Opcode	Operand Size	Latency	Repeat	Stall
MULT/U, MAD/U	16 bit	3	2	0
	32 bit	4	3	0
MUL	16 bit	3	2	1
	32 bit	4	3	2
DMULT, DMULTU	any	6	5	0
DIV, DIVU	any	36	36	0
DDIV, DDIVU	any	68	68	0

Table 1: R4650 Integer Multiply Operation

The MIPS-III architecture defines that the results of a multiply or divide operation are placed in the HI and LO registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions.

The R4650 adds a new multiply instruction, "MUL", which can specify that the multiply results bypass the "Lo" register and are placed immediately in the primary register file. By avoiding the explicit "Move-from-Lo" instruction required when using "Lo", throughput of multiply-intensive operations is increased.

An additional enhancement offered by the R4650 is an atomic "multiply-add" operation, MAD, used to perform multiply-accumulate operations. This instruction multiplies two numbers and adds the product to the current contents of the HI and LO registers. This operation is used in numerous DSP algorithms, and allows the R4650 to cost reduce systems requiring a mix of DSP and control functions.

Finally, aggressive implementation techniques feature low latency for these operations along with pipelining to allow new operations to be issued before a previous one has fully completed. Table 1 also shows the repeat rate (peak issue rate), latency, and number of processor stalls required for the various operations. The R4650 performs automatic operand size detection to determine the size of the operand, and implements hardware interlocks to prevent overrun, allowing this high-performance to be achieved with simple programming.

Floating-Point Co-Processor

The R4650 incorporates an entire single-precision floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

The floating-point unit of the R4650 directly implements single-precision floating point operations. This enables the R4650 to perform functions such as graphics rendering, without requiring extensive die area or power consumption. The single-precision unit of the R4650 is directly compatible with the single-precision operation of the R4600, and features the same latencies and repeat rates.

The R4650 does not directly implement the double-precision operations found in the R4600. However, to maintain software compatibility, the R4650 will signal a trap when a double-precision operation is initiated, allowing the requested function to be emulated in software. Alternatively, the system architect could use a software library emulation of double-precision functions, selected at compile time, to eliminate the overhead associated with trap and emulation.

Floating-Point Units

The R4650 floating-point execution units perform single precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 6 cycles.

As in the IDT79R4600, the R4650 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with IEEE Standard 754. Double precision operations are not directly supported; attempts to execute double-precision floating point operations, or refer directly to double-precision registers, result in the R4650 signalling a "trap" to the CPU, enabling emulation of the requested function.

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Table 2 gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Instruction Latency
ADD	4
SUB	4
MUL	8
DIV	32
SQRT	31
CMP	3
FIX	4
FLOAT	6
ABS	1
MOV	1
NEG	1
LWC1	2
SWC1	1

Table 2: Floating-Point Operation

Floating-Point General Register File

The floating-point register file is made up of thirty-two 32-bit registers. These registers are used as source or target registers for the single-precision operations.

References to these registers as 64-bit registers (as supported in the R4600) will cause a trap to be signalled to the integer unit.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual to physical address translation and cache protocols, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent.

In the R4650, significant changes in CP0 relative to the R4600 have been implemented. These changes are designed to simplify memory management, facilitate debug, and speed real-time processing.

System Control Co-Processor Registers

The R4650 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's address translation is controlled, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4650 includes registers to implement a real-time cycle counting facility, which aids in cache diagnostic testing, assists in data error detection, and facilitates software debug. Alternatively, this timer can be used as the operating system reference timer, and can signal a periodic interrupt.

Table 3 shows the CP0 registers of the R4650.

Number	Name	Function / Changes (relative to R4600 boards)
0	IBase	Instruction address space base (new in R4650)
1	IBound	Instruction address space bound (new in R4650)
2	DBase	Data address space base (new in R4650)
3	DBound	Data address space bound (new in R4650)
4-7, 10, 20-25, 29, 31	-	not used
8	BadVAddr	Virtual address on address exceptions — changed to 32 bits
9	Count	Counts every other cycle — no change
11	Compare	Generate interrupt when `Count` = `Compare` — no change
12	Status	Miscellaneous control/status — delete `KX`, `SX`, and `KSU` low bit, add cache locking bits
13	Cause	Exception/Interrupt information — add bits for watch exceptions
14	EPC	Exception PC — changed to 32 bits
15	PRId	Processor ID — Imp changed to 0x22
16	Config	Cache size fields changed to reflect R4650 cache sizes. `K0` field deleted, since function is now in CAlg.
17	CAlg	Cache attributes for the 8 512MB regions of the virtual address space — new register
18	IWatch	Instruction breakpoint virtual address — new register
19	DWatch	Data breakpoint virtual address — new register
26	ECC	no change
27	CacheErr	no change
28	TagLo	no change
30	ErrorEPC	CacheError exception PC — changed to 32 bits

Table 3: R4650 CPO Registers

Operation modes

The R4650 supports two modes of operation: user mode and kernel mode.

Kernel mode operation is typically used for exception handling and operating system kernel functions, including CP0 management and access to IO devices. In kernel mode, software has access to the entire address space and all of the co-processor 0 registers, and can select whether to enable co-processor 1 accesses. The processor enters kernel mode at reset, and whenever an exception is recognized.

User mode is typically used for applications programs. User mode accesses are limited to a subset of the virtual address space, and can be inhibited from accessing CP0 functions.

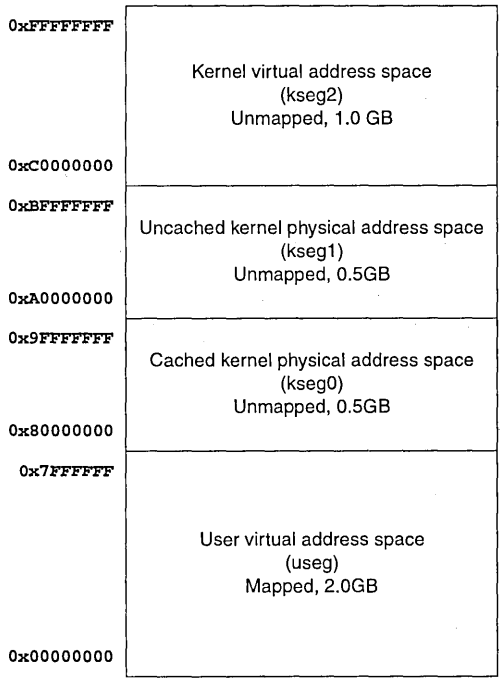


Figure 3: Mode Virtual Addressing (32-bit mode)

Virtual to Physical Address Mapping

The 4GB virtual address space of the R4650 is shown in figure 3. The 4 GB address space is divided into addresses accessible in either kernel or user mode (kuseg), and addresses only accessible in kernel mode (kseg2:0).

The R4650 supports the use of multiple user tasks sharing common virtual addresses, but mapped to separate physical addresses. This facility is implemented via the "base-bounds" registers contained in CP0.

When a user virtual address is asserted (load, store, or instruction fetch), the R4650 compares the virtual address with the contents of the appropriate "bounds" register (instruction or data). If the virtual address is "in bounds", the value of the corresponding "base" register is added to the virtual address to form the physical address for that reference. If the address is not within bounds, an exception is signalled.

This facility enables multiple user processes in a single physical memory without the use of a TLB. This type of operation is further supported by a number of development tools for the R4650, including real-time operating systems and "position independent code".

Kernel mode addresses do not use the base-bounds registers, but rather undergo a fixed virtual to physical address translation.

Debug Support

To facilitate software debug, the R4650 adds a pair of "watch" registers to CP0. When enabled, these registers will cause the CPU to take an exception when a "watched" address is appropriately accessed.

Interrupt Vector

The R4650 also adds the capability to speed interrupt exception decoding. Unlike the R4600, which utilizes a single common exception vector for all exception types (including interrupts), the R4650 allows kernel software to enable a separate interrupt exception vector. When enabled, this vector location speeds interrupt processing by allowing software to avoid decoding interrupts from general purpose exceptions.

Cache Memory

In order to keep the R4650's high-performance pipeline full and operating efficiently, the R4650 incorporates on-chip instruction and data caches that can each be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of over 1500 MB per second at a pipelineclock frequency of 133MHz. The cache subsystem is similar in construction to that found in the R4600, although some changes have been implemented. Table 6is an overview of the caches found on the R4650.

Instruction Cache

The R4650 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 8KB in size and is parity protected.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 20-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 533MB/sec at 133MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill, can write 64 bits-per-cycle to

minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

In addition, the contents of one set of the instruction cache (set "A") can be "locked" by setting a bit in a CP0 register. Locking the set prevents its contents from being overwritten by a subsequent cache miss; refill occurs then only into "set B".

This operation effectively "locks" time critical code into one 4kB set, while allowing the other set to service other instruction streams in a normal fashion. Thus, the benefits of cached performance are achieved, while deterministic real-time response is preserved.

Data Cache

For fast, single cycle data access, the R4650 includes an 8KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size. Table 4 lists the R4650 cache attributes.

Characteristics	Instruction	Data
Size	8KB	8KB
Organization	2-way set associative	2-way set associative
Line size	32B	32B
Index	$vAddr_{11..0}$	$vAddr_{11..0}$
Tag	$pAddr_{31..12}$	$pAddr_{31..12}$
Write policy	n.a.	writeback /writethru
Line transfer order	read sub-block order	read sub-block order
	write sequential	write sequential
Miss restart after transfer of	entire line	first word
Parity	per-word	per-byte
Cache locking	set A	set A

Table 4: R4650 Cache Attributes

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through for certain address ranges, using the CAlg register in CP0. Cache protocols supported for the data cache are:

- **Uncached**. Addresses in a memory area indicated as uncached will not be read from the cache. Stores to such addresses will be written directly to main memory, without changing cache contents.
- **Writeback**. Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later writeback. If the cache lookup misses, the target line is first brought into the cache before the cache is updated.
- **Write-through with write allocate.** Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated and main memory will also be written; the state of the "writeback" bit of the cache line will be unchanged. If the cache lookup misses, the target line is first brought into the cache before the cache is updated.
- **Write-through without write-allocate.** Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first

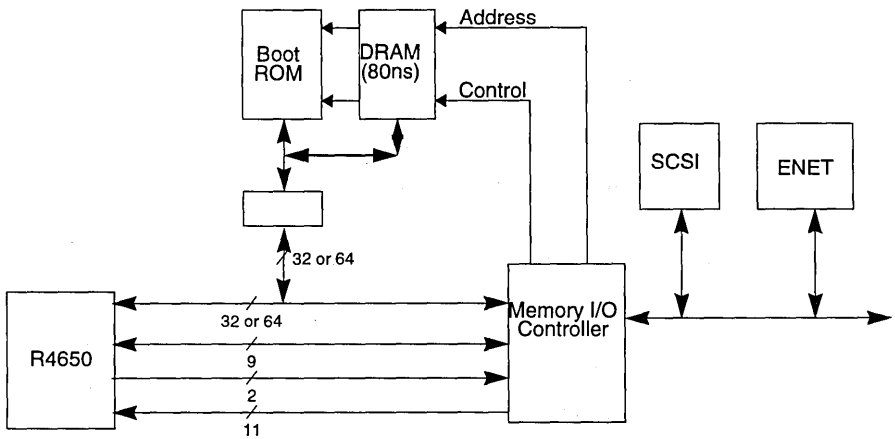


Figure 4: Typical R4650 System Architecture

searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later writeback. If the cache lookup misses, then only main memory is written.

Associated with the Data Cache is the store buffer. When the R4650 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4650 to execute a store every processor cycle and to perform back-to-back stores without penalty.

Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four address and data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

System Interface

The R4650 supports a 64-bit system interface that is bus compatible with the R4600 system interface. In addition, the R4650 supports a 32-bit system interface mode, allowing the CPU to interface directly with a lower cost memory system.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 533MB/sec at 133MHz.

Figure 4 shows a typical system using the R4650. In this example two banks of DRAMs are used to supply and accept data with a DDxxDD data pattern

The R4650 clocking interface allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock, and can be between 25 and 67MHz (somewhat dependent on maximum pipeline speed for the CPU).

An on-chip phase-locked-loop generates the pipeline clock from the system interface clock by multiplying it up an amount selected at system reset. Supported multipliers are values 2 through 8 inclusive, allowing systems to implement pipeline clocks at significantly higher frequency than the system interface clock.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4650 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, SysAD can be viewed as a 32-bit multiplexed bus, with 4 parity check bits.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The bus frequency and reference timing of the R4650 are taken from the input clock. The rate at which the CPU transmits data to the system interface is programmable via boot time mode control bits. The rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4650. Again, the system designer has the flexibility to make these price/performance trade-offs.

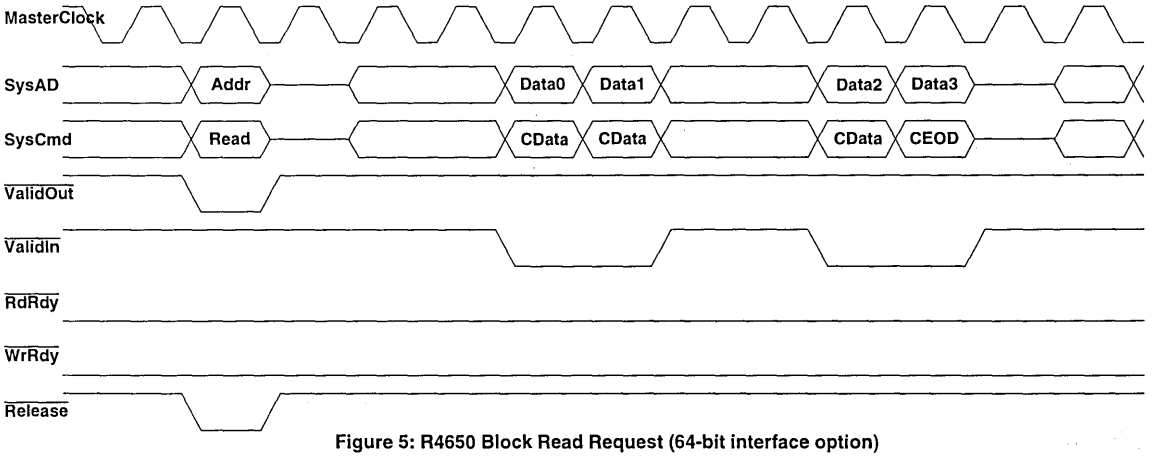


Figure 5: R4650 Block Read Request (64-bit interface option)

System Command Bus

The R4650 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4650. Processor requests are initiated by the R4650 and responded to by an external device. External requests are issued by an external device and require the R4650 to respond.

The R4650 supports single datum (one to eight byte) and 8-word block transfers on the SysAD bus. In the case of a single-datum transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred. The choice of 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles, and whether a single datum transfer larger than 4 bytes needs to be broken into two smaller transfers.

Handshake Signals

There are six handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the R4650 whether it can accept a new read or write transaction. The R4650 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$ and $\overline{\text{Release}}$ are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{\text{ExtRqst}}$. The R4650 responds by asserting $\overline{\text{Release}}$ to release the system interface to slave state.

$\overline{\text{ValidOut}}$ and $\overline{\text{ValidIn}}$ are used by the R4650 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4650 asserts $\overline{\text{ValidOut}}$ when it is driving these buses with a valid command or data, and the external device drives $\overline{\text{ValidIn}}$ when it has control of the buses and is driving a valid command or data.

Non-overlapping System Interface

The R4650 requires a non-overlapping system interface, compatible with the R4600. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4650 issues another request. The R4650 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4650.

The R4650 asserts $\overline{\text{ValidOut}}$ and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has $\overline{\text{RdRdy}}$ or Read transactions asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting $\overline{\text{Release}}$. The external device can then begin sending the data to the R4650.

Figure 5 shows a processor block read request and the external agent read response. The read latency is 4 cycles ($\overline{\text{ValidOut}}$ to $\overline{\text{ValidIn}}$), and the response data pattern is DDxxDD. Figure 6 shows a processor block write.

Write Reissue and Pipeline Write

The R4600 and the R4650 implement additional write protocols designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of 2 cycles per write. A write

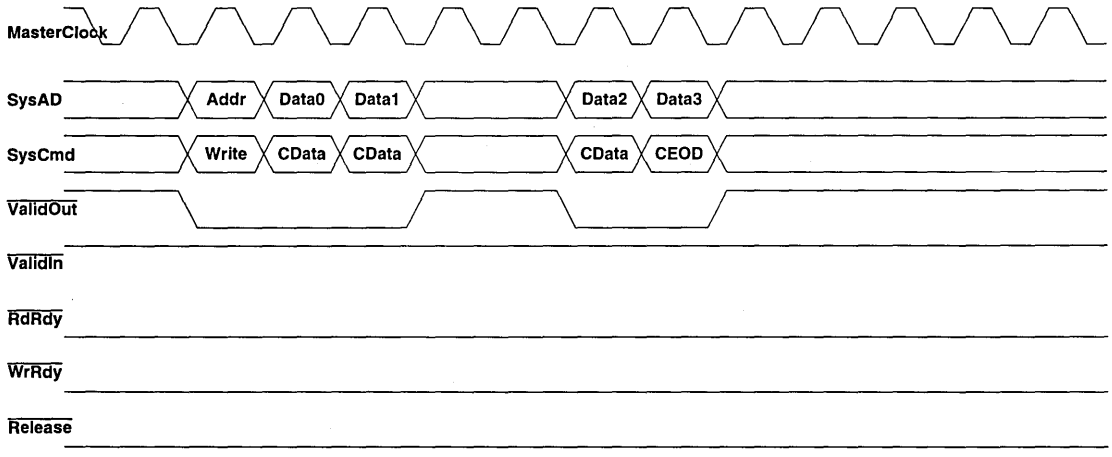


Figure 6: R4650 Block Write Request (64-bit system interface)

issues if WrRdy is asserted 2 cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issues again. Pipelined writes have the same 2-cycle per write repeat rate, but can issue one more write after WrRdy de-asserts. They still follow the issue rule as R4x00 mode for other writes.

External Requests

The R4650 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4650 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus.

The following is a list of the supported external requests:

- Read Response
- Null

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the VccoK Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

Boot-Time Modes

The boot-time serial mode stream is defined in Table 5. Bit 0 is the bit presented to the processor when VccoK is asserted; bit 255 is the last.

Power Management

CP0 is also used to control the power management for the R4650. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU. The standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by any interrupt.

Standby Mode Operation

The R4650 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as "Standby Mode".

Entering Standby Mode

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (i.e. the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Mode bit	Description	
0	Reserved (must be zero)	
4..1	Writeback data rate	
	64-bit	32-bit
	0 → D,	0 → W,
	1 → DDx,	1 → WWx,
	2 → DDxx,	2 → WWxx,
	3 → DxDx,	3 → WxWx,
	4 → DDxxx,	4 → WWxxx,
	5 → DDxxxx,	5 → WWxxxx,
	6 → DxxDxx,	6 → WxxWxx,
	7 → DDxxxxxx,	7 → WWxxxxxx,
	8 → DxxxDxxx,	8 → WxxxWxxx,
	9-15 reserved	9-15 reserved
7..5	Clock multiplier 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved	
8	0 → Little endian, 1 → Big endian	
10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue	
11	Disable the timer interrupt on Int[5].	
12	0 → 64-bit system interface 1 → 32-bit system interface	
14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)	
255..15	must be zero	

Table 5: Boot time mode stream

Thermal Considerations

The R4650 utilizes special packaging techniques to improve the thermal properties of high-speed processors. The R4650 is packaged using cavity down packaging in a 208-pin MQUAD.

The R4650 utilizes the MQUAD package (the "MS" package), which is an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing. Due to the heat-spreading effect of the aluminum, the MQUAD package allows for an efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The R4650 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 6.

	ØCA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
208 MQUAD	21	13	10	9	8	7

Table 6: Thermal Resistance (ØCA) at Various Airflows

Note that the R4650 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79R4650 Hardware User's Manual.*

PIN DESCRIPTION

The following is a list of interface, interrupt, and miscellaneous pins available on the R4650. Pins marked with one asterisk are active when low.

Pin Name	Type	Description
System interface:		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity For the R4650 this signal is unused on input and zero on output.
Clock/control interface:		
MasterClock	Input	Master clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.
Interrupt interface:		
Int*(5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Pin Name	Type	Description
Initialization interface:		
Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4650 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with MasterClock.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterClock.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	R4650 5.0V±5%	RV4650 3.3V±5%	Unit
		Commercial	Commercial	
V_{TERM}	Terminal Voltage with respect to GND	−0.5[2] to +7.0	−0.5[2] to +4.6	V
T_C	Operating Temperature (case)	0 to +85	0 to +85	°C
T_{BIAS}	Case Temperature Under Bias	−55 to +125	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	−55 to +125	°C
I_{IN}	DC Input Current	20[3]	20[3]	mA
I_{OUT}	DC Output Current	50[4]	50[4]	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = −2.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. When V_{IN} < 0V or V_{IN} > V_{CC}
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

5

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	R4650	RV4650
			V_{CC}	V_{CC}
Commercial	0°C to +85°C (Case)	0V	5.0V±5%	3.3V±5%

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4650

(V_{CC} = 5.0±5%, T_{CASE} = 0°C to +85°C)

Parameter	R4650 80MHz		R4650 100MHz		R4650 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	3.5V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	0.8V	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

POWER CONSUMPTION—R4650

Parameter		R4650 80MHz		R4650 100MHz		R4650 133MHz		Conditions
		Typical[9]	Max	Typical[9]	Max	Typical[9]	Max	
System Condition:		80/40MHz		100/50MHz		133/44MHz		—
I_{CC}	standby	—	50 mA	—	75 mA	—	100 mA	C_L = 0pF[8]
		—	125 mA	—	150 mA	—	200 mA	C_L = 50pF
	active, 64-bit bus option	575 mA	800 mA	700 mA	1200 mA	950 mA	1350 mA	C_L = 0pF No SysAd activity[8]
		675 mA	1200 mA	800 mA	1400 mA	1050 mA	1750 mA	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		675 mA	1400 mA	800 mA	1675 mA	1050 mA	2000 mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[8]
	active, 32-bit bus option	575 mA	800 mA	700 mA	1000 mA	950 mA	1350 mA	C_L = 0pF No SysAd activity[8]
		625 mA	1000 mA	750 mA	1200 mA	1000 mA	1550 mA	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		625 mA	1100 mA	750 mA	1350 mA	1000 mA	1650 mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[8]

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4650

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—R4650

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Pipeline clock frequency	PClk		50	80	50	100	50	133	MHz
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock Frequency(5)	—	—	20	40	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	—	±250	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTES:

5. Operation of the R4650 is only guaranteed with the Phase Lock Loop enabled.
6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.
8. Guaranteed by Design.
9. Typical integer instruction mix and cache miss rates.

System Interface Parameters—R4650(6)

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	11	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Output Hold	t_{DOH} *	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	5	—	3.5	—	3.5	—	ns
Data Hold	t_{DH}		2.5	—	1.5	—	1.5	—	ns

* 25pf loading on external putput signals, fastest settings

Boot Time Interface Parameters—R4650

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE RV4650

(V_{CC} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
V_{OHC}	—	—	—	—	—	—	—
V_{ILC}	—	—	—	—	—	—	—
V_{IHC}	—	—	—	—	—	—	—
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

POWER CONSUMPTION—RV4650

Parameter		RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Conditions
		Typical[9]	Maximum	Typical[9]	Maximum	Typical[9]	Maximum	
System Condition:		80/40MHz		100/50MHz		133/44MHz		—
I_{CC}	standby	—	40 mA	—	50 mA	—	60 mA	C_L = 0pF[8]
		—	90 mA	—	100 mA	—	110 mA	C_L = 50pF
	active, 64-bit bus option	375 mA	575 mA	475 mA	700 mA	625 mA	925 mA	C_L = 0pF, No SysAd activity[8]
		450 mA	800 mA	550 mA	925 mA	700 mA	1150 mA	C_L = 50pF R4x00 Icompatible writes T_C = 25°C
		450 mA	950 mA	550 mA	925 mA	700 mA	1300 mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C[8]
	active, 32-bit bus option	375 mA	575 mA	475 mA	700 mA	625 mA	925 mA	C_L = 0pF, No SysAd activity[8]
		400 mA	700 mA	525 mA	825 mA	650 mA	1050 mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		400 mA	775 mA	525 mA	825 mA	650 mA	1125 mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C[8]

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—RV4650

(V_{CC}=3.3V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—RV4650

Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Pipeline clock frequency	PClk		50	80	50	100	50	133	MHz
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock Frequency(5)	—	—	20	40	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	—	±250	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTES:

10.Operation of the RV4650 is only guaranteed with the Phase Lock Loop enabled.

System Interface Parameters—RV4650(6)

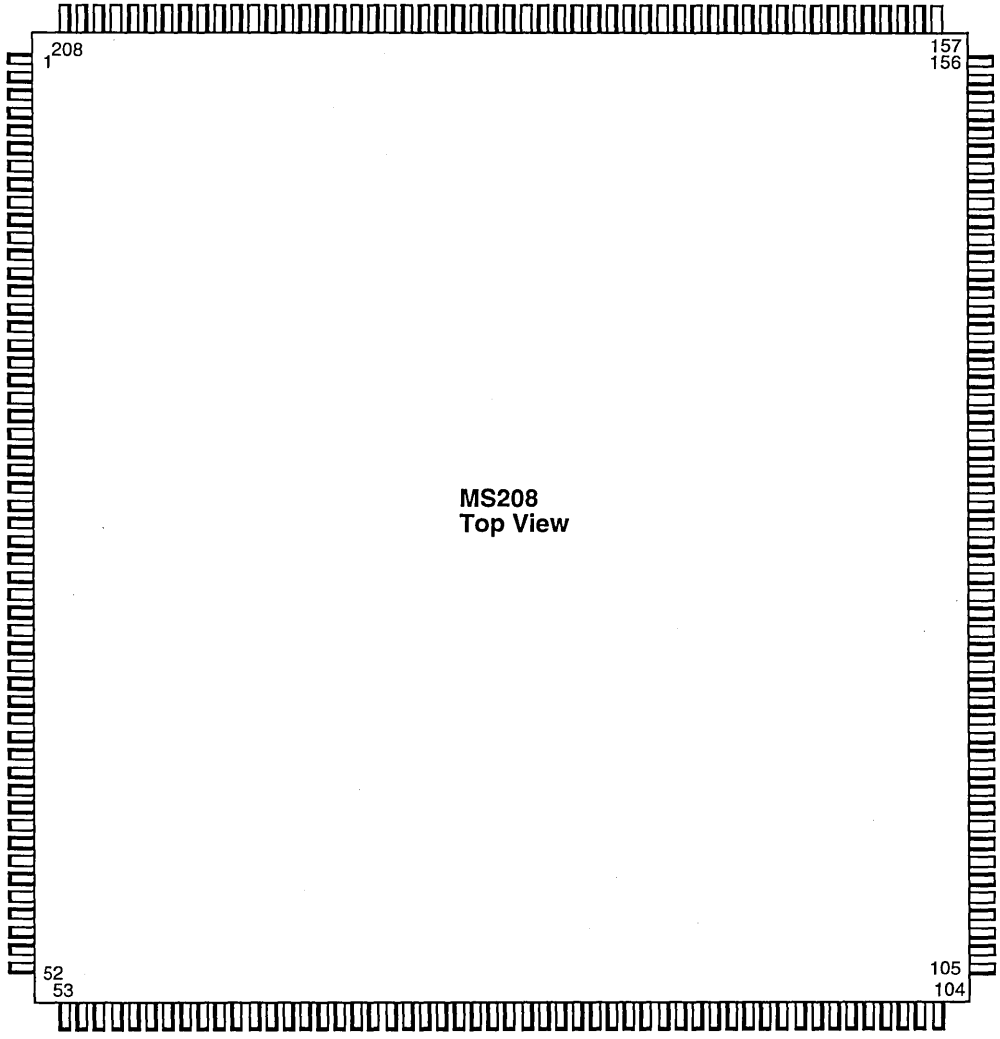
Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	11	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Output Hold	t_{DOH} *	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	5	—	3.5	—	3.5	—	ns
Data Hold	t_{DH}		2.5	—	1.5	—	1.5	—	ns

* 25pf loading on external putput signals, fastest settings

Boot Time Interface Parameters—RV4650

Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

PHYSICAL SPECIFICATIONS — 208-PIN MQUAD

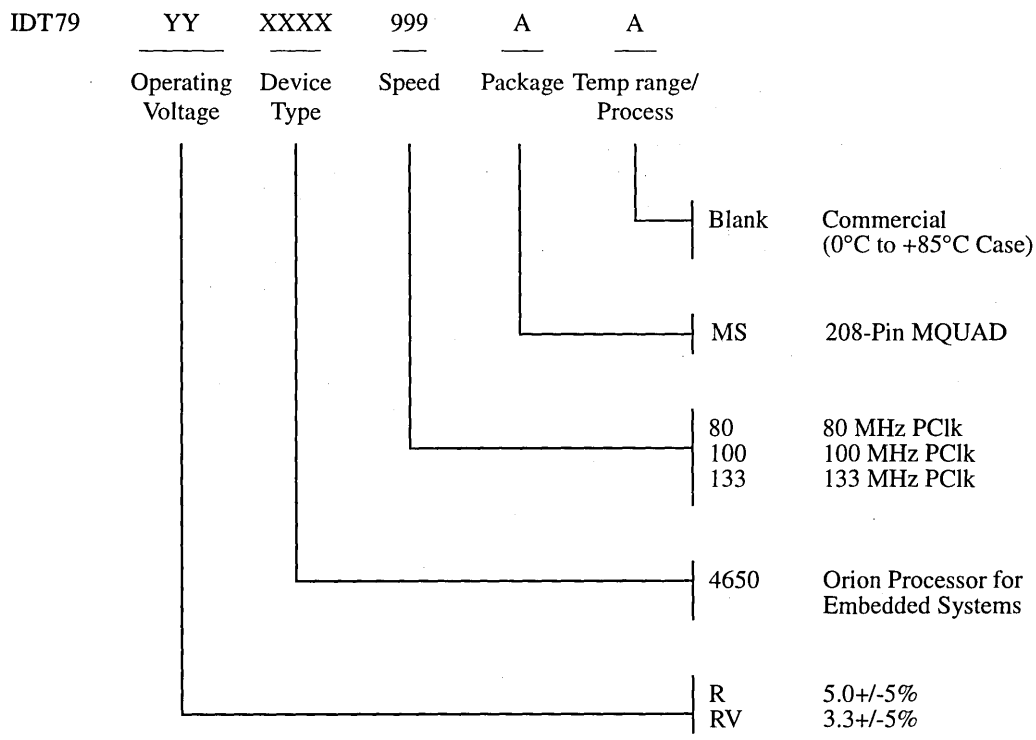


R4650 MQUAD PACKAGE PIN-OUT*

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	N.C.	107	N.C.	159	SysAD59
4	N.C.	56	N.C.	108	N.C.	160	ColdReset*
5	N.C.	57	SysCmd2	109	N.C.	161	SysAD28
6	N.C.	58	SysAD36	110	N.C.	162	Vcc
7	N.C.	59	SysAD4	111	N.C.	163	Vss
8	N.C.	60	SysCmd1	112	N.C.	164	SysAD60
9	N.C.	61	Vss	113	N.C.	165	Reset*
10	SysAD11	62	Vcc	114	SysAD52	166	SysAD29
11	Vss	63	SysAD35	115	ExtRqst*	167	SysAD61
12	Vcc	64	SysAD3	116	Vcc	168	SysAD30
13	SysCmd8	65	SysCmd0	117	Vss	169	Vcc
14	SysAD42	66	SysAD34	118	SysAD21	170	Vss
15	SysAD10	67	Vss	119	SysAD53	171	SysAD62
16	SysCmd7	68	Vcc	120	RdRdy*	172	SysAD31
17	Vss	69	SysAD2	121	Modein	173	SysAD63
18	Vcc	70	Int5*	122	SysAD22	174	Vcc
19	SysAD41	71	SysAD33	123	SysAD54	175	Vss
20	SysAD9	72	SysAD1	124	Vcc	176	VccOK
21	SysCmd6	73	Vss	125	Vss	177	SysADC3
22	SysAD40	74	Vcc	126	Release*	178	SysADC7
23	Vss	75	Int4*	127	SysAD23	179	N.C.
24	Vcc	76	SysAD32	128	SysAD55	180	N.C.
25	SysAD8	77	SysAD0	129	NMI*	181	N.C.
26	SysCmd5	78	Int3*	130	Vcc	182	N.C.
27	SysADC4	79	Vss	131	Vss	183	N.C.
28	SysADC0	80	Vcc	132	SysADC2	184	N.C.
29	Vss	81	Int2*	133	SysADC6	185	VccP
30	Vcc	82	SysAD16	134	SysAD24	186	VssP
31	SysCmd4	83	SysAD48	135	Vcc	187	MasterClock
32	SysAD39	84	Int1*	136	Vss	188	Vcc
33	SysAD7	85	Vss	137	SysAD56	189	Vss
34	SysCmd3	86	Vcc	138	SysAD25	190	SysADC5
35	Vss	87	SysAD17	139	SysAD57	191	SysADC1
36	Vcc	88	SysAD49	140	Vcc	192	Vcc
37	SysAD38	89	Int0*	141	Vss	193	Vss
38	SysAD6	90	SysAD18	142	IOOut	194	SysAD47
39	ModeClock	91	Vss	143	SysAD26	195	SysAD15
40	WrRdy*	92	Vcc	144	SysAD58	196	SysAD46
41	SysAD37	93	SysAD50	145	IOIn	197	Vcc
42	SysAD5	94	ValidIn*	146	Vcc	198	Vss
43	Vss	95	SysAD19	147	Vss	199	SysAD14
44	Vcc	96	SysAD51	148	SysAD27	200	SysAD45
45	N.C.	97	Vss	149	N.C.	201	SysAD13
46	N.C.	98	Vcc	150	N.C.	202	SysAD44
47	N.C.	99	ValidOut*	151	N.C.	203	V_{SS}
48	N.C.	100	SysAD20	152	N.C.	204	V_{CC}
49	N.C.	101	N.C.	153	N.C.	205	SysAD12
50	N.C.	102	N.C.	154	N.C.	206	SysCmdP
51	N.C.	103	N.C.	155	N.C.	207	SysAD43
52	N.C.	104	N.C.	156	N.C.	208	N.C.

*N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

ORDERING INFORMATION



Valid Combinations:

IDT 79R4650 - 80, 100, 133	MQUAD package

Integrated Device Technology, Inc.

ENHANCED ORION 64-BIT RISC MICROPROCESSOR

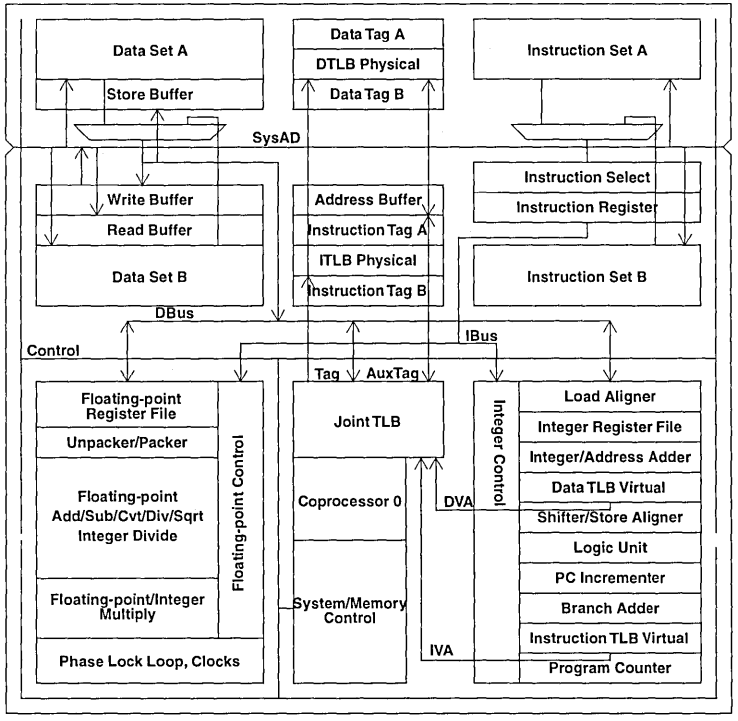
ORION™
IDT79R4700™
PRELIMINARY

FEATURES:

- True 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit floating-point operations
  - 64-bit registers
  - 64-bit virtual address space
- High-performance microprocessor
  - 175 peak MIPS at 175MHz
  - 87 peak MFLOP/s at 175MHz
  - 132 SPECint92 at 175MHz
  - Two-way set associative caches
- Improved FPA multiply performance
  - 1 mul, 1 add every 4 clock cycles
- High level of integration
  - 64-bit integer CPU
  - 64-bit floating-point unit
  - 16KB instruction cache; 16KB data cache
  - Flexible MMU with large TLB
- Low-power operation
  - 3.3V power supply
  - 24mW/MHZ typical internal power dissipation (2.4W @ 100MHz, 3.3V)
  - Standby mode reduces internal power
- Standard operating system support includes:
  - Microsoft Windows™ NT
  - UNISOFT Unix™ System V.4
- Fully software and pin-compatible with R4600 ORION Processor Family
- Available in R4600 pin-compatible 179-pin PGA or 208-pin MQUAD
- 100-175MHz with mode bit dependent output clock frequencies
- 64GB physical address space
- Processor family for a wide variety of applications
  - Desktop workstations and PCs
  - Deskside or departmental servers
  - High-performance embedded applications (e.g. color printers, multi-media and internetworking.)

5

BLOCK DIAGRAM:



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DESCRIPTION:

The IDT79R4700 Enhanced ORION 64-Bit RISC Microprocessor is a follow-on to the IDT79R4600, and is fully compatible with it. The R4700 has improved FPA multiply operations. The RV4700 is available only in 3.3V. The remaining features of the R4700 are the same.

The R4700 supports a wide variety of processor-based applications, from 32-bit Windows NT desktop or notebook systems through high-performance, 64-bit OLTP systems. Compatible with the R4600 family for both hardware and software, the R4700 will serve in many of the same applications, but, in addition supports faster floating point computation, thus improving its performance in graphics-oriented applications. It does not provide integrated secondary cache and multiprocessor support as found in the R4000SC and R4000MC, but an external secondary cache can be designed around it. The large on-chip two-way set associative caches make this unnecessary in many systems.

The R4700 brings R4400SC performance levels to the R4000PC package, while at the same time providing lower cost and lower power. It does this by providing larger on-chip caches that are two-way set associative, fewer pipeline stalls, and early restart for data cache misses. It also improves the performance of floating point multiply operations and allows 1 multiply and 1 add every 4 clock cycles. The result is >120 SPECint92 and >90 SPECfp92 (exact figures are system-dependent).

The R4700 provides complete upward application-software compatibility with the IDT79R3000™ family of microprocessors, including the IDT RISController™ 79R3051™/R3052™/R3041™/R3071™/R3081™ as well as the IDT79R4000 family of microprocessors. Microsoft Windows NT and UNISOFT Unix V.4 operating systems insure the availability of thousands of applications programs, geared to provide a complete solution to a large number of processing needs. An array of development tools facilitates the rapid development of R4700-based systems, enabling a wide variety of customers to take advantage of the MIPS Open Architecture philosophy.

The 64-bit computing and addressing capability of the R4700 enables a wide variety of capabilities previously limited by a smaller address space. For example, the large address space allows operating systems with extensive file mapping; direct access to large files can occur without explicit I/O calls. Applications such as large CAD databases, multi-media, and high-quality image storage and retrieval all directly benefit from the enlarged address space.

This data sheet provides an overview of the features and architecture of the R4700 CPU. A more detailed description of the processor appears in the *IDT79R4600 and IDT79R4700 RISC Processor Hardware User's Manual*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

HARDWARE OVERVIEW

The R4700 family brings a high-level of integration designed for high-performance computing. The key elements of the R4700 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

Pipeline

The R4700 uses a 5-stage pipeline similar to the IDT79R3000. The simplicity of this pipeline allows the R4700 to be lower cost and lower power than super-scalar

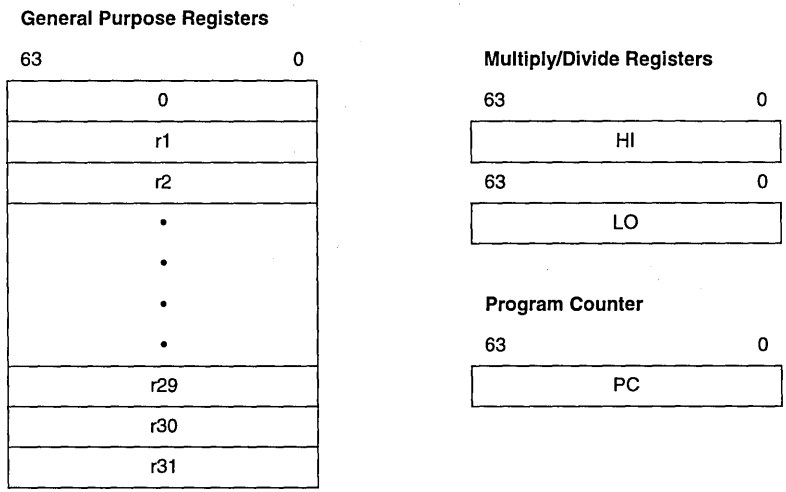
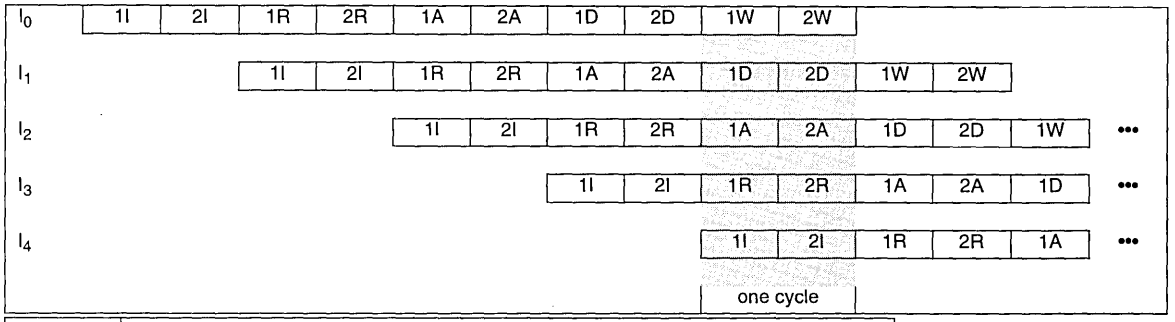


Figure 1: CPU Registers



1I-1R	Instruction cache access
2I	Instruction virtual to physical address translation in ITLB
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation in DTLB
1D-2D	Virtual to physical address translation in JTLB
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Figure 2: R4700 Pipeline

or super-pipelined processors. Unlike the R3000, the R4700 does virtual-to-physical translation in parallel with cache access. This allows the R4700 to operate at over three times the frequency of the R3000 and to support a larger TLB for address translation.

Compared to the 8-stage R4000 pipeline, the R4700 is more efficient (requires fewer stalls).
Figure 2 shows the R4700 pipeline.

Integer Execution Engine

The R4700 implements the MIPS Instruction Set architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4700 includes the same additions to the instruction set as found in the R4000 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture.

In addition to the instruction extensions detailed above, new instructions defined in the R4600 that take advantage of the 64-bit architecture of the processor are also incorporated into the R4700. The R4700 is fully software-compatible with the R4600. When operating as a 32-bit processor, the R4700 will take an exception on these new instructions.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

Register File

The R4700 has thirty-two general-purpose registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

ALU

The R4700 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized

and can perform an operation in a single pipeline cycle.

Integer Multiply/Divide

The R4700 uses the floating-point unit to perform integer multiply and divide. The results of the operation are placed in the *HI* and *LO* registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions. Table 1 below shows the number of processor internal cycles required between an integer multiply or divide and a subsequent MFHI or MFLO operation, in order that no interlock or stall occurs. The R4700 performs an integer multiply faster than the R4600 by 2 clock cycles. However, it takes the same number of clock cycles for integer division.

	32-bit	64-bit
MULT	6 - 9	7 - 10
DIV	42	74

Table 1: Integer multiply/divide cycles

Floating-Point Co-Processor

The R4700 incorporates an entire floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a "seamless" interface with the integer unit, decoding and executing instructions in parallel with the integer unit. The floating point coprocessor of the R4700 has improved the floating multiply operations compared to the R4600. This improves the peak MFLOPS to be equal to half of the pipeline clock rate.

Floating-Point Units

The R4700 floating-point execution units supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 4 cycles.

As in the IDT79R3010A and IDT79R4000, the R4700 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments and highly desirable for debugging in any environment.

The floating-point unit's operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with the IEEE Standard 754. The floating point unit improves the multiply compared to the R4600 by performing a single precision multiply in 4 clock cycles and a double precision multiply in 5 clock cycles.

Table 2 gives the latencies of some of the floating-point instructions in internal processor cycles. Note that multiplies are pipelined, so that a new multiply can be initiated every 4 pipeline cycles

Floating-Point General Register File

The floating-point register file is made up of thirty-two 64-bit registers. With the LDC1 and SDC1 instructions the floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store double-word instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

Operation	Single Precision	Double Precision
ADD	4	4
SUB	4	4
MUL	4	5
DIV	32	61
SQRT	31	60
CMP	3	3
FIX	4	4
FLOAT	6	6
ABS	1	1
MOV	1	1
NEG	1	1
LWC1, LDC1	2	2
SWC1, SDC1	1	1

Table 2: Floating-Point Cycles

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent. The R4700 CP0 is identical to that of the R4600.

The Memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer (the ITLB), a data address translation buffer (the DTLB), a Joint TLB (the JTLB), and co-processor registers used for the virtual memory mapping sub-system.

System Control Co-Processor Registers

The R4700 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4700 includes registers to implement a real-time cycle counting facility, to aid in cache diagnostic testing, and to assist in data error detection. Figure 3 shows the CP0 registers.

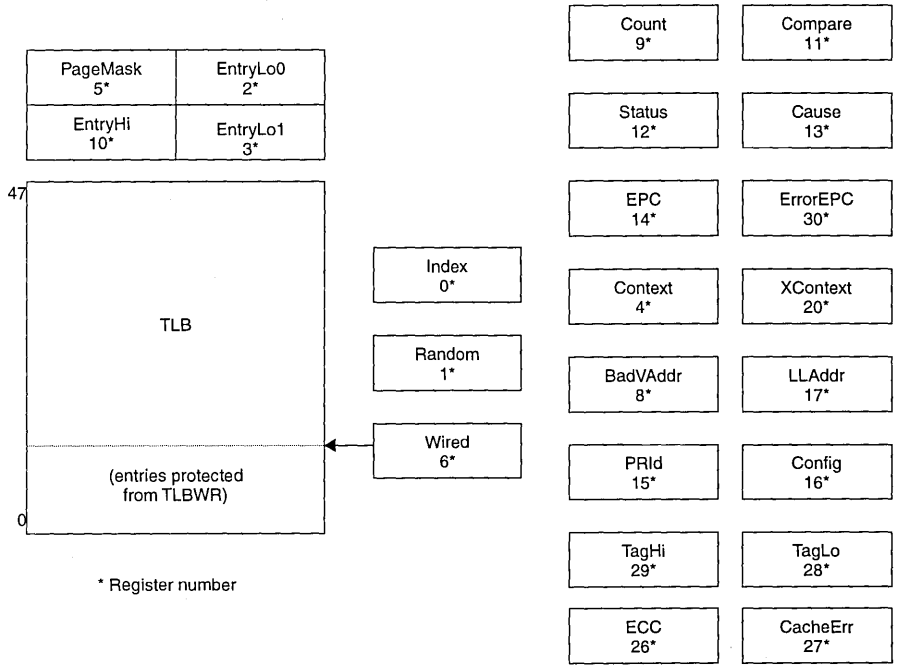


Figure 3: The R4700 CP0 Registers

Virtual to Physical Address Mapping

The R4700 provides three modes of virtual addressing:

- user mode
- supervisor mode
- kernel mode

This mechanism is available to system software to provide a secure environment for user processes. Bits in a status register determine which virtual addressing mode is used. In the user mode, the R4700 provides a single, uniform virtual address space of 256GB (2GB for 32-bit address mode).

When operating in the kernel mode, four distinct virtual address spaces, totalling 1024GB (4GB in 32-bit address mode), are simultaneously available and are differentiated by the high-order bits of the virtual address.

The R4700 processor also supports a supervisor mode in which the virtual address space is 256.5GB (2.5GB in 32-bit address mode), divided into three regions based on the high-order bits of the virtual address.

Figure 4 shows the address space layout for 32-bit virtual address operation.When the R4700 is configured for 64-bit virtual addressing, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout.

Joint TLB

For fast virtual-to-physical address decoding, the R4700 uses a large, fully associative TLB which maps 96 Virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space, and the replacement characteristics of various memory regions. First, the page size canbe configured, on a per-entry basis, to map a page size of 4KB to 16MB (in multiples of 4). A CP0 register is loaded with the page size of a mapping, and that size is entered into the TLB when a new entry is written. Thus, operating systems can provide special purpose maps; for example, a typical frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement

algorithm when a TLB miss occurs. The R4700 provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings can be locked into the TLB, and thus avoid being randomly replaced. This facilitates the design of real-time systems, by allowing deterministic access to critical software.

The joint TLB also contains information to control the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is: uncached, non-coherent write-back, non-coherent write-through write-allocate, non-coherent write-through no write-allocate. Non-coherent write-back is typically used for both code and data on the R4700; the write-through modes support more efficient frame buffer accesses than the R4000 family; cache coherency is not supported, however.

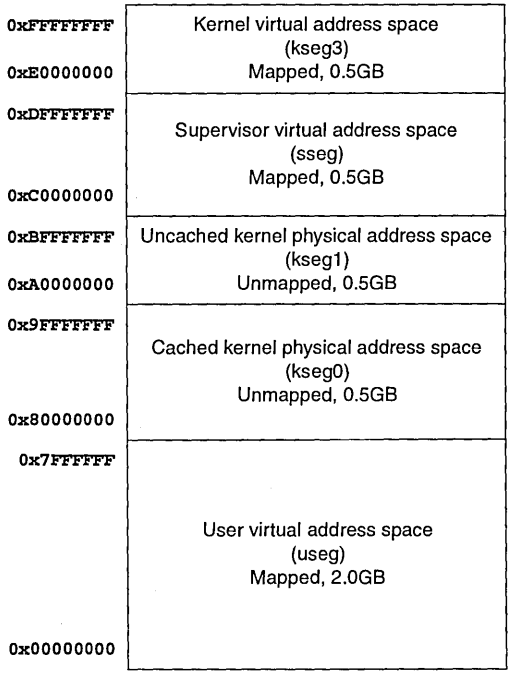


Figure 4: Kernel Mode Virtual Addressing (32-bit Mode)

Instruction TLB

The R4700 also incorporates a 2-entry instruction TLB. Each entry maps a 4KB page. The instruction TLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is invisible to the user.

Data TLB

The R4700 also incorporates a 4-entry data TLB. Each entry maps a 4KB page. The data TLB improves performance by allowing data address translation to occur in parallel with data address translation. When a miss occurs on an data address translation, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used half is filled. The operation of the DTLB is invisible to the user.

Furthermore, the large 2-way set-associative caches increase emulation performance of DOS and Windows 3.1 applications when running under Windows NT.

Cache Memory

In order to keep the R4700's high-performance pipeline full and operating efficiently, the R4700 incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 2.4GB per second at a pipeline clock frequency of 150MHz. The cache subsystem is the same as for the R4600.

Instruction Cache

The R4700 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 16KB in size and is protected with word parity.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 24-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 700MB/sec at 175MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill writes 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

Data Cache

For fast, single cycle data access, the R4700 includes a 16KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through on a per-page basis when it is appropriate, such as for frame buffers.

Associated with the Data Cache is the store buffer. When the R4700 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4700 to execute a store every processor cycle and to perform back-to-back stores without penalty.

Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four 64-bit address and 64-bit data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

System Interface

The R4700 supports a 64-bit system interface that is compatible with the R4000PC system interface. This interface operates from two clocks provided by the R4700, TClock[1:0] and RClock[1:0], at some division of the internal clock.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 700MB/sec at 175MHz.

Figure 5 shows a typical system using the R4700. In this example two banks of DRAMs are used to supply and accept data with a DDxxDD data pattern.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4700 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The data rate and the bus frequency at which the R4700 transmits data to the system interface are programmable via boot time mode control bits. Also, the rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4700. Again, the system designer has the flexibility to make these price/performance trade-offs.

System Command Bus

The R4700 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4700. Processor requests are initiated by the R4700 and responded to by an external device. External requests are issued by an external device and require the R4700 to respond.

The R4700 supports one to eight byte and block transfers on the SysAD bus. In the case of a sub-doubleword transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred.

Handshake Signals

There are six handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the R4700 whether it can accept a new

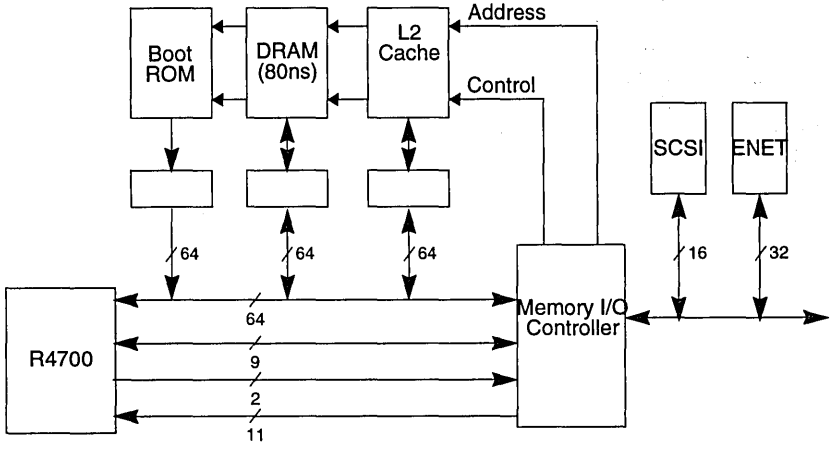


Figure 5: Typical Desktop System Block Diagram

read or write transaction. The R4700 samples these signals before deasserting the address on read and write requests.

ExtRqst and Release are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts ExtRqst. The R4700 responds by asserting Release to release the system interface to slave state.

ValidOut and ValidIn are used by the R4700 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4700 asserts ValidOut when it is driving these buses with a valid command or data, and the external device drives ValidIn when it has control of the buses and is driving a valid command or data.

Non-overlapping System Interface

The R4700 uses a non-overlapping system interface, compatible with the R4600. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4700 issues another request. The R4700 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4700.

For processor read transaction the R4700 asserts ValidOut and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has RdRdy asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting Release. The external device can then begin sending the data.

Figure 6 shows a processor block read request and the external agent read response. The read latency is 4 cycles (ValidOut to ValidIn), and the response data pattern is DDxxDD. Figure 7 shows a processor block write.

Write Reissue and Pipeline Write

The R4600 and the R4700 implement additional write protocols designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of 2 cycles per write. A write issues if WrRdy is asserted 2 cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issues again. Pipelined writes have the same 2-cycle per write repeat rate, but can issue one more write after WrRdy de-asserts. They still follow the issue rule as R4x00 mode for other writes.

External Requests

The R4700 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4700 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus. It also may issue requests to the processor, such as a request for the R4700 to write to the R4700 interrupt register.

The following is a list of the supported external requests:

- Write
- Null
- Read Response

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost seriel EEPROM; alternatively the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the VccOK Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

JTAG Interface

For compatibility with the R4000PC, the R4700 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

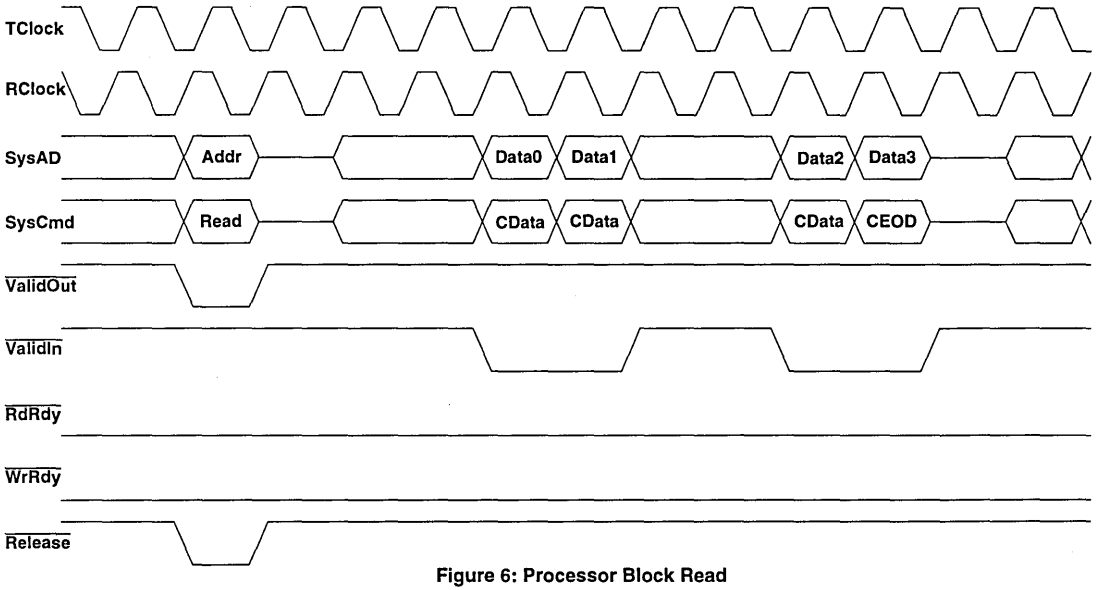


Figure 6: Processor Block Read

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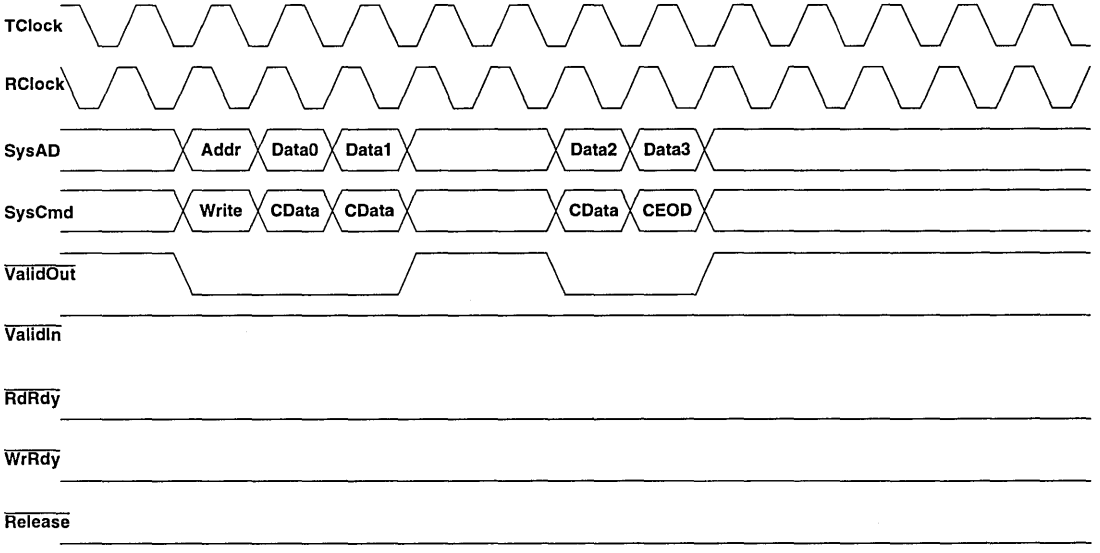


Figure 7: Processor Block Write

Boot-Time Modes

The boot-time serial mode stream is defined in Table 3. Bit 0 is the bit presented to the processor when VccOK is asserted; bit 255 is the last.

Power Management

CP0 is also used to control the power management for the R4700. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU. The standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by an interrupt.

Mode bit	Description	Mode bit	Description
0	reserved (must be zero)	14..13	Output driver strength 10 → 100% strength (fastest), 11 → 83% strength, 00 → 67% strength, 01 → 50% strength (slowest)
4..1	Writeback data rate 0 → D, 1 → DDx, 2 → DDxx, 3 → DxDx, 4 → DDxxx, 5 → DDxxxx, 6 → DxxDxx, 7 → DDxxxxxx, 8 → DxxxDxxx, 9-15 reserved	bit 15	0 -> TClock[0] enabled 1 -> TClock[0] disabled
7..5	Clock divisor 0 → 2, 1 → 3, 2 → 4, 3 → 5, 4 → 6, 5 → 7, 6 → 8, 7 reserved	bit 16	0 -> TClock[1] enabled 1 -> TClock[1] disabled
8	0 → Little endian, 1 → Big endian	bit 17	0 -> RClock[0] enabled 1 -> RClock[0] disabled
10..9	00 → R4000 compatible, 01 → reserved, 10 → pipelined writes, 11 → write re-issue	bit 18	0 -> RClock[1] enabled 1 -> RClock[1] disabled
11	Disable the timer interrupt on Int[5]. 0 → Enabled 1 → Disabled	255..19	Reserved (must be zero)
12	reserved (must be zero)		

Table 3: Boot time mode stream

PIN DESCRIPTION

The following is a list of interface, interrupt, and miscellaneous pins available on the R4700. Signals marked with one asterisk are active when low.

Pin Name	Type	Description
System interface:		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity for the R4700 unused on input and zero on output.
Clock/control interface:		
MasterClock	Input	Master clock Master clock input at one half the processor operating frequency.
MasterOut	Output	Master clock out Master clock output aligned with MasterClock.
RClock(1:0)	Output	Receive clocks Two identical receive clocks at the system interface frequency.
TClock(1:0)	Output	Transmit clocks Two identical transmit clocks at the system interface frequency.
IOOut	Output	Reserved for future output Always HIGH.
IOIn	Input	Reserved for future input Should be driven HIGH.
SyncOut	Output	Synchronization clock out Synchronization clock output. Must be connected to SyncIn through an interconnect that models the interconnect between MasterOut, TClock, RClock, and the external agent.

Pin Name	Type	Description
SyncIn	Input	Synchronization clock in Synchronization clock input. See SyncOut.
Fault*	Output	Fault Always HIGH.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.

Interrupt interface:

Int*(5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Initialization interface:

Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4700 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. The clocks SClock, TClock, and RClock begin to cycle and are synchronized with the de-assertion edge of ColdReset. ColdReset must be de-asserted synchronously with MasterOut.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterOut.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

** For compatibility with the R4600, the R4650 supports the JTAG interface pins, with the serial input connected to serial output. Boundary scan is not supported.

Standby Mode Operations

The R4700 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as "Standby Mode" .

Entering Standby Mode

Executing the WAIT iunstruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, some of the input pin clocks (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) and the output clocks (TClock[1:0], RClock[1:0], SyncOut, Modeclock and MasterOut) will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (i.e. the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Thermal Considerations

The R4700 utilizes special packaging techniques to improve the thermal properties of high-speed processors. The R4700 is packaged using cavity down packaging in a 179-pin PGA package with integral thermal slug, and a 208-lead MQUAD QFP package. These packages effectively dissipate the power of the CPU, increasing device reliability.

The R47000 utilizes the MQUAD package (the "MS" package), which is an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing. Due to the heat-spreading effect of the aluminum, the package allows for an efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The R4700 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device.

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 5.

	$\varnothing_{CA}$					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
PGA	16	7	5	3	2.5	2
MQUAD	20	12	9	8	7	6

Table 5: Thermal Resistance ($\varnothing_{CA}$) at Various Airflows

Note that the R4700 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79R4600/R4700 Hardware User's Manual.*

5

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	RV4700 3.3V±5%	R4700 5.0V±5%	Unit
		Commercial	Commercial	
V_{TERM}	Terminal Voltage with respect to GND	−0.5[2] to +4.6	−0.5[2] to +7.0	V
T_C	Operating Temperature (case)	0 to +85	0 to +85	°C
T_{BIAS}	Case Temperature Under Bias	−55 to +125	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	−55 to +125	°C
I_{IN}	DC Input Current	20[3]	20[3]	mA
I_{OUT}	DC Output Current	50	50[4]	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = −2.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. When V_{IN} < 0V or V_{IN} > V_{CC}
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	RV4700	R4700
			V_{CC}	V_{CC}
Commercial	0°C to +85°C (Case)	0V	3.3V±5%	5.0V±5%

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4700

(V_{CC} = 5.0±5%, T_{CASE} = 0°C to +85°C)

Parameter	R4700 100MHz		R4700 133MHz		R4700 150MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	3.5V	—	3.5V	—	3.5V	—	
V_{IL}	–0.5V	0.8V	–0.5V	0.8V	–0.5V	0.8V	—
V_{IH}	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

Power Consumption—R4700

Parameter		R4700 100MHz		R4700 133MHz		R4700 150MHz		Conditions
		Typical[9]	Max	Typical[9]	Max	Typical[9]	Max	
System Condition:		100/25MHz		133/33MHz		150/38MHz		—
I_{CC}	standby	—	175mA	—	225mA	—	260mA	C_L = 0pF[8]
		—	250mA	—	325mA	—	370mA	C_L = 50pF
	active	875mA	1000mA	1175mA	1300mA	1325mA	1500mA	C_L = 0pF No SysAd activity[8]
		975mA	1200mA	1275mA	1500mA	1450mA	1700mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		975mA	1400mA	1275mA	1675mA	1450mA	1900mA	C_L = 50pF Pipelined writes or write re-issue T_C = 25°C[8]

5

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4700

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—R4700

Parameter	Symbol	Test Conditions	R4700 100MHz		R4700 133MHz		R4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	4	—	3	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	4	—	3	—	3	—	ns
MasterClock Frequency(5)	—	—	25	50	25	67	25	75	MHz
MasterClock Period	t_{MCP}	—	20	40	15	40	13.3	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$(8)	—	—	±500	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	4	—	3.5	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	4	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256*t_{MCP}	—	256*t_{MCP}	—	256*t_{MCP}	ns
JTAG Clock Period	$t_{JTAGCKP}$	—	—	4*t_{MCP}	—	4*t_{MCP}	—	4*t_{MCP}	ns

NOTES:
5. Operation of the R4700 is only guaranteed with the Phase Lock Loop enabled.
6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.
8. Guaranteed by Design.
9. Typical integer instruction mix and cache miss rates.

System Interface Parameters—R4700[6]

Parameter	Symbol	Test Conditions	R4700 100MHz		R4700 133MHz		R4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output[7]	t_{DO}	$mode_{14..13}$ = 10 (fastest)	1.0	9	1.0	9	1.0	8	ns
		$mode_{14..13}$ = 11	1.3	11	1.3	10	1.3	9.3	ns
		$mode_{14..13}$ = 00	1.6	13	1.6	11	1.6	10.6	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Setup	t_{DS}	t_{rise} = 5ns, t_{fall} = 5ns	3.5	—	3.5	—	3.5	—	ns
Data Hold	t_{DH}		1.5	—	1.5	—	1.5	—	ns

Boot Time Interface Parameters—R4700

Parameter	Symbol	Test Conditions	R4700 100MHz		R4700 133MHz		R4700 150MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

Capacitive Load Deration—R4700

Parameter	Symbol	R4700 100MHz		R4700 133MHz		R4700 150MHz		Units
		Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	2	—	2	—	2	ns/25pF

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—RV4700

(V_{CC} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Conditions
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
V_{OHC}	—	—	—	—	—	—	—	—	—
V_{ILC}	—	—	—	—	—	—	—	—	—
V_{IHC}	—	—	—	—	—	—	—	—	—
C_{IN}	—	10pF	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	—	20uA	Input/Output Leakage

Power Consumption—RV4700

Parameter		RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Conditions
		Typical (9)	Max	Typical (9)	Max	Typical (9)	Max	Typical (9)	Max	
System Condition:		100/25MHz		133/33MHz		150/38MHz		175/44MHz		—
I_{CC}	standby	—	125mA	—	175mA	—	200mA	—	200mA	C_L = 0pF(8)
		—	175mA	—	225mA	—	250mA	—	250mA	C_L = 50pF
	active	575mA	875mA	775mA	1150mA	875mA	1300mA	1025mA	1500mA	C_L = 0pF, No SysAd activity(8)
		650mA	1100mA	850mA	1375mA	950mA	1550mA	1200mA	1800mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		650mA	1275mA	850mA	1525mA	950mA	1725mA	1200mA	2000mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C(8)

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—RV4700

(V_{CC}=3.3V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—RV4700

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		Units
			Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	4	—	3	—	ns
MasterClock Frequency(5)	—	—	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$(8)	—	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	ns

Parameter	Symbol	Test Conditions	RV4700 150MHz		RV4700 175MHz		Units
			Min	Max	Min	Max	
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	3	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	3	—	3	—	ns
MasterClock Frequency(10)	—	—	25	75	25	87.5	MHz
MasterClock Period	t_{MCP}	—	13.3	40	11.4	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	ps
Clock Jitter for MasterOut, SyncOut, TClock, RClock	$t_{JitterOut}$(8)	—	—	±500	—	±500	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	3.5	—	3.5	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	3.5	—	3.5	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTE:
10.Operation of the RV4700 is only guaranteed with the Phase Lock Loop enabled.

System Interface Parameters—RV4700[6]

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Output[7]	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	9	1.0	9	1.0	8	1.0	8	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	2.0	12	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	3.5	—	3.5	—	3.5	—	3.5	—	ns
Data Hold	t_{DH}		1.5	—	1.5	—	1.5	—	1.5	—	ns

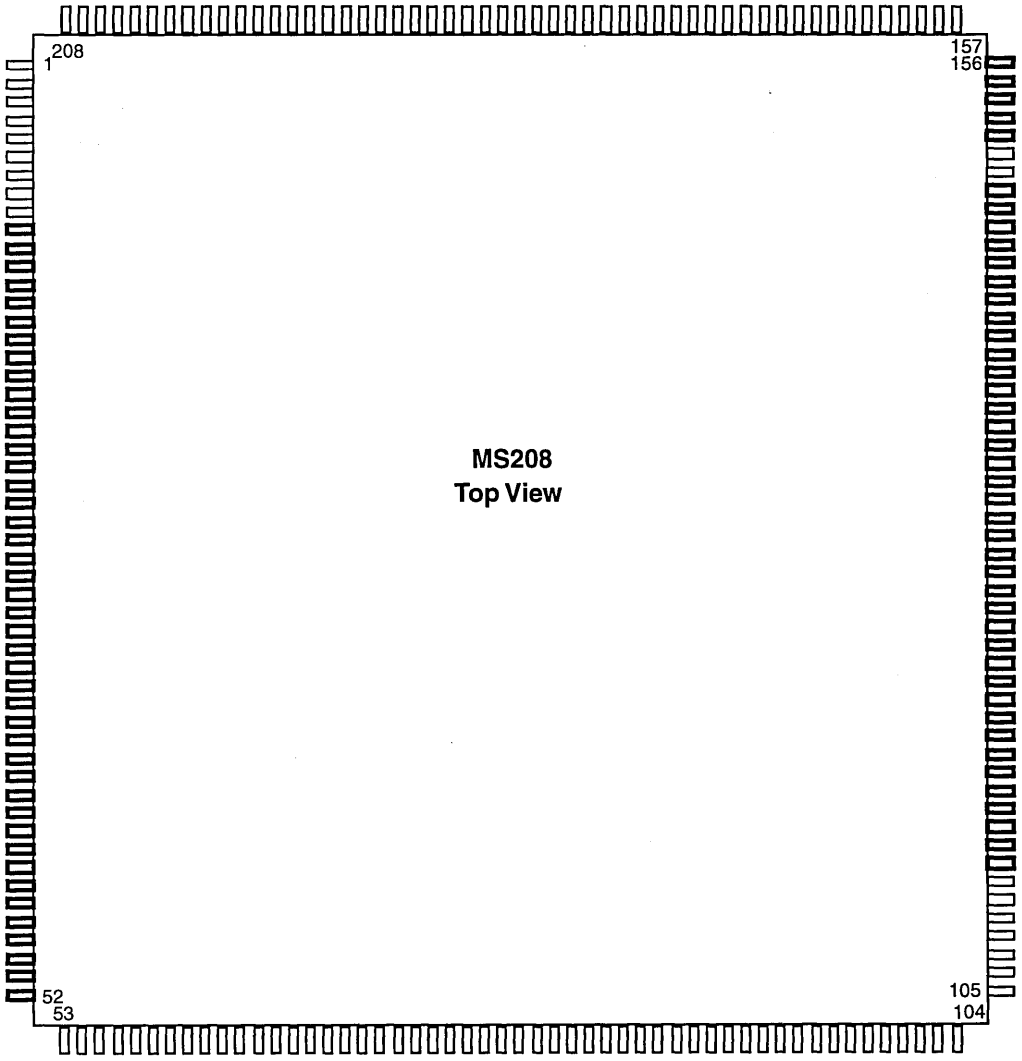
Boot Time Interface Parameters—RV4700

Parameter	Symbol	Test Conditions	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	0	—	Master Clock Cycle

Capacitive Load Deration—RV4700

Parameter	Symbol	RV4700 100MHz		RV4700 133MHz		RV4700 150MHz		RV4700 175MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	2	—	2	—	2	—	2	ns/25pF

PHYSICAL SPECIFICATIONS — 208-PIN MQUAD



MS208
Top View

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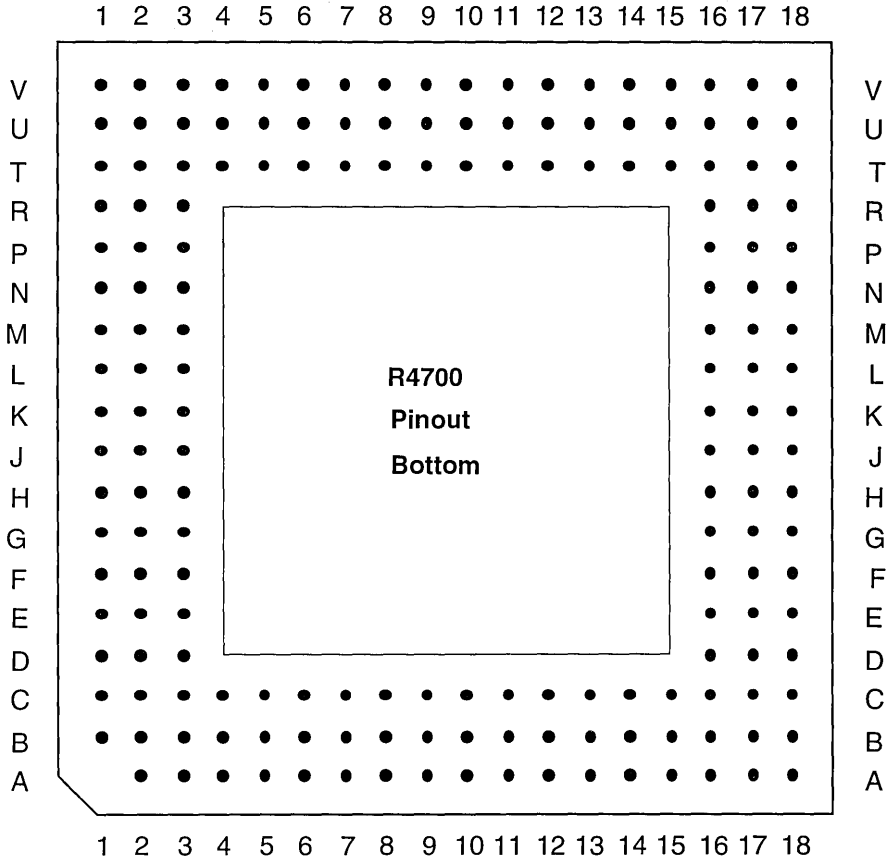
PHYSICAL SPECIFICATIONS — PGA



2884 drw 12

R4700 MQUAD PACKAGE PIN-OUT*

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	Vss	55	SysCmd2	107	N.C.	159	RClock0
4	Vcc	56	SysAD36	108	N.C.	160	RClock1
5	SysAD45	57	SysAD4	109	Vcc	161	SyncOut
6	SysAD13	58	SysCmd1	110	Vss	162	SysAD30
7	Fault*	59	Vss	111	SysAD21	163	Vcc
8	SysAD44	60	Vcc	112	SysAD53	164	Vss
9	Vss	61	SysAD35	113	RdRdy*	165	SysAD62
10	Vcc	62	SysAD3	114	ModeIn	166	MasterOut
11	SysAD12	63	SysCmd0	115	SysAD22	167	SysAD31
12	SysCmdP	64	SysAD34	116	SysAD54	168	SysAD63
13	SysAD43	65	Vss	117	Vcc	169	Vcc
14	SysAD11	66	Vcc	118	Vss	170	Vss
15	Vss	67	N.C.	119	Release*	171	VccOK
16	Vcc	68	N.C.	120	SysAD23	172	SysADC3
17	SysCmd8	69	SysAD2	121	SysAD55	173	SysADC7
18	SysAD42	70	Int5*	122	NMI*	174	Vcc
19	SysAD10	71	SysAD33	123	Vcc	175	Vss
20	SysCmd7	72	SysAD1	124	Vss	176	N.C.
21	Vss	73	Vss	125	SysADC2	177	N.C.
22	Vcc	74	Vcc	126	SysADC6	178	N.C.
23	SysAD41	75	Int4*	127	Vcc	179	N.C.
24	SysAD9	76	SysAD32	128	SysAD24	180	N.C.
25	SysCmd6	77	SysAD0	129	Vcc	181	VccP
26	SysAD40	78	Int3*	130	Vss	182	VssP
27	N.C.	79	Vss	131	SysAD56	183	N.C.
28	N.C.	80	Vcc	132	N.C.	184	N.C.
29	Vss	81	Int2*	133	SysAD25	185	MasterClock
30	Vcc	82	SysAD16	134	SysAD57	186	Vcc
31	SysAD8	83	SysAD48	135	Vcc	187	Vss
32	SysCmd5	84	Int1*	136	Vss	188	SyncIn
33	SysADC4	85	Vss	137	IOOut	189	Vcc
34	SysADC0	86	Vcc	138	SysAD26	190	Vss
35	Vss	87	SysAD17	139	SysAD58	191	N.C.
36	Vcc	88	SysAD49	140	IOIn	192	SysADC5
37	SysCmd4	89	Int0*	141	Vcc	193	SysADC1
38	SysAD39	90	SysAD18	142	Vss	194	N.C.
39	SysAD7	91	Vss	143	SysAD27	195	Vcc
40	SysCMD3	92	Vcc	144	SysAD59	196	Vss
41	Vss	93	SysAD50	145	ColdReset*	197	SysAD47
42	Vcc	94	ValidIn*	146	SysAD28	198	SysAD15
43	SysAD38	95	SysAD19	147	Vcc	199	N.C.
44	SysAD6	96	SysAD51	148	Vss	200	SysAD46
45	ModeClock	97	Vss	149	SysAD60	201	Vcc
46	WrRdy*	98	Vcc	150	Reset*	202	Vss
47	SysAD37	99	ValidOut*	151	SysAD29	203	SysAD14
48	SysAD5	100	SysAD20	152	SysAD61	204	N.C.
49	Vss	101	SysAD52	153	Vcc	205	TClock1
50	Vcc	102	ExtRqst*	154	Vss	206	TClock0
51	N.C.	103	N.C.	155	N.C.	207	N.C.
52	N.C.	104	N.C.	156	N.C.	208	N.C.

*N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

R4700 PGA Pin-out

Function	Pin
$\overline{\text{ColdReset}}$	T14
$\overline{\text{ExtRqst}}$	U2
$\overline{\text{Fault}}$	B16
Reserved O (NC)	U10
Reserved I (Vcc)	T9
IOIn	T13
IOOut	U12
Int0	N2
Int1	L3
Int2	K3
Int3	J3
Int4	H3
Int5	F2
MasterClock	J17
MasterOut	P17
ModeClock	B4
ModeIn	U4
NMI	U7
RClock0	T17
RClock1	R16
$\overline{\text{RdRdy}}$	T5
Release	V5
$\overline{\text{Reset}}$	U16
SyncIn	J16
SyncOut	P16
SysAD0	J2
SysAD1	G2
SysAD2	E1
SysAD3	E3
SysAD4	C2
SysAD5	C4
SysAD6	B5
SysAD7	B6
SysAD8	B9

Function	Pin
SysAD9	B11
SysAD10	C12
SysAD11	B14
SysAD12	B15
SysAD13	C16
SysAD14	D17
SysAD15	E18
SysAD16	K2
SysAD17	M2
SysAD18	P1
SysAD19	P3
SysAD20	T2
SysAD21	T4
SysAD22	U5
SysAD23	U6
SysAD24	U9
SysAD25	U11
SysAD26	T12
SysAD27	U14
SysAD28	U15
SysAD29	T16
SysAD30	R17
SysAD31	M16
SysAD32	H2
SysAD33	G3
SysAD34	F3
SysAD35	D2
SysAD36	C3
SysAD37	B3
SysAD38	C6
SysAD39	C7
SysAD40	C10
SysAD41	C11
SysAD42	B13
SysAD43	A15

Function	Pin
SysAD44	C15
SysAD45	B17
SysAD46	E17
SysAD47	F17
SysAD48	L2
SysAD49	M3
SysAD50	N3
SysAD51	R2
SysAD52	T3
SysAD53	U3
SysAD54	T6
SysAD55	T7
SysAD56	T10
SysAD57	T11
SysAD58	U13
SysAD59	V15
SysAD60	T15
SysAD61	U17
SysAD62	N16
SysAD63	N17
SysADC0	C8
SysADC1	G17
SysADC2	T8
SysADC3	L16
SysADC4	B8
SysADC5	H16
SysADC6	U8
SysADC7	L17
SysCmd0	E2
SysCmd1	D3
SysCmd2	B2
SysCmd3	A5
SysCmd4	B7
SysCmd5	C9
SysCmd6	B10

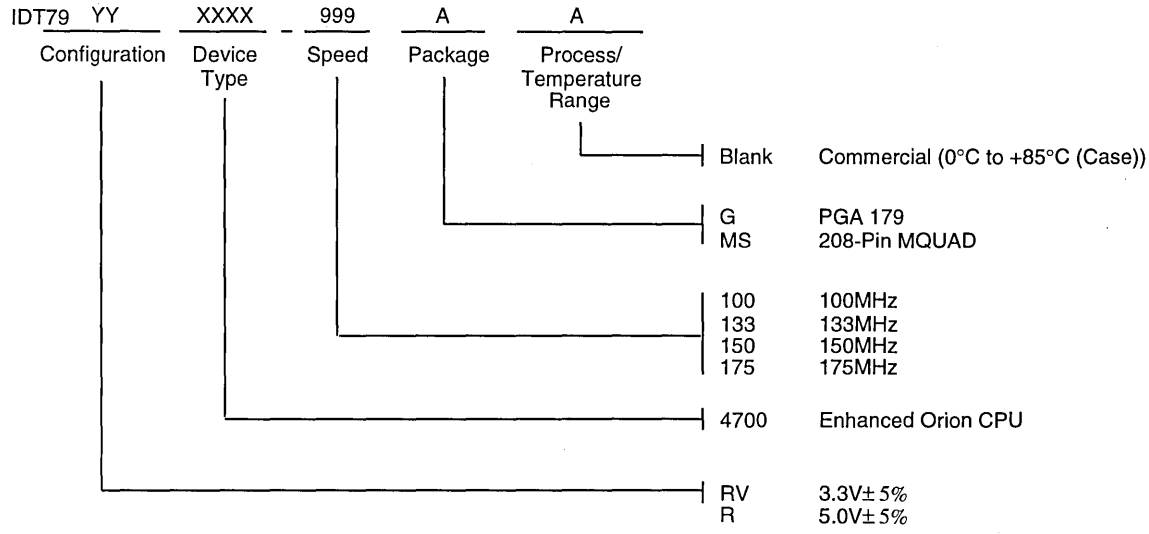
Function	Pin
SysCmd7	B12
SysCmd8	C13
SysCmdP	C14
TClock0	C17
TClock1	D16
VccOk	M17
$\overline{\text{ValidIn}}$	P2
$\overline{\text{ValidOut}}$	R3
$\overline{\text{WrRdy}}$	C5
VccP	K17
VssP	K16
Vcc	A2
Vcc	A4
Reserved I (Vcc)	A7
Vcc	A9
Vcc	A11
Vcc	A13
Vcc	A16
Vcc	B18
Vcc	C1
Vcc	D18
Vcc	F1
Vcc	G18
Vcc	H1
Vcc	J18
Vcc	K1
Vcc	L18
Vcc	M1
Vcc	N18
Vcc	R1
Vcc	T18
Vcc	U1
Vcc	V3
Vcc	V6
Vcc	V8

Function	Pin
Vcc	V10
Vcc	V12
Vcc	V14
Vcc	V17
Vss	A3
Vss	A6
Vss	A8
Vss	A10
Vss	A12
Vss	A14
Vss	A17
Vss	A18
Vss	B1
Vss	C18
Vss	D1
Vss	F18
Vss	G1
Vss	H18
Vss	J1
Vss	K18
Vss	L1
Vss	M18
Vss	N1
Vss	P18
Vss	R18
Vss	T1
Vss	U18
Vss	V1
Vss	V2
Vss	V4
Vss	V7
Vss	V9
Vss	V11
Vss	V13
Vss	V16

Function	Pin
Vss	V18
JTMS	E16
JTDO	F16
JTDI	G16
JTCK	H17

5

ORDERING INFORMATION



Valid Combinations:

IDT	79R4700 - 100, 133, 150	PGA, MQUAD Package
	79RV4700 - 100, 133, 150, 175	PGA, MQUAD Package

RISC SUPPORT COMPONENTS

A RISC microprocessor is an important, but not self-sufficient, element of a high-performance general or embedded computing system. Equally important is the memory system (both cache and main memory) and the I/O interface to the execution core.

By providing these system solutions as building blocks, IDT allows its customers the maximum flexibility in achieving their price/performance goals while minimizing time-to-market, real estate and complexity of the end system.

This section of the data book contains some selected devices which have either been specifically designed for particular RISC processors or found to be exceptionally useful in these high-performance systems.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

SINGLE-CHIP SYSTEM CONTROLLER

IDT79R3715
ADVANCE INFORMATION

FEATURES

- System Controller for the pin-compatible IDT R30xx family of processors
- DRAM Controller
  - 1 - 40 MB directly, 1 - 3 banks directly
  - Device depth supported: 256K - 4M
  - Non-interleave
- ROM Controller
  - 1 - 20MB, Address-space support bank size: 1- 8MB
  - Support for standard and burst ROMs
  - Support for interleave or non-interleave
- Direct Interface to external DMA master
- I/O Bus follows 8/16-bit Intel 80186 style
- I/O Controller
  - Two 8-bit and two 16-bit external channels
  - DMA and non-DMA access for the 8-bit channels
  - 8-32 packing, 32-8 unpacking logic for DMA access
  - 16-32 packing, 32-16 unpacking for CPU/ external DMA master coprocessor accesses
  - Round robin arbitration
  - Programmable timing for I/O and control signals
  - Big and Little Endian support
- PCMCIA Support
  - Through 16-bit I/O bus, using simple glue logic
  - 16-bit to 32-bit packing and 32-bit to 16-bit unpacking
  - Big and Little Endian support
  - 256MB address space dedicated to 2 PCMCIA slots
- 24-bit Timer/Counter, In-Circuit testing capability
- Centronics Interface
  - Bi-directional Centronics, compliant with IEEE1284
  - Supports DMA and CPU controlled transfers
  - Supports the following modes: Compatible; Nibble; Byte; ECP; EPP
- Interrupt Controller
  - 6 external level interrupts (through the PIO pins)
  - 14 internal interrupts
  - Individual interrupt mask capability, enabling polling or interrupt-driven systems
- General Purpose I/O
  - Six programmable Input (interrupts) or Output pins

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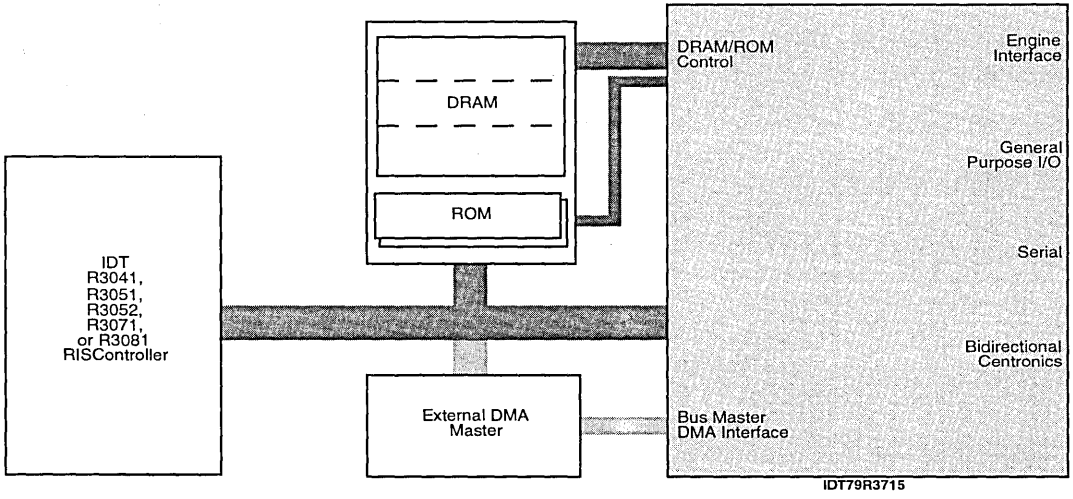


IDT79R3715 System Organization

3715-20

OVERVIEW

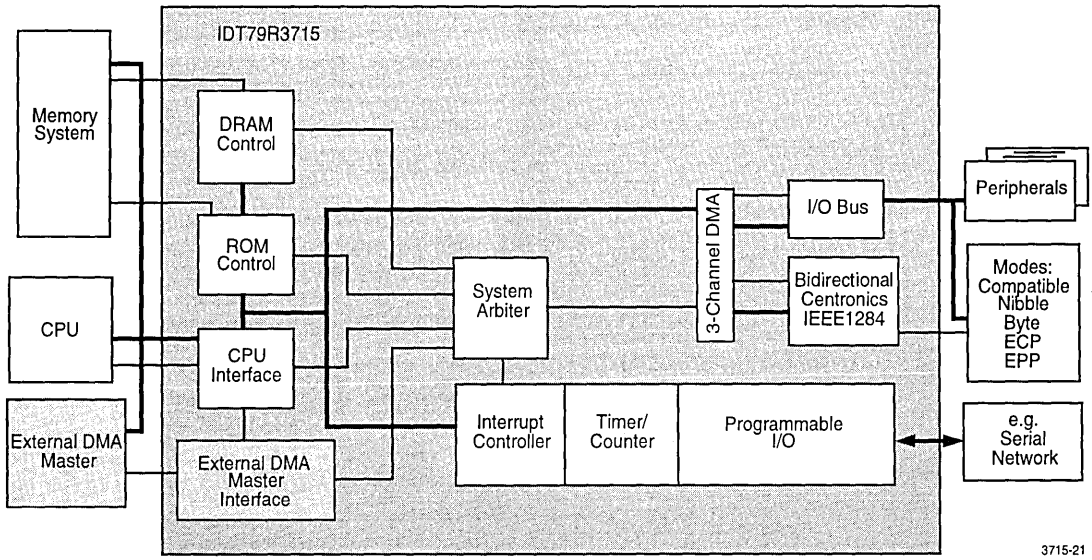
The IDT79R3715 is a single-chip System Controller designed to complement IDT's R30xx family of 32-bit embedded processors. It has all of the features necessary to maximize the performance of a RISC-based system and reduce the overall system chip count.

The R3715 can move large amounts of data quickly without the need for processor intervention. It also achieves a significant reduction in system cost by its high level of integration. Additional savings come from the architecture of the I/O controller, which allows for the utilization of low cost peripheral components (disk controller, network controller, etc.), while attaining the higher level of performance only associated with costlier components.

Some of the architectural characteristics that result in very high performance include:

- incorporating a tightly coupled interface to any of the R30xx RISC CPUs
- minimizing latency to critical resources
- partitioning the system in a balanced way to attain efficient use of shared resources
- enabling several simultaneous operations in the system

The R3715 is ideal for modular design of laser printers because it allows a high level of programmability and incorporates the control logic for an industry standard interface to peripherals. This gives OEMs the ability to offer several products from the same basic design, as well as the ability to upgrade systems in the field. The block diagram that follows shows the R3715 configuration.



IDT79R3715 Block Diagram

FUNCTIONAL DESCRIPTION

Processor Interface

The R3715 has a glueless interface to the IDT R3041/51/52/71/81 family of RISC processors. It supports these devices in both slave and master modes of operation. As slave, they support CPU access to memory and I/O devices, and as master, handle accesses on the A/D bus.

As slave the R3715 supports processor single transfer read or write, as well as burst read access. Each supports processor access to the ROM, DRAM, devices on the I/O bus, and the R3715 internal registers. Burst read is supported only for DRAM or ROM read access. ACK* and RDCEN* timing is fixed for the R3715 registers. DRAM access can be extended by one clock, and access timing for ROM and I/O are programmable.

As master the R3715 will request the bus by asserting BUSREQ* when a DMA source (internal or external) needs to transfer data to or from the DRAM / ROM / I/O Channel.

The priority between the DMA sources is in the following descending order:

- Access in process
- I/O DMA
- External DMA master

The CPU will get ownership of the A/D bus for at least one cycle after four DMA accesses. This assumes that each external DMA master (external agent) bus possession is counted as one, regardless of the number of transfers it executes on the bus. In the default state, when there is no DMA request, the bus is owned by the CPU.

Figure 2.1 shows the CPU-to-R3715 interface.

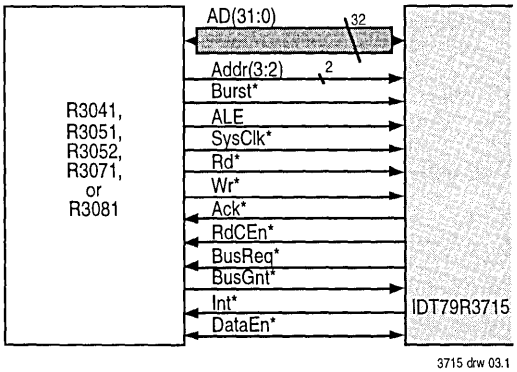


Figure 2.1 RISController to R3715 Interface

External DMA Master Interface

The R3715 has a simple interface to the external DMA master coprocessor. It supports the external DMA master operation in its slave and master modes. As slave it supports the processor read and write accesses to the external DMA master, and as master it enables access to the DRAM, ROM, and 16 bit I/O bus (for font cartridges). The R3715 directly controls the data buffers and the address buffer needed to isolate the external DMA master from the A/D bus.

The R3715 decodes CPU access to the external DMA master and asserts ECS*, EAS*, and EDS*. The address is latched into an external transparent latch (373-type) when the processor asserts ALE and is driven into the multiplexed bus (DAL[31:0]) by EATOE*. Data is driven to or from the external DMA master by transceivers controlled by EADDIR* and EADOE*. To end an external DMA master cycle the R3715 asserts RDCEN* and ACK* to the CPU when the external DMA master asserts EDTACK*.

In external DMA master mode, the external DMA master requests the bus by asserting EBREQ*. The R3715 will grant the bus by asserting EBGNT* (provided no other DMA device has requested the bus and provided also that it was granted by the CPU to the R3715). The external DMA master will assert EAS* first, and then EDS*, to initiate an access to a system resource (e.g. DRAM). The R3715 will assert EADOE* and EADDIR* to drive the external DMA master address, and ALE to latch it. In the data phase it will assert EADDIR* and EADOE* according to the access direction (Read or Write).

To end the cycle the R3715 will assert EDTACK* to the external DMA master. When it does not require the bus any longer the external DMA master will release it by deasserting EBREQ*

External access to the DRAM takes 5 clocks from EAS* to EDTACK*. Frequencies above 25 MHz may need an additional clock cycle. One clock can be added to this interval by using the ExtCas bit in the DRAM control register.

Figure 2.2 on the following page shows a typical implementation of an external DMA master interface.

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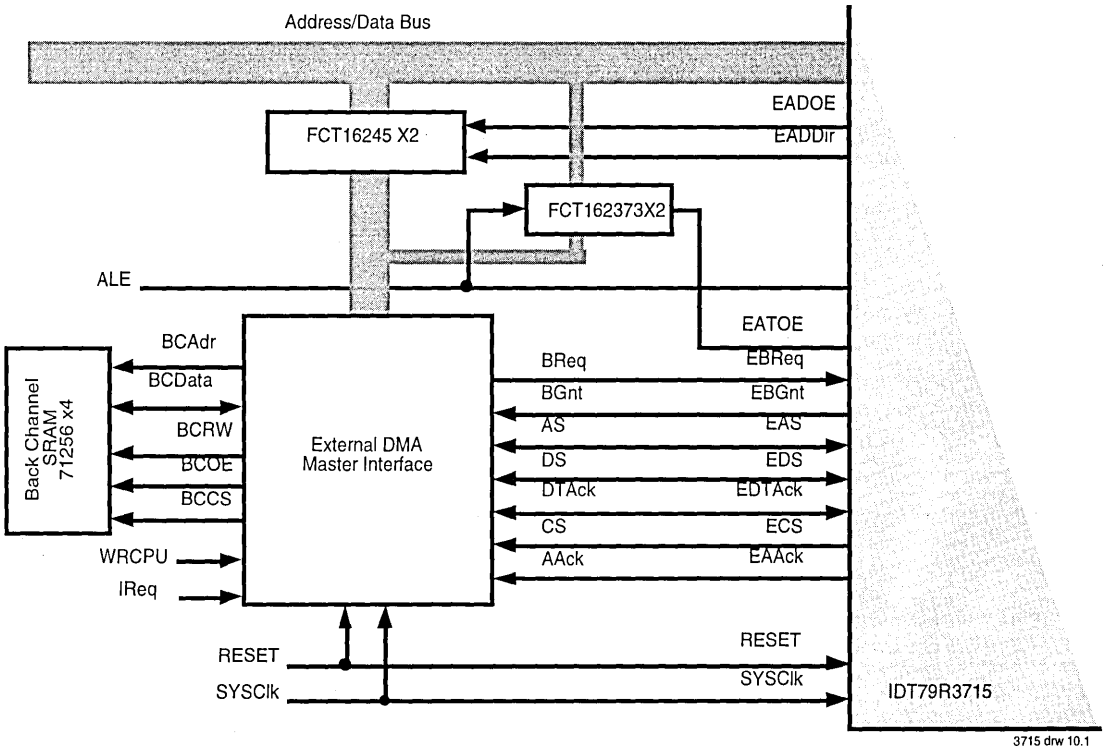

Figure 2.2 External DMA Master Coprocessor Implementation

ROM

The ROM controller supports up to 20 Mbyte of memory with several device types and system configurations. To support these system and device options, the assertion time of RDCEN* and ACK* by the R3715 can be programmed, thus accommodating different types of memory architectures, including standard ROMs, interleaved ROMs, and burst ROMs.

There are three CS signals to support up to three banks of ROM. Each ROM bank can be either non-interleaved or interleaved (composed of 2 leaves of ROM differentiated by ADDR[2]). ROMCS[2]* controls the boot bank and has a fixed address space of 4 Mbyte. Address space for ROMCS[1]* and ROMCS[0]* is programmable to 1, 2, 4, or 8 Mbyte.

The R3715 puts the 3 ROM bank address ranges in a contiguous address space. In other words, the start address of the next ROMCS[x]* will follow the last address of the previous ROMCS[x-1]*. For interleaved support, ROMOE* is provided to control the OE of the interleave multiplexer. The R3715 also supports burst ROM, and can be made to write to the ROM space (for flash or debug) with additional glue logic.

After reset, the R3715 is configured with the maximum number of wait states between each data transfer (16 clocks between each RDCEN*) and 64 clocks between ROMCS[x]* to ACK*. The initial (reset) space size for ROMCS[1]* and ROMCS[0]* is 1 Mbyte, and 4Mbytes for ROMCS[2]*.

Figure 2.3 on the following page shows the configuration of the ROM/DRAM memory system.

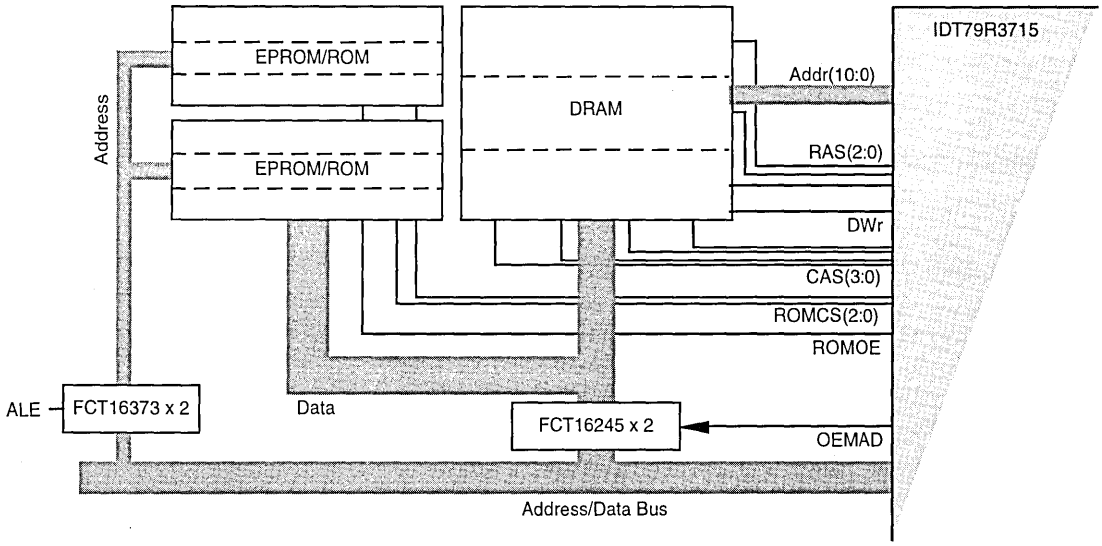

Figure 2.3 R3715 ROM/DRAM Memory System 3715 drw 04.1

DRAM

The DRAM controller supports directly 1 to 40 Mbytes of DRAM, with up to three non-interleaved banks. The address space starts at physical address 0. The DRAM device types supported have the following attributes: page mode, early write, and "CAS before RAS" refresh.

The DRAM controller supports single transfer reads and writes and burst reads. Various DRAM device depths are supported and the address space is continuous for the selected configuration. The DRAM controller can be configured to support different device depth for the base bank (RAS[0]*) and the extension banks (RAS[1]* and RAS[2]*).

For systems running at high frequency there is an option to extend the CAS* signals by an additional cycle. An external DMA master may sample data on the rising edge of SYSCLK*, and the CPU on the falling edge. It is possible to extend the CAS* by one cycle for external DMA master accesses. To minimize the refresh penalty IDT recommends that you program the refresh frequency according to the value of SYSCLK*.

The initial values of the R3715 control registers at reset are shown in the tables in Section 3.

PIO Port

Each of the PIO[5:0] pins can be individually programmed to be an output or input pin by writing to the PIO Control register. When programmed as an input pin it can be used as a level (active LOW) interrupt. The PIO pins are synchronized and pulled up internally. At reset, all PIOs are initialized as inputs.

Interrupt Controller

Each interrupt source on the R3715 is maskable. The Cause register bit will reflect the cause of the interrupt, and writing a '0' into it will acknowledge the internal interrupt. For example - if the "BandInt" bit was active, the CPU should write 'fffB' into the Cause register, in order to reset the interrupt flag.

The external interrupts, PIO[5:0], are acknowledged at the source of the interrupt (the interrupt flag is deasserted when PIO is inactive), the corresponding bits in the Interrupt Cause register are read only.

At reset, all interrupts are masked in the mask register.

DMA-Based Serial Interface

One of the DMA-supported I/O channels can be used to support protocols such as AppleTalk directly, with only the addition of an external communication controller, such as the 85C30 or 85C230, and the I/O interface devices it requires. The R3715 I/O FIFO and Burst DMA capabilities aid in separating the real-time demands of protocols such as AppleTalk from the real-time demands of the engine interface, but without the cost implications of external buffering.

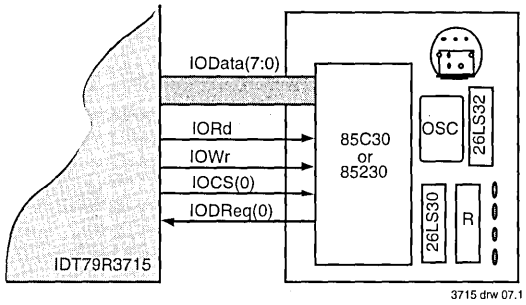

Figure 2.4 DMA-Supported AppleTalk I/O Port

Programmable Timer/Counter

The general purpose timer/counter can be programmed to function as a timer or as a counter. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will start the counter if the Enable bit is active. As a timer on terminal count, it will cause an interrupt, reload with the value stored in the Timer/Counter Value register and continue to count.

The Timer/Counter counting is enabled or disabled by the enable bit. The value *n* should be written to the Counter in order to count to *n* clocks. At reset, the counter is disabled.

I/O Bus

The R3715 supports two 8-bit (IOCS[1:0]*) and two 16-bit (IOGPµCS[1:0]*) external I/O channels that share the IODATA[15:0] pins. The two 8-bit I/O channels and the first 16-bit I/O channel (IOGPCS[0]*) each has a 16 Mbyte address space. The second 16 bit I/O channel (IOGPCS[1]*) has a 256 Mbyte address space.

Timing of the control signals to an I/O channel is programmable. The user can specify the length of IORD* and IOWR* signals. The IOCS[1:0]*, IOGPCS[1:0]* or DMAACK[1:0]* are asserted one cycle before the IORD* or IOWR* signals become active, and remain active for one cycle after IORD* or IOWR* are dasserted. RDCEN* and ACK* will be asserted by the R3715 to end a processor (or EDTACK* to end an external DMA master) I/O cycle.

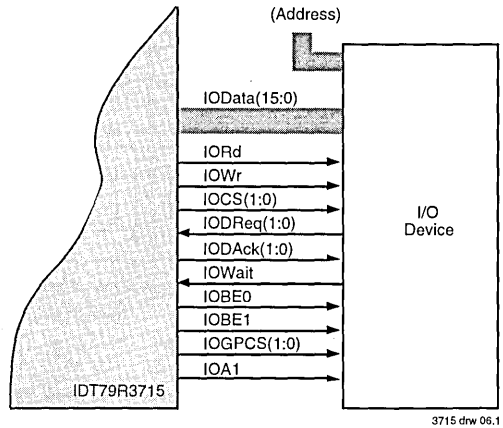

Figure 2.5 General Purpose I/O Device Interface

8-bit I/O Channels

The R3715 supports processor byte accesses (reads and writes) to devices located on the two 8 bit I/O channels. These accesses can be made using any of the four bytes on the 32 bit data bus. The R3715 will transfer the correct byte (according to the 4 Byte Enables) to the 8 bit I/O bus (IODATA[7:0]).

The I/O channel unit on the R3715 operates as a DMA controller with the two 8 bit I/O channels. DMA operations between I/O devices and the DRAM are supported. Eight bit data is packed or unpacked during DMA access into a 32 bit register for I/O DMA read or write respectively.

DMA Operations

Processor requests have priority over DMA requests. The priority for DMA operations is round robin for the Centronics and the two external 8-bit DMA engines. DMAREQ[1:0]* can be masked by writing '0' to the enable bit of the channel. A channel will not participate in the arbitration if the channel is disabled or if the I/O BIU (Bus Interface Unit) is owned by another channel.

The I/O BIU is emptied into memory in a DMA read access under the following conditions: 1) if the I/O BIU is full, or 2) if there is no DMA request (DMAREQ[1:0]) from the channel which owns the I/O BIU for a time out period, or 3) the byte count reaches zero.

In the write direction if the DMAREQ* from the channel that owns the I/O BIU is not active for a time out period, and the I/O BIU is not empty, arbitration will resume on the I/O bus. The time out period is set to 32 clocks. The clock period value cannot be changed, only enabled or disabled.

16-bit I/O Channels

The R3715 supports processor and external DMA master accesses (reads and writes) to devices located on the two 16-bit I/O channels.

For 16-bit devices, the CPU can read or write to any byte or half word. Processor or external DMA master access to the 16-bit I/O channels with any combination of byte enables active, will be performed in two consecutive I/O cycles in case of 3 or 4 byte accesses. In the two cycles, data will be packed or unpacked from a 32-bit register for an I/O read or write respectively. Conversion between big and little endian is supported for 16-bit devices.

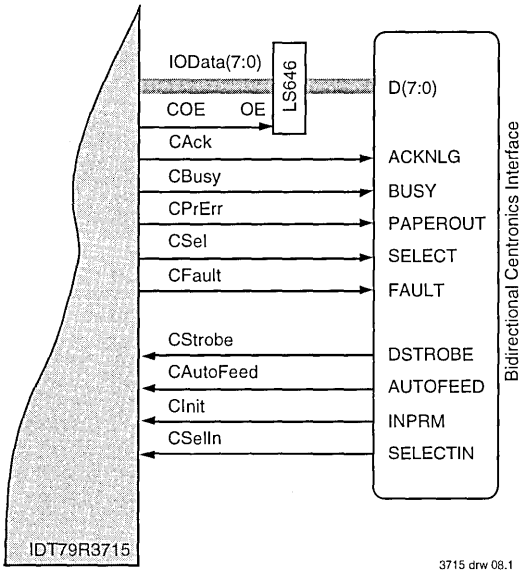

Figure 2.6 IEEE P1284 Bidirectional Centronics I/O Port

Centronics IEEE 1284 Communication

IDT's Centronics implementation meets the IEEE 1284 definition of a compliant device. It supports the following modes: Compatible, Nibble, Byte, ECP and EPP, as well as the negotiation necessary for transition between different modes. Support for the Compatible mode includes the following three variations: Standard, IBM Epson, and Classic.

Note: IDT urges designers to review the IEEE1284 Rev. 2 specification for a complete discussion of this Centronics standard.

There are two ways to handle the Centronics protocol. In the first option, data is transferred in DMA fashion and is only applicable in the Compatible, ECP, and EPP modes. The second option is interrupt driven, and applies to all modes. That is, Byte and Nibble modes are only interrupt driven.

There is support for special character detection in the Centronics incoming data. Control data characters like ^C or ^T can be detected and the CPU will be interrupted.

Figure 2.6 shows the configuration of the IEEE P1284 bidirectional centronics I/O port.

Negotiation

The R3715 defaults after reset to Compatible mode. The negotiation phase starts when the host sets CSELECTIN* HIGH and CAUTOFD* LOW. The R3715 interrupts the CPU by asserting the CentWrInt interrupt. The CPU interrupt routine includes reading the extensibility request value from the Centronics External register, and writing to the Centronics Control register to specify the supported mode. Note that the interpretation of the CenRdInt and CentWrInt interrupts, and the interrupt handler response, will be different in each mode.

Table 2.1 summarizes the values of host requests and the CPU interrupt routine response.

Request mode	Request value	Interrupt response: Mode-supported value	Interrupt response: Mode-not-supported value
Extensibility link first byte	1000 0000 xxxx xxxx	1110 1xxx	0111 0110
EPP	0100 0000	1100	0111
ECP with RLE	0011 0000	1011	0111
ECP	0001 0000	1011	0111
Device ID: -Nibble -Byte -ECP with RLE -ECP without RLE	 0000 0100 0000 0101 0001 0100 0011 0100	 1001 1010 1011 1011	 0111 0111 0111 0111
Byte	0000 0001	1010	0111
Nibble	0000 0000	0001	1111

Table 2.1 Interrupt Responses During Negotiation Phase

Compatible Mode

The CPU needs to configure the Compatible mode to one of the three supported modes: IBM, Classic or Standard, and to a data transfer option (DMA or interrupt per byte). Setting the modes and options is done by writing to the mode register (values are specified in the Centronics Mode register table).

In the interrupt per byte mode, the CPU will read data

responds to the CentRdInt interrupt. In DMA mode the CPU will initialize the DMA registers (addresses 1d0000a0, 1d000080 & 1d00098) before starting the DMA operation. The R3715 will assert interrupt CentDMAInt when the DMA counter will reach terminal count.

A host request to return to Compatible mode from any of the other modes is indicated to the CPU by the assertion of the CentRstInt interrupt.

Nibble Mode

The R3715 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to the Nibble data register. The R3715 sends the byte to the host over the control lines in two consecutive nibble transactions.

Byte Mode

The R3715 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to Centronics External register.

Extensibility Link

Assertion of CentWrInt interrupt while in Compatible. mode indicates to the CPU an extensibility request. The CPU will read from the Centronics External register the extensibility request value, and write to the control register the next mode and proper response.

ECP Mode

DMA and interrupt per byte options are supported for the ECP mode.

In the interrupt per byte option, the R3715 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt.

In reverse transfer, in response to CentWrInt*, the CPU must first write to the Centronics status register (to the Busy bit). This indicates whether the CPU sends a command or data byte, and then write the data to the Centronics External register.

In forward transfer, in response to CentRdInt the CPU needs to read from the Centronics host register (Autofeed bit) to know whether the host is sending data or command, and then read the data from the Centronics register.

Note: RLE compression is supported only in interrupt per byte mode.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA. CentWrInt* will be asserted when the host requests data and the DmaDir bit in the Mode register indicates a read direction (From the IEEE1284 port to memory). CentRdInt will be asserted when the host sends data and the DmaDir bit indicates a write direction or when the host sends a command byte.

EPP Mode

DMA and interrupt per byte options are supported for the EPP mode, as follows:

In the interrupt per byte option, the R3715 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt. It will distinguish between data and address by the contents of the strobe Selectin and AutoFd bits in the host buffer.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA.

CentWrInt will be asserted: 1) when the host requests data, and the DmaDir bit in the Mode register indicates a read direction (from the Centronics port to memory), or 2) when the host asks for an address byte.

CentRdInt will be asserted: 1) when the host sends data and the DmaDir bit indicates a write direction, or 2) when the host sends an address byte.

CPU Control

This mode enables the CPU to set the values of the Centronics status register, and communicate with the host in compatible mode.

Character Detection.

The value of the three CentDetect 8-bit registers is constantly compared to the Centronics incoming data. When a match occurs the CPU is interrupted. Characters as ^C or ^T can be detected during Centronics DMA operations and the CPU can respond without the need to wait to the end of the DMA operation.

Programmable Timing

To allow for higher than specified (by the IEEE1284 standard) data rates, the minimum delay can be programmed to values lower than the minimum required by this standard.

PIN INFORMATION

Logic Symbols

Signals marked with an asterisk are active when low. Dashed arrows in figure 1.2 indicate MUX'ed signals.

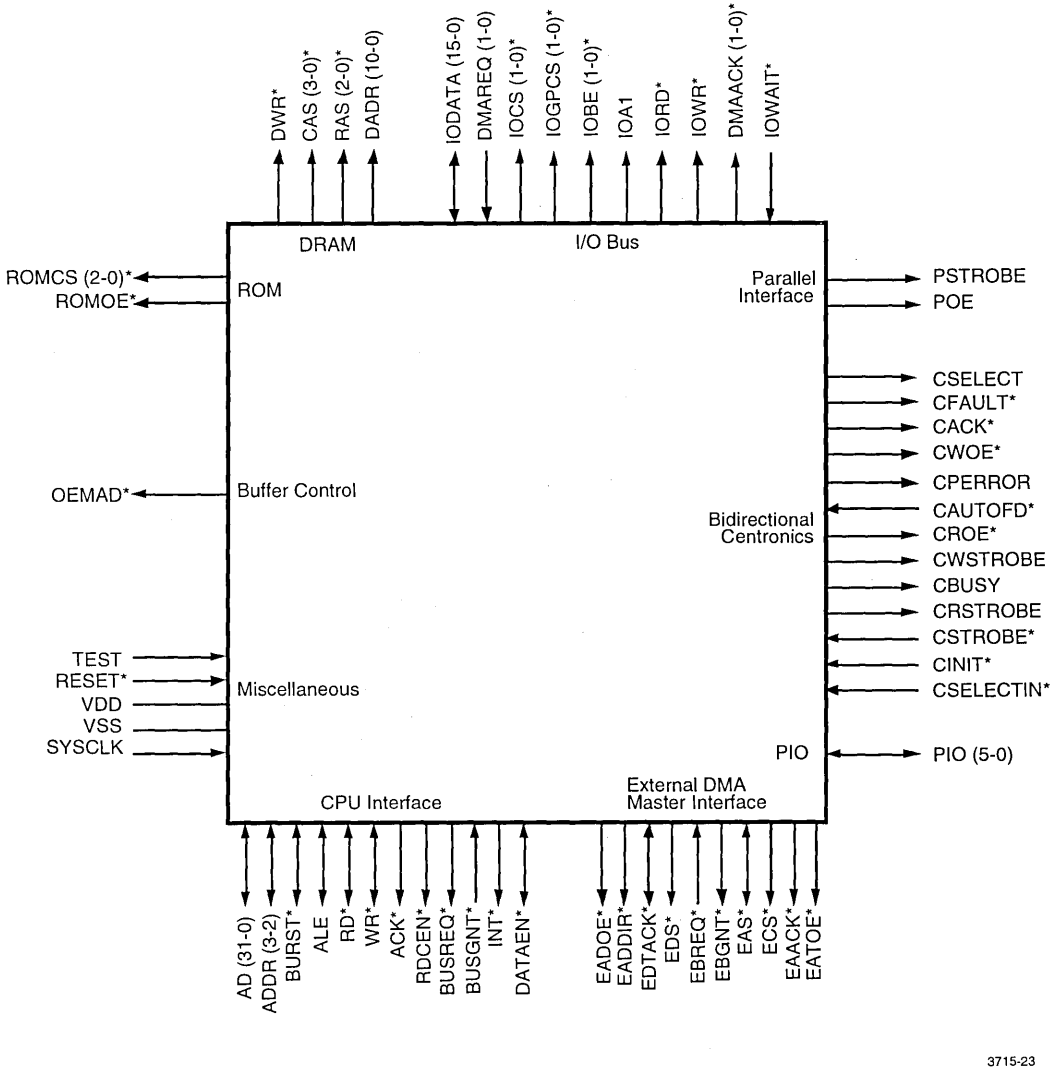

Figure 1.1 Logic Symbol for R3715

Pin Assignment Table

Pin names with a trailing asterisk (*) identify pins that are active when low.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
CPU Interface				
A/D[31:0]	P.U.	I/O	8mA	**Address/Data:** Multiplexed address and data bus. In the Address phase: A/D[31:4] are address, A/D[3:0] are Byte Enable[3:0]. During external DMA Master cycles, A/D[3:2] contain address bits 3 and 2, and not Byte Enables. In the Data phase: Data[31:0]
ADDR[3:2]	P.U.	I/O	4mA	**Non Multiplexed Address:** Connected to the CPU ADDR[3:2]. In DMA cycles the R3715 drives these lines.
BURST*	P.U.	I/O	2mA	**Burst Transfer:** Used only during read cycles, the BURST* signal indicates that the current bus read is requesting a block of four contiguous words from memory. The pin connects to the CPU's BURSTWRNEAR* signal. In DMA cycles the R3715 drives this signal HIGH.
ALE	P.D.	I/O	4mA	**Address Latch Enable:** Used by the CPU to indicate that the A/D bus contains valid address information for the bus transaction. During external DMA master cycles, the R3715 asserts ALE to capture the address supplied by the external DMA master.
SYSCLK		I		**System Clock:** Connected directly to the CPU SYSCLK* output.
RD*	P.U.	I/O	2mA	**Read:** Indicates a read access by the CPU. In DMA cycles the R3715 drives the signal HIGH.
WR*	P.U.	I/O	2mA	**Write:** Indicates a write access by the CPU or the external DMA master. In a non-external DMA master cycle the R3715 drives this signal HIGH. Its negation indicates a read access by the external DMA master (during external DMA master).
ACK*		O	2mA	**Acknowledge:** Indicates to the CPU that the memory system has sufficiently processed the bus transaction i.e. that the CPU may either terminate a write cycle or process read data.
RDCEN*		O	2mA	**Read Buffer Clock Enable:** Indicates to the CPU that there is valid data on the A/D bus. Used during read cycles only.
BUSREQ*		O	2mA	**Bus Request:** The R3715 requests the CPU bus which is required for I/O and External DMA's.
BUSGNT*		I		**Bus Grant:** Indicates that the CPU has relinquished the bus.
INT*		O	2mA	**Interrupt:** "OR's" the internal and external interrupt sources.
DATAEN*		I/O	4mA	**Data Enable:** indicates the data phase in CPU read cycles. In DMA the R3715 asserts DATAEN* when the ROM/DRAM drives data onto A/D[31:0].
ROM				
ROMCS*[2:0]		O	4mA	**ROM Chip Select:** Select one of the 3 ROM banks. They can be connected to the ROM's Chip Select or Output Enable. ROMCS[2]* is connected to the boot ROM, with starting physical address 0x1fc00000.
ROMOE*		O	4mA	**ROM Output Enable:** Asserted when there is an access to any of the ROM banks. Used to output- enable the ROM data in systems where there is a buffer between ROM and DRAM data bus; eg. when using an interleaved ROM configuration.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
DRAM				
DADR[10:0]		O	8ma	**DRAM Address:** Multiplexed row and column address connected to the DRAM address.
RAS[2:0]*		O	4mA	**Row Adress Select:** Directly connected, on a bank basis, with the RAS* inputs of the DRAMs. Supports up to three banks of DRAMs.
CAS[3:0]*		O	4mA	**Column Address Select:** Directly connected, on a byte basis (can be across banks), to the CAS* inputs of the DRAMs. Connects a CAS* to each of the four bytes in every bank.
DWR*		O	12mA	**DRAM Write:** Connects to the write pin of each of the DRAMs.
External DMA Master Interface				
EBREQ*	P.U.	I		**External DMA Master Bus Request:** An external DMA master bus request to make a system resource access in master mode.
EBGNT*		O	2mA	**External DMA Master Bus Grant:** The R3715 asserts EBGNT* to grant the CPU bus to the external DMA master. Once the EBGNT* is asserted, it remains so until EBREQ* is deasserted.
EAS*	P.U.	I/O	2mA	**External DMA Master Address Strobe:** Master Mode (input) - the coprocessor indicates that it is driving valid data on the A/D bus. Slave mode (output) - the R3715 indicates that it is driving valid data on the A/D bus
EDS*		O	2mA	**External DMA Master Data Strobe:** Master mode (input) - during Write indicates that there is valid data on the A/D bus. During Read indicates data phase. Slave mode (output) - the R3715 drives EDS* to indicate that it is ready to accept data during reads or that valid data is available during write on the A/D bus.
EDTACK*	P.U.	I/O	2mA	**External DMA Master Data Acknowledge:** Master mode (output) - The R3715 asserts EDTACK* to indicate that the system is receiving or driving the requested data to/from the A/D bus. Slave mode (input) - The external DMA master asserts EDTACK* to signal that it has supplied or received data on its bus.
EAACK*		O	2mA	**External DMA Master Address Acknowledge:** The R3715 asserts EAACK* in the same clock that it asserts ALE for the external DMA master. This insures that the external DMA master continues driving the address until latched by the system.
ECS*		O	2mA	**External DMA Master Chip Select:** When the CPU accesses the external DMA master, the R3715 asserts ECS*. It is active one clock before R3715 asserts EAS*.
EADOE*		O	4mA	**External DMA Master A/D Output Enable:** The R3715 asserts EADOE* when the external DMA master drives the address to the A/D bus, and in the data phases of the external DMA master.
EADDIR*		O	4mA	**External DMA Master A/D Direction:** The R3715 asserts EADDIR* (LOW) when the external DMA master drives the A/D bus.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
EATOE*		O	4mA	**External DMA Master Address To Output Enable:** The R3715 asserts EATOE* in the address phase of cycles in which the CPU accesses the external DMA master.
Buffer Control				
OEMAD*		O	4mA	**Output Enable between Memory and A/D:** Output enable for the data path transceiver between the memory system (ROM and DRAM) and the A/D bus.
I/O Bus				
IODATA[15:0]	P.U.	I/O	8mA	**Input/Output Device Data:** Bidirectional 16-bit I/O Data bus.
IORD*		O	12mA	**Input/Output Device Read:** Active during Read from an I/O device.
IOWR*		O	12mA	**Input/Output Device Write:** Active during Write to an I/O device.
IOCS[1:0]*		O	2mA	**Input/Output Device Chip Select:** Chip selects for 8 bit I/O channels 0 and 1.
IOGPCS[1:0]*		O	2mA	**Input/ Output Device Chip Select:** Chip selects for 16 bit I/O channels 0 and 1.
DMAREQ[1:0]*	P.D.	I		**DMA Request:** Requesting DMA service on 8-bit channels 0 and 1.
DMAACK[1:0]*		O	2mA	**DMA Acknowledge:** Indicating that DMA access is granted on 8-bit channels 0 and 1.
IOA1		O	8mA	**Input/Output Device Address bit 1:** Provides a half word (16 bit) address on the I/O bus.
IOBE[1:0]*		O	2mA	**Input/Output Device Byte Enable:** Indicates which byte data bus is valid on the 16 bit I/O bus. IOBE[1]* corresponds to IODATA[15:8] and IOBE[0] corresponds to IODATA[7:0].
IOWAIT*	P.U.	I		**Input/Output Device Wait:** Indicates to the R3715 that a transfer cycle on the I/O bus needs to be extended.
PIO[5:0]	P.U.	I/O	8mA	**Programmable Input/Output:** Individually programmed pins for inputs, interrupt inputs or outputs.
Bidirectional Centronics				
CWOE*		O	2mA	**Centronics Write Output Enable:** Controls the Output Enable signal of the data register from the printer to the host.
CROE*		O	2mA	**Centronics Read Output Enable:** Controls the OE* of the Centronics external register in the direction from the host to the printer (the IODATA[7:0] bus).
CWSTROBE		O	2mA	**Centronics Write Strobe:** Clocks data from IODATA[7:0] into the Centronics register (from printer to host).
CRSTROBE		O	2mA	**Centronics Read Strobe:** Clocks data from the host into the Centronics register (from host to printer).

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CSTROBE*	P.U.	I		**Centronics Strobe:** Host driven. Compatibility mode: Set active low to transfer data into peripheral device's input latch. Data is valid while signal is low. Negotiation phase: Set active low to transfer extensibility request value into peripheral device's input latch. Data is valid on the leading (falling) edge of HostClk (CSTROBE*). Reverse data transfer phase: Set high during Nibble Mode transfers to avoid latching data into peripheral device. Pulsed low during Byte Mode transfers to acknowledge transfer of data from the peripheral. The peripheral device shall ensure that this pulse does not transfer a new data byte into the peripheral's input latch. ECP mode: Used in a closed-loop handshake with PeriphAck (CBUSY) to transfer data or address information from the host to the peripheral device. EPP mode: Set low to denote an address or data write operation to the peripheral device. Set high to denote an address or data read operation from the peripheral device. For a more detailed description refer to section 4.1 of the IEEE P1284 D2.00 specification.
CACK*		O	2mA	**Centronics acknowledge:** Peripheral device driven. Compatibility mode: Pulsed low by the peripheral device to acknowledge transfer of a data byte from the host. Negotiation phase: Set low to acknowledge 1284 support, then set high to indicate that the Xflag (CSELECT) and data available flags may be read. Reverse data transfer phase: Used in both Nibble and Byte Modes to qualify data being sent to the host. Reverse idle phase: Set low then high by peripheral device to cause an interrupt indicating to host that data is available. ECP mode: Used in a closed-loop handshake with HostAck (CAUTOFD*) to transfer data from the peripheral device to the host. EPP mode: Used by the peripheral device to interrupt the host. This signal is active high and positive edge triggered. For a more detailed description refer to section 4.3 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CBUSY		O	2mA	**Centronics Busy:** Peripheral device driven. Compatibility mode: Driven high to indicate the peripheral device is not ready to receive data. Negotiation phase: Reflects the present state of the peripheral device's forward channel. Reverse data transfer phase: Nibble mode: Data bits 3 then 7, then forward channel busy status. Byte mode: Forward channel busy status. Reverse idle phase: Forward channel busy status. ECP mode: Used by peripheral for flow control in the forward direction. PeriphAck (CBUSY) also provides a ninth data bit used to determine whether command or data information is present on the data signals in the reverse direction. EPP mode: Driven inactive as a positive acknowledgment from the peripheral device that transfer of data or address os completed. Signal is active when low, and should be driven active as an indication that the device is ready for the next address or data transfer. For a more detailed description refer to section 4.4 of the IEEE P1284 D2.00 specification.
CPERROR		O	2mA	**Centronics Printer Error:** Peripheral device driven. Compatibility mode: Driven high to indicate that the peripheral device has encountered an error in its paper path. Note that this signal's meaning varies among peripheral devices. Peripherals shall set nFault (CFAULT*) low whenever they set Perror (CPERROR) high. Negotiation phase: Set high to indicate 1284 support, then follows nDataAvail (CFAULT*). Reverse data transfer phase: Nibble mode: Data bits 2 then 6. Byte mode: Same as nDataAvail (CFAULT*). ECP mode: The peripheral drives this signal low to acknowledge nReverseRequest (CINIT*). The host relies upon nAckReverse (CPERROR) to determine when it is permitted to drive the data signals. EPP mode (User Defined 1): A manufacturer-specific signal. For a more detailed description refer to section 4.5 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CSELECT		O	2mA	**Centronics Select:** Peripheral device driven. Compatibility mode: Set high to indicate that the peripheral device is online. Negotiation phase: Used by peripheral device to reply to the requested extensibility byte sent by the host during the negotiation phase. Affirmative response is indicated with the signal high for all request values except for Nibble Mode Reverse Channel Transfer, which is indicated affirmative with the signal low. Reverse data transfer phase: Nibble mode: Data bits 1 then 5. Byte mode: Same as negotiation phase. Reverse idle phase: Same as negotiation phase. ECP mode: Same as negotiation phase. EPP mode (User Defined 3): A manufacturer-specific signal. For a more detailed description of this signal refer to section 4.6 of the IEEE P1284 D2.00 specification. For more details about the negotiation phase refer to section 6.4 of the same specification.
CAUTOFD*	P.U.	I		**Centronics Autofeed:** Host driven. Compatibility mode: Interpretation varies among peripheral devices. Set low by host to put some printers into auto line feed mode. Also may be used as a 9th data, parity, or command/data control bit. Negotiation phase: Set low in conjunction with 1284 Active (CSELECTIN*) being set high to request a 1284 mode, then set high after peripheral device sets PtrClk (CACK*) low. Reverse data transfer phase: Nibble mode: Set low to indicate host can receive peripheral device to host data, then set high to acknowledge receipt of that nibble. Byte mode: Same as Nibble mode to request and acknowledge bytes. Following a reverse channel transfer, the interface transitions to idle phase when HostBusy (CAUTOFD*) is set low and peripheral device has no data available. Reverse idle phase: Set high in response to PtrClk (CACK*) low pulse to re-enter reverse data transfer phase. If set high with 1284 Active (CSELECTIN*) being set low, the 1284 idle phase is aborted and the interface returns to Compatibility mode. ECP mode: The host drives this signal for flow control in the reverse direction. It is used in an interlocked handshake with PeriphClk (CACK*). HostAck (CAUTOFD*) also provides a 9th data bit used to determine whether command or data information is present on the data signals in the forward direction. EPP mode: Used to denote a data cycle, and is active when low. For a more detailed description refer to section 4.7 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CINIT*	P.U.	I		**Centronics Initialize:** Host driven. Compatibility mode: Pulsed low in conjunction with 1284 Active (CSELECTIN*) low to reset the interface and force a return to Compatibility mode idle phase. Negotiation phase: Set high. Reverse data transfer phase: Set high. ECP mode: Driven low to place the channel in the reverse direction. While in this mode the peripheral is allowed to drive only the bidirectional data signals when nReverseRequest (CINIT*) is low and 1284 Active (CSELECTIN*) is high. EPP mode: When driven active (low), initiates a termination cycle that returns the interface to Compatibility mode. For a more detailed description refer to section 4.9 of the IEEE P1284 D2.00 specification.
CFAULT*		O	2mA	**Centronics Fault:** Peripheral device driven. Compatibility mode: Set low by peripheral device to indicate that an error has occurred. The meaning of this signal varies among peripheral devices. Negotiation phase: Set high to acknowledge 1284 compatibility. In Nibble or Byte mode it is then set low to indicate peripheral device to host data is available following host setting HostBusy (CAUTOFD*) high. Reverse data transfer phase: Nibble mode: Set low to indicate that peripheral device has data ready to send to host, then used to send data bits 0, then 4. Byte mode: Used to indicate that data is available. ECP mode: In this mode the peripheral may drive this pin low to request communication with the host. The request is only a suggestion to the host, who has ultimate control over the transfer direction. Typically used to generate an interrupt to the host, also provides a mechanism for peer-to-peer communication. Signal is valid in both forward and reverse directions. EPP mode (User Defined 2): Manufacturer-specific signal. For a more detailed description refer to section 4.10 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CSELECTIN*	P.U.	I		**Centronics Select Input:** Host driven. Compatibility mode: Set low by host to select peripheral device. Negotiation phase: Set high in conjunction with HostBusy (CAUTOFD*) being set low to request a 1284 mode. Reverse data transfer phase: Set high to indicate that bus direction is peripheral device to host. Set low to terminate 1784 mode and set bus direction host to peripheral device. Reverse idle phase: Same as Reverse data transfer phase. ECP mode: Driven high by the host while in ECP mode. Set low by the host to terminate ECP mode and return the link to the Compatibility mode. EPP mode: Used to denote an address cycle, and is active low. For a more detailed description refer to section 4.11 of the IEEE P1284 D2.00 specification.
Parallel Port Control				
PSTROBE*		O		**Parallel Strobe:** Clocks 8-bit or 16-bit parallel data from IODATA[15:0].
POE*		O		**Parallel Output Enable:** When active (LOW) it controls the output enable of a data buffer for 8-bit or 16-bit wide parallel data into IODATA[15:0].
Misc.				
TEST	P.D.	I		**Master Output Enable:** When TEST is HIGH and RESET* is active, ALL the device outputs and I/Os are tri-stated (in a system, TEST should be pulled down to GND).
RESET*		I		**Reset:** Will reset the R3715 to the initial state.
VDD				**+5V** (+/-5%)
VSS				**Ground**

NOTE:
[1] Pull Up/Pull Dn identifies pins with internal Pull Up (P.U.) or Pull Down (P.D.) resistors. P.U./P.D. values are 35K-150Kohm depending on the process variation.

AC TIMING CHARACTERISTICS

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Signal(s)	Description	Min	Max	Unit
t1	SYSCLK	Pulse Width High	12		ns
t2	SYSCLK	Pulse Width Low	12		ns
t3	SYSCLK	Clock period	30		ns
t4	RESET*	Pulse Width from VDD Valid	200		us
t5	Reserved				
t6	BUSREQ*, ACK*, RDCEN*	Valid from SYSCLK rising	2	17	ns
t7	A/D[31:0], OEMAD*, EADOE*	Valid from SYSCLK falling	2	15	ns
t8	A/D[31:0], ADDR[3:2], WR*, PIO[5:0], EAS*, EDS*, EDTACK*	Driven from SYSCLK rising	0	20	ns
t9	A/D[31:0]	Tri-state from SYSCLK rising	0	15	ns
t10	A/D[31:0]	Set-up to SYSCLK falling	6		ns
t11	A/D[31:0]	Set-up to ALE falling	7		ns
t12	ALE	Set-up to SYSCLK falling	7		ns
t13	BURST*, RD*, DATAEN*, WR*, ADDR[3:2], BUSGNT*	Set-up to SYSCLK rising	10		ns
t14	ALE, BURST*, RD*, DATAEN*, INT*, PIO[5:0], IODATA[15:0], EAS*, EDS*, EDTACK*	Tri-state from SYSCLK rising	0	20	ns
t15	ALE, BURST*, RD*, DATAEN*, PIO[5:0]	Driven from SYSCLK rising	0	20	ns
t16	ALE, BURST*, RD*, DATAEN*, IOGPCS*, ROMCS*[2:0], IORD*, IOWR*, ROMOE*, IOA1, IOBE*[1:0], INT*, DMAACK*[1:0], PIO[5:0], ADDR[3:2], WR*, EAS*, EDS*, EDTACK*, ECS*, EBGNT*, EAACK*	Valid from SYSCLK rising	3	15	ns
t17	ADDR[3:2], WR*	Tri-state from SYSCLK rising	2	20	ns
t18	DADR[10:0]	Valid from AD address valid	6	25	ns
t19	DADR[10:0]	Valid from SYSCLK rising	3	27	ns
t20	RAS*[2:0], DWR*	Valid from SYSCLK rising	2	17	ns
t21	CAS*[3:0]	SYSCLK rising to CAS* LOW	2	13	ns
t22	CAS*[3:0]	SYSCLK falling to CAS* HIGH	2	13	ns
t23	IODATA[15:0]	Hold from IOWR* rising	15		ns
t24	IODATA[15:0]	Set-up to SYSCLK rising	9		ns
t25	IODATA[15:0]	Driven from SYSCLK rising	0	15	ns
t26	IOWAIT*	Set-up to SYSCLK rising	18		ns
t27	DMAREQ*[1:0], PIO[5:0]	Asynchronous Inputs		Asynch	
t28	Reserved				
t29	Reserved				
t30	Reserved				
t31	TEST, EBREQ*	Setup to SYSCLK rising	8		ns
t32	EAS*, EDS*, EDTACK*	Setup to SYSCLK rising	13		ns
t33	EADDIR*, EATOE*	Valid from SYSCLK rising	2	20	ns

Note:
[1] Internal VCLK frequency (divided or not) should be lower than 85% of SYSCLK frequency. Valid only in the SYSCLK during which IODATA is sampled.

DC ELECTRICAL SPECIFICATIONS

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		200	mA	VDD = 5V, Ta=25C
CINCLK	CLK Input Capacitance		11	pF	
CIN	Input Capacitance		5	pF	

REGISTER MAP AND TABLES—R3715

For the register map and tables in this section, please note:

- Reads and Writes to and from the R3715 internal registers should be word (32-bit) accesses.
- The 0x notations indicate hexadecimal values, as in notations for the C language.
- Bit 0 is the least significant bit.

6

REGISTER MAP

Description	Physical Address	Description	Physical Address
ROM Configuration	0x1d000000	DMA Count 0	0x1d000090
PIO Value	0x1d000040	DMA Count 1	0x1d000094
PIO Control	0x1d000044	DMA Centronics Count	0x1d000098
PIO Read Pins	0x1d00005c	I/O Channel Timing	0x1d0000a0
Timer/Counter Value	0x1d000048	Centronics Status	0x1d000100
Timer/Counter Control	0x1d00004c	Centronics Control	0x1d000104
Interrupt Cause	0x1d000050	Centronics Nibble Data	0x1d000108
Interrupt Mask	0x1d000054	Centronics Host	0x1d00010c
Interrupt Write	0x1d000060	Centronics Mode	0x1d000110
Test	0x1d000064	Centronics Minimum Delay	0x1d000114
DRAM Control	0x1d000058	Centronics Data Detect 0	0x1d0000a4
DMA Address 0	0x1d000080	Centronics Data Detect 1	0x1d0000a8
DMA Address 1	0x1d000084	Centronics Data Detect 2	0x1d0000ac
DMA Centronics Address	0x1d000088		

REGISTER TABLES

The remainder of this section contains register tables for the R3715.

ROM Configuration

This register is used to set the ROM address space for the two configurable ROM banks (ROMCS[1:0]*) and to set the number of wait state cycles inserted between data phases.[1]

Address: 1d000000

Bits	Field name	Function	Initial Value
0-3	First	The gap (number of cycles) from ROMCS* active to the first RDCEN*. 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
4-7	Gap1	The gap between the first RDCEN* and the second RDCEN* 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
8-11	Gap2	The gap between the second RDCEN* and the third RDCEN*. 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
12-15	Gap3	The gap between the third RDCEN* and the fourth RDCEN* 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
16-21	AckTime	The gap from ROMCS* active to AckTime in block read 000000 - one cycle 000001 - two cycles n cycles (1 to 64 cycles range)	0x3f
22-23	SpaceSize	ROMCS[1:0]* address space size (ROMCS[2] has a fixed 4 Mbyte address space) 00 - 8 Mbyte 01 - 4 Mbyte 10 - 2 Mbyte 11 - 1 Mbyte	0x3

NOTE:

[1]It is the user's responsibility to set AckTime timing correctly.

PIO Value

This register is used to set the value for those PIO pins configured by the PIO Control register as outputs.

Address: 1d000040

Bits	Field name	Function	Initial Value
0-5	PIO Value	Value of the PIO pins configured as outputs	0x0

PIO Control

This register sets the direction of the PIO pins.

Address: 1d000044

Bits	Field name	Function	Initial Value
0-5	PIO Control	Sets the direction of the corresponding PIO pin: 0 - Output 1 - Input	0x3f
6	Reserved	Must be 0	0

PIO Read Pins

This address is used to read inputs from the PIO pins.

Address: 1d00005C

Bits	Field name	Function	Initial Value
0-5	PIO Input Value	Value on the PIO pins	

Timer/Counter Value

This register is used to set the number of clocks to be counted by the Timer/Counter.

Address: 1d000048

Bits	Field name	Function	Initial Value
0-23	T/C Value	Number of clocks to count. Set to n to count to n.	0x000000

Timer/Counter Control

This register is used to enable and disable the Timer/Counter and to select the specific mode of use.

Address: 1d00004c

Bits	Field name	Function	Initial Value
0	Enable	Timer/Counter count enable 0 - Disable 1 - Enable	0x0
1	Select	Select mode of operation 0 - Counter 1 - Timer	0x0

Interrupt Cause

This register is used to identify the source behind an interrupt; it can also be used for polling of a specific interrupt or set of interrupts. A value of 1 indicates assertion of the interrupt. This register is also used to clear internal interrupts, writing a 0 will reset the corresponding internal interrupt. Writing a 1 will have no effect on the interrupt. External interrupts should be cleared via an external mechanism.

Address: 1d000050

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Mask

This interrupt is used to mask (disable) specific interrupt sources, both internal and external (PIO). All the interrupts are maskable. A value of 0 masks the corresponding interrupt.

Address: 1d000054

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CenRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Write

This register is used to write to the Interrupt Cause register. This register should be used for interrupt testing only.

Address: 1d000060

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	

Test

No reading or writing from/to this address. Doing so may result in improper generation of this device.

Address: 1d000064

DRAM Control

This register is used to set the desired DRAM device depth, access time (both for the CPU and external DMA master) and refresh frequency.

Address: 1d000058

Bits	Field name	Function	Initial Value
0-2	DevDepth Bank 1-2	Depth of the DRAM device used, in words. 000 - 256K 001 - 512K 010 - 1M 011 - 2M 100 - 4M	0x0
3-4	DevDepth Bank 0	Depth of the DRAM device used, in words. 00 - 256K 01 - 512K 10 - 1M 11 - 2M	0x0
5	ExtCas	CAS duration for both CPU and external DMA master accesses. 0 - CAS is active for one and a half cycles 1 - CAS is active for two and a half cycles	0x0
6	ExtCas	CAS duration for external DMA master accesses only. 0 - CAS is active in external DMA master accesses for one and a half cycles 1 - CAS is active in external DMA master accesses for two and a half cycles	0x0
7-8	RefFreq	SYSCLK frequency. 00 - 15.6 uS refresh time at 16MHz 01 - 15.6 uS refresh time at 20MHz 10 - 15.6 uS refresh time at 25MHz 11 - 15.6 uS refresh time at 33MHz	0x0

DMA Address 0

This register is used to set the first DRAM address used in channel 0 DMA operations.

Address: 1d000080

Bits	Field name	Function	Initial Value
0-25	DmaAddr0	First address for DMA channel 0.	0x0

DMA Address 1

This register is used to set the first DRAM address used in channel 1 DMA operations.

Address: 1d000084

Bits	Field name	Function	Initial Value
0-25	DmaAddr1	First address for DMA channel 1.	0x0

DMA Centronics Address

This register is used to set the first DRAM address used in Centronics DMA operation.

Address: 1d000088

Bits	Field name	Function	Initial Value
0-25	DmaAddrCent	First address for Centronics DMA.	0x0

DMA Count 0

This register is used to set the number of bytes to be transferred in a channel 0 DMA operation.

Address: 1d000090

Bits	Field name	Function	Initial Value
0-15	DmaCnt0	DMA count channel 0. Load with n-1 to transfer n.	0x0

DMA Count 1

This register is used to set the number of bytes to be transferred in a channel 1 DMA operation.

Address: 1d000094

Bits	Field name	Function	Initial Value
0-15	DmaCnt1	DMA count channel 1. Load with n-1 to transfer n.	0x0

DMA Centronics Count

This register is used to set the number of bytes to be transferred in a Centronics DMA operation.

Address: 1d000098

Bits	Field name	Function	Initial Value
0-15	DmaCntCen	Centronics DMA count. Load with n-1 to transfer n.	0x0

I/O Channel Timing

This register is used to configure the I/O bus parameters, including signal timing; DMA enabling, time-out, and direction; and the endianess of the 16-bit I/O channels. The DevTime fields specify the number of cycles IORD* or IOWR* are asserted in an I/O or DMA access. The Time Out Enable (TOEn) field chooses between inserting 32 clock cycles between arbitration cycles or not; normally, enabling this bit results in better system performance.

Address: 1d00000a0

Bits	Field name	Function	Initial Value
0-3	DevTime0	8-bit I/O channel 0 (IOCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
4	DmaEn0	DMA enable 8-bit channel 0. 0 - DMA disable 1 - DMA enable	0x0
5	DmaR/W0	DMA Read or Write 8-bit channel 0. 0 - DMA write 1 - DMA read	0x0
6-9	DevTime1	8-bit channel 1 (IOCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
10	DmaEn1	DMA enable 8-bit channel 1. 0 - DMA disable 1 - DMA enable	0x0
11	DmaR/W1	DMA Read or Write 8-bit channel 1. 0 - DMA write 1 - DMA read	0x0
12-15	CenTime	Centronics external register access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
16	DmaEnCen	Centronics DMA enable. 0 - DMA disable 1 - DMA enable	0x0
17	DmaR/WCen	DMA Read or Write for the Centronics interface. 0 - DMA write 1 - DMA read	
18-21	DevTime3	16-bit I/O channel 0 (IOGPCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
22-25	DevTime4	16-bit I/O channel 1 (IOGPCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
26	BigEndian0	Big or Little Endian for the 16-bit I/O channel 0 0 - Big Endian 1 - Little Endian	0x0
27	BigEndian1	Big or Little Endian for the 16-bit I/O channel 1 0 - Big Endian 1 - Little Endian	0x0
28	TOEn	Time Out Enable for both DMA channels 0 - Time out disabled, time out is 0 clocks 1 - Time out enabled, time out is 32 clocks	0x0

Centronics Status

This register is used to implement the Centronics hand-shake protocol via software by the CPU.

Address: 1d000100

Bits	Field name	Function	Initial Value
0	Busy	Busy indication 0 - Ready 1 - Busy	0x0
1	Ack	Acknowledge 0 - acknowledge 1 - Normal	
2	Fault	Fault indication 0 - Fault 1 - Normal	
3	Select	Select 0 - Off line 1- On line	
4	Perror	Paper Error indication 0 - No error 1- Error	

Centronics Control

This register is used to set the Centronics transfer mode per the IEEE 1284 specification Rev. 2.

Address: 1d000104

Bits	Field name	Function	Initial Value
0-2	Mode	IEEE 1284 modes 000 - Compatible 001 - Nibble 010 - Byte 011 - ECP 100 - EPP 101 - CPU control 110 - extensibility link 111 - termination	0x0
3	NegRep	Negotiation Reply All modes except nibble mode: 0 - mode requested by host is not supported by the peripheral 1- mode requested is supported Nibble mode: 0- mode requested by host is supported by the peripheral 1- mode requested is not supported	0x0

Centronics Nibble Data

This register is used to post the data to be transferred in nibble mode.

Address: 1d000108

Bits	Field name	Function	Initial Value
0-7	NibData	Nibble mode Centronics data to be sent to the host	

Centronics Host

This register is used to read inputs from the host in the Centronics protocol pins.

Address: 1d00010c

Bits	Field name	Function (In compatible mode)	Initial Value
0	Strobe	Set LOW by the host to transfer data	
1	SelectIn	Set LOW by host to select printer	
2	Init	Pulsed LOW with SelectIn active LOW to reset the Centronics interface	
3	AutoFd	Set LOW by the host to put the printer in auto-feed mode.	

Centronics Mode

This register is used to set the Centronics DMA parameters and select the protocol options in Compatible mode.

Address: 1d000110

Bits	Field name	Function	Initial Value
0-1	Application	See IEEE 1284 standard for details 00 - Standard 01 - IBM Epson 10 - Reserved 11 - Classic	
2	DmaEn	0 - transmission executed by CPU 1 - transmission executed by DMA	
3	DmaDir	0 - DMA write 1 - DMA reads	

Centronics Minimum Delay

This register contains the values that are needed for each operating frequency to comply with the IEEE 1284 standard (minimum of 500ns and 2500ns). However for systems with higher performance requirements, it is possible to program the minimum delays for lower values.

Address:1d000114

Bits	Field name	Function	Initial Value
0-6	2500ns	16MHz - 0x28	
		20MHz - 0x32	
		25MHz - 0x3f	
		33MHz - 0x53	
7-13	500ns	16MHz - 0x08	
		20MHz - 0x0a	
		25MHz - 0x0d	
		33MHz - 0x11	

Centronics Data Detect 0

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a4

Bits	Field name	Function	Initial Value
0-7	DataDet0	Data to be used for comparison with the incoming data.	

Centronics Data Detect 1

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a8

Bits	Field name	Function	Initial Value
0-7	DataDet1	Data to be used for comparison with the incoming data.	

Centronics Data Detect 2

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000ac

Bits	Field name	Function	Initial Value
0-7	DataDet2	Data to be used for comparison with the incoming data.	

EXTERNAL ADDRESS SPACE

The address space allocated to the different resources in the system is shown in Table 4.1. Bits 29-31 are not decoded so that physical aliases of 512 Mbyte are created. This enables the software to access the same system resource using different attributes (i.e cached space vs. uncached space, kernel vs. user).

Description	Size	Physical Address Range[1]
DRAM	40M	0X00000000: 0x027FFFFF
ROMCS[2]*.	4M	0x1FC00000: 0x1FFFFFFF
ROMCS[1]*	8M	0x1F400000: 0x1FBFFFFF
ROMCS[0]*	8M	0x1EC00000: 0x1F3FFFFF
IO channel 0	16M	0x08000000: 0x08FFFFFF
IO channel 1	16M	0x09000000: 0x09FFFFFF
IO channel 2	16M	0x0B000000: 0x0BFFFFFF
IO channel 3	256M	0x0C000000: 0x1BFFFFFF
Centronics external register	1M	0x0A000000: 0x0A0FFFFF
External DMA master address space	16M	0x1C000000: 0x1CFFFFFF
Internal registers	16M	0x1D000000: 0x1DFFFFFF

Table Note: [1]This column specifies maximum range.

Table 4.1 External Address Space

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IMPLEMENTATION EXAMPLES

Full Implementation

A possible implementation of a fully featured system is shown in Figure 5.1. This system includes a 2-way interleaved ROM array, and uses external multiplexers (FCT257x8) that are controlled by MUX_ADDR[2] to choose one bank or the other. The R3715 directly provides the output enable signal to these multiplexers (ROMOE*), as well as the chip select signal to the ROM banks (ROMCS*[2:0]).

The control to the DRAM banks is provided directly by signals coming out of the R3715. These signals can directly control up to 3 banks of DRAM and 40MB. This implementation supports an external DMA master, and so an extra set of latches and transceivers are used to accommodate it. All control signals necessary to provide DMA master and slave operations to the external DMA master are provided. Multiplexing between the external DMA master and CPU is done via BUSGNT*.

The R3715 video/engine interface processes line and page synchronization signals from the engine and provides it with a serial video data stream.

The R3715 also generates the control signals necessary to transfer parallel byte or word data to and from the parallel interface (POE* and PSTROBE*).

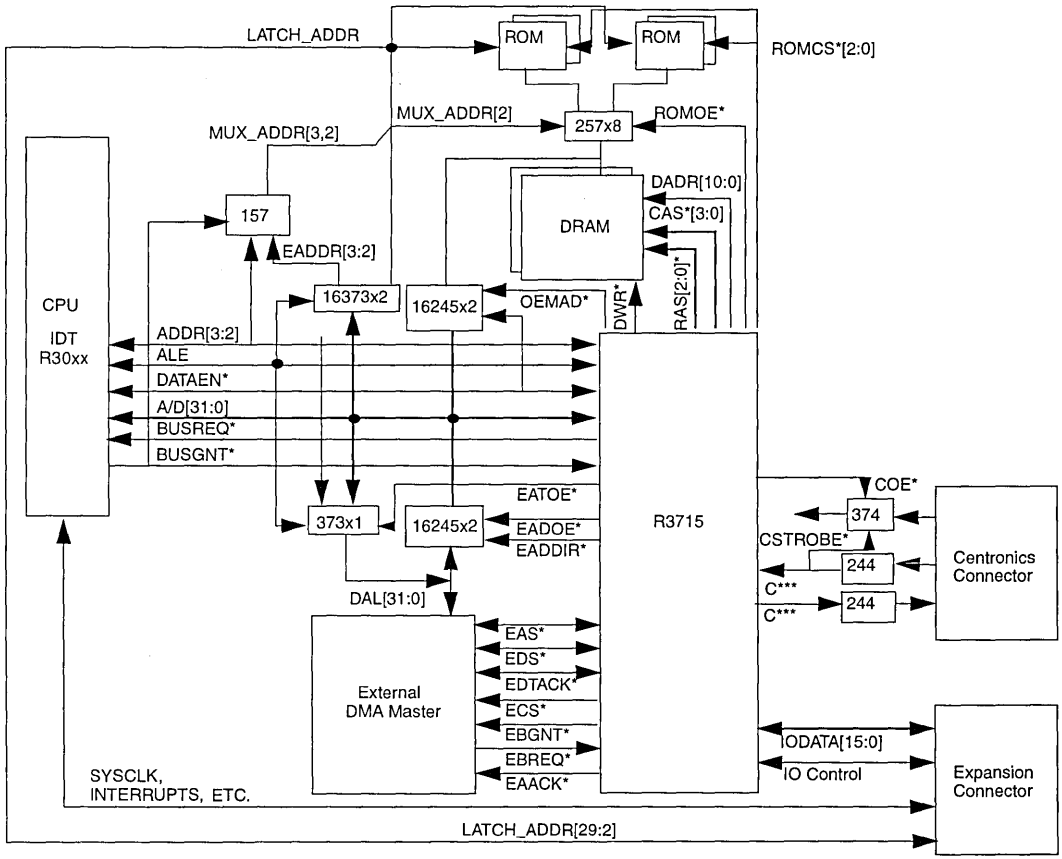


Figure Note: C***=Centronics Control Signals

Figure 5.1 Full Implementation With Interleaved ROM

A full complement of signals is provided by the R3715 to implement an IEEE1284 bi-directional Centronics interface.

The 80186-style I/O bus interfaces to a connector that can be used to expand features by adding standard industry peripherals like SCSI, PCMCIA cards, UARTs, Ethernet, etc.

Minimal Implementation

Figure 5.2 shows a minimal implementation. In this case, we show the lower end CPU in the R3051 Family, the R3041.

A simple non-interleaved ROM subsystem is used in this case, with only 1 bank - the boot bank ROMCS[2]*.

The DRAM system contains only 1 bank and as we mentioned before, the R3715 directly provides all the necessary signals.

Since a coprocessor is not used in this case, the interface to the AD bus is very simple.

The balance of the features shown is the same, but this could conceivably include simpler implementations of each, like less peripherals via the IODATA bus, or a lower video rate that could be associated with an engine with less dots per inch or less pages per minute.

Both the full and the minimal implementations shown demonstrate the flexibility of the R3715 as a common block that enables modular designs or designs that can be upgraded in the field.

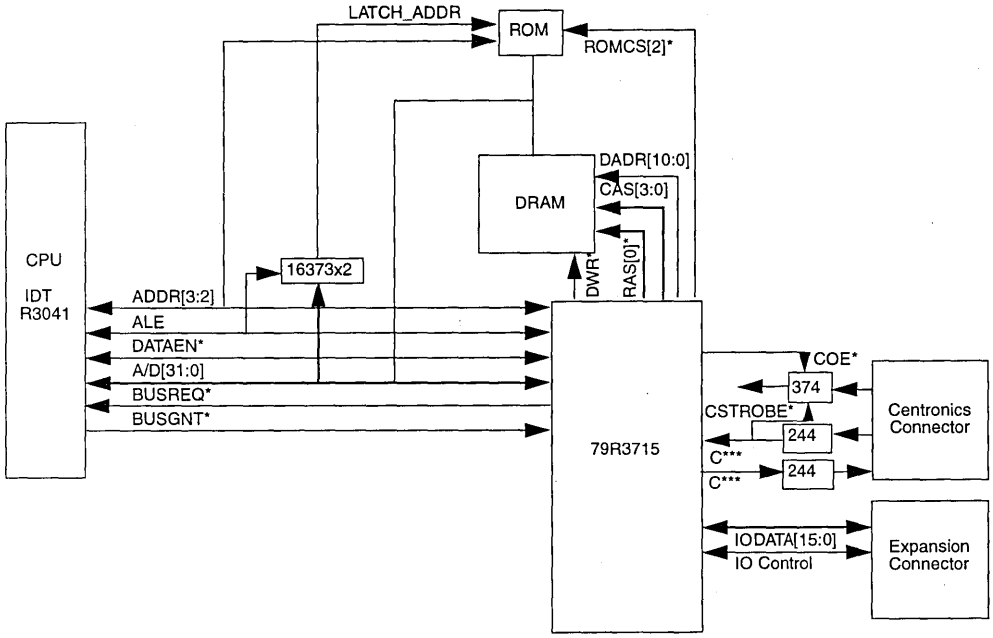


Figure Note: C***=Centronics Control Signals

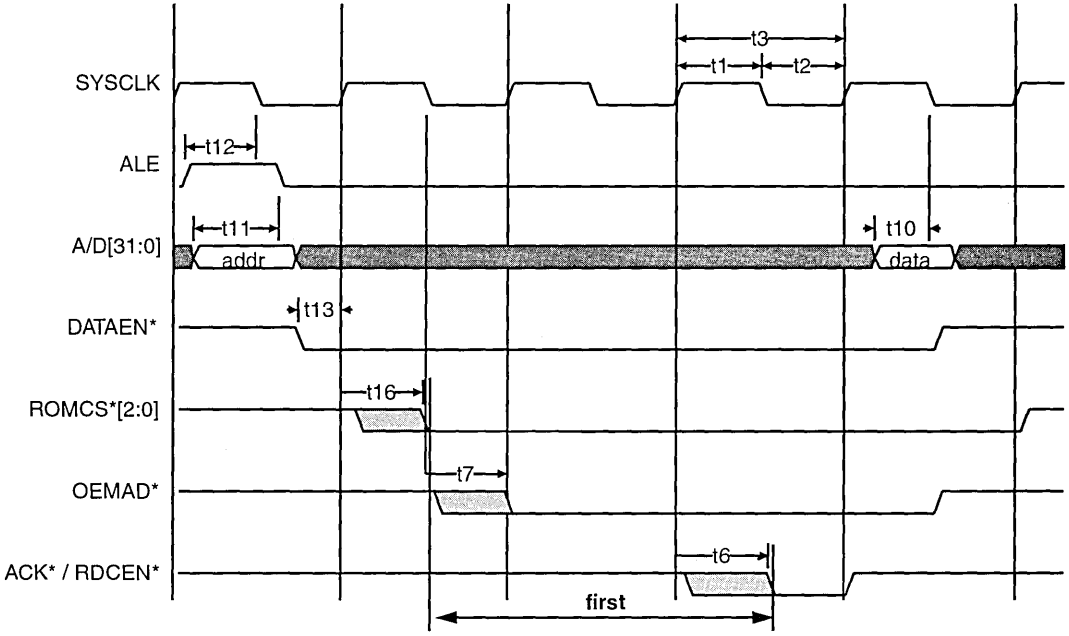
Figure 5.2 Minimal Implementation

PINOUT TABLE

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	AD(14)	41	EAS*	81	IOBE(1)*	121	RAS*[0]
2	AD(13)	42	ECS*	82	IOBE(0)*	122	RAS(1)*
3	AD(12)	43	EAACK*	83	IOGPCS[1]*	123	RAS(2)*
4	AD(11)	44	PIO(0)	84	IOGPCS[0]*	124	CAS(0)*
5	AD(10)	45	PIO(1)	85	IOCS(1)*	125	CAS(1)*
6	VDD	46	PIO(2)	86	IOCS(0)*	126	CAS(2)*
7	VSS	47	PIO(3)	87	DMAREQ(0)	127	CAS(3)*
8	AD(9)	48	PIO(4)	88	DMAREQ(1)	128	DWR*
9	AD(8)	49	PIO(5)	89	IODATA(15)	129	ROMCS(2)*
10	AD(7)	50	CSELECTIN*	90	IODATA(14)	130	VDD
11	AD(6)	51	CINIT*	91	IODATA(13)	131	VSS
12	AD(5)	52	CSTROBE*	92	IODATA(12)	132	ROMCS(1)*
13	AD(4)	53	CRSTROBE	93	IODATA(11)	133	ROMCS(0)*
14	AD(3)	54	CBUSY	94	IODATA(10)	134	ROMOE*
15	AD(2)	55	VDD	95	IODATA(9)	135	Reserved
16	AD(1)	56	SYSCLK	96	IODATA(8)	136	Reserved
17	AD(0)	57	VSS	97	IODATA(7)	137	Reserved
18	VDD	58	CWSTROBE	98	IODATA(6)	138	Reserved
19	VSS	59	CROE*	99	IODATA(5)	139	AD(31)
20	VSS	60	VDD	100	IODATA(4)	140	AD(30)
21	BURST*	61	CAUTOFD*	101	VDD	141	AD(29)
22	ADDR(3)	62	CPERROR	102	VDD	142	AD(28)
23	ADDR(2)	63	CSELECT	103	VSS	143	VSS
24	ALE	64	CWOE*	104	IODATA(3)	144	AD(27)
25	RD*	65	CACK*	105	IODATA(2)	145	AD(26)
26	WR*	66	CFAULT*	106	IODATA(1)	146	AD(25)
27	DATAEN*	67	POE*	107	IODATA(0)	147	AD(24)
28	BUSGNT*	68	PSTROBE*	108	DADR(10)	148	AD(23)
29	RESET*	69	N.C.	109	DADR(9)	149	AD(22)
30	ACK*	70	N.C.	110	DADR(8)	150	VDD
31	RDCEN*	71	N.C.	111	DADR(7)	151	VSS
32	BUSREQ*	72	N.C.	112	VDD	152	AD(21)
33	INT*	73	VDD	113	VSS	153	AD(20)
34	EADOE*	74	VSS	114	DADR(6)	154	AD(19)
35	EADDIR*	75	IOWAIT*	115	DADR(5)	155	AD(18)
36	EATOE*	76	DMAACK(1)*	116	DADR(4)	156	AD(17)
37	EDTACK*	77	DMAACK(0)*	117	DADR(3)	157	AD(16)
38	EDS*	78	IOWR*	118	DADR(2)	158	AD(15)
39	EBREQ*	79	IORD*	119	DADR(1)	159	OEMAD*
40	EBGNT*	80	IOA1	120	DADR(0)	160	TEST

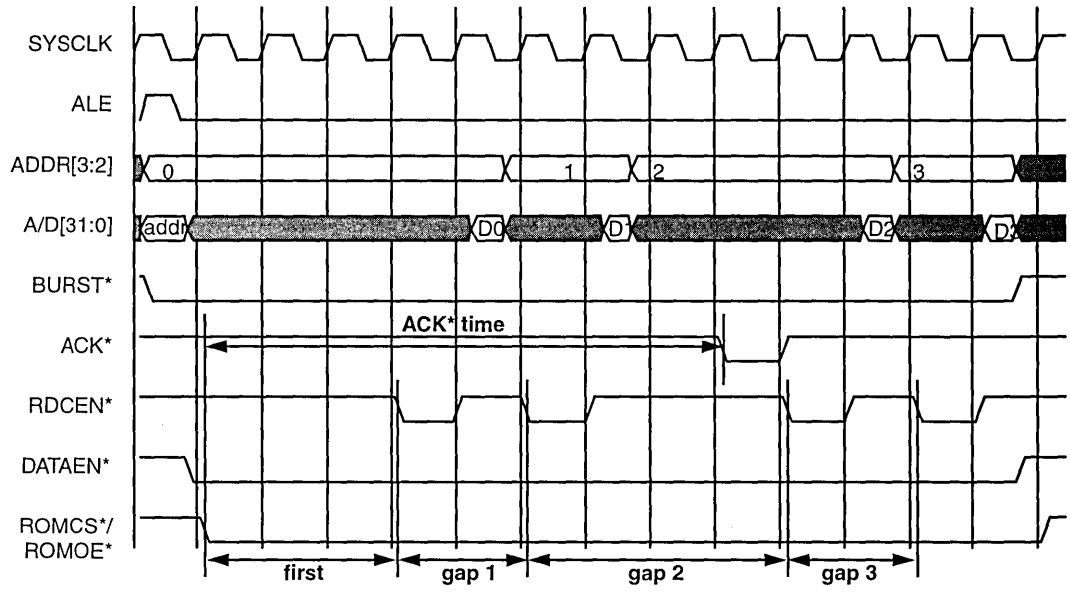
TIMING DIAGRAMS

This section contains timing diagrams for the R3715 signals.

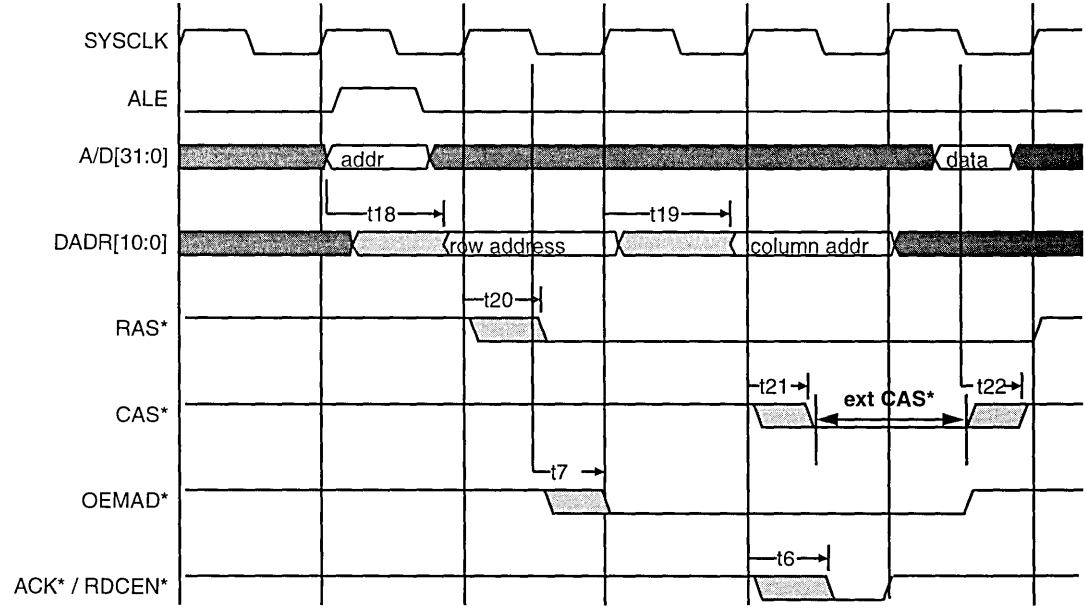


ROM Read (Programmable)

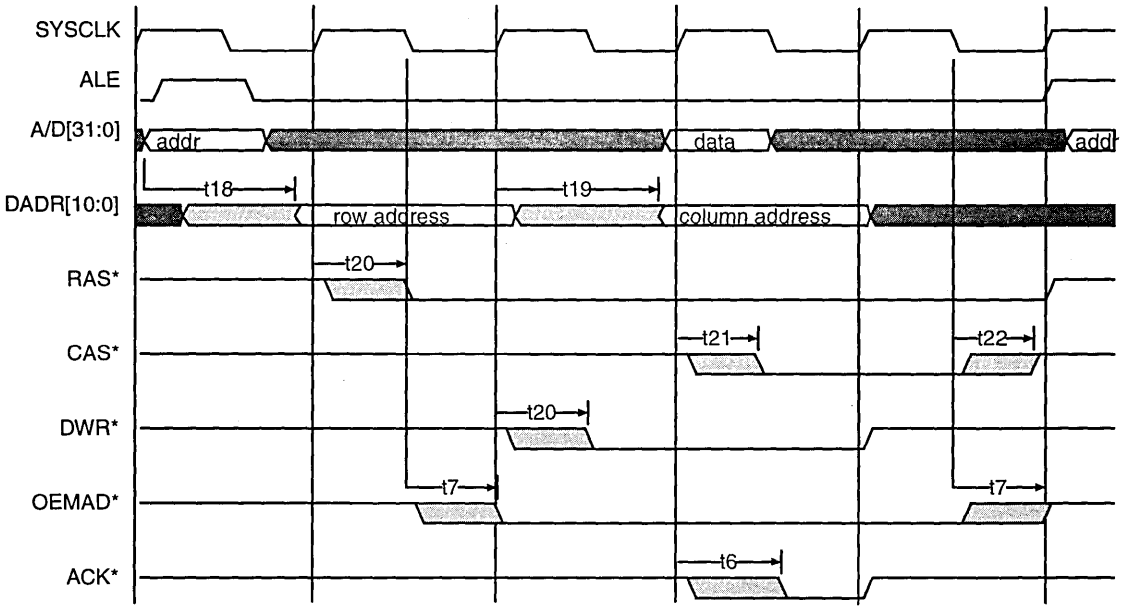
6



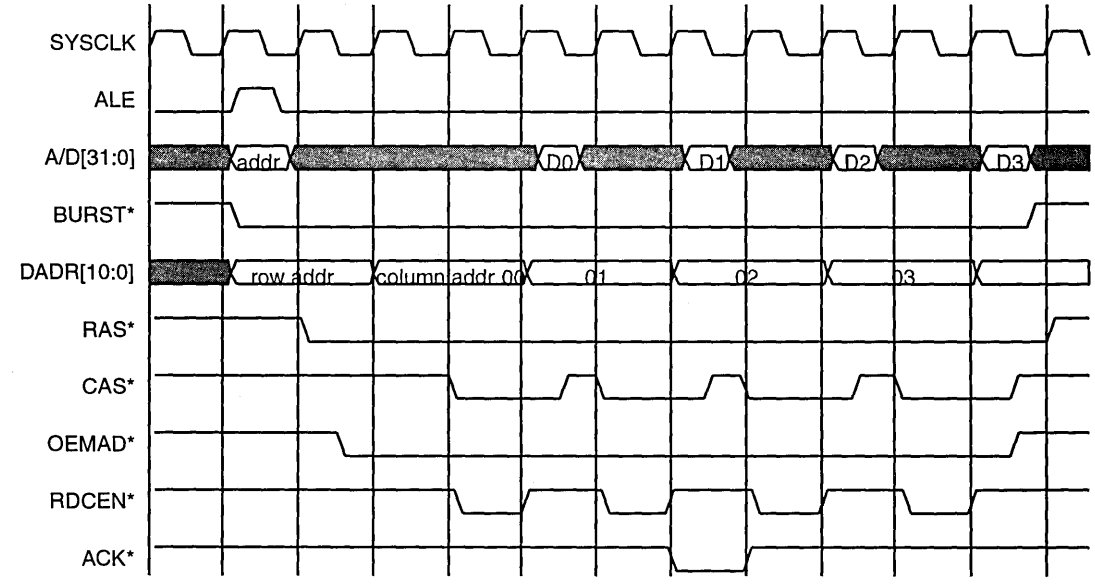
Interleaved ROM Burst Read (Programmable)



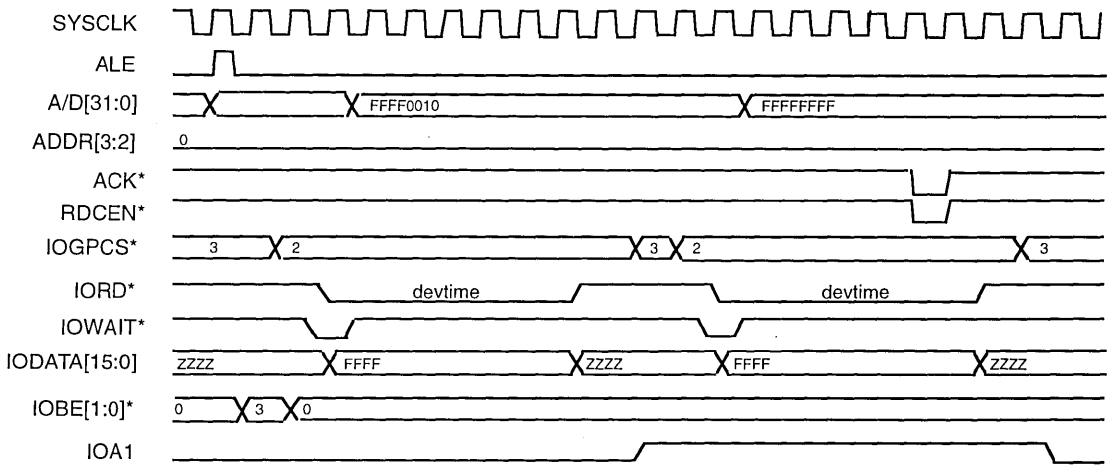
DRAM Read (Programmable)



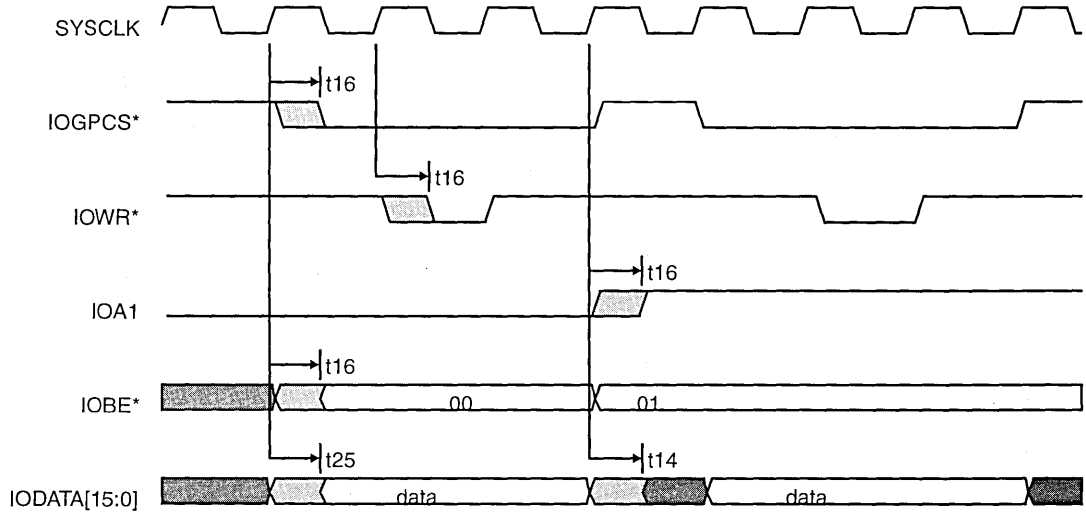
DRAM Write



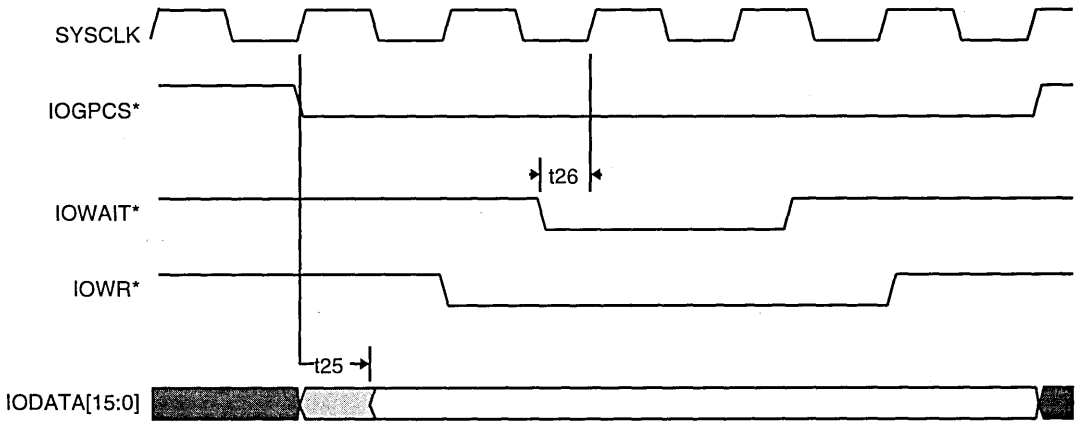
DRAM Burst Read



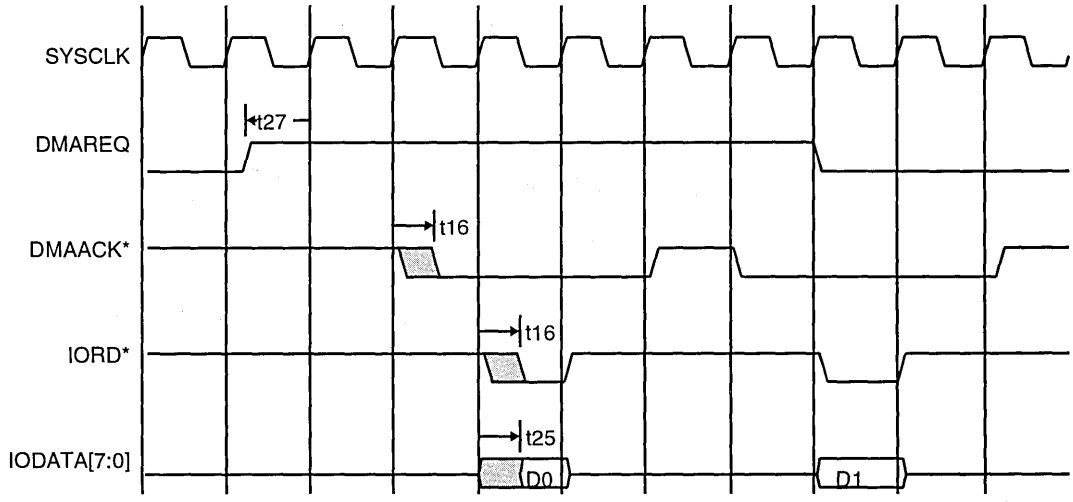
I/O Read 16-Bit



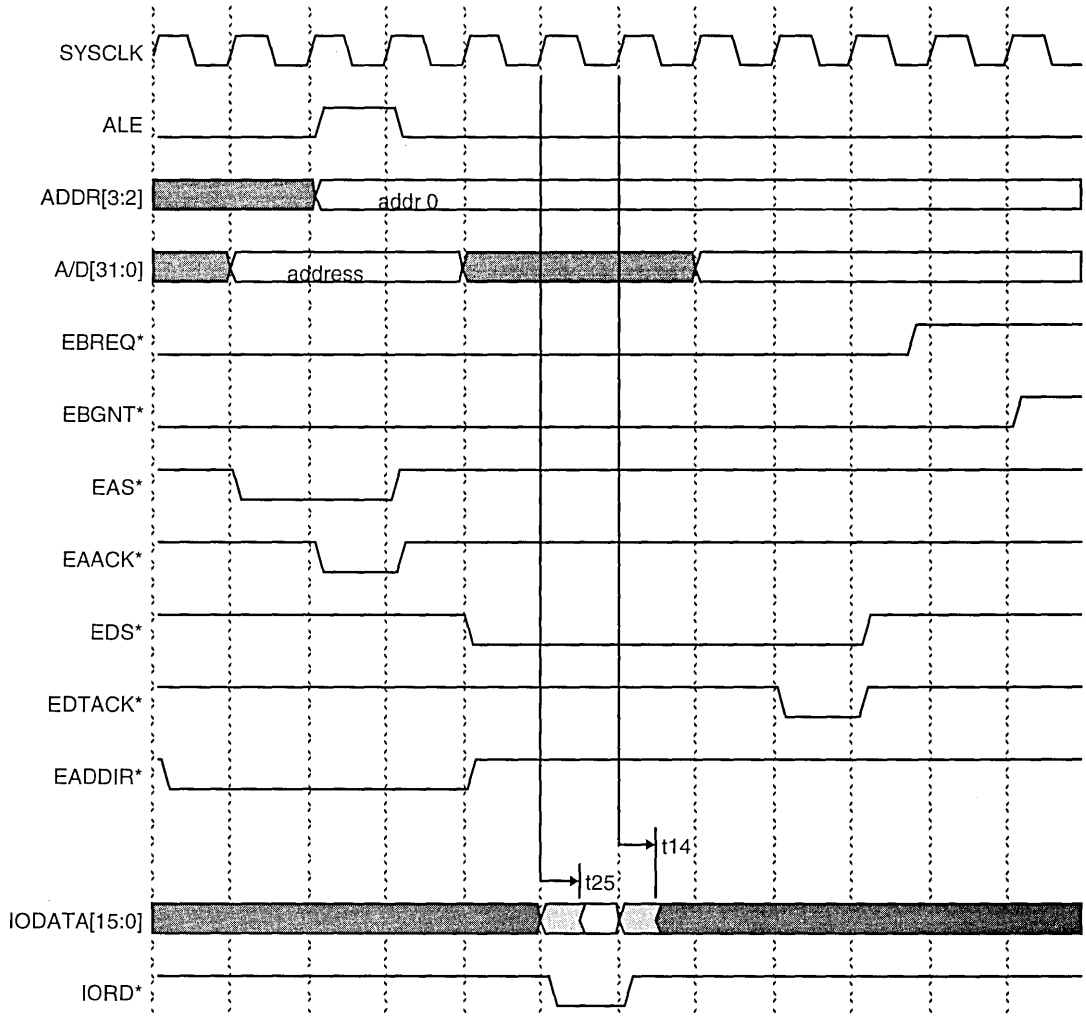
I/O Write 24-Bit



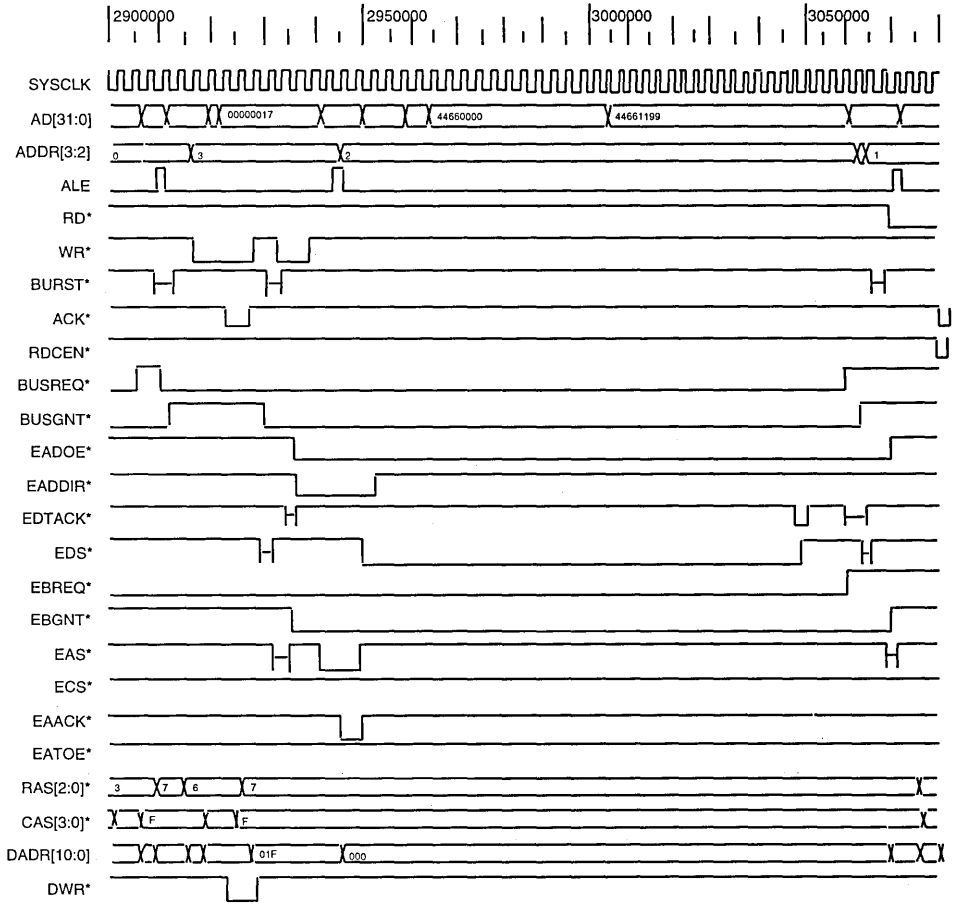
I/O Write (With Wait State)



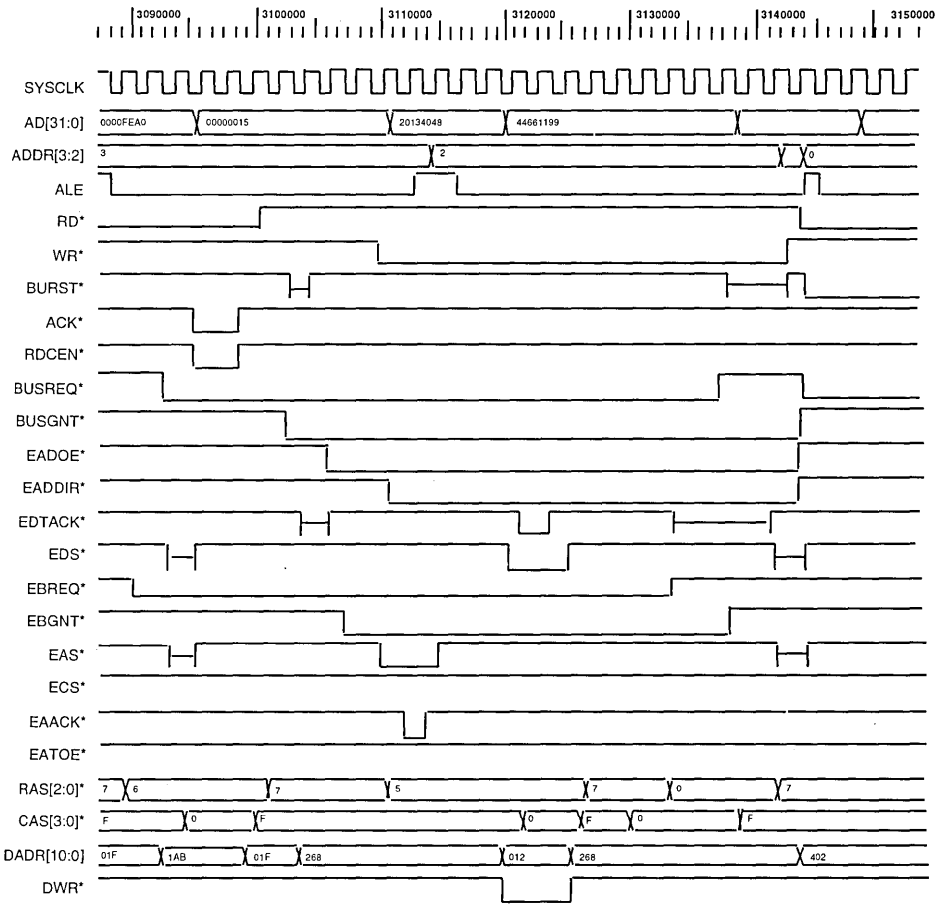
I/O Bus DMA Read



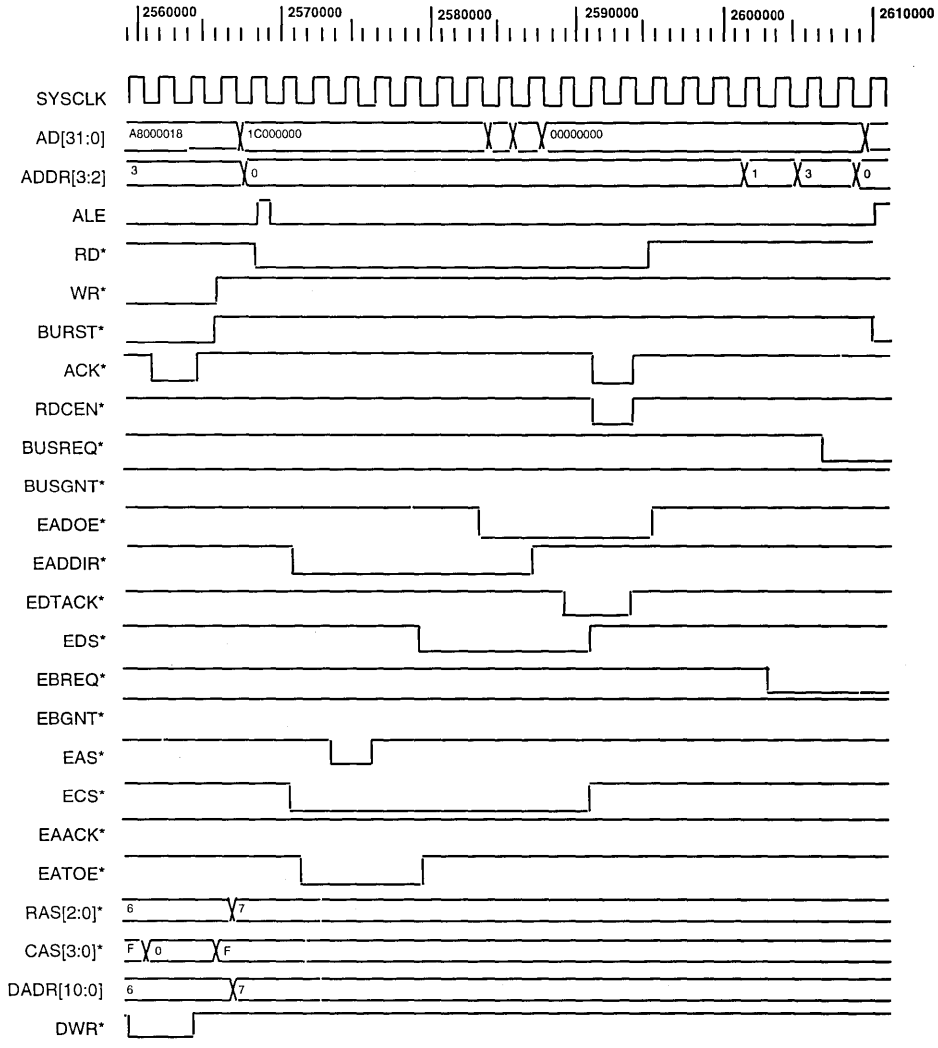
External DMA Master— Master I/O Read



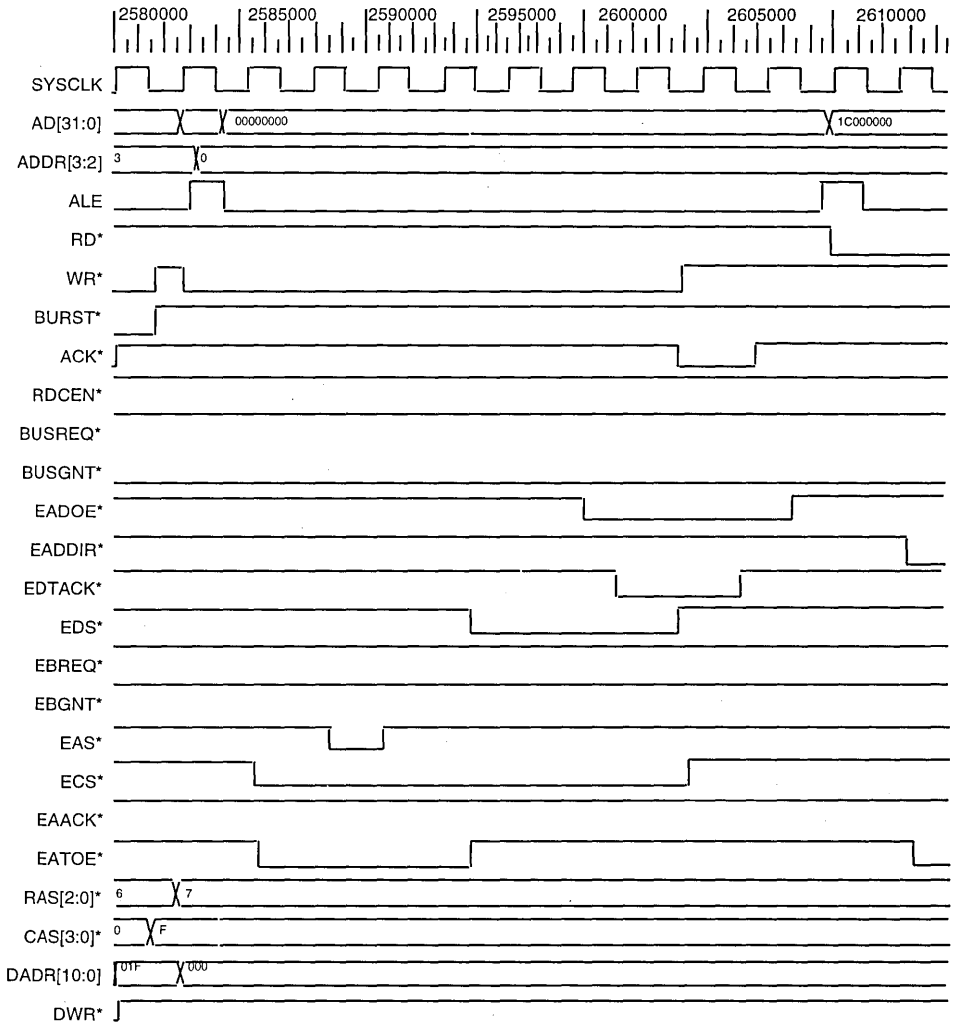
External DMA Master— Master Read



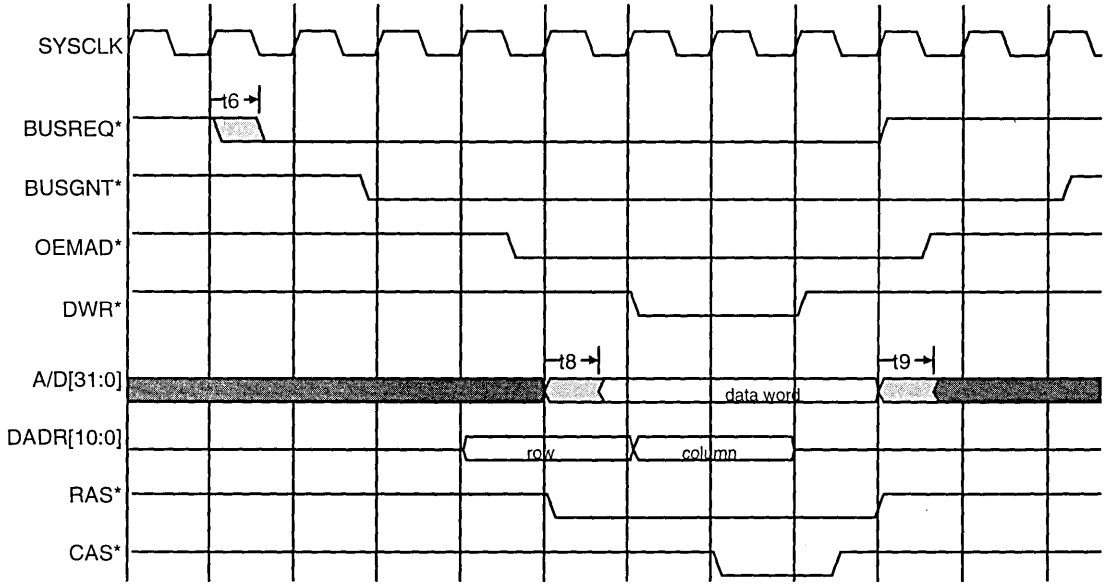
External DMA Master— Master Write



External DMA Master— Slave Read

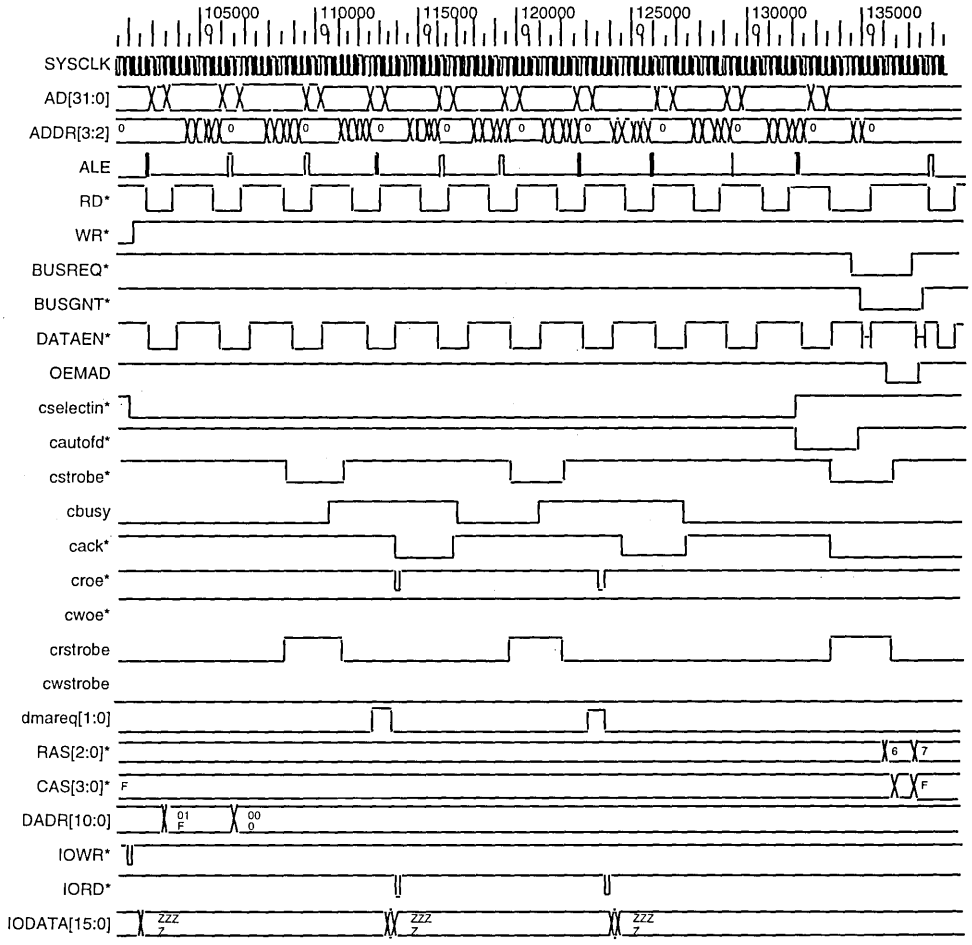


External DMA Master— Slave Write



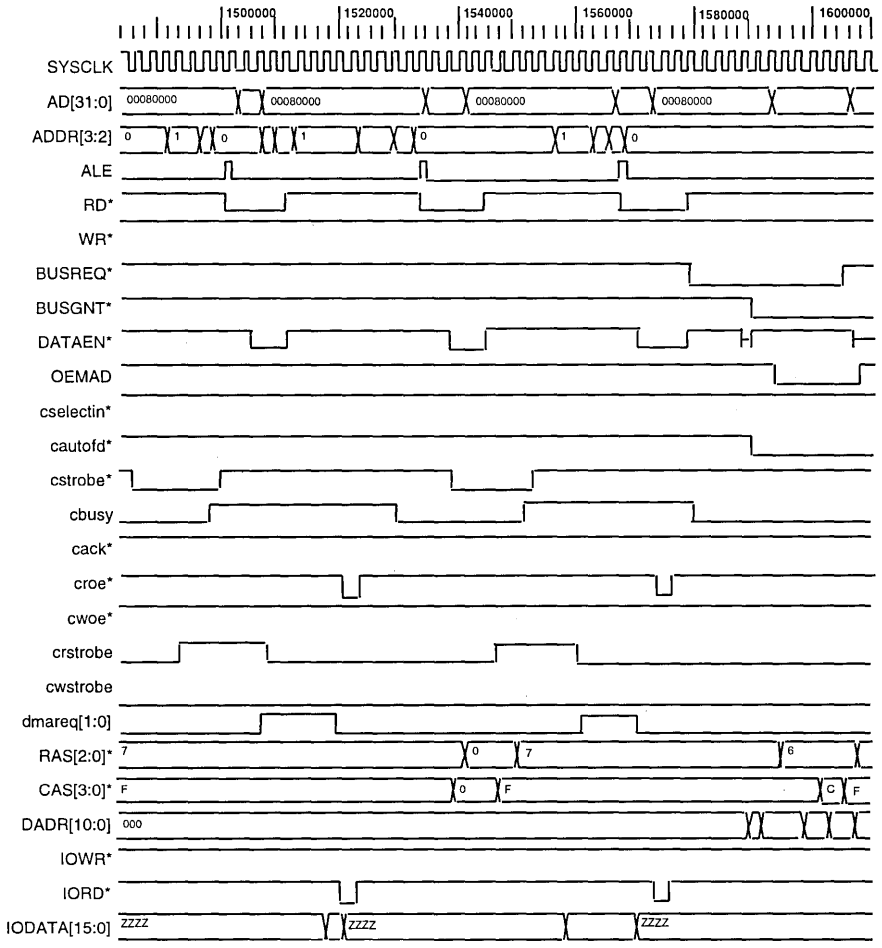
A/D Bus DMA Write

6

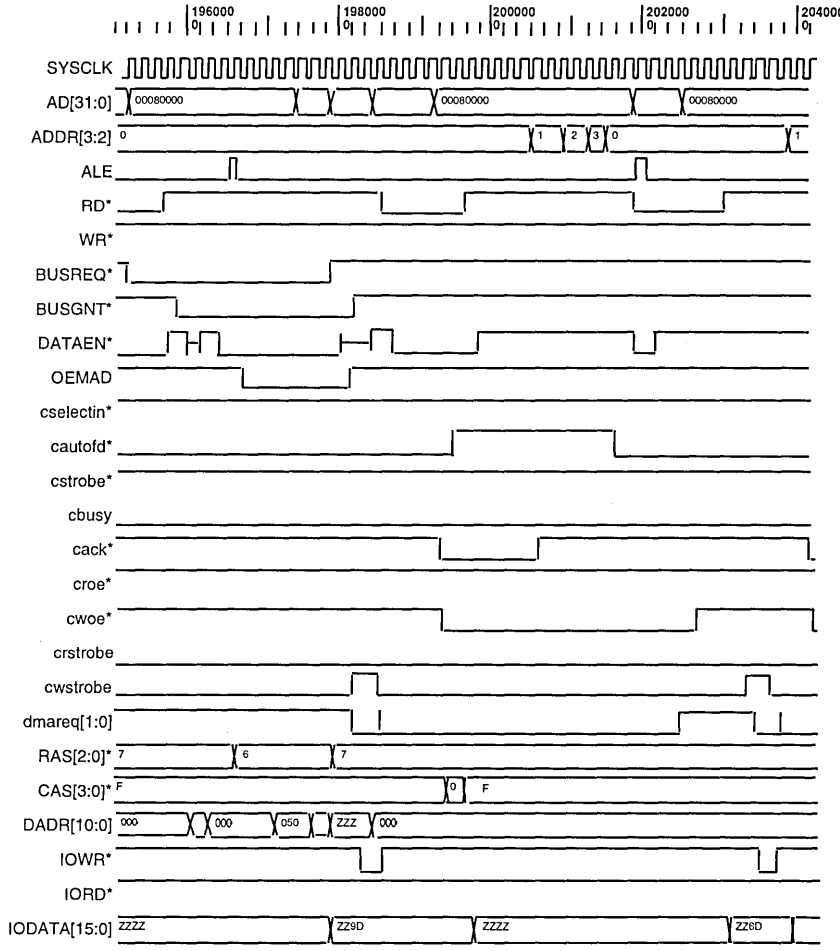


Centronics Compatible DMA—Standard

(Application=00)



ECP Forward Transfer



ECP Reverse Transfer

PACKAGE

160-Pin Quad Flat Package (QFP, EIAJ)

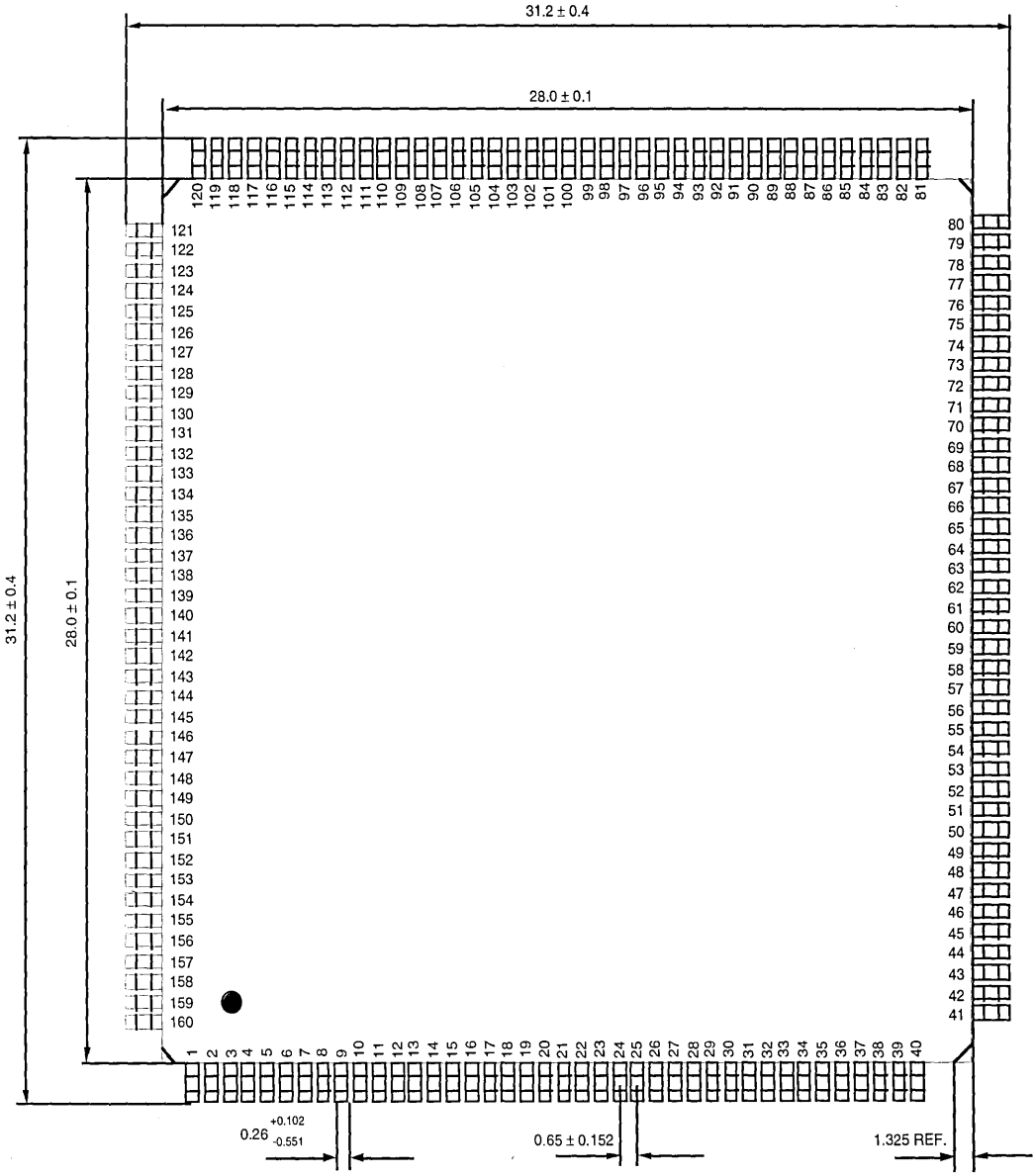


Figure 10.1 160-Pin Quad Flat Package

3134 drw 03

160 - Pin Quad Flat Package—Expanded View (QFP, EIAJ)

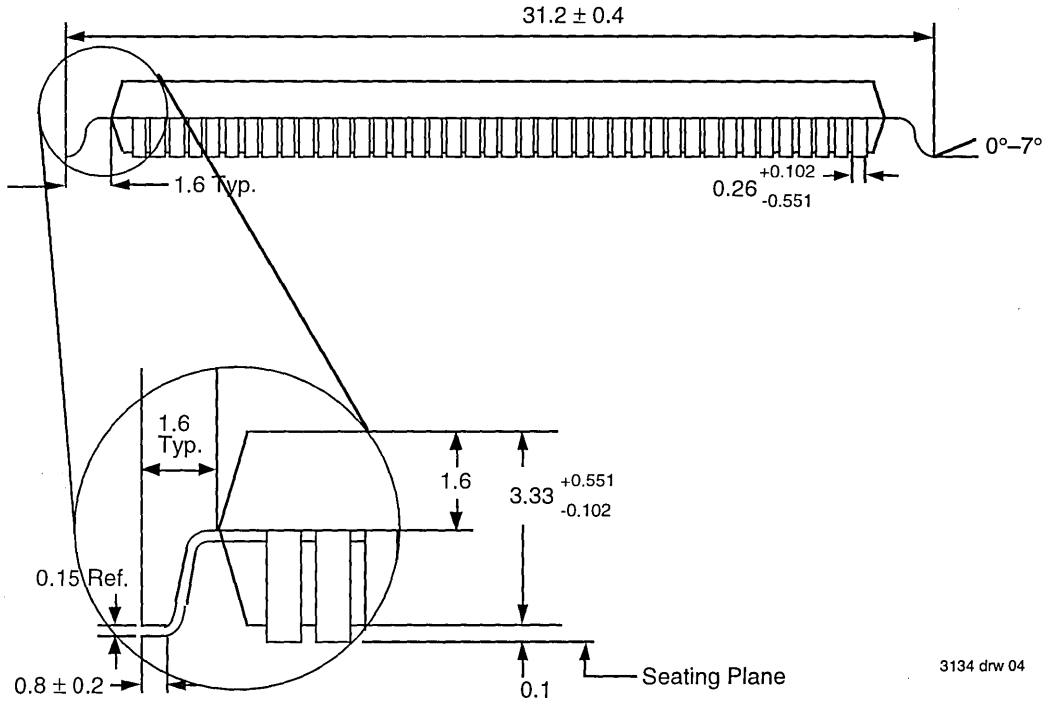


Figure 10.2 Expanded View of Figure 10.1 Detail

VALID COMBINATIONS

79R3715PF	160-pin PQFP

Integrated Device Technology, Inc.

LASER PRINTER INTEGRATED SYSTEM CONTROLLER

IDT79R3710
IDT79R3740
ADVANCE INFORMATION

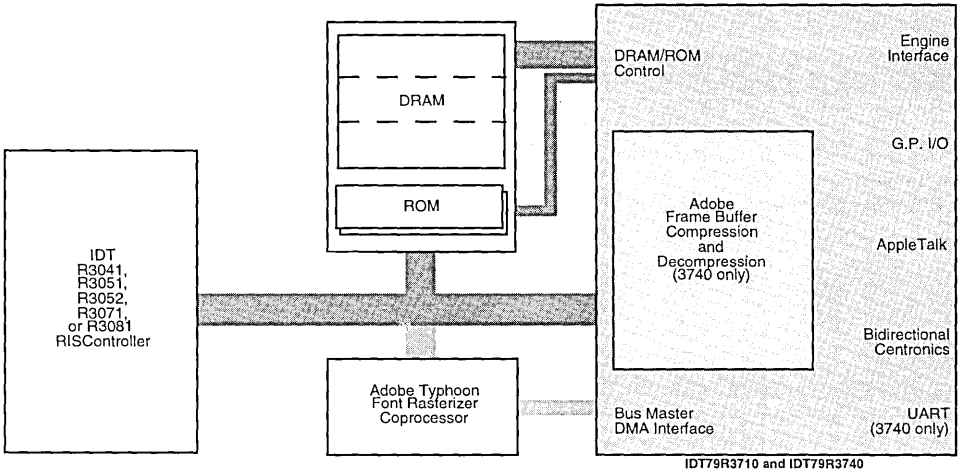
FEATURES

- Pin-Compatible System Controller with Laser Printer-specific features for the IDT R30xx family of processors
- DRAM Controller
  - 1 - 40 MB directly, 1 - 3 banks directly
  - Device depth supported: 256K - 4M
  - Non-interleave
- ROM Controller
  - 1 - 20MB, Address-space support bank size: 1- 8MB
  - Support for standard and burst ROMs
  - Support for interleave or non-interleave
- Direct Interface to Adobe Typhoon rasterizer coprocessor
- I/O Bus follows 8/16-bit Intel 80186 style
- I/O Controller
  - Two 8-bit and two 16-bit external channels
  - DMA and non-DMA access for the 8-bit channels
  - 8-32 packing, 32-8 unpacking logic for DMA access
  - 16-32 packing, 32-16 unpacking for CPU/ Typhoon coprocessor accesses
  - Round robin arbitration
  - Programmable timing for I/O and control signals
  - Big and little endian support
- PCMCIA Support
  - Through 16-bit I/O bus, using simple glue logic
  - 16-bit to 32-bit packing and 32-bit to 16-bit unpacking
  - Big and little endian support
  - 256MB address space dedicated to 2 PCMCIA slots
- Engine Control
  - Supports control and status lines to the engine
  - Horizontal and vertical margin counters
- 24-bit Timer/Counter, In-Circuit testing capability
- High-performance CMOS technology
- Video Controller
  - Four-entry (32-bit wide) FIFO with data serializer
  - Video data Phase Lock Loop (PLL)
  - DMA support (with chaining)
  - Full duplex printing support
  - Inverse video
  - 10MHz with PLL, 28MHz with external clock
- Centronics Interface
  - Bi-directional Centronics, compliant with IEEE1284
  - Supports DMA and CPU controlled transfers
  - Supports the following modes:
  - Compatible; Nibble; Byte; ECP; EPP
- Interrupt Controller
  - 6 external level interrupts (through the PIO pins)
  - 14 internal interrupts
  - Individual interrupt mask capability, enabling polling or interrupt-driven systems
- General Purpose I/O
  - Six programmable Input (interrupts) or Output pins

Special IDT79R3740-only features

- UART on-chip, 16550-style
- Incorporates Adobe Memory Booster Technology
  - Achieves greater than 4:1 lossless compression for most pages
  - Reduced DRAM requirements up to 4 MB for 600 dpi letter-size; with higher resolutions, achieves even greater DRAM savings
  - Supports monochrome and bi-level color devices
  - Always prints the page with minimum memory cost
  - Supports printer page rates up to 20 ppm

6



IDT79R3710 and IDT79R3740 System Organization

3710-20

OVERVIEW

The IDT79R3710 and IDT79R3740 are single chip CMOS System Controllers designed to complement IDT's R30xx family of 32-bit embedded processors. They have all of the features necessary to implement a high-performance, high-quality, feature-rich laser printer, at a similar or lower cost than that of low-end laser printers.

For instance, both the R3710 and R3740 facilitate the implementation of high-quality Multi-Function imaging products (printers that include functions such as fax, copier, or scanner). In addition, the R3740 includes state-of-the-art Adobe Memory Booster (AMB) technology. The R3710 and R3740 can be interchanged in a single design, allowing multiple end products from a single design effort.

The R3710 and R3740 support high resolution printers, since they can move large amounts of data quickly without the need for processor intervention. They also achieve a significant reduction in system cost by their high level of integration, and for the R3740, from the AMB circuitry on-board. Additional savings come from the architecture of the I/O controller, which allows for the utilization of low cost peripheral components (disk controller, network controller, etc.), while attaining the higher level of performance only associated with costlier components.

Some of the architectural characteristics that result in very high performance include:

- incorporating a tightly coupled interface to the R30xx RISC CPU;
- minimizing latency to critical resources;
- partitioning the system in a balanced way to attain efficient use of shared resources;
- enabling several simultaneous operations in the system.

The R3710 and R3740 are ideal for modular design of laser printers because they allow a high level of programmability, and because they incorporate the control logic for an industry standard interface to peripherals. This gives OEMs the ability to offer several products from the same basic design, as well as the ability to upgrade systems in the field.

Block diagrams on the following page show R3710 and R3740 configuration.

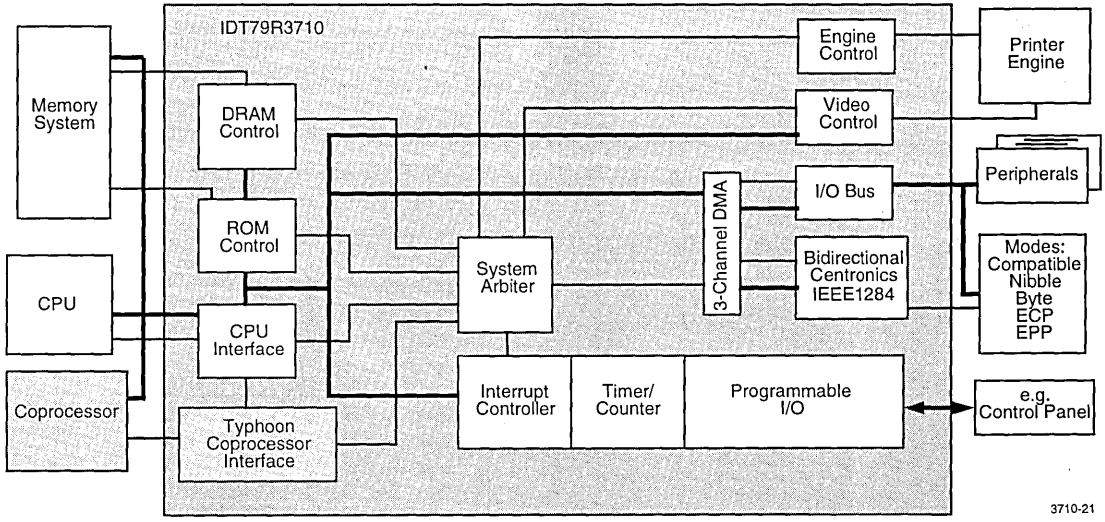
Adobe Memory Booster Technology (For the R3740 only)

In the R3740 Controller Adobe and IDT provide a comprehensive solution for memory cost reduction that supports a complex set of system goals. Two underlying printer implementation strategies are supported.

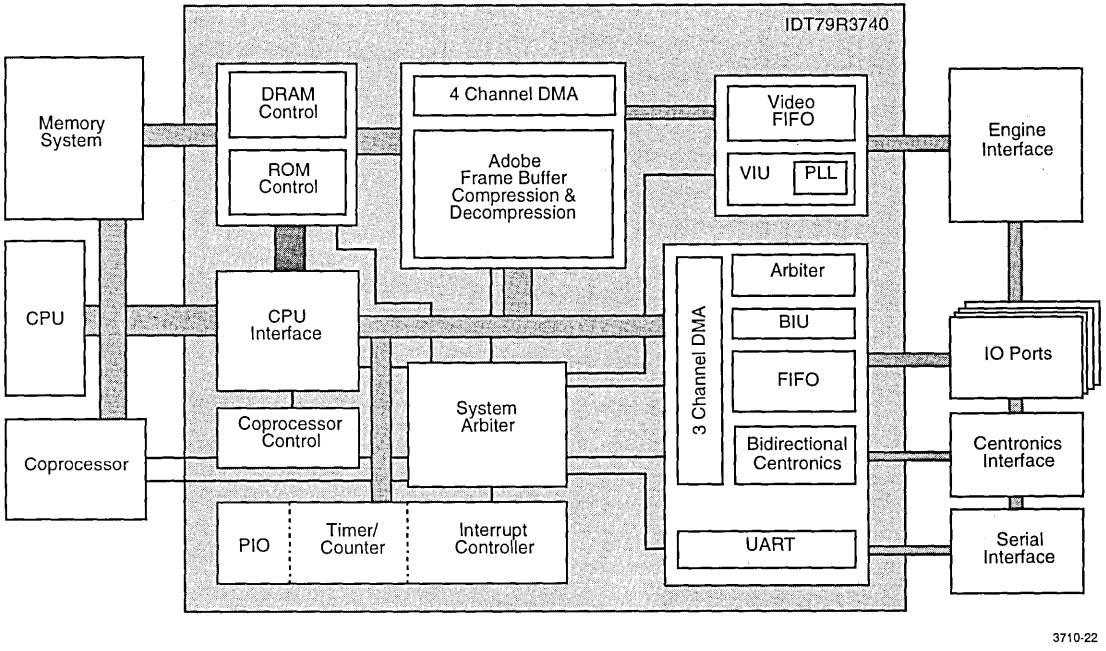
First, the compression scheme must consistently provide greater than four-to-one compression for most of the pages printed, across a wide range of page styles, using a lossless compression algorithm to maintain high page quality, regardless of data type (fonts, graphics or scanned halftone images). This affords the opportunity to significantly lower memory cost.

Secondly, Adobe memory booster always prints the page, avoiding the all-or-nothing extreme of full compression or the "page not printed because" error message. To implement this strategy, Adobe Memory Booster utilizes a two-step process, beginning with a lossless compression algorithm to provide full compression in a minimum memory system. If this cannot be achieved in the available memory space, a new data compression technology from Adobe provides a price/quality trade-off by achieving a higher compression ratio.

Both the lossless and the alternative compression technologies used by Adobe Memory Booster are implemented in the R3740, providing full support of this cost- saving strategy.



IDT79R3710 Block Diagram



IDT79R3740 Block Diagram

FUNCTIONAL DESCRIPTION

Processor Interface

The R3710 and R3740 have a glueless interface to the IDT R3041/51/52/71/81 family of RISC processors. They operate either as a slave, supporting CPU access to memory and I/O devices, or as a master, handling accesses on the A/D bus.

As slave the R3710 or R3740 supports processor single transfer read or write, as well as burst read access. Each supports processor access to the ROM, DRAM, devices on the I/O bus, the Typhoon coprocessor and the R3710 or R3740 internal registers. Burst read is supported only for DRAM or ROM read access. ACK* and RDCEN* timing is fixed for both the R3710 and R3740 registers. DRAM access can be extended by one clock, and access timing for ROM and I/O are programmable.

As master the R3710 or R3740 will request the bus by asserting BUSREQ* when a DMA source (internal or external) needs to transfer data to or from the DRAM / ROM / I/O Channel.

The priority between the DMA sources is in the following descending order:

- Access in process
- Video out
- Decompression and compression (for the R3740 only)
- I/O DMA
- Typhoon.

The CPU will get ownership of the A/D bus for at least one cycle after four DMA accesses. This assumes that each Typhoon (external agent) bus possession is counted as one, regardless of the number of transfers it executes on the bus. In the default state, when there is no DMA request, the bus is owned by the CPU.

Figure 2.1 shows the CPU-to-R3710/R3740 interface.

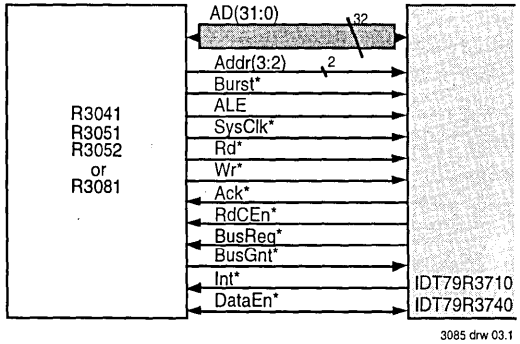


Figure 2.1: RISController to R3710/R3740 Interface

Co-Processor (Typhoon) Interface

The R3710 and R3740 have simple interfaces to the Typhoon coprocessor. They support the Typhoon in its slave and master modes of operation. As slaves they support the processor read and write accesses to the Typhoon, and as masters they enable Typhoon access to the DRAM, ROM, and 16 bit I/O bus (for font cartridges). The R3710 and R3740 directly control the data buffers and the address buffer needed to isolate the Typhoon from the A/D bus.

The R3710 and R3740 decode CPU access to the Typhoon and assert TCS*, TAS*, and TDS*. The address is latched into an external transparent latch (373-type) when the processor asserts ALE and is driven into the Typhoon multiplexed bus (DAL[31:0]) by TATOE*. Data is driven to or from the Typhoon by transceivers controlled by TADDIR* and TADOE*. To end a Typhoon cycle both the R3710 and R3740 assert RDCEN* and ACK* to the CPU when the Typhoon asserts TDTACK*.

In Typhoon master mode, the Typhoon requests the bus by asserting TBREQ*. The R3710 or R3740 will grant the bus by asserting TBGNT* (provided no other DMA device has requested the bus and provided also that it was granted by the CPU to the R3710 or R3740). The Typhoon will assert TAS* first, and then TDS*, to initiate an access to a system resource (e.g. DRAM). The R3710 or R3740 will assert TADOE* and TADDIR* to drive the Typhoon address, and ALE to latch it. In the data phase it will assert TADDIR* and TADOE* according to the access direction (Read or Write).

To end the cycle the R3710 or R3740 will assert TDTACK* to the Typhoon. When it does not require the bus any longer the Typhoon will release it by deasserting TBREQ*

Typhoon access to the DRAM takes 5 clocks from TAS* to TDTACK*. Frequencies above 25 MHz may need an additional clock cycle. One clock can be added to this interval by using the TypExtCas bit in the DRAM control register.

Figure 2.2 shows the implementation of the Adobe Typhoon Coprocessor interface.

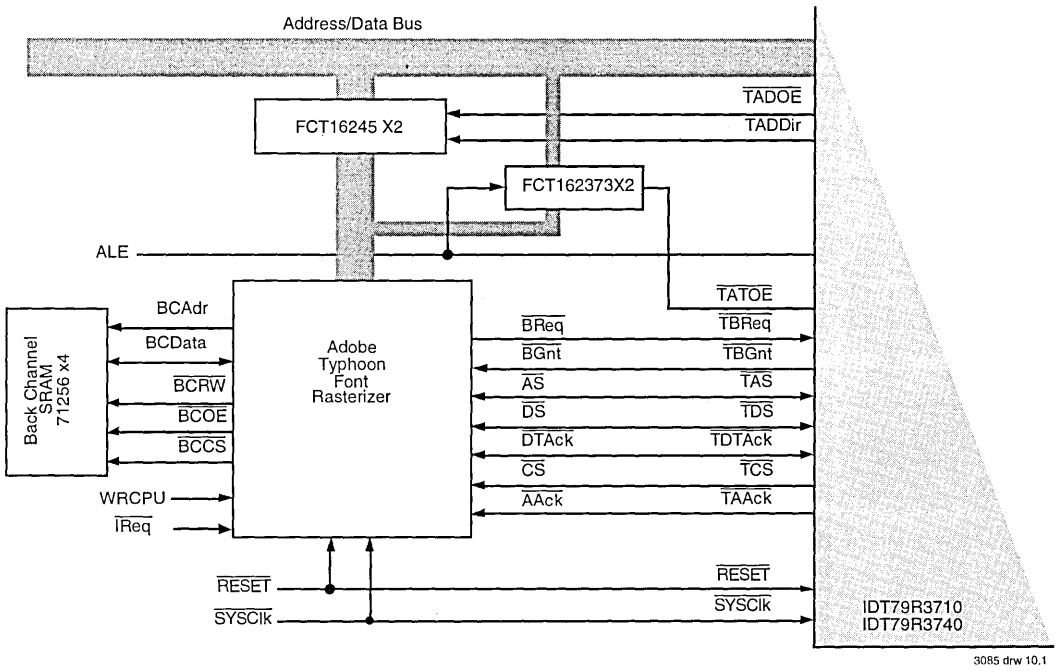


Figure 2.2: Adobe Typhoon Coprocessor Implementation

ROM

The ROM controller supports up to 20 Mbyte of memory with several device types and system configurations. To support these system and device options, the assertion time of RDCEN* and ACK* by the R3710 and R3740 can be programmed, thus accommodating different types of memory architectures, including standard ROMs, interleaved ROMs, and burst ROMs.

There are three CS signals to support up to three banks of ROM. Each ROM bank can be either non-interleaved or interleaved (composed of 2 leaves of ROM differentiated by ADDR[2]). ROMCS[2]* controls the boot bank and has a fixed address space of 4 Mbyte. Address space for ROMCS[1]* and ROMCS[0]* is programmable to 1, 2, 4, or 8 Mbyte.

The R3710 or R3740 puts the 3 ROM bank address ranges in a contiguous address space. In other words, the start address of the next ROMCS[x]* will follow the last address of the previous ROMCS[x-1]*. For interleaved support, ROMOE* is provided to control the OE of the interleave multiplexer. The R3710 and R3740 also support burst ROMs, and can be made to write to the ROM space (for Flash or debug) with additional glue logic.

After reset, the R3710 or R3740 is configured with the maximum number of wait states between each data transfer (16 clocks between each RDCEN*) and 64 clocks between ROMCS[x]* to ACK*. The initial (reset) space size for ROMCS[1]* and ROMCS[0]* is 1 Mbyte, and 4Mbytes for ROMCS[2]*.

Figure 2.3 shows the configuration of the ROM/DRAM memory system.

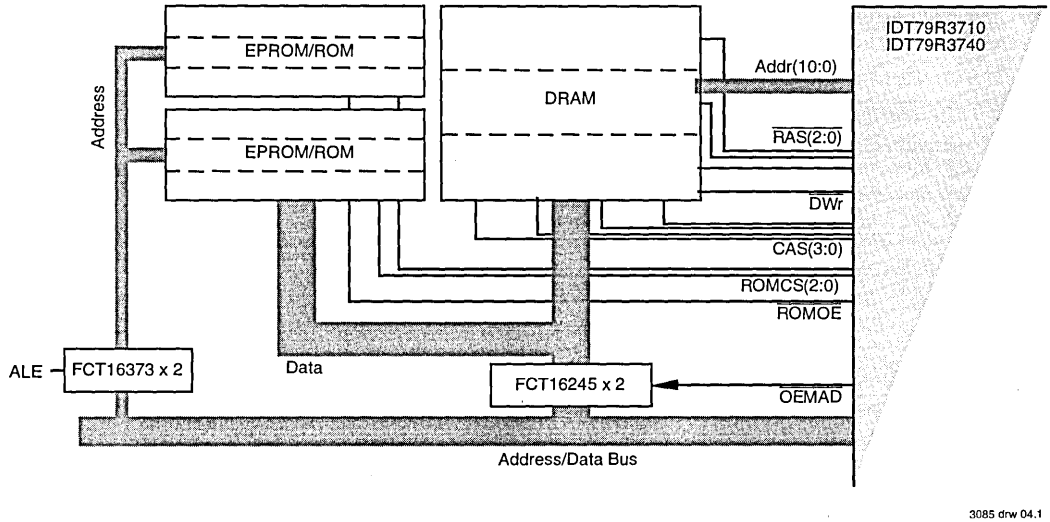


Figure 2.3: R3710/R3740 ROM/DRAM Memory System

DRAM

The DRAM controller supports directly 1 to 40 Mbytes of DRAM, with up to three non-interleaved banks. The address space starts at physical address 0. The DRAM device types supported have the following attributes: page mode, early write, and "CAS before RAS" refresh.

The DRAM controller supports single transfer reads and writes and burst reads. Various DRAM device depths are supported and the address space is continuous for the selected configuration. The DRAM controller can be configured to support different device depth for the base bank (RAS[0]*) and the extension banks (RAS[1]* and RAS[2]*).

For systems running at high frequency there is an option to extend the CAS* signals by an additional cycle. Since the Typhoon samples data on the rising edge of SYSCLK*, and the CPU on the falling edge, for systems above 25MHz it may be necessary to extend the CAS* by one cycle for Typhoon accesses. To minimize the refresh penalty IDT recommends you program the refresh frequency according to the value of SYSCLK*.

The initial values of the R3710 and R3740 control registers at reset are shown in section 3.13.

Programmable Engine Interface

The R3710 and R3740 move data from the page buffer memory (for the R3740, compressed data in DRAM) to the print engine by DMA in two ways: 1) For the R3740, through the decompression logic for compressed bands, or 2) for the R3710, directly. 32-bit words are buffered in a 4-deep, 32-bit-wide video FIFO and serialized for output to the print engine video input. A video PLL is provided for synchronization of the video to LineSync. A PLL bypass option is provided for systems with an already-synchronized video clock.

The Serializer can shift video data in either direction to support duplex printing. Also, horizontal and vertical margin counters are provided and appropriately synchronized to PageSync and LineSync.

Figure 2.5 shows the R3710/R3740 engine interface.

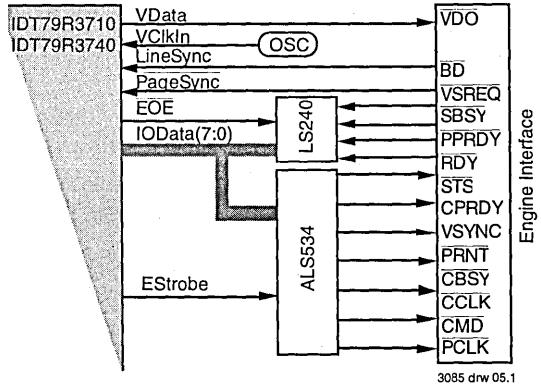


Figure 2.5: R3710/R3740 Engine Interface

PIO Port

Each of the PIO[5:0] pins can be individually programmed to be an output or input pin by writing to the PIO Control register. When programmed as an input pin it can be used as a level (active LOW) interrupt. The PIO pins are synchronized and pulled up internally. At reset, all PIOs are initialized as inputs.

For the R3740 only, the PIO(4) and PIO(5) pins are shared with the UART pins RI and DCD, respectively. Their functionality (PIO or UART) is determined by bit 6 in the PIO control register.

Interrupt Controller

Each interrupt source on the R3710 and R3740 is maskable. The Cause register bit will reflect the cause of the interrupt, and writing a '0' into it will acknowledge the internal interrupt. For example - if the "BandInt" bit was active, the CPU should write 'fffB' into the Cause register, in order to reset the interrupt flag.

The external interrupts, PIO[5:0], are acknowledged at the source of the interrupt (the interrupt flag is deasserted when PIO is inactive), the corresponding bits in the Interrupt Cause register are read only.

At reset, all interrupts are masked in the mask register.

DMA AppleTalk

One of the DMA-supported I/O channels can be used to support AppleTalk directly, with only the addition of an external communication controller, such as the 85C30 or 85C230, and the I/O interface devices it requires. The R3710 and R3740's I/O FIFO and Burst DMA capabilities aid in the separation of the real-time demands of the AppleTalk protocol from the real-time demands of the engine interface, but without the system cost implications of "buffered" AppleTalk.

Figure 2.8 shows the configuration of an AppleTalk I/O port.

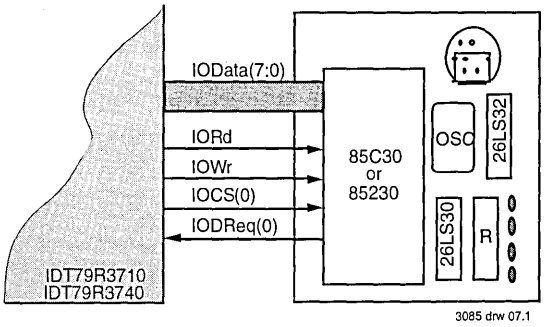


Figure 2.8: DMA-Supported AppleTalk I/O Port

Programmable Timer/Counter

The general purpose timer/counter can be programmed to function as a timer or as a counter. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will start the counter if the Enable bit is active. As a timer on terminal count, it will cause an interrupt, reload with the value stored in the Timer/Counter Value register and continue to count.

The Timer/Counter counting is enabled or disabled by the enable bit. The value *n* should be written to the Counter in order to count to *n* clocks. At reset, the counter is disabled.

I/O Bus

The R3710 and R3740 support two 8-bit (IOCS[1:0]*) and two 16-bit (IOGPμCS[1:0]*) external I/O channels that share the IODATA[15:0] pins. The two 8-bit I/O channels and the first 16-bit I/O channel (IOGPCS[0]*) each has a 16 Mbyte address space. The second 16 bit I/O channel (IOGPCS[1]*) has a 256 Mbyte address space.

Timing of the control signals to an I/O channel is programmable. The user can specify the length of IORD* and IOWR* signals. The IOCS[1:0]*, IOGPCS[1:0]* or DMAACK[1:0]* are asserted one cycle before the IORD* or IOWR* signals become active, and remain active for one cycle after IORD* or IOWR* are dasserted. RDCEN* and ACK* will be asserted by the R3710 or R3740 to end a processor (or TDTACK* to end a Typhoon) I/O cycle.

Figure 2.10 shows the configuration of the general purpose I/O device interface.

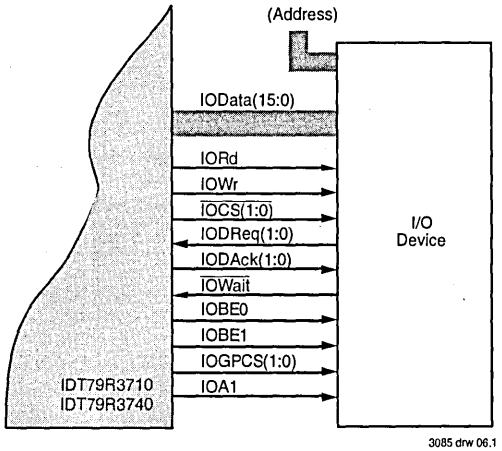


Figure 2.10: General Purpose I/O Device Interface

8-bit I/O Channels

The R3710 and R3740 support processor byte accesses (reads and writes) to devices located on the two 8 bit I/O channels. These accesses can be made using any of the four bytes on the 32 bit data bus. The R3710 or R3740 will transfer the correct byte (according to the 4 Byte Enables) to the 8 bit I/O bus (IODATA[7:0]).

The I/O channel unit on the R3710 and R3740 operates as a DMA controller with the two 8 bit I/O channels. DMA operations between I/O devices and the DRAM are supported. Eight bit data is packed or unpacked during DMA access into a 32 bit register for I/O DMA read or write respectively.

DMA Operations

Processor requests have priority over DMA requests. The priority for DMA operations is round robin for the Centronics and the two external 8-bit DMA engines. DMAREQ[1:0]* can be masked by writing '0' to the enable bit of the channel. A channel will not participate in the arbitration if the channel is disabled or if the I/O BIU (Bus Interface Unit) is owned by another channel.

The I/O BIU is emptied into memory in a DMA read access under the following conditions: 1) if the I/O BIU is full, or 2) if there is no DMA request (DMAREQ[1:0]) from the channel which owns the I/O BIU for a time out period, or 3) the byte count reaches zero.

In the write direction if the DMAREQ* from the channel that owns the I/O BIU is not active for a time out period, and the I/O BIU is not empty, arbitration will resume on the I/O bus. The time out period is set to 32 clocks. The clock period value cannot be changed, only enabled or disabled.

16-bit I/O Channels

The R3710 and R3740 support processor and Typhoon accesses (reads and writes) to devices located on the two 16-bit I/O channels.

For 16-bit devices, the CPU can read or write to any byte or half word. Processor or Typhoon access to the 16-bit I/O channels with any combination of byte enables active, will be performed in two consecutive I/O cycles in case of 3 or 4 byte accesses. In the two cycles, data will be packed or unpacked from a 32-bit register for an I/O read or write respectively. Conversion between big and little endian is supported for 16-bit devices.

The following signals support Canon type engines: *a)* Engine Strobe (ESTROBE*) - Clocks data into the engine control register from IODATA[15:0] to be driven to the engine and *b)* Engine Output Enable (EOE*) - drives the engine status to the IODATA[15:0].

Centronics IEEE 1284 Communication

IDT's Centronics implementation meets the IEEE 1284 definition of a compliant device. It supports the following modes: Compatible, Nibble, Byte, ECP and EPP, as well as the negotiation necessary for transition between different modes. Support for the Compatible mode includes the following three variations: Standard, IBM Epson, and Classic.

NOTE: This data sheet does not include a complete discussion of the IEEE 1284 bi-directional Centronics standard. IDT urges designers to review the IEEE1284 Rev. 2 specification.

There are two ways to handle the Centronics protocol. In the first option, data is transferred in DMA fashion and is only applicable in the Compatible, ECP, and EPP modes. The second option is interrupt driven, and applies to all modes. That is, Byte and Nibble modes are only interrupt driven.

There is support for special character detection in the Centronics incoming data. Control data characters like ^C or ^T can be detected and the CPU will be interrupted.

Figure 2.11 shows the configuration of the IEEE P1284 bidirectional centronics I/O port.

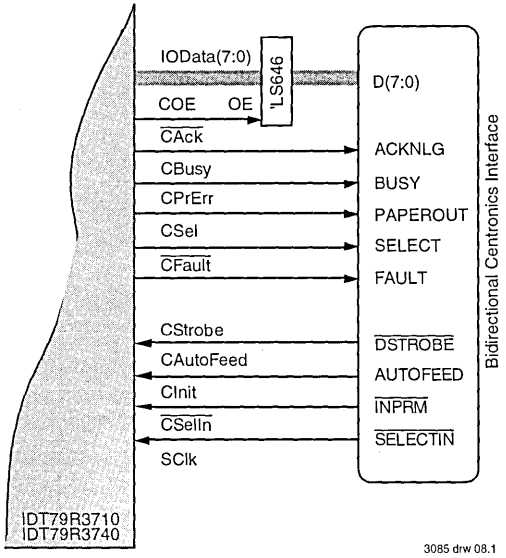


Figure 2.11: IEEE P1284 Bidirectional Centronics I/O Port

Centronics Interrupts

There are 7 interrupts related to the AMB:

1) LineInt - active when the last word of the line was read from the output FIFO.

2) BandInt - active when the last word of the last line was read from the output FIFO.

3) PageInt - active when PAGESYNC* is active.

4) ComDMAInt - active when the last word of the band was written to the DRAM by the DMA write engine.

5) ComErrInt - active when the DMA write engine has filled the given space in the dram and did not reach the last word of the band.

6) DecDMAInt - when the data goes directly to the engine (Print = 0 or Bypass = 0 in the Status register), DecDMAInt is active when the last word of the band was written to the input FIFO. When the data goes to memory, DecDMAInt is active when the last word of the band was written to the DRAM by the DMA write engine.

7) DecErrInt - when the data goes to memory, DecErrInt is active when the dma write engine has filled the given space in the DRAM and did not reach the last word of the band.

Negotiation

The R3710 or R3740 defaults after reset to Compatible mode. The negotiation phase starts when the host sets CSELECTIN* HIGH and CAUTOFD* LOW. The R3710 or R3740 interrupts the CPU by asserting the CentWrInt interrupt. The CPU interrupt routine includes reading the extensibility request value from the Centronics External register, and writing to the Centronics Control register to specify the supported mode. Note that the interpretation of the CenRdInt and CentWrInt interrupts, and the interrupt handler response, will be different in each mode.

Table 2.11 on the next page summarizes the values of host requests and the CPU interrupt routine response.

Compatible Mode

The CPU needs to configure the Compatible mode to one of the three supported modes: IBM, Classic or Standard, and to a data transfer option (DMA or interrupt per byte). Setting the modes and options is done by writing to the mode register (values are specified in the Centronics Mode register table).

In the interrupt per byte mode, the CPU will read data from the Centronics External register every time it responds to the CentRdInt interrupt. In DMA mode the CPU will initialize the DMA registers (addresses 1d0000a0, 1d000080 & 1d00098) before starting the DMA operation. The R3710 or R3740 will assert interrupt CentDMAInt when the DMA counter will reach terminal count.

A host request to return to Compatible mode from any of the other modes is indicated to the CPU by the assertion of the CentRstInt interrupt.

Nibble Mode

The R3710 or R3740 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to the Nibble data register. The R3710 or R3740 sends the byte to the host over the control lines in two consecutive nibble transactions.

Byte Mode

The R3710 or R3740 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to Centronics External register.

Extensibility Link

Assertion of CentWrInt interrupt while in Compatible. mode indicates to the CPU an extensibility request. The CPU will read from the Centronics External register the extensibility request value, and write to the control register the next mode and proper response.

ECP Mode

DMA and interrupt per byte options are supported for the ECP mode.

In the interrupt per byte option, the R3710 or R3740 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt.

In reverse transfer, in response to CentWrInt*, the CPU must first write to the Centronics status register (to the Busy bit). This indicates whether the CPU sends a command or data byte, and then write the data to the Centronics External register.

In forward transfer, in response to CentRdInt the CPU needs to read from the Centronics host register (Autofeed bit) to know whether the host is sending data or command, and then read the data from the Centronics register.

NOTE: RLE compression is supported only in interrupt per byte mode.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA. CentWrInt* will be asserted when the host requests data and the DmaDir bit in the Mode register indicates a read direction (From the IEEE1284 port to memory). CentRdInt will be asserted when the host sends data and the DmaDir bit indicates a write direction or when the host sends a command byte.

EPP Mode

DMA and interrupt per byte options are supported for the EPP mode, as follows:

In the interrupt per byte option, the R3710 or R3740 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt. It will distinguish between data and address by the contents of the strobe Selectin and AutoFd bits in the host buffer.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA.

CentWrInt will be asserted: 1) when the host requests data, and the DmaDir bit in the Mode register indicates a read direction (from the Centronics port to memory), or 2) when the host asks for an address byte.

CentRdInt will be asserted: 1) when the host sends data and the DmaDir bit indicates a write direction, or 2) when the host sends an address byte.

CPU Control

Request mode	Request value	Interrupt response: Mode-supported value	Interrupt response: Mode-not-supported value
Extensibility link first byte	1000 0000 xxxx xxxx	1110 1xxx	0111 0110
EPP	0100 0000	1100	0111
ECP with RLE	0011 0000	1011	0111
ECP	0001 0000	1011	0111
Device ID: -Nibble -Byte -ECP with RLE -ECP without RLE	 0000 0100 0000 0101 0001 0100 0011 0100	 1001 1010 1011 1011	 0111 0111 0111 0111
Byte	0000 0001	1010	0111
Nibble	0000 0000	0001	1111

Table 2.11: Interrupt Responses During Negotiation Phase

This mode enables the CPU to set the values of the Centronics status register, and communicate with the host in compatible mode.

Character Detection.

The value of the three CentDetect 8-bit registers is constantly compared to the Centronics incoming data. When a match occurs the CPU is interrupted. Characters as ^C or ^T can be detected during Centronics DMA operations and the CPU can respond without the need to wait to the end of the DMA operation.

Programmable Timing

To allow for higher than specified (by the IEEE1284 standard) data rates, the minimum delay can be programmed to values lower than the minimum required by this standard.

R3710 Video Controller/Interface

The R3710 moves the video data from the frame buffer memory to the printer engine. The data is moved by the DMA controller into an internal FIFO (four entries deep, 32 bit wide), serialized and driven to the engine. The video is a serial stream (one bit wide) of digital data. For a Canon-type printer interface, where the video clock is synchronized by the controller, there is a phase lock loop (PLL) on the R3710. The PLL synchronizes the video data to the LINESYNC*. For engines that supply an already-synchronized video clock there is a PLL bypass option. When the PLL option is selected, the input clock (VCLKIN) for the video must be eight times the desired synchronized video clock rate.

The R3710 can shift data in two directions to support duplex printing. Vertical and horizontal page margins are supported. The vertical skip counter sets the vertical margin of the page (how many lines to skip before starting to output video). The horizontal skip counter sets the horizontal page margin (how many dots to skip from the beginning of each line before starting to print). The vertical skip counter starts counting on PAGESYNC*, and decreases every LINESYNC*. The horizontal counter is loaded and starts counting on LINESYNC* and decrements every video clock. After finishing the skip time, the actual data is shifted out. Load *n-1* into the VerSkip or HorSkip fields of the Video Configuration register in order to skip *n* lines or pixels, respectively. The DMA has shadow registers, for the address and for the count.

The R3710 supports inverse printing. If an inverse video image from the frame buffer is to be printed, write 1 to the InvVid field of the Video Configuration Register.

In addition, the R3710 supports duplex printing (printing on both sides of the page). This is supported by enabling the video DMA address to count up or down, as set in the CntDir field of the Video Control register, and by configuring the video data shift direction in the VidDir field of the Video Configuration register. All 4 combinations of these 2 fields are allowed to provide flexibility.

Working with the Video Controller should be viewed as working with 2 independent state machines that work in parallel and are synchronized by the 4-entry deep video FIFO. One state machine is the DMA, that brings data from the frame buffer in the DRAM into the video FIFO. The second state machine is the Video Controller itself, which takes the data FIFO into a shift register and shifts it out to the printer's engine. In addition, the Video Controller is responsible for the synchronization with the printer's engine(PAGESYNC* and LINESYNC* signals), including the horizontal and vertical margin generation.

An example of how to use the Video Controller is found in the Applications section.

There are 4 interrupts related to the video:

- LineInt - Active when the last word of the line was read from the Engine DMA FIFO. It does not indicate that the last pixel of the line was output from the R3710. To set a new number of words in a line, the CPU should write to the Line Word Counter (1d0000c4) after the interrupt.
- BandInt - Active when the last word of the last line was read from the Engine DMA FIFO. It does not indicate that the last pixel of the line was output from the R3710. To set a new number of lines in a band, the CPU should write to the band line counter (1d0000c8) after the interrupt. For a blank band, the CPU should activate the blank bit in the Engine Scan register after the interrupt. There are no DMA cycles for a blank band, thus the DMA for the next band can start while the blank band is being printed.
- EngDMAInt - Active when the last word of the band was written to the Engine DMA FIFO. The next band DMA can start while video is working. If the DMAEn bit in the Engine Scan register is active, the EngDMAInt causes an automatic load of the DMA words counter and address counter; which starts a new DMA cycle.
- PageInt - Active after a falling edge of PAGESYNC*.

The following restrictions should be followed:

- RESET* width should be longer then 5 VCLK cycles. (VCLK is equal to VCLKIN when the PLL bypass is used or VCLKIN / 8 when the PLL is used).
- VCLK frequency should be less than 85% of SYSCLK frequency.
- VCLKIN frequency should be equal or less than 80 MHz.
- PAGESYNC* and LINESYNC* width should be longer than VCLK width.
- The number of pixels per line must be a multiple of 32; padding with 0's must be done if necessary.

6

R3740 Video Controller/Interface: Compressor/Decompressor Engines

The compressor and decompressor state machines in the R3740 implement both the lossless and alternative compression algorithms used by Adobe's Memory Booster (AMB) technology.

Both the compressor and decompressor operate as master DMA devices, using four separate DMA channels provided by the processor interface logic. The compressor and decompressor can operate simultaneously, compressing and decompressing data from one memory location to another. This simultaneous operation insures that the highest engine pages rates can be achieved, since one page of rasterized data can be decompressed while the next one is being compressed.

In addition, the decompressor is capable of decompressing a data stream from memory directly to the engine through the video path. This avoids the need to first decompress rasterized data to memory, and then DMA it to video. This provides a mechanism for lowering the memory system bandwidth and allowing support of higher page rate engines.

In the case of contention for resources between the compression and decompression state machines, the decompressor has higher priority for DMA from memory, since the process of decompressing data to the engine is time critical.

The compressor and decompressor make use of internal SRAM arrays as working storage, to increase compression and decompression speeds.

Both the compressor and decompressor are controlled by a number of registers in the IDT79R3740, which enable the driver software to control the locations of the memory buffers which hold the data to be compressed or decompressed, the type of compression (lossless or alternative) to be done, and whether the decompressor is to output its data to memory or through the video path.

If there is sufficient memory available to avoid the need for compression, a "bypass" path exists to move data directly from memory to video, providing a standard video DMA service.

Figures 2.13.a and 2.13.b on the next page show the R3740 compressor and decompressor implementation.

AMB Interrupts

There are 7 interrupts related to the AMB:

1) LineInt - active when the last word of the line was read from the output FIFO.

2) BandInt - active when the last word of the last line was read from the output FIFO.

3) PageInt - active when PAGESYNC* is active.

4) ComDMAInt - active when the last word of the band was written to the DRAM by the DMA write engine.

5) ComErrInt - active when the DMA write engine has filled the given space in the dram and did not reach the last word of the band.

6) DecDMAInt - when the data goes directly to the engine (Print = 0 or Bypass = 0 in the Status register), DecDMAInt is active when the last word of the band was written to the input FIFO. When the data goes to memory, DecDMAInt is active when the last word of the band was written to the DRAM by the DMA write engine.

7) DecErrInt - when the data goes to memory, DecErrInt is active when the dma write engine has filled the given space in the DRAM and did not reach the last word of the band.

DMA Controller

The monochrome AMB has four independent DMA channels, two for the compressor and two for the decompressor. Each DMA channel has a four entry deep 32 bit-wide FIFO, and burst transfer capability.

The DMA controller assumes that each DMA transfer moves a band of data. Shadow DMA registers are used when compressed data is being decompressed directly to the printer engine. This feature can be used in order to DMA the next band's compressed data while the decompressor is decompressing the current band. (See figures 2.13.a and 2.13.b. on the next page.)

Video Controller

The AMB moves the video data from the frame buffer memory to the printer engine. The video is a serial stream (1-bit wide) of digital data. The data is moved by the DMA controller to the video FIFO through one of three options: through the lossless decompressor; through the alternative decompressor; or directly. The data from the FIFO is then serialized and shifted to the engine.

For a Canon type printer where the video clock is generated by the controller there is a phase lock loop (PLL) to synchronizes the video data to the LINESYNC* input signal. For engines that supply the video clock to the controller there is a PLL bypass option. When the PLL option is selected the input clock for the video has to be multiplied by 8. Video data can be shifted in two directions (VidDir field of the Video Configuration register) and DMA address counters can count up or down, to support duplex printing (printing on both sides of the page).

Vertical and horizontal page margins are supported. The vertical skip counter sets the page vertical margin (how many lines to skip before starting to output video). The horizontal skip counter sets the horizontal page margin (how many dots to skip from the beginning of each line before starting to print). The vertical skip counter

starts counting on PAGESYNC*, and decreases every LINESYNC*. The horizontal counter is loaded and starts counting on LINESYNC* and decrements every video clock. After finishing the skip count, the actual data is shifted out.

The R3740 supports inverse printing for engines that use the opposite signal level to represent a black dot.

The Video Controller is responsible for synchronization with the printer's engine (PAGESYNC* and LINESYNC* signals).

The following restrictions should be followed:

- RESET* width should be longer then 5 VCLK cycles. (VCLK is equal to VCLKIN when the PLL bypass is used or VCLKIN / 8 when the PLL is used).
- VCLK frequency should be less than SYSCLK frequency and not more then 33MHz.
- VCLKIN frequency should be equal or less than 80 MHz.
- PAGESYNC* and LINESYNC* width should be longer than VCLK width.
- The number of pixels per line must be a multiple of 32; padding with 0's must be done if necessary.

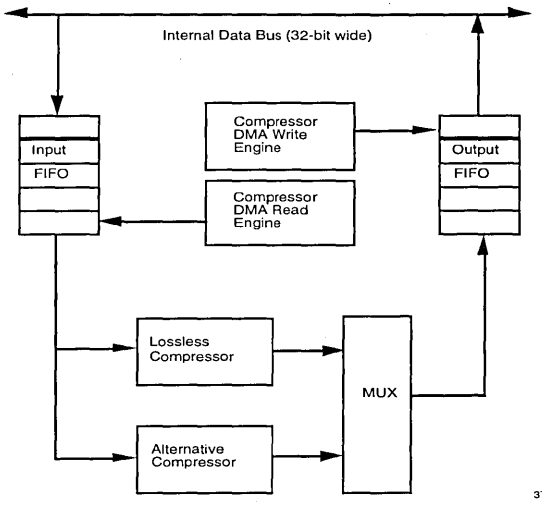


Figure 2.13.b: Compressor Block Diagram

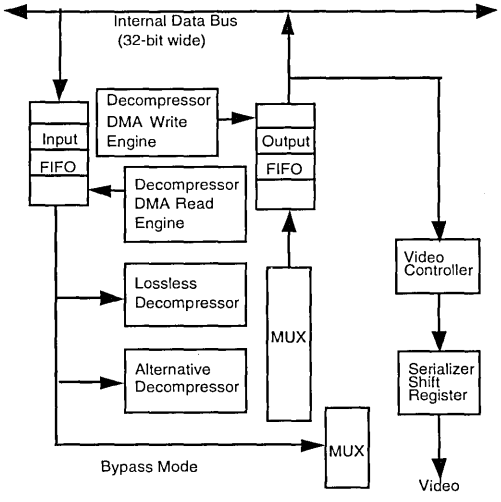


Figure 2.13.a: Decompressor Block Diagram

R3740 UART Serial Interface

The UART is an asynchronous communication element fully compatible with the PC industry standard 16550. The UART includes two 16-byte FIFOs, one for transmitted data and one for received data. This double buffering considerably reduces CPU interrupts, and can be activated by placing the UART in the FIFO mode.

The UART includes modem control signals DSR, DTR, RI, and DCD. It also incorporates programmable serial interface characteristics, like characters/bit (5,6,7, or 8); parity generation and detection (even, odd, or none); stop bit generation (1, 1.5, or 2); baud rate generation (DC to 56K baud

The UART offers independent control of transmit, receive, line status, data set interrupts, and FIFO usage. It also offers full status reporting capabilities.

The UART performs serial to parallel conversion of data characters received from peripheral devices or modems, and parallel to serial conversion on data characters transmitted by the CPU. When FIFO mode is enabled, 16-bytes of information are buffered on-chip both for reception and transmission; the receive FIFO also provides 3-bits per byte of error status.

The complete status of the UART can be read by the CPU at any time during operation. The information obtained includes the type and condition of the transfer operations being performed, and error conditions involving parity, overrun, framing, and break interrupt. The programmable baud rate generator divides the timing reference clock input by a programmable divisor.

The UART pins and registers are specified in the pin assignment and the register tables, respectively. Please refer to VLSI Technology's VL16C550 document for a more detailed functional description.

Figure 2.14 shows the implementation of the UART serial interface.

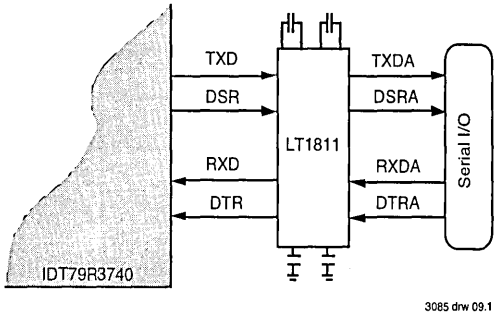


Figure 2.14: UART Serial Interface Implementation

DC ELECTRICAL SPECIFICATIONS—R3710

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+ 0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		200	mA	VDD = 5V, Ta=25C
CINCLK	CLK Input Capacitance		11	pF	
CIN	Input Capacitance		5	pF	

DC ELECTRICAL SPECIFICATIONS—R3740

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+ 0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		300	mA	VDD = 5V, Ta=25C
CINCLK	CLK Input Capacitance		6	pF	
CIN	Input Capacitance		6	pF	

AC TIMING CHARACTERISTICS—R3710

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Signals	Description	Min	Max	Unit
t1	SYSCLK	Pulse Width High	12		ns
t2	SYSCLK	Pulse Width Low	12		ns
t3	SYSCLK	Clock period	30		ns
t4	RESET*	Pulse Width from VDD Valid	200		us
t5	RESET*	Minimum Pulse Width	40		VCLKIN
t6	BUSREQ*, ACK*, RDCEN*	Valid from SYSCLK rising	2	17	ns
t7	A/D[31:0], OEMAD*, TADOE*	Valid from SYSCLK falling	2	15	ns
t8	A/D[31:0], ADDR[3:2], WR*, PIO[5:0], TAS*, TDS*, TDTACK*	Driven from SYSCLK rising	0	20	ns
t9	A/D[31:0]	Tri-state from SYSCLK rising	0	15	ns
t10	A/D[31:0]	Set-up to SYSCLK falling	6		ns
t11	A/D[31:0]	Set-up to ALE falling	7		ns
t12	ALE	Set-up to SYSCLK falling	7		ns
t13	BURST*, RD*, DATAEN*, WR*, ADDR[3:2], BUSGNT*	Set-up to SYSCLK rising	10		ns
t14	ALE, BURST*, RD*, DATAEN*, INT*, PIO[5:0], IODATA[15:0], TAS*, TDS*, TDTACK*	Tri-state from SYSCLK rising	0	20	ns
t15	ALE, BURST*, RD*, DATAEN*, PIO[5:0]	Driven from SYSCLK rising	0	20	ns
t16	ALE, BURST*, RD*, DATAEN*, IOGPCS*, ROMCS*[2:0], IORD*, IOWR*, ROMOE*, IOA1, IOBE*[1:0], INT*, DMAACK*[1:0], PIO[5:0], ADDR[3:2], WR*, TAS*, TDS*, TDTACK*, TCS*, TBGNT*, TAACK*	Valid from SYSCLK rising	3	15	ns
t17	ADDR[3:2], WR*	Tri-state from SYSCLK rising	2	20	ns
t18	DADR[10:0]	Valid from AD address valid	6	25	ns
t19	DADR[10:0]	Valid from SYSCLK rising	3	27	ns
t20	RAS*[2:0], DWR*	Valid from SYSCLK rising	2	17	ns
t21	CAS*[3:0]	SYSCLK rising to CAS* LOW	2	13	ns
t22	CAS*[3:0]	SYSCLK falling to CAS* HIGH	2	13	ns
t23	IODATA[15:0]	Hold from IOWR* rising	15		ns
t24	IODATA[15:0]	Set-up to SYSCLK rising	9		ns
t25	IODATA[15:0]	Driven from SYSCLK rising	0	15	ns
t26	IOWAIT*	Set-up to SYSCLK rising	18		ns
t27	DMAREQ*[1:0], PIO[5:0], LINESYNC*, PAGESYNC*	Asynchronous Inputs		Asynch	
t28	VCLKIN	Pulse Width High	5		ns
t29	VCLKIN	Pulse Width Low	5		ns
t30	VCLKIN(1)	Clock period	12.5		ns
t31	TEST, TBREQ*	Setup to SYSCLK rising	8		ns
t32	TAS*, TDS*, TDTACK*	Setup to SYSCLK rising	13		ns
t33	TADDIR*, TATOE*	Valid from SYSCLK rising	2	20	ns

AC TIMING CHARACTERISTICS—R3740

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Signals	Description	Min	Max	Unit
t1	SYSCLK	Pulse Width High	17		ns
t2	SYSCLK	Pulse Width Low	17		ns
t3	SYSCLK	Clock period	40		ns
t4	RESET*	Pulse Width from VDD Valid	200		us
t5	RESET*	Minimum Pulse Width	40		VCLKIN
t6	BUSREQ*, ACK*, RDCEN*	Valid from SYSCLK rising	4	20	ns
t7	A/D[31:0], OEMAD*, TADOE*	Valid from SYSCLK falling	2	15	ns
t8	A/D[31:0], ADDR[3:2], WR*, PIO[5:0], TAS*, TDS*, TDTACK*	Driven from SYSCLK rising	0	30	ns
t9	A/D[31:0]	Tri-state from SYSCLK rising	0	20	ns
t10	A/D[31:0]	Set-up to SYSCLK falling	6		ns
t11	A/D[31:0]	Set-up to ALE falling	7		ns
t12	ALE	Set-up to SYSCLK falling	7		ns
t13	BURST*, RD*, DATAEN*, WR*, ADDR[3:2], BUSGNT*	Set-up to SYSCLK rising	16		ns
t14	ALE, BURST*, RD*, DATAEN*, INT*, PIO[5:0], IODATA[15:0], TAS*, TDS*, TDTACK*	Tri-state from SYSCLK rising	0	30	ns
t15	ALE, BURST*, RD*, DATAEN*, PIO[5:0]	Driven from SYSCLK rising	0	30	ns
t16	ALE, BURST*, RD*, DATAEN*, IOGPCS*, ROMCS*[2:0], IORD*, IOWR*, ROMOE*, IOA1, IOBE*[1:0], INT*, DMAACK*[1:0], PIO[5:0], ADDR[3:2], WR*, TAS*, TDS*, TDTACK*, TCS*, TBGNT*, TAACK*	Valid from SYSCLK rising	4	20	ns
t17	ADDR[3:2], WR*	Tri-state from SYSCLK rising	4	30	ns
t18	DADR[10:0]	Valid from AD address valid	6	28	ns
t19	DADR[10:0]	Valid from SYSCLK rising	5	36	ns
t20	RAS*[2:0], DWR*	Valid from SYSCLK rising	4	19	ns
t21	CAS*[3:0]	SYSCLK rising to CAS* LOW	4	18	ns
t22	CAS*[3:0]	SYSCLK falling to CAS* HIGH	4	18	ns
t23	IODATA[15:0]	Hold from IOWR* rising	15		ns
t24	IODATA[15:0]	Set-up to SYSCLK rising	14		ns
t25	IODATA[15:0]	Driven from SYSCLK rising	0	15	ns
t26	IOWAIT*	Set-up to SYSCLK rising	18		ns
t27	DMAREQ*[1:0], PIO[5:0], LINESYNC*, PAGESYNC*, DSR, rxd	Asynchronous Inputs		Asynch	
t28	VCLKIN	Pulse Width High	5		ns
t29	VCLKIN	Pulse Width Low	5		ns
t30	VCLKIN[1]	Clock period	12.5		ns
t31	TEST, TBREQ*	Setup to SYSCLK rising	8		ns
t32	TAS*, TDS*, TDTACK*	Setup to SYSCLK rising	13		ns
t33	TADDIR*, TATOE*	Valid from SYSCLK rising	5	30	ns
t34	txd, DTR	Asynchronous outputs			

NOTE:

[1] Internal VCLK frequency (divided or not) should be lower than 85% of SYSCLK frequency. Valid only in the SYSCLK during which IODATA is sampled.

PIN INFORMATION

Logic Symbols

Signals marked with an asterisk are active when low. Dashed arrows in figure 1.2 indicate MUX'ed signals.

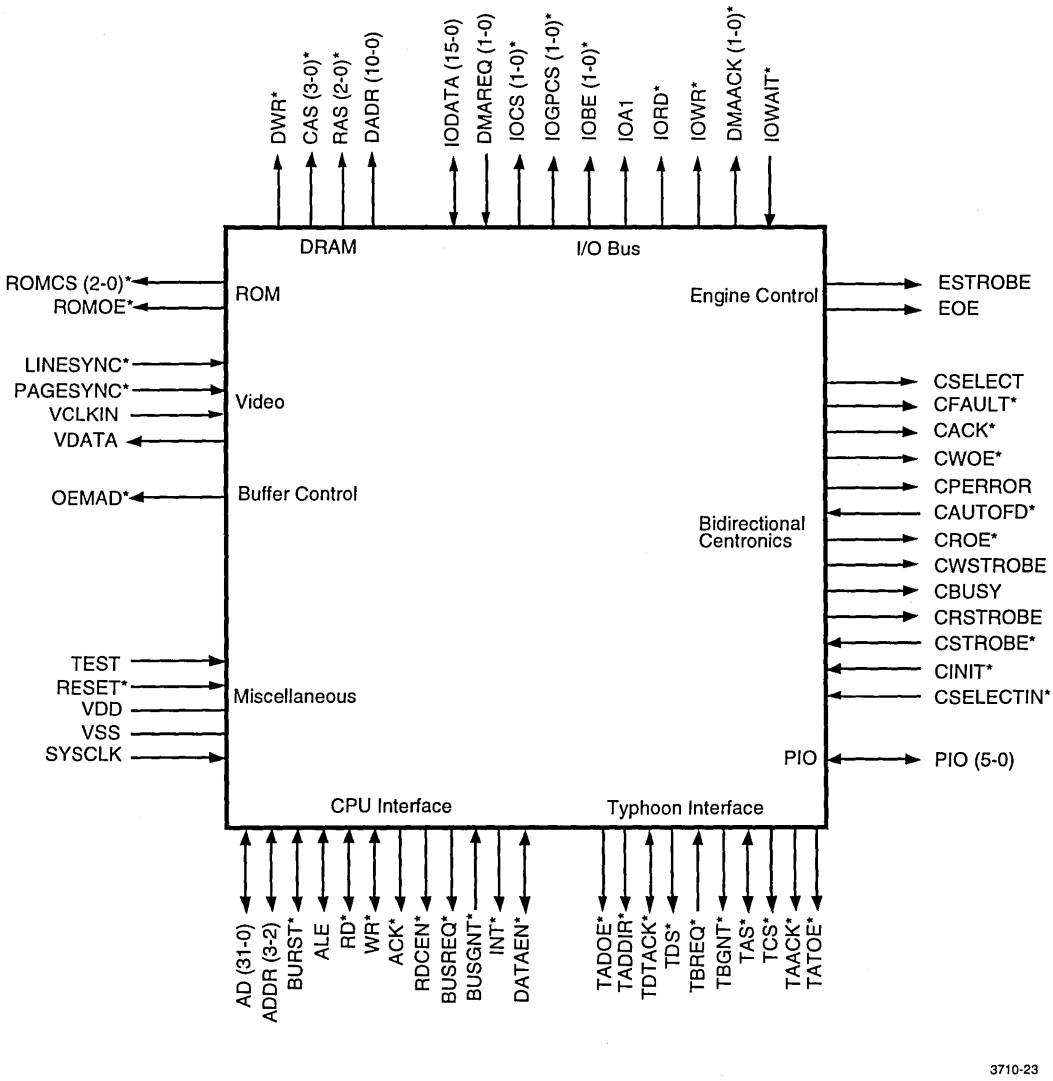


Fig. 1.1: Logic Symbol for R3710

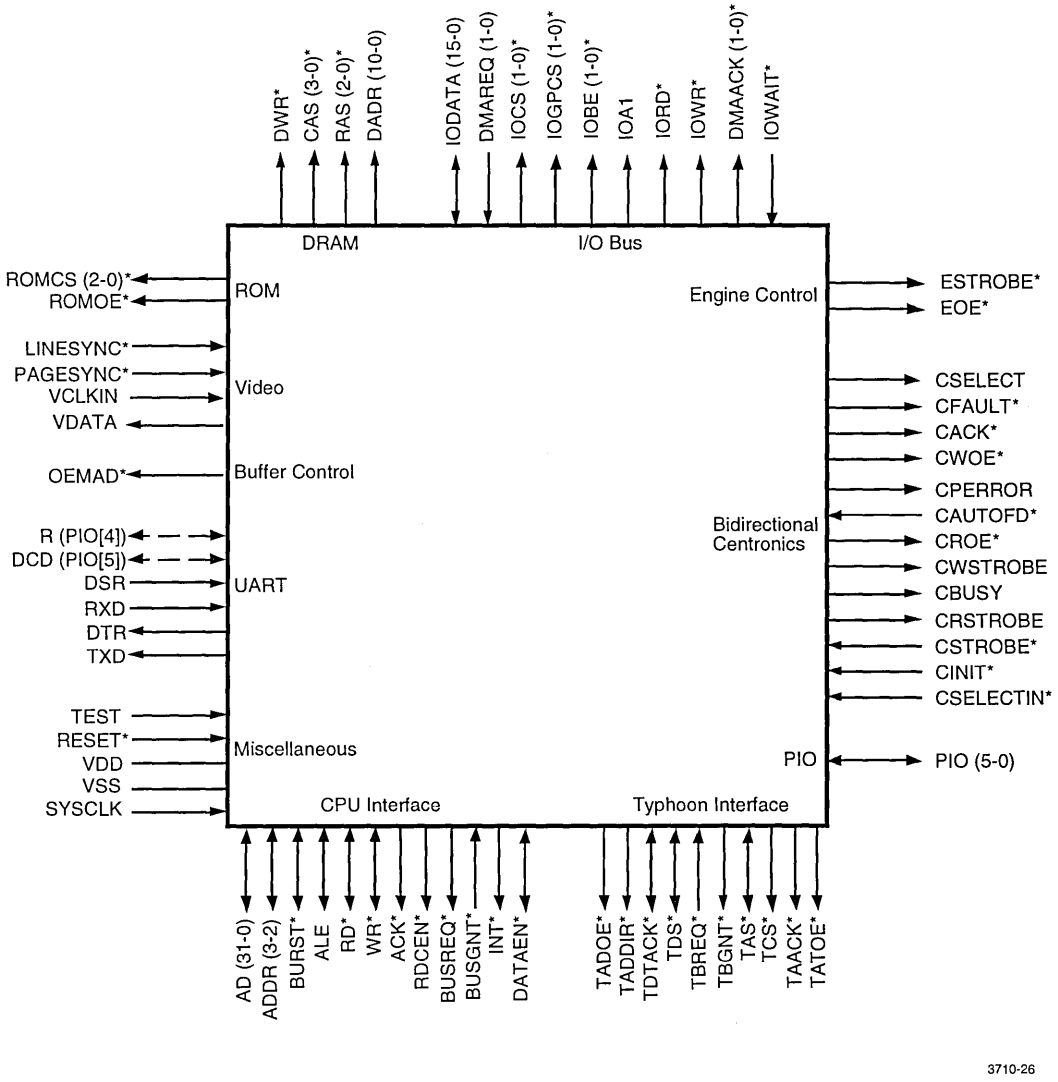


Fig. 1.2: Logic Symbol for R3740

Pin Assignment Table

Pins identified with an asterisk are active when low.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CPU Interface				
A/D[31:0]	P.U. (R3710 only)	I/O	R3710: 8mA R3740: 4mA	**Address/Data:** Multiplexed address and data bus. In the Address phase: A/D[31:4] are address, A/D[3:0] are Byte Enable[3:0]. During Typhoon Master cycles, A/D[3:2] contain address bits 3 and 2, and not Byte Enables. In the Data phase: Data[31:0]
ADDR[3:2]	P.U. (R3710 only)	I/O	4mA	**Non Multiplexed Address:** Connected to the CPU ADDR[3:2]. In DMA cycles the R3710 or R3740 drives these lines.
BURST*	P.U. (R3710 only)	I/O	2mA	**Burst Transfer:** Used only during read cycles, the BURST* signal indicates that the current bus read is requesting a block of four contiguous words from memory. The pin connects to the CPU's BURST/WRNEAR* signal. In DMA cycles the R3710 or R3740 drives this signal HIGH.
ALE	P.D. (R3710 only)	I/O	R3710: 4mA R3740: 2mA	**Address Latch Enable:** Used by the CPU to indicate that the A/D bus contains valid address information for the bus transaction. During Typhoon DMA cycles, the R3710 or R3740 asserts ALE to capture the address supplied by the Typhoon.
SYSCLK		I		**System Clock:** Connected directly to the CPU SYSCLK* output.
RD*	P.U. (R3710 only)	I/O	2mA	**Read:** Indicates a read access by the CPU. In DMA cycles the R3710 or R3740 drives the signal HIGH.
WR*	P.U. (R3710 only)	I/O	2mA	**Write:** Indicates a write access by the CPU or the Typhoon. In a non-Typhoon DMA cycle the R3710 or R3740 drives this signal HIGH. Its negation indicates a read access by the Typhoon (during Typhoon DMA).
ACK*		O	2mA	**Acknowledge:** Indicates to the CPU that the memory system has sufficiently processed the bus transaction i.e. that the CPU may either terminate a write cycle or process read data.
RDCEN*		O	2mA	**Read Buffer Clock Enable:** Indicates to the CPU that there is valid data on the A/D bus. Used during read cycles only.
BUSREQ*		O	2mA	**Bus Request:** The R3710 or R3740 requests the CPU bus which is required for: Video, I/O and Typhoon DMA's.
BUSGNT*		I		**Bus Grant:** Indicates that the CPU has relinquished the bus.
INT*		O	2mA	**Interrupt:** "OR's" the internal and external interrupt sources.
DATAEN*		I/O	4mA	**Data Enable:** indicates the data phase in CPU read cycles. In DMA the R3710 or R3740 asserts DATAEN* when the ROM/DRAM drives data onto A/D[31:0].

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
ROM				
ROMCS*[2:0]		O	4mA	**ROM Chip Select:** Select one of the 3 ROM banks. They can be connected to the ROM's Chip Select or Output Enable. ROMCS[2]* is connected to the boot ROM, with starting physical address 0x1fc00000.
ROMOE*		O	4mA	**ROM Output Enable:** Asserted when there is an access to any of the ROM banks. Used to output- enable the ROM data in systems where there is a buffer between ROM and DRAM data bus; eg. when using an interleaved ROM configuration.
DRAM				
DADR[10:0]		O	8ma	**DRAM Address:** Multiplexed row and column address connected to the DRAM address.
RAS[2:0]*		O	R3710: 4mA R3740: 12mA	**Row Adress Select:** Directly connected, on a bank basis, with the RAS* inputs of the DRAMs. Supports up to three banks of DRAMs.
CAS[3:0]*		O	4mA	**Column Address Select:** Directly connected, on a byte basis (can be across banks), to the CAS* inputs of the DRAMs. Connects a CAS* to each of the four bytes in every bank.
DWR*		O	12mA	**DRAM Write:** Connects to the write pin of each of the DRAMs.
Typhoon Interface				
TBREQ*	P.U.	I		**Typhoon Bus Request:** A Typhoon bus request to make a system resource access in master mode.
TBGNT*		O	2mA	**Typhoon Bus Grant:** The R3710 or R3740 asserts TBGNT* to grant the CPU bus to the Typhoon. Once the TBGNT* is asserted, it remains so until TBREQ* is deasserted.
TAS*	P.U. (R3710 only)	I/O	2mA	**Typhoon Address Strobe:** Master Mode (input) - the coprocessor indicates that it is driving valid data on the A/D bus. Slave mode (output) - the R3710 or R3740 indicates that it is driving valid data on the A/D bus
TDS*		R3710 only: O R3740 only: I/O	2mA	**Typhoon Data Strobe:** Master mode (input) - during Write indicates that there is valid data on the A/D bus. During Read indicates data phase. Slave mode (output) - the R3710 or R3740 drives TDS* to indicate that it is ready to accept data during reads or that valid data is available during write on the A/D bus.
TDTACK*	P.U. (R3710 only)	I/O	2mA	**Typhoon Data Acknowledge:** Master mode (output) - The R3710 or R3740 asserts TDTACK* to indicate that the system is receiving or driving the requested data to/from the A/D bus. Slave mode (input) - The Typhoon asserts TDTACK* to signal that it has supplied or received data on its bus.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
TAACK*		O	2mA	**Typhoon Address Acknowledge:** The R3710 or R3740 asserts TAACK* in the same clock that it asserts ALE for the Typhoon. This insures that the Typhoon continues driving the address until latched by the system.
TCS*		O	2mA	**Typhoon Chip Select:** When the CPU accesses the Typhoon, the R3710 or R3740 asserts TCS*. It is active one clock before R3710 or R3740 asserts TAS*.
TADOE*		O	4mA	**Typhoon A/D Output Enable:** The R3710 or R3740 asserts TADOE* when the Typhoon drives the address to the A/D bus, and in the data phases of the Typhoon.
TADDIR*		O	4mA	**Typhoon A/D Direction:** The R3710 or R3740 asserts TADDIR* (LOW) when the Typhoon drives the A/D bus.
TATOE*		O	4mA	**Typhoon Address To Output Enable:** The R3710 or R3740 asserts TATOE* in the address phase of cycles in which the CPU accesses the Typhoon.
Buffer Control				
OEMAD*		O	4mA	**Output Enable between Memory and A/D:** Output enable for the data path transceiver between the memory system (ROM and DRAM) and the A/D bus.
I/O Bus				
IODATA[15:0]	P.U. (R3710 only)	I/O	8mA	**Input/Output Device Data:** Bidirectional 16-bit I/O Data bus.
IORD*		O	R3710: 12mA R3740: 8 mA	**Input/Output Device Read:** Active during Read from an I/O device.
IOWR*		O	R3710: 12mA R3740: 8mA	**Input/Output Device Write:** Active during Write to an I/O device.
IOCS[1:0]*		O	R3710: 2mA R3740: 4mA	**Input/Output Device Chip Select:** Chip selects for 8 bit I/O channels 0 and 1.
IOGPCS[1:0]*		O	R3710: 2mA R3740: 4mA	**Input/ Output Device Chip Select:** Chip selects for 16 bit I/O channels 0 and 1.
DMAREQ[1:0]*	P.D. (R3710 only)	I		**DMA Request:** Requesting DMA service on 8-bit channels 0 and 1.
DMAACK[1:0]*		O	2mA	**DMA Acknowledge:** Indicating that DMA access is granted on 8-bit channels 0 and 1.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
IOA1		O	8mA	**Input/Output Device Address bit 1:** Provides a half word (16 bit) address on the I/O bus.
IOBE[1:0]*		O	R3710: 2mA	**Input/Output Device Byte Enable:** Indicates which byte data bus is valid on the 16 bit I/O bus.
			R3740: 4mA	IOBE[1]* corresponds to IODATA[15:8] and IOBE[0] corresponds to IODATA[7:0].
IOWAIT*	P.U.	I		**Input/Output Device Wait:** Indicates to the R3710 or R3740 that a transfer cycle on the I/O bus needs to be extended.
PIO[5:0]	P.U. (R3710 only)	I/O	8mA	**Programmable Input/Output:** Individually programmed pins for inputs, interrupt inputs or outputs.
Bidirectional Centronics				
CWOE*		O	2mA	**Centronics Write Output Enable:** Controls the Output Enable signal of the data register from the printer to the host.
CROE*		O	2mA	**Centronics Read Output Enable:** Controls the OE* of the Centronics external register in the direction from the host to the printer (the IODATA[7:0] bus).
CWSTROBE		O	2mA	**Centronics Write Strobe:** Clocks data from IODATA[7:0] into the Centronics register (from printer to host).
CRSTROBE		O	2mA	**Centronics Read Strobe:** Clocks data from the host into the Centronics register (from host to printer).
CSTROBE*	P.U.	I		**Centronics Strobe:** Host driven. Compatibility mode: Set active low to transfer data into peripheral device's input latch. Data is valid while signal is low. Negotiation phase: Set active low to transfer extensibility request value into peripheral device's input latch. Data is valid on the leading (falling) edge of HostClk (CSTROBE*). Reverse data transfer phase: Set high during Nibble Mode transfers to avoid latching data into peripheral device. Pulsed low during Byte Mode transfers to acknowledge transfer of data from the peripheral. The peripheral device shall ensure that this pulse does not transfer a new data byte into the peripheral's input latch. ECP mode: Used in a closed-loop handshake with PeriphAck (CBUSY) to transfer data or address information from the host to the peripheral device. EPP mode: Set low to denote an address or data write operation to the peripheral device. Set high to denote an address or data read operation from the peripheral device. For a more detailed description refer to section 4.1 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CACK*		O	2mA	**Centronics acknowledge:** Peripheral device driven. Compatibility mode: Pulsed low by the peripheral device to acknowledge transfer of a data byte from the host. Negotiation phase: Set low to acknowledge 1284 support, then set high to indicate that the Xflag (CSELECT) and data available flags may be read. Reverse data transfer phase: Used in both Nibble and Byte Modes to qualify data being sent to the host. Reverse idle phase: Set low then high by peripheral device to cause an interrupt indicating to host that data is available. ECP mode: Used in a closed-loop handshake with HostAck (CAUTOFD*) to transfer data from the peripheral device to the host. EPP mode: Used by the peripheral device to interrupt the host. This signal is active high and positive edge triggered. For a more detailed description refer to section 4.3 of the IEEE P1284 D2.00 specification.
CBUSY		O	2mA	**Centronics Busy:** Peripheral device driven. Compatibility mode: Driven high to indicate the peripheral device is not ready to receive data. Negotiation phase: Reflects the present state of the peripheral device's forward channel. Reverse data transfer phase: Nibble mode: Data bits 3 then 7, then forward channel busy status. Byte mode: Forward channel busy status. Reverse idle phase: Forward channel busy status. ECP mode: Used by peripheral for flow control in the forward direction. PeriphAck (CBUSY) also provides a ninth data bit used to determine whether command or data information is present on the data signals in the reverse direction. EPP mode: Driven inactive as a positive acknowledgment from the peripheral device that transfer of data or address os completed. Signal is active when low, and should be driven active as an indication that the device is ready for the next address or data transfer. For a more detailed description refer to section 4.4 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
CPERROR		O	2mA	**Centronics Printer Error:** Peripheral device driven. Compatibility mode: Driven high to indicate that the peripheral device has encountered an error in its paper path. Note that this signal's meaning varies among peripheral devices. Peripherals shall set nFault (CFAULT*) low whenever they set Perror (CPERROR) high. Negotiation phase: Set high to indicate 1284 support, then follows nDataAvail (CFAULT*). Reverse data transfer phase: Nibble mode: Data bits 2 then 6. Byte mode: Same as nDataAvail (CFAULT*). ECP mode: The peripheral drives this signal low to acknowledge nReverseRequest (CINIT*). The host relies upon nAckReverse (CPERROR) to determine when it is permitted to drive the data signals. EPP mode (User Defined 1): A manufacturer-specific signal. For a more detailed description refer to section 4.5 of the IEEE P1284 D2.00 specification.
CSELECT		O	2mA	**Centronics Select:** Peripheral device driven. Compatibility mode: Set high to indicate that the peripheral device is online. Negotiation phase: Used by peripheral device to reply to the requested extensibility byte sent by the host during the negotiation phase. Affirmative response is indicated with the signal high for all request values except for Nibble Mode Reverse Channel Transfer, which is indicated affirmative with the signal low. Reverse data transfer phase: Nibble mode: Data bits 1 then 5. Byte mode: Same as negotiation phase. Reverse idle phase: Same as negotiation phase. ECP mode: Same as negotiation phase. EPP mode (User Defined 3): A manufacturer-specific signal. For a more detailed description of this signal refer to section 4.6 of the IEEE P1284 D2.00 specification. For more details about the negotiation phase refer to section 6.4 of the same specification.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
CAUTOFD*	P.U.	I		**Centronics Autofeed:** Host driven. Compatibility mode: Interpretation varies among peripheral devices. Set low by host to put some printers into auto line feed mode. Also may be used as a 9th data, parity, or command/data control bit. Negotiation phase: Set low in conjunction with 1284 Active (CSELECTIN*) being set high to request a 1284 mode, then set high after peripheral device sets PtrClk (CACK*) low. Reverse data transfer phase: Nibble mode: Set low to indicate host can receive peripheral device to host data, then set high to acknowledge receipt of that nibble. Byte mode: Same as Nibble mode to request and acknowledge bytes. Following a reverse channel transfer, the interface transitions to idle phase when HostBusy (CAUTOFD*) is set low and peripheral device has no data available. Reverse idle phase: Set high in response to PtrClk (CACK*) low pulse to re-enter reverse data transfer phase. If set high with 1284 Active (CSELECTIN*) being set low, the 1284 idle phase is aborted and the interface returns to Compatibility mode. ECP mode: The host drives this signal for flow control in the reverse direction. It is used in an interlocked handshake with PeriphClk (CACK*). HostAck (CAUTOFD*) also provides a 9th data bit used to determine whether command or data information is present on the data signals in the forward direction. EPP mode: Used to denote a data cycle, and is active when low. For a more detailed description refer to section 4.7 of the IEEE P1284 D2.00 specification.
CINIT*	P.U.	I		**Centronics Initialize:** Host driven. Compatibility mode: Pulsed low in conjunction with 1284 Active (CSELECTIN*) low to reset the interface and force a return to Compatibility mode idle phase. Negotiation phase: Set high. Reverse data transfer phase: Set high. ECP mode: Driven low to place the channel in the reverse direction. While in this mode the peripheral is allowed to drive only the bidirectional data signals when nReverseRequest (CINIT*) is low and 1284 Active (CSELECTIN*) is high. EPP mode: When driven active (low), initiates a termination cycle that returns the interface to Compatibility mode. For a more detailed description refer to section 4.9 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
CFAULT*		O	2mA	**Centronics Fault:** Peripheral device driven. Compatibility mode: Set low by peripheral device to indicate that an error has occurred. The meaning of this signal varies among peripheral devices. Negotiation phase: Set high to acknowledge 1284 compatibility. In Nibble or Byte mode it is then set low to indicate peripheral device to host data is available following host setting HostBusy (CAUTOFD*) high. Reverse data transfer phase: Nibble mode: Set low to indicate that peripheral device has data ready to send to host, then used to send data bits 0, then 4. Byte mode: Used to indicate that data is available. ECP mode: In this mode the peripheral may drive this pin low to request communication with the host. The request is only a suggestion to the host, who has ultimate control over the transfer direction. Typically used to generate an interrupt to the host, also provides a mechanism for peer-to-peer communication. Signal is valid in both forward and reverse directions. EPP mode (User Defined 2): Manufacturer-specific signal. For a more detailed description refer to section 4.10 of the IEEE P1284 D2.00 specification.
CSELECTIN*	P.U.	I		**Centronics Select Input:** Host driven. Compatibility mode: Set low by host to select peripheral device. Negotiation phase: Set high in conjunction with HostBusy (CAUTOFD*) being set low to request a 1284 mode. Reverse data transfer phase: Set high to indicate that bus direction is peripheral device to host. Set low to terminate 1784 mode and set bus direction host to peripheral device. Reverse idle phase: Same as Reverse data transfer phase. ECP mode: Driven high by the host while in ECP mode. Set low by the host to terminate ECP mode and return the link to the Compatibility mode. EPP mode: Used to denote an address cycle, and is active low. For a more detailed description refer to section 4.11 of the IEEE P1284 D2.00 specification.
Engine Control				
ESTROBE*		O	2mA	**Engine Strobe:** Clocks data into the printer's engine register from IODATA[15:0]
EOE*		O	2mA	**Engine Output Enable:** When active (LOW), it drives the printer's engine status into IODATA[15:0]

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
Video Control				
VCLKIN	P.U.	I		**Video Clock In:** Used for generating the video clock VCLK which is the video data clock. The VCLKIN frequency is either VCLK*8 or VCLK.
VDATA		O	4mA	**Video Data:** to the printer.
LINESYNC*	P.U.	I		**Line Synchronization:** Input from the printer that indicates the beginning of a line. In some printers this is called Beam Detect (BD) or SYNCBD*.
PAGESYNC*	P.U.	I		**Page Synchronization:** Input from the printer that indicates the beginning of the page.
UART (R3740 only)				
PIO[4]/RI		I/O		**Programmable Input/Output or Ring Indicator:** As input, it can be alternatively used as a Ring Indicator for external modem or as a programmable I/O pin. In the modem option a change from LOW to HIGH will set a flag in the Modem Status Register and cause an interrupt.
PIO[5]/DCD		I/O		**Programmable Input/Output or Data Carrier Detect:** As input, it can be alternatively used as Data Carrier Detect for external modem or as a programmable I/O pin. In the modem option a change on the pin will set a flag in the Modem Status register and cause an interrupt.
DSR		I		**Data Set Ready:** Used to start the receiving of data on RXD. A change in the value of this input will set a flag in the Modem Status register and cause an interrupt.
RXD		I		**Serial Data Input:** Data input to the receiver.
DTR		O		**Data Terminal Ready:** A LOW indicates that the part is ready to receive data. This output is controlled by writing to the Modem Control register.
TXD		O		**Serial Data Output:** Data from the transmit register is shifted out via this pin.
Misc.				
TEST	P.D. (R3710 only)	I		**Master Output Enable:** When TEST is HIGH and RESET* is active, ALL the device outputs and I/Os are tri-stated (in a system, TEST should be pulled down to GND).
RESET*		I		**Reset:** Will reset the R3710 or R3740 to the initial state.
VDD				**+5V** (+/-5%)
VSS				**Ground**

NOTE:

[1] Pull Up/Pull Dn identifies pins with internal Pull Up (P.U.) or Pull Down (P.D.) resistors. The R3740 has internal P.U. resistors only for input pins, and no internal P.D. resistors. P.U./P.D. values are: For R3710, 35K-150Kohm depending on the process variation, and for R3740, 30Kohm maximum.

REGISTER MAPS AND TABLES

For the register maps and tables in this section, please note:

- Reads and Writes to and from the R3710 and R3740 internal registers should be word (32-bit) accesses.
- The 0x notations indicate hexadecimal values, as in notations for the C language.
- Bit 0 is the least significant bit.

Register Map—R3710

Description	Physical Address	Description	Physical Address
ROM Configuration	0x1d000000	DMA Centronics Count	0x1d000098
Video Configuration	0x1d000020	I/O Channel Timing	0x1d0000a0
PIO Value	0x1d000040	Video Control	0x1d0000c0
PIO Control	0x1d000044	Line Word Counter	0x1d0000c4
PIO Read Pins	0x1d00005c	Band Line Counter	0x1d0000c8
Timer/Counter Value	0x1d000048	Video DMA Address Counter	0x1d0000cc
Timer/Counter Control	0x1d00004c	Video DMA Word Counter	0x1d0000do
Interrupt Cause	0x1d000050	Centronics Status	0x1d000100
Interrupt Mask	0x1d000054	Centronics Control	0x1d000104
Interrupt Write	0x1d000060	Centronics Nibble Data	0x1d000108
Test	0x1d000064	Centronics Host	0x1d00010c
DRAM Control	0x1d000058	Centronics Mode	0x1d000110
DMA Address 0	0x1d000080	Centronics Minimum Delay	0x1d000114
DMA Address 1	0x1d000084	Centronics Data Detect 0	0x1d0000a4
DMA Centronics Address	0x1d000088	Centronics Data Detect 1	0x1d0000a8
DMA Count 0	0x1d000090	Centronics Data Detect 2	0x1d0000ac
DMA Count 1	0x1d000094		

Register Map—R3740

Description	Physical Address	Description	Physical Address
ROM Configuration	0x1d000000	Decode Source Address	0x1d0000cc
Video Configuration	0x1d000020	Decode Source Bytes	0x1d0000d0
PIO Value	0x1d000040	Upsample Line Counter	0x1d0000d4
PIO Control	0x1d000044	Upsample Band Counter	0x1d0000d8
PIO Read Pins	0x1d00005c	Encode Control	0x1d0000dc
Timer/Counter Value	0x1d000048	Encode Target Address	0x1d0000e0
Timer/Counter Control	0x1d00004c	Encode Target Bytes	0x1d0000e4
Interrupt Cause	0x1d000050	Encode Source Address	0x1d0000e8
Interrupt Mask	0x1d000054	Encode Source Bytes	0x1d0000ec
Interrupt Write	0x1d000060	Downsample Line Counter	0x1d0000f0
Test	0x1d000064	Status	0x1d0000f4
DRAM Control	0x1d000058	Line Word Counter	0x1d0000f8
DMA Address 0	0x1d000080	Band Line Counter	0x1d0000fc
DMA Address 1	0x1d000084	Centronics Status	0x1d000100
DMA Centronics Address	0x1d000088	Centronics Control	0x1d000104
DMA Count 0	0x1d000090	Centronics Nibble Data	0x1d000108
DMA Count 1	0x1d000094	Centronics Host	0x1d00010c
DMA Centronics Count	0x1d000098	Centronics Mode	0x1d000110
I/O Channel Timing	0x1d0000a0	Centronics Minimum Delay	0x1d000114
Decode Control	0x1d0000c0	Centronics Data Detect 0	0x1d0000a4
Decode Target Address	0x1d0000c4	Centronics Data Detect 1	0x1d0000a8
Decode Target Bytes	0x1d0000c8	Centronics Data Detect 2	0x1d0000ac

UART Register Map—R3740 only

Description	DLAB	Address	Description	DLAB	Address
Receiver Buffer	0	0x1d000300	Line Status	X	0x1d000314
Transmitter Holding	0	0x1d000300	Modem Status	X	0x1d000318
Interrupt Enable	0	0x1d000304	Scratch Pad	X	0x1d00031c
Interrupt Information	X	0x1d000308	Divisor Latch LSB[1]	1	0x1d000300
FIFO Control	X	0x1d000308	Divisor Latch MSB[1]	1	0x1d000304
Line Control	X	0x1d00030c	SYSCLK Divisor	X	0x1d000700
Modem Control	X	0x1d000310			

NOTE:

[1] Bit 7 of the UART Line Control register is used to gain access to the Divisor Latch registers. The Divisor Access Bit (DLAB) is zero on reset, and must be set to one to gain access to the Divisor Latch registers. The DLAB can be changed by writing to Line Control Bit 7.

ROM Configuration

This register is used to set the ROM address space for the two configurable ROM banks (ROMCS[1:0]*) and to set the number of wait state cycles inserted between data phases.[1]

Address: 1d000000

Bits	Field name	Function	Initial Value
0-3	First	The gap (number of cycles) from ROMCS* active to the first RDCEN*. 0000 - one cycle 0001 - two cycles n-1 - n cycles (1 to 16 cycles range)	0xf
4-7	Gap1	The gap between the first RDCEN* and the second RDCEN* 0000 - one cycle 0001 - two cycles n-1 - n cycles (1 to 16 cycles range)	0xf
8-11	Gap2	The gap between the second RDCEN* and the third RDCEN*. 0000 - one cycle 0001 - two cycles n-1 - n cycles (1 to 16 cycles range)	0xf
12-15	Gap3	The gap between the third RDCEN* and the fourth RDCEN* 0000 - one cycle 0001 - two cycles n - 1 - n cycles (1 to 16 cycles range)	0xf
16-21	AckTime	The gap from ROMCS* active to AckTime in block read 0000 - one cycle 0001 - two cycles n - 1 - n cycles (1 to 16 cycles range)	0x3f
22-23	SpaceSize	ROMCS[1:0]* address space size (ROMCS[2] has a fixed 4 Mbyte address space) 00 - 8 Mbyte 01 - 4 Mbyte 10 - 2 Mbyte 11 - 1 Mbyte	0x3

NOTE:

[1]It is the user's responsibility to set AckTime timing correctly.

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Video Configuration

This register is used for setting the horizontal and vertical margins; selecting PLL ON or OFF; setting video polarity; and setting the video bitstream shift direction for duplex (two-sided) printing. It is recommended that VerSkip and HorSkip only be changed at page boundaries.

Address: 1d000020

Bits	Field name	Function	Initial Value
0-12	VerSkip	Number of lines for the Vertical Skip from PAGE-SYNC*. Load n-1 to skip *n* lines.	0x0
13	VSE	Vertical Skip Enable 0 - Disable 1 - Enable	0x0
14-26	HorSkip	Number of pixels for the Horizontal Skip from LINE-SYNC*. Load n-1 to skip n pixels.	0x0
27	HSE	Horizontal Skip Enable 0 - Disable 1 - Enable	0x0
28	PLL	Video PLL Enable 0 - PLL Bypass 1 - PLL On	0x1
29	InvVid	Inverse Video, selects the video data polarity 0 - Non-inverse 1 - Inverse video	0x0
30	VidDir	Video Direction indicates the shifting direction of the video data, allowing printing on both-sides of a page 0 - MSB to LSB 1 - LSB to MSB	0x0

PIO Value

This register is used to set the value for those PIO pins configured by the PIO Control register as outputs.

Address: 1d000040

Bits	Field name	Function	Initial Value
0-5	PIO Value	Value of the PIO pins configured as outputs	0x0

PIO Control

This register sets the direction of the PIO pins.

Address: 1d000044

Bits	Field name	Function	Initial Value
0-5	PIO Control	Sets the direction of the corresponding PIO pin: 0 - Output 1 - Input	0x3f
6	Reserved	Must be 0	0

PIO Read Pins

This address is used to read inputs from the PIO pins.

Address: 1d00005C

Bits	Field name	Function	Initial Value
0-5	PIO Input Value	Value on the PIO pins	

Timer/Counter Value

This register is used to set the number of clocks to be counted by the Timer/Counter.

Address: 1d000048

Bits	Field name	Function	Initial Value
0-23	T/C Value	Number of clocks to count. Set to n to count to n.	0x000000

Timer/Counter Control

This register is used to enable and disable the Timer/Counter and to select the specific mode of use.

Address: 1d00004c

Bits	Field name	Function	Initial Value
0	Enable	Timer/Counter count enable 0 - Disable 1 - Enable	0x0
1	Select	Select mode of operation 0 - Counter 1 - Timer	0x0

Interrupt Cause

This register is used to identify the source behind an interrupt; it can also be used for polling of a specific interrupt or set of interrupts. A value of 1 indicates assertion of the interrupt. This register is also used to clear internal interrupts, writing a 0 will reset the corresponding internal interrupt. Writing a 1 will have no effect on the interrupt. External interrupts should be cleared via an external mechanism.

Address: 1d000050

Bits	Field name	Function	Initial Value
0	R3710: EngDMAInt R3740: DecDMAInt	Engine DMA interrupt	
1	LineInt	Line interrupt	
2	BandInt	Band interrupt	
3	PageInt	Page interrupt	
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	ComDMAInt	Compressor DMA interrupt	
9	DecErrInt	Decompressor error interrupt	
10	ComErrInt	Compressor error interrupt	
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Mask

This interrupt is used to mask (disable) specific interrupt sources, both internal and external (PIO). All the interrupts are maskable. A value of 0 masks the corresponding interrupt.

Address: 1d000054

Bits	Field name	Function	Initial Value
0	R3710: EngDMAInt R3740: DecDMAInt	Engine DMA interrupt	
1	LineInt	Line interrupt	
2	BandInt	Band interrupt	
3	PageInt	Page interrupt	
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	DecErrInt	Decompressor error interrupt	
9	ComErrInt	Compressor error interrupt	
10	CentRstInt	Centronics reset interrupt	
11	CenRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Write

This register is used to write to the Interrupt Cause register. This register should be used for interrupt testing only.

Address: 1d000060

Bits	Field name	Function	Initial Value
0	R3710: EngDMAInt R3740: DecDMAInt	Engine DMA interrupt	
1	LineInt	Line interrupt	
2	BandInt	Band interrupt	
3	PageInt	Page interrupt	
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	DecErrInt	Decompressor error interrupt	
9	ComErrInt	Compressor error interrupt	
10	CentRstInt	Centronics reset interrupt	
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	

Test

No reading or writing from/to this address. Doing so may result in improper generation of this device.

Address: 1d000064

DRAM Control

This register is used to set the desired DRAM device depth, access time (both for the CPU and Typhoon) and refresh frequency.

Address: 1d000058

Bits	Field name	Function	Initial Value
0-2	DevDepth Bank 1-2	Depth of the DRAM device used, in words. 000 - 256K 001 - 512K 010 - 1M 011 - 2M 100 - 4M	0x0
3-4	DevDepth Bank 0	Depth of the DRAM device used, in words. 00 - 256K 01 - 512K 10 - 1M 11 - 2M	0x0
5	ExtCas	CAS duration for both CPU and Typhoon accesses 0 - CAS is active for one and a half cycles 1 - CAS is active for two and a half cycles	0x0
6	TypExtCas	CAS duration for Typhoon accesses only 0 - CAS is active in Typhoon accesses for one and a half cycles 1 - CAS is active in Typhoon accesses for two and a half cycles	0x0
7-8	RefFreq	SYSCLK frequency 00 - 15.6 uS refresh time at 16MHz 01 - 15.6 uS refresh time at 20MHz 10 - 15.6 uS refresh time at 25MHz 11 - 15.6 uS refresh time at 33MHz	0x0

DMA Address 0

This register is used to set the first DRAM address used in channel 0 DMA operations.

Address: 1d000080

Bits	Field name	Function	Initial Value
0-25	DmaAddr0	First address for DMA channel 0.	0x0

DMA Address 1

This register is used to set the first DRAM address used in channel 1 DMA operations.

Address: 1d000084

Bits	Field name	Function	Initial Value
0-25	DmaAddr1	First address for DMA channel 1.	0x0

DMA Centronics Address

This register is used to set the first DRAM address used in Centronics DMA operation.

Address: 1d000088

Bits	Field name	Function	Initial Value
0-25	DmaAddrCent	First address for Centronics DMA.	0x0

DMA Count 0

This register is used to set the number of bytes to be transferred in a channel 0 DMA operation.

Address: 1d000090

Bits	Field name	Function	Initial Value
0-15	DmaCnt0	DMA count channel 0. Load with n-1 to transfer n.	0x0

DMA Count 1

This register is used to set the number of bytes to be transferred in a channel 1 DMA operation.

Address: 1d000094

Bits	Field name	Function	Initial Value
0-15	DmaCnt1	DMA count channel 1. Load with n-1 to transfer n.	0x0

DMA Centronics Count

This register is used to set the number of bytes to be transferred in a Centronics DMA operation.

Address: 1d000098

Bits	Field name	Function	Initial Value
0-15	DmaCntCen	Centronics DMA count. Load with n-1 to transfer n.	0x0

I/O Channel Timing

This register is used to configure the I/O bus parameters, including signal timing; DMA enabling, time-out, and direction; and the endianess of the 16-bit I/O channels. The DevTime fields specify the number of cycles IORD* or IOWR* are asserted in an I/O or DMA access. The Time Out Enable (TOEn) field chooses between inserting 32 clock cycles between arbitration cycles or not; normally, enabling this bit results in better system performance.

Address: 1d00000a0

Bits	Field name	Function	Initial Value
0-3	DevTime0	8-bit I/O channel 0 (IOCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
4	DmaEn0	DMA enable 8-bit channel 0. 0 - DMA disable 1 - DMA enable	0x0
5	DmaR/W0	DMA Read or Write 8-bit channel 0. 0 - DMA write 1 - DMA read	0x0
6-9	DevTime1	8-bit channel 1 (IOCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
10	DmaEn1	DMA enable 8-bit channel 1. 0 - DMA disable 1 - DMA enable	0x0
11	DmaR/W1	DMA Read or Write 8-bit channel 1. 0 - DMA write 1 - DMA read	0x0
12-15	CenTime	Centronics external register access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
16	DmaEnCen	Centronics DMA enable. 0 - DMA disable 1 - DMA enable	0x0
17	DmaR/WCen	DMA Read or Write for the Centronics interface. 0 - DMA write 1 - DMA read	
18-21	DevTime3	16-bit I/O channel 0 (IOGPCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
22-25	DevTime4	16-bit I/O channel 1 (IOGPCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0

Bits	Field name	Function	Initial Value
26	BigEndian0	Big or Little Endian for the 16-bit I/O channel 0 0 - Big Endian 1 - Little Endian	0x0
27	BigEndian1	Big or Little Endian for the 16-bit I/O channel 1 0 - Big Endian 1 - Little Endian	0x0
28	TOEn	Time Out Enable for both DMA channels 0 - Time out disabled, time out is 0 clocks 1 - Time out enabled, time out is 32 clocks	0x0

Video Control—R3710 only

This register sets the video data DMA parameters, including the DRAM address count direction for full-duplex (both sides of the sheet) printing, video data DMA enabling, last band indication, and blank band indication. The latter is used to print a blank band instead of requiring DRAM space.

Address: 1d0000c0

Bits	Field name	Function	Initial Value
0	CntDir	DRAM address count direction 0 - count up 1 - count down	0x0
1	DmaEn	Video DMA start enable 0 - Disable start of DMA 1 - Enable start of DMA	0x0
2	LastBand	Last Band indication 0 - Not last band 1 - Last band	0x0
3	BlankBand	Blank Band Indication 0 - Not Blank band 1 - Blank band	0x0

Line Word Counter—R3710 only

This register is used to set the number of words in a line. This does not include the horizontal margin defined by the HorSkip field (left margin) in the Video Configuration register.

Address: 1d0000c4

Bits	Field name	Function	Initial Value
0-10	LineWordCnt	Number of words in line. Set to n-1 if n is wanted.	0x0

Band Line Counter—R3710 only

This register is used to set the number of lines in a band. The aggregate of all the bands in a page does not include the VerSkip field (top margin) defined in the Video Configuration register.

Address: 1d0000c8

Bits	Field name	Function	Initial Value
0-10	BandLineCnt	Number of lines in band. Set to n-1 if n is wanted.	0x0

Video DMA Address Counter—R3710 only

This register is used to set the first DRAM word address from which the video DMA operation is to be done. Bits 0 and 1 are ignored (should be 0).

Address: 1d0000cc

Bits	Field name	Function	Initial Value
0-23	DmaAddress	First address for the video DMA. Set to n-1 if n is wanted.	0x0

Video DMA Word Counter—R3710 only

This register is used to set the number of 32-bit words to be transferred in the video DMA operation.

Address: 1d0000d0

Bits	Field name	Function	Initial Value
0-22	DmaCnt	Number of 32-bit words in the video DMA transfer. Set to n-1 to transfer n?	0x0

Decode Control—R3740 only

This register sets the decoder DMA parameters.

Address: 1d0000c0

Bits	Field name	Function	Initial Value
0	CntDir	DRAM address count direction 0 - count up 1 - count down	0x0
1	DmaEn	DMA start enable 0 - Disable start of DMA 1 - Enable start of DMA	0x0
2	LastBand	Last band indication 0 - Not last band 1 - Last band	0x0
3	BlankBand	Blank band indication 0 - Not Blank band 1 - Blank band	0x0
4	UpLastBand	Up-sampler last band indication 0 - Not last band 1 - Last band	0x0

Decode Target Address—R3740 only

This register is used to set the first DRAM word address to which the decoded data is written. Bits 0 and 1 are ignored (should be 0).

Address: 1d0000c4

Bits	Field name	Function	Initial Value
0-23	DmaAddress	First address for the decoder DMA write engine. Set to n-1 if n is wanted.	0x0

Decode Target Bytes—R3740 only

This register is used to set the number of bytes to be transferred in the decoder DMA write operation.

Address: 1d0000c8

Bits	Field name	Function	Initial Value
0-21	DmaCnt	Number of bytes to write via DMA transfer. Set to n-1 to transfer n bytes	0x0

Decode Source Address—R3740 only

This register is used to set the first DRAM word address to which the encoded data is read. Bits 0 and 1 are ignored (should be 0).

Address: 1d0000cc

Bits	Field name	Function	Initial Value
0-23	DmaAddress	First address for the decoder DMA read engine. Set to n-1 if n is wanted.	0x0

Decode Source Bytes—R3740 only

This register is used to set the number of bytes to be transferred in the decoder DMA read operation.

Address: 1d0000d0

Bits	Field name	Function	Initial Value
0-21	DmaCnt	Number of bytes to read via DMA transfer. Set to n-1 to transfer n bytes	0x0

Upsample Line Counter—R3740 only

This register is used to set the number of upsampled words in a line.

Address: 1d0000d4

Bits	Field name	Function	Initial Value
0-10	LineWordCnt	Number of words in current upsampled line. Set to n-1 if n is wanted.	0x0

Upsample Band Counter—R3740 only

This register is used to set the number of upsampled lines in a band. The aggregate of all the bands in a page does not include the VerSkip field (top margin) defined in the Video Configuration register.

Address: 1d0000d8

Bits	Field name	Function	Initial Value
0-10	BandLineCnt	Number of lines in current upsampled band. Set to n-1 if n is wanted.	0x0

Encode Control—R3740 only

This register sets the encoder DMA parameters.

Address: 1d0000dc

Bits	Field name	Function	Initial Value
0	CntDir	DRAM address count direction 0 - count up 1 - count down	0x0
1	DmaEn	DMA start enable 0 - Disable start of DMA 1 - Enable start of DMA	0x0
2	EncodeDir	Encode bits direction 0 - Scanline direction is left to right 1 - Scanline direction is right to left	0x0

Encode Target Address—R3740 only

This register is used to set the first DRAM word address to which the encoded data is written. Bits 0 and 1 are ignored (should be 0).

Address: 1d0000e0

Bits	Field name	Function	Initial Value
0-23	DmaAddress	First address for the encoder DMA write engine. Set to n-1 if n is wanted.	0x0

Encode Target Bytes—R3740 only

This register is used to set the number of bytes to be transferred in the encoder DMA write operation.

Address: 1d0000e4

Bits	Field name	Function	Initial Value
0-21	DmaCnt	Number of bytes to write via DMA transfer. Set to n-1 to transfer n bytes	0x0

Encode Source Address—R3740 only

This register is used to set the first DRAM word address from which the encoded data is read. Bits 0 and 1 are ignored (should be 0).

Address: 1d0000e8

Bits	Field name	Function	Initial Value
0-23	DmaAddress	First address for the encoder DMA read engine. Set to n-1 if n is wanted.	0x0

Encode Source Bytes—R3740 only

This register is used to set the number of bytes to be transferred in the encoder DMA read operation.

Address: 1d0000ec

Bits	Field name	Function	Initial Value
0-21	DmaCnt	Number of bytes to read via DMA transfer. Set to n-1 to transfer n bytes	0x0

Downsample Line Counter—R3740 only

This register is used to set the number of downsampled words in a line.

Address: 1d0000f0

Bits	Field name	Function	Initial Value
0-10	LineWordCnt	Number of words in current downsampled line. Set to n-1 if n is wanted.	0x0

Status—R3740 only

This register is used to set the status of the encoder and the decoder.

Address: 1d0000f4

Bits	Field name	Function	Initial Value
0	Mode	Mode of operation 0 - Upsampling/Downsampling 1 - Compression/Decompression	0x0
1	Print	Decode to engine or memory 0 - To engine 1 - To memory	0x0
2	Bypass	Bypass the decode operation 0 - Bypass 1 - Do not bypass	0x0
3	DataRdy	Data ready for engine (this bit is Read only) 0 - Not ready 1 - Ready	0x0

Line Word Counter—R3740 only

This register is used to set the number of words in a line.

Address: 1d0000f8

Bits	Field name	Function	Initial Value
0-10	LineWordCnt	Number of words in current printed line. Set to n-1 if n is wanted.	0x0

Band Line Counter—R3740 only

This register is used to set the number of lines in a band.

Address: 1d0000fc

Bits	Field name	Function	Initial Value
0-10	BandLineCnt	Number of lines in current printed band. Set to n-1 if n is wanted.	0x0

Centronics Status

This register is used to implement the Centronics hand-shake protocol via software by the CPU.

Address: 1d000100

Bits	Field name	Function	Initial Value
0	Busy	Printer busy indication 0 - Ready 1 - Busy	0x0
1	Ack	Printer acknowledge 0 - acknowledge 1 - Normal	
2	Fault	Fault indication 0 - Fault 1 - Normal	
3	Select	Select 0 - Off line 1- On line	
4	Perror	Paper Error indication 0 - No error 1- Error	

Centronics Control

This register is used to set the Centronics transfer mode per the IEEE 1284 specification Rev. 2.

Address: 1d000104

Bits	Field name	Function	Initial Value
0-2	Mode	IEEE 1284 modes 000 - Compatible 001 - Nibble 010 - Byte 011 - ECP 100 - EPP 101 - CPU control 110 - extensibility link 111 - termination	0x0
3	NegRep	Negotiation Reply All modes except nibble mode: 0 - mode requested by host is not supported by the peripheral (eg. printer) 1- mode requested is supported Nibble mode: 0- mode requested by host is supported by the peripheral (eg. printer) 1- mode requested is not supported	0x0

Centronics Nibble Data

This register is used to post the data to be transferred in nibble mode.

Address: 1d000108

Bits	Field name	Function	Initial Value
0-7	NibData	Nibble mode Centronics data to be sent to the host	

Centronics Host

This register is used to read inputs from the host in the Centronics protocol pins.

Address: 1d00010c

Bits	Field name	Function (In compatible mode)	Initial Value
0	Strobe	Set LOW by the host to transfer data	
1	SelectIn	Set LOW by host to select printer	
2	Init	Pulsed LOW with SelectIn active LOW to reset the Centronics interface	
3	AutoFd	Set LOW by the host to put the printer in auto-feed mode.	

Centronics Mode

This register is used to set the Centronics DMA parameters and select the protocol options in Compatible mode.

Address: 1d000110

Bits	Field name	Function	Initial Value
0-1	Application	See IEEE 1284 standard for details 00 - Standard 01 - IBM Epson 10 - Reserved 11 - Classic	
2	DmaEn	0 - transmission executed by CPU 1 - transmission executed by DMA	
3	DmaDir	0 - DMA write 1 - DMA reads	

Centronics Minimum Delay

This register contains the values that are needed for each operating frequency to comply with the IEEE 1284 standard (minimum of 500ns and 2500ns). However for systems with higher performance requirements, it is possible to program the minimum delays for lower values.

Address:1d000114

Bits	Field name	Function	Initial Value
0-6	2500ns	16MHz - 0x28 20MHz - 0x32 25MHz - 0x3f 33MHz - 0x53	
7-13	500ns	16MHz - 0x08 20MHz - 0x0a 25MHz - 0x0d 33MHz - 0x11	

Centronics Data Detect 0

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a4

Bits	Field name	Function	Initial Value
0-7	DataDet0	Data to be used for comparison with the incoming data.	

Centronics Data Detect 1

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a8

Bits	Field name	Function	Initial Value
0-7	DataDet1	Data to be used for comparison with the incoming data.	

Centronics Data Detect 2

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000ac

Bits	Field name	Function	Initial Value
0-7	DataDet2	Data to be used for comparison with the incoming data.	

UART Receiver Buffer—R3740 only

This register holds the five to eight bit received word. If less than 8 bits are received the data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received. This is a Read only register.

DLAB: 0 Address: 1d000300

Bits	Field name	Function	Initial Value
0-7	RecData	Received data	

UART Transmitter Holding—R3740 only

This register holds the five to eight bit transmitted word. If less than 8 bits are transmitted the data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit transmitted. This is a Write only register.

DLAB: 0 Address: 1d000300

Bits	Field name	Function	Initial Value
0-7	TranData	Transmitted data	

UART Interrupt Enable—R3740 only

This register is used to independently enable the four serial channel interrupt sources that set the UARTInt bit in the interrupt cause register. A logic one enables the interrupt and a logic zero will disable the interrupt. Master Reset will disable all interrupts and reset the all bits in this register to zero.

DLAB: 0 Address: 1d000304

Bits	Field name	Function	Initial Value
0	RcvDataAv	Enable received data available.	
1	TrHldEmpty	Enable transmitter holding empty	
2	RcvLineStat	Enable receiver line status interrupts	
3	ModStat	Enable modem status interrupt	
4-7	IntEn[4:7]	Always 0	

UART Interrupt Information—R3740 only

This register contains an interrupt code that denotes the priority and the source of the interrupt that is pending . This is a Read only register.

DLAB: x Address: 1d000308

Bits	Field name	Function	Initial Value
0-2	IntInf[0:2]	Five recognizable codes are implemented: xx1 - No interrupt pending 110 - First Priority; Receiver Line Status interrupt caused by OE, FE, PE, or BI. Cleared by reading the Line Status register. 100 - Second Priority; Received Data interrupt-caused by Received Data Available. Cleared by reading the Receiver Buffer register. 010 - Third Priority; Transmitter Holding interrupt - caused by Transmitter Holding Register empty. Cleared by reading the Interrupt Information register or writing to the Transmitter Holding Register. 000 - Fourth Priority; Modem Status interrupt - caused by DSR, RI, DCD. Cleared by reading the Modem Status register.	
3-7	IntInf[3:7]	Always 0.	

UART FIFO Control—R3740 only

This register is used to enable and clear the FIFOs, set the trigger level of the receiver FIFO, and select the type of DMA signaling. This is a Write only register.

DLAB: x Address: 1d000308

Bits	Field name	Function	Initial Value
0	FIFOEn	When HIGH, enables both the transmit and receiver FIFOs. All bytes in both FIFOs can be cleared by resetting this bit. Data is cleared automatically from the FIFOs when changing from FIFO mode (FIFOEn =1) to non-FIFO mode (FIFOEn =0) and vice versa. Programming of other FIFO bits is enabled by setting FIFOEn HIGH.	
1	RcvClear	When HIGH, clears all bytes in the receiver FIFOs and reset the counter logic to 0. This does not clear the shift register.	
2	TrClear	When HIGH, clears all bytes in the transmit FIFOs and resets the counter logic to 0. This does not clear the shift register.	
3	IntDMAMode	When HIGH, will change the RxRdyInt and TxRdyInt interrupts from DMA mode 0 to DMA mode 1 if FIFOEn = 0	
4-5	Reserved		
6-7	RcvTrigLev	Controls the trigger level for the receiver FIFO interrupt and follows the 16550 convention: 00 - 1 01 - 4 10 - 8 11 - 14	

UART Line Control—R3740 only

This register controls the format of the data character. It is cleared by Master Reset to a state of 00 Hex.

DLAB: x Address: 1d00030c

Bits	Field name	Function	Initial Value
0-1	CharLeng	Defines the data character word length. 00 - character length is 5 bits 01 - character length is 6 bits 10 - character length is 7 bits 11 - character length is 8 bits	
2	StopBitSel	Stop Bit Select - When zero, there is one stopbit. When one, the number of stop bits is determined by the word length. If the word length is 5 and stop bit select is HIGH there are 1.5 stop bits. Else if stop bit select is HIGH there are 2 stop bits.	
3	ParEn	Parity Enable - When HIGH and parity is enabled, a parity bit is placed and checked between the last data character and the stop bits.	
4	ParSel	Parity Select - When HIGH and parity is enabled, EVEN parity is selected. When LOW and parity is enabled ODD parity is selected.	
5	StickPar	Stick Parity - When HIGH and parity is enabled, it causes the transmission and reception of a parity bit in the opposite state from the value of bit 4 of the Line Control register.	
6	BrkCtrl	Break Control - When HIGH, the serial output TXD is set to zero, but does not affect the transmitter logic. When returned to LOW, TXD is released from the LOW state.	
7	DLAB	Divisor Latch Access Bit.	

UART Modem Control—R3740 only

This register controls the interface with a modem.

DLAB: x Address: 1d000310

Bits	Field name	Function	Initial Value
0	DTROut	When this bit is set HIGH the DTR output is forced LOW. When this bit is set LOW the DTR output is set HIGH.	
1-3	ModCont[1:3]	Not used.	
4	LoopBack	When set HIGH, a local loopback mode for diagnostic testing is activated. The TXD pin is set inactive and internally connected directly to the RXD pin. All external input on the RXD pin is ignored. The three modem control inputs (DSR, DCD,and RI) are disconnected. The modem control output (DTR) is internally connected to the modem control input and externally set inactive.	
5-7	ModCont[5:7]	Always 0.	

UART Line Status—R3740 only

This register provides status indications on the receiver and transmitter operations of this part.

DLAB: x Address: 1d000314

Bits	Field name	Function	Initial Value
0	DataRdy	Data Ready - a HIGH value indicates that the receiver has data that is ready to be read from the Read Buffer register. This bit is reset when such register is read.	
1	OvrErr	Overrun Error - a HIGH value indicates that the data in the Read Buffer register has been overwritten by the receiver before it was read. This bit is reset when the Line Status register is read.	
2	ParErr	Parity Error - is set HIGH when the received character does not have the correct even or odd parity. This bit is reset when the Line Status register is read.	
3	FraErr	Framing Error - a HIGH value indicates that the received character did not have a valid stop bit. This bit is reset when the Line Status register is read.	
4	BrkInt	Break Interrupt - is set HIGH when RXD is held LOW for longer than one data character. This bit is reset when the Line Status register is read.	
5	TrHldEmpty	Transmitter Holding Register Empty - is set HIGH when the transmitter is ready to receive another word to transmit in the Transmitter Holding register. This bit is reset LOW when a character is transferred to the Transmitter Shift register, and remains LOW until the character is transferred to the Transmitter Shift register.	
6	TrEmpty	Transmitter Empty - is set HIGH when the Transmitter Holding register and the Transmitter Shift register are both empty. This is reset LOW when a character is transferred to the Transmitter Holding register and remains LOW until all characters have been transferred to TXD.	
7	LineStat7	Always 0.	

UART Modem Status—R3740 only

This register provides status information about the modem input lines.

DLAB: x Address: 1d000318

Bits	Field name	Function	Initial Value
0	ModStat0	Always 0.	
1	DelDSR	Delta Data Set Ready - when HIGH indicates a change in state of the DSR input pin. This bit is cleared when the Modem Status register is read.	
2	TraEdRI	Trailing Edge Ring Indicator - when HIGH, it indicates a LOW to HIGH transition has occurred on the RI input pin. This bit is clear when the Modem Status register is read.	
3	DelCD	Delta Data Carrier Detect - when HIGH, it indicates a change of state on the DCD input pin. This bit is cleared when the Modem Status register is read.	
4	ModStat4	Not used.	
5	DSR	Data Set Ready - indicates the state of the DSR pin.	
6	RI	Ring Indicator - indicates the state of the RI pin.	
7	DCD	Data Carrier Detect - indicates the state of the DCD pin.	

UART Scratch Pad—R3740 only

This register has no effect on the operation of the IDT79R3740. The user can store any information in this 8-bit register.

DLAB: x Address: 1d00031c

Bits	Field name	Function	Initial Value
0-7	ScrPad	User defined	

UART Divisor Latch LSB—R3740 only

This register contains the lower 8 bits of the baud rate divisor. In combination with the corresponding MSB, the 16-bit baud rate divisor allows for baud rates of UARTCLK (SYSCLK divided by the number in the SYSCLK Divisor register), divided by any number from 1 to 2^{16}-1.

DLAB: 1 Address: 1d000300

Bits	Field name	Function	Initial Value
0-7	DivLatLSB	Baud rate divisor lower 8 bits.	

UART Divisor Latch MSB—R3740 only

This register contains the upper 8 bits of the baud rate divisor. In combination with the corresponding LSB, the 16-bit baud rate divisor allows for baud rates of UARTCLK (SYSCLK divided by the number in the SYSCLK Divisor register), divided by any number from 1 to 2^{16}-1.

DLAB: 1 Address: 1d000304

Bits	Field name	Function	Initial Value
0-7	DivLatMSB	Baud rate divisor upper 8 bits.	

UART SYSCLK Divisor—R3740 only

This register contains 4 bits of the SYSCLK rate divisor. SYSCLK will be divided by any number from 1 to 16.

DLAB: x Address: 1d000700

Bits	Field name	Function	Initial Value
0-3	SysClkDiv	SYSCLK rate divisor.	

EXTERNAL ADDRESS SPACE

The address space allocated to the different resources in the system is shown in Table 1. Bits 29-31 are not decoded so that physical aliases of 512 Mbyte are created. This enables the software to access the same system resource using different attributes (i.e cached space vs. uncached space, kernel vs. user).

Description	Size	Physical Address Range[1]
DRAM	40M	0X00000000: 0x027FFFFF
ROMCS[2]*.	4M	0x1FC00000: 0x1FFFFFFF
ROMCS[1]*	8M	0x1F400000: 0x1FBFFFFF
ROMCS[0]*	8M	0x1EC00000: 0x1F3FFFFF
IO channel 0	16M	0x08000000: 0x08FFFFFF
IO channel 1	16M	0x09000000: 0x09FFFFFF
IO channel 2	16M	0x0B000000: 0x0BFFFFFF
IO channel 3	256M	0x0C000000: 0x1BFFFFFF
Centronics External register	1M	0x0A000000: 0x0A0FFFFF
Engine Control	1M	0x0A800000: 0x0A8FFFFF
Typhoon address space	16M	0x1C000000: 0x1CFFFFFF
Internal registers	16M	0x1D000000: 0x1DFFFFFF

Note:
[1] This table specifies maximum range.

Table 4.1: External Address Space

6

IMPLEMENTATION EXAMPLES

Full Implementation

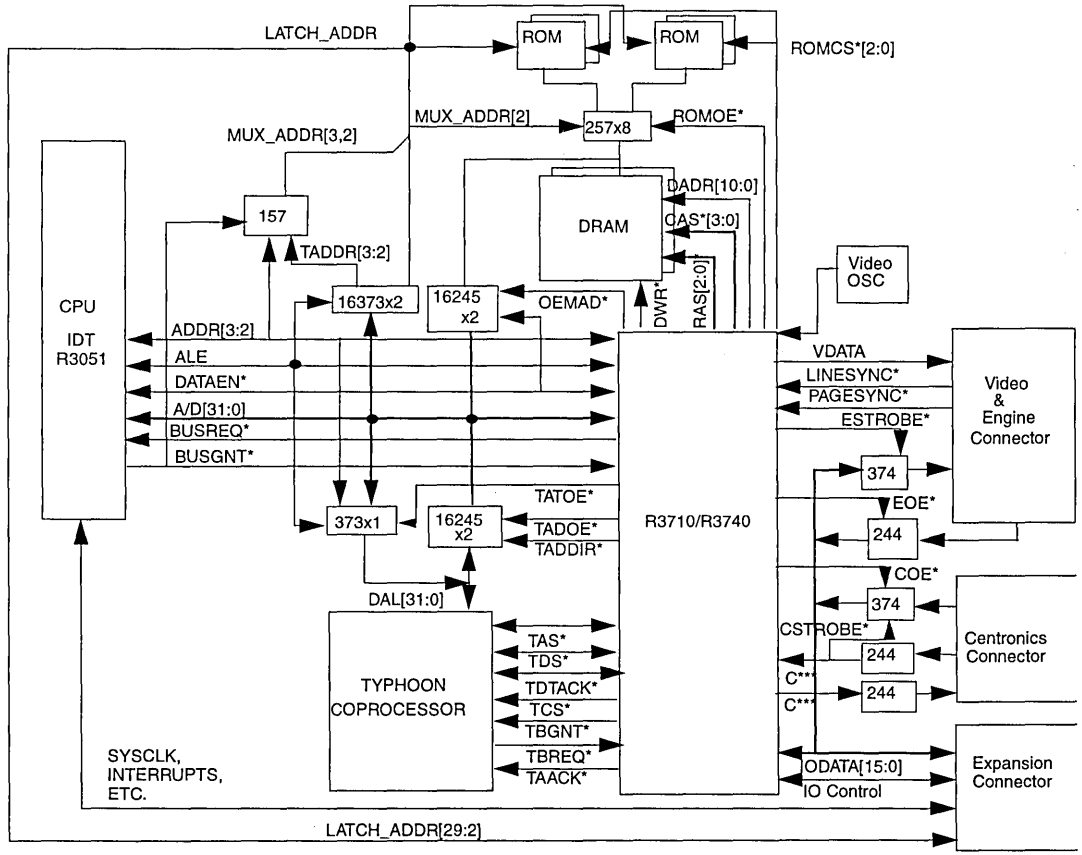
A possible implementation of a fully featured system is shown in Figure 5.1. This system includes a 2-way interleaved ROM array, and uses external multiplexers (FCT257x8) that are controlled by MUX_ADDR[2] to choose one bank or the other. The R3710 or R3740 directly provides the output enable signal to these multiplexers (ROMOE*), as well as the chip select signal to the ROM banks (ROMCS*[2:0]).

The control to the DRAM banks is provided directly by signals coming out of the R3710 or R3740. These signals can directly control up to 3 banks of DRAM and 40MB.

This implementation supports Adobe's Typhoon rasterizing coprocessor and thus an extra set of latches and transceivers are used to accommodate it. All control signals necessary to provide DMA master and slave operations to the Typhoon are provided. Multiplexing between the Typhoon and CPU is done via BUSGNT*.

The R3710 or R3740's video/engine interface processes line and page synchronization signals from the engine and provides it with a serial video data stream.

The R3710 or R3740 also generates the control signals necessary to transfer parallel byte or word data to and from the printer's engine (EOE* and ESTROBE*).



NOTE: C***=Centronics Control Signals

Figure 5.1 Full Implementation With Interleaved ROM

A full complement of signals is provided by the R3710 or R3740 to implement an IEEE1284 bi-directional Centronics interface.

The 80186-style I/O bus interfaces to a connector that can be used to expand features by adding standard industry peripherals like SCSI, PCMCIA cards, UARTs, Ethernet, etc.

Minimal Implementation

Figure 5.2 shows a minimal implementation. In this case, we show the lower end CPU in the R3051 Family, the R3041.

A simple non-interleaved ROM subsystem is used in this case, with only 1 bank - the boot bank ROMCS[2]*.

The DRAM system contains only 1 bank and as we mentioned before, the R3710 or R3740 directly provides all the necessary signals.

Since a coprocessor is not used in this case, the interface to the AD bus is very simple.

The balance of the features shown is the same, but this could conceivably include simpler implementations of each, like less peripherals via the IODATA bus, or a lower video rate that could be associated with an engine with less dots per inch or less pages per minute.

Both the full and the minimal implementations shown demonstrate the flexibility of the R3710 or R3740 as a common block that enables modular designs or designs that can be upgraded in the field.

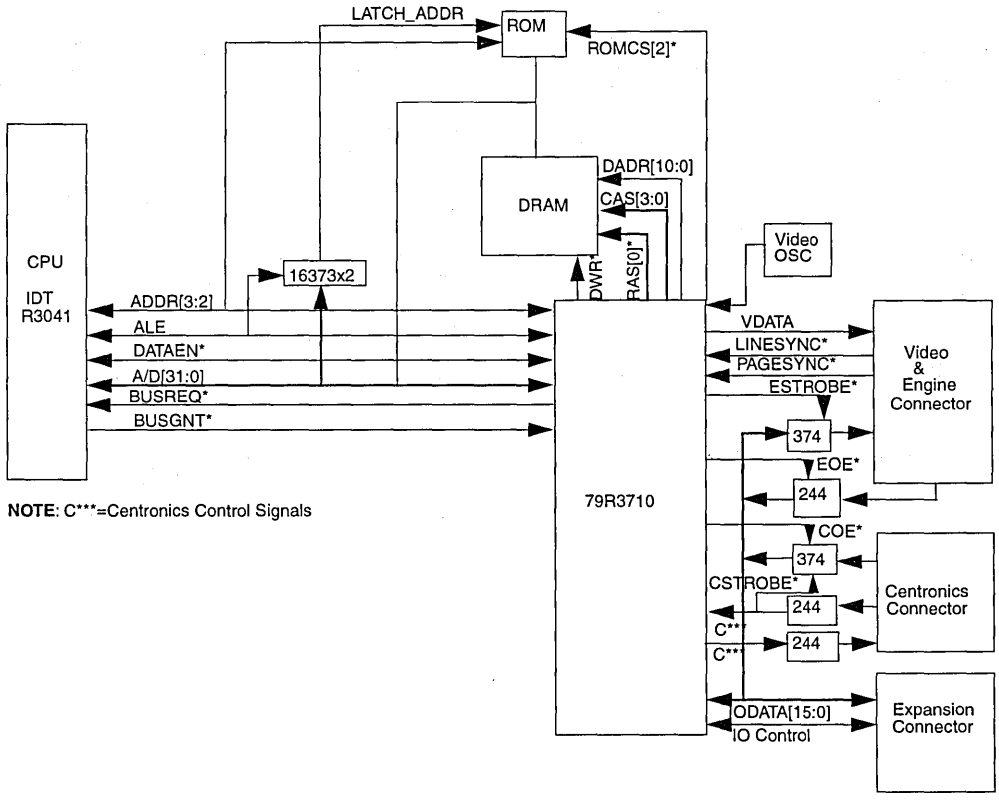


Figure 5.2 Minimal Implementation

Example of Video Controller Setup (R3710 only)

Working with the Video Controller should be viewed as working with 2 independent state machines that work in parallel and are synchronized by the 4-entry deep video FIFO (Figure 5.3). One state machine is the DMA, that brings data from the frame buffer in the DRAM into the video FIFO. The second state machine is the Video Controller itself, which takes the data from the FIFO into a shift register and shifts it out to the printer's engine.

In addition, the Video Controller is responsible for the synchronization with the printer's engine (PAGESYNC* and LINESYNC* signals), including the horizontal and vertical margin generation.

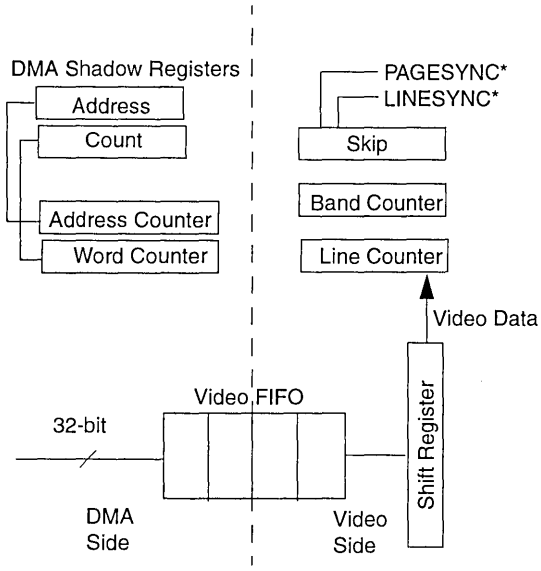


Figure 5.3 Video Block Diagram

Setup Procedure Example (R3710 only)

The following is an example of a simple procedure for using the Video Controller for the R3710. We will be using one DMA per band, and *n* bands per page:

1. At the initialization sequence, set the PLL field to either 1 for using the on-board PLL or 0 to bypass it.
2. Initialize the Band and Line counters (BandLineCnt, LineWordCnt), remembering that a value of *n-1* is needed to count to *n*. It is recommended that Line and Band size change on page boundaries only.
3. Initialize the Vertical and Horizontal margin parameters (VerSkip, HorSkip, VSE, HSE fields).
4. Choose the desired values for the Inverse Video (InvVideo) and Video Direction(VidDir) fields.
5. Set the LastBand field to a value of 0 and the BlankBand field to a value of 1.
6. Set the video DMA address (DmaAddress). Notice that it is a 24-bit word address with the R3710 ignoring the 2 least significant bits. For instance, if the current DMA should start from physical address hex 0234, a value of 0x 00000234 should be written to the address register (no shifting by 2-bits is required).
7. Set the Video DMA Word counter (DmaCnt) to *n-1* when *n*x32 pixels need to be transferred into the video FIFO for printing.
8. Set the address count direction (CntDir) to either up or down.
9. Write 1 to the DMAEn field.
10. Write the address and count registers for the next band.
11. Write the next address and count registers on the occurrence of the EngDMAInt interrupt.
12. Continue step 11 on each EngDMAInt.
13. On the *n-1* EngDMAInt, write 0 to the DMAEn field.
14. On the next BandInt interrupt, write 1 to the LastBand field.

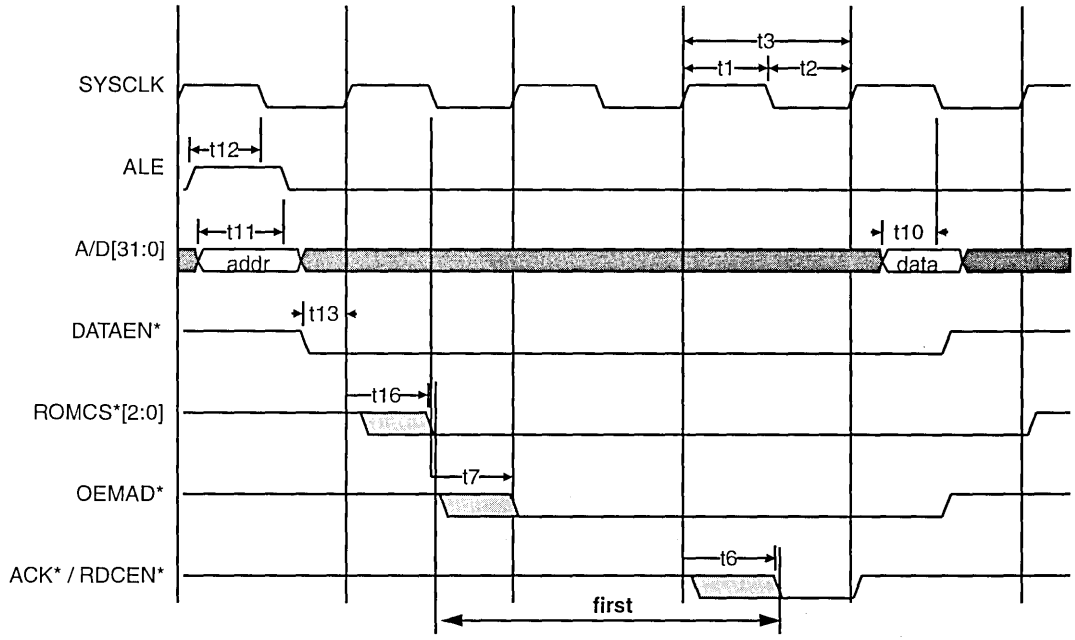
Repeat steps 2 through 14 of this procedure for every page.

PINOUT TABLE

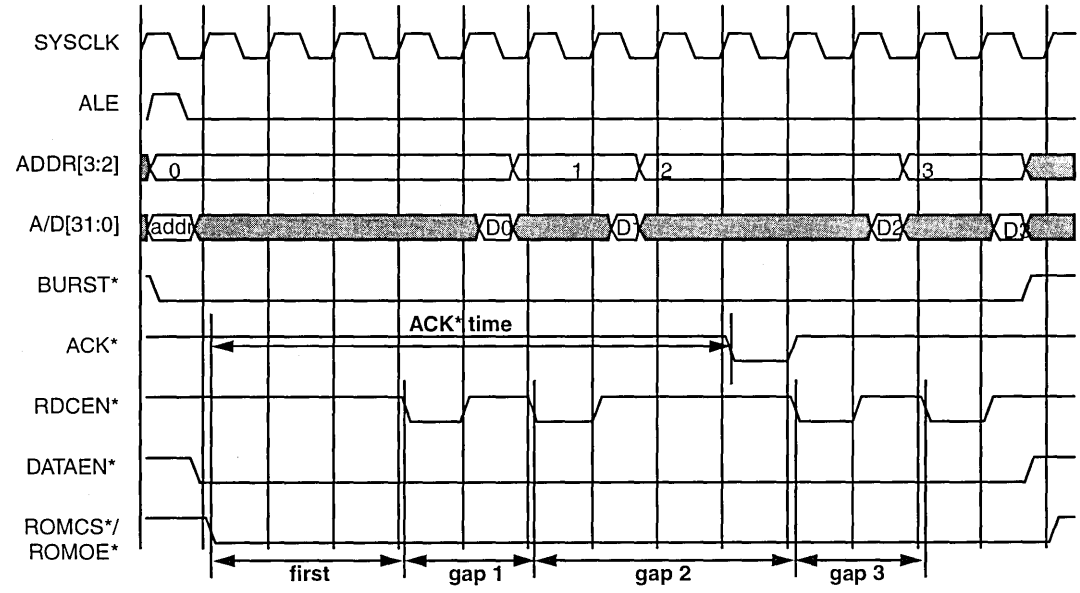
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	AD(14)	41	TAS*	81	IOBE(1)*	121	RAS*[0]
2	AD(13)	42	TCS*	82	IOBE(0)*	122	RAS(1)*
3	AD(12)	43	TAACK*	83	IOGPCS[1]*	123	RAS(2)*
4	AD(11)	44	PIO(0)	84	IOGPCS[0]*	124	CAS(0)*
5	AD(10)	45	PIO(1)	85	IOCS(1)*	125	CAS(1)*
6	VDD	46	PIO(2)	86	IOCS(0)*	126	CAS(2)*
7	VSS	47	PIO(3)	87	DMAREQ(0)	127	CAS(3)*
8	AD(9)	48	R3710: PIO(4) R3740: PIO(4)/RI	88	DMAREQ(1)	128	DWR*
9	AD(8)	49	R3710: PIO(5) R3740: DCD (PIO(5))	89	IODATA(15)	129	ROMCS(2)*
10	AD(7)	50	CSELECTIN*	90	IODATA(14)	130	VDD
11	AD(6)	51	CINIT*	91	IODATA(13)	131	VSS
12	AD(5)	52	CSTROBE*	92	IODATA(12)	132	ROMCS(1)*
13	AD(4)	53	CRSTROBE	93	IODATA(11)	133	ROMCS(0)*
14	AD(3)	54	CBUSY	94	IODATA(10)	134	ROMOE*
15	AD(2)	55	VDD	95	IODATA(9)	135	LINESYNC*
16	AD(1)	56	SYSCLK	96	IODATA(8)	136	PAGESYNC*
17	AD(0)	57	VSS	97	IODATA(7)	137	VCLKIN
18	VDD	58	CWSTROBE	98	IODATA(6)	138	VDATA
19	VSS	59	CROE*	99	IODATA(5)	139	AD(31)
20	VSS	60	VDD	100	IODATA(4)	140	AD(30)
21	BURST*	61	CAUTOFD*	101	VDD	141	AD(29)
22	ADDR(3)	62	CPERROR	102	VDD	142	AD(28)
23	ADDR(2)	63	CSELECT	103	VSS	143	VSS
24	ALE	64	CWOE*	104	IODATA(3)	144	AD(27)
25	RD*	65	CACK*	105	IODATA(2)	145	AD(26)
26	WR*	66	CFAULT*	106	IODATA(1)	146	AD(25)
27	DATAEN*	67	EOE*	107	IODATA(0)	147	AD(24)
28	BUSGNT*	68	ESTROBE*	108	DADR(10)	148	AD(23)
29	RESET*	69	R3710: N.C. R3740: TXD	109	DADR(9)	149	AD(22)
30	ACK*	70	R3710: N.C. R3740: RXD	110	DADR(8)	150	VDD
31	RDCEN*	71	R3710: N.C. R3740: DSR	111	DADR(7)	151	VSS
32	BUSREQ*	72	R3710: N.C. R3740: DTR	112	VDD	152	AD(21)
33	INT*	73	VDD	113	VSS	153	AD(20)
34	TADOE*	74	VSS	114	DADR(6)	154	AD(19)
35	TADDIR*	75	IOWAIT*	115	DADR(5)	155	AD(18)
36	TATOE*	76	DMAACK(1)*	116	DADR(4)	156	AD(17)
37	TDTACK*	77	DMAACK(0)*	117	DADR(3)	157	AD(16)
38	TDS*	78	IOWR*	118	DADR(2)	158	AD(15)
39	TBREQ*	79	IORD*	119	DADR(1)	159	OEMAD*
40	TBGNT*	80	IOA1	120	DADR(0)	160	TEST

TIMING DIAGRAMS

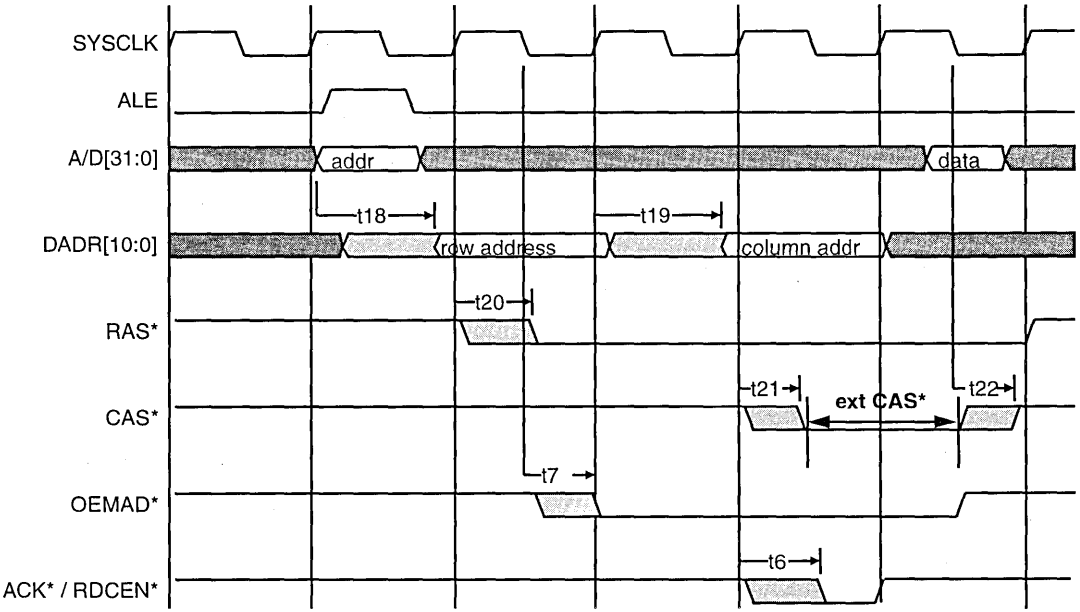
This section contains timing diagrams for the R3710 and R3740 signals. Diagrams that apply to only one controller are identified as either "R3710" or "R3740."



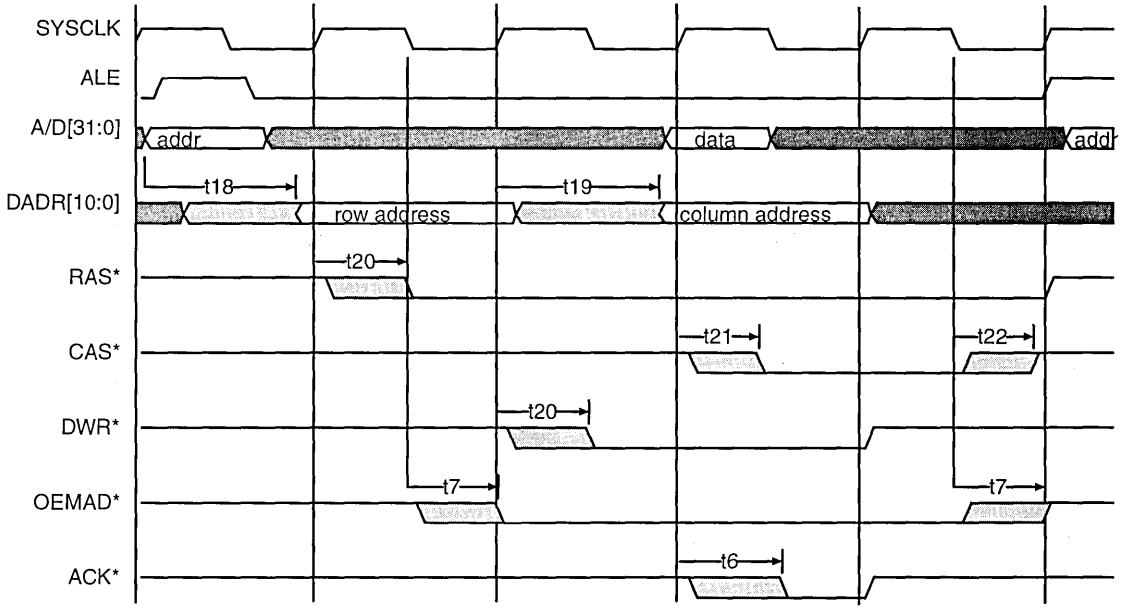
ROM Read (Programmable)



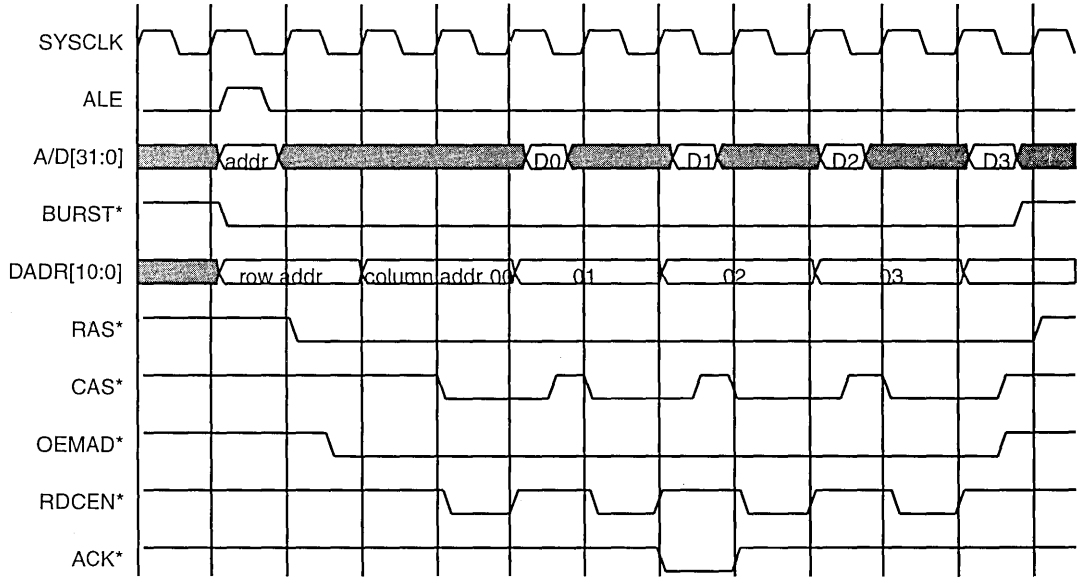
Interleaved ROM Burst Read (Programmable)



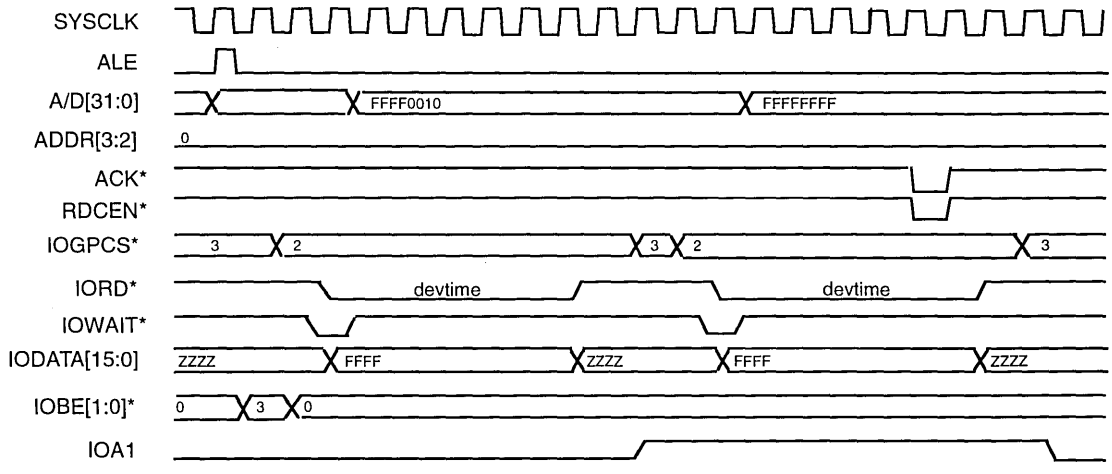
DRAM Read (Programmable)



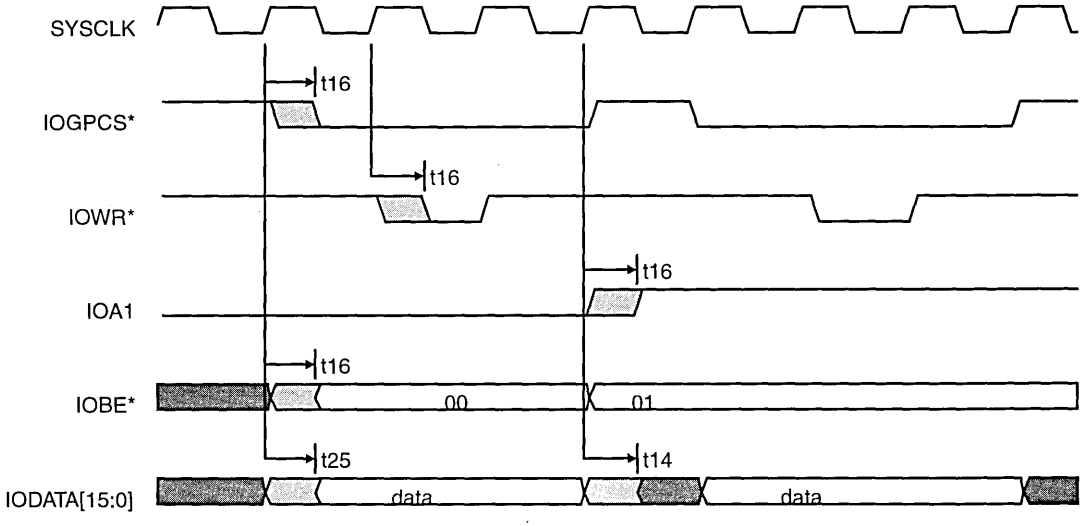
DRAM Write



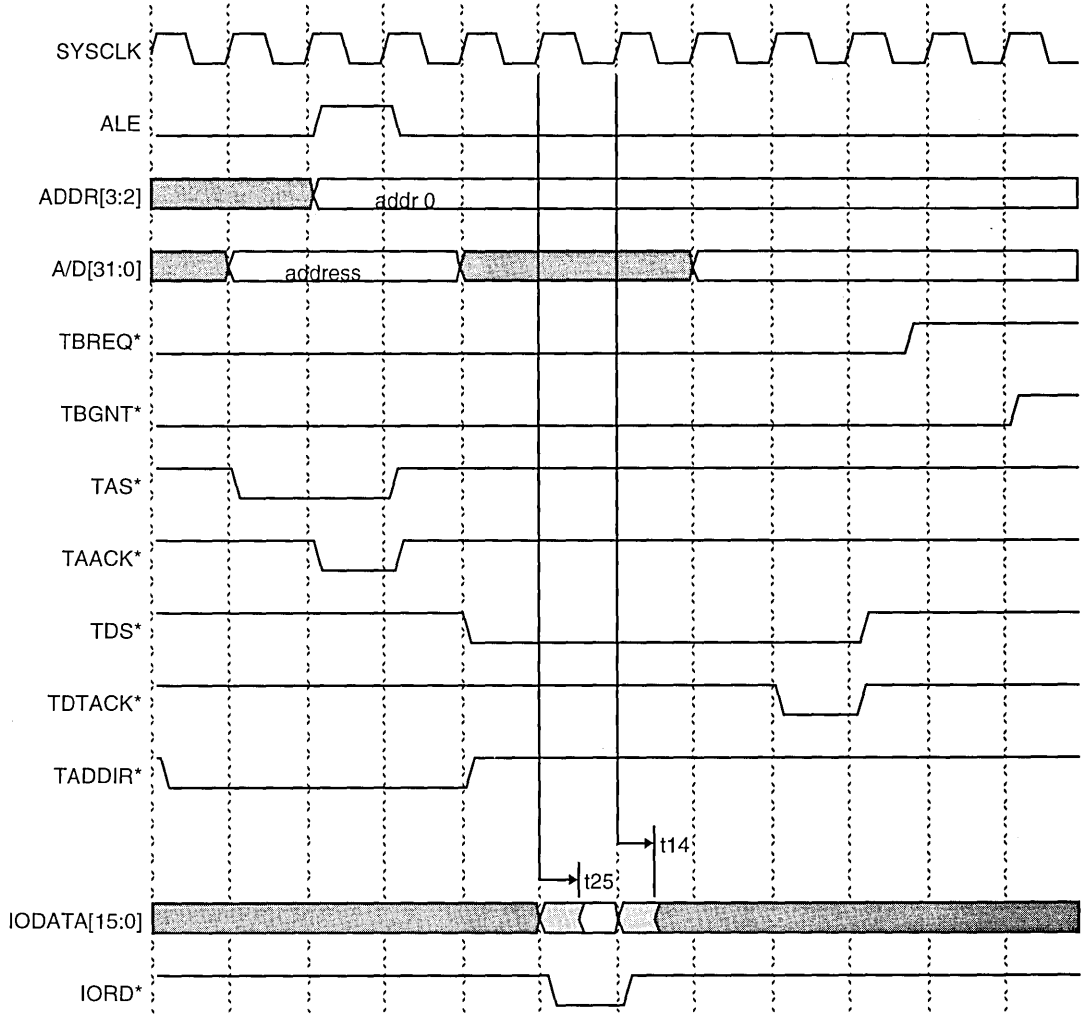
DRAM Burst Read



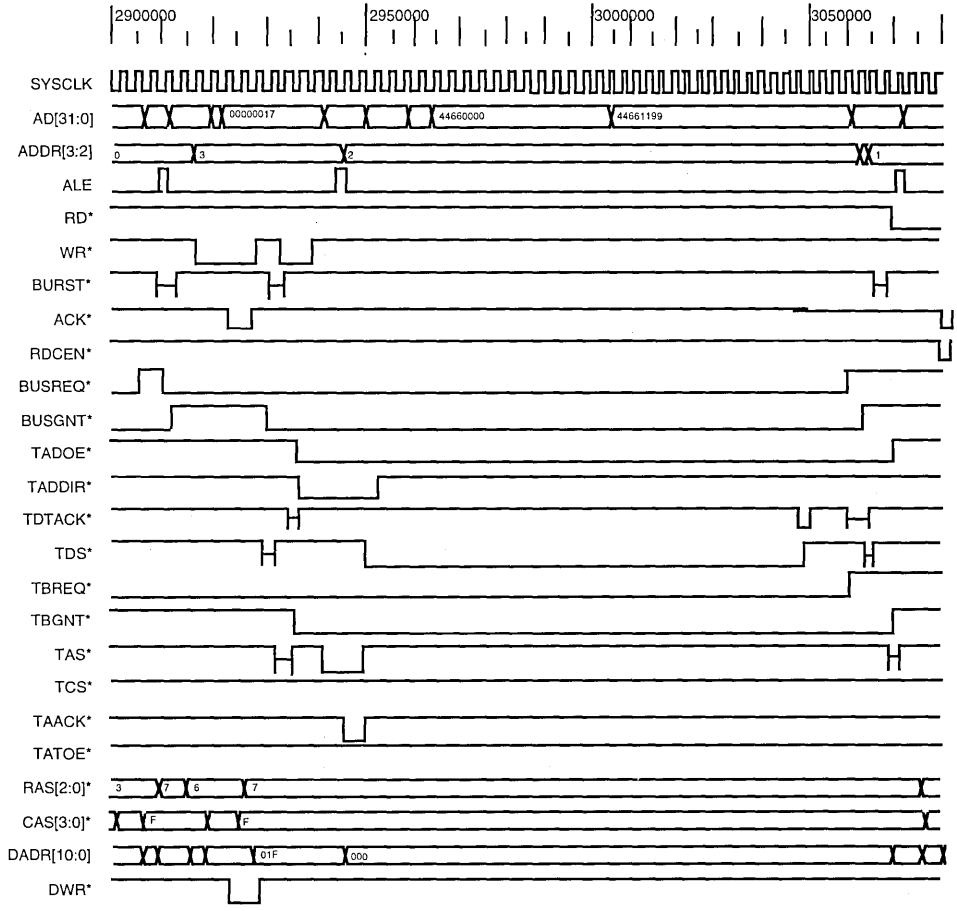
I/O Read 16-Bit



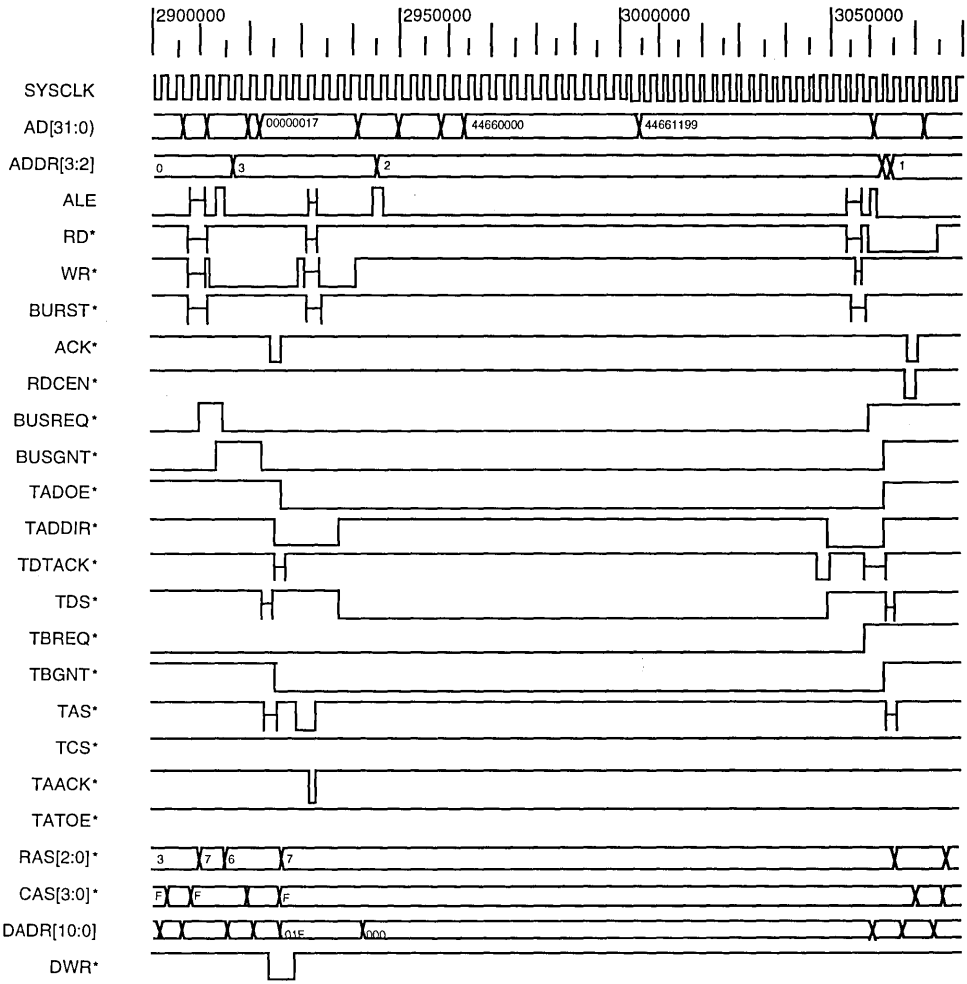
I/O Write 24-Bit



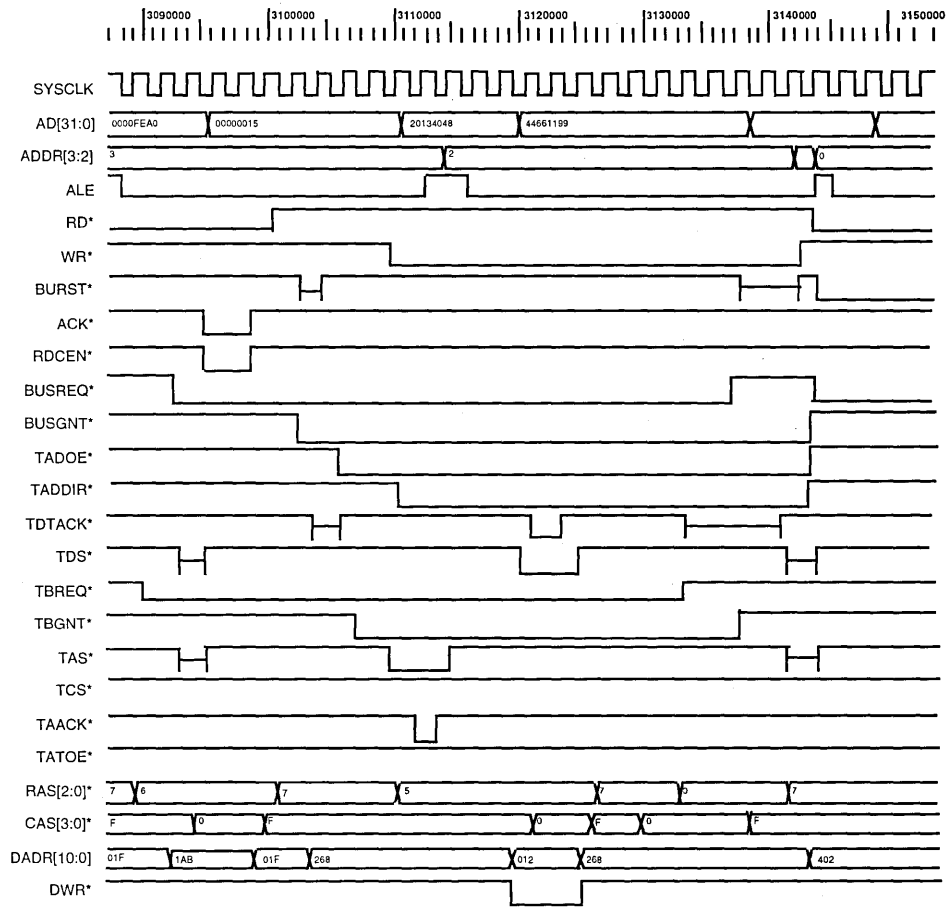
Typhoon Master I/O Read



Typhoon Master Read—R3710



Typhoon Master Read—R3740



Typhoon Master Write—R3710

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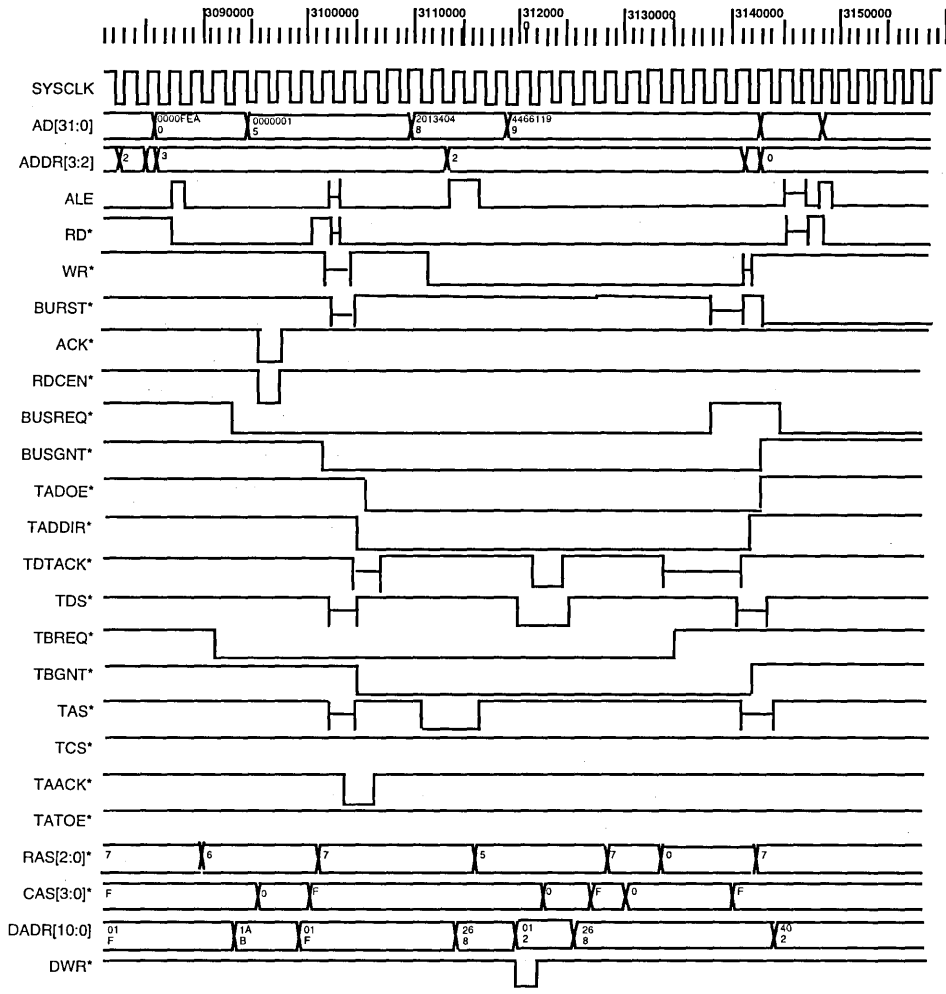
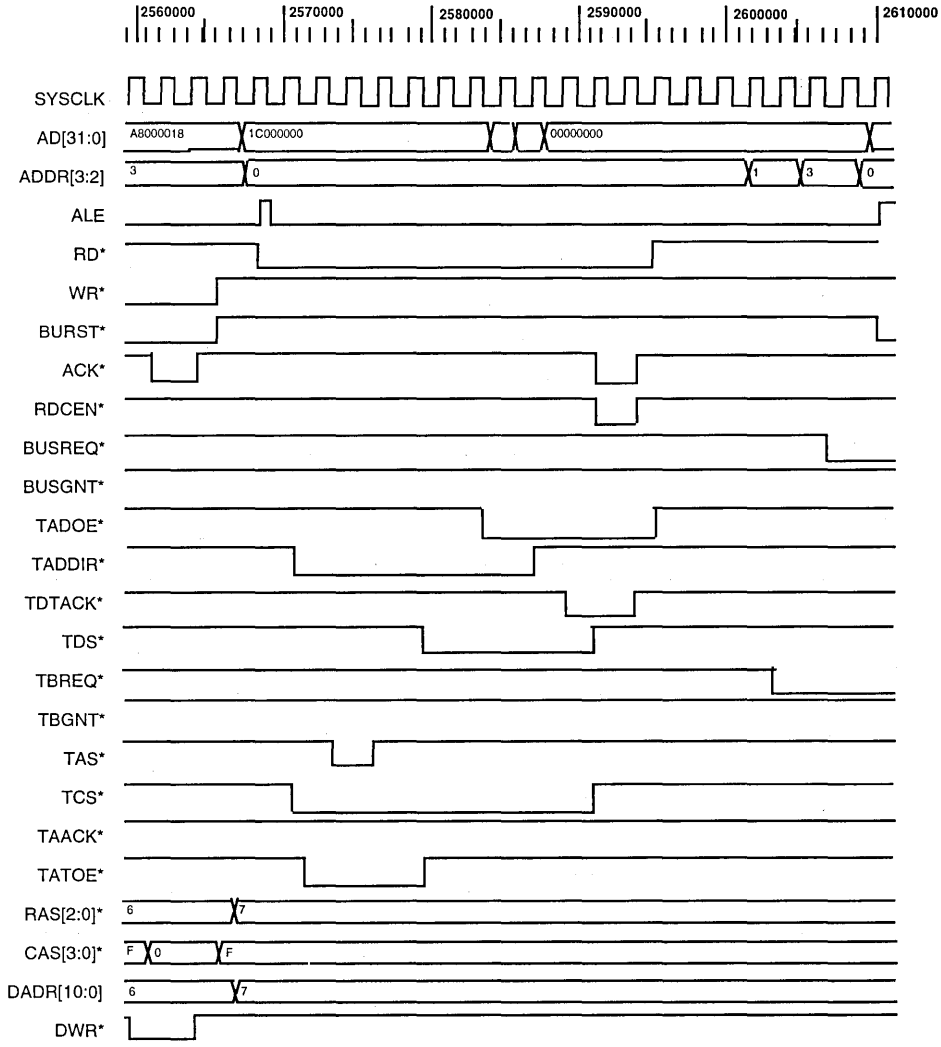
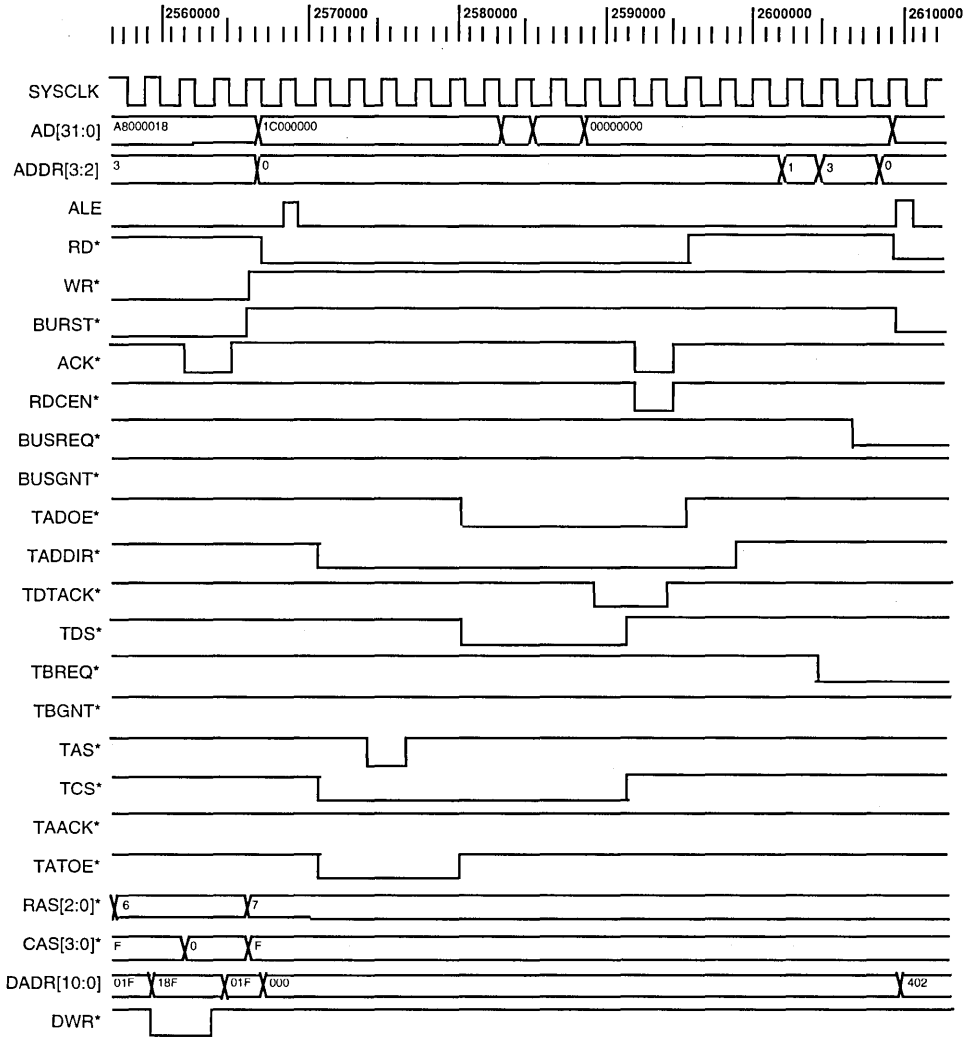


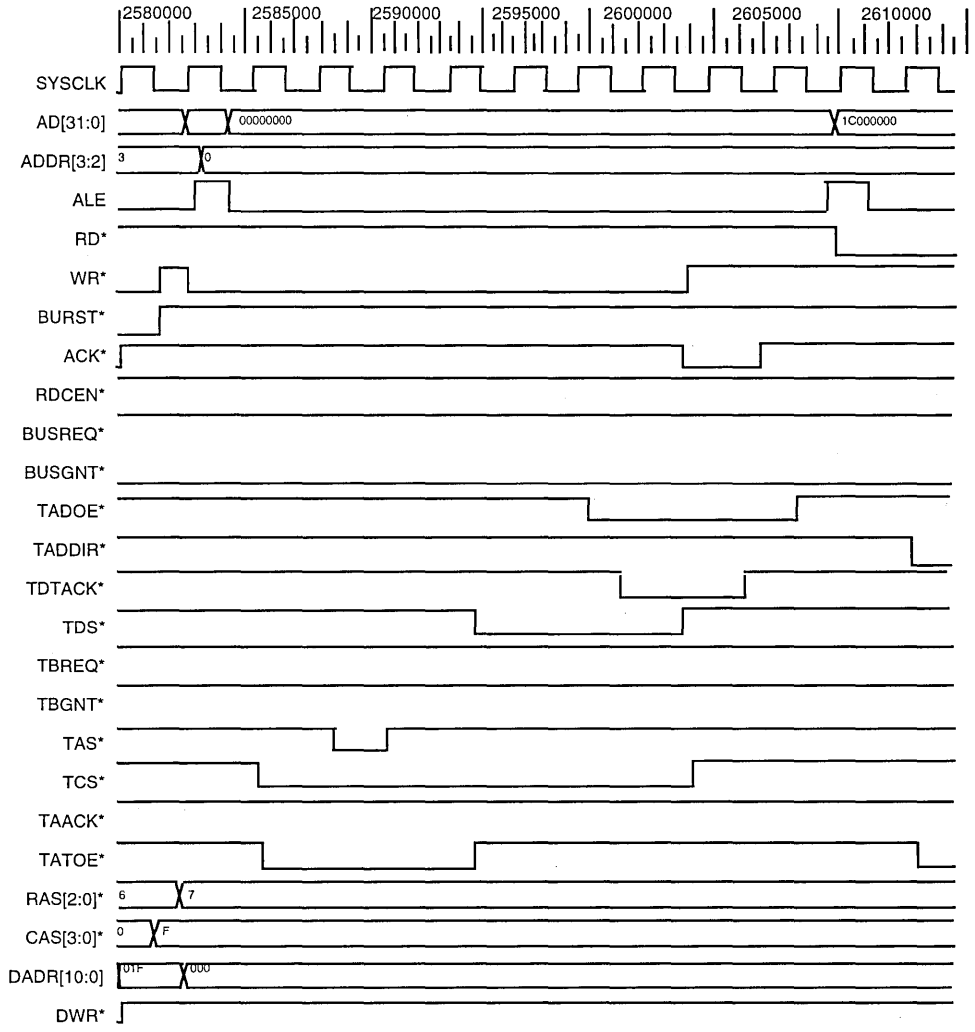
Typhoon Master Write—R3740



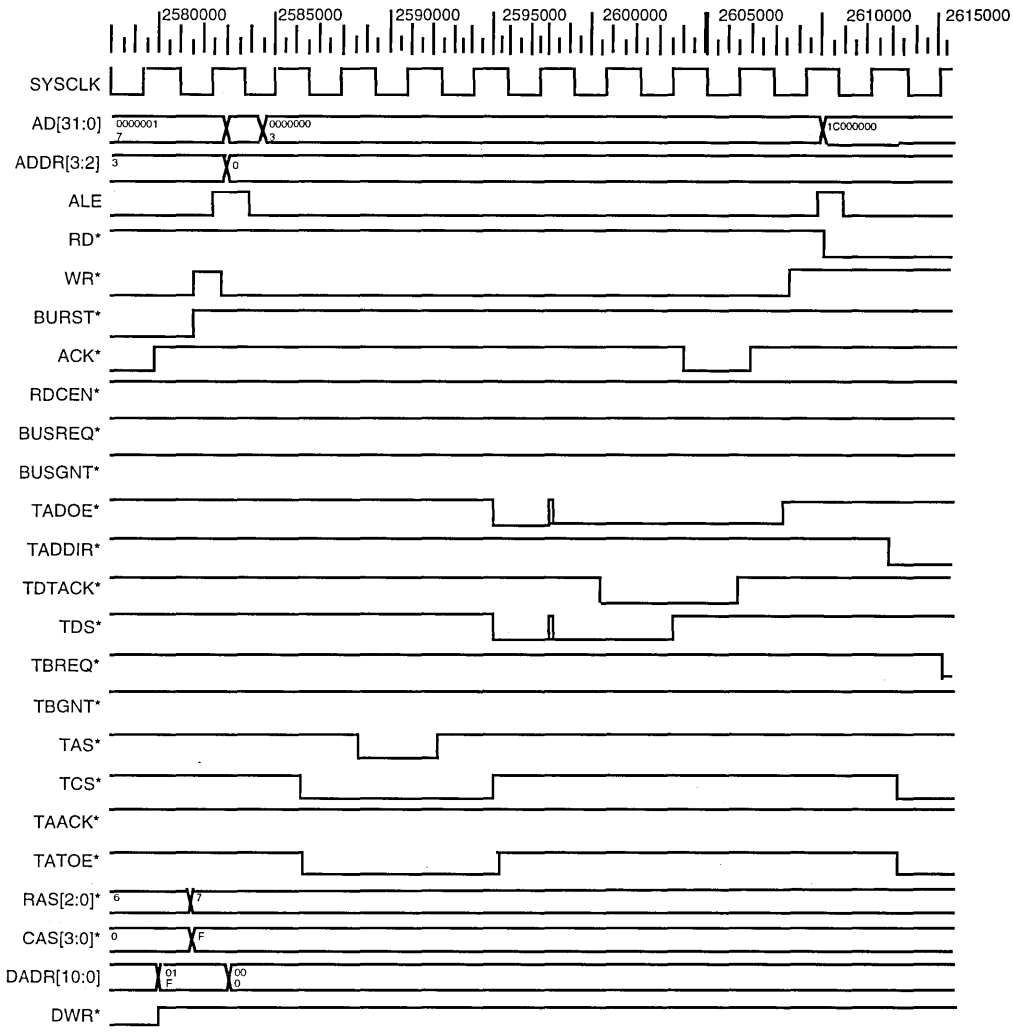
Typhoon Slave Read—R3710



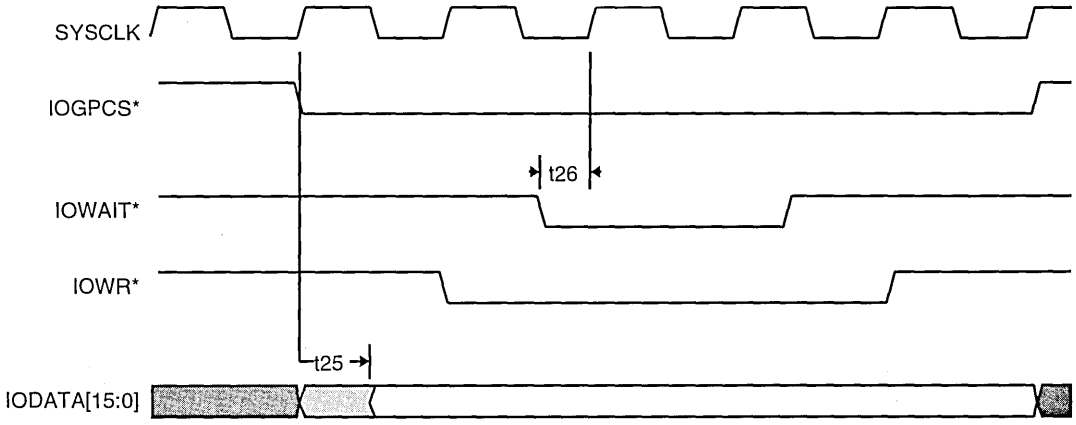
Typhoon Slave Read—R3740



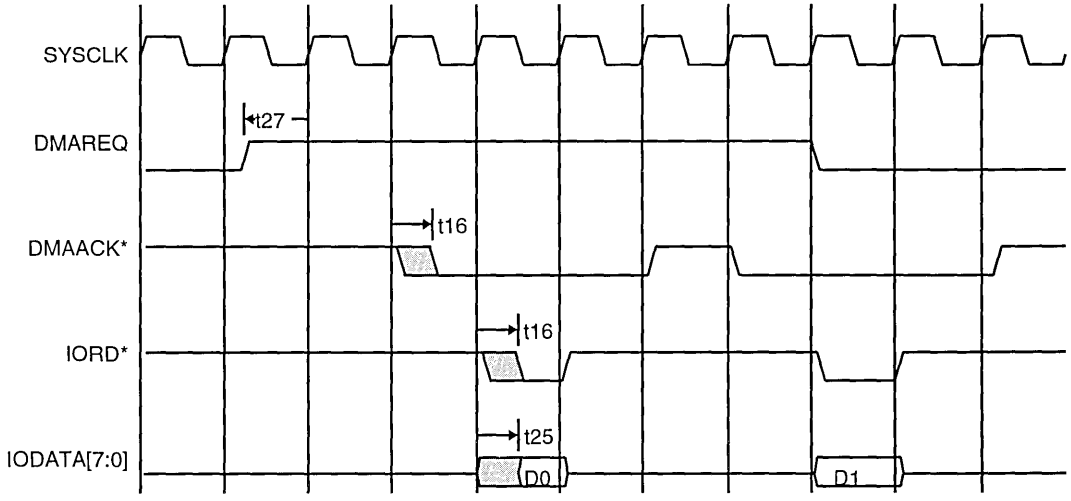
Typhoon Slave Write—R3710



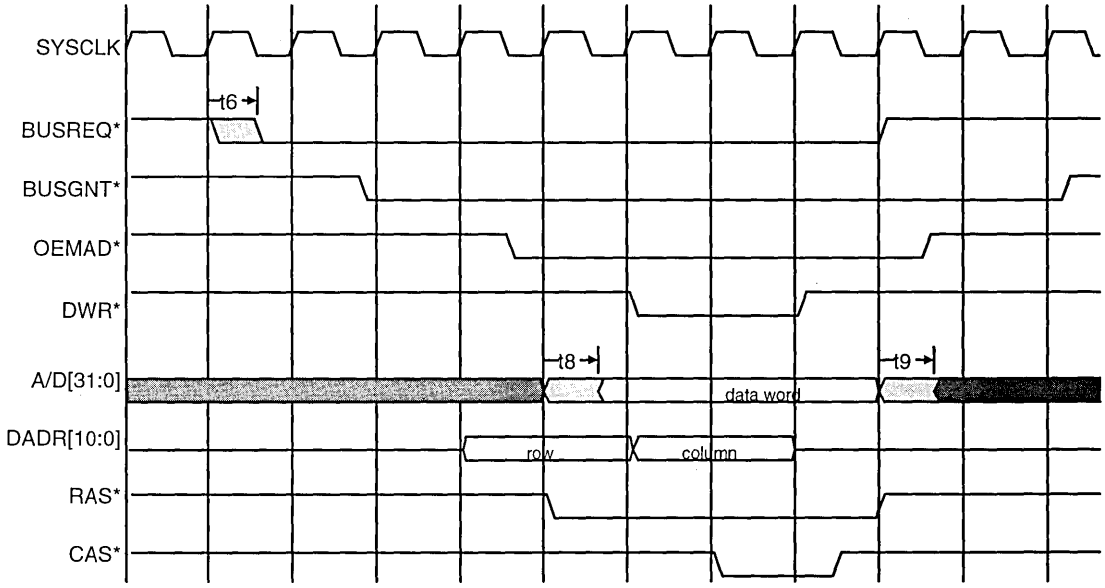
Typhoon Slave Write—R3740



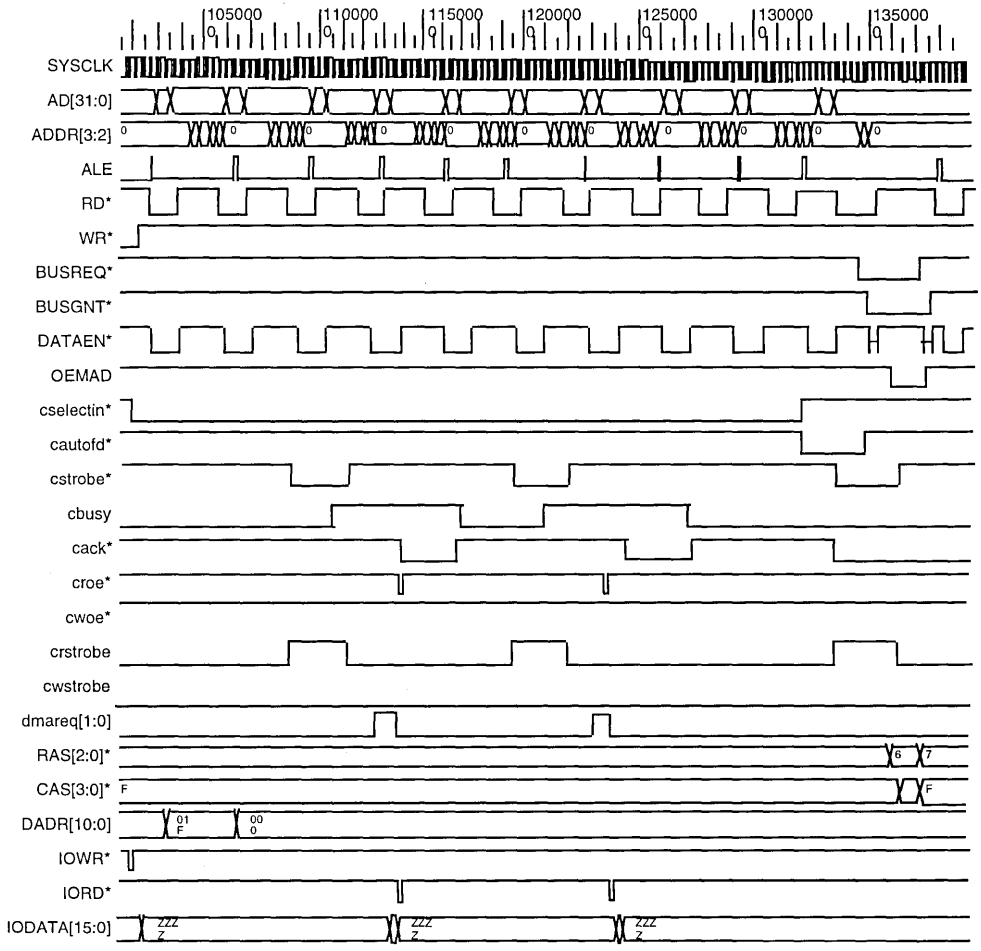
I/O Write (With Wait State)



I/O Bus DMA Read

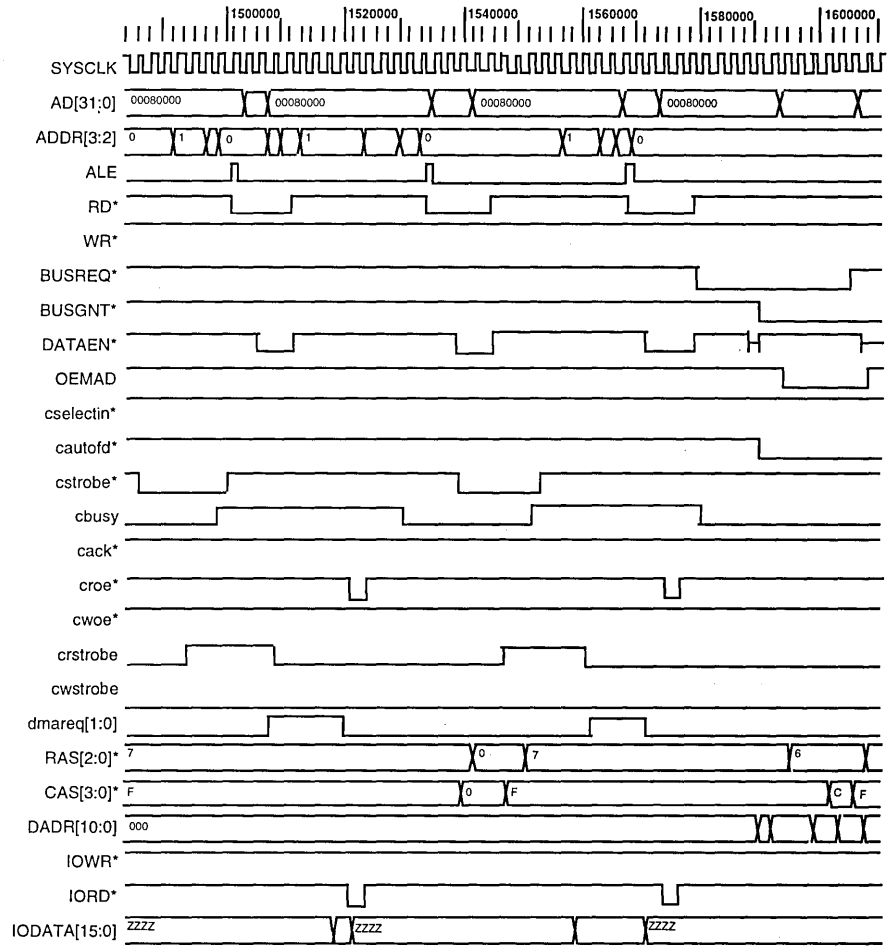


A/D Bus DMA Write

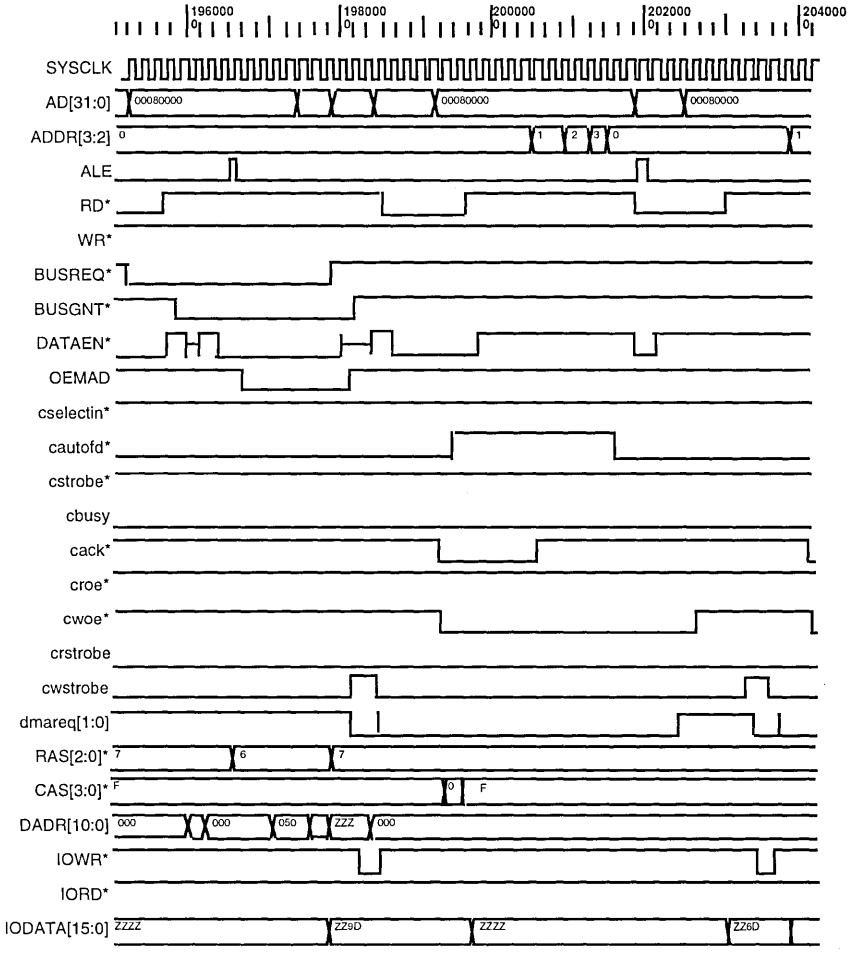


Centronics Compatible DMA—Standard

(Application=00)



ECP Forward Transfer



ECP Reverse Transfer

PACKAGE

160-Pin Quad Flat Package (QFP, EIAJ)

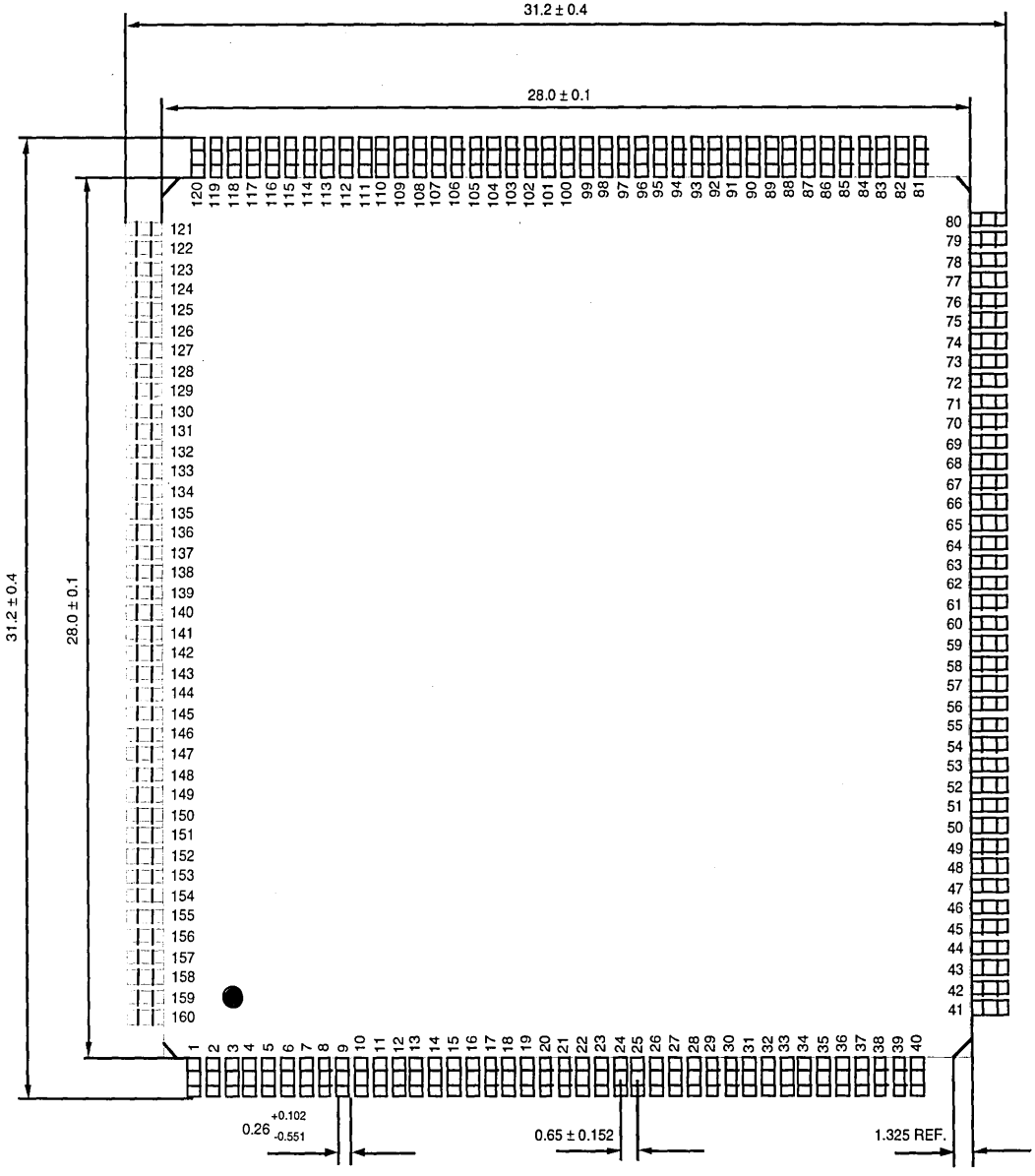


Figure 10.1: 160-Pin Quad Flat Package

3134 drw 03

160 - Pin Quad Flat Package—Expanded View (QFP, EIAJ)

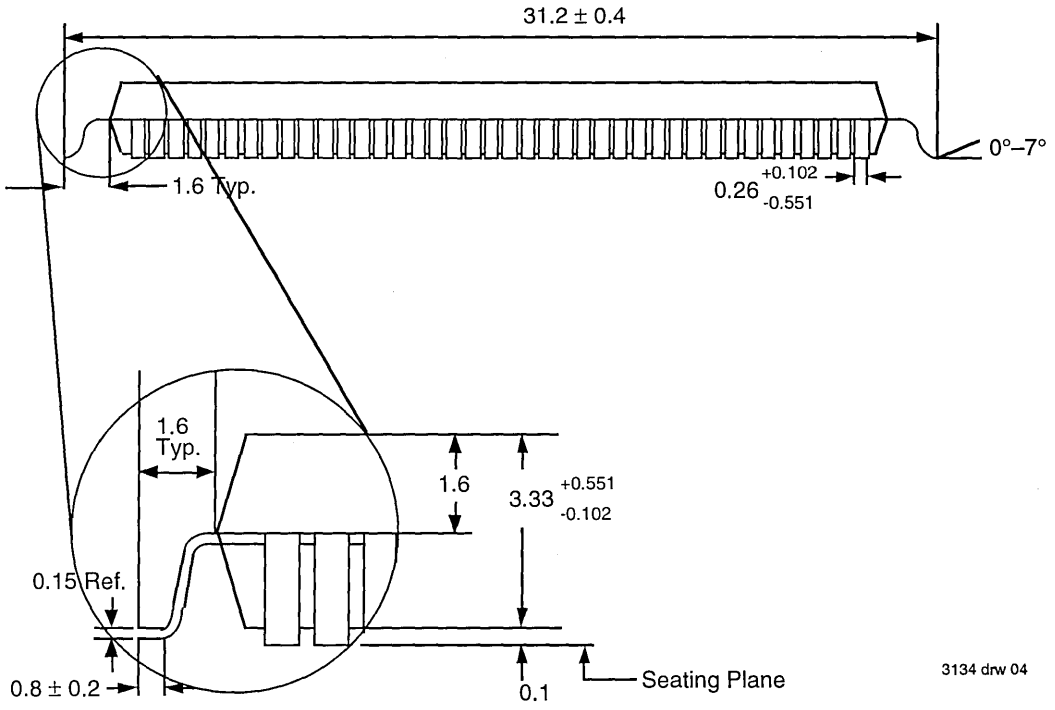


Figure 10.2: Expanded View

ORDERING INFORMATION

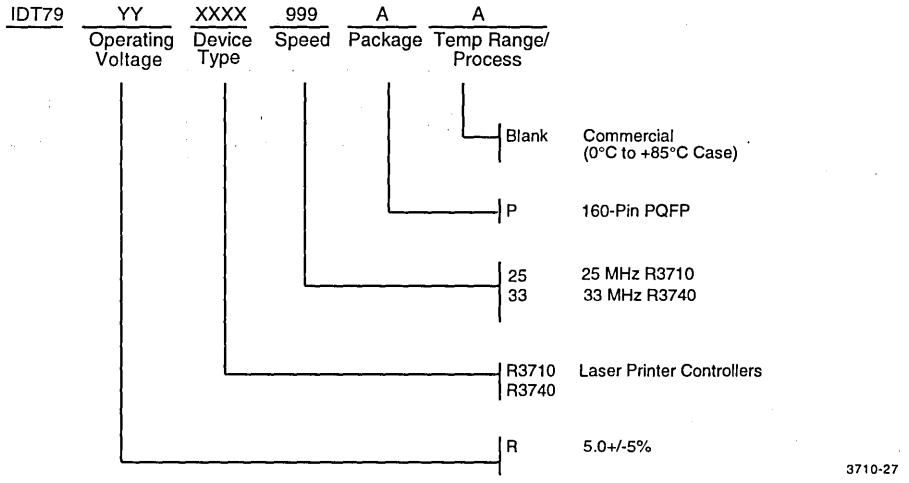


Figure 11.1: Ordering Information

Integrated Device Technology, Inc.

R4761 ORION Family Memory and I/O Controller

ORION
IDT79R4761™
Product Brief

FEATURES:

- Direct interface to IDT ORION R4600/R4700/R4650 RISC processors
  - 64-Bit interface support for R4600/R4700/R4650
  - 32-Bit interface support for R4650
- 50 MHz bus frequency
- 1 Gbyte address space
  - Flexible DRAM interface
  - Direct interface to 512 Mbytes
  - Available two-way interleaving
  - Transparent refresh
  - Supports 16 Mbit DRAMs
  - Individually programmable timing parameters,bank sizes
- RS-232 serial port (16450 UART)
- Flexible ROM/SRAM interface
  - Direct interface to 64 Mbytes
  - Available two-way interleaving
  - Each bank can be ROM, SRAM, or Flash ROM
  - Individually programmable timing parameters and bank sizes
- Serial EEPROM interface
  - Reads 256 configuration bits at power-on
  - Reads 8- and 16-bit random values
- Peripheral interface
  - Four ports total
  - Three ports configurable as DMA
  - "Smart" DMA support
  - External intelligent agent (e.g. R4762) interface support
  - Single and demand DMA protocol
  - Two "queued" DMA channels
  - Programmable timing parameters
- Memory-to-memory DMA channel
- Interrupt controller/prioritizer
  - Eight interrupt levels
  - Fixed or rotating prioritization
- Packaged in 208 PQFP

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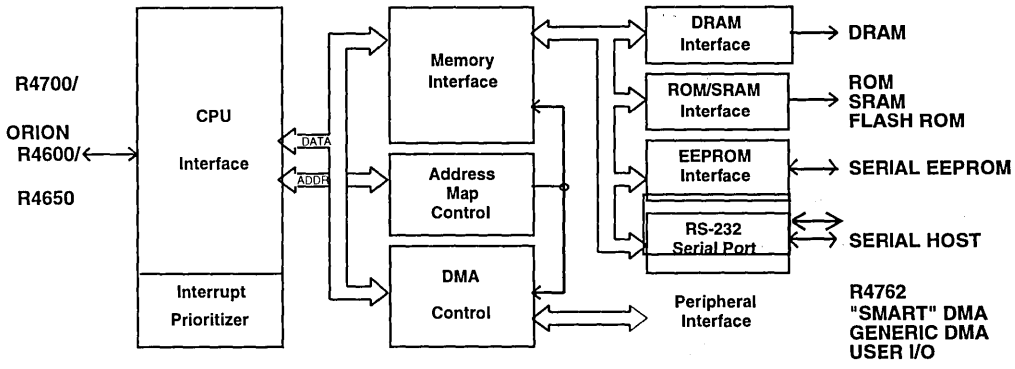

FIGURE 1: 4761 BLOCK DIAGRAM

DESCRIPTION:

The IDT79R4761 is a high performance memory/peripheral controller for the IDT R4600, R4700, and R4650 RISC microprocessors. The on-chip functions include: an Orion/R4650 interface, an R4762 interface, a serial EEPROM controller, a DRAM controller, a ROM/SRAM controller, a peripheral interface with DMA capability, an interrupt controller/prioritizer, and a serial interface (UART).

CPU Interface

The CPU interface connects directly to the Orion R4600/R4700 and R4650 processors. The 32-bit bus mode of the R4650 is supported. R4000 compatible write mode and write re-issue modes are supported. All bus arbitration functions for the system are managed by R4761, including those involving the SX-12 device. A single interrupt to the CPU is provided from the interrupt prioritizer. Boot-mode initialization from the EEPROM is handled totally by R4761, in conjunction with an external low-cost PAL, and can be expanded for future CPU versions.

R4762 Interface

The R4762 interface connects directly to the R4762 PCI Bridge device. CPU access of R4762/PCI address space and R4762 access of system DRAM are supported. R4762 DMA transfers to DRAM up to 64 bytes are supported.

Serial EEPROM Interface

The serial EEPROM interface reads the 256-bit initialization stream from a standard 2K-byte serial EEPROM at system power-on and cold resets. An external PAL assists in the sequence, allowing the R4761 to buffer only the first 16 bits. Once initialization is complete, the CPU can read 8- or 16-bit values from the EEPROM.

Memory Controllers

The memory controllers in the R4761 are flexible and efficient. The DRAM controller directly interfaces to four noninterleaved banks or two interleaved banks, up to a maximum of 512 MBytes. DRAM word depths up to 16M are supported, and each bank can have a different word depth. Programmable timing parameters control the RAS-CAS and refresh timing. Both concurrent and staggered CAS-before-RAS refresh are supported. Sustained zero-wait state transfers are possible with interleaving, while noninterleaved configurations use at least 1 wait state.

ROM/SRAM Controller

The ROM/SRAM controller also controls four noninterleaved banks or two interleaved banks, up to a maximum of 64 MBytes. Word depths from 16K to 2M are allowed. Each bank can be read-only ROM, Flash ROM, or SRAM, and each has its own word depth and timing parameters. Interleaved banks can be intermixed with noninterleaved banks. Interleaving allows zero-wait state sustained transfers.

Peripheral Interface

A flexible peripheral interface provides four multi-function ports for external devices using synchronous signal protocols. All ports can be configured as user I/O, with edge- or level-sensitive interrupt capability on inputs. Port0 can support the R4762 device. Three of the ports can be configured for direct memory access (DMA), including one "smart" peripheral that can use either Intel and Motorola bus arbitration. An internal memory-to-memory DMA channel is also included. DMA devices can transfer to/from DRAM or ROM/SRAM at the full memory transfer rate (one doubleword per clock for interleaved configurations), and can be selected for single-transfer or demand-transfer mode. Two of the DMA channels have an alternate address pointer, allowing queued buffer applications. The R4761 performs DMA arbitration using fixed or rotating priority.

Serial Interface

A serial interface compatible with a 16450 UART is included. The baud rate input clock can be selectively prescaled by 16, allowing flexibility in fine-tuning the exact frequencies desired. Baud rates from 50 to 38.5K bits per second are possible.

Interrupt Controller

An eight-level interrupt controller is also contained in the R4761. Each of the four peripheral ports, plus the memory-to-memory DMA channel, UART, and internal R4761 exceptions make up the eight levels. Two prioritization methods are available: fixed and rotating. A single interrupt signal is provided to the CPU.

Integrated Device Technology, Inc.

PCI-to-Orion Bus Bridge

ORION

IDT79R4762

Product Brief

FEATURES

- Glue-less bridge between Orion family, including R4600, R4700, R4650, and 32-bit PCI
- Extensive use of internal buffering de-couples PCI and local-bus latencies
  - 64-byte CPU write to PCI FIFO
  - 32-byte CPU read from PCI FIFO
  - 128-byte local memory access FIFO
  - 32-byte DMA FIFO
- Simple interface to external Orion family local-bus memory controller
- Supports 32-bit (e.g. R4650) or 64-bit CPU bus modes to 50MHz
- Supports 32-bit PCI to 33 MHz
- Functions for host or adapter-card PCI bridges
- Interrupt generation capability
- On-chip DMA controller
- Programmable memory mapping
- Host arbiter functions on chip:
  - 5 master arbitration
  - Programmable fixed or round-robin priority scheme
  - Host bridge parking, when there is no bus owner
  - Configuration support
  - Moves data between PCI and local memory
  - Supports both chaining and non-chaining operation
  - Scatter-gather support
- Optional byte-swapper function between PCI and local bus
- Packaged in 208-pin QFP

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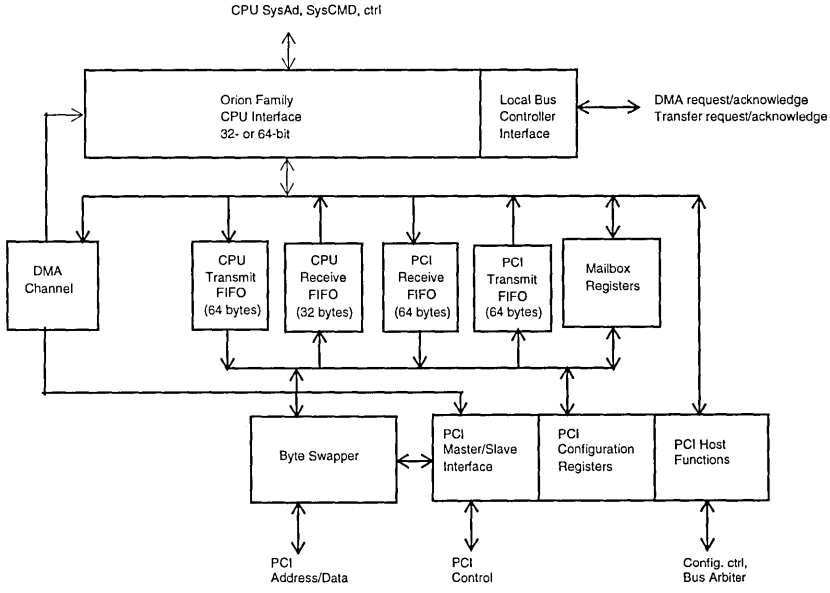

FIGURE 1: R4762 BLOCK DIAGRAM

DESCRIPTION:

The IDT79R4762 is designed to provide a simple low-cost bridge between an Orion family CPU, its local memory resources, and the PCI bus. The R4762 can be used in systems implementing an Orion family CPU on a PCI add-in adapter card, or in systems implementing an Orion CPU as the host off a PCI-based system.

The R4762 is designed to mate the PCI bus effectively with an Orion family CPU. Although PCI offers high bandwidth and relatively low latency, the Orion family offers significantly higher bandwidth. The R4762 has been designed to de-couple the speeds of the two buses and incorporates a significant amount of FIFO logic to mate the bandwidth and latency requirements of the two busses.

This product brief is intended to provide an overview of capabilities on the R4762 PCI bridge. A block diagram of the R4762 is included on page 1.

PCI Interface Features

The R4762 is a fairly high-performance PCI interface chip, consistent with the class of CPU being bridged to PCI. It also supports the generation of back-to-back cycles, to maximize PCI bandwidth. The R4762 does not perform "address stepping" as a bus master, but the R4762 does respond to PCI bus requests with "medium speed DEVSEL" timing.

The R4762 PCI interface implements a pair of "mail box" registers: one for local bus to PCI and the other for PCI to local bus, when an agent on one side writes to the appropriate mail box and interrupt is signalled to the other side.

In addition, the R4762 implements a "latency timer" for the PCI bus. If the transaction is not completed within the time-out period, the R4762 will signal a PCI disconnect, causing the transaction to be re-tried later. After an appropriate number of re-tries has been attempted and the transaction remains uncompleted, an error condition is signalled and the transaction aborted.

Since the MIPS architecture is purely memory based (rather than memory and I/O spaces), the R4762 divides a portion of the memory address space into the following sub-sections: PCI-memory, PCI-I/O, PCI-configuration, and Internal R4762 register space. Burst accesses are supported only to memory.

PCI Master Mode Operation

As a PCI master, the R4762 can generate memory,I/O, or configuration cycles for direct local to PCI bus accesses. Memory read, memory write, memory read multiple, and memory read line cycles are supported.

If the local bus address maps to the PCI I/O space, as a PCI master, the R4762 generates a PCI I/O cycle. Similarly, accesses mapped to the PCI bus configuration space will generate configuration cycles.

PCI Target Mode Operation

As a PCI target, the R4762 allows access to its internal registers and to the Orion local bus, with the following commands: I/O read, I/O write, memory read, memory write, memory read multiple, memory read line, memory write, and invalidate. The R4762 supports read or write access of byte, word, or long-word size. Using an address generated from an internal I/O base register, for PCI I/O accesses, the R4762 will generate local bus memory cycles. The R4762 can also perform target initiated terminations such as retry, disconnects, and target-abort.

PCI Configuration Support

The R4762 includes an internal configuration space, which meets the requirements for a host bridge. In "host mode," the R4762 is configurable by the Orion-family processor. In addition, the R4762 can generate configuration cycles; it supports both "type 0" and "type 1" configuration cycles, using mechanism #1. In "target mode," the R4762 is configurable from the PCI bus.

Local Bus Writes to PCI

The master transmit buffer provides a write buffer for host writes to the CPU. This allows the CPU to issue the write command, address, and data at maximum speed, even though the PCI latency can be longer. The transmit buffer is 2 cache lines deep; therefore, up to two CPU write commands can be buffered without incurring CPU stalls. Errors that may occur during PCI writes are reported back to the CPU using a general interrupt.

Local Bus Reads from PCI

The R4762 implements a number of features to insure memory coherency and to avoid deadlocks on the PCI bus. To insure memory coherency, the R4762 processes all pending PCI writes before processing a host read to the PCI bus. To avoid deadlocks, if the CPU is awaiting a read transaction across the PCI bus, the R4762 signals a RETRY back to other PCI masters attempting to read the CPU local memory.

Various factors dictate the architecture of the master receive FIFO buffer of the R4762:

- The Orion family processes cache misses using sub-block (burst order), while not all memory systems support this sequence. Thus, the R4762 processes cache fill requests as a sequential read of 8 words and picks the data out in the correct order to return it to the CPU.
- Since the PCI bus allows multi-word transfers to be broken off by the target, the R4762 implements a local memory bi-directional FIFO capable of buffering an entire cache line. Thus, a processor request such as a burst read can be processed as multiple PCI reads.

PCI Write to Local Bus

The R4762 target write buffer is designed to buffer more than one PCI write transaction, allowing the bus to be freed while the actual write occurs on the CPU local bus.

To insure memory coherency, target writes are completed before PCI reads of the local bus are processed. To insure bus efficiency, a retry is signaled to the PCI bus, in this case, to allow the bus to be freed for other uses until the target writes are retired.

PCI Read from Local Bus

If the local bus is free, the R4762 will pre-fetch up to one cache line from the local bus memory and save this data in the local memory FIFO. This data is immediately provided to the PCI bus; meanwhile, the R4762 will pre-fetch an additional cache line and save this in the FIFO. Thus, burst transfers larger than the cache line size (e.g. ATM cells of 48 bytes) can occur at true PCI speeds. If the read terminates before the data in the FIFO is exhausted, the data is flushed from the FIFO.

Note that the R4762 assumes that the local bus memory will process DMA requests using a sequential data ordering algorithm. Although the R4762 will issue the same cache line read command as an Orion CPU will for a cache line, the R4762 expects data to be returned starting with the word requested and then sequentially until the end of the line. This is done to minimize PCI latency. Sub-block ordering would cause the R4762 to await data from the local memory controller which the PCI bus can never use.

DMA Controller

In addition to providing data buffering between the local bus and the PCI bus, the R4762 includes an on-chip DMA controller to facilitate data movement between the buses. The R4762 DMA controller is a single-channel controller that can perform chaining or non-chaining. Scatter-gather capability is supported.

The R4762 is programmed with the command location in memory. When DMA is started, the R4762 DMAs the control block from memory, which causes the appropriate transfers to begin. When this control block is processed, the R4762 will DMA the next control block from memory (the location of this next control block is a parameter in the first block). This will continue until it completes a control block with an "end-of-chain" flag set. The DMA controller has its own FIFO.

To share the local and PCI bus resources with the rest of the system, the R4762 implements a set of rules to allow other agents to access these busses during DMA transfer.

Local Bus Controller Interface

The R4762 uses a simple interface to the Orion local bus memory controller. Figure 1 shows a typical system implementation of an R4762-based adapter card. For a host-based application, the processor sub-system would look similar.

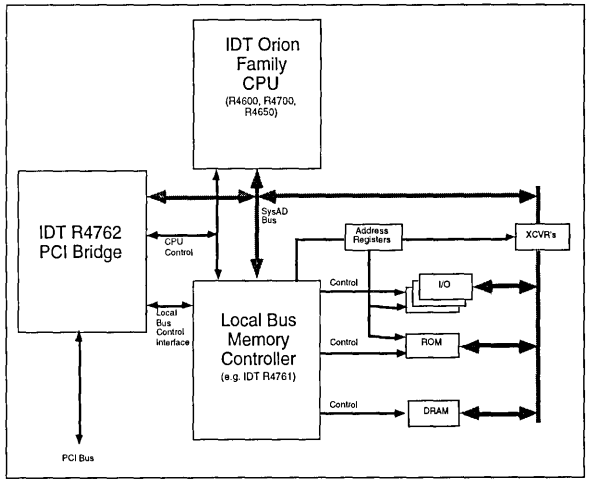

Figure 2: PCI Adapter Card built with R4762

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Integrated Device Technology, Inc.

RISC DEVELOPMENT SUPPORT PRODUCTS

INTRODUCTION

For engineers developing software and hardware products around the IDT79R3000 and IDT79R4000 Instruction Set Architecture (ISA), which includes the IDT79R30xx families of RISControllers and the R4000 Orion Family. IDT offers three software products and several prototyping and evaluation systems. This catalog primarily focuses on products manufactured and sold directly by Integrated Device Technology.

SOFTWARE PRODUCTS

IDT/c—IDT's optimizing ANSI C-compiler. This compiler, which uses the GNU C front end, includes full ANSI C compatibility and highly efficient floating point emulation libraries for IDT79R30xx-based systems (without hardware floating point) and IDT79R4650-based systems. A unique debug control scripting language makes it easy to locate hardware problems that occur only under rare conditions. IDT/c includes the compiler, optimizer, assembler, linker, librarian, C libraries, Floating Point Libraries, and symbolic debugger.

IDT/sim—IDT/sim is IDT's System Integration Manager, used to bring up new hardware and to support the symbolic debug in both the MIPS and IDT C compilers. IDT/sim is a ROMable debug kernal with extensive diagnostics built-in. It is supplied in EPROM on all IDT prototyping boards, and is available in source code for use with either the MIPS or IDT C Compilers.

IDT/kit—IDT/kit, the Kernel Integration ToolKit, contains source code and compiled versions of a complete set of routines for initializing systems, servicing interrupts, handling floating point exceptions, and so forth. Also included is source code for ANSI libraries, for the Floating Point Emulation Libraries and for transcendental functions.

PROTOTYPING SYSTEMS

Completely assembled and tested hardware systems are available for prototyping and initial software porting. All systems include a CPU, serial I/O, EPROM containing the IDT/sim monitor, and some amount of RAM. These systems have provision for simple addition of user-defined hardware. Units are available which support the IDT79R30xx and IDT79R4xxx families.

For laser printer controllers, the IDT79S389A Reference Platform provides a ready prototyping target for R30xx Family laser printer controllers using PostScript Level 2 software from Adobe.

THIRD PARTY DEVELOPMENT TOOLS

The increasing popularity of IDT's RISC microprocessors has resulted in a dramatic increase in the number of third party tools available. For information on these products, contact your local IDT sales representative.

- Real-Time Operating Systems from Lynx, Wind River, Accelerated Technology and Integrated Systems, Inc.
- Compilers from MIPS, Green Hills, BSO Tasking, Cygnus Support and Embedded Performance, Inc.
- VME Boards from CES, RISQ Modular Systems, Omnibyte, Densan, Heurikon
- Device Simulation Models from Zycad, HDL, CAE Technology and Synopsys
- Peripheral Support Circuits from Chrysalis Research, DeskStation Technology, Galileo Technology, and Mentor ARC, Inc.
- Page Description Language interpreters from Adobe Systems, PCPI, Phoenix Technology, Inc. Pipeline Associates, Inc and Rastek, Inc.
- In-Circuit Emulators from Embedded Performance, Inc. and Topmax, Inc.
- Logic Analyzer support from Hewlett-Packard and Tektronix

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Integrated Device Technology, Inc.

THIRD-PARTY DEVELOPMENT TOOLS AND APPLICATIONS SOFTWARE FOR IDT RISC PROCESSORS

OVERVIEW

The MIPS/IDT RISC Microprocessor family is supported by a wide variety of third-party development tools and applications software. Many of these tools are software products, useful across the entire line of processors; others of these are hardware development tools, appropriate for one or two members of the family.

As the MIPS architecture is increasingly popular and successful, many new tools are constantly being announced. IDT encourages our customers to work closely with their local sales representative for a current list of third party support. This listing is current as of the date of this document.

Product Name	Vendor	Phone	FAX
Software Development Tools			
Nucleus:DBUG/DBUG+, PC	Accelerated Technology	334-661-5770	334-661-5788
XoftWare-System Software	AGE Logic, Inc.	619-755-1000	619-755-3998
SDE-MIPS	Algorithmics, Ltd.	011-44-171-700-3301	011-44-171-700-3400
R3000 Cross-Development Package	BSO/Tasking, Inc.	617-320-9400	617-320-9212
UDB-Universal Source DB	CaseTools, Inc.	408-685-0336	408-685-0312
Compilers, Cross Development Sys.	Cygnus Support	415-903-1400	415-903-0122
Model CCE3K-SW Tools	Embedded Performance	408-434-2210	408-435-7800
Compilers, Development SW	Green Hills Software, Inc.	617-862-2002	617-862-2427
IDT/c, IDT/sim	IDT	408-492-8208	408-492-8469
R3000/R4000 Compilers	MIPS Technologies, Inc.	415-390-4170	415-390-6170
StethoScope, WINDVIEW	Wind River Systems, Inc.	510-748-4100	510-814-2011
Software Libraries			
Nucleus FILE, Nucleus Net	Accelerated Technology	334-661-5770	334-661-5788
IDT/kit (IDT79S909)	IDT	408-492-8208	408-492-8469
VDS Kit-Video Library	Performance Computing, Inc.	503-641-1221	503-641-3344
USFiles, USNet	U.S. Software	503-641-8446	503-644-2413
Ada Development Tools			
DACS MIPS Ada CC System	DDC-I	602-275-7172	602-275-7502
ADA Compiler	Green Hills Software	617-862-2002	617-862-2427
VADS-Ada System	Rational Corporation	408-496-3600	408-496-3636
RISCADA Development System	Thompson Software Prod.	619-457-2700	619-452-2117
Real-Time Operating Systems			
Nucleus Plus, Nucleus RTX	Accelerated Technology	334-661-5770	334-661-5788
QUITOS	Advanced Real Time Systems	011-33-1-64589090	011-33-1-64589149
CHORUS CLASSIX	Chorus Systems	408-879-4100	408-879-4102
MULTI Debug Servers	Green Hills Software, Inc.	617-862-2002	617-862-2427
pSOSystem/MIPS	Integrated Systems, Inc.-ISI	408-980-1500	408-980-0400
C-Executive, PSX	JMI Software System, Inc.	215-628-0840	215-628-0353
AMX3000	Kadak Products Ltd.	604-734-2796	604-734-8114
LynxOS	Lynx Real-Time Systems	408-354-7770	408-354-7085
MultiTask	U.S. Software	503-641-8446	503-644-2413
UniPlus +	Unisoft Corp.	415-794-2666	415-794-2668
VxWorks 5.1 RTOS	Wind River Systems, Inc.	510-748-4100	510-814-2011

Product Name	Vendor	Phone	FAX
Logic Analyzers			
ML-4400 Logic Analyzer	American Arium	714-731-1661	714-731-6344
CLAS 4000 Logic Analyzer	Biomation	408-434-2210	408-435-7970
PIXXXX Logic Analyzer PP	Corelis	310-926-6727	310-404-6196
HP-16500 Logic Analysis System	Hewlett-Packard Co.	800-452-4844	
DAS9200, Model 32GPX	Tektronix, Inc.	800-426-2200	413-448-8003
In-Circuit Emulators			
ICEMAN 3041, SYS-R3051	Embedded Performance, Inc.	408-434-2210	408-435-7970
TMax 5501-30xx Emulator	Topmax	602-730-2530	602-730-2550
NetROM ROM Emulator	XLNT Designs, Inc.	619-487-9320	619-487-9768
Evaluation Boards			
P-4000i	Algorithmics Ltd.	011-44-71-700-3301	011-44-71-700-3400
CMA Universal Development Systems	Cogent Engineering	508-632-2020	508-632-1211
VME Boards	Creative Electronics (CES)	011-41-022-7925745	011-41-022-7925748
Evaluation Kits	IDT	408-492-8208	408-492-8469
Prometheus 4600	Integrated Real-Time Systems	408-241-4950	
PULSAR 3000 VME board	Omnibyte Corporation	708-231-6880	708-231-7042
RISQengine Computer Boards	RISQ Modular Systems	510-490-0732	510-490-7225
Nitro-VLB Booster	ShaBLAMM! Computer, Inc.	408-730-9696	408-730-4940
RISC 4X00 CPU Boards	Siemens Nixdorf (SNI)	011-33-1-34819227	011-33-1-34819667
SLOTSAVER 3000	Vigilant Technologies, Inc.	305-680-6759	305-434-9048
Simulation Tools/Models			
Verilog Models for R4XXX	CAE Technology, Inc.	408-526-9207	408-526-9308
VHDL models for R30XX	Chrysalis Research Corp.	617-371-9115	617-371-9175
SOFT•RISC Verilog Models	HDL Systems Corp.	408-522-2600	408-522-2626
Logic Modeling	Synopsys Logic Modeling	503-690-6900	503-690-6906
Model Bank	Zycad Corporation	201-347-7900	201-347-8525
Support Components			
IDT R3715, R3740	IDT	800-345-7015	408-492-8674
RXI--RXD Chipset	Chrysalis	617-271-0943	617-275-4461
LogiCore Chipset	DeskStation Technology	913-599-1900	913-599-4024
Galileo-2, Galileo-3, ...	Galileo Technology, Inc.	408-451-1400	408-451-1404
WINset-PCI Rx00, VL R4x00	Mentor ARC, Inc.	510-656-0100	510-656-3246
Consulting/Design Services			
Design Services	Chrysalis Research Corp.	508-371-9115	508-371-9175
Software Development Class	Embedded Performance, Inc.	408-434-2210	408-435-7970
Training Class	IDT	408-492-8208	408-492-8469
Design, Development Mfg.	IDT RISC Subsystems Div.	408-492-5668	408-988-5600
Hardware/Software Design	RISQ Modular Systems, Inc.	510-490-0732	510-490-7225
Consulting/Design Services	Topmax	602-730-2530	602-730-2550
Page Description Languages			
Adobe Postscript Software	Adobe Systems, Inc.	415-961-4400	415-961-3769
IDT79S389 Reference Plt.	IDT	408-492-8208	408-492-8469
Postscript Porting Services	PCPI	619-485-8411	619-487-5809
Peerless Page	Peerless Systems Corp.	310-536-0908	310-297-3264
Phoenix Page	Phoenix Technologies, Ltd.	617-551-5030	617-661-4802
PowerPage Level 2, PCL 5x	Pipeline Associates	201-267-3840	201-267-3715
Mirror_5E-PCL Emulation	Rastek Corporation	205-882-0882	205-882-0238

Integrated Device Technology, Inc.

TRAINING CLASS-

Applications Development with the IDT R3041, R3051, R3052, R3071, R3081 RISControllers and R4600, R4700 and R4650 Orion Family

OVERVIEW

IDT offers a training class intended to provide in-depth knowledge on the use and capabilities of the 32-bit R30xx RISControllers and the 64-bit R4xxx Processors. The class is intended to provide an accurate basis for device evaluation, as well as to provide a design engineer with the ability to rapidly bring an application based on IDT parts to production.

The class is intended for engineers who are designing with the IDT processor family, and who wish to minimize time to market. It is also appropriate for customers performing a detailed processor survey prior to device selection. The class covers both hardware as well as software issues.

COURSE CONTENTS

The course provides a detailed discussion, including hands-on workshops, on both the hardware and software considerations appropriate to applications which are either new development projects or porting projects from another architecture to IDT's RISC architecture. While the course does assume basic familiarity with hardware and software development, the course does not assume previous RISC training or experience.

The course prepares the participant to create designs around a RISController from the R30xx family as well as around the R4xxx (Orion) family, through detailed lectures and hands-on workshops and laboratory sessions. The programming environment is reviewed, as are various hardware price-performance trade-offs.

Major topics covered are CPU overview, pipeline scheduling, co-processor overview, floating point accelerator overview, 64-bit vs. 32-bit considerations, error checking, cache architecture, memory management unit, exception processing, compatibility issues, timing, IDT/c compiler tool-chain, source level debugger and utilities.

COURSE LOCATION AND SCHEDULE

The course is held on three consecutive days at the IDT facility in Santa Clara, California. Directions, accommodations, and schedule information is available from your local sales representative.

DAY 1

MIPS Architecture Overview
- CPU Integer Unit
- Floating Point Accelerator
- System Control Co-Processor
- On-chip Caches
- System Interface
- Lab

Cache Architecture
- Cache Architecture
- Operation
- Flushing
- Performance
- Lab

Memory Management
- Overview
- Virtual to Physical Address Translation
- TLB Operation
- Lab

Exception Handling
- Precise Exception Model
- Exception Processing
- Software Techniques
- Exception Latency
- Special Techniques

DAY 2

R30xx System Interface
- Operations Priority
- Read Interface
- Write Interface
- DMA Interface

System Design Topics
- Input Clock Considerations
- System Clock State Machines
- Bus Turn Around
- Using Ack and RdCEn
- Lab

R4xxx System Interface
- Clock Generation
- Read Interface
- Write Interface
- DMA Interface
- System Design Topics
- Lab

DAY 3

IDT Tool Chains
- IDT Compiler & Libraries
- Important Compiler Options & Utilities
- High Level Language to Assembly Interface
- Getting a Prototype Running
- IDT Startup Module
- How to Service External Interrupt
- Floating Point Emulation

Software Lab
- Real/Emulation mode Floating Point
- Cached/Uncached Execution
- Debugging Exercises
- Unaligned Data Handling Exercises
- Inlining Assembly in C program
- Using Cache Ops to Speed Up Program

Integrated Device Technology, Inc.

CENTAURUS LASER PRINTER CONTROLLER IDT79S389 R3051™ FAMILY REFERENCE PLATFORM FOR PostScript™ Level 2 SOFTWARE FROM ADOBE®

FEATURES

- Software-ready laser printer controller suitable for Adobe OEMs developing PostScript Level 2 products
- IDT/Adobe demonstration platform for PostScript Level 2 software running on IDT's R3051 RISController™ family
- IDT/OEM R3041™/R3051/R3081™ based prototyping target and reference design (25MHz)
- Uses IDT79R3721 DRAM Controller and IDT73720 Bus Exchangers
- Options for two-way interleaved or non-interleaved (jumpers) DRAM memory system
  - Up to 16MB DRAM (four 72-pin sockets; 1MB or 4MB SIMMs)
  - 4 non-interleaved banks or 2 two-way interleaved banks
- Options for two-way interleaved or non-interleaved EPROM/ROM memory system
  - Up to 4MB ROM (8 32-pin sockets; 1, 2 or 4Mb EPROM/ROMs)
  - 2 non-interleaved banks or 1 two-way interleaved bank
- 512 bytes serial EEROM
- Programmable DUART (85C30) with RS232C and AppleTalk® ports
- SCSI Controller (53C80) with one SCSI port (2 connector locations)
- Centronics parallel input port
- Adobe reference front panel interface (based on Canon LBP-8 MARKIIIR 6-button/LCD/LED front panel)
- IDT FIFO-based Canon video interface to LBP-SX/RX engines
- Clock, reset and interrupt generation logic
- Expansion bus connector for:
  - Custom engine interfaces (600dpi, color, etc.)
  - Additional I/O (Ethernet, Adobe FAX, etc.)
  - Additional font ROM space
- Shipped with IDT/sim™ initialization and monitor debug software (PostScript EPROMs available from Adobe)
- Executes various Adobe software (provided only under license from Adobe Systems Incorporated), including:
  - Adobe's high-level and low-level monitors
  - Adobe Print Architecture
  - Adobe's PostScript Level 2 Interpreter

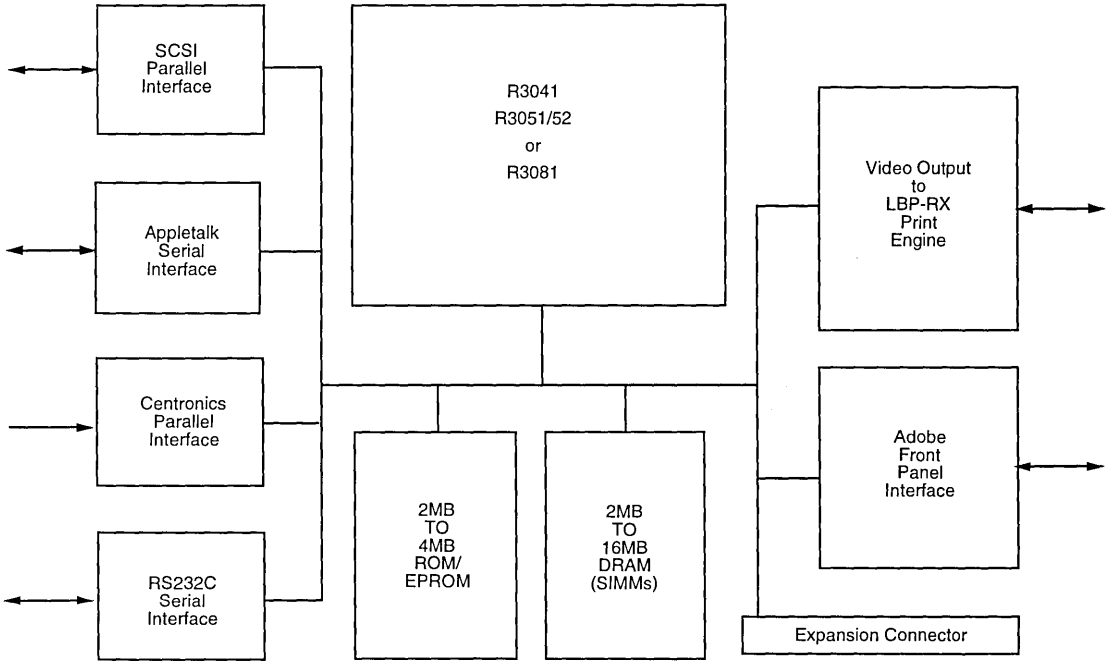


Figure 1. IDT79S389 Block Diagram

MARCH 1994

INTRODUCTION

The IDT79S389 provides an R3051 family laser printer controller reference platform for rapid adaptation into OEM differentiated products using PostScript Level 2 software from Adobe. "Reference platform" means that IDT and Adobe engineers have jointly developed both hardware and software modules for the specified configuration. This provides a baseline hardware and software design to accelerate time-to-market where changes can be limited to one or two areas (form factor, engine interface or I/O options), without having to start at the beginning.

Since the IDT R3051 family includes pin-compatible members with and without floating point accelerator hardware on chip, Adobe software licensees will be able to obtain "core PostScript" binaries in two versions: one compiled with the MIPS C-compiler assuming the presence of the FPA (for IDT79R3081), and another version based on IDT's floating point emulation libraries (for IDT79R3041, R3051 and R3052).

The IDT79S389 is completely self contained, and is intended for use either on the desktop, or installed inside a variety of Canon print engines; e.g. Canon OEM engines LBP-SX and LBP-RX, Canon LBP-8 MARKIIIR and HP LaserJet III. The IDT79S389 fits into any of the above engine mounting locations, including the standard power supply and video interface connections. For evaluation on the desktop, a PC-style 4-pin power supply connector is also provided. Figure 1 illustrates the simplified block diagram of the IDT79S389 Reference Platform.

The IDT79S389 Reference Platform is designed around the R3051 RISController family, including the IDT79R3081 and the R3041. All devices in the R3051 family are pin- and software-compatible. As a consequence, R3041, R3051E, R3052, R3052E, R3081 and R3081E can be substituted for the R3051 throughout this manual. For details on the R3051 family refer to the data sheets and hardware user manuals.

SYSTEM OVERVIEW

Figure 2 illustrates a high-level schematic of the data paths and various subsystems of the board. The user's manual that ships with the board provides extensive detail on the board, including complete schematics, PAL equations, and theory of operation.

Address and Data Path

The R3051 family uses a time multiplexed address and data bus. The IDT79S389 demultiplexes this bus into an address bus and two data buses. The use of two data buses both minimizes the loading of the buses, and allows either or both of the EPROM and DRAM subsystems to be interleaved.

The address path is constructed using IDT 74FCT162373 16-bit wide transparent latches, and is de-multiplexed off the A/D bus using the processor supplied ALE output signal.

The data paths are provided by a pair of IDT 73720 Bus Exchangers. The 73720 in general is a 3-port, 16-bit wide transceiver, used to multiplex a common CPU port between two data ports (typically found in two way interleaved sys-

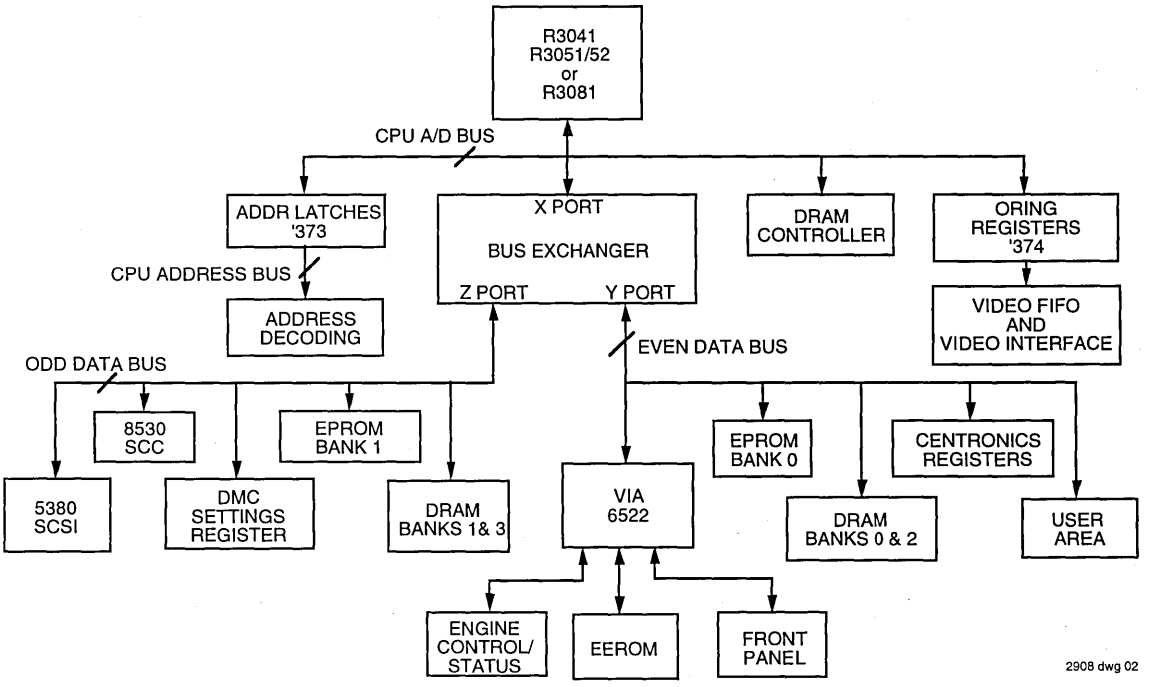


Figure 2. IDT79S389 High Level Schematics

	1MB SIMM non-interleaved	1MB SIMM interleaved	4MB SIMM non-interleaved	4MB SIMM interleaved
Bank 0	0x0080_0000 -> 0x008F_FFFF	0x0080_0000 -> 0x009F_FFFF (even)	0x0080_0000 -> 0x00BF_FFFF	0x0080_0000 -> 0x00FF_FFFF (even)
Bank 1	0x0090_0000 -> 0x009F_FFFF	0x0080_0000 -> 0x009F_FFFF (odd)	0x00C0_0000 -> 0x00FF_FFFF	0x0080_0000 -> 0x00FF_FFFF (odd)
Bank 2	0x00A0_0000 -> 0x00AF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (even)	0x0100_0000 -> 0x013F_FFFF	0x0100_0000 -> 0x017F_FFFF (even)
Bank 3	0x00B0_0000 -> 0x00BF_FFFF	0x00A0_0000 -> 0x00AF_FFFF (odd)	0x0140_0000 -> 0x017F_FFFF	0x0100_0000 -> 0x017F_FFFF (odd)

Table 1. DRAM Memory Map

tems). The control of the 73720 Bus Exchangers is performed by a dedicated PAL, which directs transfers between the CPU and the appropriate data bus, and insures that bus conflicts are avoided.

State Machines

The IDT79S389 uses a distributed state machine structure to implement control of the various peripheral subsystems. In this structure, each peripheral subsystem has dedicated control PALs associated with it. These PALs monitor the start of a transaction, and either ignore the transaction (if intended for other subsystems), or provide the appropriate control responses back to the processor at the appropriate times, according to the latency of the targeted subsystem. A master PAL generates a common "Cycle End" indicator to all state machines, indicating that they can await another transaction.

The advantage of this distributed state machine structure is that memory subsystems can be independently added, removed, or modified, without impacting the rest of the system. This simplifies end user customizing and system debug.

The disadvantage of this structure is that the number of PALs required is larger than if the state machines were centralized. It is expected that customers using this as a reference design would customize and/or cost reduce the state machines and I/O subsystems, using interface ASICs, ASSPs, or condensed PALs.

In addition to the distributed state machines, the IDT79S389 contains a number of PALs providing common functions to all state machines. These functions include address decoding, Cycle End generation, data path steering logic, bus timeout, and CPU input/response synchronization.

CPU Subsystem

The IDT79S389 board incorporates the standard R3051 family PLCC footprint. It is targeted to run at 25MHz, although its frequency may be scaled up or down, as appropriate. Note that when scaling frequency, the user should reprogram the wait states associated with the various memory and peripheral subsystems, and may need or choose to use faster or slower control and memory devices. The board and software do not require the use of a TLB.

DRAM Subsystem

The DRAM subsystem of the IDT79S389 board supports the use of 256K x 32 or 1M x 32 72-pin SIMM memories. Up to 4 SIMMs may be used, for a maximum of 16MB of DRAM memory. The memory can be interleaved or non-interleaved, according to a set of DIP switches.

The DRAM system is controlled by the IDT79R3721 DRAM controller. This device features an R3051 family bus interface, and implements direct control of the DRAM devices. The timing and configuration of the DRAMs is programmable in the R3721, according to the settings of an internal mode register.

To maximize user flexibility without requiring PROM changes, the IDT79S389 memory maps a set of DIP switches, called the MSEL switches. At system startup, the value of these switches is read by the CPU and then written to the IDT79R3721 DRAM controller, to configure the system timing model. Thus, in order to change the memory configuration or timing, the user merely needs to set the DIP switches and reset the board.

The DRAM memory is memory mapped to the address space 0x0080_0000 to 0x017F_FFFF, depending on the size of SIMM, number of SIMMs, and interleaving chosen. Table 1 illustrates the address map, depending on configuration. Table 2 illustrates the read and write latency (measured in clock cycles) of the various memory configurations, assuming 80ns SIMMs and a 25MHz system.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	1	2
Non-page Write	4	4
Page Write	3	3

Table 2. Number of Clock Cycles for Various DRAM Transfers

The IDT79S389 board is shipped with two 1MB 80ns SIMMs in a non-interleaved configuration. Additional SIMMs can be added by the user, and interleaving can easily be selected.

	1Mb EPROM	2Mb EPROM	4Mb EPROM
Bank 0 (non-Interleaved)	0x1FC0_0000 -> 0x1FC7_FFFF	0x1FC0_0000 -> 0x1FCF_FFFF	0x1FC0_0000 -> 0x1FDF_FFFF
Bank 1 (non-interleaved)	0x1FC8_0000 -> 0x1FCF_FFFF	0x1FD0_0000 -> 0x1FDF_FFFF	0x1FE0_0000 -> 0x1FFF_FFFF
Bank 0 (Interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (even)	0x1FC0_0000 -> 0x1FDF_FFFF (even)	0x1FC0_0000 -> 0x1FFF_FFFF (even)
Bank 1 (interleaved)	0x1FC0_0000 -> 0x1FCF_FFFF (odd)	0x1FC0_0000 -> 0x1FDF_FFFF (odd)	0x1FC0_0000 -> 0x1FFF_FFFF (odd)

Table 3. EPROM Address Map

EPROM Subsystem

The EPROM subsystem contains 8 sockets, capable of accepting 1Mb, 2Mb, or 4Mb devices. The sockets accept 8-bit wide EPROMs in the DIP package.

The board can be used with either 4 or 8 EPROM devices; if 8 devices are used, Interleaved or non-interleaved operation can be selected. The density of EPROM, and the interleaving factor, are selected via jumpers and PALs for the board. The board ships with 512KB of 120ns EPROM installed in a single bank; the EPROMs contain the IDT/sim monitor program ported to this board.

The EPROMs reside in the physical address range 0x1FC0_0000 through 0x1FFF_FFFF. This address space includes the system exception vectors, as well as the bootup code, and can be accessed either through or around the on-chip processor cache, according to the virtual address used. Table 3 shows the physical address map for the EPROMs. Table 4 shows the memory latency of the EPROM subsystem, for 120ns EPROMs and a 25MHz system.

SCSI Subsystem

The IDT79S389 board contains a single SCSI channel, implemented using the 53C80 SCSI controller. Although there is only one channel, there are two SCSI connectors on the board, to support the differences in the form factor of the various laser engines supported.

The SCSI device resides in the address range 0x0074_0000 through 0x0074_FFFF.

Serial Channels Subsystem

The IDT79S389 board implements two serial channels. One is a traditional RS-232 channel, and is accessed by a DB-25 connector. The other channel supports AppleTalk, and uses the standard AppleTalk connector. The board includes voltage translators and transceivers to implement the electrical protocols required by these standards.

	Interleaved	Non-Interleaved
First Word of Read	5	5
Adjacent words	4	1.6 (1-3-1)

Table 4. Number of Clock Cycles for Various EPROM Transfers

The serial channels are implemented using a single 85C30 SCC serial controller. The address space for the serial controller is 0x0073_0000 through 0x0073_FFFF.

EEROM Interface

The IDT79S389 board includes a 512B EEROM to store various configuration data. The EEROM is accessed by the 65C22 VIA device, which is memory mapped to 0x0071_0000 through 0x0071_FFFF.

Centronics Interface

The board also includes a unidirectional Centronics port. Centronics data is read from address space 0x0075_0000 through 0x0075_FFFF; Centronics status is written in the address space 0x0076_0000 through 0x0076_FFFF.

Front Panel Interface

The front panel interface corresponds to a Canon LBP-8 Mark IIIR, and uses a series of switches, LEDs, and LCDs to implement front panel control. Front panel is accessed by the 65C22 VIA device, which is memory mapped to 0x0071_0000 through 0x0071_FFFF.

Video Interface

The video interface corresponds to the interface requires for the Canon LBP-8 Mark IIIR, based on the Canon LBP-RX print engine. The video interface is implemented using discrete logic, with status taken from the 65C22.

Video data is sent to the video interface by performing an aliased read of the DRAM memory. If a processor read of the 16MB region starting at 0x0880_0000 is detected, the access will be processed as a DRAM read. However, the read data returned from the DRAM will be captured by the video interface, and later shifted out to the print engine. This technique eliminates overhead by not requiring the processor to explicitly write the data to the video channel.

User Expansion Area

In addition to the memory systems described above, the IDT79S389 board contains a user expansion connector. The user expansion connector allows users to add custom features to the board for software development. Features which could be added might include an Ethernet channel, additional font ROM, or a different engine and front panel interface.

The IDT79S389 board provides a User Chip Select, mapped to address 0x0078_0000 through 0x0078_FFFF, for use with the expansion connector.

Board Form Factor

The form factor and hole placement of the board allows it to be directly mounted into either a Canon LBP-8 Mark IIIR laser printer, the HP LaserJet III, or the Canon OEM print engines LBP-SX or LBP-RX engines. The placement of the video, front panel, and power connectors, are compatible with these form factors.

In addition, the board can be run on a benchtop using a standard PC compatible power supply. If the board is used in this fashion to drive an engine, it is recommended that a common ground between the board and the engine be provided.

Summary: Address Map and Interrupt Assignment

Table 5 is a summary of the address map of the IDT79S389 board. Table 6 shows the interrupt assignments of the CPU.

Memory Subsystem	Start Address	End Address
VIA	0x0071_0000	0x0071_FFFF
SCC	0x0073_0000	0x0073_FFFF
SCSI	0x0074_0000	0x0074_FFFF
Centronics Data	0x0075_0000	0x0075_FFFF
Centronics Status	0x0076_0000	0x0076_FFFF
User Chip Select	0x0078_0000	0x0078_FFFF
MSEL Switches	0x0079_0000	0x0079_FFFF
R3721 Mode Register	0x007A_0000	0x007A_FFFF
DRAM	0x0080_0000	0x017F_FFFF
Aliased Video DRAM	0x0880_0000	0x097F_FFFF
EPROM	0x1FC0_0000	0x1FFF_FFFF

Table 5. IDT79S389 Memory Map Summary

Device	CPU Interrupt
Reserved	Int(0)
R3081 Floating Point	Int(1)
VIA	Int(2)
HFull/Video Reset	Int(3)
SCSI	Int(4)
SCC	Int(5)

Table 6. IDT79S389 Interrupt Assignment

SPECIFICATION SUMMARY

Order Number: IDT79S389

Maximum on board memory capacity:

DRAM — Four 72-pin SIMM sockets for 256K x 32 or 1M x 32 (1 to 16MB)

EPROM — Eight 32-pin sockets for 128K x 8 to 512K x 8 (to 4MB)

Serial EEROM — One 8-pin socket for serial EEROM (512bytes)

Debug Monitor EPROM: IDT/sim Version 4.0 ported to IDT79S389

Serial Ports: Controlled by 85C30 DUART.

Serial — CRT terminal connector or for downloading J3 (25-pin AMP 748133-1,DB25S, right angle female).

Appletalk — AppleTalk connector J2 (8-pin AMP 749179-1, D8 8, right angle female).

Parallel port:

Centronics — 36-pin, female, right angle, standard Centronics parallel connector (R.Nugent RPM-C36SB-SR-TG).

SCSI port: Controlled by 53C80 SCSI controller. SCSI connector J5 or J10 (50-pin, female, right angle, (R.Nugent RPM-C50SB-SR-TG).

Video: Standard 20-pin, male Canon LBP-RX video interface connector (HIROSE PCN-10-20P 2.54DSA).

Front Panel: J7, 34-pin male, right angle connector (AMP 1-103149-7).

Expansion: Four 40-pin male, four wall headers, J11-14 (MOLEX 39-26-7404).

Physical: Compatible with Canon RX, SX engine form factors.

Operating Temp: 0–50°C.

Power Supply: 5.0V ± 5%, 3 Amps typical (estimate).

PHYSICAL LAYOUT

The physical layout of the IDT79S389 Reference Platform reflects the board's primary objectives:

1. Software delivery vehicle for PostScript Level 2 software from Adobe
   - — Memory space appropriate for PostScript Level 2 software typical implementations,
   - — Various memory configurations (interleaved vs non-interleaved, code running out of DRAM or out of ROM) to easily evaluate cost and performance alternatives.

2. Cost-Effective design model for IDT79R3051 RISController family
   - — NO zero-wait-state memory,
   - — Minimum complexity board configuration (6 layers),
   - — Fits industry standard Canon LBP-RX print engine.

3. Advanced hardware starting point for rapid evaluation, cost-performance point analysis and development of OEM finished products.

4. Advanced software-ready controller, suitable for immediate development with PostScript Level 2 software from Adobe, and adaptation to other print engines and communications ports (Adobe software available only under license from Adobe Systems Incorporated).

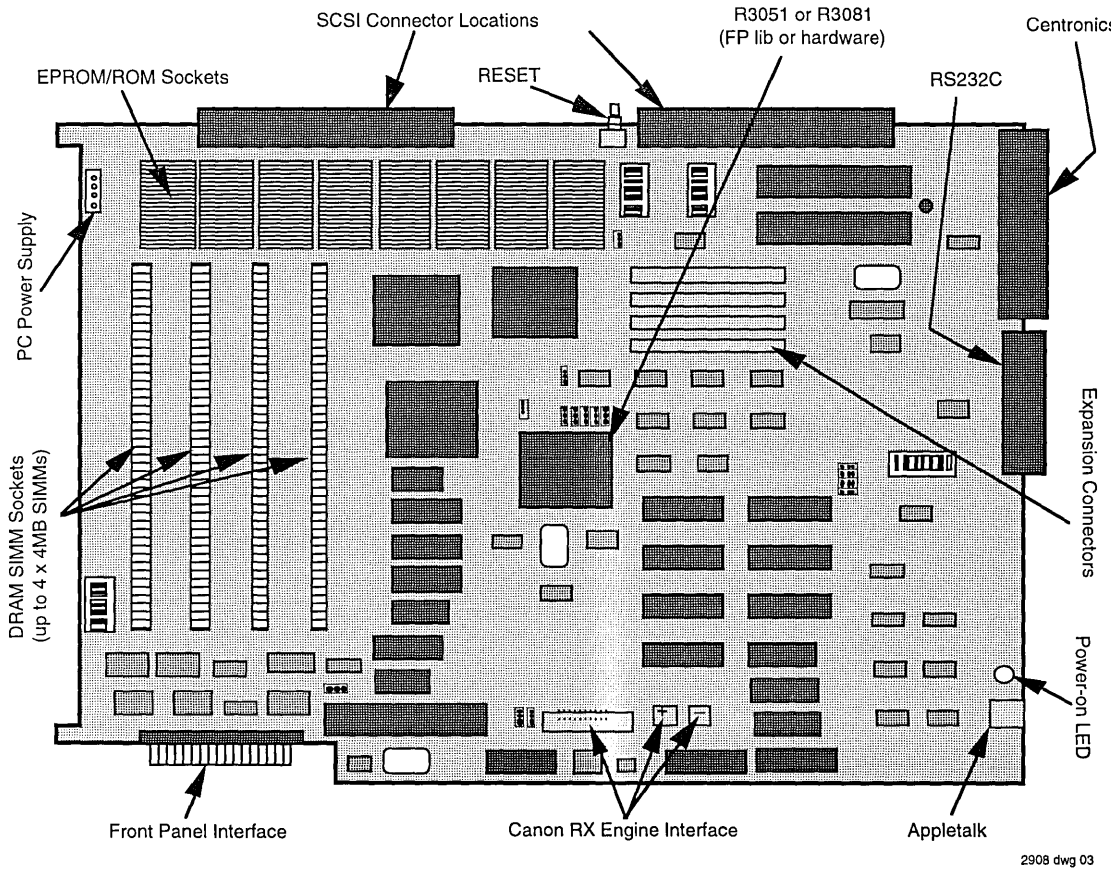


Figure 3. IDT79S389 Board Layout

ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's guide includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R3081 CPU plugged in, but samples of the R3052 and R3041 are provided. The R3051 can also be ordered to allow user upgrades.

Evaluation Boards

R3041 Evaluation Kit	20 MHz System Board	79S341
R3051 Evaluation Kit	25 MHz System Board	79S385A
R3081 Evaluation Kit	33 MHz System Board with Ethernet	79S381
R4600 Evaluation Kit	50 MHz to 75 MHz System Board with Ethernet	79S460

Integrated Device Technology, Inc.

R3051™ FAMILY EVALUATION KIT

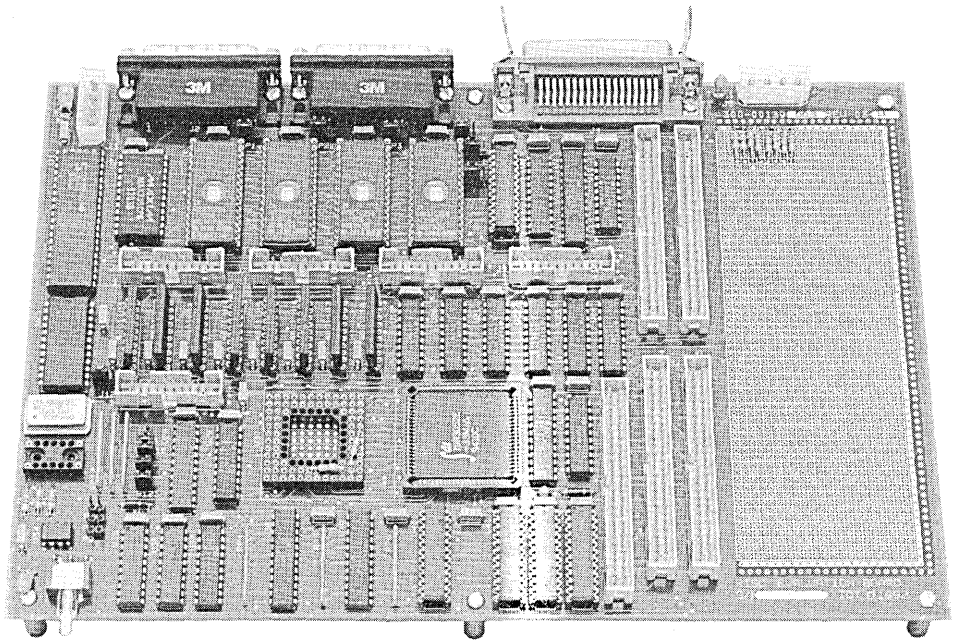
IDT79S385A

FEATURES:

- Complete 25MHz RISC System Board
  - — Requires only 5V supply and terminal to operate
  - — Supports R3041™, R3051, R3052™, R3071™ or R3081™ highly integrated RISC CPUs
  - — Board contains an IDT79R3052E
  - — 1MB of non-interleaved DRAM, expandable to 4MB
  - — 128KB of EPROM, expandable to 2MB
  - — Serial and Parallel Ports
  - — Connectors provided for easy connection to HP Logic Analyzer
  - — Wire-wrap area on the board
- IDT/c™ for IBM PC compatibles included in kit
  - — Hardware or software floating point
  - — Remote symbolic debug
- IDT's System Integration Manager (IDT/sim™) included in EPROM
  - — High capability debug monitor
  - — Simplifies software development
- Complete set of documentation included
  - — Supplied with complete set of board schematics
  - — PAL equations supplied on IBM PC 3.5" disks
  - — User's manuals for R3051 family, IDT/sim, and IDT/c
- Utility programs also included
  - — Program utility disk
  - — HP16500A Logic Analyzer disassembly software
- R3081 sample also included for board upgrade

DESCRIPTION:

The IDT79S385A Evaluation Kit is a complete kit for evaluating the R3051 hardware and software environment. The kit contains a working system, including all schematics and theory of operation, an R3081 sample to allow the user to upgrade the system capabilities, and a complete software development environment, including debug monitor and "C" compiler/assembler toolchain. Finally, the kit is complemented by documentation, logic analyzer software, and utility programs.



IDT79S385 RISC System Board. Actual Size 8.5" x 11"

SEPTEMBER 1995

COMPLETE SINGLE BOARD COMPUTER

The 79S385 board is a complete working RISC system intended as a complete design example using the R3051 family of highly integrated RISC CPUs. The board requires only a simple CRT terminal and a 5V power supply for operation. Figure 2 shows a block diagram of the79S385 board.

The board is designed around IDT's R3051 family of highly integrated RISC CPUs. An R3052E CPU chip (8KB I-cache and 2KB D-cache, with on-chip TLB) is included in a socket, but any member of the family can be substituted. The 79S385A kit includes a sample of a 25MHz R3081 in a PGA pinout, to allow the user to upgrade the system. A large wire-wrap area is available on the board for adding additional hardware. All the schematics and details of the designs are supplied with the board, including all PAL equations on an IBM format 3.5" disk.

The 79S385 board is supplied with 1MB of DRAM in socketed 256K x 4 ZIPs; the ZIPs can be replaced with 4MB devices to obtain 4MB of DRAM on the board (an applications brief on upgrading memory is included in the kit). Other hardware on board includes a 2681 DUART and an 8254 counter/timer; both these devices are supported with drivers in IDT/sim. A parallel Centronics port is available for higher speed download of code into the board.

The board contains 128KB of EPROM expandable to 2MB by replacing the EPROMs with higher density devices. The EPROMs contain IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing, and I/O.

There are two serial ports, a free-running programmable timer, and a parallel Centronics port for high-speed download of software. A set of expansion connectors permits external hardware to be connected to the board, and a wire-wrap area on the board can be used to build additional hardware without using a second board.

The board is designed to be placed on a flat table-top surface. Standoffs are provided for physical support.

The 3051 Bus, along with other control signals, is connected to a set of pins in the center of the board next to the wire wrap area. These signals can be used to connect additional hardware on either the wire-wrap area or on another board via a ribbon cable. DMA control is provided. Table 1 shows the signal description for the expansion connector.

IDT/SIM DEBUG MONITOR SOFTWARE

IDT's System Integration Manager (IDT/sim) is included in EPROMs on the board. This software permits downloading of code from a host system, execution control with breakpoints, in-line assembly and disassembly, and a variety of commands to control main memory, cache memory, and the internal TLB. It provides all the resources needed to bring up new hardware and software.

The evaluation kit also includes a complete set of user documentation for the IDT/sim software tool. The capabilities of IDT/sim are described in a separate data sheet.

IDT/C "C" COMPILER FOR IBM PC COMPATIBLES

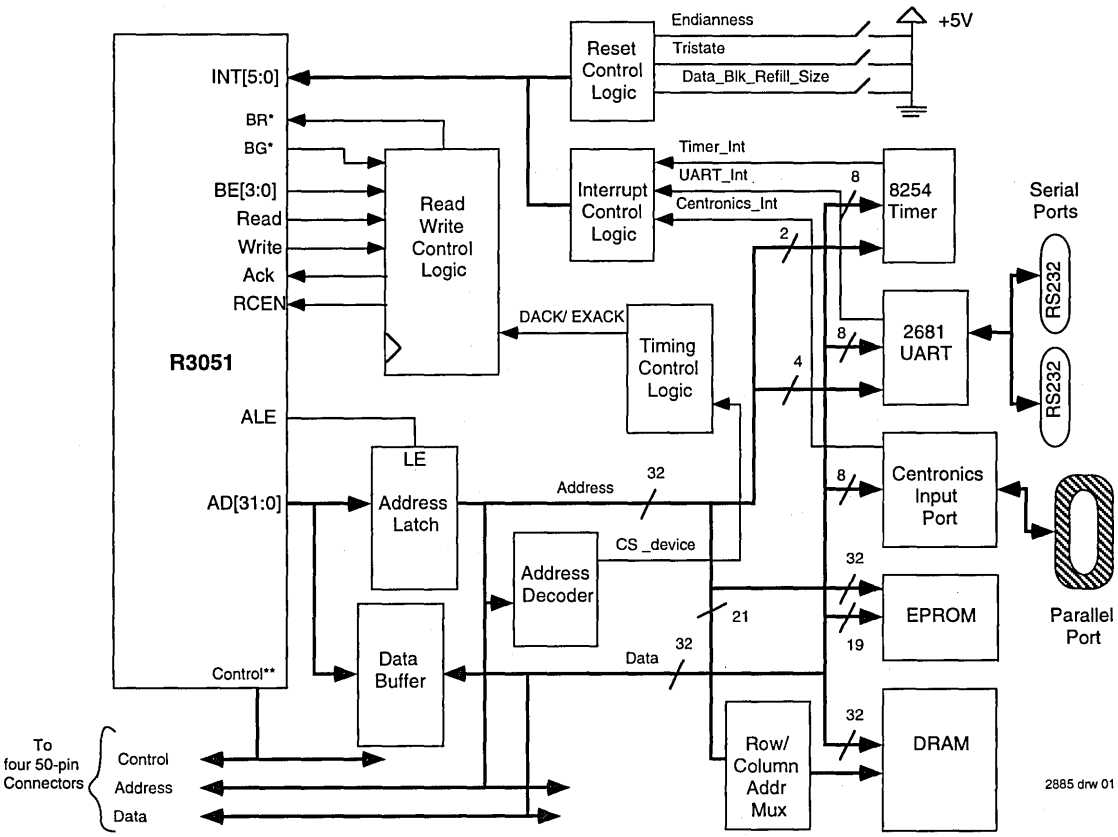
In addition, the evaluation kit contains a complete copy of the IDT/c software development toolchain, hosted on IBM PC compatible computers. IDT/c, described in a separate data sheet, includes:

- The ability to generate big- or little-endian code

Signal Name	I or O	Description
EA00-EA31	I/O	32-bit buffered address bus
ED00-ED31	I/O	32-bit buffered data bus
SYSOUT	O	Buffered SYSCLK Clock from CPU; used to synchronize data transfers
MRES#	O	Copy of the Reset signal to the CPU
MREQ	O	Memory Request output (handshaking signal for data transfers)
EXACK#	I	Acknowledge input (handshaking for data transfers)
IP4-IP5	I	Auxillary input pin to the 2681 UART
WEA-WED	O	Write Enables for the four bytes of the data word
UCS	O	Chip select signal decoded from the high order address bits for external hardware
INT0:INT5	I	Interrupt inputs to the R3052
RD#	O	Memory Read output signal from the 3052
WR#	O	Memory Write output signal from the 3052
BREQ#	I	Bus Request input to the 3052
BUSGNT#	O	Bus Grant output from the 3052

2885 tbl 01

Table 1. Signals Supplied on Expansion Connector



** These control signals include R3051 and the on-board control logic signals as well.

Figure 2. IDT79S385 Board Block Diagram

- Hardware or software floating point support
- "C" library support, including source libraries
- Remote symbolic debug

LOGIC ANALYZER INTERFACE

The 79S385A evaluation kit also includes the ability to simply use an HP16500A logic analyzer for execution trace and software debug. The board includes a set of connectors to easily allow connection of the logic analyzer to the board. Also included is a disk for the HP16500 containing disassembly software, allowing the analyzer to display a disassembled listing of the software executing on the system.

KIT SUMMARY

The IDT 79S385A evaluation kit is a complete low-cost package for evaluation of the R3051 family, especially its software environment. The kit allows the user to develop and execute high-level language programs, to look at a software development toolchain for the IDT R3051 family, and to evaluate a hardware design around the R3051 family.

KIT CONTENTS

IDT79S385 RISC Evaluation Board
IDT/c Multi-Host compiler toolchain
IDT/sim debug monitor included in board EPROMs.
User's Manuals for:

- IDT79S385 board
- R3051
- R3081
- IDT/sim
- IDT/c

Applications Guide for R3051 family
Program Utility Disk
Disassembler for HP16500 Logic Analyzer
PAL Equations on IBM PC compatible 3.5" disk format

BOARD SPECIFICATIONS

CPU
25MHz R3052E on board
25MHz R3081 sample included

Cache Ram
8KB I-cache, 2KB D-cache (in 3052 chip)
16KB I-Cache, 4KB D-Cache configurable to
8KB I-Cache, 8KB-DCache (in R3081 chip)

Cacheable Address Space
4GB

DMA Support
Bi-directional tri-stateable buffers can be used to write to DRAM from external logic

Block Refill
4 word instruction block size
1 or 4 word data block size programmable via jumper

Endianness (Byte Ordering)
User programmable via jumper

Read/Write Buffers
Both are 4 words deep (inside R3052 chip)

Interrupts
6 User Interrupts, three synchronized with SYSCLK

I/O characteristics
TTL levels from FCT logic devices, PALs and R3052

Power Supply
2 amps (typical) at 5V, 25°C, at rated speed

Environmental Conditions
Ambient temperature 0°C to +50°C
Relative Humidity 5% to 95%

Clock Frequency
25MHz

Interconnection
Five 50-pin connectors, containing Address, Data, and Control signals and R3052 signals
Five 20-pin plugs for use with HP logic analyzer
Two RS-232 serial ports on DB-25 connectors
One parallel Centronics port for input

User Selectable Options
Endianness, data block refill size
Tri-State mode of 3052

ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R3052E CPU plugged in, but any member of the 3051 family can be used. An additional sample of the R3081 is included to allow user upgrades.

Evaluation Boards

R3051 Family Evaluation Kit 79S385A

EPROM Upgrades

The following part numbers update the evaluation board hardware to the latest version of the IDT/sim monitor.

Evaluation boards 7RS901BGP
Use with 79S385 only

Integrated Device Technology, Inc.

R3041™ EVALUATION KIT

IDT79S341

FEATURES:

- Complete low-cost 20MHz RISC system
  - Plug-in AT-style card or stand alone mode
  - Supports the R3041™ highly-integrated, low-cost RISController™ CPU
  - DRAM/memory controller logic implemented with a single low-cost PLA chip
  - Capability to test different hardware wait-state and clocking options
  - 128KBytes of boot EPROM expandable to 512KB
  - 1MByte DRAM expandable to 4MB
  - 8/16/32-bit wide DRAM array
  - Two Serial Ports
  - 16-bit external Counter/Timer
  - PC ISA interface logic
  - Connector provided for easy connection to a logic analyzer
- IDT/c™ for PC included in kit:
  - Software floating point emulation
  - Remote symbolic debug
- IDT's System Integration Manager (IDT/sim™) included in EPROM
  - On-board debug monitor
  - Simplifies software development
- IDT's PCIO16 Terminal Emulation Program (IDT/pcio16™) included in kit
  - Allows communication and downloading between the board and PC
- Complete set of documentation included
  - User's Manual for R3041 Evaluation board
  - Installation and operation guide for standalone and PC configurations
  - Design and theory of operation documentation
  - Includes complete set of board schematics and PLA equations
  - User's Manual for R3041, IDT/c, and IDT/sim
  - Application Guide for the R3051 Family

FUNCTIONAL BLOCK DIAGRAM

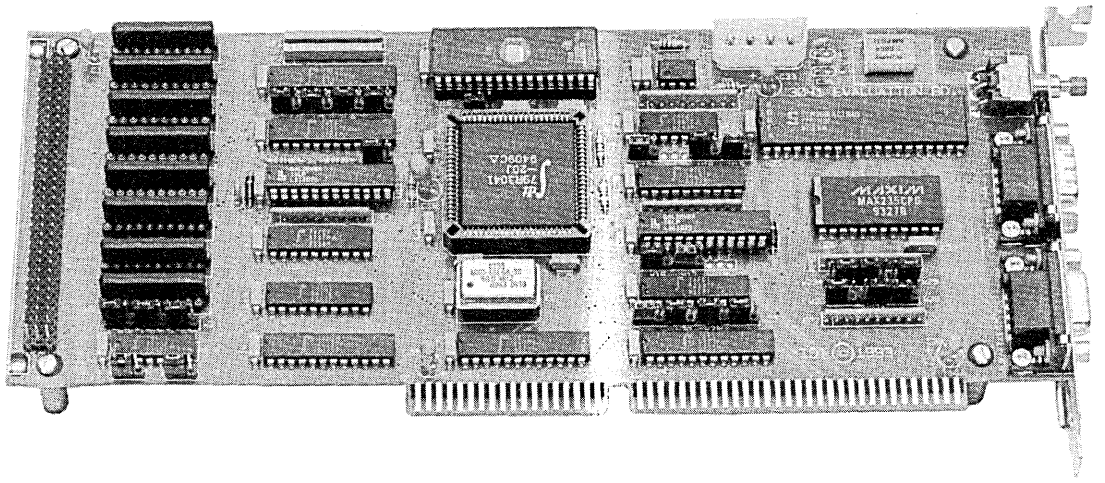


Figure 1. R3041 System Evaluation Board. Actual Size 4.2" x 10.0"

DESCRIPTION

The IDT79S341 Evaluation Kit is a complete kit for evaluating the R3041 hardware and software environment. The kit contains a working system, including a User's Manual with installation guide, schematics, PLA equations, theory of operation, and design notes. A complete software development environment, including debug monitor and "C" compiler/assembler toolchain for the PC is included. The kit also includes the R3041 User's Manual and the R3051 Family Applications Guide.

COMPLETE SINGLE BOARD COMPUTER

The 79S341 Evaluation Board is an example of a complete working MIPS R3000-based RISC System. The board is a low-cost and parts-count design example using the highly integrated R3041 RISController CPU. Primary uses of the board include:

1. Evaluating the R3041 architecture.
2. Prototyping and running software.

The board is highly configurable and contains hardware options for state machine experiments as well as for setting different DRAM sizes, speeds and 32/16/8-bit memory widths.

The 79S341 Evaluation Board is designed around the IDT79R3041 RISController. The R3041 is a highly integrated low-cost version of the R3051 family of RISControllers and includes 2KB of on chip instruction and 512B of on chip data cache. The R3041 also contains memory controller support circuitry including programmable bus width, a refresh timer, read and write strobes, and address multiplexer controls. Thus on the S341 board, the DRAM controller, memory controller, and I/O controller are implemented externally within a single low-cost 24-pin PLA.

Although the R3041 can run in an R3051 family bus-compatible mode, on the 79S341 Evaluation Board, specific superset bus features of the R3041 are taken advantage of; for instance the 8-bit boot PROM capability, to reduce chip count and cost. Other boards, such as the IDT79S385A R3051 evaluation board kit, as described in a separate data sheet, can be used to demonstrate the R3041 using its R3051 bus-compatible mode.

The 79S341 Evaluation Board can be operated in one of two ways. In the default configuration as a standalone board, the 79S341 board requires only a standard RS232-C CRT video terminal and a 5V power supply for operation. The board can be placed on a flat table-top surface by using the removable standoffs which are provided for physical support. The standoffs can be removed for the alternate configuration as a PC/AT ISA backplane add-in board. In this second configuration, the 79S341 Board only requires a PC/AT compatible personal computer. Using the IDT/pcio16 PC/AT software program included in the kit provides a terminal emulator and downloader directly over the PC/AT backplane.

The 79S341 board contains a single 128K x 8 EPROM and can be upgraded to a user supplied 256K x 8 or 512K x 8 EPROM. Main memory consists of eight 256K x 4 (1Mb) DRAM ZIPs. There are two serial ports, one external timer in addition to the internal timer on the R3041, and a PC/AT backplane 16-bit I/O interface for downloading software. A logic analyzer connector permits external observation and evaluation of key CPU signals.

The boot EPROM contains IDT's System Integration Manager (IDT/sim), a debug monitor kernel that supports download of code from host systems, remote debug interface, execution control commands including single stepping and instruction tracing, memory probing, register probing, line-based assembly, and disassembly of code.

The board supports the use of 32/16/8-bit wide DRAM array configurations through the use of hardware jumper options. The board can be populated with either the default 1Mb DRAM ZIPs or with user supplied 4Mb DRAM ZIPs. Thus the board supports anywhere from 256KB to 4MB of main memory.

An IDT MacStation, SPARCstation, (or PC/AT) can be connected to the 79S341 via one of the serial ports and user developed code (generated using a cross-compiler such as GNU-C, MIPS-C, or the IDT/c compiler) can be downloaded to the board. In the add-in board mode, the 79S341 can be installed on the backplane of a PC/AT personal computer. Development can done completely from the PC/AT or downloads can be transferred from a workstation to the PC (via user supplied ethernet) and then through the PC/AT backplane of the 79S341. When used on the PC/AT backplane, additional server software which runs under MS-DOS is included, which allows CRT video emulation and program downloading via the PC/AT ISA backplane.

In addition, a logic analyzer connector is provided allowing additional hardware observability.

The 79S341 is constructed using through-hole devices on a 4-layer 4.2" x 10.0" PC/AT form factor compatible epoxy laminate board with standoffs and is intended either as a standalone bench top device or as a backplane add-in card.

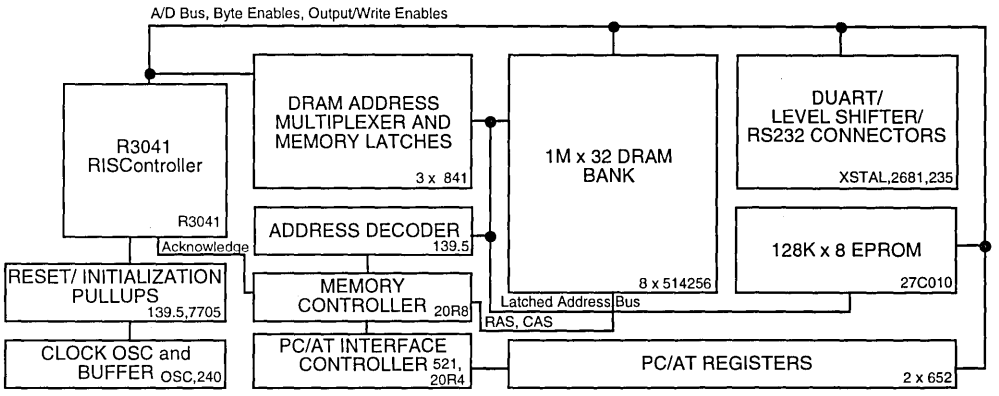


Figure 2. 79S341 Board Block Diagram

IDT/C MULTI-HOSTED C-COMPILER

The evaluation kit contains a complete copy of the IDT/c software development toolchain, hosted on IBM PC-386/486 compatible computers and SUN SparcStation. IDT/c, described in a separate data sheet, includes:

- ANSI-C optimizing compiler, assembler, linker, and librarian
- ANSI-C library support (source libraries available separately)
- Supports multiple memory segments for embedded system code
- Software floating point support
- Remote symbolic debug

IDT/SIM DEBUG MONITOR SOFTWARE

IDT's System Integration Manager (IDT/sim) is included in an EPROM on the board. This software permits downloading of code from a host system, execution control with breakpoints, in-line assembly and disassembly, and a variety of commands to control registers, cache memory, and main memory. IDT/sim provides all the resources needed to bring up new hardware and software.

The evaluation kit also includes a complete set of user documentation for the IDT/sim software tool. The capabilities of IDT/sim are described in a separate data sheet.

IDT/PCIO16 TERMINAL EMULATION AND DOWNLOAD UTILITY SOFTWARE

IDT's PC 16-bit I/0 Terminal Emulation and Download Utility Software (IDT/pcio16) is included on an IBM PC compatible disk for use with an IBM PC AT-Bus compatible (ISA) machine. IDT/pcio16 allows the evaluation board to be operated from the PC/AT ISA backplane. The PC/AT acts as a video screen and keyboard terminal for the board by communicating through the backplane. IDT/pcio16 also includes download utilities to move s-record files from the PC/AT to the evaluation board.

KIT SUMMARY

The IDT79S341 evaluation kit is a complete, low-cost package for evaluation of the R3041 RISController and its software environment. The kit allows users to develop and execute high-level language "C" programs, to look at a software development toolchain for the IDT R3051 family, and to evaluate a low-cost hardware design using the R3041 RISController.

KIT CONTENTS

- 79S341 RISC Evaluation Board
- IDT/c Multi-Host compiler toolchain (IBM PC-compatible version)
- IDT/sim debug monitor included in board EPROM User's Manuals for:
  - 79S341 board
  - R3041
  - IDT/c
  - IDT/sim
  - Applications Guide for R3051 family
- IDT/pcio16 software on IBM PC compatible 3.5" disk format
- 6' cable for serial port from board for connection with 9-pin male or 25-pin male connector

BOARD SPECIFICATIONS

7

CPU	20MHZ R3041
On-chip	2KB I-cache, 512B D-cache

On-Board Memory Capacity:

As shipped (Minimum):	DRAM — 256K x 32 (1MB) EPROM — 128K x 8 (128KB)
Maximum:	DRAM — 1M x 32 (4MB) EPROM — 512K x 8 (512KB)
Debug Monitor EPROM:	128K x 8 (128KB) containing IDT/sim.
Serial Ports:	Controlled by SCN2681 DUART. CRT Terminal connects to J3.

Software configurable features.

Default state:	9600 Baud, 8 bits, no parity, 1 stop bit.

AUX Download port connects to J4.

Software configurable features:

Default state:	9600 Baud, 8 bits, no parity, 1 stop bit.
Serial Port Connectors:	Two DTE DB9s (right angle female) connectors.
Timers:	1. Programmable counter/timer 16-bit timer on 2681 DUART. 2. On-chip R3041 24-bit timer used for DRAM refresh timer.
Interrupts:	3 synchronized, 3 unsynchronized (4 used on-board with 2 spares).
Expansion Connector:	One 96-pin Right angle (male) DIN compatible. Connects with 96-pin reverse DIN (female). Contains R3052 A/D bus, control signals, and Bufferred SysClk.

User Selectable Options:

Standalone vs. PC/AT ISA configuration, PC/AT ISA I/O address, interrupt number, DRAM size, 32/16/8 DRAM width, Boot PROM size, Endianess, cache vs. debug mode, Data Block Refill size

Physical Dimensions:

PC/AT ISA Form Factor compatible: 4.2" x 10.0".

Operating Temperature:	0°C to 50°C
Relative Humidity:	5% - 95%
Power Supply:	5.0V ± 5%, 0.75Amps typical
Power Supply Connection (if used):	One 4-pin power supply connector (4p-pin PC disk drive)
PC/AT Compatibility (if used):	PC/AT 8.33MHz ISA Bus backplane slot
PC/AT System Requirements (if used):	DOS 3.0 or higher, 640K memory, 3.5" floppy disk drive

ORDERING INFORMATION

Each kit is shipped with an evaluation board, complete schematics and PLA equations, as well as a complete software development toolchain for "C" language programming. User's Manuals include instructions on compiling "C" programs, downloading code, and operating the Software Integration Manager.

Evaluation Board

R3041 Evaluation Kit 79S341

Integrated Device Technology, Inc.

R3081™ EVALUATION KIT

IDT79S381

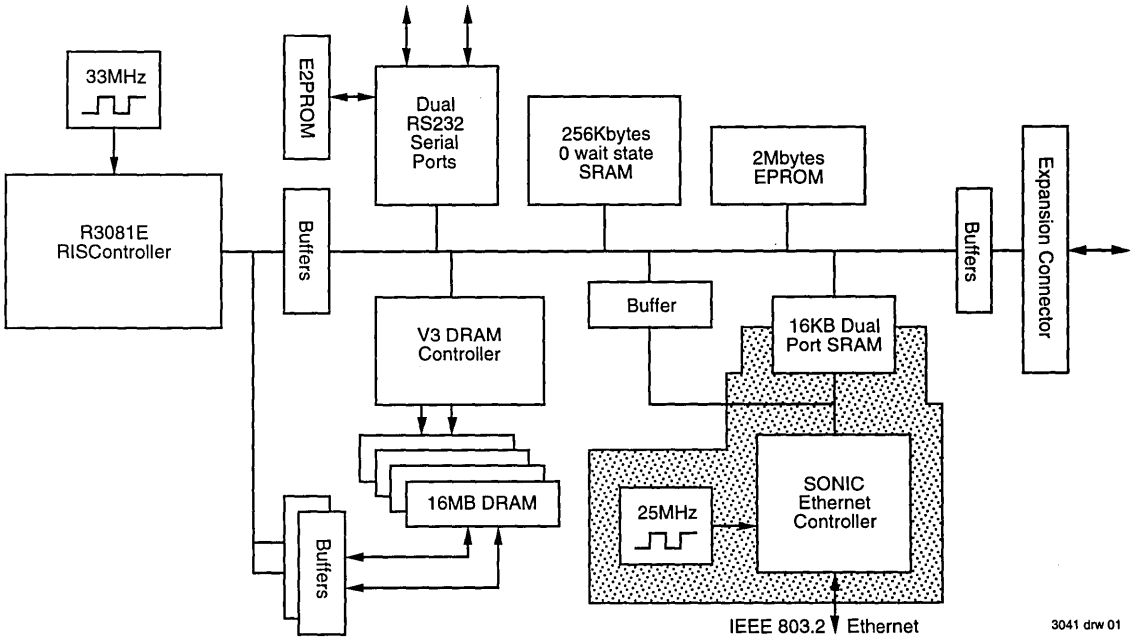
FEATURES:

- Complete 33MHz RISC System Board
- Supports R3081™, R3052™, R3051™, R3041™ CPUs
- Includes:
  - R3081 CPU, with R3041, R3051 and R3071 samples
  - 2MB interleaved DRAM, expandable to 4MB, 8MB, or 16MB
  - 256KB zero-wait-state SRAM
  - 512KB of EPROM expandable to 1MB or 2MB
  - 1024-bit serial EEPROM
  - 2 serial ports
  - **IEEE 802.3** Ethernet subsystem with 8KB dual-port SRAM expandable to 16KB
  - Expansion connector

DESCRIPTION:

IDT's R3081 Evaluation Kit is a complete evaluation and development kit for IDT's R3051 family of RISControllers™. Designed to demonstrate the optimal performance of these RISControllers, zero-wait state memories allow one to see the true performance of IDT's R3041, R3051/2, and R3081 devices. For those developing large segments of code, the IEEE ethernet interface allows for quick downloading of large code blocks. The system supports up to 16MBytes of DRAM. On top of the system board with an on-board monitor, IDT's System Integration Manager (IDT/sim™), the complete package includes IDT's IDT/c compiler (IDT/c™), samples of our R3041, R3051 and R3071 devices, and a complete documentation package including a user's guide, board schematics, and PAL equations.

FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

Each kit is shipped with an evaluation board, complete schematics and PLA equations, as well as a complete software development toolchain for "C" language programming, downloading code, and operating the Software Integration Manager.

Evaluation Board
R3081 Evaluation Kit.....79S381

Integrated Device Technology, Inc.

Orion™ R4600™ EVALUATION and DEVELOPMENT PLATFORM

Preliminary
79S460

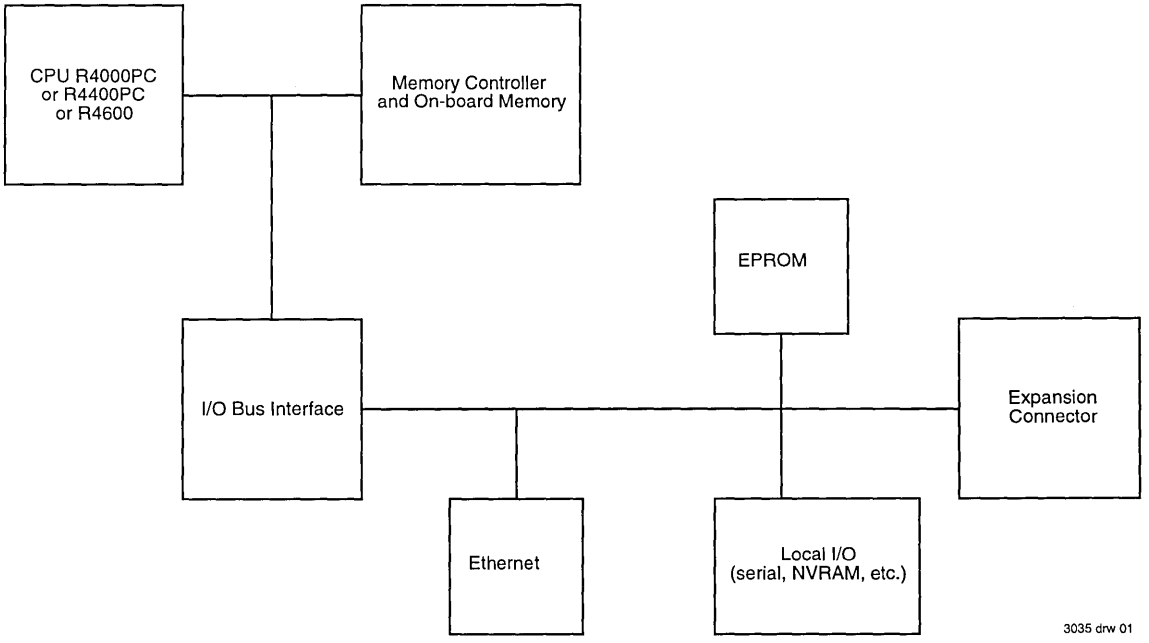
FEATURES:

- Complete RISC System Development Board
  - — Supports R4600 at speeds of 100, 133 or 150 MHz
- Uses a12 pin PC-style power connector with +12V, –12V and +5V
- System interface and memory system runs at 50MHz
- 2MB minimum of non-interleaved DRAM, expandable to 96MB in 4 SIMMs
  - — 2 SIMMs for base memory and 2 SIMMs for expansion memory
  - — Tuned for 60ns DRAMs but can use 70 or 80ns DRAMs
- 256KB of EPROM, expandable to 1MB
- Ethernet connection (thick net) via the DP83932 SONIC Controller
- Dual serial ports through NEC 72001 DUART
- Daughter board expansion area
- Provides for logic analyzer connection
- Shipped with IDT/sim™ (System Integration Manager) in EPROM
  - — High capability debug monitor
  - — Simplifies software development
- Complete set of documentation included
  - — Complete set of board schematics
  - — Complete PAL sources
  - — Board specifications manual
  - — Design manual with the theory of operations
  - — User's manual for IDT/sim

DESCRIPTION:

The 79S460 Evaluation Board is a complete design for evaluating the R4600 hardware and software environment. The package contains a working system, including schematics and theory of operations, complete documentation, and a debug monitor for software development.

FUNCTIONAL BLOCK DIAGRAM



3035 drw 01

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SEPTEMBER 1995

COMPLETE SINGLE BOARD COMPUTER

The79S460 is a complete working RISC system intended as a design example using the R4600 highly integrated CPU. The board requires only a simple CRT terminal and a PC-style power supply for operations. While intended to use the R4600, the board also supports the pin compatible R4400™PC.

The R4600 Evaluation Board is supplied with 2MB of DRAM in the base memory SIMM sockets. This can be upgraded to 32MB for base memory (4Mx36 SIMMs). The expansion memory SIMMs can provide an additional 64MB of DRAM. Other hardware on the board includes a NEC 72001 DUART and a DP83932 SONIC Ethernet Controller; both devices are supported with drivers in IDT/sim. The Ethernet connection is provided for higher speed download of code to the board.

The board contains 256KB of EPROM expandable to 1MB by replacing the given EPROM with a higher density device and adding the second EPROM. The enclosed EPROM contains IDT's powerful System Integration Manager (IDT/sim), a debugging monitor that supports download of code from host systems, execution control commands, memory probing and I/O. The capabilities of IDT/sim are described in a separate data sheet.

The R4600 Evaluation Board also contains a daughter-board expansion bus. This is controlled by logic similar to a simplified i486 local bus but is expanded to 64-bits and operates at 33MHz. Daughter-boards provide slave memory or registers accessible to the R4600 CPU and can also be DMA masters capable of reading and writing to memory.

ORDERING INFORMATION

Each unit is shipped with complete schematics and PAL equations. A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the correct timing interfaces to additional hardware. Boards are shipped with the R4600 CPU plugged-in, but the R4400PC can also be used. The R4400PC can also be ordered to allow user upgrades.

EVALUATION BOARD

R4600 Evaluation Kit.....79S460

Integrated Device Technology, Inc.

ORION ™79S464 EVALUATION KIT

IDT79S464

FEATURES:

The major features of the 79S464 RISController Evaluation Board include:

- Complete 50MHz RISC system
- Default standalone board configuration for use with external terminal
- Supports the R4600/R4700/R4650 highly integrated RISController CPUs
- 4, 16, or 64MByte DRAM, interleaved, 60nsec for 50MHz bus
- 4MBytes of EPROM, non-interleaved, non-cacheable
- IDT's System Integration Manager (IDT/sim) included in EPROM
- Two serial RS232 channels (in Cirrus CL-CD1284)
- Intel 82C54 timer for OS interrupt (UNIX, CExec, NT, etc.)
- Clock, reset, and interrupt generation logic
- P1284 bidirectional interface using the Cirrus CL-CD1284; supports all 5 modes

DESCRIPTION:

The 79S464 Evaluation Board is an example of a complete working MIPS R4600 RISC System. The board is a low cost and parts count design example using the highly integrated R4600 RISController CPU. Primary uses of the board include:

1. Evaluating the R4600/R4700/R4650 architecture.
2. Prototyping and running software.

The board is highly configurable and contains hardware options for setting different DRAM sizes and bus speed. Figure 1 shows a block diagram of the 79S464 RISC evaluation board.

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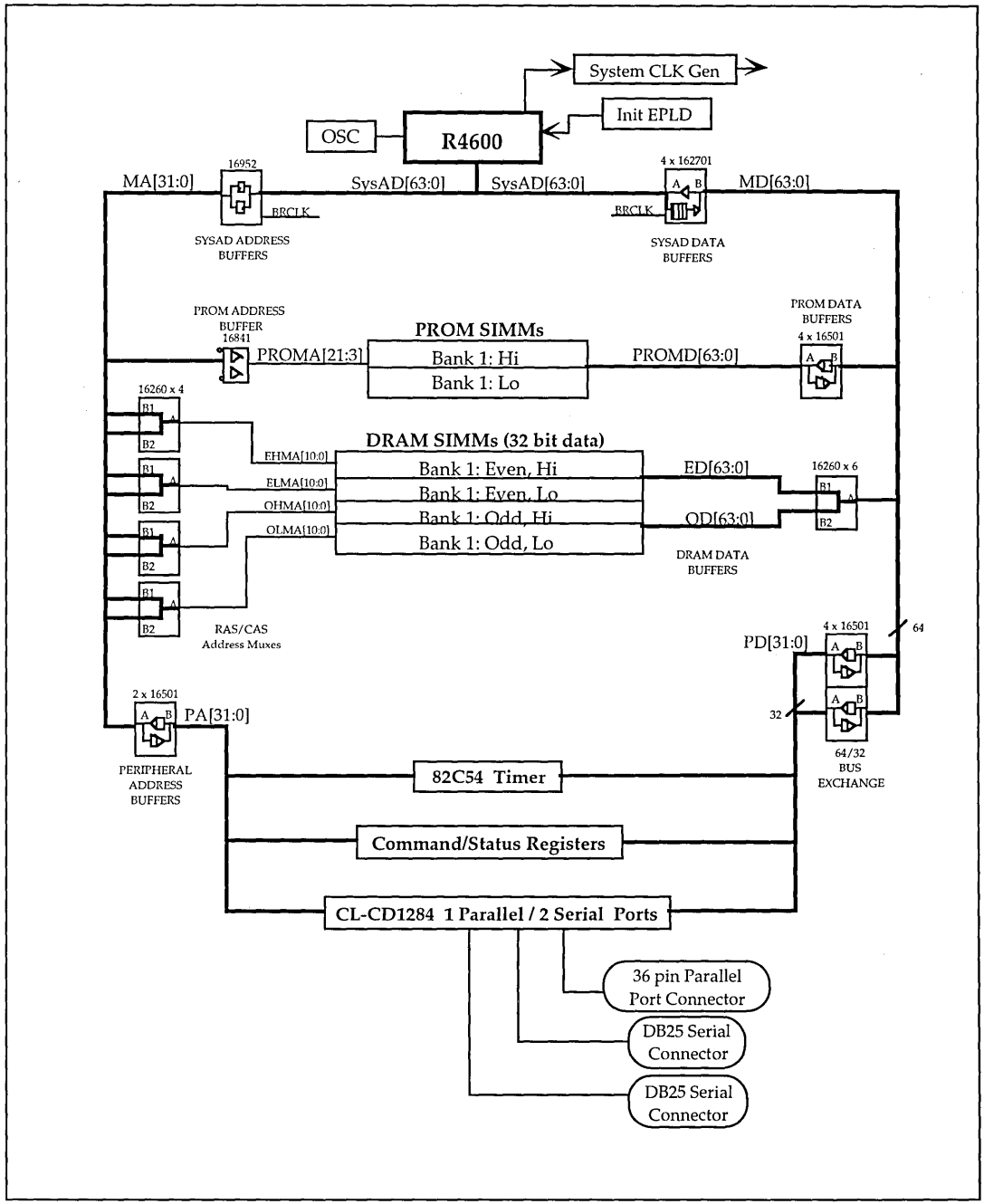

Figure 1 79S464 R4600 Evaluation Board Block Diagram

EXPLANATION OF FEATURES

The 79S464 Evaluation Board is configured as a standalone board, and requires only a standard RS232-C CRT video terminal and a 5 volt power supply for operation. The board can be placed on a flat tabletop surface by using the removable standoffs which are provided for physical support.

The 79S464 board contains two 512Kx32 PROM SIMMs. Main memory consists of 4, 16, or 64 MBytes, using 256Kx32, 1Mx32, or 4Mx32 DRAM SIMMs. There are two serial ports and one external timer in addition to the internal timer on the R4600.

The boot EPROM contains IDT's System Integration Manager (IDT/sim), a debug monitor kernel that supports download of code from host systems, remote debug interface, execution control commands including single stepping and instruction tracing, memory probing, register probing, line-based assembly, and disassembly of code.

The board supports the use of 32-bit wide DRAM SIMMs through the use of hardware jumper options. The board can be populated with up to 4 SIMMs: 256Kx32, 1Mx32, or 4Mx32 DRAM SIMMs. Thus, the board supports from 4 to 64MBytes of main memory.

A MIPS workstation, SPARCstation, or PC/AT can be connected to the 79S464 via one of the serial ports and user developed code (generated using a cross-compiler such as GNU/GCC++, MIPS/C, or the IDT/c compiler) can be downloaded to the board.

The 79S464 is designed around the IDT79R4600 RISController. The R4600 is a highly integrated version of the Orion family of RISControllers and includes 16KBytes of on chip instruction and 16KBytes of on chip data cache. For further details on the R4600 RISController, please refer to the *R4600/R4700 Hardware User's Manual* and the R4600 data sheet.

The 79S464 can be used to evaluate the performance of the R4600 or the R4700. In addition, the 79S461, when populated with the R4650, can be plugged into the R4600 CPU socket. This allows the R4650's performance in the system to be evaluated as well.

The 79S464 is constructed using both through-hole devices and surface mount on a 13" x 10" PCB rectangular form factor laminate board with standoffs, and is intended for use as a standalone bench top device.

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Ordering Information:

Each kit is shipped with an evaluation board, complete schematics, and PAL equations, A user's manual includes instructions on downloading code, operating the Software Integration Manager, and providing the corrent timing interfaces to additional hardware. Boards are shipped with the R4600 CPU plugged-in.

Evaulation Board

R4600 Evaluation Kit 79S464

Integrated Device Technology, Inc.

IDT/sim™ SYSTEM INTEGRATION MANAGER ROMABLE DEBUGGING KERNEL

IDT79S901

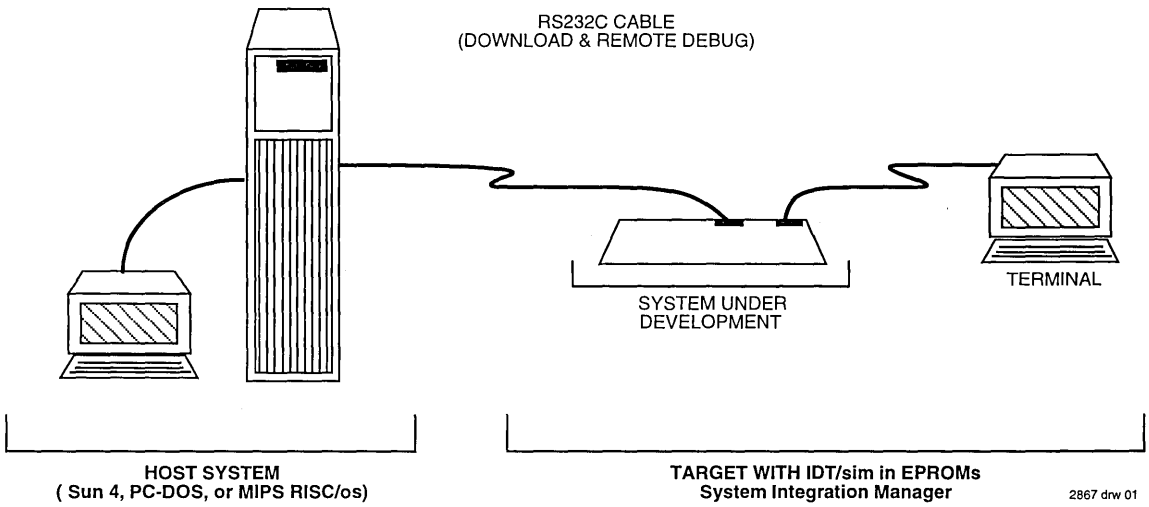
FEATURES

- Complete source code provided
- Robust debug monitor
- Supports remote source-level debug
  GDB—IDT/c tool chain
  DBX—MIPS tool chain
- Remote file access—connects target to remote host file system
- Ethernet and Centronics support for fast download
- Diagnostic tests for memory, cache, MMU, FPA, and system
- Adaptable to systems with or without hardware floating point accelerator
- Includes a variety of device drivers
- Easy to add new user interface commands and I/O device drivers

Powerful Tool for Integration of RISController Based systems

The IDT79S901 System Integration Manager (IDT/sim) is a ROMable debug monitor product that permits convenient control and debug of RISC systems built around IDT's R30xx RISController™, R4400™, R4600™, R4700™ and R4650™ CPUs. Facilities are included to operate the CPU under controlled conditions: examining and altering the contents of memory, manipulating and controlling R30xx, R4xxx resources (such as cache, TLB and coprocessors), loading programs from host machines, and controlling the path of execution of loaded programs.

IDT/sim source code includes IDT's MicroMonitor, a very simple monitor which requires only a UART and ROM to be functional for performing the initial debugging and integration of new hardware.



IDT/sim Features

IDT/sim is a software tool to help system designers debug hardware designs and port software to systems based on one of the R3000 ISA CPUs, R4400, R4600, R4700 and R4650. The software is supplied in EPROMs on most IDT RISC Development products, and may be purchased in source-code form so it can be modified, compiled and installed on your system.

IDT/sim provides all the basic functions needed to get a new hardware design debugged and to port and debug software on it. Typically, the monitor is compiled and burned into EPROMs that are plugged into the target system. Approximately 115KB of EPROM is needed for the binary code, and 71KB of RAM is needed for storing variables. Once installed, the designer communicates with the monitor via a simple terminal connected to an RS-232 port on the target system. Source code is included to support a variety of UARTs for this port. On start-up, the monitor will determine the cache and main memory sizes automatically.

Diagnostics

The monitor includes a set of diagnostic routines for testing the integrity of the hardware. The diagnostic suite includes: main memory tests which exercise all address and data paths; a cache memory test which runs memory tests on both caches, checks tag memory, and verifies that instructions can be executed from cache; a system test which checks the ability to read and write full words, half-words, and bytes and checks the cache operation for valid, hit/miss, and invalidation; a MMU test which checks the operation of the TLB inside the CPU; and a Floating Point test which tests the functionality of the on-chip FPA, including exception interrupts.

Download Support

Object code created on a software development system can be downloaded in either ASCII S-records or binary formats to the target system's memory. The code can be produced with IDT/c, the MIPS RISCross Compiler tools, or several third party compiler toolchains.

The IDT/sim console may also be used as a terminal to a software development system accessed through a second serial port. On targets which implement ethernet, utilities are also available to support ethernet downloads, and remote file access.

Debug Commands

A variety of commands are included in IDT/sim to support software/hardware debug. IDT/sim commands can be grouped into several categories, including: Execution Control (breakpoint, call, continue, go, gotill, next, step, unbreak); Memory Commands (assemble, cache flush, compare, disassemble, dump, dump cache, dump registers, fill, fill registers, move read/write cache, search and substitute); TLB Commands (dump, flush, map, pid and probe); Remote Debug (source-level debug with gdb on and IDT/c Host or dbx on a MIPS RISC/os system; and Communications (remote file access, terminal emulator and set baud rate).

Run-Time Support

IDT/sim includes over 50 functions that can be called by user's programs to perform common I/O and R30xx, R4xxx control operations. A complete list of commands is listed later in this document.

Feature Set

R4650 Orion Support: IDT/sim has been upgraded to support the latest 64-bit RISController family member, the 79R4650. This support has been implemented as a series of "IFDEF" options to the base 32-bit source tree. This approach allows a common set of features across 32 and 64-bit targets with a single development environment.

R3710/15 Support: IDT/sim now supports IDT79R3710/15 Laser printer integrated system controller for IDT R30xx RISController family. Features supported are: ROM controller, DRAM controller, Centronics, Timer, Printer interface diagnostics.

IDT MicroMonitor: IDT/sim includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware.

Source-level Debug: Fully integrated with IDT's new compiler toolchain (IDT/c Version 5.1) which supports source-level debug using gdb. IDT/sim supports gdb as a front end (with full access to /sim's commands) or use of an ASCII terminal in a stand-alone mode.

Remote File Access: IDT/sim has implemented features to allow connection of the target with a remote host file system allowing file transfer between target and host at run time. As an example, this can be useful for accessing large data images residing on a host without linking them with the application.Ethernet support is also included.

Trace Facility: Traces the memory accesses of a user program. Provides for tracing the path of execution, reads-from memory, or writes-to memory. Trace qualifiers allow the tracing of a specific instruction or class of instructions or references to particular memory ranges. The user may stop tracing on the following conditions: trace buffer full, hitting a breakpoint, executing a specific instruction, or accessing a specific memory range. The trace buffer contents may be displayed using standard R30xx, and R4xxx family mnemonics.

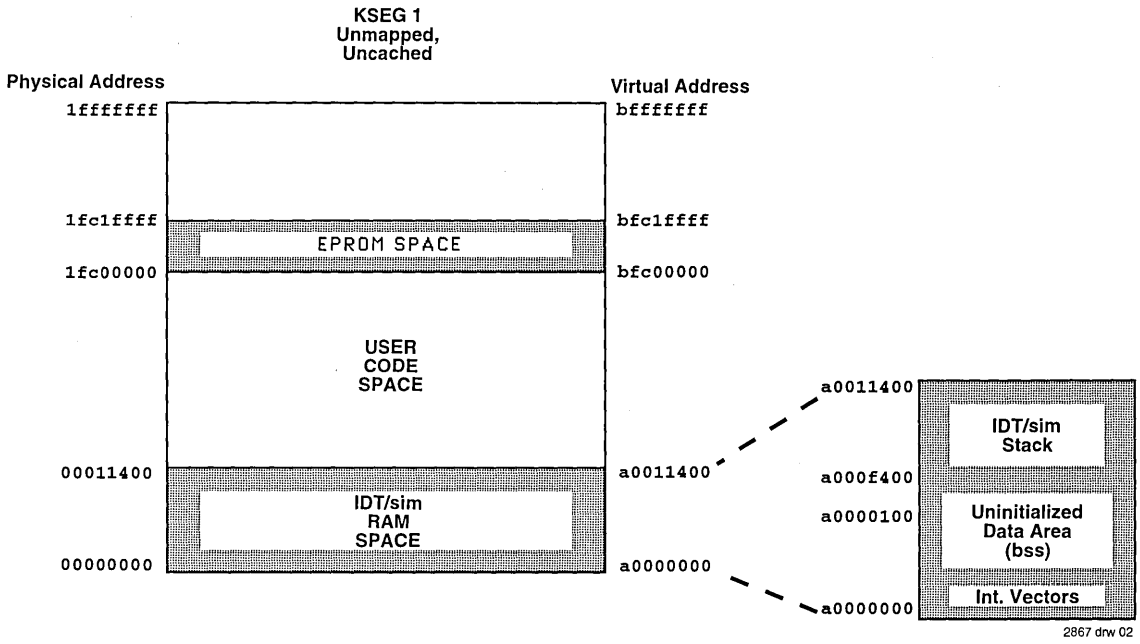


Figure 2 IDT/sim Memory Map

Figure 2 shows the memory utilized by IDT/sim. The EPROM space starts at virtual address bfc00000, which is the R3000's start-up address. The compiled version of IDT/sim with all features included occupies about 115KB of EPROM space, and is normally placed in 128KB of EPROM. IDT/sim uses main memory to store interrupt vectors, variables, and a stack. Approximately 71KB of RAM space is reserved for this data.

IDT/sim COMMANDS

asm <addr> examine and change memory interactively using standard assembler mnemonics

benchmark/bm
Facilitates benchmarking

brk|b [addresslist]
Set/display breakpoints

cacheflush/cf [-i|-d]
Flush the I-cache and/or the D-cache

call|ca <address> [arg1 arg2 ... arg8}
Call subroutine with up-to 8 arguments

checksum|cs
Display the checksums for an address range

compare|cp [-w|-b|-h] <RANGE> <destination>
Compare the block of memory specified by RANGE to the block of memory that starts at *destination*

cont|c
Continues execution of the client process from where it last halted execution.

dbgint|di [<-e|-d DEV>]
Debug interrupt enable/disable - allows 'break key' to generate external interrupt

debug|db [DEV]
Enter remote debug mode

dis <RANGE>
Disassemble target memory specified by RANGE

disptag|dt [-i] RANGE
Displays the instruction or data cache tag values and data contents

dr [reg#|name\reg_group]
Print out the current contents of register(s)

dt
Dump the trace buffer

dump|d [-w|-h] <RANGE>
Dump the memory specified by RANGE to the display

enable DEVICE
Connect to remote hosfor file access

fill|f [-w|-h|-b|-l|-r] <RANGE> [value_list.]
Fills memory specified by range with value_list

fr [-s/-d] <reg#|name> <value>
Fill <reg#name> with <value>

go|g [-n] <address>
Start execution at address <address>

gotill|gt <address>
Continue execution until address <address>

help|? [commandlist]
This command will print out a list of the commands available in the monitor. If a command list is supplied, only the syntax for the commands in the list is displayed

history|h
Displays the last 16 commands entered

idb [DEVICE] Connect to remote host source level debugger.init/i
Initialize prom monitor (warm reset)

load|l [options] DEV
Download code to target

move|m [-w|-b|-h] <RANGE> <destination>
Move the block of memory specified by RANGE to the address specified by *destination*

next/n [count]
Step over subroutine calls

rad [-o|-d|-h]
Set the default radix to the requested base.

rc [-i] <-w|-b|-h] <RANGE>
Isolate and read from cache

regsel|rs [-c|-h]
Select either the compiler names or the hardware names for registers

search|sr [-w|-b|-h] <RANGE> <value> [mask]
Search area of memory for value.

seg [-0|-1|-2|-u]
Set the default segment to the requested k-segment.

setbaud/sb DEV
Set the baud rate on a serial channel

step|s [<count>]
Single step count times

sub [-w|-h|-b|-l|-r] <address>
Examine and change memory interactively.

t {-a/-o/-e/-d/-r RANGE/-w RANGE/-c RANGE/-i INS/-m MSK}
Trace command

tc [-e BPNUM] [-d BPNUM]
Trace conditionally command

te [DEV]
Connects the console port straight though to a second serial port

tex [RANGE]
Exclude tracing calls to RANGE

tlbdump|td [RANGE]
Dumps the contents of the TLB

tlbflush|tf [RANGE]
Displays the current process identifier (pid)

tlbmap|tm [-i index] [-ndgv] <vaddress> <paddress>
Virtual-to-physical mapping of the TLB

tlbpid/ti [pid]
Set/display TLB PID

tlbptov/tp|tm <physaddr>
Probe the TLB

ts [-b/-f/-o/-r RANGE/-w RANGE/-i INS/-m MSK]
Stop trace command

unbrk|ub <bpnumlist>
Clear breakpoints

wc [-i] [-w/-b/-h] <RANGE> [value_list]
Isolate and write to I or D cache

wtfile <filename> [value_list]
Write file to remote host file system

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RUN TIME SUPPORT ENTRY POINTS

_exit
atob
clear_cache
cli
close
exc_utlb_code
flush_cache
get_mem_conf
get_range
getchar
gets
install_command
install_immediate_int
install_new_dev
install_normal_int
ioctl
longjmp
open
printf
putchar
puts
rclose
read
reinit
reset
restart
rfileinit
rgets
rlseek
ropen
rprintf
rread
rwrite
set_mem-conf
setjmp
showcar
sprintf
strcat
strcmp
strcpy
strlen
tokenize
timer_start
timer_stop
write

DEVICE DRIVERS (INCLUDED IN SOURCE CODE)

68681/2681 DUART
8530 SCC
SCSI
Centronics Parallel
8254 Timer/Counter
8251 UART

ORDERING INFORMATION

To order an IDT board-level product, see EPROM order codes below. To order IDT/sim in source code, order the Internal Use License AND order the software on the appropriate source media. You may also order binary distribution rights for the run-time version of the monitor. Ask your IDT sales office for information.

LICENSES

Internal Source License 79S901SL

Permits purchase of up to six copies of source code (any media combination) and use of source code to develop run-time binaries on up to six machines at a time, but does not permit inclusion of the run time code in an end product. Also purchase one or more of the Source Media listed below.

Limited Binary Distribution Rights 79S901BDR-L

Extension to Internal Source License to permit inclusion of binary code into end product. Internal Source License must be referenced on order or ordered simultaneously. This license permits up to 100 copies to be distributed royalty-free. For additional copies, purchase Unlimited Binary Distribution Rights.

SOURCE MEDIA

IDT/sim source code can be compiled with either the MIPS C-compiler, or with IDT/c version 4.1 or later. Earlier versions of IDT/c cannot compile this code. The products listed below are media only and must be purchased with license 79S901SL, listed above.

Source for 386/486PC, MS-DOS 79S901DOS

Compile with IDT/c C-Compiler. Shipped with 1.44MB 3.5" diskettes.

Source SUN Machines 79S901SUN

Use with MIPS C-Compiler or with IDT/c. Developmental Use License number must be referenced on order, or must be ordered simultaneously.

Integrated Device Technology, Inc.

IDT/c™ Multi-Host GNU C-Compiler System

IDT7S930

FEATURES:

- ANSI C-Compliant GNU Compiler, Assembler, Linker, Librarian, and ANSI Libraries
- Full Development Environment Including start-up code, cache management routines, etc.
- Efficient Software Floating Point Emulation Library for systems without hardware FPU. Includes Transcendentals
- GDB Provides full source and assembly level debug through IDT/sim™ interface
- Sun 4 (Sparc™), PC-DOS™, and SGI Irix 5.2™ Host Platforms
- Fully object code compatible with MIPS RISCross Compilers™
- Supports entire IDT family of MIPS ISA Processors (R3000/R3500™, R3041™, R3051™, R3052™, R3071™, R3081™, R4400™, R4600™·R4650™, and R4700™)

OPTIMIZING C-COMPILER SYSTEM:

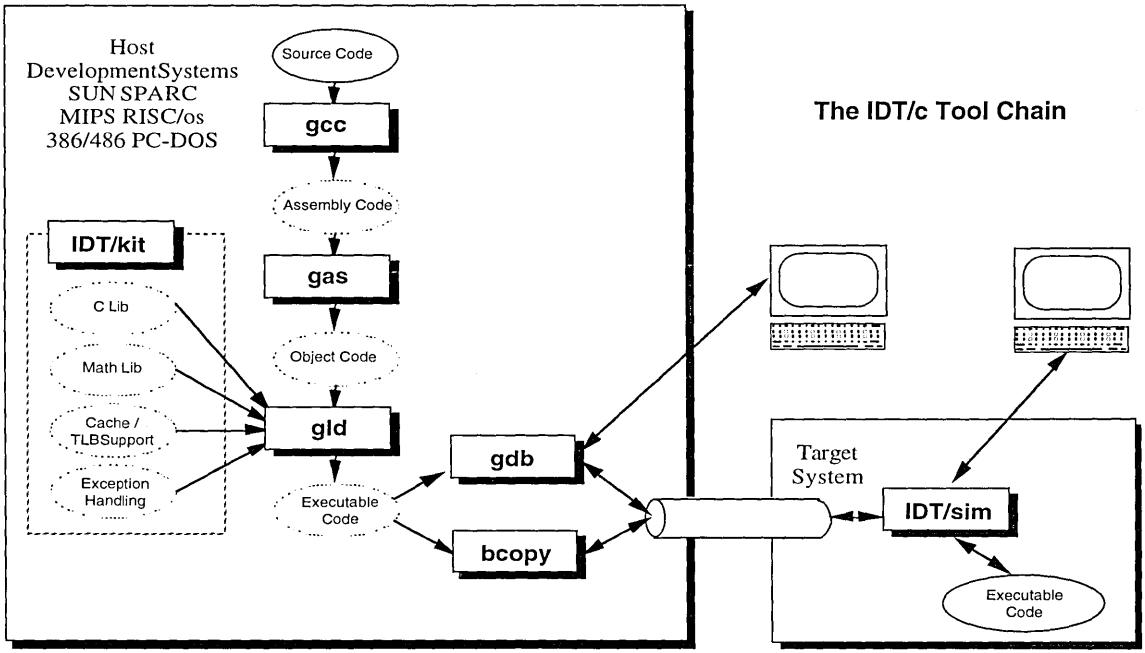
IDT/c is a C-compiler system for the IDT RISController™ family of embedded microprocessors. It supports development for any of the MIPS R3000 and R4000 family of microprocessors and their derivatives, including the IDT Orion Family.

The toolchain has been specifically designed for developing and debugging code that runs on a remote target. The compiler system includes the GNU C-compiler, assembler, linker, librarian, and source level debugger. The full GNU suite of libraries is included and it is supplemented by the IDT/kit™ libraries in binary form.

IDT/kit is a complete set of architecture-specific code (including start-up code, cache and exception management code, etc.) optimized for RISController family development. A complete assembly language floating point emulation library is also included for use in systems without a hardware FPU. IDT/kit is also available in source form.

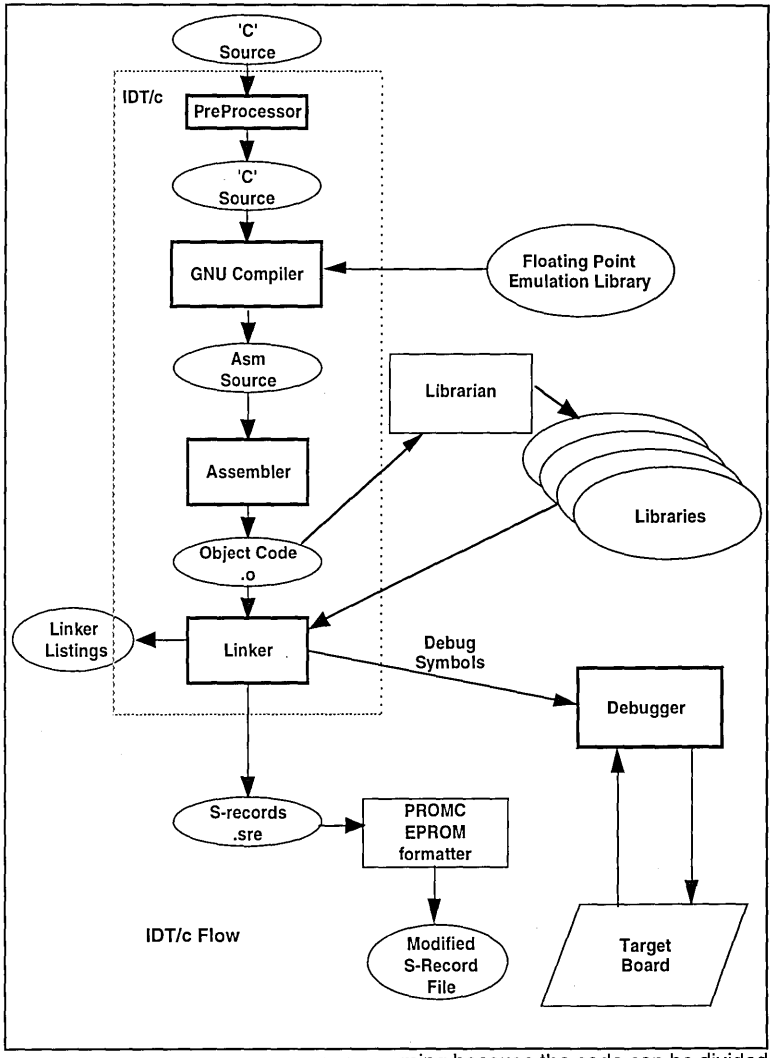
IDT/c is available for execution on SunOS™, and SGI Irix 5.2 workstations as well as PC-DOS hosts. Other host ports are available from 3rd parties.

New features in release 5.1/6.1 of IDT/c include an upgrade to the current release of the GNU compiler suite, full implementation of gdb support and an improved floating point emulation library.



OVERVIEW

The IDT/c compiler system is a complete development package for CPUs based on the R3000 and R4000 architecture. It contains an optimizing cross compiler, assembler, linker, and download utilities. The 'C'-compiler is compliant with ANSI 'C' standard and generates optimized code equal in performance to the best available C-compilers. The assembler supports the R3000 machine instructions and architecture described in the book *MIPS RISC Architecture*, by Gerry Kane, including both native and synthetic instructions. The complete IDT/c package runs on a variety of host machines and operating systems, and is fully compatible with other IDT development software, such as IDT/sim and IDT/kit.



Compiler

The C pre-processor is GNU cpp and the compiler itself is the GNU C Compiler gcc. All C-preprocessing features are supported. The entire toolchain included in IDT/c has been tested for compliance to the ANSI C standard using the Plum Hall test suite. The C-compiler performs extensive optimization in multiple passes through the code. Switches can be used to select particular optimizations.

The output of the compiler is an assembly language file. Modules compiled by IDT/c can be assembled and linked in the MIPS environment with modules compiled by the MIPS compiler. It is also possible to use IDT/c to compile, assemble and link modules which have been generated for the MIPS toolchain.

Optimizing Assembler

The IDT/c assembler implements the MIPS native and synthetic instruction set. Both big and little endian versions of the compiler are supplied in a standard IDT/c 5.1/6.1 package. The assembler produces object (".o") files which can be linked together with other object files or libraries to produce an executable file. All object files produced by IDT/c are in MIPS ECOFF format and are compatibile with the MIPS RISCross™ compilers. This allows a user to link code generated by IDT/c with objects or libraries generated by MIPS compilers. This is essential when using a real-time operating system or code libraries which are provided in binary and have been compiled using MIPS' compilers.

Linker

The linker combines separately assembled program files into one object module. Command line switches or script files may be used to define the placement in memory of program segments.

There are several types of output file formats supported, including S-Records, Intel hex, and binary image. The S-Record files are useful in downloading to target boards. The hex format file is useful for EPROM programming because the code can be divided into multiple files under this format. S-Records can be downloaded to a target containing the IDT/sim monitor using a supplied download utility.

Floating Point Library

IDT/c includes a floating point emulation library. A switch in the compiler is set at compile time to determine how the compiler should handle floating point instructions. In the normal mode, it will produce R3010 Floating Point Accelerator (FPA)-compatible instructions in the object code. This mode results in the highest performance for targets, which include the R3010, or for sys-

tems based on the R3500 or R3081, which include a R3010 compatible hardware floating point accelerator on-chip. If the switch is set the other way, the compiler will insert calls to the floating point emulation library instead, and the floating point emulation library must be available at link time. Because the compiler knows about the library during compile time, it can perform optimizations not otherwise possible and minimize the execution penalty for using software instead of hardware. This mode allows systems without a R3010 (such as those based on an R3041, R3051, or R3052) to implement efficient floating point arithmetic while using a lower cost CPU.

Librarian

IDT/c supports object code libraries to reduce the number of files that must be dealt with explicitly during program development. Many compiled routines may be stored in a single library file by using the Librarian utility. At link time, the linker extracts only the routines actually used.

Gdb—Remote Source Level Debugger

Remote debugging differs from the 'conventional' in several ways. The control of a target program relies on a communication line and debugging agent on the target instead of using operating system signals and related services.

Gdb has been enhanced to work with IDT/sim to provide full control of the target program. The distinguishing features are: a program mode in which gdb executes scripts that contain debugging and flow control commands; and host file services which provide the target program with full access to the host file system. The required physical link between host and target is a single RS232 line, though IDT/sim can be modified to use whatever interface is available in hardware.

It is also possible to use direct low-level IDT/sim debugging commands from a gdb session.

Remote file services

IDB supports file open, close, read, write, seek; printf; and gets commands in the standard C library format.

FLOATING POINT EMULATION MODE

When floating point and double length variables are used in C programs, compilers usually produce assembly instructions that directly operate on floating point arguments and use a designated register set to hold floating point operands. The C-compiler is aware of underlying hardware and attempts to produce optimal code by using all available resources.

The R3000 architecture has the floating point coprocessor in separate chip (R3010). There are numerous floating point instructions that operate on the 32 floating point registers inside the R3010. When floating point hardware is not present—for example, an R3000 without the R3010, or a R3041, R3051 or R3052 controller chip—executing programs that use floating point arithmetic requires software that can compensate for the missing hardware. There are two basic solutions to this problem: trapping on the floating point instructions at execution time and relying on the trap handler simulating the FPU in software; or modifying the compiler so that it does not produce any instructions for the FPU in its output.

Using the operating environment to trap all attempts to execute instructions on (non-existent) floating point hardware offers the advantage of using a single object code version of the application whether hardware FPU is present or not. The disadvantage is that the complete FPU state machine must be emulated since the code produced by the C-compiler assumes the real hardware is present. The code that must be executed for each FP instruction is substantial: the trapping overhead for each FP instruction, the maintenance of the FP state machine, and the instructions to execute the required FP operation on integer hardware.

For example, the sequence below requires 3 traps, each of which involves saving all the registers used in the particular trap routine, maintaining the state of the 'virtual' FP register set somewhere in memory, performing the actual FP arithmetic (double addition), and updating the 'virtual' FPU status register bits.

```
lwc1        $f14, ($9)
lwc1        $f15, 4($9)
add.d       $f8, $f14, $f6
```

The solution implemented in IDT/c is to switch the compiler to a different mode for the two environments. In emulation mode, the compiler does not assume presence of any additional hardware, so only R3000 instructions are produced, and FP operations are performed by calls to special routines. The calls are compiler-generated and there is absolutely no difference on the C source level. The same C program that generated the example above would generate the following code in IDT/c emulation mode.

```
lw          $4, ($9)
lw          $5, 4($9)
jal         __adddf3
```

The only overhead is that of performing FP operations on the R3000 integer hardware. On floating point intensive applications, IDT/c typically yields execution times four to five times slower than R3010 execution times, but eight to twelve time faster than the trap-based hardware floating point emulation method described above.

IDT/C PERFORMANCE

IDT/c Version 5.1/6.1 was developed with the goal of improving several aspects of the usefulness of the toolchain, and to provide a solid base upon which to build further performance improvements and feature enhancements. The main areas of interest were reliability, maintainability, debugger functionality, and floating point emulation performance.

ORDERING INFORMATION

The IDT/c C-Compiler is an efficient C-compiler system based on the popular GNU C and hosted on a variety of computers. The IDT/c system includes the compiler, assembler and linker, as well as the full GNU library suite and the IDT/kit libraries. All versions of the software are shipped on a single CD-ROM, readable by DOS and SUN systems. A single user license is included with the product. Contact your IDT sales office for multiple user licensing.

IDT/c Cross Compiler Package and Embedded Development Libraries

The IDT/c package listed below includes the GNU C Cross Compiler for MIPS and the entire IDT/kit library suite in binary form, including the IDT software floating point emulation library. For developers who wish to customize the code to fit their hardware environment, the source to IDT/sim and IDT/kit is available, as is a binary distribution license for each product.

IDT/c Cross Compiler Package

Single User Binary, 386/486 machine, MS-DOS or SUN SunOS 4.x on a multi-format CD-ROM 79S930

Integrated Device Technology, Inc.

IDT/kit™ KERNEL INTEGRATION TOOLKIT

IDT79S909

FEATURES:

- Source code and object code versions of commonly used routines for R3000 and R4000 ISA CPUs
- Start-Up Code to initialize CPU, MMU, and C runtime environment
- Cache control code to size, initialize, flush, and clear for DMA
- Re-entrant Exception Handler
- Floating Point Emulation Library and Transcendental Math Functions
- ANSI Standard C Library
- Time Support Functions
- MicroMonitor for initial hardware debug
- Interface Library to IDT/sim™ monitor

ESSENTIAL CODE FOR R30XX SYSTEMS

IDT/kit (Kernal Integration Toolkit) consists of libraries and routines for important system software operations for R3000-based and R4000-based CPUs. Modules are provided for initializing systems, handling interrupts, servicing floating point exceptions, and many other other common operations. Libraries are included for floating point emulation, transcendental arithmetic routines, and ANSI standard C functions. All IDT/kit libraries are supplied in source code (C and assembly) and in object modules compiled for both little- and big-endian systems and for both hardware and software emulation floating point.

IDT's MicroMonitor is also included in the IDT/kit package. The MicroMonitor is a very simple monitor for initial debug of new hardware. It requires only that the CPU, EPROM, and a serial port be operational. The MicroMonitor can be an invaluable aid for detecting state machine problems in first article hardware.

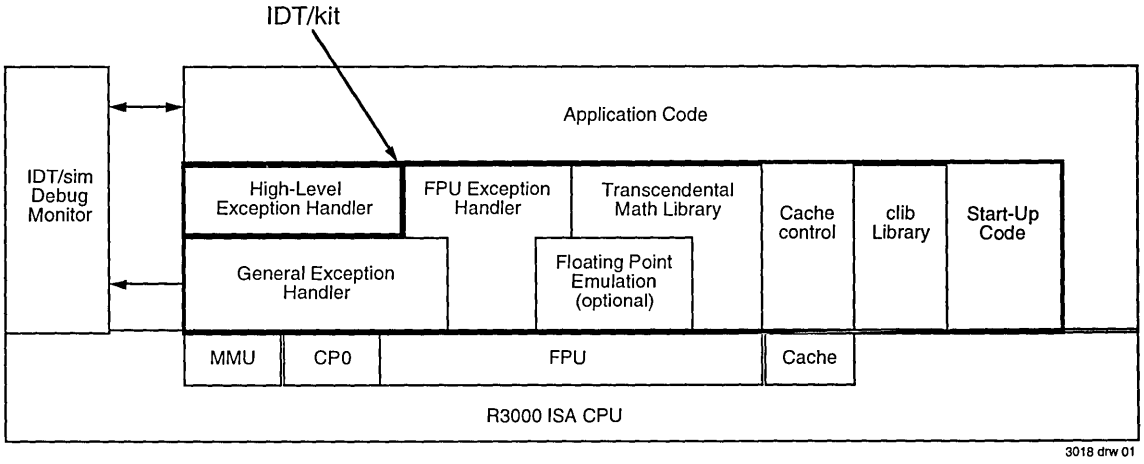


Figure 1. Schematic Representation of the modules in IDT/kit, showing how they control parts of the R3000 or R4000 CPU and connect to IDT/sim, IDT's debug monitor.

IDT/KIT™ FEATURES

The IDT Kernel Integration Toolkit (IDT/kit) consists of a set of libraries ready to be linked with user developed code. IDT/kit contains functions that would normally be furnished by an operating system like UNIX but without the overhead. Functions are provided for initializing the system, memory management, exception handling and time support; an ANSI standard 'C' library and a math library with transcendental functions are supplied.

This environment can be compiled with IDT/c or MIPS compilers, Big or Little Endian, Cached or Uncached and with an optional Emulation Mode if no Floating Point Accelerator is installed. With IDT/kit, floating point emulation support is transparent to the user application.

IDT/kit typically would co-exist with IDT/sim and become part of a total development and debug environment. On a system where IDT/sim is installed, all the commands, entry points and debugging facilities of IDT/sim are available to the Kernel Integration Toolkit. When using IDT/sim, IDT/kit filters exceptions first. If IDT/kit does not handle an exception, then it is passed to IDT/sim.

Default exception handlers intercept exceptions, save the environment, preserve the Exception Registers for later analysis, restore the environment and return to continue program execution. The default handlers can easily be replaced or extended with more robust handlers written by the user.

IDT/kit relieves the application from the low-level tweaking necessary to get started, but leaves easy hooks into the system for expansion and polishing as the development progresses. All code is supplied in source code (C and assembly), to allow easy access for modifications needed to tailor the system to specific needs. This allows the programmer to shorten the project development time by easing the development of hardware-specific resources like cache, MMU and exception handling.

IDT/kit includes IDT's MicroMonitor, a very simple monitor for performing the initial debugging of new hardware. The only hardware which must be functioning to run the MicroMonitor is the CPU, EPROM and a serial port function. This allows for immediate debugging of hardware even when the DRAM memory is *not* functioning.

IDT/KIT COMPONENTS

1. MICROMONITOR:

A small assembly language monitor to aid in debugging the hardware design. The MicroMonitor requires only that three hardware resources are functional: the CPU can execute instructions, the EPROM can provide instructions and the UART can send and receive characters.

2. IDT_CSU.S, THE START UP MODULE

Supplies the initialization and set up code necessary for operation of the system.

- initialize the Status Register
  a) clear parity error bit
  b) set Coprocessor 1 usable bit correctly
  c) clear all IntMasks enabled
  d) set kernel/user mode
- set Cause Register
  a) clear software Interrupts Pending
- clear bss area
- establish temporary uncached user stack
- determine memory and cache sizes
- establish permanent stack at Top of Memory
- flush I and D-Caches
- if there is a Translation Lookaside Buffer invalidate it
- initialize library if IDT's standard C Library is used
- initialize exception handlers
- jmp to users' main()

3. LIBIKIL.A, KERNEL INTEGRATION LIBRARY:

The IDT Kernel Integration Library (libikil.a) is a library which can be linked to user programs to supply functions required to support the environment of the R3000 ISA family. This library is divided into four sections: Memory Handling, General Exception Handling, Floating Point Exception Handling and Time Support Functions.

a. memory handling — the full range of functions necessary to manage main memory, cached memory and the Translate Lookaside Buffers
b. general exception handling — the functions used in enabling and handling any interrupt exceptions, hardware or software, asserted by the CPU
c. floating point exception handling — provides the support for the Floating Point Unit, the R3010, or for Emulation Software for floating point arithmetic , "strongly recommended" by the IEEE Standard 754-1985. It is transparent to the application code calling this interface whether hardware or software emulation is being employed.
d. Time support functions using the 8254 timer as a prototype

4. LIBILNK.A, THE IDT/SIM INTERFACE LIBRARY:

The IDT/sim linking module which interfaces with all the functions available with IDT/sim not defined with IDT/kit or by the user

5. LIBIC.A, ANSI STANDARD C LIBRARY:

The IDT Standard C Library (**libic.a**) is a standard archive library which, when linked with the users' filename.o files, provides the functions defined by the ANSI standard including standard I/O, String and Character functions, Utility functions, and memory allocation functions.

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6. LIBIMATH.A, MATHEMATICS LIBRARY:

The IDT Math Library (**libimath.a**) is a standard archive library which, when linked with the users' filename.o files, provides the transcendental functions required for standard math processing. Whether hardware floating point or software emulation is be used is transparent to the application code calling this library.

HOW IDT/KIT IS USED

IDT's Kernel Integration Toolkit includes a robust set of tools for the embedded controller developer. They are "packaged" in accessible, modular containers, the IDT/kit libraries. The four libraries, arranged by function, supply most of the routines required by RISC applications. Only those libraries needed to resolve function calls must be entered on the link command line; the others are never accessed which establishes a fully modular environment.

IDT/kit serves as an envelope for the installation's application code. The source module, idt_csu.S, is linked first, then the development code and, finally, any kit libraries required to support function calls. This allows the developer to concentrate on the application and not waste resources re-developing the support routines. Although the libraries are provided complete and ready to link, source code for all the functions is also distributed to allow easy examination for information or as a template for additional routines. All the necessary Make/Batch files are included to facilitate any changes, additions or corrections. Some examples:

strcpy (or any of the C library routines) — perhaps your installation has developed a super-algorithm. It isn't quite ANSI Standard, but does your job better. Simply edit the source in the clib subdirectory (or replace the one that is there), execute the makefile for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, libic.a, now contains your code. Your module could also be placed on the system Link line before the corresponding library and the call would be resolved before the library is searched.

Interrupt Handling — you want the default interrupt handler (it's already there), but you need an additional flag set. Edit the routine in the killib subdirectory, run the Make/batch file for your configuration (IDT/c or MIPS, Big or Little Endian, REAL or Emulation Mode) and the library, libikil.a, now contains "your "default interrupt handler.

These kinds of simple modifications allow the IDT/kit routines to be tailored for a specific system without expending the time to investigate and understand all the routines; only the section applicable to the application need be tweaked and the Make/Batch files provide easy guidelines for doing it.

IDT/kit FUNCTION LIST

CSU_IDT.S: START UP MODULE

start() ---------- Startup routine

LIBIKIL.A: KERNEL INTEGRATION LIBRARY

Programmable interval timer driver

install_timer_driver() install timer driver
i8254init() ---------- timer driver init
i8254open() ---------- opens the device
i8254ioctl() ---------- i/o control function

Assembly level exception handling

disable_int() ---------- clear selected interrupts
enable_int() ---------- set selected interrupts
exc_norm_code() ---- general exception code
exc_utlb_code() ------ UTLB Miss code
exception() ---------- general exception code
init_erc_vecs() -------- init vector code
longjmp() ---------- go to setjmp() point
other_excp() ---------- handles other exception
setjmp() ---------- set setjmp() state

High level exception handling

add_ext_int_func() -- set default exc handler
clr_except_ptr() ------ clears setjmp pointer
config_memory() ----- size of main memory
extern_int() ---------- external interrupt code
exception() ---------- general exception code
get_except_ptr() ----- get execption pointer
init_tlb() ---------- initializes TLB
mem_exc_hdlr() ------ memory exception code
sae_errmsg() ---------- prints msg & exits
set_except_ptr() ------ sets setjmp pointer
spurious_int() -------- unexpected ext interrupt

FPU interface module

fp_defaultHdlr() ------- default handler
fp_disableTrap() ----- clears trap bits in fpcsr
fp_enableTrap() ------ sets trap bits in fpcsr
fp_init() ---------- init floating Point
fp_int() ---------- FP interrupt dispatcher
fp_signal() ---------- user exception handler
fpclr_stickybits() ------ clear sticky bits in fpcsr
fpget_excregs() ------ get Exc Regs
fpget_fpcsr() ---------- get FP Control/Status
fpget_RM() ---------- get rounding mode fpcsr
fpget_stickyBits() ---- get sticky bits fpcsr
fpset_fpcsr() ---------- set FP Control/Status
fpset_RM() ---------- sets rounding mode
fpset_stickyBits() ---- sets sticky bits in fpcsr
fpset_excregs() ------- set Exc Register buffer

Assembly language FPU access

clr_CAUSE() ---------- clears SW bits in CAUSE
get_CAUSE() --------- returns contents of CAUSE
get_fpcsr() ---------- returns FPU csr
get_cp0epc() ---------- gets epc
get_STATUS() -------- status register contents
set_CAUSE() --------- sets CAUSE Register
set_fpcsr() ---------- sets FPU csr

Functions affecting I/D Caches

clear_Dcache() ------- invalidate portion of Dcache
clear_Icache() -------- invalidate portion of Icache
config_Dcache() ----- size of Data cache
config_Icache() ------- size Instruction cache
flush_Dcache() ------- invalidates entire Data cache
flush_Icache() -------- invalidates entire Inst cache
get _mem_conf() ----- gets memory configuration
size_cache() ---------- finds size of cache

Assembly language TLB access

resettlb() ---------- invalidates tlb entry
ret_tlblo() ---------- returns tlb entry lo reg
ret_tlbhi() ---------- returns tlb entry hi reg
ret_tlbpid() ---------- returns tlb process ID field
set_tlbpid() ---------- sets current tlb pid
tlbprobe() ---------- probes tlb
tlbmapping() ---------- maps tlb entry

Time support module

time_cmd_init() ------- starts clock
time_init() ---------- init timer drvr
timer_int ---------- clock interrupt routine
time() ---------- returns timer tics
time_it() ---------- times the selected function

Assm language Write Buff Routine

wbflush() ---------- flushes the write buffer

LIBILNK: IDT/SIM LINK LIBRARY

Cache Routines

clear_cache() --------- clears portion of I and D
flush_cache() --------- flushes entire I and D

Character Routines

getchar() ---------- inputs a character
putchar() ---------- outputs a character
showchar() ---------- makes character visible

Command Line Interpreter

cli() ---------- Command Line Interpreter
get_range() ---------- parses the range spec
tokenize() ---------- parses the command line

Exit and Reenter Routines

_exit() ---------- exit & return to monitor
promexit() ---------- exit & return to monitor
reinit() ---------- reinitializes monitor
reset() ---------- resets prom monitor
restart() ---------- restarts the debug monitor

Help Screen Routine

help() ---------- prints Help Screen

ROUTINES TO EXTEND IDT/SIM

install_commands() - adds user commands
install_immediate_int nstalls user interrupt
install_new_dev() ---- installs new device
install_normal_int() -- installs user interrupt

Routines for low level I/O

close() ---------- closes an open device
open() ---------- opens a device
read() ---------- reads data from device
write() ---------- writes data to an device

I/O Control Function

ioctl() ---------- sets I/O flags / calls drivers

7

Routines to save /restore context

longjmp() ----------restores setjmp context
setjmp() ----------saves the current context

Memory configuration routines

get_mem_conf() -----returns mem configuration
set_mem_conf()------sets the mem configuration

Formatting print routine

printf() ----------formatting print routine

Dummy routines for libic

_init_file() ----------dummy file routine
_init_sbrk()----------dummy sbrk routine

String routines

atob()----------Ascii string convert
gets()----------gets string function
puts()----------outputs string to I/O
strcat()----------concatenates two strings
strcmp()----------compares two strings
strcpy()----------copies one string to another
strlen()----------returns length of string

LIBIC.A: ANSI STANDARD C LIBRARY

abs()----------absolute value of integer
atof()----------fp value of an Ascii string
atoi()----------integer value of Ascii str
atol()----------long value of Ascii str
bsearch()----------binary search of a array
div()----------rem & quot of int division
ferror()----------error during a file operation?
atexit()----------routines called at exit time
exit()----------Terminate with status
fopen()----------open file/ret file stream ptr.
fclose()----------close a file
fdopen()----------open stream
labs()----------absolute value of long arg
ldiv()----------rem & quotient of division
free()----------free allocated memory
malloc()----------memory allocation
realloc()----------reallocation of memory
fscanf()----------read data from a file
printf()----------display data on the std I/O
qsort()----------quick sort routine
rand()----------generates random number
srand()----------seed for random num genr
sbrk()----------mem allocation bp routine
scanf()----------read data from standard input
sprintf()----------output data into a string
sscanf()----------read data from a string
memcmp()----------compare two memory arrays
memcpy()----------memory array copy
memmove()----------memory array move
memchr()----------ret ptr to first matched char
memset()----------place a char in memory array
strlen()----------return string length
strcmp()----------strings are identical?
strcpy()----------copy string
strncpy()----------copy n characters of a string
strchr()----------ret ptr to first match of a char
strchr()----------ret ptr to last match of a char
strcat()----------concatenate a strings
strncat()----------concatenate strings
strspn()----------len of prefix of str
strcspn()----------len of prefix of str
strpbrk()----------ptr to first occur of any char
strstr()----------string a occurs in string b?
strtok()----------return tokens
strtod()----------convert string to a double
strtol()----------convert string to long int

LIBIMATH.A: TRANSCENDENTAL MATH LIBRARY

acosh()----------inv hyperbolic cosine of x
acos()----------cos -1 (x)
asin()----------sin -1(x)
asinh()----------inverse hyperbolic sine of x
atan()----------tan -1 (x)
atan2()----------tan -1 (x/y)
atan2()----------tan -1 (x/y)
atanh()----------inv hyperbolic tangent of x
cabs()----------complex absolute value
exp()----------exponential function e^x
hypot()----------sqrt (x*x + y*y)
z_abs()----------double-complex absolute
cbrt()----------cube root of x
cosh()----------hyperbolic cosine of x
exp()----------exponential function e^x
expm1()----------exponent (x - 1)
ceil()----------smallest int not < x, double
floor()----------largest int not > x, double
rint()----------nearest x in dir of round
fmod()----------fp remof x/y, sign of x
atan()----------tan -1 (x)
cos()----------cos of x
exp()----------exponential function e^x
log()----------natural logarithm ln(x), x>0
log10()----------base 10 logarithm, x>0
sin()----------sine of x
sqrt()----------square root of x, x>= 0
tan()----------tan of x
xtoi()----------raises x to integer power, i
sim_fpint()----------simulate IEEE standard trap
sim_unint----------sim FP Unimplemented Op
log()----------natural logarithm ln(x), x>0
log10()----------base 10 logarithm, x>0
log1p()----------log (1 + x)
log__L()----------og(1 + x) -2s/s
pow()----------x^y
cos()----------cos of x
sin()----------sine of x
sinh()----------hyperbolic sine of x
copysign()----------returns x with sign of y
drem()----------x - n*y, integer nearest n
finite()----------1 = real x; 0 = INF or NAN x
logb()----------exponent of x^n
scalb()----------x * (2**n) computed for n
sqrt()----------square root of x, x>= 0
tan()----------tan of x
expm1()----------exponent (x - 1)
tanh()----------hyperbolic tangent of x
fabs()----------absolute value of number
frexp()----------returns mantissa;exp in *ptr
isnan()----------tests for floating point NaN
ldexp()----------returns quantity *2^exp
pow()----------x^y

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