Intel® 80303 I/O Processor Initialization Considerations

White Paper

July 2000

Order Number: 273392-001

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1.0 Summary

This paper describes some of the changes that have been made on the Intel® 80303 I/O processor relative to the Intel® i960® RM/RN I/O processor. These changes if not taken into considerations may cause the 80303 I/O processor to malfunction. For a complete list of changes made to the 80303 I/O processor please refer to the "Design Considerations when Migrating from the 80960 RM/RN I/O Processor to the 80303 I/O processor" document. These changes may have an impact for those trying to port an existing 80960 RM/RN I/O Processor initialization code to the 80303 I/O processor.

Table 1. Partial Changes from Intel® i960® RM/RN I/O Processor to Intel® 80303 I/O Processor

Register Name	Address	Description
RFR - Refresh Frequency Register	0000 1568H	The default value has changed from 300H on the Intel® i960® RM/RN I/O processors to 000h on the Intel® 80303 I/O processor. A value other then 000H must be programmed into this register to cause refresh cycles.
SDCR.2 - SDRAM Control Register	0000 1504H	On the i960RM/RN I/O processors this bit can be used to determine the SDRAM data bus width. 0 = 32-bits 1 = 64 bits On the 80303 I/O processor, this bit is a reserved bit because only 72-bit (ECC always on) data bus width is supported. If this bit is read it may return a '0'.
SBR0[2:0] - SDRAM Boundary Register	0000 150CH	On the i960RM/RN I/O processors, bits SBR0[5:0] are used to program the upper boundary of SDRAM bank 0. On the 80303 I/O processor, bits SBR0[2:0] are now reserved. Instead, bits SBR0[7:3] are used to program the upper limit. If this register is not properly programmed, the Memory Controller Unit (MCU) will not respond to read and write requests.
SBR1[2:0] - SDRAM Boundary Register	0000 1510H	On the i960RM/RN I/O processors, bits SBR1[5:0] are used to program the upper boundary of SDRAM bank 0. On the 80303 I/O processor, bits SBR1[2:0] are now reserved. Instead, bits SBR1[7:3] are used to program the upper limit. If this register is not properly programmed, the Memory Controller Unit (MCU) will not respond to read and write requests.
PIRSR[3:0] - PCI Interrupt Routing Select Register	0000 1050H	On the i960RM/RN I/O processors, after reset the secondary PCI interrupts (S_INTx#) are routed to the 80960 core. On the 80303 I/O processor, after reset the secondary PCI interrupts (S_INTx#) are routed to the primary PCI interrupts (P_INTx#). The user must ensure the secondary interrupts are steered correctly.
ECCR.3 - ECC Control Register	0000 1534H	On the i960RM/RN I/O processor, this bit can be used to turn ECC either on or off. On the 80303 I/O processor this bit is reserved since ECC is always turned on. The user must make sure that the SDRAM entries are initialized by writing 64-bit words using stl instruction. This will generate and write the correct ECC code into the SDRAM entries.

2.0 References

2.1 Related Documents

- *Design Considerations Migrating from Intel® 80960RM/RN I/O Processor to Intel® 80303 I/O Processor* Application Note (273396)