THE JIM WILLIAMS PAPERS

MOST ENGINEERS THINK designing analog circuits for high-frequency and high-speed applications is a black art known only to a few wizards. If you are among that majority, prepare to enter the sorcerers' inner circle. Jim Williams has pried loose the secrets of practical, high-speed analog design. By codifying his observations, he has moved high-speed analog design away from the art realm and toward the engineering domain.

Williams presents his discoveries in the articles that follow. Each article is self-contained, so you won't have to read the first article to understand the second. He delves into the mysteries of power-supply bypassing, parasitic coupling, and compensation. He discusses ways to prevent amplifiers from oscillating, how to keep oscillators stable, and how to couple high-speed analog circuits to the digital world. He even discusses the problems you'll face when your analog circuits outperform your test equipment. In short, he tells you how to obtain full performance from your high-speed analog silicon.

Regarding this undertaking, Williams writes

Even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high-speed circuits can work only if you negotiate compromises with nature. Ignorance of or contempt for physical law is a direct route to frustration. Mother Nature laughs at dilettantes and dabblers. She crushes arrogance unknowingly.

Over the past 15 years, the name Jim Williams has become synonymous with analog design in EDN. He published his first article in EDN on May 5, 1975, while teaching and conducting research at the Massachusetts Institute of Technology. In 1979, he started a 3-year stint as a linear designer at National Semiconductor Corp. Williams joined Linear Technology Corp (Milpitas, CA) in 1982 and continued to write innumerable articles about his designs, which today cover almost every analog function you can name.

Williams' devotion to the art of analog design drives his successful and unconventional career. Although he has no formal degree in engineering—Williams describes his experience with formal education as an incredible impedance mismatch—Williams was designing circuits, or in his words, "bumbling around circuits," long before he'd heard of calculus. Williams now describes himself as a floater. He spends about half of his time as a staff scientist doing what he's done for the last 15 years: designing circuits and writing about them. The rest of the time he's either acting as a mentor for engineers at his company or designing circuits for specific customers.

Despite working in the competitive business of selling semiconductors, Williams manages to balance the commercial aspirations of his employer while designing and writing about circuits that often include a competitor's device. You are about to read his latest opus—the product of one year's effort. These secrets didn't pry loose easily, and Williams has a mountain of breadboards for proof. EDN is proud of its long-standing relationship with Jim Williams and is proud to present a work of this caliber.

Illustration by John Schreck

THE
JIM WILLIAMS
PAPERS

The mysteries of probing

Unless you master the mysteries of probing and oscillography, you'll be doomed to measuring the errors in your setup and oscilloscope, not the errors in your circuit.

Jim Williams, *Linear Technology Corp*

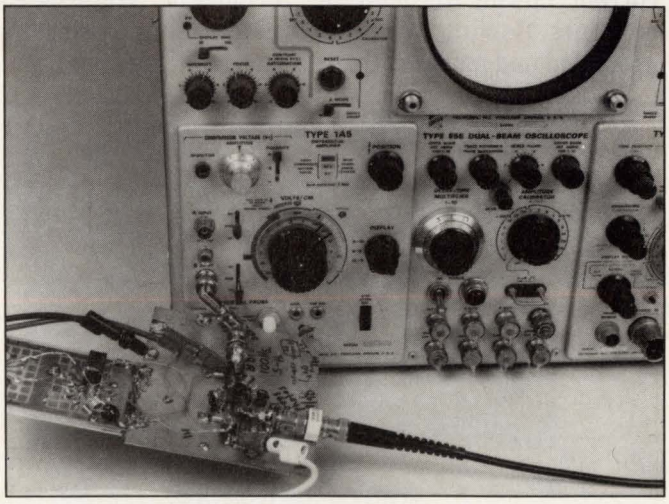
Measuring a high-speed linear circuit is a classic problem in observability. The problem is twofold: Stimulating and probing the circuit without disturbing its behavior and ensuring that the waveforms on your oscilloscope's screen are valid representations of your circuit's behavior. Problems can start before you apply power to your prototype.

Even something as simple as cabling requires thought. All coaxial cable is not the same. Always route high-speed signals to and from your circuit board with good-quality coaxial cable. Use cable appropriate to your system's characteristic impedance.

Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in distorted waveforms. A poor cable choice can adversely affect 0.01% settling in the 100- to 200-nsec region. Similarly, poor-quality cable can spoil even the cleanest pulse generator's 1-nsec rise time or purity. All too typically, inappropriate cable can introduce tailing, rise-time degradation, aberrations following transitions, nonlinear impedance, and other undesirable effects.

Other potential cabling problems begin at your circuit's input. The driven end of an input cable is usually an instrument (such as a pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. The cable and its termination, selected by the experimenter, often cause problems.

Fig 1a shows severe ringing on the pulse edges at the output of an unterminated pulse-generator cable. Reflections cause this ringing and you can eliminate it by terminating the cable. Always terminate the source with its characteristic impedance when driving cable or long printed-circuit traces. In the high-speed



One of the secrets of probing is that *sometimes the best probe is no probe. Oscilloscopes are so well designed that a 25-year-old scope suffices for 90% of today's applications.*

linear domain, any conductor longer than one inch is suspect.

In **Fig 1b** the cable is terminated, but ripple and aberration are still present following the high-speed edges. In this instance the terminating resistors' leads are lengthy (~¾ in.), sabotaging the wideband termination. The best terminating resistors for 50Ω cable are the BNC coaxial type. Their impedance vs frequency is flat into the GHz range. Although these terminators are practical on the test bench, they are rarely board-level components.

These coaxial terminators should not simply be resistors in an enclosure. Good grade, 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor. The terminators' designers devoted significant effort to the connections to the actual resistive element. In particular, the terminators have the largest possible connection-surface area to minimize high-speed losses.

Termination resistors

The best termination resistors for pc-boards are carbon or metal-film types having the shortest possible lead lengths. These resistors' "end-cap" connections provide better high-speed characteristics than the rod-connected composition types' connections. Wirewound resistors, because of their inherent, pronounced inductance, are completely unsuitable for high-speed work. This prohibition includes noninductive types of resistors.

Another termination consideration is disposing of the current flowing through the terminator. High-speed currents flowing from the terminating resistor's grounded end must not disrupt your circuit's operation. For example, returning terminator current to ground near the grounded positive input of an inverting op-amp would be unwise. The high-speed, high-density current flow could cause serious corruption of the op amp's reference. For example, 5V pulses through a 50Ω termination generate 100-mA current spikes.

This possible corruption is another reason why, for bench testing, the coaxial BNC terminators are preferable to discrete, breadboard-mounted resistors. In the coaxial types, the termination current returns directly to the source generator and never flows in the breadboard. Select terminations carefully, and evaluate the effects of their placement in your test setup.

Figs 2a and **2b** illustrate these terminators' performance nicely. In **Fig 2a**, a 1-GHz sampling scope (Tektronix 556 with 1S1 sampling plug-in and P6032 probe) monitors a 1-nsec pulse with 350-psec rise and fall times. The waveform is clean, with only a slight hint of ring after the falling edge. The setup used in **Fig 2a** is a high-grade BNC coaxial terminator. The setup in **Fig 2b** does not share these attributes. Rather, a 50Ω carbon-composition resistor with lead lengths of about ⅛ in. terminate the generator. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5× reduction to capture these unwanted events.

Connectors, such as BNC barrel extensions and tee-type adapters, represent a discontinuity in the cable and can introduce small but undesirable effects. In general, you should use them as close as possible to a terminated point in the system. Using them in the middle of a cable run provides only minimal absorption of their mismatch and reflections.

The worst offenders among connectors are adapters.

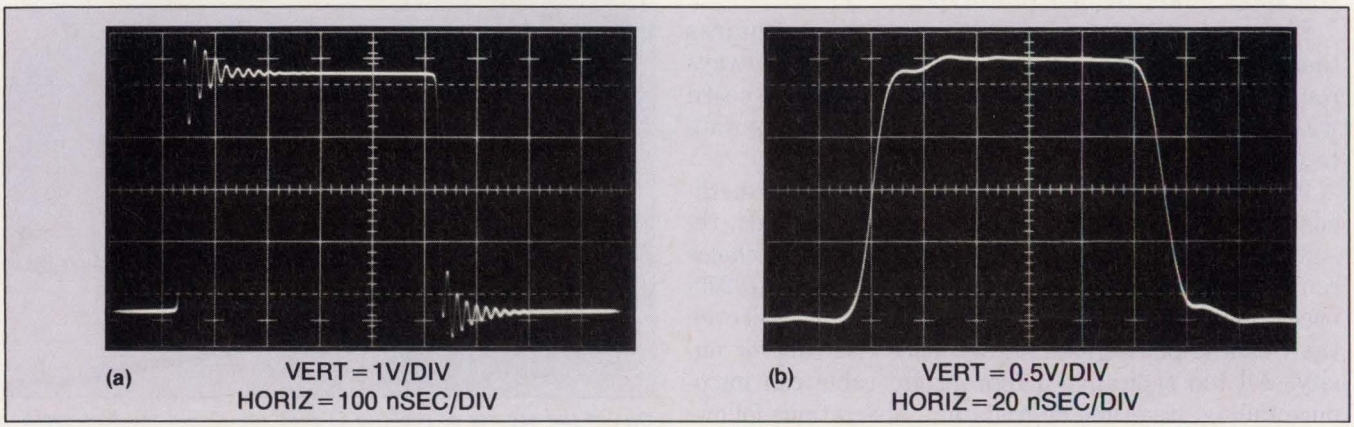


Fig 1—In scope photo a, *an unterminated cable causes severe ringing. In* ***b,*** *improperly spec'ed termination resistors reduce, but do not eliminate, ringing.*

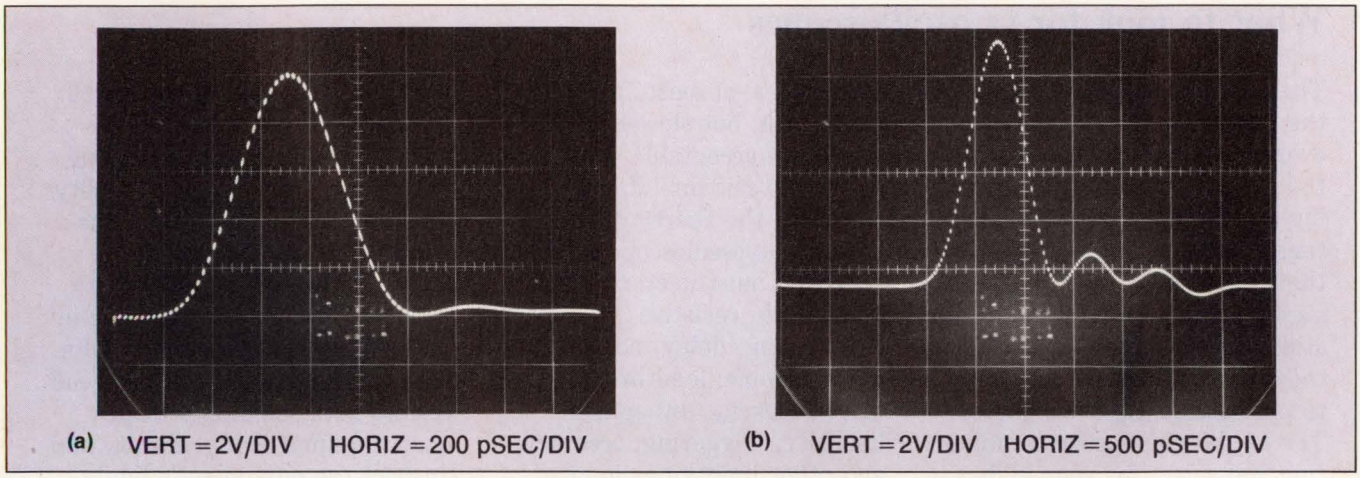


Fig 2—Coaxial-termination resistors (a) *are superior in performance to carbon-composition resistors (**b**).*

The lack of standard connectors among wideband instrumentation makes this situation unfortunate. The mismatch caused by a BNC-to-GR874 adapter at the input of a wideband sampling scope is small, but clearly discernible on an oscilloscope. Similarly, you can readily measure mismatches in almost all adapters on a high-frequency network analyzer, such as the Hewlett-Packard 4195A—even in theoretically identical adapters of different manufacture. (For additional wisdom and terror along these lines, see **Ref 1.**)

BNC connections are easily the most common, but not necessarily the most desirable, wideband connectors. The ingenious GR874 connector has notably superior high-frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

Choosing the proper probe

After you find the type of connector that is best for your needs, you must choose a probe. Your oscilloscope's probe becomes an integral part of the circuit under test. Therefore, choosing which oscilloscope probe to use for a measurement is absolutely crucial.

Sometimes, however, the best probe is no probe at all. In some circumstances, connecting critical breadboard points directly to the oscilloscope is not only possible, but preferable. Connecting directly to critical breadboard points provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases, however, the direct connection is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it.

Of course, this mechanical inconvenience is why equipment makers developed oscilloscope probes in the first place, and why they have put so much effort into their probes' development. (**Ref 2** is an excellent reference for the designing of probes.)

Probes are the most overlooked source of oscillographic mismeasurement. The most obvious culprit is probes' input resistance, but input capacitance usually dominates in a high-speed measurement. You can lose much time chasing phantom circuit events that are actually caused by improperly selected or applied probes. Pay particular attention to the probe's input capacitance. Standard 10-MΩ, 10× probes typically have 8 to 10 pF of input capacitance, with 1× types having much higher input capacitance.

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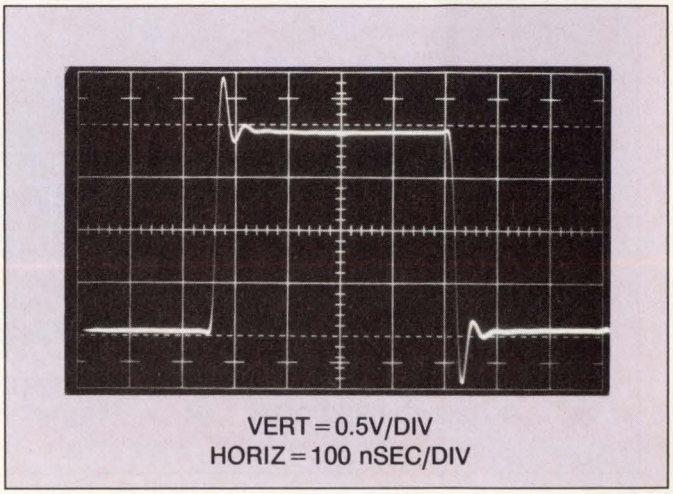

Fig 3—The capacitance of a probe clipped *to another node in the circuit distorts this amplifier's response.*

THE
JIM WILLIAMS
PAPERS

What to look for in oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. Perhaps only the zealotry devoted to timekeeping equals the protracted and intense development devoted to these machines. That instruments manufactured 25 years ago still suffice for more than 90% of today's measurements is a tribute to past oscilloscope designers. The oscilloscope-probe combination you select for your high-speed work is the most important equipment decision you can make.

Ideally, your oscilloscope should have at least 150-MHz bandwidth, but slower instruments are acceptable if you understand their limitations. Be certain of the characteristics of your probe-oscilloscope combination. You must keep rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy, and other limitations in mind. High-speed linear circuitry demands a great deal from test equipment, and you can save yourself countless hours by knowing your instruments well.

Engineers have wasted obscene amounts of time pursuing "circuit problems" that in reality arose from misunderstood, misapplied, or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, you can get good results with seemingly inadequate equipment if you know and respect the equipment's limitations.

Familiarity with equipment and thoughtful measurement technique permit useful measure-

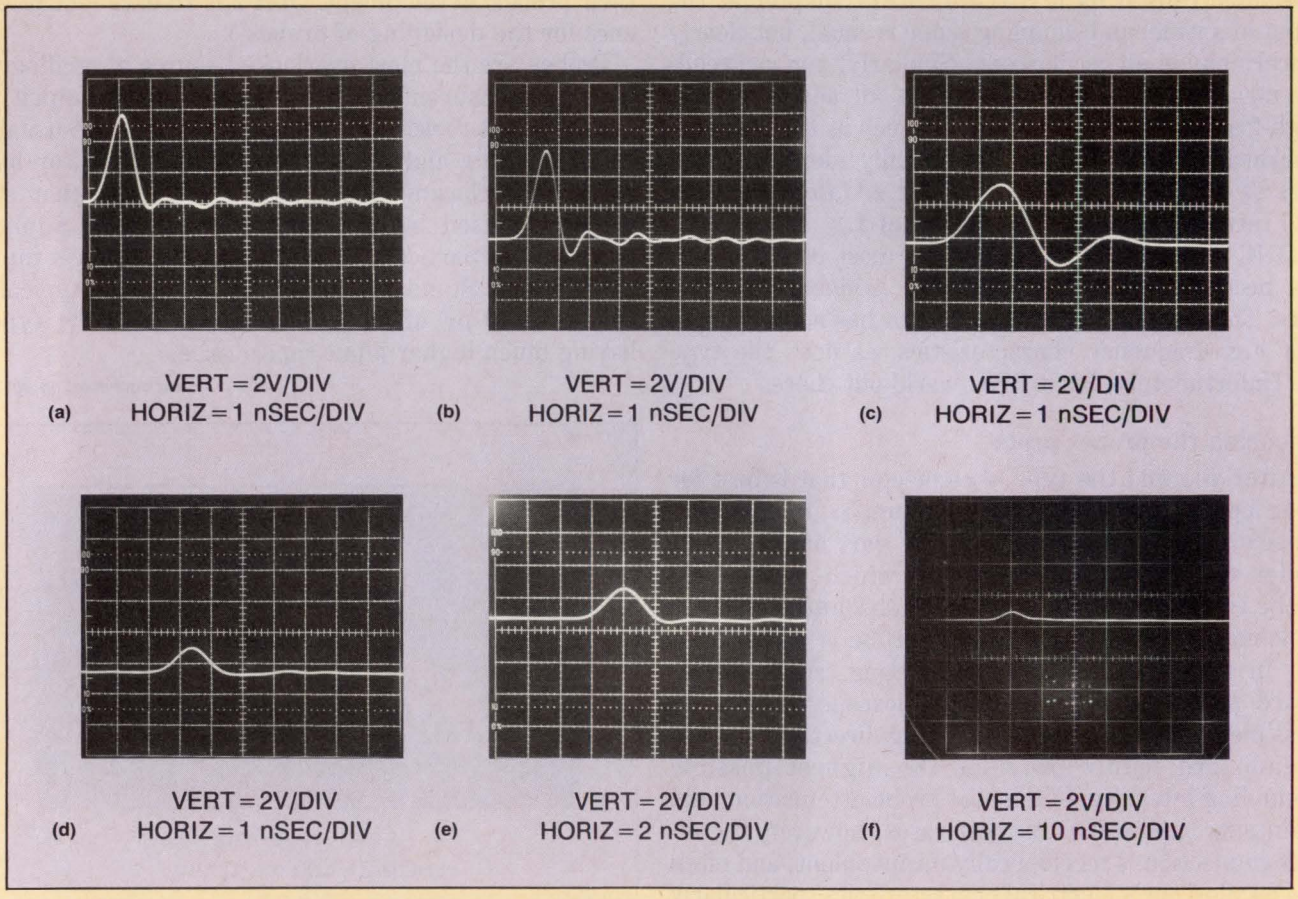

Fig A—This series of photos shows *what the fast pulse in* ***Fig 2a*** *(pg 167) looks like on a variety of oscilloscopes.*

ments seemingly beyond instrument specifications. A 50-MHz oscilloscope cannot track a 5-nsec rise-time pulse, but it can measure a 2-nsec delay between two such events. Using such techniques, you can often deduce the desired information. In some situations no amount of cleverness will work and you must use the right equipment (for example, a faster oscilloscope).

Sometimes "reality checking" a limited-bandwidth instrument with a higher-bandwidth oscilloscope is all that you need to do. For high-speed work, brute-force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high-speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if your budget is limited, spend for bandwidth.

Probe-oscilloscope combinations of varying bandwidths produce dramatic differences in their displays. The series of scope photos in this box shows what a fast pulse looks like on various oscilloscopes. **Fig 2a** (pg 167) in the main text shows the output of a very fast pulse (**Ref 3**) monitored with a 1-GHz sampling scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a hint of ringing after the falling edge. The rise and fall times of 350 psec are suspicious, as the sampling oscilloscope's rise time is also 350 psec.

Fig Aa shows the same pulse observed on a 350-MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1 nsec, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. Poor grounding technique (1½ in. of ground lead to the ground plane) creates the prolonged rippling after the pulse fall.

Fig Ab shows results from the same 350-MHz oscilloscope with a 3-GHz, 10× probe (Tektronix P6056, 50Ω input). Displayed results are nearly identical, because the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse's falling edge.

Fig Ac equips the same oscilloscope with a 10× probe specified at a 290-MHz bandwidth (Tektronix P-6047). Additionally,

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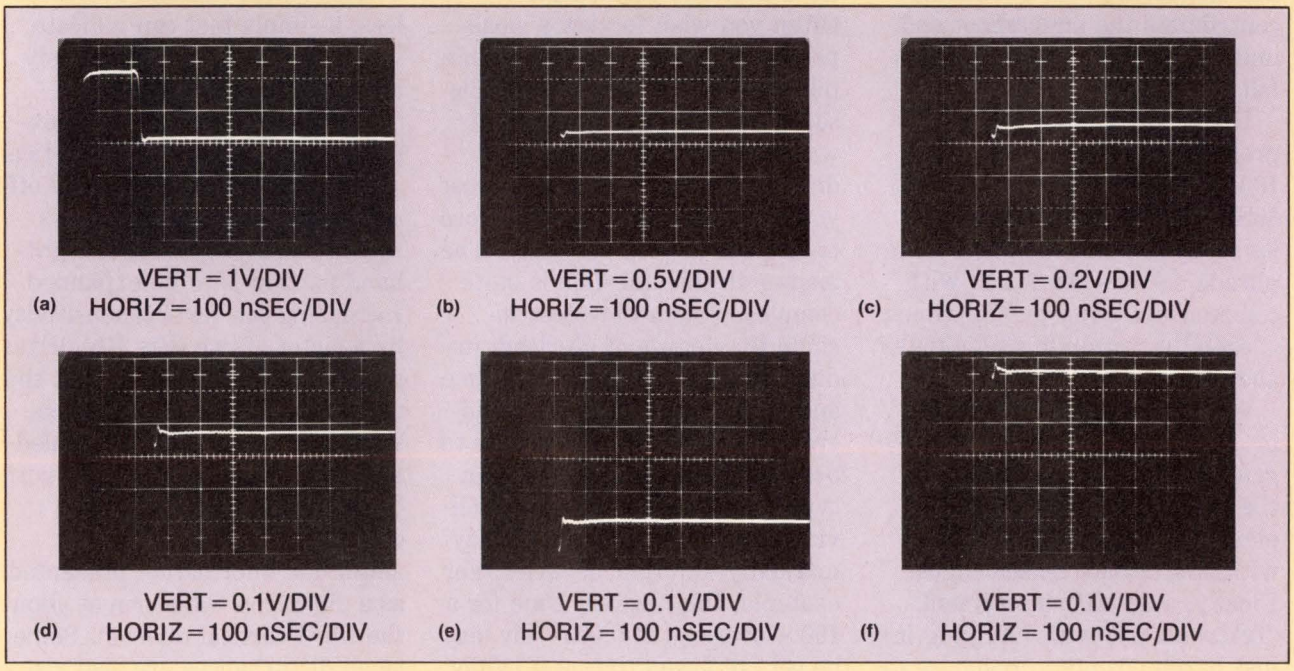


Fig B—Your particular oscilloscope may *perform peculiarly when overloaded, as this series of scope photos demonstrates.*

The probe-caused problem in **Fig 3** shows up as output peaking and ringing. In other respects the display is acceptable. A second 10× probe connected to the amplifier's summing junction causes this output peaking. Because the summing point is so central to analyzing op-amp operation, it often has a probe attached. At high speeds, the probe's 10-pF input capacitance causes a significant lag in feedback action, forcing the amplifier to overshoot and hunt as it seeks the null point. Minimizing this effect calls for probes having the lowest possible input capacitance, mandating FET types or special passive probes. Account for the effects of probe capacitance, which often dominate the probe's impedance at high-speeds. A standard 10-pF 10× probe, combined with a 1-kΩ source resistance, forms a 10-nsec lag.

But, by far, improper grounding is the greatest source of error in probe use. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is the parasitic inductance in the probe's ground connection.

Fig 4 shows an amplifier output that rings and distorts badly after rapid voltage excursions. Here, the circuit is not at fault; the probe's ground lead is too long. For general-purpose work, most probes come with ground leads about six inches long. At low frequencies this length is fine. At high-speed, the long ground lead looks inductive, causing the ringing shown.

Fast probes always come with a variety of spring clips and accessories designed to aid in making the

What to look for in oscilloscopes *(continued)*

the oscilloscope was in its 1-MΩ input mode, reducing bandwidth to a specified 250 MHz. Amplitude degrades to less than 4V, and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In **Fig Ad** a 100-MHz, 10× probe (Hewlett-Packard Model 10040A) substitutes for the 290-MHz unit. The oscilloscope and its setup remains the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned up grounding eliminates aberrations.

A Tektronix 454A (150 MHz) produced **Fig Ae**'s trace. A pulse generator connected directly to the oscilloscope's input. Displayed amplitude is about 2V, with appropriate 2-nsec edges. Finally, a 50-MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (**Fig Af**). Indicated amplitude is 0.5V, with edges reading about 7 nsec. This last display is a long way from the 10V and 350 psec that's really there.

A final oscilloscope characteristic is overload performance. Often you wish to view a small portion of a large waveform's amplitude. In many cases the oscilloscope must supply an accurate waveform after the display is driven off screen. How long must you wait after an overload before taking the display seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types. Among a given type, individual instruments often display markedly different behavior. For example, the recovery time for a 100× overload at 0.005V/div may be very different than at 0.1V/div. The recovery may also vary with waveform shape, dc content, and repetition rate.

With so many variables, clearly you must approach measurements involving oscilloscope overload with caution. Nevertheless, a simple test can indicate when overdrive is deleteriously affecting an oscilloscope.

Place the waveform to be expanded on the screen at a vertical sensitivity that eliminates all off-screen activity. **Fig Ba** shows such a display. The lower right-hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (**Fig Bb**) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, you can see small-amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of

lowest possible inductive connection to ground. Most of these attachments assume that your circuit has a ground plane—which it should have. Always try to make the shortest possible connection to ground; anything longer than one inch may cause trouble. The ideal probe-ground connection is purely coaxial. Probes mated directly to board-mounted coaxial connectors give the best results.

Sometimes determining if probe grounding is the cause of observed waveform aberrations is difficult. One good test is to disturb the grounding setup and see if changes occur. Touching the ground plane or jiggling probe-ground connectors or wires should have no effect. If you are using a ground-strap wire, try changing its orientation or simply squeezing it together to change and minimize its loop area. If any waveform change occurs, your probe grounding is unacceptable.

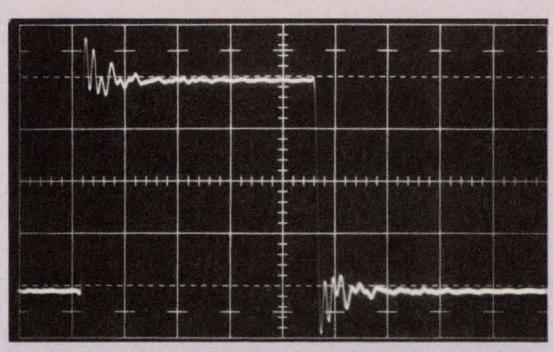


***Fig 4—Probe capacitance isn't the only fly in** the ointment; here, an overly long ground lead induces ringing.*

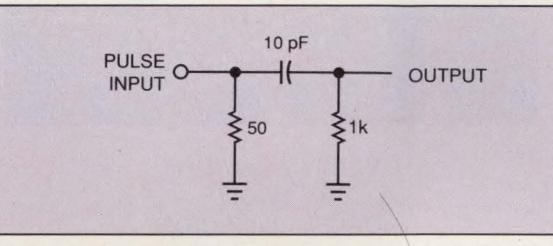


***Fig 5—Monitoring this simple circuit's** response to a pulse illustrates several potential probing problems.*

the original waveform is believable.

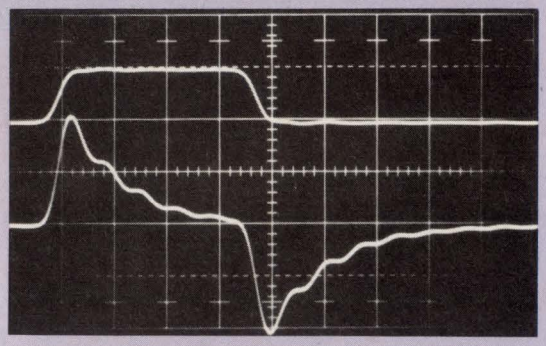
In **Fig Bc**'s display, gain is higher, and all the features of the **Fig Bb** example are amplified accordingly. The basic waveshape appears clearer, and the dip and small disturbances are also easier to see. No new waveform characteristics appear. The **Fig Bd** photo brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in **Fig Bc**. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble.

A further test can confirm that overloading is influencing this waveform. In **Fig Be**'s photo, the gain remains the same but the vertical position knob has repositioned the display at the screen's bottom. This shifts the oscilloscope's dc operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (**Fig Bf**). Obviously, for this particular waveform, you cannot obtain accurate results at this gain.

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low levels, a high-sensitivity differential plug-in is indispensable. The Tektronix 1A7 and 7A22 feature 10-μV sensitivity, although bandwidth is limited to 1 MHz. The units also have selectable highpass and lowpass filters and good high-frequency, common-mode rejection. Tektronix type 1A5, W, and 7A13 are differential comparators. They have calibrated dc nulling ("sideback") sources, letting you observe both small, slowly moving events on top of common mode dc or fast events riding on a waveform.

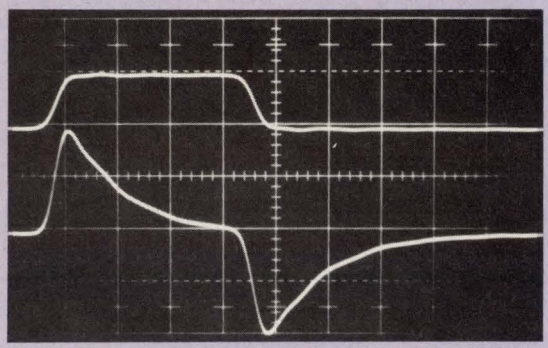
A special case is the sampling oscilloscope. Because of its nature of operation, a sampling scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples (**Ref 4**).

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. The **box,** "Measuring amplifier settling time," in the article "Subduing high-speed op-amp problems" (scheduled for the October 24 issue of EDN), shows ways to do this when measuring DAC/amplifier settling time to very high accuracy at high speed.



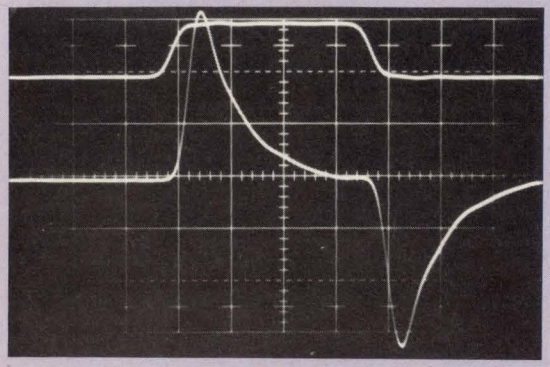
(a)

VERT = A = 5V/DIV
B = 1V/DIV
HORIZ = 10 nSEC/DIV



(b)

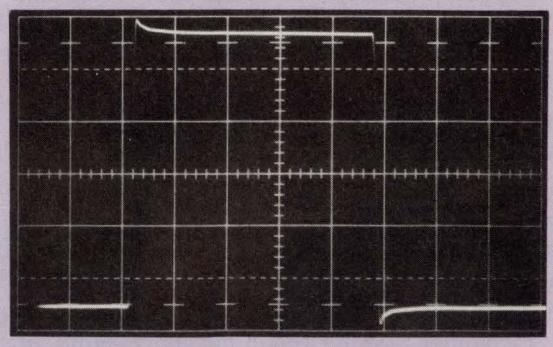
VERT = A = 5V/DIV
B = 1V/DIV
HORIZ = 10 nSEC/DIV



(c)

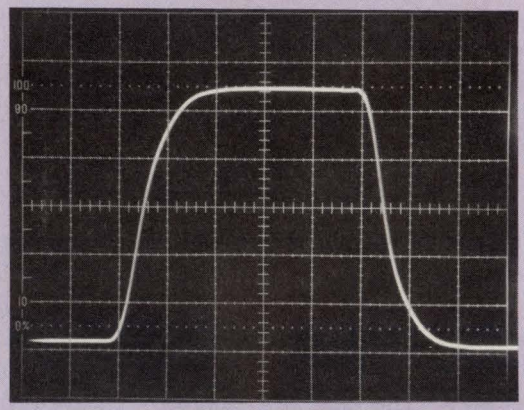
VERT = A = 5V/DIV
B = 1V/DIV
HORIZ = 10 nSEC/DIV

Fig 6—A probe's capacitance and ground-lead *inductance add ringing and distortion to the output (**a**). Substituting a spring clip for the ground lead cleans up the output trace somewhat (**b**). Substituting an FET probe for the ground lead (**c**) reveals a 50% amplitude distortion in **b**.*



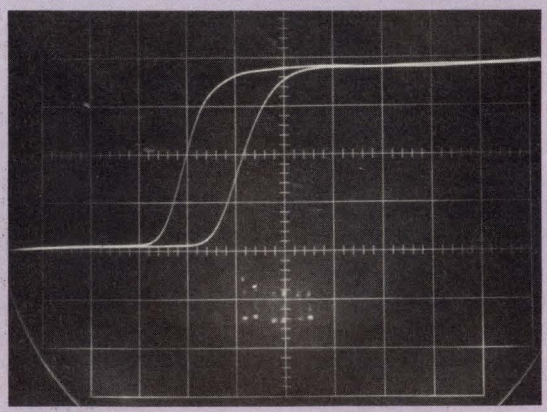
(a)

VERT = 2V/DIV
HORIZ = 50 nSEC/DIV



(b)

VERT = 0.5V/DIV
HORIZ = 20 nSEC/DIV



(c)

VERT = A = 0.5V/DIV
B = 0.5V/DIV
HORIZ = 10 nSEC/DIV

Fig 7—In a, a grossly miscompensated or improperly *selected oscilloscope probe causes an op amp to appear to be delivering an 11V output from a 5V supply. In **b**, a probe having insufficient bandwidth rounds off the edges of this waveform. Probes can also add significant delay to observed waveforms (**c**).*

The simple network of the circuit in **Fig 5** shows just how easily poorly chosen or used probes cause bad results. A 9-pF input-capacitance probe with a 4-in. ground strap monitors the output (**Fig 6a**). Although the pulse input is clean, the output contains ringing. Using the same probe with a ¼-in. spring-tip ground-connection accessory seemingly cleans up everything (**Fig 6b**). However, substituting a 1-pF FET probe (**Fig 6c**) reveals a 50% output-amplitude error in **Fig 6b**'s measurement. The FET probe's low-input capacitance allows a more accurate version of the circuit's action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5 nsec because of delay in its active circuitry. Hence, you must make separate measurements with each probe to determine amplitude and timing characteristics of the output.

Poorly compensated probe

In **Fig 7a**, the probe is properly grounded, but a new problem pops up. This photo shows an amplifier output excursion of 11V—quite a trick from an amplifier running from ±5V rails. Engineers commonly report this confusing problem when they work on high-speed circuits. The problem arises not because of a suspension of natural law, but from a grossly miscompensated or improperly selected oscilloscope probe. Use probes that match your oscilloscope's inputs and compensate them properly.

Fig 7b illustrates another probe-induced problem. Here the waveform's amplitude seems correct, but the amplifier appears slow, developing pronounced edge rounding. Here, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1× or "straight" probes. Their bandwidth is 20 MHz or less and their capacitive loading is high. Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope that has adequate bandwidth.

Mismatched probes account for the apparent excessive amplifier delay in **Fig 7c**'s amplifier. The display shows delay of almost 12 nsec for an amplifier that specs 6 nsec. Always keep in mind that various types of probes have different signal-transit delay times. At high-sweep speeds this effect shows up in multitrace displays as time skew between individual channels. Using similar probes will eliminate this problem, but measurement requirements often dictate dissimilar probes. In such cases you should measure the differential delays and then mentally factor them in to reduce error when interpreting the display. Note that active probes, such as FET and current probes, have signal transit times as long as 25 nsec. A fast 10×- or 50Ω-probe's delay can be inside 3 nsec. Account for probe delays in interpreting oscilloscope displays.

Fig 8a depicts a wildly distorted amplifier output. The output slews quickly, but the pulse's top and bottom recovery have lengthy, tailing responses. Additionally, the amplifier's output seems to clip well below its nominal-rated output swing. A common oversight is responsible for these conditions—An FET probe monitors the amplifier's output in this example. The probe's common-mode input range has been exceeded, causing the probe to overload, clip, and distort badly.

The rising pulse drives the probe deeply into saturation, forcing its internal circuitry away from normal

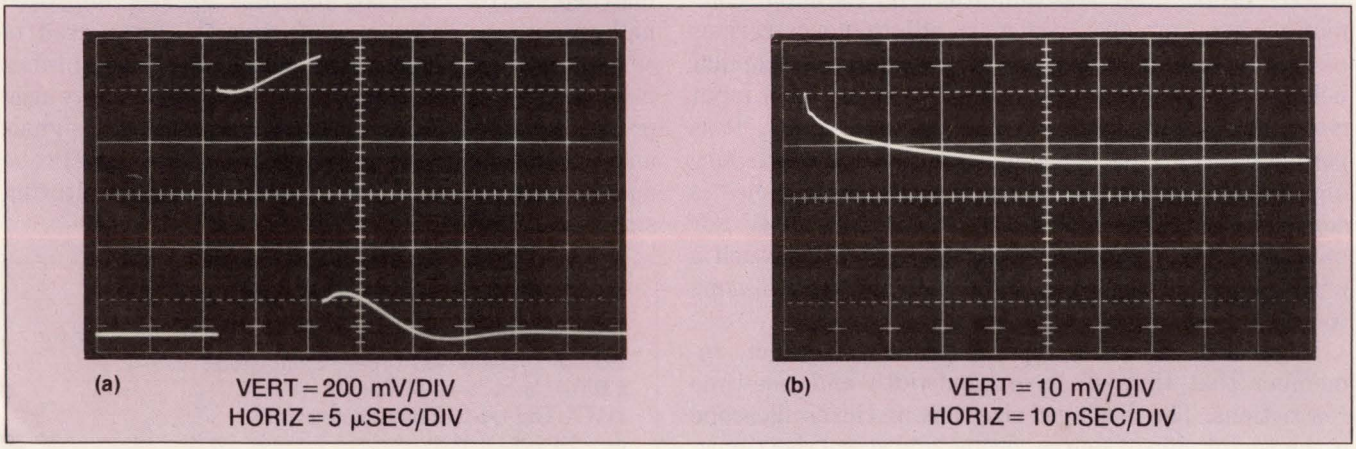


Fig 8—Section a shows the result of overdriving an FET probe's internal circuitry, *and* ***b*** *illustrates the inadvisability of attaching bargain-basement probes to a high-speed circuit.*

operating points. Under these conditions the displayed pulse top is invalid. When the circuit's output falls, the probe's overload recovery is lengthy and uneven, causing the tailing. More subtle forms of FET probe overdrive may show up as extended delays, but there is no obvious signal distortion. Avoid saturation effects arising from an FET probe's common-mode input limitations (typically ±1V) by using 10× and 100× attenuator heads when required.

A peaked, tailing response is the characteristic depicted in **Fig 8b**. The photo shows the final 40 mV of a 2.5V amplifier excursion. Instead of a sharp corner that settles cleanly, peaking occurs, followed by a lengthy tailing decay. An inexpensive "off-brand" 10× probe picked off this waveform. Such probes are often poorly designed, and constructed from materials inappropriate for high-speed work. Selecting and integrating materials for wideband probes is a specialized and difficult art. Probe designers must expend substantial design effort to get good fidelity at high speeds. Never use probes unless their manufacturer specifies them for wideband operation. Obtain probes from a vendor you trust.

When choosing your probe, also keep in mind that you cannot use all 10× probes with all oscilloscopes indiscriminately; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes, designed for 50Ω inputs, (with 500Ω to 1kΩ resistance) usually have input capacitance of 1 or 2 pF. They are a very good choice if you can stand the low resistance. FET probes maintain high-input resistance and keep capacitance at the 1-pF level, but have substantially more delay than passive probes.

FET probes also have limitations on the input common-mode range that you must adhere to or serious measurement errors will result. Contrary to popular belief, FET probes do not have extremely high input resistance—some types are as low as 100 kΩ. It is possible to construct a wideband FET probe with very high input impedance, although input capacitance is somewhat higher than standard FET probes. For measurements requiring these characteristics, such a probe is useful (see **box**, "Build your own oscilloscope tools").

Regardless of which type of probe you select, remember that they all have bandwidth and rise-time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe, and scope rise times,

$$T_{RISE}=\sqrt{(T_{RISE\ SOURCE})^2+(T_{RISE\ PROBE})^2+(T_{RISE\ OSCILLOSCOPE})^2}.$$

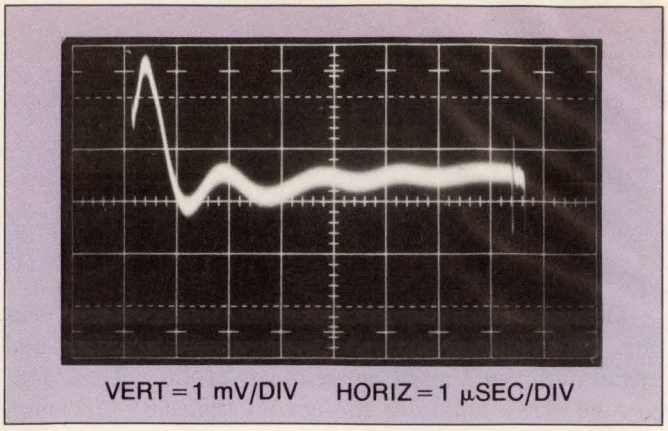


Fig 9—What appears to be a circuit's ringing *is actually the oscilloscope recovering from overdrive arising from an off-screen excursion.*

This equation warns that some rise-time degradation must occur in a cascaded system. In particular, if the probe and oscilloscope have the same rise time, the system's response will be slower than either.

Current probes are useful and convenient. The passive transformer types are fast and have less delay than the Hall-effect versions. The Hall types, however, respond at dc and low frequency, while the transformer types typically roll off somewhere below 1 kHz to 100 Hz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT that will confuse the unwary. The Tektronix CT-1 current probe, albeit not nearly as versatile as the clip-on probes, bears mention. Although the CT-1 is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at a 1-GHz bandwidth, the CT-1 produces 5-mV/mA output with only 0.6-pF loading. The decay time-constant of this ac-current probe is ~1%/50 nsec, resulting in a low-frequency limit of 35 kHz.

A very special probe is the differential probe. You may think of a differential probe as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential-input oscilloscope to the circuit board. The probes' matched, active circuitry provides greatly improved high-frequency, common-mode rejection compared to single-ended probing or even matched, passive probes used with a differential amplifier. The differential probe's resultant ability to reject common-mode signals and "ground noise" at high frequency lets this probe deliver exceptionally clean results when monitoring small, fast signals.

Acronyms used in this article

BNC—BNC coax connector. A twist-lock connector for various types of RG-type coaxial cables.
CRT—Cathode-ray tube
DAC—Digital-to-analog converter
dc—Direct current
FET—Field-effect transistor
IC—Integrated circuit

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can introduce stray capacitance to a suspected circuit node while you observe the results on the CRT. Two fingers, lightly moistened, can provide an experimental resistance path. Some engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

You can mount a miniature coaxial connector on your circuit board and mate whichever type of probe you choose to it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. If you use a current probe, a ground connection is not usually required. However, at high speeds, a ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of current probes, a long strap is usually permissible.

Even an ideal probe connection does not guarantee an accurate scope display. **Fig 9** shows the final movements of an amplifier output excursion. Setting the scope at only 1-mV per division, the objective is to view the settling residue at high resolution. Multiple time constants, nonlinear recovery, and tailing characterize this response. Note also the high-speed event just before the waveform begins its negative going-transition. What you are actually seeing is the oscilloscope recovering from excessive overdrive. You should approach any observation that requires off-screen positioning of parts of the waveform with the greatest caution. Oscilloscopes vary widely in their response to overdrive, bringing displayed results into question. Approach all oscilloscope measurements that require off-screen activity with caution. Know your instrument's capabilities and limitations. EDN

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Author's biography

For more information on this article's author, see pg 163

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

Build your own oscilloscope tools

Under most circumstances the 1- to 2-pF input capacitance and 10-MΩ resistance of FET probes is more than adequate for difficult probing situations. Occasionally, however, you may need very high input resistance along with high speed. At some sacrifice in speed and input capacitance, compared with commercial probes, you can construct such a probe.

Fig A shows schematic details. IC_1, a 350-MHz hybrid FET buffer, forms the electrical core

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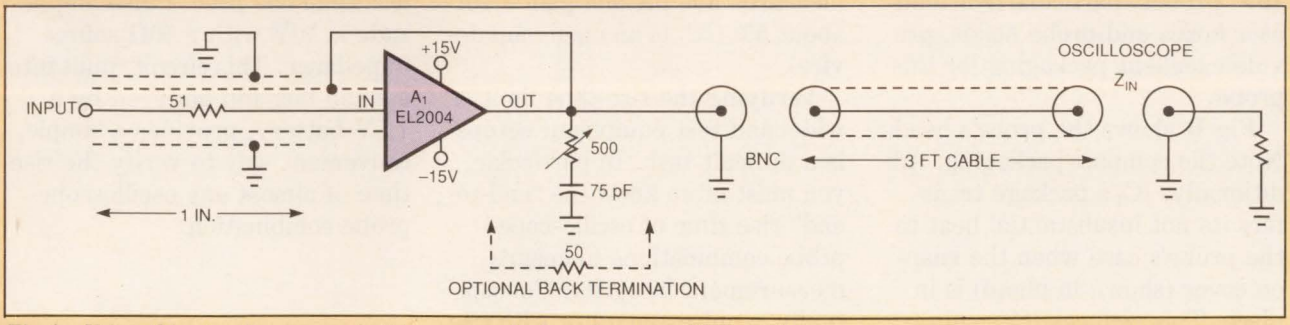

***Fig A—Using this circuit, you can** build your own high-performance FET oscilloscope probe.*

Build your own oscilloscope tools *(continued)*

of the probe. This device is a low input-capacitance, wideband-FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower's input stage when the probe sees low ac impedance. IC_1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4 pF. A ground-referred shield encircles the guard shield, reducing pickup and making high-quality ground connections to the circuit under test easy.

IC_1 drives the output BNC cable to feed the oscilloscope. Normally, back-terminating the cable at IC_1 is undesirable because the oscilloscope sees only half of IC_1's output. Although a back termination provides the best signal dynamics, the resulting attenuation is a heavy penalty. You can trim the RC damper for best edge response while still maintaining an unattenuated output.

What you can't see in the schematic is the probe's physical construction. You must built the probe very carefully to maintain low input capacitance, low bias current, and wide bandwidth. The probe's head is particularly critical. Make every effort to minimize the length of wire between IC_1's input and the probe's tip. In our lab, we have found that discarded pieces of broken 10× probes, particularly attenuator boxes and probe heads, provide excellent packaging for this probe.

Fig B shows the probe's head. Note the compact packaging. Additionally, IC_1's package transfers its not-insubstantial heat to the probe's case when the snap-on cover (shown in photo) is in place. This reduces IC_1's substrate temperature, keeping bias current down. IC_1's input connects directly to the probe's head to minimize parasitic capacitance. The power supply for IC_1, located in a separate enclosure, feeds in through separate wires. IC_1's output goes to the oscilloscope via conventional BNC hardware.

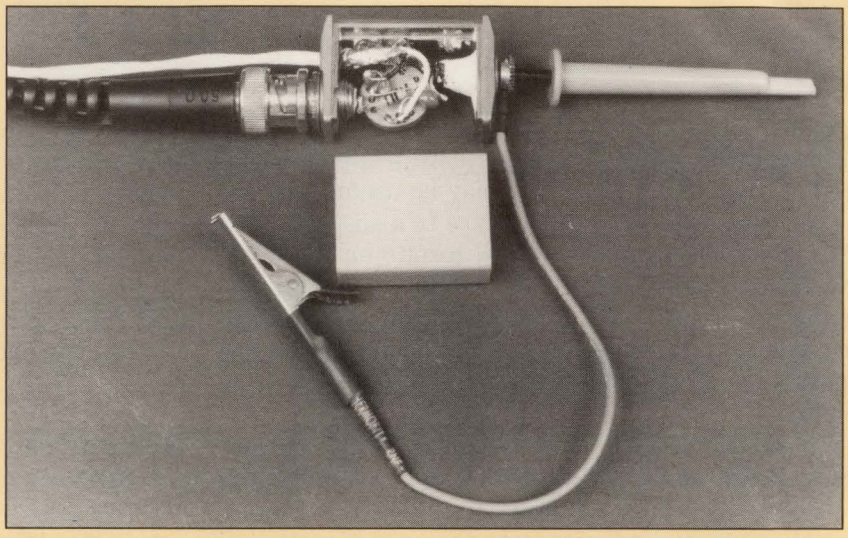

***Fig B—The components in Fig A fit** nicely into a salvaged commercial probe.*

Fig C shows the probe's output responding to an input as monitored on a 350-MHz oscilloscope (Tektronix 485). Measured specifications for Linear Technology's version of this probe include a rise time of 6 nsec, 6-nsec delay, and 350-MHz bandwidth. The delay time splits evenly between the amplifier and cable. Input capacitance is about 4 pF without the probe-hook tip and 7 pF with the hook tip. Input bias current measured 400 pA and gain error about 5% (IC_1 is an open-loop device).

Verifying the rise-time limit of wideband test equipment setups is a difficult task. In particular, you must often know the "end-to-end" rise time of oscilloscope-probe combinations to ensure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. The circuit described in **Ref 1** does this, providing a 1-nsec pulse having rise and fall times less than 350 psec. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time of almost any oscilloscope-probe combination.

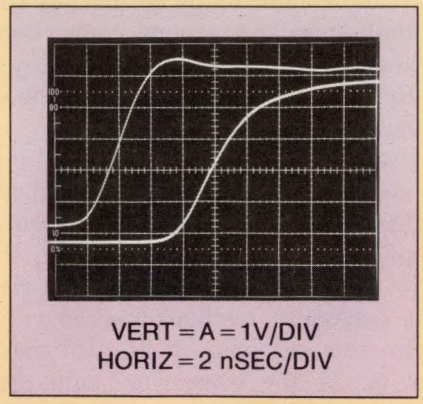

***Fig C—This scope photo shows the homemade probe's** output responding to an input.*

THE
JIM WILLIAMS
PAPERS

Correcting power-supply problems

To ensure proper operation of circuits that use high-speed op amps, you need to pay careful attention to power-supply bypassing. Of equal importance are layout techniques and the need to establish a proper ground plane.

Jim Williams, *Linear Technology Corp*

Two of the most common problems encountered in any circuit design that uses high-speed op amps are those of power-supply bypassing and pc-board layout techniques. Of these two problems, power-supply bypassing is by far the most common. Bypassing is necessary to maintain a low supply impedance. Any dc resistance or inductance in supply wires and pc-board traces can quickly raise this impedance to unacceptable levels. A high-impedance supply lets the supply voltage vary as the current levels of the devices connected to it change. Such a situation almost always causes unruly operation of the individual devices. Moreover, several devices connected to an unbypassed supply can "communicate" through the finite-supply impedances, causing erratic operating modes.

Bypass capacitors furnish a simple way to eliminate these problems by providing a local reservoir of energy at the device. A bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of the type of capacitor to use for bypassing is a critical issue. **Fig 1** shows the output of an unbypassed amplifier driving a 100Ω load. The power supply the amplifier sees at its terminals has a high impedance at high frequencies. This impedance forms a voltage divider with the amplifier and its load, letting the supply move as internal conditions in the amplifier change. As shown, this action causes local feedback, and oscillation occurs. Therefore, always use bypass capacitors at appropriate supply-rail points.

In **Fig 2** the 100Ω load is removed, and the amplifier

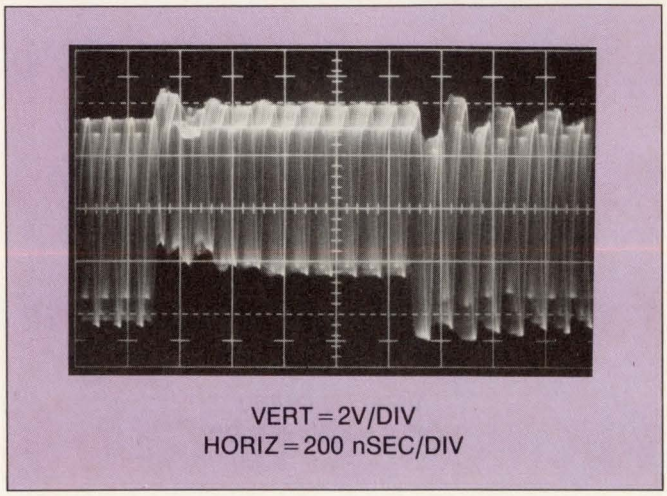

Fig 1—The output of an amplifier *drives a 100Ω load without bypass capacitors.*

displays a pulse output. The unbypassed amplifier responds surprisingly well, but overshoot and ringing dominate. Always use bypass capacitors to avoid overshoot and ringing. In **Fig 3**, the settling is noticeably better, but some ringing remains. This response is typical of lossy bypass capacitors, or good ones placed too far away from the amplifier. Use good quality, low-loss bypass capacitors, and place them as close to the amplifier as possible.

The multiple-time-constant ringing in **Fig 4** often indicates a poor grade of paralleled bypass capacitors or excessive trace length between the capacitors. Although paralleling capacitors of different characteristics is a good way to get wideband bypassing, you need to consider such action carefully. Resonant interaction between the capacitors can also cause such a waveform after a step input. This type of response is often aggravated by heavy amplifier loading. When paralleling bypass capacitors, plan the layout and breadboard with the units you plan to use in production.

Fig 5 addresses a more subtle bypassing problem. The trace shows the last 40-mV excursion of a 5V step almost settling cleanly in 300 nsec. The slight overshoot is due to a loaded (500Ω) amplifier without quite enough bypassing. Increasing the total supply bypassing from 0.1 to 1 μF cured this problem. Use large-value paralleled bypass capacitors when you need very fast settling, particularly if the amplifier is heavily loaded, or sees fast load steps.

The problem of peaking on the leading and trailing corners (**Fig 6**) is typical of poor layout practice. Depicted here, a unity-gain inverter suffers from excessive trace area at the summing point. Only 2 pF of stray capacitance caused the peaking and ringing. Minimize trace area and stray capacitance at critical nodes. Consider layout as an integral part of the circuit, and plan it accordingly.

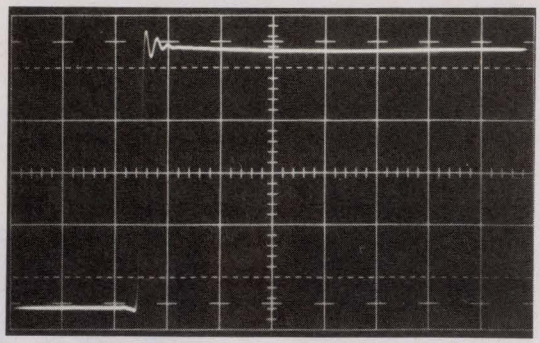

Fig 3—A poor-quality bypass capacitor *allows some ringing in the amplifier's output.*

About bypass capacitors

Bypass capacitors are used to maintain low power-supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power-supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing

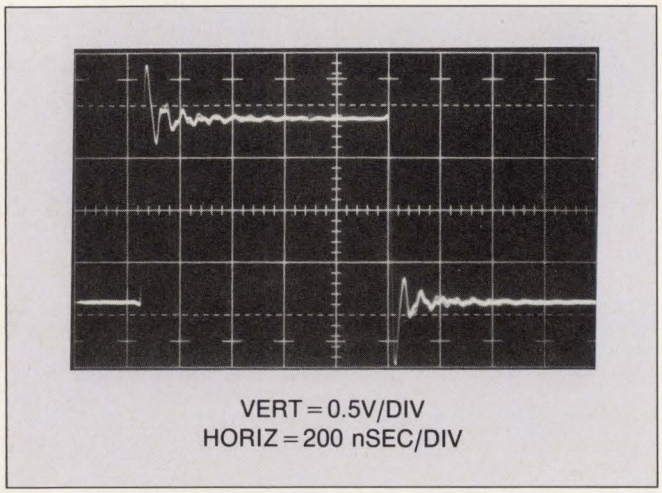

Fig 2—An unbypassed amplifier with no load *can be surprisingly stable—temporarily.*

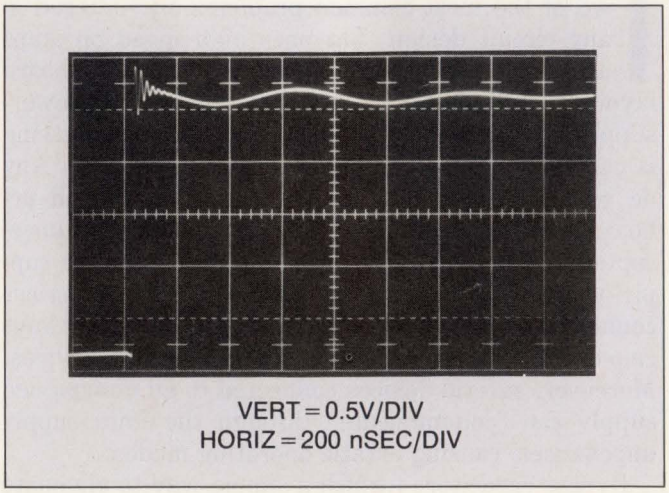

Fig 4—Paralleled bypass capacitors *form a resonant network, which produces ringing.*

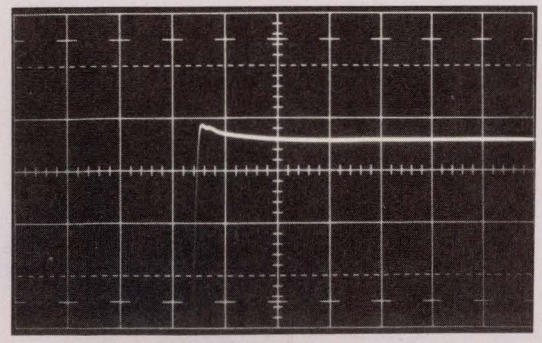

Fig 5—This waveform shows a more subtle bypassing problem. *Not-quite-good-enough bypassing causes a few millivolts of peaking.*

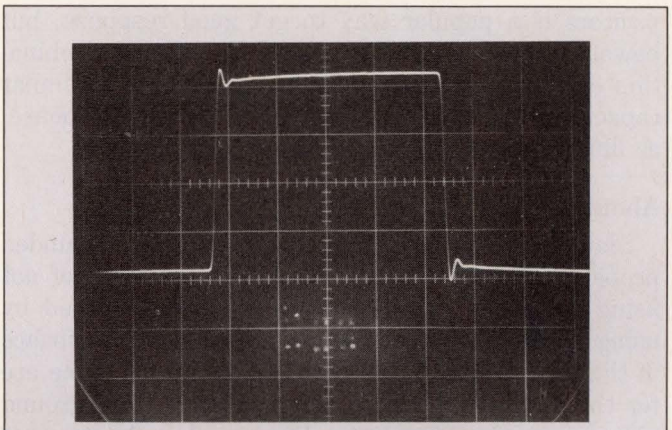

Fig 6—This waveform is a typical result of poor layout. *Only 2 pF of capacitance at the summing point introduces peaking on the leading and trailing corners.*

is still necessary because no power supply or regulator has zero output impedance at 100 MHz. You determine the type of capacitor to use by its application, the frequency domain of the circuit, cost factors, board space, and many other considerations. It is possible, however, to make some useful generalizations.

All capacitors contain parasitic terms (some examples of which appear in **Fig 7**). In bypass applications, leakage and dielectric absorption are second-order terms, but series resistance (R) and inductance (L) are not. These latter terms limit the capacitor's ability to damp transients and maintain low power-supply impedance. Bypass capacitors must often be large in value to absorb long transients, necessitating electrolytic types that have large values of series R and L.

Different types of electrolytics and combinations of electrolytic and nonpolarized capacitors have markedly different characteristics. Which type (or types) to use is a matter of passionate debate in some circles. The test circuit of **Fig 8** and accompanying photos are useful in evaluating the choices. The photos show the response of five bypassing methods to the transient generated by the test circuit. **Fig 9a** shows an unbypassed line that sags and ripples badly at large amplitudes. **Fig 9b** uses a 10-μF aluminum electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A 10-μF tantalum unit (**Fig 9c**) offers cleaner response, and the 10-μF aluminum electrolytic combined with a 0.01-μF ceramic type (**Fig 9d**) is even better. Combining electrolytics with nonpolarized ca-

Acronyms used in this article

air wire—A connection from lead-to-lead without going to a specific terminal or point.
BNC—BNC coax connector. A twist-lock connector for various types of RG-type coaxial cables.
DAC—Digital-to-analog converter
IC—Integrated circuit
pc board—Printed-circuit board
pc card—Printed-circuit card

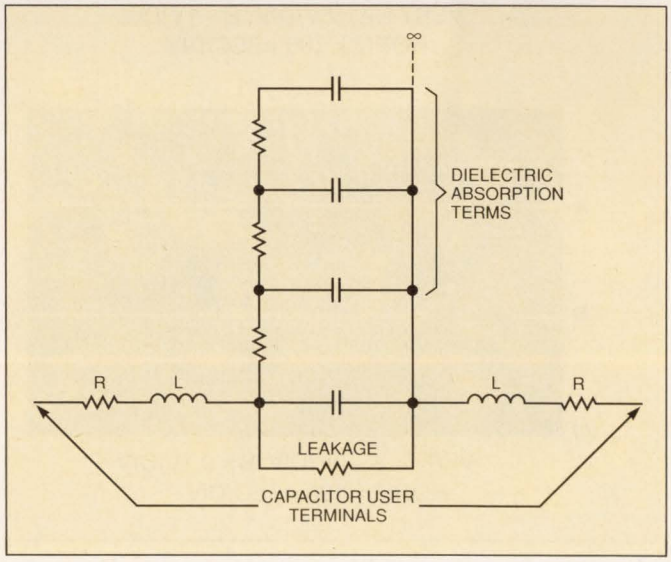

Fig 7—All capacitors have parasitics. *In bypass applications, the series resistance (R) and inductance (L) limit the capacitor's ability to maintain a low supply impedance.*

pacitors is a popular way to get good response, but beware of picking the wrong pair. The wrong combination of supply-line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as illustrated in **Fig 10**.

About ground planes

Similar to that resulting from a poorly grounded probe, the **Fig 11** waveform shows the result of not using a ground plane. A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (ac currents travel along the surface of a conductor) and covers the entire area of the board, a ground plane provides a way to access a low-inductance ground from

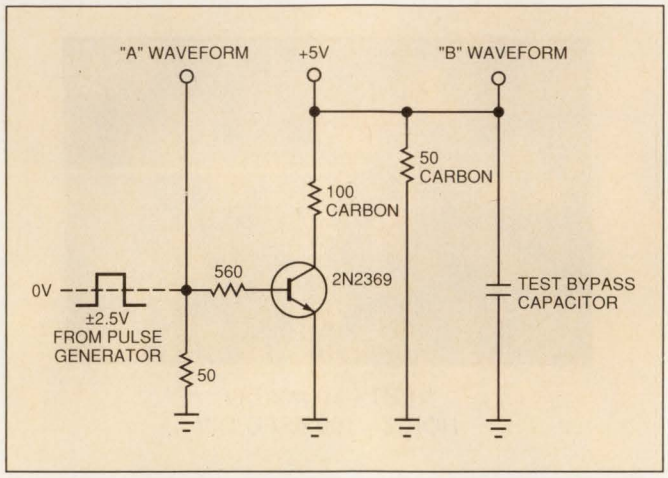

Fig 8—This test circuit, *together with various types of bypass capacitors, produced the waveforms shown in* ***Figs 9a*** *through* ***d****.*

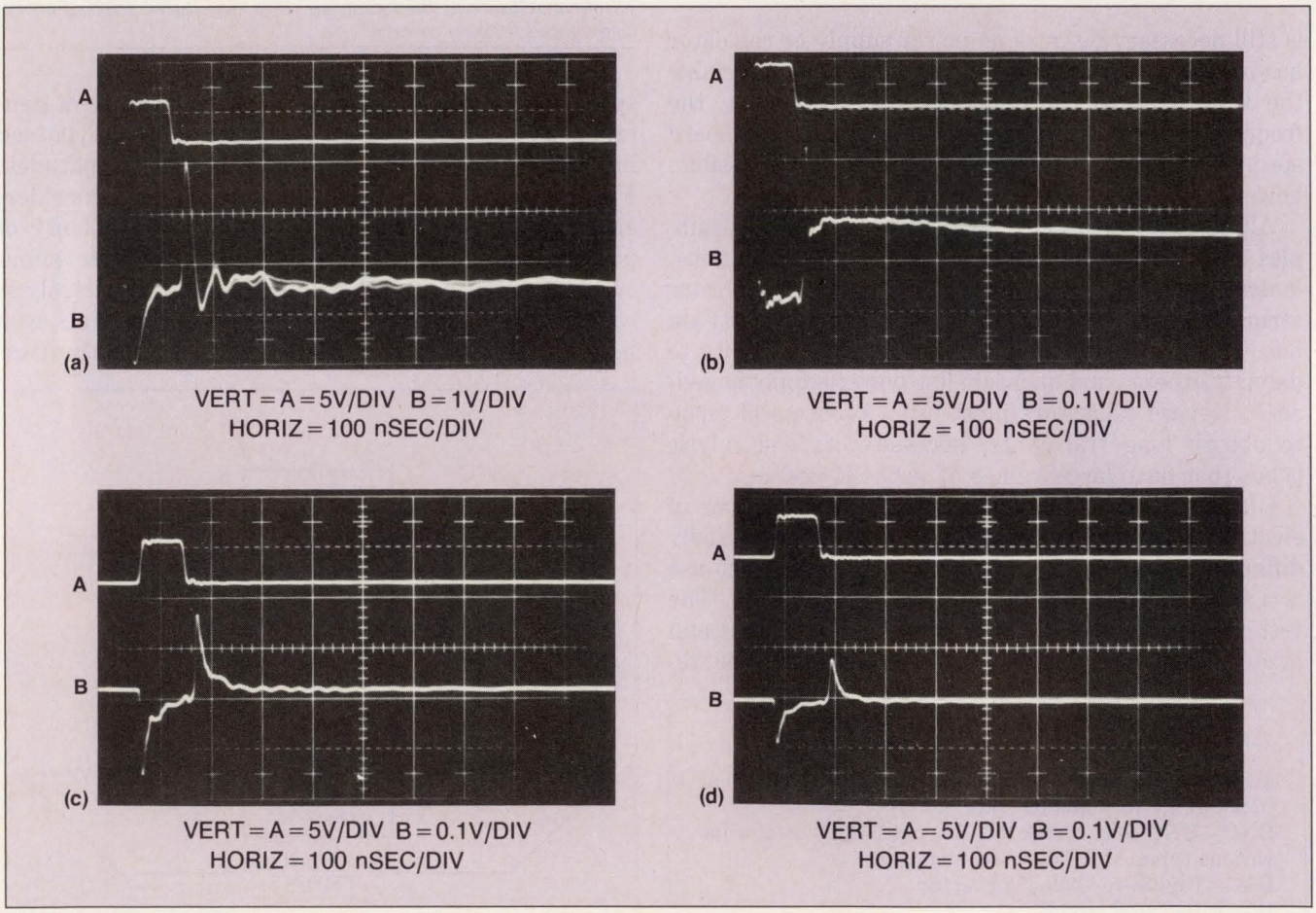

Fig 9—The response of this unbypassed line (a) *sags and has a high ripple content. A 10-μF aluminum-electrolytic capacitor (***b****) somewhat reduces that disturbance. A 10-μF tantalum capacitor (***c****) offers cleaner response than that shown in* **b**. *Combining different capacitor types provides further improvement. A 10-μF aluminum capacitor and a 0.01-μF ceramic type (***d****) substantially smooth out the disturbance.*

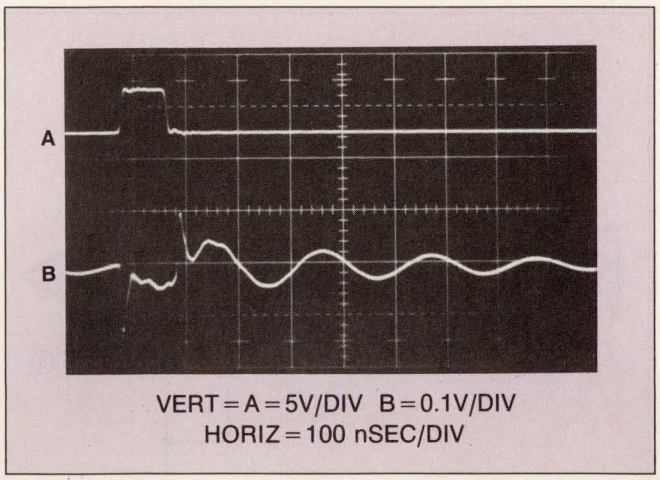

Fig 10—Some paralleled combinations can cause ringing. *Always try various types before specifying.*

anywhere on the board. A ground plane also minimizes the effects of stray capacitance in the circuit by referring them to ground. This reference breaks up potential unintended and harmful feedback paths. Always use a ground plane with high-speed circuitry.

Although the term ground plane is often used as a mystical and ill-defined cure for spurious circuit operation, there is actually little mystery to the usefulness and operation of a ground plane. Like many phenomena, the operational principle of a ground plane is surprisingly simple.

As previously mentioned, ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a current-carrying wire (**Fig 12a**) surrounded by radii of a magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the current flowing through the wire. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This computation implies integrating on the radius from $R = R_W$ to infinity—a very large number. However, consider the case that **Fig 12b** illustrates, where two wires in space carry the same current in either direction. The fields produced cancel.

When the fields cancel, the inductance is much smaller than in the single-wire case and can be made arbitrarily small by reducing the distance between the two wires. This reduction of inductance between current-carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source, through its conductor and back to ground, includes a large loop area. This path produces a large inductance for the conductor and can cause ringing because of LRC effects. It is worth noting that, at 100 MHz, a 10-nH inductor has an impedance of 6Ω. At 10 mA, a 60-mV drop results.

A ground plane provides a return path directly under

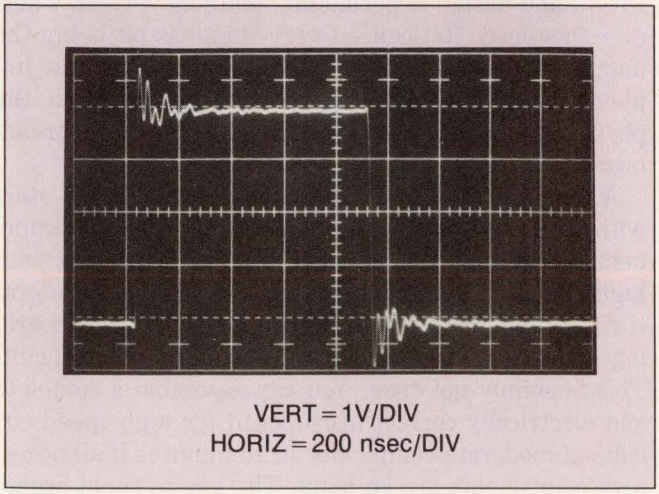

Fig 11—Instabilities caused by the lack of a ground plane *can produce a result similar to that of a poorly grounded test probe.*

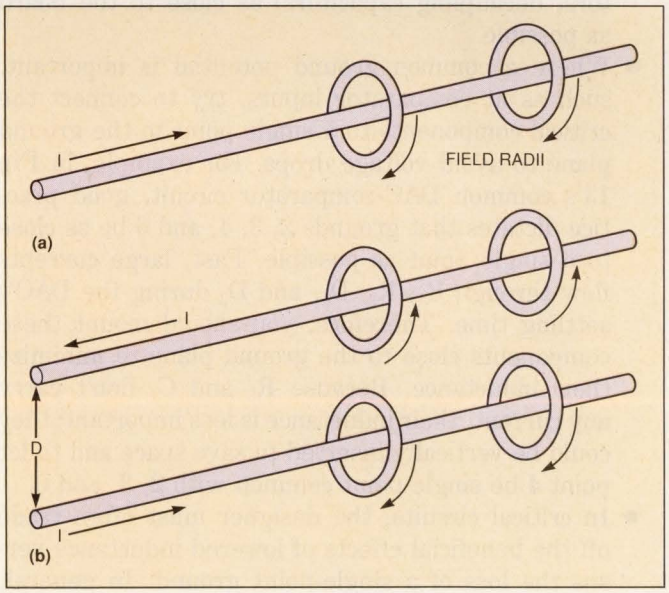

Fig 12—A current-carrying wire *produces a magnetic field (***a***). Two wires in space, carrying the same current in opposite directions, produce a cancellation of the magnetic field (***b***).*

the signal-carrying conductor through which the return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Current will always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to "ground plane" one whole side of the pc card (usually the component side for wave-solder considerations) and run the signal conductors on the other side. This procedure will provide a low-inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to ac skin effects (ac currents travel along a conductor's surface). Moreover, ground planes aid the circuit's high-frequency stability by referring stray capacitances to ground.

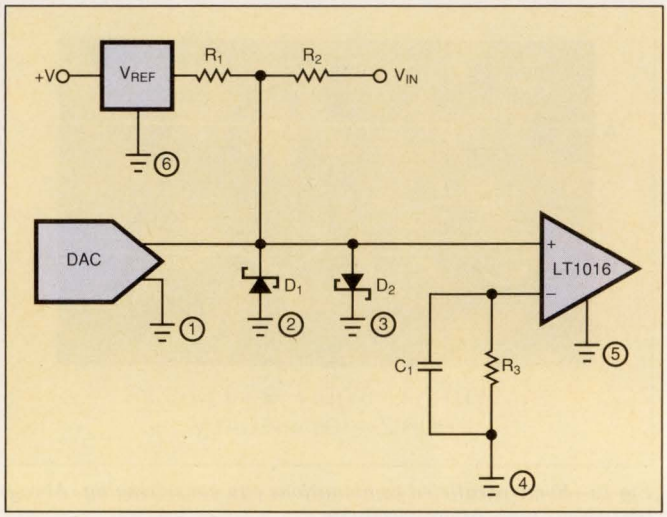

***Fig 13—In this combination analog-digital circuit**, good practice dictates that grounds 2, 3, 4, and 6 be as close to a single point as possible.*

Practical hints for ground planes

The following guidelines are useful in the establishment and use of a ground plane.

- Ground-plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
- Mount components that conduct substantial fast-rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
- Where a common ground potential is important, such as at comparator inputs, try to connect the critical components to a single point in the ground plane to avoid voltage drops. For example, in **Fig 13**'s common DAC-comparator circuit, good practice dictates that grounds 2, 3, 4, and 6 be as close to a single point as possible. Fast, large currents flow through R_1, R_2, D_1, and D_2 during the DAC's settling time. Therefore, you should mount these components close to the ground plane to minimize their inductance. Because R_3 and C_1 don't carry any current, their inductance is less important; they could be vertically inserted to save space and to let point 4 be single-point common with 2, 3, and 6.
- In critical circuits, the designer must often trade off the beneficial effects of lowered inductance versus the loss of a single-point ground. In general, however, keep trace lengths short. Inductance varies directly with length, and no ground plane will achieve perfect cancellation.

Putting the guidelines for capacitor choices and the establishment of a proper ground plane to practical use usually starts with a breadboard. The breadboard is both the designer's playground and proving ground. It is there that reality resides, and where paper (or computer) designs meet their master. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant, explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess both carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that don't work. Implementing the above approaches begins with the physical construction methods used to build the breadboard.

A breadboard for a high-speed circuit must start with a ground plane. In addition, bypassing, component layout, and connections should be consistent with high-speed operations. Because of these considerations, there is a common misconception that breadboarding high-speed circuits is time consuming and difficult. This is simply not true. You can assemble a complete and electrically correct breadboard for high-speed circuits of moderate complexity in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them.

This procedure permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Use all degrees of freedom in making connections and mounting components. Don't be bashful about bending IC pins to suit desired low-capacitance connections, or air-wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components. It's true that printed-circuit construction is eventually required, but when initially breadboarding forget about pc boards and production constraints. Later, when the circuit works and is well understood, you can take care of pc-board adaptations.

The **Fig 14** amplifier circuit is a good working example of breadboarding techniques. This circuit is a high-impedance, wideband amplifier that has low-input capacitance. Q_1 and IC_1 form the high-frequency path, with the 900 to 100Ω feedback divider setting the gain. IC_2 and Q_2 close a dc stabilization loop, minimizing the dc offset between the circuit's input and output. Critical nodes in this circuit include Q_1's gate (because of the desired low-input capacitance) and IC_1's input-related connections (because of their high-speed operation). Note that the connections associated with IC_2 handle only dc, and are much less sensitive to layout. These determinations dominate the breadboard's construction.

Fig 15a shows the initial breadboard construction. The copper-clad board is equipped with banana-type connectors. The connector's mounting nuts are simply soldered to the board, securing the connectors. After adding IC_1 and the bypass capacitors (**Fig 15b**), observe that IC_1's leads have been bent out. Bending the leads permits the amplifier to sit down on the ground plane, minimizing parasitic capacitance. Also, the bypass capacitors are soldered to the amplifier power pins right at the capacitor's body. The capacitor's leads are returned to the banana power jacks. This connection method provides good amplifier bypassing, while mechanically supporting the amplifier. It also eliminates separate wire runs to the power pins.

Fig 15c shows the addition of discrete components in the high-speed path. Q_1's gate is connected directly to the BNC input socket, as is the 10-MΩ resistor associated with IC_2's negative input. Note that the end of this resistor that sees a high frequency is cut very short, while the other end is left uncut. The 900 to 100Ω divider is installed at IC_1, with very short connections to IC_1's negative input. IC_1's 10-MΩ resistor receives similar treatment to that of the BNC-connected 10-MΩ resistor; the high-frequency end is cut short, while the end destined for connection to IC_2 remains uncut. Q_2's collector and Q_1's source, both high-speed points, are tied closely together with IC_1's positive input.

Finally, dc amplifier IC_2 and its associated components are air-wired into the breadboard (**Fig 15d**). Their dc operation permits this, while the construction technique makes connections to the previously wired nodes easy. You can bend the previously uncommitted ends of the 10-MΩ resistors in any way necessary to make connections. All other components associated with IC_2 receive similar treatment, and the circuit is ready for experimentation.

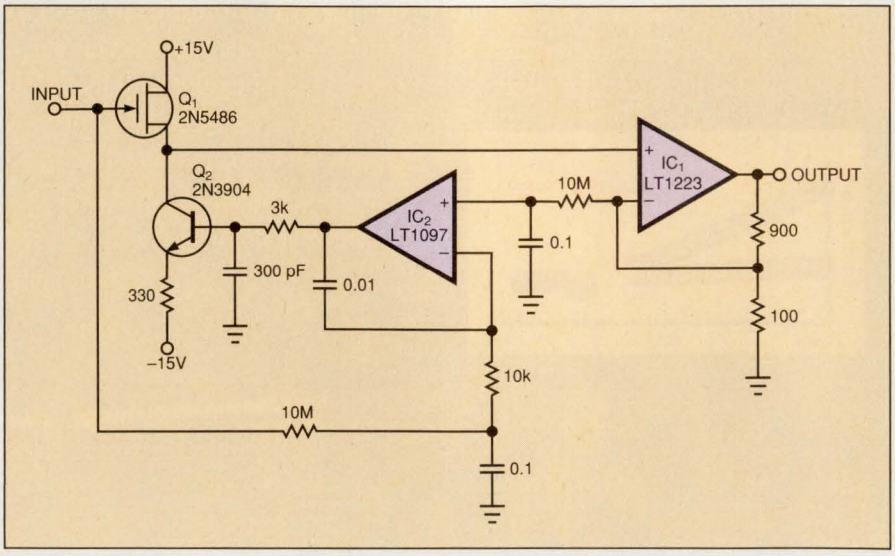

***Fig 14—This stabilized FET-input amplifier** is an example of the breadboarding techniques shown in **Fig 15a** through **d**.*

Despite the breadboard's seemingly haphazard construction, the circuit works well. Input capacitance measures a few pF (including the BNC connector), and bias current is about 100 pA. Slew rate is 1000 V/μsec, and the bandwidth approaches 100 MHz. Even with 50-mA loading, the output is clean, with no sign of oscillation or other instabilities.

Once the breadboard seems to work, it's useful to begin thinking about the pc-board layout and component choices for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms, such as resistors, capacitors, and physical layout changes, to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

Finally, design the breadboard to be quick and easy to build, work with, and modify. Observe the circuit, and listen to what it is telling you before trying to get it the desired state. Don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result—whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial. EDN

Author's biography

For more information on this article's author, see pg 163 .

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

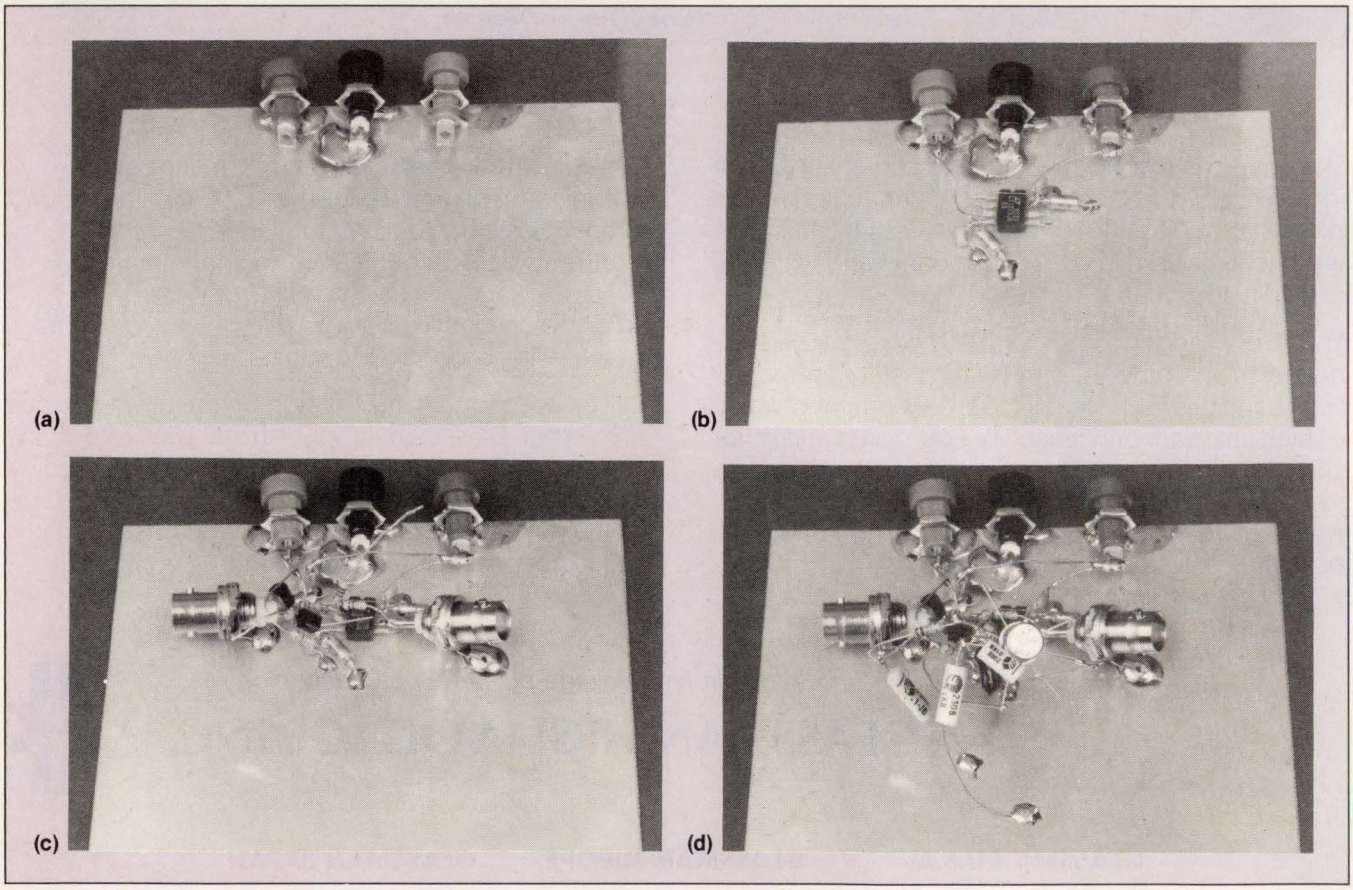

Fig 15—In the initial breadboard construction (a), *banana jacks are soldered to a copper-clad board. With the addition of a high-speed amplifier, IC_1 (***b***), bypass capacitors provide support while the bent amplifier pins ease connections and minimize the distance to the ground plane. High-speed discrete components and BNC connectors are added to* **c**. *Note the short connections at the amplifier input pins (left side of package). The uncommitted ends of the 10-MΩ resistors are just visible. Finally, you wire the dc servo amplifier to complete the connections to the 10-MΩ resistors (***d***). This part of the circuit is not layout sensitive.*