



MICREL
SEMICONDUCTOR



**Data
Book
1991**

A CORPORATE COMMITMENT TO EXCELLENCE IN SUPPLYING INTELLIGENT POWER SEMICONDUCTORS:

Micrel Semiconductor was founded in 1978 in the heart of "Silicon Valley". We are a profitable, self-funded, full service semiconductor company. Dedication to full service is expressed in our advanced capabilities such as a comprehensive CAD/CAE support team, an extensive macro library, and our own state-of-the-art wafer fabrication and test facilities. All growth, product development, and acquisitions have been funded through retained earnings.

Micrel's objective is to be a major supplier of smart power products which incorporate our ASIS™ (Application Specific Integrated Subsystem) philosophy to integrate as much in silicon as conceivably possible. Thus Micrel has developed a process technology which combines bipolar, CMOS Si-gate, and DMOS technologies. The bipolar component allows us to build precision analog functions. CMOS allows us to incorporate fast, low power, dense, digital logic. DMOS provides high voltage power MOSFETs. This uniquely flexible, high voltage compatible process enabled our success in several custom smart power designs and led to the development of the industry's first semicustom smart power array, the Micrel MPD8020, which founded the semicustom intelligent power niche. Building upon these accomplishments, Micrel introduced a line of proprietary and second-sourced standard products which address the intelligent power marketplace.

"Intelligent Power" is the combining of low voltage linear and digital functions with high voltage, high current output devices. This allows for the further integration of functions heretofore handled primarily by modules and hybrids. By combining these low voltage and high voltage functions monolithically we have dramatically improved reliability and packaging density. Micrel is dedicated to support this new and exciting Intelligent Power semiconductor market. Whether your application is automotive, industrial controls, telecommunications, medical equipment, office automation, avionics, or military, Micrel has the solution. We extensively test our products to insure they meet the highest standards of quality and reliability.

Micrel is proud of its success and has established a standard of business performance envied by others in the industry. We are dedicated to service and you have my personal commitment that Micrel will meet or exceed your strictest standard of excellence.



Ray Zinn
President and Chief Executive Officer
Micrel, Inc.

Some products in this book are protected by one or more of the following patents: 4,764,589; 4,914,546; 4,951,101; 4,979,001.

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General Information

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Introduction

Micrel History

Micrel Semiconductor has a distinguished history in the fields of testing, manufacturing and development of digital and analog high voltage interface integrated circuits in gate array, semicustom, and standard cell technologies.

Test Service Beginning

Micrel was founded in 1978 as an independent high performance testing facility for manufacturers and consumers of digital and analog ICs. The company grew quickly and added LSI test systems, wafer probers, and autohandling equipment for high and low temperature production testing.

Micrel established a reputation for excellent customer service, high quality, and fast turn-around responsiveness. Design, fabrication, and test services were integrated into many programs serving IC manufacturers, IC users, and hybrid manufacturers. Micrel's services became a recognized quality resource for many industrial, commercial, and military customers.

Micrel's IC Test Division remains the leading independent facility for customers who need to supplement in-house capability with high-accuracy wafer characterization and functional final testing. The operation features six major VLSI automatic test systems as well as wafer probe stations, automatic device handlers, and support equipment. The operation offers environmental and stress facilities to meet most commercial and Mil-Std test conditions required for ICs.

Foundry Added

Micrel launched a program of reinvestment and diversification that first led to custom wafer fabrication for other merchant/makers, and eventually progressed to developing the Micrel line of semicustom and standard product Smart Power ICs.

In 1981, Micrel acquired its own IC fabrication facility in Sunnyvale, CA. Micrel's Wafer Fab Division provides IC manufacturers with a silicon foundry which addresses their unique processing requirements for volume production or short runs. The facility also makes it possible for independent design groups to produce sophisticated high quality ICs.

Micrel has subsequently extended the foundry capability to produce a full complement of CMOS/DMOS/Bipolar/NMOS/PMOS processes with both metal gate and silicon gate, dual metal and dual Poly feature size down to 2 microns, with operating voltage from 1.5V up to 250V.

Second Sourcing and Radiation Hardened ICs

In 1983, the Company again expanded its base by becoming a qualified second source supplier of discontinued or follow-on program ICs. Micrel signed agreements with several manufacturers to produce their products to original specifications, using — in most cases — the original tooling and special equipment. Micrel manufactures a number of second-sourced ICs to Military class B requirements for use in programs such as Hellfire, Standard Missile I, F-16, and SINGARS.

In 1987, Micrel signed an agreement with National Semiconductor to take over the manufacture of the CD4000 and MM54CXXX families of radiation hardened (Radhard) ICs used in a number of critical military programs such as MilStar. More recently, Micrel purchased tooling and inventories of the CDI three micron line. The products include CMOS silicon gate and metal gate parts. Micrel now supplies these products to former CDI customers.

Innovative Smart Power Arrays

In 1987, Micrel announced the first semicustom linear/digital/power array for high voltage (HV) power applications, the MPD8020. The Smart Power Array does for power circuit designers what gate and linear array ASICs do for low voltage digital and linear designers. The IC provides a semicustom array that can quickly and economically be applied to critical power design challenges.

On one monolithic IC, Micrel combines CMOS analog circuits, TTL/CMOS compatible high speed CMOS logic, and high voltage DMOS power drivers. MPD8020 wafers are held at the last step before metallization. After the customer specifies the interconnect pattern, Micrel turns each IC into a proprietary Smart Power ASIC.

The MPD8020 ASIS™ (Application Specific Integrated System) provides high level system integration and intelligence with smaller size and lower cost. Aspects of value, performance, reliability, and power handling capability are increased greatly through Micrel's proprietary BCD (Bipolar, CMOS, DMOS) technology combination.

Standard Interface Products

Micrel produces a line of standard IC's designed to interface between the microprocessor and the load:

- MIC5010/11/12/13 High side power MOSFET predriver
- MIC426/1426/4420/4423/4465 Low side power MOSFET drivers
- MIC8030 Dichroic LCD driver, 100V/38 segments
- MIC4807 Latched driver, 8 outputs, 100V/200mA each
- MIC8010 LCD driver, 30V/38 segments
- MIC50395 LED driver, 6 decade, up/down counter
- MM5451 LED driver, 35 segments
- CD4000 Series Radhard CMOS logic family

Serving Today's Customers

Micrel is positioned to become the leader in Smart Power technology. In 1989 the Company opened a regional design center in Japan, and in 1990, opened other regional design centers throughout the United States and Western Europe. Micrel will continue to announce new standard Smart Power products and the development of other standard and semicustom arrays. These products will address key growth areas of Smart N-Channel Power MOSFET drive and Smart Control of high voltage components including motors, relays, displays, printers, and power supplies.

Micrel's customers include major military subcontractors who impose SCD criteria for standard 883C Class S or B requirements or special screening. Other customers include manufacturers of high volume commercial products from garage door openers and telecom devices to medical pill boxes. Micrel welcomes customer visits to discuss design, production and testing issues.



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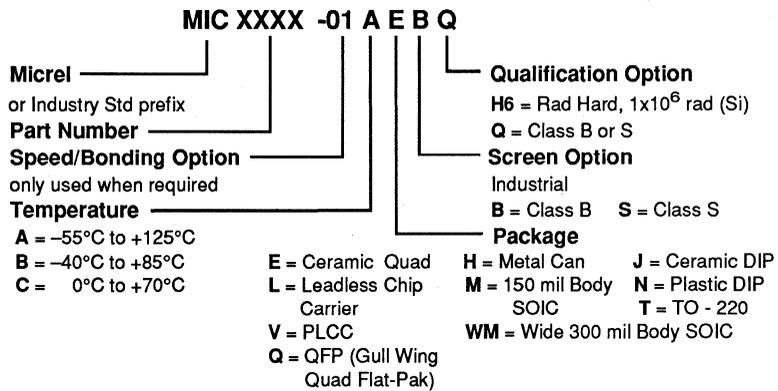
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Ordering Information

Ordering Information:





Industry Cross Reference Guide

Micrel **Direct Replacement** devices are shown in boldface.

Micrel *Similar Replacement* devices (some circuit modifications may be required) are shown in italics.

Manufacturer	Micrel Replacement	Manufacturer	Micrel Replacement
Gould AMI S4520	MIC8010 <i>MIC8030, MIC8031</i>	SGS M5450 M5451 SGS1626/2626/3626	MM5450 MM5451 MIC426, MIC1426, MIC4423, MIC4426
Holt HI-8010	MIC8010 <i>MIC8030, MIC8031</i>	Silicon General SG1626/2626/3626 SG1644/2644/3644	MIC426, MIC1426, MIC4423, MIC4426 MIC426, MIC1426, MIC4423, MIC4426
Intersil ICL7667 ICM7233	MIC426, MIC1426, MIC4423, MIC4426 MIC7233	Siliconix SG1626/2626/3626	MIC426, MIC1426, MIC4423, MIC4426 MIC426, MIC1426, MIC4423, MIC4426
IXYS IXLD426 IXLD427 IXLD428 IXLD1426 IXLD1427 IXLD1428 IXLD4420 IXLD4423 IXLD4424 IXLD4425 IXLD4426 IXLD4427 IXLD4428 IXLD4429	MIC426 MIC427 MIC428 MIC1426 MIC1427 MIC1428 MIC4420 MIC4423 MIC4424 MIC4425 MIC4426 MIC4427 MIC4428 MIC4429	Sprague UCN-4807 UCN-5800A UCN-5801A UCN-5821A UCN-5822A UCN-5823A UCN-5841A UCN-5842A UCN-5843A	MIC4807 MIC5800 MIC5801, 58P01, MIC59P50 MIC5821 MIC5822 MIC5823 MIC5841, 58P42, MIC59P60 MIC5842, 58P42, MIC59P60 MIC5843
Lansdale ML4350	MIC4350	Teledyne TSC426 TSC427 TSC428 TSC1426 TSC1427 TSC1428 TSC4420 TSC4423 TSC4424 TSC4425 TSC4426 TSC4427 TSC4428 TSC4429 TSC4465 TSC4466 TSC4467 TSC4468 TSC4469	MIC426 MIC427 MIC428 MIC1426 MIC1427 MIC1428 MIC4420 MIC4423 MIC4424 MIC4425 MIC4426 MIC4427 MIC4428 MIC4429 MIC4465 MIC4466 MIC4467 MIC4468 MIC4469
Maxim ICL7667 ICM7233 TSC426	MIC426, MIC1426, MIC4423, MIC4426 MIC7233 MIC426, MIC1426, MIC4423, MIC4426	Toshiba TC5002B	MIC5002
Motorola MC4350 MH0026	MIC4350 MIC426, MIC1426, MIC4423, MIC4426		
National Semiconductor DS0026 LP2950 LP2951 MM5450 MM5451 NHM0026	MIC426, MIC1426, MIC4423, MIC4426 LP2950, MIC2950 LP2951, MIC2951 MM5450 MM5451 MIC426, MIC1426, MIC4423, MIC4426		

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Quality/Reliability Program

Our Philosophy

Product quality and reliability are two of the most critical elements for achieving success in today's semiconductor industry. Micrel has attained success as a semiconductor supplier by designing and processing parts that meet the most strenuous applications and most adverse environments. Micrel has accomplished this by never wavering from the philosophy that quality must be built into each and every device and process.

Micrel considers product reliability to be an expression of the quality philosophy extended over the expected life of each product. Micrel's philosophy begins in the design stage and continues, under strict monitoring and control, throughout the development, production, testing and packaging of each product.

Micrel's specific goal is to produce devices that are without defect from their given specifications for performance and product life. Product testing and comparative studies are ongoing activities at Micrel as we continue our search for new and more effective methods for manufacturing products with built-in quality. The Micrel quality program is in full compliance with MIL-I-45208, and equipment calibration meets all requirements of MIL-STD-45662.

Quality Program Elements

Quality and reliability in Micrel products are obtained through a number of quality assurance program elements, most of which contain multiple levels of requirements and procedures. These program elements comprise the Micrel Quality Assurance Program.

I. Supplier requirements

Vendor certification of compliance to published specifications is required for process materials, gasses, substrates, masks, etc., as well as for components, parts and materials used in assembly.

II. Fabrication QA is based on a Statistical Process Control (SPC) Program including:

1. Test procedures
2. Document control
 - Specifications/recipes
 - Process change notice (PCN)
 - Engineering change notice (ECN)

3. Critical process-step monitoring
 - Particulates
 - Critical dimensions
 - Electrical performance
4. Extended SPC programs
 - Process Limit Control (PLC)
 - Process on Exception (POE)
5. Outgoing QA
 - Visual Inspection
 - To Micrel Standards
 - To Mil-883 Class B or Class S

III. Vendor Requirements

Certification of compliance to published Micrel or customer specifications is required for processes, materials, and services from third-party vendors.

IV. Assembly QA Program

1. Test procedures
2. Document control
 - Specifications
 - Control systems
 - Engineering change notices (ECN)
3. Critical-step monitoring
 - Assembly processes
 - Critical dimensions
 - Environmental processes
4. Acceptance Test Procedure
 - Electrical performance
 - Component marking
5. Outgoing QA
 - Visual Inspection
 - To Micrel Standards
 - To Mil-883 Class B or Class S

Organization

At Micrel, quality assurance management reports directly to the President of the corporation. All quality and reliability issues are independent of the production organizations.

The QA Manager's responsibilities are to establish and maintain effective controls for monitoring Micrel manufacturing and test services, equipment and processes (as well as our suppliers and contractors), to report the findings to the President, and to initiate statistically valid techniques to further improve Micrel quality and reliability levels.

The QA Manager is responsible for implementation and administration of multiple quality-related programs and systems for both commercial and military grade processes and products. Activities under the QA Manager's control include: incoming inspection, in-process quality control, qualification testing, conformance testing, document control, specification review, failure analysis, internal audit, quality procedures training, and ongoing vendor qualification and performance appraisal.

Statistical Process Control

Foremost of the Micrel quality assurance programs is their Statistical Process Control (SPC) methodology. Because of the company's unique mix of proprietary, custom and foundry products, SPC at Micrel is approached on two levels.

- Level 1 Traditional SPC utilizing process capability studies, design of experiments, Pareto analysis, histograms and X-bar R charting of critical process steps.
- Level 2 Extended SPC methodology adds Process Limit Control (PLC) and Process on Exception (POE) programs as super-sets to the standard SPC programs.

Micrel's Process Limit Control (PLC) program provides absolute control of wafer runs during processing. Parameters are measured and recorded at every process steps against established limits. When any measurement value is found to exceed a specification limit, the run is immediately stopped and process engineering is notified. Before the run can proceed, engineering must evaluate the data and determine the run disposition during that production shift.

The Process on Exception (POE) program monitors and controls wafers during electrical testing. Wafer probe results are compared against specifications. Any exceptions to either absolute, preferred, or target specifications are noted and detailed reports are generated. Engineering may then exercise some influence over yield issues by determining which electrical performance criteria are critical.

The results of SPC, PLC and POE performance monitoring are reviewed on a monthly basis. Trends are charted, corrective actions are evaluated and process improvements are implemented as a result of the data.

Document Control

Document control is an integral part of the Micrel quality assurance program. It is designed to assure that operating procedures and customer requirements are translated into regulatory written instructions. Document control is responsible for initiating, approving, distributing, revising, recalling, and archiving internal control systems in the form of product run sheets (recipes), process and test specifications, etc.

Micrel's two main specification control methodologies utilize engineering change notice (ECN) and process change notice (PCN) systems.

- ECN The engineering change notice system follows standard industry procedures for process and test specifications, travelers, forms, and drawings.
- PCN The process change notice system is an extension of Micrel's unique, highly-detailed product run sheet (recipe) control system. PCN mechanisms meet the extreme demands for accuracy required in wafer processing.

Packaged product quality is controlled by a detailed set of instructions that are issued and controlled as part of the ECN system. These instructions cover all assembly and back-end processing steps and include the build-diagram, burn-in drawing, test set-up specification, test traveler, etc.

Inspection and Test Points

The flow charts accompanying this section describe the sequential steps of semiconductor processing and fabrication, and the associated test or inspection procedures and documentation.

Equipment Calibration

Micrel maintains a calibration system that conforms to MIL-STD-45662 and ensures measurement accuracy of equipment used to determine product workmanship and acceptability. Major provisions of the program include:

- Qualification of external calibration services,
- References traceable to National Institute of Standards and Technology (NIST). Identification of measurement and test equipment for type (electrical, mechanical, and optical) and frequency of calibration
- Certification history of equipment calibration and recall
- Recall status report history
- Audit history (calibration date stickers and recall designation)

Quality Control

The quality control program includes multiple inspections of material in-process, as well as final acceptance inspection of outgoing finished products. The QC system comprises product integrity characterizations of dimensional, structural, electrical and visual parameters. It also includes environmental and procedural monitoring checks.

The program elements include, but are not necessarily limited to:

- Particulate monitoring
- Temperature and relative humidity monitoring
- Electrostatic discharge monitoring and control
- Specification compliance reviews
- Random monitoring of wafers in-process
- Critical dimension qualification of product lot samples
- Wafer/die electrical sort
- Performance/trend data analysis
- Storage, handling, packaging and identification of raw materials, work-in-progress, and finished goods
- Returned material analysis

Finished product is inspected and tested prior to its shipment to the customer. Random sampling methodology is used to check deliverable wafer, die or part quality against published Micrel workmanship standards and customer specifications.

This final-product quality control program includes systems and procedures that assure the following:

- Correlation and qualification of test equipment to internal and customer specifications
- Manufacturing test operations are proper and complete
- Product lots conform to detailed test requirements for visual, mechanical and electrical performance criteria
- Documentation for each product/lot is proper and complete

New Products and Processes

New products or major process changes must undergo complete evaluation before they are certified at Micrel. Quality Assurance participation and approval is required in new product design reviews, product characterization and reliability studies, and documentation preparation.

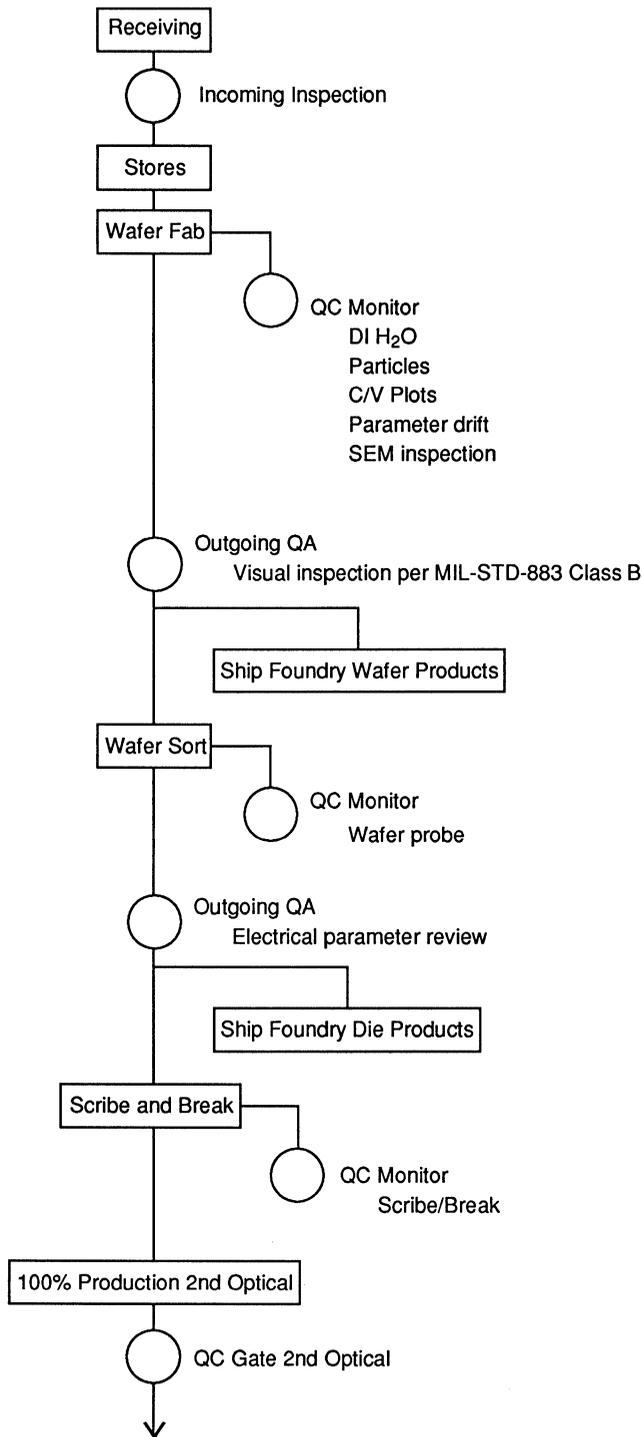
Certification is granted to new products or processes only after rigorous stress-testing, thorough monitoring of critical dimensions, careful failure analysis, and full process/trend data review. New packages are qualified and released for production only after Quality Assurance has determined that all environmental, mechanical and electrical tests are satisfactorily completed.

Complete and proper documentation of all material, process, procedure or packaging changes is required for final Quality Assurance certification.

Summary

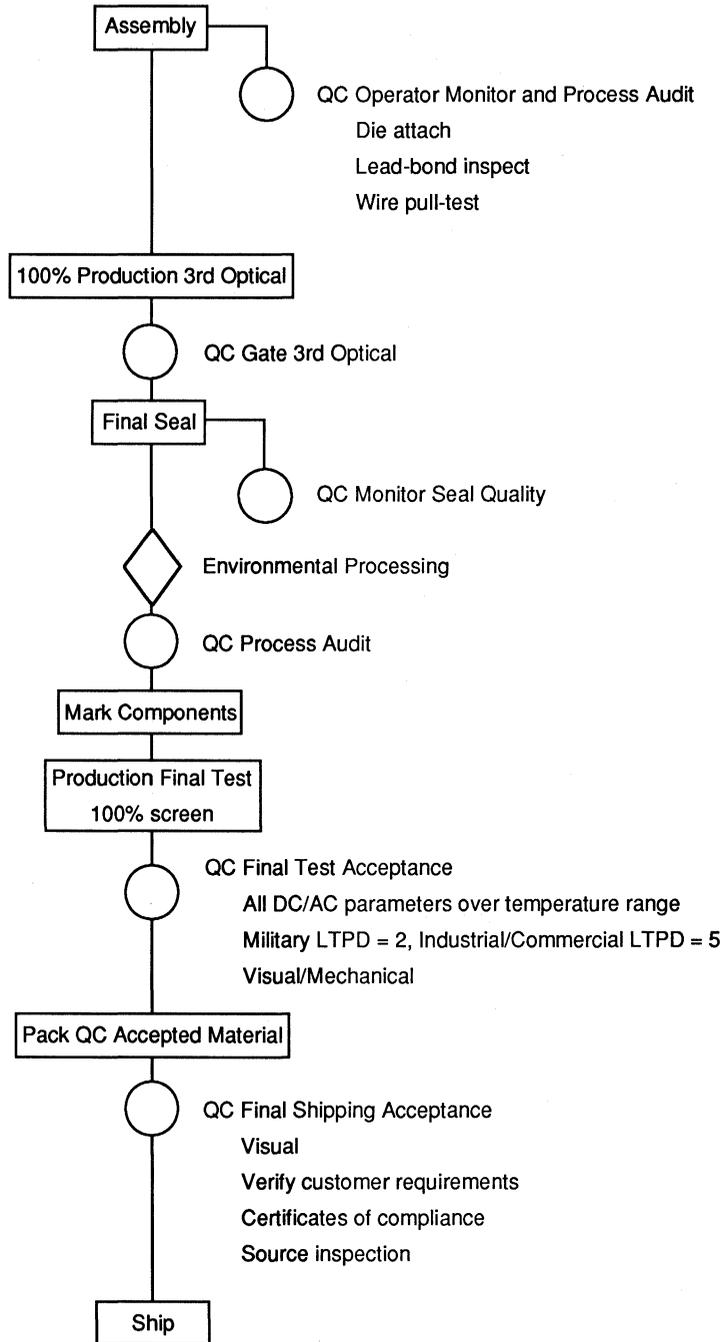
The Micrel Quality Assurance philosophy — that quality must be built into every process and product — is realized by the company's thorough implementation of the policies, procedures and processes required to ensure that our products and services meet the highest standards for material and workmanship.

Micrel Quality Flow for Semiconductor Circuit Manufacturing



1

Micrel Quality Flow for Semiconductor Assembly



FLOW CHART NOTES

Customer Returns

Perform analysis, answer and/or generate corrective action request, make disposition of return

Specification Review

Review internal specifications, verify agreement to customer requirements, issue specification to production

Reliability Assurance

Qualification — Test each device family in accordance with MIL-STD-883, Method 5004 and 5005, Class B

Certification — New products and major process changes subjected to accelerated test and process analysis

Failure Analysis — Performed on all Qualification and Process Monitor failures and customer returns as needed

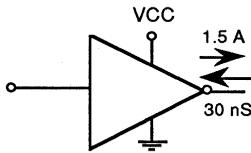
Document Control — Maintains files of all latest drawings and specifications, controls and issues wafer run-sheets, specifications, drawings and ECN numbers, distributes copies to specification control books and user groups.



SECTION 2: MOSFET DRIVERS

Page

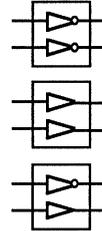
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Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC426 Family (Original)

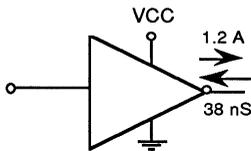
- * 30 nS into 1000 pF
- * 4.5 V to 18 V supply
- * 1.5 A peak output
- * 6 Ω output impedance
- * Available in surface mount packages



MIC426

MIC427

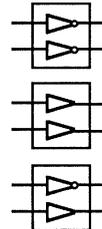
MIC428



Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC1426 Family (Low Cost)

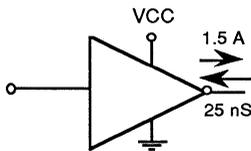
- * Low cost predriver
- * 38 nS into 1000 pF
- * 4.75 V to 16 V supply
- * 1.2 A peak output
- * 8 Ω output impedance
- * Available in surface mount packages



MIC1426

MIC1427

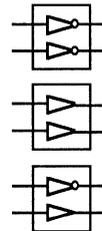
MIC1428



Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF.

MIC 4426 Family (Protected)

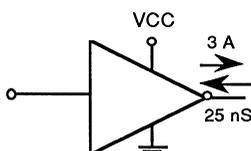
- * Latch-up protected
- * 25 nS into 1000 pF
- * 1.5 A peak output
- * Withstands 5 V negative swing
- * 4.5 V to 18 V supply
- * 7 Ω output impedance
- * Available in surface mount packages



MIC4426

MIC4427

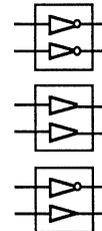
MIC4428



Drives a hex 4 - hex 5 size MOSFET; 6000 pF to 12000 pF.

MIC 4423 Family (High Current)

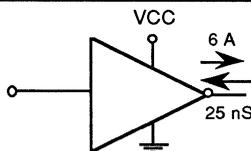
- * Latch-up protected
- * 25 nS into 1800 pF
- * 3 A peak output
- * Withstands 5 V negative swing
- * 4.5 V to 18 V supply
- * 3.5 Ω output impedance
- * Available in surface mount packages



MIC4423

MIC4424

MIC4425



Drives a hex 6 - hex 7 size MOSFET; 15000 pF to 16000 pF.

MIC4420/4429 (Singles)

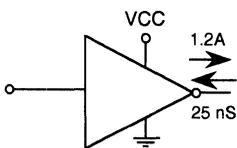
- * Latch-up protected
- * 25 nS into 10,000 pF
- * 6 A peak output
- * Withstands 5 V negative swing
- * 4.5 V to 18 V supply
- * 2.5 Ω output impedance
- * Available in surface mount and high temperature packages



MIC4420

MIC4429

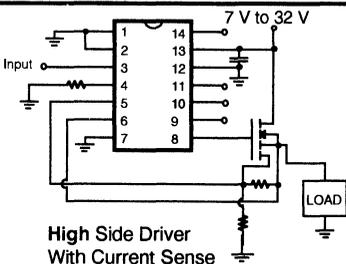
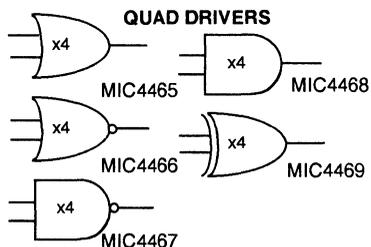
FET Driver Selection Guide



Drives a hex 0 - hex 3 size MOSFET; 400 pF to 3000 pF

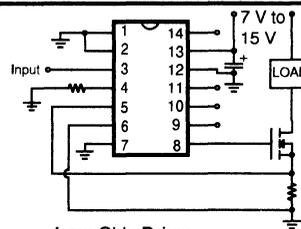
MIC4465 Family (Quads)

- * Latch-up protected
- * 25 nS into 470 pF
- * 1.2 A peak output
- * 4.5 V to 18 V supply
- * Available in surface mount packages
- * Five logic choices

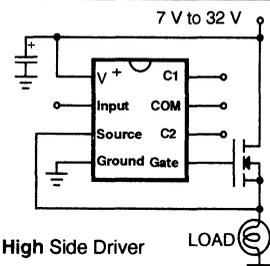


High Side Driver With Current Sense

- ### MIC5010
- * Full featured predriver
 - * Optional speed up caps
 - * 7 V to 32 V supply
 - * Internal charge pump
 - * 60 μ S into 1 nF
 - * Over current sensing
 - * Fault flag output
 - * Dynamic sensing threshold
 - * Surface mount packages

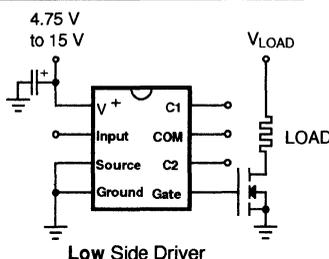


Low Side Driver With Current Sense

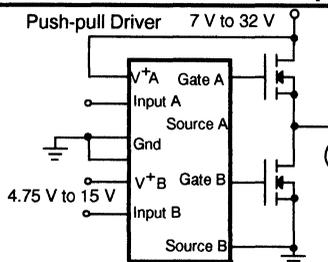


High Side Driver

- ### MIC5011
- * Minimum parts count
 - * Optional speed up caps
 - * 4.75 V to 32 V supply
 - * Internal charge pump
 - * 60 μ S into 1 nF
 - * Surface mount packages

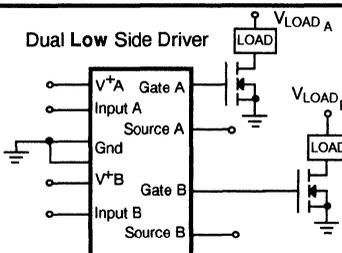


Low Side Driver

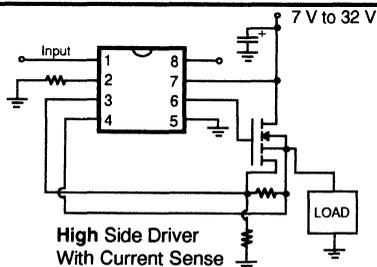


Push-pull Driver 7 V to 32 V

- ### MIC5012
- * Dual predriver
 - * Provides high and low side drive for H-bridge
 - * 4.75 V to 32 V supply
 - * Internal charge pump
 - * 60 μ S into 1 nF
 - * Surface mount packages

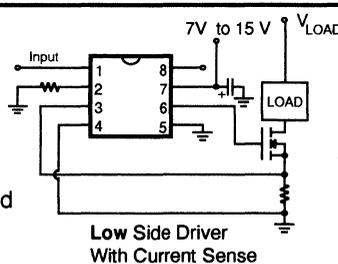


Dual Low Side Driver



High Side Driver With Current Sense

- ### MIC5013
- * Over current sensing
 - * 7 V to 32 V supply
 - * Internal charge pump
 - * 60 μ S into 1 nF
 - * Fault flag output
 - * Dynamic sensing threshold
 - * Surface mount packages



Low Side Driver With Current Sense



MIC426/427/428

Dual Power MOSFET Driver

General Description

The MIC426/427/428 are dual CMOS high speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equalling the supply. The CMOS output will be within 25 mV of ground or positive supply. Bipolar designs are capable of swinging only within 1 volt of the supply.

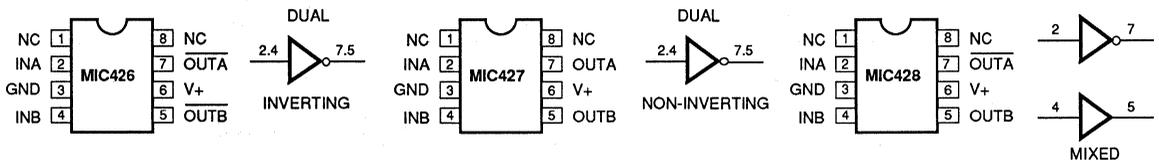
The low impedance high current driver outputs will swing a 1000 pF load 18 V in 30 nS. The unique current and voltage drive qualities make the MIC426/427/428 ideal power MOSFET drivers, line drivers and DC to DC converter building blocks.

Input logic signals may equal the power supply voltage. Input current is a low 1 μ A making direct interface to CMOS/BIPOLAR switch mode power supply control integrated circuits

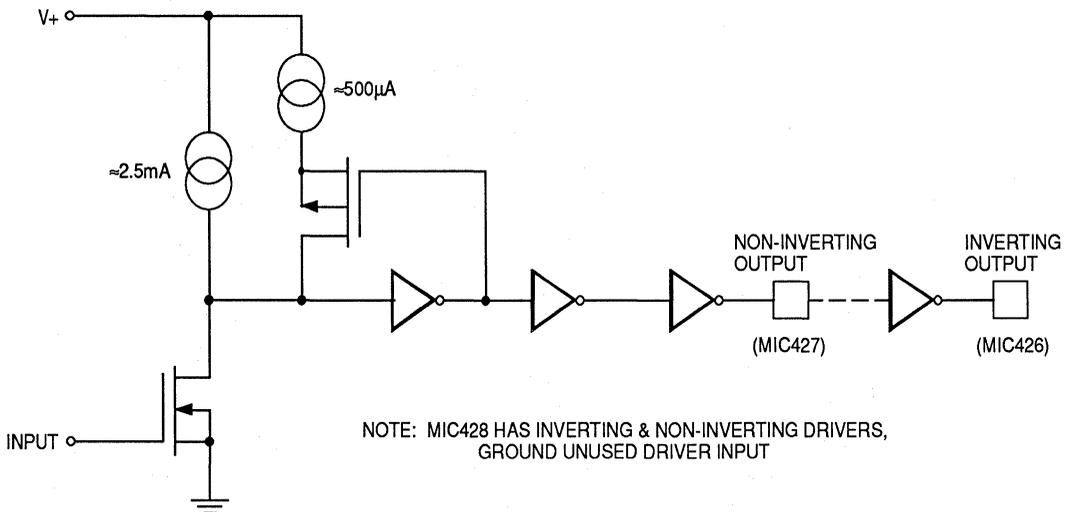
Features

- High Speed Switching ($C_H = 1000$ pF) 30 nS
- High Peak Output Current 1.5 A
- High Output Voltage Swing $V_S - 25$ mV
GND + 25 mV
- Low Input Current (Logic "0" or "1") 1 μ A
- TTL/CMOS Input Compatible
- Available in Inverting & Non-Inverting Configurations
- Wide Operating Supply Voltage 4.5 V to 18 V
- Low Power Consumption
(Inputs Low) 0.4 mA
(Inputs High) 8 mA
- Single Supply Operation
- Low Output Impedance 6 Ω
- Pin Out Equivalent to DS0026 & MMH0026

Pin Configuration



Functional Diagram



possible as well as open collector analog comparators.

Quiescent power supply current is 8 mA maximum. The MIC426 requires 1/5 the current of the pin compatible bipolar DS0026 device. This is important in DC to DC converter applications with power efficiency constraints and high frequency switch mode power supply applications. Quiescent

current is typically 6 mA when driving a 1000 pF load 18 V at 100 kHz.

The inverting MIC426 driver is pin compatible with the bipolar DS0026 and MMH0026 devices. The MIC427 is non-inverting; the MIC428 contains an inverting and non-inverting driver.

Ordering Information

Part Number	Temperature Range	Package	Configuration
MIC426CM MIC426BM	0°C to +70°C -40°C to +85°C	8-pin SOIC	Inverting
MIC426CN	0°C to +70°C	8-pin plastic DIP	Inverting
MIC426BJ MIC426AJ	-40°C to +85°C -55°C to +125°C	8-pin CerDIP	Inverting
MIC426CY	—	CHIP	Inverting
MIC427CM MIC427BM	0°C to +70°C -40°C to +85°C	8-pin SOIC	Non-Inverting
MIC427CN	0°C to +70°C	8-pin plastic DIP	Non-Inverting
MIC427BJ MIC427AJ	-40°C to +85°C -55°C to +125°C	8-pin CerDIP	Non-Inverting
MIC427CY	—	CHIP	Non-Inverting
MIC428CM MIC428BM	0°C to +70°C -40°C to +85°C	8-pin SOIC	Non-Inv. & Inverting
MIC428CN	0°C to +70°C	8-pin plastic DIP	Non-Inv. & Inverting
MIC428BJ MIC428AJ	-40°C to +85°C -55°C to +125°C	8-pin CerDIP	Non-Inv. & Inverting
MIC428CY	—	CHIP	Non-Inv. & Inverting

2

Absolute Maximum Ratings (Notes 1, 2, and 3)

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Supply Voltage	20 V
Input Voltage Any Terminal	$V_S + 0.3 \text{ V to GND} - 0.3 \text{ V}$
Maximum Chip Temperature	150°C
Storage Temperature	-65°C to 150°C
Lead Temperature (10 sec)	300°C
Package Thermal Resistance	
CerDIP $R_{\theta J-A}$ (°C/W)	150
CerDIP $R_{\theta J-C}$ (°C/W)	50
PDIP $R_{\theta J-A}$ (°C/W)	125
PDIP $R_{\theta J-C}$ (°C/W)	42
SOIC $R_{\theta J-A}$ (°C/W)	250
SOIC $R_{\theta J-C}$ (°C/W)	75

Operating Temperature Range

C Version	0°C to +70°C
B Version	-40°C to +85°C
A Version	-55°C to +125°C

MIC426 Electrical Characteristics: $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-1		1	μA
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	$V_{IN} = 0.8\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		10	15	Ω
7	R_O	Output Resistance	$V_{IN} = 2.4\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		6	10	Ω
8	I_{PK}	Peak Output Current			1.5		A
SWITCHING TIME							
9	T_R	Rise Time	Test Figure 1			30	nS
10	T_F	Fall Time	Test Figure 1			20	nS
11	T_{D1}	Delay Time	Test Figure 1			40	nS
12	T_{D2}	Delay Time	Test Figure 1			75	nS
POWER SUPPLY							
13	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			8.0	mA
14	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.4	mA

MIC426 Electrical Characteristics:Over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA

MIC426 Electrical Characteristics:Over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified (Continued).

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	$V_{IN} = 0.8\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		13	20	Ω
7	R_O	Output Resistance	$V_{IN} = 2.4\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		8	15	Ω
SWITCHING TIME							
8	T_R	Rise Time	Test Figure 1			60	nS
9	T_F	Fall Time	Test Figure 1			40	nS
10	T_{D1}	Delay Time	Test Figure 1			60	nS
11	T_{D2}	Delay Time	Test Figure 1			120	nS
POWER SUPPLY							
12	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			12.0	mA
13	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.6	mA

MIC427 Electrical Characteristics: $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-1		1	μA
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	$V_{IN} = 2.4\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		10	15	Ω
7	R_O	Output Resistance	$V_{IN} = 0.8\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		6	10	Ω
8	I_{PK}	Peak Output Current			1.5		A

MIC427 Electrical Characteristics: $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified. (Continued)

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
SWITCHING TIME							
9	T_R	Rise Time	Test Figure 1			30	nS
10	T_F	Fall Time	Test Figure 1			20	nS
11	T_{D1}	Delay Time	Test Figure 1			40	nS
12	T_{D2}	Delay Time	Test Figure 1			75	nS
POWER SUPPLY							
13	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			8.0	mA
14	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.4	mA

MIC427 Electrical Characteristics:Over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	$V_{IN} = 2.4\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		13	20	Ω
7	R_O	Output Resistance	$V_{IN} = 0.8\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		8	15	Ω
SWITCHING TIME							
8	T_R	Rise Time	Test Figure 1			60	nS
9	T_F	Fall Time	Test Figure 1			40	nS
10	T_{D1}	Delay Time	Test Figure 1			60	nS
11	T_{D2}	Delay Time	Test Figure 1			120	nS
POWER SUPPLY							
12	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			12.0	mA
13	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.6	mA

MIC428 Electrical Characteristics: $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-1		1	μA
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	Output High $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		10	15	Ω
7	R_O	Output Resistance	Output High $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		6	10	Ω
8	I_{PK}	Peak Output Current			1.5		A
SWITCHING TIME							
9	T_R	Rise Time	Test Figure 1			30	nS
10	T_F	Fall Time	Test Figure 1			20	nS
11	T_{D1}	Delay Time	Test Figure 1			40	nS
12	T_{D2}	Delay Time	Test Figure 1			75	nS
POWER SUPPLY							
13	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			8.0	mA
14	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.4	mA

MIC428 Electrical Characteristics:Over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT							
1	V_{IH}	Logic 1 Input Voltage		2.4			V
2	V_{IL}	Logic 0 Input Voltage				0.8	V
3	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-10		10	μA

MIC428 Electrical Characteristics:Over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT							
4	V_{OH}	High Output Voltage		$V_S - 0.025$			V
5	V_{OL}	Low Output Voltage				0.025	V
6	R_O	Output Resistance	Output High $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		13	20	Ω
7	R_O	Output Resistance	Output High $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		8	15	Ω
SWITCHING TIME							
8	T_R	Rise Time	Test Figure 1			60	nS
9	T_F	Fall Time	Test Figure 1			40	nS
10	T_{D1}	Delay Time	Test Figure 1			60	nS
11	T_{D2}	Delay Time	Test Figure 1			120	nS
POWER SUPPLY							
12	I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			12.0	mA
13	I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.6	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.**Note 2:** Static Sensitive device (above 2kV). Unused devices must be stored in conductive material to protect devices from static discharge and static fields.**Note 3:** Switching times guaranteed by design.

Switching Time Test Circuits

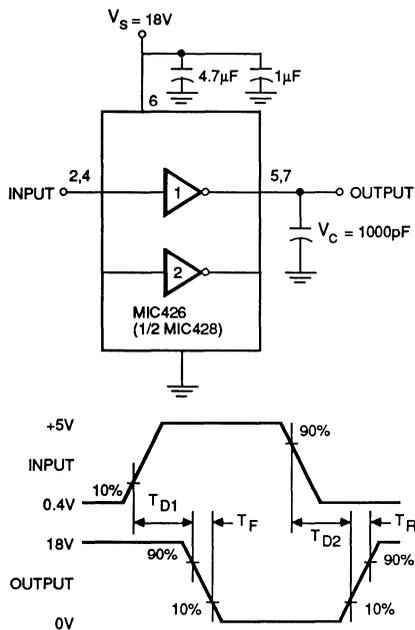


Figure 1. Inverting Driver Switching Time

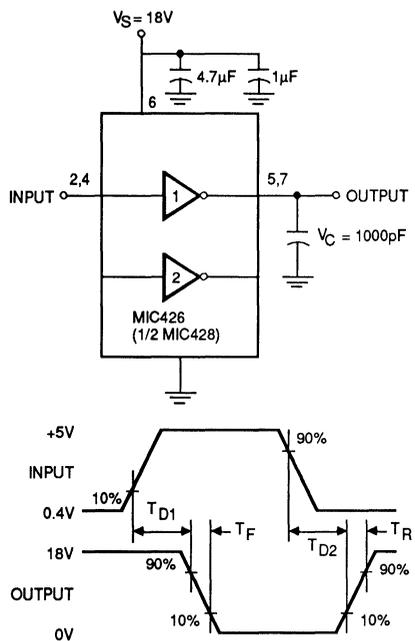
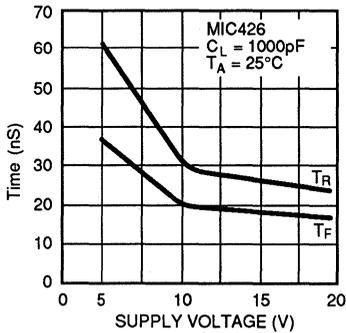


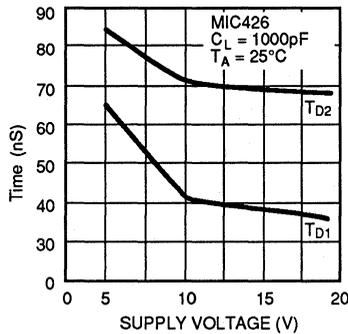
Figure 2. Non-Inverting Driver Switching Time

Typical Characteristic Curves

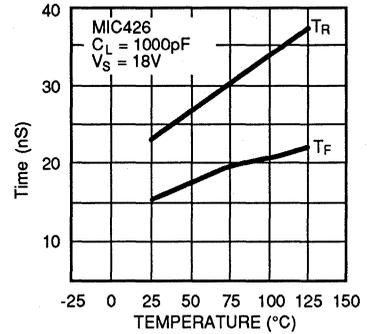
Rise and Fall Time vs Supply Voltage



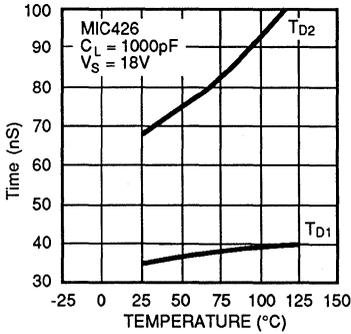
Delay Time vs Supply Voltage



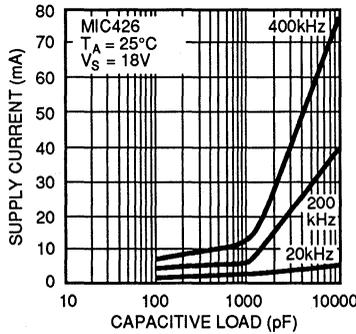
Rise and Fall Time vs Temperature



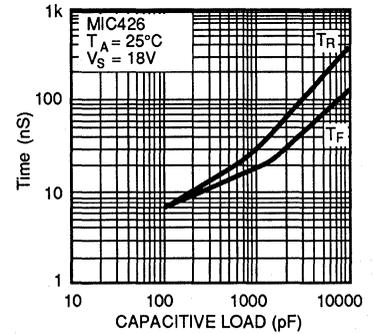
Delay Time vs Temperature



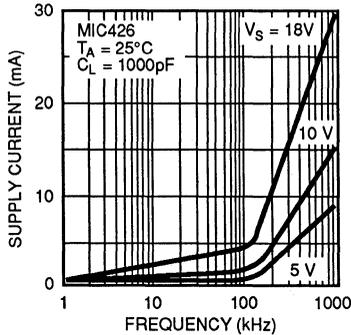
Supply Current vs Capacitive Load



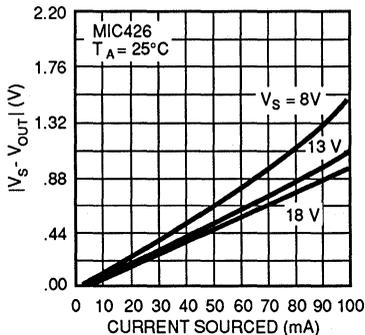
Rise and Fall Time vs Capacitive Load



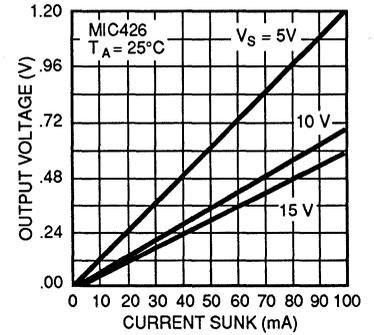
Supply Current vs Frequency



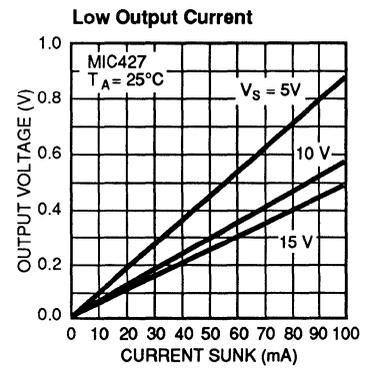
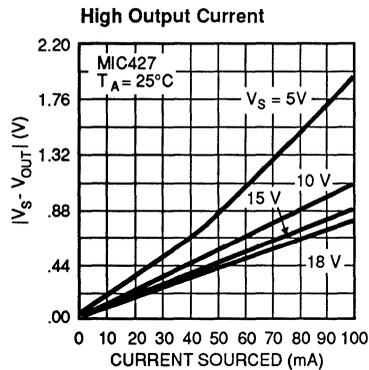
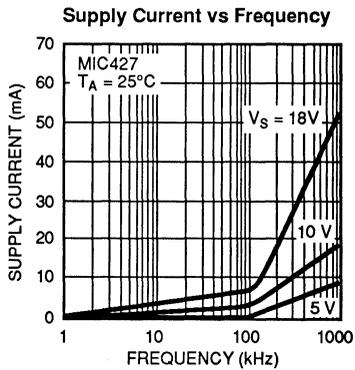
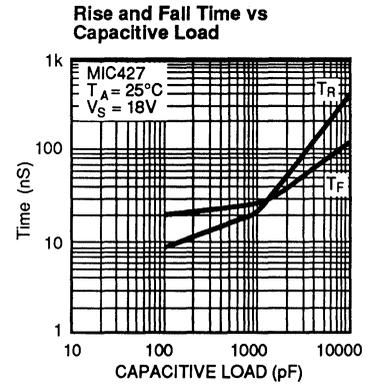
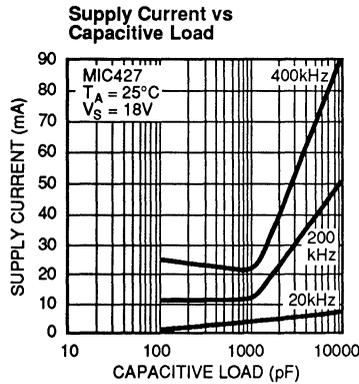
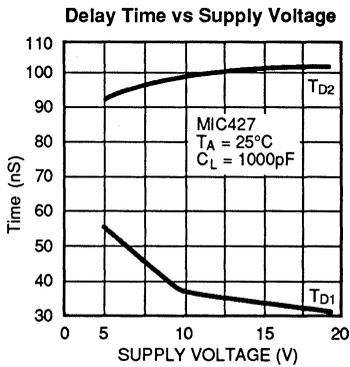
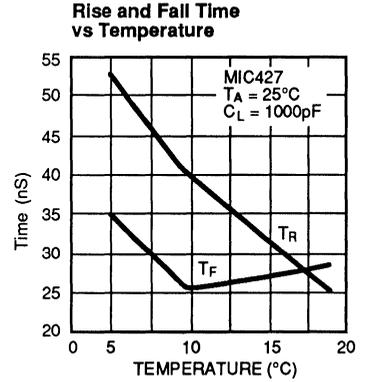
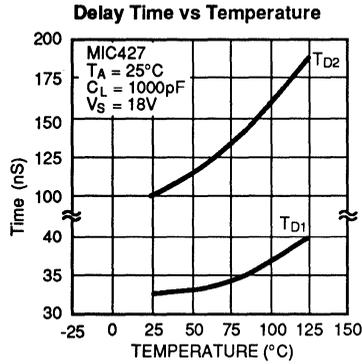
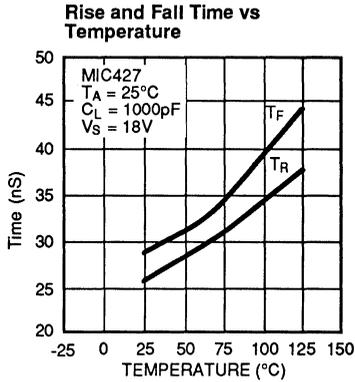
High Output vs Current



Low Output Current

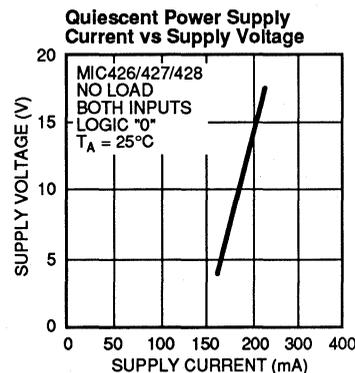
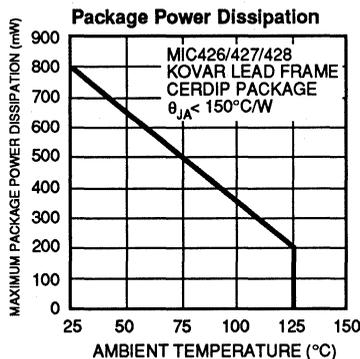
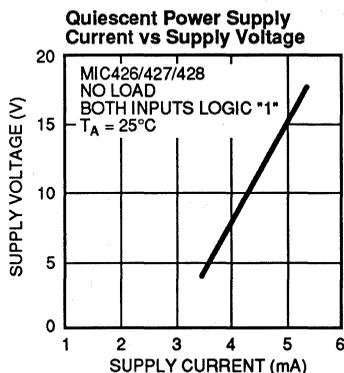


Typical Characteristic Curves (Continued)



2

Typical Characteristic Curves (Continued)



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 1000 pF load 18 volts in 25 nS requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 4.7 μF solid tantalum capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The MIC426 and MIC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 400 μA maximum. Minimum power dissipation occurs for logic "0" inputs for the MIC426/427/428; unused driver inputs **must be grounded or tied to the positive supply**.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V making the device TTL compatible over the 4.5 V to 18 V operating supply range. Input current is less than 1 μA over this range.

The MIC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The MIC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15 V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_O = P_{DC} + P_{AC} \\ = V_O(I_{DC}) + f C_L V_S^2$$

Where: V_O = DC output voltage
 I_{DC} = DC output load current
 f = Switching frequency
 V_S = Supply voltage

In power MOSFET drive applications, the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

The magnitude of P_{AC} is readily estimated for several cases:

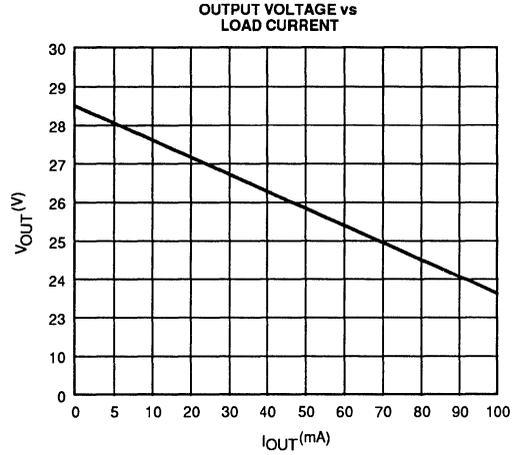
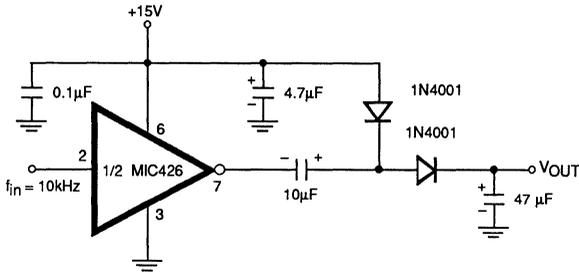
- | | |
|---------------------|---------------------|
| A. 1. $f = 200$ kHz | B. 1. $f = 200$ kHz |
| 2. $C_L = 1000$ pF | 2. $C_L = 1000$ pF |
| 3. $V_S = 18$ V | 3. $V_S = 15$ V |
| 4. $P_{AC} = 65$ mW | 4. $P_{AC} = 45$ mW |

During output level state changes, a current surge will flow through the series connected N and P channel output

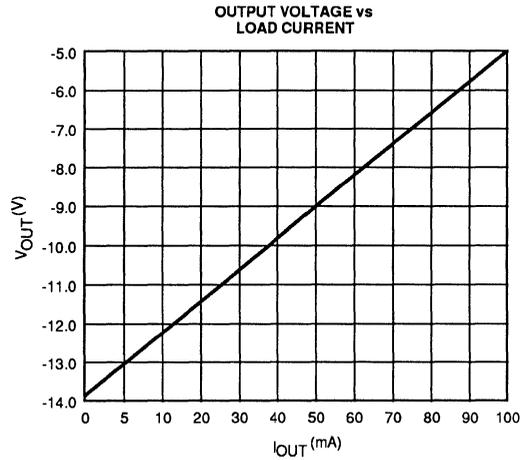
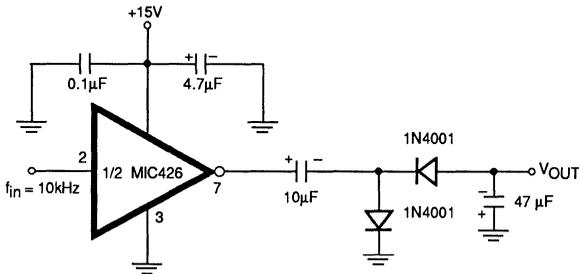
MOSFETS as one device is turning "ON" while the other is turning "OFF." The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must**

be tied to ground and not be allowed to float. Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

Voltage Doubler



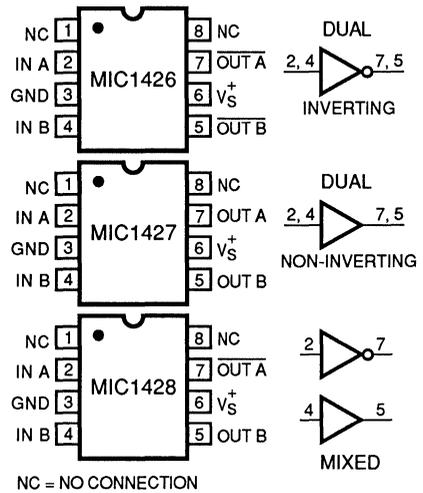
Voltage Inverter



Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC1426CM	0–70°C	8-Pin SO	Inverting
MIC1426CN	0–70°C	8-Pin Plastic DIP	Inverting
MIC1427CM	0–70°C	8-Pin SO	Non-Inverting
MIC1427CN	0–70°C	8-Pin Plastic DIP	Non-Inverting
MIC1428CM	0–70°C	8-Pin SO	Inverting and Non-Inverting
MIC1428CN	0–70°C	8-Pin Plastic DIP	Inverting and Non-Inverting

Pin Configurations



Test Circuits

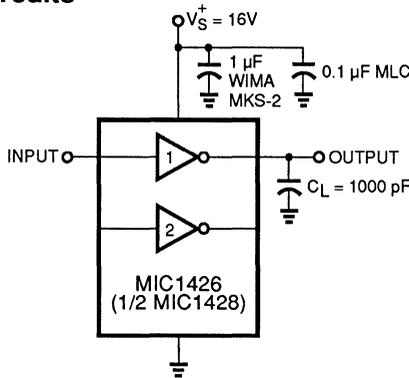


Figure 1. Inverting Driver Switching Time

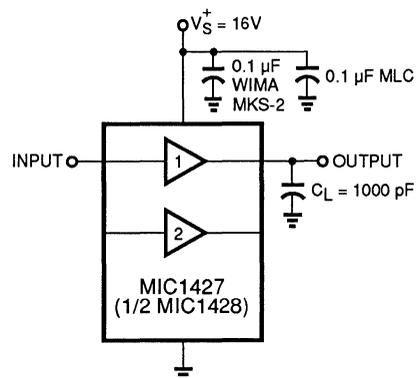


Figure 2. Non-Inverting Driver Switching Time

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation		Input Voltage, Any Terminal	$V_S + 0.3V$ to GND $-0.3V$
Plastic DIP	1W	Operating Temperature: C Version	$0^{\circ}C$ to $+70^{\circ}C$
SOIC	500 mW	Maximum Chip Temperature	$+150^{\circ}C$
Derating Factor		Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Plastic DIP	8 mW/ $^{\circ}C$	Lead Temperature (10 sec)	$+300^{\circ}C$
SOIC	4 mW/ $^{\circ}C$		
Supply Voltage	18V		

- NOTES:**
1. Functional operation above the absolute maximum stress ratings is not implied.
 2. Static-sensitive device (above 2kV). Unused devices must be stored in conductive material to protect devices from static discharge.
 3. Switching times guaranteed by design.

Electrical Characteristics: $T_A = 25^{\circ}C$ with $4.75V < V_S < 16V$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1, Input Voltage		3			V
V_{IL}	Logic 0, Input Voltage				0.8	V
I_{IN}	Input Current	$0V < V_{IN} < V_S$	-1		1	μA
OUTPUT						
V_{OH}	High Output Voltage	Test Figures 1 and 2	$V_S - 0.025$			V
V_{OL}	Low Output Voltage	Test Figures 1 and 2			0.025	V
R_O	Output Resistance	$V_{IN} = 0.8V$ $I_{OUT} = 10 mA, V_S = 16V$		12	18	Ω
R_O	Output Resistance	$V_{IN} = 3V$ $I_{OUT} = 10 mA, V_S = 16V$		8	12	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Current	Withstand Reverse Current	>500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figures 1 and 2			35	nS
t_F	Fall Time	Test Figures 1 and 2			25	nS
t_{D1}	Delay Time	Test Figures 1 and 2			75	nS
t_{D2}	Delay Time	Test Figures 1 and 2			75	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3V$ (Both Inputs) $V_{IN} = 0V$ (Both Inputs)			9 0.5	mA mA

Electrical Characteristics:

Over operating temperature range with $4.75V < V_{S^+} < 16V$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1, Input Voltage		3			V
V_{IL}	Logic 0, Input Voltage				0.8	V
I_{IN}	Input Current	$0V < V_{IN} < V_S$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage	Test Figures 1 and 2	$V_S - 0.025$			V
V_{OL}	Low Output Voltage	Test Figures 1 and 2			0.025	V
R_O	Output Resistance	$V_{IN} = 0.8V$ $I_{OUT} = 10 \text{ mA}$, $V_S = 16V$		15	23	Ω
R_O	Output Resistance	$V_{IN} = 3V$ $I_{OUT} = 10 \text{ mA}$, $V_S = 16V$		10	18	Ω
I	Latch-Up Current	Withstand Reverse Current	>500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figures 1 and 2			60	nS
t_F	Fall Time	Test Figures 1 and 2			40	nS
t_{D1}	Delay Time	Test Figures 1 and 2			125	nS
t_{D2}	Delay Time	Test Figures 1 and 2			125	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3V$ (Both Inputs)			13	mA
I_S	Power Supply Current	$V_{IN} = 0V$ (Both Inputs)			0.7	mA

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000 pF load 16 V in 25 nS, requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5 in.) should be used. A 1.0 μF film capacitor in parallel with one or two 0.1 μF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

The MIC1426 and MIC1428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

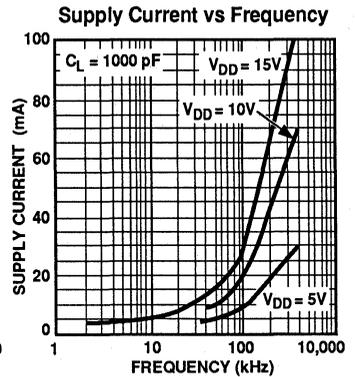
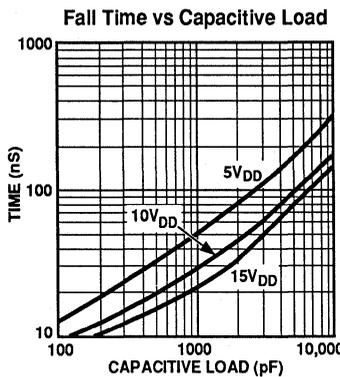
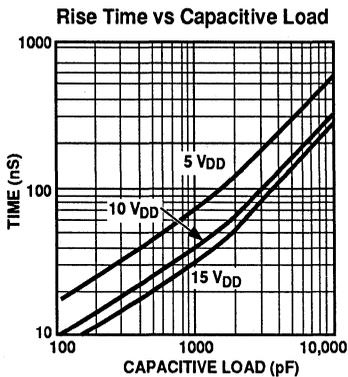
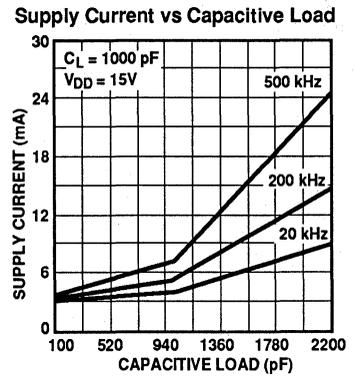
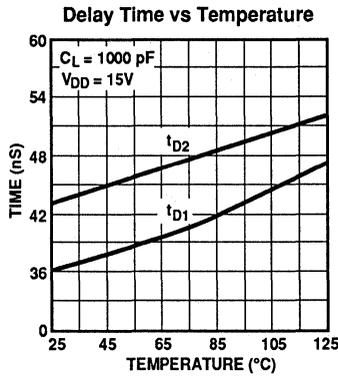
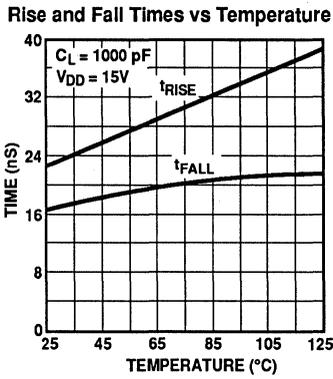
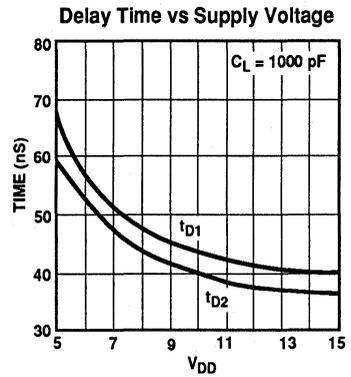
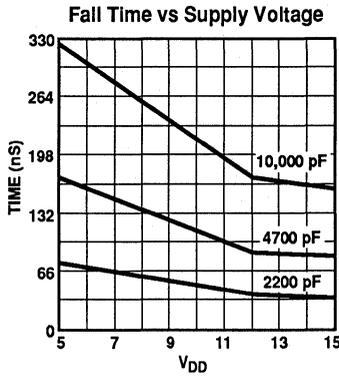
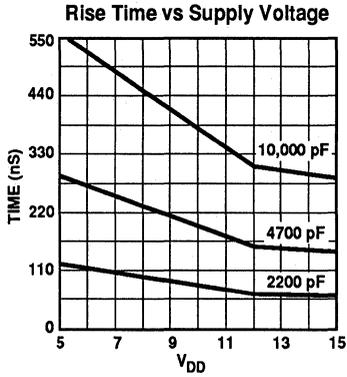
Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 9 mA. Logic "0" input level signals reduce quiescent current to 500 μA maximum. **Unused driver inputs must be connected to V_{S^+} or GND.** Minimum power dissipation occurs for logic "0" inputs for the MIC1426/27/28.

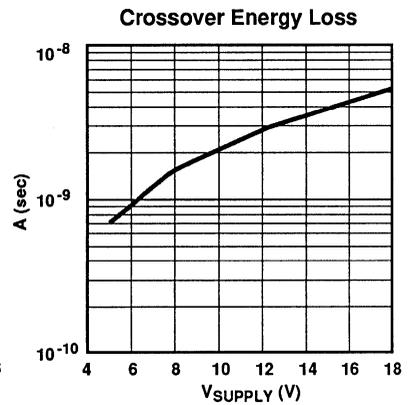
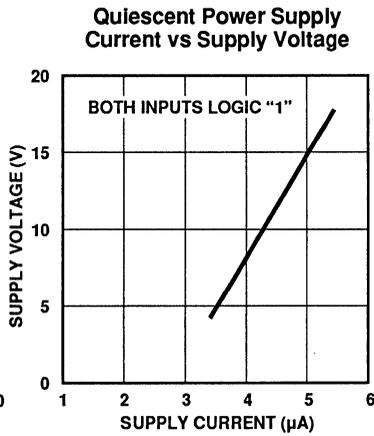
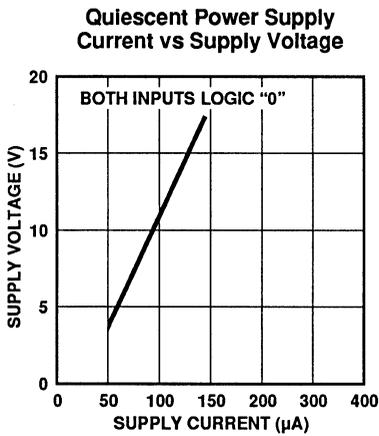
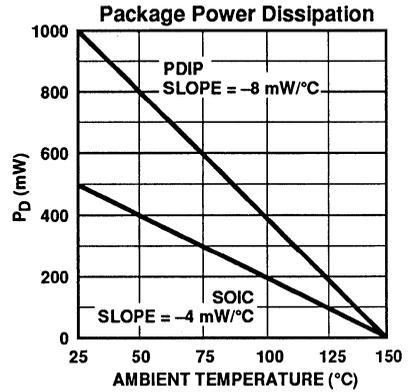
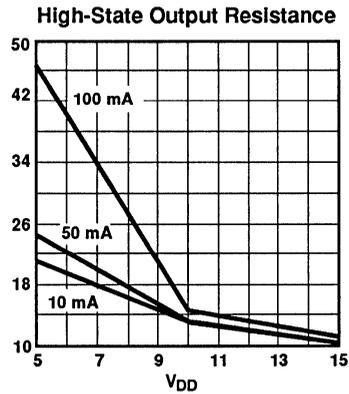
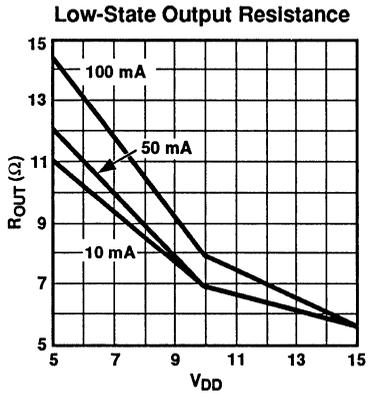
The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V, making logic "1" input any voltage greater than 1.5 V up to V_{S^+} . Input current is less than 1 μA over this range.

The MIC1426/27/28 may be directly driven by the TL494, SG1526/27, MIC18HC42, TSC170 and similar switch-mode power supply integrated circuits.

MIC1426/7/8 Typical Characteristic Curves



MIC1426/7/8 Typical Characteristic Curves (Cont.)





MIC4420/4429

High-Speed, High-Current Single MOSFET Driver

General Description

The MIC4420/4429 CMOS MOSFET drivers are tough, efficient, and easy to use. This family of devices are 6A (peak) single output MOSFET drivers.

The MIC4420/4429 will drive even the largest MOSFETs and improve the safe operating area margin.

These devices are tough due to extra steps taken to protect them from failures. An epitaxial layer is used to prevent CMOS latch-up. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part. Special circuits have been added to protect against damage from electrostatic discharge. They are also tough because of Micrel's commitment to quality in manufacturing.

Because these devices are fabricated in CMOS, they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during power up/down sequencing.

These CMOS drivers are easy to use. Three or more discrete components can be replaced with a single device to save PCB area. Any logic input from 2.4V to V_{DD} can be used without external speed-up capacitors or resistor networks.

This family is available in inverting (MIC4429) and non-inverting (MIC4420) configurations.

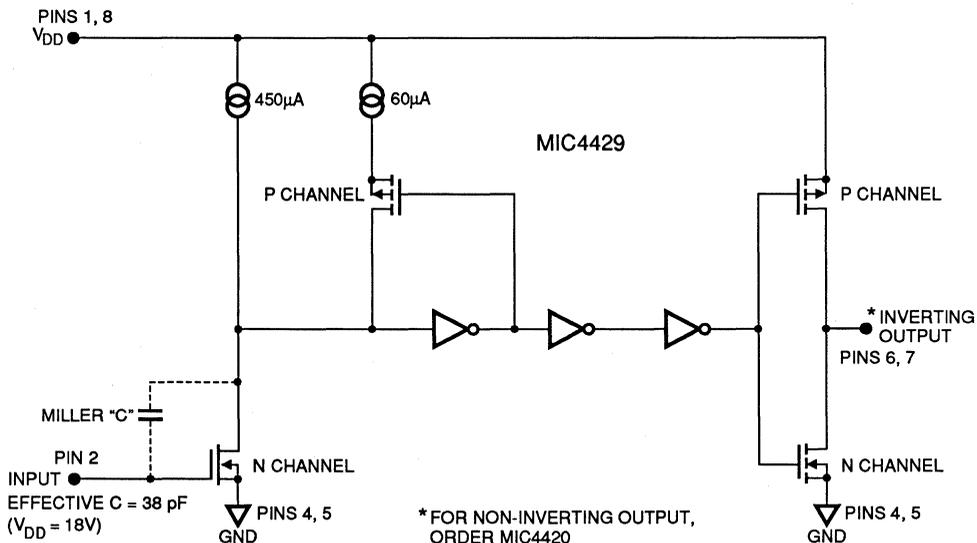
Features

- Built using reliable CMOS processes
- Latch-Up Protected: Will Withstand >500 mA Reverse Output Current
- Logic Input Will Withstand Negative Swing of Up to 5V
- Matched Rise and Fall Times 25 nS
- High Peak Output Current 6 A Peak
- Wide Operating Range 4.5 V to 18 V
- High Capacitive Load Drive 10,000 pF
- Low Delay Time 55 nS Typ
- Logic High Input for Any Voltage From 2.4 V to V_{DD}
- Low Supply Current 450 μ A With Logic 1 Input
- Low Output Impedance 2.5 Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- MIL-STD-883 Method 5004/5005 version available

Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

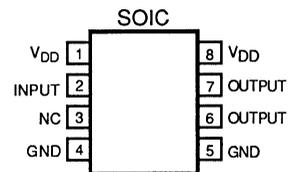
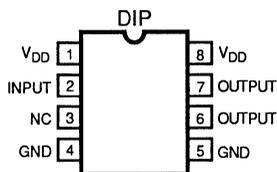
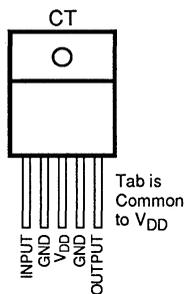
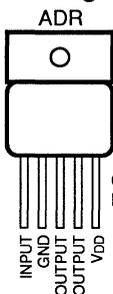
Functional Diagram



Ordering Information

Part No.	Temperature Range	Package	Configuration
MIC4420CN	0°C to +70°C	8-Pin PDIP	Non-Inverting
MIC4420BN	-40°C to +85°C	8-Pin PDIP	Non-Inverting
MIC4420CM	0°C to +70°C	8-Pin SOIC	Non-Inverting
MIC4420BM	-40°C to +85°C	8-Pin SOIC	Non-Inverting
MIC4420BJ	-40°C to +85°C	8-Pin CerDIP	Non-Inverting
MIC4420AJ	-55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4420AJB	-55°C to +125°C	8-Pin CerDIP	Non-Inverting
MIC4420CT	0°C to +70°C	5-Pin TO-220	Non-Inverting
MIC4420ADR	-55°C to +125°C	5-Pin MO-078	Non-Inverting
MIC4420ADRB	-55°C to +125°C	5-Pin MO-078	Non-Inverting
MIC4429CN	0°C to +70°C	8-Pin PDIP	Inverting
MIC4429BN	-40°C to +85°C	8-Pin PDIP	Inverting
MIC4429CM	0°C to +70°C	8-Pin SOIC	Inverting
MIC4429BM	-40°C to +85°C	8-Pin SOIC	Inverting
MIC4429BJ	-40°C to +85°C	8-Pin CerDIP	Inverting
MIC4429AJ	-55°C to +125°C	8-Pin CerDIP	Inverting
MIC4429AJB	-55°C to +125°C	8-Pin CerDIP	Inverting
MIC4429CT	0°C to +70°C	5-Pin TO-220	Inverting
MIC4429ADR	-55°C to +125°C	5-Pin MO-078	Inverting
MIC4429ADRB	-55°C to +125°C	5-Pin MO-078	Inverting

Pin Configurations



NOTE: Duplicate pins must both be connected for proper operation.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Power Dissipation, $T_{\text{AMBIENT}} \leq 25^{\circ}\text{C}$

PDIP	1W
SOIC	500 mW
CerDIP	800 mW
MO-078AA	1.75W
5-Pin TO-220	1.5W

Power Dissipation, $T_{\text{CASE}} \leq 25^{\circ}\text{C}$

MO-078AA	10W
5-Pin TO-220	12.5W

Derating Factors (To Ambient)

PDIP	8 mW/°C
SOIC	4 mW/°C
CerDIP	6.4 mW/°C
MO-078AA	14 mW/°C
5-Pin TO-220	12 mW/°C

Thermal Impedances (To Case)

MO-078AA $R_{\theta\text{J-C}}$	12.5°C/W
5-Pin TO-220 $R_{\theta\text{J-C}}$	10°C/W

Storage Temperature -65°C to +125°C

Operating Temperature (Chip) 150°C

Operating Temperature (Ambient)

C Version	0°C to +70°C
B Version	-40°C to +85°C
A Version	-55°C to +125°C

Lead Temperature (10 sec) 300°C

Supply Voltage 20V

Input Voltage -5V to V_{DD}

Input Current ($V_{\text{IN}} > V_{\text{DD}}$) 50 mA

Electrical Characteristics: ($T_A = 25^\circ\text{C}$ with $4.5\text{ V} < V_{DD} < 18\text{ V}$ unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4	1.8		V
V_{IL}	Logic 0 Input Voltage			1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		-5		$V_{DD}+0.3$	V
I_{IN}	Input Current	$0\text{ V} < V_{IN} < V_S$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	$V_{DD}-0.025$			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output Low	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{ V}$		2.1	2.8	Ω
R_O	Output Resistance, Output High	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{ V}$		1.5	2.5	Ω
I_{PK}	Peak Output Current	$V_{DD} = 18\text{ V}$ (See Figure 5)		6		A
I_R	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, $C_L = 2500\text{ pF}$		25	35	nS
t_F	Fall Time	Test Figure 1, $C_L = 2500\text{ pF}$		25	35	nS
t_{D1}	Delay Time	Test Figure 1		55	75	nS
t_{D2}	Delay Time	Test Figure 1		55	75	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3\text{ V}$ $V_{IN} = 0\text{ V}$		0.45 55	1.5 150	mA μA
V_{DD}	Operating Input Voltage		4.5		18	V

Electrical Characteristics: ($T_A = 25^\circ\text{C}$ with $4.5\text{ V} < V_{DD} < 18\text{ V}$ unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
$V_{IN}(\text{Max})$	Input Voltage Range		-5		$>V_{DD}$	V
I_{IN}	Input Current	$0\text{ V} < V_{IN} < V_S$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage	See Figure 1	$V_{DD}-0.025$			V
V_{OL}	Low Output Voltage	See Figure 1			0.025	V
R_O	Output Resistance, Output Low	$I_{OUT} = 10\text{ mA}, V_{DD} = 18\text{ V}$		3	5	Ω
R_O	Output Resistance, Output High	$I_{OUT} = 10\text{ mA}, V_{DD} = 18\text{ V}$		2.3	5	Ω
SWITCHING TIME (Note 3)						
t_R	Rise Time	Test Figure 1, $C_L = 2500\text{ pF}$		32	60	nS
t_F	Fall Time	Test Figure 1, $C_L = 2500\text{ pF}$		34	60	nS
t_{D1}	Delay Time	Test Figure 1		50	100	nS
t_{D2}	Delay Time	Test Figure 1		65	100	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3\text{ V}$ $V_{IN} = 0\text{ V}$		0.45 0.06	1.5 0.4	mA mA
V_{DD}	Operating Input Voltage		4.5		18	V

- NOTE 1:** Functional operation above the absolute maximum stress ratings is not implied.
- NOTE 2:** Static-sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent damage from static discharge.
- NOTE 3:** Switching times guaranteed by design.

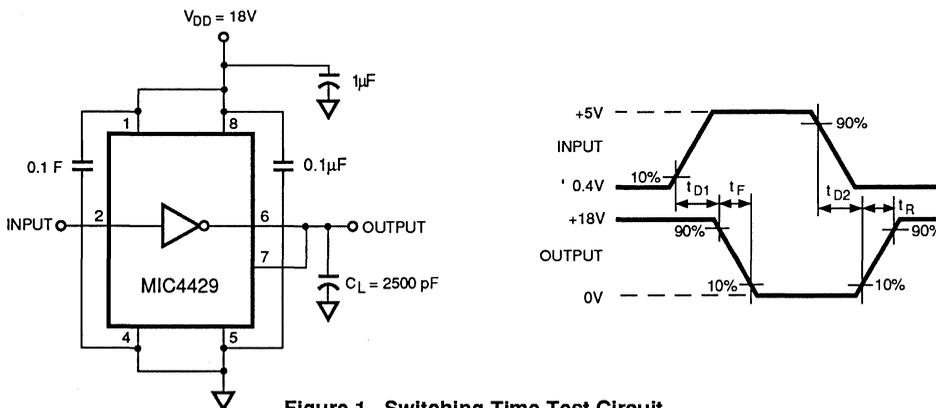
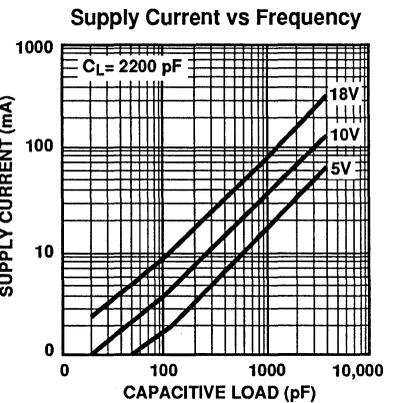
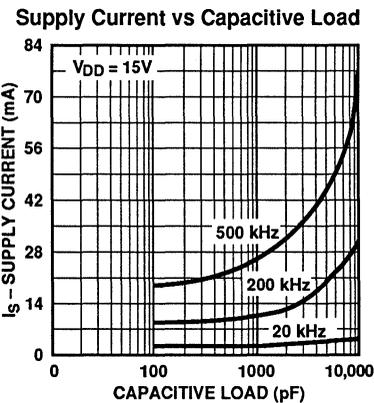
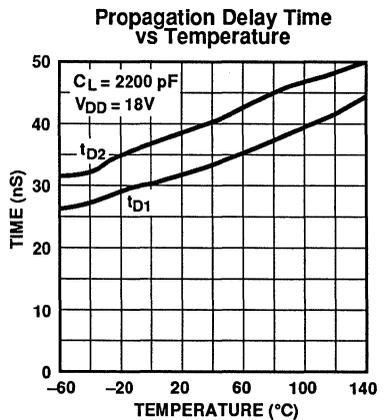
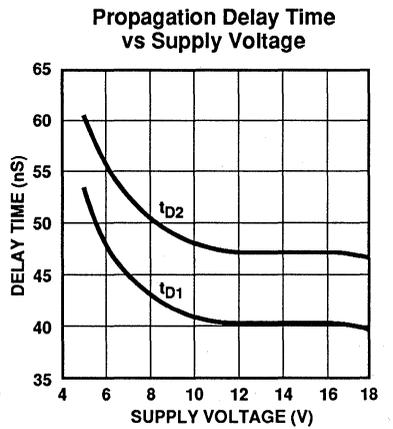
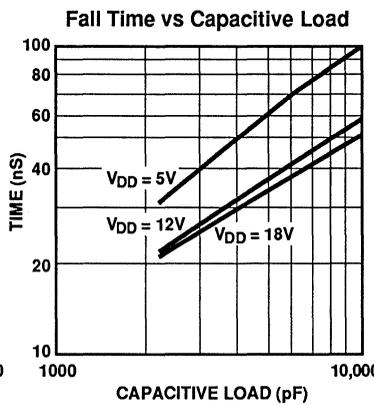
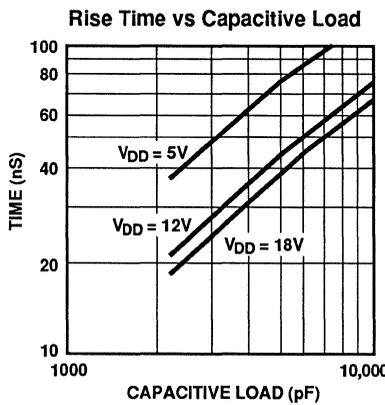
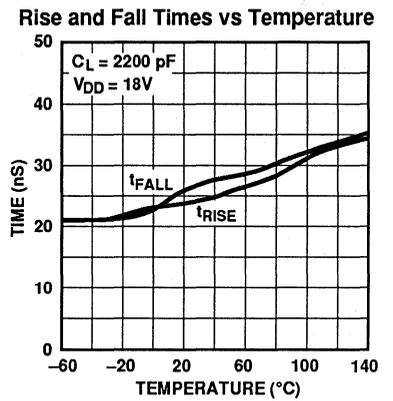
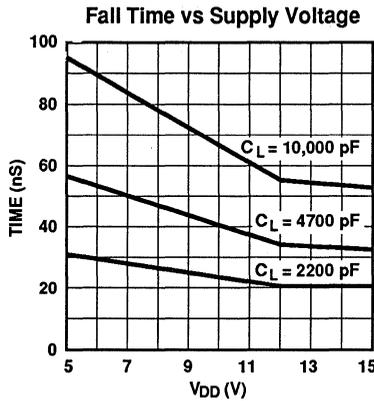
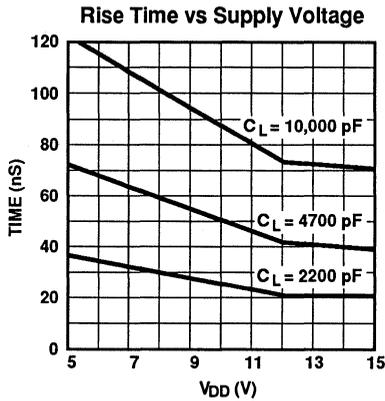


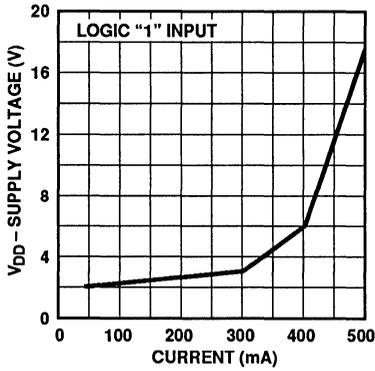
Figure 1. Switching Time Test Circuit

Typical Characteristic Curves

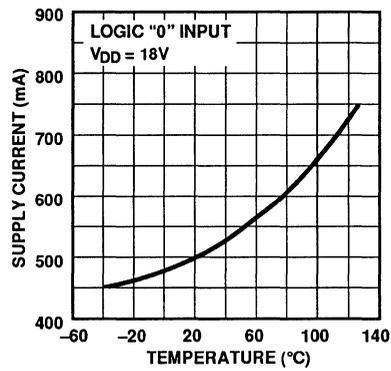


Typical Characteristic Curves (Cont.)

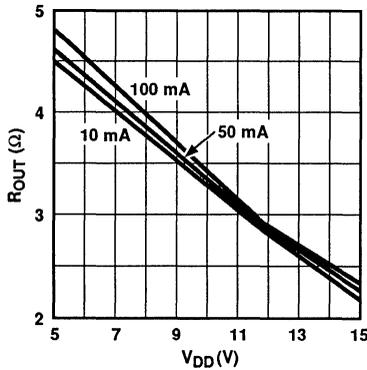
Quiescent Power Supply Voltage vs Supply Current



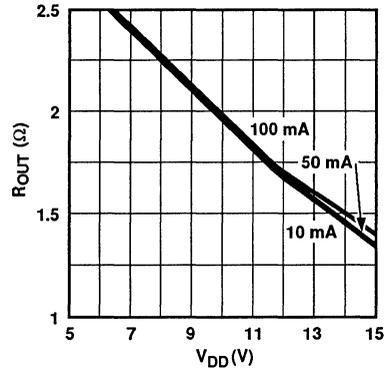
Quiescent Power Supply Current vs Temperature



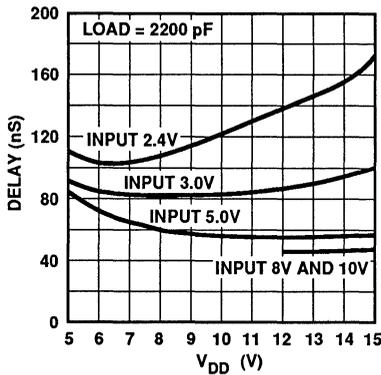
High-State Output Resistance



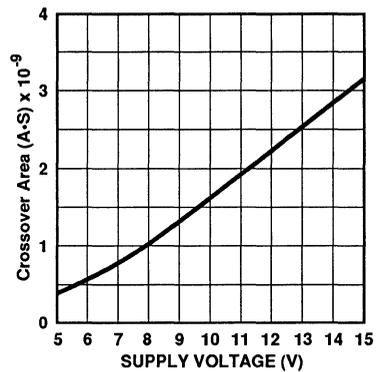
Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay



Total nA·S Crossover



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Applications Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 2500 pF load to 18 volts in 25 nS requires a 1.8 A current from the device power supply.

The MIC4420/4429 has double bonding on the supply pins, the ground pins and output pins. This serves to reduce parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (< 0.5 inch) should be used. A 1 μF low ESR film capacitor in parallel with two 0.1 μF low ESR ceramic capacitors, (such as AVX RAM GUARD®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4420/4429 demands careful PC board layout for best performance. Since the MIC4429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switch-

ing speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5 shows the feedback effect in detail. As the MIC4429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05 Ω of PC trace resistance can produce hundreds of millivolts at the MIC4429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4429 GND pins should, however, still be connected to power ground.

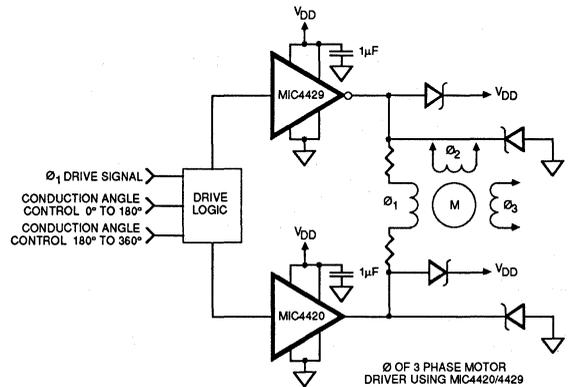


Figure 3. Direct Motor Drive

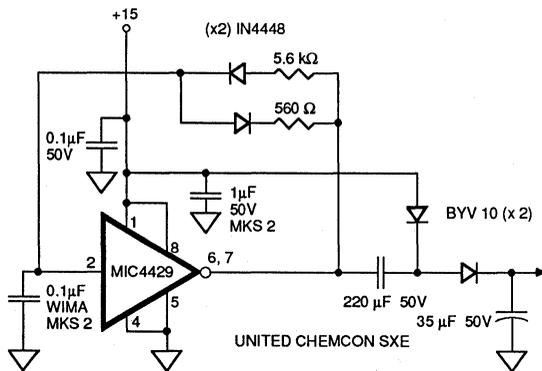
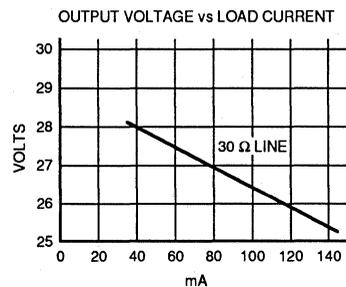


Figure 4. Self Contained Voltage Doubler



Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2 C V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F C (V^+_{S})^2$$

where:

F = Operating Frequency

C = Load Capacitance

V⁺_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I V_D (1-D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA; a logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V^+_{S} [D I_H + (1-D) I_L]$$

where:

I_H = quiescent current with input high

I_L = quiescent current with input low

D = fraction of time input is high (duty cycle)

V⁺_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V⁺_S to ground. The transition power dissipation is approximately:

$$P_T = F V^+_{S} (A \cdot S)$$

where (A·S) is a time-current factor derived from Figure 7.

Total power (P_D) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in Figure 7 in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency) to find Watts.

R_O = Output resistance of a driver in Ohms.

V⁺_S = Power supply voltage to the IC in Volts.

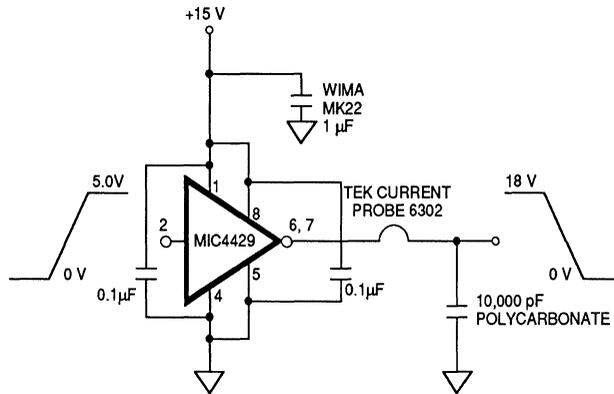


Figure 6. Peak Output Current Test Circuit

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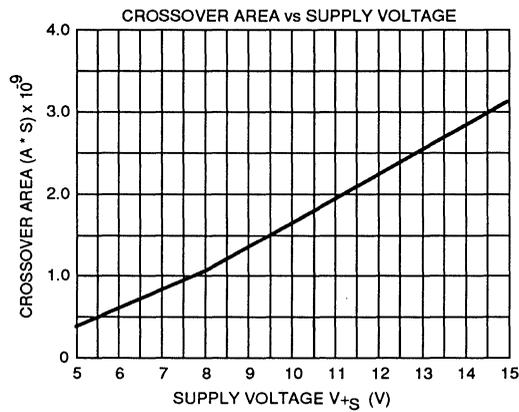


Figure 7. Total A · nS Crossover



MIC4423/4424/4425

3A Dual High Speed MOSFET Driver

General Description

The MIC4423/4424/4425 family of parts are CMOS buffer/drivers built using a highly reliable "tough" CMOS process. They are higher output current versions of the new MIC4426 family of buffer/drivers, which, in turn, are improved versions of the MIC426/427/428 family. All three families are pin-compatible. The MIC4423/24/25 drivers are capable of giving reliable service in far more demanding electrical environments than their antecedents. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking, of either polarity, occurs on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2kV of electrostatic discharge.

As a result, the MIC4423/24/25 series drivers are much easier to use, more flexible in operation, and much more forgiving than any other driver, CMOS or bipolar, currently available. Because they are fabricated in CMOS, they dissipate a minimum of power, and provide rail-to-rail voltage swings to better insure the logic state of any load they drive.

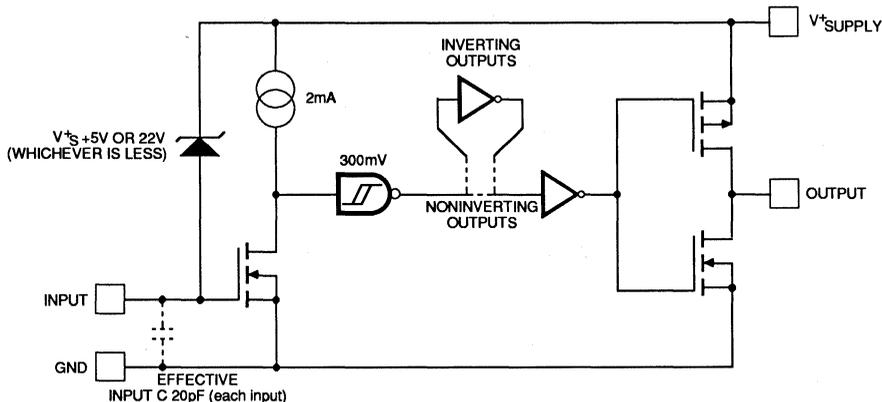
Although primarily intended for driving power MOSFETs, the 4423/4424/4426 series drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the MIC4423/24/25. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

Features

- Built using reliable, low power CMOS processes
- Latch-Up Protected: Withstands >500mA Reverse Current
- Logic Input Will Withstand Negative Swing Up to 5V
- ESD Protected 2 kV
- High Peak Output Current 3A Peak
- Wide Operating Range 4.5V to 18V
- High Capacitive Load Drive Capability 1800 pF in 25 nS
- Short Delay Times <40 nS Typ
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_S^+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
 - 3.5 mA with Logic 1 Input
 - 350 μ A with Logic 0 Input
- Low Output Impedance 3.5 Ω Typ.
- Output Voltage Swing to Within 25 mV of Ground or V_S^+
- Pin-Out Same as MIC426/427/428
- Available in Inverting, Non-Inverting, and Differential Configurations
- MIL-STD-883 Method 5004/5005 version available

As MOSFET drivers, the MIC4423/24/25 can easily switch 1000 pF gate capacitances in under 30 nS, and provide low enough impedances in both the ON and OFF states to assure that a MOSFET's intended state will not be affected even by large transients.

Functional Diagram



Ordering Information

Part Number	Temperature Range	Package
MIC4423CWM MIC4423BWM	0°C to +70°C -40°C to +85°C	16-Pin SO Wide
MIC4423CN MIC4423BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4423BJ MIC4423AJ MIC4423AJB	-25°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP
MIC4424CWM MIC4424BWM	0°C to +70°C -40°C to +85°C	16-Pin SO Wide
MIC4424CN MIC4424BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4424BJ MIC4424AJ MIC4424AJB	-25°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP
MIC4425CWM MIC4425BWM	0°C to +70°C -40°C to +85°C	16-Pin SO Wide
MIC4425CN MIC4425BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4425BJ MIC4425AJ MIC4425AJB	-25°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP

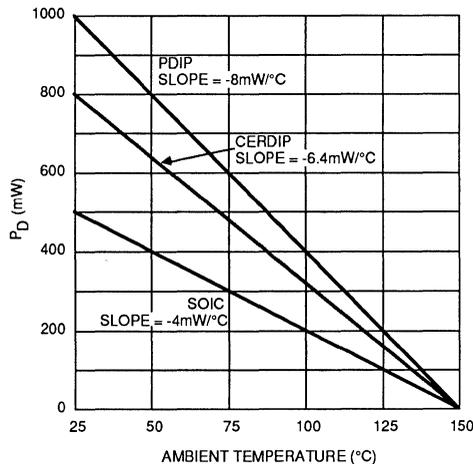
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**Absolute Maximum Ratings
(Notes 1, 2, and 3)**

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Supply Voltage	22 V
Maximum Chip Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (10 sec.)	300°C
Package Thermal Resistance	
CERDIP R _{θJ-A} (°C/W)	150
CERDIP R _{θJ-C} (°C/W)	50
PDIP R _{θJ-A} (°C/W)	125
PDIP R _{θJ-C} (°C/W)	42
SOIC R _{θJ-A} (°C/W)	250
SOIC R _{θJ-C} (°C/W)	75
Operating Temperature Range	
C Version	0°C to +70°C
B Version	-40°C to +85°C
A Version	-55°C to +125°C

Package Power Dissipation



MIC4423/4424/4425 Electrical Characteristics:Specifications measured at $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$-5 \leq V_{IN} \leq V_S^+$	-1		1	μA
OUTPUT						
V_{OH}	High Output Voltage		$V_S - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance HI State	$I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		2.8	5	Ω
R_O	Output Resistance LO State	$I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		3.5	5	Ω
I_{PK}	Peak Output Current			3		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1, $C_L = 1800\text{ pF}$		23	35	nS
T_F	Fall Time	Test Figure 1, $C_L = 1800\text{ pF}$		25	35	nS
T_{D1}	Delay Time	Test Figure 1, $C_L = 1800\text{ pF}$		33	75	nS
T_{D2}	Delay Time	Test Figure 1, $C_L = 1800\text{ pF}$		38	75	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)		1.5	2.5	mA
I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)		0.15	0.25	mA

MIC4426/4427/4428 Electrical Characteristics:Specifications measured over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$-5 \leq V_{IN} \leq V^+$	-10		10	μA
OUTPUT						
V_{OH}	High Output Voltage		$V_S - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V

MIC4426/4427/4428 Electrical Characteristics:

Specifications measured over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT						
R_O	Output Resistance, Output High	$V_{IN} = 0.8\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		3.7	8	Ω
R_O	Output Resistance, Output Low	$V_{IN} = 2.4\text{ V}$ $I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		4.3	8	Ω

SWITCHING TIME						
T_R	Rise Time	Test Figure 1, $C_L = 1800\text{ pF}$		28	60	nS
T_F	Fall Time	Test Figure 1, $C_L = 1800\text{ pF}$		32	60	nS
T_{D1}	Delay Time	Test Figure 1, $C_L = 1800\text{ pF}$		32	100	nS
T_{D2}	Delay Time	Test Figure 1, $C_L = 1800\text{ pF}$		38	100	nS

POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)		20	3.5	mA
I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)		0.20	0.3	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.

Note 2: Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.

Note 3: Switching times guaranteed by design.

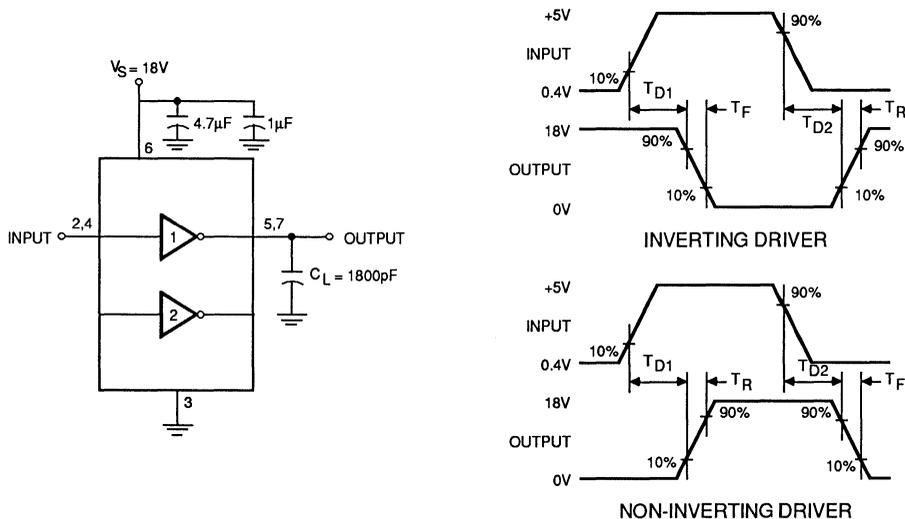
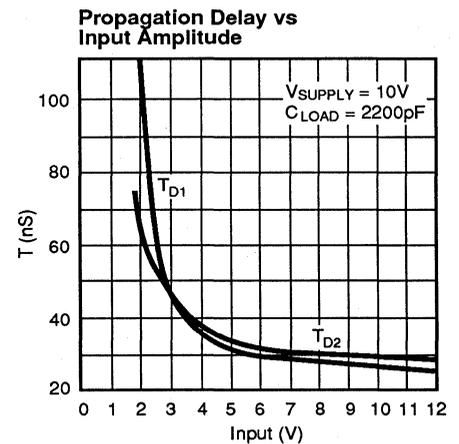
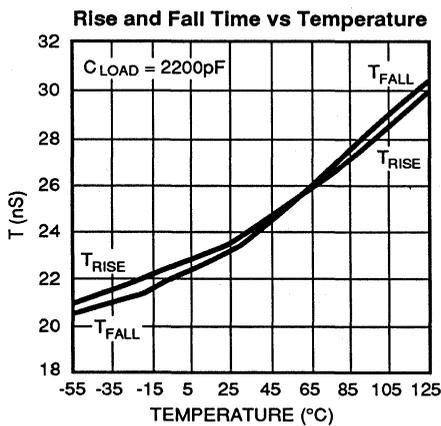
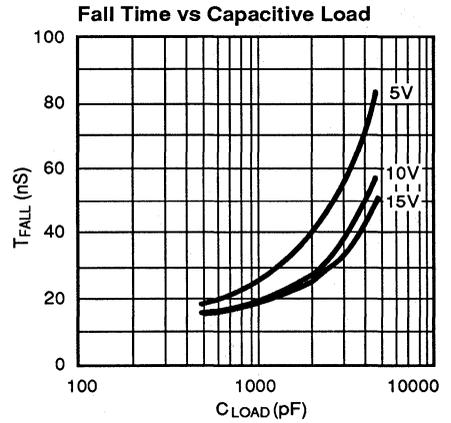
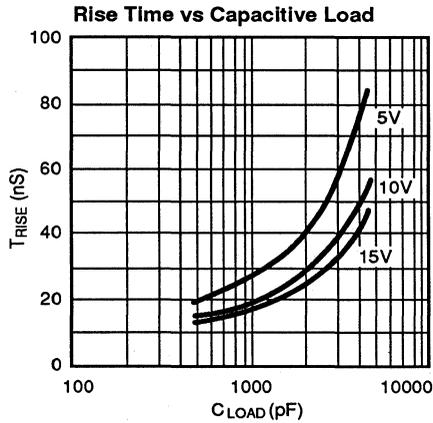
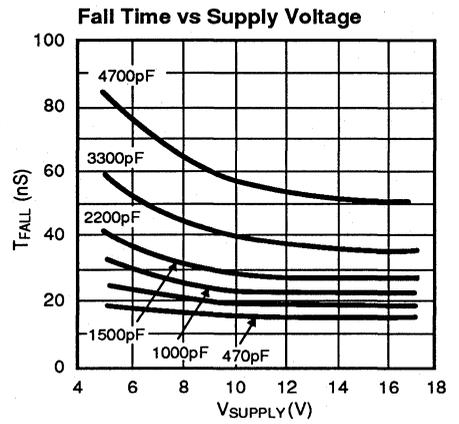
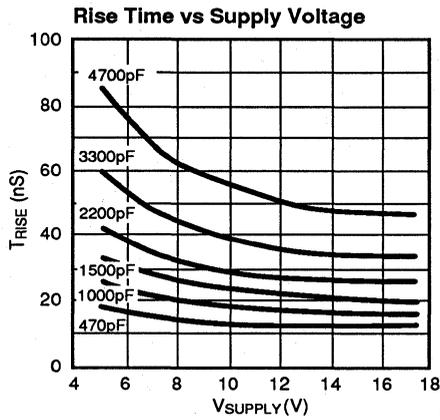
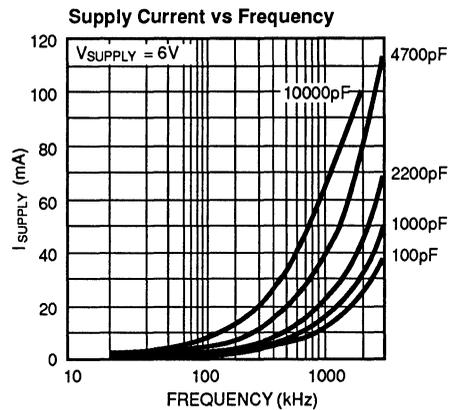
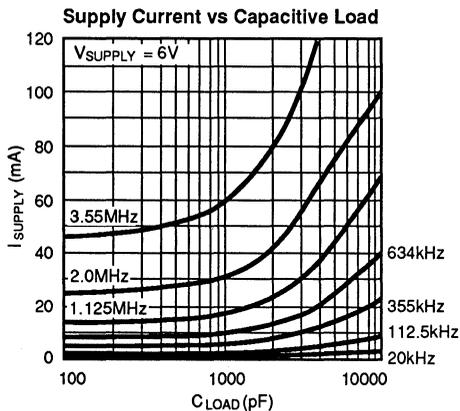
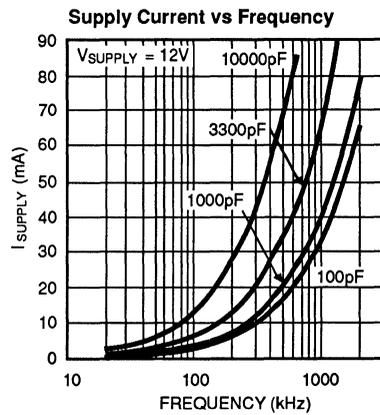
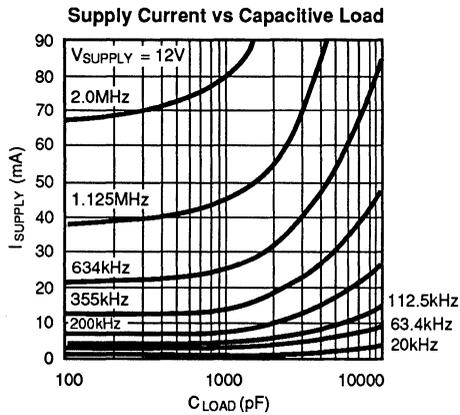
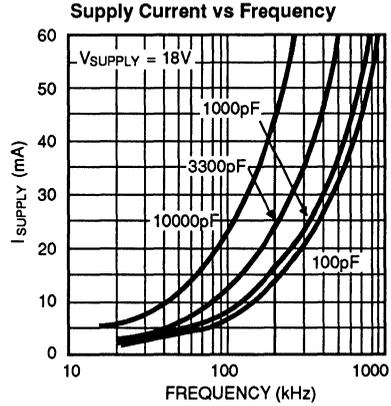
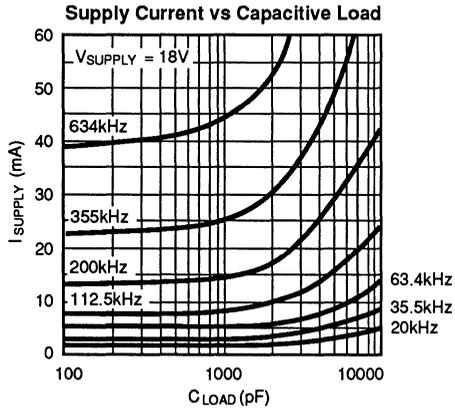


Figure 1. Switching Time Test Circuit

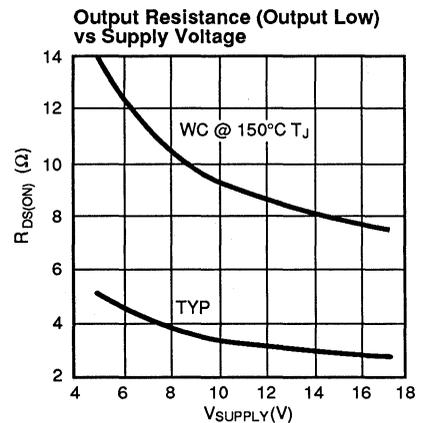
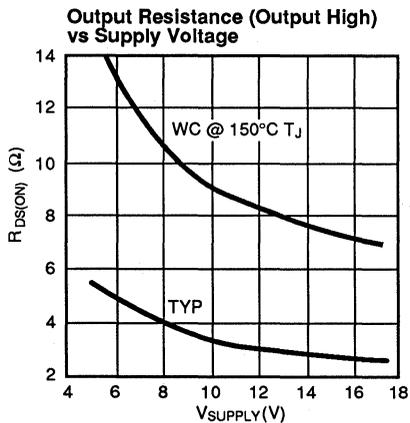
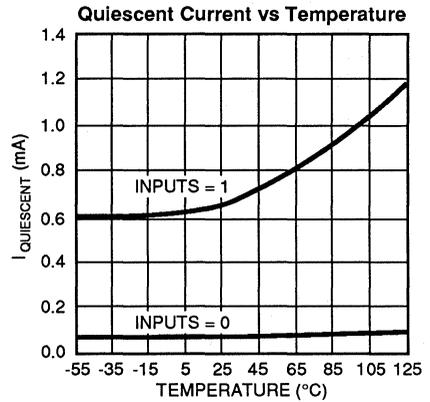
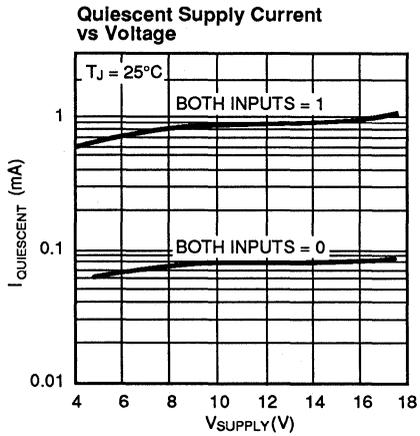
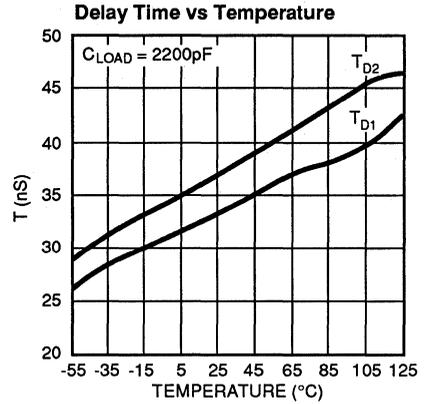
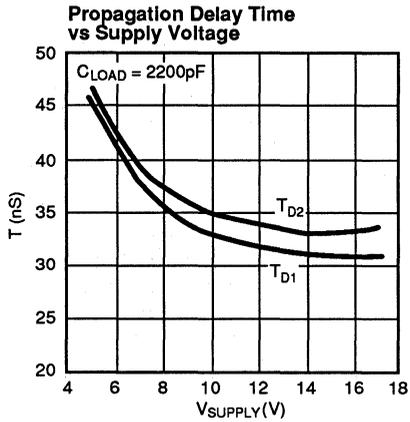
Typical Characteristic Curves



Typical Characteristic Curves (Continued)



Typical Characteristic Curves (Continued)



Application Information

Although the MIC4423/24/25 drivers have been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage which will, when attended to, provide better operation of the device:

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000pF from 0 to 15 volts in 20 nS requires a constant current of 1.5A. In practice, the charging current is not constant, and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have a **VERY** low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100X the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. NOTE PLEASE that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service. (in-house we use WIMA™ film capacitors and AVX Ramguard™ ceramics. Several other manufacturers of equivalent devices exist.) The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large Δl) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. Good bypassing practice is essential to proper operation of high speed driver ICs!

Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare

circumstances) it is also necessary to turn the load OFF. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

Best practice for a ground path is obviously a well laid out ground plane. However, this is not always practical, and a poorly-laid out ground plane can be worse than none. Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load are what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: The inductance of a 2cm long land, 1.59mm (.062") wide on a PCB with no ground plane is approximately 45nH. Assuming a dl/dt of 0.3A/nS (which will allow a current of 3A to flow after 10 nS, and is thus slightly slow for our purposes) a voltage of 13.5 Volts will develop along this land in response to our postulated ΔI . For a 1cm land, (approximately 15nH) 4.5 Volts is developed. Either way, anyone using TTL-level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59mm (.062") land of 2oz. Copper carrying 3A will be about 4mV/cm (10mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to turn the driver's load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the

twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e. minimize sharp bends, or narrowings in the land, as these will cause ringing. For a rough estimate, on a 1.59mm (.062") thick G-10 PCB a pair of opposing lands each 2.36mm (.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a .787mm (.031") thick board. For accurate impedance matching with a MIC4423/24/25 driver, on a 1.59mm (.062") board a land width of 42.75mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 3.18mm (.125") would be required on a 1.59mm (.062") board.

While one could, in theory, use matching transformers at both ends of a piece of coax, or a dozen or so matched pieces of coax in parallel for transmission between a driver and a distant load. In practice, in situations where the absolute minimum in delay between the driver and the load must be obtained, it is generally easiest to relocate the driver as close as possible to the load (using adequate power supply bypassing, of course) and then connect the input of the driver back to the logic using a single piece of coax.

Driving At Controlled Rates

Occasionally there are situations where a controlled rise or fall time which may be considerably longer than the normal rise or fall time of the driver's output is desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding and PCB layout, and then reduce the switching speed of the load (NOT the driver) by adding a noninductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the schmitt-trigger action of the driver's input it is not possible to slow the rate of rise (or fall) of the driver's input signal to achieve slowing of the output.

Input Stage

The input stage of the MIC4423/24/25 consists of a single-MOSFET class A stage with an input capacitance of ≤ 38 pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a -2mA current source. Thus, the quiescent current drawn by the driver varies, depending on the logic state of the input.

Following the input stage is a buffer stage which provides ~ 300 mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used or when noise is present on the input. Input voltage switching threshold is -1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4423/24/25 drivers can also be driven directly by the SG1524/25/26/27, TL494/95, TL594/95, NE5560/61/62/68, TSC170, MIC18HC42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MIC4423/24/25, in addition to providing 2kV or more of ESD protection, also works to prevent latchup or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled OFF and ON. The MIC4423/24/25 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. T_{D2} , for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or V_{CC} may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several Amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when

driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs Frequency and Supply Current vs Load characteristic curves furnished with this data sheet aid in estimating power dissipation in the driver. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CerDIP package, from the datasheet, is 150°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 800mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

- I = the current drawn by the load
- R_O = the output resistance of the driver when the output is high, at the power supply voltage used (See characteristic curves)
- D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2 C V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F C (V^+_S)^2$$

where:

- F = Operating Frequency
- C = Load Capacitance
- V^+_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the

part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I V_D (1-D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q , as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of $\leq 0.2\text{mA}$; a logic high will result in a current drain of $\leq 2.0\text{mA}$. Quiescent power can therefore be found from:

$$P_Q = V^+_S [D I_H + (1-D) I_L]$$

where:

- I_H = quiescent current with input high
- I_L = quiescent current with input low
- D = fraction of time input is high (duty cycle)
- V^+_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V^+_S to ground. The transition power dissipation is approximately:

$$P_T = F V^+_S (A \cdot S)$$

where $(A \cdot S)$ is a time-current factor derived from the graph on page 12.

Total power (P_D) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term.

EXAMPLE 1: A MIC4423 operating on a 12V supply driving two capacitive loads of 3000pF each, operating at 250kHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First calculate load power loss:

$$\begin{aligned} P_L &= F \times C \times (V^+_S)^2 \\ P_L &= 250,000 \times (3 \times 10^{-6} + 3 \times 10^{-6}) \times 12^2 \\ &= 0.2160\text{W} \end{aligned}$$

Then transition power loss:

$$P_T = F \times V^+_{S} \times (A \cdot S) \\ = 250,000 \cdot 12 \cdot 2.5 \times 10^{-8} = 0.0750W$$

Then quiescent power loss:

$$P_Q = V^+_{S} \times [D \times I_H + (1-D) \times I_L] \\ = 12 \times [(0.5 \times 0.0035) + (0.5 \times 0.0003)] \\ = 0.0228W$$

Total power dissipation, then, is:

$$P_D = 0.2160 + 0.0750 + 0.0228 \\ = 0.3138W$$

Assuming a plastic package, with an $R_{\theta J-A}$ of 170°C/W, this will result in the junction running at:

$$0.3138 \times 170 = 53.3^\circ C$$

above ambient, which, given a maximum ambient temperature of 60°C, will result in a maximum junction temperature of 113.3°C.

EXAMPLE 2: A MIC4424 operating on a 15V input, with one driver driving a 50Ω resistive load at 1MHz, with a duty cycle of 67%, and the other driver quiescent, in a maximum ambient temperature of 40°C:

$$P_L = I^2 \times R_O \times D$$

First, I_O must be determined.

$$I_O = V^+_{S} / (R_O + R_{LOAD})$$

Given R_O from the characteristic curves then,

$$I_O = 15 / (6.3 + 50)$$

$$I_O = 0.2664A$$

and:

$$P_L = 0.2664 \times 6.3 \times 0.67 \\ = 0.2996W$$

$$P_T = F \times V^+_{S} \times (A \cdot S) / 2$$

(because only one side is operating)

$$= (1,000,000 \times 15 \times 3.3 \times 10^{-8}) / 2 \\ = 0.2475 W$$

and:

$$P_Q = 15 \times [(0.67 \times .00125) + (0.33 \times .000125) + \\ (1 \times 0.000125)]$$

(this assumes that the unused side of the driver has its input grounded, which is more efficient)

$$= 0.0150W$$

then:

$$P_D = 0.2996 + 0.2475 + 0.0150 \\ = 0.5621W$$

In a ceramic package with an $R_{\theta J-A}$ of 150°C/W, this amount of power results in a junction temperature given the maximum

40°C ambient of:

$$(0.5621 \times 150) + 40 = 124.3^\circ C$$

The actual junction temperature will be lower than calculated both because duty cycle is less than 100% and because the graph lists $R_{DS(on)}$ at a T_J of 150°C and the $R_{DS(on)}$ at 125°C T_J will be somewhat lower.

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver in Hertz

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

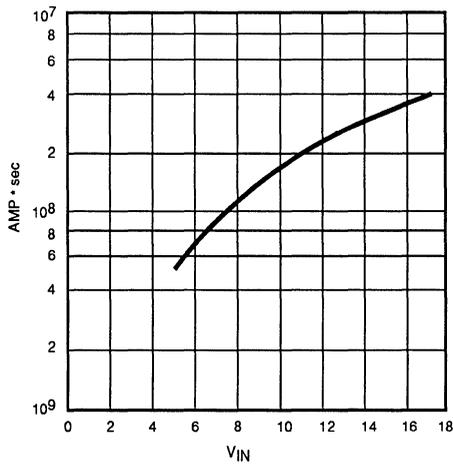
P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts. NOTE: The "shoot-through" current from a dual transition (once up, once down) for both drivers is stated in the graph on page 12 in ampere-nanoseconds. This figure must be multiplied by the number of repetitions per second (frequency to find Watts).

R_O = Output resistance of a driver in Ohms.

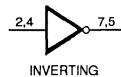
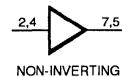
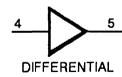
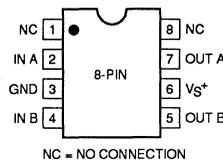
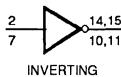
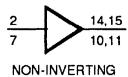
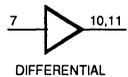
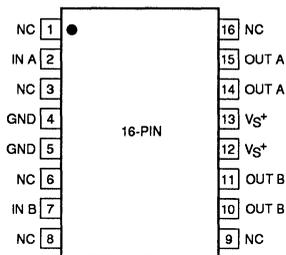
V^+_{S} = Power supply voltage to the IC in Volts.

Crossover Energy Loss



NOTE: THE VALUES ON THIS GRAPH REPRESENT THE LOSS SEEN BY BOTH DRIVERS IN A PACKAGE DURING ONE COMPLETE CYCLE. FOR A SINGLE DRIVER DIVIDE THE STATED VALUES BY 2. FOR A SINGLE TRANSITION OF A SINGLE DRIVER, DIVIDE THE STATED VALUE BY 4.

Pin Configuration





General Description

The MIC4426/4427/4428 family of buffer/drivers are CMOS devices built using a new, highly reliable CMOS process. They are improved versions of the MIC426/427/ 428 family of buffer/drivers (with which they are pin compatible) and are capable of giving reliable service in far more demanding electrical environments: They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking, of either polarity, occurs on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2kV of electrostatic discharge.

As a result, the MIC4426/27/28 series drivers are much easier to use, more flexible in operation, and much more forgiving than any other driver, CMOS or bipolar, currently available. Because they are fabricated in CMOS, they dissipate a minimum of power, and provide rail-to-rail voltage swings to better insure the logic state of any load they are driving.

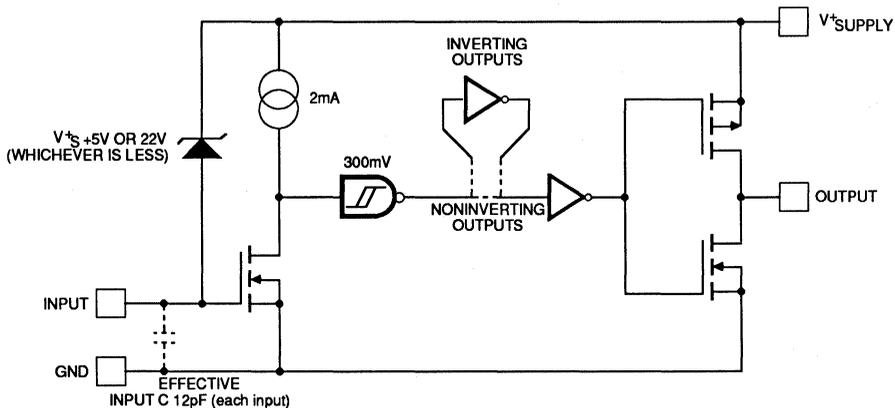
Although primarily intended for driving power MOSFETs, the 4426/4427/4428 series drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the MIC4426/27/28. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

Features

- Built using reliable, low power CMOS processes
- Latch-Up Protected: Withstands >500 mA Reverse Current
- Logic Input Will Withstand Negative Swing Up to 5V
- ESD Protected 2 kV
- High Peak Output Current 1.5A Peak
- Wide Operating Range 4.5V to 18V
- High Capacitive Load Drive Capability 1000 pF in 25 nS
- Short Delay Times <40 nS Typ
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_s^+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
 - 4 mA with Logic 1 Input
 - 400 μ A with Logic 0 Input
- Low Output Impedance 7 Ω
- Output Voltage Swing to Within 25 mV of Ground or V_s^+
- Pin-Out Same as MIC426/427/428
- Available in Inverting, Non-Inverting, and Differential Configurations
- MIL-STD-883 Method 5004/5005 version available

As MOSFET drivers, the MIC4426/27/28 can easily switch 1000 pF gate capacitances in under 30nS, and provide low enough impedances in both the ON and OFF states to assure that a MOSFET's intended state will not be affected even by large transients.

Functional Diagram



Ordering Information

Part Number	Temperature Range	Package
MIC4426CM MIC4426BM	0°C to +70°C -40°C to +85°C	8-Pin SOIC
MIC4426CN MIC4426BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4426BJ MIC4426AJ MIC4426AJB	-40°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP
MIC4427CM MIC4427BM	0°C to +70°C -40°C to +85°C	8-Pin SOIC
MIC4427CN MIC4427BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4427BJ MIC4427AJ MIC4427AJB	-40°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP
MIC4428CM MIC4428BM	0°C to +70°C -40°C to +85°C	8-Pin SOIC
MIC4428CN MIC4428 BN	0°C to +70°C -40°C to +85°C	8-Pin Plastic DIP
MIC4428BJ MIC4428AJ MIC4428AJB	-40°C to +85°C -55°C to +125°C -55°C to +125°C	8-Pin CerDIP
MIC4426CY MIC4426AY MIC4427CY MIC4427AY MIC4428CY MIC4428AY	0°C to +70°C -55°C to +125°C 0°C to +70°C -55°C to +125°C 0°C to +70°C -55°C to +125°C	Die Die Die Die Die Die

2

Absolute Maximum Ratings (Notes 1 and 2)

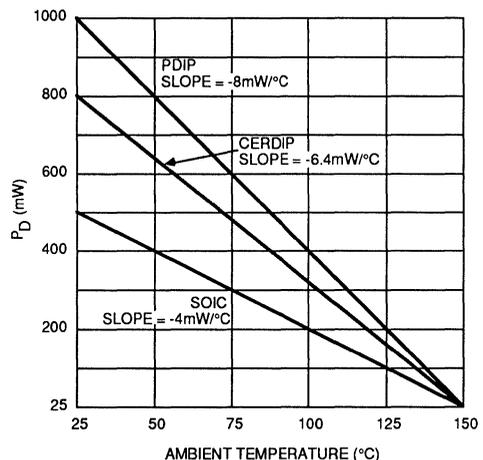
If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Supply Voltage	22 V
Maximum Chip Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (10 sec.)	300°C
Package Thermal Resistance	
CERDIP R _{θJ-A} (°C/W)	150
CERDIP R _{θJ-C} (°C/W)	50
PDIP R _{θJ-A} (°C/W)	125
PDIP R _{θJ-C} (°C/W)	42
SOIC R _{θJ-A} (°C/W)	250
SOIC R _{θJ-C} (°C/W)	75

Operating Temperature Range

C Version	0°C to +70°C
B Version	-40°C to +85°C
A Version	-55°C to +125°C

Package Power Dissipation



MIC4426/4427/4428 Electrical Characteristics:Specifications measured at $T_A = 25^\circ\text{C}$ with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-1		1	μA
OUTPUT						
V_{OH}	High Output Voltage		$V_S - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	$I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		7	10	Ω
I_{PK}	Peak Output Current			1.5		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1		25	30	nS
T_F	Fall Time	Test Figure 1		25	30	nS
T_{D1}	Delay Time	Test Figure 1			30	nS
T_{D2}	Delay Time	Test Figure 1			50	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			4.5	mA
I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.4	mA

MIC4426/4427/4428 Electrical Characteristics:Specifications measured over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	-1		1	μA
OUTPUT						
V_{OH}	High Output Voltage		$V_S - 0.025$			V
V_{OL}	Low Output Voltage				0.025	V
R_O	Output Resistance	$I_{OUT} = 10\text{ mA}$, $V_S = 18\text{ V}$		9	12	Ω

MIC4426/4427/4428 Electrical Characteristics:

Specifications measured over operating temperature range with $4.5\text{ V} \leq V_S \leq 18\text{ V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT						
I_{PK}	Peak Output Current			1.5		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
T_R	Rise Time	Test Figure 1			40	nS
T_F	Fall Time	Test Figure 1			40	nS
T_{D1}	Delay Time	Test Figure 1			40	nS
T_{D2}	Delay Time	Test Figure 1			60	nS
POWER SUPPLY						
I_S	Power Supply Current	$V_{IN} = 3.0\text{ V}$ (Both Inputs)			8	mA
I_S	Power Supply Current	$V_{IN} = 0.0\text{ V}$ (Both Inputs)			0.6	mA

Note 1: Functional operation above the absolute maximum stress ratings is not implied.

Note 2: Static Sensitive device (above 2kV). Store only in conductive containers. Handling personnel and equipment should be grounded to prevent static damage.

2

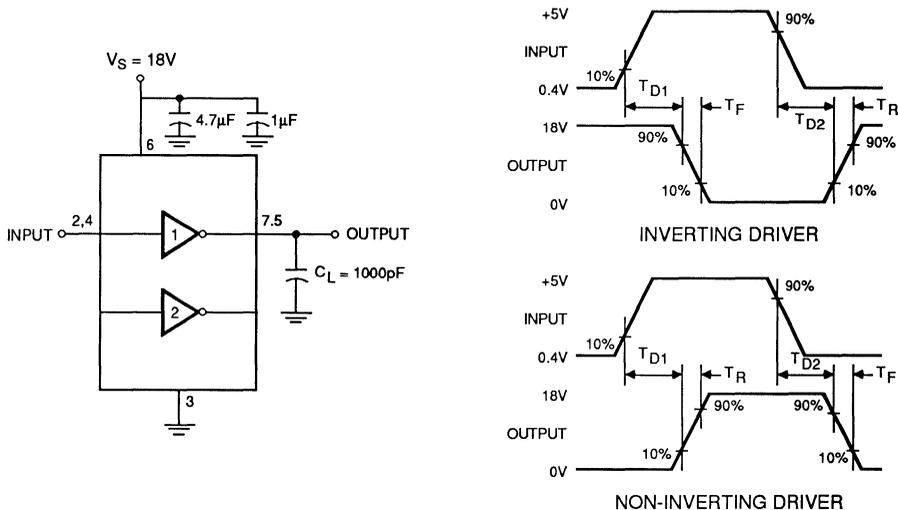
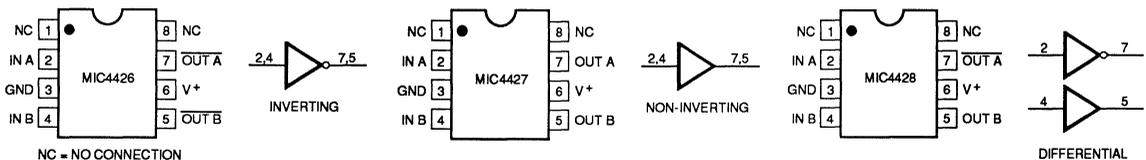
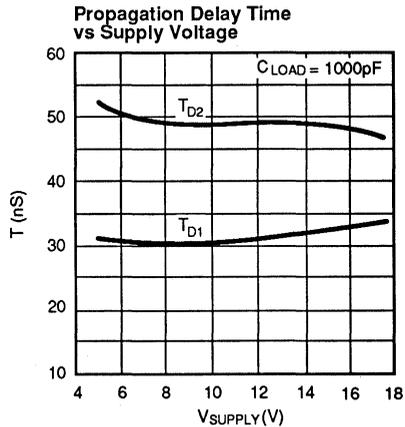
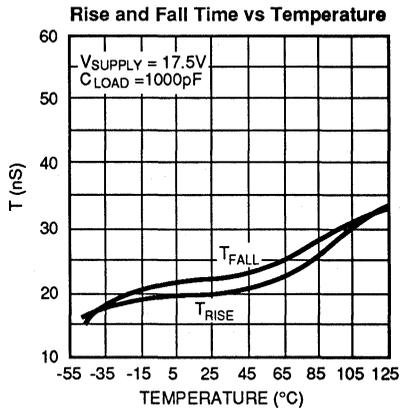
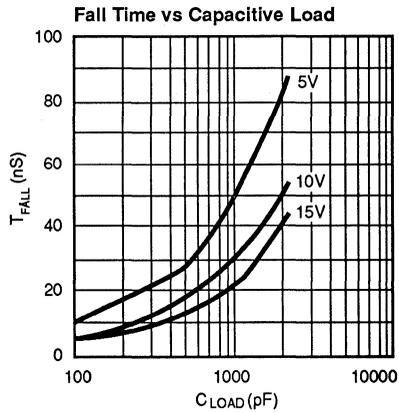
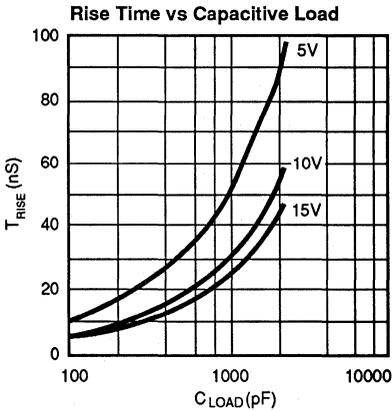
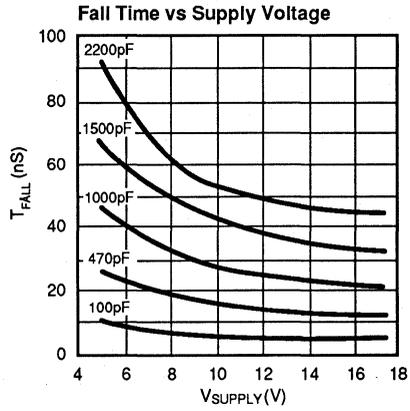
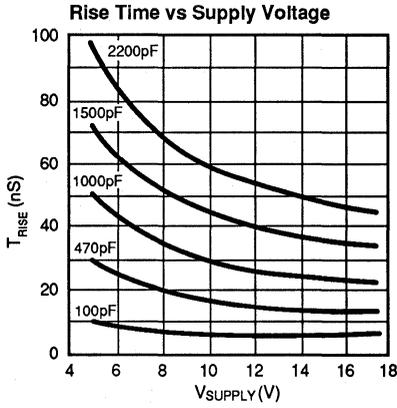


Figure 1. Switching Time Test Circuit

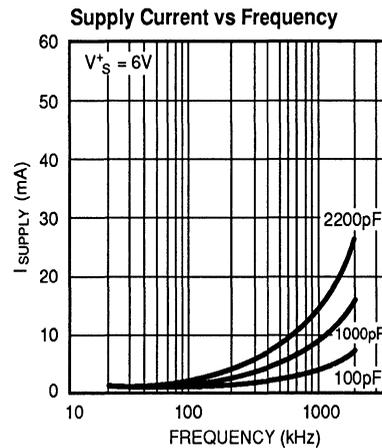
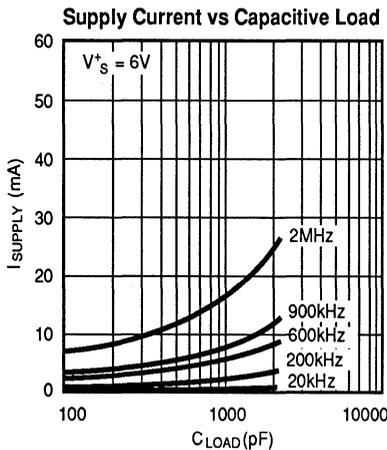
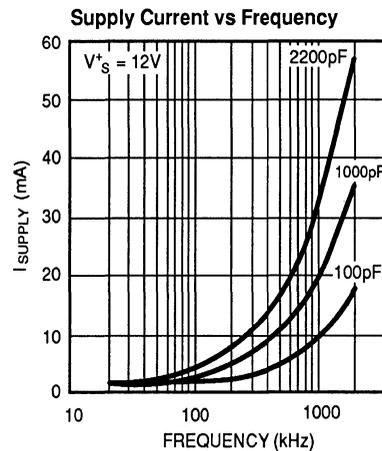
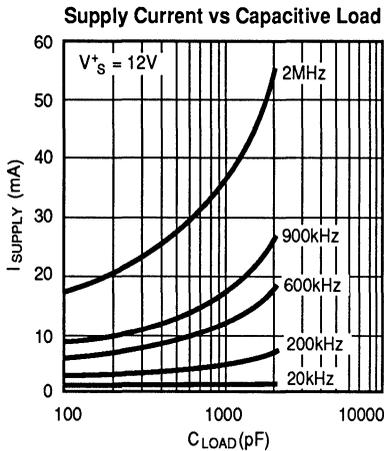
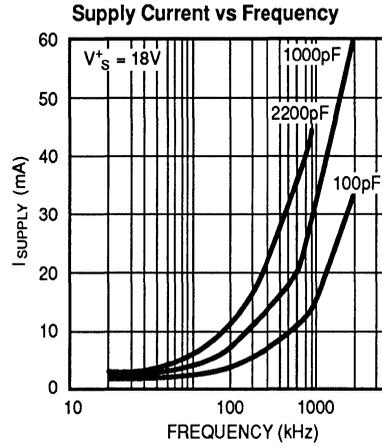
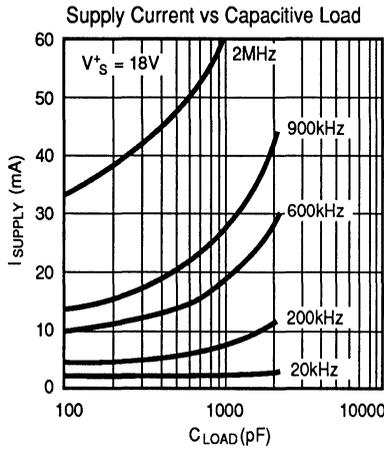
Pin Configuration



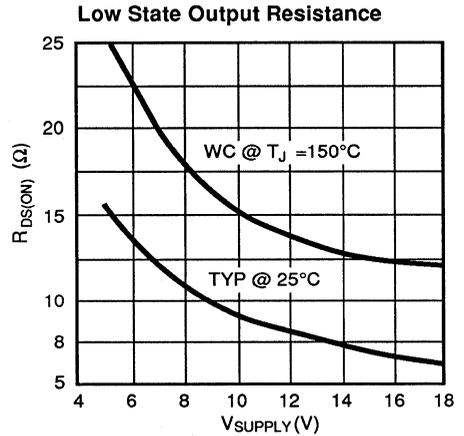
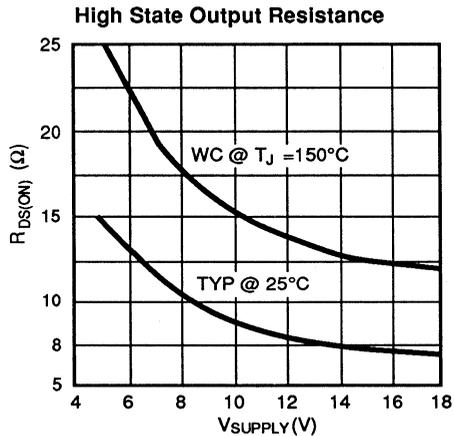
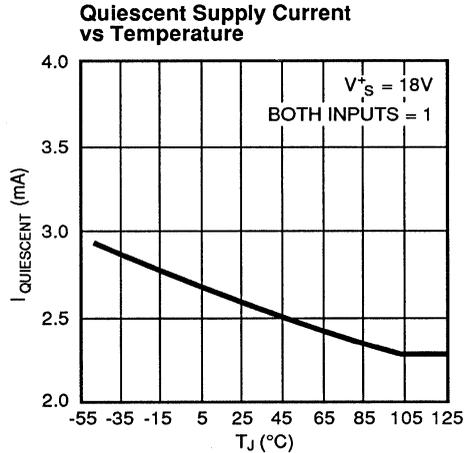
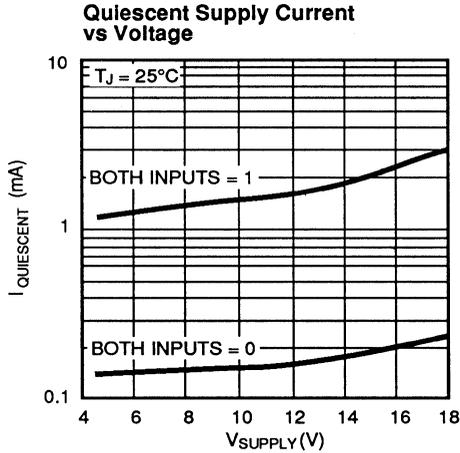
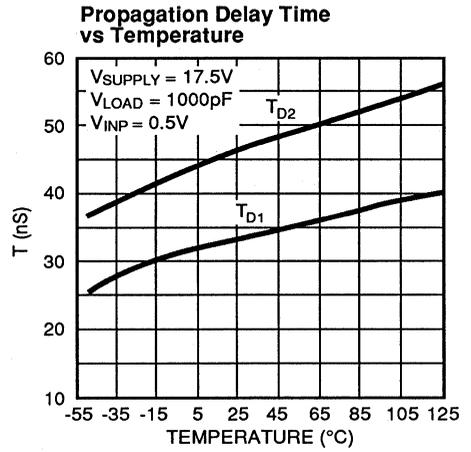
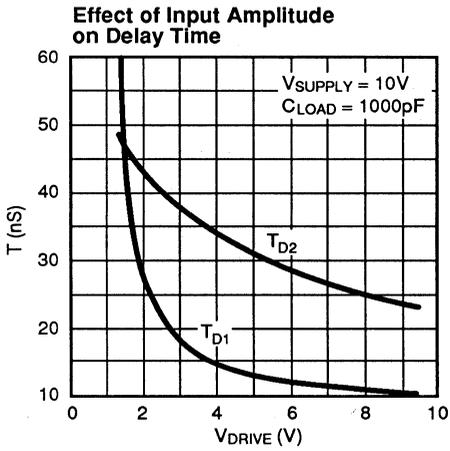
Typical Characteristic Curves



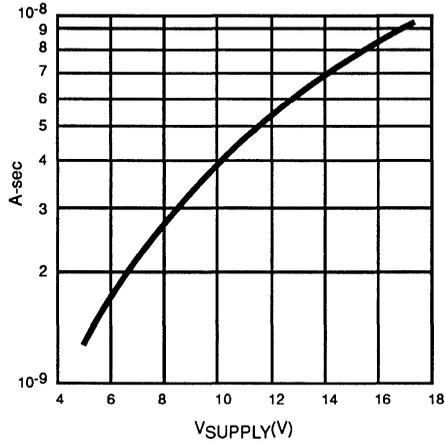
Typical Characteristic Curves (Continued)



Typical Characteristic Curves (Continued)



Crossover Energy Loss



Note 1: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.



MIC4465/4466/4467/4468/4469

Power Logic CMOS Quad Drivers

General Description

The MIC4465/6/7/8/9 family of 4-output CMOS buffer/drivers is an expansion from the earlier single- and dual-output drivers, to which they are functionally closely related. Because package pin count permitted it, each driver has been equipped with a 2-input logic gate for added flexibility. Placing four high-power drivers in a single package also improves system reliability and reduces total system cost. In some applications, one of these drivers can replace not only two packages of single-input drivers, but some of the associated logic as well.

Although primarily intended for driving power MOSFETs, and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive), which requires a high-efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with MIC446X series drivers. The only limitation

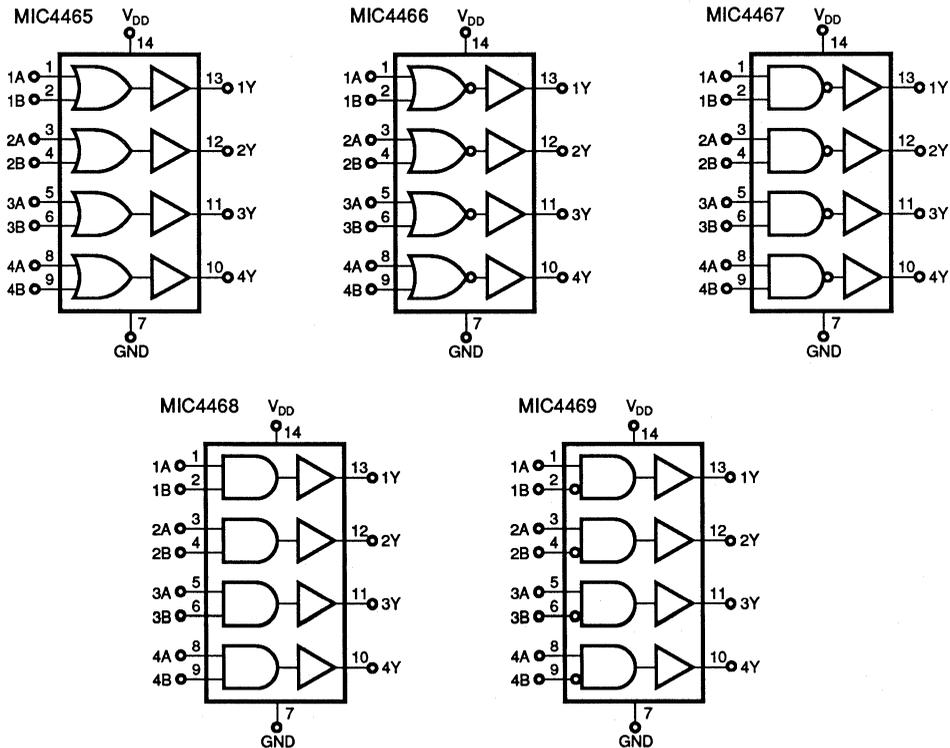
Features

- Built using reliable, low power CMOS processes
- Latchproof! Withstands 500 mA Inductive Kickback
- 5 Input Logic Choices
- Symmetrical Rise and Fall Times25 nS
- Short, Equal Delay Times75 nS
- High Peak Output Current1.2A
- Wide Operating Range 4.5 to 18V
- Inputs = Logic 1 for Any Input From 2.4V to V_{DD}
- 2 kV ESD Protection on All Pins

Applications

- General-Purpose CMOS Logic Buffer
- Driving All 4 MOSFETs in an H-Bridge
- Direct Small-Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin-Switching Network Driver

Logic Diagrams



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage	22V
Input Voltage	(GND – 5V) to (V _{DD} + 0.3V)
Maximum Chip Temperature	
Operating	150°C
Storage	–65° to +150°C
Maximum Load Temperature (10 sec, for soldering)	300°C
Operating Ambient Temperature	
C Version	0° to +70°C
B Version	–40° to +85°C
A Version	–55° to +125°C
Power Dissipation	
P Package (14-Pin Plastic DIP)	1.5W
WM Package (16-Pin Wide SOIC)	1W
J Package (14-Pin CerDIP)	1.25W
L Package (20-Pin LCC)	1W

Package Thermal Resistance

P Package (14-Pin Plastic DIP)	R _{θJ-A}	12 mW/°C
	R _{θJ-C}	20 mW/°C
WM Package (16-Pin Wide SOIC)	R _{θJ-A}	8 mW/°C
	R _{θJ-C}	31 mW/°C
J Package (14-Pin CerDIP)	R _{θJ-A}	10 mW/°C
	R _{θJ-C}	45 mW/°C
L Package (20-Pin LCC)	R _{θJ-A}	8 mW/°C
	R _{θJ-C}	40 mW/°C

Electrical Characteristics: Measured at T_A = 25°C with 4.5 V ≤ V_{DD} ≤ 18 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V _{IH}	Logic 1 Input Voltage		2.4			V
V _{IL}	Logic 0 Input Voltage				0.8	V
I _{IN}	Input Current	0 ≤ V _{IN} ≤ V _{DD}	–1		1	μA
OUTPUT						
V _{OH}	High Output Voltage	I _{LOAD} = 10 mA	V _{DD} –0.15			V
V _{OL}	Low Output Voltage	I _{LOAD} = 10 mA			0.15	V
R _O	Output Resistance	I _{OUT} = 10 mA, V _{DD} = 18V		10	15	Ω
I _{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current		>500			mA
SWITCHING TIME						
t _R	Rise Time	Test Figure 1			25	nS
t _F	Fall Time	Test Figure 1			25	nS
t _{D1}	Delay Time	Test Figure 1			75	nS
t _{D2}	Delay Time	Test Figure 1			75	nS
POWER SUPPLY						
I _S	Power Supply Current Supply				4	mA

Electrical Characteristics:

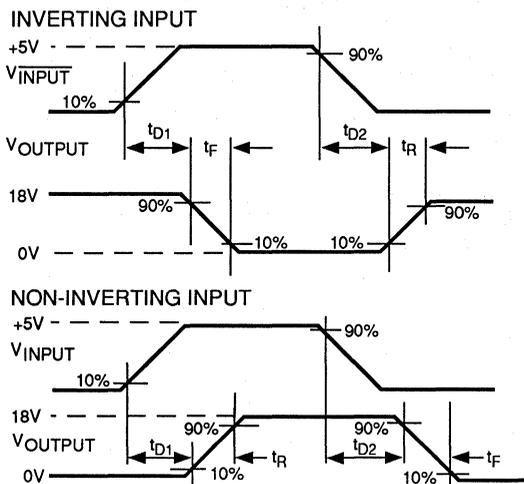
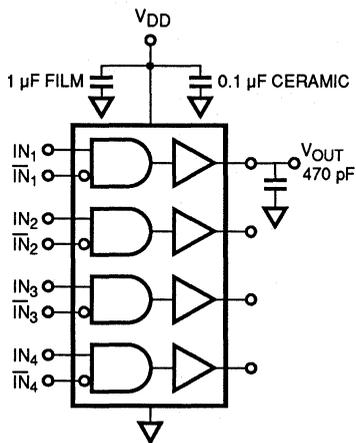
Measured over operating temperature range with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT						
V_{IH}	Logic 1 Input Voltage		2.4			V
V_{IL}	Logic 0 Input Voltage				0.8	V
I_{IN}	Input Current	$0 \leq V_{IN} \leq V_{DD}$	-1		1	μA
OUTPUT						
V_{OH}	High Output Voltage	$I_{LOAD} = 10\text{ mA}$	$V_{DD}-0.3$			V
V_{OL}	Low Output Voltage	$I_{LOAD} = 10\text{ mA}$			0.3	V
R_O	Output Resistance	$I_{OUT} = 10\text{ mA}, V_{DD} = 18\text{V}$		20	30	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current		500			mA
SWITCHING TIME						
t_R	Rise Time	Test Figure 1			50	nS
t_F	Fall Time	Test Figure 1			50	nS
t_{D1}	Delay Time	Test Figure 1			100	nS
t_{D2}	Delay Time	Test Figure 1			100	nS
POWER SUPPLY						
I_S	Power Supply Current Supply				8	mA

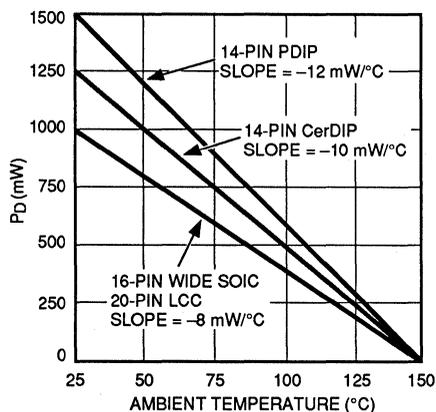
NOTE 1: Functional operation above the absolute maximum stress ratings is not implied.

NOTE 2: Static sensitive device (above 2kV). Store only in conductive containers. Handling personnel and equipment should be grounded to prevent static damage.

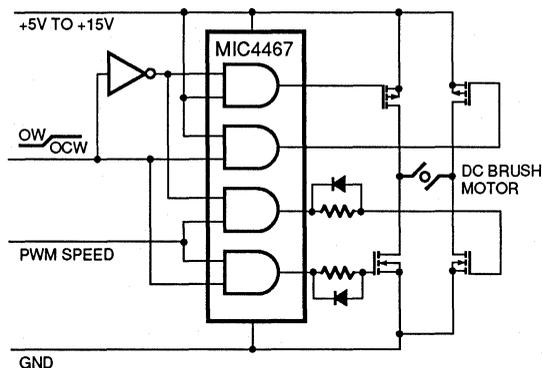
Test Figure 1



Package Power Dissipation



Quad Driver Drives H Bridge to Control Motor Speed and Direction



General Description

The MIC5010 is the full-featured member of the Micrel MIC5010X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The MIC5010 is compatible with standard or current-sensing power FETs in both high- and low-side driver topologies.

The MIC5010 charges a 1 nF load in 60 μ S typical and protects the MOSFET from over-current conditions. Faster switching is achieved by adding two 1 nF charge pump capacitors. The current sense trip point is fully programmable and a dynamic threshold allows high in-rush current loads to be started. A fault pin indicates when the MIC5010 has turned off the FET due to excessive current.

Other members of the Micrel predriver family include the MIC5011 minimum parts count 8 pin predriver, MIC5012 dual predriver, and MIC5013 protected 8 pin predriver.

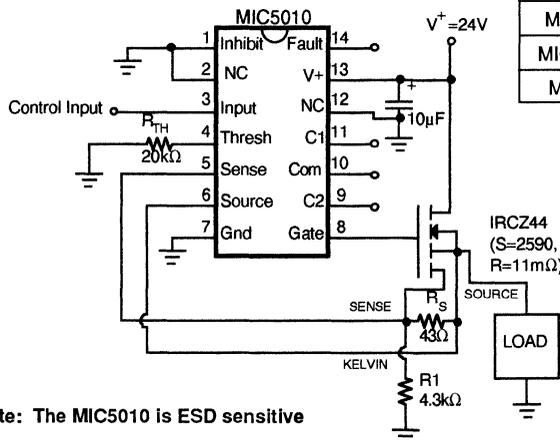
Features

- 7V-32V operation
- Less than 1 μ A standby current in the 'off' state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal zener clamp for gate protection
- 25 μ S typical turn-on time to 50% gate overdrive
- Programmable over-current sensing
- Dynamic current threshold for high in-rush loads
- Fault output pin indicates current faults
- Implements high- or low-side switches

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching
- Motion control

Typical Application



Note: The MIC5010 is ESD sensitive

Figure 1. High-Side Driver with Current-Sensing MOSFET

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC5010BN	-40°C to +85°C	14-pin Plastic DIP
MIC5010BJ	-40°C to +85°C	14-pin Ceramic DIP
MIC5010BM	-40°C to +85°C	14-pin SOIC
MIC5010AJ	-55°C to +125°C	14-pin Ceramic DIP
MIC5010AJB	-55°C to +125°C	14-pin Ceramic DIP
MIC5010B	-40°C to +85°C	Die

$$R_S = \frac{SR(V_{TRIP} + 100mV)}{R_L I_L - (V_{TRIP} + 100mV)}$$

$$R1 = \frac{V^+ SRR_S}{100mV (SR + R_S)}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 30A \text{ (trip current)}$$

$$V_{TRIP} = 100mV$$

Protected under one or more of the following Micrel patents: patent #4,951,101; patent # 4,914,546

Absolute Maximum Ratings (Note 1, 2)

Inhibit Voltage, Pin 1	-1V to V+
Input Voltage, Pin 3	-10V to V+
Threshold Voltage, Pin 4	-0.5 to +5V
Sense Voltage, Pin 5	-10V to V+
Source Voltage, Pin 6	-10V to V+
Current into Pin 6	50 mA
Gate Voltage, Pin 8	-1V to 50V
Supply Voltage (V+), Pin 13	-0.5V to 36V
Fault Output Current, Pin 14	-1 mA to +1 mA
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Power Dissipation	1.56W
θ_{JA} (Plastic DIP)	80 °C/W
θ_{JA} (Ceramic DIP)	105°C/W
θ_{JA} (SOIC)	115°C/W
Ambient Temperature: B version	-40°C to +85°C
Ambient Temperature: A version	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature	260°C
(Soldering, 10 seconds)	
Supply Voltage (V+), Pin 13	7V to 32V high side 7V to 15V low side

Electrical Characteristics (Note 3) Test circuit, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V^+=15\text{V}$, $V_1=0\text{V}$, $I_4=I_5=I_{14}=0$, all switches open, unless otherwise specified.

Parameter	Conditions		Min	Typ	Max	Units	
Supply Current, I13	V+=32V	V _{IN} =0V, S4 closed		0.1	10	μA	
		V _{IN} =V _S =32V, I ₄ =200 μA		9	20	mA	
Logic Input Voltage Threshold, V _{IN}	Adjust V _{IN} for V _{GATE} low				2	V	
	Adjust V _{IN} for V _{GATE} high		4.5				
Logic Input Current, I3	V+=32V	V _{IN} =0V	-1			μA	
		V _{IN} =32V			1		
Input Capacitance	Pin 3			5		pF	
Gate Drive, V _{GATE}	S1, S2 closed, V _S =V+, V _{IN} =5V	V+=7V, I ₈ =0	13	15		V	
		V+=15V, I ₈ =100 μA	24	27			
Zener Clamp, V _{GATE} -V _{SOURCE}	S2 closed, V _{IN} =5V	V+=15V, V _S =15V	11	12.5	15	V	
		V+=32V, V _S =32V	11	13	16		
Gate Turn-on Time, t _{ON} (Note 4)	V _{IN} switched from 0 to 5V; measure time for V _{GATE} to reach 20V			25	50	μS	
Gate Turn-off Time, t _{OFF}	V _{IN} switched from 5 to 0V; measure time for V _{GATE} to reach 1V			4	10	μS	
Threshold Bias Voltage, V4	I ₄ =200 μA		1.7	2	2.2	V	
Current Sense Trip Voltage, V _{SENSE} -V _{SOURCE}	S2 closed, V _{IN} =5V, Increase I ₅	V+=7V, I ₄ =100 μA	S4 closed	75	105	135	mV
			VS=4.9V	70	100	130	
		V+=15V, I ₄ =200 μA	S4 closed	150	210	270	
			VS=11.8V	140	200	260	
		V+=32V, I ₄ =500 μA	VS=0V	360	520	680	
		VS=25.5V	350	500	650		
Peak Current Trip Voltage, V _{SENSE} -V _{SOURCE}	S3, S4 closed, V+=15V, V _{IN} =5V		1.6	2.1		V	
Fault Output Voltage, V14	V _{IN} =0V, I ₁₄ =-100 μA			0.4	1	V	
	V _{IN} =5V, I ₁₄ =100 μA, current sense tripped		14	14.6			
Current Sense Inhibit, V1	V1 above which current sense is disabled			7.5	13	V	
	V1 below which current sense is enabled		1	7.5		V	

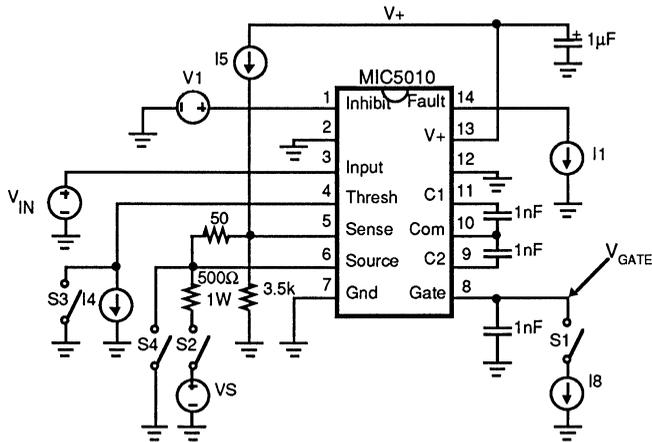
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2: The MIC5010 is ESD sensitive.

Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at $T_A=25^\circ\text{C}$ and $T_A=85^\circ\text{C}$ (125°C for A version), and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

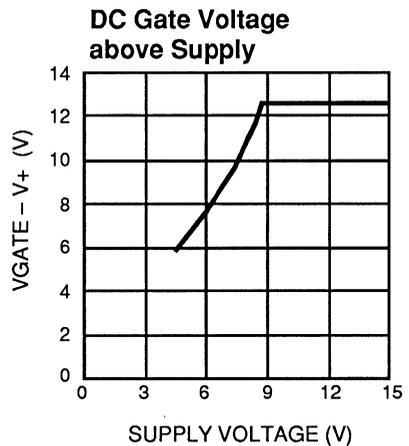
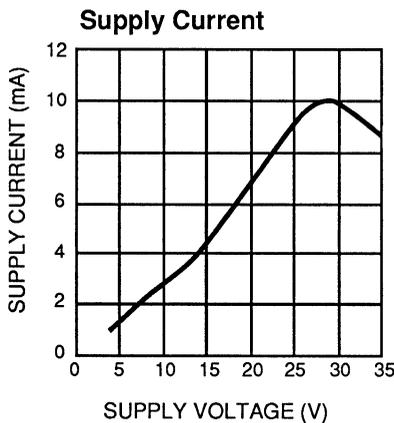
Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster--see Applications Information.

Test Circuit



2

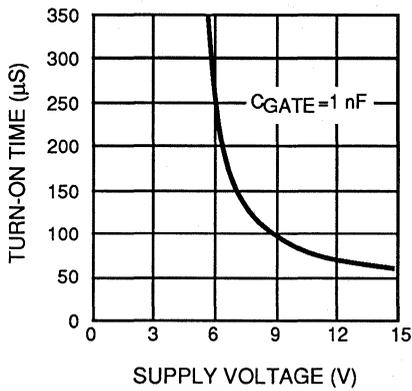
Typical Characteristics



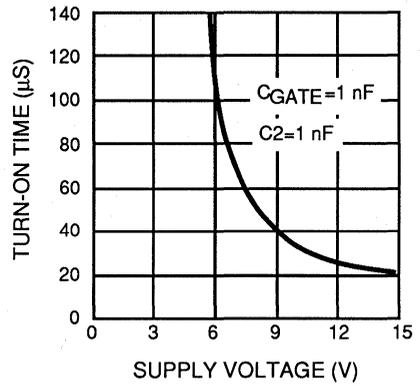
* Time for gate voltage to reach V+ + 5V in test circuit with VS = V+ - 5V (prevents gate clamp from interfering with measurement).

Typical Characteristics (Continued)

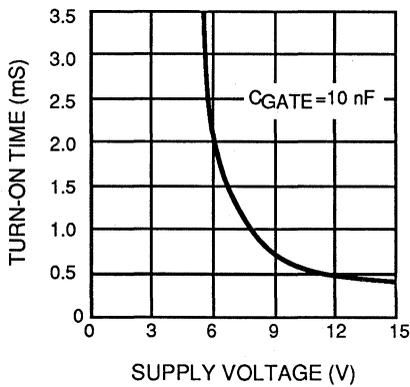
High-side Turn-on Time*



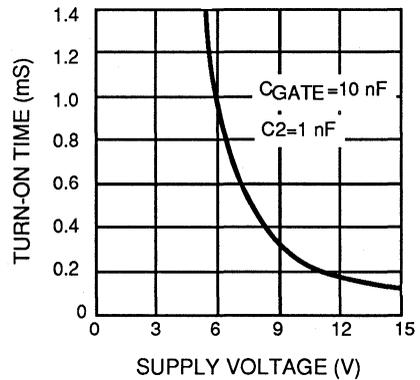
High-side Turn-on Time*



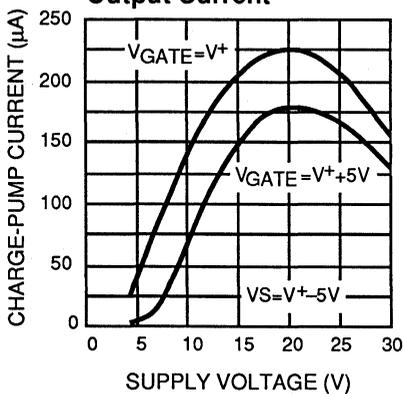
High-side Turn-on Time*



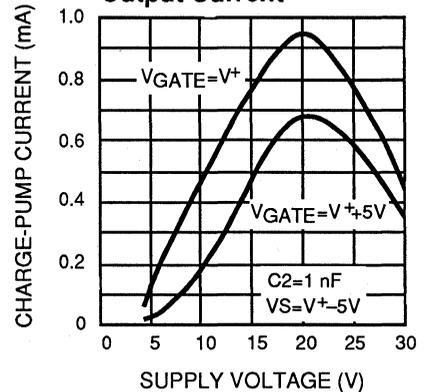
High-side Turn-on Time*



Charge Pump Output Current

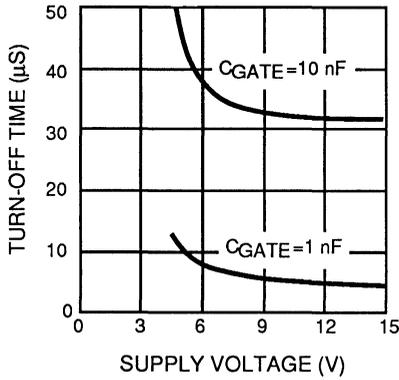


Charge Pump Output Current

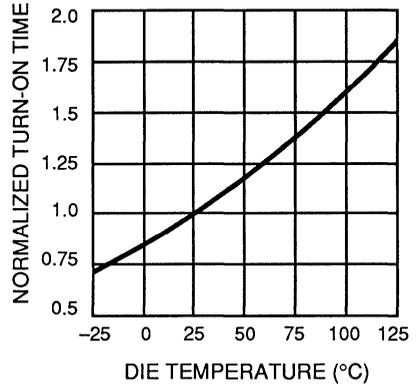


Typical Characteristics (Continued)

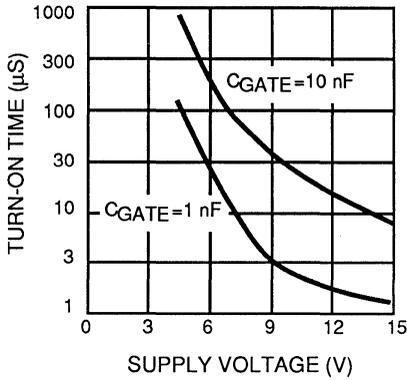
Turn-off Time



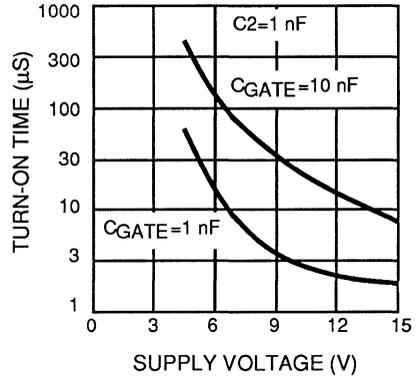
Turn-on Time



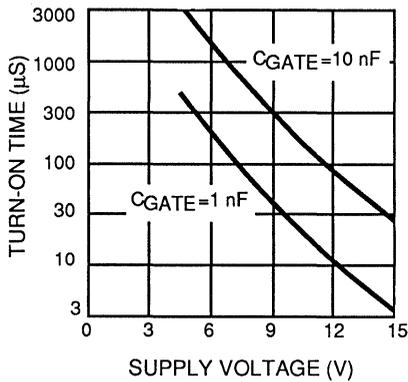
Low-side Turn-on Time for Gate = 5V



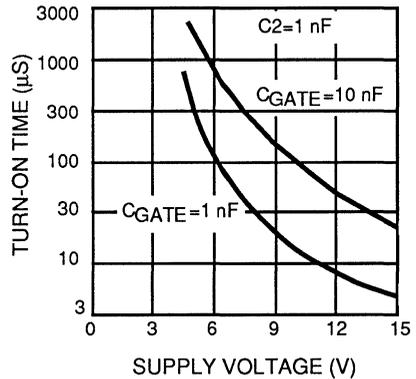
Low-side Turn-on Time for Gate = 5V



Low-side Turn-on Time for Gate = 10V



Low-side Turn-on Time for Gate = 10V



2

Applications Information

Functional Description (Refer to Block Diagram)

The various MIC5010 functions are controlled via a logic block connected to the input pin 3. When the input is low all functions are turned off for low standby current, and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET. A bandgap type voltage regulator is also turned on which biases the current sense circuitry.

The charge pump incorporates a 100 kHz oscillator and on-chip pump capacitors capable of charging 1 nF to 5V above supply in 60 μS typical. With the addition of 1 nF capacitors at C1 and C2, the turn-on time is reduced to 25 μS typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason a zener clamp (12.5V typical) is provided between the gate pin 8 and the source pin 6 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

The current sense operates by comparing the sense voltage at pin 5 to an offset version of the source voltage at pin 6. Current I_4 flowing in threshold pin 4 is mirrored and returned to the source via a 1 kΩ resistor to set the offset or trip voltage. When $(V_{SENSE} - V_{SOURCE})$ exceeds V_{TRIP} , the current sense trips and sets the current sense latch to turn off the power FET. An integrating comparator is used to reduce sensitivity to spikes on pin 5. The latch is reset to turn the FET back on by "recycling" the input pin 3 low and then high again.

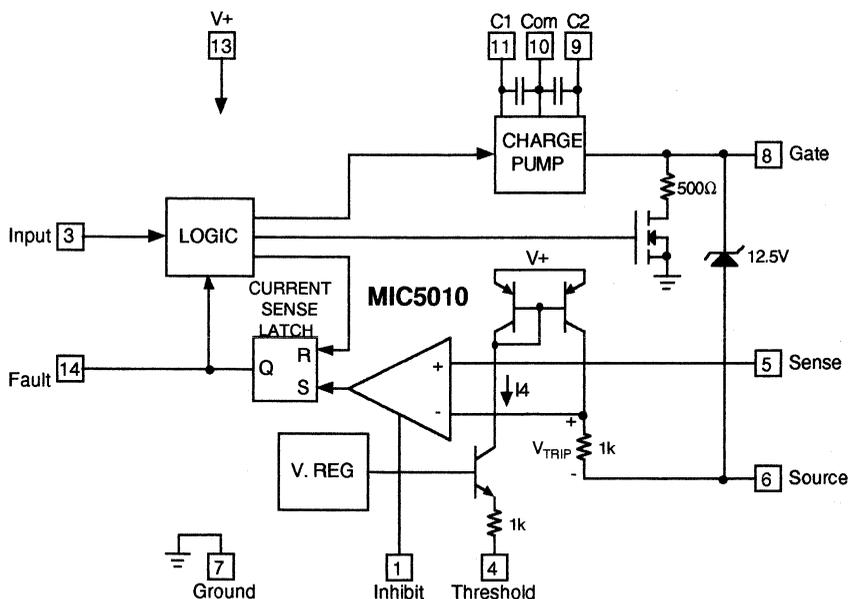
A resistor R_{TH} from pin 4 to ground sets I_4 , and hence V_{TRIP} . An additional capacitor C_{TH} from pin 4 to ground creates a higher trip voltage at turn-on, which is necessary to prevent high in-rush current loads such as lamps or capacitors from false-tripping the current sense.

When the current sense has tripped, the fault pin 14 will be high as long as the input pin 3 remains high. However, when the input is low the fault pin will also be low.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of common pitfalls encountered while prototyping: *Supplies*: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components--especially electrolytic capacitors--with possibly catastrophic results. A 10 μF supply bypass capacitor *at the chip* is recommended.

Block Diagram



Pin Description (Refer to Figures 1 and 2)

Pin Number	Pin Name	Pin Function
1	Inhibit	Inhibits current sense function when connected to supply. Normally grounded.
3	Input	Resets current sense latch and turns on power MOSFET when taken above threshold (3.5V typical). Pin 3 requires <math><1 \mu\text{A}</math> to switch.
4	Threshold	Sets current sense trip voltage according to: $V_{\text{TRIP}} = \frac{2200}{R_{\text{TH}} + 1000}$ where R_{TH} to ground is 3.3k to 21k Ω . Adding capacitor C_{TH} increases the trip voltage at turn-on to 2V. Use $C_{\text{TH}} = 10 \mu\text{F}$ for a 10 mS turn-on time constant.
5	Sense	The sense pin causes the current sense to trip when V_{SENSE} is V_{TRIP} above V_{SOURCE} . Pin 5 is used in conjunction with a current shunt in the source of a 3 lead FET or a resistor R_{S} in the sense lead of a current sensing FET.
6	Source	Reference for the current sense voltage on pin 5 and return for the gate clamp zener. Connect to the load side of current shunt or kelvin lead of current sensing FET. Pins 5 and 6 can safely swing to -10V when turning off inductive loads.
7	Ground	
8	Gate	Drives and clamps the gate of the power FET. Pin 8 will be clamped to approximately -0.7V by an internal diode when turning off inductive loads.
9, 10, 11	C2, Com, C1	Optional 1 nF capacitors reduce gate turn-on time; C2 has dominant effect.
13	V+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10 μF is recommended close to pins 13 and 7.
14	Fault	Outputs status of protection circuit when pin 3 is high. Fault low indicates normal operation; fault high indicates current sense tripped.

Applications Information (Continued)

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50 mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100 mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5010 is suited for use in high- or low-side driver applications with over-current protection for both current-sensing and standard MOSFETs. In addition, the MIC5010 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the **Test Circuit**) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types. Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10 μs to $V_{GS}=1V$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics. Each topology is described in this section. Note that I_L , as used in the design equations, is the load current that just trips the over-current comparator.

Low-Side Driver with Current Shunt (Figure 2). The over-current comparator monitors R_S and trips if $I_L \times R_S$ exceeds V_{TRIP} . R_{TH} is selected to produce the desired trip voltage.

As a guideline, keep V_{TRIP} within the limits of 100 mV and 500 mV ($R_{TH}=3.3\text{ k}\Omega$ to 21 kΩ). Thresholds at the high end offer the best noise immunity, but also compromise switch drop (especially in low voltage applications) and power dissipation.

The trip current is set higher than the maximum expected load current—typically twice that value. Trip point accuracy is a function of resistor tolerances, comparator offset (only a few millivolts), and threshold bias voltage (V_4). The values shown in Figure 2 are designed for a trip current of 20 amperes. It is important to ground pin 6 at the *current shunt* R_S , to eliminate the effects of ground resistance.

A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5010 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener.

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μs or less on a 12 to 15V supply.

High-Side Driver with Current Shunt (Figure 3). The comparator input pins (source and sense) float with the current sensing resistor (R_S) on top of the load. R1 and R2 add a small, additional potential to V_{TRIP} to prevent false-triggering of the over-current shutdown circuit with open or inductive loads. R1 is sized for a current flow of 1 mA, while R2 contributes a drop of 100mV. The shunt voltage should be 200 to 500 mV at the trip point. The example of Figure 3 gives a 10A trip current when the output is near supply. The trip point is somewhat reduced when the output is at ground as the voltage drop across R1 (and therefore R2) is zero.

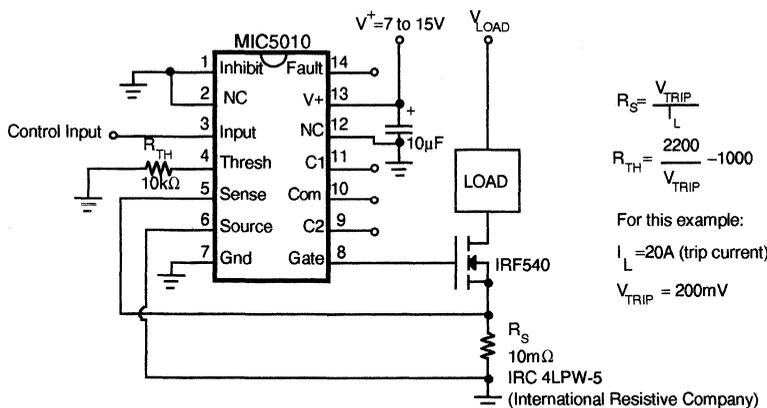


Figure 2. Low-Side Driver with Current Shunt

Applications Information (Continued)

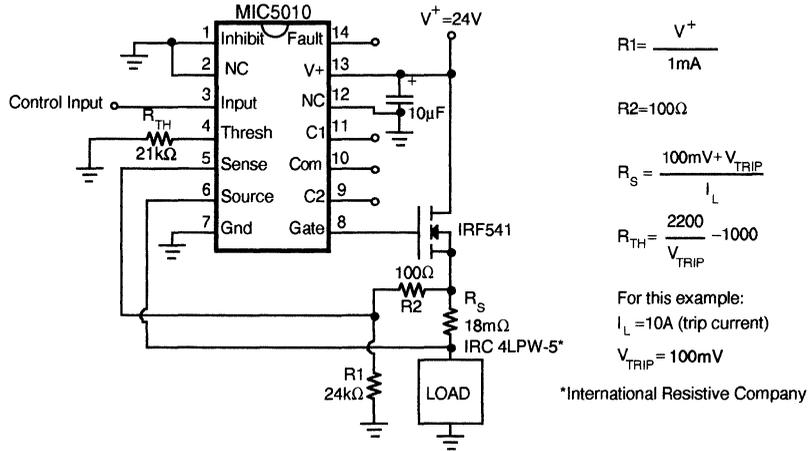


Figure 3. High-Side Driver with Current Shunt

High-side drivers implemented with MIC501X predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the predriver holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5010 source and sense pins (5 and 6) are designed to withstand this negative excursion without damage. External clamp diodes are unnecessary, but may be added to reduce power dissipation in the MOSFET.

Current Shunts (R_S). Low-valued resistors are necessary for use at R_S . Values for R_S range from 5 to 50 mΩ, at 2 to 10W. Worthy of special mention are Kelvin-sensed, "four-terminal" units supplied by a number of manufacturers†. Kelvin-sensed resistors eliminate errors that are caused by lead and terminal resistances, and simplify product assembly. 10% tolerance is normally adequate, and with shunt potentials of 200 mV thermocouple effects are insignificant. Temperature coefficient is important; a linear, 500 ppm/°C change will contribute as much as 10% shift in the over-current trip point. Most power resistors designed for current shunt service drift less than 100 ppm/°C.

Low-Side Driver with Current Sensing MOSFET (Figure 4). Several manufacturers now supply power MOSFETs in which a small sampling of the total load current is diverted to a "sense" pin. One additional pin, called "Kelvin source," is included to eliminate the effects of resistance in the source bond wires. Current-sensing MOSFETs are specified with a sensing ratio "S" which describes the relation-

ship between the on-resistance of the sense connection and the body resistance "R" of the main source pin. Current sensing MOSFETs eliminate the current shunt required by standard MOSFETs.

The design equations for a low-side driver using a current sensing MOSFET are shown in Figure 4. "S" is specified on the MOSFET's datasheet, and "R" must be measured or estimated. V_{TRIP} must be less than $R \times I_L$, or else R_S will become negative. Substituting a MOSFET with higher on-resistance, or reducing V_{TRIP} fixes this problem. $V_{\text{TRIP}} = 100$ to 200 mV is suggested. Although the load supply is limited only by MOSFET ratings, the MIC5010 supply should be limited to 15V to prevent damage to the gate clamp zener. Output clamping is necessary for inductive loads.

"R" is the body resistance of the MOSFET, excluding bond resistances. $R_{\text{DS(ON)}}$ as specified on MOSFET data sheets includes bond resistances. A Kelvin-connected ohmmeter (using TAB and SOURCE for forcing, and SENSE and KELVIN for sensing) is the best method of evaluating "R." Alternatively, "R" can be estimated for large MOSFETs ($R_{\text{DS(ON)}} \leq 100$ mΩ) by simply halving the stated $R_{\text{DS(ON)}}$, or by subtracting 20 to 50 mΩ from the stated $R_{\text{DS(ON)}}$ for smaller MOSFETs.

High-Side Driver with Current Sensing MOSFET (Figure 1). The design starts by determining the value of "S" and "R" for the MOSFET (use the guidelines described for the low-side version). Let $V_{\text{TRIP}} = 100$ mV, and calculate R_S for

†Suppliers of Kelvin-sensed power resistors:

Dale Electronics, Inc., 2064 12th Ave., Columbus, NE 68601. Tel: (402) 564-3131
 International Resistive Co., P.O. Box 1860, Boone, NC 28607-1860. Tel: (704) 264-8861
 Kelvin, 14724 Ventura Blvd., Ste. 1003, Sherman Oaks, CA 91403-3501. Tel: (818) 990-1192
 RCD Components, Inc., 520 E. Industrial Pk. Dr., Manchester, NH 03103. Tel: (603) 669-0054
 Ultronix, Inc., P.O. Box 1090, Grand Junction, CO 81502. Tel: (303) 242-0810



Applications Information (Continued)

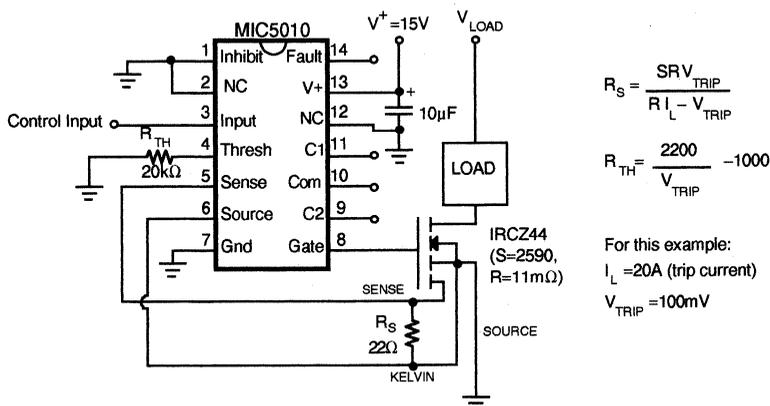


Figure 4. Low-Side Driver with Current-Sensing MOSFET

$$R_S = \frac{SRV_{TRIP}}{R I_L - V_{TRIP}}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:
 $I_L = 20A$ (trip current)
 $V_{TRIP} = 100mV$

a desired trip current. Next calculate R_{TH} and R_1 . The trip point is somewhat reduced when the output is at ground as the voltage drop across R_1 is zero. No clamping is required for inductive loads.

Typical Applications

Start-up into a Dead Short. If the MIC5010 attempts to turn on a MOSFET when the load is shorted, a very high current flows. The over-current shutdown will protect the MOSFET, but only after a time delay of 5 to 10 μS . The MOSFET must be capable of handling the overload; consult the device's SOA curve. If a short circuit causes the MOSFET to exceed its 10 μS SOA, a small inductance in series with the source can help limit di/dt to control the peak current during the 5 to 10 μS delay.

When testing short-circuit behavior, use a current probe rated for both the peak current and the high di/dt.

The over-current shutdown delay varies with comparator overdrive, owing to noise filtering in the comparator. A delay of up to 100 μS can be observed at the threshold of shutdown. A 20% overdrive reduces the delay to near minimum.

Incandescent Lamps. The cold filament of an incandescent lamp exhibits less than one-tenth as much resistance as when the filament is hot. The initial turn-on current of a #6014 lamp is about 70A, tapering to 4.4A after a few hundred milliseconds. It is unwise to set the over-current trip point to 70A to accommodate such a load. A "resistive" short that draws less than 70A could destroy the MOSFET by allowing sustained, excessive dissipation. If the over-current trip point is set to less than 70A, the MIC5010 will not start a cold filament. The solution is to start the lamp with a high trip point, but reduce this to a reasonable value after the lamp is hot.

The MIC5010 over-current shutdown circuit is designed to handle this situation by varying the trip point with time (see Figure 5). R_{TH1} functions in the conventional manner, providing a current limit of approximately twice that required by the lamp. R_{TH2} acts to increase the current limit at turn-on to approximately 10 times the steady-state lamp current. The high initial trip point decays away according to a 20 mS time constant contributed by C_{TH} . R_{TH2} could be eliminated with C_{TH} working against the internal 1 k Ω resistor, but this results in a very high over-current threshold. As a rule of thumb design the over-current circuitry in the conventional manner, then add the R_{TH2}/C_{TH} network to allow for lamp start-up. Let $R_{TH2} = (R_{TH1} + 10) - 1k\Omega$, and choose a capacitor that provides the desired time constant working against R_{TH2} and the internal 1 k Ω resistor.

When the MIC5010 is turned off, the threshold pin (4) ap-

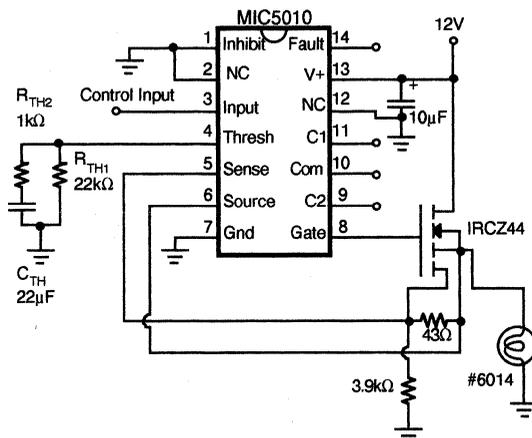


Figure 5. Time-Variable Trip Threshold

Applications Information (Continued)

pears as an open circuit, and C_{TH} is discharged through R_{TH1} and R_{TH2} . This is much slower than the turn-on time constant, and it simulates the thermal response of the filament. If the lamp is pulse-width modulated, the current limit will be reduced by the residual charge left in C_{TH} .

Modifying Switching Times. Do not add external capacitors to the gate to slow down the switching time. Add a resistor (1 k Ω to 51 k Ω) in series with the gate of the MOSFET to achieve this result.

External capacitors can be added at C1 and C2 for faster switching times (see **Block Diagram**). Values of 100 pF to 1 nF produce useful speed increases. If component count is critical, C2 (pins 9 to 10) can be used alone with only a small loss of speed compared to using both capacitors.

Bootstrapped High-Side Driver (Figure 6). The speed of a high-side driver can be increased to better than 10 μ S by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100 Hz to 20 kHz), or where it is energized for only a short period of time (≤ 25 mS). If the load is left energized for a long period of time (> 25 mS), the bootstrap capacitor will discharge and the MIC5010 supply pin will fall to $V^+ = V_{DD} - 1.4$. Under this condition pins 5 and 6 will be held above V^+ and may false trigger the over-current circuit. A larger capacitor will lengthen the maximum "on" time; 1000 μ F will hold the circuit up for 2.5 seconds, but requires more charge time when the circuit is turned off. The optional Schottky barrier diode improves turn-on time on supplies of less than 10V.

Since the supply current in the "off" state is only a small leakage, the 100 nF bypass capacitor tends to remain charged for several seconds after the MIC5010 is turned off. In a PWM application the chip supply is actually much higher than the system supply, which improves switching time.

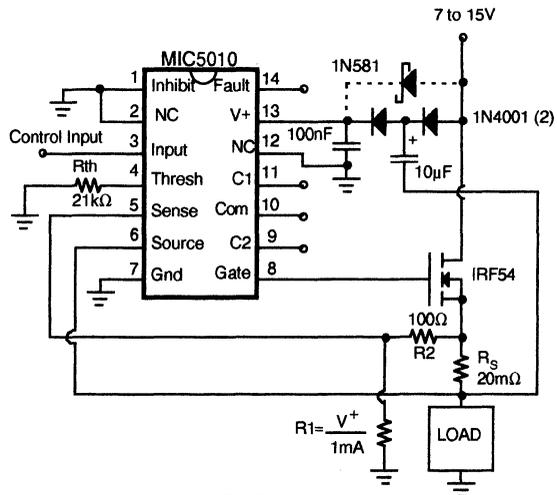


Figure 6. Bootstrapped High-Side Driver

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Electronic Circuit Breaker (Figure 7). The MIC5010 forms the basis of a high-performance, fast-acting circuit breaker. By adding feedback from FAULT to INPUT the breaker can be made to automatically reset. If an over-

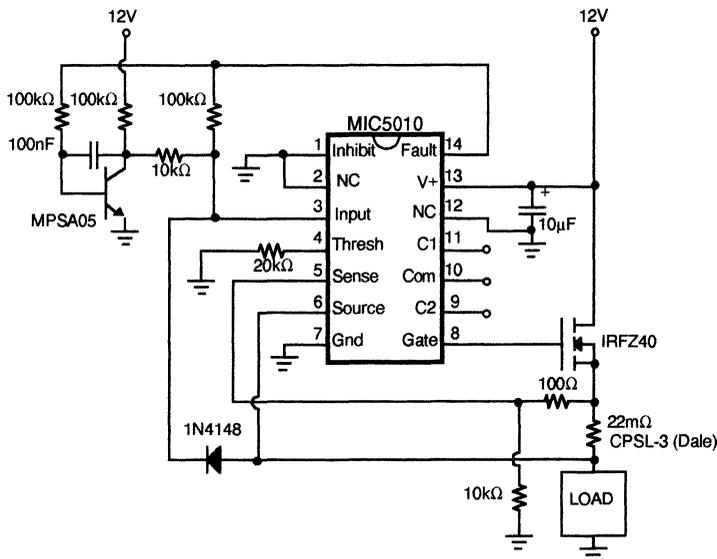


Figure 7. 10-Ampere Electronic Circuit Breaker

Applications Information (Continued)

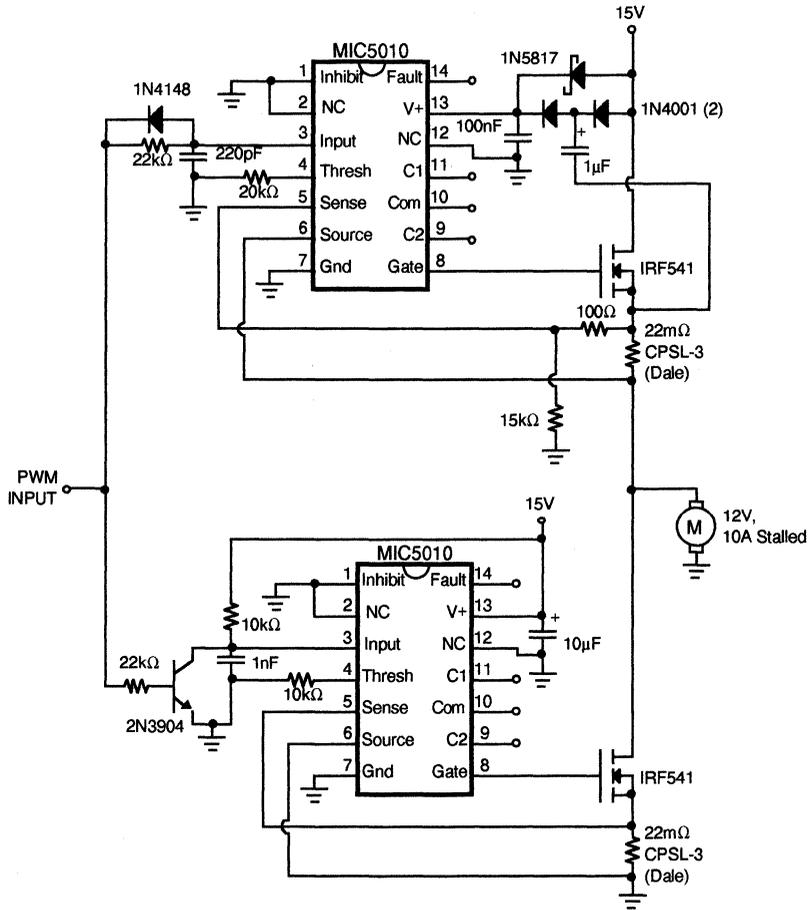


Figure 11. Half-Bridge Motor Driver

Applications Information (Continued)

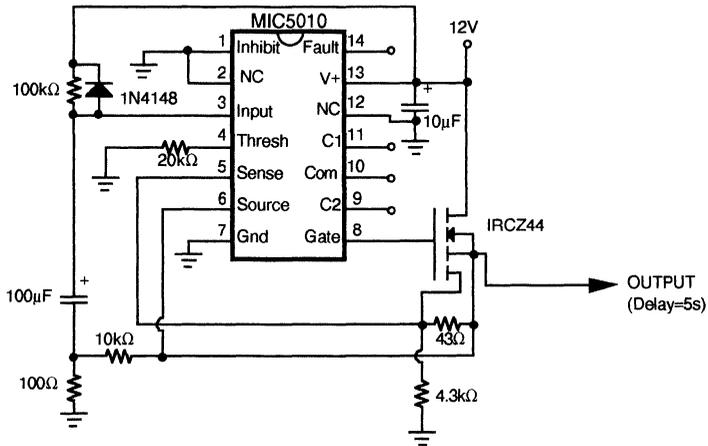


Figure 12. Time-Delay Relay with 30A Over-Current Protection

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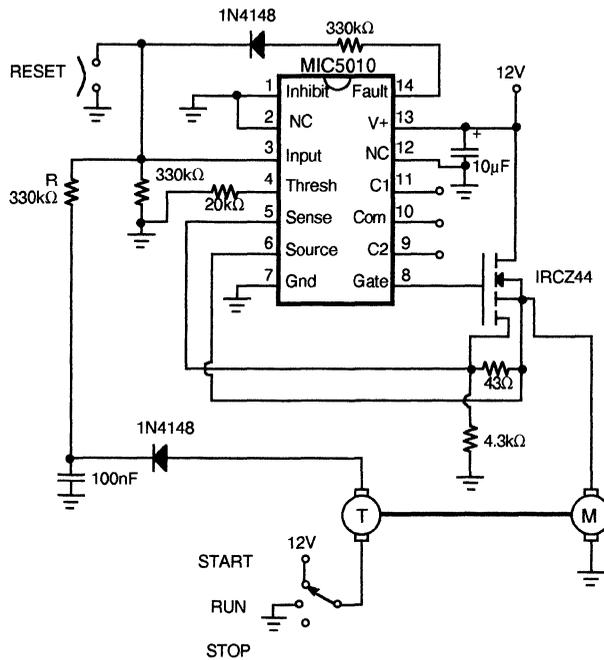


Figure 13. Motor Stall Shutdown

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5010, it is helpful to understand the operation of the gate control circuitry (see Figure 14). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5010 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5010 is commanded on. Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3

turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5010 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5010 operate quickly in low-side applications. In high-side applications Q5 pre-charges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

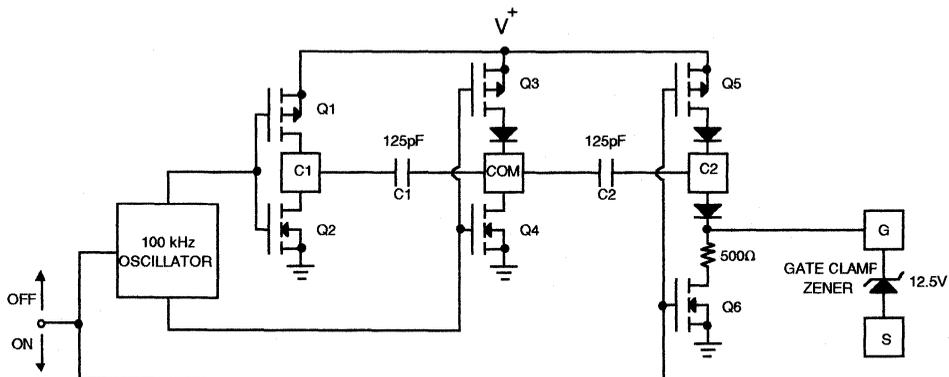


Figure 14. Gate Control Circuit Detail



MIC5011

Minimum Parts Count MOSFET Predriver

General Description

The MIC5011 is the "minimum parts count" member of the Micrel MIC501X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 8-pin MIC5011 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low-side switch.

The MIC5011 charges a 1 nF load in 60 μ S typical with no external components. Faster switching is achieved by adding two 1 nF charge pump capacitors. Operation down to 4.75V allows the MIC5011 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple, paralleled MOSFETs can be driven by a single MIC5011 for ultra-high current applications.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5012 dual predriver, and MIC5013 protected 8 pin predriver.

Features

- 4.75V-32V operation
- Less than 1 μ A standby current in the 'off' state
- Internal charge pump to drive the gate of an N-channel power FET above supply
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power FETs operating on logic supplies
- 25 μ S typical turn-on time with optional external capacitors
- Implements high- or low-side drivers

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching

Typical Applications

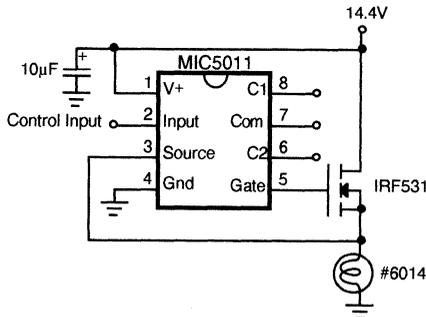


Figure 1. High Side Driver

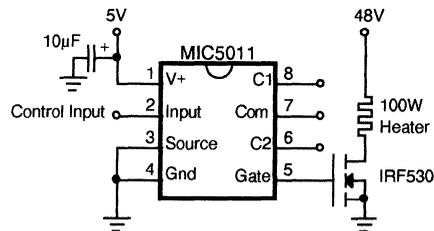


Figure 2. Low Side Driver

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC5011BN	-40°C to +85°C	8-pin Plastic DIP
MIC5011BJ	-40°C to +85°C	8-pin Ceramic DIP
MIC5011BM	-40°C to +85°C	8-pin SOIC
MIC5011AJ	-55°C to +125°C	8-pin Ceramic DIP
MIC5011AJB	-55°C to +125°C	8-pin Ceramic DIP

Protected under one or more of the following Micrel patents: patent #4,951,101; patent # 4,914,546

Note: The MIC5011 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage (V+), Pin 1	-0.5V to 36V
Input Voltage, Pin 2	-10V to V+
Source Voltage, Pin 3	-10V to V+
Current into Pin 3	50 mA
Gate Voltage, Pin 5	-1V to 50V
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Power Dissipation	1.25W
θ_{JA} (Plastic DIP)	100°C/W
θ_{JA} (Ceramic DIP)	125°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	-40°C to +85°C
Ambient Temperature: A version	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V+), Pin 1	7V to 32V high side 4.75V to 15V low side

Electrical Characteristics (Note 3) Test circuit, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V^+ = 15\text{V}$, all switches open, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Current, I_1	$V^+ = 32\text{V}$ $V_{IN} = 0\text{V}$, $V_S = 0\text{V}$, S2 closed		0.1	10	μA
		$V_{IN} = V_S = 32\text{V}$		8	20
Logic Input Voltage Threshold, V_{IN}	$V^+ = 4.75\text{V}$	Adjust V_{IN} for V_{GATE} low			2
		Adjust V_{IN} for V_{GATE} high	4.5		
	$V^+ = 15\text{V}$	Adjust V_{IN} for V_{GATE} high			5
Logic Input Current, I_2 (Note 5)	$V^+ = 32\text{V}$	$V_{IN} = 0\text{V}$	-1		μA
		$V_{IN} = 32\text{V}$			1
Input Capacitance	Pin 2		5		pF
Gate Drive, V_{GATE}	S1, S2 closed, $V_S = V^+$	$V^+ = 4.75\text{V}$, $I_5 = 0$, $V_{IN} = 4.5\text{V}$	7	10	
		$V^+ = 15\text{V}$, $I_5 = 100\ \mu\text{A}$, $V_{IN} = 5\text{V}$	24	27	
Zener Clamp $V_{GATE} - V_{SOURCE}$	S2 closed, $V_{IN} = 5\text{V}$	$V^+ = 15\text{V}$, $V_S = 15\text{V}$	11	12.5	15
		$V^+ = 32\text{V}$, $V_S = 32\text{V}$	11	13	16
Gate Turn-on Time, t_{ON} (Note 4)	V_{IN} switched from 0 to 5V; measure time for V_{GATE} to reach 20V		25	50	μS
	As above, with C1 and C2 removed (Pins 6, 7, and 8 open)		60	200	
Gate Turn-off Time, t_{OFF}	V_{IN} switched from 5 to 0V; measure time for V_{GATE} to reach 1V		4	10	μS

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified Operating Ratings.

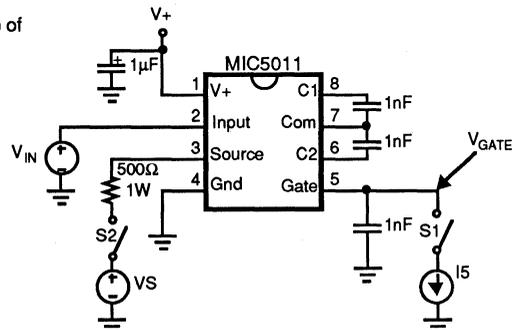
Note 2: The MIC5011 is ESD sensitive.

Note 3: Minimum and maximum Electrical Characteristics are 100% tested at $T_A = 25^\circ\text{C}$ and $T_A = 85^\circ\text{C}$, and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

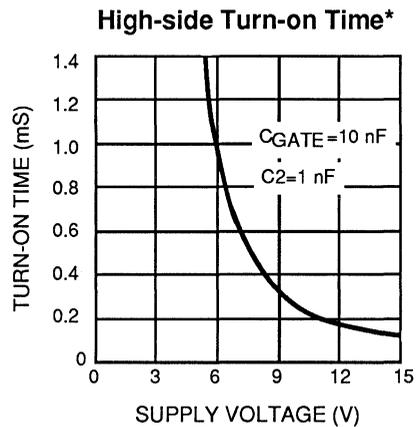
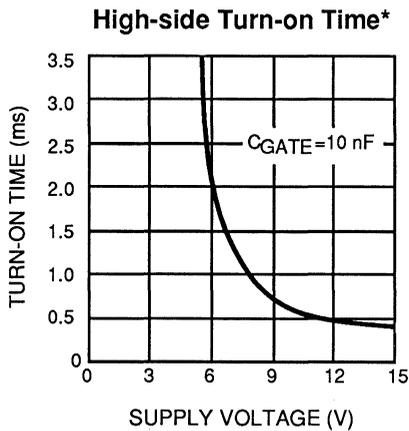
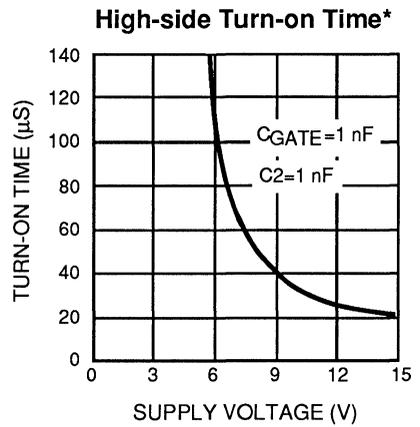
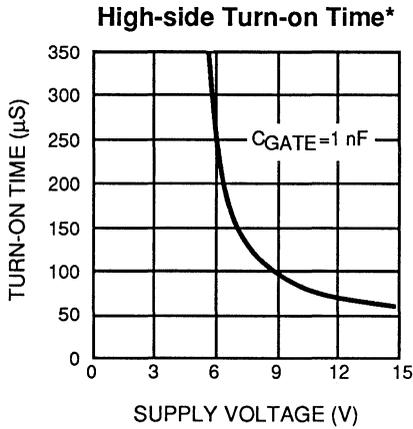
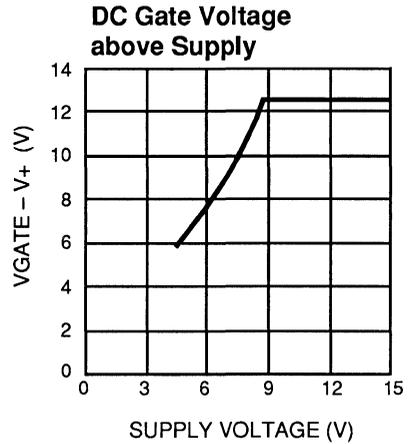
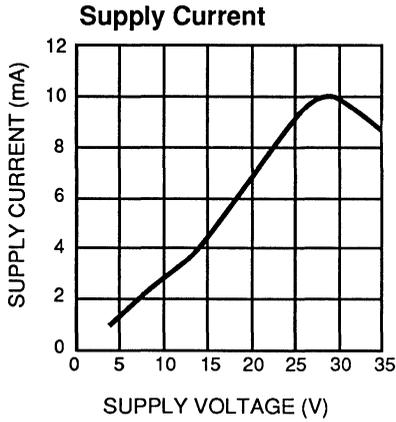
Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see Applications Information. Maximum value of switching speed seen at 125°C , units operated at room temperature will reflect the typical value shown.

Note 5: Specially sorted units with V_{IN} max (for a gate low output) of 3.5V are available. Contact factory for more details.

Test Circuit



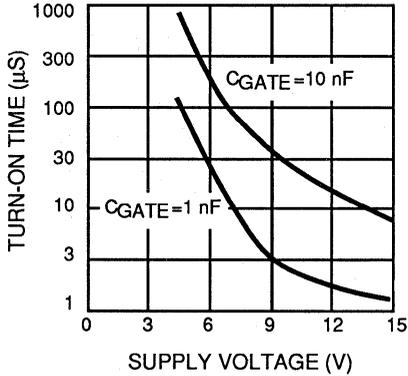
Typical Characteristics



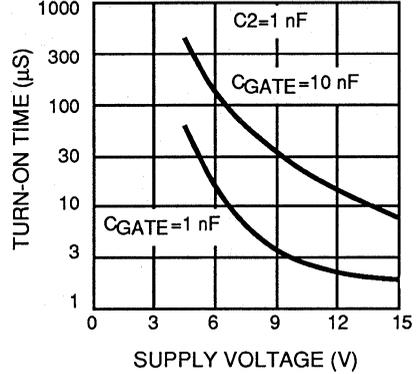
* Time for gate voltage to reach $V^+ + 5V$ in test circuit with $V_S = V^+ - 5V$

Typical Characteristics (Continued)

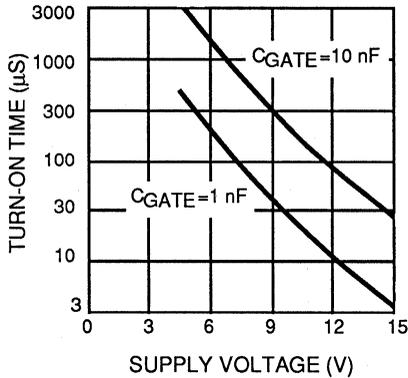
Low-side Turn-on Time for Gate = 5V



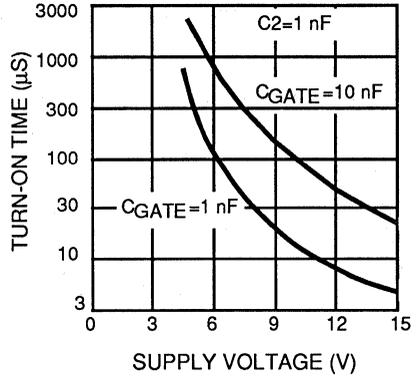
Low-side Turn-on Time for Gate = 5V



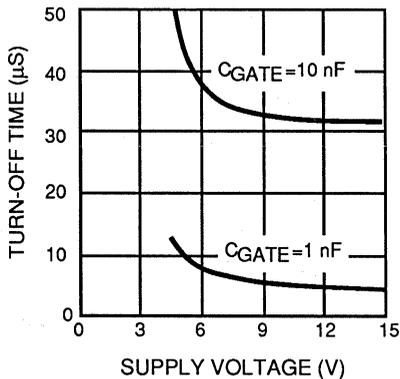
Low-side Turn-on Time for Gate = 10V



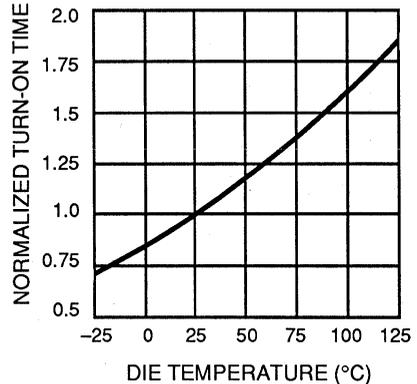
Low-side Turn-on Time for Gate = 10V



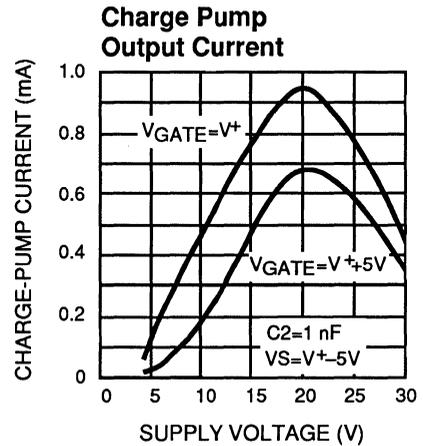
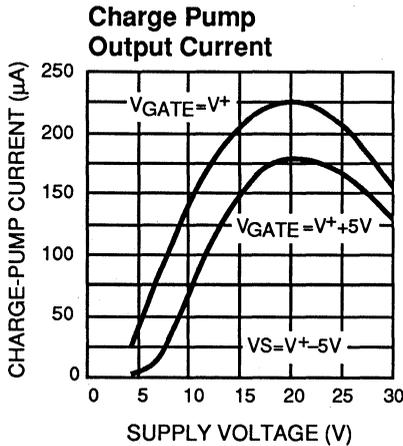
Turn-off Time



Turn-on Time



Typical Characteristics (Continued)

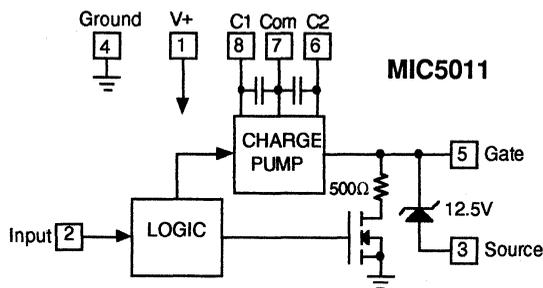


Pin Description (Refer to Typical Applications)

Pin Number	Pin Name	Pin Function
1	V+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10 µF is recommended close to pins 1 and 4.
2	Input	Turns on power MOSFET when taken above threshold (3.5V typical). Pin 2 requires <1 µA to switch.
3	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Pin 3 can safely swing to -10V when turning off inductive loads.
4	Ground	
5	Gate	Drives and clamps the gate of the power FET. Pin 5 will be clamped to approximately -0.7V by an internal diode when turning off inductive loads.
6, 7, 8	C2, Com, C1	Optional 1 nF capacitors reduce gate turn-on time; C2 has dominant effect.

2

Block Diagram



Applications Information

Functional Description (Refer to Block Diagram)

The MIC5011 functions are controlled via a logic block connected to the input pin 2. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100 kHz oscillator and on-chip pump capacitors capable of charging 1 nF above supply in 60 µS typical. With the addition of 1 nF capacitors at C1 and C2, the turn-on time is reduced to 25 µS typical (see Figure 3). The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin 5 and source pin 3 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies

Applications Information (Continued)

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: *Supplies*: many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components--especially electrolytic capacitors--with possibly catastrophic results. A 10 μF supply bypass capacitor *at the chip* is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50 m Ω power MOSFET for low drop, but careless construction techniques could easily add 50 to 100 m Ω resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5011 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5011 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in Figure 1) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types (Figures 2 and 4). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10 μs to $V_{\text{GS}}=1\text{V}$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver (Figure 1). The high-side topology works well down to $V^+=7\text{V}$ with standard MOSFETs. From 4.75 to 7V supply, a logic-level MOSFET can be substituted since the MIC5011 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

High-side drivers implemented with MIC501X predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET

source 5V or more below ground, while the MIC5011 holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5011 source pin (3) is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Low-Side Driver (Figure 2). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5011 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener. If the external capacitors are added, the output will reach 9V in approximately 250 μs and limit at 11V, on a 5V supply. Without capacitors, the switching speed is 500 μs on a 5V supply.

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μs or less on a 12 to 15V supply.

Modifying Switching Times (Figure 3). High-side switching times can be improved by a factor of 2 or more by adding external charge pump capacitors of 1 nF each. In cost-sensitive applications, omit C1 (C2 has a dominant effect on speed).

Do not add external capacitors to the MOSFET gate. Add a resistor (1 k Ω to 51 k Ω) in series with the gate to slow

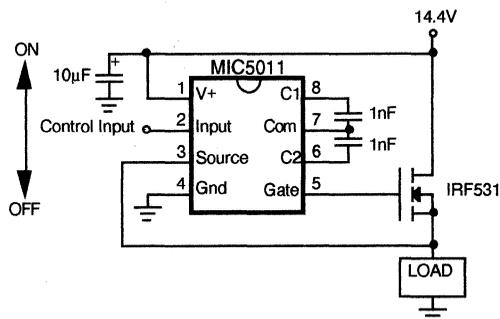


Figure 3. High Side Driver with External Charge Pump Capacitors

down the switching time.

Bootstrapped High-Side Driver (Figure 4). The speed of a high-side driver can be increased to better than 10 μs by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100 Hz to 20 kHz), or where it is energized continuously. The Schottky barrier diode prevents the MIC5011 supply pin from dropping more than 200 mV below the drain supply, and it also improves turn-on time on supplies of less than 10V. Since the supply current in the "off" state is only a small leakage, the 100 nF bypass capacitor tends to remain charged for several seconds after the MIC5011

Applications Information (Continued)

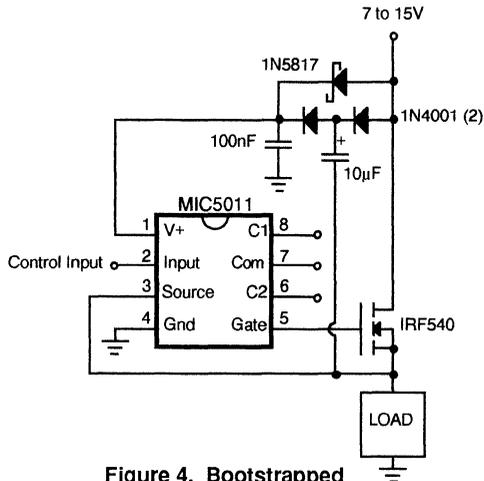


Figure 4. Bootstrapped High-Side Driver

is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

Opto-Isolated Interface (Figure 5). Although the MIC5011 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5011 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5011 will turn OFF.

Industrial Switch (Figure 6). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from

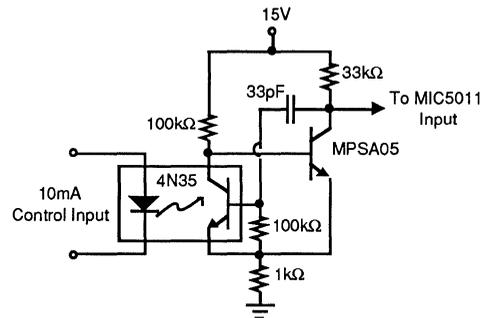


Figure 5. Improved Opto-Isolator Performance

the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

High-Voltage Bootstrap (Figure 7). Although the MIC5011 is limited to operation on 4.75-32V supplies, a floating bootstrap arrangement can be used to build a high-side switch that operates on much higher voltages. The MIC5011 and MOSFET are configured as a low-side driver, but the load is connected in series with ground.

Power for the MIC5011 is supplied by a charge pump. A 20kHz square wave (15Vp-p) drives the pump capacitor and delivers current to a 100 µF storage capacitor. A zener diode limits the supply to 18V. When the MIC5011 is off, power is supplied by a diode connected to a 15V supply. The circuit of Figure 5 is put to good use as a barrier between low voltage control circuitry and the 90V motor supply.

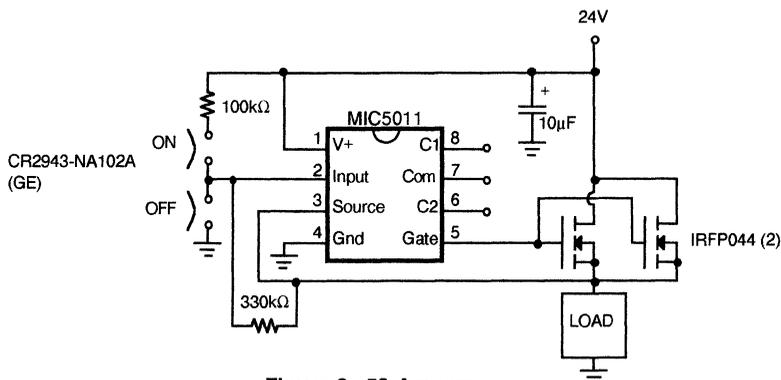


Figure 6. 50-Ampere Industrial Switch

Applications Information (Continued)

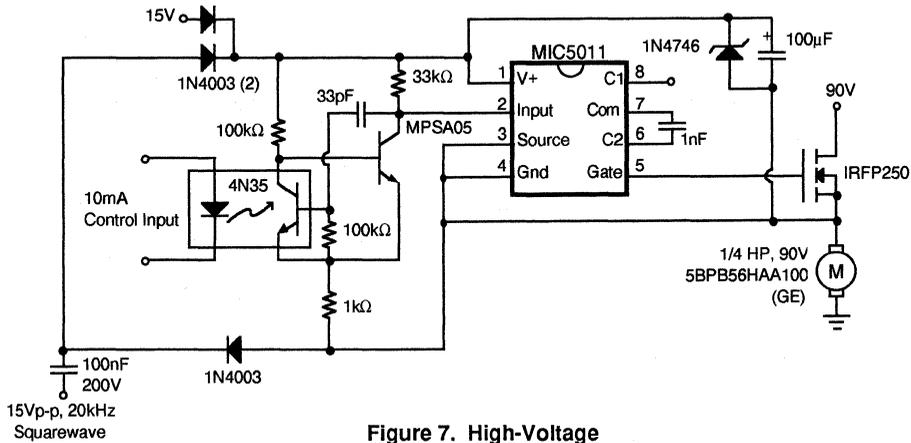


Figure 7. High-Voltage Bootstrapped Driver

Half-Bridge Motor Driver (Figure 8). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20 kHz range.

The circuit of Figure 8 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2-3 μ S dead time effectively eliminating cross conduction. Two of these circuits can be connected together to form an H-bridge for locked antiphase or sign/magnitude control.

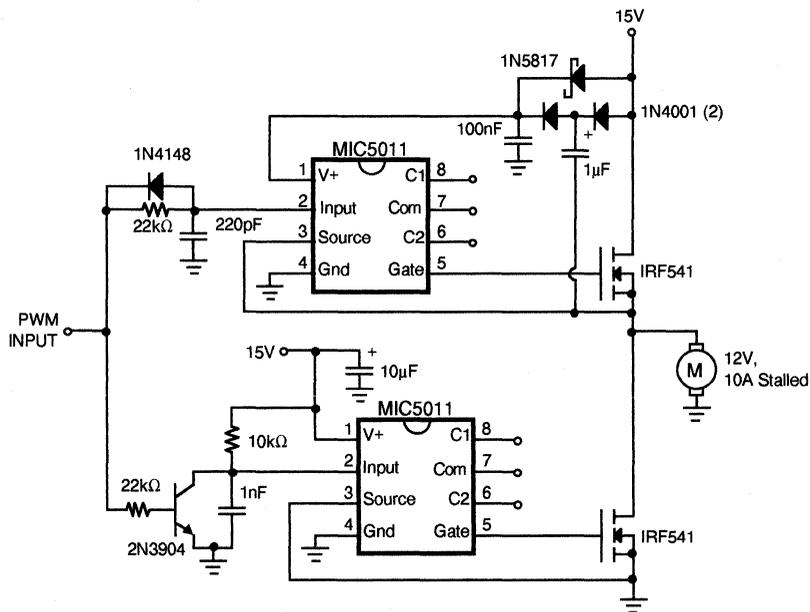


Figure 8. Half-Bridge Motor Driver

Applications Information (Continued)

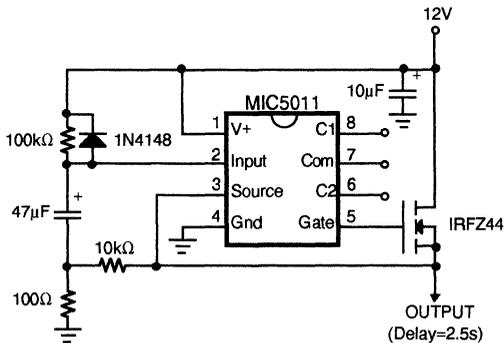


Figure 9. 30 Ampere Time-Delay Relay

Time-Delay Relay (Figure 9). The MIC5011 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100 kΩ/1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system. Hysteresis has been added to guarantee clean switching at turn-on.

Motor Driver with Stall Shutdown (Figure 10). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5011 input ON. If the motor slows down, the tach output is reduced, and the MIC5011 switches OFF. Resistor "R" sets the shutdown threshold.

Electronic Governor (Figure 11). The output of an ac tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5011. When the motor is stalled there is no tachometer output, and MIC5011 input is pulled high delivering full power to the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5011 input low, shutting the output off. Since the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5011 to switch on and off at the frequency of the tachometer signal. A PWM action results since the average dc voltage at the input decreases as the motor spins faster. The 1kΩ potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100 nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

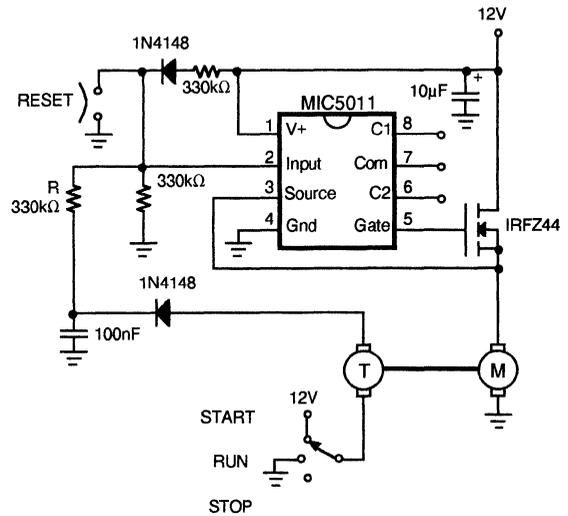


Figure 10. Motor Stall Shutdown

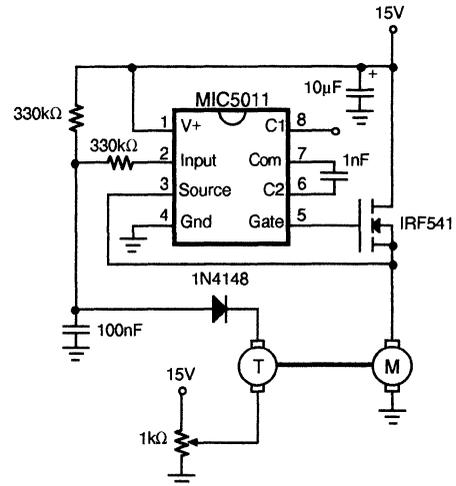


Figure 11. Electronic Governor

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5011, it is helpful to understand the operation of the gate control circuitry (see Figure 12). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5011 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5011 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing pin C2 above supply (charge is dumped

into the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5011 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5011 operate quickly in low-side applications. In high-side applications Q5 pre-charges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

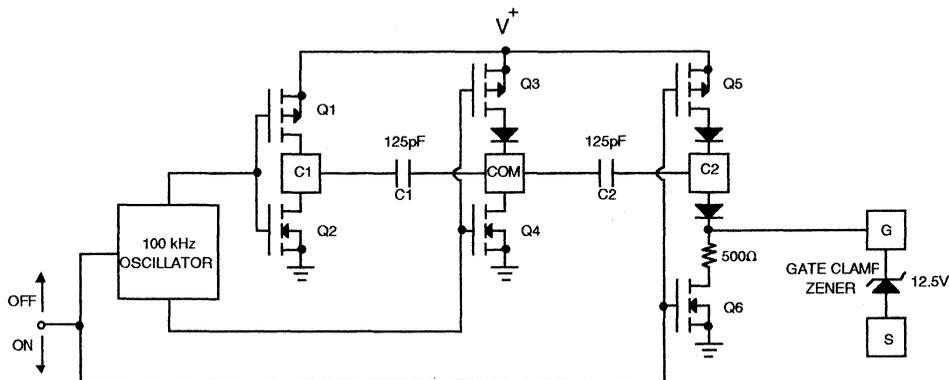


Figure 12. Gate Control Circuit Detail

Introduction

Power MOSFETs are often preferred over bipolar transistors as high current switches. In static switching applications the MOSFET takes no drive power, where a bipolar transistor requires a large base current. Bipolar transistors also exhibit inferior SOA when compared to power MOSFETs. In high side switching circuits N-channel MOSFETs are preferred over P-channel devices owing to the lower cost of an N-channel device for a given "on" resistance. Unfortunately, N-channel MOSFETs are not well-suited in high-side switch applications because in order to fully enhance the MOSFET, the gate must be driven to a potential higher than the drain supply. While a separate supply could be used for the gate drive circuitry, this is unnecessary if a charge pump is used to drive the MOSFET's gate.

A simple charge pump voltage doubler is shown in Figure 1. The object is to charge C_1 from the supply, and then transfer its charge to C_2 . Since C_2 is referred to V_{DD} , V_{OUT} will be greater than V_{DD} .

The switch is first connected to ground, charging C_1 (through D_1) to the supply voltage. Next, the switch is toggled to supply. C_1 dumps its charge through D_2 into

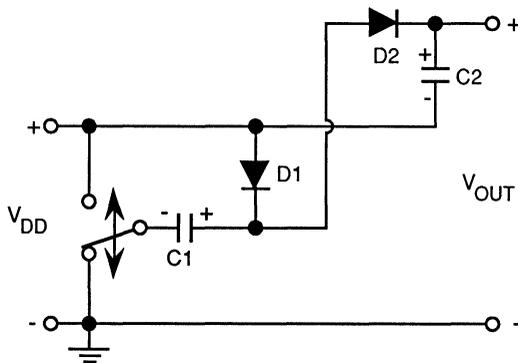


Figure 1. Charge Pump Voltage Doubler

C_2 . If the process is repeated C_2 will eventually charge to a potential equal to V_{DD} , lifting V_{OUT} to $2 \times V_{DD}$ (neglecting switch and diode losses). If V_{OUT} is used to drive the gate of an N-channel MOSFET, the device will be enhanced by an amount equal to V_{DD} . A similar technique is employed by the MIC5011 high side MOSFET pre-driver to enhance an N-channel MOSFET without the need for a second supply.

The MIC5011

A simplified block diagram of the MIC5011 is shown in Figure 2. The charge pump is configured as a tripler, and operates at a 100 kHz rate. The oscillator is enabled by the control logic to turn the MOSFET on. For supplies greater than 13V the charge pump can develop in excess of 20V gate drive--more than the average power MOSFET can safely handle. A clamp is included on-chip to limit the gate drive to approximately 12.5V. Figure 3 shows gate drive as a function of supply voltage.

Turning the MOSFET off involves more than just stopping the charge pump oscillator: charge stored on the gate of the MOSFET must be dumped by an active pull-down. The pull-down is turned off when the MIC5011 is commanded to turn the power MOSFET back on.

Small charge pump capacitors (≈ 100 pF) are included on-chip, and provision is made for adding external pump capacitors (pins 6, 7, and 8) where faster switching is desired. A useful increase in turn-on switching speed will be observed for values of 100 pF to 1 nF. Full enhancement gate rise times range from several hundred microseconds for low supply voltage, a large MOSFET, and no external charge pump capacitors, to less than 50 μ s for supplies of 12 to 15V and 1 nF external charge pump capacitors. The *output* rise time is very fast when operating on high (15V) supply voltages, as the charge pump drives the MOSFET gate up to V_{DD} within 2 μ s of the input going high.

The control input turns the MOSFET on for any input greater than approximately 3.5V, so the MIC5011 interfaces directly with CMOS logic, open collector gates, opto-isolators, switches, etc. Interfacing techniques are discussed in greater detail in a later section.

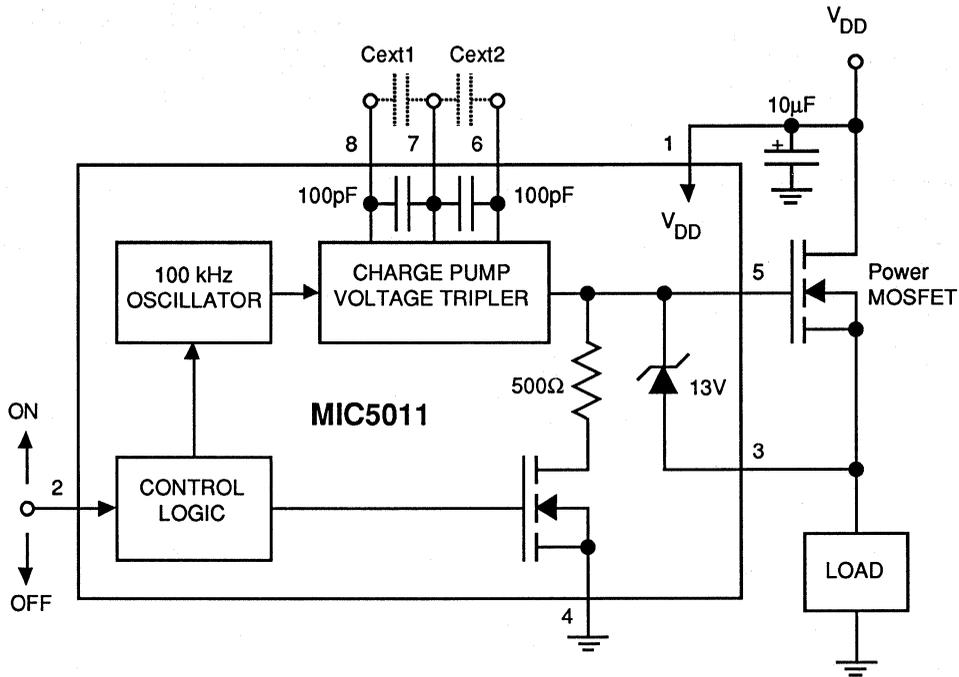


Figure 2. MIC5011 Block Diagram

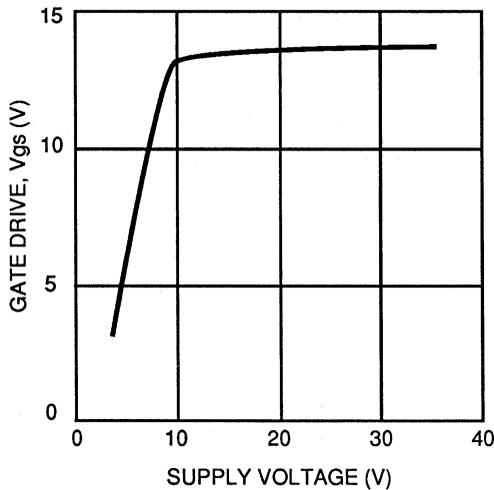


Figure 3. Gate Drive vs. Supply Voltage

Inductive Loads

Many loads such as solenoids, motors, and relays, exhibit inductive characteristics. When an inductive load is commutated a negative voltage spike results (see Figure 4). The spike is clamped by the power MOSFET's source as the MIC5011 holds the gate at ground potential. The load inductance drives the source as far negative as necessary to threshold the MOSFET and force it to carry the load current (typically 5 to 8V below ground). In Figure 4 the spike develops 29V across the MOSFET while it carries the full load current. No clamp diode is necessary since the MOSFET performs this task, but safe operating area (SOA) and the additional dissipation should not be forgotten. SOA is often not an issue, such as in this example where the IRF530 can handle 25A at 29V V_{DS} (the load is only 0.5A).

Motors, which are often considered "inductive" loads present a different problem. A spinning motor continues to generate a voltage after the MIC5011 shuts off. In applications where feedback is employed to control the MIC5011, the motor voltage may interfere with the operation of the circuit. The circuits of Figure 5 and "Push Button Control" of Figure 7 will not work with motor loads.

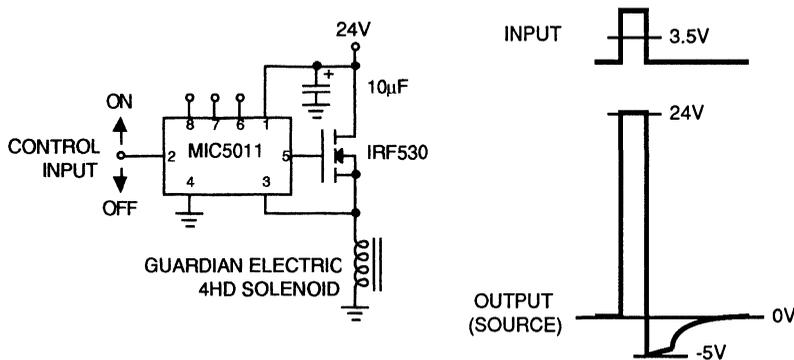


Figure 4. Clamping Inductive Transients

Noise Immunity

In combination with an appropriate power MOSFET, the MIC5011 can control virtually any load that operates on a 4.75 to 32V supply. Aside from the negative spike produced by inductive loads, other pitfalls await the unwary high-side switch designer. For example, ground noise generated when switching a high-power load, especially one with a high inrush current such as an incandescent lamp, can cause oscillations at turn-on or turn-off with slow-moving inputs. Good bypassing is essential; a 10 μ F aluminum electrolytic capacitor is recommended from supply to ground. Don't confuse charge pump action with spurious oscillations. A slight "ripple" (synchronous with the charge pump clock at pin 8) is normally present on the rising edge of the output; rail-to-rail oscillations at the output are indicative of spurious feedback.

Attention should be paid to layout. For example, the

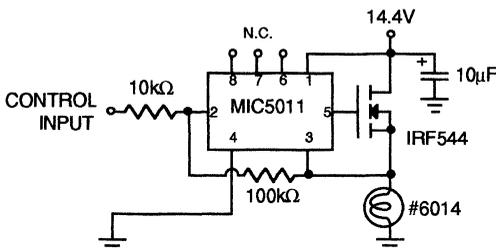


Figure 5. Adding Hysteresis to Suppress Oscillations with Slow-Moving Inputs

MIC5011 ground pin should be returned to the input signal ground, not the load ground. The MIC5011 is non-inverting, and hysteresis is easily added for any load other than a motor (see Figure 5). Any arbitrary noise margin is added by selecting the appropriate resistor ratio.

5V Operation

The MIC5011 is suitable for use in high-side driver circuits down to about 7V. A low-side driver topology works down to 4.75V, and is suitable for operation on a 5V logic supply. Figure 6 shows a complete low-side driver for use on 4.75 to 15V supplies. Pin 3 is grounded to clamp the gate potential at 12.5V.

Only the power MOSFET breakdown ratings limit the load voltage. In fact, half- or full-wave rectified ac could be applied to the load where economy is important. Don't forget to add a clamp diode to inductive loads.

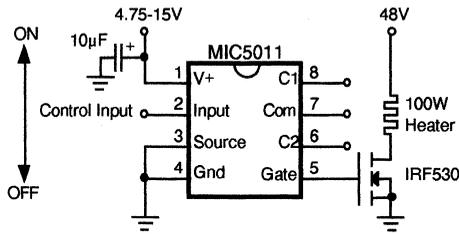
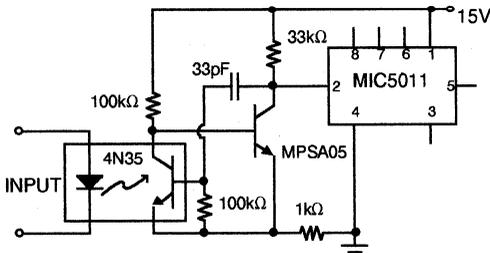


Figure 6. Low-Side Driver

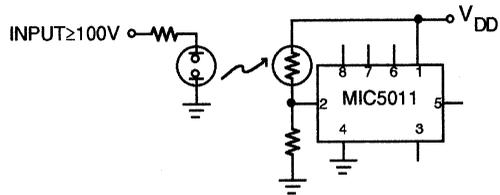
Control Inputs

The MIC5011 is easily interfaced to any control signal. The input threshold is approximately 3.5V, and the input current is less than 1 μ A. Some examples of typical control inputs are shown in Figure 7. For industrial applications, electrical isolation may be desirable for either safety or noise reasons. Opto-isolators are a good choice for this use and with the hysteresis circuit shown, they provide clean switching. High voltages can be sensed and acted upon with a neon light and a light-dependent resistor.

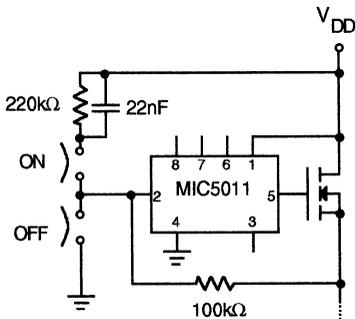
Familiar momentary "ON/OFF" push buttons are easily accommodated as shown. The "ON" button is AC coupled so that any contention between the "ON" and "OFF" buttons is resolved in favor of the "OFF" button. Hysteresis is used to latch the output into the appropriate state. 5V logic commands are interfaced by a CMOS gate. Since the MIC5011 input includes electrostatic discharge protection to the supply, the logic gate should not be powered from a supply higher than V_{DD} .



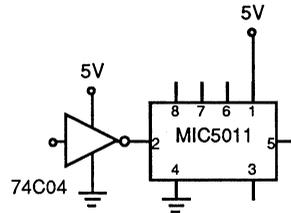
OPTICALLY ISOLATED INPUT



HIGH VOLTAGE INPUT (POSITIVE OR NEGATIVE POLARITY)



PUSH BUTTON CONTROL



5V LOGIC INTERFACE

Figure 7. Various Interface Circuits

Introduction

In battery powered applications, such as laptop computers, power control has a major impact on battery life. For example, laptop or notebook computers often have a "sleep" mode, where the hard drive spins down and the display backlighting turns off while the RAM—containing valuable user data—is maintained. A microprocessor can easily make such power management decisions, but implementing the hardware for

the actual switching can be complicated. "High-side" switching is required; i.e., the positive supply voltage must be controlled. Common grounds for busses and shielding limits the possibility of "low side" switching in a standard negative ground system. This note discusses a logic controlled power switch that simplifies microprocessor driven high-side supply switching.

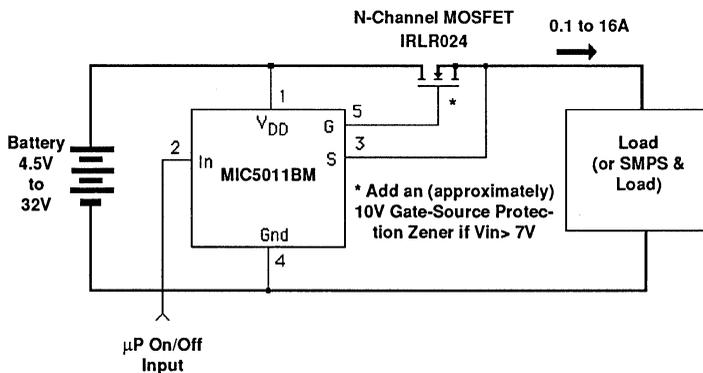


Figure 1. MIC5011 DB-1 Schematic Diagram.

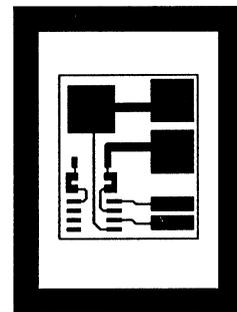


Figure 2. MIC5011 DB-1 Low Voltage Logic Controlled Power Switch

2

Power Switches

These high-side implementations have historically taken one of two forms: relays or PNP transistors. Both have drawbacks in that relatively large drive current is required: neither can be switched directly from a microprocessor port or standard logic. Mechanical relays are bulky, expensive, and have limited lifetimes. Bipolar transistors exhibit a fixed voltage drop that reduce margins, especially in 5V logic systems. This voltage drop has a devastating effect on

defining battery end-of-life (per charge cycle).

Another method of power switching is the N-Channel DMOS FET. This FET has no inherent voltage drop, except for the $I \times r_{DS}$ loss, and requires almost no drive power; unfortunately, it does need a gate driving voltage of from 4V to 10V above the supply voltage in high-side applications. In other words, it is an *almost* ideal switch.

DMOS FET Advantages vs. Relays

- Non-mechanical (much longer life)
- No contact bounce
- Extremely low drive current requirement
- Smaller Size
- Lighter weight
- Lower cost

DMOS FET Advantages vs. PNP

- No fixed voltage drop
- Extremely low drive current requirement
- Larger Safe Operating Region

The Micrel MIC5010 Family

The MIC5011, and its relatives, controls the N-Channel DMOS FET by generating a gate drive control voltage 4V to 10V above the supply. Its CMOS compatible control input directly interfaces with microprocessors, and its BCD (Bipolar-CMOS-DMOS) construction allows nearly zero power drain in the OFF state. Pairing the MIC5011 with a low cost DMOS FET gives you a simple, reliable, easy-to-interface method of power management.

The MIC5011 is designed for this application and features:

- 4.5V to 32V Operation
- Very low OFF power consumption—0.1 μ A typical
- No external components required
- Built-in zener clamp for protecting standard DMOS gates
- Available in small 8-pin surface mount packages

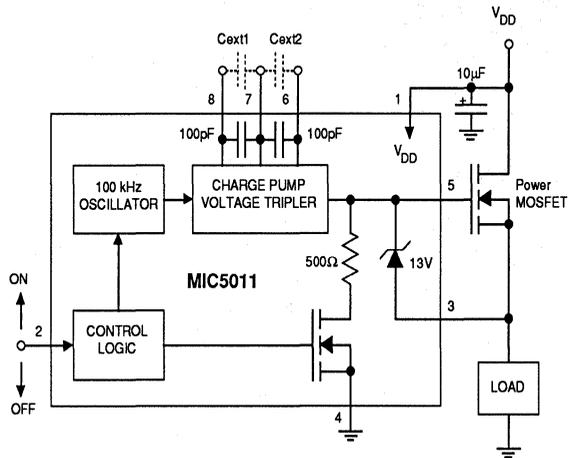
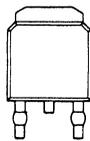


Figure 3. MIC5011 Block Diagram and Typical Application



G D S

Figure 4. IRLR024 DMOS FET

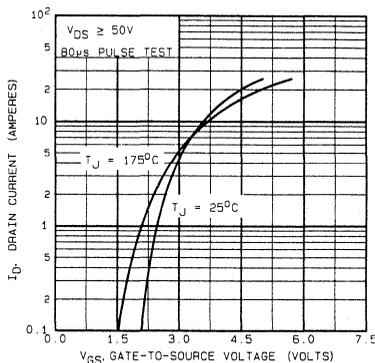


Figure 5. IRLR024 Characteristics

The IRLR024 N-Channel DMOS FET

The 100m Ω surface mount IRLR024 is employed as the pass device in this demonstration circuit. This N-Channel DMOS FET features “Logic Level” gate drive voltages and can pass over 50A of peak current (limited by power dissipation considerations). Key features include:

- Low ON resistance—100m Ω maximum
- “Logic Level” gate threshold—ON at VGS=4V; VGS=5V for full enhancement.
- High pass current
- Surface mount package

One drawback of this “logic level” device is that its sensitive gate cannot withstand more than 10V of VGS drive. Although the MIC5011 includes a protective zener clamp, the zener’s 12.5V threshold is inadequate. With supply voltages from 4.5V to 7V, this is not a problem; however, above 7V, either an external zener clamp must be added to the MIC5011 gate drive output or else a standard threshold FET should be used.

The Micrel MIC5011 DB-1 Demonstration Unit

This demonstration unit is built on a single sided board using surface mount techniques. It has been designed to control 4.5V to 7V supplies, but can easily be modified to use 4.5V to 32V supply voltages. The first thing you will notice from the schematic, Figure 1, is its simplicity; only two components are needed. The MIC5011 contains all of the necessary intelligence and the drive circuitry required by the N-Channel DMOS FET.

Four lines provide +Vcc, Switched-Vcc, Control, and Ground. Vcc and Switched-Vcc are current carrying lines, so thick, low resistances traces are necessary. Both Control and Ground are low current lines, so thin traces are sufficient.

Simply connect Vcc to 4.5V to 7V, Switched-Vcc to your load, Control to a logic output, and Ground. When the logic level is high (greater than approximately 3.5V), the load will be energized. The IRLR024 will exhibit less than 100mΩ of resistance, so voltage drop, hence power loss, with typical peripherals will be low. Current drain of up to 16A continuous, 64A peak, can be drawn with suitable heatsinking (limit current to 4A without additional heatsinking). With a low logic level, the load will be switched off. Total power drain from the Vcc line will be negligible; only approximately 0.1μA (leakage current) flows.

Application Notes

Operating Voltages

This circuit, as designed, controls 4.5V to 7V digital supply voltages. If higher voltages must be switched, one of two modifications must be made. To switch widely varying supplies in the 4.5V to 32V range, use an approximately 7.5V zener clamp, such as the MLL4693 or equivalent, across the gate and source of the FET. If your application switches 7V to 32V, replace the "logic level" FET with a standard gate N-Channel DMOS FET, such as the IRF540, BUZ1LS2, or the SMP60N05. Regardless of the operating voltage or FET employed, the MIC5011 allows power control from a standard CMOS-level logic signal.

Faster Switching

If switching time is critical, adding a 1000pF capacitor from pins 6-7 on the MIC5011 will help. Another 1000pF capacitor from pins 7-8 will further accelerate switching time, but by a smaller margin.

Dual Independent Switches

When two separate circuits require switching, the MIC5012 Dual High Side FET Driver provides two independent drivers in a single 14-pin DIP or 16-pin surface mount package.

Current Limiting

Replace the MIC5011 with the MIC5013 to enable current limiting. See the MIC5013 datasheet for information.

Parts List

- MIC5011BM Surface mount MOSFET driver
- IRLR024 Surface mount DMOS FET
- MLL4693 Surface mount 7.5V zener diode (optional)



Figure 6. MIC5011 DB-1 Board Layout

Additional Notes

Although the MIC5011 datasheet specifically states that a minimum of 7V of supply voltage is required for high-side driving, the introduction of “logic level” N-Channel DMOS FETs requiring only 4V to 5V V_{GS} for full ON operation enables this minimum operating voltage to be lowered. The MIC5011 provides gate enhancement with supply voltages down to below 3.5V. Variations in the control voltage threshold, however, restrict low voltage operations to somewhat less than 4.5V.



MIC5012

Dual Power MOSFET Predriver

General Description

The MIC5012 is the dual member of the Micrel MIC501X predriver family. These ICs are designed to drive the gate of an N-channel power MOSFET above the supply rail in high-side power switch applications. The 14-pin MIC5012 is extremely easy to use, requiring only a power FET and nominal supply decoupling to implement either a high- or low- side switch.

The MIC5012 charges a 1 nF load in 60 μ S typical. Operation down to 4.75V allows the MIC5012 to drive standard MOSFETs in 5V low-side applications by boosting the gate voltage above the logic supply. In addition, multiple, paralleled MOSFETs can be driven by a single MIC5012 for ultra-high current applications.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5011 minimum parts count predriver, and MIC5013 protected 8 pin predriver.

Features

- 4.75V-32V operation
- 2 independent predrivers; implements high and low side drivers
- Less than 1 μ A standby current in the 'off' state per channel
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- Minimum external parts count
- Can be used to boost drive to low-side power FETs operating on logic supplies
- Independent supply pins for half-bridge applications

Applications

- Lamp drivers
- Motion Control
- Heater switching
- Power bus switching
- Half or full H-bridge drivers

Typical Applications

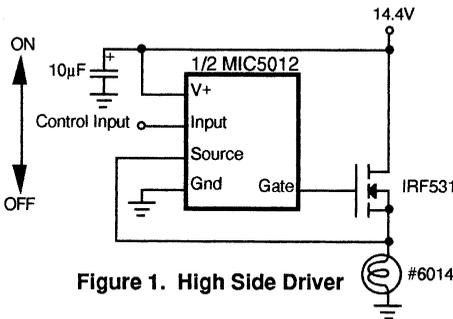


Figure 1. High Side Driver

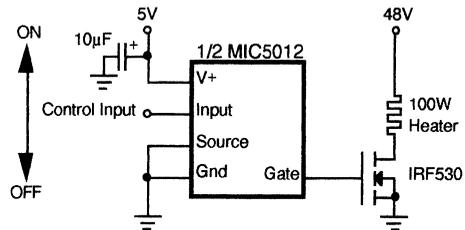


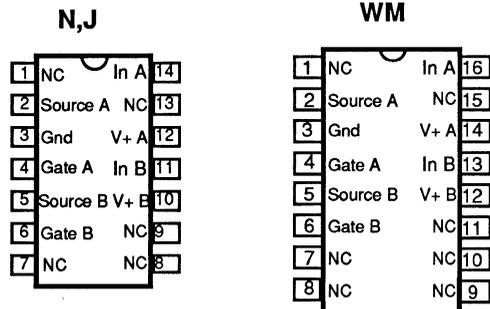
Figure 2. Low Side Driver

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC5012BN	-40°C to +85°C	14-pin Plastic DIP
MIC5012BJ	-40°C to +85°C	14-pin Ceramic DIP
MIC5012BWM	-40°C to +85°C	16-pin Wide SOIC
MIC5012AJ	-55°C to +125°C	14-pin Ceramic DIP
MIC5012AJB	-55°C to +125°C	14-pin Ceramic DIP

Protected under one or more of the following Micrel patents:
 patent #4,951,101; patent # 4,914,546

Connection Diagram



Note: The MIC5012 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Supply Voltage (V ⁺), Pins 10, 12	-0.5V to 36V
Input Voltage, Pins 11, 14	-10V to V ⁺
Source Voltage, Pins 2, 5	-10V to V ⁺
Current into Pins 2, 5	50 mA
Gate Voltage, Pins 4, 6	-1V to 50V
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Power Dissipation	1.56W
θ_{JA} (Plastic DIP)	80°C/W
θ_{JA} (Ceramic DIP)	105°C/W
θ_{JA} (SOIC)	105°C/W
Ambient Temperature: B version	-40°C to +85°C
Ambient Temperature: A version	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature	260°C
(Soldering, 10 seconds)	
Supply Voltage (V ⁺), Pin 1	7V to 32V high side 4.75V to 15V low side

Electrical Characteristics (Note 3) Test circuit, per channel, T_A=-55°C to +125°C, V⁺=15V, all switches open, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units	
Supply Current	V ⁺ =32V V _{IN} =0V, V _S =0V, S2 closed		0.1	10	μA	
	V _{IN} =V _S =32V		8	20	mA	
Logic Input Voltage Threshold, V _{IN} (Note 5)	V ⁺ =4.75V Adjust V _{IN} for V _{GATE} low			2	V	
	Adjust V _{IN} for V _{GATE} high	4.5				
	V ⁺ =15V Adjust V _{IN} for V _{GATE} high			5		
Logic Input Current, I _{IN}	V ⁺ =32V V _{IN} =0V	-1			μA	
	V _{IN} =32V			1		
Input Capacitance	Pins 11, 14		5		pF	
Gate Drive, V _{GATE}	S1, S2 closed, V _S =V ⁺	V ⁺ =4.75V, I _{GATE} =0, V _{IN} =4.5V	7	10	V	
		V ⁺ =15V, I _{GATE} =100 μA, V _{IN} =5V	24	27		
Zener Clamp V _{GATE} -V _{SOURCE}	S2 closed, V _{IN} =5V	V ⁺ =15V, V _S =15V	11	12.5	15	V
		V ⁺ =32V, V _S =32V	11	13	16	
Gate Turn-on Time, t _{ON} (Note 4)	V _{IN} switched from 0 to 5V; measure time for V _{GATE} to reach 20V		60	200	μS	
Gate Turn-off Time, t _{OFF}	V _{IN} switched from 5 to 0V; measure time for V _{GATE} to reach 1V		4	10	μS	

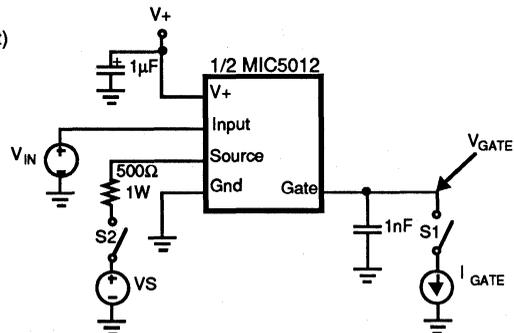
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2: The MIC5012 is ESD sensitive.

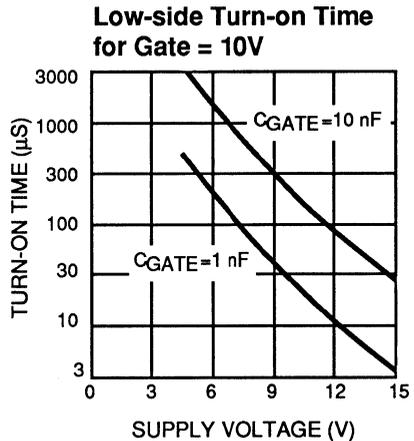
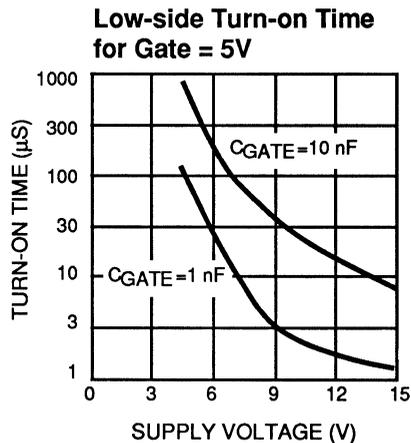
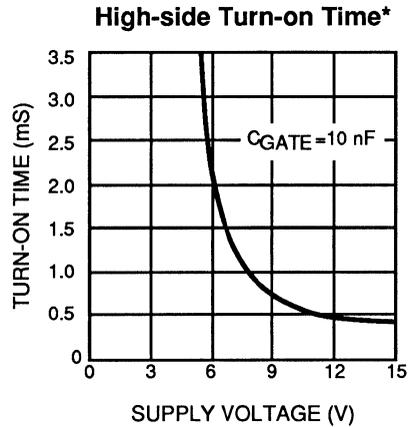
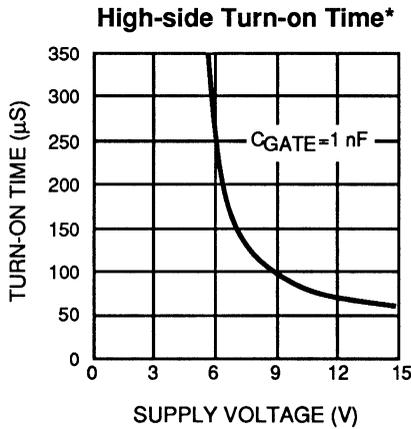
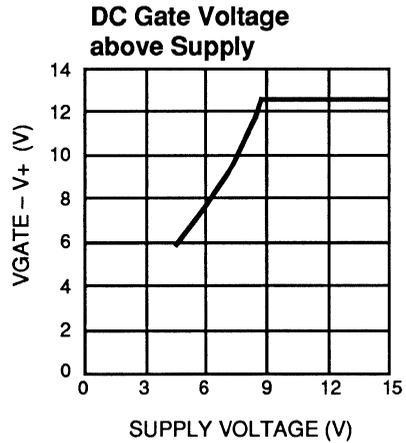
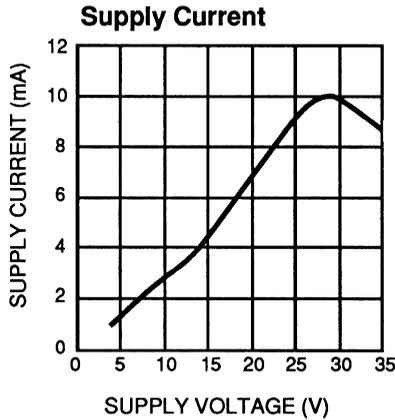
Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at T_A=25°C and T_A=85°C(125°C for A version), and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster-see **Applications Information**. Maximum value of switching speed seen at 125°C, units operated at room temperature will reflect the typical value shown.

Note 5: Specially sorted units with V_{IN} max (for a gate low output) of 3.5 V are available.

Test Circuit

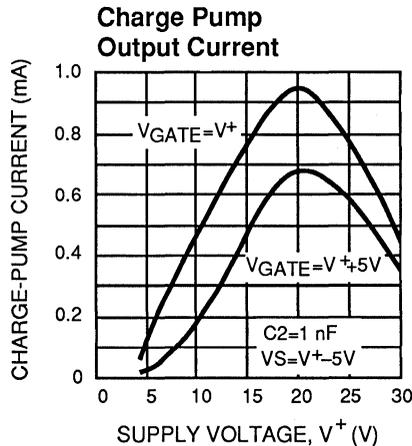
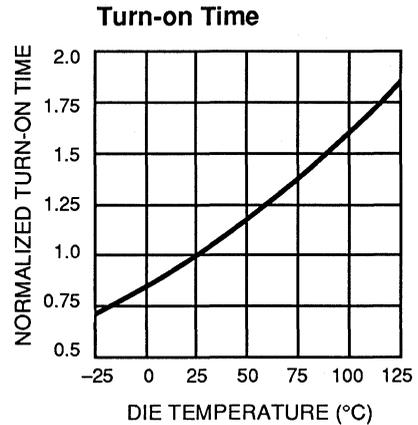
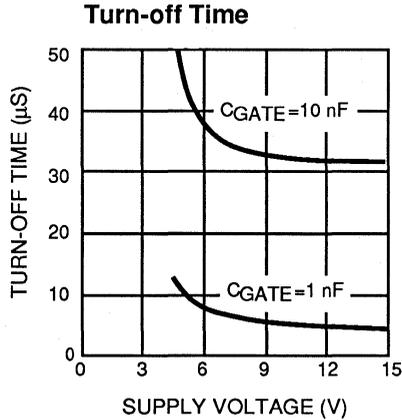
Typical Characteristics (per channel)



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* Time for gate voltage to reach V+ + 5V in test circuit with VS = V+ - 5V (prevents gate clamp from interfering with measurement).

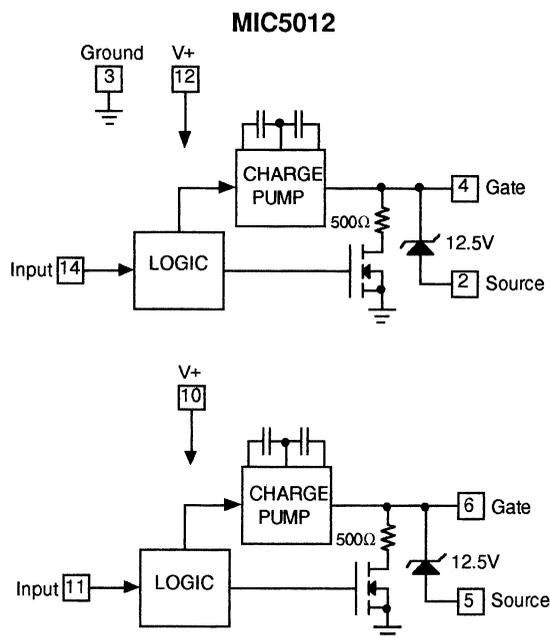
Typical Characteristics (Continued)



Pin Description (Refer to Typical Applications)

Pin Number	Pin Name	Pin Function
12, 10	V^+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. 10 μF is recommended close to the chip.
14, 11	Input	Turns on power MOSFET when taken above threshold (3.5V typical). Requires <1 μA to switch.
2, 5	Source	Connects to source lead of power FET and is the return for the gate clamp zener. Source pin can safely swing to -10V when turning off inductive loads.
3	Ground	Both channels share a common ground at pin 3
4, 6	Gate	Drives and clamps the gate of the power FET. The gate pin will be clamped to approximately -0.7V by an internal diode when turning off inductive loads.

Block Diagram



Applications Information

Functional Description (Refer to Block Diagram)

The MIC5012 consists of two independent predrivers sharing a common ground. The functions are controlled via a logic block connected to the logic input. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET.

The charge pump incorporates a 100 kHz oscillator and on-chip pump capacitors capable of charging 1 nF to 5V above supply in 60 μS typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin and source pin to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

Since the supply pins are independent, the two predrivers contained in the MIC5012 can be operated from separate supplies of different values (see Figure 6).

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal, low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: *Supplies:*

Applications Information (Continued)

many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Always monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components—especially electrolytic capacitors—with possibly catastrophic results. A 10 μF supply bypass capacitor *at the chip* is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50 mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100 mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5012 is suited for use with standard MOSFETs in high- or low-side driver applications. In addition, the MIC5012 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in Figure 1) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types (Figures 2 and 4). Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10 μs to $V_{GS}=1V$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics.

High-Side Driver (Figure 1). The high-side topology works well down to $V^+=7V$ with standard MOSFETs. From 4.75 to 7V supply, a logic-level MOSFET can be substituted since the MIC5012 will not reach 10V gate enhancement (10V is the maximum rating for logic-compatible MOSFETs).

High-side drivers implemented with MIC501X predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the MIC5012 holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5012 source pin is designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Applications Information (Continued)

Low-Side Driver (Figure 2). A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5012 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener. The switching speed to 10V enhancement is 300 μ S driving 1 nF on a 5V supply. On a 15V supply the turn-on time is less than 2 μ S to 10V

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μ S or less on a 12 to 15V supply.

Modifying Switching Times. Do not add external capacitors to the MOSFET gate. Add a resistor (1 k Ω to 51 k Ω) in series with the gate to slow down the switching time.

Bootstrapped High-Side Driver (Figure 3). The speed of a high-side driver can be increased to better than 10 μ S by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100 Hz to 20 kHz), or where it is energized continuously. The Schottky barrier diode prevents the MIC5012 supply pin from dropping more than 200 mV below the drain supply, and it also improves turn-on time on supplies of less than 10V. Since the supply current in the "off" state is only a small leakage, the 100 nF bypass capacitor tends to remain charged for several seconds after the MIC5012 is turned off. In a PWM application the chip supply is sustained at a higher potential than the system supply, which improves switching time.

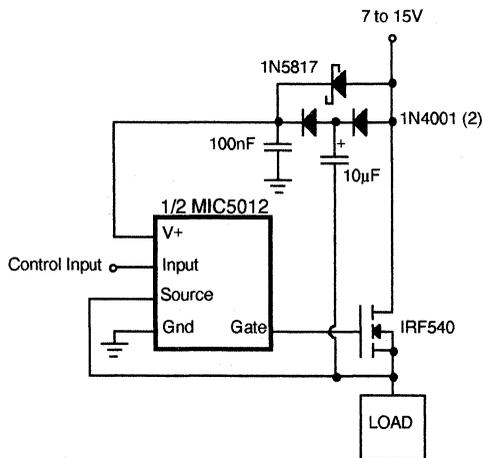


Figure 3. Bootstrapped High-Side Driver

Opto-Isolated Interface (Figure 4). Although the MIC5012 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscilla-

tions on the rise and fall of the output. The circuit shown accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5012 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5012 will turn OFF.

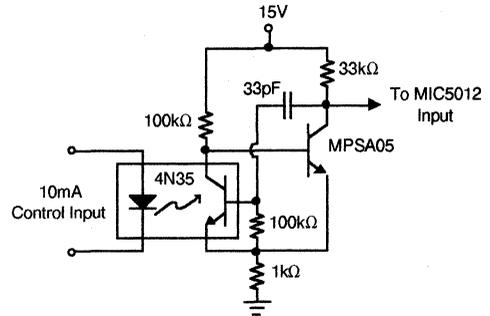


Figure 4. Improved Opto-Isolator Performance

Industrial Switch (Figure 5). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if both switches close simultaneously, the "off" button has precedence.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

Half-Bridge Motor Driver (Figure 6). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20 kHz range.

The circuit of Figure 6 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2-3 μ S dead time effectively eliminating cross conduction. Two of these circuits can be connected together to form an H-bridge for locked antiphase or sign/magnitude control.

Time-Delay Relay (Figure 7). The MIC5012 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100 k Ω /1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system. Hysteresis has been added to guarantee clean switching at turn-on.

Applications Information (Continued)

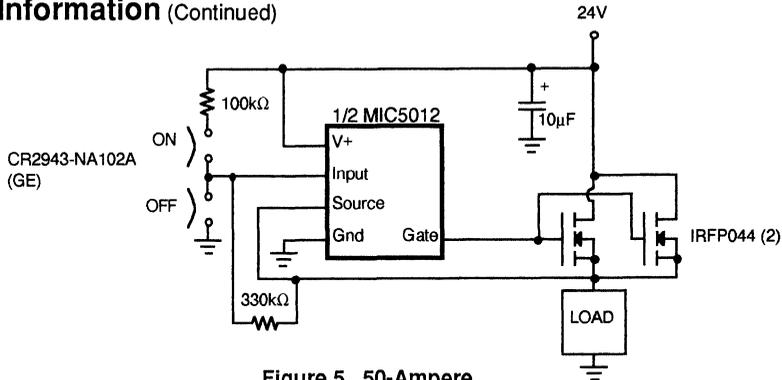


Figure 5. 50-Ampere Industrial Switch

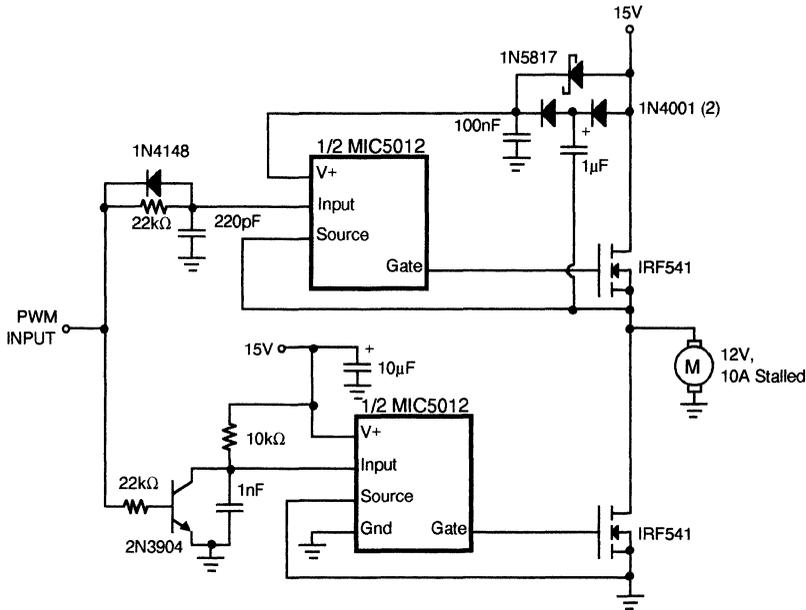


Figure 6. Half-Bridge Motor Driver

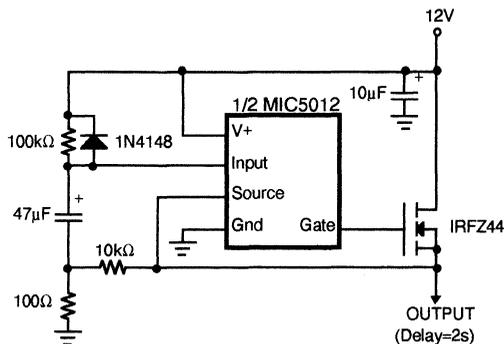


Figure 7. 30 Ampere Time-Delay Relay

2

Applications Information (Continued)

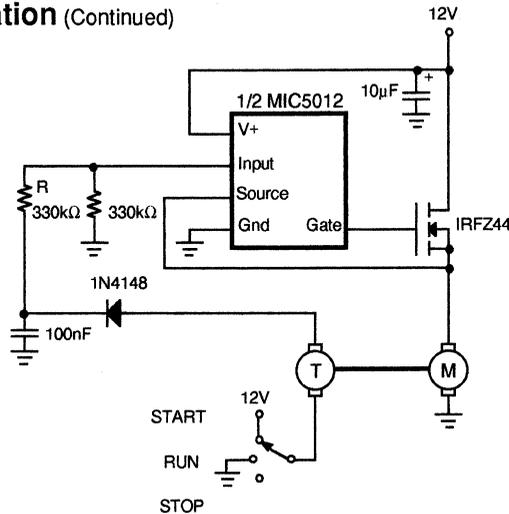


Figure 8. Motor Stall Shutdown

Motor Driver with Stall Shutdown (Figure 8). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5012 input ON. If the motor slows down, the tach output is reduced, and the MIC5012 switches OFF. Resistor "R" sets the shutdown threshold.

Electronic Governor (Figure 9). The output of an ac tachometer can be used to form a PWM loop to maintain the speed of a motor. The tachometer output is rectified, partially filtered, and fed back to the input of the MIC5012. When the motor is stalled there is no tachometer output, and MIC5012 input is pulled high delivering full power to

the motor. If the motor spins fast enough, the tachometer output is sufficient to pull the MIC5012 input low, shutting the output off. Since the rectified waveform is only partially filtered, the input oscillates around its threshold causing the MIC5012 to switch on and off at the frequency of the tachometer signal. A PWM action results since the average dc voltage at the input decreases as the motor spins faster. The $1k\Omega$ potentiometer is used to set the running speed of the motor. Loop gain (and speed regulation) is increased by increasing the value of the 100 nF filter capacitor.

The performance of such a loop is imprecise, but stable and inexpensive. A more elaborate loop would consist of a PWM controller and a half-bridge.

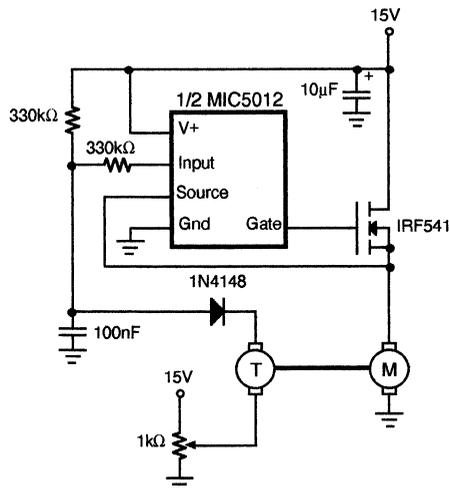


Figure 9. Electronic Governor

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5012, it is helpful to understand the operation of the gate control circuitry (see Figure 12). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5012 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5012 is commanded on, and Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing C2 above supply (charge is dumped into

the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5012 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5012 operate quickly in low-side applications. In high-side applications Q5 pre-charges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

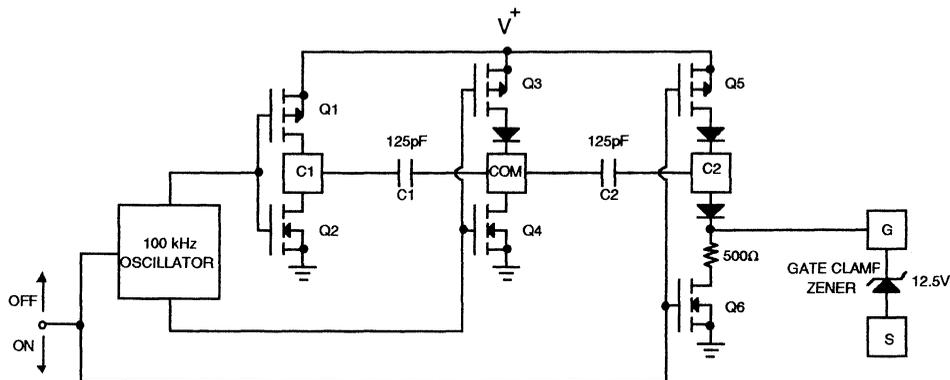


Figure 10. Gate Control Circuit Detail

General Description

The MIC5013 is an 8-pin MOSFET predriver with over-current shutdown and a fault flag. It is designed to drive the gate of an N-channel power MOSFET above the supply rail high-side power switch applications. The MIC5013 is compatible with standard or current-sensing power MOSFETs in both high- and low-side driver topologies.

The MIC5013 charges a 1 nF load in 60 μ S typical and protects the MOSFET from over-current conditions. The current sense trip point is fully programmable and a dynamic threshold allows high in-rush current loads to be started. A fault pin indicates when the MIC5013 has turned off the FET due to excessive current.

Other members of the Micrel predriver family include the MIC5010 full-featured predriver, MIC5011 minimum parts count predriver, and MIC5012 dual predriver.

Features

- 7V-32V operation
- Less than 1 μ A standby current in the 'off' state
- MIL-STD-883 Method 5004/5005 version available
- Available in small outline SOIC packages
- Internal charge pump to drive the gate of an N-channel power FET above supply
- Internal zener clamp for gate protection
- 60 μ S typical turn-on time to 50% gate overdrive
- Programmable over-current sensing
- Dynamic current threshold for high in-rush loads
- Fault output pin indicates current faults
- Implements high- or low-side switches

Applications

- Lamp drivers
- Relay and solenoid drivers
- Heater switching
- Power bus switching
- Motion control

Typical Application

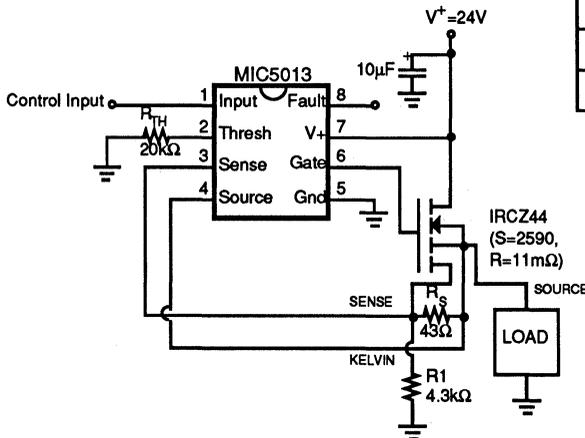


Figure 1. High-Side Driver with Current-Sensing MOSFET

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC5013BN	-40°C to +85°C	8-pin Plastic DIP
MIC5013BJ	-40°C to +85°C	8-pin Ceramic DIP
MIC5013BM	-40°C to +85°C	8-pin SOIC
MIC5013AJ	-55°C to +125°C	8-pin Ceramic DIP
MIC5013AJB	-55°C to +125°C	8-pin Ceramic DIP

$$R_s = \frac{SR(V_{TRIP} + 100mV)}{R_L - (V_{TRIP} + 100mV)}$$

$$R_1 = \frac{V^+ SRR_s}{100mV (SR + R_s)}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 30A \text{ (trip current)}$$

$$V_{TRIP} = 100mV$$

Protected under one or more of the following Micrel patent #4,951,101; patent # 4,914,546

Note: The MIC5013 is ESD sensitive.

Absolute Maximum Ratings (Note 1, 2)

Input Voltage, Pin 1	-10 to +V ⁺
Threshold Voltage, Pin 2	-0.5 to +5V
Sense Voltage, Pin 3	-10V to V ⁺
Source Voltage, Pin 4	-10V to V ⁺
Current into Pin 4	50 mA
Gate Voltage, Pin 6	-1V to 50V
Supply Voltage (V ⁺), Pin 7	-0.5V to 36V
Fault Output Current, Pin 8	-1 mA to +1 mA
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Power Dissipation	1.25W
θ_{JA} (Plastic DIP)	100°C/W
θ_{JA} (Ceramic DIP)	125°C/W
θ_{JA} (SOIC)	170°C/W
Ambient Temperature: B version	-40°C to +85°C
Ambient Temperature: A version	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Supply Voltage (V ⁺), Pin 1	7V to 32V high side 7V to 15V low side

Electrical Characteristics (Note 3) Test circuit, T_A = -55°C to +125°C, V⁺ = 15V, all switches open, unless otherwise specified.

Parameter	Conditions		Min	Typ	Max	Units
Supply Current, I ₇	V ⁺ = 32V	V _{IN} = 0V, S4 closed		0.1	10	μA
		V _{IN} = V _S = 32V, I ₂ = 200 μA		9	20	mA
Logic Input Voltage Threshold, V _{IN}	Adjust V _{IN} for V _{GATE} low				2	V
	Adjust V _{IN} for V _{GATE} high		4.5			
Logic Input Current, I ₁	V ⁺ = 32V	V _{IN} = 0V	-1			μA
		V _{IN} = 32V			1	
Input Capacitance	Pin 1			5		pF
Gate Drive, V _{GATE}	S1, S2 closed, V _{IN} = 5V, V _S = V ⁺	V ⁺ = 7V, I ₆ = 0	13	15		V
		V ⁺ = 15V, I ₆ = 10 μA	24	27		
Zener Clamp, V _{SENSE} - V _{SOURCE}	S2 closed, V _{IN} = 5V	V ⁺ = 15V, V _S = 15V	11	12.5	15	V
		V ⁺ = 32V, V _S = 32V	11	13	16	
Gate Turn-on Time, t _{ON}	V _{IN} switched from 0 to 5V; measure time for V _{GATE} to reach 20V			60	200	μS
Gate Turn-off Time, t _{OFF}	V _{IN} switched from 5 to 0V; measure time for V _{GATE} to reach 1V			4	10	μS
Threshold Bias Voltage, V ₂	I ₂ = 200 μA		1.7	2	2.2	V
Current Sense Trip Voltage, V _{SENSE} - V _{SOURCE}	S2 Closed, V _{IN} = 5V, Increase I ₃	V ⁺ = 7V, S4 closed	75	105	135	mV
		I ₂ = 100 μA, V _S = 4.9V	70	100	130	
		V ⁺ = 15V, S4 closed	150	210	270	
		I ₂ = 200 μA, V _S = 11.8V	140	200	260	
		V ⁺ = 32V, V _S = 0V	360	520	680	
Peak Current Trip Voltage, V _{SENSE} - V _{SOURCE}	S3, S4 closed, V ⁺ = 15V, V _{IN} = 5V	I ₂ = 500 μA, V _S = 25.5V	350	500	650	V
			1.6	2.1		
Fault Output Voltage, V ₈	V _{IN} = 0V, I ₈ = -100 μA			0.4	1	V
	V _{IN} = 5V, I ₈ = 100 μA, current sense tripped		14	14.6		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

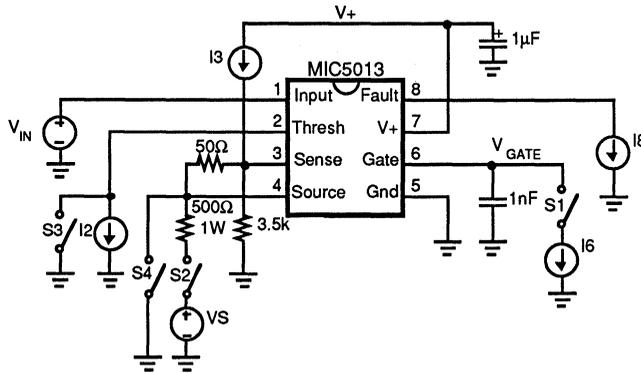
Note 2: The MIC5013 is ESD sensitive.

Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C (125°C for A version), and 100% guaranteed over the entire operating temperature range. Typicals are characterized at 25°C and represent the most likely parametric norm.

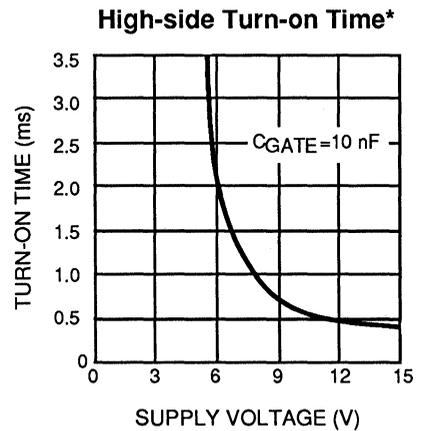
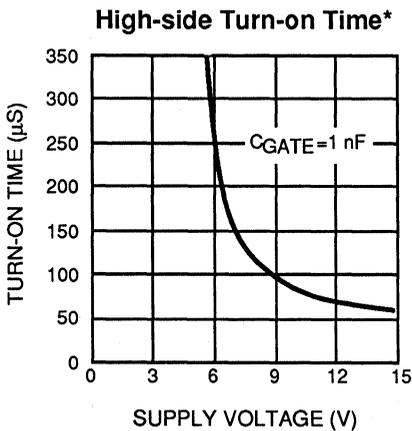
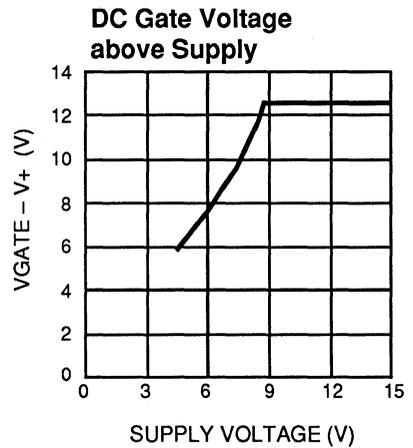
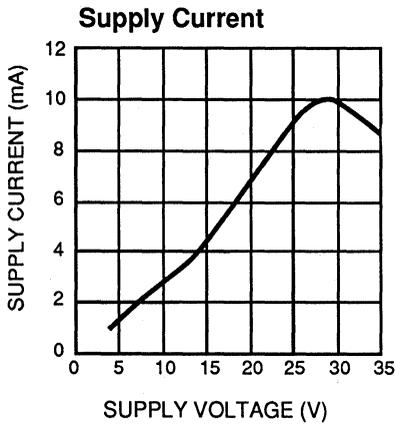
Note 4: Test conditions reflect worst case high-side driver performance. Low-side and bootstrapped topologies are significantly faster—see **Applications Information**. Maximum value of switching speed seen at 125°C, units operated at room temperature will reflect the typical value shown.

Note 5: Specially sorted units with V_{IN} max (for a gate low output) of 3.5V are available. Contact factory for details.

Test Circuit



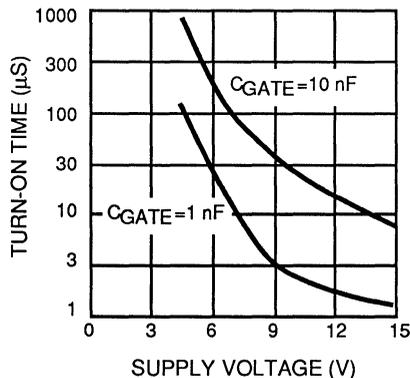
Typical Characteristics



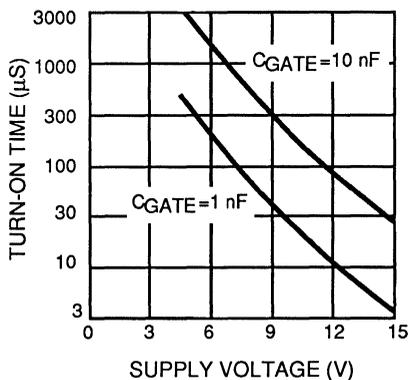
* Time for gate voltage to reach V+ + 5V in test circuit with VS = V+ - 5V (prevents gate clamp from interfering with measurement).

Typical Characteristics (Continued)

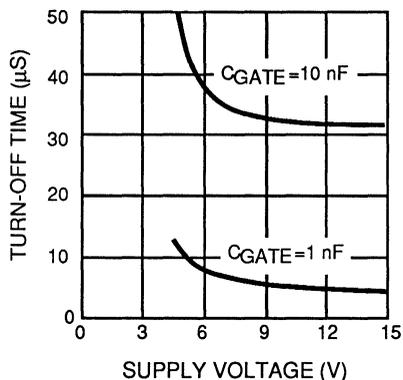
Low-side Turn-on Time for Gate = 5V



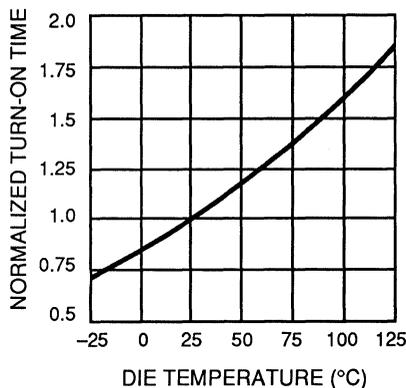
Low-side Turn-on Time for Gate = 10V



Turn-off Time

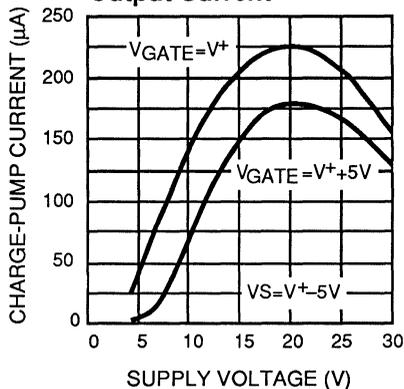


Turn-on Time



2

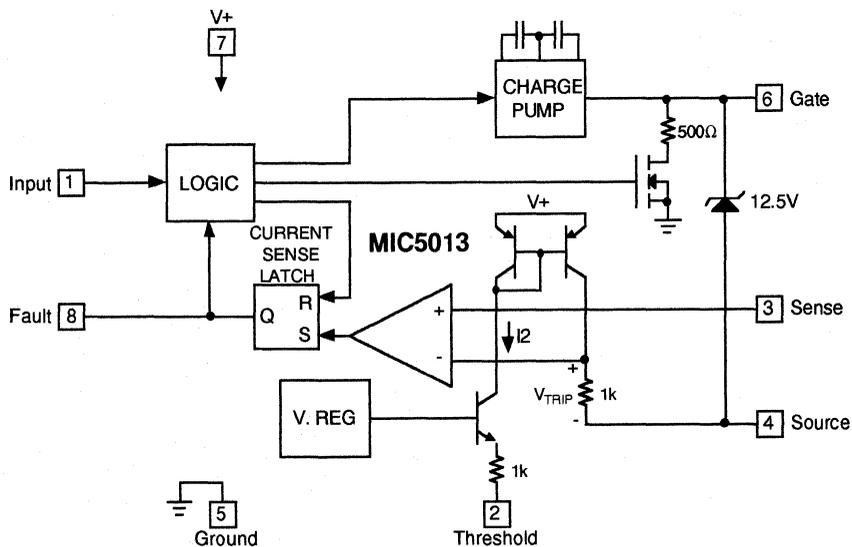
Charge Pump Output Current



Pin Description (Refer to Figures 1 and 2)

Pin Number	Pin Name	Pin Function
1	Input	Resets current sense latch and turns on power MOSFET when taken above threshold (3.5V typical). Pin 1 requires <math>< 1 \mu\text{A}</math> to switch.
2	Threshold	Sets current sense trip voltage according to: $V_{\text{TRIP}} = \frac{2200}{R_{\text{TH}} + 1000}$ where R_{TH} to ground is 3.3k to 20k Ω . Adding capacitor C_{TH} increases the trip voltage at turn-on to 2V. Use $C_{\text{TH}} = 10 \mu\text{F}$ for a 10 ms turn-on time constant.
3	Sense	The sense pin causes the current sense to trip when V_{SENSE} is V_{TRIP} above V_{SOURCE} . Pin 3 is used in conjunction with a current shunt in the source of a 3 lead FET or a resistor R_{S} in the sense lead of a current sensing FET.
4	Source	Reference for the current sense voltage on pin 3 and return for the gate clamp zener. Connect to the load side of current shunt or kelvin lead of current sensing FET. Pins 3 and 4 can safely swing to -10V when turning off inductive loads.
5	Ground	
6	Gate	Drives and clamps the gate of the power FET. Pin 6 will be clamped to approximately -0.7V by an internal diode when turning off inductive loads.
7	V+	Supply pin; must be decoupled to isolate from large transients caused by the power FET drain. $10 \mu\text{F}$ is recommended close to pins 7 and 5.
8	Fault	Outputs status of protection circuits when pin 1 is high. V8 low indicates normal operation ; V8 high indicates current sense tripped.

Block Diagram



Applications Information

Functional Description (refer to block diagram)

The various MIC5013 functions are controlled via a logic block connected to the input pin 1. When the input is low, all functions are turned off for low standby current and the gate of the power MOSFET is also held low through 500Ω to an N-channel switch. When the input is taken above the turn-on threshold (3.5V typical), the N-channel switch turns off and the charge pump is turned on to charge the gate of the power FET. A bandgap type voltage regulator is also turned on which biases the current sense circuitry.

The charge pump incorporates a 100 kHz oscillator and on-chip pump capacitors capable of charging 1 nF to 5V above supply in 60 μS typical. The charge pump is capable of pumping the gate up to over twice the supply voltage. For this reason, a zener clamp (12.5V typical) is provided between the gate pin 6 and source pin 4 to prevent exceeding the V_{GS} rating of the MOSFET at high supplies.

The current sense operates by comparing the sense voltage at pin 3 to an offset version of the source voltage at pin 4. Current I_2 flowing in threshold pin 2 is mirrored and returned to the source via a 1 kΩ resistor to set the offset, or trip voltage. When $(V_{SENSE} - V_{SOURCE})$ exceeds V_{TRIP} , the current sense trips and sets the current sense latch to turn off the power FET. An integrating comparator is used to reduce sensitivity to spikes on pin 3. The latch is reset to turn the FET back on by "recycling" the input pin 1 low and then high again.

A resistor R_{TH} from pin 2 to ground sets I_2 , and hence V_{TRIP} . An additional capacitor C_{TH} from pin 2 to ground creates a higher trip voltage at turn-on, which is necessary to prevent high in-rush current loads such as lamps or capacitors from false-tripping the current sense.

When the current sense has tripped, the fault pin 8 will be high as long as the input pin 1 remains high. However, when the input is low the fault pin will also be low.

Construction Hints

High current pulse circuits demand equipment and assembly techniques that are more stringent than normal low current lab practices. The following are the sources of pitfalls most often encountered during prototyping: *Supplies:* many bench power supplies have poor transient response. Circuits that are being pulse tested, or those that operate by pulse-width modulation will produce strange results when used with a supply that has poor ripple rejection, or a peaked transient response. Monitor the power supply voltage that appears at the drain of a high-side driver (or the supply side of the load in a low-side driver) with an oscilloscope. It is not uncommon to find bench power supplies in the 1 kW class that overshoot or undershoot by as much as 50% when pulse loaded. Not only will the load current and voltage measurements be affected, but it is possible to over-stress various components--especially electrolytic capacitors--with possibly catastrophic results. A 10 μF supply bypass capacitor *at the chip* is recommended.

Residual Resistances: Resistances in circuit connections may also cause confusing results. For example, a circuit may employ a 50 mΩ power MOSFET for low drop, but careless construction techniques could easily add 50 to 100 mΩ resistance. Do not use a socket for the MOSFET. If the MOSFET is a TO-220 type package, make high-current drain connections to the tab. Wiring losses have a profound effect on high-current circuits. A floating millivoltmeter can identify connections that are contributing excess drop under load.

Circuit Topologies

The MIC5013 is suited for use in high- or low-side driver applications with over-current protection for both current-sensing and standard MOSFETs. In addition, the MIC5013 works well in applications where, for faster switching times, the supply is bootstrapped from the MOSFET source output. Low voltage, high-side drivers (such as shown in the **Test Circuit**) are the slowest; their speed is reflected in the gate turn-on time specifications. The fastest drivers are the low-side and bootstrapped high-side types. Load current switching times are often much faster than the time to full gate enhancement, depending on the circuit type, the MOSFET, and the load. Turn-off times are essentially the same for all circuits (less than 10 μS to $V_{GS}=1V$). The choice of one topology over another is based on a combination of considerations including speed, voltage, and desired system characteristics. Each topology is described in this section. Note that I_L , as used in the design equations, is the load current that just trips the over-current comparator.

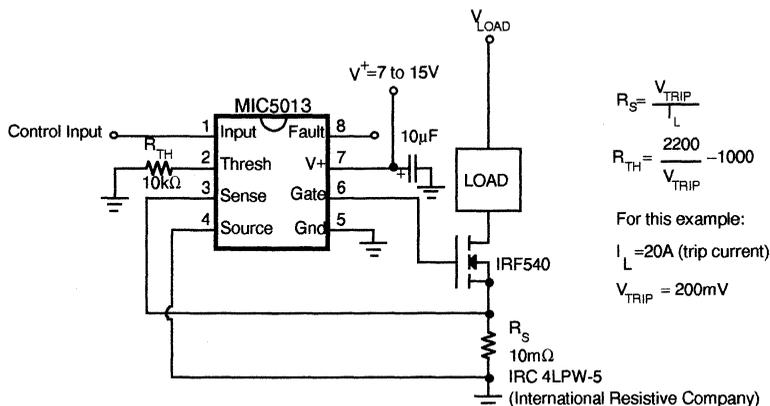
Low-Side Driver with Current Shunt (Figure 2). The over-current comparator monitors R_S and trips if $I_L \times R_S$ exceeds V_{TRIP} . R_{TH} is selected to produce the desired trip voltage.

As a guideline, keep V_{TRIP} within the limits of 100 mV and 500 mV ($R_{TH}=3.3$ kΩ to 21 kΩ). Thresholds at the high end offer the best noise immunity, but also compromise switch drop (especially in low voltage applications) and power dissipation.

The trip current is set higher than the maximum expected load current--typically twice that value. Trip point accuracy is a function of resistor tolerances, comparator offset (only a few millivolts), and threshold bias voltage (V_2). The values shown in Figure 2 are designed for a trip current of 20 amperes. It is important to ground pin 4 *at the current shunt* R_S , to eliminate the effects of ground resistance.

A key advantage of the low-side topology is that the load supply is limited only by the MOSFET BV_{DSS} rating. Clamping may be required to protect the MOSFET drain terminal from inductive switching transients. The MIC5013 supply should be limited to 15V in low-side topologies; otherwise, a large current will be forced through the gate clamp zener.

Applications Information (Continued)



$$R_S = \frac{V_{TRIP}}{I_L}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 20A \text{ (trip current)}$$

$$V_{TRIP} = 200mV$$

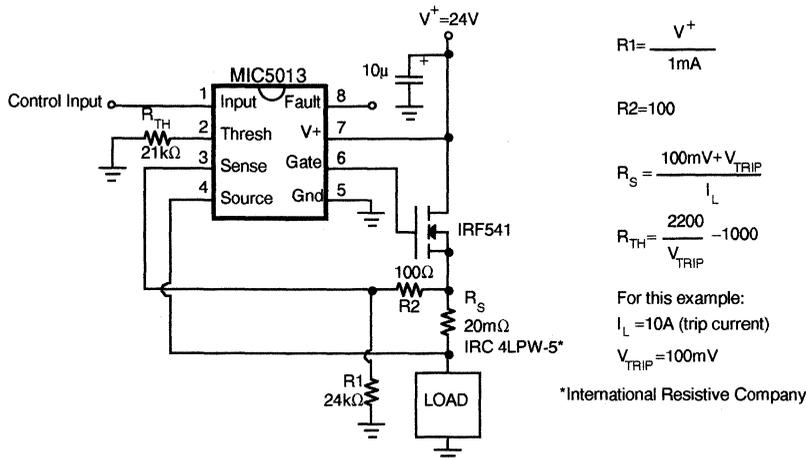
Figure 2. Low-Side Driver with Current Shunt

Low-side drivers constructed with the MIC501X family are also fast; the MOSFET gate is driven to near supply immediately when commanded ON. Typical circuits achieve 10V enhancement in 10 μS or less on a 12 to 15V supply.

High-Side Driver with Current Shunt (Figure 3). The comparator input pins (source and sense) float with the current sensing resistor (R_S) on top of the load. R1 and R2 add a small, additional potential to V_{TRIP} to prevent false-triggering of the over-current shutdown circuit with open or inductive loads. R1 is sized for a current flow of 1 mA, while R2 contributes a drop of 100mV. The shunt voltage should be 200 to 500 mV at the trip point. The example of Figure 3 gives a 10A trip current when the output is near supply. The trip point is somewhat reduced when the output is at ground as the voltage drop across R1 (and therefore R2) is zero.

High-side drivers implemented with MIC5013 predrivers are self-protected against inductive switching transients. During turn-off an inductive load will force the MOSFET source 5V or more below ground, while the predriver holds the gate at ground potential. The MOSFET is forced into conduction, and it dissipates the energy stored in the load inductance. The MIC5013 source and sense pins (3 and 4) are designed to withstand this negative excursion without damage. External clamp diodes are unnecessary.

Current Shunts (R_S). Low-valued resistors are necessary for use at R_S. Values for R_S range from 5 to 50 mΩ, at 2 to 10W. Worthy of special mention are Kelvin-sensed, "four-terminal" units supplied by a number of manufacturers† (see next page). Kelvin-sensed resistors eliminate errors caused by lead and terminal resistances, and simplify product assembly. 10% tolerance is normally adequate,



$$R1 = \frac{V^+}{1mA}$$

$$R2 = 100$$

$$R_S = \frac{100mV + V_{TRIP}}{I_L}$$

$$R_{TH} = \frac{2200}{V_{TRIP}} - 1000$$

For this example:

$$I_L = 10A \text{ (trip current)}$$

$$V_{TRIP} = 100mV$$

*International Resistive Company

Figure 3. High-Side Driver with Current Shunt

Applications Information (Continued)

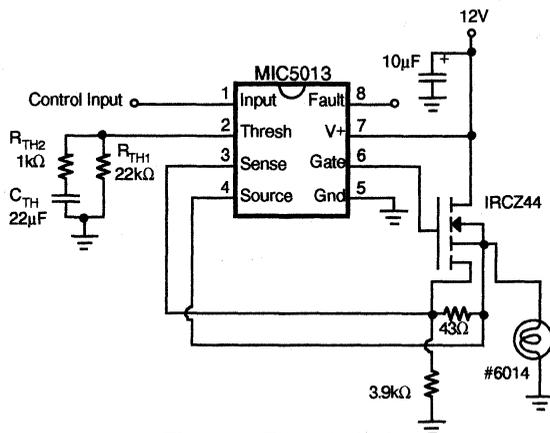


Figure 5. Time-Variable Trip Threshold

Incandescent Lamps. The cold filament of an incandescent lamp exhibits less than one-tenth as much resistance as when the filament is hot. The initial turn-on current of a #6014 lamp is about 70A, tapering to 4.4A after a few hundred milliseconds. It is unwise to set the over-current trip point to 70A to accommodate such a load. A "resistive" short that draws less than 70A could destroy the MOSFET by allowing sustained, excessive dissipation. If the over-current trip point is set to less than 70A, the MIC5013 will not start a cold filament. The solution is to start the lamp with a high trip point, but reduce this to a reasonable value after the lamp is hot.

The MIC5013 over-current shutdown circuit is designed to handle this situation by varying the trip point with time (see Figure 5). R_{TH1} functions in the conventional manner, providing a current limit of approximately twice that required by the lamp. R_{TH2} acts to increase the current limit at turn-on to approximately 10 times the steady-state lamp current. The high initial trip point decays away according to a 20 ms time constant contributed by C_{TH} . R_{TH2} could be eliminated with C_{TH} working against the internal 1 kΩ resistor, but this results in a very high over-current threshold. As a rule of thumb design the over-current circuitry in the conventional manner, then add the R_{TH2}/C_{TH} network to allow for lamp start-up. Let $R_{TH2}=(R_{TH1}+10)-1k\Omega$, and choose a capacitor that provides the desired time constant working against R_{TH2} and the internal 1 kΩ resistor.

When the MIC5013 is turned off, the threshold pin (2) appears as an open circuit, and C_{TH} is discharged through R_{TH1} and R_{TH2} . This is much slower than the turn-on time constant, and it simulates the thermal response of the filament. If the lamp is pulse-width modulated, the current limit will be reduced by the residual charge left in C_{TH} .

Modifying Switching Times. Do not add external capacitors to the gate to slow down the switching time. Add a re-

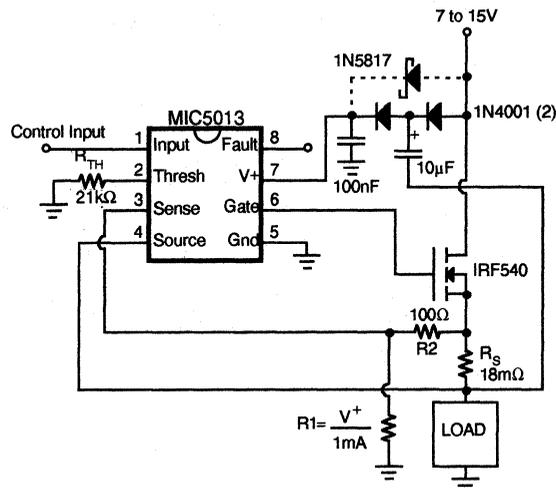


Figure 6. Bootstrapped High-Side Driver

sistor (1kΩ to 51kΩ) in series with the gate of the MOSFET to achieve this result.

Bootstrapped High-Side Driver (Figure 6). The speed of a high-side driver can be increased to better than 10 μ S by bootstrapping the supply off of the MOSFET source. This topology can be used where the load is pulse-width modulated (100 Hz to 20 kHz), or where it is energized for only a short period of time (≤ 25 ms). If the load is left energized for a long period of time (> 25 ms), the bootstrap capacitor will discharge and the MIC5013 supply pin will fall to $V^+=V_{DD}-1.4$. Under this condition pins 3 and 4 will be held above V^+ and may false trigger the over-current circuit. A larger capacitor will lengthen the maximum "on" time; 1000 μ F will hold the circuit up for 2.5 seconds, but requires more charge time when the circuit is turned off. The optional Schottky barrier diode improves turn-on time on supplies of less than 10V.

Since the supply current in the "off" state is only a small leakage, the 100 nF bypass capacitor tends to remain charged for several seconds after the MIC5013 is turned off. In a PWM application the chip supply is actually much higher than the system supply, which improves switching time.

Electronic Circuit Breaker (Figure 7). The MIC5013 forms the basis of a high-performance, fast-acting circuit breaker. By adding feedback from FAULT to INPUT the breaker can be made to automatically reset. If an over-current condition occurs, the circuit breaker shuts off. The breaker tests the load every 18 ms until the short is removed, at which time the circuit latches ON. No reset button is necessary.

Opto-Isolated Interface (Figure 8). Although the MIC5013 has no special input slew rate requirement, the lethargic transitions provided by an opto-isolator may cause oscillations on the rise and fall of the output. The circuit shown

Applications Information (Continued)

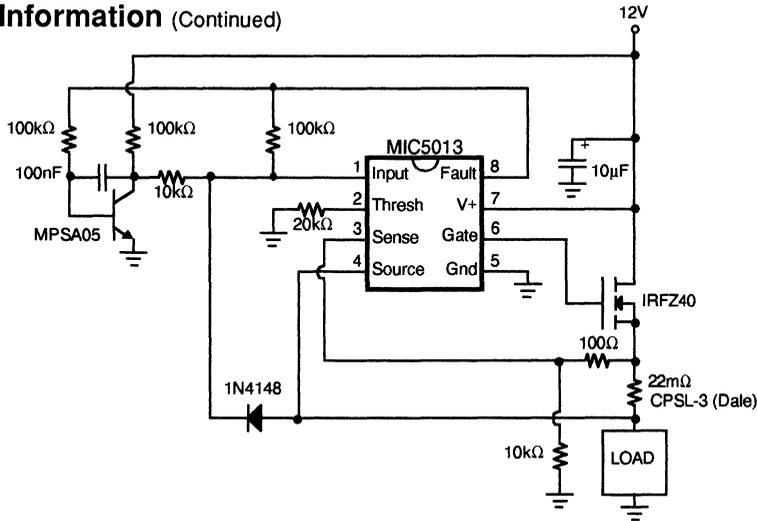


Figure 7. 10-Ampere Electronic Circuit Breaker

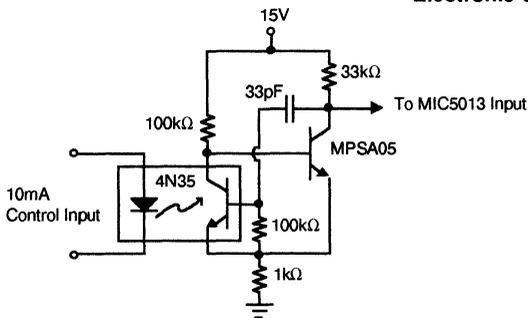


Figure 8. Improved Opto-Isolator Performance

accelerates the input transitions from a 4N35 opto-isolator by adding hysteresis. Opto-isolators are used where the control circuitry cannot share a common ground with the MIC5013 and high-current power supply, or where the control circuitry is located remotely. This implementation is intrinsically safe; if the control line is severed the MIC5013 will turn OFF.

Fault-Protected Industrial Switch (Figure 9). The most common manual control for industrial loads is a push button on/off switch. The "on" button is physically arranged in a recess so that in a panic situation the "off" button, which extends out from the control box, is more easily pressed. This circuit is compatible with control boxes such as the CR2943 series (GE). The circuit is configured so that if

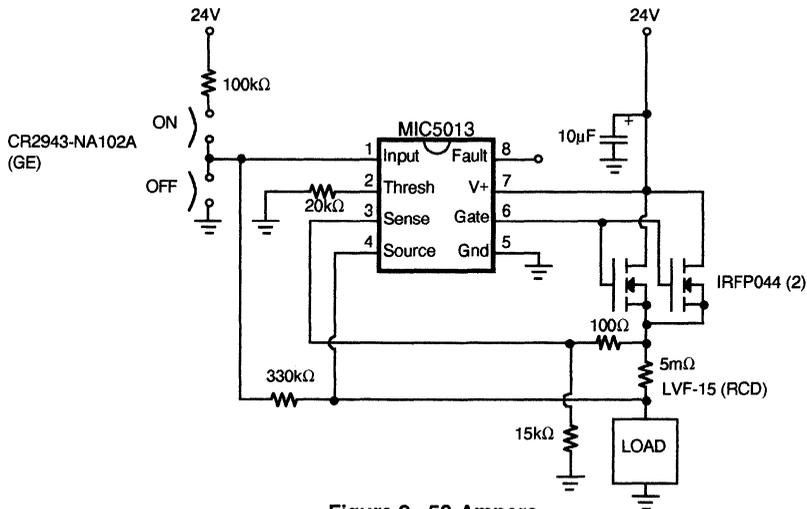


Figure 9. 50-Ampere Industrial Switch

Applications Information (Continued)

both switches close simultaneously, the "off" button has precedence. If there is a fault condition the circuit will latch off, and it can be reset by pushing the "on" button.

This application also illustrates how two (or more) MOSFETs can be paralleled. This reduces the switch drop, and distributes the switch dissipation into multiple packages.

High-Voltage Bootstrap (Figure 10). Although the MIC5013 is limited to operation on 7-32V supplies, a floating bootstrap arrangement can be used to build a high-side switch that operates on much higher voltages. The MIC5013 and MOSFET are configured as a low-side driver, but the load is connected in series with ground. The high speed normally associated with low-side drivers is retained in this circuit.

Power for the MIC5013 is supplied by a charge pump. A 20kHz square wave (15Vp-p) drives the pump capacitor and delivers current to a 100 μ F storage capacitor. A zener diode limits the supply to 18V. When the MIC5013 is off, power is supplied by a diode connected to a 15V supply. The circuit of Figure 8 is put to good use as a barrier between low voltage control circuitry and the 90V motor supply.

Half-Bridge Motor Driver (Figure 11). Closed loop control of motor speed requires a half-bridge driver. This topology presents an extra challenge since the two output devices should not cross conduct (shoot-through) when switching. Cross conduction increases output device power dissipation and, in the case of the MIC5013, could trip the over-current comparator. Speed is also important, since PWM control requires the outputs to switch in the 2 to 20 kHz range.

The circuit of Figure 11 utilizes fast configurations for both the top- and bottom-side drivers. Delay networks at each input provide a 2-3 μ s dead time effectively eliminating

cross conduction. Both the top- and bottom-side drivers are protected, so the output can be shorted to either rail without damage.

The top-side driver is based on the bootstrapped circuit of Figure 6, and cannot be switched on indefinitely. The bootstrap capacitor (1 μ F) relies on being pulled to ground by the bottom-side output to recharge. This limits the maximum duty cycle to slightly less than 100%.

Two of these circuits can be connected together to form an H-bridge. If the H-bridge is used for locked antiphase control, no special considerations are necessary. In the case of sign/magnitude control, the "sign" leg of the H-bridge should be held low (PWM input held low) while the other leg is driven by the magnitude signal.

If current feedback is required for torque control, it is available in chopped form at the bottom-side driver's 22 m Ω current-sensing resistor.

Time-Delay Relay (Figure 12). The MIC5013 forms the basis of a simple time-delay relay. As shown, the delay commences when power is applied, but the 100 k Ω /1N4148 could be independently driven from an external source such as a switch or another high-side driver to give a delay relative to some other event in the system.

Hysteresis has been added to guarantee clean switching at turn-on. Note that an over-current condition latches the relay in a safe, OFF condition. Operation is restored by either cycling power or by momentarily shorting pin 1 to ground.

Motor Driver with Stall Shutdown (Figure 13). Tachometer feedback can be used to shut down a motor driver circuit when a stall condition occurs. The control switch is a 3-way type; the "START" position is momentary and forces the driver ON. When released, the switch returns to the "RUN" position, and the tachometer's output is used to hold the MIC5013 input ON. If the motor slows down, the

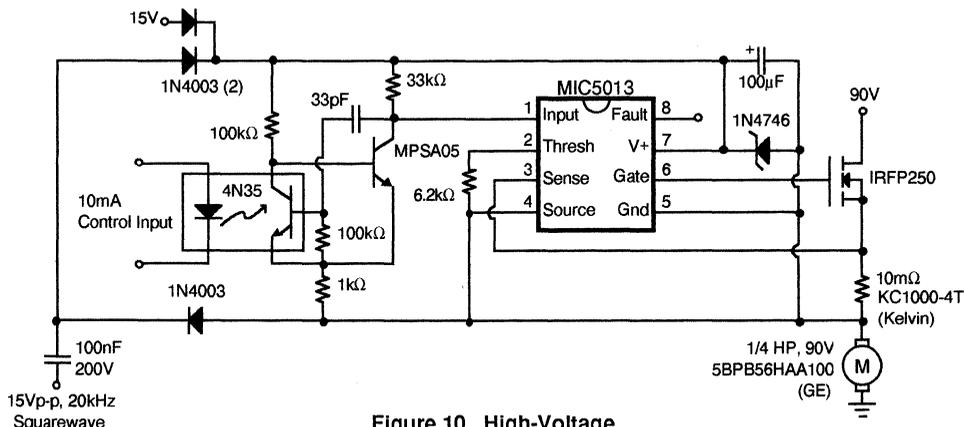


Figure 10. High-Voltage Bootstrap Driver

Applications Information (Continued)

tach output is reduced, and the MIC5013 switches OFF. Resistor "R" sets the shutdown threshold. If the output current exceeds 30A, the MIC5013 shuts down and remains in that condition until the momentary "RESET" button is pushed. Control is then returned to the START/RUN/STOP switch.

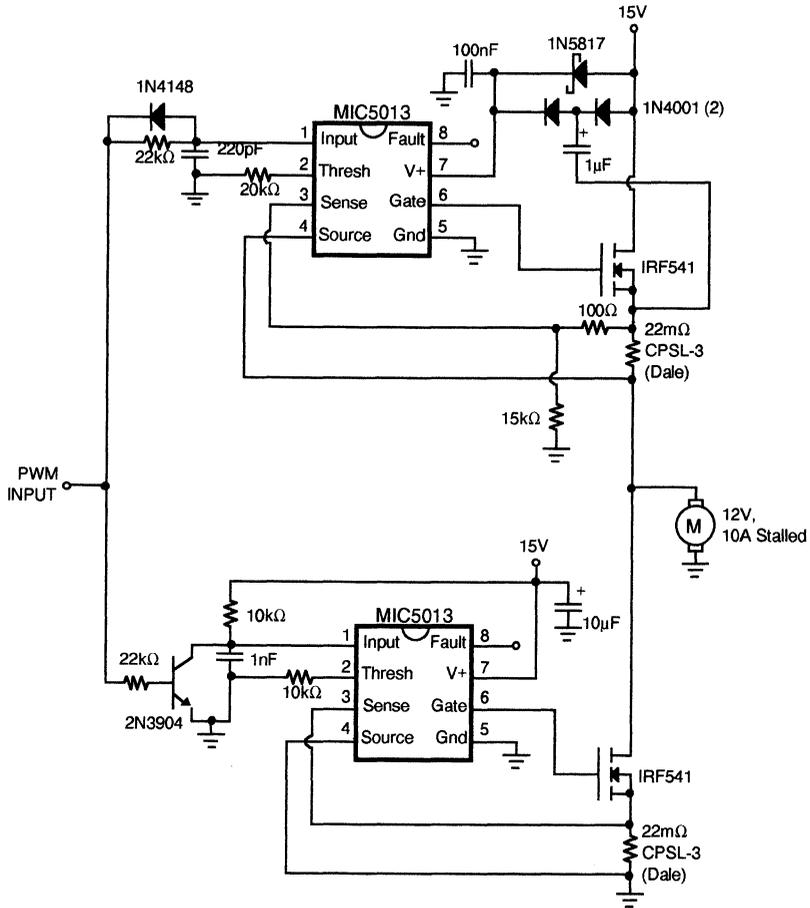


Figure 11. Half-Bridge Motor Driver

2

Applications Information (Continued)

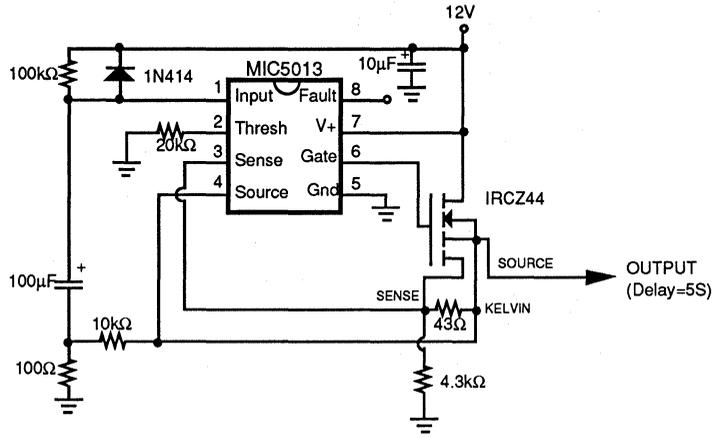


Figure 12. Time-Delay Relay with 30A Over-Current Protection

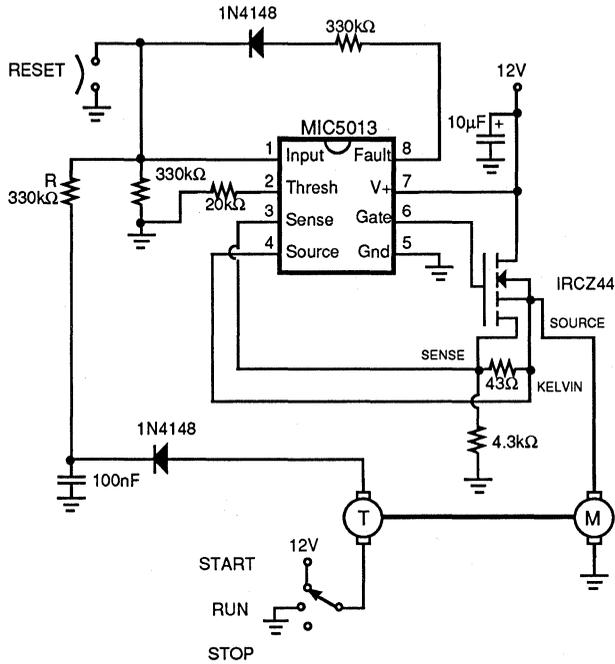


Figure 13. Motor Stall Shutdown

Applications Information (Continued)

Gate Control Circuit

When applying the MIC5013, it is helpful to understand the operation of the gate control circuitry (see Figure 14). The gate circuitry can be divided into two sections: 1) charge pump (oscillator, Q1-Q5, and the capacitors) and 2) gate turn-off switch (Q6).

When the MIC5013 is in the OFF state, the oscillator is turned off, thereby disabling the charge pump. Q5 is also turned off, and Q6 is turned on. Q6 holds the gate pin (G) at ground potential which effectively turns the external MOSFET off.

Q6 is turned off when the MIC5013 is commanded on. Q5 pulls the gate up to supply (through 2 diodes). Next, the charge pump begins supplying current to the gate. The gate accepts charge until the gate-source voltage reaches 12.5V and is clamped by the zener diode.

A 2-output, three-phase clock switches Q1-Q4, providing a quasi-tripling action. During the initial phase Q4 and Q2 are ON. C1 is discharged, and C2 is charged to supply through Q5. For the second phase Q4 turns off and Q3 turns on, pushing C2 above supply (charge is dumped into

the gate). Q3 also charges C1. On the third phase Q2 turns off and Q1 turns on, pushing the common point of the two capacitors above supply. Some of the charge in C1 makes its way to the gate. The sequence is repeated by turning Q2 and Q4 back on, and Q1 and Q3 off.

In a low-side application operating on a 12 to 15V supply, the MOSFET is fully enhanced by the action of Q5 alone. On supplies of more than approximately 14V, current flows directly from Q5 through the zener diode to ground. To prevent excessive current flow, the MIC5013 supply should be limited to 15V in low-side applications.

The action of Q5 makes the MIC5013 operate quickly in low-side applications. In high-side applications Q5 pre-charges the MOSFET gate to supply, leaving the charge pump to carry the gate up to full enhancement 10V above supply. Bootstrapped high-side drivers are as fast as low-side drivers since the chip supply is boosted well above the drain at turn-on.

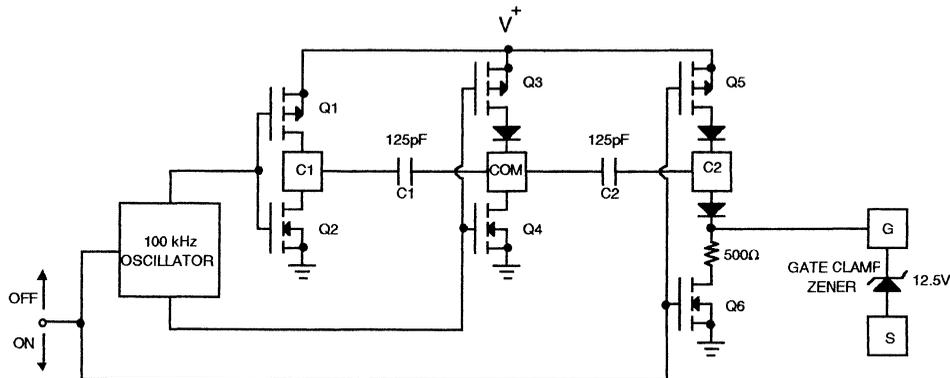


Figure 14. Gate Control Circuit Detail



SECTION 3: LATCHED DRIVERS

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MIC59P60 Protected 8-Bit Serial Input Latched Driver	3-42



Latched Driver Selection Guide

All Micrel Latched Drivers are available in die form. Special package options available on most latched drivers: please contact factory for details.

DEVICE	Number of Latches	Maximum Voltage	Nominal Drive Current (mA)	Parallel Input	Serial Input	Output Transient Protection	Temperature	PACKAGE
MIC4807 Protected Addressable Low Side Driver	8	80	200	•		•	A	18 Pin CerDIP
	8	80	200	•		•	B	18 Pin PDIP
MIC5800 Latched Driver	4	50	500	•		•	B	14 Pin PDIP
MIC5801 Latched Driver	8	50	500	•		•	B	22 Pin PDIP
MIC58P01 Protected Latched Driver	8	70	500	•		•	B	22 Pin PDIP
MIC5821 Serial Input Latched Driver	8	50	500		•		B	16 Pin PDIP
MIC5822 Serial Input Latched Driver	8	80	500		•		B	16 Pin PDIP
MIC5823 Serial Input Latched Driver	8	100	500		•		B	16 Pin PDIP
MIC5841 Serial Input Latched Driver	8	50	500		•	•	B	18 Pin PDIP
MIC5842 Serial Input Latched Driver	8	80	500		•	•	B	18 Pin PDIP
MIC58P42 Protected Serial Input Latched Driver	8	70	500		•	•	B	18 Pin PDIP
MIC5843 Serial Input Latched Driver	8	100	500		•	•	B	18 Pin PDIP
MIC59P50 Protected Parallel Input Latched Driver	8	70	500	•		•	B	24 Pin PDIP
MIC59P60 Protected Serial Input Latched Driver	8	70	500		•	•	B	20 Pin PDIP

Temperature Code:

A = -55°C to +125°C

B = -40°C to +85°C



General Description

The MIC4807 is an 80V, 8-channel, addressable low side driver with latch and TTL/CMOS compatible logic inputs. Each logic input is composed of a comparator with a 1.4V bandgap-derived reference serving as the trip point. The address (A_{IN} , B_{IN} , and C_{IN}) and Data-in logic inputs have an internal $50\mu A$ pull-up current source, while the Output Enable (OE), Chip Select (CS), and Clear logic inputs have an internal $75\mu A$ pull-down sink. If the logic lines to the MIC4708 are severed, these currents guarantee that the outputs will turn OFF.

Individual latches in the MIC4807 are selected by a binary address presented at inputs A_{IN} , B_{IN} , and C_{IN} . Data-in is directed to the addressed latch while CS is held low, allowing an individual output to be pulse-width modulated. When CS is set high again, the last Data-in is stored in the latch. If Data-in = "1", the addressed output is turned on, and if Data-in = "0", the addressed output is turned off.

Information presented to Data-in and the address inputs is transferred to the latches while CS is pulled low. For application, where several outputs must be (Continued)

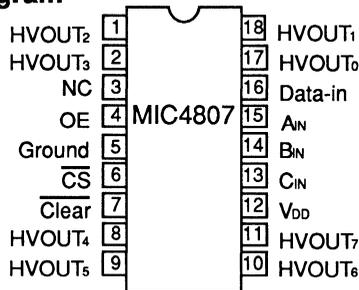
Features

- 4.5V-16V operation
- Eight 80V, 100mA outputs
- Off-state leakage less than $10\mu A$ at $25^\circ C$
- Short circuit proof
- Thermal shutdown with hysteresis
- DMOS output devices ($R_{ON} \leq 7\Omega$ at $25^\circ C$)

Applications

- Lamp Drivers
- Solenoid Drivers
- Display Drivers
 - Electroluminescent
 - Vacuum Fluorescent
 - Plasma
- Relay Drivers
- Print Head Drivers
- Heater Drivers
- Power Semiconductor Drivers
- Security Systems
- Environmental Controls
- Process Controllers

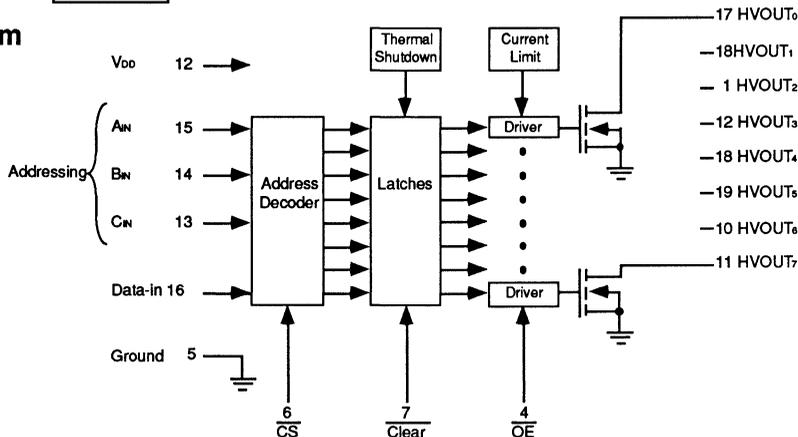
Pin Diagram



Ordering Information

Part Number	Operating Temperature-Range	Package
MIC4807AJB	-55°C to 125°C	18 Lead Ceramic DIP
MIC4807BN	-40°C to 85°C	18 Lead Plastic DIP

Block Diagram



General Description (Continued)

turned on simultaneously, Gray Code address sequencing can be applied to Ain, Bin, Cin, while Data-in is held high and \overline{CS} is held low. Data-in will be transferred to each address in turn, without the need to toggle \overline{CS} . Similarly, a set of outputs could be simultaneously turned off by setting Data-in low. Gray Code ensures that no intermediate addresses are inadvertently accessed. A typical Gray Code is 0, 1, 3, 2, 6, 7, 5, 4.

Each output drive circuit has a high-voltage, power DMOS device configured as a transconductance loop. This loop limits the output current to typically 200mA. While current limiting keeps the output device within its allowable safe-operating area (SOA), the power dissipation may be excessive. Long-term survival is guaranteed by thermal shutdown.

When operated below current limit, the outputs appear as small-valued resistors (typically 5.1 Ω at 25°C) connected to ground. The "ON" resistance (R_{ON}) has a strong, positive

temperature coefficient (approximately 7500 ppm/°C) which promotes current sharing if two or more outputs are paralleled.

Absolute Maximum Ratings (Notes 1, 2 and 3)

Output Voltage ($V_{OUT, OFF}$)	100V
Supply Voltage (V_{DD})	16.5V
Logic Input Voltage (V_{IN})	-0.5V to $V_{DD} + 0.5$
Continuous Output Current (I_{OUT})	Internally Limited
Power Dissipation (P_D , Note 2)	Internally Limited
Ambient Temperature (T_A):	
B Version	-40°C to +85°C
A version	-55°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	-65°C to +150°C
θ_{JA} - Plastic DIP	130°C/W
θ_{JA} - Ceramic DIP	90°C/W

Electrical Characteristics: (Note 6) MIC4807BN, $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$ unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)		5.5 1.5	10 3	mA mA
$V_{IN} (0)$	Logic Input Voltage	$4.5\text{V} \leq V_{DD} \leq 16\text{V}$			0.8	V
$V_{IN} (1)$			2.0			V
$I_{IN} (0)$	Logic Input Current for A_{IN} , B_{IN} , C_{IN} , and Data-in	$V_{IN} = 0\text{V}$	-100	-70	-25	μA
$I_{IN} (1)$	Logic Input Current for \overline{CS} , OE, and Clear	$V_{IN} = V_{DD}$	25	130	250	μA
I_{OUT}	Output Leakage Current	OE = 0V, $V_{OUT} = 80\text{V}$		1	10	μA
R_{ON}	Output "ON" Resistance	Output is ON, $V_{OUT} = 0.7\text{V}$, $V_{DD} = 10\text{V}$		5.1	7	Ω
I_{SC}	Short Circuit Current	Output is ON, $V_{OUT} = 50\text{V}$ $10\text{V} \leq V_{DD} \leq 15\text{V}$ (Note 5)	140	190	250	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	$I_{OUT} = 50\text{mA}$, $V_{DD} = 10\text{V}$ $I_{OUT} = 100\text{mA}$, $V_{DD} = 10\text{V}$		0.26 0.51	0.35 0.7	V V
	Data and Address Set-up Time	$V_{DD} = 10\text{V}$ for all timing tests (A, see Timing Diagram)	400			nS
	Data and Address Hold Time	(B)	50			nS
	\overline{CS} Pulse Width	(C)	500			nS
	Turn-on Delay	(D)			2.5	nS

Electrical Characteristics: (Note 6) MIC4807BN, $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$ unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			2.5	μS
	Output Disable Response Time	(F)			2	μS
	Output Enable Response Time	(G)			2	μS
	$\overline{\text{Clear}}$ Response Time	(H)			2.5	μS
	$\overline{\text{Clear}}$ Pulse Width	(I)	500			nS

Electrical Characteristics: (Note 6) MIC4807AJB, $T_A = 55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{DD} = 15\text{V}$ unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5		16	V
I_{DD}	Supply Current	OE = L (Note 3) OE = H (Note 4)			15 4	mA mA
$V_{IN}(0)$	Logic Input Voltage	$4.5\text{V} \leq V_{DD} \leq 16\text{V}$			0.8	V
$V_{IN}(1)$			2.0			V
$I_{IN}(0)$	Logic Input Current for A_{IN} , B_{IN} , C_{IN} , and Data-in	$V_{IN} = 0\text{V}$	-150		-10	μA
$I_{IN}(1)$	Logic Input Current for $\overline{\text{CS}}$, OE, and $\overline{\text{Clear}}$	$V_{IN} = V_{DD}$	25		300	μA
I_{OUT}	Output Leakage Current	OE = 0V, $V_{OUT} = 80\text{V}$		5.1	7	μA
R_{ON}	Output "ON" Resistance	Output is ON, $V_{OUT} = 0.7\text{V}$, $V_{DD} = 10\text{V}$			12	Ω
I_{SC}	Short Circuit Current	Output is ON < $V_{OUT} = 50\text{V}$ $10\text{V} \leq V_{DD} \leq 15\text{V}$ (Note 5)	100		300	mA
V_{OUT}	Output Voltage (OFF)				80	V
V_{OUT}	Output Voltage (ON)	$I_{OUT} = 50\text{mA}$, $V_{DD} = 10\text{V}$ $I_{OUT} = 100\text{mA}$, $V_{DD} = 10\text{V}$			0.6 1.2	V V
	Data and Address Set-up Time	$V_{DD} = 10\text{V}$ for all timing tests (A, see Timing Diagram)	700			nS
	Data and Address Hold Time	(B)	50			nS
	$\overline{\text{CS}}$ Pulse Width	(C)	1000			nS
	Turn-on Delay	(D)			5	μS

Electrical Characteristics: (Note 6) MIC4807BN, $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{V}$ unless otherwise specified (see Test Circuit).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Turn-Off Delay	(E)			5	μS
	Output Disable Response Time	(F)			4	μS
	Output Enable Response Time	(G)			4	μS
	$\overline{\text{Clear}}$ Response Time	(H)			5	μS
	$\overline{\text{Clear}}$ Pulse Width	(I)	1000			nS

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: The junction temperature is internally limited by a thermal shutdown circuit. The maximum power dissipation is a function of T_{JMAX} , θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX} - T_A) / \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C , and the MIC4807 will go into thermal shutdown.

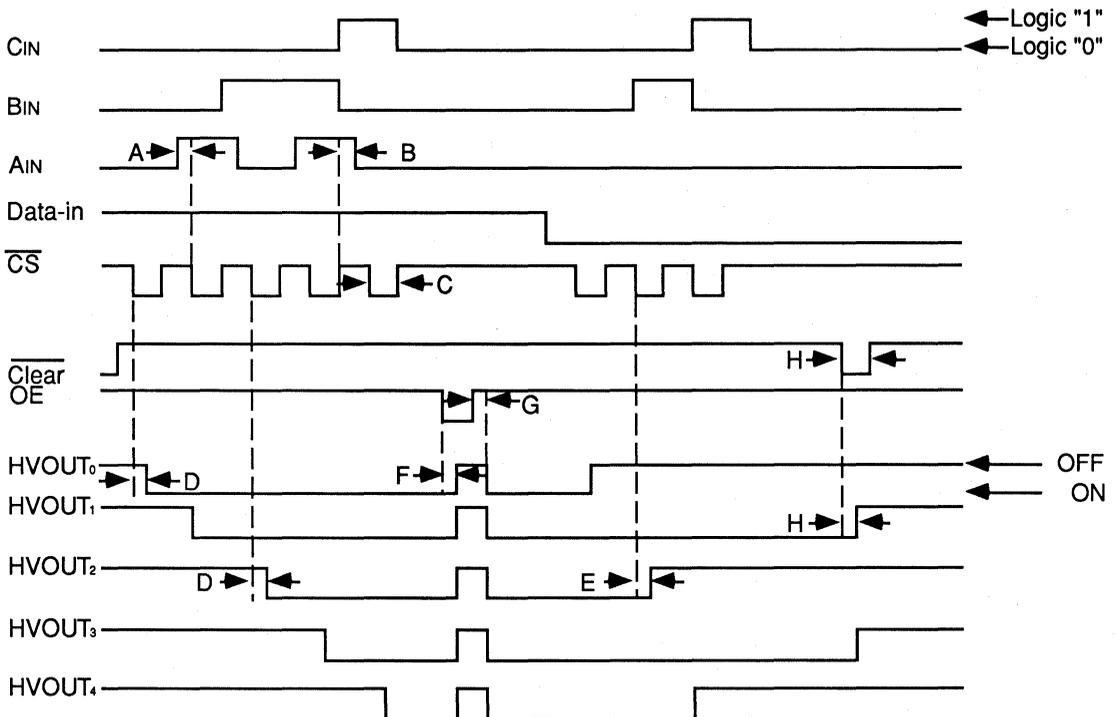
Note 3: All outputs are off when **OUTPUT ENABLE** is pulled low.

Note 4: All outputs are turned on during this test.

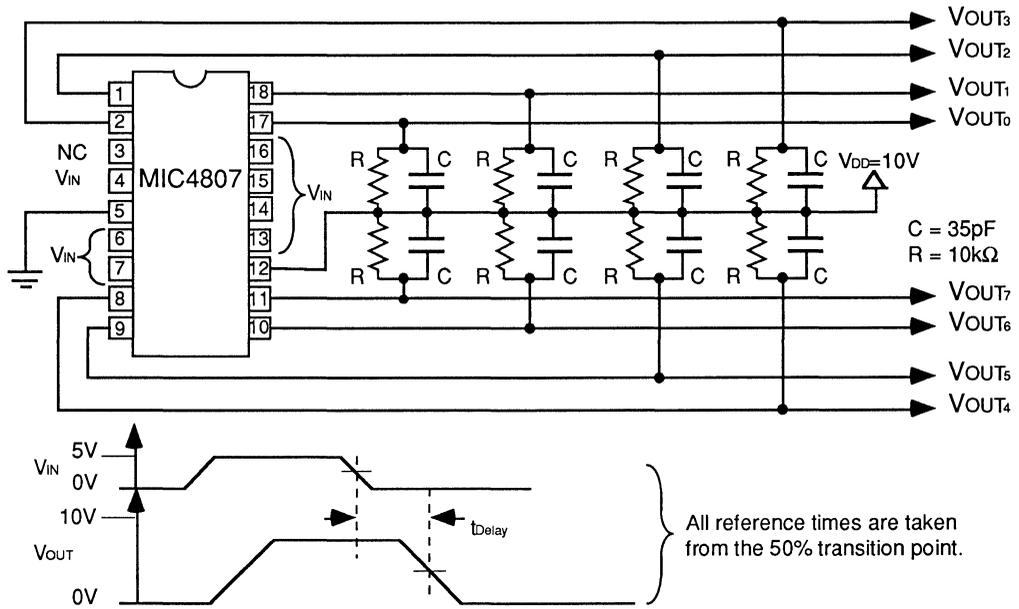
Note 5: Pulse testing is used to avoid thermal shutdown.

Note 6: Minimum and Maximum limits are tested and 100% guaranteed over the temperature range specified. Typicals are measured at 25°C and represent the most likely parametric norm.

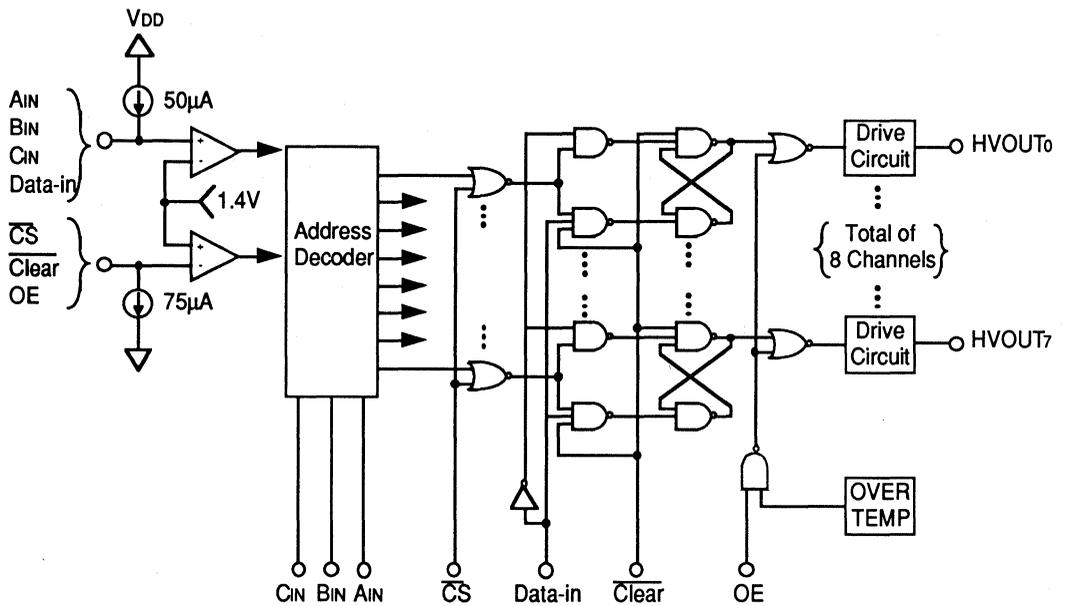
Timing Diagram



Test Circuit and AC Waveform Measurement Standards



Equivalent Logic Diagram



Truth Table

\overline{CS}	\overline{Clear}	Data-In	C_{IN}	B_{IN}	A_{IN}	OE	HVOUT ₀	HVOUT ₁	HVOUT ₂	HVOUT ₃	HVOUT ₄	HVOUT ₅	HVOUT ₆	HVOUT ₇	Functional Mode
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	P	P	P	P	P	P	P	P	Memory
L	H	D	L	L	L	H	\overline{D}	P	P	P	P	P	P	P	Address HVOUT ₀
L	H	D	L	L	H	H	P	\overline{D}	P	P	P	P	P	P	Address HVOUT ₁
L	H	D	L	H	L	H	P	P	\overline{D}	P	P	P	P	P	Address HVOUT ₂
L	H	D	L	H	H	H	P	P	P	\overline{D}	P	P	P	P	Address HVOUT ₃
L	H	D	H	L	L	H	P	P	P	P	\overline{D}	P	P	P	Address HVOUT ₄
L	H	D	H	L	H	H	P	P	P	P	P	\overline{D}	P	P	Address HVOUT ₅
L	H	D	H	H	L	H	P	P	P	P	P	P	\overline{D}	P	Address HVOUT ₆
L	H	D	H	H	H	H	P	P	P	P	P	P	P	\overline{D}	Address HVOUT ₇
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking

L = Low Logic Level

X = Don't Care

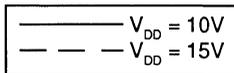
H = High Logic Level

P = Previous State

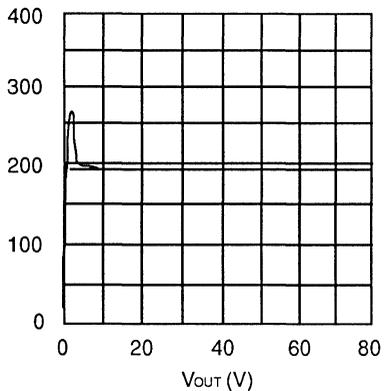
D = Data (High or Low)

Typical DC Output Characteristics for the "On" State:

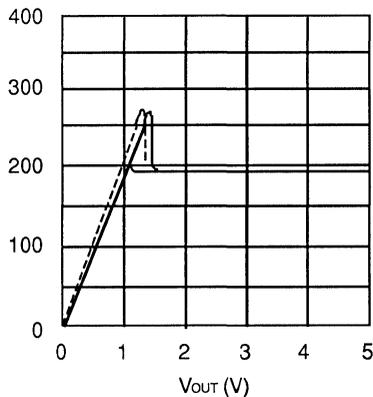
($V_{DD} = 10V$ and $T = 25^{\circ}C$ unless other wise specified)



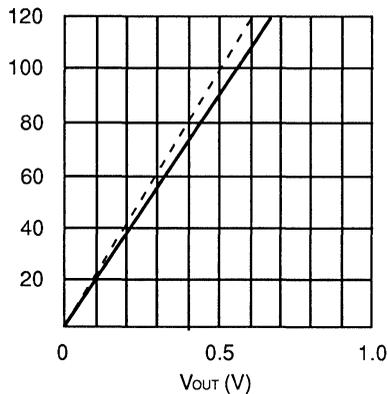
SHORT CIRCUIT CURRENT



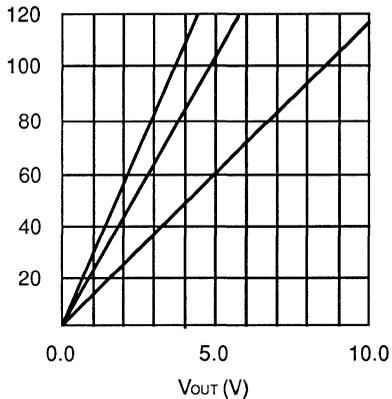
EXPANDED VERSION OF SHORT CIRCUIT CURRENT FOR LOW OUTPUT VOLTAGE (V_{out})



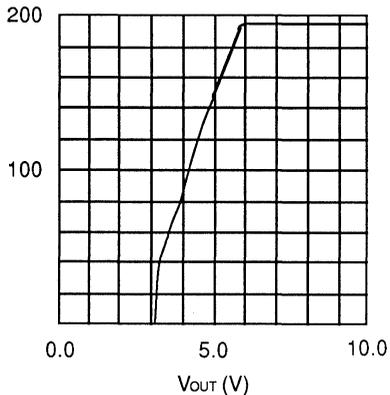
I_{out} FOR SEPARATE V_{DD} 'S



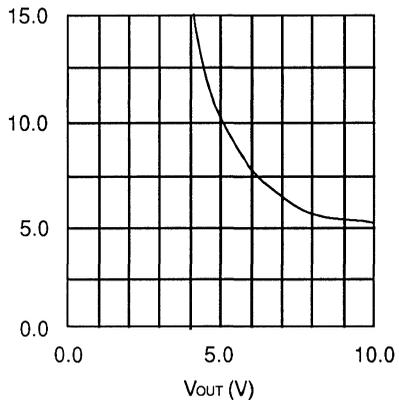
I_{out} AT 3 TEMPERATURES



SHORT CIRCUIT CURRENT LIMIT (I_{sc})



ON RESISTANCE (R_{on})



Pin Description

Pin No.	Pin Name	Functional Description
5	Ground	Electrical ground to chip substrate.
12	V _{DD}	Positive logic supply voltage (10V-15V).
1, 2, 8, 9,10, 11, 17,18	HVOUT ₀ through HVOUT ₇	These are the high voltage (HV) open outputs, each of which is capable of sinking 100mA when switched on, and standing off 80V when switched off. In addition, each output channel is equipped with an analog current limiter to protect it from shorts to the positive high voltage supply. When an output is shorted (up to 80V), a maximum of 225mA (200mA nominal) will flow through it to ground.
13, 14, 15	C _{IN} , B _{IN} , & A _{IN}	When these inputs are combined together they form the BCD address used to select the desired output. Each input is TTL compatible with an internal pull-up current source of 50mA.
6	CS	When \overline{CS} is at logic "0" the device is actively addressed, and when \overline{CS} is at logic "1" the decoded address and input Data are inhibited, making the part unaddressable. \overline{CS} is TTL compatible with an internal pull-down current sink of 75 μ A.
7	\overline{Clear}	\overline{Clear} resets all the outputs to the off state when pulled to logic "0", and is TTL compatible with an internal pull-down current sink of 75 μ A.
16	Data-in	Data-in determines the state of the output being addressed. When Data-in is at logic "0" the addressed output is turned off, and when Data-in is at logic "1" the addressed output is turned on. Data-in is TTL compatible with an internal pull-up current source of 50 μ A.
4	OE	OE allows the bank of eight outputs to be duty cycled together. When OE is at logic "1" the outputs are enabled to follow their respective latches, and when OE is at logic "0" all the outputs are turned off. OE is TTL Compatible with a pull-down current sink of 75 μ A.



Application Note 2

MIC4807 Display Dimmer

by Mitchell Lee

Abstract: The MIC4807 is an 8 channel, addressable low side driver is guaranteed to deliver 100mA minimum at up to 80V, per channel. This note discusses the operation of the MIC4807 and shows how it can be used as a display driver with dimming for incandescent indicators.

Introduction

The MIC4807 contains 8 low side drivers that are controlled by addressable latches (see Figure 1). Open-drain, N-channel MOSFETs of approximately 5.1Ω "on" resistance are used as output devices. The MOSFETs are designed for operation to 80V.

Each output is controlled by its own addressable latch; the latches are selected by a 3-bit parallel address (A_{in} , B_{in} , and C_{in}). A "1" at the data input turns the corresponding MOSFET on.

Power ICs demand protection from excessive current and dissipation, and to this end the MIC4807 includes short-circuit current limiting and thermal shutdown. In fact, the chip can withstand a dead short to 80V without damage. The output limits at typically 200 mA, and the chip is guaranteed to deliver 100 mA minimum over temperature. While current limiting provides short-term protection from load faults, thermal shutdown protects against sustained fault conditions by shutting off all outputs when the die temperature exceeds 150°C . Current limiting and thermal shutdown are indispensable, yet they are sorely lacking in many other functionally similar ICs where the implementation of protection circuits is left as an exercise for the user.

Incandescent Lamp Characteristics

Owing to their superior light output, incandescent lamps are preferred over other display devices for use in bright environments. Unfortunately, incandescent lamps have a number of characteristics that make them difficult to work with in practical applications. For example, lamps do not lend themselves to multiplexing. It is technically possible to multiplex lamps by a higher-than-rated supply voltage in conjunction with PWM techniques to control filament power dissipation.

A major pitfall of multiplexing is reliability. If the multiplex circuit fails to advance for any reason (power-up phenomenon, slow or stuck oscillator, etc.) the lamps will burn out instantly. In addition, the switched current increases proportionally with the supply voltage, necessitating larger switches.

Since multiplexing is impractical, each lamp must have its own dedicated driver. This adds circuit overhead not only in the number of drivers, but also in terms of communicating with the drivers.

The brightness of an Incandescent lamp is an asset in brightly illuminated environments, but what happens at night? Under contrasting conditions of low ambient light levels, the bright display can temporarily blind persons viewing it. Examples of environments with wide-ranging light levels include the cockpit of an airplane, or the operator's cab on farm or construction machinery. A dimming feature is highly desirable for any incandescent display.

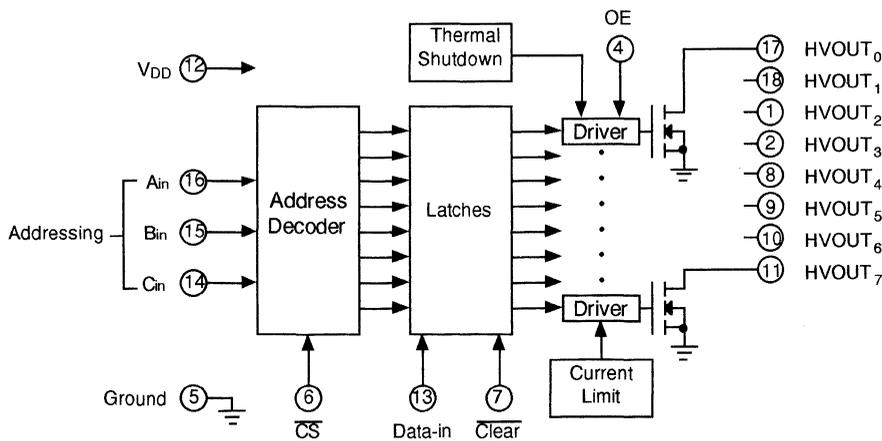


Figure 1. MIC4807 Block Diagram

Unlike LEDs, incandescent lamps require more current and voltage than 5V digital logic circuits can deliver. In particular, lamps draw an appreciable inrush current because the filament resistance is much lower when cold than when hot. Inrush currents of 10 times rated operating current are not uncommon. This impacts both the current rating of the driver and the lifetime of the lamp. Among other contributing factors, lamp lifetime is limited by the severe thermal shock experienced at turn-on.

Display Driver

Figure 2 shows a practical display driver circuit using the MIC4807. #1835 miniature lamps were selected for use on a loosely regulated "48V" system supply, which normally ran about 110% rated voltage. The #1835 lamp is specified at 55V and 50 mA, and it can easily withstand $\pm 15\%$ variations in a 48V supply without loss of rated life. The lamps are housed in #31099 (GTE/Sylvania) in-

dicator assemblies. Output current limit precludes the possibility of chip destruction from short circuit conditions such as arise when a lamp socket is "tested" for power with the conductive end of a screwdriver. Long-term short circuits (wiring faults) are handled by the MIC4807's thermal shutdown circuit.

When the MIC4807 cold-starts a #1835 lamp, the output is immediately driven into current limit since it cannot deliver the full inrush current. The cold resistance of a #1835 lamp is approximately 94Ω ; an initial current of 585 mA would flow if connected directly to 55V. The MIC4807 current limit is typically 200 mA at room temperature, which reduces the thermal shock at turn-on and increases lamp lifetime. Note that applying 200 mA to the cold filament is equivalent to an initial lamp voltage of only 18.8V.

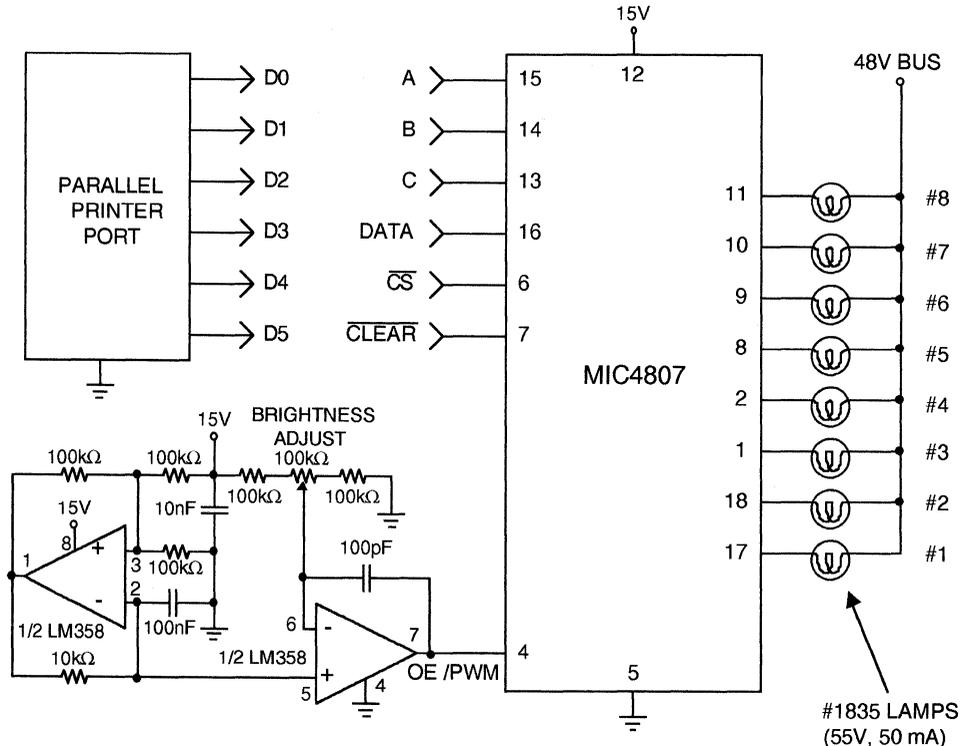


Figure 2. MIC4807 Display Controller with PWM Dimming

Display Dimming

Dimming is achieved by pulse-width modulation applied to the OUTPUT ENABLE (OE) pin. Since OUTPUT ENABLE acts on all 8 channels, the lamps are simultaneously dimmed by one control signal and maintain equal brightness, regardless of the dimming level.

An LM358 dual op-amp forms the basis of a variable PWM. The control range extends from completely off to completely on, and to any intermediate brightness level.

The PWM frequency (400 Hz) is considerably higher than the filament's thermal time constant, so the filament's resistance (and temperature) changes very little between "on" and "off" periods. Figure 3 shows the pulsed filament current in a PWM application for a single #1835 lamp as a function of duty cycle. Lamp manufacturers recommend a PWM frequency of at least 400 Hz to eliminate aging effects associated with thermal cycling. At an extremely dim 10% duty cycle, a #1835 lamp accepts current pulses of 90 mA on a 55V supply, exhibiting a filament resistance of 611 Ω . At 100% duty cycle the current falls to 50 mA, at a resistance of 1100 Ω . In any dimming circuit the driver circuitry must be sized to deliver the pulsed, low duty cycle current required by the relatively cool filament. This is typically twice the rated (100% duty cycle) lamp current.

MIC4807 Programming

The MIC4807 programming interface consists of a 3-bit address, a data line, and two control lines (see Figure 2). CLEAR is straightforward; a low on this pin asynchronously clears the internal latches to turn all outputs off.

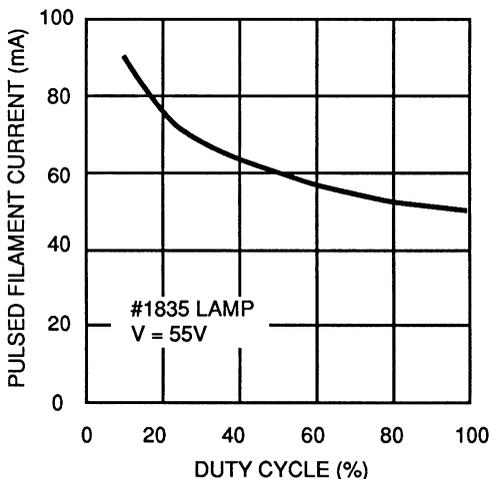


Figure 3. Pulsed Filament Current vs. Duty Cycle

Programming is accomplished by addressing an output, presenting the desired data (1=ON, 0=OFF), and strobing CHIP SELECT with a logic low. DATA is transferred to the addressed output on the falling edge of CHIP SELECT, and is latched in place when CHIP SELECT returns to a high state. In larger displays, CHIP SELECT serves as a means of controlling several MIC4807s while the address, OUTPUT ENABLE, CLEAR, and DATA lines are paralleled.

For bench testing purposes a personal or laptop/portable computer is quite useful. A parallel printer port is commonly available and serves as a convenient means of programming one or more MIC4807s. Software changes can be made quickly and easily and, depending on the programming language used, the program can be stepped manually so that each bit can be checked "on the fly." This presents no problems because the MIC4807 is fully static.

An evaluation program written in BASIC is listed in Figure 4. The program consists of 5 parts. The control/input section is lines 100 through 130. This portion scans the keyboard, and branches to other parts of the program depending on which key is pressed. A "line return" branches to lines 3000 through 3030 where the MIC4807 is cleared and the computer's record of the MIC4807 latch states [8-element array D(A)] is cleared. Execution then returns to lines 100 through 130. A "?" invokes a lamp test function--all of the outputs are turned on by lines 2000 through 2060. Pressing any other key reprograms the MIC4807 with the original data, and returns execution to lines 100 through 130. Pressing any number from 1 to 8 toggles the associated output on or off (lines 1000 through 1020). Lines 4000 through 4020 are accessed from several points in the program; these lines write data to a given address by toggling CHIP SELECT.

The parallel output word is given a value according to which MIC4807 pins should be high or low at any given time. A_{in} has a numeric (decimal) value of 1, $B_{in}=2$, $C_{in}=4$, DATA=8, CHIP SELECT=16, and CLEAR=32 to represent a logical "1" at each pin. The port number (8) specified in the "OUT" statements will vary from computer to computer. While final evaluation of data communications must be carried out with the actual host processor, using a computer during the debugging phase of the display design is most helpful.

An equivalent block diagram of the MIC4807 logic circuitry is shown in Figure 5. Note that CHIP SELECT, DATA, CLEAR, AND OUTPUT ENABLE operate on all channels in parallel. The address decoder determines to which latch CHIP SELECT is directed. DATA has no effect on the other latches as their clocking signals remain low.

```

10 REM MIC4807 CONTROL PROGRAM
20 GOSUB 3000
30 REM A=1,B=2,C=4,DATA=8,CS=16,CLR=32
100 A$=INKEY$:IF A$="" THEN GOTO 100 ELSE
    LET A=ASC(A$)-49
110 IF A=-36 THEN GOSUB 3000
120 IF A=14 THEN GOSUB 2000
130 IF A<0 OR A>7 THEN GOTO 100
1000 D(A)=8-D(A)+2*A+96:REM TOGGLE OUTPUT
1010 GOSUB 4000
1020 GOTO 100
2000 REM "?" TURNS ON ALL OUTPUTS FOR TEST
2010 FOR A=0 TO 7
2020 OUT 8,A+56:OUT 8,A+40:OUT 8,A+56
2030 NEXT A
2040 IF INKEY$="" THEN GOTO 2040
2050 FOR A=0 TO 7:GOSUB 4000:NEXT A
2060 RETURN
3000 REM CLEAR DISPLAY AND MEMORY
3010 OUT 8,16:OUT 8,48
3020 FOR A=0 TO 7:D(A)=A+48:NEXT A
3030 RETURN
4000 REM COMMUNICATIONS DRIVER
4010 OUT 8,D(A):OUT 8,D(A)-16:OUT 8,D(A)
4020 RETURN
9999 END

```

Figure 4. MIC4807 Control Program Listing

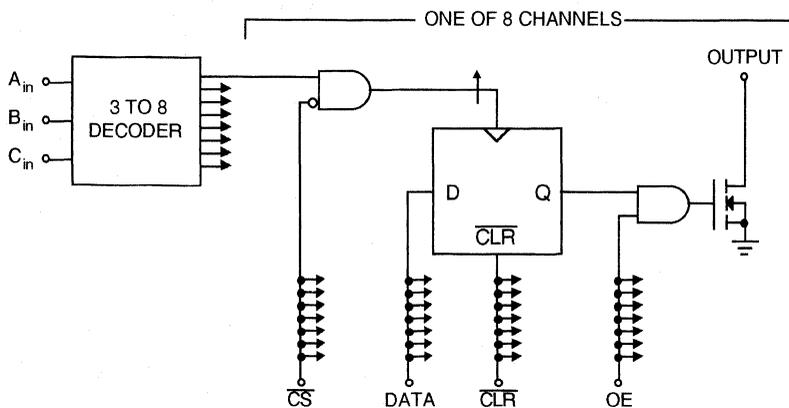


Figure 5. Block Diagram of Logic Circuitry



MIC5800/5801

Latched Drivers

Preliminary Information

General Description

The MIC5800/5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC5800 contains four latched drivers and the MIC5801 contains eight latched drivers.

Data input rates are greatly improved in these devices. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on power package

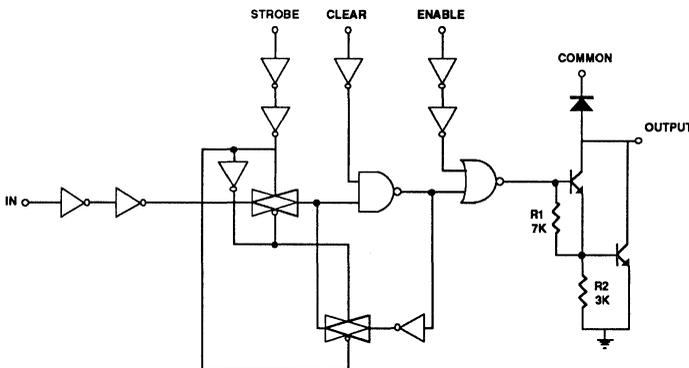
Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

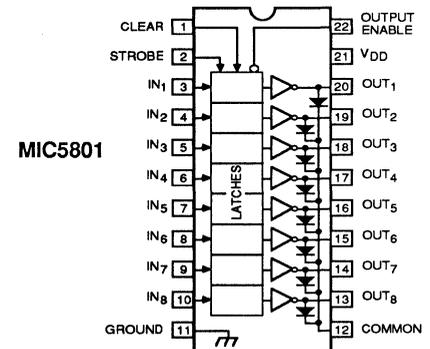
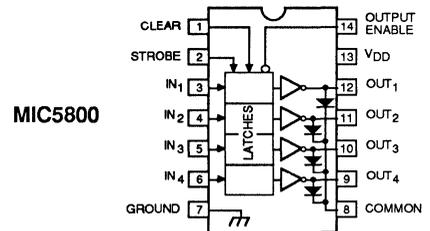
Ordering Information

Part Number	Temperature Range	Package
MIC5800BN	-40°C to +85°C	14-pin Plastic DIP
MIC5801BN	-40°C to +85°C	22-pin Plastic DIP

Functional Diagram



Pin Configurations



dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

MIC5800, the 4-latch device, is packaged in a standard 14-pin dual in-line plastic package. MIC5801, the 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

Absolute Maximum Ratings: (Notes 1, 2, 3)

at +25°C Free-Air Temperature

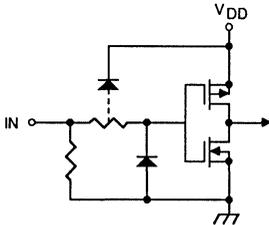
Output Voltage, V_{CE}	50 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Continuous Collector Current, I_C	500 mA
Package Power Dissipation	
MIC5800(Note 1)	1.6 W
MIC5801(Note 2)	2.0 W
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature Range, T_S	-65°C to +125°C

Note 1: Derate at the rate of 16.7 mW/°C above $T_A = +25^\circ\text{C}$

Note 2: Derate at the rate of 20 mW/°C above $T_A = +25^\circ\text{C}$

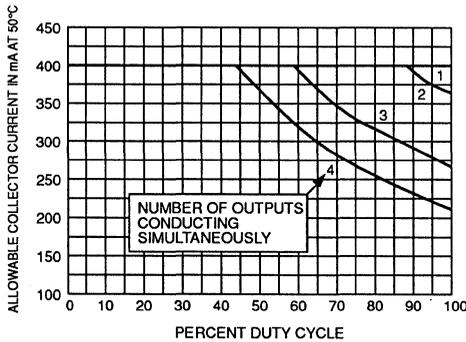
Note 3: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input

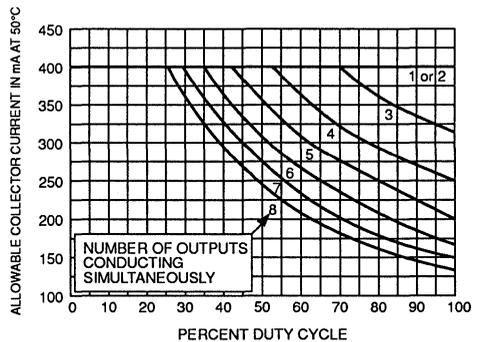


Allowable Output Current As A Function of Duty Cycle

MIC5800



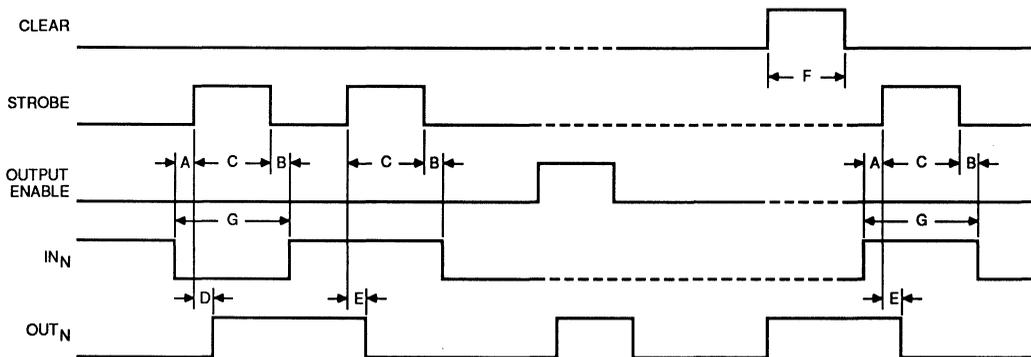
MIC5801



Electrical Characteristics: at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 50\text{V}$, $T_A = +25^\circ\text{C}$			50	μA
		$V_{CE} = 50\text{V}$, $T_A = +70^\circ\text{C}$			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\text{mA}$		0.9	1.1	V
		$I_C = 200\text{mA}$		1.1	1.3	
		$I_C = 350\text{mA}$, $V_{DD} = 7.0\text{V}$		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\text{V}$	10.5			
		$V_{DD} = 10\text{V}$	8.5			
		$V_{DD} = 5.0\text{V}$ (See Note)	3.5			
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50	200		$\text{k}\Omega$
		$V_{DD} = 10\text{V}$	50	300		
		$V_{DD} = 5.0\text{V}$	50	600		
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\text{V}$, Outputs Open		1.0	2.0	mA
		$V_{DD} = 10\text{V}$, Outputs Open		0.9	1.7	
		$V_{DD} = 5.0\text{V}$, Outputs Open		0.7	1.0	
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\text{V}$, Outputs Open, Inputs = 0 V			200	μA
	$V_{DD} = 5.0\text{V}$, Outputs Open, Inputs = 0 V		50	100		
Clamp Diode Leakage Current	I_R	$V_R = 50\text{V}$, $T_A = +25^\circ\text{C}$			50	μA
		$V_R = 50\text{V}$, $T_A = +70^\circ\text{C}$			100	
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		1.7	2.0	V

NOTE 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Timing Conditions

(Logic Levels are V_{DD} and Ground)

- A. Minimum data active time before strobe enabled (data set-up time) 50 nS
- B. Minimum data active time after strobe disabled (data hold time) 50 nS
- C. Minimum strobe pulse width 125 nS
- D. Typical time between strobe activation and output on to off transition 500 nS
- E. Typical time between strobe activation and output off to on transition 500 nS
- F. Minimum clear pulse width 300 nS
- G. Minimum data pulse width 225 nS

Truth Table

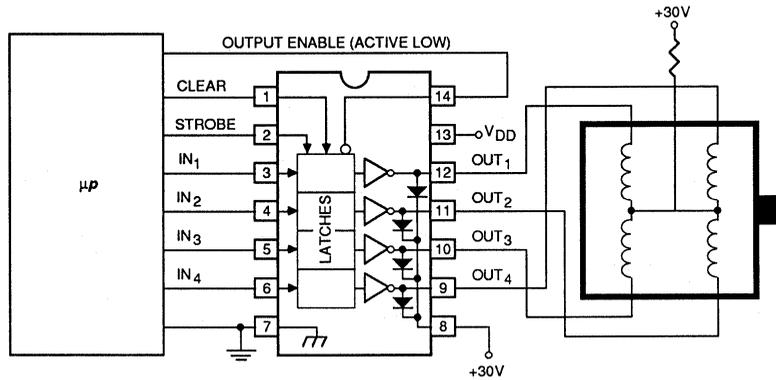
IN _N	Strobe	Clear	Output Enable	OUT _N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
 t-1 = previous output state
 t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

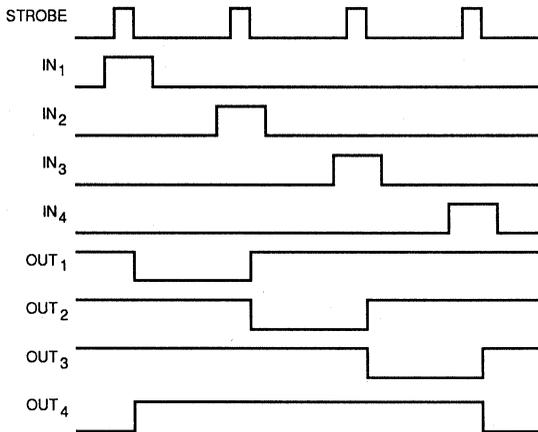
Typical Application

Unipolar Stepper-Motor Drive

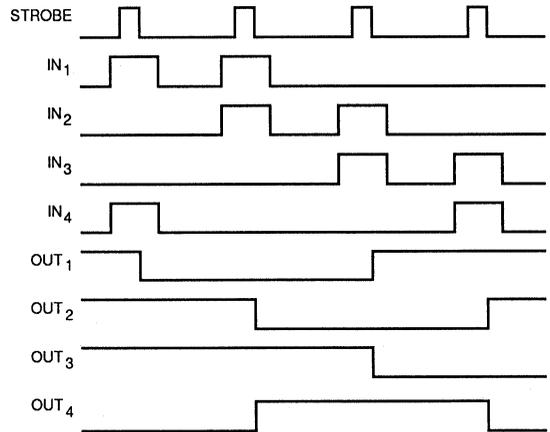


MIC5800

UNIPOLAR WAVE DRIVE



UNIPOLAR 2-PHASE DRIVE





MIC58P01

Latched Driver

Preliminary Information

General Description

The MIC58P01 latched driver is a high-voltage, high-current integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, RESET and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P01 contains eight latched drivers.

The MIC58P01 is similar to the MIC5801, but has added features such as thermal shutdown, undervoltage lockout and over current shutdown that makes it "bullet proof"-- ideal for automotive or industrial environments. During thermal shutdown, all channels are disabled. An over current condition shuts down only the affected channel and must be 1 μ S long before shutdown occurs. To turn the channel back on, the OUTPUT ENABLE/RESET pin must be pulsed high.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

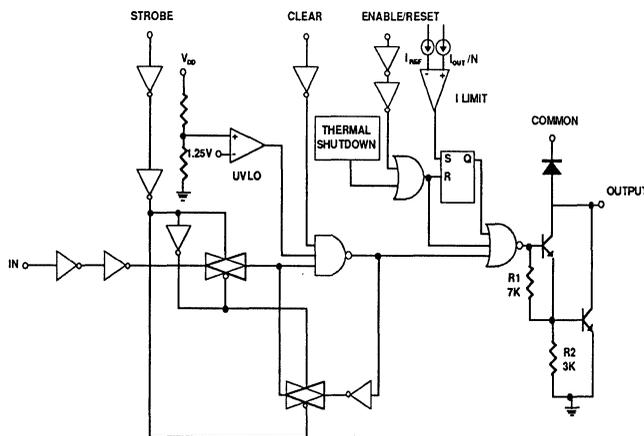
Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Thermal Shutdown
- Output Current Limit (500mA minimum threshold)
- Under Voltage Lockout

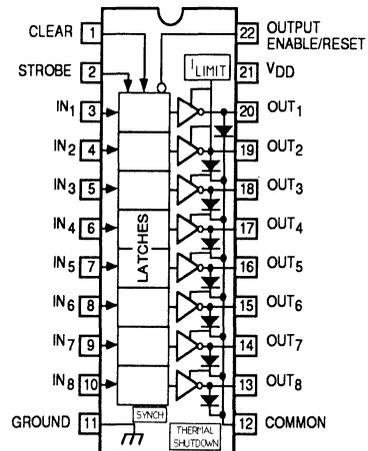
Ordering Information

Part Number	Temperature Range	Package
MIC58P01BN	-40°C to +85°C	22-pin Plastic DIP

Functional Diagram



Pin Configurations



MIC58P01

The MIC58P01 has open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 70 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The MIC58P01 is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

Absolute Maximum Ratings: (Notes 1, 2)

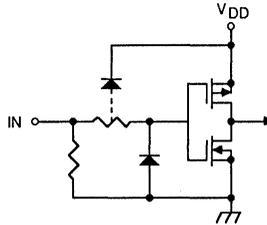
at +25°C Free-Air Temperature

Output Voltage, V_{CE}	70 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Continuous Collector Current, I_C	500 mA
Package Power Dissipation MIC5801 (Note 1)	2.25 W
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature Range, T_S	-65°C to +125°C

Note 1: Derate at the rate of 20 mW/°C above $T_A = +25^\circ\text{C}$

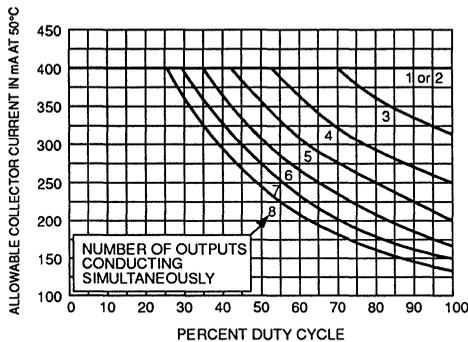
Note 2: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input



Allowable Output Current As A Function of Duty Cycle

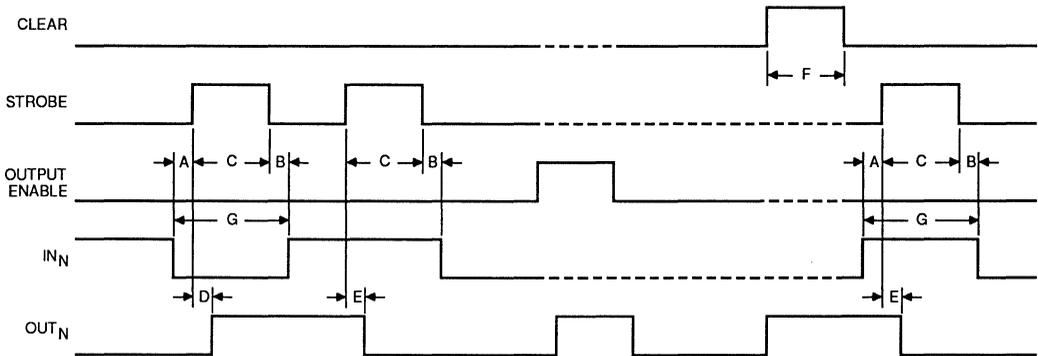
MIC58P01



Electrical Characteristics: at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 70\text{V}, T_A = +25^\circ\text{C}$			50	μA
		$V_{CE} = 70\text{V}, T_A = +70^\circ\text{C}$			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\text{mA}$		0.9	1.1	V
		$I_C = 200\text{mA}$		1.1	1.3	
		$I_C = 350\text{mA}, V_{DD} = 7.0\text{V}$		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
		$V_{DD} = 12\text{V}$	10.5			
	$V_{DD} = 10\text{V}$	8.5				
	$V_{DD} = 5.0\text{V}$ (See Note)	3.5				
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50	200		$\text{k}\Omega$
		$V_{DD} = 10\text{V}$	50	300		
		$V_{DD} = 5.0\text{V}$	50	600		
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\text{V}$, Outputs Open		1.0		mA
		$V_{DD} = 10\text{V}$, Outputs Open		0.9		
		$V_{DD} = 5.0\text{V}$, Outputs Open		0.7		
Current Limit				600		mA
Under Voltage Lockout				4.5		V
Thermal Shutdown			160	165		$^\circ\text{C}$
Clamp Diode Leakage Current	I_R	$V_R = 50\text{V}, T_A = +25^\circ\text{C}$			50	μA
		$V_R = 50\text{V}, T_A = +70^\circ\text{C}$			100	
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Timing Conditions

(Logic Levels are V_{DD} and Ground)

- A. Minimum data active time before strobe enabled (data set-up time) 50 nS
- B. Minimum data active time after strobe disabled (data hold time) 50 nS
- C. Minimum strobe pulse width 125 nS
- D. Typical time between strobe activation and output on to off transition 500 nS
- E. Typical time between strobe activation and output off to on transition 500 nS
- F. Minimum clear pulse width 300 nS
- G. Minimum data pulse width 225 nS

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current limit is activated, the output ENABLE/RESET pin must be pulled high and returned to a low state.

Truth Table

IN _N	Strobe	Clear	Output Enable	OUT _N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant

t-1 = previous output state

t = present output state



MIC5820 Family

Serial-Input, Latched Drivers

Preliminary Information

General Description

BiCMOS technology gives the MIC5820 family flexibility beyond the reach of standard logic buffers and power driver arrays. These devices each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches and eight bipolar current-sink Darlington output drivers. Except for maximum driver output voltage ratings, the MIC5821, MIC5822, and MIC5823 are identical.

These devices have greatly improved data-input rates. With a 5V logic supply, they will typically operate at better than 5MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL and DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

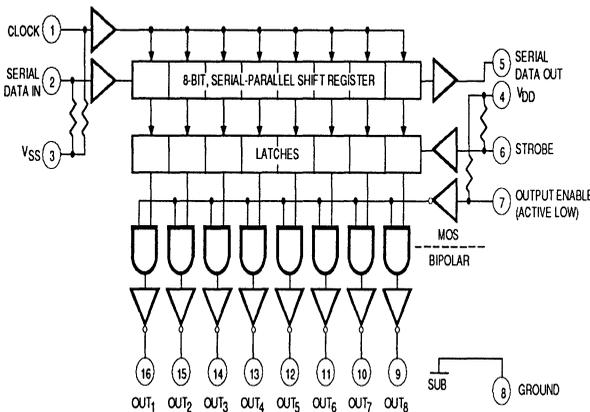
Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- 16-Pin Dual In-Line Plastic Package

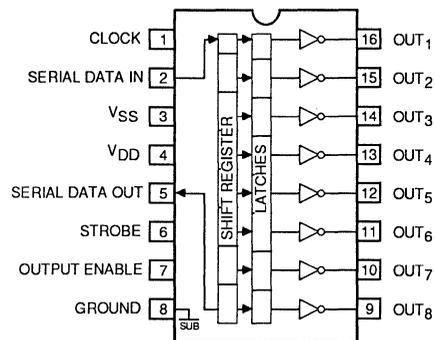
Ordering Information

Part Number	Temperature Range	Package
MIC5821BN	-40°C to +85°C	16-pin Plastic DIP
MIC5822BN	-40°C to +85°C	16-pin Plastic DIP
MIC5823BN	-40°C to +85°C	16-pin Plastic DIP

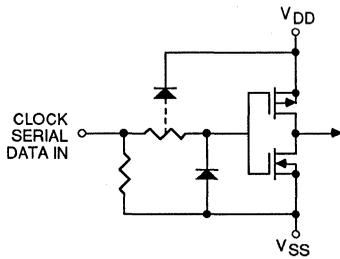
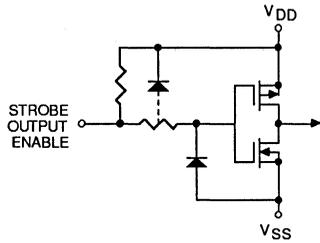
Functional Diagram



Pin Configuration



Typical Input Circuits



Absolute Maximum Ratings (Note 1)

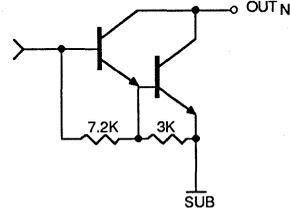
at 25°C Free-Air Temperature and $V_{SS} = 0V$

Output Voltage, V_{CE} (MIC5821)	50V
(MIC5822)	80V
(MIC5823)	100V
Logic Supply Voltage, V_{DD}	15V
Input Voltage Range, V_{IN}	-0.3V to $V_{DD} + 0.3V$
Continuous Output Current, I_{OUT}	500mA
Package Power Dissipation, P_D (Note 1)	1.67W
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature Range, T_S	-65°C to +125°C

Note 1: Derate at the rate of 16.7mW/°C above $T_A = +25°C$

Note 2: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Output Driver



Maximum Allowable Duty Cycle

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 12V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	73%	62%	55%	47%	40%
7	83%	71%	62%	54%	46%
6	97%	82%	72%	63%	53%
5	100%	98%	87%	75%	63%
4	100%	100%	100%	93%	79%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = 0\text{V}$ (unless otherwise specified)

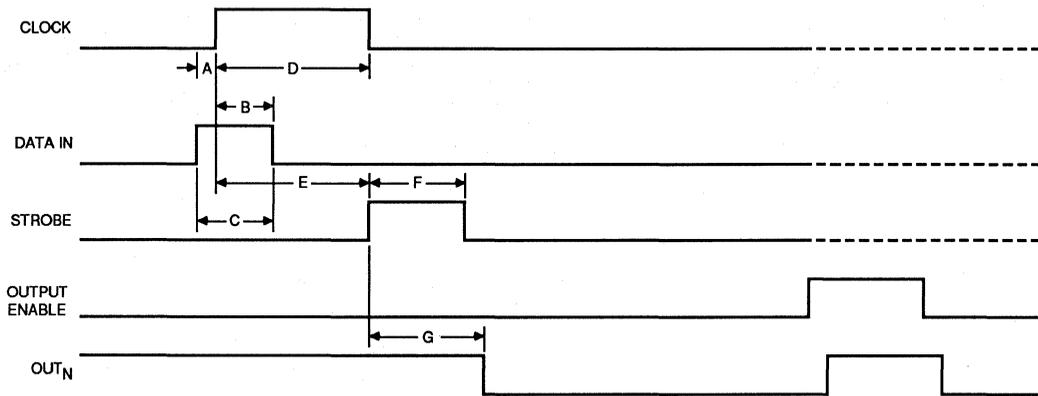
Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Unit
Output Leakage Current	I_{CEX}	MIC5821A	$V_{OUT} = 50\text{V}$		50	μA
			$V_{OUT} = 50\text{V}, T_A = +70^\circ\text{C}$		100	
		MIC5822A	$V_{OUT} = 80\text{V}$		50	
			$V_{OUT} = 80\text{V}, T_A = +70^\circ\text{C}$		100	
		MIC5823A	$V_{OUT} = 100\text{V}$		50	
			$V_{OUT} = 100\text{V}, T_A = +70^\circ\text{C}$		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\text{mA}$		1.1	V
			$I_{OUT} = 200\text{mA}$		1.3	
			$I_{OUT} = 350\text{mA}, V_{DD} = 7.0\text{V}$		1.6	
Input Voltage	$V_{IN(0)}$	ALL			0.8	V
		ALL	$V_{DD} = 12\text{V}$	10.5		
	$V_{DD} = 10\text{V}$		8.5			
	$V_{DD} = 5.0\text{V}$		3.5			
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\text{V}$	50		$\text{k}\Omega$
			$V_{DD} = 10\text{V}$	50		
			$V_{DD} = 5.0\text{V}$	50		
Supply Current	$I_{DD(ON)}$	ALL	One Driver ON, $V_{DD} = 12\text{V}$		4.5	mA
			One Driver ON, $V_{DD} = 10\text{V}$		3.9	
			One Driver ON, $V_{DD} = 5.0\text{V}$		2.4	
	$I_{DD(OFF)}$	ALL	All Drivers OFF, $V_{DD} = 5.0\text{V}$, All Inputs = 0V		1.6	
			All Drivers OFF, $V_{DD} = 12\text{V}$, All Inputs = 0V		2.9	

3

MIC5840 Family Truth Table

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable	Output Contents						
		I_1	I_2	I_3	I_8	R_1			R_2	R_3	R_8	I_1	I_2		I_3	I_8	P_1	P_2	P_3
H		H	R_1	R_2	R_7	R_7																
L		L	R_1	R_2	R_7	R_7																
X		R_1	R_2	R_3	R_8	R_8																
		X	X	X	X	X	L															
		P_1	P_2	P_3	P_8	P_8	H															
																						
																						

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State



Timing Conditions

($T_A = +25^\circ\text{C}$, Logic Levels are V_{DD} and V_{SS})

$V_{DD} = 5.0\text{V}$

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	75 nS
B. Minimum Data Active Time After Clock Pulse (Data Hold Time)	75 nS
C. Minimum Data Pulse Width	150 nS
D. Minimum Clock Pulse Width	150 nS
E. Minimum Time Between Clock Activation and Strobe	300 nS
F. Minimum Strobe Pulse Width	100 nS
G. Typical Time Between Strobe Activation and Output Transition	500 nS

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.



MIC5840 Family

8-Bit Serial-Input, Latched Driver Family

Preliminary Information

General Description

Using BiCMOS technology, the MIC5840 integrated circuits were fabricated to be used in a wide variety of peripheral power driver applications. The three devices in this series each have an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlingtong output drivers.

These three devices differ only in maximum voltage ratings. The MIC5843 offers premium performance with a minimum output-breakdown voltage rating of 100V (50V sustaining). The drivers can be operated with a split supply where the negative supply is up to $-20V$.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids and other inductive loads.

These devices have improved speed characteristics. With a 5V logic supply, they will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of $-40^{\circ}C$

to $+85^{\circ}C$. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

Features

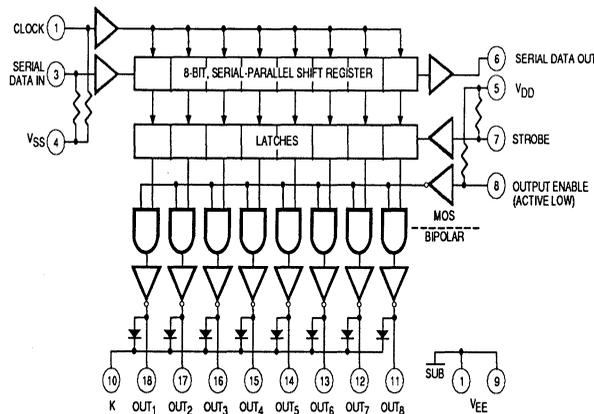
- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- 18-Pin Dual In-Line Plastic Package

Ordering Information

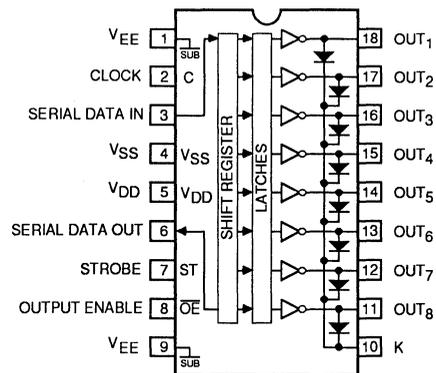
Part Number	Temperature Range	Package
MIC5841BN	$-40^{\circ}C$ to $+85^{\circ}C$	18-pin Plastic DIP
MIC5842BN	$-40^{\circ}C$ to $+85^{\circ}C$	18-pin Plastic DIP
MIC5843BN	$-40^{\circ}C$ to $+85^{\circ}C$	18-pin Plastic DIP

3

Functional Diagram



Pin Configuration



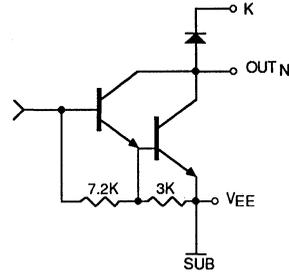
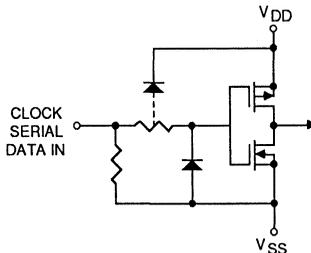
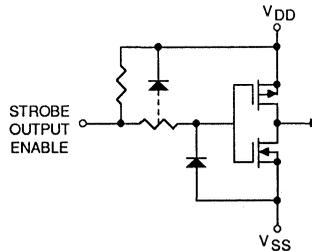
Absolute Maximum Ratings (Note 1, 2, 3)at 25°C Free-Air Temperature and $V_{SS} = 0V$

Output Voltage, V_{CE} (MIC5841)	50V
(MIC5842)	80V
(MIC5843)	100V
Output Voltage, $V_{CE(SUS)}$ (MIC5841) (Note 1)	35V
(MIC5842)	50V
(MIC5843)	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage, V_{EE}	-20V
Input Voltage Range, V_{IN}	-0.3V to $V_{DD} + 0.3V$
Continuous Output Current, I_{OUT}	500mA
Package Power Dissipation, P_D (Note 2)	1.82W
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature Range, T_S	-65°C to +125°C

Note 1: For inductive load applications.

Note 2: Derate at the rate of 18.2mW/°C above $T_A = +25°C$

Note 3: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Output Driver**Typical Input Circuits**

Maximum Allowable Duty Cycle $V_{DD} = 5.0V$

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 5.0V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

 $V_{DD} = 12V$

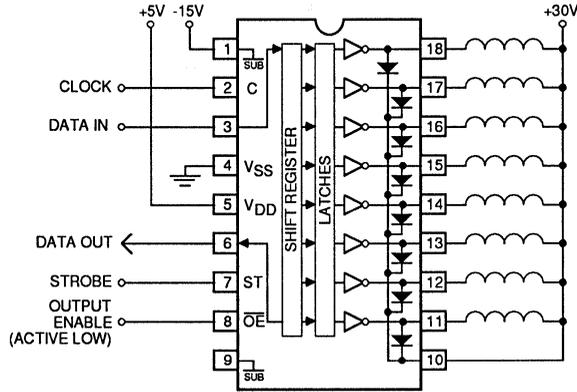
Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 12V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits		
				Min.	Max.	Unit
Output Leakage Current	I_{CEX}	MIC5841	$V_{OUT} = 50\text{V}$		50	μA
			$V_{OUT} = 50\text{V}, T_A = +70^\circ\text{C}$		100	
		MIC5842	$V_{OUT} = 80\text{V}$		50	
			$V_{OUT} = 80\text{V}, T_A = +70^\circ\text{C}$		100	
		MIC5843	$V_{OUT} = 100\text{V}$		50	
			$V_{OUT} = 100\text{V}, T_A = +70^\circ\text{C}$		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\text{mA}$		1.1	V
			$I_{OUT} = 200\text{mA}$		1.3	
			$I_{OUT} = 350\text{mA}, V_{DD} = 7.0\text{V}$		1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	MIC5841	$I_{OUT} = 350\text{mA}, L = 2\text{mH}$	35		V
		MIC5842	$I_{OUT} = 350\text{mA}, L = 2\text{mH}$	50		
		MIC5843	$I_{OUT} = 350\text{mA}, L = 2\text{mH}$	50		
Input Voltage	$V_{IN(0)}$	ALL			0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 12\text{V}$	10.5		
			$V_{DD} = 10\text{V}$	8.5		
			$V_{DD} = 5.0\text{V}$	3.5		
Input Resistance	R_{IN}	ALL	$V_{DD} = 12\text{V}$	50		$\text{k}\Omega$
			$V_{DD} = 10\text{V}$	50		
			$V_{DD} = 5.0\text{V}$	50		
Supply Current	$I_{DD(ON)}$	ALL	All Drivers ON, $V_{DD} = 12\text{V}$		16	mA
			All Drivers ON, $V_{DD} = 10\text{V}$		14	
			All Drivers ON, $V_{DD} = 5.0\text{V}$		8.0	
	$I_{DD(OFF)}$	ALL	All Drivers OFF, $V_{DD} = 12\text{V}$		2.9	
			All Drivers OFF, $V_{DD} = 10\text{V}$		2.5	
			All Drivers OFF, $V_{DD} = 5.0\text{V}$		1.6	
Clamp Diode Leakage Current	I_R	MIC5841	$V_R = 50\text{V}$		50	μA
		MIC5842	$V_R = 80\text{V}$		50	
		MIC5843	$V_R = 100\text{V}$		50	
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350\text{mA}$		2.0	V

Typical Application

Relay/Solenoid Driver MIC5843





MIC58P42

8-Bit Serial-Input Latched Driver

Preliminary Information

General Description

The MIC58P42 is fabricated using BiCMOS technology for use in a wide variety of peripheral power driver applications. This device has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlingtons output drivers, with transient protection diodes.

This device, which is similar to the MIC5842, has added features such as thermal shutdown, undervoltage lockout (UVLO), and overcurrent shutdown which makes it "bullet proof", ideal for automotive and industrial applications. During thermal shutdown all channels are disabled. An overcurrent condition shuts down only the affected channel, and must be 1µS long before shutdown occurs. To turn the channel back on, the OUTPUT ENABLE/RESET pin must be pulsed high. The drivers can be operated with a split supply where the negative supply is up to -20V. Thermal shutdown occurs at a junction temperature of 165°C. UVLO prevents operation below 4.5V with 0.5V hysteresis.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids and other inductive loads.

These devices have improved speed characteristics. With a 5V logic supply, they will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits

Features

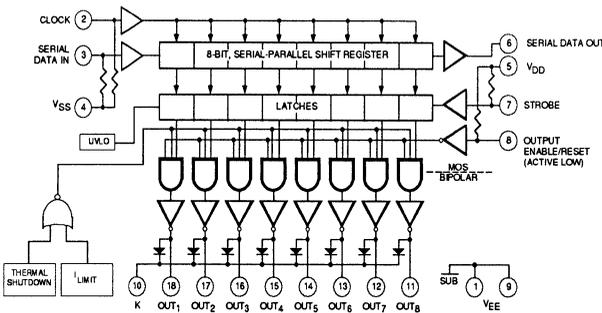
- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- 18-Pin Dual In-Line Plastic Package
- Thermal Shutdown
- Undervoltage Lockout
- Output Current Limit

Ordering Information

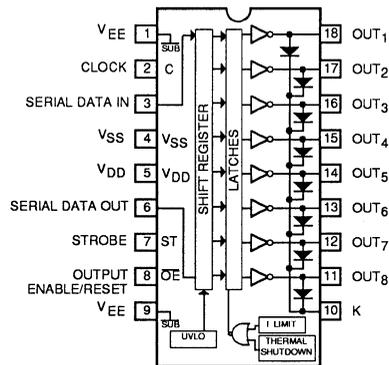
Part Number	Temperature Range	Package
MIC58P42BN	-40°C to +85°C	18-pin Plastic DIP

3

Functional Diagram



Pin Configuration



may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of -40°C to $+85^{\circ}\text{C}$. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

Absolute Maximum Ratings (Note 1, 2, 3)

at 25°C Free-Air Temperature and $V_{SS} = 0\text{V}$

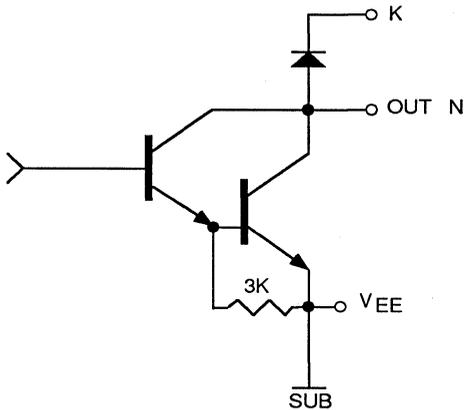
Output Voltage	70V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage, V_{EE}	-20V
Input Voltage Range, V_{IN}	-0.3V to $V_{DD} + 0.3\text{V}$
Continuous Output Current, I_{OUT}	500mA
Package Power Dissipation, P_D (Note 2)	1.82W
Operating Temperature Range, T_A	-40°C to $+85^{\circ}\text{C}$
Storage Temperature Range, T_S	-65°C to $+150^{\circ}\text{C}$

Note 1: For inductive load applications.

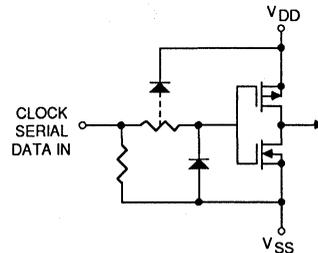
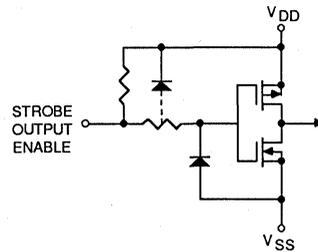
Note 2: Derate at the rate of $18.2\text{mW}/^{\circ}\text{C}$ above $T_A = +25^{\circ}\text{C}$

Note 3: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Output Driver



Typical Input Circuits



Maximum Allowable Duty Cycle

$V_{DD} = 5.0V$

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 5.0V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

$V_{DD} = 12V$

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 12V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}			50	μA
		$T_A = +70^\circ\text{C}$		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{mA}$		1.1	V
		$I_{OUT} = 200\text{mA}$		1.3	
		$I_{OUT} = 350\text{mA}$, $V_{DD} = 7.0\text{V}$		1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 350\text{mA}$, $L = 2\text{mH}$	50		V
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{V}$	10.5		
		$V_{DD} = 10\text{V}$	8.5		
		$V_{DD} = 5.0\text{V}$	3.5		
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50		$\text{k}\Omega$
		$V_{DD} = 10\text{V}$	50		
		$V_{DD} = 5.0\text{V}$	50		
Supply Current	$I_{DD(ON)}$	All Drivers ON, $V_{DD} = 12\text{V}$		16	mA
		All Drivers ON, $V_{DD} = 10\text{V}$		14	
		All Drivers ON, $V_{DD} = 5.0\text{V}$		8.0	
	$I_{DD(OFF)}$	All Drivers OFF, $V_{DD} = 12\text{V}$		2.9	
		All Drivers OFF, $V_{DD} = 10\text{V}$		2.5	
		All Drivers OFF, $V_{DD} = 5.0\text{V}$		1.6	
Clamp Diode Leakage Current	I_R	$V_R = 70\text{V}$		50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		2.0	V
Current Limit			500		mA
Undervoltage Lockout				4.5	V
Thermal Shutdown			160		$^\circ\text{C}$



MIC59P50

Latched Driver

Preliminary Information

General Description

The MIC59P50 latched driver is a high-voltage, high-current integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Although similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, undervoltage lockout (UVLO), and short circuit current limit.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The driver can be operated with a split supply, where the negative supply is down to -20V.

Data input rates are greatly improved in these devices. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

The MIC59P50 has open-collector outputs and integral

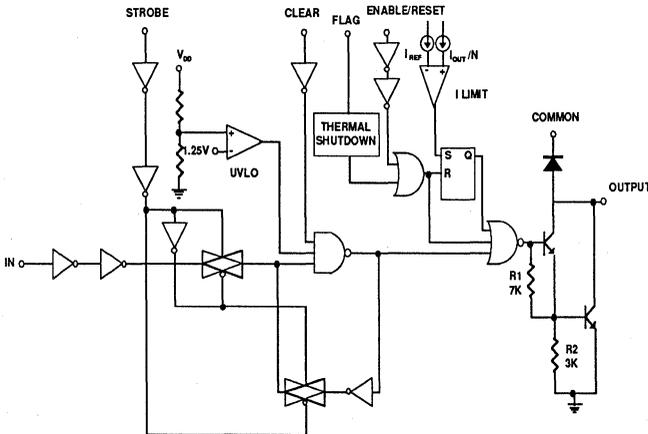
Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Output Current Limit (500 mA minimum)
- Undervoltage Lockout
- Thermal Shutdown

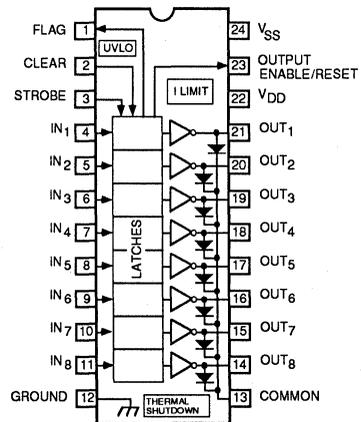
Ordering Information

Part Number	Temperature Range	Package
MIC59P50BN	-40°C to +85°C	24-pin Plastic DIP

Functional Diagram



Pin Configurations



MIC59P50

diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 70 V in the OFF state. Because of limitations on power package dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

Each of these eight outputs has an independent current limit of 500 mA minimum. Upon current limit, the affected channel will shut down until V_{DD} is cycled low or the ENABLE/RESET pin is pulsed high. Current pulses less than 1 μ S will not activate current limiting. Temperatures above 165°C will shut down the device and activate the open collector FLAG output at pin 1. The UVLO circuit prevents operation below 4.5V; hysteresis of 0.5V is provided.

The MIC59P50 is supplied in a 24-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

Absolute Maximum Ratings: (Notes 1, 2)

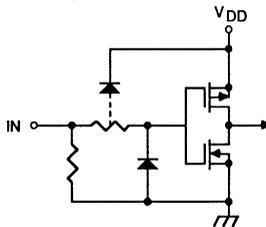
at +25°C Free-Air Temperature

Output Voltage, V_{CE}	70 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	-0.3 V to $V_{DD} + 0.3$ V
Continuous Collector Current, I_C	500 mA
Package Power Dissipation MIC59P50 (Note 1)	2.25 W
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature Range, T_S	-65°C to +125°C

Note 1: Derate at the rate of 20 mW/°C above $T_A = +25^\circ\text{C}$

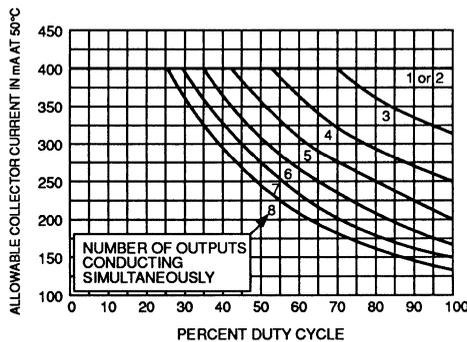
Note 2: Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input



Allowable Output Current As A Function of Duty Cycle

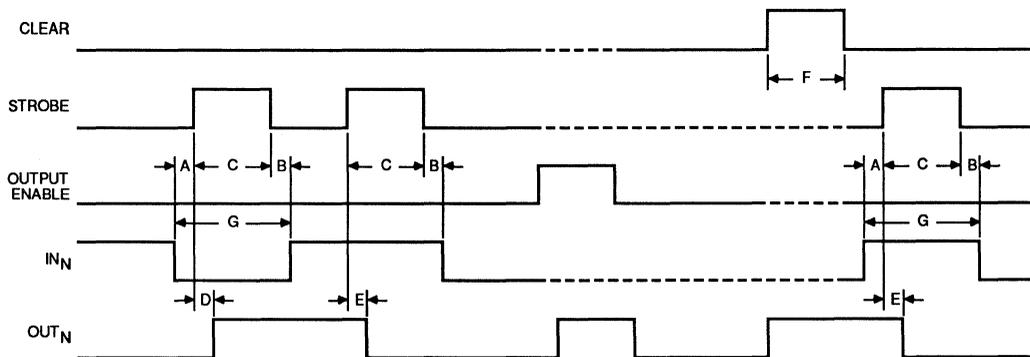
MIC59P50



Electrical Characteristics: at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 50\text{V}$, $T_A = +25^\circ\text{C}$			50	μA
		$V_{CE} = 50\text{V}$, $T_A = +70^\circ\text{C}$			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\text{mA}$		0.9	1.1	V
		$I_C = 200\text{mA}$		1.1	1.3	
		$I_C = 350\text{mA}$, $V_{DD} = 7.0\text{V}$		1.3	1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
		$V_{DD} = 12\text{V}$	10.5			
	$V_{DD} = 10\text{V}$	8.5				
	$V_{DD} = 5.0\text{V}$ (See Note)	3.5				
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50	200		k Ω
		$V_{DD} = 10\text{V}$	50	300		
		$V_{DD} = 5.0\text{V}$	50	600		
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\text{V}$, Outputs Open		1.0	2.0	mA
		$V_{DD} = 10\text{V}$, Outputs Open		0.9	1.7	
		$V_{DD} = 5.0\text{V}$, Outputs Open		0.7	1.0	
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\text{V}$, Outputs Open, Inputs = 0 V			200	μA
$V_{DD} = 5.0\text{V}$, Outputs Open, Inputs = 0 V		50	100			
Clamp Diode Leakage Current	I_R	$V_R = 50\text{V}$, $T_A = +25^\circ\text{C}$			50	μA
		$V_R = 50\text{V}$, $T_A = +70^\circ\text{C}$			100	
Current Limit	I_{LIM}	$R_L = 0\Omega$	500			mA
Under Voltage Lockout	V_{LO}			4.5		V
UVLO Hysteresis	V_{LOH}			0.5		V
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		1.7	2.0	V
Thermal Shutdown			160	165		$^\circ\text{C}$

NOTE 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".



Timing Conditions

(Logic Levels are V_{DD} and Ground)

- A. Minimum data active time before strobe enabled (data set-up time) 50 nS
- B. Minimum data active time after strobe disabled (data hold time) 50 nS
- C. Minimum strobe pulse width 125 nS
- D. Typical time between strobe activation and output on to off transition 500 nS
- E. Typical time between strobe activation and output off to on transition 500 nS
- F. Minimum clear pulse width 300 nS
- G. Minimum data pulse width 225 nS

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current limit is activated, the OUTPUT ENABLE must be pulsed high to restore operation.

Truth Table

IN _N	Strobe	Clear	Output Enable	OUT _N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant

t-1 = previous output state

t = present output state



MIC59P60

8-Bit Serial-Input Latched Driver

Preliminary Information

General Description

Using BiCMOS technology, the MIC59P60 is fabricated for a wide variety of peripheral power driver applications. This device has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sink Darlingtons output drivers.

This device, which is similar to the MIC5842, has additional features such as thermal shutdown, undervoltage lockout, and short circuit current limit. These features serve to "bullet proof" this device, making it ideal for automotive or industrial applications.

The MIC59P60 offers a minimum output-breakdown voltage rating of 70V (50V sustaining). The drivers can be operated with a split supply where the negative supply, V_{EE} , is up to -20V.

The 500 mA outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids and other inductive loads.

This device offers improved speed characteristics. With a 5V logic supply, it will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS logic levels. TTL or DTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

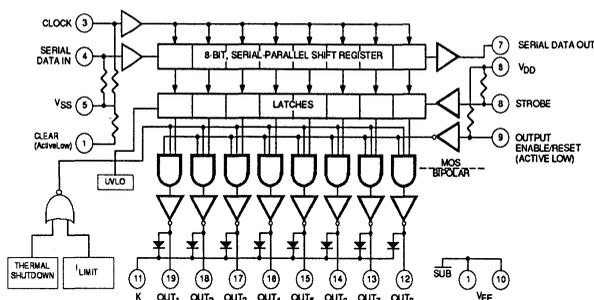
Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low-Power CMOS Logic and Latches
- High-Voltage Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- 20-Pin Dual In-Line Plastic Package
- Output Current Limit (500 mA min)
- Under Voltage Lockout
- Thermal Shutdown

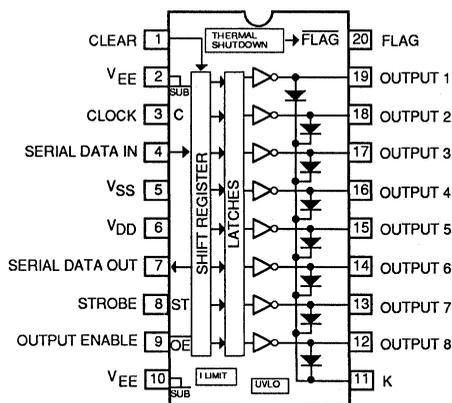
Ordering Information

Part Number	Temperature Range	Package
MIC59P60BN	-40°C to +85°C	20-pin Plastic DIP

Functional Diagram



Pin Configuration



The MIC59P60 is supplied in 20-pin dual in-line plastic packages for operation over the temperature range of -40°C to $+85^{\circ}\text{C}$. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current might require a reduction in duty cycle. A copper-alloy lead frame provides for maximum package power dissipation.

Absolute Maximum Ratings (Note 1, 2, 3)

at 25°C Free-Air Temperature and $V_{SS} = 0\text{V}$

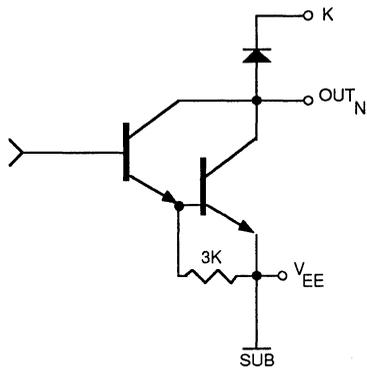
Output Voltage, V_{CE}	70V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage, V_{EE}	-20V
Input Voltage Range, V_{IN}	-0.3V to $V_{DD} + 0.3\text{V}$
Continuous Output Current, I_{OUT}	500mA
Package Power Dissipation, P_D (Note 2)	2.0W
Operating Temperature Range, T_A	-40°C to $+85^{\circ}\text{C}$
Storage Temperature Range, T_S	-65°C to $+125^{\circ}\text{C}$

Note 1: For Inductive load applications.

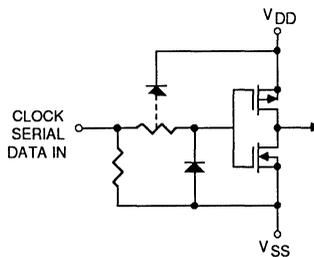
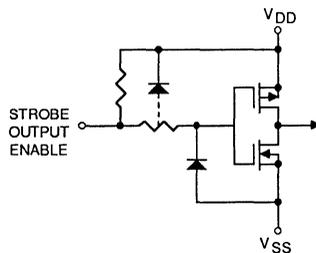
Note 2: Derate at the rate of $18.2\text{mW}/^{\circ}\text{C}$ above $T_A = +25^{\circ}\text{C}$

Note 3: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Output Driver



Typical Input Circuits



Maximum Allowable Duty Cycle

$V_{DD} = 5.0V$

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 5.0V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

$V_{DD} = 12V$

Number of Outputs ON ($I_{OUT} = 200mA$ $V_{DD} = 12V$)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Electrical Characteristics at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

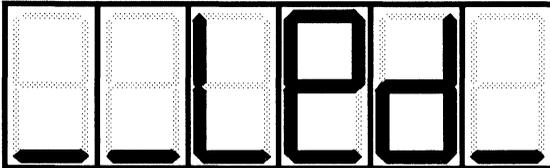
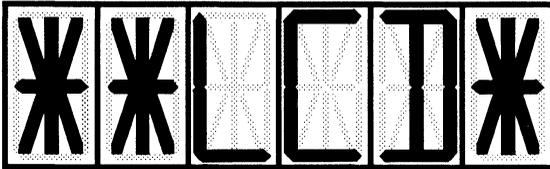
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Unit
Output Leakage Current	I_{CEX}	$V_{OUT} = 70\text{V}$		50	μA
		$V_{OUT} = 70\text{V}$, $T_A = +70^\circ\text{C}$		100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{mA}$		1.1	V
		$I_{OUT} = 200\text{mA}$		1.3	
		$I_{OUT} = 350\text{mA}$, $V_{DD} = 7.0\text{V}$		1.6	
Collector-Emitter	$V_{CE(SUS)}$	$I_{OUT} = 350\text{mA}$, $L = 2\text{mH}$	50		V
Input Voltage	$V_{IN(0)}$			0.8	V
	$V_{IN(1)}$	$V_{DD} = 12\text{V}$	10.5		
		$V_{DD} = 10\text{V}$	8.5		
		$V_{DD} = 5.0\text{V}$	3.5		
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50		$\text{k}\Omega$
		$V_{DD} = 10\text{V}$	50		
		$V_{DD} = 5.0\text{V}$	50		
Supply Current	$I_{DD(ON)}$	All Drivers ON, $V_{DD} = 12\text{V}$		16	mA
		All Drivers ON, $V_{DD} = 10\text{V}$		14	
	$I_{DD(OFF)}$	All Drivers ON, $V_{DD} = 5.0\text{V}$		8.0	
		All Drivers OFF, $V_{DD} = 12\text{V}$		2.9	
		All Drivers OFF, $V_{DD} = 10\text{V}$		2.5	
		All Drivers OFF, $V_{DD} = 5.0\text{V}$		1.6	
Clamp Diode Leakage Current	I_R	$V_R = 70\text{V}$		50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		2.0	V
Output Current Limit	I_{lim}		500		mA
UVLO Level	$V_{DD\ MIN}$			4.5	V
UVLO Hysteresis	UVLO (hyst)		0.2		V
Thermal Shutdown			160		$^\circ\text{C}$



SECTION 4: DISPLAY DRIVERS

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***If your product's
display is:***



Vacuum Fluorescent

Consider:

MIC7233 MIC8013
MIC8010 MIC8014
MIC8011 MIC8030
MIC8012 MIC8031

MIC4350 MIC50396
MIC4807 MIC50397
MIC5002 MIC50398
MIC5005 MIC50399
MIC5007 MM5450
MIC50395 MM5451

MIC4807 MIC8014
MIC8010 MIC8030
MIC8012 MIC8031
MIC8013

NUMERICAL

MIC4350
MIC4807
MIC5002
MIC5005
MIC5007
MIC50395
MIC50396
MIC50397
MIC50398
MIC50399

ALPHANUMERIC

MIC7233
MIC8010
MIC8011
MIC8012
MIC8013
MIC8014
MIC8030
MIC8031
MM5450
MM5451

DOT MATRIX

MIC8010
MIC8011
MIC8012
MIC8013
MIC8014
MIC8030
MIC8031
MM5450
MM5451



Display Driver Selection Guide

All Micrel Display Drivers are available in die form. Special package options are available on most display drivers: please contact factory for details.

DEVICE	Number of Segments	Serial Input/Latched Output	Counter	7 Segment Decoder	BCD Output	LED Driver	LCD Driver	Vacuum Fluorescent Driver	Single Supply	Single or Multiple Supplies	PACKAGE
MIC4350 Counter/Latch Decoder & Driver	7	•	•	•		•			•	•	16 Pin PDIP
	7	•	•	•		•			•	•	16 Pin CerDIP
MIC4807 Protected Addressable Low Side Driver	8					•		•	•	•	See "Latched Driver" Section.
	8					•		•	•	•	
MIC5002 4 Digit Counter Decoder	4x7	•	•	•	•	•			•	•	28 Pin DIP
MIC5005 4 Digit Counter Decoder	4x7	•	•	•		•			•	•	24 Pin PDIP
MIC5007 4 Digit Counter Decoder	4x4	•	•		•	•			•	•	16 Pin PDIP
MIC50395 6 Decade Counter Decoder to 9999.99	6x7	•	•	•	•	•			•		40 Pin PDIP
MIC50396 6 Decade Counter Decoder to 99:59:59	6x7	•	•	•	•	•			•		40 Pin PDIP
MIC50397 6 Decade Counter Decoder to 59:59.99	6x7	•	•	•	•	•			•		40 Pin PDIP
MIC50398 6 Decade Counter Decoder	6x7		•	•		•			•		28 Pin PDIP
MIC50399 6 Decade Counter Decoder	6x7		•		•	•			•		28 Pin PDIP
MIC7233 Alphanum. LCD Dr.	4x18	•					•		•		40 Pin PDIP
MIC8010 Dichroic LCD Driver	30	•					•	•	•	•	40 Pin PDIP
	30	•					•	•	•	•	40 Pin LCC
MIC8011 Dichroic LCD Driver	38	•					•	•	•	•	48 Pin PDIP
	38	•					•	•	•	•	52 Pin QFP
MIC8012 Dichroic LCD Driver With Switching Regulator	30	•					•	•	•	•	40 Pin PDIP
	30	•					•	•	•	•	
MIC8013 Dichroic LCD Driver	30	•					•	•	•	•	40 Pin DIP /LCC
MIC8014 Dichroic LCD Driver	32	•					•	•	•	•	44 Pin PLCC
	32	•					•	•	•	•	44 Pin Cer Quad
MIC8030 50V LCD Driver	32	•					•	•	•	•	44 Pin LCC/PLCC
	38	•					•	•	•	•	48 Pin PDIP
MIC8031 100V LCD Driver	32	•					•	•	•	•	44 Pin LCC/PLCC
	38	•					•	•	•	•	48 Pin PDIP
MM5450 LED Display Driver	34	•				•			•		40 Pin PDIP
	34	•				•			•		44 Pin PLCC
MM5451 LED Display Driver	35	•				•			•		40 Pin PDIP
	35	•				•			•		44 Pin PLCC



MIC4350

CMOS Counter/Latch Decoder/Driver

General Description

The MIC4350 is a CMOS device combining the functions of an NBCD counter, four-bit latch, and a seven-segment decoder/driver. It provides up to 25 mA drive/segment for current sinking for displays which require current sinking in the active mode. A lamp blanking input is provided for intensity modulation. A lamp test feature is also available. Synchronous or asynchronous operation is available when the high driving serial output is used in conjunction with the Enable input and some external gating. Automatic suppression of leading zeros in the display is provided by the counter Reset.

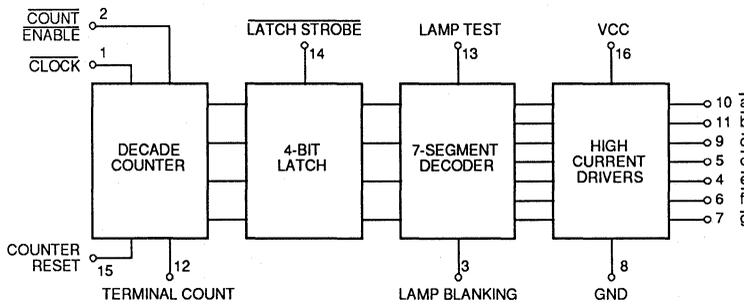
Features

- CMOS version of TTL equivalent MC4350L, 4350P
- 25 mA driver/segment for current sinking
- Synchronous or asynchronous operation
- Lamp blanking for intensity modulation
- Leading zero suppression

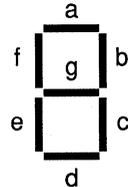
Applications

- Incandescent lamp drivers
- Panel displays
- Modulated intensity functions

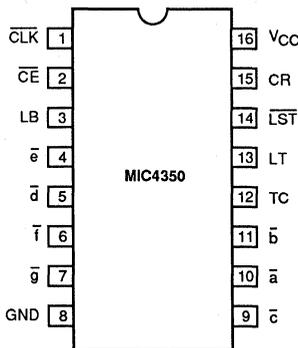
Functional Diagram



Segment Identification



Pin Configuration



Ordering Information*

Part Number	Temperature Range	Package
MIC4350AJ	-55°C to +125°C	16-pin Ceramic DIP
MIC4350CN	0°C to +70°C	16-pin Plastic DIP

* Contact factory for other options

Absolute Maximum Ratings

V _{CC} , DC Supply Voltage	7 V
V _{IN} , Input Voltage Range	-0.5 V to V _{CC} +0.5 V
I _{OL2} , (Continuous), Low Level Output Driver Current	25 mA
P _D , Power Dissipation	300 mW
T _A , Operating Temperature Range	-55°C to +125°C
T _{STG} , Storage Temperature Range	-65°C to +150°C

Pin Function

1.	CLK	If \overline{CE} and CR are both at "0" the counter advances one state when clock changes "1" to "0".
2.	\overline{CE}	Logic "0" enables count. Logic "1" inhibits count.
3.	LB	No effect if LT at "1". With LT at "0", a "1" at LB turns off outputs \overline{a} to \overline{g} ; a "0" allows \overline{a} to \overline{g} to display normally.
4.	\overline{e}	Segment identification.
5.	\overline{d}	Segment identification.
6.	\overline{f}	Segment identification.
7.	\overline{g}	Segment identification.
8.	GND	Ground.
9.	\overline{c}	Segment identification.
10.	\overline{a}	Segment identification.
11.	\overline{b}	Segment identification.
12.	TC	High only when counter is in 1001 (nine) state. LB, LT, \overline{LST} have no effect.
13.	LT	"1" turns outputs \overline{a} to \overline{g} on regardless of other inputs.
14.	\overline{LST}	"0" stores counter output data as it was prior to "1" to "0" transition. "1" allows decoder to be driven directly from counter outputs.
15.	CR	"1" resets counter to 1010 (ten). This turns all transistors off on next latch strobe providing automatic zero suppression. Next enabled clock pulse advances counter to 0001.
16.	V _{CC}	Supply voltage.

Recommended Operating Conditions

V _{CC} , DC Supply Voltage	4.5 V to 5.5 V
V _{IN} , DC Input Voltage	0 to V _{CC}
T _A , Operating Temperature	A version: -55°C to +125°C C version: 0°C to +70°C

Functional Description

Count Enable (\overline{CE}) may be changed with (\overline{CLK}) either high or low.

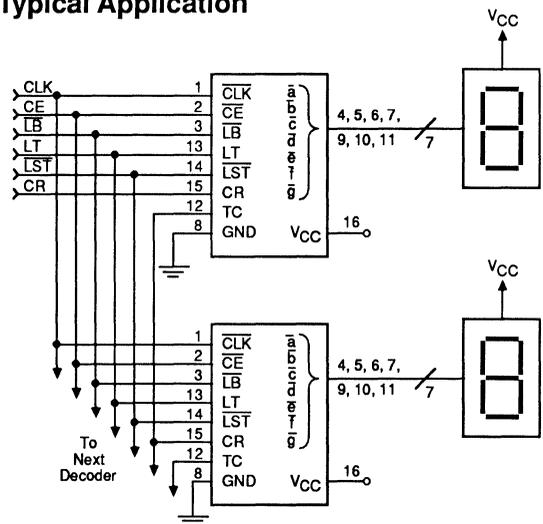
Counter reset (\overline{CR}) overrides count enable (\overline{CE}) and clock (CLK). It may be changed regardless of levels present at count enable (\overline{CE}) and clock (CLK).

Latch strobe (\overline{LST}), lamp blanking (LB) and lamp test (LT) may be changed regardless of levels at count enable (\overline{CE}), clock (CLK) and counter reset (CR).

Refer to timing diagram if a logic "1" to "0" transition on clock (CLK) can occur while levels are changing on count enable (\overline{CE}) or latch strobe (\overline{LST}), or if a logic "0" to "1" transition of counter reset (CR) can occur simultaneously with a "0" to "1" transition of latch strobe (\overline{LST}).

Tie all unused inputs to ground except for latch strobe (\overline{LST}), which must be returned to a logic "1" level if not used.

Typical Application



Functional Truth Table

Function	Input						Output							
	CLOCK	$\overline{\text{CE}}$	CR	$\overline{\text{LST}}$	LT	LB	TC	$\overline{\text{a}}$	$\overline{\text{b}}$	$\overline{\text{c}}$	$\overline{\text{d}}$	$\overline{\text{e}}$	$\overline{\text{f}}$	$\overline{\text{g}}$
Lamp Test	X	X	X	X	1	X	—	0	0	0	0	0	0	0
Lamp Blanking	X	X	X	X	0	1	—	1	1	1	1	1	1	1
Reset	X	X	1	1	0	0	0	1	1	1	1	1	1	1
Enable	P	1	0	1	0	0	0	1	1	1	1	1	1	1
STATE SEQUENCE	1	P1	0	0	1	0	0	0	1	0	0	1	1	1
	2	P2	0	0	1	0	0	0	0	0	1	0	0	1
	3	P3	0	0	1	0	0	0	0	0	0	1	1	0
	4	P4	0	0	1	0	0	0	1	0	0	1	1	0
	5	P5	0	0	1	0	0	0	0	1	0	0	1	0
	6	P6	0	0	1	0	0	0	0	1	0	0	0	0
	7	P7	0	0	1	0	0	0	0	0	0	1	1	1
	8	P8	0	0	1	0	0	0	0	0	0	0	0	0
	9	P9	0	0	1	0	0	1	0	0	0	0	1	0
	0	P10	0	0	1	0	0	0	0	0	0	0	0	1
	1	P11	0	0	1	0	0	0	1	0	0	1	1	1
LATCH	P	0	0	0	0	0	0	1	0	0	1	1	1	

P = Any number of pulses may be applied

P_N = n pulses on the clock input

X = Don't Care



General Description

The MIC5002/5/7 is an ion-implanted, P-channel MOS, four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MIC5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the SCAN input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low-threshold voltages for input DTL/TTL compatibility are achieved through an ion-implantation process. Enhancement mode devices, as well as depletion-mode devices, are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25mW of power.

The block diagram, Figure 1, shows all options available on the MIC5002 MOS/LSI. Other members of this family which

Features

- Single-supply operation or double-supply for higher output drive
- Multiplexed seven-segment and/or BCD outputs
- TTL-compatible inputs
- Four decades of synchronous counting
- Minimum external component count
- Low power consumption

Ordering Information

Part Number	Temperature Range	Package
MIC5002CN	0°C to +70°C	28-Pin Plastic DIP
MIC5005CN	0°C to +70°C	24-Pin Plastic DIP
MIC5007CN	0°C to +70°C	16-Pin Plastic DIP

Functional Diagram

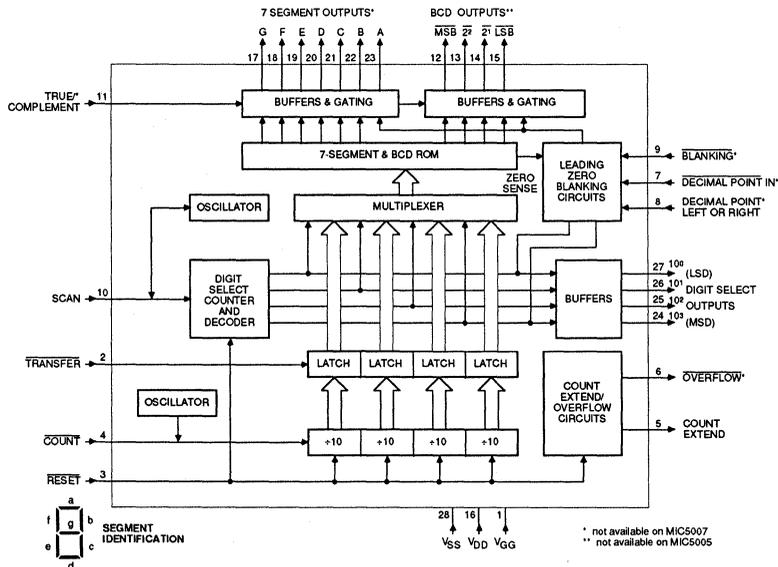


Figure 1

Pin Configurations

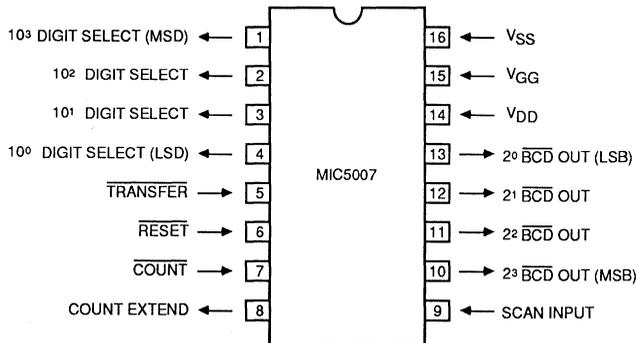
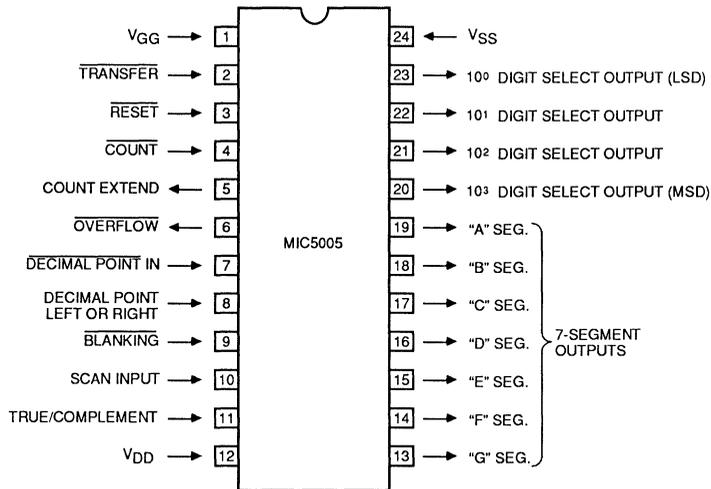
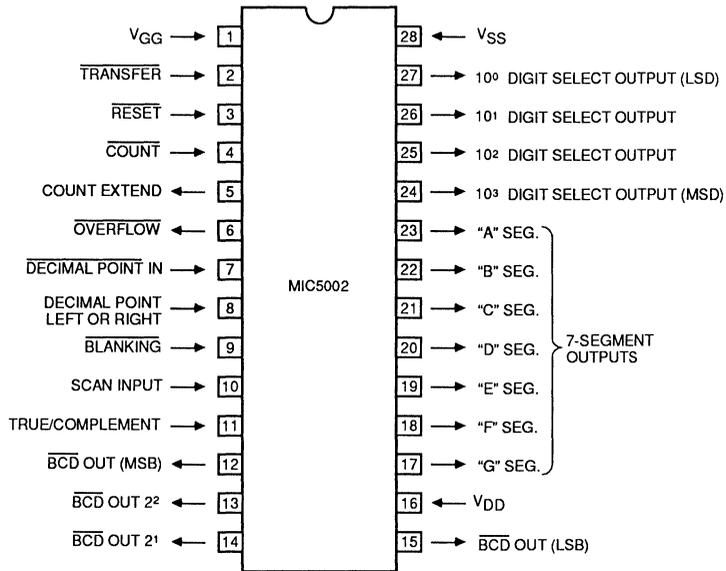


Figure 2

are different versions of this same chip are the MIC5005 and MIC5007. The MIC5005 is supplied in a 24-pin package and does not include the BCD outputs. The MIC5007 is supplied in a 16-pin package. (See Figure 2 for these members of the display counter/decoder family.)

Functional Description (MIC5002)

V_{GG}, Pin 1

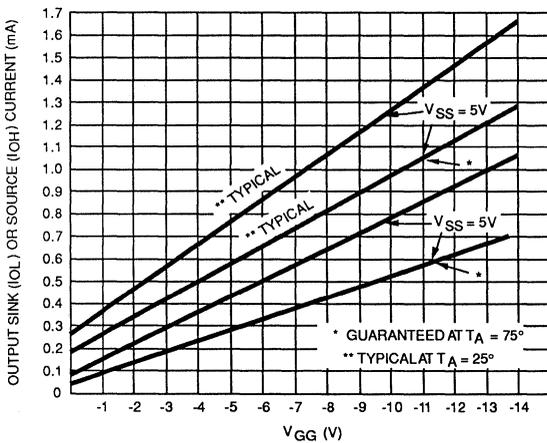
V_{GG} is the output gate drive voltage supply. It must be tied to a supply which is no greater than V_{DD} and no less than V_{DD} - 13.2V. Higher output drive capability is realized when V_{GG} is maintained at the recommended level of V_{DD} - 12V. (See Figure 3 for typical output characteristics.)

TRANSFER, Pin 2

While TRANSFER is at logic 0, data in the decade counters is continuously transferred to the latches. This input may be left at 0 for a continuous transfer and display mode or may be driven high to subsequently cause the latches to store the current counter contents.

Storage occurs internally when TRANSFER is taken to a 1 and the next negative edge of COUNT INPUT occurs. This allows asynchronous COUNT and TRANSFER operation since the transfer is terminated internally prior to incrementing the counters. This means that a COUNT negative edge must follow a TRANSFER command before a reset is applied to assure transfer of data. An external reset command must be delayed at least one COUNT negative edge following a transfer. External transfer should terminate at least 1 μS prior to this COUNT negative edge and RESET should occur no sooner than 1 μS following that edge.

Output Drive Characteristics



(I_{OL} @ V₀ = V_{SS} - 0.75V; T_A = 25°C and T_A = 75°C
 I_{OH} @ V₀ = V_{DD} + 0.75V; V_{DD} = 0V)

Figure 3

RESET, Pin 3

The decade counters are reset to 0000 when RESET is at logic 0. The RESET input at logic 0 also forces the scan counter to the MSD output and resets the OVERFLOW latch output to a logic 1. It maintains this condition as long as a logic 0 is present at RESET and overrides all other associated inputs. As indicated previously, the decade counter should not be reset until a transfer has been terminated.

Since the RESET input resets the scan counter to the MSD, the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{SCAN} should be much greater than four times F_{RESET}.

Ideally, the reset pulse should also be made narrow to prevent its duration from causing the MSD to be on much longer than the other digits and thus appear to be brighter.

COUNT, Pin 4

The decade counters are synchronously incremented on the negative edge of the COUNT input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}. (See Table 1.)

COUNT EXTEND, Pin 5

COUNT EXTEND is a feature provided to enable MIC5002s to be cascaded. Whenever the counter state attains 9999 count, the COUNT EXTEND output goes high. This output remains logical 1 only until the next negative transition of COUNT occurs or a RESET signal is applied.

Typical Count Oscillator Frequencies vs. Capacitance Between V_{SS} and COUNT

Capacitance	Typical Frequency
470 pF	135 kHz
1000 pF	90 kHz
4700 pF	33 kHz
20000 pF	9.5 kHz

(V_{SS} = 5.75V; V_{DD} = 0V; V_{GG} = -12V; T_A = 25°C)

Table 1

Typical Scan Oscillator Frequencies vs. Capacitance Between V_{SS} and SCAN Input

Capacitance	Typical Frequency
470 pF	17 kHz
1000 pF	11.2 kHz
4700 pF	4.0 kHz
20000 pF	1.33 kHz

(V_{SS} = 5.75V; V_{DD} = 0V; V_{GG} = -12V; T_A = 25°C)

Table 2

OVERFLOW, Pin 6 (N/A on MIC5007)

OVERFLOW occurs on the 10,000th count input following a reset. It is normally high and, when activated, goes low to indicate that the decade counters have gone from 9999 to 0000 without encountering a reset. Once activated, the OVERFLOW latch will remain low until RESET is pulled low.

DECIMAL POINT IN, Pin 7 (N/A on MIC5007)

With DECIMAL POINT IN held high, the device employs leading zero blanking. This causes any leading zeros in the display latches to be blanked when their DIGIT SELECT goes high. At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or DECIMAL POINT IN is clocked to a 0. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

Leading zero blanking may be inhibited by wiring DECIMAL POINT IN to ground. The MIC5007 does not have a pin for DECIMAL POINT IN and therefore does not have leading zero blanking.

In the DECIMAL POINT RIGHT mode, even though the DECIMAL POINT IN is clocked, unblanking is delayed until the following digit is enabled.

DECIMAL POINT LEFT OR RIGHT, Pin 8 (N/A on MIC5007)

Bringing this control to logic 1 allows the use of displays with the decimal point physically located on the left side of the numeral. Logic 0 on this input allows for a right-handed decimal point.

BLANKING, Pin 9

The BLANKING input at logic 0 forces the 7-segment outputs to the off-state and BCD to the equivalent of the number zero. This condition is maintained on a dc basis as long as the BLANKING input is zero. The DIGIT SELECT outputs continue to operate at the scan rate as described.

SCAN INPUT, Pin 10

The DIGIT SELECT COUNTER is incremented by a negative edge on the SCAN INPUT. During the time the SCAN INPUT is at 0, the SEGMENT and DIGIT SELECT outputs are forced off and the complement BCD outputs are forced to logic 1. The off level of the 7-segment and BCD outputs is determined by the state of the TRUE/COMPLEMENT input. This remains until the SCAN INPUT returns to logic 1.

The DIGIT SELECT COUNTER is a one-of-four counter, scanning from MSD to LSD, enabling one quad latch output at a time, and presenting a logic 1 to the corresponding DIGIT SELECT output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the VSS or VDD supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to VSS. (See Table 2.)

TRUE/COMPLEMENT, Pin 11 (N/A on MIC5007)

When this control is driven to 0, inversion of both the BCD and 7-segment outputs occurs. Depending upon the display used, combinations of the BLANKING input and TRUE/COMPLEMENT control can be chosen to give a lamp test.

BCD OUT, Pins 12 through 15 (N/A on MIC5005)

The BCD outputs are push-pull and are designed to drive directly to the base of common emitter transistors. Output characteristics are shown in Figure 3.

VDD, Pin 16

VDD is the negative supply and is nominally ground.

SEGMENT OUTPUTS, Pins 17 through 23 (N/A on MIC5007)

The SEGMENT OUTPUT buffers are identical to the BCD output buffers.

DIGIT SELECT OUTPUTS, Pins 24 through 27

The DIGIT SELECT OUTPUTS are push-pull and go high during their appropriate times to accomplish the multiplexing of the digits.

VSS, Pin 28

VSS is the positive supply voltage and is nominally maintained at 5Vdc with respect to VDD.

Absolute Maximum Ratings* (See Notes 1 and 2)

Absolute Maximum V_{SS}	7.5V
V_{GG} Supply Range	$0V \geq V_{GG} \geq -13.2V$
Operating Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Operating Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{SS}	Supply Voltage	$V_{SS} - V_{DD}$	4.5	5.0	7.5	V	1,2
V_{GG}	Supply Voltage	$V_{GG} - V_{DD}$	-13.2	-12	V_{DD}	V	1,2
F_C	Count Frequency		dc		250	kHz	

DC Characteristics

($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0V$; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	$V_{DD}+0.8$	V	
V_{IH}	Input Voltage, Logic 1 (High)	$V_{SS} - 1$	V_{SS}	$V_{SS}+0.3$	V	3
I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	$V_{GG} = -12V$
C_{IN}	Input Capacitance		3	10	pF	$T_A = 25^{\circ}C$, $f = 1MHz$, $V_{IN} = V_{SS}$
I_{IL}	Input Current, Logic 0, Count Input Scan Input Decimal Point Input Other Logic Inputs			1.6 1.6 1.0 1.0	mA mA μA mA	5 5
I_{OL}	Output Current, Logic 0	0.5			mA	6, $V_{GG} = -12V$
I_{OH}	Output Current, Logic 1	0.5			mA	6, $V_{GG} = -12V$
V_{OL}	Output Voltage, Logic 0			$V_{DD}+0.2$	V	4
V_{OH}	Output Voltage, Logic 1	$V_{DD}-0.2$			V	4

NOTES:

- $V_{DD} = 0V$.
- $V_{SS} - V_{GG}$ no more than 20.7V.
- Internal pull-up resistors (approx. 10k) are provided at all inputs other than Count Input, Scan Input and Decimal Point Input.
- $V_{GG} = -12V \pm 10\%$. Outputs open.
- Measurement made at $V_I = V_{DD} + 0.4V$. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at $V_I = +0.4V$ is 1.6mA. 400 μA source current is sufficient to represent a logic 1 and hold off or override the internal oscillators.
- I_{OL} measured at $V_O = V_{SS} - 0.75V$. (Direct driving base pnp emitter to V_{SS} .) I_{OH} measured at $V_O = V_{DD} + 0.75V$. (Direct driving base npn emitter to V_{DD} .)

AC Characteristics(V_{SS} = +5V ±%; V_{GG} = V_{DD} = 0V; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

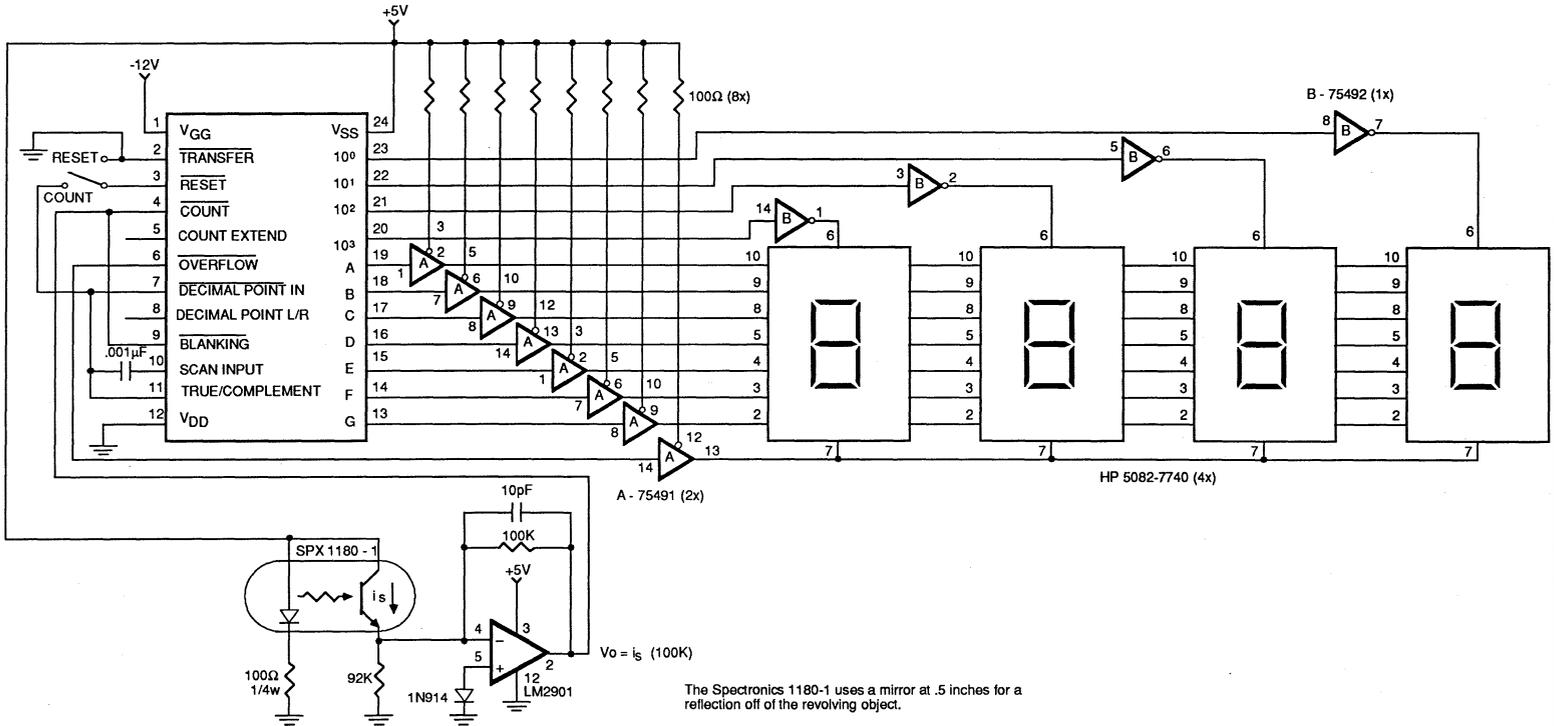
Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
f _{CI}	Count Input Frequency	dc		250	kHz	
f _{SI}	Scan Input Frequency	dc		50	kHz	
t _{RD}	Reset to Any Output Delay			15	μS	
t _{PW}	Logic 0 Pulse Width, <u>Reset Input</u> <u>Count Input</u> <u>Scan Input</u> <u>Transfer Input</u>	1.0			μS	
		1.0			μS	
		10.0			μS	
		2.5			μS	
t _{PH}	Logic 1 Time <u>Count Input</u> <u>Scan Input</u>	3.0			μS	
		10.0			μS	
t _{SD}	Scan to Output Disable Time <u>Digit Select Outputs</u> <u>All Data Outputs</u>			15	μS	7
				15	μS	7
t _{SE}	Scan to Output Enable Time <u>Digit Select Outputs</u> <u>All Data Outputs</u>			15	μS	8
				15	μS	8
t _{CE}	Count Input to Count Extend Delay to 1 or 0			15	μS	9
t _{OF}	Count Input to Overflow Delay (On)			15	μS	9
t _{ROF}	Reset Input to Overflow Delay (Off)			5	μS	

NOTES:

- V_{DD} = 0V.
- V_{SS} - V_{GG} no more than 20.7V.
- Internal pull-up resistors (approx. 10k) are provided at all inputs other than Count Input, Scan Input and Decimal Point Input.
- V_{GG} = -12V ± 10%. Outputs open.
- Measurement made at V_I = V_{DD} + 0.4V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6mA. 400μA source current is sufficient to represent a logic 1 and hold off or override the internal oscillators.
- I_{OL} measured at V_O = V_{SS} - 0.75V. (Direct driving base pnp emitter to V_{SS}.) I_{OH} measured at V_O = V_{DD} + 0.75V. (Direct driving base npn emitter to V_{DD}.)
- Delay measured from the negative edge of the SCAN input.
- Delay measured from the rising edge of the SCAN input.
- Delay measured from the negative edge of the COUNT input.

Typical Application: Revolution Counter

4-14



The Spectronics 1180-1 uses a mirror at .5 inches for a reflection off of the revolving object.

Figure 5



MIC50395CN/50396CN/50397CN

Six Decade Counter / Display Decoder

General Description

The MIC50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MIC50396 and MIC50397 operate identically to the MIC50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MIC50396 is well suited for industrial timer applications while the MIC50397 is best suited for stop watch or real time computer clock applications.

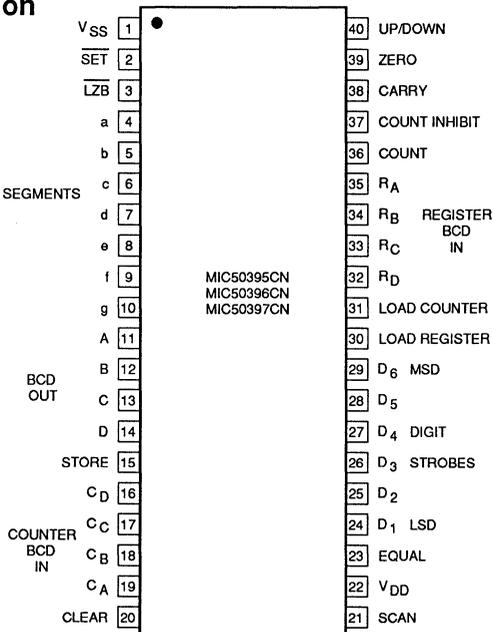
Features

- Single power supply
- Schmitt-Trigger on the count-input
- Drives common anode or cathode displays (CA with buffer)
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Loadable compare-register with comparator output
- Multiplexed BCD and seven-segment outputs
- Internal scan oscillator
- Direct LED segment drive
- Interfaces directly with CMOS logic
- Leading zero blanking
- MIC50396 programmed to count time:
 - 99 hrs. 59 min. 59 sec.
- MIC50397 programmed to count time:
 - 59 hrs. 59 min. 99/100 sec.

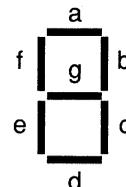
Ordering Information

Part Number	Temp. Range	Package
MIC50395CN	0–70°C	40-pin Plastic DIP
MIC50396CN	0–70°C	40-pin Plastic DIP
MIC50397CN	0–70°C	40-pin Plastic DIP

Pin Connection



Segment Identification



Operations:

Six Decade Counter, Latch

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed 0.75 μ S prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 μ S prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

Inputs, Outputs

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS} . The Carry, Equal, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS} . All inputs except Counter BCD, Register BCD, and SCAN inputs are high impedance CMOS compatible.

Three basic outputs originate from the counter: zero output, equal output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period

following a negative transition of Load Counter or Load Register.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the equal output, zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

Six Decade Compare Register

The register is loaded identically to the load counter paragraph described previously. The register may be loaded independently of the counter, however, the clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven segment outputs.

BCD Seven Segment Outputs

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the SET input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when \overline{SET} is low. Applying V_{SS} to SET allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the LZB input high. Typically the interdigit blanking time is 5 to 25 μ S when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs.

Scan Oscillator

The MIC50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode.

An external oscillator may also be used to drive the scan input. In either case, external capacitors of 150pF each will be required from V_{SS} to Counter BCD inputs and register BCD inputs. This will allow asynchronous loading of the BCD inputs.

In the internal drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (5→25 μ S). Display brightness can be controlled by the duty cycle of the external scan oscillator.

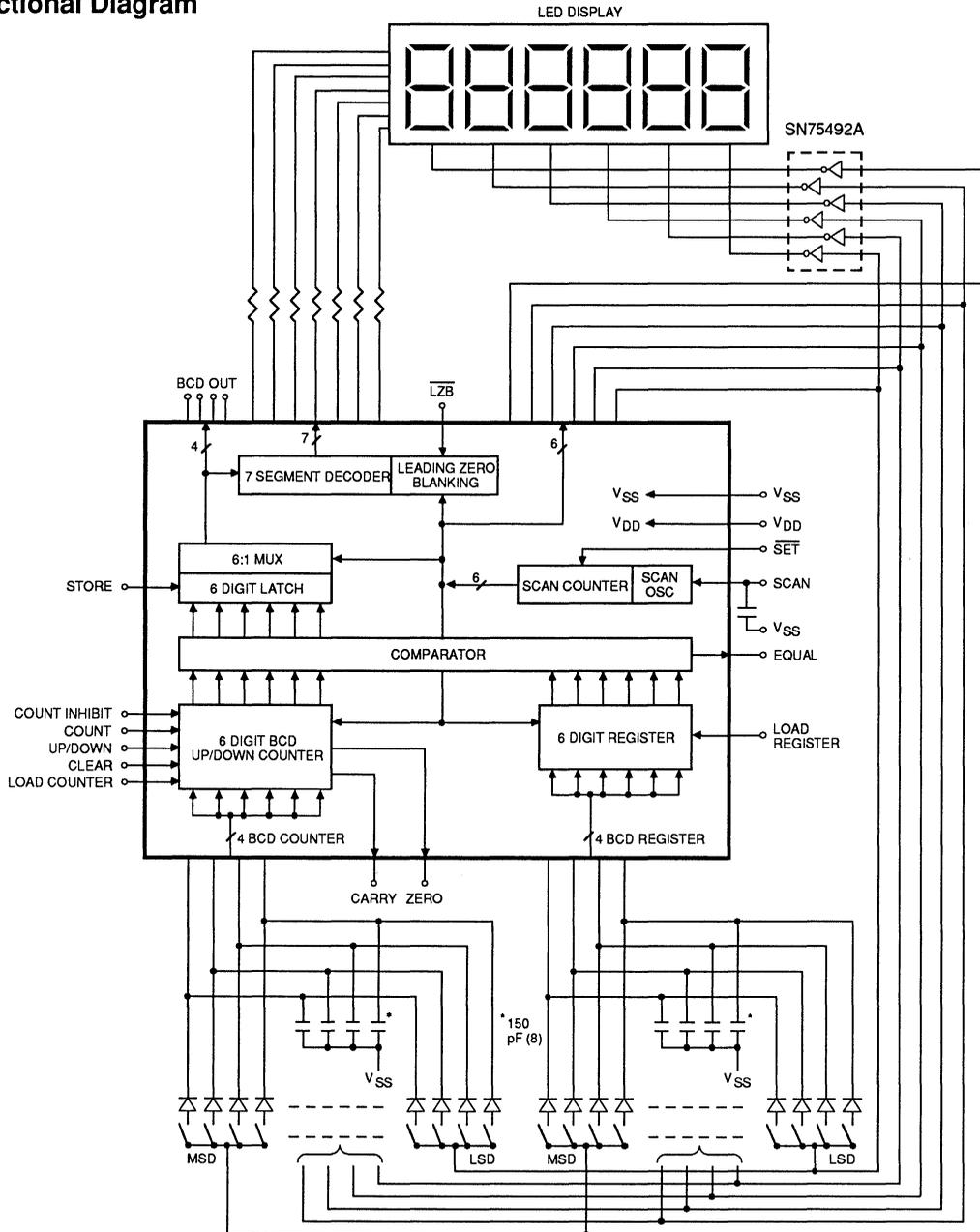
*Carry occurs at 99:59:59 for the 50396 and 59:59:99 for the 50397

If external capacitors on the BCD inputs are undesirable, it will be necessary to synchronize the negative going edge of the load register and/or load counter command to coincide with the positive going edge of the scan input signal. Also the V_{SS} range should be limited from 10.8 to 13.2 Volts.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to scan input.

C_{IN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

Functional Diagram



Absolute Maximum Ratings

Voltage on Any Terminal Relative to V_{SS} +0.3V to -20V
 Operating Temperature Range (Ambient) 0°C to +70°C
 Storage Temperature Range (Ambient) -40°C to +100°C

Maximum Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	0	70	C	
V_{SS}	Supply voltage ($V_{DD} = 0V$)	10	15	V	1
I_{SS}	Supply Current		35	mA	2
B_V	Break Down Voltage (Segment only @ 10 μA)		$V_{SS} - 26$	V	
P_D	Power Dissipation		670	mW	3

Electrical Characteristics

($V_{DD} = 0V$, $V_{SS} = +10.0V$ to $+15.0$, $0^\circ C \leq T_A \leq 70^\circ C$)

Static Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage, "0"	V_{DD}	$0.2 V_{SS}$	V	
V_{IH}	Input High Voltage, "1"	$V_{SS} - 1$	V_{SS}	V	4
V_{OL}	Output Voltage "0" @ 30 μA		$0.2 V_{SS}$	V	5
V_{OH}	Output Voltage "1" @ 1.5 mA	$0.8 V_{SS}$		V	5
I_{OH}	Output Current "1" Digit strobos Segment outputs	3.0 10.0		mA mA	6 7
I_{SCAN}	Scan Input Pullup Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15 V	2	40	μA	
I_{SET}	\overline{SET} Input Pullup Current @ 0V	5	60	μA	

Note 1: With 150 pF capacitor to V_{SS} from counter BCD and register BCD inputs.

Note 2: I_{SS} with inputs and outputs open at 0°C. 33 mA at 25°C and 28 mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. ($\theta_{JA} = 100$ C/Watt)

Note 3: All outputs loaded.

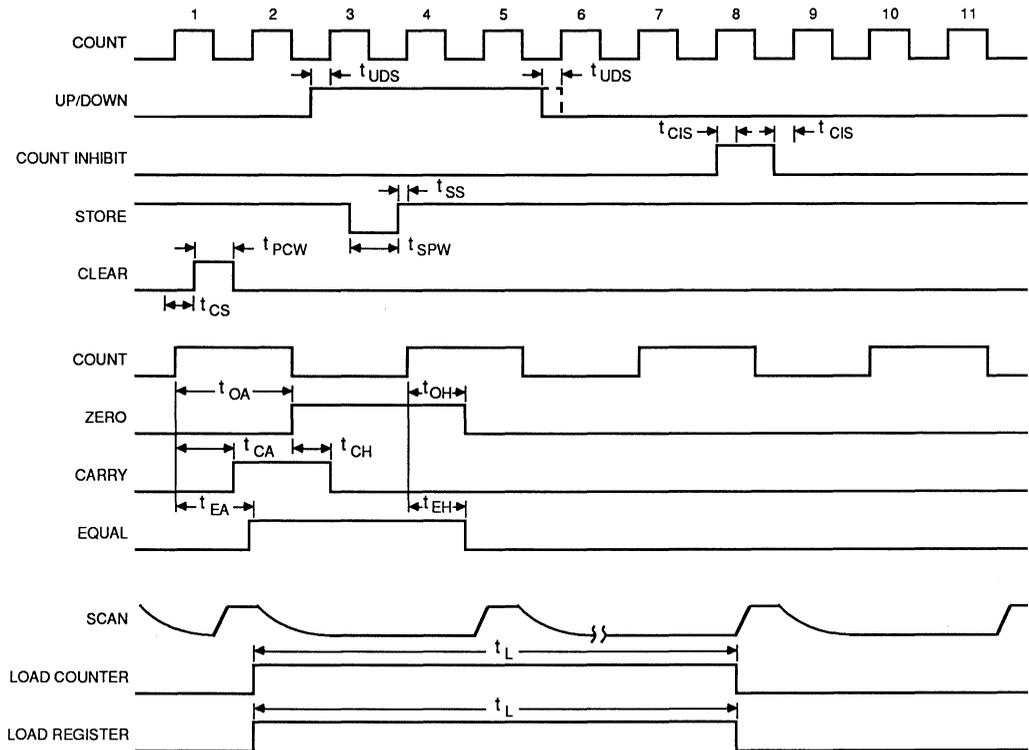
Note 4: MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is $V_{SS} - 2.5$ V. Those inputs have internal pulldown resistors to V_{DD} .

Note 5: This applied to the push pull CMOS compatible outputs. Does not include digit strobos or segment outputs.

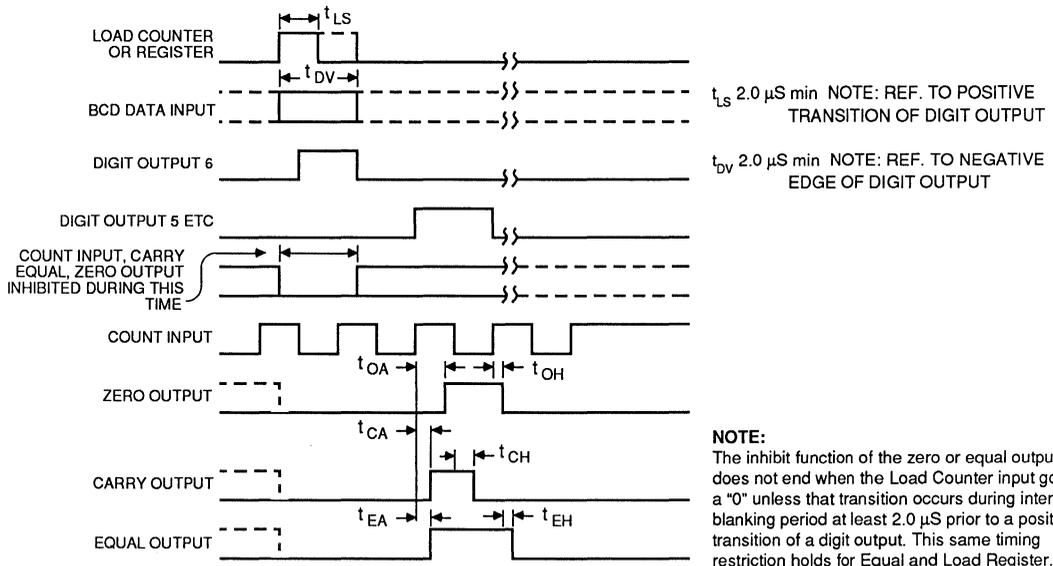
Note 6: For $V_{OUT} = V_{SS} - 2.0$ Volts. Average value over one digit cycle.

Note 7: For $V_{OUT} = V_{SS} - 3.0$ Volts. Average value over one digit cycle.

Timing



Loading Counter, Register (1 Digit)



Dynamic Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
f_{CI}	Count Input Frequency	0	1.00	MHz	8,9
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	400		nS	10
t_{SPW}	Store Pulse Width	2.0		μ S	
t_{SS}	Store Setup Time	0		μ S	11
t_{CIS}	Count Inhibit Setup Time	0		μ S	11
t_{UDS}	Up/Down Setup Time	-0.75		μ S	11
t_{CPW}	Clear Pulse Width	2.0		μ S	11
t_{CS}	Clear Setup Time	-0.5		μ S	11
t_{OA}	Zero Access Time		3.0	μ S	11
t_{OH}	Zero Hold Time		1.5	μ S	11
t_{CA}	Carry Access Time		1.5	μ S	11
t_{CH}	Carry Hold Time	0.9		μ S	12
t_{EA}	Equal Access Time	2.0		μ S	11
t_{EH}	Equal Hold Time	1.5		μ S	11
t_L	Load Time	$1/6 f_{SI}$			

Note 8: Measured at 50% duty cycle.

Note 9: If carry, equal, or zero outputs are used, the count frequency will be limited by their respective output times.

Note 10: The count pulse width must be greater than the carry access time when using the carry output.

Note 11: The positive edge of the count input is the $t = 0$ reference.

Note 12: Measured from negative edge of count input.



MIC50398CN/MIC50399CN

Six Decade Counter / Display Decoder

General Description

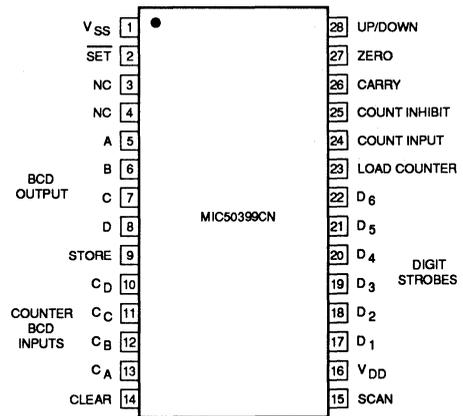
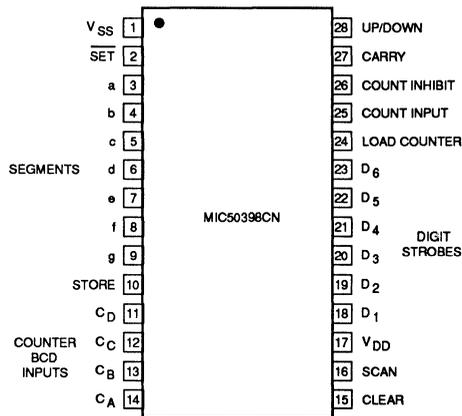
The MIC50398/9 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with storage latches. The counter can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD or 7-segment format to the output. These devices are intended to interface directly with the standard CMOS logic families.

Features

- Single power supply
- Schmitt-Trigger on the count-input
- Six decades of synchronous up/down counting
- Look-ahead carry or borrow
- Loadable counter
- Multiplexed seven-segment outputs MIC50398N
- Multiplexed BCD outputs, MIC50399N
- Internal scan oscillator

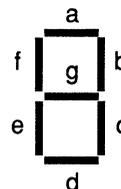
Pin Connection



Ordering Information

Part Number	Temp. Range	Package
MIC50398CN	0-70°C	28-pin Plastic DIP
MIC50399CN	0-70°C	28-pin Plastic DIP

Segment Identification



Operations:

Six Decade Counter, Latch

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input. Count inhibit must remain high while the count input is high to inhibit counting.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed 0.75 μ S prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 μ S prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

Inputs, Outputs

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS} . The Carry, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS} . All inputs except Counter BCD and SCAN inputs are high impedance CMOS compatible.

Two basic outputs originate from the counter: zero output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited. Zero output is on the MIC50399 only.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same count input. During a load counter operation the carry output is inhibited.

A count frequency of 1.5 MHz can be achieved if the zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

BCD & Seven Segment Outputs

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the \overline{SET} input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when \overline{SET} is low. Applying V_{SS} to \overline{SET} allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse brings up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Typically the interdigit blanking time is 3 to 10 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs. BCD outputs are on MIC50399 only.

Scan Oscillator

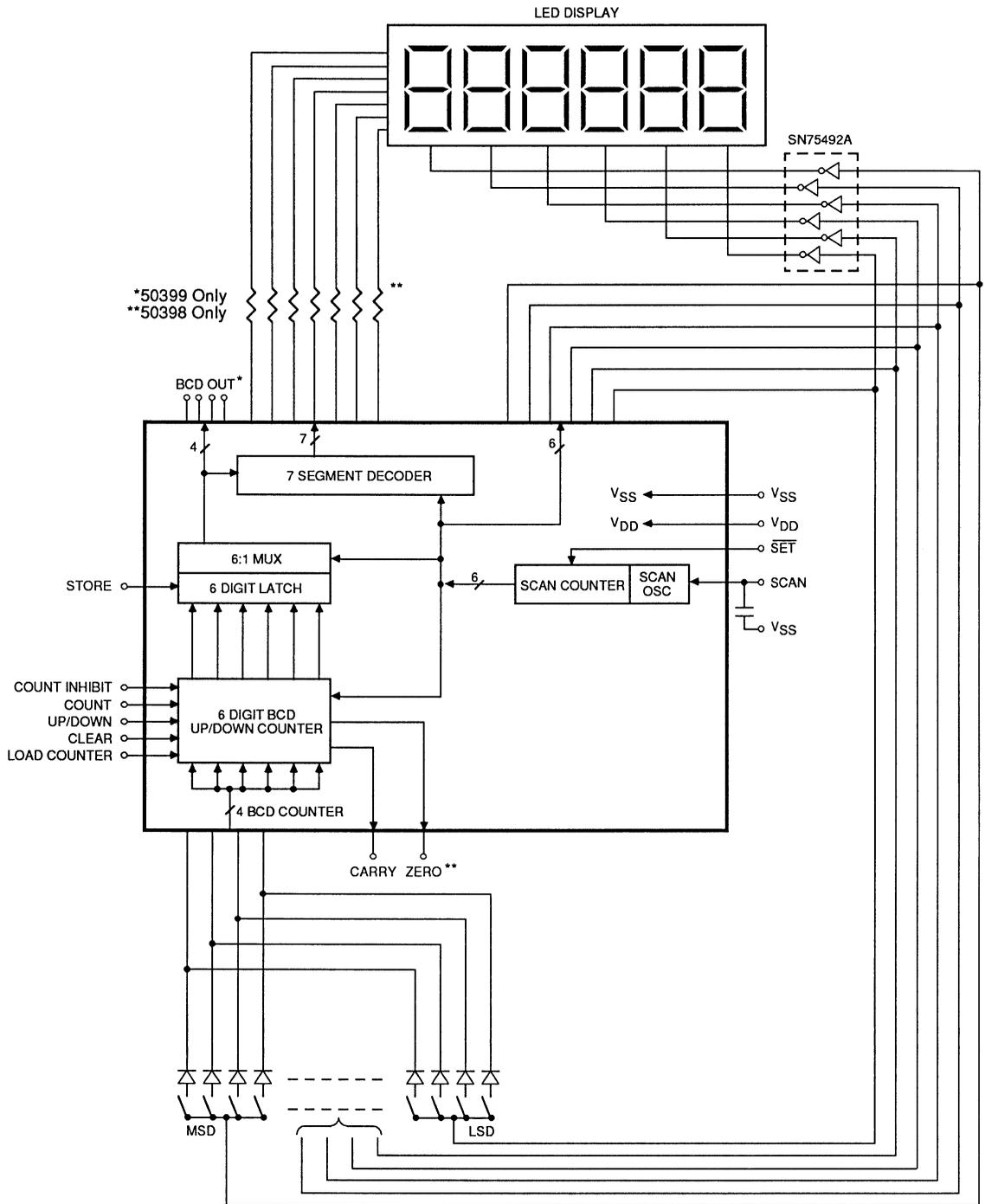
The counters have an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode. An external oscillator may also be used to drive the scan input.

In the external drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (3→10 μ S). Display brightness can be controlled by the duty cycle of the external scan oscillator.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor values from V_{SS} to scan input.

C_{IN}	Min	Max
820 pF	1.4 kHz	4.8 kHz
470 pF	2.0 kHz	6.8 kHz
120 pF	7.0 kHz	20 kHz

Functional Diagram



Absolute Maximum Ratings*

Voltage on Any Terminal Relative to V_{SS} +0.3V to -20V
 Operating Temperature Range (Ambient) 0°C to +70°C
 Storage Temperature Range (Ambient) -40°C to +100°C

*Operating above absolute maximum ratings may damage the device.

Maximum Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
T_A	Operating Temperature	0	70	°C	
V_{SS}	Supply voltage ($V_{DD} = 0V$)	10	15	V	
I_{SS}	Supply Current		40	mA	1
B_V	Break Down Voltage (Segment only @ 10 μA)		$V_{SS} - 26$	V	MIC50398 only
P_D	Power Dissipation		670	mW	2

Electrical Characteristics

($V_{DD} = 0V$, $V_{SS} = +10.0V$ to $+15.0$, $0^\circ C \leq T_A \leq 70^\circ C$)

Static Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage, "0"	V_{DD}	$0.2 V_{SS}$	V	
V_{IH}	Input High Voltage, "1"	$V_{SS} - 1$	V_{SS}	V	3
V_{OL}	Output Voltage "0" @ 30 μA		$0.2 V_{SS}$	V	4
V_{OH}	Output Voltage "1" @ 1.5 mA	$0.8 V_{SS}$		V	4
I_{OH}	Output Current "1" Digit strobos Segment outputs	3.0		mA	5
		10.0		mA	6
I_{SCAN}	Scan Input Pullup Current @ 0 V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15 V	2	40	μA	
I_{SET}	SET Input Pullup Current @ 0V	5	60	μA	

Note 1: I_{SS} with inputs and outputs open at 0°C. 33 mA at 25°C and 28 mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. ($\theta_{JA} = 100^\circ C/Watt$)

Note 2: All outputs loaded.

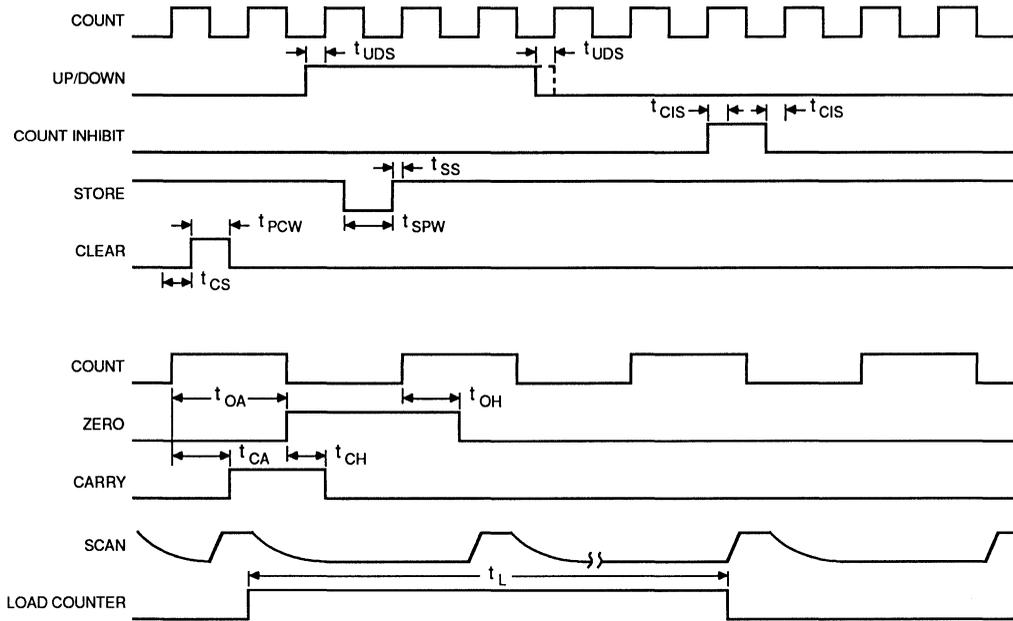
Note 3: MIN V_{IH} from C_A C_B C_C C_D inputs is $V_{SS} - 3.5$ V. Those inputs have internal pulldown resistors to V_{DD} .

Note 4: This applied to the push pull CMOS compatible outputs. Does not include digit strobos on segment outputs.

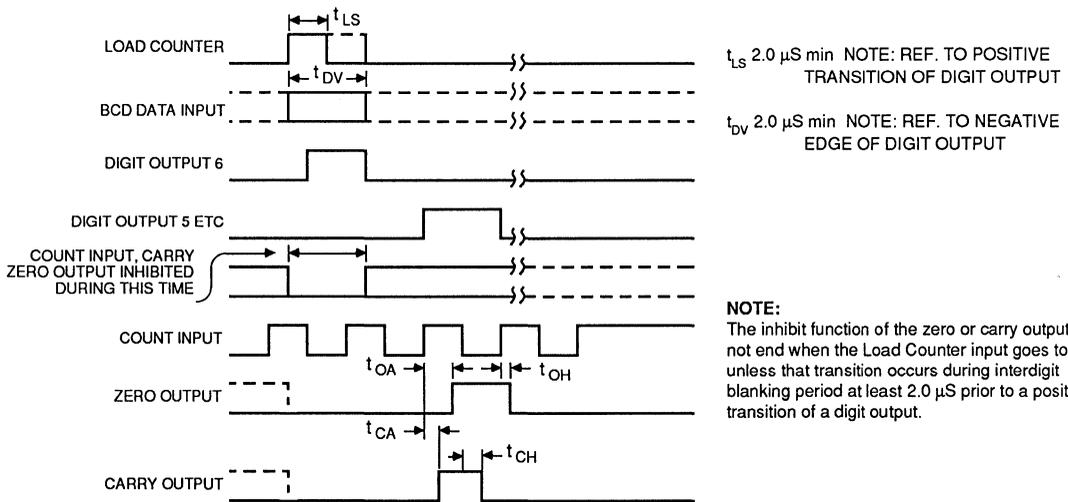
Note 5: For $V_{OUT} = V_{SS} - 2.0$ Volts. Average value over one digit cycle.

Note 6: For $V_{OUT} = V_{SS} - 3.0$ Volts. Average value over one digit cycle.

Timing



Loading Counter, Register (1 Digit)



Dynamic Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
f_{CI}	Count Input Frequency	0	1.5	MHz	7,8
f_{SI}	Scan Input Frequency	0	20	kHz	
t_{CPW}	Count Pulse Width	325		nS	9
t_{SPW}	Store Pulse Width	2.0		μ S	
t_{SS}	Store Setup Time	0		μ S	10
t_{CIS}	Count Inhibit Setup Time	0		μ S	10
t_{UDS}	Up/Down setup Time	-0.75		μ S	10
t_{CPW}	Clear Pulse Width	2.0		μ S	10
t_{CS}	Clear Setup Time	-0.5		μ S	10
t_{OA}	Zero Access Time		3.0	μ S	10 MIC50399 only
t_{OH}	Zero Hold Time		1.5	μ S	10 MIC50399 only
t_{CA}	Carry Access Time		1.5	μ S	10
t_{CH}	Carry Hold Time		0.9	μ S	11
t_L	Load Time		$1/6 f_{SI}$		12

Note 7: Measured at 50% duty cycle.

Note 8: If carry or zero outputs are used, the count frequency will be limited by their respective output times.

Note 9: The count pulse width must be greater than the carry access time when using the carry output.

Note 10: The positive edge of the count input is the $t = 0$ reference.

Note 11: Measured from negative edge of count input.

Note 12: Time to load one digit.



MIC7233

Triplex LCD Decoder/Driver

General Description

The MIC7233 Triplex Liquid Crystal Display Decoder/Driver accepts parallel input data which is ASCII encoded and TTL compatible. Data is decoded to drive alpha-numeric 18 segment - 4 digit Liquid Crystal Displays. Timing and voltage generation for triplex operation is performed by the MIC7233 through an internal oscillator and an internal voltage divider. Chip select input pins have internal 1 MΩ pull-down resistors.

Eight bit parallel input data is decoded into two address bits for digit select, and six ASCII encoded data bits which are decoded into 64 independent combinations for segment drive. MIC7233 drivers may be cascaded to drive displays with more than 4 digits.

The MIC7233 is manufactured using InCMOS process technology which is an all-implant high speed Silicon Gate CMOS process. It features shallow junction structures for superior speed/power characteristics and built in anti-latch protection.

Devices are available in die form, or in 40 lead plastic DIP packages. The MIC7233 is protected against Electrostatic Discharge.

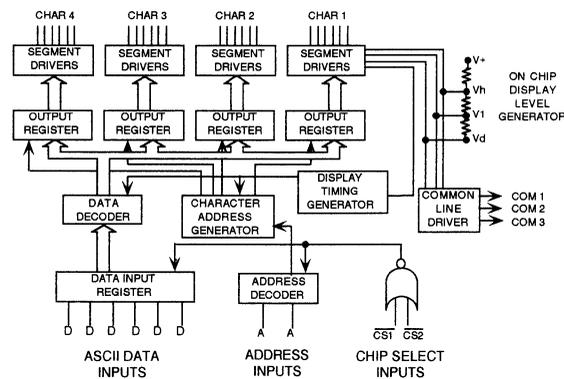
Features

- 4 Digit - 18 Segment Alpha-Numeric Drive
- 6 Bit ASCII Parallel Input Format
- Pin and Function Compatible with the ICM7233
- 50 nS Write Cycle Time
- Direct Interface to High Speed Microprocessors
- Data Retention
- On Chip Oscillator
- Triplex Operation
- Very Low Standby Power
- Simple Digital Interface
- TTL Compatible Inputs
- Electrostatic Discharge Protection
- Cascadable for Large Number of Digits

Applications

- Portable Instrumentation
- Portable Data Entry Devices
- Process Control Equipment
- Test Equipment
- Industrial Instrumentation
- Panel Meters
- Computer Peripherals
- Medical Equipment
- Machine Control Systems
- Communication Systems

Block Diagram

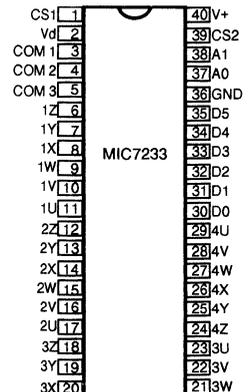


For further information on MIC7233, please contact the factory.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC7233CN	0°C to 70°C	40-pin Plastic DIP
MIC7233CX	0°C to 70°C	Die

Pin Description



General Description

The MIC8010 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8010 is available in die form; contact the factory concerning dice and custom packaging requirements

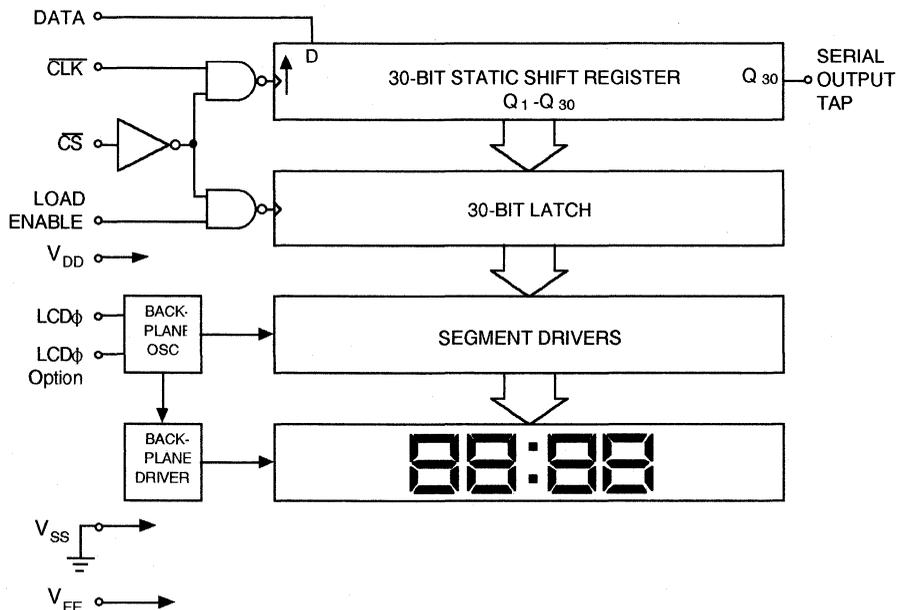
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC8010-01BN	- 40°C to + 85°C	40 pin Plastic DIP
MIC8010-02BN	- 40°C to + 85°C	40 pin Plastic DIP
MIC8010-01AL	- 55°C to +125°C	40 pin Ceramic LCC
MIC8010-02AL	- 55°C to +125°C	40 pin Ceramic LCC

Features

- Pin-for-pin compatible with Holt HI8010
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Drives 30 segments
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

Block Diagram



Note: The MIC8010 is ESD sensitive.

Absolute Maximum Ratings (Note 1, Note 2)

Supply Voltage:		Operating Temperature Range:	
V_{DD}	-0.3V to +18V	MIC8010-01BN, -02BN	-40°C to +85°C
V_{EE}	$V_{DD}-35V$ to +0.3V	MIC8010-01AL, -02AL	-55°C to +125°C
Input Voltage (except LCD ϕ)	-0.3V to $V_{DD}+0.3V$	Storage Temperature Range	-65°C to +150°C
LCD ϕ Input Voltage	$V_{DD}-35V$ to $V_{DD}+0.3V$	Power Dissipation	250 mW
DC Current Drain per input pin	10 mA		

DC Electrical Characteristics (Notes 3 and 4)

$V_{DD}=5V$, $V_{EE}=-25V$, $V_{SS}=0V$, $T_A=25^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	μA
	I_{EE}	no load, $f_{BP}=100Hz$			150	
Input Low Voltage (excluding LCD ϕ)	V_{IL}		0		1.3	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$			$0.2V_{DD}$	V
Input High Voltage (excluding LCD ϕ)	V_{IH}		2		V_{DD}	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$	$0.5V_{DD}$			V
Input Low Voltage (LCD ϕ)	V_{ILX}		V_{EE}		2	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$			$0.1V_{DD}$	V
Input High Voltage (LCD ϕ)	V_{IHx}		2.5		V_{DD}	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$	$0.9V_{DD}$			V
Input Current	I_{IN}	$V_{DD}=0$ to 5V			1	μA
Input Capacitance	C_I				5	pF
Segment Output Impedance	R_{SEG}	$I_L=10\mu A$			10	k Ω
Backplane Output Impedance	R_{BP}	$I_L=10\mu A$			450	Ω
Data Out Current	I_{DOH}	Source Current, $V_{OH}=4.5V$			0.6	mA
	I_{DOL}	Sink Current, $V_{OL}=0.5V$	-0.6			

AC Electrical Characteristics (Note 3)

$V_{EE}=-25V$, $V_{SS}=0V$, $T_A=25^\circ C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Period	t_{CL}	$V_{DD}=5V$	1000			nS
		$V_{DD}=10V$	500			
Clock Pulse Width	t_{CW}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			
Data-In Setup	t_{DS}	$V_{DD}=5V$	300			nS
		$V_{DD}=10V$	150			
Data-In Hold	t_{DH}	$V_{DD}=5V$	10			nS
		$V_{DD}=10V$	10			
Chip Select Setup to Clock	t_{CSS}	$V_{DD}=5V$	200			nS
		$V_{DD}=10V$	100			

AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Chip Select Hold to Clock	t_{CSH}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			
Load Setup to Clock	t_{LS}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	280			
Chip Select Setup to Load	t_{CSL}		0			nS
Load Pulse Width	t_{LW}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	300			
Chip Select Hold to Load	t_{LCS}		0			nS
Data Out Valid from Clock	t_{CDO}	$V_{DD}=5V$			600	nS
		$V_{DD}=10V$			300	

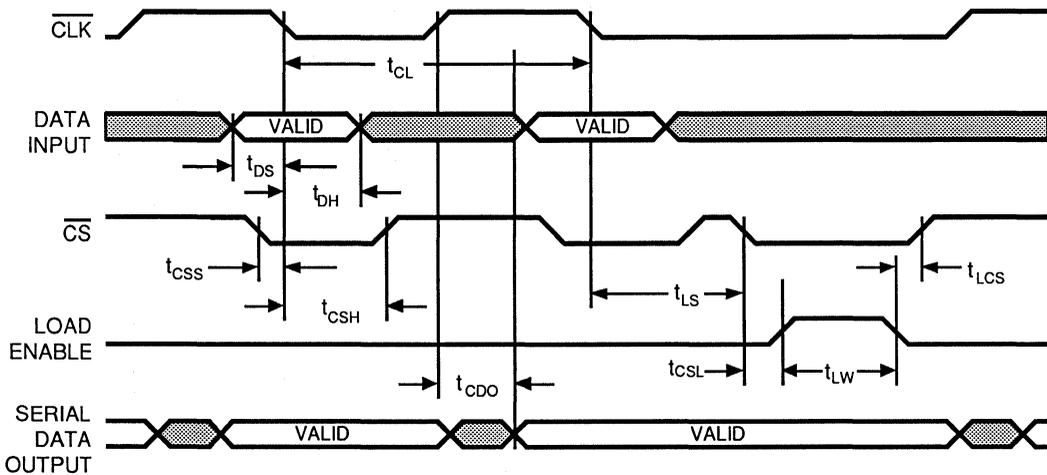
Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are referred to $V_{SS}=0V$.

Note 3: **Minimum** and **Maximum** values are guaranteed and 100% tested. **Typical** values represent the most likely parametric norm.

Note 4: $V_{DD} - 32V < V_{EE} < V_{DD} - 5V$ is required for proper device operation.

Timing Diagram



Applications Information

The MIC8010 utilizes a serial data interface as a means of programming the LCD segment outputs. The interface protocol is compatible with software written for the Holt HI-8010.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). $DATA\ INPUT$ is shifted in on the falling edges of $CLOCK$, and the contents of the shift register exit at $SERIAL\ DATA\ OUTPUT$ on the rising edges of $CLOCK$. A high level (V_{DD}) at $LOAD$ enables the transfer of data from the shift register to the latch. The latch is transparent while $LOAD$ is held high.

If data is shifted into the internal register but not immediately loaded into the latch, $CLOCK$ should remain low. The driver may then be deselected without disturbing the contents of the shift register. If $CLOCK$ is held high while $CHIP\ SELECT$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting $SERIAL\ DATA\ OUTPUT$ from one chip to $DATA\ INPUT$ of the next. $LOAD$, $CLOCK$, and $CHIP\ SELECT$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8010 can operate from a single supply of $V_{DD}=4$ to 18V, with V_{EE} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{EE} for segment/backplane voltage. V_{EE} is then negative with respect to V_{SS} , and the potential across V_{DD} and V_{EE} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{EE} to V_{DD} . For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator ($LCD\phi$ and $LCD\phi$ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC}+256$. With $R_{OSC}=150\ k\Omega$ and $C_{OSC}=470\ pF$, $f_{OSC}=25.6\ kHz$ and $f_{BP}=100\ Hz$.

Devices with a "-02" suffix bring out only $LCD\phi$, leaving $LCD\phi$ Option disconnected. In this case $LCD\phi$ is driven with an external clock; in a typically application several MIC8010-02 drivers would be slaved to a master MIC8010-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. The feature is used in driving displays other than LCD displays, such as VF or LED. $LCD\phi$ is connected to V_{DD} for this mode.

Typical Applications (Continued)

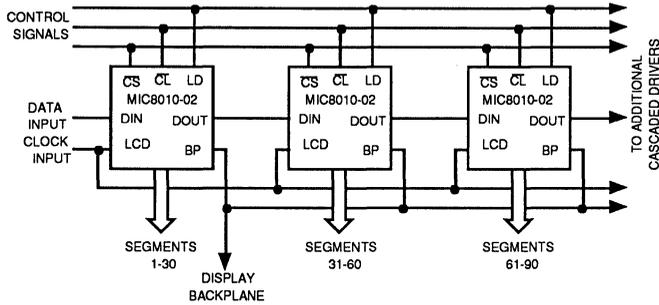


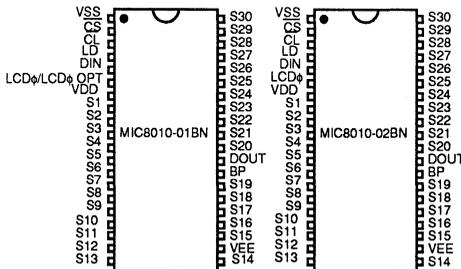
Figure 3. Cascading with External Clocking Source - 02 Configuration

Pin Assignments

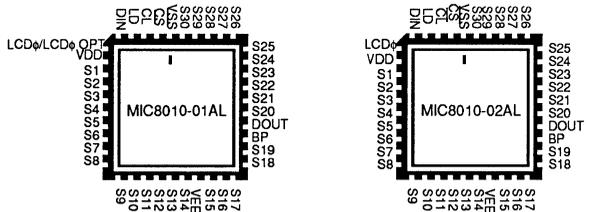
Function	Device Suffix	
	-01	-02
V _{SS} (Ground)	1	1
Chip Select	2	2
Clock	3	3
Load	4	4
Data Input	5	5
LCD ϕ	6	6
LCD ϕ Option	6	NC
V _{DD}	7	7
Segment 1	8	8
Segment 2	9	9
Segment 3	10	10
Segment 4	11	11
Segment 5	12	12
Segment 6	13	13
Segment 7	14	14
Segment 8	15	15
Segment 9	16	16
Segment 10	17	17
Segment 11	18	18
Segment 12	19	19
Segment 13	20	20

Function	Device Suffix	
	-01	-02
Segment 14	21	21
V _{EE}	22	22
Segment 15	23	23
Segment 16	24	24
Segment 17	25	25
Segment 18	26	26
Segment 19	27	27
Backplane	28	28
Data Output	29	29
Segment 20	30	30
Segment 21	31	31
Segment 22	32	32
Segment 23	33	33
Segment 24	34	34
Segment 25	35	35
Segment 26	36	36
Segment 27	37	37
Segment 28	38	38
Segment 29	39	39
Segment 30	40	40

Connection Diagrams



40 Pin Plastic DIP



40 Pin Ceramic Chip Carrier



MIC8011

Liquid Crystal Display Driver

General Description

The MIC8011 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8011 is available in die form; contact factory concerning dice and custom packaging requirements.

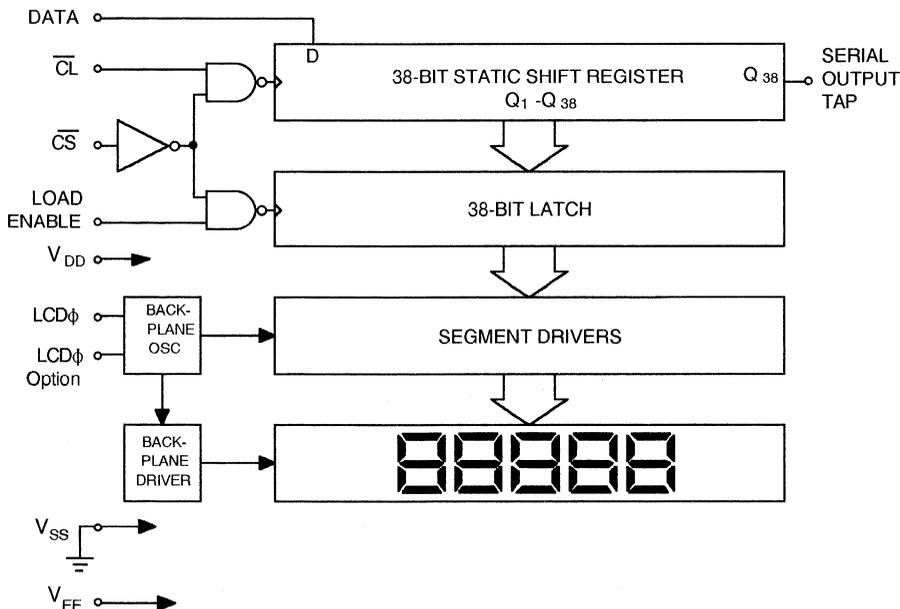
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC8011-01BN	-40°C to +85°C	48 pin Plastic DIP
MIC8011-02BN	-40°C to +85°C	48 pin Plastic DIP
MIC8011-03BQ	-40°C to +85°C	52 pin QFP

Features

- Cascadable serial interface
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability.
- Drives 38 segments
- Compatible with dichroic, midchroic, or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details.
- 60 V extended output swing available (contact factory for details)

Block Diagram



Note: The MIC8011 is ESD sensitive.

Absolute Maximum Ratings (Note 1, Note 2)

Supply Voltage:		Operating Temperature Range:	
V_{DD}	-0.3V to +18V	MIC8011-01BN, -02BN	-40°C to +85°C
V_{EE}	$V_{DD}-35V$ to +0.3V	MIC8011-03BV	-40°C to +85°C
Input Voltage (except LCD ϕ)	-0.3V to $V_{DD}+0.3V$	Storage Temperature Range	-65°C to +150°C
LCD ϕ Input Voltage	$V_{DD}-35V$ to $V_{DD}+0.3V$	Power Dissipation	250 mW
DC Current Drain per input pin	10 mA		

DC Electrical Characteristics (Notes 3 and 4)

$V_{DD} = 5V$, $V_{EE} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	μA
	I_{EE}	no load, $f_{BP}=100Hz$			150	
Input Low Voltage (excluding LCD ϕ)	V_{IL}		0		1.3	V
		-55°C to +125°C, $V_{DD} = 4V-16V$			$0.2V_{DD}$	V
Input High Voltage (excluding LCD ϕ)	V_{IH}		2		V_{DD}	V
		-55°C to +125°C, $V_{DD} = 4V-16V$	$0.5V_{DD}$			V
Input Low Voltage (LCD ϕ)	V_{ILX}		V_{EE}		2	V
		-55°C to +125°C, $V_{DD} = 4V-16V$			$0.1V_{DD}$	V
Input High Voltage (LCD ϕ)	V_{IHx}		2.5		V_{DD}	V
		-55°C to +125°C, $V_{DD} = 4V-16V$	$0.9V_{DD}$			V
Input Current	I_{IN}	$V_{DD}=0$ to 5V			1	μA
Input Capacitance	C_I				5	pF
Segment Output Impedance	R_{SEG}	$I_L=10\mu A$			10	k Ω
Backplane Output Impedance	R_{BP}	$I_L=10\mu A$			450	Ω
Data Out Current	I_{DOH}	Source Current, $V_{OH}=4.5V$			0.6	mA
	I_{DOL}	Sink Current, $V_{OL}=0.5V$	-0.6			

AC Electrical Characteristics (Note 3)

$V_{EE} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Period	t_{CL}	$V_{DD}=5V$	1000			nS
		$V_{DD}=10V$	500			
Clock Pulse Width	t_{CW}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			
Data-In Setup	t_{DS}	$V_{DD}=5V$	300			nS
		$V_{DD}=10V$	150			
Data-In Hold	t_{DH}	$V_{DD}=5V$	10			nS
		$V_{DD}=10V$	10			
Chip Select Setup to Clock	t_{CSS}	$V_{DD}=5V$	200			nS
		$V_{DD}=10V$	100			
Chip Select Hold to Clock	t_{CSH}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			

AC Electrical Characteristics (Continued)

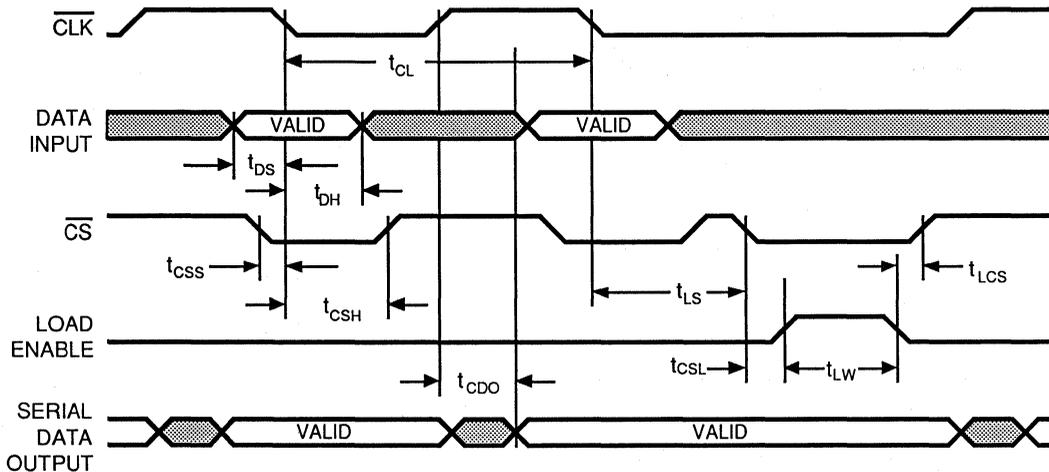
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Load Setup to Clock	t_{LS}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	280			
Chip Select Setup to Load	t_{CSL}		0			nS
Load Pulse Width	t_{LW}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	300			
Chip Select Hold to Load	t_{LCS}		0			nS
Data Out Valid from Clock	t_{CDO}	$V_{DD}=5V$			600	nS
		$V_{DD}=10V$			300	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are referred to $V_{SS}=0V$.

Note 3: Minimum and Maximum values are guaranteed and 100% tested. **Typical** values represent the most likely parametric norm.

Note 4: $V_{DD} - 32V < V_{EE} < V_{DD} - 5V$ is required for proper device operation.

Timing Diagram

Applications Information

The MIC8011 utilizes a serial data interface as a means of programming the LCD segment outputs. The interface protocol is compatible with software written for the Holt HI-8010.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). $\overline{DATA\ INPUT}$ is shifted in on the falling edges of \overline{CLOCK} , and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of \overline{CLOCK} . A high level (V_{DD}) at \overline{LOAD} enables the transfer of data from the shift register to the latch. The latch is transparent while \overline{LOAD} is held high.

If data is shifted into the internal register but not immediately loaded into the latch, \overline{CLOCK} should remain low. The driver may then be deselected without disturbing the contents of the shift register. If \overline{CLOCK} is held high while $\overline{CHIP\ SELECT}$ is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting $\overline{SERIAL\ DATA\ OUTPUT}$ from one chip to $\overline{DATA\ INPUT}$ of the next. \overline{LOAD} , \overline{CLOCK} , and $\overline{CHIP\ SELECT}$ are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line

Power Supplies

The MIC8011 can operate from a single supply of $V_{DD}=4$ to 18V, with V_{EE} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{EE} for segment/backplane voltage. V_{EE} is then negative with respect to V_{SS} , and the potential across V_{DD} and V_{EE} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{EE} to V_{DD} . For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

The on-chip oscillator (Figure 1) is available in three configurations. Devices with the "-01" suffix feature a 1-pin oscillator ($\overline{LCD\phi}$ and $\overline{LCD\phi\ Option}$ tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC}+256$. With $R_{OSC}=150\text{ k}\Omega$ and $C_{OSC}=470\text{ pF}$, $f_{OSC}=25.6\text{ kHz}$ and $f_{BP}=100\text{ Hz}$.

Devices with a "-02" suffix bring out only $\overline{LCD\phi}$, leaving $\overline{LCD\phi\ Option}$ disconnected. In this case $\overline{LCD\phi}$ is driven with an external clock; in a typically application several MIC8011-02 drivers would be slaved to a master MIC8011-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

Devices with the "-03" suffix have both the $\overline{LCD\phi}$ and $\overline{LCD\phi\ Option}$ available externally, allowing operation in either of the previous two configurations.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. This feature is used in driving displays other than LCD, such as VF or LED. $\overline{LCD\phi}$ is connected to V_{DD} for this mode.

Typical Applications

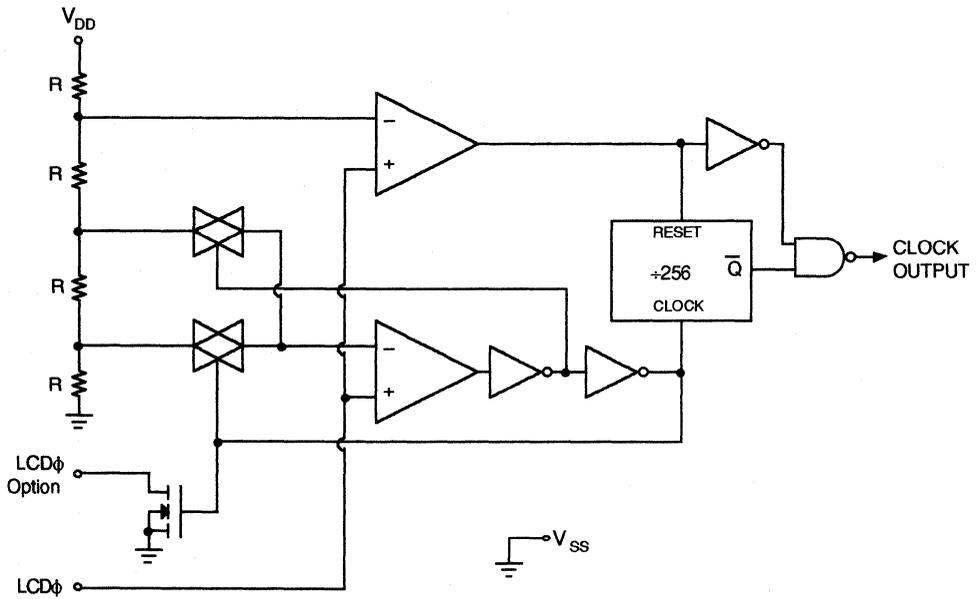


Figure 1. Internal Oscillator Circuit

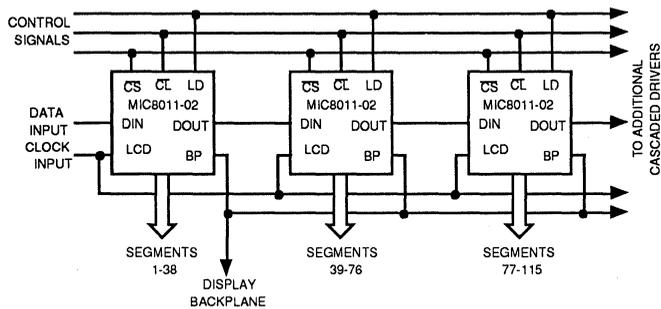


Figure 2. Cascading with External Clocking Source - Option -02

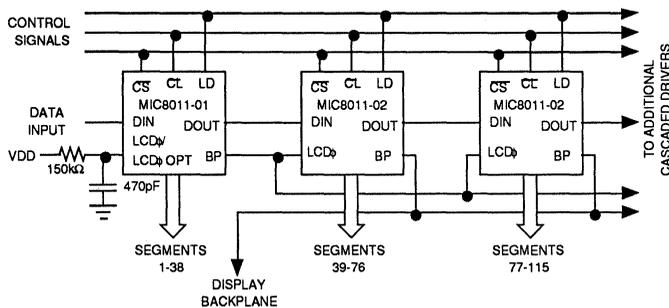


Figure 3. Cascading with Internal Clock Oscillator- Option -01

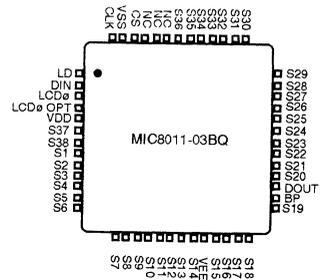
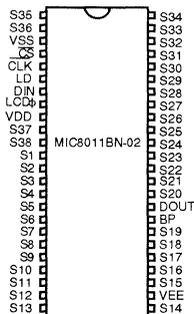
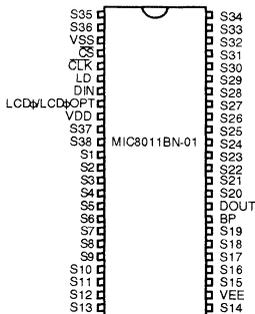
Pin Assignments

Function	Device Suffix		
	-01	-02	-03
VSS	3	3	50
Chip Select	4	4	51
Clock	5	5	52
Load	6	6	1
Data Input	7	7	2
LCD \emptyset	8	8	3
LCD \emptyset Option	8	NC	4
VDD	9	9	5
Segment 37	10	10	6
Segment 38	11	11	7
Segment 1	12	12	8
Segment 2	13	13	9
Segment 3	14	14	10
Segment 4	15	15	11
Segment 5	16	16	12
Segment 6	17	17	13
Segment 7	18	18	14
Segment 8	19	19	15
Segment 9	20	20	16
Segment 10	21	21	17
Segment 11	22	22	18
Segment 12	23	23	19
Segment 13	24	24	20
Segment 14	25	25	21
VEE	26	26	22

Function	Device Suffix		
	-01	-02	-03
Segment 15	27	27	23
Segment 16	28	28	24
Segment 17	29	29	25
Segment 18	30	30	26
Segment 19	31	31	27
Back Plane	32	32	28
Data Output	33	33	29
Segment 20	34	34	30
Segment 21	35	35	31
Segment 22	36	36	32
Segment 23	37	37	33
Segment 24	38	38	34
Segment 25	39	39	35
Segment 26	40	40	36
Segment 27	41	41	37
Segment 28	42	42	38
Segment 29	43	43	39
Segment 30	44	44	40
Segment 31	45	45	41
Segment 32	46	46	42
Segment 33	47	47	43
Segment 34	48	48	44
Segment 35	1	1	45
Segment 36	2	2	46

Pin Configurations

4



48 - Pin DIPS -01, -02

52 - Pin QFP -03



MIC8012

Liquid Crystal Display Driver

General Description

The MIC8012 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. An on-chip backplane oscillator is included.

A switching regulator is included on-chip to provide a negative supply where only a single, positive supply is available to power the chip.

In addition to the package options shown, the MIC8012 is available in die form; contact factory concerning dice and custom packaging requirements.

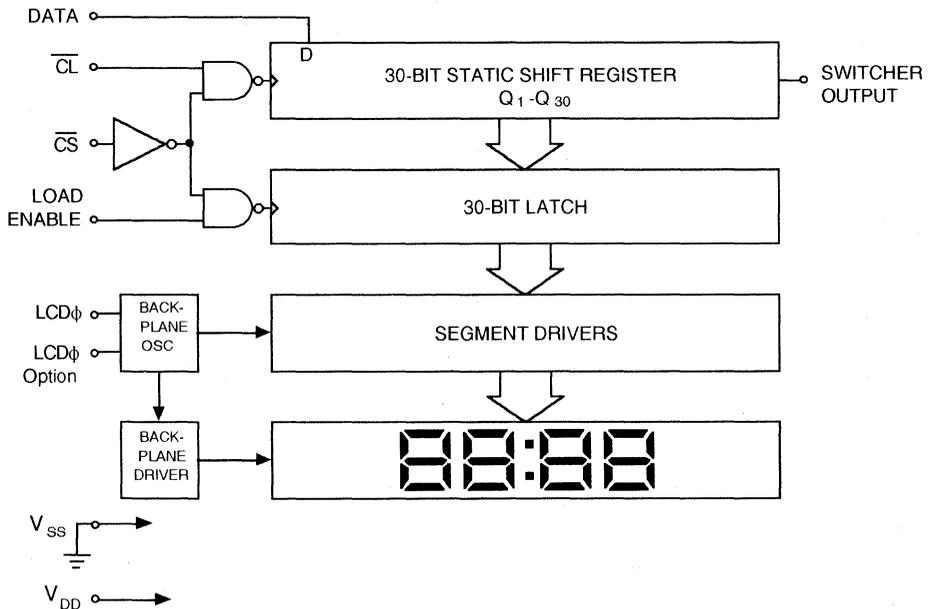
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC8012-01BN	-40°C to +85 °C	40 pin Plastic DIP

Features

- Serial interface
- Drives 30 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Compatible with dichroic, midchroic, or TM displays
- Internal backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- On-chip switching regulator for negative supply voltage
- Mil spec (883C) or extended temperature range part available; contact factory for details
- 60 V extended output swing available; contact factory for details.

Block Diagram



Note: the MIC8012 is ESD sensitive.

Absolute Maximum Ratings (Note 1, Note 2)

Supply Voltage:		Operating Temperature Range:	
V_{DD}	-0.3V to +18V	MIC8012-01BN	-40°C to +85°C
V_{EE}	$V_{DD}-35V$ to +0.3V	Storage Temperature Range	-65°C to +150°C
Input Voltage (except LCD ϕ)	-0.3V to $V_{DD}+0.3V$	Power Dissipation	250 mW
LCD ϕ Input Voltage	$V_{DD}-35V$ to $V_{DD}+0.3V$		
DC Current Drain per input pin	10 mA		

DC Electrical Characteristics (Notes 3 and 4)

$V_{DD} = 5V$, $V_{EE} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage	V_{DD}		3		18	V
Supply Current	I_{DD}	no load			200	μA
	I_{EE}	no load, $f_{BP}=100Hz$			150	
Input Low Voltage (excluding LCD ϕ)	V_{IL}		0		1.3	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$			$0.2V_{DD}$	V
Input High Voltage (excluding LCD ϕ)	V_{IH}		2		V_{DD}	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$	$0.5V_{DD}$			V
Input Low Voltage (LCD ϕ)	V_{ILX}		V_{EE}		2	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$			$0.1V_{DD}$	V
Input High Voltage (LCD ϕ)	V_{IHx}		2.5		V_{DD}	V
		-55 °C to +125 °C, $V_{DD} = 4V-16V$	$0.9V_{DD}$			V
Input Current	I_{IN}	$V_{DD}=0$ to 5V			1	μA
Input Capacitance	C_I				5	pF
Segment Output Impedance	R_{SEG}	$I_L=10\mu A$			10	k Ω
Backplane Output Impedance	R_{BP}	$I_L=10\mu A$			450	Ω

4

AC Electrical Characteristics (Note 3)

$V_{EE} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Period	t_{CL}	$V_{DD}=5V$	1000			nS
		$V_{DD}=10V$	500			
Clock Pulse Width	t_{CW}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			
Data-In Setup	t_{DS}	$V_{DD}=5V$	300			nS
		$V_{DD}=10V$	150			
Data-In Hold	t_{DH}	$V_{DD}=5V$	10			nS
		$V_{DD}=10V$	10			
Chip Select Setup to Clock	t_{CSS}	$V_{DD}=5V$	200			nS
		$V_{DD}=10V$	100			
Chip Select Hold to Clock	t_{CSH}	$V_{DD}=5V$	450			nS
		$V_{DD}=10V$	220			

AC Electrical Characteristics (Continued)

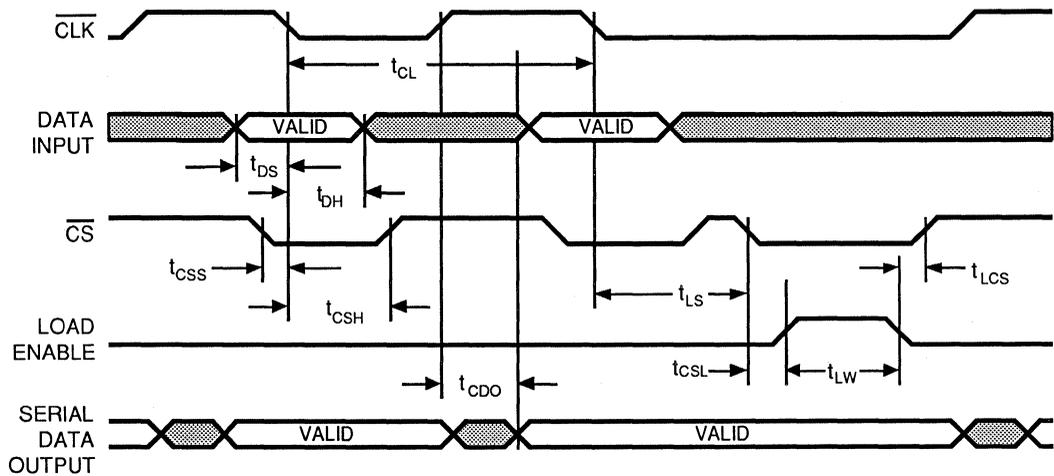
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Load Setup to Clock	t_{LS}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	280			
Chip Select Setup to Load	t_{CSL}		0			nS
Load Pulse Width	t_{LW}	$V_{DD}=5V$	500			nS
		$V_{DD}=10V$	300			
Chip Select Hold to Load	t_{LCS}		0			nS
Data Out Valid from Clock	t_{CDO}	$V_{DD}=5V$			600	nS
		$V_{DD}=10V$			300	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are referred to $V_{SS}=0V$.

Note 3: **Minimum** and **Maximum** values are guaranteed and 100% tested. **Typical** values represent the most likely parametric norm.

Note 4: $V_{DD} - 32V < V_{EE} < V_{DD} - 5V$ is required for proper device operation.

Timing Diagram

Applications Information

Power Supplies

The MIC8012 includes a p-channel switch that serves as an inverting buck-boost switching supply to develop V_{EE} (negative supply voltage) where only a positive supply is available (see Figure 1). Although the duty cycle of the p-channel gate drive is approximately 50%, the inductor current is operated in a discontinuous mode to obtain an output (V_{EE}) that is greater in magnitude than the input supply (V_{DD}). Regulation is provided by a zener diode. The switching frequency is 1/2 that of the internal backplane oscillator.

Programming

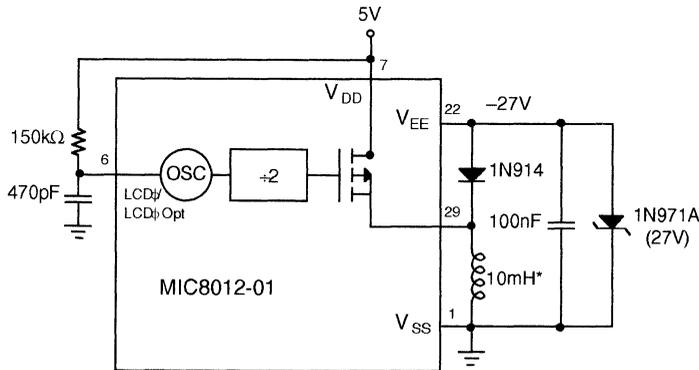
The MIC8012 utilizes an internal shift register as the means of loading segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when CHIP SELECT is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of CLOCK. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Oscillator

A one-pin oscillator (Figure 3) is made available by internally bonding $LCD\phi$ and $LCD\phi$ -Option together. An external resistor and capacitor set the operating frequency (see Figure 3), and the backplane frequency is $f_{OSC}+256$. With $R_{OSC}=150\text{ k}\Omega$ and $C_{OSC}=470\text{ pF}$, $f_{OSC}=25.6\text{ kHz}$ and $f_{BP}=100\text{ Hz}$.

A number of MIC8010-02 and/or MIC8011-02 drivers may be slaved to the MIC8012-01 oscillator by connecting their $LCD\phi$ inputs to the MIC8012-01 backplane output (see Figure 2). In this configuration the "slaved" backplane outputs are tied in parallel and operate at the frequency of $LCD\phi$. In this application the MIC8012 can generate the negative V_{EE} supply for all of the display drivers.



* 129T, 30 gauge Cu,
wound on Philips (Ferroxcube)
core #2213P-A600-3B7

Figure 1. Switching Supply Connection

Applications Information (Continued)

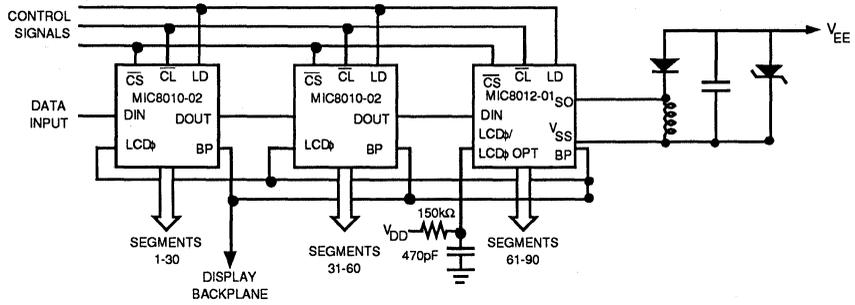


Figure 2. Cascading with MIC8010/12

Applications Information (Continued)

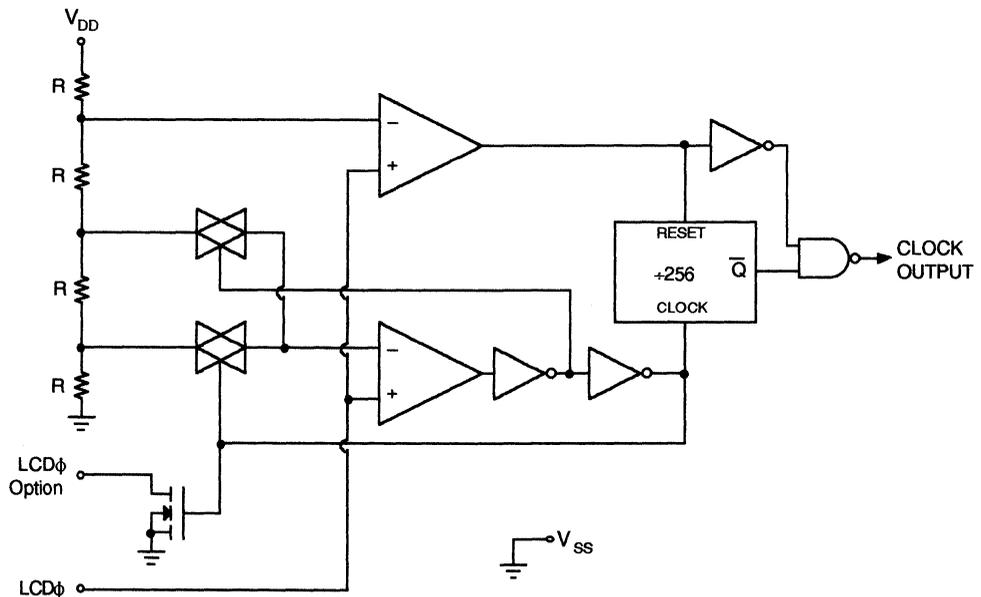


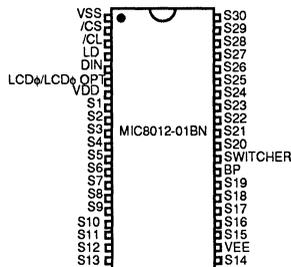
Figure 3. Internal Oscillator Circuit

Pin Assignments

Function	Pin
V _{SS} (Ground)	1
Chip Select	2
Clock	3
Load	4
Data Input	5
LCD ϕ	6
LCD ϕ Option	6
V _{DD}	7
Segment 1	8
Segment 2	9
Segment 3	10
Segment 4	11
Segment 5	12
Segment 6	13
Segment 7	14
Segment 8	15
Segment 9	16
Segment 10	17
Segment 11	18
Segment 12	19
Segment 13	20

Function	Pin
Segment 14	21
VEE	22
Segment 15	23
Segment 16	24
Segment 17	25
Segment 18	26
Segment 19	27
Backplane	28
Switcher Output	29
Segment 20	30
Segment 21	31
Segment 22	32
Segment 23	33
Segment 24	34
Segment 25	35
Segment 26	36
Segment 27	37
Segment 28	38
Segment 29	39
Segment 30	40
(Pins 41,42,43,44 are NC)	

Connection Diagram



40 Pin Plastic DIP



MIC8013

Liquid Crystal Display Driver

General Description

The MIC8013 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8013 is available in die form; contact factory concerning dice and custom packaging requirements

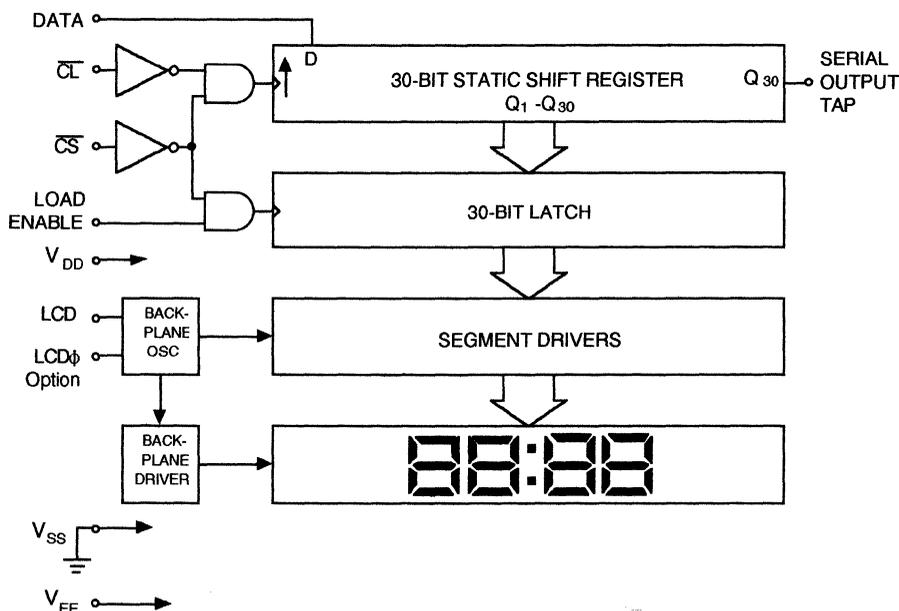
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC8013-01BN	- 40°C to +85°C	40 pin Plastic DIP
MIC8013-02BN	- 40°C to +85°C	40 pin Plastic DIP
MIC8013-01AL	- 55°C to +125°C	40 pin Ceramic LCC
MIC8013-02AL	- 55°C to +125°C	40 pin Ceramic LCC

Features

- Logic compatible with AMI/Gould S4520
- Drives 30 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec or extended temperature range part available; contact factory for details
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

Block Diagram



Note: The MIC8013 is ESD sensitive.

Absolute Maximum Ratings (Note 1, Note 2)

V_{DD}	-0.3V to +17V	Operating Temperature Range:	
V_{BB}	$V_{SS} + 0.3V$ to $V_{DD} - 32V$	MIC8013-01BN, -02BN	-40°C to +85°C
Input Voltage (except LCD ϕ)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$	MIC8013-01AL, -02AL	-55°C to +125°C
LCD ϕ Input Voltage	$V_{BB} - 0.3V$ to $V_{DD} + 0.3V$	Storage Temperature Range	-65°C to +150°C
DC Current Drain per input pin	10 mA	Power Dissipation	250 mW

DC Electrical Characteristics (Notes 3 and 4)

$3V \leq V_{DD} \leq 16V$, $V_{BB} = -25V$, $V_{SS} = 0V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Supply Voltage	V_{DD}		3		16	V
Display Supply Voltage	V_{BB}	$V_{BB} \leq V_{SS}$	$V_{DD} - 32$		$V_{DD} - 5$	V
Supply Current (external oscillator)	I_{DD}	no load, CMOS input levels			200	
Supply Current (internal oscillator)		$V_{DD} \leq 5V$			200	μA
		no load, $V_{DD} = 16V$, CMOS input levels			750	
Display Driver Current	I_{BB}	$f_{BP} = 100Hz$, no loads			-200	μA
Input Low Voltage (excluding LCD ϕ)	V_{IL}		V_{SS}		$0.2V_{DD}$	V
Input High Voltage (excluding LCD ϕ)	V_{IH}	$V_{DD} \geq 5V$	$0.5V_{DD}$		V_{DD}	V
Input Low Voltage (LCD ϕ)	V_{ILX}	externally driven	V_{BB}		$0.1V_{DD}$	V
Input High Voltage (LCD ϕ)	V_{IHx}	externally driven	$0.9V_{DD}$		V_{DD}	V
Input Leakage Current	I_L	$V_{DD} = 0$ to $5V$			1	μA
Input Capacitance	C_I				5	pF
DC Bias (Average) Any Segment Output to Backplane	V_{OAVG}				+/- 25	mV
Segment Output	C_{LSEG}				1000	pF
Backplane Output	C_{LBP}				40000	pF
Segment Output Impedance	R_{SEG}	$I_L = 10\mu A$			10	k Ω
Backplane Output Impedance	R_{BP}	$I_L = 10\mu A$			312	Ω
Data Out Output Impedance	R_{DD}				3	k Ω
Data Out Current	I_{DOH}	Source Current, $V_{OH} = V_{DD} - 5V$			0.6	mA
	I_{DOL}	Sink Current, $V_{OL} = 0.5V$	-0.6			

AC Electrical Characteristics (Note 3)

$V_{BB} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Cycle time (noncascaded)	t_{CYC}	$V_{DD} = 3V$	1000			nS
		$V_{DD} = 5V$	500			
		$V_{DD} \geq 7.5V$	320			
Cycle time (cascaded)	t_{CYC}	$V_{DD} = 3V$	1300			nS
		$V_{DD} = 5V$	600			
		$V_{DD} \geq 7.5V$	350			

AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Pulse Width Low/High	t_{OL}, t_{OH}	$V_{DD} = 3V$	450			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
Clock Pulse Width High (cascaded)	t_{OH}	$V_{DD} = 3V$	750			nS
		$V_{DD} = 5V$	320			
		$V_{DD} \geq 7.5V$	180			
Clock Rise, Fall Time (Note 4)	t_r, t_f			1		μS
Data-in Setup	t_{DS}	$V_{DD} = 3V$	300			nS
		$V_{DD} = 5V$	150			
		$V_{DD} \geq 7.5V$	120			
\overline{CS} Setup to Clock	t_{CSC}	$V_{DD} = 3V$	200			nS
		$V_{DD} = 5V$	100			
		$V_{DD} \geq 7.5V$	50			
Data-In Hold	t_{DH}	$V_{DD} = 5V$	10			nS
		$V_{DD} \geq 7.5V$	10			
\overline{CS} Hold	t_{CCS}	$V_{DD} = 3V$	450			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
Load Pulse Setup (Note 5)	t_{CL}	$V_{DD} = 3V$	500			nS
		$V_{DD} = 5V$	280			
		$V_{DD} \geq 7.5V$	180			
\overline{CS} Hold (rising LOAD to rising \overline{CS})	t_{LCS}	$V_{DD} = 3V$	300			nS
		$V_{DD} = 5V$	200			
		$V_{DD} \geq 7.5V$	150			
Load Pulse Delay	t_{LC}		0			nS
Load Pulse Width (Note 5)	t_{LW}	$V_{DD} = 3V$	500			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
\overline{CS} Setup to Load	t_{CSL}		0			nS
Data Out Valid from Clock	t_{CDO}	$V_{DD} = 3V$			550	nS
		$V_{DD} = 5V$			220	
		$V_{DD} \geq 7.5V$			110	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are referred to $V_{SS}=0V$.

Note 3: Minimum and Maximum values are guaranteed and 100% tested. **Typical** values represent the most likely parametric norm.

Note 4: Power consumption increases for clock rise or fall times greater than 100 nS

Note 5: LOAD may also be held high while clocking. In this case, the latch is transparent, and the falling edge of LOAD will latch the data

Note 6: $V_{DD} - 32V < V_{BB} < V_{DD} - 5V$ is required for proper device operation.

Applications Information

The MIC8013 utilizes a serial data interface as a means of programming the LCD segment outputs.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of CLOCK, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of CLOCK. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, CLOCK should remain high. The driver may then be deselected without disturbing the contents of the shift register. If CLOCK is held low while CHIP SELECT is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, CLOCK, and CHIP SELECT are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8013 can operate from a single supply of $V_{DD}=4$ to 18V, with V_{BB} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{BB} for segment/backplane voltage. V_{BB} is then negative with respect to V_{SS} , and the po-

tential across V_{DD} and V_{BB} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{BB} to V_{DD} . For higher output voltage swing see the MIC8030 series devices.

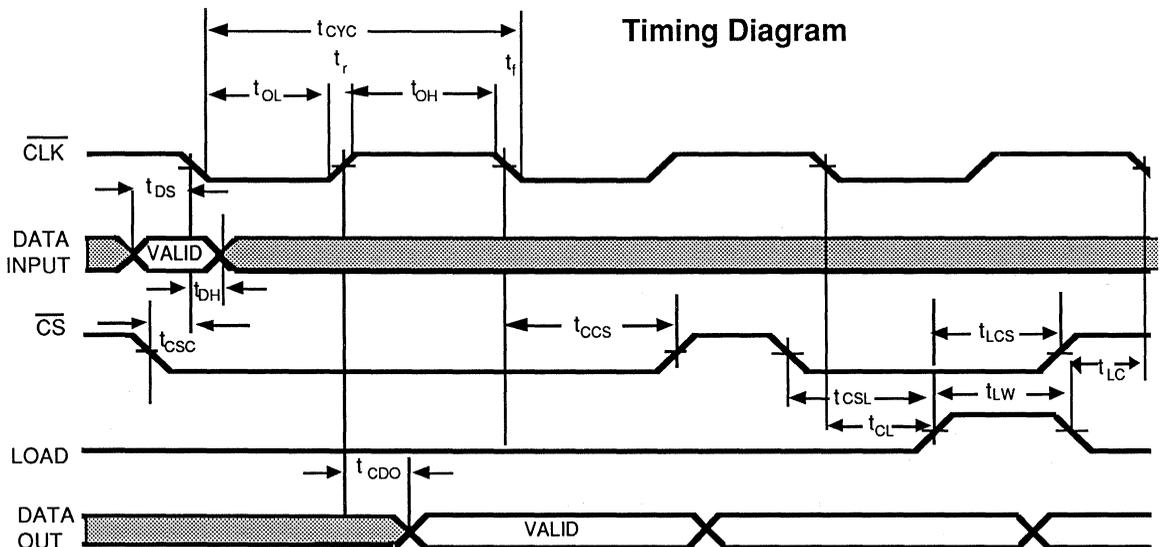
Internal Oscillator

The on-chip oscillator (Figure 1) is available in two configurations. Devices with the "-01" suffix feature a 1-pin oscillator ($LCD\phi$ and $LCD\phi$ Option tied together). An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC}+256$. With $R_{OSC}=150$ k Ω and $C_{OSC}=470$ pF, $f_{OSC}=25.6$ kHz and $f_{BP}=100$ Hz.

Devices with a "-02" suffix bring out only $LCD\phi$, leaving $LCD\phi$ Option disconnected. In this case $LCD\phi$ is driven with an external clock; in a typical application several MIC8013-02 drivers would be slaved to a master MIC8013-01 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

An "-03" suffix version of this part is available which offers the option of using either of the two above mentioned configurations. The CHIP SELECT is always low on this option; contact factory for more details.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, dc manner. $LCD\phi$ is connected to V_{DD} for this mode, used primarily for driving LED and VF type displays.



Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	LOAD	Q ₁ (SR)	Q _N (SR)	BP	Q _N (DRIVER)
X	X	1	0	NC	NC	0	Q _N (L)
X	X	1	1	NC	NC	1	Q _N (L)
0		0	0	NC	NC	1	Q _N (L)
0		0	1	NC	NC	1	Q _N (L)
0		0	0	0	Q _{(N - 1) -- Q_N}	1	Q _N (L)
0		0	1	0	Q _{(N - 1) -- Q_N}	1	Q _N (SR)
1		0	0	NC	NC	1	Q _N (L)
1		0	1	NC	NC	1	Q _N (L)
1		0	0	1	Q _{(N - 1) -- Q_N}	1	Q _N (L)
1		0	1	1	Q _{(N - 1) -- Q_N}	1	Q _N (SR)

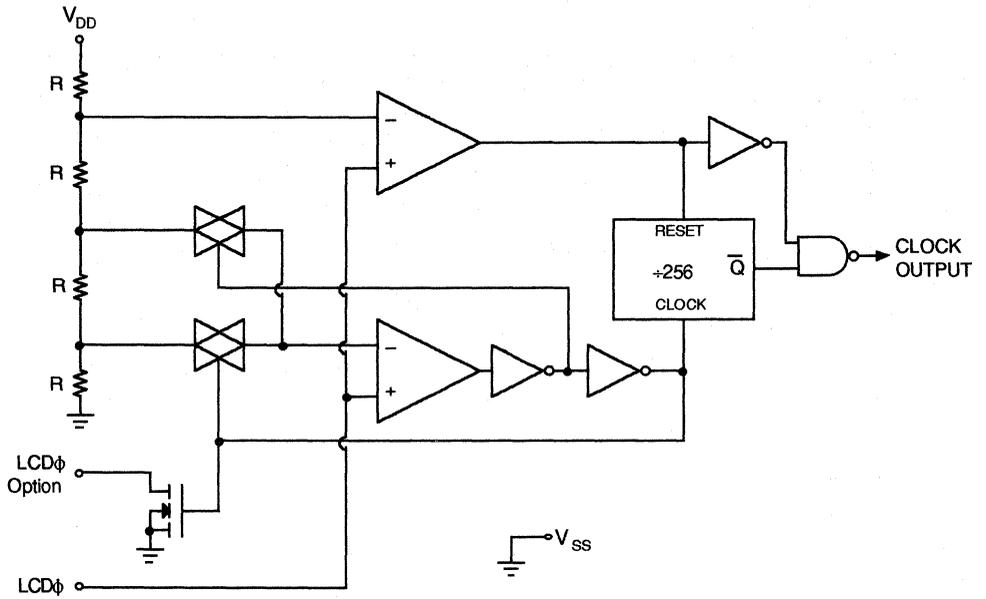


Figure 1. Internal Oscillator Circuit

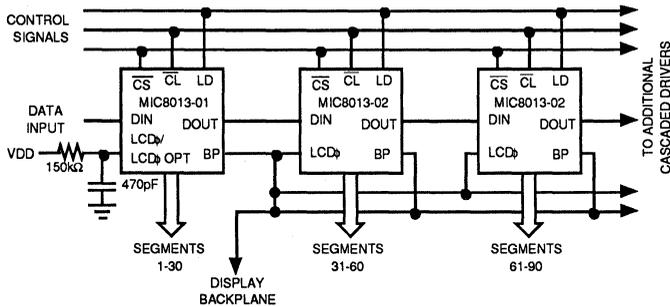


Figure 2. Cascading with Internal Clock Oscillator - 01 Option

Typical Applications (Continued)

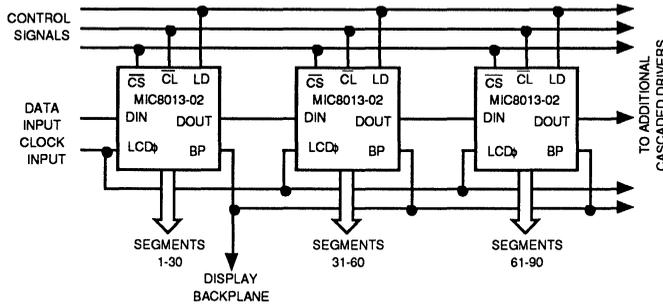


Figure 3. Cascading with External Clocking Source - 02 Option

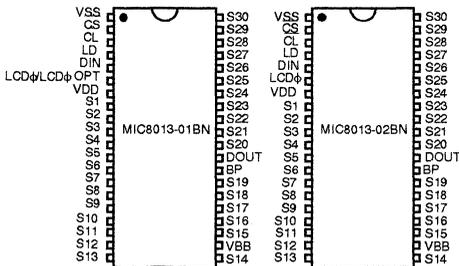
Pin Assignments

Function	Device Suffix	
	-01	-02
V _{SS} (Ground)	1	1
Chip Select	2	2
Clock	3	3
Load	4	4
Data Input	5	5
LCDφ	6	6
LCDφ Option	6	NC
V _{DD}	7	7
Segment 1	8	8
Segment 2	9	9
Segment 3	10	10
Segment 4	11	11
Segment 5	12	12
Segment 6	13	13
Segment 7	14	14
Segment 8	15	15
Segment 9	16	16
Segment 10	17	17
Segment 11	18	18
Segment 12	19	19
Segment 13	20	20

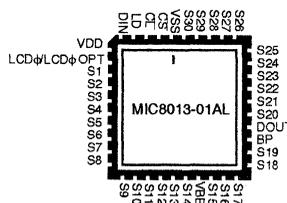
Function	Device Suffix	
	-01	-02
Segment 14	21	21
V _{BB}	22	22
Segment 15	23	23
Segment 16	24	24
Segment 17	25	25
Segment 18	26	26
Segment 19	27	27
Backplane	28	28
Data Output	29	29
Segment 20	30	30
Segment 21	31	31
Segment 22	32	32
Segment 23	33	33
Segment 24	34	34
Segment 25	35	35
Segment 26	36	36
Segment 27	37	37
Segment 28	38	38
Segment 29	39	39
Segment 30	40	40

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Connection Diagrams



40 Pin Plastic DIP



40 Pin Ceramic Chip Carrier



MIC8014

Liquid Crystal Display Driver

General Description

The MIC8014 driver is designed for use with liquid crystal displays. A serial data interface is used to load an internal register, which in turn controls the segment outputs. A FIFO output allows multiple chips to be cascaded and programmed via a single, serial interface. An on-chip backplane oscillator is included.

In addition to the package options shown, the MIC8014 is available in die form; contact factory concerning dice and custom packaging requirements

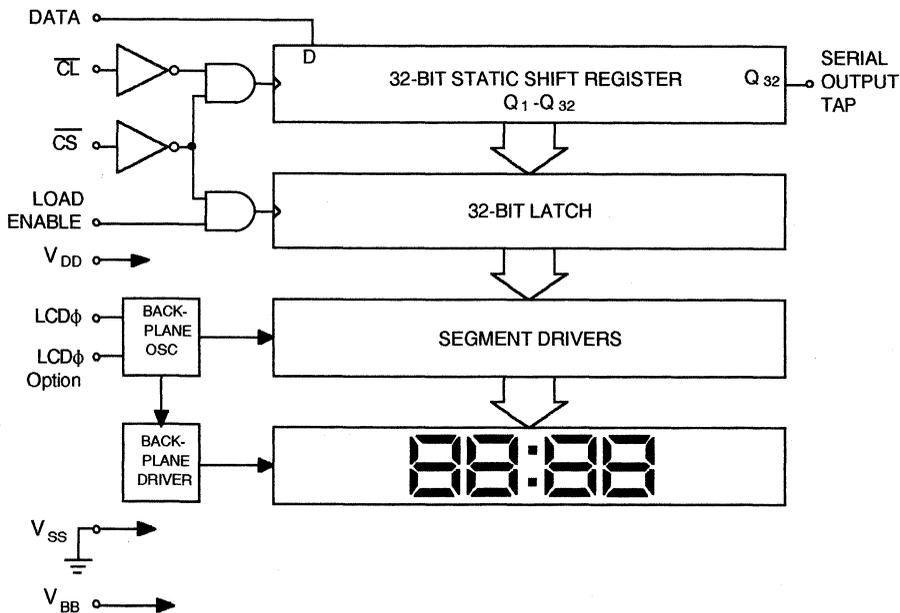
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC8014-03BV	-40°C to +85 °C	44 pin PLCC
MIC8014-03AE	-55°C to +125 °C	44 pin CERQUAD

Features

- Pin to pin compatible with AMI/Gould S4520
- Drives 32 segments
- Built using Micrel's proprietary rugged high voltage CMOS process for improved reliability.
- Compatible with dichroic, midchroic, VF or TM displays
- Internal or external backplane oscillator
- 3V to 18V logic supply range
- 5V to 35V output drive swing
- Single or split power supply operation
- Mil spec (883C) or extended temperature range part available; contact factory for details.
- Cascadable serial interface
- 60V extended output swing available; contact factory for details

Block Diagram



Note: The MIC8014 is ESD sensitive.

Absolute Maximum Ratings (Note 1, Note 2)

V_{DD}	-0.3V to +17V	Operating Temperature Range:	
V_{BB}	$V_{SS} + 0.3V$ to $V_{DD} - 32V$	MIC8014-03BV	-40°C to +85°C
Input Voltage (except LCD ϕ)	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$	MIC8014-03AE	-55°C to +125°C
LCD ϕ Input Voltage	$V_{BB} - 0.3V$ to $V_{DD} + 0.3V$	Storage Temperature Range	-65°C to +150°C
DC Current Drain per input pin	10 mA	Power Dissipation	250 mW

DC Electrical Characteristics (Notes 3 and 4)

$3V \leq V_{DD} \leq 16V$, $V_{BB} = -25V$, $V_{SS} = 0V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Supply Voltage	V_{DD}		3		16	V
Display Supply Voltage	V_{BB}	$V_{BB} \leq V_{SS}$	$V_{DD} - 32$		$V_{DD} - 5$	V
Supply Current (external oscillator)	I_{DD}	no load, CMOS input levels			200	
Supply Current (internal oscillator)		$V_{DD} \leq 5V$			200	μA
		no load, $V_{DD} = 16V$, CMOS input levels			750	
Display Driver Current	I_{BB}	$f_{BP} = 100\text{ Hz}$, no loads			-200	μA
Input Low Voltage (excluding LCD ϕ)	V_{IL}		V_{SS}		$0.2V_{DD}$	V
Input High Voltage (excluding LCD ϕ)	V_{IH}	$V_{DD} \geq 5V$	$0.5V_{DD}$		V_{DD}	V
Input Low Voltage (LCD ϕ)	V_{ILX}	externally driven	V_{BB}		$0.1V_{DD}$	V
Input High Voltage (LCD ϕ)	V_{IHX}	externally driven	$0.9V_{DD}$		V_{DD}	V
Input Leakage Current	I_L	$V_{DD} = 0$ to $5V$			1	μA
Input Capacitance	C_I				5	pF
DC Bias (Average) Any Segment Output to Backplane	V_{OAVG}				+/- 25	mV
Segment Output	C_{LSEG}				1000	pF
Backplane Output	C_{LBP}				40000	pF
Segment Output Impedance	R_{SEG}	$I_L = 10\mu A$			10	k Ω
Backplane Output Impedance	R_{BP}	$I_L = 10\mu A$			312	Ω
Data Out Output Impedance	R_{DD}				3	k Ω
Data Out Current	I_{DOH}	Source Current, $V_{OH} = V_{DD} - 5V$			0.6	mA
	I_{DOL}	Sink Current, $V_{OL} = 0.5V$	-0.6			

AC Electrical Characteristics (Note 3)

$V_{BB} = -25V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Cycle time (noncascaded)	t_{CYC}	$V_{DD} = 3V$	1000			nS
		$V_{DD} = 5V$	500			
		$V_{DD} \geq 7.5V$	320			
Cycle time (cascaded)	t_{CYC}	$V_{DD} = 3V$	1300			nS
		$V_{DD} = 5V$	600			
		$V_{DD} \geq 7.5V$	350			

AC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock Pulse Width Low/High	t_{OL}, t_{OH}	$V_{DD} = 3V$	450			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
Clock Pulse Width High (cascaded)	t_{OH}	$V_{DD} = 3V$	750			nS
		$V_{DD} = 5V$	320			
		$V_{DD} \geq 7.5V$	180			
Clock Rise, Fall Time (Note 4)	t_r, t_f			1		μS
Data-in Setup	t_{DS}	$V_{DD} = 3V$	300			nS
		$V_{DD} = 5V$	150			
		$V_{DD} \geq 7.5V$	120			
\overline{CS} Setup to Clock	t_{CSC}	$V_{DD} = 3V$	200			nS
		$V_{DD} = 5V$	100			
		$V_{DD} \geq 7.5V$	50			
Data-In Hold	t_{DH}	$V_{DD} = 5V$	10			nS
		$V_{DD} \geq 7.5V$	10			
\overline{CS} Hold	t_{CCS}	$V_{DD} = 3V$	450			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
Load Pulse Setup (Note 5)	t_{CL}	$V_{DD} = 3V$	500			nS
		$V_{DD} = 5V$	280			
		$V_{DD} \geq 7.5V$	180			
\overline{CS} Hold (rising LOAD to rising \overline{CS})	t_{LCS}	$V_{DD} = 3V$	300			nS
		$V_{DD} = 5V$	200			
		$V_{DD} \geq 7.5V$	150			
Load Pulse Delay	t_{LC}		0			nS
Load Pulse Width (Note 5)	t_{LW}	$V_{DD} = 3V$	500			nS
		$V_{DD} = 5V$	220			
		$V_{DD} \geq 7.5V$	140			
\overline{CS} Setup to Load	t_{CSL}		0			nS
Data Out Valid from Clock	t_{CDO}	$V_{DD} = 3V$			550	nS
		$V_{DD} = 5V$			220	
		$V_{DD} \geq 7.5V$			110	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Electrical Characteristics** do not apply when operating the device beyond its specified operating ratings.

Note 2: All voltages are referred to $V_{SS}=0V$.

Note 3: Minimum and Maximum values are guaranteed and 100% tested. **Typical** values represent the most likely parametric norm.

Note 4: Power consumption increases for clock rise or fall times greater than 100 nS

Note 5: LOAD may also be held high while clocking. In this case, the latch is transparent, and the falling edge of LOAD will latch the data

Note 6: $V_{DD} - 32V < V_{BB} < V_{DD} - 5V$ is required for proper device operation.

Applications Information

The MIC8014 utilizes a serial data interface as a means of programming the LCD segment outputs.

An internal shift register is used to load segment data, and a latch is used to transfer this data to the segment drivers. The shift register can be loaded when chip select is held low (V_{SS}). DATA INPUT is shifted in on the falling edges of CLOCK, and the contents of the shift register exit at SERIAL DATA OUTPUT on the rising edges of CLOCK. A high level (V_{DD}) at LOAD enables the transfer of data from the shift register to the latch. The latch is transparent while LOAD is held high.

If data is shifted into the internal register but not immediately loaded into the latch, CLOCK should remain high. The driver may then be deselected without disturbing the contents of the shift register. If CLOCK is held low while CHIP SELECT is toggled, an extra clock pulse will be generated in the chip, thereby shifting the data.

A data "1" causes the associated segment output to operate 180° out of phase with the backplane output, thus turning the segment on (the segment becomes opaque). If a "0" is loaded, the associated segment will remain off (clear).

Several chips can be cascaded by simply connecting SERIAL DATA OUTPUT from one chip to DATA INPUT of the next. LOAD, CLOCK, and CHIP SELECT are each paralleled to allow simultaneous control of all drivers with only 3 lines plus one data line.

Power Supplies

The MIC8014 can operate from a single supply of $V_{DD}=4$ to 18V, with V_{BB} and V_{SS} at ground, or from two supplies with V_{DD} for logic voltage and V_{BB} for segment/backplane volt-

age. V_{BB} is then negative with respect to V_{SS} , and the potential across V_{DD} and V_{BB} must be limited to 35V. If 5V logic levels are used to program the display driver, then V_{DD} should be 5V. The segment and backplane drivers obtain maximum available output swing by switching from V_{BB} to V_{DD} . For higher output voltage swing see the MIC8030 series devices.

Internal Oscillator

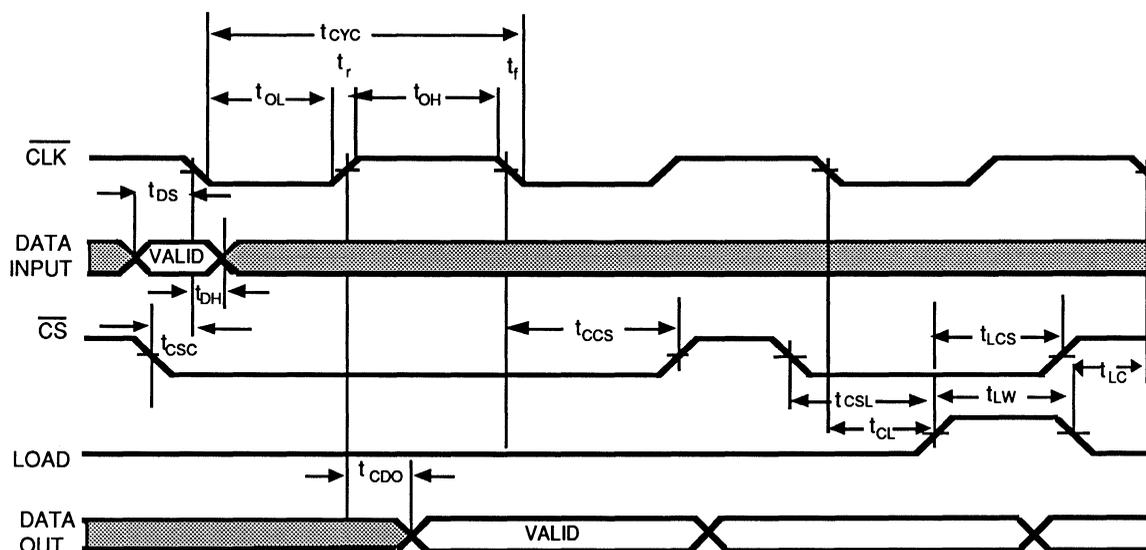
The on-chip oscillator (Figure 1) can be used in two configurations. If pins 19 and 20 are tied together, ($LCD\phi$ and $LCD\phi$ Option tied together), a one pin oscillator configuration results. An external resistor and capacitor set the operating frequency (see Figure 2), and the backplane frequency is $f_{OSC}+256$. With $R_{OSC}=150\text{ k}\Omega$ and $C_{OSC}=470\text{ pF}$, $f_{OSC}=25.6\text{ kHz}$ and $f_{BP}=100\text{ Hz}$.

To configure this device such that an external oscillator can be used, connect the oscillator to $LCD\phi$, leaving $LCD\phi$ Option disconnected. In a typical application, several MIC8014 drivers would be slaved to a master MIC8014 to drive a large display with a common backplane. Figure 2 shows this mode of operation. The input clock signal resets the divider shown in Figure 1 on each cycle so that the backplane operates at the external clock frequency.

An "-03" suffix is used to indicate that this device has both $LCD\phi$ and $LCD\phi$ Option pinned out externally, unlike other members of the MIC8010 family.

The oscillator may be disabled entirely, which allows the segment and backplane outputs to operate in a static, DC manner. $LCD\phi$ is connected to V_{DD} for this mode, used in conjunction with VF or LED displays.

Timing Diagram



Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	LOAD	Q ₁ (SR)	Q _N (SR)	BP	Q _N (DRIVER)
X	X	1	0	NC	NC	0	Q _N (L)
X	X	1	1	NC	NC	1	Q _N (L)
0		0	0	NC	NC	1	Q _N (L)
0		0	1	NC	NC	1	Q _N (L)
0		0	0	0	Q _{(N-1) -- Q_N}	1	Q _N (L)
0		0	1	0	Q _{(N-1) -- Q_N}	1	Q _N (SR)
1		0	0	NC	NC	1	Q _N (L)
1		0	1	NC	NC	1	Q _N (L)
1		0	0	1	Q _{(N-1) -- Q_N}	1	Q _N (L)
1		0	1	1	Q _{(N-1) -- Q_N}	1	Q _N (SR)

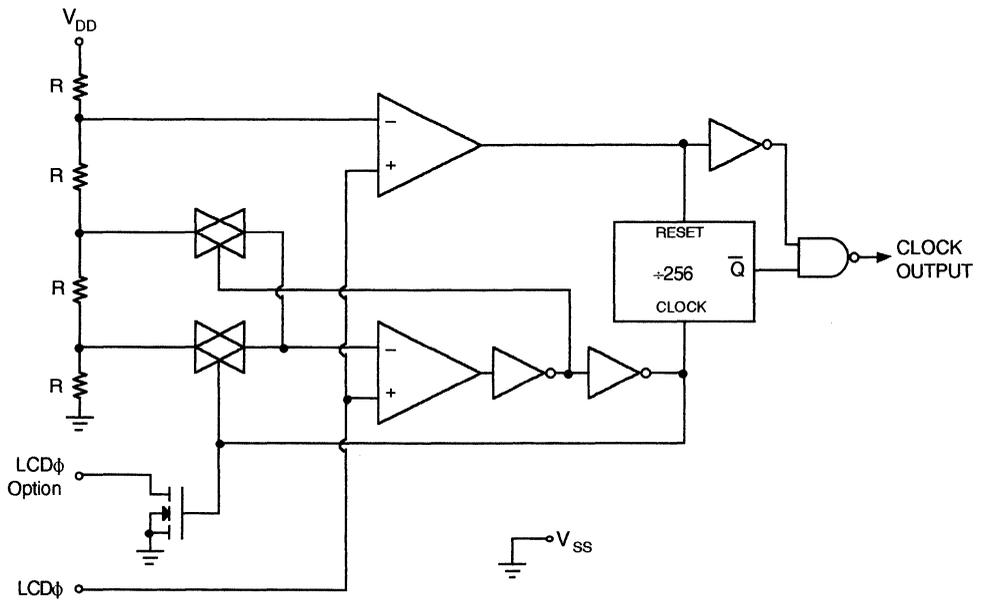


Figure 1. Internal Oscillator Circuit

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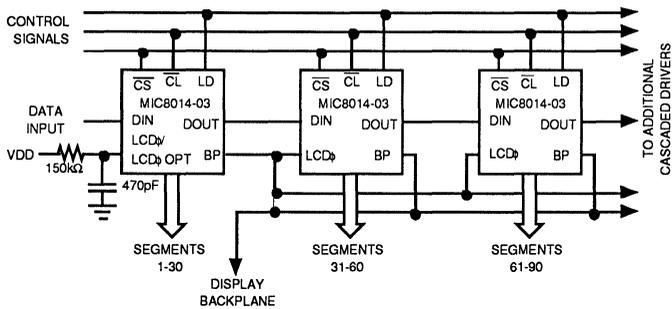


Figure 2. Cascading with Internal Clock Oscillator

Typical Applications (Continued)

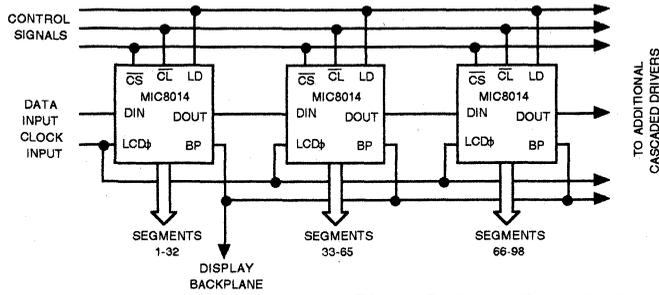


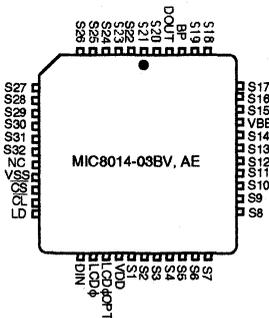
Figure 3. Cascading with External Clocking Source

Pin Assignments

Function	Device Suffix -03
Segment 21	1
Segment 22	2
Segment 23	3
Segment 24	4
Segment 25	5
Segment 26	6
Segment 27	7
Segment 28	8
Segment 29	9
Segment 30	10
Segment 31	11
Segment 32	12
NC	13
VSS	14
CS	15
Clock	16
Load	17
Data In	18
LCD φ	19
LCD φ Opt.	20
VDD	21
Segment 1	22

Function	Device Suffix -03
Segment 2	23
Segment 3	24
Segment 4	25
Segment 5	26
Segment 6	27
Segment 7	28
Segment 8	29
Segment 9	30
Segment 10	31
Segment 11	32
Segment 12	33
Segment 13	34
Segment 14	35
VBB	36
Segment 15	37
Segment 16	38
Segment 17	39
Segment 18	40
Segment 19	41
BP	42
Data Out	43
Segment 20	44

Connection Diagram





General Description

The MIC8030/MIC8031 is a CMOS high voltage liquid crystal display driver. Up to 38 segments can be driven from four CMOS level inputs (CLOCK, DATA IN, LOAD and CHIP SELECT). The MIC8031 is rated at 100V and the MIC8030 is rated at 50V. Data is loaded serially into a shift register, and transferred to latches which hold the data until new data is received.

The backplane can be driven from external source, or the internal oscillator can be used. If the internal oscillator is used, the frequency of the backplane will be determined by an external resistor and capacitor. The oscillator need not be used if a DC output is desired.

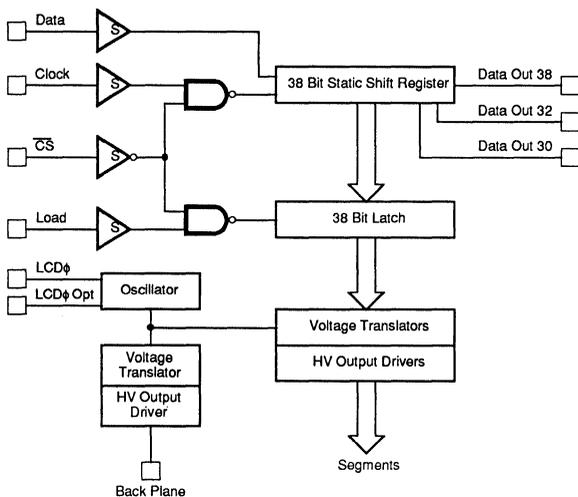
Features

- High Voltage Outputs capable of a driving up to 100 volt outputs from 5 to 15 volt logic
- Drives 30, 32, or 38 segments
- Cascadable
- On chip Oscillator or External Backplane Input
- CMOS construction for wide supply range and low power consumption
- Schmitt Triggers on all inputs
- CMOS, PMOS, and NMOS compatible

Applications

- Dichroic and Standard Liquid Crystal Displays
- Flat Panel Displays
- Print Head Drives
- Vacuum Fluorescent Displays

Functional Diagram

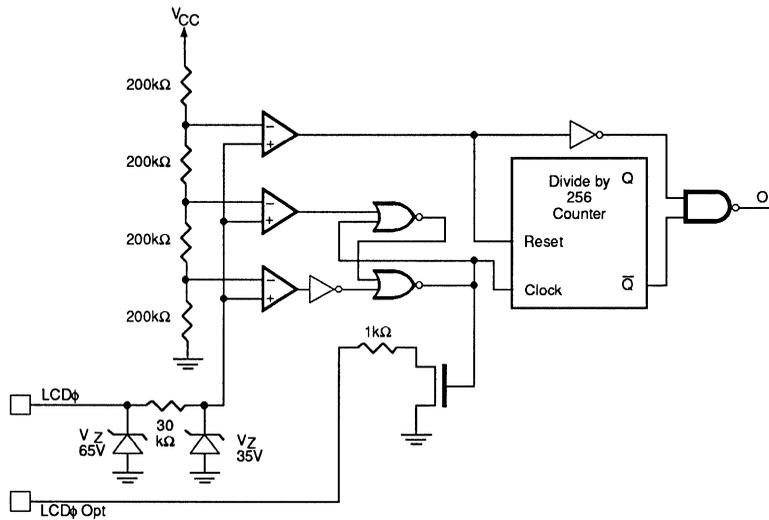


Ordering Information

Part Number	Temperature Range	Package
MIC8030AEB MIC8031AEB	-55°C to +125°C	44 lead CER QUAD, Class B screened
MIC8030ALB MIC8031ALB	-55°C to +125°C	44 lead Ceramic Leadless Chip Carrier, Class B screened
MIC8030CL MIC8031CL	0°C to +70°C	44 pin Leadless Chip Carrier
MIC8030CV MIC8031CV	0°C to +70°C	44 pin PLCC
MIC8030CN MIC8031CN	0°C to +70°C	48 pin plastic DIP

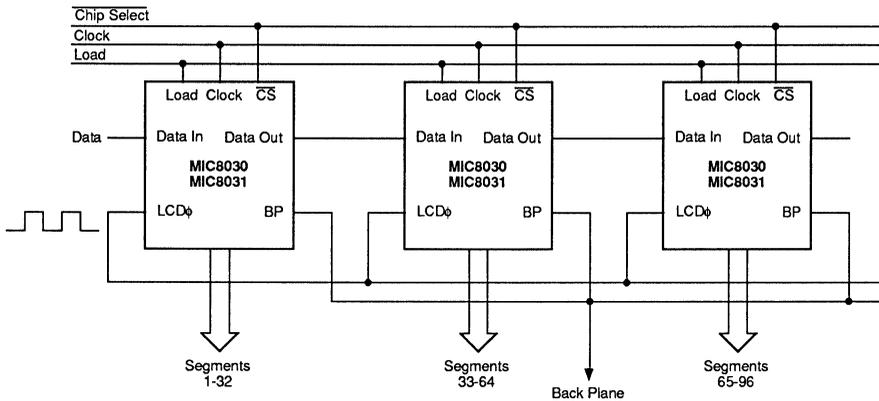
* Contact factory for other package options.

Internal Oscillator Circuit

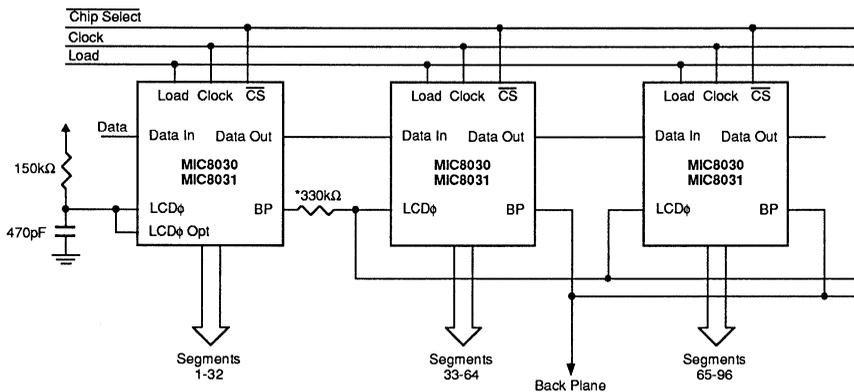


Typical Application

External Oscillator



Internal Oscillator



*Required if using MIC8031 with $V_{BP} > 50V$.

Absolute Maximum Ratings

V _{CC}	18V
V _{BB} (MIC8030)	75V
V _{BB} (MIC8031)	110V
Inputs (CLK, DATA IN, LOAD, \overline{CS})	-0.5V to 18V
Inputs (LCD0)	-0.5V to 50V
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Maximum Current into and out of any segment	20 mA
Maximum Power Dissipation, any segment	50 mW
Maximum Total power dissipation	600 mW

DC Electrical Characteristics: V_{CC} = 5V, V_{SS} = 0V, V_{BB} = 35V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V _{CC}	Logic Supply Voltage	MIC8030	4.5	5	5.5	V
V _{CC}	Logic Supply Voltage	MIC8031	4.5	5	16.5	V
V _{BB}	Display Supply Voltage	MIC8030	20	35	50	V
V _{BB}	Display Supply Voltage	MIC8031	20	35	100	V
I _{CC}	Supply Current (external oscillator)	Note 1		35	250	μA
	Supply Current (internal oscillator)	Note 1		35	250	
I _{BB}	Display Driver Current	F _{BP} = 100Hz No Loads		7	100	μA
I _{BB}	Display Driver Current	MIC8031, V _{BB} = 100V		20	200	μA
INPUTS (CLK, DATA IN, LOAD, \overline{CS})						
V _{IH}	Input High Level		V _{CC} - 1.5	V _{CC} - 1.8	V _{CC}	V
V _{IL}	Input Low Level		0	2.5	2.0	V
I _L	Input Leakage Current			<1	5	μA
C _I	Input Capacitance	Note 2		5	10	pF
INPUT LCD0						
V _{IH}	LCD0 Input High Level	Externally driven	0.9V _{CC}	V _{CC}	50	V
V _{IL}	LCD0 Input Low Level	Externally driven	-0.5V	0	0.1V _{CC}	V
I _{LCD0}	LCD0 Leakage Current	V _{LCD0} = 15V		2	10	μA
I _{LCD0}	LCD0 Leakage Current	V _{LCD0} = 35V		6	100	μA
I _{LCD0}	LCD0 Leakage Current	V _{LCD0} = 50V			1	mA
CAPACITANCE LOADS (TYPICAL)						
C _{LSEG}	Segment Output	F _{BP} < 100Hz			100	pF
C _{LBP}	Backplane Output	F _{BP} < 100Hz			4000	pF
V _{OAVG}	DC Bias (Average) Any Segment	F _{BP} < 100Hz, Note 2			+25	mV
OUTPUT TO BACKPLANE						
R _{SEG}	Segment Output Impedance	I _L = 100μA		1.4	10	kΩ
R _{BP}	Backplane Output Impedance	I _L = 100μA		170	312	Ω
R _{DATA OUT}	Data Out Output Impedance	I _L = 100μA		1.8	3	kΩ

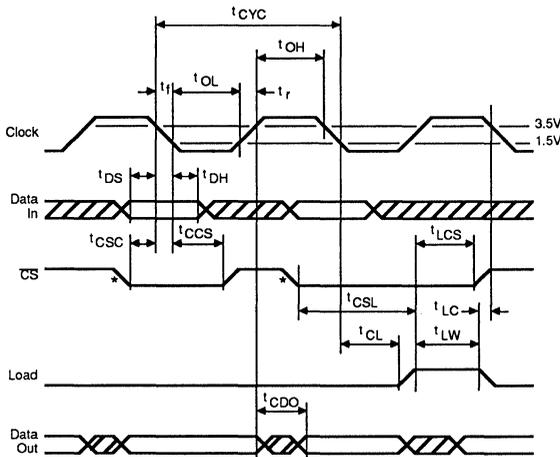
Note 1: CMOS input levels. No loads.

Note 2: Guaranteed by design but not tested on a production basis.

AC Electrical Characteristics: $V_{CC} = 5V$, $V_{SS} = 0V$, $V_{BB} = 35V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$

Symbol	Parameter	Min	Typ	Max	Units
t _{CYC}	Cycle Time	500			nS
t _{OL} , t _{OH}	Clock Pulse Width low/high	250			nS
t _r , t _f	Clock rise/fall			1	μS
t _{DS}	Data In Setup	100			nS
t _{CSC}	\overline{CS} Setup to Clock	100			nS
t _{DH}	Data Hold	10			nS
t _{CCS}	\overline{CS} Hold	220			nS
t _{CL}	Load Pulse Setup	250			nS
t _{LCS}	\overline{CS} Hold (rising load to rising \overline{CS})	200			nS
t _{LW}	Load Pulse Width	300			nS
t _{LC}	Load Pulse Delay (falling load to falling clock)	0			nS
t _{CDO}	Data Out Valid from Clock			220	nS
t _{CSL}	\overline{CS} Setup to LOAD	0			nS
F _{BP}	Backplane Frequency	50	100	2000	Hz

Timing Diagram



* The CS high-to-low transition will generate a clock pulse.

Logic Truth Table

Data In	Clock	Chip Select	Load	Q ₁ (SR)	Q _N (SR)	Q _N (DRIVER)
X	X	1	X	NC	NC	Q _N (L)
0	⌋	0	0	NC	NC	Q _N (L)
0	⌋	0	1	NC	NC	Q _N (L)
0	⌋	0	0	0	Q _N - 1 → Q _N	Q _N (L)
0	⌋	0	1	0	Q _N - 1 → Q _N	Q _N (SR)
1	⌋	0	0	NC	NC	Q _N (L)
1	⌋	0	1	NC	NC	Q _N (L)
1	⌋	0	0	1	Q _N - 1 → Q _N	Q _N (L)
1	⌋	0	1	1	Q _N - 1 → Q _N	Q _N (SR)



MIC8030/MIC8031 Application Hints on Compatibility with Display Drivers Produced by AMI and HOLT

The MIC8030/MIC8031 can be made compatible with all bonding options of the Gould-AMI S4520 as well as all bonding options of the HOLT HI-8010. However, the high voltage supply must be positive with respect to ground for the MIC8030/MIC8031. Both AMI and HOLT use a negative High Voltage. See MIC8010/11/12/13 family for drop in replacements in existing sockets.

High Voltage Supply

Device	Vmin	Vmax	Absolute Max
MIC8031	20V	100V	110V
MIC8030	20V	50V	75V
HI-8010	Vlogic-35V	+0.3V	Vlogic-35V
S4520	Vlogic-32V	+0.3V	Vlogic-32V

Logic Power Supply

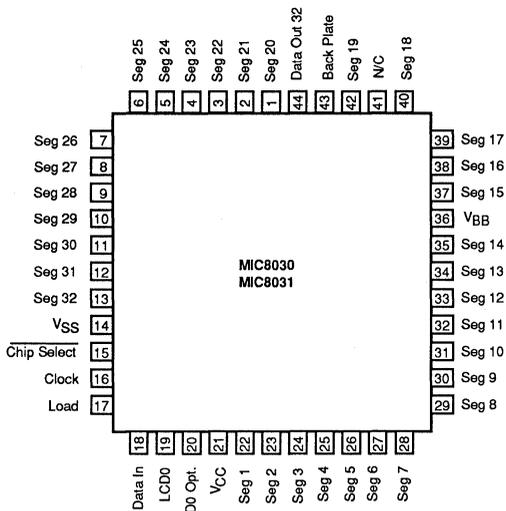
Device	Vmin	Vmax	Absolute Max
MIC8031	4.5V	16.5V	18V
MIC8030	4.5V	5.5V	18V
HI-8010	3.0V	18.0V	18V
S4520	3.0V	16.0V	17V

As can be seen above, the MIC8030/MIC8031 are superior to both AMI and HOLT in the voltage that can be applied to a Dichroic LCD display. Using the MIC8030/MIC8031 allows for a derating of 50%/70% if operated at 35V; the HI-8010 allows for no derating at 35V and the S4520 allows for no derating at 32V.

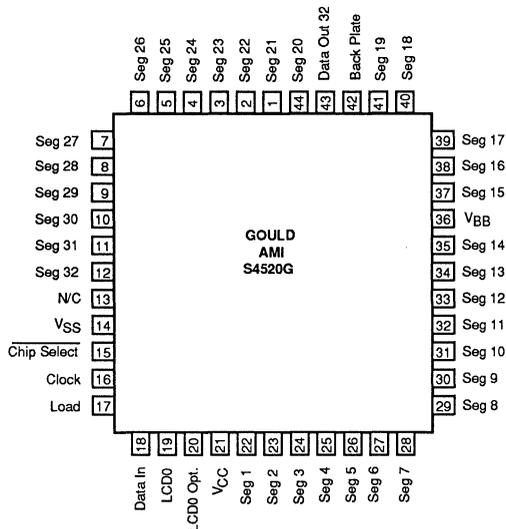
When placing the MIC8030/MIC8031 in a pin compatible configuration on a board which previously used a HOLT or AMI device, care must be taken before changing the polarity of the High Voltage Supply, to reverse the direction of any polarized filter capacitor on the High Voltage line, as well check any other circuit (like a zener diode, etc) which contacts the High Voltage line.

The pin out drawings match the MIC8030/MIC8031 to the S4520. By moving the No-Connect, from pin 41 to pin 13 and shifting the displaced signals clockwise, the pin out can be matched.

Other pin outs that can be matched are the S4520A, S4520B, S4520C, S4520S, S4520F, S4520G, HI-8010L5, HI-8010L6, HI-8010L7, HI-8010C5, HI-8010C6, and the HI-8010C7. Other packaging options are available, all options must use a positive V_{BB}.



**MIC8030/MIC8031
Standard 44 Pin Quad Package**



**S4520G
AMI 44 Pin Quad Package**



General Description

The MM5450 and MM5451 LED display drivers are monolithic MOS IC's fabricated in an N-Channel, metal-gate process. The technology produces low threshold, enhancement mode, and ion-implanted depletion mode devices. These devices are available in packaged or die form, suitable for conventional packaging, hybrid assembly or chip on board technology.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} .

Features

- Continuous brightness control
- Serial data input
- No load signal requirement
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA capability
- Alphanumeric capability
- Available in die or packaged form

Applications

- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Ordering Information

Part Number	Temp. Range	Package
MM5450N	-25 to +85°C	40-pin Plastic DIP
MM5451N	-25 to +85°C	40-pin Plastic DIP
MM5450V	-25 to +85°C	44-pin PLCC
MM5451V	-25 to +85°C	44-pin PLCC
MM5450/51 Die		none

Block Diagram

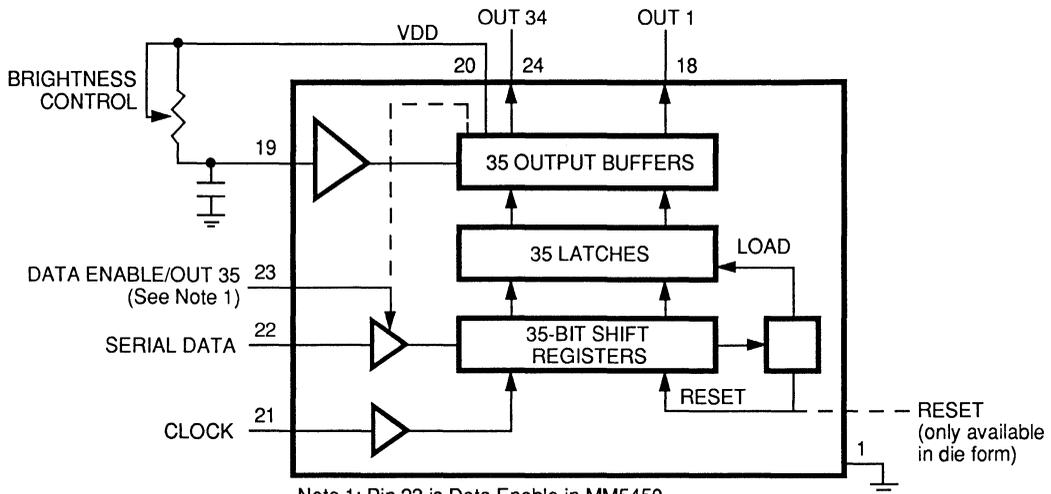
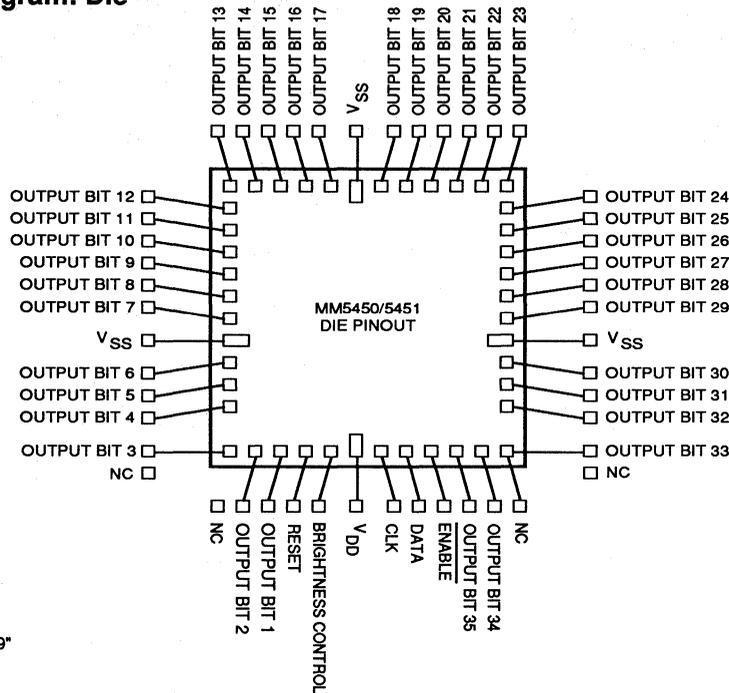


Figure 1.

Connection Diagram: Die



Note: Die size is .106" x .99"

Figure 2.

Connection Diagram: Dual-in-line Package

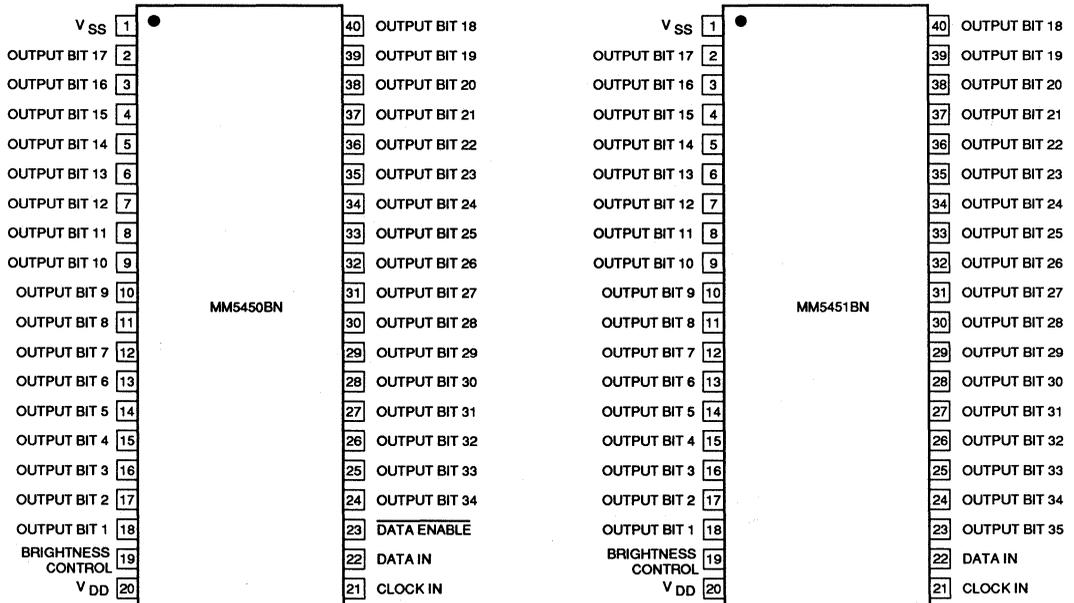


Figure 3a, 3b.

Connection Diagram: Plastic Leaded Chip Carrier

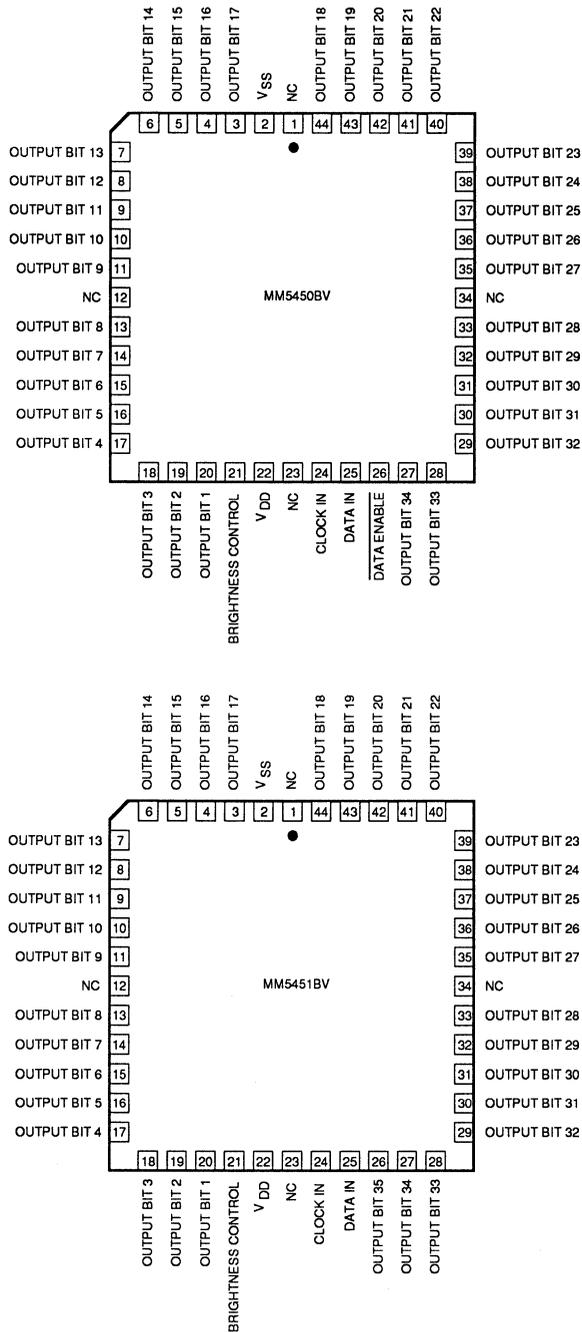


Figure 4a, 4b.

Functional Description

The MM5450 and MM5451 were designed to drive either 4 or 5 digit alphanumeric LED displays with the added benefit of requiring minimal interface with the display or data source.

Data is transferred serially via 2 signals; clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading "1" followed by the allowed 35 data bits. These 35 data bits are latched after the 36th has been transferred. This scheme provides non multiplexed, direct drive to the LED display. Characters currently displayed (thus, data output) changes only if the serial data bits differ from those previously transferred.

Control of the output current for LED displays provides for the display brightness. To prevent oscillations, a 1nF capacitor should be connected to pin 19, brightness control.

The block diagram is shown in Figure 1. For the MIC5450, the DATA ENABLE is a metal option and is used instead of the 35th output. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an external reset connection shown which is available on unpackaged (die) units only.

Figure 2 illustrates the die "pinout", or pad location for bonding in "chip on board" applications.

Figure 5 shows the input data format. A leading "1" is followed by 35 bits of data. After the 36th had been transferred, a LOAD signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. The low side of the clock is used to generate a RESET signal which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 and 4 show the pin-out of the MIC5450 and MIC5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 5 shows the timing relationships between data, clock and DATA ENABLE. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT} . The following equation can be used for calculations.

$$T_j = (V_{OUT}) (I_{LED}) (\text{No. of segments}) (124^\circ\text{C/W}) + T_A$$

where:

$$T_j = \text{junction temperature} + 150^\circ\text{C max}$$

$$V_{OUT} = \text{the voltage at the LED driver outputs}$$

$$I_{LED} = \text{the LED current}$$

$$124^\circ\text{C/W} = \text{thermal resistance of the package}$$

$$T_A = \text{ambient temperature}$$

The above equation was used to plot Figures 7–9.

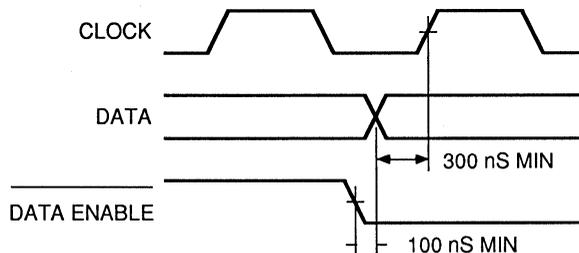


Figure 5.

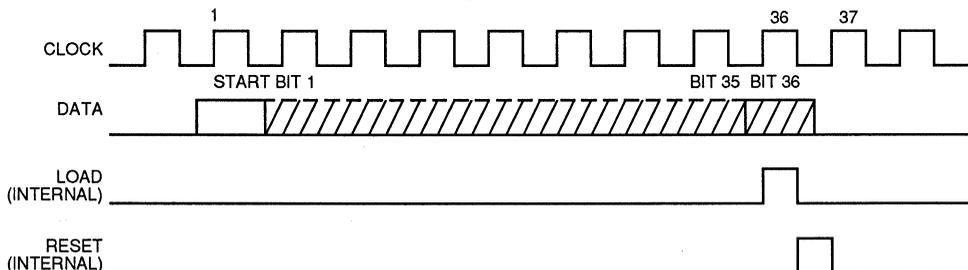


Figure 6. Input Data Format

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+12V$	Junction Temperature	+150°C
Operating Temperature	-25°C to +85°C	Lead Temperature	300°C
Storage Temperature	-65°C to +150°C	(max. soldering time is 10 seconds)	
Power Dissipation	560 mW at +85°C 1 mW at +25°C		

Electrical Characteristics

T_A within operating range, $V_{DD} = 4.5$ V to 11.0 V, $V_{SS} = 0$ V unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			7	mA
Input Voltages					
Logical "0" Level (V_L)	$\pm 10 \mu A$ Input Bias	-0.3		0.8	V
Logical "1" Level (V_H)	$4.75 \leq V_{DD} \leq 5.25$	2.2		V_{DD}	V
	$V_{DD} > 5.25$	$V_{DD} - 2$		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	$V_{OUT} = 3.0$ V			10	μA
Segment ON	$V_{OUT} = 1.0$ V (Note 3)	0		15	mA
	Brightness Input = 0 μA	0		10	μA
	Brightness Input = 100 μA	2.0	2.7	4	mA
	Brightness Input = 740 μA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
Output Matching (Note 1)				± 20	%
Clock input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_H		950			nS
Low Time, t_L		950			nS
Data Input					
Set-Up Time, t_{DS}		300			nS
Hold Time, t_{DH}		300			nS
Data Enable Input Set-up Time, t_{DES}		100			nS
Reset Pad Current (Die Version)		8			μA

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN}) / 2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See Figures 7, 8 and 9 for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See Figures 8 and 9 for allowable V_{OUT} vs. I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ nS, $t_f \leq 20$ nS, $f = 500$ kHz, 50% $\pm 10\%$ duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 nS.

Typical Performance Characteristics

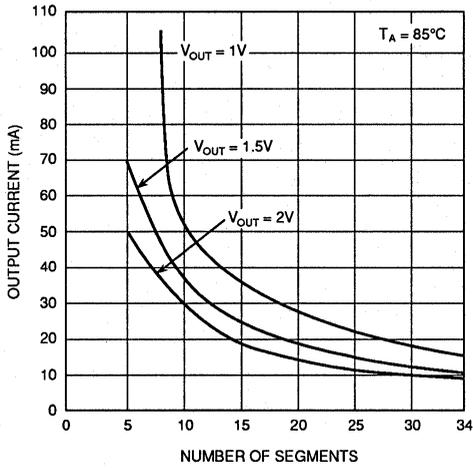


Figure 7.

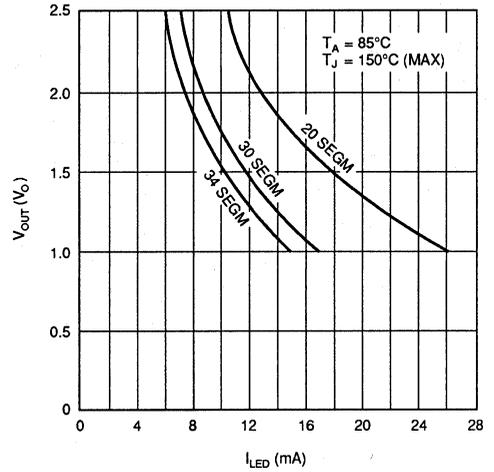


Figure 8.

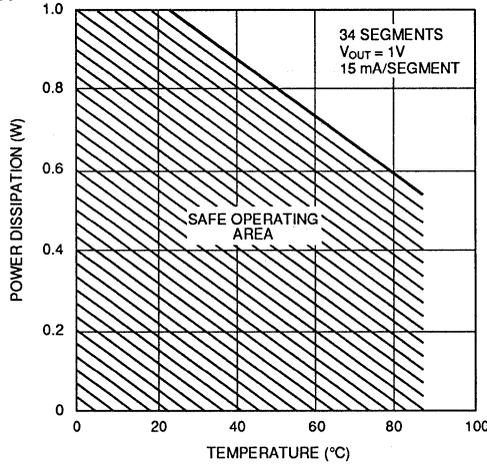


Figure 9.

Typical Applications

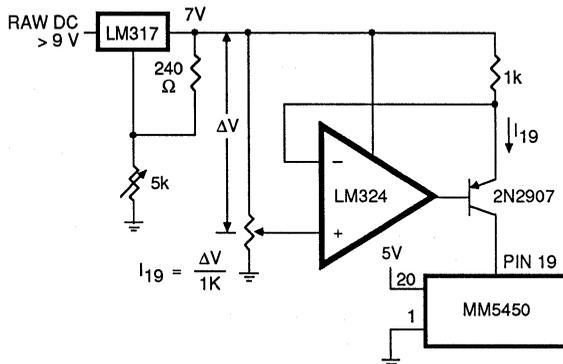


Figure 10. Typical Application of Constant Current Brightness Control

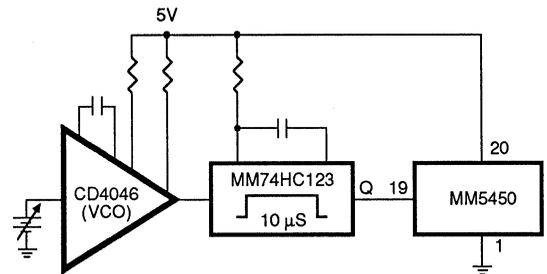


Figure 11. Brightness Control Varying the Duty Cycle

Typical Applications

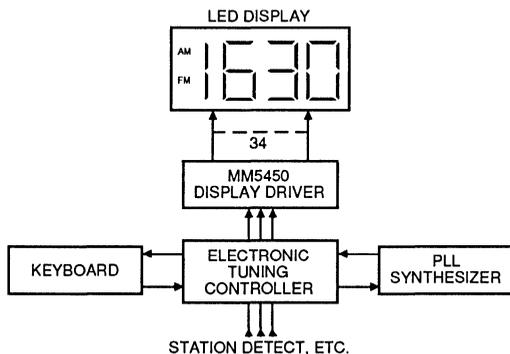


Figure 12. Basic Electronically Tuned Radio System

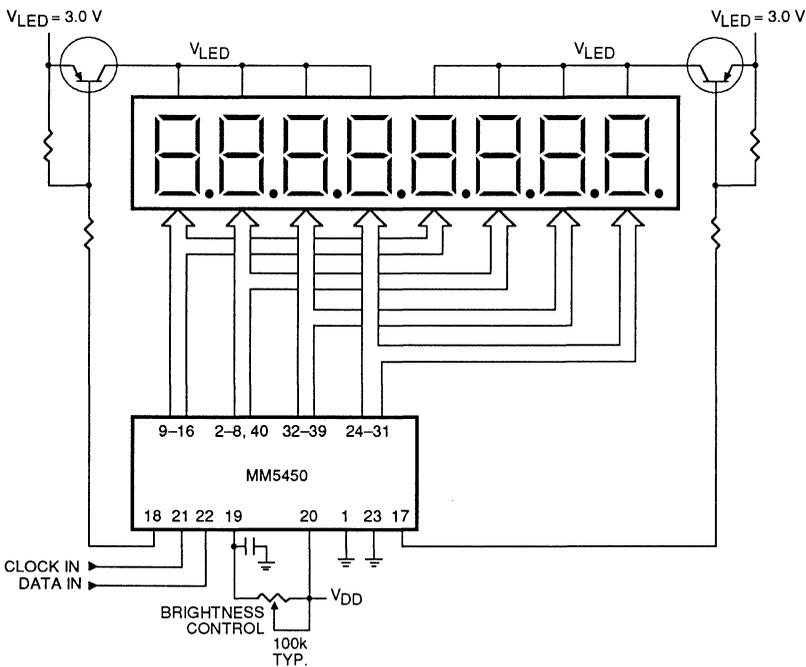


Figure 13. Duplexing 8 Digits with One MM5450.



High Voltage Semicustom Power Array

SECTION 5: HIGH VOLTAGE SEMICUSTOM POWER ARRAY	<u>Page</u>
MPD8020 CMOS/DMOS Semicustom High Power Array	5-2
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MPD8020

CMOS/DMOS SEMICUSTOM

HIGH VOLTAGE ARRAY

CONCEPT

The MPD8020 is a monolithic I.C. semiconductor array of low voltage CMOS analog and digital circuits on the same chip with high voltage DMOS power transistors. For quick turnaround time, wafers are held at the last step (metalization) where the customer's specific metal interconnect pattern makes each wafer run into thousands of custom I.C.'s. These smart power ASIC's (Application Specific I.C.'s) cast in silicon the proprietary advantages of the customer's design even for moderate volume applications, and give the customer a size, reliability and performance advantage over the competition!

GENERAL DESCRIPTION

The MPD8020 CMOS/DMOS Semicustom High Voltage Array uses **Micrel's** proprietary process to combine TTL/CMOS compatible high speed CMOS logic, CMOS analog, and high voltage DMOS power drive circuits on the same monolithic I.C. A single +5 Volt to +15 Volt supply powers the logic and analog circuitry while the high voltage portion functions at voltages of from +20 Volts to +100 Volts. An optional internal voltage pump with the help of two external components generates an extra voltage such that the high side gates of the power N-channel DMOS FET's are driven approximately 15 Volts above the +100 Volt supply allowing rail-to-rail high voltage switching.

The MPD8020 in combination with **Micrel's** CAD systems, CAE simulations (SPICE, HILO, TIMVER, etc.) and an experienced fab and test group give a design engineer a highly versatile means of taking a circuit idea from concept to packaged silicon.

AVAILABLE IN:

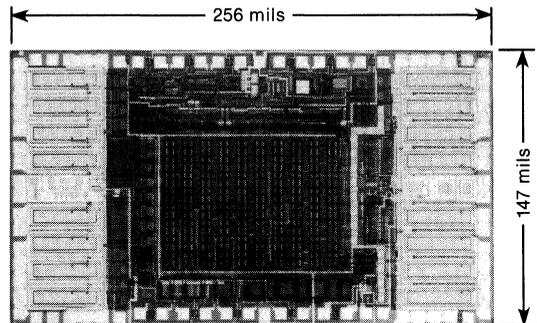
- Chip Form
- 16 to 48 pin plastic DIP's
- 16 to 48 pin ceramic DIP's
- Ceramic LCC's
- Surface mount packages
- PLCC
- Fused lead PLCC and DIP's
- Custom packages

FEATURES

- 16 N-Channel DMOS power FET's (fully floating sources, gates and drains), each 100 V, 200 mA, and 10 ohms.
- DMOS can be paralleled for 100 V, 3.2 Amp, 0.625 ohm single, half bridge, full bridge or bilateral switches.
- 200 CMOS gates in an uncommitted gate array.
- 12 TTL/CMOS I/O buffers.
- 3 op amp / comparator / Schmitt Triggers.
- 1 unity gain analog buffer.
- Bandgap reference (1.25 V / 2.5 V).
- Overtemperature sensor.
- Voltage pump (drives high side gates above V_{DD}).
- 16 medium current sink pre-drivers.
- 16 high voltage level-shifting high side pre-drivers.
- Separate analog and digital ground (V_{SS}) pads.
- Numerous logic I/O, high voltage I/O, V_{CC} and V_{DD} pads.
- Miscellaneous resistors, capacitors, and a zener.
- Available to military temperature range specifications.
- Selection of military, commercial, and power packages.

APPLICATIONS

- Switching regulators
- Motor control
- Bilateral analog switching
- High voltage switching
- Relay and solenoid driver
- Smart switch with bus decode
- Half or full bridge driver
- 3 phase driver
- Lamp driver
- Differential line driver
- Automotive switching
- Printer solenoid driver
- High voltage display driver



MPD8020 CMOS/DMOS/Bipolar Semicustom Array

Protected under Patent Numbers: #4,951,101; #4,979,001

MPD8020 MACRO CELL MENU

- 16 fully floating 100 V, 200 mA, 10 ohm Vertical-DMOS FET's
- 16 high voltage 100 V P and N channel level shifters (made up of 32 cross coupled 20 to 50 mA P & N channel pairs)
- 200 CMOS gates in an uncommitted gate array
 - over 30 pre-designed logic "templates" of shift registers, decoders, flip-flops, NAND gates, NOR gates, etc.
 - general purpose op amps, comparators and Schmitt Triggers, implemented in the gate array
- 12 TTL/CMOS I/O buffers
- 16 logic predrivers (with logic enable) for bottom side DMOS drive
- 3 configurable op amp / comparator / Schmitt Trigger cells which can be hooked-up as:
 - ground sensing or V_{CC} sensing amplifiers or comparators
 - folded cascode high performance amplifiers
 - NPN input amplifiers
 - programmable bandwidth / power consumption amplifiers
- A unity gain buffer with adaptive bias (to drive large loads with minimum quiescent current)
- A bandgap reference with a 1.25 V output plus multiple programmable outputs up to V_{CC}
- An over-temperature protection circuit with programmable temperature trip points and hysteresis
- A master bias programming circuit for all the linears
- A high voltage V_{++} "doubler" for N-channel gate drive above the +100 V V_{DD} rail
- A low voltage (V_{CC}) pass regulator to drive a local low voltage analog and digital power supply from the high voltage supply
- Multiple current mirrors both at high (100 V) and low (15 V) levels
- Floating zener clamps, avalanche zeners, references and Schottky diodes
- Diffusion, diffusion P-well, pinched and poly resistors
- 40 picofarads of on-chip capacitance
- Isolated PNP and NPN transistors

What MICREL Supplies with the MPD8020

- MPD8020 CMOS/DMOS Semicustom High Voltage Array Data Sheet
- MPD8020 Kit Part #1, Analog SSI and MSI Circuits
 - Kit parts in a 40 pin DIP with eleven commonly used analog circuits
 - Kit Part #1 data sheet with specifications and application hints
- MPD8020 Kit Part #2, Digital SSI and MSI Circuits
 - Kit parts in a 40 pin DIP with eight revealing digital circuits for checking speed and digital timing characteristics (also some analog circuits implemented in the gate array)
 - Kit Part #2 data sheet with specifications and application hints
- Highly experienced design and applications engineers on call to discuss how to optimize putting a complex analog, digital, and power circuit on one I.C.

What MICREL Needs from You — the Designer

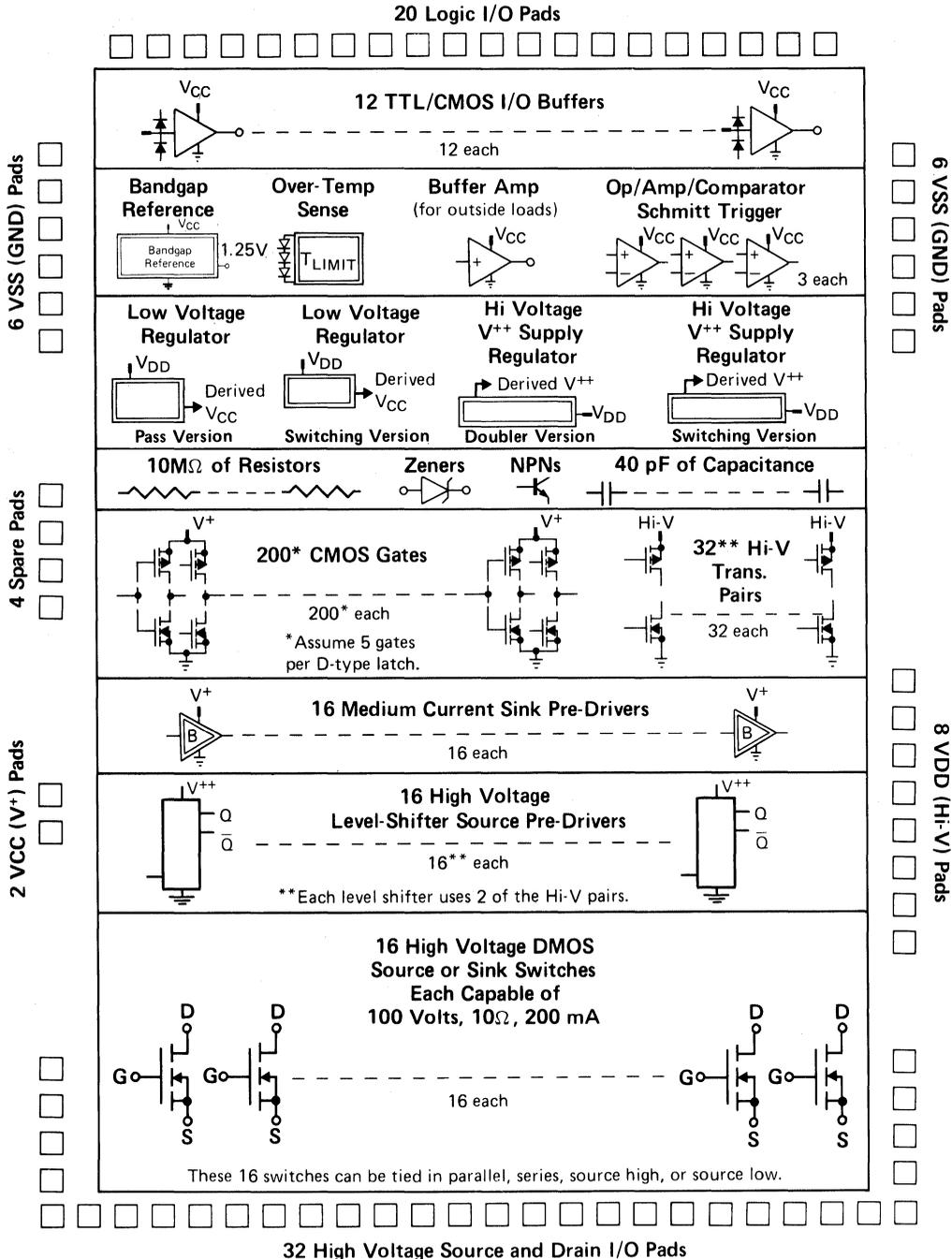
- System block diagram with basic I/O specifications, or
- Schematic of circuit implemented with analog, digital and discrete power transistors plus the I/O specifications, or
- Breadboard using our kit parts plus "glue" logic and I/O specifications, or
- Spice and Hi-Low netlists or any other compatible computer generated description and I/O specifications.

Typical Semicustom Design Cycle Following Exploratory Discussions and Contract Initiation

Week	Action
1	Design & Customer Interface
2	Design & Customer Interface
3	Electrical & Layout Computerized Checks
4	Mask Generation
5	Mask Generation
6	Apply ASIC Masks to Preprocessed Wafers
7	Wafer Test
8	Package Test Units
9	Final Test, QA & Ship 25 Units

DETAILED COMPONENT

AND PAD LISTING: This diagram lists the components available to the designer for laying out an MPD8020 semicustom circuit. The I/O pads shown around the periphery represent the total number available; all pads are not normally used in a given circuit/package combination.



MPD8020 ELECTRICAL SPECIFICATIONS

MPD8020 SPECIFICATIONS AND MASK PROGRAMMABILITY

The MPD8020 is a highly versatile mask programmable semicustom chip and the electrical specifications of the predesigned macros cannot be fully specified for all possible bias currents and all possible transistor combinations. For example, the linear block op amp will exhibit different gain bandwidth, slewrate, and input voltage capabilities, depending on the transistors used and the bias current into the current mirrors. The hysteresis and trip points of the overtemperature protection macro and the Schmitt trigger similarly are a function of what the designer specifies in the I/O parameters.

The following specifications are examples of how the MPD8020 can function, but should not be considered the final word on performance specifications.

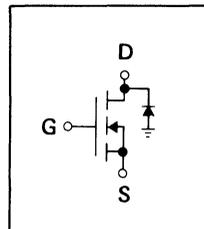
Greater speed, lower offsets, different operating ranges are all available by making engineering tradeoffs and by exercising design options.

Absolute Maximum Ratings

Storage Temperature	Ts	-65 to +150°C
Operating Temp	Ta	MIC8020 0 to +70°C
		MIC8020M -55 to +125°C
DC Input Voltage		 -0.5 to Vdd
	(any input pin to Vss)	 +0.5 Volts
Vcc Supply Voltage		 18 Volts
Drain-Source Voltage	Bvdss	 110 Volts
Drain-Gate Voltage	Bvdgr, Rgs=20K-ohm	 110 Volts
Continuous Drain Current per output	Id	 200mA
Pulsed Drain Current per outlet Gate-Source Voltage	Ip	 500mA
	Vgs	 +/-20 Volts

N-CHANNEL DMOS POWER FET'S

The 16 DMOS power FET's are fully floating between ground and Vdd. Normally a 35V gate-to-source protection diode is inserted to protect the gate from excessive transients. Each DMOS FET may be tied to Vdd, ground, or in between. Paralleling 2 or more DMOS FET's reduces the "ON" resistance and increases the current handling capability in a ratio directly proportional to the number of FET's used.



Electrical characteristics @ Vss=0V T =25°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 BV _{DSS, DRAIN}	V _{in} = 0V; I _D = 100μA	100			V
2 I _D (continuous)	V _{in} = 15V; V _{out} ≤ 2V	200			mA
3 I _D (pulse)	V _{in} = 15V; V _{out} ≤ 8V (note 1)	500			mA
4 R _{DS} (15V)	V _{in} = 15V; I _D = 100mA (note 1)		8	14	ohm
5 R _{DS} (10V)	V _{in} = 10V; I _D = 100mA (note 1)		9	24	ohm
6 I _{DSS}	V _{in} = 0V; T _j = 125°C, V _{DS} = 100V		100	1000	μA
7 V _{th}	I _D = 1mA; V _{DS} = V _{GS}		3	5	V
8 V _{DS} (on)	I _D = 100mA; V _{in} = 15V (note 1)			1.4	V
9 C _{iss}	(note 2)		35	60	pF
10 t _d (on)	(notes 1 & 3); V _{in} = 0V, 15V; R _s = 50 ohm		33	40	ns
11 t _r (off)	(notes 1 & 3); V _{in} = 0V, 15V; R _s = 50 ohm		50	70	ns
12 I _{in}	V _{in} = 0V or V _{in} = 15V		1	10	μA

Note 1—Pulse test; pulswidth ≤ 300μs, duty cycle ≤ 2%

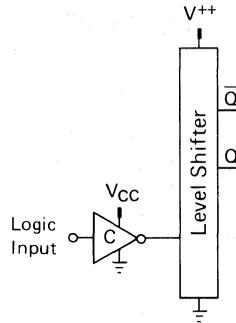
Note 2—Guaranteed by design, but not tested on a production basis.

Note 3—R_L = 1000 ohm non-inductive 10W resistor to 100V supply; measured from 50% of input to 50% of output.

HIGH VOLTAGE LEVEL SHIFTERS

The 16 possible level shifters are each made up of 2 N-channel and 2 P-channel high voltage, thick gate oxide (capable of withstanding the full V^{++} supply in either direction), transistors connected in 2 cross coupled pairs. Multiple level shifters or augmented outputs may be metalized-in for greater drive capability.

The 64 high voltage CMOS transistors (used in the level shifters) are also available in uncommitted form for high voltage logic and use as switching and pass devices for voltage regulators.



Electrical characteristics @ $V_{SS}=0V$, $V_{CC}=15V$, $V_{DD}=100V$, 1 open source DMOS connected to the \bar{Q} output, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 $BV_{DSS, DRAIN}$	$V_{in} = 0V$; $I_D = 100\mu A$	100			V
2 $V_{in, low}$	$ I_{in} \leq 1mA @ V_{out} = 100V$		7.8	2.5	V
3 $V_{in, high}$	$I_D = 100mA$; (note 1)	12.5	7.6		V
4 $t_d (on)$	(notes 1 & 2); $R_s = 50 \text{ ohms}$		37	65	ns
5 $t_f (off)$	(notes 1 & 2); $R_s = 50 \text{ ohms}$		35	60	ns

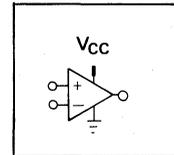
Note 1—Pulse test; pulsewidth $\leq 300\mu S$, duty cycle $\leq 2\%$

Note 2— $R_L = 700 \text{ ohm}$ non-inductive 10W resistor to a 70V supply; measured from 50% of input to 50% of output.

GROUND SENSING OP AMP FROM A LINEAR MACRO

A configurable linear gain macro metalized as an op amp with P-channel MOS transistors in the input is capable of sensing linear signals down to (and approximately 300 millivolts below) ground. The gain, bandwidth, slewrate, etc. are functions of the master bias current fed to the op amp. The following specifications are one snapshot of the op amp at the bias and voltage shown below.

Other op amp options include NPN bipolar inputs, N-channel MOSFET inputs, and lighter frequency compensation.



All of the linear macro implementations, with the exception of the linear buffer, are intended to drive light loads (i.e. another op amp, a comparator, a gate, etc.) and so they are tested with high impedance loads on the order of a megaohm. Gain degradation should be expected at loads of 100K ohms or less.

Electrical characteristics @ $V_{SS}=0V$, $V_{CC}=15V$, $R_{bias}=390K \text{ Ohms}$, $T_a=25^\circ C$ unless otherwise specified.

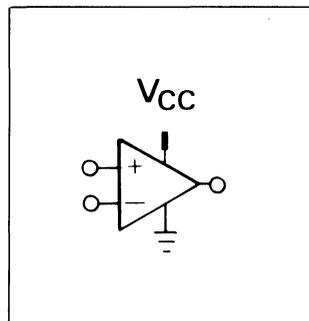
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 $V_{in, Range}$		-0.3		13.5	V
2 $ V_{OS} $	$V_{in, common mode} = 7.5V$		2.7	30	mV
3 $V_{out, Swing}$	$R_L = 1M \text{ ohm}$	0.2		13.0	V
4 AV_{OL}	$V_{in, common mode} = 7.5V$	1.5	25		V/mV
5 CMRR	$V_{in} = 5V, 10V$	40	88		dB
6 PSRR	$V_{CC} = 14V, 15V$	50	88		dB
7 Slew Rate	$V_{REF} = 7.5V, V_{in} = 7V, 8V$		3		V/ μs
8 Bandwidth	-3dB small signal unity gain		4		MHz
9 $ I_{in} $	$V_{in, common mode} = 7.5V$			1.0	μA

GROUND SENSING COMPARATOR FROM A LINEAR MACRO

A linear macro, configured as a comparator with ground sensing inputs, has P-channel MOS inputs and like the ground sensing op amp can accept signals down to approximately 300 millivolts below ground. The gain and response speed are a function of the bias and supply voltage. The following specifications are one snapshot of the comparator at the bias and voltage shown below.

Other comparator options include NPN bipolar inputs, N-channel MOSFET inputs, and higher bias for increased accuracy, higher input voltage range, and speed respectively.

All of the linear macros, with the exception of the linear buffer, are intended to drive light loads (i.e. op amps, gates, etc.) and so are tested with high impedance loads on the order of a megaohm. Gain degradation should be expected at loads of 100K ohms or less.



Electrical characteristics @ $V_{SS}=0V$, $V_{CC}=15V$, $R_{BIAS}=390K$ Ohms, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{in} Range		-0.3		13.5	V
2 $ V_{OS} $	$V_{in \text{ common mode}} = 7.5V$		2.5	30	mV
3 CMRR	$V_{in \text{ common mode}} = 5V, 10V$	60	65		dB
4 PSRR	$V_{CC} = 14V, 15V$; $V_{in \text{ common mode}} = 7.5V$	50	53		dB
5 AV_{OL}	$V_{in \text{ common mode}} = 7.5V$	1.5	10		V/mV
6 V_{OH}	$R_L = 1M$ ohms to ground	13.4	14.8		V
7 V_{OL}	$R_L = 1M$ ohms to ground		0.01	0.5	V
8 Response, TTL	$V_{REF} = 1.4V$; $V_{in} = 0.8, 2.0V$; note 1, note 2		290	300	ns
9 Response, 110mV	$V_{REF} = 1.4V$; $V_{in} = 1.345V, 1.455V$; note 1, note 2		750	900	ns
10 $ I_{in} $	$V_{in \text{ common mode}} = 7.5V$			1.0	μA

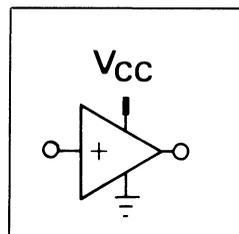
Note 1—Measured from 50% of input to 50% of output.

Note 2— $R_{BIAS} = 56K$ ohms; decreasing R_{BIAS} increases the speed. Chip designs allow changing current mirror ratios to improve speed while leaving R_{BIAS} unchanged.

UNITY GAIN BUFFER

The unity gain buffer provides a relatively high current linear element for driving analog signals off of the chip.

For increased accuracy the buffer is normally included in the loop with another linear macro or one of the gate array implementations of an op amp.

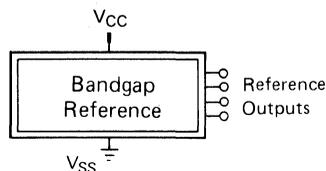


Electrical characteristics @ $V_{ss}=0V$, $V_{cc}=15V$, $R_{bias}=390K$ Ohms, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 Voltage Gain	$V_{in} = 7.5V$	0.9		1.2	V/V
2 V_{out} Range	$R_L = 2M$ ohms to ground	1.5		13.5	V
3 V_{out} Swing	$R_L = 2K$ ohms to ground	2.5		12.5	V
4 Slew Rate	$V_{in} = 1.5V$ to $13.5V$		280		$V/\mu S$
5 $ I_{in} $	$V_{in} = 7.5V$			1.0	μA

BANDGAP REFERENCE

The bandgap reference supplies a low drift reference voltage for the overtemperature, overvoltage, overcurrent, and linear comparison functions of the chip. The basic output is approximately 1.25V with ratioed voltage taps available from a resistor chain extending up to close to V_{cc} . Popular taps include 2.5V, 5V, 10V, etc., but the additional output need not be restricted to integer multiples of 1.25V.



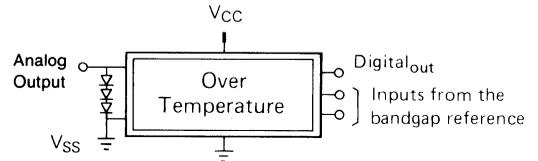
Electrical characteristics @ $V_{ss}=0V$, $V_{cc}=15V$, $I_{bias}=3.5\mu A$, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{out}			1.21	1.35	V
2 V_{out} average T.C.	$-55^\circ C \leq T_j \leq 125^\circ C$		300		ppm/ $^\circ C$

OVERTEMPERATURE DETECTION CIRCUIT

The overtemperature detector senses the temperature of the chip and reacts with a digital "1" output when the chip exceeds a predetermined temperature (+125°C in the example below). Built-in hysteresis prevents the circuit from resetting until the chip passes a preset lower trip point (+85°C in this example) thereby inhibiting thermal oscillations.

Both trip points are mask programmable from the output of the bandgap reference.



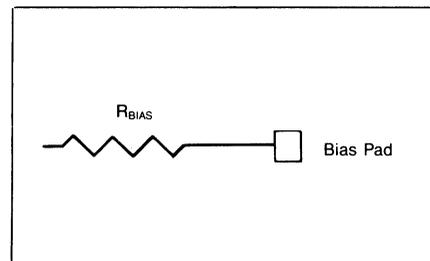
Electrical characteristics @ $V_{ss}=0V$, $V_{cc}=15V$, $R_{bias}= 390K$ Ohms, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1 V_{out} Digital	$T_j = 125^\circ C$	14.5	14.94		V
2 V_{out} Analog	$T_j = 25^\circ C$, $I_{out} = 1\mu A$		1.8	2.2	V
3 V_{out} Analog T.C.	$-55^\circ C \leq T_j \leq +155^\circ C$, $I_{out} = 10\mu A$		6.7		mV/ $^\circ C$
4 V_{out} Digital	Low temperature $T_j < +85^\circ C$		0.006	0.5	V
5 V_{out} Digital	Temp decreasing $+85^\circ C < T_j < +125^\circ C$	14.5	14.94		V
6 V_{out} Digital	Temp increasing $+85^\circ C < T_j < +125^\circ C$		0.006	0.5	V

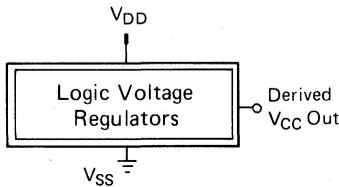
BIAS

A single bias resistor (or current source) is used to program all of the current mirrors used in the linear portions of the chip. The same current is also used to determine the operating point of linear op amps, and comparators, imprinted on the gate array. Typical bias configurations call for a resistor tied from V_{cc} to the bias pin (which would be one N-channel MOS threshold above ground) or alternatively the resistor is tied from ground to the bias pin (which in that case would be one P-channel MOS threshold below V_{cc}).

The master bias input allows programming of the speed, bandwidth, output driver, and power dissipation of most of the analog functions on the chip.

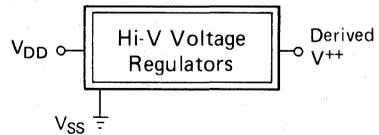


INTERNAL VOLTAGE REGULATORS



Internal regulators can generate local low level digital/analog voltages (Vcc) from a single Vdd high voltage supply of 20 Volts to 100 Volts or extra high (V++) voltages above Vdd.

Low Voltage digital/analog Vcc voltage is normally derived using a pass regulator for low current requirements. A switching regulator using an inductor is used when current requirements are high and input/output voltage differentials are large.

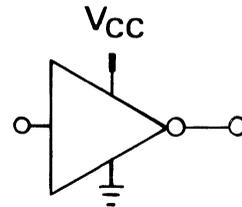


Extra high voltage (V++) is normally derived using a voltage “doubler.” V++ is needed to power the level shifters used to pull the N-channel DMOS gates above Vdd. An external clamping zener diode holds V++ at 15V to 20V above Vdd (for Vdd ≥ 20V). This zener diode gives over voltage protection to the level shifters, while holding V++ at 18V to 20V above Vdd.

This is sufficient to insure “rail-to-rail” switching of DMOS power FET’s. For cases requiring higher efficiency, V++ can be derived using an inductor in a switching regulator.

TTL/CMOS INPUT/OUTPUT BUFFERS

The 12 TTL/CMOS I/O buffers accept TTL and CMOS logic level input signals and are capable of driving offchip TTL or CMOS gates and buses.



Electrical characteristics @ Vss=0V, Ta=25°C unless otherwise specified.

PARAMETER	CONDITIONS	Vcc = 15V			Vcc = 5V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
1 V _{IH}		12.5	7.6		2.0	1.5		V
2 V _{IL}			7.4	2.5		1.3	0.8	V
3 V _{OH}	I _o = 10 μA	13.5	14.9		4.5	4.99		V
4 V _{OL}	I _o = 10 μA		.01	1.5		.005	0.5	V
5 I _{in}				1			1	μA
6 I _{OH}	V _{out} = V _{IH} min	2	24		0.4	15		mA
7 I _{OL}	V _{out} = V _{IL} max	13	40		6	7.7		mA
8 C _{in}			7.5			7.5		pF
9 t _{PLH}	C _L = 15pF to gnd		55	100		55	150	nS
10 t _{PHL}	C _L = 15pF to gnd		55	100		55	150	nS

DIGITAL GATE ARRAY

The 200 gates which make up the digital gate array are two input logic elements. Each gate's 2 P-channel and 2 N-channel transistors are floating and can be used to make up transmission gates, op amps, comparators, Schmitt triggers and so forth.

Pre-designed digital macros for the gate array include NAND gates, NOR gates, flip-flops, decoders, latches, shift registers, counter, etc. Essentially any 74XX, 74CXX, or 4000 series digital function of reasonable

size can be imprinted on the array. Extensive underpasses and logic highways are present to optimize utilization of the array.

The following table shows some of the gate delays low-to-high and high-to-low for various implementations of NAND and NOR gates. NOR gates with their use of stacked slow P-channel FET's are slower than NAND gates which use paralleled P-channel's to accomplish this logic function.

Electrical characteristics @ $V_{SS}=0V$, $T_a=25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	$V_{CC} = 15V$			$V_{CC} = 5V$			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
1 V_{OH}	$V_{in} = V_{IH}$	13.5	7.6		4.5	1.5		V
2 V_{OL}	$V_{in} = V_{IL}$		7.4	1.5		1.3	0.5	V
3 $ I_{in} $	$V_{in} = V_{CC}$			1			1	μA
4 t_{PLH} Inverter	(note 1)		1.4			3.5		ns
5 t_{PLH} 2input NAND	(note 1)		1.4			4.1		ns
6 t_{PLH} 4input NAND	(note 1)		2.2			6.0		ns
7 t_{PLH} 2input NOR	(note 1)		2.0			6.3		ns
8 t_{PLH} 4input NOR	(note 1)		6.3			19.0		ns
9 t_{PHL} — inverter	(note 1)		0.5			1.0		ns
10 t_{PHL} 2input NAND	(note 1)		0.6			1.8		ns
11 t_{PHL} 4input NAND	(note 1)		2.5			8.4		ns
12 t_{PHL} 2input NOR	(note 1)		0.5			1.0		ns
13 t_{PHL} 4input NOR	(note 1)		0.6			2.8		ns
14 f_{osc}	Nine gate. Free running ring oscillator		50			20		MHz

Note 1—Delay time is measured from 50% point of input to 50% point of output.

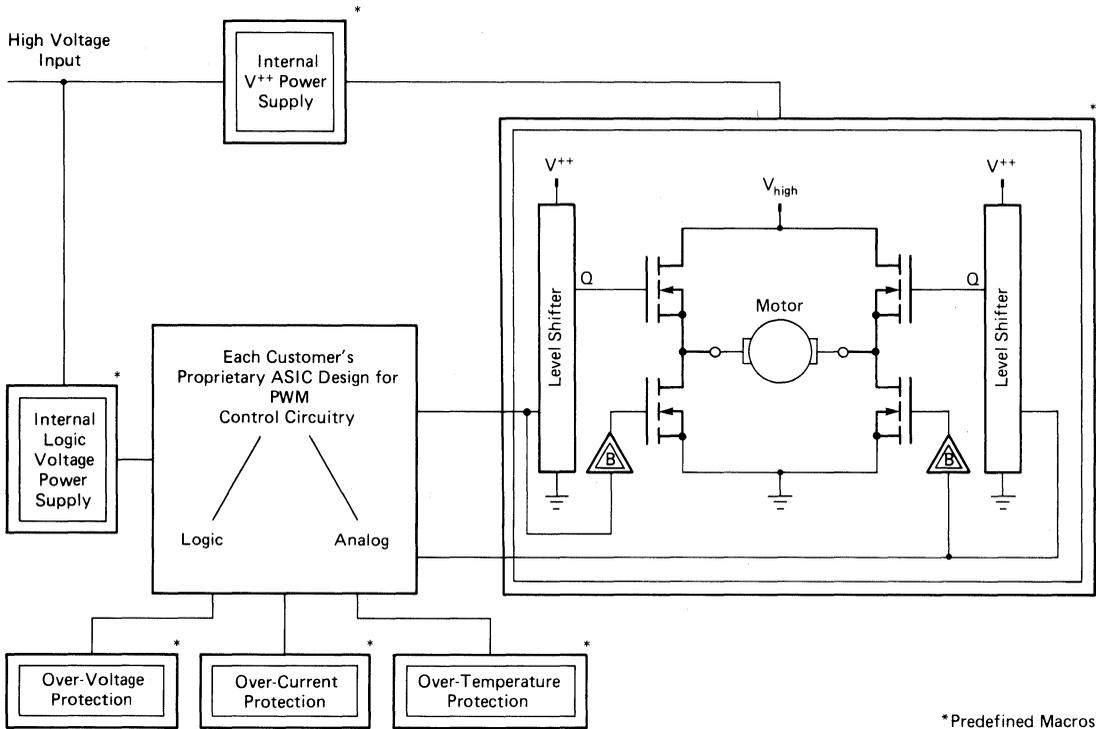
ZENERS, RESISTORS, AND CAPACITORS

The array contains a large number of zener diodes with 35V, 10V, and 6V breakdowns. In addition there are polysilicon resistors for the 0.1 ohm to 1K ohm range, p-plus resistors for the 1K ohm to 10K ohm range, and p-well resistors for the 10K ohm to 1M ohm range. Each of the linear gain blocks plus the buffer

amplifier and the bandgap reference contain capacitors (which are available if a particular circuit is not used) and in addition the innate capacitance of diodes and zener diode can be used for implementing delay and AC coupling functions.

MPD8020 APPLICATION EXAMPLES

MOTOR CONTROL APPLICATION



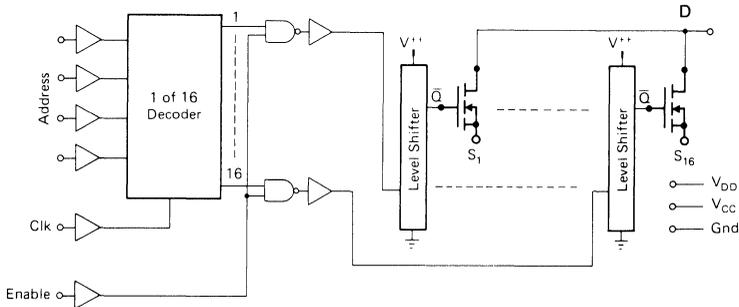
*Predefined Macros

The above motor control application shows how a mixture of predefined macros and customer proprietary ASIC control circuits are used to make a circuit optimally fit an application. Each transistor in the bridge can be a single DMOS FET, or 2 to 4

FET's in parallel for added current capability. Three phase motor control simply requires an additional level shifter and buffer driver. Since there are 16 DMOS FET's, 16 level shifters and sixteen drivers, a large number of drive combinations are possible.

DECODER DRIVER APPLICATIONS

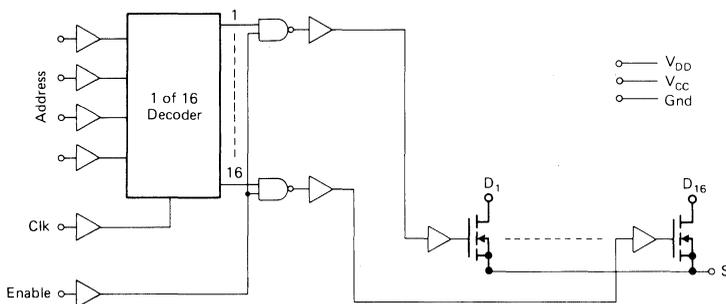
1 of 16 HIGH SIDE DECODER-DRIVER APPLICATION



COMMON DRAIN VERSION

- 4 bit address input
- 16 outputs of 200 mA (500mA pulse) each at up to 100 Volts
- Enable input for multichip systems
- Optional over-temperature, over-current and over-voltage sensing

1 of 16 CURRENT SINKING DECODER-DRIVER APPLICATION



COMMON SOURCE VERSION

- 4 bit address input
- 16 outputs of 200 mA (500mA pulse) each at up to 100 Volts
- Enable input for multichip systems
- Optional over-temperature, over-current and over-voltage sensing

Common drain and common source decoder drivers can be run as 1 of 16 as shown above or the DMOS outputs can be paralleled for greater output current capability.

MPD8020 KIT PARTS

Micrel offers two kit parts for use in developing ASIC designs on the MPD8020 CMOS/DMOS/Bipolar semicustom array.

MPD8020-KIT PART # 1 ANALOG SSI AND MSI CIRCUITS APPLIED TO THE MPD8020

PURPOSE

Kit Part #1 demonstrates the operation of several of the analog SSI and MSI circuits which can be implemented on the MPD8020 CMOS/DMOS Semicustom High Voltage Array. This kit part offers the designer the opportunity to see one set of characteristics of the array. Since all of the op amps, comparators, power DMOS FET's, bandgap, Schmitt Trigger, and digital circuits are configurable, parameters such as gain, offset, drive current, temperature settings, etc. can be changed and in fact optimized for each designer's application. This kit part shows the performance of several of the analog circuits plus some of the digital circuits in one of their many configurations.

DESCRIPTION

The metal and contact masks which define Kit Part #1 were applied to the MPD8020 CMOS/DMOS Semicustom High Voltage Array such that eleven analog circuits are available. These circuits are:

1. Comparator, with ground sensing inputs
2. Op Amp, with ground sensing inputs
3. Unity gain buffer
4. Over Temperature detector circuit
5. Pass version of a local Vcc voltage regulator (dropped from Vdd)
6. Voltage "doubler" for V++ (above Vdd)
7. Open drain DMOS FET (10 Ohm) with direct gate access
8. Open drain DMOS FET (10 Ohm) with logic input
9. Open source DMOS FET (10 Ohm) with high voltage level shifter
10. Bandgap reference
11. Pulse width modulator "H" Bridge (3.3 Ohm) with steering and enable

MPD8020-KIT PART # 2 ANALOG SSI AND MSI CIRCUITS APPLIED TO THE MPD8020 (PLUS GATE ARRAY LINEAR CIRCUITS)

PURPOSE

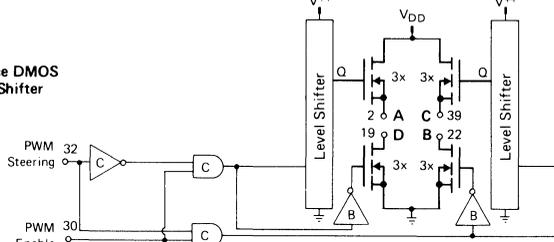
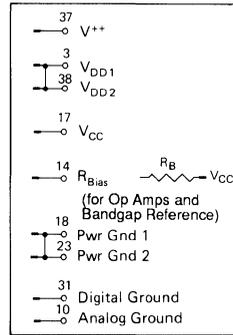
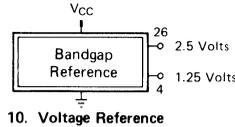
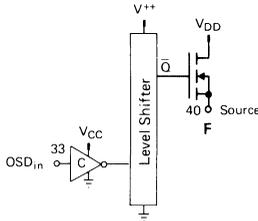
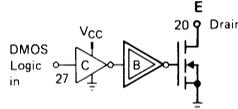
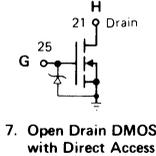
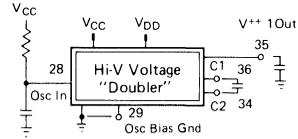
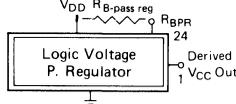
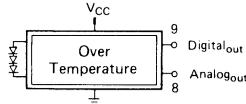
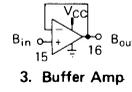
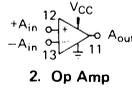
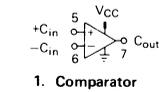
Kit Part #2 demonstrates the operation of several of the digital SSI and MSI circuits which can be implemented on the MPD8020 CMOS/DMOS Semicustom High Voltage Array. This kit part offers the designer the opportunity to see actual gate delays, shift register speeds, ring counter operation, etc. versus supply voltage and temperature. Analog circuits imposed on the digital array are explored using a transmission gate/analog switch, comparator, Schmitt Trigger, and op amps. This kit part shows a few of the myriad of digital (and analog) macros which can be implemented in the digital array. Any 74C or 4000 series logic function or set of functions taking up fewer than 200 gates can be put on the gate array.

DESCRIPTION

The metal and contact masks which define Kit Part #2 were applied to the MPD8020 CMOS/DMOS Semicustom High Voltage Array such that eight digital circuits are available. These circuits are:

1. 4-bit parallel output shift register plus a shift by sixteen output
2. Ring oscillator and gate timing check circuits
3. TTL compatible flip-flop
4. Comparator (built from gate array transistors)
5. Schmitt Trigger (built from gate array transistors)
6. Op Amp (built from gate array transistors) and the unity gain buffer
7. Op Amp (1 of the 3 configurable macros) with NPN bipolar input transistors
8. Transmission-gate/analog-switch

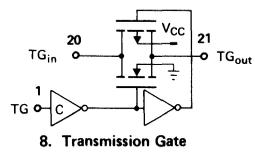
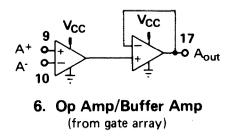
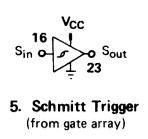
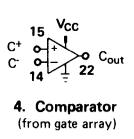
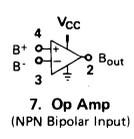
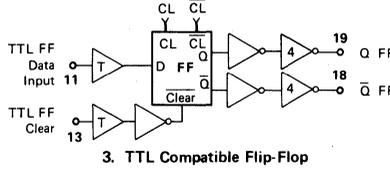
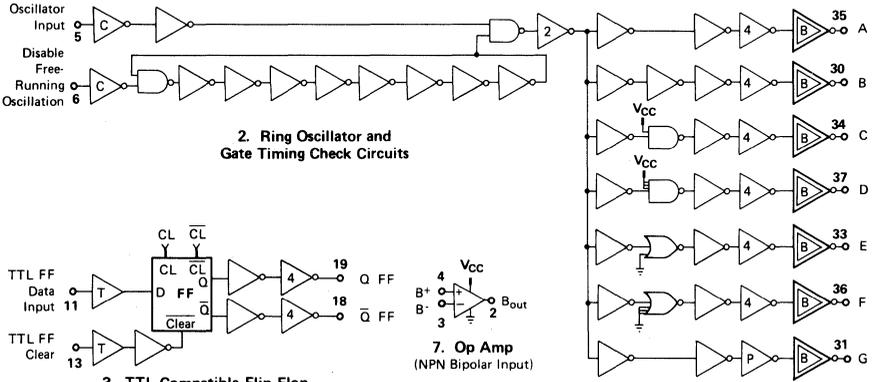
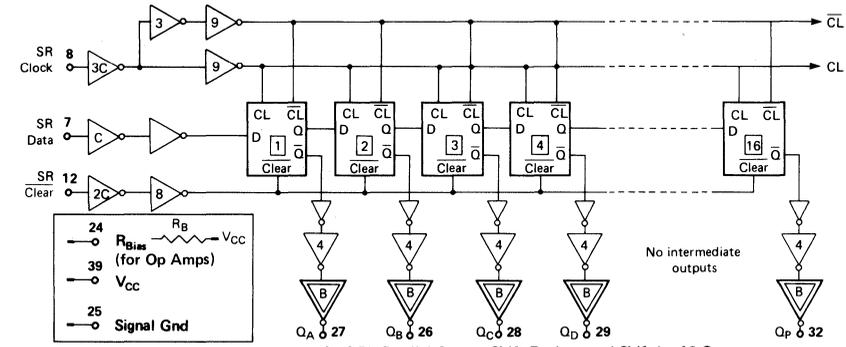
**MPD8020 KIT PART #1
ANALOG SSI AND MSI CIRCUIT OVERVIEWS**



Vcc out Pass Reg	1	40	F
A	2	39	C
Vdd 1	3	38	Vdd 2
1.25 Volts	4	37	V++
+Cin	5	36	C1
-Cin	6	35	V++ 1 out
Cout	7	34	C2
T Sense Analog out	8	33	O.S.D. in
T Sense Digital out	9	32	PWM Steering
Analog Ground	10	31	Digital Ground
Amp out	11	30	PWM Enable
+ Amp in	12	29	Osc Bias Gnd
- Amp in	13	28	Osc in
RBIAS (Op Amps)	14	27	DMOS Logic in
Buffer in	15	26	2.5 Volts
Buffer out	16	25	G (DMOS Gate)
Vcc	17	24	R bias of Pass Reg
Power Gnd 1	18	23	Pwr Gnd 2
D	19	22	B
E	20	21	H

**Kit Part #1 Pin-out
TOP VIEW**

MPD8020 KIT PART #2 DIGITAL SSI AND MSI CIRCUITS OVERVIEWS



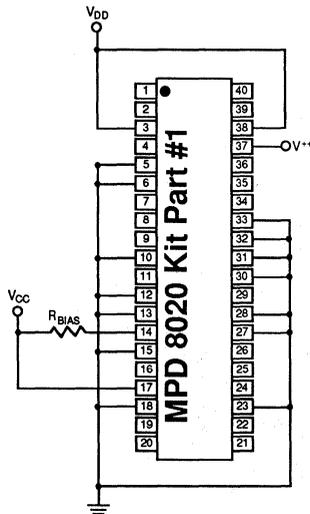
TG (Trans'n Gate Logic) 1	MPD8020 Kit Part #2	40	N/C
B Out 2		39	VCC
B- 3		38	N/C
B+ 4		37	D
Oscillator in 5		36	F
Disable Free Running 6		35	A
S R Data in 7		34	C
S R Clock 8		33	E
A+ 9		32	QP
A- 10		31	G
TTL FF Data in 11		30	B
S R Clear 12		29	QD
TTL FF Clear 13		28	QC
C- 14		27	QA
C+ 15		26	QB
Schmitt in 16		25	Singal Gnd (VSS)
A out 17		24	RBias (For Op Amps)
TTL Q 18		23	Schmitt Out
TTL Q 19		22	C Out
Trans'n Gate in 20		21	Trans'n Gate Out

Kit Part #2 Pin-out TOP VIEW

Application Hints KP1

Unused Inputs

Unused inputs should be tied together to V_{CC} or ground, specifically pins 5, 6, 12, 13, 15, 27, 28, 30, 32, and 33; not doing so can cause excessive and/or variable I_{CC} current. R_{BIAS} (pin 14) and oscillator bias ground (pin 29) should be left floating when not in use.



**Unused
Input Pins
KP1**

Analog Circuits

The analog circuits i.e. (the comparator, op amp, buffer amp, and the over temperature detection circuit) all require that pin 10 (analog ground) is grounded, and pin 14 (R_{BIAS}) is connected through a bias resistor (usually 390 k Ω) to V_{CC} .

The buffer amp is designed to be used in the loop with either the op amp or the comparator to drive analog signals off the chip; any offset associated with the buffer amp will be divided by the gain of the previous stage. Suitable frequency compensation for loop stability should be employed. The gain, slewrate, output drive capability, and bandwidth of the linears may be adjusted by changing R_{BIAS} (and therefore I_{BIAS}).

The true rise and fall times on the comparator are about 50nS when driving an on chip load such as a gate (0.5 pF), when $V_{CC} = 15V$ and $R_{BIAS} = 390 k\Omega$. If this comparator is used to drive an off chip load, the rise and fall times will be much larger due

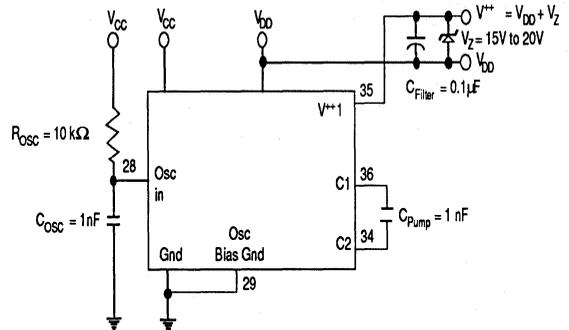
to capacitive loading and the other effects. With a scope probe on the output, the capacitive loading from the probe, pad, and the bond wire, is about 20 pF, or about 40 times larger than the intended load.

High Voltage Circuits

The high voltage doubler is used to generate the V^{++} supply. V^{++} is used for the level shifters, and should be greater than 15 volts above V_{DD} ; for simplification, V^{++} may be connected to V_{DD} , however the DMOS outputs will be one threshold below V_{DD} when the DMOS is on.

The level shifters come in two varieties, those in Kit Part-1A and those in Kit Part-1B. Kit Part-A1 is marked with a dot: MPD8020 "●". The level shifters are faster in Kit Part-1B than those in Kit Part-1A, however the current for the level shifters is larger in Kit Part-1B than Kit Part-1A.

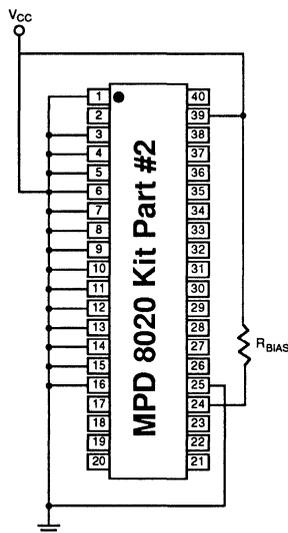
The voltage doubler may be driven either by a square wave generator or an external RC circuit connected to pin 28 (osc. in). The frequency of oscillation is approximately $f = 1 / (0.7 C_{OSC} (R_{OSC} + 4300))$. Connecting a 10 k Ω resistor to V_{CC} and a 1nF capacitors to ground resistor to V_{CC} and a 1nF capacitor to ground will generate a frequency of about 100kHz. For both cases pin 29 (oscillator bias ground) must be connected to ground. The recommended value C_{PUMP} is 1nF (between pin 34 and pin 36) and $C_{FILTER} = 1.0 \mu F$ (pin 35 to V_{DD}); an external 15V to 20V zener diode should be connected from V^{++} 1 out to



Application Hints KP2

Unused Inputs

Unused inputs should be tied together to V_{CC} or ground, specifically pins 1, 3, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15 and 16; not doing so can cause excessive and/or variable I_{CC} current. Disable free running oscillator (pin 6) must be tied to V_{CC} when not in use.



Digital Circuits

The free running oscillator will toggle at approximately 20MHz (for $V_{CC} = 5V$). Since CMOS draws current only during switching, a high I_{CC} will be observed when the oscillator is enabled (pin 6 to ground). At higher voltages, the oscillator will toggle faster, and draw a significant I_{CC} ; it is therefore recommended that the free running oscillator be disabled during testing of other functions.

Analog Circuits

The analog circuits (i.e. the comparator, NPN op amp, and the op amp/buffer amp) all require that pin 24 (R_{BIAS}) is connected through a bias resistor (usually 390 k Ω) to V_{CC} .

The comparator and NPN op amp are designed to drive internal loads (i.e. small capacitive loads such as a buffer, logic, etc.,) and cannot drive resistive or moderate capacitive loads. The op amp/buffer amp combination however, is designed to drive off chip capacitive loads.

Any offset associated with the buffer amp will be divided by the gain of the previous stage. Suitable frequency compensation for loop stability should be employed. The gain, slew rate, output drive capability and bandwidth of the linears may be adjusted by changing R_{BIAS} (and therefore I_{BIAS}).

Micrel
Semiconductor
MPD8020 ASIS™
Design Package
Overview

CMOS/DMOS Semicustom Array

- Start with your circuit design needs
- Solve a problem in in:
 - Size
 - Reliability
 - Performance
 - Keeping out competition
 - Assembly and inventory costs
- Use the CMOS/DMOS technology to put any or all of the following on one IC:
 - Analog CMOS
 - Digital CMOS
 - High voltage CMOS
 - DMOS power FETs
 - Predesigned macros
 - CMOS gate array
 - Bipolar

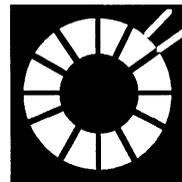
MPD8020 ASIS™ Applications

- Switching regulators
- Motion control
- Bilateral analog switches
- High voltage switching
- Relay and solenoid drivers
- Smart switch with bus decode
- Half or full bridge driver
- 3- ϕ motor driver
- Lamp driver
- Differential line drivers
- Automotive switching
- Printer solenoid drivers
- High-voltage display drivers

MPD8020 ASIS™ Advantages

Switch Mode Power Supplies

25 to 100V operation. Small size, up to 1MHz switching. Full and half H-bridge configurations. DMOS FET source/sink. "Bulletproof circuits" provide overcurrent, overvoltage, and overtemperature protection.



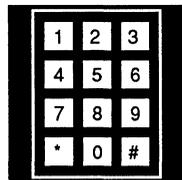
Military Avionics

80V peak, 28V operating (more than 50% derated), capable of meeting Mil Std. 704C. Use for mil spec displays, pin diode drivers, lamp drivers, compact actuator controls, relay drivers, fly-by-wire controls. Wide environmental tolerance. High MTBF. Lightweight, and small size.



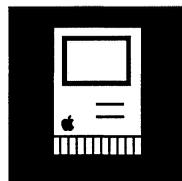
Telecommunications

48V for the central office. VLSI to reduce circuit board real estate. A perfect choice for card cages and subscriber sets. Shrink the size, increase the features and reliability.



Computer Peripherals, Office Equipment, and Industrial Controls

24V operating, 100V peak allows >50% derating for ruggedness. From FAX to friction. 16 solenoid drivers on a single chip. High efficiency and low development cost. 5V to 15V controls high current and/or high voltage. Customize your I/O. High side driver improves safety. Half, full, or 3- ϕ H-bridge configurations are great for HVAC controls, machine driver control, and robotics.

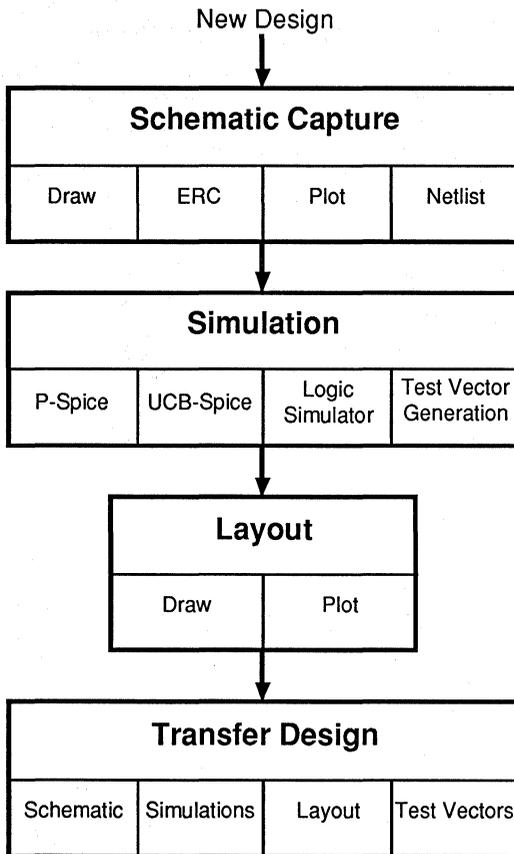


Medical Equipment

80 to 100V. High voltage for feedback and physiological needs. Semicustom array cuts costs, lowers size, reduces parts count, increases features, and improves reliability.



MPD8020 Design Flow



MPD8020 Design Package

Contents: Design books, software, and manuals

Training: 1 man week on-site at Micrel in Sunnyvale, California

Delivery: From Stock

MPD8020 ASIS™ IC Design Package Books

- Design Manual
- User's Guide
- Components Book
- Macro Book

MPD8020 Design Package Software

- **Automenu** Supports menus and runs batch jobs
- **Orcad Std III** Schematic capture
- **P-Spice** Analog and digital Spice simulation
- **UC Berkeley Spice** Analog Spice simulation
- **Orcad VST** Digital simulation
- **Probe** Analog and digital probing software
- **ICED** IC layout editor
- **Micrel 1** Component Library ("LIBRARY") symbol and model libraries
- **Micrel 2** Digital Macro Library ("DIGIMAC 1 & 2") macro symbol and model libraries
- **Micrel 3** Analog Macro Library ("ANAMAC 1 & 2") macro symbol and model libraries
- **Micrel 4** MPD8020 Base Library ("BASE") source, drain, poly, and base layers
- **Micrel 5** Macro Layout Libraries ("MACRO") analog, digital, and power layout libraries

Recommended MPD8020 Design Hardware

- IBM PC (286 or 386 based machine)
- 4M memory
- 20 MHz cache memory system
- 1.2M floppy
- 88M hard disk
- VGA card with monitor
- 20 MHz math co-processor
- Mouse and printer

Interfacing with Micrel

After discovering Micrel's MPD8020 and deciding that you can achieve a significant market advantage by using the MPD8020, follow these steps to complete the chip design and fabrication process:

Note: for jobs for Regional Design Centers (RDC) or in-house Corporate Design Centers (CDC) substitute RDC or CDC for Micrel in steps 2, 3, 4, and 6, 7, 8, 9, 10.

1. Contact Micrel or one of our customer representatives and request literature on the MPD8020. We have a data sheet and other literature available. Call Micrel at (408) 245-2500.
2. To further explore the MPD8020 solution, call Micrel for consultation on technical feasibility for use of the MPD8020 to meet design needs.
3. Send a schematic or a block diagram with a functional description or a breadboard. At this time or before the final design is completed, test vectors (also known as a table of parameters) must be submitted.
4. Micrel's marketing department reviews the business picture and general feasibility. Our design engineers evaluate feasibility of design and convert the schematic or block diagram to a schematic on the 8020 circuit using the advantages of the smart power IC solution. They also generate a chip utilization estimate.
5. With the MPD8020 schematic, the chip utilization estimate, and the customer's statement for package type and volume projections, Micrel's marketing department develops a price quote.
6. The customer's engineering group and purchasing area receives a firm quote from Micrel on price, delivery, and feasibility. You now have the information necessary for decision making.
7. Customer approval cycles are completed and a purchase order is issued to Micrel.
8. Micrel begins the design simulation stage which includes consultation with the customer when needed. This phase of design and simulation is completed.
9. The Preliminary Design Review (PDR) is completed and after any design modifications from the customer a Final Design Review (FDR) occurs. During these reviews you sit down with the Micrel engineers for up to two days and final design and testing requirements are reviewed and finalized. Note that all design modifications have to be finalized at this stage.
10. The chip is sent to layout, and through the use of Micrel's CAD tools, a pin-out is prepared. The bondability of the pin-out in the proposed assembly package is confirmed.
11. A complete continuity check is made of the layout with the schematic.
12. The circuit is sent out for masks. The masks are applied to three wafers in Micrel's fabrication facility. The chip is finalized and these first silicon chips are examined on Micrel's probe stations. Simultaneously, the automatic test equipment program for testing the chip is debugged and tested.
13. With the successful completion of these two programs, you are sent either dice or packaged units as specified for approval and integration into your system. Prototype assembly takes one week and production assembly takes four to five weeks.
14. For full military programs a 1,000 hour life and all other requirements for military standard 883 are now initiated.



MPD8020-0011

3- ϕ DC Brushless Motor Pre-Driver

Design Concept

Functional Description

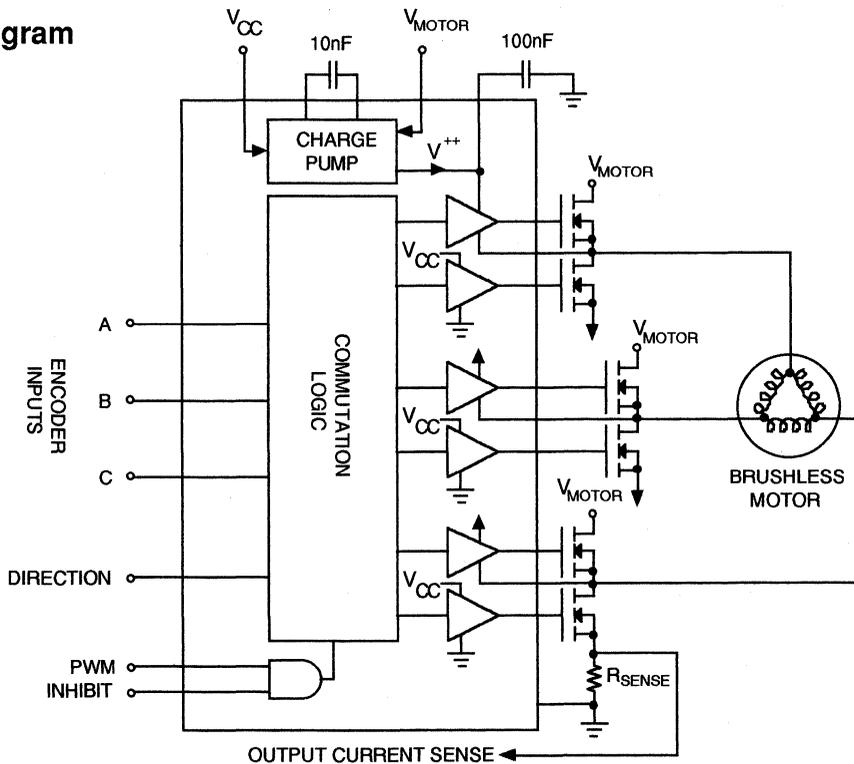
The MPD8020-0011 is a pre-driver for DC brushless motor controllers. Working with Hall-effect or optical feedback, the MPD8020-0011 develops the appropriate drive signals for directional and pulse-width modulation control of a motor. Inputs are included for implementing short circuit protection and for allowing the motor to free-wheel.

The chip drives external quasi-complementary, N-channel power MOSFET output devices. An on-chip charge pump develops the necessary gate drive potential for the high side source followers, while low side gate drive is derived from the 15V (V_{CC}) chip supply.

Features

- Drives quasi-complementary, N-channel MOSFETs
- Full commutation logic with independent PWM and inhibit inputs
- On-chip charge pump for high side drivers eliminates the need for an external gate supply.
- 64V motor supply capability
- Mil spec part available
- Compatible with 60° sensor spacing

Block Diagram



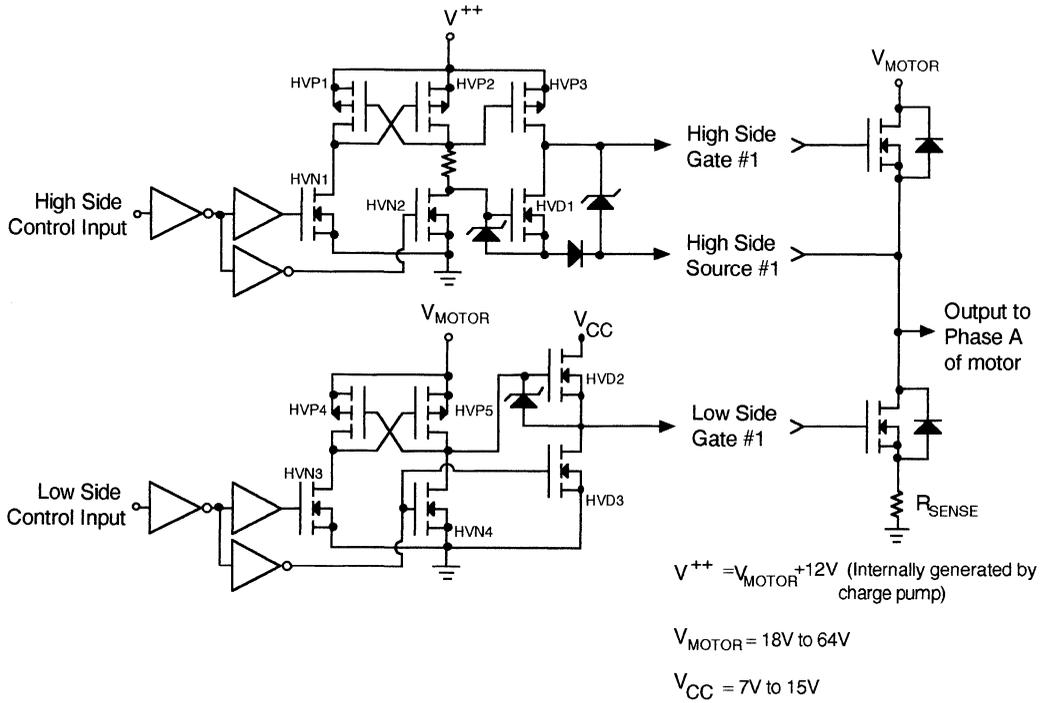


Figure 1. MPD8020-0011 Output Stage (one of three)



MPD8020-0012

8-Channel Low Side Driver with Diagnostics

Design Concept

Functional Description

The MPD8020-0012 is a high voltage, high current, microprocessor interface circuit for high reliability systems. Extensive self-diagnostic circuitry allows rapid detection and announcement of open loads, shorted loads, current overloads, and thermal problems. Included are 8 channels of open drain, N-channel DMOS power FETs that are controlled by individual inputs and a common chip enable. Each channel has a 200 mA current limit as well as full diagnostics. The circuit is implemented on Micrel's proprietary CMOS/DMOS/Bipolar process.

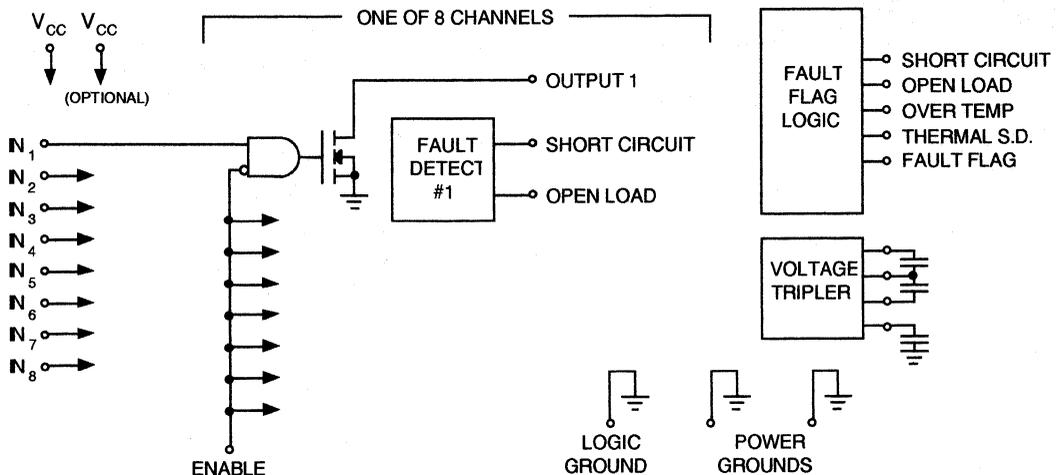
Features

- 8 open drain, N-channel outputs
- 80V, 200 mA outputs
- Logic compatible CMOS inputs with hysteresis
- Short-circuit proof
- Individual open load flags
- Individual short circuit flags
- Overtemperature warning flag and shutdown
- Summary data for short circuit, open load, and thermal flags

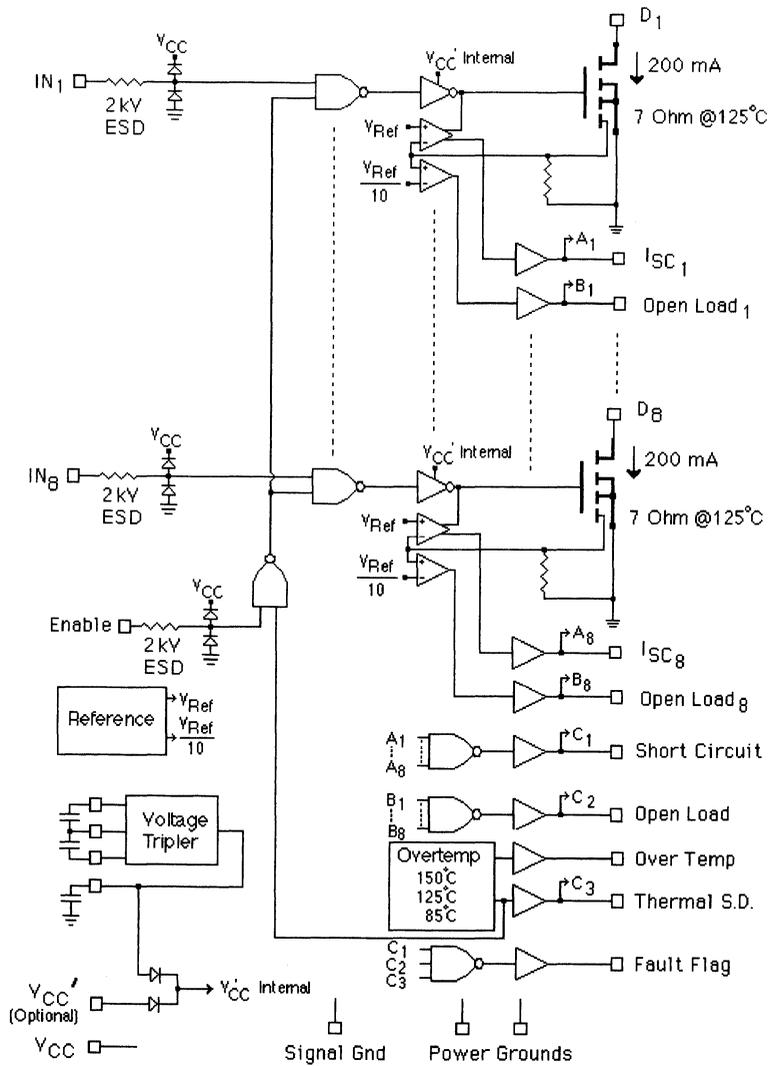
Applications

- Fault tolerant interface circuits
- A bullet-proof driver for relays, lamps, solenoids, print heads, displays

Block Diagram



Detailed Block Diagram



5



MPD8020-0013

PWM "Smart" Lamp Driver

Design Concept

General Description

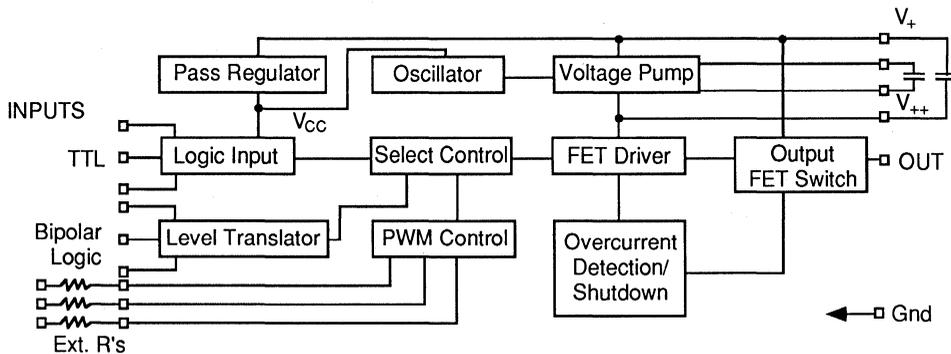
The MPD8020-0013 lamp driver is designed to operate from a 28 Volt DC, aircraft power source and drive up to four (4) 28 VDC incandescent lamps. Three duty cycle control modes set up the lamp intensities for different ambient conditions. In COM mode (100%) the lamps are full on for high ambient light. DIM mode (25%) accommodates reduced light and NV (10%) mode is used for very low ambient light. The PWM controlled intensity may be trimmed using external resistors. The intensity is controlled by logic input, either TTL/CMOS compatible or a relay/switch closure to system ground. The drive pulse rise and fall time is set at about 50 μ S to reduce current spikes and minimize EMI. The lamp driver is a high side switch for ground referenced load applications. This helps minimize corrosion due to moisture on lamp socket contacts, and potential arcing during lamp replacement. Overcurrent protection prevents damage to the IC should the lamp socket be accidentally shorted to ground while the lamp is on.

Features

The PWM Lamp Driver is a monolithic IC designed to drive 28 Volt incandescent lamps from an aircraft power source. The circuit has the following features:

- High side operation with lamp(s) connected to ground
- Input logic compatible with TTL/CMOS or switch closures
- Pre-driver with voltage pump, control and N-Channel FET Switch
- PWM to control lamp intensity from input logic
- PWM adjustment with external resistor or potentiometer
- Overcurrent detection and shutdown
- MIL STD 714A transient voltage protection
- MIL STD 883 qualification
- 16 pin ceramic side brace DIP package
- Bipolar logic compatible, <-5, >+5

Block Diagram



Technology

The fabrication technology chosen is CMOS/DMOS/Bipolar. It is the process of choice when combining analog, digital, and power MOSFET functions on a single IC. This technology is ideal for applications requiring interface between a microcontroller and electromechanical loads. The analog cells provide load current detection and control by using op-amps, comparators, a voltage regulator and a precision voltage reference. The N-Channel FETs provide high voltage (120V),

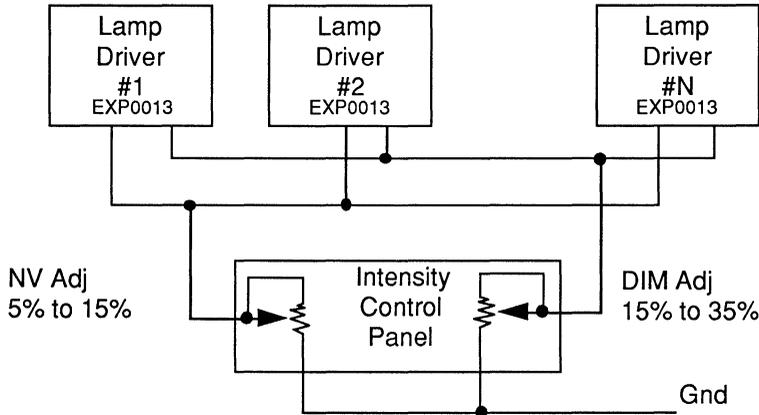
high current up to 2 Amps. The digital gate array provides logic interface to a microcontroller and output logic. Status output signals are accessed through the digital interface.

The CMOS/DMOS/Bipolar process technology is available for full custom and semicustom development programs requiring the use of intelligent control and power interface capability. Packaging is available for special needs.

Specifications

Operating Voltage	28 Volts nominal (18 to 31 V)
Load Current	500 mA Max (4 incandescent Lamps)
Logic Input (TTL)	$V_{SS}/+1.0V$ to $3.5/V_{CC}$
Logic Input(Bipolar)	"1">+5V, "0"<-5V
Switch Control Input	-5V/+5V to 100K Ohm
DIM Mode	25% Duty Cycle +/-2% over temperature range
NV Mode	10% Duty Cycle +/-2% over temperature range
Pulse Rise and Fall time	30µS min to 100µS max.
Output Noise	200mV P-P
Voltage Transient Protection	80V with +/-1-100V/10µS pulse
Overcurrent Protection	700 mA
Overtemperature Protection	155 deg C max.

Lamp Driver Intensity Control





MPD8020-0014

High Current Sink/Source Driver

Design Concept

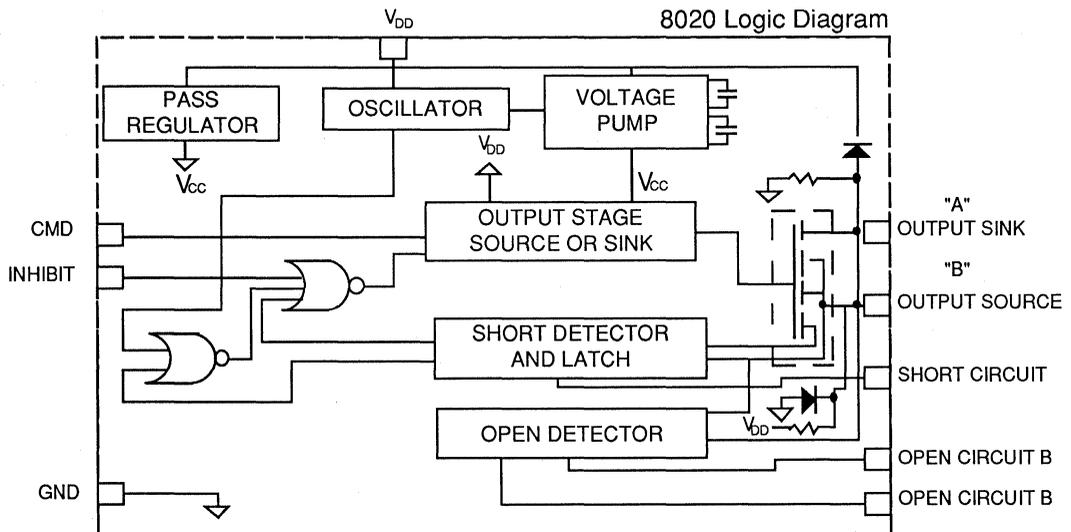
General Description:

The MPD8020-0014 High Current Driver is designed to drive a single N Channel Power MOSFET in either a Sink or Source load configuration. It is designed to operate from a Mil-STD-704D Avionics 28 volt bus, and includes transient voltage protection circuitry. An input logic high turns ON the Power MOSFET selected to meet the $R_{DS(on)}$ and load current required for the application. A sense circuit determines if the load is in sink or source configuration. The FET sense lead generates current proportional to the load, and a reference voltage and comparator determines the current value for overcurrent protection. Flags are generated to indicate an open or short circuit load. The overcurrent detector turns off the driver, and periodically monitors the overcurrent condition, preventing damage to the MOSFET driver.

Features

- Smart Drive for Solenoid or Relays
- Input Logic Compatible with TTL or CMOS
- 16 Pin Side Braze Ceramic DIP package
- Operation Temperature of 55°C to +125°C
- Configurable to drive loads of 5 to 500 Amps
- High Side or Low Side Operation
- Short or Open Circuit Detection and Shutdown with Internal Reset
- Avionic Mil-STD-704D Voltage with Transient Protection
- Switch Load Current of 5 Amps
- Mil-STD-883 Qualification

Block Diagram



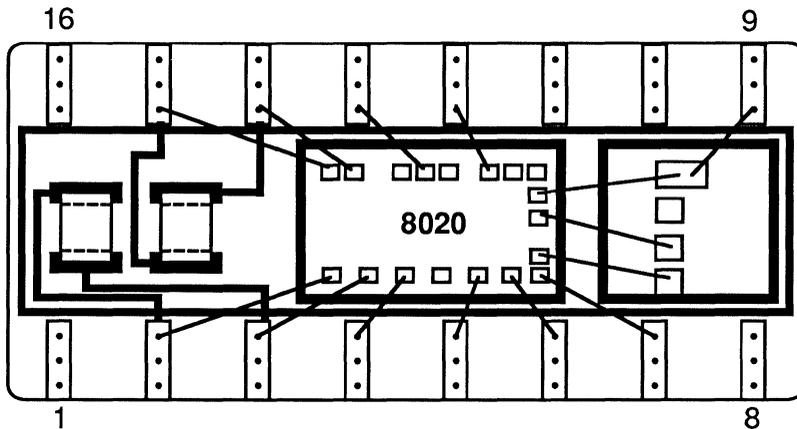
TECHNOLOGY

The process technology is CMOS/DMOS, combining analog, digital and power MOSFET driver macros on a monolithic microcircuit.

The technology is ideal for applications requiring interface between a microcontroller and electromechanical loads, and operating from an avionics 28 volt power bus.

The analog macros provide load current detection and control using op-amps, comparators, voltage regulator and precision voltage reference. A voltage doubler provides gate voltage enhancement for the MOSFET gate drive. Cross coupled pairs interface low level digital logic to high voltage drivers. Status output signals are accessed through digital buffers.

16 Pin Sidebrazed (300mil width)





Voltage Regulators and Assorted Products

	<u>Page</u>
SECTION 6: VOLTAGE REGULATORS AND ASSORTED PRODUCTS	
LP2950/2951 Micropower Voltage Regulator	6-2
MIC18HC42 BiCMOS Current Mode Switching Regulator	6-16
MIC2950/2951 Micropower Voltage Regulator	6-20
MIC3830 Compound Topology SMPS Controller	6-34
MIC5009 Counter/Time Base	6-42



LP2950C/AC and LP2951/C/AC

Adjustable Micropower Voltage Regulators

General Description

The LP2950 and 2951 are micropower voltage regulators with very low dropout voltage (typically 40 mV at light loads and 380 mV at 100 mA), and very low quiescent current (75 μ A typical). The quiescent current of the LP2950/LP2951 increases only slightly in dropout, thus prolonging battery life. This feature, among others, makes the LP2950 and 2951 ideally suited for use in battery-powered systems.

Available in a 3-pin TO-92 package, the LP2950 is pin-compatible with the older 5V regulators. Plastic or ceramic DIP packages and additional system functions such as programmable output voltage and logic controlled shutdown are available with the 8-lead LP2951.

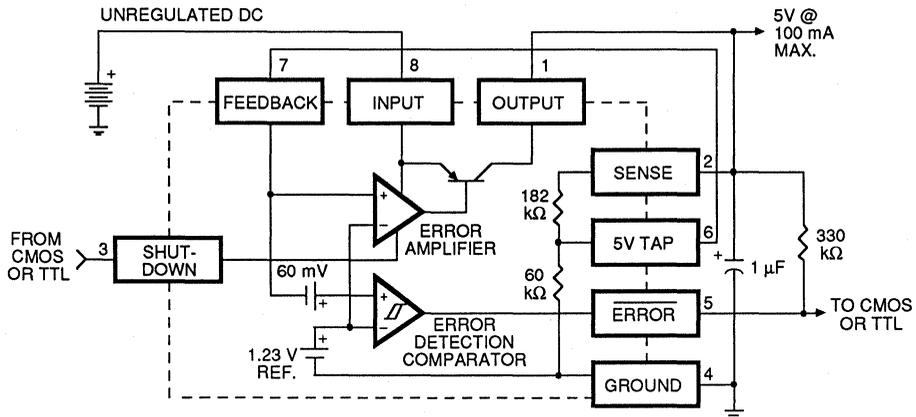
Features

- High accuracy 5V, guaranteed 100 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as regulator or reference
- Needs only 1 μ F for stability
- Current and thermal limiting

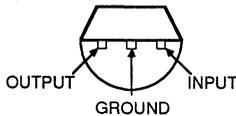
LP2951 Versions Only

- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

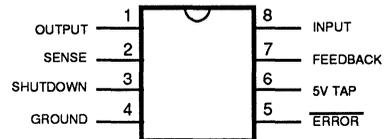
Block Diagram and Pin Configurations



LP2951 Pinout
(LP2951-01AJ, LP2951-02AJ, LP2951-03AJ, LP2951-02BN or LP2951-03BN)



TO-92 Plastic Package Bottom View
(LP2950-02BZ-5.0, LP2950-03BZ-5.0)



SO-8 Package
(LP2951-02BM or LP2951-03BM)

See MIC2950 for a part with 1) higher output (150 mA)
2) transient protection (60V), and 3) Reverse input protection 20V)

Additional features available with the LP2951 also include an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. This may also be used as a power-on reset. A logic-compatible shutdown input is also available which enables the regulator to be switched on and off. This part may also be pin-strapped for a 5 V output, or programmed from 1.24 V to 29 V with the use of two external resistors.

The LP2950 is available as either an -02 or -03 version. The -02 and -03 versions are guaranteed for junction temperatures from -40°C to +125°C; the -02 version has a tighter output and

reference voltage specification range over temperature. The LP2951 is available as an -01, -02, or -03 version. The -01 version is guaranteed for junction temperatures from -55°C to +150°C, and has slightly different specifications limits over the full operating temperature range.

The LP2950 and 2951 have a tight initial tolerance (0.5% typical), a very low output voltage temperature coefficient which allows use as a low-power voltage reference, and extremely good load and line regulation (.05% typical). This greatly reduces the error in the overall circuit, and is the result of careful design techniques and process control.

Ordering Information

Part Number	Temperature Range*	Package
LP2950-02BZ LP2950-03BZ	-40°C to +125°C	3-pin TO-92 plastic
LP2951-02BM LP2951-03BM	-40°C to +125°C	8-pin SO-8
LP2951-01AJ	-55°C to +150°C	8-pin CERDIP
LP2951-02BJ LP2951-03BJ	-40°C to +125°C	8-pin CERDIP
LP2951-02BN LP2951-03BN	-40°C to +125°C	8-pin Plastic DIP

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range (Note 8)	
LP2951-01	-55°C to +150°C
LP2950-02/LP2950-03, LP2951-02/LP2951-03	-40°C to +125°C
Input Supply Voltage	-0.3V to +30V
Feedback Input Voltage (Notes 9 and 10)	-1.5V to +30V
Shutdown Input Voltage (Note 9)	-0.3V to +30V
Error Comparator Output Voltage (Note 9)	-0.3V to +30V
ESD Rating is to be determined.	

Electrical Characteristics (Note 1)

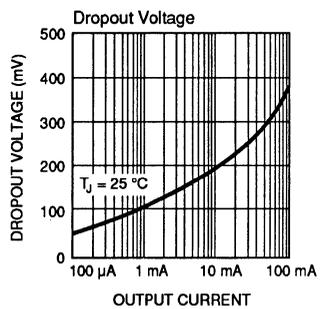
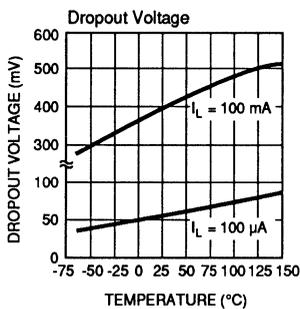
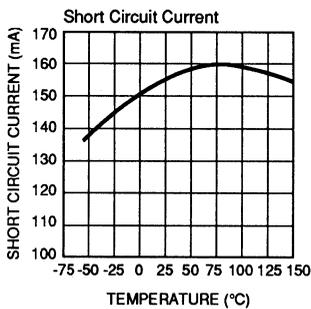
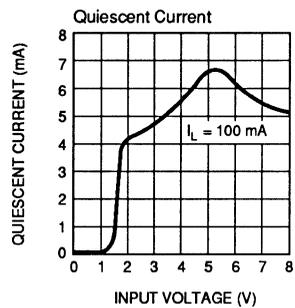
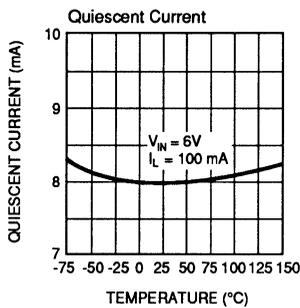
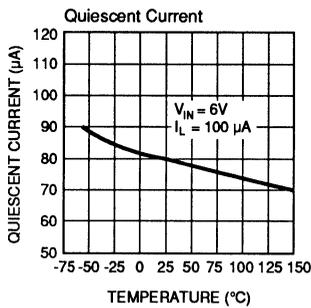
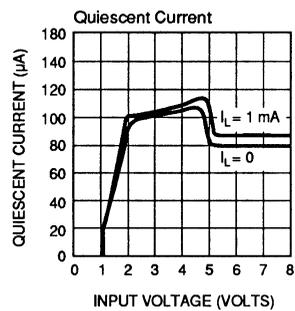
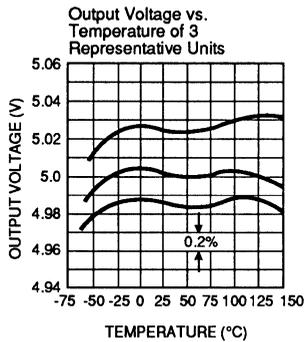
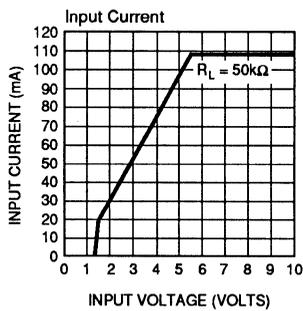
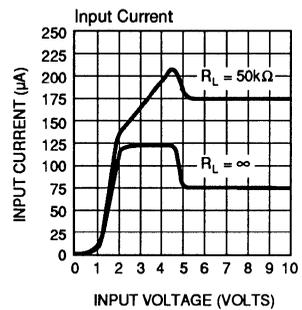
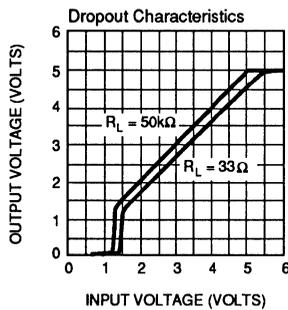
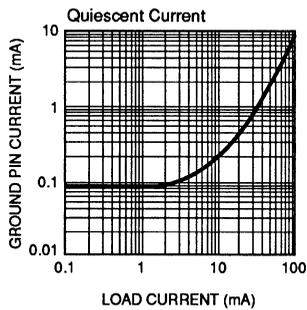
Parameter	Conditions (Note 2)	LP2951-01		LP2950-02 LP2951-02			LP2950-03 LP2951-03			Units
		Typ.	Tested Limit (Note 3)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	
Output Voltage	$T_J = 25^\circ\text{C}$	5.000	5.025 4.975	5.000	5.025 4.975		5.000	5.050 4.950		V max V min
	$-25^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$					5.050 4.950			5.075 4.925	V max V min
	Full Operating Temperature Range		5.060 4.940			5.060 4.940			5.100 4.900	V max V min
Output Voltage	$100\ \mu\text{A} \leq I_L \leq 100\ \text{mA}$ $T_J \leq T_{J_{\text{MAX}}}$		5.075 4.925			5.070 4.930			5.120 4.880	V max V min
Output Voltage Temperature Coefficient	(Note 12)	20	120	20		100	50		150	ppm/ $^\circ\text{C}$
Line Regulation (Note 14)	$6\text{V} \leq V_{\text{IN}} \leq 30\text{V}$ (Note 15)	0.03	0.10 0.50	0.03	0.10	0.20	0.04	0.20	0.40	% max % max
Load Regulation (Note 14)	$100\ \mu\text{A} \leq I_L \leq 100\ \text{mA}$	0.04	0.10 0.30	0.04	0.10	0.20	0.10	0.20	0.30	% max % max
Dropout Voltage (Note 5)	$I_L = 100\ \mu\text{A}$	50	80 150	50	80	150	50	80	150	mV max mV max
	$I_L = 100\ \text{mA}$	380	450 600	380	450	600	380	450	600	mV max mV max
Ground Current	$I_L = 100\ \mu\text{A}$	75	120 140	75	120	140	75	120	140	μA max μA max
	$I_L = 100\ \text{mA}$	8	12 14	8	12	14	8	12	14	mA max mA max
Dropout Ground Current	$V_{\text{IN}} = 4.5\text{V}$ $I_L = 100\ \mu\text{A}$	110	170 200	110	170	200	110	170	200	μA max μA max
Current Limit	$V_{\text{OUT}} = 0$	160	200 220	160	200	220	160	200	220	mA max mA max
Thermal Regulation	(Note 13)	0.05	0.20	0.05	0.20		0.05	0.20		%/W max
Output Noise, 10 Hz to 100 KHz	$C_L = 1\ \mu\text{F}$	430		430			430			μV rms
	$C_L = 200\ \mu\text{F}$	160		160			160			μV rms
	$C_L = 3.3\ \mu\text{F}$ (Bypass = $0.01\ \mu\text{F}$ Pins 7-1 (LP2951))	100		100			100			μV rms

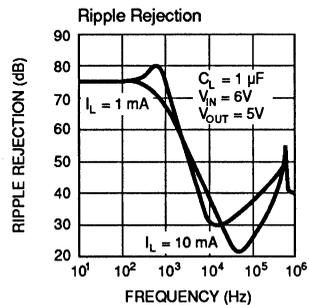
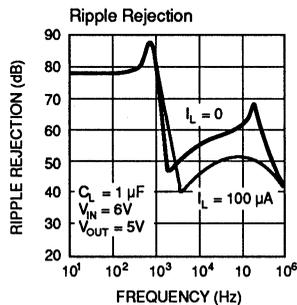
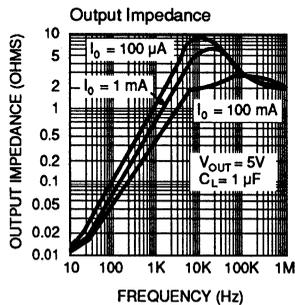
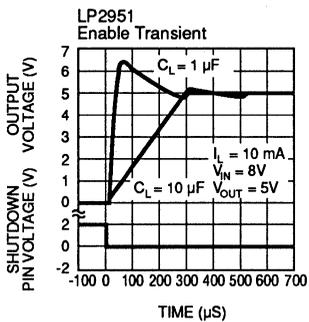
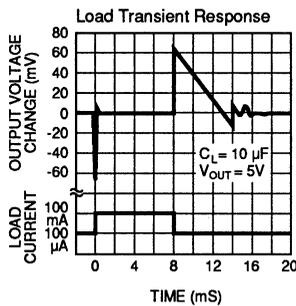
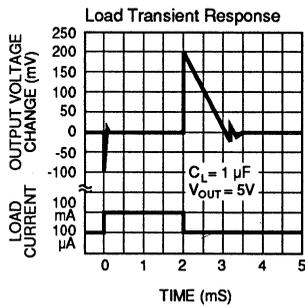
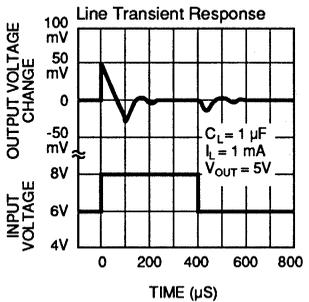
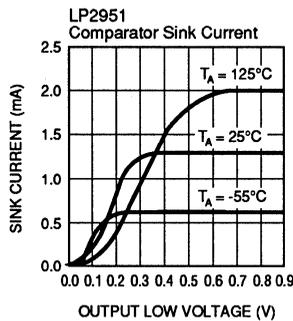
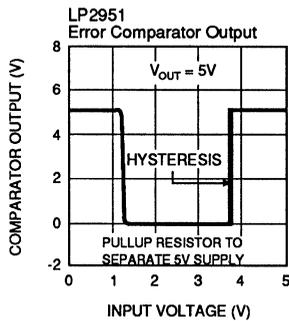
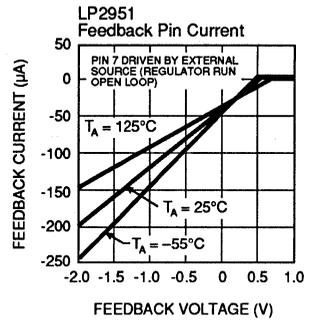
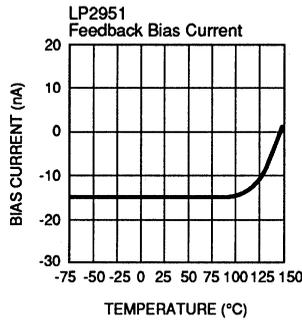
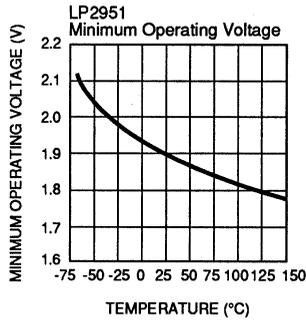
Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 2)	LP2951-01		LP2951-02			LP2951-03			Units
		Typ.	Tested Limit (Note 3)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	
Reference Voltage		1.235	1.250 1.260 1.220 1.200	1.235	1.250 1.220	1.260 1.200	1.235	1.260 1.210	1.270 1.200	V max V max V min V min
Reference Voltage	(Note 7)		1.270 1.190			1.270 1.190			1.285 1.185	V max V min
Feedback Pin Bias Current		20	40 60	20	40	60	20	40	60	nA max nA max
Reference Voltage Temperature Coefficient	(Note 12)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C
Output Leakage Current	$V_{OH} = 30V$	0.01	1.00 2.00	0.01	1.00	2.00	0.01	1.00	2.00	μA max μA max
Output Low Voltage	$V_{IN} = 4.5V$ $I_{OL} = 400 \mu A$	150	250 400	150	250	400	150	250	400	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 25	60	40	25	60	40	25	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 140	75	95	140	75	95	140	mV max mV max
Hysteresis (Note 6)		15		15			15			mV
Input Logic Voltage	Low High	1.3	0.6 2.0	1.3		0.7 2.0	1.3		0.7 2.0	V V max V min
Shutdown Pin Input Current	$V_{SHUTDOWN} = 2.4V$	30	50 100	30	50	100	30	50	100	μA max μA max
	$V_{SHUTDOWN} = 30V$	450	600 750	450	600	750	450	600	750	μA max μA max
Regulator Output Current in Shutdown	(Note 11)	3	10 20	3	10	20	3	10	20	μA max μA max

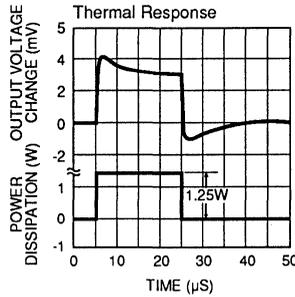
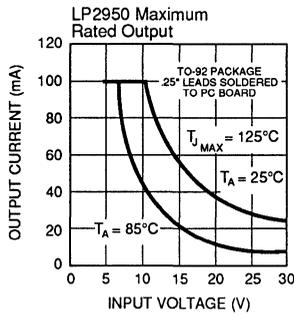
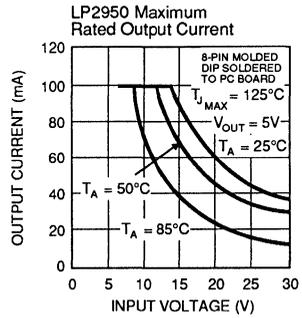
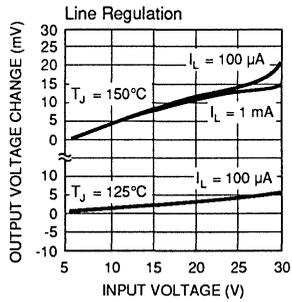
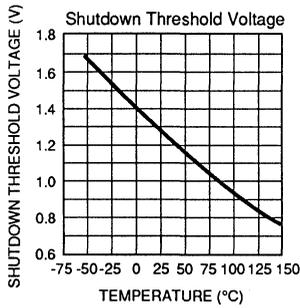
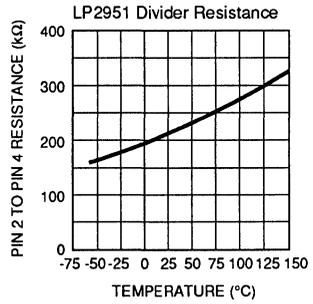
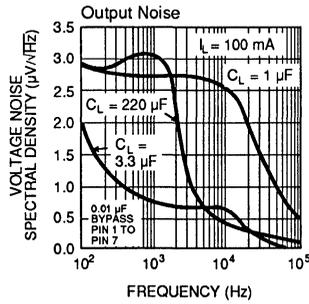
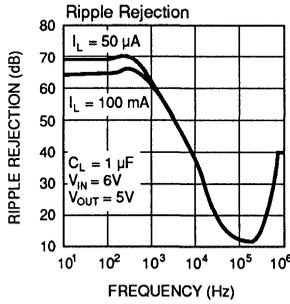
- Note 1:** Boldface limits apply at temperature extremes.
- Note 2:** Unless otherwise specified all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_{IN} = 6\text{ V}$, $I_L = 100\ \mu\text{A}$ and $C_L = 1\ \mu\text{F}$. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense ($V_{OUT} = 5\text{ V}$) and $V_{SHUTDOWN} \leq 0.6\text{ V}$.
- Note 3:** Guaranteed and 100% production tested.
- Note 4:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
- Note 5:** Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V (2.3 V over temperature) must be taken into account.
- Note 6:** Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain $= V_{OUT}/V_{REF} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by $95\text{ mV} \times 5\text{V}/1.235\text{ V} = 384\text{ mV}$. Thresholds remain constant as a percent of V_{OUT} as V_{OUT} is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.
- Note 7:** $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\text{ V})$, $2.3\text{V} \leq V_{IN} \leq 30\text{V}$, $100\ \mu\text{A} < I_L \leq 100\text{ mA}$, $T_J \leq T_{JMAX}$.
- Note 8:** The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistances of the 8-pin DIP packages are 105°C/W for the molded plastic (N) and 130°C/W for the CERDIP (J) junction to ambient when soldered directly to a PC board. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W .
- Note 9:** May exceed input supply voltage.
- Note 10:** When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
- Note 11:** $V_{SHUTDOWN} \geq 2\text{ V}$, $V_{IN} \leq 30\text{ V}$, $V_{OUT} = 0$, with Feedback pin tied to 5V Tap.
- Note 12:** Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
- Note 13:** Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at $V_{IN} = 30\text{ V}$ (1.25 W pulse) for $T = 10\text{ mS}$.
- Note 14:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered in the specification for thermal regulation.
- Note 15:** Line regulation for the LP2951 is tested at 150°C for $I_L = 1\text{ mA}$. For $I_L = 100\ \mu\text{A}$ and $T_J = 125^\circ\text{C}$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Typical Performance Characteristics





Typical Performance Characteristics (Continued)



Applications Information

External Capacitors

A 1.0 μF (or greater) capacitor is required between the LP2950/LP2951 output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about -30°C , so solid tantalums are recommended for operation below -25°C . The important parameters of the capacitor are an ESR of about $5\ \Omega$ or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to $0.33\ \mu\text{F}$ for current below 10 mA or $0.1\ \mu\text{F}$ for currents below 1 mA. Using the 8-pin versions at voltages below 5 V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 100 mA load at 1.23V output (Output shorted to Feedback) a $3.3\ \mu\text{F}$ (or greater) capacitor should be used.

The LP2950 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the LP2951 version with external resistors, a minimum load of $1\ \mu\text{A}$ is recommended.

A $0.1\ \mu\text{F}$ capacitor should be placed from the LP2950/LP2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the LP2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a $100\ \text{pF}$ capacitor between Output and Feedback and increasing the output capacitor to at least $3.3\ \mu\text{F}$ will remedy this.

Error Detection Comparator Output

A logic low output will be produced by the comparator whenever the LP2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the 2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the LP2951 input is ramped up and down. The ERROR signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{\text{OUT}} = 4.75$). Since the LP2951's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will

vary with the load current. The output voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink $400\ \mu\text{A}$, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1M Ω . The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5 V supply. To avoid this invalid response, ERROR should be pulled up to V_{OUT} (See figure 2).

Programming the Output Voltage (LP2951)

The LP2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference and its 30V maximum rating. An external pair of resistors is required, as shown in Figure 2.

The complete equation for the output voltage is

$$V_{\text{OUT}} = V_{\text{REF}} \times \{ 1 + R_1/R_2 \} + I_{\text{FB}} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20 nA. The minimum recommended load current of $1\ \mu\text{A}$ forces an upper limit of 1.2 M Ω on the value of R_2 , if the regulator must work with no load (a condition often found in CMOS in standby), I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1 . For better accuracy, choosing $R_2 = 100\ \text{k}\Omega$ reduces this error to 0.17% while increasing the resistor program current to $12\ \mu\text{A}$. Since the LP2951 typically draws $60\ \mu\text{A}$ at no load with Pin 2 open-circuited, this is a small price to pay.

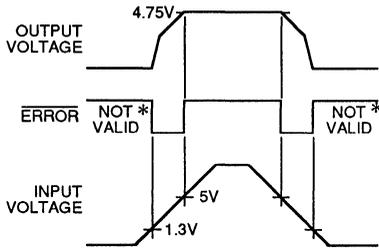
Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output capacitor. This is the only method by which noise can be reduced on the 3 lead LP2950 and is relatively inefficient, as increasing the capacitor from $1\ \mu\text{F}$ to $220\ \mu\text{F}$ only decreases the noise from $430\ \mu\text{V}$ to $160\ \mu\text{V}$ rms for a 100kHz bandwidth at 5V output.

Noise can be reduced fourfold by a bypass capacitor across R_1 , since it reduces the high frequency gain from 4 to unity. Pick

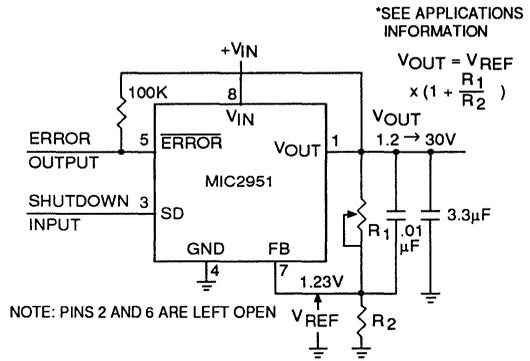
$$C_{\text{BYPASS}} \cong \frac{1}{2\pi R_1 \cdot 200\ \text{Hz}}$$

or about $0.01\ \mu\text{F}$. When doing this, the output capacitor must be increased to $3.3\ \mu\text{F}$ to maintain stability. These changes reduce the output noise from $430\ \mu\text{V}$ to $100\ \mu\text{V}$ rms for a 100 kHz bandwidth at 5V output. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.



* SEE APPLICATIONS INFORMATION

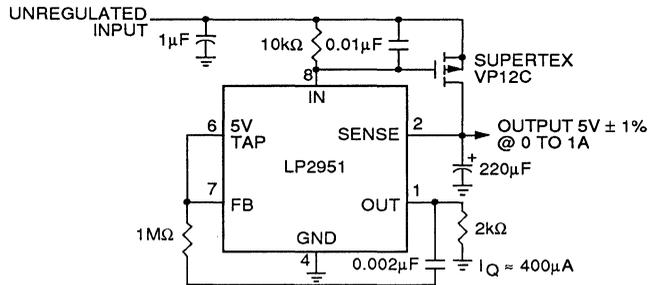
Figure 1. ERROR Output Timing



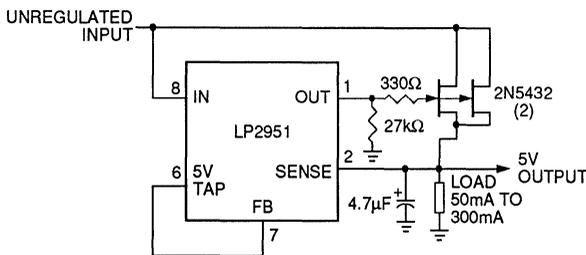
NOTE: PINS 2 AND 6 ARE LEFT OPEN

Figure 2. Adjustable Regulator

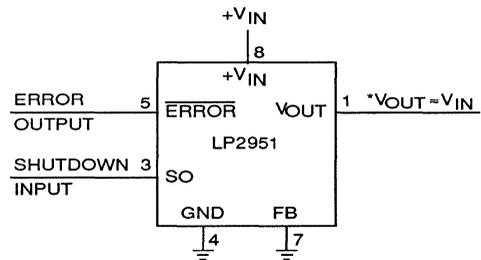
Typical Applications



1A Regulator with 1.2 V Dropout

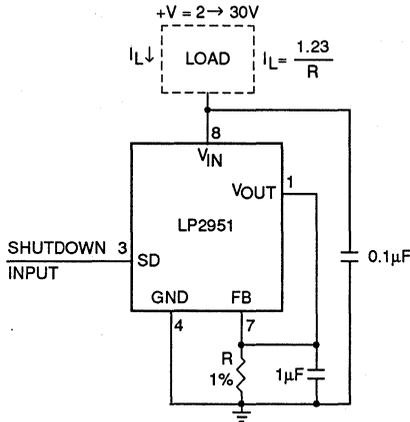


300 mA Regulator with 0.75 V Dropout

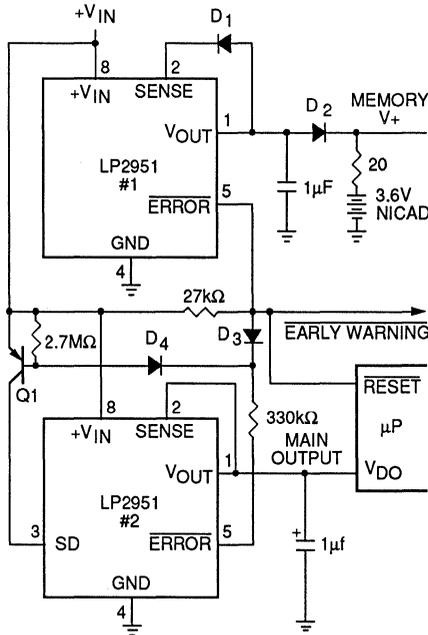


Wide Input Voltage Range Current Limiter

*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40 mV TO 400 mV, DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 160 mA.



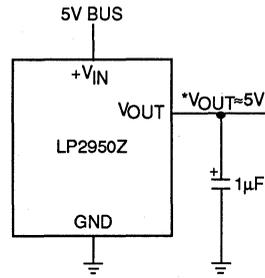
Low Drift Current Source



Regulator with Early Warning and Auxillary Output

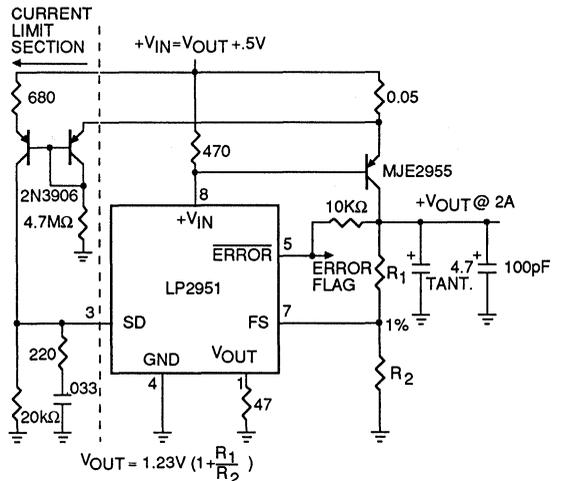
- EARLY WARNING FLAG ON LOW INPUT VOLTAGE
- MAIN OUTPUT LATCHES OFF AT LOWER INPUT VOLTAGES
- BATTERY BACKUP ON AUXILLARY OUTPUT

OPERATION: REG. #1'S V_{OUT} IS PROGRAMMED ONE DIODE DROP ABOVE 5 V. ITS ERROR FLAG BECOMES ACTIVE WHEN $V_{IN} \leq 5.7$ V. WHEN V_{IN} DROPS BELOW 5.3 V, THE ERROR FLAG OF REG. #2 BECOMES ACTIVE AND VIA Q1 LATCHES THE MAIN OUTPUT OFF. WHEN V_{IN} AGAIN EXCEEDS 5.7 V REG. #1 IS BACK IN REGULATION AND THE EARLY WARNING SIGNAL RISES, UNLATCHING REG. #2 VIA D3.



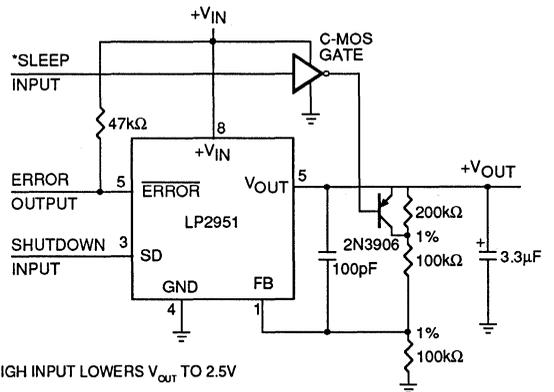
5 Volt Current Limiter

* MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40 MV TO 400 MV, DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 160 MA.

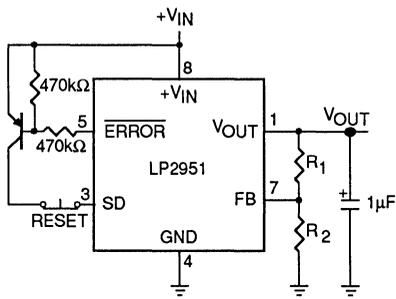


FOR 5 V_{OUT} USE INTERNAL RESISTORS. WIRE PIN 6 TO 7, AND WIRE PIN 10 TO $+V_{OUT}$ BUS.

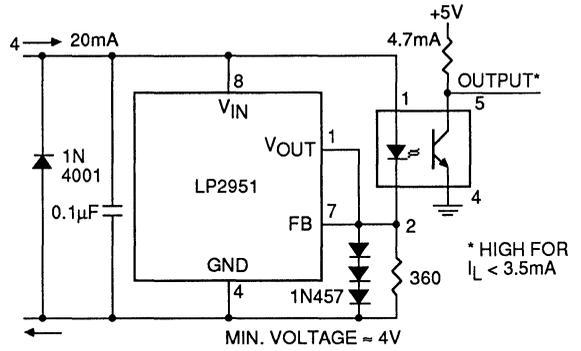
2 Ampere Low Dropout Regulator



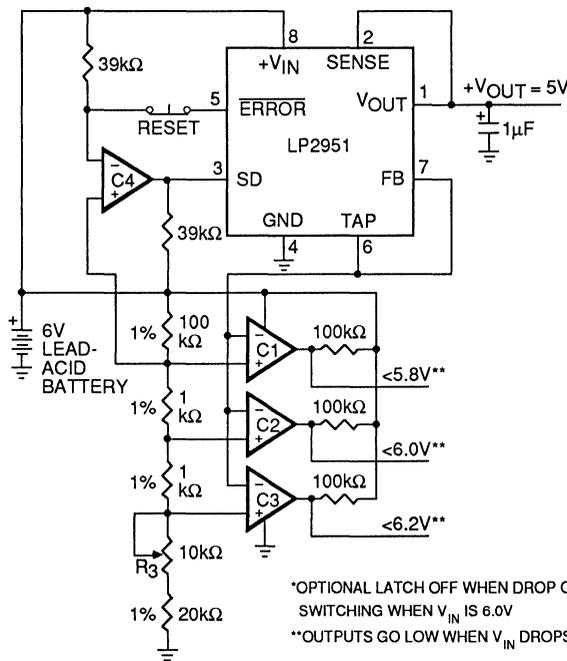
5 V Regulator with 2.5 V Sleep Function



Latch Off When Error Flag Occurs

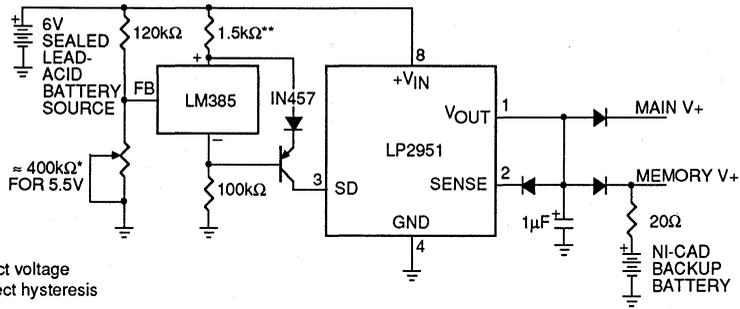


Open Circuit Detector for 4→20 Current Loop



*OPTIONAL LATCH OFF WHEN DROP OUT OCCURS. ADJUST R3 FOR C2 SWITCHING WHEN V_{IN} IS 6.0V
 **OUTPUTS GO LOW WHEN V_{IN} DROPS BELOW DESIGNATED THRESHOLDS.

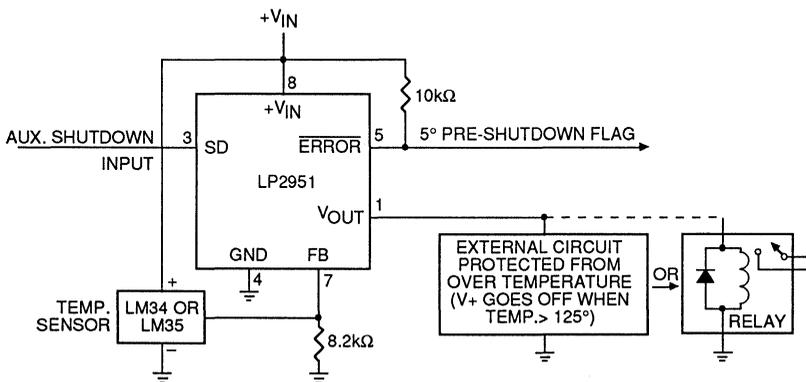
Regulator with State-of-Charge Indicator



* Sets disconnect voltage
 ** Sets disconnect hysteresis

Low Battery Disconnect

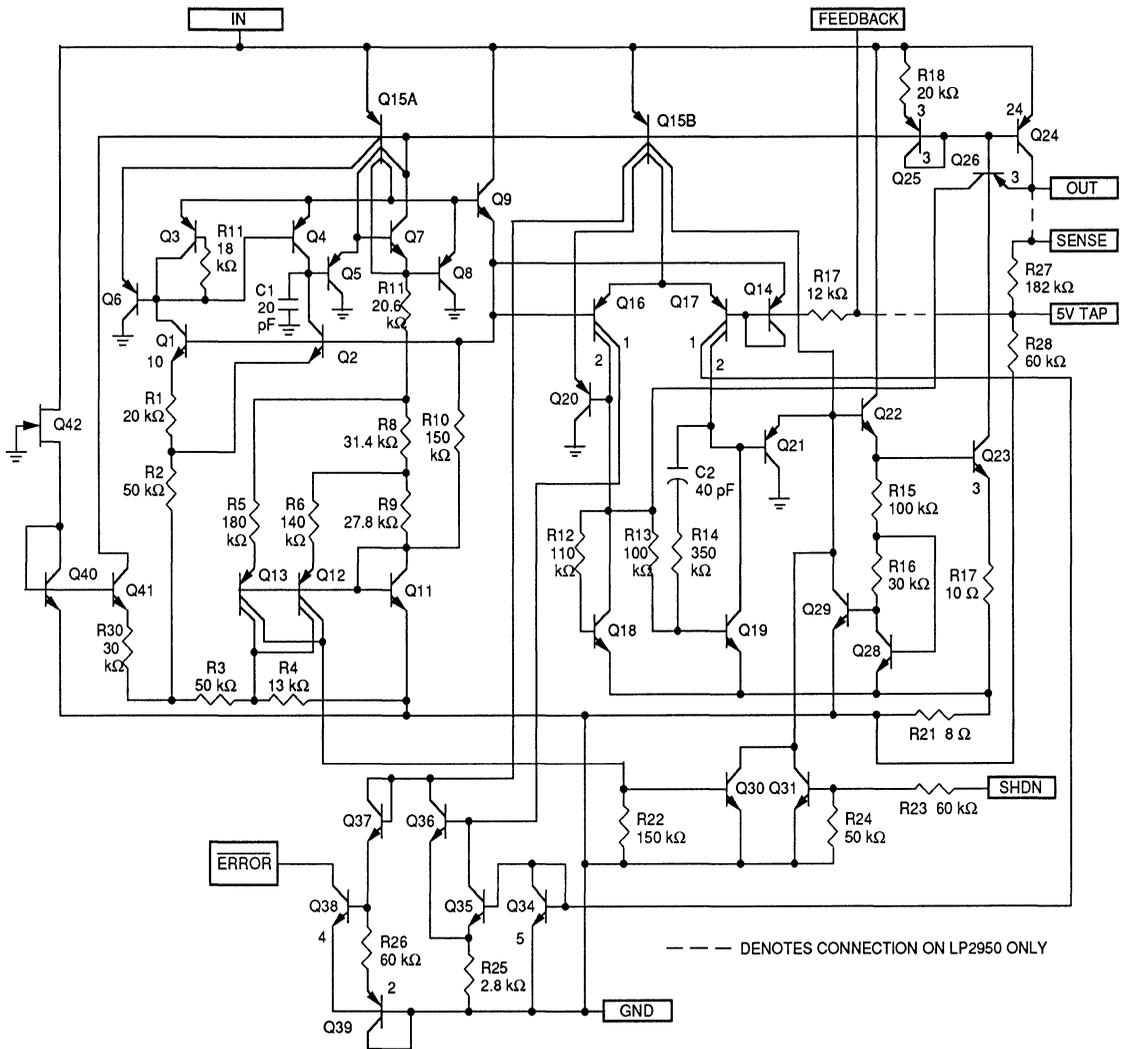
For values shown, Regulator shuts down when $V_{IN} < 5.5\text{ V}$ and turns on again at 6.0 V. Current drain in disconnected mode is 150μA.



LM34 for 125°F Shutdown
 LM35 for 125°C Shutdown

System Overtemperature Protection Circuit

Schematic Diagram



6



MIC2950-02/03 and MIC2951-01/02/03

Adjustable Micropower Voltage Regulators

Preliminary Information

General Description

The MIC2950 and MIC2951 are "bulletproof" micropower voltage regulators with very low dropout voltage (typically 40 mV at light loads and 380 mV at 100 mA), and very low quiescent current (75 μ A typical). Like their predecessors the LP2950 and LP2951, the quiescent current of the MIC2950/MIC2951 increases only slightly in dropout, thus prolonging battery life. The MIC2950/MIC2951 are pin for pin compatible with the LP2950/LP2951.

The key additional features and improvements offered include higher output current (150mA), positive transient protection for up to 60 V (load dump), and the ability to survive an unregulated input voltage transient of up to 20V below ground (reverse battery).

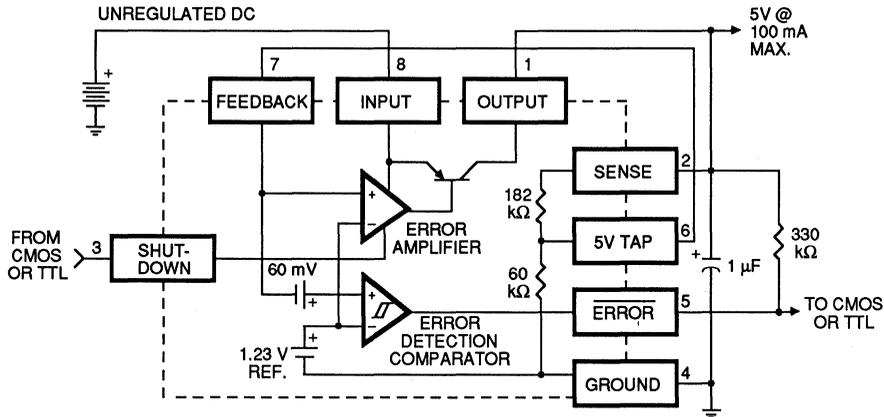
Features

- High accuracy 5V, guaranteed 150 mA output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as regulator or reference
- Needs only 1.5 μ F for stability
- Current and thermal limiting
- Unregulated DC input can withstand -20 V negative transients and +60 V positive transients

MIC2951 Versions Only

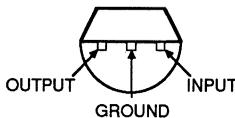
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Pin Configuration

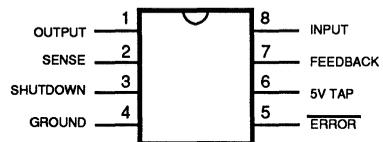


MIC2951 Pinout

(MIC2951-01AJ, MIC2951-02AJ, MIC2951-03AJ, MIC2951-02BN or MIC2951-03BN)



TO-92 Plastic Package Bottom View
(MIC2950-02BZ-5.0, MIC2950-03BZ-5.0)



SO-8 Package
(MIC2951-02BM or MIC2951-03BM)

Available in a 3-pin TO-92 package, the MIC2950 is pin-compatible with the older 5V regulators. Plastic or ceramic DIP packages and additional system functions such as programmable output voltage and logic controlled shutdown are available with the 8-lead MIC2951.

These system functions also include an error flag output that warns of a low output voltage, which is often due to failing batteries on the input. This may also be used as a power-on reset. A logic-compatible shutdown input is also available which enables the regulator to be switched on and off. This part may also be pin-strapped for a 5 V output, or programmed from 1.24 V to 29 V with the use of two external resistors.

The MIC2950 is available as either an -02 or -03 version. The

-02 and -03 versions are guaranteed for junction temperatures from -40°C to +125°C; the -02 version has a tighter output and reference voltage specification range over temperature. The MIC2951 is available as an -01, -02, or -03 version. The -01 version is guaranteed for junction temperatures from -55°C to +150°C, and has slightly different specifications limits over the full operating temperature range.

The MIC2950 and MIC2951 have a tight initial tolerance (0.5% typical), a very low output voltage temperature coefficient which allows use as a low-power voltage reference, and extremely good load and line regulation (.05% typical). This greatly reduces the error in the overall circuit, and is the result of careful design techniques and process control.

Ordering Information

Part Number	Temperature Range*	Package
MIC2950-02BZ MIC2950-03BZ	-40°C to +125°C	3-pin TO-92 plastic
MIC2951-02BM MIC2951-03BM	-40°C to +125°C	8-pin SO-8
MIC2951-01AJ	-55°C to +150°C	8-pin CERDIP
MIC2951-02BJ MIC2951-03BJ	-40°C to +125°C	8-pin CERDIP
MIC2951-02BN MIC2951-03BN	-40°C to +125°C	8-pin Plastic DIP

* Junction temperatures

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact your local Micrel representative/distributor for availability and specifications.

Power dissipation	Internally Limited
Lead Temp. (Soldering, 5 seconds)	260°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range (Note 8)	
MIC2951-01	-55°C to +150°C
MIC2950-02/MIC2950-03, MIC2951-02/MIC2951-03	-40°C to +125°C
Input Supply Voltage (Note 9)	-20V to +60V
Feedback Input Voltage (Notes 10 and 11)	-1.5V to +30V
Shutdown Input Voltage (Note 10)	-0.3V to +30V
Error Comparator Output Voltage (Note 10)	-0.3V to +30V
ESD Rating is to be determined.	

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 2)	MIC2951-01		MIC2950-02 MIC2951-02			MIC2950-03 MIC2951-03			Units
		Typ.	Tested Limit (Note 3)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	
Output Voltage	$T_J = 25^\circ\text{C}$	5.000	5.025 4.975	5.000	5.025 4.975		5.000	5.050 4.950		V max V min
	$-25^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$					5.050 4.950			5.075 4.925	V max V min
	Full Operating Temperature Range		5.060 4.940			5.060 4.940			5.100 4.900	V max V min
Output Voltage	$100 \mu\text{A} \leq I_L \leq 150 \text{ mA}$ $T_J \leq T_{J_{\text{MAX}}}$		5.075 4.925			5.070 4.930			5.120 4.880	V max V min
Output Voltage Temperature Coefficient	(Note 13)	20	120	20		100	50		150	ppm/ $^\circ\text{C}$
Line Regulation (Note 14)	$6\text{V} \leq V_{\text{IN}} \leq 30\text{V}$ (Note 15)	0.03	0.10 0.50	0.03	0.10	0.20	0.04	0.20	0.40	% max % max
Load Regulation (Note 14)	$100 \mu\text{A} \leq I_L \leq 150 \text{ mA}$	0.04	0.10 0.30	0.04	0.10	0.20	0.10	0.20	0.30	% max % max
Dropout Voltage (Note 5)	$I_L = 100 \mu\text{A}$	50	80 150	50	80	150	50	80	150	mV max mV max
	$I_L = 150 \text{ mA}$	380	450 600	380	450	600	380	450	600	mV max mV max
Ground Current	$I_L = 100 \mu\text{A}$	75	120 140	75	120	140	75	120	140	μA max μA max
	$I_L = 150 \text{ mA}$	11	16 20	11	16	20	11	16	20	mA max mA max
Dropout Ground Current	$V_{\text{IN}} = 4.5\text{V}$ $I_L = 100 \mu\text{A}$	110	170 200	110	170	200	110	170	200	μA max μA max
Current Limit	$V_{\text{OUT}} = 0$	240	300 350	240	300	350	240	300	350	mA max mA max
Thermal Regulation	(Note 14)	0.05	0.20	0.05	0.2		0.05	0.20		%/W max
Output Noise, 10 Hz to 100 KHz	$C_L = 1.5 \mu\text{F}$	430		430			430			μV rms
	$C_L = 200 \mu\text{F}$	160		160			160			μV rms
	$C_L = 3.3 \mu\text{F}$ (Bypass = $0.01 \mu\text{F}$ Pins 7-1 (MIC2951))	100		100			100			μV rms

Electrical Characteristics (Note 1) (Continued)

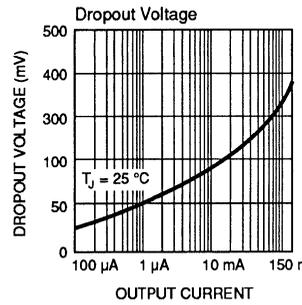
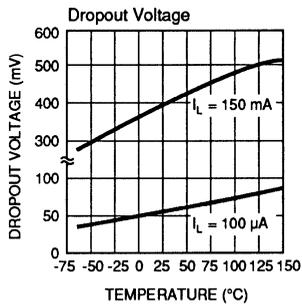
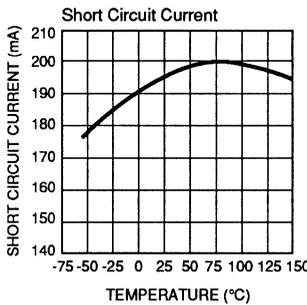
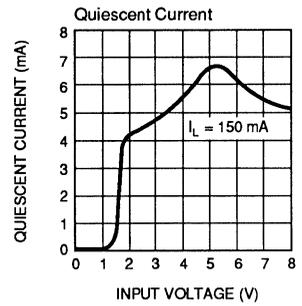
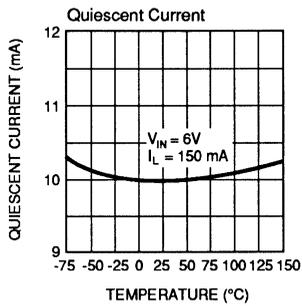
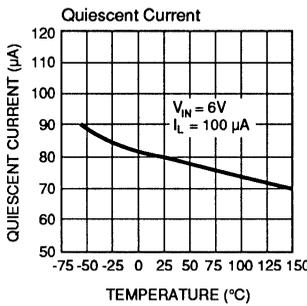
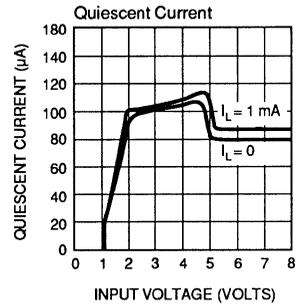
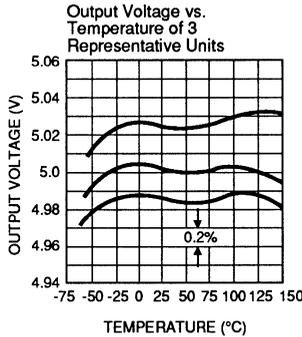
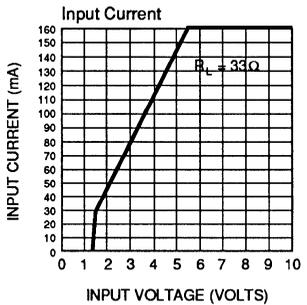
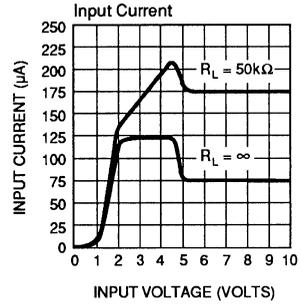
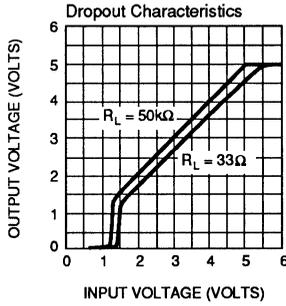
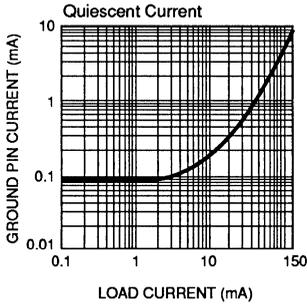
Parameter	Conditions (Note 2)	MIC2951-01		MIC2951-02			MIC2951-03			Units
		Typ.	Tested Limit (Note 3)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	Typ.	Tested Limit (Note 3)	Design Limit (Note 4)	
Reference Voltage		1.235	1.250 1.260 1.220 1.200	1.235	1.250 1.220	1.260 1.200	1.235	1.260 1.210	1.270 1.200	V max V max V min V min
Reference Voltage	(Note 7)		1.270 1.190			1.270 1.190			1.285 1.185	V max V min
Feedback Pin Bias Current		20	40 60	20	40	60	20	40	60	nA max nA max
Reference Voltage Temperature Coefficient	(Note 13)	20		20			50			ppm/°C
Feedback Pin Bias Current Temperature Coefficient		0.1		0.1			0.1			nA/°C

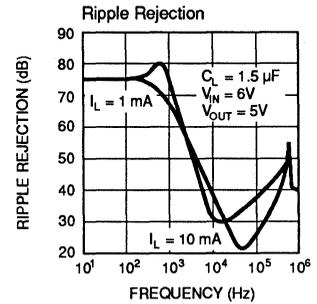
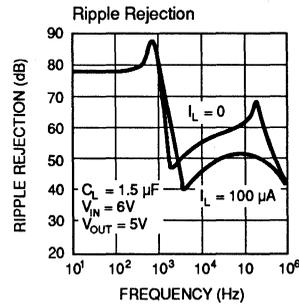
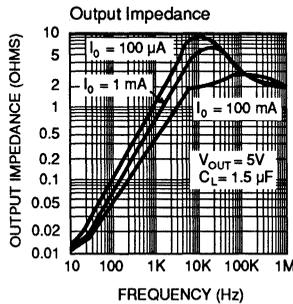
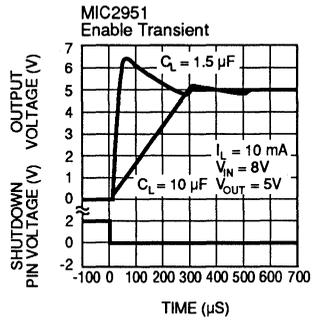
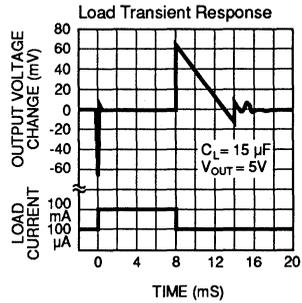
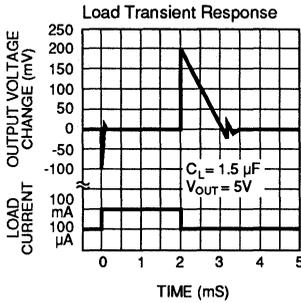
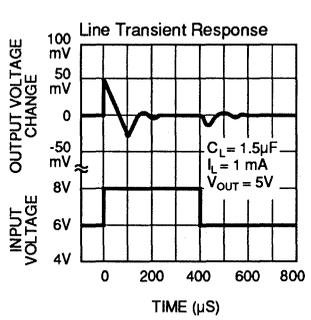
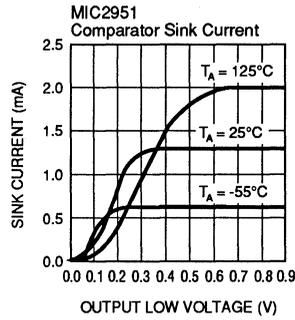
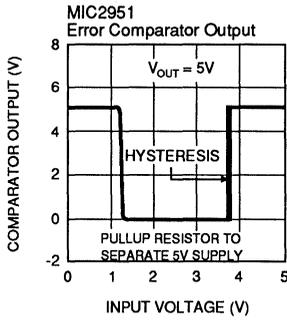
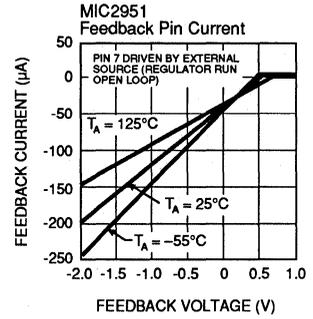
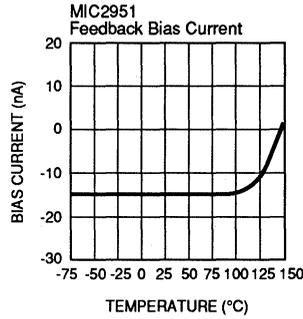
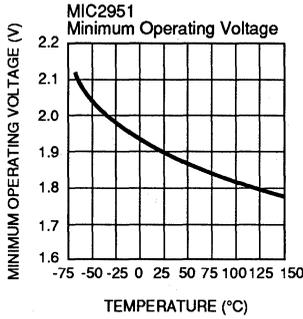
Output Leakage Current	$V_{OH} = 30V$	0.01	1.00 2.00	0.01	1.00	2.00	0.01	1.00	2.00	μA max μA max
Output Low Voltage	$V_{IN} = 4.5V$ $I_{OL} = 400 \mu A$	150	250 400	150	250	400	150	250	400	mV max mV max
Upper Threshold Voltage	(Note 6)	60	40 25	60	40	25	60	40	25	mV min mV min
Lower Threshold Voltage	(Note 6)	75	95 140	75	95	140	75	95	140	mV max mV max
Hysteresis	(Note 6)	15		15			15			mV

Input Logic Voltage	Low High	1.3	0.6 2.0	1.3		0.7 2.0	1.3		0.7 2.0	V V max V min
Shutdown Pin Input Current	$V_{SHUTDOWN} = 2.4V$	30	50 100	30	50	100	30	50	100	μA max μA max
	$V_{SHUTDOWN} = 30V$	450	600 750	450	600	750	450	600	750	μA max μA max
Regulator Output Current in Shutdown	(Note 12)	3	10 20	3	10	20	3	10	20	μA max μA max

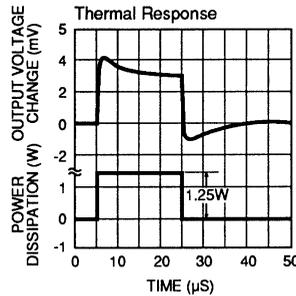
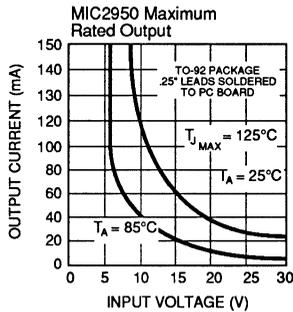
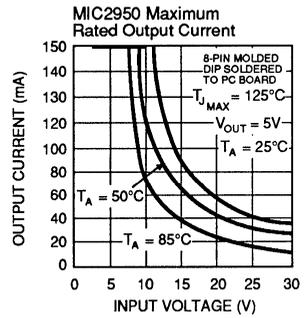
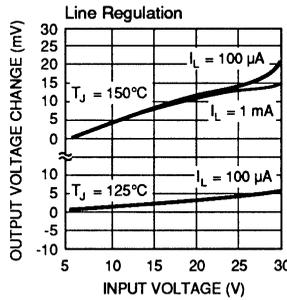
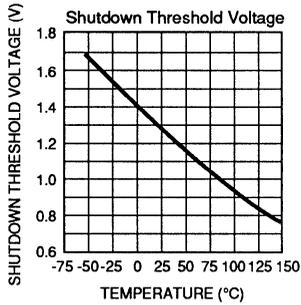
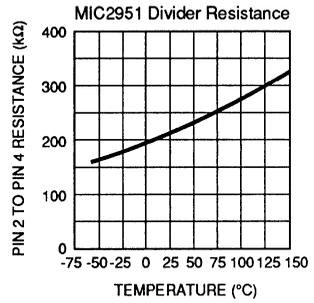
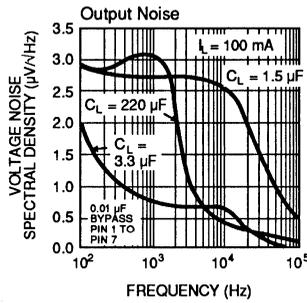
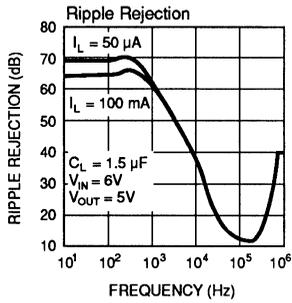
- Note 1:** Boldface limits apply at temperature extremes.
- Note 2:** Unless otherwise specified all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_{IN} = 6\text{ V}$, $I_L = 100\ \mu\text{A}$ and $C_L = 1\ \mu\text{F}$. Additional conditions for the 8-pin versions are Feedback tied to 5V Tap and Output tied to Output Sense ($V_{OUT} = 5\text{ V}$) and $V_{SHUTDOWN} \leq 0.6\text{ V}$.
- Note 3:** Guaranteed and 100% production tested.
- Note 4:** Guaranteed but not 100% production tested. These limits are not used to calculate outgoing AQL levels.
- Note 5:** Dropout Voltage is defined as the input to output differential at which the output voltage drops 100 mV below its nominal value measured at 1V differential. At very low values of programmed output voltage, the minimum input supply voltage of 2 V (2.3 V over temperature) must be taken into account.
- Note 6:** Comparator thresholds are expressed in terms of a voltage differential at the Feedback terminal below the nominal reference voltage measured at 6V input. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain $= V_{OUT}/V_{REF} = (R1 + R2)/R2$. For example, at a programmed output voltage of 5V, the Error output is guaranteed to go low when the output drops by $95\text{ mV} \times 5\text{V}/1.235\text{ V} = 384\text{ mV}$. Thresholds remain constant as a percent of VOUT as VOUT is varied, with the dropout warning occurring at typically 5% below nominal, 7.5% guaranteed.
- Note 7:** $V_{REF} \leq V_{OUT} \leq (V_{IN} - 1\text{ V})$, $2.3\text{V} \leq V_{IN} \leq 30\text{V}$, $100\ \mu\text{A} < I_L \leq 150\text{ mA}$, $T_J \leq T_{J\text{MAX}}$.
- Note 8:** The junction-to-ambient thermal resistance of the TO-92 package is 180°C/W with 0.4" leads and 160°C/W with 0.25" leads to a PC board. The thermal resistances of the 8-pin DIP packages are 105°C/W for the molded plastic (N) and 130°C/W for the CERDIP (J) junction to ambient when soldered directly to a PC board. Junction to ambient thermal resistance for the S.O. (M) package is 160°C/W .
- Note 9:** Maximum positive supply voltage of 60 V must be of limited duration (< 100 mS) and duty cycle (1%). The maximum continuous supply voltage is 30 V.
- Note 10:** May exceed input supply voltage.
- Note 11:** When used in dual-supply systems where the output terminal sees loads returned to a negative supply, the output voltage should be diode-clamped to ground.
- Note 12:** $V_{SHUTDOWN} \geq 2\text{ V}$, $V_{IN} \leq 30\text{ V}$, $V_{OUT} = 0$, with Feedback pin tied to 5V Tap.
- Note 13:** Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
- Note 14:** Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50 mA load pulse at $V_{IN} = 30\text{ V}$ (1.25 W pulse) for $T = 10\text{ mS}$.
- Note 15:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered in the specification for thermal regulation.
- Note 16:** Line regulation for the MIC2951 is tested at 150°C for $I_L = 1\text{ mA}$. For $I_L = 100\ \mu\text{A}$ and $T_J = 125^\circ\text{C}$, line regulation is guaranteed by design to 0.2%. See Typical Performance Characteristics for line regulation versus temperature and load current.

Typical Performance Characteristics





Typical Performance Characteristics (Continued)



Applications Information

Automotive Applications

The MIC2950/2951 are ideally suited for automotive applications for a variety of reasons. They will operate over a wide range of input voltages, have very low dropout voltages (40 mV at light loads), and very low quiescent currents (75 μ A typical). These features are necessary for use in battery powered systems, such as automobiles. They are also "bulletproof" devices; with the ability to survive both reverse battery (negative transients up to 20 V below ground), and load dump (positive transients up to 60 V) conditions. A wide operating temperature range with low temperature coefficients is yet another reason to use these versatile regulators in automotive designs.

External Capacitors

A 1.5 μ F (or greater) capacitor is required between the MIC2950/MIC2951 output and ground to prevent oscillations due to instability. Most types of tantalum or aluminum electrolytics will be adequate; film types will work, but are costly and therefore not recommended. Many aluminum electrolytics have electrolytes that freeze at about -30°C , so solid tantalums are recommended for operation below -25°C . The important parameters of the capacitor are an ESR of about 5 Ω or less and a resonant frequency above 500 kHz. The value of this capacitor may be increased without limit.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.5 μ F for current below 10 mA or 0.15 μ F for currents below 1 mA. Using the 8-pin versions at voltages below 5 V runs the error amplifier at lower gains so that more output capacitance is needed. For the worst-case situation of a 150 mA load at 1.23V output (Output shorted to Feedback) a 5 μ F (or greater) capacitor should be used.

The MIC2950 will remain stable and in regulation with no load in addition to the internal voltage divider, unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications. When setting the output voltage of the MIC2951 version with external resistors, a minimum load of 1 μ A is recommended.

A 0.1 μ F capacitor should be placed from the MIC2950/MIC2951 input to ground if there is more than 10 inches of wire between the input and the AC filter capacitor or if a battery is used as the input.

Stray capacitance to the MIC2951 Feedback terminal (pin 7) can cause instability. This may especially be a problem when using high value external resistors to set the output voltage. Adding a 100 pF capacitor between Output and Feedback and increasing the output capacitor to at least 3.3 μ F will remedy this.

Error Detection Comparator Output

A logic low output will be produced by the comparator whenever the MIC2951 output falls out of regulation by more than approximately 5%. This figure is the comparator's built-in

offset of about 60 mV divided by the 1.235 reference voltage. (Refer to the block diagram on Page 1). This trip level remains "5% below normal" regardless of the programmed output voltage of the MIC2951. For example, the error flag trip level is typically 4.75V for a 5V output or 11.4V for a 12V output. The out of regulation condition may be due either to low input voltage, current limiting, or thermal limiting.

Figure 1 is a timing diagram depicting the $\overline{\text{ERROR}}$ signal and the regulated output voltage as the MIC2951 input is ramped up and down. The $\overline{\text{ERROR}}$ signal becomes valid (low) at about 1.3V input. It goes high at about 5V input (the input voltage at which $V_{\text{OUT}} = 4.75$). Since the MIC2951's dropout voltage is load-dependent (see curve in Typical Performance Characteristics), the input voltage trip point (about 5V) will vary with the load current. The output voltage trip point (approx. 4.75V) does not vary with load.

The error comparator has an open-collector output which requires an external pullup resistor. Depending on system requirements, this resistor may be returned to the 5V output or some other supply voltage. In determining a value for this resistor, note that while the output is rated to sink 400 μ A, this sink current adds to battery drain in a low battery condition. Suggested values range from 100k to 1M Ω . The resistor is not required if this output is unused.

In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external 5 V supply. To avoid this invalid response, $\overline{\text{ERROR}}$ should be pulled up to V_{OUT} (See figure 2).

Programming the Output Voltage (MIC2951)

The MIC2951 may be pin-strapped for 5V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5V Tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference and its 30V maximum rating. An external pair of resistors is required, as shown in Figure 2.

The complete equation for the output voltage is

$$V_{\text{OUT}} = V_{\text{REF}} \times \{ 1 + R_1/R_2 \} + I_{\text{FB}} R_1$$

where V_{REF} is the nominal 1.235 reference voltage and I_{FB} is the feedback pin bias current, nominally -20 nA. The minimum recommended load current of 1 μ A forces an upper limit of 1.2 M Ω on the value of R_2 , if the regulator must work with no load (a condition often found in CMOS in standby). I_{FB} will produce a 2% typical error in V_{OUT} which may be eliminated at room temperature by trimming R_1 . For better accuracy, choosing $R_2 = 100\text{k}$ reduces this error to 0.17% while increasing the resistor program current to 12 μ A. Since the MIC2951 typically draws 60 μ A at no load with Pin 2 open-circuited, this is a small price to pay.

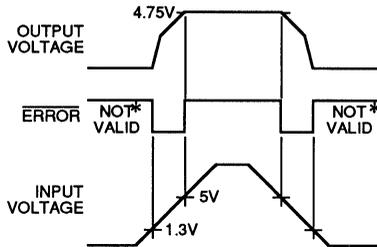
Reducing Output Noise

In reference applications it may be advantageous to reduce the AC noise present at the output. One method is to reduce the regulator bandwidth by increasing the size of the output

capacitor. This is the only method by which noise can be reduced on the 3 lead MIC2950 and is relatively inefficient, as increasing the capacitor from 1 μF to 220 μF only decreases the noise from 430 μV to 160 μV rms for a 100kHz bandwidth at 5V output.

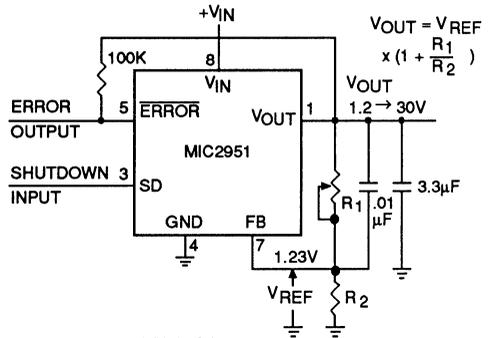
Noise can be reduced fourfold by a bypass capacitor across R_1 , since it reduces the high frequency gain from 4 to unity. Pick

$$C_{\text{BYPASS}} \equiv \frac{1}{2\pi R_1 \cdot 200 \text{ Hz}}$$



* SEE APPLICATIONS INFORMATION

Figure 1. ERROR Output Timing

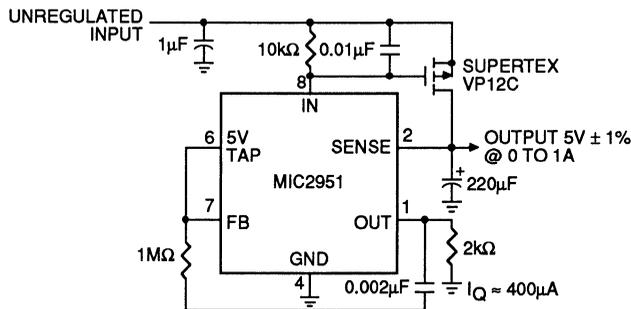


NOTE: PINS 2 AND 6 ARE LEFT OPEN

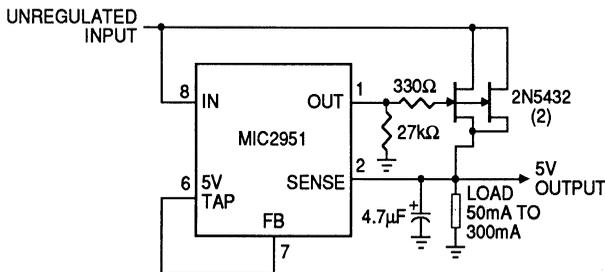
*SEE APPLICATIONS INFORMATION

Figure 2. Adjustable Regulator

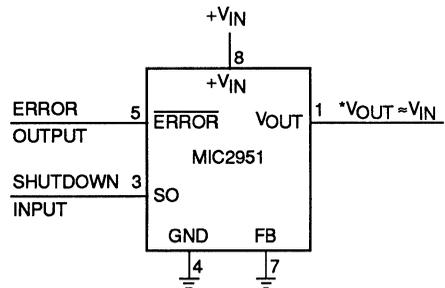
Typical Applications



1A Regulator with 1.2 V Dropout

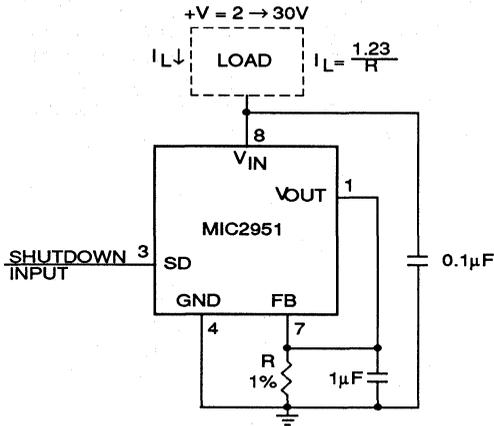


300 mA Regulator with 0.75 V Dropout

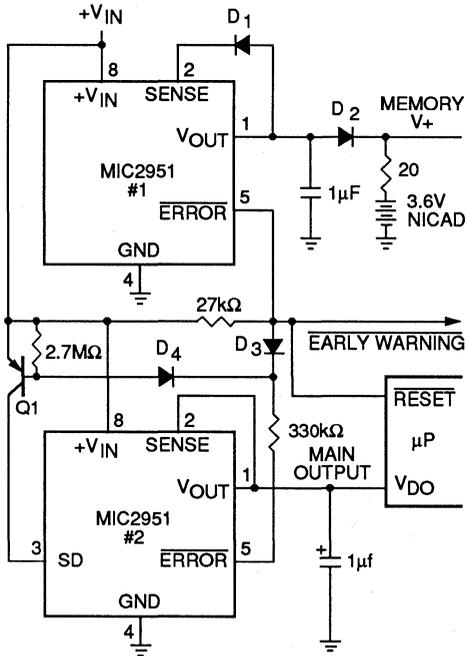


Wide Input Voltage Range Current Limiter

*MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40 mV TO 400 mV, DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 240 mA.



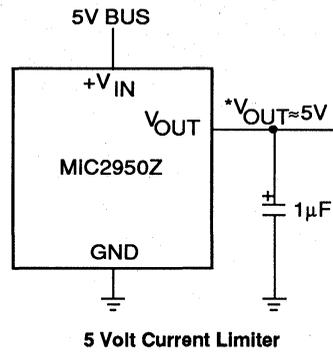
Low Drift Current Source



Regulator with Early Warning and Auxillary Output

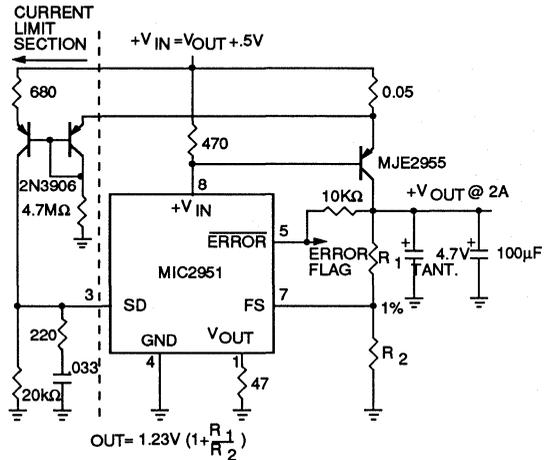
- EARLY WARNING FLAG ON LOW INPUT VOLTAGE
- MAIN OUTPUT LATCHES OFF AT LOWER INPUT VOLTAGES
- BATTERY BACKUP ON AUXILIARY OUTPUT

OPERATION: REG. #1'S V_{OUT} IS PROGRAMMED ONE DIODE DROP ABOVE 5 V. ITS ERROR FLAG BECOMES ACTIVE WHEN $V_{IN} \leq 5.7$ V. WHEN V_{IN} DROPS BELOW 5.3 V, THE ERROR FLAG OF REG. #2 BECOMES ACTIVE AND VIA Q1 LATCHES THE MAIN OUTPUT OFF. WHEN V_{IN} AGAIN EXCEEDS 5.7 V REG. #1 IS BACK IN REGULATION AND THE EARLY WARNING SIGNAL RISES, UNLATCHING REG. #2 VIA D3.



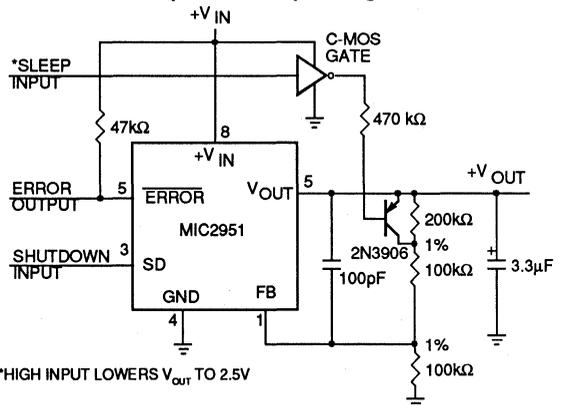
5 Volt Current Limiter

* MINIMUM INPUT-OUTPUT VOLTAGE RANGES FROM 40 MV TO 400 MV, DEPENDING ON LOAD CURRENT. CURRENT LIMIT IS TYPICALLY 240 MA.

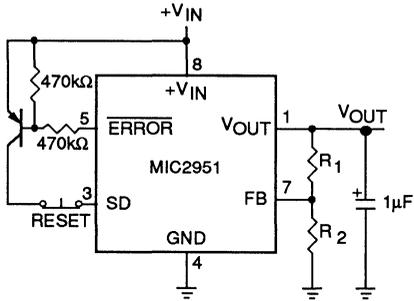


FOR 5 V_{OUT} USE INTERNAL RESISTORS. WIRE PIN 6 TO 7, AND WIRE PIN 20 TO $+V_{OUT}$ BUS.

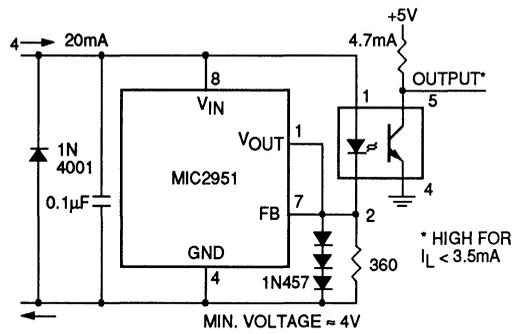
2 Ampere Low Dropout Regulator



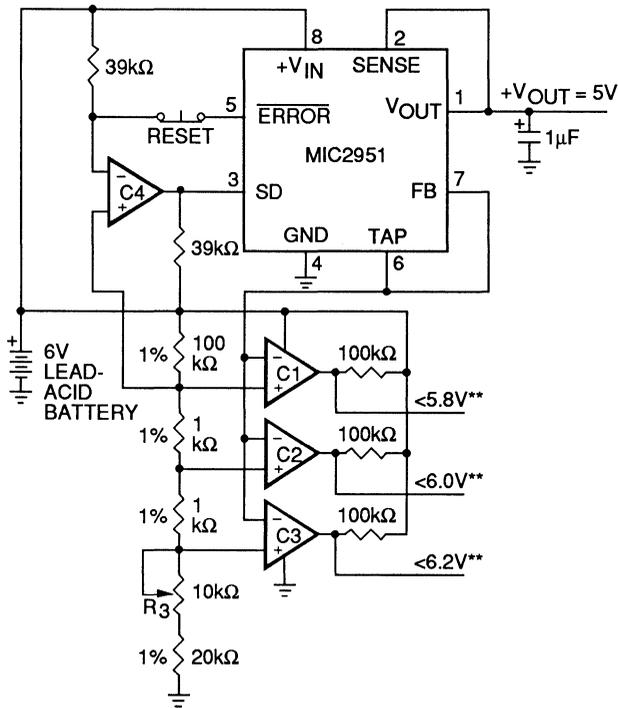
5 V Regulator with 2.5 V Sleep Function



Latch Off When Error Flag Occurs

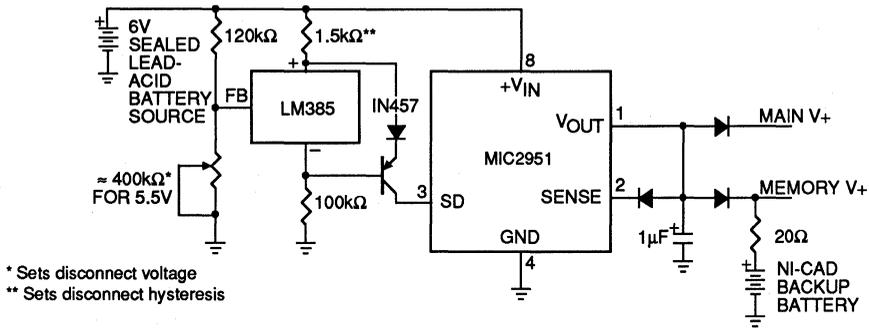


Open Circuit Detector for 4→20 Current Loop



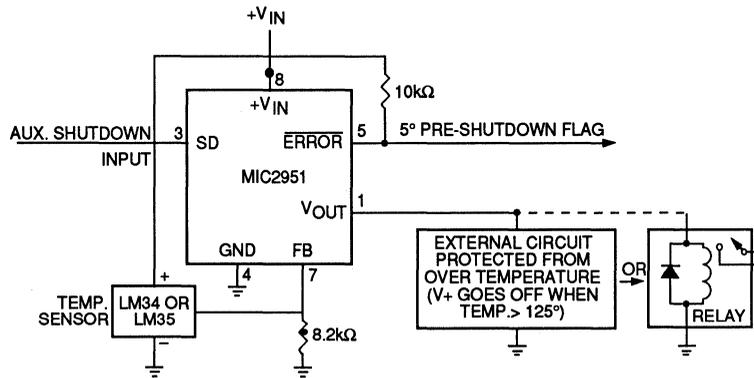
*OPTIONAL LATCH OFF WHEN DROP OUT OCCURS. ADJUST R3 FOR C2 SWITCHING WHEN V_{IN} IS 6.0V
 **OUTPUTS GO LOW WHEN V_{IN} DROPS BELOW DESIGNATED THRESHOLDS.

Regulator with State-of-Charge Indicator



Low Battery Disconnect

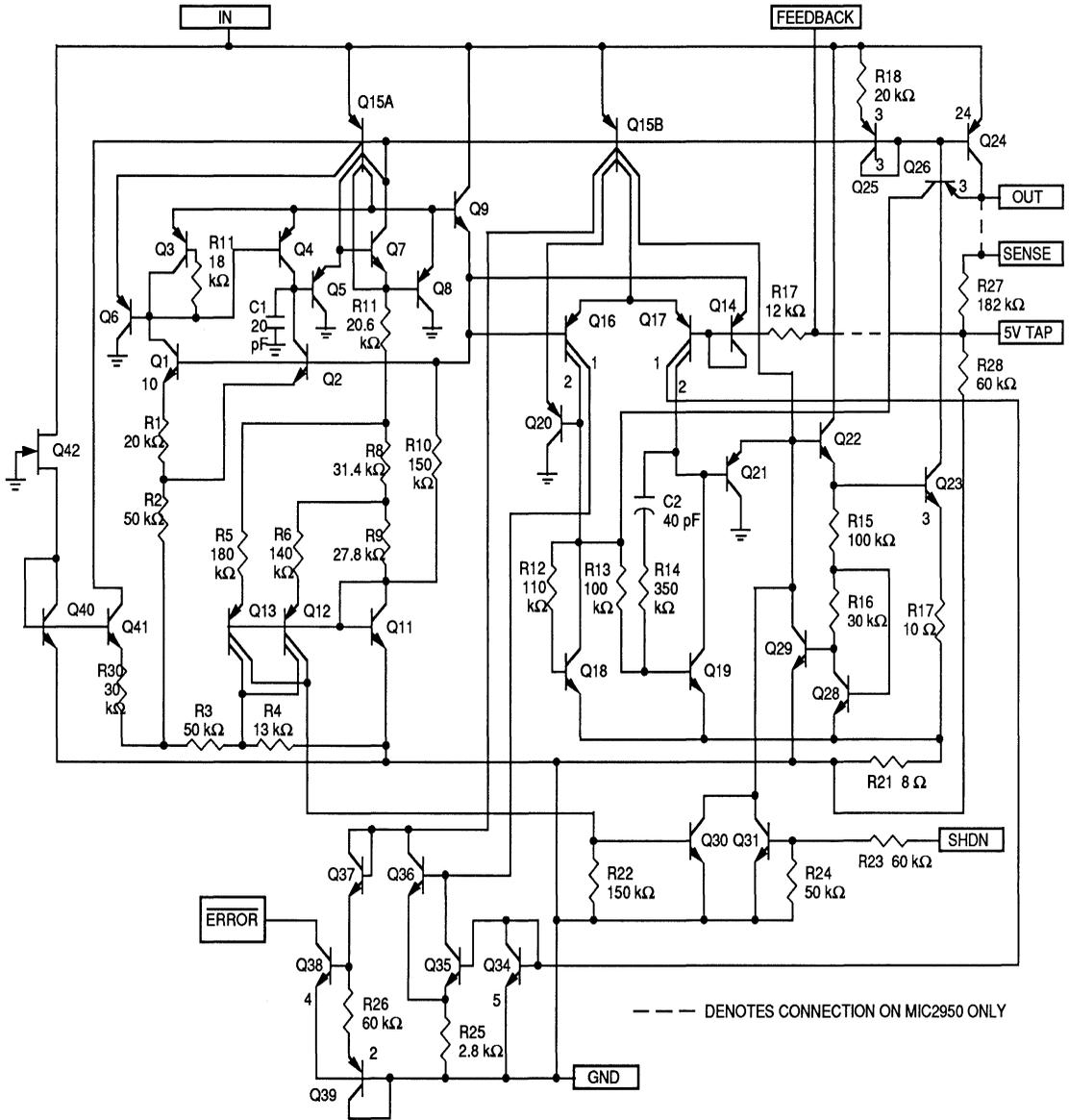
For values shown, Regulator shuts down when $V_{IN} < 5.5\text{ V}$ and turns on again at 6.0 V. Current drain in disconnected mode is 150μA.



LM34 for 125°F Shutdown
LM35 for 125°C Shutdown

System Overtemperature Protection Circuit

Schematic Diagram





MIC3830

Compound Topology PWM Control IC

ADVANCE INFORMATION

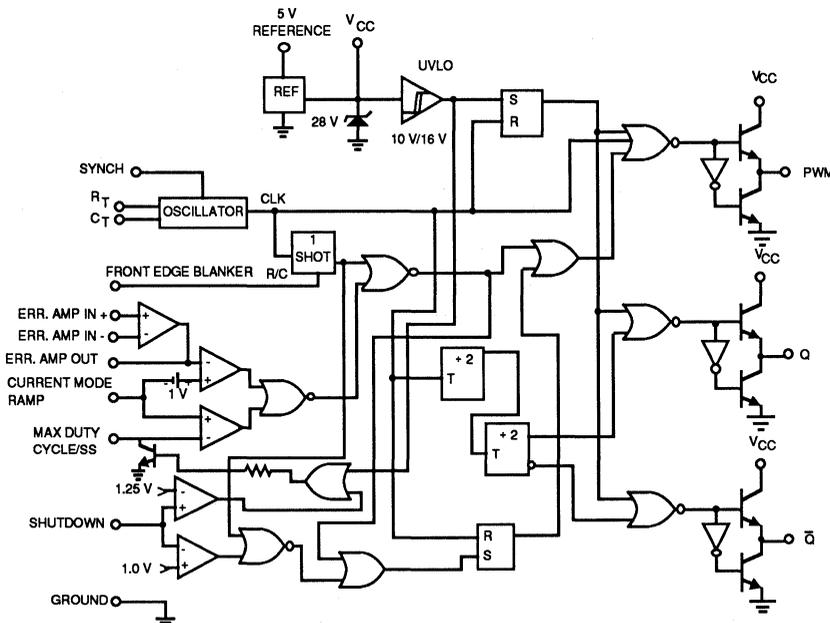
General Description

The MIC3830 is a current mode pulse width modulation controller specifically designed for switched mode power supply and regulated DC to DC converter applications. Although this versatile controller can be used in many topologies, it incorporates special features which make it ideal for use in current fed converter topologies in which a converter stage is followed by a 50 % duty cycle inverter stage. Current fed topologies are preferable to voltage fed topologies as they eliminate over current spiking which can cause failures of the switching elements.

The three optimized power transistor output stages have a peak output current of 1 A, allowing the use of either power MOSFETs, IGBTs, or bipolar transistors as switching elements. Two of the three stages, Q and \bar{Q} , have a fixed 50% duty cycle and operate at 1/4 the system frequency. They are designed to interface with the inverter stage. The third is the main output, and has a programmable maximum duty cycle. It can operate up to 500 kHz. Totem pole output stages are used for efficient direct drive of the switching transistors.

Either current mode or voltage mode control can be used. If voltage mode control is desired, the C_T pin is simply tied to the current mode ramp pin.

Functional Diagram



Features

- * 11 V to 28 V operation
- * Current or voltage mode control
- * 0.5 mA max start-up current
- * 1 A peak output current
- * 50 nS maximum rise and fall times
- * 500 kHz PWM stage
- * 3 optimized totem pole output drive stages
- * Soft start function
- * Undervoltage lockout with hysteresis
- * Zener clamp
- * Cycle by cycle current limit
- * Programmable front edge current pulse blanking
- * PWM latch to eliminate multiple outputs due to noise or ringing.

Applications

- * Switched mode power supplies

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
MIC3830BN	- 40 °C to + 85 °C	16 pin Plastic DIP
MIC3830BJ	- 40 °C to + 85 °C	16 pin Ceramic DIP

This IC has been "bullet-proofed" by the addition of cycle by cycle current limiting and soft start. Front edge current blanking allows the systems designer to delay the onset of the current limit until all systems transients have died away.

Programmability of this function is accomplished via the size of external capacitor added to the I_{blank} pin. Under-voltage lockout with hysteresis prevents spurious turn-ons due to system noise, and a PWM latch has been added to eliminate multiple outputs due to noise or ringing.

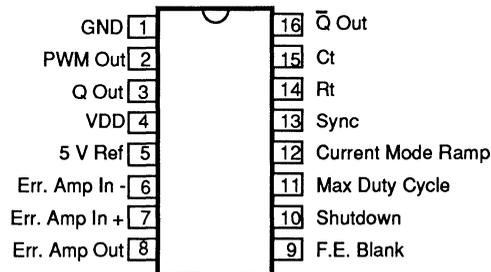
Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{DD}), Pin 4	28 V
Source/Sink Load Current	1 A
Maximum Zener Current	50 mA
Junction Temperature	150 °C
Lead Temperature, Soldering	260 °C for 10 seconds
θ_{JA} Ceramic DIP	100 °C/W
θ_{JA} Plastic DIP	135 °C/W

Operating Ratings (Notes 1 and 2)

Storage Temperature Range	-65 °C to +150 °C
Operating Temperature Range	-40 °C to +85 °C
Reference Load Current	0 to 25 mA
Supply Voltage (V_{DD}), Pin 4	11 V to 28 V
Oscillator Frequency Range	10 kHz to 500 kHz
Oscillator Timing Resistor	1k Ω to 100k Ω
Oscillator Timing Capacitor	390 pF to .01 μ F
Available Deadtime Range	150 nS to 4 μ S

Pin Configuration



Electrical Characteristics (Note 3) See figure 1 for test circuit. $T_A = -40$ °C to +85 °C, $V_{DD} = 15$ V, $f = 52$ kHz unless otherwise specified.

Parameter	Conditions	Min	Typical	Max	Units
Reference Section					
Output Voltage	$I_O = 1$ mA, $T_A = 25$ °C	4.90	5.0	5.10	V
Input Regulation	$V_{CC} = 12$ V to 25 V		2.0	20	mV
Output Regulation	$I_O = 1$ mA to 20 mA		3.0	25	mV
Temp Stability			-0.2		mV/°C
Total Output Variation	Line, load, temp	4.82		5.18	V
Output Noise Voltage	$f = 10$ Hz to 10 kHz, $T_A = 25$ °C		50		μ V
Long Term Stability	$T_A = 125$ °C, 1000 hrs		5.0		mV
Output Short Circuit Current	$V_{REF} = 0$	25	60	160	mA
Oscillator Section					
Frequency	$T_A = 25$ °C	47	52	57	kHz
Voltage Stability	$V_{CC} = 12$ V to 25 V		0.5		%
Temp Stability			5.0		%
Amplitude			1.7		V
Discharge Current	$T_A = 25$ °C		8.3		mA
	-40 °C to +85 °C			9.5	mA

Electrical Characteristics (Continued)

Parameter	Conditions	Min	Typical	Max	Units
Error Amplifier Section					
Input Offset Voltage		-15	±2	15	mV
Input Bias Current			0.6	3.0	μA
Input Offset Current			0.1	1.0	μA
Open Loop Gain	$1 < V_O < 4V$	60	95		dB
CMRR	$1.5 < V_{CM} < 5.5 V$	75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		dB
Output Sink Current	$V_{PIN8} = 1V$	1.0	2.5		mA
Output Source Current	$V_{PIN8} = 4V$	-0.5	-1.3		mA
Output High Voltage	$I_{PIN8} = -0.5 mA$	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN8} = 1 mA$	0	0.5	1.0	V
Soft Start/Duty Cycle Clamp Section					
Bias Current			-1.2		μA
Discharge Current		1			mA
Duty Cycle Clamp Accuracy		40	50	60	%
Current Limit/Shutdown Section					
Bias Current			-1.2		μA
Current Limit		0.9	1.0	1.1	V
Threshold					
Shutdown Threshold		1.125	1.25	1.375	V
Delay to Output			200	300	nS
PWM Comparator Section					
Bias Current			-1	-5	μA
Duty Cycle Range		0		85	%
Zero D.C. Threshold					
Delay to Output			200	300	nS
Blanking Network					
Input Bias Current			-1		μA
Blanking Threshold		0.9	1.0	1.1	V
Output Sections					
Output Low Level	$I_{SINK} = 20 mA$		0.1	0.4	
	$I_{SINK} = 200 mA$		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20 mA$	13			
	$I_{SOURCE} = 200 mA$	12	13.5		V
Rise Time	$T_A = 25^\circ C, C_L = 1 nF$		50	150	nS
Fall Time	$T_A = 25^\circ C, C_L = 1 nF$		50	150	nS
UVLO Saturation	$V_{CC} = 6 V, I_L = 1 mA$		0.7	1.1	V

Electrical Characteristics (Continued)

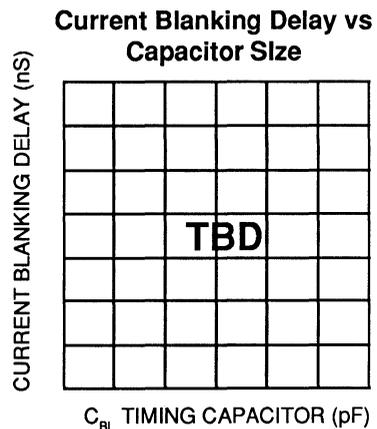
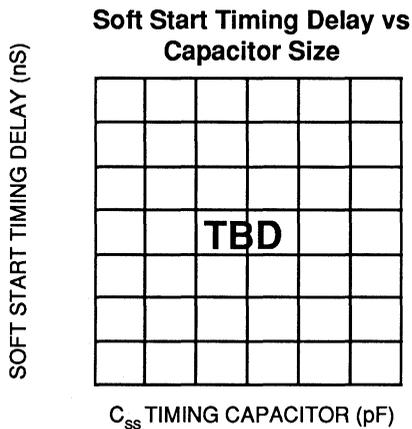
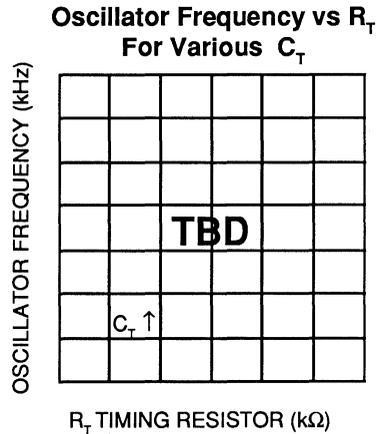
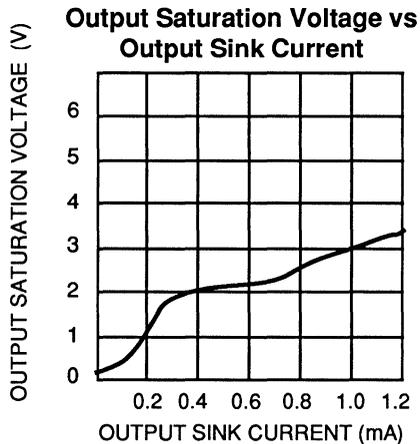
Parameter	Conditions	Min	Typical	Max	Units
Under- Voltage Lockout Section					
Upper Threshold		14.5	16	17.5	V
Lower Threshold		8.5	10	11.7	V
Total Standby Current					
Startup Current			0.2	0.5	mA
Operating Supply			22		mA
V _{CC} Zener Voltage	I _{CC} = 25 mA		28		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified **Operating Ratings**.

Note 2: The MIC3830 is ESD sensitive.

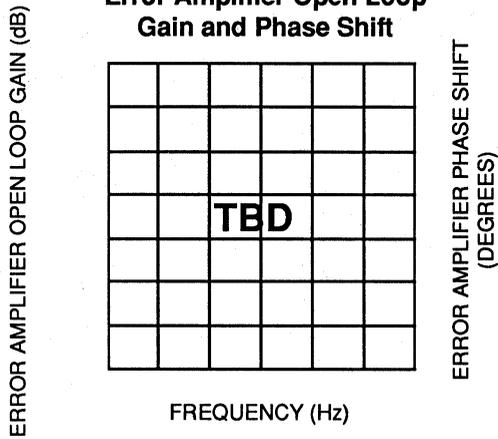
Note 3: Minimum and maximum **Electrical Characteristics** are 100% tested at T_A = 25°C and T_A = 85°C, and 100% guaranteed over the entire operating range. Typicals are characterized at 25°C and represent the most likely parametric norm.

Typical Characteristics

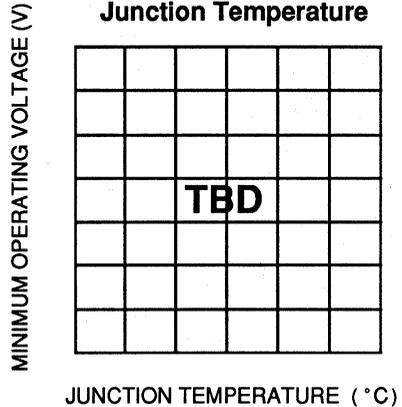


Typical Characteristics (Continued)

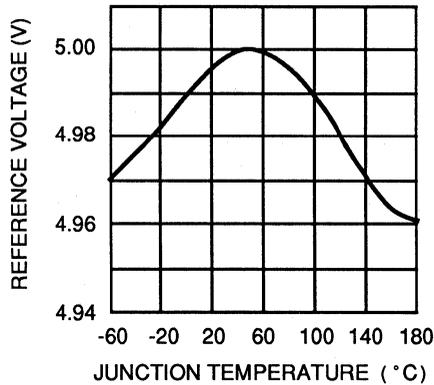
Error Amplifier Open Loop Gain and Phase Shift



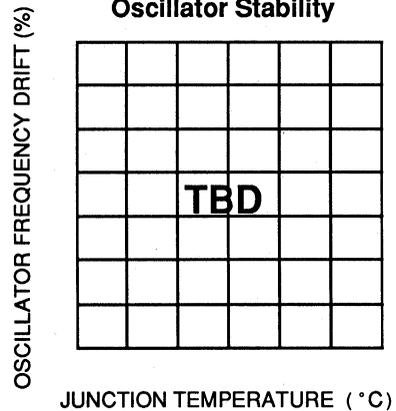
Minimum Operating Voltage vs Junction Temperature



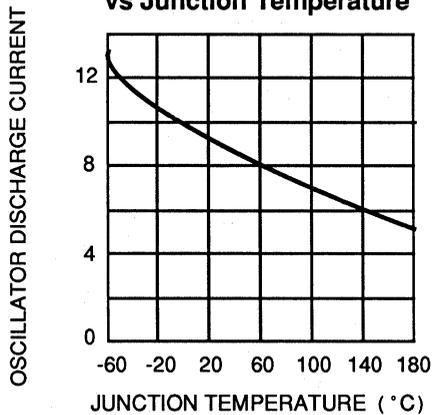
Reference Voltage vs Junction Temperature



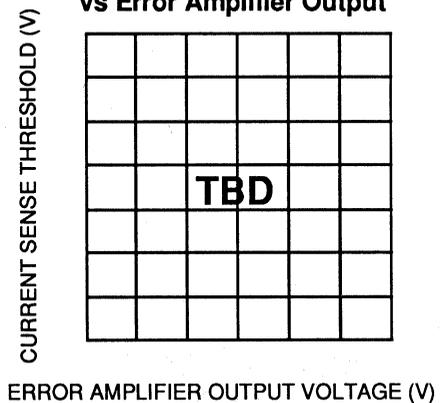
Oscillator Stability



Oscillator Discharge Current vs Junction Temperature



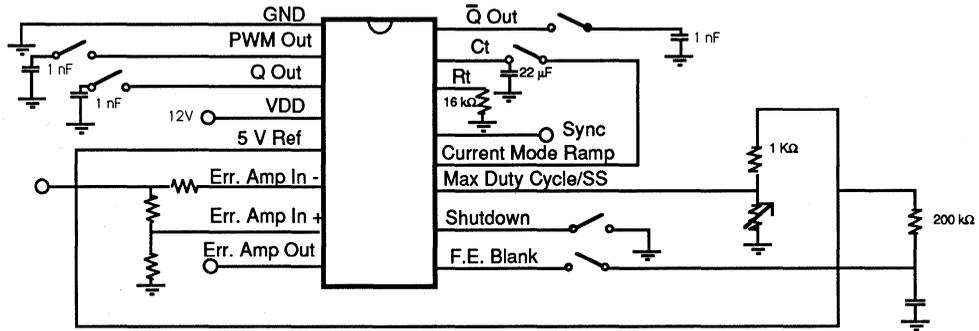
Current Sense Threshold vs Error Amplifier Output



Pin Description

Pin Number	Pin Name	Pin Function
1	Ground	
2	PWM Out	Totem pole output stage with variable duty cycle
3	Q Out	Totem pole output stage designed for 50% duty cycle operation, for use with a push-pull, half, or full bridge stage
4	V _{DD}	Supply pin
5	5 V reference	Bandgap reference pin; provides a 5-volt reference voltage trimmed to 2% accuracy. It can be used as a 5 V source for other parts of the circuitry.
6	Error Amplifier in -	Inverting input to the error amplifier. The biasing scheme used will determine polarity of the power supply .
7	Error Amplifier in +	Noninverting input to the error amplifier.
8	Error Amplifier out	Filters placed on this pin can be used to tailor the open loop gain or frequency reponse of the error amplifier.
9	F.E. Blanking	This pin is used to set the turn-on delay such that initial system transients due to device parasitics do not trip the over current sense. This time constant is selected via the size capacitor placed on this pin (see corresponding characteristic curve).
10	Shutdown	A low level signal applied to this pin will shut down the device outputs. This pin should be grounded during normal operation.
11	Max Duty Cycle	The voltage applied to this pin controls the max duty cycle (conversely deadtime). See Applications Information.
12	Current Mode Ramp	This pin is the noninverting input to the PWM op amp, and is used to select current vs. voltage mode operation. If voltage mode operation is desired, pin 15 (oscillator capacitor) is tied together with this pin.
13	Synch	This pin can be tied to other devices to generate a master system clock.
14	R _T	Oscillator timing resistor
15	C _T	Oscillator timing capacitor
16	\bar{Q} Out	Totem pole output stage designed for 50% duty cycle operation that is 180 degrees out of phase with Q Out for use as the other side of the push-pull, half, or full bridge stage

Test Circuit



Applications Information

Functional Description (Refer to Functional Diagram)

The basic function of the MIC3830 can be described as follows: A sawtooth waveform is fed to the noninverting input of one of two PWM comparators where it is compared against the output of an error amplifier, which is simply an op amp that compares the output voltage of the power supply with an externally supplied reference voltage (the reference voltage pin may be used). This sawtooth waveform can be generated by the internal oscillator (voltage mode control) or fed back from the output inductor (current mode control). The output of this comparator is a square wave. This square wave is NOR'ed with the output of another comparator which will be low if either the undervoltage lockout or the soft start functions have been activated (less than 10V on the input, or 1.25 V across an externally supplied sense resistor will trip each, respectively). The resulting signal is then subjected to two more levels of logic gates, which perform the front edge blanking and overcurrent protection functions, respectively (a one shot is used to provide for turnon delay, and 1.0 V sensed across an externally supplied resistor will trip the overcurrent sense function). This signal, controllable in duty cycle by the max duty cycle input (which forms the inverting input to the second PWM comparator if soft start or UVLO are not activated), then drives the main output stage. This output is intended to drive the main converter stage of the compound topology system.

The two 50 % duty cycle stages are driven by the Q and \bar{Q} outputs of the second of two cascaded "divide-by-two" T-flip-flops. These are used to ensure that the two outputs are always 180 degrees out of phase. The internal oscillator provides the T inputs to each of the FFs. These two outputs are primarily intended to drive power transistors for push-pull, half or full bridge inverter stages. They operate at 1/4 the total system frequency.

Each output stage is a sturdy totem pole configuration, with 1.0 A peak current capability.

CURRENT VS VOLTAGE MODE CONTROL

Current mode control is a method of using the output inductor current waveform (which happens to be a sawtooth), instead of generating a sawtooth waveform internally. It is preferable to voltage mode control as it provides more instantaneous feedback from the output stage, limits peak switching transistor current, removes one pole from the output which simplifies compensation in the negative feedback stage, provides an automatic input voltage feedforward which results in good rejection of input line transients, and results in symmetrical flux excursion (for push-pull stage), eliminating the problem of core saturation. Current mode control is achieved in the MIC3830 by using the current mode ramp pin to input the inductor current.

If voltage mode control is desired, the current mode ramp pin is tied to the C_T pin. The internal oscillator is programmable up to 500 kHz by selection of the appropriate resistor and capacitor.

A more detailed look at each of the pertinent sections is given below.

OSCILLATOR

The oscillator stage serves two functions, first is to provide the linear sawtooth waveform fed to the PWM comparator in voltage mode control. Secondly, it toggles the flip-flop which provides the Q and \bar{Q} outputs. The frequency of oscillation is externally programmed via the choice of timing resistor and capacitor. A nominal voltage of 3.6 V appears on the R_T pin; the resulting current is then mirrored through the C_T pin which charges the timing capacitor and generates the linear ramp. It is important to select an appropriate capacitor; at high frequencies effective series resistance, effective series inductance, dielectric loss and dielectric absorption all affect frequency stability and accuracy. RF capacitors such as silver mica, glass, polystyrene, or COG ceramics are recommended. High K ceramics should not be used. The SYNC output of this stage allows two or more MIC3830s to be

connected together with one master system clock. The oscillators in the slave units are disabled by grounding C_T and connecting R_T to the 5V reference pin. It is important to keep such cascaded units as close together as possible to minimize transmission line effects.

ERROR AMPLIFIER

The error amplifier is an op amp with a low impedance output that is used to sense output conditions and provide a DC output based on those conditions to the PWM comparator. The output of this stage is provided externally such that the closed loop gain or frequency response of the system can be tailored. The open loop gain of this stage is typically 90 dB. It can be reduced simply by putting a load resistor on the error amp output pin.

VOLTAGE REFERENCE

This section consists of a 5 V bandgap reference internally trimmed to 2% accuracy over temperature. It provides not only an internal 5 V reference, but can be used to supply 5 V to other parts of the system. If desired, this can be bypassed by connecting the V_{REF} and the V_{CC} pins together.

PWM COMPARATORS

Each comparator compares two signals; the first compares a sawtooth waveform with the output of the error amplifier. The second compares the max duty cycle input (which allows tailoring of the resultant duty cycle, if soft or UVLO are not active) with the sawtooth. Both of these outputs are NOR'ed together; this final output square wave is used to drive the main output stage.

OVERCURRENT SENSING

Overcurrent sensing and shutdown is accomplished via an external sense resistor connected from the switching element to ground. This voltage is then fed into the noninverting input of a sensing comparator. The inverting input is set to 1.0 V internally; if the voltage sensed equals or exceeds 1.0 V, the corresponding input to the logic gates is pulled low, and the PWM comparator output is overridden.

SOFT START

This feature operates in the same manner as the overcurrent sensing, except that it does not trip until the sensed voltage reaches 1.25 V. When this feature is active, the PWM comparator output will ramp up slowly, with a time constant determined by the size of external capacitor chosen on the current limit/SS pin. This feature prevents damage due to large inrush currents generated when the device attempts to restart after having been shut down by the current limit function.

UNDERVOLTAGE LOCKOUT

Undervoltage lockout is accomplished by means of a Schmitt trigger in which the inverting input is tied to V_{CC} and the noninverting input is tied to an internally generated 16 V supply. A 28 V zener clamp is used between the inverting input and ground which clamps the input voltage to 28 V max. The undervoltage lockout feature with hysteresis prevents spurious turnons at insufficient voltages. A voltage of greater than 10V is required for turnon.

OUTPUT DRIVERS

The output drivers are totem pole stages designed to sink and source 1.0 A peak current. This peak current was chosen to provide the designer with the option of using bipolar, MOSFET, or IGBT switching elements. To minimize ringing on the output waveform, the series inductance seen by the drivers should be as low as possible. This can be accomplished by keeping the distance between the MIC3830 and the switching elements as short as possible, or using carbon composition series damping resistors.



MIC5009CN

Counter Time-Base Circuit

General Description

The MIC5009 is a highly versatile MOS oscillator and divider chain manufactured by Micrel using a depletion-load ion-implantation process and P-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8 . The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination, the internal oscillator with an external crystal, or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

The MIC5009 consists basically of a series of counters, selected via an internal multiplexer. The $+10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

With an input frequency of 1MHz, the MIC5009 provides the basic time periods necessary for most frequency measuring instruments, i.e., $1\mu\text{s}$ through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1MHz input. Using a 1/1.2 MHz input, the MIC5009 can also provide a 50/60Hz output for accurate generation of line frequencies in portable instruments or clocks.

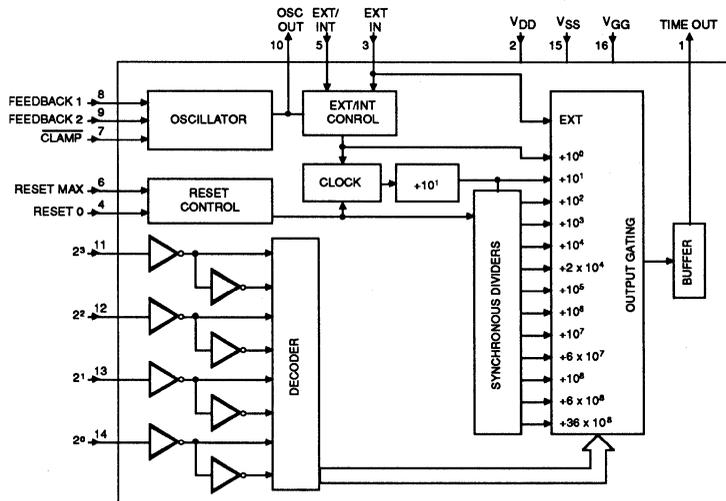
Features

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
 - External signal
 - External RC network
 - External crystal
- Operates DC to above 1MHz
- Binary-encoded for frequency selection
- Resettable to highest or lowest state
- Twenty different modes of division

Ordering Information

Part Number	Temperature Range	Package
MIC5009CN	0°C to 70°C	16-pin Plastic DIP

Functional Diagram



Pin Configuration

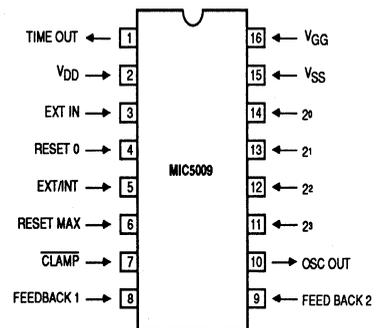


Figure 1

The time-base output (TIME OUT) is a square wave; its frequency is determined by the selected counter division, and by the oscillator or external input frequency. The falling edge of the output square wave should be used to control external circuitry.

Division Modes vs. Control Inputs

Table 1

DIVISION SELECTORS				NORMAL Mode 0 $R_{MAX} = 0$ $R_0 = 0$	BYPASS MODES		
2^3	2^2	2^1	2^0		Mode 1 $R_{MAX} = V_{GG}$ $R_0 = 0$	Mode 2 $R_{MAX} = 0$ $R_0 = V_{GG}$	Mode 3 $R_{MAX} = V_{GG}$ $R_0 = V_{GG}$
0	0	0	1	$+ 10^1$	$+ 10^1$	$+ 10^1$	$+ 10^1$
0	0	1	0	$+ 10^2$	$+ 10^2$	$+ 10^2$	$+ 10^2$
0	0	1	1	$+ 10^3$	$+ 10^3$	$+ 10^3$	$+ 10^3$
0	1	0	0	$+ 10^4$	$+ 10^4$	$+ 10^4$	$+ 10^4$
0	1	0	1	$+ 10^5$	$+ 10^2$	$+ 10^5$	$+ 10^2$
0	1	1	0	$+ 10^6$	$+ 10^3$	$+ 10^6$	$+ 10^3$
0	1	1	1	$+ 10^7$	$+ 10^4$	$+ 10^7$	$+ 10^4$
1	0	0	0	$+ 10^8$	$+ 10^5$	$+ 10^5$	$+ 10^5$
1	0	0	1	$+ 6 \times 10^7$	$+ 6 \times 10^4$	$+ 6 \times 10^4$	$+ 6 \times 10^1$
1	0	1	0	$+ 36 \times 10^8$	$+ 36 \times 10^5$	$+ 36 \times 10^5$	$+ 36 \times 10^2$
1	0	1	1	$+ 6 \times 10^8$	$+ 6 \times 10^5$	$+ 6 \times 10^5$	$+ 6 \times 10^2$
1	1	1	0	$+ 2 \times 10^4$	$+ 2 \times 10^1$	$+ 2 \times 10^1$	$+ 2 \times 10^1$

* SPECIAL ADDRESSES:

- 0000 - Oscillator signal selected by EXT/INT appears at TIME OUT
- 1100 or 1101 - Forces TIME OUT to logic 0 level
- 1111 - Signal at EXT IN appears at TIME OUT
- Logic 1 = High = V_{SS}
- Logic 0 = Low = V_{DD}

RC Operation

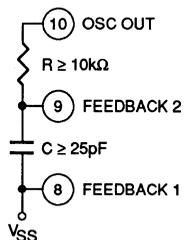


Figure 3

Crystal Operation

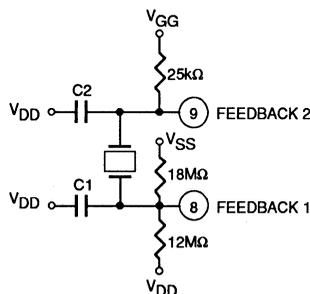


Figure 4

Functional Description

TIME OUT, Pin 1

TIME OUT is the output of the divider chain. It is a square wave whose period depends upon the division mode. For this reason, external circuitry should be triggered on the falling edge of this signal.

V_{DD}, Pin 2

V_{DD} is normally ground for the chip and the other supply voltages are measured with respect to V_{DD}.

EXT IN, Pin 3

When using an external frequency source to operate the MIC5009, the signal should be applied at EXT IN and EXT/INT should be brought to a logic 1 level. The counters are incremented on the falling edge of EXT IN and the signal applied to this pin must be TTL-compatible. When unused, this pin can be tied either high or low.

RESET 0, Pin 4

A positive going pulse of 10 μ S or longer applied to RESET 0 will reset the counters to their lowest state. Taking RESET 0 to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes according to Table 1.

EXT/INT, Pin 5

A logic 1 level on EXT/INT will gate the signal present at EXT IN through to the counters. A logic 0 level applied to EXT/INT will gate the internal oscillator (RC/crystal) through to the counters.

RESET MAX, Pin 6

A positive going pulse of 10 μ S or longer on RESET MAX will reset counters to their highest state. RESET MAX enables the user to set up the counters to provide a falling TIME OUT edge at the next oscillator cycle or negative going EXT IN, regardless of which divider chain is selected.

Taking RESET MAX to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes given in Table 1.

CLAMP, Pin 7

CLAMP is used in conjunction with the RC mode of operation. Its purpose is to provide accurate start-up operations.

When CLAMP is taken to a logic 0 level, the internal circuitry is held at a fixed reference voltage. Then, when CLAMP is taken to a logic 1 level, the oscillator's first cycle will be a full cycle.

FEEDBACK 1 and FEEDBACK 2, Pins 8 and 9

FEEDBACK 1 and FEEDBACK 2 are oscillator ports. Operation in the RC mode is achieved as shown in Figure 3. Frequency is approximately $0.8/RC$. R must be greater than or equal to 10k Ω and C must be greater than or equal to 25 pF for proper operation. Operation in the crystal oscillator

mode is shown in Figure 4. The crystal operates in the parallel resonant mode, should operate properly with a 5mW drive, and should have a loading capacitance (C_L) of ≤ 32 pF. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. The series combination of C1 and C2 should not exceed the value of C_L.

OSC OUT, Pin 10

The oscillator output, provided at Pin 10, is not a true logic output but may be used to drive a high impedance device such as other MOS circuitry. OSC OUT reflects the state of the internal oscillator.

2³, 2², 2¹, and 2⁰, Pins 11 through 14

The division selector inputs are used to select the ratio of the TIME OUT frequency to the oscillator input frequency. The effect of specific combinations of logic levels on these pins is shown in Table 1. Note that when all division selector inputs are high, the signal applied to EXT IN appears at the TIME OUT output. Also when RESET 0 and RESET MAX are used in conjunction with the division selector inputs, several more modes can be accessed. (See Table 1.)

V_{SS}, Pin 15

V_{SS} is the positive supply voltage and should be maintained at 5 V_{DC} \pm 10% with respect to V_{DD}.

V_{GG}, Pin 16

V_{GG} is the negative supply voltage and should be maintained at -12Vdc with respect to V_{DD}.

Figure 5 shows a very simple test circuit which demonstrates the MIC5009 in the crystal oscillator mode. The division selector switches control the divide mode. The output frequency will be related to the 1MHz oscillator frequency according to Table 1.

Simple Test Configuration

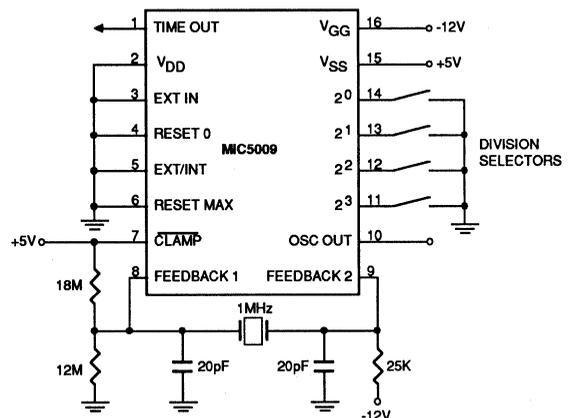
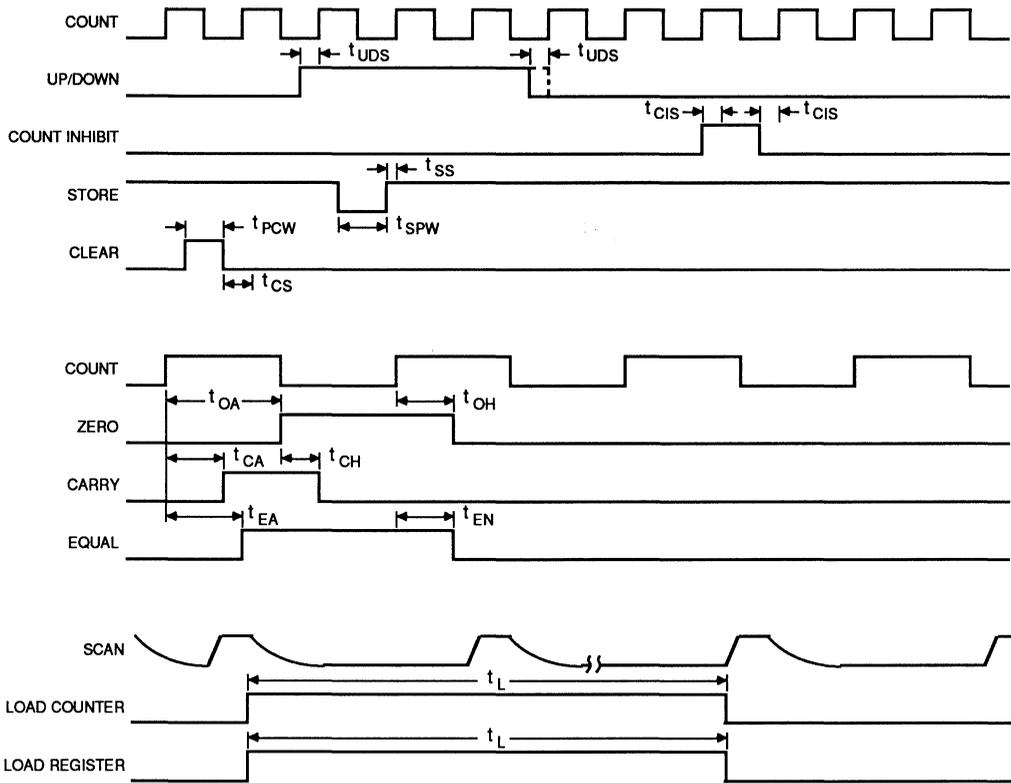
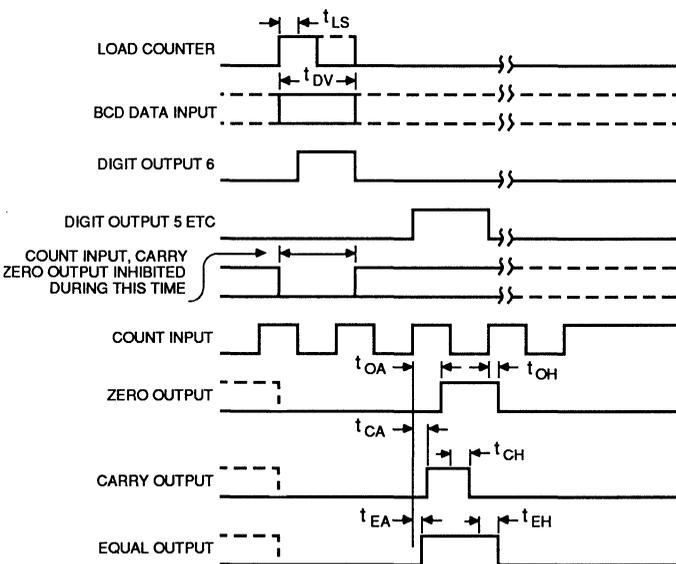


Figure 5

Timing



Loading Counter, Register (1 Digit)



t_{LS} 2.0 μ Smin

NOTE: REF. TO POSITIVE TRANSITION OF DIGIT OUTPUT

t_{DV} 2.0 μ S min

NOTE: REF. TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:
The inhibit function of the zero or equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 μ S prior to a positive transition of a digit output. This same timing restriction holds for Equal and Load Register.

Absolute Maximum Ratings*

Voltage on Any Terminal Relative to V_{SS}	+0.3V to -20V
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range (Ambient)	-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics - DC

($V_{SS} = +5V \pm 10\%$; $V_{DD} = 0V$; $V_{GG} = -12.0V \pm 20\%$; $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{SS}	Supply Voltage	+4.5		+5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	-9.6		-14.4	V	
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
R	Feedback Resistance	0.1		2.5	M Ω	Figure 3
V_{IL}	Input Voltage, Logic 0, Reset Inputs Reset (Bypass Mode) All Other Logic Inputs	0.0 V_{GG}		0.8 $V_{GG} + 1.0$ 0.8	V V V	Note 2
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	$V_{SS} - 1.0$	V_{SS}	$V_{SS} + 0.3$	V	Note 2
I_{IL}	Input Current, Logic 0			-1.6	mA	Note 2; $V_I = 0.4V$
V_{OL}	Output Voltage, Logic 0			0.4	V	$I_{OL} = 1.6mA^*$
V_{OH}	Output Voltage, Logic 1	2.4			V	$I_{OH} = -40\mu A^*$

Electrical Characteristics - AC

($V_{SS} = +5V \pm 10\%$; $V_{DD} = -12.0V \pm 20\%$; $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted)

Symbol	Parameter	Min.	Typ.†	Max.	Units	Notes
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	dc		200	kHz	
f_{EXT}	External Frequency	dc		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, \overline{CLAMP}	$1/2f_{osc}$				Note 5
	EXT IN	200			nS	
t_{PH}	Logic 1 Pulse Width, EXT IN	200			nS	
	RESET MAX	10.0			μS	
	RESET 0	10.0			μS	
f_{STA}	Frequency Stability w/Volt. Change, RC Mode w /Temp. Change, RC Mode Crystal Mode		± 3.0 -0.2		%/V %/°C	Note 3 Note 4
t_{EE}	Jitter, Edge-to-Edge Variation			15	nS	Temp. & Supply Voltage Constant

NOTES:

- † Typical values at $V_{SS} = +5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, and $T_A = 25^\circ C$.
- Logic inputs at V_{SS} , output open-circuited. Each logic input (see Note 2) contributes an additional 1.6mA (max) to I_{SS} when at logic 0 level.
- Logic inputs are RESET MAX, RESET 0. Address inputs: EXT IN, EXT/INT, and \overline{CLAMP} .
- Frequency variations due to power supply changes only.
- Crystal mode stability is dependent upon crystal.
- Minimum logic 0 time at \overline{CLAMP} input is 50% of oscillator period ($f_{osc} = \text{oscillator frequency}$)

* V_{OH} , V_{OL} apply only to TIME OUT.



Micrel Services and Special Products

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Source for Mature or Discontinued Integrated Circuits	7-10
Radiation Hardened Integrated Circuits	7-15



Micrel Services and Special Products

Micrel Services and Special Products

Choice . . . the freedom to select what suits you best. The ability to choose is your reward when you go with Micrel. Whether you need full design and fabrication services, or a little relief for your fab or test facility during a peak production crisis, Micrel offers a wide range of choices to fulfill your digital and analog semiconductor processing requirements.

This section describes some of Micrel's service and special product offerings, including:

1. Custom IC Capability

Supporting processes for:

Bipolar

CMOS — Silicon Gate or Metal Gate

Merged technology (BiCMOS, BCD)

Custom Design Services

Internal design group — linear, digital

Process-qualified contract design services

2. Foundry Services

Processes optimized to customer recipes

Mil-Spec qualified

Full service

Process engineering

Prototype development

Production facility

3. IC Testing Services

Inspection

Upgrade screening (burn-in)

Class testing

Electrical test/sort

4. Source for Discontinued IC's

Micrel alternative to last-time-buy problem

Micrel alternative to OEM final-run problem

Extended-life Mil-Spec products

5. Radiation Hardened IC's

Custom IC Capability

Micrel provides a complete solution for custom product design and development of customer-specific ICs to Mil-Spec standards. Our IC design specialists have the experience, organization, and resources to deliver — from concept to production — fast turn-around, high-quality circuits for a wide variety of applications and processes.

Micrel has assembled a team of design specialists experienced in both digital and analog disciplines and industry-standard design rules. In addition to designing our own product line, this team has successfully generated microprocessor, memory, logic control and other designs for a broad range of custom, commercial, and military grade devices. They are uniquely qualified in combining digital, analog, and mixed-mode circuits for high-voltage and low-voltage integrated circuits.

Micrel has built a management team experienced in the implementation of high-yield designs. Micrel can take your project from any stage — functional specification, block diagram, circuit design, database tape or PG tape—to any desired level of completion — processed silicon, tested die or graded, packaged product.

Micrel has provided our design team with the latest CAD/CAM systems, engineering tools for circuit simulation, emulation, and verification, as well as complete foundry and test facilities that include electrical and environmental cycling.

In addition to the company's internal design staff, Micrel maintains on-going relationships with pre-qualified design consulting firms. The result is the ability to deliver, with maximum flexibility, short development-cycle IC's at very attractive prices.

Supported Processes

Micrel maintains a library of proven, high-yield, configurable processes for the following technologies:

Standard NMOS, CMOS, PMOS & Bipolar

Single or double CMOS — Silicon Gate or Metal Gate

Exclusive merged-technology — Bipolar/CMOS/DMOS (BCD)

These process libraries, which can help you get your design to market faster, are a direct result of Micrel's long experience in manufacturing the company's standard products and custom IC's in our own foundry. A detailed discussion of Micrel's process and foundry capabilities is provided later in this chapter.

The Leader in Smart Power Design

Micrel design specialists are experts in Intelligent Power technology. Through the company's experience in developing and producing our highly successful ASIS™ semiconductor product line, Micrel is now the leading source of design support for this fast growing IC market segment.

Micrel's expertise in interfacing low-voltage analog and digital signal processing circuits to high-voltage high-power electrical and electro-mechanical components makes us uniquely qualified. Micrel can help you provide cost-effective, reliable solutions for high-voltage interface applications in:

- Transportation
- Telecommunications
- Avionics
- Medical
- Industrial
- Computers
- Office automation
- Motor control
- Power supplies
- Solenoid/actuator control
- HV physiological stimulus
- Process control
- Peripheral drive control
- Print-head drivers
- Display Products
- Sensor Controllers
- Battery-powered vehicles

You're in Control

When you work with the Micrel custom design team, you retain control of your own product. Our engineers will work with you as technical consultants to help you determine the feasibility, production requirements and specifications of your project. Micrel's goal is to see that your specifications are met.

Micrel's designers will generate layouts and develop a database for your circuit using industry-standard design rules appropriate for the process technology being implemented. Prior to release, the circuit database is checked against your specification for electrical and design-rule violations until it is error-free.

Micrel's engineers review device characterization data and evaluate functional and parametric requirements to ensure compliance with your specification prior to approval of the prototype. Full functional and environmental parametric test programs, designed to your specifications, are used for final product testing.

Foundry Services

The Micrel Wafer Fab Division offers foundry services to commercial or military IC designers and manufacturers who seek a production solution compatible with their specific application or technology needs. The Micrel foundry provides a variety of wafer processing resources which can address your unique requirements for short runs or volume production of devices to 2 μ geometries.

Micrel has a modern fabrication facility using projection lithography (4 inch), positive or negative resist, all-dry-etch and "all-implanted" processing, in-house implant and sputtered metal, and has the capability to produce up to 10,000 wafers/month. Sophisticated measurement equipment is used to monitor and record line widths, particle levels, film thicknesses, and other important parameter; final electrical characterization of the wafer test die is provided by automated test equipment.

Micrel has combinations of design, process and foundry services that are sure to fit your exact needs. There are a number of options you can select from. Each choice is designed to match your specific situation or requirements to the appropriate Micrel solution:

- | | |
|-----------------|--|
| 1. Foundry | Micrel duplicates your process (COT) |
| 2. R&D Foundry | Micrel develops a new process to meet your unique need |
| 3. Semi-custom | Micrel's technology, your design, Micrel's process |
| 4. Custom | Your circuit, Micrel's technology, design, and process |
| 5. Full service | Your specification, Micrel's design, technology, process, test and packaging |

Micrel's Process Advantage

Micrel will optimize our process to your needs. This approach to contract foundry business stands apart from others in the industry. Because of Micrel's long-term expertise in foundry operations, and the company's stringent quality control and in-process test procedures, you don't have to modify your needs to match the company's foundry process.

For manufacturers looking to off-load excess production, this means that you can expect the same quality and performance from Micrel produced parts as from those produced in your own facility.

For developers looking for short production runs, this means that you don't have to compromise your design to achieve the prototype results you seek.

The Full Service Foundry

When you choose Micrel for your wafer fabrication needs, you get a full service foundry capable of providing engineering support for your product's design, process, production, packaging, and reliability requirements. The same technical staff that has made Micrel IC products world-renowned for innovation, quality and performance is available to assist you in evaluating your circuit design, process recipe or test system for your semiconductor devices.

Two examples of the Micrel foundry commitment to service are Computer Aided Design (CAD) support and customized test patterns. Micrel CAD support helps you with often overlooked tasks such as alignment marks and scribe lines. Micrel can also order your masks from the mask vendor and ensure that they are built correctly. Unlike most foundries, Micrel will match your layout rules or design requirements with a customized wafer test pattern. This gives you many practical advantages:

- **Yield Improvement/Process Development.** Custom test structures, equipped with Spreading Resistance Profile (SRP) bars and optimized for your particular product, streamline data collection and provide an accurate means of characterizing your process.
- **Correlation with Simulations.** Personalized test patterns provide custom geometry devices that can confirm CAD models. Breadboarding, reliability testing, and evaluating radiation hardened characteristics are other benefits.

You have a choice in selecting the classification and quality standards to which your devices are manufactured. The highly-effective Micrel Quality Program, used for the production of our own commercial ICs, is our default standard. You may also select upgrades to: industrial Class B, military Class S or Class B (MIL-STD-883) including full radiation hardening (RADHARD), or custom production requirements designed to your particular specification definitions.

Process Capabilities

A well documented and controlled computer generated process traveler gives Micrel the capability to run a wide variety of MOS and bipolar technologies to 2Å design rules. These include single and double metal, single and double poly, as well as special variations of field and gate oxides for linear and digital devices.

For analog devices, Micrel can add DMOS or bipolar devices to CMOS technologies, CMOS devices to bipolar technologies, thin-film resistors, zener-zap devices, special capacitors, and many other enhancements. Micrel technologies and specification controls produce devices over a broad range of performance capabilities:

Bipolar — 10, 20, 30, 40 Volts*

BiCMOS — 10, 20, 30, 40 Volts*

BCD — 10, 40, 70, 150 Volts*

CMOS Si Gate — 5, 10, 15, 20, 25 Volts*

CMOS Metal Gate — 5, 10, 20, 45, 60 Volts*

PMOS and NMOS Metal Gate — 5, 10, 20, 45 Volts*

The accompanying tables and summaries in this section provide some examples of the Micrel Wafer Fab Division process capabilities. While this information is comprehensive, it is not necessarily complete. Micrel continually reviews and updates its process and production capabilities as part of our commitment to keep pace with the leading edge of the semiconductor industry. For information on the company's most current processes and capabilities, contact your Micrel sales representative.

- * *Operating voltage. Maximum voltage is 30% to 100% higher.*

MICREL STANDARD PROCESSES AND TECHNOLOGY SUMMARY

[See legend for description of (1) through (10)]			(1) SPEC NO.	(2) BKDN V	(3) OX THK	(4) RST TYPE	(5) PLY NO.	(6) MTL NO.	(7) WELL TYPE	(8) LDD OPTN	(9) LOW V	(10) SCHKY OPTN	
2.0μ	POLY	GATE	CMOS	032	6.0	300	P	2	2	P	N	—	—
2.5μ	POLY	GATE	CMOS	026	7.0	350	P	2	2	P	N	—	—
3.0μ	POLY	GATE	CMOS	016	8.0	400	P	2	2	P	N	—	—
3.0μ	POLY	GATE	CMOS	2/25	8.0	400	P	2	1	P/N	N	—	—
4.0μ	POLY	GATE	CMOS	003	12	500	P	1	1	P	N	—	—
5.0μ	POLY	GATE	CMOS	005	16	750	P	2	1	P	N	—	—
5.0μ	POLY	GATE	CMOS	018	16	750	N	2	1	P	N	—	—
5.0μ	POLY	GATE	CMOS	027	18	750	P	2	1	P	Y	—	—
5.0μ	POLY	GATE	CMOS	028	30	1.0	P	2	1	P	Y	—	—
5.0μ	POLY	GATE	CMOS	031	20	750	P	2	1	P	Y	—	—
5.0μ	POLY	GATE	CMOS	044	20	750	P	2	1	P	Y	3.0	—
11.0μ	POLY	GATE	CMOS	019	30	1.7	N	2	1	P	N	—	—
7.0μ	POLY	GATE	NMOS	050	15	1.0	N	1	1	—	N	—	—
7.0μ	POLY	GATE	PMOS	034	25	1.2	P	1	1	—	N	—	—
EPI-20μ	POLY*	GATE	BCD	001	140	750	P	2	2	P	N	5.0	Y
EPI-14μ	POLY*	GATE	BCD	047	70	500	P	1	2	P	Y/N	—	—
5.0μ	METAL	GATE	CMOS	015	12	800	P	—	1	P	N	—	—
6.0μ	METAL	GATE	CMOS	017	15	800	P	—	1	P	N	—	—
6.0μ	METAL	GATE	CMOS	035	15	800	N	—	1	P	N	—	—
7.0μ	METAL	GATE	CMOS	029	18	1.0	N	—	1	P	N	—	—
8.0μ	METAL	GATE	CMOS	007	20	1.0	N	—	1	P	N	—	—
9.0μ	METAL	GATE	CMOS	009	25	1.2	N	—	1	P	N	—	—
11.0μ	METAL	GATE	CMOS	006	30	1.7	N	—	1	P	N	—	—
12.0μ	METAL	GATE	CMOS	008	35	1.7	N	—	1	P	N	—	—
16.0μ	METAL	GATE	CMOS	024	45	2.5	N	—	1	P	Y	8.0	—
5.0μ	METAL	GATE	NMOS	042	13	800	P	—	1	—	N	—	—
8.0μ	METAL	GATE	PMOS	043	18	1.2	N	—	1	—	N	—	—
10.0μ	METAL	GATE	PMOS	020	20	1.2	N	—	1	—	N	—	—
EPI—14μ	METAL*	GATE	BICMOS	041	40	1.2	P	—	2	P	N	11	Y
EPI—14μ			BIPOlar	014	40	—	N	—	1	—	—	—	Y
EPI—13μ			BIPOlar	014	30	—	N	—	1	—	—	—	Y
EPI—11μ			BIPOlar	014	20	—	N	—	1	—	—	—	Y
EPI—8μ			BIPOlar	014	10	—	N	—	1	—	—	—	Y

(* Documents controlled)

LEGEND

- (1) **Q/A Specification Number** 200-0XXX
- (2) **BREAKDOWN VOLTAGE:** BVdss at 1µA for MOS, LVceo at 1 mA for BiCMOS/Bipolar. In cases where multiple voltage devices exist, the highest voltage Spec is shown. Bipolar and BiCMOS processes have various options on base ohms/sq, BVEBO, BVCBO, and field thresholds.
- (3) **GATE OXIDE THICKNESS:** In Angstroms (kÅ if decimal included). If multiple oxides are used, the thinnest is shown.
- (4) **RESIST TYPE:** P for positive, N for negative. All negative processes can be converted to positive. Positive products must use projection master tooling. Negative products may use projection master or working plate tooling.
- (5) **NUMBER OF POLY LAYERS:** Any polysilicon gate process can have a double or triple poly option. Double metal processes are limited to two layers of poly only. Poly or sichrome resistors are available; consult Spec.#200-0045 for sichrome option.
- (6) **NUMBER OF METAL LAYERS:** Any process (including metal gate) may use double metal (2 layers poly max). Dry-etched narrow pitch metal, usually reserved for 3µ or less, process can be included with other processes also.
- (7) **WELL TYPE:** P for P-well, N for N-well. any process can be converted from pwell to nwell or vice versa. Most designers choose pwell in an attempt to better optimize K-prime ratios and pwell processes are better suited to N-on-N+ EPI options. Nwell processes are often chosen to take advantage of NMOS cell libraries existing on P (100) substrate processes.
- (8) **LDD:** Y for yes, N for no. Lightly doped drain (LDD) or some form of drain engineering is an option on all MOS or BiCMOS processes. It is typically used to extend operating voltage, improve output impedance, or reduce drain charge trapping.
- (9) **LOW VOLTAGE DEVICE:** The channel length (in drawn microns) of a low voltage device is shown when this exists. This option is typically used in analog-digital applications where the low voltage device is used for high density digital functions.
- (10) **SCHOTTKY:** Y for yes, — for "Not Applicable" Schottky option.

BIPOLAR, BICMOS TECHNOLOGY SUMMARY

EPI	TECHNOLOGY ¹	VOLTS LVCEO	NPN-BASE SHEET-P	POWER RANGE
14µ	Bipolar	40V	200 175 150 125	Low to High
14µ	BiCMOS	40V	175 125	Low to High Single/Double Metal
13µ	Bipolar	30V	200 175 150 125	Low to High
11µ	Bipolar	20V	200 175 150 125	Low to High
8µ	Bipolar	12V	200 175	Medium

- (1) All of the technologies listed above come with various complementary devices and process additions as noted in the following summaries.

CMOS PROCESSES

- Numerous digital and analog Si-gate technologies, from 2 μ /5V to 16 μ /45V
- Anisotropically etched contacts, down to 1.5 x 2 μ
- Anisotropically etched poly, pitch down to 4 μ (2 μ /2 μ)
- Chemically vacuum etched metal, pitch down to 7 μ
- Dry etched metal, pitch down to 6 μ
- RadHard CMOS Si gate technologies
- Super RadHard CMOS metal gate technologies
- CMOS metal gate technology, down to 5 μ /12V
- Double or triple Poly technology
- Nitride-on-oxide poly-to-poly capacitors
- Sichrome resistor capability, 2k ohm/sq (DAC's)
- LDD/MLDD processes for higher voltages
- DDD processes for higher voltages
- 3 μ and 5 μ extended-drain for higher voltage
- Cryogenic-optimized processes
- Buried and surface-channel CCD
- Double-poly EPROM technology
- Gate oxides, down to 200A
- KOH-etch capability for poly-on-nitride gates
- Transient-upset protected CMOS (Neutron-irradiation)
- N on N+ CMOS for latch-up reduction
- P on P+ CMOS for latch-up reduction
- Retrograde P-well for latch-up reduction
- Optical sensors with nitride-type anti-reflective coating
- Extended-drain CMOS for high-voltage (160V)
- Dielectric isolation capability/experience
- Buried-contact or buried-poly via capability
- CMOS-type Bipolar technology and buried Zeners
- Plasma nitride passivation option
- Military-style nitride-on-oxide metal gate technology
- 15 ohm to 1 megaohm/sq poly resistors (Stabilized)
- Low-noise processes
- Low-leakage processes
- Contrast-enhanced-material lithography
- Metal fuses

BIPOLAR PROCESSES

- Bipolar processes from 6 μ EPI/10V to 20 μ EPI/170V
- Schottky diodes available with Al, AlSi, AlCu, AlSiCu, or Pt/TiW/Al
- Platinum silicide/TiW technology available
- 2k Ω /sq sichrome resistor capability (DAC's)
- Optical sensors with nitride-type anti-reflective coating
- Dielectric isolation capability/experience
- Plasma nitride passivation capability
- Poly-interconnect, resistor, or field-plate option
- Washed-emitter technology
- Poly-emitter technology
- Characterized up/down isolation technology
- Pressure sensors, Hall-effect sensors, optical sensors
- 3 μ thick metal etch capability
- Low-noise processes
- Low-leakage processes
- Zener-zapping
- Metal fuses
- Implanted (Antimony) buried layer

BICMOS PROCESSES

- Metal gate CMOS along with power NPNs and power PNP
- Option to add metal gate LDMOS for no additional masks
- In P-well Si gate or metal gate CMOS technologies, a high performance vertical PNP (separate collector) may be added with one additional N base mask and is supported by predefined macros
- In P-well Si gate CMOS technology, a lateral NPN with good Beta and separate collector may be used and is supported by predefined macros
- BiCMOS options are available which are fully isolated (like Bipolar), just N-EPI on N+ starting material, or "No EPI"

DMOS PROCESSES

- Discrete devices up to 2 GHz and up to 300 watts
- Dual-well metal gate DMOS/CMOS technology to 80V
- D.I. version of DMOS/CMOS
- Lateral (Si gate or metal gate) or vertical DMOS

MICREL SI-GATE BIPOLAR-CMOS-DMOS (BCD)

- DMOS/HVPCH and bipolar transistors: 50V, 100V, or 200V
- High-voltage CMOS: 45V
- 6V, 7V, 8V Zeners/buried-Zeners
- Pre-tested analog/digital macros
- 5V-In to 200V-Out translators
- H-bridge capability (All-NCH)
- Double-poly high voltage nitride-on oxide capacitor technology
- Depletion devices
- High voltage resistors: 100V/200V
- High-efficiency voltage tripler
- Stabilized BiCMOS band-gap reference
- Over-temp/over-voltage capability
- Sense-FET capability (On-chip)
- Latch-up-proof process
- LDMOS and VDMOS on same wafer
- High voltage (100V/200V) gate VDMOS option
- Option for no-body-effect on VDMOS or HVPCH

Special Technologies

- Pressure transducer
- Optical sensors
- Hall effect devices
- Solar cells
- Focal plane
- Imaging
- CCD
- Very low threshold
- BiCMOS
- BiCMOS - DMOS (BCD)

IC Testing Services

Full-service IC screening and high-performance testing continues to be the very foundation of the business, as it has been since Micrel was first started in 1978. What this heritage means to you is an experienced team of experts provides you with high-quality off-load services for screening and testing of your commercial, industrial or military grade VLSI devices.

Over the years, Micrel has continually invested in equipment and facilities that assure you advanced capabilities for component inspection, upgrade-screening, wafer-sort, and electrical testing to meet industrial Class B or MIL-STD 883, Class B or Class S requirements. Micrel uses modern automated test equipment (ATE), wafer probe, and autohandling equipment available for high and low temperature production testing.

The choice Micrel offers to you is a facility capable of meeting your specific test needs, whatever they may be. Some of the leading semiconductor manufacturers in the world ship production wafers to Micrel for probe and ink services, thereby freeing large blocks of their own tester time for internal use. Research and development centers rely on Micrel to provide thorough testing of prototype design samples. Other manufacturers use Micrel to assemble, test, and provide 100% good parts (with performance data certification) for high reliability programs.

Customers like these, who have come to depend on Micrel as their reliable choice for test services, get the results they need because of the company's fundamental commitment to customer satisfaction. Micrel's excellent engineering support and quality control systems insure maximum die-per-wafer yield to exacting customer specifications.

Micrel's complete approach to product reliability means that included in testing services are:

- Automatic lead straightening
- Full ESD handling precautions
- Certificate of Compliance

The quick turn-around policy insures that you get the service you need to meet your customer shipment requirements.

As a full-service test facility, Micrel can provide as much capability as you need for your particular situation.

Incoming Inspection

Micrel can perform 100% (or sample) electrical test at any temperature from -65°C to $+150^{\circ}\text{C}$ using automatic device handlers with computer-controlled testers.

You can use Micrel's incoming inspection testing to insure that properly tested product reaches your assembly lines, thereby reducing rework cycles caused when problems go undetected. Quick turn-around times keep your inventory moving. Micrel engineering support will work with your vendors, when required, to solve testing or correlation problems.

Upgrade Screening

Perform burn-in and testing at hot and cold temperature extremes in order to increase your reliability factor on commercial product. Micrel can provide this logical alternative to purchasing Hi-Rel parts when they are not readily available. Sample testing of package-related tests is also available when hermetic packages are involved.

Raw Class Testing

Manufacturers may off-load excess testing requirements to Micrel for expert, quick-turn, initial test after assembly. IC's may be drop-shipped from overseas, then forwarded to a specified location after Micrel completes testing and lead straightening.

Micrel is fully qualified to provide an extension to your final test function when necessary to meet your customer demands. Micrel will develop test software and hardware as required, working with your engineering group or customer specifications. Then, Micrel will perform electrical screening to Class B, Class S or to your specification control drawing (SCD) requirements. Groups A, B, C, and D qualification or quality conformance inspection (QCI) as required, can be performed.

Micrel uses automatic handlers for all package types and stringent ESD precautions are in place from incoming acceptance to final ship.

Assembly and Test

Micrel offers a complete solution if your product requires an uncommon IC package that is not part of your generic part number standard. We will purchase die and packaging, assemble them to your requirements, then screen and test the parts to your specified quality level.

Assembly and test service procedures comply with our standard product quality requirements and customer specifications. Die and certification data from its manufacturer or distributor are visually inspected for acceptability prior to

assembly in the plastic or ceramic package that you specify. You may choose either aluminum or gold wire-bond material. Pre-cap visual inspection and certification is performed. Screening and testing is done to the Class S, Class B or SCD requirements that you specify.

The assembly and test program makes it possible for you to ship to your customer good parts with accompanying performance data or certification of compliance.

Test Services Summary

Device classes:	Microprocessors, memories, interface logic, linear, TTL, CMOS, ECL, HC/HCT logic, custom and semicustom logic
Electrical test:	Raw class and receiving inspection screening to generic or customer specifications
Wafer sort:	Electrical sort with individual wafer or wafer lot summaries
Burn-in:	Both static and dynamic
Lead straightening:	Both 300 mil and 600 mil packages
Environmental Test:	Stabilization bake, temperature cycle and quality conformance inspection
Military test:	Full MIL-STD 883C, Class S or Class B screening or commercial upgrading, automatic high/low temperature
Engineering test:	Device characterization, statistical data, histograms, schmoo plots, electrical failure analysis, and vendor qualification
Test software:	Over 600 programs currently available, custom test programming available for all IC products or discrete devices

Test Equipment (Partial list)

ATE Systems:	Fairchild Sentry 7, 3 ea. with five 60-pin test heads (4 high voltage, 1 low voltage)
	Fairchild Sentry 20, 2 ea. with four 60-pin test heads (1 high voltage, 3 low voltage)
	Fairchild Sentry 8, 1 ea. with one 120-pin test head for low voltage, and one 60-pin test head for high voltage
Wafer Probers:	Electroglass, 6 ea. hot chuck, 3, 4, and 5-inch wafers

Autohandlers:	MCT, 5 ea. DIP, 300 and 600 mil, (-55°C to +150°C) MCT, 1 ea. LCC/PLCC (-55°C to +150°C) Delta, 1 ea. DIP, hot/cold, 300, 400, 600 mil (-55°C to +150°C) Delta, 2 ea. Flat-pack, hot/cold, all sizes (-65°C to +150°C) PAE, 1 ea. DIP, hot rail (+25°C to +70°C)
Burn-in Ovens:	Criteria IV, 3 ea. dynamic (36 boards per system) AMT-14000, 1 ea. dynamic (56 boards per system) Blue-M, 3 ea. static (20 boards per system)
Temperature Cycle:	Blue-M, 1 ea. temperature cycling system, all package types (-65°C to +150°C)
Lead Straighteners:	ATM, 2 ea. for 300 and 600 mil packages

Micrel, The Source for "Mature" or Discontinued IC's

Micrel is the primary wafer foundry for processing mature or obsolete MOS technologies. Since 1981, the company has been processing wafers using tooling supplied by our customers, by previously qualified manufacturers, or by reverse engineering the design.

Micrel uses a program approach to solving discontinued product problems on a specific project basis. Micrel does not merely buy out a stock of old IC's and hope to sell them to the market. Micrel's program approach includes full responsibility for manufacturing a device from base tooling, processing the die, packaging the device according to customer performance requirements, and screening and testing the final part to customer specifications.

Micrel's program approach resolves problems you might face if you were attempting to deal with a discontinued IC situation on your own; problems such as, how to get a copy of the test program, or how to get the die bonded in a specified package configuration.

Micrel's experience in providing test and foundry services to the semiconductor industry makes us ideally suited to provide the exact solution you need to solve a specific discontinued IC situation. Micrel alternatives offers you a choice when faced with some of the scenarios common to the discontinued IC problem.

Making the Right Choice

There are four primary options that an IC Buyer should be considering when evaluating solutions to the impact of discontinued IC technologies and specific obsoleted IC.

Option 1 — Last Time Buy

The Last-Time or Life-Time-Buy option attempts to resolve the problem, usually unsuccessfully, by purchasing a quantity of ICs that fulfill all forecast production requirements, spares commitments and maintenance contracts. Wafer storage that prevents damage due to oxidation, environment or handling can be costly.

Since most government programs will not fund future undefined events, the risk is placed on the contractor. If you over-estimate, expenses can never be recovered. If you under-estimate, you risk losing follow-on production and spares orders (typically the most profitable of contracts).

This option can leave you short of parts later on.

Option 2 — Product Redesign

This option resolves the problem by eliminating the need for discontinued ICs. The system (or module) is redesigned using off-the-shelf, close to equivalent ICs.

For life-time procurements, the problems of spares logistics and maintenance commitments are significant. A redesigned module or product usually requires requalification of the system with inherent costs and risks based on the probability of success.

Another consideration for this option is the impact on new products. Technical resources that could be directed to new product development are directed to sustaining old product support and a window of market opportunity may be lost.

This option is costly, risky, and time consuming.

Option 3 — Emulation

This option resolves the problem by replacing the obsoleted IC with another equivalent in form, fit and function. The most common vehicle for this option is the gate array or standard cell IC. Basic parameter specifications are usually achievable. However, the IC is processed to a different technology and employs a different design layout which will effect inherent performance characteristics.

One of the tools for evaluating an equivalent IC is a schmoo plot, which is a graphic presentation of device performance boundaries, and is generated by varying combinations of test conditions simultaneously. The window or overlap of common performance characteristics can be established by laying out the plot of one device over the plot of the other device.

The performance overlap of two devices made with different technologies and layout design will be much smaller than the individual schmoo plots. This indicates the two devices will meet the inherent performance requirements, but are not equivalent in other circuit design criteria. The result may be that significant requalification costs are incurred to test the new IC in each circuit application.

This option is seldom the correct solution, as many IC's are custom designs.

Option 4 — The Micrel Solution

The Micrel solution resolves the problem by transferring the device technology to another manufacturer who is capable of running the applicable process and performing the test program conditions. This approach duplicates the qualified device by using the same design data base software, master tooling, process specification and test program. A duplicated device is assured by using the same starting material, working plates, process steps and test specifications.

The critical phase in this option is in securing the production tooling and test software from a qualified manufacturer. If the obsoleted IC is not readily available, the buyer should negotiate the tooling as a condition to the last-time-buy order. The qualified manufacturer is most cooperative at this time because the technology is current and takes less effort to accumulate the transfer package, plus he wants to maintain good customer relationships and at the same time give up responsibility for support of the product.

If design tooling is not available from the original manufacturer, Micrel can quote on reverse engineering the product from a photograph of the die. This may be a better, more cost effective solution than a complete redesign of a device function.

The time factor for bringing up a new product on a mature process is typically 3 to 6 months for prototype ICs. If reverse engineering is required, 6 to 9 months will be required to provide product. To assure a smooth transition to the new device source, the buyer should have a one (1) year supply of IC's to meet forecast requirements. This allows adequate time to evaluate the device in the system, qualify the device to meet contractual quality requirements and integrate the device into the production build cycle.

Using Micrel as your aftermarket IC manufacturer offers the best solution to the problem of discontinued IC's. As an alternate supplier of the duplicated device, the company offers the lowest cost-risk product with the highest probability of program success.

Micrel Semiconductor is an excellent choice as your aftermarket IC manufacturer. Since 1978, Micrel has provided engineering start-up, tooling, procurement and on-time deliveries of products previously discontinued. If you need obsoleted or discontinued IC's to keep older systems in production, or to maintain a spare parts inventory for maintenance, Micrel is the right choice to provide the answers to your problems.

MICREL "MATURE" PRODUCTS LIST

Part Number	Description	DIP Package	Notes
MIC2257	5/8 Serial to Parallel Receiver	24	1
MIC2259	5/8 Parallel to Serial Transmitter	28	1
MIC2260	5/8 Serial to Parallel Receiver	28	1
MIC2533	1K Static Shift Register	8	
MIC2534	2 x 512 Static Shift Register	8	
MIC2535	2 x 480 Static Shift Register	8	
MIC2827	2K Dynamic Shift Register	8	
MIC2833	1K Static Shift Register	8	
MIC2855	Quad 128 Bit Shift Register	16	
MIC2857	512 Bit Shift Register	8	
CD4000A	Dual 3 Input NOR/Inverter	14	2
CD4001A/B	Quad 2 Input NOR	14	2
CD4002A/B	Dual 4 Input NOR	14	2
CD4006A	18 Bit Static Shift Register	14	2
CD4007A/UB	Dual Complementary Pair + Inverter	14	2

MICREL "MATURE" PRODUCTS LIST (Continued)

Part Number	Description	DIP Package	Notes
CD4009A	Hex Inverting Buffer	14	2
CD4010A	Hex Buffer	14	2
CD4011A/B	Quad 2 Input NAND	14	2
CD4012A/B	Dual 4 Input NAND	14	2
CD4013A/B	Dual D Flip-Flop	14	2
CD4014A/B	8 Bit Static Shift Register	16	2
CD4015A/B	Dual 4-Bit Static Shift Register	16	2
CD4016A/B	Quad Analog Switch/Multiplexer	14	2
CD4017A/B	Decade Counter	16	2
CD4018A/B	Presetable Divide-by-N Counter	16	2
CD4019A/B	Dual AND/OR Select Gate	16	2
CD4020A/B	14 Bit Binary Counter	16	2
CD4021A/B	8 Bit Static Shift Register	16	2
CD4022A/B	Octal Counter	16	2
CD4023A/B	Triple 3 Input NAND	14	2
CD4024A/B	Seven Stage Ripple Counter	14	2
CD4025A/B	Triple 3 Input NOR	14	2
CD4027A/B	Dual J-K Flip-Flop	16	2
CD4028A/B	BCD-to-Decimal Decoder	16	2
CD4029A/B	Binary/Decade Up/Down Counter	16	2
CD4030A	Quad Exclusive OR Gate	14	2
CD4031A/B	64 Bit Static Shift Register	16	2
CD4034B	8 Bit Universal Bus Register	24	2
CD4035A/B	4 Bit Parallel Shift Register	16	2
CD4040A/B	12 Bit Binary Counter	16	2
CD4041A	Quad True/Complement Buffer	14	2
CD4042A/B	Quad Transparent Latch	16	2
CD4043A/B	Quad NOR R-S Latch	16	2
CD4044A/B	Quad NAND R-S Latch	16	2
CD4046B	Phase Locked Loop	14	2
CD4047B	Monostable/Astable Multivibrator	14	2
CD4048A/B	Expandable 8 Input Gate	16	2
CD4049A/UB	Hex Buffer	16	2
CD4050A/B	Hex Buffer	16	2
CD4051A/B	Analog Mux/Demux	16	2

MICREL "MATURE" PRODUCTS LIST (Continued)

Part Number	Description	DIP Package	Notes
CD4052A/B	Analog Mux/Demux	16	2
CD4053A/B	Analog Mux/Demux	16	2
CD4066A/B	Quad Analog Switch/Multiplexer	14	2
CD4069A/UB	Hex Inverter	14	2
CD4070B	Quad Exclusive OR	14	2
CD4071B	Quad 2 Input OR	14	2
CD4072B	Dual 4 Input OR	14	2
CD4073B	Triple 3 Input AND	14	2
CD4075B	Triple 3 Input OR	14	2
CD4076B	Quad D Register	16	2
CD4081B	Quad 2 Input AND	14	2
CD4082B	Dual 4 Input AND	14	2
CD4093B	Quad 2 Input NAND Schmitt Trigger	14	2
CD4094B	8 Bit Shift/Store Register	16	2
CD4099B	8 Bit Addressable Latch	16	2
CD40106B	Hex Schmitt Trigger	14	2
CD40160B	BCD Counter	16	2
CD40161B	Binary Counter	16	2
CD40162B	BCD Counter	16	2
CD40163B	Binary Counter	16	2
CD40174B	Hex D Flip Flop	16	2
CD40192B	Decade Up/Down Counter	16	2
CD40193B	Binary Up/Down Counter	16	2
CD4510B	BCD Up/Down Counter	16	2
CD4512B	8 Channel Data Selector	16	2
CD4514B	4 Bit Transparent Latch	24	2
CD4515B	4 Bit Transparent Latch	24	2
CD4516B	Binary Up/Down Counter	16	2
CD4518B	Dual BCD Up Counter	16	2
CD4520B	Dual Binary Up Counter	16	2
CD4528B	Dual Monostable Multivibrator	16	2
CD4584B	Hex Schmitt Trigger	14	2
CD4724B	8 Bit Addressable Latch	16	2
MIC5009	Counter/Time Base	16	1
MM54C04	Hex Inverter	14	2

MICREL "MATURE" PRODUCTS LIST (Continued)

Part Number	Description	DIP Package	Notes
MM54C09	Quad 2 Input AND Gate	14	2
MM54C14	Hex Inverting Schmitt Trigger	14	2
MM54C42	BCD to Decimal Decoder	16	2
MM54C85	4 Bit Magnitude Comparator	16	2
MM54C86	Quad 2 Input Exclusive OR Gate	14	2
MM54C160	Synchronous Decade Counter	16	2
MM54C161	Synchronous Binary Counter	16	2
MM54C162	Synchronous Decade Counter	16	2
MM54C163	Synchronous Binary Counter	16	2
MM54C164	8 Bit Serial In/Parallel Out	14	2
MM54C173	Quad D Flip Flop	16	2
MM54C174	Hex D Flip Flop	16	2
MM54C175	Quad D Flip Flop	16	2
MM54C192	Synchronous Decade Up/Down Counter	16	2
MM54C193	Synchronous Binary Up/Down Counter	16	2
MM54C200	256 Bit RAM	16	2
MM54C240	Inverting Octal Buffer	20	2
MM54C244	Octal Buffer	20	2
MM54C374	Octal D Flip Flop	20	2
MM54C901	Hex Inverting Buffer	14	2
MM54C902	Hex Buffer	14	2
MM54C903	Hex Inverting Buffer	14	2
MM54C904	Hex Buffer	14	2
MM54C905	12 Bit Successive Approximation Register	24	2
MM54C906	Open Drain Buffer	14	2
MM54C907	Open Drain Buffer	14	2
MM54C914	Hex Schmitt Trigger	14	2
MM70C96	Hex Inverting Buffer	16	2
MM70C98	Hex Inverting Buffer	16	2
MM78C29	Quad Single Ended Line Driver	14	2
MM78C30	Dual Differential Line Driver	14	2

Note 1: Parts available in Plastic DIP or in ceramic DIP screened to Class B on special order.

Note 2: Radiation hardened CMOS devices. Some devices require a non-recurring set up charge. Contact Micrel for further information.

Radiation Hardened IC's

Micrel has been processing radiation hard CMOS metal gate logic since 1986, when NSC and Micrel initiated a technology and product transfer agreement. Micrel manufacturers megarad hardened Metal Gate devices such as the NSC and RCA CD4000 series logic. We can process these die to full MIL-SPEC 883, Class B or S requirements.

General Electric was Micrel's first significant customer, requiring a Class S, 1 megarad, 54C244 Octal Buffer Driver in a 20-lead flatpak for the MilStar program. Since then, Micrel has supplied radiation hardened IC's to the major U.S. military and aerospace manufacturers.

The following parts have been qualified to Mil-STD-883C Class B or S and are generally available from production stock. These parts are qualified to 1 megarad total dose, and Class S or B depending on the customer's requirements.

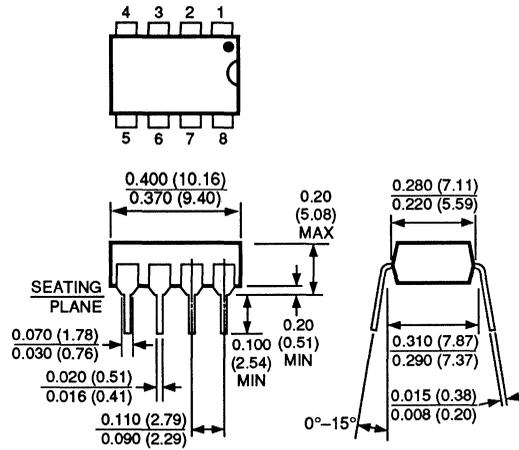
<u>Part Number</u>	<u>Description</u>	<u>Package</u>
MIC54C14JBR	Hex Schmidt Trigger	14
MIC54C157JBR	Quad 2 Input Multiplier	16
MIC54C85JBR	4 Bit Magnitude Comparator	16
MIC54C174FSR	Hex D Flip Flop	16
MIC54C244FSR	Octal Buffer and Line Driver	21
MIC54C905JSR	12 Bit Successive Approximation Buffer	21
MIC54C906JBR	Hex Open Drain N Channel Buffer	14
MIC54C922JBR	Keyboard Encoder	20
MIC54C941JBR	Octal Buffer/Line Receiver/Line Driver	20



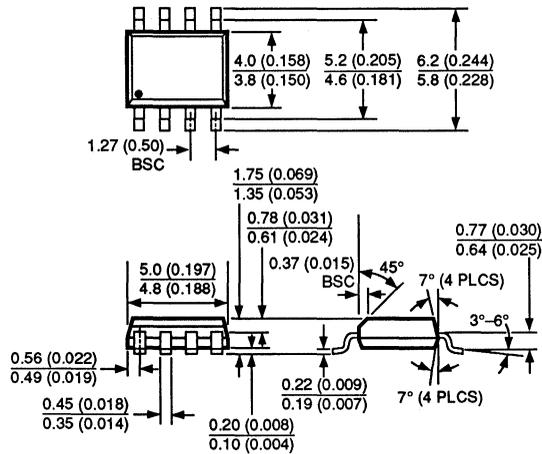
SECTION 8: PACKAGING INFORMATION

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8-Pin DIP	8-2
8-Pin SOIC	8-2
8-Pin CerDIP	8-3
14-Pin Plastic DIP	8-3
14-Pin SOIC	8-4
14-Pin CerDIP	8-4
16-Pin Plastic DIP	8-5
16-Pin SOIC Wide	8-5
16-Pin CerDIP	8-6
18-Pin Plastic DIP	8-6
18-Pin CerDIP	8-7
20-Pin Plastic DIP	8-7
20-Pin LCC	8-8
22-Pin Plastic DIP	8-8
24-Pin Plastic DIP	8-9
28-Pin Plastic DIP	8-9
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44-Pin Gull Wing QFP	8-12
44-Pin LCC	8-12
44-Pin Quad PAC	8-13
48-Pin Plastic DIP	8-13
52-Pin Gull Wing QFP	8-14

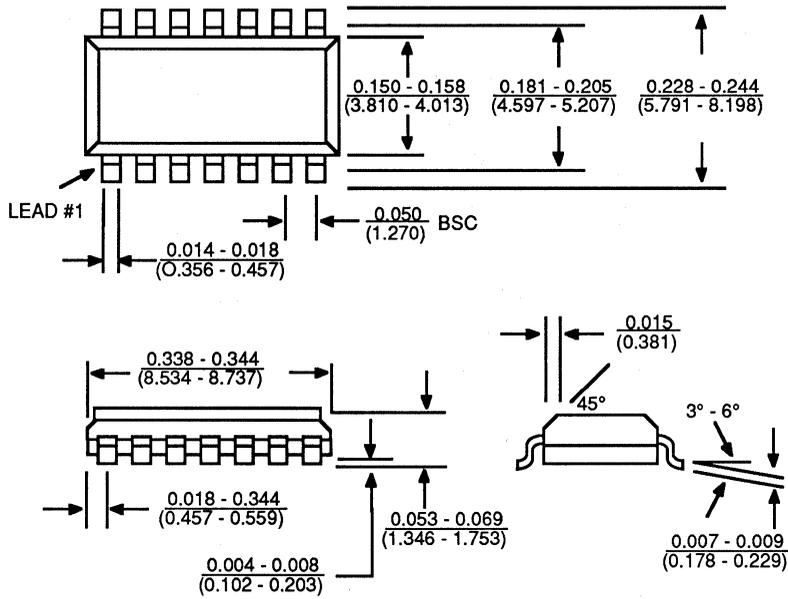
8-Pin DIP (N)



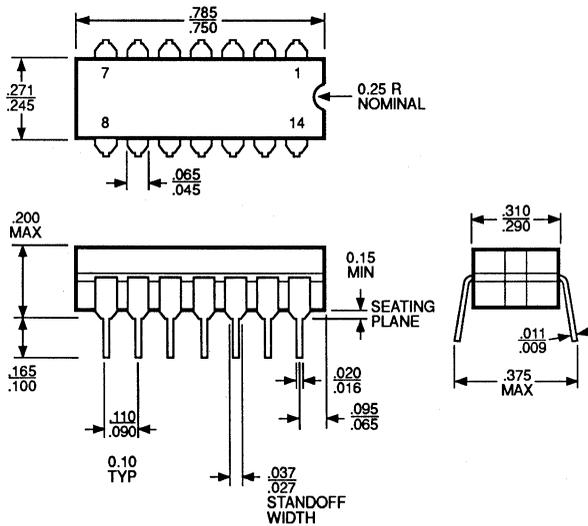
8-Pin SOIC (M)



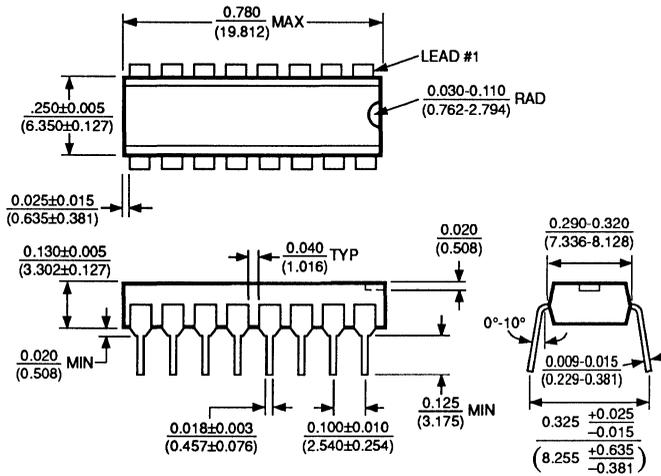
14-Pin SOIC (M)



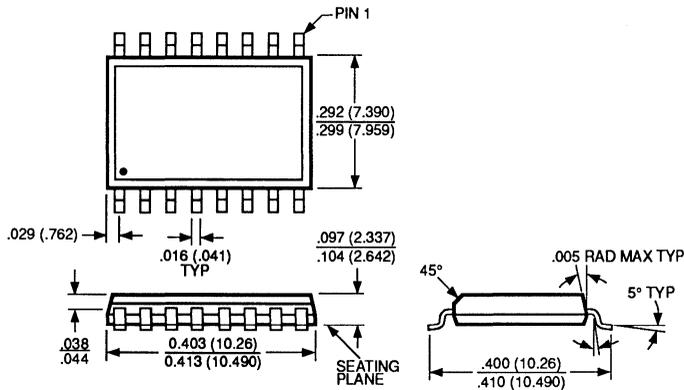
14-Pin CerDIP (J)



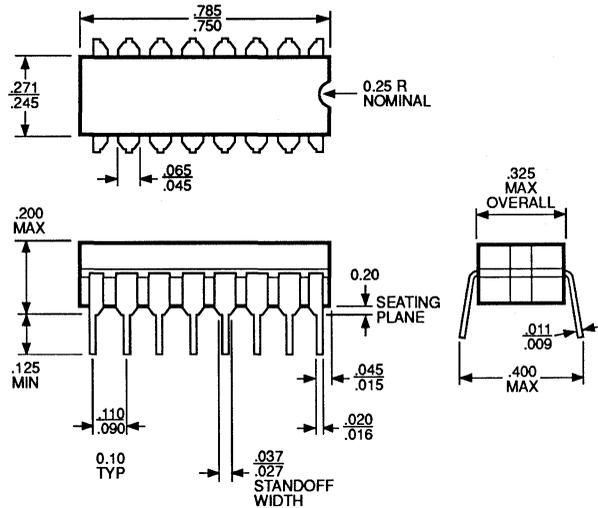
16-Pin Plastic DIP (N)



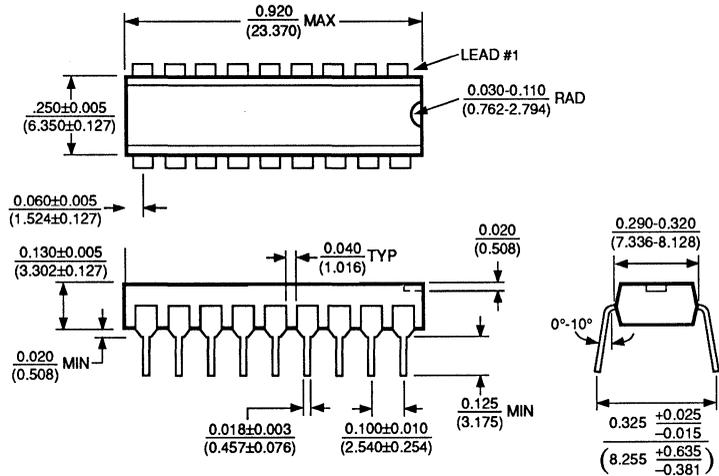
16-Pin SOIC (Wide) (WM)



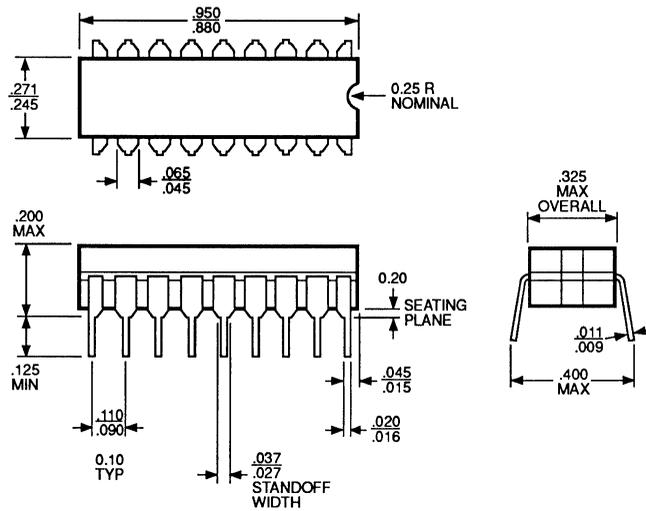
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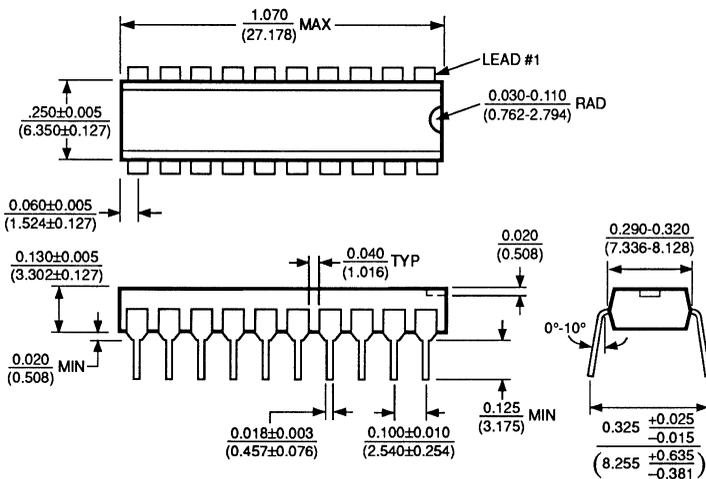
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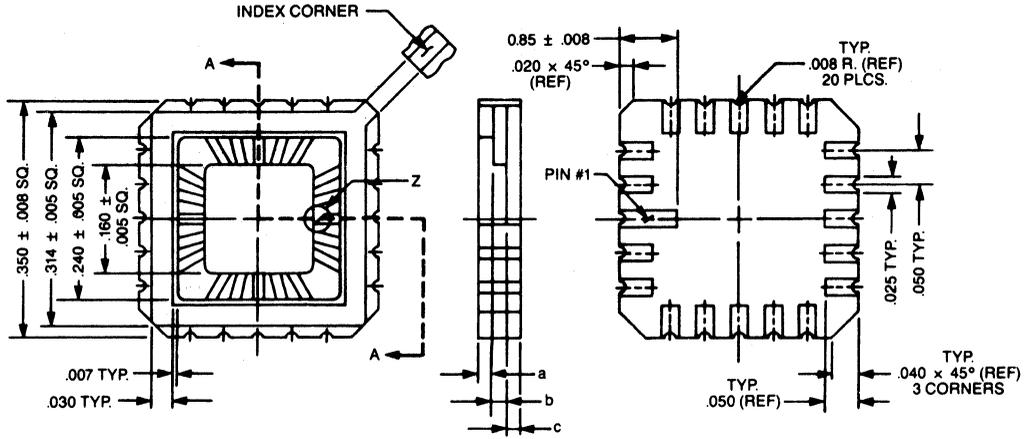
18-Pin CerDIP (J)



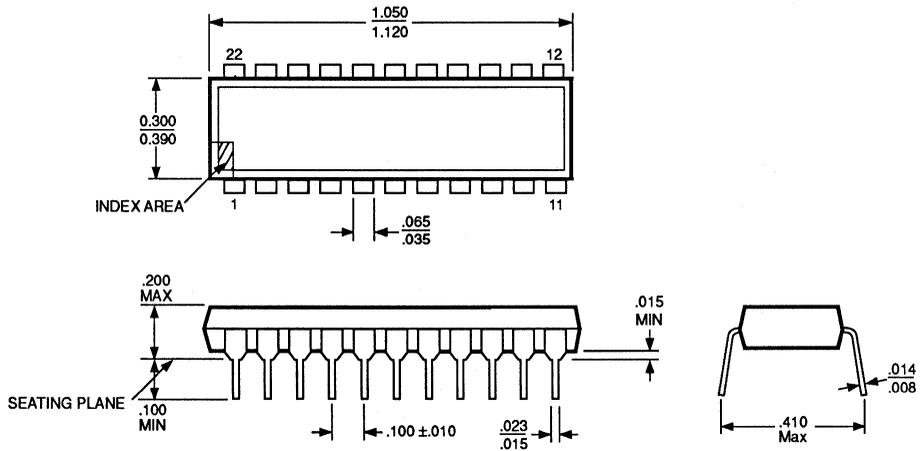
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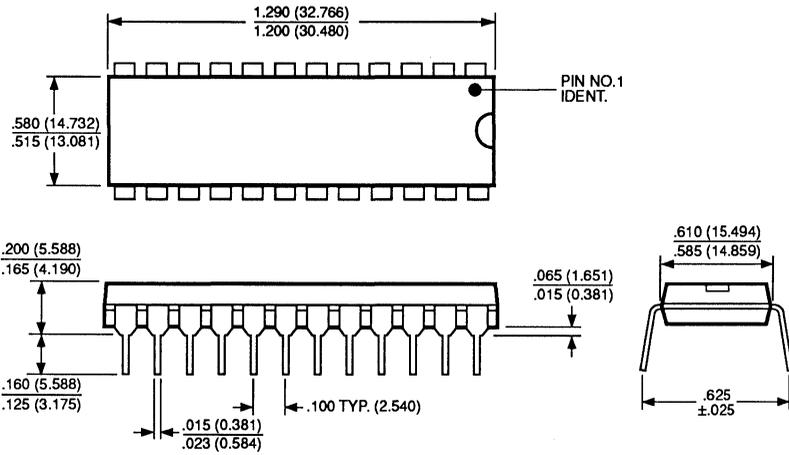
20-Pin LCC (L)



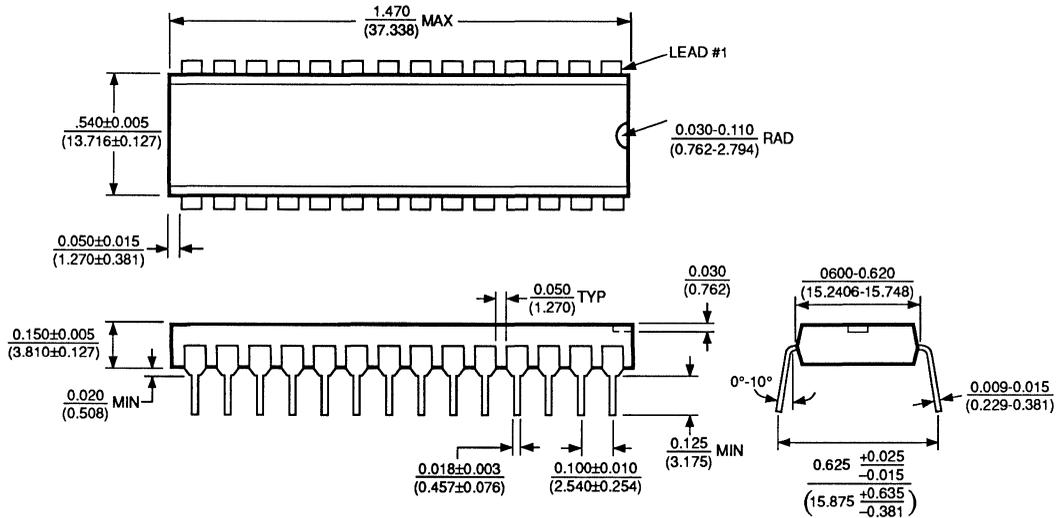
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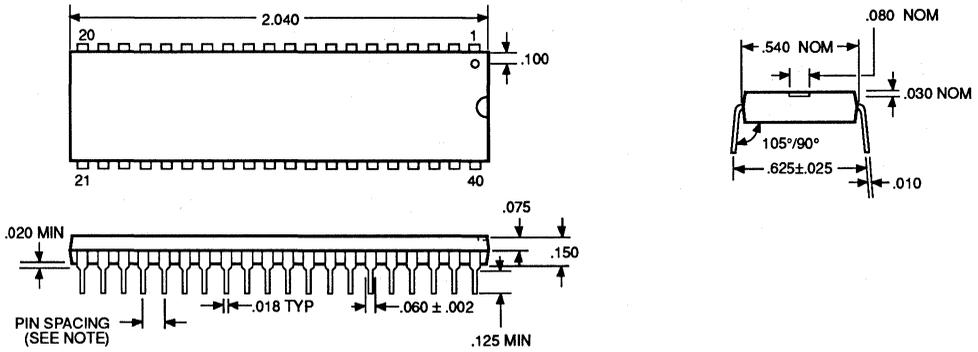
24-Pin Plastic DIP (N)



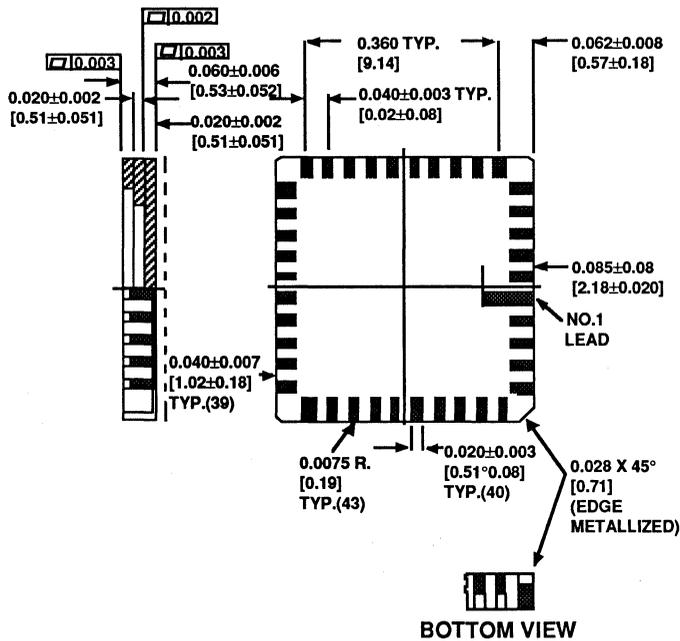
28-Pin Plastic DIP (N)



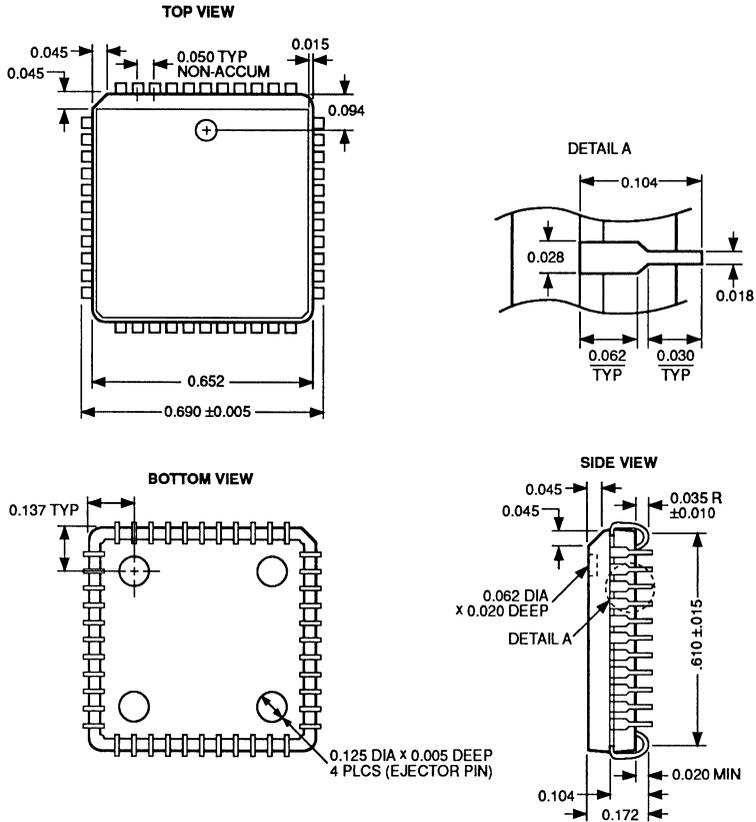
40-Pin Plastic DIP (N)



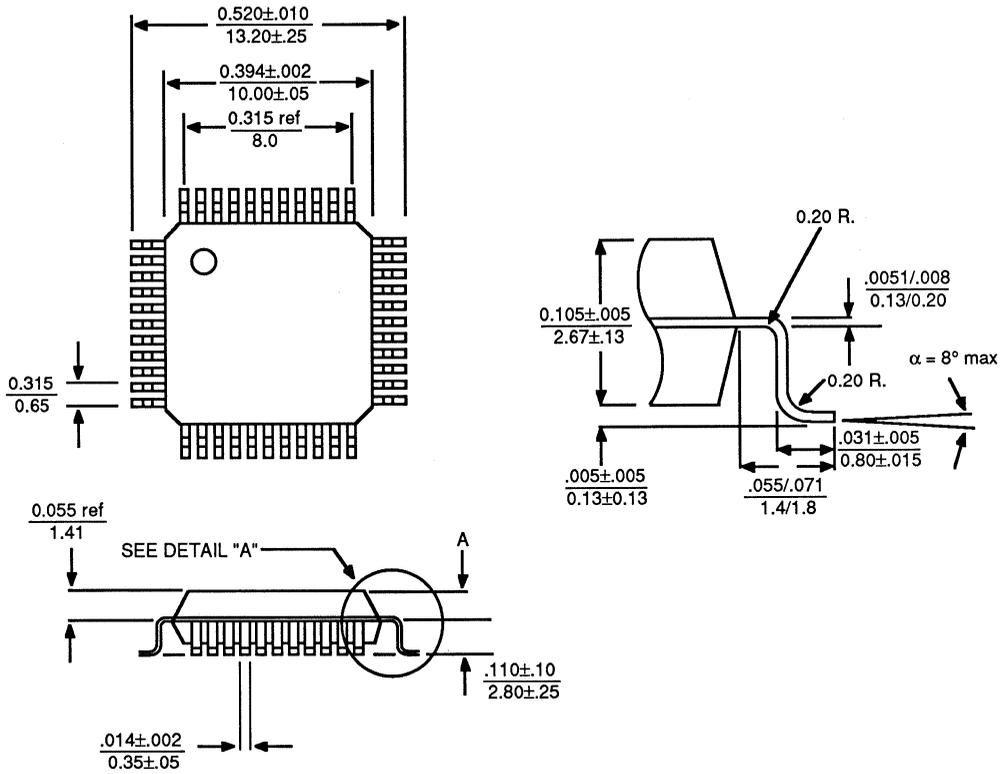
40-Pin LCC (L)



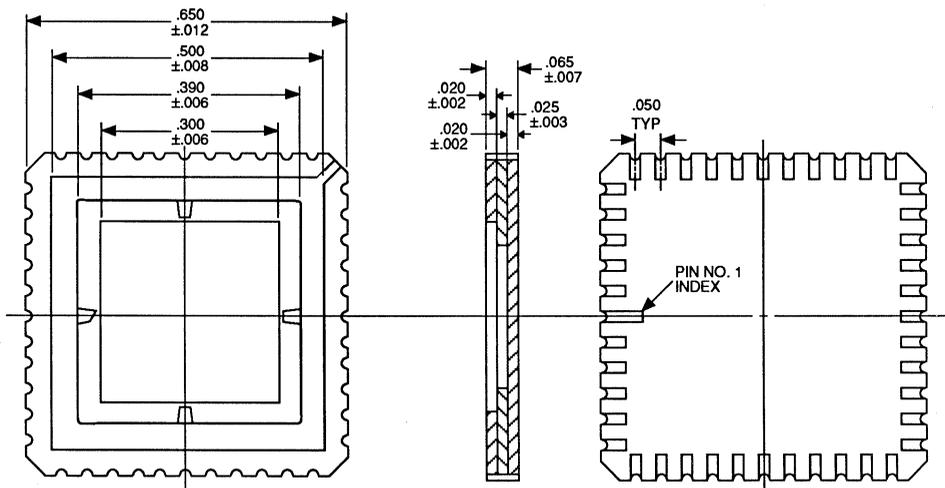
44-Pin PLCC (V)



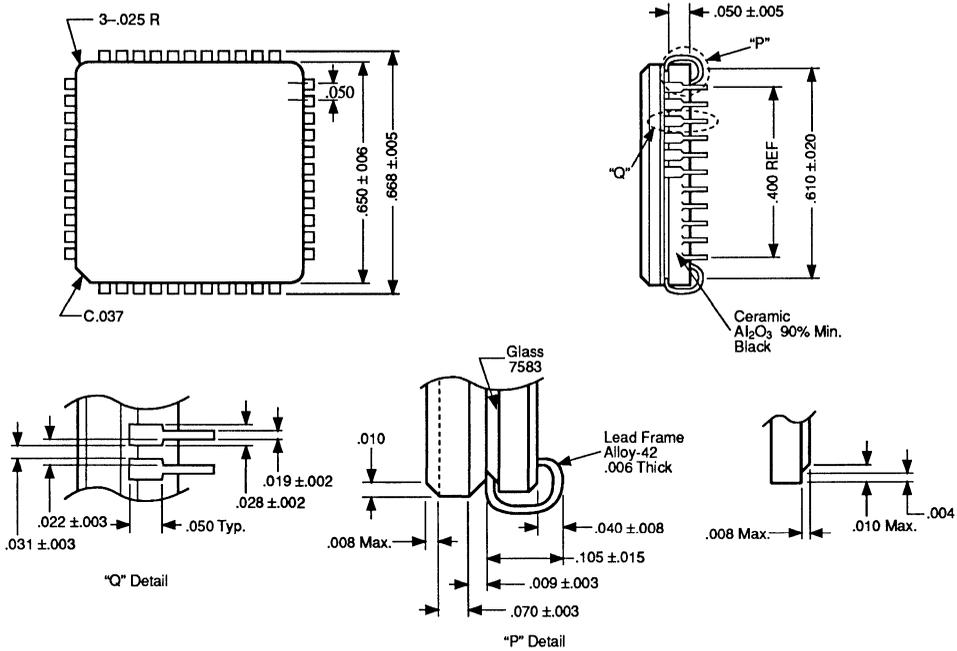
44-Pin Gull Wing QFP (Q)



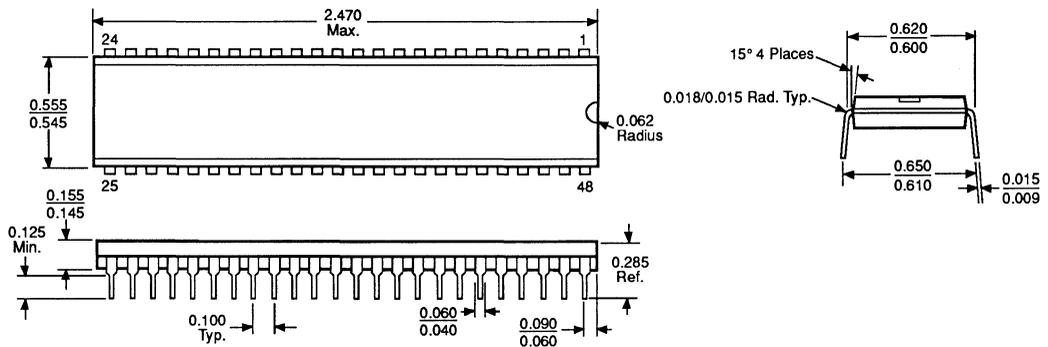
44-Pin LCC (L)



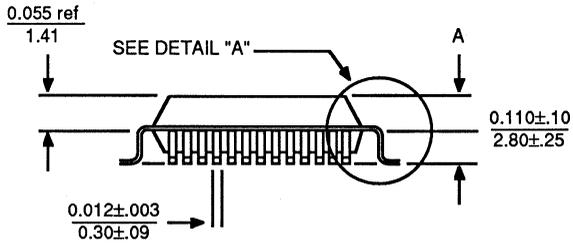
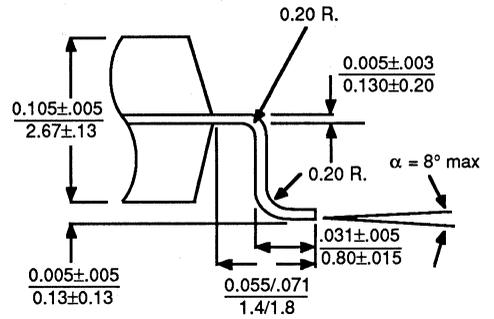
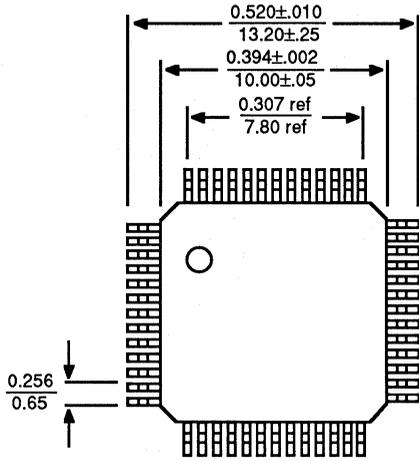
44-Pin Quad PAC (E)



48-Pin Plastic DIP (N)



52-Pin Gull Wing QFP (Q)





Worldwide Sales Offices and Design Centers

SECTION 9: WORLDWIDE SALES OFFICES AND DESIGN CENTERS

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U.S. Sales Representatives

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Huntsville, AL 35802
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2323 E. Magnolia, Suite 115
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Fax: 214-235-0271

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Fax: 408-982-9224

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Solana Beach, CA 92075
Tel: 619-481-9310
Fax: 619-481-2026

R.T.S. Associates

1111 El Camino Real, Suite 101
Tustin, CA 92680
Tel: 714-730-9561
Fax: 714-730-9585

The L.C.S. Company
781 Phelan Road, Suite 5
Pinon Hills, CA 92372
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6 Cedar Ridge Rd.
Collinsville, CT 06022
Tel: 203-693-6567
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2655 Interplex Drive, Suite 104
Trevose, PA 19047
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Fax: 215-244-4104

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GEORGIA

Electronic Marketing Associates
6695 Peachtree Industrial
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Atlanta, GA 30360
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Fax: 404-446-9363

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IDAHO

Contact Micrel Directly

ILLINOIS

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Applied Data Management
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Batesville, IN 47006
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12001 Whip Road
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Fax: 617-273-4856

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Cedar Rapids, IA 52402
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Burlington, MA 01803
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Fax: 201-288-7583

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6512 Six Forks Road, Suite 601A
Raleigh, NC 27615
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8505 Tanglewood Square
Chagrin Falls, OH 44022
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Omega Electronic Sales
2655 Interplex Drive, Suite 104
Trevose, PA 19047
Tel: 215-244-4000
Fax: 215-244-4104

PENNSYLVANIA (West)

See Ohio

RHODE ISLAND

Contact Micrel Directly

SOUTH DAKOTA

Contact Micrel Directly

SOUTH CAROLINA

Electronic Marketing Associates
210 W. Stone Avenue
Greenville, SC 29609
Tel: 803-233-4637
Fax: 830-242-3089

TENNESSEE

Electronic Marketing Associates
6695 Peachtree Industrial Blvd.
Suite 101
Atlanta, GA 30360
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Barry Sales
1300 E. Arapaho, Suite 105
Richardson, TX 75081
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VERMONT

Dynamic Sales
Rd. #1, Box 117-W
Graniteville, VT 05654
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Fax: 802-476-4223

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Boyle Associates
12001 Whip Road
Reston, VA 22091
Tel: 703-620-9558
Fax: 703-476-0414

WASHINGTON

Contact Micrel Directly

WASHINGTON D.C.

Boyle Associates
12001 Whip Road
Reston, VA 22091
Tel: 703-620-9558
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WISCONSIN

Contact Micrel Directly

WYOMING

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Tel: 214-245-1266
Fax: 800-356-3701

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4520-E West 34th Street
Houston, TX 77092
Tel: 713-956-9091
Fax: 713-956-2501

CONNEX TEK, INC.

8204 North Lamar, Suite B-11
Austin, TX 78753
Tel: 512-837-9892
Fax: 512-837-3324

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SEMICONDUCTOR CORP.

212 Chambers Roads
Suite 209
Tustin, CA 92680
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Reseda, CA 91335
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Tel: 305-735-2555
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Fax: 301-995-6332

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19 Corporate Place
107 Audubon Road, Building 1
Wakefield, MA 01880
Tel: 617-246-4442
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39 U.S. Route 46
Pine Brook, NJ 07058
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Fax: 201-882-8398

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6000 New Horizons Blvd.
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Tel: 516-226-6000
Fax: 516-226-5886

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Marlton, NJ 08053
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Fax: 609-596-0612

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100 Bluff Drive
Rochester, NY 14445
Tel: 716-248-5980
Fax: 716-248-9132

OPTO PLUS+ INC.

23382 Madero, Unit A
Mission Viejo, CA 92691
Tel: 714-380-8654
Fax: 714-380-0761



International Representatives and Distributors

INTERNATIONAL REPRESENTATIVES

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102 rue des Nouvelles
F92150 Suresnes
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Fax: 331-450-64699

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8000 Munchen 70
Tel: 49-089-723-7078
Fax: 49-089-723-1625

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I.E.S.
50 Betzalel Street
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Fax: 972-3-751-0927

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AC SIS s.r.l.
20149 Milano
Via Alberto Mario, 26
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Fax: 02-469-7607

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Kawasho Corporation
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30F, Hamamatsu-cho
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Tokyo
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Fax: 813-35-78-5921

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Mogul Electronics
Unit 11 Vestry Estate
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Kent TN14 5EU
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Fax: 44-732-740394

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CH du Grand Clos 1
P.O. Box 93
CH1752 Villars Sur Glane
Switzerland
Tel: 41-37-410060
Fax: 41-37-410070

ISC FRANCE

28, Rue De la Procession
B.P. 118-92153 Suresnes Cedex
France
Tel: 331-45-064275
Fax: 331-45-064699

LAGERKRANTZ KELTECH AB

Box 981
S 191 29 Sollentuna
Sweden
Tel: 08-754-7400
Fax: 08-754-4709

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Century House, Park Road
Southborough, Tunbridge Wells
Kent, TN4 0NX
United Kingdom
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Fax: 892-510-624

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28008 Madrid
Spain
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Fax: 34-1-542-7896

KAWASHO CORPORATION

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30F, Hamamatsu-cho
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Burwood, Victoria
Australia 3125
Tel: 03-808-8911
Fax: 03-808-9168



Design Centers

Electronic Technology Corp.

ISU Research Park
2501 North Loop Drive
Ames, IA 50010
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Fax: 515-296-7001

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2975 Bowers Ave.
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Santa Clara, CA 95051
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Fax: 408-748-0216

Micro Circuit Engineering, Ltd.

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Fax: (0684) 299435

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Fax: 813-35-78-5921

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FAX (408) 245-4175

