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Product Brief

M68340EVS EVALUATION SYSTEM

The M68340EVS evaluation system (EVS) is a board set designed to provide a low-cost method of evaluating the MC68340 integrated processor with direct memory access (IPD), and to provide development support for design of MC68340-based systems.

The M68340EVS consists of the M68340 business card computer (BCC), M68340 business card computer development interface (BCCDI), and the M68340 platform board (PFB). Additionally, the EVS includes two software debug monitor programs (340Bug and EVSbug). Using the EVS (as shown in Figure 1), the user can design, debug, and evaluate MC68340 IPD-based applications. The EVS also functions as a production tool for final test or fault analysis of user target systems.

The EVS requires a user-supplied power supply, RS-232C cable, and an RS-232C compatible terminal or host computer for functional operation. Although the EVS will function using a terminal, the preferred communication device is a host computer. Operating the EVS with a host computer allows the user to develop code with an MS-DOS™-based assembler or C compiler. Once code is developed, the program can be saved and downloaded to the EVS from the host computer.

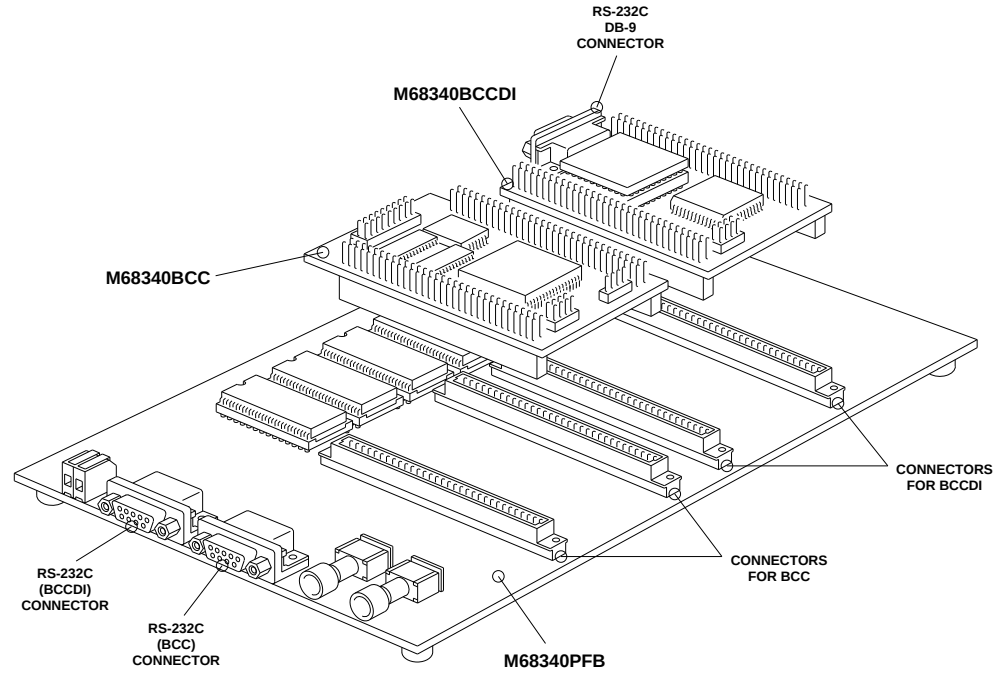

Figure 1. M68340 Evaluation System

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M68340 BUSINESS CARD COMPUTER

The BCC operates as a standalone single-board computer or as a predefined core in larger custom applications. The BCC consists of a 2.3 x 3.9 in. (5.84 x 9.9 cm) printed circuit board (PCB) using surface-mount technology. The BCC contains the resident MC68340 IPD, on-board memory, and peripheral interface circuits. The BCC hardware features are as follows:

- MC68340 Integrated Processor with DMA
- 64K x 16-Bit Erasable Programmable Read Only Memory (EPROM)
- 32K x 16-Bit Byte-Addressable Random Access Memory (RAM)
- RS-232C-Compatible Terminal/Host Computer Input/Output (I/O) Port
- Background Mode Interface Port
- EVS Interface Connectors

As shipped, the BCC EPROM contains a debug monitor called 340Bug. Communication with 340Bug requires either a terminal or a host computer running terminal emulation software. The user can interface with the 340Bug via the PFB terminal RS-232C port or the BCC RS-232C connector.

The 340Bug uses several on-chip resources to operate. One of the MC68340 serial channels is used for terminal communications, and several chip selects are used for EPROM and RAM interfacing. The EPROM containing 340Bug software and RAM must remain in the memory map at the programmed locations for the 340Bug to execute properly. Chip selects, serial port parameters, auto-boot (turnkey), and operating environments are easily customized by the user.

M68340 BUSINESS CARD COMPUTER DEVELOPMENT INTERFACE

The BCCDI consists of a 2.25 x 3.5 in. (5.7 x 8.9 cm) PCB using surface-mount technology. The BCCDI is a single-board computer which uses the same EVS interface connectors as the BCC. The BCCDI, in conjunction with an MS-DOS host computer, provides an alternate debug monitor to the 340Bug, called EVSbug.

Communication with EVSbug requires a host computer operating the EVS software. The user can interface with EVSbug via the BCCDI RS-232C port or the PFB PC RS-232C port. The BCCDI hardware features are as follows:

- MC68HC811E2 Programmable Microcontroller Unit (MCU)
- Motorola Custom Hardware Breakpoint Chip
- RS-232C-Compatible Terminal/Host Computer I/O Port
- Background Mode Interface Port
- EVS Interface Connectors

EVSbug, in conjunction with the BCCDI, implements a debug monitor for the MC68340. EVSbug differs from 340Bug in that it requires no resources from the MC68340 to operate. EVSbug functions by placing the MC68340 into background mode when executing the debug monitor commands.

EVSbug commands enable BCC EPROM user-code programming. Programming is controlled via the BCCDI from data downloaded through the serial interface from the host computer. The EPROM programming voltage is generated by the PFB power converter.

M68340 PLATFORM BOARD

The PFB consists of a 6 x 10 in. (15.24 x 25.4 cm) PCB, which provides a base for installing the BCC and BCCDI PCBs. There are four memory expansion sockets on the PFB, allowing the addition of 32K x 8 static RAMs or EPROMs. An additional socket is provided for an MC68881 or MC68882 floating point coprocessor device. Interface connectors are available for quick connection to a logic analyzer or a prototype board.

The PFB also has two DB-9 RS-232C serial communication connectors. These serial connectors are I/O ports for communicating with the BCC and BCCDI. A header is provided for background mode connections to the MC68340. The PFB hardware features are as follows:

- Four 32K x 8 RAM/EPROM Sockets (unpopulated)
- MC68881/MC68882 Floating Point Coprocessor Socket (unpopulated)
- External Power Supply Connector (5 V and ground)
- Two RS-232C-Compatible Terminal/Host Computer I/O Ports
- Logic Analyzer Interface Port
- Background Mode Interface Port
- EVS Interface Connectors (for BCC and BCCDI interconnection)

M68340EVS SOFTWARE DEBUG MONITORS

Two software debug monitors (340Bug and EVSbug) are available to the user. Using either debug monitor program, the user interacts with the EVS through predefined monitor commands entered at the terminal/host computer keyboard. These commands perform functions such as display or modify memory, display or modify MC68340 internal registers, program execution under various levels of control, control access to various I/O peripherals connected to the EVS, and control programming of the BCC EPROM.

The 340Bug monitor is primarily used with the BCC in the standalone configuration, utilizing an RS-232C compatible terminal or host computer. The 340Bug monitor is factory programmed in the BCC EPROM. System evaluation facilities are available for loading and executing user programs. System calls (via TRAP #15) are an aid in generating user programs. System calls access selected functional routines contained within 340Bug, including input and output routines. TRAP #15 also transfers control back to 340Bug at the end of a user program. Table 1 lists the available 340Bug commands.

The EVSbug monitor is factory supplied on two MS-DOS 5 1/4 inch floppy disks. The first disk contains the CPU32 (MC68340) freeware assembler. The second disk contains the EVSbug monitor program. Both the assembler and EVSbug monitor are loaded into the host computer by the user. Hardware breakpoints are supported in EVSbug by a custom hardware breakpoint chip on the BCCDI. The EVSbug provides a self-contained programming and operating environment. Table 2 lists the available EVSbug commands.

When using a host computer, either the 340Bug or EVSbug monitor can be used. Assembler and monitor updates for 340Bug and EVSbug are available via Motorola's Freeware Bulletin Board Service (512-891-3733). Additional operating systems, debuggers, assemblers, and compliers supplied by third party vendors in disk or ROM form, may be included with the M68340EVS.

Table 1. Monitor (340Bug) Commands

Command	Description
BC <range><del><addr> [;B|W|L]	Block of Memory Compare
BF <range><del><data>[<del><increment>] [;B|W|L]	Block of Memory Fill
BM <range><del><addr> [;B|W|L]	Block of Memory Move
BR {<addr>[:<count>]}	Breakpoint Insert
BS <range><del><text> [;B|W|L] or <range><del><data>[<del><mask>] [;B|W|L|N|V]	Block of Memory Search
BV <range><del><data>[<del><increment>] [;B|W|L]	Block of Memory Verify
DC <exp>|<addr>	Data Conversion
DU [<port><del>]<range><del>[<text><del>][<addr>][<offset>] [;B|W|L]	Dump S-Records
GD [<addr>]	Go Direct (Ignore Breakpoints)
GN	Go to Next Instruction
GO [<addr>]	Go Execute User Program
GT <addr>[:<count>]	Go To Temporary Breakpoint
HE [<command>]	Help
LO [<port><del>][<addr>][;<X/-C/T>][=<text>]	Load S-Records from Host
MA [<name>]	Macro Define/Display
MAE <name><del><line#><del>[<string>]	Macro Edit
MAL	Macro Expansion Listing Enable
MD[S] <addr>[;<count>|<addr>][; [B|W|L|DI]]	Memory Display
MM <addr>[; [[B|W|L][A][N]]|[DI]]	Memory Modify
MS <addr>{Hexadecimal number}/{'string'}	Memory Set
NOBR [<addr>]	Breakpoint Delete
NOMA [<name>]	Macro Delete
NOMAL	Macro Expansion Listing Disable
NOPA [<port>]	Printer Detach
OF [Rn[;A]]	Offset Registers Display/Modify
PA [<port>]	Printer Attach
PF [<port>]	Port Format
RD {[+|-|=][<dname>][/]}{[+|-|=][<reg1>[-<reg2>]][/]}	Register Display
RESET	Cold/Warm Reset
RM <reg>	Register Modify
RS <reg>[<exp>][;A]	Register Set
SD	Switch Directories
T [<count>]	Trace
TC [<count>]	Trace On Change of Control Flow
TM [<port>][<escape>]	Transparent Mode
TT <addr>	Trace To Temporary Breakpoint
VE [<port>][<addr>][;<X/-C>][=<text>]	Verify S-Records Against Memory
Diagnostic Monitor (340Diag) Commands	
HE	Help
ST	Self Test
SD	Switch Directories
LE	Loop-On-Error Mode
SE	Stop-On-Error Mode
LC	Loop-Continue Mode
NV	Non-Verbose Mode
DE	Display Error Counters
ZE	Clear (Zero) Error Counters
DP	Display Pass Count
ZP	Zero Pass Count
WL.<size> [<addr> [<del><data>]]	Write Loop
RL.<size> [<addr> [<del><data>]]	Read Loop
WR.<size> [<addr> [<del><data>]]	Write/Read Loop
CPU	Central Processor Unit Tests
MT	Memory Tests
BERR	Bus Error Test

Table 2. Monitor (EVSbug) Commands

Menu	Commands	Description
File	Load	Download (DOS file S-Records) from Host Computer to EVS RAM
	Save	Upload (Create DOS file S-Records) from EVS RAM or EPROM to Host
	Computer	
	Prog	Program BCC EPROM with DOS file (S-Records)
Register	Display	Display/Examine MC68340 Register Contents
	Modify	Modify MC68340 Register Contents
	I/O Regs	Change MC68340 Register Memory Locations via Predefined Register Names
Memory	Display	Display User Memory Contents
	Modify	Modify User Memory Contents
	Fill	Block Fill User Memory with Byte, Word, or Longword
	Search	Search Block of User Memory with Byte, Word, or Longword
	Asm/Dasm	Assemble/Disassemble (Interactive)
Debug	Go	Go (Execute Program)
	Status	Display Status of MC68340 FREEZE, RESET, and HALT Signal States
	Abort	Abort/Halt MC68340 Program Execution
	Trace	Trace Program Execution on a Instruction-by-Instruction Basis
	Reset	Reset/Re-Initialize MC68340
	Call	Call/Execute Subroutine and Return to Specified Address
Breakpt	Set one	Set One Address and Mask Value into Breakpoint Table
	Clr one	Clear/Delete Specified Address (including Mask Value) from Breakpoint Table
	Display	Display all Breakpoint Table Addresses and Mask Values
	Zap All	Remove all Breakpoint Table Addresses and Mask Values
DOS	Shell	Temporarily Suspend EVSbug Monitor and Exit to DOS
	Quit	Terminate EVSbug Monitor and Return to DOS
Help	Commands	Display Description of EVSbug Commands
	Version	Display BCCDI and EVSbug Firmware Revision Levels

EVS MODES OF OPERATION

There are four modes for configuring the EVS: 1) software debug configuration, 2) hardware debug configuration, 3) BCC standalone configuration, and 4) limited background mode configuration. These modes allow the user to configure the EVS for various needs in the development, debug, and test cycle. Figure 2 illustrates EVS configurations.

SOFTWARE DEBUG CONFIGURATION

The software debug configuration is normally the first mode of operation. In this configuration, application code can be created or downloaded and executed; the BCC EPROM can be reprogrammed using the EVSbug debug monitor. This configuration uses the PFB, the BCC, and, optionally, the BCCDI (depending on which debug monitor is used). In addition, a logic analyzer (via the logic analyzer connectors on the BCC and PFB) can be used, and the PFB sockets for expanding memory or adding hardware floating-point support can be used. EVS power and ground are supplied through the PFB.

In the software debug configuration, either the 340Bug or the EVSbug debug monitor can be used. When using 340Bug, the BCCDI is not used but may remain in the system, and the host computer or terminal must be connected to the terminal connector on the PFB. If EVSbug is chosen, the BCCDI is used and must be in place on the PFB; the host computer must be connected to the PC connector on the PFB. EVSbug gives the additional capabilities of executing hardware breakpoints and reprogramming the EPROM on the BCC.

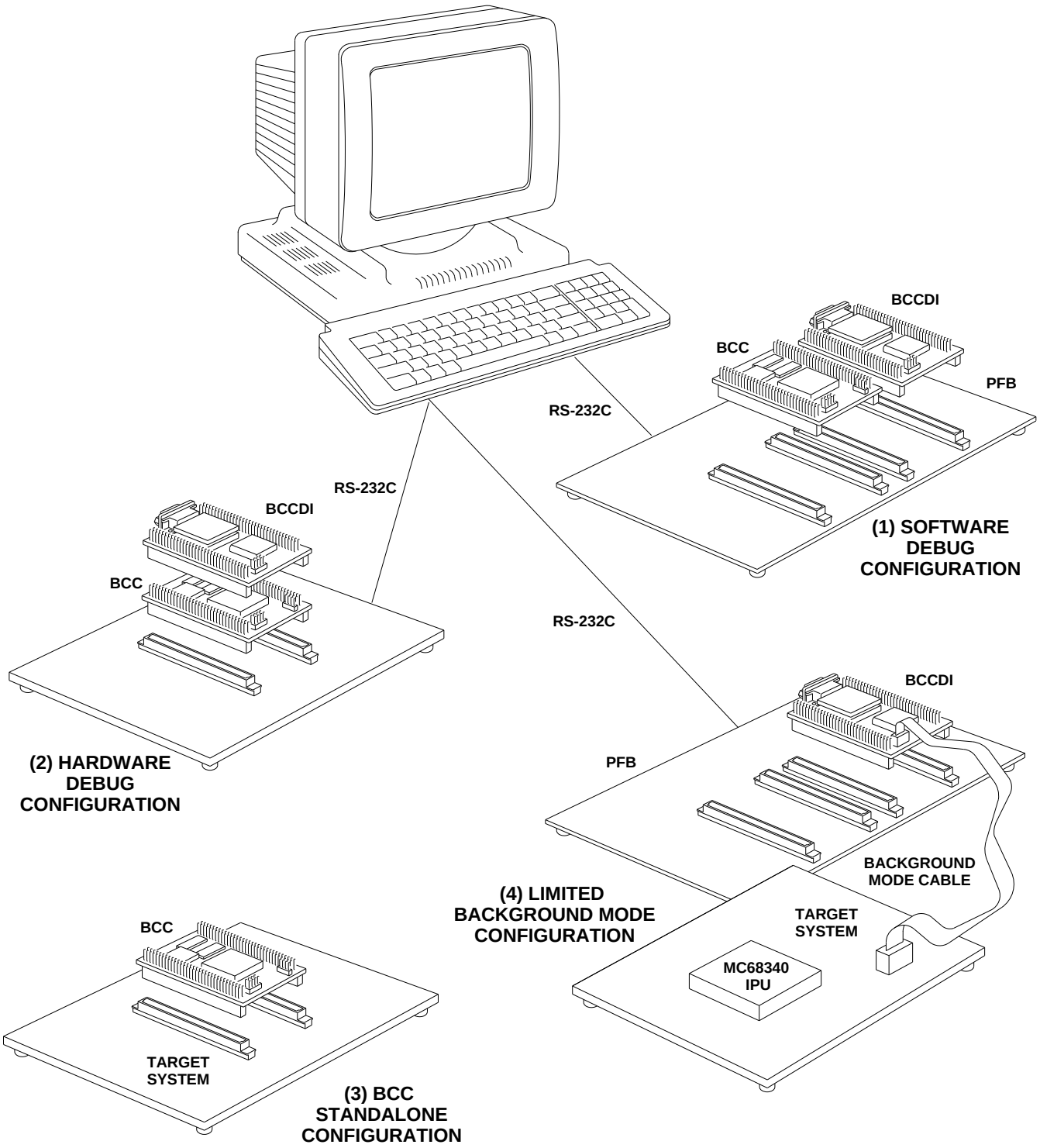

Figure 2. EVS Modes of Operation

HARDWARE DEBUG CONFIGURATION

The hardware debug configuration is used to debug prototype (target system) hardware. To use the hardware debug configuration, install the BCC in the target system and the BCCDI on the BCC. In this configuration, emulation of the MC68340 IPD with hardware breakpoints is possible by connecting a host computer to the BCCDI RS-232C connector and operating the EVSbug debug monitor program. Logic analyzer connection can be made via the BCCDI EVS interface connectors. Power and ground are supplied via the user's target system.

BCC STANDALONE CONFIGURATION

Once the hardware and software debug configurations are finished, the BCC standalone configuration can be employed. In this mode, the BCC is installed on the target system without the BCCDI. The standalone configuration provides a method for functionally testing the prototype without additional emulation hardware or software support. Serial communication with a terminal is user-application dependent. Power and ground are provided by the target system.

A typical use of the standalone configuration is one in which the user code has been debugged and programmed into the BCC EPROM, using the software debug configuration. Optionally, the BCC EPROM can be disabled on the BCC, with the boot code contained in target system memory.

LIMITED BACKGROUND MODE CONFIGURATION

Limited background mode configuration is provided for final test or fault analysis of the target system. This mode requires that a background mode interconnection capability is available on the target system. A background mode cable (not supplied) is required for connecting the target system and the BCCDI background mode interface ports. Connection to a host computer is made via the BCCDI RS-232C port. Power and ground are supplied through the PFB.

The background mode configuration provides the user with limited emulation capabilities because hardware breakpoints are not available (the Motorola custom hardware breakpoint chip must have access to the MC68340 IPD address lines to provide breakpoints). However, background instructions may be used in target code to halt execution. While connected to the BCCDI via the background mode cable, the user can examine memory locations and download and exercise specific test programs. An entire final test program can be performed on the target system using the background mode.

MORE INFORMATION

The MC68340 IPD combines the following functional units on a single IC:

- CPU32 — 32-bit, MC68020-Derived Core Processor
- Direct Memory Access (DMA) Controller
- Serial I/O — Two-Channel USART with Baud Rate Generators, MC2681/MC68681 Compatible
- Timers — Two independent 16-bit timers with 8-bit prescalers
- System Integration Module (SIM) Incorporating the Following Functions:
  - System Configuration
  - Clock Generation
  - System Protection
  - Interrupt Response
  - Chip Select and Wait State
  - Parallel I/O
  - Periodic Interrupt Timer
  - IEEE 1149.1 (JTAG)
- Up to 20 Discrete I/O Lines
- Static Low-Power Design (HCMOS) with Standby Mode
- 16.78-MHz, Maximum Frequency at 5-V Supply
- 144-Lead Quad Flat Pack or 145 Pin Grid Array

Documentation on the MC68340 Integrated Processor with DMA is available:

BR572/D	*MC68340 Product Brief*
MC68340/D	*MC68340 Technical Summary*
MC68340UM/AD	*MC68340 User's Manual*
M68000PM/AD	*M68000 Programmer's Reference Manual*

More detailed documentation on the M68340EVS evaluation system comes with the product:

M68340EVS/AD1	*M68340EVS Evaluation System User's Manual*
M68340BCC/AD1	*M68340BCC Business Card Computer User's Manual*
M68340BUG/AD1	*M68340BUG Debug Monitor User's Manual*

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