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*Communications and Advanced*
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# MCF5204

*Product Brief*

## MCF5204 ColdFire™ Integrated Microprocessor

The MCF5204 integrated microprocessor combines a ColdFire™ processor core with several peripheral functions such as timers and serial interface. Designed for cost-sensitive embedded control applications, the ColdFire core delivers enhanced performance while maintaining low system cost. To speed program execution, the on-chip instruction cache and SRAM provide one-cycle access to critical code and data. The MCF5204 processor greatly reduces the time required for system design and implementation by packaging common system functions on chip and providing glueless interfaces to 8- and 16-bit SRAM, ROM, and I/O devices.

The revolutionary ColdFire microprocessor architecture gives cost-sensitive, high-volume markets new levels of price and performance. Based on the concept of variable-length RISC technology, ColdFire combines the architectural simplicity of conventional 32-bit RISC with a memory-saving, variable-length instruction set. In defining the ColdFire architecture for embedded processing applications, Motorola incorporated RISC architecture for peak performance and a simplified version of the variable-length instruction set found in the M68000 Family for code density.

By using a variable-length instruction set architecture, embedded processor designers using ColdFire RISC processors will enjoy significant system-level advantages over conventional fixed-length RISC architectures. The denser binary code for ColdFire processors consumes less valuable memory than any fixed-length instruction set RISC processor available. This improved code density means more efficient system memory use for a given application, and requires slower, less costly memory to help achieve a target performance level.

The integrated peripheral functions provide high performance and flexibility. The serial interface consists of a programmable full duplex UART. The MCF5204 has two 16-bit general-purpose multimode timers, one of which provides a separate input and output signal. For system protection, the processor includes a programmable 16-bit software watchdog timer and several bus monitors. In addition, common system functions such as chip-selects, interrupt control, and IEEE 1149.1 Test (JTAG) support are included.

A sophisticated debug interface supports both background-debug mode and real-time trace. This interface is common to all ColdFire-based processors and allows common emulator support across the entire ColdFire Family.

ColdFire is a trademark of Motorola.

1. $I^2C$ bus is a proprietary Philips interface bus.

The primary features of the MCF5204 integrated processor include the following:

- ColdFire Processor Core
  - — Variable-length RISC
  - — 32-bit internal address bus with up to 4 Mbytes of off-chip linear address space
  - — 16-bit data bus
  - — 16 user-visible 32-bit wide registers
  - — Supervisor / User modes for system protection
  - — Vector base register to relocate exception-vector table
  - — Optimized for high-level language constructs
  - — 13.5 MIPS at 33Mhz
- 512-Byte Direct-Mapped Instruction Cache
- 512-Byte On-Chip SRAM
  - — Provides one-cycle access to critical code and data
- Universal Synchronous/Asynchronous Receiver/Transmitter (UART)
  - — Full duplex operation
  - — UART timer provides baud rate generation based on system clock
  - — External clock provided via timer TIN pin
  - — Modem control signals available (CTS, RTS)
  - — Processor-interrupt capability
- Dual 16-Bit General-Purpose Multimode Timers
  - — 8-bit prescaler
  - — Timer input and output pins (For Timer 1 only)
  - — 30ns resolution with 33MHz system clock
  - — Processor-interrupt capability
- System Interface
  - — Glueless bus interface to 8-, 16- SRAM, ROM, and I/O devices
  - — 6 programmable chip-select signals
  - — Programmable wait states and port sizes
  - —System protection
    - 16-bit software watchdog timer with prescaler
    - Double bus fault monitor
    - Bus timeout monitor
    - Spurious interrupt monitor
  - — Programmable interrupt controller
    - Low interrupt latency
    - 4 external interrupt inputs
    - Programmable interrupt priority and autovector generator
  - — IEEE 1149.1 test (JTAG) support
  - — 8-Bit General-Purpose I/O Interface
- System Debug Support
  - — Real-time trace
  - — Background debug interface
- Fully Static 5.0-Volt Operation
- 100 Pin TQFP Package

# OVERVIEW

Figure 1 is a block diagram of the MCF5204 processor. The paragraphs that follow provide an overview of the device.

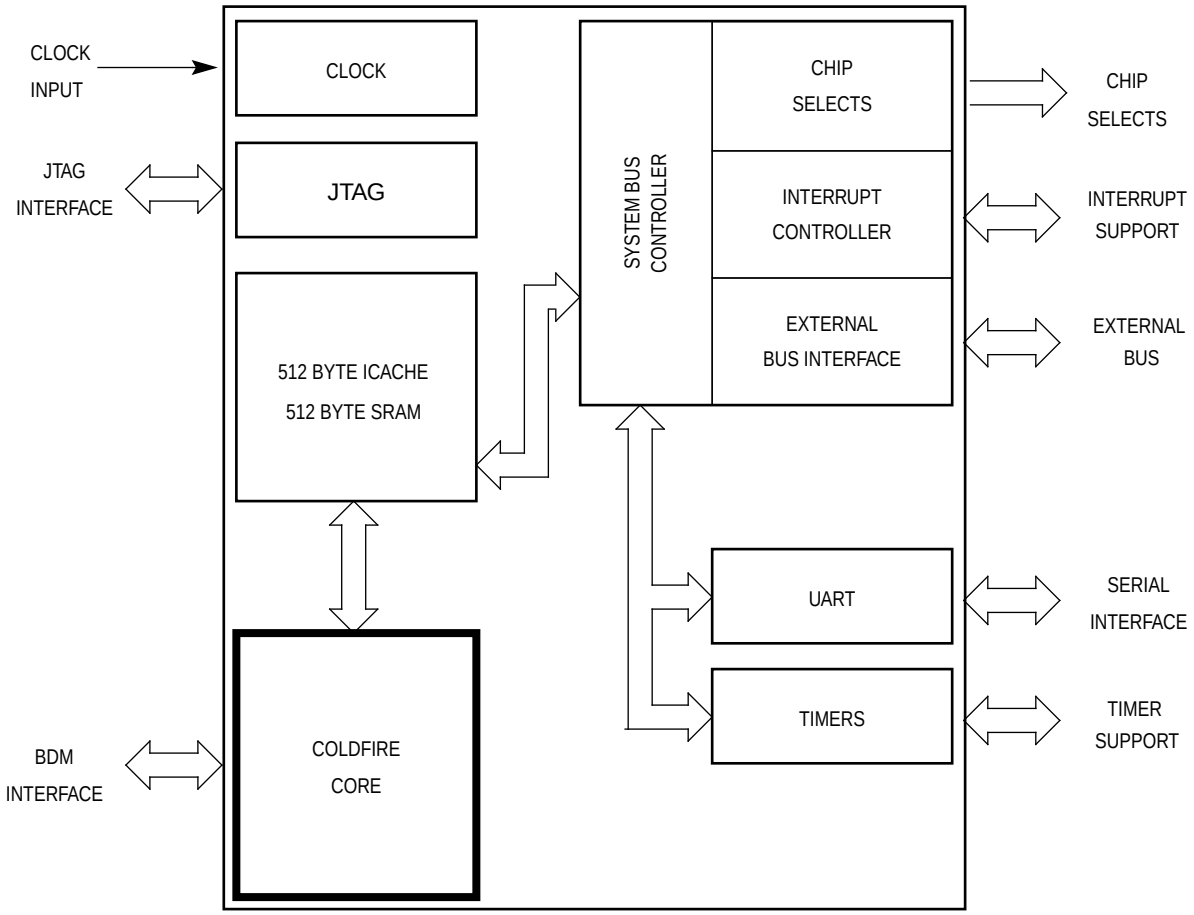


**Figure 1. MCF5204 Block Diagram**

## ColdFire Processor Core

The ColdFire processor core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, thereby minimizing time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC datapath with a dual-read-ported register file feeding an arithmetic/logic unit.

## Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The MCF5204 processor uses a 512-byte, direct-mapped instruction cache to achieve 13.5 MIPS at 33 MHz.The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16- and 8-bit port sizes to quickly fill cache lines.

## Internal SRAM

The 512-byte on-chip SRAM provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance.

## UART Module

The timer internal to the full duplex UART module provides baud-rate generation based on the system clock. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and as many as two stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{RTS}$) and clear-to-send ($\overline{CTS}$) lines.

## Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer. One of the timers provides package pins for use in any of three modes. One mode captures the timer value with an external event. Another mode triggers an external signal or interrupts the CPU when the timer reaches a set value, while a third mode counts external events. Each timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. The programmable timer-output pin generates either an active-low pulse or toggles the output.

## System Interface

The MCF5204 processor provides a glueless interface to 8-bit and 16-bit port size SRAM, ROM, FLASH and peripheral devices with independent programmable control of the assertion and negation of chip-selects and write-enables.

### External Bus Interface

The bus interface controller transfers information between the ColdFire core and external memory, and peripherals. The external bus interface provides as many as 22 bits of address bus space, a 16-bit data bus, and all associated control signals. This interface implements an extended asynchronous protocol that supports bursting operations.

### 8-Bit General-Purpose I/O Interface

An 8-bit general-purpose programmable I/O port serves as either an input or an output on a bit-by-bit basis. This port is multiplexed with the timer, UART, and upper address pins.

### Chip-Selects

Six programmable chip-select outputs provide signals that enable external memory and peripheral circuits. These signals also interface to 8- or 16- bit ports. The base address, access permissions, wait-state insertion, write protection, automatic termination, and timing wave forms are all programmable with configuration registers.

**Interrupt Controller.** The interrupt controller provides user-programmable control of four external interrupt and four internal peripheral interrupts. Users can program each internal or external interrupt to any one of seven interrupt levels and four priority levels within each of these levels.

**System Protection.** The MCF5204 processor contains a 16-bit software watchdog timer with an 8-bit prescaler. The programmable software watchdog timer provides either a level 7 interrupt or a hardware reset on timeout. The MCF5204 processor also contains a reset status register that indicates the cause of the last reset.

**IEEE 1149.1 JTAG.**To help with system diagnostics and manufacturing testing, the MCF5204 processor includes dedicated user-accessible test logic that complies with the IEEE 1149.1 standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1 standard.

## System Debug Interface

The ColdFire processor core debug interface supports real-time trace and background-debug mode. A four-pin background debug mode (BDM) interface provides system debug. The BDM is a proper subset of the BDM interface provided on Motorola's 683XX Family of parts.

In real-time trace, four status lines provide information on processor activity in real time (PST pins). A 4-bit wide debug data bus (DDATA) displays operand data, which helps track the machine's dynamic execution path as the change-of-flow instructions execute.

## Pinout and Package

The MCF5204 device is supplied in 16, 25, and 33MHz speeds in a 100-pin plastic thin quad flat pack package with the pinout shown in Figure 2.

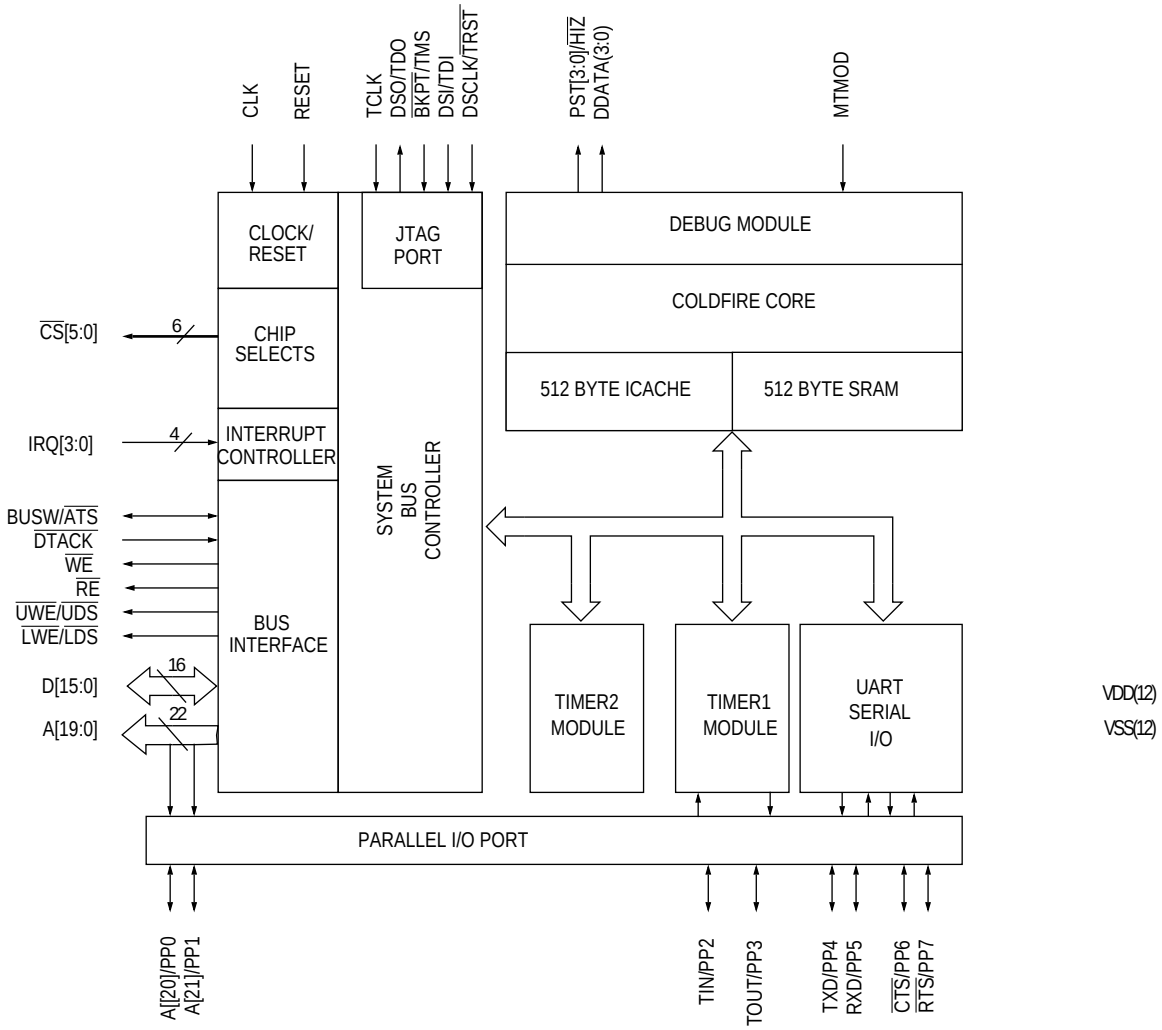


**Figure 2. MCF5204 Signal Block Diagram**

## Documentation

Additional and detailed information is available from Motorola literature distribution centers.

| DOCUMENT NUMBER | DOCUMENT TITLE | AVAILABILITY |
|---|---|---|
| MCF5204UM/AD | MCF5204 User's Manual | 3Q96 |
| MCF5200PRM/AD | MCF5200 ColdFire Family Programmer's Reference Manual | now |

## DEVELOPMENT TOOLS AND EVALUATION SYSTEMS

For information on third-party development tools support, refer to the High Performance Embedded Systems Source (BR729/D).

ColdFire evaluation systems are available. Contact your local Motorola sales office for technical details and additional information on these boards.

Visit the Motorola web site at http://www.mot.com/coldfire for additional information on any ColdFire family product.



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