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PRODUCT INFORMATION

Custom 68300

Product Brief

Custom 68300 Integrated Processors

Motorola's Custom 68300 integrated processors allow the designers of high-volume digital systems to place their application-specific circuitry on chip with an M68000 family microprocessor. More than 100,000 gates of custom logic can be added to an M68000 family core processor to produce the best solution for a designer's system. By using a Custom 68300 processor, a designer can reduce the total system cost, component count, and power consumption while providing higher performance and greater reliability. Some members of the core processor family provide special power-management features such as 3.3 V and static operation. The M68000 family of core processors offers the designer a range of performance from 1 to 10 MIPS (soon to be extended to 50 MIPS) while maintaining complete code compatibility throughout the family. The M68000 processors have a proven architecture with a broad base of application and system software support, including real-time kernels, operating systems, and compilers, in addition to a wide range of tools to support software development. Figure 1 shows a typical die layout for a Custom 68300 integrated processor.

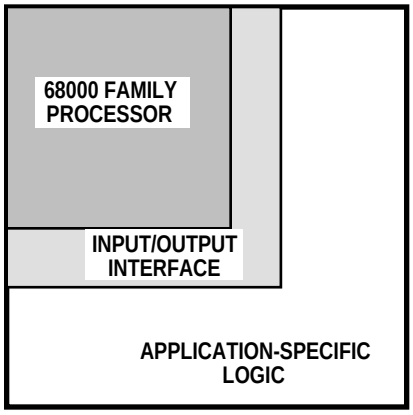

Figure 1. Typical Die Layout

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A designer can create a complete product line using the Custom 68300 program by implementing one base design using a variety of core processors. For designers already familiar with M68000 family design, migration to Custom 68300 processors is facilitated by using the same bus interfaces found on the standard M68000 family members. Additionally, many M68000 peripherals are available for integration. Custom 68300 design is simplified by a complete design system that includes both a broad cell-based library and effective CAD tools. By building on its proven M68000 microprocessor architecture and superior manufacturing capabilities, Motorola's Custom 68300 program offers designers the best path to higher system integration.

CUSTOM 68300

Designers who may be interested in pursuing Custom 68300 parts include:

- Designers looking for more system integration whose needs are not met by standard 68300 parts
- Users of 8- and 16-bit integrated solutions who need higher system performance
- Designers of high-volume applications who need to reduce cost, space, and/or power consumption

To develop parts that best suit system requirements in the shortest time frame, integrated circuit design is performed using a methodology created, tested, and documented by Motorola. In this way, Custom 68300 integrated processors can be created quickly and efficiently, with the resulting 68300 part containing all of the features needed for the system.

To implement the application-specific logic, the designer uses Motorola's standard cell library. This library offers an extensive range of digital design elements as well as an expanding range of peripheral modules. Each cell in the library has been designed for optimum size and performance. The added flexibility of high-speed, high-density cells allows the designer to achieve the most cost-effective solution while satisfying critical timing requirements. The standard cell library has been thoroughly characterized and maintained to ensure the conversion from a simulated design to working silicon is smooth. Motorola will continue to develop standard 68300 family parts as market needs are determined and evaluated. Additionally, if desired by both Motorola and the designer, custom parts may also become standard parts. Standard parts are sold on the open market, allowing costs to be spread over additional units, resulting in lower piece prices for high-volume users.

ADVANTAGES

Many designers face tough challenges in reducing product cost. By incorporating user-designed, Motorola-supplied functions into a single Custom 68300 chip, a system designer can realize significant savings in cost, power consumption, board space, and pin count. The equivalent functionality can easily require 20 separate components. Each component might have 16–64 pins, totaling over 350 connections. Each connection is a candidate for a bad solder joint or misrouted trace. Each component is another part to qualify, purchase, inventory, and maintain. Each component requires a share of the

printed circuit board. Each component draws power—often to drive large buffers to get signals to another chip. The cumulative power consumption of all the components must be available from the power supply. The signals between the core processor unit and a peripheral might not be compatible nor run from the same clock, requiring time delays or other special design considerations.

In an M68300 family component, the major functions and glue logic are all properly connected internally, timed with the same clock and fully tested. Only essential signals are brought out to pins. Parts are packaged in surface-mount packages for the smallest possible footprint.

CORE PROCESSOR UNIT

The core processor unit is the heart of an integrated processor. This unit supervises system functions, makes decisions, manipulates data, and directs I/O. Currently, designers have a choice of four different core processors; more powerful core processors will be added in the future. The EC000, CPU32, 020, and 030 cores, like all M68000 family processors, are based on the powerful and flexible M68000 architecture. Complete upward code compatibility is supported by all M68000 family processors. The programmer can use any of the eight 32-bit data registers for fast manipulation of data and any of the eight 32-bit address registers for indexing data in memory. Flexible instructions for data movement, arithmetic functions, logical operations, shifts and rotates, bit set and clear, conditional and unconditional program branches, and overall system control are supported.

The core processors can operate on data types of single bits, binary-coded decimal (BCD) digits, and 8, 16, and 32 bits. The CPU32 core additionally supports quad words; the 020 and 030 cores also support bit fields. Peripherals and data in memory can reside anywhere in the 4-Gbyte linear address space. A supervisor operating mode protects system-level resources from the more restricted user mode, allowing a true virtual environment to be developed. Many addressing modes complement these instructions, including predecrement and postincrement, which allow simple stack and queue maintenance and scaled indexed for efficient table accesses. Data types and addressing modes are supported orthogonally by all data operations and with all appropriate addressing modes. Position-independent code is easily written. For more information about programming with the M68000 family, refer to the *M68000 Programmer's Reference Manual* (M68000PM/AD).

All M68000 family processors recognize interrupts of seven different priority levels and allow a peripheral to vector the processor to the desired service routine. Internal trap exceptions ensure proper instruction execution with good addresses and data, allow operating system intervention in special situations, and permit instruction tracing. Hardware signals can either terminate or rerun bad memory accesses before instructions process data incorrectly.

EC000 CORE

The EC000 core is a core implementation of the MC68000 32-bit microprocessor architecture designed for use in the Custom 68300 program. The EC000 core has a

statically selectable 8-bit or 16-bit data bus. The address bus is 32-bits wide for use as either a 24-bit address bus, as on the 16-bit M68000 family microprocessors, or as a 32-bit address bus to fully support the internal architecture. The EC000 core will soon be available in a static version and includes some functions not found on the standard MC68000 and MC68EC000 microprocessors. These features include signals that permit easier interfacing between the core processor and the surrounding logic as well as emulation support. For more information about the EC000 core, refer to the *Custom 68300 Core Data Manual* (M68300CP/D) and the *M68000 8-/16-/32- Bit Microprocessor User's Manual* (M68000UM/AD).

CPU32 CORE

The CPU32 core is a static core specially designed for use as a 32-bit core processor. Designers used the MC68020 as a model and included advances of the later M68000 family processors, including a fast 32 $\times$ 32 multiply and 32-bit conditional branches. New instructions, such as table lookup and interpolate and low-power stop, support specific requirements of embedded control applications. The SIM40 provides the bus interface for the CPU32. It also contains much of the glue logic that typically supports the microprocessor and its interface with the peripheral and memory system. A system integration modulo (SIM40) provides programmable circuits to perform address decoding and chip selects, wait-state insertion, interrupt handling, clock generation, bus arbitration, watchdog timing, discrete I/O, and power-on reset timing. For more information about the CPU32 core, refer to the *Custom 68300 Core Data Manual* (M68300CP/D) and the *MC68330 Integrated CPU32 Microprocessor User's Manual* (MC68330UM/AD).

020 CORE

The 020 core is a static core based on the MC68020 32-bit microprocessor, a full 32-bit implementation of the M68000 architecture. The 020 core provides additional addressing modes to provide enhanced support for high-level languages. A 256-byte on-chip instruction cache speeds program execution. The 020 core also has a flexible coprocessor interface that efficiently supports communication with external coprocessors such as a floating-point unit. For more information about the 020 core, refer to the *Custom 68300 Core Data Manual* (M68300CP/D) and the *M68020 32-Bit Microprocessor User's Manual* (M68020UM/AD).

030 CORE

The 030 core, based on the MC68EC030 embedded control microprocessor, provides additional features beyond those of the 020 core. A synchronous bus allows two-clock interaction with system peripherals able to support the 32-bit bus. The 256-byte data cache also improves performance by reducing memory accesses. A cache burst-fill mechanism allows efficient use of the bus for quickly getting information into the caches. Additionally, if memory management is desired, the designer can also use the 030 core. For more information about the 030 core, refer to the *Custom 68300 Core Data Manual* (M68300CP/D) and the *MC68030 Enhanced 32-Bit Microprocessor User's Manual* (MC68030UM/AD) or (MC68EC030UM/AD) .

Table 1. Summary of Core Processor Features

Feature	EC000 Core	CPU32 Core	020 Core	030 core
Address Bus	32 bit	32 bit	32 bit	32 bit
Data Bus	8 or 16 bit	16 bit	32 bit	32 bit
Dynamic Bus Sizing	No	Yes	Yes	Yes
Asynchronous Bus Interface	4 clocks	3 clocks	3 clocks	3 clocks
Synchronous Bus Interface	—	2 clocks 16 bits	—	2 clocks 32 bits
Addressing Modes	14	14	18	18
Data Types	5	6	7	7
Number of Instructions	81	94	112	115
System Integration	No	Yes	No	No
Static Operation	1Q93	Yes	Yes	Yes
3.3 V Operation	Yes	Yes	Yes	Yes
Instruction Cache	No	No	256 byte	256 byte
Data Cache	No	No	No	256 byte
Cache Burst Fill	No	No	No	Yes
Memory Management	No	No	No	Optional
Coprocessor Interface	No	No	Yes	Yes
Performance	2.5 MIPS at 16.67 MHz	6.0 MIPS at 25 MHz	6.5 MIPS at 25 MHz	8.8 MIPS at 33 MHz
Availability	Now	1Q93	2Q93	1Q94

STANDARD CELL LOGIC

Application-specific logic is easily implemented using Motorola's MDA08 family of CMOS standard cells which features a diverse set of digital cells as well as a growing library of peripheral devices. The standard cell library is based on Motorola's unified design rules that allow new functions to be continually added. Each cell in the MDA08 standard cell library has been designed for optimum size and performance. The added flexibility of high-speed, high-density cells allows the designer to achieve the most cost-effective solution while satisfying critical timing requirements. Additionally, each cell has been completely characterized, allowing swift and reliable transition from simulation to silicon. For more information about the MDA08 standard cell library, refer to *MDA08 CMOS Standard Cell Data* (DL154/D).

The MDA08 library has the following features:

- Extensive Digital Element Library
- 0.8-micron Triple-Level-Metal CMOS Process
- 370-ps Typical Delay with a Fanout of 2 (260 ps for Hi-Drive Gate)
- Configurable RAM, ROM, and PLA
- CMOS, TTL, or Schmitt-Trigger I/O Cells
- 4, 8, 16, 24, or 48 mA Drive I/O Cells

DESIGN METHODOLOGY

The Custom 68300 program supports the use of several types of functional blocks that can be integrated on one chip, including hard macros, soft macros, and synthesizable blocks. Further information about the design methodology is available in the *Custom 68300 Integrated Microprocessors Design Manual* (M68300DM/AD).

HARD MACRO BLOCKS

Hard macro blocks are hand-laid-out designs generated by Motorola and packaged for use by designers as elements of larger designs. The blocks are not relaid for each new design. These blocks, which perform major functions such as central processing or communications, are generally derived from standard functions and/or parts available from Motorola. The user is not allowed access to the internal signals or allowed to make changes to the internal workings of the blocks. These blocks are very efficient in terms of silicon area, but allow little flexibility for the user. They are also reusable, allowing easy migration to new parts.

Supported blocks include:

- EC000 Core
- 330 Core
- 020 Core
- 030 Core
- CM146818B Real-Time Clock—provides 112 bytes of CMOS SRAM and allows a backup power supply

SOFT MACRO BLOCKS

The soft macros are functions that are described and physically implemented in terms of standard cells. These blocks are laid out to best fit the layout of each application-specific design. As technology improves, these blocks are easily upgraded with only minor alterations to the design. However, minor timing changes may occur as these blocks are relaid out. These blocks, which are generally Motorola proprietary, include the following functions:

- 68681 DUART
- 68901 Multifunction Peripheral
- 53C90 SCSI Controller
- DMA Controller
- DRAM Controller
- Interrupt Controller

SYNTHESIZABLE BLOCKS

The synthesizable blocks are created using a special high-level language. The designer simply defines logical functions through the use of this special language, and, once compiled, the function is automatically implemented at the gate level. The synthesizable logic is easily and quickly implemented and modified.

These compiled functions include:

- Fixed-Function Compilers Allow Designers To Select the Size of the Following Functions:
  - —Single-Port RAM
  - —Multi-Port RAM
  - —ROM
  - —Programmable Logic Array
  - —High Drive Clock Buffer
  - —Adders and Multipliers
- Synopsys® Synthesizable Macro Cells (customizable JTAG controllers, memory detection and correction circuits, DRAM control, interrupt encoding and decoding, and SCSI interface circuits)

DESIGN TOOLS

Currently, Motorola supports the following tool set for Custom 68300 design:

- Cadence Framework™—Schematic Capture
- Synopsys®—Synthesis Tool
- Cadence Verilog®—Simulator
- Cadence Veritime™—Static Timing Analysis

In the future, Motorola will support other tool sets.

TEST METHODOLOGY

Testing is a major component of the production of custom chips. The cost of generating quality tests for complex components can be very high. To produce Six-Sigma quality in Custom 68300 devices requires a partnership in quality between Motorola and its customers. Motorola ensures the quality of design and test for the core processors and the hard and soft macros. The designer is responsible for ensuring total part quality by providing quality design and test for the application-specific circuits.

To ensure adequate quality test coverage, Motorola provides information about automatic test generation and guidelines for testability in the *Custom 68300 Integrated Microprocessors Design Manual* (M68300DM/AD).

PACKAGE INFORMATION

Designers can choose the package that best suits their needs from several offered by Motorola. Factors to consider when choosing a package include number of leads, size of package body, spacing of leads, and thermal characteristics. The packages currently offered include 80, 100, 128, 144, 160, 208, and 240 pin quad flat packs. Higher pin count packages will be available in the future.

DOCUMENTATION

The documents listed in the following table contain information on the Custom 68300 program. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page or from your local Motorola sales office if marked in the LDC column.

Document Number	Document Name	LDC
M68300DM/AD	*Custom 68300 Integrated MIcroprocessors Design Manual*	3Q93
M68300CP/D	*Custom 68300 Core Processor Data Manual*	2Q93
M68000UM/AD	*MC68000 Microprocessor User's Manual*	Yes
MC68330UM/AD	*MC68330 Integrated CPU32 Processor User's Manual*	Yes
M68020UM/AD	*M68020 32-Bit Microprocessor User's Manual*	Yes
MC68030UM/AD	*MC68030 Enhanced 32-Bit User's Manual*	Yes
M68000PM/AD	*M68000 Family Programmer's Reference Manual*	Yes
DL154/D	*MDA08 CMOS Standard Cell Data Manual*	Yes
MC68681/D	*MC68681 Advance Information*	Yes
MC68901/D	*MC68901 Advance Information*	Yes
BR729/D	*The 68K Source*	Yes
BR1407/D	*3.3 Volt Logic and Interface Circuits*	Yes
BR1114/D	*68300 Integrated Processor Family Brochure*	Yes

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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