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Communications and Advanced Consumer Technologies Group

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MCF5203

Product Brief

MCF5203 ColdFire™ Integrated Microprocessor

ColdFire™ represents a revolutionary microprocessor architecture that has been optimized for embedded processing applications. ColdFire brings new levels of price and performance to cost-sensitive high-volume markets. Based on the concept of variable-length RISC technology, ColdFire combines the architectural simplicity of conventional 32-bit RISC with a memory-saving, variable-length instruction set.

Using a variable-length instruction set architecture, ColdFire RISC processors offer embedded processor designers significant system-level advantages over conventional fixed-length RISC architectures. The more dense binary code for ColdFire processors occupies less valuable memory than for any fixed-length instruction set RISC processor available. This improved code density results in systems that (1) require less memory for a given application and (2) use slower and less costly memory to achieve a given performance level.

One of the first ColdFire family members, the MCF5203 has been optimized for cost-effective performance in deeply embedded applications. Although similar in architecture to its counterpart, the MCF5202, the MCF5203 is the only ColdFire processor optimized for bursting on a 16-bit bus.

The primary features of the MCF5203 processor include the following:

- Variable-Length RISC Code Density
  - — Requires less memory than fixed-length RISC equivalents
  - — Uses slower memory for a given performance level than fixed-length RISCs
  - — Improves effectiveness of cache memory
- Simple Instruction Set Architecture
  - — Optimized for high-level language constructs
  - — Designed to minimize die size
  - — 16 user-visible 32-bit-wide registers
  - — Supervisor / User modes for system protection
  - — Vector base register to relocate exception-vector table
- Dynamic Bus Sizing
  - — 16-, and 8-bit bus support
  - — Bursting Capability on read and write cycles
- 2-Kbyte On-Chip Unified Cache
  - — High performance nonblocking cache implementation
  - — Four-way set associative
- Debug Module Including Background Debug (BDM) and Real-Time Debug Support
- Low Interrupt Latency Accelerates Reponsiveness In Real-Time Applications

- Full Static Design Allows Operation Down to DC for Minimizing Power Consumption
- Three-State Pin
- JTAG IEEE 1149.1
- Single Bus Clock Input
- Low-Cost 100-Pin TQFP Packaging
- Fully Supported by Industry-Leading Third-Party Tools Developers

OVERVIEW

Figure 1 is a block diagram of the MCF5203 processor. The following paragraphs provide an overview of the MCF5203 processor.

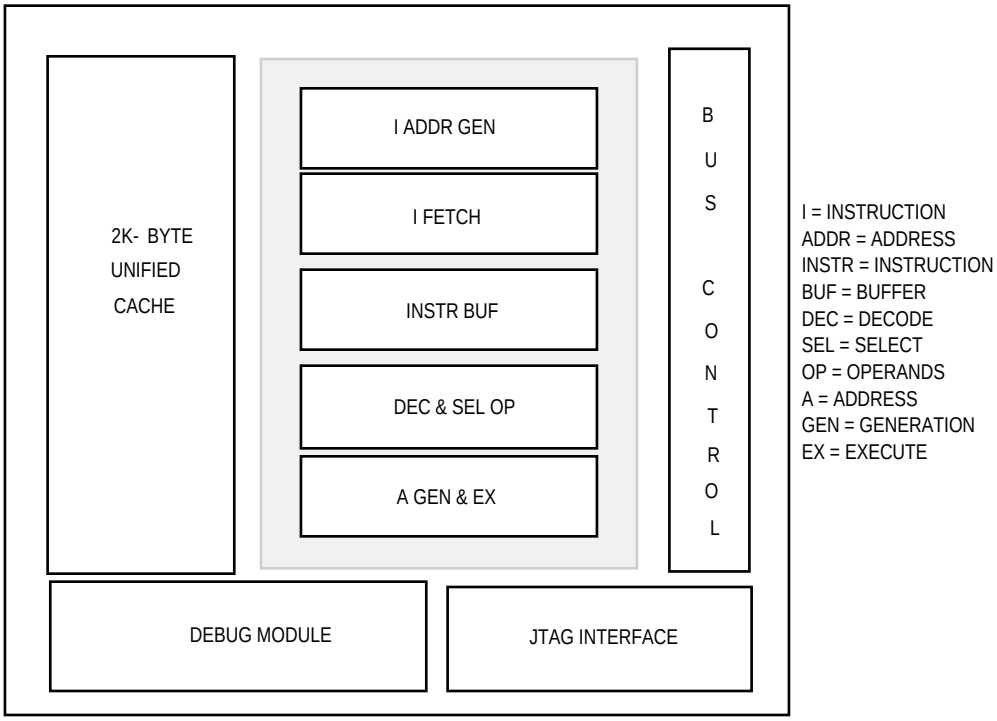

Figure 1. MCF5203 Block Diagram

COLDFIRE PROCESSOR CORE

The ColdFire processor core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, thereby minimizing time

stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC datapath with a dual-read ported register file feeding an arithmetic/logic unit.

UNIFIED CACHE

The MCF5203 processor contains a high-performance nonblocking, 2-Kbyte, four-way set-associative, unified (instruction and data) cache. The cache improves system performance by providing low latency data to the processor core. This decouples processor performance from system memory performance and increases bus availability for alternate bus masters.

The nonblocking design of the MCF5203 cache services read hits or write hits from the processor while a fill (caused by a cache allocation) is in progress. The cache can operate in either writethrough or copyback modes with no write-allocates for misses to writethrough memory.Cache design allows the MCF5203 to achieve 25MIPs performance at 33MHz.

The cache is organized as four-way set associative with 16-byte lines. Each line consists of an address tag and state information that shows line validity. In the cache, the state information indicates whether the line is invalid, valid, or dirty.

EXTERNAL BUS INTERFACE

The bus interface controller supports a high-speed, multiplexed, synchronous, external bus interface. The bus controller also provides a burst mode for fast data transfer for both reads and writes. The processor uses burst mode to update a single cache line (four longwords), minimizing cache update time. The bus controller performs burst write cycles to transfer four longwords to system memory, maximizing memory write performance. The bus controller operates concurrently with all of the other functional units of the device to maintain maximum system throughput.

The MCF5203 processor supports dynamic bus sizing. The MCF5203 device can access 8- and 16-bit memory and peripherals in the system. Control signals from the system indicate to the processor the width of the memory or peripheral being accessed during the given bus cycle.

DEBUG INTERFACE

The ColdFire processor core debug interface supports real-time trace and background-debug mode.

In real-time trace, four status lines provide information on processor activity in real time (PST pins). A 4-bit-wide debug data bus (DDATA) displays operand data, which helps track the machine’s dynamic execution path as the change-of-flow instructions execute.

A 4-pin background debug mode (BDM) interface provides system debug. The BDM is a proper subset of the BDM interface provided on Motorola’s 683xx family of parts.

JTAG

To help with system diagnostics and manufacturing testing, the MCF5203 processor includes dedicated user-accessible test logic that complies with the IEEE 1149.1 standard for boundary scan testability, often referred to as Joint Test Action Group (JTAG). For more information, refer to the IEEE 1149.1 standard.

POWER CONSUMPTION MANAGEMENT

The MCF5203 processor is very power-efficient because of static logic design. In addition to operating at slower frequencies to reduce power consumption, this processor can dynamically control power with the STOP instruction. This instruction shuts down active circuits in the processor and halts instruction execution. Processing can be resumed by resetting the part or by generating a valid interrupt.

PINOUT AND PACKAGE

The MCF5203 device is supplied in a 100-pin plastic thin-quad flat-pack package with the pinout shown in Figure 2.

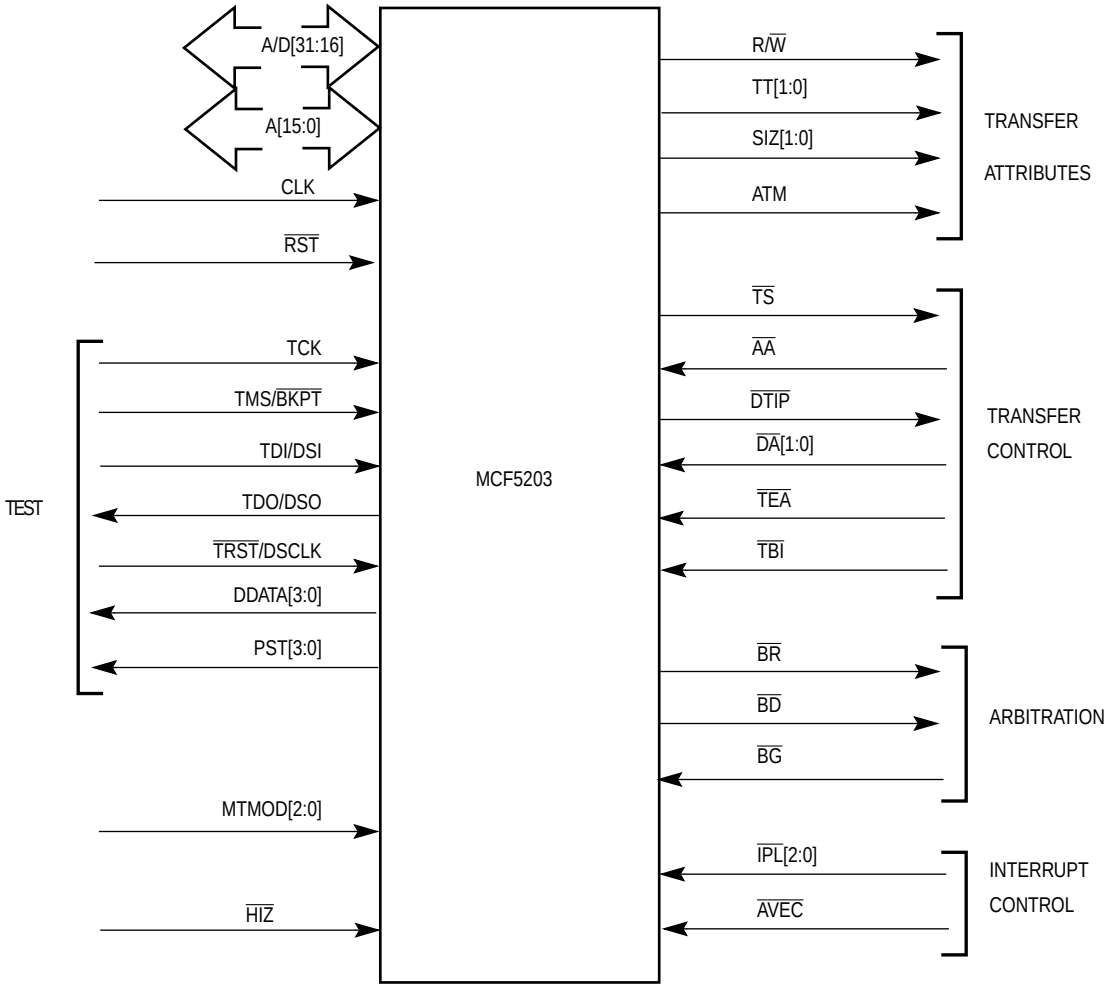

Figure 2. MCF5203 Pinout

MORE INFORMATION

The following table identifies the packages and operating frequencies available for the MCF5203 processor.

MCF5203 Package/Frequency Availability

	FREQUENCY		
PACKAGE	**16.67MHZ**	**25MHZ**	**33MHZ**
Thin Plastic Quad Flat Pack 100 lead	4Q96	4Q96	4Q96

The documents listed in the following table contain detailed information that pertain to the MCF5203 processor. These documents may be obtained from the Literature Distribution Centers at the addresses listed on the last page of this document.

MCF5203 Documentation

DOCUMENT NUMBER	DOCUMENT TITLE	AVAILABILITY
MCF5202UM/AD	MCF5202/ User's Manual (Includes MCF5203)	now
MCF5200PRM/AD	ColdFire Family Programmer's Reference Manual	now

DEVELOPMENT TOOLS AND EVALUATION SYSTEMS

For information on third-party development tools support, refer to the High Performance Embedded Systems Source (BR729/D).

ColdFire evaluation systems are available. Contact your local Motorola sales office for technical details and additional information on these boards.

Visit the Motorola web site at http://www.mot.com/coldfire for additional information on any ColdFire family product.

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SEMICONDUCTOR PRODUCT INFORMATION