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PRODUCT INFORMATION

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MC68LC040

Product Brief

Third-Generation 32-Bit Low-Power Microprocessor

The MC68LC040 is a high-performance, 32-bit, 3.3-V, static microprocessor that provides a low-power mode of operation. The MC68LC040 features dual on-chip caches, fully independent instruction and data demand-paged memory management units (MMUs), and a pipelined integer unit. A high degree of instruction execution parallelism is achieved through the use of a full internal Harvard architecture, multiple internal buses, and independent execution units. Accessed through the LPSTOP instruction, a low-power mode of operation is provided that allows for full power-down capability. The operating current is further reduced by the use of a 3.3-V power supply. The 3.3-V power supply and the low-power mode reduce system power usage dramatically. The functionality provided by the MC68LC040 makes it the ideal choice for a range of high-performance, power-sensitive, general computing and embedded processing applications.

The high level of integration results in high performance while reducing overall system power consumption for the MC68LC040. Complete code compatibility with the MC68000 family allows the designer to utilize existing code and past experience to bring products to market quickly. Additionally, a broad base of established development tools, including real-time kernels, operating systems, languages, and applications, assist in product development. Figure 1 shows a simplified block diagram of the MC68LC040.

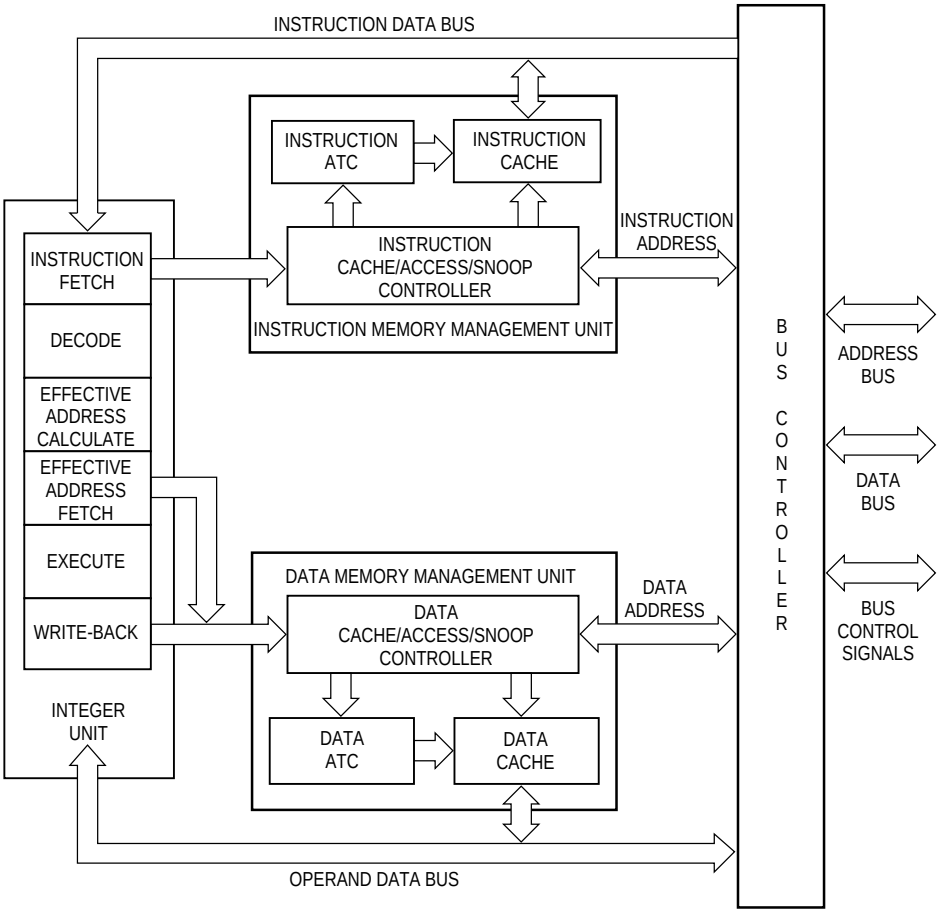

Figure 1. MC68LC040 Simplified Block Diagram

The primary features of the MC68LC040 are as follows:

- MC68040 Integer Performance
  —22 MIPS at 25 MHz and 29 MIPS at 33 MHz
- Independent Instruction and Data MMUs
- Dual 4-Kbyte On-chip Caches
  — Separate Data and Instruction Cache
  — Simultaneous Access
- Bus Snooping
  — Multi-Master and Multi-Processor Support
  — MC68LC040-Compatible Function
- Full 32-Bit Nonmultiplexed Address and Data Bus
  — 32-Bit Bus Maximizes Data Throughput
  — Nonmultiplexed Bus Simplifies Design
  — Provides for Highest Possible Performance
- Concurrent Operation of Integer Unit, MMUs, Caches, and Bus Controller Provides High Performance
- Power Consumption Control
  — Static HCMOS Technology Reduces Power in Normal Operation
  — Low-Voltage Operation at 3.3 V ±300 mV
  — LPSTOP Provides an Idle State for Lowest Standby Current
- 0–33 MHz
- 184-Pin Ceramic Quad Flat Pack

SIGNALS

Figure 2 shows the MC68LC040 signals in their functional groups. Three signals have been added to the MC68LC040: system clock disable ($\overline{SCD}$), loss of clock (LOC), and low-frequency operations ($\overline{LFO}$).

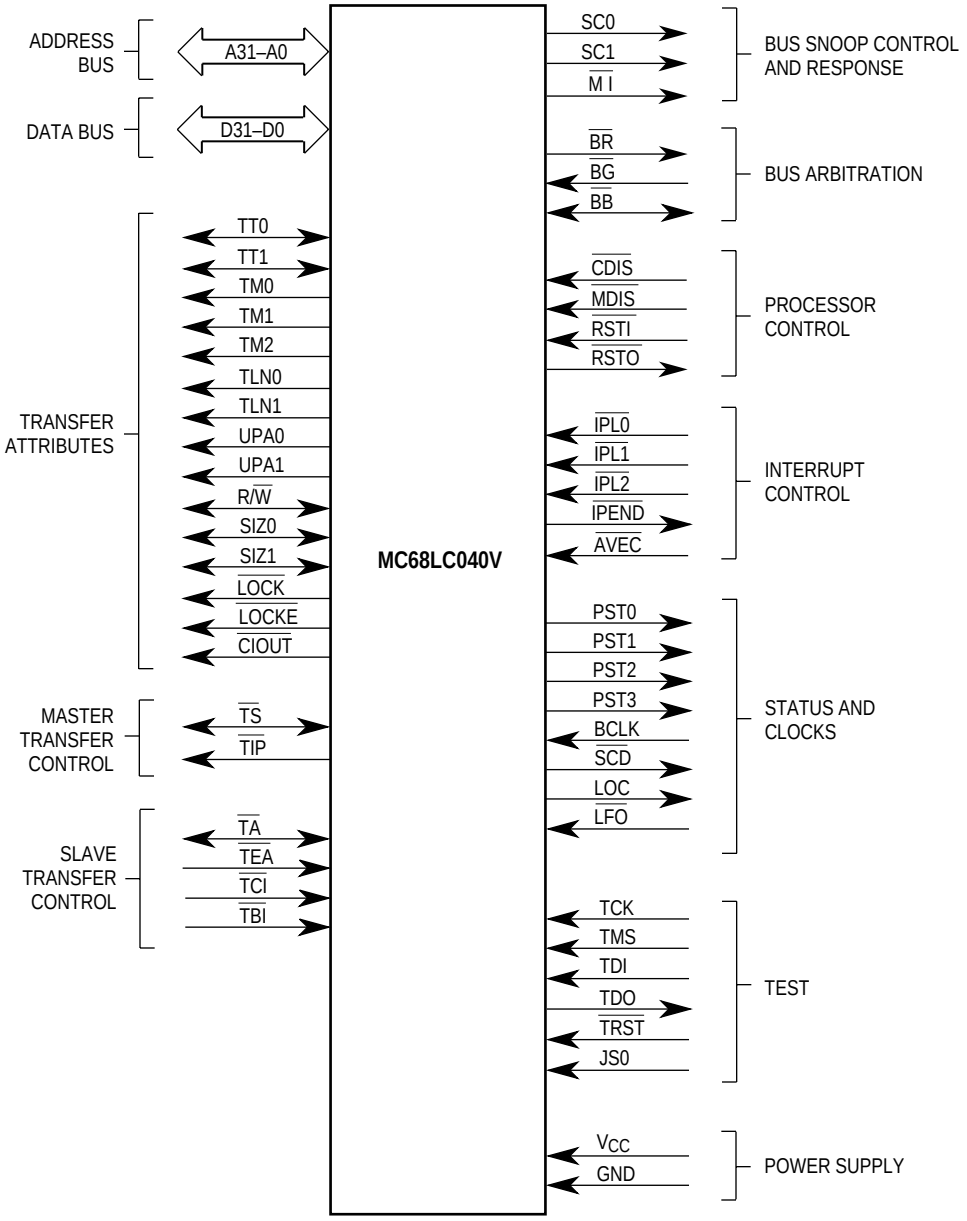

Figure 2. MC68LC040 Functional Signal Groups

INTEGER UNIT

The integer unit, which conducts logical and arithmetic operations on the MC68LC040, contains a six-stage integer execution pipeline. The pipeline allows the handling of six separate instructions simultaneously. The pipeline contains special shadow registers that can begin processing future instructions for conditional branches while the main pipeline is processing current instructions. This minimizes latency in the change of instruction flow, improving branch performance. The six stages of the pipeline are:

1. Instruction Fetch—Fetching an instruction from memory.
2. Decode—Converting an instruction into micro-instructions.
3. Effective Address <ea> Calculate—If the instruction calls for data from memory, the location of the data is calculated.
4. Effective Address <ea> Fetch—Data is fetched from memory.
5. Execute—The data is manipulated during execution.
6. Write-Back—The result of the computation is written back to on-chip caches or external memory.

The write-back stage holds the operand until the opportune moment when no data fetches are required. The write-back can defer writes indefinitely until either the data memory unit is free or another write is pending from the execution stage. Holding the data in the write-back stage maximizes system performance by not interrupting the incoming instruction or data stream.

MEMORY MANAGEMENT UNITS

The MC68LC040 contains independent instruction and data MMUs. Each MMU contains a 64-entry address translation cache (ATC) used to keep the most recently used translation. The full addressing range of the MC68LC040 is 4 Gbytes (4,294,967,296 bytes). Most MC68LC040 systems implement a much smaller physical memory, but by using virtual memory techniques, the system can appear to have a full 4 Gbytes of physical memory available to each user program. Each MMU fully supports demand-paged virtual-memory operating systems with either 4- or 8-Kbyte page sizes. Each MMU protects supervisor areas from accesses by user programs and also provides write protection on a page-by-page basis. For maximum efficiency, each MMU operates in parallel with other processor activities. The MMUs can be disabled for emulator and debugging support.

ADDRESS TRANSLATION

The ATCs store recently used logical-to-physical address translation information, as page descriptors, for instruction and data accesses. These caches are 64-entry, four-way, set-associative. Each MMU initiates address translation by searching for a descriptor containing the address translation information in the ATC. If the descriptor does not reside in the ATC, the MMU performs external bus cycles through the bus controller to search the translation tables in physical memory. After being located, the page descriptor is loaded into the ATC, and the address is correctly translated for the access.

TRANSPARENT TRANSLATION

Four transparent translation registers, two each for instruction and data accesses, are provided on the MC68LC040 MMU to allow portions of the logical address space to be transparently mapped and accessed without the need for corresponding entries resident in the ATC. Each register can be used to define a range of logical addresses from 16 Mbytes to 4 Gbytes with a base address and a mask. All addresses within these ranges are not mapped and are optionally protected against user or supervisor accesses and write accesses. Logical addresses in these areas become the physical addresses for memory access. The transparent translation feature allows rapid movement of large blocks of data in memory or I/O space without disturbing the context of the on-chip ATCs or incurring delays associated with translation table searches.

INSTRUCTION AND DATA CACHES

Studies have shown that typical programs spend much of their execution time in a few main routines or tight loops. Earlier members of the M68000 family took advantage of this locality of reference phenomenon to varying degrees. The MC68LC040 takes further advantage of cache technology with its two, independent, on-chip, physical caches, one for instructions and one for data. The caches reduce the processor's external bus activity and increase CPU throughput by lowering the effective memory access time. For a typical system design, the large caches of these devices yield a very high hit rate, providing a substantial increase in system performance.

The autonomous nature of the caches allows instruction-stream fetches, data-stream fetches, and external accesses to occur simultaneously with instruction execution. For example, if the processor requires both an instruction access and an external peripheral access and if the instruction is resident in the on-chip cache, the peripheral access proceeds unimpeded rather than being queued behind the instruction fetch. If a data operand is also required and it is resident in the data cache, it can also be accessed without hindering either the instruction access from its cache or the peripheral access external to the chip. The inherent parallelism also allows multiple instructions that do not require any external accesses to execute concurrently while the processor is performing an external access for a previous instruction.

Each cache is 4 Kbytes, accessed by physical addresses. The data cache can be configured as write-through or deferred copyback on a page basis. This allows for optimizing the system design for high performance with the deferred copyback writes to system memory.

Cachability of data in each memory page is controlled by two bits in the page descriptor. Cachable pages can be either write-through or copyback, with no write-allocate for misses to write-through pages.

A 16-byte write buffer maximizes performance by deferring writes from the integer execution pipeline back to the data cache until the cache is available to receive data. The instruction execution pipeline does not stall when data destined for the data cache is loaded into the write buffer. The write buffer effectively decouples the pipeline from the data cache, allowing one-clock-cycle writes.

CACHE ORGANIZATION

The instruction and data caches are each organized as four-way set-associative, with 16-byte lines. Each line consists of an address tag and state information that shows the line’s validity. In the data cache, the state information indicates whether the line is invalid, valid, or dirty.

CACHE COHERENCY

The MC68LC040 has the ability to snoop the external bus during accesses by other bus masters to maintain coherency between the caches and external memory systems. External cycles can be flagged on the bus as snoopable or nonsnoopable. When an external cycle is marked as snoopable, the bus snooper checks the caches for a coherency conflict based on the state of the corresponding cache line and the type of external cycle. External write cycles are snooped by both the instruction cache and data cache; whereas, external read cycles are snooped only by the data cache.

Although the internal execution units and the bus snooper circuit all have access to the on-chip caches, the snooper has priority over the execution units to allow the snooper to resolve coherency discrepancies immediately.

BUS CONTROLLER

The bus controller supports a high-speed, nonmultiplexed, synchronous, external bus interface. The bus controller also provides a burst mode for fast data transfer for both reads and writes. The processor uses burst mode to update a single cache line (four long words), minimizing the time it takes to update the cache. Burst write cycles are also performed by the bus controller to transfer up to 128 bits to system memory in five clock cycles, maximizing memory write performance. The bus controller operates concurrently with all of the other functional units of the device to maintain maximum system throughput.

IEEE 1149.1 TEST

To aid in system diagnostics, the MC68LC040 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

POWER CONSUMPTION MANAGEMENT

The MC68LC040 is very power efficient due to the use of a 3.3-V power supply static logic design. The resulting power consumption is typically 1.5 W in full operation @ 33 MHz—far less than microprocessors that use a 5-V power supply. The 3.3-V power supply reduces current consumption by 40–60% over microprocessors that use a 5-V power supply .

These processors have additional methods of dynamically controlling power consumption during operation. Running a special low-power stop (LPSTOP) instruction shuts down the active circuits in the processor, halting instruction execution. Power consumption in this standby mode is reduced to about 200 μA.

Processing and power consumption can be resumed by resetting the part or by generating an interrupt. The frequency of operation can be lowered to reduce current consumption when the device is in low-power stop mode.

PHYSICAL

The MC68LC040 is available as 0–33 MHz, 3.3 V ±300 mV supply voltages in a ceramic quad flat pack.

MORE INFORMATION

The following table identifies the packages and operating frequencies available for the MC68LC040.

MC68LC040 Package/Frequency Availability

Package	Frequency	
	25 MHz	33 MHz
Ceramic Quad Flat Pack (FE)	✔	✔

The documents listed in the following table contain detailed information that pertain to the MC68LC040. These documents may be obtained from the Literature Distribution Centers at the addresses listed on the last page of this document.

Documentation

Document Number	Document Title
BR1115/D	*M680x0 CPU Family*
M68040UM/AD	*M68040 User's Manual*
M68000PM/AD	*M68000 Family Programmer's Reference Manual*
BR729/D	*The 68K Source*
BR1407/D	*3.3 Volt Logic and Interface Circuits*

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nipon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-Pacific: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrail Estate, Tai Po, N.T., Hong Kong.