A/D CONVERSION SERIES — PART 2
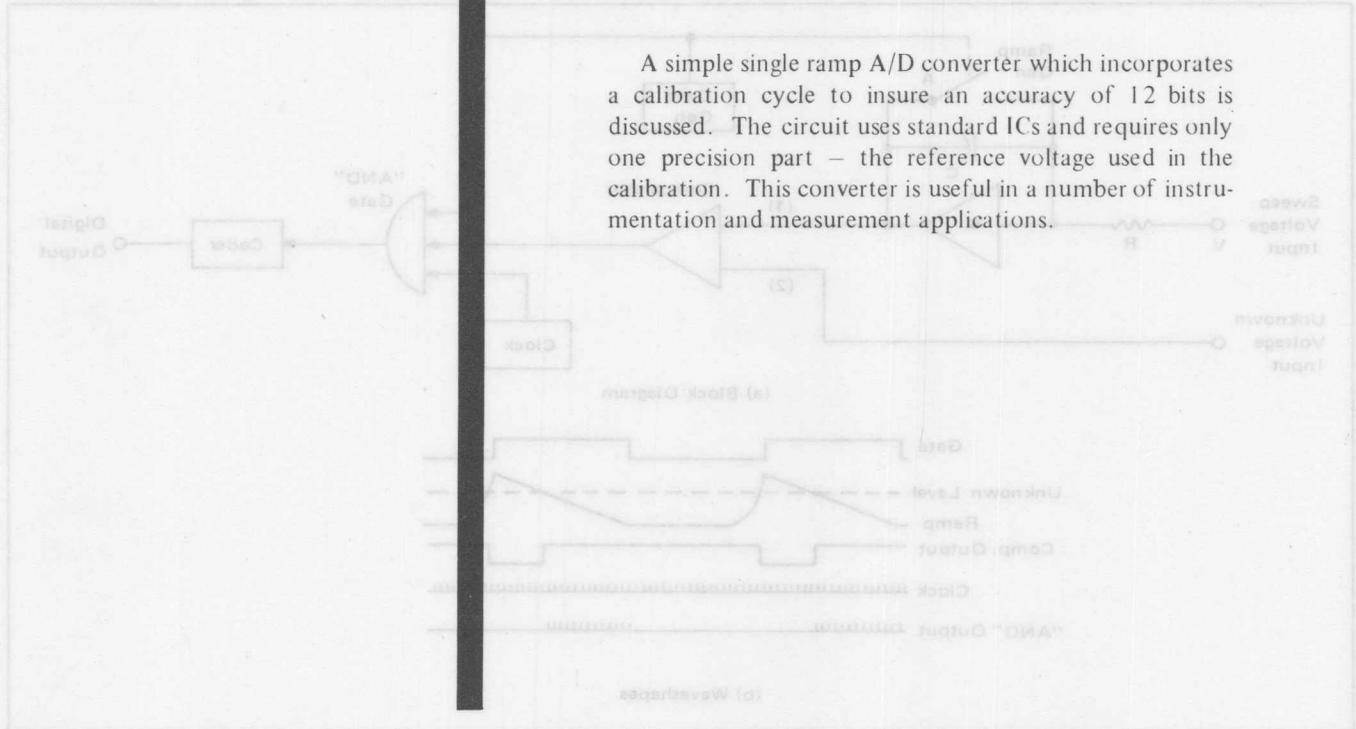
A SINGLE RAMP
ANALOG-TO-DIGITAL CONVERTER

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A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part — the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

MOTOROLA Semiconductor Products Inc.

A SINGLE RAMP ANALOG-TO-DIGITAL CONVERTER

INTRODUCTION

The current trend towards digital readout, both in laboratory test equipment and in industrial instrumentation has created a large demand for simple but accurate analog-to-digital (A/D) converters. However, the two words "simple" and "accurate" are usually contradictory; simple converters usually are not accurate.

As an aid to understanding the range of accuracies available in A/D converters, three general categories of accuracy might be identified; 2 to 6 bits, 6 to 10 bits, and greater than 10 bits. The lowest category, with accuracy up to about 1%, can be attained by most of the simple schemes. Digital panel meters usually fall in this class. The second class, 6 to 10 bits, with an accuracy up to 0.1% requires a more sophisticated approach and is represented by 3-1/2 digit digital volt meters (DVM). The final class which includes 4 and 5 digit DVMs and precision instrumentation, is the subject of this note.

Probably the simplest, and certainly the easiest to understand of the available A/D designs, is the single ramp converter. This converter generates a time gate signal whose length is proportional to the unknown analog voltage. This gate allows a series of oscillator clock pulses to pass into a counter. The number of pulses passed is proportional to the length of the gate pulse. These clock pulses are converted to a digital number in whatever code is desired: Binary, BCD, gray, or other.

The simple converter suffers from several inaccuracies; the voltage-to-time converter may be non-linear, its starting time and stopping time may be uncertain or it may have the wrong transfer gain. The clock pulse generator may introduce inaccuracies if it is too fast, too slow, or varies in frequency with time.

The following sections describe a method of correcting all these inaccuracies, except the non-linearity of the voltage-to-time converter. In brief, a known analog input is measured and the resulting digital number is compared to the correct answer. If this digital number is not correct, the converter is automatically adjusted so that the correct answer will be produced. This calibration cycle is interlaced with cycles which measure the unknown analog voltage, thereby providing compensation for all but the
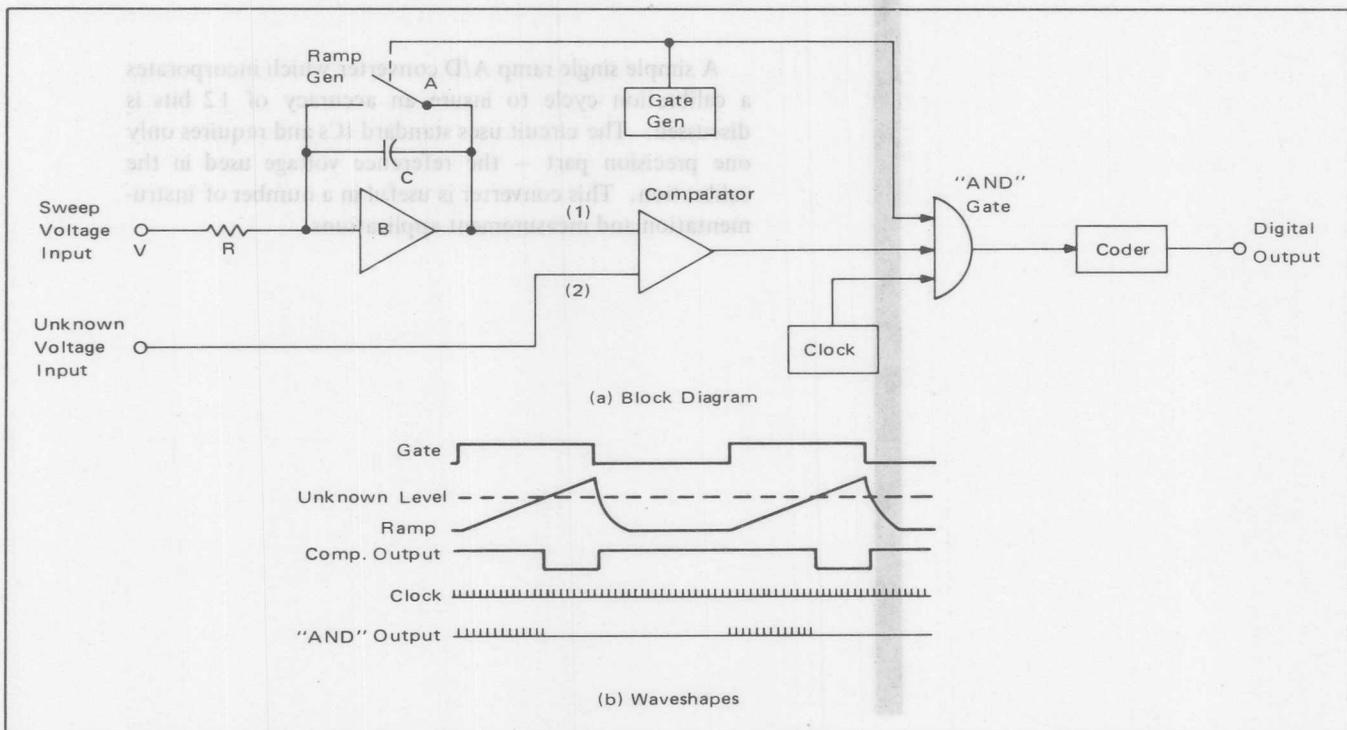

FIGURE 1 – Simplified Single Ramp A/D

most rapid variations in converter accuracy. The known input must, of course, be as accurate as the desired measurements. The explanation also describes a method which senses input signal polarity.

THEORY OF OPERATION

The ramp type A/D converter uses a linearly rising voltage ramp to convert an unknown voltage to an equivalent time interval. This time interval is used to gate a portion of the output of a clock-oscillator. The cycles of the oscillator which are passed by the time gate constitute a digital number proportional in value to the unknown voltage. The train of pulses is normally converted to a more usable number system such as binary, BCD, gray, etc. Figure 1 shows the single ramp A/D converter in a simple form. In general, some time is required for recovery of the ramp after each use, as well as for whatever digital operations that may be required to produce the type of digital word desired. Therefore, timing gates are required to separate the various operations. Figure 1(a) includes a simple arrangement to accomplish the desired gating, and Figure 1(b) shows typical waveshapes. Operation of the various components shown on the block diagram will now be described.

The ramp generator consists of an operational amplifier with a capacitor in the feedback path. The input is from a constant sweep voltage through a resistor. Because the operational amplifier input terminal remains at virtual ground, the current through the resistor is constant. This current is available to charge the capacitor, resulting in a linear ramp voltage. It is important that the ramp be linear, because this is the only significant source of error not corrected by the calibration cycle used in the A/D converter described in this note.

The comparator is also a high gain amplifier. Whenever input (2) is more positive than input (1), the comparator output is high, otherwise the output is low. The clock and gate generators are oscillators which produce the waveforms indicated. The "AND" gate has a positive output whenever all its inputs are positive, a zero output otherwise.

The coder may take various forms; for example, if binary code output is desired, the coder is a binary counter.

This simple type of A/D converter works extremely well if only a few bits of accuracy is required. However, as more accuracy is demanded, various errors begin to become apparent. The following paragraphs discuss these errors and describe a particular configuration which uses several techniques to reduce their effect.

There are two types of ramp errors (other than non-linearities); those related to slope, and those related to starting time. If the ramp starts late, fewer than the correct number of counts will be included. If the slope of the ramp is too steep, it will reach the unknown voltage too soon and fewer than the correct pulse count will be included. Comparator voltage offset and delay have an effect similar to errors in ramp starting time. If the ramp voltage must exceed the unknown voltage by a given amount to change the state of the comparator, the gate will close late and too many counts will be included. Likewise, comparator propagation delay will cause too many counts to be indicated for a similar reason. Taking the above errors in order; variations in ramp slope are caused by variations in the sweep voltage V, input resistance R, capacitance C, and to a much smaller extent, non-ideal parameters of the op amp B, and the reset switch A. Variations in ramp start time are caused by changes in the offset voltage and delay time of operational amplifier B.
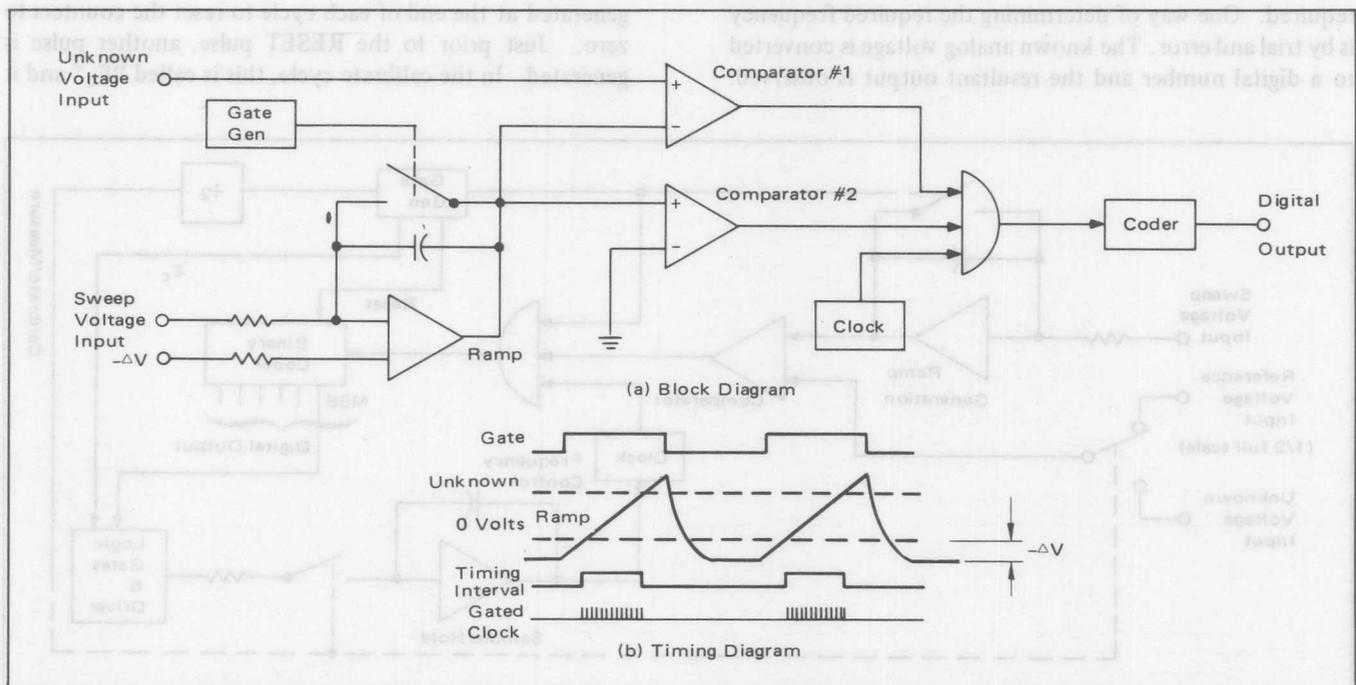

FIGURE 2 — Single Ramp Starting Below Zero

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It is desirable to employ some means of assuring that ramp delay errors be small, and react predictably to environmental variations. A frequently-used method is to start the ramp below the zero reference voltage as shown in Figure 2. Then the timing gate is opened by the ramp crossing the zero reference and closed by its crossing the unknown voltage. The two crossings are detected by identical comparator circuits and should therefore track each other well. Delays and non-linearities associated with ramp start-up are also eliminated by this technique. One small problem is created by this technique: It is very difficult to synchronize the clock with the opening of the timing gate because the gate opening is an analog event not related to the clock. This non-synchronization can result in a 1/2 least significant bit (LSB) error if the gating occurs during the rise time of the clock. With practical clock speeds and standard logic families, this error will occur less than 1% of the time.

The clock frequency, of course, has the same effect on count correctness as does ramp slope – if the clock is too slow it will not produce a sufficient number of pulses during the gate interval. Variations in clock frequency can be made small by use of a crystal or other high Q frequency determining device.

The previous discussions indicate that even if the counter is gated perfectly, there are still at least two factors which can cause errors; improper ramp slope and improper clock frequency. As mentioned previously, these are closely related because too fast a clock or too shallow a ramp slope both result in too many counts being gated. Therefore, if the clock frequency could be controlled, it could be used to compensate not only for its own drift, but also for ramp slope errors. (An alternate method would be to control the ramp slope.) Oscillator frequency can very easily be controlled if it is known what frequency is required. One way of determining the required frequency is by trial and error. The known analog voltage is converted to a digital number and the resultant output is observed.

If the output indication is too high, the clock could be slowed down and vice versa. Figure 3 shows a block diagram of such a calibration scheme. The voltage reference has been selected to be exactly half the full scale value of the converter. In a binary counter, the most significant bit is switched only under one condition, and this is at exactly half the full-scale count. This fact is utilized as will be seen later and is the main reason calibration of a binary system is done at the half-scale value.

If BCD counters are used, the MSB normally goes to a "one" at the count of 8 and returns to a "zero" at 10. In this case, calibration would be done at 80% of full scale rather than 50%.

In operation, the comparator is switched alternatively between the unknown voltage and the reference voltage. The MSB of the binary output is decoded so that it can be determined if the oscillator frequency is too high or too low. This decoded output, is converted to a bipolar dc voltage, and used to control the oscillator frequency. Because this calibration output can, at most, be available 25% of the time (and in the instrument shown here is available a much smaller percentage of the time), a means must be provided to store the value when it is not present at the decoder output. In the system shown, an integrating operational amplifier is used in a sample and hold circuit.

The capacitor and charging resistor values are selected so that the voltage resulting from an error will correct the oscillator frequency by an amount corresponding to about LSB/4. The benefit of using the most significant bit (MSB) is that its decoding always provides the proper error sense, even when large errors are present. This is true because the MSB only changes state once at half of the full count.

Figure 4 shows the waveshapes generated for control of the A/D converter. Note that there are alternating CALIBRATE and MEASURE cycles. A RESET pulse is generated at the end of each cycle to reset the counters to zero. Just prior to the RESET pulse, another pulse is generated. In the calibrate cycle, this is called "E_c" and it
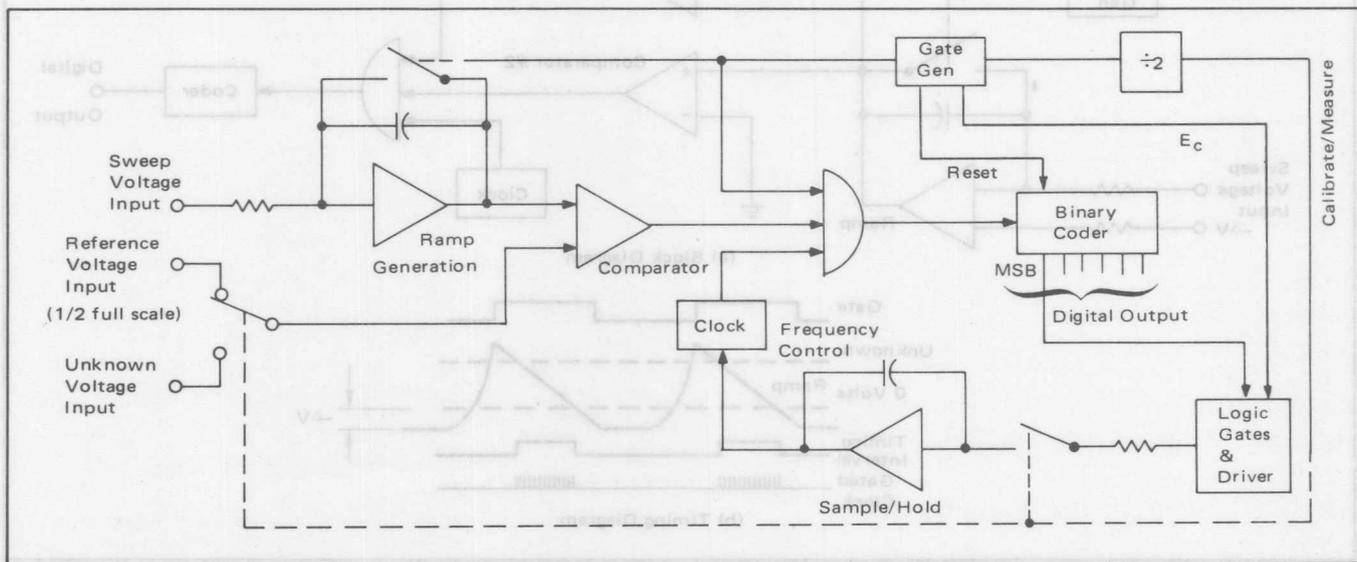

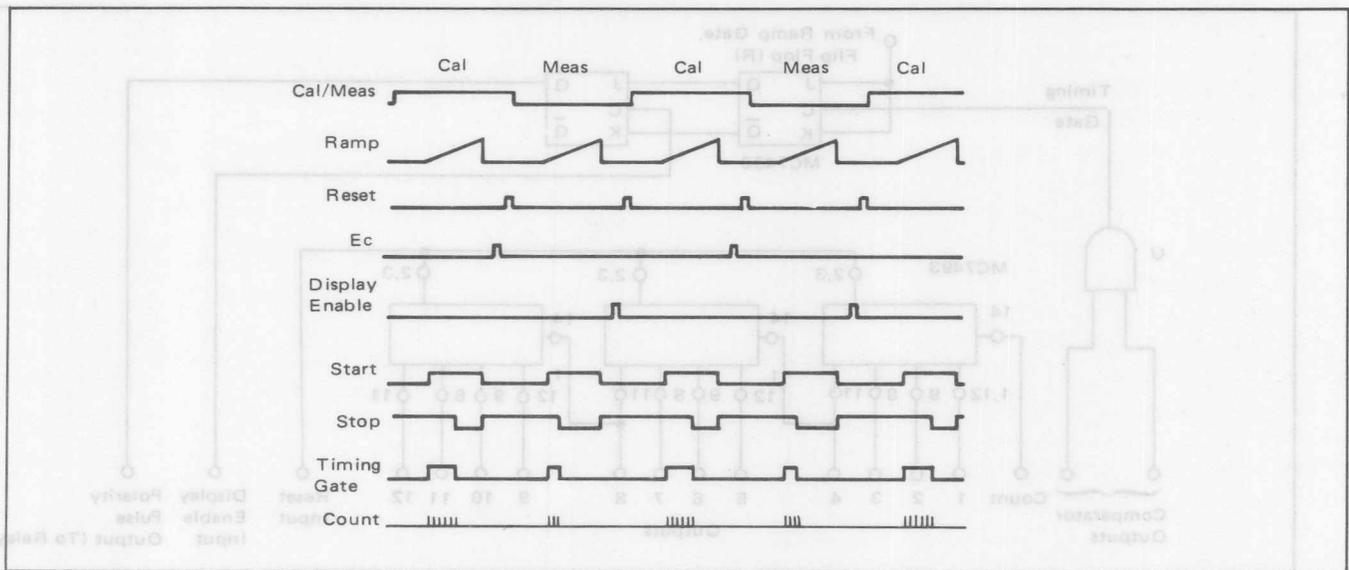
FIGURE 3 – Calibration Block Diagram

FIGURE 4 — System Waveshapes

is used to gate the error signal into the sample-and-hold circuit. In the MEASURE cycle this pulse is called DISPLAY ENABLE and is used to latch the digital equivalent of the unknown analog voltage into the output display.

The error voltage changes rapidly during the "E_C" pulse and remains constant between pulses. With large errors, such as might be present for a few seconds when the unit was first turned on, a staircase error waveshape would be produced, but at near zero error, the MSB error decoder output will be toggling between a plus and minus value to produce a squarewave. This toggling during the calibration cycle has no real effect on the measuring cycle because the oscillator frequency is only being shifted an amount corresponding to LSB/4 which is less than the resolution of the converter.

This converter, as so far described, cannot distinguish between a negative input voltage and zero input. It gives a zero output for either one. To correct this situation, additional circuitry is required. If a zero or negative input voltage is applied, we note that during the MEASURE cycle a STOP pulse is generated before or simultaneously with the START pulse, or in other words: no TIMING GATE is generated. In this event, it is desired that the input polarity be reversed with a mechanical relay. If no TIMING GATE is present during the following MEASURE cycle, as would be the case with zero input, the input should again be reversed. Hence, with an exactly zero voltage input, the input switch should be reversed once each cycle, and the plus and minus sign should likewise alternate at the cycle rate.

The electronics to accomplish the above polarity sensing is implemented as follows: polarity is indicated by a J-K flip-flop, S, connected so it will change state every time it receives a negative going pulse. The TIMING GATE is connected to its input so that each occurrence of a TIMING GATE signal will trigger the flip-flop S. Use of the negative edge triggering assures that the flip-flop will not trigger

until the end of the TIMING GATE, i.e., after the measurement is completed. Thus this flip-flop triggers when the ramp crosses either the unknown or Reference voltage level.

In operation, flip-flop S changes state at the end of each measurement of a positive voltage. The TIMING GATE which is always present during the CALIBRATE cycle (because the reference voltage is always positive) returns the flip-flop S to its original state, ready for the next measurement. However, if the input is negative or zero, only the CALIBRATE cycle TIMING GATE will be present, so the state of flip-flop S would alternate for each cycle.

A second J-K flip-flop, T, is connected to flip-flop S such that its state is forced to be the same as that of flip-flop S at the time of the DISPLAY ENABLE pulse. With two flip-flops connected in this way, the polarity relay (and readout) will only be activated under the conditions that the unknown input is either negative or exactly zero voltage.

FEASIBILITY MODEL

A prototype model A/D converter was constructed which utilized all the techniques previously discussed. The linear voltage ramp is started at a voltage below ground potential. Two comparators are used, the first to generate a START signal at the time the ramp crosses zero volts, and the second to generate the STOP signal when the ramp crosses the voltage being measured. Two cycles of operation are used: CALIBRATE and MEASURE. During the CALIBRATE cycle a voltage equal to one-half of full scale voltage is measured and the resulting count compared to the known correct count. If the counts are different, the resultant error voltage is used to adjust the clock frequency.

Standard IC operational amplifiers and the MTTL family of IC digital devices are used in the feasibility model. Figure 5 is the schematic diagram.

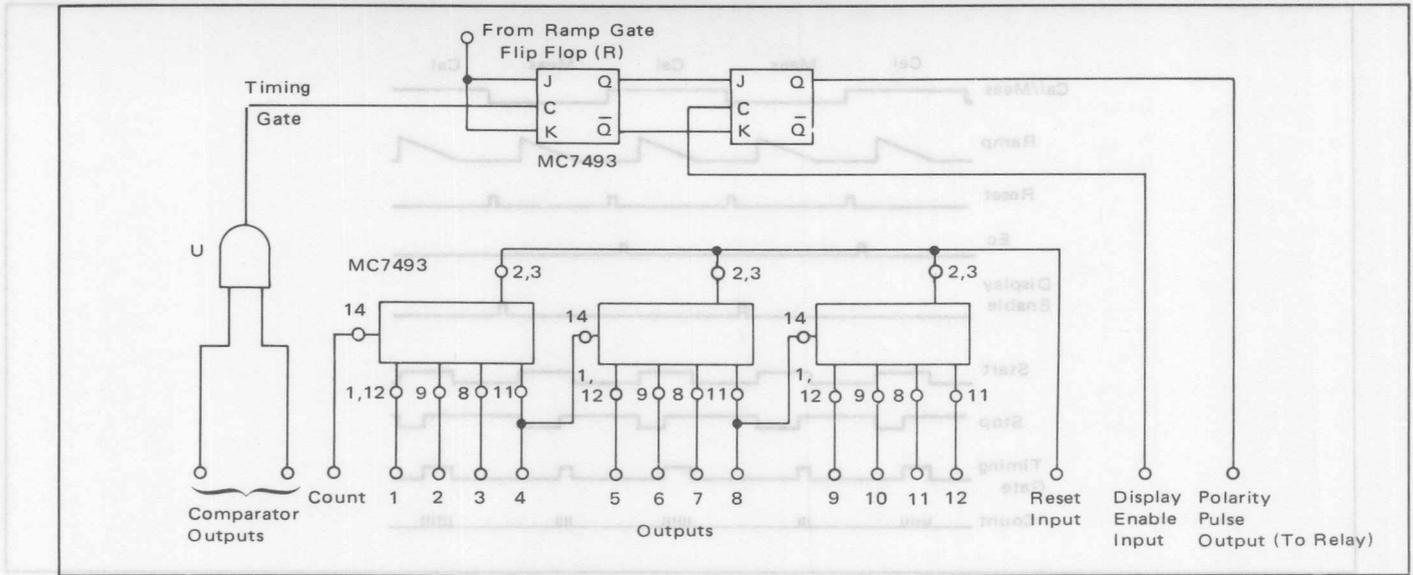The components were assembled on two PC boards, the

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FIGURE 5 (a) — Schematic of Counting Circuit

From Ramp Gate
Flip Flop (R)

Timing
Gate

J Q   J Q
C   C
K Q̄   K Q̄

MC7493

MC7493

U

14   14   14

2,3   2,3   2,3

1,12 9 8 11   1,12 9 8 11   1,12 9 8 11

Comparator
Outputs

Count 1 2 3 4   5 6 7 8   9 10 11 12   Reset   Display   Polarity
                                                    Input   Enable   Pulse
                Outputs   Input   Output (To Relay)

RAMP VOLTAGE
GENERATOR

–15 V
100 k   2.2 k
MPS6514
A
2000 pf
1M
Sweep
Voltage
Input
220
B MC1741
10 k

RAMP POLARITY INVERTER

–15 V
2.2 k
B Negative
Output
Voltage
22 k
22 k
A Positive
Input
Voltage
C
MPS6517

COMPARATOR/GATE

+15 V
MLM101A
3   6
2   F
8
1
3 pf
5.1 k
5.1 k
1 k
3 pf
2   1   8
3   G   6
MLM1014
5.1 k
To Inputs
of Gate U

15 k
13
2   12
1   I
15 k   MC3001

REFERENCE UNKNOWN SWITCH

+15 V
100 k
MFE 4012
Reference
Voltage
Input
gnd
91
91
2N5364
E
Unknown
Voltage
Input
100 k
Polarity
Reversing
Relay
2.7 k
MPS6514
H
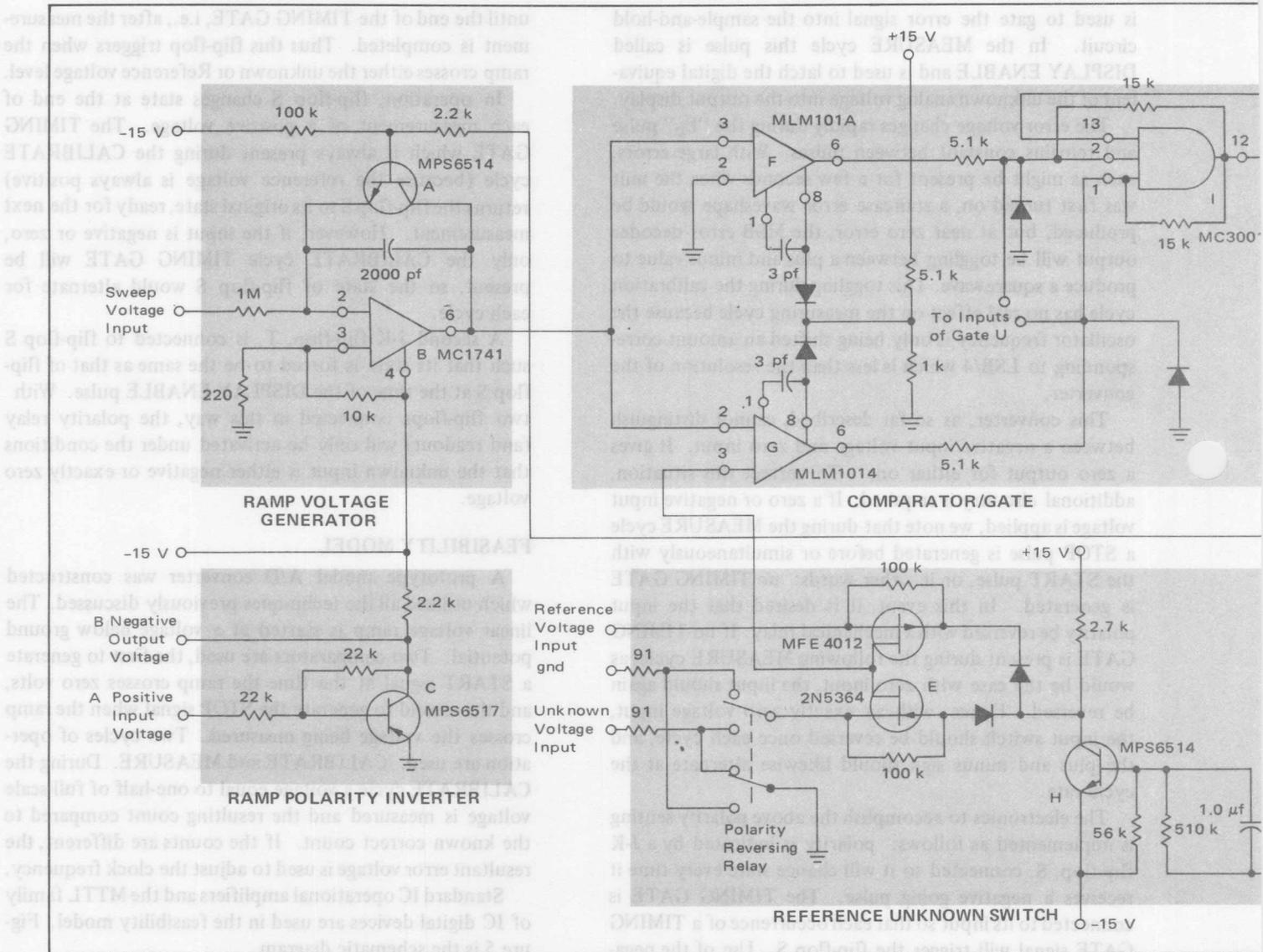56 k   510 k   1.0 µf
–15 V

FIGURE 5 (b) –

first including all the circuitry of Figure 5(a), and the second the circuitry of Figure 5(b), (b) being the basic A/D converter, (a) being the counter and output word coder. Components A and B of Figure 5(b) make up the ramp generator; the transistor switch, when open, allows the ramp to rise. Values are selected so that the ramp reaches its maximum value of nearly +15 volts in about 3 milliseconds. The resistors connected to the non-inverting input of the operational amplifier cause the ramp to start below 0 volts allowing comparator F to sense the ramp zero crossing.
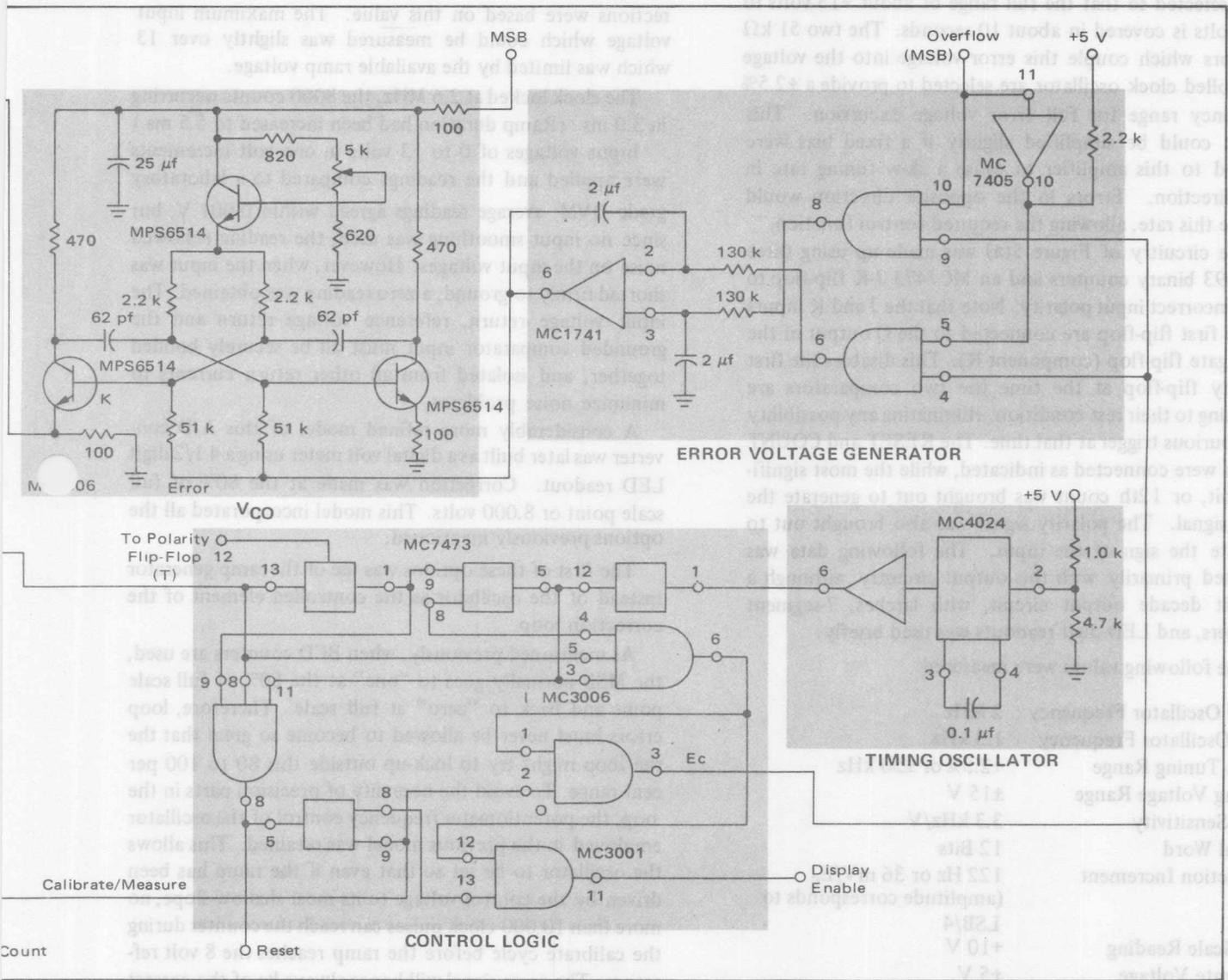
Transistor C is provided on the board to increase the versatility of the circuit. A negative voltage is required for the SWEEP INPUT. This may be provided from an external source or, by use of the inverter C, may be derived from the positive reference voltage or the +5 volts supply.

Components, D, E, and H are the switches which alternate the converter input between the unknown analog input being measured and the known reference voltage. Complementary FET switches are used so that the same wave_____pe can be used to control both switches.

Components F and G are the two comparators which sense the time when the ramp voltage crosses zero volts and either the reference voltage or the unknown voltage. Their outputs, in conjunction with component I, gate the appropriate number of clock counts to the output.

The two resistors from the inputs of component I to its output provide positive feedback which eliminates any tendency the gate might have to oscillate because of the rather slow pulse transitions from the comparators.

The clock oscillator is an RC multivibrator consisting of transistors K and M. Transistor L is a current source used to provide a small degree of isolation from the +15 volt supply. The potentiometer in the base of transistor L sets the oscillator operating range, providing a coarse frequency control. Note that use of the previously mentioned alternate control system — control of ramp slope rather than oscillator frequency — would allow use of a simple crossed-gate fixed frequency oscillator.

ERROR VOLTAGE GENERATOR

TIMING OSCILLATOR

CONTROL LOGIC

_____verter Schematic

All the timing gates originate from the oscillator which is one half of component P. Flip-flops R and Q provide suitable frequency divisions, while gates I and O supply the various gates shown in Figure 4.

The last remaining circuit, made up of operational amplifier N and parts of the gate circuit O, is the sample and hold circuit used to generate the error control signal which is the principal advantage of this type of A/D converter. The sense determining signal; the most significant bit in a binary counter or the overflow from the last decade of a BCD counter, gates the input to either the inverting or the non-inverting input of operational amplifier N. The other gated signal, called E_c, is a pulse, generated only during the calibrate cycle, which occurs after the calibrate count has settled, but just prior to counter reset. The two 2 μF capacitors hold the error signal constant except during the E_c gate, and also in conjunction with the two input resistors, determine the amplitude of error signal generated when either input is gated on. These values were selected so that the full range of about +15 volts to −15 volts is covered in about 10 seconds. The two 51 kΩ resistors which couple this error voltage into the voltage controlled clock oscillator are selected to provide a ±2.5% frequency range for full error voltage excursion. This circuit could be simplified slightly if a fixed bias were applied to this amplifier to cause a slow tuning rate in one direction. Errors in the opposite direction would reverse this rate, allowing the required control function.

The circuitry of Figure 5(a) was made up using three MC7493 binary counters and an MC7473 J-K flip-flop to sense incorrect input polarity. Note that the J and K inputs of the first flip-flop are connected to the Q output of the ramp gate flip-flop (component R). This disables the first polarity flip-flop at the time the two comparators are returning to their rest condition, eliminating any possibility of a spurious trigger at that time. The RESET and COUNT inputs were connected as indicated, while the most significant bit, or 12th count was brought out to generate the error signal. The polarity signal was also brought out to indicate the sign of the input. The following data was obtained primarily with this output circuitry, although a 4 digit decade output circuit, with latches, 7-segment decoders, and LED digit readouts was used briefly.

The following values were measured:

Clock Oscillator Frequency	2 MHz
Gate Oscillator Frequency	1.3 kHz
Clock Tuning Range	+2.5% or ±50 kHz
Tuning Voltage Range	±15 V
VCO-Sensitivity	3.3 kHz/V
Digital Word	12 Bits
Correction Increment	122 Hz or 36 mV/E_c (amplitude corresponds to LSB/4
Full Scale Reading	+10 V
Calibrate Voltage	+5 V
Calibrate Time	1.024 ms

Sweep Time (ramp)	3.1 ms
Overrange	1.052 ms or 50%
Correction Rate	10 Hz/ms
Maximum Correction Time	10 seconds
Voltage Ramp Slope	5 V/ms

The error voltage, i.e., the dc voltage applied to the clock VCO, was observed to toggle each calibrate cycle. Occasionally when a power supply transient occurred, two or three corrections would be made in the same direction indicating a momentary error of 1/2 or 3/4 LSB. This indicates that accuracy was almost always within ±LSB/4 and peak errors did not exceed +LSB/2.

Only one manual control is used in this circuit, a potentiometer, to displace the VCO lock-in range by about ±25%. Its adjustment is very non-critical.

The converter was also tested with a 4-1/2 digit BCD counter and display. The signal used for calibration was the 8000 count output (this is the BCD MSB). A reference voltage of 8.000 volts was used and clock frequency corrections were based on this value. The maximum input voltage which could be measured was slightly over 13 which was limited by the available ramp voltage.

The clock locked at 2.6 MHz, the 8000 counts occurring in 3.0 ms. (Ramp duration had been increased to 5.5 ms.)

Input voltages of 0 to 13 volts in one volt increments were applied and the readings compared to a laboratory grade DVM; average readings agreed within 0.001 V, but since no input smoothing was used, the reading followed noise on the input voltages. However, when the input was shorted firmly to ground, a zero reading was obtained. The input voltage return, reference voltage return and the grounded comparator input must all be securely bonded together, and isolated from all other return currents to minimize noise problems.

A considerably more refined model of this A/D converter was later built as a digital volt meter using a 4 1/2 digit LED readout. Correction was made at the 80% of full scale point or 8.000 volts. This model incorporated all the options previously mentioned.

The first of these options was use of the ramp generator instead of the oscillator as the controlled element of the correction loop.

As mentioned previously, when BCD counters are used, the MSB normally goes to "one" at the 80% of full scale point and back to "zero" at full scale. Therefore, loop errors must never be allowed to become so great that the the loop might try to lock-up outside this 80 to 100 per cent range. To avoid the necessity of precision parts in the loop, the potentiometer frequency control of the oscillator employed in the previous model was retained. This allows the oscillator to be set so that even if the ramp has been driven by the control voltage to its most shallow slope, no more than 10,000 clock pulses can reach the counter during the calibrate cycle before the ramp reaches the 8 volt reference. The error signal will hence always be of the correct polarity to drive the ramp up until the proper 8,000 pulses

are reached when the ramp crosses the 8 volt reference, at which point the loop locks.

The ramp generator and the integrating amplifier which provides the error control voltage are shown in Figure 6(a).
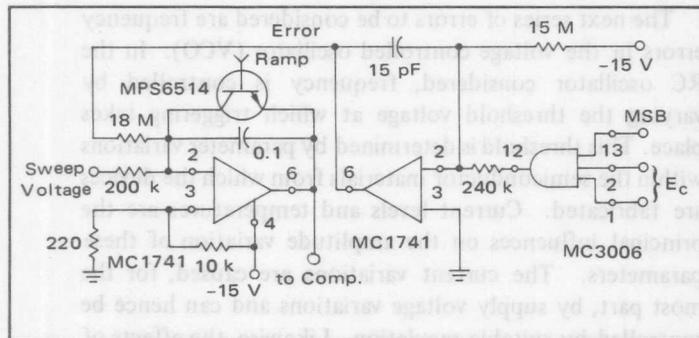

FIGURE 6(a) — Ramp and Error Generator

The error input to the integrating amplifier is single-ended, i.e., error pulses are supplied only when the gate count is too high, control in the other direction being provided by a fixed bias as was discussed previously as an option. With no error pulses the integrated error signal drifts slowly positive, while with continuous error pulses, it steps more negative at the same average rate.

Another feature of this model, not previously mentioned, is the use of the 60 hertz line frequency to synchronize the system as shown in Figure 6(b). This improves
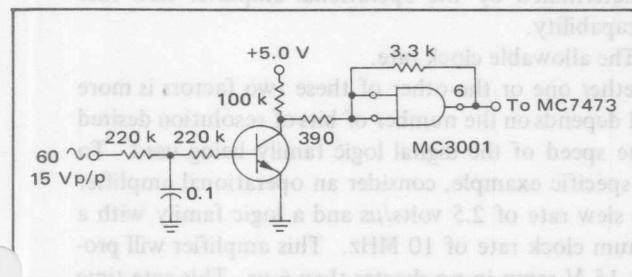

FIGURE 6(b) — Line Synchronous Circuit

the appearance of the display when a digital readout is used, since the voltage under measurement frequently has a small 60 hertz component. When the sampling rate is synchronized with this "hum", the reading is always taken at the same point in the "hum" waveshape so the last digit is less prone to fluctuate. The actual reading obtained is, of course, the input voltage at this instant and may not be the RMS value of the input signal plus hum.

Another small difference between this model and the previous is the use of a potentiometer to vary the offset of one of the comparators. This forms a zero offset adjust for the instrument and allows the output to read zero for a non-zero input, a condition sometimes desirable when the input comes from a transducer. This adjustment allows the use of a less precise operational amplifier, the MLM 301A, for the comparators. Figure 6(c) shows the circuit.

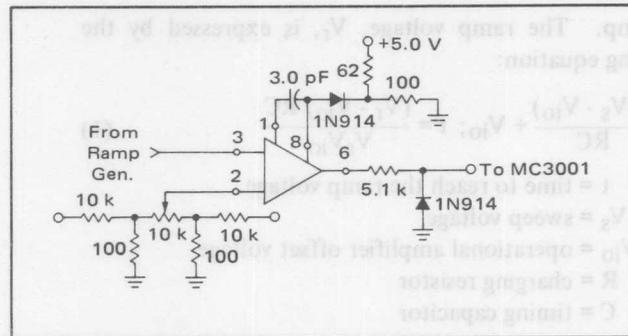Figure 7 shows a photo of a laboratory A/D converter of this type.

FIGURE 6(c) — Offset Adjustment

CONCLUSION

The application of feedback techniques to the single ramp A/D converter for the purpose of improving its long-term accuracy is very feasible. The model which was constructed worked very well, displaying an accuracy of about 1 part in 10,000. Advantages of the technique include simplicity of concept, non-criticalness of components and extremely good long term accuracy. The only precision element required is the reference voltage; the system accuracy is proportional to the reference voltage accuracy. A further advantage which makes this technique unique is: the correction loop may be closed around the entire system (except for the polarity reversing relay). For example, if a scaling amplifier is used, this amplifier can be included in the loop and any variations in its characteristics will be cancelled out.

The speed of the unit constructed was about 85 measurements per second. By use of MECL logic this rate could, in principal, be increased to more than 5000 measurements per second.

APPENDIX

The following paragraphs present a brief examination of the errors encountered in the A/D converter previously described.

RAMP VOLTAGE ERRORS

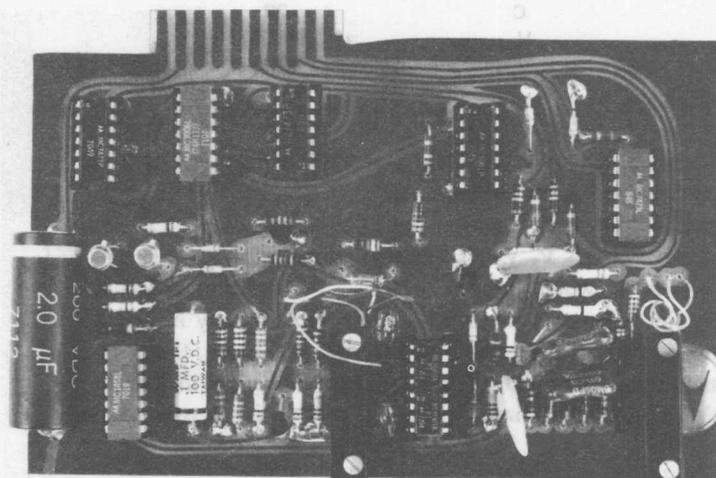The errors to be considered first concern the timing of

FIGURE 7 — A/D Converter

the ramp. The ramp voltage, V_r, is expressed by the following equation:

$$V_r = \frac{t(V_s - V_{io})}{RC} + V_{io}; \quad t = \frac{(V_r - V_{io})RC}{V_s V_{io}} \quad (1)$$

where: t = time to reach the ramp voltage
V_s = sweep voltage
V_{io} = operational amplifier offset voltage
R = charging resistor
C = timing capacitor

This ramp voltage is compared, first with zero volts, then with the unknown voltage to produce a time interval proportional to the magnitude of the unknown voltage. The time of zero crossing, t_o, is:

$$t_o = \frac{(V_{iol} - V_{io})RC}{V_s - V_{io}} + t_{pi} \quad (2)$$

where: V_{iol} = comparator #1 offset voltage
t_{pi} = comparator #1 propagation time

The time of crossing the unknown voltage level is:

$$t_1 = \frac{(V_u - V_{io} + V_{io2})RC}{V_s - V_{io}} + t_{p2} \quad (3)$$

where: V_u = unknown voltage
V_{io2} = comparator #2 offset voltage
t_{p2} = comparator #2 propagation time

The desired time interval, $\triangle t$, is then obtained by subtraction:

$$\triangle t = t_1 - t_o = \frac{(V_u + V_{io2} - V_{io1})RC}{V_s - V_{io}} + t_{p2} - t_{p1} \quad (4)$$

The partial derivitive of this expression is taken with respect to each variable. It is then noted that, for the worst case,

$$V_u = 2V_s \quad (5)$$

This value is substituted into each partial derivitive to give the values listed in Table 1.

TABLE 1 PARTIAL DERIVITIVES

With respect to:	Worst case value:
R	2C
C	2R
V_u	RC/V_s
V_s	$2RC/V_s$

These values indicate that, for worst case, the gate time is sensitive to the three parameters, R, C, and V_s in a ratio of 2:1. In other words, if one of these values, such as the sweep voltage V_s varies 10% the time gate ($t_1 - t_0$) will vary 20% (worst case). Because a periodic correction is employed to remove long term errors, it is only noise on these quantities which is of interest. Of these, the most significant is noise on the reference voltage. This can in theory be minimized by using proper by-passing pro-

cedures. If thin film resistors are used, resistor noise is typically reduced to 0.1 μV per volt. Capacitor noise is even less significant. Ramp timing errors, therefore, compute to be very small.

VCO ERRORS

The next series of errors to be considered are frequency errors in the voltage controlled oscillator (VCO). In the RC oscillator considered, frequency is controlled by varying the threshold voltage at which triggering takes place. This threshold is determined by parameter variations within the semiconductor materials from which the devices are fabricated. Current levels and temperatures are the principal influences on the amplitude variation of these parameters. The current variations are caused, for the most part, by supply voltage variations and can hence be controlled by suitable regulation. Likewise, the effects of temperature variations are removed by the periodic calibrations. However, at any given temperature and current level, there is still a frequency jitter caused by a combination of thermal noise in the resistors and semiconductors, and residual supply voltage noise. In the feasibility model described in the previous paragraphs, this residual noise resulted in converter errors of about one part in 10,000.

OPERATING SPEED

The speed of operation of a ramp type A/D converter is dependent upon two major factors:

1. The maximum slope of the ramp voltage which is determined by the operational amplifier slew rate capability.
2. The allowable clock rate.

Whether one or the other of these two factors is more critical depends on the number of bits of resolution desired and the speed of the digital logic family being used. To give a specific example, consider an operational amplifier with a slew rate of 2.5 volts/μs and a logic family with a maximum clock rate of 10 MHz. This amplifier will produce a 15 V ramp in no shorter than 6 μs. This gate time interval will pass 60 clock pulses. To assure 1/2 least significant bit accuracy, twice the number of pulses as there are bits of resolution must be used. This imposes a critical resolution of 5 bits with 60 clock pulses. If greater than 5 bits are required, speed will be limited by the clock speed, while for less than 5 bits, the ramp slew rate places a limitation on speed. If a high speed logic family, like MECL, which allows clock speeds of greater than 200 MHz is used, the critical resolution with a 2.5 V/μs ramp generator is computed to be 9 bits.