Interfacing National's DP8466A to the SMD Storage Module Device Interface Standard (Hard Sectored Drive)

National Semiconductor
Application Note 501
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March 1987

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AN-501

1.0 INTRODUCTION

With the advent of computer technology, the demand for high performance memory devices has been increasing. Before the introduction of 5¼ and 8 inch Winchester disk drives in the late 1970's, minicomputers and mainframes were the only systems that utilized rigid disks. Storage capacity, data transfer rates and to some extent cost, are the main factors which determine the performance of Winchester drives. The data transfer rate is highly dependent on the interface protocol adopted by the drive and also the electronics. The defacto industry standard drive interface for low end systems, ST506 by Seagate Technology, supports a maximum data transfer rate of 5 Mbits/sec and requires the disk controller to take care of data separation (synchronization and decoding). With the intention of supporting higher data transfer rates, newer standards were defined, like the ESDI (Enhanced Small Device Interface), which incorporates data separation on the drive itself and supports a data transfer rate of 10 Mbits/sec. The intelligent disk interface standards like SCSI and IPI, incorporate an interface to the host system with a well established high level communication protocol, however they also need to incorporate a drive-level interface like ESDI, SMD, etc.

With the intention of standardization of a common interface and to prevent product obsolescence, Control Data Corporation developed an intelligent interface called the Storage Module Device (SMD). This interface allows different drives to use the same hardware signals, even though their capacities and physical sizes were different. Variations of the SMD were also introduced. SMD started out at 9.667 Mbits/s data transfer rate and has since gone through several upgrades to a 24 Mbit/s option (SMD-E), introduced recently by Control Data Corporation. The SMD disk interface is a high quality proven attachment and is well on its way to becoming a defacto industry standard. It incorporates error recovery facilities, includes power sequencing for multiple units and is adaptable to many different rigid-disk storage units. Although it requires two very bulky and expensive cables, in high-end products this is an acceptable drawback and SMD still remains a popular choice for the higher capacity 5¼ and 8 inch Winchesters. It offers several advantages over the ST506 type interface in the high capacity arena (like parallel seek instead of serial step pulses and better status reporting), however, it is not a trivial interface when it comes down to designing a controller.

This application note looks into the definition of the SMD interface and the various design aspects of building a Disk Controller for a hard sectored drive supporting the SMD interface, using National Semiconductor's Disk Data Controller IC, DP8466A (DDC). Emphasis is laid on the disk interface design as that is of relevance to the DDC. The DDC is the most versatile LSI disk controller in the market today, offering fully programmable format features, maximum range in data rate (50 Kbits/s to 25 Mbits/s, dual DMA capability with a transfer rate of 10 Mbytes/sec, programmable error checking and correction and many other features which makes the design of a disk controller simpler and less complex. To be able to support high performance drives in the future, disk controller IC's must be capable of handling data transfer rates $>$20 Mbits/s. The DDC concentrates on the high speed data path signals, while the slower drive control operations are left to an inexpensive microcontroller, or the local (on board) microprocessor. The DDC in conjunction with this local intelligence, can achieve the Disk Controller function which was accomplished by 100–150 SSI/MSI integrated circuits in earlier Disk Controller systems, minimizing complexity, cost and system overhead.

2.0 SMD INTERFACE DEFINITION

The SMD disk interface standard started out as a dominant de-facto standard for 14″ OEM Winchester drives and is virtually the basis of 8″-14″ OEM disk drive industry today, with an eye out for the 5¼″ OEM market in the future. It was approved by the ANSI committee (ANSI X3.91), in 1982. The interface consists of a 60-pin twisted pair control (A) cable and a 20-pin data (B) cable with a molded foil ground plane on one side. The 'A' cable is responsible for all head movements, status reporting and issuing commands, while the 'B' cable is used for reading and writing NRZ data. The 'A' cable assignments are shown in *Figure 1.* Address and Control functions are transferred on ten BUS OUT lines. The significance of the information on these lines is indicated by one of the six TAG functions as shown in *Figure 2.* Status for real time control, device identity and current sector status are returned on eight BUS IN lines. Drives are selected by separate UNIT SELECT lines on the 'A' cable, which have their own strobe line, UNIT SELECT TAG. All TAG lines except UNIT SELECT TAG are gated by the UNIT SELECTED signal, unit referring to the drive. The 'B' cable (Data) I/O signal assignments are shown in *Figure 1.* This cable essentially handles the transmission of data and clock information, which could be at very high transfer rates. The 'A' interface cable may be connected to the controller in a star-chained mode or daisy-chained mode. Most of the drive manufacturers support a dual channel option, where the drive could be accessed by two controllers. This is controlled by three special signals on the 'A' cable—PRIORITY SELECT, BUSY and RELEASE lines.

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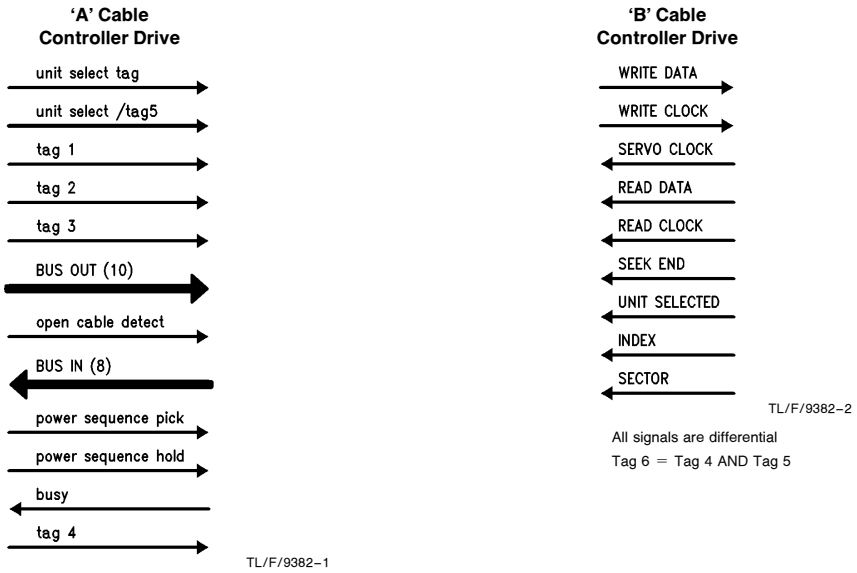

FIGURE 1. SMD Interface Cable Assignments

All input and output signals are differential in nature, and utilize industry standard transmitters and receivers. When used with properly shielded cables, this interface provides a terminated, differential transmission system for long distances, up to 50 feet, in noisy electrical environments. The maximum number of drives connected to the 'A' cable is 16. The recommended TTL differential drivers and receivers are the MC3453 and MC3550. The appropriate terminations for the driver/receiver combinations are shown in *Figure 3.* The detailed schematic in the appendix also shows them in the design. There are certain drives like CDC's 9772-XMD drive (24 MHz), where the high data rates and timing requirements at the drive necessitate the use of ECL drivers and receivers, with the appropriate terminations. The schematic in the appendix outlines the connection requirements for these with the appropriate terminations.

3.0 DISK SIDE INTERFACING

In the SMD interface it is fairly obvious that a lot of control is necessary to perform even a simple operation. The disk controller must perform simultaneous operations on both cables, as well as monitor status signals to determine if the command was executed properly. The disk controller board essentially provides a connection from the drive-level interface to the system. Its main functions are to handle the disk's control and data path, to transfer data between the disk and the system. The Disk Controller interfaces to the disk drive at one end and the main system at the other end. On the disk side the DDC interface to the drive can be broken down into two main paths—control path and data path. The control path essentially comprises of the 'A' cable signals on the SMD interface. These are differential in nature and require differential drivers/receivers to drive the cable between the chip and the interface connectors. The local μP has to activate and monitor the control lines in a certain sequence to achieve a desired operation, defined by the SMD protocol. The interface is activated by asserting the OPEN CABLE DETECT signal. This signal is sent through two drivers paralleled and the regular termination resistor is omitted. The first task then is to select the drive using the UNIT SELECT lines, latching them with the UNIT SELECT TAG. UNIT SELECTED is asserted by the drive indicating the selection of the drive. The unit is checked to see if it is ready for the next operation by monitoring the READY line. Once ready, the head and cylinder addresses are provided to place the drive's head assembly at the desired position on the media, and then the desired sector of data is sought. On arriving at the desired sector, the read/write operation is performed. In case of an unsuccessful operation, an error condition is flagged which could be determined by reading the status and monitoring other signal lines. *Figure 4* gives a detailed flow chart of the sequence of drive control operations performed by the local μP for the SMD interface standard. The status information presented on the interface is a function of the various TAG lines as seen in *Figure 2.*

Bus Out Bit	Unit Select Tag	Tag1 (cyl se.l)	Tag2 (head and upp cyl sel)	Tag3 (control sel)	Tag4 (curr sector)	Tag5 (extnd status)				Tag6 (Device Type)
0		2^0	2^0	Write Gate	0	0	1	0	1	0
1		2^1	2^1	Read Gate	0	0	0	1	1	0
2		2^2	2^2	Servo Offset +	0	0	0	0	0	0
3		2^3	2^3	Servo Offset −	0	0	0	0	0	0
4		2^4	2^4	Fault Clear	0	0	0	0	0	0
5		2^5		AME	0	0	0	0	0	0
6		2^6		Return to Zero	0	0	0	0	0	0
7		2^7	2^{10}	dztz str (Early)	0	0	0	0	0	0
8		2^8	2^{11}	dztz str (Late)	0	0	0	0	0	0
9		2^9		Release	0	0	0	0	0	0
						①	②	③	④	

Bus in Bits	Drive Status	curr sector cnt	Fault Status ①	Operating Status ②	Diagnostic Status ③	Diagnostic Execute Status ④	Device Type Status (User Defined)
0	Unit Ready	2^0	RD * WR				
1	On Cylinder	2^1	(RD + WR) * oncyl				
2	Seek Error	2^2	First Seek				
3	Fault	2^3	Write				
4	WR Protect	2^4	WR * WR Protect				
5	AMF	2^5	Head Select				
6	Index Mark	2^6	Voltage				
7	Sector Mark	2^7	Valid Status Available			tst	

FIGURE 2. Tag Bus Decode Information Available on the 'A' Cable

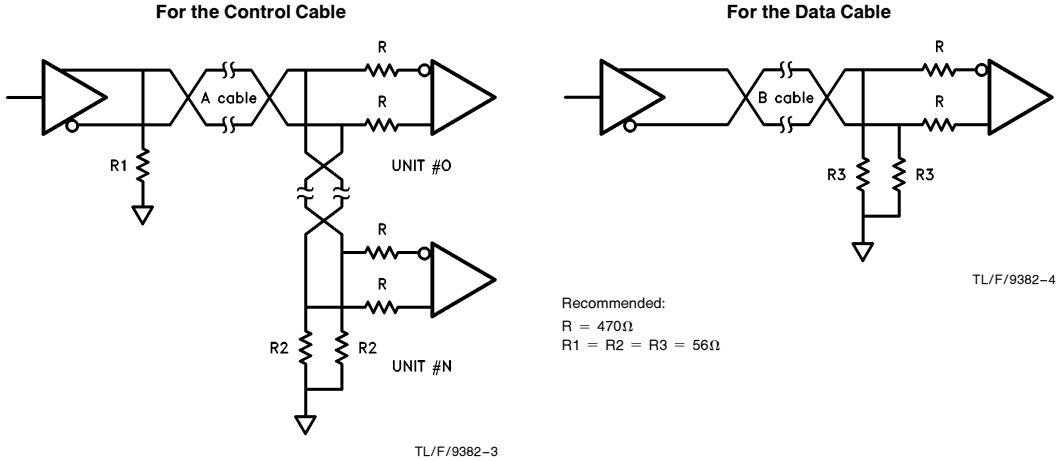

FIGURE 3. Driver/Receiver Combinations with the Appropriate Terminations for 'A' and 'B' Cable

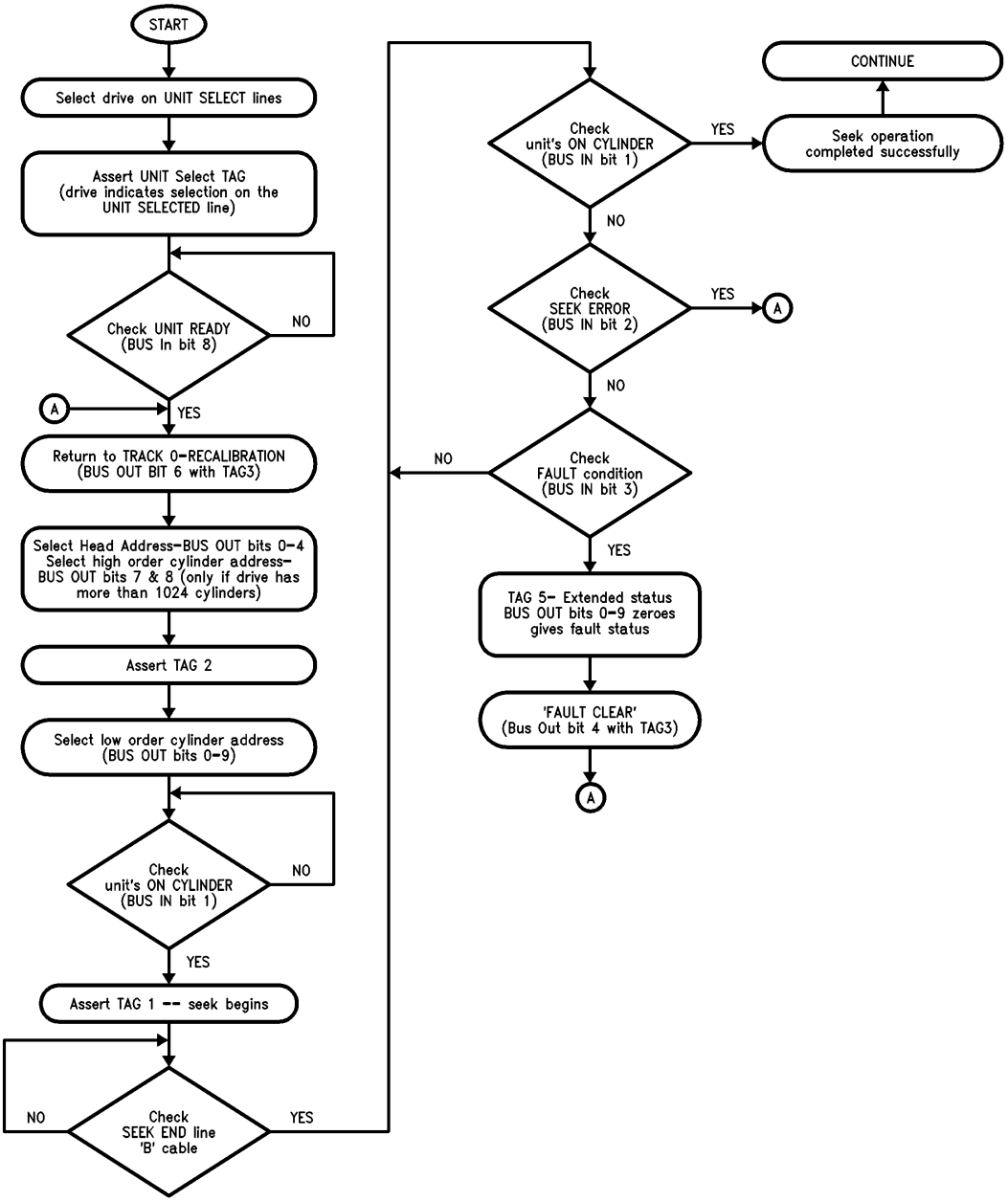

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FIGURE 4. Control Path—Flow of Operations

The other component of the Disk Controller system is the data path. The SMD 'B' cable essentially contains the data path signals to the drive. It consists of lines to transmit serial NTZ data to and from the drive. Associated with the read/write lines are the clocks: Read Clock for reading data, Write Clock for writing data and a Servo Clock synchronous with the rotation of the spindle, for reference. Additional signals help in determining the status of each drive on the bus. The main component of the data path in a disk controller system is the Disk Data Controller IC, like the DP8466A. The DDC can be programmed to operate in accordance to the SMD interface specification for the associated operations like formatting, reading and writing. Read Gate and Write Gate are the two main read/write control signals in the data path. Write Gate enables the write operation and is validated only when UNIT READY, ON CYLINDER, SEEK END are false. If Write Gate is asserted under any other conditions, a fault occurs and writing is inhibited. There are also certain drive dependent constraints which affect the read/write timing and must be taken care of. Listed below are some of them. Details can be found in the SMD specification.

1. write circuit turn-on delay
2. head select transients
3. read after write transients
4. read/write—encoding/decoding delays
5. write after read transients
6. PLL synchronization time

The DDC supports most of the specifications of the SMD standard, however there are certain specifications that the DDC does not directly support. These can be taken care of through software or with the help of external logic. A discussion of these considerations is given in the following sections.

4.0 HANDLING THE SMD RECOMMENDED FORMAT AND INTERFACE SPECIFICATIONS

Figure 5 shows the recommended format for SMD drives. There are certain fields in the format which are not directly supported by the DDC, which however can be implemented as discussed below.

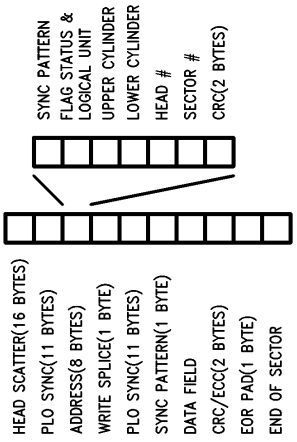

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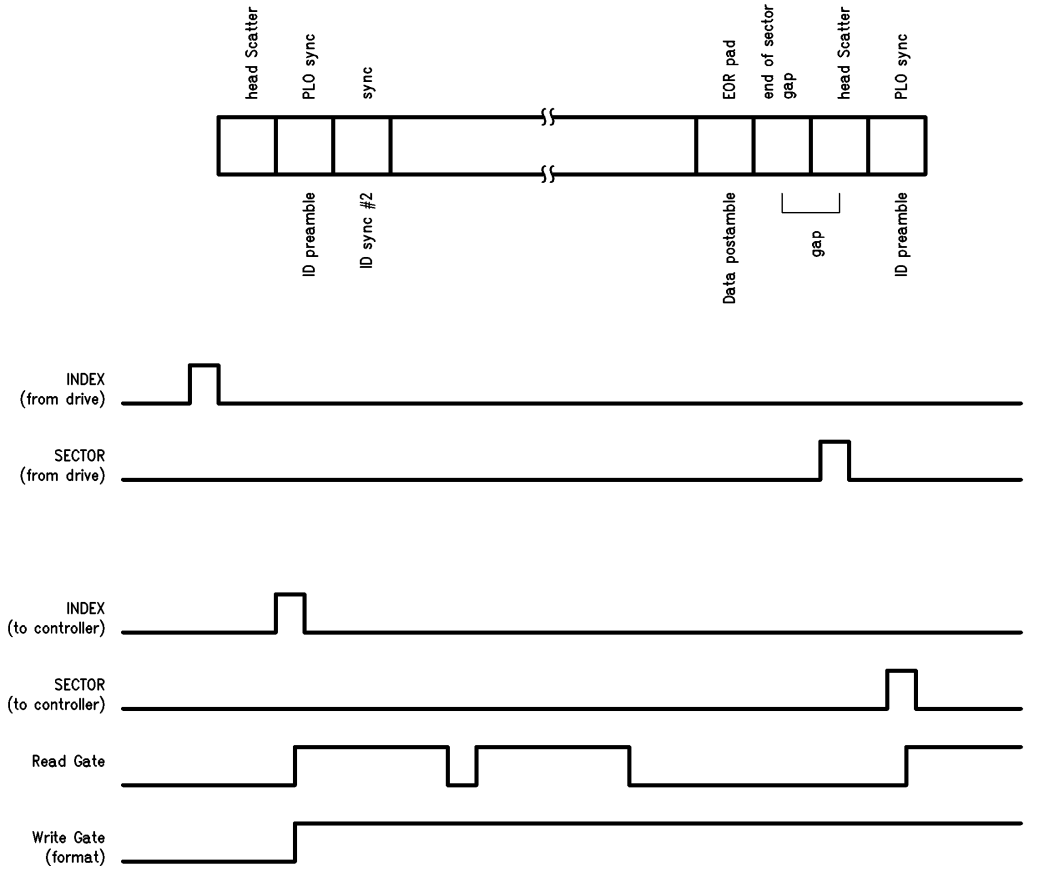
FIGURE 5. SMD Recommended Format (Hardsectored)

4.1 The Write Splice Field

The SMD format specification recommends a zero byte header postamble, a one byte write splice field and an eleven byte data preamble, (PLO sync field). The DDC does not support a separate register for the write splice field between the header and the data segments in its format parameter RAM. However this can be easily taken care of by the programmable format feature of the DDC. The format parameter registers are programmed to have a 12 byte data preamble, one byte longer than the desired length. This byte is considered for practical purposes as the write splice. Hence when formatted this will have the same pattern as the data preamble. During a write operation, this byte is kept as part of the data preamble and with the standard requirement of 8 clocks write propagation delay in the drive (due to write circuitry), the data gets written on the media beyond the write splice field, at the correct place in the preamble. In case of a read operation, this byte is considered to be part of the header postamble. Since the DDC asserts read gate 11.5 bits into the data preamble, it will never be asserted in the write splice. In this manner the write splice field can be implemented to support the recommended SMD format specification. It should be noted however that it is mandatory to use at least a one byte header postamble with the DDC for proper operation.

4.2 The Post Index/Sector Gap Field (Head Scatter)

The recommended format in the SMD standard supports a gap felled after the index/sector pulse, referred to as the post index/sector gap or head scatter. This is necessary mainly to accommodate drive dependent transients as mentioned earlier. The DP8466A does not support a separate field for this gap and also uses the index/sector pulse as a reference for the read/write control signals. To implement this gap field, an external counter is used to delay the index/sector pulse from the drive, by the desired gap count, before presentation to the DDC. The circuitry to achieve this is shown in the schematic in Appendix A. Since the index/sector pulse is presented to the DDC delayed by the length of the Head Scatter field, at the time it starts writing the PLO field etc., it's at the right area on the media. The gap field at the end of the sector is written till a sector pulse is received by the DDC. Hence the gap pattern gets written for the Head Scatter field of the next sector. *Figure 6* shows the details of this technique and the manipulation of the parameter fields.



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The disk controller writes the end of sector gap over the head scatter area, hence achieving the writing of the post index/sector gap. The last sector overlaps to write the head scatter for the first sector.

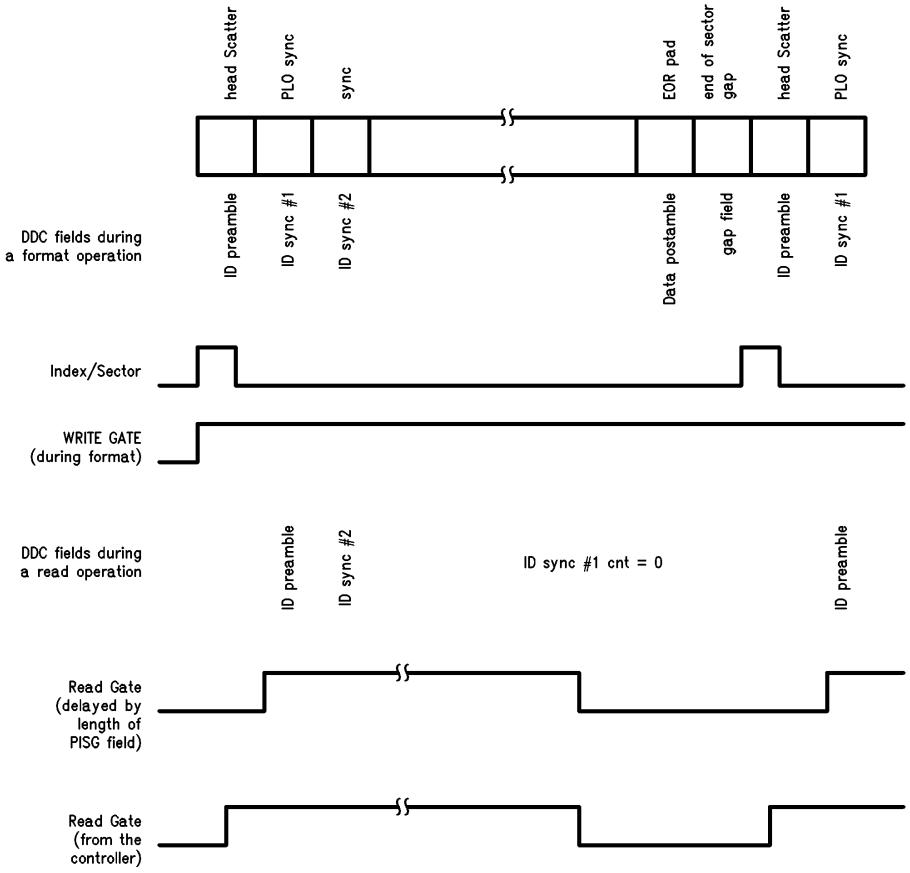
FIGURE 6. PISG Implementation (Technique 1)

4.3 Read/Write Gate Timing Restrictions

On assertion of Write Gate, there is a write splice before data is actually written on the media. Hence when reading the data, it must be ensured that Read Gate is asserted sometime after the write splice. In the DDC the delay between Write and Read Gate in the Data field is 8.5 bit times, which satisfactorily covers the write splice. However at the beginning of the sector it is only 0.5 bit times, hence Read Gate would have to be delayed to prevent assertion of the Read Gate during the write splice. This would be a problem only in the first sector after the index pulse, as during a format operation Write Gate remains asserted till the Index pulse is encountered again. This is done by delaying the Read Gate by 8 bits from the DDC to the drive, using a counter as shown in the schematic in the appendix. This results in the read gate assertion delayed by a byte even in the data field which does not make any difference to the performance.

4.4 Alternative Technique to Implement the Shortcomings in Section 4.2 and 4.3

An alternative technique to implement the Post index/sector gap and the problem of asserting read gate in splice at the beginning of the sector is to have a single delay circuit which delays the read gate qualified by index/sector, assertion to the drive by the length of this gap. The manipulations of the DDC fields to achieve this is shown in *Figure 7.*



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Note: Read Gate assertion needs to be delayed only at the index or sector pulse.

FIGURE 7. PISG Implementation (Technique 2)

4.5 MUXing the Two Clocks on the SMD INTERFACE 'B' CABLE

The 'B' cable has two clock outputs— the SERVO CLOCK and the READ CLOCK. The SERVO CLOCK signal is a phase locked clock, (frequency dependent on the drive), generated from the servo track bits and is available at all times. The READ CLOCK signal defines the beginning of a data cell and is synchronous with the detected data. This signal is derived from the SERVO CLOCK. At the start of a read operation, READ GATE is asserted by the controller. This initiates the PLL on the drive to begin locking on the data from the media. Till this point, the clock sent to the controller is the reference clock (similar to the SERVO CLOCK frequency). When the PLL achieves phase lock, the clock transmitted on the READ CLOCK line to the controller is the one in phase sync with the data. An undefined clock may be transmitted at the point of obtaining phase sync, upon initiating or ceasing a read operation. Read Clock is in phase sync within 2.5 μs after Read Gate is asserted, (worst case). Also the WRITE CLOCK generated by the DP8466A is essentially the SERVO CLOCK retransmitted to the drive synchronized to the NRZ Write Data. The DP8466A has only one clock input line (READ CLOCK). Hence the switching of the SERVO or READ CLOCK to the DP8466A must be done externally. Also since the DP8466A's clock input cannot accommodate short pulses, this switching must be done without short pulses. The external circuitry to multiplex the two clocks and the deglitcher is shown in the schematic. This can safely operate up to clock frequencies of 25 MHz. To take care of the undefined pulse occurring on obtaining phase sync, the Read Gate signal delayed by 3 μs (to accommodate worst case lock time), is used as the 'switch' control input.

4.5.1 GLITCHLESS CLOCK MULTIPLEXER CIRCUIT

With Read Gate active (high), the source of the 8466 Read Clock is the Read Clock input signal. When Read Gate is inactive, the 8466 Read Clock will come from the Servo Clock input. If the switching between the two clocks would result in a less-than-normal-width pulse in a simple multiplexer, this glitchless circuit allows the currently active clock to finish a full one or two clock pulses before the output goes low and waits one or two clock times until the new clock appears at the ''8466 Read Clock'' output. So there may be one or two missing pulses but there will never be a ''glitch'' (narrow pulse width).

If the disk system also uses the National Semiconductor DP8463B (2, 7) RLL ENDEC, no external circuitry is required as this glitchless multiplexer is already incorporated into the DP8463B.

5.0 SYSTEM CONSIDERATIONS AND CONCLUSIONS

The DP8466A supports a dual channel onboard DMA controller which simplifies the task of interfacing to any system bus. System design considerations are flexible to the designer as outlined in the Application Note: ''Designing an ESDI Disk Controller system with National's DP8466A'' and AN-413. An effort has been made in this application note to introduce the designer to the SMD interface, and explain the intricacies of designing to its specifications with the DP8466A. The emphasis was on the disk side design and a representative design of the disk side is included in the appendix. This is the disk side for a disk controller designed for the 25 MHz XMD drive from Control Data Corporation. The board was built and tested in the Labs at National and was found to perform satisfactorily. For more details on the SMD standard, refer to the ANSI document on SMD interface specifications. For more details on the DP8466A refer to AN-413 and the datasheet.

GLITCHLESS MULTIPLEXER

Block Diagram

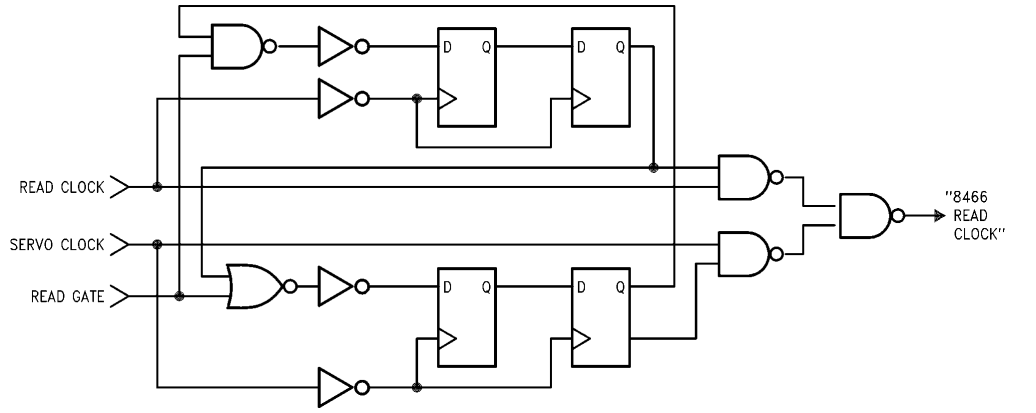

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FIGURE 8. Glitchless Multiplexer

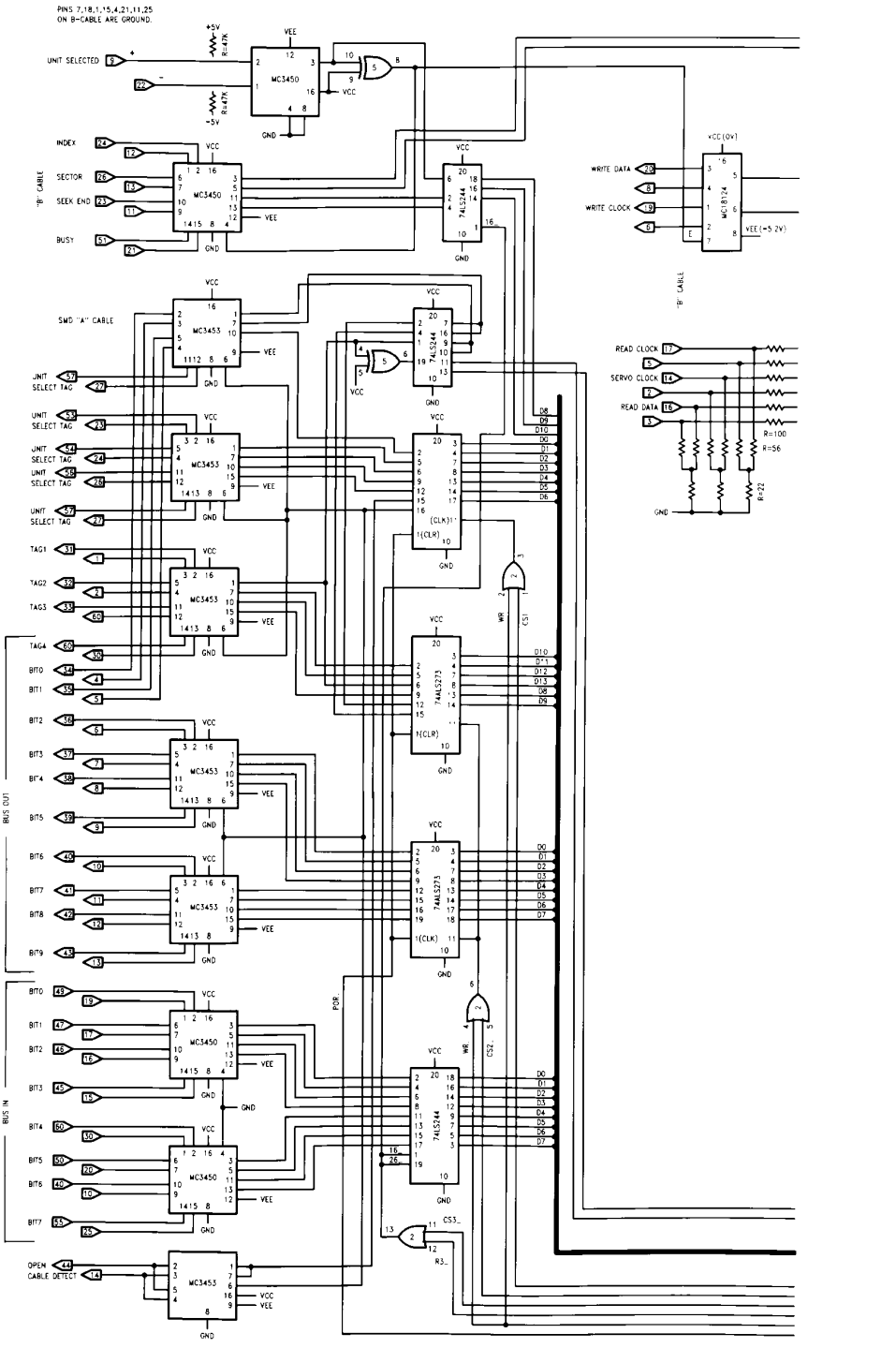

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FIGURE 9

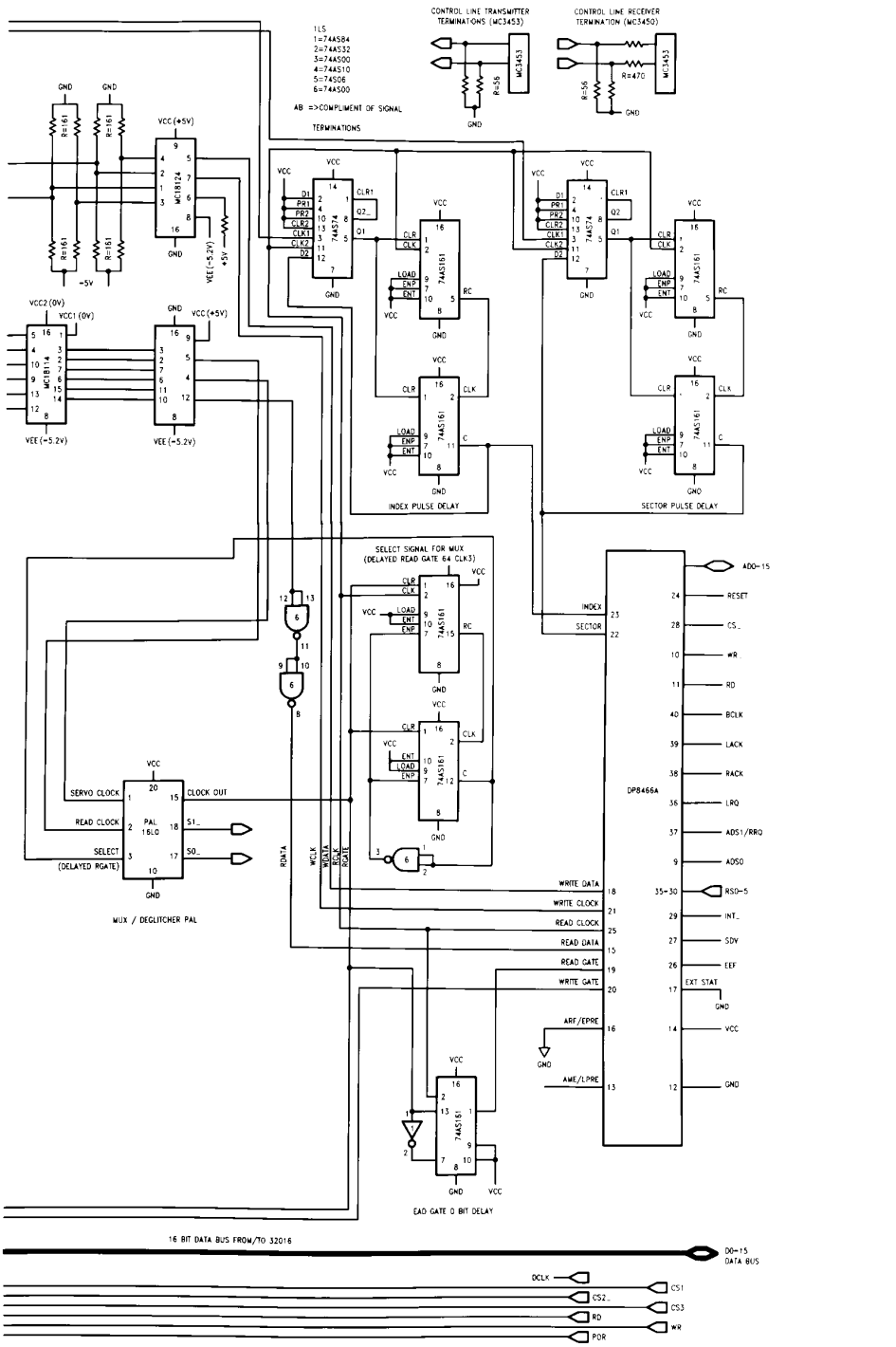

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FIGURE 9 (Continued)

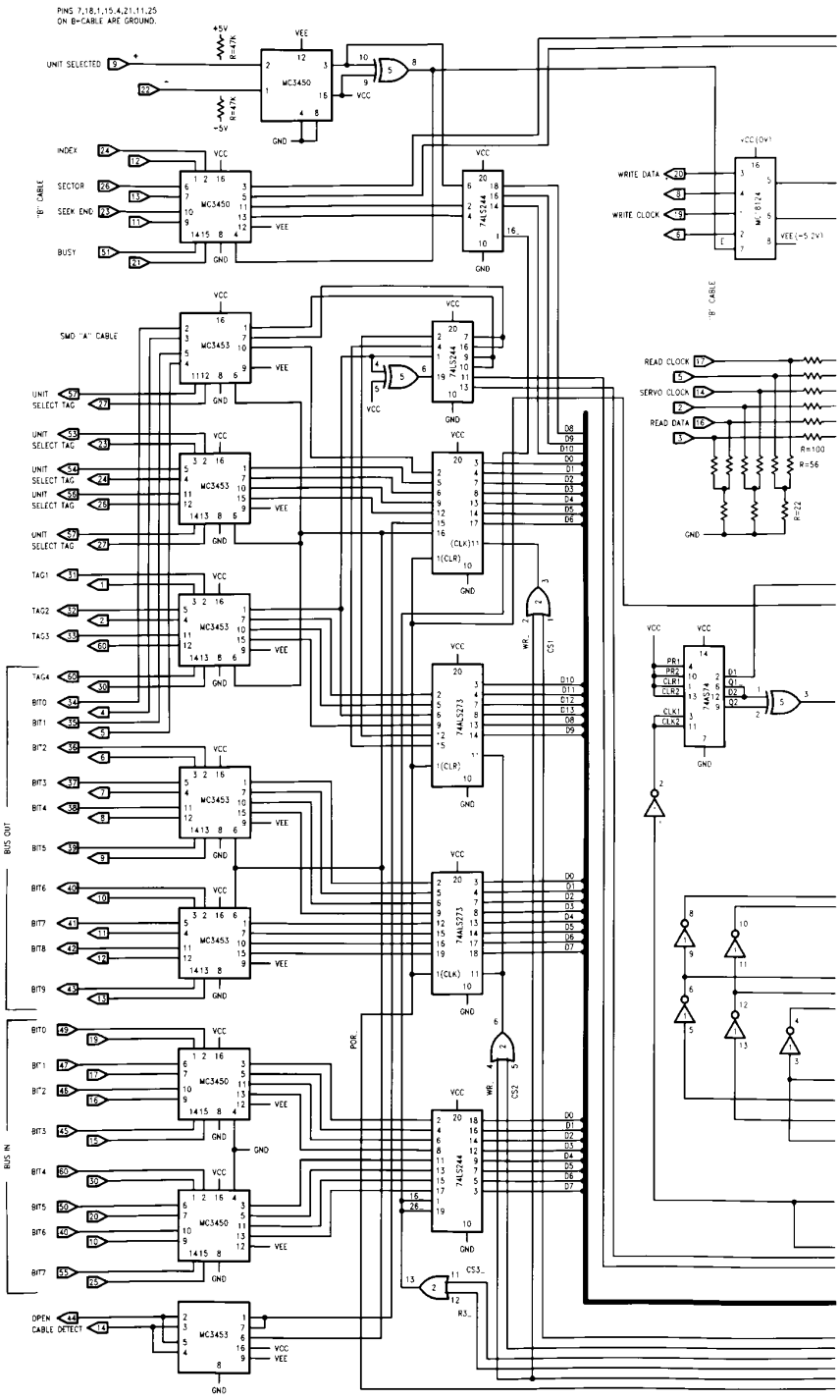

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FIGURE 10

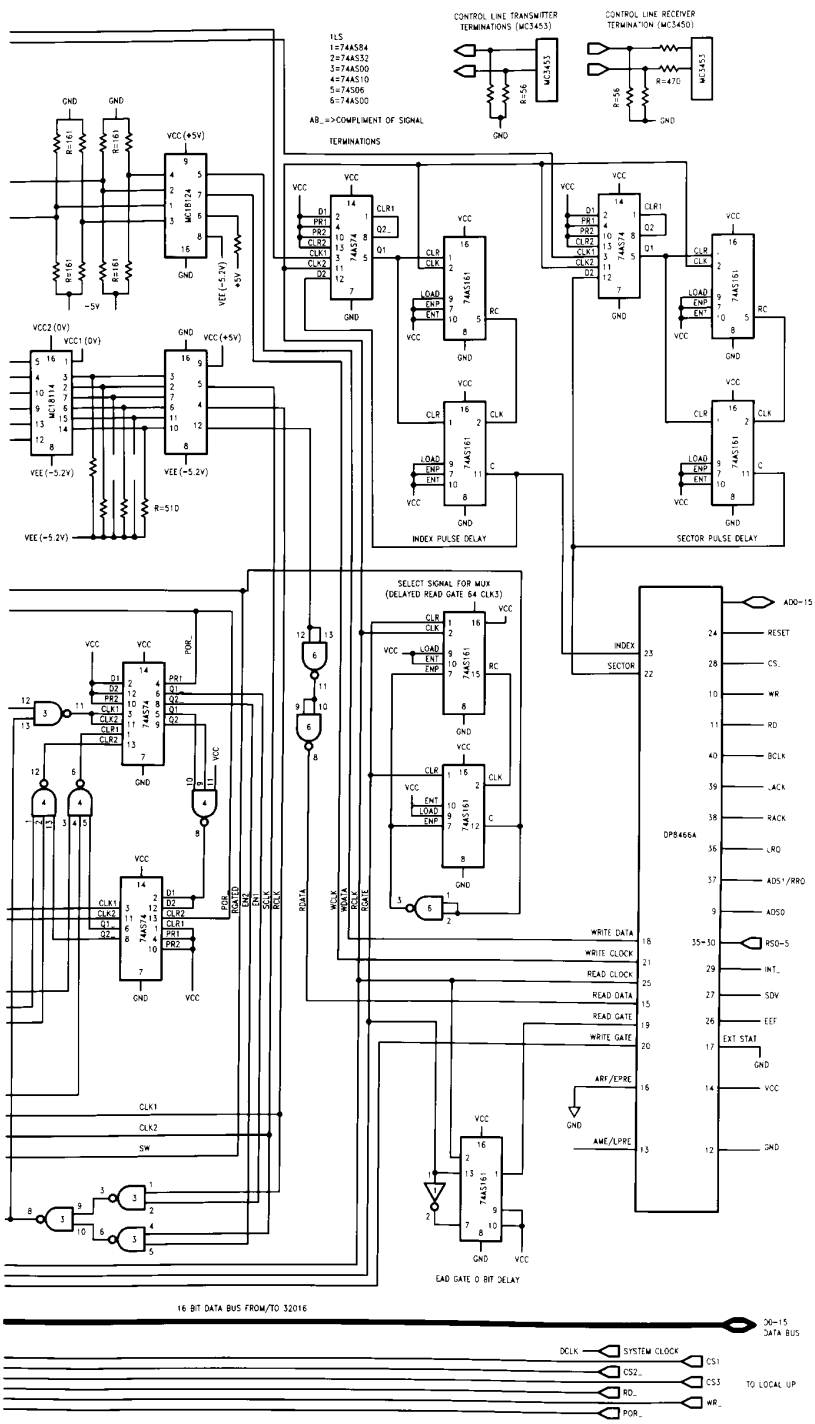

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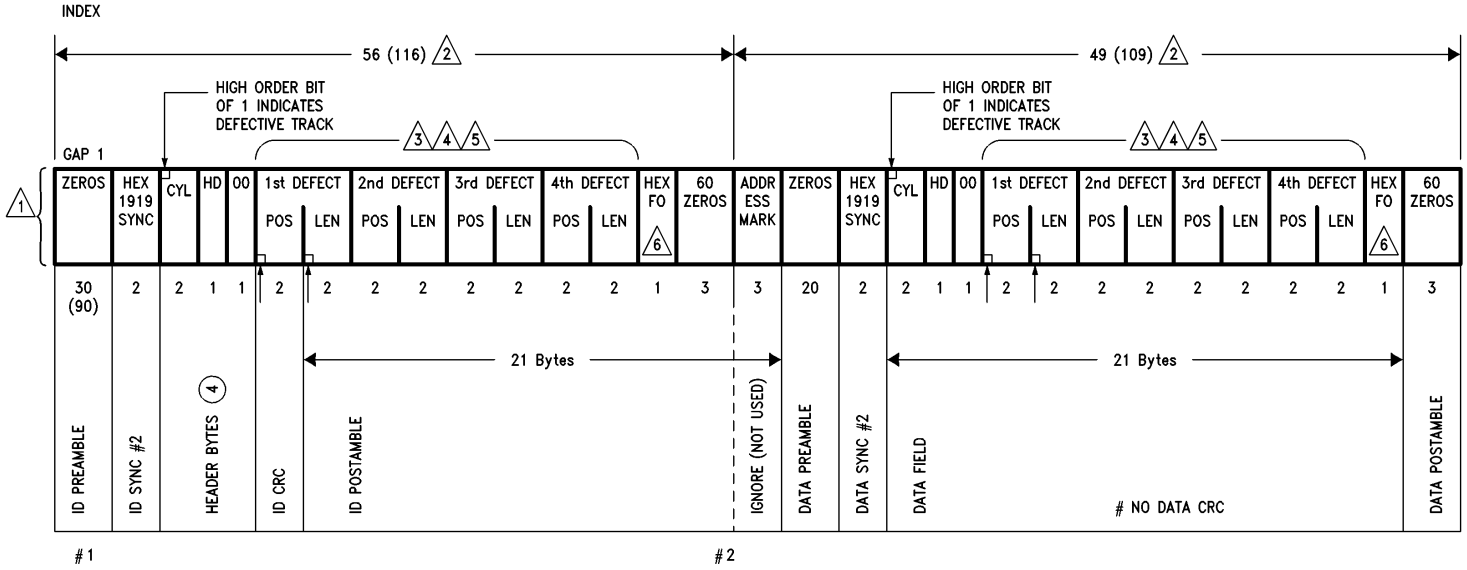
FIGURE 10 (Continued)

Defect List Format (SMD Drives)



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Notes:

No data CRC is selected, OPERATION is IGNORE HEADER—READ DATA

If in case of a defect, so that #1 field becomes 90 and #2 field becomes 60 then it poses no complications for reading the defect information. However if the defect format is to be written again then it might cause complications as the max. byte count for a field is 32 bytes, hence cannot be done unless delayed physically.

Under no conditions can sync #1 be used with a pattern of zeroes. Its count must be kept zero.

Note that this technique to enable the DP8466 to be able to read the defect list format is possible only if written in two parts originally. HITACHI, NEC and CDC support the above but *not FUJITSU*.

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