LVDS Performance: Bit Error Rate (BER) Testing Test Report #2

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LVDS CABLE DRIVING PERFORMANCE

This report provides the results of a series of Bit Error Rate tests performed on the DS90C031/2 LVDS Quad Line Drive/ Receiver devices. Four drivers were used to drive 1 to 5 meters of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

The questions of: How Far? and How Fast? seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about the cable, connector, and information about the printed circuit board (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be the best test set up. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and Bit Error Rate tests (BER).

WHAT IS A BER TEST?

Bit Error Rate testing is one way to measure the performance of a communications system. The standard equation for a bit error rate measurement is:

$$\text{Bit Error Rate} = \frac{\text{(Number of Bit Errors)}}{\text{(Total Number of Bits)}}$$

Common measurement points are bit error rates of:

$\leq 1 \times 10^{-12} \rightarrow$ One or less errors in 1 trillion bits sent

$\leq 1 \times 10^{-14} \rightarrow$ One or less errors in 100 trillion bits sent

Note that BER testing is time intensive. The time length of the test is determined by the data rate and also the desired performance bench mark. For example if the data rate is 50 Mbps, and the bench mark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

BER TEST CIRCUIT

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as shown in *Figure 1*. This figure details the test circuit that was used. It includes the following components:

PCB#1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) 28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report cable lengths of 1 and 5 meters were tested.

PCB#2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is a AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

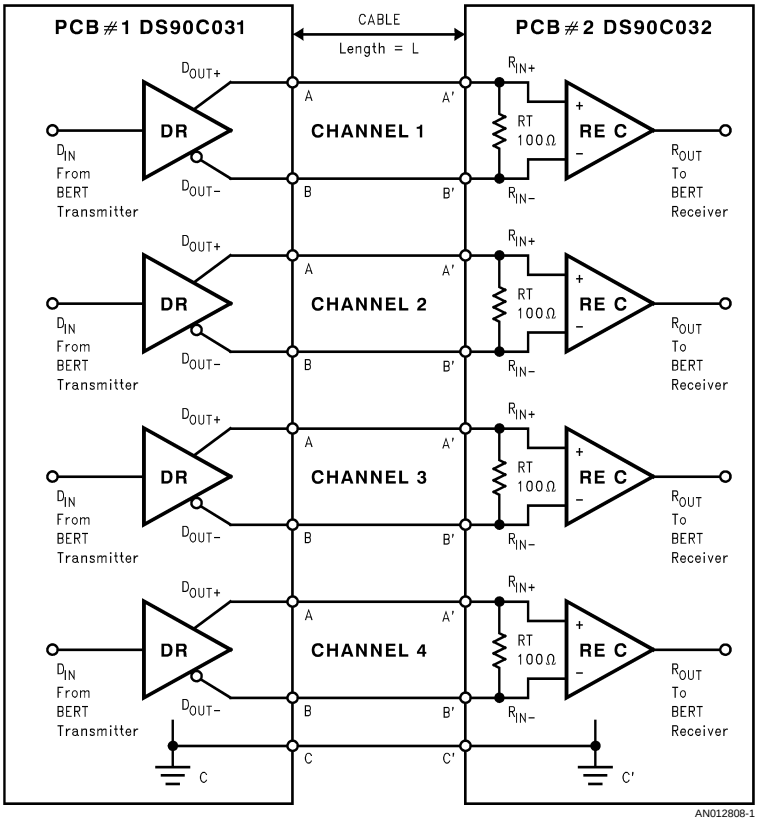

FIGURE 1. LVDS BER Test Circuit

TEST PROCEDURE

A parallel high-speed BER transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The BER tester was configured to provide a PRBS (Pseudo Random Bit Sequence) of $2^{15} - 1$ (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4 bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded, which included: elapsed seconds, total bits transmitted, and the number of bit errors recorded. For the three tests documented below, a power supply voltage of +5.0V was used, and the tests were conducted at room temperature.

TESTS AND RESULTS

The goal of the tests was to demonstrate error rates of less that $< 1 \times 10^{-12}$ are obtainable.

TEST #1 Conditions:

Data Rate = 50 Mbps

Cable Length = 1 meter

PRBS Code = $2^{15} - 1$ NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a SOS (Simultaneous Output Switching) condition on the device.

TEST #1 Results:

Total Seconds: 87,085 (1 day)

Total Bits: $1{,}723 \times 10^{13}$

Errors = 0

Error Rate = $< 1 \times 10^{-12}$

TEST #2 Conditions:

Data Rate = 100 Mbps

Cable Length = 1 meter

PRBS Code = $2^{15} - 1$ NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #2 Results:

Total Seconds: 10,717 (~3 hr.)

Total Bits: 4.38×10^{12}

Errors = 0

Error Rate = $< 1 \times 10^{-12}$

TEST #3 Conditions:

Data Rate = 100 Mbps

Cable Length = 5 meter

PRBS Code = $2^{15} - 1$ NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

TEST #3 Results:

Total Seconds: 10,050

Total Bits: 4×10^{12}

Errors = 0

Error Rate = $< 1 \times 10^{-12}$

CONCLUSIONS

All three of the tests ran error free and have demonstrated low bit error rates using LVDS technology. Thus the tests concluded error rates of $< 1 \times 10^{-12}$ can be obtained at 100 Mbps operation across 5 meters of twisted pair cable. BER tests only provide a Go–No Go (Pass-Fail) data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in the tests conducted by increasing the cable length from 1 meter to 5 meters, and also adjusting the data rate from 50 Mbps to 100 Mbps. Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and by applying heat/cold to the DUT (Device Under Test). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e. 24 hours). BER tests conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal. BER tests do not measure the signal fidelity on the LVDS interconnect directly. Additional tests are recommended to conclude that the signal quality on the interconnecting media also meets system requirements.

REFERENCES

To probe further the following National Semiconductor Application Notes are recommended which are all located in the INTERFACE Databook:

AN-808 Long Transmission Lines and Data Signal Quality

AN-916 A Practical Guide to Cable Selection

AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report #1

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